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(54) **METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE**

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(57) **ABSTRACT**

There is provided a method of manufacturing a semiconductor device. The method includes forming a plurality of wires on an insulating layer, forming a sacrificial layer between the plurality of wires, forming a cover layer on the plurality of wires and the sacrificial layer, and removing the sacrificial layer formed below the cover layer by using mild plasma having a plasma damage rate to the insulating layer of 0.01 to 0.1 Å/s.

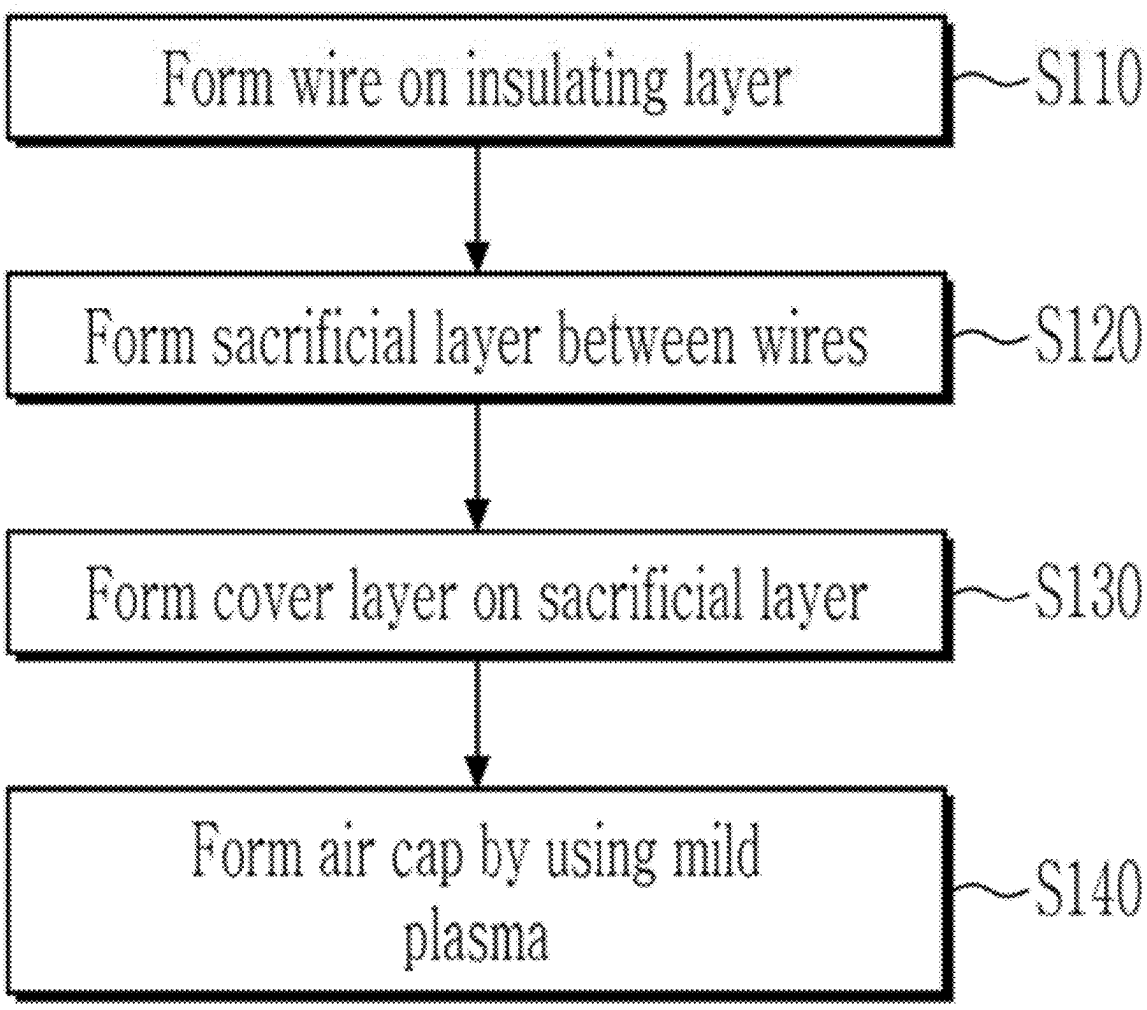


FIG. 1

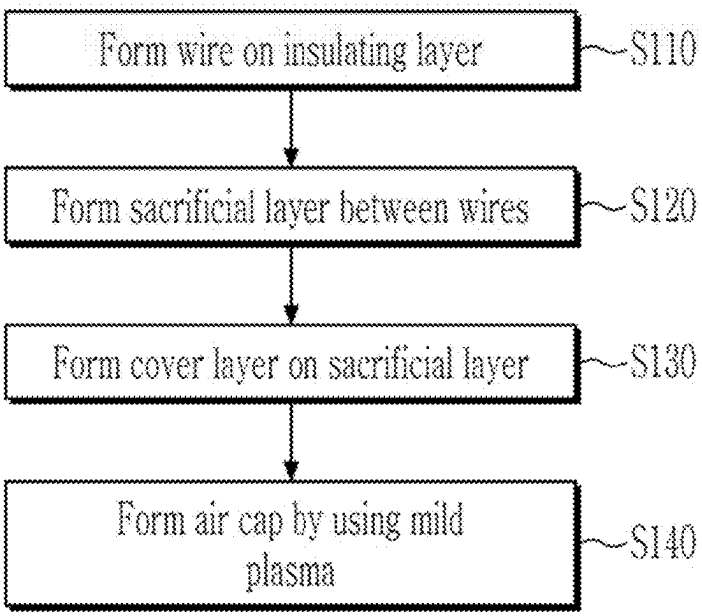

Form wire on insulating layer
S110
Form sacrificial layer between wires
S120
Form cover layer on sacrificial layer
S130
Form air cap by using mild plasma
S140

FIG. 2

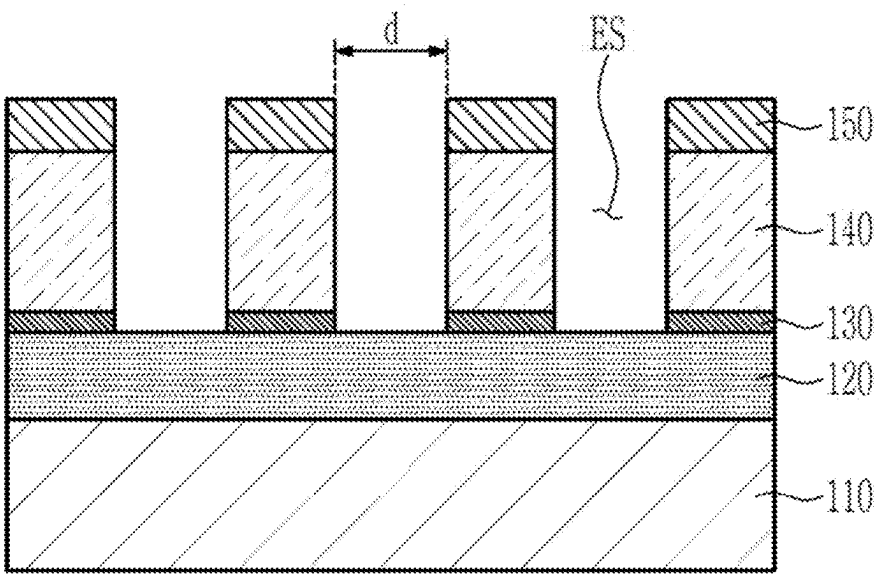


FIG. 3

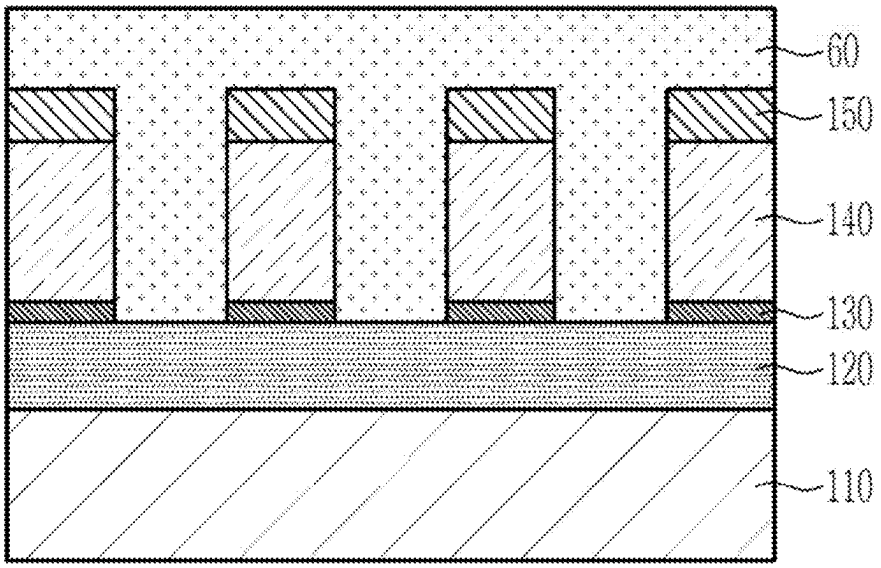


FIG. 4

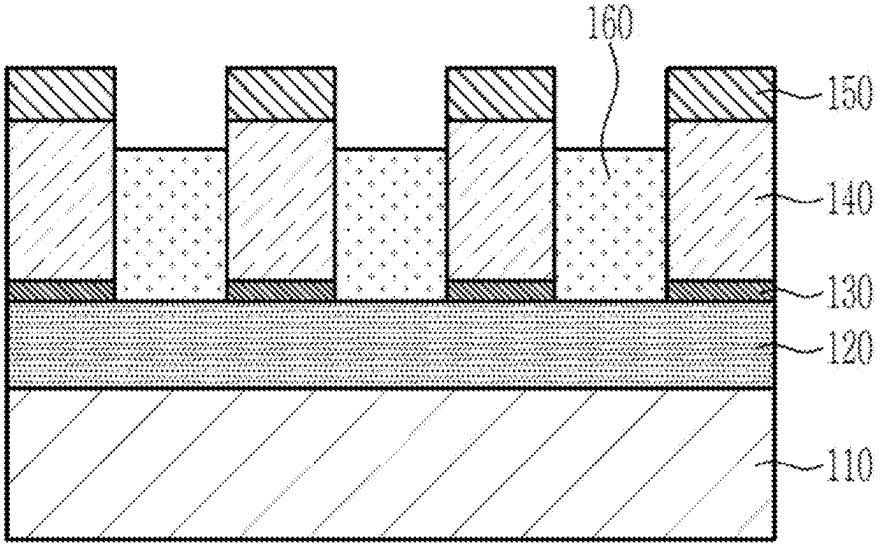


FIG. 5

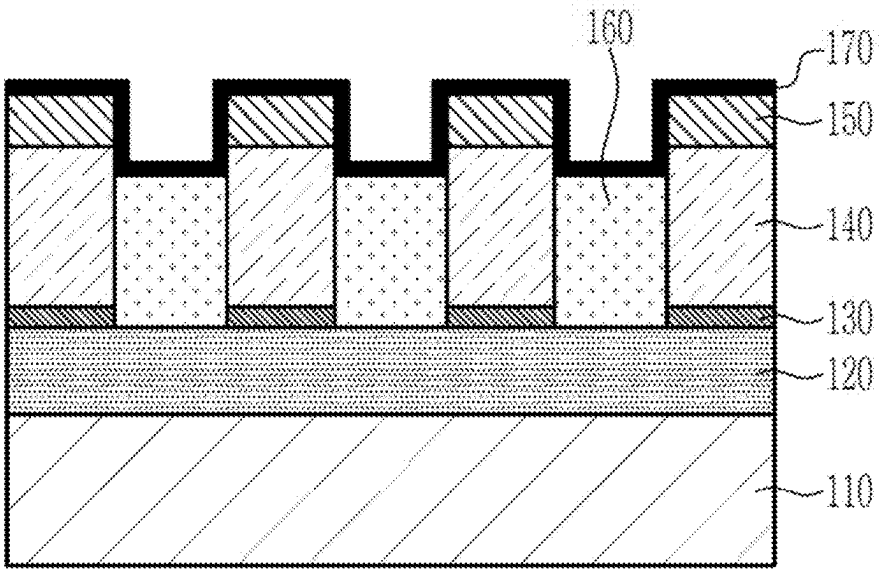


FIG. 6

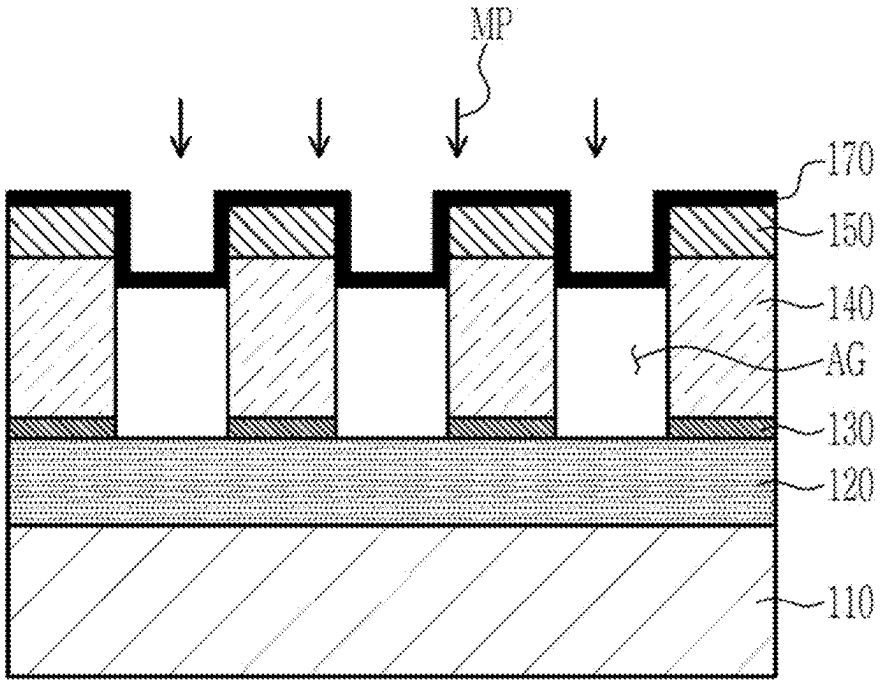


FIG. 7

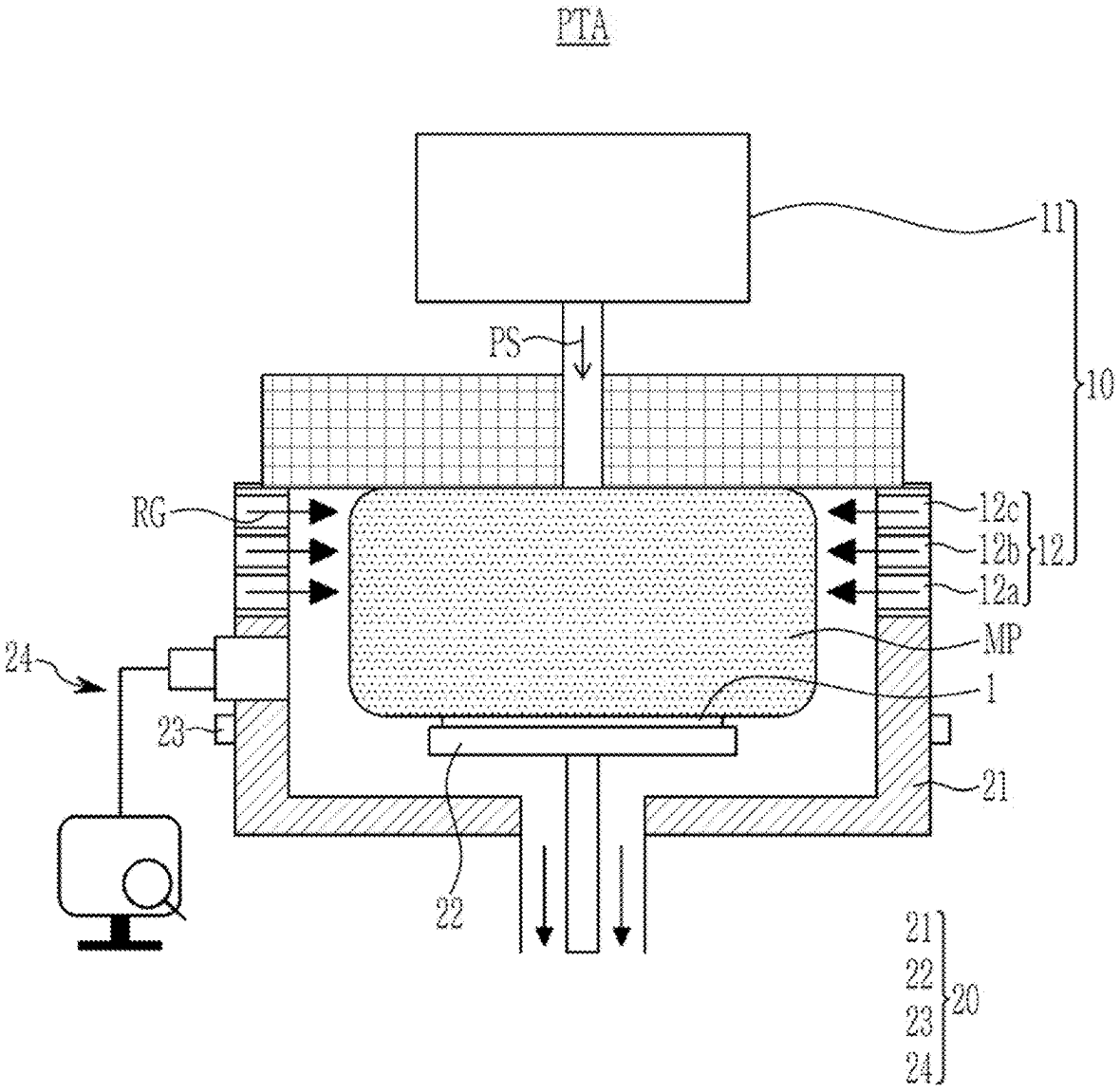


FIG. 8

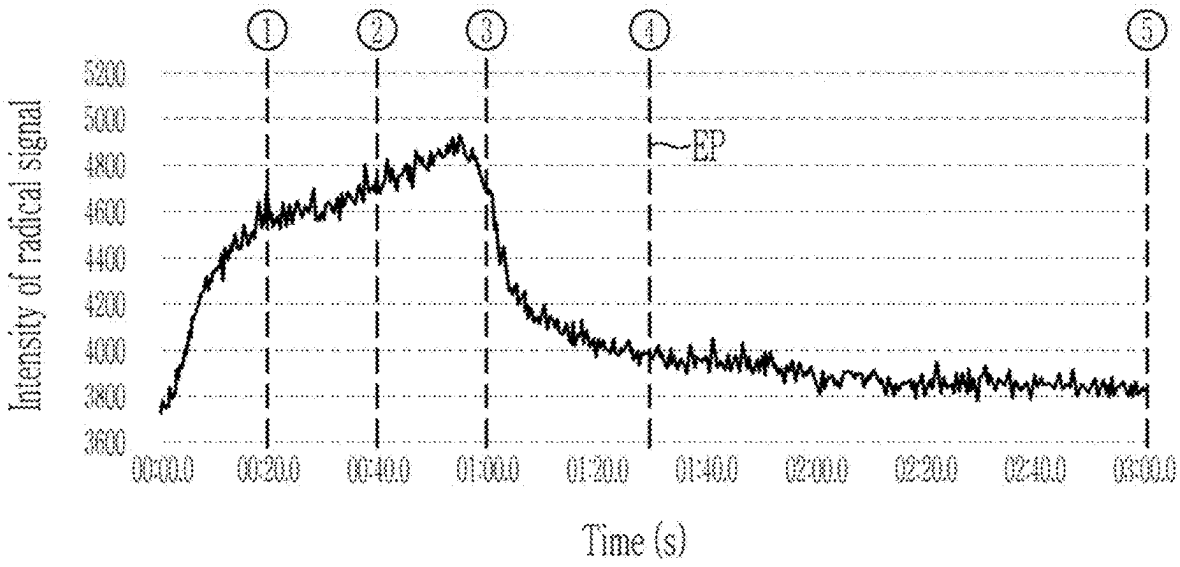

①
②
③
④
⑤
EP
Intensity of radical signal
520
500
480
460
440
420
400
380
360
00:00.0
00:20.0
00:40.0
01:00.0
01:20.0
01:40.0
02:00.0
02:20.0
02:40.0
03:00.0
Time (s)

FIG. 9

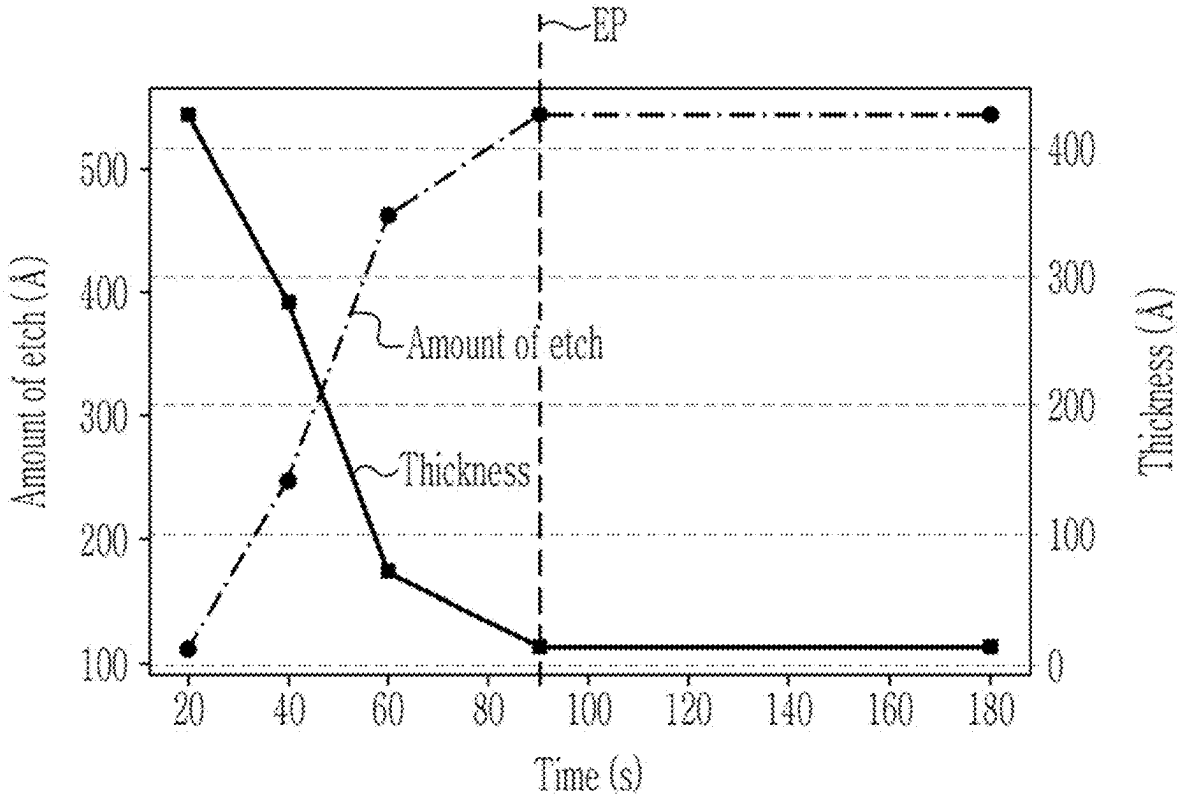

EP
Amount of etch
Thickness
Amount of etch (Å)
Thickness (Å)
Time (s)
500
400
300
200
100
400
300
200
100
0
20
40
60
80
100
120
140
160
180

FIG. 10

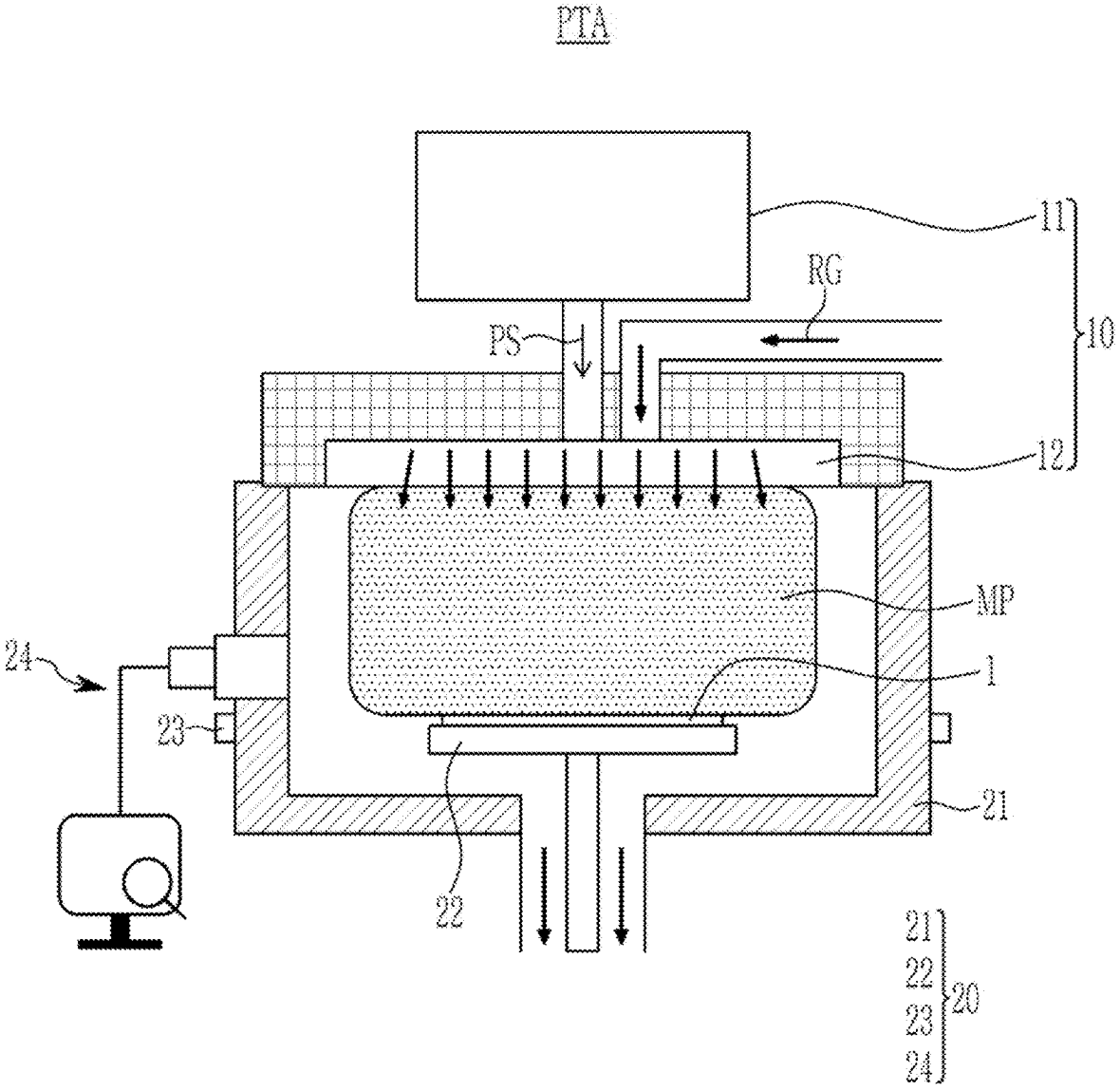


FIG. 11

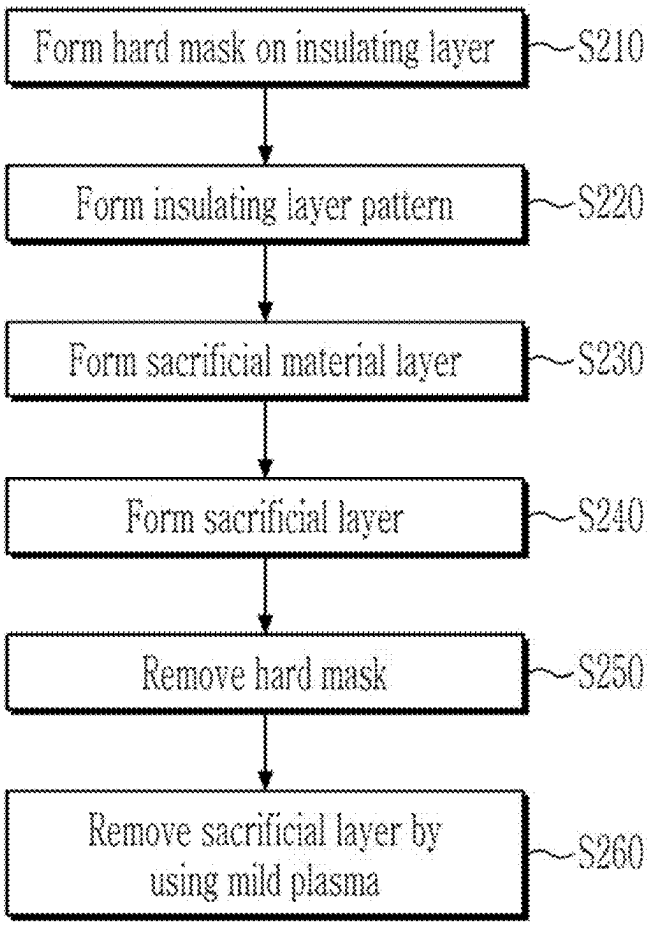

Form hard mask on insulating layer
S210
Form insulating layer pattern
S220
Form sacrificial material layer
S230
Form sacrificial layer
S240
Remove hard mask
S250
Remove sacrificial layer by using mild plasma
S260

FIG. 12

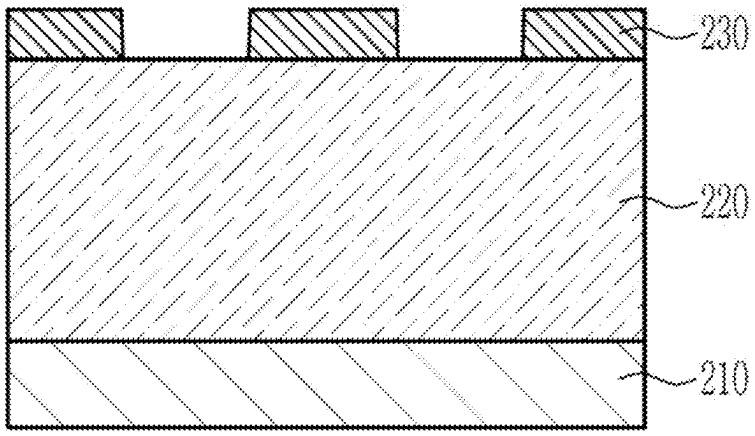


FIG. 13

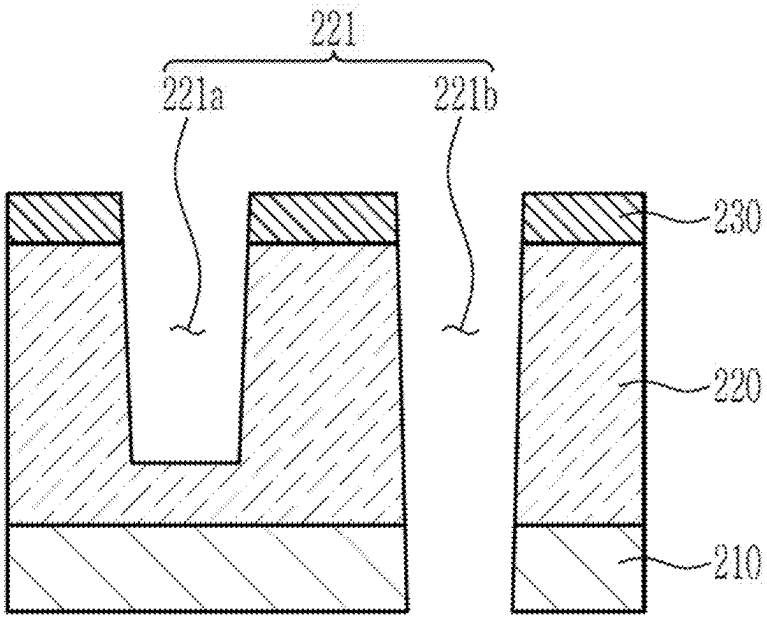


FIG. 14

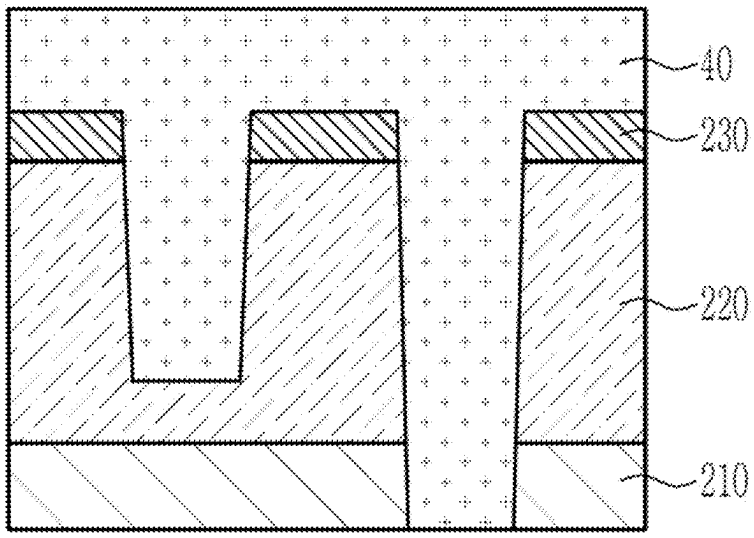


FIG. 15

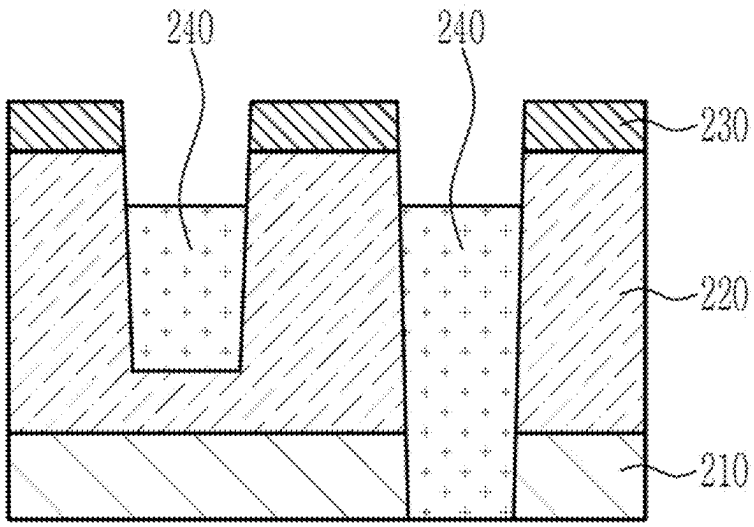


FIG. 16

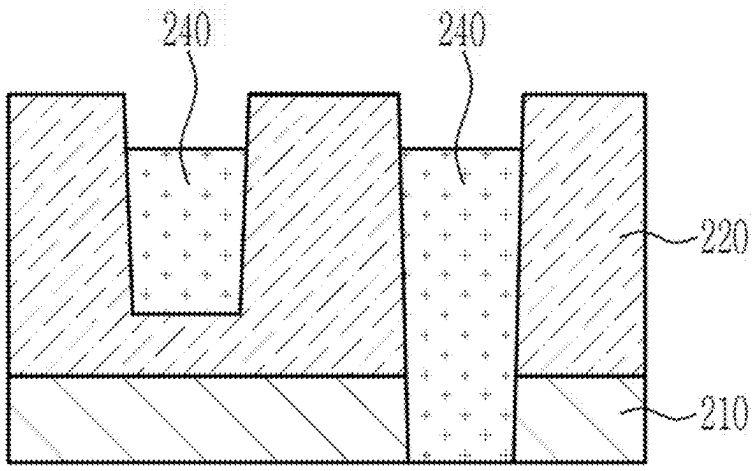
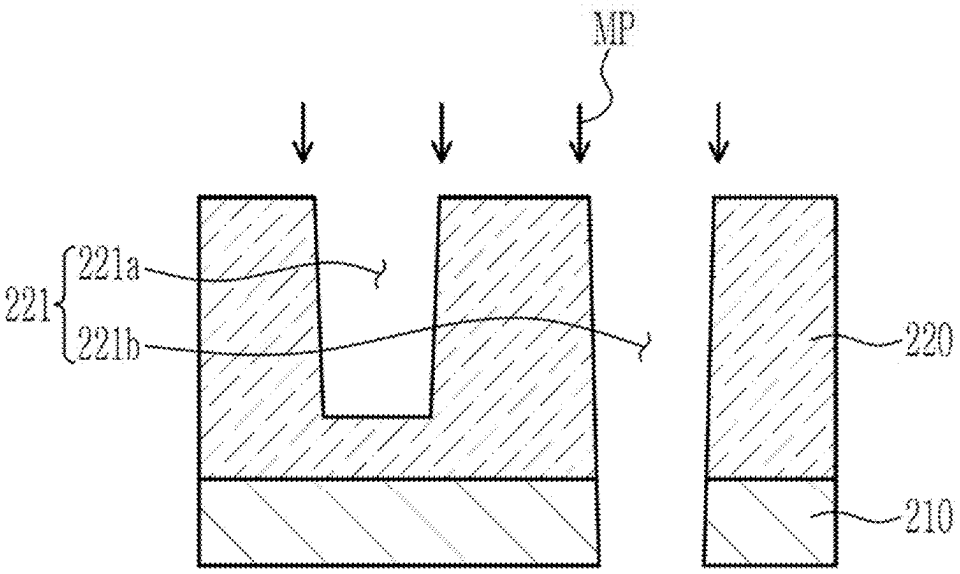


FIG. 17



METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is based on and claims priority to and the benefit of Korean Patent Application No. 10-2024-0021058 filed in the Korean Intellectual Property Office on Feb. 14, 2024, the entire contents of which are incorporated herein by reference.

BACKGROUND

1. Field

[0002] The disclosure relates to a method of manufacturing a semiconductor device, and more particularly, to a method of manufacturing a semiconductor device using plasma treatment.

2. Description of the Related Art

[0003] Semiconductor devices may be manufactured by a variety of semiconductor manufacturing processes including etching, deposition, ashing, or cleaning processes.

[0004] In a front-end-of-line (FEOL) process, which is an initial stage process, for manufacturing a semiconductor device, an air gap structure to improve the signal transmission delay (RC Delay) in the wire. Similar to the FEOL process, a back-end-of-line (BEOL) process, which is a latter process in the manufacturing process of the semiconductor device, is also introducing an air gap structure to improve the signal transmission delay (RC Delay) in the wire.

[0005] In order to form the air gap structure, a sacrificial layer may be removed by pyrolysis. However, when pyrolysis is used to remove the sacrificial layer, a high-temperature heat treatment process is required for a long time. For example, a low-temperature heat treatment process at 400° C. or lower results in a low rate of sacrificial layer removal.

[0006] In addition, when pyrolysis is used to remove the sacrificial layer, real-time process monitoring is not possible, and it is difficult to control the residue substance after the heat treatment process. This can lead to problems, such as leakage current, caused by the residue substance. Moreover, providing additional measures to manage or address these problems may lead to longer process times, which may reduce productivity.

SUMMARY

[0007] One or more aspects of the disclosure provide a method of manufacturing a semiconductor device that is capable of improving productivity by removing a sacrificial layer in a low temperature process using a plasma treatment apparatus.

[0008] According to an aspect of the disclosure, there is provided a method of manufacturing a semiconductor device, the method including: forming a plurality of wires on an insulating layer, the insulating layer provided on a substrate; forming a sacrificial layer between the plurality of wires; forming a cover layer on the plurality of wires and the sacrificial layer; and forming an air gap by removing the sacrificial layer using mild plasma having a plasma damage rate to the insulating layer of 0.01 to 0.1 Å/s.

[0009] According to another aspect of the disclosure, there is provided a method of manufacturing a semiconductor device, the method including: forming a mask on an insulating layer, the insulating layer provided on a substrate; patterning the insulating layer by using the mask to form an insulating layer pattern; forming a sacrificial material layer on the insulating layer and the mask; reducing a thickness of the sacrificial material layer to form a sacrificial layer and expose the mask; removing the mask; and removing the sacrificial layer by using mild plasma having a plasma damage rate to the insulating layer of 0.01 to 0.1 Å/s.

[0010] According to another aspect of the disclosure, there is provided a method of manufacturing a semiconductor device, the method including: forming a conductive layer and a mask on an insulating layer, the insulating layer provided on a substrate; etching the conductive layer to form a plurality of wires by using the mask; forming a sacrificial material layer on a space between the plurality of wires and the mask; reducing a thickness of the sacrificial material layer by an etch back process to form a sacrificial layer; forming a cover layer on the mask, the plurality of wires and the sacrificial layer; and forming of an air gap by removing the sacrificial layer by using mild plasma having a plasma damage rate to the insulating layer of 0.01 to 0.1 Å/s.

[0011] According to the embodiments, the sacrificial layer may be completely removed in a low-temperature process of 100° C. or lower by using the plasma treatment apparatus, thereby eliminating the risk due to residue substances and improving productivity by reducing process time.

[0012] Furthermore, by removing the sacrificial layer by using mild plasma with a plasma damage rate of 0.01 to 0.1 Å/s to the insulating layer, plasma induced damage (PID) to the insulating layer may be minimized.

[0013] In addition, the removal process of the sacrificial layer may be monitored in real time by using an optical emission spectroscopy device installed in the plasma treatment apparatus, allowing for more precise control of the air gap formation process.

[0014] Furthermore, while only temperature and pressure may be controlled in the heat treatment process, additional control parameters, such as the power of the plasma source, the flow rate, type, and mixing ratio of the reaction gases, in addition to temperature and pressure, may be obtained in the plasma treatment process, allowing for more precise control of the formation process of the air gap.

BRIEF DESCRIPTION OF DRAWINGS

[0015] Embodiments herein are illustrated in the accompanying drawings, throughout which like reference letters indicate corresponding parts in the various figures. The embodiments herein will be better understood from the following description with reference to the following illustrative drawings. Embodiments herein are illustrated by way of examples in the accompanying drawings, and in which:

[0016] FIG. **1** is a flowchart schematically illustrating a method of manufacturing a semiconductor device according to an embodiment.

[0017] FIGS. **2** to **6** are diagrams illustrating the method of manufacturing the semiconductor device according to the embodiment.

[0018] FIG. **7** is a schematic diagram of a plasma treatment apparatus used in the method of manufacturing the semiconductor device according to the embodiment.

[0019] FIG. **8** is a graph illustrating a change in a radical signal measured by a optical emission spectroscopy device of the plasma treatment apparatus over time.

[0020] FIG. **9** is a graph illustrating a thickness and the amount of etch of a sacrificial layer removed by a plasma treatment apparatus and the amount of etch over time.

[0021] FIG. **10** is a schematic diagram of the plasma treatment apparatus used in the method of manufacturing the semiconductor device according to another embodiment.

[0022] FIG. **11** is a flowchart schematically illustrating a method of manufacturing a semiconductor device according to another embodiment.

[0023] FIGS. **12** to **17** are diagrams illustrating the method of manufacturing the semiconductor device according to another embodiment.

DETAILED DESCRIPTION

[0024] Hereinafter, embodiments of the disclosure will be described with reference to accompanying drawings so as to be easily understood by a person ordinary skilled in the art. The disclosure may be variously implemented and is not limited to the following embodiments.

[0025] The drawings and description are to be regarded as illustrative in nature and not restrictive. Like reference numerals designate like elements throughout the specification.

[0026] In addition, the size and thickness of each configuration illustrated in the drawings are arbitrarily illustrated for understanding and ease of description, but the disclosure is not limited thereto. In the drawings, the thickness of layers, films, panels, regions, etc., are exaggerated for clarity. In the drawings, for understanding and ease of description, the thickness of some layers and areas is exaggerated.

[0027] Further, it will be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" another element, it may be directly on the other element or intervening elements may also be present. On the other hand, when an element is referred to as being "directly on" another element, there are no intervening elements present.

[0028] In addition, unless explicitly described to the contrary, the word "comprise", and variations such as "comprises" or "comprising", will be understood to imply the inclusion of stated elements but not the exclusion of any other elements.

[0029] Further, throughout the specification, when it is referred to as "in a plan view", it means when a target part is viewed from above, and when it is referred to as "in a cross-sectional view", it means when the cross-section obtained by cutting a target part vertically is viewed from the side.

[0030] FIG. **1** is a flowchart schematically illustrating a method of manufacturing a semiconductor device according to an embodiment, and FIGS. **2** to **6** are diagrams illustrating the method of manufacturing the semiconductor device according to an embodiment.

[0031] According to an embodiment illustrated in FIG. **1**, the method may include forming a plurality of wires on an insulating layer (S**110**), forming a sacrificial layer between the plurality of wires (S**120**), forming cover layer on the sacrificial layer (S**130**) and forming an air cap using mild plasma (S**140**). However, the disclosure is not limited thereto, and as such, according to another embodiment, one or more other operations may be performed in addition to the operations illustrated in FIG. **1**. Referring to FIGS. **1** and **2**, in operation (S**110**), the method of manufacturing a semiconductor device according to an embodiment of the disclosure includes forming an insulating layer **120** on a substrate **110**, and forming a plurality of wires **140** on the insulating layer **120**.

[0032] For example, the insulating layer **120** may be formed on the substrate **110**. The substrate **110** may include, but is not limited to, a semiconductor chip formed by a front end of line (FEOL) process, and the like.

[0033] The insulating layer **120** may include a dielectric material having a dielectric constant smaller than a reference value. For example, the insulating layer **120** may include a dielectric material having a dielectric constant smaller than silicon oxide (SiO_2).

[0034] According to an embodiment, the dielectric material may include hydrocarbon compounds, carbides, carbon, or combinations thereof. For example, the dielectric material may be char or ash including a variety of hydrocarbon compounds, carbides, carbons, or combinations thereof, produced by pyrolysing hydrocarbon-based polymers, where the carbon rings of the hydrocarbon-based polymer are broken by pyrolysis. For example, the hydrocarbon-based polymer may include an aromatic hydrocarbon polymer, a (meth)acrylic polymer, a vinylpyridine polymer, a vinylester polymer, a vinylpyrrolidone polymer, an olefin polymer, or a combination thereof.

[0035] The dielectric material may include 60 wt % to 90 wt % carbon and 10 wt % to 40 wt % hydrogen. For example, the weight ratios of carbon and hydrogen may be based on the total weight of the dielectric material. For example, the dielectric material may include 70 wt % to 90 wt % carbon and 10 wt % to 30 wt % hydrogen, 72 wt % to 88 wt % carbon and 12 wt % to 28 wt % hydrogen, or 75 wt % to 85 wt % carbon and 15 wt % to 25 wt % hydrogen.

[0036] Moreover, the dielectric material may further include additional components including, but not limited to, halogen elements, nitrogen (N), oxygen (O), fluorine (F), sulfur (S), phosphorus (P), sodium (Na), magnesium (Mg), manganese (Mn), silicon (Si), sulfur (S), iron (Fe), or combinations thereof. The additional components may be derived from the components of the hydrocarbon-based polymer used to form the dielectric material. The additional components may be included at 0 wt % to 10 wt % based on the total weight of the dielectric material.

[0037] According to an embodiment, the dielectric material may include a carbon-doped silicon oxide (SiOC), or a porous silicon oxide.

[0038] For example, the carbon-doped silicon oxide is a silicon oxide in which at least some of the oxygen atoms bonded to the silicon are substituted with an organic group containing carbon. For example, the carbon-doped silicon oxide may be trimethylsilane (TMS) (BLACKDIAMOND™), tetramethylcyclotetrasilane (TMCTS) (Coral™), dimethyldimethoxysilane (DMDMOS) (Aurora™), or hydrogen silsesquioxane (HSG).

[0039] For example, the porous silicon oxide may be formed by oxidizing a carbon-doped silicon oxide and removing organic matters containing carbon. For example, when oxidizing agent is applied to a carbon-doped silicon oxide, silicon oxide (SiOx) may be formed by oxidizing the carbon-doped silicon oxide and an organic matter containing carbon may be removed.

[0040] Referring to FIG. **2**, an anti-diffusion layer, a conductive layer, and a hard mask **150** may be sequentially stacked on the insulating layer **120**, and the conductive layer and the anti-diffusion layer may be etched by using the hard mask **150** as an etch-resistant layer to form an anti-diffusion wire **130** and the plurality of wires **140**.

[0041] The anti-diffusion wire **130** may prevent conductive components contained in the plurality of wires **140** from diffusing into the insulating layer **120** containing the dielectric material. The anti-diffusion wire **130** may also serve as an adhesive layer to attach the plurality of wires **140** to the insulating layer **120**.

[0042] The plurality of wires **140** may be spaced apart from each other. For example, the plurality of wires **140** may be spaced apart from each other by a an interval d. For example, the interval d may be predetermined. The plurality of wires **140** spaced apart from each other may form an exposed space ES between adjacent wires **140**. For example, the exposed space ED may expose the insulating layer **120**.

[0043] Referring to FIGS. **1** and **3**, in operation (S**120**), a sacrificial material layer **60** may be deposited over the exposed space ES between the plurality of wires **140** and the hard mask **150**. Thereafter, as illustrated in FIG. **4**, an etch back process may be performed on the sacrificial layer **60**. For example, the etch back process may be performed, using hydrogen plasma (H_2 plasma) or the like. The etch back process may be performed on the sacrificial layer **60** to the thickness of the sacrificial material layer **60** to form a recessed sacrificial layer **160** between the wires **140**. However, the disclosure is not limited thereto, and as such, according to another embodiment, the sacrificial layer **240** may be etched in a different manner.

[0044] The sacrificial layer **160** may include a carbon composite formed by a thermopolymerization reaction of a precursor with a ring structure or a linear structure. For example, the sacrificial layer **160** may include a polyurea formed by a thermopolymerization reaction of isocyanate and amine.

[0045] Referring to FIGS. **1** and **5**, in operation (S**130**), a cover layer **170** may be formed over the hard mask **150** and the sacrificial layer **160**.

[0046] Referring to FIGS. FIGS. **1** and **6**, in operation (S**140**), the sacrificial layer **160** formed under the cover layer **170** may be removed using a plasma treatment apparatus to form an air gap (AG). A plasma treatment apparatus is illustrated according to an embodiment in FIG. **7**.

[0047] According to an embodiment, the sacrificial layer **160** may be removed by using mild plasma MP generated by the plasma treatment apparatus PTA. The mild plasma MP may refer to plasma having a plasma damage rate of 0.01 to 0.1 Å/s to the insulating layer **120** including a dielectric material.

[0048] Accordingly, damage to the insulating layer **120** by the mild plasma MP used to remove the sacrificial layer **160** may be minimized.

[0049] Furthermore, in the process of forming an air gap AG, the total thickness variation of the insulating layer **120** may be 10 Å or less. Thus, damage to the insulating layer **120** caused by the mild plasma MP may be minimized.

[0050] The plasma damage rate to the insulating layer **120** may be measured using the change in thickness of the insulating layer **120** caused by the mild plasma MP. In other words, the plasma damage rate to the insulating layer **120** may be measured by measuring the initial thickness of an insulating layer sample made of the same material as the insulating layer **120**, exposing the insulating layer sample to mild plasma MP, and then wet etching the insulating layer sample by using an etchant, such as using hydrofluoric acid (HF), to measure the final thickness of the insulating layer sample.

[0051] Hereinafter, the plasma treatment apparatus PTA for forming the air gap AG will be described in detail with reference to the drawings.

[0052] FIG. **7** is a schematic diagram of the plasma treatment apparatus used in the method of manufacturing the semiconductor device according to the embodiment of the disclosure.

[0053] As illustrated in FIG. **7**, the plasma treatment apparatus PTA used in the method of manufacturing the semiconductor device according to the embodiment of the disclosure may include a plasma generator **10** and a plasma chamber **20**. However, the disclosure is not limited thereto, and as such, according to an embodiment, the plasma treatment apparatus PTA may include a controller configured to control one or more operations of the plasma treatment apparatus PTA. For example, the controller may include a memory storing one or more instructions, and a processor configured to executed the one or more instructions to perform the one or more operations of the plasma treatment apparatus PTA.

[0054] The plasma generator **10** may generate mild plasma MP. The plasma generator **10** may include a plasma source supply unit **11** and a reaction gas supply unit **12**.

[0055] The plasma source supply unit **11** may supply a plasma source PS into the plasma chamber **20**. The plasma source PS may include, but is not limited to, surface wave plasma (SWP), remote Inductively coupled plasma (ICP), and very high frequency plasma (VHF). The ICP utilizes an induced magnetic field induced by a coiled RF antenna to generate plasma.

[0056] The reaction gas supply unit **12** may supply reaction gas RG to the interior of the plasma chamber **20**. The reaction gas RG may be excited by the plasma source PS to generate mild plasma MP.

[0057] The reaction gas supply **12** may include a plurality of sub-gas supply units **12***a*, **12***b*, and **12***c* that are installed on the side of the plasma chamber **20**. For example, the plurality of sub-gas supply units **12***a*, **12***b*, and **12***c* may be installed to surround the plasma chamber **20**. For example, the plurality of sub-gas supply units **12***a*, **12***b*, and **12***c* may have a ring shape.

[0058] The plurality of sub-gas supply units **12***a*, **12***b*, and **12***c* may include a first gas supply unit **12***a*, a second gas supply unit **12***b*, and a third gas supply unit **12***c*. For example, the first gas supply unit **12***a* is a lower gas supply unit, the second gas supply unit **12***b* is an intermediate gas supply unit, and the third gas supply unit **12***c* is an upper gas supply unit, installed in turn from the bottom according to the height of the side of the plasma chamber **20**. The lower gas supply unit **12***a* may be located closest to a semiconductor device **1** including the sacrificial layer **160**. However, the disclosure is not limited thereto, and as such, order and the arrangement of the sub-gas supply units **12***a*, **12***b* and **12***c* may be different.

[0059] According to an embedment, the mild plasma MP may be generated by a plasma source PS exciting reaction gas RG supplied through the lower gas supply unit **12***a*. For example, the mild plasma MP may be a plasma with the

plasma damage rate of 0.01 to 0.1 Å/s to the insulating layer **120** generated by the plasma source PS exciting reaction gas RG supplied through the lower gas supply unit **12***c*. According to an embodiment, plasma with the plasma damage rate equal to or greater than 0.1 Å/s to the insulating layer **120** including the dielectric material may be generated by the plasma source PS exciting reaction gas RG supplied through the intermediate gas supply unit **12***b* and the upper gas supply unit **12***c*.

[0060] The reaction gas RG may include, but is not limited to, hydrogen (H_2), oxygen (O_2), carbon dioxide (CO_2), ammonia (NH_3), nitrogen (N_2), helium (He), argon (Ar), or mixed gas thereof.

[0061] In the plasma chamber **20**, the semiconductor device **1** having the sacrificial layer **160** is located, and the sacrificial layer **160** of the semiconductor device **1** may be removed by using the mild plasma MP to form an air gap AG.

[0062] The plasma chamber **20** may include a chamber main body **21**, a plasma electrode **22**, a temperature control unit **23**, and an optical emission spectroscopy device (OES) device **24**. The temperature control unit **23** may be a controller or a control circuit.

[0063] The chamber main body **21** may including a stage (or a platform) for receiving the semiconductor device **1**. Moreover, the chamber main body **21** may include a space in which the mild plasma MP is generated. For example, the space in which the mild plasma MP is generated may be provided above the stage receiving the semiconductor device **1**.

[0064] The plasma electrode **22** applies a voltage to the plasma source PS and the reaction gas RG to generate the mild plasma MP, and may act as a support unit on which the semiconductor device **1** is seated.

[0065] The temperature control unit **23** may include a heater or the like surrounding the chamber main body **21**. The sacrificial layer **160** may be removed at a low temperature of 100 degrees or less by using the temperature control unit **23**.

[0066] The optical emission spectroscopy device **24** may include an optical sensor to detect luminescence spectra, a luminescence spectroscopy unit to analyze the luminescence spectra, and the like. The optical emission spectroscopy device **24** may determine the point at which the intensity of the radical signal becomes constant as an end point EP of the plasma treatment process and turn off the plasma treatment apparatus.

[0067] FIG. **8** is a graph illustrating a change in a radical signal measured by the optical emission spectroscopy device of the plasma treatment apparatus over time, and FIG. **9** is a graph illustrating a thickness of a sacrificial layer removed by a plasma treatment apparatus and the amount of etch over time.

[0068] As illustrated in FIG. **8**, a point at which the intensity of the time-varying radical signal becomes constant may be determined as the end point EP of the plasma treatment process. Moreover, as illustrated in FIG. **9**, a point at which the thickness and the amount of etching of the sacrificial layer **160** removed by the plasma treatment apparatus becomes constant may also be determined as the end point EP of the plasma treatment process. Thus, the end point EP of the plasma treatment process may be accurately determined in real time and the plasma treatment apparatus may be turned off.

[0069] In this way, in the process of forming the air gap AG, the change in the radical signal of the mild plasma MP may be measured by using the optical emission spectroscopy device **24** of the plasma treatment apparatus. This allows the formation process of the air gap AG to be monitored in real time to accurately determine a time point of turning off the plasma treatment process. Thus, the formation process of the air gap AG may be controlled more precisely.

[0070] While the reaction gas supply unit of the embodiment includes the plurality of sub-gas supply units **12***a*, **12***b*, and **12***c*, the disclosure is not limited thereto, and as such, according to another embodiment, the reaction gas may be supplied in another manner. For example, a reaction gas supply unit may supply the reaction gas through a shower head.

[0071] FIG. **10** is a schematic diagram of the plasma treatment apparatus used in the method of manufacturing the semiconductor device according to another embodiment.

[0072] As illustrated in FIG. **10**, the reaction gas supply unit **12** may include a shower head **12** that disperses and supplies reaction gas RG to the interior of the plasma chamber **20**.

[0073] The mild plasma MP may be generated by a plasma source PS exciting reaction gas RG supplied through the shower head **12**.

[0074] According to an embodiment, the sacrificial layer **160** may be completely removed in a low-temperature process of 100° C. or lower by using the plasma treatment apparatus PTA, thereby eliminating the risk due to residue substances and improving productivity by reducing process time.

[0075] In the process of forming the air gap AG, the process temperature may be controlled to 100° C. or lower using the temperature control unit of the plasma treatment apparatus. In other words, when pyrolysis is used to remove the sacrificial layer, the heat treatment process at a high temperature of 400° C. or higher needs to be carried out for a long time, and residue substances are easy to be generated, which may cause leakage current due to the residue substances.

[0076] However, in the plasma treatment apparatus using the mild plasma MP, as in the present embodiment, the sacrificial layer may be completely removed in a short time even with a low-temperature process of 100° C. or lower, thereby minimizing the generation of leakage current, which may improve productivity.

[0077] In addition, while only temperature and pressure may be controlled in the heat treatment process, additional control parameters, such as the power of the plasma source, the flow rate, type, and mixing ratio of the reaction gases, in addition to temperature and pressure, may be obtained in the plasma treatment process, allowing for more precise control of the formation process of the air gap AG.

[0078] In the above embodiment, the air gap is formed by removing the sacrificial layer with minimal damage to the insulating layer including the dielectric material using mild plasma, but other embodiments are possible in which an insulating layer pattern is completed by removing the sacrificial layer with minimal damage to the insulating layer including the dielectric material using mild plasma.

[0079] Hereinafter, a method of manufacturing a semiconductor device according to another embodiment of the disclosure will be described in detail with reference to FIGS. **11** to **16**.

[0080] FIG. **11** is a flowchart schematically illustrating a method of manufacturing a semiconductor device according to another embodiment, and FIGS. **12** to **17** are diagrams illustrating the method of manufacturing the semiconductor device according to another embodiment.

[0081] According to an embodiment illustrated in FIG. **11**, the method may include forming a hard mask on an insulating layer (S**210**), forming an insulating layer pattern (S**220**), forming a sacrificial material layer on the insulating layer pattern (S**230**), forming the sacrificial layer (S**240**), removing the hard mask (S**250**), and removing the sacrificial layer by using mild plasma (S**260**). Referring to FIGS. **11** and **12**, in operation (S**210**), the method of manufacturing a semiconductor device according to another embodiment of the disclosure may include forming a hard mask **230** on an insulating layer **220** on a substrate **210**. The substrate **210** may include a semiconductor chip formed by a front end of line (FEOL) process, and the like. The insulating layer **220** may include a dielectric material having a smaller dielectric constant than a reference value. For example, the insulating layer **120** may include a dielectric material having a smaller dielectric constant than silicon oxide (SiO_2).

[0082] The hard mask **230** may have a pattern that exposes one or more portions of the insulating layer **220**. For example, as shown in FIG. **12**, the hard mask **230** may have open space in between to expose an upper surface of the insulation layer **220**.

[0083] Referring to FIGS. **11** and **13**, in operation (S**220**), the insulating layer **220** may be patterned by using the hard mask **230** as an etch mask, to form an insulating layer pattern **221** on the insulating layer **220**. The insulating pattern **221** may include a trench **221***a* or a through-hole **221***b* formed in the insulating layer **220**. However, the disclosure is not limited to the patterns illustrated in FIG. **13**, and as such, various other patterns may be formed on the insulating layer **220**.

[0084] Referring to FIGS. **11** and **14**, in operation (S**230**), a sacrificial material layer **40** may be formed S**230** on the insulating layer **220** and the hard mask **230**. The sacrificial material layer **40** may be formed on the insulating layer **220**. For example, the sacrificial material layer **40** may be formed to cover the insulating layer **220** to prevent etching of the insulating layer **220** when the hard mask **230** is etched in a later process. The sacrificial material layer **40** may fill the insulating layer pattern **221** formed on the insulating layer **220**. For example, sacrificial material layer **40** may fill the trench **221***a* or the through-hole **221***b*. The sacrificial material layer **40** may include a carbon composite formed by a thermopolymerization reaction of a precursor with a ring structure or a linear structure.

[0085] Referring to FIGS. **11** and **15**, in operation (S**240**), the thickness of the sacrificial material layer **40** may be reduced by an etch back process, such as ashing, to form a sacrificial layer **240**. However, the disclosure is not limited thereto, and as such, according to another embodiment, the sacrificial layer **240** may be etched in a different manner. In this case, the hard mask **230** covered by the sacrificial material layer **40** is exposed to the outside, but the insulating layer **220** covered by the sacrificial layer **240** is only partially exposed to the outside, and most of the insulating layer **220** is not exposed.

[0086] Referring to FIGS. **11** and **16**, in operation (S**250**), an etching process may be performed to remove the hard mask **230**. In this case, the insulating layer **220** is largely covered by the sacrificial layer **240**, so the insulating layer **220** is not etched in the etching process that removes the hard mask **230**.

[0087] Referring to FIGS. **11** and **17**, in operation (S**260**), the sacrificial layer **240** filled in the insulating layer pattern **221** of the insulating layer **220** is removed by using a plasma treatment apparatus PTA to complete the insulating layer pattern **221**.

[0088] Here, the mild plasma MP generated by the plasma treatment apparatus PTA may be utilized to remove the sacrificial layer **240**. The mild plasma MP may refer to plasma having a plasma damage rate of 0.01 to 0.1 Å/s to the insulating layer **220** including a dielectric material.

[0089] Thus, damage to the insulating layer **220** by the mild plasma MP used to remove the sacrificial layer **240** may be minimized.

[0090] Further, in the process of removing the sacrificial layer **240** that fills the insulating layer pattern **221** of the insulating layer **220**, the change in the radical signal of the mild plasma MP may be measured by using the luminescence spectroscopy apparatus **24** of the plasma processing device. Accordingly, the removal process of the sacrificial layer **240** may be monitored in real time to accurately determine a time point of turning off the plasma treatment process. Thus, the removal process of the sacrificial layer **240** may be more precisely controlled.

[0091] Although embodiments of the disclosure has been described in detail, the scope of the disclosure is not limited by the embodiments. Various changes and modifications using the basic concept of the disclosure defined in the accompanying claims by those skilled in the art shall be construed to belong to the scope of the present disclosure.

What is claimed is:

1. A method of manufacturing a semiconductor device, the method comprising:

forming a plurality of wires on an insulating layer, the insulating layer provided on a substrate;

forming a sacrificial layer between the plurality of wires;

forming a cover layer on the plurality of wires and the sacrificial layer; and

forming an air gap by removing the sacrificial layer using mild plasma having a plasma damage rate to the insulating layer of 0.01 to 0.1 Å/s.

2. The method of claim **1**, wherein the plasma damage rate to the insulating layer is measured by using a change in thickness of a sample insulating layer caused by the mild plasma.

3. The method of claim **1**, wherein in the forming of the air gap, a total change in thickness of the insulating layer is 10 Å or less.

4. The method of claim **1**, wherein the forming of the air gap comprises controlling a process temperature to be less than or equal to 100 degrees.

5. The method of claim **1**, wherein the forming of the air gap comprises monitoring the forming of the air gap in real time through a change in a radical signal of the mild plasma by using a luminescence spectroscope device.

6. The method of claim **1**, wherein the insulating layer comprises a dielectric material having a smaller dielectric constant than silicon oxide (SiO_2).

7. The method of claim **1**, wherein the sacrificial layer comprises a carbon composite formed by a thermopolymerization reaction of a precursor with a ring structure or a linear structure.

8. The method of claim **1**, wherein the mild plasma is produced by a plasma generating unit of a plasma treatment apparatus, and

wherein the sacrificial layer is removed in a plasma chamber of the plasma treatment apparatus using the mild plasma.

9. The method of claim **8**, further comprising:

supplying, by a plasma source supply unit, a plasma source into a plasma chamber; and

supplying, a reaction gas supply unit, reaction gas into the plasma chamber to react with the plasma source to produce the mild plasma.

10. The method of claim **9**, wherein the reaction gas supply unit comprises a plurality of sub-gas supply units installed on a side of the plasma chamber, and

wherein the plurality of sub-gas supply units includes a first gas supply unit, a second gas supply unit, and a third gas supply unit installed on the plasma chamber, the first gas supply unit being provided at a level lower than the second gas supply unit and the third gas supply unit in the plasma chamber, and

wherein the mild plasma is generated by the plasma source exciting the reaction gas supplied through the first gas supply unit.

11. The method of claim **9**, wherein the reaction gas supply unit comprises a shower head for dispersing and supplying the reaction gas into the plasma chamber, and

wherein the mild plasma is generated by the plasma source exciting the reaction gas supplied through the shower head.

12. The method of claim **9**, wherein the plasma source comprises one of surface wave plasma (SWP), remotely inductively coupled plasma (ICP), and very high frequency plasma (VHF).

13. A method of manufacturing a semiconductor device, the method comprising:

forming a mask on an insulating layer, the insulating layer provided on a substrate;

patterning the insulating layer by using the mask to form an insulating layer pattern;

forming a sacrificial material layer on the insulating layer and the mask;

reducing a thickness of the sacrificial material layer to form a sacrificial layer and expose the mask;

removing the mask; and

removing the sacrificial layer by using mild plasma having a plasma damage rate to the insulating layer of 0.01 to 0.1 Å/s.

14. The method of claim **13**, wherein in the removing of the sacrificial layer, a total change in thickness of the insulating layer is 10 Å or less.

15. The method of claim **13**, wherein the removing of the sacrificial layer comprises controlling controls a process temperature to be less than or equal to 100 degrees.

16. The method of claim **13**, further comprising monitoring the removing process of the sacrificial layer in real time through a change in a radical signal of the mild plasma by using a luminescence spectroscope device.

17. The method of claim **13**, wherein the insulating layer comprises a dielectric material having a smaller dielectric constant than silicon oxide (SiO_2).

18. The method of claim **13**, wherein the sacrificial layer comprises a carbon composite formed by a thermopolymerization reaction of a precursor with a ring structure or a linear structure.

19. A method of manufacturing a semiconductor device, the method comprising:

forming a conductive layer and a mask on an insulating layer, the insulating layer provided on a substrate;

etching the conductive layer to form a plurality of wires by using the mask;

forming a sacrificial material layer on a space between the plurality of wires and the mask;

reducing a thickness of the sacrificial material layer by an etch back process to form a sacrificial layer;

forming a cover layer on the mask, the plurality of wires and the sacrificial layer; and

forming of an air gap by removing the sacrificial layer by using mild plasma having a plasma damage rate to the insulating layer of 0.01 to 0.1 Å/s.

20. The method of claim **19**, wherein the insulating layer comprises a dielectric material having a smaller dielectric constant than silicon oxide (SiO_2).

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