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(54) **POWER SEMICONDUCTOR MODULE ARRANGEMENT AND METHOD FOR PRODUCING THE SAME**

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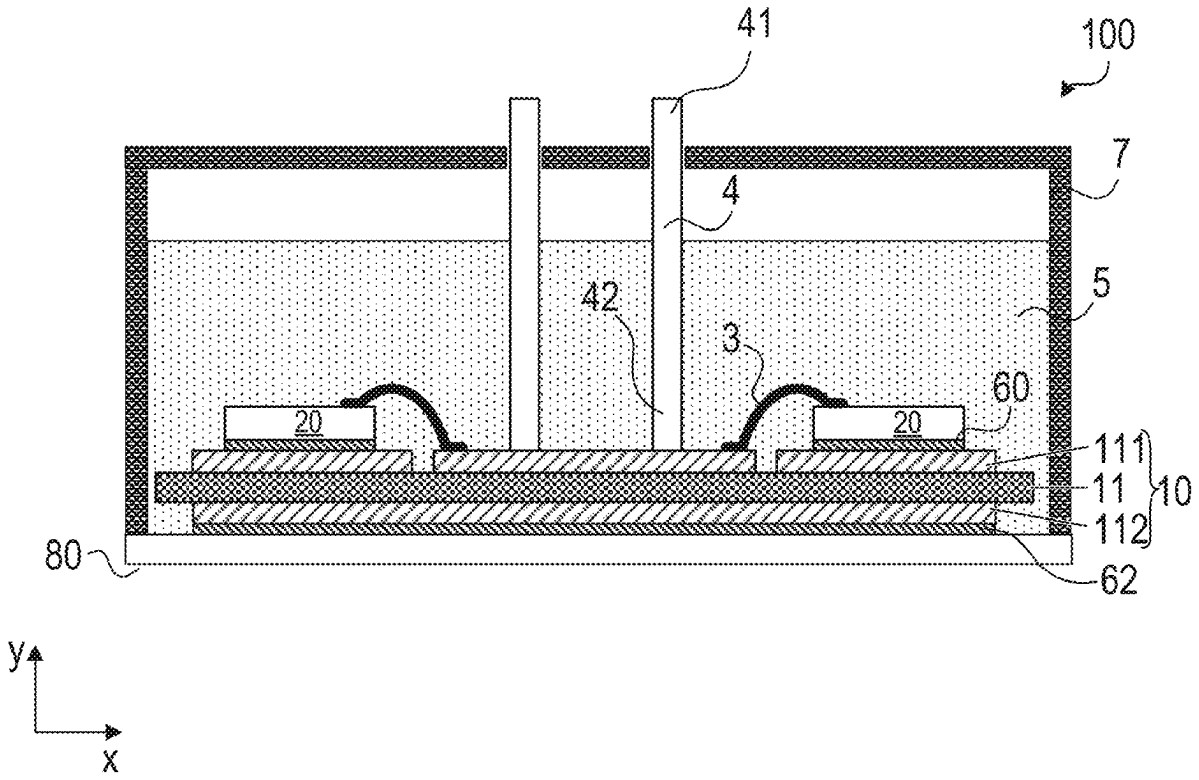
(57) **ABSTRACT**

A semiconductor module arrangement includes a substrate having a dielectric insulation layer and a metallization layer arranged on a first side of the dielectric insulation layer, a base plate, and a connection layer. The connection layer is arranged between the substrate and the base plate and attaches the substrate to the base plate. The connection layer directly adjoins the base plate and a second side of the dielectric insulation layer, opposite the first side. The connection layer includes a sinter paste and an adhesion promoter.



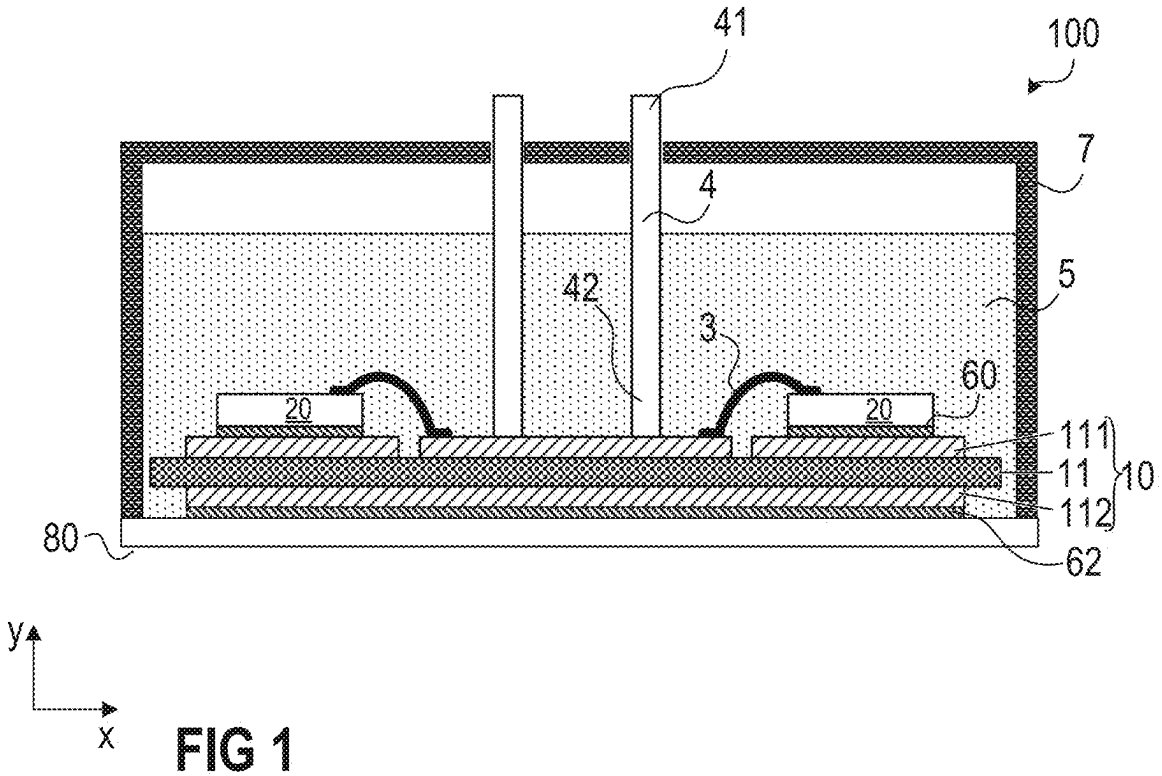

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FIG 1

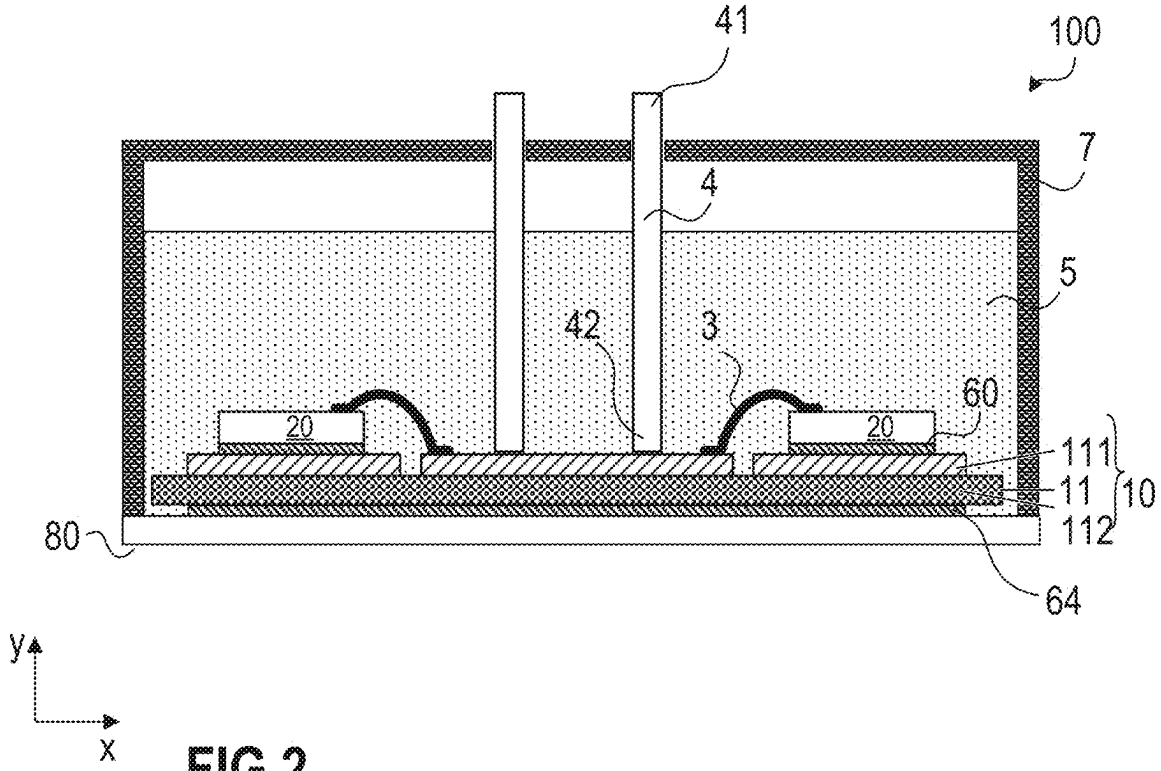
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FIG 2

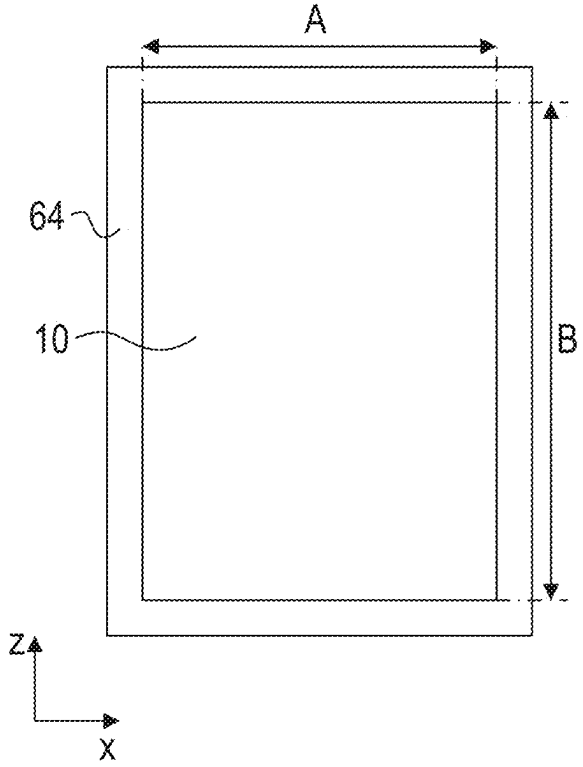

FIG 3

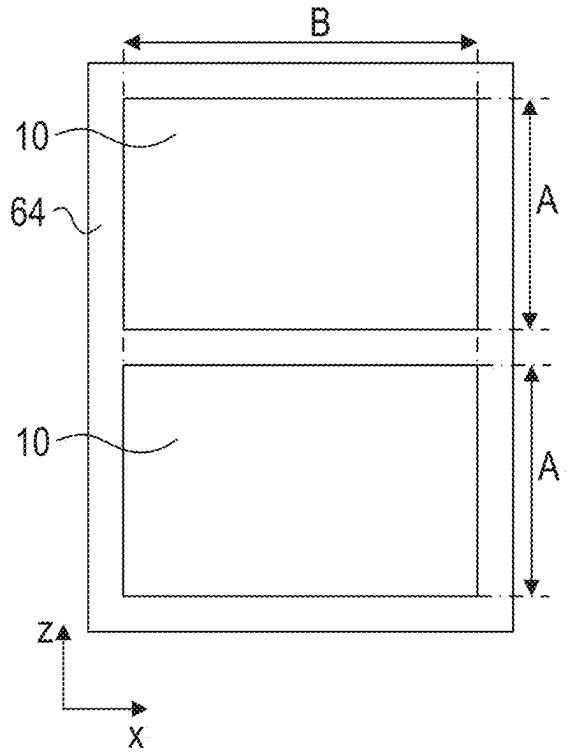

FIG 4

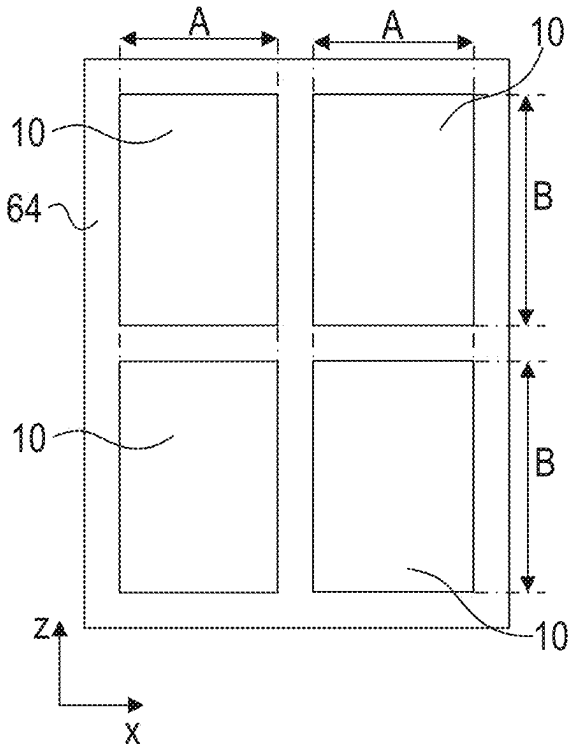

FIG 5

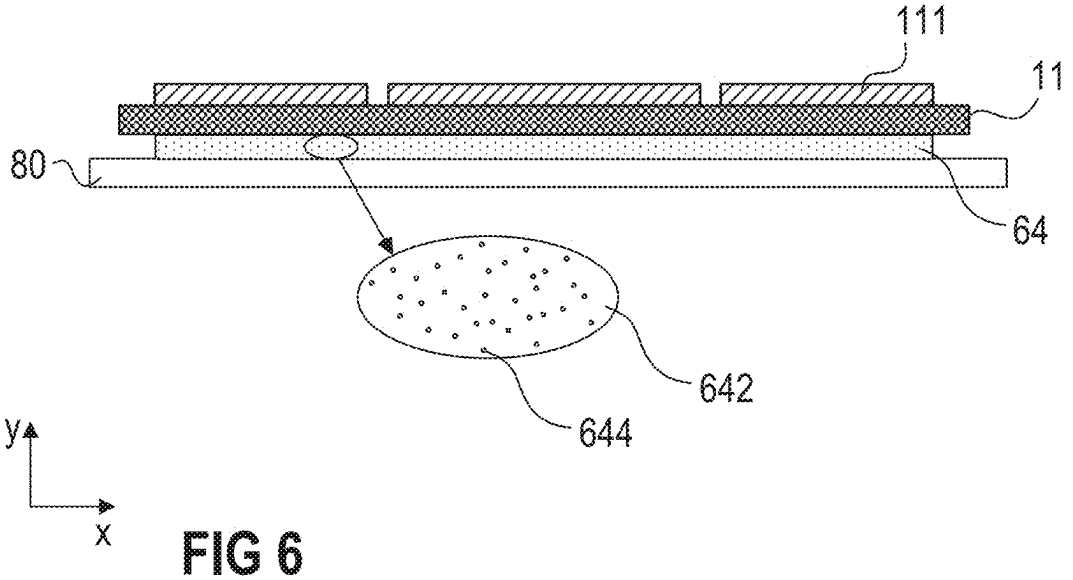

FIG 6

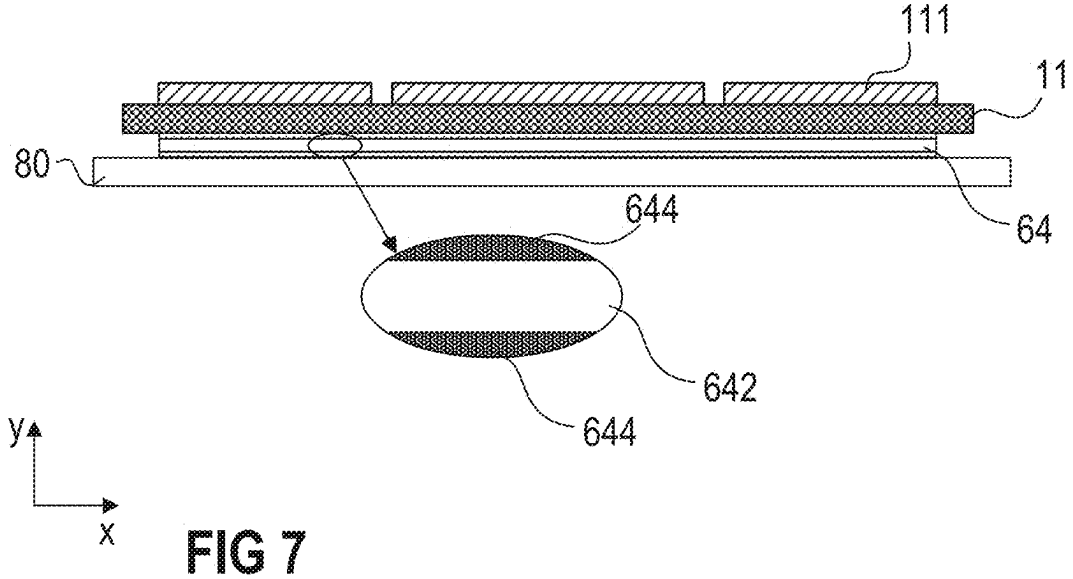

FIG 7

POWER SEMICONDUCTOR MODULE ARRANGEMENT AND METHOD FOR PRODUCING THE SAME

TECHNICAL FIELD

[0001] The instant disclosure relates to a power semiconductor module arrangement and to a method for producing such a power semiconductor module arrangement.

BACKGROUND

[0002] Power semiconductor module arrangements often include at least one substrate. A semiconductor arrangement including a plurality of controllable semiconductor elements (e.g., two or more IGBTs) is arranged on each of the at least one substrate. Each substrate usually comprises a substrate layer (e.g., a ceramic layer), a first metallization layer deposited on a first side of the substrate layer and a second metallization layer deposited on a second side of the substrate layer. The controllable semiconductor elements are mounted, for example, on the first metallization layer. At least some controllable semiconductor elements of the power semiconductor module arrangement perform a plurality of switching operations during the operation of the power semiconductor module arrangement. When performing many switching operations within a short period of time, for example, the controllable semiconductor elements generate heat. Heat that is generated during the operation of the power semiconductor module arrangement is mostly dissipated from the controllable semiconductor elements to the substrate and further through a base plate to a heat sink.

[0003] There is a need for a power semiconductor module arrangement in which heat can be effectively conducted away from the semiconductor elements, and which can be produced at low costs.

SUMMARY

[0004] A power semiconductor module arrangement includes a substrate including a dielectric insulation layer and a metallization layer arranged on a first side of the dielectric insulation layer, a base plate, and a connection layer, wherein the connection layer is arranged between the substrate and the base plate and attaches the substrate to the base plate, the connection layer directly adjoins the base plate and a second side of the dielectric insulation layer, opposite the first side, and the connection layer includes a sinter paste and an adhesion promoter.

[0005] A method includes forming a connection layer, arranging a substrate on a base plate with the connection layer arranged between the substrate and the base plate, and performing a sintering process, thereby connecting the substrate to the base plate by means of the connection layer, wherein the substrate includes a dielectric insulation layer and a metallization layer arranged on a first side of the dielectric insulation layer, when the substrate is arranged on the base plate, the connection layer directly adjoins the base plate and a second side of the dielectric insulation layer, opposite the first side, and the connection layer includes a sinter paste and an adhesion promoter.

[0006] The invention may be better understood with reference to the following drawings and the description. The components in the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention. Moreover, in the figures, like referenced numerals designate corresponding parts throughout the different views.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. **1** is a cross-sectional view of a power semiconductor module arrangement.

[0008] FIG. **2** is a cross-sectional view of a power semiconductor module arrangement according to embodiments of the disclosure.

[0009] FIG. **3** is top view of a base plate with a substrate mounted thereon.

[0010] FIG. **4** is a top view of a base plate with two substrates mounted thereon.

[0011] FIG. **5** is a top view of a base plate with four substrates mounted thereon.

[0012] FIG. **6** is a cross-sectional view of a power semiconductor module arrangement according to embodiments of the disclosure.

[0013] FIG. **7** is a cross-sectional view of a power semiconductor module arrangement according to further embodiments of the disclosure.

DETAILED DESCRIPTION

[0014] In the following detailed description, reference is made to the accompanying drawings. The drawings show specific examples in which the invention may be practiced. It is to be understood that the features and principles described with respect to the various examples may be combined with each other, unless specifically noted otherwise. In the description as well as in the claims, designations of certain elements as "first element", "second element", "third element", etc. are not to be understood as enumerative. Instead, such designations serve solely to address different "elements". That is, e.g., the existence of a "third element" does not necessarily require the existence of a "first element" and a "second element". An electrical line or electrical connection as described herein may be a single electrically conductive element, or include at least two individual electrically conductive elements connected in series and/or parallel. Electrical lines and electrical connections may include metal and/or semiconductor material, and may be permanently electrically conductive (i.e., non-switchable). A semiconductor body as described herein may be made from (doped) semiconductor material and may be a semiconductor chip or be included in a semiconductor chip. A semiconductor body has electrically connectable pads and includes at least one semiconductor element with electrodes.

[0015] Referring to FIG. **1**, a cross-sectional view of a conventional power semiconductor module arrangement **100** is illustrated. The power semiconductor module arrangement **100** includes a housing **7** and a substrate **10**. The substrate **10** includes a dielectric insulation layer **11**, a (structured) first metallization layer **111** attached to the dielectric insulation layer **11**, and a (structured) second metallization layer **112** attached to the dielectric insulation layer **11**. The dielectric insulation layer **11** is disposed between the first and second metallization layers **111**, **112**.

[0016] Each of the first and second metallization layers **111**, **112** may consist of or include one of the following materials: copper; a copper alloy; aluminum; an aluminum alloy; any other metal or alloy that remains solid during the operation of the power semiconductor module arrangement.

The substrate **10** may be a ceramic substrate, that is, a substrate in which the dielectric insulation layer **11** is a ceramic, e.g., a thin ceramic layer. The ceramic may consist of or include one of the following materials: aluminum oxide; aluminum nitride; zirconium oxide; silicon nitride; boron nitride; or any other dielectric ceramic. Alternatively, the dielectric insulation layer **11** may consist of an organic compound and include one or more of the following materials: Al_2O_3, AlN, ZrO_2, SiC, BeO, BN, or Si_3N_4. For instance, the substrate **10** may, e.g., be a Direct Copper Bonding (DCB) substrate, a Direct Aluminum Bonding (DAB) substrate, or an Active Metal Brazing (AMB) substrate. Further, the substrate **10** may be an Insulated Metal Substrate (IMS). An Insulated Metal Substrate generally comprises a dielectric insulation layer **11** comprising (filled) materials such as epoxy resin or polyimide, for example. The material of the dielectric insulation layer **11** may be filled with ceramic particles, for example. Such particles may comprise, e.g., SiO_2, Al_2O_3, AlN, SiN or BN and may have a diameter of between about 1 μm and about 50 μm.

[0017] The substrate **10** is arranged in a housing **7**. In the example illustrated in FIG. **1**, the substrate **10** is arranged on a base plate **80** which forms a base surface of the housing **7**, while the housing **7** itself solely comprises sidewalls and, optionally, a top or cover. In some power semiconductor module arrangements **100**, more than one substrate **10** is arranged on the same base plate **80** and within the same housing **7**. The base plate **80** may comprise a layer of a metallic material such as, e.g., AlSiC, AlC, Al, MgSiC, or Cu. Other materials, however, are generally also possible.

[0018] One or more semiconductor bodies **20** may be arranged on the at least one substrate **10**. Each of the semiconductor bodies **20** arranged on the at least one substrate **10** may include a diode, an IGBT (Insulated-Gate Bipolar Transistor), a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor), a JFET (Junction Field-Effect Transistor), a HEMT (High-Electron-Mobility Transistor), or any other suitable semiconductor element.

[0019] The one or more semiconductor bodies **20** may form a semiconductor arrangement on the substrate **10**. In FIG. **1**, only two semiconductor bodies **20** are exemplarily illustrated. The second metallization layer **112** of the substrate **10** in FIG. **1** is a continuous layer. In some semiconductor modules **100**, the second metallization layer **112** may be a structured layer. The first metallization layer **111** is a structured layer in the example illustrated in FIG. **1**. "Structured layer" in this context means that the respective metallization layer is not a continuous layer, but includes recesses between different sections of the layer. Such recesses are schematically illustrated in FIG. **1**. The first metallization layer **111** in this example includes three different sections. Different semiconductor bodies **20** may be mounted to the same or to different sections of the first metallization layer **111**. Different sections of the first metallization layer **111** may have no electrical connection or may be electrically connected to one or more other sections using electrical connections **3** such as, e.g., bonding wires. Semiconductor bodies **20** may be electrically connected to each other or to the first metallization layer **111** using electrical connections **3**, for example. Electrical connections **3**, instead of bonding wires, may also include bonding ribbons, connection plates or conductor rails, for example, to name just a few examples. The one or more semiconductor bodies **20** may be electrically and mechanically connected to the substrate **10** by an electrically conductive connection layer **60**. Such an electrically conductive connection layer **60** may be a solder layer, a layer of an electrically conductive adhesive, or a layer of a sintered metal powder, e.g., a sintered silver (Ag) powder, for example. The one or more substrates **10** may be mechanically and thermally connected to a base plate **80** by means of a connection layer **62**. The connection layer **62** in conventional semiconductor modules **100** may be an electrically insulating adhesive layer, a solder layer, a layer of an electrically conductive adhesive, or a layer of a sintered metal powder, e.g., a sintered silver (Ag) powder, for example.

[0020] The power semiconductor module arrangement **100** illustrated in FIG. **1** further includes terminal elements **4**. The terminal elements **4** provide an electrical connection between the inside and the outside of the housing **7**. The terminal elements **4** may be electrically connected to the first metallization layer **111** with a second end **42**, while a first end **41** of the terminal elements **4** protrudes out of the housing **7**. The terminal elements **4** may be electrically contacted from the outside at their first end **41**.

[0021] Arranging the terminal elements **4** centrally on the substrate **10** is only an example. According to other examples, terminal elements **4** may be arranged closer to or adjacent to the sidewalls of the housing **7**. The second end **42** of a terminal element **4** may be electrically and mechanically connected to the substrate **10** by means of an electrically conductive connection layer (not specifically illustrated in FIG. **1**). Such an electrically conductive connection layer may be a solder layer, a layer of an electrically conductive adhesive, or a layer of a sintered metal powder, e.g., a sintered silver (Ag) powder, for example. Alternatively, the terminal elements **4** may also be coupled to the substrate by means of ultrasonic welding.

[0022] The power semiconductor module arrangement **100** may further include an encapsulant **5**. The encapsulant **5** may consist of or include a cured silicone gel or may be a rigid molding compound, for example. The encapsulant **5** may at least partly fill the interior of the housing **7**, thereby covering the components and electrical connections that are arranged on the substrate **10**. The terminal elements **4** may be partly embedded in the encapsulant **5**. At least their first ends **41**, however, are not covered by the encapsulant **5** and protrude from the encapsulant **5** through the housing **7** to the outside of the housing **7**. The encapsulant **5** is configured to protect the components and electrical connections of the power semiconductor module **100**, in particular the components arranged inside the housing **7**, from certain environmental conditions and mechanical damage. The encapsulant **5** is further configured to electrically insulate areas with different potentials (e.g., different sections of the first metallization layer **111**) from each other.

[0023] The second metallization layer **112** of the substrate **10** is generally not required for the overall function of the semiconductor module **100**. That is, the second metallization layer **112** generally does not conduct any currents during operation of the semiconductor module **100**. Therefore, it is generally possible that the second metallization layer **112** be omitted altogether. It is, however, not possible to directly attach the dielectric insulation layer **11** of a substrate **10** to a base plate **80** by means of conventional sinter pastes. Omitting the second metallization layer, however, reduces the overall costs of a semiconductor module **100**. Further, by omitting the second metallization layer **112**, the overall

thermal resistance Rth of the stack formed by the substrate **10** and the base plate **80** could be reduced, and the heat could be conducted away from the semiconductor bodies **20** to the base plate **80** more effectively.

[0024] Now referring to FIG. **2**, a semiconductor module arrangement **100** according to embodiments of the disclosure comprises a substrate **10** comprising a dielectric insulation layer **11** and a metallization layer **111** arranged on a first side of the dielectric insulation layer **11**. The substrate **10**, however, does not comprise a second metallization layer **112**. The semiconductor module **100** further comprises a base plate **80**, and a connection layer **64**. The connection layer **64** is arranged between the substrate **10** and the base plate **80** and attaches the substrate **10** to the base plate **80**. As the substrate **10** does not comprise a second metallization layer **112**, the connection layer **64** directly adjoins the base plate **80** and a second side of the dielectric insulation layer **11**, opposite the first side. The connection layer **64** comprises a sinter paste **642** and an adhesion promoter **644** (see, e.g., FIGS. **6** and **7**). Due to the adhesion promoter **644**, the connection layer **64** not only adheres to the base plate **80**, but also to the dielectric insulation layer **11** of the substrate **10**.

[0025] As has been mentioned before, the dielectric insulation layer **11** may consist of or include one of the following materials: Al_2O_3; AlN; ZrO_2; SiC; BeO; BN; or Si_3N_4. The base plate **80** may consist of or include one of the following materials: AlSiC, AlC, Al, MgSiC, or Cu. The sinter paste **642** may comprise at least one of copper, and silver, for example, and the adhesion promoter **644** may comprise or consist of, for example, titanium, chromium, or vanadium (e.g., vanadium nanoparticles).

[0026] According to some embodiments, the adhesion promoter **644** may be distributed within the sinter paste **642**. This is schematically illustrated in FIG. **6**. FIG. **6** schematically illustrates a cross-sectional view of a semiconductor module comprising a base plate **80**, a substrate **10**, and a connection layer **64**. A section of the connection layer **64** is illustrated in an enlarged view in order to illustrate the adhesion promoter **644** distributed within the sinter paste **642**. In order to produce the connection layer **64**, the sinter paste **642** and the adhesion promoter **644** may be mixed together. The adhesion promoter **644**, when mixed into the sinter paste **642**, is also present on the surfaces of the connection layer **64**. When the substrate **10** is arranged on the base plate **80** with the connection layer **64** arranged therebetween, and a sinter process is performed, the adhesion promoter **644** on the surfaces of the connection layer **64** reacts with the base plate **80** and with the dielectric insulation layer **11** of the substrate **10**. In this way, the substrate **10** may be permanently connected to the base plate **80**, even if no second metallization layer **112** is present. After mixing the sinter paste **642** with the adhesion promoter **644**, the connection layer **64** may be formed on a surface of the base plate **80**, and the substrate **10** may then be arranged on the connection layer **64**. It is, however, also possible to form the connection layer **64** on the substrate (i.e., on the second side of the dielectric insulation layer **11**) and to arrange the substrate **10** with the connection layer **64** formed thereon on the base plate **80**.

[0027] Instead of distributing the adhesion promoter **644** within the sinter paste **642**, however, it is also possible that the connection layer **64** comprises a first sublayer consisting of adhesion promoter **644**, a second sublayer consisting of sinter paste **642**, and a third sublayer consisting of adhesion promoter **644**, wherein the first sublayer is arranged such that it directly adjoins the base plate **80**, the third sublayer is arranged such that it directly adjoins the dielectric insulation layer **11**, and the second sublayer is arranged between and directly adjoins the first sublayer and the third sublayer. This is schematically illustrated in FIG. **7** which schematically illustrates a cross-sectional view of a semiconductor module comprising a base plate **80**, a substrate **10**, and a connection layer **64**. A section of the connection layer **64** is illustrated in an enlarged view in order to illustrate the first, second, and third sublayers.

[0028] A connection layer **64** comprising different sublayers may be formed in any suitable way. According to one example, the connection layer **64** may be formed by forming the second sublayer consisting of sinter paste, forming the first sublayer consisting of adhesion promoter on a first surface of the second sublayer, and forming the third sublayer consisting of adhesion promoter on a second surface of the second sublayer, opposite the first surface. The connection layer **64** comprising the first, second, and third sublayers may then be arranged between the substrate **10** and the base plate **80** (e.g., as a prefabricated foil). According to another example, the first sublayer is formed on the base plate **80**, and the second sublayer is subsequently formed on the first sublayer. The third sublayer may then be formed on the second sublayer, thereby forming a layer stack (connection layer **64**) comprising the first sublayer, the second sublayer, and the third sublayer on the base plate **80**. Alternatively, such a layer stack (connection layer **64**) may be formed on the dielectric insulation layer **11**, and the substrate **10** with the connection layer **64** formed thereon can then be arranged on the base plate **80**. According to an even further example, the first sublayer may be formed on the base plate **80**, and the third sublayer may be formed on the substrate **10**. The second sublayer in this example can either be formed on the first sublayer or on the third sublayer, before arranging the substrate **10** on the base plate **80**. That is, the connection layer **64**, comprising the first sublayer, the second sublayer, and the third sublayer is completed when the substrate **10** is arranged on the base plate **80**.

[0029] According to yet another example, the insulation layer **11** may consist of two sublayers. In this example, a first sublayer comprises an adhesion promoter **644** and the second sublayer comprises a sinter paste **642**. In some cases, depending upon the material from which the base plate **80** is made, the sublayer of sinter paste **642** can establish a secure bond with the baseplate **80** without need for a third sublayer of adhesion promoter **644**. Where a copper base plate **80** is used, for example, a third sublayer of adhesion promoter **644** may not be necessary.

[0030] A substrate **10** and a base plate **80** generally have different coefficients of thermal expansion, CTE. A dielectric insulation layer **11** consisting of AlN, for example, has a CTE of about $4\times10^{-6\circ}$ C.$^{-1}$ A base plate **80** consisting of Cu, for example, has a CTE of about $17\times10^{-6\circ}$ C.$^{-1}$ Generally speaking, the dielectric insulation layer **11** has a first coefficient of thermal expansion, CTE1, and the base plate **80** has a second coefficient of thermal expansion, CTE2, that is different from the first CTE1. The connection layer **64** may have a third coefficient of thermal expansion, CTE3, wherein CTE1<CTE3<CTE2. For example, the connection layer **64** may have a third coefficient of thermal expansion CTE3 of between $4\times10^{-6\circ}$ C.$^{-1}$ and $17\times10^{-6\circ}$ C.$^{-1}$ The

CTE3 of the connection layer **64** depends on the specific composition of the connection layer **64**. That is, by using different materials for the sinter paste **642** and the adhesion promoter **644**, and by using different sinter paste **642**/adhesion promoter **644** ratios, the CTE3 of the resulting connection layer **64** may be individually adjusted.

[0031] Generally, substrates **10** of any size can be used in the semiconductor modules described herein. In some semiconductor modules **100**, only one (exactly one/not more than one) substrate **10** is arranged on a base plate **80**. This is schematically illustrated in FIG. **3**. In other semiconductor modules **100**, more than one substrate **10** can be arranged on a single base plate **80**. A semiconductor module comprising two substrates **10** arranged on a base plate **80** is schematically illustrated in FIG. **4**, and a semiconductor module **100** comprising four substrates **10** arranged on a base plate **80** is schematically illustrated in FIG. **5**. Any other number of substrates **10** on a base plate **80** is generally possible. Each of the one or more substrates **10** illustrated in FIGS. **3**, **4** and **5** has a rectangular shape. Other shapes, however, are generally also possible. The substrates **10**, for example, may also have rounded corners. Each of the one or more substrates **10** has a width A in a first horizontal direction, and a length B in a second horizontal direction perpendicular to the first horizontal direction. The one or more substrates **10** arranged on the base plate **80** may be comparably large substrates **10**, having a width A of at least 30 millimeters, and a length B of at least 40 millimeters, for example. The advantages of directly mounting the dielectric insulation layer **11** to a base plate **80** and omitting the second metallization layer **112** (improved Rth, reduced thickness of layer stack formed by substrate **10**, connection layer **64**, and base plate **80**, and reduced overall costs of semiconductor module) become even more significant for larger substrates **10**. However, it is generally also possible to arrange smaller substrates **10** to a base plate **80** in the way described above.

[0032] A method according to embodiments of the disclosure comprises forming a connection layer **64**, arranging a substrate **10** on a base plate **80** with the connection layer **64** arranged between the substrate **10** and the base plate **80**, and performing a sintering process, thereby connecting the substrate **10** to the base plate **80** by means of the connection layer **64**, wherein the substrate **10** comprises a dielectric insulation layer **11** and a metallization layer **111** arranged on a first side of the dielectric insulation layer **11**, wherein, when the substrate **10** is arranged on the base plate **80**, the connection layer **64** directly adjoins the base plate **80** and a second side of the dielectric insulation layer **11**, opposite the first side, and the connection layer **64** comprises a sinter paste **642** and an adhesion promoter **644**.

[0033] Forming the connection layer **64** may comprise mixing the sinter paste **642** with the adhesion promoter **644**. After mixing the sinter paste **642** with the adhesion promoter **644**, the connection layer **64** may either be formed on a surface of the base plate **80**, or on the second side of the dielectric insulation layer **11**.

[0034] Alternatively, forming the connection layer **64** may comprise forming a second sublayer consisting of sinter paste **642** and forming a first sublayer consisting of adhesion promoter **644** on a first surface of the second sublayer. Forming the connection layer **64** may further comprise forming a third sublayer on the second sublayer, such that the second sublayer is arranged between the first sublayer and the third sublayer. Irrespective of whether the connection layer **64** comprises two or three sublayers, the connection layer **64** in this example may be a prefabricated mat that may be arranged on a surface of the base plate **80** or on a surface of the dielectric insulation layer **11**, before arranging the substrate **10** on the base plate **80**.

[0035] Alternatively, forming the connection layer **64** may comprise forming a sublayer consisting of sinter paste **642** on the base plate **80**, and forming a sublayer consisting of adhesion promoter **644** either on the second sublayer, or on the dielectric insulation layer **11** of the substrate **10** (connection layer **62** comprises two sublayers), or forming the connection layer **64** may comprise forming a sublayer consisting of adhesion promoter **644** on the base plate **80**, subsequently forming a sublayer consisting of sinter paste **642** on the sublayer consisting of adhesion promoter **644**, and forming a further sublayer consisting of adhesion promoter **644** either on the sublayer consisting of sinter paste **642**, or on the dielectric insulation layer **11** of the substrate **10** (connection layer **62** comprises three sublayers).

[0036] As used herein, the terms "having," "containing," "including," "comprising" and the like are open ended terms that indicate the presence of stated elements or features, but do not preclude additional elements or features. The articles "a," "an" and "the" are intended to include the plural as well as the singular, unless the context clearly indicates otherwise.

[0037] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that a variety of alternate and/or equivalent implementations may be substituted for the specific embodiments shown and described without departing from the scope of the present invention. This application is intended to cover any adaptations or variations of the specific embodiments discussed herein. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

1. A semiconductor module arrangement, comprising:

a substrate comprising a dielectric insulation layer and a metallization layer arranged on a first side of the dielectric insulation layer;

a base plate; and

a connection layer,

wherein the connection layer is arranged between the substrate and the base plate and attaches the substrate to the base plate,

wherein the connection layer directly adjoins the base plate and a second side of the dielectric insulation layer, opposite the first side,

wherein the connection layer comprises a sinter paste and an adhesion promoter.

2. The semiconductor module arrangement of claim **1**, wherein the adhesion promoter is distributed within the sinter paste.

3. The semiconductor module arrangement of claim **1**, wherein the connection layer comprises a first sublayer consisting of the adhesion promoter and a second sublayer consisting of the sinter paste, and wherein the first sublayer is arranged such that the first sublayer directly adjoins the dielectric insulation layer, and the second sublayer directly adjoins the first sublayer on a side opposite the dielectric insulation layer.

4. The semiconductor module arrangement of claim **3**, wherein the connection layer further comprises a third

sublayer consisting of the adhesion promoter, and wherein the third sublayer directly adjoins the second sublayer such that the second sublayer is arranged between the first sublayer and the third sublayer.

5. The semiconductor module arrangement of claim **1**, wherein the sinter paste comprises at least one of copper and silver.

6. The semiconductor module arrangement of claim **1**, wherein the dielectric insulation layer comprises one of: Al_2O_3; AlN; ZrO_2; SiC; BeO; BN; and Si_3N_4.

7. The semiconductor module arrangement of claim **1**, wherein the base plate comprises one of: AlSiC; AlC; Al; MgSiC; and Cu.

8. The semiconductor module arrangement of claim **1**, wherein:

the substrate has a width in a first horizontal direction that is at least 30 millimeters; and

the substrate has a length in a second horizontal direction perpendicular to the first horizontal direction that is at least 40 millimeters.

9. The semiconductor module arrangement of claim **1**, wherein the dielectric insulation layer has a first coefficient of thermal expansion (CTE1), the base plate has a second coefficient of thermal expansion (CTE2), and the connection layer has a third coefficient of thermal expansion (CTE3), and wherein CTE1<CTE3<CTE2.

10. The semiconductor module arrangement of claim **1**, wherein the adhesion promoter comprises titanium, chromium, or vanadium.

11. A method, comprising:

forming a connection layer;

arranging a substrate on a base plate with the connection layer arranged between the substrate and the base plate; and

performing a sintering process that connects the substrate to the base plate by the connection layer,

wherein the substrate comprises a dielectric insulation layer and a metallization layer arranged on a first side of the dielectric insulation layer,

wherein when the substrate is arranged on the base plate, the connection layer directly adjoins the base plate and a second side of the dielectric insulation layer, opposite the first side,

wherein the connection layer comprises a sinter paste and an adhesion promoter.

12. The method of claim **11**, wherein forming the connection layer comprises mixing the sinter paste with the adhesion promoter.

13. The method of claim **12**, further comprising:

after mixing the sinter paste with the adhesion promoter, forming the connection layer on a surface of the base plate.

14. The method of claim **12**, further comprising:

after mixing the sinter paste with the adhesion promoter, forming the connection layer on the second side of the dielectric insulation layer.

15. The method of claim **11**, wherein forming the connection layer comprises forming a second sublayer consisting of the sinter paste and forming a first sublayer consisting of the adhesion promoter on a first surface of the second sublayer.

16. The method of claim **15**, wherein forming the connection layer further comprises forming a third sublayer on the second sublayer, such that the second sublayer is arranged between the first sublayer and the third sublayer.

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