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PIXEL ARRAY AND METHOD FOR MANUFACTURING THE SAME

Abstract

A pixel array may include a plurality of pixel regions including a first pixel region and a second pixel region. The pixel array may include a metal grid structure over the plurality of pixel regions. The pixel array may include a light blocking layer. A first portion of the light blocking layer may be over the first pixel region and under the metal grid structure. The first portion may have a first thickness. A second portion of the light blocking layer may be over the second pixel region and under the metal grid structure. The second portion may have a second thickness that is different from the first thickness.

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Background/Summary

RELATED APPLICATION
[0001] This application is a divisional of U.S. patent application Ser. No. 16/949,928, filed Nov. 20, 2020, which is incorporated herein by reference in its entirety.
BACKGROUND
[0002] An image sensor, such as a complementary metal oxide semiconductor (CMOS) image sensor, includes an array of pixel regions and supporting logic. The pixel regions of the array are semiconductor devices for measurements of incident light (i.e., light that is directed toward the pixel regions), and the supporting logic facilitates readout of the measurements.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0003] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.
[0004] FIG. **1** is a diagram of an example environment in which systems and/or methods described herein may be implemented.
[0005] FIGS. **2**A-**2**N are diagrams of an example of forming a pixel array that enables light emitting diode (LED) flicker reduction and improved dynamic range, as described herein.
[0006] FIG. **3** is a diagram of an example another pixel array that enables LED flicker reduction and improved dynamic range, as described herein.
[0007] FIG. **4** is a diagram of example components of one or more devices of FIG. **1**.
[0008] FIG. **5** is a flowchart of an example process relating to forming a pixel array that enables LED flicker reduction and improved dynamic range.
DETAILED DESCRIPTION
[0009] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.
[0010] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper,” “front,” “back,” “over,” and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.
[0011] In general, image sensors, such as charge coupled device (CCD) and CMOS image sensors, have a dynamic range of approximately 70 decibels (dB). An image sensor with a high dynamic

range (e.g., 100 dB or more) may be needed in some applications. For example, an image sensor with a dynamic range of 100 dB or more may be needed in an automotive application to be able to handle different extreme lighting conditions, such as driving from a dark tunnel into bright sunlight. Another example of an extreme lighting condition in the automotive context occurs when the image sensor needs to image light emitting diode (LED) illuminated light sources (e.g., vehicle lights, traffic lights, signs, and/or the like) that are pulsed at for example 90-300 Hertz (Hz) with a high peak light intensity. In such an LED lighting situation, there is often flickering present in output images caused by the LED light sources, which can result in unreliable or inaccurate image sensing. Thus, in addition to requiring a high dynamic range, the image sensor may need to employ an LED flicker reduction (LFR) technique.

[0012] One technique for providing LED flicker reduction is to include pixel regions in the array that have a low quantum efficiency (QE) (e.g., as compared to a QE of “standard” pixel regions of the array). The low QE pixel regions have a longer integration time without being overexposed, which facilitates capture of LED light and, therefore, can be utilized to reduce LED flicker. In some cases, low QE is achieved in a pixel region by partially blocking light received by the pixel region. The partial light blocking can be achieved by forming a light blocking layer above the pixel region. The light blocking layer can be, for example, a metal layer, such as a titanium (Ti) layer or a titanium nitride (TiN) layer. The light blocking layer is formed over a metal grid structure of the pixel array, where the metal grid structure is a structure designed to provide isolation of pixel regions in the array and to direct incoming light (e.g., toward a pixel region).

[0013] In practice, tight control of both thickness and uniformity of the light blocking layer are critical for providing a low QE pixel region. However, the thickness and the uniformity of the light blocking layer are impacted by a design of the metal grid structure. Therefore, as dimensions of the metal grid structure become smaller and smaller, the light blocking layer is impacted. For example, with miniaturization of pixel arrays, widths of pillars of the metal grid structure become smaller, meaning that formation of the light blocking layer such that the light blocking layer lies on the pillars becomes challenging or even impossible. As another example, distances between the pillars of the metal grid structure decrease with miniaturization of pixel arrays, meaning that controlling thickness and uniformity of the light blocking layer between the pillars becomes challenging or even impossible.

[0014] Some implementations described herein provide techniques and apparatuses for a pixel array that provides LFR and improves dynamic range. In some implementations, the pixel array includes a plurality of pixel regions and a metal grid structure over the plurality of pixel regions. In some implementations, the pixel array includes a light blocking layer, a first portion of which is over a first pixel region and under the metal grid structure and a second portion of which is over the second pixel region and under the metal grid structure. Here, the first portion of the light blocking layer has a first thickness and the second portion of the light blocking layer has a second thickness that is different from (e.g., greater than or less than) the first thickness. In some implementations, the pixel array includes a third pixel region, and the light blocking layer is not present substantially over the third pixel region.

[0015] Notably, the light blocking layer is formed before the metal grid structure, meaning that the light blocking layer is beneath the metal grid structure (e.g., rather than being formed on or over the metal grid structure). By forming the light blocking layer such that the light blocking layer is beneath the metal grid structure, dimensions of the metal grid structure do not impact uniformity and thickness of the light blocking layer. As a result, the uniformity and thickness of the light blocking layer can be tightly controlled even with miniaturization of the metal grid structure, without impacting performance of the pixel array.

[0016] Furthermore, a thickness of the light blocking layer can differ over different pixel regions of the pixel array. For example, as noted above, the light blocking layer can have a first thickness over the first pixel region, can have a second (different) thickness over the second pixel region, and may

not be present over the third pixel region. As a result, QEs vary among the pixel regions of the pixel array. For example, the first pixel region may be a low QE region (e.g., when the first thickness is greater than the second thickness), the second pixel region may be a middle QE region, and the third pixel region may be a normal QE region (e.g., since no light blocking layer is formed over the third pixel region). Such a multi-QE pixel array improves dynamic range of the pixel array. Further, in some implementations, the light blocking layer may serve to reduce crosstalk between pixel regions of the pixel array. Additional details are provided below.

[0017] FIG. **1** is a diagram of an example environment **100** in which systems and/or methods described herein may be implemented. As shown in FIG. **1**, environment **100** may include a plurality of semiconductor processing tools **102**-**114** and a wafer/die handling device **116**. The plurality of semiconductor processing tools **102**-**114** may include a deposition tool **102**, an exposure tool **104**, a developer tool **106**, an etch tool **108**, a photoresist removal tool **110**, a planarization tool **112**, an implantation tool **114**, and/or another type of semiconductor processing tool. The tools included in example environment **100** may be included in a semiconductor clean room, a semiconductor foundry, a semiconductor processing and/or manufacturing facility, and/or the like.

[0018] The deposition tool **102** is a semiconductor processing tool that includes a semiconductor processing chamber and one or more devices capable of depositing various types of materials onto a substrate. In some implementations, the deposition tool **102** includes a spin coating tool that is capable of depositing a photoresist layer on a substrate such as a wafer. In some implementations, the deposition tool **102** may deposit a metal material to form one or more conductors or conductive layers, may deposit an insulating material to form a dielectric or insulating layer, and/or the like as described herein. In some implementations, the deposition tool **102** includes a chemical vapor deposition (CVD) tool such as a plasma-enhanced CVD (PECVD) tool, a high-density plasma CVD (HDP-CVD) tool, a sub-atmospheric CVD (SACVD) tool, a plasma-enhanced atomic layer deposition (PEALD) tool, or another type of CVD tool. In some implementations, the deposition tool **102** includes a physical vapor deposition (PVD) tool, such as a sputtering tool or another type of PVD tool. In some implementations, the example environment **100** includes a plurality of types of deposition tools **102**.

[0019] The exposure tool **104** is a semiconductor processing tool that is capable of exposing a photoresist layer to a radiation source, such as an ultraviolet light (UV) source (e.g., a deep UV light source, an extreme UV light source, and/or the like), an x-ray source, and/or the like. The exposure tool **104** may expose a photoresist layer to the radiation source to transfer a pattern from a photomask to the photoresist layer. The pattern may include one or more semiconductor device layer patterns for forming one or more semiconductor devices, may include a pattern for forming one or more structures of a semiconductor device, may include a pattern for etching various portions of a semiconductor device, and/or the like. In some implementations, the exposure tool **104** includes a scanner, a stepper, or a similar type of exposure tool.

[0020] The developer tool **106** is a semiconductor processing tool that is capable of developing a photoresist layer that has been exposed to a radiation source to develop a pattern transferred to the photoresist layer from the exposure tool **104**. In some implementations, the developer tool **106** develops a pattern by removing unexposed portions of a photoresist layer. In some implementations, the developer tool **106** develops a pattern by removing exposed portions of a photoresist layer. In some implementations, the developer tool **106** develops a pattern by dissolving exposed or unexposed portions of a photoresist layer through the use of a chemical developer.

[0021] The etch tool **108** is a semiconductor processing tool that is capable of etching various types of materials of a substrate, wafer, or semiconductor device. For example, the etch tool **108** may include a wet etch tool, a dry etch tool, and/or the like. In some implementations, the etch tool **108** includes a chamber that is filled with an etchant, and the substrate is placed in the chamber for a particular time period to remove particular amounts of one or more portions of the substrate. In

some implementations, the etch tool **108** may etch one or more portions of the substrate using a plasma etch or a plasma-assisted etch, which may involve using an ionized gas to isotopically or directionally etch the one or more portions.

[0022] The photoresist removal tool **110** is a semiconductor processing tool that is capable of removing a portion of a photoresist layer deposited a substrate. For example, the photoresist removal tool **110** may remove remaining portions of the photoresist layer (e.g., using a chemical stripper and/or another technique) after the etch tool **108** etches the substrate **202**.

[0023] The planarization tool **112** is a semiconductor processing tool that is capable of polishing or planarizing various layers of a wafer or semiconductor device. For example, a polishing device may include a chemical mechanical polishing (CMP) device and/or another type of polishing device. In some implementations, the polishing device may polish or planarize a layer of deposited or plated material. A CMP process may include depositing a slurry (or polishing compound) onto a polishing pad. A wafer may be mounted to a carrier, which may rotate the wafer as the wafer is pressed against the polishing pad. The slurry and polishing pad act as an abrasive that polishes or planarizes one or more layers of the wafer as the wafer is rotated. The polishing pad may also be rotated to ensure a continuous supply of slurry is applied to the polishing pad.

[0024] The implantation tool **114** is a semiconductor processing tool that is used to implant ions into a substrate of a semiconductor wafer. In some implementations, the implantation tool **114** generates ions in an arc chamber from a source material such as a gas or a solid. The source material is provided into the arc chamber, and an arc voltage is discharged between a cathode and an electrode to produce a plasma containing ions of the source material. One or more extraction electrodes are used to extract the ions from the plasma in the arc chamber and accelerate the ions to form an ion beam. In some implementations, the implantation tool **114** can be used to form a SPAD in a substrate, as described herein.

[0025] Wafer/die handling device **116** includes a mobile robot, a robot arm, a tram or rail car, and/or another type of device that are used to handle wafers and/or dies and/or transport wafers and/or dies between semiconductor processing tools **102-114** and/or to and from other locations such as a wafer rack, a storage room, and/or the like. In some implementations, wafer/die handling device **116** may be a programmed device to travel a particular path and/or may operate semi-autonomously or autonomously.

[0026] The number and arrangement of devices shown in FIG. **1** are provided as one or more examples. In practice, there may be additional devices, fewer devices, different devices, or differently arranged devices than those shown in FIG. **1**. Furthermore, two or more devices shown in FIG. **1** may be implemented within a single device, or a single device shown in FIG. **1** may be implemented as multiple, distributed devices. Additionally, or alternatively, a set of devices (e.g., one or more devices) of environment **100** may perform one or more functions described as being performed by another set of devices of environment **100**.

[0027] FIGS. **2**A-**2**N are diagrams of an example of forming a pixel array **200** (or a portion thereof) that enables LFR and improved dynamic range. The pixel array **200** may be included in an image sensor, such as a CMOS image sensor or another type of image sensor.

[0028] As shown in FIG. **2**A, as part of a process associated with forming pixel array **200**, a substrate **202** is provided. The substrate **202** may include a semiconductor die substrate, a semiconductor wafer, or another type of substrate in which semiconductor pixels may be formed. In some implementations, the substrate **202** is formed of silicon, a material including silicon, a III-V compound semiconductor material such as gallium arsenide (GaAs), a silicon on insulator (SOI), or another type of semiconductor material that is capable of generating a charge from photons of incident light. As shown in FIG. **2**A, the substrate **202** includes a first surface **202***a* and a second surface **202***b*.

[0029] As shown in FIG. **2**B, a plurality of pixel regions **203** of the pixel array **200** may be formed in the substrate **202**. For example, a pixel region **203***a* may be formed by doping a portion of the

substrate **202**, a pixel region **203***b* may be formed by doping another potion of the substrate **202**, a pixel region **203***c* may be formed by doping another portion of the substrate **202**, and so on. Some of the pixel regions **203** may be adjacent pixel regions (e.g., pixel regions that are next to and/or share a side with each other) and some of the pixel regions **203** may be non-adjacent pixel regions.
[0030] In some implementations, a semiconductor processing tool (e.g., the implantation tool **114**) dopes the portions of the substrate **202** using an ion implantation technique to form a photodiode **204** in each of the pixel regions **203** (e.g., a photodiode **204***a* in pixel region **203***a*, a photodiode **204***b* in pixel region **203***b*, a photodiode **204***c* in pixel region **203***c*, and so on). In these examples, the semiconductor processing tool may generate ions in an arc chamber from a source material such as a gas or a solid. The source material may be provided into the arc chamber, and an arc voltage is discharged between a cathode and an electrode to produce a plasma containing ions of the source material. One or more extraction electrodes may be used to extract the ions from the plasma in the arc chamber and accelerate the ions to form an ion beam. In some implementations, other techniques and/or types of ion implantation tools are used to form the ion beam. The ion beam may be directed at the pixel regions **203** to implant ions in the substrate **202**, thereby doping the substrate **202** to form the photodiodes **204** in each of the pixel regions **203**. In some implementations, the substrate **202** may be doped with a plurality of types of ions to form a p-n junction for each photodiode **204**. For example, the substrate **202** may be doped with an n-type dopant to form a first portion (e.g., an n-type portion) of a photodiode **204** and a p-type dopant to form a second portion (e.g., a p-type portion) of the photodiode **204**.
[0031] As shown in FIGS. **2**C-**2**E, one or more deep trench isolation (DTI) elements **208** are formed at sides of (e.g., at boundaries of) pixel regions **203** of the substrate **202**, where the one or more DTI elements **208** are formed in one or more openings **205** on the first surface **202***a* of the substrate **202**. In some implementations, a boundary of a pixel region **203** is defined by a near edge of a DTI element **208** at a side of the pixel region **203**, by a far edge of the DTI element **208** at the side of the pixel region **203**, by a substantial middle of the DTI element near to the pixel region **203**, or at another point relative to the DTI element **208** at the side of the pixel region **203**. In some implementations, a boundary of a given pixel region **203** may partially overlap a boundary of an adjacent pixel region **203**. For example, if a boundary of the pixel region **203***a* is defined by the far edge of the DTI element **208** between the pixel region **203***a* and the pixel region **203***b* and a boundary of the pixel region **203***b* is defined by the far edge of the DTI element **208** between the pixel region **203***a* and the pixel region **203***b*, then the boundary of the pixel region **203***a* partially overlaps the boundary of the pixel region **203***b*.
[0032] The DTI element **208** is an element to provide isolation for photodiodes **204** of the pixel array **200** (e.g., to reduce optical crosstalk between neighboring photodiodes **204** of the pixel array **200**). In particular, DTI elements **208** may be formed at or within boundaries of pixel regions **203** of the substrate **202**.
[0033] In some implementations, one or more semiconductor processing tools may be used to form the one or more DTI elements **208** in the substrate **202**. For example, the deposition tool **102** may form a photoresist layer on the first surface **202***a* of the substrate **202**, the exposure tool **104** may expose the photoresist layer to a radiation source to pattern the photoresist layer, the developer tool **106** may develop and remove portions of the photoresist layer to expose the pattern, and the etch tool **108** may etch the one or more portions of substrate **202** to form one or more openings **205**, as shown in FIG. **2**C. In some implementations, the photoresist removal tool **110** removes the remaining portions of the photoresist layer (e.g., using a chemical stripper and/or another technique) after the etch tool **108** etches the substrate **202**. Next, the deposition tool **102** may deposit a dielectric liner layer **206** (e.g., a layer formed from a material with a relatively high dielectric constant (K), such as silicon nitride, silicon oxide, oxynitride, or another type of high-K material) on the first surface **202***a* and surfaces of the openings **205**, as shown in FIG. **2**D. Next, the deposition tool **102** may fill the remainder of the openings **205** with a material (e.g., an oxide

material such as a silicon oxide (SiO.sub.x) or another dielectric material) that provides optical isolation, and the planarization tool **112** may remove excess dielectric material using a CMP technique. FIG. **2**E illustrates the pixel array **200** after filling of the openings **205** and the planarization. In some implementations, the one or more DTI elements **208** may be formed in a grid layout in which the one or more DTI elements **208** extend laterally across the substrate **202** and intersect at various locations.

[0034] As shown in FIG. **2**F, a first portion of a buffer layer **210** may be formed over the first surface **202***a* of substrate **202** (e.g., on the dielectric liner layer **206** and the DTI elements **208**). The buffer layer **210** may function as a passivation layer between the photodiodes **204** and the upper layers of the pixel array **200**. In some implementations, the buffer layer **210** includes an oxide material such as a silicon oxide (SiO.sub.x). In some implementations, a silicon nitride (SiN.sub.x), a silicon carbide (SiC.sub.x), or a mixture thereof, such as a silicon carbon nitride (SiCN), a silicon oxynitride (SiON), or another dielectric material is used in place of the buffer layer **210** as a passivation layer. In some implementations, a semiconductor processing tool (e.g., the deposition tool **102**) may deposit the material over the substrate **202** to form the first portion of the buffer layer **210**.

[0035] As shown in FIGS. **2**G-**2**J, a light blocking layer **212** is formed. The light blocking layer **212** is a layer to at least partially block light over one or more pixel regions **203** of the pixel array **200** in association with enabling LFR for the pixel array **200** and/or improving dynamic range of the pixel array **200**, as described herein. In some implementation light blocking layer s, the light blocking layer **212** may be formed from, for example, titanium (Ti), titanium nitride (TiN), or another type of material that at least partially blocks incoming light. In some implementations, portions of the light blocking layer **212** are present over one or more pixel regions **203** of the pixel array **200**, while no portion of the light blocking layer **212** is present substantially over one or more other pixel regions **203** of the pixel array **200**. For example, as illustrated in FIG. **2**J, a first portion of the light blocking layer **212** may be over the pixel region **203***a* and a second portion of the light blocking layer **212** may be over the pixel region **203***c*, but no portion of the light blocking layer **212** may be substantially over the pixel region **203***b* (e.g., no portion of the light blocking layer **212** is present directly above the photodiode **204***b* in the pixel region **203***b*, no portion of the light blocking layer **212** is present over an area between the DTI elements **208** at the sides of pixel region **203***b*, and/or the like). In some implementations, thicknesses vary among portions of the light blocking layer **212** formed over the pixel regions **203**, as described below. In some implementations, a given portion of the light blocking layer **212** has a thickness that is less than or equal to approximately 1000 angstroms. In some implementations, the light blocking layer **212** is under a metal grid structure **214** of the pixel array **200** (i.e., the light blocking layer **212** is formed before the metal grid structure **214** is formed).

[0036] In some implementations, one or more semiconductor processing tools may be used to form the light blocking layer **212**. For example, the deposition tool **102** may deposit a first layer of light blocking material (e.g., Ti, TiN, and/or the like) over the pixel regions **203** of the pixel array **200**, as shown in FIG. **2**G. The deposition tool **102** may form a photoresist layer on the first layer of light blocking material, the exposure tool **104** may expose the photoresist layer to a radiation source to pattern the photoresist layer, the developer tool **106** may develop and remove portions of the photoresist layer to expose the pattern, and the etch tool **108** may etch the one or more portions of the first layer of light blocking material to form a first layer of a portion of the light blocking layer **212** over the pixel region **203***a*, as shown in FIG. **2**H. In some implementations, the photoresist removal tool **110** removes the remaining portions of the photoresist layer (e.g., using a chemical stripper and/or another technique) after the etch tool **108** etches the first layer of light blocking material. The deposition tool **102** may deposit a second layer of the light blocking material over the pixel regions **203** of the pixel array **200**, as shown in FIG. **2**I. The deposition tool **102** may form a photoresist layer on the second layer of light blocking material, the exposure tool

104 may expose the photoresist layer to a radiation source to pattern the photoresist layer, the developer tool **106** may develop and remove portions of the photoresist layer to expose the pattern, and the etch tool **108** may etch the one or more portions of the second layer of light blocking material to form a second layer of the portion of the light blocking layer **212** over the pixel region **203***a* and a portion of the light blocking layer **212** over the pixel region **203***c*, as shown in FIG. **2**J. In some implementations, the photoresist removal tool **110** removes the remaining portions of the photoresist layer (e.g., using a chemical stripper and/or another technique) after the etch tool **108** etches the second layer of light blocking material.

[0037] In some implementations, the presence or absence of a portion of the light blocking layer **212** over a given pixel region **203** and a thickness of a portion of the light blocking layer **212** over the given pixel region **203** (when present) may be used to control a QE of the given pixel region **203**. For example, in the pixel array **200** shown in FIG. **2**J, the first portion of the light blocking layer **212** over the pixel region **203***a* has a first thickness, the second portion of the light blocking layer **212** over the pixel region **203***c* has a second thickness that is less than the first thickness, and no portion of the light blocking layer **212** is present directly above the photodiode **204***b* in the pixel region **203***b* such that the light blocking layer **212** is not substantially over the pixel region **203***b*. Here, the first thickness being greater than the second thickness causes a QE of the pixel region **203***a* to be lower than a QE of the pixel region **203***c*. Further, no portion of the light blocking layer **212** being substantially over the pixel region **203***b* causes the pixel region **203***b* to have a higher QE than the pixel region **203***a* and the pixel region **203***c*. Thus, in this example, the pixel region **203***a* may have a low QE region, the pixel region **203***c* may have a middle QE region, and the pixel region **203***b* may have a standard QE region (e.g., since the QE of the pixel region **203***b* is not modified by the light blocking layer **212**). In some implementations, as illustrated in FIG. **2**J, the low QE pixel region **203***a* and the middle QE pixel region **203***c* may be non-adjacent pixel regions **203** (e.g., the standard QE pixel region **203***b* may be between the low QE pixel region **203***a* and the middle QE pixel region **203***c* in the pixel array **200**).

[0038] In some implementations, a given portion of the light blocking layer **212** layer can extend to at least a boundary between a pixel region **203** and an adjacent pixel region **203**. For example, as shown in FIG. **2**J, the first portion of the light blocking layer **212** over the pixel region **203***a* can extend at least to a boundary between the pixel region **203***a* and the pixel region **203***b* (e.g., a boundary defined by a far edge of a DTI element **208** between the pixel region **203***a* and the pixel region **203***b* or at a point between a substantial middle of the DTI element **208** between the pixel region **203***a* and the pixel region **203***b*). Similarly, the second portion of the light blocking layer **212** over the pixel region **203***c* can extend at least to a boundary between the pixel region **203***c* and the pixel region **203***b* (e.g., a boundary defined by a far edge of a DTI element **208** between the pixel region **203***c* and the pixel region **203***b* or at a point between a substantial middle of the DTI element **208** between the pixel region **203***c* and the pixel region **203***b*). In some implementations, forming a portion of the light blocking layer **212** in this manner reduces crosstalk between pixel regions **203** of the pixel array **200**.

[0039] In some implementations, one or more portions of the light blocking layer **212** are formed beneath, on top of, and/or within the buffer layer **210**. In some implementations, one or more portions of the light blocking layer **212** may be formed such that the one or more portions of the light blocking layer **212** are at the bottom of the buffer layer **210** (e.g., deposited on the first surface **202***a* of substrate **202**, such as on the dielectric liner layer **206** and the DTI elements **208**). In some implementations, one or more portions of the light blocking layer **212** may be formed such that the one or more portions of the light blocking layer **212** are at the top of the buffer layer **210** (e.g., deposited on buffer layer **210**). In some implementations, one or more portions of the light blocking layer **212** may be formed such that the one or more portions of the light blocking layer **212** are within the buffer layer **210** (e.g., deposited on buffer layer **210** with an additional buffer layer **210** deposited on the one or more portions of the light blocking layer **212**, as shown in FIG.

2K).
[0040] As shown in FIG. **2**K, a second portion of buffer layer **210** may be formed over the first surface **202***a* of substrate **202** (e.g., on the light blocking layer **212** and the first portion of the buffer layer **210**). In some implementations, a semiconductor processing tool (e.g., the deposition tool **102**) may deposit the material over the substrate **202** to form the second portion of the buffer layer **210** and the planarization tool **112** may remove excess material using a CMP technique. In some implementations, a total thickness of the buffer layer **210** may be in a range from approximately 500 angstroms to approximately 3000 angstroms.
[0041] As shown in FIGS. **2**L and **2**M, a metal grid structure **214** may be formed on over the plurality of pixel regions **203** (e.g., on the buffer layer **210**). The metal grid structure **214** is a structure to improve isolation among photodiodes **204** of the pixel array **200**. For example, the metal grid structure **214** may direct light between a given photodiode **204** and a neighboring photodiode **204** such that optical crosstalk is reduced and/or such that light sensitivity of the photodiode **204** is improved. In some implementations, the metal grid structure **214** includes a metal material, such as tungsten or another type of metal material with reflective properties. In some implementations, the metal grid structure **214** is formed in a grid layout in which the metal grid structure **214** extends laterally across the substrate **202** and intersects at various locations. In some implementations, a height of an element of the metal grid structure **214** may be in a range from approximately 1500 angstroms to approximately 3000 angstroms. In some implementations, a width of an element of the metal grid structure **214** may be in a range from approximately 190 nanometers to approximately 500 nanometers.
[0042] In some implementations, one or more semiconductor processing tools may be used to form the metal grid structure **214**. For example, the deposition tool **102** may deposit a layer of metal material from which the metal grid structure **214** is to be formed, as shown in FIG. **2**L. The deposition tool **102** may form a photoresist layer on the layer of metal material, the exposure tool **104** may expose the photoresist layer to a radiation source to pattern the photoresist layer, the developer tool **106** may develop and remove portions of the photoresist layer to expose the pattern, and the etch tool **108** may etch the one or more portions of the layer of metal material to from metal grid elements of the metal grid structure **214**, as shown in FIG. **2**M. In some implementations, the photoresist removal tool **110** removes the remaining portions of the photoresist layer (e.g., using a chemical stripper and/or another technique) after the etch tool **108** etches the layer of metal material.
[0043] As shown in FIG. **2**N, an oxide layer **216** may be formed over the first surface **202***a* of substrate **202** (e.g., on the metal grid structure **214** and the buffer layer **210**). In some implementations, the oxide layer **216** may function to provide protection for other layers of the pixel array **200**. In some implementations, the oxide layer **216** includes an oxide material such as a silicon oxide (SiO.sub.x). In some implementations, a semiconductor processing tool (e.g., the deposition tool **102**) may deposit the material over the substrate **202** to form the oxide layer **216**.
[0044] The number and arrangement of components, structures, and/or layers shown in FIGS. **2**A-**2**N are provided as one or more examples. In practice, there may be additional components, structures, and/or layers; fewer components, structures, and/or layers; different components, structures, and/or layers; and/or differently arranged components, structures, and/or layers than those shown in FIGS. **2**A-**2**N. That is, as indicated above, FIGS. **2**A-**2**N are provided as an example, and other examples may differ from what is described with regard to FIGS. **2**A-**2**N.
[0045] FIG. **3** is a diagram of a pixel array **200** that enables LFR and improved dynamic range. As shown in FIG. **3**, the pixel array **200** includes components described in connection with FIGS. **2**A-**2**N.
[0046] In the pixel array **200**, with regard to FIG. **3** and in contrast to FIGS. **2**A-**2**N, a length of a given portion of the light blocking layer **212** is shorter than a length of the light blocking layer **212** of the pixel array **200** of FIGS. **2**A-**2**N. For example, as shown in FIG. **3**, the first portion of the

light blocking layer **212** over the pixel region **203***a* can extend at least to a boundary between the pixel region **203***a* and the pixel region **203***b* (e.g., a boundary defined by a near edge of a DTI element **208** between the pixel region **203***a* and the pixel region **203***b*). Similarly, the second portion of the light blocking layer **212** over the pixel region **203***c* can extend at least to a boundary between the pixel region **203***c* and the pixel region **203***b* (e.g., a boundary defined by a near edge of a DTI element **208** between the pixel region **203***c* and the pixel region **203***b*). In some implementations, having a shorter length for a portion of the light blocking layer **212** for a given pixel region **203** reduces interference with operation of a neighbor pixel region **203** of the pixel array **200**.

[0047] As indicated above, FIG. **3** is provided as an example. Other examples may differ from what is described with regard to FIG. **3**.

[0048] FIG. **4** is a diagram of example components of a device **400**. In some implementations, one or more of the semiconductor processing tools **102-114** and/or the wafer/die handling device **116** may include one or more devices **400** and/or one or more components of device **400**. As shown in FIG. **4**, device **400** may include a bus **410**, a processor **420**, a memory **430**, a storage component **440**, an input component **450**, an output component **460**, and a communication component **470**.

[0049] Bus **410** includes a component that enables wired and/or wireless communication among the components of device **400**. Processor **420** includes a central processing unit, a graphics processing unit, a microprocessor, a controller, a microcontroller, a digital signal processor, a field-programmable gate array, an application-specific integrated circuit, and/or another type of processing component. Processor **420** is implemented in hardware, firmware, or a combination of hardware and software. In some implementations, processor **420** includes one or more processors capable of being programmed to perform a function. Memory **430** includes a random access memory, a read only memory, and/or another type of memory (e.g., a flash memory, a magnetic memory, and/or an optical memory).

[0050] Storage component **440** stores information and/or software related to the operation of device **400**. For example, storage component **440** may include a hard disk drive, a magnetic disk drive, an optical disk drive, a solid state disk drive, a compact disc, a digital versatile disc, and/or another type of non-transitory computer-readable medium. Input component **450** enables device **400** to receive input, such as user input and/or sensed inputs. For example, input component **450** may include a touch screen, a keyboard, a keypad, a mouse, a button, a microphone, a switch, a sensor, a global positioning system component, an accelerometer, a gyroscope, an actuator, and/or the like. Output component **460** enables device **400** to provide output, such as via a display, a speaker, and/or one or more light-emitting diodes. Communication component **470** enables device **400** to communicate with other devices, such as via a wired connection and/or a wireless connection. For example, communication component **470** may include a receiver, a transmitter, a transceiver, a modem, a network interface card, an antenna, and/or the like.

[0051] Device **400** may perform one or more processes described herein. For example, a non-transitory computer-readable medium (e.g., memory **430** and/or storage component **440**) may store a set of instructions (e.g., one or more instructions, code, software code, program code, and/or the like) for execution by processor **420**. Processor **420** may execute the set of instructions to perform one or more processes described herein. In some implementations, execution of the set of instructions, by one or more processors **420**, causes the one or more processors **420** and/or the device **400** to perform one or more processes described herein. In some implementations, hardwired circuitry may be used instead of or in combination with the instructions to perform one or more processes described herein. Thus, implementations described herein are not limited to any specific combination of hardware circuitry and software.

[0052] The number and arrangement of components shown in FIG. **4** are provided as an example. Device **400** may include additional components, fewer components, different components, or differently arranged components than those shown in FIG. **4**. Additionally, or alternatively, a set of

components (e.g., one or more components) of device **400** may perform one or more functions described as being performed by another set of components of device **400**.

[0053] FIG. **5** is a flowchart of an example process **500** relating to forming a pixel array **200** that enables LFR and improved dynamic range. In some implementations, one or more process blocks of FIG. **5** may be performed by a semiconductor processing tool (e.g., one or more of the semiconductor processing tools **102**-**114** described above). Additionally, or alternatively, one or more process blocks of FIG. **5** may be performed by one or more components of device **400**, such as processor **420**, memory **430**, storage component **440**, input component **450**, output component **460**, and/or communication component **470**.

[0054] As shown in FIG. **5**, process **500** may include forming a first photodiode in a first pixel region of a pixel array (block **510**). For example, one or more semiconductor processing tools (e.g., the implantation tool **114**) may form a first photodiode **204***a* in a first pixel region **203***a* of a pixel array **200**, as described above.

[0055] As further shown in FIG. **5**, process **500** may include forming a second photodiode in a second pixel region of the pixel array (block **520**). For example, one or more semiconductor processing tools (e.g., the implantation tool **114**) may form a second photodiode **204***c* in a second pixel region **203***c* of the pixel array **200**, as described above.

[0056] As further shown in FIG. **5**, process **500** may include forming a light blocking layer over at least the first pixel region and the second pixel region, the light blocking layer including a first portion over the first pixel region, the first portion having a first thickness, and the light blocking layer including a second portion over the second pixel region, the second portion having a second thickness that is different from the first thickness (block **530**). For example, one or more semiconductor processing tools (e.g., the deposition tool **102**, the etching tool **108**, and/or the like) may form a light blocking layer **212** over at least the first pixel region **203***a* and the second pixel region **203***c*, the light blocking layer **212** including a first portion over the first pixel region **203***a*, the first portion having a first thickness, and the light blocking layer **212** including a second portion over the second pixel region **203***c*, the second portion having a second thickness that is different from the first thickness, as described above.

[0057] As further shown in FIG. **5**, process **500** may include forming a metal grid structure above the first portion of the light blocking layer and the second portion of the light blocking layer (block **540**). For example, one or more semiconductor processing tools (e.g., the deposition tool **102**, the etching tool **108**, and/or the like) may form a metal grid structure **214** above the first portion of the light blocking layer **212** and the second portion of the light blocking layer **212**, as described above.

[0058] Process **500** may include additional implementations, such as any single implementation or any combination of implementations described below and/or in connection with one or more other processes described elsewhere herein.

[0059] In a first implementation, the second thickness being different from the first thickness causes a QE of the second pixel region **203***c* to be different from a QE of the first pixel region **203***a*.

[0060] In a second implementation, alone or in combination with the first implementation, process **500** includes forming a third photodiode **204***b* in a third pixel region **203***b* of the pixel array **200**, wherein no portion of the light blocking layer **212** is formed substantially over the third pixel region **203***b*.

[0061] In a third implementation, alone or in combination with one or more of the first and second implementations, forming the light blocking layer **212** comprises depositing a first layer of light blocking material over at least the first pixel region **203***a* and the second pixel region **203***c*, etching the first layer of light blocking material such that a portion of the first layer of light blocking material is over the first pixel region **203***a* and such that no portion of the first layer of light blocking material is over the second pixel region **203***c*, depositing a second layer of light blocking material over at least the first pixel region **203***a* and the second pixel region **203***c*, and etching the

second layer of light blocking material such that a portion of the second layer of light blocking material is over the first pixel region **203***a* and such that a portion of the second layer of light blocking material is over the second pixel region **203***c*.

[0062] In a fourth implementation, alone or in combination with one or more of the first through third implementations, process **500** includes depositing at least a portion of a buffer layer **210** prior to depositing the first layer of the light blocking material.

[0063] In a fifth implementation, alone or in combination with one or more of the first through fourth implementations, process **500** includes depositing at least a portion of a buffer layer **210** after etching the second layer of the light blocking material.

[0064] In a sixth implementation, alone or in combination with one or more of the first through fifth implementations, at least one of the first portion of the light blocking layer **212** is formed to extend to at least a boundary between the first pixel region **203***a* and a pixel region adjacent to the first pixel region **203***a*, or the second portion of the light blocking layer is formed to extend to at least a boundary between the second pixel region **203***c* and a pixel region adjacent to the second pixel region **203***c*.

[0065] Although FIG. **5** shows example blocks of process **500**, in some implementations, process **500** may include additional blocks, fewer blocks, different blocks, or differently arranged blocks than those depicted in FIG. **5**. Additionally, or alternatively, two or more of the blocks of process **500** may be performed in parallel.

[0066] In this way, a pixel array may include a light blocking layer that enables LFR and improves dynamic range. In some implementations, the light blocking layer is formed before the metal grid structure, meaning that the light blocking layer is beneath the metal grid structure (e.g., rather than being formed on or over the metal grid structure). By forming the light blocking layer such that the light blocking layer is beneath the metal grid structure, dimensions of the metal grid structure do not impact uniformity and thickness of the light blocking layer. As a result, the uniformity and thickness of the light blocking layer can be tightly controlled even with miniaturization of the metal grid structure, without impacting performance of the pixel array. Furthermore, a thickness of the light blocking layer can differ over different pixel regions of the pixel array, meaning that the pixel array may be a multi-QE pixel array that enables improved dynamic range. Additionally, in some implementations, the light blocking layer may serve to reduce crosstalk between pixel regions of the pixel array.

[0067] As described in greater detail above, some implementations described herein provide a pixel array. The pixel array includes a plurality of pixel regions including a first pixel region and a second pixel region. The pixel array includes a metal grid structure over the plurality of pixel regions. The pixel array includes a light blocking layer, a first portion of the light blocking layer being over the first pixel region and under the metal grid structure, the first portion having a first thickness, and a second portion of the light blocking layer being over the second pixel region and under the metal grid structure, the second portion having a second thickness that is different from the first thickness.

[0068] As described in greater detail above, some implementations described herein provide a method. The method includes forming a first photodiode in a first pixel region of a pixel array. The method includes forming a second photodiode in a second pixel region of the pixel array. The method includes forming a light blocking layer over at least the first pixel region and the second pixel region, the light blocking layer including a first portion over the first pixel region, the first portion having a first thickness, and the light blocking layer including a second portion over the second pixel region, the second portion having a second thickness that is different from the first thickness. The method includes forming a metal grid structure above the first portion of the light blocking layer and the second portion of the light blocking layer.

[0069] As described in greater detail above, some implementations described herein provide a pixel array. The pixel array includes a plurality of pixel regions including a first pixel region, a second

pixel region, and a third pixel region. The pixel array includes a metal grid structure including a first metal grid element and a second metal grid element, the first metal grid element being over a boundary between the first pixel region and the third pixel region, and the second metal grid element being over a boundary between the second pixel region and the third pixel region. The pixel array includes a light blocking layer above the plurality of pixel regions and below the metal grid structure, the light blocking layer including a first portion and a second portion, the first portion having a first thickness and being over the first pixel region and extending at least to a boundary between the first pixel region and the third pixel region, the second portion having a second thickness and being over the second pixel region and extending at least to a boundary between the second pixel region and the third pixel region or a fourth pixel region, the second thickness being different from the first thickness.

[0070] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

Claims

1. A method, comprising: forming a plurality of photodiodes in a plurality of pixel regions; forming one or more portions of one or more light blocking layers over the plurality of photodiodes; and forming a metal grid structure over the one or more portions of the one or more light blocking layers.

2. The method of claim 1, wherein the one or more portions of the one or more light blocking layers comprises: a first portion, over a first photodiode of the plurality of photodiodes, having a first thickness, and a second portion, over a second photodiode of the plurality of photodiodes, having a second thickness different from the first thickness.

3. The method of claim 2, wherein the plurality of photodiode comprises a third photodiode between the first photodiode and the second photodiode, wherein no portion of the one or more light blocking layers is over the third photodiode.

4. The method of claim 2, wherein the first portion is of a first light blocking layer of the one or more blocking layers, and wherein the second portion is of a second light blocking layer of the one or more blocking layers.

5. The method of claim 1, wherein forming the one or more portions of the one or more light blocking layers comprises: depositing a first light blocking layer, of the one or more light blocking layers, over at least the plurality of pixel regions; etching the first light blocking layer such that a portion of the first light blocking layer is over a first pixel region of the plurality of pixel regions and such that no portion of the first light blocking layer is over a second pixel region of the plurality of pixel regions; depositing a second light blocking layer, of the one or more light blocking layers, over the portion of the first light blocking layer and the second pixel region; and etching the second light blocking layer such that a portion of the second light blocking layer is over the second pixel region and such that no portion of the second light blocking layer is over the first light blocking layer.

6. The method of claim 1, wherein forming the one or more portions of one or more light blocking layers comprises: forming a buffer layer over the plurality of photodiodes; and forming the one or more portions of the one or more light blocking layers within the buffer layer.

7. The method of claim 6, wherein forming the buffer layer comprises: depositing a first portion of

the buffer layer over the plurality of photodiodes, wherein the one or more portions of the one or more light blocking layers are formed over the first portion of the buffer layer; and depositing a second portion of the buffer layer over the one or more portions of the one or more light blocking layers.

8. A method, comprising: forming a plurality of pixel regions in a substrate; forming one or more deep trench isolation (DTI) elements in the substrate and at sides of the plurality of pixel regions; and forming a buffer layer over the plurality of pixel regions and the one or more DTI elements, wherein the buffer layer comprises a first material, and the one or more DTI elements comprise a second material different from the first material.

9. The method of claim 8, wherein the one or more DTI elements comprises inwardly angled sidewalls.

10. The method of claim 8, wherein forming the one or more DTI elements comprises: forming one or more openings in the substrate and at the sides of the plurality of pixel regions; and forming the one or more DTI elements in the one or more openings.

11. The method of claim 10, wherein the one or more DTI elements comprises: forming a dielectric liner on a surface of the substrate and in the one or more openings; and forming the one or more DTI elements on a portion of the dielectric liner in the one or more openings.

12. The method of claim 11, wherein the buffer layer intersects with the dielectric liner and the one or more DTI elements.

13. The method of claim 8, further comprising: forming one or more portions of one or more light blocking layers within the buffer layer.

14. A method, comprising: forming a plurality of pixel regions in and entirely surrounded by a substrate; forming a plurality of deep trench isolation (DTI) elements in the substrate and at sides of the plurality of pixel regions; forming a buffer layer over the plurality of DTI elements; and forming a metal grid structure over the buffer layer and the plurality of DTI elements.

15. The method of claim 14, further comprising: forming an oxide layer over the buffer layer and the metal grid structure.

16. The method of claim 15, wherein the oxide layer intersects with the buffer layer and the metal grid structure.

17. The method of claim 15, wherein the metal grid structure intersects with the buffer layer and the oxide layer.

18. The method of claim 14, wherein the metal grid structure comprises a plurality of discrete elements that align with the plurality of DTI elements.

19. The method of claim 18, wherein at least one of: a height of the plurality of discrete elements of the metal grid structure is in a range from approximately 1500 angstroms to approximately 3000 angstroms, or a width of the plurality of discrete elements of the metal grid structure is in a range from approximately 190 nanometers to approximately 500 nanometers.

20. The method of claim 14, further comprising: forming a plurality of portions, of one or more light blocking layers and between different sets of the plurality of DTI elements, within the buffer layer.