US 20250260302A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2025/0260302 A1**

Chevallier et al. (43) **Pub. Date: Aug. 14, 2025**

(54) **CURRENT SENSING IN A MULTIPHASE POWER CONVERTER**

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(21) Appl. No.: **18/735,396**

(22) Filed: **Jun. 6, 2024**

Related U.S. Application Data

(60) Provisional application No. 63/553,400, filed on Feb. 14, 2024.

Publication Classification

(51) **Int. Cl.**

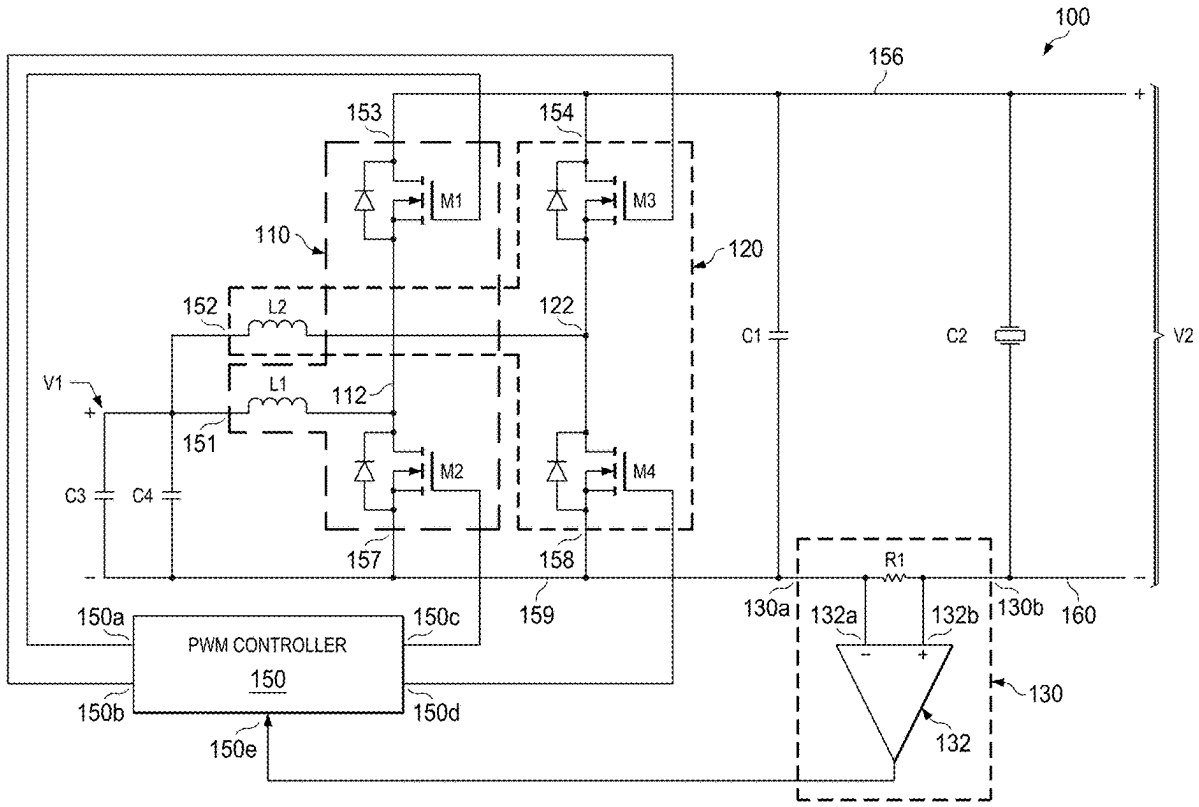
H02M 1/00	(2007.01)
G01R 19/165	(2006.01)
G01R 19/25	(2006.01)
H02M 3/157	(2006.01)
H02M 3/158	(2006.01)

(52) **U.S. Cl.**

CPC ***H02M 1/0009*** (2021.05); ***G01R 19/16528*** (2013.01); ***G01R 19/25*** (2013.01); ***H02M 3/157*** (2013.01); ***H02M 3/1586*** (2021.05)

(57) **ABSTRACT**

A multiphase power converter includes a first and second phase circuits and a current sense circuit. The first phase circuit has a first input, a first output, and a first terminal. The first output is coupled to a positive voltage terminal, and the first terminal is coupled to a first negative voltage terminal. The second phase circuit has a second input, a second output, and a second terminal. The second input is coupled to the first input, the second output is coupled to the positive voltage terminal, and the second terminal is coupled to the first negative voltage terminal. The current sense circuit has first and second current sense terminals. The first current sense terminal is coupled to the first negative voltage terminal and the second current sense terminal is coupled to a second negative voltage terminal.



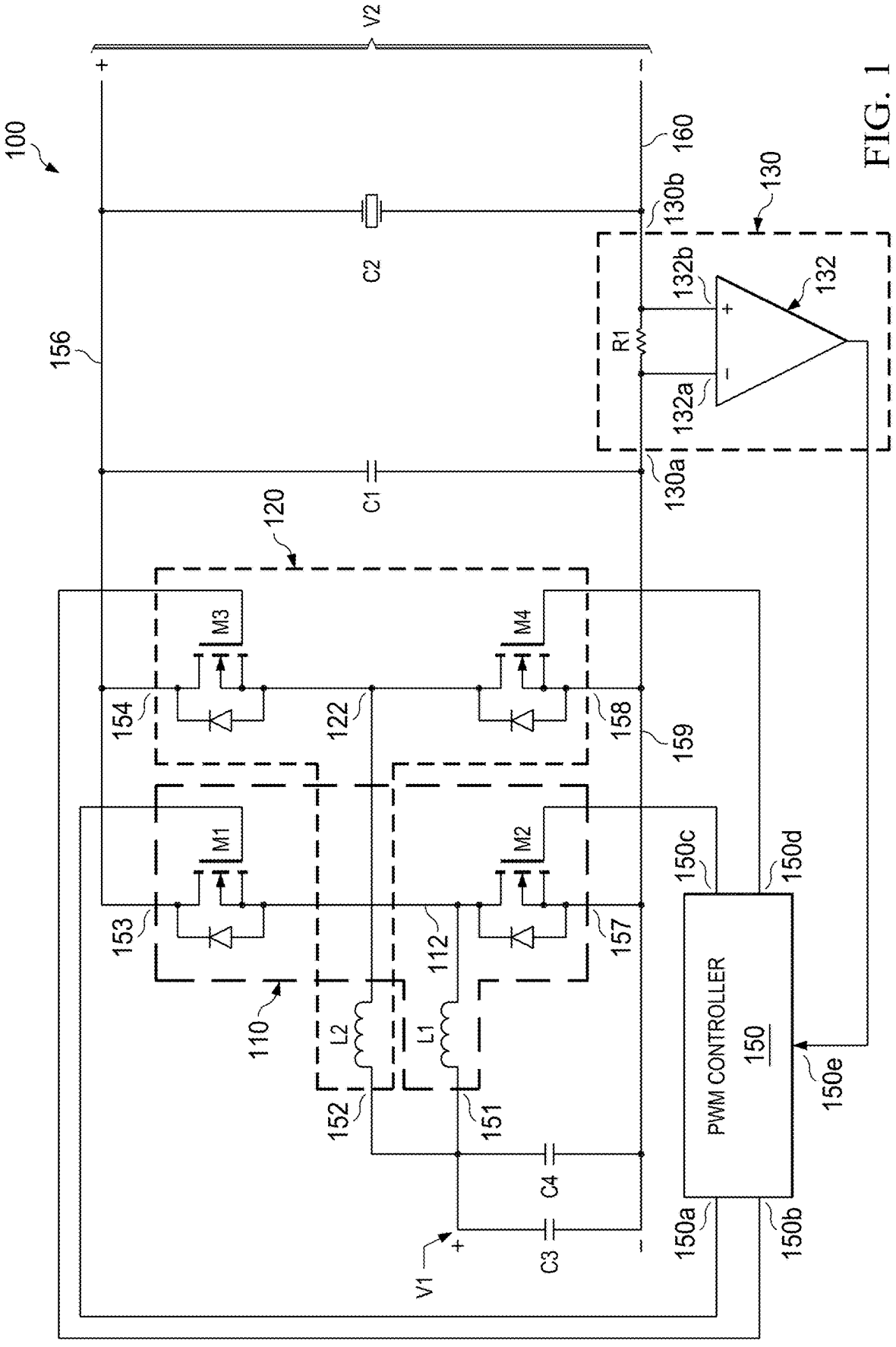

V2
+
-
100
160
130
130b
C2
132b
132
R1
+
-
156
132a
130a
C1
120
M3
M4
154
122
158
159
M1
M2
153
112
157
150c
150d
110
L2
L1
PWM CONTROLLER
150
152
151
150e
C4
C3
V1
+
-
150a
150b

FIG. 1

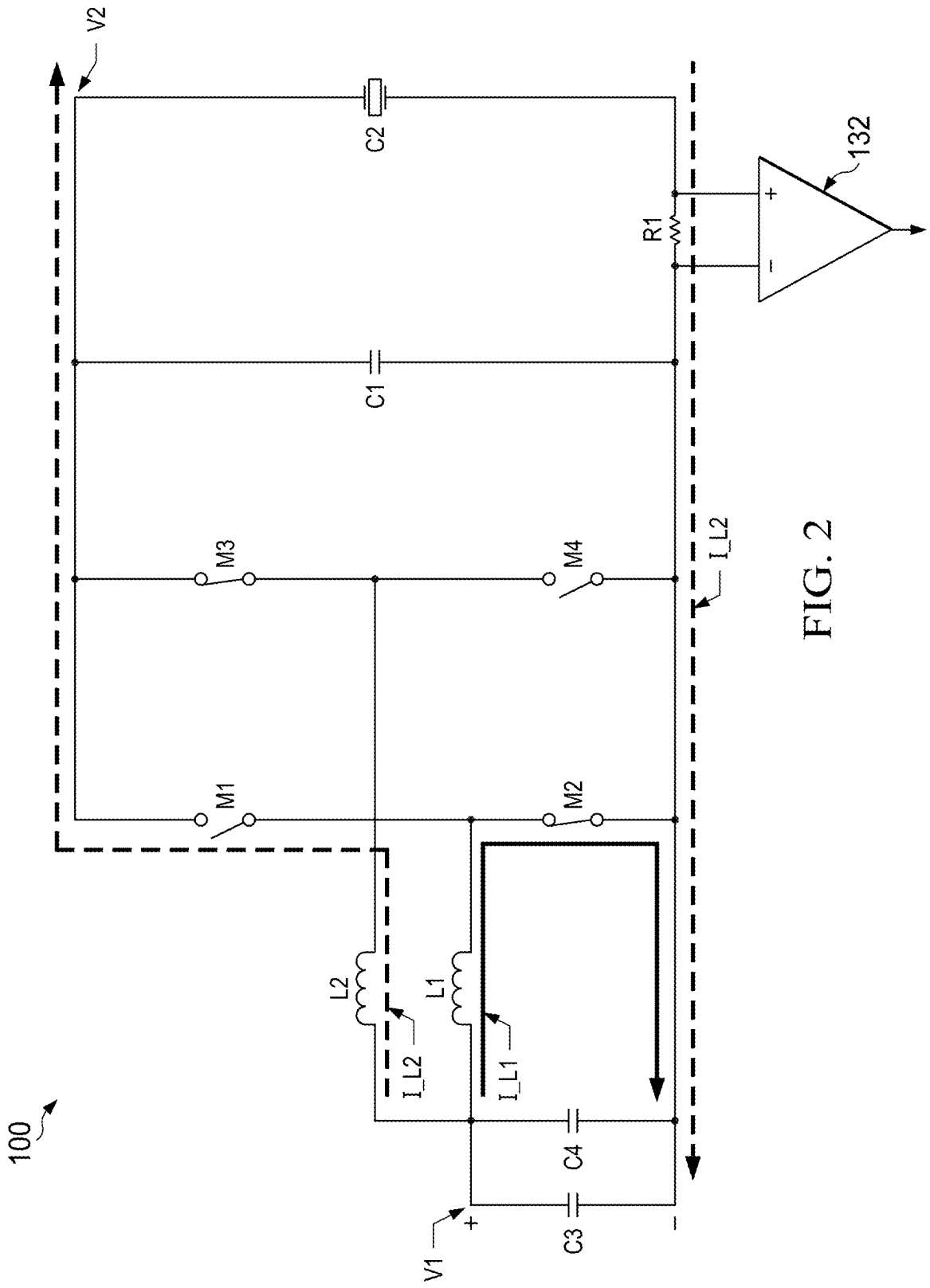


FIG. 2

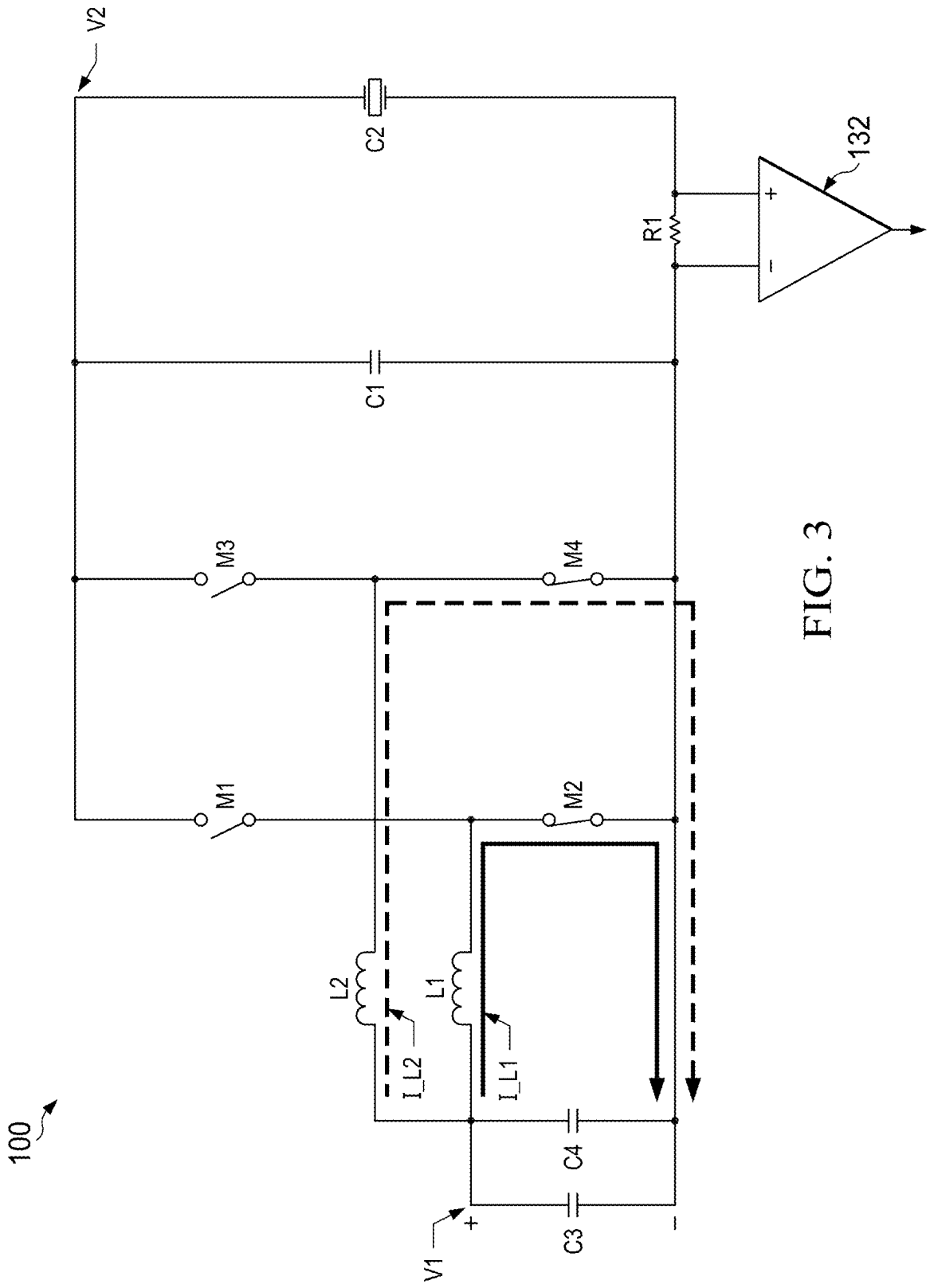


FIG. 3

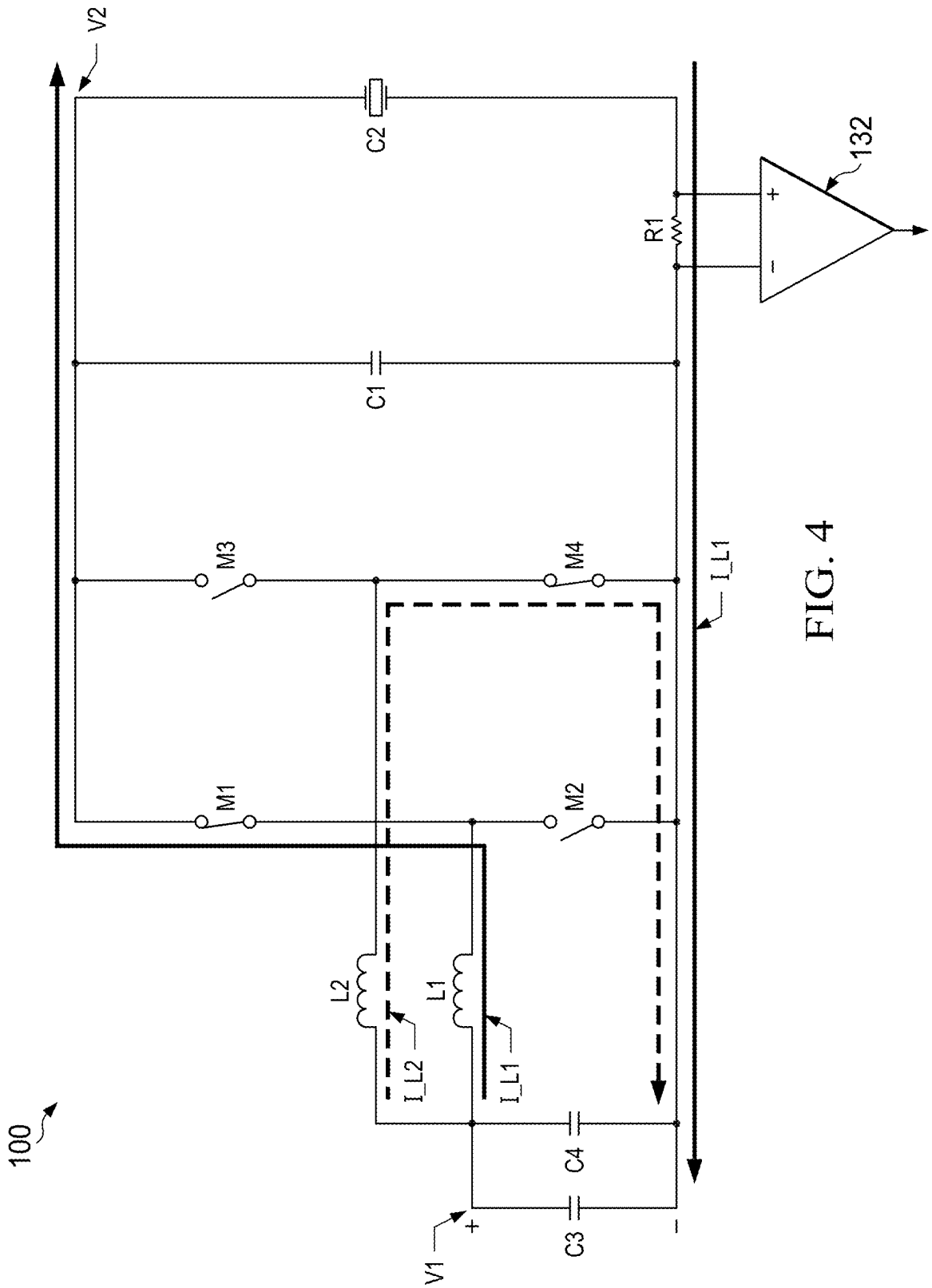


FIG. 4

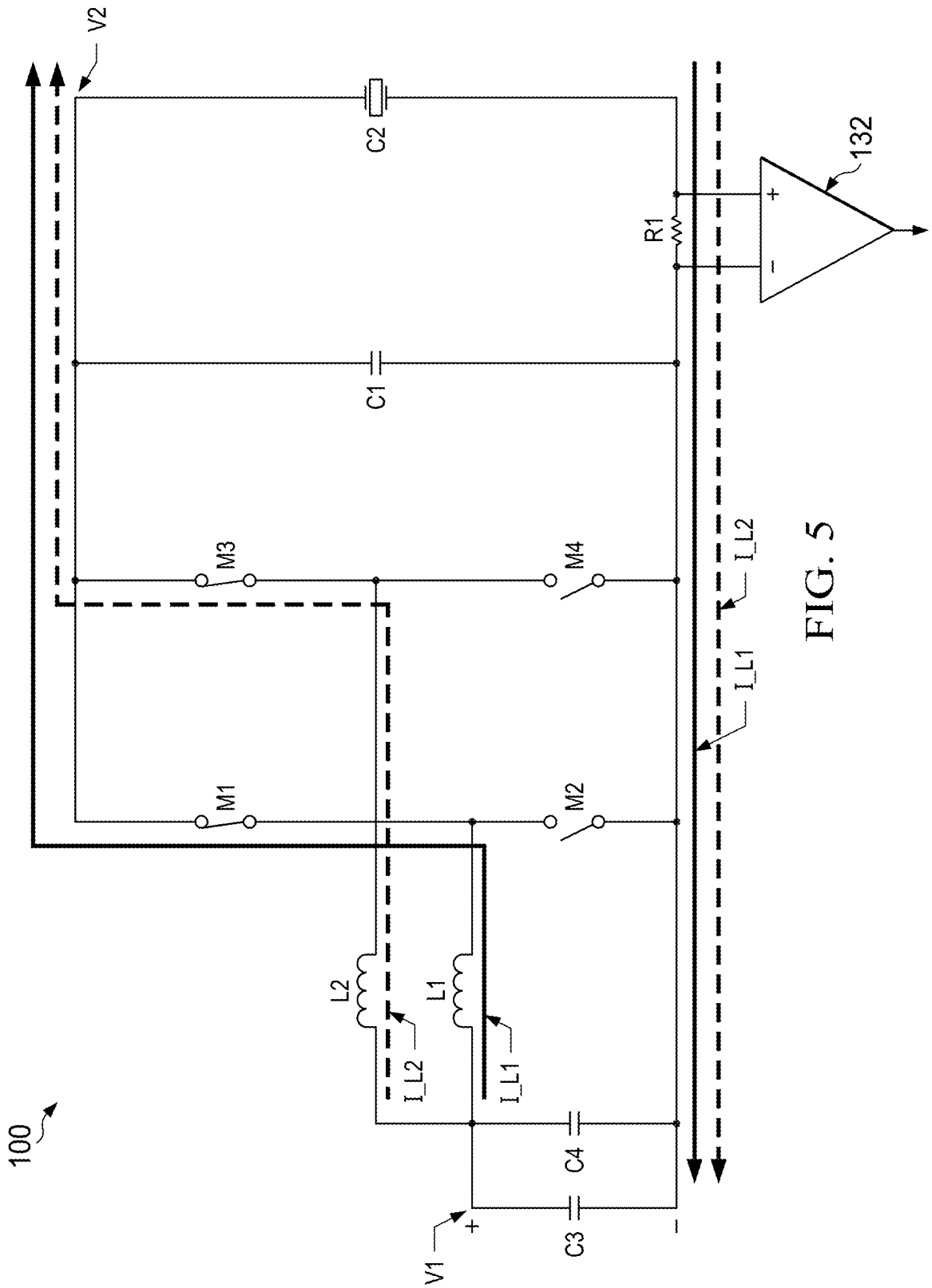


FIG. 5

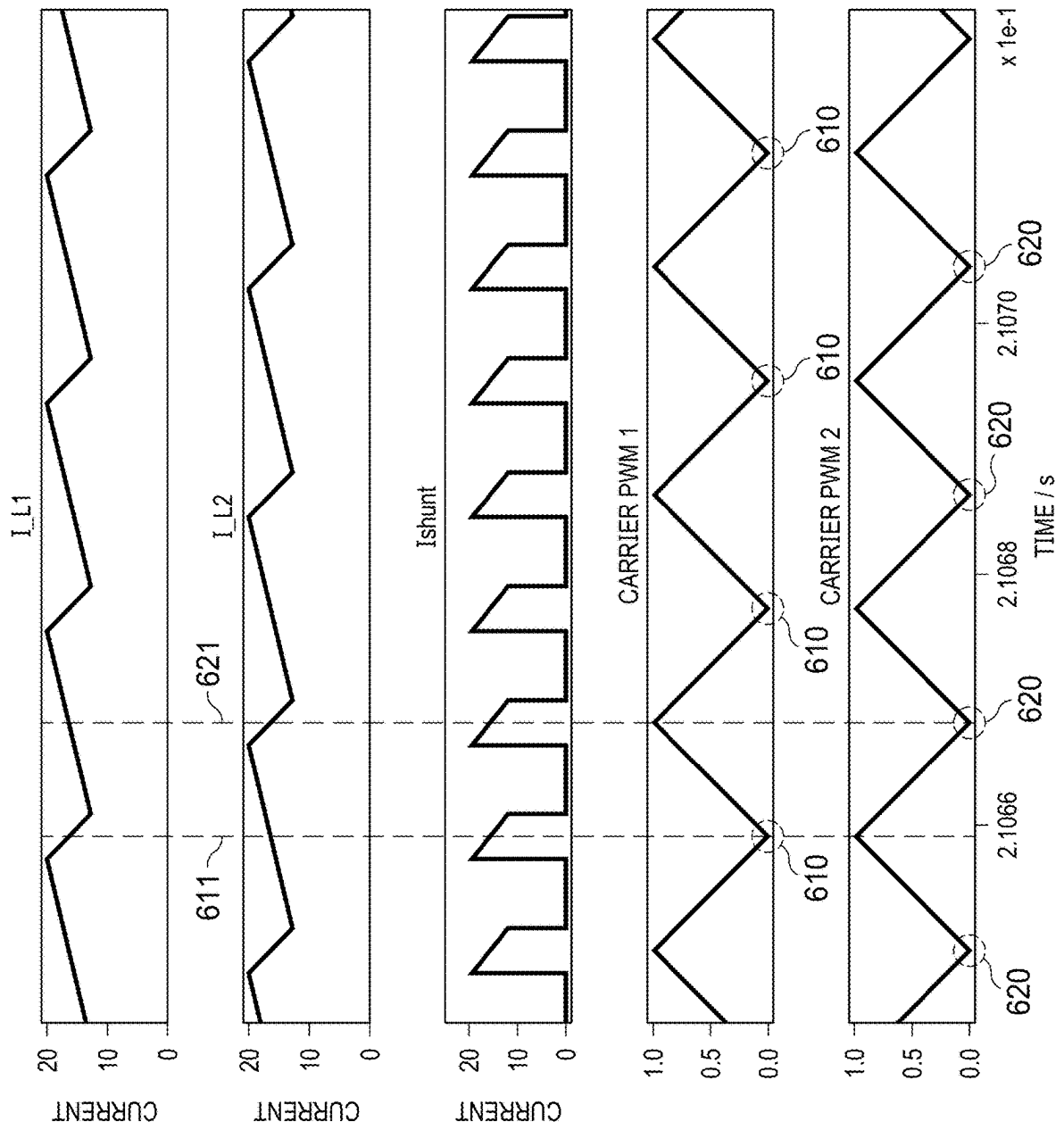

I_L1
I_L2
Ishunt
CARRIER PWM 1
CARRIER PWM 2
CURRENT
20
10
0
1.0
0.5
0.0
611
621
610
620
2.1066
2.1068
2.1070
TIME / s
x 1e-1

FIG. 6

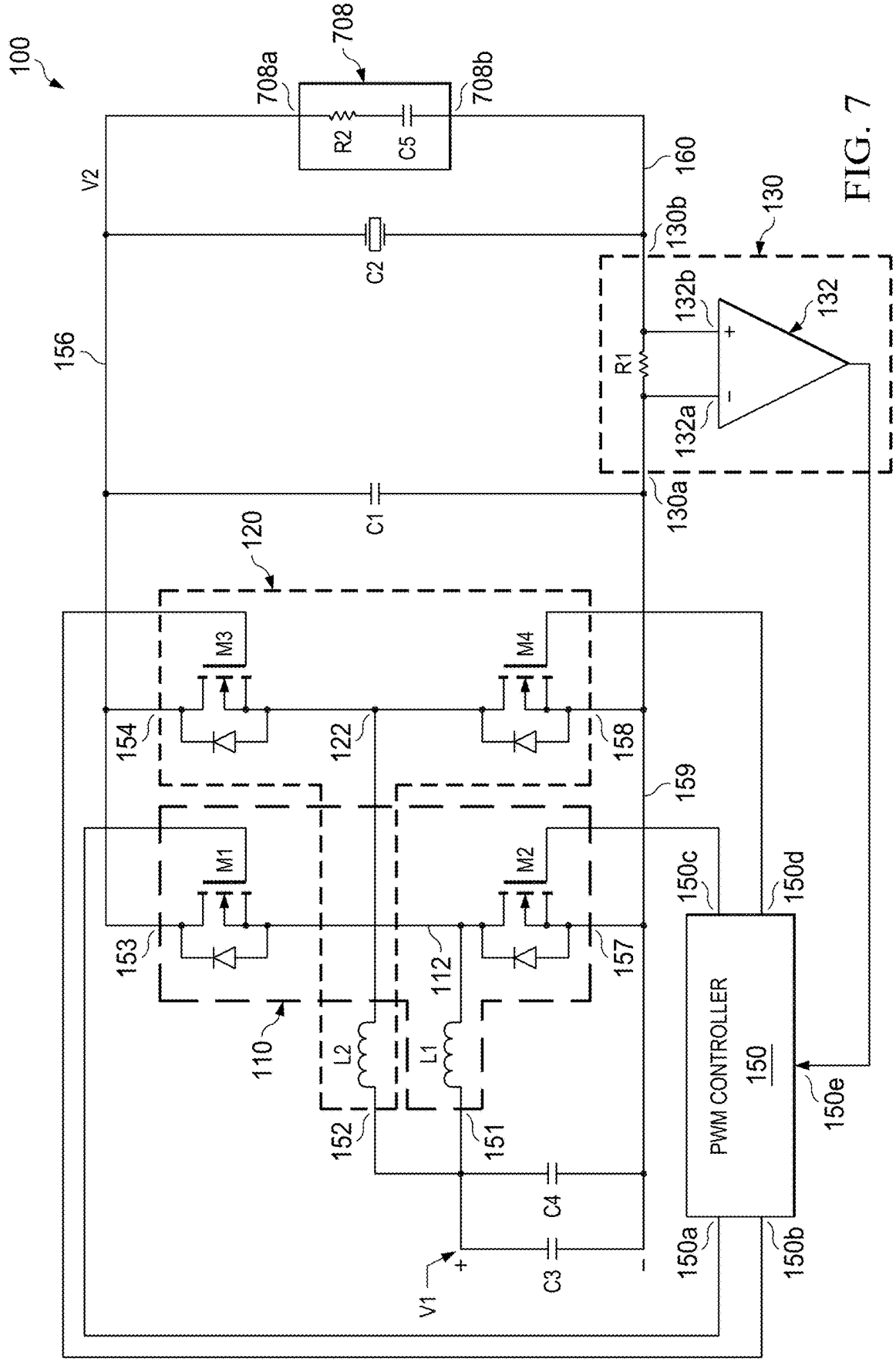

100
708
708a
708b
R2
C5
V2
160
130
130b
C2
132b
132
156
R1
132a
130a
C1
120
M3
M4
154
122
158
159
M1
M2
153
112
157
110
L2
L1
152
151
C4
C3
V1
150c
150d
PWM CONTROLLER
150
150e
150a
150b

FIG. 7

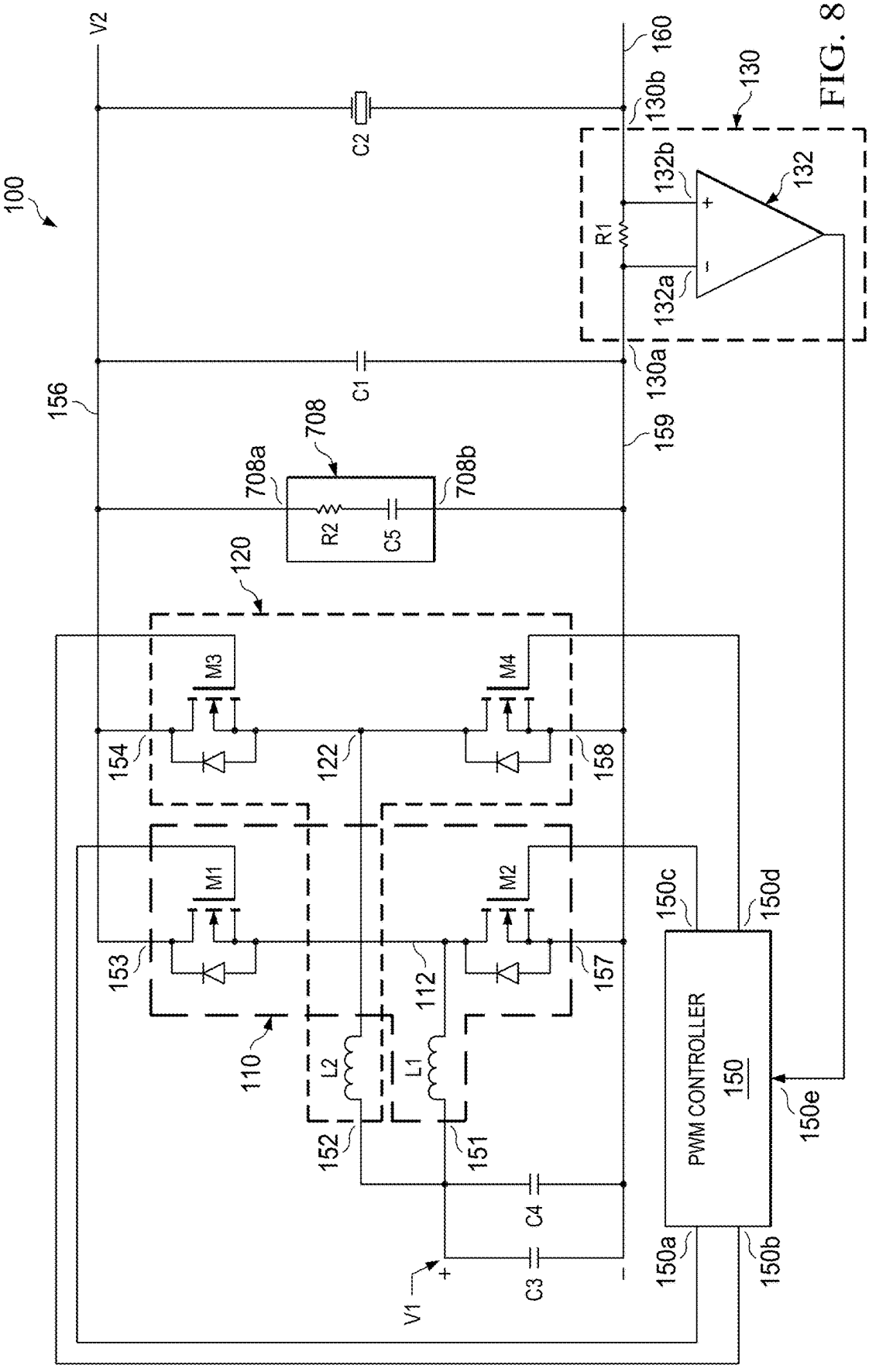

100
V2
C2
160
130
130b
132b
132
R1
132a
130a
C1
156
159
708
708a
708b
R2
C5
120
M3
M4
154
122
158
M1
M2
153
112
157
110
L2
L1
152
151
C4
C3
V1
PWM CONTROLLER
150
150a
150b
150c
150d
150e

FIG. 8

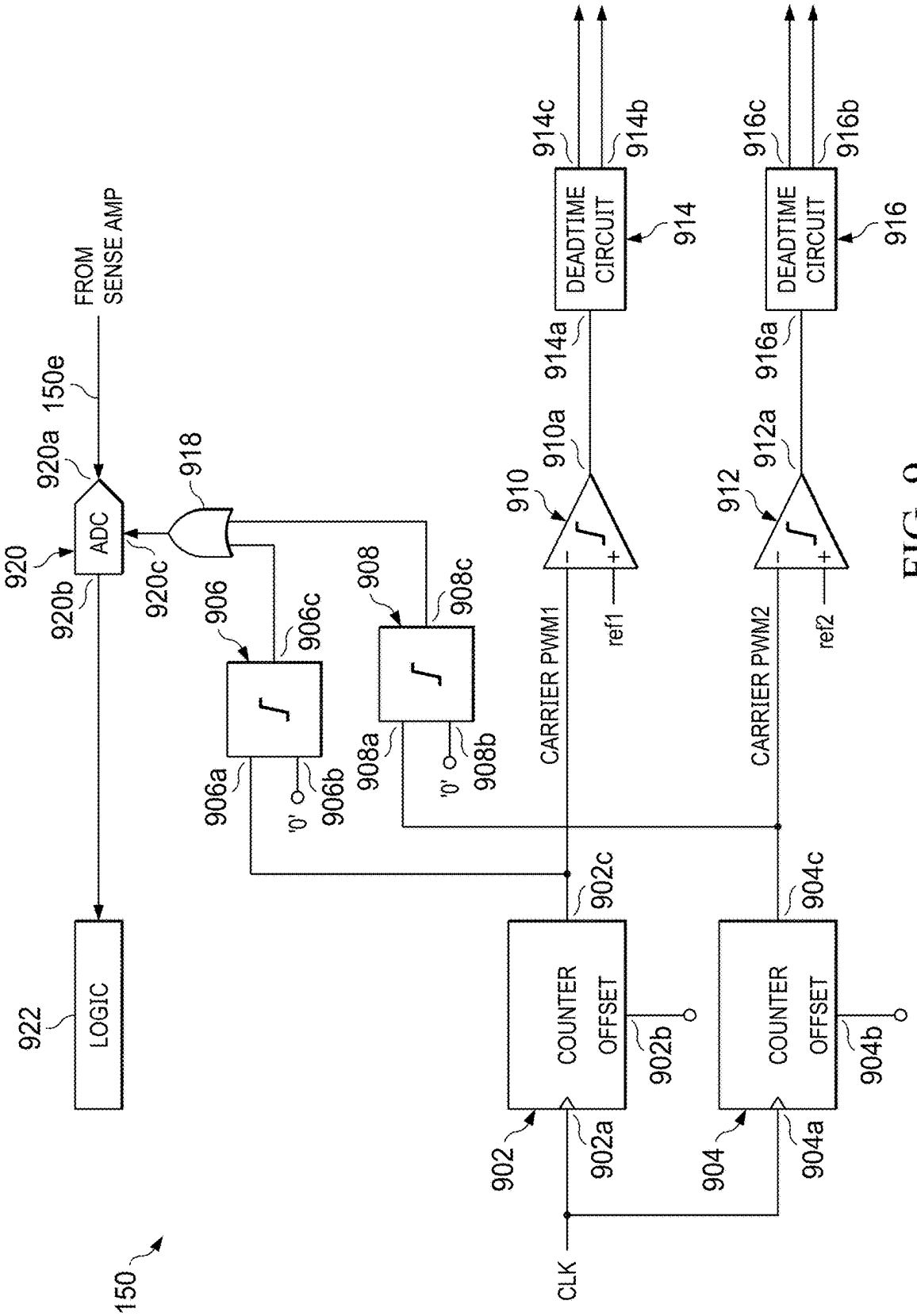

150
FROM SENSE AMP
150e
920
920a
920b
920c
ADC
918
922
LOGIC
906
906a
906b
906c
'0'
908
908a
908b
908c
'0'
910
910a
912
912a
CARRIER PWM1
CARRIER PWM2
ref1
ref2
914
914a
914b
914c
916
916a
916b
916c
DEADTIME CIRCUIT
DEADTIME CIRCUIT
902
902a
902b
902c
904
904a
904b
904c
COUNTER
OFFSET
COUNTER
OFFSET
CLK

FIG. 9

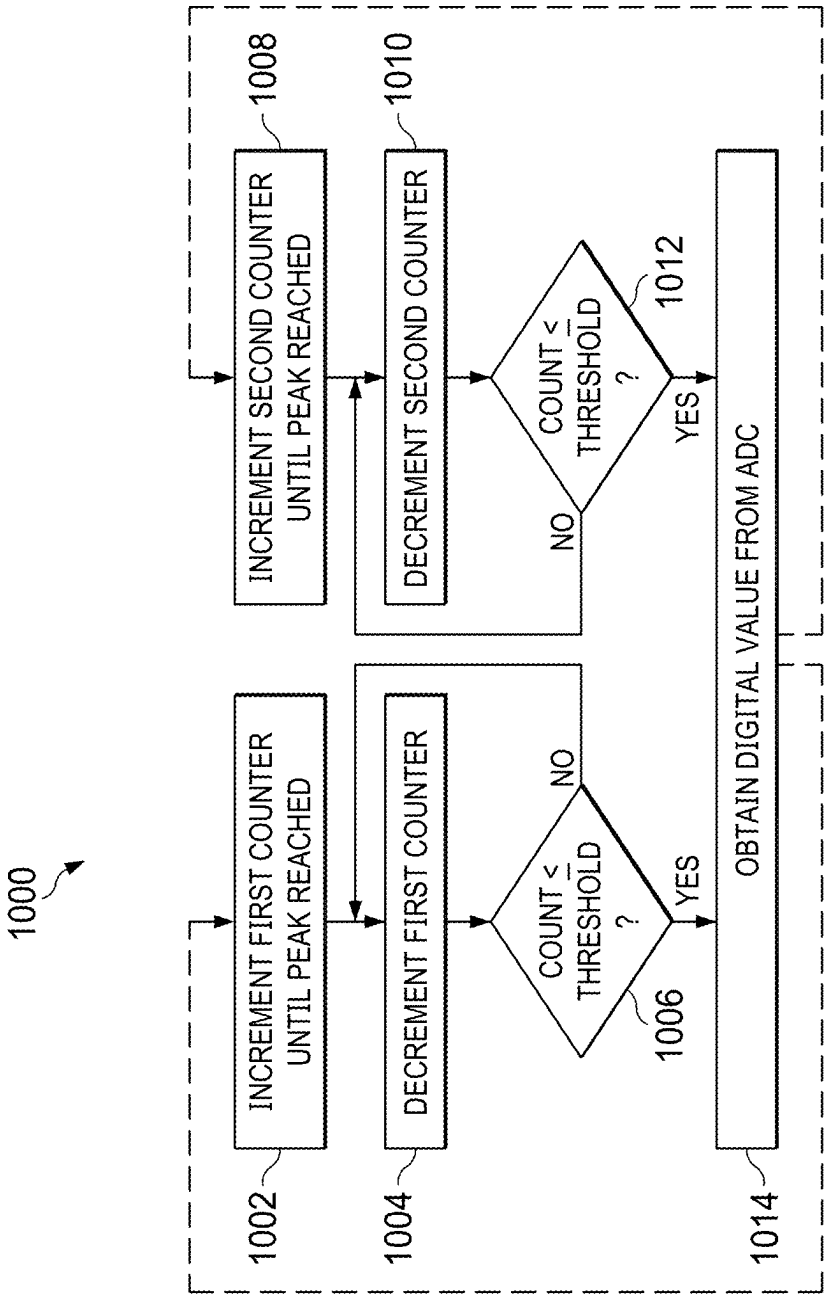

1000
INCREMENT FIRST COUNTER UNTIL PEAK REACHED
1002
DECREMENT FIRST COUNTER
1004
COUNT < THRESHOLD ?
1006
NO
YES
INCREMENT SECOND COUNTER UNTIL PEAK REACHED
1008
DECREMENT SECOND COUNTER
1010
COUNT < THRESHOLD ?
1012
NO
YES
OBTAIN DIGITAL VALUE FROM ADC
1014

FIG. 10

CURRENT SENSING IN A MULTIPHASE POWER CONVERTER

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to U.S. Provisional Application No. 63/553,400, filed Feb. 14, 2024, which is hereby incorporated by reference.

BACKGROUND

[0002] A multiphase power converter (also referred to as an interleaved power converter) includes two or more phases coupled together in parallel. Examples of multiphase power converters include boost converters, buck converters, and so on. the current through phases should approximately match each other. If the current through each phase is not approximately balanced, heat generated by the phases will not be equally shared, thereby contributing to reduced efficiency and reliability.

SUMMARY

[0003] In one example, a multiphase power converter includes a first and second phase circuits and a current sense circuit. The first phase circuit has a first input, a first output, and a first terminal. The first output is coupled to a positive voltage terminal, and the first terminal is coupled to a first negative voltage terminal. The second phase circuit has a second input, a second output, and a second terminal. The second input is coupled to the first input, the second output is coupled to the positive voltage terminal, and the second terminal is coupled to the first negative voltage terminal. The current sense circuit has first and second current sense terminals. The first current sense terminal is coupled to the first negative voltage terminal and the second current sense terminal is coupled to a second negative voltage terminal.

[0004] In another example, a multiphase power converter includes a first phase circuit having an input and an output, and a second phase circuit having an input coupled to the input of the first phase circuit and having an output coupled to the output of the first phase circuit. A first capacitor has first and second terminals. The first terminal of the first capacitor is coupled to the outputs of the first and second phase circuits. A second capacitor has first and second terminals. The first terminal of the second capacitor is coupled to the outputs of the first and second phase circuits. A resistor has first and second terminals, the first terminal of the resistor coupled to the second terminal of the first capacitor and the second terminal of the resistor coupled to second terminal of the second capacitor.

[0005] In yet another example, a circuit includes an analog-to-digital converter (ADC) having an analog input and a control input. A first comparator has first and second inputs and an output. The output of the first comparator is coupled to the control input. A second comparator has third and fourth inputs and an output. A first counter has an input and an output. The output of the first counter is coupled to the first and third inputs.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. **1** is a schematic diagram of a multiphase power converter, in an example.

[0007] FIGS. **2-4** represent four different states of operation of the multiphase power converter, in examples.

[0008] FIG. **6** is a timing diagram illustrating example waveforms for inductor currents, sense current, and PWM carrier waves of the multiphase power converter, in an example.

[0009] FIG. **7** is a schematic diagram of the multiphase power converter including a damping circuit in a first location within the multiphase power converter, in an example.

[0010] FIG. **8** is a schematic diagram of the multiphase power converter including the damping circuit in a second location within the multiphase power converter, in another example

[0011] FIG. **9** is a block diagram of a PWM controller in the multiphase power converter, in an example.

[0012] FIG. **10** is a flow diagram illustrating the operation of the PWM controller, in an example.

DETAILED DESCRIPTION

[0013] The same reference numbers or other reference designators are used in the drawings to designate the same or similar (either by function and/or structure) features.

[0014] Balancing the current between the phases of a multiphase power converter includes measuring the current in each phase. The multiphase power converter described herein implements current sensing that advantageously does not require multiple current sense circuits nor isolated circuits or devices for sensing current, e.g., isolated amplifiers, isolated Hall effect sensors for the current sense circuit.

[0015] FIG. **1** is a schematic diagram of a multiphase power converter **100**, in an example. In this example, multiphase power converter **100** includes two phases, but the principles described herein apply to any number of phases of a multiphase power converter. Multiphase power converter **100** includes phase circuits **110** and **120**, capacitors C**1**, C**2**, C**3**, and C**4**, a pulse width modulation (PWM) controller **150**, and a current sense circuit **130**. In one example, transistors M**1**-M**4**, capacitors C**1**-C**4**, inductors L**1** and L**2**, and PWM controller **150** are discrete components mounted on a printed circuit board (PCB).

[0016] Multiphase power converter **100** is a bidirectional power converter. For example, multiphase power converter **100** can receive a voltage V**1** and produce a larger voltage V**2** (boost converter), or receive a voltage V**2** and produce a voltage V**1** at a lower voltage level (buck converter). Phase circuits **110** and **120** have respective terminals **151** and **152** coupled together to receive or provide voltage V**1**. Phase circuits **110** and **120** also have respective terminals **153** and **154** coupled together and to a positive voltage terminal **156** to provide or receive voltage V**2**. Phase circuits **110** and **120** have respective terminals **157** and **158** coupled together at a negative voltage terminal **159**. The terms "positive voltage rail" and "negative voltage rail" are relative terms meaning that the voltage on a positive supply voltage terminal is more positive than the voltage on a negative supply voltage terminal. The voltage of the negative supply voltage terminal may be earth ground or a voltage other than earth ground.

[0017] Capacitors C**3** and C**4** are coupled in parallel between inputs **151**/**152** and the negative supply voltage terminal. Current sense circuit **130** has terminals **130***a* and **130***b* and is coupled into the negative supply voltage terminal. Capacitor C**1** has a terminal coupled to the positive voltage terminal **156** and a terminal coupled to the negative voltage terminal **159** and to terminal **130***a* of current sense circuit **130**. Capacitor C**2** has a terminal coupled to the

positive voltage terminal **156** and a terminal coupled to terminal **130***b* of current sense circuit **130**. Current sense circuit **130** includes a low resistance resistor R**1** (e.g., **10** milliohms). Due to the low resistance of resistor R**1**, the voltage drop across resistor R**1** is small enough that the connection of terminal **130***b* of current sense circuit **130** and capacitor C**2** is also referred to herein as a negative voltage terminal **160**. Current sense circuit **130** also includes an amplifier **132** which has positive and negative inputs **132***a* and **132***b* coupled to opposing terminals resistor R**1**. In another example, current sense circuit **130** includes a Hall effect sensor

[0018] Phase circuit **110** includes an inductor L**1** and transistors M**1** and M**2**. Phase circuit **120** includes an inductor L**2** and transistors M**3** and M**4**. In this example, transistors M**1**-M**4** are n-channel field effect transistors (NFETs) but some or all of the transistors can be implemented as other types of transistors in other examples. The source of transistor M**1** is coupled to the drain of transistor M**2** at a switching terminal **112**. One terminal of inductor L**1** is coupled to input **151** and another terminal of inductor L**1** is coupled to the switching terminal **112**. The drain of transistor M**1** is coupled to the output **153**, and the source of transistor M**2** is coupled to the negative voltage terminal **159**. The configuration of phase circuit **120** is similar to that of phase circuit **110**. The source of transistor M**3** is coupled to the drain of transistor M**4** at a switching terminal **122**. One terminal of inductor L**2** is coupled to input **152** and another terminal of inductor L**2** is coupled to the switching terminal **122**. The drain of transistor M**3** is coupled to the output **154**, and the source of transistor M**4** is coupled to the negative voltage terminal **159**.

[0019] PWM controller includes logic has outputs **150***a*, **150***b*, **150***c*, and **150***d* and an input **150***e*. Output **150***a* is coupled to the gate of transistor M**1**. Output **150***b* is coupled to the gate of transistor M**3**. Output **150***c* is coupled to the gate of transistor M**2**. Output **150***d* is coupled to the gate of transistor M**4**. In one example, PWM controller **150** includes digital circuit components such as logic gates, flip-flops, registers. In another example, PWM controller **150** includes a programmable logic circuit such as a microcontroller. Current sense circuit has an output **130***c* coupled to the output of amplifier **132**. Output **130***c* is coupled to the input **150***e* of PWM controller **150**.

[0020] As shown in FIG. **1**, current sense circuit **130** is located in the negative voltage terminal of multiphase power converter **100**. Other possible locations for the current sense circuit include, for example, locations adjacent (e.g., coupled to) inductors L**1** and L**2**. For example, the current sense circuit **130** could be coupled between inductor L**1** and switching terminal **112**. However, locating the current sense circuit at that position in the circuit would mean including two current sense circuits-one connected to inductor L**1** and another connected to inductor L**2**—thereby increasing the area of the multiphase power converter (e.g., the area of the PCB on which the components of the power converter are mounted), part count, and cost. Further, due to the relatively high voltages at the switching terminals **112** and **122**, the amplifiers **132** within the respective current sense circuits **130** may need to be isolated amplifiers, or another type of isolated current sensor may be used such as a Hall effect sensor. Locating the current sense circuit **130** at the negative voltage terminal of multiphase power converter **100** between capacitors C**1** and C**2**, as shown in FIG. **1**, advantageously avoids the necessity of having two current sense circuits and avoids the amplifier **132** from being an isolated amplifier.

[0021] FIGS. **2**-**4** represent four different states of multiphase power converter **100**. The difference in the four states are the on and off states of transistors M**1**-M**4** (shown symbolically as switches in FIGS. **2**-**4**). In FIG. **2**, transistors M**2** and M**3** are on (closed) and transistors M**1** and M**4** are off (open). In FIG. **3**, transistors M**2** and M**4** are on and transistors M**1** and M**3** are off. In FIG. **4**, transistors M**1** and M**4** are on and transistors M**2** and M**3** are off. In FIG. **5**, transistors M**1** and M**3** are on and transistors M**2** and M**4** are off. In FIGS. **2**-**4**, the current through inductor L**1** is current I_L**1** and the current through inductor L**2** is current I_L**2**.

[0022] In the states depicted in FIGS. **2** and **4**, the current through resistor R**1** is one or the other of current I_L**1** or I_L**2**. In FIG. **2** with transistors M**2** and M**3** on and transistors M**1** and M**4** off, current I_L**2** flows through inductor L**2**, through transistor M**3** and back through resistor R**1** and through capacitors C**3** and C**4** to inductor L**2**. In this state, current I_L**1** circulates through inductor L**1**, transistor M**2** and capacitors C**3** and C**4**. Accordingly, the current through resistor R**1** is equal to the current I_L**2** of inductor L**2**.

[0023] In FIG. **3**, with transistors M**2** and M**4** on, current I_L**2** circulates through inductor L**2**, transistor M**4**, and capacitor C**3** and C**4**. Similarly, current I_L**1** circulates through inductor L**1**, transistor M**2**, and capacitor C**3** and C**4**. Neither current I_L**1** nor I_L**2** flows through resistor R**1** in this state.

[0024] In FIG. **4** with transistors M**1** and M**4** on and transistors M**2** and M**3** off, current I_L**1** flows through inductor L**1**, through transistor M**1** and back through resistor R**1** and through capacitors C**3** and C**4** to inductor L**1**. In this state, current I_L**2** circulates through inductor L**2**, transistor M**4** and capacitors C**3** and C**4**. Accordingly, the current through resistor R**1** is equal to the current I_L**1** of inductor L**1**.

[0025] In FIG. **5**, with transistors M**1** and M**3** on, current I_L**2** flows through inductor L**2**, transistor M**3** and back through resistor R**1** and capacitors C**3** and C**4**. Similarly, current I_L**1** flows through inductor L**1**, transistor M**1** and back through resistor R**1** and capacitors C**3** and C**4**. Accordingly, the current through resistor R**1** in this state is the sum of current I_L**1** and IL**2**.

[0026] The states corresponding to FIGS. **2** and **4** are the states in which PWM controller **150** should obtain a current sense reading from amplifier **132**. Obtaining a current sense reading when PWM controller **150** is operating transistors M**1**-M**4** in the state corresponding to FIG. **3** is useless because neither inductor's current flows through resistor R**1** in that state. Further, obtaining a current sense reading when PWM controller **150** is operating transistors M**1**-M**4** in the state corresponding to FIG. **5** does not provide an indication of either inductor's individual current.

[0027] FIG. **6** is a timing diagram illustrating example waveforms for current I_L**1** through inductor L**1**, current I_L**2** through inductor L**2** current Ishunt (current through resistor R**1**), carrier PWM **1** (carrier waveform for phase circuit **110**), and carrier PWM **2** (carrier waveform for phase circuit **120**). During each PWM switching cycle for phase circuit **110**, the current I_L**1** through inductor L**1** increases during the state corresponding to FIGS. **2** and **3** and then, following a short time period spent in the state of FIG. **3**, decreases during the state corresponding to FIGS. **4** and **5**. Similarly, during each PWM switching cycle for phase

circuit **120**, the current I_L2 through inductor L2 increases during the state corresponding to FIGS. **3** and **4** and then decreases during the states corresponding to FIGS. **5** and **2**.

[0028] The carrier PWM **1** and carrier PWM **2** signals are generated internally to PWM controller **150**, as described below and shown in FIG. **9**. PWM controller **150** obtains the current sense value from current sense circuit **130** when each carrier PWM **1**, **2** signal reaches its lowest value or is within a threshold of the lowest value. Accordingly, at time points **610**, PWM controller **150** obtains a current sense value from current sense circuit **130**. The current sense value at that point in time corresponds to the state in which current I_L1 is decreasing as indicated by dashed line **611** and current Ishunt (current of resistor R1) is the current I_L1 of inductor L1. At time points **620**, PWM controller **150** obtains a current sense value from current sense circuit **130**. The current sense value at time point **620** corresponds to the state in which current I_L2 is decreasing as indicated by dashed line **621** and current Ishunt is the current I_L2 of inductor L2.

[0029] A purpose of capacitor C1 in FIG. **1** is to reduce the parasitic inductance in the conductors (e.g., copper traces on a circuit board) between the outputs **153**, **154** and terminals **157**, **158** of phase circuits **110** and **120** and the load powered by multiphase power converter **100**. Capacitor C1 may be a ceramic capacitor and located on the circuit board close to the phase circuits **110**, **120**. By reducing the parasitic inductance, capacitor C1 helps to reduce the peak voltage of Vout and reduce the voltage across each transistor during switching. Capacitor C2 may be a thin film capacitor and functions to reduce the ripple current and voltage ripple at the output of multiphase power converter **100**. A downside of having both capacitors C1 and C2 is a resonance that may form between the two capacitors based on the equivalent series inductance of capacitors C1 and C2 and the parasitic inductance of the traces connecting capacitor C1 to capacitor C2. The resonance manifests itself as ringing in the output current each time the transistors change state. Because current sense circuit **130** is positioned between capacitors C1 and C2, current sense circuit **130** also detects the ringing which (a) may make less accurate a determination of the current through either of the phase circuits **110** and **120** and (b) may trigger false positives of overcurrent detection.

[0030] FIG. **7** is a schematic diagram of multiphase power converter **100** similar to that of FIG. **1**. Multiphase power converter **100** in FIG. **7**, however, includes a damping circuit **708**. In one example, damping circuit includes a resistor R2 coupled in series with a capacitor C5. Terminal **708***a* of damping circuit **708** is coupled to the positive voltage terminal **156** and another terminal **708***b* of damping circuit **708** is coupled to the negative voltage terminal **160** and terminal **130***b* of current sense circuit **130**. In one example, the capacitance of capacitor C5 is set approximately equal to the capacitance of capacitor C1, and the resistance of resistor R2 is set approximately equal to:

$$R2 = \sqrt{\frac{L_\sigma}{C1}} \qquad \text{Eq. (1)}$$

where L_σ is the sum of the parasitic impedances of capacitors C1 and C2 and the parasitic inductance of the traces connecting capacitor C1 to C2 Damping circuit attenuates the ringing in the current through resistor R1, which otherwise would be present absent the damping circuit.

[0031] FIG. **8** is a schematic diagram of multiphase power converter **100** in another example. The example of FIG. **8** is similar to that of FIG. **7**. A difference is the location of damping circuit **708**. In FIG. **8**, terminal **708***a* of damping circuit **708** is coupled to positive voltage terminal **156** and terminal **708***b* is coupled to negative voltage terminal **159** and to terminal **130***a* of current sense circuit **130**. The example damping circuit **708** in FIG. **8** also is a series combination of resistor R2 and capacitor C5, whose values can be set as per the description above.

[0032] FIG. **9** is a block diagram of PWM controller **150**, in an example. PWM controller **150** includes counters **902** and **904**, comparators **906**, **908**, **910**, and **912**, deadtime circuits **914** and **916**, OR gate **918**, an analog-to-digital converter (ADC), and logic **922**. Counter **902** has a clock input **902***a*, an offset input **902***b*, and an output **902***c*. Counter **904** has a clock input **904***a*, an offset input **904***b*, and an output **904***c*. A clock signal, CLK, is provided to the clock inputs **902***a* and **904***a* of counters **902** and **904**. The output count values from counters **902** and **904** are Carrier PWM **1** and Carrier PWM **2**, respectively. In one example, counters **902** and **904** are digital counters that count up to a first value and then count down to a second value, back up to the first value and so on. The offset inputs **902***b* and **904***b* receive respective fixed offset values. In one example, the frequency of clock signal CLK is 100 MHz and the frequency of Carrier PWM **1** and Carrier PWM **2** is 10 KHz. Each counter **902** and **904** counts up from 0 to 5000, down from 5000 to 0, and so on. Based on the offset values provided to offset inputs **902***b* and **904**, while counter **902** counts up from 0 to 5000, counter **904** counts down from 5000 to 0.

[0033] The output **902***c* of counter **902** is coupled to an input **906***a* of comparator **906** and to the positive input of comparator **910**. The output **904***c* of counter **904** is coupled to input **908***a* of comparator **908** and to the positive input of comparator **912**. Each negative input of comparators **910** and **912** receives a reference signal ref1 and ref2, respectively. Reference signals ref1 and ref2 are indicative of the duty cycles of the respective phase circuits **110** and **120**. The output **910***a* of comparator **910** is coupled to an input **914***a* of deadtime circuit **914**. Deadtime circuit **914** produces a complementary pair of output signals at its outputs **914***b* and **914***c* to drive respective transistors M1 and M2 while ensuring a suitable deadtime between one transistor (M1, M2) turning off and the other transistor (M2, M1) turning on. Comparator **910** compares the signal Carrier PWM **1** to the reference signal ref1. The signals at outputs **914***b* and **914***c* for phase circuit **110** are provided by deadtime circuit **914** to drivers (not shown) to turn on and off transistors M1 and M2 of phase circuit **110**. The output **912***a* of comparator **912** is coupled to an input **916***a* of deadtime circuit **916**. Deadtime circuit **916** produces a complementary pair of output signals at its outputs **916***b* and **916***c* to drive respective transistors M3 and M4 while ensuring a suitable deadtime between one transistor (M3, M4) turning off and the other transistor (M4, M3) turning on. Comparator **912** compares the signal Carrier PWM **2** to the reference signal ref2. The signals at outputs **916***b* and **916***c* for phase circuit **120** are provided by deadtime circuit **916** to drivers (not shown) to turn on and off transistors M3 and M4 of phase circuit **120**.

[0034] Comparator **906** compares Carrier PWM **1** to a reference value (e.g., 0) provided to its input **906***b* and determines when the Carrier PWM **1** value is equal to the reference value. Similarly, comparator **908** compares Carrier PWM **2** to a reference value (e.g., 0) provided to its input **908***b* and determines when the Carrier PWM **2** value is equal to the reference value. The outputs **906***c* and **908***c* of comparators **906** and **908**, respectively, are provided to inputs of OR gate **918**. ADC **1020** as an analog input **920***a*, a digital output **920***b*, and a control input **920***c*. The signal from the current sense circuit **130** is provided to analog input **920***a* of ADC **920**. OR gate **918** logically ORs the output signals from comparators **906** and **908**. Each comparator **906**, **908** generates its output signal to be logic high when its respective Carrier PWM **1**, **2** reaches the threshold. The output signal from OR gate is provided to the control **920***c* of ADC **920**. When the signal at the control input **920***c* is logic high, the ADC **920** is activated/enabled to convert the analog input signal from current sense circuit **130** to a digital output value provided to logic **922**. Logic **922** may include logic gates, flip-flops, etc. configured to determine whether the current through the phase circuits **110** and **120** are balanced. In one example, if the currents through phase circuits **110** and **120** are not balanced, then the reference signals ref**1** and/or ref**2** can be adjusted within PWM controller **150** to adjust the duty cycle of the transistors of one phase circuit relative to the other to better balance the current.

[0035] FIG. **10** is a flow diagram **1000** illustrating the operation of PWM controller **150**. Operations **1002**, **1004**, and **1006** are performed in parallel with operations **1008**, **1010**, and **1012**. At operation **1002**, counter **902** increments its output value until a peak value is reached. Then, at operation **1004**, counter **902** begins decrementing its output value. At operation **1006**, the output value from counter **902** is compared to a threshold (e.g., 0). If the output value from counter **902** has not reached the threshold, then control loops back to operation **1004**. Otherwise, operation **1014** is performed. Similarly, at operation **1008**, counter **904** increments its output value until a peak value is reached. Then, at operation **1010**, counter **904** begins decrementing its output value. At operation **1012**, the output value from counter **904** is compared to a threshold (e.g., 0). If the output value from counter **904** has not reached the threshold, then control loops back to operation **1010**. Otherwise, operation **1014** is performed. At operation **1014**, a digital value is obtained from ADC **920** by, for example, OR gate **918** generating a signal to control input **920***c* to activate/enable ADC **920** to generate a digital output value based on the analog input signal at input **150***e*.

[0036] In this description, the term "couple" may cover connections, communications, or signal paths that enable a functional relationship consistent with this description. For example, if device A generates a signal to control device B to perform an action: (a) in a first example, device A is coupled to device B by direct connection; or (b) in a second example, device A is coupled to device B through intervening component C if intervening component C does not alter the functional relationship between device A and device B, such that device B is controlled by device A via the control signal generated by device A.

[0037] Also, in this description, the recitation "based on" means "based at least in part on." Therefore, if X is based on Y, then X may be a function of Y and any number of other factors.

[0038] A device that is "configured to" perform a task or function may be configured (e.g., programmed and/or hardwired) at a time of manufacturing by a manufacturer to perform the function and/or may be configurable (or reconfigurable) by a user after manufacturing to perform the function and/or other additional or alternative functions. The configuring may be through firmware and/or software programming of the device, through a construction and/or layout of hardware components and interconnections of the device, or a combination thereof.

[0039] As used herein, the terms "terminal", "node", "interconnection", "pin" and "lead" are used interchangeably. Unless specifically stated to the contrary, these terms are generally used to mean an interconnection between or a terminus of a device element, a circuit element, an integrated circuit, a device or other electronics or semiconductor component.

[0040] A circuit or device that is described herein as including certain components may instead be adapted to be coupled to those components to form the described circuitry or device. For example, a structure described as including one or more semiconductor elements (such as transistors), one or more passive elements (such as resistors, capacitors, and/or inductors), and/or one or more sources (such as voltage and/or current sources) may instead include only the semiconductor elements within a single physical device (e.g., a semiconductor die and/or integrated circuit (IC) package) and may be adapted to be coupled to at least some of the passive elements and/or the sources to form the described structure either at a time of manufacture or after a time of manufacture, for example, by an end-user and/or a third-party.

[0041] While the use of particular transistors is described herein, other transistors (or equivalent devices) may be used instead with little or no change to the remaining circuitry. For example, a field effect transistor ("FET") (such as an n-channel FET (NFET) or a p-channel FET (PFET)), a bipolar junction transistor (BJT—e.g., NPN transistor or PNP transistor), an insulated gate bipolar transistor (IGBT), and/or a junction field effect transistor (JFET) may be used in place of or in conjunction with the devices described herein. The transistors may be depletion mode devices, drain-extended devices, enhancement mode devices, natural transistors or other types of device structure transistors. Furthermore, the devices may be implemented in/over a silicon substrate (Si), a silicon carbide substrate (SiC), a gallium nitride substrate (GaN) or a gallium arsenide substrate (GaAs).

[0042] References may be made in the claims to a transistor's control input and its current terminals. In the context of a FET, the control input is the gate, and the current terminals are the drain and source. In the context of a BJT, the control input is the base, and the current terminals are the collector and emitter.

[0043] References herein to a FET being "ON" or "enabled" means that the conduction channel of the FET is present and drain current may flow through the FET. References herein to a FET being "OFF" or "disabled" means that the conduction channel is not present so drain current

does not flow through the FET. An "OFF" FET, however, may have current flowing through the transistor's body-diode.

[0044] Circuits described herein are reconfigurable to include additional or different components to provide functionality at least partially similar to functionality available prior to the component replacement. Components shown as resistors, unless otherwise stated, are generally representative of any one or more elements coupled in series and/or parallel to provide an amount of impedance represented by the resistor shown. For example, a resistor or capacitor shown and described herein as a single component may instead be multiple resistors or capacitors, respectively, coupled in parallel between the same nodes. For example, a resistor or capacitor shown and described herein as a single component may instead be multiple resistors or capacitors, respectively, coupled in series between the same two nodes as the single resistor or capacitor.

[0045] While certain elements of the described examples are included in an integrated circuit and other elements are external to the integrated circuit, in other example embodiments, additional or fewer features may be incorporated into the integrated circuit. In addition, some or all of the features illustrated as being external to the integrated circuit may be included in the integrated circuit and/or some features illustrated as being internal to the integrated circuit may be incorporated outside of the integrated. As used herein, the term "integrated circuit" means one or more circuits that are: (i) incorporated in/over a semiconductor substrate; (ii) incorporated in a single semiconductor package; (iii) incorporated into the same module; and/or (iv) incorporated in/on the same printed circuit board.

[0046] Uses of the phrase "ground" in the foregoing description include a chassis ground, an Earth ground, a floating ground, a virtual ground, a digital ground, a common ground, and/or any other form of ground connection applicable to, or suitable for, the teachings of this description. In this description, unless otherwise stated, "about," "approximately" or "substantially" preceding a parameter means being within +/−10 percent of that parameter or, if the parameter is zero, a reasonable range of values around zero.

[0047] Modifications are possible in the described examples, and other examples are possible, within the scope of the claims.

What is claimed is:

1. A multiphase power converter, comprising:

a first phase circuit having a first input, a first output, and a first terminal, the first output coupled to a positive voltage terminal, and the first terminal coupled to a first negative voltage terminal;

a second phase circuit having a second input, a second output, and a second terminal, the second input coupled to the first input, the second output coupled to the positive voltage terminal, and the second terminal coupled to the first negative voltage terminal; and

a current sense circuit having first and second current sense terminals, the first current sense terminal coupled to the first negative voltage terminal and the second current sense terminal coupled to a second negative voltage terminal.

2. The multiphase power converter of claim **1**, further comprising:

a first capacitor having first and second capacitor terminals, the first capacitor terminal coupled to the positive voltage terminal, and the second capacitor terminal coupled to the first current sense terminal; and

a second capacitor having third and fourth capacitor terminals, the third capacitor terminal coupled to the positive voltage terminal, and the fourth capacitor terminal coupled to the second current sense terminal.

3. The multiphase power converter of claim **2**, further comprising a damping circuit having first and second damping circuit terminals, the first damping circuit terminal coupled to the positive voltage terminal.

4. The multiphase power converter of claim **3**, wherein the damping circuit includes a resistor coupled in series with a third capacitor.

5. The multiphase power converter of claim **3**, wherein the second damping circuit terminal is coupled to the second current sense terminal.

6. The multiphase power converter of claim **3**, wherein the second damping circuit terminal is coupled to the first current sense terminal.

7. The multiphase power converter of claim **1**, wherein the current sense circuit includes a resistor having a first resistor terminal coupled to the first current sense terminal and a second resistor terminal coupled to the second current sense terminal.

8. The multiphase power converter of claim **1**, further comprising a controller configured to generate a carrier signal, determine that a magnitude of the carrier signal has fallen below a threshold, and convert an analog signal from the current sense circuit to a digital signal.

9. The multiphase power converter of claim **1**, wherein the current sense circuit has an output, the multiphase power converter further comprises a controller including:

an analog-to-digital converter (ADC) having an analog input and a control input, the analog input coupled to the output of the current sense circuit;

a comparator having a first input, a second input, and an output, the first input of the comparator configured to receive a threshold value, and the output of the comparator coupled to the control input of the ADC; and

a counter having an output coupled to the second input of the comparator.

10. A multiphase power converter, comprising:

a first phase circuit having an input and an output;

a second phase circuit having an input coupled to the input of the first phase circuit and having an output coupled to the output of the first phase circuit;

a first capacitor having first and second terminals, the first terminal coupled to the outputs of the first and second phase circuits;

a second capacitor having first and second terminals, the first terminal of the second capacitor coupled to the outputs of the first and second phase circuits; and

a resistor having first and second terminals, the first terminal of the resistor coupled to the second terminal of the first capacitor and the second terminal of the resistor coupled to second terminal of the second capacitor.

11. The multiphase power converter of claim **10**, further comprising a damping circuit having first and second terminals, the first terminal of the damping circuit coupled to the first terminals of the first and second capacitors.

12. The multiphase power converter of claim **11**, wherein the resistor is a first resistor, and wherein the damping circuit includes a second resistor coupled in series with a third capacitor.

13. The multiphase power converter of claim **11**, wherein the second terminal of the damping circuit is coupled to the second terminal of the first capacitor.

14. The multiphase power converter of claim **11**, wherein the second terminal of the damping circuit is coupled to the second terminal of the second capacitor.

15. The multiphase power converter of claim **10**, further comprising:

an amplifier coupled to the resistor and having an output; and

a controller configured to generate a carrier signal, determine that a magnitude of the carrier signal equals or is below a threshold, and convert an analog signal from the output of the amplifier to a digital signal.

16. The multiphase power converter of claim **10**, further comprising an amplifier coupled to the resistor and having an output, the multiphase power converter further comprises a controller including:

an analog-to-digital converter (ADC) having an analog input and a control input, the analog input coupled to the output of the amplifier;

a comparator having a first input, a second input, and an output, the first input of the comparator configured to receive a threshold voltage, and the output of the comparator coupled to the control input of the ADC; and

a counter having an output coupled to the second input of the comparator.

17. A circuit, comprising:

an analog-to-digital converter (ADC) having an analog input and a control input;

a first comparator having first and second inputs and an output, the output coupled to the control input;

a second comparator having third and fourth inputs and an output; and

a first counter having an input and an output, the output coupled to the first and third inputs.

18. The circuit of claim **17**, further comprising:

a third comparator having fifth and sixth inputs and an output, the output of the third comparator coupled to the control input;

a fourth comparator having seventh and eighth inputs and an output; and

a second counter having an input and an output, the output of the second counter coupled to the fifth and sixth inputs.

19. The circuit of claim **18**, wherein the inputs of the first and second counters are configured to receive a clock signal.

20. The circuit of claim **18**, wherein the ADC has a digital output and is configured to generate a digital output signal at the digital output in response to a signal at its control input.

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