United States Patent Application Publication	20250266387
Kind Code	A1
Publication Date	August 21, 2025
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SELF-ALIGNED INTERCONNECT STRUCTURE

Abstract

A semiconductor structure including an interconnect structure disposed over a semiconductor substrate. A lower metal line is disposed at a first height over the semiconductor substrate and extends through a first interlayer dielectric layer. A second interlayer dielectric layer is disposed at a second height over the semiconductor substrate and includes a first dielectric material. An upper metal line is disposed at a third height over the semiconductor substrate. A via is disposed at the second height. The via extends between the lower metal line and the upper metal line. A protective dielectric structure is disposed at the second height. The protective dielectric structure includes a protective dielectric material and is disposed along a first set of opposing sidewalls of the via, the protective dielectric material differing from the first dielectric material.

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Family ID: **1000008578169**

Appl. No.: **19/198764**

Filed: **May 05, 2025**

Related U.S. Application Data

parent US continuation 18359012 20230726 parent-grant-document US 12322723 child US 19198764
parent US continuation 17868946 20220720 parent-grant-document US 11798910 child US 18359012
parent US division 16898670 20200611 parent-grant-document US 11488926 child US 17868946

Publication Classification

Int. Cl.: **H01L23/00** (20060101); **H01L21/768** (20060101); **H01L23/522** (20060101)

U.S. Cl.:

CPC **H01L24/48** (20130101); **H01L21/76802** (20130101); **H01L21/76877** (20130101); H01L21/76808 (20130101); H01L21/76897 (20130101); H01L23/5226 (20130101)

Background/Summary

REFERENCE TO RELATED APPLICATIONS [0001] This Application is a Continuation of U.S. application Ser. No. 18/359,012, filed on Jul. 26, 2023, which is a Continuation of U.S. application Ser. No. 17/868,946, filed on Jul. 20, 2022 (now U.S. Pat. No. 11,798,910, issued on Oct. 24, 2023), which is a Divisional of U.S. application Ser. No. 16/898,670, filed on Jun. 11, 2020 (now U.S. Pat. No. 11,488,926, issued on Nov. 1, 2022). The contents of the above-referenced Patent Applications are hereby incorporated by reference in their entirety.

BACKGROUND

[0002] Modern day integrated chips contain millions of semiconductor devices, such as active semiconductor devices (e.g., transistors) and/or passive semiconductor devices (e.g., resistors, diodes, capacitors). The semiconductor devices are electrically interconnected by way of back-end-of-the-line (BEOL) metal interconnect layers that are formed above the semiconductor devices on an integrated chip. A typical integrated chip comprises a plurality of back-end-of-the-line metal interconnect layers including different sized metal wires vertically coupled together with metal contacts (i.e., vias).

Description

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0004] FIG. **1**A illustrates a top layout view of some embodiments of an integrated chip comprising a self-aligned interconnect structure.

[0005] FIG. **1**B illustrates a cross-sectional view of some embodiments of the integrated chip of FIG. **1**A in a first direction.

[0006] FIG. **1**C illustrates a cross-sectional view of some embodiments of the integrated chip of FIG. **1**A in a second direction.

[0007] FIG. **1**D illustrates an alternative top layout view of some embodiments of an integrated chip comprising a self-aligned interconnect structure.

[0008] FIG. **2** illustrates a three-dimensional view of some embodiments of a portion of the integrated chip of FIG. **1**A.

[0009] FIG. **3** illustrates a cross-sectional view of some embodiments of an integrated chip comprising a self-aligned interconnect structure.

[0010] FIG. **4** illustrates a top layout view of some embodiments of the integrated chip of FIG. **3**.

[0011] FIG. **5**A illustrates a top layout view of some embodiments of an integrated chip comprising

a self-aligned interconnect structure.
[0012] FIG. **5**B illustrates a cross-sectional view of some embodiments of the integrated chip of FIG. **5**A in a first direction.
[0013] FIG. **5**C illustrates a cross-sectional view of some embodiments of the integrated chip of FIG. **5**A in a second direction.
[0014] FIG. **6** illustrates a three-dimensional view of some embodiments of a portion of the integrated chip of FIG. **5**A.
[0015] FIGS. **7**A-**24** illustrate a series of cross-sectional views of some embodiments of a method for forming an integrated chip comprising a self-aligned interconnect structure.
[0016] FIG. **25** illustrates a flow diagram of some embodiments of a method for forming an integrated chip comprising a self-aligned interconnect structure.
DETAILED DESCRIPTION
[0017] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.
[0018] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper” and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.
[0019] Many integrated chips include semiconductor devices disposed on a semiconductor substrate. The semiconductor devices are typically connected to one another by an interconnect structure disposed over the semiconductor substrate. The interconnect structure may include a plurality of lower metal lines laterally spaced apart by a first interlayer dielectric (ILD) layer. A plurality of upper metal lines may be disposed over the lower metal lines and laterally spaced apart by a second ILD layer. Conductive contacts may couple the lower metal lines to the semiconductor devices on the semiconductor substrate, and conductive vias may extend through the second ILD layer to vertically couple to the lower metal lines to the upper metal lines. In this way, the interconnect structure can couple the devices to one another to achieve a predetermined circuit configuration, such as a microprocessor, application specific integrated circuit (ASIC), memory device, image sensor device, and the like.
[0020] A challenge with some interconnect structures arises due to misalignment that occurs during manufacturing. More particularly, to manufacture such an interconnect structure, the lower metal lines are formed, and the second ILD layer is formed over the lower metal lines. Then, a mask is patterned over the second ILD layer, and an etch is carried out with the mask in place to form via openings that extend downwardly through the second ILD layer to upper surfaces of the lower metal lines. Metal is then deposited in these via openings, thereby establishing the vias of the interconnect structure. Ideally, each via would be centered directly over its corresponding lower metal line, such that sidewalls of the via reside entirely over an upper surface of the lower metal line (e.g., sidewalls of the via would not overhang the outer edges of the lower metal line).

However, due to slight misalignment of the mask during processing, in reality the via openings may be laterally shifted slightly from their ideal positions and the actual via openings may have outer edges that extend laterally past (and downward alongside) the outer sidewalls of the lower metal lines. Consequently, when the metal is subsequently formed in the via openings, the metal may also extend laterally beyond (and downward alongside) the sidewalls of the lower metal lines, thereby reducing the effective distance/separation between adjacent lower metal lines. In some scenarios, this metal can form an unexpected conductive “bridge” between two adjacent lower metal lines that would otherwise be isolated from one another, such that this “bridge” leads to an unexpected short circuit that is detrimental (or fatal) to the final chip. In other cases, this metal can simply reduce the distance between the two adjacent lower metal lines, thereby allowing for increased current leakage between the two adjacent lower metal lines, which can lead to reduced performance and/or cause long-term reliability concerns.

[0021] Accordingly, various embodiments of the present disclosure relate to an integrated chip comprising a self-aligned interconnect structure for improving the reliability of the integrated chip and a method for forming the self-aligned interconnect structure. The self-aligned interconnect structure may comprise a plurality of lower metal lines within a first interlayer dielectric (ILD) layer, a plurality of upper metal lines within a second ILD layer, and a plurality of vias disposed between the plurality of lower metal lines and the plurality of upper metal lines. A protective dielectric structure is disposed along sidewalls of the plurality of vias. The protective dielectric structure may further electrically isolate vias and underlying neighboring metal lines to limit current leakage and to limit unwanted short circuits from occurring between the vias and neighboring metal lines. Thus, the self-aligned interconnect structure increases the performance and reliability of the integrated chip.

[0022] FIG. **1**A illustrates a top layout view of some embodiments of an integrated chip **100** including a self-aligned interconnect structure, and FIGS. **1**B-**1**C illustrate cross-sectional views of the integrated chip **100** and the self-aligned interconnect structure **154** consistent with some embodiments of FIG. **1**A. The integrated chip may also be referred to as a semiconductor structure.

[0023] Referring now to FIGS. **1**A, **1**B, and **1**C concurrently, one can see that the self-aligned interconnect structure **154** includes a plurality of metal layers and a plurality of dielectric layers disposed over a semiconductor substrate **102**. More particularly, a first interlayer dielectric (ILD) layer **112** may be disposed over the semiconductor substrate **102** at a first height **164**. A plurality of lower metal lines **114**, such as metal-**1** lines for example, may extend through the first ILD layer **112** at the first height **164**. The plurality of lower metal lines **114** may include a first lower metal line **114***a*, a second lower metal line **114***b*, and a third lower metal line **114***c*, which extend in a first direction in parallel with a first axis **168**. A second ILD layer **118** may be disposed over the semiconductor substrate **102** at a second height **166** that is greater than the first height **164**. A third ILD layer **132** may be disposed over the semiconductor substrate **102** at a third height **176** that is greater than the second height **166**. A plurality of upper metal lines **152**, such as metal-2 lines for example, may extend through the third ILD layer **132** at the third height **176**. The plurality of upper metal lines **152** may include a first upper metal line **152***a* and a second upper metal line **152***b*, which extend in a second direction in parallel with a second axis **170** perpendicular to the first axis **168**. Contacts (e.g., **108**) may extend through dielectric layer **106** to connect the lower metal lines **114** to device structures **104**, and vias (e.g., **150***a*, **150***b*) may electrically connect the lower metal lines **114** to the upper metal lines **152**. For example, a first via **150***a* may connect the first lower metal line **114***a* to the first upper metal line **152***a*, and a second via **150***b* may connect the second lower metal line **114***b* to the second upper metal line **152***b*. The vias (e.g., **150***a*, **150***b*) may be disposed at the second height **166** and may extend through the second ILD layer **118**. A first etch stop layer **110** and second etch stop layer **116** may also be present.

[0024] Some aspects of this disclosure appreciate that if a via, such as first via **150***a* were misaligned, issues could arise. For example, if the first via **150***a* were misaligned to the right in

FIG. **1**B (see **172**), the misaligned via **172** (or "tiger tooth") could cause first metal line **114***a* and/or first upper metal line **152***a* to experience increased current leakage with respect to second lower metal line **114***b* and/or second upper metal line **152***b*, or could potentially even cause an unexpected conductive bridge to form between first lower metal line **114***a* and second lower metal line **114***b* for example. Similarly, if the first via **150***a* were misaligned to the left in FIG. **1**B (see **174**), the misaligned via **174** (or "tiger tooth") could cause first lower metal line **114***a* and/or first upper metal line **152***a* to experience increased current leakage with respect to third lower metal line **114***c*, or could potentially even cause an unexpected conductive bridge to form between first lower metal line **114***a* and third lower metal line **114***c*, for example.

[0025] Therefore, to limit the effects of such misalignment, the self-aligned interconnect structure **154** includes a protective dielectric structure **130**. The protective dielectric structure **130** may be disposed at the second height **166** and may extend through the second ILD layer **118** into a top portion of the first ILD layer **112**. The protective dielectric structure **130** in FIGS. **1**A-**1**C includes a "stripe" layout when viewed from above, and helps limit the via misalignment. The material of the protective dielectric structure **130** may have a lower etch rate than that of the first ILD layer **112** and second ILD layer **118** with respect to the etchant used to form an opening for the first via **150***a* and second via **150***b*. Thus, by having the protective dielectric structure **130** disposed along sidewalls of the first via **150***a* and second via **150***b*, over-etch regions may be eliminated and thus, a potential for current leakage or short circuits to occur between electrically isolated vias and lower metal lines may be decreased. As a result, the overall performance and reliability of the integrated circuit may be increased.

[0026] In the embodiment of FIG. **1**A-**1**C, the protective dielectric structure **130** may be disposed on two opposite sides of the first via **150***a* (see FIG. **1**B) but not on the other two sides of the first via **150***a* (see FIG. **1**C). Thus, a first protective dielectric structure **130***a* and a second protective dielectric structure **130***b* may be symmetric about the first lower metal line **114***a* with respect to the first axis **168**. The protective dielectric structure **130** may have a length **156** in the first direction **168**, and a width **160** in the second direction **170**. The length **156** of the protective dielectric structure **130** may be greater than a width **158** of the upper metal lines **152**, and greater than a width **159** of the vias (e.g., **150***a*, **150***b*). Having the length **156** of the protective dielectric structure **130** be greater than the width of the vias ensures that the outer sidewalls of the vias are completely covered by the protective dielectric structure **130** along the width **159** of the vias. The width **160** of the protective dielectric structure **130** may be greater than a distance **162** between neighboring lower metal lines (e.g., **114***a*, **114***b*). Having the width **160** of the protective dielectric structure **130** being greater than the distance **162** helps to reduce the chances of over-etch regions and/or "tiger tooth" from occurring.

[0027] In some embodiments, the semiconductor substrate **102** comprises silicon, any III-V semiconductor compound, any other suitable material, or any combination of the foregoing. In some embodiments, the device structure **104** comprises a transistor device. In some embodiments, dielectric layer **106** comprises silicon oxide, silicon nitride, a low-k dielectric, or any combination of the foregoing. In some embodiments, the contact **108** comprises copper, cobalt, tungsten, aluminum, titanium, or any combination of the foregoing.

[0028] In some embodiments, the first etch stop layer **110** and the second etch stop layer **116** comprise silicon carbide, silicon oxide, silicon oxycarbide, silicon nitride, silicon carbon nitride, silicon oxynitride, silicon oxycarbide nitride, aluminum oxynitride, aluminum oxide, any other suitable material, or any combination of the foregoing. The first etch stop layer **110** and the second etch stop layer **116** may have a thickness of about 10 to 1000 angstroms.

[0029] In some embodiments, any of the first ILD layer **112**, the second ILD layer **118**, and the third ILD layer **132** comprise a first dielectric material. The first dielectric material may comprise silicon carbide, silicon oxide, silicon oxycarbide, silicon nitride, silicon carbon nitride, silicon oxynitride, silicon oxycarbide nitride, any other suitable dielectric, a low-k dielectric, or any combination of the foregoing. The first ILD layer **112**, the second ILD layer **118**, and the third ILD layer **132** may each have a thickness of about 30 to 800 angstroms.

[0030] In some embodiments, the lower metal lines **114** comprise a first metal and the upper metal lines **152** comprise a second metal. The first metal and the second metal may each comprise tantalum, tantalum nitride, titanium nitride, copper, aluminum, cobalt, ruthenium, molybdenum, iridium, tungsten, or any combination of the foregoing. The lower metal lines **114** and the upper metal lines **152** may have a thickness of about 10 to 1000 angstroms.

[0031] In some embodiments, the protective dielectric structure **130** comprises a protective dielectric material. The protective dielectric material may comprise hafnium oxide, lithium niobium oxide, lithium nickel oxide, magnesium oxide, manganese oxide, molybdenum oxide, niobium oxide, nickel oxide, silicon oxide, silicon oxycarbide, silicon oxycarbide nitride, silicon carbide, tin oxide, tin silicon oxide, strontium oxide, tantalum pentoxide, tantalum oxynitride, tungsten oxide, zinc oxide, zirconium oxide, some other metal oxide, or any combination of the foregoing. The protective dielectric structure **130** may have a thickness of about 10 to 1000 angstroms.

[0032] In some embodiments, the vias (e.g., **150***a*, **150***b*) comprise tantalum, tantalum nitride, titanium nitride, copper, aluminum, cobalt, ruthenium, molybdenum, iridium, tungsten, or any combination of the foregoing. The via **150** may have a thickness of about 10 to 1000 angstroms.

[0033] It will be appreciated that although the top view of FIG. **1**A shows the protective dielectric structure as being symmetrical on opposite sides of each via, other embodiments are also possible. For instance, in FIG. **1**A, the protective dielectric structures disposed between neighboring lower metal lines (which are spaced apart at a regularly repeating pitch and are generally electrically isolated from one another) are particularly beneficial because they limit unexpected conductive bridges and current leakage that could otherwise occur because of via misalignment. Thus, in FIG. **1**A, protective dielectric structures **130***a*, **130***b*, **130***d*, **130***e*, **130***f* are particularly beneficial in this regard. In contrast, because protective dielectric structures **130***c*, **130***g*, **130***h*, **130***i*, and **130***j* in FIG. **1**A do not separate electrically isolated nearest neighboring lower metal lines from one another, these dielectric structures can be omitted in other embodiments, such as shown in FIG. **1**D. Thus, in FIG. **1**D, the protective dielectric structure can be asymmetric on opposite sides of a via (see e.g., **180**), and/or can be present only around some vias (see e.g., **180**, **182**) while not being present around other vias (see e.g., **184**).

[0034] FIG. **2** illustrates a three-dimensional view of a portion of the self-aligned interconnect structure, as indicated by the dashed rectangle in FIG. **1**A. A first lower metal line **114***a*, a second lower metal line **114***b*, and a third lower metal line **114***c* extend through the first ILD layer **112** in the first direction **168**. A first upper metal line **152***a*, a second upper metal line **152***b* extend in the second direction **170** over the lower metal lines. A first via **150***a* connects the first lower metal line **114***a* to the first upper metal line **152***a*, and a second via **150***b* connects the second lower metal line **114***b* to the second upper metal line **152***b*.

[0035] The protective dielectric structure **130** may be disposed on two opposing sides of the vias, such that a sidewall of the first protective dielectric structure **130***a* neighbors a first outer sidewall of the first via **150***a* and a sidewall of the second protective dielectric structure **130***b* neighbors a second outer sidewall of the first via **150***a* opposite the first outer sidewall. In some embodiments, the protective dielectric structure **130** extends through the second ILD layer **118** and through the second etch stop layer **116** into the first ILD layer **112**. The protective dielectric structure **130** may laterally separate the first lower metal line **114***a* from the second lower metal line **114***b* at a top of the first lower metal line **114***a* and a top of the second lower metal line **114***b*. A lowermost surface of the protective dielectric structure **130** may be disposed below a lowermost surface of the first via **150***a* and/or second via **150***b* and below and uppermost surface of the plurality of lower metal lines **114**. The protective dielectric structure **130** may electrically isolate the first via **150***a* from the second lower metal line **114***b*.

[0036] FIG. **3** illustrates a cross-sectional view of some embodiments of an integrated chip **300** comprising a self-aligned interconnect structure. The cross-sectional view of FIG. **3** may be taken across the line C-C′ in FIG. **4**. The second protective dielectric structure **130***b* may comprise a different width than the first protective dielectric structure **130***a* and the third protective dielectric structure **130***c*. For example, sidewalls of the second protective dielectric structure **130***b* that neighbor the first via **150***a* and the second via **150***b* may be disposed over the underlying metal lines (e.g., the second lower metal line **114***b* and the third lower metal line **114***c*) that underly the first via **150***a* and the second via **150***b*. In addition, inner sidewalls of the first protective dielectric structure **130***a* and the third protective dielectric structure **130***c* that neighbor the first via **150***a* and the second via **150***b* may be disposed over neighboring metal lines (e.g., the second lower metal line **114***b* and the third lower metal line **114***c*, respectively) while outer sidewalls of the first protective dielectric structure **130***a* and the third protective dielectric structure **130***c* that do not neighbor the first via **150***a* or the second via **150***b* may not be disposed over neighboring metal lines of the plurality of lower metal lines (e.g., may not be disposed over the first lower metal line **114***a* and the fourth lower metal line **114***d*). Such a configuration results in the first protective dielectric structure **130***a*, the second protective dielectric structure **130***b*, and the third protective dielectric structure **130***c* comprising different widths.

[0037] By disposing the protective dielectric structure **130** over the tops of the lower metal lines (e.g., **114***b*, **114***c*) that are connected to vias (e.g., **150***a*, **150***b*) and isolated from neighboring lower metal lines (e.g., **114***a*, **114***d*), a potential for a gap to exist between the protective dielectric structure and the underlying metal line connected to a via is eliminated. As a result, the potential for over-etching into the first ILD layer **112** when forming via openings is decreased. In turn, the potential for unwanted leakage or shorts to occur between electrically isolated vias and metal lines of the plurality of lower metal lines is reduced and thus, the reliability of the integrated chip **300** is increased.

[0038] FIG. **4** illustrates a top layout view of some embodiments of the integrated chip **300** of FIG. **3**. The second protective dielectric structure **130***b* neighbors the first via **150***a* and the second via **150***b* on both sides while the first protective dielectric structure **130***a* and the third protective dielectric structure **130***c* only neighbor the vias (e.g., **150***a*, **150***b*) on one side. Sidewalls of the first protective dielectric structure **130***a*, the second protective dielectric structure **130***b*, and the third protective dielectric structure **130***c* that neighbor the first via **150***a* or the second via **150***b* (e.g., inner sidewall of the first protective dielectric structure **130***a*, inner sidewall of the third protective dielectric structure **130***c*, and sidewalls of the second protective dielectric structure **130***b*) are formed over a top of the underlying lower metal lines (e.g., **114***b*, **114***c*). Sidewalls of the first protective dielectric structure **130***a*, the second protective dielectric structure **130***b*, and the third protective dielectric structure **130***c* that do not neighbor the first via **150***a* or the second via **150***b* (e.g., outer sidewalls of the first protective dielectric structure **130***a* and the third protective dielectric structure **130***c*) are formed over a top of the first ILD layer **112** and spaced apart from neighboring lower metal lines (e.g., **114***a*, **114***d*). As a result, a first width **160***b* of the inner portion of the protective dielectric structure **130** (e.g., **130***b*) is greater than a second width **160***c* of the outer portions of the protective dielectric structure **130** (e.g., **130***a*, **130***c*). The first width **160***b* is greater than a width **162***b* between the second lower metal line **114***b* and the third lower metal line **114***c*, but the second width **160***c* is not greater than a width **162***c* between the first lower metal line **114***a* and the second lower metal line **114***b* nor is it greater than a width **162***c* between the third lower metal line **114***c* and the fourth lower metal line **114***d*.

[0039] FIG. **5**A-5C and FIG. **6** illustrate another embodiment of an integrated chip **500** comprising a protective dielectric structure **130** that includes a “ring” layout when viewed from above that helps limit via misalignment. Thus, rather than the protective dielectric structure **130** manifesting as “stripes” as depicted in FIGS. **1**A-**1**D, in FIGS. **5**A-**5**C and FIG. **6**, the protective dielectric structure **130** is a “ring” of dielectric material that laterally surrounds the via **150** on all sides. Thus, the protective dielectric structure **130** may be disposed along a first set of opposing sidewalls of the first via **150***a* that extend in parallel with the first axis **168** and along a second set of opposing sidewalls of the first via **150***a* that extend in parallel with the second axis **170** (i.e., perpendicular to the first axis **168**).

[0040] FIGS. **7**A-**24** illustrate cross-sectional views **700**-**2400** of some embodiments of a method of forming an integrated chip comprising a self-aligned interconnect structure **154**. Although FIGS. **7**A-**24** are described in relation to a method, it will be appreciated that the structures disclosed in FIGS. **7**A-**24** are not limited to such a method, but instead may stand alone as structures independent of the method.

[0041] As shown in cross-sectional view **700** of FIG. **7**A, a first etch stop layer **110** is formed over a semiconductor substrate **102**. A first ILD layer **112** is formed over the first etch stop layer **110**. The first etch stop layer **110** and the first ILD layer **112** may each be formed by physical vapor deposition (PVD), chemical vapor deposition (CVD), atomic layer deposition (ALD), or a spin on process and may be formed at a temperature of about 150 to 500 degrees Celsius.

[0042] As shown in cross-sectional view **750** of FIG. **7**B, a first anti-reflective coating (ARC) layer **115** is formed over the first ILD layer **112**, a second ARC layer **117** is formed over the first ARC layer **115**, and a first photoresist mask **119** is formed over the second ARC layer **117**. The first ARC layer **115**, the second ARC layer **117**, and the first photoresist mask **119** may be formed by CVD or a spin on process. The first ARC layer **115** may comprise a different material than the second ARC layer **117**. Any of the first ARC layer **115** and the second ARC layer **117** may comprise silicon oxide, silicon nitride, silicon carbide, silicon oxynitride, aluminum oxide, titanium oxide, tantalum oxide, magnesium fluoride, lanthanum fluoride, aluminum fluoride, some other anti-reflective material, or any combination of the foregoing. The first photoresist mask **119** may be patterned by a photolithographic process. In some embodiments, a different number of ARC layers may be used.

[0043] As shown in cross-sectional view **800** of FIG. **8**A, the first ARC layer **115** and the second ARC layer **117** are etched with the first photoresist mask **119** in place. The first ILD layer **112** and the first etch stop layer **110** are also etched to form a plurality of first trenches **113** in the first ILD layer **112** that are laterally spaced apart from each other by the first ILD layer **112**.

[0044] The etches illustrated in FIG. **8**A may comprise inductively coupled plasma (ICP) etching, capacitively couple plasma (CCP) etching, or remote plasma etching and may utilize methane, fluoromethane, difluoromethane, fluoroform, octafluorocyclobutane, hexafluoro-1,3-butadiene, tetrafluoromethane, hydrogen, hydrogen bromide, carbon monoxide, carbon dioxide, oxygen, Boron trichloride, chlorine, nitrogen, helium, neon, argon, any other suitable etchant, or any combination of the foregoing. The etches may alternatively or additionally comprise a wet etching process that may utilize hydrofluoric acid, nitric acid, acetic acid, hydrochloric acid, phosphoric acid, citric acid, or any combination of the foregoing. The etches may be performed in an atmosphere with a pressure of 0.2 to 120 millitorrs and a temperature of 0 to 100 degrees Celsius. A power utilized during the etches may be about 50 to 3000 watts and a bias voltage applied during the etches may be about 0 to 1200 volts.

[0045] As shown in cross-sectional view **850** of FIG. **8**B, the first ARC layer **115**, the second ARC layer **117**, and the first photoresist mask **119** are removed. The removal may comprise one or more etches such as, for example, an ICP etching, CCP etching, remote plasma etching, isotropic chemical etching, or a wet etching process that may utilize hydrofluoric acid, nitric acid, acetic acid, hydrochloric acid, phosphoric acid, citric acid, or any combination of the foregoing.

[0046] As shown in cross-sectional view **900** of FIG. **9**A, a first metal **121** is deposited in the plurality of first trenches **113** to form a plurality of lower metal lines **114** in the plurality of first trenches **113** and along sidewalls of the first ILD layer **112**. Metal lines of the plurality of lower metal lines **114** are laterally spaced apart from one another by the first ILD layer **112**. The first metal **121** may be deposited by sputtering, electroplating, or another suitable metal deposition technique and, deposition may occur at a temperature of about 150 to 500 degrees Celsius.

[0047] As shown in cross-sectional view **950** of FIG. **9**B, a chemical mechanical polish (CMP) is performed on the first metal **121** to remove the first metal **121** from a top of the first ILD layer **112**.

[0048] As shown in cross-sectional view **1000** of FIG. **10**, a second etch stop layer **116** is formed over the first ILD layer **112**. A second ILD layer **118** is formed over the second etch stop layer **116**. The second etch stop layer **116** and the second ILD layer **118** may be formed by PVD, CVD, ALD, or a spin on process and may be formed at a temperature of about 150 to 500 degrees Celsius.

[0049] As shown in cross-sectional view **1100** of FIG. **11**, a third ARC layer **120** is formed over the second ILD layer **118**. A fourth ARC layer **122** is formed over the third ARC layer **120**. In addition, a second photoresist mask **124** is formed over the fourth ARC layer **122**. The third ARC layer **120**, the fourth ARC layer **122**, and the second photoresist mask **124** may be formed by CVD or a spin on process. The second photoresist mask **124** may comprise openings aligned over portions of the first ILD layer **112** that are disposed between metal lines of the plurality of lower metal lines **114**. The second photoresist mask **124** may be patterned by a photolithographic process. The third ARC layer **120** may comprise a different material than the fourth ARC layer **122**. Any of the third ARC layer **120** and the fourth ARC layer **122** may comprise silicon oxide, silicon nitride, silicon carbide, silicon oxynitride, aluminum oxide, titanium oxide, tantalum oxide, magnesium fluoride, lanthanum fluoride, aluminum fluoride, some other anti-reflective material, or any combination of the foregoing. In some embodiments, a different number of ARC layers may be used.

[0050] As shown in cross-sectional view **1200** of FIG. **12**, the third ARC layer **120** and the fourth ARC layer **122** are etched with the second photoresist mask **124** in place. The second ILD layer **118**, the second etch stop layer **116**, and the first ILD layer **112** are also etched to form a plurality of first openings **126** (i.e., a plurality of first recesses) in the second ILD layer **118**, over and in the first ILD layer **112**, and between metal lines of the plurality of lower metal lines **114**. Openings of the plurality of first openings **126** may extend from over one metal line of the plurality of lower metal lines **114** to over a neighboring metal line of the plurality of lower metal lines **114**.

[0051] The etches illustrated in FIG. **12** may comprise ICP etching, CCP etching, or remote plasma etching and may utilize methane, fluoromethane, difluoromethane, fluoroform, octafluorocyclobutane, hexafluoro-1,3-butadiene, tetrafluoromethane, hydrogen, hydrogen bromide, carbon monoxide, carbon dioxide, oxygen, Boron trichloride, chlorine, nitrogen, helium, neon, argon, any other suitable etchant, or any combination of the foregoing. The etches may alternatively or additionally comprise a wet etching process that may utilize hydrofluoric acid, nitric acid, acetic acid, hydrochloric acid, phosphoric acid, citric acid, or any combination of the foregoing. The etches may be performed in an atmosphere with a pressure of 0.2 to 120 millitorrs and a temperature of 0 to 100 degrees Celsius. A power utilized during the etches may be about 50 to 3000 watts and a bias voltage applied during the etches may be about 0 to 1200 volts.

[0052] As shown in cross-sectional view **1300** of FIG. **13**, the third ARC layer **120**, the fourth ARC layer **122**, and the second photoresist mask **124** are removed. The removal may comprise one or more etches such as, for example, an ICP etching, CCP etching, remote plasma etching, isotropic chemical etching, or a wet etching process that may utilize hydrofluoric acid, nitric acid, acetic acid, hydrochloric acid, phosphoric acid, citric acid, or any combination of the foregoing.

[0053] As shown in cross-sectional view **1400** of FIG. **14**, a protective dielectric material **128** is deposited over the second ILD layer **118** and in the plurality of first openings **126** to form a protective dielectric structure **130** in the plurality of first openings **126**. The protective dielectric material **128** may be formed by PVD, CVD, ALD, or a spin on process and may be formed at a temperature of 150 to 400 degrees Celsius.

[0054] As shown in cross-sectional view **1500** of FIG. **15**, a CMP is performed on the protective dielectric material **128** to remove the protective dielectric material from a top of the second ILD layer **118**. As a result, the protective dielectric structure **130** that is disposed in the plurality of first openings **126** comprises top surfaces even with the top of the second ILD layer **118**.

[0055] As shown in cross-sectional view **1600** of FIG. **16**, a third ILD layer **132** is formed over the second ILD layer **118** and over the protective dielectric structure **130**. The third ILD layer **132** may be formed by PVD, CVD, ALD, or a spin on process and may be formed at a temperature of 150 to 400 degrees Celsius.

[0056] As shown in cross-sectional view **1700** of FIG. **17**, a fifth ARC layer **134** is formed over the third ILD layer **132**. A sixth ARC layer **136** is formed over the fifth ARC layer **134**. In addition, a third photoresist mask **138** is formed over the sixth ARC layer **136**. The fifth ARC layer **134**, the sixth ARC layer **136**, and the third photoresist mask **138** may be formed by CVD or a spin on process. The third photoresist mask **138** may comprise an opening aligned over the protective dielectric structure **130**. The third photoresist mask **138** may be patterned by a photolithographic process. The fifth ARC layer **134** may comprise a different material than the sixth ARC layer **136**. Any of the fifth ARC layer **134** and the sixth ARC layer **136** may comprise silicon oxide, silicon nitride, silicon carbide, silicon oxynitride, aluminum oxide, titanium oxide, tantalum oxide, magnesium fluoride, lanthanum fluoride, aluminum fluoride, some other anti-reflective material, or any combination of the foregoing. In some embodiments, a different number of ARC layers may be used.

[0057] As shown in cross-sectional view **1800** of FIG. **18**, the fifth ARC layer **134** and the sixth ARC layer **136** are etched with the third photoresist mask **138** in place. The third ILD layer **132**, is also etched to form a second trench **140** in the third ILD layer **132** and over the protective dielectric structure **130**. The second trench **140** may have a width of about 5 to 3000 nanometers. Sidewalls of the second trench **140** may be angled at 50 to 95 degrees, as measured from horizontal.

[0058] The etches illustrated in FIG. **18** may comprise reactive ion etching such as, for example, ICP etching or CCP etching and may utilize methane, fluoromethane, difluoromethane, fluoroform, octafluorocyclobutane, hexafluoro-1,3-butadiene, tetrafluoromethane, hydrogen, hydrogen bromide, carbon monoxide, carbon dioxide, oxygen, Boron trichloride, chlorine, nitrogen, helium, neon, argon, any other suitable etchant, or any combination of the foregoing. The etches may alternatively or additionally comprise a wet etching process that may utilize hydrofluoric acid, nitric acid, acetic acid, hydrochloric acid, phosphoric acid, citric acid, or any combination of the foregoing. The etches may be performed in an atmosphere with a pressure of 0.2 to 120 millitorrs and a temperature of 0 to 100 degrees Celsius. A power utilized during the etches may be about 50 to 3000 watts and a bias voltage applied during the etches may be about 0 to 1200 volts.

[0059] As shown in cross-sectional view **1900** of FIG. **19**, the fifth ARC layer **134**, the sixth ARC layer **136**, and the third photoresist mask **138** are removed. The removal may comprise one or more etches such as, for example, an ICP etching, CCP etching, remote plasma etching, isotropic chemical etching, or a wet etching process that may utilize hydrofluoric acid, nitric acid, acetic acid, hydrochloric acid, phosphoric acid, citric acid, or any combination of the foregoing.

[0060] As shown in cross-sectional view **2000** of FIG. **20**, a seventh ARC layer **142** and an eighth ARC layer **144** are formed over the third ILD layer **132**, in the second trench **140**, and over the protective dielectric structure **130**. In addition, a fourth photoresist mask **146** is formed over the eighth ARC layer **144**. The seventh ARC layer **142**, the eighth ARC layer **144**, and the fourth photoresist mask **146** may be formed by CVD or a spin on process. The fourth photoresist mask **146** may comprise openings aligned over portions of the second ILD layer **118** that are disposed between portions of the protective dielectric structure **130**. The fourth photoresist mask **146** may be patterned by a photolithographic process. The seventh ARC layer **142** may comprise a different material than the eighth ARC layer **144**. Any of the seventh ARC layer **142** and the eighth ARC layer **144** may comprise silicon oxide, silicon nitride, silicon carbide, silicon oxynitride, aluminum oxide, titanium oxide, tantalum oxide, magnesium fluoride, lanthanum fluoride, aluminum fluoride, some other anti-reflective material, or any combination of the foregoing. In some embodiments, a different number of ARC layers may be used.

[0061] As shown in cross-sectional view **2100** of FIG. **21**, the seventh ARC layer **142** and the eighth ARC layer **144** are etched with the fourth photoresist mask **146** in place. In addition, the

portions of the second ILD layer **118** that are disposed between the portions of the protective dielectric structure **130** are etched to form a plurality of via openings **148** (i.e., a plurality of second recesses) in the second ILD layer **118** between the portions of the protective dielectric structure **130** and over metal lines of the plurality of lower metal lines **114**. Via openings of the plurality of via openings **148** may have a width of about 5 to 300 nanometers. Sidewalls of via openings of the plurality of via openings **148** may be angled at 40 to 90 degrees, as measured from horizontal.
[0062] The etches illustrated in FIG. **21** may comprise ICP etching, CCP etching, or remote plasma etching and may utilize methane, fluoromethane, difluoromethane, fluoroform, octafluorocyclobutane, hexafluoro-1,3-butadiene, tetrafluoromethane, hydrogen, hydrogen bromide, carbon monoxide, carbon dioxide, oxygen, Boron trichloride, chlorine, nitrogen, helium, neon, argon, any other suitable etchant, or any combination of the foregoing. The etches may alternatively or additionally comprise a wet etching process that may utilize hydrofluoric acid, nitric acid, acetic acid, hydrochloric acid, phosphoric acid, citric acid, or any combination of the foregoing. The etches may be performed in an atmosphere with a pressure of 0.2 to 120 millitorrs and a temperature of 0 to 100 degrees Celsius. A power utilized during the etches may be about 50 to 3000 watts and a bias voltage applied during the etches may be about 0 to 1200 volts.
[0063] In some embodiments, due to a misalignment in the fourth photoresist mask **146**, the etch may not remove all of the second ILD layer **118** and the second etch stop layer **116** that exists between the portions of the protective dielectric structure **130**.
[0064] It will be appreciated that the second ILD layer **118** and the second etch stop layer **116** have higher etch rates than the protective dielectric structure **130** during the etch that forms the plurality of via openings **148**. Thus, even if a misalignment of the fourth photoresist mask **146** occurs, the via openings **148** will not extend laterally past the sidewalls of the underlying metal lines because the protective dielectric structure **130** extends over the sidewalls of the underlying metal lines and the low etch rate of the protective dielectric structure **130** allows it to withstand the etch without much of the protective dielectric structure **130** being removed. As a result, over-etching of the second ILD layer **118** into the first ILD layer **112** when forming the via openings **148** may be prevented, thereby preventing a via **150** from being misaligned. By preventing the via **150** from being misaligned, undesirable via formations (e.g., “tiger tooth's”) may be prevented. In turn, a potential for undesirable leakage currents or short circuits to occur between electrically isolated metal lines of the plurality of lower metal lines **114** may be reduced, thereby increasing the performance and reliability of the integrated chip.
[0065] If, for example, misalignment of the fourth photoresist mask **146** were to occur without the protective dielectric structure **130** in place, the etch that forms the via openings **148** may extend laterally beyond sidewalls of the underlying lower metal lines and vertically into the first ILD layer **112**, thereby resulting in misaligned vias (e.g., **174**, **172** of FIG. **1**B) that may undesirably short electrically isolated lower metal lines. Thus, the protective dielectric structure **130** is implemented in the integrated chip to prevent such undesirable conditions from occurring, thereby increasing the performance and reliability of the integrated chip.
[0066] As shown in cross-sectional view **2200** of FIG. **22**, the seventh ARC layer **142** and the eighth ARC layer **144** are removed. The removal may comprise one or more etches such as, for example, an ICP etching, CCP etching, remote plasma etching, isotropic chemical etching, or a wet etching process that may utilize hydrofluoric acid, nitric acid, acetic acid, hydrochloric acid, phosphoric acid, citric acid, or any combination of the foregoing.
[0067] As shown in cross-sectional view **2300** of FIG. **23**, a second metal **151** is deposited in the plurality of via openings **148** and in the second trench **140** to form a plurality of vias **150** and an upper metal line **152**, respectively. The second metal may be formed by sputtering, electroplating, or another suitable metal deposition technique and, deposition may occur at a temperature of 150 to 400 degrees Celsius.
[0068] In some embodiments, the plurality of vias are in contact with the protective dielectric

structure **130** along one sidewall. In other embodiments, the plurality of vias may be in contact with the protective dielectric structure **130** along two sidewalls or may not be in contact with the protective dielectric structure **130**, depending on whether a portion of the second ILD layer **118** remains in the plurality of via openings **148** after forming the plurality of via openings **148** by etching. Sidewalls of the plurality of vias **150** may be separated from the second ILD layer by the protective dielectric structure **130** after the plurality of vias **150** are formed.
[0069] As shown in cross-sectional view **2400** of FIG. **24**, a CMP is performed on the upper metal line **152** to bring a top of the upper metal line **152** even with a top of the third ILD layer **132**.
[0070] Again, by forming the protective dielectric structure **130**—which has a lower etch rate than the second ILD layer **118** during the via opening **148** etch—around vias **150**, between vias **150**, and between metal lines of the plurality of lower metal lines **114**, the forming of misaligned vias (e.g., **174**, **172** of FIG. **1**B) may be prevented. As a result, a potential for undesirable leakage currents or short circuits to occur between electrically isolated vias and lower metal lines may be decreased. In turn, the overall reliability of the integrated circuit may be increased.
[0071] FIG. **25** illustrates a flow diagram of some embodiments of a method **2500** for forming an integrated chip comprising a self-aligned interconnect structure.
[0072] While method **2500** is illustrated and described below as a series of acts or events, it will be appreciated that the illustrated ordering of such acts or events are not to be interpreted in a limiting sense. For example, some acts may occur in different orders and/or concurrently with other acts or events apart from those illustrated and/or described herein. In addition, not all illustrated acts may be required to implement one or more aspects or embodiments of the description herein. Further, one or more of the acts depicted herein may be carried out in one or more separate acts and/or phases.
[0073] At **2502**, a first metal (e.g., **121**) is deposited to form a first metal layer (e.g., **114**) in a first interlayer dielectric layer (e.g., **112**). See, for example, FIG. **9**A.
[0074] At **2504**, a second interlayer dielectric layer (e.g., **118**) is formed over the first metal layer (e.g., **114**). See, for example, FIG. **10**.
[0075] At **2506**, a first etch is performed into the second interlayer dielectric layer (e.g., **118**) to form a first recess and a second recess (e.g., **126**) in the second interlayer dielectric layer. See, for example, FIG. **12**.
[0076] At **2508**, a first protective dielectric structure (e.g., **130**) is formed in the first recesses (e.g., **126**) and a second protective dielectric structure (e.g., **130**) is formed in the second recess (e.g., **126**). See, for example, FIGS. **14** and **15**.
[0077] At **2510**, a third interlayer dielectric layer (e.g., **132**) is formed over the first protective dielectric structure and over the second protective dielectric structure (e.g., **130**). See, for example, FIG. **16**.
[0078] At **2512**, a second etch is performed into the third interlayer dielectric layer (e.g., **132**) to form a first trench (e.g., **140**) in the third interlayer dielectric layer. See, for example, FIG. **18**.
[0079] At **2514**, a third etch is performed into the second interlayer dielectric layer (e.g., **118**) to form a third recess (e.g., **148**) in the second interlayer dielectric layer that extends between the first protective dielectric structure and the second protective dielectric structure (e.g., **130**). See, for example, FIG. **21**.
[0080] At **2516**, a second metal (e.g., **151**) is deposited in the third recess and in the first trench to form a first via (e.g., **150**) and a second metal layer (e.g., **152**), respectively. See, for example, FIG. **23**.
[0081] In short, various embodiments of the present disclosure relate to an integrated chip comprising a self-aligned interconnect structure for improving the reliability of the integrated chip and a method for forming the self-aligned interconnect structure.
[0082] Accordingly, in some embodiments, the present disclosure relates to a semiconductor structure including an interconnect structure disposed over a semiconductor substrate. The

interconnect structure includes a first interlayer dielectric layer disposed at a first height over the semiconductor substrate. A lower metal line is disposed at the first height over the semiconductor substrate and extending laterally along a first axis through the first interlayer dielectric layer. A second interlayer dielectric layer is disposed at a second height over the semiconductor substrate, the second interlayer dielectric layer comprising a first dielectric material and the second height being greater than the first height. A third interlayer dielectric layer is disposed at a third height over the semiconductor substrate, the third height being greater than the second height. An upper metal line is disposed at the third height over the semiconductor substrate, the upper metal line extending laterally through the third interlayer dielectric layer along a second axis perpendicular to the first axis. A via is disposed at the second height. The via extends between an upper surface of the lower metal line and a lower surface of the upper metal line to electrically couple the lower metal line to the upper metal line. In addition, a protective dielectric structure is disposed at the second height. The protective dielectric structure comprises a protective dielectric material and is disposed along a first set of opposing sidewalls of the via, the protective dielectric material differing from the first dielectric material and the first set of sidewalls being in parallel with the first axis.

[0083] In other embodiments, the present disclosure relates to a semiconductor structure including an interconnect structure disposed over a semiconductor substrate. The interconnect structure includes a first interlayer dielectric layer that is disposed at a first height over the semiconductor substrate. A first lower metal line and a second lower metal line are disposed at the first height over the semiconductor substrate and extending laterally through the first interlayer dielectric layer, the first lower metal line extending in parallel with the second lower metal line in a first direction and spaced apart from the second lower metal line by a first distance measured laterally through the first interlayer dielectric layer. A second interlayer dielectric layer is disposed at a second height over the semiconductor substrate, the second interlayer dielectric layer comprising a first dielectric material and the second height being greater than the first height. A third interlayer dielectric layer is disposed at a third height over the semiconductor substrate, the third height being greater than the second height. An upper metal line is disposed at the third height over the semiconductor substrate, the second metal line extending laterally through the third interlayer dielectric layer in a second direction and crossing over at least one of the first lower metal line and the second lower metal line, the second direction perpendicular to the first direction. A via extends from a lower surface of the upper metal line to an upper surface of the first lower metal line. Finally, a first protective dielectric structure comprising a protective dielectric material is spaced laterally between uppermost portions of nearest neighboring sidewalls of the first lower metal line and the second lower metal line and extending upwardly along a first sidewall of the via, wherein the protective dielectric material differs from the first dielectric material.

[0084] In yet other embodiments, the present disclosure relates to a method for forming a semiconductor structure. The method includes depositing a first metal to form a first metal layer in a first interlayer dielectric layer. A second interlayer dielectric layer comprising a first dielectric material is formed over the first metal layer. A first recess and a second recess are formed in the second interlayer dielectric layer. The first recess and the second recess extend through the second interlayer dielectric layer into the first interlayer dielectric layer and extend below an upper surface of the first metal layer. A first protective dielectric structure and a second protective dielectric structure are formed in the first recess and the second recess, respectively, wherein the first protective dielectric structure and the second protective dielectric structure comprise a protective dielectric material different from the first dielectric material. A third interlayer dielectric layer is formed over the first protective dielectric structure and the second protective dielectric structure. A first trench is formed in the third interlayer dielectric layer. The first trench extends through the third interlayer dielectric layer to a top of the first protective dielectric structure and a top of the second protective dielectric structure. A third recess is formed in the second interlayer dielectric

layer. The third recess extends through the second interlayer dielectric layer to the first metal layer, wherein the third recess is disposed between the first protective dielectric structure and the second protective dielectric structure. Finally, a second metal is deposited in the third recess and in the first trench to form a first via and a second metal layer, respectively.
[0085] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

Claims

1. An integrated chip comprising: a semiconductor substrate; a first dielectric layer over the semiconductor substrate; a first conductive line between sidewalls of the first dielectric layer; a second dielectric layer over the first dielectric layer and the first conductive line; a conductive via over the first conductive line and between sidewalls of the second dielectric layer; a second conductive line over the conductive via, the conductive via coupling the second conductive line to the first conductive line; and a first protective dielectric structure extending along a first sidewall of the conductive via and a first sidewall of the first conductive line.
2. The integrated chip of claim 1, wherein the first protective dielectric structure is directly over the first sidewall of the first conductive line and an upper surface of the first conductive line.
3. The integrated chip of claim 1, wherein the second dielectric layer extends along a second sidewall of the conductive via, opposite the first sidewall of the conductive via, and the first dielectric layer extends along a second sidewall of the first conductive line, opposite the first sidewall of the first conductive line.
4. The integrated chip of claim 1, further comprising: a second protective dielectric structure extending along a second sidewall of the conductive via, opposite the first sidewall of the conductive via, and along a second sidewall of the first conductive line, opposite the first sidewall of the first conductive line, the first protective dielectric structure and the second protective dielectric structure comprising a different dielectric than the first dielectric layer and the second dielectric layer.
5. The integrated chip of claim 4, further comprising: a third conductive line and a fourth conductive line on opposite sides of the first conductive line and laterally spaced from the first conductive line, wherein the first protective dielectric structure extends directly between the first conductive line and the third conductive line, and wherein the second protective dielectric structure extends directly between the first conductive line and the fourth conductive line.
6. The integrated chip of claim 1, wherein the first conductive line is elongated in a first direction, the second conductive line is elongated in a second direction different than the first direction, and the first protective dielectric structure is elongated in the first direction.
7. The integrated chip of claim 6, wherein a pair of sidewalls of the second conductive line extend in the second direction and are directly over the first protective dielectric structure.
8. The integrated chip of claim 1, wherein the first protective dielectric structure extends along a lower surface of the second conductive line.
9. The integrated chip of claim 1, wherein a lower surface of the first protective dielectric structure is below a top surface of the first conductive line and on an upper surface of the first dielectric layer.
10. An integrated chip comprising: a semiconductor substrate; a first lower conductive line and a

second lower conductive line over the semiconductor substrate, the first lower conductive line laterally spaced from the second lower conductive line; a first dielectric layer over the semiconductor substrate and directly between the first lower conductive line and the second lower conductive line; a second dielectric layer over the first dielectric layer, the first lower conductive line, and the second lower conductive line; a first conductive via over and coupled to the first lower conductive line and between first sidewalls of the second dielectric layer; a second conductive via over and coupled to the second lower conductive line and between second sidewalls of the second dielectric layer; and a protective dielectric layer between the first conductive via and the second conductive via and between the first lower conductive line and the second lower conductive line.

11. The integrated chip of claim 10, wherein the first dielectric layer comprises a first dielectric, the second dielectric layer comprises a second dielectric, and the protective dielectric layer comprises a third dielectric different than the first dielectric and the second dielectric.

12. The integrated chip of claim 10, wherein the protective dielectric layer extends from a sidewall of the first conductive via to a sidewall of the second conductive via.

13. The integrated chip of claim 12, wherein the protective dielectric layer extends from a sidewall of the first lower conductive line to a sidewall of the second lower conductive line.

14. The integrated chip of claim 10, further comprising: an upper conductive line over the first conductive via, the first conductive via extending between the first lower conductive line and the upper conductive line, the protective dielectric layer extending from a lower surface of the upper conductive line to below a top surface of the first lower conductive line.

15. The integrated chip of claim 10, wherein the protective dielectric layer is on an upper surface of the first lower conductive line, on an upper surface of the second lower conductive line, and extends below the upper surface of the first lower conductive line and below the upper surface of the second lower conductive line.

16. An integrated chip comprising: a semiconductor substrate; a first dielectric layer over the semiconductor substrate, the first dielectric layer comprising a first dielectric; a first conductive line over the semiconductor substrate and between sidewalls of the first dielectric layer, the first conductive line elongated in a first direction; a second dielectric layer over the first dielectric layer and the first conductive line, the second dielectric layer comprising a second dielectric; a conductive via over the first conductive line and between sidewalls of the second dielectric layer, the conductive via having a first sidewall extending in the first direction and a second sidewall extending in a second direction transverse to the first direction; a second conductive line over the conductive via, the second conductive line elongated in the second direction, the conductive via extending from the first conductive line to the second conductive line; and a protective dielectric structure over the first dielectric layer and between the sidewalls of the second dielectric layer, the protective dielectric structure comprising a third dielectric different than the first dielectric and the second dielectric, wherein the protective dielectric structure is on the first sidewall of the conductive via and the second dielectric layer is on the second sidewall of the conductive via.

17. The integrated chip of claim 16, wherein the conductive via has a third sidewall extending in the first direction, and wherein the protective dielectric structure is on the third sidewall of the conductive via.

18. The integrated chip of claim 16, wherein the protective dielectric structure has a sidewall extending in the first direction from a first sidewall of the second dielectric layer, along the first sidewall of the conductive via, to a second sidewall of the second dielectric layer.

19. The integrated chip of claim 16, wherein the protective dielectric structure extends along an upper portion of a sidewall of the first conductive line and the first dielectric extends along a lower portion of the sidewall of the first conductive line.

20. The integrated chip of claim 16, wherein the first sidewall of the conductive via and the second sidewall of the conductive via are directly over the first conductive line.