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Im et al.

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(54) **SEMICONDUCTOR PACKAGE INCLUDING A HEAT DISSIPATION STRUCTURE**

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(73) Assignee: **SAMSUNG ELECTRONICS CO., LTD.**, Suwon-si (KR)

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(21) Appl. No.: **18/052,187**

(22) Filed: **Nov. 2, 2022**

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(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**

H01L 23/02	(2006.01)
H01L 23/31	(2006.01)
H01L 23/367	(2006.01)
H01L 23/373	(2006.01)
H01L 23/498	(2006.01)
H01L 23/00	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 23/367*** (2013.01); ***H01L 23/3128*** (2013.01); ***H01L 23/3736*** (2013.01); ***H01L 23/49811*** (2013.01); ***H01L 23/49822*** (2013.01); *H01L 24/16* (2013.01); *H01L 2224/16227* (2013.01)

(58) **Field of Classification Search**

CPC H01L 23/367; H01L 23/3128; H01L 23/3736; H01L 23/49811; H01L 23/49822; H01L 24/16; H01L 2224/16227; H01L 23/552; H01L 2224/81; H01L 21/56; H01L 23/3142; H01L 23/315; H01L 23/3733; H01L 25/105; H01L 23/3677; H01L 23/5389; H01L 23/49816

USPC 257/668

See application file for complete search history.

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Primary Examiner — Theresa T Doan

(74) *Attorney, Agent, or Firm* — Morgan, Lewis & Bockius LLP

(57) **ABSTRACT**

A semiconductor package includes a first substrate, a semiconductor chip disposed on the first substrate, a mold layer disposed on the first substrate and at least partially covering the semiconductor chip, and a heat dissipation structure disposed on a first top surface of the semiconductor chip and in the mold layer. The heat dissipation structure covers an inner side surface of the mold layer. A surface roughness of the first top surface of the semiconductor chip is greater than a surface roughness of a side surface of the semiconductor chip, and a surface roughness of the inner side surface of the mold layer is greater than a surface roughness of a top surface of the mold layer. The heat dissipation structure includes voids therein.

20 Claims, 24 Drawing Sheets

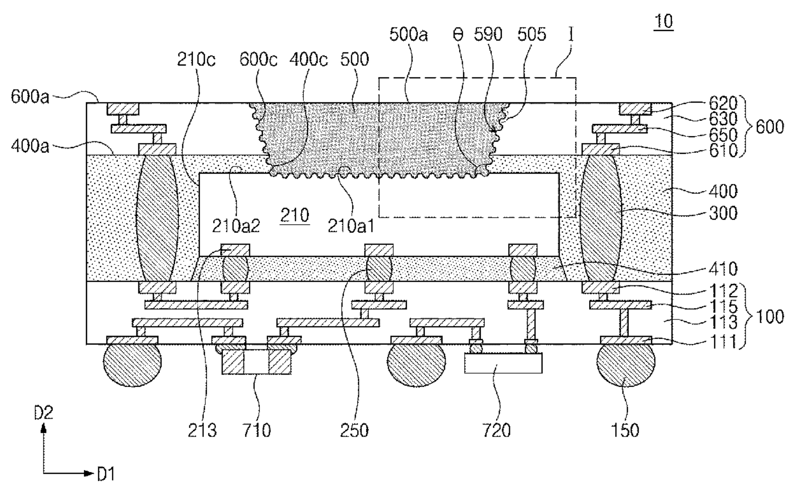

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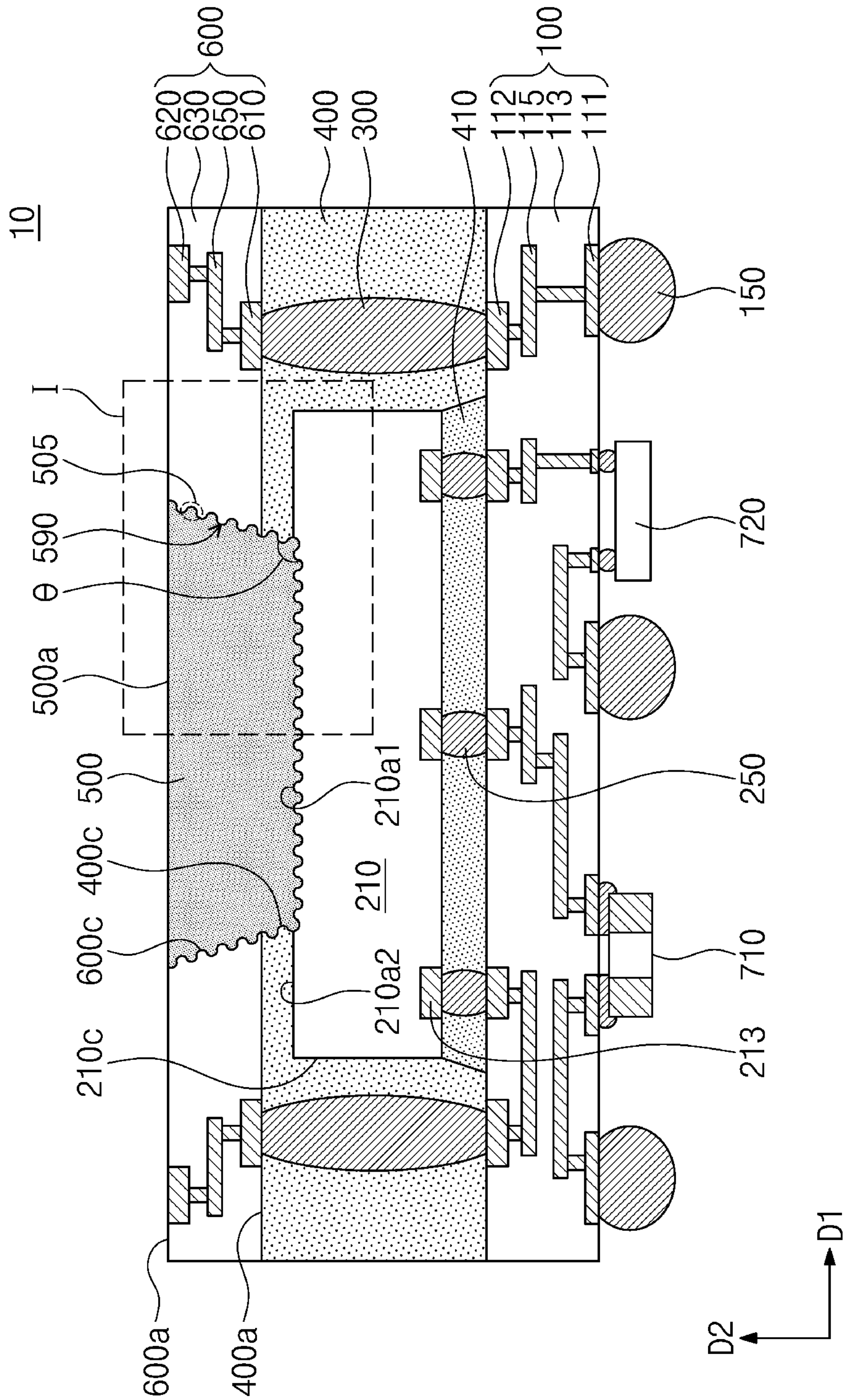
FIG. 1A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600
620
630
650
610
400
300
410
100
112
115
113
111
150
720
250
710
213
I
505
590
θ
500a
500
400c
600c
210c
210a1
210
210a2
600a
400a
D1
D2

FIG. 1B

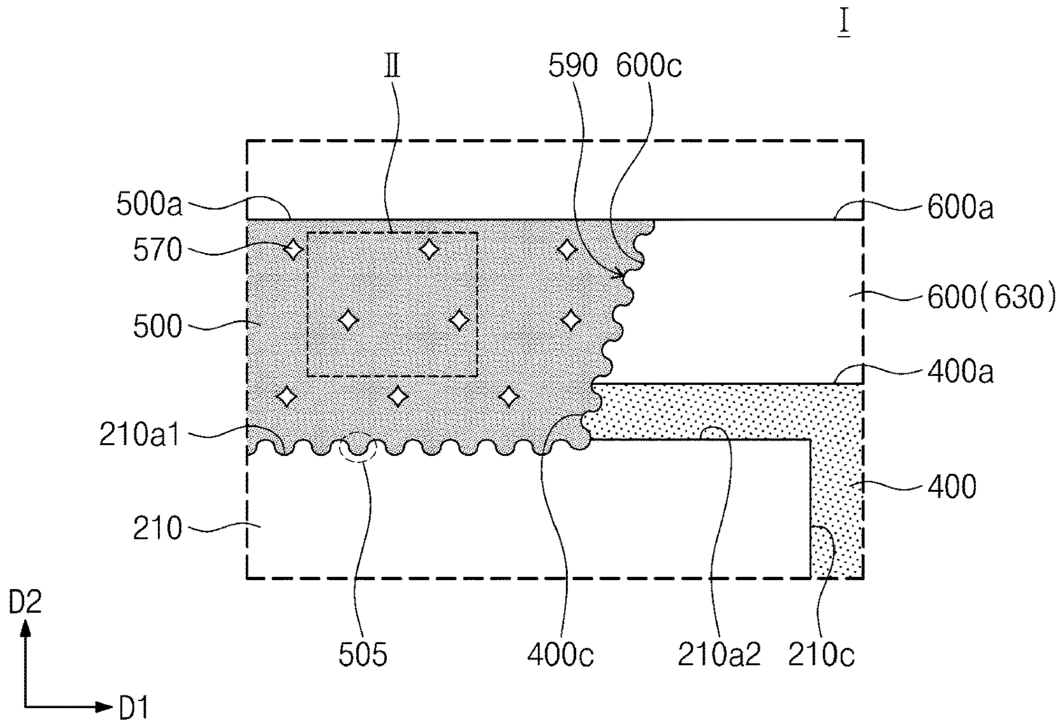

I
II
590
600c
500a
600a
570
500
600(630)
400a
210a1
400
210
505
400c
210a2
210c
D2
D1

FIG. 1C

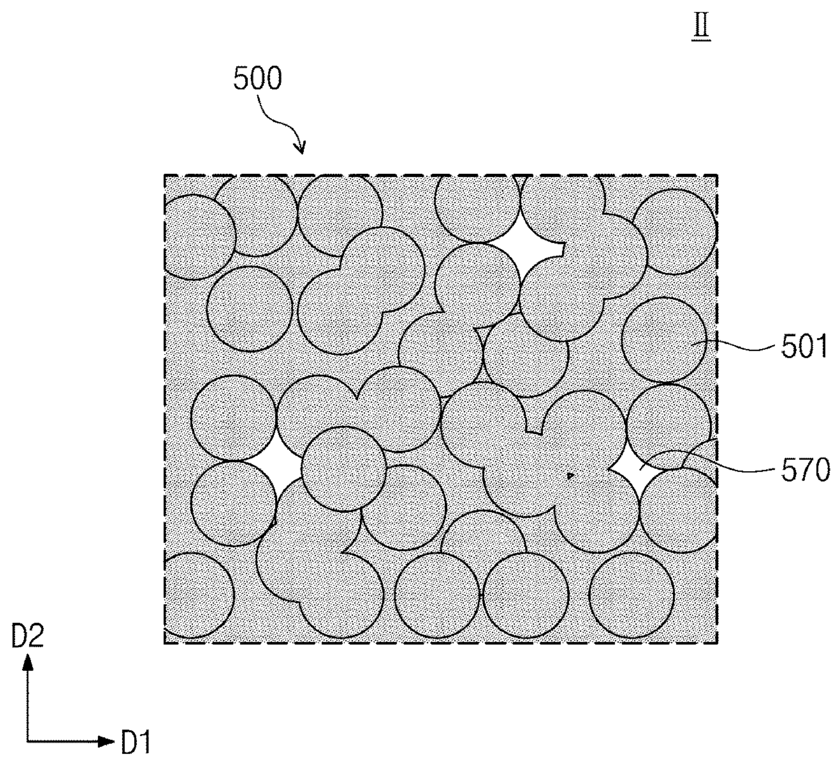

II
500
501
570
D2
D1

FIG. 1D

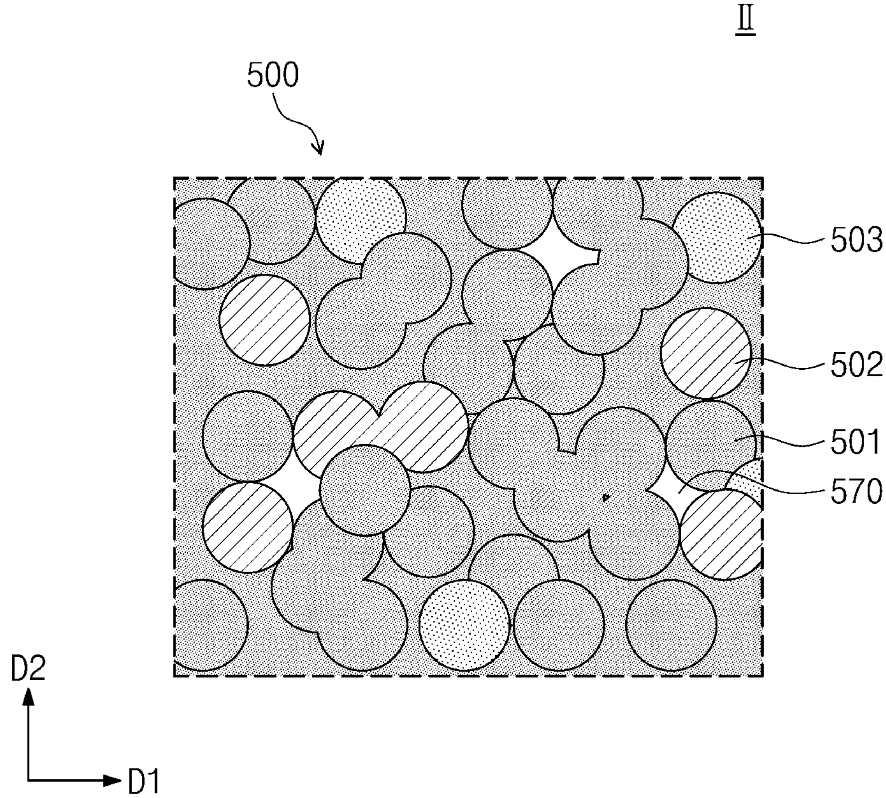


FIG. 2A

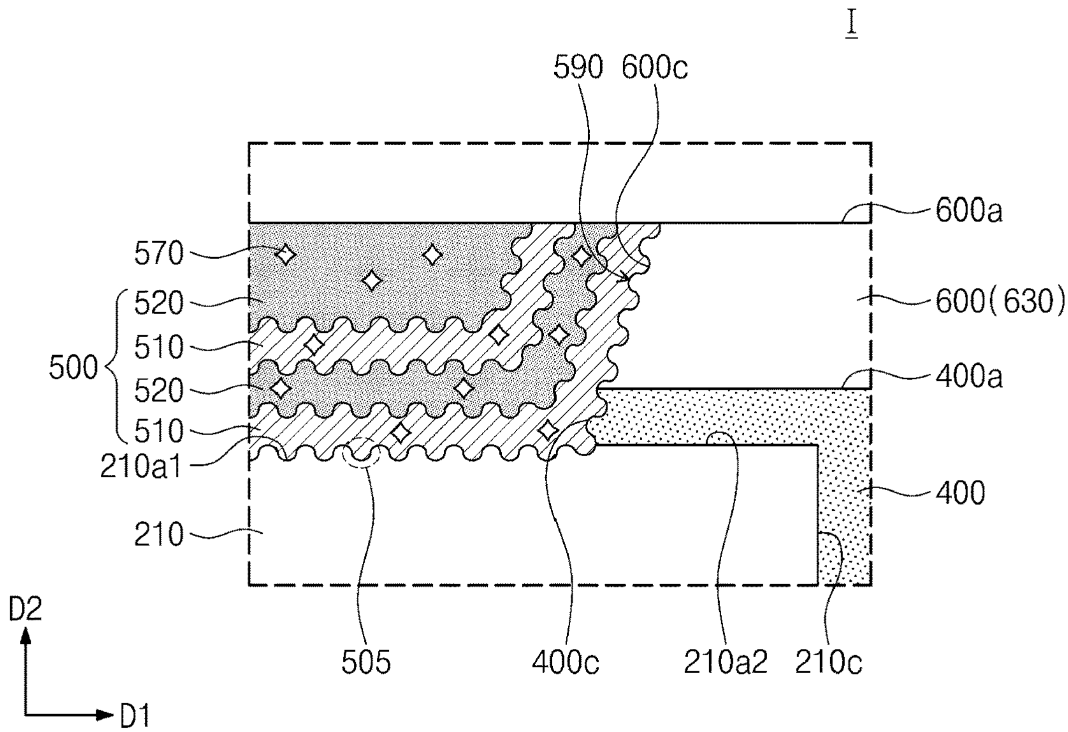

I
590
600c
600a
570
520
510
520
510
500
600(630)
400a
210a1
400
210
D2
D1
505
400c
210a2
210c

FIG. 2B

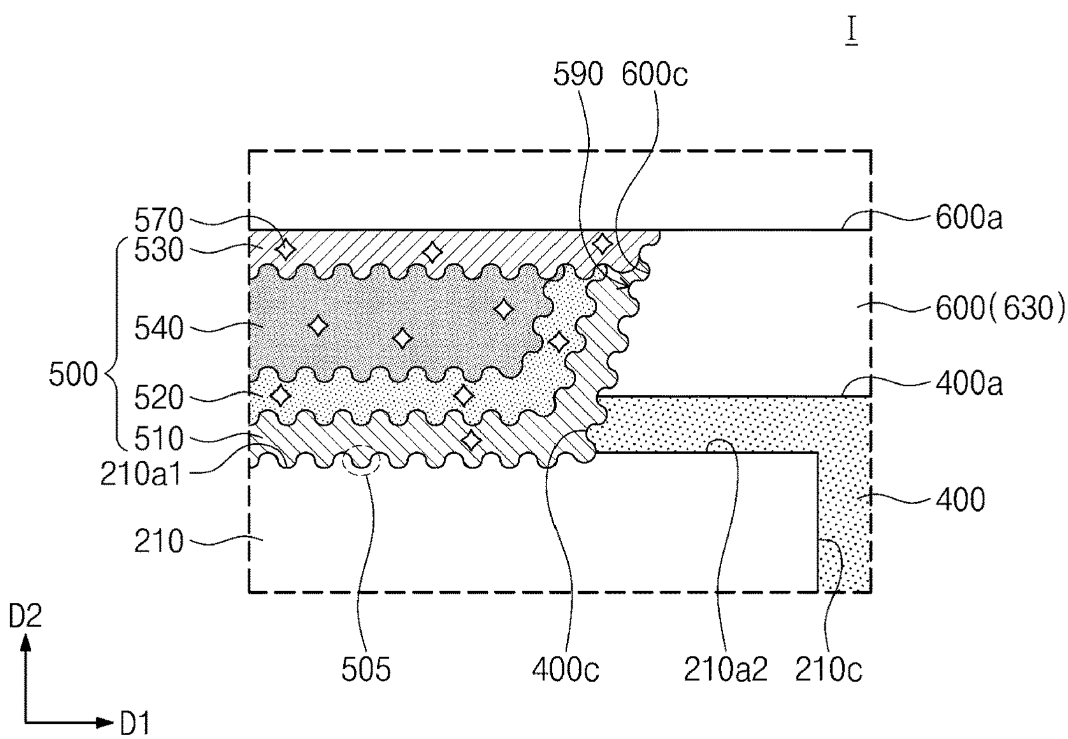

I
590
600c
570
530
600a
540
600(630)
500
520
400a
510
210a1
400
210
D2
D1
505
400c
210a2
210c

FIG. 2C

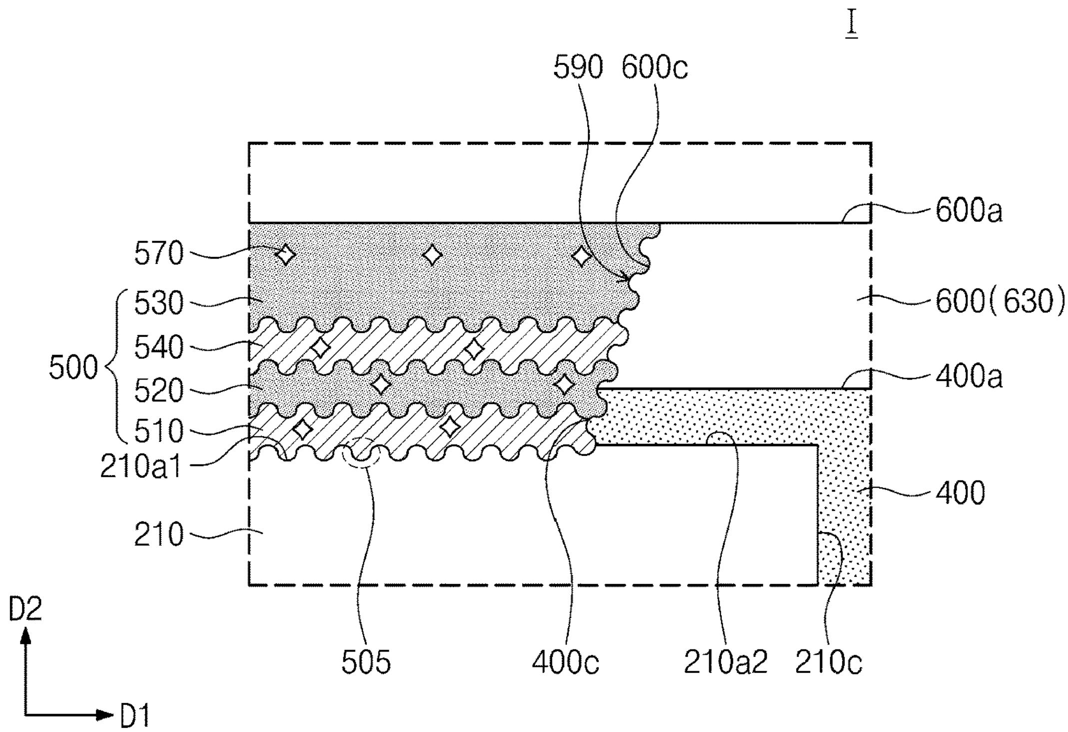

I
590 600c
600a
570
530
540
500
520
510
210a1
210
600(630)
400a
400
505
400c
210a2
210c
D2
D1

FIG. 2D

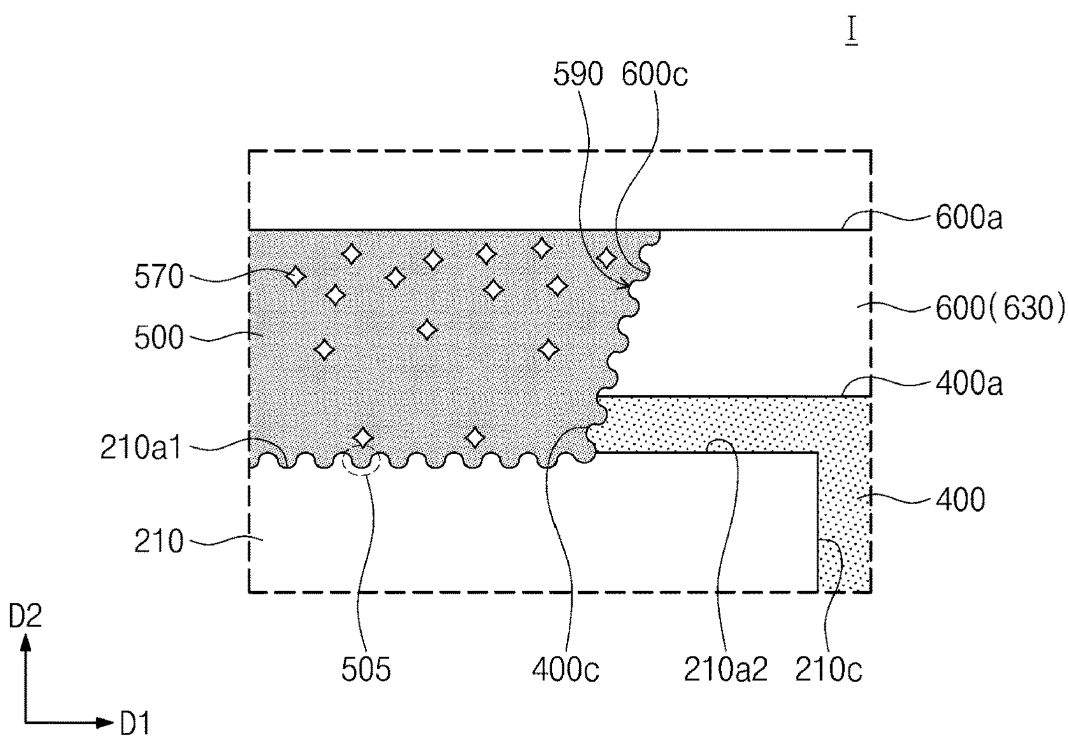

I
590 600c
600a
570
500
210a1
210
600(630)
400a
400
505
400c
210a2
210c
D2
D1

FIG. 2E

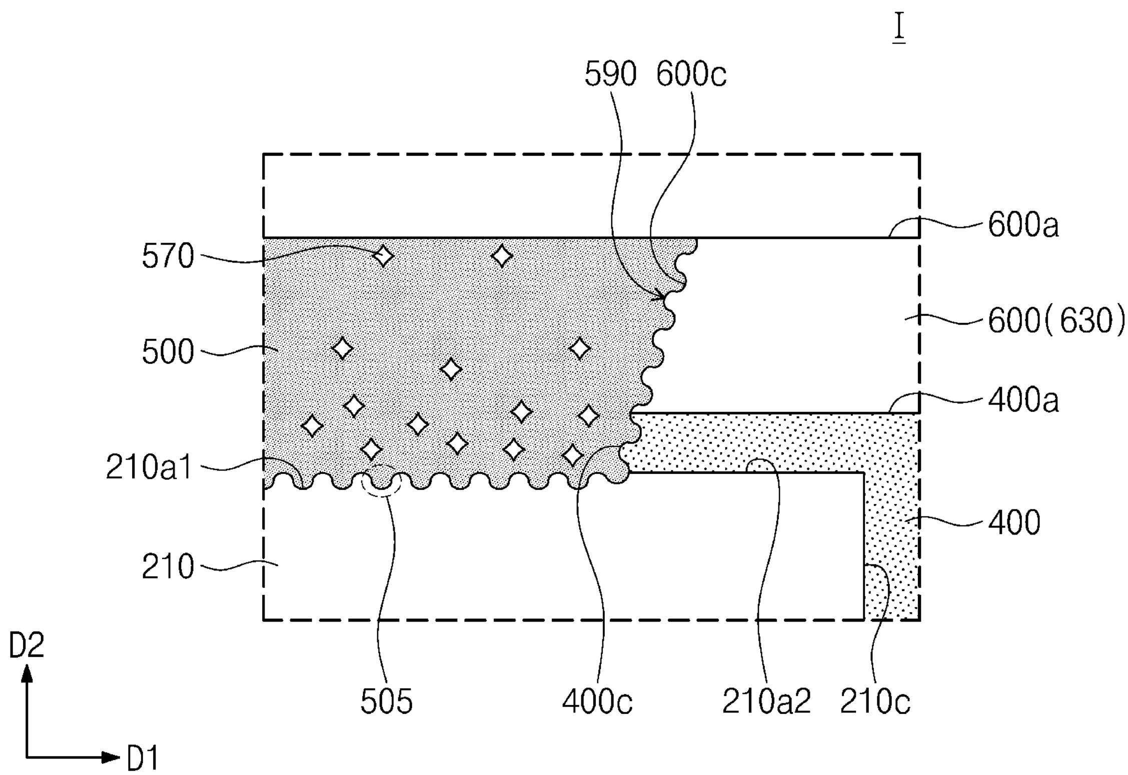

I
590
600c
600a
570
600(630)
500
400a
210a1
400
210
D2
D1
505
400c
210a2
210c

FIG. 3A

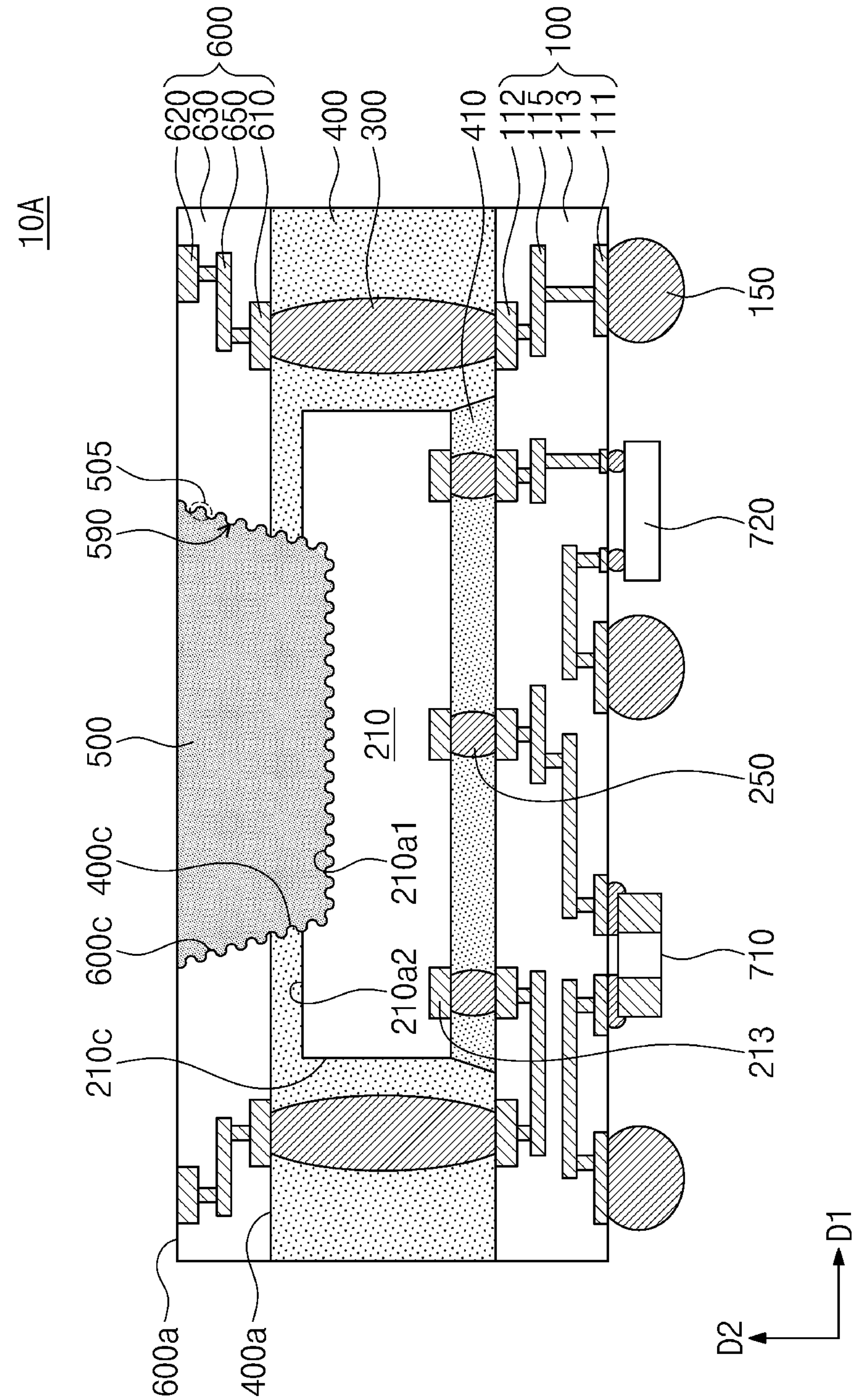

10A
600
620
630
650
610
400
300
410
112
115
113
111
100
150
720
250
710
213
505
590
500
400c
600c
210c
210
210a1
210a2
600a
400a
D1
D2

FIG. 3B

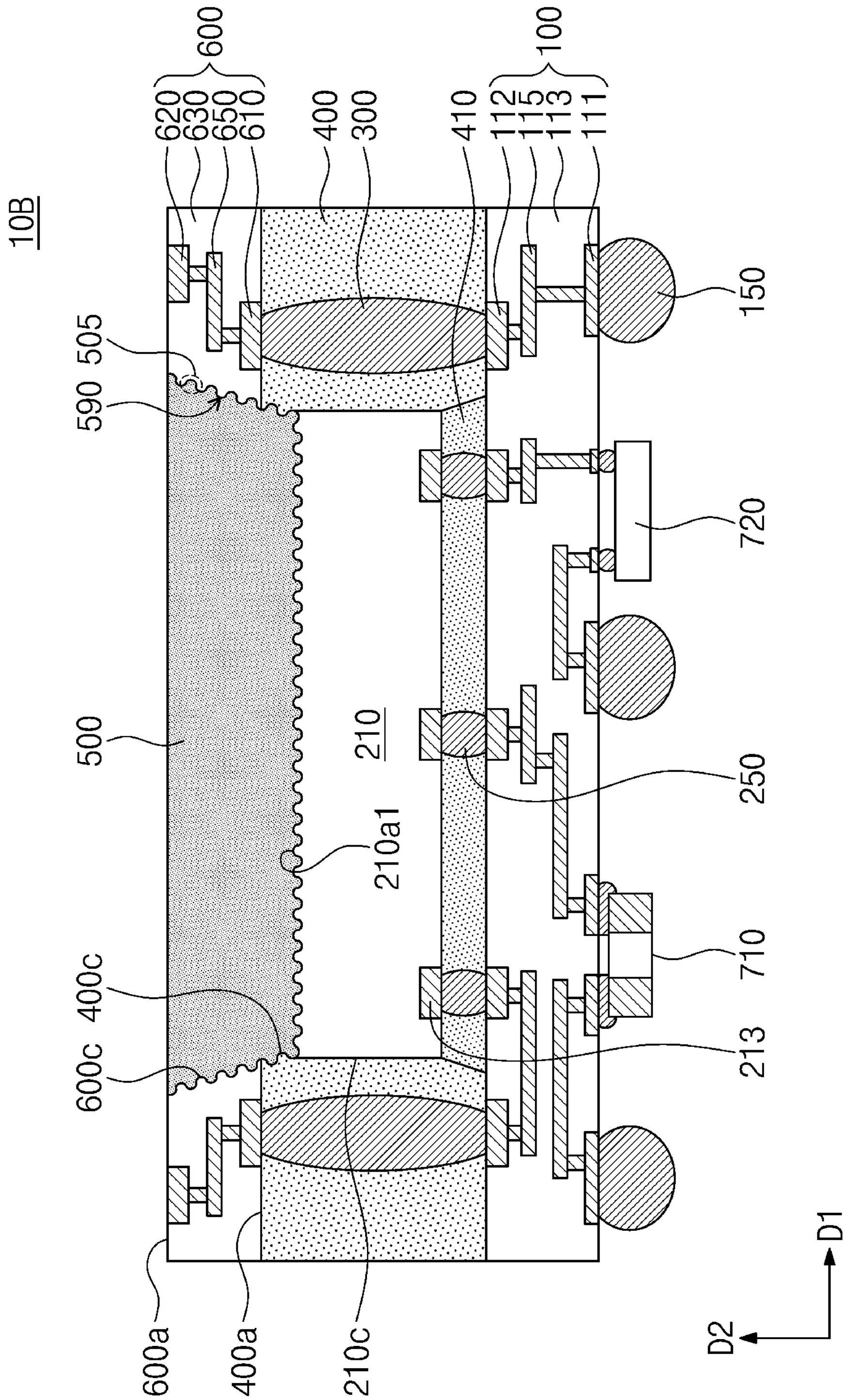
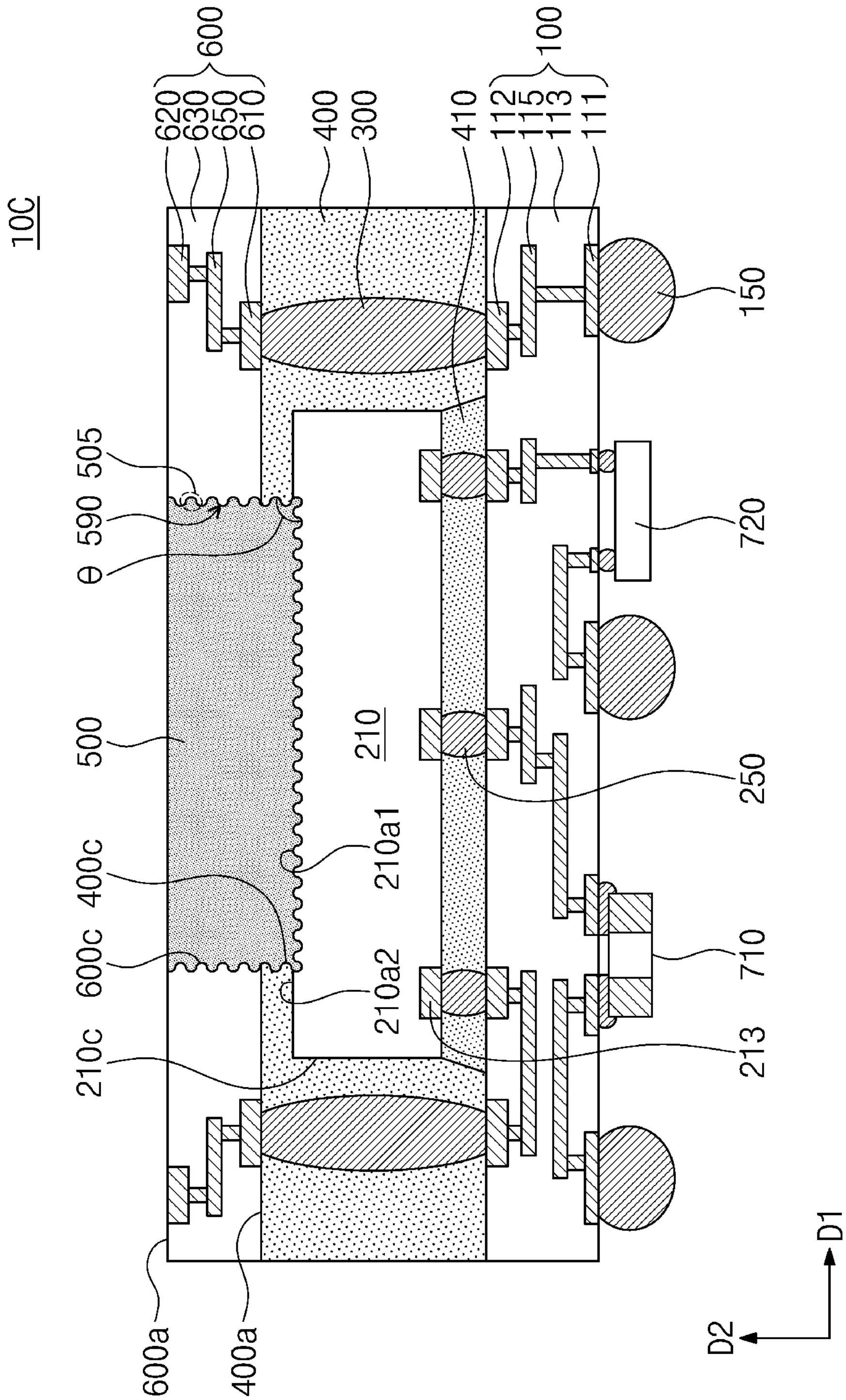

10B
600
620
630
650
610
400
300
410
100
112
115
113
111
150
720
250
710
213
505
590
500
210
210a1
400c
600c
600a
400a
210c
D2
D1

FIG. 3C



10C
600
620
630
650
610
400
300
410
100
112
115
113
111
150
505
590
θ
720
500
210
250
400c
210a1
600c
210a2
710
210c
213
600a
400a
D2
D1

FIG. 3D

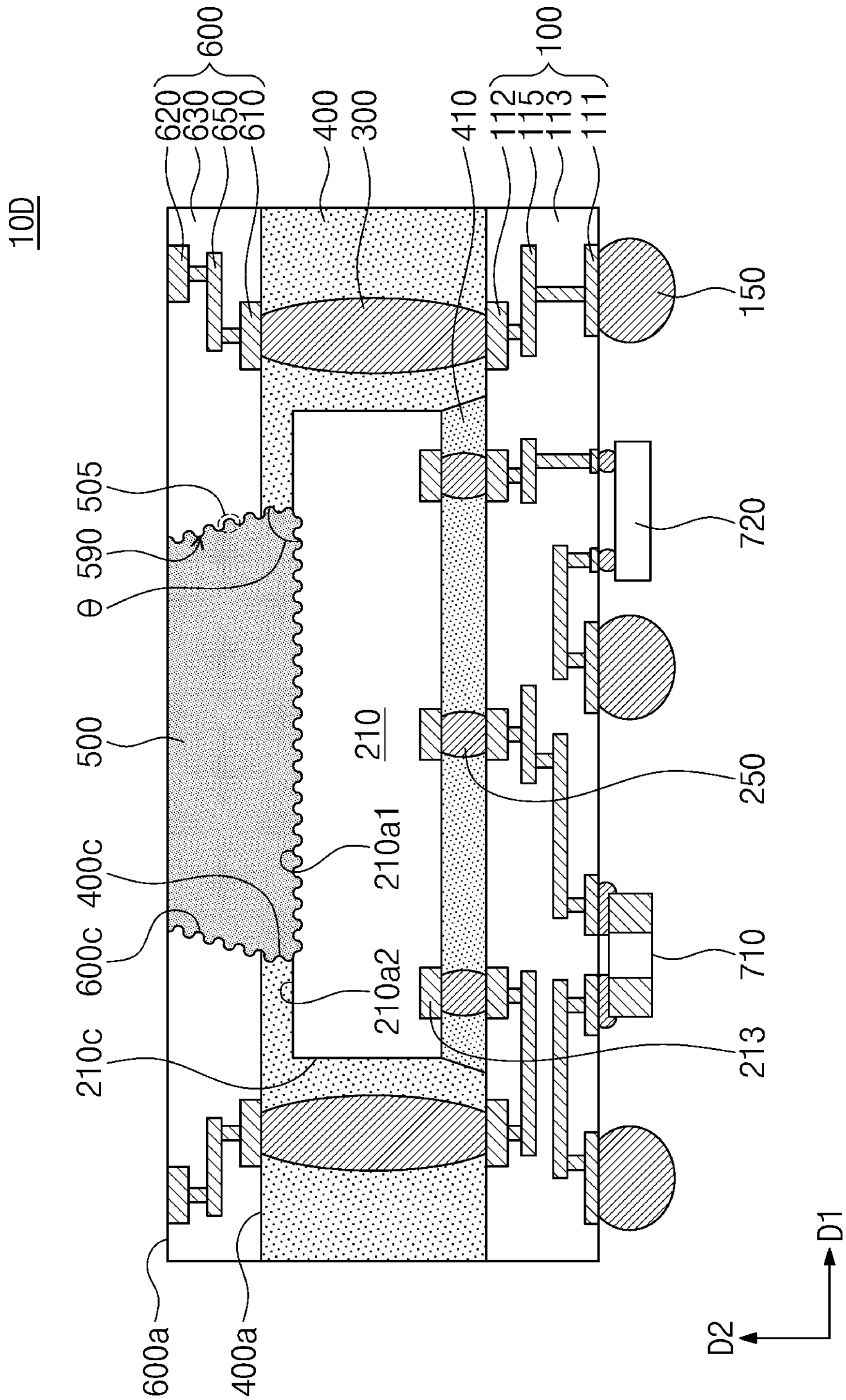

10D
600
620
630
650
610
400
300
410
100
112
115
113
111
150
720
250
710
213
505
590
θ
500
400c
600c
210c
210
210a1
210a2
600a
400a
D1
D2

FIG. 3E

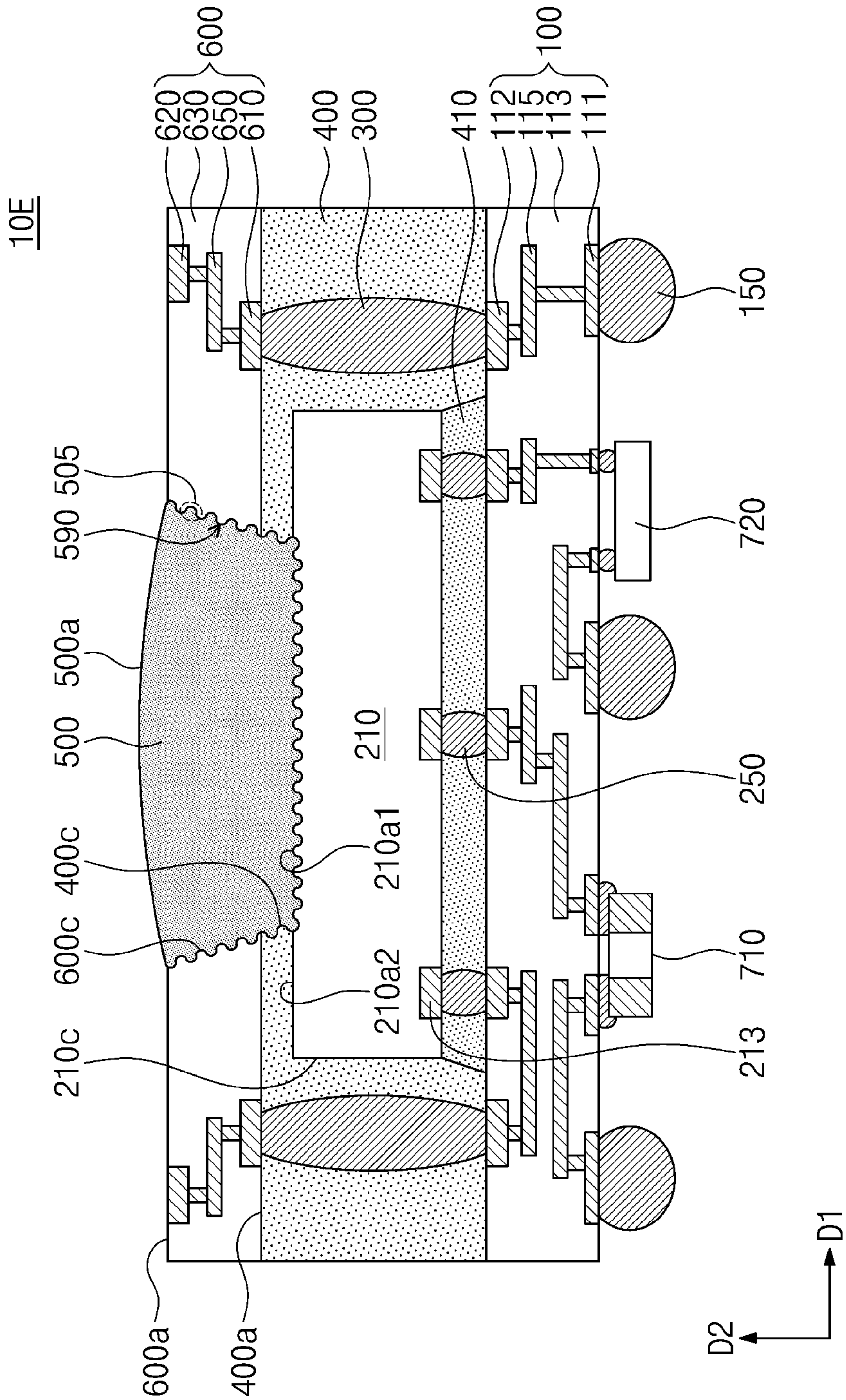

10E
600
620
630
650
610
400
300
410
100
112
115
113
111
150
720
250
710
213
505
590
500a
500
400c
600c
210c
210
210a1
210a2
600a
400a
D1
D2

FIG. 3F

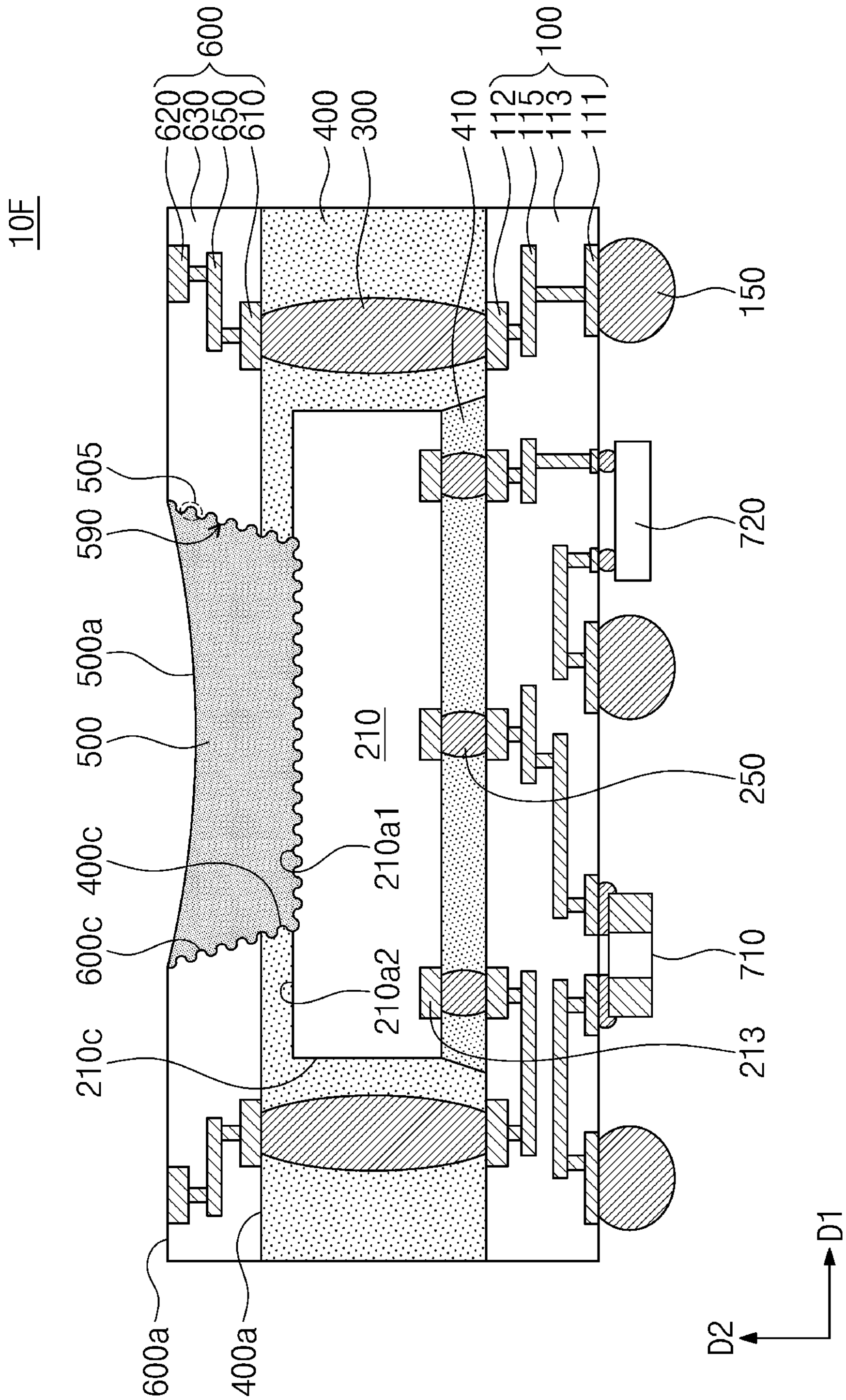

10F
600
620
630
650
610
400
300
410
100
112
115
113
111
150
505
590
500a
500
210
720
400c
210a1
250
600c
210a2
213
710
210c
600a
400a
D1
D2

FIG. 3G

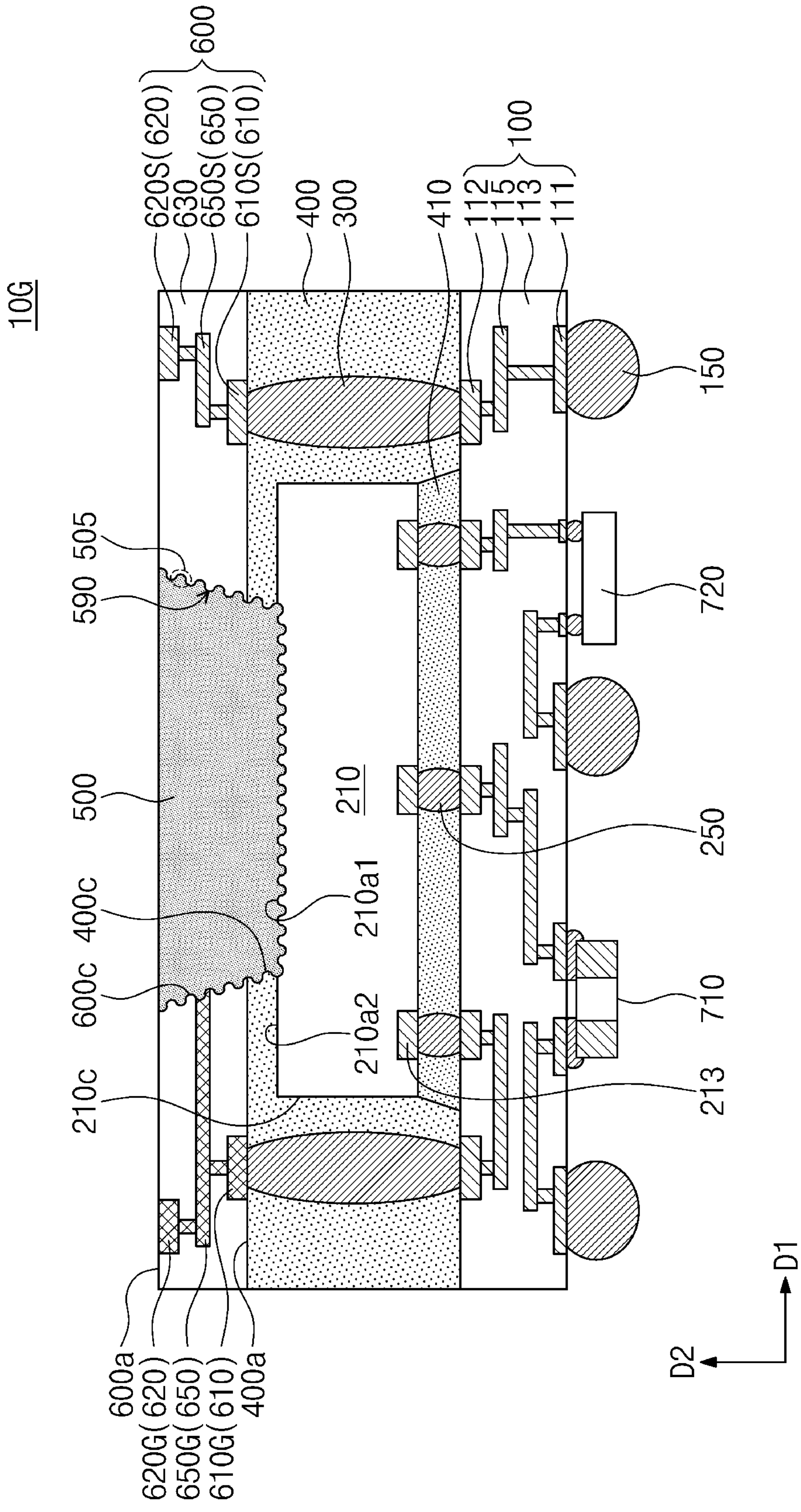

10G
600
620S(620)
630
650S(650)
610S(610)
400
300
410
100
112
115
113
111
150
720
250
710
213
505
590
500
400c
600c
210c
210a1
210a2
210
600a
620G(620)
650G(650)
610G(610)
400a
D1
D2

FIG. 3H

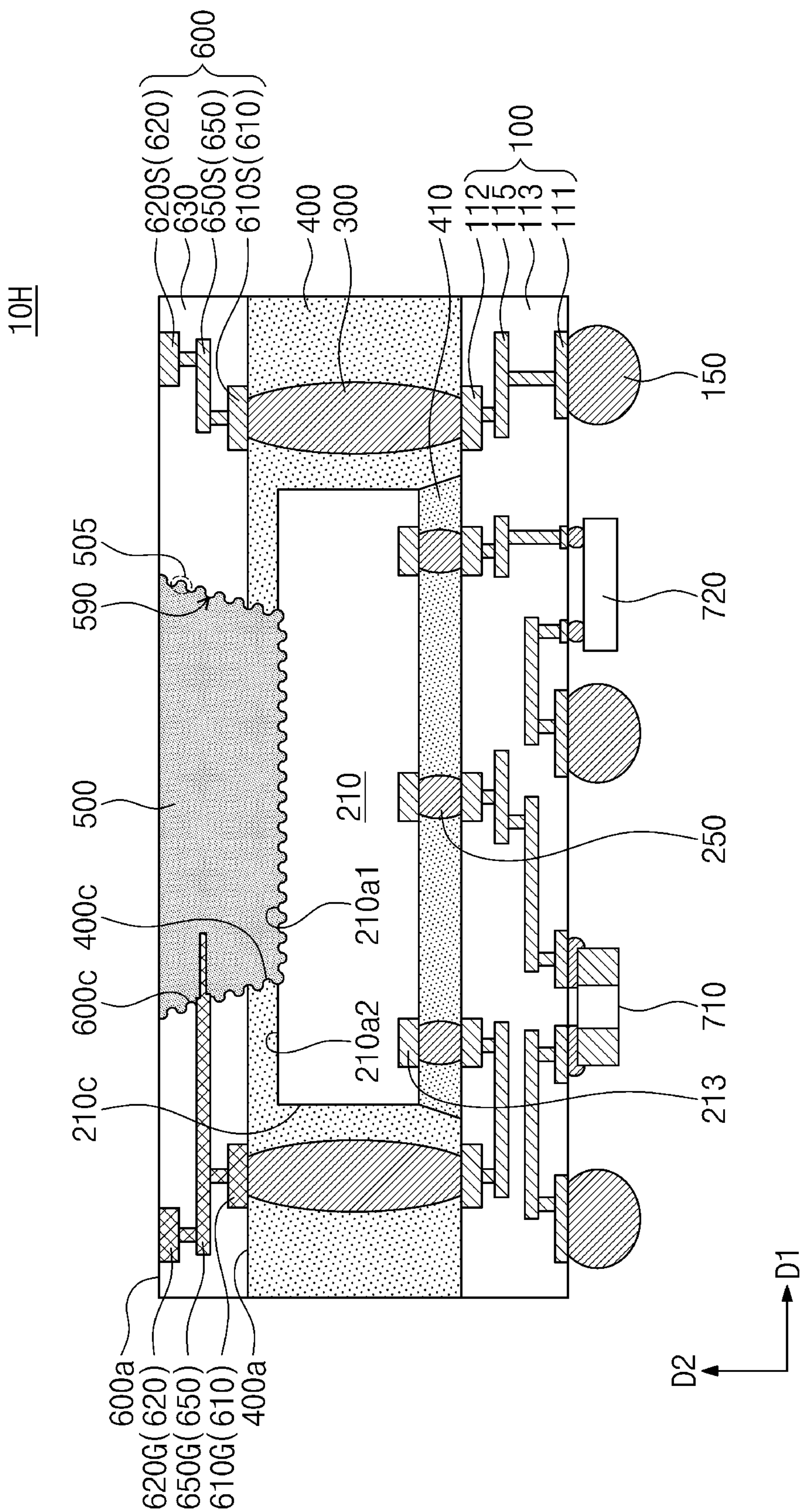

10H
600
620S(620)
630
650S(650)
610S(610)
400
300
410
100
112
115
113
111
150
505
590
720
500
210
250
400c
210a1
600c
710
210a2
213
210c
600a
620G(620)
650G(650)
610G(610)
400a
D1
D2

FIG. 3I

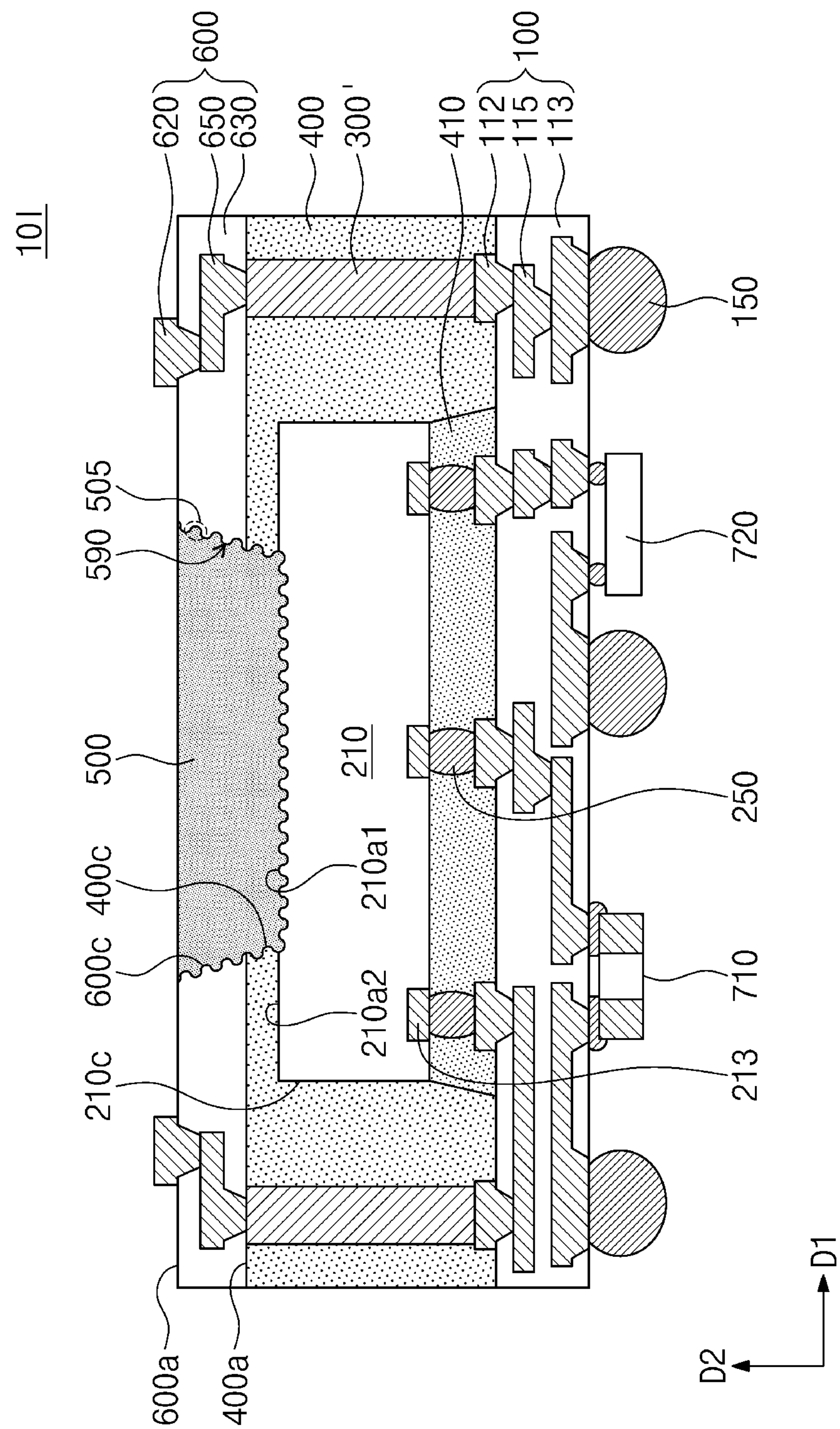

101
620
650
630
600
400
300'
410
112
115
113
100
150
505
590
720
500
210
250
400c
210a1
600c
210a2
710
210c
213
600a
400a
D2
D1

FIG. 3J

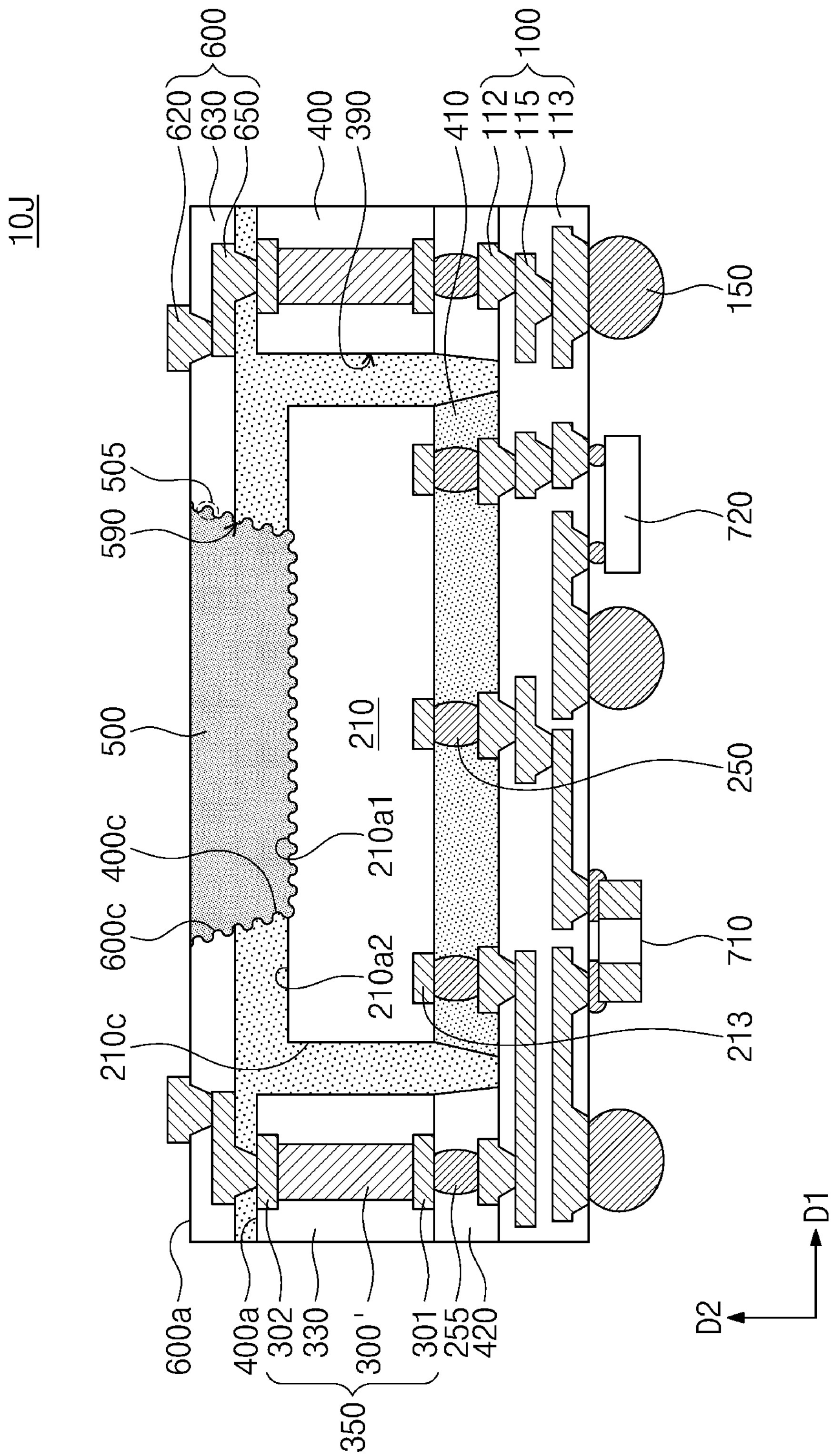
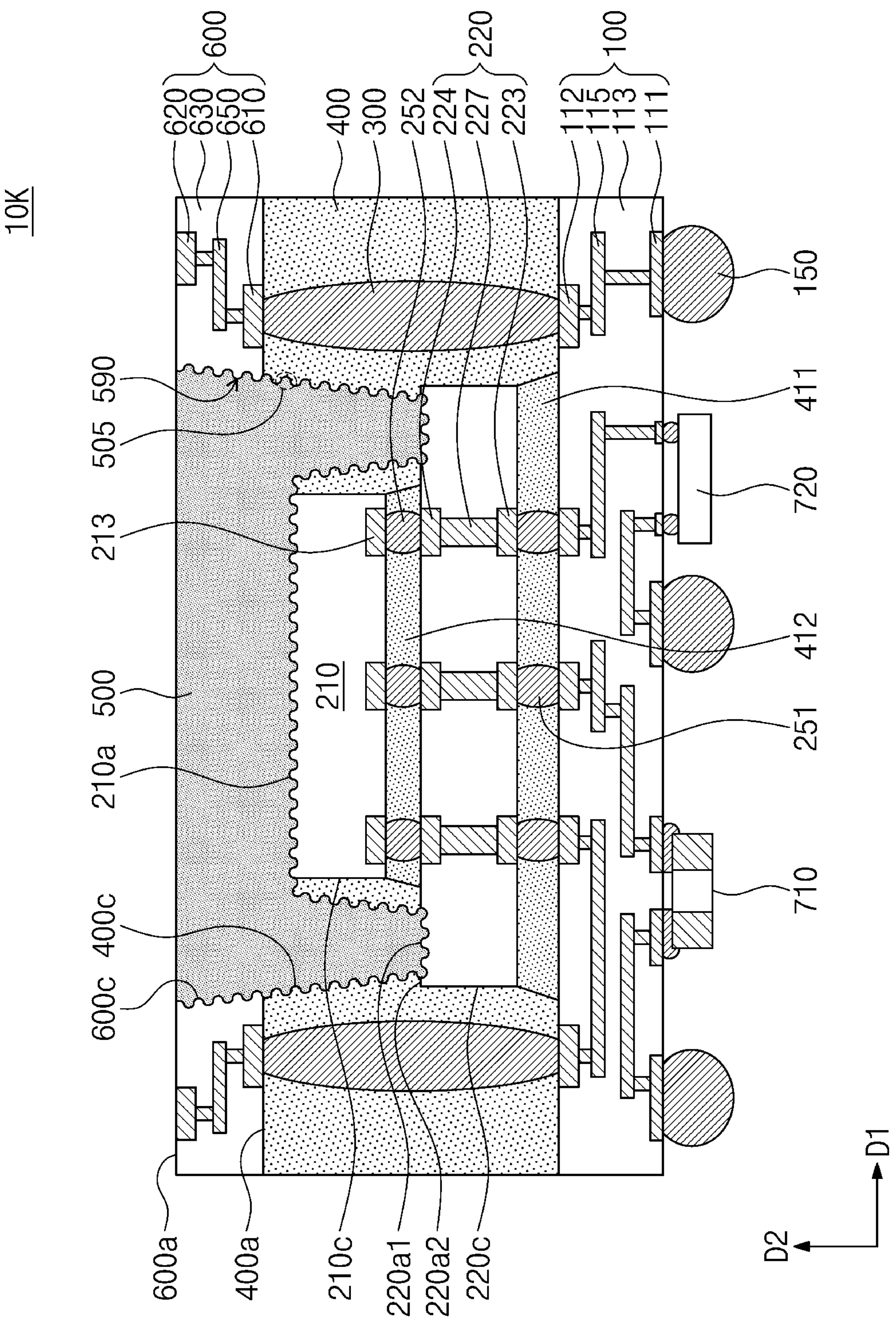

10J
600
620
630
650
400
390
410
100
112
115
113
150
505
590
500
210
720
250
400c
210a1
600c
210a2
710
210c
213
600a
400a
302
330
300'
301
255
420
350
D1
D2

FIG. 3K


10K
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620
630
650
610
400
300
252
224
227
223
220
112
115
113
111
100
150
590
505
411
720
213
412
210
500
251
210a
710
400c
600c
600a
400a
210c
220a1
220a2
220c
D1
D2

FIG. 4

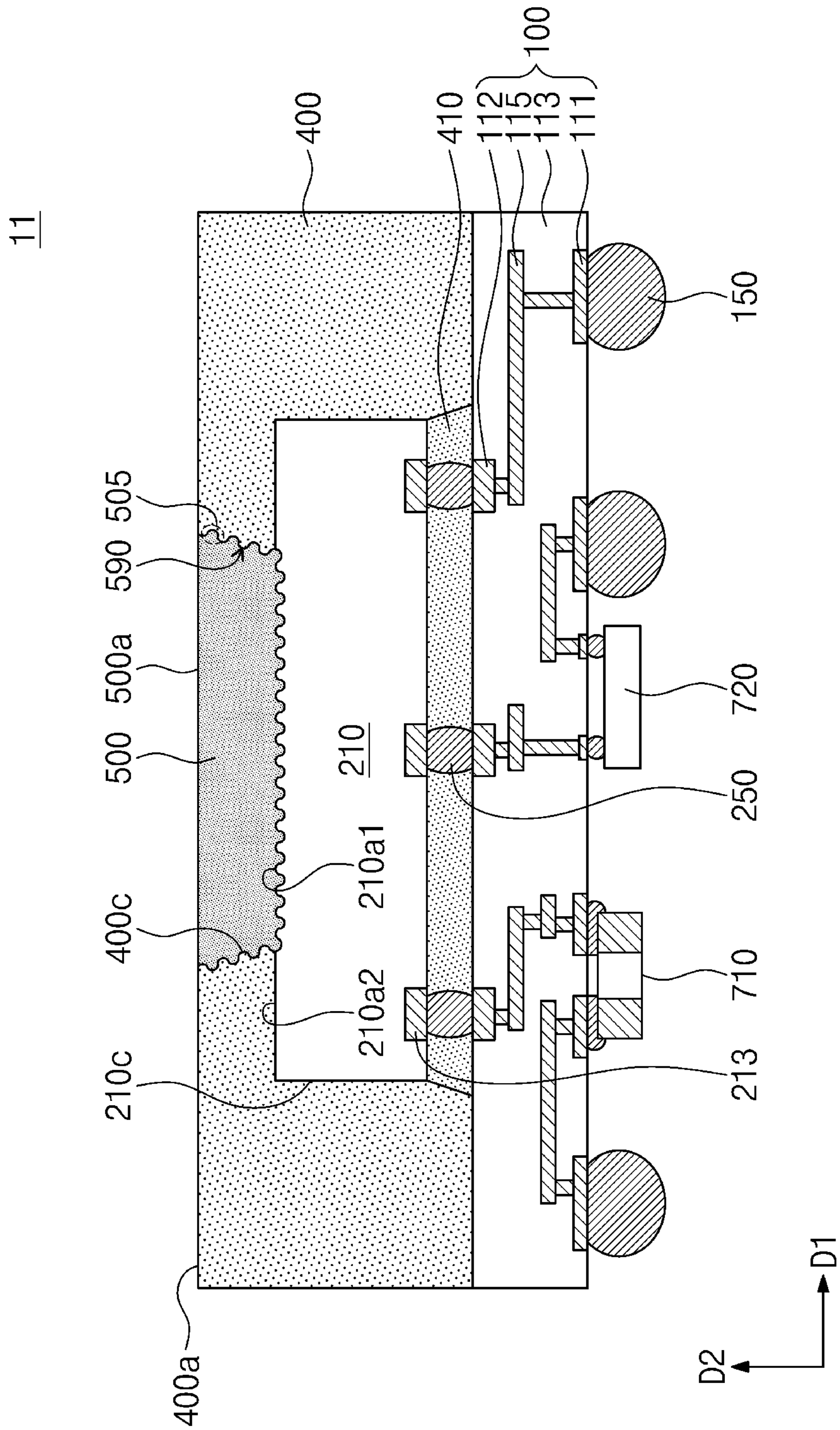
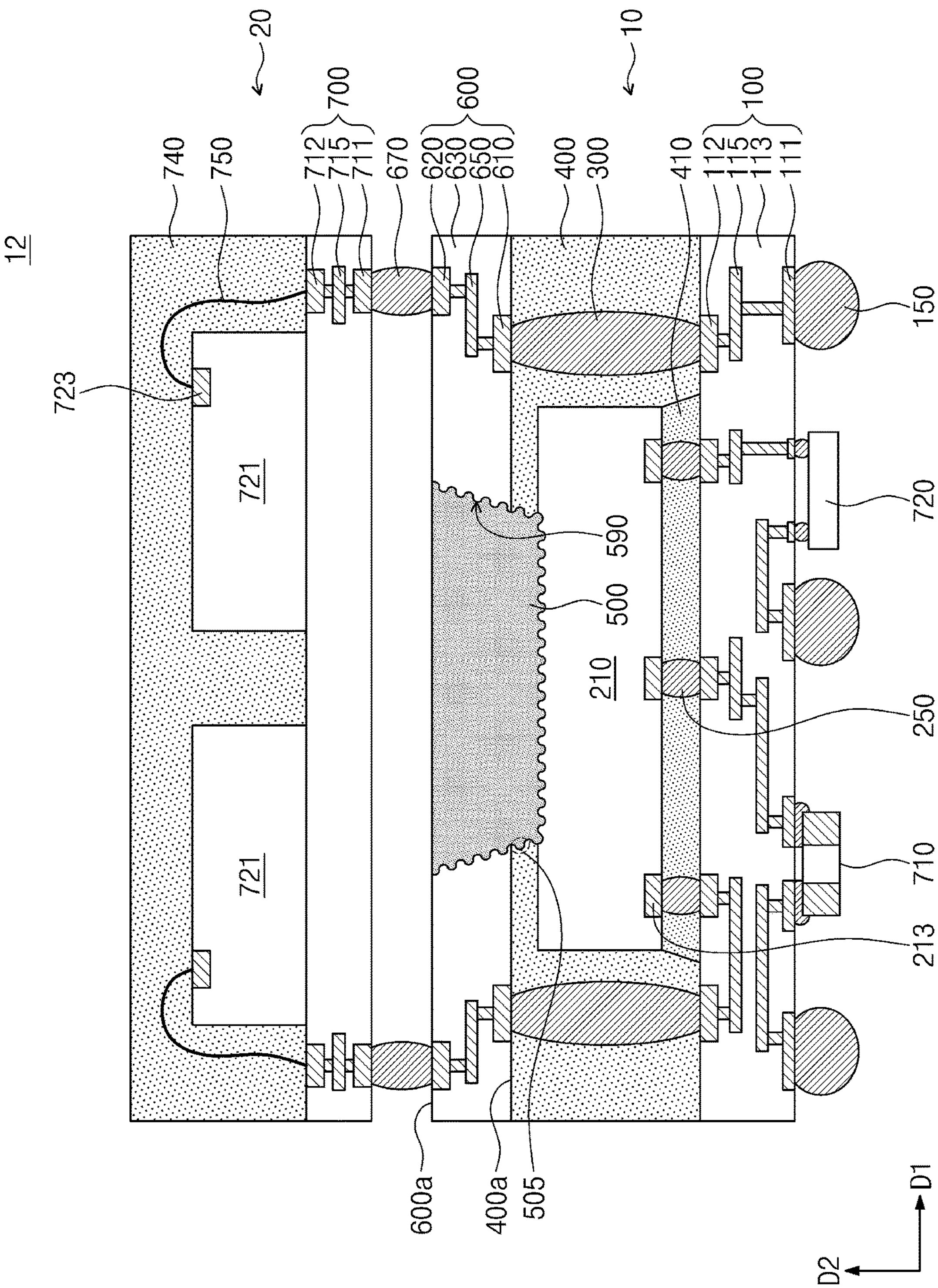

11
400
410
112
115
113
111
100
150
505
590
500a
500
210
210a1
400c
210a2
210c
213
250
720
710
400a
D1
D2

FIG. 5A


12
20
10
700
712
715
711
670
600
620
630
650
610
740
750
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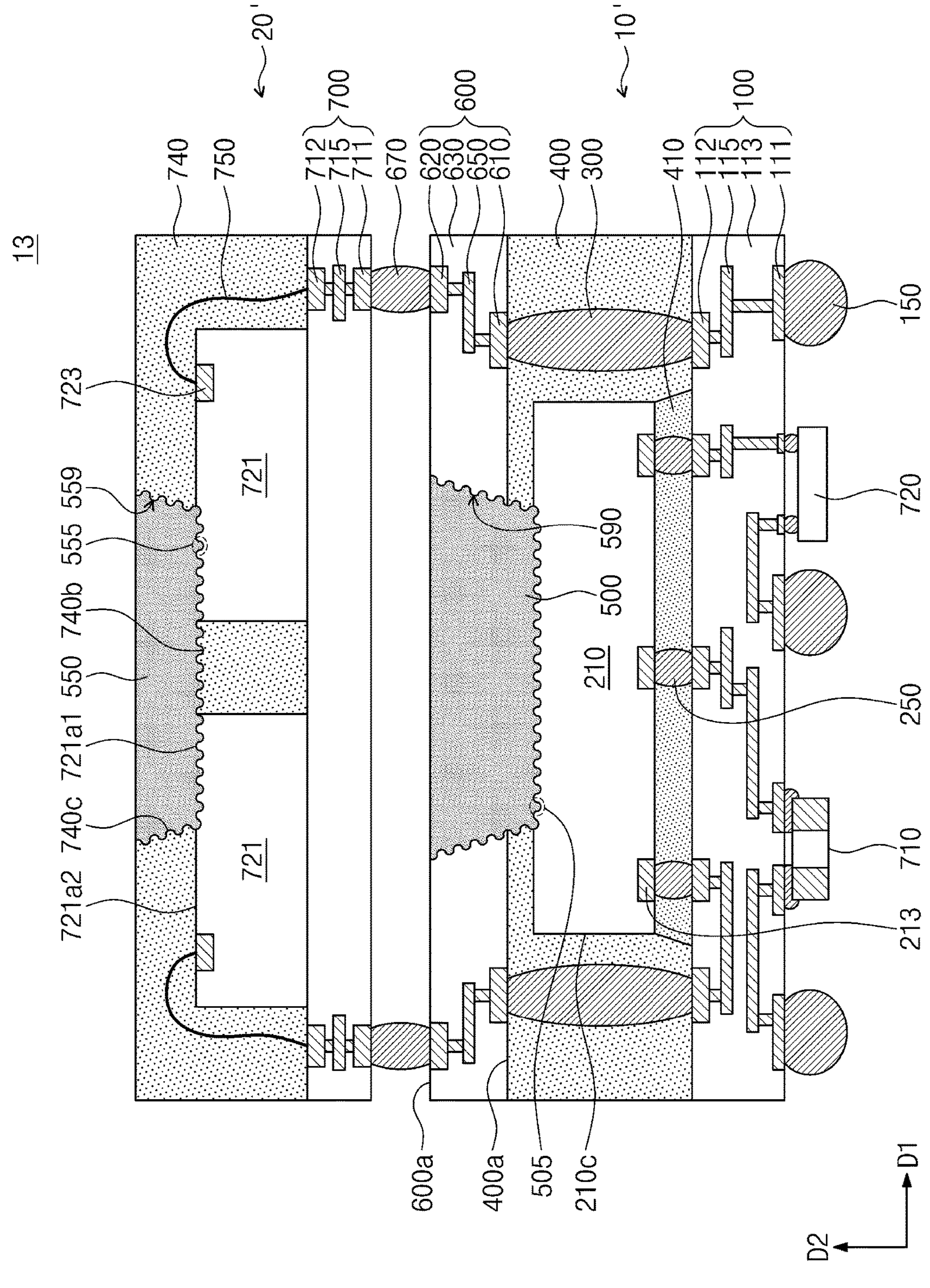
100
112
115
113
111
150
723
721
721
590
500
210
720
250
710
213
600a
400a
505
D1
D2

FIG. 5B


13
20'
10'
700
600
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750
712
715
711
670
620
630
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610
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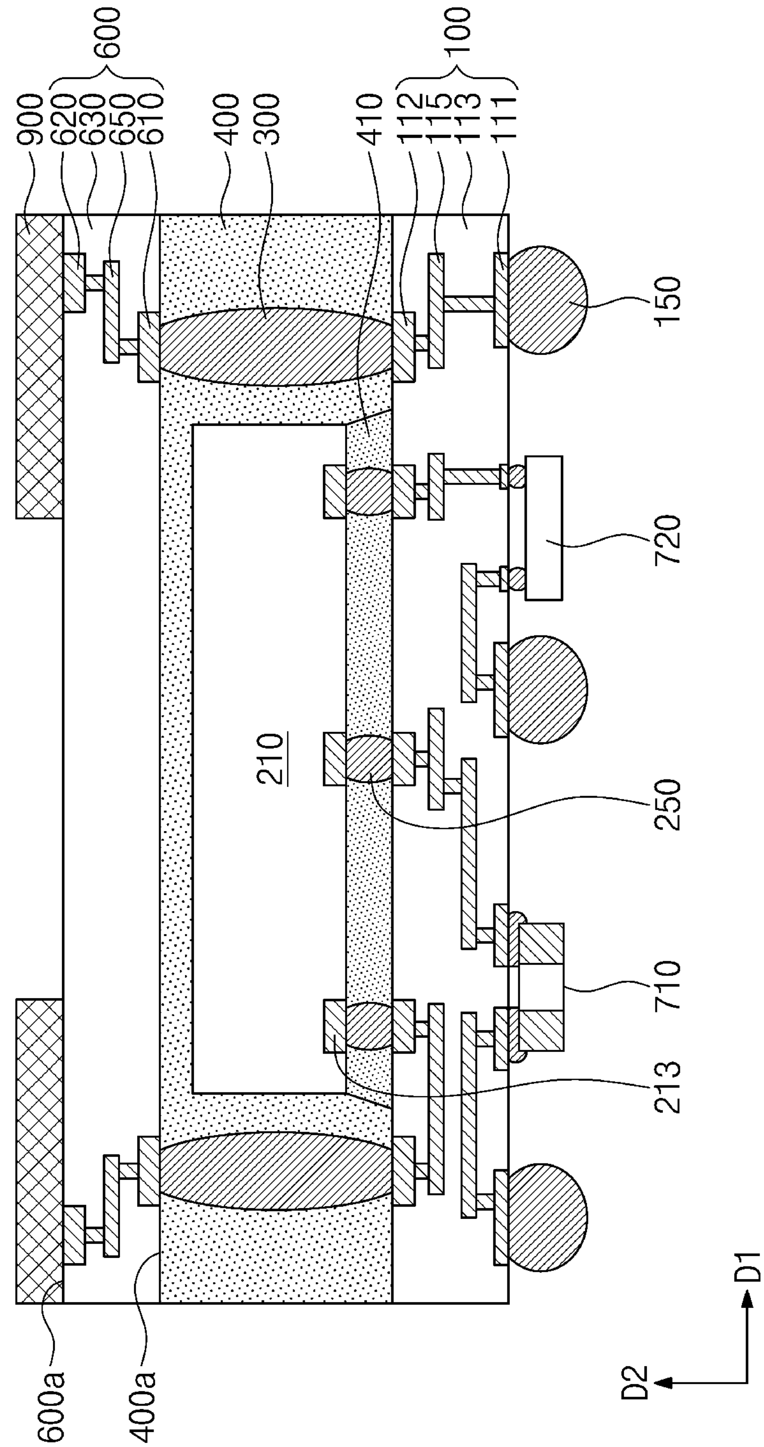
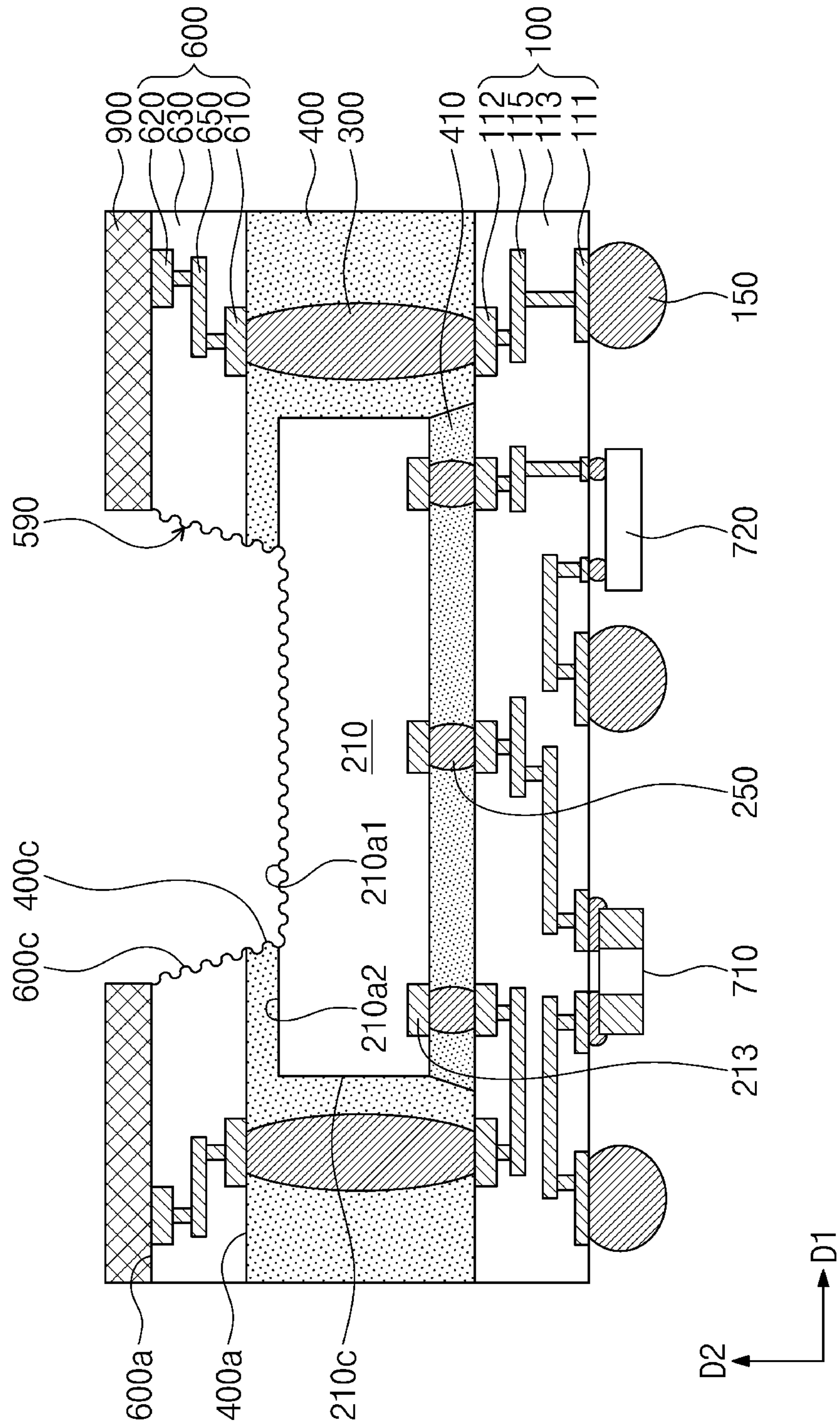
410
112
115
113
111
150
723
721
721
559
555
740b
550
721a1
740c
721a2
590
500
210
250
720
710
213
600a
400a
505
210c
D1
D2

FIG. 6A



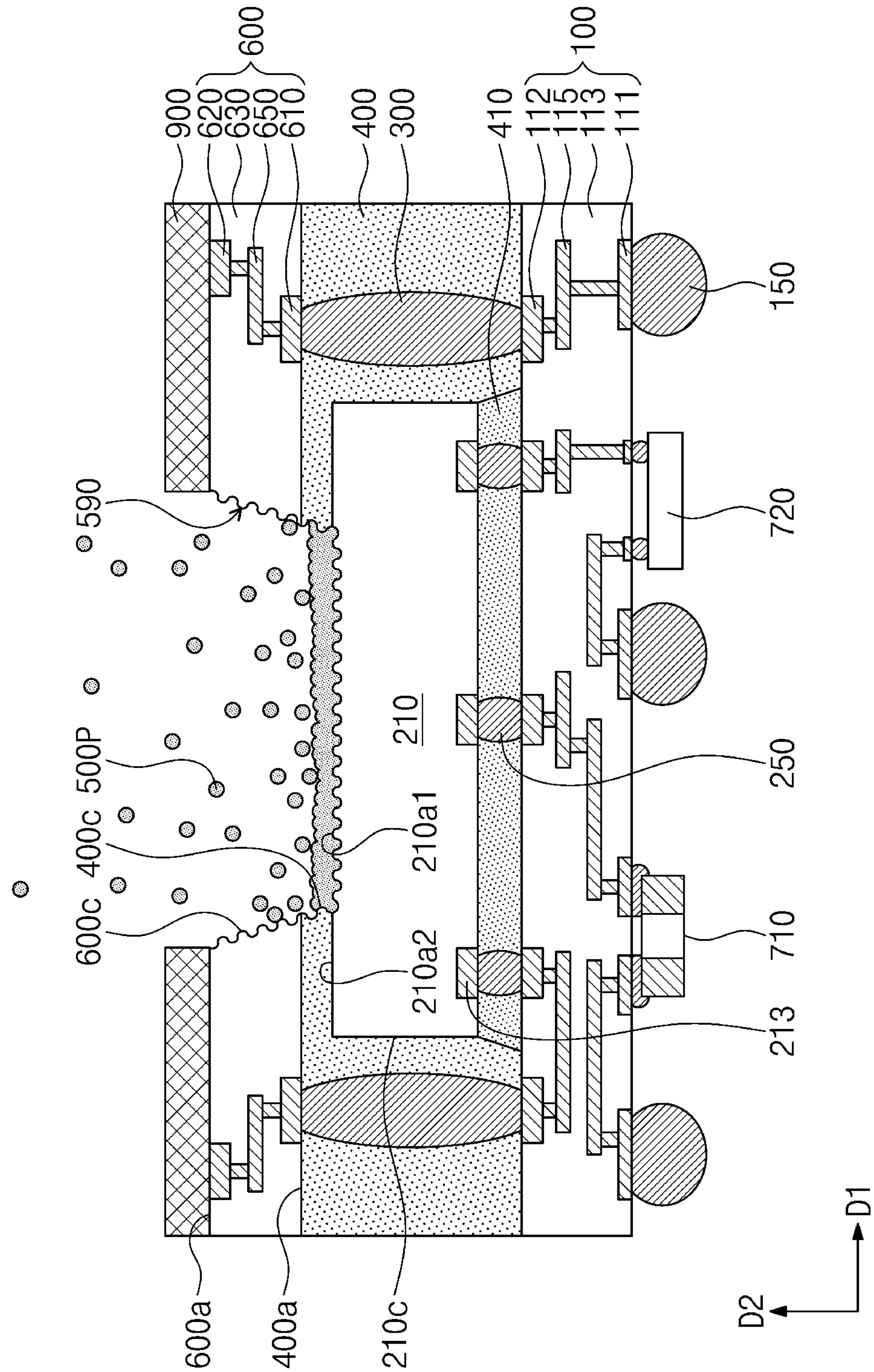
600
900
620
630
650
610
400
300
410
100
112
115
113
111
150
720
210
250
710
213
600a
400a
D1
D2

FIG. 6B



600
900
620
630
650
610
400
300
410
100
112
115
113
111
150
720
590
210
250
210a1
400c
600c
210a2
710
213
600a
400a
210c
D1
D2

FIG. 6C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900
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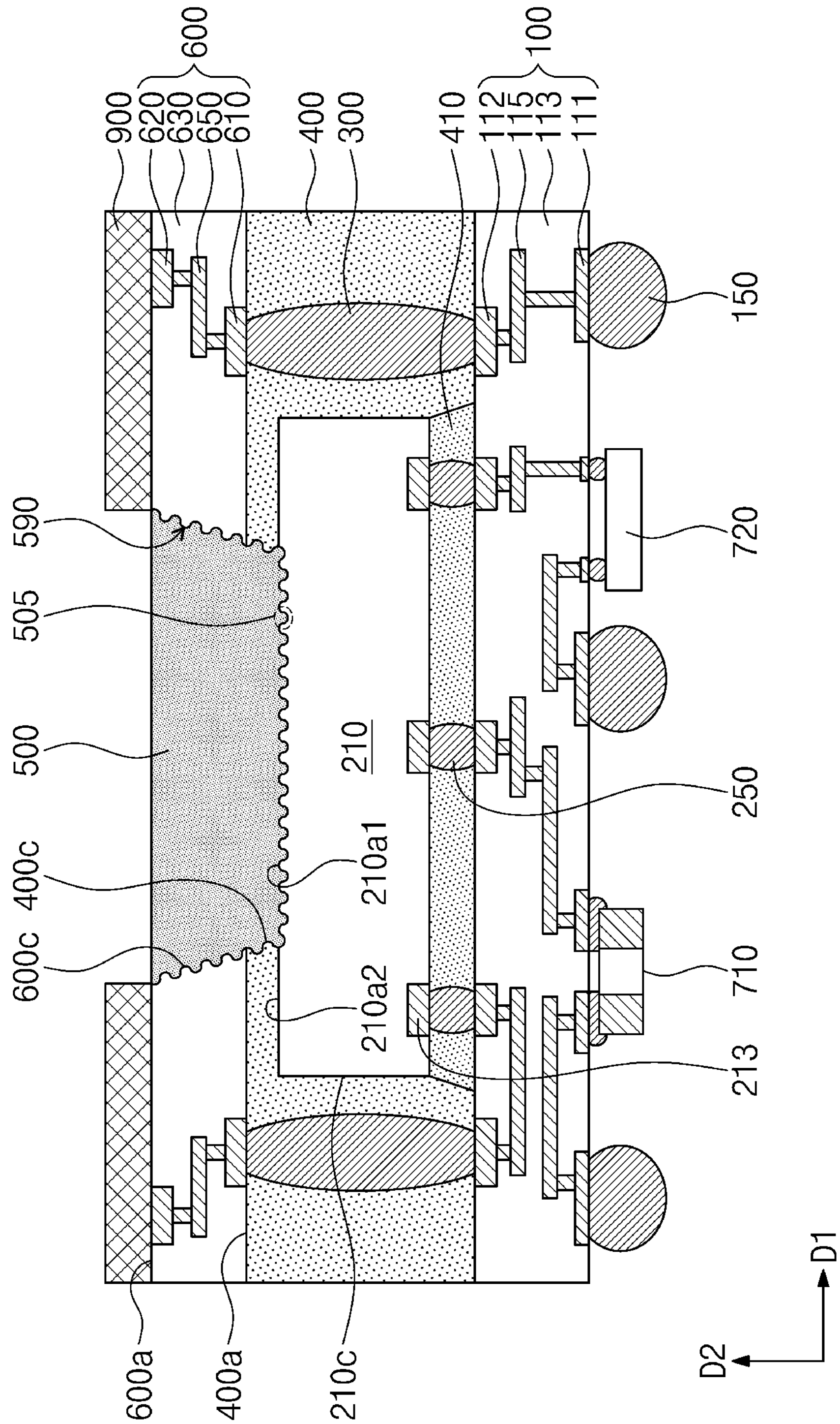
610
400
300
410
100
112
115
113
111
150
720
250
710
213
590
500P
400c
600c
210
210a1
210a2
600a
400a
210c
D1
D2

FIG. 6D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300
410
100
112
115
113
111
150
720
590
505
500
210
250
400c
210a1
600c
210a2
710
213
600a
400a
210c
D2
D1

SEMICONDUCTOR PACKAGE INCLUDING A HEAT DISSIPATION STRUCTURE

CROSS-REFERENCE TO RELATED APPLICATIONS

This U.S. non-provisional patent application claims priority under 35 U.S.C. § 119 to Korean Patent Application No. 10-2021-0165882, filed on Nov. 26, 2021, in the Korean Intellectual Property Office, the entire contents of which are hereby incorporated by reference.

TECHNICAL FIELD

The present disclosure relates to a semiconductor package, and in particular, to a semiconductor package including a heat dissipation structure.

DISCUSSION OF THE RELATED ART

Integrated circuits are generally disposed within a semiconductor package so that the integrated circuits may be protected from damage and more easily connected within electronic devices. Since the semiconductor package is formed of various materials, semiconductor packages may be prone to warping as the various materials undergo thermal expansion differently. This warpage issue may lead to a failure in a process of fabricating or using the semiconductor package. Thus, deterioration of thermal and electric characteristics of the semiconductor package may be prevented or suppressed in various environments.

SUMMARY

A semiconductor package includes a first substrate, a semiconductor chip disposed on the first substrate, a mold layer disposed on the first substrate and at least partially covering the semiconductor chip, and a heat dissipation structure disposed on a first top surface of the semiconductor chip and in the mold layer. The heat dissipation structure at least partially covers an inner side surface of the mold layer. A surface roughness of the first top surface of the semiconductor chip is greater than a surface roughness of a side surface of the semiconductor chip, and a surface roughness of the inner side surface of the mold layer is greater than a surface roughness of a top surface of the mold layer. The heat dissipation structure includes voids disposed therein.

A semiconductor package includes a first substrate, a semiconductor chip disposed on the first substrate, a conductive structure disposed on the first substrate and laterally spaced apart from the semiconductor chip, a mold layer disposed on the first substrate and covering a side surface of the conductive structure and the semiconductor chip, a second substrate disposed on the conductive structure and the mold layer, and a heat dissipation structure disposed in the mold layer and the second substrate and covering a top surface of the semiconductor chip. The heat dissipation structure include protruding portions. The protruding portions are in contact with the top surface of the semiconductor chip, an inner side surface of the mold layer, and an inner side surface of the second substrate. The heat dissipation structure includes voids disposed therein.

A semiconductor package includes a first substrate including a first insulating layer and first conductive patterns, solder balls disposed on a bottom surface of the first substrate, a semiconductor chip disposed on a top surface of the first substrate, a mold layer disposed on the top surface of the first substrate and covering the semiconductor chip, and a heat dissipation structure disposed on a top surface of the semiconductor chip and in the mold layer. A thermal conductivity of the heat dissipation structure is greater than a thermal conductivity of the mold layer, and the heat dissipation structure includes first protruding portions. The first protruding portions are in contact with the top surface of the semiconductor chip and an inner side surface of the mold layer, and the heat dissipation structure includes voids disposed therein.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete appreciation of the present disclosure and many of the attendant aspects thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:

FIG. **1**A is a cross-sectional view illustrating a semiconductor package according to an embodiment of the inventive concept;

FIG. **1**B is an enlarged cross-sectional view illustrating a portion I of FIG. **1**A;

FIG. **1**C is a diagram illustrating an enlarged structure of a portion II of FIG. **1**B;

FIG. **1**D is a diagram illustrating a heat dissipation structure according to an embodiment of the inventive concept;

FIG. **2**A is a diagram illustrating a heat dissipation structure according to an embodiment of the inventive concept;

FIG. **2**B is a diagram illustrating a heat dissipation structure according to an embodiment of the inventive concept;

FIG. **2**C is a diagram illustrating a heat dissipation structure according to an embodiment of the inventive concept;

FIG. **2**D is a diagram illustrating a heat dissipation structure according to an embodiment of the inventive concept;

FIG. **2**E is a diagram illustrating a heat dissipation structure according to an embodiment of the inventive concept;

FIG. **3**A is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept;

FIG. **3**B is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept;

FIG. **3**C is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept;

FIG. **3**D is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept;

FIG. **3**E is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept;

FIG. **3**F is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept;

FIG. **3**G is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept;

FIG. **3**H is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept;

FIG. **3**I is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept;

FIG. **3**J is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept;

FIG. **3**K is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept;

FIG. **4** is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept;

FIG. **5**A is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept;

FIG. **5**B is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept; and

FIGS. **6**A to **6**D are diagrams illustrating a semiconductor package according to an embodiment of the inventive concept.

DETAILED DESCRIPTION

Example embodiments of the inventive concepts will now be described more fully with reference to the accompanying drawings. Like reference numerals in the drawings and specification may denote like elements, and thus to the extent that a description of one or more elements has been omitted, it may be assumed that these elements are at least similar to corresponding elements that have been described elsewhere within the specification.

FIG. **1**A is a cross-sectional view illustrating a semiconductor package according to an embodiment of the inventive concept. FIG. **1**B is an enlarged cross-sectional view illustrating a portion I of FIG. **1**A.

Referring to FIGS. **1**A and **1**B, a semiconductor package **10** may include a first substrate **100**, a first semiconductor chip **210**, a mold layer **400**, and a heat dissipation structure **500**. The semiconductor package **10** may further include a conductive structure **300** and a second substrate **600**. The semiconductor package **10** may be disposed a lower semiconductor package.

The first substrate **100** may be a printed circuit board (PCB) or a re-distribution layer. The first substrate **100** may include a first insulating layer **113**, first lower pads **111**, first conductive patterns **115**, and first upper pads **112**. The first insulating layer **113** may include a plurality of layers. The first lower pads **111** and the first upper pads **112** may be disposed on a bottom surface and a top surface of the first substrate **100**, respectively. The first conductive patterns **115** may be disposed in the first substrate **100**. The first upper pads **112** may be coupled to the first lower pads **111** through the first conductive patterns **115**. The expression "two elements are electrically connected or coupled to each other" may mean that the elements are directly connected or coupled to each other or are indirectly connected or coupled to each other through other conductive elements. In the present specification, an expression "an element is electrically connected to the first substrate **100**" may mean that the element is electrically connected to the first conductive patterns **115**. The first lower pads **111**, the first conductive patterns **115**, and the first upper pads **112** may be formed of or may otherwise include a metallic material (e.g., aluminum, copper, tungsten, and/or titanium).

The semiconductor package may further include solder balls **150**. The solder balls **150** may be disposed on the bottom surface of the first substrate **100** and may be coupled to the first lower pads **111**. External electrical signals may be transmitted to the first substrate **100** through the solder balls **150**. The solder balls **150** may be formed of or may otherwise include a metallic material (e.g., solder materials). The solder material may include tin (Sn), silver (Ag), zinc (Zn), and/or alloys thereof.

The first semiconductor chip **210** may be mounted on the first substrate **100**. The first semiconductor chip **210** may be a logic chip, a memory chip, or a buffer chip. The first semiconductor chip **210** may include a semiconductor substrate, first integrated circuits, and first chip pads **213**. The semiconductor substrate may include a silicon substrate. The first integrated circuits may be disposed in the first semiconductor chip **210**. The first chip pads **213** may be disposed on a bottom surface of the first semiconductor chip **210** and may be coupled to the first integrated circuits. In the present specification, the expression "an element is electrically connected to a semiconductor chip" may mean that the element is electrically connected to integrated circuits in the semiconductor chip through chip pads. The first semiconductor chip **210** may have a first top surface **210***a***1** and a second top surface **210***a***2**.

Conductive bumps **250** may be interposed between the first substrate **100** and the first semiconductor chip **210** and may be electrically connected to the first upper pads **112** and the first chip pads **213**. The conductive bumps **250** may include solder balls and/or solder pillar. The conductive bumps **250** may be formed of or may otherwise include a conductive material (e.g., solder materials). As an example, the first semiconductor chip **210** may be mounted on the first substrate **100** by a thermo compression bonding method. In this case, the first semiconductor chip **210** may be in direct contact with the first substrate **100**, and the first chip pads **213** may be directly coupled to the first upper pads **112**, respectively.

A first under-fill layer **410** may be interposed between the first substrate **100** and the first semiconductor chip **210** to hermetically seal the conductive bumps **250**. The first under-fill layer **410** may be formed of or may otherwise include an insulating polymer.

The conductive structure **300** may be disposed on a top surface of an edge region of the first substrate **100**. The conductive structure **300** may be laterally spaced apart from the first semiconductor chip **210**. As used herein, two elements that are laterally spaced apart from each other may be horizontally spaced apart from each other. The term "horizontal" or "horizontally" will be used to refer to a direction that is substantially parallel to the top surface of the first substrate **100**. For example, a first direction D**1** may be one of such horizontal directions. The term "vertical" or "vertically" will be used to refer to a direction that is substantially perpendicular to the top surface of the first substrate **100**. For example, a second direction D**2** may be one of such vertical directions.

The conductive structure **300** may include a plurality of conductive structures **300**, which are laterally spaced apart from each other. The conductive structures **300** may be respectively disposed on and electrically connected to the first upper pads **112**. The conductive structures **300** may be electrically connected to the first semiconductor chip **210** or the solder balls **150** through the first substrate **100**. The conductive structures **300** may include solder balls, conductive pillars, or combinations thereof. The conductive structures **300** may be formed of or may otherwise include a conductive material (e.g., solder materials or metallic materials).

The mold layer **400** may be disposed on the first substrate **100** and may at least partially cover the first semiconductor chip **210**. For example, the mold layer **400** may at least partially cover a side surface **210***c* and a second top surface **210***a***2** of the first semiconductor chip **210**. The mold layer **400** may cover side surfaces of the conductive structures **300** with top surfaces of the conductive structures **300** left exposed. As an example, the under-fill layer may be omitted, and the mold layer **400** may be extended to a region under the bottom surface of the first semiconductor chip **210** and may at least partially cover the conductive bumps **250**. The mold layer **400** may be formed of or may otherwise include an insulating polymer (e.g., epoxy-based molding compound (EMC)).

The second substrate **600** may be disposed on the top surfaces of the conductive structures **300** and a top surface **400***a* of the mold layer **400**. The second substrate **600** may be electrically connected to the conductive structures **300**. The second substrate **600** may be an interposer substrate or a re-distribution layer.

The second substrate **600** may include a second insulating layer **630**, second lower pads **610**, second conductive patterns **650**, and second upper pads **620**. The second insulating layer **630** may include a plurality of layers. The second insulating layer **630** may be formed of or may otherwise include an insulating resin (e.g., solder resist materials). The second insulating layer **630** may have a relatively low thermal conductivity.

The second lower pads **610** may be disposed on a bottom surface of the second substrate **600**. The second lower pads **610** may be coupled to the conductive structures **300**, respectively. The second conductive patterns **650** may be disposed in the second insulating layer **630** and may be coupled to the second lower pads **610**. The second upper pads **620** may be disposed on a top surface **600***a* of the second substrate **600**. The second upper pads **620** may be electrically connected to the second lower pads **610** through the second conductive patterns **650**. At least one of the second upper pads **620** might not be vertically overlapped with the second lower pad **610** electrically connected thereto. The arrangement and number of the second upper pads **620** might not necessarily be limited to those of the conductive structures **300** and may be freely designed. The second lower pads **610**, the second conductive patterns **650**, and the second upper pads **620** may be formed of or may otherwise include a metallic material (e.g., copper). An electric connection with the second substrate **600** may include an electric connection with the second conductive patterns **650**.

The heat dissipation structure **500** may be disposed on the first top surface **210***a***1** of the first semiconductor chip **210** and may at least partially cover the first top surface **210***a***1** of the first semiconductor chip **210**. The second top surface **210***a***2** of the first semiconductor chip **210** may be spaced apart from the heat dissipation structure **500**. The heat dissipation structure **500** may be disposed in the first substrate **100** and the mold layer **400**. For example, the heat dissipation structure **500** may be disposed in an opening **590**. The opening **590** may be disposed to penetrate the mold layer **400** and the second substrate **600** and may expose the first top surface **210***a***1** of the first semiconductor chip **210**. The opening **590** may expose an inner side surface **400***c* of the mold layer **400** and an inner side surface **600***c* of the second substrate **600**. The inner side surface **600***c* of the second substrate **600** may expose the second insulating layer **630** but not the second conductive patterns **650**. Accordingly, the heat dissipation structure **500** may be spaced apart from the second conductive patterns **650** and might not be electrically connected to the second conductive patterns **650**.

The heat dissipation structure **500** may be in contact with the first top surface **210***a***1** of the first semiconductor chip **210**, the inner side surface **400***c* of the mold layer **400**, and the inner side surface **600***c* of the second substrate **600**. The heat dissipation structure **500** may have a plurality of first protruding portions **505**. The first protruding portions **505** may be disposed on the first top surface **210***a***1** of the first semiconductor chip **210**, the inner side surface **400***c* of the mold layer **400**, and the inner side surface **600***c* of the second substrate **600**. A surface roughness of the first top surface **210***a***1** of the first semiconductor chip **210** may be greater than a surface roughness of the side surface **210***c* of the first semiconductor chip **210**. The surface roughness of the first top surface **210***a***1** of the first semiconductor chip **210** may be greater than a surface roughness of the second top surface **210***a***2** of the first semiconductor chip **210**. As an example, the surface roughness of the first top surface **210***a***1** of the first semiconductor chip **210** may be equal to or smaller than the surface roughness of the second top surface **210***a***2** of the first semiconductor chip **210**. A surface roughness of the inner side surface **400***c* of the mold layer **400** may be greater than a surface roughness of the top surface **400***a* of the mold layer **400**. A surface roughness of the inner side surface **600***c* of the second substrate **600** may be greater than a surface roughness of the top surface **600***a* of the second substrate **600**.

A width of a top surface **500***a* of the heat dissipation structure **500** may be larger than a width of a bottom surface of the heat dissipation structure **500**. Here, the top surface **500***a* of the heat dissipation structure **500** may be externally exposed (e.g., exposed to ambient air). The top surface **500***a* of the heat dissipation structure **500** may be disposed at substantially the same level as the top surface **600***a* of the second substrate **600**. As an example, the top surface **500***a* of the heat dissipation structure **500** may be disposed at a level different from the top surface **600***a* of the second substrate **600**. The bottom surface of the heat dissipation structure **500** may be in contact with the first semiconductor chip **210**. A side surface of the heat dissipation structure **500** may be inclined at an angle with respect to the bottom surface of the heat dissipation structure **500**. For example, an angle θ between the bottom and side surfaces of the heat dissipation structure **500** may be an obtuse angle. The angle θ between the bottom and side surfaces of the heat dissipation structure **500** may be greater than 95°. For example, the angle θ between the bottom and side surfaces of the heat dissipation structure **500** may range from 95° to 120°.

The heat dissipation structure **500** may have voids **570** disposed therein. As an example, each of the voids **570** may be an empty space that is filled with the air. The voids **570** may be spaced apart from each other.

The heat dissipation structure **500** may be formed of or may otherwise include a conductive material (e.g., metallic materials). As an example, the heat dissipation structure **500** may include a silicon-containing material or silica. The heat dissipation structure **500** may be formed of or may otherwise include copper (Cu), aluminum (Al), nickel (Ni), titanium (Ti), tungsten (W), tantalum (Ta), silicon (Si), silicon carbide (SiC), oxides thereof, and/or alloys thereof. Hereinafter, the material of the heat dissipation structure **500** and the voids **570** will be described in more detail.

FIG. **1**C is a diagram illustrating a heat dissipation structure according to an embodiment of the inventive concept and in particular illustrating an enlarged structure of a portion II of FIG. **1**B.

Referring to FIG. **1**C, the heat dissipation structure **500** may include a plurality of first particles **501**. The first particles **501** may be in contact with each other and may be combined to each other. There may be no observable interface between the first particles **501**, but the inventive concept is not necessarily limited to this example. The first particles **501** may be formed of or may otherwise include the same material. For example, the first particles **501** may be formed of or may otherwise include at least one of the afore-described materials (e.g., copper (Cu), aluminum (Al), nickel (Ni), titanium (Ti), tungsten (W), tantalum (Ta), silicon (Si), silicon carbide (SiC), oxides thereof, and/or alloys thereof).

The voids **570** may be disposed between the first particles **501**. For example, each of the voids **570** may be an empty space between the first particles **501**. It is noted, however, that only some of the first particles **501** are separated from each other by the voids **570** and so others of the first particles **501** are connected to one another.

FIG. **1**D is a diagram illustrating a heat dissipation structure according to an embodiment of the inventive concept and corresponding to an enlarged structure of the portion II of FIG. **1**B.

Referring to FIG. **1**D, the heat dissipation structure **500** may include the first particles **501** and second particles **502**. The first particles **501** may have some of the same features as those in the embodiments of FIG. **1**C. For example, the first particles **501** may be in contact with each other and may be combined/connected to each other. The second particles **502** may be disposed between the first particles **501**. The second particles **502** may be formed of or may otherwise include one of the afore-enumerated materials for the first particles **501**. However, the second particles **502** may be formed of or may otherwise include a material different from the first particles **501**. The second particles **502** may be combined/connected to each other, and an interface between the second particles **502** might not be distinguished. However, the inventive concept is not necessarily limited to this example.

The heat dissipation structure **500** may further include third particles **503**. The third particles **503** may be disposed between the first particles **501**. The third particles **503** may be formed of or may otherwise include a material different from the first and second particles **501** and **502**. For example, the third particles **503** may be formed of or may otherwise include a material that is one of the afore-enumerated materials for the first particles **501** but is different from the materials of the first and second particles **501** and **502**.

The voids **570** may be disposed between the first to third particles **501**, **502**, and **503**.

The shapes and materials of the first to third particles **501**, **502**, and **503** may be variously changed. For example, the heat dissipation structure **500** may further include fourth particles, and in this case, the fourth particles may be formed of or may otherwise include a material different from the first to third particles **501**, **502**, and **503**.

Referring back to FIGS. **1**A and **1**B, the heat dissipation structure **500** may have a relatively high thermal conductivity. For example, the thermal conductivity of the heat dissipation structure **500** may be higher than that of the mold layer **400**. The thermal conductivity of the heat dissipation structure **500** may be higher than that of the second insulating layer **630**. The thermal conductivity of the heat dissipation structure **500** may be higher than that of the semiconductor substrate of the first semiconductor chip **210**. The semiconductor substrate of the first semiconductor chip **210** may be formed of or may otherwise include, for example, silicon. In an embodiment, the thermal conductivity of the heat dissipation structure **500** may range from 20 W/mK to 400 W/mK. In the case where the heat dissipation structure **500** has a thermal conductivity higher than 20 W/mK, heat, which is generated from the first semiconductor chip **210** during an operation of the semiconductor package **10**, may be quickly dissipated to the outside through the heat dissipation structure **500**. Accordingly, the first semiconductor chip **210** and the semiconductor package **10** therewith may have an increased ability to dissipate heat.

In the case where a differences between thermal expansion coefficients of the first semiconductor chip **210**, the second substrate **600**, and the mold layer **400** is excessively large, the semiconductor package may suffer a warpage issue. In an embodiment, since the heat dissipation structure **500** is used, a difference in thermal expansion coefficient between the first semiconductor chip **210**, the second substrate **600**, and the mold layer **400** may be reduced by the heat dissipation structure **500**. For example, the thermal expansion coefficient of the heat dissipation structure **500** may be smaller than or equal to 16 ppm/K. Accordingly, a propensity for the semiconductor package to warp may be reduced.

The semiconductor package **10** may further include a first passive device **710** and/or a second passive device **720**. The first passive device **710** and the second passive device **720** may be mounted on the bottom surface of the first substrate **100**. The first passive device **710** and the second passive device **720** may be laterally spaced apart from each other. Electric signals or voltages, which are input through the solder balls **150**, may be transferred to the first semiconductor chip **210** or the conductive structures **300** through the first and second passive devices **710** and **720**. The first passive device **710** and the second passive device **720** may be of different kinds. In an embodiment, the first passive device **710** and the second passive device **720** may include a capacitor, a resistor, or an inductor. As an example, the second passive device **720** may be of the same kind as the first passive device **710**.

FIG. **2**A is a diagram illustrating a heat dissipation structure according to an embodiment of the inventive concept and corresponding to an enlarged structure of the portion I of FIG. **1**A.

Referring to FIG. **2**A, the heat dissipation structure **500** may include a first heat-dissipation layer **510** and a second heat-dissipation layer **520**. The first heat-dissipation layer **510** may at least partially cover the first top surface **210*a*1** of the first semiconductor chip **210**. A bottom surface of the first heat-dissipation layer **510** may be the bottom surface of the heat dissipation structure **500**. The bottom surface of the first heat-dissipation layer **510** may have a relatively high surface roughness. For example, the surface roughness of the bottom surface of the first heat-dissipation layer **510** may be greater than the surface roughness of the side surface **210*c*** of the first semiconductor chip **210**. The first heat-dissipation layer **510** may further cover the inner side surface **400*c*** of the mold layer **400** and the inner side surface **600*c*** of the second substrate **600**. The first heat-dissipation layer **510** may include a first material. The first material may include, for example, titanium, tantalum, nickel, aluminum, or alloys thereof. For example, the first heat-dissipation layer **510** might not include copper. The first heat-dissipation layer **510** may serve as a barrier layer. For example, the first heat-dissipation layer **510** may prevent diffusion of a second material included in the second heat-dissipation layer **520**. This may make the first semiconductor chip **210** more durable. A content ratio of a mass of copper in the first heat-dissipation layer **510**, relative to a total mass of the first heat-dissipation layer **510**, may be smaller than a content ratio of a mass of copper in the second heat-dissipation layer **520**, relative to a total mass of the second heat-dissipation layer **520**. The expression "a content ratio of copper is small" may also include a case in which copper is absent.

The first heat-dissipation layer **510** may include the first particles **501** described in the embodiment of FIG. **1**C. As an example, the first heat-dissipation layer **510** may include the first to third particles **501**, **502**, and **503** described in the embodiment of FIG. **1**D.

The second heat-dissipation layer **520** may be disposed on the first heat-dissipation layer **510**. A second surface of the second heat-dissipation layer **520** may have an appreciable surface roughness. The second surface of the second heat-dissipation layer **520** may be in contact with the first heat-dissipation layer **510**. Alternatively, the second surface of the second heat-dissipation layer **520** may be flat (e.g., planar).

The second heat-dissipation layer **520** may include a second material. The second material may include copper (Cu), aluminum, nickel (Ni), titanium (Ti), tantalum, silicon (Si), silicon carbide (SiC), oxides thereof, and/or alloys thereof. However, the second material may be different from the first material. The second heat-dissipation layer **520** may include the first particles **501** described in the embodiment of FIG. **1**C or may include one or more of the first to third particles **501**, **502**, and **503** described in the embodiment of FIG. **1**D.

The voids **570** may be disposed in the first heat-dissipation layer **510** and the second heat-dissipation layer **520**. As an example, the first heat-dissipation layer **510** and/or the second heat-dissipation layer **520** might not include the voids **570**.

The heat dissipation structure **500** may include a plurality of first heat-dissipation layers **510** and a plurality of second heat-dissipation layers **520**. The first heat-dissipation layers **510** and the second heat-dissipation layers **520** may be repeatedly and alternately stacked. The numbers of the first and second heat-dissipation layers **510** and **520** in the heat dissipation structure **500** may be variously changed. As an example, the heat dissipation structure **500** may include one first heat-dissipation layer **510** and one second heat-dissipation layer **520**. For example, the heat dissipation structure **500** may have a double-layered structure.

FIG. **2**B is a diagram illustrating a heat dissipation structure, according to an embodiment of the inventive concept, and corresponding to an enlarged structure of the portion I of FIG. **1**A.

Referring to FIG. **2**B, the heat dissipation structure **500** may include the first heat-dissipation layer **510**, the second heat-dissipation layer **520**, and a third heat-dissipation layer **530**. The first heat-dissipation layer **510** and the second heat-dissipation layer **520** may be substantially the same as those in the embodiment of FIG. **2**A. The first heat-dissipation layer **510** may be configured to prevent diffusion of the second material, which is included in the second heat-dissipation layer **520**, or diffusion of a third material, which is included in the third heat-dissipation layer **530**.

The third heat-dissipation layer **530** may be disposed on the second heat-dissipation layer **520**. The third heat-dissipation layer **530** may extend to a region on the first heat-dissipation layer **510**. A top surface of the third heat-dissipation layer **530** may be exposed to external air. For example, the top surface of the third heat-dissipation layer **530** may be exposed to a region on the top surface **400***a* of the mold layer **400** or the top surface **600***a* of the second substrate **600**. The third heat-dissipation layer **530** may be a protection layer or an oxidation prevention layer. For example, the third heat-dissipation layer **530** may prevent the first heat-dissipation layer **510** or the second heat-dissipation layer **520** from being damaged (e.g., oxidized).

A content ratio of copper in the third heat-dissipation layer **530** (with respect to the entirety, by mass) may be smaller than a content ratio of copper in the second heat-dissipation layer **520** (with respect to the entirety, by mass). The expression "a content ratio of copper is small" may mean a case in which copper is absent. The third heat-dissipation layer **530** may include a third material. The third material may be different from the second material. The third material may be the same as or different from the first material included in the first heat-dissipation layer **510**. For example, the third material may include aluminum (Al), nickel (Ni), titanium (Ti), tantalum, silicon (Si), silicon carbide (SiC), oxides thereof, and/or alloys thereof. The third heat-dissipation layer **530** might not include copper. The third heat-dissipation layer **530** may include the first particles **501** described in the embodiment of FIG. **1**C or may include one or more of the first to third particles **501**, **502**, and **503** described in the embodiment of FIG. **1**D.

The heat dissipation structure **500** may further include a fourth heat-dissipation layer **540**. The fourth heat-dissipation layer **540** may be disposed between the second heat-dissipation layer **520** and the third heat-dissipation layer **530**. The third heat-dissipation layer **530** may further cover a top surface of the fourth heat-dissipation layer **540**. As an example, the fourth heat-dissipation layer **540** may be formed of or may otherwise include a fourth material that is different from the first material and the third material. The fourth material may include copper (Cu), aluminum (Al), nickel (Ni), titanium (Ti), tungsten (W), tantalum (Ta), tantalum, silicon (Si), silicon carbide (SiC), oxides thereof, and/or alloys thereof. A content ratio of copper in the fourth heat-dissipation layer **540** may be equal to or higher than a content ratio of copper in the first heat-dissipation layer **510** and a content ratio of copper in the third heat-dissipation layer **530**. The fourth heat-dissipation layer **540** may include the first particles **501** described in the embodiment of FIG. **1**C or may include one or more of the first to third particles **501**, **502**, and **503** described in the embodiment of FIG. **1**D.

The number of the stacked heat-dissipation layers (e.g., **510**, **520**, **530**, and **540**) may be variously changed. As an example the first heat-dissipation layer **510**, the second heat-dissipation layer **520**, the third heat-dissipation layer **530**, and/or the fourth heat-dissipation layer **540** may be omitted. As an example, a fifth heat-dissipation layer may be further disposed between the second heat-dissipation layer **520** and the fourth heat-dissipation layer **540**. As other example, at least two layers of the first heat-dissipation layer **510**, the second heat-dissipation layer **520**, the third heat-dissipation layer **530**, and the fourth heat-dissipation layer **540** may be repeatedly stacked.

Each of a first surface of the first heat-dissipation layer **510**, the second surface of the second heat-dissipation layer **520**, and a third surface of the third heat-dissipation layer **530** may have a specific surface roughness. The second surface of the second heat-dissipation layer **520** may be in contact with the fourth heat-dissipation layer **540**. The third surface of the third heat-dissipation layer **530** may be in contact with the fourth heat-dissipation layer **540**. The third surface of the third heat-dissipation layer **530** may be a bottom surface of the third heat-dissipation layer **530**. As an example, the first surface of the first heat-dissipation layer **510**, the second surface of the second heat-dissipation layer **520**, and/or the third surface of the third heat-dissipation layer **530** may be flat.

The voids **570** may be disposed in the first heat-dissipation layer **510**, the second heat-dissipation layer **520**, the third heat-dissipation layer **530**, and/or the fourth heat-dissipation layer **540**. As an example, the voids **570** may be disposed in the first heat-dissipation layer **510**, the second heat-dissipation layer **520**, the third heat-dissipation layer **530**, and the fourth heat-dissipation layer **540**. As an example, the first heat-dissipation layer **510**, the second heat-dissipation layer **520**, the third heat-dissipation layer **530**, and/or the fourth heat-dissipation layer **540** might not include the voids **570**.

FIG. 2C is a diagram illustrating a heat dissipation structure, according to an embodiment of the inventive concept, and corresponding to an enlarged structure of the portion I of FIG. 1A.

Referring to FIG. 2C, the heat dissipation structure **500** may include the first heat-dissipation layer **510**, the second heat-dissipation layer **520**, the third heat-dissipation layer **530**, and the fourth heat-dissipation layer **540**. The first heat-dissipation layer **510**, the second heat-dissipation layer **520**, the third heat-dissipation layer **530**, and the fourth heat-dissipation layer **540** may be substantially the same as those in the embodiment of FIG. **2**A or the embodiment of FIG. **2**B. However, the first heat-dissipation layer **510** might not be extended to the inner side surface **600***c* of the second substrate **600**. The second heat-dissipation layer **520** and the third heat-dissipation layer **530** might not be extended to an upper portion of the inner side surface **600***c* of the second substrate **600**. The shapes of the first heat-dissipation layer **510**, the second heat-dissipation layer **520**, the third heat-dissipation layer **530**, and the fourth heat-dissipation layer **540** may be variously changed.

FIG. **2**D is a diagram illustrating a heat dissipation structure according to an embodiment of the inventive concept and corresponding to an enlarged structure of the portion I of FIG. **1**A.

Referring to FIG. **2**D, the heat dissipation structure **500** may include a lower portion and an upper portion. The lower portion of the heat dissipation structure **500** may be interposed between the upper portion thereof and the first semiconductor chip **210**. The heat dissipation structure **500** may have the voids **570**. A sum of areas of the voids **570** per unit area in the upper portion of the heat dissipation structure **500** may be larger than a sum of areas of the voids **570** per unit area in the lower portion of the heat dissipation structure **500**. For example, the number of the voids **570** per unit area in the upper portion of the heat dissipation structure **500** may be greater than the number of the voids **570** per unit area in the lower portion of the heat dissipation structure **500**. A mean area of the voids **570** in the upper portion of the heat dissipation structure **500** may be larger than a mean area of the voids **570** in the lower portion of the heat dissipation structure **500**. Unlike the illustrated structure, the voids **570** may be disposed in the upper portion of the heat dissipation structure **500** but might not be disposed in the lower portion of the heat dissipation structure **500**.

FIG. **2**E is a diagram illustrating a heat dissipation structure according to an embodiment of the inventive concept and corresponding to an enlarged structure of the portion I of FIG. **1**A.

Referring to FIG. **2**E, a sum of areas of the voids **570** per unit area in the lower portion of the heat dissipation structure **500** may be larger than a sum of areas of the voids **570** per unit area in the upper portion of the heat dissipation structure **500**. For example, the number of the voids **570** per unit area in the lower portion of the heat dissipation structure **500** may be greater than the number of the voids **570** per unit area in the upper portion of the heat dissipation structure **500**. A mean area of the voids **570** in the lower portion of the heat dissipation structure **500** may be larger than a mean area of the voids **570** in the upper portion of the heat dissipation structure **500**.

Unlike the illustrated structure, the voids **570** may be disposed in the lower portion of the heat dissipation structure **500** but might not be disposed in the upper portion of the heat dissipation structure **500**.

FIG. **3**A is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept.

Referring to FIG. **3**A, the semiconductor package **10**A may include the first substrate **100**, the solder balls **150**, the first semiconductor chip **210**, the mold layer **400**, the conductive structures **300**, the second substrate **600**, and the heat dissipation structure **500**.

The opening **590** may be further extended into the first semiconductor chip **210**. For example, a bottom surface of the opening **590** may be disposed at a level that is lower than the second top surface **210***a***2** of the first semiconductor chip **210**. The uppermost portion of the first top surface **210***a***1** of the first semiconductor chip **210** may be disposed at a level that is lower than the second top surface **210***a***2**. Thus, the heat dissipation structure **500** may be further disposed in the first semiconductor chip **210**. The bottom surface of the heat dissipation structure **500** may be disposed at a level that is lower than the second top surface **210***a***2** of the first semiconductor chip **210**.

FIG. **3**B is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept.

Referring to FIG. **3**B, the semiconductor package **10**B may include the first substrate **100**, the solder balls **150**, the first semiconductor chip **210**, the mold layer **400**, the conductive structures **300**, the second substrate **600**, and the heat dissipation structure **500**. A width of the bottom surface of the heat dissipation structure **500** may be equal to or larger than a width of the first semiconductor chip **210**. The first semiconductor chip **210** may have the first top surface **210***a***1** but might not have the second top surface **210***a***2**. For example, a top surface of the first semiconductor chip **210** might not be in contact with the mold layer **400**.

FIG. **3**C is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept.

Referring to FIG. **3**C, the semiconductor package **10**C may include the first substrate **100**, the solder balls **150**, the first semiconductor chip **210**, the mold layer **400**, the conductive structures **300**, the second substrate **600**, and the heat dissipation structure **500**. The side surface of the heat dissipation structure **500** may be substantially perpendicular to the bottom surface thereof. The angle θ between the bottom and side surfaces of the heat dissipation structure **500** may be about 90°.

FIG. **3**D is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept

Referring to FIG. **3**D, the semiconductor package **10**D may include the first substrate **100**, the solder balls **150**, the first semiconductor chip **210**, the mold layer **400**, the conductive structures **300**, the second substrate **600**, and the heat dissipation structure **500**. The side surface of the heat dissipation structure **500** may be inclined at an angle with respect to the bottom surface thereof. The angle θ between the bottom and side surfaces of the heat dissipation structure **500** may be an acute angle. For example, the angle θ between the bottom and side surfaces of the heat dissipation structure **500** may be smaller than 85°.

FIG. **3**E is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept.

Referring to FIG. **3**E, the semiconductor package **10**E may include the first substrate **100**, the solder balls **150**, the first semiconductor chip **210**, the mold layer **400**, the conductive structures **300**, the second substrate **600**, and the heat dissipation structure **500**. The top surface **500***a* of the heat dissipation structure **500** may have a dome shape. The top surface **500***a* of the heat dissipation structure **500** may be upwardly convex. For example, a center region of the top surface **500***a* of the heat dissipation structure **500** may be disposed at a level that is higher than an edge region of the top surface **500***a* of the heat dissipation structure **500**. The center region of the top surface **500**_a_ of the heat dissipation structure **500** may be disposed at a level that is higher than the top surface **600**_a_ of the second substrate **600**. In a plan view, the edge region of the heat dissipation structure **500** may be disposed between the center region of the heat dissipation structure **500** and the second substrate **600**.

FIG. **3**F is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept.

Referring to FIG. **3**F, the semiconductor package **10**F may include the first substrate **100**, the solder balls **150**, the first semiconductor chip **210**, the mold layer **400**, the conductive structures **300**, the second substrate **600**, and the heat dissipation structure **500**. In an embodiment, the top surface **500**_a_ of the heat dissipation structure **500** may be concave. The center region of the top surface **500**_a_ of the heat dissipation structure **500** may be disposed at a level that is lower than the edge region of the top surface **500**_a_ of the heat dissipation structure **500**. The center region of the top surface **500**_a_ of the heat dissipation structure **500** may be disposed at a level that is lower than the top surface **600**_a_ of the second substrate **600**.

FIG. **3**G is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept.

Referring to FIG. **3**G, the semiconductor package **10**G may include the first substrate **100**, the solder balls **150**, the first semiconductor chip **210**, the mold layer **400**, the conductive structures **300**, the second substrate **600**, and the heat dissipation structure **500**.

The second substrate **600** may include the second insulating layer **630**, the second lower pads **610**, the second conductive patterns **650**, and the second upper pads **620**. The second lower pads **610** may include a lower signal pad **610**S and a lower ground pad **610**G. The lower ground pad **610**G may be spaced apart from the lower signal pad **610**S and may be electrically separated from the lower signal pad **610**S. The second conductive patterns **650** may include a signal conductive pattern **650**S and a ground conductive pattern **650**G. The ground conductive pattern **650**G may be spaced apart from the signal conductive pattern **650**S and may be electrically separated from the signal conductive pattern **650**S. The second upper pads **620** may include an upper signal pad **620**S and an upper ground pad **620**G. The upper ground pad **620**G may be spaced apart from the upper signal pad **620**S and may be electrically separated from the upper signal pad **620**S.

The upper signal pad **620**S may be electrically connected to the lower signal pad **610**S through the signal conductive pattern **650**S. The signal conductive pattern **650**S might not be exposed or extended to the opening **590**. The signal conductive pattern **650**S may be spaced apart from and electrically separated from the heat dissipation structure **500**.

The upper ground pad **620**G may be electrically connected to the lower ground pad **610**G through the ground conductive pattern **650**G. At least a portion of the ground conductive pattern **650**G may be exposed or extended to the opening **590**. For example, the ground conductive pattern **650**G may have a side surface that is exposed to the outside of the second substrate **600** near the inner side surface **600**_c_. The heat dissipation structure **500** may cover at least a portion of the ground conductive pattern **650**G. The heat dissipation structure **500** may be electrically connected to the ground conductive pattern **650**G. Accordingly, it may be possible to apply a ground voltage to the heat dissipation structure **500** during an operation of the semiconductor package **10**G. Accordingly, the heat dissipation structure **500** may serve as a shielding layer. For example, the heat dissipation structure **500** may be used to prevent an electromagnetic interference (EMI) issue associated with the first semiconductor chip **210**. The electromagnetic interference issue may mean a failure in receiving/transmitting function of an electric element caused by an electromagnetic wave emitted from or passing through another electric element. Accordingly, it may be possible to increase reliability in a process of operating the semiconductor package **10**G.

FIG. **3**H is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept.

Referring to FIG. **3**H, the semiconductor package **10**H may include the first substrate **100**, the solder balls **150**, the first semiconductor chip **210**, the mold layer **400**, the conductive structures **300**, the second substrate **600**, and the heat dissipation structure **500**. The heat dissipation structure **500** and the second substrate **600** may be substantially the same as those in the embodiment of FIG. **3**G. For example, the heat dissipation structure **500** may be in contact with the ground conductive pattern **650**G and may be electrically connected to the ground conductive pattern **650**G. Here, the ground conductive pattern **650**G may include a protruding portion that is extended into the heat dissipation structure **500**. A thickness of the ground conductive pattern **650**G in the heat dissipation structure **500** may be smaller than a thickness of the ground conductive pattern **650**G in the second insulating layer **630**. Unlike the illustrated structure, the thickness of the ground conductive pattern **650**G in the heat dissipation structure **500** may be substantially equal to the thickness of the ground conductive pattern **650**G in the second insulating layer **630**.

FIG. **3**I is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept.

Referring to FIG. **3**I, the semiconductor package **10**I may include the first substrate **100**, the solder balls **150**, the first semiconductor chip **210**, the mold layer **400**, the conductive structures **300'**, the second substrate **600**, and the heat dissipation structure **500**. The first substrate **100** may have the same or similar features as that in the embodiment of FIG. **1**A. For example, the first substrate **100** may include the first insulating layer **113**, the first conductive patterns **115**, and the first upper pads **112**. The first substrate **100** may be a re-distribution layer or a redistribution substrate. The first conductive patterns **115** may be redistribution patterns. The first substrate **100** might not include the first lower pads **111** described with reference to FIG. **1**A. In this case, the lowermost ones of the first conductive patterns **115** may serve as solder pads. For example, the solder balls **150** may be disposed on bottom surfaces of the lowermost ones of the first conductive patterns **115**. The first insulating layer **113** may be formed of or may otherwise include a photosensitive polymer.

The conductive structures **300'** may be disposed between the first substrate **100** and the second substrate **600**. In an embodiment, the conductive structures **300'** may include conductive posts or metal pillars. The conductive structures **300'** may be formed of or may otherwise include a metallic material (e.g., copper). The conductive structures **300'** may be formed of or may otherwise include a solder material.

The second substrate **600** may be disposed to have the same or similar features as that in the embodiment of FIG. **1**A. For example, the second substrate **600** may include the second insulating layer **630**, the second conductive patterns **650**, and the second upper pads **620**. The second substrate **600** may be a re-distribution layer or a redistribution substrate. The second conductive patterns **650** may be redistribution patterns. The second substrate **600** might not include the second lower pads **610** described with reference to FIG. **1**A. In this case, the lowermost ones of the second conductive patterns **650** may be in contact with the conductive structures **300'**. The second insulating layer **630** may include a photosensitive polymer.

FIG. **3**J is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept. For the sake of brevity, one of the conductive structures will be described in the following description of FIG. **3**J and it may be understood that the other conductive structures are at least similarly arranged.

Referring to FIG. **3**J, the semiconductor package **10**J may include the first substrate **100**, the solder balls **150**, the first semiconductor chip **210**, a connection substrate **350**, the mold layer **400**, the second substrate **600**, and the heat dissipation structure **500**. The first substrate **100** and the second substrate **600** may be substantially the same as those in the embodiment of FIG. **3**I.

The connection substrate **350** may be disposed on the first substrate **100**. The connection substrate **350** may have a substrate hole **390**, which vertically penetrates the same. As an example, the connection substrate **350** may be fabricated by forming the substrate hole **390** to penetrate a printed circuit board vertically (i.e., from top to bottom). The first semiconductor chip **210** may be disposed in the substrate hole **390** of the connection substrate **350**. The first semiconductor chip **210** may be spaced apart from an inner side surface of the connection substrate **350**.

The connection substrate **350** may include a base layer **330** and the conductive structure **300'**. The substrate hole **390** may penetrate the base layer **330**. Unlike the illustrated structure, the base layer **330** may include a plurality of stacked layers. The base layer **330** may include an insulating material. For example, the base layer **330** may be formed of or may otherwise include carbon-based materials, ceramic materials, and/or polymers. The conductive structure **300'** may be disposed in the base layer **330**. The connection substrate **350** may further include a first connection pad **301** and a second connection pad **302**. The first connection pad **301** may be disposed on a bottom surface of the conductive structure **300'**. The second connection pad **302** may be disposed on a top surface of the conductive structure **300'**. The second connection pad **302** may be electrically connected to the first connection pad **301** through the conductive structure **300'**. The conductive structure **300'**, the first connection pad **301**, and the second connection pad **302** may be formed of or may otherwise include, for example, copper, aluminum, tungsten, titanium, tantalum, iron, and/or alloys thereof.

A connection bump **255** may be disposed between the first substrate **100** and the connection substrate **350**. The connection bump **255** may be interposed between and coupled to the first connection pad **301** and a corresponding one of the first upper pads **112**. The conductive structure **300'** may be electrically connected to the first substrate **100** by the connection bump **255**. The connection bump **255** may include solder balls, solder bumps, and/or solder pillars. The connection bump **255** may be formed of or may otherwise include a metallic material.

A second under-fill layer **420** may be disposed in a gap between the first substrate **100** and the connection substrate **350** to hermetically seal the connection bump **255**. The second under-fill layer **420** may be formed of or may otherwise include an insulating polymer.

The mold layer **400** may be disposed on the first semiconductor chip **210** and the connection substrate **350**. The mold layer **400** may be interposed between the first semiconductor chip **210** and the connection substrate **350**. In an embodiment, the mold layer **400** may be an insulating adhesive film, which is attached to a top surface of the connection substrate **350**, the second top surface **210***a***2** of the first semiconductor chip **210**, and the side surface **210***c* of the first semiconductor chip **210**. For example, an Ajinomoto build-up film (ABF) may be used as the adhesive insulating film. As an example, the mold layer **400** may be formed of or may otherwise include an insulating polymer (e.g., epoxy-based polymer). The mold layer **400** may be formed of or may otherwise include a material different from the second under-fill layer **420**. As other example, the second under-fill layer **420** may be omitted, and the mold layer **400** may be further extended into a gap between the first substrate **100** and the connection substrate **350**.

FIG. **3**K is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept.

Referring to FIG. **3**K, the semiconductor package **10**K may include the first substrate **100**, the solder balls **150**, the first semiconductor chip **210**, a second semiconductor chip **220**, the mold layer **400**, the conductive structure **300**, the second substrate **600**, and the heat dissipation structure **500**.

The second semiconductor chip **220** may be interposed between the first substrate **100** and the first semiconductor chip **210**. The second semiconductor chip **220** may include a first top surface **220***a***1** and a second top surface **220***a***2**. The second semiconductor chip **220** may include lower conductive pads **223**, penetration vias **227**, and upper conductive pads **224**. The lower conductive pads **223** and the upper conductive pads **224** may be respectively disposed on bottom and top surfaces of the second semiconductor chip **220**. The penetration vias **227** may be disposed in the second semiconductor chip **220**. For example, the penetration vias **227** may penetrate the second semiconductor chip **220**. The upper conductive pads **224** may be electrically connected to the lower conductive pads **223** through the penetration vias **227**.

First conductive bumps **251** may be interposed between the first substrate **100** and the first semiconductor chip **210** and may be electrically connected to the first upper pads **112** and the lower conductive pads **223**. A first under-fill pattern **411** may be disposed in a gap region between the first substrate **100** and the first semiconductor chip **210** to hermetically seal the first conductive bumps **251**. The first conductive bumps **251** and the first under-fill pattern **411** may be formed of or may otherwise include the same materials as the conductive bumps **250** and the first under-fill layer **410**, respectively, described with reference to FIG. **1**A.

Second conductive bumps **252** may be interposed between the first semiconductor chip **210** and the second semiconductor chip **220** and may be electrically connected to the upper conductive pads **224** and the first chip pads **213**. A second under-fill pattern **412** may be disposed in a gap region between the first semiconductor chip **210** and the second semiconductor chip **220** to hermetically seal the second conductive bumps **252**. The second conductive bumps **252** and the second under-fill pattern **412** may be formed of or may otherwise include the same materials as the conductive bumps **250** and the first under-fill layer **410**, respectively, described with reference to FIG. **1**A.

The heat dissipation structure **500** may be disposed on the first top surface **210***a***1** of the first semiconductor chip **210** and in the opening **590**. The heat dissipation structure **500** may at least partially cover the inner side surface **600***c* of the second substrate **600** and the inner side surface **400***c* of the mold layer **400**. The heat dissipation structure **500** may further penetrate the mold layer **400** and may at least partially cover the first top surface **220**a**1** of the second semiconductor chip **220**. The heat dissipation structure **500** may be spaced apart from the second top surface **220**a**2** of the second semiconductor chip **220**. The first top surface **220**a**1** of the second semiconductor chip **220** may have a surface roughness that is greater than a side surface **220**c of the second semiconductor chip **220**. The first top surface **220**a**1** of the second semiconductor chip **220** may have a surface roughness that is greater than the second top surface **220**a**2** of the second semiconductor chip **220**. As an example, the first top surface **220**a**1** of the second semiconductor chip **220** may have a surface roughness that is equal to or smaller than the second top surface **220**a**2** of the second semiconductor chip **220**. The heat dissipation structure **500** may include the first protruding portions **505**, and the first protruding portions **505** may be further disposed on the first top surface **220**a**1** of the second semiconductor chip **220**.

The heat dissipation structure **500** may be interposed between the side surface **210**c of the first semiconductor chip **210** and the conductive structure **300**. The heat dissipation structure **500** may be laterally spaced apart from the conductive structure **300**.

FIG. **4** is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept.

Referring to FIG. **4**, a semiconductor package **11** may include the first substrate **100**, the solder balls **150**, the first semiconductor chip **210**, the second semiconductor chip **220**, the mold layer **400**, and the heat dissipation structure **500**. The semiconductor package **11** might not include the second substrate **600** and the conductive structure **300** described in the embodiment of FIG. **1**A. The top surface **500**a of the heat dissipation structure **500** may be disposed at a level that is equal to or different from the top surface **400**a of the mold layer **400**.

The afore-described embodiments may be combined to each other to realize the inventive concept. For example, at least two of the embodiments for the semiconductor package **10** of FIG. **1**A, the semiconductor package **10**A of FIG. **3**A, the semiconductor package **10**B of FIG. **3**B, the semiconductor package **10**C of FIG. **3**C, the semiconductor package **10**D of FIG. **3**D, the semiconductor package **10**E of FIG. **3**E, the semiconductor package **10**F of FIG. **3**F, the semiconductor package **10**G of FIG. **3**G, the semiconductor package **10**H of FIG. **3**H, the semiconductor package **10**I of FIG. **3**I, the semiconductor package **10**J of FIG. **3**J, the semiconductor package **10**K of FIG. **3**K, and the semiconductor package **11** of FIG. **4** may be combined to each other. As an example, the semiconductor package **10** of FIG. **1**A, the semiconductor package **10**A of FIG. **3**A, the semiconductor package **10**B of FIG. **3**B, the semiconductor package **10**C of FIG. **3**C, the semiconductor package **10**D of FIG. **3**D, the semiconductor package **10**E of FIG. **3**E, the semiconductor package **10**F of FIG. **3**F, the semiconductor package **10**G of FIG. **3**G, the semiconductor package **10**H of FIG. **3**H, the semiconductor package **10**I of FIG. **3**I, the semiconductor package **10**J of FIG. **3**J, or the semiconductor package **10**K of FIG. **3**K might not include the second substrate **600** and the conductive structure **300**, as in the semiconductor package **11** in the embodiment of FIG. **4**.

FIG. **5**A is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept.

Referring to FIG. **5**A, a semiconductor package **12** may include a lower semiconductor package **10'** and an upper semiconductor package **20**. The lower semiconductor package **10'** may be substantially the same as the semiconductor package **10** described in the embodiment of FIG. **1**A. For example, the lower semiconductor package **10'** may include the first substrate **100**, the solder balls **150**, the first semiconductor chip **210**, the conductive structure **300**, the mold layer **400**, the second substrate **600**, and the heat dissipation structure **500**. The lower semiconductor package **10'** may further include the first and second passive devices **710** and **720**, the conductive bumps **250**, and the first under-fill layer **410**. As an example, the lower semiconductor package **10'** may be substantially the same as the semiconductor package **10**A of FIG. **3**A, the semiconductor package **10**B of FIG. **3**B, the semiconductor package **10**C of FIG. **3**C, the semiconductor package **10**D of FIG. **3**D, the semiconductor package **10**E of FIG. **3**E, the semiconductor package **10**F of FIG. **3**F, the semiconductor package **10**G of FIG. **3**G, the semiconductor package **10**H of FIG. **3**H, the semiconductor package **10**I of FIG. **3**I, the semiconductor package **10**J of FIG. **3**J, or the semiconductor package **10**K of FIG. **3**K.

The upper semiconductor package **20** may be disposed on the lower semiconductor package **10'**. The upper semiconductor package **20** may include an upper substrate **700**, an upper semiconductor chip **721**, and an upper mold layer **740**. The upper substrate **700** may be disposed on the top surface **600**a of the second substrate **600** and may be spaced apart from the top surface **600**a of the second substrate **600**. The upper substrate **700** may be a printed circuit board (PCB) or a re-distribution layer. The upper substrate **700** may include first substrate pads **711**, second substrate pads **712**, and metal lines **715**. The first and second substrate pads **711** and **712** may be respectively disposed on bottom and top surfaces of the upper substrate **700**. The metal lines **715** may be disposed in the upper substrate **700** and may be coupled to the first and second substrate pads **711** and **712**.

The upper semiconductor chip **721** may be mounted on the top surface of the upper substrate **700**. The upper semiconductor chip **721** may include upper chip pads **723** and second integrated circuits. The second integrated circuits may be disposed in the upper semiconductor chip **721**. The upper chip pads **723** may be disposed on the top surface of the upper semiconductor chip **721** and may be coupled to the second integrated circuits. The upper chip pads **723** may be formed of or may otherwise include, for example, a metallic material. The upper semiconductor chip **721** may be a semiconductor chip that is of a different kind from the first semiconductor chip **210**. For example, the first semiconductor chip **210** may be a logic chip, and the upper semiconductor chip **721** may be a memory chip.

The upper semiconductor package **20** may further include bonding wires **750**. The bonding wires **750** may be disposed on the top surface of the upper semiconductor chip **721** and may be coupled to the second substrate pads **712** and the upper chip pads **723**. The bonding wires **750** may be formed of or may otherwise include, for example, a metallic material.

The upper semiconductor package **20** may include a plurality of upper semiconductor chips **721**. The upper semiconductor chips **721** may be laterally spaced apart from each other.

The upper mold layer **740** may be disposed on the upper substrate **700** and may at least partially cover top and side surfaces of the upper semiconductor chips **721**. In an embodiment, the upper mold layer **740** may also at least partially cover the bonding wires **750**. The upper mold layer **740** may be formed of or may otherwise include an insulating polymer (e.g., epoxy-based molding compound).

The upper semiconductor package **20** may further include connection solder balls **670**. The connection solder balls **670** may be disposed between the second substrate **600** and the upper substrate **700**. For example, the connection solder balls **670** may be disposed between the second upper pads **620** and the first substrate pads **711** and may be coupled to the second upper pads **620** and the first substrate pads **711**. Thus, the upper semiconductor chip **721** may be electrically connected to the first semiconductor chip **210** or the solder balls **150** through the connection solder balls **670**.

FIG. **5**B is a diagram illustrating a semiconductor package according to an embodiment of the inventive concept.

Referring to FIG. **5**B, a semiconductor package **13** may include the lower semiconductor package **10'**, an upper semiconductor package **20'**, and the connection solder balls **670**. The lower semiconductor package **10'**, the upper semiconductor package **20'**, and the connection solder balls **670** may be substantially the same as those in the lower semiconductor package **10'**, the upper semiconductor package **20**, and the connection solder balls **670** in the embodiment of FIG. **5**A.

However, the upper semiconductor package **20'** may further include an upper heat dissipation structure **550**. The upper heat dissipation structure **550** may be disposed on a first top surfaces **721**a**1** of the upper semiconductor chips **721** and in the upper mold layer **740**. The upper heat dissipation structure **550** may be disposed in an upper opening **559**. The upper opening **559** may penetrate a top surface of the upper mold layer **740** and may expose the first top surfaces **721**a**1** of the upper semiconductor chips **721** and an inner bottom surface **740**b of the upper mold layer **740**. The inner bottom surface **740**b of the upper mold layer **740** may be disposed at the same or similar level as the first top surfaces **721**a**1** of the upper semiconductor chips **721**. The upper heat dissipation structure **550** might not cover second top surfaces **721**a**2** of the upper semiconductor chips **721**. The upper mold layer **740** may at least partially cover the second top surfaces **721**a**2** of the upper semiconductor chips **721**. The upper heat dissipation structure **550** may be similar to the heat dissipation structure **500** of FIG. **1**A or the heat dissipation structure **500** of FIG. **4**. For example, the upper heat dissipation structure **550** may include a plurality of second protruding portions **555**, and the second protruding portions **555** may be disposed on the first top surfaces **721**a**1** of the upper semiconductor chips **721**, inner side surfaces **740**c of the upper mold layer **740**, and the inner bottom surface **740**b of the upper mold layer **740**. A surface roughness of the first top surfaces **721**a**1** of the upper semiconductor chips **721** may be greater than a surface roughness of the side surfaces of the upper semiconductor chips **721**. A surface roughness of the inner side surfaces **740**c of the upper mold layer **740** and a surface roughness of the inner bottom surface **740**b of the upper mold layer **740** may be greater than a surface roughness of the top surface of the upper mold layer **740**. The upper mold layer **740** may at least partially cover the second top surfaces **721**a**2** of the upper semiconductor chips **721**.

The upper heat dissipation structure **550** may further include voids disposed therein. The voids in the upper heat dissipation structure **550** may be substantially the same as the voids **570** of FIG. **1**B, the voids **570** of FIG. **1**C, the voids **570** of FIG. **1**D, the voids **570** of FIG. **2**D, or the voids **570** of FIG. **2**E.

Since the upper semiconductor package **20'** includes the upper heat dissipation structure **550**, heat, which is generated by the upper semiconductor chips **721** during an operation of the upper semiconductor package **20'**, may be more quickly dissipated to the outside. Accordingly, it may be possible to increase thermal dissipation and operational characteristics of the upper semiconductor package **20'**.

FIGS. **6**A to **6**D are diagrams illustrating a semiconductor package according to an embodiment of the inventive concept.

Referring to FIG. **6**A, the first semiconductor chip **210**, the conductive structure **300**, the mold layer **400**, and the second substrate **600** may be formed on the top surface of the first substrate **100**. The conductive bumps **250** and the first under-fill layer **410** may be formed between the first substrate **100** and the first semiconductor chip **210**. The second substrate **600** may be formed on the mold layer **400** and may at least partially cover the top surface **400**a of the mold layer **400**. A mask pattern **900** may be formed on the top surface **600**a of the second substrate **600**. The mask pattern **900** may be formed of or may otherwise include a metallic material (e.g., stainless steel). The mask pattern **900** may have a guide opening. The guide opening may expose the top surface **600**a of the second substrate **600**. The guide opening may be overlapped with the first semiconductor chip **210**, in a plan view. The first and second passive devices **710** and **720** and the solder balls **150** may be formed on the bottom surface of the first substrate **100**.

Referring to FIG. **6**B, the opening **590** may be formed in the second substrate **600** and the mold layer **400** and may expose the semiconductor chip. The formation of the opening **590** may include removing the second substrate **600** and the mold layer **400**, which are exposed by the mask pattern **900**. The removal of the second substrate **600** and the mold layer **400** may be performed by a blast process. For example, the blast process may be a sand blast process. In an embodiment, polishing particles (e.g., silica, metal, glass, and/or glass) may be disposed on the second substrate **600** exposed through the opening **590**. The polishing particles may collide with the second substrate **600** and the mold layer **400**, and in this case, the second substrate **600** and the mold layer **400** may be partially removed by the collision of the polishing particles. Thus, the opening **590** may be formed. The opening **590** may expose the first top surface **210**a**1** of the first semiconductor chip **210**, the inner side surface **600**c of the second substrate **600**, and the inner side surface **400**c of the mold layer **400**. After the blast process is finished, the surface roughness of the first top surface **210**a**1** of the first semiconductor chip **210** may be greater than the surface roughness of the side surface **210**c of the first semiconductor chip **210**. The surface roughness of the inner side surface **400**c of the mold layer **400** may be greater than the surface roughness of the top surface **400**a of the mold layer **400**. The surface roughness of the inner side surface **600**c of the second substrate **600** may be greater than the surface roughness of the top surface **600**a of the second substrate **600**.

Referring to FIGS. **6**C and **6**D, preliminary particles **500**P may be sprayed into the opening **590**. The spraying of the preliminary particles **500**P may be performed by a cold spraying process. The preliminary particles **500**P may be a solid powder. The preliminary particles **500**P may be formed of or may otherwise include copper (Cu), aluminum (Al), nickel (Ni), titanium (Ti), tungsten (W), tantalum (Ta), and/or silicon carbide (SiC). The preliminary particles **500**P may be formed of or may otherwise include the same material or different materials. As a result of the spraying of the preliminary particles **500**P, the heat dissipation structure **500** may be formed. The preliminary particles **500**P may collide with the first top surface **210**a**1** of the first semiconductor chip **210**, the inner side surface **600**c of the second substrate **600**, and the inner side surface **400**c of the mold layer **400** at a relatively fast speed. In this case, as shown in FIG. **6**D, the heat dissipation structure **500** may have the first protruding portions **505**, which are formed on the first top surface **210***a***1** of the first semiconductor chip **210**, the inner side surface **600***c* of the second substrate **600**, and the inner side surface **400***c* of the mold layer **400**. The surface roughness of the first top surface **210***a***1** of the first semiconductor chip **210**, the surface roughness of the inner side surface **400***c* of the mold layer **400**, and the surface roughness of the inner side surface **600***c* of the second substrate **600** after the formation of the heat dissipation structure **500** may be different from those before the formation of the heat dissipation structure **500**. The surface roughness of the first top surface **210***a***1** of the first semiconductor chip **210**, the surface roughness of the inner side surface **400***c* of the mold layer **400**, and the surface roughness of the inner side surface **600***c* of the second substrate **600** after the formation of the heat dissipation structure **500** may be greater than the surface roughness of the side surface **210***c* of the first semiconductor chip **210**, the surface roughness of the top surface **400***a* of the mold layer **400**, and the surface roughness of the top surface **600***a* of the second substrate **600**, respectively.

After a spray coating process is finished, an annealing process may be further performed on the heat dissipation structure **500**. The annealing process may include thermally treating the heat dissipation structure **500**. As a result of the annealing process, the preliminary particles **500**P may be combined to each other. Accordingly, the preliminary particles **500**P may form the first particles **501** described with reference to FIG. **1**C or the first to third particles **501**, **502**, and **503** described with reference to FIG. **1**D. There may be no observable interface between the first particles **501** or between the first to third particles **501**, **502**, and **503**. The heat dissipation structure **500** may have the voids **570** described with reference to the embodiments of FIGS. **1**C and **1**D. Each of the voids **570** may be an empty space that is disposed between the first particles **501** or between the first to third particles **501**, **502**, and **503**.

Referring back to FIG. **1**A, the mask pattern **900** may be removed to expose the top surface **600***a* of the second substrate **600**. A semiconductor package, according to an embodiment of the inventive concept, may be fabricated through the afore-described process.

According to an embodiment of the inventive concept, a semiconductor package may include a heat dissipation structure. Accordingly, it may be possible to increase thermal dissipation and operational reliability of the semiconductor package. It may be possible to prevent a warpage issue in the semiconductor package.

While example embodiments of the inventive concept have been particularly shown and described, it will be understood by one of ordinary skill in the art that variations in form and detail may be made therein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A semiconductor package, comprising:

a first substrate;

a semiconductor chip disposed on the first substrate;

a mold layer disposed on the first substrate and covering the semiconductor chip; and

a heat dissipation structure disposed on a first top surface of the semiconductor chip and also disposed in the mold layer, the heat dissipation structure at least partially covering an inner side surface of the mold layer,

wherein a surface roughness of the first top surface of the semiconductor chip is greater than a surface roughness of a side surface of the semiconductor chip,

wherein a surface roughness of the inner side surface of the mold layer is greater than a surface roughness of a top surface of the mold layer, and

wherein the heat dissipation structure includes voids disposed therein.

2. The semiconductor package of claim **1**, wherein the heat dissipation structure comprises protruding portions, and

wherein the protruding portions are disposed on both the first top surface of the semiconductor chip and the inner side surface of the mold layer.

3. The semiconductor package of claim **1**, wherein the heat dissipation structure comprises particles that are connected to one another, and

wherein the voids are disposed between the particles.

4. The semiconductor package of claim **1**, wherein a side surface of the heat dissipation structure is inclined at an angle with respect to a bottom surface thereof.

5. The semiconductor package of claim **1**, wherein the heat dissipation structure comprises:

a first heat-dissipation layer at least partially covering the first top surface of the semiconductor chip;

a second heat-dissipation layer disposed on the first heat-dissipation layer; and

a third heat-dissipation layer disposed on the second heat-dissipation layer and exposed to a region on the top surface of the mold layer,

wherein a ratio of a mass of copper in the first heat-dissipation layer, relative to a total mass of the first heat-dissipation layer, and a ratio of a mass of copper in the third heat-dissipation layer, relative to a total mass of the third heat-dissipation layer, are each smaller than a ratio of a mass of copper in the second heat-dissipation layer, relative to a total mass of the second heat-dissipation layer.

6. The semiconductor package of claim **5**, wherein the voids are disposed in each of the first heat-dissipation layer, the second heat-dissipation layer, and the third heat-dissipation layer.

7. The semiconductor package of claim **1**, wherein a sum of areas of the voids, per unit area, in a lower portion of the heat dissipation structure is different than a sum of areas of the voids, per unit area, in an upper portion of the heat dissipation structure.

8. The semiconductor package of claim **1**, further comprising a second substrate disposed on the top surface of the mold layer,

wherein the heat dissipation structure penetrates the second substrate and is in contact with an inner side surface of the second substrate, and

wherein a surface roughness of the inner side surface of the second substrate is greater than a surface roughness of a top surface of the second substrate.

9. The semiconductor package of claim **8**, wherein the second substrate comprises an insulating layer and a ground conductive pattern disposed in the insulating layer, and

wherein the ground conductive pattern is exposed to an outside of the second substrate through the inner side surface of the second substrate and is in contact with the heat dissipation structure.

10. The semiconductor package of claim **1**, wherein the semiconductor chip further comprises a second top surface,

wherein the heat dissipation structure is spaced apart from the second top surface of the semiconductor chip, and

wherein the surface roughness of the first top surface of the semiconductor chip is greater than a surface roughness of the second top surface.

11. A semiconductor package, comprising:
a first substrate;
a semiconductor chip disposed on the first substrate;
a conductive structure disposed on the first substrate, the conductive structure being laterally spaced apart from the semiconductor chip;
a mold layer disposed on the first substrate and at least partially covering the semiconductor chip and a side surface of the conductive structure;
a second substrate disposed on both the conductive structure and the mold layer; and
a heat dissipation structure disposed in both the mold layer and the second substrate and covering a top surface of the semiconductor chip,
wherein the heat dissipation structure comprises protruding portions,
wherein the protruding portions are in contact with the top surface of the semiconductor chip, an inner side surface of the mold layer, and an inner side surface of the second substrate, and
wherein the heat dissipation structure includes voids disposed therein.

12. The semiconductor package of claim **11**, wherein a surface roughness of the top surface of the semiconductor chip is greater than a surface roughness of a side surface of the semiconductor chip,
wherein a surface roughness of the inner side surface of the mold layer is greater than a surface roughness of a top surface of the mold layer, and
wherein a surface roughness of the inner side surface of the second substrate is greater than a surface roughness of a top surface of the second substrate.

13. The semiconductor package of claim **11**, wherein the second substrate further comprises:
signal conductive patterns spaced apart from the heat dissipation structure; and
a ground conductive pattern, that is electrically insulated from the signal conductive pattern and is exposed to an outside of the second substrate through the inner side surface of the second substrate,
wherein the heat dissipation structure is electrically connected to the ground conductive pattern.

14. The semiconductor package of claim **11**, wherein an angle between bottom and side surfaces of the heat dissipation structure is an obtuse angle.

15. The semiconductor package of claim **11**, wherein the second substrate comprises a re-distribution layer or an interposer substrate.

16. A semiconductor package, comprising:
first substrate including a first insulating layer and first conductive patterns;
solder balls disposed on a bottom surface of the first substrate;
a semiconductor chip disposed on a top surface of the first substrate;
a mold layer disposed on the top surface of the first substrate and covering the semiconductor chip; and
a heat dissipation structure disposed on a top surface of the semiconductor chip and in the mold layer,
wherein a thermal conductivity of the heat dissipation structure is greater than a thermal conductivity of the mold layer,
wherein the heat dissipation structure comprises first protruding portions,
wherein the first protruding portions are in contact with both the top surface of the semiconductor chip and an inner side surface of the mold layer, and
wherein the heat dissipation structure includes voids disposed therein.

17. The semiconductor package of claim **16**, further comprising:
a conductive structure disposed on the first substrate and laterally spaced apart from the semiconductor chip; and
a second substrate disposed on both a top surface of the conductive structure and a top surface of the mold layer,
wherein the heat dissipation structure extends into the second substrate and is in contact with an inner side surface of the second substrate, and
wherein a surface roughness of the inner side surface of the second substrate is greater than a surface roughness of a top surface of the second substrate.

18. The semiconductor package of claim **17**, further comprising an upper package mounted on the top surface of the second substrate,
wherein the upper package comprises an upper substrate, an upper semiconductor chip, an upper mold layer, and an upper heat dissipation structure,
wherein the upper heat dissipation structure is disposed on both a top surface of the upper semiconductor chip and in the upper mold layer,
wherein the upper heat dissipation structure comprises second protruding portions, and
wherein the second protruding portions are disposed on both the top surface of the upper semiconductor chip and an inner side surface of the upper mold layer.

19. The semiconductor package of claim **16**, wherein the thermal conductivity of the heat dissipation structure ranges from 20 W/mK to 400 W/mK.

20. The semiconductor package of claim **16**, wherein the heat dissipation structure comprises particles that are connected to each other,
wherein the voids are disposed between the particles, and
wherein the particles comprise copper (Cu), aluminum (Al), nickel (Ni), titanium (Ti), tungsten (W), tantalum (Ta), silicon (Si), silicon carbide (SiC), oxides thereof, and/or alloys thereof.

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