United States Patent Application Publication	20250266365
Kind Code	A1
Publication Date	August 21, 2025
Inventor(s)	Yeh; Shu-Shen et al.

ECCENTRIC VIA STRUCTURES FOR STRESS REDUCTION

Abstract

A method includes forming a first dielectric layer, forming a first redistribution line including a first via extending into the first dielectric layer, and a first trace over the first dielectric layer, forming a second dielectric layer covering the first redistribution line, and patterning the second dielectric layer to form a via opening. The first redistribution line is revealed through the via opening. The method further includes depositing a conductive material into the via opening to form a second via in the second dielectric layer, and a conductive pad over and contacting the second via, and forming a conductive bump over the conductive pad. The conductive pad is larger than the conductive bump, and the second via is offset from a center line of the conductive bump.

Inventors: **Yeh; Shu-Shen (Taoyuan City, TW), Yang; Che-Chia (Taipei City, TW), Hsu; Chia-Kuei (Hsinchu, TW), Lin; Po-Yao (Zhudong Township, TW), Jeng; Shin-Puu (Hsinchu, TW), Lin; Chia-Hsiang (Zhubei City, TW)**

Applicant: **Taiwan Semiconductor Manufacturing Co., Ltd.** (Hsinchu, TW)

Family ID: **1000008576825**

Appl. No.: **19/197500**

Filed: **May 02, 2025**

Related U.S. Application Data

parent US continuation 18766974 20240709 parent-grant-document US 12322703 child US 19197500
parent US continuation 17126881 20201218 parent-grant-document US 12094828 child US 18766974
us-provisional-application US 63053317 20200717

Publication Classification

Int. Cl.: **H01L23/538** (20060101); **H01L21/48** (20060101); **H01L21/768** (20060101); **H01L23/00** (20060101)

U.S. Cl.:

CPC **H01L23/5384** (20130101); **H01L21/4853** (20130101); **H01L21/486** (20130101); **H01L21/76802** (20130101); **H01L23/5385** (20130101); **H01L23/5386** (20130101); **H01L24/14** (20130101);

Background/Summary

PRIORITY CLAIM AND CROSS-REFERENCE [0001] This application is a continuation of U.S. patent application Ser. No. 18/766,974, entitled “Eccentric via structures for Stress reduction,” filed Jul. 9, 2024, which is a continuation of U.S. patent application Ser. No. 17/126,881, entitled “Eccentric via structures for Stress reduction,” filed Dec. 18, 2020, now U.S. Pat. No. 12,094,828, issued on Sep. 17, 2024, which claims the benefit of U.S. Provisional Application No. 63/053,317, filed Jul. 17, 2020, and entitled “A Novel Eccentric Structure of Stacking Via for Stress Reduction on Fan-out Structure,” which applications are hereby incorporated herein by reference.

BACKGROUND
[0002] With the evolving of semiconductor technologies, semiconductor chips/dies are becoming increasingly smaller. In the meantime, more functions need to be integrated into the semiconductor dies. Accordingly, the semiconductor dies need to have increasingly greater numbers of I/O pads packed into smaller areas, and the density of the I/O pads rises quickly over time. As a result, the packaging of the semiconductor dies becomes more difficult, which adversely affects the yield of the packaging.
[0003] A typical bonding structure may include an Under-Bump-Metallurgy (UBM), which is a metal pad, and a metal pillar on the UBM. A solder region may be used for bonding the metal pillar to another electrical connector of another package component.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0004] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.
[0005] FIGS. **1** through **12** illustrate the cross-sectional views of intermediate stages in the formation of an interconnect component including eccentric bonding structures in accordance with some embodiments.
[0006] FIG. **13** illustrates a package including eccentric bonding structures in accordance with some embodiments.
[0007] FIG. **14** illustrates the cross-sectional view of an eccentric bonding structure in accordance with some embodiments.
[0008] FIG. **15** illustrates the top view of an eccentric bonding structure in accordance with some embodiments.
[0009] FIG. **16** illustrates the cross-sectional view of an eccentric bonding structure in accordance with some embodiments.
[0010] FIG. **17** illustrates the top view of an eccentric bonding structure in accordance with some

embodiments.
[0011] FIGS. **18** and **19** illustrate the structures that are simulated in accordance with some embodiments.
[0012] FIG. **20** illustrates a process flow for forming an interconnect component including eccentric bonding structures in accordance with some embodiments.
DETAILED DESCRIPTION
[0013] The following disclosure provides many different embodiments, or examples, for implementing different features of the invention. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.
[0014] Further, spatially relative terms, such as “underlying,” “below,” “lower,” “overlying,” “upper” and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.
[0015] A package including eccentric bonding structures and the method of forming the same are provided. In accordance with some embodiments of the present disclosure, a conductive bump (which may be a metal pillar) is formed, and a conductive pad is formed underneath the conductive bump, with the conductive pad being larger than the conductive bump. A first via is underlying and joined to the conductive pad. The first via is vertically offset from the center of the overlying conductive bump. A plurality of second vias, which are underlying and electrically connected to the first via, are also offset from the first via. The offsets may prevent the vias and the pads that have high Coefficient of Thermal Extension (CTE) values from being vertically aligned, and hence may reduce the stress. Embodiments discussed herein are to provide examples to enable making or using the subject matter of this disclosure, and a person having ordinary skill in the art will readily understand modifications that can be made while remaining within contemplated scopes of different embodiments. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements. Although method embodiments may be discussed as being performed in a particular order, other method embodiments may be performed in any logical order.
[0016] FIGS. **1** through **12** illustrate the cross-sectional views of intermediate stages in the formation of an interconnect component including eccentric bonding structures in accordance with some embodiments of the present disclosure. The corresponding processes are also reflected schematically in the process flow shown in FIG. **20**. It is appreciated that although the interconnect component including the eccentric bonding structures are formed starting from a carrier, it may also be formed starting from other components such as a fan-out interconnect structure of device dies, a part of a device die or an interposer, etc.
[0017] FIG. **1** illustrates carrier **20** and release film **22** formed on carrier **20**. Carrier **20** may be a glass carrier, a silicon wafer, an organic carrier, or the like. Carrier **20** may have a round top-view shape in accordance with some embodiments. Release film **22** may be formed of a polymer-based material (such as a Light-To-Heat-Conversion (LTHC) material), which is capable of being

decomposed under radiation such as a laser beam, so that carrier **20** may be de-bonded from the overlying structures that will be formed in subsequent processes. In accordance with some embodiments of the present disclosure, release film **22** is formed of an epoxy-based thermal-release material, which is coated onto carrier **20**.

[0018] A plurality of dielectric layers and a plurality of RDLs are formed over the release film **22**, as shown in FIGS. **1** through **4**. The respective process is illustrated as process **202** in the process flow **200** as shown in FIG. **20**. Referring to FIG. **1**, dielectric layer **24** is first formed on release film **22**. In accordance with some embodiments of the present disclosure, dielectric layer **24** is formed of a polymer, which may also be a photo-sensitive material such as polybenzoxazole (PBO), polyimide, benzocyclobutene (BCB), or the like, that may be easily patterned using a photo lithography process.

[0019] Redistribution Lines (RDLs) **26** are formed over dielectric layer **24** in accordance with some embodiments. The formation of RDLs **26** may include forming a seed layer (not shown) over dielectric layer **24**, forming a patterned mask (not shown) such as a photo resist over the seed layer, and then performing a metal plating process on the exposed seed layer. The patterned mask and the portions of the seed layer covered by the patterned mask are then removed, leaving RDLs **26** as in FIG. **1**. In accordance with some embodiments of the present disclosure, the seed layer includes a titanium layer and a copper layer over the titanium layer. The seed layer may be formed using, for example, Physical Vapor Deposition (PVD) or a like process. The plating may be performed using, for example, electro-less plating.

[0020] Further referring to FIG. **1**, dielectric layer **28** is formed on RDLs **26**. The bottom surface of dielectric layer **28** is in contact with the top surfaces of RDLs **26** and dielectric layer **24**. In accordance with some embodiments of the present disclosure, dielectric layer **28** is formed of a polymer, which may be a photo-sensitive material such as PBO, polyimide, BCB, or the like. Alternatively, dielectric layer **28** may include a non-organic dielectric material such as silicon oxide, silicon nitride, silicon carbide, silicon oxynitride, or the like. Dielectric layer **28** is then patterned to form openings **30** therein. Hence, some portions of RDLs **26** are exposed through the openings **30** in dielectric layer **28**.

[0021] Next, referring to FIG. **2**, RDLs **32** are formed to connect to RDLs **26**. RDLs **32** include metal traces (metal lines) over dielectric layer **28**. RDLs **32** also include vias extending into the openings **30** in dielectric layer **28**. RDLs **32** may also be formed through a plating process, wherein each of RDLs **32** includes a seed layer (not shown) and a plated metallic material over the seed layer. In accordance with some embodiments, the formation of RDLs **32** may include depositing a blanket metal seed layer extending into the via openings, and forming and patterning a plating mask (such as photo resist), with opening formed directly over the via openings. A plating process is then performed to plate a metallic material, which fully fills the via openings **30**, and has some portions higher than the top surface of dielectric layer **28**. The plating mask is then removed, followed by an etching process to remove the exposed portions of the metal seed layer, which was previously covered by the plating mask. The remaining portions of the metal seed layer and the plated metallic material are RDLs **32**.

[0022] The metal seed layer and the plated material may be formed of the same material or different materials. The metallic material in RDLs **32** may include a metal or a metal alloy including copper, aluminum, tungsten, or alloys thereof. RDLs **32** include RDL lines (also referred to as traces or trace portions) **32**L and via portions (also referred to as vias) **32**V, wherein trace portions **32**L are over dielectric layer **28**, and via portions **32**V are in dielectric layer **28**. Since trace portions **32**L and via portions (also referred to as vias) **32**V are formed in a same plating process, there is no distinguishable interface between vias **32**V and the corresponding overlying trace portions **32**L. Also, each of vias **32**V may have a tapered profile, with the upper portions wider than the corresponding lower portions.

[0023] Referring to FIG. **3**, dielectric layer **34** is formed over RDLs **32** and dielectric layer **28**.

Dielectric layer **34** may be formed using a polymer, which may be selected from the same group of candidate materials as those of dielectric layer **28**. For example, dielectric layer **34** may be formed of PBO, polyimide, BCB, or the like. Alternatively, dielectric layer **34** may include a non-organic dielectric material such as silicon oxide, silicon nitride, silicon carbide, silicon oxynitride, or the like.

[0024] FIG. **3** further illustrates the formation of RDLs **36**, which are electrically connected to RDLs **32**. The formation of RDLs **36** may adopt the methods and materials similar to those for forming RDLs **32**. RDLs **36** include the trace portions (RDL lines) **36**L and via portions (vias) **36**V, wherein trace portions **36**L are over dielectric layer **34**, and via portions **36**V extend into dielectric layer **34**. Also, each of vias **36**V may have a tapered profile, with the upper portions wider than the corresponding lower portions.

[0025] FIG. **4** illustrates the formation of dielectric layers **38** and **42** and RDLs **40** and **44**. In accordance with some embodiments of the present disclosure, dielectric layers **38** and **42** are formed of materials selected from the same group of candidate materials for forming dielectric layers **34** and **28**, and may include organic materials or inorganic materials, as aforementioned. It is appreciated that although in the illustrated example embodiments, four dielectric layers **28**, **34**, **38**, and **42**, and the respective RDLs **32**, **36**, **40**, and **44** formed therein are discussed as an example, fewer or more dielectric layers and RDL layers may be adopted, depending on the routing requirement.

[0026] FIGS. **5** through **10** illustrate the formation of vias **56**, conductive pads **58**, and conductive bumps **60** (FIG. **10**) in accordance with some embodiments. Referring to FIG. **5**, dielectric layer **46** is formed. The respective process is illustrated as process **204** in the process flow **200** as shown in FIG. **20**. In accordance with some embodiments, dielectric layer **46** is formed of a polymer, which may be a photo-sensitive material such as PBO, polyimide, BCB, or the like. Dielectric layer **46** is patterned to form via openings **48**, so that the underlying pad portions of RDL lines **44**L are exposed. The respective process is illustrated as process **206** in the process flow **200** as shown in FIG. **20**. In accordance with some embodiments, via openings **48** are laterally offset from the respective underlying vias **44**V. As shown in FIG. **5**, some vias **44**V (such as via **44**V-1) may be aligned to the center of the overlying RDL lines **44**L (such as **44**L-**1**). Some other vias **44**V may be offset from the centers of the respective overlying RDL lines **44**L. For example, via **44**V-2 is offset to the right side from the middle of RDL line **44**L-**2**.

[0027] Referring to FIG. **6**, metal seed layer **51** is deposited. The respective process is illustrated as process **208** in the process flow **200** as shown in FIG. **20**. In accordance with some embodiments, metal seed layer **51** includes a titanium layer and a copper layer over the titanium layer. In accordance with alternative embodiments, metal seed layer **51** includes a single copper layer, which is in physical contact with dielectric layer **46**. Plating mask **50** is then formed and patterned, with openings **52** being formed in plating mask **50**. The respective process is illustrated as process **210** in the process flow **200** as shown in FIG. **20**. Via openings **48** are under and joined with openings **52**. The top-view shape of openings **52** may include circles or polygonal shapes such as hexagonal shapes, octagonal shapes, or the like.

[0028] Referring to FIG. **7**, metallic material **54** is deposited through a plating process. The respective process is illustrated as process **212** in the process flow **200** as shown in FIG. **20**. The plating process may include electrochemical plating, electroless plating, or the like. In accordance with some embodiments, metallic material **54** comprises copper or a copper alloy. Process conditions may be adjusted, so that the top surface of the plated material **54** may be planar. In accordance with alternative embodiments, the portions of the top surfaces of metallic material **54** may have recesses, as illustrated by dashed lines **53**, which recesses are formed due to the filling of via openings **48** (FIG. **7**).

[0029] In subsequent processes, plating mask **50**, which may be a photo resist, is removed, for example, through an ashing process. The respective process is illustrated as process **214** in the

process flow **200** as shown in FIG. **20**. The underlying portions of metal seed layer **51** are thus exposed.

[0030] Referring to FIG. **8**, without removing metal seed layer **51**, plating mask **57** is formed on metal seed layer **51** and plated material **54**, with openings **52′** being formed to reveal the plated material **54**. The respective process is illustrated as process **216** in the process flow **200** as shown in FIG. **20**. Next, as shown in FIG. **9**, conductive bump **60** is formed through a plating process, which may be an electrochemical plating process or an electroless plating process, for example. The respective process is illustrated as process **218** in the process flow **200** as shown in FIG. **20**. The entireties of conductive bumps **60** may be formed of a homogeneous material such as copper or a copper alloy. Conductive bumps **60** and the underlying plated material **54** may have distinguishable interfaces in between, or may be merged with each other (for example, when both formed of copper) without distinguishable interface in between. Conductive bumps **60** are also referred to as metal pillars or metal rods due to their shapes. For example, FIG. **19** illustrates an example conductive bump **60**, which have a round top-view shape, while other shapes such as hexagonal shapes, octagonal shapes, or the like may also be adopted, depending on the top-view shapes of openings **52′**. FIG. **9** further illustrates the deposition of solder regions **62** in accordance with some embodiments, which are also deposited through plating. Solder regions **62** may be formed of or comprise AgSn, AgSnCu, SnPb, or the like. In accordance with alternative embodiments, solder regions **62** are not formed.

[0031] In a subsequent process, plating mask **57** is removed, for example, through ashing. The respective process is illustrated as process **220** in the process flow **200** as shown in FIG. **20**. Next, an etching process, which may be a wet etching process or a dry etching process, is performed to remove the exposed portions of metal seed layer **51**. The respective process is illustrated as process **222** in the process flow **200** as shown in FIG. **20**. The portions of metal seed layer **51** directly under the plated metallic material **54** are left. Throughout the description, metallic material **54** and the underlying remaining portions of metal seed layer **51** are collectively referred to as vias **56** (also referred to a top vias) and conductive pads **58**. The resulting structure is shown in FIG. **10**. Vias **56** are the portions in dielectric layer **46**, while conductive pads **58** are the portions over dielectric layer **46**. Each of vias **56** and conductive pads **58** may include a remaining portion of the metal seed layer **51**, and a portion of the plated material **54**. Conductive bumps **60** are directly over conductive pads **58**, and are laterally recessed from the edges of conductive pads **58**. Alternatively stated, conductive pads **58** are larger than conductive bumps **60**.

[0032] Throughout the description, the structure over release film **22** are referred to as interconnect component **64**. In a subsequent process, interconnect component **64** may be placed on a frame (not shown), with solder regions **62** adhered to a tape in the frame. Interconnect component **64** is then de-bonded from carrier **20**, for example, by projecting UV light or a laser beam on release film **22**, so that release film **22** decomposes under the heat of the UV light or the laser beam. The respective process is illustrated as process **224** in the process flow **200** as shown in FIG. **20**. Interconnect component **64** is thus de-bonded from carrier **20**. The resulting interconnect component **64** is shown in FIG. **11**. In the resulting structure, dielectric layer **24** may be exposed. Solder regions **62**, if formed, may be reflowed to have rounded surfaces.

[0033] Further referring to FIG. **11**, electrical connectors **66** are formed to electrically connect to RDLs **26**. In accordance with some embodiments, electrical connectors **66** are UBMs. The formation process of UBMs **66** may also include patterning dielectric layer **24** to form openings, depositing a metal seed layer, which may include a titanium layer and a copper layer on the titanium layer, forming and patterning a plating mask, plating a conductive material, removing the plating mask, and etching the metal seed layer. In accordance with other embodiments, electrical connectors **66** are solder regions, and the formation process may include patterning dielectric layer **24** (for example, through laser drilling) to form openings, placing solder balls into the openings, and performing a reflow process to reflow the solder regions.

[0034] In a subsequent process, interconnect component **64** is sawed apart in a singulation process to form a plurality of identical interconnect components **64′** (also referred to as package components **64′**). The singulation process may be performed by sawing interconnect component **64** along scribe lines **68**.
[0035] Interconnect components **64′** may be used for forming packages. FIG. **12** illustrates a portion of an example structure including interconnect component **64′** bonded to a package component **70**. Electrical connectors **72**, which are on the surface of package component **70**, may be bonded to interconnect components **64′** through soldered regions **74** in accordance with some embodiments. Solder regions **74** may include solder regions **62** as shown in FIG. **11**. Electrical connectors **72** may be UBMs, metal pillars, bond pads, or the like. In accordance with alternative embodiments, electrical connectors **72** are metal pillars, and are bonded to conductive bumps **60** through direct metal-to-metal bonding. In accordance with these embodiments, the solder regions **62** (FIG. **11**) are not formed, and conductive bumps **60** are physically joined to electrical connectors **72**. In accordance with some embodiments, underfill **76** is dispensed into the gap between package component **70** and interconnect component **64′**. Underfill **76** is in contact with the top surfaces and the sidewalls of the extension portions of conductive pads **58**, with the extension portions being extending laterally beyond the edges of the overlying conductive bumps **60**. Encapsulant **78**, which may be formed of or comprise molding compound, is dispensed. A planarization process may be performed to level the top surface of package component **70** with the top surface of encapsulant **78**.
[0036] FIG. **13** illustrates an application of interconnect components **64′**. The structure shown in FIG. **12** may also be a part of the structure shown in FIG. **13**. Each interconnect component **64′** is bonded to one or a plurality of package components **70** (including **70**A and **70**B as an example). The details of some of the structures such as the eccentric bonding structures are not shown in detail, and the details may be found referring to FIGS. **11** and **12**, and FIGS. **14-16**. In accordance with some embodiments, package components **70** include a logic die, which may be a Central Processing Unit (CPU) die, a Graphic Processing Unit (GPU) die, a mobile application die, a Micro Control Unit (MCU) die, an input-output (IO) die, a BaseBand (BB) die, an Application processor (AP) die, or the like. Package components **70** may also include memory dies such as Dynamic Random Access Memory (DRAM) dies, Static Random Access Memory (SRAM) dies, or the like. The memory dies may be discrete memory dies, or may be in the form of a die stack that includes a plurality of stacked memory dies. Package components **70** may also include System-on-Chip (SOC) dies.
[0037] In accordance with some embodiments, package components **70** include package component **70**A, which may be a logic die or an SOC die. In accordance with some embodiments, package component **70**A includes semiconductor substrate **71** and integrated circuit devices (not shown, including transistors, for example). Package components **70** may further include package component **70**B, which may be a memory die or a memory stack. Underfill **76** and molding compound **78** are also illustrated.
[0038] Interconnect component **64′** is further bonded to package component **80**. In accordance with some embodiments, package component **80** is or comprises an interposer, a package substrate, a printed circuit board, or the like. The bonding may be achieved through solder regions **82**. Underfill **84** is dispensed between interconnect component **64′** and package component **80**.
[0039] FIGS. **14** and **15** illustrate a cross-sectional view and a top view, respectively, of a part of an eccentric structure in accordance with some embodiments. The illustrated part is in region **84**A in FIG. **12**. In accordance with some embodiments, both of conductive bump **60** and conductive pad **58** have symmetric structures. For example, FIG. **15** illustrates that conductive bump **60** and conductive pad **58** may have round top-view shapes. Conductive bump **60** and conductive pad **58** may have common center line **60**C, and both of conductive bump **60** and conductive pad **58** are symmetric relative to center line **60**C. In accordance with other embodiments, conductive bump **60**

and conductive pad **58** may have other symmetric top-view shapes including, and not limited to, hexagonal shapes, octagonal shapes, or the like, which are also symmetric to center line **60**C. Via **56** is offset from center line **60**C. For example, via **56** is shifted toward left in FIG. **14**. On the other hand, via **44**V is offset from via **56**. Vias **40**V, **36**V, and **32**V may be vertically aligned to via **44**V, or may be offset from via **44**V. Throughout the description, the corresponding bonding structure is referred to as an eccentric bonding structure since the center lines of via **56** and conductive bump **60** are vertically misaligned.

[0040] In conventional structures, via **56** would have been aligned to center line **60**C. This, however, results in problems. For example, conductive bump **60**, conductive pad **58**, and vias **44**V, **40**V and **36**V are formed of metals, which have significantly greater Coefficient of Thermal Expansion (CTE) values than the CTE of surrounding materials such as dielectric layers **46**, **42**, and **38**, underfill **76**, and encapsulant **78**. When vias **56**, **44**V (and possibly vias **40**V and **36**V) are also aligned to center line **60**C, there is a high stress in the resulting structure, which may lead to delamination and trace breaking. If via **44**V is moved side-way (while via **56** is aligned to center line **60**C) to offset from conductive pad **58** in order to reduce the stress, the resulting structure would occupy a larger chip area. In the present disclosure, via **56** is offset from the center line **60**C, so that via **44**V can be offset from via **56** without incurring the area penalty, while the stress may be reduced. For example, when temperature increases, and via **56** applies a downward force to the underlying portion of RDL line **44**L, due to the flexibility of RDL line **44**L, the force is not transferred to via **44**V (or at least an attenuated force is transferred), and hence the force, if any, will not be compounded with the force generated due to the expansion of via **44**V and the underlying RDL lines and vias.

[0041] FIGS. **18** and **19** illustrate two structures, on which simulations are performed. The structure shown in FIG. **18** represents a conventional structure, which has conductive bump **60**′, via **56**′, conductive pad **58**′, RDL pad **44**L′, and via **44**V′ vertically aligned. The structure shown in FIG. **19** represents a structure formed in accordance with some embodiments of the present disclosure, which has conductive bump **60**, conductive pad **58**, via **56**, RDL line **44**L, and via **44**V. Via **56** is offset from the center lines of conductive bump **60** and conductive pad **58**. Via **44**V is offset from via **56**. The simulation results revealed that when the stress applied to RDL line **40**L′ (FIG. **18**) has a normalized magnitude of 1.0, the stress applied to RDL line **40**L (FIG. **19**) has a normalized magnitude of 0.9, which means that the embodiments of the present disclosure has the stress reduced by 10 percent compared to conventional structures.

[0042] Referring back to FIG. **14**, in accordance with some embodiments, via **56** is offset from the center line **60**C of conductive bump **60** by spacing S**1**. The offset spacing S**1** may be equal to or greater than about 8.5 μm, and may be in the range between about 8.5 μm and about 20 μm. Furthermore, is it desirable that via **56** is at least partially overlapped by conductive bump **60**. For example, FIG. **14** illustrates that a right portion of via **56** is overlapped by conductive bump **60**, while a left portion of via **56** extends beyond the left edge of conductive bump **60**. The (at least partial) overlapping of conductive bump **60** is advantageous in allowing via **56** to support both of conductive pad **58** and conductive bump **60**, and to adequately pass the stress received by via **56** from conductive pad **58** to RDL line **44**L. This allows RDL line **44**L to absorb an adequate amount of the stress. In accordance with alternative embodiments, as shown in FIG. **15**, via **56** may be shifted slightly to the right to the position shown as **56**′, so that an entirety of via **56** is overlapped by conductive bump **60**. For example, the left edge of via **56** may be aligned with the left edge of conductive bump **60** in accordance with some embodiments. As may be realized from FIG. **15**, increasing the size of conductive pad **58** to be larger than the size of conductive bump **60** allows via **56** to shift for a desirable distance.

[0043] As shown in FIG. **14**, in accordance with some embodiments of the present disclosure, via **44**V is offset from both of center line **60**C and via **56**. Via **44**V and via **56** may also offset relative to center line **60**C toward opposite directions. In accordance with some embodiments, vias **56** and

44V are on the opposite sides of center line **60**C, with neither via **56** nor via **44**V having any portion passed-through by center line **60**C. Offsetting vias **56** and **44** toward opposite directions from center line **60**C may increase the distance between vias **56** and **44**V, and increase the length of the portion of RDL line **44**L interconnecting vias **56** and **44**V. This may also increase the ability for RDL line **44**L to absorb stress. In accordance with some embodiments, vias **40**V, **36**V, and/or **32**V are vertically aligned to via **44**V. In accordance with alternative embodiments, each or all of vias **40**V, **36**V, and/or **32**V may be laterally offset from via **44**V, either toward left or toward right.
[0044] In accordance with alternative embodiments, the center line **44**VC of via **44**V is still offset from center line **60**C for a small offset amount, while via **44**V is still passed-through by center line **60**C. Offsetting via **44**V toward an opposite direction than via **56** still results in the lateral spacing between vias **56** and **44**V, and improves the stress absorption by RDL line **44**L. On the other hand, via **44**V may be overlapped by conductive pad **58** and conductive bump **60**, so that via **44**V will not occupy additional chip area (unless it needs to for signal re-routing reasons) since it occupies the same chip area occupied by conductive pad **58** and conductive bump **60**.
[0045] Referring again to FIG. **15**, some dimensions are marked. In accordance with some embodiment, from the top view, the lateral spacing S**2** between center line **60**C and the edge of via **56** may be in the range between about 4 μm and about 12 μm. The diameter Dia**58** of conductive pad **58** may be in the range between about 30 μm and 50 μm. The diameter Dia**60** of conductive bump **60** may be in the range between about 20 μm and 40 μm. The diameters Dia**56** and Dia**44**V may be in the range within 30 μm. In some embodiments, the diameters Dia**56** and Dia**44**V may be in the range between about 7 μm and about 20 μm.
[0046] FIGS. **16** and **17** illustrate a cross-sectional view and a top view, respectively, of a part of an eccentric structure in accordance with alternative embodiments. The illustrated part is in region **84**B in FIG. **12**. These embodiments are similar to the embodiments shown in FIGS. **14** and **15**, except that the center line **44**VC of via **44**V is aligned to center line **60**C of conductive bump **60**. Each or all of vias **40**V, **36**V, and **32**V may be vertically aligned to, or laterally offset from, via **44**V, either toward left or toward right. These embodiments may be adopted when the spacing between vias **56** and **44**V is large enough to provide adequate stress absorption by pad-and-trace portion **44**L, for example, when the reduction is close to saturation, and when the further increase in the spacing does not result in significant reduction in the stress. With via **44**V (and vias **40**V and **36**V) being shifted left compared to the structure as shown in FIG. **14**, the right side of chip area may be provided for the routing of other RDLs (such as RDL lines **44**A, **40**A, and **36**A, etc.).
[0047] Depending on the sizes of via **56** and via **44**V, a small portion of via **44**V may be overlapped by via **56**, or alternatively, an entirety of via **44**V is offset from via **56**. The corresponding vias **56** and **44**V are shown with dashed lines (FIG. **17**), and are marked as vias **56**″ and **44**V′, respectively.
[0048] In the example embodiments as provided above, the eccentric bonding structures are formed in a build-up substrate. In accordance with alternative embodiments, the eccentric bonding structures may be formed in an interposer, which may include a semiconductor substrate and through-vias in the semiconductor substrate. For example, when RDLs are formed for the interposer after the backside polishing for revealing through-vias, the eccentric bonding structures may be formed as parts of the RDL structure of the interposer. In accordance with yet alternative embodiments, the eccentric bonding structures may be formed in a Chip-on-Wafer-on-Substrate (CoWoS) package, wherein the eccentric bonding structures may be formed in either or both of the wafer and the package substrate. In accordance with yet alternative embodiments, the eccentric bonding structures may be formed in a fan-out package, wherein the eccentric bonding structures may be formed in the fan-out RDLs, which are formed after the molding of device dies.
[0049] In above-illustrated embodiments, some processes and features are discussed in accordance with some embodiments of the present disclosure to form a three-dimensional (3D) package. Other features and processes may also be included. For example, testing structures may be included to aid in the verification testing of the 3D packaging or 3DIC devices. The testing structures may include,

for example, test pads formed in a redistribution layer or on a substrate that allows the testing of the 3D packaging or 3DIC, the use of probes and/or probe cards, and the like. The verification testing may be performed on intermediate structures as well as the final structure. Additionally, the structures and methods disclosed herein may be used in conjunction with testing methodologies that incorporate intermediate verification of known good dies to increase the yield and decrease costs.

[0050] The embodiments of the present disclosure have some advantageous features. By forming eccentric bonding structures, the stress in the bonding structure and surrounding features is reduced. The reduction of the stress does not incur the increase in the manufacturing cost, and does not incur chip area penalty.

[0051] In accordance with some embodiments of the present disclosure, a method comprises forming a first dielectric layer; forming a first redistribution line comprising a first via extending into the first dielectric layer, and a first trace over the first dielectric layer; forming a second dielectric layer covering the first redistribution line; patterning the second dielectric layer to form a via opening, wherein the first redistribution line is revealed through the via opening; depositing a conductive material into the via opening to form a second via in the second dielectric layer, and a conductive pad over and contacting the second via; and forming a conductive bump over the conductive pad, wherein the conductive pad is larger than the conductive bump, and the second via is offset from a center line of the conductive bump. In accordance with an embodiment, the second via and the conductive pad are formed through a common plating process. In accordance with an embodiment, the second via, the conductive pad, and the conductive bump are formed using a same metal seed layer. In accordance with an embodiment, the method further includes bonding a package component over the conductive bump; and dispensing an underfill, wherein the underfill contacts a first sidewall of the conductive bump, and the underfill further contacts a top surface and a second sidewall of the conductive pad. In accordance with an embodiment, the second via comprises a first portion overlapped by the conductive bump, and a second portion extending beyond a corresponding edge of the conductive bump. In accordance with an embodiment, the first via is further offset from the center line of the conductive bump, and the first via and the second via are on opposite sides of the center line of the conductive bump. In accordance with an embodiment, the first via comprises at least a portion overlapped by the conductive bump. In accordance with an embodiment, the first via is aligned to the center line of the conductive bump.

[0052] In accordance with some embodiments of the present disclosure, a structure comprises a first dielectric layer; a first via extending into the first dielectric layer; a conductive trace over the first dielectric layer, wherein the conductive trace is over and joined to the first via; a second dielectric layer covering the conductive trace; a second via in the second dielectric layer; a conductive pad over and contacting the second via; and a conductive bump over and contacting the conductive pad, wherein the conductive pad extends laterally beyond edges of the conductive bump, and wherein the second via and the conductive bump are eccentric. In accordance with an embodiment, the conductive bump and the conductive pad have round top-view shapes. In accordance with an embodiment, the second via has a first portion overlapped by the conductive bump. In accordance with an embodiment, the second via further comprises a second portion extending beyond edges of the conductive bump. In accordance with an embodiment, the first via is aligned to a center line of the conductive bump. In accordance with an embodiment, the first via is offset from a center line of the conductive bump. In accordance with an embodiment, the first via and the second via are on opposite sides of the center line of the conductive bump, and the second via is further partially overlapped by the conductive bump.

[0053] In accordance with some embodiments of the present disclosure, a structure comprises a plurality of dielectric layers; a plurality of redistribution lines in the plurality of dielectric layers, wherein each of the plurality of redistribution lines comprises a via and a trace over and contacting the via, and the vias in the plurality of redistribution lines are stacked to form a via stack, with the

vias being vertically aligned; a top via over and contacting a top trace in a top redistribution line of the plurality of redistribution lines; a conductive pad over and contacting the top via; and a conductive bump over and joined to the conductive pad, wherein the conductive pad and the conductive bump share a common center line, and the top via is offset from the common center line, with at least a portion of the top via being overlapped by the conductive bump. In accordance with an embodiment, the common center line does not pass through the top via. In accordance with an embodiment, the top via is fully overlapped by the conductive bump. In accordance with an embodiment, the top via is partially overlapped by the conductive bump. In accordance with an embodiment, the structure further includes an underfill contacting first sidewalls of the conductive bump, and second sidewalls and a top surface of the conductive pad.

[0054] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

Claims

1. A structure comprising: a plurality of redistribution lines comprising: a plurality of vias; and a plurality of metal traces, each overlying and joined to a corresponding one of the plurality of vias, wherein the plurality of vias and the plurality of metal traces share a first vertical center line; a conductive feature over and joined to a top metal trace of the plurality of metal traces; a top via over and contacting the conductive feature, wherein the top via has a second vertical center line; a conductive pad over and contacting the top via; and a conductive bump over and contacting the conductive pad, wherein centers of the conductive pad and the conductive bump are vertically aligned to a third vertical center line, and wherein the third vertical center line is offset from the second vertical center line; and an underfill, wherein the conductive bump and the conductive pad are in the underfill.

2. The structure of claim 1, wherein the first vertical center line and the third vertical center line is a same line.

3. The structure of claim 1, wherein the first vertical center line is laterally spaced apart from the third vertical center line.

4. The structure of claim 2, wherein the first vertical center line and the second vertical center line are on opposite sides of the third vertical center line.

5. The structure of claim 2, wherein entireties of the plurality of redistribution lines are on an opposite side of the third vertical center line than an entirety of the top via.

6. The structure of claim 2, wherein the first vertical center line, the second vertical center line, and the third vertical center line are perpendicular to an interface between the conductive pad and the conductive bump.

7. The structure of claim 1, wherein the top via is partially overlapped by the conductive bump.

8. The structure of claim 1, wherein an entirety of the top via is overlapped by the conductive bump.

9. The structure of claim 1, wherein the plurality of redistribution lines have an identical structure in a cross-sectional view of the structure.

10. The structure of claim 9, wherein structures of the plurality of redistribution lines are identical to each other.

11. The structure of claim 1 further comprising: a device die over the conductive bump; and a

solder region joining the conductive bump to the device die.

12. The structure of claim 1, wherein the underfill is in physical contact with a first sidewall of the conductive pad and a second sidewall of the conductive bump to form vertical interfaces.

13. A structure comprising: a plurality of lower vias, wherein upper ones of the plurality of lower vias overlap respective underlying ones of the plurality of lower vias, and wherein a first vertical center line passes through centers of the plurality of lower vias; a top via over and electrically connected to the plurality of lower vias; a conductive pad over and contacting the top via; a conductive bump over and joined to the conductive pad to form an interface, with the conductive bump overlapping at least a portion of the top via and at least a portion of the plurality of lower vias, wherein the conductive pad and the conductive bump share a second vertical center line that is perpendicular to the interface, and wherein the top via is laterally spaced apart from both of the first vertical center line and the second vertical center line in a cross-sectional view of the structure; and a solder region over and contacting the conductive bump.

14. The structure of claim 13, wherein the plurality of lower vias is directly underlying, and is overlapped by, a center portion of the conductive bump.

15. The structure of claim 13, wherein the plurality of lower vias are on an opposite side of the second vertical center line than the top via.

16. The structure of claim 13, wherein the conductive bump is laterally recessed from edges of the conductive pad.

17. A structure comprising: a lower via; a metal feature over and physically contacting the lower via; a top via over and physically contacting the metal feature; a conductive pad over and contacting the top via; a conductive bump over and joined to the conductive pad, wherein in a top view of the structure, the conductive pad and the conductive bump share a common center, and the top via is offset from the common center; and a solder region over and contacting the conductive bump.

18. The structure of claim 17, wherein in the top view of the structure, a center of the lower via is also the common center.

19. The structure of claim 17, wherein the lower via is on an opposite side of the common center than the top via.

20. The structure of claim 17 further comprising a lower via stack comprising a plurality of stacked lower vias, wherein the lower via stack is underlying and joined to the lower via, wherein the plurality of stacked lower vias has a same cross-sectional shape as, and is vertically aligned to, the lower via.