US 20250259668A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2025/0259668 A1**

Lee et al. (43) **Pub. Date: Aug. 14, 2025**

(54) **BIT-LINE SENSE AMPLIIFIER AND SEMICONDUCTOR MEMORY DEVICE INCLUDING THE SAME**

(71) Applicant: **Samsung Electronics Co., Ltd.**, Suwon-si (KR)

(72) Inventors: **Kyuseok Lee**, Suwon-si (KR); **Hyunju Sung**, Suwon-si (KR)

(21) Appl. No.: **18/765,195**

(22) Filed: **Jul. 5, 2024**

(30) **Foreign Application Priority Data**

Feb. 8, 2024 (KR) 10-2024-0019312

Publication Classification

(51) **Int. Cl.**

G11C 11/4091	(2006.01)
G11C 11/4094	(2006.01)
G11C 11/4096	(2006.01)

(52) **U.S. Cl.**

CPC ***G11C 11/4091*** (2013.01); ***G11C 11/4094*** (2013.01); ***G11C 11/4096*** (2013.01)

(57) **ABSTRACT**

A semiconductor memory device includes a bit-line sense amplifier that includes an amplifying circuit connected to a bit-line, a complementary bit-line, a sensing bit-line, a complementary sensing bit-line, an offset cancellation circuit, an equalizer and an isolation circuit. The offset cancellation circuit connects the bit-line and the complementary bit-line to the complementary sensing bit-line and the sensing bit-line, respectively, based on an offset cancellation signal. The equalizer provides a precharge voltage to the sensing bit-line and the complementary sensing bit-line based on an equalizing signal. The isolation circuit is connected between the bit-line and the sensing bit-line and between the complementary bit-line and the complementary sensing bit-line, and connects the sensing bit-line and the complementary sensing bit-line equalized with the precharge voltage to the bit-line and the complementary bit-line, respectively, based on an isolation signal.

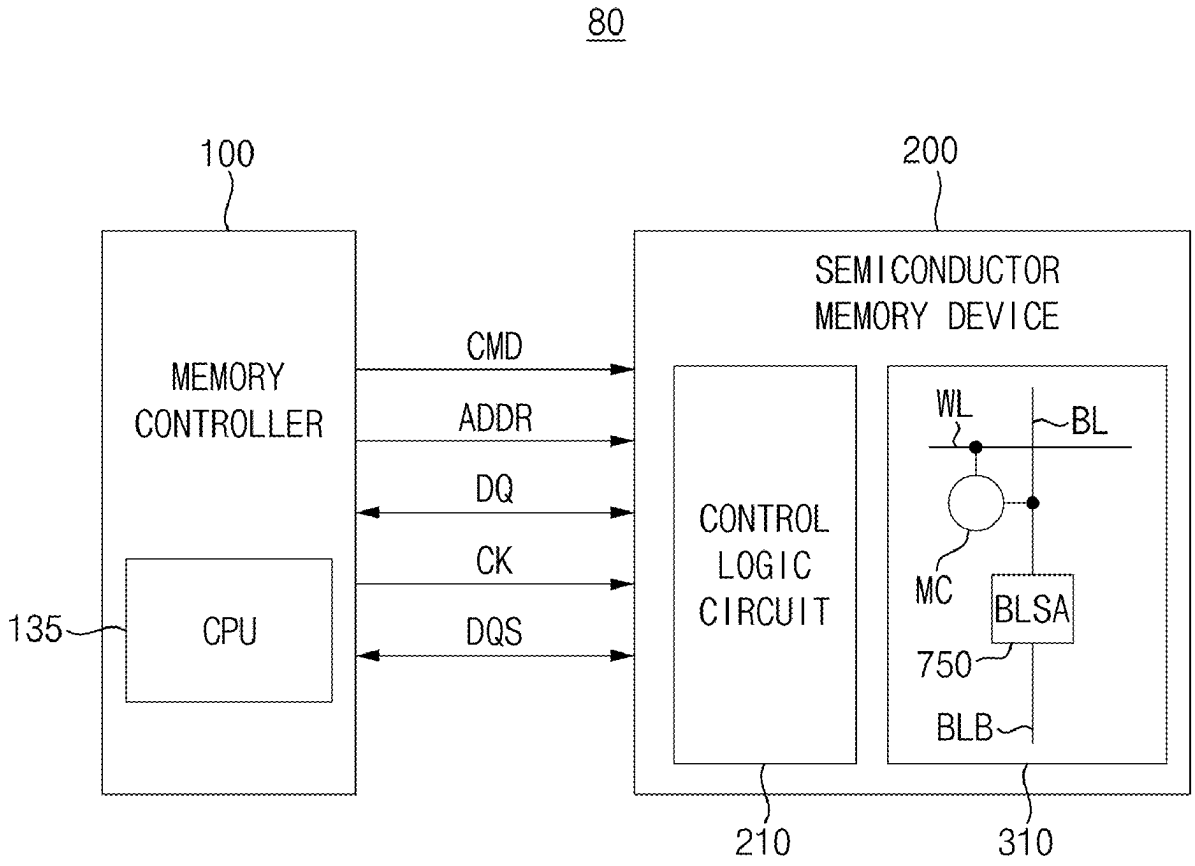


FIG. 1

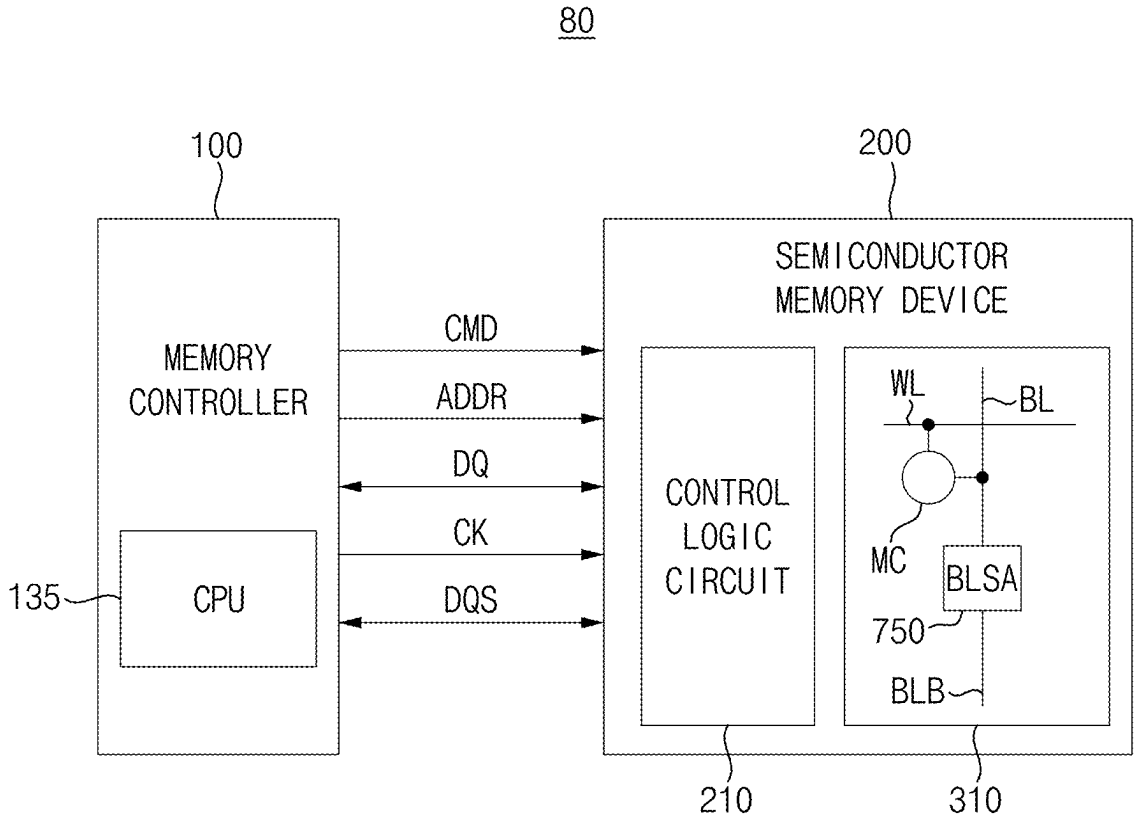

80
100
200
MEMORY CONTROLLER
CPU
135
CMD
ADDR
DQ
CK
DQS
SEMICONDUCTOR MEMORY DEVICE
CONTROL LOGIC CIRCUIT
WL
BL
MC
BLSA
750
BLB
210
310

FIG. 2

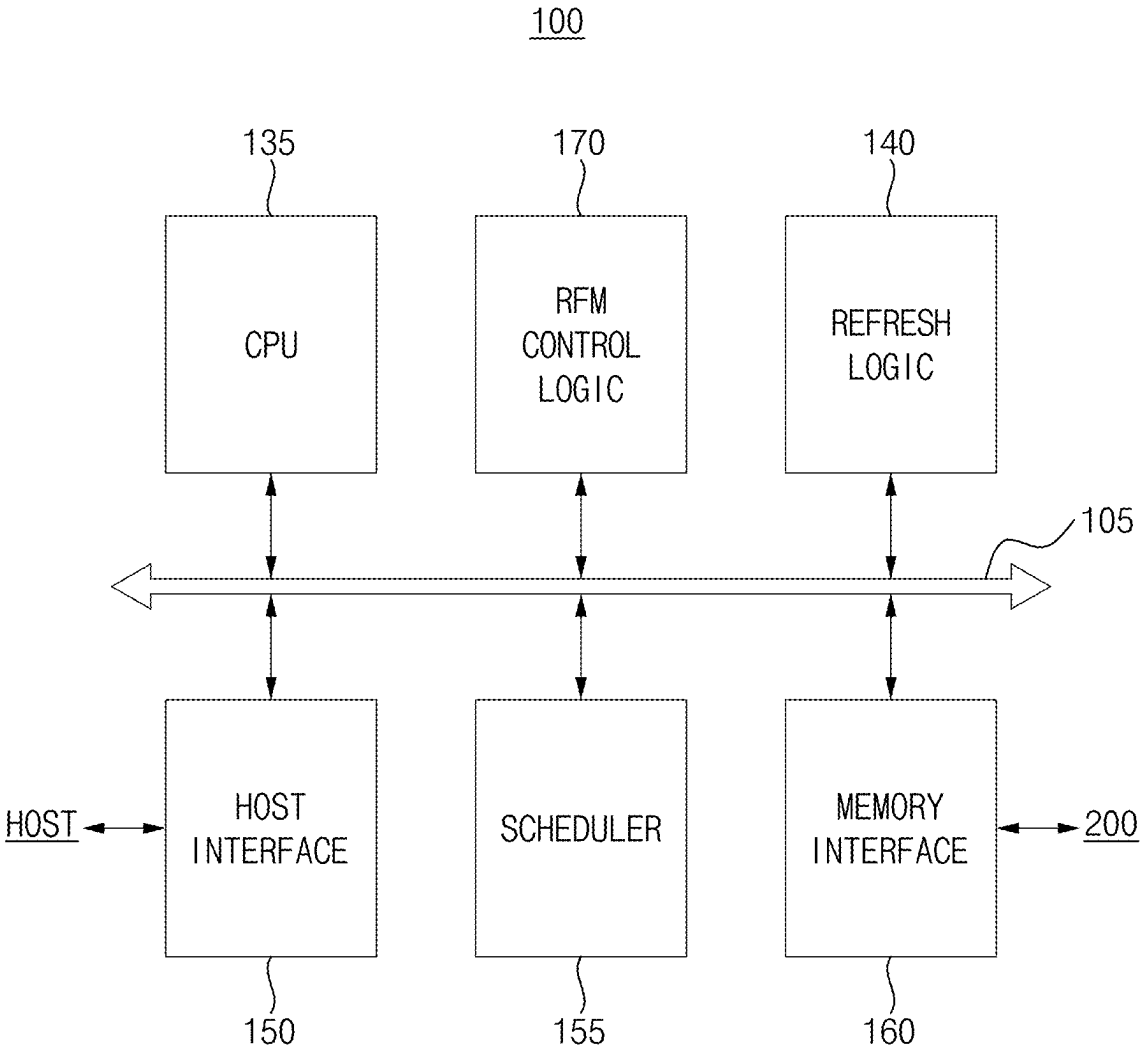

100
135
170
140
CPU
RFM CONTROL LOGIC
REFRESH LOGIC
105
HOST
HOST INTERFACE
SCHEDULER
MEMORY INTERFACE
200
150
155
160

FIG. 3

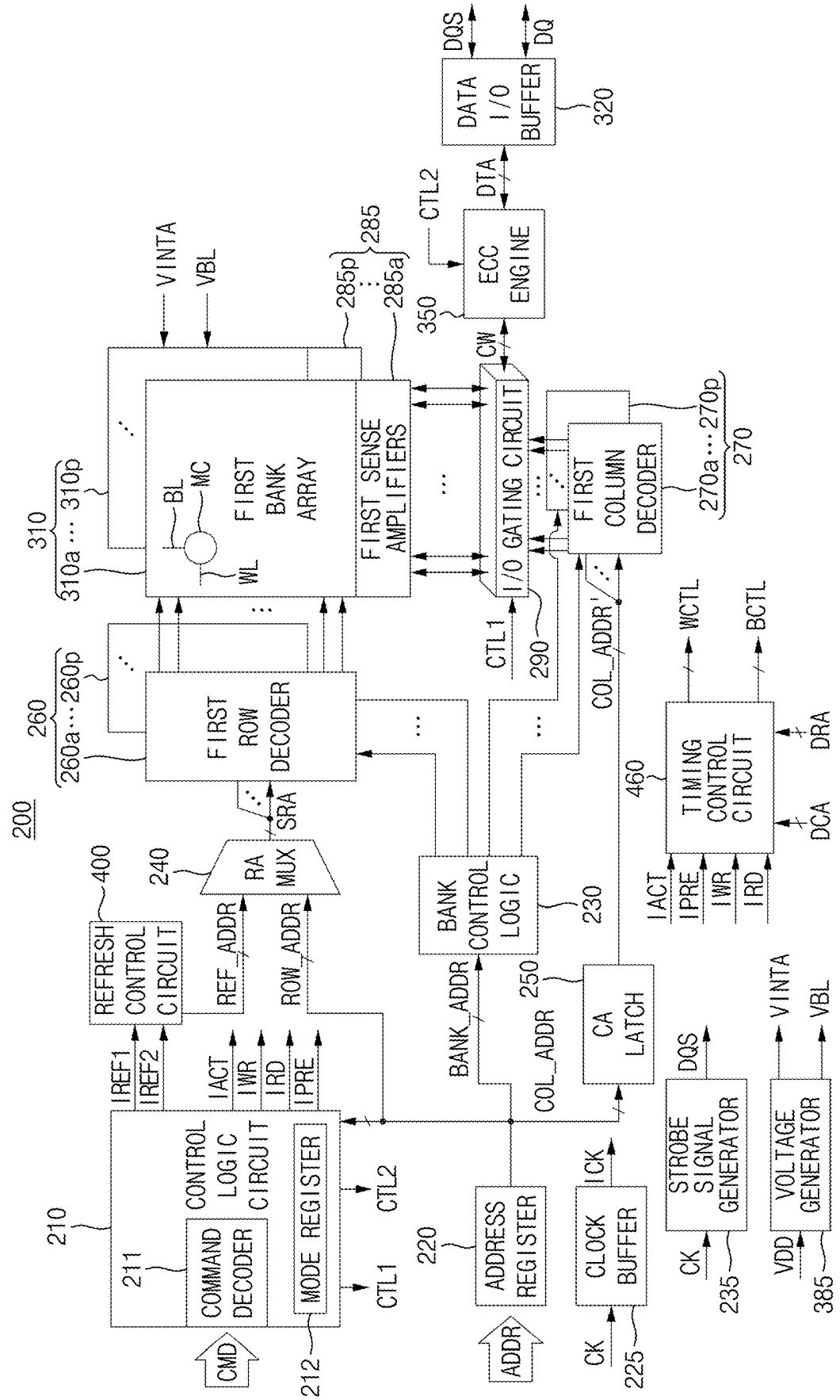

200
210
211
COMMAND DECODER
CONTROL LOGIC CIRCUIT
MODE REGISTER
212
CMD
CTL1
CTL2
220
ADDRESS REGISTER
ADDR
225
CK
CLOCK BUFFER
ICK
230
BANK CONTROL LOGIC
BANK_ADDR
COL_ADDR
250
CA LATCH
235
CK
STROBE SIGNAL GENERATOR
DQS
385
VDD
VOLTAGE GENERATOR
VINTA
VBL
240
RA MUX
SRA
REF_ADDR
ROW_ADDR
400
REFRESH CONTROL CIRCUIT
IREF1
IREF2
IACT
IWR
IRD
IPRE
260
260a ··· 260p
FIRST ROW DECODER
310
310a ··· 310p
FIRST BANK ARRAY
BL
MC
WL
285
285a ··· 285p
FIRST SENSE AMPLIFIERS
290
I/O GATING CIRCUIT
CTL1
CW
350
ECC ENGINE
CTL2
DTA
320
DATA I/O BUFFER
DQS
DQ
270
270a ··· 270p
FIRST COLUMN DECODER
COL_ADDR'
460
TIMING CONTROL CIRCUIT
IACT
IPRE
IWR
IRD
WCTL
BCTL
DRA
DCA

FIG. 4

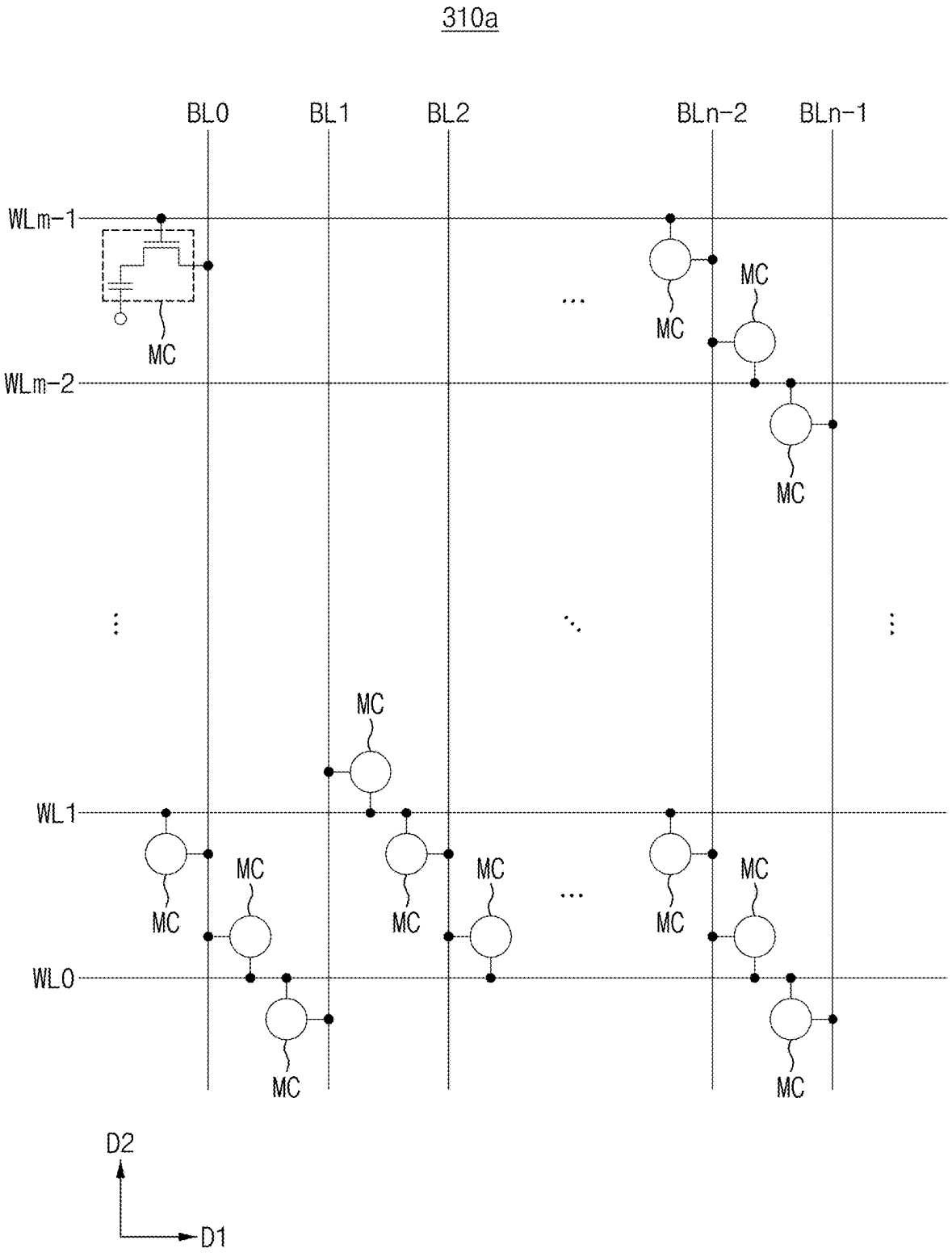


FIG. 5

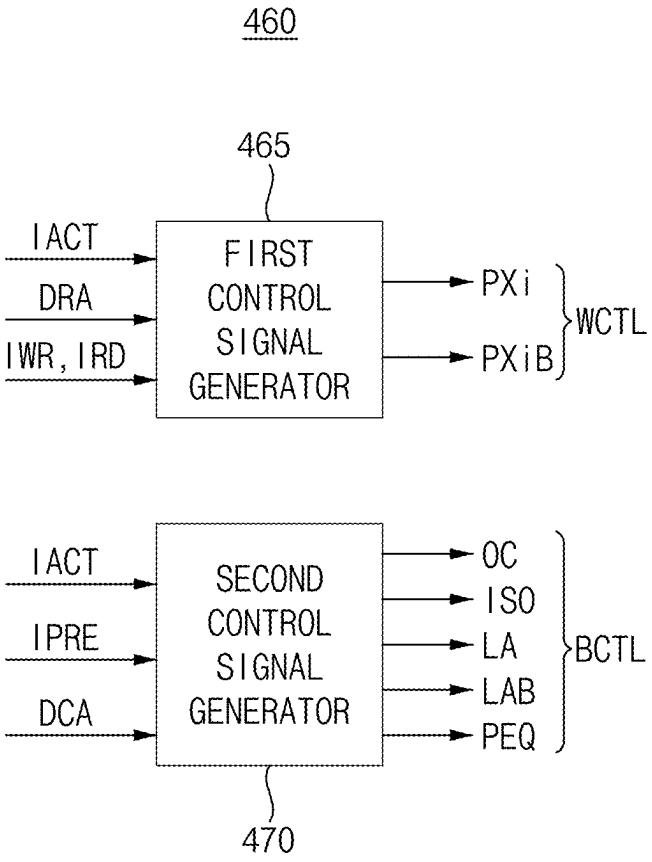

460
465
IACT
DRA
IWR, IRD
FIRST CONTROL SIGNAL GENERATOR
PXi
PXiB
WCTL
IACT
IPRE
DCA
SECOND CONTROL SIGNAL GENERATOR
OC
ISO
LA
LAB
PEQ
BCTL
470

FIG. 6

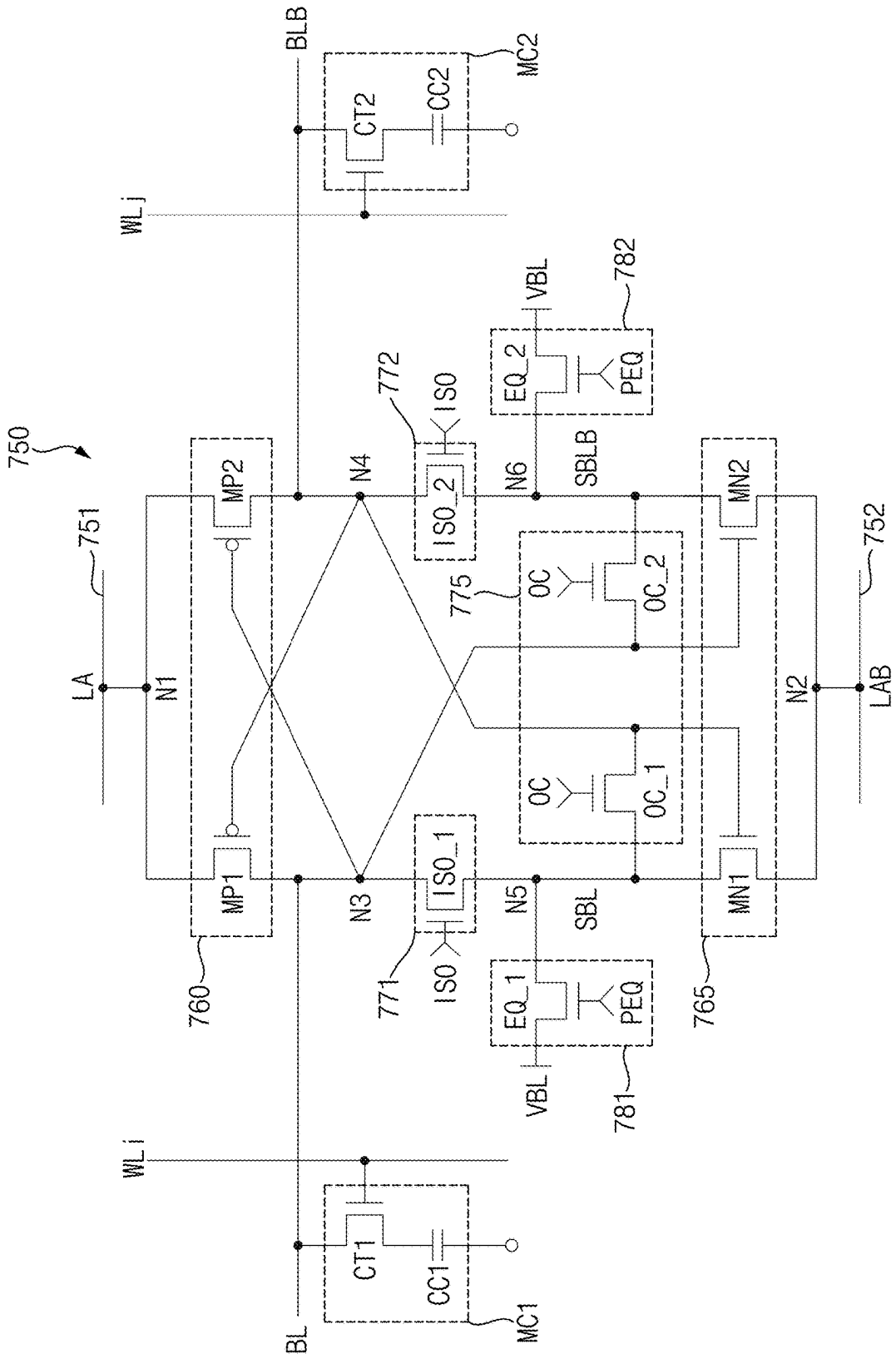

750
751
752
760
765
771
772
775
781
782
LA
LAB
N1
N2
N3
N4
N5
N6
SBL
SBLB
MP1
MP2
MN1
MN2
ISO_1
ISO_2
ISO
OC
OC_1
OC_2
EQ_1
EQ_2
PEQ
VBL
BL
BLB
WL i
WL j
CT1
CT2
CC1
CC2
MC1
MC2

FIG. 7

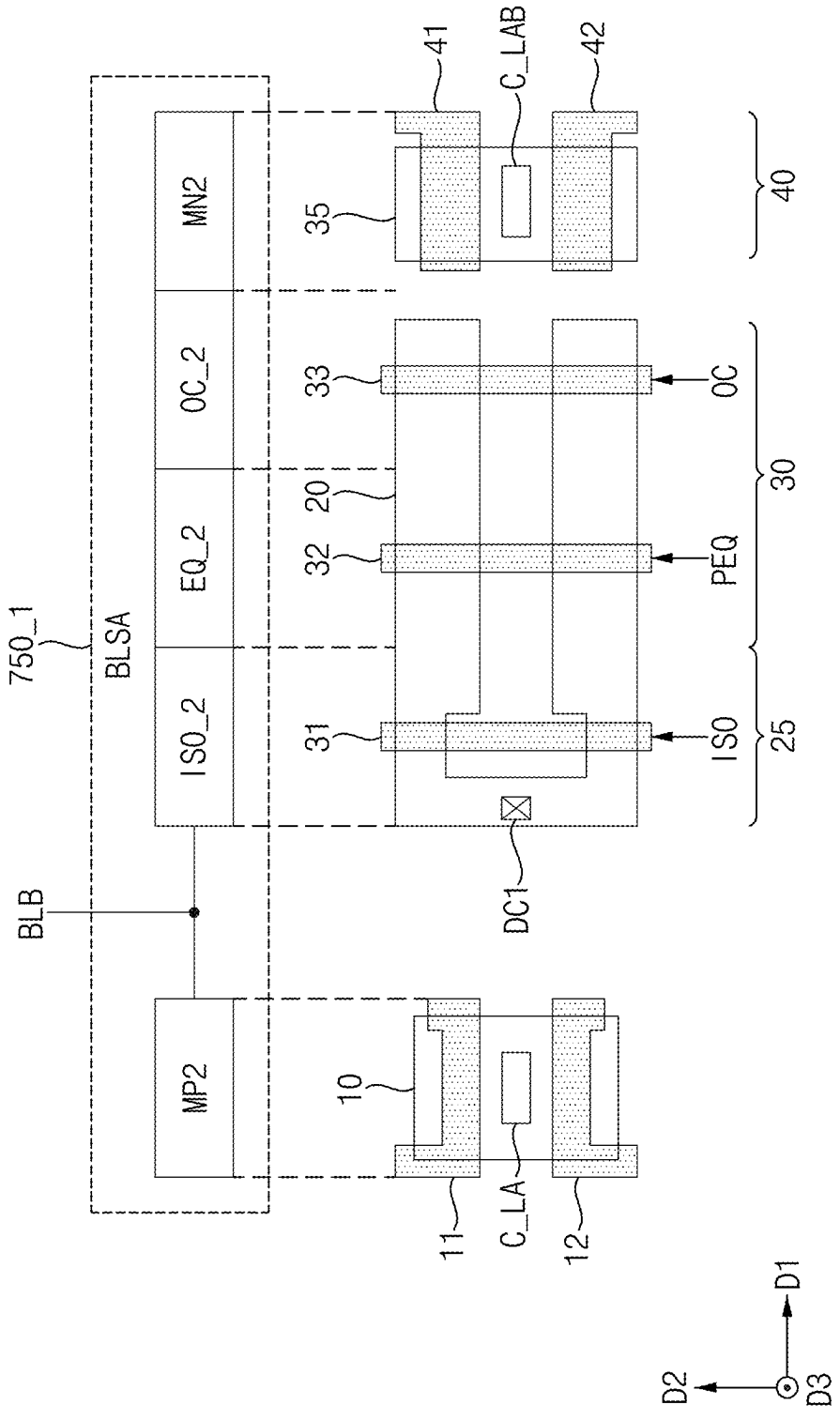

750_1
BLSA
MN2
OC_2
EQ_2
IS0_2
MP2
BLB
41
C_LAB
42
35
40
33
OC
20
32
PEQ
30
31
IS0
25
DC1
10
11
C_LA
12
D1
D2
D3

FIG. 8

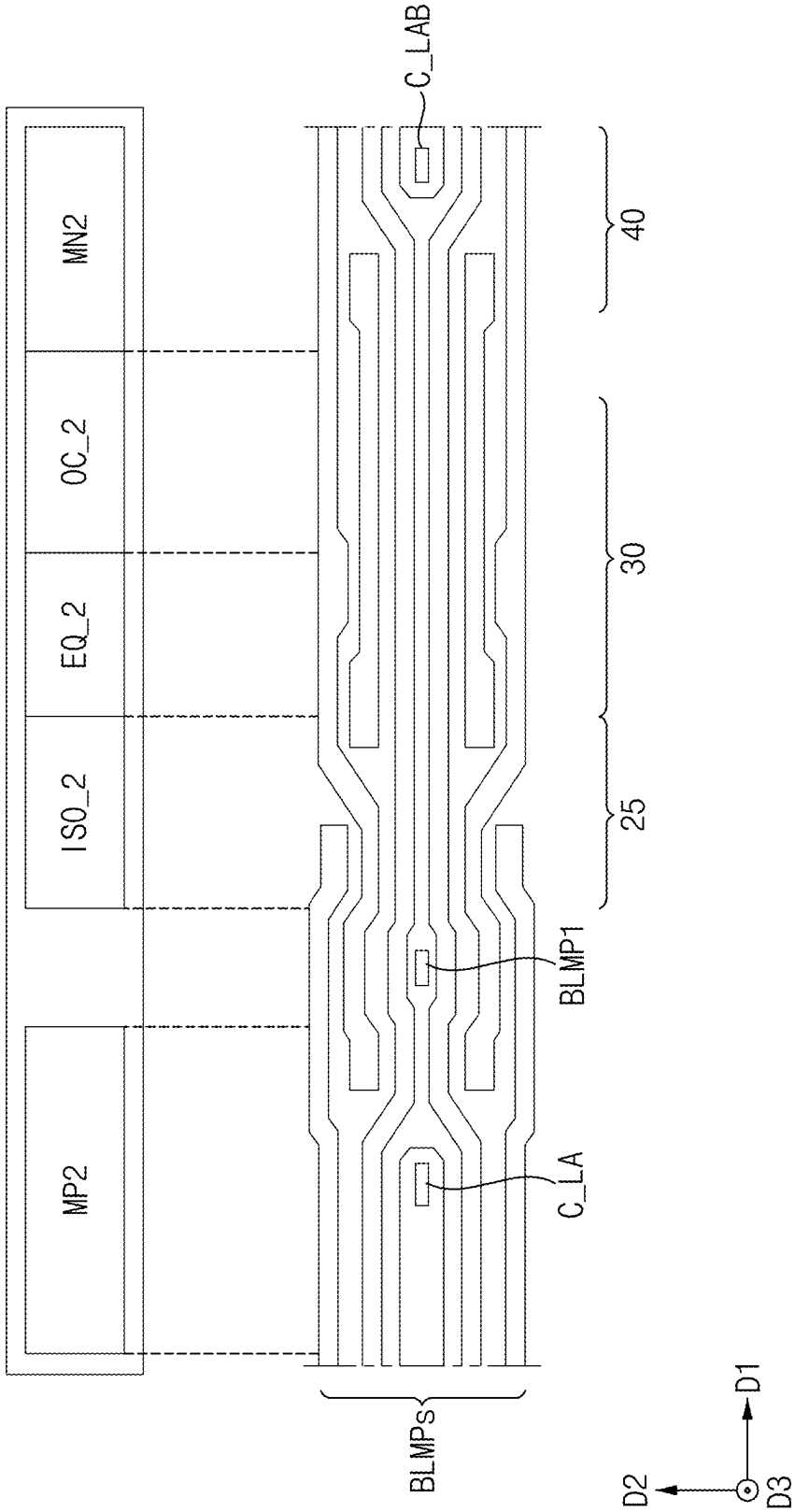


FIG. 9

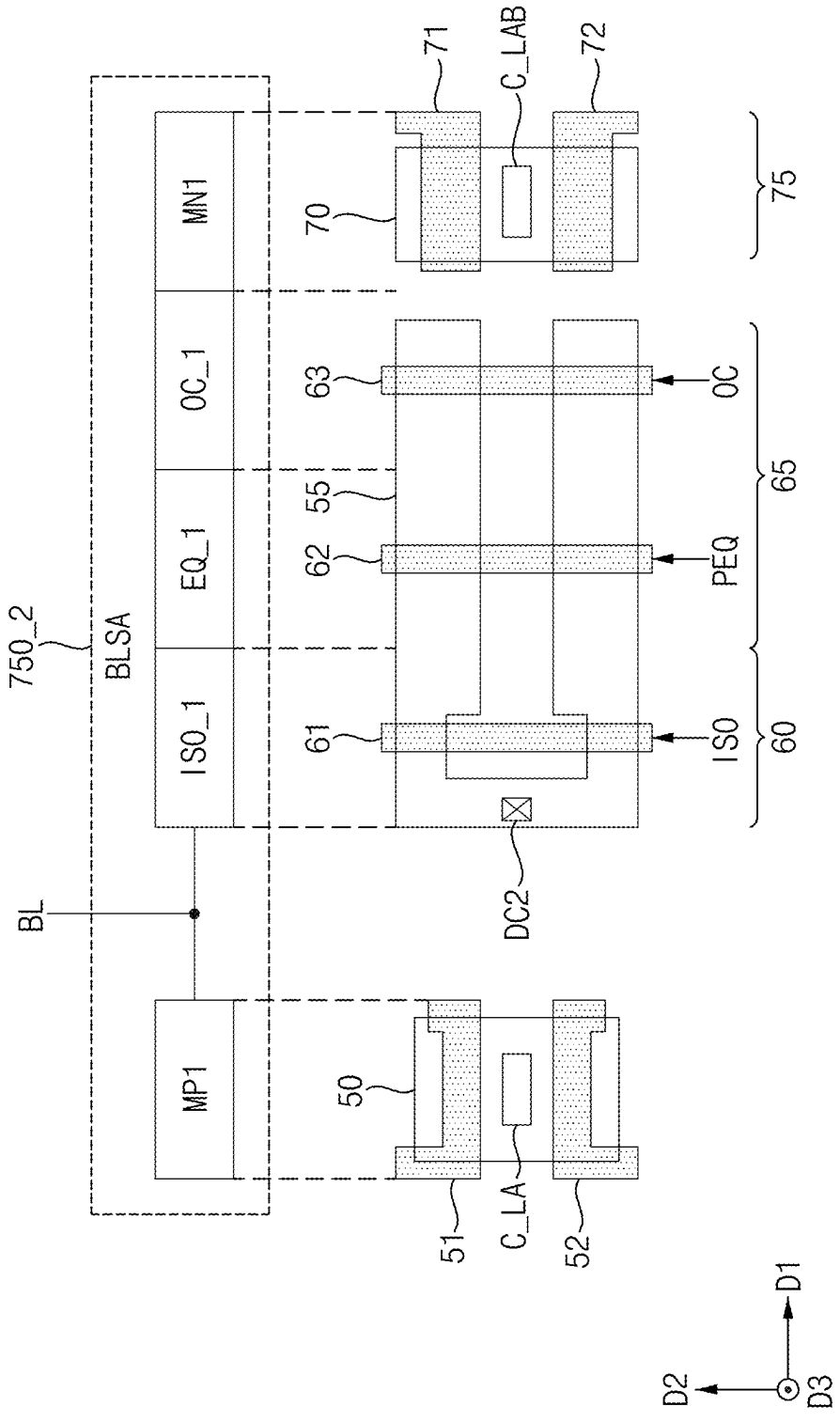

750_2
BLSA
MN1
OC_1
EQ_1
ISO_1
MP1
BL
71
C_LAB
72
70
75
63
OC
55
62
PEQ
65
61
ISO
60
DC2
50
51
C_LA
52
D1
D2
D3

FIG. 10

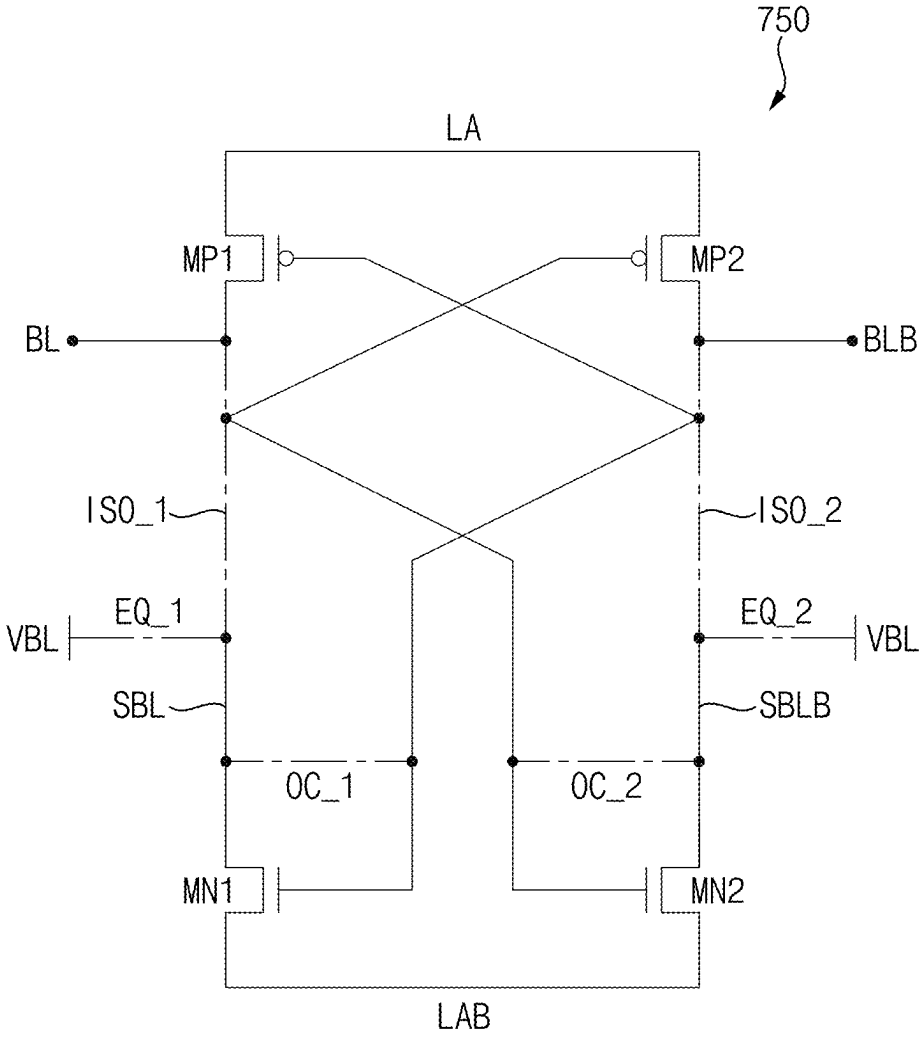

750
LA
MP1
MP2
BL
BLB
ISO_1
ISO_2
EQ_1
EQ_2
VBL
VBL
SBL
SBLB
OC_1
OC_2
MN1
MN2
LAB

FIG. 11

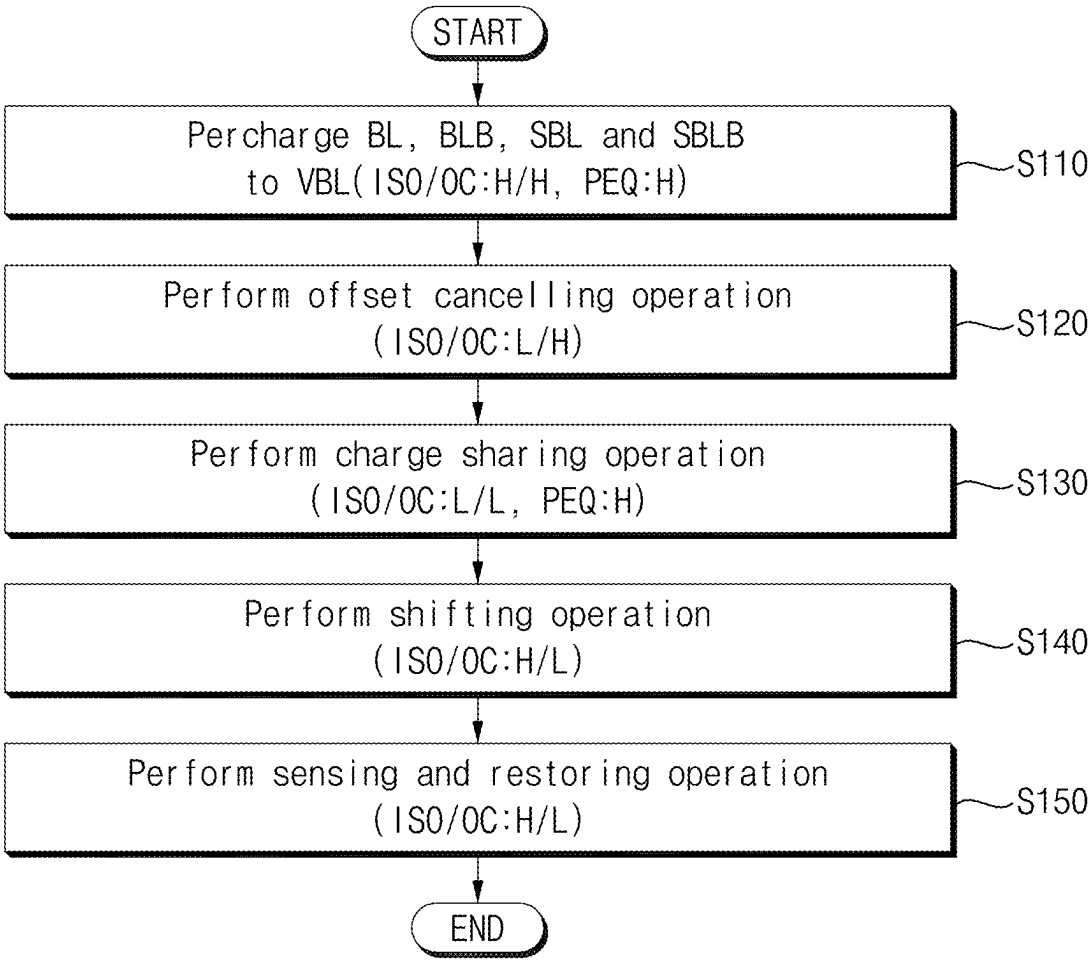
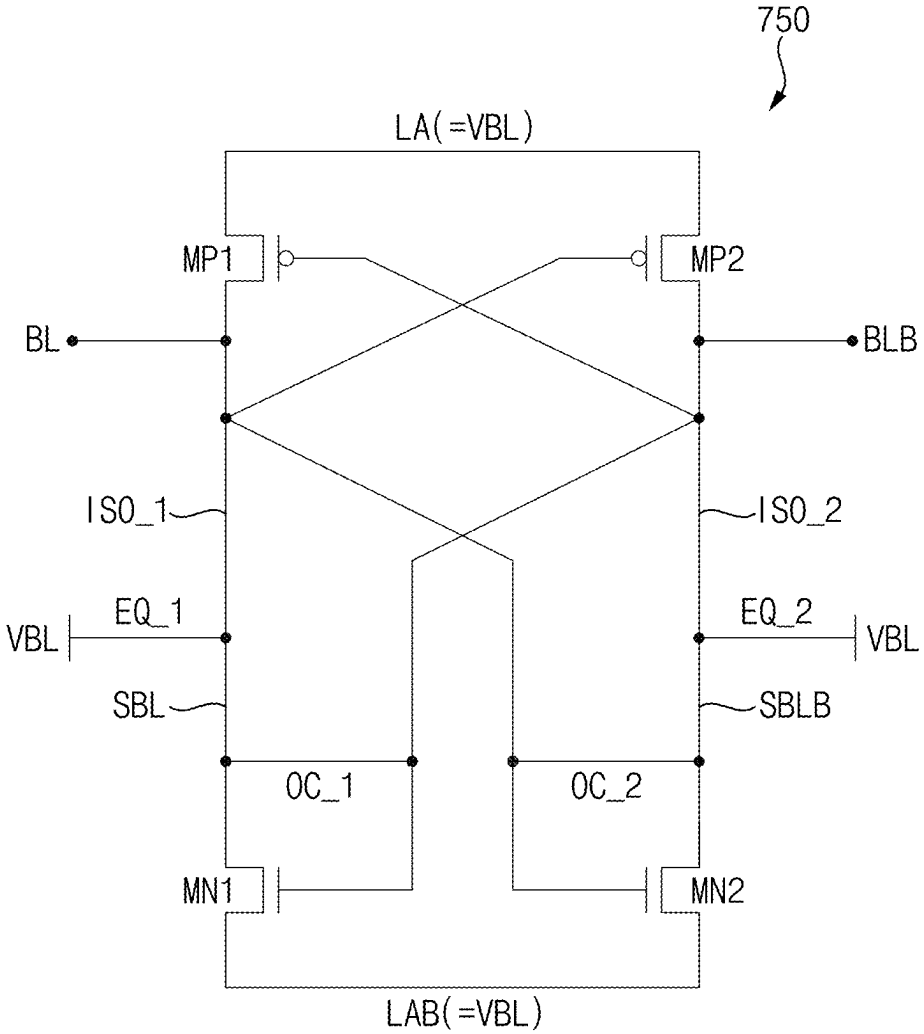
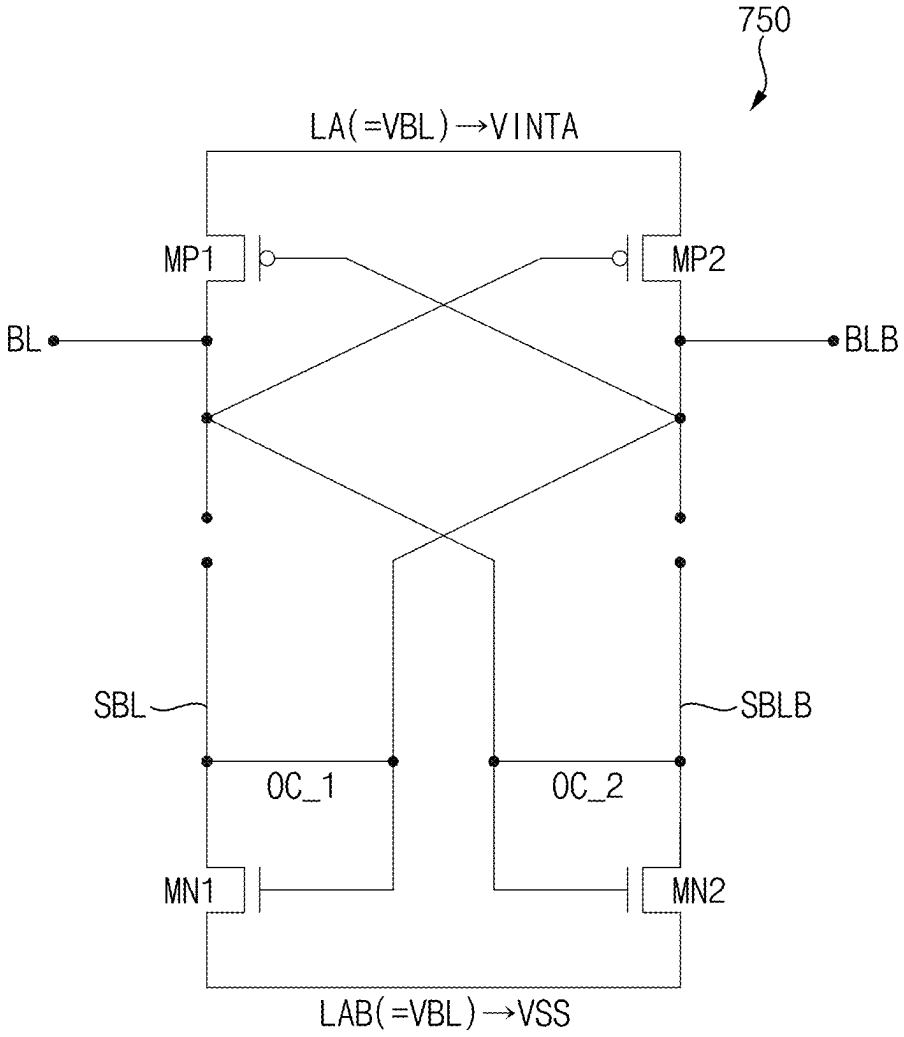

START
Percharge BL, BLB, SBL and SBLB to VBL(ISO/OC:H/H, PEQ:H)
S110
Perform offset cancelling operation (ISO/OC:L/H)
S120
Perform charge sharing operation (ISO/OC:L/L, PEQ:H)
S130
Perform shifting operation (ISO/OC:H/L)
S140
Perform sensing and restoring operation (ISO/OC:H/L)
S150
END

FIG. 12A



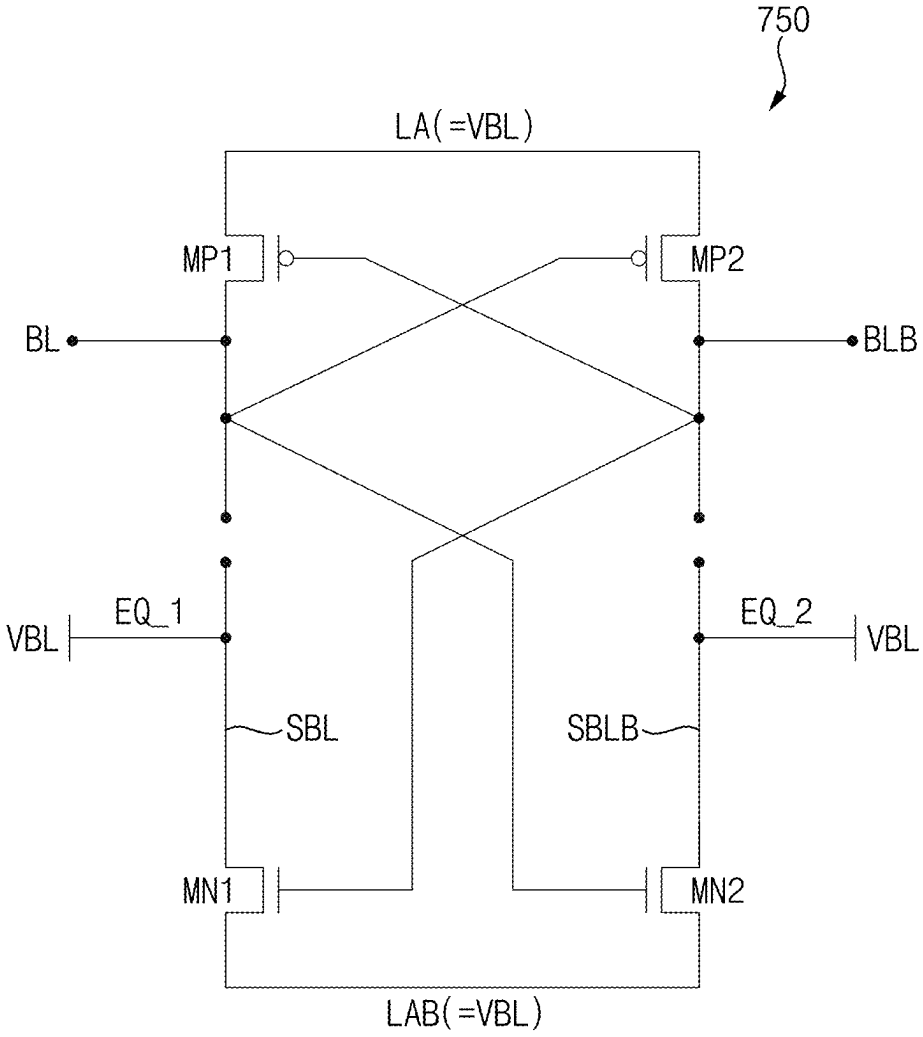
[Precharging Operation]

FIG. 12B



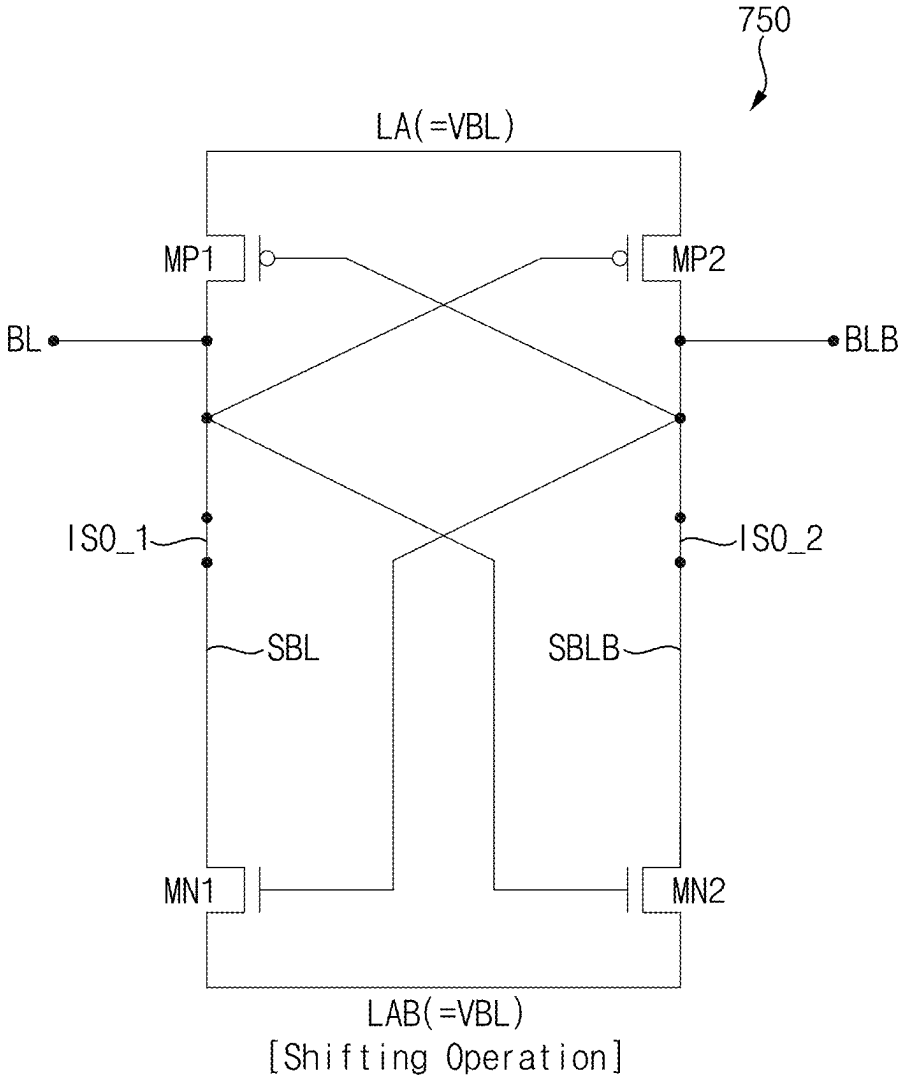
[Offset Cancelling Operation]

FIG. 12C



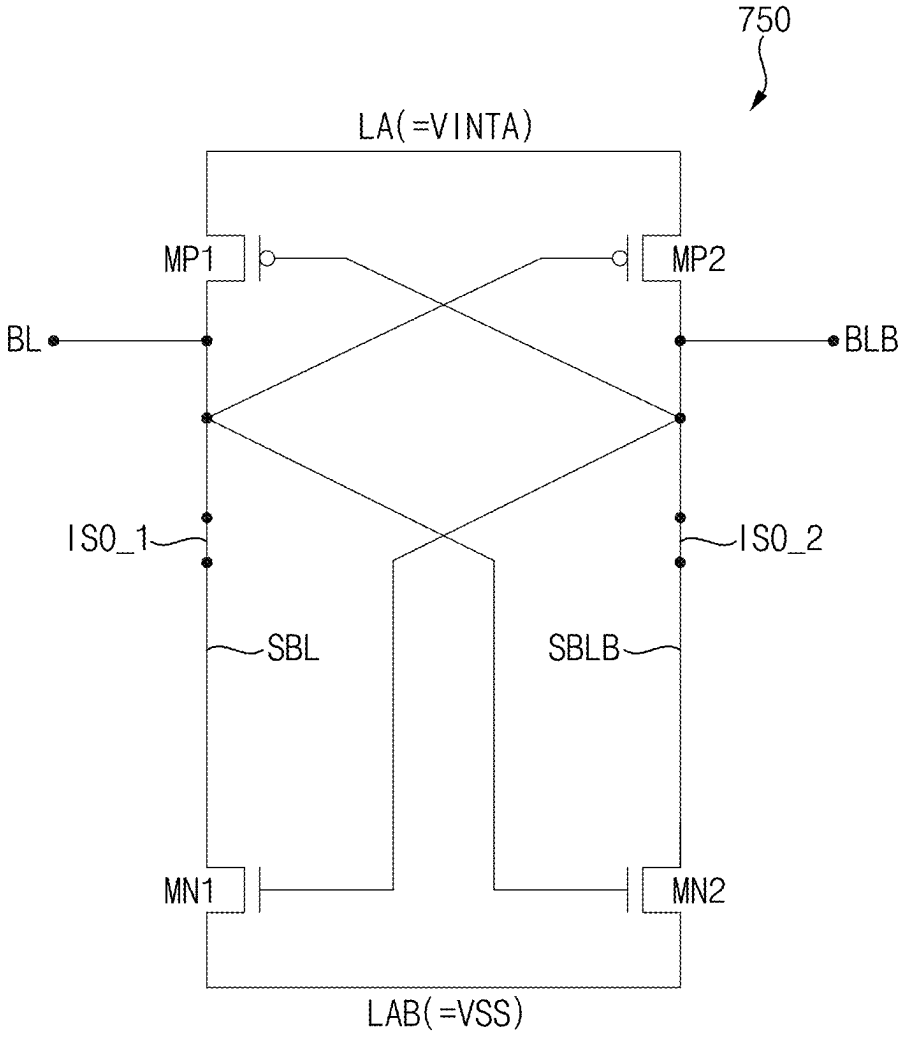
[Charge Sharing Operation]

FIG. 12D



[Shifting Operation]

FIG. 12E



[Sensing and Restoring Operation]

FIG. 13

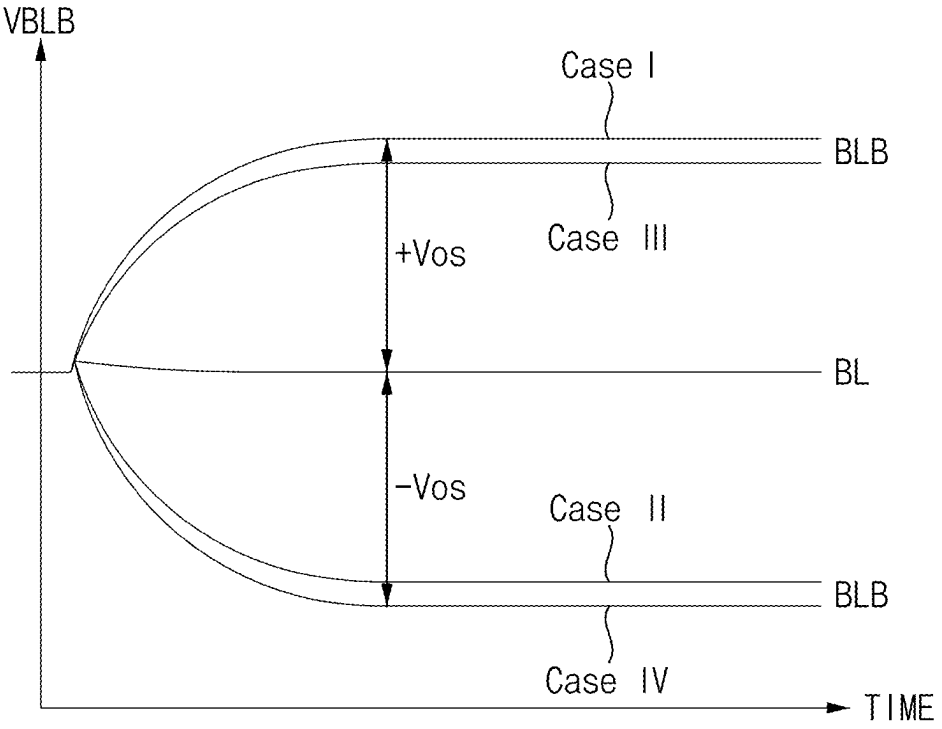


FIG. 14

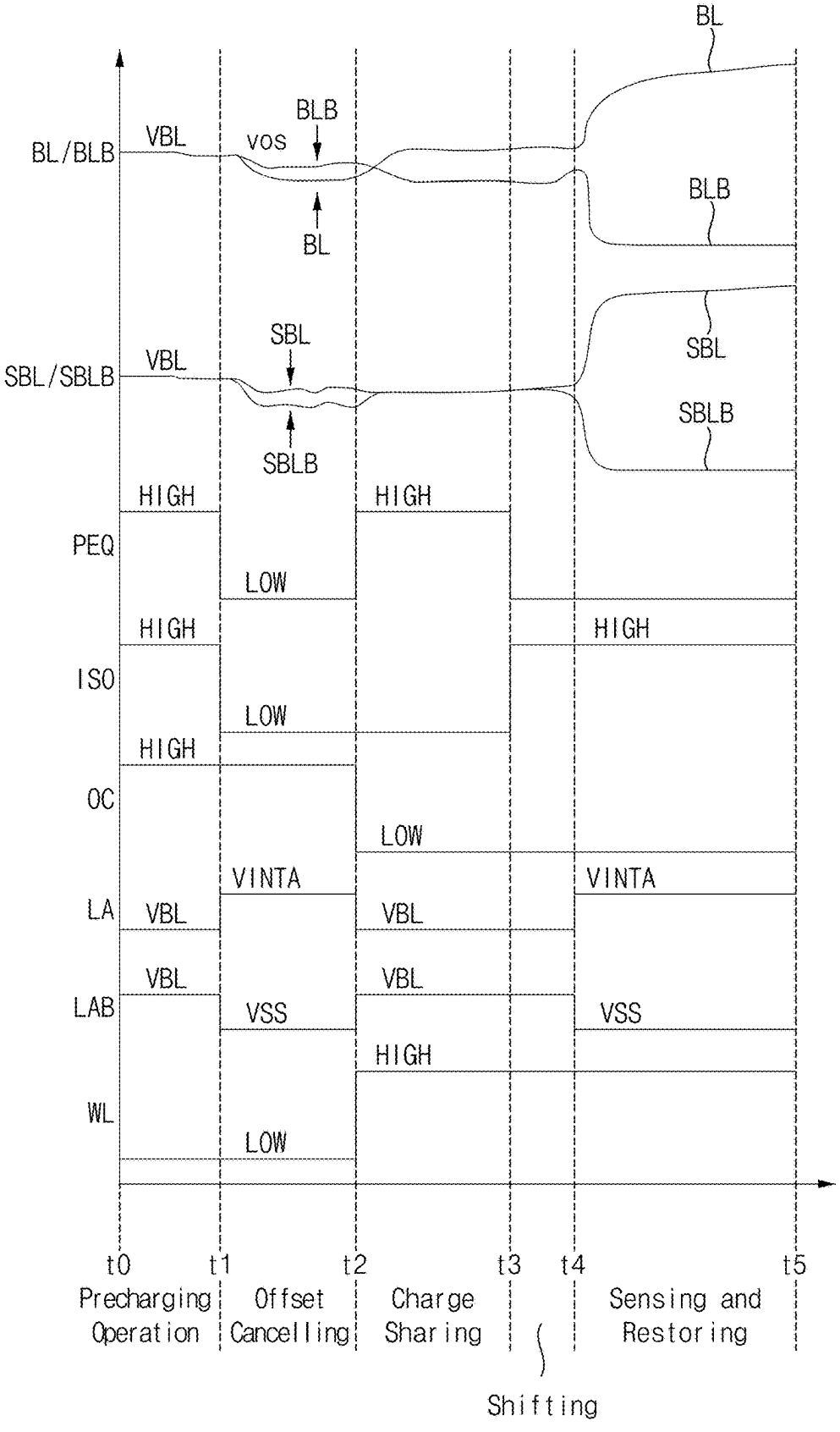

BL
BLB
BL/BLB
VBL
vos
BLB
BL
SBL
SBL/SBLB
VBL
SBL
SBLB
SBLB
HIGH
HIGH
PEQ
LOW
HIGH
HIGH
ISO
LOW
HIGH
OC
LOW
VINTA
VINTA
LA
VBL
VBL
VBL
VBL
LAB
VSS
VSS
HIGH
WL
LOW
t0
t1
t2
t3
t4
t5
Precharging Operation
Offset Cancelling
Charge Sharing
Sensing and Restoring
Shifting

FIG. 15

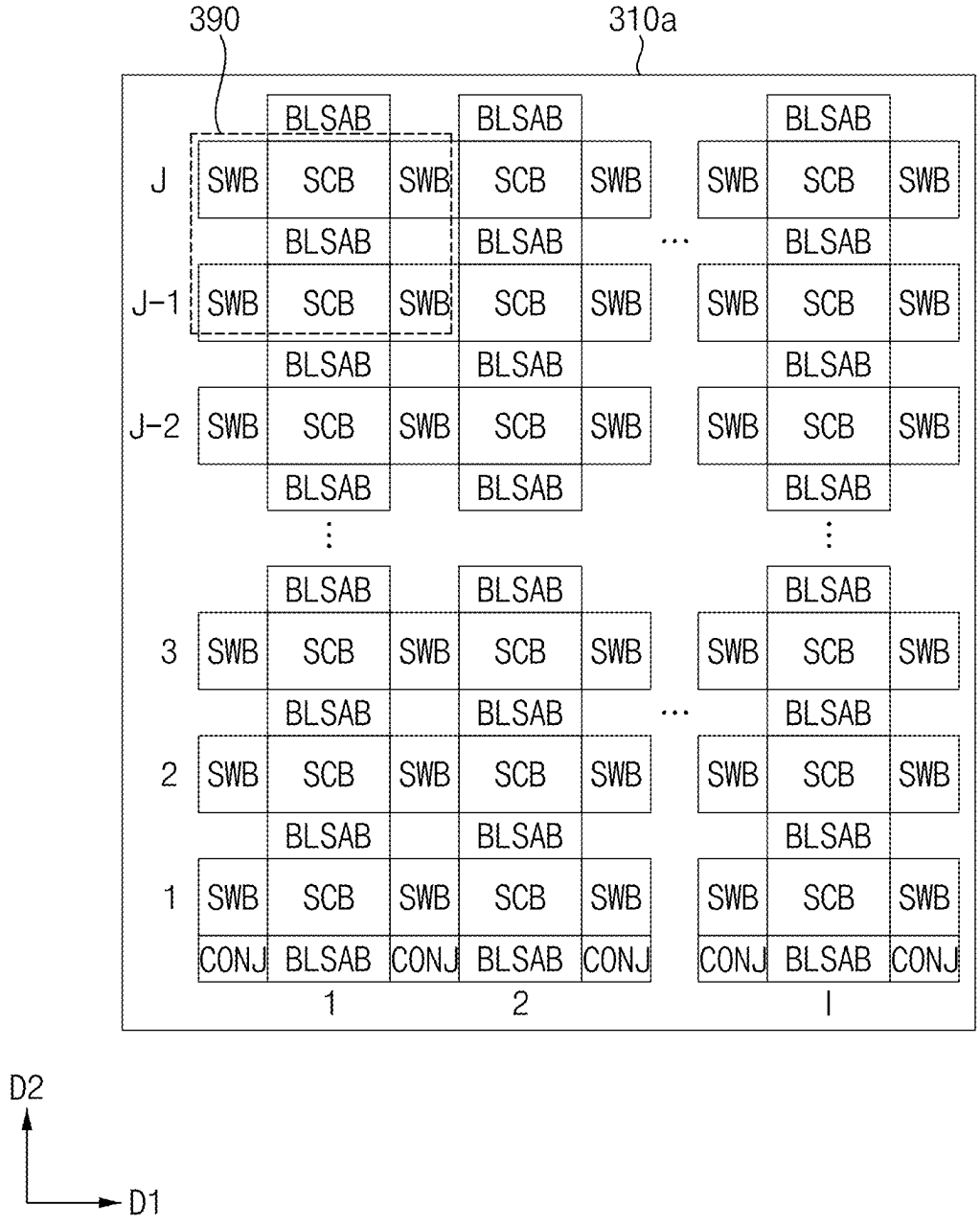


FIG. 16

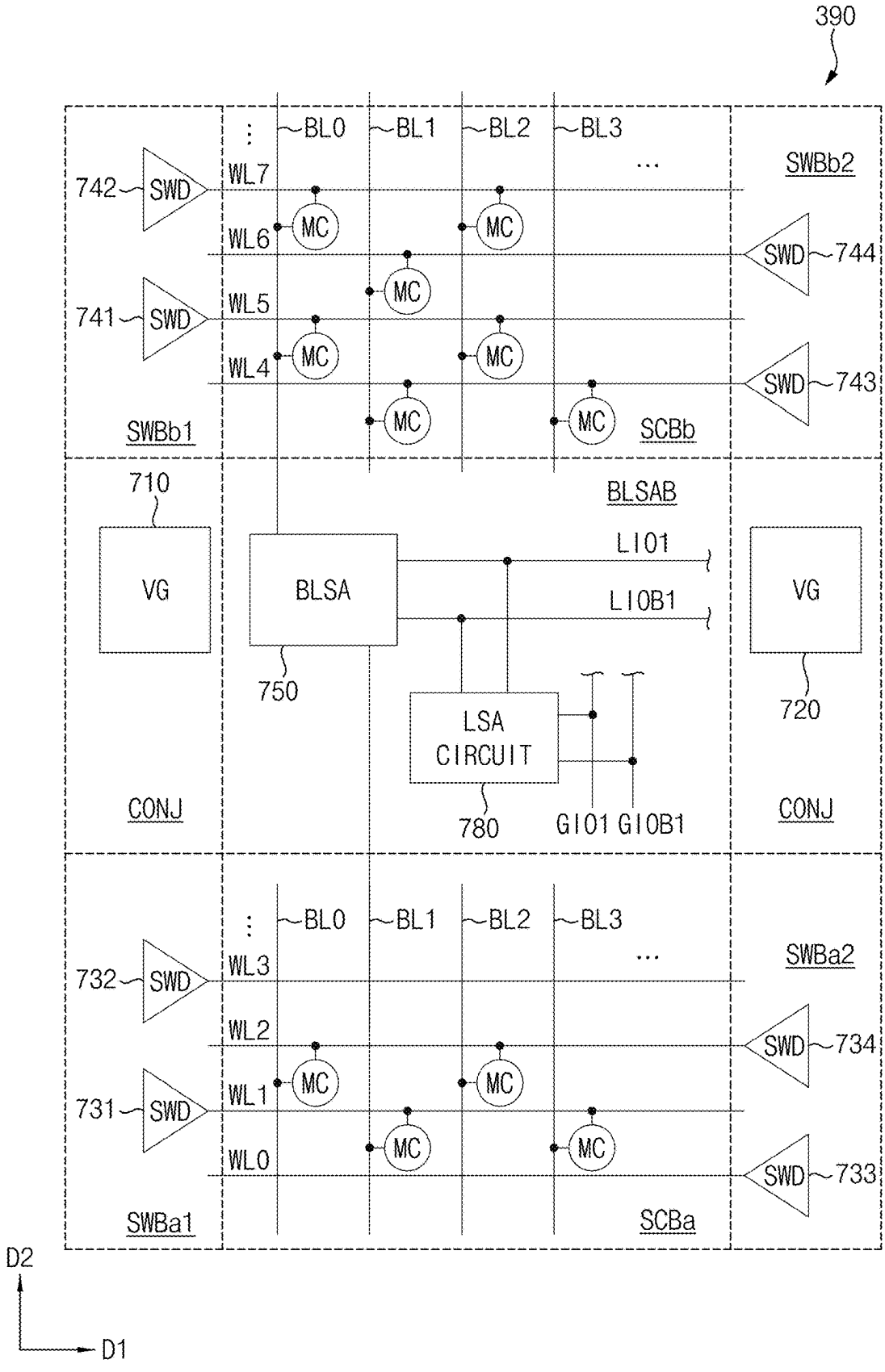

390
BL0
BL1
BL2
BL3
WL7
WL6
WL5
WL4
742
741
SWD
MC
SWBb2
744
743
SWBb1
SCBb
710
VG
BLSAB
BLSA
LIO1
LIOB1
750
LSA CIRCUIT
780
GIO1
GIOB1
720
CONJ
WL3
WL2
WL1
WL0
732
731
SWBa2
734
733
SWBa1
SCBa
D2
D1

FIG. 17

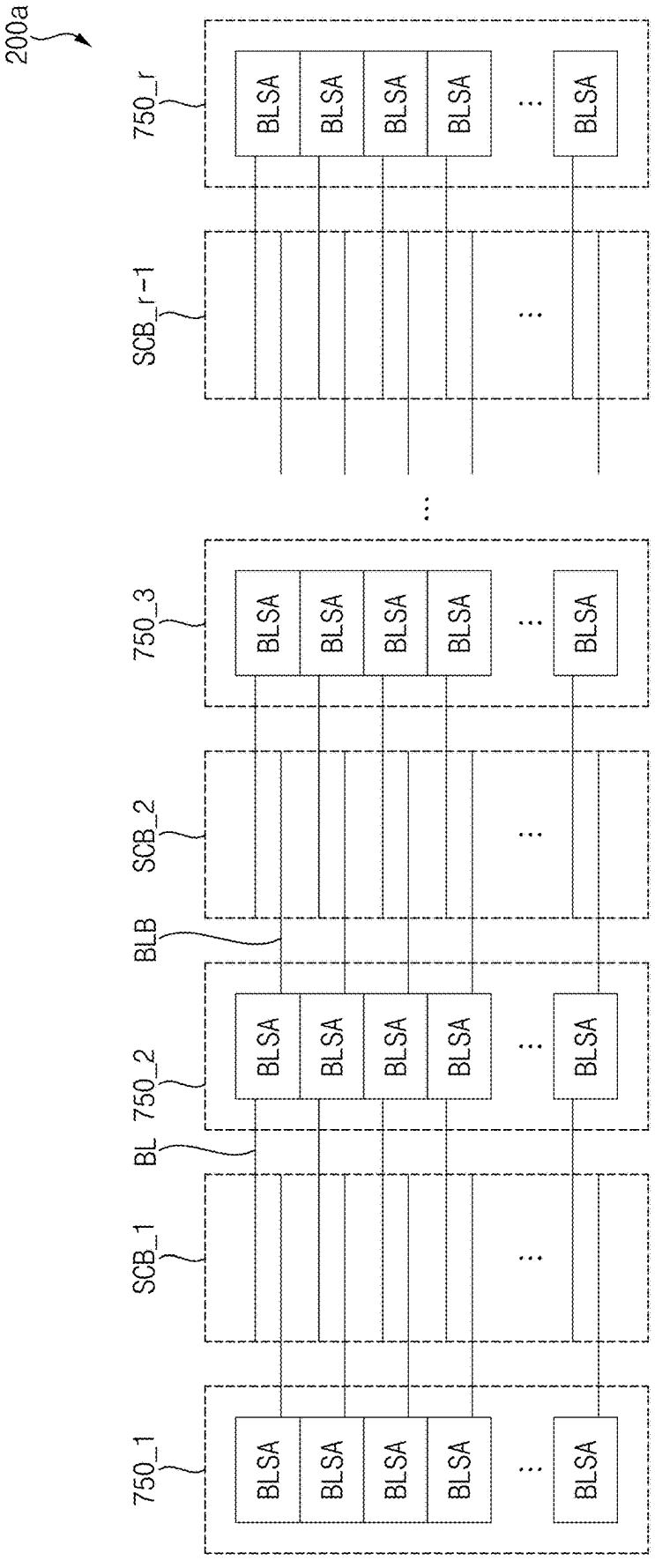


FIG. 18

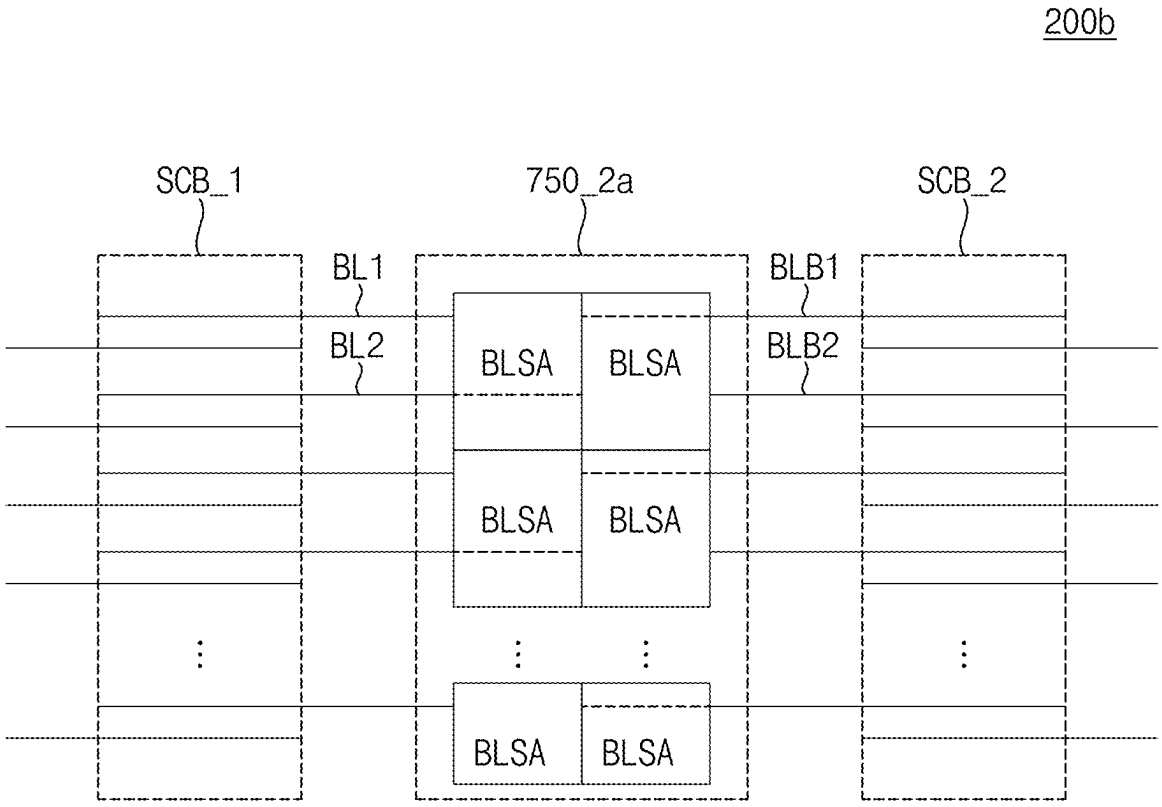

200b
SCB_1
750_2a
SCB_2
BL1
BL2
BLB1
BLB2
BLSA
BLSA
BLSA
BLSA
BLSA
BLSA

FIG. 19

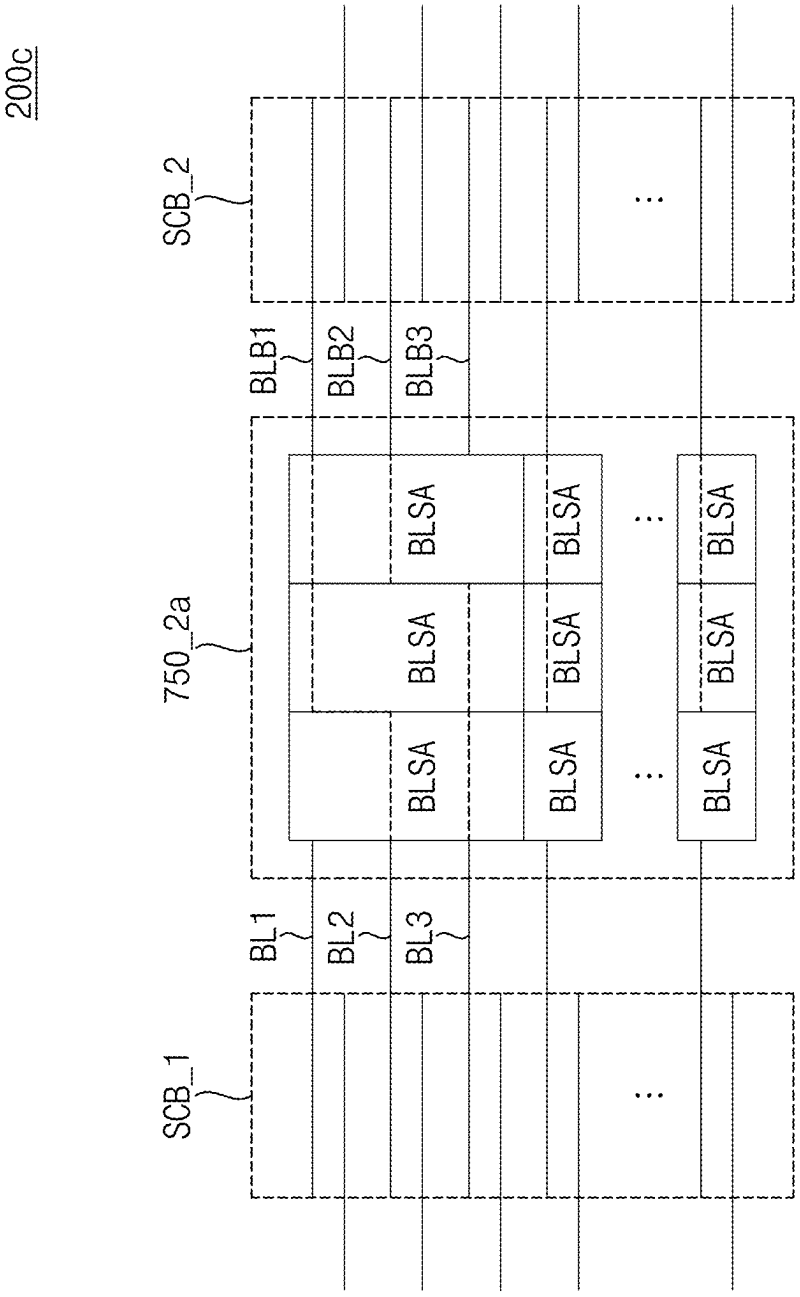

200c
SCB_2
BLB1
BLB2
BLB3
750_2a
BLSA
BLSA
BLSA
BLSA
BLSA
BLSA
BLSA
BLSA
BLSA
BL1
BL2
BL3
SCB_1

FIG. 20

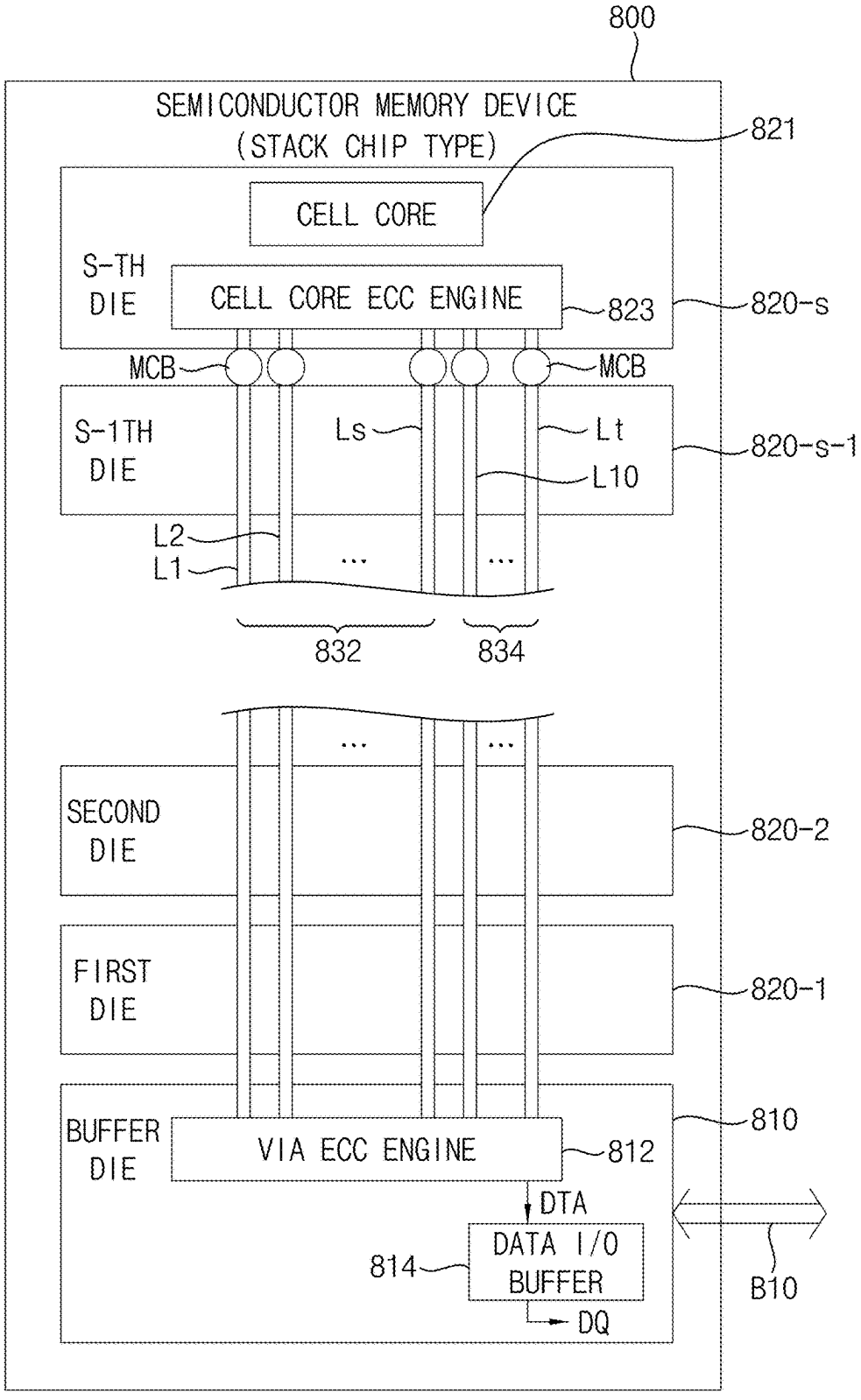
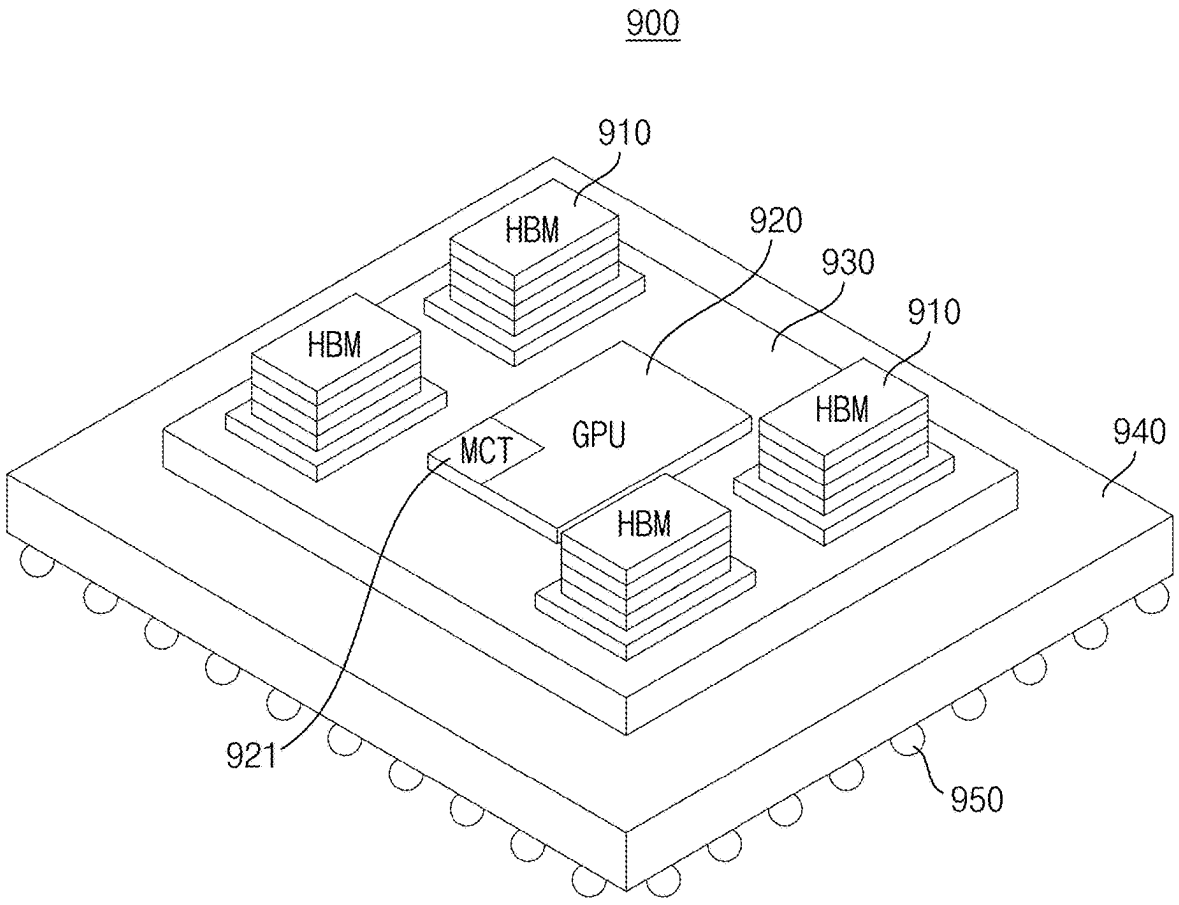

800
SEMICONDUCTOR MEMORY DEVICE
(STACK CHIP TYPE)
821
CELL CORE
S-TH
DIE
CELL CORE ECC ENGINE
823
820-s
MCB
MCB
S-1TH
DIE
Ls
Lt
L10
820-s-1
L2
L1
...
...
832
834
...
...
SECOND
DIE
820-2
FIRST
DIE
820-1
BUFFER
DIE
VIA ECC ENGINE
812
810
DTA
DATA I/O
BUFFER
814
B10
DQ

FIG. 21



BIT-LINE SENSE AMPLIIFIER AND SEMICONDUCTOR MEMORY DEVICE INCLUDING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application claims the benefit of priority under 35 U.S.C. § 119 to Korean Patent Application No. 10-2024-0019312, filed on Feb. 8, 2024, in the Korean Intellectual Property Office, the disclosure of which is incorporated by reference herein in its entirety.

BACKGROUND

[0002] The present disclosure relates to memories, and more particularly to a bit-line sense amplifier capable of reducing power consumption and a semiconductor memory device including the bit-line sense amplifier.

[0003] A semiconductor memory device may be used to store data. Random access memory (RAM) is a volatile memory device that loses data in the absence of power. A RAM is mainly used as a main memory device of a computer. A dynamic random access memory (DRAM) is a type of RAM that is volatile and made up of memory cells. For example, a DRAM uses a transistor and a capacitor per cell. To detect data stored in the memory cells of a DRAM, bit-lines and complementary bit-lines are precharged to a precharge voltage, a charge sharing operation is performed, and a difference between a voltage level of the bit-line and a voltage level of complementary bit-line results. A sense amplifier then receives and amplifies the voltage difference between the bit-line and the complementary bit-line to detect the data stored in the memory cell.

[0004] Due to recent developments in the electronics industry, there is an increasing demand for higher functionality, higher speed, and smaller sized electronic components. Accordingly, to increase the degree of integration of the semiconductor memory device, an area of a memory cell region and a peripheral circuit region have been reduced. In addition, efforts have been made to increase the amount of data processed to speed up the data processing time.

SUMMARY

[0005] Example embodiments may provide a bit-line sense amplifier capable of reducing power consumption.

[0006] Example embodiments may provide a semiconductor memory device including a bit-line sense amplifier capable of reducing power consumption.

[0007] According to example embodiments, a semiconductor memory device includes a first memory cell connected to a first word-line and a bit-line, a second memory cell connected to a second word-line and a complementary bit-line, and a bit-line sense amplifier connected to the bit-line and the complementary bit-line. The bit-line sense amplifier includes an amplifying circuit connected to the bit-line, the complementary bit-line, a sensing bit-line, a complementary sensing bit-line, an offset cancellation circuit, an equalizer and an isolation circuit. The amplifying circuit includes a P-type amplifier and an N-type amplifier, senses a voltage difference between the bit-line and the complementary bit-line based on a first control signal and a second control signal, and adjusts a voltage of the sensing bit-line and the complementary sensing bit-line based on the voltage difference. The offset cancellation circuit connects the bit-line and the complementary bit-line to the complementary sensing bit-line and the sensing bit-line, respectively, based on an offset cancellation signal. The equalizer provides a precharge voltage to the sensing bit-line and the complementary sensing bit-line based on equalizing signal. The isolation circuit is connected between the bit-line and the sensing bit-line and between the complementary bit-line and the complementary sensing bit-line, and connects the sensing bit-line and the complementary sensing bit-line equalized with the precharge voltage to the bit-line and the complementary bit-line, respectively, based on an isolation signal.

[0008] According to example embodiments, a semiconductor memory device includes a first memory cell, a second memory cell, a bit-line sense amplifier and a timing control circuit. The first memory cell is connected to a first word-line and a bit-line. The second memory cell connected to a second word-line and a complementary bit-line. The bit-line sense amplifier is connected to the bit-line and the complementary bit-line, senses a voltage difference between the bit-line and the complementary bit-line, and amplifies the voltage difference. The timing control circuit controls an operation of the bit-line sense amplifier based on internal command signals. The bit-line sense amplifier includes an amplifying circuit, an offset cancellation circuit, an equalizer and an isolation circuit. The amplifying circuit includes a P-type amplifier connected to the bit-line and the complementary bit-line and an N-type amplifier connected to a sensing bit-line and a complementary sensing bit-line, senses the voltage difference between the bit-line and the complementary bit-line based on a first control signal and a second control signal, and adjusts a voltage of the sensing bit-line and the complementary sensing bit-line based on the voltage difference. The offset cancellation circuit connects the bit-line and the complementary bit-line to the complementary sensing bit-line and the sensing bit-line, respectively, based on an offset cancellation signal. The equalizer provides a precharge voltage to the sensing bit-line and the complementary sensing bit-line based on an equalizing signal. The isolation circuit is connected between the bit-line and the sensing bit-line and between the complementary bit-line and the complementary sensing bit-line, and connects the sensing bit-line and the complementary sensing bit-line equalized with the precharge voltage to the bit-line and the complementary bit-line, respectively, based on an isolation signal.

[0009] According to example embodiments, a semiconductor memory device includes a first memory cell connected to a first word-line and a bit-line, a second memory cell connected to a second word-line and a complementary bit-line, and a bit-line sense amplifier connected to the bit-line and the complementary bit-line. The bit-line sense amplifier includes an amplifying circuit connected to a bit-line, a complementary bit-line, a sensing bit-line, a complementary sensing bit-line, an offset cancellation circuit, an equalizer and an isolation circuit. The amplifying circuit includes a P-type amplifier and an N-type amplifier, senses a voltage difference between the bit-line and the complementary bit-line based on a first control signal and a second control signal, and adjusts a voltage of the sensing bit-line and the complementary sensing bit-line based on the voltage difference. The offset cancellation circuit connects the bit-line and the complementary bit-line to the complementary sensing bit-line and the sensing bit-line, respec-

tively, based on an offset cancellation signal. The equalizer provides a precharge voltage to the sensing bit-line and the complementary sensing bit-line based on an equalizing signal. The isolation circuit is connected between the bit-line and the sensing bit-line and between the complementary bit-line and the complementary sensing bit-line, and connects the sensing bit-line and the complementary sensing bit-line equalized with the precharge voltage to the bit-line and the complementary bit-line, respectively, based on an isolation signal. The P-type amplifier is connected to a first supply line at a first node at which the first control signal is applied, is connected to the bit-line at a third node, and is connected to the complementary bit-line at a fourth node, The N-type amplifier is connected to a second supply line at a second node at which the second control signal is applied, is connected to the sensing bit-line at a fifth node and is connected to the complementary sensing bit-line at a sixth node,. The equalizer includes a first equalizing transistor and a second equalizing transistor. The first equalizing transistor is connected between a first precharge voltage node at which the precharge voltage is applied and the fifth node, and includes a gate configured to receive the equalizing signal. The second equalizing transistor is connected between a second precharge voltage node at which the precharge voltage is applied and the sixth node, and includes a gate configured to receive the equalizing signal. The isolation circuit includes a first isolation transistor and a second isolation transistor. The first isolation transistor is connected between the third node and the fifth node, and includes a gate configured to receive the isolation signal. The second isolation transistor is connected between the fourth node and the sixth node, and includes a gate configured to receive the isolation signal.

[0010] Accordingly, in the bit-line sense amplifier according to example embodiments, the equalizer provides the precharge voltage to the sensing bit-line and the complementary sensing bit-line, the isolation circuit connected the sensing bit-line and the complementary sensing bit-line that are precharged to the bit-line and the complementary bit-line, respectively, and each of the bit-line and the complementary bit-line is connected to a drain of respective one of the isolation transistors. Therefore, a voltage level of each of the bit-line and the complementary bit-line may swing between a power supply voltage and the ground voltage when the isolation signal, which is applied to gates of the isolation transistors, has a voltage level of the power supply voltage. Accordingly, the bit-line sense amplifier may reduce power consumption.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Example embodiments of the present disclosure will be described below in more detail with reference to the accompanying drawings.

[0012] FIG. **1** is a block diagram illustrating a memory system according to example embodiments.

[0013] FIG. **2** is a block diagram illustrating an example of a memory controller in FIG. **1** according to example embodiments.

[0014] FIG. **3** is a block diagram illustrating an example of a semiconductor memory device in the memory system of FIG. **1** according to example embodiments.

[0015] FIG. **4** illustrates an example of a first bank array in the semiconductor memory device of FIG. **3**.

[0016] FIG. **5** is a block diagram illustrating an example of a timing control circuit in the semiconductor memory device of FIG. **3** according to example embodiments.

[0017] FIG. **6** is a circuit diagram illustrating an example of a bit-line sense amplifier according to example embodiments.

[0018] FIG. **7** is a diagram illustrating a layout of a bit-line sense amplifier in FIG. **6** according to example embodiments.

[0019] FIG. **8** illustrates an example of a bit-line layout connected to the bit-line sense amplifier

[0020] in FIG. **7** according to example embodiments.

[0021] FIG. **9** is a circuit diagram illustrating an example of a bit-line sense amplifier according to example embodiments.

[0022] FIG. **10** shows an equivalent circuit of the bit-line sense amplifier in FIG. **6** according to example embodiments.

[0023] FIG. **11** is a flowchart for describing operations of the bit-line sense amplifier in FIG. **10** according to example embodiments.

[0024] FIGS. **12**A, **12**B, **12**C, **12**D, and **12**E are circuit diagrams for describing operations of the bit-line sense amplifier in FIG. **10** according to example embodiments.

[0025] FIG. **13** is a graph for describing operations of the bit-line sense amplifier in FIG. **10** according to example embodiments.

[0026] FIG. **14** is a timing diagram for describing operations of the bit-line sense amplifier in FIG. **6** according to example embodiments.

[0027] FIG. **15** illustrates an example of a first bank array in the semiconductor memory device of FIG. **3** according to example embodiments.

[0028] FIG. **16** illustrates a portion of the first bank array in FIG. **15** according to example embodiments.

[0029] FIG. **17** is a block diagram illustrating a semiconductor memory device that employs a bit-line sense amplifier according to example embodiments.

[0030] FIGS. **18** and **19** are diagrams illustrating a semiconductor memory device that employs a bit-line sense amplifier according to example embodiments.

[0031] FIG. **20** is a block diagram illustrating a semiconductor memory device according to example embodiments.

[0032] FIG. **21** is a configuration diagram illustrating a semiconductor package including the stacked memory device according to example embodiments.

DETAILED DESCRIPTION

[0033] Various example embodiments of the present disclosure will be described more fully hereinafter with reference to the accompanying drawings, in which example embodiments are shown.

[0034] FIG. **1** is a block diagram illustrating a memory system according to example embodiments.

[0035] Referring to FIG. **1**, a memory system **80** may include a memory controller **100** and a semiconductor memory device **200**.

[0036] The memory controller **100** may control overall operation of the memory system **80**. The memory controller **100** may control overall data exchange between an external host and the semiconductor memory device **200**. For example, the memory controller **100** may write data in the

semiconductor memory device **200** or read data from the semiconductor memory device **200** in response to request from the host.

[0037] In addition, the memory controller **100** may issue operation commands to the semiconductor memory device **200** for controlling the semiconductor memory device **200**. In some example embodiments, the semiconductor memory device **200** is a memory device including dynamic memory cells such as a DRAM, double data rate 5 (DDR5) synchronous DRAM (SDRAM), a DDR6 SDRAM or the like.

[0038] The memory controller **100** may transmit a clock signal CK (the clock signal CK may be referred to as a command clock signal), a command CMD, and an address (signal) ADDR to the semiconductor memory device **200**. Herein, for convenience of description, the terms of a clock signal CK, a command CMD, and an address ADDR and the terms of clock signals CK, commands CMD, and addresses ADDR may be used interchangeably. The memory controller **100** may transmit a data strobe signal DQS to the semiconductor memory device **200** when the memory controller **100** writes data signal DQ in the semiconductor memory device **200**. The semiconductor memory device **200** may transmit a data strobe signal DQS to the memory controller **100** when the memory controller **100** reads data signal DQ from the semiconductor memory device **200**. The address ADDR may be accompanied by the command CMD and the address ADDR may be referred to as an access address.

[0039] The memory controller **100** may include a central processing unit (CPU) **135** that controls overall operation of the memory controller **100**.

[0040] The semiconductor memory device **200** may include a memory cell array **310** that stores the data signal DQ and a control logic circuit **210**.

[0041] The control logic circuit **210** may control operations of the semiconductor memory device **200**. The memory cell array **310** may include a plurality of memory cell rows and each of the memory cell rows may include a plurality of (volatile) memory cells. The memory cell array **310** may include a bit-line sense amplifier BLSA **750**.

[0042] A memory cell MC may be connected to a word-line WL and a bit-line BL and the bit-line sense amplifier **750** may be connected to the memory cells MC through the bit-line BL and a complementary bit-line BLB.

[0043] The bit-line sense amplifier **750** may include an amplifying circuit that includes a P-type amplifier connected to the bit-line and BL and the complementary bit-line BLB and an N-type amplifier connected to a sensing bit-line and a complementary sensing bit-line, and an isolation circuit connected between the bit-line and the sensing bit-line and between the complementary bit-line and the complementary sensing bit-line. The isolation circuit may connect the sensing bit-line and the complementary sensing bit-line to the bit-line and the complementary bit-line, respectively, based on an isolation signal. Because the bit-line and the complementary bit-line are connected to drains of isolation transistors in the isolation circuit, a voltage level of each of the bit-line and the complementary bit-line may swing between a power supply voltage and a ground voltage when the isolation signal, which is applied to gates of the isolation transistors, has a voltage level of the power supply voltage.

[0044] The semiconductor memory device **200** performs a refresh operation periodically due to charge leakage of memory cells storing data. Due to scale down of the manufacturing process of the semiconductor memory device **200**, the storage capacitance of the memory cell is decreased and the refresh period is shortened. The refresh period is further shortened because the entire refresh time is increased as the memory capacity of the semiconductor memory device **200** is increased.

[0045] To compensate degradation of adjacent memory cells due to the intensive access to a particular row or a hammer address, a target row refresh (TRR) scheme was adopted and an in-memory refresh scheme is developed to reduce the burden of the memory controller. The memory controller is totally responsible for the hammer refresh operation in the TRR scheme and the semiconductor memory device is totally responsible for the hammer refresh operation in the in-memory refresh scheme.

[0046] FIG. **2** is a block diagram illustrating an example of the memory controller in FIG. **1** according to example embodiments.

[0047] Referring to FIG. **2**, the memory controller **100** may include the CPU **135**, a refresh management (RFM) control logic **170**, a refresh logic **140**, a host interface **150**, a scheduler **155** and a memory interface **160** which are connected to each other through a bus **105**.

[0048] The CPU **135** may control overall operation of the memory controller **100**. The CPU **135** may control the RFM control logic **170**, the refresh logic **140**, the host interface **150**, the scheduler **155** and the memory interface **160** through the bus **105**.

[0049] The refresh logic **140** may generate auto refresh command for refreshing memory cells of the plurality of memory cell rows based on a refresh interval of the semiconductor memory device **200**.

[0050] The host interface **150** may perform interfacing with a host. The memory interface **160** may perform interfacing with the semiconductor memory device **200**.

[0051] The scheduler **155** may manage scheduling and transmission of sequences of commands generated in the memory controller **100**.

[0052] The RFM control logic **170** may generate a refresh management command for a memory cell row associated with a row hammer, from among a plurality of memory cell rows of the semiconductor memory device **200** and may apply the refresh management command to the semiconductor memory device **200** through the memory interface **160** such that the semiconductor memory device **200** performs a hammer refresh operation on one or more victim memory cell rows which are physically adjacent to a memory cell row corresponding to a hammer address.

[0053] FIG. **3** is a block diagram illustrating an example of the semiconductor memory device in the memory system of FIG. **1** according to example embodiments.

[0054] Referring to FIG. **3**, the semiconductor memory device **200** may include the control logic circuit **210**, an address register **220**, a bank control logic **230**, a refresh control circuit **400**, a row address multiplexer **240**, a column address latch **250**, a row decoder **260**, a column decoder **270**, the memory cell array **310**, a sense amplifier unit **285**, an input/output (I/O) gating circuit **290**, an error correction code (ECC) engine **350**, a clock buffer **225**, a strobe signal generator **235**, a voltage generator **385**, a timing control circuit **460** and a data I/O buffer **320**.

[0055] The memory cell array **310** may include first through sixteenth bank arrays **310***a*~**310***p*. The row decoder **260** may include first through sixteenth row decoders

260*a*~**260***p* respectively coupled to the first through sixteenth bank arrays **310***a*~**310***p*, the column decoder **270** may include first through sixteenth column decoders **270***a*~**270***p* respectively coupled to the first through sixteenth bank arrays **310***a*~**310***p*, and the sense amplifier unit **285** may include first through sixteenth sense amplifiers **285***a*~**285***p* respectively coupled to the first through sixteenth bank arrays **310***a*~**310***p*.

[0056] The first through sixteenth bank arrays **310***a*~**310***p*, the first through sixteenth row decoders **260***a*~**260***p*, the first through sixteenth column decoders **270***a*~**270***p* and the first through sixteenth sense amplifiers **285***a*~**285***p* may form first through sixteenth banks. Each of the first through sixteenth bank arrays **310***a*~**310***p* may include a plurality of memory cells MC formed at intersections of a plurality of word-lines WL and a plurality of bit-lines BL.

[0057] The address register **220** may receive the address ADDR including a bank address BANK_ADDR, a row address ROW_ADDR and a column address COL_ADDR from the memory controller **100**. The address register **220** may provide the received bank address BANK_ADDR to the bank control logic **230**, may provide the received row address ROW_ADDR to the row address multiplexer **240**, and may provide the received column address COL_ADDR to the column address latch **250**.

[0058] The bank control logic **230** may generate bank control signals in response to the bank address BANK_ADDR. One of the first through sixteenth row decoders **260***a*~**260***p* corresponding to the bank address BANK_ADDR may be activated in response to the bank control signals, and one of the first through sixteenth column decoders **270***a*~**270***p* corresponding to the bank address BANK_ADDR may be activated in response to the bank control signals.

[0059] The row address multiplexer **240** may receive the row address ROW_ADDR from the address register **220**, and may receive a refresh row address REF_ADDR from the refresh control circuit **400**. The row address multiplexer **240** may selectively output the row address ROW_ADDR or the refresh row address REF_ADDR as a row address SRA. The row address SRA that is output from the row address multiplexer **240** may be applied to the first through sixteenth row decoders **260***a*~**260***p*.

[0060] The refresh control circuit **400** may sequentially increase or decrease the refresh row address REF_ADDR in a normal refresh mode in response to first and second refresh control signals IREF**1** and IREF**2** from the control logic circuit **210**.

[0061] The activated one of the first through sixteenth row decoders **260***a*~**260***p*, by the bank control logic **230**, may decode the row address SRA that is output from the row address multiplexer **240**, and may activate a word-line WL corresponding to the row address SRA. For example, the activated row decoder may apply a word-line driving voltage to the word-line corresponding to the row address SRA.

[0062] The column address latch **250** may receive the column address COL_ADDR from the address register **220**, and may temporarily store the received column address COL_ADDR. In some example embodiments, in a burst mode, the column address latch **250** may generate column address COL_ADDR' that increment from the received column address COL_ADDR. The column address latch **250** may apply the temporarily stored or generated column address COL_ADDR' to the first through sixteenth column decoders **270***a*~**270***p*.

[0063] The activated one of the first through sixteenth column decoders **270***a*~**270***p* may activate a sense amplifier corresponding to the bank address BANK_ADDR and the column address COL_ADDR through the I/O gating circuit **290**.

[0064] The I/O gating circuit **290** may include a circuitry for gating input/output data, and may further include input data mask logic, read data latches for storing data that is output from the first through sixteenth bank arrays **310***a*~**310***p*, and write drivers for writing data to the first through sixteenth bank arrays **310***a*~**310***p*.

[0065] Codeword CW read from a selected one bank array of the first through sixteenth bank arrays **310***a*~**310***p* may be sensed by a sense amplifier coupled to the selected one bank array from which the data is to be read, and may be stored in the read data latches. The codeword CW stored in the read data latches may be provided to the data I/O buffer **320** as data DTA after ECC decoding is performed on the codeword CW by the ECC engine **350**. The data I/O buffer **320** may convert the data DTA into the data signal DQ and may transmit the data signal DQ along with the data strobe signal DQS to the memory controller **100**.

[0066] The data signal DQ to be written in a selected one bank array of the first through sixteenth bank arrays **310***a*~**310***p* may be provided to the data I/O buffer **320** from the memory controller **100**. The data I/O buffer **320** may convert the data signal DQ to the data DTA and may provide the data DTA to the ECC engine **350**. The ECC engine **350** may perform an ECC encoding on the data DTA to generate parity bits, and the ECC engine **350** may provide the codeword CW including the data DTA and the parity bits to the I/O gating circuit **290**. The I/O gating circuit **290** may write the codeword CW in a target page in the selected one bank array through the write drivers.

[0067] The data I/O buffer **320** may provide the data signal DQ from the memory controller **100** to the ECC engine **350** by converting the data signal DQ to the data DTA in a write operation of the semiconductor memory device **200** and may convert the data DTA to the data signal DQ from the ECC engine **350** and may transmit the data signal DQ and the data strobe signal DQS to the memory controller **100** in a read operation of the semiconductor memory device **200**.

[0068] The ECC engine **350** may perform an ECC encoding on the data DTA and may perform an ECC decoding on the codeword CW based on a second control signal CTL**2** from the control logic circuit **210**.

[0069] The clock buffer **225** may receive the clock signal CK, may generate an internal clock signal ICK by buffering the clock signal CK, and may provide the internal clock signal ICK to circuit components processing the command CMD and the address ADDR.

[0070] The strobe signal generator **235** may receive the clock signal CK, may generate the data strobe signal DQS based on the clock signal CK and may provide the data strobe signal DQS to the data I/O buffer **320**.

[0071] The voltage generator **385** may generate an internal power supply voltage VINTA and a precharge voltage VBL based on a power supply voltage VDD received from an external device (i.e. the memory controller **100**) and may provide the internal power supply voltage VINTA and the precharge voltage VBL to the memory cell array **310**. For

example, a voltage level of the internal power supply voltage VINTA may be less than a voltage level of the power supply voltage VDD.

[0072] The control logic circuit **210** may control operations of the semiconductor memory device **200**. For example, the control logic circuit **210** may generate control signals for the semiconductor memory device **200** in order to perform a write operation, a read operation, and a refresh operation. The control logic circuit **210** may include a command decoder **211** that decodes the command CMD received from the memory controller **100** and a mode register **212** that sets an operation mode of the semiconductor memory device **200**.

[0073] For example, the command decoder **211** may generate the control signals corresponding to the command CMD by decoding a write enable signal, a row address strobe signal, a column address strobe signal, a chip select signal, etc. The control logic circuit **210** may provide a first control signal CTL**1** to the I/O gating circuit and the second control signal CTL**2** to the ECC engine **350**. In addition, the command decoder **211** may generate internal command signals including the first refresh control signal IREF**1**, the second refresh control signal IREF**2**, an active signal IACT, a precharge signal IPRE, a read signal IRD and a write signal IWR by decoding the command CMD.

[0074] The timing control circuit **460** may receive the active signal IACT, the precharge signal IPRE, the read signal IRD, the write signal IWR, a decoded row address DRA and a decoded column address DCA and may generate a word-line control signal WCTL for controlling word-lines WL and a bit-line control signal BCTL for controlling bit-lines BL, and may provide the word-line control signal WCTL and the bit-line control signal BCTL to the memory cell array **310**. The decoded row address DRA may be generated from the row decoder **260** and the decoded column address DCA may be generated from the column decoder **270**.

[0075] FIG. **4** illustrates an example of the first bank array in the semiconductor memory device of FIG. **3**.

[0076] Referring to FIG. **4**, the first bank array **310***a* may include a plurality of word-lines WL**0**~WLm−1 (where, m is a natural number greater than two), a plurality of bit-lines BL**0**~BLn−1 (where, n is a natural number greater than two), and a plurality of memory cells MC disposed at intersections between the word-lines WL**0**~WLm−**1** and the bit-lines BL**0**~BLn−1. Each of the memory cells MCs includes a cell transistor coupled to each of the word-lines WL**0**~WLm−1 and each of the bit-lines BL**0**~BLn−1 and a cell capacitor coupled to the cell transistor. Each of the memory cells MC may have a DRAM cell structure. Each of the word-lines WL**0**~WLm−1 extends in a first direction D**1** and each of the bit-lines BL**0**~BLn−1 extends in a second direction D**2** crossing the first direction D**1**.

[0077] The word-lines WL**0**~WLm−1 coupled to the plurality of memory cells MC may be referred to as rows of the first bank array **310***a* and the bit-lines BL**0**~BLn−1 coupled to the plurality of memory cells MC may be referred to as columns of the first bank array **310***a*.

[0078] FIG. **5** is a block diagram illustrating an example of the timing control circuit in the semiconductor memory device of FIG. **3** according to example embodiments.

[0079] Referring to FIG. **5**, the timing control circuit **460** may include a first control signal generator **465** and a second control signal generator **470**.

[0080] The first control signal generator **465** may generate the word-line control signal WCTL including first and second word-line control signals PXi and PXiB to control a word-line based on the internal command signals IACT, IWR and IRD corresponding to the command CMD, and the decoded row address DRA. In addition, the first control signal generator **465** may provide the first and second word-line control signals PXi and PXiB to the memory cell array **310**.

[0081] The second control signal generator **470** may generate the bit-line control signal BCTL including a first control signal LA, a second control signal LAB, an equalizing signal PEQ, an offset cancellation signal OC and an isolation signal ISO to control an operation of the bit-line sense amplifier connected to the selected memory cell, in response to the internal command signals IACT and IPRE and the decoded column address DCA, and may provide the bit-line control signal BCTL to the memory cell array **310**.

[0082] FIG. **6** is a circuit diagram illustrating an example of a bit-line sense amplifier according to example embodiments.

[0083] In FIG. **6**, a bit-line sense amplifier **750**, a first memory cell MC**1** and a second memory cell MC**2** are illustrated for convenience of explanation.

[0084] The bit-line sense amplifier **750**, the first memory cell MC**1** and the second memory cell MC**2** may constitute a semiconductor memory device.

[0085] Referring to FIG. **6**, the first memory cell MC**1** may include a cell transistor CT**1** coupled to a first word-line WLi and a bit-line BL, and a cell capacitor CC**1** coupled between the cell transistor CT**1** and a ground voltage or a predetermined voltage (e.g., ½ VDD) and the second memory cell MC**2** may include a cell transistor CT**2** coupled to a second word-line WLj and a complementary bit-line BLB, and a cell capacitor CC**2** coupled between the cell transistor CT**2** and the ground voltage or the predetermined voltage.

[0086] The bit-line sense amplifier **750** may include an amplifying circuit **760** and **765**, an isolation circuit **771** and **772**, an offset cancellation circuit **775** and an equalizer **781** and **782**.

[0087] The amplifying circuit **760** and **765** may be connected to the bit-line BL and the complementary bit-line BLB, may sense a voltage difference between the bit-line BL and the complementary bit-line BLB based on the first control signal LA and the second control signal LAB, and may adjust a voltage of a sensing bit-line SBL and a complementary sensing bit-line SBLB based on the voltage difference.

[0088] The amplifying circuit **760** and **765** may include a P-type amplifier **760** and an N-type amplifier **765**.

[0089] The P-type amplifier **760** may be connected to a first supply line **751** receiving the first control signal LA at a first node N**1**, may be connected to the bit-line BL at a third node N**3** and may be connected to the complementary bit-line BLB at a fourth node N**4**. The N-type amplifier **765** may be connected to a second supply line **752** receiving the second control signal LAB at a second node N**2**, may be connected to the sensing bit-line SBL at a fifth node N**5** and may be connected to the complementary sensing bit-line SBLB at a sixth node N**6**.

[0090] The P-type amplifier **760** may include a first p-channel metal-oxide semiconductor (PMOS) transistor MP**1** and a second PMOS transistor MP**2**. The N-type

amplifier **765** may include a first n-channel metal-oxide semiconductor (NMOS) transistor MN**1** and a second NMOS transistor MN**2**.

[0091] The first PMOS transistor MP**1** may be connected between the first supply line **751** (i.e., the first node N**1**) and the third node N**3**, and may include a gate connected to the complementary bit-line BLB at the fourth node N**4**. The second PMOS transistor MP**2** may be connected between the first supply line **751** (i.e., the first node N**1**) and the fourth node N**4**, and may include a gate connected to the bit-line BL at the third node N**3**.

[0092] The first NMOS transistor MN**1** may be connected between the second supply line **752** (i.e., the second node N**2**) and the fifth node N**5**, and may include a gate connected to the complementary bit-line BLB at the fourth node N**4**. The second NMOS transistor MN**2** may be connected between the second supply line **752** (i.e., the second node N**2**) and the sixth node N**6**, and may include a gate connected to the bit-line BL at the third node N**3**.

[0093] The offset cancellation circuit **775** may connect the sensing bit-line SBL and the complementary sensing bit-line SBLB to the complementary bit-line BLB and the bit-line BL, respectively, based on the offset cancellation signal OC.

[0094] The offset cancellation circuit **775** may include a first offset cancellation transistor OC_**1** and a second offset cancellation transistor OC_**2**. The first offset cancellation transistor OC_**1** may be connected between the fifth node N**5** and the fourth node N**4**, and may include a gate to receive the offset cancellation signal OC. The second offset cancellation transistor OC_**2** may be connected between the sixth node N**6** and the third node N**3**, and may include a gate to receive the offset cancellation signal OC.

[0095] The equalizer **781** and **782** may equalize the sensing bit-line SBL and the complementary sensing bit-line SBLB by providing the precharge voltage VBL to the sensing bit-line SBL and the complementary sensing bit-line SBLB, based on the equalizing signal PEQ.

[0096] The equalizer **781** and **782** may include a first equalizing transistor EQ_**1** and a second equalizing transistor EQ_**2**. The first equalizing transistor EQ_**1** may be connected between the precharge voltage VBL (i.e., a first precharge voltage node at which the precharge voltage VBL is applied) and the fifth node N**5**, and may include a gate to receive the equalizing signal PEQ. The second equalizing transistor EQ_**2** may be connected between the precharge voltage VBL (i.e., a second precharge voltage node at which the precharge voltage VBL is applied) and the sixth node N**6**, and may include a gate to receive the equalizing signal PEQ. The first equalizing transistor EQ_**1** may provide the precharge voltage VBL to the fifth node N**5** (i.e., the sensing bit-line SBL) based on the equalizing signal PEQ. The second equalizing transistor EQ_**2** may provide the precharge voltage VBL to the sixth node N**6** (i.e., the complementary sensing bit-line SBLB) based on the equalizing signal PEQ.

[0097] The isolation circuit **771** and **772** may connect/disconnect the sensing bit-line SBL and the complementary sensing bit-line SBLB to/from the bit-line BL and the complementary bit-line BLB, respectively, based on the isolation signal ISO.

[0098] The isolation circuit **771** and **772** may include a first isolation transistor ISO_**1** and a second isolation transistor ISO **2**. The first isolation transistor ISO_**1** may be connected between the fifth node N**5** and the third node N**3**, and may include a gate to receive the isolation signal ISO. The second isolation transistor ISO_**2** may be connected between the sixth node N**6** and the fourth node N**4**, and may include a gate to receive the isolation signal ISO. The first isolation transistor ISO_**1** may connect/disconnect the sensing bit-line SBL to/from the bit-line BL based on the isolation signal ISO. The second isolation transistor ISO_**2** may connect/disconnect the complementary sensing bit-line SBLB to/from the complementary bit-line BLB based on the isolation signal ISO.

[0099] In example embodiment, because each of the bit-line BL and the complementary bit-line BLB is connected to a drain of respective one of the first isolation transistor ISO_**1** and the second isolation transistor ISO_**2**, a voltage level of each of the bit-line BL and the complementary bit-line BLB may swing between a power supply voltage (e.g., VDD) and the ground voltage VSS when the isolation signal ISO, which is applied to gates of the first isolation transistor ISO **1** and the second isolation transistor ISO_**2**, has a voltage level of the power supply voltage.

[0100] In contrast, because each of the bit-line BL and the complementary bit-line BLB is connected to a source of respective one of isolation transistors in the conventional bit-line sense amplifier, a voltage level of each of the bit-line BL and the complementary bit-line BLB swings between a power supply voltage and the ground voltage VSS when the isolation signal, which is applied to gates of the isolation transistors, has a voltage level corresponding to summed result of the power supply voltage and a threshold voltage of each of the isolation transistors.

[0101] Therefore, the bit-line sense amplifier **750** may reduce power consumption by decreasing a voltage level of the isolation signal ISO and the N-type amplifier **765** may operate dominantly over the P-type amplifier **760** in an offset cancellation operation and a charge sharing operation because the first isolation transistor ISO_**1** and the second isolation transistor ISO_**2** disconnect the sensing bit-line SBL and the complementary sensing bit-line SBLB from the bit-line BL and the complementary bit-line BLB, respectively, in the offset cancellation operation and the charge sharing operation.

[0102] FIG. **7** is a diagram illustrating a layout of the bit-line sense amplifier in FIG. **6** according to example embodiments.

[0103] FIG. **7** is a layout illustrating a right half of the bit-line sense amplifier **750** in FIG. **6**.

[0104] Referring to FIG. **7**, a bit-line sense amplifier **750_1** may include a first active region **20**, a second active region **35** and a third active region **10**.

[0105] The third active region **10** may be placed on a substrate in a rectangular active pattern in a first direction D**1** and a second direction D**2** crossing the first direction D**1**. The first active region **20** may be spaced apart from the third active region **10** in the first direction D**1** on the substrate, and may be placed in an active pattern in a fork shape. The second active region **35** may be spaced apart from a first side of the first active region **20** in the first direction D**1**. The third active region **10** may be spaced apart from a second side of the first active region **20** in the first direction D**1**.

[0106] A contact C_LA for connecting to a metal pattern transferring the first control signal LA may be formed over the third active region **10**.

[0107] The first active region **20** may include a first region **25** having a horseshoe-shaped portion extending in the first

direction D1 on the substrate and a second region **30** having rectangular portions extending in the first direction D1 and spaced apart from each other in the second direction D2. For example, the first region **25** may include a horseshoe-shaped portion of the first active region **20** (e.g., in a plan view) of the first active region **20**, and the second region **30** may include rectangular portions of the first active region **20** that are spaced apart from each other (e.g., in the second direction D2). The second region **30** may be adjacent to the first region **25**. The first active region **20** may extend in the first direction D1. The horseshoe-shaped portion of the first active region **20** in the first region **25** and the rectangular portions of the first active region **20** in the second region **30** may be connected.

[0108] In example embodiments, the rectangular portions of the second region **30** may be a pair of active patterns extending parallel to each other in the first direction D1. According to some embodiments, each of the pair of active patterns may have a rectangular shape, however, the one or more embodiments are not limited thereto, and may include other shapes such as square, circular, oval, trapezoidal, and others.

[0109] The second active region **35** may be spaced apart from the first side of the first active region **20** in the first direction D1 and may include a third region **40**. The third region **40** may have a rectangular shape. A contact C_LAB for connecting to a metal pattern transferring the second control signal LAB may be formed above or under the third region **40**.

[0110] The bit-line sense amplifier **750_1** may further include a first gate pattern **31**, a second gate pattern **32**, a third gate pattern **33**, fourth gate patterns **41** and **42**, and fifth gate patterns **11** and **12**.

[0111] The first gate pattern **31** may extend in the second direction D2 on the first region **25** and may receive the isolation signal ISO. The first gate pattern **31** and the first region **25** may correspond to (i.e., may constitute) the second isolation transistor ISO_2.

[0112] The second gate pattern **32** and the third gate pattern **33** may be spaced apart from each other in the first direction D1 and may extend in the second direction D2 in parallel on the second region **30**. The second gate pattern **32** may receive the equalizing signal PEQ and the third gate pattern **33** may receive the offset cancellation signal OC. The second gate pattern **32** and the second region **30** may correspond to (i.e., may constitute) the second equalizing transistor EQ_2. The third gate pattern **33** and the second region **30** may correspond to (i.e., may constitute) the second offset cancellation transistor OC_2.

[0113] In example embodiments, the second gate pattern **32** may receive the offset cancellation signal OC and the third gate pattern **33** may receive the equalizing signal PEQ. In this case, the second gate pattern **32** and the second region **30** may correspond to (i.e., may constitute) the second offset cancellation transistor OC_2, and the third gate pattern **33** and the second region **30** may correspond to (i.e., may constitute) the second equalizing transistor EQ_2.

[0114] The fourth gate patterns **41** and **42** may be spaced apart from each other in the second direction D2 and may be provided as a rectangular shape on the third region **40**.

[0115] The fourth gate pattern **41** and the second active region **35** may correspond to (i.e., may constitute) the second NMOS transistor MN2 and the fourth gate pattern **42** and the second active region **35** may correspond to (i.e., may constitute) a second NMOS transistor of another bit-line sense amplifier.

[0116] A direct contact DC1 may be provided over the first region **25** and the complementary bit-line BLB may be connected to the drain of the second isolation transistor ISO_2 through the direct contact DC1.

[0117] As described with reference to FIG. **6**, because the complementary bit-line BLB is connected to the drain of the second isolation transistor ISO_2, a voltage level of the complementary bit-line BLB may swing between a power supply voltage VDD and the ground voltage VSS when the isolation signal ISO, which is applied to the gate of the second isolation transistor ISO_2, has a voltage level of the power supply voltage. In some embodiments, the voltage level of the complementary bit-line BLB may swing between the internal power supply voltage VINTA and the ground voltage VSS when the isolation signal ISO has the voltage level of the internal power supply voltage VINTA.

[0118] The fifth gate patterns **11** and **12** may be spaced apart from each other in the second direction D2 and may be provided as a rectangular shape on the third active region **10**.

[0119] The fifth gate pattern **11** and the third active region **10** may correspond to (i.e., may constitute) the second PMOS transistor MP2 and the fifth gate pattern **12** and the third active region **10** may correspond to (i.e., may constitute) a second PMOS transistor of another bit-line sense amplifier.

[0120] The first active region **20** and the second active region **35** may correspond to an N-type active region and the third active region **10** may be a P-type active region.

[0121] FIG. **8** illustrates an example of a bit-line layout connected to the bit-line sense amplifier in FIG. **7** according to example embodiments.

[0122] Referring to FIG. **8**, bit-line metal patterns BLMPs including a bit-line metal pattern BLMP1 may be formed on the layout of the bit-line sense amplifier **750_1** and may be connected to the bit-line sense amplifier **750_1** in FIG. **7**. The contact C_LA for connecting to a metal pattern transferring the first control signal LA and the contact C_LAB for connecting to a metal pattern transferring the second control signal LAB may be formed among the bit-line metal patterns BLMPs. The bit-line metal pattern BLMP1 may be formed on the direct contact DC1.

[0123] FIG. **9** is a circuit diagram illustrating an example of a bit-line sense amplifier according to example embodiments.

[0124] FIG. **9** is a layout illustrating a left half of the bit-line sense amplifier **750** in FIG. **6**.

[0125] Referring to FIG. **9**, a bit-line sense amplifier **750_2** may include a first active region **55**, a second active region **70** and a third active region **50**.

[0126] The third active region **50** may be placed on a substrate in a rectangular active pattern in the first direction D1 and the second direction D2. The first active region **55** may be spaced apart from the third active region **50** in the first direction DI on the substrate, and may be placed in an active pattern in a fork shape. The second active region **70** may be spaced apart from a first side of the first active region **55** in the first direction D1. The third active region **50** may be spaced apart from a second side of the first active region **55** in the first direction D1.

[0127] A contact C_LA for connecting to a metal pattern transferring the first control signal LA may be formed over the third active region **50**.

[0128] The first active region **55** may include a first region **60** having a horseshoe-shaped portion extending in the first direction D**1** on the substrate and a second region **65** having rectangular portions extending in the first direction and spaced apart from each other in the second direction D**2**. For example, the first region **60** may include a horseshoe-shaped portion (e.g., in a plan view) of the first active region **55**, and the second region **65** may include rectangular portions of the first active region **55** that are spaced apart from each other (e.g., in the second direction D**2**). The second region **65** may be adjacent to the first region **60**. The first active region **55** may extend in the first direction D**1**, and the horse-shoe shaped portion of the first active region **55** in the first region **60** and the rectangular portions of the first active region **55** in the second region **65** may be connected.

[0129] In example embodiments, the rectangular portions of the second region **65** may be a pair of active patterns extending parallel to each other in the first direction D**1**. Each of the pair of active patterns may have a rectangular shape, however, the one or more embodiments are not limited thereto, and may include other shapes such as square, circular, oval, trapezoidal, and others.

[0130] The second active region **70** may be spaced apart from a first side of the first active region **55** in the first direction D**1** and may include a third region **75**. The third region **75** may have a rectangular shape. A contact C_LAB for connecting to a metal pattern transferring the second control signal LAB may be formed over the third region **75**.

[0131] The bit-line sense amplifier **750_2** may further include a first gate pattern **61**, a second gate pattern **62**, a third gate pattern **63**, fourth gate patterns **71** and **72**, and fifth gate patterns **51** and **52**.

[0132] The first gate pattern **61** may extend in the second direction D**2** on the first region **60** and may receive the equalizing signal PEQ. The first gate pattern **61** and the first region **60** may correspond to (i.e., may constitute) the first isolation transistor ISO_**1**.

[0133] The second gate pattern **62** and the third gate pattern **63** may be spaced apart from each other in the first direction D**1** and may extend in the second direction D**2** in parallel on the second region **65**. The second gate pattern **62** may receive the second equalizing transistor EQ_**2** and the third gate pattern **63** may receive the offset cancellation signal OC. The second gate pattern **62** and the second region **65** may correspond to (i.e., may constitute) the first equalizing transistor EQ_**1**. The third gate pattern **63** and the second region **65** may correspond to (i.e., may constitute) the first offset cancellation transistor OC_**1**.

[0134] In example embodiments, the second gate pattern **62** may receive the offset cancellation signal OC and the third gate pattern **63** may receive the equalizing signal PEQ. In this case, the second gate pattern **62** and the second region **65** may correspond to (i.e., may constitute) the first offset cancellation transistor OC_**2**, and the third gate pattern **63** and the second region **60** may correspond to (i.e., may constitute) the first equalizing transistor EQ_**1**.

[0135] The fourth gate patterns **71** and **72** may be spaced apart from each other in the second direction D**2** and may be provided as a rectangular shape on the third region **70**.

[0136] The fourth gate pattern **71** and the second active region **70** may correspond to (i.e., may constitute) the first NMOS transistor MN**1** and the fourth gate pattern **72** and the second active region **70** may correspond to (i.e., may constitute) a first NMOS transistor of another bit-line sense amplifier.

[0137] A direct contact DC**2** may be provided over the first region **60** and the bit-line BL may be connected to the drain of the first isolation transistor ISO_**1** through the direct contact DC**2**.

[0138] The fifth gate patterns **51** and **52** may be spaced apart from each other in the second direction D**2** and may be provided as a rectangular shape on the third active region **50**.

[0139] The fifth gate pattern **51** and the third active region **50** may correspond to (i.e., may constitute) the first PMOS transistor MP**1** and the fifth gate pattern **52** and the third active region **50** may correspond to (i.e., may constitute) a first PMOS transistor of another bit-line sense amplifier.

[0140] The first active region **55** and the second active region **70** may correspond to an N-type active region and the third active region **50** may be a P-type active region.

[0141] As described with reference to FIG. **6**, because the bit-line BL is connected to the drain of the first isolation transistor ISO_**1**, a voltage level of the bit-line BL may swing between the power supply voltage VDD and the ground voltage VSS when the isolation signal ISO, which is applied to the gate of the first isolation transistor ISO_**1**, has a voltage level of the power supply voltage. In some embodiments, the voltage level of the bit-line BL may swing between the internal power supply voltage VINTA and the ground voltage VSS when the isolation signal ISO has the voltage level of the internal power supply voltage VINTA.

[0142] FIG. **10** shows an equivalent circuit of the bit-line sense amplifier in FIG. **6** according to example embodiments. FIG. **11** is a flowchart for describing operations of the bit-line sense amplifier in FIG. **10** according to example embodiments. FIGS. **12**A, **12**B, **12**C, **12**D, and **12**E are circuit diagrams for describing operations of the bit-line sense amplifier in FIG. **10** according to example embodiments.

[0143] In FIG. **10**, for simplicity of the drawings, the first and second equalizing transistors EQ_**1** and EQ_**2**, the first and second isolation transistors ISO_**1** and ISO_**2** and the first and second offset cancellation transistors OC_**1** and OC_**2** are illustrated using dashed lines. Operations of the equivalent circuit of the bit-line sense amplifier **750** illustrated in FIG. **10** will be described in detail with reference to FIGS. **11** and **12**A through **12**E.

[0144] Referring to FIG. **11**, the bit-line sense amplifier **750** may sequentially perform a pre-charging operation (S**110**), an offset cancelling operation (S**120**), a charge sharing operation (S**130**), a shifting operation (S**140**) and sensing and restoring operation (S**150**) in response to the isolation signal ISO, the offset cancellation signals OC, and the first and second control signals LA and LAB. For convenience of description, the operations of FIG. **11** will be described with reference to FIGS. **12**A through **12**E.

[0145] Referring to FIG. **12**A, in operation S**110** of FIG. **11**, the bit-line sense amplifier **750** performs a pre-charging operation. The bit-line sense amplifier **750** precharges the bit-line BL, the complementary bit-line BLB, the sensing bit-line SBL, and the complementary sensing bit-line SBLB to a precharge voltage VBL. For example, the equalizing signal PEQ, the isolation signal ISO and the offset cancellation signal OC may be logic high (H).

[0146] In response to the equalizing signal PEQ having a logic high level, the precharge voltage VBL is provided to the sensing bit-line SBL and the complementary sensing bit-lien SBLB, the first and second isolation transistors ISO_**1** and ISO_**2** are turned on in response to the isolation signal ISO having a logic high level and the first and second offset cancellation transistors OC_**1** and OC_**2** are turned on in response to the offset cancellation signal OC having a logic high level. Accordingly, the sensing bit-line SBL is connected to the bit-line BL and the complementary sensing bit-line SBLB is connected to the complementary bit-line BLB. Therefore, the bit-line BL, the complementary bit-line BLB, the sensing bit-line SBL and the complementary sensing bit-line SBLB may be connected to one node and charged to the precharge voltage VBL. In this case, the first and second control signals LA and LAB may be charged to the precharge voltage VBL. For example, the first control signal LA may be charged to the precharge voltage VBL by a pull-up driving circuit and the second control signal LAB may be charged to the precharge voltage VBL by a pull-down driving circuit.

[0147] Referring to FIG. **12**B, in operation S**120** of FIG. **11**, the bit-line sense amplifier **750** performs an offset cancelling operation. For example, the isolation signal ISO and the equalizing signal PEQ may be logic low (L) and the offset cancellation signals OC may be logic high (H).

[0148] The first and second isolation transistors ISO_**1** and ISO_**2** are turned off in response to the isolation signal ISO having a logic low level, and thus, the sensing bit-line SBL and the complementary sensing bit-line SBLB are disconnected from the bit-line BL and the complementary bit-line BLB, respectively. The first and second offset cancellation transistors OC_**1** and OC_**2** are turned on in response to the offset cancellation signal OC having a logic high level, and thus, the sensing bit-line SBL and the complementary sensing bit-line SBLB are connected to the complementary bit-line BLB and the bit-line BL, respectively. In this case, the first control signal LA is transitioned from the precharge voltage VBL to an internal power supply voltage VINTA and the second control signal LAB is transitioned from the precharge voltage VBL to the ground voltage VSS. The internal power supply voltage VINTA may be a voltage supplied to memory cell array **310** (see FIG. **3**).

[0149] In the bit-line sense amplifier **750**, the first and second PMOS transistors MP**1** and MP**2** may have different threshold voltages Vth from each other and the first and second NMOS transistors MN**1** and MN**2** may have different threshold voltages Vth from each other, due to a variation in manufacturing processes, temperature, or the like. In this case, the bit-line sense amplifier **750** may cause offset noise due to the difference between the threshold voltages Vth of the first and second PMOS transistors MP**1** and MP**2** and the first and second NMOS transistors MN**1** and MN**2**. Hereinafter, a method of compensating an offset of the bit-line sense amplifier **750** through an offset cancelling operation will be described with reference to first to fourth examples.

[0150] FIG. **13** is a graph for describing operations of the bit-line sense amplifier **750** in FIG. **10** according to example embodiments.

[0151] In a first example (Case I), it is assumed that a threshold voltage of the first NMOS transistor MN**1** is greater than a threshold voltage of the second NMOS transistor MN**2**. The first and second NMOS transistors MN**1** and MN**2** operate as diodes. An amount of current which flows through the first NMOS transistor MN**1** may be less than an amount of current which flows through the second NMOS transistor MN**2**. Also, an amount of current which flows through the first PMOS transistor MP**1** may be less than an amount of current which flows through the second PMOS transistor MP**2**. Accordingly, as illustrated in FIG. **13**, the voltage on the complementary bit-line BLB may be increased to a predetermined level which is greater than the voltage on the bit-line BL.

[0152] In a second example (Case II), it is assumed that the threshold voltage of the second NMOS transistor MN**2** is greater than the threshold voltage of the first NMOS transistor MN**1**. The first and second NMOS transistors MN**1** and MN**2** operate as diodes. An amount of current which flows through the second NMOS transistor MN**2** may be less than an amount of current which flows through the first NMOS transistor MN**1**. Also, an amount of current which flows through the second PMOS transistor MP**2** may be less than an amount of current which flows through the first PMOS transistor MP**1**. Accordingly, as illustrated in FIG. **13**, the voltage on the complementary bit-line BLB may be reduced to a predetermined level which is less than the voltage on the bit-line BL.

[0153] In a third example (Case III), it is assumed that the threshold voltage of the first PMOS transistor MP**1** is greater than the threshold voltage of the second PMOS transistor MP**2**. An amount of current which flows through the first PMOS transistor MP**1** may be less than an amount of current which flows through the second PMOS transistor MP**2**. The first and second NMOS transistors MN**1** and MN**2** may flow a predetermined amount of current as diodes. Accordingly, as illustrated in FIG. **13**, the voltage on the complementary bit-line BLB may be increased to a predetermined level which is greater than the voltage on the bit-line BL.

[0154] In a fourth example (Case IV), it is assumed that the threshold voltage of the second PMOS transistor MP**2** is greater than the threshold voltage of the first PMOS transistor MP**1**. An amount of current which flows through the second PMOS transistor MP**2** may be less than an amount of current which flows through the first PMOS transistor MP**1**. The first and second NMOS transistors MN**1** and MN**2** may flow a predetermined amount of current as diodes. Accordingly, as illustrated in FIG. **13**, the voltage on the complementary bit-line BLB may be reduced to a predetermined level which is less than the voltage on the bit-line BL.

[0155] In the above-described first to fourth examples (Cases I to IV), the complementary bit-line BLB is increased or decreased to the predetermined level as compared to the bit-line BL, and thus the bit-line BL and the complementary bit-line BLB have a predetermined voltage difference. Such a voltage difference may be interpreted as an offset voltage due to the offset noise. This means that the offset noise of the bit-line sense amplifier **750** may be cancelled by causing the bit-line BL and the complementary bit-line BLB to have a difference by the offset voltage. That is, the bit-line sense amplifier **750** may compensate for the offset through the offset cancelling operation.

[0156] Referring to FIG. **12**C, in operation S**130** of FIG. **11**, the bit-line sense amplifier **750** performs a charge sharing operation. For example, the isolation signal ISO and the offset cancellation signal OC may be logic low (L) and the equalizing signal PEQ may be logic high. For example, the sensing bit-line SBL and the complementary sensing

bit-line SBLB may be charged to the precharge voltage VBL based on the equalizing signal PEQ having a logic high level.

[0157] The first and second isolation transistors ISO_**1** and ISO_**2** and the first and second offset cancellation transistors OC_**1** and OC_**2** are turned off in response to the isolation signal ISO and the offset cancellation signal OC having a logic low level. The sensing bit-line SBL and the complementary sensing bit-line SBLB are disconnected from the bit-line BL, the complementary bit-line BLB, based on the offset cancellation signal OC having a logic low level.

[0158] In this case, the first word-line WLi connected to the memory cell MC**1** (see FIG. **6**) is activated, and the charge sharing operation is performed between electric charges stored in the cell capacitor CC**1** of the memory cell MC**1** and electric charges stored in the bit-line BL.

[0159] For example, when data having a value of '1' is stored in the memory cell MC**1**, a voltage level of the bit-line BL may be increased by a predetermined amount during the charge sharing operation. On the other hand, when data having a value of '0' is stored in the memory cell MC**1**, the voltage level of the bit-line BL may be decreased by a predetermined amount during the charge sharing operation.

[0160] Referring to FIG. **12**D, in operation S**140** of FIG. **11**, the bit-line sense amplifier **750** performs a shifting operation. For example, the isolation signal ISO may be logic high (H) and the offset cancellation signal OC may be logic low (L)

[0161] The sensing bit-line SBL and the complementary sensing bit-line SBLB are connected to the bit-line BL and the complementary bit-line BLB, respectively, based on the isolation signal ISO having a logic high level, and voltage levels of the bit-line BL and the complementary bit-line BLB are increased by the precharge voltage VBL of the sensing bit-line SBL and the complementary sensing bit-line SBLB. In this case, the first control signal LA and the second control signal may be maintained at the precharge voltage VBL.

[0162] Referring to FIG. **12**E, in operation S**150** of FIG. **12**, the bit-line sense amplifier **750** performs a sensing and restoring operation. For example, the isolation signal ISO may be logic high (H) and the offset cancellation signal OC may be logic low (L).

[0163] When the charge sharing operation described in FIG. **12**C is performed, the voltage of the bit-line BL may be increased or decreased by a predetermined amount according to the data stored in the memory cell MC**1**. In this case, the first control signal LA is transitioned to the internal power supply voltage VINTA and the second control signal LAB is transitioned to the ground voltage VSS. Accordingly, the bit-line sense amplifier **750** may charge each of the voltages of the sensing bit-line SBL and the complementary sensing bit-line SBLB to the internal power supply voltage VINTA and discharge each of the voltages of the sensing bit-line SBL and the complementary sensing bit-line SBLB to the ground voltage VSS based on the voltage difference between the bit-line BL and the complementary bit-line BLB.

[0164] For example, when data having a value of '1' is stored in the memory cell MC**1**, the voltage on the sensing bit-line SBL may be increased to the internal power supply voltage VINTA and the voltage on the complementary sensing bit-line SBLB may be decreased to the ground voltage VSS during the sensing operation. On the other hand, when data having a value of '0' is stored in the memory cell MC**1**, the voltage on the sensing bit-line SBL may be decreased to the ground voltage VSS and the voltage on the complementary sensing bit-line SBLB may be increased to the internal power supply voltage VINTA.

[0165] Referring to FIG. **12**E, in operation S**150** of FIG. **12**, the bit-line sense amplifier **750** performs a restoring operation. For example, the isolation signal ISO may be logic high (H), and the offset cancellation signal OC may be logic low (L).

[0166] The first and second isolation transistors ISO_**1** and ISO_**2** are turned on in response to the isolation signal ISO having a logic high level, and the first and second offset cancellation transistors OC_**1** and OC_**2** are turned off in response to the offset cancellation signal OC having a logic low level. In this case, the bit-line BL and the sensing bit-line SBL are connected by the first isolation transistor ISO_**1**, and the complementary bit-line BLB and the complementary sensing bit-line SBLB are connected by the second isolation transistor ISO_**2**. Accordingly, the voltage on the bit-line BL may be increased or decreased to a voltage level of the sensing bit-line SBL, and the voltage on the complementary bit-line BLB may be increased or decreased to a voltage level of the complementary sensing bit-line SBLB.

[0167] In some embodiments, a sensing bit-line pair SBL and SBLB of the bit-line sense amplifier **750** may be connected to a data line and data may be output to a local sense amplifier, a global sense amplifier, or the data I/O buffer **320** (see FIG. **3**) through the data line after the sensing operation.

[0168] As described above, the bit-line sense amplifier **750** performs the pre-charging operation, the offset cancelling operation, the shifting operation and the sensing and restoring operation based on the equalizing signal PEQ, the isolation signal ISO, the offset cancellation signal OC, and the first and second control signals LA and LAB. In this case, the bit-line sense amplifier **750** may compensate the offset of the bit-line sense amplifier **750** through the offset cancelling operation and may shift voltage levels of the bit-line BL and the complementary bit-line BLB through the shifting operation while the N-type amplifier **765** may operate dominantly over the P-type amplifier **760**. Therefore, a bit-line sense amplifier with enhanced performance and reduced power consumption maybe provided and a semiconductor memory device including the bit-line sense amplifier may be provided.

[0169] FIG. **14** is a timing diagram for describing the operations of the bit-line sense amplifier in FIG. **6** according to example embodiments.

[0170] An x-axis of FIG. **14** denotes time and a y-axis denotes a voltage level of signal. For example, it is assumed that the memory cell MC**1** stores data having a value of '1' and a threshold voltage of the first NMOS transistor MN**1** is greater than a threshold voltage of the second NMOS transistor MN**2** by an offset voltage Vos.

[0171] Referring to FIG. **14**, the bit-line sense amplifier **750** sequentially performs a pre-charging operation, an offset cancelling operation, a charge sharing operation, a shifting operation and a sensing and restoring operation.

[0172] In a precharge period corresponding to a first time interval t**0**~t**1**, the bit-line sense amplifier **750** perform a pre-charging operation. In this case, the equalizing signal PEQ, the isolation signal ISO and the offset cancellation

signal OC are at a logic high level (denoted as 'HIGH'), and a bit-line pair BL and BLB and a sensing bit-line pair SBL and SBLB are precharged to the precharge voltage VBL.

[0173] In an offset cancellation period corresponding to a second time interval t**1**~t**2**, the bit-line sense amplifier **750** performs an offset cancelling operation. In this case, the equalizing signal PEQ and the isolation signal ISO become logic low. The first control signal LA is increased from the precharge voltage VBL to the internal power supply voltage VINTA and the second control signal LAB is reduced from the precharge voltage VBL to the ground voltage VSS (denoted as 'LOW'). The bit-line sense amplifier **750** may perform the offset cancelling operation based on the method described in FIGS. **11** and **12**B. During the offset cancelling operation, the voltage on the sensing bit-line SBL and the complementary bit-line BLB may be greater than the voltage on the complementary sensing bit-line SBLB and the bit-line BL by the offset voltage Vos. Accordingly, the voltages on the bit-line BL and the complementary bit-line BLB have a difference by the offset voltage Vos, and thus the offset noise of the bit-line sense amplifier **750** may be cancelled.

[0174] In a charge sharing period corresponding to a third time interval t**2**~t**3**, the bit-line sense amplifier **750** performs a charge sharing operation. In this case, the equalizing signal PEQ becomes logic high, the isolation signal ISO and the offset cancellation signal OC become logic low, the word-line WL (corresponding to the first word-line WLi) connected to the memory cell MC**1** is activated, and the charge sharing operation is performed between electric charges stored in the cell capacitor of the memory cell MC**1** and electric charges stored in the bit-line BL. For example, the sensing bit-line SBL and the complementary sensing bit-line SBLB may be charged to the precharge voltage VBL based on the equalizing signal PEQ having a logic high level. When data having a value of '1' is stored in the memory cell MC**1**, a voltage level of the bit-line BL may be increased by a predetermined level during the charge sharing operation. In another embodiment, when data having a value of '0' is stored in the memory cell MC**1**, the voltage level of the bit-line BL may be reduced by a predetermined level during the charge sharing operation.

[0175] In a shifting period corresponding to a fourth time interval t**3**~t**4**, the bit-line sense amplifier **750** performs a shifting operation. In this case, the equalizing signal PEQ becomes logic low, the isolation signal ISO becomes logic high and the offset cancellation signal OC becomes a logic low (i.e., the offset cancellation signal OC is maintained at a logic low level).

[0176] The sensing bit-line SBL and the complementary sensing bit-line SBLB is connected to the bit-line BL and the complementary bit-line BLB, respectively, based on the isolation signal ISO having a logic high level, and voltage levels of the bit-line BL and the complementary bit-line BLB are increased by the precharge voltage VBL of the sensing bit-line SBL and the complementary sensing bit-line SBLB. In this case, the first control signal LA and the second control signal may be maintained at the precharge voltage VBL.

[0177] In a sensing and restoring period corresponding to a fifth time interval t**4**~t**5**, the bit-line sense amplifier **750** performs a sensing and restoring operation pre-sensing operation. In this case, the isolation signal ISO is maintained at a logic high level and first and second isolation transistors ISO_**1** and ISO_**2** are turned on. The bit-line pair BL and BLB and the sensing bit-line pair SBL and SBLB are respectively connected to each other, and the bit-line pair BL and BLB may be charged or discharged to the voltage level of the sensing bit-line pair SBL and SBLB.

[0178] In this case, the first control signal LA is transitioned to the internal power supply voltage VINTA and the second control signal LAB is transitioned to the ground voltage VSS. Accordingly, the bit-line sense amplifier **750** may charge each of the voltages of the sensing bit-line SBL and the complementary sensing bit-line SBLB to the internal power supply voltage VINTA and discharge each of the voltages of the sensing bit-line SBL and the complementary sensing bit-line SBLB to the ground voltage VSS based on the voltage difference between the bit-line BL and the complementary bit-line BLB.

[0179] FIG. **15** illustrates an example of the first bank array in the semiconductor memory device of FIG. **3** according to example embodiments.

[0180] Referring to FIG. **15**, in the first bank array **310***a*, I sub-array blocks SCB may be disposed in the first direction D**1**, and J sub-array blocks SCB may be disposed in the second direction D**2** perpendicular to the first direction D**1**. I and J represent a number of the sub-array blocks SCB in the first direction D**1** and the second direction D**2**, respectively, and are natural numbers greater than two.

[0181] I sub-array blocks SCB disposed in the first direction DI in one row may be referred to as a row block. A plurality of bit-lines, a plurality of word-lines and a plurality of memory cells connected to the bit-lines and the word-lines are disposed in each of the sub-array blocks SCB.

[0182] I+1 sub word-line driver regions SWB may be disposed between the sub-array blocks SCB in the first direction D**1** as well on each side of each of the sub-array blocks SCB in the first direction D**1**. Sub word-line drivers may be disposed in the sub word-line driver regions SWB. J+1 bit-line sense amplifier regions BLSAB may be disposed, for example, between the sub-array blocks SCB in the second direction D**2** and above and below each of the sub-array blocks SCB in the second direction D**2**. Bit-line sense amplifiers to sense data stored in the memory cells may be disposed in the bit-line sense amplifier regions BLSAB.

[0183] A plurality of sub word-line drivers may be provided in each of the sub word-line driver regions SWB. One sub word-line driver region SWB may be associated with two sub-array blocks SCB adjacent to the sub word-line driver region SWB in the first direction D**1**.

[0184] A plurality of conjunction regions CONJ may be disposed adjacent the sub word-line driver regions SWB and the bit-line sense amplifier regions BLSAB. A voltage generator may be disposed in each of the conjunction regions CONJ.

[0185] A portion **390** in the first bank array **310***a* will be described with reference to FIG. **16** below.

[0186] FIG. **16** illustrates a portion of the first bank array in FIG. **16** according to example embodiments.

[0187] Referring to FIGS. **15** and **16**, in the portion **390** of the first bank array **310***a*, sub-array blocks SCBa and SCBb, the bit-line sense amplifier regions BLSAB, four sub word-line driver regions SWBa**1**, SWBa**2**, SWBb**1** and SWBb**2** and two of the conjunction regions CONJ are disposed.

[0188] The sub-array block SCBa may include a plurality of word-lines WL**0**~WL**3** extending in the first direction D**1** and a plurality of bit-line BL**0**~BL**3** extending in the second

direction D2. The sub-array block SCBa may include a plurality of memory cells MCs disposed at intersections of the word-lines WL0~WL3 and the bit-line BL0~BL3. The sub-array block SCBb may include a plurality of word-lines WL4~WL7 extending in the first direction D1 and the plurality of bit-line BL0~BL3 extending in the second direction D2. The sub-array block SCBb may include a plurality of memory cells MCs disposed at intersections of the word-lines WL4~WL7 and the bit-line BL0~BL3.

[0189] With reference to FIG. **16**, the sub word-line driver regions SWBa1 and SWBa2 may include a plurality of sub word-line drivers **731**, **732**, **733** and **734** that respectively drive the word-lines WL0~WL3. The sub word-line driver regions SWBb1 and SWBb2 may include a plurality of sub word-line drivers **741**, **742**, **743** and **744** that respectively drive the word-lines WL4~WL7.

[0190] The bit-line sense amplifier region BLSAB may include the bit-line sense amplifier **750** coupled to the bit-line BL0 in the sub array block SCBb and the bit-line BL1 in the sub array block SCBa, and a local sense amplifier LSA circuit **780**. The bit-line sense amplifier **750** may sense and amplify a voltage difference between the bit-lines BL0 and BL1 to provide the amplified voltage difference to a local I/O line pair LIO1 and LIOB1. The local I/O line pair LIO1 and LIOB1 may correspond to the sensing bit-line SBL and the complementary sensing bit-line SBLB in FIG. **6**. The bit-line BL1 in the sub array block SCBa may correspond to the complementary bit-line BLB in FIG. **6**.

[0191] The local sense amplifier circuit **780** may control electrical connection between the local I/O line pair LIO1 and LIOB1 and a global I/O line pair GIO1 and GIOB1.

[0192] As illustrated in FIG. **16**, the conjunction regions CONJ may be disposed adjacent to the bit-line sense amplifier region BLSAB and the sub word-line driver regions SWBa1, SWBb1, SWBa2 and SWBb2. Voltage generators VGs **710** and **720** may be disposed in the conjunction regions CONJ.

[0193] FIG. **17** is a block diagram illustrating a semiconductor memory device that employs a bit-line sense amplifier according to example embodiments.

[0194] Referring to FIG. **17**, a semiconductor memory device **200***a* may include a plurality of sub array blocks SCB_1, SCB_2, . . . , and SCB_*r*−1 (r is an integer greater than three) and a plurality of bit-line sense amplifiers **750_1**, **750_2**, **750_3**, . . . , and **750_***r*.

[0195] Each of the plurality of bit-line sense amplifiers **750_1**, **750_2**, **750_3**, . . . , and **750_***r* may include a plurality of bit-line sense amplifiers BLSA. Each of the plurality of bit-line sense amplifiers BLSA may employ the bit-line sense amplifier **750** in FIG. **6**.

[0196] Each of the plurality of bit-line amplifiers BLSA is a circuit element that operates when the memory device **200***a* operates, and is distinguished from dummy sense amplifiers **750_1** and **750_***r* implemented in a region other than a region in which bit-line sense amplifiers **750_2~750_***r*−1 are implemented.

[0197] In example embodiments, an odd bit-line of the sub array block SCB_1 may be connected to a bit-line BL, and an even bit-line may be connected to a complementary bit-line BLB. The bit-line sense amplifier **750_2** may be connected to each of the bit-line pairs BL and BLB in both directions.

[0198] FIGS. **18** and **19** are diagrams illustrating a semiconductor memory device that employs a bit-line sense amplifier according to example embodiments.

[0199] FIGS. **18** and **19** correspond to first and second sub array blocks SCB_1 and SCB_2 and bit-line sense amplifiers **750_2***a* which are some of the plurality of sub array blocks SCB_1, SCB_2, . . . , and SCB_*r*−1 and the plurality of bit-line sense amplifiers **750_1**, **750_2**, **750_3**, . . . , and **750_***r* described above in FIG. **17**. Each of the bit-line sense amplifiers **750_2***a* may include the plurality of bit-line sense amplifiers BLSA.

[0200] Unlike the semiconductor memory device **200***a* of FIG. **17**, in the semiconductor memory device **200***b* of FIG. **18**, two bit-line sense amplifiers BLSA in the second bit-line sense amplifiers **750_2***a* are placed to be adjacent to each other. The two bit-line sense amplifiers BLSA may be connected to first and second bit-lines BL1 and BL2, and first and second complementary bit-lines BLB1 and BLB2. One of the two bit-line sense amplifiers BLSA may detect the voltage change of the first bit-line pairs BL1 and BLB1, and the other one may detect the voltage change of the second bit-line pairs BL2 and BLB2.

[0201] Unlike the semiconductor memory device **200***a* of FIG. **17**, in the semiconductor memory device **200***c* of FIG. **19**, three bit-line sense amplifiers BLSA in the second bit-line sense amplifier **750_2***a* are adjacent to each other (e.g., are placed side-by-side). The three bit-line sense amplifiers BLSA may be connected to first to third bit-lines BL1, BL2 and BL3 and first to third complementary bit-lines BLB1, BLB2 and BLB3. Each of the three bit-line sense amplifiers BLSA may detect the voltage change of each of the first to third bit-line pairs (BL1 and BLB1), (BL2 and BLB2), and (BL3 and BLB3).

[0202] The semiconductor memory devices **200***b* and **200***c* of FIGS. **18** and **19** may be selectively applied according to the tendency in which the size of the unit cell decreases due to the miniaturization of the design-rules according to the high integration of memory cell elements. According to example embodiments, r bit-line sense amplifiers BLSA are placed adjacent to each other, and the r bit-line sense amplifiers BLSA are connected to first to r-th bit-lines BL1 to BLr and first to r-th complementary bit-lines BLB1 to BLBr, and each of the r bit-line sense amplifiers BLSA may detect the voltage change of each of the first to r-th bit-line pairs (BL1 and BLB1) to (BLr and BLBr).

[0203] FIG. **20** is a block diagram illustrating a semiconductor memory device according to example embodiments.

[0204] Referring to FIG. **20**, a semiconductor memory device **800** may include at least one buffer die **810** and a plurality of memory dies **820-1** to **820-***s* (s is a natural number equal to or greater than three) providing a soft error analyzing and correcting function in a stacked chip structure.

[0205] The plurality of memory dies **820-1** to **820-***s* are stacked on the buffer die **810** and conveys data through a plurality of through substrate via (e.g., through silicon via (TSV)) lines.

[0206] Each of the memory dies **820-1** to **820-***s* may include a cell core **821** to store data and a cell core ECC engine **823** which generates transmission parity bits (i.e., transmission parity data) based on transmission data to be sent to the at least one buffer die **810**. The cell core **821** may include a plurality of memory cells having DRAM cell structure. The cell core **821** may include a bit-line sense

amplifier that detects a voltage difference between a bit-line and a complementary bit-line connected to the memory cells.

[0207] The bit-line sense amplifier of the cell core **821** may correspond to the bit-line sense amplifier **750** Of FIG. **6**. The bit-line sense amplifier of the cell core **821** may include an amplifying circuit that includes a P-type amplifier connected to a bit-line and a complementary bit-line and an N-type amplifier connected to a sensing bit-line and a complementary sensing bit-line, and an isolation circuit connected between the bit-line and the sensing bit-line and between the complementary bit-line and the complementary sensing bit-line. The isolation circuit may connect the sensing bit-line and the complementary sensing bit-line to the bit-line and the complementary bit-line, respectively, based on an isolation signal. Because the bit-line and the complementary bit-line are connected to drains of isolation transistors in the isolation circuit, a voltage level of each of the bit-line and the complementary bit-line may swing between the power supply voltage (or the internal power supply voltage) and a ground voltage when the isolation signal, which is applied to gates of the isolation transistors, has a voltage level of the power supply voltage (or the internal power supply voltage).

[0208] The buffer die **810** may include a via ECC engine **812** which corrects a transmission error using the transmission parity bits when a transmission error is detected from the transmission data received through the TSV liens and generates error-corrected data.

[0209] The buffer die **810** may further include a data I/O buffer **814**. The data I/O buffer **814** may generate the data signal DQ by sampling data DTA from the via ECC engine **812** and may output the data signal DQ to an outside.

[0210] The semiconductor memory device **800** may be a stack chip type memory device or a stacked memory device which conveys data and control signals through the TSV lines. The TSV lines may be also called 'through electrodes'.

[0211] The cell core ECC engine **823** may perform error correction on data which is outputted from the memory die **820**-*p* (where, p is a natural number) before the transmission data is sent.

[0212] A data TSV line group **832** which is formed at one memory die **820**-*s* may include TSV lines L**1**, and L**2** to Ls (s is a natural number equal to or greater than three), and a parity TSV line group **834** may include TSV lines L**10** to Lt (t is a natural number equal to or greater than eleven). The TSV lines L**1**, and L**2** to Ls of the data TSV line group **832** and the parity TSV lines L**10** to Lt of the parity TSV line group **834** may be connected to micro bumps MCB which are correspondingly formed among the memory dies **820-1** to **820**-*s*.

[0213] The semiconductor memory device **800** may have a three-dimensional (3D) chip structure or a 2.5D chip structure to communicate with the host through a data bus B**10**. The buffer die **810** may be connected to the memory controller through the data bus B**10**.

[0214] According to example embodiments, as illustrated in FIG. **20**, the cell core ECC engine **823** may be included in the memory die, the via ECC engine **812** may be included in the buffer die **810**. Accordingly, it may be possible to detect and correct soft data fail. The soft data fail may include a transmission error which is generated due to noise when data is transmitted through TSV lines.

[0215] FIG. **21** is a configuration diagram illustrating a semiconductor package including the stacked memory device according to example embodiments.

[0216] Referring to FIG. **21**, a semiconductor package **900** may include one or more stacked memory devices **910** and a graphic processing unit (GPU) **920**.

[0217] The one or more stacked memory devices **910** and the GPU **920** may be mounted on an interposer **930**, and the interposer **930** on which the one or more stacked memory devices **910** and the GPU **920** are mounted may be mounted on a package substrate **940** mounted on solder balls **950**. The GPU **920** may include a memory controller MCT **921**, and for example, the GPU **920** may be implemented as an application processor (AP).

[0218] A stacked memory device **910** may be implemented in various forms, and the stacked memory device **910** may be a memory device in a high bandwidth memory (HBM) form in which a plurality of layers are stacked. Accordingly, the stacked memory device **910** may include a buffer die and a plurality of memory dies and each of the plurality of memory dies include a cell core and the cell core may include a bit-line sense amplifier that detects a voltage difference between a bit-line and a complementary bit-line. The stacked memory device **910** may correspond to the semiconductor memory device **800** of FIG. **20**.

[0219] The one or more stacked memory devices **910** may be mounted on the interposer **930**, and the GPU **920** may communicate with the one or more stacked memory devices **910**. For example, each of the one or more stacked memory devices **910** and the GPU **920** may include a physical region, and communication may be performed between the one or more stacked memory devices **910** and the GPU **920** through the physical regions. Meanwhile, when the stacked memory device **910** includes a direct access region, a test signal may be provided into the stacked memory device **910** through conductive means (e.g., solder balls **950**) mounted under package substrate **940** and the direct access region.

[0220] Aspects of the present disclosure may be applied to systems using semiconductor memory devices that employ volatile memory cells. For example, aspects of the present disclosure may be applied to systems such as be a smart phone, a navigation system, a notebook computer, a desk top computer and a game console that use the semiconductor memory device as a working memory.

[0221] The foregoing is illustrative of example embodiments and is not to be construed as limiting thereof. Although a few example embodiments have been described, those skilled in the art will readily appreciate that many modifications are possible in the example embodiments without materially departing from the novel teachings and advantages of the present disclosure. Accordingly, all such modifications are intended to be included within the scope of the present invention as defined in the claims.

What is claimed is:

1. A semiconductor memory device comprising:

a first memory cell connected to a first word-line and a bit-line;

a second memory cell connected to a second word-line and a complementary bit-line; and

a bit-line sense amplifier connected to the bit-line and the complementary bit-line, and the bit-line sense amplifier comprising:

an amplifying circuit including a P-type amplifier connected to the bit-line and the complementary bit-line

and an N-type amplifier connected to a sensing bit-line and a complementary sensing bit-line, and the amplifying circuit configured to:

sense a voltage difference between the bit-line and the complementary bit-line based on a first control signal and a second control signal, and adjust a voltage of the sensing bit-line and the complementary sensing bit-line based on the voltage difference;

an offset cancellation circuit configured to connect the bit-line and the complementary bit-line to the complementary sensing bit-line and the sensing bit-line, respectively, based on an offset cancellation signal;

an equalizer configured to provide a precharge voltage to the sensing bit-line and the complementary sensing bit-line based on an equalizing signal; and

an isolation circuit connected between the bit-line and the sensing bit-line and between the complementary bit-line and the complementary sensing bit-line, and the isolation circuit configured to:

connect the sensing bit-line and the complementary sensing bit-line equalized with the precharge voltage to the bit-line and the complementary bit-line, respectively, based on an isolation signal.

2. The semiconductor memory device of claim **1**, wherein the P-type amplifier includes:

a first p-channel metal-oxide semiconductor (PMOS) transistor connected to a first supply line at a first node at which the first control signal is applied and connected to the bit-line at a third node, and including a gate connected to the complementary bit-line at a fourth node, and

a second PMOS transistor connected between the first supply line and the fourth node and including a gate connected to the third node, and

wherein the N-type amplifier includes:

a first n-channel metal-oxide semiconductor (NMOS) transistor connected to a second supply line at a second node at which the second control signal is applied and connected to the sensing bit-line at a fifth node, and including a gate connected to the fourth node, and

a second NMOS transistor connected to the second supply line at the second node and connected to the complementary sensing bit-line at a sixth node, and including a gate connected to the third node.

3. The semiconductor memory device of claim **2**, wherein the equalizer includes:

a first equalizing transistor connected between a first precharge voltage node at which the precharge voltage is applied and the fifth node, and including a gate configured to receive the equalizing signal, and

a second equalizing transistor connected between a second precharge voltage node at which the precharge voltage is applied and the sixth node, and including a gate configured to receive the equalizing signal, and

wherein the isolation circuit includes:

a first isolation transistor connected between the third node and the fifth node, and including a gate configured to receive the isolation signal, and

a second isolation transistor connected between the fourth node and the sixth node, and including a gate configured to receive the isolation signal.

4. The semiconductor memory device of claim **3**,

wherein, in a charge sharing period, the first equalizing transistor and the second equalizing transistor are configured to equalize the sensing bit-line and the complementary sensing bit-line with the precharge voltage based on the equalizing signal, and

wherein, in a shifting period, the first isolation transistor and the second isolation transistor are configured to increase voltage levels of the third node and the fourth node, respectively, by connecting the sensing bit-line and the complementary sensing bit-line to the bit-line and the complementary sensing bit-line, respectively, based on the isolation signal.

5. The semiconductor memory device of claim **4**, wherein, in the shifting period, the first isolation transistor and the second isolation transistor are turned-on in response to the isolation signal having a logic high level.

6. The semiconductor memory device of claim **3**, wherein the offset cancellation circuit includes:

a first offset cancellation transistor connected between the fifth node and the fourth node, and including a gate configured to receive the offset cancellation signal, and

a second offset cancellation transistor connected between the sixth node and the third node, and including a gate configured to receive the offset cancellation signal.

7. The semiconductor memory device of claim **6**, wherein the bit-line sense amplifier further comprises:

a first active region including a first region and a second region adjacent to the first region, wherein, in a plan view:

the first region includes a horseshoe-shaped portion of the first active region, and extends in a first direction, and

the second region includes rectangular portions extending in the first direction, of the first active region that are spaced apart from each other in a second direction crossing the first direction;

a second active region including a rectangular shape, the second active region being spaced apart from a first side of the first active region in the first direction;

a third active region including a rectangular shape, the third active region being spaced apart from a second side of the first active region in the first direction;

a first gate pattern extending in the second direction on the first region;

a second gate pattern and a third gate pattern that extend in the second direction on the second region and are spaced apart from each other in the first direction;

a fourth gate pattern having a rectangular shape on the second active region; and

a fifth gate pattern having a rectangular shape on the third active region.

8. The semiconductor memory device of claim **7**, wherein the first region and the first gate pattern correspond to one of the first and second isolation transistors, and the first gate pattern is configured to receive the isolation signal.

9. The semiconductor memory device of claim **7**, wherein the second region and the second gate pattern correspond to one of the first and second equalizing transistors, and the second gate pattern is configured to receive the equalizing signal.

10. The semiconductor memory device of claim **7**, wherein the second region and the third gate pattern correspond to one of the first and second offset cancellation transistors, and the third gate pattern is configured to receive the offset cancellation signal.

11. The semiconductor memory device of claim 7,
wherein the second active region and the fourth gate pattern correspond to one of the first and second NMOS transistors, and
wherein the third active region and the fifth gate pattern correspond to one of the first and second PMOS transistors.

12. The semiconductor memory device of claim 7, wherein each of the first active region and the second active region is N-type and the third active region is P-type.

13. The semiconductor memory device of claim 1,
wherein the P-type amplifier is connected to:
a first supply line at a first node at which the first control signal is applied,
the bit-line at a third node, and
the complementary bit-line at a fourth node,, and
wherein the N-type amplifier is connected to:
a second supply line at a second node at which the second control signal is applied,
the sensing bit-line at a fifth node, and
the complementary sensing bit-line at a sixth node.

14. The semiconductor memory device of claim 13, wherein, during a precharge period:
the equalizer is configured to provide the precharge voltage to the sensing bit-line and the complementary sensing bit-line, based on the equalizing signal,
the offset cancellation circuit is configured to connect the fifth node to the fourth node, and connect the sixth node to the third node, based on the offset cancellation signal, and
the isolation circuit is configured to connect the fifth node to the third node, and connect the sixth node to the fourth node, based on the isolation signal.

15. The semiconductor memory device of claim 13, wherein, during an offset cancellation period:
the equalizer is configured to disconnect a first precharge voltage node at which the precharge voltage is applied from the sensing bit-line and disconnect a second precharge voltage node at which the precharge voltage is applied from the complementary sensing bit-line, based on the equalizing signal,
the offset cancellation circuit is configured to connect the fifth node to the fourth node, and connect the sixth node to the third node, based on the offset cancellation signal, and
the isolation circuit is configured to disconnect the fifth node from the third node, and disconnect the sixth node from the fourth node, based on the isolation signal.

16. The semiconductor memory device of claim 15, wherein, during a charge sharing period:
the equalizer is configured to provide the precharge voltage to the sensing bit-line and the complementary sensing bit-line, based on the equalizing signal,
the offset cancellation circuit is configured to disconnect the fifth node from the fourth node, and disconnect the sixth node to the third node, based on the offset cancellation signal, and
the isolation circuit is configured to disconnect the fifth node from the third node, and disconnect the sixth node from the fourth node, based on the isolation signal.

17. The semiconductor memory device of claim 13, wherein, during a shifting period,
the equalizer is configured to disconnect a first precharge voltage node at which the precharge voltage is applied from the sensing bit-line and disconnect a second precharge voltage node at which the precharge voltage is applied from the complementary sensing bit-line, based on the equalizing signal,
the offset cancellation circuit is configured to disconnect the fifth node from the fourth node, and disconnect the sixth node from the third node, based on the offset cancellation signal, and
the isolation circuit is configured to connect the fifth node to the third node, and connect the sixth node to the fourth node, based on the isolation signal.

18. A semiconductor memory device comprising:
a first memory cell connected to a first word-line and a bit-line;
a second memory cell connected to a second word-line and a complementary bit-line;
a bit-line sense amplifier connected to the bit-line and the complementary bit-line, and the bit-line sense amplifier configured to:
sense a voltage difference between the bit-line and the complementary bit-line, and
amplify the voltage difference; and
a timing control circuit configured to control an operation of the bit-line sense amplifier based on internal command signals,
wherein the bit-line sense amplifier comprises:
an amplifying circuit including a P-type amplifier connected to the bit-line and the complementary bit-line and an N-type amplifier connected to a sensing bit-line and a complementary sensing bit-line, the amplifying circuit configured to:
sense the voltage difference between the bit-line and the complementary bit-line based on a first control signal and a second control signal, and
adjust a voltage of the sensing bit-line and the complementary sensing bit-line based on the voltage difference;
an offset cancellation circuit configured to connect the bit-line and the complementary bit-line to the complementary sensing bit-line and the sensing bit-line, respectively, based on an offset cancellation signal;
an equalizer configured to provide a precharge voltage to the sensing bit-line and the complementary sensing bit-line based on an equalizing signal; and
an isolation circuit connected between the bit-line and the sensing bit-line and between the complementary bit-line and the complementary sensing bit-line, and the isolation circuit configured to:
connect the sensing bit-line and the complementary sensing bit-line equalized with the precharge voltage to the bit-line and the complementary bit-line, respectively, based on an isolation signal.

19. The semiconductor memory device of claim 18, wherein the P-type amplifier includes:
a first p-channel metal-oxide semiconductor (PMOS) transistor connected to a first supply line at a first node at which the first control signal is applied and connected to the bit-line at a third node, and including a gate connected to the complementary bit-line at a fourth node, and
a second PMOS transistor connected between the first supply line and the fourth node, and including a gate connected to the third node,

wherein the N-type amplifier includes:

a first n-channel metal-oxide semiconductor (NMOS) transistor connected to a second supply line at a second node at which the second control signal is applied and connected to the sensing bit-line at a fifth node, and including a gate connected to the fourth node, and

a second NMOS transistor connected to the second supply line at the second node and connected to the complementary sensing bit-line at a sixth node, and including a gate connected to the third node,

wherein the equalizer includes:

a first equalizing transistor connected between a first precharge voltage node at which the precharge voltage is applied and the fifth node, and including a gate configured to receive the equalizing signal, and

a second equalizing transistor connected between a second precharge voltage node at which the precharge voltage is applied and the fifth node, and including a gate configured to receive the equalizing signal, and

wherein the isolation circuit includes:

a first isolation transistor connected between the third node and the fifth node, and including a gate configured to receive the isolation signal, and

a second isolation transistor connected between the fourth node and the sixth node, and including a gate configured to receive the isolation signal.

20. A semiconductor memory device comprising:

a first memory cell connected to a first word-line and a bit-line;

a second memory cell connected to a second word-line and a complementary bit-line;

a bit-line sense amplifier connected to the bit-line and the complementary bit-line, and the bit-line sense amplifier comprising:

an amplifying circuit including a P-type amplifier connected to the bit-line and the complementary bit-line and an N-type amplifier connected to a sensing bit-line and a complementary sensing bit-line, and the amplifying circuit configured to:

sense a voltage difference between the bit-line and the complementary bit-line based on a first control signal and a second control signal, and

adjust a voltage of the sensing bit-line and the complementary sensing bit-line based on the voltage difference;

an offset cancellation circuit configured to connect the bit-line and the complementary bit-line to the complementary sensing bit-line and the sensing bit-line, respectively, based on an offset cancellation signal;

an equalizer configured to provide a precharge voltage to the sensing bit-line and the complementary sensing bit-line based on an equalizing signal; and

an isolation circuit connected between the bit-line and the sensing bit-line and between the complementary bit-line and the complementary sensing bit-line, and the isolation circuit configured to:

connect the sensing bit-line and the complementary sensing bit-line equalized with the precharge voltage to the bit-line and the complementary bit-line, respectively, based on an isolation signal,

wherein the P-type amplifier is connected to:

a first supply line at a first node at which the first control signal is applied,

the bit-line at a third node, and

the complementary bit-line at a fourth node,

wherein the N-type amplifier is connected to:

a second supply line at a second node at which the second control signal is applied,

the sensing bit-line at a fifth node, and

the complementary sensing bit-line at a sixth node,

wherein the equalizer comprises:

a first equalizing transistor connected between a first precharge voltage node at which the precharge voltage is applied and the fifth node, and including a gate configured to receive the equalizing signal; and

a second equalizing transistor connected between a second precharge voltage node at which the precharge voltage is applied and the sixth node, and including a gate configured to receive the equalizing signal, and

wherein the isolation circuit comprises:

a first isolation transistor connected between the third node and the fifth node, and including a gate configured to receive the isolation signal; and

a second isolation transistor connected between the fourth node and the sixth node, and including a gate configured to receive the isolation signal.

* * * * *