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(54) **SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE**

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(57) **ABSTRACT**

A standard cell is formed between first and second power lines, lying astride a third power line. The spacing between the first and third power lines is greater than the spacing between the second and third power lines. The standard cell has a first logic circuit that receives an input A and outputs a signal to an internal node and a second logic circuit that receives the signal from the internal node and outputs an output Y. Transistors constituting the first logic circuit are formed in a region between the second and third power lines, and transistors constituting the second logic circuit are formed in a region between the first and third power lines.

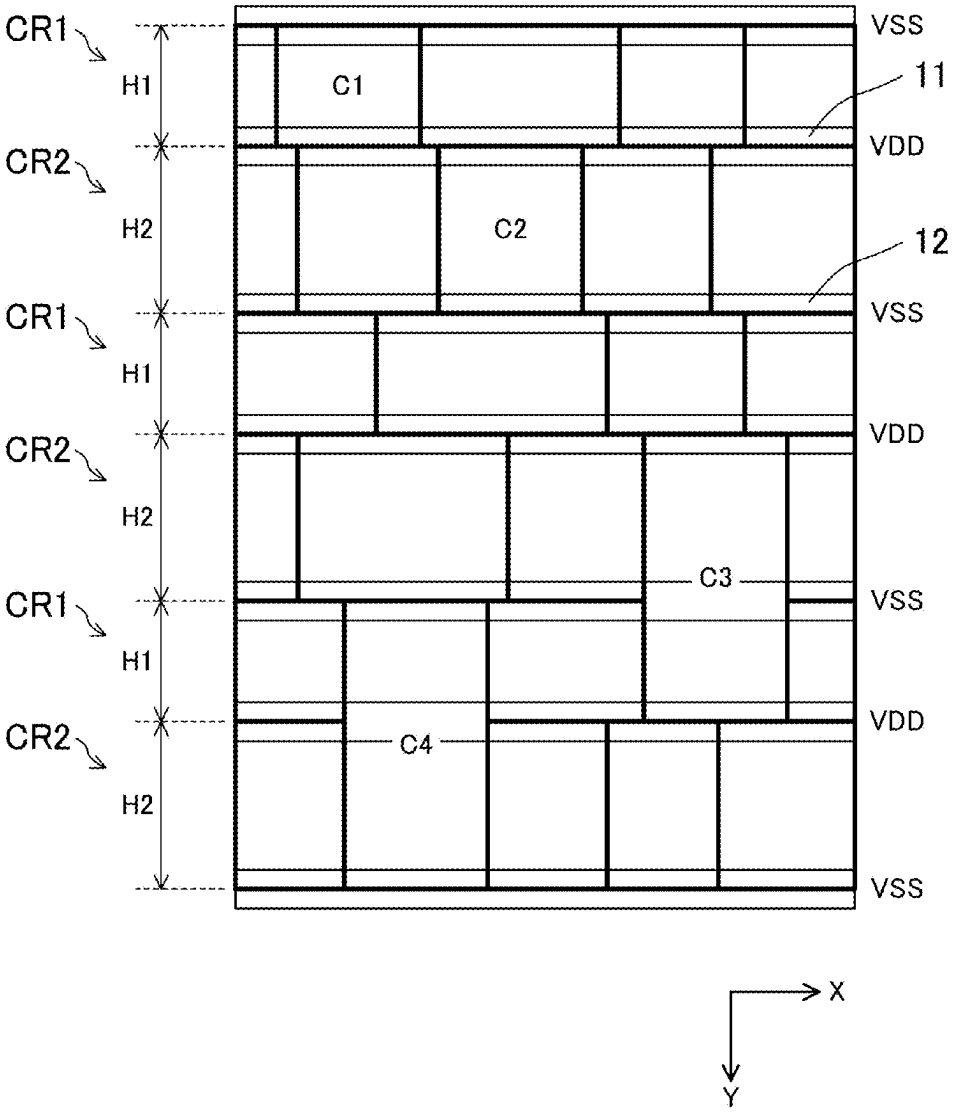


FIG.1

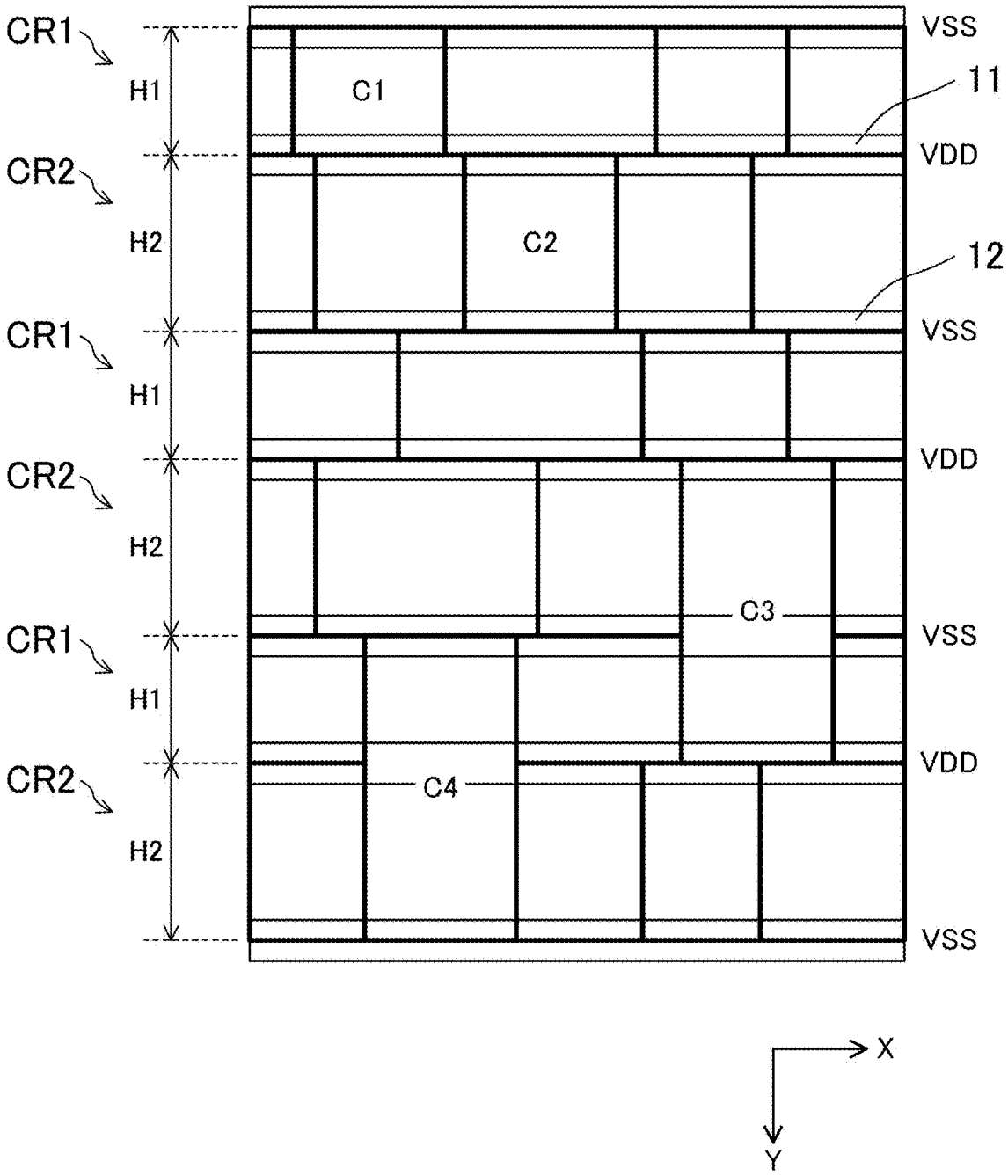

CR1
H1
CR2
H2
CR1
H1
CR2
H2
CR1
H1
CR2
H2
C1
C2
C3
C4
VSS
11
VDD
12
VSS
VDD
VSS
VDD
VSS
X
Y

FIG.2A

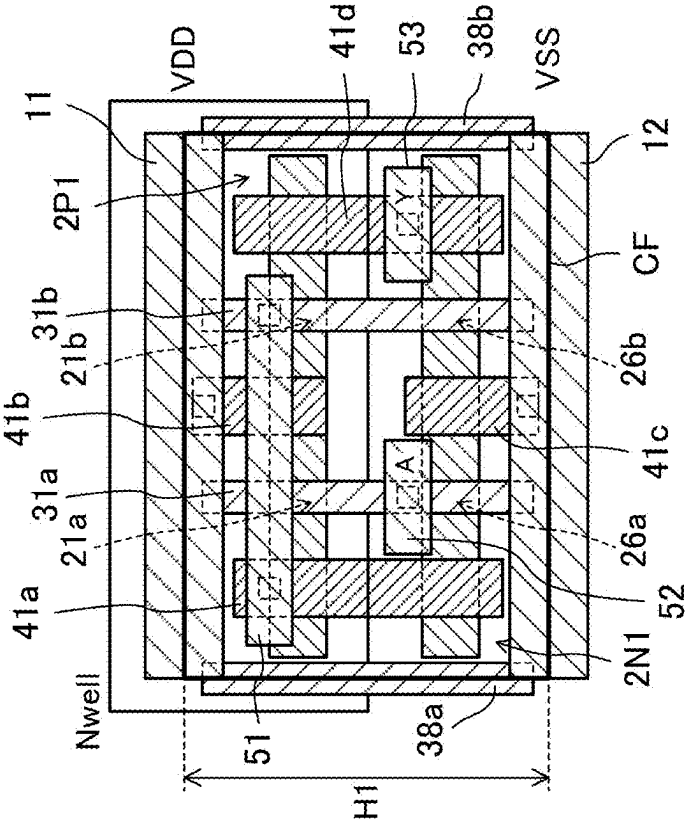

VDD
VSS
11
12
2P1
CF
31b
21b
41b
31a
21a
41a
41d
53
38b
26b
41c
26a
52
2N1
Nwell
51
38a
H1
CELL C1

FIG.2B

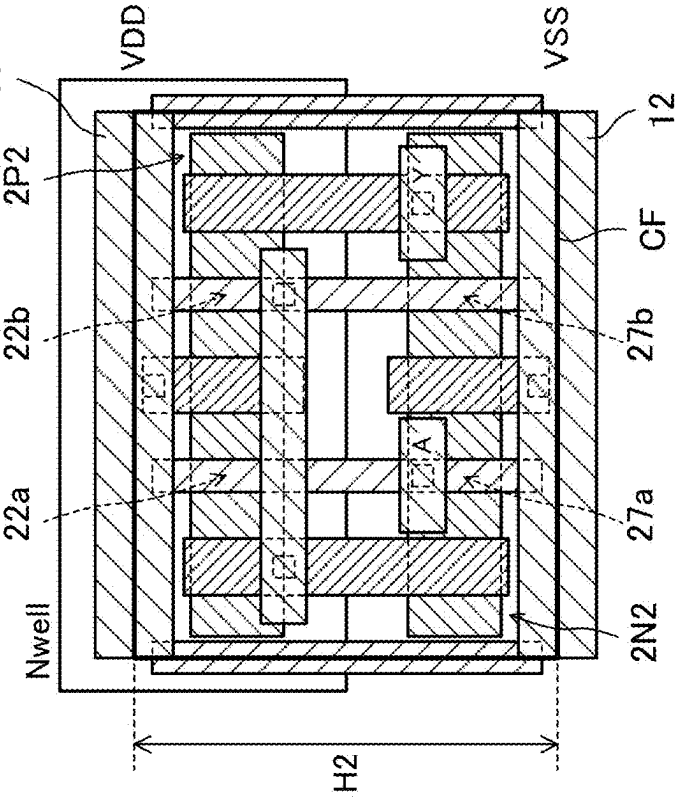

VDD
VSS
11
12
2P2
CF
22b
27b
22a
27a
2N2
Nwell
H2
CELL C2
X
Y
Active
LI
Gate
M0
M1
Via(Gate/LI-M0)
Via(M0-M1)

FIG.3

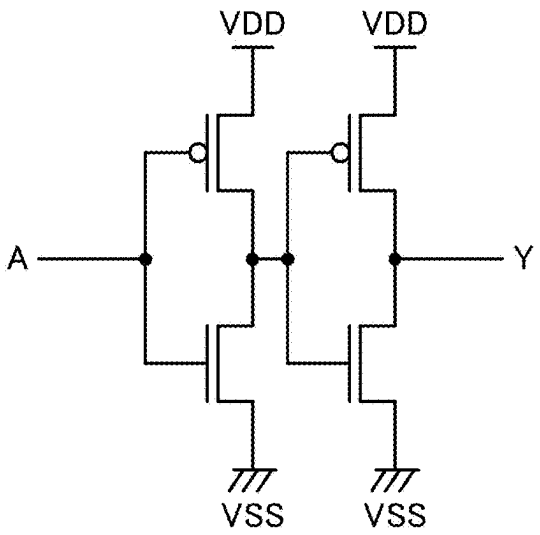


FIG.4

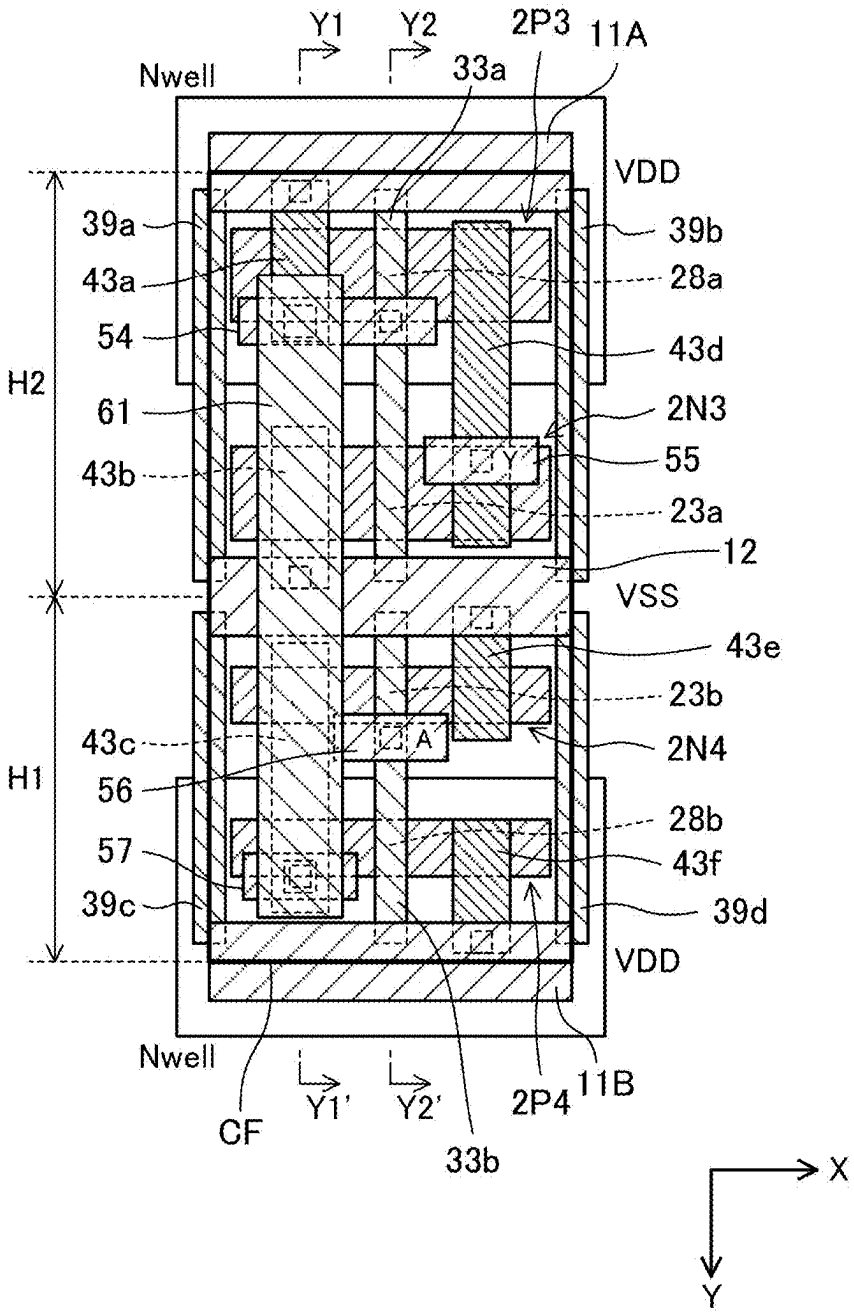

Y1
Y2
2P3
11A
Nwell
33a
VDD
39a
39b
43a
28a
54
43d
H2
61
2N3
43b
55
23a
12
VSS
43e
23b
43c
2N4
H1
56
28b
57
43f
39c
39d
VDD
Nwell
Y1'
Y2'
CF
2P4
11B
33b
X
Y

FIG.5A

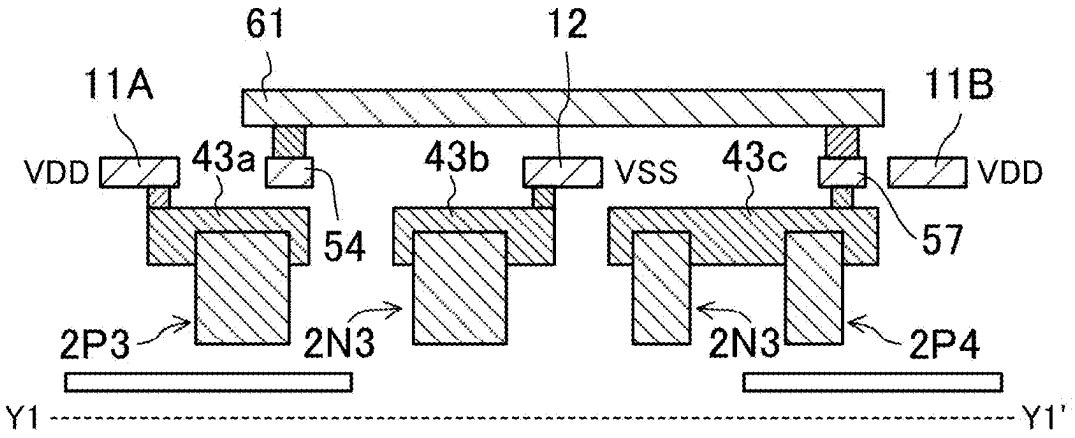

61
12
11A
11B
VDD
43a
43b
VSS
43c
VDD
54
57
2P3
2N3
2N3
2P4
Y1
Y1'

FIG.5B

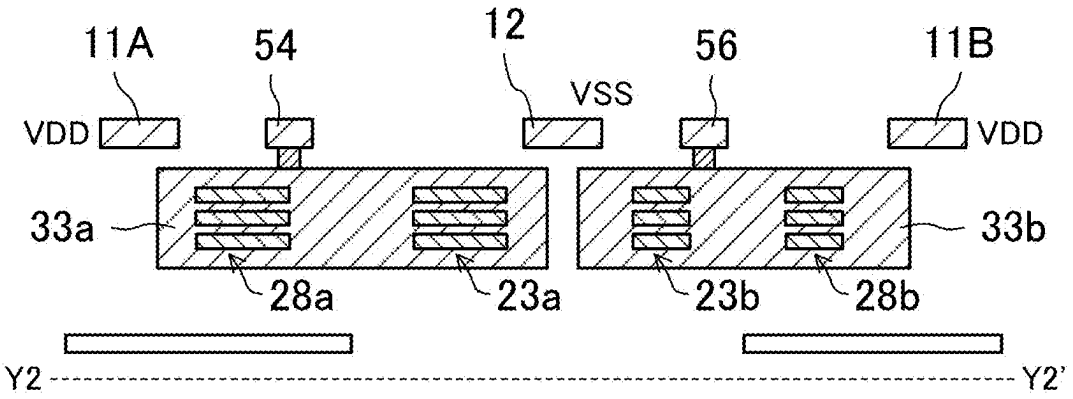

11A
54
12
VSS
56
11B
VDD
VDD
33a
33b
28a
23a
23b
28b
Y2
Y2'

FIG.6

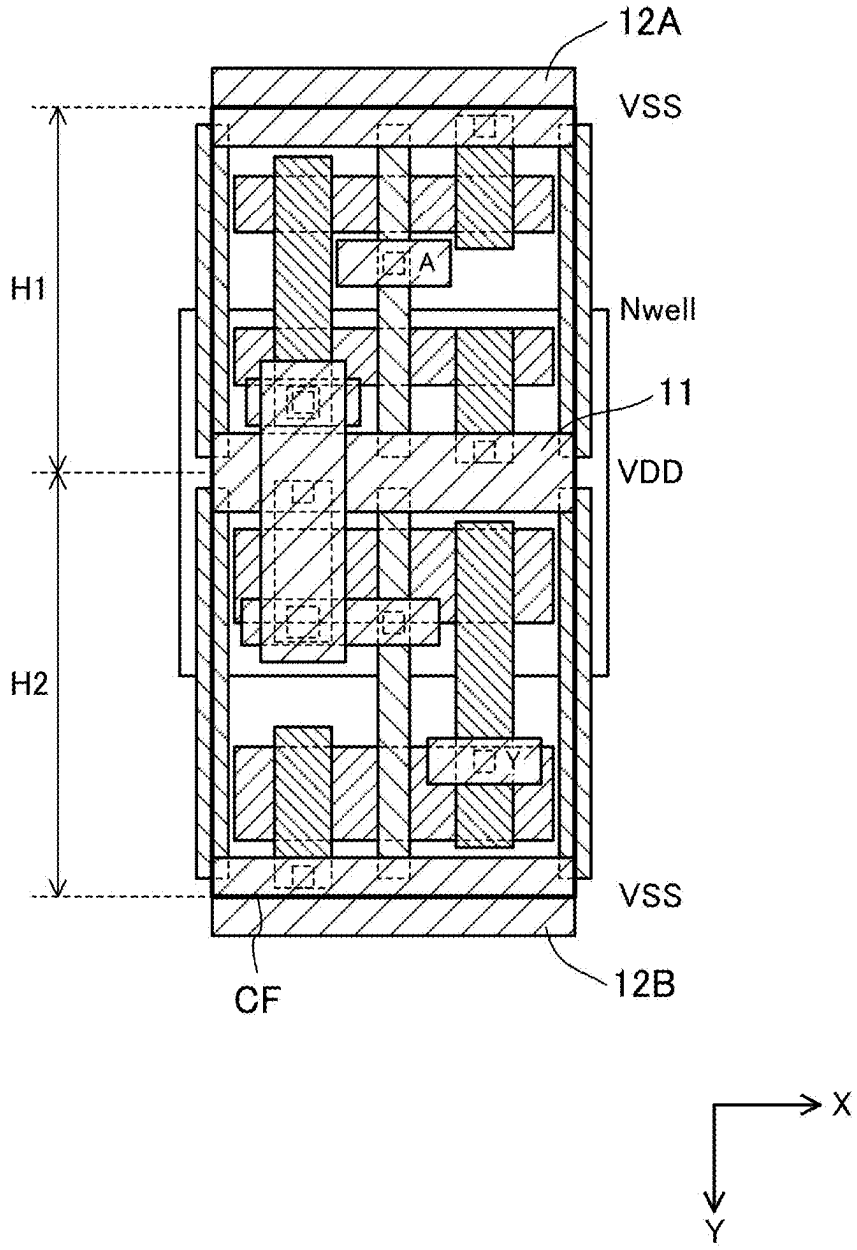


FIG.7

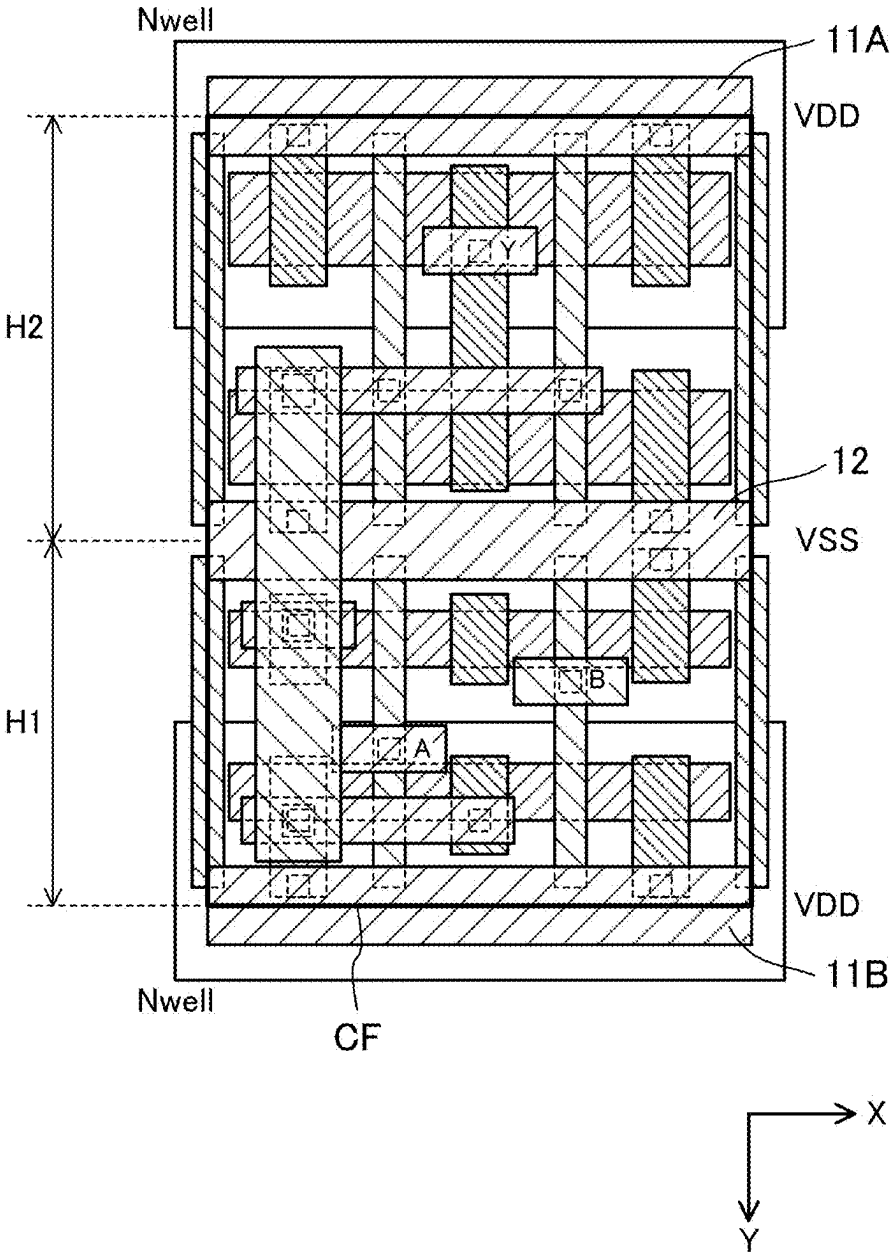


FIG.8

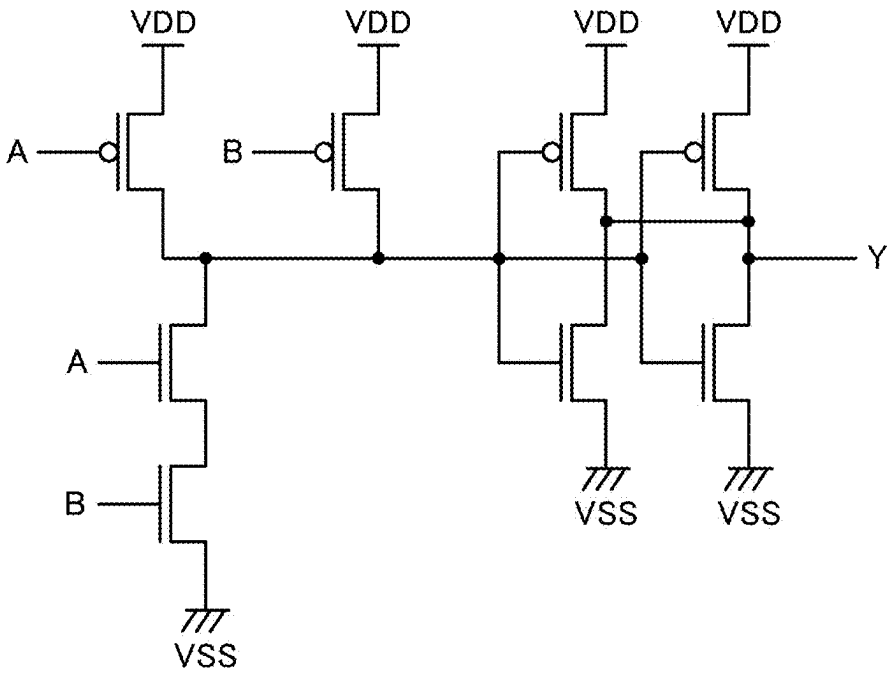


FIG.9

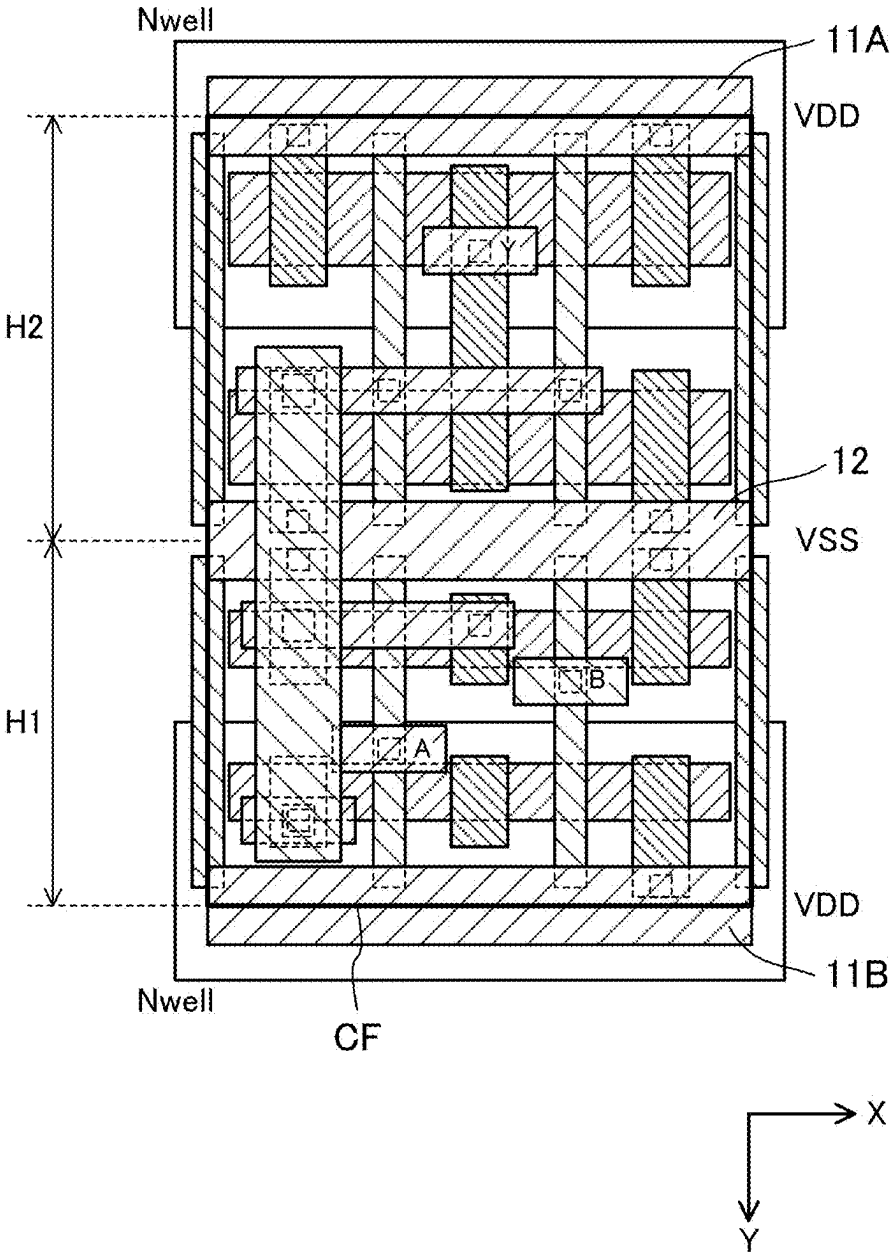


FIG.10

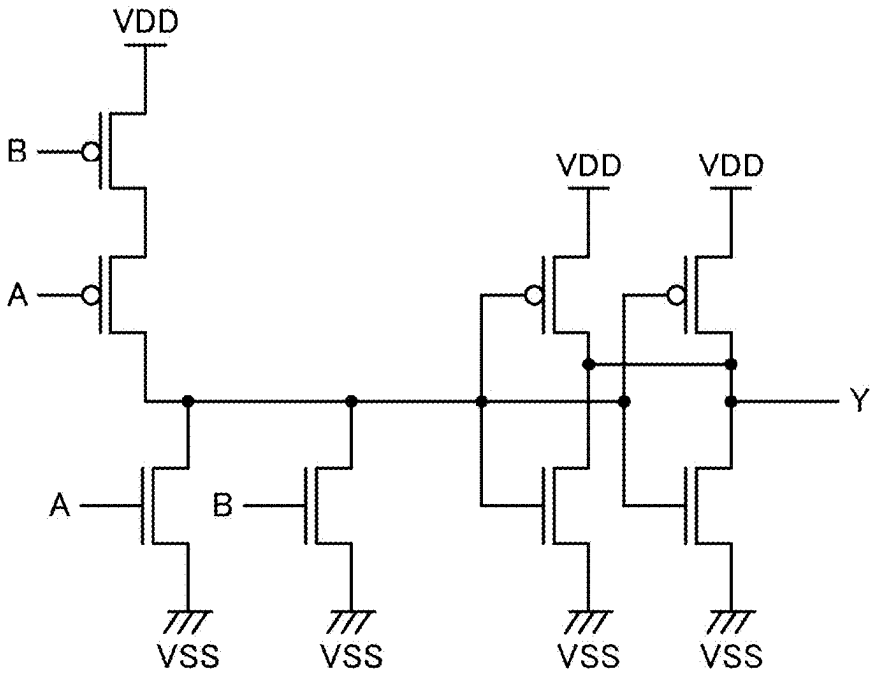


FIG.11

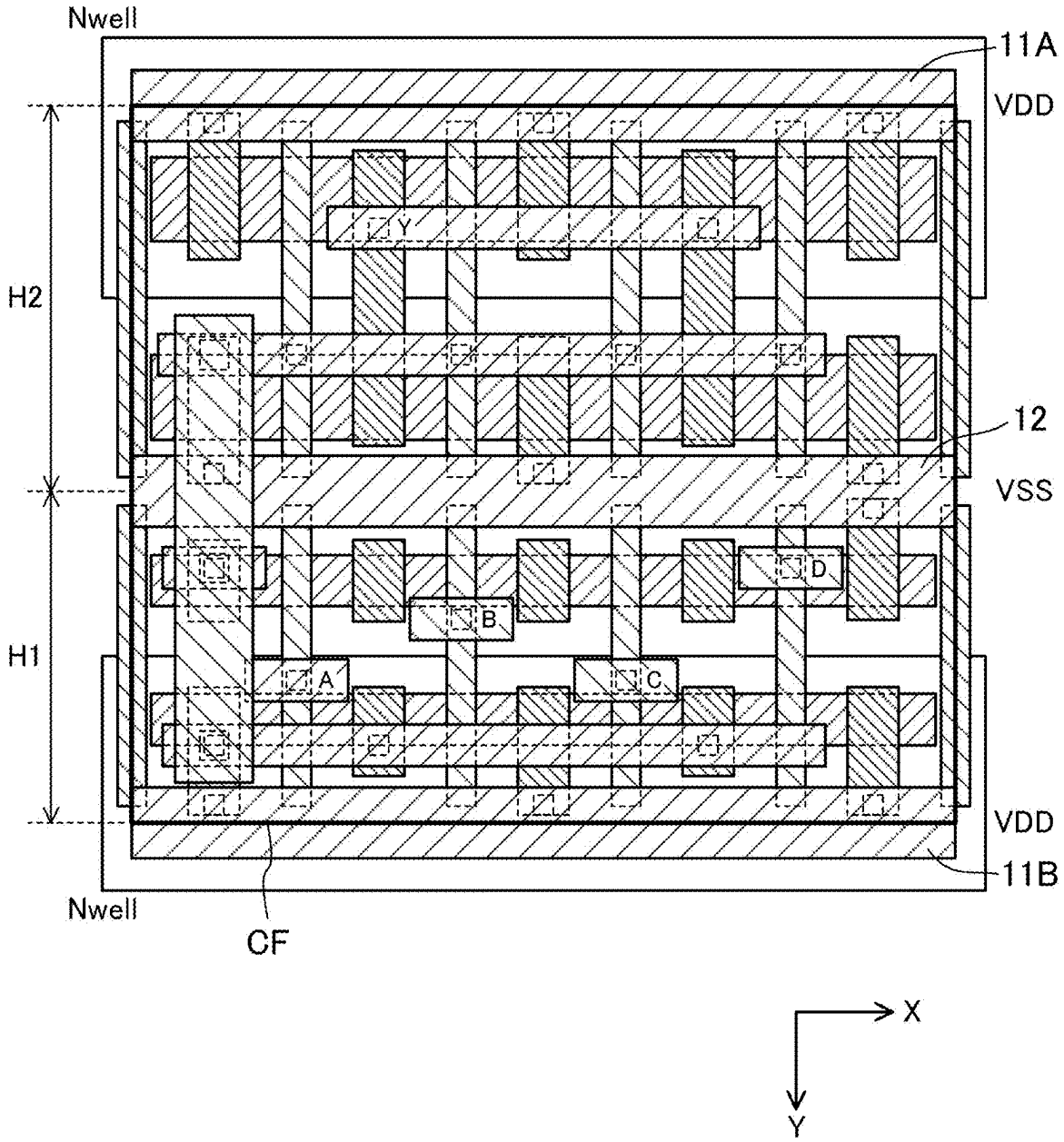


FIG.12

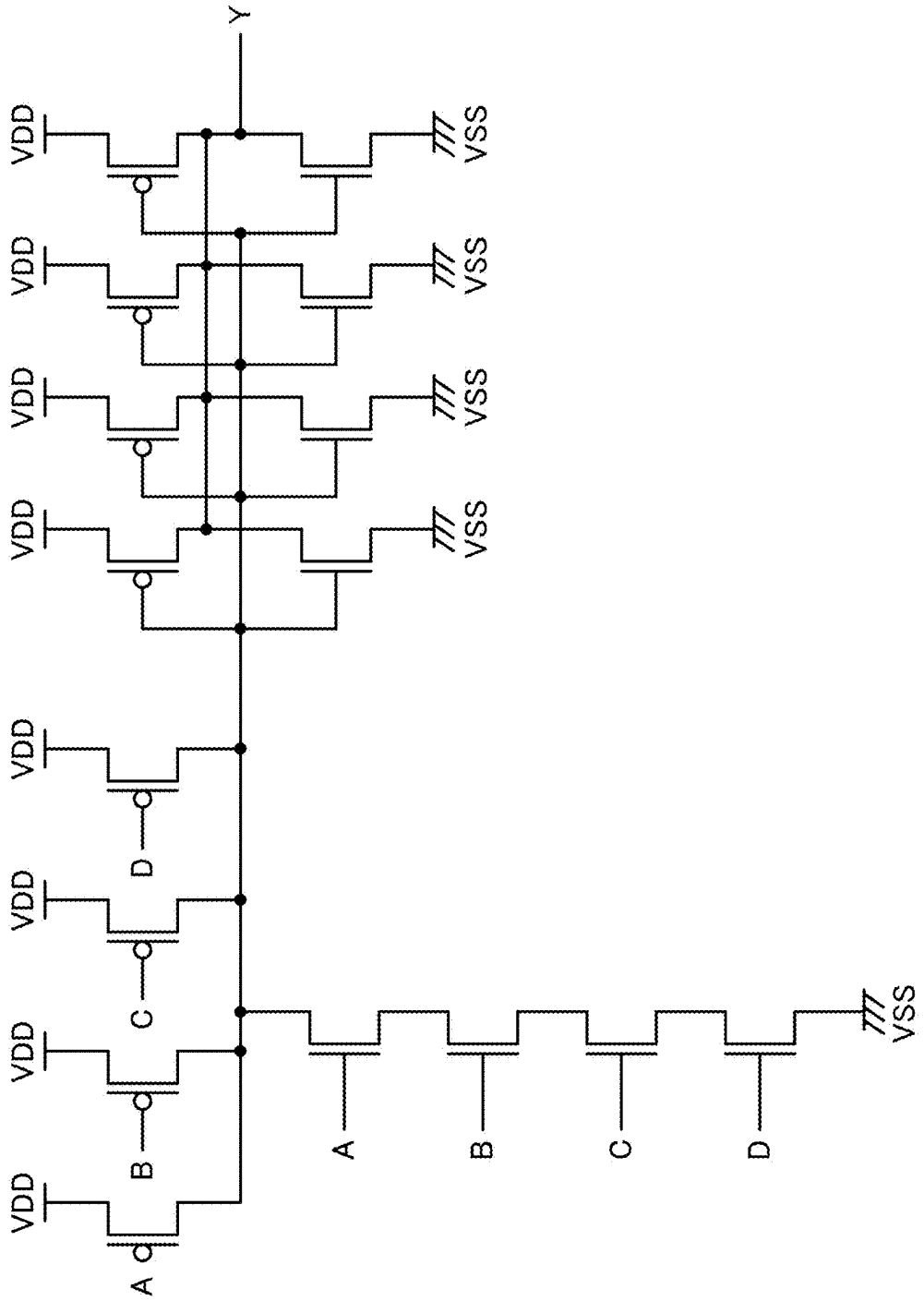


FIG.13

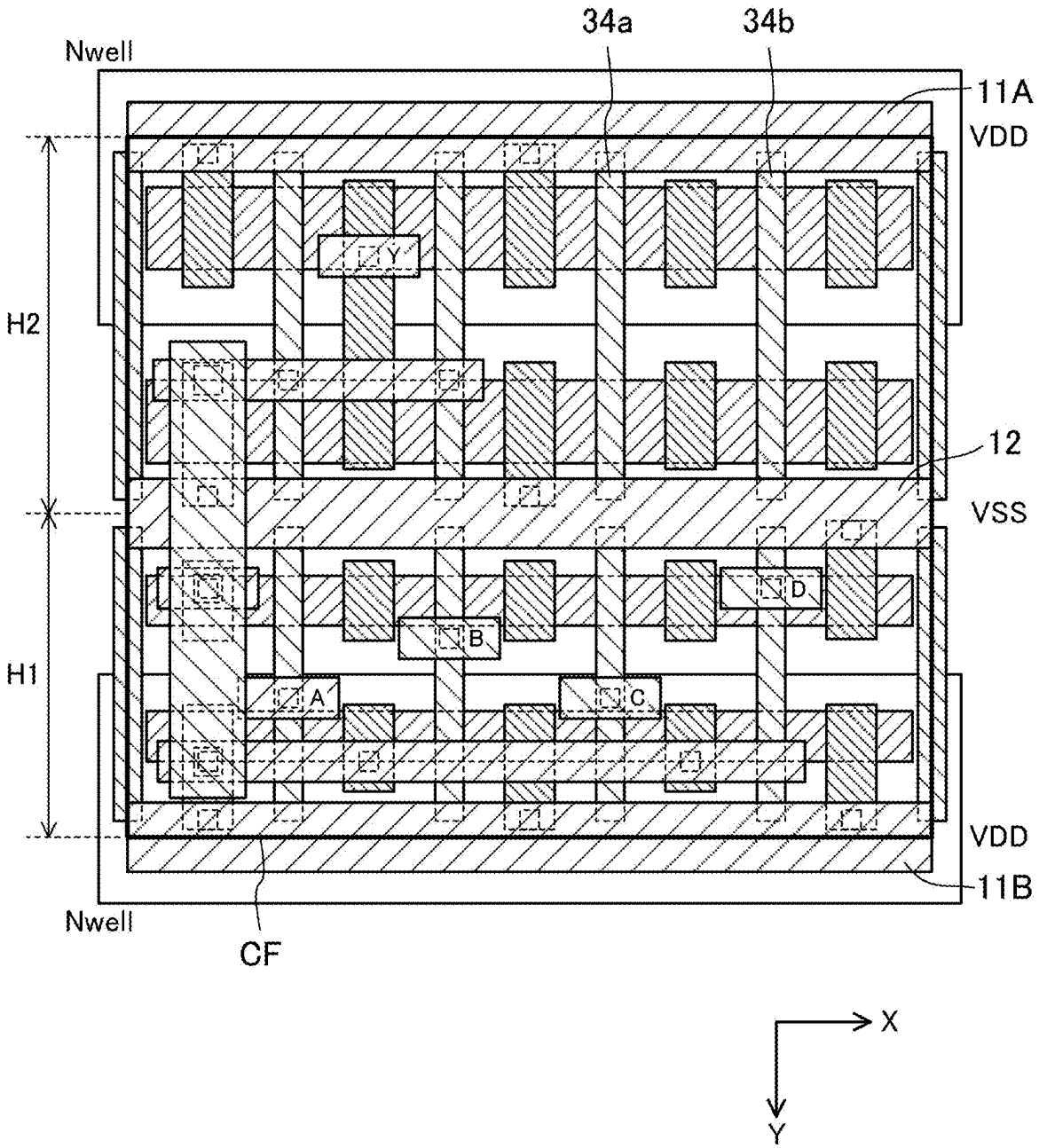


FIG.14

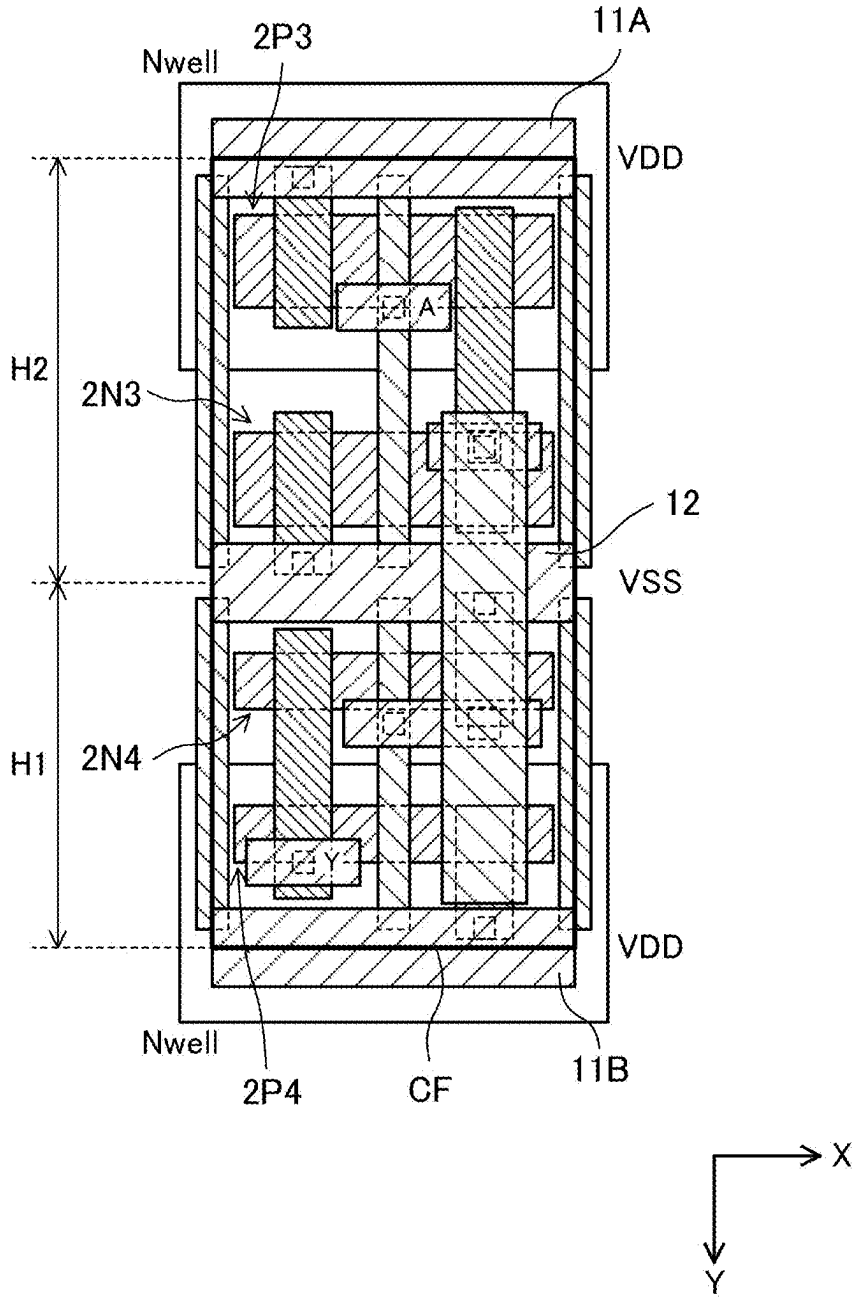


FIG.15

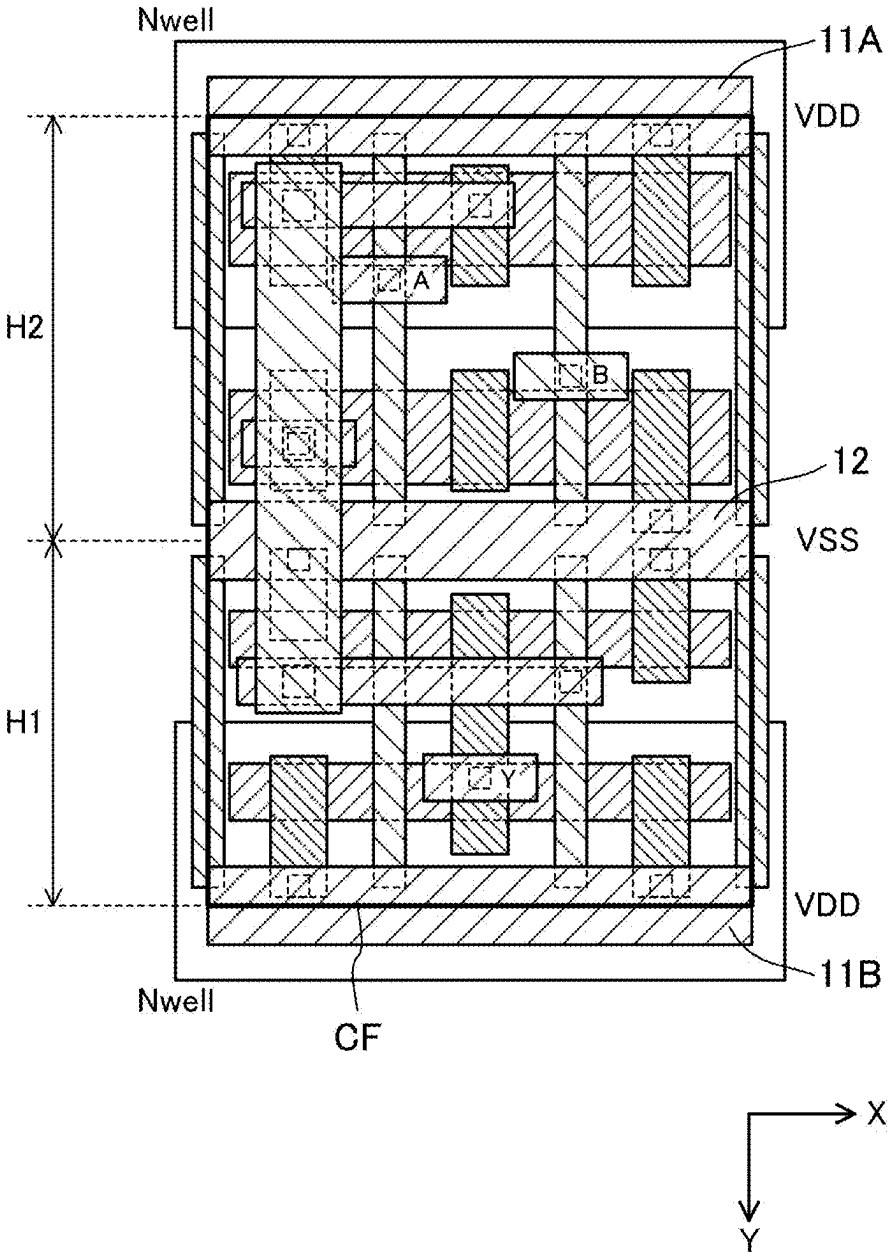
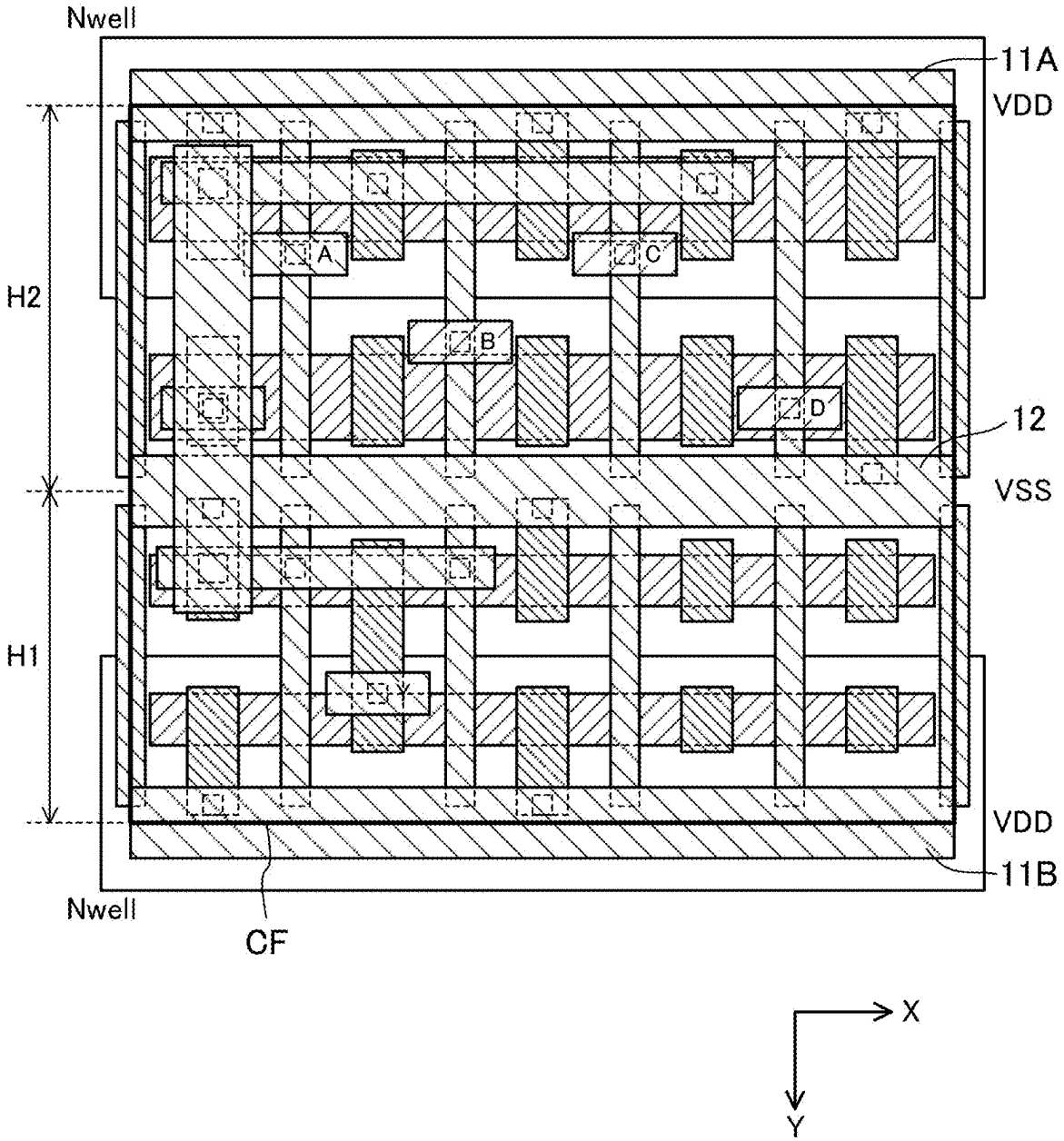


FIG.16



SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This is a continuation of International Application No. PCT/JP2023/041091 filed on Nov. 15, 2023, which claims priority to Japanese Patent Application No. 2022-190002 filed on Nov. 29, 2022. The entire disclosures of these applications are incorporated by reference herein.

BACKGROUND

[0002] The present disclosure relates to a semiconductor integrated circuit device.

[0003] As a method for forming a semiconductor integrated circuit on a semiconductor substrate, a standard cell method is known. The standard cell method is a method in which basic units (e.g., inverters, latches, flipflops, and full adders) having specific logical functions are prepared in advance as standard cells, and a plurality of such standard cells are placed on a semiconductor substrate and connected through interconnects, whereby an LSI chip is designed.

[0004] Also, as for a transistor, which is a basic constituent of an LSI, improvement in integration degree, reduction in operating voltage, and improvement in operating speed have been achieved by reducing (scaling) the gate length. In recent years, however, increase in off current due to excessive scaling and the resulting significant increase in power consumption have raised a problem. To solve this problem, three-dimensional transistors, of which the transistor structure has changed from the conventional planar structure to a three-dimensional structure, have been vigorously studied. A nanosheet FET is one example of such three-dimensional transistors.

[0005] US Patent Application Publication No. 2022/0262786 discloses a semiconductor integrated circuit device in which standard cell rows different in height are arranged alternately and some standard cells lie astride a plurality of standard cell rows.

[0006] The cited patent document describes optimizing the performance of standard cells lying astride a plurality of standard cell rows different in height. However, the cited patent document has not disclosed a specific layout structure of such standard cells.

[0007] An objective of the present disclosure is presenting a layout structure of a standard cell lying astride a plurality of standard cell rows different in height.

SUMMARY

[0008] According to the first mode of the disclosure, a semiconductor integrated circuit device includes: a first power line extending in a first direction and supplying a first power supply voltage; a second power line extending in the first direction and supplying the first power supply voltage; a third power line extending in the first direction between the first power line and the second power line, and supplying a second power supply voltage different from the first power supply voltage; and a standard cell formed between the first power line and the second power line, wherein the spacing between the first power line and the third power line is greater than the spacing between the second power line and the third power line, the standard cell includes a first logic circuit configured to receive an input signal from an input terminal and output a signal to an internal node, and a second logic circuit configured to receive the signal from the internal node and output an output signal to an output terminal, a first transistor constituting the first logic circuit is formed in a region between the second power line and the third power line, and a second transistor constituting the second logic circuit is formed in a region between the first power line and the third power line.

[0009] According to the above mode, the standard cell is formed between the first power line and the second power line, lying astride the third power line. The spacing between the first and third power lines is greater than the spacing between the second and third power lines. The standard cell has a first logic circuit that receives an input signal and outputs a signal to an internal node and a second logic circuit that receives the signal from the internal node and outputs an output signal. First transistors constituting the first logic circuit are formed in a region between the second and third power lines, and second transistors constituting the second logic circuit are formed in a region between the first and third power lines. Therefore, the channel width of the second transistors can be made greater than the channel width of the first transistors. In this way, a circuit small in input capacity and high in output drive capability can be implemented with a small area.

[0010] According to the second mode of the disclosure, a semiconductor integrated circuit device includes: a first power line extending in a first direction and supplying a first power supply voltage; a second power line extending in the first direction and supplying the first power supply voltage; a third power line extending in the first direction between the first power line and the second power line, and supplying a second power supply voltage different from the first power supply voltage; and a standard cell formed between the first power line and the second power line, wherein the spacing between the first power line and the third power line is greater than the spacing between the second power line and the third power line, the standard cell includes a first logic circuit configured to receive an input signal from an input terminal and output a signal to an internal node, and a second logic circuit configured to receive the signal from the internal node and output an output signal to an output terminal, a first transistor constituting the first logic circuit is formed in a region between the first power line and the third power line, and a second transistor constituting the second logic circuit is formed in a region between the second power line and the third power line.

[0011] According to the above mode, the standard cell is formed between the first and second power lines, lying astride the third power line. The spacing between the first and third power lines is greater than the spacing between the second and third power lines. The standard cell has a first logic circuit that receives an input signal and outputs a signal to an internal node and a second logic circuit that receives the signal from the internal node and outputs an output signal. First transistors constituting the first logic circuit are formed in a region between the first and third power lines, and second transistors constituting the second logic circuit are formed in a region between the second and third power lines. Therefore, the channel width of the second transistors can be made smaller than the channel width of the first transistors. Thus, since the output drive capability of the first

logic circuit is great and the input capacity of the second logic circuit is small, the delay inside the standard cell can be reduced.

[0012] According to the present disclosure, a small-area, high-speed semiconductor integrated circuit device can be implemented using a standard cell lying astride a plurality of standard cell rows different in height.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. **1** shows an example of a block layout of a semiconductor integrated circuit device according to an embodiment.

[0014] FIGS. **2**A and **2**B are plan views showing layout structure examples of single-height cells.

[0015] FIG. **3** is a circuit diagram of a buffer circuit.

[0016] FIG. **4** is a plan view showing a layout structure example of a double-height cell according to the first embodiment.

[0017] FIGS. **5**A and **5**B are cross-sectional views of the layout structure of FIG. **4**.

[0018] FIG. **6** is a plan view showing a layout structure example of a double-height cell according to the first embodiment.

[0019] FIG. **7** is a plan view showing a layout structure example of a double-height cell according to the first embodiment.

[0020] FIG. **8** is a circuit diagram of a 2-input AND circuit.

[0021] FIG. **9** is a plan view showing a layout structure example of a double-height cell according to the first embodiment.

[0022] FIG. **10** is a circuit diagram of a 2-input OR circuit.

[0023] FIG. **11** is a plan view showing a layout structure example of a double-height cell according to the first embodiment.

[0024] FIG. **12** is a circuit diagram of a 4-input AND circuit.

[0025] FIG. **13** is a plan view showing a layout structure example of a double-height cell according to the first embodiment.

[0026] FIG. **14** is a plan view showing a layout structure example of a double-height cell according to the second embodiment.

[0027] FIG. **15** is a plan view showing a layout structure example of a double-height cell according to the second embodiment.

[0028] FIG. **16** is a plan view showing a layout structure example of a double-height cell according to the second embodiment.

DETAILED DESCRIPTION

[0029] Embodiments of the present disclosure will be described hereinafter with reference to the accompanying drawings. In the following embodiments, it is assumed that the semiconductor integrated circuit device includes a plurality of standard cells (hereinafter simply called cells as appropriate), and at least some of the standard cells include nanosheet field effect transistors (FETs). The nanosheet FET is a FET using a thin sheet (nanosheet) through which a current flows. Such a nanosheet is formed of silicon, for example.

[0030] As used herein, "VDD" and "VSS" refer to the power supply voltages or the power supplies themselves. Also, as used herein, an expression indicating that sizes such as widths are identical, like the "same wiring width," is to be understood as including a range of manufacturing variations.

[0031] Note that, in the plan views such as FIG. **1**, the horizontal direction in the figure is hereinafter referred to as an X direction (corresponding to the first direction), the vertical direction in the figure as a Y direction (corresponding to the second direction), and the direction perpendicular to the substrate plane as a Z direction.

First Embodiment

[0032] FIG. **1** shows an example of a block layout of a semiconductor integrated circuit device according to an embodiment. The block layout of FIG. **1** is configured by placing standard cells. In FIG. **1**, only the cell frames of standard cells and power lines are illustrated, omitting the internal structures of the standard cells and interconnects between the standard cells.

[0033] In the block layout of FIG. **1**, power lines **11** supplying the power supply voltage VDD and power lines **12** supplying the power supply voltage VSS are laid alternately in the Y direction. Cells are arranged in line in the X direction between the power lines **11** and the power lines **12**, forming cell rows CR**1** and CR**2**. Each of the power lines **11** and **12** is shared by the cell rows CR**1** and CR**2** formed immediately above and below the power line in the figure.

[0034] The height of the cell rows CR**1** is H**1** and the height of the cell rows CR**2** is H**2**, where the height H**2** is greater than the height H**1** (H**2**>H**1**). The cell rows CR**1** and the cell rows CR**2** are arranged alternately in the Y direction.

[0035] Cells C**1** and C**2** are single-height cells. The cell C**1**, placed in the cell row CR**1**, has the height H**1**, and the cell C**2**, placed in the cell row CR**2**, has the height H**2**. Cells C**3** and C**4** are double-height cells. The cells C**3** and C**4**, placed astride the cell rows CR**1** and CR**2**, have a height (H**1**+H**2**). In the cell C**3**, the power line **12** supplying VSS runs across the center portion. In the cell C**4**, the power line **11** supplying VDD runs across the center portion.

[0036] FIGS. **2**A-**2**B are plan views showing layout structure examples of single-height cells in the block layout of FIG. **1**, where FIG. **2**A shows the cell C**1** and FIG. **2**B shows the cell C**2**. Note that, in the block layout of FIG. **1**, the cell C**1** of FIG. **2**A is placed in a vertically flipped position. The power lines **11** and **12** are formed in an M0 interconnect layer that is a metal interconnect layer. CF denotes the cell frame.

[0037] FIG. **3** is a circuit diagram of the single-height cells of FIGS. **2**A and **2**B. As shown in FIG. **3**, the cells C**1** and C**2** of FIGS. **2**A and **2**B are each constituted by two-staged inverters, forming a buffer circuit having an input A and an output Y.

[0038] In the cell C**1** shown in FIG. **2**A, an active region **2**P**1** forming the channels, sources, and drains of p-type transistors is formed in a p-type transistor region on an n-type well (NWell). The active region **2**P**1** includes nanosheets **21***a* and **21***b* each having a structure of three sheets lying one above another and extending in the X direction. An active region **2**N**1** forming the channels, sources, and drains of n-type transistors is formed in an n-type transistor region on a p-type substrate. The active region **2**N**1** includes nanosheets **26***a* and **26***b* each having a structure of three sheets lying one above another and extending in the X direction. Note that, in the active regions, the portions that are to be the sources and the drains on both

sides of the nanosheets are formed by epitaxial growth from the nanosheets. Note also that the active region of the n-type transistors may be formed on a p-type well, not on the p-type substrate.

[0039] Gate interconnects **31***a* and **31***b* extending in parallel in the Y direction are formed from the p-type transistor region over to the n-type transistor region. Also, dummy gate interconnects **38***a* and **38***b* are formed on the side portions of the cell frame CF in the X direction. The dummy gate interconnect **38***a* is shared with a cell placed on the left in the figure, and the dummy gate interconnect **38***b* is shared with a cell placed on the right in the figure. The gate interconnects **31***a* and **31***b* and the dummy gate interconnects **38***a* and **38***b* have the same width and are placed at the same pitch.

[0040] The gate interconnect **31***a* surrounds the peripheries of the nanosheets **21***a* included in the active region **2**P**1** in the Y and Z directions via gate insulating films (not shown). Also, the gate interconnect **31***a* surrounds the peripheries of the nanosheets **26***a* included in the active region **2**N**1** in the Y and Z directions via gate insulating films (not shown). The gate interconnect **31***b* surrounds the peripheries of the nanosheets **21***b* included in the active region **2**P**1** in the Y and Z directions via gate insulating films (not shown). Also, the gate interconnect **31***b* surrounds the peripheries of the nanosheets **26***b* included in the active region **2**N**1** in the Y and Z directions via gate insulating films (not shown).

[0041] Local interconnects **41***a*, **41***b*, **41***c*, and **41***d* (abbreviated as LI in the figures) extending in the Y direction are formed in a local interconnect layer. The local interconnects **41***a* and **41***d* extend from the p-type transistor region over to the n-type transistor region. The local interconnect **41***a* is connected to the portions that are to be the sources or the drains located on the left of the gate interconnect **31***a* in the figure in the active regions **2**P**1** and **2**N**1**. The local interconnect **41***b* is connected to the portion that is to be the source or the drain located between the gate interconnects **31***a* and **31***b* in the active region **2**P**1**. The local interconnect **41***c* is connected to the portion that is to be the source or the drain located between the gate interconnects **31***a* and **31***b* in the active region **2**N**1**. The local interconnect **41***d* is connected to the portions that are to be the sources or the drains located on the right of the gate interconnect **31***b* in the figure in the active regions **2**P**1** and **2**N**1**.

[0042] Metal interconnects **51**, **52**, and **53** extending in the X direction are formed in the M0 interconnect layer in which the power lines **11** and **12** are also formed. The metal interconnect **51** is connected to the local interconnect **41***a* through a via, and also connected to the gate interconnect **31***b* through a via. The metal interconnect **52** is connected to the gate interconnect **31***a* through a via. The metal interconnect **52** corresponds to the input A of the buffer circuit. The metal interconnect **53** is connected to the local interconnect **41***d* through a via. The metal interconnect **53** corresponds to the output Y of the buffer circuit.

[0043] The layout structure of the cell C**2** shown in FIG. **2**B is basically the same as that of the cell C**1** shown in FIG. **2**A. However, since the height H**2** of the cell C**2** is greater than the height H**1** of the cell C**1** (H**2**>H**1**), the size of active regions **2**P**2** and **2**N**2** in the Y direction in the cell C**2** is greater than the size of the active regions **2**P**1** and **2**N**1** in the Y direction in the cell C**1**. That is, the width of nanosheets **22***a* and **22***b* and nanosheets **27***a* and **27***b* in the cell C**2** is greater than the width of the nanosheets **21***a* and **21***b* and the nanosheets **26***a* and **26***b* in the cell C**1** (note that the width of nanosheets herein refers to the width or the size in the Y direction in the figure). Therefore, the output drive capability of the cell C**2** is greater than the output drive capability of the cell C**1**. Also, the input capacity of the cell C**2** is greater than the input capacity of the cell C**1**.

[0044] FIG. **4** is a plan view showing a layout structure example of the double-height cell C**3** in the block layout of FIG. **1**. FIGS. **5**A and **5**B are cross-sectional views of the layout structure of FIG. **4**, where FIG. **5**A is a cross section taken along line Y**1**-Y**1'** and FIG. **5**B is a cross section taken along line Y**2**-Y**2'**. The circuit structure of the cell C**3** of FIGS. **4**, **5**A, and **5**B is as shown in FIG. **3**, that is, constituted by two-staged inverters, forming a buffer circuit having an input A and an output Y. The input-side inverter corresponds to the first logic circuit according to the present disclosure, and the output-side inverter corresponds to the second logic circuit according to the present disclosure.

[0045] As shown in FIG. **4**, in the cell C**3**, the power line **12** supplying VSS is laid in the center portion in the Y direction. Also, power lines **11**A and **11**B supplying VDD are laid in both end portions in the Y direction. In the region between the power lines **11**A and **12**, having the height H**2**, transistors constituting the output-side inverter of the buffer circuit are formed. In the region between the power lines **11**B and **12**, having the height H**1**, transistors constituting the input-side inverter of the buffer circuit are formed.

[0046] An active region **2**N**3** forming the channel, source, and drain of an n-type transistor is formed in an n-type transistor region on the upper side of the power line **12** in the figure. The active region **2**N**3** includes nanosheets **23***a* having a structure of three sheets lying one above another and extending in the X direction. An active region **2**N**4** forming the channel, source, and drain of an n-type transistor is formed in an n-type transistor region on the lower side of the power line **12** in the figure. The active region **2**N**4** includes nanosheets **23***b* having a structure of three sheets lying one above another and extending in the X direction.

[0047] An active region **2**P**3** forming the channel, source, and drain of a p-type transistor is formed in a p-type transistor region on the lower side of the power line **11**A, which is laid in the upper end portion, in the figure. The active region **2**P**3** includes nanosheets **28***a* having a structure of three sheets lying one above another and extending in the X direction. An active region **2**P**4** forming the channel, source, and drain of a p-type transistor is formed in a p-type transistor region on the upper side of the power line **11**B, which is laid in the lower end portion, in the figure. The active region **2**P**4** includes nanosheets **28***b* having a structure of three sheets lying one above another and extending in the X direction.

[0048] A gate interconnect **33***a* extending in the Y direction is formed in the region between the power lines **11**A and **12**, and dummy gate interconnects **39***a* and **39***b* are formed on the side portions of the cell frame CF in the X direction. The dummy gate interconnect **39***a* is shared with a cell placed on the left in the figure, and the dummy gate interconnect **39***b* is shared with a cell placed on the right in the figure. The gate interconnect **33***a* and the dummy gate interconnects **39***a* and **39***b* have the same width and are placed at the same pitch.

[0049] The gate interconnect **33***a* surrounds the peripheries of the nanosheets **28***a* included in the active region **2**P**3**

in the Y and Z directions via gate insulating films (not shown). Also, the gate interconnect **33***a* surrounds the peripheries of the nanosheets **23***a* included in the active region **2**N**3** in the Y and Z directions via gate insulating films (not shown).

[0050] A gate interconnect **33***b* extending in the Y direction is formed in the region between the power lines **11**B and **12**, and dummy gate interconnects **39***c* and **39***d* are formed on the side portions of the cell frame CF in the X direction. The dummy gate interconnect **39***c* is shared with a cell placed on the left in the figure, and the dummy gate interconnect **39***d* is shared with a cell placed on the right in the figure. The gate interconnect **33***b* and the dummy gate interconnects **39***c* and **39***d* have the same width and are placed at the same pitch.

[0051] The gate interconnect **33***b* surrounds the peripheries of the nanosheets **28***b* included in the active region **2**P**4** in the Y and Z directions via gate insulating films (not shown). Also, the gate interconnect **33***b* surrounds the peripheries of the nanosheets **23***b* included in the active region **2**N**4** in the Y and Z directions via gate insulating films (not shown).

[0052] Local interconnects **43***a*, **43***b*, **43***c*, **43***d*, **43***e*, and **43***f* extending in the Y direction are formed in a local interconnect layer. The local interconnect **43***a* is connected to the portion that is to be the source or the drain located on the left of the gate interconnect **33***a* in the figure in the active region **2**P**3**, and also connected to the power line **11**A through a via. The local interconnect **43***b* is connected to the portion that is to be the source or the drain located on the left of the gate interconnect **33***a* in the figure in the active region **2**N**3**, and also connected to the power line **12** through a via. The local interconnect **43***c* is connected to the portions that are to be the sources or the drains located on the left of the gate interconnect **33***b* in the figure in the active regions **2**N**4** and **2**P**4**.

[0053] The local interconnect **43***d* is connected to the portions that are to be the sources or the drains located on the right of the gate interconnect **33***a* in the figure in the active regions **2**N**3** and **2**P**3**. The local interconnect **43***e* is connected to the portion that is to be the source or the drain located on the right of the gate interconnect **33***b* in the figure in the active region **2**N**4**, and also connected to the power line **12** through a via. The local interconnect **43***f* is connected to the portion that is to be the source or the drain located on the right of the gate interconnect **33***b* in the figure in the active region **2**P**4**, and also connected to the power line **11**B through a via

[0054] Metal interconnects **54**, **55**, **56**, and **57** extending in the X direction are formed in an M0 interconnect layer in which the power lines **11**A, **11**B, and **12** are also formed. The metal interconnect **54** is connected to the gate interconnect **33***a* through a via. The metal interconnect **55** is connected to the local interconnect **43***d* through a via, and corresponds to the output terminal Y of the buffer circuit. The metal interconnect **56** is connected to the gate interconnect **33***b* through a via, and corresponds to the input terminal A of the buffer circuit. The metal interconnect **57** is connected to the local interconnect **43***c* through a via.

[0055] A metal interconnect **61** extending in the Y direction is formed in an M1 interconnect layer that is a metal interconnect layer located above the M0 interconnect layer. The metal interconnect **61** is connected to the metal interconnects **54** and **57** through vias, and corresponds to the inner node of the buffer circuit.

[0056] In the double-height cell C**3** shown in FIGS. **4**, **5**A, and **5**B, the height H**2** of the region between the power lines **11**A and **12** is greater than the height H**1** of the region between the power lines **11**B and **12** (H**2**>H**1**). Therefore, the size of the active regions **2**P**3** and **2**N**3** in the Y direction is greater than the size of the active regions **2**P**4** and **2**N**4** in the Y direction. That is, the width of the nanosheets **23***a* and **28***a* of the transistors constituting the output-side inverter is greater than the width of the nanosheets **23***b* and **28***b* of the transistors constituting the input-side inverter. The cell C**3** can therefore implement a buffer circuit small in input capacity (equivalent to that of the cell C**1**) and high in output drive capability (equivalent to that of the cell C**2**) with a small area. As a result, a high-speed, small-area semiconductor integrated circuit device can be implemented. This is particularly effective when the output drive capability of a cell connected to the input A of the cell C**3** is small and when the load capacity due to a cell or cells and interconnects connected to the output Y is large.

[0057] FIG. **6** is a plan view showing a layout structure example of the double-height cell C**4** in the block layout of FIG. **1**. The circuit structure of the cell C**4** of FIG. **6** is as shown in FIG. **3**, that is, constituted by two-staged inverters, forming a buffer circuit having an input A and an output Y.

[0058] As shown in FIG. **6**, in the cell C**4**, the power line **11** supplying VDD is laid in the center portion in the Y direction. Also, power lines **12**A and **12**B supplying VSS are laid in both end portions in the Y direction. In the region between the power lines **11** and **12**A, having the height H**1**, transistors constituting the input-side inverter of the buffer circuit are formed. In the region between the power lines **11** and **12**B, having the height H**2**, transistors constituting the output-side inverter of the buffer circuit are formed.

[0059] Since the layout structure of the cell C**4** of FIG. **6** can be easily known by analogy from the layout structure of the cell C**3** shown in FIGS. **4**, **5**A, and **5**B, detailed description is omitted here.

[0060] The double-height cell C**4** of FIG. **6** can obtain similar effects to those obtained by the double-height cell C**3** shown in FIGS. **4**, **5**A, and **5**B. That is, the height H**2** of the region between the power lines **11** and **12**B is greater than the height H**1** of the region between the power lines **11** and **12**A (H**2**>H**1**). Therefore, the width of the nanosheets of the transistors constituting the output-side inverter is greater than the width of the nanosheets of the transistors constituting the input-side inverter. The cell C**4** can therefore implement a buffer circuit small in input capacity (equivalent to that of the cell C**1**) and high in output drive capability (equivalent to that of the cell C**2**) with a small area. As a result, a high-speed, small-area semiconductor integrated circuit device can be implemented. This is particularly effective when the output drive capability of a cell connected to the input A of the cell C**4** is small and when the load capacity due to a cell or cells and interconnects connected to the output Y is large.

<Other Layout Structure Examples>

[0061] Other layout structure examples of the double-height cell C**3** according to this embodiment will be described. Note that, in the following examples, the layout structure shown in FIGS. **4**, **5**A, and **5**B is used as the basic

configuration, and description may be omitted for configurations that can be easily known by analogy from the above description.

(1) 2-Input AND Circuit

[0062] FIG. **7** is a plan view showing another layout structure of the double-height cell C**3**. The layout structure of FIG. **7** has a cell width ½ times that of FIG. **4**. The cell C**3** shown in FIG. **7** implements a 2-input AND circuit shown in FIG. **8**. The 2-input AND circuit shown in FIG. **8** includes a NAND gate at the first stage and an inverter at the second stage. The second-stage inverter is constituted by two inverters connected in parallel. The first-stage NAND gate corresponds to the first logic circuit according to the present disclosure, and the second-stage inverter corresponds to the second logic circuit according to the present disclosure.

[0063] As shown in FIG. **7**, in the cell C**3**, the power line **12** supplying VSS is laid in the center portion in the Y direction. Also, the power lines **11**A and **11**B supplying VDD are laid in both end portions in the Y direction. In the region between the power lines **11**A and **12**, having the height H**2**, transistors constituting the second-stage inverter of the 2-input AND circuit are formed. In the region between the power lines **11**B and **12**, having the height H**1**, transistors constituting the first-stage NAND gate of the 2-input AND circuit are formed.

[0064] In the double-height cell C**3** of FIG. **7**, the width of the nanosheets of the transistors constituting the second-stage inverter is greater than the width of the nanosheets of the transistors constituting the first-stage NAND gate. Therefore, the cell C**3** can implement a 2-input AND circuit small in input capacity (equivalent to that of the cell C**1**) and high in output drive capability (equivalent to double that of the cell C**2** because two inverters are connected in parallel) with a small area.

(2) 2-Input OR Circuit

[0065] FIG. **9** is a plan view showing yet another layout structure of the double-height cell C**3**. The layout structure of FIG. **9** has a cell width ½ times that of FIG. **4**. The cell C**3** shown in FIG. **9** implements a 2-input OR circuit shown in FIG. **10**. The 2-input OR circuit shown in FIG. **10** includes a NOR gate at the first stage and an inverter at the second stage. The second-stage inverter is constituted by two inverters connected in parallel. The first-stage NOR gate corresponds to the first logic circuit according to the present disclosure, and the second-stage inverter corresponds to the second logic circuit according to the present disclosure.

[0066] As shown in FIG. **9**, in the cell C**3**, the power line **12** supplying VSS is laid in the center portion in the Y direction. Also, the power lines **11**A and **11**B supplying VDD are laid in both end portions in the Y direction. In the region between the power lines **11**A and **12**, having the height H**2**, transistors constituting the second-stage inverter of the 2-input OR circuit are formed. In the region between the power lines **11**B and **12**, having the height H**1**, transistors constituting the first-stage NOR gate of the 2-input OR circuit are formed.

[0067] In the double-height cell C**3** of FIG. **9**, the width of the nanosheets of the transistors constituting the second-stage inverter is greater than the width of the nanosheets of the transistors constituting the first-stage NOR gate. Therefore, the cell C**3** can implement a 2-input OR circuit small in input capacity (equivalent to that of the cell C**1**) and high in output drive capability (equivalent to double that of the cell C**2** because two inverters are connected in parallel) with a small area.

(3) 4-Input AND Circuit

[0068] FIG. **11** is a plan view showing yet another layout structure of the double-height cell C**3**. The layout structure of FIG. **11** has a cell width ⅝ times that of FIG. **4**. The cell C**3** shown in FIG. **11** implements a 4-input AND circuit shown in FIG. **12**. The 4-input AND circuit shown in FIG. **12** includes a 4-input NAND gate at the first stage and an inverter at the second stage. The second-stage inverter is constituted by four inverters connected in parallel. The first-stage 4-input NAND gate corresponds to the first logic circuit according to the present disclosure, and the second-stage inverter corresponds to the second logic circuit according to the present disclosure.

[0069] As shown in FIG. **11**, in the cell C**3**, the power line **12** supplying VSS is laid in the center portion in the Y direction. Also, the power lines **11**A and **11**B supplying VDD are laid in both end portions in the Y direction. In the region between the power lines **11**A and **12**, having the height H**2**, transistors constituting the second-stage inverter of the 4-input AND circuit are formed. In the region between the power lines **11**B and **12**, having the height H**1**, transistors constituting the first-stage 4-input NAND gate of the 4-input AND circuit are formed.

[0070] In the double-height cell C**3** of FIG. **11**, the width of the nanosheets of the transistors constituting the second-stage inverter is greater than the width of the nanosheets of the transistors constituting the first-stage NAND gate. Therefore, the cell C**3** can implement a 4-input AND circuit small in input capacity (equivalent to that of the cell C**1**) and high in output drive capability (equivalent to four times that of the cell C**2** because four inverters are connected in parallel) with a small area.

(4) Another 4-Input AND Circuit

[0071] FIG. **13** is a plan view showing yet another layout structure of the double-height cell C**3**. The layout structure of FIG. **13** has a cell width ⅝ times that of FIG. **4**. The cell C**3** shown in FIG. **13** implements a 4-input AND circuit, like the layout structure of FIG. **11**. In FIG. **13**, however, the second-stage inverter is constituted by two inverters connected in parallel, not four inverters connected in parallel.

[0072] As shown in FIG. **13**, in the cell C**3**, the power line **12** supplying VSS is laid in the center portion in the Y direction. Also, the power lines **11**A and **11**B supplying VDD are laid in both end portions in the Y direction. In the region between the power lines **11**A and **12**, having the height H**2**, transistors constituting the second-stage inverter of the 4-input AND circuit are formed. Note here that transistors constituted by gate interconnects **34***a* and **34***b* are dummy transistors that do not contribute to circuit operation. That is, the cell C**3** of FIG. **13** includes dummy transistors. In the region between the power lines **11**B and **12**, having the height H**1**, transistors constituting the first-stage NAND gate of the 4-input AND circuit are formed.

[0073] In the double-height cell C**3** of FIG. **13**, the width of the nanosheets of the transistors constituting the second-stage inverter is greater than the width of the nanosheets of

the transistors constituting the first-stage NAND gate. Therefore, the cell C**3** can implement a 4-input AND circuit small in input capacity (equivalent to that of the cell C**1**) and high in output drive capability (equivalent to double that of the cell C**2** because two inverters are connected in parallel) with a small area.

Second Embodiment

[0074] FIG. **14** is a plan view showing a layout structure example of the double-height cell C**3** according to the second embodiment. The circuit structure of the cell C**3** of FIG. **14** is as shown in FIG. **3**, that is, constituted by two-staged inverters, forming a buffer circuit having an input A and an output Y.

[0075] In the layout structure of FIG. **14**, in comparison with the layout structure of FIG. **4**, the positions of the input-side inverter and the output-side inverter are changed with each other vertically in the figure. That is, in FIG. **14**, transistors constituting the input-side inverter of the buffer circuit are formed in the region between the power lines **11**A and **12** having the height H**2**. Transistors constituting the output-side inverter of the buffer circuit are formed in the region between the power lines **11**B and **12** having the height H**1**. Note that, since the layout structure of FIG. **14** can be easily known by analogy from the description in the first embodiment, detailed description is omitted here.

[0076] In the double-height cell C**3** shown in FIG. **14**, the height H**2** of the region between the power lines **11**A and **12** is greater than the height H**1** of the region between the power lines **11**B and **12** (H**2**>H**1**). Therefore, the size of active regions **2**P**3** and **2**N**3** in the Y direction is greater than the size of active regions **2**P**4** and **2**N**4** in the Y direction. That is, the width of the nanosheets of transistors constituting the input-side inverter is greater than the width of the nanosheets of transistors constituting the output-side inverter. Therefore, in the cell C**3**, while the input capacity is great (equivalent to that of the cell C**2**), the output drive capability of the input-side inverter is great. Also, the input capacity of the output-side inverter is small. As a result, the delay inside the cell from the input-side inverter to the output-side inverter becomes small.

[0077] Therefore, when the output drive capability of a cell connected to the input A is sufficiently great and the load capacity due to a cell or cells and interconnects connected to the output Y is small, a small-area, high-speed semiconductor integrated circuit device can be implemented.

<Other Layout Structure Examples>

[0078] Other layout structure examples of the double-height cell C**3** according to this embodiment will be described. Note that description may be omitted for configurations that can be easily known by analogy from the above description.

(1) 2-Input AND Circuit

[0079] FIG. **15** is a plan view showing another layout structure of the double-height cell C**3**. The layout structure of FIG. **15** has a cell width ⅔ times that of FIG. **14**. The cell C**3** shown in FIG. **15** implements a 2-input AND circuit shown in FIG. **8**.

[0080] In the layout structure of FIG. **15**, in comparison with the layout structure of FIG. **7**, the positions of the first-stage NAND gate and the second-stage inverter are changed with each other vertically in the figure. That is, transistors constituting the first-stage NAND gate of the 2-input AND circuit are formed in the region between the power lines **11**A and **12** having the height H**2**. Transistors constituting the second-stage inverter of the 2-input AND circuit are formed in the region between the power lines **11**B and **12** having the height H**1**.

[0081] In the double-height cell C**3** of FIG. **15**, the width of the nanosheets of transistors constituting the first-stage NAND gate is greater than the width of the nanosheets of transistors constituting the second-stage inverter. Therefore, in the cell C**3**, while the input capacity is great (equivalent to that of the cell C**2**), the output drive capability of the first-stage NAND gate is great. Also, the input capacity of the second-stage inverter is small. As a result, the delay inside the cell from the NAND gate to the inverter becomes small.

[0082] Therefore, when the output drive capabilities of cells connected to the inputs A and B are sufficiently great and the load capacity due to a cell or cells and interconnects connected to the output Y is small, a small-area, high-speed semiconductor integrated circuit device can be implemented.

(2) 4-Input AND Circuit

[0083] FIG. **16** is a plan view showing yet another layout structure of the double-height cell C**3**. The layout structure of FIG. **16** has a cell width ⅚ times that of FIG. **14**. The cell C**3** shown in FIG. **16** implements a 4-input AND circuit same in layout structure as that of FIG. **13**.

[0084] In the layout structure of FIG. **16**, in comparison with the layout structure of FIG. **13**, the positions of the first-stage 4-input NAND gate and the second-stage inverter are changed with each other vertically in the figure. That is, transistors constituting the first-stage 4-input NAND gate of the 4-input AND circuit are formed in the region between the power lines **11**A and **12** having the height H**2**. Transistors constituting the second-stage inverter of the 4-input AND circuit are formed in the region between the power lines **11**B and **12** having the height H**1**.

[0085] In the double-height cell C**3** of FIG. **16**, the width of the nanosheets of transistors constituting the first-stage 4-input NAND gate is greater than the width of the nanosheets of transistors constituting the second-stage inverter. Therefore, in the cell C**3**, while the input capacity is great (equivalent to that of the cell C**2**), the output drive capability of the first-stage 4-input NAND gate is great. Also, the input capacity of the second-stage inverter is small. As a result, the delay inside the cell from the NAND gate to the inverter becomes small.

[0086] Therefore, when the output drive capabilities of cells connected to the inputs A, B, C, and D are sufficiently great and the load capacity due to a cell or cells and interconnects connected to the output Y is small, a small-area, high-speed semiconductor integrated circuit device can be implemented.

[0087] While the nanosheets have the structure of three sheets lying one above another and the cross-sectional shape of the sheet structure is illustrated as a rectangle in the above embodiments, the number of sheets, and the cross-sectional shape, of the structure of the nanosheets are not limited to these.

[0088] According to the present disclosure, the performance of a standard cell lying astride a plurality of standard cell rows different in height can be improved. The present disclosure is therefore useful for reduction in the area, and increase in the speed, of a semiconductor integrated circuit device, for example.

1. A semiconductor integrated circuit device, comprising:
a first power line extending in a first direction and supplying a first power supply voltage;
a second power line extending in the first direction and supplying the first power supply voltage;
a third power line extending in the first direction between the first power line and the second power line, and supplying a second power supply voltage different from the first power supply voltage; and
a standard cell formed between the first power line and the second power line, wherein
the spacing between the first power line and the third power line is greater than the spacing between the second power line and the third power line,
the standard cell includes
a first logic circuit configured to receive an input signal from an input terminal and output a signal to an internal node, and
a second logic circuit configured to receive the signal from the internal node and output an output signal to an output terminal,
a first transistor constituting the first logic circuit is formed in a region between the second power line and the third power line, and
a second transistor constituting the second logic circuit is formed in a region between the first power line and the third power line.

2. The semiconductor integrated circuit device of claim **1**, wherein
the first and second transistors are nanosheet field effect transistors (FETs), and
the width of the nanosheet of the second transistor is greater than the width of the nanosheet of the first transistor.

3. The semiconductor integrated circuit device of claim **1**, wherein
the standard cell includes
a dummy transistor that does not contribute to a logical function of the circuit.

4. A semiconductor integrated circuit device, comprising:
a first power line extending in a first direction and supplying a first power supply voltage;
a second power line extending in the first direction and supplying the first power supply voltage;
a third power line extending in the first direction between the first power line and the second power line, and supplying a second power supply voltage different from the first power supply voltage; and
a standard cell formed between the first power line and the second power line, wherein
the spacing between the first power line and the third power line is greater than the spacing between the second power line and the third power line,
the standard cell includes
a first logic circuit configured to receive an input signal from an input terminal and output a signal to an internal node, and
a second logic circuit configured to receive the signal from the internal node and output an output signal to an output terminal,
a first transistor constituting the first logic circuit is formed in a region between the first power line and the third power line, and
a second transistor constituting the second logic circuit is formed in a region between the second power line and the third power line.

5. The semiconductor integrated circuit device of claim **4**, wherein
the first and second transistors are nanosheet field effect transistors (FETs), and
the width of the nanosheet of the second transistor is smaller than the width of the nanosheet of the first transistor.

6. The semiconductor integrated circuit device of claim **4**, wherein
the standard cell includes
a dummy transistor that does not contribute to a logical function of the circuit.

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