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(54) **3D INTEGRATED CIRCUIT INCLUDING PROTECTION CIRCUIT**

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(57) **ABSTRACT**

A 3D integrated circuit includes a first integrated circuit including a first substrate. A second integrated circuit is stacked on the first integrated circuit. A through via extends through the first substrate and electrically connects the first integrated circuit and the second integrated circuit to one another. A plurality of protection circuits is disposed at opposite sides of the through via in a keep-out zone surrounding the through via and is electrically connected to the through via.

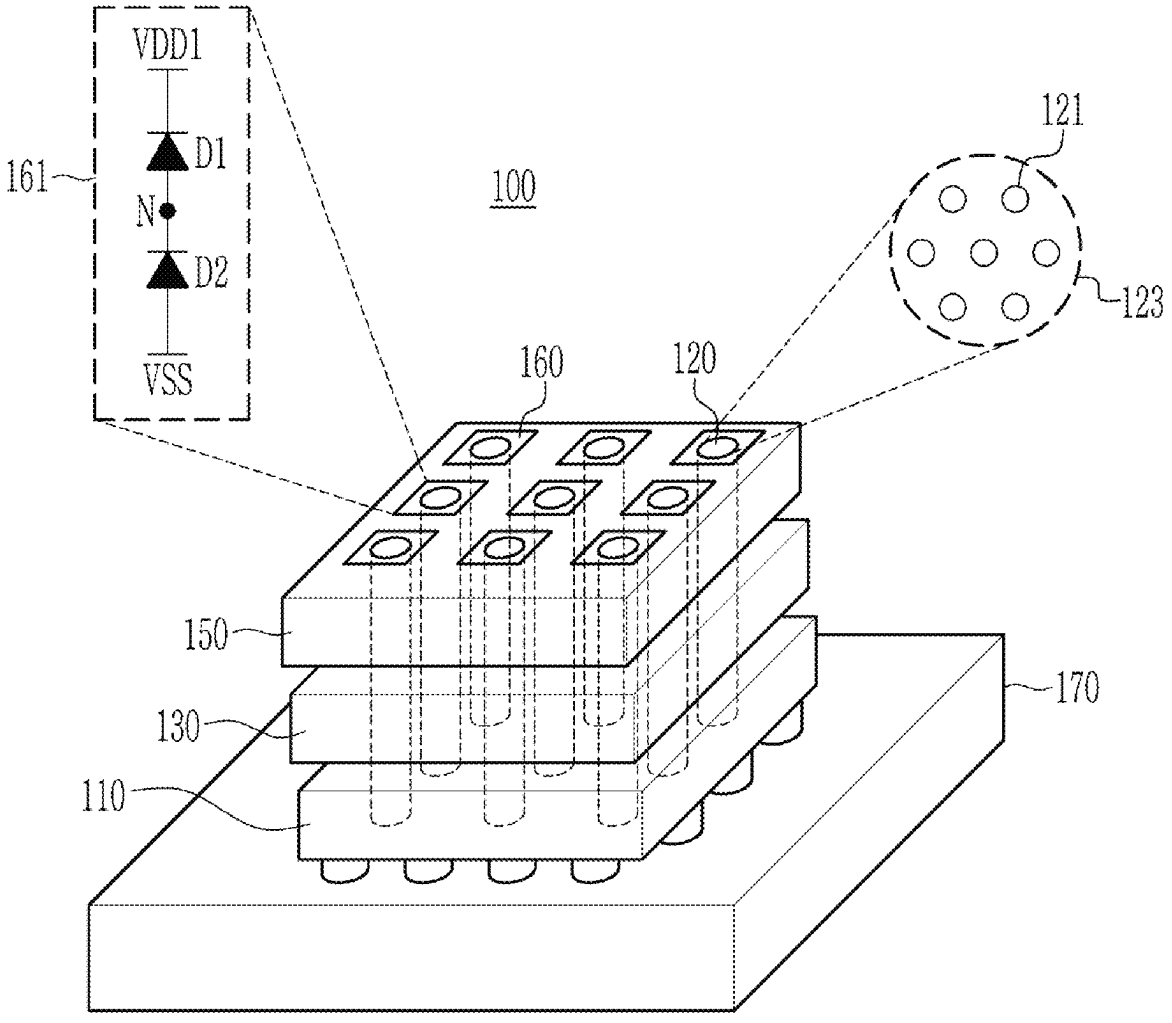


FIG. 1

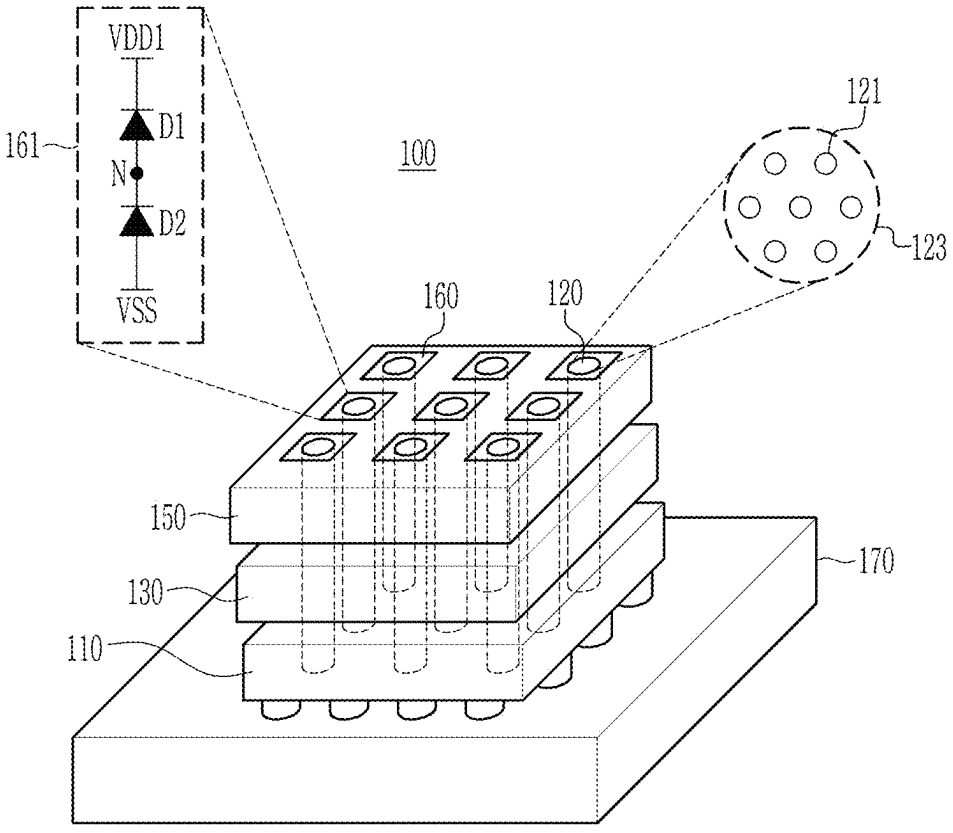


FIG. 2

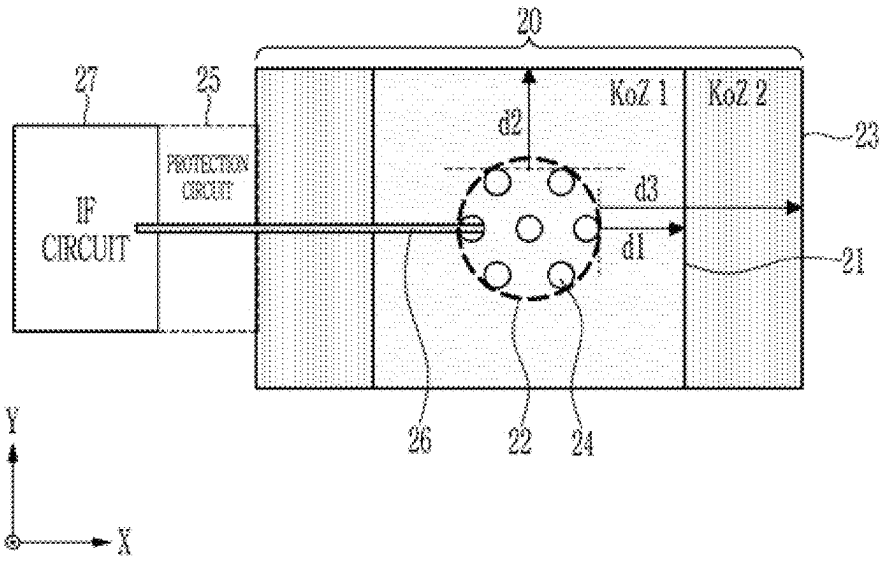

20
27
25
KoZ 1
KoZ 2
d2
23
PROTECTION CIRCUIT
IF CIRCUIT
d3
d1
21
26
22
24
Y
X

FIG. 3

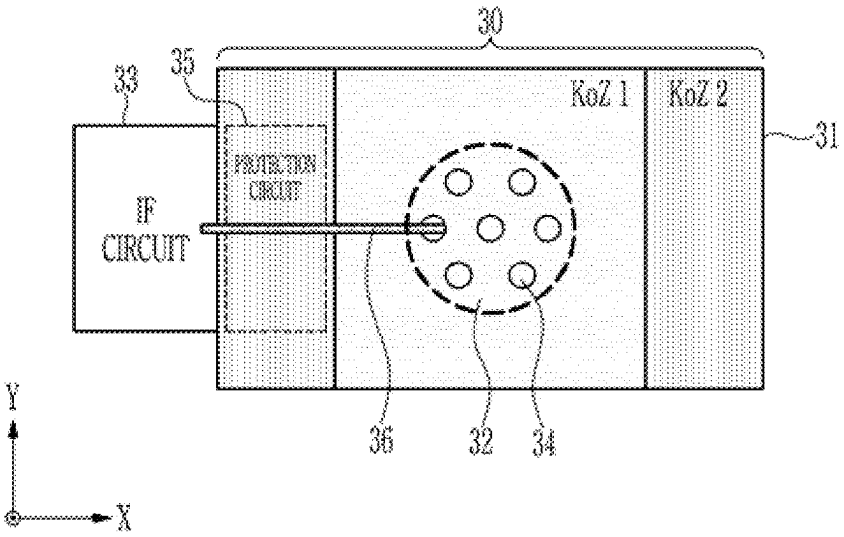

30
35
33
KoZ 1
KoZ 2
31
PROTECTION CIRCUIT
IF CIRCUIT
36
32
34
Y
X

FIG. 4

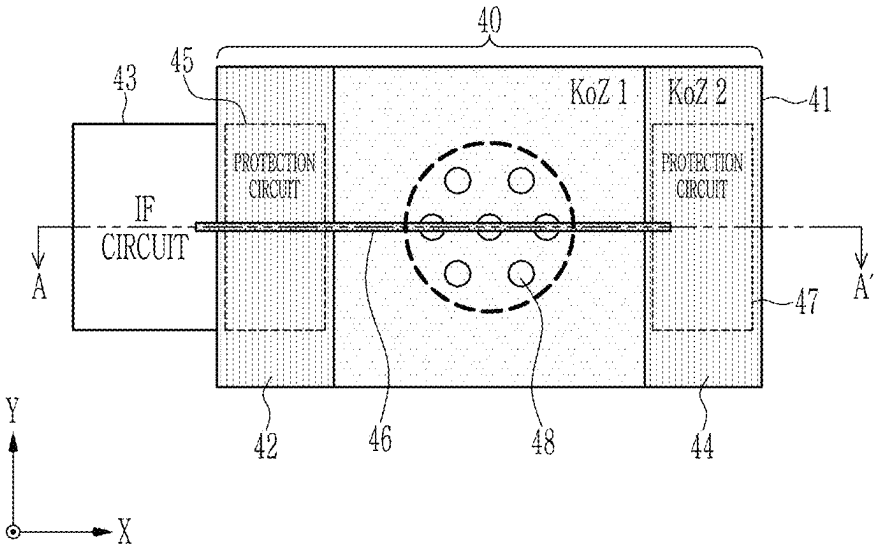

40
45
43
KoZ 1
KoZ 2
41
PROTECTION CIRCUIT
PROTECTION CIRCUIT
IF CIRCUIT
A
A'
47
Y
X
42
46
48
44

FIG. 5

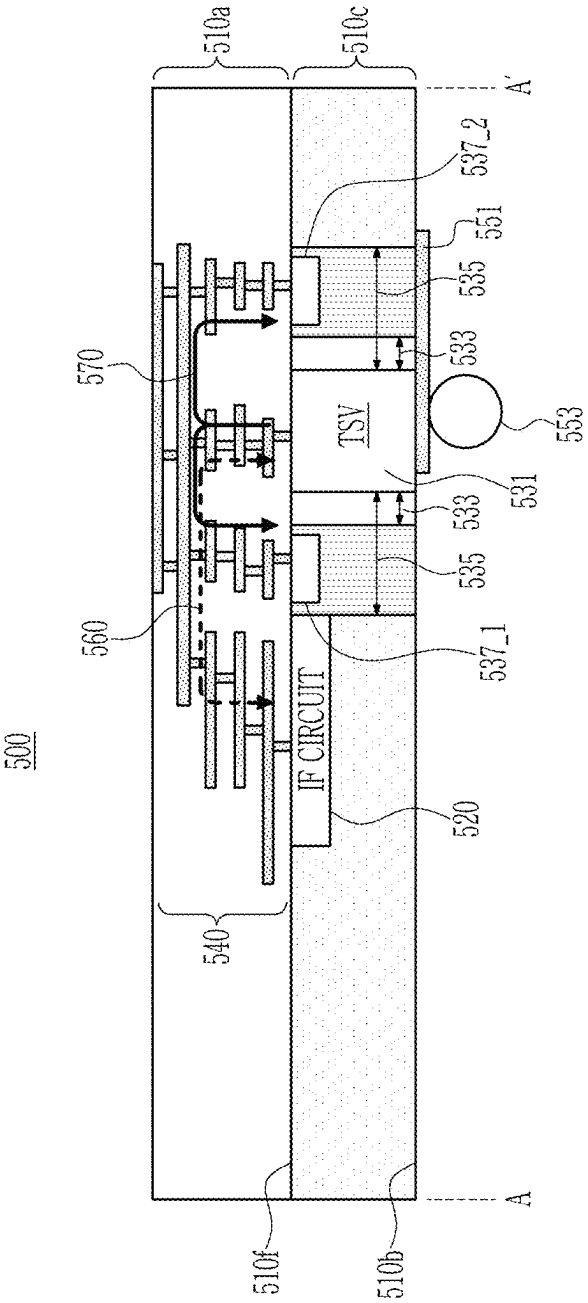

500
510a
510c
A'
A
537_2
551
535
533
570
TSV
553
531
533
535
560
537_1
IF CIRCUIT
520
540
510f
510b

FIG. 6

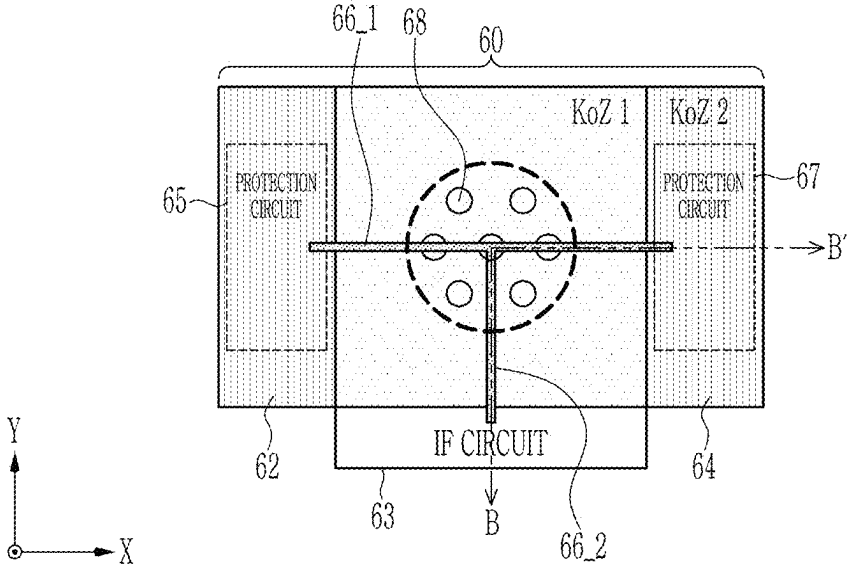

66_1
68
60
KoZ 1
KoZ 2
PROTECTION CIRCUIT
PROTECTION CIRCUIT
65
67
B'
IF CIRCUIT
62
63
B
66_2
64
Y
X

FIG. 7

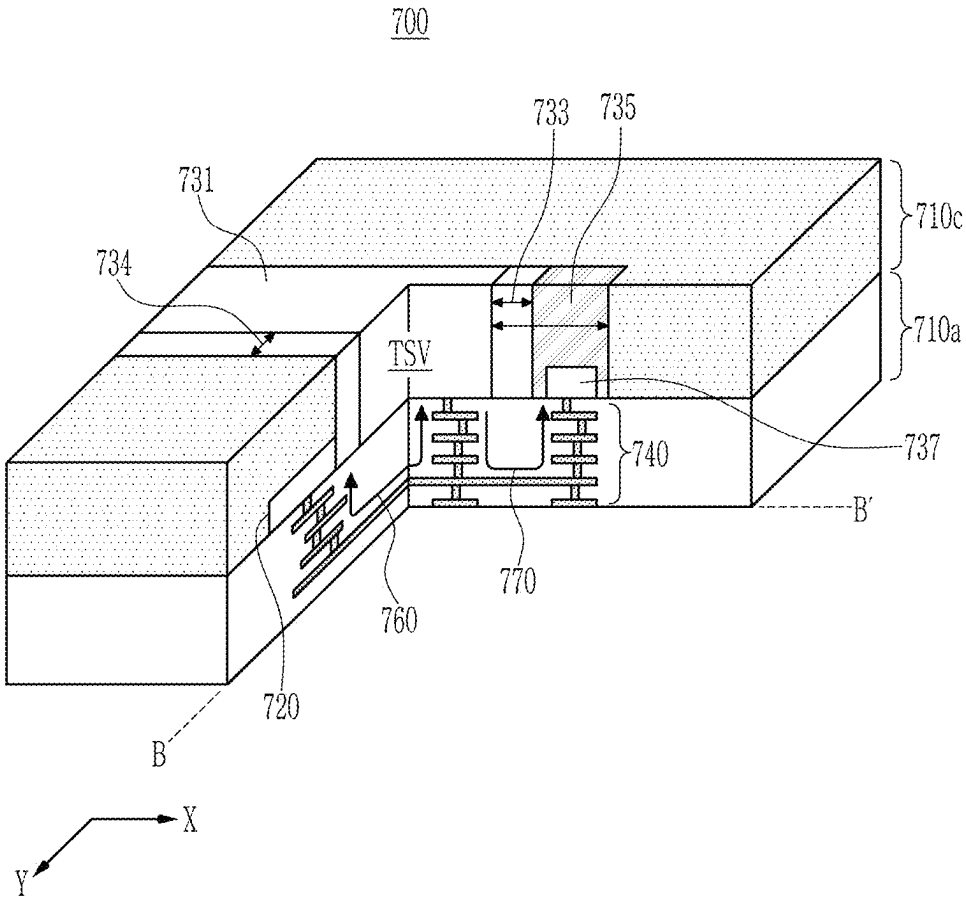
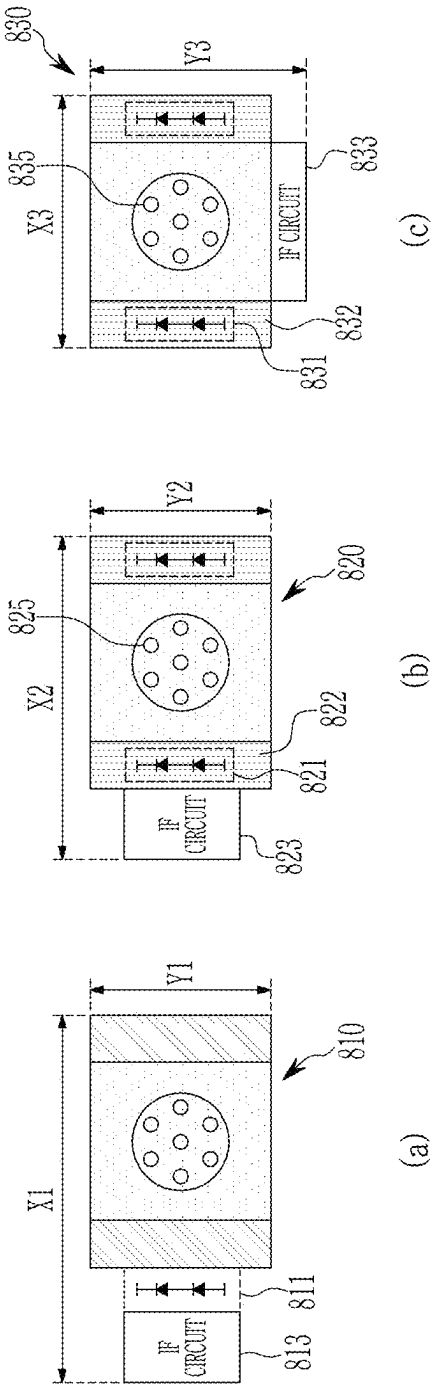


FIG. 8



	(a)	(b)	(c)
SIZE (X(um) x Y(um))	23 x 10	18.5 x 10	14 x 14
Area (um2)	230	185	196
Area Ratio	-	80.43%	85.22%

(d)

FIG. 9

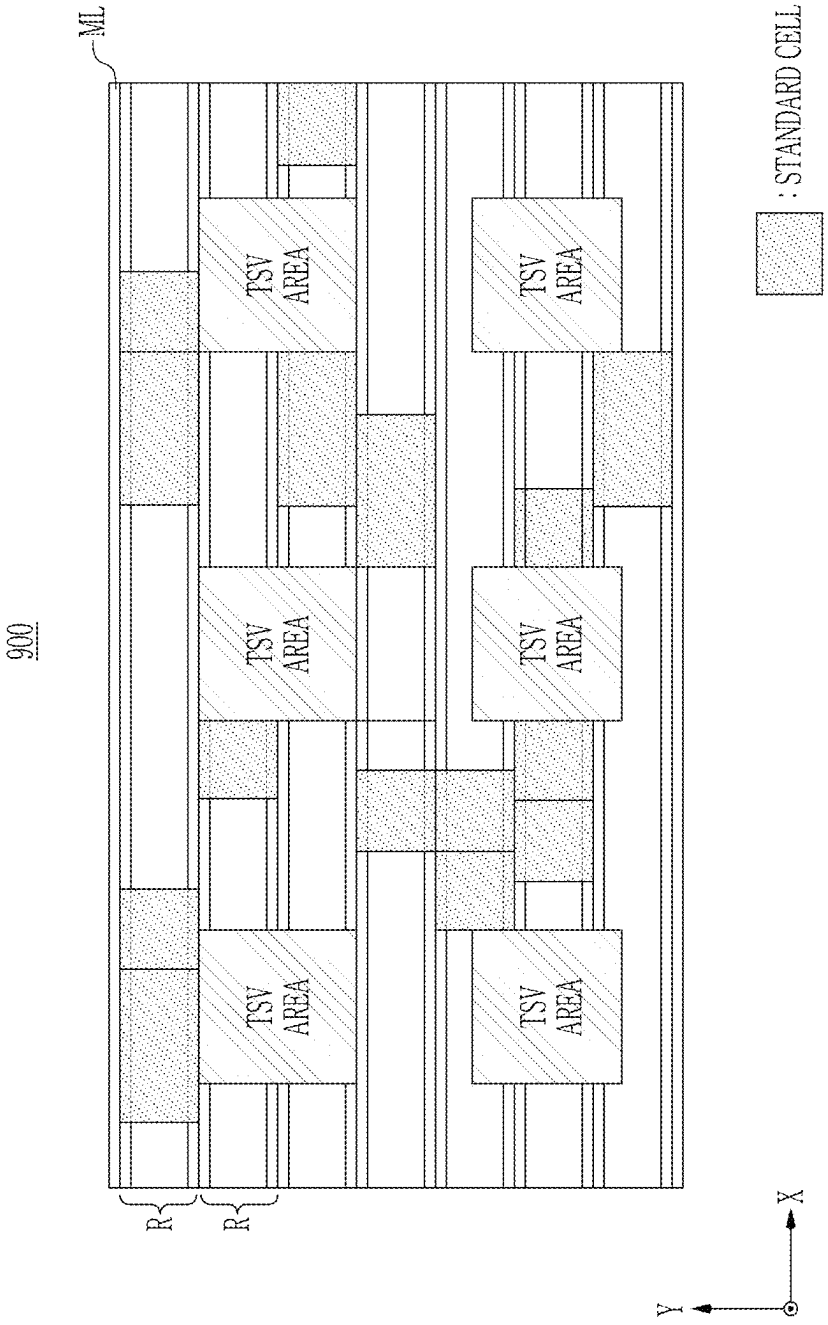

900
ML
TSV AREA
TSV AREA
TSV AREA
TSV AREA
TSV AREA
TSV AREA
R
R
: STANDARD CELL
X
Y

FIG. 10

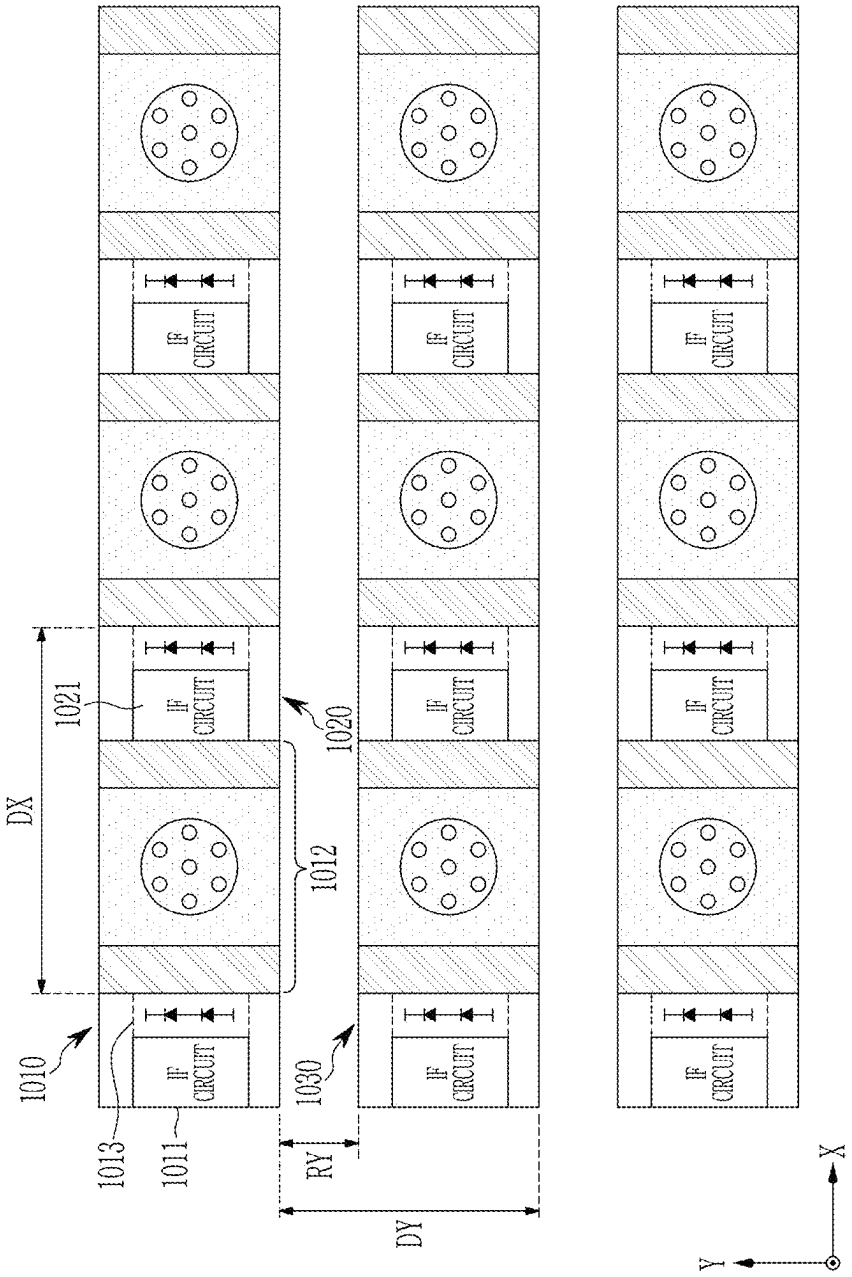


FIG. 11

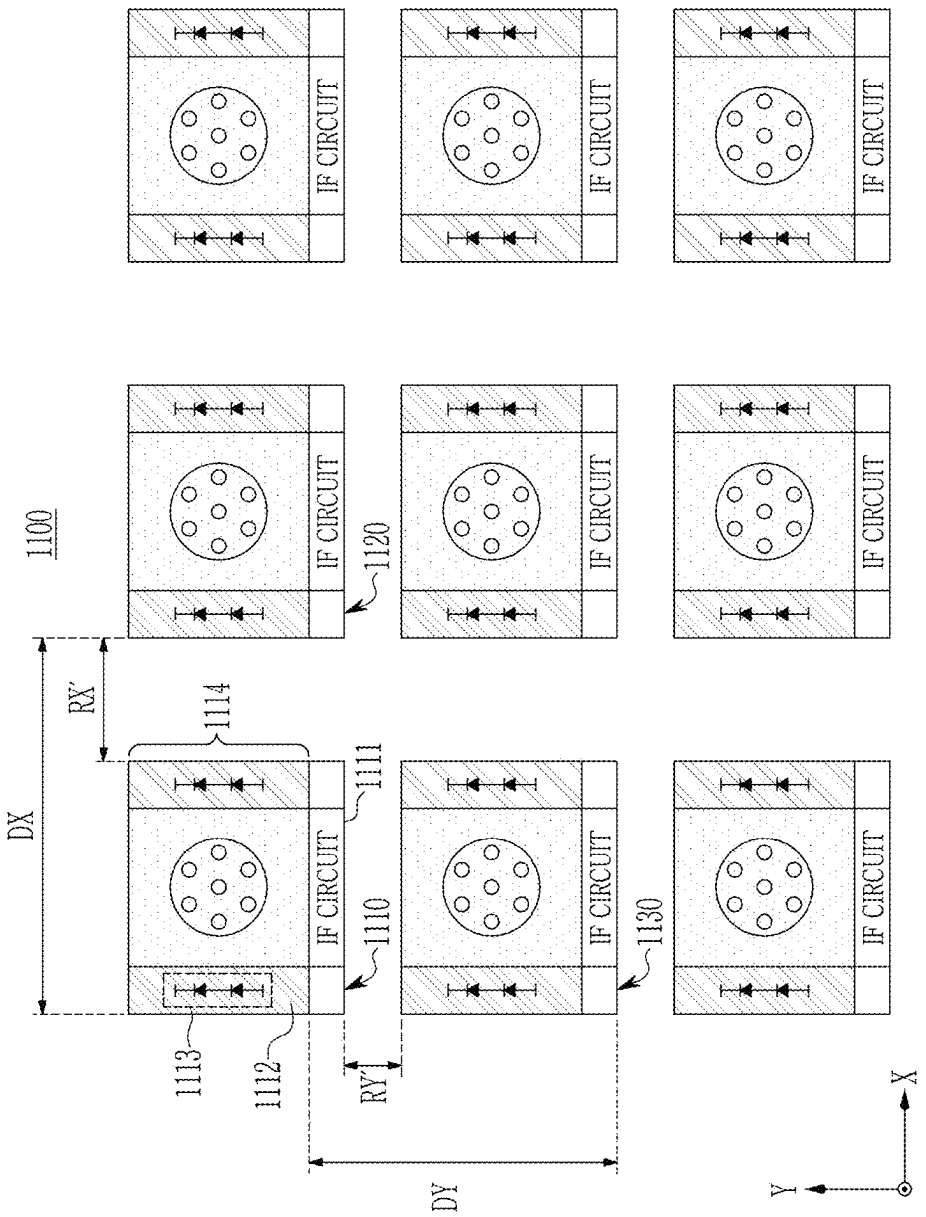

1100
IF CIRCUIT
1120
1114
1111
1110
1130
1113
1112
RX'
RY'
DX
DY
Y
X

FIG. 12

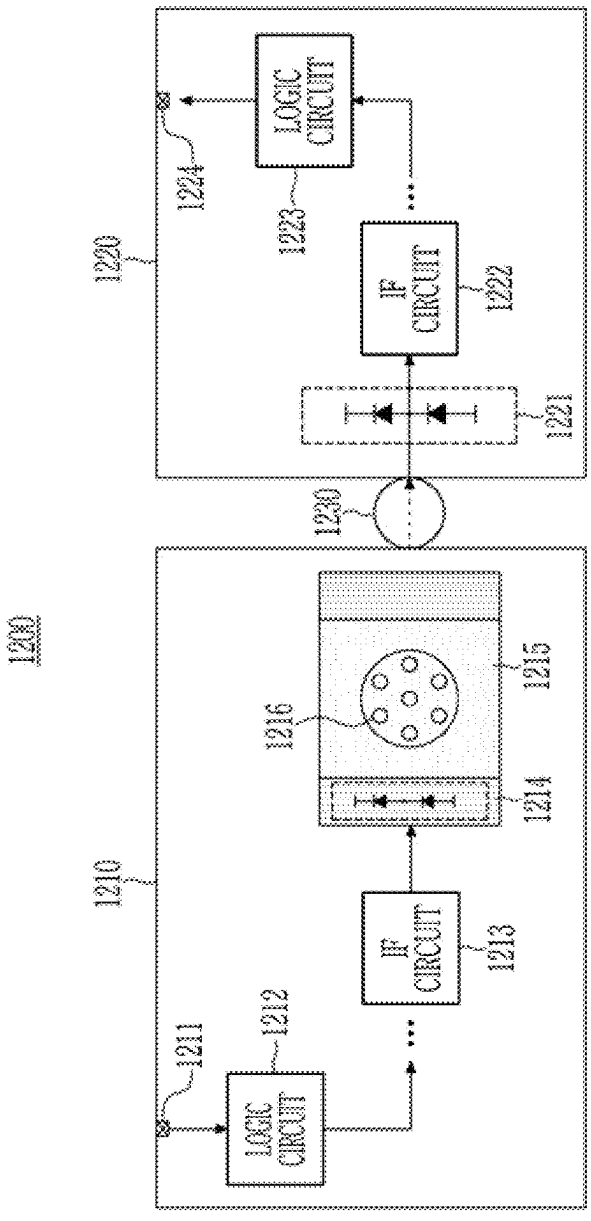
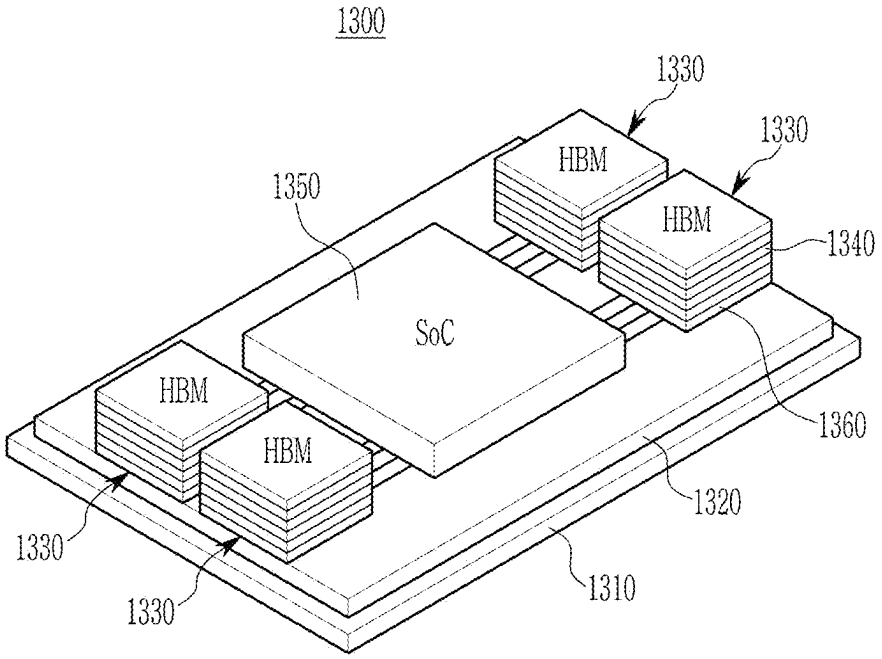

1200
1210
1211
1212
LOGIC CIRCUIT
IF CIRCUIT
1213
1214
1215
1216
1220
1221
1222
1223
1224
LOGIC CIRCUIT
IF CIRCUIT

FIG. 13


1300
1330
1330
HBM
HBM
1350
1340
SoC
HBM
HBM
1360
1320
1330
1330
1310

3D INTEGRATED CIRCUIT INCLUDING PROTECTION CIRCUIT

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to Korean Patent Application No. 10-2024-0025314, filed in the Korean Intellectual Property Office on Feb. 21, 2024, and Korean Patent Application No. 10-2024-0050823, filed in the Korean Intellectual Property Office on Apr. 16, 2024, the entire contents of which are incorporated herein by reference.

TECHNICAL FIELD

[0002] The present disclosure relates to an integrated circuit and, more specifically, to a three-dimensional (3D) integrated circuit (IC) including a protection circuit.

DISCUSSION OF THE RELATED ART

[0003] As electronic devices such as portable electronic devices become smaller, semiconductor elements disposed therein have also become smaller and lighter. As semiconductor elements become smaller, three-dimensional (3D) integrated circuits (ICs) in which multiple chips are stacked upon each other over a base substrate are being manufactured so as to integrate more circuits within a limited space.

[0004] In the manufacture of integrated circuits, a process including charged ions, such as a plasma etching process, may be used. For example, during the manufacture of an integrated circuit, a lowest metal layer closest to the substrate may be connected to the gate poly of a metal-oxide semiconductor (MOS) transistor. In the plasma etching process step of forming or interconnecting metal layers, etc., the lowest metal layer absorbs charge from the plasma, forming a sufficiently high voltage, relative to the substrate, that can destroy the thin gate dielectric that separates the gate poly from the substrate. This is called plasma induced gate oxide damage or the antenna effect. This may cause yield and reliability issues for integrated circuits.

SUMMARY

[0005] A 3D integrated circuit includes a first integrated circuit including a first substrate. A second integrated circuit is stacked on the first integrated circuit. A through via extends through the first substrate and electrically connects the first integrated circuit and the second integrated circuit to one another. A plurality of protection circuits is disposed at opposite sides of the through via in a keep-out zone surrounding the through via and is electrically connected to the through via.

[0006] An integrated circuit includes a through via extending through the first substrate. A first keep-out zone is disposed on the first substrate, and has a first boundary around the through via and spaced apart from the through via by a first distance in a first direction, and a second boundary spaced apart from the through via by a second distance in a second direction perpendicular to the first direction. A second keep-out zone is disposed on the first substrate, and has a third boundary around the through via and spaced apart from the through via by a third distance in the first direction, and a fourth boundary spaced apart from the through via by the second distance in the second direction. A first protection circuit is disposed outside of the first keep-out zone and inside of the second keep-out zone and is electrically connected to the through via. An integrated circuit is disposed outside of the second keep-out zone and includes an interface circuit electrically connected to the through via.

[0007] A 3D integrated circuit includes a first substrate. A through via extends through the first substrate. A first keep-out zone is disposed on the first substrate and includes an area around the through via at a first distance from the through via. A second keep-out zone is disposed on the first substrate and includes an area extended by a second distance from the first keep-out zone in a first direction and in a direction opposite to the first direction. A protection circuit is disposed outside of the first keep-out zone and inside of the second keep-out zone and is electrically connected to the through via. An interface circuit is adjacent to the first keep-out zone in a second direction perpendicular to the first direction and is electrically connected to the through via.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] A more complete appreciation of the present disclosure and many of the attendant aspects thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:

[0009] FIG. **1** is a perspective view illustrating a three-dimensional (3D) integrated circuit including a through via according to an embodiment.

[0010] FIG. **2** is a schematic diagram illustrating a TSV cell and a protection circuit according to a comparative embodiment.

[0011] FIG. **3** is a schematic diagram illustrating a TSV cell according to an embodiment.

[0012] FIG. **4** is a schematic diagram illustrating a TSV cell according to an embodiment.

[0013] FIG. **5** is a cross-sectional view taken along a line A-A' of FIG. **4**.

[0014] FIG. **6** is a schematic diagram illustrating a TSV cell according to an embodiment.

[0015] FIG. **7** is a perspective view showing a cross-section taken along a line B-B' of FIG. **6**.

[0016] FIG. **8** is a schematic diagram illustrating an effect of reducing an area occupied by a protection circuit according to an embodiment.

[0017] FIG. **9** is a schematic diagram illustrating a layout of an integrated circuit.

[0018] FIG. **10** is a schematic diagram illustrating a TSV area according to a comparative embodiment.

[0019] FIG. **11** is a schematic diagram illustrating a TSV area according to an embodiment.

[0020] FIG. **12** is a schematic diagram illustrating a signal transmission path of a logical signal according to an embodiment.

[0021] FIG. **13** is a perspective view illustrating a semiconductor device according to an embodiment.

DETAILED DESCRIPTION OF THE DRAWINGS

[0022] In the following detailed description, certain embodiments of the present disclosure have been shown and described, simply by way of illustration. As those skilled in the art would realize, the described embodiments may be modified in various different ways, all without departing from the spirit or scope of the present disclosure.

[0023] While each drawing may represent one or more particular embodiments of the present disclosure, drawn to scale, such that the relative lengths, thicknesses, and angles can be inferred therefrom, it is to be understood that the present invention is not necessarily limited to the relative lengths, thicknesses, and angles shown. Changes to these values may be made within the spirit and scope of the present disclosure, for example, to allow for manufacturing limitations and the like. In addition, in the following description, the formation of the first structure on or above the second structure may include embodiments in which the first and second structures are formed in direct contact, and embodiments may also include where additional structures may be formed between the first and second structures such that the first and second structures are not in direct contact.

[0024] In addition, spatially related terms, such as "below", "lower", "lower portion", "above", "upper portion", etc., may be used for ease of description to depict the relationship of any one element or structure illustrated in the drawing to another element or structure.

[0025] Like reference numerals may designate like elements throughout the specification and the drawings.

[0026] In addition, expressions written in the singular may be construed in the singular or plural unless an explicit expression such as "one" or "single" is used. Terms including ordinal numbers such as first, second, and the like will be used to describe various component and are not necessarily to be interpreted as limiting these components. These terms may be used for the purpose of distinguishing one constituent element from other constituent elements.

[0027] FIG. **1** illustrates a three-dimensional (3D) integrated circuit including a through via according to an embodiment. In an embodiment, a through via may be a through silicon via (TSV), but the present disclosure is not necessarily limited thereto.

[0028] Referring to FIG. **1**, a three-dimensional integrated circuit (3D IC) **100** may include integrated circuits **110**, **130**, and **150** and a printed circuit board (PCB) **170**. Each of the integrated circuits **110**, **130**, and **150** of the 3D integrated circuit **100** may be connected by through vias **120**. Each of the integrated circuits **110**, **130**, and **150** may transmit and receive logic signals or power voltages through the through vias **120**.

[0029] In an embodiment, at least one through via **120** may form a unit through via structure **123**. The unit through via structure **123** may include a plurality of through vias **121**. The through vias **121** may be arranged regularly (e.g., at regular intervals). For example, each of the integrated circuits **110**, **130**, and **150** may transmit and receive logic signals or power voltages through the unit through via structure **123**. Hereinafter, the through via **121** may refer to any through via **121** among the through vias included in the unit through via structure **123**.

[0030] Bumps (e.g., micro bumps or solder bumps) or hybrid copper bonding (HCB) may be disposed between the integrated circuits **110**, **130**, and **150**. The integrated circuits **110**, **130**, and **150** may be electrically connected through bumps or hybrid copper bonding disposed between the integrated circuits **110**, **130**, and **150**. The integrated circuits **110**, **130**, and **150** may transmit and receive logic signals or power voltages through bumps or hybrid copper bonding disposed between the integrated circuits **110**, **130**, and **150**.

[0031] The first integrated circuit **150** may include an area (i.e., keep-out zone (KoZ)) **160** where circuits are selectively disposed to prevent defects caused by formation of the through via **121**. For example, a circuit or metal layer might not be disposed in the keep-out zone **160** by setting the keep-out zone **160** to be spaced apart from the through via **121** by a predetermined distance, in order to prevent carrier mobility of active silicon existing near the through via **121** from being reduced. The keep-out zone **160** may include a keep-out zone in a front-end-of-line (FEOL) process and a keep-out zone in a back-end-of-line (BEOL) process. A detailed description thereof will be provided later with reference to FIG. **2**. Hereinafter, the keep-out zone **160** including the through via **121** may be referred to as a TSV cell.

[0032] In an embodiment, the TSV cell may include a protection circuit **161**. The protection circuit **161** may be disposed in the keep-out zone **160**. The protection circuit **161** may protect the integrated circuit from an electrical effect occurring during a manufacturing process of the integrated circuit. For example, the protection circuit **161** may protect the first integrated circuit **150** by preventing an antenna effect or electrostatic discharge (ESD). Hereinafter, the protection circuit **161** is illustrated and described as including a plurality of diodes, but a configuration of the protection circuit **161** is not necessarily limited thereto.

[0033] The integrated circuit includes a transistor, and a gate electrode of the transistor may include a first layer and a second layer. Herein, the first layer may include a metal, and the second layer may include a polysilicon layer. In the following, the second layer is described as the polysilicon layer of the gate electrode of the transistor.

[0034] In the 3D integrated circuit **100**, an antenna effect may occur due to damage to a gate poly due to charge generated during an etching operation of the through via **121**. For example, the gate poly of the MOS transistor on the first integrated circuit **150** may be connected to the through via **121** through a metal layer. In a manufacturing process of an integrated circuit, charge due to a plasma etching process accumulate in a floating gate poly on the first integrated circuit **150**, which may destroy a gate dielectric material. To prevent this problem, the 3D integrated circuit **100** may include the protection circuit **161** disposed in the TSV cell.

[0035] In an embodiment, the protection circuit **161** may include a first diode D**1** connected between a node N and a line of a first power VDD**1** and a second diode D**2** connected between a node N and a line of a ground power VSS. The first diode D**1** and the second diode D**2** may be connected in a reverse direction. An anode of the first diode D**1** may be connected to the node N, and a cathode of the first diode D**1** may be connected to the first power VDD**1** having a higher voltage level than that of the node N. A cathode of the second diode D**2** may be connected to the node N, and may be connected to the ground power VSS having a lower voltage level than that of the node N of the second diode D**2**. When a voltage of a signal level within a normal operating range is applied to the node N, each diode (D**1** and D**2**) is reverse biased and therefore does not conduct. However, when a high voltage is applied to the node N, the diodes D**1** and D**2** are conducted due to strong reverse bias, and a charge due to static electricity may be discharged directly to the line of the first power VDD**1** or the line of the ground power VSS. For example, the protection circuit **161** may create another electrical path for discharging charge. However, a structure of the protection circuit **161** is illustrative, and the present disclosure is not necessarily limited thereto.

[0036] According to an embodiment, an area occupied by the protection circuit **161** in the first integrated circuit **150** may be reduced by providing the protection circuit **161** in the keep-out zone **161**, and thus an area of the first integrated circuit **150** may be efficiently utilized.

[0037] FIG. **2** illustrates a view for describing a TSV cell and a protection circuit according to a comparative embodiment.

[0038] Referring to FIG. **2**, the TSV cell **20** may include a through via **24**. At least one through via **24** may be disposed. The at least one through via **24** may form a unit through via structure **22**. The unit through via structure **22** may include a plurality of through vias **24** regularly arranged. A boundary **21** of a first keep-out zone KoZ 1 and a boundary **23** of a second keep-out zone (KoZ 2) are determined by a distance from an edge of an outermost through via of the unit through-via structure **22**. For example, a boundary of the first keep-out zone KoZ 1 in the first direction (e.g., X direction) may be spaced apart from the outermost through via by a first distance d1 in the first direction, and a boundary of the first keep-out zone KoZ 1 in the second direction (e.g., Y direction) may be spaced apart from the outermost through via by a second distance d2 in the second direction. The first direction and the second direction may be perpendicular, and the first distance d1 and the second distance d2 may be the same or different from each other. A boundary of the second keep-out zone KoZ 2 in the first direction (e.g., X direction) may be spaced apart from the outermost through via by a third distance d3 in the first direction, and a boundary of the second keep-out zone KoZ 2 in the second direction (e.g., Y direction) may be spaced apart from the outermost through via by the second distance d2 in the second direction. The first distance d1 and the third distance d3 may be different from each other, and the third distance d3 may be greater than the first distance d1. A boundary **23** of the second keep-out zone KoZ 2 is expanded from a boundary **21** of the first keep-out zone KoZ 1 in the first direction (e.g., X direction) and in a direction opposite to the first direction. The second keep-out zone KoZ 2 may be an area extended from the first keep-out zone KoZ 1 in the first direction. The first keep-out zone KoZ 1 may be a smaller area than the second keep-out zone KoZ 2. For example, the second keep-out zone KoZ 2 may occupy a larger area than the first keep-out zone KoZ 1.

[0039] The second keep-out zone KoZ 2 may be an area in which active semiconductor devices (i.e., transistors used to transmit/process signals) formed during the FEOL process are not disposed. The FEOL process may form various layers and patterns necessary for the functioning of active semiconductor devices. The second keep-out zone KoZ 2 may be an area where active semiconductor devices are not disposed in order to prevent interference between the through via **24** and the active semiconductor devices.

[0040] The first keep-out zone KoZ 1 may be an area in which metal layers, vias, etc. formed during the BEOL process are not disposed. The BEOL process may form metal layers to connect active semiconductor devices and other components. The first keep-out zone KoZ 1 may be an area in which metal layers other than predefined metal layers (e.g., metal layers connected to through-silicon vias) are not disposed to prevent interference between the through via **24** and the metal layers.

[0041] The through via **24** of the TSV cell **20** may transmit a logic signal received from an adjacent interface circuit **27** to another integrated circuit, or may transmit logic signals received from other integrated circuits to the interface circuit **27**. The through via **24** and the interface circuit **27** may be connected through a plurality of metal layers **26**. Herein, the interface circuit **27** may include various logic elements. For example, the interface circuit **27** may be various logic elements such as AND gates, OR gates, NOR gates, XOR gates, inverters, etc., or memory elements such as latches and flip-flops.

[0042] A protection circuit **25** may be disposed on a path between the through via **24** and the interface circuit **27**. For example, the protection circuit **25** may be connected to the metal layer **26** connecting the through via **24** and the interface circuit **27**. The protection circuit **25**, according to a comparative embodiment, may be disposed outside of the TSV cell **20**. The protection circuit **25**, according to the comparative embodiment, may be disposed adjacent to the TSV cell **20** outside of the TSV cell **20**. The protection circuit **25**, according to the comparative embodiment, may be disposed between the interface circuit **27** and the TSV cell **20** outside of the TSV cell **20**.

[0043] According to the comparative example, the protection circuit **25** disposed outside of the TSV cell **20** occupies a large area within the integrated circuit. For example, there is a problem that the area of the integrated circuit might not be efficiently utilized due to the protection circuit **25** disposed outside of the TSV cell **20**.

[0044] FIG. **3** illustrates a view for describing a TSV cell according to an embodiment. For example, it illustrates a schematic layout diagram to describe a TSV cell including a protection circuit.

[0045] In an embodiment, the TSV cell **30** may include a protection circuit **35**. For example, the protection circuit **35** may be disposed in the second keep-out zone KoZ 2 of the TSV cell **30**. The protection circuit **35** includes a passive semiconductor device (i.e. a transistor not used to transmit/process signals), and thus it is disposed in the second keep-out zone KoZ 2 (i.e. inside a boundary **31** of the TSV cell).

[0046] If the protection circuit **35** is disposed too close to the through via **34**, unexpected damage may occur in the protection circuit **35** during the manufacturing process, so the protection circuit **35** may be disposed outside of the first keep-out zone KoZ 1. The protection circuit **35** may be an antenna protection circuit (e.g., antenna diode, etc.) to prevent antenna effects, or an ESD protection circuit (e.g., an ESD diode, a clamp, etc.) to prevent ESD, but the present disclosure is not necessarily limited thereto.

[0047] In an embodiment, the TSV cell **30** and an interface circuit **33** may be disposed adjacent to each other in the first direction (e.g., X direction). The through via **34** of the TSV cell **30** may transmit a logic signal received from an adjacent interface circuit **33** to another integrated circuit, or may transmit logic signals received from other integrated circuits to the interface circuit **33**. The through via **34** and the interface circuit **33** may be connected through a plurality of metal layers **36**.

[0048] In an embodiment, the protection circuit **35** within the TSV cell **30** may be disposed on a path between the interface circuit **33** and the through via **34**. For example, the protection circuit **35** may be connected to a plurality of metal layers **36** connecting the interface circuit **33** and the through via **34**. The protection circuit **35**, which is an electrical path for discharging charge flowing toward the interface circuit

33, may protect the transistors in the interface circuit 33 from various electrical effects.

[0049] According to an embodiment, an area of the integrated circuit may be efficiently utilized by positioning the protection circuit 25 within the TSV cell 20. For example, a size of the integrated circuit may be reduced or a sufficient area where logic elements may be disposed on the integrated circuit may be secured.

[0050] FIG. 4 illustrates a view for describing a TSV cell according to an embodiment. For example, it illustrates a schematic layout diagram to describe a TSV cell including a plurality of protection circuits.

[0051] In an embodiment, the TSV cell 40 may include protection circuits 45 and 47. The second keep-out zone KoZ 2 of the TSV cell 40 may include a first area 44 extending from the first keep-out zone KoZ 1 in the first direction (e.g., X direction), and a second area 42 extending in a direction opposite to the first direction. The TSV cell 40 may include a protection circuit 47 disposed in the first area 44 and a protection circuit 45 disposed in the second area 42. The protection circuits 45 and 47 may be disposed in the second keep-out zone KoZ 2 at opposite sides of a through via 48. The protection circuits 45 and 47 may be disposed outside of the first keep-out zone KoZ 1 at opposite sides of the through via 48. Structures of the protection circuits 45 and 47 may be the same or different from each other.

[0052] In an embodiment, the protection circuits 45 and 47 may be disposed on a path between an interface circuit 43 and the through via 48. For example, the protection circuits 45 and 47 may be connected to the metal layer 46 connecting the interface circuit 43 and the through via 48. The protection circuits 45 and 47, which are an electrical paths for discharging charge flowing toward the interface circuit 43, may protect the transistors in the interface circuit 43 from various electrical effects. According to an embodiment, the TSV cell 40 may include a plurality of protection circuits, further increasing the protection effect for transistors around the TSV cell through the protection circuits without increasing an area occupied by the protection circuits in the integrated circuit.

[0053] FIG. 5 illustrates a cross-sectional view taken along a line A-A' of FIG. 4.

[0054] For example, FIG. 5 illustrates a cross-sectional view of one integrated circuit 500 among a plurality of integrated circuits constituting a 3D integrated circuit. Referring to FIG. 5, according to an embodiment, the 3D integrated circuit may further include additional integrated circuits above and/or below the integrated circuit 500. For example, the integrated circuit 500 may correspond to the first integrated circuit 150 according to FIG. 1. Additionally, although a portion of integrated circuit 500 is shown here, the integrated circuit 500 may include additional components.

[0055] In an embodiment, the integrated circuit 500 may include a BEOL layer 510*a* and a substrate layer 510*c*. The substrate layer 510*c* may be or may include a semiconductor substrate material such as silicon. An interface circuit 520 that transmits and receives logic signals to and from other adjacent dies may be disposed on and/or within the substrate layer 510*c*. The interface circuit 520 may be active elements such as MOS transistors. The substrate layer 510*c* may include a through via 531 extending through the substrate layer 510*c*. The through via 531 may extend from a front surface 510*f* to a back surface 510*b* of the substrate layer 510*c*.

[0056] In an embodiment, a boundary of the first keep-out zone KoZ 1 in the first direction (e.g., X direction) around the through via 531 is determined by a first distance 533 from the through via 531 on the substrate layer 510*c*. A boundary of the second keep-out zone KoZ 2 in the first direction (e.g., X direction) around the through via 531 may be determined by a second distance 535 from the through via 531. Referring to FIG. 2, as described above, the first keep-out zone KoZ 1 may be an area where metal layers, vias, etc. formed during the BEOL process are not disposed, and the second keep-out zone KoZ 2 may be an area where an active semiconductor device formed during the FEOL process is not disposed. In FIG. 5, the first keep-out zone KoZ 1 and the second keep-out zone KoZ 2 are shown extending through the substrate layer 510*c*, but this is for convenience of understanding, and in fact, the first keep-out zone KoZ 1 and the second keep-out zone KoZ 2 are areas around the through via 531 on the substrate layer 510*b*, and might not extend through the substrate layer 510*c*.

[0057] In an embodiment, the substrate layer 510*c* may include protection circuits 537 disposed on and/or within the substrate layer 510*c*. The protection circuits 537 may be disposed in the second keep-out zone KoZ 2 and outside of the first keep-out zone KoZ 1. The protection circuits 537 may be disposed outside of the first keep-out zone KoZ 1 and inside of the second keep-out zone KoZ 2 at opposite sides of the through via 531.

[0058] In an embodiment, the interface circuit 520 may be disposed adjacent to the first protection circuit 537_1 among the protection circuits 537 in the first direction (e.g., X direction). The first protection circuit 537_1 may be disposed between the interface circuit 520 and the through via 531 in the first direction (e.g., X direction). In an embodiment, the interface circuit 520, a protection circuit 537_1, and the through via 531 may be sequentially disposed in the first direction X. Additionally, a protection circuit 537_2 may be further disposed at an opposite side of the protection circuit 537_1 centered on the through via 531.

[0059] In an embodiment, the BEOL layer 510*a* may include a plurality of metal layers 540. The metal layers 540 may include a plurality of metal lines and a plurality of metal vias connecting them. The interface circuit 520 may be electrically connected to the through via 531 through the metal layers 540. For example, the interface circuit 520 may transmit logic signals to the through via 531 or receive logic signals from the through via 531 through the metal layers 540. The interface circuit 520 may transmit and receive logic signals to and from the through via 531 through a first path 560.

[0060] In an embodiment, the protection circuits 537 may be electrically connected to the through via 531 through the metal layers 540. The protection circuits 537 may be electrically connected to the interface circuit 520 through the metal layers 540. For example, charge generated during an etching process to form the through via 531 may flow to the protection circuits 537 through a second path 570. Charge generated during the etching process to form the through via 531 may be discharged through the protection circuits 537 disposed in the second keep-out zone KoZ 2. In an embodiment, the protection circuit 537 may be connected to the metal layers 540 connecting the interface circuit 520 and the

through via **531**. The protection circuit **537**, which is an electrical path for discharging charge flowing through the interface circuit **520**, may protect the transistors in the interface circuit **520** from various electrical effects.

[0061] In an embodiment, a redistribution layer (RDL) **551** may be disposed on the back surface **510***b* of the substrate layer **510***c* to form an electrical connection with adjacent dies. The through via **531** may provide an electrical connection between the metal layers **540** and the redistribution layer **551** through conductive materials within the through via **531**. The redistribution layer **551** may include a plurality of metallization patterns between adjacent dies. The redistribution layer **551** may form an electrical connection with the metal layers **540** through the conductive materials in the through via **531**.

[0062] In an embodiment, the redistribution layer **551** may be connected to an interconnection structure **553**. Herein, the interconnection structure **553** may include a bump (e.g., a micro bump or a solder bump) or hybrid copper bonding. The interconnection structure **553** may be formed of a conductive material such as copper, aluminum, etc. The interface circuit **520** may transmit and receive logic signals to and from the outside through the interconnection structure **553**, the redistribution layer **551**, the through via **531**, the metal layers **540**, etc. However, some of these elements may be omitted or other necessary elements may be added as needed.

[0063] FIG. **6** illustrates a view for describing a TSV cell according to an embodiment. For example, it illustrates a schematic layout diagram to describe a TSV cell including a plurality of protection circuits.

[0064] In an embodiment, the TSV cell **60** may include protection circuits **65** and **67** disposed in the second keep-out zone KoZ 2 extended in the first direction X. The second keep-out zone KoZ 2 may include a first area **64** extending from the first keep-out zone KoZ 1 in the first direction (e.g., X direction) and a second area **62** extending in a direction opposite to the first direction, and each area may include protection circuits **65** and **67**. The protection circuits **65** and **67** may be disposed in the second keep-out zone KoZ 2 at opposite sides of a through via **68**. The protection circuits **65** and **67** may be disposed outside of the first keep-out zone KoZ 1 at opposite sides of the through via **68**. Structures of the protection circuits **65** and **67** may be the same or different from each other. However, the present disclosure is not necessarily limited thereto, and one of the first area **64** and the second area **62** may include a protection circuit. The through via **68** and the protection circuits **65** and **67** may be connected through a plurality of metal layers **66_1**.

[0065] In an embodiment, the TSV cell **60** and an interface circuit **63** may be disposed adjacent to each other in a second direction (e.g., Y) perpendicular to the first direction (e.g., X direction). The interface circuit **63** may be disposed adjacent to the first keep-out zone KoZ 1 in the second direction (e.g., Y). No element might be disposed between the interface circuit **63** and the first keep-out zone KoZ 1 in the second direction (e.g., Y). The through via **68** of the TSV cell **60** may transmit a logic signal received from an adjacent interface circuit **63** to another integrated circuit, or may transmit logic signals received from other integrated circuits to the interface circuit **63**. The through via **68** and the interface circuit **33** may be connected through a plurality of metal layers **66 2**.

[0066] FIG. **7** illustrates a perspective view showing a cross-section taken along a line B-B' of FIG. **6**.

[0067] For example, FIG. **7** illustrates a cross-sectional view of one integrated circuit **700** among a plurality of integrated circuits constituting a 3D integrated circuit. Referring to FIG. **7**, according to an embodiment, the 3D integrated circuit may further include additional integrated circuits above and/or below the integrated circuit **700**. For example, the integrated circuit **700** according to FIG. **7** may correspond to the first integrated circuit **150** according to FIG. **1**. Additionally, although a portion of integrated circuit **700** is shown here, the integrated circuit **700** may include additional components. To the extent that an element is not described in detail with respect to this figure, it may be understood that the element is at least similar to a corresponding element that has been described elsewhere within the present disclosure.

[0068] In an embodiment, the integrated circuit **700** may include an interface circuit **720** disposed on and/or within the substrate layer **510***c*. The substrate layer **710***c* may include a through via **731** extending through the substrate layer **710***c*. On the substrate layer **710***c*, the first keep-out zone KoZ 1 around the through via **731** may be determined by a first distance **733** from the through via **731** in the first direction (e.g., X) and a second distance **734** in the second direction (e.g., Y) perpendicular to the first direction (e.g., X). On the substrate layer **710***c*, the second keep-out zone KoZ 2 around the through via **731** may be determined by a third distance **735** from the through via **731** in the first direction (e.g., X) and the second distance **734** in the second direction (e.g., Y) perpendicular to the first direction (e.g., X). The first distance **733** and the second distance **734** may be different from or the same as each other, and the third distance **735** may be greater than the first distance **733**. Accordingly, the second keep-out zone KoZ 2 may occupy a larger area than the first keep-out zone KoZ 1.

[0069] In an embodiment, the integrated circuit **700** may include a protection circuit **737** disposed on and/or within the substrate layer **510***c*. The protection circuit **737** may be disposed in the second keep-out zone KoZ 2 and outside of the first keep-out zone KoZ 1.

[0070] In an embodiment, the interface circuit **720** may be disposed adjacent to the through via **731** in the second direction (e.g., Y) perpendicular to the first direction (e.g., X direction). The interface circuit **720** may be disposed adjacent to the first keep-out zone KoZ 1 in the second direction (e.g., Y) perpendicular to the first direction (e.g., X direction). No element might be disposed between the interface circuit **720** and the first keep-out zone KoZ 1 in the second direction (e.g., Y). The interface circuit **720** and the protection circuit **737** may be disposed in directions perpendicular to each other based on the through via **731**, and may be disposed adjacent to the through via **731** in directions perpendicular to each other.

[0071] In an embodiment, the interface circuit **720** may transmit logic signals to or receive logic signals from the through via **731** through the metal layers **740** in the BEOL layer **710***a*. The interface circuit **720** may transmit and receive logic signals to and from the through via **731** by using a first path **760**.

[0072] In an embodiment, the protection circuit **737** may be electrically connected to the through via **731** and the interface circuit **720** through the metal layers **740**. For

example, charge generated during an etching process to form the through via **731** may flow to the protection circuit **737** through a second path **770**.

[0073] According to an embodiment, the semiconductor device **700** may minimize a distance between the interface circuit **720** and the through via **731**. Accordingly, a length of the metal layer **740** connecting the interface circuit **720** and the through via **731** may be reduced, which may increase signal integrity (SI) and provide other desirable characteristics.

[0074] FIG. **8** illustrates a view for describing an effect of reducing an area occupied by a protection circuit according to an embodiment.

[0075] FIG. **8**, element (a), illustrates a TSV cell **810**, a protection circuit **811**, and an interface circuit **813** according to a comparative example. According to the comparative example of FIG. **8**, element (a), the protection circuit **811** is disposed outside of the TSV cell **810** and adjacent to the TSV cell **810**, and the protection circuit **811** and the interface circuit **813** are disposed adjacent to each other in a same direction (e.g., first direction) as a direction in which the protection circuit **811** is adjacent to the TSV cell **810**.

[0076] FIG. **8**, element (b), illustrates a TSV cell **820**, a protection circuit **821**, and an interface circuit **823** according to an example. According to an example of FIG. **8**, element (b), the protection circuit **821** is disposed in a FEOL keep-out zone **822** inside of the TSV cell **820**, and the protection circuit **821** and the interface circuit **823** may be disposed adjacent to each other in a same direction as a direction in which the protection circuit **821** is disposed adjacent to the through via **825** (e.g., the first direction). Herein, the TSV cell **820** is illustrated as including a plurality of protection circuits **821**, but the present disclosure is not necessarily limited thereto.

[0077] FIG. **8**, element (c), illustrates a TSV cell **830**, a protection circuit **821**, and an interface circuit **823** according to an example. According to an example of FIG. **8**, element (c), the protection circuit **831** may be disposed in a FEOL keep-out zone **832** inside of the TSV cell **830**, and the TSV cell **820** and the interface circuit **823** may be disposed adjacent to each other in a direction perpendicular to a direction (first direction) in which the protection circuit **821** is disposed adjacent to the through via **835** (e.g., the second direction).

[0078] FIG. **8**, element (d), is a table shown to compare areas occupied by the TSV cell, the protection circuit, and the interface circuit according to the comparative example FIG. **8**, element (a), and the examples FIG. **8**, element (b), and FIG. **8**, element (c), of the present disclosure. According to the table in FIG. **8**, element (d), a length X**1** of the TSV cell **810**, the protection circuit **811**, and the interface circuit **813** in the first direction according to the comparative example of FIG. **8**, element (a), is 23 μm, and a length Y**1** in the second direction is 10 μm, and thus an area occupied by the TSV cell **810**, the protection circuit **811**, and the interface circuit **813** according to the comparative example of FIG. **8**, element (a), is 230 μm^2. On the other hand, a length X**2** of the TSV cell **820**, the protection circuit **821**, and the interface circuit **823** in the first direction according to the example of FIG. **8**, element (b), is 18.5 μm, and a length Y**2** in the second direction is 10 μm, and thus an area occupied by the TSV cell **820**, the protection circuit **821**, and the interface circuit **823** according to the example of FIG. **8**, element (b), is 185 μm^2, and a length X**3** of the TSV cell **830**, the protection circuit **831**, and the interface circuit **833** in the first direction according to the example of FIG. **8**, element (c), is 14 μm, and a length Y**3** in the second direction is 14 μm, and thus an area occupied by the TSV cell **830**, the protection circuit **831**, and the interface circuit **833** according to the example FIG. **8**, element (c), is 196 μm^2.

[0079] For example, compared to the area according to the comparative example FIG. **8**, element (a), the area occupied by the TSV cell, the protection circuit, and the interface circuit according to the examples FIG. **8**, element (b), and FIG. **8**, element (c), may be reduced by 19.57% and 14.78%, respectively. There is an advantage in that the area of the integrated circuit may be efficiently utilized by reducing the size of the semiconductor device or arranging other logic elements according to the reduced area.

[0080] FIG. **9** schematically illustrates a layout of an integrated circuit. In an embodiment, the integrated circuit **900** may include a plurality of metal lines ML extending in a row direction (e.g., X direction). The metal lines ML may intersect to provide a power voltage (e.g., VDD) and a ground voltage VSS.

[0081] In an embodiment, the integrated circuit **900** may include a plurality of standard cells. Herein, the standard cells may include logic elements, memory elements, filler cells, etc. The standard cells may be arranged to overlap the metal lines ML. Herein, the standard cells arranged in each row R are shown, but the present disclosure is not necessarily limited thereto, and the standard cells may be formed over a plurality of rows R.

[0082] In an embodiment, the integrated circuit **900** may further include a TSV area. The TSV area may include a TSV cell including a through-via, a protection circuit, and an interface circuit for transmitting and receiving a logic signal to and from the through-via. TSV areas may be regularly arranged on the integrated circuit **900**. For example, the TSV areas may be spaced apart from each other by a predetermined distance in the first direction (e.g., X) and the second direction (e.g., Y). Alternatively, the TSV areas may be irregularly arranged on the integrated circuit **900**.

[0083] The TSV cell, the protection circuit, and the interface circuit may be implemented as one TSV module. In an embodiment, the TSV area may include TSV modules arranged in an m×n (m by n) format (where "m" and "n" are integers equal to or greater than 1). For example, the TSV area may include one TSV module or may include multiple TSV modules. In an embodiment, some of the TSV areas may include one TSV module, and remaining TSV areas may include a plurality of TSV modules arranged in an m×n (m by n) format.

[0084] The TSV area may further include standard cells. The TSV area may include standard cells disposed in a remaining area after positioning the TSV module. A detailed description of the TSV area will be provided with reference to FIGS. **10** and **11**.

[0085] FIG. **10** illustrates a TSV area according to a comparative embodiment. For example, the TSV area, according to the comparative embodiment of FIG. **10**, is shown as including a plurality of TSV modules arranged in a 3×3 (3 by 3) shape, but the present disclosure is not necessarily limited thereto.

[0086] The TSV area **1000**, according to the comparative embodiment, may include a plurality of TSV modules **1010**, **1020**, and **1030**. The first TSV module **1010**, according to the comparative embodiment, may include a TSV cell **1012**,

a protection circuit **1013**, and an interface circuit **1011**. The protection circuit **1013** in the first TSV module **1010**, according to the comparative embodiment, may be disposed outside of the TSV cell **1012**.

[0087] According to the comparative example, the first TSV module **1010** and the second TSV module **1020** may be spaced apart from each other by a predetermined first distance DX in the first direction (e.g., X direction). The first TSV module **1010** and the third TSV module **1030** may be spaced apart by a predetermined second distance DY in a second direction (e.g., Y direction) perpendicular to the first direction.

[0088] According to the comparative embodiment, an interface circuit **1021** that transmits and receives logic signals to and from a through via in the second TSV module **1020** may be disposed adjacent to the first TSV module **1010**. For example, the interface circuit **1021** and the first TSV module **1010** may be attached and disposed in the first direction (e.g., X direction). Accordingly, no standard cell may be disposed between the interface circuit **1021** and the first TSV module **1010**.

[0089] According to the comparative example, the first TSV module **1010** and the third TSV module **1030** may be arranged adjacent to each other in the second direction (e.g., Y direction). The first TSV module **1010** and the third TSV module **1030** may be spaced apart from one another by a third distance RY in the second direction (e.g., Y direction). A plurality of standard cells may be disposed between the first TSV module **1010** and the third TSV module **1030**. Additionally, a plurality of metal layers may be disposed between the first TSV module **1010** and the third TSV module **1030**.

[0090] According to the comparative embodiment, an area where standard cells can be disposed in the TSV area **1000** is merely an area of the third distance RY between the first TSV module **1010** and the third TSV module **1030**. For example, many standard cells are disposed in a limited space, which may cause various problems such as routing congestion.

[0091] FIG. **11** illustrates a TSV area according to an embodiment. For example, the TSV area, according to an embodiment of FIG. **11**, is shown as including a plurality of TSV cells a protection circuit, and an interface circuit arranged in a 3×3 (3 by 3) shape, but the present disclosure is not necessarily limited thereto. In addition, each of the TSV cell, the protection circuit, and the interface circuit may be implemented as one TSV module.

[0092] The TSV area **1100**, according to an embodiment, may include a plurality of TSV modules **1110**, **1120**, and **1130**. The first TSV module **1110**, according to an embodiment, may include a TSV cell **1114**, a protection circuit **1113**, and an interface circuit **1111**. The protection circuit **1113** in the first TSV module **1110**, according to an embodiment, may be disposed inside of the TSV cell **1114**. According to an embodiment, the protection circuit **1113** within the second TSV module **1110** may be disposed in the second keep-out zone KoZ 2 within the TSV cell **1114**. A structure of the protection circuit **1113** is not necessarily limited thereto.

[0093] According to an embodiment, the first TSV module **1110** and the second TSV module **1120** may be spaced apart from each other by a predetermined first distance DX in the first direction (e.g., X direction). The first TSV module **1110** and the third TSV module **1130** may be spaced apart by a predetermined second distance DY in a second direction (e.g., Y direction) perpendicular to the first direction. In an embodiment, the first TSV module **1110** and the second TSV module **1020** are spaced apart by the first distance DX in the first direction (e.g., X direction), so that there may be a space equal to a third distance RX' in the first direction (e.g., X direction) between the first TSV module **1110** and the second TSV module **1020**. In addition, the first TSV module **1110** and the third TSV module **1030** are spaced apart by the second distance DY in the second direction (e.g., Y direction), so that there may be a space equal to a fourth distance RY' in the second direction (e.g., Y direction) between the first TSV module **1110** and the third TSV module **1030**.

[0094] In an embodiment, a plurality of standard cells may be located in an area of the third distance RX' and an area of the fourth distance RY'. For example, with the protection circuit disposed within the TSV cell, there is an advantage in that an area where standard cells can be disposed within the TSV area **1100** may increase, the area may be utilized efficiently, and problems such as routing congestion may be solved. Additionally, the TSV area **1100** according to an embodiment may reduce the first distance DX and the second distance DY as needed. For example, there is an advantage in that the area occupied by the TSV area **1100** in the integrated circuit may be reduced by arranging the TSV modules **1110**, **1120**, and **1130** closer to each other.

[0095] FIG. **12** illustrates a view for describing a signal transmission path of a logical signal according to an embodiment. For example, it represents a signal transmission path of a logic signal transmitted from a first integrated circuit to a second integrated circuit through a through-via.

[0096] In an embodiment, the 3D integrated circuit **1200** may include a first integrated circuit **1210** and a second integrated circuit **1220**. The first integrated circuit **1210** may include a logic circuit **1212**, an interface circuit **1213**, and a TSV cell **1215**. In an embodiment, the interface circuit **1213** and the TSV cell **1215** may be implemented as a TSV module. In an embodiment, the TSV cell **1215** may include a through-via **1216**, and may include a protection circuit **1214** in a region spaced apart from the through-via **1216** by a predetermined distance. In an embodiment, the second integrated circuit **1210** may include an interface circuit **1222** and a logic circuit **1223**. The second integrated circuit **1220** may further include a protection circuit **1221**. However, as needed, some components within each die may be omitted, or other necessary components may be added.

[0097] In an embodiment, the first integrated circuit **1210** may receive a logic signal from the outside through an input port **1211**. The logic signal may be transmitted to the through-substrate via **1215** through the logic circuit **1212** and the interface circuit **1213** in the first integrated circuit **1210**. The logic signal may be transmitted to the second integrated circuit **1220** through an interconnection structure **1230**. The logic signal may be transmitted to the outside through the interface circuit **1222** and the logic circuit **1223** in the second integrated circuit **1220** and through an output port **1224**.

[0098] FIG. **13** illustrates a semiconductor device according to an embodiment.

[0099] Referring to FIG. **13**, the semiconductor device **1300** may be a memory module including at least one stack semiconductor chip **1330** and a system-on-chip (SOC) **1350** mounted on a package substrate **1310** such as a printed circuit board.

[0100] An interposer **1320** may be optionally further provided on the package substrate **1310**. The stack semiconductor chip **1330** may be formed as a chip-on-chip (CoC). The stack semiconductor chip **1330** may include at least one memory chip **1340** stacked on a buffer chip **1360** such as a logic chip. The buffer chip **1360** and at least one memory chip **1340** may be connected to each other by a through silicon via (TSV). In an embodiment, the buffer chip **1360** and the at least one memory chip **1340** may include the protection circuits and the interface circuits described with reference to FIGS. **1** to **12**. Accordingly, the semiconductor device **1300** according to an embodiment may include a through substrate via that electrically connects stacked semiconductor chips **1330**, and the at least one memory chip **1340** may include a first keep-out zone and a second keep-out zone around the through-substrate via. According to an embodiment, the semiconductor device **1300** may efficiently utilize an area of the semiconductor device **1300** by designing the protection circuit within the at least one memory chip **1340** to be disposed within the second keep-out zone around the through substrate via. In an embodiment, the stack semiconductor chip **1330** may be, e.g., a high bandwidth memory (HBM) of 500 GB/sec to 1 TB/sec or more.

[0101] While this disclosure has been described in connection with what is presently considered to be practical embodiments, it is to be understood that the disclosure is not necessarily limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent dispositions included within the spirit and scope of the present disclosure.

What is claimed is:

1. A three-dimensional (3D) integrated circuit, comprising:

a first integrated circuit including a first substrate;

a second integrated circuit stacked on the first integrated circuit;

a through via extending through the first substrate and electrically connecting the first integrated circuit to the second integrated circuit; and

a plurality of protection circuits disposed at opposite sides of the through via in a general keep-out zone surrounding the through via and electrically connected to the through via.

2. The 3D integrated circuit of claim **1**, wherein the general keep-out zone includes:

a first keep-out zone including an area spaced apart from an outer edge of the through via by a first distance in a first direction; and

a second keep-out zone including an area spaced apart from an outer edge of the first keep-out zone by a second distance that is greater than the first distance from the through via in the first direction,

wherein the plurality of protection circuits are disposed within the second keep-out zone.

3. The 3D integrated circuit of claim **2**, further comprising

an interface circuit which is adjacent to a first protection circuit among the plurality of protection circuits in the first direction outside of the second keep-out zone, and configured to transmit and receive logic signals to and from the second integrated circuit through the through via.

4. The 3D integrated circuit of claim **3**, wherein

the second keep-out zone includes a first area and a second area outside of the first keep-out zone at opposite sides of the through via, and

the first protection circuit is disposed in the first area, and a second protection circuit among the plurality of protection circuits is disposed in the second area.

5. The 3D integrated circuit of claim **3**, wherein

the through via and the interface circuit are electrically connected to one another using a plurality of metal layers, and the protection circuits are electrically connected to the plurality of metal layers.

6. The 3D integrated circuit of claim **2**, further comprising:

an interface circuit adjacent to the first keep-out zone outside of the second keep-out zone in a second direction perpendicular to the first direction, and configured to transmit and receive logic signals to and from the second integrated circuit through the through via.

7. The 3D integrated circuit of claim **2**, wherein:

the first keep-out zone is an area that does not include a metal layer other than the metal layer connected to the through via, and

the second keep-out zone is an area in which an active semiconductor device is not disposed.

8. The 3D integrated circuit of claim **1**, wherein

the protection circuits include an antenna protection circuit configured to provide antenna effect protection to the first integrated circuit.

9. The 3D integrated circuit of claim **8**, wherein

the antenna protection circuit includes an antenna diode.

10. The 3D integrated circuit of claim **1**, wherein

the plurality of protection circuits are electrostatic discharge (ESD) protection circuits configured to provide ESD protection to the first integrated circuit.

11. An integrated circuit, comprising:

a through extending through a first substrate;

a first keep-out zone disposed on the first substrate, and having a first boundary around the through via and spaced apart from the through via by a first distance in a first direction, and a second boundary spaced apart from the through via by a second distance in a second direction perpendicular to the first direction;

a second keep-out zone disposed on the first substrate, and having a third boundary around the through via and spaced apart from the through via by a third distance in the first direction, and a fourth boundary spaced apart from the through via by the second distance in the second direction;

a first protection circuit disposed outside of the first keep-out zone and inside of the second keep-out zone and electrically connected to the through via; and

an integrated circuit disposed outside of the second keep-out zone and including an interface circuit electrically connected to the through via.

12. The integrated circuit of claim **11**, wherein

the third distance is greater than the first distance.

13. The integrated circuit of claim **11**, wherein

the interface circuit, the first protection circuit, and the through via are sequentially arranged in the first direction.

14. The integrated circuit of claim **13**, further comprising:

a second protection circuit disposed outside of the first keep-out zone and inside of the second keep-out zone,

and disposed at an opposite side of the first protection circuit with respect to the through via.

15. The integrated circuit of claim **11**, wherein

the interface circuit is disposed adjacent the first keep-out zone in the second direction.

16. The integrated circuit of claim **15**, wherein

no element is disposed between the interface circuit and the first keep-out zone.

17. The integrated circuit of claim **11**, wherein

the first protection circuit includes an antenna protection circuit configured to provide antenna effect protection to a transistor located on the first substrate and an ESD protection circuit configured to provide ESD protection.

18. A three-dimensional (3D) integrated circuit comprising:

a first substrate;

a through via extending through the first substrate;

a first keep-out zone disposed on the first substrate and including an area around the through via at a first distance from the through via;

a second keep-out zone disposed on the first substrate and including an area extended by a second distance in a first direction from the first keep-out zone and in a direction opposite to the first direction;

a protection circuit disposed outside of the first keep-out zone and inside of the second keep-out zone and electrically connected to the through via; and

an interface circuit adjacent to the first keep-out zone in a second direction perpendicular to the first direction and electrically connected to the through via.

19. The 3D integrated circuit of claim **18**, wherein

the first keep-out zone is a keep-out zone in a back-end-of-line (BEOL) process, and the second keep-out zone is a keep-out zone in a front-end-of-line (FEOL) process.

20. The 3D integrated circuit of claim **18**, wherein

no element is disposed between the interface circuit and the first keep-out zone.

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