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Isolated Gate Driver

Abstract

An apparatus comprising an input stage comprising a first input, a second input, a first AC coupler, and a second AC coupler. The first AC coupler is coupled between the first input and a third input. The second AC coupler is coupled between the second input and a fourth input. A comparator coupled to the third input, the fourth input, and an output. The comparator provides an output signal at the output based on a comparison between a level of a first voltage at the third input, and a level of a second voltage at the fourth input. A feedback circuit, coupled to the output, the third input, and the fourth input. The feedback circuit receives the output signal, and provides, based on the output signal, a first feedback voltage to the third input.

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATIONS [0001] This application is a continuation of U.S. application Ser. No. 18/352,484, filed Jul. 14, 2023, which is a non-provisional of and claims priority to U.S. Provisional Application No. 63/390,611, filed Jul. 19, 2022 and U.S. Provisional Application No. 63/436,242, filed Dec. 30, 2022. Each of the above referenced applications is incorporated by reference herein in its entirety for all purposes.

FIELD OF THE DISCLOSURE
[0002] The disclosure relates generally to photovoltaic power systems. M ore specifically, the disclosure provides a system and method for regulating power production between power sources in a photovoltaic power system.
BACKGROUND OF THE DISCLOSURE
[0003] In the field of electronics, driver circuits (also referred to as 'gate drivers') may be employed to provide a signal for transitioning an electronic switch between states (e.g., between an 'on-state' in which the switch is conducting, and an 'off-state' in which the switch does not conduct). Examples of such switches may comprise transistors such as metal oxide semiconductor field effect transistors (MOSFETs), bipolar junction transistors (BJTs), insulated gate bipolar transistors (IG BTs), Gallium Nitride transistors, or Silicon Carbide (SiC) transistors. Regardless of the type of switch employed, a drive signal is required to cause the switch to transition between states. A gate driver may be configured to provide a signal to a control terminal of a switch (e.g., a gate terminal in a MOSFET, a Base terminal in a BJT). For example, in cases in which the switch is a MOSFET, the MOSFET includes a source terminal, a gate terminal, and a drain terminal. The state of the MOSFET may be controlled by applying a voltage to the gate terminal, relative to the source. Such a gate voltage may be on the order of several volts (e.g., 3V, 5V, 10V, 12V, 15V).
[0004] An example of an electronic device, in which a gate driver or gate drivers may be employed, may be a transistor half-bridge, which comprises two transistors coupled in series at a switching connection point. A connection point (e.g., may also be referred to as node) may be a connection between two or more electrical components (e.g., resistors, transistors, capacitors, inductors, diodes and the like). The series coupling of the two transistors may be connected across a voltage. For example, in cases in which n-type MOSFETS are employed, the source of a first transistor (also referred to as a 'high-side' transistor) may be coupled with the drain of a second transistor (also referred to as a 'low-side' transistor). The source of the low-side transistor may be coupled to a reference (e.g., ground), and the drain of the high-side transistor may be coupled with a voltage level (e.g., relative to the reference). In some cases, this voltage level may be tens, hundreds or even thousands of Volts. As such, while the voltage level required to drive high-side MOSFET, relative to the switch node, may be on the order of several volts, the voltage level required to drive high-side MOSFET, relative to the reference, may be one the order of tens or hundreds of volts.
[0005] A control signal for controlling the switches may be generated, for example, at a level of a few volts relative to the reference (e.g., 3.3V, 5V, 10V, or 12V relative to ground). A high-side gate driver may generate a voltage required to control the high-side switch relative to the switching node based on the control signal. However, as mentioned above, the switching node (e.g., which may be a reference of the high-side gate driver), may transition between zero volts, and tens or hundreds of volts relative to the reference. Such transitions may potentially damage the gate driver

or preceding circuitry (e.g., due to currents and/or voltages above the ratings of circuit components). Therefore, the high-side gate driver may be isolated from preceding circuitry (e.g., to reduce the probability of fault to the gate driver or preceding circuitry). The terms ‘isolated’, AC-coupled, or DC-blocked are used herein interchangeably.
[0006] For example, isolation of the high-side gate driver may be achieved using transformers, opto-couplers, capacitors, or Hall-effect sensors. The isolated gate driver may change the reference of the control signal (e.g., such that the switching node is the reference node of the control signal), and may further amplify the power of the control signal.
BRIEF SUMMARY OF THE DISCLOSURE
[0007] The following presents a simplified summary of the disclosure in order to provide a basic understanding of some aspects of the disclosure. This summary is not an extensive overview of the disclosure. It is not intended to identify key or critical elements of the disclosure or to delineate the scope of the disclosure. The following summary merely presents some concepts of the disclosure in a simplified form as a prelude to the more detailed description provided below.
[0008] A first aspect of the disclosure herein provides an isolated gate driver configured to provide a control signal to a control terminal of a switch. The isolated gate driver according to the disclosure herein may comprise an input stage for providing DC isolation for the gate driver, a comparator, and a feedback circuit. The comparator may compare a level of a first voltage with a level of a second voltage. In cases in which the first input voltage into the comparator may comprise two or more voltage levels, the output from the comparator may comprise two or more states, each of the at least two states may correspond to one of the at least two voltage levels. The feedback circuit may be configured to receive the output signal and set, based on the state of the output signal, the level of the first feedback voltage to one of the at least two voltage levels of the input voltage.
[0009] A second aspect of the disclosure herein provides a method for an isolated gate driver. In a first step a level of a first voltage at a first input, is compared by a comparator with a level of a second voltage at a second input. In a second step, a first feedback voltage is selected by a feedback circuit. In a third step, the first feedback voltage is applied to a first input of the comparator.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0010] A more complete understanding of the present disclosure and the advantages thereof may be acquired by referring to the following description in consideration of the accompanying drawings, in which like reference numbers indicate like features, and wherein:
[0011] FIG. **1** illustrates a schematic illustration of an apparatus, in accordance with aspects of the disclosure;
[0012] FIG. **2**A illustrates an isolation circuit according to aspects of the description herein;
[0013] FIGS. **2**B-**2**D illustrate examples of diagrams relating to a circuit according to aspects of the description herein;
[0014] FIGS. **3**A-**3**D illustrate examples of voltage levels generator according to aspects of the disclosure herein;
[0015] FIG. **4** illustrates an isolation circuit according to aspects of the disclosure herein;
[0016] FIG. **5** illustrates an apparatus in accordance with aspects of the disclosure herein;
[0017] FIG. **6** illustrates an apparatus in accordance with aspects of the disclosure herein;
[0018] FIG. **7** illustrate methods according to aspects of the disclosure herein;
[0019] FIG. **8** illustrate methods according to aspects of the disclosure herein;
[0020] FIGS. **9**A and **9**B, illustrate examples of implementing a capacitor using IC metal layers;
[0021] FIGS. **10**A-**10**D illustrate examples of AC couplers according to aspects of the disclosure

herein;

[0022] FIGS. **11**A-**11**F illustrate examples of waveforms according to aspects of the disclosure herein;

[0023] FIGS. **12**A-**12**L illustrate examples of waveforms according to aspects of the disclosure herein; and

[0024] FIGS. **13**A-**13**E illustrate timing diagrams and models in accordance with aspects of the disclosure herein.

DETAILED DESCRIPTION OF THE DISCLOSURE

[0025] In the following description of the various embodiments, reference is made to the accompanying drawings, which form a part hereof, and in which is shown by way of illustration various embodiments in which the disclosure may be practiced. It is to be understood that other embodiments may be utilized and structural and functional modifications may be made without departing from the scope of the present disclosure.

[0026] Aspects of the description herein relate to an isolated gate driver configured to provide a control signal to a control terminal of a switch (e.g., a gate of a MOSFET or IGBT, a base of a BJT). The gate driver according to the description herein is isolated, and may comprise a comparator, and a feedback circuit. The feedback circuit may control the voltage levels at the inputs of the comparator such that a change in voltage level of the input signal may result in a change in voltage level in the output of the comparator (e.g., the feedback circuit may control a differential voltage, a common mode voltage, or both differential and common mode voltage at the inputs of the comparator). The feedback circuit sets feedback voltages at the input terminals of the comparator, based on an output signal from the comparator, as further explained below. For example, a first input voltage into the comparator may comprise two or more voltage levels. The output from the comparator may comprise two or more states, each of the at least two states may correspond to one of the at least two voltage levels. The feedback circuit may be configured to receive the output signal and set, based on the state of the output signal, the level of the first feedback voltage to one of the at least two voltage levels of the input voltage.

[0027] Reference is now made to FIG. **1**, which is a schematic illustration of an apparatus, generally referenced **100**, in accordance with aspects of the disclosure. Apparatus **100** may comprise a gate driver **102**, a signal generator **104** and a switch **106**. Gate driver **102** may be an isolated gate driver, and may comprise an isolator **108**, and an output stage **110**. Isolator **108** may comprise an input stage **112**, a comparator **114**, and a feedback circuit **116**. Outputs of signal generator **104** may be coupled with first and second inputs **107**.sub.1 and **107**.sub.2 of gate driver **100**. Outputs of input stage **112** may be coupled to a third and a fourth inputs **109**.sub.1 and **109**.sub.2 of comparator **114**. An output **111** of comparator **114** may be coupled to an input of output stage **110**. Output stage **110** may be coupled to switch **106** (e.g., to a control terminal of switch **106**). Feedback circuit **116** may be coupled to output **111** of comparator **114** and to input stage **114**. Switch **106**, isolator **108**, and output stage **110** may be reference to a driver reference **118**. Signal generator **104** may be reference to a signal reference **120**. Driver reference **118** may be different from signal reference **120**. Input stage **112** may comprise an AC coupler, or AC couplers, configured to DC isolate gate driver **102**, at least from signal reference **120**.

[0028] Signal generator **104** may generate an input signal (e.g., for controlling switch **106**). The input signal may comprise two or more input voltage levels between first and second inputs **107**.sub.1 and **107**.sub.2 of gate driver **100**. The two or more input voltage levels may correspond to at least two states of switch **106** (e.g., a conducting state, or a non-conducting state). The input signal is provided to comparator **114**, via input stage **112**, at third and fourth inputs **109**.sub.1 and **109**.sub.2 of comparator **114**. The signal at third and fourth input **109**.sub.1 and **109**.sub.2 may comprise a level of a first voltage, relative to driver reference **118**, at third input **109**.sub.1, and a level of a second voltage, relative to driver reference **118**, at the fourth input **109**.sub.2. Input stage **112** is further elaborated below in conjunction with FIGS. **2**A-**2**D, **3**A-**3**D and **4**. Comparator **114** may compare the level of a first voltage at third input **109**.sub.1, and a level of a second voltage at the fourth input **109**.sub.2, and provide, based on this comparison, an output signal at output **111**. The output signal at node **111** may comprise at least two states, corresponding to the at least two voltage levels between third input **109**.sub.1 and fourth input **109**.sub.2. In some cases, both the first voltage level at third input **109**.sub.1, and second voltage level at fourth input **109**.sub.2, may transition between at least two levels. In some cases, the first voltage level at third input **109**.sub.1 may transition between at least two levels, and the second voltage level at fourth input **109**.sub.2 may remain constant.

[0029] Output stage **110** may amplify (e.g., a voltage or a power) the output signal from comparator **114**, and provide the amplified output signal to a control terminal of switch **106**. The amplified output signal may also comprise at least two states for controlling switch **106** (e.g., between a conducting state and a non-conducting state, or vice versa, or maintaining the current state of switch **106**). Output stage **110** may further be elaborated below in conjunction with FIG. **6**.

[0030] The output signal at output **111** of comparator **114** may also be provided to feedback circuit **116**. Feedback circuit **116** may control the level of a first voltage at third input **109**.sub.1, and a level of a second voltage at the fourth input **109**.sub.2 such that a change in voltage level of the input signal may result in a change in voltage level in the output of comparator **114**. For example, feedback circuit **116** may provide, based on the output signal, at least a first feedback voltage to input stage **112**. For example, feedback circuit may provide a first feedback voltage to third input **109**.sub.1, as further elaborated below in conjunction with FIGS. **2**A-**2**D, **3**A-**3**D and **4**. Feedback circuit **116** may provide a second feedback voltage to fourth input **109**.sub.2, also as further elaborated below in conjunction with FIGS. **2**A-**2**D, **3**A-**3**D and **4**. For example, the level of the first feedback voltage may correspond to one of the at least two levels of the first voltage at third input **109**.sub.1, relative to reference **118**. The level of the second feedback voltage may correspond to the level of the second voltage at fourth input **109**.sub.2, relative to reference **118**.

[0031] In some cases, circuit **100** may be implemented on an Integrated Circuit (IC) employing, for example, CMOS techniques, and On-Chip metal connections (e.g., as elaborated in herein below in conjunction with FIGS. **9**A and **9**B).

[0032] Reference is made to FIGS. **2**A-**2**D which shows an isolation circuit, generally referenced **200** and related diagrams, according to aspects of the description herein. Circuit **200** may comprise an isolator **202**, and a signal generator **204**. Isolator **202** may be part of a gate driver (e.g., gate driver **102**—FIG. **1**) and may correspond to isolator **108** (FIG. **1**). Isolator **202**, may comprise an input stage **206**, a comparator **208** and a feedback circuit **210**. The outputs of signal generator **204** may be coupled to inputs **224**.sub.1 and **224**.sub.2 of isolator **202**. Signal generator **204** may be referenced to a signal reference **222**.

[0033] Input stage may comprise two AC couplers, a first AC coupler **212**, and a second AC coupler **214**. In the example of FIG. **2**A, first AC coupler **212** may comprise a first impedance (e.g., capacitor C**1**) coupled between an input **224**.sub.1 of circuit **200**, and to a comparator input **226**.sub.1 of comparator **208**. First AC coupler **212** may further comprise a second impedance (e.g., capacitor C**2**), coupled between comparator input **226**.sub.1 and a driver reference **220**. The first impedance and the second impedance form a first impedance divider between input **224**.sub.1 and driver reference **220**. Second AC coupler **214** may comprise a third impedance (e.g., capacitor C**3**) coupled between an input **224**.sub.2 of circuit **200**, and a comparator input **226**.sub.2 of comparator **208**. Second AC coupler **214** may further comprise a fourth impedance (e.g., capacitor C**4**), coupled between comparator input **226**.sub.2 and driver reference **220**. The first impedance and the second impedance form a second impedance divider between input **224**.sub.1 and driver reference **220**. Additional examples of AC couplers may be described herein below in conjunction with FIGS. **10**A-**10**D. Comparator **208** may be coupled between an isolated supply voltage Vs_iso, which is referenced to a reference voltage (referred to as ‘Vref’ in FIGS. **2**B-**2**D), at driver reference **220**. Using capacitors C**2** and C**3**, as may be shown in FIG. **2**A (and FIG. **4**), may reduce the propagation delay of a gate driver according to aspects of the disclosure (e.g., relative to gate drivers in which resistors are used instead of C**2** and C**3**—due to a reduce time constant). Also, the ratio between C**2** and C**1**, and between C**3** and C**4**, may aid in reducing transients in the signals at the inputs **226**.sub.1 and **226**.sub.2.

[0034] Feedback circuit **210** may comprise a voltage levels generator **216**, and a controller **218**. Feedback circuit may comprise two impedances Z**1** and Z**2**. Controller **218** may be coupled to an output **228** of comparator **208**, and to voltage levels generator **216**. Voltage levels generator **216** may further be coupled to comparator input **226**.sub.1, optionally, via impedance Z**1**. Voltage levels generator **216** may be coupled to comparator input **226**.sub.2, optionally, via impedance Z**2**. Controller **212** may be implemented as a microcontroller, Field Programmable Gate Array (FPGA) or an Application Specific Integrated Circuit (ASIC) configured to carry out a set of control instructions.

[0035] The output **228** of comparator **208** may be coupled to a control terminal of a switch, such as switch **232**.sub.1 (e.g., a MOSFET, an IGBT, a BJT). In the example of FIG. **2**A, switch **232**.sub.1 may be a high-side switch in a half-bridge converter **230**. Half-bridge converter **230** may comprise switch **232**.sub.1 and a switch **232**.sub.2 (e.g., a MOSFET, an IGBT, a BJT), connected in series at a switching node, which may also correspond to driver reference **220** (e.g., the gate driver reference may be the switching node). The series connection of switch **232**.sub.1 and switch **232**.sub.2 may be coupled between a supply voltage, for example, as indicated by the labels 'V+' and 'V−' in FIG. **2**A. A load **234** may be connected between driver reference **220** and a power reference **236**. In cases in which switch **232**.sub.1 is in a conducting state and switch **232**.sub.2 is in a non-conducting state, the voltage of driver reference **220** may be V+. In cases in which switch **232**.sub.1 is in a non-conducting stage and switch **232**.sub.2 is in a conducting state, the voltage of driver reference **220** may be V−. In some cases, the difference between V+ and V− may be on the order of tens, hundreds or thousands of volts. Consequently, the voltage of driver reference **220** may vary, relative to power reference **236** or signal reference **222**, by tens, hundreds or thousands of volts. According to aspects of the disclosure herein, V− may be coupled to power reference **236**. In such a case voltage level V− is power reference **236**.

[0036] Signal generator **204**, may generate an input signal. For example, the input signal may be a Pulse Width Modulation (PWM) signal for controlling switch **232**.sub.1. A duty cycle of the PWM signal may vary. The input signal may comprise two or more input voltage levels between inputs **224**.sub.1 and **224**.sub.2. The two or more input voltage levels may correspond to at least two states of switch **232**.sub.1 (e.g., a conducting state, or a non-conducting state). The input voltage levels between inputs **224**.sub.1 and **224**.sub.2 may be between 0V and several volts (e.g., 3.3V, 5V, 7.5V, 10V, 12V, 15V, less than 50V). Signal generator **204** may provide the input signal to comparator inputs **226**.sub.1 and **226**.sub.2 via input stage **206**. For example, the voltage at input **224**.sub.1 may be provided to comparator input **226**.sub.1 via AC coupler **212**, and the voltage at input **224**.sub.2 may be provided to comparator input **226**.sub.2 via AC coupler **214**.

[0037] Input stage **206** may provide DC isolation between driver reference **220** and signal reference **222**. For example, capacitor C**1** and C**4** isolate a gate driver circuit **200**, which may include isolator **202** (e.g., may also referred to as isolated reference side or floating reference side), from other system components of modules. In FIG. **2**A, capacitor C**1** and C**4** isolate gated driver circuit **200** from the signal reference side (e.g., from generator **204**). As such, the voltage levels in isolator **202** may be referenced to driver reference **220**, the voltage levels from signal generator **204** may be referenced to signal reference **222**, and the voltage levels in half bridge converter may be referenced to power reference **236**. Therefore, even in cases in which switch **232**.sub.1 is in the conducting state, and the voltage of driver reference **220** may be V+(e.g., more than 100V, more than 1000V) relative to power reference **236**, signal generator may generate the input voltage levels between inputs **224**.sub.1 and **224**.sub.2 to be between 0V and several volts. The voltage level between the output of the gate driver and driver reference **220** may also be on the order of several volts, for example, for changing the state of switch **232**.sub.1.

[0038] Comparator **208** may compare the voltage level at comparator input **226**.sub.1 with the voltage level at comparator input **226**.sub.2 and provide an output signal at output **228** based on this comparison. This output signal is provided, either via an output stage (e.g., as further elaborated below in conjunction with FIG. **6**) or directly, to the control terminal of switch **232**.sub.1. The output signal from comparator **208** may comprise at least two states (e.g., a HIGH state, or a LOW state). For example, in cases in which the voltage level at comparator input **226**.sub.1 is higher than the voltage level at comparator input **226**.sub.2, the output signal from comparator **208** may be in a HIGH state. In cases in which the voltage level at comparator input **226**.sub.1 is lower than the voltage level at comparator input **226**.sub.2, the output signal from comparator **208** may be in a LOW state. In cases in which comparator **208** is an inverting comparator, the output signal from comparator **208** may be in a HIGH state, whereas the voltage level at comparator input **226**.sub.1 is lower than the voltage level at comparator input **226**.sub.2. The output signal from comparator **208** may be in a LOW state in cases in which the voltage level at comparator input **226**.sub.1 is higher than the voltage level at comparator input **226**.sub.2. Based on the output signal from comparator **208** being in a HIGH state, switch **232**.sub.1 may transition to, or maintain a conducting state. Based on the output signal from comparator **208** being in a LOW state, switch **232**.sub.1 may transition to, or maintain a non-conducting state. Comparator **208** may be implemented with an operational amplifier (Op-Amp) or Op-Amps, with digital gates (e.g., AND gates, OR gates, XOR gates), or discrete electronic components (e.g., transistors, diodes, or resistors).

[0039] To reduce the probability of error at the output **228** of comparator **208**, capacitors C**2** and C**3** may be charged to a determined voltage levels relative to driver reference **220**. These voltage levels aim to enable comparator **208** to detect a difference between the voltage levels at comparator input **226**.sub.1, and comparator input **226**.sub.2. However, these voltage levels may change for various reasons. For example, leakage of charge from, or to capacitors C**2** and C**3** may cause these voltage levels to change (e.g., see the discussion concerning FIGS. **11**A-**11**F below). The voltage levels at comparator input **226**.sub.1, and comparator input **226** may change, for example, in cases in which signal generator **204** generates signals with a varying duty cycle (e.g., a PWM signal). In a case of a signal with varying duty cycle, the voltage levels of capacitors C**2** and C**3**, relative to driver reference **220**, may vary based on the duty cycle. Referring to FIGS. **2**B-**2**D, these figures show signals **240**, **242** and **246** from signal generator **208**. Signals **240**, **242** and **246** are of different duty cycles. Signal **240** has a duty cycle of 50%, signal **242** has a duty cycle larger than 50%, and signal **246** has a duty cycled smaller than 50%. FIGS. **2**B-**2**D further depict signals **240**, **242** and **246** relative to the voltage level at driver reference **220**. FIGS. **2**B-**2**D further depict signals **240**, **242** and **246** relative to a positive threshold voltage, '+Vth', and a negative threshold voltage '−Vth', of the voltage difference between inputs **226**.sub.1 and **226**.sub.2 at comparator **208**. +Vth, and −Vth relate to the voltage difference between the voltage levels at comparator input **226**.sub.1, and comparator input **226**.sub.2, which generate a HIGH state or a LOW state of the output signal at output **228** respectively. For example, +Vth may relate to a case in which the voltage level at comparator input **226**.sub.1 is higher than the voltage level at comparator input **226**.sub.2 (e.g., may be referred to as a positive difference between the voltage levels). −Vth may relate to a case in which the voltage level at comparator input **226**.sub.1 is lower than the voltage level at comparator input **226**.sub.2 (e.g., may be referred to as a negative difference between the voltage levels).

[0040] In FIG. **2**B, signal **240** has a duty cycle of 50%. Signal **242** may rise above +Vth, or fall below −Vth. Thus, comparator **208** may detect a voltage difference between comparator input **226**.sub.1, and comparator input **226**.sub.2. In FIG. **2**C, signal **242** has a duty cycle larger than 50%. Signal **242** may fall below −Vth, but not rise above +Vth. In such a case, comparator **208** may detect a negative difference but may not be able to detect a positive difference. In FIG. **2**D, signal **246** has a duty cycle less than 50%. Signal **246** may rise above +Vth, but not fall below

−Vth. In such a case, comparator **208** may detect a positive difference but may not be able to detect a negative difference. In FIGS. **2**C and **2**D, the effect of the duty cycle is depicted as a modulation of Vref. In FIG. **2**C, Vref is depicted as increasing, relative to **226**.sub.1. In FIG. **2**D, Vref is depicted as decreasing, relative to **226**.sub.1. For example, such a modulation of Vref may be due to the averaging of the PWM signal over capacitors C**2** and C**3**.

[0041] A circuit according to aspects of the disclosure herein, may reduce the effect of varying duty cycle on the modulation of Vref, as well as leakage of charge from capacitors C**1**, C**2**, C**3** or C**4**, by providing feedback voltage from feedback circuit **210**. Feedback circuit **210** may control the level of a first voltage at input **226**.sub.1, a level of a second voltage at the input **226**.sub.2 or both, such that a change in voltage level of the input signal may result in a change in voltage level in a corresponding change the output **228** of comparator **208** (e.g., with a determined propagation delay). For example, feedback circuit **210** may control a differential voltage, a common mode voltage, or both differential and common mode voltage at input **226**.sub.1 and **226**.sub.2. Referring to FIG. **2**A, based on an output of comparator **208**, feedback circuit **210** may provide a first feedback voltage level ‘V_1’, relative to Vref, for comparator input **226**.sub.1. Feedback circuit **210** may provide a second feedback voltage level ‘V_2’, relative to Vref, for comparator input **226**.sub.2. According to aspects of the disclosure herein, controller **218** may generate a control signal for voltage levels generator **216**, based on the output signal at output **228** of comparator **208**. Voltage levels generator **216** generates, V_1, V_2, or both V_1 and V_2, based on a control signal from controller **218**. V_1, V_2, or both V_1 and V_2, latch the input voltage of comparator **208**, based on the output state (e.g., HIGH state or LOW state) of comparator **208**. For example, in cases in which the output signal from comparator **208** is at a HIGH state, controller **218** may generate a control signal for voltage levels generator **216** to generate V_1, V_2, or both V_1 and V_2, such that the voltage at comparator input **226**.sub.1 is higher than the voltage at comparator input **226**.sub.2 (e.g., by charging or discharging C**2**, C**3**, or both via the respective impedances Z**1** and Z**2**). In cases in which the output signal from comparator **208** is at a LOW state, controller **218** may generate a control signal for voltage levels generator **216** to generate V_1, V_2, or both V_1 and V_2, such that the voltage at comparator input **226**.sub.1 is lower than the voltage comparator input **226**.sub.2 (e.g., by charging or discharging C**2**, C**3**, or both via the respective impedances Z**1** and Z**2**). Thus, with reference to FIGS. **2**C and **2**D, Vref may be maintained relative to input **226**.sub.1 and input **226**.sub.2, as depicted by dashed lines **244** and **248** respectively, at different duty cycles of the input signal.

[0042] According to aspects of the disclosure herein, voltage levels generator **216** may generate first feedback voltage level V_1, or second feedback voltage level V_2 to correspond to the input voltages at comparator inputs **226**.sub.1 and **226**.sub.2, which resulted in the state of the output signal. For example, input **224**.sub.2 may be coupled with signal reference **222**, and the voltage at input **224**.sub.1 may vary between at least two levels relative to input **224**.sub.2 (e.g., between 0V and 3.3V or 5V). In such a case, the voltage at input **226**.sub.2 may be a constant voltage level relative to Vref at driver reference **220**. The voltage at input **226**.sub.1 may correspond to one of two levels, relative to the voltage at input **226**.sub.2 (e.g., as may be determined by the capacitance values of C**1**, C**2**, C**3** and C**4**). For example, in cases in which the voltage at input **226**.sub.2 is a constant, this voltage may be referred to as ‘common voltage’, Vcm. The voltage at input **226**.sub.1 may be a differential voltage, Vd, above or below the common voltage. For example, the voltage at input **226**.sub.1 may be Vcm+V d, or Vcm−Vd.

[0043] Voltage levels generator **216** may generate V_1 to correspond to the voltage level at input **226**.sub.1, relative to Vref at driver reference **220**, which resulted in the state of the output signal from comparator **208** (e.g., the state of comparator output **228**). For example, in cases in which the voltage at input **226**.sub.2 is a constant of 0.5V relative to Vref at driver reference **220** (e.g., Vcm=0.5), voltage levels generator **216** may generate V_2 to be 0.5V relative to Vref. In cases in which a voltage level at input **226**.sub.1, that corresponds to a HIGH state at comparator output **228** is 0.65V relative to Vref (e.g., V d=0.15V above V_2), voltage levels generator **216** may generate V_1 to be 0.65V relative to Vref, based on the state of the output signal at comparator output **228** being in a HIGH state. In cases in which a voltage level at input **226**.sub.1 that corresponds to a LOW state at comparator output **228** is 0.35V relative to Vref (e.g., V d=0.15V below V_2), voltage levels generator **216** may generate V_1 to be 0.35V relative to Vref, based on the state of the output signal at comparator output **228** being in a LOW state. For example, feedback circuit **210** latches the input voltage that generated the state of the output signal until a change may occur in the input signal. As further explained below in conjunction with FIGS. **12**A-**12**L and **13**A-**13**E, feedback circuit **210** may produce a modulated feedback voltage (e.g., modulated based on the input signal) to control the voltage levels at input **226**.sub.1 and input **226**.sub.2.

[0044] According to aspects of the disclosure herein, and as further elaborated below in conjunction with FIG. **3**D, voltage levels generator **216** may comprise impedances such as Z**1** and Z**2**. Impedances Z**1** and Z**2** may define, along with capacitors C**1**, C**2**, C**3**, and C**4** a time constant or time constants. Such a time constant may be related to a rate of change of the voltage at inputs **226**.sub.1 and **226**.sub.2, which may result in a response time of voltages at inputs **226**.sub.1 and **226**.sub.2 to the generation of V_1 and V_2 by voltage levels generator **216**. For example, with reference to FIGS. **2**C and **2**D, dashed lines **244** and **248** illustrate the response of the voltage Vref at driver reference **220**, relative to the voltage at input **226**.sub.1, based on the applied feedback voltage, and the impedances Z**1** and Z**2**. As seen in FIGS. **2**C and **2**D, Vref may respond to the applied feedback voltage over a response time.

[0045] Similar to as mentioned above, in some cases, isolator **202** may be implemented on an Integrated Circuit (IC) employing, for example, CMOS techniques and On-Chip metal connections. For example, capacitors C**1**, C**2**, C**3** and C**4** may be implemented by the metals employed in the IC, as in the examples in FIGS. **9**A and **9**B.

[0046] Reference is now made to FIGS. **3**A-**3**D, which illustrate examples of voltage levels generator, such as voltage levels generator **216** (FIG. **2**A), and still referring to FIG. **2**A. FIG. **3**A illustrates a voltage levels generator, generally referenced **300**, which may comprise a voltage levels generator **302**, and a double pole multi-throw switch **304**. Voltage levels generator **302** may be coupled between an isolated supply voltage, Vs_iso, and reference **306**. Voltage levels generator **302** may generate a plurality of voltages V**1**-VN. Controller **218** (FIG. **2**A), may operate double pole multi-throw switch **304** to select V_1 and V_2, based on the output from comparator **208** at comparator output **228**.

[0047] FIG. **3**B illustrates a voltage levels generator, generally referenced **310**, which may comprise a voltage levels generator **312**, and a single pole multi-throw switch **314**. Voltage levels generator **312** may be coupled between an isolated supply voltage, Vs_iso and reference **316**. Voltage levels generator **310** may be employed, in cases in which V_2 is constant. In such a case, voltage levels generator **312** may generate V_2, as well as a plurality of voltages V**1**-V N. Controller **218** may operate single pole multi-throw switch **314** to select V_1. For example, V_2 may beset to the common voltage Vcm and V_1 may be selected to be various values above or below Vcm.

[0048] FIG. **3**C illustrates an example of voltage levels generator, generally referenced **320**. Voltage levels generator **320** may comprise a voltage levels generator **322**, and a single pole double throw switch **324**. In FIG. **3**C, voltage levels generator **322** may be implemented by an impedance divider. Voltage levels generator **322** may comprise four impedances Z**1**, Z**2**, Z**3**, and Z**4** coupled in series. Z**1** may be coupled to Z**2** at connection point **326**. Z**2** may be coupled to Z**3** at connection point **327**, and Z**3** may be coupled to Z**4** at connection point **328**. The series coupling of impedances Z**1**-Z**4** may be coupled between an isolated supply voltage, ‘Vs_iso’, and a reference **325** (e.g., which may correspond to reference **220**). Voltage levels generator **322** may generate a constant V_2 at connection point **327** between Z**2** and Z**3**. Voltage levels generator **322** may generate a V_1 to be either V**1** at connection point **326** between Z**1** and Z**2**, or V**2** at connection point **328** between Z**3** and Z**4**. Connection point **326** may be coupled to a first input of single pole double throw switch **324**. Connection point **328** may be coupled to a second input of single pole double throw switch **324**. Controller **218** may control switch **324** to select either V**1** or V**2**, as the first feedback voltage V_1.

[0049] FIG. **3**D illustrates an example of voltage levels generator, generally referenced **330**. Voltage levels generator **330** may comprise a voltage levels generator **332**, and a single pole double throw switch **334**. In FIG. **3**D, voltage levels generator **332** may be implemented by an impedance divider, and single pole double throw switch **334** may be implemented with switches **338** and **340** (depicted as two MOSFETS in FIG. **3**D). Voltage levels generator **332** may comprise four impedances Z**1**, Z**2**, Z**3**, and Z**4** coupled in series. Z**1** may be coupled to Z**2** at connection point **336**. Z**2** may be coupled to Z**3** at connection point **337**, and Z**3** may be coupled to Z**4** at connection point **338**. The series coupling of impedances Z**1**-Z**4** may be coupled between an isolated supply voltage 'Vs_iso', and a reference connection point **335** (e.g., which may correspond to reference **220**). Voltage levels generator **332** may generate a constant V_2 from the voltage at connection point **337** between Z**2** and Z**3**, applied over an impedance Z**6** coupled to connection point **337**. Impedance Z**6** may correspond to impedance Z**2** in FIG. **2**A. Voltage levels generator **332** may generate a V_1 to be either V**1** at connection point **336** between Z**1** and Z**2**, or V**2** at connection point **338** between Z**3** and Z**4**, applied over an impedance Z**5** coupled to the output of switch **334**. Impedance Z**5** may correspond to impedance Z**1** in FIG. **2**A. Connection point **336** may be coupled to a first input of single pole double throw switch **334**. Connection point **338** may be coupled to a second input of single pole double throw switch **334**. Controller **218** may control switch **334** to select V**1**, applied over Z**5**, by controlling switch **338** to be in a conducting state, and controlling switch **340** to be in a non-conducting state. Controller **218** may control switch **334** to select V**2**, applied over Z**5**, as V_1 by controlling switch **338** to be in a non-conducting state, and controlling switch **340** to be in a conducting state.

[0050] According to aspects of the disclosure a voltage levels generator such as described above in conjunction with FIGS. **1**, **2**A, **3**A-**3**D, may be implemented as a Digital to Analog Converter.

[0051] A gate driver according to aspects of the disclosure, may comprise a sensor for sensing the voltage between the driver reference (e.g., reference **220**—FIG. **2**A), and either a power reference (e.g., power reference **236**—FIG. **2**), or signal reference (e.g., signal reference **222**—FIG. **2**), or both. In some cases, the power reference and the signal reference may be one and the same. Sensing the voltage between the driver reference, and at least one of the power reference, or the signal reference may provide information, for example, relating to discrepancies between the state of the output of the comparator, and the state of either the signal generator or the half bridge converter.

[0052] Reference is now made to FIG. **4**, which illustrates an isolation circuit, generally referenced **400**, according to aspects of the description herein. Circuit **400** may be similar to circuit **200** (FIG. **2**A), and may be a part of an isolated gate driver. Circuit **400** may comprise an isolator **402**, and a signal generator **404**. Isolator **402** may comprise an input stage **406**, a comparator **408**, a feedback circuit **410**, and a sensor **411**. The outputs of signal generator **404** may be coupled to inputs **424**.sub.1 and **424**.sub.2 of isolator **402**. Signal generator **404** may be referenced to a signal reference **422**.

[0053] Input stage may comprise two AC couplers, a first AC coupler **412**, and a second AC coupler **414**. In the example of FIG. **4**, first AC coupler **412** and second AC coupler **414** are similar to first AC coupler **212** and second AC coupler **214** (FIG. **2**A). Additional examples of AC couplers may be described herein below in conjunction with FIGS. **10**A-**10**D. First AC coupler **412** may comprise a first impedance (e.g., capacitor C**1**) coupled between an input **424**.sub.1 of circuit **400**, and to a comparator input **426**.sub.1 of comparator **408**. First AC coupler **412** may further comprise a second impedance (e.g., capacitor C**2**), coupled between comparator input **426**.sub.1 and a driver reference **420**. The first impedance and the second impedance form a first impedance divider between input **424**.sub.1 and driver reference **420**. Second AC coupler **414** may comprise a third impedance (e.g., capacitor C**3**) coupled between an input **424**.sub.2 of circuit **400**, and a comparator input **426**.sub.2 of comparator **408**. Second AC coupler **414** may further comprise a fourth impedance (e.g., capacitor C**4**), coupled between comparator input **426**.sub.2 and driver reference **420**. The first impedance and the second impedance form a second impedance divider between input **424**.sub.1 and driver reference **420**. Comparator **408** may be coupled between an isolated supply voltage Vs_iso, which is referenced to a reference voltage (referred to as 'Vref' in FIG. **4**), at driver reference **420**.

[0054] Feedback circuit **410** may comprise a voltage levels generator **416**, and a controller **418**. Feedback circuit may comprise two impedances Z**1** and Z**2**. Controller **418** may be coupled to a comparator output **428** of comparator **408**, and to voltage levels generator **416**. Voltage levels generator **416** may further be coupled to comparator input **426**.sub.1, optionally, via impedance Z**1**. Voltage levels generator **416** may be coupled to comparator input **226**.sub.2, optionally, via impedance Z**2**. Voltage levels generator **416** may be similar to voltage level generators **300**, **310**, **320**, or **330** described above in conjunction with FIGS. **3**A-**3**D. Controller **412** may be implemented as a microcontroller, a Field Programmable Gate Array (FPGA) or an Application Specific Integrated Circuit (ASIC) configured to carry outa set of control instructions.

[0055] The comparator output **428** may be coupled to a control terminal of a switch, such as switch **432**.sub.1 (e.g., a MOSFET, an IGBT, a BJT). Similar to the example in FIG. **2**A, switch **432**.sub.1 may be a high-side switch in a half-bridge converter **430**. Half-bridge converter **430** may comprise switch **432**.sub.1 and a switch **432**.sub.2 (e.g., a MOSFET, an IGBT, a BJT) connected in series at a switching node, which may also correspond to driver reference **420**. The series connection of switch **432**.sub.1 and switch **432**.sub.2 may be coupled between a supply voltage, for example, as indicated by the labels 'V+' and 'V−'. A load **434** may be connected between driver reference **420** and a power reference **436**. In cases in which switch **432**.sub.1 is in a conducting state and switch **432**.sub.2 is in a non-conducting state, the voltage of driver reference **420** may be V+. In cases in which switch **432**.sub.1 is in a non-conducting state and switch **432**.sub.2 is in a conducting state, the voltage of driver reference **420** may be V−. In some cases, the difference between V+ and V− may be on the order of tens, hundreds or thousands of volts. Consequently, the voltage of driver reference **420** may vary, relative to power reference **436** or signal reference **422**, by tens, hundreds or thousands of volts. According to aspects of the disclosure herein, V− may be coupled to power reference **436**. In such a case voltage level V− is power reference **436**.

[0056] Signal generator **404**, may generate an input signal. For example, the input signal may be a Pulse Width Modulation (PWM) signal for controlling switch **432**.sub.1. A duty cycle of the PWM signal may vary. The input signal may comprise two or more input voltage levels between inputs **424**.sub.1 and **424**.sub.2. The two or more input voltage levels may correspond to at least two states of switch **432**.sub.1 (e.g., a conducting state, or a non-conducting state). The input voltage levels between inputs **424**.sub.1 and **424**.sub.2 may be between 0V and several volts (e.g., 3.3V, 5V, 7.5V, 10V, 12V, 15V, less than 50V). Signal generator **404** may provide the input signal to comparator inputs **426**.sub.1 and **426**.sub.2 via input stage **406**. For example, the voltage at input **424**.sub.1 may be provided to comparator input **426**.sub.1 via AC coupler **412**, and the voltage at input **424**.sub.2 may be provided to comparator input **426**.sub.2 via AC coupler **414**.

[0057] Input stage **406** may provide DC isolation between driver reference **420** and signal reference **422**. For example, capacitor C**1** and C**4** isolate a gate driver circuit which may include isolator **402** (e.g., may also referred to as isolated reference side or floating reference side), from other system components of modules. In FIG. **4**, capacitor C**1** and C**4** isolate gated driver circuit **400** from the signal reference side (e.g., from generator **404**). As such, the voltage levels in isolator **402** may be referenced to driver reference **420**, the voltage levels from signal generator **404** may be referenced to signal reference **422**, and voltage levels in half bridge converter may be referenced to power reference **436**. Therefore, even in cases in which switch **432**.sub.1 is in the conducting state, and the voltage of driver reference **420** may be V+(e.g., more than 100V, more than 1000V) relative to power reference **436**, signal generator may generate the input voltage levels between inputs **424**.sub.1 and **424**.sub.2 to be between 0V and several volts. The voltage level between the output of the gate driver and driver reference **420** may also be on the order of several volts, for example, for changing the state of switch **432**.sub.1.

[0058] Comparator **408** may compare the voltage level at comparator input **426**.sub.1 with the voltage level at comparator input **426**.sub.2, and provide an output signal at comparator output **228** based on this comparison. This output signal is provided, either via an output stage (e.g., as further elaborated below in conjunction with FIG. **6**) or directly, to the control terminal of switch **432**.sub.1. The output signal from comparator **408** may comprise at least two states (e.g., a HIGH state, or a LOW state). For example, in cases in which the voltage level at comparator input **426**.sub.1 is higher than the voltage level at comparator input **426**.sub.2, the output signal from comparator **408** may be in a HIGH state. In cases in which the voltage level at comparator input **426**.sub.1 is lower than the voltage level at comparator input **426**.sub.2, the output signal from comparator **408** may be in a LOW state. In cases in which comparator **408** is an inverting comparator, the output signal from comparator **408** may be in a HIGH state, whereas the voltage level at comparator input **426**.sub.1 is lower than the voltage level at comparator input **426**.sub.2. The output signal from comparator **408** may be in a LOW state in cases in which the voltage level at comparator input **426**.sub.1 is higher than the voltage level at comparator input **426**.sub.2. Based on the output signal from comparator **408** being in a HIGH state, switch **432**.sub.1 may transition to, or maintain a conducting state. Based on the output signal from comparator **408** being in a LOW state, switch **432**.sub.1 may transition to, or maintain a non-conducting state.

[0059] Similar to as described above in conjunction with FIGS. **2**A-**2**D, to reduce the probability of error at comparator output **428** of comparator **408**, capacitors C**2** and C**3** may be charged to a determined voltage levels relative to driver reference **420**. Feedback circuit **410** may control the level of a first voltage at input **426**.sub.1, and a level of a second voltage at the input **426**.sub.2 such that a change in voltage level of the input signal may result in a corresponding change in voltage level in the output **428** of comparator **408** (e.g., with a determined propagation delay). For example, feedback circuit **410** may control a differential voltage, a common mode voltage, or both differential and common mode voltage at input **426**.sub.1 and **426**.sub.2. These voltage levels aim to enable comparator **408** to detect a difference between the voltage levels at comparator input **426**.sub.1 and comparator input **426**.sub.2. However, these voltage levels may change for various reasons (e.g., leakage of charge from or to capacitors C**2** and C**3**, or varying PWM signal from signal generator **404**). A circuit according to aspects of the disclosure herein may reduce the effect of varying duty cycle on the modulation of Vref, as well as leakage of charge from capacitors C**1**, C**2**, C**3** or C**4**, by providing feedback voltage from feedback circuit **410**. For example, based on an output of comparator **408**, feedback circuit **410** may provide a first feedback voltage level ‘V_1’, relative to Vref, for comparator input **426**.sub.1. Feedback circuit **410** may provide a second feedback voltage level ‘V_2’, relative to Vref, for comparator input **426**.sub.2. According to aspects of the disclosure herein, controller **418** may generate a control signal for voltage levels generator **416**, based on the output signal at comparator output **428**. Voltage levels generator **416** generates V_1, V_2, or both V_1 and V_2, based on a control signal from controller **418**. V_1, V_2, or both V_1 and V_2, latch the input voltage of comparator **408**, based on the output state (e.g., HIGH state or LOW state) of comparator **208**. For example, in cases in which the output signal from comparator **408** is at a HIGH state, controller **418** may generate a control signal for voltage levels generator **416** to generate V_1, V_2, or both V_1 and V_2, such that the voltage at comparator input **426**.sub.1 is higher than the voltage at comparator input **426**.sub.2. In cases in which the output signal from comparator **408** is at a LOW state, controller **418** may generate a control signal for voltage levels generator **416** to generate V_1, V_2, or both V_1 and V_2, such that the voltage at comparator input **426**.sub.1 is lower than the voltage comparator input **426**.sub.2.

[0060] Similar to as described above in conjunction with FIG. **2**A, voltage levels generator **416** may generate first feedback voltage level V_1, or second feedback voltage level V_2 to correspond to the input voltages at comparator inputs **426**.sub.1 and **426**.sub.2, which resulted in the state of the output signal. For example, input **424**.sub.2 may be coupled with signal reference **422**, and the voltage at input **424**.sub.1 may vary between at least two levels relative to input **424**.sub.2 (e.g., between 0V and 3.3V or 5V). In such a case, the voltage at comparator input **426**.sub.2 may be a constant voltage level relative to the voltage at driver reference **420**. The voltage at comparator input **426**.sub.1 may correspond to one of two levels, relative to the voltage at comparator input **426**.sub.2 (e.g., as may be determined by the capacitance values of C**1**, C**2**, C**3** and C**4**). Voltage levels generator **416** may generate V_1 to correspond to the voltage level at comparator input **426**.sub.1, relative to the voltage at driver reference **420**, which resulted in the current state of the output signal from comparator **408**. For example, in cases in which the voltage at comparator input **426**.sub.2 is a constant of 0.5V relative to the voltage at driver reference **420**, voltage levels generator **416** may generate V_2 to be 0.5V relative to Vref. In cases in which a voltage level at comparator input **426**.sub.1, that corresponds to a HIGH state at comparator output **428** is 0.75V relative to the voltage at driver reference **420**, voltage levels generator **416** may generate V_1 to be 0.75V relative to the voltage at driver reference **420**, based on the state of the output signal at comparator output **428** being in a HIGH state. In cases in which a voltage level at comparator input **426**.sub.1, that corresponds to a LOW state at comparator output **428** is 0.25V relative to Vref, voltage levels generator **416** may generate V_1 to be 0.25V relative to Vref, based on the state of the output signal at comparator output **428** being in a LOW state. For example, feedback circuit **410** latches the input voltage that generated the state of the output signal.
[0061] As mentioned above, circuit **400** may comprise a sensor **411** coupled to controller **418**, and to driver reference **420**. Sensor **411** may further be coupled to either power reference **436**, or signal reference **422**, or both. In some cases, power reference **436** and signal reference **422** may be one and the same. According to embodiments of the disclosure herein, sensor **411** may be coupled between comparator input **426**.sub.1 and driver reference **420** (e.g., across capacitor C**2**).
[0062] Sensor **411** may be a voltage sensor and may be implemented by employing a resistive or capacitive divider, a resistive or capacitive bridge, comparators (e.g., employing operational amplifiers), or the like. Sensor **411** may be configured to measure the voltage between driver reference **420** and power reference **436**, between driver reference **420** and signal reference **422**, or between driver reference **420** and both power reference **436** and signal reference **422**.
[0063] Sensing (e.g., by sensor **411**) the voltage between driver reference **420**, and at least one of the power reference **436**, or the signal reference **422**, may provide information, for example, relating to discrepancies between the state of the output of comparator **408**, and the state of either signal generator **404** or half bridge converter **430**. For example, based on a measurement of the voltage between driver reference **420** and power reference **436** from sensor **411**, controller **418** may detect that the output of comparator **408** is at a HIGH state, but the voltage between driver reference **420** and power reference **436** may indicate that the output of comparator **408** should be in a LOW state (or vice versa). In cases in which controller **418** detects a discrepancy, or an unexpected change between the voltages of driver reference **420** and signal reference **422**, or between driver reference **420** and power reference **436**, controller **418** may output a previously determined control signal.
[0064] It can be shown that:
[00001] $V_p - V_{\mathrm{ref}} = \frac{C1}{C1+C2} V_{\mathrm{PWM}} - \frac{C1}{C1+C2} V_{\mathrm{ref}} + V_{p,0} \quad (1) \quad V_n - V_{\mathrm{ref}} = -\frac{C4}{C4+C3} V_{\mathrm{ref}} + V_{n,0} \quad (2)$
where ‘V.sub.p’ is a voltage at comparator input **426**.sub.1, Vref is the voltage at driver reference **420** (e.g., relative to signal reference **422**), and ‘V.sub.p,0’ is the voltage at comparator input **426**.sub.1 at a time t=0. ‘V.sub.n’ is a voltage at comparator input **426**.sub.2, and ‘V.sub.n,0’ is the voltage at comparator input **426**.sub.2 at a time t=0. As can be seen from Equation (1), V.sub.p-

V.sub.ref may increase or decrease depending on V.sub.ref and on C**2**. As can be seen from Equation (2), V.sub.n−V.sub.ref may increase or decrease depending on V.sub.ref, and on C**3**. From equations (1) and (2), V.sub.p−V.sub.n (e.g., the input to comparator **402**) depends on C**2**, C**3**, and V.sub.ref. A change in V.sub.ref, may affect the output of comparator **408** (e.g., in some cases, V.sub.p−V.sub.n voltage reduces to a level at which comparator **408** does not respond). In the example of FIG. **4**, V.sub.ref may change to be either V− or V+ of Half-bridge converter **430**. C**2** or C**3** may be selected to allow for such variations in Vref, while maintaining V.sub.n−V.sub.p at a range in which comparator **408** may respond.

[0065] According to aspects of the disclosure herein, the common voltage, Vcm, may be selected based on changes to Vref. Adjusting the common voltage based on Vref may allow for selection of C**2** and C**3** such that V.sub.p−V.sub.n may increase (e.g., thus improving the signal to noise ratio). According to aspects of the disclosure herein, sensor **411** may measure a voltage between reference **420** and signal reference **422**. Controller **418** may control voltage levels generator **416** to set a voltage at comparator input **426**.sub.2 based on this measured voltage. For example, controller **418** may control voltage levels generator **416** to set a voltage at comparator input **426**.sub.2 to be one of two voltage levels relative to Vref (e.g., Vcm is set to one of two levels relative to Vref, Vcm**1**, or Vcm**2**). Controller **418** may control voltage levels generator **416** to set a differential voltage at comparator input **426**.sub.1 to be one of two voltage levels relative to the Vref (e.g., Vd above Vcm**1** or Vcm**2**, or Vd below Vcm**1** or Vcm**2**). For example, with reference to FIG. **3**A, controller **418** may control voltage levels generator **300** to generate V_1 and V_2 based on the output from comparator **408**, and based on a measurement from sensor **411** of the voltage between driver reference **420** and signal reference **422**. Controlling Vcm based on the measured voltage between driver reference **420** and signal reference **422**, may allow for selection of C**2** and C**3** such that V.sub.p−V.sub.n increases (e.g., in some cases V.sub.p−V.sub.n may increase by a factor of two).

[0066] According to aspects of the disclosure herein, Vcm may be controlled based on a state of the output of comparator **408**. In such cases, the voltages at comparator inputs **426**.sub.1 and **426**.sub.2 may be initialized to predetermined values to correspond to an initial state of the output of comparator **408**. For example, capacitors C**2** and C**3** may be pre-charged prior to the start of operation of circuit (e.g., by initially setting the output of comparator **408** to predetermined state, which causes voltage generator **416** to initially generate voltages V_1 and V_2 based on this predetermined state). The voltages at comparator inputs **426**.sub.1 and **426**.sub.2 may be initialized to predetermined values based on a known initial state of signal generator **404**.

[0067] The examples above are related to an isolated gate driver which may be configured to control the transition of a high-side switch in a half bridge converter. An isolated gate driver according to aspects of the disclosure herein may be configured to control the transition of switches in other types of converters as well. Reference is now made to FIG. **5**, which illustrates an apparatus, generally referenced **500**, in accordance with aspects of the disclosure herein. Apparatus **500** may comprise a flyback converter **502**, an isolated gate driver **504**, and a signal generator **506**. Flyback converter **502** may comprise a transformer **510**, a switch **512**, a diode **514**, and a capacitor **516**. Switch **512** is exemplified as an n-type MOSFET.

[0068] The primary side of transformer **510** may be coupled between an isolated supply voltage, labeled ‘Vs_iso’ in FIG. **5**, and a drain of switch **512**. Capacitor **516** may be coupled in series with diode **514** at the cathode of diode **514**. The series connection of diode **514** and capacitor **516** may be coupled across transformer outputs **522**.sub.1 and **522**.sub.2 of the secondary side of transformer **510** (e.g., such that the anode of diode **514** is coupled to transformer output **522**.sub.1). An output terminal **524**.sub.1 may be coupled to the cathode of diode **514**, and an output terminal **524**.sub.2 may be coupled to transformer output **522**.sub.2. The source of switch **512** may be coupled to a driver reference **518**. A load **520** may be coupled across output terminals **524**.sub.1 and **524**.sub.2.

[0069] Signal generator **506** may be similar to signal generators **104** (FIG. **1**), signal generator **204** (FIG. **2**A), or to signal generator **404** (FIG. **4**), and may be coupled to the input of isolated gate driver **504**. Isolated gate driver **504** may be similar to isolated gate driver **400** described above in conjunction with FIG. **4** and may comprise a sensor **508**. The output of isolated gate driver **504** may be coupled to the gate of switch **512**. Signal generator **506** and load **520** may be referenced to a reference **526**. Isolated gate driver **504** and primary side of flyback converter **502** may be referenced to driver reference **518**. Sensor **508** may be coupled with reference **526**, and with driver reference **518**. Sensor **508** may be configured to measure a voltage between reference **526**, and driver reference **518**. Sensing the voltage between driver reference **518**, reference **526** provides information, for example, relating discrepancies between the state of the output of isolated gate driver **504**, and the state of switch **512**, or may be used to control Vcm to increase the signal to noise ratio.

[0070] As mentioned above in conjunction with FIG. **1**, an isolated gate driver according to the disclosure may comprise an output stage. Reference is now made to FIG. **6**, which illustrates an apparatus, generally referenced **600**, in accordance with aspects of the disclosure herein. Apparatus **600** may comprise two gate drivers, high side gate driver **608** and low side gate driver **609**. For example, high side gate driver **608** may drive a high side switch **604**.sub.1 of a half bridge **602**. Low side gate driver **609** may drive a low side switch **604**.sub.2 of a half bridge **602**. High side gate driver **608** may correspond to isolated gate driver **102** (FIG. **1**). In the example in FIG. **6**, low side switch **604**.sub.2 may be operated complementary to high side switch **604**.sub.1. As such the signals from signal generator **603** provided to low side gate driver **609** may be inverted.

[0071] High side gate driver may comprise an isolator **611** coupled to an output stage **610**. Isolator **611** may correspond to isolator **108** (FIG. **1**), isolator **202** (FIG. **2**A), or isolator **402** (FIG. **4**). Output stage **610**, may correspond to output stage **110** (FIG. **1**), and comprise level shifters **614**.sub.1, and **614**.sub.2, pre-drivers **616**.sub.1 and **616**.sub.2 and a push-pull pair **612**. Push-pull pair **612** may comprise two switches, **613**.sub.1 and **613**.sub.2 coupled in series at a driving connection point **615**. In the example of FIG. **6**, switch **613**.sub.1 is illustrated as a p-type MOSFET and switch **613**.sub.2 is illustrated as an n-type MOSFET. Push-pull pair **612** may be coupled between an isolated power supply ‘Vs_sup’ and a driver reference **618**.

[0072] Half-bridge converter **602** may comprise switch **604**.sub.1 and a switch **604**.sub.2 connected in series at a switching connection point, which is also driver reference **618**. The series connection of switch **604**.sub.1 and switch **604**.sub.2 may be coupled between supply voltage, for example, as indicated by the labels ‘V+’ and ‘V−’ in FIG. **6**. A load **622** may be connected between driver reference **618** and a power reference **624**.

[0073] The signal generator **603** may be coupled to isolator **611**. Signal generator **603** may be referenced to a signal reference **620**. Isolator **611** may be coupled to level shifter **614**.sub.1, and to level shifter **614**.sub.2. Level shifter **614**.sub.1 may be coupled to pre-driver **616**.sub.1, and level shifter **614**.sub.2 may be coupled to pre-driver **616**.sub.2. Pre-driver **616**.sub.1 may be coupled to a control terminal of switch **613**.sub.1 of push-pull pair **612**. Pre-driver **616**.sub.2 may be coupled to a control terminal of switch **613**.sub.2 of push-pull pair **612**. Driving connection point **615** may be coupled to the control terminal of switch **604**.sub.1. Isolator **611**, level shifter **614**.sub.1, level shifter **614**.sub.2, pre-driver **616**.sub.1, and pre-driver **616**.sub.2 may all be referenced to driver reference **618**.

[0074] Signal generator **603** may generate a signal for controlling the state of switch **604**.sub.1 and provide the signal to isolator **611**. Similar to as described above in conjunction with FIG. **1**, **2**A, or **4**, isolator **611** may generate an output signal which may comprise at least two states, a HIGH state and a LOW state, based on the signal from signal generator **603**. For example, the voltage level of the output signal from isolator **611** may be 0V, relative to driver reference **618**, at the LOW state. For example, the voltage level of the output signal from isolator **611** may be 3.3V, 5V, 7.5V, or 12V, relative to driver reference **618**, at the HIGH state. Isolator **611** may provide the output signal therefrom to level shifter **614**.sub.1, and to level shifter **614**.sub.2. Level shifter **614**.sub.1 may shift the voltage level of the output signal to correspond to the HIGH state or LOW state relative to driving connection point **615**. Level shifter **614**.sub.2 may shift the voltage level of the output signal to correspond to the HIGH state or LOW state relative to driver reference **618**. In some cases, level shifter **614**.sub.2 may be redundant and may be omitted from output stage **610**. In some cases, level shifter **614**.sub.2 may be employed to balance the signal delay from isolator **611** to push-pull pair **612**.

[0075] Level shifter **614**.sub.1 may provide the level shifted output signal to pre-drive **616**.sub.1. Level shifter **614**.sub.2 may provide the level shifted output signal to pre-driver **616**.sub.2. Pre-drivers **616**.sub.1 and **616**.sub.2 may pre-amplify the power or voltage from the corresponding level shifter **614**.sub.1, or **614**.sub.2. Pre-drivers **616**.sub.1 and **616**.sub.2 may invert the state of the signal from the corresponding level shifter **614**.sub.1, or **614**.sub.2. For example, in cases in which the output signal from isolator is in a HIGH state, the pre-drivers **616**.sub.1 and **616**.sub.2 may invert the corresponding level shifted signal to a LOW state.

[0076] Push-pull pair **612** may employ the signals from pre-drivers **616**.sub.1 and **616**.sub.2, and amplify the power of the output signal from isolator **611**. For example, in cases in which the pre-driver signal from pre-driver **616**.sub.1 and **616**.sub.2 is in a LOW state (the output signal from isolator **611** is in a HIGH state), switch **613**.sub.1 may transition to, or maintain a conducting state, and switch **613**.sub.2 may transition to, or maintain a non-conducting state. Consequently, the voltage level at driving connection point **615** may correspond to ‘Vs_iso’, which may correspond to a HIGH state of driving connection point **615**. For example, in the HIGH state of driving connection point **615**, switch **604**.sub.1 may transition to, or maintain a conducting state. For example, in cases in which the pre-driver signal from pre-driver **616**.sub.1 and **616**.sub.2 is in a HIGH state (the output signal from isolator **611** is in a LOW state), switch **613**.sub.1 may transition to, or maintain a non-conducting state, and switch **613**.sub.2 may transition to, or maintain a conducting state. Consequently, the voltage level at driving connection point **615** may correspond to the voltage level of driver reference **618**, which may correspond to a LOW state of driving connection point **615**. For example, in the LOW state of driving connection point **615**, switch **604**.sub.1 may transition to, or maintain a non-conducting state.

[0077] In some cases, pre-drivers **616**.sub.1 and **616**.sub.2 may not be employed. However, it is noted that in such a case, high side gate driver may bean inverting driver in which the state of driving connection point **615** is complement to the state of the input signal from signal generator **603**. Furthermore, in some cases low side gate driver **609** may be similar to high side gate driver **608**.

[0078] Reference is now made to FIG. **7**, which illustrates a method for an isolated gate driver according to aspects of the disclosure herein. In step **700**, compare a level of a first voltage at a first input of a comparator, with a level of a second voltage at a second input of a comparator. The level of the first voltage and the level of the second voltage may correspond to an input signal (e.g., a PWM signal with varying duty cycle), from a signal generator. With reference to FIG. **1**, comparator **114** may compare a level of a first voltage level, from input stage **112**, at input **109**.sub.1, with a level of a second voltage, from input stage **112**, at input **109**.sub.2. With reference to FIG. **2**A, comparator **208** may compare a first voltage level, from input stage **206**, at comparator input **226**.sub.1, with a level of a second voltage from input stage **206**, at comparator input **226**.sub.2. With reference to FIG. **4**, comparator **408** may compare a first voltage level, from input stage **406**, at comparator input **426**.sub.1, with a level of a second voltage from input stage **406**, at comparator input **426**.sub.2.

[0079] In step **702**, select a feedback voltage level, relative to a reference, based on the comparison between the level of the first voltage and the level of the second voltage. With reference to FIG. **1**, feedback circuit **116** may select a feedback voltage level, relative to reference, based on the comparison, by comparator **114**, between the level of the first voltage at comparator input **109**.sub.1 and the level of the second voltage at comparator input **109**.sub.2. With reference to FIG. **2**A, controller **218** may generate a control signal for voltage levels generator **216**, based on the output signal from comparator **208**. Voltage levels generator **216** generates V_1 (e.g., as described herein above in conjunction with FIGS. **3**A-**3**D), based on a control signal from controller **218**. With reference to FIG. **4**, controller **418** may generate a control signal for voltage levels generator **416**, based on the output signal from comparator **408**. Voltage levels generator **416** generates V_1 (e.g., as described herein above in conjunction with FIGS. **3**A-**3**D), based on a control signal from controller **418**.

[0080] In step **704**, provide the selected feedback voltage level to the first input of a comparator. With reference to FIG. **1**, feedback circuit **116** applies the selected feedback voltage to input stage **112** (e.g., to comparator input **109**.sub.1). With reference to FIG. **2**A, voltage levels generator **216** applies V_1 to comparator input **226**.sub.1. With reference to FIG. **4**, voltage levels generator **416** applies V_1 to comparator input **426**.sub.1.

[0081] As mentioned above in conjunction with FIGS. **4** and **5**, a sensor may sense the voltage between a reference of a gate driver according to the disclosure herein, and either a power reference or a signal reference or both. A feedback circuit may set the voltage at the inputs of the comparator based on this measurement or measurements. Reference is now made to FIG. **8**, which illustrates a method for an isolated gate driver according to the disclosure herein. In step **800**, measure, by sensor, a voltage between a first reference and a second reference. For example, with reference to FIGS. **4**, sensors **411** measures a voltage between driver reference **420**, and signal reference **422**. For example, with reference to FIGS. **5**, sensors **508** measures a voltage between driver reference **518**, and reference **526**.

[0082] In step **802**, determine, based on the measured voltage between the first reference and the second reference, a first feedback voltage level and a second feedback voltage level. For example, controller **418** may control voltage levels generator **416** to set a voltage at comparator input **426**.sub.2 to be one of two voltage levels relative to Vref (e.g., Vcm is set to one of two levels, Vcm**1**, or Vcm**2**, relative to Vref). Controller **418** may control voltage levels generator **416** to set a differential voltage at comparator input **426**.sub.1 to be one of two voltage levels relative to Vref (e.g., V d above Vcm**1** or Vcm**2**, or V d below Vcm**1** or Vcm**2**).

[0083] In step **804**, provide the determined first feedback voltage level to a first input of a comparator and provide the determined second feedback voltage level to a second input of a comparator. For example, with reference to FIGS. **4** and **3**A, controller **418** may control voltage levels generator **300** to generate V_1 and V_2 based on a measurement from sensor **411** of the voltage between reference **420** and signal reference **422**.

[0084] As mentioned above, in some cases, an isolator and gate driver according to aspects of the disclosure herein may be implemented on an Integrated Circuit (IC), employing, for example, CMOS techniques and On-Chip metal connections. For example, capacitors C**1**, C**2**, C**3** and C**4** (FIG. **2**A, or **4**) may be implemented by the metals employed in the IC. Reference is now made to FIGS. **9**A and **9**B which illustrate examples of capacitors, generally referenced **900** and **950** respectively, implemented using metal in an IC. In FIG. **9**A, IC capacitor **900** may comprise a first electrode **902** and a second electrode **904**. Second electrode **904** is isolated from first electrode **902** (e.g., by a dielectric material such as silicon dioxide or silicon carbide). In the example of FIG. **9**A, first electrode **902** may comprise three metal layers **906**, **908**, and **910** connected there between by via's such as via **912**. Second electrode **904** may comprise two metal layers **908** and **910** connected by a via. The capacitance of capacitor **900** may be selected by selecting a horizontal spacing **914** between first electrode **902** and second electrode **904**.

[0085] In FIG. **9**B, IC capacitor **950** may comprise a first electrode **952** and a second electrode **954**. Second electrode **954** is isolated from first electrode **942** (e.g., by a dielectric material such as silicon dioxide or silicon carbide). In the example of FIG. **9**B, first electrode **942** may comprise three metal layers **956**, **958**, and **960** connected there between by vias, such as via **962**. In the example of FIG. **9**B, second electrode **904** may comprise one metal layer **960**. The capacitance of capacitor **950** may be selected by omitting metal layers, thus increasing the vertical spacing **964** between first electrode **952** and second electrode **954**.

[0086] The AC couplers of the isolated gate drivers described herein above in conjunction with FIGS. **2**A, and **4**, comprised a capacitive divider. However, an isolator according to the disclosure herein may be employed with other types of AC couplers. Reference is now made to FIGS. **10**A, **10**B, **10**C and **10**D, which illustrate various types of AC couplers, generally referenced **1000**, **1010**, **1020**, and **1030** respectively, in accordance with aspects of the disclosure herein. Each one of AC couplers **1000**, **1010**, **1020**, or **1030** may be employed as one of AC coupler **212** or AC coupler **214** of FIG. **2**A. Each one of AC couplers **1000**, **1010**, **1020**, or **1030** may be employed as one of AC coupler **412** or AC coupler **414** of FIG. **4**.

[0087] With reference to FIG. **10**A, AC coupler **1000** may comprise an impedance divider, which may comprise two impedances **1001**.sub.1 and **1001**.sub.2 connected in series between an isolated supply voltage, 'Vs_iso', and a reference **1006**. Impedance **1001**.sub.1 may comprise a capacitor **1002**.sub.1 coupled in parallel with a resistor **10041**. Impedance **1001**.sub.2 may comprise a capacitor **1002**.sub.2 coupled in parallel with a resistor **1004**.sub.2.

[0088] With reference to FIG. **10**B, AC coupler **1010** may comprise a transformer **1012**. A primary side of the transformer may be coupled between an isolated supply voltage, 'Vs_iso', and a reference **1014**. The secondary side of transformer **1012** may be coupled between output **1016**.sub.1 and **1016**.sub.2. Transformer **1012** may comprise a parasitic capacitance **1010** between the primary and secondary windings of transformer **1012**.

[0089] With reference to FIG. **10**C, AC coupler **1020** may comprise a resistive divider, which may comprise two resistors **1022**.sub.1 and **1022**.sub.2 connected in series between an isolated supply voltage, 'Vs_iso', and a reference **1024**. The resistive divider may comprise a parasitic capacitance **1026**.

[0090] With reference to FIG. **10**D, AC coupler **1030** may comprise a capacitive divider, which may comprise two capacitors **1032**.sub.1 and **1032**.sub.2 connected in series between an isolated supply voltage, 'Vs_iso', and a reference **1034**. The capacitive divider may comprise a parasitic capacitance **1026**.

[0091] Reference is now made to FIGS. **11**A-**11**F, which illustrate examples of waveforms according to aspects of the disclosure herein. In FIGS. **11**A-**11**F, 'Vp' relates to a voltage at first input of a comparator (e.g., first input **109**.sub.1—FIG. **1**, first input **226**.sub.1—FIG. **2**A, first input **426**.sub.1—FIG. **4**). 'Vn' relates to a voltage at a second input of the comparator (e.g., second input **109**.sub.2—FIG. **1**, second input **226**.sub.2—FIG. **2**A, second input **426**.sub.2—FIG. **4**). 'Vref' relates to a voltage at a driver reference (e.g., driver reference **118**—FIG. **1**, driver reference **220**—FIG. **2**A, driver reference **420**—FIG. **4**, driver reference **518**—FIG. **5**, driver reference **618**—FIG. **6**). In the description of FIGS. **11**A-**11**F, reference is also made to FIG. **2**A for the sake of explanation. However, it is understood that the illustrations in FIGS. **11**A-**11**F relate to an isolated gate driver, as described in any of the figures of the disclosure herein.

[0092] FIGS. **11**A-**11**F illustrate an example in which no feedback is used between comparator output **228** and first input **226**.sub.1 of comparator **208**. FIGS. **11**A-**11**C illustrate an example in which a duty cycle, D, of a PWM input signal is 0.3 (D=0.3). FIGS. **11**D-**11**F illustrate an example in which the duty cycle, D, of a PWM input signal is 0.7 (D=0.7). In the examples of FIGS. **11**A-**11**F, capacitors C**2**, and C**3** of the AC couplers **212** and **214** respectively, have been pre-charged to correspond to a low state of the input PWM signal, and thus, a low state at the output of comparator **208**. For example, C**3** may be pre-charged to (Vs_iso−Vref)/2, and C**2** may be pre-charged to (Vs_iso−Vref−Viso_pwm)/2. Viso_pwm corresponds to the change in the voltage level over C**2**, in cases in which the PWM signal changes states. For example, Viso_pwm may depend on the capacitance values of C**1** and C**2** (e.g., C**1** and C**2** may form a capacitance divider). For example, in cases in which Vs_iso-Vref=5V and Viso_pwm=0.05V, C**2** may be pre-charged to 2.475V and C**3** may be pre-charged to 2.5V. Therefore, the initial voltage at the first input **226**.sub.1 of comparator **208** may be 2.475V, relative to Vref, and the initial voltage at second input **226**.sub.2 of comparator

208 may be 2.5V, relative to Vref.

[0093] FIG. **11**A illustrates an example of the voltage difference, Vp−Vn, between the voltage, Vp, at first input **226**.sub.1 of comparator **208**, and the voltage, Vn, at second input **226**.sub.2 of comparator **208**, in cases in which D=0.3. FIG. **11**B illustrates an example of the voltage difference, Vp−Vref, between the voltage at first input **226**.sub.1, Vp, and the voltage, Vref, at driver reference **220**, in cases in which D=0.3. FIG. **11**C illustrates an example of the voltage difference, Vn−Vref, between the voltage at second input **226**.sub.2, Vn, and Vref, in cases in which D=0.3.

[0094] As illustrated in FIG. **11**A, Vp−Vn may initially exceed the upper and lower thresholds of the comparator (e.g., +Vth, and −Vth in FIG. **11**A). However, as time progresses, leakage of capacitor C**2**, or C**3**, or both, which may result in a modulation of Vref due to the duty cycle, D, of the PWM signal being lower than 0.5, and may cause Vp−Vn, to rise relative to Vref. Vp−Vn, may rise to a level in which Vp−Vn does not fall below the negative threshold voltage, −Vth, of comparator **208**. In such a case, comparator **208** may latch to a high output state. The rise in the voltage level Vp−Vn may be regarded as the modulation of Vref (e.g., Vref reduces in cases in which D<0.5). As illustrate in FIGS. **11**B and **11**C, initially, Vp−Vref and Vn−Vref respectively, may be between the voltage, Vref, at driver reference **220**, and the isolated supply voltage, Vs_iso. However, as time progresses, leakage of capacitor C**2**, or C**3**, or both, may cause Vp−Vref, Vn−Vref, or both, to fall below Vref.

[0095] FIG. **11**D illustrates an example of the voltage difference, Vp−Vn, between the voltage, Vp, at first input **226**.sub.1 of comparator **208**, and the voltage, Vn, at second input **226**.sub.2 of comparator **208**, in cases in which D=0.7. FIG. **11**E illustrates the voltage difference, Vp−Vref, between the voltage at first input **226**.sub.1, Vp, and the voltage, Vref, at driver reference **220**, in cases in which D=0.7. FIG. **11**F illustrates an example of the voltage difference, Vn−Vref, between the voltage at second input **226**.sub.2, Vn, and Vref, in cases in which D=0.7.

[0096] As illustrate in FIG. **11**D, Vp−Vn may initially exceed the upper and lower thresholds of the comparator (e.g., +Vth, and −Vth in FIG. **11**D). H ow ever, as time progresses, leakage of capacitor C**2**, or C**3**, or both, which may result in a modulation of Vref due to the duty cycle, D, of the PWM signal being higher than 0.5, and may cause Vp−Vn, to fall relative to V.sub.ref. Vp−Vn, may fall to a level in which Vp−Vn does not rise above the positive threshold voltage, +Vth, of comparator **208**. In such a case, comparator **208** may latch to a low output state. The reduction in the voltage level Vp−Vn may be regarded as the modulation of Vref (e.g., Vref increases in cases in which D>0.5). As illustrate in FIGS. **11**E and **11**F, initially, Vp−Vref and Vn−Vref respectively, may be between the voltage at driver reference **220** and the isolated supply voltage, Vs_iso. However, as time progresses, leakage of capacitor C**2**, or C**3**, or both, may cause Vp−Vref, Vn−Vref, or both, to fall below Vref.

[0097] Reference is now made to FIGS. **12**A-**12**L, which illustrate examples of waveforms according to aspects of the disclosure herein. In FIGS. **12**A-**12**L, 'Vp' relates to a voltage at a first input of a comparator (e.g., first input **109**.sub.1—FIG. **1**, first input **226**.sub.1—FIG. **2**A, first input **426**.sub.1—FIG. **4**). 'V.sub.n' relates to a voltage a second input of at a comparator (e.g., second input **109**.sub.2—FIG. **1**, second input **226**.sub.2—FIG. **2**A, second input **426**.sub.2—FIG. **4**). 'Vref' relates to a voltage at a driver reference (e.g., driver reference **118**—FIG. **1**, driver reference **220**—FIG. **2**A, driver reference **420**—FIG. **4**, driver reference node **518**—FIG. **5**, driver reference node **618**—FIG. **6**).

[0098] FIGS. **12**A-**12**F illustrate examples in which feedback, (e.g., a feedback circuit as described above in conjunction with FIG. **1**, **2**A, **3**A-**3**D, or **4**) is used between the output and input of the comparator. As mentioned above in conjunction with FIGS. **1**, **2**A, and **4**, the feedback may be used to control the voltage levels at the inputs of the comparator, such that a change in voltage level of the input signal may result in a change in voltage level in the output of the comparator (e.g., reducing the probability of error due to varying duty cycles of the input signal or leakage of the capacitors). FIGS. **12**A-**12**C illustrate a case in which a duty cycle, D, of a PWM input signal is 0.3

(D=0.3). FIGS. **12**D-**12**F illustrate a case in which the duty cycle, D, of a PWM input signal is 0.7 (D=0.7). FIGS. **12**G-**12**I illustrate a case in which the duty cycle, D, of a PWM input signal is 0.95 (D=0.95), and FIGS. **12**J-**12**L illustrate a case in which the duty cycle, D, of a PWM input signal is 0.05 (D=0.05). As illustrated in FIG. **12**A, **12**D, **12**G, or **12**J, in cases in which a feedback circuit as described above is used, Vp−Vn rises above +Vth or falls below −Vth regardless of the duty cycle. As illustrated in FIG. **12**B, **12**E, **12**H, or **12**K, in cases in which a feedback circuit as described above is used, Vp−Vref remains between Vref and Vs_iso regardless of the duty cycle. As illustrated in FIG. **12**C, **12**F, **12**I, or **12**L, in cases in which a feedback circuit as described above is used, Vn−Vref also remains between Vref and Vs_iso regardless of the duty cycle.

[0099] In view of FIGS. **12**A-**12**K, a feedback circuit according to the disclosure herein (e.g., feedback circuit **116**—FIG. **1**, feedback circuit **116**—FIG. **1**, feedback circuit **216**—FIG. **2**A, feedback circuit **416**—FIG. **4**) may be configured to control the voltage levels at the inputs of the comparator (e.g., inputs **109**.sub.1 and **109**.sub.2 of comparator **114**—FIG. **1**, inputs **226**.sub.1 and **226**.sub.2 of comparator **208**, inputs **426**.sub.1 and **426**.sub.2 of comparator **408**—FIG. **1**) to be within determined values (e.g., to be between a reference voltage level, V_ref, and a supply voltage level of the circuit Vs_iso). A feedback circuit according to the disclosure herein may be configured to control a difference between the voltage levels at the inputs of the comparator to be above or below a threshold or thresholds levels of the comparator (e.g., +Vth, and −Vth). A feedback circuit according to the disclosure herein may be configured to control a midpoint of a difference between the voltage levels at the inputs of the comparator to be within predetermined values (e.g., control the difference midpoint to be centered about a value, within tolerances). For example, the feedback circuit may control a midpoint of a difference between the voltage levels at the inputs of the comparator to be about zero within determined tolerances. As further explained herein below in conjunction with FIGS. **13**A-**13**E, a feedback circuit according to the disclosure herein may be configured to control the average of a difference between the voltage levels at the inputs of the comparator to be within a determined value (e.g., regardless of the duty cycle of the input signal).

[0100] Reference is now made to FIGS. **13**A-**13**E, which illustrate timing diagrams and models in accordance with aspects of the disclosure herein. In the description of FIGS. **13**A-**13**D which follows, Vp may represent an instantaneous voltage at a first input of a comparator (e.g., first input **226**.sub.1 of comparator **208**—FIG. **2**A), and V.sub.n may represent an instantaneous voltage at a second input of the comparator (e.g., second input **226**.sub.2 of comparator **208**—FIG. **2**A). <Vp> may represent an average voltage at the first input of the comparator, and <Vn> may represent an average voltage at a second input of the comparator. <Vp−Vn> may represent the average of the difference between Vp and V n.

[0101] In the example of FIGS. **13**A-**13**D, V.sub.p transitions between a first voltage level, V**1**, and a second voltage level, V**2** (e.g., a pulsed signal as illustrated in FIG. **13**A), and Vn remains constant. The signal at the first input (e.g., a pulsed PWM signal) may average over capacitor C**2** (e.g., FIG. **2**A, or FIG. **4**) at an average value of <Vp>. In such a case, the area S**1**, should equal the area S**2** in FIG. **13**A. This condition may be expressed by the following equations:

[00002] $\mathrm{Ts} * D * \quad = \mathrm{Ts} * (1 - D) * \qquad (3)$ where $\quad + \quad = \mathrm{Va} \quad (4)$

[0102] From equations (3) and (4) and FIG. **13**A, the following equations may be written:

[00003] $\quad = D * \mathrm{Va} \quad (5) \qquad = (1 - D) * \mathrm{Va} \quad (6) \quad V1 = \langle \mathrm{Vp} \rangle - \qquad (7)$

$V2 = \langle \mathrm{Vp} \rangle + \qquad (8)$

where V**1** and V**2** are the voltage levels of Vp, relative to a reference. In cases in which Vp−Vn toggles between a first voltage level, V**1**, and a second voltage level, V**2**, it may be required that:

[00004] $\frac{\tilde{V}_1 + \tilde{V}_2}{2} = 0 \quad (9)$

{tilde over (V)}**1** and {tilde over (V)}**2** may be written as follows:

[00005] $\tilde{V}_1 = V1 - \langle \mathrm{Vn} \rangle \quad (10) \quad \tilde{V}_2 = V2 - \langle \mathrm{Vn} \rangle \quad (11)$

Using equations (5)-(8), and (10)-(11) with equation (9), may result in the following:

[00006] $\langle Vp \rangle - \langle Vn \rangle = (Va/2) * (2D - 1)$ (12)

[0103] Equation 12 relates to the requirement for maintain <Vp−Vn>=0 (e.g., centered around Vref as illustrated in FIG. **12**A, **12**D, **12**G, or **12**J). Referring to FIGS. **13**C and **13**D, a model of a PWM switch may be expressed as follows:

[00007] $Vout = D * Vx + (1 - D) * Vy$ (13)

Vx and Vy may be expressed as a difference voltage, ΔV, above or below a common voltage respectively, as follows:

[00008] $Vx = Vcom + V$ (14) $Vy = Vcom - V$ (15)

Using equations (14) and (15) with Equation (13), it may be shown that:

[00009] $Vout = Vcom + V * (2D - 1)$ (16)

If we let <Vn>=Vcom, <Vp>=Vcom+ΔV*(2D−1), and ΔV=Va/2, then the requirement of Equation 12 may be satisfied using a PWM switch (e.g., a feedback circuit producing a feedback voltage modulated based on a PWM signal). This condition may be implemented, for example, with voltage generators **320** or **330** described above in conjunction with FIGS. **3**C and **3**D, where V**1**−V**2**=Va/2, and Va=Vs_iso, and switch **324** or **334** being modulated by a PWM signal (e.g., from an output of a comparator such as comparator **114**, **210** or **410** in FIG. **1**, **2**A or **4**).

[0104] A similar derivation may be used in cases in which V n also transitions between a high and low state (e.g., as depicted in FIG. **13**E) employing the following equations:

[00010] $V3 = \langle Vn \rangle +$ (17) $V4 = \langle Vp \rangle -$ (18) $\tilde{V}_1 = V1 - V4$ (19)

$\tilde{V}_2 = V2 - V3$ (20)

which may result in the following:

[00011] $\langle Vp \rangle - \langle Vn \rangle = Va * (2D - 1)$ (21)

[0105] In equation (21), ΔV may equal Va. Based on a comparison between Equation (21) with Equation (12), the input signal into the comparator, <Vp>−<Vn>, is larger by a factor of two in cases where Vn also transitions between a high and low state. This may result in an increased signal-to-noise ratio (SNR) of the driving signal, which may result in a lower probability of error.

[0106] An advantage of an isolated gate driver according to aspects of the disclosure herein may be that isolated gate driver **102** may be coupled directly to the signal generator, without intermediate circuitry (e.g., inverters, flip flops, encoders, biasing circuits, oscillators, rectifiers and the like). This may provide various additional advantages. For example, in some cases, the capacitances of C**1**, C**2**, C**3**, or C**4** may deviate from the designed values (e.g., due to imperfections in the manufacturing process and the like). To overcome these deviations, an isolated gate driver according to aspects of the disclosure herein may be calibrated. For example, and with reference to FIG. **2**A, one or more of capacitors C**1**, C**2**, C**3**, or C**4** may be a varying capacitor, with a capacitance that may be controlled. Predetermined input signals, each having a corresponding different voltage level, may be received by the input stage **206** at terminals **224**.sub.1 and **224**.sub.2. These predetermined input signals, with the corresponding varying voltage levels, may have corresponding expected outputs (e.g., high level signal, or low level signal) from gate driver **200**. By measuring the outputs resulting from the predetermined input signals, and comparing the measured outputs with the expected outputs, a deviation of the state of the output from comparator **208**, relative to the expected output may be determined. Consequently, a deviation of the input into comparator **208**, relative to the expected input (e.g., derived from the predetermined signals and the designed values of capacitors C**1**, C**2**, C**3**, and C**4**) may be determined. In cases in which such a deviation is determined, the capacitance of the varying capacitor may be adjusted to minimize these deviations.

[0107] Another advantage of a gate driver of the disclosed technique may relate to quality control.

Similar to as described above regarding calibration, predetermined input signals, each having a corresponding different voltage level, may be received by the input stage **206** at terminals **224**.sub.1 and **224**.sub.2. These predetermined input signals, with predetermined varying voltage levels, may have corresponding expected outputs (e.g., high level signal, or low level signal) from gate driver **200**. By measuring the outputs resulting from the predetermined input signals, and comparing the measured outputs with the expected outputs, a determination may be made at what voltage levels the tested gate driver fails, and the gate driver may be rated accordingly. For example, a gate driver that failed at low voltage levels may be rated higher than a gate driver that failed at high voltage levels.
[0108] One or more aspects of the disclosure may be embodied in computer-usable data and computer-executable instructions, such as in one or more program modules, executed by one or more computers or other devices. Generally, program modules include routines, programs, objects, components, data structures, etc. that perform particular tasks or implement particular abstract data types when executed by a processor in a computer or other device. The computer executable instructions may be stored on a computer readable medium such as a hard disk, optical disk, removable storage media, solid state memory, RAM, etc. As will be appreciated by one of skill in the art, the functionality of the program modules may be combined or distributed as desired in various embodiments. In addition, the functionality may be embodied in whole or in part in firmware or hardware equivalents such as integrated circuits, field programmable gate arrays (FPGA), and the like. Particular data structures may be used to more effectively implement one or more aspects of the disclosure, and such data structures are contemplated within the scope of computer executable instructions and computer-usable data described herein.
[0109] Although the subject matter has been described in language specific to structural features and/or methodological acts, it is to be understood that the subject matter defined in the appended claims is not necessarily limited to the specific features or acts described above. Rather, the specific features and acts described above are disclosed as example forms of implementing the claims.
[0110] Various aspects will be highlighted in a set of numbered clauses herein. These aspects are not to be interpreted as being limiting of the invention or inventive concept, but are provided merely to highlight some features as described herein, without suggesting a particular order of importance or relevancy of such aspects.

Claims

1. A gate driver comprising: a comparator comprising a first input, a second input, and an output, wherein the first input and the second input are configured to receive an input signal, the input signal having an input voltage corresponding to one of a first state and a second state, wherein the comparator is configured to provide an output signal at the output based on a comparison between a level of a first voltage at the first input, and a level of a second voltage at the second input, the level of the first voltage and the level of the second voltage corresponding to the input signal, and the output signal comprises one of the first state and the second state; a sensor configured to measure a voltage level between a first reference and a second reference; and a feedback circuit, coupled to the output of the comparator and to the sensor, wherein the feedback circuit is configured to receive the output signal, and provide, based on the output signal and based on the measured voltage level between the first reference and the second reference, a first feedback voltage to the first input, and a second feedback voltage to the second input, to control the level of the first voltage and the level of the second voltage, such that a change in a state of the input signal results in a change in a state of the output from the comparator.
2. The gate driver of claim 1, wherein the feedback circuit is further configured to receive the output signal and set, based on the state of the output signal and the measured voltage level, the level of the first feedback voltage to one of at least two voltage levels relative to the first reference,

and the level of the second feedback voltage to one of at least two other voltage levels relative to the first reference.

3. The gate driver of claim 2, wherein the feedback circuit comprises a voltage levels generator configured to generate the at least two voltage levels, and the at least two other voltage levels.

4. The gate driver of claim 3, wherein the voltage levels generator comprises a first impedance and a second impedance, and wherein the voltage levels generator is configured to generate the first feedback voltage and provide the first feedback voltage to the first input via the first impedance, and the voltage levels generator is configured to generate the second feedback voltage and provide the second feedback voltage to the second input via the second impedance.

5. The gate driver of claim 3, wherein the feedback circuit further comprises a controller, coupled to the output of the comparator, and to the voltage levels generator, wherein the controller is configured to provide a control signal based on the output signal, and wherein, based on the control signal, the voltage levels generator is configured to provide the first feedback voltage to the first input and the second feedback voltage to the second input.

6. The gate driver of claim 1, further comprising an input stage comprising a third input, a fourth input, a first Alternating Current (AC) coupler, and a second AC coupler, wherein the first AC coupler is coupled between the third input and the first input of the comparator, and the second AC coupler is coupled between the fourth input and the second input of the comparator, wherein the input stage is configured to receive, at the third input and the fourth input, the input signal, and provide the input signal to the first input and the second input.

7. The gate driver of claim 6, wherein the input stage is configured to provide Direct Current (DC) isolation between the first reference and the second reference.

8. The gate driver of claim 6, wherein the first input and the second input are referenced to the first reference, and wherein the third input and the fourth input are referenced to the second reference.

9. The gate driver according to claim 6, wherein the first AC coupler comprises a first capacitor coupled to the first input and to the third input, and a second capacitor coupled between the third input and the first reference, and the second AC coupler comprises a third capacitor coupled to the second input and to the fourth input, and a fourth capacitor coupled between the fourth input and the first reference.

10. The gate driver of claim 1, wherein the first reference corresponds to a switching connection point, and wherein the second reference corresponds to one of: a power reference; or a signal reference.

11. The gate driver of claim 1, wherein the output signal is configured to control a first switch, coupled in series with a second switch at a switching connection point, wherein the switching connection point corresponds to the first reference.

12. A method comprising the steps of: comparing, by a comparator, a level of a first voltage at a first input of the comparator, and a level of a second voltage at a second input of the comparator, wherein the level of the first voltage and the level of the second voltage correspond to an input signal; providing by the comparator, an output signal at an output of the comparator, based on a comparison between the level of the first voltage at the first input and the level of the second voltage at the second input, the output signal comprises one of a first state and a second state; measuring, by a sensor, a voltage level between a first reference and a second reference; determining, by a feedback circuit, based on the comparing and based on the measuring, a first feedback voltage and a second feedback voltage; and providing, by the feedback circuit, the first feedback voltage to the first input and the second feedback voltage to the second input, wherein the level of the first feedback voltage and the level of the second feedback voltage controls the level of the first voltage and the level of the second voltage, such that a change in a state of an input signal results in a change in a state of an output signal from the comparator.

13. The method of claim 12, further comprising: receiving, by the feedback circuit, the output signal; and setting, by the feedback circuit, based on the state of the output signal and based on the measuring, the level of the first feedback voltage to one of at least two voltage levels relative to the first reference, and the level of the second feedback voltage to one of at least two other voltage levels relative to the first reference.

14. The method of claim 13, wherein the setting comprises generating by the feedback circuit, the first feedback voltage and the second feedback voltage, wherein the providing comprises providing the first feedback voltage to the first input via a first impedance and providing the second feedback voltage to the second input via a second impedance.

15. The method of claim 13, wherein the setting comprises detecting the state of the output signal.

16. The method of claim 13, wherein the setting comprises providing, by a controller, a control signal, and wherein, based on the control signal, the feedback circuit provides the first feedback voltage to the first input and the second feedback voltage to the second input.

17. The method of claim 12, further comprising receiving, from a signal generator, at a third input and a fourth input, the input signal having an input voltage that corresponds to one of the first state and the second state, wherein the first input of the comparator is Direct Current (DC) isolated, by a first Alternating Current (AC) coupler, from the third input, wherein the second input of the comparator is DC isolated, by a second AC coupler, from the fourth input.

18. The method of claim 17, wherein the first input and the second input are referenced to the first reference, and the third input and the fourth input are referenced to the second reference.

19. The method of claim 12, wherein the first reference corresponds to a switching connection point, and the second reference corresponds to one of: a power reference; or a signal reference.

20. The method of claim 12, further comprising controlling, using the output signal, a first switch, coupled in series with a second switch at a switching connection point, wherein the switching connection point corresponds to the second reference.
