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Inventor(s) KIM; Sangkyu et al.

MICRO DISPLAY DEVICE

Abstract

A micro display device can include a pixel unit disposed on a display panel, the pixel unit including a red subpixel, a green subpixel and a blue subpixel, a first power source voltage line including a first line connected between a first power source voltage supply terminal and the red subpixel, a second line connected between the first power source voltage supply terminal and the green subpixel, and a third line connected between the first power source voltage supply terminal and the blue subpixel, and a first resistance unit connected to at least a portion of the first power source voltage line.

Inventors: **KIM; Sangkyu (Paju-si, KR), YUN; JaeKyeong (Paju-si, KR)**

Applicant: **LG DISPLAY CO., LTD.** (Seoul, KR)

Family ID: **1000008295291**

Assignee: **LG DISPLAY CO., LTD. (Seoul, KR)**

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to Korean Patent Application No. 10-2024-0022056, filed in the Republic of Korea, on Feb. 15, 2024, the entirety of which is hereby incorporated by reference into the present application for all purposes as if fully set forth herein.

BACKGROUND

Field

[0002] The disclosure relates to a micro display device.

Description of Related Art

[0003] The display device includes a display panel including a plurality of subpixels, and various driving circuits such as a source driving circuit and a gate driving circuit for driving the display panel.

[0004] In the display panel of the conventional display device, transistors, various electrodes, various signal lines, and the like are formed on a glass substrate, and the driving circuits that can be implemented as integrated circuits are mounted on a printed circuit and are electrically connected to the display panel through the printed circuit.

[0005] This conventional type of structure is suitable for large display devices, but it is not suitable for small display devices. For example, there are disadvantages when a glass substrate is used in a small display device.

[0006] Therefore, many types of electronic devices that use a small display device are nowadays emerging, such as virtual reality devices, augmented reality devices, and the like.
[0007] However, a need exists for a small display device that has excellent display performance or a structure suitable for small electronic devices, such as virtual reality devices or augmented reality devices. Also, a needs exists for a display device that can improve a color luminance ratio imbalance.

SUMMARY OF THE DISCLOSURE

[0008] To address the foregoing issues, the disclosure is directed to a micro display device capable of addressing the above noted issues, including addressing color luminance ratio imbalance of micro displays.
[0009] A display device according to an embodiment of the disclosure can include a pixel unit disposed on a display panel and including a red subpixel, a green subpixel, and a blue subpixel, first power source voltage lines connected to a first power source voltage supply terminal to supply a first power source voltage to each of the red subpixel, the green subpixel, and the blue subpixel, and a first resistance unit commonly connected to the first power source voltage lines.
[0010] Although the disclosure has been shown and described in connection with example embodiments thereof, it will be appreciated by one of ordinary skill in the art that various changes or modifications can be made thereto without departing from the scope of the disclosure.
[0011] According to an embodiment of the disclosure, it is possible to address color luminance ratio imbalance by reducing the current flowing through a low-voltage driving voltage line when emitting white light by simultaneously driving the red subpixel R, green subpixel G, and blue subpixel B in the micro display.
[0012] According to an embodiment of the disclosure, it is possible to address luminance ratio difference between pixels emitting different colors of light by having a resistor in a micro display.
[0013] In other words, it is possible to reduce the difference between the white emission luminance and the sum of the respective emission luminances of the red subpixel, green subpixel, and blue subpixel.
[0014] The effects of the disclosure are not limited thereto, and the disclosure encompass other various effects.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The above and other objects, features, and advantages of the disclosure will be more clearly understood from the following detailed description, taken in conjunction with the accompanying drawings, in which:
[0016] FIG. **1** is a view schematically illustrating a micro display device according to embodiments of the present disclosure;
[0017] FIG. **2** is a view illustrating two zones of a silicon substrate of a micro display device according to an embodiment of the present disclosure;
[0018] FIG. **3** is a view illustrating a micro display device and a silicon wafer according to an embodiment of the present disclosure;
[0019] FIG. **4** is a plan view schematically illustrating a switch configuration of a micro display device according to an embodiment of the present disclosure;
[0020] FIG. **5** is an example view illustrating a subpixel structure of a micro display device according to an embodiment of the present disclosure;
[0021] FIG. **6** is another example view illustrating a subpixel structure of a micro display device according to an embodiment of the present disclosure;
[0022] FIG. **7** is an example view illustrating a cause of occurrence of a difference between a W emission luminance and the sum of R, G, and emission luminances;
[0023] FIGS. **8** and **9** are equivalent circuit diagrams illustrating examples of a partial pixel structure of a micro display device according to embodiments of the present disclosure;
[0024] FIG. **10** is an example circuit diagram illustrating driving for dropping a luminance increase that occurs according to a charging voltage of a storage capacitor during white emission and high-current driving according to an embodiment of the present disclosure; and
[0025] FIG. **11** illustrates a graph and table showing luminance comparison between per-resistance white emission of a first resistance unit and R, G, and B individual emissions according to an embodiment of the present disclosure.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0026] In the following description of examples or embodiments of the disclosure, reference will be made to the accompanying drawings in which it is shown by way of illustration specific examples or embodiments that can be implemented, and in which the same reference numerals and signs can be used to designate the same or like components even when they are shown in different accompanying drawings from one another. Further, in the following description of examples or embodiments of the disclosure, detailed descriptions of well-known functions and components incorporated herein will be omitted when it is determined that the description can make the subject matter in some embodiments of the disclosure rather unclear. The terms such as “including,” “having,” “containing,” “constituting” “make up of,” and “formed of” used herein are generally intended to allow other components to be added unless the terms are used with the term “only.” As used herein, singular forms are intended to include plural forms unless the context clearly indicates otherwise.
[0027] Terms, such as “first,” “second,” “A,” “B,” “(A),” or “(B)” can be used herein to describe elements of the disclosure. Each of these terms is not used to define essence, order, sequence, or number of elements etc., but is used merely to distinguish the corresponding element from other elements.
[0028] When it is mentioned that a first element “is connected or coupled to,” “contacts or overlaps” etc. a second element, it should be interpreted that, not only can the first element “be directly connected or coupled to” or “directly contact or overlap” the second element, but a third element can also be “interposed” between the first and second elements, or the first and second elements can “be connected or coupled to,” “contact or overlap,” etc. each other via a fourth element. Here, the second element can be included in at least one of two or more elements that “are connected or coupled to,” “contact or overlap,” etc. each other.

[0029] When time relative terms, such as “after,” “subsequent to,” “next,” “before,” and the like, are used to describe processes or operations of elements or configurations, or flows or steps in operating, processing, manufacturing methods, these terms can be used to describe non-consecutive or non-sequential processes or operations unless the term “directly” or “immediately” is used together.
[0030] In addition, when any dimensions, relative sizes etc. are mentioned, it should be considered that numerical values for an elements or features, or corresponding information (e.g., level, range, etc.) include a tolerance or error range that can be caused by various factors (e.g., process factors, internal or external impact, noise, etc.) even when a relevant description is not specified. Further, the term “can” fully encompasses all the meanings of the term “may” and vice versa.
[0031] Hereinafter, various embodiments of the disclosure are described in detail with reference to the accompanying drawings.
[0032] FIG. **1** is a view schematically illustrating a micro display device **1** according to the present embodiments.
[0033] Referring to FIG. **1**, a micro display device **1** according to the present embodiments can have a backplane structure in which a pixel array **100** and various driving circuits are configured on a silicon substrate **10**.
[0034] As used herein, the term “micro” can mean that the size of the micro display device **1** is small, or even if the size of the micro display device **1** is not small, it can mean that a manufacturing process is finely performed to produce it.
[0035] FIG. **2** is a view illustrating two zones of a silicon substrate **10** of a micro display device **1** according to the present embodiments.
[0036] The silicon substrate **10** can be of a p-type or an n-type. In the disclosure, “p” means hole, and “n” means electron.
[0037] The silicon substrate **10** can include a pixel array zone PAZ and a circuit zone CZ.
[0038] Accordingly, the micro display device **1** according to the present embodiments can include the pixel array **100** including the plurality of subpixels SP arranged in the pixel array zone PAZ of the silicon substrate **10** and driving circuits arranged in the circuit zone CZ of the silicon substrate **10**.
[0039] The circuit zone CZ of the silicon substrate **10** can be positioned around the pixel array zone PAZ of the silicon substrate **10**.
[0040] A plurality of subpixels SP, as well as signal lines for supplying various signals and voltages to the plurality of subpixels SP, can be arranged in the pixel array zone PAZ of the silicon substrate **10**.
[0041] The signal lines can include data lines for transferring a data voltage corresponding to an image signal and gate lines for transferring a scan signal (gate signal).
[0042] Further, the signal lines disposed in the pixel array zone PAZ of the silicon substrate **10** can further include a driving voltage line for transferring a driving voltage, and in some situations, can further include a sense line for transferring a reference voltage or sensing a voltage.
[0043] Signal lines disposed in the pixel array zone PAZ of the silicon substrate **10** can be electrically connected to driving circuits disposed in the circuit zone CZ of the silicon substrate **10**.
[0044] The driving circuits disposed in the circuit zone CZ of the silicon substrate **10** can include a source driving circuit **110** for driving data lines, a gate driving circuit **120** for driving gate lines, and a control circuit **130** for controlling operations of the source driving circuit **110** and the gate driving circuit **120**.
[0045] Here, the source driving circuit **110** can also referred to as a data driving circuit, a data driver or a source driving integrated circuit (or source driver IC (SDIC)). The gate driving circuit **120** can also referred to as a scan driving circuit, gate driver or a gate driving integrated circuit (or gate driver IC (GDIC)). The control circuit **130** can be a timing controller or a controller including the timing controller.
[0046] The driving circuits disposed in the circuit zone CZ of the silicon substrate **10** can further include a power circuit **140** for providing various signals and voltages used to drive the subpixels SP arranged in the pixel array zone PAZ of the silicon substrate **10** to the other circuits **110**, **120**, and **130**, or supplying the signals and voltages to the pixel array **100**.
[0047] Here, the power circuit **140** can include a power generator such as a DC-DC converter.
[0048] The driving circuits disposed in the circuit zone CZ of the silicon substrate **10** can further include at least one interface for electrical connection, signal input/output, or communication with other electronic components.
[0049] The interfaces can include, e.g., one or more of a low-voltage differential signaling (LVDS) interface, a mobile industry processor interface (MIPI), a serial interface, and the like.
[0050] As described above, by forming not only the pixel array **100**, but also driving circuits such as the source driving circuit **110**, the gate driving circuit **120**, the control circuit **130**, and the power circuit **140** on the same silicon substrate **10**, the device size can be reduced, and the manufacturing process can be efficiently and quickly performed.
[0051] Meanwhile, the circuit zone CZ can be present on one side, two sides, or three sides of the pixel array zone PAZ, or can be present while surrounding the outer periphery of the pixel array zone PAZ.
[0052] The source driving circuit **110** can be present only on one side of the pixel array zone PAZ, or can be present on two opposite sides (upper and lower sides, or left and right sides).
[0053] The gate driving circuit **120** can be present only on one side of the pixel array zone PAZ, or can be present on two opposite sides (left and right sides or upper and lower sides).
[0054] FIG. **3** is a view illustrating a micro display device **1** and a silicon wafer according to the present embodiments.
[0055] The whole or part of the micro display device **1** according to the present embodiments described above can be made in a process of manufacturing a silicon wafer.
[0056] From this point of view, the whole or part of the micro display device **1** according to the present embodiments can be viewed as a type of integrated circuit made through a silicon wafer manufacturing process (semiconductor process). In other words, large numbers of the micro display device **1** can be made through a manufacturing process applied to a same silicon wafer. For example, many micro display devices can be made together on the same silicon wafer, and then the wafter can be cut and divided to separate the individual micro display devices from each other as desired.
[0057] Accordingly, the whole or part of the micro display device **1** according to the present embodiments can be referred to as a display integrated circuit.
[0058] For example, the display integrated circuit according to the present embodiments can include a silicon substrate **10**, a plurality of subpixels SP arranged in the pixel array zone PAZ of the silicon substrate **10**, and driving circuits arranged in the circuit zone CZ of the silicon substrate **10** positioned around the pixel array zone PAZ.

[0059] As described above, since the whole or part of the micro display device **1** according to the present embodiments is made through a silicon wafer manufacturing process, there is an advantage of being able to manufacture large numbers of the micro display device **1** precisely, efficiently, and conveniently.
[0060] The micro display device **1** according to the present embodiments can be an organic light emitting diode (OLED) display, or can be another type of display such as a liquid crystal display (LCD).
[0061] Hereinafter, it is assumed that the micro display device **1** according to the present embodiments is an OLED display.
[0062] FIG. **4** is a plan view schematically illustrating a switch configuration of a micro display device according to the present embodiments. The micro display according to embodiments of the disclosure can include a switch to reduce the number of pads. For example, the number of data pads corresponding to the data lines can be reduced, which can reduce wiring and save space.
[0063] Referring to FIG. **4**, the disclosure time-divisionally supplies a data voltage VDATA output from the source driving circuit **110** through one channel to N data lines using a demultiplexer DEMUX (where N is a natural number of 2 or more).
[0064] In the following embodiments, the demultiplexer is described as having a 1:3 MUX structure for connecting one output terminal of the source driving circuit **110** to three data lines as an example, but the disclosure is not limited thereto.
[0065] The demultiplexer DEMUX can include a first switch SW**1** connected to a first data line DL**1**, a second switch SW**2** connected to a second data line DL**2**, and a third switch SW**3** connected to a third data line DL**3**.
[0066] For example, the first data line DL**1** can be connected to a red subpixel, the second data line DL**2** can be connected to a green subpixel, and the third data line DL**3** can be connected to a blue subpixel. This is merely an example, and the connection relationship between the subpixel and the data line is not limited thereto.
[0067] Accordingly, the demultiplexer DEMUX can connect the output terminal to one of the first data line DL**1**, the second data line DL**2**, and the third data line DL**3** using the first switch SW**1**, the second switch SW**2**, and the third switch SW**3**, and transfer the data voltage applied from the source driving circuit **110** to the data line connected to the output terminal.
[0068] FIG. **5** is an example view illustrating a subpixel structure of a micro display device **1** according to the present embodiments.
[0069] In the micro display device **1** according to the present embodiments, each of the plurality of subpixels SP can include an organic light emitting diode OLED, a driving transistor DRT for driving the organic light emitting diode OLED, a first transistor T**1** electrically connected between a first node N**1**, which is the gate node of the driving transistor DRT, and a data line DL, and a capacitor Cst electrically connected between the first node N**1** of the driving transistor DRT and a second node N**2**, which is the source node or the drain node of the driving transistor DRT.
[0070] The organic light emitting diode OLED can include a first electrode, an organic light emitting layer, and a second electrode.
[0071] The first electrode of the organic light emitting diode OLED can be the anode electrode (or the cathode electrode), and the second electrode of the organic light emitting diode OLED can be the cathode electrode (or the anode electrode).
[0072] A base voltage ELVSS can be applied to the second electrode of the organic light emitting diode OLED.
[0073] The driving transistor DRT includes the first node N**1**, the second node N**2**, and the third node N**3** as electrical nodes.
[0074] In the driving transistor DRT, the first node N**1** can correspond to the gate node and can be electrically connected to the source node or the drain node of the first transistor T**1**. The second node N**2** corresponds to the source node or the drain node and can be electrically connected to the first electrode of the organic light emitting diode OLED. The third node N**3** can be electrically connected to the driving voltage line DVL to receive the driving voltage ELVDD.
[0075] The first transistor T**1** can be controlled to be turned on and off by the scan signal SCAN applied to the gate node through the gate line GL, and can be electrically connected between the data line DL and the first node N**1** of the driving transistor DRT.
[0076] In the first transistor T**1**, the gate node can be electrically connected to the gate line GL, the drain node or the source node can be electrically connected to the data line DL, and the source node or the drain node can be electrically connected to the first node N**1** of the driving transistor DRT.
[0077] When the first transistor T**1** is turned on by the scan signal SCAN, the first transistor T**1** can transfer the data voltage VDATA supplied from the data line DL to the first node N**1** of the driving transistor DRT.
[0078] FIG. **6** is another example view illustrating a subpixel structure of a micro display device **1** according to the present embodiments.
[0079] Referring to FIG. **6**, in the micro display device **1** according to the present embodiments, each of the plurality of subpixels SP can further include a second transistor T**2** electrically connected between the second node N**2** of the driving transistor DRT and the sense line SL for sensing characteristics of the subpixel to perform a compensation operation.
[0080] In the second transistor T**2**, the gate node can be electrically connected to the gate line GL, the drain node or the source node can be electrically connected to the sense line SL, and the source node or the drain node can be electrically connected to the second node N**2** of the driving transistor DRT.
[0081] The second transistor T**2** can be controlled to be turned on and off by the scan signal SCAN applied to the gate node.
[0082] In the subpixel structure of FIG. **6**, the gate node of the first transistor T**1** and the gate node of the second transistor T**2** can be electrically connected to each other and can be commonly connected to one gate line GL.
[0083] In this situation, the gate node of the first transistor T**1** and the gate node of the second transistor T**2** can receive the scan signal SCAN together.
[0084] Alternatively, the gate node of the first transistor T**1** and the gate node of the second transistor T**2** can be separately connected to different gate lines GL.
[0085] In this situation, the gate node of the first transistor T**1** and the gate node of the second transistor T**2** can individually receive the scan signal SCAN.
[0086] The second transistor T**2** can be turned on to apply the reference voltage VSS to the second node N**2** of the driving transistor DRT.
[0087] Further, the second transistor T**2** can be turned off to electrically float the second node N**2** of the driving transistor DRT.
[0088] As described above, through the second transistor T**2** and the sense line SL, the voltage state of the second node N**2** of the driving transistor DRT can be controlled according to the driving type, the driving situation, and the like.
[0089] Each of the driving transistor DRT, the first transistor T**1**, and the second transistor T**2** can be an n-type transistor or a p-type transistor.

[0090] The storage capacitor Cst is not a parasitic capacitor (e.g., Cgs, Cgd), which is an internal capacitor present between the first node N**1** and the second node N**2** of the driving transistor DRT, but an external capacitor intentionally designed outside the driving transistor DRT.
[0091] FIG. **7** is an example view illustrating a cause of occurrence of a difference between a W emission luminance and the sum of R, G, and emission luminances. FIGS. **8** and **9** are equivalent circuit diagrams illustrating examples of a partial pixel structure of a micro display device according to the present embodiments.
[0092] Referring to FIGS. **4** and **7**, e.g., as shown on the left side of FIG. **7**, when only the first switch SW**1** is turned on by switching of the demultiplexer DEMUX, a data voltage can be applied to the first data line DL**1** so that the red subpixel can emit light.
[0093] Specifically, the storage capacitor Cst**1** illustrated in FIG. **8** is charged with the data voltage for light emission of the red subpixel, and the red OLED emits light based on the charged voltage.
[0094] The left graph of FIG. **7** illustrates an example of a state of a data voltage charged to the storage capacitor Cst**1** for red light emission. It can be identified that during the actual light emitting operation, the data charging state (solid line) of the storage capacitor Cst**1** is not sufficiently charged compared to the dashed line illustrated as being ideal due to RC delay, etc.
[0095] Similarly, when only the second switch SW**2** is turned on, a data voltage can be applied to the second data line DL**2** so that the green subpixel can emit light, and when only the third switch SW**3** is turned on, a data voltage can be applied to the third data line DL**3** so that the blue subpixel can emit light. Likewise, during the actual light emitting operation, the data charging state (solid line) of the storage capacitors Cst**2** and Cst**3** is not sufficiently charged compared to the dashed line illustrated as being ideal due to RC delay or the like.
[0096] As shown on the right side of FIG. **7**, when the first switch SW**1**, the second switch SW**2**, and the third switch SW**3** are sequentially turned on by the switching of the demultiplexer DEMUX, a data voltage is sequentially applied to the first data line DL**1**, the second data line DL, and the third data line DL**3**, so that all of the red subpixel, the green subpixel, and the blue subpixel emit light, and thus white light can be emitted and recognized by a viewer. Even if the red subpixel, the green subpixel, and the blue subpixel emit light sequentially, they are turned on at very short time intervals, so they can be considered to emit light substantially simultaneously (e.g., even though the red light, green light and blue light are emitted at slightly different timings, the timings are so fast and close together, that their emissions appear simultaneous to a human viewer and combine to form white light).
[0097] The graph on the right side of FIG. **7** illustrates an example of a state of a data voltage charged to each storage capacitor Cst**1**, Cst**2**, and Cst**3** for white light emission. Since the input terminal voltage, e.g., the data voltage applied from the output terminal of the demultiplexer to the data line experiences less of a swing than the left graph of FIG. **8** (e.g., the data voltage is maintained at a high level for the three different subpixels), it can be identified that the data charging state (solid line) of each of the storage capacitors Cst**1**, Cst**2**, and Cst**3** is sufficiently charged to be close to the dashed line illustrated as ideal.
[0098] The numerical value L(R)+L(G)+L(B) which is the sum of the respective emission luminances of the red subpixel, the green subpixel, and the blue subpixel is shown to be smaller than the numerical value of the white emission luminance L(W). Experimentally, during 3:1 Mux-based display panel **110** driving, the L(R)+L(G)+L(B) value, which is the sum of the respective emission luminances of R, G, and B, is only about 84% of the white emission luminance L(W) obtained by simultaneous light emission of R, G, and B.
[0099] The shortage of charging of the storage capacitor Cst that causes such a difference is due to, firstly, insufficient charging time due to RC delay and secondly a swing of the input terminal voltage (e.g., Red 5V, Green 0V, Blue 0V). This is because even if the signal of the demultiplexer is turned on in time, the state of the previous output data affects the final charging voltage of the storage capacitor Cst (e.g., transitioning from 0V to 5V takes some time and luminance will be lower than when maintaining 5V for consecutive emissions of two more subpixels within a same pixel unit). Thus, a color luminance ratio imbalance may be noticeable by a viewer, which may be even more apparent when using a small display device that is held very close to a user's eyes, such as a VR display. For example, a color luminance ratio imbalance can cause color distortion between pixel units that display part of an image that is predominantly one solid primary color (e.g., mainly just green, mainly just red, or mainly just blue) and pixel units that display part of the image that is white or predominantly white, which can impair image quality and cause eye strain and fatigue. For example, some parts of the display may appear too dim (e.g., pixel units displaying predominantly one primary color) and other parts of the display may appear too bright or washed out (e.g., pixel units displaying white), which can result in luminance inconsistencies that may be undesirably noticeable to the user.
[0100] In order to address this issue, an embodiment of the disclosure addresses the luminance increase phenomenon that occurs according to the charging voltage of the storage capacitor during white light emission and high-current driving.
[0101] Referring to FIG. **8**, an embodiment of the disclosure includes a structure in which all of the light emitting structures disposed in the red subpixel R, the green subpixel G, and the blue subpixel B simultaneously emit light to emit white light. Alternatively, each of the red subpixel R, the green subpixel G, and the blue subpixel B illustrated in FIG. **8** can be individually driven to implement red light emission, green light emission, and blue light emission.
[0102] FIG. **8** illustrates an example in which the red subpixel R, the green subpixel G, and the blue subpixel B are arranged in the horizontal direction on the display panel **100**, but the disclosure is not limited thereto, and the red subpixel R, the green subpixel G, and the blue subpixel B can be arranged in other arrangements.
[0103] Referring to FIGS. **8** and **9**, an embodiment of the disclosure addresses the illuminance increase phenomenon that occurs according to the charging voltage of the storage capacitor during white light emission and high-current driving by providing a first resistance unit at a first power source voltage line end.
[0104] Referring to FIG. **8**, the first power source voltage can be a low-potential driving voltage EVSS. The first power source voltage line can include a line L**1** connected to the anode line of the first light emitting element ED**1** from the first power source voltage supply terminal EVSS, a line L**2** connected to the anode line of the second light emitting element ED**2** from the first power source voltage supply terminal EVSS, and a line L**3** connected to the anode line of the third light emitting element ED**3** from the first power source voltage supply terminal EVSS.
[0105] The first resistance unit can be provided in at least a portion of the first power source voltage line connected between the first power source voltage supply terminal EVSS and each of the light emitting elements ED**1**, ED**2**, and ED**3**. For example, the light emitting elements ED**1**, ED**2**, and ED**3** can be connected in common to one end of first resistance unit and another end of the first

resistance unit can be connected to the first power source voltage supply terminal EVSS.
[0106] The first resistance unit can include a fixed resistance element or a variable resistance element.
[0107] The first resistance unit can be provided as a resistance element or a TFT transistor.
[0108] FIG. **8** illustrates a situation in which the first resistance unit is provided as the TFT transistor T**3**, and the TFT transistor T**3** is provided in the display panel **100**. For example, the TFT transistor T**3** can be provided in the display area or can be provided in the non-display area.
[0109] The lower graph of FIG. **8** is an i-v transfer graph showing changes in flowing current i according to changes in the gate voltage v for the transistor.
[0110] As in the graph showing the current-voltage transfer characteristics of the transistor shown on the lower side of FIG. **8**, when the first resistance unit is provided as the TFT transistor T**3**, the TFT transistor T**3** can be used as a resistor in the linear area section of the i-v curve of the TFT transistor T**3** corresponding to the circled dashed line portion.
[0111] The source node of the TFT transistor T**3** can be connected to the cathode electrode of the green subpixel, the drain node can be connected to the first power source voltage supply terminal EVSS, and the gate node can be connected to the anode electrode of the red subpixel, the anode electrode of the green subpixel, and the anode electrode of the blue subpixel. In other words, the source electrode of the TFT transistor T**3** can be connected in common to the cathode electrodes of the red, green and blue subpixels, the gate electrode of TFT transistor T**3** can be connected in common to the anode electrodes of the red, green and blue subpixels, and the drain electrode of the TFT transistor T**3** can be connected to the first power source voltage supply terminal EVSS.
[0112] Alternatively, as illustrated in FIG. **9**, the first resistance unit can be provided outside of the display panel **100** (e.g., external to the display panel **100**). In this situation, the first resistance unit can be connected to at least a partial line LA of the first power source voltage line connected between the first power source voltage supply terminal EVSS and the display panel **100**. FIG. **9** illustrates a situation in which a variable resistance element Revss is connected as a first resistance unit.
[0113] The variable resistance element Revss can be provided to vary the resistance value of the first resistance unit according to the body effect in which the threshold voltage varies according to the voltage applied to a transistor provided in the display panel **100**.
[0114] FIG. **10** is an example circuit diagram illustrating driving for dropping a luminance increase that occurs according to a charging voltage of a storage capacitor during white emission and high-current driving according to an embodiment of the disclosure.
[0115] Referring to FIG. **10**, a display panel according to an embodiment of the disclosure includes a first resistance unit Revss connected between a first power source voltage supply terminal EVSS and a light emitting element ED of a subpixel.
[0116] When the current for light emission of the light emitting element flows through the light emitting element ED, the voltage across two opposite ends of the first resistance unit Revss increases.
[0117] Accordingly, as shown in Equation 1 below, as the voltage of the first resistance unit Revss increases, the voltage of the anode end of the light emitting element ED increases, and thus the Vsb voltage increases, and thus the IOLED current decreases. When the Vsb voltage increases, the influence by the body effect increases.
[00001]

$$i_{OLED} = \frac{1}{2} C_{OX} \frac{W}{L}(V_{gs} - V_{thN})^2 V_{thN} = V_{th} + V_{sb}(\text{: Body - effectcoefficient}) \therefore i_{OLED} = \frac{1}{2} C_{OX} \frac{W}{L}(V_{gs} - (V_{th} + V_{sb}))^2 \quad \text{[Equation1}$$

[0118] In Equation 1 above, μ: Transistor Mobility, W: Transistor Channel Width, L: Transistor Channel Length, VthN: New threshold voltage changed by body effect, Vth: Threshold voltage when there is no body effect, a: Body-effect coefficient, and Vsb: Voltage source-body.
[0119] As described above, the TFT transistor T**3** can be provided in at least a portion of the first power source voltage line of one pixel constituted of the red subpixel R, the green subpixel G, and the blue subpixel B in the pixel circuit inside the display panel **100**, and the TFT transistor T**3** can be driven in the linear section to operate as a resistor, so that the voltage drop (IR drop) can be greater when the red, green, and blue light emitting elements are controlled to simultaneously emit light to implement white emission than when the red, green, and blue light emitting elements are controlled to individually emit light. In other words, the TFT transistor T**3** can act as a type of buffer or counter sink that can dampen the luminance when white light is emitted by a pixel unit so that it is more similar to the luminance of when one primary color is predominantly emitted by the pixel unit (e.g., when just the red subpixel within the pixel unit emits light, etc.). For example, the TFT transistor T**3** can step down the brightness when white light is emitted by the pixel unit so that the brightness is about same or similar to when one primary color of light is emitted by the pixel unit. In this way, image quality can be improved because the luminance can be held to be more uniform across the display panel even when displaying white on some parts of the screen and different colors of light on other parts of the screen.
[0120] Through the principle, when the red subpixel R, the green subpixel G, and the blue subpixel B simultaneously emit light to emit white light, the IOLED current flowing through the first current voltage line can be reduced, thereby addressing the color luminance ratio issue with the RGB shared micro display.
[0121] In other words, the difference between the sum L(R)+L(G)+L(B) of the respective light emission luminances of the red subpixel, the green subpixel, and the blue subpixel and the white light emission luminance L(W) can be reduced and more uniform luminance can be provided.
[0122] FIG. **11** illustrates a graph and table showing luminance comparison between per-resistance white emission of a first resistance unit and R, G, and B individual emissions according to an embodiment of the disclosure.
[0123] Referring to FIG. **11**, it can be identified that the voltage drop (IR drop) is greater when allowing the red, green, and blue light emitting elements to simultaneously emit light to emit white light than when allowing the red, green, and blue light emitting elements to individually emit light by providing the first resistance unit in at least a portion of the first power source voltage line of one pixel constituted of the red subpixel R, the green subpixel G, and the blue subpixel B, so that the luminance is reduced.
[0124] The micro display according to the above-described embodiments of the disclosure can be provided in a virtual reality (VR) device or an augmented reality (AR) device.
[0125] The above-described display panel according to embodiments of the disclosure can be briefly described again below.
[0126] A micro display device can comprise a pixel unit disposed on a display panel and including a red subpixel, a green subpixel, and a blue subpixel, a first power source voltage line including a first line connected between a first power source voltage supply terminal and the red subpixel, a second line connected between the first power source voltage supply terminal and the green subpixel,

and a third line connected between the first power source voltage supply terminal and the blue subpixel, and a first resistance unit connected to at least a portion of the first power source voltage line.
[0127] The first resistance unit can include a fixed resistance element.
[0128] The first resistance unit can include a variable resistance element.
[0129] A resistance value of the variable resistance element can be varied according to a body effect in which a threshold voltage is varied according to a voltage applied to a transistor provided in the display panel.
[0130] The first resistance unit can be provided in a display area of the display panel.
[0131] The first resistance unit can be provided in a non-display area of the display panel.
[0132] The first resistance unit can be provided outside of the display panel.
[0133] The first resistance unit can be provided as a TFT transistor.
[0134] In the first resistance unit, the TFT transistor can be used as a resistor in a linear mode section of the TFT transistor.
[0135] A source node of the TFT transistor can be connected to a cathode electrode of the green subpixel, a drain node can be connected to the first power source voltage supply terminal, and a gate node can be connected to an anode electrode of the red subpixel, an anode electrode of the green subpixel, and an anode electrode of the blue subpixel.
[0136] The red subpixel, the green subpixel, and the blue subpixel can be arranged in a horizontal direction on the display panel.
[0137] The red subpixel, the green subpixel, and the blue subpixel can emit white light through simultaneous light emission.
[0138] The foregoing features, structures, or effects are included in, but not limited to, at least one embodiment of the disclosure. The features, structures, or effects exemplified in at least one example of the disclosure can be combined or modified by one of ordinary skill in the art in other embodiments. Thus, such combinations or modifications should be interpreted as belonging to the scope of the disclosure.
[0139] The above description has been presented to enable any person skilled in the art to make and use the technical idea of the disclosure, and has been provided in the context of a particular application and its requirements. Various modifications, additions and substitutions to the described embodiments will be readily apparent to those skilled in the art, and the general principles defined herein can be applied to other embodiments and applications without departing from the spirit and scope of the disclosure. The above description and the accompanying drawings provide an example of the technical idea of the disclosure for illustrative purposes only. That is, the disclosed embodiments are intended to illustrate the scope of the technical idea of the disclosure.

Claims

1. A micro display device, comprising: a pixel unit disposed on a display panel, the pixel unit including a red subpixel, a green subpixel and a blue subpixel; a first power source voltage line including a first line connected between a first power source voltage supply terminal and the red subpixel, a second line connected between the first power source voltage supply terminal and the green subpixel, and a third line connected between the first power source voltage supply terminal and the blue subpixel; and a first resistance unit connected to at least a portion of the first power source voltage line.
2. The micro display device of claim 1, wherein the first resistance unit includes a fixed resistance element.
3. The micro display device of claim 1, wherein the first resistance unit includes a variable resistance element.
4. The micro display device of claim 3, wherein a resistance value of the variable resistance element is configured to vary based on a body effect in which a threshold voltage is varied according to a voltage applied to a transistor provided in the display panel.
5. The micro display device of claim 1, wherein the first resistance unit is disposed in a display area of the display panel.
6. The micro display device of claim 1, wherein the first resistance unit is disposed in a non-display area of the display panel.
7. The micro display device of claim 1, wherein the first resistance unit is disposed outside of the display panel.
8. The micro display device of claim 1, wherein the first resistance unit is a thin film transistor.
9. The micro display device of claim 8, wherein the thin film transistor is configured to be used as a resistor in a linear mode section of the thin film transistor.
10. The micro display device of claim 8, wherein a source node of the thin film transistor is connected to a cathode electrode of the green subpixel, a drain node of the thin film transistor is connected to the first power source voltage supply terminal, and a gate node of the thin film transistor is connected to an anode electrode of the red subpixel, an anode electrode of the green subpixel and an anode electrode of the blue subpixel.
11. The micro display device of claim 1, wherein the red subpixel, the green subpixel, and the blue subpixel are arranged in a horizontal direction on the display panel.
12. The micro display device of claim 1, wherein the red subpixel, the green subpixel, and the blue subpixel are configured to emit white light through simultaneous light emission.
13. A display device comprising: a pixel disposed on a substrate, the pixel including a first color subpixel configured to emit light of a first color, a second color subpixel configured to emit light of a second color and a third color subpixel configured to emit light of a third color; a data driver disposed on the substrate, the data driver being connected to a plurality of data lines; a gate driver disposed on the substrate, the gate driver being connected to a plurality of gate lines; a demultiplexer connected between one data line among the plurality of data lines and the first, second and third color subpixels within the pixel; and a first resistance unit connected between the pixel and a first power source voltage line.
14. The display device of claim 13, wherein the first resistance unit is configured to reduce a luminance of the pixel when the first, second and third color subpixels emit white light.
15. The display device of claim 13, wherein the first resistance unit has a fixed resistance.
16. The display device of claim 13, wherein the first resistance unit has a variable resistance.
17. The display device of claim 13, wherein the first resistance unit is disposed external to the substrate.
18. The display device of claim 13, wherein the first resistance unit is disposed on the substrate that includes the pixel, the data driver and the gate driver.
19. The display device of claim 13, wherein the first resistance unit is a thin film transistor, wherein the first color subpixel includes a first light emitting element having a first electrode and a second electrode, the second color subpixel includes a second light emitting

element having a first electrode and a second electrode, and the third color subpixel includes a third light emitting element having a first electrode and a second electrode, wherein a gate electrode of the film transistor is connected in common to the first electrode of the first light emitting element in the first color subpixel, the first electrode of the second light emitting element in the second color subpixel and the first electrode of the third light emitting element in the third color subpixel, wherein a first electrode of the thin film transistor is connected in common to the second electrode of the first light emitting element in the first color subpixel, the second electrode of the second light emitting element in the second color subpixel and the second electrode of the third light emitting element in the third color subpixel, and wherein a second electrode of the thin film transistor is connected to the first power source voltage line.

20. A display device comprising: a pixel disposed on a substrate, the pixel including a first color subpixel configured to emit light of a first color, a second color subpixel configured to emit light of a second color and a third color subpixel configured to emit light of a third color; a demultiplexer connected between one data line among the plurality of data lines and the first, second and third color subpixels within the pixel; and a first resistance unit connected between the pixel and a first power source voltage line, wherein the first resistance unit is a thin film transistor, wherein the first color subpixel includes a first light emitting element having a first electrode and a second electrode, the second color subpixel includes a second light emitting element having a first electrode and a second electrode, and the third color subpixel includes a third light emitting element having a first electrode and a second electrode, wherein a gate electrode of the film transistor is connected in common to the first electrode of the first light emitting element in the first color subpixel, the first electrode of the second light emitting element in the second color subpixel and the first electrode of the third light emitting element in the third color subpixel, wherein a first electrode of the thin film transistor is connected in common to the second electrode of the first light emitting element in the first color subpixel, the second electrode of the second light emitting element in the second color subpixel and the second electrode of the third light emitting element in the third color subpixel, and wherein a second electrode of the thin film transistor is connected to the first power source voltage line.