



US012389812B2

(12) **United States Patent**  
**Wells**

(10) **Patent No.:** **US 12,389,812 B2**

(45) **Date of Patent:** **\*Aug. 12, 2025**

(54) **METHOD AND APPARATUS PROVIDING  
MULTI-PLANED ARRAY MEMORY DEVICE**

**63/10** (2023.02); **H10B 63/84** (2023.02);  
**H10N 70/231** (2023.02); **G11C 2213/71**  
(2013.01)

(71) Applicant: **Micron Technology, Inc.**, Boise, ID  
(US)

(58) **Field of Classification Search**  
CPC .. H10N 70/821; H10N 703/231; H10B 63/84;  
H10B 63/00; G11C 13/0004  
See application file for complete search history.

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(US)

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(\*) Notice: Subject to any disclaimer, the term of this  
patent is extended or adjusted under 35  
U.S.C. 154(b) by 912 days.

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This patent is subject to a terminal dis-  
claimer.

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(21) Appl. No.: **17/078,817**

WO WO-2004100267 A1 \* 11/2004 ..... G11C 7/18

(22) Filed: **Oct. 23, 2020**

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(65) **Prior Publication Data**

US 2021/0043834 A1 Feb. 11, 2021

Lee et al., "A 90nm 1.8V 512Mb Diode-Switch PRAM with  
266MB/s Read Throughput," Int'l Solid-State Circuits Conference,  
2007, Feb. 11-15, 2007, 3 pgs. ISSCC 2007 / Session 26 / Non-  
Volatile Memories / 26.1, Digest of Technical Papers, IEEE Inter-  
national.

**Related U.S. Application Data**

(62) Division of application No. 16/125,235, filed on Sep.  
7, 2018, now Pat. No. 10,840,443, which is a division  
of application No. 15/437,308, filed on Feb. 20, 2017,  
now Pat. No. 10,084,129, which is a division of  
application No. 14/177,253, filed on Feb. 11, 2014,  
now Pat. No. 9,614,151, which is a division of  
(Continued)

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(51) **Int. Cl.**

**H10N 70/00** (2023.01)

**G11C 13/00** (2006.01)

**H10B 63/00** (2023.01)

**H10B 63/10** (2023.01)

**H10N 70/20** (2023.01)

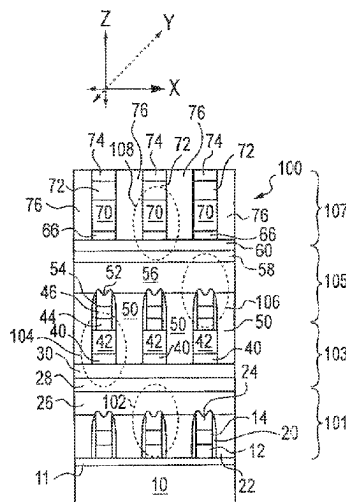
(57) **ABSTRACT**

A three-dimensional variable resistance memory array and  
method of forming the same. The memory array has memory  
cells in multiple planes in three dimensions. The planes of  
the memory cells include shared interconnect lines, dually  
connected to driving and sensing circuits, that are used for  
addressing the cells for programming and reading. The  
memory array is formed using only a single patterned mask  
per central array plane to form the memory cells of such  
planes.

(52) **U.S. Cl.**

CPC ..... **H10N 70/821** (2023.02); **G11C 13/0004**  
(2013.01); **G11C 13/0023** (2013.01); **H10B**

**20 Claims, 21 Drawing Sheets**



**Related U.S. Application Data**

application No. 11/828,092, filed on Jul. 25, 2007,  
now Pat. No. 8,679,977.

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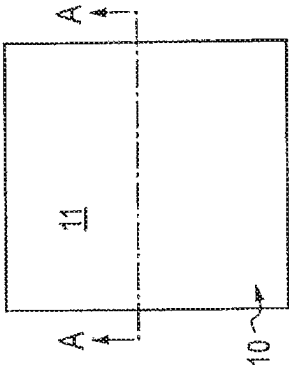


FIG. 1a

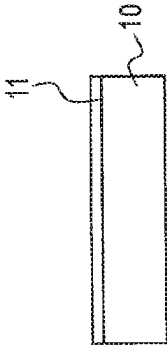


FIG. 1b

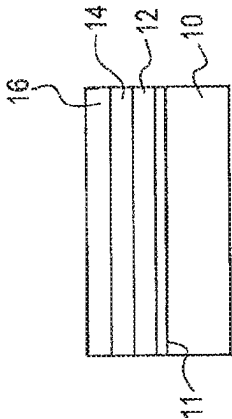


FIG. 2b

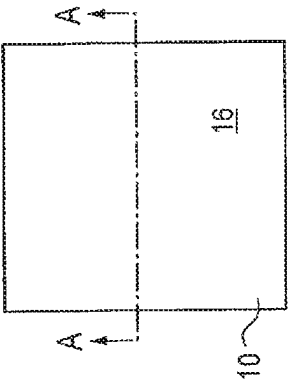


FIG. 2a

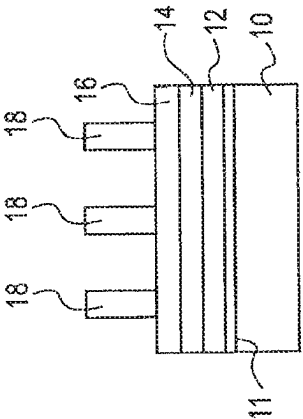


FIG. 3a

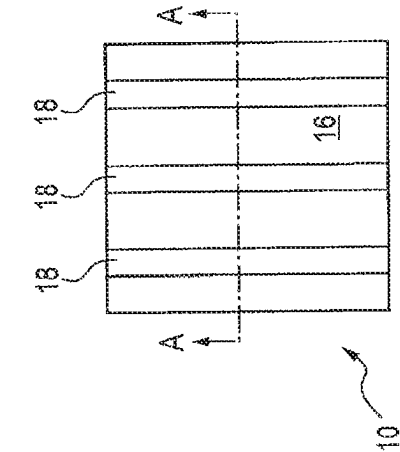


FIG. 3b

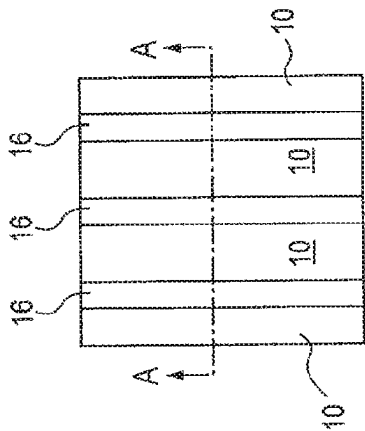


FIG. 4a

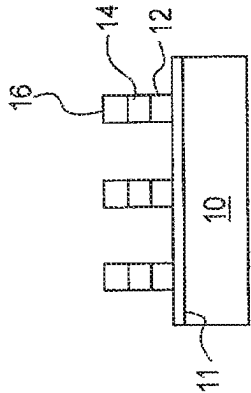
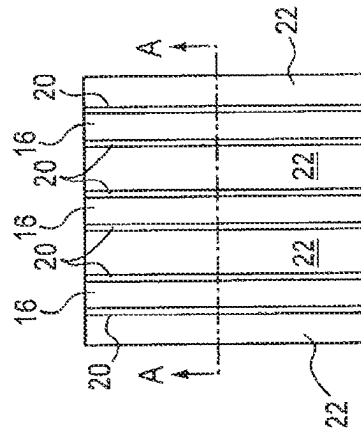




























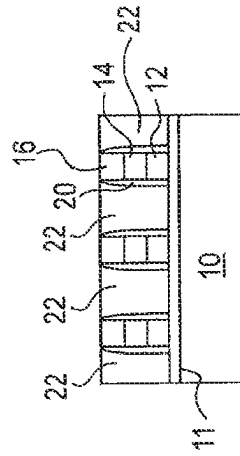


FIG. 4b





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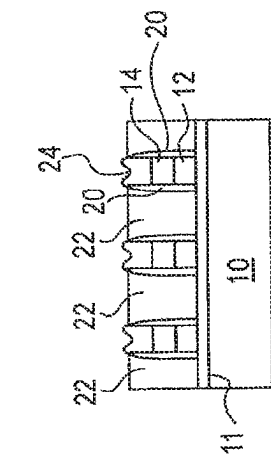
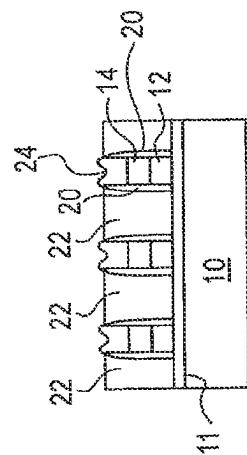


FIG. 6a

FIG. 6b





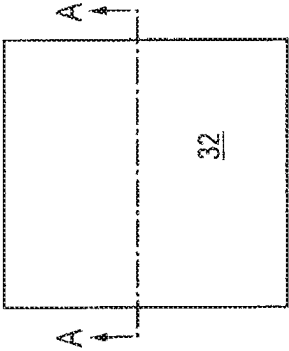


FIG. 7a

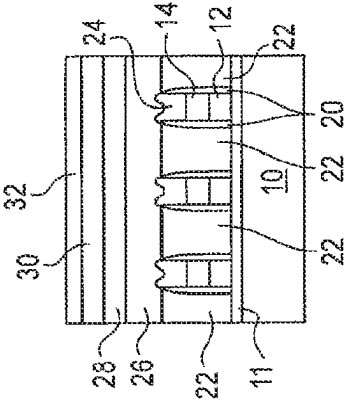
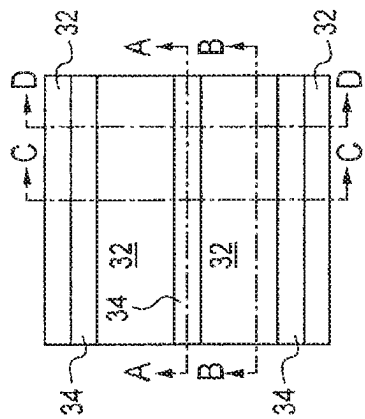
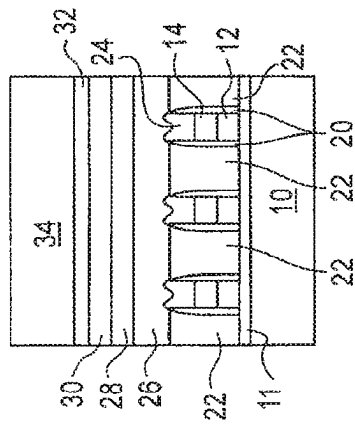


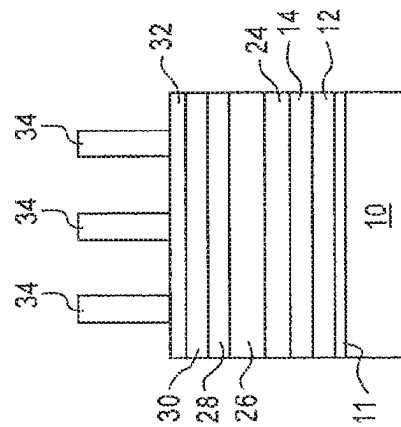
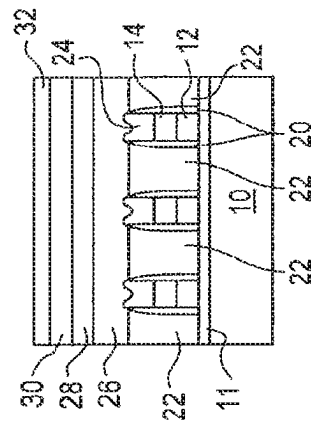
FIG. 7b



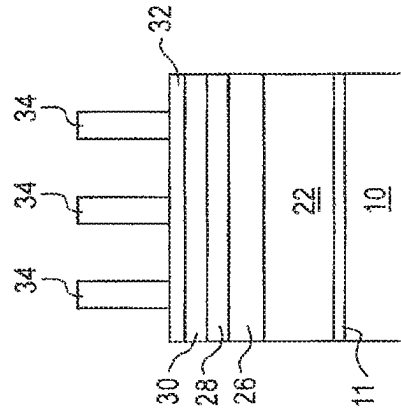
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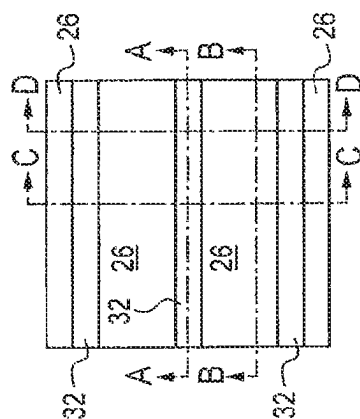


FIG. 9a

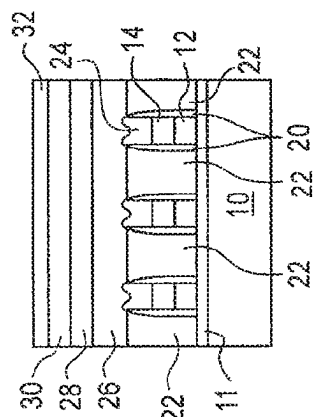


FIG. 9b

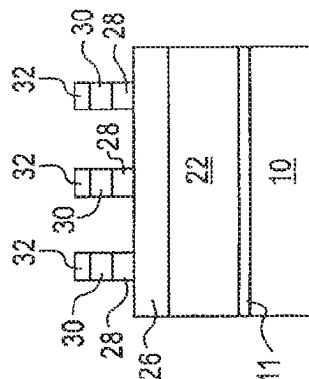


FIG. 9c

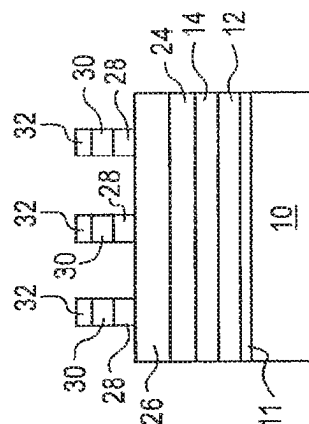


FIG. 9d

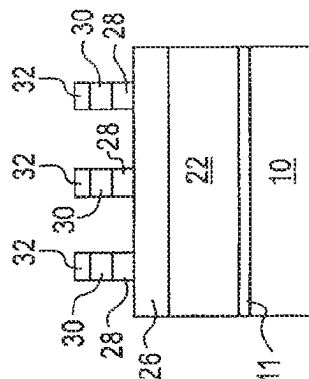


FIG. 9e

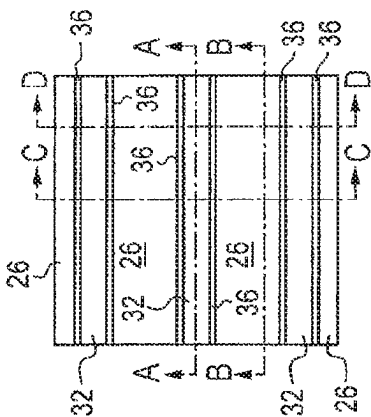


FIG. 10a

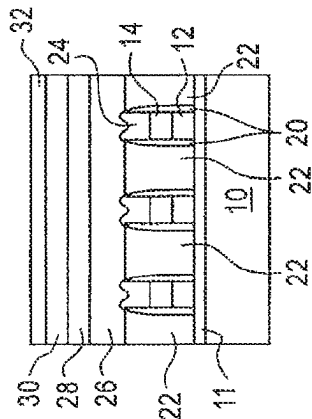


FIG. 10b

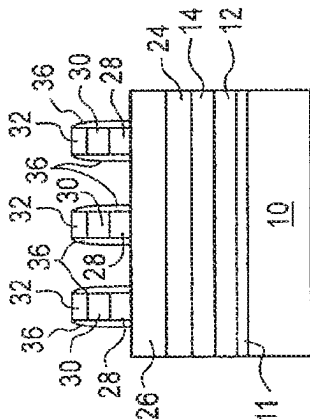


FIG. 10c

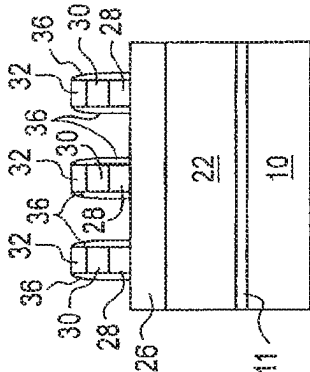


FIG. 10d

FIG. 10e

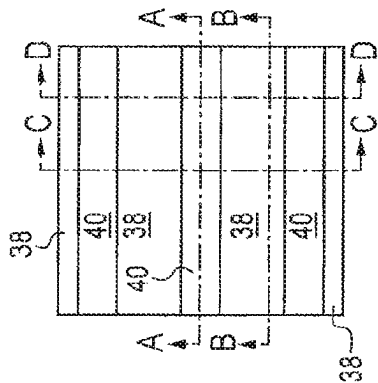


FIG. 11a

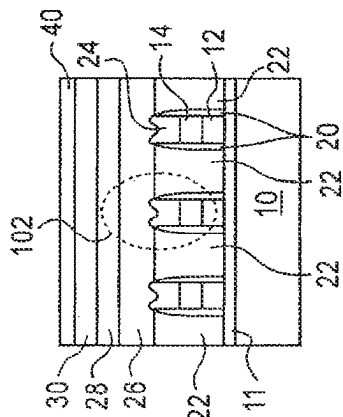


FIG. 11b

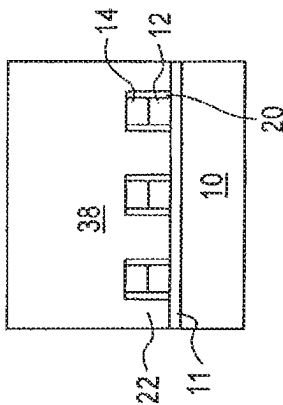


FIG. 11c

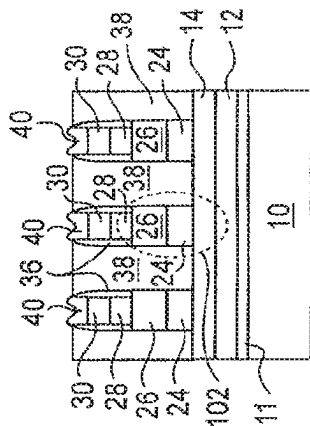


FIG. 11d

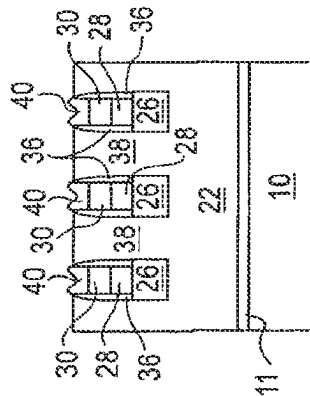


FIG. 11e

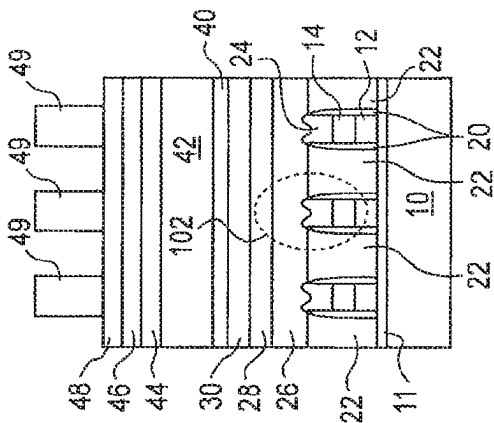


FIG. 12a

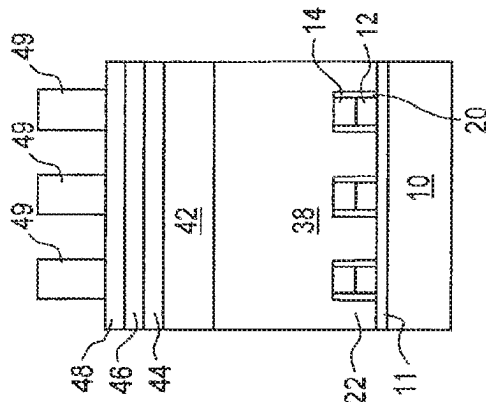


FIG. 12b

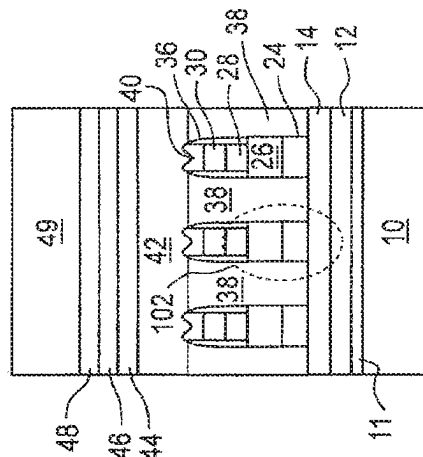


FIG. 12c

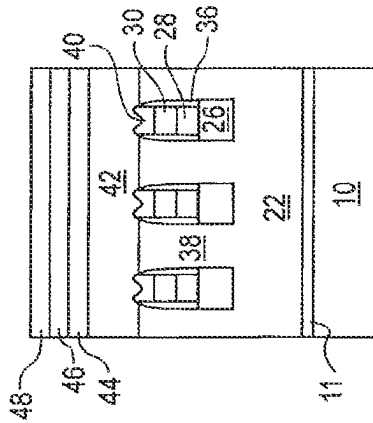


FIG. 12e

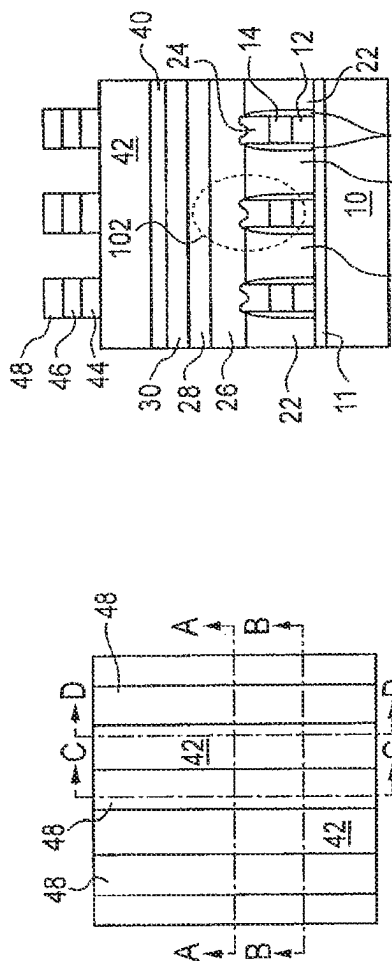


FIG. 13a

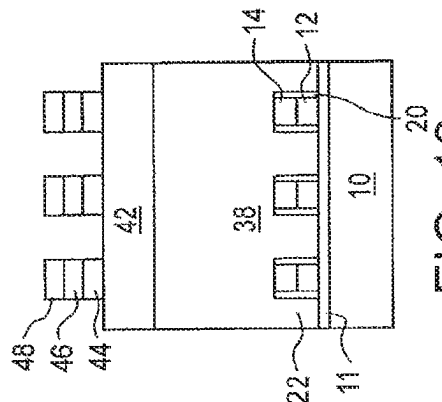


FIG. 13c

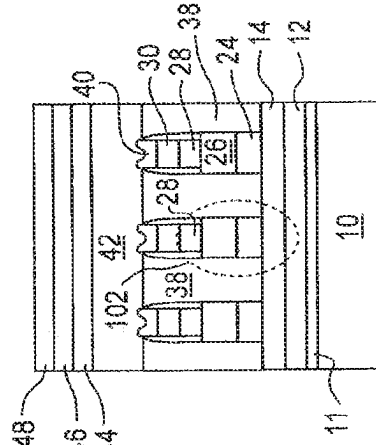


FIG. 13d

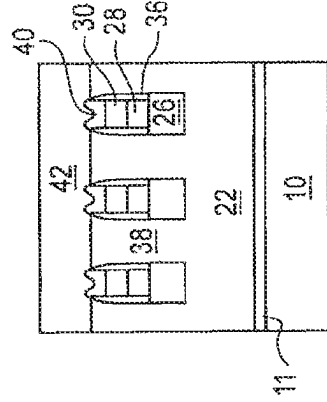


FIG. 13e

FIG. 13b

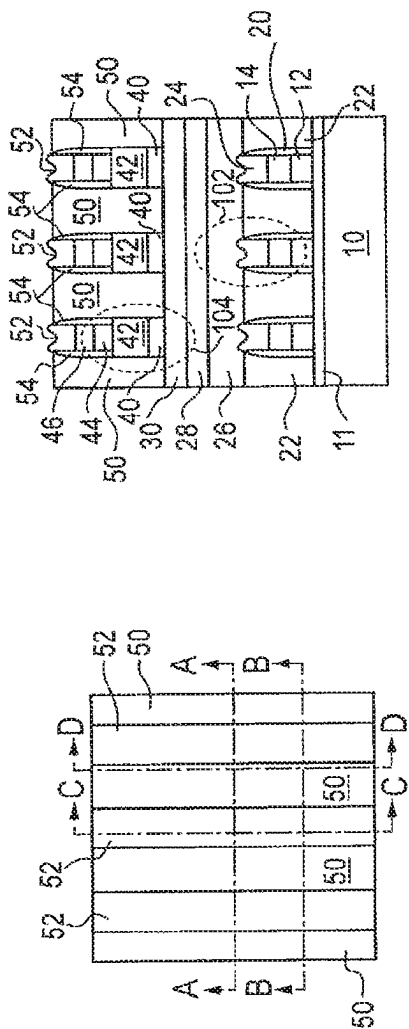


FIG. 14a

FIG. 14b

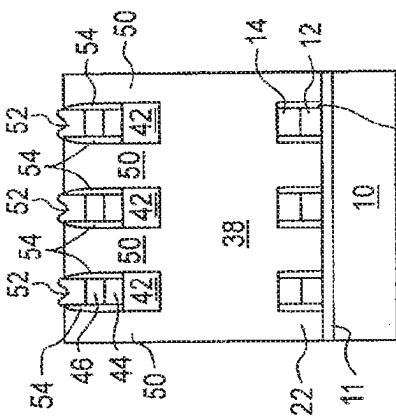


FIG. 14c

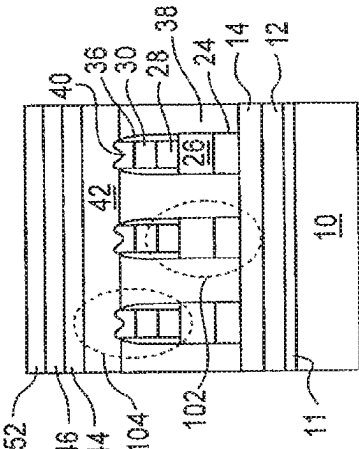


FIG. 14d

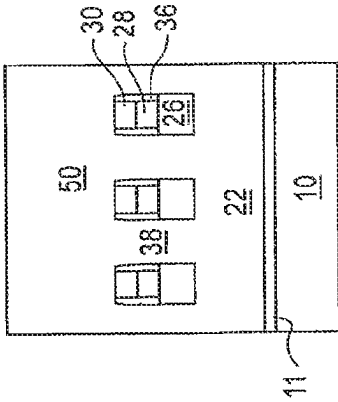


FIG. 14e



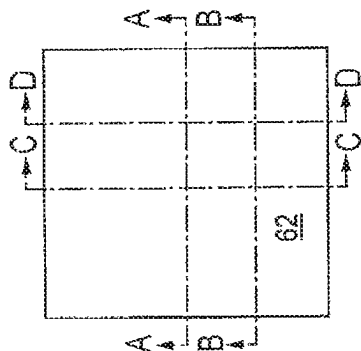


FIG. 15a

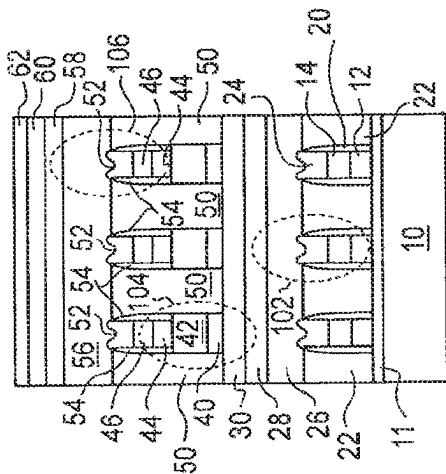


FIG. 15b

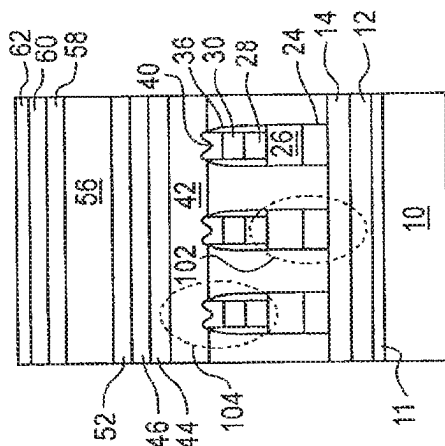


FIG. 15c

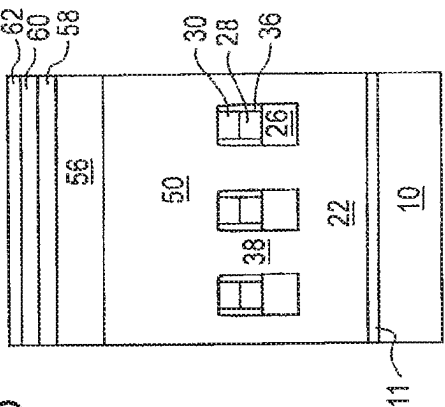


FIG. 15d

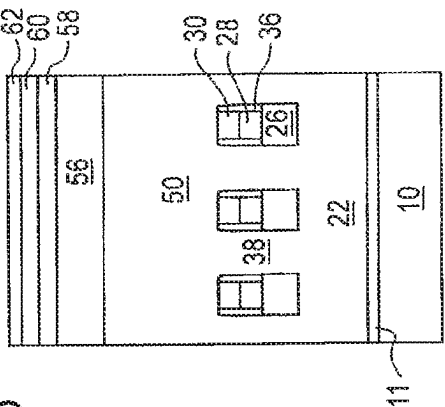
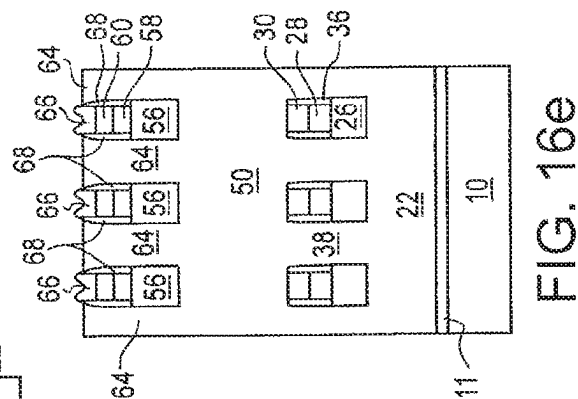
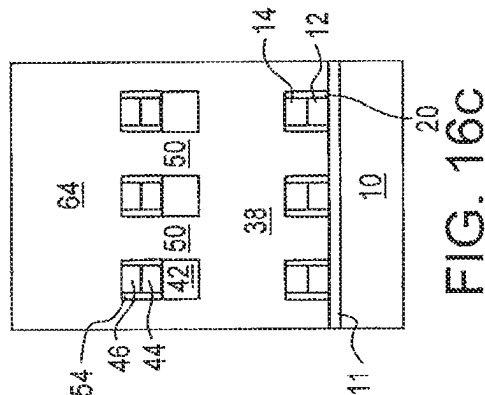
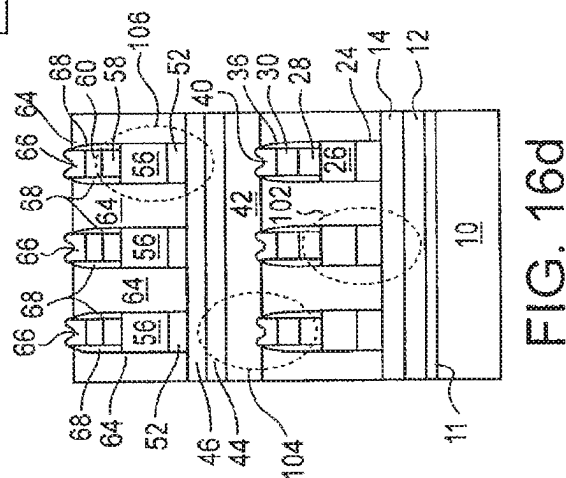
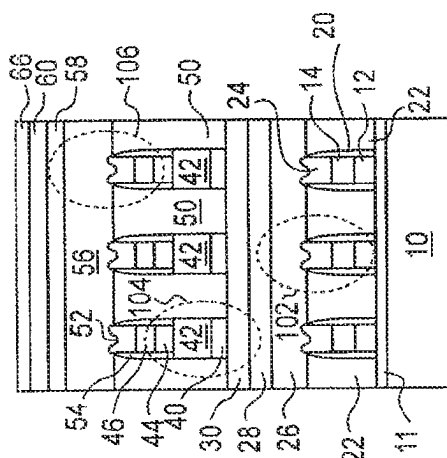
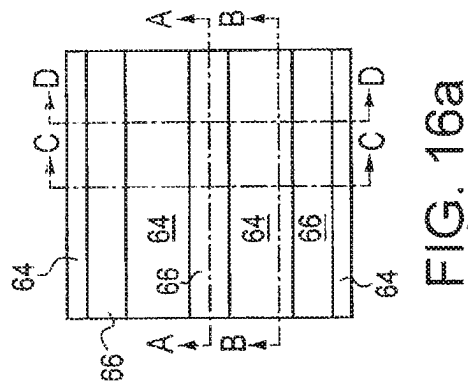


FIG. 15e



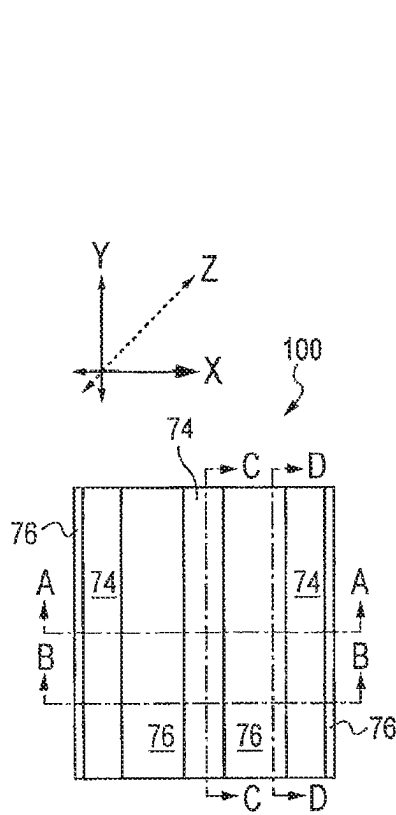


FIG. 17a

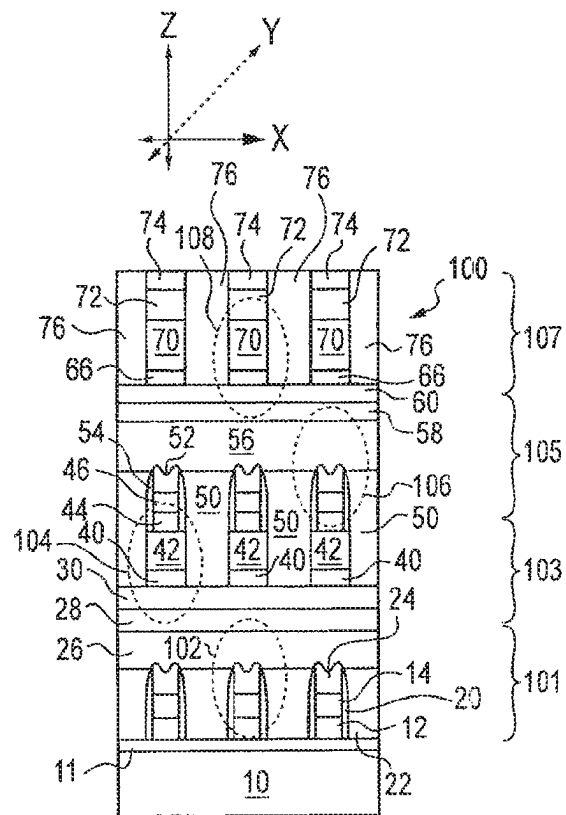


FIG. 17b

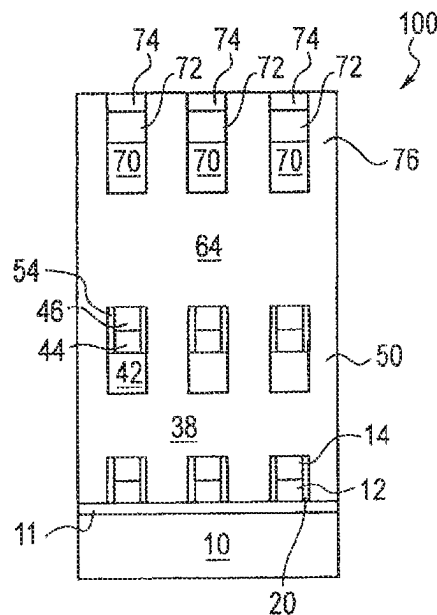


FIG. 17c

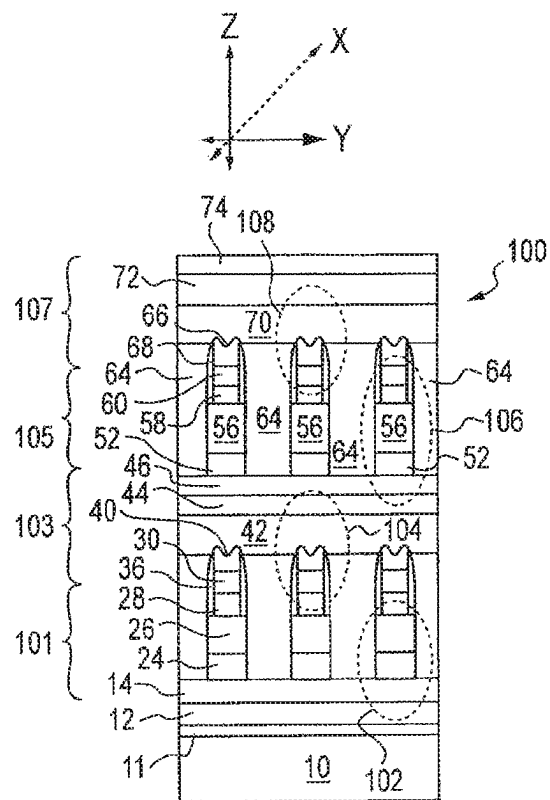


FIG. 17d

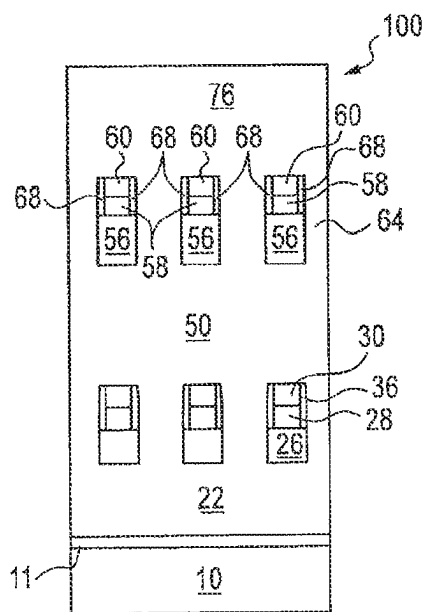


FIG. 17e

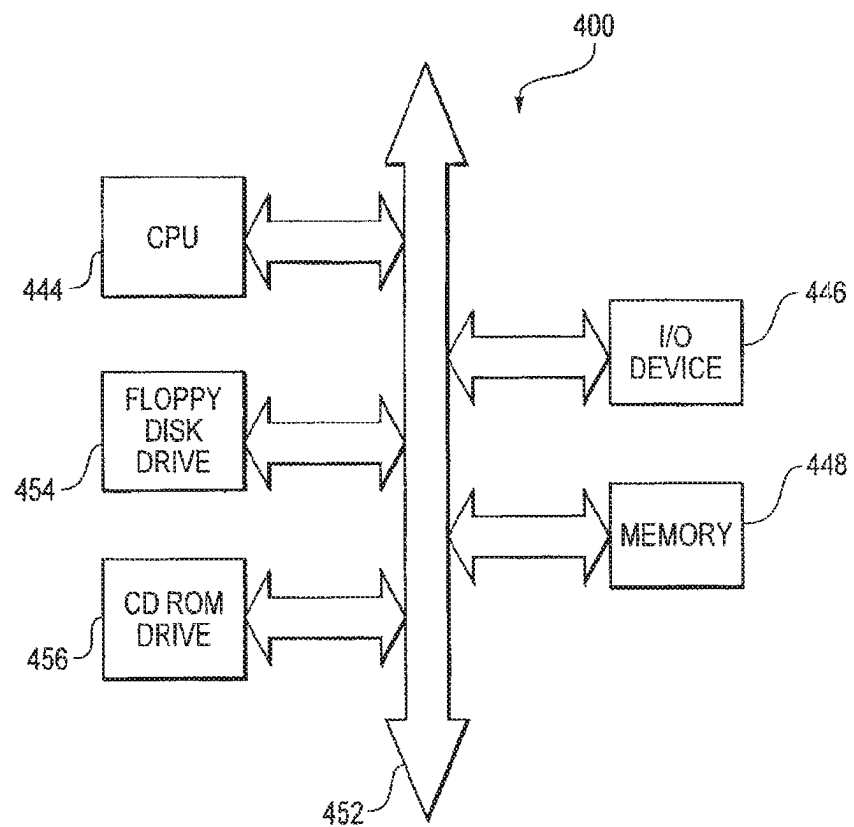


FIG. 18

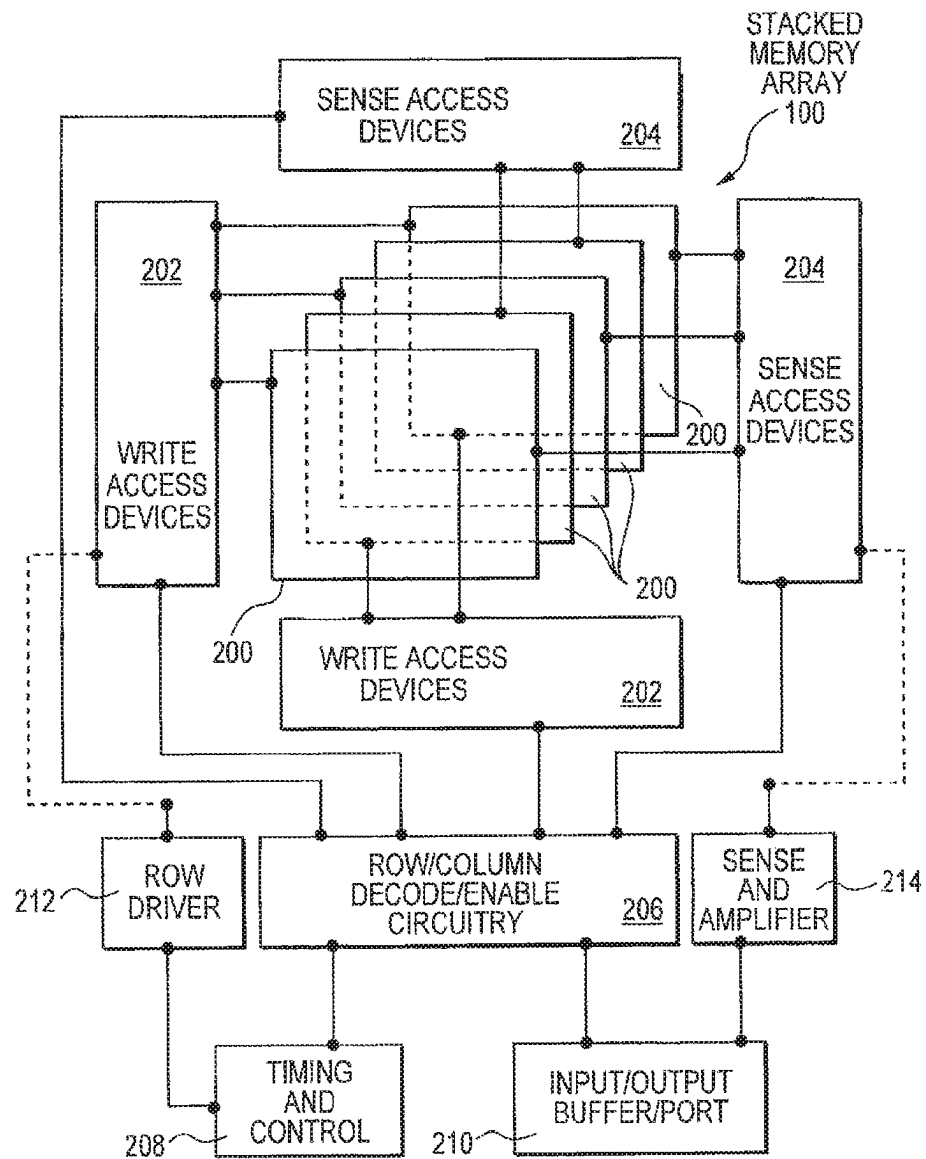


FIG. 19

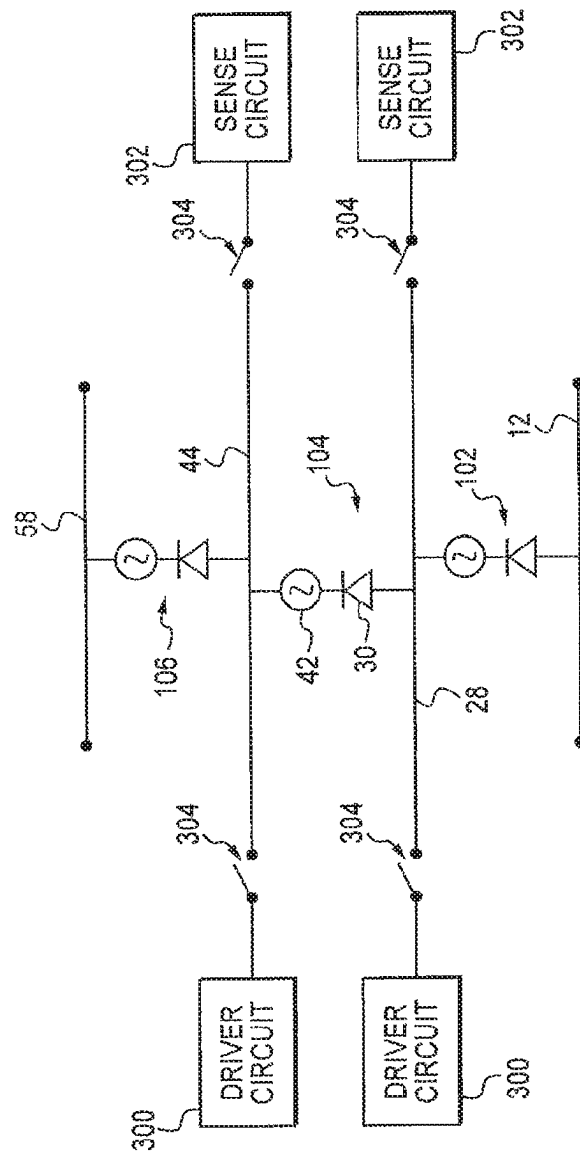


Fig. 20

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## METHOD AND APPARATUS PROVIDING MULTI-PLANED ARRAY MEMORY DEVICE

### CROSS-REFERENCE TO RELATED APPLICATIONS

The present application for Patent is a divisional of U.S. patent application Ser. No. 16/125,235 by Wells, entitled "Method And Apparatus Providing Multi-Planed Array Memory Device," filed Sep. 7, 2018, which is a divisional of U.S. patent application Ser. No. 15/437,308 by Wells, entitled "Method And Apparatus Providing Multi-Planed Array Memory Device," filed Feb. 20, 2017, which is a divisional application of U.S. patent application Ser. No. 14/177,253 by Wells, entitled "Method and Apparatus Providing Multi-Planed Array Memory Device," filed Feb. 11, 2014, which is a divisional application of U.S. patent application Ser. No. 11/828,092 by Wells, entitled "Method and Apparatus Providing Multi-Planed Array Memory Device," filed Jul. 25, 2007, assigned to the assignee hereof, and each of which is expressly incorporated by reference in its entirety herein.

### FIELD OF THE INVENTION

The present invention relates to semiconductor devices, and in particular resistance-variable memory devices, such as phase-change memory, and methods of forming the same.

### BACKGROUND OF THE INVENTION

Non-volatile (or less-volatile) memories are important elements of integrated circuits due to their ability to maintain data absent a power supply. Phase change materials, among other resistance-variable memory types, have been investigated for use in non-volatile memory cells. Phase change memory cells include phase change materials, such as chalcogenide alloys, which are capable of stably transitioning between amorphous and crystalline phases. Each phase exhibits a particular resistance state and the resistance states distinguish the logic values of the memory cell. Specifically, an amorphous state exhibits a relatively high resistance, and a crystalline state exhibits a relatively low resistance. A phase change memory cell has a phase change material between first and second electrodes. As an example, the phase change material is a chalcogenide alloy, such as described in U.S. Patent Application Publication No. 2007/0029537 (application Ser. No. 11/194,623) and U.S. Patent Application Publication No. 2007/0034905 (application Ser. No. 11/199,257), each of which are incorporated by reference herein. Phase change memory elements can comprise Ge, Se, Sb, and/or Te (e.g.,  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ ), or other chalcogenide-comprising alloys, with other optional materials positioned between two electrodes for supplying current to the element.

A portion of the phase change material is set to a particular resistance state according to the amount of current applied via the electrodes. To obtain an amorphous state, a relatively high write current pulse (a reset pulse) is applied to the phase change cell to essentially melt a portion of the material for a first period of time. The current is removed and the cell cools rapidly to a temperature below the glass transition temperature, which results in the portion of the material retaining an amorphous phase. To obtain a crystalline state, a lower current write pulse (a set pulse) is applied to the phase change cell for a second period of time (typically longer in duration than the first period of time) to

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heat the material to a temperature below its melting point. This causes the amorphous portion of the material to crystallize or re-crystallize to a crystalline phase that is maintained once the current is removed and the cell is rapidly cooled.

As in any memory type, it is a goal in the industry to have as dense a memory array as possible, so it is desirable to increase the number of memory cells in an array of a given chip area. In pursuing this, memory arrays have been designed in multiple planes in three dimensions, stacking planes of memory cells above one another. However, it is typical in the art to require many masks per memory array level for the formation of features of the memory cells and connecting circuitry. It is not uncommon for ten to twenty masks to be required per level during fabrication.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1a shows a portion of a memory array during a stage of fabrication; FIG. 1b shows a cross-section of the array shown in FIG. 1a through line A-A.

FIG. 2a shows a portion of the memory array during a stage of fabrication subsequent to that shown in FIG. 1a; FIG. 2b shows a cross-section of the array shown in FIG. 2a through line A-A.

FIG. 3a shows a portion of the memory array during a stage of fabrication subsequent to that shown in FIG. 2a; FIG. 3b shows a cross-section of the array portion shown in FIG. 3a through line A-A.

FIG. 4a shows a portion of the memory array during a stage of fabrication subsequent to that shown in FIG. 3a; FIG. 4b shows a cross-section of the array portion shown in FIG. 4a through line A-A.

FIG. 5a shows a portion of the memory array during a stage of fabrication subsequent to that shown in FIG. 4a; FIG. 5b shows a cross-section of the array portion shown in FIG. 5a through line A-A.

FIG. 6a shows a portion of the memory array during a stage of fabrication subsequent to that shown in FIG. 5a; FIG. 6b shows a cross-section of the array portion shown in FIG. 6a through line A-A.

FIG. 7a shows a portion of the memory array during a stage of fabrication subsequent to that shown in FIG. 6a; FIG. 7b shows a cross-section of the array portion shown in FIG. 7a through line A-A.

FIG. 8a shows a portion of the memory array during a stage of fabrication subsequent to that shown in FIG. 7a; FIG. 8b shows a cross-section of the array portion shown in FIG. 8a through line A-A; FIG. 8c shows a cross-section of the array portion shown in FIG. 8a through line B-B; FIG. 8d shows a cross-section of the array portion shown in FIG. 8a through line C-C; and FIG. 8e shows a cross-section of the array portion shown in FIG. 8a through line D-D.

FIG. 9a shows a portion of the memory array during a stage of fabrication subsequent to that shown in FIG. 8a; FIG. 9b shows a cross-section of the array portion shown in FIG. 9a through line A-A; FIG. 9c shows a cross-section of the array portion shown in FIG. 9a through line B-B; FIG. 9d shows a cross-section of the array portion shown in FIG. 9a through line C-C; and FIG. 9e shows a cross-section of the array portion shown in FIG. 9a through line D-D.

FIG. 10a shows a portion of the memory array during a stage of fabrication subsequent to that shown in FIG. 9a; FIG. 10b shows a cross-section of the array portion shown in FIG. 10a through line A-A; FIG. 10c shows a cross-section of the array portion shown in FIG. 10a through line B-B; FIG. 10d shows a cross-section of the array portion



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shown in FIG. 10a through line C-C; and FIG. 10e shows a cross-section of the array portion shown in FIG. 10a through line D-D.

FIG. 11a shows a portion of the memory array during a stage of fabrication subsequent to that shown in FIG. 10a; FIG. 11b shows a cross-section of the array portion shown in FIG. 11a through line A-A; FIG. 11c shows a cross-section of the array portion shown in FIG. 11a through line B-B; FIG. 11d shows a cross-section of the array portion shown in FIG. 11a through line C-C; and FIG. 11e shows a cross-section of the array portion shown in FIG. 11a through line D-D.

FIG. 12a shows a portion of the memory array during a stage of fabrication subsequent to that shown in FIG. 11a; FIG. 12b shows a cross-section of the array portion shown in FIG. 12a through line A-A; FIG. 12c shows a cross-section of the array portion shown in FIG. 12a through line B-B; FIG. 12d shows a cross-section of the array portion shown in FIG. 12a through line C-C; and FIG. 12e shows a cross-section of the array portion shown in FIG. 12a through line D-D.

FIG. 13a shows a portion of the memory array during a stage of fabrication subsequent to that shown in FIG. 12a; FIG. 13b shows a cross-section of the array portion shown in FIG. 13a through line A-A; FIG. 13c shows a cross-section of the array portion shown in FIG. 13a through line B-B; FIG. 13d shows a cross-section of the array portion shown in FIG. 13a through line C-C; and FIG. 13e shows a cross-section of the array portion shown in FIG. 13a through line D-D.

FIG. 14a shows a portion of the memory array during a stage of fabrication subsequent to that shown in FIG. 13a; FIG. 14b shows a cross-section of the array portion shown in FIG. 14a through line A-A; FIG. 14c shows a cross-section of the array portion shown in FIG. 14a through line B-B; FIG. 14d shows a cross-section of the array portion shown in FIG. 14a through line C-C; and FIG. 14e shows a cross-section of the array portion shown in FIG. 14a through line D-D.

FIG. 15a shows a portion of the memory array during a stage of fabrication subsequent to that shown in FIG. 14a; FIG. 15b shows a cross-section of the array portion shown in FIG. 15a through line A-A; FIG. 15c shows a cross-section of the array portion shown in FIG. 15a through line B-B; FIG. 15d shows a cross-section of the array portion shown in FIG. 15a through line C-C; and FIG. 15e shows a cross-section of the array portion shown in FIG. 15a through line D-D.

FIG. 16a shows a portion of the memory array during a stage of fabrication subsequent to that shown in FIG. 15a; FIG. 16b shows a cross-section of the array portion shown in FIG. 16a through line A-A; FIG. 16c shows a cross-section of the array portion shown in FIG. 16a through line B-B; FIG. 16d shows a cross-section of the array portion shown in FIG. 16a through line C-C; and FIG. 16e shows a cross-section of the array portion shown in FIG. 16a through line D-D.

FIG. 17a shows a portion of the memory array during a stage of fabrication subsequent to that shown in FIG. 16a; FIG. 17b shows a cross-section of the array portion shown in FIG. 17a through line A-A; FIG. 17c shows a cross-section of the array portion shown in FIG. 17a through line B-B; FIG. 17d shows a cross-section of the array portion shown in FIG. 17a through line C-C; and FIG. 17e shows a cross-section of the array portion shown in FIG. 17a through line D-D.

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FIG. 18 shows a processor system incorporating a memory circuit comprising an array portion as shown in FIG. 17a.

FIG. 19 shows a block diagram of circuit connections for a three-dimensional memory array.

FIG. 20 shows a simplified circuit diagram for shared interconnect lines of a memory array.

#### DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description, reference is made to various specific embodiments of the invention. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention. It is to be understood that other embodiments may be employed and that various structural, logical and electrical changes may be made without departing from the spirit or scope of the invention.

The term “substrate” used in the following description may include any supporting structure including, but not limited to, a semiconductor substrate that has an exposed substrate surface. A semiconductor substrate should be understood to include silicon, silicon-on-insulator (SOI), silicon-on-sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. When reference is made to a substrate or wafer in the following description, previous process steps may have been utilized to form regions or junctions in or over a base semiconductor or foundation. The substrate need not be semiconductor-based, but may be any support structure suitable for supporting an integrated circuit, including, but not limited to, metals, alloys, glasses, polymers, ceramics, and any other supportive materials as is known in the art. Further, the substrate can include circuitry, such as logic or access circuitry, and insulating layers so as to provide a platform upon which to form other integrated circuit devices.

Embodiments of the invention relate to resistance variable memory devices and methods of forming a three-dimensional, i.e., stacked planes, array of such devices. Although the embodiments are described as being a phase change memory type, this is for illustrative purposes since the array architecture and methods of forming same apply broadly to other resistance variable memory types, such as, for example, programmable conductor memory, polymer memory, and others that can be used in a cross-point architecture.

The embodiments of the invention are now explained with reference to the figures, which illustrate exemplary embodiments and throughout which like reference numbers indicate like features. A portion of a phase change memory array in accordance with an embodiment of the invention is shown in FIG. 17a and FIGS. 17b, 17c, 17d, and 17e, which show various cross-sections of the array portion shown in FIG. 17a. Cross-sectional views shown in FIGS. 17b and 17d show the layout of planes 101, 103, 105, 107 of memory cells and cross-sectional views shown in FIGS. 17c and 17e show the isolation of the memory cells by insulating material.

As shown in these figures, the array 100 has a stacked configuration of phase change memory cells 102, 104, 106, and 108 (see dashed rings identifying the cells), each arranged in a plane 101, 103, 105, 107 of many memory cells, each including an electrode line, e.g., 28, a phase change material, e.g., 26, a silicide diode material, e.g., 24,

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a poly diode material, e.g., **14**, and another electrode, e.g., **12**, for memory cell **102**, which is exemplary of the other cells in the multiple planes **101**, **103**, **105**, **107**. At least the poly diode material, e.g., **14**, and electrode line, e.g., **28**, are within sidewall spacers, e.g., **20**, that define the stack dimensions of the memory cell, e.g., **102**. The diodes (e.g., materials **14** and **24**) are access devices for the memory elements, e.g., phase change material **26**. The access devices need not necessarily be diodes, but can be other two-terminal devices, such as rectifiers or threshold switching devices.

The memory cells **102**, **104**, **106**, **108** are defined at the cross-point intersections of electrode lines, e.g., **12** and **28**, **28** and **44**, **44** and **58**, **58** and **72**, and the stacked configuration of the memory cells **102**, **104**, **106**, **108** is shown by the layering of the phase change material **26**, **42**, **56**, **70**. Electrode lines, e.g., **12**, **28**, **44**, **58**, **72**, are arranged in a cross-point architecture and interconnect memory cells positioned along the same lines. Four memory cell planes **101**, **103**, **105**, **107** are shown in this way, with each such plane **101**, **103**, **105**, **107** having a two-dimensional array of multiple memory cells, e.g., in the X, Y plane. The X, Y, Z dimensions are shown in FIGS. **17a**, **17b**, and **17d**. The planes **101**, **103**, **105**, **107** of memory cells are stacked in the Z dimension so as to provide a three-dimensional array where any single memory cell can be addressed for programming or reading by its X, Y, Z coordinates. Although four such planes **101**, **103**, **105**, **107** are shown in the figures, it should be understood that fewer or greater planes of memory cells can be included in the array **100**.

Each electrode line **28**, **44**, and **58** that is not the array's **100** top-most, e.g., **72**, or bottom-most electrode line, e.g., **12**, can serve as both a bit line and as a wordline in addressing memory cells for programming and reading. As shown in FIG. **17b**, for example, the electrode line **28** is configured so that it serves as a bit line for memory cell **102** and as a wordline for memory cell **104** as each respective memory cell **102**, **104** is addressed for reading or writing. Although the terms bit line and wordline originated in relation to dynamic random access memory (DRAM) technology to indicate the line carrying stored information signal and the line carrying an access control signal, respectively, herein they are used to indicate two cross-point arranged, intersecting, interconnect lines for addressing a memory cell in a memory array and just as well could be called row lines and column lines or simply, interconnect lines.

The structure of the array **100** allows the central array planes, i.e., not necessarily the top-most or bottom-most, such as the planes **103** and **105** incorporating memory cells **104** and **106**, respectively, to be fabricated with a single mask per plane and, potentially, a single mask pattern for all such planes, which makes processing faster, simpler, and less expensive when compared to techniques requiring multiple masks for memory array layer fabrication. Because the memory cells, e.g., **104**, are composed of stacks of layers defined by the dimensions of a hard mask (FIGS. **2b** to **16e**) **16**, **32**, **48**, **62**, and sidewall spacers **36**, **54**, **68**, the photolithographic mask (e.g., FIG. **8d**, **34**) that defines the hard mask, e.g., **32**, dimension (when etched) is the only mask needed during the fabrication of the respective memory cell plane. The formation of the sidewall spacers during processing, which does not require another mask, completes the definition of the memory cell dimensions and, so, only a single mask is needed.

This cross-point arrangement of the array **100** structure allows for a self-aligned process in forming the memory elements. A self-aligned memory element enables higher

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density memory arrays in a production environment than would be feasible with memory elements which must have other layers aligned, such as contacts. Masking techniques such as pitch multiplication, as described in U.S. patent application Ser. Nos. 11/214,544 and 11/514,117, and U.S. Pat. No. 5,328,810, incorporated herein by reference, may be utilized in accordance with the invention.

A self-aligned cross-point structure created with an orthogonal line/space pattern allows high density lines without the tight alignment/registration normally required for memory element fabrication. Typically, the maximum allowed registration error is  $\frac{1}{3} f$  (where  $f$  is the minimum feature line/space dimension), but with a self-aligned cross-point technology, the only alignment requirement is in connecting the ends of the lines to drivers and sense devices. While this involves some overhead of area at the edges of the array **100**, it allows one to approach a  $4f$  footprint per memory element at very small dimensions for  $f$ , e.g., about 18-50 nm. Stacking such memory elements in the way described herein makes the memory array density even higher and approaches a  $4f$  footprint/memory element for a 4-tier stack of such memory elements as shown in FIGS. **17b-17e**. Thus, higher density product is enabled by a stacked self-aligned cross-point memory element structure as described and claimed herein.

FIG. **20a** shows how this array **100** configuration includes a driver **300** and sense **302** circuit connected to each of the central electrode lines **28**, **44**, and **58** such that the driver circuit **300** of a respective electrode line, e.g., **28**, is used with the memory cell **104** of one plane of memory cells, and the sense circuit of that respective line, e.g., **28**, is used with the memory cell **102** of an adjacent plane, e.g., **101** (FIG. **17b**) of memory cells. The memory cell **104** (also FIG. **17b**) can be connected to driving and sensing circuitry by the interconnect electrode lines **28** and **44** and access devices **304**, such as gated transistors. When one of the driver **300** and sense circuit **302** is active on a given electrode line, the other is disabled.

The electrode line **28** has a sense circuit **302** and a driver circuit **300** that can be connected to the terminal ends of the line **28** by a via to a local interconnect and respective select gates **304**. A select gate **304** can be used to decouple the driver **300** from and couple the sensor **302** to the desired line **28** when the respective cell **104** is read. When the respective cell **104** is written the opposite takes place; another select gate **304** can decouple the line **28** from the sense circuit **302** and the line **28** is coupled to the driver **300**. Of course, during this operation, another line **44** is also enabled by similar circuitry to address the respective cell. Alternatively, as a possible space-saving and/or fabrication simplifying arrangement, the driver circuit **300** and sensing circuit **302** can be connected to the electrode line **28** at the same terminal end.

The stacked memory cell and shared bit line/wordline array **100** architecture allows for a higher density memory array **100** with fewer masks needed during fabrication. Also, this configuration provides a lower cost in forming the array **100** and a simpler array layout. The periphery circuitry compensates for the simpler memory array layout to control the common wordlines and bit lines, i.e., the layers of electrode lines **28**, **44**, and **58**, and utilizes select gates to float circuitry not being used.

FIG. **19** shows how the memory array **100** can be connected with addressing, programming, and readout circuitry. Each level **200** of electrode lines **12**, **28**, **44**, **58**, **72** is in electrical connection with a write access device **202** and a sense access device **204**, for example, an access transistor.

The access devices **202**, **204** electrically connect the electrode lines **12**, **28**, **44**, **58**, **72**, and thereby, the memory cells **102**, **104**, **106**, **108** (FIGS. **17b** and **17d**), which are between the representative electrode line levels **200**, to row/column decode/enable circuitry **206**. The row/column decode/enable circuitry **206** connects to timing and control circuitry **208** and row driver circuitry **212**, and to input/output buffer/port circuitry **210** and sense and amplifier circuitry **214**. As indicated above, the connections to the addressing, programming, and readout circuitry can be provided at both terminal ends of the lines, e.g., **28**, or at a single end of the lines, e.g., **28**.

According to an embodiment of the invention, the array **100** undergoes a biasing scheme in which unselected, surrounding bit lines and unselected wordlines the same level of an addressed memory cell are allowed to float, while simultaneously the selected, addressing bit line-wordline pair is subjected to a current pulse so as to cause the diode structure in the target memory cell to be pulsed in a forward bias direction. The direction of the forward bias current in the target memory cell, e.g., **104**, is consistent with the voltage difference  $V_m - V_{to}$ , which will induce the required programming current in the phase change material of the cell, e.g., **104**. This current pulse may be induced by a conventional voltage pulse having a magnitude of 2.5 volts. This biasing scheme combined with the diode structure of the memory cells provides reduced leakage current in the array. With reduced leakage current, the array **100** can be used in a wide range of applications, including as part of a dedicated memory device used in applications in which power consumption is a concern such as portable devices.

FIGS. **1a** to **17e** show stages of fabrication of a memory array **100** in accordance with an embodiment. FIGS. **1a** and **1b** show a substrate **10** upon which the array **100** can be fabricated. FIG. **1a** shows the substrate from a top view and FIG. **1b** shows the substrate **10** through cross-section A-A. The substrate **10** can include logic circuits and all support circuitry (FIG. **19**), formed on a semiconductor material under the area that will support the memory array **100** (FIG. **17b**, for example). Preferably, the substrate is covered with an insulator layer **11**, such as an oxide or silicon nitride layer, planarized to the tops of the support circuitry by chemical mechanical polishing if desired. These structures are not shown, but can be formed according to standard processing techniques known in the art.

As shown in FIGS. **2a** and **2b**, a layer of metal **12** can be deposited over the substrate **10** and insulating material **11**. The metal layer **12** can comprise conductive materials such as titanium (Ti), tungsten (W), tungsten nitride (WN), titanium nitride (TiN), titanium tungsten (TiW), carbon (C), silicon carbide (SiC), titanium aluminum nitride (TiAlN), titanium silicon nitride (TiSiN), polycrystalline silicon, tantalum (Ta), tantalum nitride (TaN), platinum (Pt), silver (Ag), gold (Au), and combinations of such materials, for example a stack of TiN/WN/W with the TiN against the next-formed poly diode material **14**, and can be deposited by known techniques, such as chemical vapor deposition, plasma enhanced chemical vapor deposition, evaporative techniques, and other methods. The metal layer **12** is preferably formed to be about 20 Å to about 2,000 Å thick. A diode layer **14** can be formed over the metal layer **12**. The poly diode material layer **14** can be made of p-type poly-Si, which with later-formed silicide (e.g., CoSi<sub>2</sub> metal), forms Schottky barrier and backside (ohmic) contact structures and can be formed by known methods as well. A hard mask layer **16** is formed over the poly diode material layer **14**. The hard mask **16** can be a nitride material and is preferably formed

to be about 20 Å to about 4,000 Å thick. As shown in FIGS. **2a** and **2b**, the metal layer **12**, poly diode material layer **14**, and hard mask layer **16** are formed as a blanket across the substrate **10** and insulating layer **11**.

As shown in FIGS. **3a** and **3b**, the hard mask **16** is patterned with a photoresist mask **18**. As shown in FIGS. **4a** and **4b**, the hard mask **16**, poly diode material layer **14**, and metal layer **12** are etched using mask **18** down to the substrate **10**, or insulator **11** (which is shown in FIG. **4b**), to leave stacked lines of these layers **12**, **14**, **16**. As shown in FIGS. **5a** and **5b**, sidewall spacers **20** are formed on the sides of the stacked lines of metal layer **12**, diode layer **14**, and hard mask **16**. These sidewall spacers **20** are formed by deposition, for example, of a nitride material or silicon oxide (SiO<sub>x</sub>) and can be deposited by atomic layer deposition over the stacked lines **12**, **14**, and **16** and then etched to leave the sidewall spacers **20**. A dielectric layer **22** is then formed over the substrate **10** and insulating layer **11**, covering the sidewall spacers **20** and hard mask **16**. The dielectric layer **22** is then planarized to expose the hard mask **16**. The dielectric layer **22** can be made of many known insulative materials, but is preferably silicon oxide (Si<sub>3</sub>O<sub>2</sub>).

As shown in FIGS. **6a** and **6b**, the hard mask **16** is removed selective to the dielectric **22** and diode layer **14**. The poly diode material layer **14** is then selectively coated with a silicide diode material **24**, such as CoSi<sub>2</sub>, which is treated to enhance electron injection into a phase change material to be formed thereover. This treatment can include forming one or more nanoparticles on the silicide diode material **24**, forming a band engineered crested barrier over the material **24**, or roughening the surface of the material **24** to increase its ability to produce high electric fields. Formation of the silicide material **24** over the poly diode material **14** creates a Schottky diode structure.

As shown in FIGS. **7a** and **7b**, phase change material, such as Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> (commonly referred to as GST), for example, is formed as a layer **26** over the silicide diode material **24** and dielectric layer **22**. Other known phase change materials can be used for layer **26**. The phase change material layer **26** can be deposited by sputtering, or other known techniques. An electrode layer **28** is formed over the phase change material layer **26** and can comprise metal or other conductive material. Preferably, the electrode layer **28** comprises the same material, e.g., TiN/WN/W, as metal layer **12** and is formed to similar dimensions. This electrode layer **28** completes the material layering for first plane **101** (FIG. **17b**) of memory cells, including cell **102** (FIG. **17b**), and also begins the material layering for next overlying plane **103** (FIG. **17b**) of memory cells, including cell **104** (FIG. **17d**), of the memory array **100**.

Another poly diode material layer **30** can be formed over the electrode layer **28** and preferably comprises the same material, e.g., p-type poly, as diode layer **14**. Another hard mask **32** is formed over the diode layer **30**. This hard mask **32** can comprise the same material, e.g., nitride, as the first hard mask **16**. As shown by FIGS. **8a** and **8b**, the hard mask **32** is patterned with a photoresist mask **34**. The photolithographic pattern for the photoresist mask **34** can be specifically designated and original for this plane **101** (FIG. **17b**) of cells, or the patterned mask used to form the photoresist mask **18** (FIG. **3b**) can be rotated 90 degrees and reused.

FIG. **8b** shows a cross-section of the substrate **10** portion shown in FIG. **8a** through line A-A, which runs through the photoresist mask **34**. FIG. **8c** shows a cross-section of the substrate **10** portion of FIG. **8a** through line B-B, which does not run through the photoresist mask **34**. FIG. **8d** shows a cross-section of the substrate portion **10** of FIG. **8a** through

line C-C, which is orthogonal to the cross-sections through lines A-A and B-B and through one of the stacked lines of layers 12, 14, and 24. FIG. 8e shows a cross-section of the substrate 10 portion shown in FIG. 8a through line D-D, also orthogonal to lines A-A and B-B, which runs through the dielectric layer 22. The cross-section lines A-A, B-B, C-C and D-D are respectfully maintained throughout the figures.

As shown in FIGS. 9a, 9d, and 9e, using the respective single, patterned, photoresist mask 34, the hard mask 32, poly diode material layer 30, and electrode layer 28 are etched to the phase change material layer 26 to leave stacked lines of these layers 28, 30, 32, which can be orthogonal to the underlying lines of layers 12, 14 and 24. As shown in FIG. 9b, layers 28, 30, and 32 are present through line A-A, but as shown in FIG. 9c, they are not present through line B-B.

FIGS. 10a, 10d, and 10e show that sidewall spacers 36 are formed on the sides of the stacked layers 28, 30, and 32. As explained above with regard to sidewall spacers 20, sidewall spacers 36 can be formed by depositing an insulating layer, e.g., silicon oxide or nitride material, over the stacked layers 28, 30, and 32 and etching. Next, as shown in FIGS. 11a, 11b, 11c, 11d, and 11e, the sidewall spacer 36 etch is continued through the phase change material layer 26 and silicide layer 24 to stop at the poly diode material 14 and singulate the silicide diode material layer 24 to prevent cross-talk among memory cells, e.g., 102 (FIG. 17b). Alternatively, this etch may be carried through the poly diode material 14 and stop on layer 12, which singulates the entire diode structure. This etching of the sidewall spacers 36 does not require another mask and completes the definition of the memory cell 102. A dielectric 38 is deposited to fill the trenches formed by the sidewall spacer 36 etch. The dielectric 38 can be planarized to the hard mask 32. Next, the hard mask 32 is removed selective to the dielectric 38 and poly diode material layer 30. The poly diode material layer 30 is then selectively coated with a silicide material 40, which is treated, e.g., by roughening, forming nanoparticles or crested barrier, etc., to enhance electron injection into a phase change material to be formed thereover. This silicide material layer 30, with the poly diode material 30, forms a Schottky diode.

As shown in FIGS. 12a, 12b, 12c, 12d, and 12e, a phase change material, such as GST, for example, is formed as a layer 42 over the silicide 40 and dielectric layer 38. Other phase change materials can also be used. The phase change material layer 42 can be deposited by sputtering, or other known techniques. An electrode layer 44 is formed over the phase change material layer 42 and can comprise metal or other conductive material. Preferably, the electrode layer 44 comprises the same material as metal layer 12 and electrode layer 28, e.g., a TiN/WN/W stack, and is formed to similar dimensions. This electrode layer 44 completes the material layering for a second plane 103 (FIG. 17b) of memory cells, including cell 104 (FIG. 14b), and begins as the first material layer for the overlying plane 105 (FIG. 17b) of memory cells, including cell 106 (FIG. 17b), of the memory array 100.

Another poly diode material layer 46 can be formed, for example, of p-type poly, over the electrode layer 44 and preferably comprises the same material as diode layers 14 and 30. Another hard mask 48 is formed over the poly diode layer 46. This hard mask 48 can comprise the same material, e.g., nitride, as the first hard mask 16 and second hard mask 32. A patterned photoresist mask 49 is formed over the hard mask 48. No more than this single mask is needed in forming the respective plane 103 (FIG. 17b) of memory cells, e.g.,

104 (FIG. 14b). As with the patterned mask 34, the pattern used to form mask 18 can be reused to form mask 49 if rotated back 90 degrees from the alignment use to form mask 34 or an original designated pattern can be used. Whether an original and plan-specific or reused and rotated mask is used, no more than a single mask per central memory cell plane, e.g., plane 103 including memory cell 104, is required.

FIGS. 13a, 13b, and 13c show that, as discussed above in relation to the processing steps shown in FIGS. 9a, 9d, and 9e, the hard mask 48 is etched to the phase change layer 42 to leave stacks of layers 44, 46, and 48. FIGS. 14a, 14b, and 14c show that sidewall spacers 54 are formed on the sides of the stacked layers 44, 46, and 48 (hard mask 48 is shown in FIG. 13b, for example). As explained above with regard to sidewall spacers 20 and 36, sidewall spacers 54 can be formed by depositing an insulating layer over the stacked layers 44, 46, and 48 and etching. The sidewall spacer 54 etch is continued through the phase change material layer 42 and silicide diode material layer 40 to singulate the silicide diode material layer 40 to prevent cross-talk among memory cells, e.g., 104 (FIG. 17d). This etch step defines the stacked memory cell 104. Alternatively, this etch may be carried through the poly diode material 30 and stop on layer 28, which singulates the entire diode structure.

Next, as also shown in FIGS. 14b, 14c and 14e, a dielectric 50 is deposited to fill the trenches formed by the sidewall spacer 54 etch. The dielectric 50 can be planarized to the hard mask 48 (e.g., FIG. 13b). Next, the hard mask 48 is removed selective to the dielectric 46 and poly diode material layer 50. The poly diode layer 46 is then selectively coated with a silicide diode material 52, such as CoSi<sub>2</sub>, which is treated, e.g., by roughening or adding nanoparticle (s) or forming a crested barrier, for enhancing electron injection into a phase change material to be formed thereover. The silicide diode material 52 forms a Schottky diode with the poly diode material 50.

As shown in FIGS. 15a, 15b, 15c, 15d, and 15e, a phase change material, such as GST, for example, is formed as a layer 56 over the silicide diode material 52 and dielectric layer 50. However, other phase change materials can be used also. The phase change material layer 56 can be deposited by sputtering, or other known techniques. An electrode layer 58 is formed over the phase change material layer 56 and can comprise metal or other conductive material. Preferably, the electrode layer 58 comprises the same material, e.g., TiN/WN/W, as metal layer 12, electrode layer 28, and electrode layer 44 and is formed to similar dimensions. This electrode layer 58 completes the material layers for a third plane 105 (FIG. 17b) of memory cells, including cell 106 (FIG. 17d), and begins as the first material layer for the overlying plane 107 (FIG. 17b) of memory cells, including cell 108 (FIG. 17b), of the memory array 100. Another poly diode layer 60 can be formed over the electrode layer 58 and preferably comprises the same material, e.g., p-type poly, as diode layers 14, 30, and 46. Another hard mask 62 is formed over the poly diode layer 60. This hard mask 62 can comprise the same material, e.g., nitride, as the hard masks 16, 32, and 48.

FIGS. 16a, 16d, and 16e show that, as discussed above in relation to the processing steps shown in FIGS. 9a and 13a, the hard mask 62 is patterned with photoresist (not shown) and etched to the phase change layer 56 to leave stacks of layers 58, 60, and 62. Again, this is the only patterned mask needed in forming this plane 105 (FIG. 17b) of memory cells and can be an original pattern or the pattern used to form mask 34 can be reused. Whether an original or reused mask

is used, no more than a single mask per central memory cell plane, such as plane 105 including memory cell 106, is required.

FIGS. 16*d* and 16*e* show that sidewall spacers 68 are formed on the sides of the stacked layers 58, 60, and 62 (hard mask 62 is shown in FIG. 15*d*, for example). As explained above with regard to sidewall spacers 20, 36, and 54, sidewall spacers 68 can be formed by depositing an insulating layer, e.g., silicon oxide or nitride, over the stacked layers 58, 60, and 62 and etching. The sidewall spacer 68 etch is continued through the phase change material layer 56 and silicide diode layer 52 to stop at the poly diode layer 50 and singulate the silicide diodes layer 52 to prevent cross-talk among memory cells, e.g., 106 (FIG. 17*b*). Alternatively, this etch may be carried through the poly diode material 46 and stop on layer 44, which singulates the entire diode structure. Next, as also shown in FIGS. 16*a*, 16*c*, 16*d*, and 16*e*, a dielectric 64 is deposited to fill the trenches formed by the sidewall spacer 68 etch. The dielectric 64 can be planarized to the hard mask 62. Next, the hard mask 62 is removed selective to the dielectric 64 and poly diode layer 60. The poly diode layer 60 is then selectively coated with a silicide diode material 66, which is treated for high electron injection for phase change material to be formed thereover; this forms a Schottky diode.

As shown in FIGS. 17*a*, 17*b*, 17*c*, 17*d*, and 17*e*, a phase change material, such as GST, for example, is formed as a layer 70 over the silicide diode material 66 and dielectric layer 64. Again, other phase change materials can be used. The phase change material layer 70 can be deposited by sputtering, or other known techniques. An electrode layer 72 is formed over the phase change material layer 70 and can comprise metal or other conductive material. Preferably, the electrode layer 70 comprises the same material, e.g., TiN/WN/W, as metal layer 12 and electrode layers 28, 44, and 58 and is formed to similar dimensions. This electrode layer 58 completes the material layers for a fourth plane 107 of memory cells, including cell 108, of the memory array 100.

Another hard mask 74 is formed over the electrode layer 72. Note, since this is the top electrode 72 stack in this embodiment, no diode need be included; however, this need not necessarily be the top electrode and additional planes of memory cells could be included in the array 100 if desired. The hard mask 74 can comprise the same material, e.g., nitride, as the hard masks 16, 32, 48, and 62 and is preferably formed to the same dimensions. FIGS. 17*a*, 17*b*, and 17*c* show that, as discussed above in relation to the processing steps shown in FIGS. 9*a*, 13*a*, and 16*a*, the hard mask 74 can be patterned with photoresist (not shown) and etched through the phase change layer 70 and silicide diode layer 66 to leave stacks of layers 66, 70, 72, and 74. Alternatively, this etch may be carried through the poly diode material 60 and stop on layer 58, which singulates the entire diode structure. Note, no sidewall spacers are necessarily included in this top-most stack. Next, as also shown in FIGS. 17*a*, 17*b*, 17*c*, and 17*e*, a dielectric 76 is deposited to fill the trenches formed defining the stacks of layers 68, 70, 72, and 74. The dielectric 76 can be planarized to the hard mask 74.

The method and structures described in relation to FIGS. 1*a* through 17*e*, 19 and 20 provide a simpler and less expensive fabrication for a three-dimensional memory array. Because no more than a single patterned mask is required to fabricate memory cell planes 103 and 105, which are the central planes of the embodiment shown, many processing steps required of prior techniques, including the use of multiple, often many, patterned masks per layer of memory cells, can be omitted from the fabrication. Further, the use of

shared interconnect lines, e.g., 44, further simplifies the array structure and also conserves valuable array landscape for other features, making for a denser memory device.

The above-described processing techniques for fabricating a memory device allow the use of a 248 nm (photolithographic) scanner, which may initially create 200 nm pitch line/space pairs with 34 nm alignment control. The array features can then be pitch multiplied to create masks of 50 nm pitch line/space pairs (nominally 25 nm each) on each array 100 level. Because there is no tight alignment requirement in fabricating the array, one does not need the typical  $f/3$  of 8 nm alignment budget that would require a state of the art photo tool (which could cost between about \$40-45 million) and may instead use a 248 nm photo tool (which typically cost between about \$15-20 million) to create high density memory products. Thus manufacturing costs can be significantly reduced by use of the above-described processes, which allow for loosening the alignment requirement of the memory array.

FIG. 18 illustrates a simplified processor system 400, such as a computer, including a memory circuit 448 employing an array of phase change memory devices as shown in FIGS. 17*a*-17*e* fabricated in accordance with the invention. A processor system, such as a computer system, generally comprises a central processing unit (CPU) 444, such as a microprocessor, a digital signal processor, or other programmable digital logic devices, which communicates with an input/output (I/O) device 446 over a bus 452. The memory circuit 448 communicates with the CPU 444 over bus 452, typically through a memory controller.

In the case of a computer system, the processor system may include peripheral devices, such as a floppy disk drive 454 and a compact disc (CD) read only memory (ROM) drive 456, which also communicate with CPU 444 over the bus 452. Memory circuit 448 is preferably constructed as an integrated circuit. If desired, the memory circuit 448 may be combined with the processor, for example CPU 444, in a single integrated circuit.

The above description and drawings should only be considered illustrative of exemplary embodiments that achieve the features and advantages described herein. Modification and substitutions to specific process conditions and structures can be made. Accordingly, the claimed invention is not to be considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.

The invention claimed is:

1. A method, comprising:

identifying an access operation for one or more memory cells that comprises a phase change element in series with a diode;

decoupling, based at least in part on the access operation, a first access circuit from a first electrode line of a first plane of a plurality of parallel planes that is coupled with the diode, wherein the first access circuit is one of a sense circuit or a driver circuit;

coupling, based at least in part on the access operation, a second access circuit with a second electrode line of a second plane of the plurality of parallel planes that is coupled with the phase change element;

coupling, based at least in part on the access operation, a third access circuit with the first electrode line, wherein the third access circuit is the other of the sense circuit or the driver circuit; and

performing the access operation for the one or more memory cells using the coupled second access circuit or the coupled third access circuit.

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2. The method of claim 1, wherein the access operation comprises a write operation,  
and wherein the third access circuit comprises the sense circuit, the method further comprising:  
coupling the third access circuit with the first electrode line after decoupling the first access circuit, wherein the third access circuit comprises the driver circuit.
3. The method of claim 1, wherein the access operation comprises a read operation,  
and wherein the third access circuit comprises the driver circuit, the method further comprising:  
coupling the third access circuit with the first electrode line after decoupling the first access circuit, wherein the third access circuit comprises the sense circuit.
4. The method of claim 1, wherein at least one of the first electrode line or the second electrode line is shared with one or more second memory cells.
5. The method of claim 1, further comprising:  
decoupling the first access circuit from the first electrode line using a first device; and  
decoupling a coupling the third access circuit with the first electrode line using a second device, wherein the first device and the second device are at different terminal ends of the first electrode line.
6. The method of claim 5, wherein the first device and the second device each comprise a select gate transistor.
7. The method of claim 1, further comprising:  
decoupling the first access circuit from the first electrode line using a first device; and  
decoupling a coupling the third access circuit with the first electrode line using the first device, wherein the first access circuit and the third access circuit are at a same terminal end of the first electrode line.
8. The method of claim 7, wherein the first device comprises a select gate transistor.
9. The method of claim 1, wherein the first electrode line and the second electrode line are arranged in a cross point architecture.
10. An apparatus, comprising:  
one or more memory cells comprising a phase change element in series with a diode;  
a first electrode line of a first plane of a plurality of parallel planes coupled with the diode;  
a second electrode line of a second plane of the plurality of parallel planes coupled with the phase change element;  
a first access circuit selectively couplable with the first electrode line;  
a second access circuit selectively couplable with the second electrode line;  
a third access circuit selectively couplable with the first electrode line; and  
one or more controllers operable to:  
identify an access operation for the one or more memory cells;  
decouple, based at least in part on identifying the access operation for the one or more memory cells, the first access circuit from the first electrode line, wherein the first access circuit is one of a sense circuit or a driver circuit;  
couple, based at least in part on the access operation, the second access circuit with the second electrode line;  
couple, based at least in part on the access operation, a third access circuit with the first electrode line, wherein the third access circuit is the other of the sense circuit or the driver circuit; and

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- perform the access operation for the one or more memory cells using the coupled second access circuit or the coupled third access circuit.
11. The apparatus of claim 10, wherein the first access circuit comprises the sense circuit, and wherein the one or more controllers are further operable to:  
couple the third access circuit with the first electrode line after decoupling the first access circuit, wherein the third access circuit comprises the driver circuit, and wherein the access operation comprises a write operation.
12. The apparatus of claim 10, wherein the first access circuit comprises the driver circuit, and wherein the one or more controllers are further operable to:  
couple the third access circuit with the first electrode line after decoupling the first access circuit, wherein the third access circuit comprises the sense circuit, and wherein the access operation comprises a read operation.
13. The apparatus of claim 10, wherein at least one of the first electrode line or the second electrode line is shared with one or more second memory cells.
14. The apparatus of claim 10, further comprising:  
a first device at a first terminal end of the first electrode line; and  
a second device at a second terminal end of the first electrode line, wherein the one or more controllers are further operable to:  
decouple the first access circuit from the first electrode line using the first device; and  
couple the third access circuit with the first electrode line using the second device.
15. The apparatus of claim 10, further comprising:  
a first device coupled with the first electrode line, wherein the one or more controllers are further operable to:  
decouple the first access circuit from the first electrode line using the first device; and  
couple the third access circuit with the first electrode line using the first device, wherein the first access circuit and the third access circuit are at a same terminal end of the first electrode line.
16. An apparatus, comprising:  
one or more memory cells comprising a phase change element in series with a diode;  
a first electrode line of a first plane of a plurality of parallel planes coupled with the diode;  
a second electrode line of a second plane of the plurality of parallel planes coupled with the phase change element;  
a first access circuit configured to be decoupled from the first electrode line based at least in part on an access operation for the one or more memory cells, wherein the first access circuit is one of a sense circuit or a driver circuit;  
a second access circuit configured to be coupled with the second electrode line based at least in part on the access operation; and  
a third access circuit configured to be coupled with the first electrode line based at least in part on the access operation, wherein the third access circuit is the other of the sense circuit or the driver circuit, and wherein the access operation for the one or more memory cells can be performed using the coupled second access circuit or the coupled third access circuit.
17. The apparatus of claim 16,  
wherein the first access circuit comprises the sense circuit, wherein the third access circuit comprises the driver

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circuit and is configured to be coupled with the first electrode line after decoupling the first access circuit, and wherein the access operation comprises a write operation.

**18.** The apparatus of claim **16**,  
wherein the first access circuit comprises the driver circuit, wherein the third access circuit comprises the sense circuit and is configured to be coupled with the first electrode line after decoupling the first access circuit, and wherein the access operation comprises a read operation.

**19.** The apparatus of claim **16**, further comprising:  
a first device configured to decouple the first access circuit from the first electrode line based at least in part on the access operation, the first device at a first terminal end of the first electrode line; and  
a second device configured to couple the third access circuit with the first electrode line, the second device at a second terminal end of the first electrode line.

**20.** The apparatus of claim **16**, further comprising:  
a first device configured to decouple the first access circuit from the first electrode line and couple the third access circuit with the first electrode line based at least in part on the access operation, wherein the first access circuit and the third access circuit are at a same terminal end of the first electrode line.

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