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Method for manufacturing semiconductor structure

Abstract

The invention provides a semiconductor structure, which comprises a chip comprising a substrate, wherein the substrate has a front surface and a back surface, and the front surface of the substrate comprises a circuit layer, the back surface of the substrate comprises a plurality of microstructures, and a thermal interface material located on the back surface of the substrate, and the thermal interface material contacts the microstructures directly.

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Background/Summary

CROSS REFERENCE TO RELATED APPLICATIONS [0001] This application is a division of U.S. Application Ser. No. 17/891,090, filed on Aug. 18, 2022. The content of the application is incorporated herein by reference.

BACKGROUND OF THE INVENTION
1. Field of the Invention
[0002] The invention relates to the field of semiconductor manufacturing, in particular to a semiconductor structure for improving the heat dissipation efficiency of a chip and a manufacturing method thereof.
2. Description of the Prior Art
[0003] With the progress of semiconductor manufacturing, the size of semiconductor chips is getting smaller and smaller, so the semiconductor chips need to accommodate more components in a limited chip area. At the same time, as the performance requirements of the chips are gradually increased, it is easier for the semiconductor chips to generate heat when running them efficiently. If the semiconductor chip is overheated, the performance of the semiconductor chip will be reduced or even damaged. Therefore, it is one of the research directions in this field to improve the heat dissipation effect of semiconductor wafers without increasing excessive cost.
SUMMARY OF THE INVENTION
[0004] The invention provides a semiconductor structure, which comprises a chip, wherein the chip comprises a substrate, wherein the substrate has a front side and a back side, and the front side of the substrate comprises a circuit layer disposed thereon, the back side of the substrate comprises a plurality of microstructures, and a thermal interface material located on the back side of the substrate, and the thermal interface material directly contacts the microstructures.
[0005] The invention also provides a manufacturing method of a semiconductor structure, which comprises providing a substrate, wherein the substrate has a front surface and a back surface, forming a circuit layer on the front surface of the substrate, forming a plurality of microstructures on the back surface of the substrate, and forming a thermal interface material on the back surface of the substrate, wherein the thermal interface material directly contacts the microstructures.
[0006] The present invention is characterized in that a plurality of microstructures (such as holes or grooves) are formed on the back surface of the substrate of the wafer, and then the thermal interface material is filled into the microstructures, and the heat sink is connected to the thermal interface material. Because the microstructure increases the surface area of the back of the substrate, the heat dissipation efficiency of the semiconductor chip can be improved after the thermal interface material is filled in the microstructure. The invention has the advantages of compatibility with existing processes and improvement of the efficiency of semiconductor chips.
[0007] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0008] FIG. **1** to FIG. **4** are schematic diagrams of manufacturing a semiconductor structure

according to the first embodiment of the present invention.
[0009] FIG. **5** is a schematic diagram of a semiconductor structure according to another embodiment of the present invention.
DETAILED DESCRIPTION
[0010] To provide a better understanding of the present invention to users skilled in the technology of the present invention, preferred embodiments are detailed as follows. The preferred embodiments of the present invention are illustrated in the accompanying drawings with numbered elements to clarify the contents and the effects to be achieved.
[0011] Please note that the figures are only for illustration and the figures may not be to scale. The scale may be further modified according to different design considerations. When referring to the words “up” or “down” that describe the relationship between components in the text, it is well known in the art and should be clearly understood that these words refer to relative positions that can be inverted to obtain a similar structure, and these structures should therefore not be precluded from the scope of the claims in the present invention.
[0012] Please refer to FIG. **1** to FIG. **4**, which are schematic diagrams of manufacturing the semiconductor structure of the present invention. First, as shown in FIG. **1**, a substrate **10**, such as a silicon wafer, or other substrates commonly used in semiconductor processes, such as a group III-V element substrate (group III-V element such as gallium nitride), a silicon germanium substrate, a silicon carbide substrate, a silicon-on-insulator, SOI), etc., can be applied to the substrate of the present invention, and the present invention is not limited thereto. The substrate **10** includes a front surface **10**A and a back surface **10**B. The front surface **10**A of the substrate **10** is formed with a circuit layer **12**. The circuit layer **12** includes various types of electronic components (such as common transistors, resistors, capacitors, memories, wires, contact structures, etc., but is not limited to this), and the circuit layer **12** may be composed of multiple layers stacked on each other. Here, the circuit layers **12** have different combinations according to the functions of the wafer to be formed, and the fabrication method and structure of the circuit layers **12** belong to the conventional technology in the field, so they will not be described in detail here. In addition, the substrate **10** (for example, a wafer) described here will be cut into a plurality of dies by a cutting step in the subsequent steps, which will be described in the subsequent paragraphs.
[0013] Referring to FIG. **1**, in some embodiments of the present invention, a thinning step P**1** can be selectively performed on the back surface **10**B of the substrate **10**, wherein the thinning step P**1** is, for example, a chemical mechanical polishing (CMP) to reduce the thickness of the substrate **10** to meet the specification requirements of semiconductor wafers. In addition, reducing the thickness of the substrate also helps to improve the heat dissipation effect of the semiconductor wafer. However, it is worth noting that in other embodiments of the present invention, the thinning step P**1** described in FIG. **1** can be selectively omitted, that is, after the circuit layer **12** is formed on the substrate **10**, the next step can be directly performed without the thinning step. This embodiment also belongs to the scope of the present invention.
[0014] Then, as shown in FIG. **2**, a photolithography and etching step P**2** is performed on the back surface **10**B of the substrate **10** to form a plurality of microstructures **14** on the back surface **10**B of the substrate **10**, wherein the microstructures **14** here include, for example, a plurality of grooves or holes, and the difference between the grooves and the holes is that, from a top view, the grooves may have a long strip structure, while the holes may have a round hole or a square hole-like structure, and the microstructures **14** may also include the combination of grooves and holes. Besides, the depth, the opening size and the spacing of the grooves and holes may be the same or different, all of which belong to the scope of the present invention. In addition, a bottom surface **14**A of the microstructure **14** is defined here.
[0015] In addition, the density and distribution of grooves and holes can also be adjusted in other embodiments of the present invention. For example, the density of the grooves or the holes can be increased in a component dense area of the wafer, and the density of the grooves or the holes can

be decreased in other peripheral areas, etc. Such embodiments also belong to the scope of the present invention.

[0016] The purpose of forming the microstructure **14** here is to increase the surface area of the back surface **10**B of the substrate **10**. In the subsequent step, a thermal interface material (TIM) will be coated or attached to the back surface **10**B of the substrate **10**. If the surface area of the back surface **10**B of the substrate **10** is increased, the heat dissipation effect of the substrate can be further improved.

[0017] Then, as shown in FIG. **3**, after the microstructure **14** is formed, a cutting step P**3** is performed to cut the substrate **10** (for example, a whole wafer structure) into a plurality of dies D. Here, the difference between the die and the chip according to the present invention will be explained. As shown in FIG. **3**, the structure of the substrate **10** and the circuit layer **12** after cutting is defined as the die D, which will be packaged in the subsequent step, and the packaged die D is defined as the chip.

[0018] Next, the cut die D is packaged to form a chip, and is electrically connected to the printed circuit board, and a thermal interface material and heat sink are formed therein. The technical content of packaging belongs to the conventional technology in the field, so it will not be repeated here. Specifically, as shown in FIG. **4**, a printed circuit board **16** is provided, and then a packaging step is carried out, and the die D shown in FIG. **3** is packaged to form a chip C, and the circuit layer **12** of the chip C can be electrically connected to the printed circuit board **16** by means of solder B, pins or wires, etc. The technical content of this part belongs to the conventional technology in the field, so it will not be repeated here. It is worth noting that, in order to improve the heat dissipation effect of the packaged chip, a heat sink **20** can be connected to the thermal interface material **18** by coating or attaching the thermal interface material **18** on the back surface **10**B of the substrate **10**. The thermal interface material **18** in the present invention is, for example, a glue layer containing metal particles, wherein the metal particles can be selected from metals with better thermal conductivity, such as silver particles. The thermal interface material **18** used in the present invention is formed by mixing the metal particles with the glue layer. The thermal interface material **18** fills into the microstructure **14**, and the thermal interface material **18** directly contacts the bottom surface **14**A of the microstructure **14** (such as the grooves or the holes), so as to improve the heat dissipation effect of the back surface **10**B of the substrate **10**. In addition, the thermal interface material **18** is connected to the heat sink **20**. The heat sink **20** here is made of metal or other materials with good thermal conductivity. The heat sink **20** has a large contact surface area with air, so it has a good heat-dissipating effect. Preferably, the area of the heat sink **20** is larger than that of the die D. In some embodiments, the heat sink **20** has a structure composed of a plurality of parallel plates. In other embodiments of the present invention, the heat sink **20** may have different structures, such as a sheet metal layer or a metal mesh structure, or the lead frame used in the packaging step may be used as the heat sink **20**, that is, the lead frame can have the function of heat dissipation besides the function of connecting elements. The above-mentioned various heat sinks **20** are all within the scope of the present invention.

[0019] FIG. **5** is a schematic diagram of a semiconductor structure according to another embodiment of the present invention. Referring to FIG. **5**, this embodiment is similar to the structure shown in FIG. **3**, but the difference of this embodiment and the first embodiment mentioned above is that the microstructures **14** with different densities, different arrangements, different shapes or different depths can be formed in different dies (such as die D**1**, die D**2**, die D**3**, die D**4** and die D**5** in FIG. **5**). For example, some dies (such as die D**1** and die D**2**) have the same microstructure size, shape or arrangement, but other dies (such as die D**3**, die D**4** and die D**5**) may have different microstructure sizes, shapes or arrangement densities. Specifically, in this embodiment, the roughness of the microstructure surface of some or all dies (for example, the die D**3** shown in FIG. **5**) can be further improved by multiple oxidation or etching, so as to further improve the surface area of microstructure **14**. In the die D**4**, a part of the microstructures **14** have

deeper depth, and the other part of the microstructures **14** have shallower depth. For example, the area near the center of the die D**4** is where the main components are located, and its microstructures **14** are deeper, so it also has a good heat dissipation effect, but the present invention is not limited to this. In addition, the density of microstructures **14** distributed in the same die D**5** may also be different (for example, the density of microstructures **14** near the middle element region is higher than that in the peripheral region). Next, after the dies D**1**-D**5** with various microstructures **14** shown in FIG. **5** are cut in the cutting step P**3**, they can be packaged and mounted on the printed circuit board **16** as shown in FIG. **4** to form the thermal interface material **18** and the heat sink **20**. The related steps are the same as those described in the above paragraphs, so they will not be repeated here.

[0020] According to the above description and drawings, the present invention provides a semiconductor structure, which comprises a substrate **10**, wherein the substrate **10** has a front surface **10**A and a back surface **10**B, and the front surface **10**A of the substrate **10** includes a circuit layer **12**, and the back surface **10**B of the substrate **10** includes a plurality of microstructures **14**, and a thermal interface material **18** located on the back surface **10**B of the substrate **10** and in contact with the microstructures **14**.

[0021] In some embodiments of the present invention, a heat sink **20** is further included, which is located on the back surface **10**B of the substrate **10** and is in contact with the thermal interface material **18**.

[0022] In some embodiments of the present invention, the heat sink **20** is a lead frame.

[0023] In some embodiments of the present invention, the thermal interface material **18** contains metal particles.

[0024] In some embodiments of the present invention, the material of the metal particles is silver.

[0025] In some embodiments of the present invention, a printed circuit board **16** is further included, and the circuit layer **12** on the substrate **10** is electrically connected with the printed circuit board **16**.

[0026] In some embodiments of the present invention, the microstructure **14** includes a plurality of grooves or holes.

[0027] In some embodiments of the present invention, the thermal interface material **18** is completely filled in the grooves or holes, and the thermal interface material **18** directly contacts a bottom surface **14**A of the grooves or holes.

[0028] Another aspect of the present invention provides a manufacturing method of a semiconductor structure, which includes providing a substrate **10**, wherein the substrate **10** has a front surface **10**A and a back surface **10**B, forming a circuit layer **12** on the front surface **10**A of the substrate **10**, forming a plurality of microstructures **14** on the back surface **10**B of the substrate **10**, and forming a thermal interface material **18** on the back surface **10**B of the substrate **10** and directly contacts the microstructures **14**.

[0029] In some embodiments of the present invention, a heat sink **20** is formed on the back surface **10**B of the substrate **10**, and is in contact with the thermal interface material **18**.

[0030] In some embodiments of the present invention, the thermal interface material **18** contains metal particles.

[0031] In some embodiments of the present invention, the material of the metal particles is silver.

[0032] Some embodiments of the present invention further include providing a printed circuit board **16**, wherein the circuit layer **12** on the substrate **10** is electrically connected with the printed circuit board **16**.

[0033] In some embodiments of the present invention, the microstructure **14** includes a plurality of grooves or holes.

[0034] In some embodiments of the present invention, the thermal interface material **18** is completely filled in the grooves or holes, and the thermal interface material **18** directly contacts a bottom surface **14**A of the grooves or holes.

[0035] In some embodiments of the present invention, it further includes thinning the substrate **10** (the thinning step P**1** in FIG. **1**) before forming the microstructure **14** on the back surface **10**B of the substrate **10**.
[0036] In some embodiments of the present invention, after the circuit layer **12** and a plurality of microstructures **14** are formed, a cutting step P**3** is further performed to cut the electrically connected substrate **10** and the circuit layer **12** into a plurality of dies.
[0037] In some embodiments of the present invention, the method of forming the microstructure **14** includes a photolithography and etching step P**2**.
[0038] The present invention is characterized in that a plurality of microstructures (such as holes or grooves) are formed on the back surface of the substrate of the wafer, and then the thermal interface material is filled into the microstructures, and the heat sink is connected to the thermal interface material. Because the microstructure increases the surface area of the back surface of the substrate, the heat dissipation efficiency of the semiconductor chip can be improved after the thermal interface material is filled in the microstructure. The invention has the advantages of compatibility with existing processes and improvement of the efficiency of semiconductor chips.
[0039] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

Claims

1. A method of manufacturing a semiconductor structure, comprising: providing a substrate, wherein the substrate has a front surface and a back surface; forming a circuit layer on the front surface of the substrate; forming a plurality of microstructures on the back surface of the substrate; and forming a thermal interface material on the back surface of the substrate and in contact with the microstructures.
2. The manufacturing method of a semiconductor structure according to claim 1, further comprising forming a heat sink on the back surface of the substrate and in contact with the thermal interface material.
3. The manufacturing method of a semiconductor structure according to claim 1, wherein the thermal interface material contains metal particles.
4. The manufacturing method of a semiconductor structure according to claim 3, wherein the material of the metal particles is silver.
5. The manufacturing method of a semiconductor structure according to claim 1, further comprising providing a printed circuit board, wherein the circuit layer on the substrate is electrically connected with the printed circuit board.
6. The manufacturing method of a semiconductor structure according to claim 1, wherein the microstructure comprises a plurality of grooves or holes.
7. The manufacturing method of a semiconductor structure according to claim 6, wherein the thermal interface material is filled in the grooves or the holes, and the thermal interface material directly contacts a bottom surface of the grooves or the holes.
8. The manufacturing method of semiconductor structure according to claim 1, further comprising: further comprising thinning the substrate before the microstructure is formed on the back surface of the substrate.
9. The manufacturing method of semiconductor structure according to claim 1, wherein after the circuit layer and the microstructures are formed, a cutting step is further performed to cut the substrate and the circuit layer on the substrate into a plurality of dies.

10. The method for manufacturing a semiconductor structure according to claim 1, wherein the method for forming the microstructure comprises a photolithography and etching step.