US 20250261377A1

(19) United States
(12) Patent Application Publication
Lin et al.

(10) Pub. No.: US 2025/0261377 A1
(43) Pub. Date: Aug. 14, 2025

(54) **SEMICONDUCTOR DIES INCLUDING LOW AND HIGH WORKFUNCTION SEMICONDUCTOR DEVICES**

(71) Applicant: **Taiwan Semiconductor Manufacturing Company, Ltd.**, Hsinchu (TW)

(72) Inventors: **Meng-Han Lin**, Hsinchu City (TW); **Chia-En Huang**, Xinfeng Township (TW)

(73) Assignee: **Taiwan Semiconductor Manufacturing Company, Ltd.**, Hsinchu (TW)

(21) Appl. No.: **19/096,989**

(22) Filed: **Apr. 1, 2025**

Related U.S. Application Data

(60) Continuation of application No. 18/678,963, filed on May 30, 2024, now Pat. No. 12,289,891, which is a division of application No. 17/585,932, filed on Jan. 27, 2022, now Pat. No. 12,069,862.

(60) Provisional application No. 63/225,228, filed on Jul. 23, 2021.

Publication Classification

(51) **Int. Cl.**

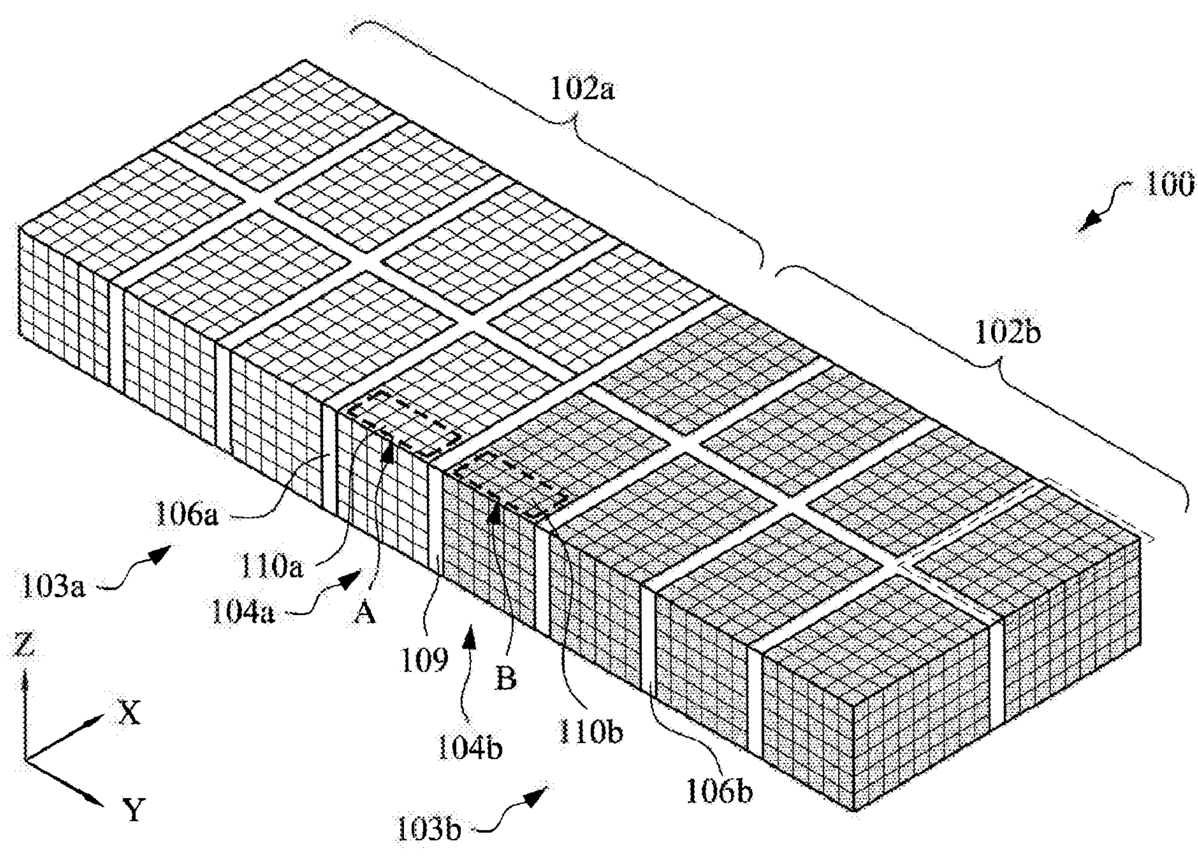
H10B 51/20	(2023.01)
H10B 51/10	(2023.01)
H10B 51/30	(2023.01)
H10D 30/01	(2025.01)
H10D 30/69	(2025.01)
H10D 64/01	(2025.01)
H10D 64/27	(2025.01)

(52) **U.S. Cl.**

CPC ***H10B 51/20*** (2023.02); ***H10B 51/10*** (2023.02); ***H10B 51/30*** (2023.02); ***H10D 30/0415*** (2025.01); ***H10D 30/701*** (2025.01); ***H10D 64/033*** (2025.01); ***H10D 64/514*** (2025.01); ***H10D 64/517*** (2025.01)

(57) **ABSTRACT**

A method of making a semiconductor die includes forming, over a substrate, a stack including insulating layers and sacrificial layers alternatively on top of each other; replacing a portion of first sacrificial layers located in a first portion of the stack to form first gate layers; forming first channel layers extending in a first direction in the first portion; forming first memory layers extending in the first direction in the first portion; replacing a portion of second sacrificial layers located in a second portion of the stack to form second gate layers; forming second channel layers extending in the first direction in the second portion; and forming second memory layers extending in the first direction in the second portion.



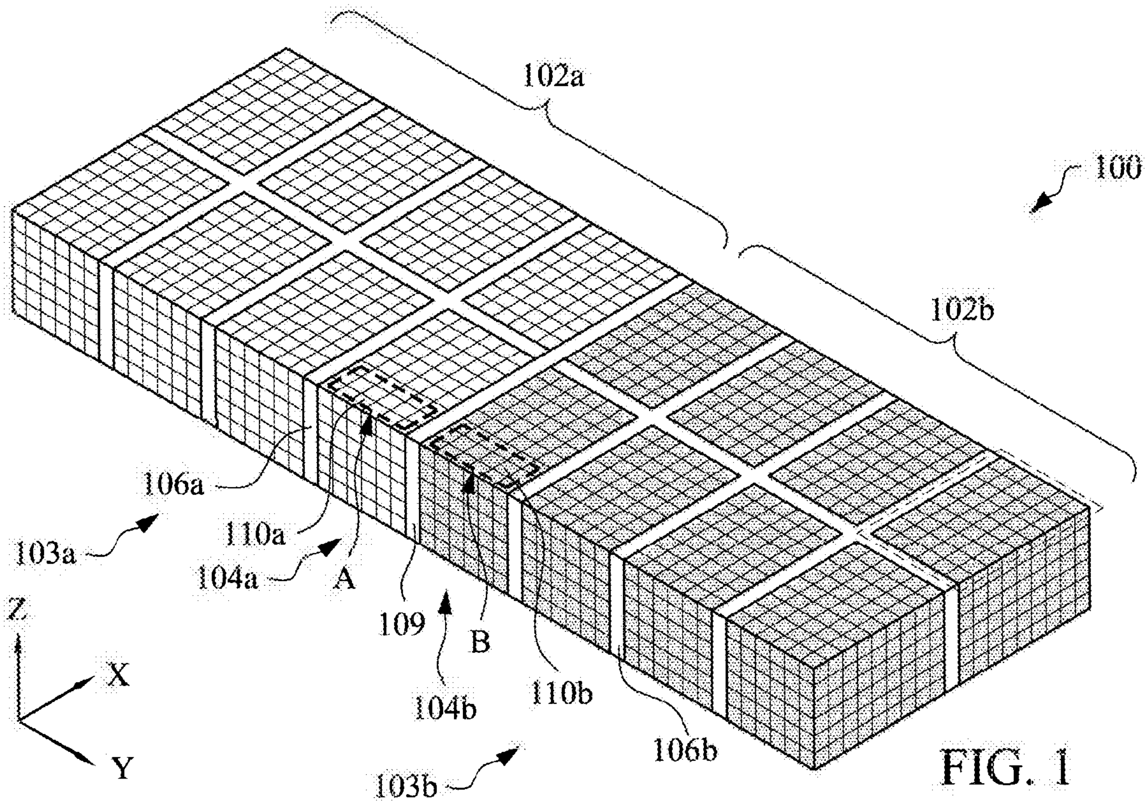

102a
100
102b
106a
103a
110a
104a
A
109
B
104b
110b
106b
103b
Z
X
Y

FIG. 1

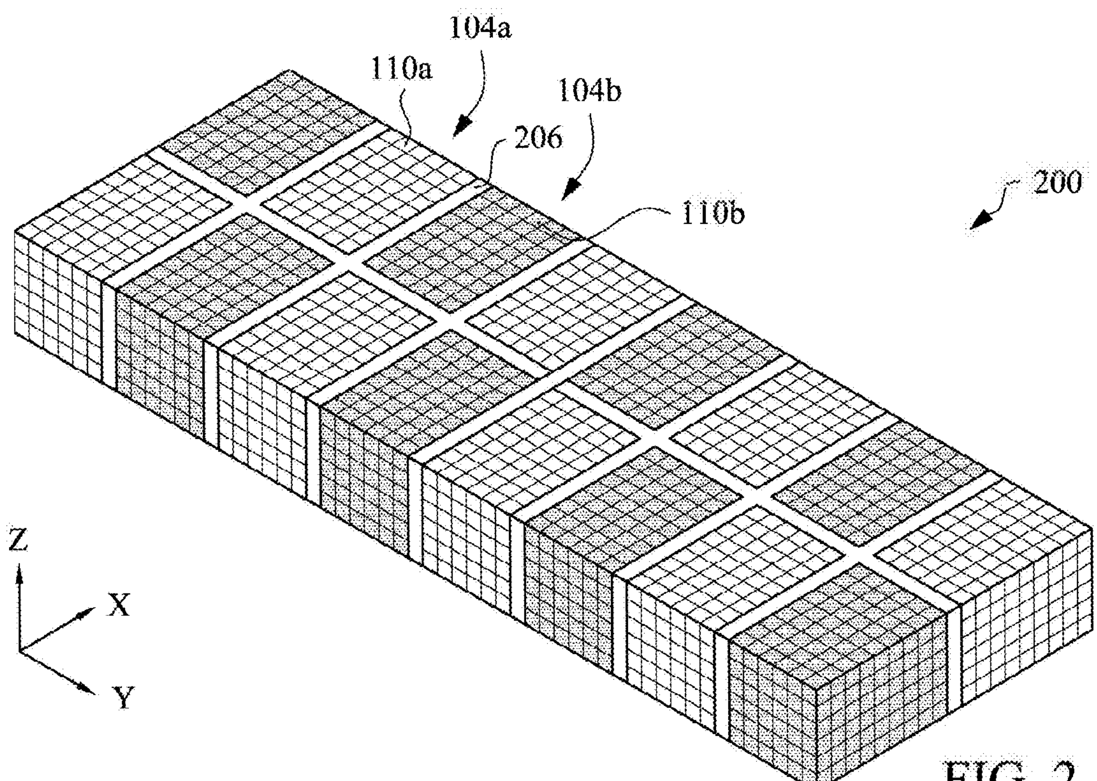

104a
110a
104b
206
200
110b
Z
X
Y

FIG. 2

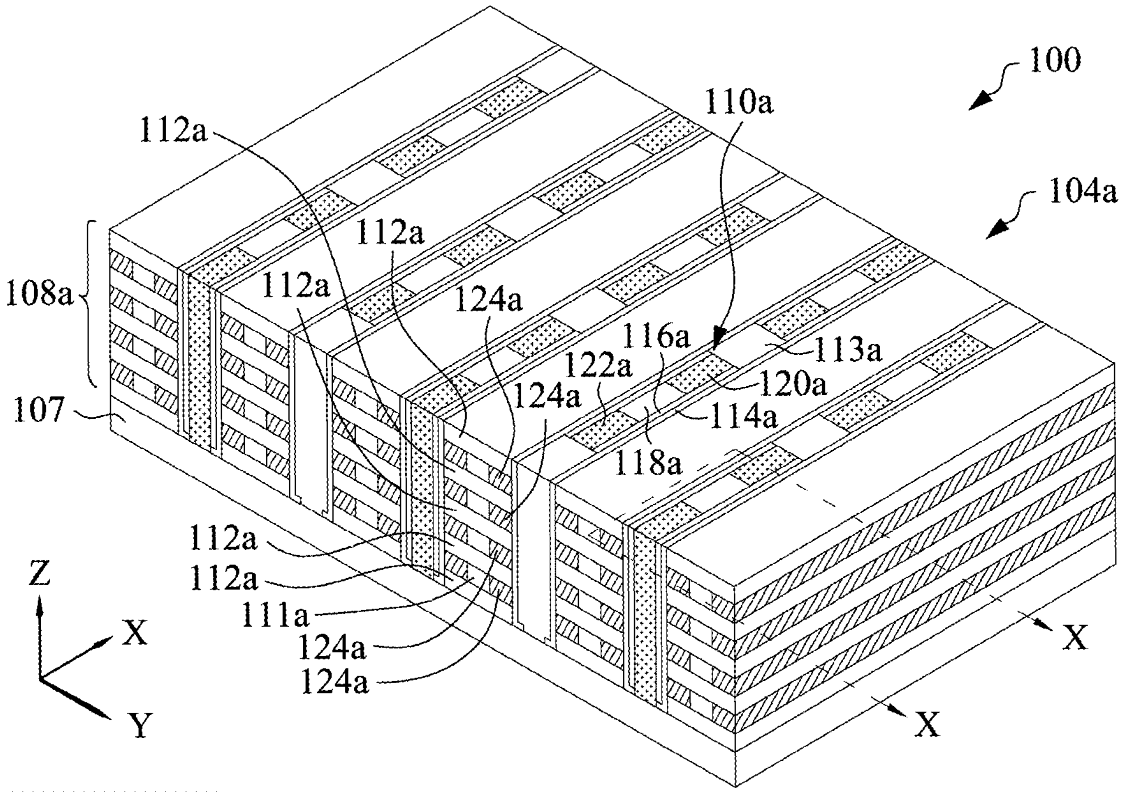

100
110a
112a
104a
112a
108a
112a
124a
116a
113a
122a
120a
124a
114a
107
118a
112a
112a
Z
111a
X
124a
X
124a
Y
X

FIG. 3A

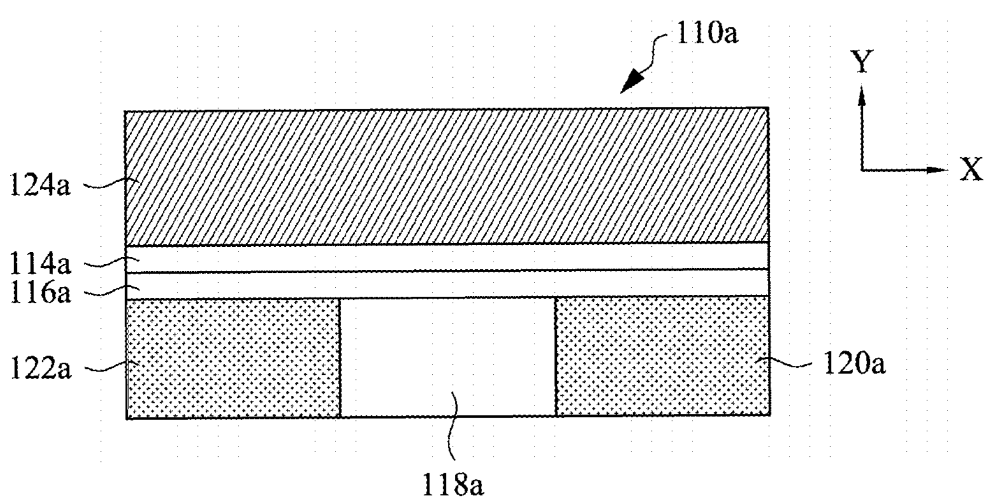

110a
Y
124a
X
114a
116a
122a
120a
118a

FIG. 3B

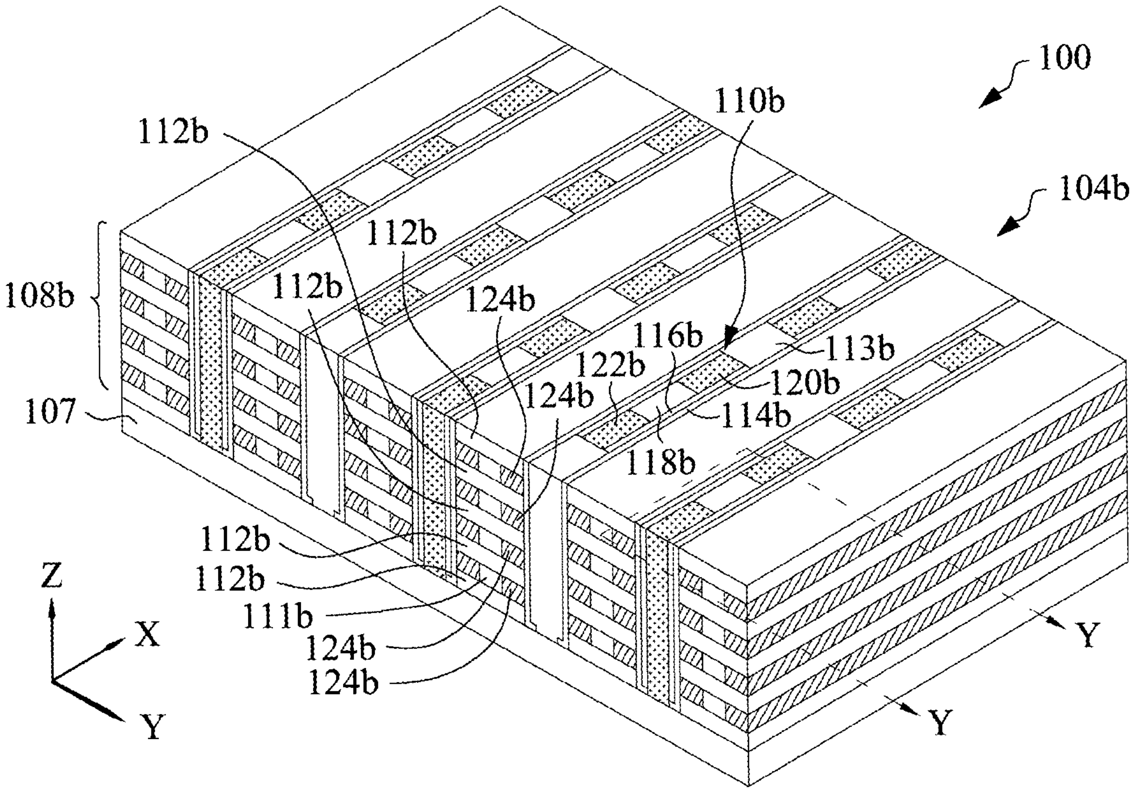

100
110b
112b
104b
112b
108b
112b
124b
116b
113b
122b
120b
124b
114b
107
118b
112b
112b
111b
124b
124b
Z
X
Y
Y
Y

FIG. 4A

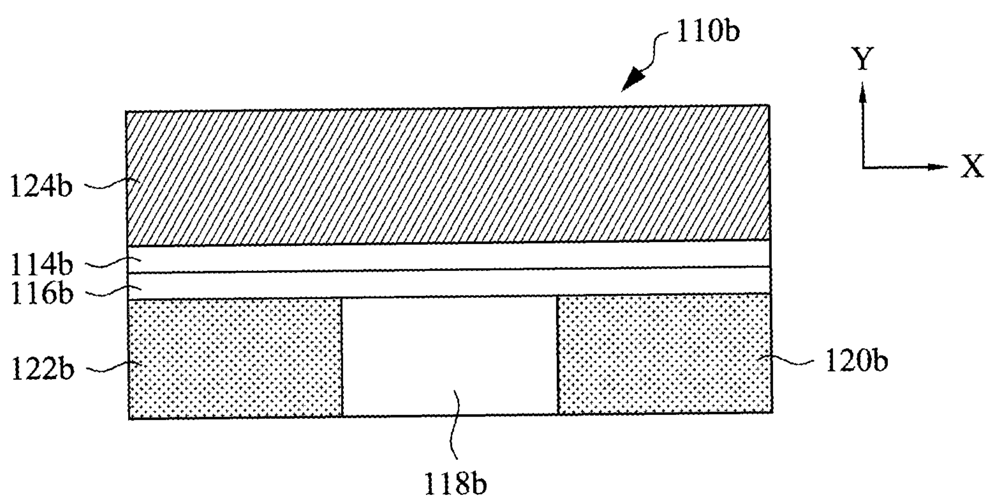

110b
Y
X
124b
114b
116b
122b
120b
118b

FIG. 4B

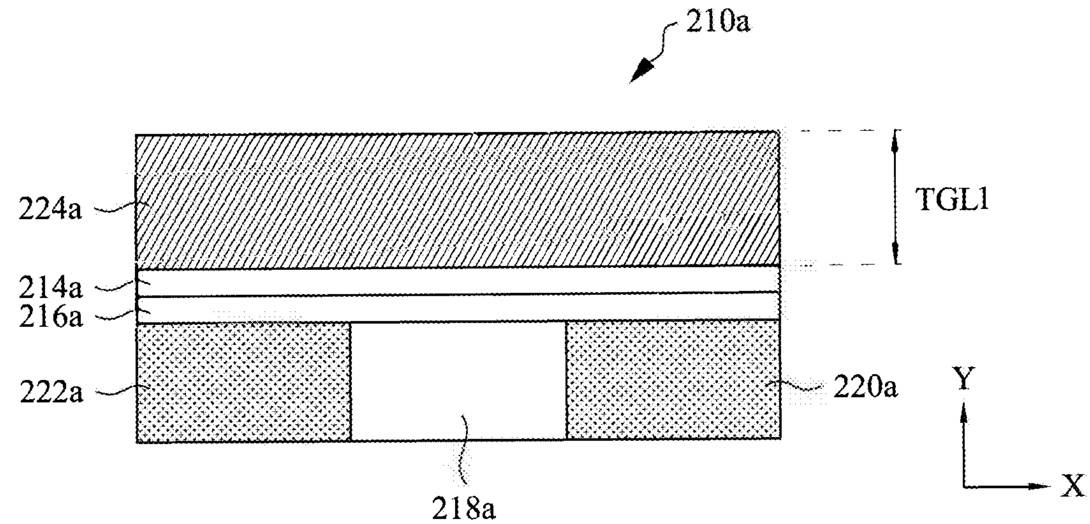

210a
224a
214a
216a
222a
220a
218a
TGL1
Y
X

FIG. 5A

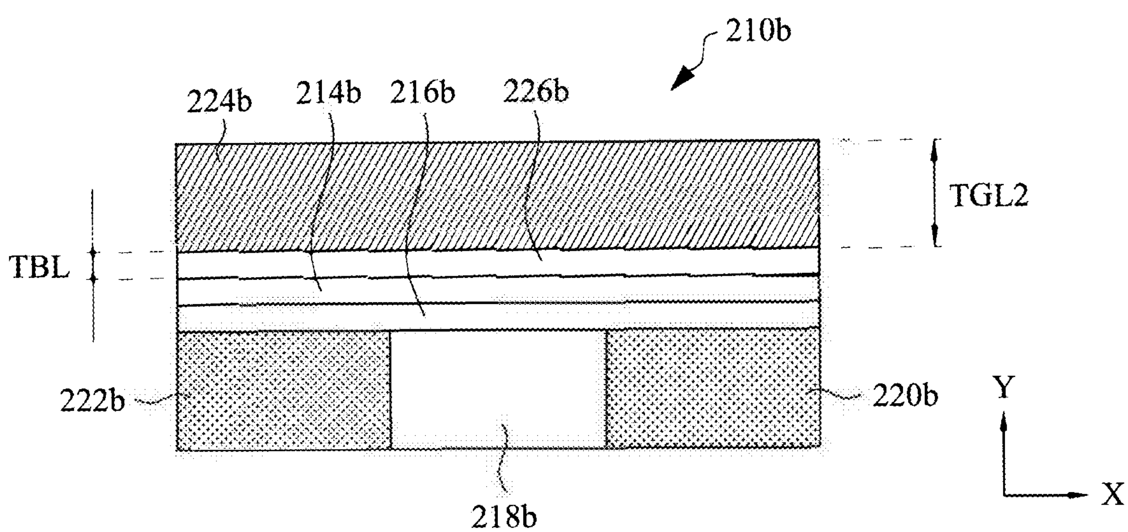

210b
224b
214b
216b
226b
TBL
TGL2
222b
220b
218b
Y
X

FIG. 5B

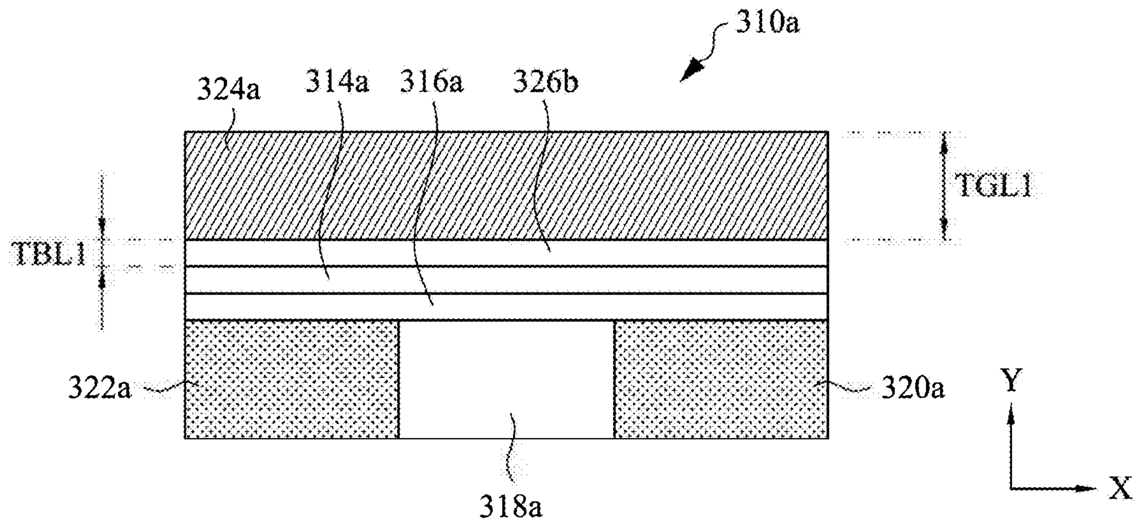

310a
324a
314a
316a
326b
TGL1
TBL1
322a
320a
318a
Y
X

FIG. 6A

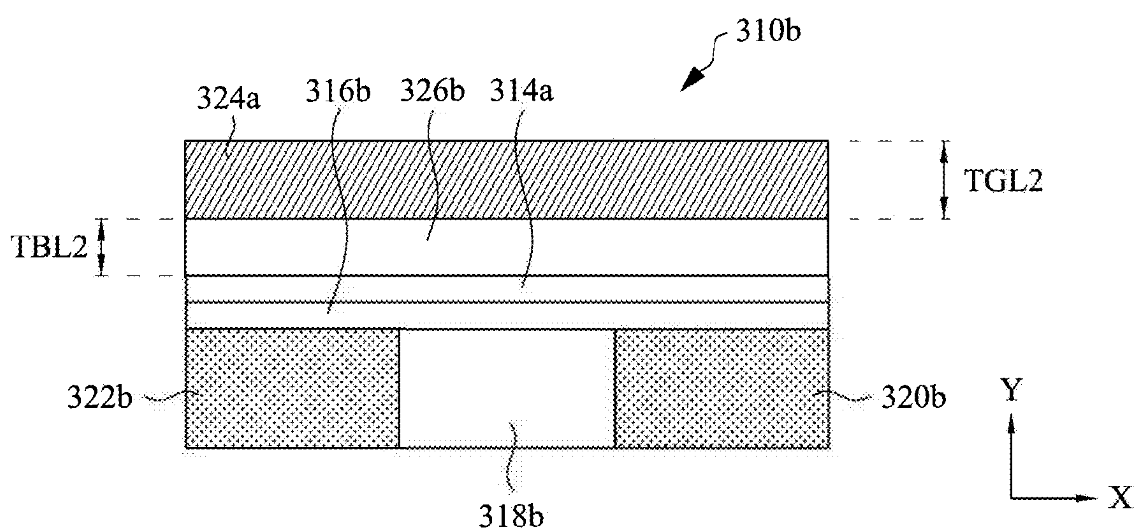

310b
324a
316b
326b
314a
TGL2
TBL2
322b
320b
318b
Y
X

FIG. 6B

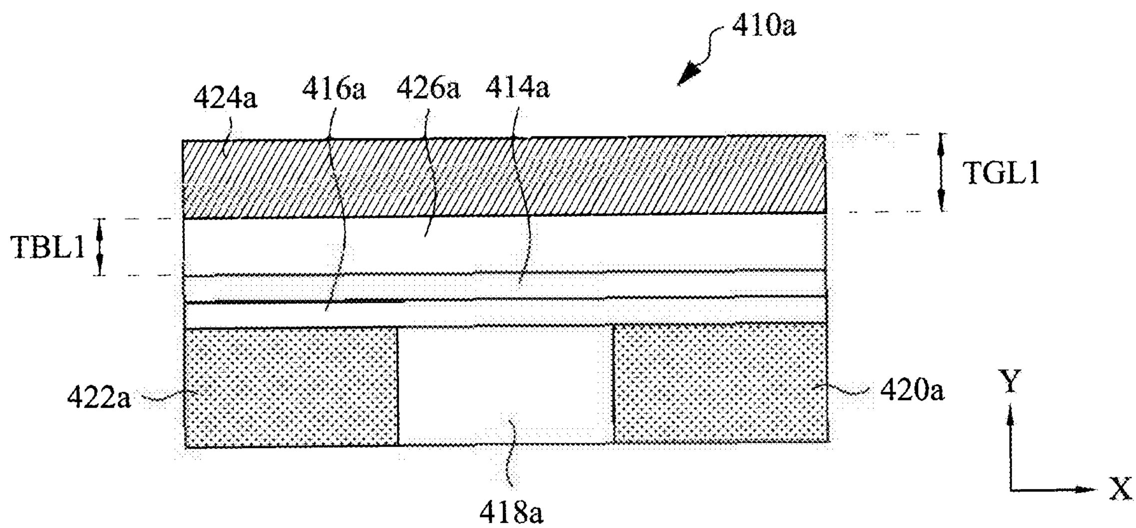

410a
424a
416a
426a
414a
TGL1
TBL1
422a
420a
418a
Y
X

FIG. 7A

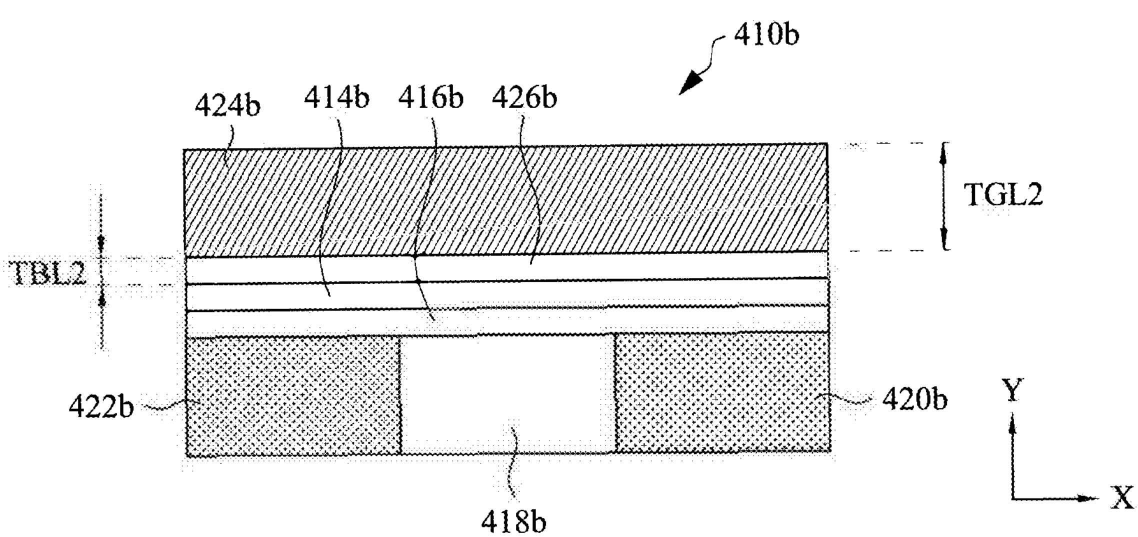

410b
424b
414b
416b
426b
TGL2
TBL2
422b
420b
418b
Y
X

FIG. 7B

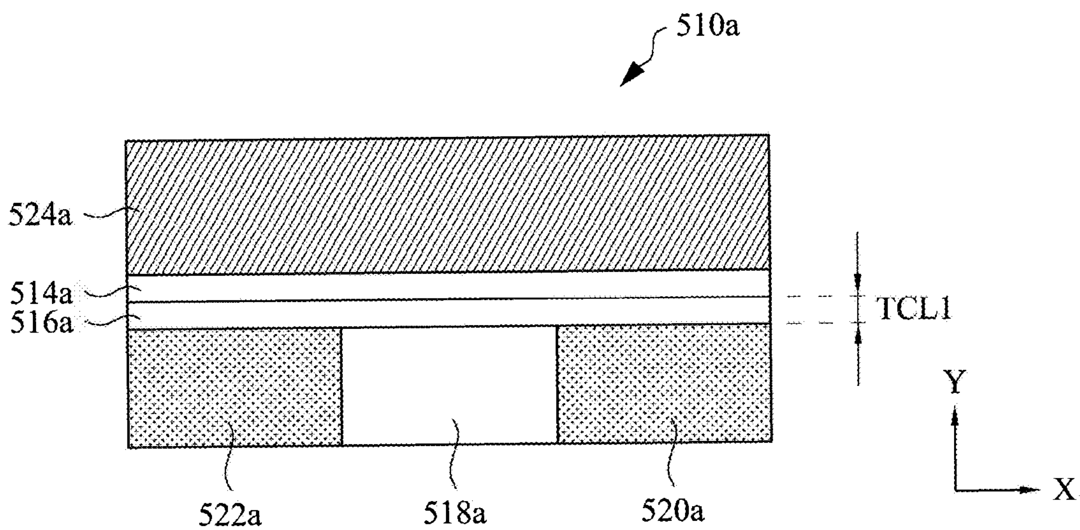

510a
524a
514a
516a
TCL1
Y
X
522a
518a
520a

FIG. 8A

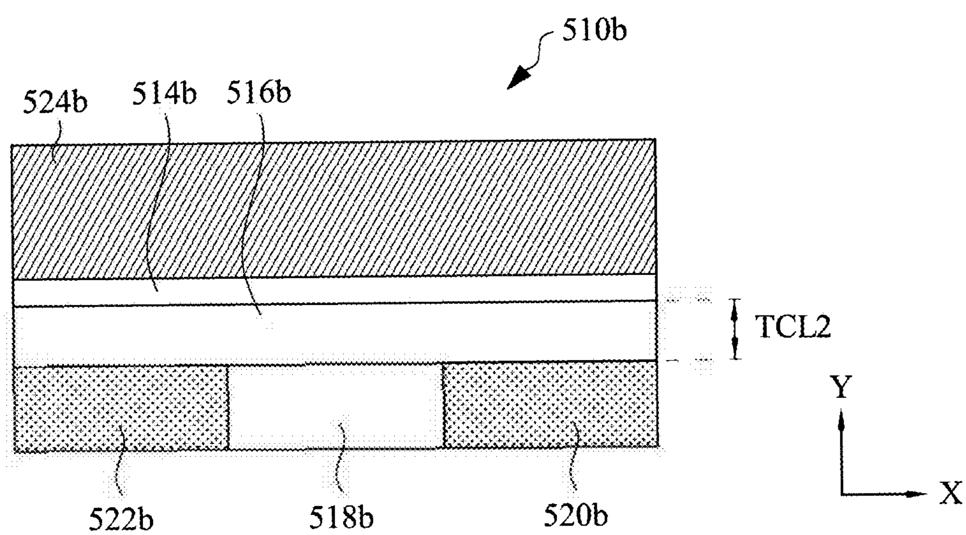

510b
524b
514b
516b
TCL2
Y
X
522b
518b
520b

FIG. 8B

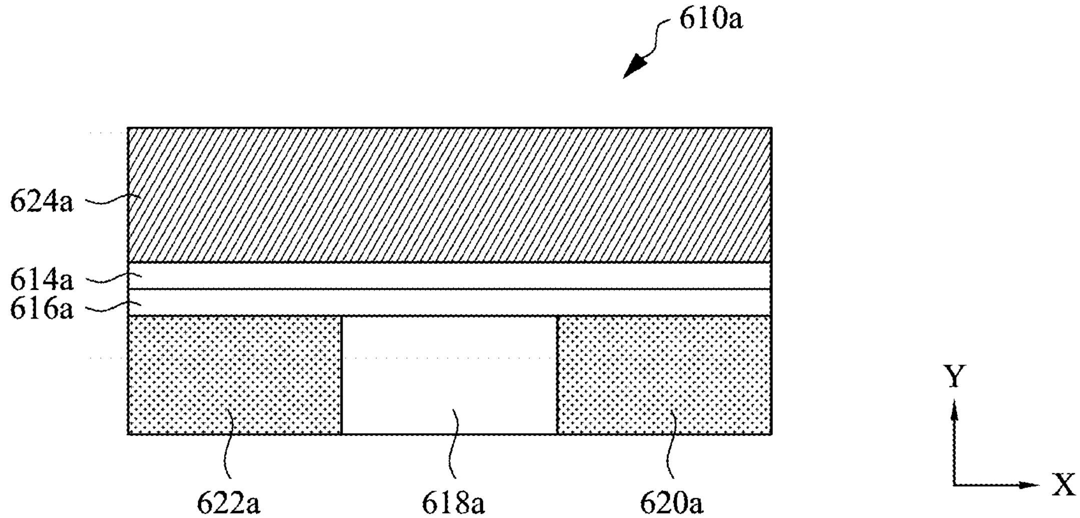

610a
624a
614a
616a
622a
618a
620a
Y
X

FIG. 9A

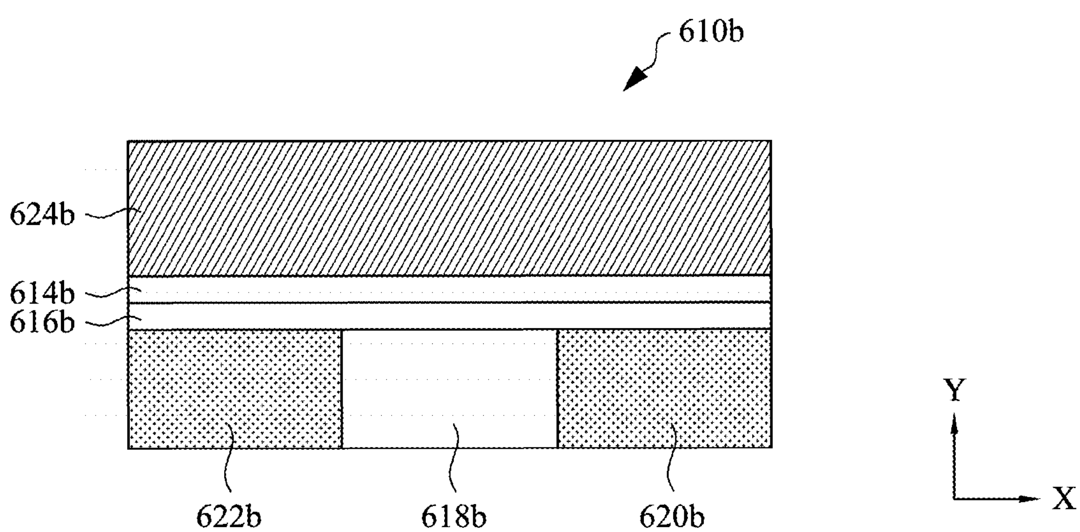

610b
624b
614b
616b
622b
618b
620b
Y
X

FIG. 9B

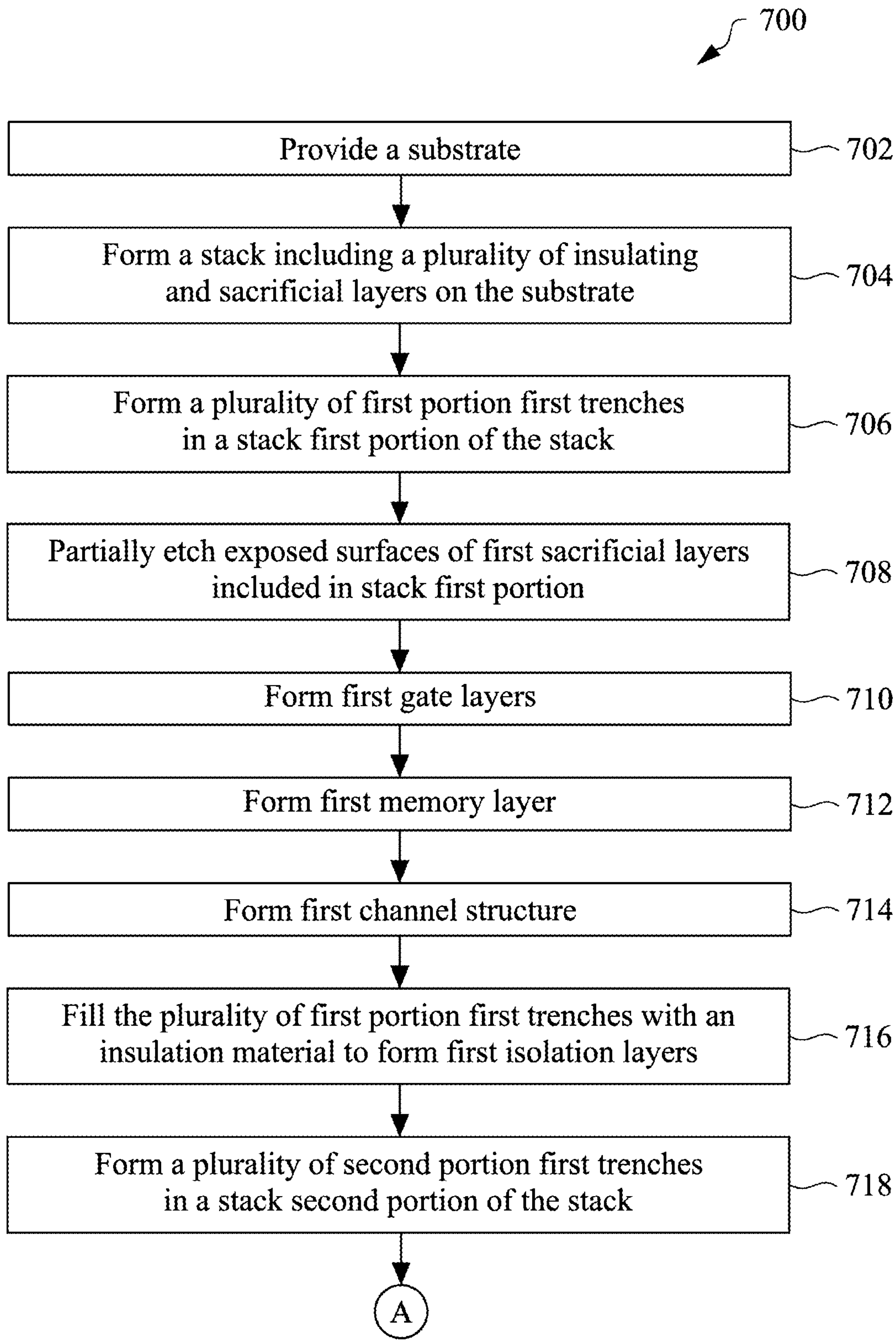

700
Provide a substrate
702
Form a stack including a plurality of insulating and sacrificial layers on the substrate
704
Form a plurality of first portion first trenches in a stack first portion of the stack
706
Partially etch exposed surfaces of first sacrificial layers included in stack first portion
708
Form first gate layers
710
Form first memory layer
712
Form first channel structure
714
Fill the plurality of first portion first trenches with an insulation material to form first isolation layers
716
Form a plurality of second portion first trenches in a stack second portion of the stack
718
A

FIG. 10A

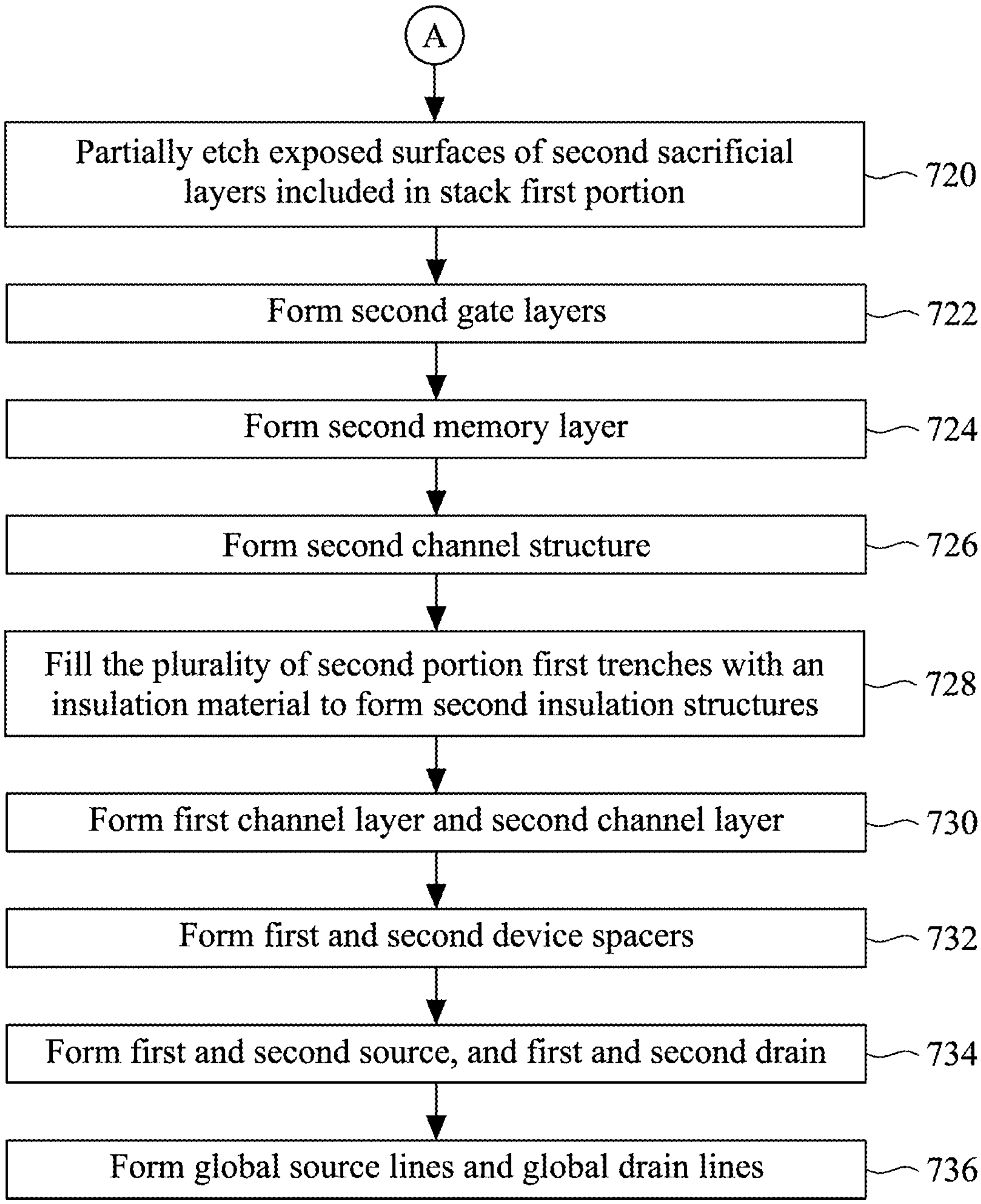

A
Partially etch exposed surfaces of second sacrificial layers included in stack first portion
720
Form second gate layers
722
Form second memory layer
724
Form second channel structure
726
Fill the plurality of second portion first trenches with an insulation material to form second insulation structures
728
Form first channel layer and second channel layer
730
Form first and second device spacers
732
Form first and second source, and first and second drain
734
Form global source lines and global drain lines
736

FIG. 10B

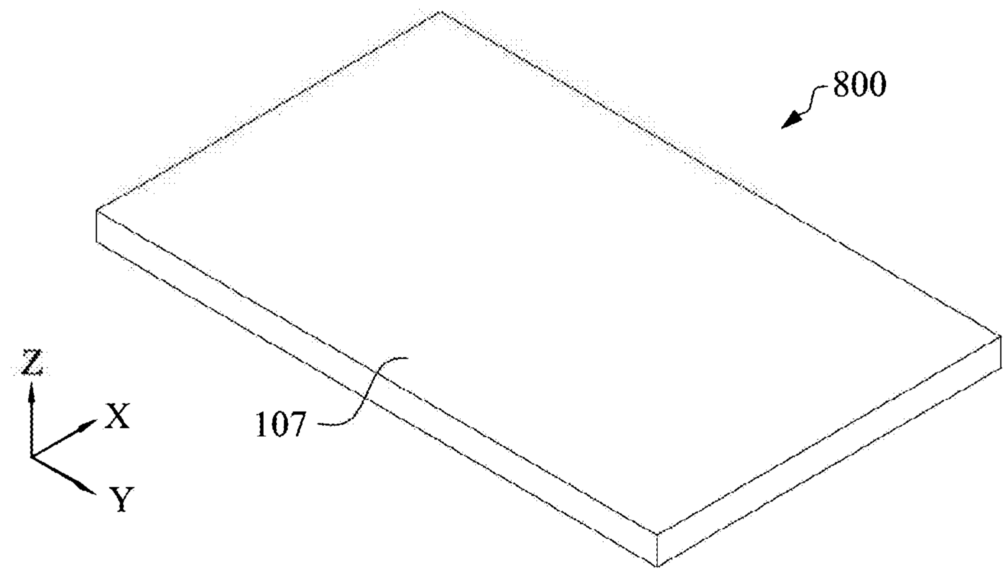


FIG. 11

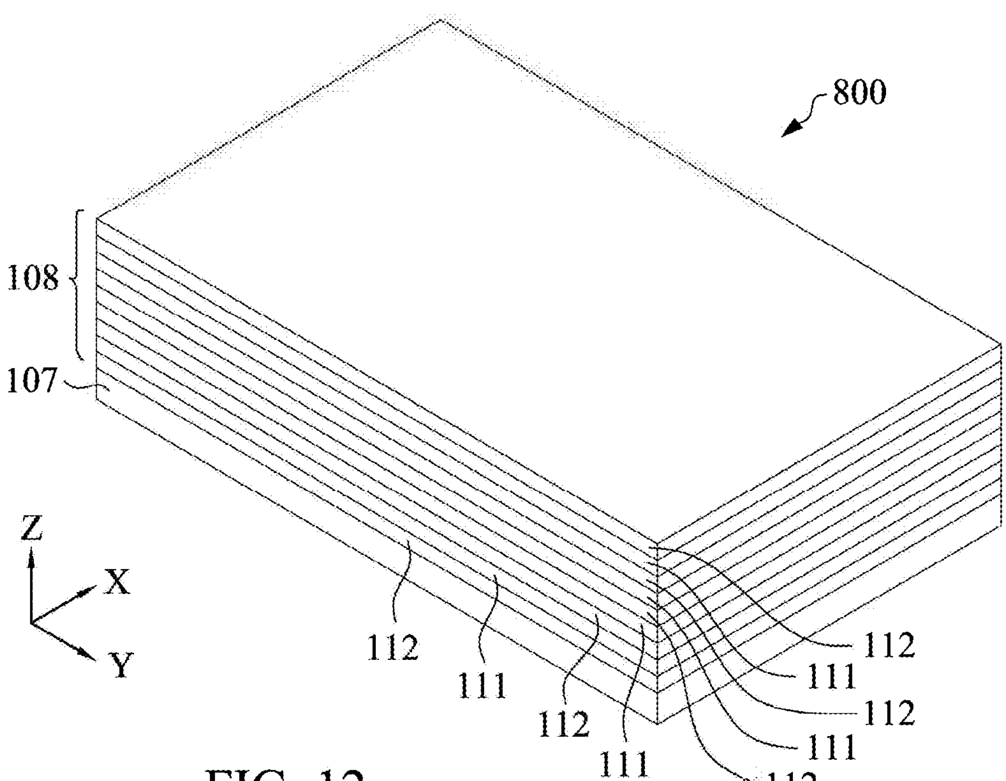


FIG. 12

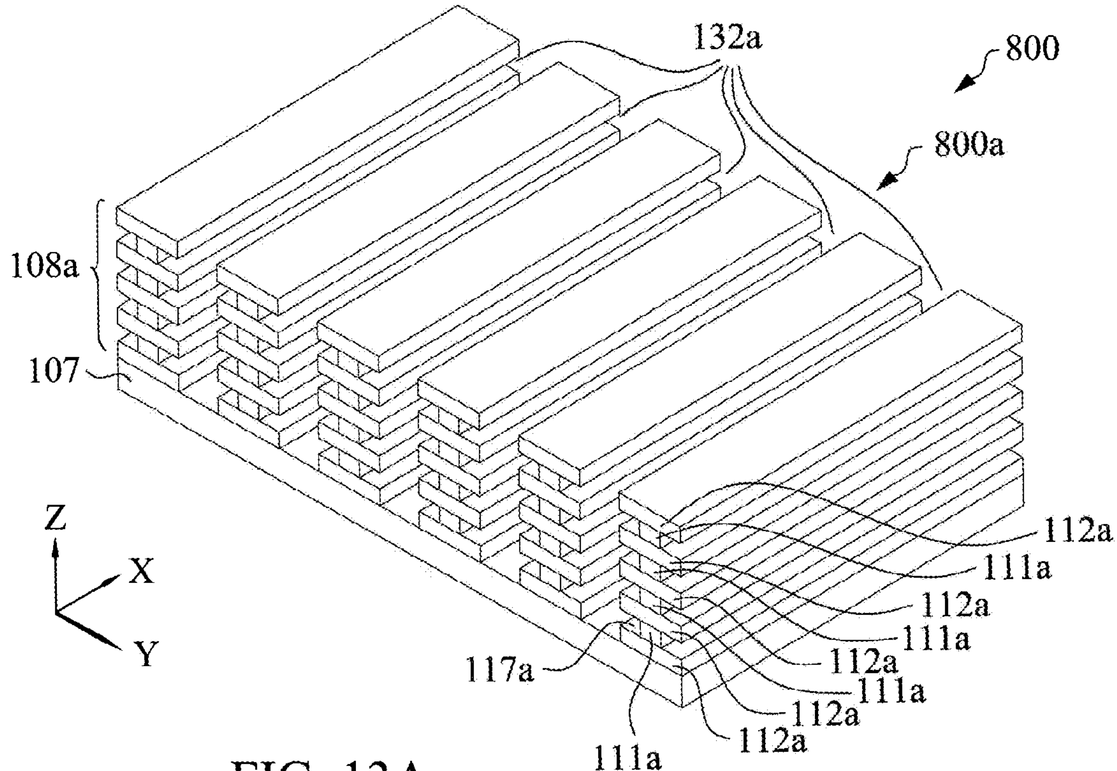


FIG. 13A

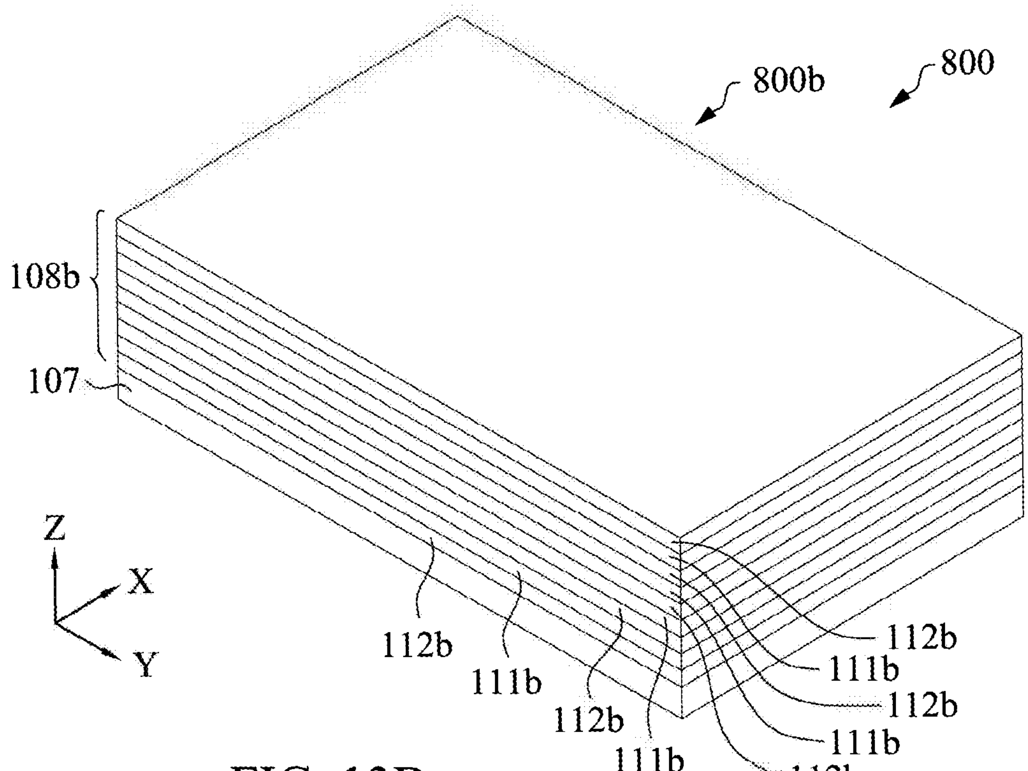


FIG. 13B

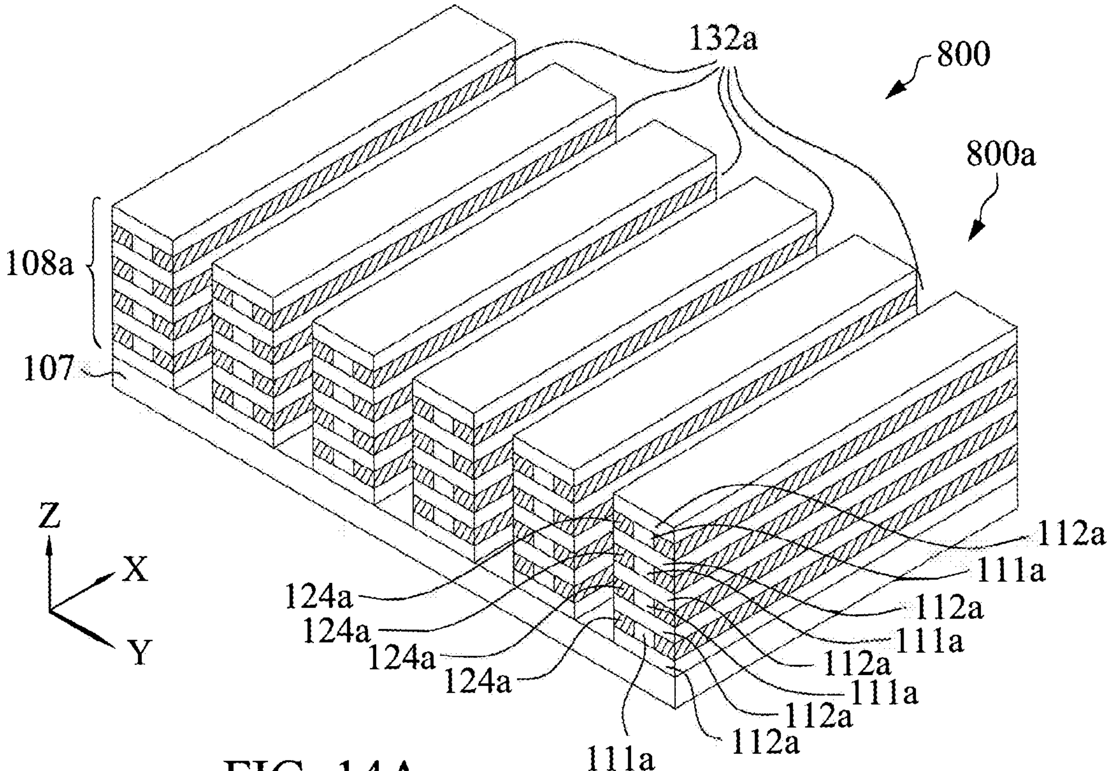


FIG. 14A

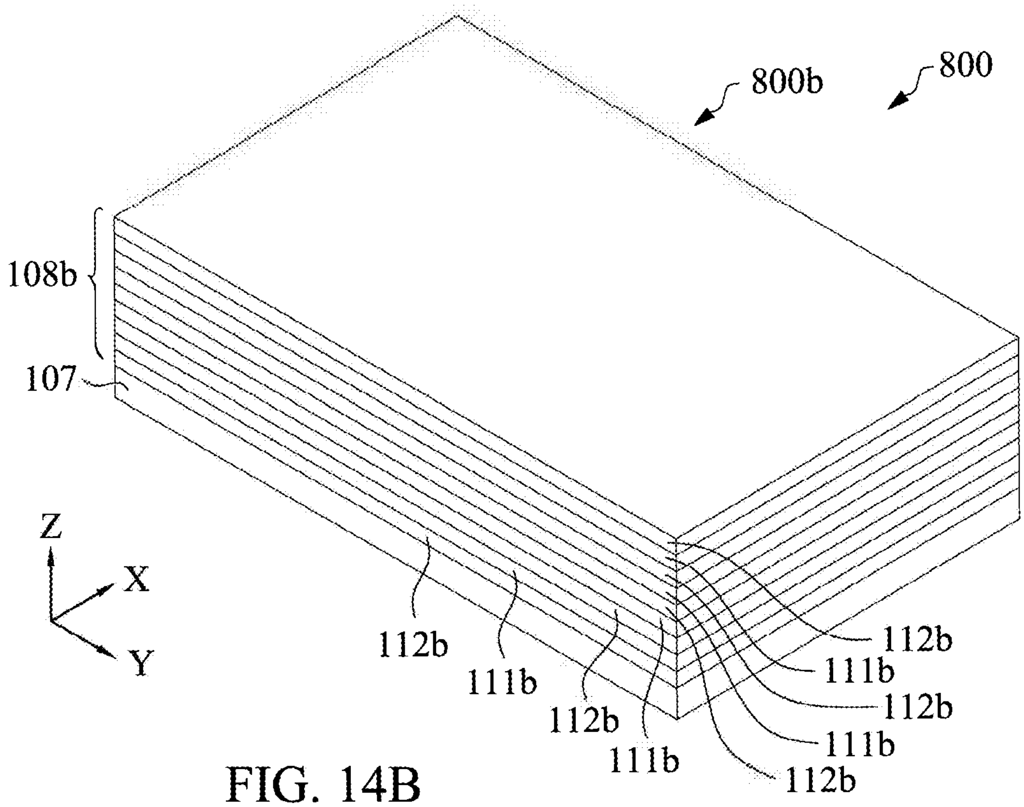


FIG. 14B

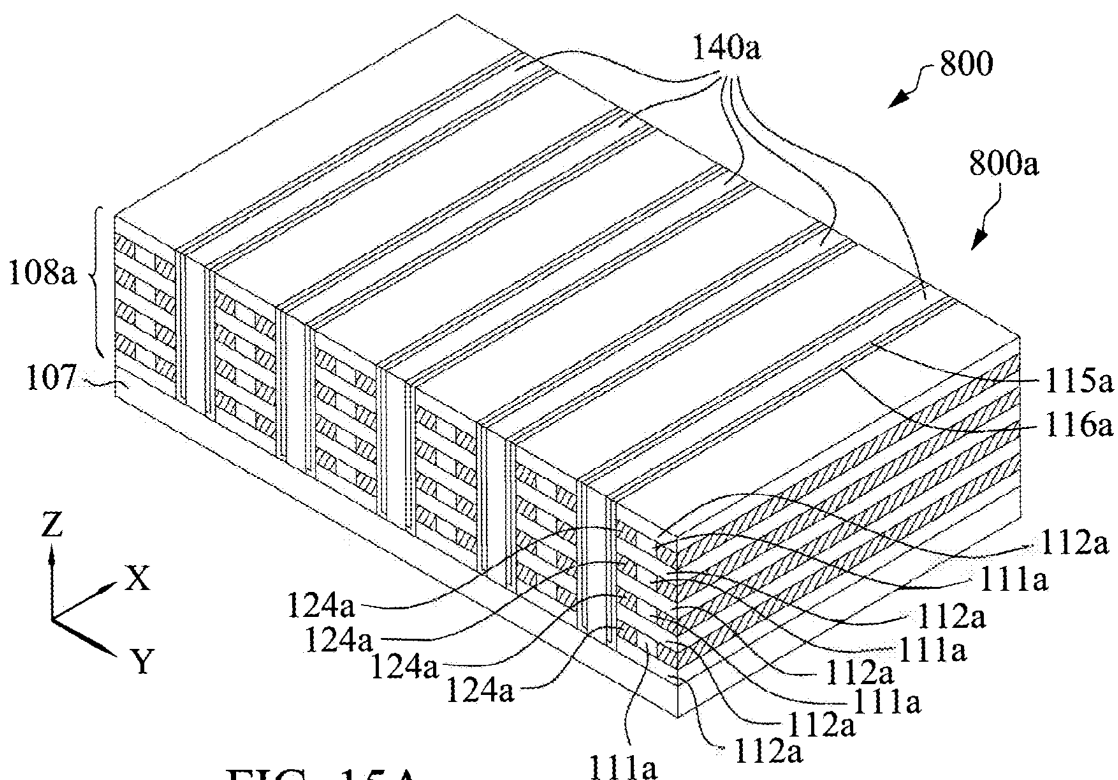


FIG. 15A

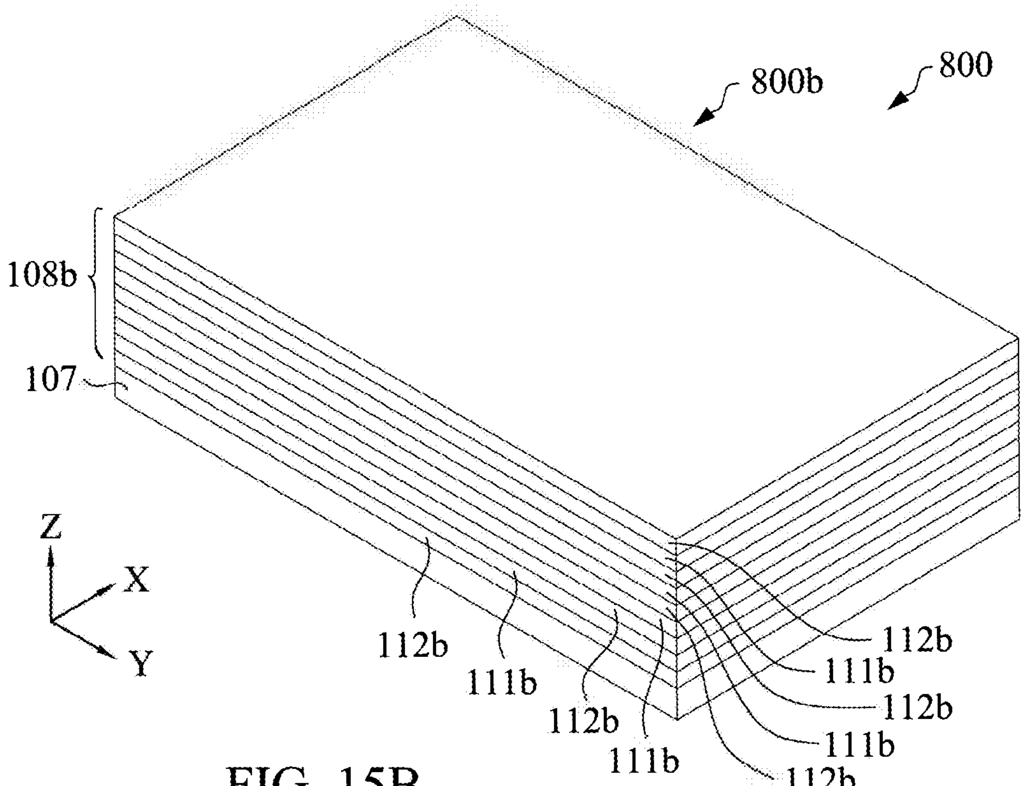


FIG. 15B

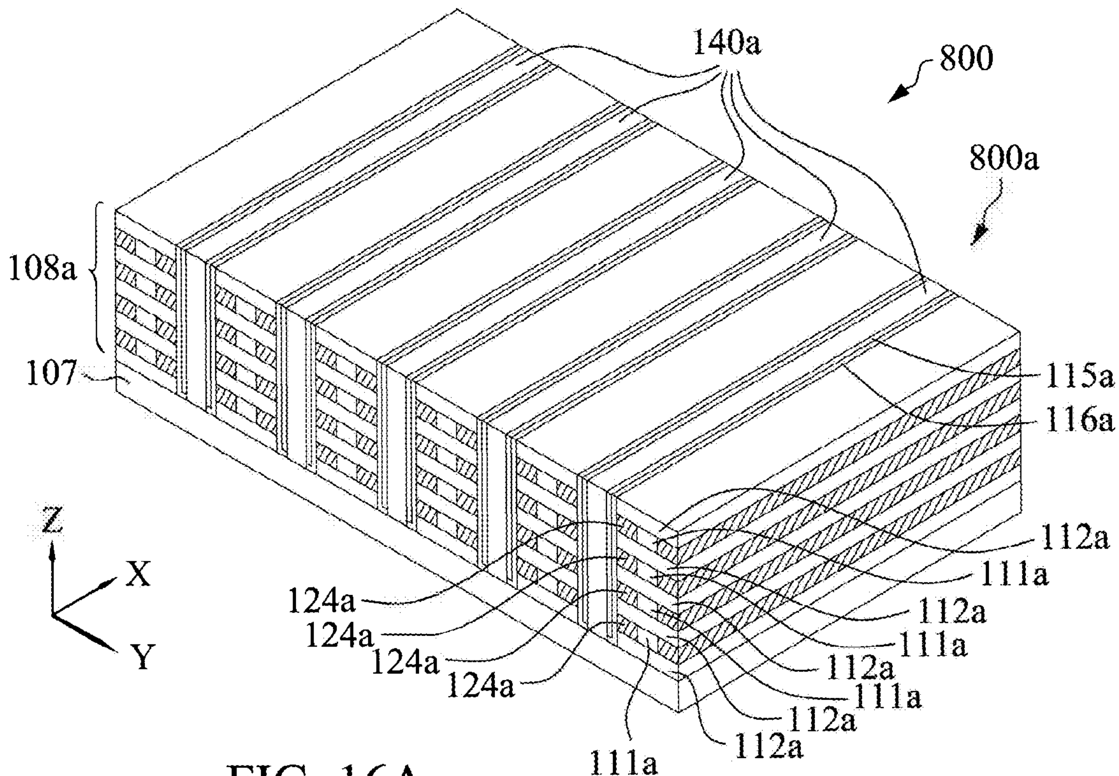


FIG. 16A

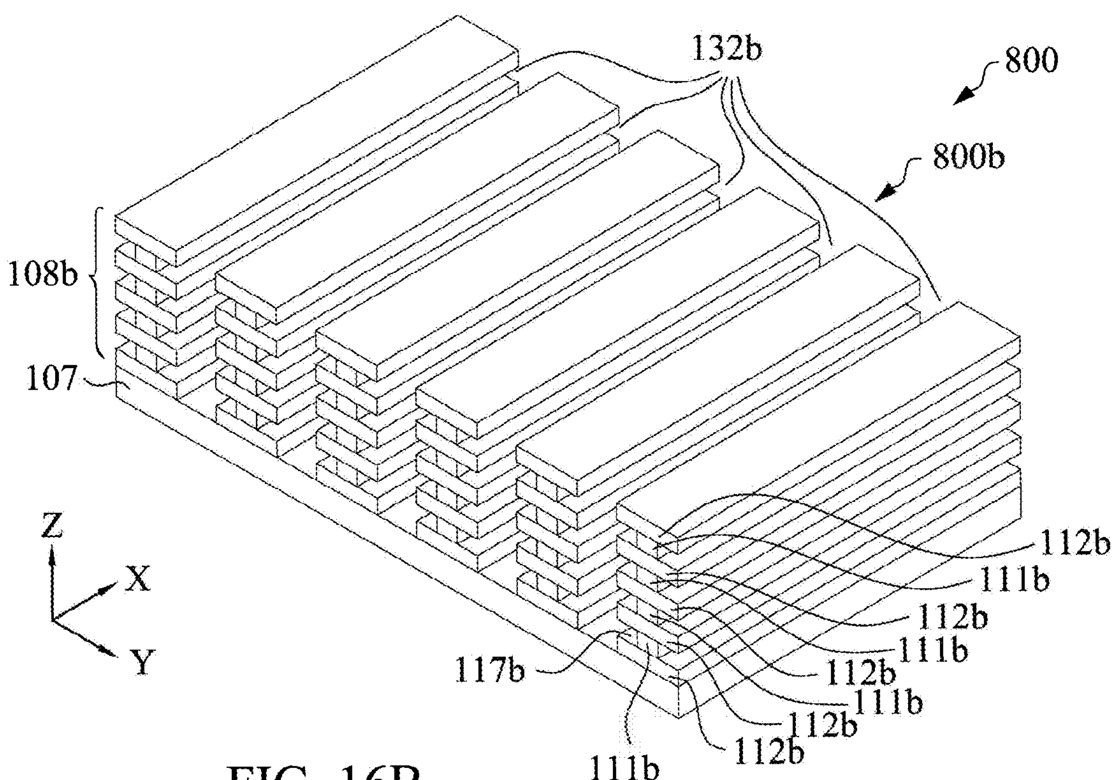


FIG. 16B

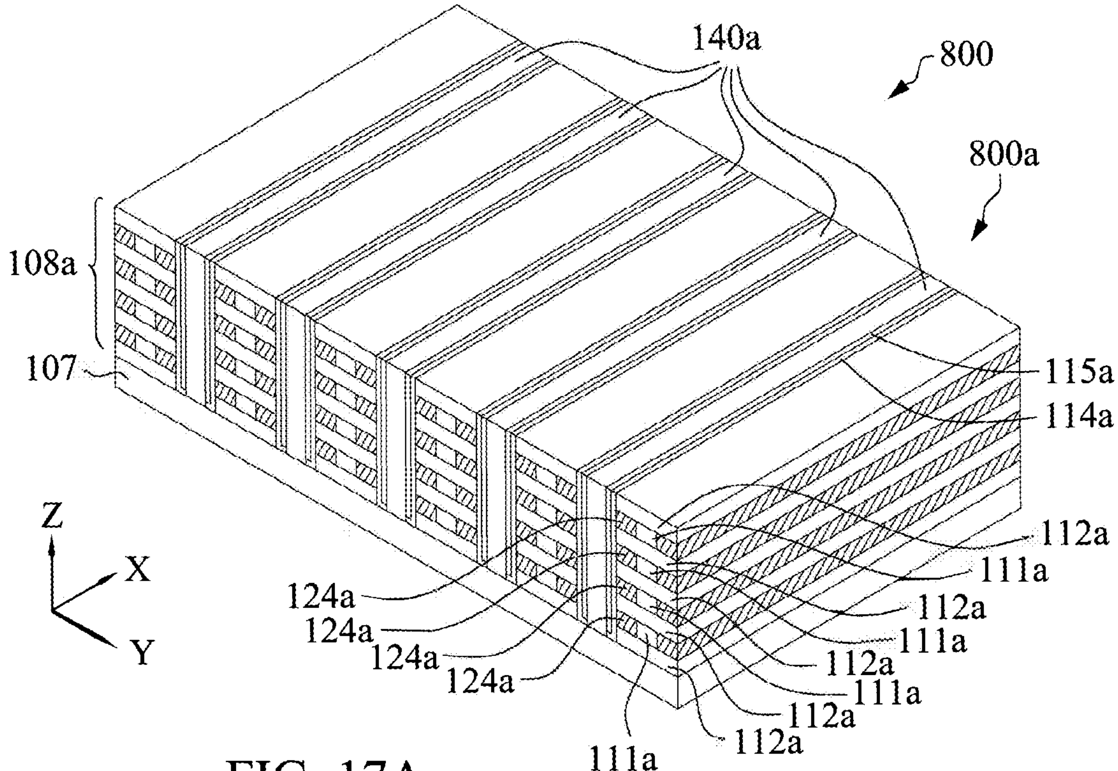


FIG. 17A

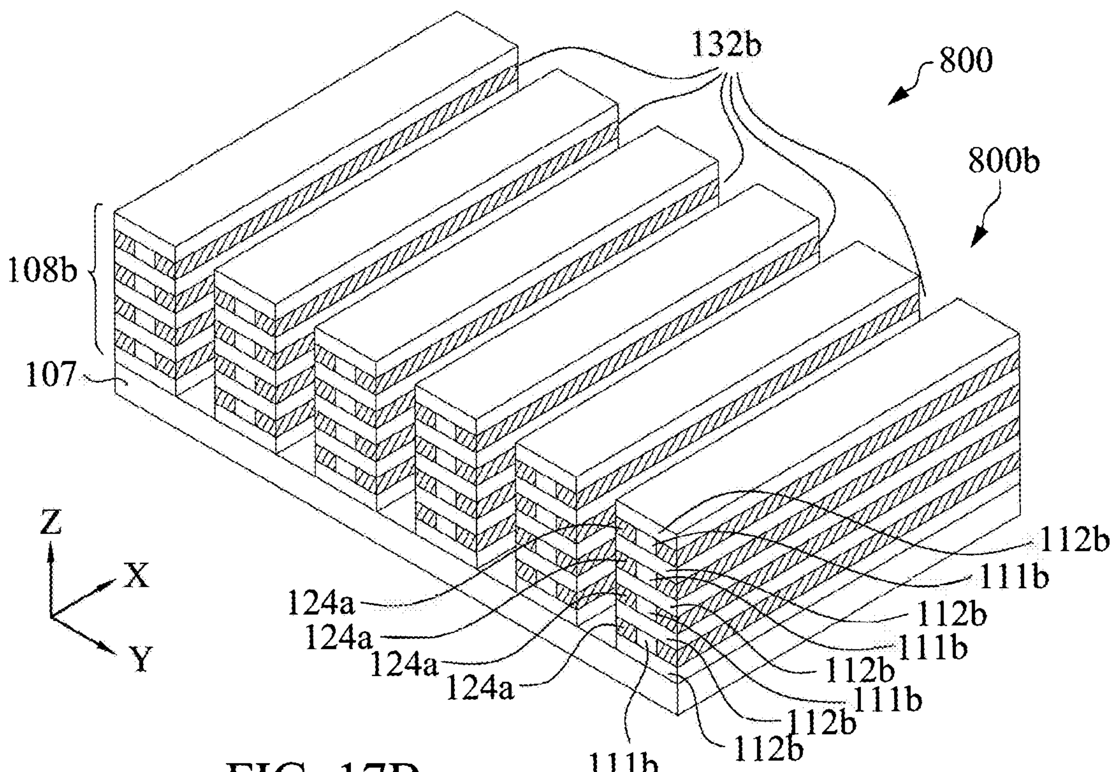


FIG. 17B

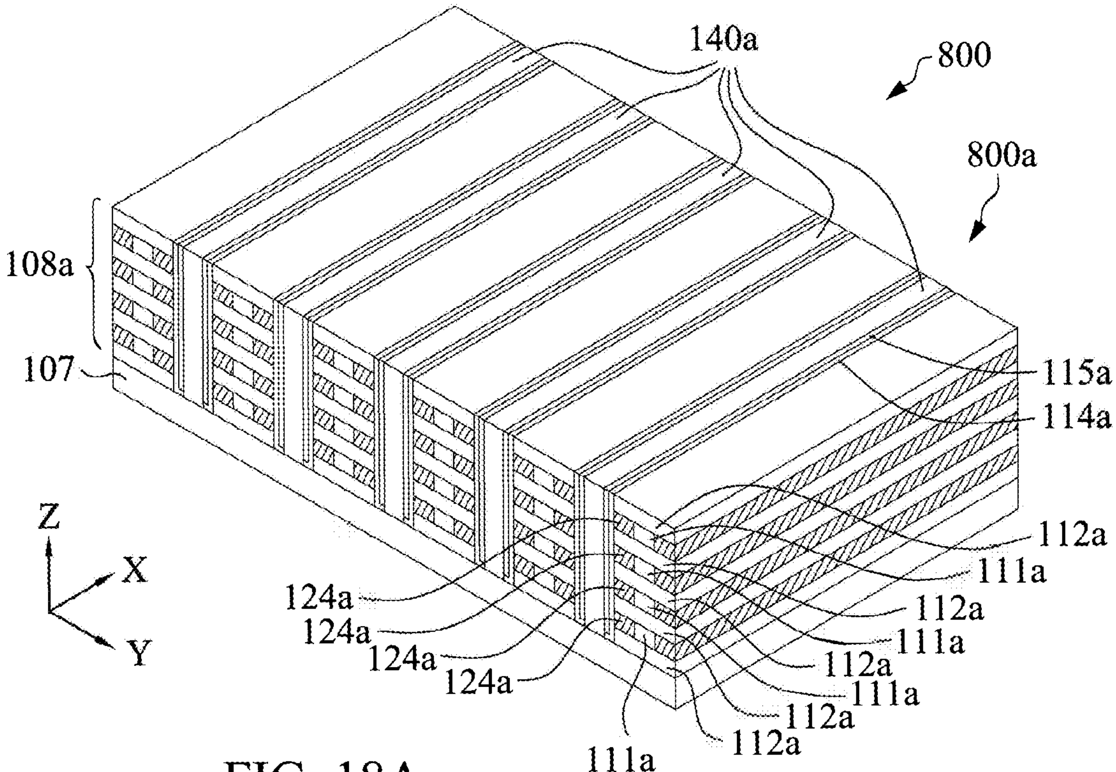


FIG. 18A

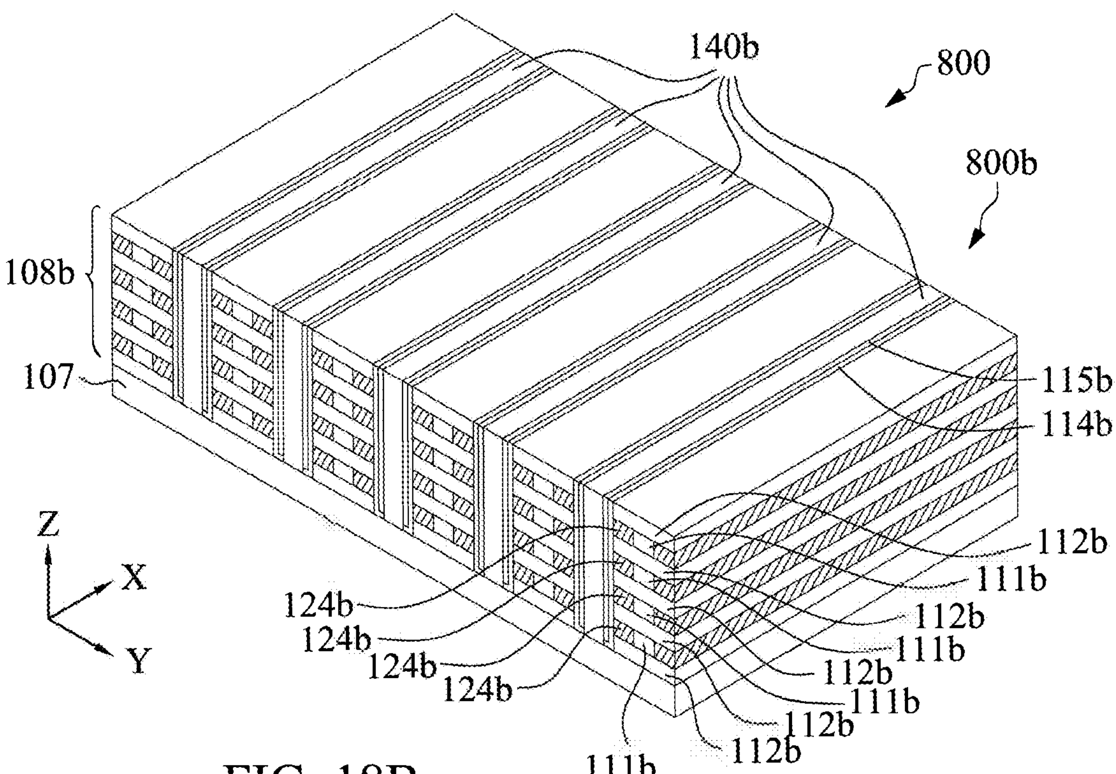


FIG. 18B

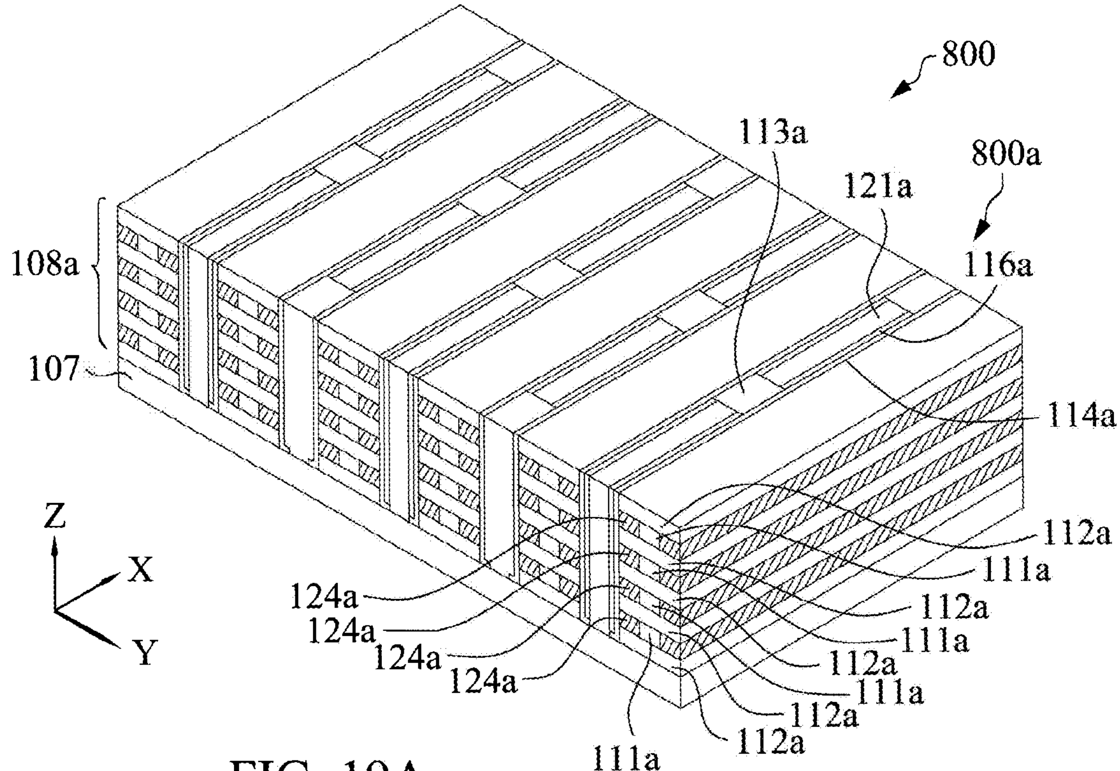


FIG. 19A

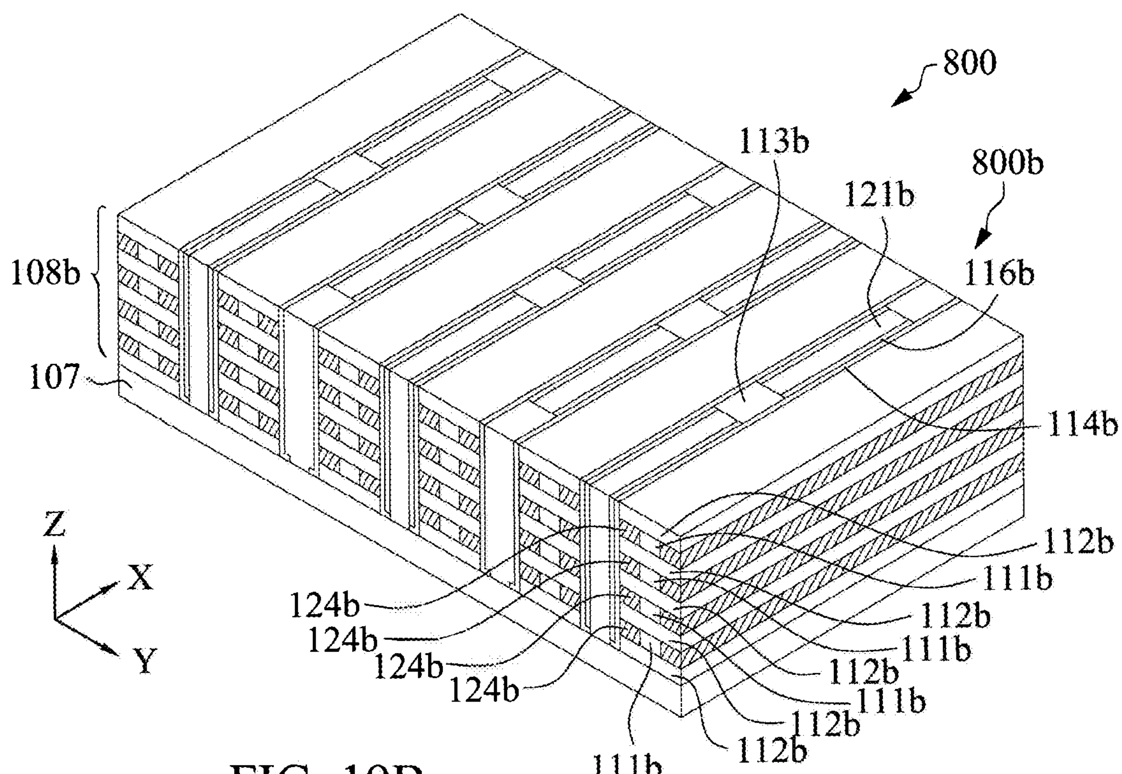


FIG. 19B

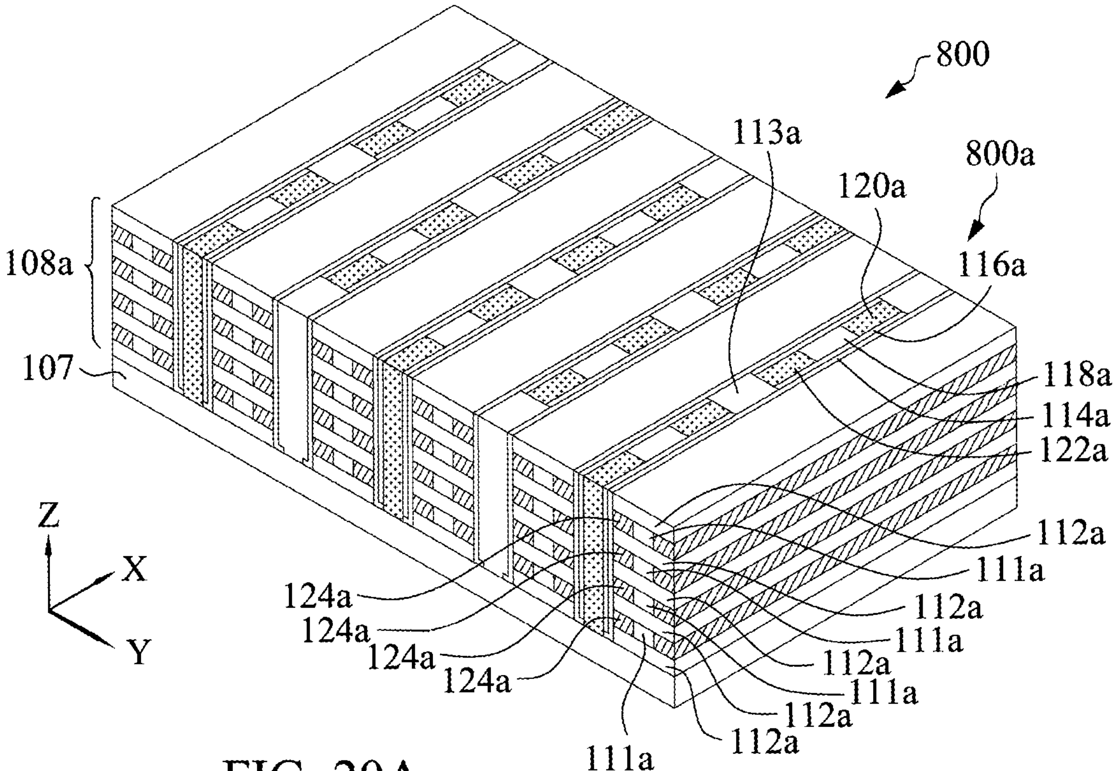


FIG. 20A

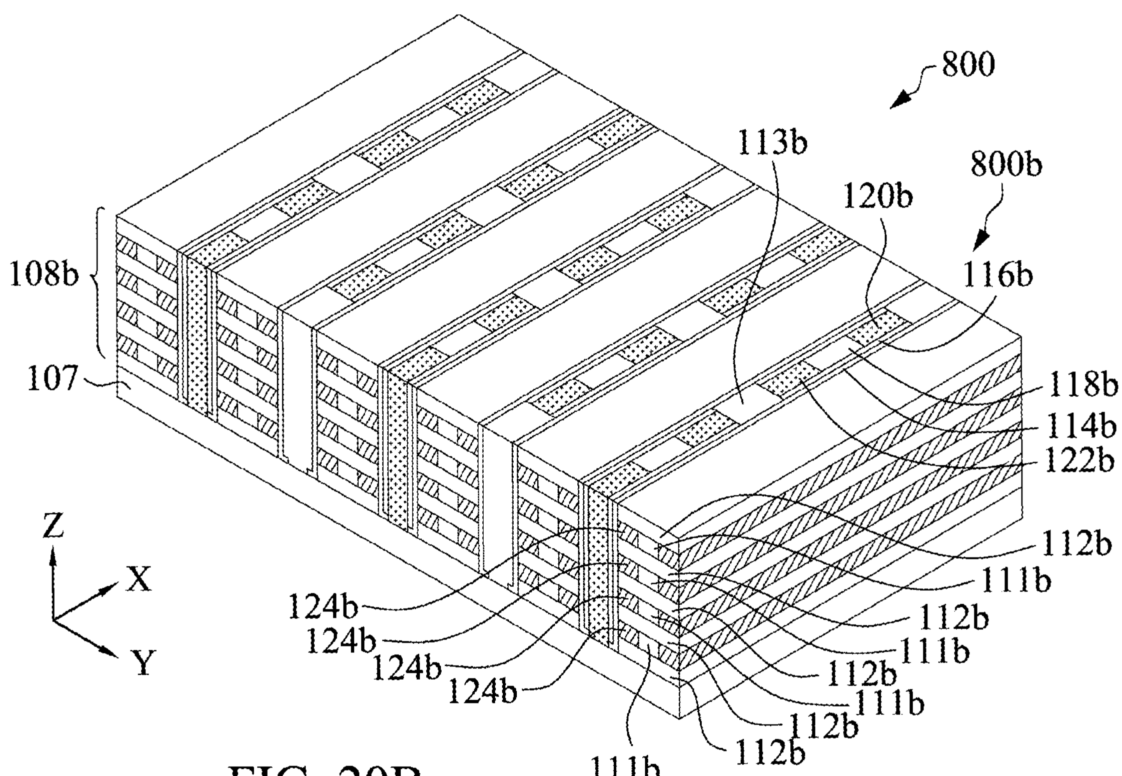


FIG. 20B

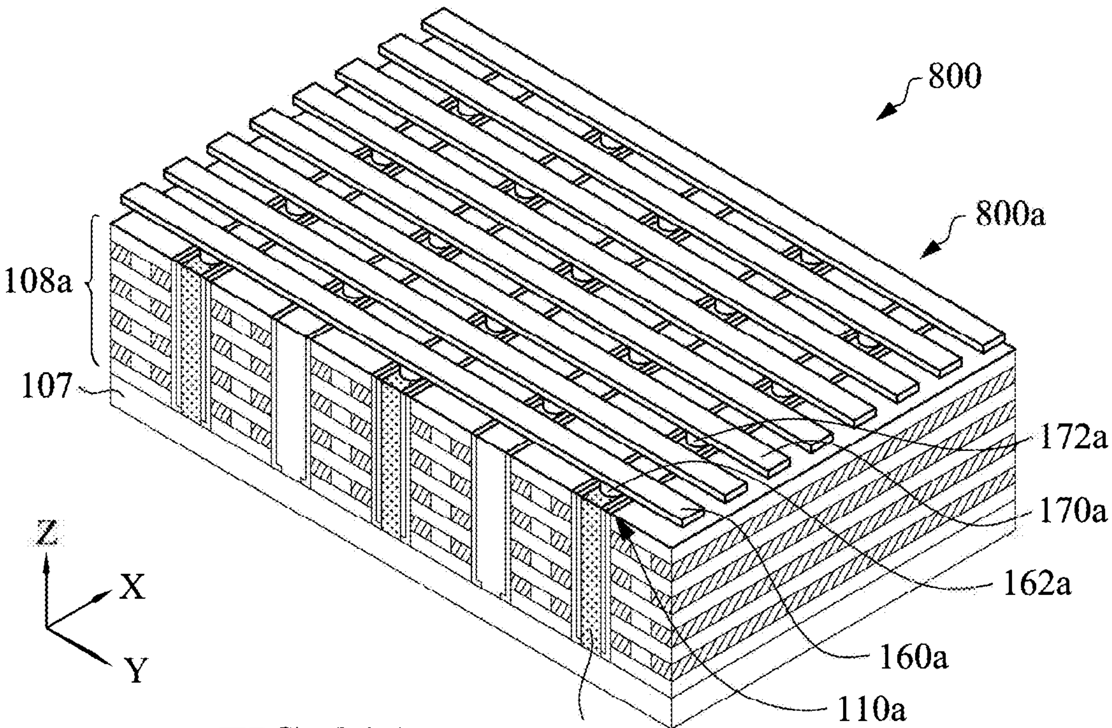


FIG. 21A

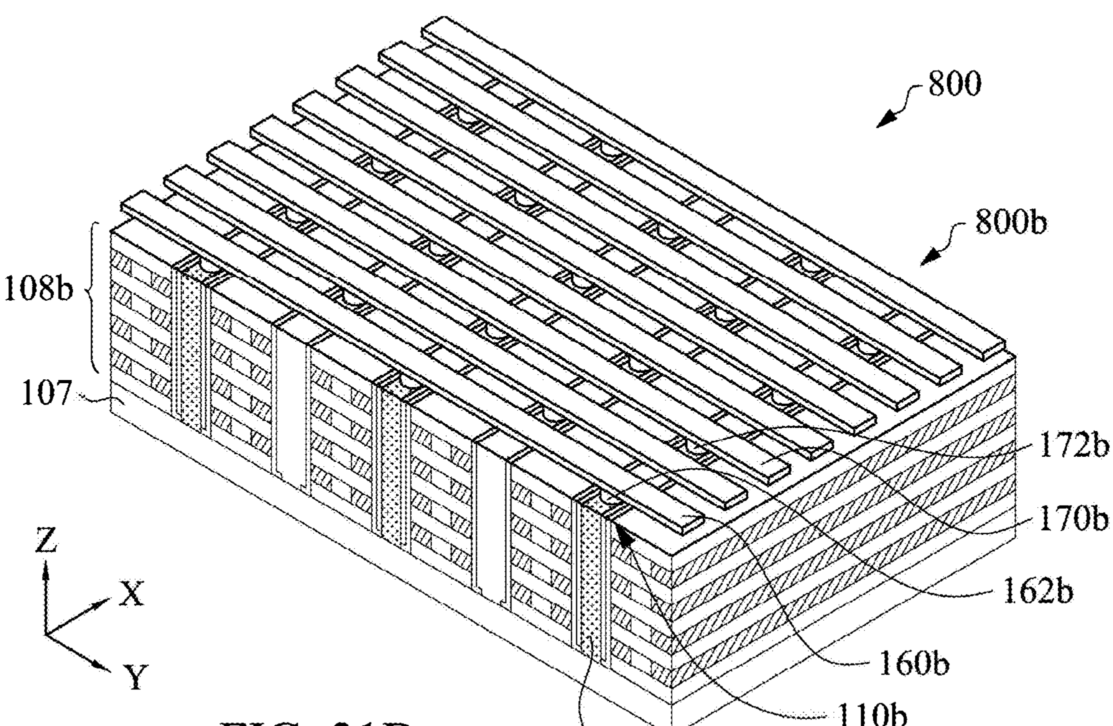


FIG. 21B

SEMICONDUCTOR DIES INCLUDING LOW AND HIGH WORKFUNCTION SEMICONDUCTOR DEVICES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Utility application Ser. No. 18/678,963, filed May 30, 2024, which is a divisional of U.S. application Ser. No. 17/585,932, filed Jan. 27, 2022 (now U.S. Pat. No. 12,069,862), which claims the benefit of and priority to U.S. Provisional Patent Application No. 63/225,228, filed Jul. 23, 2021, the entire disclosures of which are incorporated herein by reference for all purposes.

BACKGROUND

[0002] The present disclosure generally relates to semiconductor devices, and particularly to methods of making a 3-dimensional (3D) memory device.

[0003] The semiconductor industry has experienced rapid growth due to continuous improvements in the integration density of a variety of electronic components (e.g., transistors, diodes, resistors, capacitors, etc.). For the most part, this improvement in integration density has come from repeated reductions in minimum feature size, which allows more components to be integrated into a given area.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0005] FIG. **1** is a perspective view of a semiconductor die having a first array of a first set of semiconductor devices having a first workfunction disposed on a first side of the semiconductor die, and a second array of a second set of semiconductor devices having a second workfunction greater than the first workfunction disposed on a second side of the semiconductor die, according to embodiment.

[0006] FIG. **2** is a perspective view of a semiconductor die having a first set of semiconductor devices having a first workfunction, and a second set of semiconductor devices having a second workfunction greater than the first workfunction, the first set of semiconductor devices being disposed adjacent to the second set of semiconductor devices in at least a first direction, a second direction perpendicular to the first direction, or the first direction and the second direction, according to embodiment.

[0007] FIG. **3**A is a top, perspective view of a portion of the semiconductor die of FIG. **1** including the first set of semiconductor devices indicated by the arrow A in FIG. **1**, according to an embodiment.

[0008] FIG. **3**B is a top cross-section view of a first semiconductor device included in the first set of semiconductor devices of FIG. **3**A, taken along the line X-X in FIG. **3**A, according to an embodiment.

[0009] FIG. **4**A is a top, perspective view of a portion of the semiconductor die of FIG. **1** including the second set of semiconductor devices indicated by the arrow B in FIG. **1**, according to an embodiment.

[0010] FIG. **4**B is a top cross-section view of a second semiconductor device included in the second set of semiconductor devices of FIG. **4**A, taken along the line Y-Y in FIG. **4**A, according to an embodiment

[0011] FIG. **5**A is a top cross-section view of a first semiconductor device having a first workfunction, and FIG. **5**B is a top cross-section of a second semiconductor device having a second workfunction greater than the first workfunction, each of which can be included in the semiconductor die of FIG. **1** or FIG. **2**, according to an embodiment.

[0012] FIG. **6**A is a top cross-section view of a first semiconductor device having a first workfunction, and FIG. **6**B is a top cross-section of a second semiconductor device having a second workfunction greater than the first workfunction, each of which can be included in the semiconductor die of FIG. **1** or FIG. **2**, according to an embodiment.

[0013] FIG. **7**A is a top cross-section view of a first semiconductor device having a first workfunction, and FIG. **7**B is a top cross-section of a second semiconductor device having a second workfunction greater than the first workfunction, each of which can be included in the semiconductor die of FIG. **1** or FIG. **2**, according to an embodiment.

[0014] FIG. **8**A is a top cross-section view of a first semiconductor device having a first workfunction, and FIG. **8**B is a top cross-section of a second semiconductor device having a second workfunction greater than the first workfunction, each of which can be included in the semiconductor die of FIG. **1** or FIG. **2**, according to an embodiment.

[0015] FIG. **9**A is a top cross-section view of a first semiconductor device having a first workfunction, and FIG. **9**B is a top cross-section of a second semiconductor device having a second workfunction greater than the first workfunction, each of which can be included in the semiconductor die of FIG. **1** or FIG. **2**, according to an embodiment.

[0016] FIGS. **10**A-**10**B are schematic flow charts of a method for forming a semiconductor die, according to an embodiment.

[0017] FIGS. **11**, **12**, **13**A-**13**B, **14**A-**14**B, **15**A-**15**B, **16**A-**16**B, **17**A-**17**B, **18**A-**18**B, **19**A-**19**B, **20**A-**20**B, and **21**A-**21**B illustrate various views of an example semiconductor die (or a portion of the example semiconductor die) during various fabrication stages, made by the method of FIGS. **10**A-**10**B, in accordance with some embodiments.

DETAILED DESCRIPTION

[0018] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over, or on a second feature in the description that follows May include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0019] Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper" "top," "bottom" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0020] As used herein, the terms "about" and "approximately" generally mean plus or minus 10% of the stated value. For example, about 0.5 would include 0.45 and 0.55, about 10 would include 9 to 11, about 1000 would include 900 to 1100.

[0021] For next generation semiconductor devices, particularly memory devices, it is desirable to include memories that can perform high speed computing as well as memories that can provide long term storage (i.e., low leakage). Current semiconductor die manufacturing processes and semiconductor dies formed therefrom include high speed computing devices and the long term storage devices formed on separate dies, which are then integrated together using a chip integration process (e.g., using an interposer, or a 2.5 dimensional process). However, the separation between the two dies causes propagation delay as data is being transferred between computing and storage memory devices which can reduce data fidelity and increase processing time.

[0022] Embodiments of the present disclosure are discussed in the context of forming a semiconductor die, and particularly, in the context of forming semiconductor dies including 3D memory devices in which a first set of semiconductor devices that have low workfunction and provide high speed computing are formed monolithically with a second set of semiconductor devices that have high workfunction such that the second set of semiconductor devices provide long term storage. This beneficially reduces computing power needed to perform the same operation, reduces propagation losses, and reduces manufacturing cost, time, and complexity.

[0023] FIG. **1** is a perspective view of a semiconductor die **100**, according to an embodiment. The semiconductor die **100** has a first array **103***a* of a first set **104***a* of semiconductor devices **110***a* (hereinafter "first semiconductor devices **110***a*") disposed at a first location of the semiconductor die **100**, and a second array **103***b* of a second set **104***b* of second semiconductor devices **110***b* (hereinafter "second semiconductor devices **110***b*") disposed at a second location of the semiconductor die **100** different from the first location. For example, as shown in FIG. **1**, the first array **103***a* is disposed on a first side **102***a* (or first portion) of the semiconductor die **100** in a first direction (e.g., the X-direction), and the second array **103***b* is disposed on a second side **102***b* of the semiconductor die **100** in the first direction (e.g., the X-direction). An array isolation layer **109** is interposed between the first array **103***a* and the second array **103***b* and serves to electrically isolate the first array **103***a* from the second array **103***b* and extends in a second direction (e.g., the Y-direction) that is perpendicular to the first direction. The array isolation layer **109** may be formed from an electrically insulative material, for example, silicon dioxide (SiO_2), silicon nitride (SiN), silicon oxide (SiO), silicon carbide nitride (SiCN), silicon oxycarbonitride (SiOCN), silicon oxynitride (SiON), HfO2, TaO_X, TiO_X, AlO_X, any other suitable material, or combination thereof.

[0024] The first semiconductor devices **110***a* included in each of the first set **104***a* of the first array **103***a* are disposed in a 3D configuration. For example, the first semiconductor devices **110***a* in the first set **104***a* are stacked on top of each other in the vertical direction (e.g., the Z-direction), and disposed adjacent to each other in the first direction (e.g., the X-direction) and the second direction (e.g., the Y-direction). In other words, the first set **104***a* of the first semiconductor devices **110***a* are arranged in a cube formation. A first set of isolation layers **106***a* is interposed between each of the first set **104***a* of the first set of semiconductor devices **110***a* to electrically isolate each of the first set **104***a* of first semiconductor devices **110***a* from each other. For example, the first set of isolation layers **106***a* may include first portions that extend in the first direction (e.g., the X-direction) from a second portion that extends in the second direction (e.g., the Y-direction). The first set of isolation layers **106***a* may be formed from an electrically insulative material, for example, silicon dioxide (SiO_2), silicon nitride (SiN), silicon oxide (SiO), silicon carbide nitride (SiCN), silicon oxycarbonitride (SiOCN), silicon oxynitride (SiON), HfO2, TaO_X, TiO_X, AlO_X, any other suitable material, or combination thereof.

[0025] Similarly, the second semiconductor devices **110***b* included in each of the second set **104***b* of the second array **103***b* are disposed in a 3D configuration, for example, stacked on top of each other in the vertical direction (e.g., the Z-direction), and disposed adjacent to each other in the first direction (e.g., the X-direction) and the second direction (e.g., the Y-direction), similar to the first set **104***a* of the first semiconductor devices **110***a*. A second set of isolation layers **106***b* is interposed between each of the second set **104***b* of the second set of semiconductor devices **110***b* to electrically isolate each of the second set **104***b* of second semiconductor devices **110***b* from each other. For example, the second set of isolation layers **106***b* may include first portions that extend in the first direction (e.g., the X-direction) from a second portion that extends in the second direction (e.g., the Y-direction). The second set of isolation layers **106***b* may be formed from the same material as the first set of isolation layers **106***a*.

[0026] Each of the first set **104***a* of the first semiconductor devices **110***a* have a first workfunction to cause each of the first semiconductor devices **110***a* to store memory for a time period in a range of about 0.1 microsecond to 999 microsecond. Moreover, each of the second set **104***b* of second semiconductor devices **110***b* have a second workfunction to cause the second semiconductor devices **110***b* to store memory for a time period of greater than 5 years. In some embodiments, a ratio of the first workfunction to the second workfunction may be in range of 1:2 to 1:100, inclusive. Other ranges and values are contemplated and should be considered to be within the scope of the present application.

[0027] Expanding further, the first semiconductor devices **110***a* have a low workfunction such that the first semiconductor devices **110***a* have a high cell current, high endurance or lifetime (e.g., greater than $1e^{10}$ days), can retain data in a time range of microseconds (e.g., in a range of 0.1 microsecond to 999 microsecond, inclusive), but is unable to perform 2-bit computation due to data loss concerns. These properties allow the first semiconductor devices **110***a* to be used for data processing and computing operations. In contrast, the second semiconductor devices **110***b* have a high workfunction such that the second semiconductor devices **110***b* have a low cell current relative to the cell current of the first semiconductor devices **110***a*, lower endurance than the first semiconductor devices **110***a* (e.g., a ratio of the endurance of the first semiconductor devices **110***a* to the second semiconductor devices **110***b* may be in a range of 2:1 to 10:1), can retain or store data for a time period of greater than 10 years, and can perform 2-bit operation allowing high density storage. Thus, the second semiconductor devices **110***b* can be used for long term data storage of data generated after processing and computing by the first semiconductor devices **110***a*. Thus, the semiconductor die **100** integrates processing and computing, as well as long term memory storage in a single die reducing processing time, increasing processing speed, and reducing lag and propagation delays, and data loss.

[0028] FIG. **2** is a perspective view of a semiconductor die **200**, according to another embodiment. The semiconductor die **200** includes the first set **104***a* of second semiconductor devices **110***a* and the second set **104***b* of first semiconductor devices **110***b* as described with respect to the semiconductor die **100**. However, different from the semiconductor die **200**, the first set **104***a* of first semiconductor devices **110***a* is disposed adjacent to the second set **104***b* of the second semiconductor devices **110***b* in at least the first direction (e.g., the X-direction), the second direction (e.g., the Y-direction), or the first direction and the second direction. In other words, a first set **104***a* is disposed alternately with a second set **104***b* in the X-direction as well as the Y-direction throughout a length and a width of the semiconductor die **200**. A set isolation layer **206** interposed between each of the first set **104***a* and the second set **104***b*. For example, the set isolation layer **206** may include first portions that extend in the first direction (e.g., the X-direction) from a second portion that extends in the second direction (e.g., the Y-direction). The set isolation layer **206** may be formed from an electrically insulative material, for example, silicon dioxide (SiO_2), silicon nitride (SiN), silicon oxide (SiO), silicon carbide nitride (SiCN), silicon oxycarbonitride (SiOCN), silicon oxynitride (SiON), HfO2, TaO_X, TiO_X, AlO_X, any other suitable material, or combination thereof.

[0029] It should be appreciated that while semiconductor die **100** and semiconductor die **200** illustrate particular embodiments of the first set **104***a* of first semiconductor devices **110***a* and the second set **104***b* of the second semiconductor dies **110***b* arranged in specific configurations, in other embodiments the first set **104***a* of the first semiconductor devices **110***a* and the second set **104***b* of the second semiconductor devices **110***b* can be arranged in any suitable configuration or arrangement in a semiconductor die with an isolation layer electrical isolating adjacent sets **104***a*/**104***b* from each other. All such arrangements are contemplated and should be considered to be within the scope of the present disclosure.

[0030] FIG. **3**A is a top, perspective view of a first portion of the semiconductor die **100** of FIG. **1** including the first set **104***a* of the first semiconductor devices **110***a* indicated by the arrow A in FIG. **1**, and FIG. **4**A is a top, perspective view of a second portion of the semiconductor die **100** indicated by the arrow B in FIG. **1** that includes the second set **104***b* of the second semiconductor devices **110***b*, according to an embodiment. The semiconductor die **100** includes a substrate **107** (e.g., a silicon, or silicon on insulator (SOI) substrate, germanium, silicon oxide, silicon carbide, silicon-germanium, silicon nitride, or any other suitable substrate) on which the plurality of semiconductor devices **110***a/b* are disposed. The first semiconductor devices **110***a* and the second semiconductor devices **110***b* are respectively arranged in a plurality of rows within their respective sets **104***a/b*, each of which extend in a first direction (e.g., the direction). Each semiconductor device **110***a/b* is separated and electrically isolated from an adjacent semiconductor device **110***a/b* within a row by a device spacer **113***a/b*, which may be formed from an electrically insulating material [e.g., silicon oxide (SiO_2), silicon nitride (SiN), silicon oxide (SiO), silicon carbide nitride (SiCN), silicon oxycarbonitride (SiOCN), silicon oxynitride (SiON), HfO2, TaO_X, TiO_X, AlO_X, etc.].

[0031] FIG. **3**B is a top cross-section view of the first semiconductor device **110***a* included in the first set **104***a* of FIG. **3**A, taken along the line X-X in FIG. **3**A, and FIG. **4**B is a top cross-section view of the second semiconductor device **110***b* included in the second set **104***b* of FIG. **4**A, taken along the line Y-Y in FIG. **4**A. Referring now to FIGS. **3**A-**4**B, each semiconductor device **110***a/b* includes a source **120***a/b*, and a drain **122***a/b* spaced apart from the source **120***a/b* in a first direction (e.g., the X-direction). An inner spacer **118***a/b* is disposed between the source **120***a/b* and the drain **122***a/b*. A channel layer **116***a/b* is disposed on radially outer surfaces of the source **120***a/b* and the drain **122***a/b* in a second direction (e.g., the Y-direction) orthogonal to the first direction, and extends in the first direction. A memory layer **114***a/b* is disposed on a radially outer surface of the channel layer **116***a/b* in the second direction and extends in the first direction. The semiconductor device **110***a/b* may also include a stack **108***a/b* disposed on outer surfaces of the memory layer **114***a/b* in the second direction, the stack **108***a/b* comprising a plurality of insulating layers **112***a/b* and a plurality of gate layers **124***a/b* alternatively stacked on top of each other in a vertical direction (e.g., the Z-direction), and extending in the first direction (e.g., the X-direction).

[0032] Expanding further, the source **120***a/b* and the drain **122***a/b* may include a conducting material, for example, metals such as Al, Ti, TiN, TaN, Co, Ag, Au, Cu, Ni, Cr, Hf, Ru, W, Pt, WN, Ru, any other suitable material or a combination or alloy thereof. In some embodiments, the source **120***a/b* and/or the drain **122***a/b* may include a semiconductor material, for example, an n or p-doped semiconductor such as Si, SiGe, or any other semiconductor material (e.g., IGZO, ITO, IWO, poly silicon, amorphous Si, etc.), and may be formed using a deposition process, an epitaxial growth process, or any other suitable process. The source **120***a/b* extends from a top surface of the semiconductor die **100** to the substrate **107** in a vertical direction (e.g., the Z-direction).

[0033] The inner spacer **118***a/b* extends between the source **120***a/b* and the drain **122***a/b*. The inner spacer **118***a/b* may be formed from an electrically insulating material, for example, silicon nitride (SiN), silicon oxide (SiO), SiO_2, silicon carbide nitride (SiCN), silicon oxycarbonitride (SiOCN), silicon oxynitride (SiON), HfO2, TaO_X, TiO_X, AlO_X, etc. The inner spacer **118***a/b* extends from a top surface of the semiconductor die **100** to the substrate **107** in a vertical direction (e.g., the Z-direction).

[0034] A channel layer **116***a/b* is disposed outwards of a radially outer surface of the source **120***a/b* and the drain **122***a/b* in a second direction (e.g., the Y-direction) perpendicular to the first direction (e.g., the X-direction) and is in electrical contact with the source **120***a/b* and the drain **122***a/b*. The channel layer **116***a/b* extends from a top surface of the semiconductor die **100** to the substrate **107** in a vertical direction (e.g., the Z-direction). The channel layer **116***a/b* extends in the first direction (e.g., the X-direction) from an axially outward edge of the source **120***a/b* to an opposite axially outward edge of the drain **122***a/b*. In some embodiments, the channel layer **116***a/b* may be formed from a semiconductor material, for example, Si (e.g., polysilicon or amorphous silicon), Ge, SiGe, silicon carbide (SIC), IGZO, ITO, ZnO, IWO, etc. and can be an n-type or p-type doped semiconductor. In the particular embodiment shown in FIGS. **3**A-**4**B, each semiconductor device **110***a/b* includes a pair of channel layers **116***a/b*. One of the pair of channel layers **116***a/b* is disposed radially outwards of first radially outer surfaces of the source **120***a/b* and the drain **122***a/b* in the second direction (e.g., the Y-direction), and the other of the pair of channel layers **116***a/b* is disposed radially outwards of second radially outer surfaces of the source **120***a/b* and the drain **122***a/b* opposite the first radially outer surfaces. In other embodiments, each semiconductor device **110***a/b* may include a single channel layer **116***a/b* disposed radially outwards of the first or the second radially outer surfaces of the source **120***a/b* and the drain **122***a/b*. In some embodiments, the channel layer **116***a/b* may include a doped material (e.g., a doped semiconductor), doped with a first concentration of a dopant (e.g., an n-type or p-type dopant).

[0035] A memory layer **114***a/b* is disposed on a radially outer surface of the channel layer **116***a/b* in the second direction (e.g., the Y-direction) and extends in the first direction (e.g., the X-direction). The memory layer **114***a/b* extends from a top surface of the semiconductor die **100***a/b* to the substrate **107** in a vertical direction (e.g., the Z-direction). In some embodiments, the memory layer **114***a/b* may include a ferroelectric material, for example, lead zirconate titanate (PZT), $PbZr/TiO_3$, $BaTiO_3$, $PbTiO_2$, HfO_2, Hr1-x$Z_{rx}O_2$, ZrO_2, TiO_2, NiO, TaO_x, Cu_2O, Nb_2O_5, AlO_x, etc. The memory layer **114***a/b* extends in the first direction (e.g., the X-direction) along the axial extent of the semiconductor die **100** in the first direction such that each semiconductor device **110***a/b* located in a row of the array of semiconductor devices **110***a/b* includes a portion of the memory layer **114***a/b*, and the memory layer **114***a/b* is connected to each of the semiconductor devices **110***a/b* included in a corresponding row. In other embodiments, each of the semiconductor devices **110***a/b* includes a memory layer which extends from an axially outer edge of the source **120***a/b* to an opposite axially outer edge of the drain **122***a/b*. As described with respect to the channel layer **116***a/b*, while FIGS. **3**A and **4**A show two memory layers **114***a/b*, a portion of each of which is included in each of the semiconductor devices **110***a/b* included in a row, in other embodiments, each semiconductor device **110***a/b* may include a single memory layer.

[0036] The semiconductor device **110***a/b* may include at least one gate layer disposed on a radially outer surface of the memory layer **114***a/b* in the second direction (e.g., the Y-direction), and extending in the first direction (e.g., the X-direction). For example, as shown in FIG. **3**A and **4**A, the semiconductor die **100** also include a stack **108***a/b* disposed on the substrate **107**. The stack **108***a/b* is disposed on an outer surface of the memory layer **114***a/b*, for example, on outer surfaces of each of the memory layer **114***a/b* included in each row of semiconductor devices **110***a/b*, such that the stack **108***a/b* is interposed between adjacent rows of semiconductor devices **110***a/b*. As shown in FIGS. **3**A and **4**A, the stack **108***a/b* include a plurality of insulating layers **112***a/b*, and a plurality of gate layers **124***a/b* alternatively stacked on top of one another in the vertical direction or the Z-direction. Particularly, the first semiconductor devices **110***a* includes a first gate layer **124***a*, and the second semiconductor devices **110***b* includes a second gate layer **124***b* different from the first gate layer **124***a*. For example, the at least one second gate layer **124***b* included in each of the second set of second semiconductor devices **110***b* may have a second property different from a first property of the at least one first gate layer **124***a*, the first property configured to cause each of the first set **104***a* of the first semiconductor devices **110***a* to have a first workfunction, and the second property configured to cause each of the second set **104***b* of the second semiconductor devices **110***b* to have a second workfunction greater than the first workfunction, as described in further detail herein.

[0037] In some embodiments, a topmost layer and a bottommost layer of the stack **108***a/b* may include an insulating layer **112***a/b* of the plurality of insulating layers **112***a/b*. The bottommost insulating layer **112***a/b* may be disposed over the substrate **107**. The insulating layer **112***a/b* may include silicon nitride (SiN), silicon oxide (SiO), SiO_2, silicon carbide nitride (SiCN), silicon oxycarbonitride (SiOCN), silicon oxynitride (SiON), HfO2, TaO_X, TiO_X, AlO_X, etc. Within the stack **108***a/b*, two parallel gate layers **124***a/b* are located adjacent to each other and interposed between two vertically separated insulating layers **112***a/b* in the vertical direction (e.g., the Z-direction), each of the two gate layers **124***a/b* associated with a different semiconductor device **110***a/b*. A sacrificial layer **111***a/b* is interposed between the two gate layers **124***a/b* in the second direction (e.g., the Y-direction) and serves to electrically isolate the two gate layers **124***a/b* from each other. In some embodiments, an adhesive layer may be interposed between the gate layer/s **124***a/b* and the adjacent insulating layers **112***a/b* as well as the sacrificial layer **111***a/b* disposed therebetween, and facilitate adhesion of the gate layer **124***a/b* to the insulating layer **112***a/b*, and may also serve as a spacer between two parallel gate layers **124***a/b* that are interposed between the same vertically separated insulating layers **112***a/b*. In some embodiments, the adhesion layer (e.g., the adhesive layer) may include e.g., titanium (Ti), chromium (Cr), TiN, TaN, WN, or any other suitable adhesive material.

[0038] As described previously, the first semiconductor devices **110***a* have a first workfunction and the second semiconductor devices **110***b* have a second workfunction which is greater than the first workfunction. In the embodiment shown in FIGS. **3**A-**4**B, the source **120***a*, drain **122***a*, inner spacers **118***a*, channel layers **116***a*, and memory layers **114***a* included in the first semiconductor devices **110***a*, are substantially the same as the source **120***b*, drain **122***b*, inner spacer **118***b*, channel layers **116***b*, and memory layers **114***b* included in the second semiconductor devices **110***b*, i.e., are formed from the same material and are structurally and functionally similar to each other. However, the first gate layers **124***a* included in each of the first set **104***a* of first semiconductor devices **110***a* (FIGS. **3**A-**3**B) include a first material to cause the each of the first set **104***a* of first semiconductor devices **110***a* to have the first workfunction (e.g., the first material has the first workfunction), and the second gate layer **124***b* included in each of the second set **104***b* of second semiconductor devices **110***b* (FIG. **4**A-**4**B) comprises a second material different from the first material to cause each of the second set **104***b* of second semiconductor devices **110***b* to have the second workfunction that is greater than the first workfunction (e.g., the second material has the second workfunction). A workfunction value is associated with the material composition of the workfunction layer, i.e., the gate layers **124***a/b*, and thus, the material of the workfunction layer is chosen to tune its workfunction value so that a target threshold voltage V_t is achieved in the first semiconductor devices **110***a* and the second semiconductor devices **110***b* that is to be formed.

[0039] In particular embodiments, the first material of the first gate layer **124***a* may be a n-type or n-doped semiconductor material which causes the first semiconductor devices **110***a* to have the first workfunction. Example n-type workfunction metals that may include Ti, Ag, TaAl, TaAlC, TiAlN, TaC, TaCN, TaSiN, Mn, Zr, other suitable n-type workfunction materials, or combinations thereof. Moreover, the second material of the second gate layer **124***b* may include a p-type or p-doped semiconductor material which causes the second semiconductor devices **110***b* to have the second workfunction. Example p-type workfunction metals that may include TiN, TaN, Ru, Mo, Al, WN, $ZrSi_2$, $MoSi_2$, $TaSi_2$, $NiSi_2$, WN, other suitable p-type workfunction materials, or combinations thereof. While shown as including a single layer, each of the gate layers **124***a/b* may include multi-layers of the workfunction material, or combinations thereof.

[0040] While FIGS. **3**A-**4**B show particular embodiments of the first semiconductor devices **110***a* having a first workfunction and second semiconductor devices **110***b* having a second workfunction greater than the first workfunction, various configurations of first semiconductor devices having a low workfunction and second semiconductor devices having a high workfunction can be employed in the first set **104***a* and the second set **104***b* of the semiconductor die **100**, the semiconductor die **200**, or any other semiconductor die described herein. Example embodiments of first semiconductor devices and second semiconductor devices that can be included in the semiconductor die **100** or the semiconductor die **200** are shown and described in FIGS. **5**A-**9**B. It should be appreciated that while FIGS. **3**A-**4**B, **5**A-**5**B, **6**A-**6**B, **7**A-**7**B, **8**A-**8**B, and **9**A-**9**B illustrate particular combinations of first and second semiconductor devices having different workfunctions, the semiconductor die **100**, **200**, or any other semiconductor die described herein can include any combination of first and second semiconductor devices as described with respect to FIGS. **3**A-**9**B.

[0041] In some embodiments, a barrier layer may be used to define a workfunction of a semiconductor device. For example, FIG. **5**A is a top cross-section view of a first semiconductor device **210***a* having a first workfunction, and FIG. **5**B is a top cross-section view of a second semiconductor device **210***b* having a second workfunction greater than the first workfunction, which can be included in the semiconductor die **100**, **200**, or any other semiconductor die described herein. The first semiconductor device **210***a* is substantially similar to the first semiconductor device **110***a* and includes a first source **220***a* spaced apart from a first drain **222***a* in a first direction (e.g., the X-direction) with a first inner spacer **218***a* disposed therebetween. A first channel layer **216***a* is disposed on outer surfaces of the first source **220***a* and the first drain **222***a* in the second direction (e.g., the Y-direction) and extends in the first direction. A first memory layer **214***a* is disposed on an outer surface of the first channel layer **216***a*, and at least one first gate layer **224***a* is disposed on an outer surface of the first channel layer **216***a* in the second direction and extends in the first direction. The first material of the first gate layer **224***a* includes a n-type or n-doped semiconductor material which causes the first semiconductor devices **210***a* to have the first workfunction, as described with respect to the first semiconductor device **210***a*. The first gate layer **224***a* has a first thickness TGL**1** measured in the second direction (e.g., the Y-direction).

[0042] The second semiconductor device **210***b* includes a second source **220***b* spaced apart from a second drain **222***b* in the first direction (e.g., the X-direction) with a second inner spacer **218***b* disposed therebetween. A second channel layer **216***b* is disposed on outer surfaces of the second source **220***b* and the second drain **222***b* in the second direction (e.g., the Y-direction) and extends in the second direction. A second memory layer **214***b* is disposed on an outer surface of the second channel layer **216***b*. However, different from the second semiconductor device **110***b*, the second semiconductor device **210***b* includes a barrier layer **226***b* disposed on outer surface of the second memory layer **214***b* in the second direction and extending in the first direction. At least one second gate layer **224***b* is disposed on an outer surface of the barrier layer **226***b* in the second direction and extends in the first direction such that the barrier layer **226***b* is interposed between the second memory layer **214***b* and the at least one second gate layer **224***b*. A second material of the second gate layer **224***b* also includes an n-type or n-doped semiconductor material, which may be the same material used to form the first gate layer **224***a*. The barrier layer **226***b* is formed from any material that can be used to control the workfunction of the second semiconductor device **210***b*, for example, p-type workfunction material that may include TiN, TaN, Ru, Mo, Al, WN, $ZrSi_2$, $MoSi_2$, $TaSi_2$, $NiSi_2$, WN, other suitable high workfunction materials, or combinations thereof, or an n-type workfunction metals that may include Ti, Ag, TaAl, TaAlC, TiAlN, TaC, TaCN, TaSiN, Mn, Zr, other suitable n-type workfunction materials, or combinations thereof. In some embodiments, the barrier layer **226***b* includes a p-type or p-doped material.

[0043] The barrier layer **226***b* has a barrier layer thickness TBL. The material used to form the barrier layer **226***b* and the barrier layer thickness TBL can be adjusted to control workfunction of the second semiconductor device **210***b*, for example, by inhibiting metal diffusion form the second gate layer **224***b* which increases threshold voltage (V_t) and causes the second semiconductor device **210***b* to have the second workfunction that is greater than the first workfunction.

[0044] In some embodiments, the second gate layer **224***b* has a second thickness TGL**2** measured in the second direction (e.g., the Y-direction) that is less than the first thickness TGL**1**. For example, a ratio between the first thickness TGL**1** and the second thickness TGL**2** (TGL**1**:TGL**2**) may be in a range of 1:0.9 to 1:0.1, inclusive (e.g., 1:0.9, 1:0.8, 1:0.7, 1:0.6, 1:0.5, 1:0.4, 1:0.3, 1:0.2, or 1:0.1, inclusive). Moreover, the first thickness TGL**1** of the first gate layer **224**a may be approximately equal to (e.g., within ±10%) a sum of a second thickness TGL**2** of the second gate layer **224**b included in each of the second set of semiconductor devices **210**b and the thickness TBL of the barrier layer **226**b included in the second semiconductor device **210**b (i.e., TGL**1**=TGL**2**+TBL). These ranges are only examples and other ranges and values of first thickness TGL**1**, the second thickness, and the barrier layer TBL are contemplated and should be considered to be within the scope of this application.

[0045] In some embodiments, a thickness of a barrier layer may be adjusted to control a workfunction of semiconductor devices included in a semiconductor die. For example FIG. **6**A is a top cross-section view of a first semiconductor device **310**a having a first workfunction, and FIG. **6**B is a top cross-section of a second semiconductor device **310**b having a second workfunction greater than the first workfunction, which can be included in the semiconductor die **100**, **200** or any other semiconductor die described herein, according to an embodiment.

[0046] The first semiconductor device **310**a includes a first source **320**a spaced apart from a first drain **322**a in a first direction (e.g., the X-direction) with a first inner spacer **318**a disposed therebetween. A first channel layer **316**a is disposed on outer surfaces of the first source **320**a and the first drain **322**a in the second direction (e.g., the Y-direction) and extends in the first direction. A first memory layer **314**a is disposed on an outer surface of the first channel layer **316**a. However, different from the first semiconductor device **110**a, **210**a, the first semiconductor device **310**a includes a first barrier layer **326**a disposed on outer surface of the first memory layer **314**a in the second direction and extending in the first direction. At least one first gate layer **324**a is disposed on an outer surface of the first barrier layer **326**a in the second direction and extends in the first direction such that the first barrier layer **326**a is interposed between the first memory layer **314**a and the at least one first gate layer **324**a. A first material of the first gate layer **324**a includes an n-type or n-doped semiconductor material. The first barrier layer **326**a is formed from any material that can be used to control the workfunction of the first semiconductor device **310**a, for example, p-type workfunction material that may include TiN, TaN, Ru, Mo, Al, WN, $ZrSi_2$, $MoSi_2$, $TaSi_2$, $NiSi_2$, WN, other suitable high workfunction materials, or combinations thereof, or an n-type workfunction metals that may include Ti, Ag, TaAl, TaAlC, TiAlN, TaC, TaCN, TaSiN, Mn, Zr, other suitable n-type workfunction materials, or combinations thereof. In some embodiments, the first barrier layer **326**a includes a p-type or p-doped material. The first barrier layer **326**a has a first barrier thickness TBL**1** and the first gate layer **324**a has a first thickness TGL**1**.

[0047] The second semiconductor device **310**b includes a second source **320**b spaced apart from a second drain **322**b in the first direction (e.g., the X-direction) with a second inner spacer **318**b disposed therebetween. A second channel layer **316**b is disposed on outer surfaces of the second source **320**b and the second drain **322**b in the second direction (e.g., the Y-direction) and extends in the second direction. A second memory layer **314**b is disposed on an outer surface of the second channel layer **316**b. A second barrier layer **326**b disposed on outer surface of the second memory layer **314**b in the second direction and extending in the first direction. At least one second gate layer **324**b is disposed on an outer surface of the second barrier layer **326**b in the second direction and extends in the first direction such that the second barrier layer **326**b is interposed between the second memory layer **314**b and the at least one second gate layer **324**b. A second material of the second gate layer **324**b also includes a p-type or p-doped semiconductor material, which may be the same material used to form the first gate layer **324**a. Moreover, the second barrier layer **326**b may be formed from any material that can be used to control the workfunction of the second semiconductor device **310**b, for example, a p-type or p-doped material, or an n-type or n-doped material, for example, the same material or different material from the first barrier layer **326**a. In some embodiments, the second barrier layer **326**b includes a p-type or p-doped material.

[0048] The second barrier layer **326**b has a second barrier thickness TBL**2** and the second gate layer **324**b has a second thickness TGL**2**. The second barrier thickness TBL**2** of the second barrier layer **326**b is greater than the first barrier thickness TBL**1** of the first barrier layer **326**a. For example, a ratio between the first barrier thickness TBL**1** and the second barrier thickness TBL**2** may be in range of 0.1:1 to 0.9:1, inclusive (e.g., 0.1:1, 0.2:1, 0.3:1, 0.4:1, 0.5:1, 0.6:1, 0.7:1, 0.8:1, or 0.9:1, inclusive). The second barrier thickness TBL**2** of the second barrier layer **326**b creates a larger diffusion barrier between the second memory layer **314**b and the second gate layer **324**b of the second semiconductor device **310**b, relative to the thinner first barrier layer **326**a of the first semiconductor device **310**a, thereby causing the second workfunction of the second semiconductor device **310**b to be greater than the first workfunction of the first semiconductor device **310**a.

[0049] The first thickness TGL**1** of the first gate layer **324**a is greater than the second thickness TGL**2** of the second gate layer **324**b. For example, a ratio between the first thickness TGL**1** and the second thickness TGL**2** may be in a range of 1:0.1 to 1:0.9, inclusive (e.g., 1:0.1, 1:0.2, 1:0.3, 1:0.4, 1:0.5, 1:0.6, 1:0.7, 1:0.8, or 1:0.9, inclusive). In some embodiments, a first sum of the first thickness TGL**1** of the first gate layer **324**a and the first barrier thickness TBL**1** is approximately equal to a second sum of the second thickness TGL**2** of the second gate layer **324**b and the second barrier thickness TBL**2**. These ranges are only examples and other ranges and values of first thickness TGL**1**, the second thickness TGL**2**, and the barrier layer TBL**1** and TBL**2** are contemplated and should be considered to be within the scope of this application.

[0050] FIG. **7**A is a top cross-section view of a first semiconductor device **410**a having a first workfunction, and FIG. **7**B is a top cross-section of a second semiconductor device **410**b having a second workfunction greater than the first workfunction, which can be included in the semiconductor die **100**, **200** or any other semiconductor die described herein, according to another embodiment. The first and second semiconductor devices **410**a, **410**b depict another example embodiment of semiconductor devices in which a barrier layer thickness can be used to control the workfunction of semiconductor devices.

[0051] Expanding further, the first semiconductor device **410**a includes a first source **420**a spaced apart from a first drain **422**a in a first direction (e.g., the X-direction) with a first inner spacer **418**a disposed therebetween. A first channel layer **416**a is disposed on outer surfaces of the first source **420**a and the first drain **422**a in the second direction (e.g., the Y-direction) and extends in the first direction. A first memory layer **414***a* is disposed on an outer surface of the first channel layer **416***a*. The first semiconductor device **410***a* includes a first barrier layer **426***a* disposed on outer surface of the first memory layer **414***a* in the second direction and extending in the first direction. At least one first gate layer **424***a* is disposed on an outer surface of the first barrier layer **426***a* in the second direction and extends in the first direction such that the first barrier layer **426***a* is interposed between the first memory layer **414***a* and the at least one first gate layer **424***a*.

[0052] Different from the first semiconductor device **110***a*, **210***a*, **310***a*, a first material of the first gate layer **424***a* includes a p-type or p-doped semiconductor material, for example, TiN, TaN, Ru, Mo, Al, WN, $ZrSi_2$, $MoSi_2$, $TaSi_2$, $NiSi_2$, WN, other suitable high workfunction materials, or combinations thereof. Moreover, the first barrier layer **426***a* is formed from any material that can be used to control the workfunction of the first semiconductor device **410***a*, for example, p-type workfunction material that may include TiN, TaN, Ru, Mo, Al, WN, $ZrSi_2$, $MoSi_2$, $TaSi_2$, $NiSi_2$, WN, other suitable high workfunction materials, or combinations thereof, or an n-type workfunction metals that may include Ti, Ag, TaAl, TaAlC, TiAlN, TaC, TaCN, TaSiN, Mn, Zr, other suitable n-type workfunction materials, or combinations thereof. In some embodiments, the first barrier layer **426***a* includes a n-type or n-doped material. The first barrier layer **426***a* has a first barrier thickness TBL**1** and the first gate layer **424***a* has a first thickness TGL**1**.

[0053] The second semiconductor device **410***b* includes a second source **420***b* spaced apart from a second drain **422***b* in the first direction (e.g., the X-direction) with a second inner spacer **418***b* disposed therebetween. A second channel layer **416***b* is disposed on outer surfaces of the second source **420***b* and the second drain **422***b* in the second direction (e.g., the Y-direction) and extends in the second direction. A second memory layer **414***b* is disposed on an outer surface of the second channel layer **416***b*. A second barrier layer **426***b* disposed on outer surface of the second memory layer **414***b* in the second direction and extending in the first direction. At least one second gate layer **424***b* is disposed on an outer surface of the second barrier layer **426***b* in the second direction and extends in the first direction such that the second barrier layer **426***b* is interposed between the second memory layer **414***b* and the at least one second gate layer **424***b*. A second material of the first gate layer **424***a* also includes a p-type or p-doped semiconductor material, which may be the same material used to form the first gate layer **424***a*. Moreover, the second barrier layer **426***b* may be formed from any material that can be used to control the workfunction of the second semiconductor device **410***b*, for example, a p-type or p-doped material, or an n-type or n-doped material, for example, the same material or different material from the first barrier layer **426***a*. In some embodiments, the second barrier layer includes an n-type or n-doped material. The second barrier layer **426***b* has a second barrier thickness TBL**2** and the second gate layer **424***b* has a second thickness TGL**2**.

[0054] Different from the semiconductor devices **310***a/b*, the second barrier thickness TBL**2** of the second barrier layer **426***b* is less than the first barrier thickness TBL**1** of the first barrier layer **426***a*. For example, a ratio between the first barrier thickness TBL**1** and the second barrier thickness TBL**2** may be in range of 1:0.1 to 1:0.9, inclusive (e.g., 1:0.1, 1:0.2, 1:0.3, 1:0.4, 1:0.5, 1:0.6, 1:0.7, 1:0.8, or 1:0.9, inclusive). The first barrier thickness TBL**1** of the first barrier layer **426***a* creates a larger diffusion barrier relative to the second barrier thickness TBL**2** of the second barrier layer **426***b* such that the first barrier layer **426***a* allows less diffusion and in combination with the p-type first gate layer **424***a* causes the first semiconductor device **410***a* to have a low first workfunction. In contrast, the thinner second barrier layer **426***b* of the second semiconductor device **410***b* allows more diffusion and in combination with the p-type second gate layer **424***b* causes the second semiconductor device **410***b* to have the high second workfunction.

[0055] The first thickness TGL**1** of the first gate layer **424***a* is less than the second thickness TGL**2** of the second gate layer **424***b*. For example, a ratio between the first thickness TGL**1** and the second thickness TGL**2** may be in a range of 0.1:1 to 0.9:1, inclusive (e.g., 0.1:1, 0.2:1, 0.3:1, 0.4:1, 0.5:1, 0.6:1, 0.7:1, 0.8:1, or 0.9:1, inclusive). In some embodiments, a first sum of the first thickness TGL**1** of the first gate layer **424***a* and the first barrier layer **426***a* is approximately equal to a second sum of the second thickness TGL**2** of the second gate layer **424***b* and the second barrier thickness TBL**2**. These ranges are only examples and other ranges and values of first thickness TGL**1**, the second thickness, and the barrier layer TBL are contemplated and should be considered to be within the scope of this application.

[0056] In some embodiments, a thickness of the channel layer may be used to define a workfunction of the semiconductor devices included in the semiconductor die **100**, **200**, or any other semiconductor die described herein. For example, FIG. **8**A is a top cross-section view of a first semiconductor device **510***a* having a first workfunction, and FIG. **8**B is a top cross-section view of a second semiconductor device **510***b* having a second workfunction greater than the first workfunction, which can be included in the semiconductor die **100**, **200**, or any other semiconductor die described herein. The first semiconductor device **510***a* is substantially similar to the first semiconductor device **110***a* and includes a first source **520***a* spaced apart from a first drain **522***a* in a first direction (e.g., the X-direction) with a first inner spacer **518***a* disposed therebetween. A first channel layer **516***a* is disposed on outer surfaces of the first source **520***a* and the first drain **522***a* in the second direction (e.g., the Y-direction) and extends in the first direction. A first memory layer **514***a* is disposed on an outer surface of the first channel layer **516***a*, and at least one first gate layer **524***a* is disposed on an outer surface of the first channel layer **516***a* in the second direction and extends in the first direction. The first material of the first gate layer **524***a* may include an n-type or n-doped, or a p-type or p-doped semiconductor material. In some embodiments, the first gate layer **524***a* may include an n-type or n-doped material. Moreover, the first channel layer **516***a* may have a first channel thickness TCL**1**.

[0057] The second semiconductor device **510***b* includes a second source **520***b* spaced apart from a second drain **522***b* in the first direction (e.g., the X-direction) with a second inner spacer **518***b* disposed therebetween. A second channel layer **516***b* is disposed on outer surfaces of the second source **520***b* and the second drain **522***b* in the second direction (e.g., the Y-direction) and extends in the second direction. A second memory layer **514***b* is disposed on an outer surface of the second channel layer **516***b*. At least one second gate layer **524***b* is disposed on an outer surface of the second channel layer **516***b* in the second direction and extends in the first direction. A second material of the second gate layer **524***b* may include an n-type or n-doped semiconductor material, or a p-type or p-doped semiconductor material. In some embodiments, the second gate layer **524***b* includes a p-type or p-doped material. Different from the second semiconductor device **110***b*, **210***b*, **310***b*, **410***b*, the second channel layer **516***b* has a second channel thickness TCL**2** which is different from the first channel thickness TCL**1**, for example, greater than the first channel thickness TCL**1** of the first channel layer **516***a* such that the second semiconductor device **510***b* has the second workfunction that is greater than the first workfunction.

[0058] Adjusting the thickness of the second channel layer **516***b* relative to the first channel layer **516***a* is therefore, used to control depletion depth across the channel layer **516***a/b* and thus, the workfunction of the semiconductor devices **510***a/b*. In some embodiments, the first gate layer **524***a* includes an n-type material and the second gate layer **524***b* includes a p-type material. In such embodiments, the second channel thickness TCL**2** may be greater than the first channel thickness TCL**1**. For example, a ratio of the second channel thickness TCL**2** to the first channel thickness TCL**1** (TCL**2**:TCL**1**) may be in a range of 1.5:1 to 5:1, inclusive (e.g., 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 4.5:1, or 5:1, inclusive). In other embodiments, the first gate layer **524***a* includes a p-type or p-doped material and the second gate layer **524***b* includes an n-type or n-doped material. In such embodiments, the first channel thickness TCL**1** may be greater than the second channel thickness TCL**2**. For example, a ratio of the first channel thickness TCL**1** to the second channel thickness TCL**2** (TCL**1**:TCL**2**) may be in a range of 1.5:1 to 5:1, inclusive (e.g., 1.5:1, 2:1, 2.5:1, 3:1, 3.5:1, 4:1, 4.5:1, or 5:1, inclusive). These ranges are only examples and other ranges and values of first channel thickness TCL**1** and the second channel thickness TCL**2** are contemplated and should be considered to be within the scope of this application.

[0059] In some embodiments, a material of a channel layer may be selected to cause the semiconductor device to either have a low workfunction or a high workfunction such that the semiconductor die includes both the low workfunction and high workfunction semiconductor devices. For example, FIG. **9**A is a top cross-section view of a first semiconductor device **610***a* having a first workfunction, and FIG. **9**B is a top cross-section view of a second semiconductor device **610***b* having a second workfunction greater than the first workfunction, which can be included in the semiconductor die **100**, **200**, or any other semiconductor die described herein. The first semiconductor device **610***a* is substantially similar to the first semiconductor device **110***a* and includes a first source **620***a* spaced apart from a first drain **622***a* in a first direction (e.g., the X-direction) with a first inner spacer **618***a* disposed therebetween. A first channel layer **616***a* is disposed on outer surfaces of the first source **620***a* and the first drain **622***a* in the second direction (e.g., the Y-direction) and extends in the first direction. A first memory layer **614***a* is disposed on an outer surface of the first channel layer **616***a*, and at least one first gate layer **624***a* is disposed on an outer surface of the first channel layer **616***a* in the second direction and extends in the first direction. The first material of the first gate layer **624***a* may include an n-type or n-doped, or a p-type or p-doped semiconductor material. In some embodiments, the first gate layer **624***a* may include an n-type or n-doped material.

[0060] The first channel layer **616***a* is formed from a first material, for example, Si (e.g., polysilicon or amorphous silicon); Ge; SiGe; a compound semiconductor including silicon carbide (SiC); gallium arsenic; gallium phosphide; indium phosphide; indium arsenide; indium antimonide; indium gallium zinc oxide (IGZO); indium tin oxide (ITO); indium zinc oxide (IZO); indium tungsten oxide (IWO); an alloy semiconductor including SiGe, GaAsP, AlInAs, AlGaAs, GaInAs, GaInP, and/or GaInAsP; any other suitable material, or combinations thereof.

[0061] The second semiconductor device **610***b* includes a second source **620***b* spaced apart from a second drain **622***b* in the first direction (e.g., the X-direction) with a second inner spacer **618***b* disposed therebetween. A second channel layer **616***b* is disposed on outer surfaces of the second source **620***b* and the second drain **622***b* in the second direction (e.g., the Y-direction) and extends in the second direction. A second memory layer **614***b* is disposed on an outer surface of the second channel layer **616***b*. At least one second gate layer **624***b* is disposed on an outer surface of the second channel layer **616***b* in the second direction and extends in the first direction. A second material of the second gate layer **624***b* may include an n-type or n-doped semiconductor material, or a p-type or p-doped semiconductor material. The second material of the second gate layer **624***b* may be the same or different from the first material of the first gate layer **624***a*.

[0062] The second channel layer **616***b* is formed from a second channel material that is different from the first channel material of the first channel layer **616***a*, for example, Si (e.g., polysilicon or amorphous silicon); Ge; SiGe; a compound semiconductor including silicon carbide (SiC); gallium arsenic; gallium phosphide; indium phosphide; indium arsenide; indium antimonide; indium gallium zinc oxide (IGZO); indium tin oxide (ITO); indium zinc oxide (IZO); indium tungsten oxide (IWO); an alloy semiconductor including SiGe, GaAsP, AlInAs, AlGaAs, GaInAs, GaInP, and/or GaInAsP; any other suitable material, or combinations thereof.

[0063] For example, the first gate layer **624***a* and the second gate layer **624***b* may include a n-type material, and the first channel material may include a semiconductor material doped with a low concentration of a dopant which reduces threshold voltage and causes the first semiconductor device **610***a* to have the low first workfunction. Moreover, the second channel layer **616***b* also includes a semiconductor material (e.g., same or different from the first channel material) doped with a higher concentration of the dopant relative to the first semiconductor material which increases threshold voltage and causes the second semiconductor device **610***b* to have the high second workfunction. In other embodiments, the first channel material or the second channel material may be an oxide-based semiconductor. In such embodiments, the first channel layer **616***a* of the first semiconductor device **610***a* that has a low workfunction and high speed may have a lower amount of oxygen vacancies, relative to the second channel layer **616***b* of the second semiconductor device **610***b* that has a higher concentration of oxygen concentration. In this manner, by having a different channel material in the first semiconductor device **610***a* and the second semiconductor device **610***b*, the first semiconductor device **610***a* is configured to have a lower workfunction than the second semiconductor device **610***b*.

[0064] FIG. **10**A-**10**B illustrate a flowchart of a method **700** for forming a semiconductor die **800**, for example, a die including a plurality of 3D memory devices (e.g., any of the semiconductor devices described with respect to FIGS. **1-9**B), according to an embodiment. For example, at least some of the operations (or steps) of the method **700** may be used to form a die including a set of first semiconductor devices having a first workfunction (e.g., the first semiconductor device **110***a*, **210***a*, **310***a*, **410***a*, **510***a*, **610***a*) and a set of second semiconductor devices having a second workfunction greater than the first workfunction (e.g., the second semiconductor device **110***b*, **210***b*, **310***b*, **410***b*, **510***b*, **610***b*), which may include nanosheet transistors, a nanowire transistor devices, vertical transistor devices, or the like. It should be noted that the method **700** is merely an example, and is not intended to limit the present disclosure. Accordingly, it is understood that additional operations may be provided before, during, and after the method **700** of FIGS. **10**A-**10**B, and that some other operations may only be described briefly herein. In some embodiments, operations of the method **700** may be associated with perspective views and associate cross-section views of an example semiconductor die **800** at various fabrication stages as shown in FIGS. **11**, **12**, **13**A, **13**A, **14**B, **15**A, **15**B, **16**A, **16**B, **17**A, **17**B, **18**A, **18**B, **19**A, **19**B, **20**A, **20**B, **21**A, and **21**B in some embodiments are represented with respect to the semiconductor die **800** that represents a 3D memory device, the operations are equally applicable to any other semiconductor device, for example, the semiconductor devices **110***a/b*, **210***a/b*, **310***a/b*, **410***a/b*, **510***a/b*, **610***a/b* shown in FIGS. **1-9**B or any other semiconductor die (e.g., a GAA FET device, a nanosheet transistor device, a nanowire transistor device, a vertical transistor device, etc.). Although FIGS. **11-21**B illustrate the semiconductor die **800** including the set of semiconductor devices **110***a*/**110***b*, it is understood the semiconductor die **800** may include a number of other devices such as inductors, fuses, capacitors, coils, etc., which are not shown in FIGS. **11-21**B, for purposes of clarity of illustration.

[0065] The method **700** may generally include providing a substrate. A stack including a plurality of insulating layers and a plurality of sacrificial layers alternatively stacked on top of each other is formed on the substrate. At least a portion of first sacrificial layers of the plurality of sacrificial layers located in a stack first portion of the stack is replaced to form first gate layers. The method **700** also includes forming first channel layers extending in a first direction in the stack first portion, and forming first memory layers extending in the first direction in the stack first portion. Subsequently, at least a portion of second sacrificial layers of the plurality of sacrificial layers located in a stack second portion of the stack are replaced to form second gate layers. The method **700** also includes forming second channel layers extending in the first direction in the stack second portion, and forming second memory layers extending in the first direction in the stack second portion. The method **700** also includes forming: first sources and first drains spaced apart from a corresponding first source in the first direction such that a corresponding first channel layer is disposed on radially outer surface of the first sources and the first drains in the first direction to form a first set of semiconductor devices, and second sources and second drains spaced apart from a corresponding second source in the first direction such that a corresponding second channel layer is disposed on radially outer surface of the second sources and the second drains in the first direction to form a second set of semiconductor devices. Each of the first set of semiconductor devices has a first workfunction different from a second workfunction of each of the second set of semiconductor devices. In some embodiments, the first gate layers included in each of the first set of semiconductor devices includes a first material to cause the each of the first set of semiconductor devices to have the first workfunction, and the second gate layer included in each of the second set of semiconductor devices includes a second material different from the first material to cause each of the second set of semiconductor devices to have the second workfunction.

[0066] Expanding further, the method **700** starts with operation **702** that includes providing a substrate, for example, the substrate **107**. Corresponding to operation **702**, FIG. **11** shows a top, perspective view of the substrate **107**. The substrate **107** may be a semiconductor substrate, such as a bulk semiconductor, a semiconductor-on-insulator (SOI) substrate, or the like, which may be doped (e.g., with a p-type or an n-type dopant) or undoped. The substrate **107** may be a wafer, such as a silicon wafer. Generally, an SOI substrate includes a layer of a semiconductor material formed on an insulator layer. The insulator layer may be, for example, a buried oxide (BOX) layer, a SiO layer, a SiN layer, any other suitable insulator layer or combination thereof. The insulator layer is provided on a substrate, typically a silicon or glass substrate. Other substrates, such as a multi-layered or gradient substrate may also be used. In some embodiments, the semiconductor material of the substrate **107** may include silicon; germanium; a compound semiconductor including silicon carbide, gallium arsenic, gallium phosphide, indium phosphide, indium arsenide, and/or indium antimonide; an alloy semiconductor including SiGe, GaAsP, AlInAs, AlGaAs, GaInAs, GaInP, and/or GaInAsP, any other suitable semiconductor material, or combinations thereof. In other embodiments, the substrate **107** may include an etch stop layer that may be formed using a plasma deposition process, for example, using PVD, CVD, LPCVD, PECVD, ALD, MBE, HARP, any other suitable process or a combination thereof. In various embodiments, the substrate **107** may include SiN, SiO, SiO_2, SiCN, SiOCN, SiON, HfO2, TaO_X, TiO_X, AlO_X, a metal carbide, any other suitable material or combination thereof, and may include a single layer or various sublayers.

[0067] At operation **704**, a stack (e.g., the stack **108** shown in FIGS. **3**A, **4**A, and **12**) is formed on the substrate **107**. The stack **108** includes a plurality of insulating layers (e.g., the insulating layers **112**) and a plurality of sacrificial layers (e.g., the sacrificial layers **111** shown in FIGS. **3**A, **4**A, and **12**) alternately stacked on top of each other in the vertical direction (e.g., the Z-direction). Corresponding to operation **704**, FIG. **12** is a top, perspective view of the semiconductor die **800** after forming the stack **108** on top of the substrate **107**. The insulating layers **112** and the sacrificial layers **111** are alternately disposed on top of one another in the Z-direction. For example, one of the sacrificial layers **111** is disposed over one of the insulating layers **112**, then another one of the insulating layers **112** is disposed on the sacrificial layer **111**, so on and so forth. As shown in FIG. **12**, a topmost layer (e.g., a layer distal most from the substrate **107**) and a bottommost layer (e.g., a layer most proximate to the substrate **107**) of the stack **108** may include an insulating layer **112**. While FIG. **12** shows the stack **108** as including

5 insulating layers **112** and 4 sacrificial layers, the stack **108** may include any number of insulating layers **112** and sacrificial layers **111** (e.g., 4, 5, 6, 7, 8, 16, 24, 48, 64, 128, or even more). In various embodiments, if the number of sacrificial layers **111** in the stack **108** is n, a number of insulating layers **112** in the stack **108** may be n+1.

[0068] In some embodiments, each of the plurality of insulating layers **112** may have about the same thickness, for example, in a range of about 5 nm to about 100 nm, inclusive. Moreover, the sacrificial layers **111** may have the same thickness or different thickness from the insulating layers **112**. The thickness of the sacrificial layers **111** may range from a few nanometers to few tens of nanometers (e.g., in a range of 5 nm to 100 nm, inclusive, but other ranges and values are also contemplated and are within the scope of this disclosure). In other embodiments, a topmost sacrificial layer **111** and/or a bottom most sacrificial layer **111** may be thicker (e.g., 1.2×, 1.4×. 1.6×, 1.8×, 2×, 2.5×, or 3× thicker) than the other sacrificial layers **111** disposed therebetween.

[0069] The insulating layers **112** and the sacrificial layers **111** have different compositions. In various embodiments, the insulating layers **112** and the sacrificial layers **111** have compositions that provide for different oxidation rates and/or different etch selectivity between the respective layers. In some embodiments, the insulating layers **112** may be formed from SiO, and the sacrificial layers **111** may be formed from SiN. In various embodiments, the insulating layers **112** may be formed from any suitable first material (e.g., an insulating material) as described with respect to the semiconductor die **100**, and the sacrificial layers **111** may be formed from a second material (e.g., also an insulating material) that is different from the first material. In some embodiments, the sacrificial layers **111** may include SiN, HfO_2, TaOx, TiO_x, AlO_x, or any other material that has a high etch selectivity relative to the insulating layers **112** (e.g., an etch selectivity ratio of at least 1:100). The sacrificial layers **111** are merely spacer layers that are eventually removed and do not form an active component of the semiconductor die **800**.

[0070] In various embodiments, the insulating layers **112** and/or the sacrificial layers **111** may be epitaxially grown from the substrate **107**. For example, each of the insulating layers **112** and the sacrificial layers **111** may be grown by a MBE process, a CVD process such as a metal organic CVD (MOCVD) process, a furnace CVD process, and/or other suitable epitaxial growth processes. In other embodiments, the insulating layers **112** and the sacrificial layers **111** may be grown using an atomic layer deposition (ALD) process.

[0071] At operation **706**, a plurality of first portion first trenches are formed in a stack first portion of the stack of the semiconductor die. At operation **708**, an exposed surfaces of first sacrificial layers included in the stack first portion are partially etched. However, no operation is performed in a stack second portion of the stack of the semiconductor die during operations **706** and **708**. Corresponding to operation **706-708**, FIG. **13**A is a top, perspective view of a first portion **800***a* of the semiconductor die **800** including a stack first portion **108***a* after forming a plurality of first portion first trenches **132***a* up to the substrate **107** and partially etching first sacrificial layers **111***a*, and FIG. **13**B is top, perspective view of a second portion **800***b* of the semiconductor die **800** including a stack second portion **108***b* on which no processing operation is performed. The stack first portion **108***a* includes first insulating layers **112***a* and first sacrificial layers **111***a*. The plurality of first portion first trenches **132***a* extend in the X-direction and are formed through the stack first portion **108***a* up to the substrate **107** by etching the stack first portion **108***a* in the Z-direction. The etching process for forming the plurality of first portion first trenches **132***a* may include a plasma etching process, which can have a certain amount of anisotropic characteristic. For example, the first portion first trenches **132***a* may be formed, for example, by depositing a photoresist or other masking layer on a top surface of the first portion **800***a* of the semiconductor die **800**, i.e., the top surface of the topmost first insulating layer **112***a* of the stack first portion **108***a*, and a pattern corresponding to the first portion first trenches **132***a* defined in the masking layer (e.g., via photolithography, e-beam lithography, or any other suitable lithographic process). In other embodiments, a hard mask may be used.

[0072] Subsequently, the stack first portion **108***a* may be etched using a plasma etching process (including radical plasma etching, remote plasma etching, and other suitable plasma etching processes, RIE, DRIE), gas sources such as Cl_2, HBr, CF_4, CHF_3, CH_2F_2, CH_3F, C_4F_6, BCl_3, SF_6, H_2, NF_3, and other suitable etch gas sources and combinations thereof can be used with passivation gases such as N_2, O_2, CO_2, SO_2, CO, CH_4, $SiCl_4$, and other suitable passivation gases and combinations thereof. Moreover, for the plasma etching process, the gas sources and/or the passivation gases can be diluted with gases such as Ar, He, Ne, and other suitable dilutive gases and combinations thereof to form the first portion first trenches **132***a*. As a non-limiting example, a source power of 10 Watts to 3,000 Watts, a bias power of 0 watts to 3,000 watts, a pressure of 1 millitorr to 5 torr, and an etch gas flow of 0 sccm to 5,000 sccm may be used in the etching process. However, it is noted that source powers, bias powers, pressures, and flow rates outside of these ranges are also contemplated. As shown in FIG. **13**A, the etch used to form the plurality of first portion first trenches **132***a* etches through each of the first sacrificial layers **111***a* and first insulating layers **112***a* of the stack first portion **108***a* such that each of the plurality of first portion first trenches **132***a* extend form the topmost first insulating layer **112***a* through the bottommost first insulating layer **112***a* to the substrate **107**.

[0073] Next, exposed surfaces of the first sacrificial layers **111***a* within the first portion first trenches **132***a* are partially etched so as to reduce a width of the first sacrificial layers **111***a* relative to the first insulating layers **112***a* in the stack first portion **108***a*. For example, the exposed surfaces extend in the X-direction and etching the exposed surfaces of the first sacrificial layers **111***a* reduces a width of the first sacrificial layers **111***a* on either side of the first sacrificial layers **111***a* in the Y-direction. In some embodiments, the first sacrificial layers **111***a* may be etched using a wet etch process (e.g., hydrofluoric etch, buffered hydrofluoric acid, phosphoric acid, etc.). In other embodiments, the exposed surfaces of the sacrificial layers **111***a* may be partially etched using a plasma etching process (including radical plasma etching, remote plasma etching, and other suitable plasma etching processes, RIE, DRIE), gas sources such as Cl_2, HBr, CF_4, CHF_3, CH_2F_2, CH_3F, C_4F_6, BCl_3, SF_6, H_2, NF_3, and other suitable etch gas sources and combinations thereof can be used with passivation gases such as N_2, O_2, CO_2, SO_2, CO, CH_4, $SiCl_4$, and other suitable passivation gases and combinations thereof. Moreover, for the plasma etching process, the gas sources and/or the passivation gases can be diluted with gases such as Ar, He, Ne, and other suitable dilutive gases and combinations thereof. As a non-limiting example, a source power of 10 Watts to 3,000 Watts, a bias power of 0 watts to 3,000 watts, a pressure of 1 millitorr to 5 torr, and an etch gas flow of 0 sccm to 5,000 sccm may be used in the etching process. However, it is noted that source powers, bias powers, pressures, and flow rates outside of these ranges are also contemplated.

[0074] Partially etching the first sacrificial layers **111***a* in the Y-direction reduces a width of the first sacrificial layers **111***a* relative to the first insulating layers **112***a* disposed in the stack first portion **108***a* such that first cavities **117***a* are formed whose boundaries are formed by top and bottom surfaces of adjacent first insulating layers **112***a* and a surface of the partially etched first sacrificial layers **111***a* that face the first portion first trenches **132***a* and extend in the X-direction. In some embodiments, an adhesive layer may be formed on exposed portions of sidewalls of the first cavities **117***a,* and the sidewalls of the first insulating layer **112***a* that form a sidewall of the first portion first trenches **132***a* facilitate adhesion of gate layers to these surfaces. In various embodiments, the adhesive layers may include a material that has good adhesion with each of the first insulating layers **112***a,* the sacrificial layers **111***a,* and the gate layers **124***a,* for example, Ti, Cr, TiN, WN, etc. The adhesive layers may be deposited using any suitable method including, for example, molecular beam deposition (MBD), ALD, CVD, PECVD, MOCVD, epitaxial growth, and the like. In some embodiments, the adhesive layer may have a thickness in a range of 0.1 nm to 5 nm, inclusive, or any other suitable thickness. In other embodiments, the adhesion layer is excluded.

[0075] At operation **710**, first gate layers are formed in first cavities of the stack first portion, but no processing operation is performed in the stack second portion. Corresponding to operation **710**, FIG. **14**A is a top, perspective view of the stack first portion after forming first gate layers **124***a* in the first cavities **117***a,* and FIG. **14**B is a top, perspective view of the stack second portion **180***b* where no processing operation is performed. In various embodiments, the first gate layers **124***a* are formed by depositing a gate dielectric and/or gate metal in the first cavities **117***a* (e.g., over the adhesive layer), such that the portion of the first gate layers **124***a* is continuous along the walls of each of the first portion first trenches **132***a.* In various embodiments, the first gate layers **124***a* may be formed from a high-k dielectric material. Although, each of the portion of the first gate layers **124***a* shown in FIG. **14**A is shown as a single layer, in other embodiments, the first gate layers **124***a* can be formed as a multi-layer stack (e.g., including a gate dielectric layer and a gate metal layer), while remaining within the scope of the present disclosure. The first gate layers **124***a* may be formed of different high-k dielectric materials or a similar high-k dielectric material. Example high-k dielectric materials include a metal oxide or a silicate of Hf, Al, Zr, La, Mg, Ba, Ti, Pb, and combinations thereof (e.g., Al, Ti, TiN, TaN, Co, Ag, Au, Cu, Ni, Cr, Hf, Ru, W, Pt, WN, Ru, etc.). The portion of the gate layers **124***a* can be deposited using any suitable method, including, for example, MBD, ALD, CVD, PECVD, MOCVD, epitaxial growth, and the like.

[0076] In some embodiments, the first gate layers **124***a* may be formed from a first material having a first workfunction which causes the first semiconductor devices **110***a* formed in the first portion **800***a* to have low first workfunction, as previously described herein. In some embodiments, the first gate layers **124***a* may include a stack of multiple metal materials. For example, the gate metal may be a p-type workfunction layer, an n-type workfunction layer, multi-layers thereof, or combinations thereof. The workfunction layer may also be referred to as a workfunction metal. Example p-type workfunction metals that may include TiN, TaN, Ru, Mo, Al, WN, $ZrSi_2$, $MoSi_2$, $TaSi_2$, $NiSi_2$, WN, other suitable p-type workfunction materials, or combinations thereof. Example n-type workfunction metals that may include Ti, Ag, TaAl, TaAlC, TiAlN, TaC, TaCN, TaSiN, Mn, Zr, other suitable n-type workfunction materials, or combinations thereof. A workfunction value is associated with the material composition of the workfunction layer, and thus, the material of the workfunction layer is chosen to tune its workfunction value so that a target threshold voltage V_t is achieved in the device that is to be formed, i.e., a low threshold voltage in the first semiconductor devices **110***a.* The workfunction layer(s) may be deposited by CVD, PVD, ALD, and/or other suitable process.

[0077] At operation **712**, a first memory layer is formed in each of the plurality of first portion first trenches on exposed radial surfaces of the insulating layers and the portion of the gate layers located in the second trenches, such that the first memory layer extends in the first direction (e.g., the X-direction), and from the top surface of the semiconductor die to the substrate. At operation **714**, a first channel layer structure is formed within each of the plurality of first portion first trenches on exposed radial surfaces of the first memory layer such that the channel layer structure also extends in the first direction. At operation **716**, the plurality of first portion first trenches are filled with an insulating material to form first isolation layers. However, no processing operation is performed on the stack second portion during operations **712-716**.

[0078] Corresponding to operations **712-716**, FIG. **15**A is a top, perspective view of the first portion **800***a* of the semiconductor die **800** after forming first channel layer structure **115***a,* first memory layer **114***a,* and first isolation layers **140***a,* and FIG. **15**B is a top, perspective view of the second portion **800***b* on which no processing operation is performed. The first memory layer **114***a* may include a ferroelectric material, for example, lead zirconate titanate (PZT), $PbZr/TiO_3$, $BaTiO_3$, $PbTiO_2$, HfO_2, Hr1-$xZ_{rx}O_2$, ZrO_2, TiO_2, NiO, TaO_x, Cu_2O, Nb_2O_5, AlO_x, etc. The first memory layer **114***a* may be formed using PVD, CVD, LPCVD, PECVD, ALD, MBE, any other suitable process or a combination thereof. A conformal coating may be deposited such that the first memory layer **114***a* is continuous on the walls of the first portion first trenches **132***a.*

[0079] The first channel layer structure **115***a* is formed on a radially inner surface of the first memory layer **114***a* in the Y-direction. In some embodiments, the first channel layer structure **115***a* may be formed from a semiconductor material, for example, Si (e.g., polysilicon or amorphous silicon that may be n-type or p-type), Ge, SiGe, silicon carbide (SiC), IGZO, ITO, IZO, ZnO, IWO, etc. The first channel layer structure **115***a* may be formed using PVD, CVD, LPCVD, PECVD, ALD, MBE, any other suitable process or a combination thereof. A conformal coating may be deposited such that the first channel layer structure **115***a* is continuous on the radially inner surface of the first memory layer **114***a.* In some embodiments, the first channel layer structure **115***a* may be formed from a first channel material or have a first channel thickness to cause the first semiconductor devices **110**a formed in the first portion **800**a to have the first workfunction as previously described herein.

[0080] The insulating material may be deposited in the first portion first trenches **132**a to form the first isolation layers **140**a using any suitable method, for example, MBD, ALD, CVD, PECVD, MOCVD, epitaxial growth, and the like. The first isolation layer **140**a may include SiO_2, SiON, SiN, SiCN, HfO_2, TaO_x, TiO_x, AlO_x, etc. In some embodiments, the first isolation layers **140**a may be formed from the same material of the first insulating layers **112**a. A CMP operation may be performed after filling the first portion first trenches **132**a with the insulating material to form the first isolation layers **140**a to planarize the top surface of the semiconductor die **800**.

[0081] At operation **718**, a plurality of second portion first trenches are formed in the stack second portion of the stack of the semiconductor die. At operation **720**, exposed surfaces of second sacrificial layers included in the stack second portion are partially etched. However, no operation is performed in the stack first portion of the stack of the semiconductor die during operations **718** and **720**. Corresponding to operation **718-720**, FIG. **16**B is a top, perspective view of a second portion **800**b of the semiconductor die **800** including the stack second portion **108**b after forming a plurality of second portion first trenches **132**b up to the substrate **107** and partially etching exposed surfaces of second sacrificial layers **111**b including the stack second portion **180**b, and FIG. **16**A is top, perspective view of the first portion **800**a of the semiconductor die **800** on which no processing operation is performed during operations **718-720**.

[0082] The stack second portion **108**b includes second insulating layers **112**b and second sacrificial layers **111**b. The plurality of second portion first trenches **132**b extend in the X-direction and are formed through the stack second portion **108**b up to the substrate **107** by etching the stack second portion **108**b in the Z-direction. The etching process for forming the plurality of second portion first trenches **132**b may include a plasma etching process, which can have a certain amount of anisotropic characteristic. For example, the second portion first trenches **132**b may be formed, for example, by depositing a photoresist or other masking layer on a top surface of the second portion **800**b of the semiconductor die **800**, i.e., the top surface of the topmost second insulating layer **112**b of the stack second portion **108**b, and a pattern corresponding to the second portion first trenches **132**b defined in the masking layer (e.g., via photolithography, e-beam lithography, or any other suitable lithographic process). In other embodiments, a hard mask may be used.

[0083] Subsequently, the stack second portion **108**b may be etched using a plasma etching process (including radical plasma etching, remote plasma etching, and other suitable plasma etching processes, RIE, DRIE), gas sources such as Cl_2, HBr, CF_4, CHF_3, CH_2F_2, CH_3F, C_4F_6, BCl_3, SF_6, H_2, NF_3, and other suitable etch gas sources and combinations thereof can be used with passivation gases such as N_2, O_2, CO_2, SO_2, CO, CH_4, $SiCl_4$, and other suitable passivation gases and combinations thereof. Moreover, for the plasma etching process, the gas sources and/or the passivation gases can be diluted with gases such as Ar, He, Ne, and other suitable dilutive gases and combinations thereof to form the second portion first trenches **132**b. As a non-limiting example, a source power of 10 Watts to 3,000 Watts, a bias power of 0 watts to 3,000 watts, a pressure of 1 millitorr to 5 torr, and an etch gas flow of 0 sccm to 5,000 sccm may be used in the etching process. However, it is noted that source powers, bias powers, pressures, and flow rates outside of these ranges are also contemplated. As shown in FIG. **16**B, the etch used to form the plurality of second portion first trenches **132**b etches through each of the second sacrificial layers **111**b and the second insulating layers **112**b of the stack second portion **108**b such that each of the plurality of second portion first trenches **132**b extend form the topmost second insulating layer **112**b through the bottommost second insulating layer **112**b to the substrate **107**.

[0084] Next, exposed surfaces of the second sacrificial layers **111**b within the second portion first trenches **132**b are partially etched so as to reduce a width of the second sacrificial layers **111**b relative to the second insulating layers **112**b in the stack second portion **108**b. For example, the exposed surfaces extend in the X-direction and etching the exposed surfaces of the second sacrificial layers **111**b reduces a width of the second sacrificial layers **111**b on either side of the second sacrificial layers **111**b in the Y-direction. In some embodiments, the second sacrificial layers **111**b may be etched using a wet etch process (e.g., hydrofluoric etch, buffered hydrofluoric acid, phosphoric acid, etc.). In other embodiments, the exposed surfaces of the second sacrificial layers **111**b may be partially etched using a plasma etching process (including radical plasma etching, remote plasma etching, and other suitable plasma etching processes, RIE, DRIE), gas sources such as Cl_2, HBr, CF_4, CHF_3, CH_2F_2, CH_3F, C_4F_6, BCl_3, SF_6, H_2, NF_3, and other suitable etch gas sources and combinations thereof can be used with passivation gases such as N_2, O_2, CO_2, SO_2, CO, CH_4, $SiCl_4$, and other suitable passivation gases and combinations thereof. Moreover, for the plasma etching process, the gas sources and/or the passivation gases can be diluted with gases such as Ar, He, Ne, and other suitable dilutive gases and combinations thereof. As a non-limiting example, a source power of 10 Watts to 3,000 Watts, a bias power of 0 watts to 3,000 watts, a pressure of 1 millitorr to 5 torr, and an etch gas flow of 0 sccm to 5,000 sccm may be used in the etching process. However, it is noted that source powers, bias powers, pressures, and flow rates outside of these ranges are also contemplated.

[0085] Partially etching the second sacrificial layers **111**b in the Y-direction reduces a width of the second sacrificial layers **111**b relative to the second insulating layers **112**b disposed in the stack second portion **108**b such that second cavities **117**b are formed whose boundaries are formed by top and bottom surfaces of adjacent second insulating layers **112**b and a surface of the partially etched second sacrificial layers **111**b that face the second portion first trenches **132**b and extend in the X-direction. In some embodiments, an adhesive layer may be formed on exposed portions of sidewalls of the second cavities **117**b, as previously described herein with respect to the first cavities **117**a.

[0086] At operation **722**, second gate layers are formed in second cavities of the stack second portion, but no processing operation is performed in the stack first portion. Corresponding to operation **722**, FIG. **17**B is a top, perspective view of the stack second portion **180**b after forming second gate layers **124**b in the second cavities **117**b and FIG. **17**A is a top, perspective view of the stack first portion **180**a where no processing operation is performed. In various embodiments, the second gate layers **124**b are formed by depositing a gate dielectric and/or gate metal in the second cavities **117***b* (e.g., over the adhesive layer), such that the portion of the second gate layers **124***b* is continuous along the walls of each of the second portion first trenches **132***b*. In various embodiments, the second gate layers **124***b* may be formed from a high-k dielectric material. Although, each of the second gate layers **124***b* shown in FIG. **17**B is shown as a single layer, in other embodiments, the second gate layers **124***b* can be formed as a multi-layer stack (e.g., including a gate dielectric layer and a gate metal layer), while remaining within the scope of the present disclosure. The second gate layers **124***b* may be formed of different high-k dielectric materials or a similar high-k dielectric material. Example high-k dielectric materials include a metal oxide or a silicate of Hf, Al, Zr, La, Mg, Ba, Ti, Pb, and combinations thereof (e.g., Al, Ti, TiN, TaN, Co, Ag, Au, Cu, Ni, Cr, Hf, Ru, W, Pt, WN, Ru, etc.). The second gate layers **124***b* can be deposited using any suitable method, including, for example, MBD, ALD, CVD, PECVD, MOCVD, epitaxial growth, and the like.

[0087] In some embodiments, the second gate layers **124***b* may be formed from a second material having a second workfunction which causes the second semiconductor devices **110***b* formed in the second portion **800***b* to have the high second workfunction, as previously described herein. In some embodiments, the second gate layers **124***b* may include a stack of multiple metal materials. For example, the gate metal may be a p-type workfunction layer, an n-type workfunction layer, multi-layers thereof, or combinations thereof. The workfunction layer may also be referred to as a workfunction metal. Example p-type workfunction metals that may include TiN, TaN, Ru, Mo, Al, WN, $ZrSi_2$, $MoSi_2$, $TaSi_2$, $NiSi_2$, WN, other suitable p-type workfunction materials, or combinations thereof. Example n-type workfunction metals that may include Ti, Ag, TaAl, TaAlC, TiAlN, TaC, TaCN, TaSiN, Mn, Zr, other suitable n-type workfunction materials, or combinations thereof. A workfunction value is associated with the material composition of the workfunction layer, and thus, the material of the workfunction layer is chosen to tune its workfunction value so that a target threshold voltage V_t is achieved in the device that is to be formed, i.e., a high threshold voltage in the second semiconductor devices **110***b*. The workfunction layer(s) may be deposited by CVD, PVD, ALD, and/or other suitable process.

[0088] At operation **724**, a second memory layer is formed in each of the plurality of second portion first trenches on exposed radial surfaces of the second insulating layers and the portion of the second gate layers located in the second portion first trenches, such that the second memory layer extends in the first direction (e.g., the X-direction), and from the top surface of the semiconductor die to the substrate. At operation **726**, a second channel layer structure is formed within each of the plurality of second portion first trenches on exposed radial surfaces of the second memory layer such that the second channel layer structure also extends in the first direction. At operation **728**, the plurality of second portion first trenches are filled with an insulating material to form second isolation layers. However, no processing operation is performed on the stack first portion during operations **724-728**.

[0089] Corresponding to operations **724-728**, FIG. **18**B is a top, perspective view of the second portion **800***b* of the semiconductor die **800** after forming second channel layer structure **115***b*, second memory layer **114***b*, and second isolation layers **140***b*, and FIG. **18**A is a top, perspective view of the first portion **800***a* on which no processing operation is performed. The second memory layer **114***b* may include a ferroelectric material, for example, lead zirconate titanate (PZT), PbZr/TiO_3, $BaTiO_3$, $PbTiO_2$, HfO_2, Hr1-$xZ_{rx}O_2$, ZrO_2, TiO_2, NiO, TaO_x, Cu_2O, Nb_2O_5, AlO_x, etc. The second memory layer **114***b* may be formed using PVD, CVD, LPCVD, PECVD, ALD, MBE, any other suitable process or a combination thereof. A conformal coating may be deposited such that the second memory layer **114***b* is continuous on the walls of the second portion first trenches **132***b*.

[0090] The second channel layer structure **115***b* is formed on a radially inner surface of the second memory layer **114***b* in the Y-direction. In some embodiments, the second channel layer structure **115***b* may be formed from a semiconductor material, for example, Si (e.g., polysilicon or amorphous silicon that may be n-type or p-type), Ge, SiGe, silicon carbide (SiC), IGZO, ITO, IZO, ZnO, IWO, etc. The second channel layer structure **115***b* may be formed using PVD, CVD, LPCVD, PECVD, ALD, MBE, any other suitable process or a combination thereof. A conformal coating may be deposited such that the second channel layer structure **115***b* is continuous on the radially inner surface of the second memory layer **114***b*. In some embodiments, the second channel layer structure **115***b* may be formed from a second channel material or have a second channel thickness to cause the second semiconductor devices **110***b* formed in the second portion **800***b* to have the second workfunction, as previously described herein.

[0091] The insulating material may be deposited in the second portion first trenches **132***b* to form the second isolation layers **140***b* using any suitable method, for example, MBD, ALD, CVD, PECVD, MOCVD, epitaxial growth, and the like. The second isolation layers **140***b* may include SiO_2, SiON, SiN, SiCN, HfO_2, TaO_x, TiO_x, AlO_x, etc. In some embodiments, the second isolation layers **140***b* may be formed from the same material as the second insulating layers **112***b*. A CMP operation may be performed after filling the first portion first trenches **132***a* with the insulating material to form the first isolation layers **140***a* to planarize the top surface of the semiconductor die **800**.

[0092] At operation **730**, first channel layers and second channel layers are formed. At operation **732**, first and second device spacers are formed. Corresponding to operation **732-734**, FIG. **19**A is a top, perspective view of the first portion **800***a* and FIG. **19**B is a top, perspective view of the second portion **800***b*, after forming first channel layers **116***a* and first device spacers **113***a* in the first portion, and second channel layers **116***b* and second device spacers **113***b* in the second device portion **800***b*. The first and second portions **800***a* and **800***b* are now processed simultaneously. The channel layers **116***a/b* may be formed by etching through portions of the isolation layers **140***a/b* and adjacent portions of the channel layer structures **115***a/b* in the Z-direction up to the substrate **107**, such that an array of first channel layers **116***a* are formed in the first portion **800***a*, and an array of second channel layers **116***b* are formed in the second portion **800***b*, which are co-extensive with first inner spacer structures **121***a* and second inner spacer structures **121***b* formed from the first isolation layer **140***a* and the second isolation layer **140***b*, respectively.

[0093] The isolation layers **140***a/b* and the channel layer structures **115***a/b* may be etched simultaneously or sequentially, using a dry etch, for example, a plasma etching process (including radical plasma etching, remote plasma etching, and other suitable plasma etching processes, RIE, DRIE), gas sources such as Cl_2, HBr, CF_4, CHF_3, CH_2F_2, CH_3F, C_4F_6, BCl_3, SF_6, H_2, NF_3, and other suitable etch gas sources and combinations thereof can be used with passivation gases such as N_2, O_2, CO_2, SO_2, CO, CH_4, $SiCl_4$, and other suitable passivation gases and combinations thereof. Moreover, for the plasma etching process, the gas sources and/or the passivation gases can be diluted with gases such as Ar, He, Ne, and other suitable dilutive gases and combinations thereof to form the channel layers **116***a/b* and the inner spacer structures **121***a/b*. As a non-limiting example, a source power of 10 Watts to 3,000 Watts, a bias power of 0 watts to 3,000 watts, a pressure of 1 millitorr to 5 torr, and an etch gas flow of 0 sccm to 5,000 sccm may be used in the etching process. The cavities formed due to the etching process are then filled with an insulating material (e.g., using MBD, ALD, CVD, PECVD, MOCVD, epitaxial growth, and the like), for example, the same material used to form the isolation layers **140***a/b*, to form the device spacers **113***a/b* with the inner spacer structures **121***a/b* disposed between adjacent device spacers **113***a/b*. Thus, a plurality of rows that include the memory layers **114***a/b* and the channel layers **116***a/b* are formed in the semiconductor die first portion **800***a* and second portion **800***b*, respectively, extending in the X-direction, and having device spacers **113***a/b* disposed at regular intervals separating adjacent semiconductor devices **110***a/b* that will be form in subsequent steps in the semiconductor die **800**. A CMP operation may be performed after forming the device spacers **113***a/b* to planarize the top surface of the semiconductor die **800**.

[0094] At operation **734**, a first source and first drain are formed in the first portion **800***a*, and second source and second drain are formed in the second portion **800***b*. Corresponding to operation **734**, FIG. **20**A is a top, perspective view of the first portion **800***a* of the semiconductor die **800** after forming first sources **120***a* and first drains **122***a*, and FIG. **20**B is a top, perspective view of the second portion **800***b* of the semiconductor die **800** after forming second sources **120***b* and second drains **122***b*. To form the sources **120***a/b* and drains **122***a/b*, cavities may be formed at axial ends of the inner spacer structures **121***a/b* in the X-direction to form inner spacers **118***a/b* by etching through the inner spacer structures **121***a/b* in the Z-direction. The cavities may be formed using a dry etch, for example, a plasma etching process (including radical plasma etching, remote plasma etching, and other suitable plasma etching processes, RIE, DRIE), gas sources such as Cl_2, HBr, CF_4, CHF_3, CH_2F_2, CH_3F, C_4F_6, BCl_3, SF_6, H_2, NF_3, and other suitable etch gas sources and combinations thereof can be used with passivation gases such as N_2, O_2, CO_2, SO_2, CO, CH_4, $SiCl_4$, and other suitable passivation gases and combinations thereof. Moreover, for the plasma etching process, the gas sources and/or the passivation gases can be diluted with gases such as Ar, He, Ne, and other suitable dilutive gases and combinations thereof to form the third cavities. As a non-limiting example, a source power of 10 Watts to 3,000 Watts, a bias power of 0 watts to 3,000 watts, a pressure of 1 millitorr to 5 torr, and an etch gas flow of 0 sccm to 5,000 sccm may be used in the etching process.

[0095] Sources **120***a/b* and drains **122***a/b* are formed by filling the cavities with the source and the drain material, respectively. The sources **120***a/b* and the drains **122***a/b* may be formed by depositing the drain material in the cavities using an epitaxial growth process, PVD, CVD, LPCVD, PECVD, ALD, MBE, any other suitable process or a combination thereof, a HARP, another applicable process, or combinations thereof. In-situ doping (ISD) may be applied to form doped sources **120***a/b* or drains **122***a/b*, thereby creating the junctions for each semiconductor devices **110***a/b*. N-type devices can be formed by implanting arsenic (As) or phosphorous (P), and p-type devices can be formed by implanting boron (B). The sources **120***a/b* and drains **122***a/b* are located at opposite axial ends of corresponding inner spacers **118***a/b*. Portions of radially outer surface of the sources **120***a/b* and drains **122***a/b* are in contact with corresponding portions of a radially inner surface of the channel layer **116***a/b*. A CMP operation may be performed after forming the sources **120***a/b* drains **122***a/b* to planarize the top surface of the semiconductor die **800**.

[0096] At operation **736**, first and second global source lines, and first and second global drain line are formed on a top surface of the stack first portion disposed in the first portion **800***a*, and on a top surface of the stack second portion disposed in the second portion of the semiconductor die, respectively, and electrically coupled to corresponding sources and drains. Corresponding to operation **736**, FIG. **21**A is a top, perspective view of the first portion **800***a* showing the first global source lines **160***a* and first global drain lines **170***a* coupled to corresponding first sources **120***a* and first drains **122***a* through first source vias **162***a* and first drain vias **172***a*, respectively. Similarly, FIG. **21**B is a top, perspective view of the second portion **800***b* showing the second global source lines **160***b* and second global drain lines **170***b* coupled to corresponding second sources **120***b* and second drains **122***b* via second source vias **162***b* and second drain vias **172***b*, respectively.

[0097] In some embodiments, to form the global source lines **160***a/b* and global drain lines **170***a/b*, source vias **162***a/b* are formed on a top surface of the corresponding sources **120***a/b* and drain vias **172***a/b* are formed on top surfaces of the corresponding drains **122***a/b*. The source vias **162***a/b* and the drain vias **172***a/b* may be formed from a conducting material for example, tungsten (W), copper (Cu), cobalt (Co), etc. In some embodiments, the source vias **162***a/b* and the drain vias **172***a/b* may be formed using a dual damascene process. For example, a cavity may be formed in the sources **120***a/b* and the drains **122***a/b*. In some embodiments, a spacer layer may be deposited on a top surface of the semiconductor die **800** (e.g., a top surface of the topmost insulating layer **112***a/b*) and throughholes formed in the spacer layer at locations corresponding to the source vias **162***a/b* and drain vias **172***a/b*.

[0098] In some embodiments, a diffusion barrier (e.g., a Ta based material) may be deposited in each of the fourth cavities, and a thin metal (e.g., Cu) seed layer is deposited on the diffusion barrier (e.g., using PVD, CVD, MBOE, ALD, etc.). This is followed by electroplating of the metal (e.g., Cu) on the metal seed layer until the metal fills the trenches and projects axially upwards of the sources **120***a/b* and the drains **122***a/b*. This process can be repeated until the source vias **162***a/b* and the drain vias **172***a/b* having a desired height are obtained. The sacrificial layer may be removed before or after forming the source vias **162***a/b* and the drain vias **172***a/b*, or be left disposed on the top surface of the semiconductor die **800**.

[0099] The plurality of global source lines **160***a/b* are formed that are coupled to a set of the source vias **162***a/b* and thereby, a set of sources **120***a/b*. Similarly, a set of global drain lines **170***a/b* are formed that are coupled to a set of the drain vias **172***a/b* and thereby, a set of drains **122***a/b*, and may be formed simultaneously with the global source lines **160***a/b*. Each of the global source lines **160***a/b* and the global drain lines **170***a/b* extend in the Y-direction. The global source lines **160***a/b* and the global drain lines **170***a/b* may be formed from a conducting material, for example, tungsten (W), copper (Cu), cobalt (Co), etc. The global source lines **160***a/b* and the global drain lines **170***a/b* may also be formed using a dual damascene process, for example, after formation of the source vias **162***a/b* and drain vias **172***a/b* before removing the spacer layer. While the semiconductor die **800** is shown without the spacer layer, in some embodiments, the spacer layer may remain included in the final semiconductor die **800**. The global source lines **160***a/b* and the global drain lines **170***a/b* may be used to communicate an electrical signal (e.g., a current or voltage) to corresponding sources **120***a/b*, and the global drain lines **170***a/b* may be used to receive an electrical signal (e.g., a current or voltage) from a corresponding drain **122***a/b*, when the gate layer **124***a/b* is activated.

[0100] In some embodiments, a semiconductor die comprises a first set of semiconductor devices disposed at a first location of the semiconductor die, each of the first set of semiconductor devices having a first workfunction to cause each of the first set of semiconductor devices to store memory for a first time. The semiconductor die also includes a second set of semiconductor devices disposed at a second location of the semiconductor die different from the first location, each of second set of semiconductor devices having a second workfunction that is greater than the first workfunction to cause each of the second set of semiconductor devices to store memory for a second time period greater than the first time period.

[0101] In some embodiments, a semiconductor die comprises a first set of semiconductor devices disposed at a first location of the semiconductor die, and a second set of semiconductor devices disposed at a second location of the semiconductor die different from the first location. Each of the first and second set of semiconductor devices comprises a source, a drain spaced apart from the source in a first direction, and a channel layer disposed radially outwards of at least one radially outer surface of the source and the drain in a second direction perpendicular to the first direction and extending in the first direction. A memory layer is disposed on a radially outer surface of the channel layer in the second direction and extends in the first direction. At least one first gate layer is disposed on a radially outer surface of the memory layer. The at least one gate layer included in each of the first set of semiconductor devices has a first property and the at least one gate layer included in each of the second set of semiconductor devices has a second property different from the first property, the first property configured to cause each of the first set of semiconductor devices to have a first workfunction, and the second property configured to cause each of the second set of semiconductor devices to have a second workfunction greater than the first workfunction.

[0102] In some embodiments, a method of making a semiconductor die comprises providing a substrate, and forming a stack comprising a plurality of insulating layers and a plurality of sacrificial layers alternatively stacked on top of each other. The method comprises replacing at least a portion of first sacrificial layers of the plurality of sacrificial layers located in a stack first portion of the stack to form first gate layers. The method comprises forming first channel layers extending in a first direction in the stack first portion. The method comprises forming first memory layers extending in the first direction in the stack first portion. The method comprises subsequently, replacing at least a portion of second sacrificial layers of the plurality of sacrificial layers located in a stack second portion of the stack to form second gate layers. The method comprises forming second channel layers extending in the first direction in the stack second portion, and forming second memory layers extending in the first direction in the stack second portion. The method comprises forming: first sources and first drains spaced apart from a corresponding first source in the first direction such that a corresponding first channel layer is disposed on radially outer surface of the first sources and the first drains in the first direction to form a first set of semiconductor devices, and second sources and second drains spaced apart from a corresponding second source in the first direction such that a corresponding second channel layer is disposed on radially outer surface of the second sources and the second drains in the first direction to form a second set of semiconductor devices. Each of the first set of semiconductor devices has a first workfunction different from a second workfunction of each of the second set of semiconductor devices.

[0103] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A semiconductor die, comprising:

a plurality of first semiconductor devices arranged in a first set that extends vertically along a first direction, the first semiconductor devices each having a first workfunction;

a plurality of second semiconductor devices arranged in a second set that extends vertically along the first direction, the second semiconductor devices each having a second workfunction that is greater than the first workfunction; and

an isolation layer extending vertically along the first direction and laterally along a second direction, the isolation layer interposed between the first set and the second set along a third direction perpendicular to the first direction and the second direction.

2. The semiconductor die of claim **1**, further comprising:

a plurality of the first semiconductor devices arranged in a third set that extends vertically along the first direction; and a plurality of the second semiconductor devices arranged in a fourth set that extends vertically along the first direction.

3. The semiconductor die of claim **2**, wherein:

the third set is disposed adjacent to the first set along the second direction or the third direction, and

the fourth set is disposed adjacent to the second set along the second direction or the third direction.

4. The semiconductor die of claim **3**, wherein:

the isolation layer is a first isolation layer,

the semiconductor die further comprises:

a second isolation layer extending vertically along the first direction and between the first set and the third set, the second isolation layer including a first portion extending laterally along the second direction and a second portion extending laterally along the third direction; and

a third isolation layer extending vertically along the first direction and between the second set and the fourth set, the third isolation layer including a first portion extending laterally along the second direction and a second portion extending laterally along the third direction, and

the first isolation layer extends between the second isolation layer and the third isolation layer.

5. The semiconductor die of claim **2**, wherein:

the first set and the fourth set are disposed adjacent to one another along the second direction, and

the second set and the third set are disposed adjacent to one another along the second direction.

6. The semiconductor die of claim **5**, wherein:

the isolation layer is the first isolation layer that extends between the third set and the fourth set, and

the semiconductor die further comprises a second isolation layer extending vertically along the first direction and laterally along the third direction, the second isolation layer separating the first set from the fourth set along the second direction and separating the second set from the third set laterally along the second direction.

7. The semiconductor die of claim **1**, wherein:

the first set includes the first semiconductor devices stacked vertically along the first direction and spaced laterally along the second direction and the third direction, respectively, and

the second set includes the second semiconductor devices stacked vertically along the first direction and spaced laterally along the second direction and the third direction, respectively.

8. The semiconductor die of claim **1**, wherein each of the first semiconductor devices and each of the second semiconductor devices includes:

a source extending vertically along the first direction,

a drain extending vertically along the first direction and spaced apart from the source along the second direction,

an inner spacer disposed between the source and the drain,

a channel layer stacked over the inner spacer, the source, and the drain along the third direction, and

a memory layer stacked over the channel layer along the third direction.

9. The semiconductor die of claim **8**, wherein:

each of the first semiconductor devices includes a first gate layer stacked over the memory layer and extending along the second direction, the first gate layer including a first semiconductor material having the first workfunction, and

each of the second semiconductor devices includes a second gate layer stacked over the memory layer and extending along the second direction, the second gate layer including a second semiconductor material having the second workfunction.

10. The semiconductor die of claim **9**, wherein the first semiconductor material includes a n-type semiconductor material and the second semiconductor material includes a p-type semiconductor material.

11. A semiconductor die, comprising:

first semiconductor devices arranged in a first three-dimensional (3D) set, the first semiconductor devices each having a first workfunction;

second semiconductor devices arranged in a second 3D set that is disposed laterally adjacent to the first 3D set, the second semiconductor devices each having a second workfunction that is greater than the first workfunction; and

an isolation layer extending along a vertical direction and electrically isolating the first 3D set from the second 3D set.

12. The semiconductor die of claim **11**, wherein:

the first 3D set is adjacent to the second 3D set along a first lateral direction, and

the isolation layer extends along a second lateral direction perpendicular to the first lateral direction.

13. The semiconductor die of claim **11**, wherein the isolation layer includes a first portion that extends along a first lateral direction and a second portion that extends along a second lateral direction perpendicular to the first lateral direction.

14. The semiconductor die of claim **11**, wherein the first 3D set and the second 3D set are arranged in a first alternate pattern along a first lateral direction and a second lateral pattern along a second lateral direction perpendicular to the first lateral direction.

15. The semiconductor die of claim **11**, wherein each of the first semiconductor devices and each of the second semiconductor devices includes:

a source extending along the vertical direction,

a drain extending along the vertical direction and spaced apart from the source along a first lateral direction,

an inner spacer disposed between the source and the drain,

a channel layer disposed radially outwards of an outer surface of the inner spacer along a second lateral direction perpendicular to the first lateral direction, and

a memory layer disposed radially outwards of an outer surface of the channel layer along the second lateral direction.

16. The semiconductor die of claim **15**, wherein:

each of the first semiconductor devices includes a first gate layer disposed radially outwards of an outer surface of the memory layer along the second lateral direction, the first gate layer extending along the first lateral direction and including a first semiconductor material having the first workfunction, and

each of the second semiconductor devices includes a second gate layer disposed radially outwards of the outer surface of the memory layer along the second lateral direction, the second gate layer extending along the first lateral direction and including a second semiconductor material having the second workfunction.

17. A semiconductor die, comprising:

a first location including a first three-dimensional (3D) set of first semiconductor devices stacked vertically along a first direction, the first semiconductor devices each having a first workfunction;

a second location including a second 3D set of second semiconductor devices stacked vertically along the first direction, the second semiconductor devices each having a second workfunction that is greater than the first workfunction; and

an isolation layer extending vertically along the first direction and laterally along a second direction perpendicular to the first direction, the isolation layer separating the first location from the second location.

18. The semiconductor die of claim **17**, wherein:

the first location includes a first array of a plurality of the first 3D sets spaced apart along the second direction and a third direction perpendicular to the first direction and the second direction, and

the second location includes a second array of a plurality of the second 3D sets spaced apart along the second direction and the third direction.

19. The semiconductor die of claim **18**, wherein:

the isolation layer is a first isolation layer, and

the semiconductor die further comprises:

a second isolation layer separating two adjacent first 3D sets in the first array; and

a third isolation layer separating two adjacent second 3D sets in the second array.

20. The semiconductor die of claim **19**, wherein each of the second isolation layer and the third isolation layer includes a first portion that extends along the second direction and a second portion that extends along the third direction.

* * * * *