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SEMICONDUCTOR DEVICE

Abstract

A semiconductor device that can be miniaturized or highly integrated can be provided. In the semiconductor device, a first interlayer film having a first opening portion and a second interlayer film having a second opening portion are stacked. Parts of structures of two or more trench capacitors are provided in the first opening portion. Parts of structures of two or more vertical transistors are provided are the second opening portion. The second opening portion includes a region overlapping with the first opening portion. The upper electrode of the first vertical transistor and the upper electrode of the second vertical transistor each include a cutout portion at a position overlapping with the second opening portion. In a plan view, the outline of the cutout portion matches or roughly matches with part of the outline of the second opening.

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Background/Summary

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] One embodiment of the present invention relates to a semiconductor device, a memory device, and an electronic apparatus. One embodiment of the present invention also relates to a method for manufacturing the semiconductor device.

[0002] Note that one embodiment of the present invention is not limited to the above technical field. Examples of the technical field of one embodiment of the present invention include a semiconductor device, a display apparatus, a light-emitting apparatus, a power storage device, a memory device, an electronic apparatus, a lighting device, an input device (e.g., a touch sensor), an input/output device (e.g., a touch panel), a method for driving any of them, and a method for manufacturing any of them.

[0003] In this specification and the like, a semiconductor device means a device that utilizes semiconductor characteristics, and refers to a circuit including a semiconductor element (e.g., a transistor, a diode, or a photodiode), a device including the circuit, and the like. The semiconductor device also means devices that can function by utilizing semiconductor characteristics. For example, an integrated circuit, a chip including an integrated circuit, and an electronic component including a chip in a package are examples of the semiconductor device. In some cases, a memory device, a display device, a light-emitting apparatus, a lighting device, and an electronic apparatus themselves are semiconductor devices and also include a semiconductor device.

2. Description of the Related Art

[0004] In recent years, semiconductor devices have been developed, and large scale integrations (LSIs), central processing unit (CPUs), memories (memory devices), and the like are mainly used in semiconductor devices. A CPU is an aggregation of semiconductor elements; the CPU includes a semiconductor integrated circuit (including a transistor and a memory) formed into a chip by processing a semiconductor wafer, and is provided with an electrode that is a connection terminal.

[0005] An integrated circuit (IC) of an LSI, a CPU, a memory, or the like is mounted on a circuit board, for example, a printed wiring board, to be used as one of components of a variety of electronic apparatuses.

[0006] A technique by which a transistor is formed using a semiconductor thin film formed over a substrate having an insulating surface has been attracting attention. The transistor is used in a wide range of electronic devices such as an integrated circuit (IC) and a display device. As semiconductor materials usable for the transistor, silicon-based semiconductor materials have been widely used, but oxide semiconductors have been attracting attention as alternative materials.

[0007] A transistor using an oxide semiconductor is known to have an extremely low leakage current in an off state. For example, Patent Document 1 discloses a low-power CPU utilizing a characteristic of a low leakage current of the transistor including an oxide semiconductor. For example, Patent Document 2 discloses a memory device and the like that can retain stored data for a long time by utilizing a characteristic of a low leakage current of the transistor including an oxide semiconductor.

[0008] In recent years, demand for an integrated circuit with higher density has risen with reductions in size and weight of electronic apparatuses. In addition, the productivity of a semiconductor device including an integrated circuit is desired to be improved. For example, Patent Document 3 and Non-Patent Document 1 disclose a technique to achieve an integrated circuit with higher density by making a plurality of memory cells overlap with each other by stacking a first

transistor including an oxide semiconductor film and a second transistor including an oxide semiconductor film. Patent Document 4 discloses a technique for achieving an integrated circuit with higher density by forming a channel of a transistor including an oxide semiconductor film in the vertical direction.

REFERENCE

[0009] [Patent Document 1] Japanese Published Patent Application No. 2012-257187 [0010] [Patent Document 2] Japanese Published Patent Application No. 2011-151383 [0011] [Patent Document 3] PCT International Publication No. 2021/053473 [0012] [Patent Document 4] Japanese Published Patent Application No. 2013-211537 [0013] [Non-Patent Document 1]M. Oota, et al., “3D-Stacked CAAC-In—Ga—Zn Oxide FETs with Gate Length of 72 nm”, IEDM Tech. Dig., 2019, pp. 50-53

SUMMARY OF THE INVENTION

[0014] An object of one embodiment of the present invention is to provide a transistor, a semiconductor device, or a memory device that can be miniaturized or highly integrated. An object of one embodiment of the present invention is to provide a highly reliable transistor, a highly reliable semiconductor device, or a highly reliable memory device. An object of one embodiment of the present invention is to provide a semiconductor device or a memory device having low power consumption. An object of one embodiment of the present invention is to provide a semiconductor device or a memory device having high operation speed. An object of one embodiment of the present invention is to provide a semiconductor device or a memory device including a transistor with favorable electrical characteristics. An object of one embodiment of the present invention is to provide a semiconductor device or a memory device including a transistor with high on-state current. An object of one embodiment of the present invention is to provide a semiconductor device or a memory device including a transistor with low parasitic capacitance. An object of one embodiment of the present invention is to provide a method for manufacturing the above-described transistor, semiconductor device, or memory device.

[0015] Note that the description of these objects does not preclude the presence of other objects. One embodiment of the present invention does not necessarily achieve all of these objects. Other objects can be derived from the description of the specification, the drawings, and the claims.

[0016] One embodiment of the present invention is a semiconductor device including a first insulating layer, a second insulating layer, a first capacitor, a second capacitor, a first transistor, and a second transistor. The first insulating layer includes a first opening portion. The second insulating layer includes a second opening portion. The second insulating layer is positioned over the first insulating layer. The second opening portion includes a region overlapping with the first opening portion. The first capacitor includes a first electrode provided along a sidewall of the first opening portion, a dielectric provided to cover the first electrode, and a second electrode including a region facing the first electrode with the dielectric interposed therebetween in the first opening portion. The second capacitor includes the first electrode, the dielectric, and a third electrode including a region facing the first electrode with the dielectric interposed therebetween in the first opening portion. The first transistor includes a first oxide semiconductor layer. The second transistor includes a second oxide semiconductor layer. The first oxide semiconductor layer and the second oxide semiconductor layer each include a region provided along a sidewall of the second opening portion.

[0017] Another embodiment of the present invention is a semiconductor device including a first capacitor, a second capacitor, a first transistor, a second transistor, a first insulating layer, a second insulating layer, a third insulating layer, and a fourth insulating layer. The first capacitor includes a first conductive layer, a second conductive layer, and a fifth insulating layer. The second capacitor includes the first conductive layer, a third conductive layer, and the fifth insulating layer. The first transistor includes a first oxide semiconductor layer, a fourth conductive layer, a fifth conductive layer, a sixth conductive layer, and a sixth insulating layer. The second transistor includes a second

oxide semiconductor layer, the fifth conductive layer, a seventh conductive layer, an eighth conductive layer, and the sixth insulating layer. The first insulating layer includes a first opening portion. The first conductive layer includes a region positioned in the first opening portion. The fifth insulating layer is positioned over the first conductive layer. The second conductive layer and the third conductive layer each include a region facing the first conductive layer with the fifth insulating layer interposed therebetween in the first opening portion. The second insulating layer is positioned over the second conductive layer and the third conductive layer. The fourth conductive layer and the seventh conductive layer are positioned over the second insulating layer. The fourth conductive layer is electrically connected to the second conductive layer. The seventh conductive layer is electrically connected to the third conductive layer. The third insulating layer is positioned over the fourth conductive layer and the seventh conductive layer. The fifth conductive layer is positioned over the third insulating layer. The fourth insulating layer is positioned over the third insulating layer and the fifth conductive layer. The sixth conductive layer and the eighth conductive layer are provided to be apart from each other over the fourth insulating layer. The fourth insulating layer, the fifth conductive layer, and the third insulating layer include a second opening portion. The second opening portion includes a portion overlapping with the fourth conductive layer, a portion overlapping with the seventh conductive layer, and a portion overlapping with the second insulating layer positioned between the fourth conductive layer and the seventh conductive layer. The sixth insulating layer covers a sidewall of the second opening portion. The first oxide semiconductor layer includes a region facing the fifth conductive layer with the sixth insulating layer interposed therebetween in the second opening portion, a region in contact with the fourth conductive layer in the second opening portion, and a region in contact with the sixth conductive layer outside the second opening portion. The second oxide semiconductor layer includes a region facing the fifth conductive layer with the sixth insulating layer interposed therebetween in the second opening portion, a region in contact with the seventh conductive layer in the second opening portion, and a region in contact with the eighth conductive layer outside the second opening portion.

[0018] In the above embodiment, the first conductive layer may include a region along a sidewall of the first opening portion.

[0019] The semiconductor device in the above embodiment may include a ninth conductive layer and a tenth conductive layer. The second insulating layer may include a third opening portion reaching the second conductive layer and a fourth opening portion reaching the third conductive layer. The ninth conductive layer may be positioned in the third opening portion. The tenth conductive layer may be positioned in the fourth opening portion. The fourth conductive layer may include a region in contact with a top surface of the ninth conductive layer. The seventh conductive layer may include a region in contact with a top surface of the tenth conductive layer.

[0020] The semiconductor device in the above embodiment may include a seventh insulating layer. The second insulating layer may include a first depressed portion at a position overlapping with the first opening portion, and the seventh insulating layer may be provided to fill at least a part of the first depressed portion.

[0021] In the above embodiment, the sixth insulating layer in the second opening portion may be circular in a plan view, and the first oxide semiconductor layer and the second oxide semiconductor layer in the second opening portion may be each arc-shaped in the plan view.

[0022] In the above embodiment, the fourth conductive layer may include a second depressed portion at a position overlapping with the second opening portion. The sixth insulating layer may be in contact with a sidewall of the second depressed portion, and the first oxide semiconductor layer may be in contact with at least a part of a bottom portion of the second depressed portion.

[0023] In the above embodiment, the fourth conductive layer may include a first layer and a second layer over the first layer, and the second layer may include the second depressed portion.

[0024] In the above embodiment, the sixth insulating layer may be in contact with a part of a side

surface of the sixth conductive layer on the second opening portion side, and the first oxide semiconductor layer may be in contact with another part of the side surface of the sixth conductive layer on the second opening portion side.
[0025] In the above embodiment, the sixth insulating layer may be in contact with part of the side surface of the fourth conductive layer on the second opening portion side, and the first oxide semiconductor layer may be in contact with another part of the side surface of the fourth conductive layer on the second opening portion side.
[0026] In the above embodiment, an end portion of the first oxide semiconductor layer outside the second opening portion may be positioned closer to the second opening portion than an end portion of the sixth conductive layer outside the second opening portion is.
[0027] The semiconductor device in the above embodiment may include an eighth insulating layer and an eleventh conductive layer. The eighth insulating layer may be positioned over the first oxide semiconductor layer and the second oxide semiconductor layer. The eleventh conductive layer may include, in the second opening portion, a region facing the fifth conductive layer with the eighth insulating layer, the first oxide semiconductor layer, and the sixth insulating layer interposed therebetween and a region facing the fifth conductive layer with the eighth insulating layer, the second oxide semiconductor layer, and the sixth insulating layer interposed therebetween.
[0028] In the above embodiment, a height of a bottom surface of the eleventh conductive layer in a portion positioned between the fourth conductive layer and the seventh conductive layer may be lower than a height of a top surface of the fourth conductive layer in a portion not overlapping with the second opening portion.
[0029] The semiconductor device in the above embodiment may include a ninth insulating layer and a twelfth conductive layer. The ninth insulating layer may be positioned over the eighth insulating layer and include a fifth opening portion at a position overlapping with the second opening portion. The twelfth conductive layer may be provided over the ninth insulating layer and include a region in contact with the eleventh conductive layer.
[0030] According to one embodiment of the present invention, a transistor, a semiconductor device, or a memory device that can be miniaturized or highly integrated can be provided. According to one embodiment of the present invention, a highly reliable transistor, a highly reliable semiconductor device, or a highly reliable memory device can be provided. According to one embodiment of the present invention, a semiconductor device or a memory device having low power consumption can be provided. According to one embodiment of the present invention, a semiconductor device or a memory device having high operation speed can be provided. According to one embodiment of the present invention, a semiconductor device or a memory device including a transistor with favorable electrical characteristics can be provided. According to one embodiment of the present invention, a semiconductor device or a memory device including a transistor with high on-state current can be provided. According to one embodiment of the present invention, a semiconductor device or a memory device including a transistor with low parasitic capacitance can be provided. According to one embodiment of the present invention, a method for manufacturing the above-described transistor, semiconductor device, or memory device can be provided.
[0031] Note that the description of these effects does not preclude the presence of other effects. One embodiment of the present invention does not necessarily have all of these effects. Other effects can be derived from the description of the specification, the drawings, and the claims.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0032] In the accompanying drawings:
[0033] FIGS. **1**A to **1**D are plan views illustrating examples of a semiconductor device;

[0034] FIGS. **2**A and **2**B are cross-sectional views illustrating an example of a semiconductor device, FIG. **2**C is a perspective view illustrating an example of the semiconductor device, FIG. **2**D is a plan view illustrating an example of the semiconductor device, and FIG. **2**E is a circuit diagram illustrating an example of a memory cell;
[0035] FIG. **3**A is a cross-sectional view illustrating an example of a semiconductor device, and FIG. **3**B is a plan view illustrating an example of the semiconductor device;
[0036] FIGS. **4**A and **4**B are cross-sectional views illustrating examples of a semiconductor device;
[0037] FIGS. **5**A and **5**B are cross-sectional views illustrating examples of a semiconductor device;
[0038] FIGS. **6**A and **6**B are cross-sectional views illustrating examples of a semiconductor device;
[0039] FIGS. **7**A and **7**B are cross-sectional views illustrating examples of a semiconductor device;
[0040] FIG. **8** is a cross-sectional view illustrating an example of a semiconductor device;
[0041] FIGS. **9**A and **9**B are cross-sectional views illustrating examples of a semiconductor device;
[0042] FIGS. **10**A and **10**B are cross-sectional views illustrating examples of a semiconductor device;
[0043] FIGS. **11**A and **11**B are cross-sectional views illustrating examples of a semiconductor device;
[0044] FIGS. **12**A and **12**B are cross-sectional views illustrating examples of a semiconductor device;
[0045] FIGS. **13**A and **13**B are cross-sectional views illustrating examples of a semiconductor device;
[0046] FIGS. **14**A and **14**B are cross-sectional views illustrating examples of a semiconductor device;
[0047] FIG. **15**A is a cross-sectional view illustrating an example of a semiconductor device, and FIGS. **15**B and **15**C are plan views illustrating examples of the semiconductor device;
[0048] FIG. **16**A is a plan view illustrating an example of a semiconductor device, and FIGS. **16**B and **16**C are cross-sectional views illustrating examples of the semiconductor device;
[0049] FIG. **17**A is a plan view illustrating an example of a semiconductor device, and FIGS. **17**B and **17**C are cross-sectional views illustrating examples of the semiconductor device;
[0050] FIGS. **18**A and **18**D are plan views illustrating examples of a semiconductor device, and FIGS. **18**B and **18**C are cross-sectional views illustrating examples of the semiconductor device;
[0051] FIGS. **19**A and **19**D are plan views illustrating examples of a semiconductor device, and FIGS. **19**B and **19**C are cross-sectional views illustrating examples of the semiconductor device;
[0052] FIG. **20**A is a plan view illustrating an example of a method for manufacturing a semiconductor device, and FIGS. **20**B and **20**C are cross-sectional views illustrating examples of the method for manufacturing the semiconductor device;
[0053] FIG. **21**A is a plan view illustrating an example of the method for manufacturing the semiconductor device, and FIGS. **21**B and **21**C are cross-sectional views illustrating examples of the method for manufacturing the semiconductor device;
[0054] FIG. **22**A is a plan view illustrating an example of the method for manufacturing the semiconductor device, and FIGS. **22**B and **22**C are cross-sectional views illustrating examples of the method for manufacturing the semiconductor device;
[0055] FIG. **23**A is a plan view illustrating an example of the method for manufacturing the semiconductor device, and FIGS. **23**B and **23**C are cross-sectional views illustrating examples of the method for manufacturing the semiconductor device;
[0056] FIG. **24**A is a plan view illustrating an example of the method for manufacturing the semiconductor device, and FIGS. **24**B and **24**C are cross-sectional views illustrating examples of the method for manufacturing the semiconductor device;
[0057] FIG. **25**A is a plan view illustrating an example of the method for manufacturing the semiconductor device, and FIGS. **25**B and **25**C are cross-sectional views illustrating examples of the method for manufacturing the semiconductor device;

[0058] FIG. **26**A is a plan view illustrating an example of the method for manufacturing the semiconductor device, and FIGS. **26**B and **26**C are cross-sectional views illustrating examples of the method for manufacturing the semiconductor device;
[0059] FIG. **27**A is a plan view illustrating an example of the method for manufacturing the semiconductor device, and FIGS. **27**B and **27**C are cross-sectional views illustrating examples of the method for manufacturing the semiconductor device;
[0060] FIG. **28**A is a plan view illustrating an example of the method for manufacturing the semiconductor device, and FIGS. **28**B and **28**C are cross-sectional views illustrating examples of the method for manufacturing the semiconductor device;
[0061] FIG. **29**A is a plan view illustrating an example of the method for manufacturing the semiconductor device, and FIGS. **29**B and **29**C are cross-sectional views illustrating examples of the method for manufacturing the semiconductor device;
[0062] FIG. **30**A is a plan view illustrating an example of the method for manufacturing the semiconductor device, and FIGS. **30**B and **30**C are cross-sectional views illustrating examples of the method for manufacturing the semiconductor device;
[0063] FIG. **31**A is a plan view illustrating an example of the method for manufacturing the semiconductor device, and FIGS. **31**B and **31**C are cross-sectional views illustrating examples of the method for manufacturing the semiconductor device;
[0064] FIG. **32**A is a plan view illustrating an example of the method for manufacturing the semiconductor device, and FIGS. **32**B and **32**C are cross-sectional views illustrating examples of the method for manufacturing the semiconductor device;
[0065] FIG. **33**A is a plan view illustrating an example of the method for manufacturing the semiconductor device, and FIGS. **33**B and **33**C are cross-sectional views illustrating examples of the method for manufacturing the semiconductor device;
[0066] FIG. **34**A is a plan view illustrating an example of the method for manufacturing the semiconductor device, and FIGS. **34**B and **34**C are cross-sectional views illustrating examples of the method for manufacturing the semiconductor device;
[0067] FIG. **35**A is a plan view illustrating an example of the method for manufacturing the semiconductor device, and FIGS. **35**B and **35**C are cross-sectional views illustrating examples of the method for manufacturing the semiconductor device;
[0068] FIG. **36**A is a plan view illustrating an example of the method for manufacturing the semiconductor device, and FIGS. **36**B and **36**C are cross-sectional views illustrating examples of the method for manufacturing the semiconductor device;
[0069] FIG. **37**A is a plan view illustrating an example of the method for manufacturing the semiconductor device, and FIGS. **37**B and **37**C are cross-sectional views illustrating examples of the method for manufacturing the semiconductor device;
[0070] FIG. **38**A is a plan view illustrating an example of the method for manufacturing the semiconductor device, and FIGS. **38**B and **38**C are cross-sectional views illustrating examples of the method for manufacturing the semiconductor device;
[0071] FIG. **39**A is a plan view illustrating an example of the method for manufacturing the semiconductor device, and FIGS. **39**B and **39**C are cross-sectional views illustrating examples of the method for manufacturing the semiconductor device;
[0072] FIG. **40**A is a plan view illustrating an example of the method for manufacturing the semiconductor device, and FIGS. **40**B and **40**C are cross-sectional views illustrating examples of the method for manufacturing the semiconductor device;
[0073] FIG. **41**A is a plan view illustrating an example of the method for manufacturing the semiconductor device, and FIGS. **41**B and **41**C are cross-sectional views illustrating examples of the method for manufacturing the semiconductor device;
[0074] FIG. **42** is a band diagram of an oxide semiconductor layer;
[0075] FIGS. **43**A and **43**B are plan views each illustrating an example of a semiconductor device;

[0076] FIGS. **44**A and **44**B are plan views each illustrating an example of a semiconductor device;
[0077] FIG. **45** is a cross-sectional view illustrating an example of a semiconductor device;
[0078] FIG. **46** is a cross-sectional view illustrating an example of a semiconductor device;
[0079] FIG. **47** is a block diagram illustrating an example of a semiconductor device;
[0080] FIGS. **48**A to **48**D are circuit diagrams each illustrating an example of a memory cell;
[0081] FIGS. **49**A and **49**B are schematic perspective views each illustrating an example of a semiconductor device;
[0082] FIG. **50** is a block diagram illustrating a CPU;
[0083] FIGS. **51**A and **51**B are schematic diagrams illustrating an example of a semiconductor device;
[0084] FIGS. **52**A and **52**B are schematic perspective views illustrating examples of semiconductor devices;
[0085] FIG. **53** is a conceptual diagram illustrating a hierarchy of memory devices;
[0086] FIGS. **54**A and **54**B are circuit diagrams illustrating examples of semiconductor devices, and FIG. **54**C illustrates an example of an electronic component including a semiconductor device;
[0087] FIG. **55** illustrates an example of an electronic component;
[0088] FIGS. **56**A to **56**C illustrate an example of a large computer, FIG. **56**D illustrates an example of space equipment, and FIG. **56**E illustrates an example of a storage system that can be used in a data center;
[0089] FIGS. **57**A to **57**F illustrate examples of electronic apparatuses;
[0090] FIGS. **58**A to **58**G illustrate examples of electronic apparatuses; and
[0091] FIGS. **59**A to **59**F illustrate examples of electronic apparatuses.

DETAILED DESCRIPTION OF THE INVENTION

[0092] Embodiments will be described in detail with reference to the drawings. Note that the present invention is not limited to the following description, and it will be readily appreciated by those skilled in the art that modes and details of the present invention can be modified in various ways without departing from the spirit and scope of the present invention. Thus, the present invention should not be construed as being limited to the description in the following embodiments.
[0093] Note that in structures of the invention described below, the same portions or portions having similar functions are denoted by the same reference numerals in different drawings, and the description thereof is not repeated. The same hatching pattern is used for portions having similar functions, and the portions are not denoted by specific reference numerals in some cases.
[0094] For easy understanding, the position, size, range, and the like of each component illustrated in drawings do not represent the actual position, size, range, and the like in some cases. Therefore, the disclosed invention is not necessarily limited to the position, size, range, or the like disclosed in the drawings.
[0095] Note that ordinal numbers such as “first” and “second” in this specification and the like are used for convenience and do not limit the number or the order (e.g., the order of steps or the stacking order) of components. The ordinal number added to a component in a part of this specification may be different from the ordinal number added to the component in another part of this specification or the scope of claims.
[0096] A transistor is a kind of semiconductor elements and enables amplification of a current or a voltage, switching operation for controlling conduction or non-conduction, and the like. A transistor in this specification includes, in its category, an insulated-gate field effect transistor (IGFET) and a thin film transistor (TFT).
[0097] In this specification and the like, a transistor including an oxide semiconductor or a metal oxide in its semiconductor layer and a transistor including an oxide semiconductor or a metal oxide in its channel formation region are each sometimes referred to as an oxide semiconductor (OS) transistor. A transistor including silicon in its channel formation region is sometimes referred to as a Si transistor.

[0098] In this specification and the like, a transistor is an element including at least three terminals of a gate, a drain, and a source. The transistor includes a region where a channel is formed (also referred to as a channel formation region) between the drain (a drain terminal, a drain region, or a drain electrode) and the source (a source terminal, a source region, or a source electrode), and a current can flow between the source and the drain through the channel formation region. Note that in this specification and the like, a channel formation region refers to a region through which a current mainly flows.
[0099] The functions of a “source” and a “drain” are sometimes replaced with each other when a transistor of different polarity is used or when the direction of current flow is changed in circuit operation, for example. Thus, the terms “source” and “drain” can be used interchangeably in this specification.
[0100] Note that impurities in a semiconductor refer to, for example, elements other than the main components of the semiconductor. For example, an element with a concentration of lower than 0.1 atomic % is an impurity. When a semiconductor contains an impurity, an increase in density of defect states or a reduction in crystallinity of the semiconductor may occur, for example. In the case where the semiconductor is an oxide semiconductor, examples of an impurity that changes the characteristics of the semiconductor include Group 1 elements, Group 2 elements, Group 13 elements, Group 14 elements, Group 15 elements, and transition metals other than the main components of the oxide semiconductor. Specific examples include hydrogen, lithium, sodium, silicon, boron, phosphorus, carbon, and nitrogen. Note that water also serves as an impurity in some cases. Entry of an impurity may cause oxygen vacancies (also referred to as V.sub.O) in an oxide semiconductor, for example.
[0101] Note that in this specification and the like, an oxynitride refers to a material in which an oxygen content is higher than a nitrogen content. A nitride oxide refers to a material in which a nitrogen content is higher than an oxygen content.
[0102] The content of an element such as hydrogen, oxygen, carbon, or nitrogen in a film can be analyzed by secondary ion mass spectrometry (SIMS) or X-ray photoelectron spectroscopy (XPS or electron spectroscopy for chemical analysis (ESCA)), for example. XPS is suitable when the content of a target element is high (e.g., 0.5 atomic % or more, or 1 atomic % or more). In contrast, SIMS is suitable when the content of a target element is low (e.g., less than 0.5 atomic %, or less than 1 atomic %). To compare the contents of elements, analysis with a combination of SIMS and XPS is preferably used.
[0103] Note that in this specification and the like, the term “content percentage” refers to the proportion of a component contained in a film. In the case where an oxide semiconductor layer contains a metal element X, a metal element Y, and a metal element Z whose atomic numbers are respectively represented by A.sub.X, A.sub.Y, and A.sub.Z, the content percentage of the metal element X can be represented by A.sub.X/(A.sub.X+A.sub.Y+A.sub.Z). Moreover, in the case where the atomic ratio of the metal element X to the metal element Y to the metal element Z contained in an oxide semiconductor layer is represented by B.sub.X:B.sub.Y:B.sub.Z, the content of the metal element X can be represented by B.sub.X/(B.sub.X+B.sub.Y+B.sub.Z).
[0104] Note that the terms “film” and “layer” can be used interchangeably depending on the case or the circumstances. For example, the term “conductive layer” can be replaced with the term “conductive film”. As another example, the term “insulating film” can be replaced with the term “insulating layer”.
[0105] In this specification and the like, the term “parallel” indicates that the angle subtended between two straight lines is greater than or equal to −10° and less than or equal to 10°. Thus, the case where the angle is greater than or equal to −5° and less than or equal to 5° is also included. The term “substantially parallel” indicates that the angle subtended between two straight lines is greater than or equal to −20° and less than or equal to 20°. The term “perpendicular” indicates that the angle subtended between two straight lines is greater than or equal to 80° and less than or equal

to 100°. Thus, the case where the angle is greater than or equal to 850 and less than or equal to 950 is also included. In addition, the term “substantially perpendicular” indicates that the angle subtended between two straight lines is greater than or equal to 700 and less than or equal to 110°.
[0106] The expression “connection” in this specification includes “electrical connection”, for example. Note that the expression “electrical connection” is used in some cases to specify the connection relation of a circuit element as an object. The term “electrical connection” includes “direct connection” and “indirect connection”. The expression “A and B are directly connected” means that A and B are connected to each other without a circuit element such as a transistor or a switch (note that a wiring is not a circuit element) therebetween, for example. By contrast, the expression “A and B are indirectly connected” means that A and B are connected to each other with at least one circuit element therebetween.
[0107] For example, assuming that a circuit including A and B is in operation, the circuit can be specified as “A and B are indirectly connected” as an object when electric signal transmission and reception or electric potential interaction between A and B occurs at some point during the operation period of the circuit. Note that even when neither electric signal transmission and reception nor electric potential interaction between A and B occurs at some point during the operation of the circuit, the circuit can be specified as “A and B are indirectly connected” as long as electric signal transmission and reception or electric potential interaction between A and B occurs at another point during the operation period of the circuit.
[0108] Examples of the case where the expression “A and B are indirectly connected” can be used include the case where A and B are connected to each other through a source and a drain of at least one transistor. By contrast, examples of the case where the expression “A and B are indirectly connected” cannot be used include the case where an insulator is present on the path from A to B. Specific examples thereof include the case where a capacitor is connected between A and B and the case where a gate insulating film or the like of a transistor is present between A and B. In such cases, the expression “a gate (A) of a transistor and a source or a drain (B) of the transistor are indirectly connected” cannot be used.
[0109] Another example of the case where the expression “A and B are indirectly connected” cannot be used is the case where a plurality of transistors are connected through their sources and drains on the path from A to B and a constant electric potential V is supplied from a power source, GND, or the like to a node between one of the transistors and another one of the transistors.
[0110] Unless otherwise specified, an off-state current in this specification and the like refers to a leakage current generated between a source and a drain when a transistor is in an off state (also referred to as a non-conducting state or a cutoff state). Unless otherwise specified, the off state of an n-channel transistor means that a gate-source voltage V.sub.gs is lower than a threshold voltage V.sub.th (the off state of a p-channel transistor means that V.sub.gs is higher than V.sub.th).
[0111] Note that “normally-on characteristics” in this specification and the like means a state where a channel is formed and a current flows through a transistor even when no voltage is applied to a gate. Furthermore, “normally-off characteristics” means a state where a current does not flow through a transistor when no potential or a ground potential is applied to a gate.
[0112] Note that in this specification and the like, a tapered shape refers to a shape such that at least part of a side surface of a component is inclined with respect to a substrate surface or a formation surface of the component. For example, a tapered shape preferably includes a region where the angle subtended between the inclined side surface and the substrate surface or the formation surface (such an angle is also referred to as a taper angle) is greater than 0° and less than 90°. Note that the side surface of the component, the substrate surface, and the formation surface are not necessarily completely flat and may be substantially planar shape with a slight curvature or with slight unevenness.
[0113] In this specification and the like, when the expression “A is positioned over B” is used, at least part of A is positioned over B. In other words, A includes a region positioned over B, for

example. Similarly, when the expression “A is in contact with B” or “A overlaps with B” is used, at least part of A is in contact with or overlaps with B. This can be rephrased as that A includes a region in contact with B or A includes a region overlapping with B, for example. Similarly, in this specification and the like, when the expression “A covers B” is used, at least part of A covers B. This can be rephrased as that A includes a region covering B, for example.

[0114] In this specification and the like, disconnection refers to a phenomenon in which a layer, a film, or an electrode is split because of the shape of the formation surface (e.g., a level difference).

[0115] In the drawings for this specification and the like, arrows indicating an X direction, a Y direction, and a Z direction are illustrated in some cases. In this specification and the like, the “X direction” is a direction along the X axis, and unless otherwise specified, the forward direction and the reverse direction are not distinguished in some cases. The same applies to the “Y direction” and the “Z direction”. The X direction, the Y direction, and the Z direction are directions intersecting with each other. For example, the X direction, the Y direction, and the Z direction are directions orthogonal to each other.

Embodiment 1

[0116] In this embodiment, a semiconductor device of one embodiment of the present invention and a method for manufacturing the semiconductor device will be described with reference to drawings.

[0117] One embodiment of the present invention relates to a semiconductor device including a trench capacitor and a vertical transistor. The semiconductor device of one embodiment of the present invention can include a memory cell including a trench capacitor and a vertical transistor. Therefore, the semiconductor device of one embodiment of the present invention can be a memory device.

[0118] In this specification and the like, a vertical transistor refers to a transistor in which a source electrode and a drain electrode are provided at different levels. For example, a transistor in which the bottom surface of the source electrode and the bottom surface of the drain electrode are provided at different levels can be referred to as a vertical transistor. Here, of the source electrode and the drain electrode, an electrode at a lower level from a reference surface is referred to as a lower electrode, and an electrode at a higher level from the reference surface is referred to as an upper electrode. The reference surface can be, for example, the top surface of a substrate or the top surface of a base insulating layer. An interlayer film is provided between the lower electrode and the upper electrode.

[0119] In this specification and the like, a trench capacitor refers to a capacitor in which at least parts of a pair of electrodes and a dielectric are positioned in an opening portion formed in an interlayer film, and at least one of the pair of electrodes is provided along the sidewall of the opening portion.

[0120] The semiconductor device of one embodiment of the present invention includes a first interlayer film and a second interlayer film over the first interlayer film. The first interlayer film includes a first opening portion, and the second interlayer film includes a second opening portion. Parts of structures of two or more trench capacitors are provided in the first opening portion. For example, at least parts of the lower electrode, the upper electrode, and the dielectric of the first capacitor and at least parts of the lower electrode, the upper electrode, and the dielectric of the second capacitor can be provided in the first opening portion.

[0121] Parts of structures of two or more vertical transistors are provided in the second opening portion. Specifically, at least part of a semiconductor layer of the first vertical transistor and at least part of a semiconductor layer of the second vertical transistor are provided in the second opening portion. Thus, a channel formation region of the first vertical transistor and a channel formation region of the second vertical transistor are provided in the second opening portion.

[0122] The second opening portion includes a region overlapping with the first opening portion. Thus, the first vertical transistor is provided to include a region overlapping with a first trench

capacitor. The second vertical transistor is provided to include a region overlapping with a second trench capacitor.

[0123] Therefore, a semiconductor device with a small occupation area of each memory cell can be provided according to one embodiment of the present invention. Accordingly, a semiconductor device that can be miniaturized or highly integrated can be provided.

Structure Example 1 of Semiconductor Device

[0124] FIG. **1**A is a plan view illustrating an example of a semiconductor device of one embodiment of the present invention. The semiconductor device illustrated in FIG. **1**A includes a capacitor **100***a*, a capacitor **100***b*, a transistor **200***a*, and a transistor **200***b*. That is, the semiconductor device illustrated in FIG. **1**A includes two capacitors and two transistors.

[0125] FIG. **1**B is a plan view illustrating an example of the capacitor **100***a* and the capacitor **100***b*. FIG. **1**C is a plan view illustrating an example of the transistor **200***a* and the transistor **200***b*. FIGS. **1**B and **1**C are diagrams in which some components illustrated in FIG. **1**A are omitted. FIG. **1**D is a diagram in which some components illustrated in FIG. **1**C are omitted. For the sake of clarity of the drawings, some components, e.g., an insulating layer, are not illustrated in the plan views in FIGS. **1**A and **1**D. Some components may be omitted also in plan views mentioned below.

[0126] FIG. **2**A is a cross-sectional view taken along a dashed-dotted line A**1**-A**2** in FIG. **1**A, for example. FIG. **2**B is a cross-sectional view taken along a dashed-dotted line A**3**-A**4** in FIG. **1**A, for example. FIG. **2**C is a schematic perspective view illustrating the semiconductor device illustrated in FIGS. **1**A to **1**D and FIGS. **2**A and **2**B. Specifically, FIG. **2**C is a schematic perspective view of the semiconductor device sectioned along a dashed-dotted line B**1**-B**2** in FIG. **1**A, for example, where the capacitor **100***a* and the transistor **200***a* are illustrated. Some components are omitted in FIG. **2**C. FIG. **2**D is a cross-sectional view taken along a dashed-dotted line A**5**-A**6** in FIG. **2**A. FIG. **2**D is also referred to as a plan view.

[0127] In FIGS. **1**A to **1**D and FIGS. **2**A to **2**D, the X direction, the Y direction, and the Z direction are indicated by arrows. The directions denoted by X, Y, and Z are consistent in FIGS. **1**A to **1**D and FIGS. **2**A to **2**D but may be inconsistent among the drawings. The same applies to plan views and cross-sectional views mentioned below.

[0128] FIG. **2**E is a circuit diagram of the semiconductor device illustrated in FIG. **1**A and FIG. **2**A. The semiconductor device of one embodiment of the present invention includes a memory cell **150***a* and a memory cell **150***b* as illustrated in FIG. **1**A and FIGS. **2**A and **2**E. The memory cell **150***a* includes the capacitor **100***a* and the transistor **200***a*. The memory cell **150***b* includes the capacitor **100***b* and the transistor **200***b*. In other words, the structure illustrated in FIG. **1**A and FIG. **2**A functions as two memory cells.

[0129] FIG. **3**A is an enlarged view of a region including the transistor **200***a* and the transistor **200***b* illustrated in FIG. **2**A. FIG. **3**B is an enlarged view of FIG. **2**D. FIG. **4**A is an enlarged view of the capacitor **100***a* and the capacitor **100***b* illustrated in FIG. **2**A.

[0130] One of the source and the drain of the transistor **200***a* is connected to one of a pair of electrodes of the capacitor **100***a*. The other of the source and the drain of the transistor **200***a* is connected to a wiring BILa. A first gate of the transistor **200***a* is connected to a wiring WOL. A second gate of the transistor **200***a* is electrically connected to a wiring BGL. The other of the pair of electrodes of the capacitor **100***a* is connected to a wiring CAL.

[0131] One of the source and the drain of the transistor **200***b* is connected to one of a pair of electrodes of the capacitor **100***b*. The other of the source and the drain of the transistor **200***b* is connected to a wiring BILb. A first gate of the transistor **200***b* is connected to the wiring WOL. A second gate of the transistor **200***b* is electrically connected to the wiring BGL. The other of the pair of electrodes of the capacitor **100***b* is connected to the wiring CAL.

[0132] The semiconductor device illustrated in FIGS. **1**A to **1**D and FIGS. **2**A to **2**D includes an insulating layer **180** over a substrate (not illustrated); a conductive layer **110** and an insulating layer **111** over the insulating layer **180**; a memory cell **150***a* and a memory cell **150***b* over the conductive

layer **110**; an insulating layer **160** over the conductive layer **110** and the insulating layer **111**; an insulating layer **185** over the insulating layer **160**; an insulating layer **186** over the insulating layer **185**; an insulating layer **280** over the insulating layer **185** and the insulating layer **186**; and an insulating layer **281** over the insulating layer **280**. The insulating layers **180**, **111**, **160**, **185**, **186**, **280**, and **281** function as interlayer films. The conductive layer **110** functions as the wiring CAL. Hereinafter, the memory cell **150***a* and the memory cell **150***b* are collectively referred to as a memory cell **150** in some cases. The capacitor **100***a* and the capacitor **100***b* are collectively referred to as a capacitor **100** in some cases. Moreover, the transistor **200***a* and the transistor **200***b* are collectively referred to as a transistor **200** in some cases.

[0133] The memory cell **150***a* includes the capacitor **100***a* over the conductive layer **110** and the transistor **200***a* over the capacitor **100***a*. Similarly, the memory cell **150***b* includes the capacitor **100***b* over the conductive layer **110** and the transistor **200***b* over the capacitor **100***b*.

[0134] The capacitor **100***a* includes a conductive layer **115** over the conductive layer **110**, an insulating layer **121** over the conductive layer **115**, and a conductive layer **120***a* over the insulating layer **121**. Similarly, the capacitor **100***b* includes the conductive layer **115** over the conductive layer **110**, the insulating layer **121** over the conductive layer **115**, and a conductive layer **120***b* over the insulating layer **121**.

[0135] In the capacitor **100***a* and the capacitor **100***b*, the conductive layer **120***a* and the conductive layer **120***b* each function as one of a pair of electrodes (sometimes referred to as an upper electrode). In the capacitor **100***a* and the capacitor **100***b*, the conductive layer **115** functions as the other of the pair of electrodes (sometimes referred to as a lower electrode). Furthermore, in the capacitor **100***a* and the capacitor **100***b*, the insulating layer **121** functions as a dielectric. From the above, the capacitor **100** is a metal-insulator-metal (MIM) capacitor.

[0136] As illustrated in FIGS. **2**A and **2**B, an opening portion **190** reaching the conductive layer **110** is provided in the insulating layer **160**. At least part of the conductive layer **115** is placed in the opening portion **190**. The conductive layer **115** includes a region in contact with the top surface of the conductive layer **110** in the opening portion **190** and a region in contact with the side surface of the insulating layer **160** in the opening portion **190**. At least parts of the insulating layer **121**, the conductive layer **120***a*, and the conductive layer **120***b* are provided in the opening portion **190**.

[0137] The insulating layer **121** is provided to cover the conductive layer **115** in the opening portion **190**. The insulating layer **121** can include a region positioned in the opening portion **190** and a region positioned over the insulating layer **160**.

[0138] The conductive layer **120***a* and the conductive layer **120***b* each include a region facing the conductive layer **115** with the insulating layer **121** therebetween in the opening portion **190**. Thus, in the capacitor **100***a* and the capacitor **100***b*, the upper electrode and the lower electrode face each other with the dielectric therebetween on the sidewall of the opening portion **190** as well as on the bottom portion of the opening portion **190** in the opening portion **190**. Thus, the capacitance per unit area can be higher than that of the case where the capacitor **100***a* and the capacitor **100***b* are planar capacitors, for example. As the depth of the opening portion **190** becomes larger, the capacitances of the capacitor **100***a* and the capacitor **100***b* can be increased. Increasing the capacitances per unit area of the capacitor **100***a* and the capacitor **100***b* in this manner allows stable reading operation of the semiconductor device. This also allows further miniaturization or high integration of the semiconductor device.

[0139] As illustrated in FIGS. **1**A and **1**B, the opening portion **190** preferably has a circular shape in the plan view. When the opening portion has a circular shape in the plan view, the processing accuracy in forming the opening portion can be increased, and thus the opening portion can be formed to have minute sizes. Note that in this specification and the like, the circular shape is not limited to a perfect circular shape.

[0140] FIGS. **2**A and **2**B illustrate an example where the sidewall of the opening portion **190** is perpendicular to the top surface of the conductive layer **110**. In this case, the opening portion **190**

has a cylindrical shape. This structure enables miniaturization or high integration of the semiconductor device.

[0141] The conductive layer **115**, the insulating layer **121**, and the conductive layers **120***a* and **120***b* are stacked along the sidewall of the opening portion **190** and the top surface of the conductive layer **110**. The capacitor **100** having such a structure may be referred to as a trench-type capacitor or a trench capacitor.

[0142] For example, FIG. **2**A illustrates an example in which the conductive layer **120***a* and the conductive layer **120***b* are provided along the top surface and the side surface of the insulating layer **121** in the opening portion **190**. In this case, part of the end portion of the conductive layer **120***a* and part of the end portion of the conductive layer **120***b* can be positioned in the opening portion **190**.

[0143] FIGS. **2**A to **2**C illustrate an example in which the insulating layer **121** is patterned. Thus, the insulating layer **160**, the insulating layer **185**, the insulating layer **186**, and the like include a region not overlapping with the insulating layer **121**. Thus, for example, in the case where an opening portion reaching the conductive layer **110** is provided in the insulating layers in order to connect the conductive layer **110** to another conductive layer, the opening portion does not need to be provided in the insulating layer **121**. Thus, the opening portion reaching the conductive layer **110** can be easily formed.

[0144] FIGS. **2**A and **2**C illustrate an example in which part of the end portion of the insulating layer **121** is aligned or substantially aligned with the end portion of the conductive layer **120***a* positioned over the insulating layer **160**. FIGS. **2**A and **2**C illustrate an example in which another part of the end portion of the insulating layer **121** is aligned or substantially aligned with the end portion of the conductive layer **120***b* positioned over the insulating layer **160**. Although the details will be described later, processing the insulating layer **121** and a conductive film to be the conductive layer **120***a* and the conductive layer **120***b* with the use of the same mask enables the end portions of the conductive layer **120***a* and the conductive layer **120***b* positioned over the insulating layer **160** and the end portions of the insulating layer **121** to have the above-described structure.

[0145] The insulating layer **185** is provided over the capacitor **100***a* and the capacitor **100***b*. The insulating layer **186** is provided over the insulating layer **185**. The insulating layer **185** is provided along the top surface and the side surface of the conductive layer **120***a*, the top surface and the side surface of the conductive layer **120***b*, and the top surface of the insulating layer **121** in the opening portion **190**. Accordingly, the insulating layer **185** has a depressed portion **187** at a position overlapping with the opening portion **190**. The insulating layer **186** is provided to fill at least part of the depressed portion **187**.

[0146] The insulating layer **185** includes a region not overlapping with the insulating layer **186**. For example, after the insulating layer **186** is formed over the insulating layer **185**, planarization treatment is performed on the insulating layer **186** until at least part of the top surface of the insulating layer **185** is exposed. Thus, the insulating layer **185** can include a region not overlapping with the insulating layer **186**.

[0147] Since the insulating layer **186** is provided to fill at least part of the depressed portion **187** and the top surface of the insulating layer **186** is planarized, the transistor **200***a* and the transistor **200***b* over the insulating layer **185** can be easily formed. For example, a component of the transistor **200***a* and a component of the transistor **200***b* can be prevented from being divided due to a step caused by the depressed portion **187**. This can increase the manufacturing yield of the semiconductor device, and thus an inexpensive semiconductor device can be provided.

[0148] An opening portion reaching the conductive layer **120***a* and an opening portion reaching the conductive layer **120***b* are provided in the insulating layer **185**. The conductive layer **161***a* is provided in the opening portion reaching the conductive layer **120***a*, and the conductive layer **161***b* is provided in the opening portion reaching the conductive layer **120***b*.

[Transistor **200**]

[0149] The transistor **200***a* includes a conductive layer **220***a* over the conductive layer **161***a*, the insulating layer **185**, and the insulating layer **186**; a conductive layer **255** over the insulating layer **280**; a conductive layer **240***a* over the insulating layer **281**; an insulating layer **225**; an oxide semiconductor layer **230***a* over the conductive layer **220***a* and the conductive layer **240***a*; an insulating layer **250** over the oxide semiconductor layer **230***a*; and a conductive layer **260** over the insulating layer **250**. Here, FIG. **1**D is a plan view in which the conductive layer **260**, the oxide semiconductor layer **230***a*, and the oxide semiconductor layer **230***b* illustrated in FIG. **1**C are omitted and the conductive layers **240***a* and **240***b* are shown with hatching patterns.
[0150] Similarly, the transistor **200***b* includes a conductive layer **220***b* over the conductive layer **161***b*, the insulating layer **185**, and the insulating layer **186**; the conductive layer **255** over the insulating layer **280**; the conductive layer **240***b* over the insulating layer **281**; the insulating layer **225**; the oxide semiconductor layer **230***b* over the conductive layer **220***b* and the conductive layer **240***b*; the insulating layer **250** over the oxide semiconductor layer **230***b*; and the conductive layer **260** over the insulating layer **250**.
[0151] The oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b* function as semiconductor layers of the transistor **200***a* and the transistor **200***b*, respectively. The conductive layer **255** functions as a first gate electrode of each of the transistor **200***a* and the transistor **200***b*. The insulating layer **225** functions as a first gate insulating layer of each of the transistor **200***a* and the transistor **200***b*. The conductive layer **260** functions as a second gate electrode of each of the transistor **200***a* and the transistor **200***b*. The insulating layer **250** functions as a second gate insulating layer of each of the transistor **200***a* and the transistor **200***b*.
[0152] The conductive layer **220***a* functions as one of a source electrode and a drain electrode of the transistor **200***a*. The conductive layer **220***b* functions as one of a source electrode and a drain electrode of the transistor **200***b*. The conductive layer **240***a* functions as the other of the source electrode and the drain electrode of the transistor **200***a*. The conductive layer **240***b* functions as the other of the source electrode and the drain electrode of the transistor **200***b*.
[0153] The conductive layer **220***a* is connected to the conductive layer **120***a* through the conductive layer **161***a*. In this manner, the upper electrode of the capacitor **100***a* is connected to one of the source electrode and the drain electrode of the transistor **200***a*. Similarly, the conductive layer **220***b* is connected to the conductive layer **120***b* through the conductive layer **161***b*. Thus, the upper electrode of the capacitor **100***b* is connected to one of the source electrode and the drain electrode of the transistor **200***b*. The conductive layer **161***a* can be in contact with the conductive layer **120***a* and the conductive layer **220***a*, for example. The conductive layer **161***b* can be in contact with the conductive layer **120***b* and the conductive layer **220***b*, for example. Furthermore, the conductive layer **220***a* can include a region in contact with the top surface of the conductive layer **161***a*, for example. Furthermore, the conductive layer **220***b* can include a region in contact with the top surface of the conductive layer **161***b*, for example.
[0154] The conductive layer **255** is provided to extend in the X direction and the conductive layer **260** is provided to extend in the Y direction. The region where the conductive layer **255** extends functions as one of the wiring WOL and the wiring BGL. The region where the conductive layer **260** extends functions as the other of the wiring WOL and the wiring BGL. The conductive layer **255** and the conductive layer **260** can each be regarded as also having a function of a gate wiring. In addition, the conductive layer **255** may be provided to extend in the Y direction. The conductive layer **260** may be provided to extend in the X direction.
[0155] The insulating layer **280** is positioned over the conductive layers **220***a* and **220***b*. The insulating layer **281** is positioned over the conductive layer **255**.
[0156] As illustrated in FIGS. **1**A, **1**C, and **1**D and FIGS. **2**A to **2**D, an opening portion **290** reaching the conductive layers **220***a* and **220***b* and the insulating layer **186** is provided in the insulating layer **280**, the conductive layer **255**, and the insulating layer **281**. As illustrated in FIGS. **1**A, **1**C, and **1**D, the opening portion **290** preferably has a circular shape in the plan view. When the

opening portion has a circular shape, the processing accuracy in forming the opening portion can be increased as described above, and thus the opening portion can be formed to have a minute size.

[0157] The opening portion **290** includes an opening portion in the insulating layer **280**, an opening portion of the conductive layer **255**, and an opening portion of the insulating layer **281**. The shape and the size of the opening portion **290** in the plan view may differ from layer to layer. When the shape of the opening portion **290** is circular in the plan view, the opening portions included in the layers may or may not be concentric with each other.

[0158] At least parts of the components of the transistor **200***a* and the transistor **200***b* are provided in the opening portion **290**. Specifically, at least parts of the insulating layer **225**, the oxide semiconductor layer **230***a*, the oxide semiconductor layer **230***b*, the insulating layer **250**, and the conductive layer **260** are provided in the opening portion **290**. In addition, the parts of the insulating layer **225**, the oxide semiconductor layer **230***a*, the oxide semiconductor layer **230***b*, the insulating layer **250**, and the conductive layer **260** that are provided in the opening portion **290** reflect the shape of the opening portion **290**.

[0159] The insulating layer **225** is provided along the sidewall of the opening portion **290**, the side surface of the conductive layer **220***a* that overlaps with the opening portion **290**, and the side surface of the conductive layer **220***b* that overlaps with the opening portion **290**. The oxide semiconductor layer **230***a* is provided along the top surface of the conductive layer **240***a*, the side surface of the insulating layer **225**, the top surface of the conductive layer **220***a*, and the top surface of the insulating layer **186**. The oxide semiconductor layer **230***b* is provided along the top surface of the conductive layer **240***b*, the side surface of the insulating layer **225**, the top surface of the conductive layer **220***b*, and the top surface of the insulating layer **186**. The insulating layer **250** is provided along the top surface and the side surface of the oxide semiconductor layer **230***a*, the top surface and the side surface of the oxide semiconductor layer **230***b*, the top surface of the insulating layer **186**, the top surface and the side surface of the conductive layer **240***a*, the top surface and the side surface of the conductive layer **240***b*, and the top surface of the insulating layer **281**. Here, the insulating layer **225** is provided along the sidewall of the opening portion **290**, and the oxide semiconductor layers **230***a* and **230***b* are provided along the side surface of the insulating layer **225**, which means that the oxide semiconductor layers **230***a* and **230***b* are provided along the sidewall of the opening portion **290**. The insulating layer **250** is provided along the side surfaces of the oxide semiconductor layers **230***a* and **230***b* in the opening portion **290**, which means that the insulating layer **250** is also provided along the sidewall of the opening portion **290**.

[0160] The conductive layer **240***a* and the conductive layer **240***b* are provided apart from each other over the insulating layer **281**. The conductive layer **240***a* and the conductive layer **240***b* are provided to extend in the Y direction. The extending region of the conductive layer **240***a* and the extending region of the conductive layer **240***b* function as the wiring BILa and the wiring BILb, respectively. Alternatively, the conductive layer **240***a* and the conductive layer **240***b* may be provided to extend in the X direction.

[0161] The conductive layer **240***a* and the conductive layer **240***b* include a cutout portion at a position overlapping with the opening portion **290**. In a plan view, the outline of the cutout portion matches or roughly matches with part of the outline of the opening portion **290**. For example, in the case where the opening portion **290** is circular in the plan view, the cutout portion is arc-shaped. The sidewall of the opening portion **290** includes the side surface of the insulating layer **280**, the side surface of the conductive layer **255**, and the side surface of the insulating layer **281**.

[0162] The contact area between the conductive layer **240***a* and the oxide semiconductor layer **230***a* and the contact area between the conductive layer **240***b* and the oxide semiconductor layer **230***b* are larger in the case where the conductive layer **240***a* and the conductive layer **240***b* each include the cutout portion than in the case where the conductive layer **240***a* and the conductive layer **240***b* include no cutout portion. Thus, the on-state current of the transistor **200***a* and the transistor **200***b* can be increased. Here, the case where the conductive layer **240***a* and the

conductive layer **240***b* include no cutout portion refers to the case where the side surfaces of the conductive layers **240***a* and **240***b* that face each other do not match with the outline of the opening portion **290**, in which case the shapes of the conductive layers **240***a* and **240***b* in the plan view are, for example, quadrangular.

[0163] The insulating layer **225** is provided along at least part of the sidewall of the opening portion **290**. In FIGS. **2**A to **2**D, the insulating layer **225** is provided to cover the sidewall of the opening portion **290**. Specifically, the insulating layer **225** includes a region in contact with the side surface of the insulating layer **281**, a region in contact with the side surface of the conductive layer **255**, and a region in contact with the side surface of the insulating layer **280** in the opening portion **290**. The insulating layer **225** includes a region in contact with the inner side surface (on the opening portion **290** side in the plan view) of the conductive layer **240***a* and a region in contact with the inner side surface (on the opening portion **290** side in the plan view) of the conductive layer **240***b*. The insulating layer **225** can also be referred to as a sidewall, a sidewall insulating layer, or a sidewall protective layer, for example.

[0164] The insulating layer **225** includes a region in contact with the side surface of the conductive layer **220***a* on the opening portion **290** side and a region in contact with the side surface of the conductive layer **220***b* on the opening portion **290** side in some cases. In this case, the insulating layer **225** can include a region in contact with the insulating layer **186**. In addition, the insulating layer **225** may include a region in contact with the insulating layer **185**.

[0165] The oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b* are provided apart from each other. As illustrated in FIG. **2**D, the oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b* in the opening portion **290** are each provided to have an arc shape in the plan view.

[0166] The oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b* are provided to cover part of the insulating layer **225** in the opening portion **290**. The oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b* each include a region facing the conductive layer **255** with the insulating layer **225** therebetween in the opening portion **290**. The oxide semiconductor layer **230***a* includes a region in contact with the top surface of the conductive layer **220***a* in the opening portion **290** and a region in contact with the top surface of the conductive layer **240***a* outside the opening portion **290**. Similarly, the oxide semiconductor layer **230***b* includes a region in contact with the top surface of the conductive layer **220***b* in the opening portion **290** and a region in contact with the top surface of the conductive layer **240***b* outside the opening portion **290**. The oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b* can each include a region in contact with the top surface of the insulating layer **186**.

[0167] Outside the opening portion **290**, the end portions of the oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b* are positioned inward (on the opening portion **290** side) from the end portions of the conductive layer **240***a* and the conductive layer **240***b*.

[0168] The insulating layer **250** is provided to cover the oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b* in the opening portion **290**. The insulating layer **250** is provided to cover the top surfaces and the side surfaces of the oxide semiconductor layer **230***a*, the oxide semiconductor layer **230***b*, the conductive layer **240***a*, and the conductive layer **240***b* over the insulating layer **281**. The insulating layer **250** can include a region in contact with the insulating layer **186**. The insulating layer **250** has a depressed portion at a position overlapping with the opening portion **290**.

[0169] The conductive layer **260** is provided to fill at least part of the depressed portion of the insulating layer **250**. The conductive layer **260** includes a region facing the oxide semiconductor layer **230***a* with the insulating layer **250** therebetween and a region facing the oxide semiconductor layer **230***b* with the insulating layer **250** therebetween in the opening portion **290**. The conductive layer **260** includes a region facing the conductive layer **255** with the insulating layer **225**, the oxide semiconductor layer **230***a*, and the insulating layer **250** therebetween and a region facing the

conductive layer **255** with the insulating layer **225**, the oxide semiconductor layer **230***b*, and the insulating layer **250** therebetween in the opening portion **290**.

[0170] As described above, the oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b* are provided in the opening portion **290**. The transistor **200***a* and the transistor **200***b* each have a structure in which a current flows in the vertical direction since one of a source electrode and a drain electrode (here, the conductive layer **220***a* and the conductive layer **220***b*) is positioned on the lower side and the other of the source electrode and the drain electrode (here, the conductive layer **240***a* and the conductive layer **240***b*) is positioned on the upper side. In other words, a channel is formed along the sidewall of the opening portion **290**. That is, the transistor **200***a* and the transistor **200***b* are vertical transistors.

[0171] The conductive layer **255** includes a region facing the conductive layer **260** with the insulating layer **225**, the oxide semiconductor layer **230***a*, and the insulating layer **250** therebetween and a region facing the conductive layer **260** with the insulating layer **225**, the oxide semiconductor layer **230***b*, and the insulating layer **250** therebetween. In the oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b*, the region sandwiched between the conductive layer **255** and the conductive layer **260** and the vicinity of the region function as channel formation regions of the transistor **200***a* and the transistor **200***b*. One of a region of the oxide semiconductor layer **230***a* which is in the vicinity of the conductive layer **220***a* and a region of the oxide semiconductor layer **230***a* which is in the vicinity of the conductive layer **240***a* functions as a source region, and the other functions as a drain region. Similarly, one of a region of the oxide semiconductor layer **230***b* which is in the vicinity of the conductive layer **220***b* and a region of the oxide semiconductor layer **230***b* which is in the vicinity of the conductive layer **240***b* functions as a source region, and the other functions as a drain region. In other words, a channel formation region is sandwiched between the source region and the drain region.

[0172] The above structure enables the channel formation region and at least one of the source region and the drain region to be formed in the opening portion **290**. Thus, the areas occupied by the transistor **200***a* and the transistor **200***b* can be reduced as compared with a planar transistor in which the channel formation region, the source region, and the drain region are provided separately on the XY plane. Accordingly, the semiconductor device can be miniaturized or highly integrated.

[0173] In the semiconductor device of this embodiment, the capacitor **100***a* and the capacitor **100***b* are provided in one opening portion **190**. Furthermore, the channel formation regions of the transistor **200***a* and the transistor **200***b* are provided in one opening portion **290**. This structure can reduce the area occupied by the memory cell **150**, for example, compared with the case where only one capacitor is provided in one opening portion **190** and the channel formation region of only one transistor is provided in one opening portion **290**. Accordingly, miniaturization or higher integration of the semiconductor device can be achieved.

[0174] The transistor **200***a* and the transistor **200***b* illustrated in FIGS. **1**A to **1**D and FIGS. **2**A to **2**D each include the conductive layer **255** functioning as the first gate electrode and the conductive layer **260** functioning as the second gate electrode. By changing the potential applied to the conductive layer **260** independently of the potential applied to the conductive layer **255**, the threshold voltages V.sub.th of the transistors can be controlled. Specifically, when a negative potential is applied to the conductive layer **260**, the V.sub.th of the transistors can be further increased and the off-state currents can be reduced. Thus, a drain current at a 0 V potential applied to the conductive layer **255** can be lower when a negative potential is applied to the conductive layer **260** than when no potential or a potential of 0 V or higher is applied to the conductive layer **260**. In addition, the conductive layer **255** may function as the second gate electrode and the conductive layer **260** may function as the first gate electrode.

[0175] Alternatively, the conductive layer **260** may be connected to the conductive layer **255**. By applying the same potential to the conductive layer **255** and the conductive layer **260** that are connected to each other, the on-state current can be increased, variations in the initial

characteristics can be reduced, degradation in electric characteristics due to a negative gate bias-temperature (−GBT) stress test, and fluctuations in current-onset voltages at different drain voltages can be suppressed.

[0176] As described above, the transistor **200***a* and the transistor **200***b* illustrated in FIGS. **1**A to **1**D and FIGS. **2**A to **2**D each have a structure including two gate electrodes (the first gate electrode and the second gate electrode). Thus, the transistor **200***a* and the transistor **200***b* can have favorable electrical characteristics.

[0177] The conductive layer **240***a* and the conductive layer **240***b* are preferably not positioned in the opening portion **290**. That is, the conductive layer **240***a* and the conductive layer **240***b* preferably do not include a region in contact with the side surface of the insulating layer **281** in the opening portion **290**. With this structure, cutout portions of the conductive layer **240***a* and the conductive layer **240***b* and an opening portion of the insulating layer **280** can be formed collectively. Furthermore, the insulating layer **225**, the oxide semiconductor layer **230***a*, the oxide semiconductor layer **230***b*, and the like can be inhibited from being divided due to a step between the conductive layer **240***a* and the insulating layer **280**, a step between the conductive layer **240***b* and the insulating layer **280**, or the like.

[0178] As illustrated in FIG. **1**A and FIGS. **2**A and **2**C, the transistor **200***a* is provided to include a region overlapping with the capacitor **100***a*, and the transistor **200***b* is provided to include a region overlapping with the capacitor **100***b*. The opening portion **290** where parts of structures of the transistor **200***a* and the transistor **200***b* are provided includes a region overlapping with the opening portion **190** where parts of structures of the capacitor **100***a* and the capacitor **100***b* are provided. Thus, the area occupied by the memory cell **150** can be smaller than in the case where the opening portion **190** and the opening portion **290** do not overlap with each other, for example. Accordingly, miniaturization or higher integration of the semiconductor device can be achieved. FIG. **1**A illustrates an example in which the opening portion **190** and the opening portion **290** have the same shape in the plan view; however, the opening portion **190** and the opening portion **290** may have different shapes. The sizes (e.g., diameters in the case of circular shapes) of the opening portion **190** and the opening portion **290** in the plan view may be different from each other.

[0179] In addition, the opening portion **190** may be provided with parts of structures of three or more capacitors. Parts of structures of three or more transistors may be provided in the opening portion **290**. For example, parts of structures of four capacitors can be provided in the opening portion **190** and parts of structures of four transistors can be provided in the opening portion **290**.

[0180] FIG. **3**A is an enlarged view of a region including the transistor **200***a* and the transistor **200***b* illustrated in FIG. **2**A as described above. FIG. **3**B is an enlarged view of FIG. **2**D. In FIG. **3**A, an opening portion that is included in the insulating layer **185** and reaches the conductive layer **120***a* is referred to as an opening portion **191***a*. An opening portion that is included in the insulating layer **185** and reaches the conductive layer **120***b* is referred to as an opening portion **191***b*.

[0181] As illustrated in FIG. **3**B, the side surface of the conductive layer **255** provided outside the opening portion **290** faces the side surface of the oxide semiconductor layer **230***a* and the side surface of the oxide semiconductor layer **230***b* with the insulating layer **225** therebetween. The side surface of the conductive layer **260** provided in the region including the center of the opening portion **290** faces the side surface of the oxide semiconductor layer **230***a* and the side surface of the oxide semiconductor layer **230***b* with the insulating layer **250** therebetween. In other words, at least part of a portion of the oxide semiconductor layer **230***a* that is positioned in the opening portion **290** serves as the channel formation region of the transistor **200***a*. At least part of a portion of the oxide semiconductor layer **230***b* that is positioned in the opening portion **290** serves as the channel formation region of the transistor **200***b*. In this case, for example, the channel width of the transistor **200***a* is determined by the length of the perimeter of a portion of the oxide semiconductor layer **230***a* that is positioned in the opening portion **290**. The channel width of the transistor **200***b* is determined by the length of the perimeter of a portion of the oxide semiconductor layer **230***b* that is

positioned in the opening portion **290**. Accordingly, it can be said that the channel widths of the transistor **200***a* and the transistor **200***b* are determined by the width of the opening portion **290** (the diameter in the case where the opening portion **290** is circular in the plan view) and the distance between the oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b*, e.g., the distance between the end portion of the oxide semiconductor layer **230***a* and the end portion of the oxide semiconductor layer **230***b*. In FIGS. **3**A and **3**B, the width of the opening portion **290** is denoted by D. FIG. **3**B also illustrates a channel width W of the transistor **200***a* and a distance Hab between the end portion of the oxide semiconductor layer **230***a* and the end portion of the oxide semiconductor layer **230***b*. Note that the distance Hab can be measured on the XY plane including the conductive layer **255**.

[0182] By increasing the width D of the opening portion **290**, the channel width per unit area can be increased and the on-state current can be increased. Meanwhile, the area occupied by the transistor **200**, e.g., the area of the transistor **200** in the plan view, is roughly determined by the width of the opening portion **290**. When the width D of the opening portion **290** is reduced, the area occupied by the transistor **200** can be reduced and the semiconductor device can be highly integrated.

[0183] The width D of the opening portion **290** sometimes varies in the depth direction (the Z direction in the case where the side surface of the opening portion **290** is perpendicular to the substrate surface). Here, the shortest distance between two side surfaces of the insulating layer **281** in the opening portion **290** in a cross-sectional view is particularly used as the width D. In other words, the minimum width of the opening portion **290** in the insulating layer **281** is used as the width D of the opening portion **290**. Here, the cross-sectional view refers to a cross section seen from the X direction or the Y direction of a region including the center (or the center of gravity) of the opening portion **290** seen from the Z direction. The width of the opening portion **290** at the highest position, the width of the opening portion **290** at the lowest position, or the width of the opening portion **290** at the midpoint therebetween in the insulating layer **281**, or the average value of these three widths may be used as the width D.

[0184] Although an example in which the width D is determined by the width of the opening portion **290** in the insulating layer **281** is described here, there is no particular limitation on the method for determining the width D. For example, in the cross-sectional view, the shortest distance between the two side surfaces of the conductive layer **255** on the opening portion **290** side or the shortest distance between the two side surfaces of the insulating layer **281** on the opening portion **290** side can be used as the width D. For example, the shortest distance between the inner side surface (on the opening portion **290** side in the plan view) of the conductive layer **240***a* and the inner side surface (on the opening portion **290** side in the plan view) of the conductive layer **240***b* in the cross-sectional view may be used as the width D.

[0185] The width D of the opening portion **290** is determined by the thicknesses of the insulating layer **225**, the oxide semiconductor layer **230***a*, the insulating layer **250**, and the conductive layer **260** provided in the opening portion **290**. The width D of the opening portion **290** is preferably, for example, greater than or equal to 5 nm, greater than or equal to 10 nm, or greater than or equal to 20 nm and less than or equal to 300 nm, less than or equal to 200 nm, less than or equal to 100 nm, less than or equal to 60 nm, less than or equal to 50 nm, less than or equal to 40 nm, or less than or equal to 30 nm.

[0186] Note that the width D of the opening portion **290** is larger than the distance Hab. Specifically, the width D of the opening portion **290** is preferably larger than the sum of twice the thickness of the insulating layer **225** and the distance Hab. In this manner, the oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b* (also collectively referred to as an oxide semiconductor layer **230**) can be provided in the opening portion **290**. Here, the thickness of the insulating layer **225** refers to the width in the X direction of at least part of the insulating layer **225** in the example illustrated in FIG. **3**A. Furthermore, the width D of the opening portion **290** is

preferably larger than the sum of twice the thickness of the insulating layer **225**, twice the thickness of the oxide semiconductor layer **230***a* or **230***b*, and the distance Hab. This can inhibit a reduction in the thickness (i.e., decreased film thickness) of the oxide semiconductor layer **230** and a reduction in the area of the channel formation region in the plan view. Here, for example, the thickness of the oxide semiconductor layer **230** refers to the width in the X direction of at least part of the oxide semiconductor layer **230** positioned in the opening portion **290** in the example illustrated in FIG. **3**A.

[0187] Furthermore, a small distance Hab is preferable. When the distance Hab is shortened, the channel width W can be increased. Moreover, the semiconductor device can be miniaturized or highly integrated. For example, the distance Hab is preferably greater than or equal to 10 nm and less than or equal to 60 nm, further preferably greater than or equal to 10 nm and less than or equal to 50 nm, still further preferably greater than or equal to 10 nm and less than or equal to 40 nm, yet still further preferably greater than or equal to 10 nm and less than or equal to 30 nm. The distance Hab is, for example, preferably greater than or equal to 5 nm and less than or equal to 50 nm, further preferably greater than or equal to 5 nm and less than or equal to 40 nm, still further preferably greater than or equal to 5 nm and less than or equal to 30 nm.

[0188] The channel length of each of the transistors **200***a* and **200***b* corresponds to the distance between the source region and the drain region. For example, in the case where the conductive layer **255** functions as the first gate electrode, the channel length of each of the transistor **200***a* and the transistor **200***b* is the length of a region of each of the oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b* that faces the conductive layer **255** with the insulating layer **225** therebetween in the cross-sectional view. In other words, the channel lengths of the transistor **200***a* and the transistor **200***b* are determined by the thickness of the conductive layer **255**. In the case where the conductive layer **260** and the conductive layer **255** are connected to each other, the channel lengths of the transistor **200***a* and the transistor **200***b* are the lengths of regions interposed between the conductive layer **260** and the conductive layer **255** in the oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b* in the cross-sectional view. In other words, the channel lengths of the transistor **200***a* and the transistor **200***b* are determined by the thickness of the conductive layer **255**. In FIG. **3**A, the channel length L of the transistor **200***a* is indicated by a dashed-dotted double-headed arrow.

[0189] In the case where the conductive layer **260** functions as the first gate electrode, the channel length of the transistor **200***a* can be determined by the thickness of the insulating layer **280** over the conductive layer **220***a*, the thickness of the conductive layer **255**, the thickness of the insulating layer **281**, the thickness of the conductive layer **240***a*, and the like in the cross-sectional view. Similarly, the channel length of the transistor **200***b* can be determined by the thickness of the insulating layer **280** over the conductive layer **220***b*, the thickness of the conductive layer **255**, the thickness of the insulating layer **281**, the thickness of the conductive layer **240***b*, and the like in the cross-sectional view.

[0190] Further miniaturization of a planar transistor is difficult since the channel length of the planar transistor is restricted by the light exposure limit of photolithography; however, the channel lengths of the transistor **200***a* and the transistor **200***b* can be determined by the thickness or the like of the conductive layer **255**. Thus, the transistor **200***a* and the transistor **200***b* can each have an extremely small channel length less than or equal to the light exposure limit of photolithography (e.g., less than or equal to 60 nm, less than or equal to 50 nm, less than or equal to 40 nm, less than or equal to 30 nm, less than or equal to 20 nm, or less than or equal to 10 nm, and greater than or equal to 0.1 nm, greater than or equal to 1 nm, or greater than or equal to 5 nm). Accordingly, the transistor **200***a* and the transistor **200***b* can have higher on-state current and higher frequency characteristics.

[0191] Note that the channel length of each of the transistor **200***a* and the transistor **200***b* is determined by the thickness or the like of the conductive layer **255**; thus, the channel length does

not affect the area occupied by the transistor **200***a* and the transistor **200***b*, for example, the area occupied by the transistor **200***a* and the transistor **200***b* in the plan view. When the channel lengths of the transistor **200***a* and the transistor **200***b* are, for example, less than or equal to 1 μm, less than or equal to 500 nm, or less than or equal to 300 nm, the productivity, yield, and the like in the formation of the opening portion **290** and the like can be increased.

[0192] From the above, the channel length of the transistor included in the semiconductor device of one embodiment of the present invention is preferably greater than or equal to 0.1 nm, greater than or equal to 1 nm, or greater than or equal to 5 nm, and less than or equal to 1 μm, less than or equal to 500 nm, or less than or equal to 300 nm.

[0193] The channel length L of the transistor **200** is preferably shorter than at least the channel width W of the transistor **200**. The channel length L of the transistor **200** is preferably greater than or equal to 0.1 times and less than or equal to 0.99 times, further preferably greater than or equal to 0.5 times and less than or equal to 0.8 times the channel width W of the transistor **200**. This structure enables the transistor to have favorable electrical characteristics and high reliability.

[0194] In addition, the channel width W of the transistor **200** may be less than or equal to the channel length L of the transistor **200**. This structure enables miniaturization or high integration of the semiconductor device.

[0195] As described above, when the opening portion **290** is formed to be circular in the plan view, the insulating layer **225** in the opening portion **290** has a ring shape or an annular shape in the plan view. Specifically, the insulating layer **225** includes an annular portion having an opening portion that is concentric with the opening portion **290**. The oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b* are provided to be arc-shaped. Furthermore, the insulating layer **250** and the conductive layer **260** are provided along the shapes of the insulating layer **225**, the oxide semiconductor layer **230***a*, and the oxide semiconductor layer **230***b*. This makes each of the distance between the conductive layer **255** and the oxide semiconductor layer **230***a* and the distance between the conductive layer **260** and the oxide semiconductor layer **230***a* substantially uniform, so that a gate electric field can be substantially uniformly applied to the oxide semiconductor layer **230***a*. Similarly, this makes each of the distance between the conductive layer **255** and the oxide semiconductor layer **230***b* and the distance between the conductive layer **260** and the oxide semiconductor layer **230***b* substantially uniform, so that a gate electric field can be substantially uniformly applied to the oxide semiconductor layer **230***b*.

[0196] Although this embodiment describes the example where the opening portion **190** and the opening portion **290** each have a circular shape in the plan view, the present invention is not limited to the example. The opening portion **190** and the opening portion **290** in the plan view can have a circular shape, a substantially circular shape such as an elliptical shape, a polygonal shape such as a triangular shape, a quadrangular shape (including a rectangular shape, a rhombic shape, and a square), a pentagonal shape, or a star polygonal shape, or any of these polygonal shapes whose corners are rounded, for example. Note that the polygonal shape may be a concave polygonal shape (a polygonal shape having at least one interior angle greater than 180°) or a convex polygonal shape (a polygonal shape having all the interior angles less than or equal to 180°).

[0197] The conductive layer **240***a* and the conductive layer **240***b* can each have a stacked-layer structure of two or more layers. FIG. **3**A illustrates an example where the conductive layer **240***a* has a two-layer structure of a conductive layer **240***a***1** and a conductive layer **240***a***2** over the conductive layer **240***a***1**. Similarly, in the example, the conductive layer **240***b* has a two-layer structure of a conductive layer **240***b***1** and a conductive layer **240***b***2** over the conductive layer **240***b***1**.

[0198] The conductive layer **220***a* and the conductive layer **220***b* can each have a stacked-layer structure of two or more layers. FIG. **3**A illustrates an example where the conductive layer **220***a* has a two-layer structure of a conductive layer **220***a***1** and a conductive layer **220***a***2** over the conductive layer **220***a***1**. Similarly, in the example, the conductive layer **220***b* has a two-layer

structure of a conductive layer **220***b***1** and a conductive layer **220***b***2** over the conductive layer **220***b***1**.

[0199] In the example illustrated in FIG. **3**A, the top surface of the conductive layer **220***a* includes a depressed portion **221***a* and the top surface of the conductive layer **220***b* includes a depressed portion **221***b*. Specifically, the top surface of the conductive layer **220***a***2** includes the depressed portion **221***a* and the top surface of the conductive layer **220***b***2** includes the depressed portion **221***b*. Hereinafter, the depressed portion **221***a* and the depressed portion **221***b* may be collectively referred to as a depressed portion **221**.

[0200] The depressed portion **221***a* and the depressed portion **221***b* are provided at positions overlapping with the opening portion **290**. In the case where the conductive layer **220***a* has a two-layer structure of the conductive layer **220***a***1** and the conductive layer **220***a***2**, the bottom surface of the depressed portion **221***a* corresponds to the bottom surface of the depressed portion of the conductive layer **220***a***2**, and the side surface of the depressed portion **221***a* corresponds to the side surface of the depressed portion of the conductive layer **220***a***2**. Similarly, the bottom surface of the depressed portion **221***b* corresponds to the bottom surface of the depressed portion of the conductive layer **220***b***2**, and the side surface of the depressed portion **221***b* corresponds to the side surface of the depressed portion of the conductive layer **220***b***2**. The bottom portion of the opening portion **290** includes the bottom surface of the depressed portion **221***a* and the bottom surface of the depressed portion **221***b*. The sidewall of the opening portion **290** can be regarded as including the side surface of the depressed portion **221***a*, the side surface of the depressed portion **221***b*, the side surface of the insulating layer **280**, the side surface of the conductive layer **255**, and the side surface of the insulating layer **281**.

[0201] When each conductive layer **220** (the conductive layers **220***a* and **220***b*) includes the depressed portion **221** at the position overlapping with the opening portion **290**, the heights of the bottom surfaces of the insulating layer **250** and the conductive layer **260** in the opening portion **290** can be made lower than the height of the top surface of the conductive layer **220** which is in contact with the insulating layer **280**, as compared with the case where the depressed portion **221** is not provided. Here, the heights of the surfaces can be determined with a surface where a transistor is formed (formation surface of a transistor) used as a reference plane. Here, the top surface of the insulating layer **186** in a region overlapping with the conductive layer **220** is used as a reference plane. The reference plane is not limited to a surface where a transistor is formed. For example, the top surface of a substrate where a transistor or a semiconductor device is provided may be used as the reference plane.

[0202] When the height of the bottom surface of the conductive layer **260** is lowered, a gate electric field is easily applied from the conductive layer **260** to the channel formation regions of the oxide semiconductor layers **230***a* and **230***b*. Accordingly, the transistors **200***a* and **200***b* can have favorable electrical characteristics. Furthermore, a gate electric field is also easily applied from the conductive layer **260** to a region of the oxide semiconductor layer **230***a* that is in contact with the conductive layer **220***a***2** and a region of the oxide semiconductor layer **230***b* that is in contact with the conductive layer **220***b***2**. This can increase the on-state current of the transistor **200***a* and the transistor **200***b*. In both of the cases where the conductive layer **220***a* and the conductive layer **220***b* are used for the drain electrodes and where the conductive layer **240***a* and the conductive layer **240***b* are used for the drain electrodes, the transistor **200***a* and the transistor **200***b* can have favorable electrical characteristics.

[0203] In the case where the depressed portion **221** is provided in the conductive layer **220***a***2** and the conductive layer **220***b***2**, a depressed portion **222** is provided in the insulating layer **186** at a position overlapping with the opening portion **290** in some cases, for example. In that case, the height of the bottom surface of the insulating layer **250** and the height of the bottom surface of the conductive layer **260** in the opening portion **290** can be further lowered.

[0204] FIG. **4**A is an enlarged view of the capacitor **100***a* and the capacitor **100***b* illustrated in FIG.

2A as described above. For example, FIG. **4**A illustrates a structure in which the top surface of the conductive layer **110** includes a depressed portion. The depressed portion is provided at a position overlapping with the opening portion **190**. Here, the bottom portion of the depressed portion of the conductive layer **110** may be included in the bottom portion of the opening portion **190**. The sidewall of the depressed portion of the conductive layer **110** and the side surface of the insulating layer **160** may be included in the sidewall of the opening portion **190**.

[0205] When the conductive layer **110** includes a depressed portion at a position overlapping with the opening portion **190**, the contact area between the conductive layer **110** and the conductive layer **115** can be increased, compared with the case where the depressed portion is not provided. Thus, the contact resistance between the conductive layer **110** and the conductive layer **115** can be lowered.

[0206] The conductive layer **115** includes a region **101** with a curved corner in the depressed portion of the conductive layer **110**. This structure can inhibit electric field concentration on the insulating layer **121** in the vicinity of the region **101**, as compared with the case where the region **101** has an angular portion (a right angle or an acute angle) in the cross-sectional view, for example. The height from a reference surface of an end surface **103** of the conductive layer **115** is lower than that of a top surface **105** of the insulating layer **160**. This structure can inhibit electric field concentration on the insulating layer **121** in the vicinity of the end surface **103**, as compared with the case where the end surface **103** is positioned at a higher level than the insulating layer **160** is. When the concentration of electric field on the insulating layer **121** is inhibited in this manner, the dielectric breakdown of the insulating layer **121** can be inhibited, leading to formation of a highly reliable semiconductor device. In addition, for example, FIG. **4**A illustrates an example in which a region **102** between the top surface **105** of the insulating layer **160** and the side surface of the opening portion **190** has a curved portion. In the example illustrated in FIG. **4**A, the end surface **103** can be referred to as an upper end surface of the conductive layer **115**.

[0207] FIG. **4**B illustrates an example in which the end surface **103** illustrated in FIG. **4**A is provided at a higher level than the insulating layer **160** is. In the example illustrated in FIG. **4**B, the region **102** between the top surface **105** of the insulating layer **160** and the side surface of the opening portion **190** has a curved portion. In the example illustrated in FIG. **4**B, the end surface **103** has a tapered shape. In the case where the region **102** has a curved portion and the end surface **103** has a tapered shape, the concentration of electric field in the insulating layer **121** on the vicinity of the region **102** and the vicinity of the end surface **103** can be inhibited even when the end surface **103** is positioned at a higher level than the insulating layer **160** is. Accordingly, dielectric breakdown of the insulating layer **121** is inhibited, and thus a highly reliable semiconductor device can be provided. In the example illustrated in FIG. **4**B, the end surface **103** can be referred to as a side end surface of the conductive layer **115**.

[0208] FIG. **5**A illustrates an example in which the conductive layer **110** illustrated in FIG. **4**A has a two-layer structure of a conductive layer **1101** and a conductive layer **110_2** over the conductive layer **110_1**. FIG. **5**A illustrates a structure in which the top surface of the conductive layer **110_2** includes a depressed portion.

[0209] A material that can be used for the conductive layer **220***a***1** and the conductive layer **220***b***1** described later can be used for the conductive layer **110_1**. In addition, a material that can be used for the conductive layer **220***a***2** and the conductive layer **220***b***2** described later can be used for the conductive layer **110_2**. For example, a conductive material containing oxygen can be used for the conductive layer **110_2**. In addition, a material having higher conductivity than that used for the conductive layer **110_2** is preferably used for the conductive layer **110_1**. Specifically, for example, an oxide conductor (e.g., ITO, ITSO, or In—Zn oxide) is preferably used for the conductive layer **110_2**, and tungsten is preferably used for the conductive layer **110_1**. For the conductive layer **110_1**, ruthenium, titanium nitride, tantalum nitride, or the like may be used.

[0210] The use of a conductive material containing oxygen for the conductive layer **110_2** enables

a curved portion to easily formed in the region **101** in some cases. In this case, the concentration of electric field on the insulating layer **121** in the vicinity of the region **101** is easily inhibited.

[0211] FIG. **5**B illustrates an example in which the insulating layer **121** in FIG. **4**A is not patterned. Thus, the number of manufacturing steps of the semiconductor device can be smaller than that of the case where the insulating layer **121** is patterned. Meanwhile, by patterning the insulating layer **121**, for example, the insulating layer **180**, the insulating layer **111**, the insulating layer **160**, the insulating layer **185**, the insulating layer **186**, the insulating layer **280**, the insulating layer **281**, the insulating layer **250**, and the like illustrated in FIGS. **2**A to **2**C each include a region not overlapping with the insulating layer **121**. Thus, in the case where an opening portion reaching the conductive layer **110** is provided in the insulating layers in order to connect the conductive layer **110** to another conductive layer, for example, an opening portion does not need to be provided in the insulating layer **121**. Thus, the opening portion reaching the conductive layer **110** can be easily formed as compared with the case where the insulating layer **121** is not patterned.

[0212] FIG. **6**A illustrates an example in which the conductive layer **220***a***2**, the conductive layer **220***b***2**, and the insulating layer **186** illustrated in FIG. **3**A have no depressed portions. In the example illustrated in FIG. **6**A, the heights of the bottom surfaces of the oxide semiconductor layer **230***a*, the oxide semiconductor layer **230***b*, and the insulating layer **250** in the opening portion **290** can be the same as or substantially the same as the heights of the bottom surface of the conductive layer **220***a***1** and the bottom surface of the conductive layer **220***b***1**. In the example illustrated in FIG. **6**A, the height of the bottom surface of the insulating layer **225** can be the same as or substantially the same as the heights of the top surface of the conductive layer **220***a***2** and the top surface of the conductive layer **220***b***2**.

[0213] FIG. **6**B illustrates an example in which the conductive layer **220***a***2** and the conductive layer **220***b***2** illustrated in FIG. **3**A each include a first depressed portion and a second depressed portion positioned outside the first depressed portion. FIG. **6**B illustrates an example in which the first depressed portion has a larger depth than the second depressed portion. In other words, the bottom portion of the first depressed portion is positioned below the bottom portion of the second depressed portion (at a position closer to the insulating layer **186**). When the opening portion **290** is formed, the second depressed portion is provided in the conductive layer **220***a***2** and the conductive layer **220***b***2**. After that, when the insulating film is formed and processed to form the insulating layer **225**, the first depressed portion is provided in the conductive layer **220***a***2** and the conductive layer **220***b***2**. Thus, in FIG. **6**B, the sidewall of the second depressed portion is aligned with the side surface of the insulating layer **280** in the opening portion **290**. A sidewall of the first depressed portion is aligned with a surface of the insulating layer **225** on the oxide semiconductor layer **230***a* side or the oxide semiconductor layer **230***b* side. Hereinafter, the first depressed portion and the second depressed portion are collectively referred to as a depressed portion in some cases.

[0214] In FIG. **6**B, the insulating layer **225** is in contact with the bottom portions and the sidewalls of the depressed portions (specifically, the second depressed portions) of the conductive layer **220***a* and the conductive layer **220***b*, and is in contact with the side surfaces of the insulating layer **280**, the conductive layer **255**, the insulating layer **281**, the conductive layer **240***a*, and the conductive layer **240***b* in the opening portion **290**. The oxide semiconductor layer **230***a* is in contact with the bottom portion and the sidewall of the depressed portion (specifically, the first depressed portion) of the conductive layer **220***a* and the side surface of the insulating layer **225** in the opening portion **290**. Similarly, the oxide semiconductor layer **230***b* is in contact with the bottom portion and the sidewall of the depressed portion (specifically, the first depressed portion) of the conductive layer **220***b* and the side surface of the insulating layer **225** in the opening portion **290**. The insulating layer **250** is positioned inward from the oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b* in the opening portion **290**. The conductive layer **260** is positioned inward from the insulating layer **250** in the opening portion **290**.

[0215] When the conductive layer **220***a***2** includes the first depressed portion and the second

depressed portion, the side surface of the conductive layer **220***a***2** is in contact with the oxide semiconductor layer **230***a*. Accordingly, the contact area between the conductive layer **220***a***2** and the oxide semiconductor layer **230***a* can be increased, so that the contact resistance between the conductive layer **220***a***2** and the oxide semiconductor layer **230***a* can be lowered. Thus, the on-state current of the transistor **200***a* can be increased. Similarly, when the conductive layer **220***b***2** includes the first depressed portion and the second depressed portion, the on-state current of the transistor **200***b* can be increased.

[0216] Although FIG. **6**B illustrates the structure in which the conductive layer **220***a***2** includes the first depressed portion and the second depressed portion, the present invention is not limited to the structure. FIG. **7**A illustrates an example in which only the second depressed portion is provided in the conductive layer **220***a***2** illustrated in FIG. **6**B. In other words, the conductive layer **220***a***2** and the conductive layer **220***b***2** may have no depressed portion in a region overlapping with the insulating layer **225**.

[0217] In the conductive layer **220***a***2** and the conductive layer **220***b***2**, a depressed portion may be formed in one or both of a step of forming the opening portion **290** and a step of forming the insulating layer **225**. In the example of the semiconductor device illustrated in FIG. **6**B, depressed portions are formed in the conductive layer **220***a***2** and the conductive layer **220***b***2** in both of the steps. Meanwhile, FIG. **7**A illustrates an example of the semiconductor device in which a depressed portion is not formed in the conductive layer **220***a***2** and the conductive layer **220***b***2** in the step of forming the opening portion **290**, and a depressed portion is formed in the conductive layer **220***a***2** and the conductive layer **220***b***2** in the step of forming the insulating layer **225**.

[0218] In the example illustrated in FIG. **7**A, the insulating layer **225** is in contact with the side surface of the insulating layer **280**, the side surface of the conductive layer **255**, the side surface of the insulating layer **281**, the side surface of the conductive layer **240***a*, the side surface of the conductive layer **240***b*, the top surface of the conductive layer **220***a***2**, and the top surface of the conductive layer **220***b***2** in the opening portion **290**. The oxide semiconductor layer **230***a* is in contact with the bottom portion and the sidewall of the depressed portion in the conductive layer **220***a***2** and the side surface of the insulating layer **225** in the opening portion **290**. Similarly, the oxide semiconductor layer **230***b* is in contact with the bottom portion and the sidewall of the depressed portion of the conductive layer **220***b***2** and the side surface of the insulating layer **225** in the opening portion **290**.

[0219] When the depressed portion is formed in the conductive layer **220***a***2** in the step of forming the insulating layer **225**, the oxide semiconductor layer **230***a* can be in contact with the bottom portion and the sidewall of the depressed portion of the conductive layer **220***a***2**. This is preferable because the contact area between the oxide semiconductor layer **230***a* and the conductive layer **220***a***2** is increased and the contact resistance between the oxide semiconductor layer **230***a* and the conductive layer **220***a***2** can be reduced. Similarly, when the depressed portion is formed in the conductive layer **220***b***2** in the step of forming the insulating layer **225**, the contact resistance between the oxide semiconductor layer **230***b* and the conductive layer **220***b***2** can be lowered, which is preferable.

[0220] FIG. **7**B illustrates an example in which the side surface of the conductive layer **240***a***2** and the side surface of the conductive layer **240***b***2** are not covered with the insulating layer **225**. In the example illustrated in FIG. **7**B, the side surface of the conductive layer **220***a***2** and the side surface of the conductive layer **220***b***2** are not covered with the insulating layer **225**.

[0221] The insulating layer **225** illustrated in FIG. **7**B can be in contact with at least part of the side surface of the conductive layer **240***a***1** and at least part of the side surface of the conductive layer **240***b***1**. The insulating layer **225** illustrated in FIG. **7**B can be in contact with at least part of the side surface of the conductive layer **220***a***1** and at least part of the side surface of the conductive layer **220***b***1**. Here, the insulating layer **225** is in contact with neither the side surface on the opening portion **290** side of the conductive layer **240***a***2** nor the side surface on the opening portion **290** side

of the conductive layer **240***b***2**. The insulating layer **225** is in contact with neither the side surface of the conductive layer **220***a***2** nor the side surface of the conductive layer **220***b***2**. Note that the insulating layer **225** may be in contact with at least parts of the side surface of the conductive layer **240***a***2** and the side surface of the conductive layer **240***b***2**. The insulating layer **225** may be in contact with at least parts of the side surface of the conductive layer **220***a***2** and the side surface of the conductive layer **220***b***2**.

[0222] In the case where the conductive layer **260** functions as the first gate electrode, the channel lengths of the transistor **200***a* and the transistor **200***b* can be shortened with the structure illustrated in FIG. **7**B. Accordingly, the transistor can have a high on-state current.

[0223] In the case where the side surface on the opening portion **290** side of the conductive layer **240***a***2** includes a portion not covered with the insulating layer **225**, the portion is in contact with the oxide semiconductor layer **230***a*. Similarly, in the case where the side surface on the opening portion **290** side of the conductive layer **240***b***2** includes a portion not covered with the insulating layer **225**, the portion is in contact with the oxide semiconductor layer **230***b*. In this way, the contact area between the oxide semiconductor layer **230***a* and the conductive layer **240***a***2** and the contact area between the oxide semiconductor layer **230***b* and the conductive layer **240***b***2** can be increased. Thus, the contact resistance between the oxide semiconductor layer **230***a* and the conductive layer **240***a* and the contact resistance between the oxide semiconductor layer **230***b* and the conductive layer **240***b* can be lowered.

[0224] Furthermore, in the case where at least part of the side surface of the conductive layer **240***a***1** is not covered with the insulating layer **225**, a portion of the conductive layer **240***a***1** that is not covered with the insulating layer **225** is in contact with the oxide semiconductor layer **230***a*. Similarly, in the case where at least part of the side surface of the conductive layer **240***b***1** is not covered with the insulating layer **225**, a portion of the conductive layer **240***b***1** that is not covered with the insulating layer **225** is in contact with the oxide semiconductor layer **230***b*. In this manner, the contact area between the oxide semiconductor layer **230***a* and the conductive layer **240***a* and the contact area between the oxide semiconductor layer **230***b* and the conductive layer **240***b* can be increased. Thus, the contact resistance between the oxide semiconductor layer **230***a* and the conductive layer **240***a* and the contact resistance between the oxide semiconductor layer **230***b* and the conductive layer **240***b* can be lowered.

[0225] FIG. **8** is a diagram illustrating an example in which the depressed portion in the conductive layer **220***a***2** and the depressed portion in the conductive layer **220***b***2** illustrated in FIG. **6**B each include a curved portion. Specifically, in the example illustrated in FIG. **8**, the first depressed portion and the second depressed portion each include a curved portion.

[0226] When the depressed portion of the conductive layer **220***a***2** and the depressed portion of the conductive layer **220***b***2** each have a curved portion, portions of the oxide semiconductor layer **230***a*, the oxide semiconductor layer **230***b*, the insulating layer **250**, and the like that are provided over the depressed portions and in the vicinities of the depressed portions each have a curved portion in some cases. In other words, the portions each have a curved surface or a concave surface in the cross-sectional view in some cases. In addition, the portions may each have no corner portion in the cross-sectional view in some cases. Accordingly, the concentration of electric field on the insulating layer **250** in the vicinity of the depressed portions is relieved, and the withstand voltages of the transistor **200***a* and the transistor **200***b* can be increased, so that the electrostatic breakdown of the transistor **200***a* and the transistor **200***b* can be inhibited. Accordingly, the reliability of the semiconductor device can be improved.

<Component Materials of Semiconductor Device>

[0227] Materials that can be used for the semiconductor device of this embodiment are described below. Note that the layers included in the semiconductor device of this embodiment may each have a single-layer structure or a stacked-layer structure. Hereinafter, the oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b* are collectively referred to as the oxide

semiconductor layer **230** in some cases. The conductive layer **120***a* and the conductive layer **120***b* are collectively referred to as a conductive layer **120** in some cases. The conductive layer **161***a* and the conductive layer **161***b* are collectively referred to as a conductive layer **161** in some cases. The conductive layers **220***a* and the conductive layer **220***b* are collectively referred to as the conductive layer **220** in some cases. Furthermore, the conductive layer **240***a* and the conductive layer **240***b* are collectively referred to a conductive layer **240** in some cases.

[Oxide Semiconductor Layer]

[0228] As described above, the oxide semiconductor layer **230** includes the channel formation region. The oxide semiconductor layer **230** further includes the source region and the drain region. The source region and the drain region are low-resistance regions having a higher carrier concentration than the channel formation region. The oxide semiconductor layer **230** may have a single-layer structure or a stacked-layer structure of two or more layers.

[0229] There is no particular limitation on the crystallinity of the semiconductor material used for the oxide semiconductor layer **230**, and any of an amorphous semiconductor, a single crystal semiconductor, and a semiconductor having crystallinity other than single crystal (a microcrystalline semiconductor, a polycrystalline semiconductor, or a semiconductor partly including crystal regions) may be used. A single crystal semiconductor or a semiconductor having crystallinity is preferably used, in which case degradation of the transistor characteristics can be inhibited.

[0230] In the transistor **200**, the oxide semiconductor layer **230** including the channel formation region preferably includes a metal oxide (also referred to as an oxide semiconductor) functioning as a semiconductor. In the case where a metal oxide functioning as a semiconductor is used for the oxide semiconductor layer **230**, the transistor **200** can be regarded as an OS transistor.

[0231] When oxygen vacancies (Vo) and impurities are in the channel formation region of the oxide semiconductor in an OS transistor, electrical characteristics of the OS transistor easily vary and the reliability thereof may worsen in some cases. A defect that is an oxygen vacancy into which hydrogen enters (hereinafter also referred to as V.sub.OH in some cases) is formed and an electron serving as a carrier is generated in some cases. Thus, when the channel formation region of the oxide semiconductor includes oxygen vacancies, the OS transistor tends to have normally-on characteristics. Therefore, the oxygen vacancies and the impurities are preferably reduced as much as possible in the channel formation region of the oxide semiconductor. In other words, the oxide semiconductor preferably includes an i-type (intrinsic) or substantially i-type channel formation region with a low carrier concentration.

[0232] Meanwhile, preferably, the source region and the drain region of the OS transistor include more oxygen vacancies, include more V.sub.OH, or have a higher concentration of an impurity such as hydrogen, nitrogen, or a metal element than the channel formation region, and thus are low-resistance regions with high carrier concentrations. In other words, the source region and the drain region of the OS transistor are preferably regions having higher carrier concentrations and lower resistances than the channel formation region.

[0233] The band gap of the metal oxide functioning as a semiconductor is preferably greater than or equal to 2.0 eV, further preferably greater than or equal to 2.5 eV. The use of a metal oxide having a wide band gap for the oxide semiconductor layer **230** can reduce the off-state current of the transistor **200**. The off-state current of the OS transistor is small, so that power consumption of the semiconductor device can be sufficiently reduced. The OS transistor has high frequency characteristics, which enables the semiconductor device to operate at high speed.

[0234] For the oxide semiconductor layer that can be used as the semiconductor layer of the transistor of one embodiment of the present invention, description in Embodiment 2 can be referred to. Here, detailed description thereof is omitted.

[0235] Note that for the semiconductor device of this embodiment, a transistor including a different semiconductor material in its channel formation region may be used. Examples of the different

semiconductor material include a single-element semiconductor and a compound semiconductor.
[0236] Examples of the single-element semiconductor that can be used as the semiconductor material include silicon and germanium. Examples of silicon that can be used as the semiconductor material include single crystal silicon, polycrystalline silicon, microcrystalline silicon, and amorphous silicon. An example of polycrystalline silicon is low-temperature polysilicon (LTPS).
[0237] Examples of the compound semiconductor that can be used as the semiconductor material include silicon carbide, silicon germanium, gallium arsenide, indium phosphide, boron nitride, and boron arsenide. Boron nitride that can be used for the semiconductor layer preferably includes an amorphous structure. Boron arsenide that can be used for the semiconductor layer preferably includes a crystal with a cubic structure. Other examples of the compound semiconductor include an organic semiconductor and a nitride semiconductor. In addition, the oxide semiconductor as mentioned above is also one kind of the compound semiconductor. These semiconductor materials may contain an impurity as a dopant.
[0238] The semiconductor device of this embodiment may include a transistor containing a layered material functioning as a semiconductor in a channel formation region. Note that the details of the layered material will be described in Embodiment 6.
[Insulating Layer]
[0239] An inorganic insulating film is preferably used for each of the insulating layers (the insulating layer **180**, the insulating layer **111**, the insulating layer **160**, the insulating layer **121**, the insulating layer **185**, the insulating layer **186**, the insulating layer **280**, the insulating layer **281**, the insulating layer **250**, the insulating layer **225**, and the like) included in the semiconductor device. Examples of the inorganic insulating film include an oxide insulating film, a nitride insulating film, an oxynitride insulating film, and a nitride oxide insulating film. Examples of the oxide insulating film include a silicon oxide film, an aluminum oxide film, a magnesium oxide film, a gallium oxide film, a germanium oxide film, an yttrium oxide film, a zirconium oxide film, a lanthanum oxide film, a neodymium oxide film, a hafnium oxide film, a tantalum oxide film, a cerium oxide film, a gallium zinc oxide film, and a hafnium aluminate film. Examples of the nitride insulating film include a silicon nitride film and an aluminum nitride film. Examples of the oxynitride insulating film include a silicon oxynitride film, an aluminum oxynitride film, a gallium oxynitride film, an yttrium oxynitride film, and a hafnium oxynitride film. Examples of the nitride oxide insulating film include a silicon nitride oxide film and an aluminum nitride oxide film. An organic insulating film may be used for the insulating layer included in the semiconductor device.
[0240] With miniaturization and high integration of a transistor, for example, a problem such as generation of a leakage current may arise because of a thin gate insulating layer. When a material with a high relative permittivity (a high-k material) is used for the gate insulating layer, the voltage at the time of operation of the transistor can be reduced while the physical thickness is maintained. Furthermore, the equivalent oxide thickness (EOT) of the gate insulating layer can be reduced. By contrast, when a material with a low relative permittivity is used for the insulating layer functioning as an interlayer film, the parasitic capacitance generated between wirings can be reduced. Thus, a material is preferably selected depending on the function of an insulating layer. In addition, a material with a low relative permittivity is a material with high dielectric strength.
[0241] Examples of the material with a high relative permittivity include aluminum oxide, gallium oxide, hafnium oxide, tantalum oxide, zirconium oxide, hafnium zirconium oxide, an oxide containing aluminum and hafnium, an oxynitride containing aluminum and hafnium, an oxide containing silicon and hafnium, an oxynitride containing silicon and hafnium, and a nitride containing silicon and hafnium.
[0242] Examples of the material with a low relative permittivity include inorganic insulating materials such as silicon oxide, silicon oxynitride, and silicon nitride oxide, and resins such as polyester, polyolefin, polyamide (e.g., nylon and aramid), polyimide, polycarbonate, and an acrylic resin. Other examples of the inorganic insulating material with a low relative permittivity include

silicon oxide containing fluorine, silicon oxide containing carbon, and silicon oxide containing carbon and nitrogen. Another example is porous silicon oxide. Note that these silicon oxides can contain nitrogen.

[0243] A material that can have ferroelectricity may be used for the insulating layer included in the semiconductor device. Examples of the material that can have ferroelectricity include metal oxides such as hafnium oxide, zirconium oxide, and hafnium zirconium oxide. Examples of the material that can have ferroelectricity also include a material in which an element J**1** (the element J**1** here is one or more of zirconium, silicon, aluminum, gadolinium, yttrium, lanthanum, strontium, and the like) is added to hafnium oxide. Here, the atomic ratio of hafnium to the element J**1** can be set as appropriate; the atomic ratio of hafnium to the element J**1** can be, for example, 1:1 or the neighborhood thereof. Examples of the material that can have ferroelectricity also include a material in which an element J**2** (the element J**2** here is one or more of hafnium, silicon, aluminum, gadolinium, yttrium, lanthanum, strontium, and the like) is added to zirconium oxide. The atomic ratio of zirconium to the element J**2** can be set as appropriate; the atomic ratio of zirconium to the element J**2** can be, for example, 1:1 or the neighborhood thereof. As the material that can have ferroelectricity, a piezoelectric ceramic having a perovskite structure, such as lead titanate (PbTiOx), barium strontium titanate (BST), strontium titanate, lead zirconate titanate (PZT), strontium bismuth tantalate (SBT), bismuth ferrite (BFO), or barium titanate, may be used.

[0244] Examples of the material that can have ferroelectricity also include a metal nitride containing an element M**1**, an element M**2**, and nitrogen. Here, the element M**1** is one or more of aluminum, gallium, indium, and the like. The element M**2** is one or more of boron, scandium, yttrium, lanthanum, cerium, neodymium, europium, titanium, zirconium, hafnium, vanadium, niobium, tantalum, chromium, and the like. Note that the atomic ratio of the element M**1** to the element M**2** can be set as appropriate. A metal oxide containing the element M**1** and nitrogen has ferroelectricity in some cases even though the metal oxide does not contain the element M**2**. Examples of the material that can have ferroelectricity also include the above metal nitride to which an element M**3** is added. The element M**3** is one or more of magnesium, calcium, strontium, zinc, cadmium, and the like. Here, the atomic ratio between the element M**1**, the element M**2**, and the element M**3** can be set as appropriate.

[0245] Examples of the material that can have ferroelectricity also include perovskite-type oxynitrides such as SrTaO.sub.2N and BaTaO.sub.2N, and GaFeO.sub.3 with a κ-alumina-type structure.

[0246] The metal oxides and metal nitrides described above are non-limiting examples. For example, a metal oxynitride in which nitrogen is added to any of the above metal oxides, a metal nitride oxide in which oxygen is added to any of the above metal nitrides, or the like may be used.

[0247] As the material that can have ferroelectricity, a mixture or a compound each containing a plurality of materials selected from the above-listed materials can be used, for example. Alternatively, the insulating layer **121** to be described in Embodiment 3 can have a stacked-layer structure of a plurality of materials selected from the above-listed materials. Incidentally, since the above-listed materials and the like may change their crystal structures (characteristics) according to a variety of processes and the like as well as film formation conditions, a material that exhibits ferroelectricity is referred to not only as a ferroelectric but also as a material that can have ferroelectricity in this specification and the like.

[0248] A metal oxide containing one or both of hafnium and zirconium can have ferroelectricity even when being a thin film of several nanometers. A metal oxide containing one or both of hafnium and zirconium can have ferroelectricity even when having a minute area. Accordingly, the use of a metal oxide containing one or both of hafnium and zirconium enables miniaturization of the semiconductor device. Examples of the metal oxide containing one or both of hafnium and zirconium include hafnium oxide, zirconium oxide, and hafnium zirconium oxide. Typical examples of the hafnium zirconium oxide include HfZrO.sub.X (X is a real number greater than 0).

A metal oxide obtained by adding Y (yttrium) to HfZrO.sub.X (X is a real number greater than 0) can also be used. By adding Y (yttrium) to HfZrO.sub.X (X is a real number greater than 0), the ferroelectricity can be increased.

[0249] As described later, the metal oxide containing one or both of hafnium and zirconium can also be a material of an insulating layer having a function of capturing or fixing hydrogen. Thus, when a metal oxide containing one or both of hafnium and zirconium is used for at least part of the gate insulating layer, hydrogen contained in the oxide semiconductor layer can be captured or fixed, so that the hydrogen concentration in the oxide semiconductor layer can be reduced. Furthermore, the transistor including the gate insulating layer can function as a ferroelectric field effect transistor (FeFET).

[0250] Note that in this specification and the like, the material that can have ferroelectricity processed into a layered shape is referred to as a ferroelectric layer, a metal oxide film, or a metal nitride film in some cases. Furthermore, a device including such a ferroelectric layer, a metal oxide film, or a metal nitride film is sometimes referred to as a ferroelectric device in this specification and the like.

[0251] It is said that ferroelectricity is exhibited by displacement of oxygen or nitrogen of a crystal included in a ferroelectric layer due to an external electric field. Ferroelectricity is presumably exhibited depending on the crystal structure of a crystal included in a ferroelectric layer. Thus, in order that the insulating layer can exhibit ferroelectricity, the insulating layer **121** needs to include a crystal. In particular, the insulating layer preferably includes a crystal having an orthorhombic crystal structure, in which case ferroelectricity is exhibited. A crystal included in the insulating layer may have one or more of crystal structures selected from tetragonal, orthorhombic, monoclinic, and hexagonal crystal structures. Alternatively, the insulating layer may have an amorphous structure. In that case, the insulating layer may have a composite structure including an amorphous structure and a crystal structure.

[0252] Addition of a Group 3 element in the periodic table to an oxide containing one or both of hafnium and zirconium increases the oxygen vacancy concentration in the oxide and facilitates formation of a crystal having an orthorhombic crystal structure. This is preferable because the proportion of the crystal having an orthorhombic crystal structure is increased and the amount of remanent polarization can be increased. On the other hand, too much addition of the Group 3 element might decrease the crystallinity of the oxide and hinder the exhibition of ferroelectricity. Thus, the content percentage of the Group 3 element in the oxide containing one or both of hafnium and zirconium is preferably higher than or equal to 0.1 atomic % and lower than or equal to 10 atomic %, further preferably higher than or equal to 0.1 atomic % and lower than or equal to 5 atomic %, still further preferably higher than or equal to 0.1 atomic % and lower than or equal to 3 atomic %. Here, the content percentage of the Group 3 element refers to the proportion of the number of the Group 3 element atoms in the number of all metal element atoms contained in the layer. The Group 3 element is preferably one or more selected from scandium, lanthanum, and yttrium, further preferably one or both of lanthanum and yttrium.

[0253] Any of the materials with a high relative permittivity is preferably used for the insulating layer **121**. Using such a material with a high relative permittivity for the insulating layer **121** allows the insulating layer **121** to be thick enough to inhibit a leakage current and the capacitor **100** to have a sufficiently high capacitance.

[0254] It is preferable to use stacked insulating layers each including such a material with a high relative permittivity for the insulating layer **121**. A stacked-layer structure using a material with a high relative permittivity and a material having higher dielectric strength than the material with a high relative permittivity is preferably used. For example, as the insulating layer **121**, an insulating film in which zirconium oxide, aluminum oxide, and zirconium oxide are stacked in this order can be used. An insulating film in which zirconium oxide, aluminum oxide, zirconium oxide, and aluminum oxide are stacked in this order can be used, for example. For another example, an

insulating film in which hafnium zirconium oxide, aluminum oxide, hafnium zirconium oxide, and aluminum oxide are stacked in this order can be used. The stacking of such an insulating layer having relatively high dielectric strength, such as aluminum oxide, can increase the dielectric strength and inhibit electrostatic breakdown of the capacitor **100**.

[0255] Moreover, any of the above-described materials that can have ferroelectricity may be used for the insulating layer **121**.

[0256] A metal oxide containing one or both of hafnium and zirconium is preferable as the insulating layer **121** because the metal oxide can have ferroelectricity even when being a thin film of several nanometers as described above. The thickness of the insulating layer **121** is preferably less than or equal to 100 nm, further preferably less than or equal to 50 nm, still further preferably less than or equal to 20 nm, yet still further preferably less than or equal to 10 nm (typically greater than or equal to 2 nm and less than or equal to 9 nm). For example, the thickness of the insulating layer **121** is preferably greater than or equal to 8 nm and less than or equal to 12 nm. With the use of the ferroelectric layer that can have a small thickness, the capacitor **100** can be combined with a miniaturized semiconductor element such as a transistor to constitute parts of a semiconductor device.

[0257] A metal oxide containing one or both of hafnium and zirconium is preferable as the insulating layer **121** because the metal oxide can have ferroelectricity even with a minute area. For example, the metal oxide can exhibit ferroelectricity even with an area (occupied area) of a ferroelectric layer of less than or equal to 100 μm.sup.2, less than or equal to 10 μm.sup.2, less than or equal to 1 μm.sup.2, or less than or equal to 0.1 μm.sup.2 in a plan view. Furthermore, even with an area of less than or equal to 10000 nm.sup.2 or less than or equal to 1000 nm.sup.2, the metal oxide can have ferroelectricity in some cases. With a small-area ferroelectric layer, the area occupied by the capacitor **100** can be reduced.

[0258] The ferroelectric refers to an insulator having properties of causing internal polarization by application of an electric field from the outside and maintaining the polarization even after the electric field is made zero. Thus, with the use of a capacitor that includes this material as a dielectric (hereinafter, such a capacitor is sometimes referred to as a ferroelectric capacitor), a nonvolatile memory element can be formed. A nonvolatile memory element including a ferroelectric capacitor is sometimes referred to as a ferroelectric random access memory (FeRAM), a ferroelectric memory, or the like. For example, a ferroelectric memory includes a transistor and a ferroelectric capacitor, and one of a source and a drain of the transistor is connected to one terminal of the ferroelectric capacitor. Thus, in the case of using a ferroelectric capacitor as the capacitor **100**, the semiconductor device described in this embodiment functions as a ferroelectric memory.

[0259] A transistor including a metal oxide can have stable electrical characteristics when surrounded by an insulating layer having a function of inhibiting passage of impurities and oxygen. The insulating layer having a function of inhibiting passage of impurities and oxygen can have, for example, a single-layer structure or a stacked-layer structure of an insulating layer containing one or more of boron, carbon, nitrogen, oxygen, fluorine, magnesium, aluminum, silicon, phosphorus, chlorine, argon, gallium, germanium, yttrium, zirconium, lanthanum, neodymium, hafnium, and tantalum. Specifically, as a material for the insulating layer having a function of inhibiting passage of impurities and oxygen, a metal oxide such as aluminum oxide, magnesium oxide, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, or tantalum oxide, a metal nitride such as aluminum nitride or silicon nitride, a metal nitride oxide such as silicon nitride oxide can be used.

[0260] Specific examples of the material for the insulating layer having a function of inhibiting passage of oxygen and impurities such as water and hydrogen include a metal oxide such as aluminum oxide, magnesium oxide, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, tantalum oxide, and an oxide containing aluminum and hafnium (hafnium aluminate). Furthermore, nitrides such as aluminum

nitride, aluminum titanium nitride, and silicon nitride can be given, for example. Moreover, a metal nitride oxide such as silicon nitride oxide can be given.

[0261] An insulating layer in contact with an oxide semiconductor layer, such as a gate insulating layer, or an insulating layer provided in the vicinity of the oxide semiconductor layer preferably includes a region containing oxygen (hereinafter, sometimes referred to as excess oxygen) that is released by heating. For example, when an insulating layer including a region containing excess oxygen is in contact with an oxide semiconductor layer or positioned in the vicinity of the oxide semiconductor layer, oxygen vacancies in the oxide semiconductor layer can be reduced. Examples of a material for an insulating layer in which a region containing excess oxygen is easily formed include silicon oxide, silicon oxynitride, and porous silicon oxide.

[0262] As the insulating layer in contact with the oxide semiconductor layer or the insulating layer provided in the vicinity of the oxide semiconductor layer, a barrier insulating layer against hydrogen is preferably used. When the insulating layer has a barrier property against hydrogen, diffusion of hydrogen into the oxide semiconductor layer can be inhibited.

[0263] Examples of a material for an insulating layer having a function of capturing or fixing hydrogen include metal oxides such as an oxide containing hafnium, an oxide containing magnesium, an oxide containing aluminum, an oxide containing aluminum and hafnium (hafnium aluminate), and an oxide containing hafnium and silicon (hafnium silicate). Furthermore, these metal oxides may further contain zirconium, and an example of such a metal oxide is an oxide containing hafnium and zirconium.

[0264] The insulating layer having a function of capturing or fixing hydrogen preferably has an amorphous structure. In a metal oxide having an amorphous structure, some oxygen atoms have a dangling bond, which allows the metal oxide to have a high property of capturing or fixing hydrogen. Thus, when the insulating layer has an amorphous structure, the function of capturing or fixing hydrogen can be enhanced. For example, the amorphous structure of the metal oxide may be achieved by addition of silicon. For example, an oxide containing hafnium and silicon (hafnium silicate) is preferably used.

[0265] When the insulating layer has an amorphous structure, formation of a crystal grain boundary can be inhibited. Inhibiting formation of a crystal grain boundary can increase the planarity of the insulating layer. This enables the insulating layer to have uniform thickness distribution and the number of extremely thin portions to be reduced, so that the withstand voltage of the insulating layer can be increased. In addition, the thickness distribution of the film provided over the insulating layer can be uniform. Furthermore, inhibiting formation of a crystal grain boundary in the insulating layer can reduce a leakage current due to the defect states in the crystal grain boundary. Thus, the insulating layer can function as an insulating film with a low leakage current.

[0266] In addition, the insulating layer may partly include one or both of a crystal region and a crystal grain boundary.

[0267] A function of capturing or fixing a target substance can also be referred to as a property that does not easily allow diffusion of a target substance. Thus, a function of capturing or fixing a target substance can be rephrased as a barrier property.

[0268] In this specification and the like, a barrier insulating layer refers to an insulating layer having a barrier property. In addition, the barrier property refers to a property that does not easily allow diffusion of a target substance (also referred to as a property that does not easily allow passage of a target substance, a property with low permeability of a target substance, or a function of inhibiting diffusion of a target substance). In addition, hydrogen described as a target substance refers to at least one of a hydrogen atom, a hydrogen molecule, and a substance bonded to hydrogen, such as a water molecule or OH.sup.−, for example. Unless otherwise specified, an impurity described as a target substance refers to an impurity in a channel formation region or a semiconductor layer, and for example, refers to at least one of a hydrogen atom, a hydrogen molecule, a water molecule, a nitrogen atom, a nitrogen molecule, a nitrogen oxide molecule (e.g.,

N.sub.2O, NO, or NO.sub.2), a copper atom, and the like. Oxygen described as a target substance refers to, for example, at least one of an oxygen atom, an oxygen molecule, and the like.
[0269] Examples of a material for a barrier insulating layer against hydrogen include aluminum oxide, magnesium oxide, hafnium oxide, gallium oxide, silicon nitride, and silicon nitride oxide.
[0270] Examples of a material for a barrier insulating layer against oxygen include an oxide containing one or both of aluminum and hafnium, magnesium oxide, gallium oxide, gallium zinc oxide, silicon nitride, and silicon nitride oxide. Examples of the oxide containing one or both of aluminum and hafnium include aluminum oxide, hafnium oxide, an oxide containing aluminum and hafnium (hafnium aluminate), and an oxide containing hafnium and silicon (hafnium silicate).
[0271] The insulating layer **180**, the insulating layer **111**, the insulating layer **160**, the insulating layer **185**, and het insulating layer **186** each function as an interlayer film and thus is preferably formed using the above-described material with a low relative permittivity. In the case where a material with a low relative permittivity is used for an interlayer film, the parasitic capacitance generated between wirings can be reduced.
[0272] As the insulating layer **185**, a barrier insulating layer against hydrogen is preferably used. When the insulating layer **185** provided below the oxide semiconductor layer **230** has a barrier property against hydrogen, diffusion of hydrogen into the oxide semiconductor layer **230** from below the transistor **200** can be inhibited. For example, a silicon nitride film is preferably used as the insulating layer **185**.
[0273] The concentrations of impurities such as water and hydrogen in the insulating layers **185** and **186** are preferably reduced. This can inhibit entry of impurities such as water and hydrogen into the channel formation region of the oxide semiconductor layer **230**.
[0274] The insulating layer **280** functions as an interlayer film and thus is preferably formed using any of the above-described materials with a low relative permittivity. In the case where a material with a low relative permittivity is used for an interlayer film, the parasitic capacitance generated between wirings can be reduced. For example, silicon oxide or silicon oxynitride can be used for the insulating layer **280**.
[0275] The concentrations of impurities such as water and hydrogen in the insulating layer **280** are preferably reduced. This can inhibit entry of impurities such as water and hydrogen into the channel formation region of the oxide semiconductor layer **230**.
[0276] For example, the insulating layer including a region containing excess oxygen can be formed by a sputtering method in an oxygen-containing atmosphere. Since a molecule containing hydrogen is not used as a film formation gas in the sputtering method, the concentration of hydrogen in the insulating layer **280** can be reduced. When at least one layer in the insulating layer **280** is formed by a sputtering method in this manner, oxygen can be supplied from the insulating layer **280** to the channel formation region of the oxide semiconductor layer **230**, so that oxygen vacancies and V.sub.OH therein can be reduced.
[0277] In addition, since the thickness of the insulating layer **280** over the conductive layer **220***a* or the conductive layer **220***b* affects the channel length of the transistor **200**, the thickness of the insulating layer **280** is set as appropriate depending on the design value of the channel length of the transistor **200**.
[0278] For example, FIG. **3**A illustrates an example in which the insulating layer **280** has a single-layer structure. The insulating layer **280** can have a stacked-layer structure of two or more layers. FIG. **9**A illustrates an example in which the insulating layer **280** illustrated in FIG. **3**A has a three-layer structure of an insulating layer **280_1**, an insulating layer **280_2** over the insulating layer **280_1**, and an insulating layer **280_3** over the insulating layer **280_2**. In this case, it is preferable that the above-described material with a low relative permittivity be used as the insulating layer **2802** and barrier insulating layers against oxygen be used as the insulating layer **280_1** and the insulating layer **280_3**. Thus, the conductive layer **220** and the conductive layer **255** can be inhibited from being oxidized and having an increased resistance.

[0279] For example, it is preferable that a silicon nitride film or an aluminum oxide film be used as each of the insulating layer **280_1** and the insulating layer **280_3** and a silicon oxide film be used as the insulating layer **280_2**. Note that each of the insulating layer **280_1** and the insulating layer **280_3** may have a stacked-layer structure of two or more layers.
[0280] For the insulating layer **281**, an insulating material usable for the insulating layer **280** can be used. Incidentally, the insulating layer **160** may have a structure similar to the structure applicable to the insulating layer **280**.
[0281] For example, FIG. **3**A illustrates an example in which the insulating layer **281** has a single-layer structure. The insulating layer **281** can have a stacked-layer structure of two or more layers. For example, as illustrated in FIG. **9**A, the insulating layer **281** can have a three-layer structure of an insulating layer **281_1**, an insulating layer **281_2** over the insulating layer **281_1**, and an insulating layer **281_3** over the insulating layer **281_2**. In this case, it is preferable that any of the above-described materials with a low relative permittivity be used as the insulating layer **281_2** and barrier insulating layers against oxygen be used as the insulating layer **281_1** and the insulating layer **281_3**. Thus, the conductive layer **255** and the conductive layer **240** can be inhibited from being oxidized and having an increased resistance.
[0282] For example, it is preferable that a silicon nitride film or an aluminum oxide film be used as each of the insulating layers **281_1** and **281_3** and a silicon oxide film be used as the insulating layer **281_2**. Each of the insulating layer **281_1** and the insulating layer **281_3** may have a stacked-layer structure of two or more layers.
[0283] As the insulating layer **250**, a barrier insulating layer against hydrogen is preferably used. When the insulating layer **250** provided over the oxide semiconductor layer **230** has a barrier property against hydrogen, diffusion of hydrogen contained in the conductive layer **260** into the oxide semiconductor layer **230** can be inhibited. For example, a silicon nitride film is suitable as the insulating layer **250** because of its high barrier property against hydrogen.
[0284] Since the insulating layer **250** is in contact with the oxide semiconductor layer **230**, an insulating layer having a function of capturing or fixing hydrogen is preferably used as the insulating layer **250**. In this case, hydrogen contained in the oxide semiconductor layer **230** can be captured or fixed more effectively. Thus, the hydrogen concentration in the oxide semiconductor layer **230** (in particular, the hydrogen concentration in the channel formation region of the transistor) can be reduced. Accordingly, V.sub.OH in the channel formation region can be reduced, so that the channel formation region can be an i-type or substantially i-type region.
[0285] As the insulating layer **250**, an insulating layer including a region containing excess oxygen is preferably used. Accordingly, oxygen can be supplied from the insulating layer **250** to the oxide semiconductor layer **230**, so that oxygen vacancies in the oxide semiconductor layer **230** can be reduced. A silicon oxide film, a silicon oxynitride film, or the like has a thermally stable structure and thus is suitable for the insulating layer **250**.
[0286] FIG. **3**A illustrates an example where the insulating layer **250** has a single-layer structure. In addition, the insulating layer **250** may have a stacked-layer structure of two or more layers. In that case, the insulating layer **250** is preferably formed of two or more kinds of films. When the insulating layer **250** is formed of two or more kinds of films, the insulating layer **250** can have a plurality of functions. Examples of the functions of the insulating layer **250** include a function of extracting hydrogen from the oxide semiconductor layer **230** and a function of inhibiting diffusion of hydrogen into the oxide semiconductor layer **230**.
[0287] For example, the insulating layer **250** can have a two-layer structure of a first insulating layer and a second insulating layer over the first insulating layer. In this case, the first insulating layer is in contact with the oxide semiconductor layer **230**. For example, an insulating layer having a function of capturing or fixing hydrogen is preferably used as the first insulating layer, and a barrier insulating layer against hydrogen is preferably used as the second insulating layer. With such a structure, the hydrogen concentration in the oxide semiconductor layer **230** can be reduced

and diffusion of hydrogen into the oxide semiconductor layer **230** can be inhibited. Thus, the transistor can have high reliability. For example, a hafnium oxide film or a hafnium silicate film can be used as the first insulating layer, and a silicon nitride film can be used as the second insulating layer.

[0288] Alternatively, for example, an insulating layer including a region containing excess oxygen is preferably used as the first insulating layer, and a barrier insulating layer against hydrogen is preferably used as the second insulating layer. Alternatively, for example, an insulating layer including a region containing excess oxygen is preferably used as the first insulating layer, and an insulating layer having a function of capturing or fixing hydrogen is preferably used as the second insulating layer. With such a structure, the amount of oxygen vacancies and the hydrogen concentration in the oxide semiconductor layer **230** can be reduced, so that diffusion of hydrogen into the oxide semiconductor layer **230** can be inhibited. Thus, the transistor can have high reliability.

[0289] The insulating layer **250** can include a third insulating layer between the oxide semiconductor layer **230** and the first insulating layer, for example. In other words, the insulating layer **250** can have a three-layer structure of the third insulating layer, the first insulating layer over the third insulating layer, and the second insulating layer over the first insulating layer.

[0290] For example, an insulating layer including a region containing excess oxygen or an insulating layer containing a material with a low relative permittivity is preferably used as the third insulating layer, an insulating layer having a function of capturing or fixing hydrogen is preferably used as the first insulating layer, and an insulating layer having a barrier property against hydrogen and oxygen is preferably used as the second insulating layer. A silicon oxide film or a silicon oxynitride film is preferably used as the third insulating layer. When an oxide film is used as the third insulating layer in contact with the oxide semiconductor layer **230**, oxygen can be supplied to the oxide semiconductor layer **230**. Providing the second insulating layer can inhibit oxygen contained in the third insulating layer from diffusing into the conductive layer **260** and inhibit the conductive layer **260** from being oxidized. Furthermore, a reduction in the amount of oxygen supplied from the third insulating layer to the oxide semiconductor layer **230** can be inhibited.

[0291] The insulating layer **250** can include a fourth insulating layer between the oxide semiconductor layer **230** and the third insulating layer, for example. In other words, the insulating layer **250** can have a four-layer structure of the fourth insulating layer, the third insulating layer over the fourth insulating layer, the first insulating layer over the third insulating layer, and the second insulating layer over the first insulating layer.

[0292] As the fourth insulating layer, an insulating layer having a barrier property against oxygen is preferably used. Note that the first to third insulating layers can have a structure similar to that of the layers used in the above three-layer structure. The fourth insulating layer is in contact with the oxide semiconductor layer **230** and the conductive layer **240**. When the fourth insulating layer has a barrier property against oxygen, release of oxygen from the oxide semiconductor layer **230** can be inhibited. This inhibits formation of an oxide film on the side surface of the conductive layer **240** due to oxidization of the side surface. It is thus possible to inhibit a reduction in the on-state current or field-effect mobility of the transistor **200**.

[0293] As the fourth insulating layer, an aluminum oxide film is preferably used, for example. An aluminum oxide film has a function of capturing or fixing hydrogen, and thus is suitably used as the fourth insulating layer in contact with the oxide semiconductor layer **230**. Specifically, the insulating layer **250** preferably has a four-layer structure where an aluminum oxide film, a silicon oxide film, a hafnium oxide film, and a silicon nitride film are stacked in this order from the oxide semiconductor layer **230** side.

[0294] The insulating layer **250** is preferably thin. For example, when the insulating layer **250** has a thickness greater than or equal to 1 nm and less than or equal to 20 nm, preferably greater than or equal to 3 nm and less than or equal to 10 nm, the subthreshold swing value (also referred to as S

value), which is one of transistor characteristics, can be reduced. Note that the S value means the amount of change in gate voltage in a subthreshold region when a drain voltage is constant and a drain current is changed by one order of magnitude.

[0295] The thickness of each layer included in the insulating layer **250** is preferably greater than or equal to 0.1 nm and less than or equal to 10 nm, further preferably greater than or equal to 0.1 nm and less than or equal to 5 nm, further preferably greater than or equal to 0.5 nm and less than or equal to 5 nm, further preferably greater than or equal to 1 nm and less than 5 nm, further preferably greater than or equal to 1 nm and less than or equal to 3 nm. Additionally, each layer included in the insulating layer **250** at least partly preferably includes a region with the above-described thickness.

[0296] Typically, the thicknesses of the fourth insulating layer, the third insulating layer, the first insulating layer, and the second insulating layer are 1 nm, 2 nm, 2 nm, and 1 nm, respectively. Such a structure enables the transistor to have favorable electrical characteristics even when the transistor is miniaturized or highly integrated.

[0297] In addition, it is acceptable that the second insulating layer is not provided in the insulating layer **250** having the four-layer structure. For example, an insulating layer having a barrier property against oxygen can be used as the fourth insulating layer, an insulating layer including a material with a low relative permittivity can be used as the third insulating layer, and an insulating layer having a function of capturing or fixing hydrogen can be used as the first insulating layer. Specifically, it is possible to employ a three-layer structure where an aluminum oxide film, a silicon oxide film, and a hafnium oxide film are stacked in this order from the oxide semiconductor layer **230** side.

[0298] Moreover, in formation of the insulating layer **250** having a stacked-layer structure of a plurality of insulating films, an atomic layer deposition (ALD) process is preferably performed twice or more. For example, two or more kinds of the insulating films included in the insulating layer **250** are preferably formed through an ALD process. When at least two kinds of insulating films are formed through an ALD process, the coverage with the insulating layer **250** and the thickness uniformity of the insulating layer **250** can be improved. When two or more kinds of films, e.g., two or more kinds of insulating films are successively formed through an ALD process, the productivity can be increased.

[0299] The insulating layer **225** can be formed using an insulating material usable for the insulating layer **250**.

[0300] As described above, oxygen vacancies and impurities are preferably reduced as much as possible in the channel formation region of the oxide semiconductor layer. It is particularly preferable that hydrogen be reduced as much as possible in the channel formation region of the oxide semiconductor layer.

[0301] In view of this, a barrier insulating layer against hydrogen is preferably used as the insulating layer **225** provided outside the oxide semiconductor layer **230**. Accordingly, diffusion of hydrogen into the oxide semiconductor layer **230** can be inhibited, and the reliability of the transistor **200** can be improved. For example, as the insulating layer **225**, a silicon nitride film, a silicon nitride oxide film, or an aluminum oxide film is preferably used, and a silicon nitride film is further preferably used.

[0302] Note that a silicon nitride film also has a barrier property against oxygen. Thus, using a silicon nitride film as the insulating layer **225** can inhibit extraction of oxygen from the oxide semiconductor layer **230**, and accordingly can inhibit formation of oxygen vacancies in the oxide semiconductor layer **230**. Furthermore, when a silicon nitride film is used as the insulating layer **225**, excess oxygen can be prevented from being supplied to the oxide semiconductor layer **230**. Thus, the channel formation region of the oxide semiconductor layer **230** can be prevented from containing excess oxygen, whereby the reliability of the transistor **200** can be improved. The insulating layer **225** is in contact with the side surface of the conductive layer **240***a* and the side

surface of the conductive layer **240***b* in the opening portion **290** in some cases. In this case, the use of a silicon nitride film as the insulating layer **225** can inhibit oxidation of the side surface of the conductive layer **240***a* and the side surface of the conductive layer **240***b* in the opening portion **290** and formation of oxide films on the side surfaces. It is thus possible to inhibit a reduction in the on-state current or the field-effect mobility of the transistor **200**.

[0303] A silicon nitride film included in the insulating layer **225** is preferably formed by a plasma-enhanced ALD (PEALD). This can improve the coverage of the sidewall of the opening portion **290** with the insulating layer **225**, so that the insulating layer **225** with a uniform thickness can be formed.

[0304] For the insulating layer **225**, any of the above-described materials that can have ferroelectricity can also be used.

[0305] For example, FIG. **3**A illustrates an example in which the insulating layer **225** has a single-layer structure. The insulating layer **225** can have a stacked-layer structure of two or more layers. FIG. **9**B illustrates an example in which the insulating layer **225** has a two-layer structure of an insulating layer **225_1** and an insulating layer **225_2**.

[0306] FIG. **9**B illustrates an example in which the insulating layer **225** includes two layers of the insulating layer **2251** and the insulating layer **225_2**; the insulating layer **225_1** is in contact with the conductive layer **220**, the insulating layer **280**, the conductive layer **255**, the insulating layer **281**, and the conductive layer **240**; and the insulating layer **225_2** is positioned between the insulating layer **225_1** and the oxide semiconductor layer **230**. The insulating layer **225** illustrated in FIG. **9**B has a two-layer structure of the insulating layer **225_1** and the insulating layer **225_2** over the insulating layer **225_1**.

[0307] The insulating layer **225_1** provided in contact with the side surface of the insulating layer **280** in the opening portion **290** is preferably formed using a barrier insulating layer against hydrogen, and the insulating layer **225_2** provided in contact with the oxide semiconductor layer **230** is preferably formed using an insulating layer having a function of capturing or fixing hydrogen. This structure enables the hydrogen concentration in the oxide semiconductor layer **230** to be reduced. Accordingly, the electrical characteristics and reliability of the transistor can be improved. For example, it is preferable that a silicon nitride film be used as the insulating layer **225_1** and a hafnium oxide film, a hafnium silicate film, or an aluminum oxide film be used as the insulating layer **225_2**. Here, the insulating layer **225_1** contains silicon and nitrogen, and the insulating layer **2252** contains oxygen and one or both of hafnium and aluminum.

[0308] The insulating layer **225_1** can be formed using a barrier insulating layer against hydrogen, and the insulating layer **225_2** can be formed using an insulating layer including a region containing excess oxygen. This structure enables one or both of oxygen vacancies and hydrogen in the oxide semiconductor layer **230** to be reduced. Accordingly, the electrical characteristics and reliability of the transistor can be improved. For example, it is preferable that a silicon nitride film be used as the insulating layer **225_1** and a silicon oxide film, a silicon oxynitride film, or an aluminum oxide film be used as the insulating layer **225_2**. Here, the insulating layer **225_1** contains silicon and nitrogen, and the insulating layer **225_2** contains oxygen and one or both of silicon and aluminum. In particular, when a silicon oxide film is used as the insulating layer **225_2**, the insulating layer **2252** contains silicon and oxygen.

[0309] Typically, a silicon nitride film and a silicon oxide film can be used as the insulating layer **225_1** and the insulating layer **225_2**, respectively. The thicknesses of the insulating layer **225_1** and the insulating layer **225_2** are each 2 nm.

[0310] As described above, the barrier insulating layer against hydrogen encloses the periphery of the oxide semiconductor layer **230** in a ring shape, and an insulating layer having a function of capturing or fixing hydrogen or an insulating layer including a region containing excess oxygen is provided in the vicinity of the oxide semiconductor layer **230**, in which case one or both of oxygen vacancies and impurities in the oxide semiconductor layer **230** can be reduced. Accordingly, the

electrical characteristics and reliability of the transistors can be improved.
[0311] Here, another structure example of the insulating layer **225** illustrated in FIG. **9**B is illustrated in FIGS. **10**A and **10**B. FIG. **10**A illustrates an example in which the bottom surface of the insulating layer **2252** includes a region in contact with the bottom portion of the depressed portion **221***a*, a region in contact with the bottom portion of the depressed portion **221***b*, and a region in contact with the bottom portion of the depressed portion **222**.
[0312] In the example illustrated in FIG. **10**B, the conductive layer **220***a***2** and the conductive layer **220***b***2** each include a first depressed portion and a second depressed portion positioned outside the first depressed portion. In the example illustrated in FIG. **10**B, the insulating layer **186** includes a third depressed portion and a fourth depressed portion positioned outside the third depressed portion. The depth of the first depressed portion is greater than that of the second depressed portion, and the depth of the third depressed portion is greater than that of the fourth depressed portion. In the formation of the opening portion **290**, the second depressed portion is provided in the conductive layer **220***a***2** and the conductive layer **220***b***2**, and the fourth depressed portion is provided in the insulating layer **186**. After that, at the time of processing the insulating layer **225_1**, the first depressed portion is provided in the conductive layer **220***a***2** and the conductive layer **220***b***2**, and the third depressed portion is provided in the insulating layer **186**.
[0313] In the example illustrated in FIG. **10**B, the insulating layer **225_1** is provided in contact with the bottom portion and the sidewall of the second depressed portion and the bottom portion and the sidewall of the fourth depressed portion. The insulating layer **225_2** is provided in contact with the bottom portion and the sidewall of the first depressed portion and the bottom portion and the sidewall of the third depressed portion.
[0314] For example, the insulating layer **225_1** is formed in contact with the sidewall of the opening portion **290**, the side surface of the conductive layer **220***a*, and the side surface of the conductive layer **220***b*. After that, an insulating film to be the insulating layer **2252** is formed and processed, so that the insulating layer **225** having the structure illustrated in FIG. **10**A or **10**B can be formed. The contact area between the insulating layer **225_1** and the oxide semiconductor layer **230** can be reduced, compared with the transistor **200** illustrated in FIG. **9**B, and thus the insulating layer **225_2** can be in contact with the oxide semiconductor layer **230**.
[0315] The insulating layer **225** can have a three-layer structure of a first insulating layer, a second insulating layer, and a third insulating layer. For example, it is preferable that one of the first to third insulating layers be formed using a barrier insulating layer against hydrogen, another be formed using an insulating layer having a function of capturing or fixing hydrogen, and the other be formed using an insulating layer including a region containing excess oxygen. This structure enables the electrical characteristics and reliability of the transistor to be improved.
[0316] Moreover, the insulating layer **225** can have a four-layer structure of the first insulating layer, the second insulating layer, the third insulating layer, and a fourth insulating layer. For example, it is preferable that one of the first to fourth insulating layers be formed using a barrier insulating layer against hydrogen, another be formed using an insulating layer having a function of capturing or fixing hydrogen, another be formed using an insulating layer including a region containing excess oxygen, and the other be formed using an insulating layer having a barrier property against oxygen. This structure can inhibit a reduction in the amount of on-state current or a reduction in the field-effect mobility of the transistor **200**.
[0317] For the stacked-layer structure of the first to fourth insulating layers in the insulating layer **225**, the stacked-layer structure of the first to fourth insulating layers in the insulating layer **250** can be referred to. In addition, the stacking order in the insulating layer **225** is preferably reverse from the stacking order in the insulating layer **250**. For example, in the case where the insulating layer **225** has a three-layer structure, the insulating layer **225** can have a three-layer structure of the second insulating layer in contact with the conductive layer **255**, the first insulating layer over the second insulating layer, and the third insulating layer over the first insulating layer. In this case, the

third insulating layer is in contact with the oxide semiconductor layer **230**.

[Conductive Layer]

[0318] For each of the conductive layers (the conductive layers **110**, **115**, **120**, **161**, **220**, **240**, **255**, **260**, and the like) included in the semiconductor device, it is preferable to use a metal element selected from aluminum, chromium, copper, silver, gold, platinum, zinc, tantalum, nickel, titanium, iron, cobalt, molybdenum, tungsten, hafnium, vanadium, niobium, manganese, magnesium, zirconium, beryllium, indium, ruthenium, iridium, strontium, lanthanum, and the like; an alloy containing any of the above metal elements; an alloy containing a combination of the above metal elements; or the like. As an alloy containing any of the above metal elements, a nitride of the alloy or an oxide of the alloy may be used. For example, tantalum nitride, titanium nitride, tungsten, a nitride containing titanium and aluminum, a nitride containing tantalum and aluminum, ruthenium oxide, ruthenium nitride, an oxide containing strontium and ruthenium, an oxide containing lanthanum and nickel, or the like is preferably used. A semiconductor having high electrical conductivity, typified by polycrystalline silicon containing an impurity element such as phosphorus, or silicide such as nickel silicide may be used.

[0319] A conductive material containing nitrogen, such as a nitride containing tantalum, a nitride containing titanium, a nitride containing molybdenum, a nitride containing tungsten, a nitride containing ruthenium, a nitride containing tantalum and aluminum, or a nitride containing titanium and aluminum; a conductive material containing oxygen, such as ruthenium oxide, an oxide containing strontium and ruthenium, or an oxide containing lanthanum and nickel; or a material containing a metal element such as titanium, tantalum, or ruthenium is preferable because it is a conductive material that is not easily oxidized, a conductive material having a function of inhibiting oxygen diffusion, or a material maintaining its conductivity even after absorbing oxygen. Examples of the conductive material containing oxygen include indium oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide (also referred to as In—Sn oxide or ITO), indium tin oxide containing titanium oxide, indium tin oxide containing silicon (also referred to as ITSO), indium zinc oxide (also referred to as In—Zn oxide or IZO (a registered trademark)), and indium zinc oxide containing tungsten oxide. In this specification and the like, a conductive film formed using the conductive material containing oxygen may be referred to as an oxide conductive film.

[0320] A conductive material containing tungsten, copper, or aluminum as its main component is preferable because it has high conductivity.

[0321] A plurality of conductive layers formed using any of the above materials may be stacked. For example, a stacked-layer structure combining a material containing any of the above metal elements and a conductive material containing oxygen may be employed. Alternatively, a stacked-layer structure combining a material containing any of the above metal elements and a conductive material containing nitrogen may be employed. Further alternatively, a stacked-layer structure combining a material containing any of the above metal elements, a conductive material containing oxygen, and a conductive material containing nitrogen may be employed.

[0322] In the case where a metal oxide is used for the channel formation region of the transistor, the conductive layer functioning as the gate electrode preferably employs a stacked-layer structure combining a material containing any of the above metal elements and a conductive material containing oxygen. In that case, the conductive material containing oxygen is preferably provided on the channel formation region side. When the conductive material containing oxygen is provided on the channel formation region side, oxygen released from the conductive material is easily supplied to the channel formation region.

[0323] For example, a conductive material with high conductivity such as tungsten can be used for the conductive layer **110**. With the use of a conductive material with high conductivity, the conductive layer **110** can have an improved conductivity and functions well as the wiring CAL.

[0324] For the conductive layer **115**, a single layer or stacked layers of a conductive material that is

less likely to be oxidized, a conductive material having a function of inhibiting diffusion of oxygen, or the like is preferably used. For example, titanium nitride, ITSO, or the like may be used. Alternatively, a structure in which titanium nitride is stacked over tungsten may be used, for example. Alternatively, for example, a structure in which tungsten is stacked over first titanium nitride and second titanium nitride is stacked over the tungsten may be used. This structure can inhibit the conductive layer **115** from being oxidized by the insulating layer **121** when an oxide is used for the insulating layer **121**. This structure can also inhibit the conductive layer **115** from being oxidized by the insulating layer **160** when an oxide is used for the insulating layer **160**.

[0325] Each of the conductive layers **220** and **240** is in contact with the oxide semiconductor layer **230**. Thus, each of the conductive layers **220** and **240** is preferably formed using a conductive material that is not easily oxidized, a conductive material that maintains its low electric resistance even after being oxidized, a metal oxide that has conductivity (also referred to as an oxide conductor), or a conductive material that has a function of inhibiting diffusion of oxygen. Examples of the conductive material include a conductive material containing nitrogen and a conductive material containing oxygen. Thus, a decrease in conductivity of each of the conductive layers **220** and **240** can be inhibited.

[0326] When a conductive material containing oxygen is used for the conductive layer **220**, the conductive layer **220** can maintain its conductivity even when after absorbing oxygen. Similarly, when a conductive material containing oxygen is used for the conductive layer **240**, the conductive layer **240** can maintain its conductivity even after absorbing oxygen. For each of the conductive layers **220** and **240**, ITO, ITSO, In—Zn oxide, or the like is preferably used, for example.

[0327] In the case where the conductive layer **220** and the conductive layer **240** each have a stacked-layer structure, a conductive material containing oxygen is preferably used for a layer having the largest contact area with the oxide semiconductor layer **230** in the stacked-layer structure, in which case the contact resistance between the conductive layer **220** and the oxide semiconductor layer **230** and the contact resistance between the conductive layer **240** and the oxide semiconductor layer **230** can be reduced.

[0328] For example, the conductive layer **220***a* illustrated in FIG. **3**A has a two-layer structure of the conductive layer **220***a***1** and the conductive layer **220***a***2** over the conductive layer **220***a***1**. Similarly, the conductive layer **220***b* has a two-layer structure of the conductive layer **220***b***1** and the conductive layer **220***b***2** over the conductive layer **220***b***1**. In this case, for the conductive layers **220***a***2** and **220***b***2**, a conductive material that is less likely to be oxidized, a conductive material that maintains low electric resistance even when oxidized, a conductive metal oxide, or a conductive material having a function of inhibiting diffusion of oxygen is preferably used. For the conductive layer **220***a***2** and the conductive layer **220***b***2**, a conductive material containing oxygen is preferably used, for example. A material having conductivity higher than those for the conductive layer **220***a***2** and the conductive layer **220***b***2** is preferably used for each of the conductive layer **220***a***1** and the conductive layer **220***b***1**. Specifically, it is preferable that an oxide conductor (e.g., ITO, ITSO, or In—Zn oxide) be used for the conductive layer **220***a***2** and the conductive layer **220***b***2** and tungsten be used for the conductive layer **220***a***1** and the conductive layer **220***b***1**. For the conductive layer **220***a***1** and the conductive layer **220***b***1**, ruthenium, titanium nitride, tantalum nitride, or the like may be used. When an oxide conductor is used as the conductive layer **220***a***2** mainly in contact with the oxide semiconductor layer **230***a*, the contact resistance with the oxide semiconductor layer **230***a* can be reduced. Similarly, when an oxide conductor is used as the conductive layer **220***b***2** mainly in contact with the oxide semiconductor layer **230***b*, the contact resistance with the oxide semiconductor layer **230***b* can be reduced. When a material having higher conductivity than an oxide conductor is used for the layer included in the conductive layer **220***a* and the layer included in the conductive layer **220***b*, the conductivity of the conductive layer **220***a* and the conductive layer **220***b* can be increased.

[0329] For example, FIG. **3**A illustrates an example in which the conductive layer **220***a***1**, the

conductive layer **220***b***1**, the conductive layer **220***a***2**, and the conductive layer **220***b***2** each have a single-layer structure. Note that one or both of the conductive layers **220***a***1** and **220***a***2** may have a stacked-layer structure of two or more layers. Similarly, one or both of the conductive layers **220***b***1** and **220***b***2** may have a stacked-layer structure of two or more layers. FIG. **11**A illustrates an example in which the conductive layer **220***a***1** has a two-layer structure of a conductive layer **220***a***11** and a conductive layer **220***a***12** over the conductive layer **220***a***11** and the conductive layer **220***b***1** has a two-layer structure of a conductive layer **220***b***11** and a conductive layer **220***b***12** over the conductive layer **220***b***11**. In this case, the conductive layer **220***a* has a three-layer structure of the conductive layer **220***a***11**, the conductive layer **220***a***12** over the conductive layer **220***a***11**, and the conductive layer **220***a***2** over the conductive layer **220***a***12**. Similarly, the conductive layer **220***b* has a three-layer structure of the conductive layer **220***b***11**, the conductive layer **220***b***12** over the conductive layer **220***b***11**, and the conductive layer **220***b***2** over the conductive layer **220***b***12**.

[0330] For example, a conductive material that is less likely to be oxidized or a conductive material having a function of inhibiting diffusion of oxygen is preferably used for the conductive layers **220***a***11** and **220***b***11**. A material having high conductivity is preferably used for the conductive layers **220***a***12** and **220***b***12**. Moreover, a conductive material containing oxygen (preferably, an oxide conductor) is preferably used for the conductive layers **220***a***2** and **220***b***2**. Specifically, titanium nitride is preferably used for the conductive layers **220***a***11** and **220***b***11**, tungsten is preferably used for the conductive layers **220***a***12** and **220***b***12**, and an oxide conductor (e.g., ITO, ITSO, or In—Zn oxide) is preferably used for the conductive layers **220***a***2** and **220***b***2**. In this case, the titanium nitride film is in contact with one or both of the insulating layer **185** and the insulating layer **186**, and the oxide conductive film is in contact with the oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b*, for example. In addition, an oxide conductor is used for a layer closest to the channel formation region of the oxide semiconductor layer **230***a* and a layer closest to the channel formation region of the oxide semiconductor layer **230***b*. Since the oxide conductor has a lower contact resistance with the oxide semiconductor layer **230***a* than tungsten, the current path between the source and the drain can be shortened and the on-state currents of the transistors **200***a* and **200***b* can be increased. Such a structure enables the conductivity to be maintained even when the conductor layer **220***a* is in contact with the oxide semiconductor layer **230***a* and the conductive layer **220***b* is in contact with the oxide semiconductor layer **230***b*. When a metal material (here, tungsten) having higher conductivity than the oxide conductor and titanium nitride is used for the conductive layers **220***a***12** and **220***b***12**, the conductivities of the conductive layers **220***a* and **220***b* can be increased.

[0331] For example, the conductive layer **240***a* illustrated in FIG. **3**A has a two-layer structure of the conductive layer **240***a***1** and the conductive layer **240***a***2** over the conductive layer **240***a***1**. Similarly, for example, the conductive layer **240***b* illustrated in FIG. **3**A has a two-layer structure of the conductive layer **240***b***1** and the conductive layer **240***b***2** over the conductive layer **240***b***1**. In this case, a conductive material containing oxygen is preferably used for the conductive layers **240***a***2** and **240***b***2**, for example. For the conductive layers **240***a***1** and **240***b***1**, a material having higher conductivity than the material for the conductive layers **240***a***2** and **240***b***2** is preferably used. Specifically, it is preferable that an oxide conductor (e.g., ITO, ITSO, or In—Zn oxide) be used for the conductive layers **240***a***2** and **240***b***2** and tungsten be used for the conductive layers **240***a***1** and **240***b***1**. For the conductive layers **240***a***1** and **240***b***1**, ruthenium, titanium nitride, tantalum nitride, or the like may be used. When an oxide conductor is used for the conductive layer **240***a***2** mainly in contact with the oxide semiconductor layer **230***a*, the contact resistance with the oxide semiconductor layer **230***a* can be reduced. Similarly, when an oxide conductor is used for the conductive layer **240***b***2** mainly in contact with the oxide semiconductor layer **230***b*, the contact resistance with the oxide semiconductor layer **230***b* can be reduced. When a material having higher conductivity than the oxide conductor is used for a layer included in the conductive layer **240***a* and a layer included in the conductive layer **240***b*, the conductivities of the conductive layers **240***a* and

240*b* can be increased.
[0332] In addition, a conductive material containing oxygen can be used for the conductive layers **240***a***1** and **240***b***1**, and a material having higher conductivity than the material for the conductive layers **240***a***1** and **240***b***1** can be used for the conductive layers **240***a***2** and **240***b***2**. In this case, the material having higher conductivity is used for the layers of the conductive layers **240***a* and **240***b* which are closest to the channel formation regions of the oxide semiconductor layers **230***a* and **230***b*. Thus, the current path between the source and the drain can be shortened, so that the on-state currents of the transistors **200***a* and **200***b* can be increased.
[0333] The conductive layer **255** includes a region functioning as one of the wiring WOL and the wiring BGL. The conductive layer **255** is preferably formed using a material having high conductivity such as tungsten. For the conductive layer **255**, a conductive material that is not easily oxidized, a conductive material having a function of inhibiting diffusion of oxygen, or the like is preferably used. As described above, examples of the conductive material include a conductive material containing nitrogen (e.g., titanium nitride or tantalum nitride) and a conductive material containing oxygen (e.g., ruthenium oxide). Thus, a decrease in conductivity of the conductive layer **255** can be inhibited.
[0334] It is preferable to use, for the conductive layer **255**, a conductive material containing oxygen and a metal element contained in the metal oxide where a channel is formed. Alternatively, a conductive material containing the above metal element and nitrogen (e.g., titanium nitride or tantalum nitride) may be used. One or more of ITO, indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, In—Zn oxide, and ITSO may be used. Indium gallium zinc oxide containing nitrogen may also be used. With the use of such a material, hydrogen contained in the metal oxide where a channel is formed can be captured in some cases. Hydrogen entering from a surrounding insulating layer or the like can also be captured in some cases.
[0335] FIG. **3**A illustrates an example where the conductive layer **255** has a single-layer structure, for example. The conductive layer **255** can have a stacked-layer structure of two or more layers.
[0336] As described above, the channel lengths of the transistor **200***a* and the transistor **200***b* can be determined by the thickness or the like of the conductive layer **255**. Thus, the conductive layer **255** has a thickness corresponding to a desired channel length. The thickness of the conductive layer **255** can be, for example, greater than or equal to 2 nm and less than or equal to 50 nm, greater than or equal to 3 nm and less than or equal to 30 nm, greater than or equal to 4 nm and less than or equal to 20 nm, or greater than or equal to 5 nm and less than or equal to 15 nm.
[0337] For the conductive layer **260**, a conductive material usable for the conductive layer **255** can be used.
[0338] FIG. **3**A illustrates an example where the conductive layer **260** has a single-layer structure, for example. In addition, the conductive layer **260** can have a stacked-layer structure of two or more layers. FIG. **11**B illustrates an example in which the conductive layer **260** illustrated in FIG. **3**A has a two-layer structure of a conductive layer **260_1** and a conductive layer **260_2** over the conductive layer **260_1**. In this case, in a preferable example, a titanium nitride film is preferably used as the conductive layer **260_1**, and a tungsten film is preferably used as the conductive layer **260_2**. In another preferable example, a tantalum nitride film is preferably used as the conductive layer **260_1**, and a copper film is preferably used as the conductive layer **2602**. Such a structure can increase the conductivity of the conductive layer **260**.
[0339] Alternatively, the conductive layer **260** may have a stacked-layer structure of three or more layers. The conductive layer **260** may have a three-layer structure of a tantalum nitride film, a titanium nitride film over the tantalum nitride film, and a tungsten film over the titanium nitride film, for example.
[Substrate]
[0340] As a substrate where a semiconductor device is formed, an insulator substrate, a

semiconductor substrate, or a conductor substrate can be used, for example. Examples of the insulator substrate include a glass substrate, a quartz substrate, a sapphire substrate, a stabilized zirconia substrate (e.g., an yttria-stabilized zirconia substrate), and a resin substrate. Examples of the semiconductor substrate include a semiconductor substrate of silicon or germanium and a compound semiconductor substrate of silicon carbide, silicon germanium, gallium arsenide, indium phosphide, zinc oxide, or gallium oxide. Other examples include any of the above semiconductor substrates including an insulator region, e.g., a silicon on insulator (SOI) substrate. Examples of the conductor substrate include a graphite substrate, a metal substrate, an alloy substrate, and a conductive resin substrate. Other examples include a substrate containing a nitride of a metal and a substrate containing an oxide of a metal. An insulator substrate provided with a conductor or a semiconductor, a semiconductor substrate provided with a conductor or an insulator, a conductor substrate provided with a semiconductor or an insulator, or the like is also given. Alternatively, these substrates provided with elements may be used. Examples of the element provided for the substrate include a capacitor, a resistor, a switching element, a light-emitting element, and a memory element.

[0341] The above is the description of materials that can be used for the semiconductor device of this embodiment.

[0342] The semiconductor device of one embodiment of the present invention may include an insulating layer over the transistor **200**. Specifically, an insulating layer may be provided over the conductive layer **260** and the insulating layer **250**.

[0343] As the insulating layer, a barrier insulating layer against hydrogen is preferably used. Such a structure can inhibit diffusion of hydrogen from above the transistor **200** into the oxide semiconductor layer **230**.

[0344] Although FIG. **3**A illustrates a structure where the side surface of the conductive layer **240** in the opening portion **290** and the side surface of the insulating layer **280** in the opening portion **290** are aligned or substantially aligned with each other, the present invention is not limited to the structure. For example, the side surface of the conductive layer **240** in the opening portion **290** and the side surface of the insulating layer **280** in the opening portion **290** may be discontinuous. The inclination of the side surface of the conductive layer **240** in the opening portion **290** and the inclination of the side surface of the insulating layer **280** in the opening portion **290** may be different from each other. At this time, part of the sidewall of the opening portion **290** has a tapered shape.

[0345] FIGS. **12**A and **12**B each illustrate an example where at least part of the sidewall of the opening portion **290** has a tapered shape. FIG. **12**A illustrates an example where the side surfaces of the conductive layer **240***a* and the conductive layer **240***b* in the opening portion **290** each have a tapered shape, and FIG. **12**B illustrates an example where the side surfaces of the conductive layer **240***a*, the conductive layer **240***b*, the insulating layer **281**, the conductive layer **255**, and the insulating layer **280** in the opening portion **290** each have a tapered shape.

[0346] When the sidewall of the opening portion **290** has a tapered shape, the coverage with the insulating layer **225**, the oxide semiconductor layer **230***a*, the oxide semiconductor layer **230***b*, the insulating layer **250**, and the like can be improved, so that defects such as voids can be reduced. In the case where the sidewall of the opening portion **290** has a tapered shape, for example, a taper angle (an angle θ**240**) of the side surface of the conductive layer **240***a* in the opening portion **290**, a taper angle of the side surface of the conductive layer **240***b* in the opening portion **290**, and a taper angle (an angle θ**281**) of the side surface of the insulating layer **281** in the opening portion **290** are each preferably greater than or equal to 45° and less than 90°. Specifically, the taper angles are preferably greater than or equal to 80° and less than 90°, in which case the semiconductor device can be miniaturized or highly integrated as described above. Moreover, the taper angles are preferably greater than or equal to 45° or greater than or equal to 50° and less than 80°, less than or equal to 75°, less than or equal to 70°, less than or equal to 65°, or less than or equal to 60°, in

which case the coverage with a film to be formed in the opening portion **290** is improved.
[0347] For example, the angle θ**240** is preferably smaller than the angle θ**281**. With such a structure, the coverage of the side surface of the conductive layer **240***a* in the opening portion **290** with the insulating layer **225**, the oxide semiconductor layer **230***a*, and the like is improved, so that defects such as voids can be reduced. In the case where the insulating layer **280** has a stacked-layer structure, the inclinations of the side surfaces of the layers in the opening portion **290** may be different from each other. Similarly, in the case where the conductive layers **240***a* and **240***b* have a stacked-layer structure, the inclinations of the side surfaces of the layers in the opening portion **290** may be different from each other.
[0348] As described above, the oxide semiconductor layer **230** can have a stacked-layer structure of two or more layers.
[0349] FIG. **13**A illustrates an example in which the oxide semiconductor layer **230** included in the semiconductor device illustrated in FIG. **9**B has a two-layer structure. The oxide semiconductor layer **230***a* illustrated in FIG. **13**A can have a two-layer structure of an oxide semiconductor layer **230***a***1** and an oxide semiconductor layer **230***a***2** over the oxide semiconductor layer **230***a***1**. Similarly, the oxide semiconductor layer **230***b* illustrated in FIG. **13**A can have a two-layer structure of an oxide semiconductor layer **230***b***1** and an oxide semiconductor layer **230***b***2** over the oxide semiconductor layer **230***b***1**.
[0350] FIG. **13**B illustrates an example in which the oxide semiconductor layer **230** included in the semiconductor device illustrated in FIG. **9**B has a three-layer structure. The oxide semiconductor layer **230***a* illustrated in FIG. **13**B can have a three-layer structure of the oxide semiconductor layer **230***a***1**, the oxide semiconductor layer **230***a***2** over the oxide semiconductor layer **230***a***1**, and an oxide semiconductor layer **230***a***3** over the oxide semiconductor layer **230***a***2**. Similarly, the oxide semiconductor layer **230***b* illustrated in FIG. **13**B can have a three-layer structure of the oxide semiconductor layer **230***b***1**, the oxide semiconductor layer **230***b***2** over the oxide semiconductor layer **230***b***1**, and an oxide semiconductor layer **230***b***3** over the oxide semiconductor layer **230***b***2**.
[0351] Note that the boundary (or the interface) between the oxide semiconductor layer **230***a***1** and the oxide semiconductor layer **230***a***2** and the boundary (or the interface) between the oxide semiconductor layer **230***a***2** and the oxide semiconductor layer **230***a***3** cannot be clearly observed in some cases. Similarly, the boundary (or the interface) between the oxide semiconductor layer **230***b***1** and the oxide semiconductor layer **230***b***2** and the boundary (or the interface) between the oxide semiconductor layer **230***b***2** and the oxide semiconductor layer **230***b***3** cannot be clearly observed in some cases. Thus, the boundaries are denoted by dashed lines in FIG. **13**A and FIG. **13**B.
[0352] For the oxide semiconductor layers usable for the oxide semiconductor layers **230***a***1** to **230***a***3** and the oxide semiconductor layers **230***b***1** to **230***b***3**, the description in Embodiment 2 can be referred to.
[0353] For example, FIG. **3**A illustrates a structure in which the end portion of the oxide semiconductor layer **230***a* in the opening portion **290** is positioned inward from the end portion of the conductive layer **220***a* on the opening portion **290** side (the end portion of the oxide semiconductor layer **230***a* in the opening portion **290** is positioned closer to the side surface of the conductive layer **220***b* in the opening portion **290** than the end portion of the conductive layer **220***a* on the opening portion **290** side is). FIG. **3**A also illustrates an example in which the end portion of the oxide semiconductor layer **230***b* in the opening portion **290** is positioned inward from the end portion of the conductive layer **220***b* on the opening portion **290** side (the end portion of the oxide semiconductor layer **230***b* in the opening portion **290** is positioned closer to the side surface of the conductive layer **220***a* in the opening portion **290** than the end portion of the conductive layer **220***b* on the opening portion **290** side is). In the opening portion **290**, the oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b* are in contact with the top surface of the insulating layer **186** in the illustrated example. When the end portion of the oxide semiconductor layer **230***a*

and the end portion of the oxide semiconductor layer **230***b* in the opening portion **290** are positioned over the insulating layer **186**, the oxide semiconductor film to be the oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b* can be processed relatively easily.

[0354] Note that the present invention is not limited to the above-described structures, as long as the opening portion **290** includes a region where the oxide semiconductor layer **230***a* and the conductive layer **220***a* are in contact with each other and a region where the oxide semiconductor layer **230***b* and the conductive layer **220***b* are in contact with each other. FIG. **14**A illustrates an example in which the oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b* in the opening portion **290** illustrated in FIG. **3**A are not in contact with the top surface of the insulating layer **186**. When the transistor **200***a* and the transistor **200***b* have the structure illustrated in FIG. **14**A, the distance (corresponding to the distance Hab illustrated in FIG. **3**B) between the oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b* can be increased without reductions in the contact area between the conductive layer **220***a* and the oxide semiconductor layer **230***a* and the contact area between the conductive layer **220***b* and the oxide semiconductor layer **230***b*. Accordingly, the distance between the conductive layer **220***a* and the conductive layer **220***b* can be shortened, so that the semiconductor device can be miniaturized or highly integrated.

[0355] FIG. **14**B illustrates an example in which the thickness of a portion of the oxide semiconductor layer **230***a* illustrated in FIG. **3**A that is formed over the top surface of the conductive layer **240***a* or the conductive layer **220***a* (hereinafter the thickness is referred to as a first thickness) is different from the thickness of a portion of the oxide semiconductor layer **230***a* that is formed over the sidewall of the opening portion **290** (hereinafter the thickness is referred to as a second thickness). For example, in the case where part of the oxide semiconductor layer **230***a* is deposited by a sputtering method, the first thickness and the second thickness of the oxide semiconductor layer **230***a* are different in some cases. For example, as illustrated in FIG. **14**B, the ratio of the second thickness to the first thickness is lower than 1, lower than 0.8, or lower than 0.5 in some cases. In particular, as the angle θ**281** illustrated in FIG. **12**B is closer to 90°, the ratio of the second thickness to the first thickness of the oxide semiconductor layer **230***a* tends to be smaller. The above description of the first thickness and the second thickness can apply to the oxide semiconductor layer **230***b*.

[0356] Here, FIG. **3**A illustrates a structure in which in the outside of the opening portion **290**, the end portion of the oxide semiconductor layer **230** is positioned inward from the end portion of the conductive layer **240**. In addition, the end portion of the oxide semiconductor layer **230** outside the opening portion **290** is positioned inward from the end portion of the conductive layer **240** on the side opposite to the opening portion **290**, that is, the end portion of the oxide semiconductor layer **230** outside the opening portion **290** is closer to the opening portion **290** than the end portion of the conductive layer **240** on the side opposite to the opening portion **290** is. In this case, the top surface of the conductive layer **240** includes a region in contact with the insulating layer **250** and a region in contact with the oxide semiconductor layer **230**. Specifically, the top surface of the conductive layer **240***a* includes a region in contact with the insulating layer **250** and a region in contact with the oxide semiconductor layer **230***a*. The top surface of the conductive layer **240***b* includes a region in contact with the insulating layer **250** and a region in contact with the oxide semiconductor layer **230***b*.

[0357] FIG. **15**A illustrates an example in which in the outside of the opening portion **290** illustrated in FIG. **3**A, the end portion of the oxide semiconductor layer **230** is aligned or substantially aligned with the end portion of the conductive layer **240** on the side opposite to the opening portion **290** in a plan view. In the structure illustrated in FIG. **15**A, the formation steps of the conductive layers **240***a* and **240***b* and the formation steps of the oxide semiconductor layers **230***a* and **230***b* can be partly shared. Thus, the conductive layers **240***a* and **240***b* do not need to be formed separately from the oxide semiconductor layers **230***a* and **230***b*, which leads to a reduction

in the number of steps.
[0358] FIGS. **15**B and **15**C are plan views each illustrating an example where the shape of the opening portion **290** in the plan view is a substantially quadrangular shape with rounded corners. FIG. **15**B illustrates an example in which the opening portion **290** has a substantially square shape with rounded corners in the plan view. FIG. **15**C illustrates an example in which the opening portion **290** has a substantially rectangular shape with rounded corners in the plan view. Although in the example illustrated in FIG. **15**C, the shape of the opening portion **290** in the plan view is a substantially rectangle having the long sides extending in the X direction, the shape of the opening portion **290** in the plan view may be a substantially rectangle having the long sides extending in the Y direction. In the case where the opening portion **290** has a substantially quadrangular shape in the plan view, the sides of the quadrangular shape may be non-parallel to the X direction and the Y direction.
[0359] When the shape of the opening portion **290** in the plan view is the shape illustrated in FIG. **15**B or FIG. **15**C, the channel width per unit area of each of the transistor **200***a* and the transistor **200***b* can be increased. This can increase on-state currents of the transistor **200***a* and the transistor **200***b*.
Structural Example 2 of Semiconductor Device
[0360] A structure example of the semiconductor device that is different from the structure illustrated in FIGS. **1**A to **1**D and FIGS. **2**A to **2**C is described below. Semiconductor devices illustrated in FIGS. **16**A to **16**C, FIGS. **17**A to **17**C, FIGS. **18**A to **18**D, and FIGS. **19**A to **19**D each include the capacitor **100** and a transistor whose structure is partly different from that of the transistor **200**. Note that description of the portions already described is omitted and only different portions are described in detail. Even when positions or shapes of components are different from those in the above example, the same reference numerals are used as long as the components have the same functions as those in the above example, and detailed description thereof is omitted in some cases.
[Transistor **200**A]
[0361] FIG. **16**A is a plan view of a semiconductor device including a transistor **200**Aa and a transistor **200**Ab. FIG. **16**B is a cross-sectional view taken along a dashed-dotted line A**1**-A**2** in FIG. **16**A. FIG. **16**C is a cross-sectional view taken along a dashed-dotted line A**3**-A**4** in FIG. **16**A. For the sake of clarity of the drawing, the conductive layer **260** is shown with a hatching pattern in FIG. **16**A. FIG. **2**D can be referred to for a cross-sectional view along a dashed-dotted line A**5**-A**6** in FIG. **16**B. Hereinafter, the transistor **200**Aa and the transistor **200**Ab are collectively referred to as a transistor **200**A in some cases.
[0362] The semiconductor device illustrated in FIGS. **16**A to **16**C includes the insulating layer **180**; the conductive layer **110**; the insulating layer **160**; the insulating layer **185**; the insulating layer **186**; the conductive layer **161***a*; the conductive layer **161***b*; the capacitor **100***a*; and the capacitor **100***b*; the transistor **200**Aa and the transistor **200**Ab over the insulating layer **185**, the insulating layer **186**, the conductive layer **161***a*, and the conductive layer **161***b*; the insulating layer **280** over the insulating layer **185** and the insulating layer **186**; the insulating layer **281** over the insulating layer **280**; an insulating layer **284**; an insulating layer **285** over the insulating layer **284**; and a conductive layer **265** over the transistor **200**Aa, the transistor **200**Ab, the insulating layer **284**, and the insulating layer **285**. The insulating layer **284** includes a region positioned between the conductive layer **260** and the insulating layer **285**. The insulating layer **284** and the insulating layer **285** function as interlayer films.
[0363] The semiconductor device illustrated in FIGS. **16**A to **16**C is different from the semiconductor device illustrated in FIGS. **1**A to **1**D and FIGS. **2**A to **2**C in including the conductive layer **265**, the insulating layer **284**, and the insulating layer **285**.
[0364] In the example illustrated in FIGS. **16**A to **16**C, the conductive layer **265** is provided to extend in the Y direction. The conductive layer **265** functions as the other of the wiring WOL and

the wiring BGL. Alternatively, the conductive layer **265** may be provided to extend in the X direction.

[0365] For the conductive layer **265**, a material usable for the conductive layer **260** can be used. For example, a high-melting-point material that has both heat resistance and conductivity, such as tungsten or molybdenum, can be used for the conductive layer **265**. Alternatively, a low-resistance conductive material such as aluminum or copper can be used. The use of a low-resistance conductive material can reduce wiring resistance.

[0366] The transistor **200**Aa includes the conductive layer **220***a*, the conductive layer **255**, the conductive layer **240***a*, the insulating layer **225**, the oxide semiconductor layer **230***a*, the insulating layer **250**, and the conductive layer **260**. The transistor **200**Ab includes the conductive layer **220***b*, the conductive layer **255**, the conductive layer **240***b*, the insulating layer **225**, the oxide semiconductor layer **230***b*, the insulating layer **250**, and the conductive layer **260**. The conductive layer **265** includes a region in contact with the conductive layer **260**. In addition, the conductive layer **265** may be regarded as a component of each of the transistor **200**Aa and the transistor **200**Ab. The insulating layer **284** is provided over the insulating layer **250**.

[0367] As illustrated in FIGS. **16**B and **16**C, the insulating layer **284** is positioned over the insulating layer **250**. The insulating layer **284** is provided with an opening portion **270** reaching the insulating layer **250** at a position overlapping with the opening portion **290**. At least part of the conductive layer **260** is provided in the opening portion **270**. The conductive layer **260** is in contact with the insulating layer **250** in the opening portion **270**.

[0368] The conductive layer **260** is provided to fill the opening portion **290** and the opening portion **270**. The conductive layer **260** includes a portion facing the oxide semiconductor layer **230** with the insulating layer **250** therebetween in the opening portion **290** and a portion positioned in the opening portion **270**.

[0369] A portion of the conductive layer **265** not overlapping with the opening portion **290** is mainly positioned over the insulating layer **285**. Thus, the conductive layer **265** mainly overlaps with the conductive layer **240***a* and the conductive layer **240***b* with the insulating layers **284** and **285** therebetween. Accordingly, the distance between the conductive layer **265** and the conductive layer **240***a* and the distance between the conductive layer **265** and the conductive layer **240***b* can be increased. Thus, parasitic capacitance generated between the conductive layer **265** and the conductive layer **240***a* and parasitic capacitance generated between the conductive layer **265** and the conductive layer **240***b* can be reduced. In particular, the insulating layer **285** preferably has a large thickness, for example, a thickness larger than the thickness of the insulating layer **284**, in which case the distance between the conductive layer **265** and the conductive layer **240***a* and the distance between the conductive layer **265** and the conductive layer **240***b* can be increased. In addition, the conductive layers **240***a* and **240***b* may include a portion overlapping with the conductive layer **265** without the insulating layer **285** therebetween.

[0370] FIG. **16**B illustrates an example where the width of the opening portion **270** is smaller than the width D of the opening portion **290**. The smaller the width of the opening portion **270** is, the larger the distance between the conductive layer **240***a* and the conductive layer **260** and the distance between the conductive layer **265** and the conductive layer **240***b* can be. This is preferable, in which case parasitic capacitance generated between the conductive layer **240***a* and the conductive layer **260** and parasitic capacitance generated between the conductive layer **240***b* and the conductive layer **260** can be reduced. For example, the width of the opening portion **270** is preferably smaller than or equal to that of the opening portion **290**.

[0371] The top surface of the conductive layer **260** and the top surface of the insulating layer **285** or the insulating layer **284** are preferably level with or substantially level with each other. The conductive layer **265** is provided over the insulating layer **285**, the insulating layer **284**, and the conductive layer **260**, and is in contact with the top surface of the conductive layer **260**. It can be said that the conductive layer **260** and the conductive layer **265** are connected to each other.

[0372] That is, the transistor **200**A has a structure where the parasitic capacitance generated between the other of its source and drain electrodes and a gate wiring is reduced. Accordingly, the frequency characteristics of a circuit including the transistor can be improved.
[0373] Although this embodiment describes the example where the opening portion **270** has a circular shape in the plan view, the present invention is not limited thereto. Any of the above-described shapes that can be employed for the opening portion **290** can be employed for the shape of the opening portion **270**.
[0374] The width of the opening portion **270** varies in the depth direction in some cases. Here, the maximum width of the opening portion **270** provided in the insulating layer **284** in the cross-sectional view is specifically used as the width of the opening portion **270**.
[0375] An insulating layer having a function of capturing or fixing hydrogen is preferably used as the insulating layer **284**. With such a structure, diffusion of hydrogen from above the insulating layer **284** into the oxide semiconductor layer **230** can be inhibited, and hydrogen contained in the oxide semiconductor layer **230** can be captured or fixed. Thus, the hydrogen concentration in the oxide semiconductor layer **230** can be reduced. For the insulating layer **284**, an aluminum oxide film, a hafnium oxide film, a hafnium silicate film, or the like can be used.
[0376] As the insulating layer **284**, a barrier insulating layer against hydrogen can be used. In this case, diffusion of hydrogen from above the insulating layer **284** into the oxide semiconductor layer **230** can be inhibited. A silicon nitride film and a silicon nitride oxide film can be suitably used for the insulating layer **284** because they release few impurities (e.g., water and hydrogen) and are less likely to transmit oxygen and hydrogen.
[0377] In the case where a silicon nitride film is used for the insulating layer **284**, the silicon nitride film is preferably formed by a sputtering method. A deposition gas in a sputtering method need not include molecules containing hydrogen; thus, the hydrogen concentration in the insulating layer **284** can be reduced. When the insulating layer **284** is formed by a sputtering method, a high-density silicon nitride film can be obtained.
[0378] The insulating layer **284** may have a stacked-layer structure of an insulating layer having a function of capturing or fixing hydrogen and a barrier insulating layer against hydrogen. For example, a stack of an aluminum oxide film and a silicon nitride film over the aluminum oxide film may be used as the insulating layer **284**.
[0379] The insulating layer **285** functions as an interlayer film and thus is preferably formed using any of the above-described materials with a low relative permittivity. For example, the insulating layer **285** preferably includes a silicon oxide film.
[0380] The above is the description of the semiconductor device including the transistor **200**Aa and the transistor **200**Ab in addition to the capacitor **100***a* and the capacitor **100***b*.
[Transistor **200**B]
[0381] FIG. **17**A is a plan view of a semiconductor device including a transistor **200**Ba and a transistor **200**Bb. FIG. **17**B is a cross-sectional view taken along a dashed-dotted line A**1**-A**2** in FIG. **17**A. FIG. **17**C is a cross-sectional view taken along a dashed-dotted line A**3**-A**4** in FIG. **17**A. For the sake of clarity of the drawing, the conductive layer **260** is shown with a hatching pattern in FIG. **17**A. FIG. **2**D can be referred to for a cross-sectional view along a dashed-dotted line A**5**-A**6** in FIG. **17**B. The description of portions similar to those in FIGS. **16**A to **16**C is omitted below, and only differences are described in detail. Hereinafter, the transistor **200**Ba and the transistor **200**Bb are collectively referred to as a transistor **200**B in some cases.
[0382] The semiconductor device illustrated in FIGS. **17**A to **17**C is different from the semiconductor device illustrated in FIGS. **16**A to **16**C in that the insulating layer **250** includes a portion in contact with the side surface of the insulating layer **284** in the opening portion **270**, for example.
[0383] The insulating layer **250** is in contact with the oxide semiconductor layer **230** and the insulating layer **284** in the opening portion **270**. A portion of the insulating layer **250** which is

placed in the opening portion **270** reflects the shape of the opening portion **270**. Specifically, the insulating layer **250** is provided along the sidewall of the opening portion **270** (the side surface of the insulating layer **284**). The conductive layer **260** is provided to fill at least part of a depressed portion of the insulating layer **250** reflecting the shape of the opening portion **270**.

[0384] In the semiconductor device illustrated in FIGS. **17**A to **17**C, the conductive layer **260** overlaps with neither the top surface of the conductive layer **240***a* nor the top surface of the conductive layer **240***b*. Thus, parasitic capacitance generated between the conductive layer **240***a* and the conductive layer **260** and parasitic capacitance generated between the conductive layer **240***b* and the conductive layer **260** can be reduced.

[0385] As illustrated in FIG. **17**B, the maximum width of the conductive layer **260** is smaller than a width D of the opening portion **290** in the cross-sectional view. As described above, the maximum width of the conductive layer **260** is preferably smaller than the width D of the opening portion **290**, in which case parasitic capacitance generated between the conductive layer **260** and the conductive layer **240***a* and parasitic capacitance generated between the conductive layer **260** and the conductive layer **240***b* can be reduced. For example, as in FIG. **17**B, the relation in magnitude between the two widths in the semiconductor device of one embodiment of the present invention can be observed in one cross section parallel to the Z direction.

[0386] FIG. **17**B illustrates an example where the width of the opening portion **270** is smaller than the width D of the opening portion **290**. The width of the opening portion **270** is preferably smaller than or equal to that of the opening portion **290**. In this case, the conductive layer **260** overlaps with neither the top surface of the conductive layer **240***a* nor the top surface of the conductive layer **240***b*. This is preferable because parasitic capacitance generated between the conductive layer **260** and the conductive layer **240***a* and parasitic capacitance generated between the conductive layer **260** and the conductive layer **240***b* can be reduced.

[0387] Although this embodiment mainly describes the example where the conductive layer **260** overlaps with neither the top surface of the conductive layer **240***a* nor the top surface or the conductive layer **240***b*, the conductive layer **260** may include a portion overlapping with the top surface of the conductive layer **240***a* and a portion overlapping with the top surface or the conductive layer **240***b*. The overlapping portions are preferably smaller, in which case the parasitic capacitance between the conductive layer **260** and the conductive layer **240***a* and the parasitic capacitance between the conductive layer **260** and the conductive layer **240***b* can be reduced. For example, the width of the opening portion **270** is preferably smaller than the short-side width of the conductive layer **265** (the maximum width of the conductive layer **265** in FIG. **17**B).

[0388] That is, in the transistor **200**B, the parasitic capacitance generated between the other of the source electrode and the drain electrode and the gate electrode and the parasitic capacitance generated between the other of the source electrode and the drain electrode and the gate wiring are reduced. Accordingly, the frequency characteristics of a circuit including the transistor can be improved.

[Transistor **200**C]

[0389] FIG. **18**A is a plan view of a semiconductor device including a transistor **200**Ca and a transistor **200**Cb. FIG. **18**B is a cross-sectional view taken along a dashed-dotted line A**1**-A**2** in FIG. **18**A. FIG. **18**C is a cross-sectional view taken along a dashed-dotted line A**3**-A**4** in FIG. **18**A. FIG. **18**D is a cross-sectional view taken along a dashed-dotted line A**5**-A**6** in FIG. **18**B. For the sake of clarity of the drawing, the conductive layer **255** is shown with a hatching pattern in FIG. **18**A. Hereinafter, the transistor **200**Ca and the transistor **200**Cb are collectively referred to as a transistor **200**C in some cases. FIG. **18**D is also referred to as a plan view.

[0390] The semiconductor device illustrated in FIGS. **18**A to **18**D is different from the semiconductor device illustrated in FIGS. **1**A to **1**D and FIGS. **2**A to **2**D in that an insulating layer **283** is provided but the conductive layer **260** and the insulating layer **250** are not provided.

[0391] In each of the transistor **200**Ca and the transistor **200**Cb, the conductive layer **255** functions

as a gate electrode, and the insulating layer **225** functions as a gate insulating layer. The transistor **200**Ca and the transistor **200**Cb are single-gate transistors. Here, the conductive layer **255** includes a region functioning as the wiring WOL illustrated in FIG. **2**E.

[0392] As the insulating layer **283**, a barrier insulating layer against hydrogen is preferably used. Such a structure can inhibit diffusion of hydrogen from above the transistor **200** into the oxide semiconductor layer **230**.

[0393] In addition, the insulating layer **283** can be formed using an insulating material usable for the insulating layer **250**.

[0394] An insulating layer can be provided over the insulating layer **283** to fill the opening portion **290**. As the insulating layer, a single layer or stacked layers of any of the insulators mentioned above in the above-described section [Insulator] can be used.

[0395] The structure not including the conductive layer **260** can lead to a reduction of the manufacturing cost. Furthermore, the area occupied by the semiconductor device can be reduced, and miniaturization or high integration of the semiconductor device can be achieved. Meanwhile, by providing the conductive layer **260**, a dual-gate transistor can be provided in the semiconductor device. This enables control of the threshold voltage V.sub.th of the transistor, for example. Thus, the transistors included in the semiconductor device can have favorable electric characteristics.

[Transistor **200**D]

[0396] FIG. **19**A is a plan view of a semiconductor device including a transistor **200**Da and a transistor **200**Db. FIG. **19**B is a cross-sectional view taken along a dashed-dotted line A**1**-A**2** in FIG. **19**A. FIG. **19**C is a cross-sectional view taken along a dashed-dotted line A**3**-A**4** in FIG. **19**A. FIG. **19**D is a cross-sectional view taken along a dashed-dotted line A**5**-A**6** in FIG. **19**B. For the sake of clarity of the drawing, the conductive layer **260** is shown with a hatching pattern in FIG. **19**A. Hereinafter, the transistor **200**Da and the transistor **200**Db are collectively referred to as a transistor **200**D in some cases. FIG. **19**D is also referred to as a plan view.

[0397] The semiconductor device illustrated in FIGS. **19**A to **19**D is different from the semiconductor device illustrated in FIGS. **1**A to **1**D and FIGS. **2**A to **2**D in that the conductive layer **255** and the insulating layer **281** are not provided.

[0398] In each of the transistor **200**Da and the transistor **200**Db, the conductive layer **260** functions as a gate electrode, and the insulating layer **250** functions as a gate insulating layer. The transistor **200**Da and the transistor **200**Db are single-gate transistors. Here, the conductive layer **260** includes a region functioning as the wiring WOL illustrated in FIG. **2**E.

[0399] FIGS. **19**A to **19**C illustrate an example in which the conductive layer **260** is provided to extend in the X direction. Alternatively, the conductive layer **260** may be provided to extend in the Y direction, for example.

[0400] The structure including neither the conductive layer **255** nor the insulating layer **281** can lead to a reduction the manufacturing cost of the semiconductor device. Furthermore, the area occupied by the semiconductor device can be reduced, and miniaturization or high integration of the semiconductor device can be achieved. Meanwhile, by the conductive layer **255** and the insulating layer **281**, a dual-gate transistor can be provided in the semiconductor device. This enables control of the threshold voltage V.sub.th of the transistor, for example. Thus, the transistors included in the semiconductor device can have favorable electric characteristics.

[0401] Incidentally, the above-described structures of the transistor **200** can also be employed for the transistor **200**A to the transistor **200**D.

<Example of Method for Manufacturing Semiconductor Device>

[0402] Next, a method for manufacturing a semiconductor device of one embodiment of the present invention is described. As for a material and a formation method of each component, descriptions of portions similar to those described in the above embodiment are omitted in some cases.

[0403] FIGS. **20**A, **21**A, **22**A, **23**A, **24**A, **25**A, **26**A, **27**A, **28**A, **29**A, **30**A, **31**A, **32**A, **33**A, **34**A,

35A, **36**A, **37**A, **38**A, **39**A, **40**A, and **41**A are plan views. FIGS. **20**B, **21**B, **22**B, **23**B, **24**B, **25**B, **26**B, **27**B, **28**B, **29**B, **30**B, **31**B, **32**B, **33**B, **34**B, **35**B, **36**B, **37**B, **38**B, **39**B, **40**B, and **41**B are cross-sectional views taken along dashed-dotted lines A**1**-A**2** in the respective drawings, FIGS. **20**A, **21**A, **22**A, **23**A, **24**A, **25**A, **26**A, **27**A, **28**A, **29**A, **30**A, **31**A, **32**A, **33**A, **34**A, **35**A, **36**A, **37**A, **38**A, **39**A, **40**A, and **41**A. FIGS. **20**C, **21**C, **22**C, **23**C, **24**C, **25**C, **26**C, **27**C, **28**C, **29**C, **30**C, **31**C, **32**C, **33**C, **34**C, **35**C, **36**C, **37**C, **38**C, **39**C, **40**C, and **41**C are cross-sectional views taken along dashed-dotted lines A**3**-A**4** in the respective drawings, FIGS. **20**A, **21**A, **22**A, **23**A, **24**A, **25**A, **26**A, **27**A, **28**A, **29**A, **30**A, **31**A, **32**A, **33**A, **34**A, **35**A, **36**A, **37**A, **38**A, **39**A, **40**A, and **41**A.

[0404] Thin films included in the semiconductor device (e.g., insulating films, semiconductor films, and conductive films) can be formed by a sputtering method, a chemical vapor deposition (CVD) method, a vacuum evaporation method, a molecular beam epitaxy (MBE) method, a pulsed laser deposition (PLD) method, an ALD method, or the like.

[0405] Examples of the sputtering method include an RF sputtering method in which a high-frequency power source is used for a sputtering power source, a DC sputtering method in which a DC power source is used, and a pulsed DC sputtering method in which voltage applied to an electrode is changed in a pulsed manner. The RF sputtering method is mainly used for forming an insulating film, and the DC sputtering method is mainly used for forming a metal conductive film. A pulsed DC sputtering method is mainly employed in the case where a compound such as an oxide, a nitride, or a carbide is deposited by a reactive sputtering method.

[0406] In addition, CVD methods can be classified into a plasma enhanced CVD (PECVD) method using plasma, a thermal CVD (TCVD) method using heat, a photo CVD method using light, and the like. Moreover, CVD methods can be classified into a metal CVD (MCVD) method and a metal organic CVD (MOCVD) method according to a source gas.

[0407] A high-quality film can be obtained at a relatively low temperature through a plasma CVD method. A thermal CVD method does not use plasma and thus causes less plasma damage to an object to be processed. A wiring, an electrode, an element (e.g., a transistor or a capacitor), or the like included in a semiconductor device might be charged up by receiving charge from plasma, for example. In that case, the accumulated charge might break the wiring, electrode, element, or the like included in the semiconductor device. A thermal CVD method, which does not use plasma, does not cause such plasma damage, and thus can increase the yield of the semiconductor device. A thermal CVD method yields a film with few defects because of no plasma damage during film formation.

[0408] As the ALD method, a thermal ALD method, in which reaction between a precursor and a reactant progresses with only a thermal energy, a PEALD method, in which a reactant excited by plasma is used, or the like can be used.

[0409] Moreover, some precursors used in the ALD method contain an element such as carbon or chlorine. Thus, a film formed by the ALD method sometimes contains an element such as carbon or chlorine in a larger quantity than a film formed by another film formation method. Note that these elements can be quantified by XPS or SIMS. The formation method of a metal oxide of one embodiment of the present invention, which employs an ALD method and one or both of a deposition condition with a high substrate temperature and impurity removal treatment, can form a film with smaller quantities of carbon and chlorine than a method employing an ALD method but neither the deposition condition with a high substrate temperature nor the impurity removal treatment in some cases.

[0410] Differently from a film formation method in which particles ejected from a target or the like are deposited, a film is formed by reaction at a surface of an object to be processed in an ALD method. Thus, the ALD method can give good step coverage, almost regardless of the shape of an object to be processed. In particular, the ALD method allows excellent step coverage and excellent thickness uniformity and thus can be suitably used to cover a surface of an opening portion with a high aspect ratio, for example.

[0411] A CVD method and an ALD method differ from a sputtering method in which particles ejected from a target or the like are deposited. Thus, the CVD method and the ALD method can give good step coverage, almost regardless of the shape of an object to be processed. In particular, the ALD method allows excellent step coverage and excellent thickness uniformity and thus can be suitably used to cover a surface of an opening portion with a high aspect ratio, for example. However, the ALD method has a relatively low film formation rate; hence, in some cases, the ALD method is preferably combined with another film formation method with a high film formation rate, such as a CVD method.

[0412] By a CVD method, a film with a desired composition can be formed by adjusting the flow rate ratio of the source gases. For example, a CVD method enables formation of a film whose composition is continuously changed by changing the flow rate ratio of the source gases during film formation. In the case where a film is formed while the flow rate ratio of the source gases is changed, as compared with the case where a film is formed using a plurality of film formation chambers, the time taken for the film formation can be shortened because the time taken for transfer or pressure adjustment is not required. Hence, the productivity of the semiconductor device can be improved in some cases.

[0413] An ALD method in which a plurality of kinds of precursors are introduced at the same time enables formation of a film with a desired composition. In the case where a plurality of kinds of precursors are introduced, the number of cycles for each precursor is controlled, whereby a film with a desired composition can be formed.

[0414] Alternatively, thin films included in the semiconductor device (e.g., insulating films, semiconductor films, and conductive films) can be formed by a wet process such as a spin coating method, a dip coating method, a spray coating method, an inkjet method, dispensing, screen printing, offset printing, doctor blade coating, slit coating, roll coating, curtain coating, or knife coating.

[0415] In processing thin films included in the semiconductor device, a photolithography method or the like can be employed. Alternatively, the thin films may be processed by a nanoimprinting method, a sandblasting method, a lift-off method, or the like. Alternatively, island-shaped thin films may be directly formed by a film formation method using a shielding mask such as a metal mask.

[0416] There are two typical examples of photolithography methods. In one of the methods, a resist mask is formed over a thin film to be processed, the thin film is processed by etching or the like, and then the resist mask is removed. In the other method, a photosensitive thin film is formed and then processed into a desired shape by light exposure and development.

[0417] As light for exposure in a photolithography method, it is possible to use light with the i-line (wavelength: 365 nm), light with the g-line (wavelength: 436 nm), light with the h-line (wavelength: 405 nm), or light in which the i-line, the g-line, and the h-line are mixed. Alternatively, ultraviolet light, KrF laser light, ArF laser light, or the like can be used. Exposure may be performed by liquid immersion exposure technique. As the light for exposure, extreme ultraviolet (EUV) light or X-rays may also be used. Furthermore, instead of the light used for exposure, an electron beam can be used. EUV, X-rays, or an electron beam is preferably used to enable extremely minute processing. When exposure is performed by scanning with abeam such as an electron beam, a photomask is not needed.

[0418] For etching of thin films, a dry etching method, a wet etching method, a sandblast method, or the like can be used.

[0419] An example of a method for manufacturing the semiconductor device illustrated in FIG. **1**A and FIGS. **2**A and **2**B is described with reference to some drawings.

[0420] First, as illustrated in FIGS. **20**A to **20**C, the insulating layer **180** is formed over a substrate (not illustrated), and the conductive layer **110** and the insulating layer **111** are formed over the insulating layer **180**. For example, after the insulating layer **111** is formed over the insulating layer **180**, an opening portion reaching the insulating layer **180** is formed in the insulating layer **111**.

Next, a conductive film to be the conductive layer **110** later is formed to fill the opening portion. After that, planarization treatment is performed on the conductive film until the top surface of the insulating layer **111** is exposed. In this manner, the conductive layer **110** and the insulating layer **111** can be formed. As the planarization treatment, treatment using a chemical mechanical polishing (CMP) method (also referred to as CMP treatment) is suitable.

[0421] The conductive layer **110** may be formed by a photolithography method. In that case, the insulating layer **111** is not necessarily formed.

[0422] Next, as illustrated in FIGS. **21**A to **21**C, the insulating layer **160** is formed over the conductive layer **110** and the insulating layer **111**. After that, as illustrated in FIGS. **21**A to **21**C, the insulating layer **160** is processed to have the opening portion **190** reaching the conductive layer **110**. Here, the insulating layer **160** is preferably processed by anisotropic etching. It is particularly preferable to use a dry etching method, which is suitable for microfabrication.

[0423] Next, as illustrated in FIGS. **22**A to **22**C, a conductive film **115***f* to be the conductive layer **115** later is formed to cover the opening portion **190**. The conductive film **115***f* is formed along the sidewall of the opening portion **190**, the top surface of the conductive layer **110**, and the top surface of the insulating layer **160**.

[0424] The conductive film **115***f* is a layer provided in the opening portion **190**, and thus is preferably deposited by a CVD method or an ALD method, further preferably formed by an ALD method. Thus, the conductive film **115***f* with good coverage can be formed.

[0425] Next, as illustrated in FIGS. **23**A to **23**C, the mask layer **165** is applied to the conductive film **115***f*. Then, the mask layer **165** is subjected to anisotropic etching. In this manner, a region of the mask layer **165** positioned outside the opening portion **190** is removed. For example, the region of the mask layer **165** positioned outside the opening portion **190** is preferably removed by a dry etching method. As the mask layer **165**, a resist mask, a spin on carbon (SOC) film, or a spin on glass (SOG) film can be used, for example.

[0426] Next, as illustrated in FIGS. **24**A to **24**C, etching treatment is performed on the conductive film **115***f*. Thus, the conductive layer **115** is formed in the opening portion **190**. As the etching, a dry etching method or a wet etching method can be employed. It is particularly preferable to use a dry etching method, which is suitable for microfabrication.

[0427] Next, the mask layer **165** is removed. The mask layer **165** can be removed by a wet etching method, for example. Alternatively, the mask layer **165** may be removed by a dry etching method, for example.

[0428] Next, as illustrated in FIGS. **25**A to **25**C, the insulating layer **121** is formed to cover the conductive layer **115**, and a conductive film **120***f* to be the conductive layer **120***a* and the conductive layer **120***b* later is formed over the insulating layer **121**. The insulating layer **121** and the conductive film **120***f* are each formed in the opening portion **190** having a high aspect ratio. Thus, the insulating layer **121** and the conductive film **120***f* are preferably formed by a film formation method enabling good coverage, and are further preferably formed by a CVD method, an ALD method, or the like.

[0429] Next, as illustrated in FIGS. **26**A to **26**C, the conductive film **120***f* and the insulating layer **121** are processed. The conductive film **120***f* and the insulating layer **121** can be processed by a photolithography method. Here, the conductive film **120***f* and the insulating layer **121** are preferably processed using the same photomask, in which case the number of steps can be reduced as compared with the case where the conductive film **120***f* and the insulating layer **121** are processed using different photomasks. In addition, it is acceptable that the insulating layer **121** is not processed.

[0430] As illustrated in FIGS. **27**A to **27**C, the conductive film **120***f* is then processed to form the conductive layer **120***a* and the conductive layer **120***b*. Through the above steps, the capacitor **100***a* and the capacitor **100***b* are formed.

[0431] Next, as illustrated in FIGS. **28**A to **28**C, the insulating layer **185** is formed to cover the

capacitor **100***a* and the capacitor **100***b*, and the insulating layer **186** is formed over the insulating layer **185**. Specifically, the insulating layer **185** can be formed to cover the conductive layer **120***a*, the conductive layer **120***b*, and the insulating layer **121**. The insulating layer **185** is formed along the side surface of the conductive layer **120***a*, the top surface of the conductive layer **120***a*, the side surface of the conductive layer **120***b*, the top surface of the conductive layer **120***b*, the side surface of the insulating layer **121**, the top surface of the insulating layer **121**, and the top surface of the insulating layer **160**. The insulating layer **185** is formed to include the depressed portion **187** at a position overlapping with the opening portion **190**. The insulating layer **186** is formed to fill the depressed portion **187**.

[0432] The insulating layer **185** and the insulating layer **186** are each a layer provided in the opening portion **190**, and thus are preferably formed by a CVD method or an ALD method. For example, the insulating layer **185** formed along the side surfaces of the conductive layer **120***a* and the conductive layer **120***b* is particularly preferably formed by an ALD method. The insulating layer **186** formed to fill the opening portion **190** is particularly preferably formed by a CVD method. Alternatively, one or both of the insulating layers **185** and **186** may be formed by a sputtering method, for example. For example, the insulating layer **186** may be formed by a sputtering method.

[0433] Next, as illustrated in FIGS. **29**A to **29**C, planarization treatment is performed on the insulating layer **186** until the top surface of the insulating layer **185** is exposed. CMP treatment is suitable for the planarization treatment. For the sake of clarity of the drawing, exposed regions of the top surface of the insulating layer **185** are shown with a hatching pattern in FIG. **29**A.

[0434] By the planarization treatment, part of the insulating layer **185** as well as the insulating layer **186** is removed in some cases. Thus, the thickness of the insulating layer **185** in the exposed regions of the top surface thereof is smaller than that in the other region in some cases. Here, a material that enables easy end-point detection in planarization treatment is preferably used for the insulating layer **185**, in which case part of the insulating layer **185** can be inhibited from being removed. For example, silicon oxide and silicon nitride can be used as the insulating layer **186** and the insulating layer **185**, respectively.

[0435] When the insulating layer **186** is formed to fill the depressed portion **187** and the insulating layer **186** is planarized, the transistor **200***a* and the transistor **200***b* can be easily formed in a later step. For example, the conductive layer **220***a*, the conductive layer **220***b*, the oxide semiconductor layer **230***a*, the oxide semiconductor layer **230***b*, and the insulating layer **250** that are formed in later steps can be prevented from being divided due to a step generated by the depressed portion **187**. Furthermore, a method for manufacturing a semiconductor device with high production yield can be provided.

[0436] Next, as illustrated in FIGS. **30**A to **30**C, the opening portion **191***a* reaching the conductive layer **120***a* and the opening portion **191***b* reaching the conductive layer **120***b* are formed in the insulating layer **185**. Here, when the opening portion **191***a* and the opening portion **191***b* are formed in exposed regions of the top surface of the insulating layer **185**, the insulating layer **186** does not need to be processed. This is preferable because the opening portion **191***a* and the opening portion **191***b* can be easily formed.

[0437] After that, the conductive layer **161***a* is formed to fill the opening portion **191***a*, and the conductive layer **161***b* is formed to fill the opening portion **191***b*. For example, a conductive film to be the conductive layer **161***a* and the conductive layer **161***b* later is formed over the conductive layer **120***a*, the conductive layer **120***b*, the insulating layer **185**, and the insulating layer **186**. Next, planarization treatment is performed on the conductive film until the top surface of the insulating layer **186** is exposed. CMP treatment is suitable for the planarization treatment. In the above manner, the conductive layer **161***a* and the conductive layer **161***b* can be formed. The conductive layer **161***a* is formed in contact with the conductive layer **120***a*, and the conductive layer **161***b* is formed in contact with the conductive layer **120***b*.

[0438] Then, as illustrated in FIGS. **31**A to **31**C, the conductive layer **220***a* is formed over the conductive layer **161***a*, the insulating layer **185**, and the insulating layer **186**, and the conductive layer **220***b* is formed over the conductive layer **161***b*, the insulating layer **185**, and the insulating layer **186**. For example, a first conductive film to be the conductive layer **220***a***1** and the conductive layer **220***b***1** later is formed, and a second conductive film to be the conductive layer **220***a***2** and the conductive layer **220***b***2** later is formed over the first conductive film. Then, the first conductive film and the second conductive film are processed so that the conductive layer **220***a* including the conductive layer **220***a***1** and the conductive layer **220***a***2** and the conductive layer **220***b* including the conductive layer **220***b***1** and the conductive layer **220***b***2** can be formed. The conductive layer **220***a* is formed to include a region in contact with the top surface of the conductive layer **161***a*. The conductive layer **220***b* is formed to include a region in contact with the top surface of the conductive layer **161***b*.

[0439] Next, as illustrated in FIGS. **32**A to **32**C, the insulating layer **280** is formed over the conductive layer **220***a*, the conductive layer **220***b*, the insulating layer **185**, and the insulating layer **186**. Planarization treatment by a CMP method or the like is preferably performed after formation of the insulating layer **280** to planarize the top surface of the insulating layer **280**. By the planarization treatment of the insulating layer **280**, a surface over which the conductive layer **255** functioning as a wiring is to be formed can be made flat, whereby disconnection of the conductive layer **255** can be inhibited. Incidentally, it is acceptable that the planarization treatment is not performed, in which case the manufacturing cost can be reduced.

[0440] Next, as illustrated in FIGS. **32**A to **32**C, the conductive layer **255** is formed over the insulating layer **280**. The conductive layer **255** is preferably formed by a sputtering method, for example. By using a sputtering method that does not need to use a molecule containing hydrogen as a deposition gas, the hydrogen concentration in the conductive layer **255** can be reduced and entry of hydrogen into the oxide semiconductor layer **230** can be inhibited.

[0441] Next, as illustrated in FIGS. **33**A to **33**C, the insulating layer **281** is formed over the conductive layer **255** and the insulating layer **280**. Planarization treatment by a CMP method or the like is preferably performed after formation of the insulating layer **281** to planarize the top surface of the insulating layer **281**. By the planarization treatment of the insulating layer **281**, surfaces over which the conductive layers **240***a* and **240***b* are to be formed can be made flat, whereby disconnection of each of the conductive layers **240***a* and **240***b* can be inhibited. Incidentally, it is acceptable that the planarization treatment is not performed, in which case the manufacturing cost can be reduced.

[0442] Next, as illustrated in FIGS. **33**A to **33**C, a conductive film **240***f***1** is formed over the insulating layer **281**, and a conductive film **240***f***2** is formed over the conductive film **240***f***1**. The conductive film **240***f***1** is a conductive film to be the conductive layer **240***a***1** and the conductive layer **240***b***1** later. The conductive film **240***f***2** is a conductive film to be the conductive layer **240***a***2** and the conductive layer **240***b***2** later. Hereinafter, the conductive film **240***f***1** and the conductive film **240***f***2** may be collectively referred to as a conductive film **240***f*.

[0443] Then, as illustrated in FIGS. **34**A to **34**C, the opening portion **290** is formed in the conductive film **240***f*, the insulating layer **281**, the conductive layer **255**, and the insulating layer **280**. The opening portion **290** is formed so that at least part of the top surface of each of the conductive layer **220***a***2**, the conductive layer **220***b***2**, and the insulating layer **186** is exposed. In this case, the depressed portion **221***a* and the depressed portion **221***b* are preferably provided at respective positions of the conductive layer **220***a***2** and the conductive layer **220***b***2** overlapping with the opening portion **290**. By forming the opening portion **290**, the bottom portion and the sidewall of each of the depressed portion **221***a* and the depressed portion **221***b* are preferably exposed. In the insulating layer **186**, the depressed portion **222** is provided at a position that overlaps with the opening portion **290** and is between the conductive layer **220***a* and the conductive layer **220***b* in some cases.

[0444] For microfabrication and a reduction in transistor size, in forming the opening portion **290**, parts of the conductive layer **220***a***2** and the conductive layer **220***b***2**, part of the insulating layer **280**, part of the conductive layer **255**, and part of the conductive film **240***f* are preferably processed using anisotropic etching. It is particularly preferable to use a dry etching method, which is suitable for microfabrication. The opening portion **290** may be formed under processing conditions different between layers. Depending on the materials, processing conditions, and the like of the conductive layers **220***a***2** and **220***b***2**, the insulating layer **280**, the conductive layer **255**, the insulating layer **281**, the conductive film **240***f***1**, and the conductive film **240***f***2**, the inclinations of the side surfaces of the conductive layers **220***a***2** and **220***b***2**, the inclination of the side surface of the insulating layer **280**, the inclination of the side surface of the conductive layer **255**, the inclination of the side surface of the insulating layer **281**, the inclination of the side surface of the conductive film **240***f***1**, and the inclination of the side surface of the conductive film **240***f***2** may be different from each other in the opening portion **290**.

[0445] In the formation step of the opening portion **290** or the like, a region containing a halogen element is sometimes provided in at least one of the bottoms and the sidewalls of the depressed portion **221***a* and the depressed portion **221***b*, the side surface of the insulating layer **280**, the side surface of the conductive layer **255**, the side surface of the insulating layer **281**, the side surface of the conductive film **240***f***1**, and the top surface and the side surface of the conductive film **240***f***2**. Examples of the region include a region containing fluorine, a region containing chlorine, and a region containing fluorine and chlorine. In some cases, a halogen element originating from an etching gas used in dry etching remains in the region, for example.

[0446] Subsequently, heat treatment is preferably performed. The heat treatment is performed, for example, at higher than or equal to 250° C. and lower than or equal to 650° C., preferably higher than or equal to 300° C. and lower than or equal to 500° C., further preferably higher than or equal to 320° C. and lower than or equal to 450° C.

[0447] The heat treatment is performed in a nitrogen gas atmosphere, an inert gas atmosphere, or an atmosphere containing an oxidizing gas at 10 ppm or more, 1% or more, or 10% or more. For example, in the case where the heat treatment is performed in a mixed atmosphere of a nitrogen gas and an oxygen gas, the proportion of the oxygen gas is preferably approximately 20%. The heat treatment may be performed under a reduced pressure. Alternatively, heat treatment may be performed in an atmosphere of a nitrogen gas or an inert gas, and then another heat treatment may be performed in an atmosphere containing an oxidizing gas at 10 ppm or more, 1% or more, or 10% or more in order to compensate for released oxygen. By the above-described heat treatment, impurities such as hydrogen and water contained in the insulating layer **280** or the like can be reduced before the oxide semiconductor layer **230** is formed.

[0448] The gas used in the above heat treatment is preferably highly purified. For example, the amount of moisture contained in the gas used in the above heat treatment is preferably 1 ppb or less, further preferably 0.1 ppb or less, still further preferably 0.05 ppb or less. The heat treatment using a highly purified gas can prevent the entry of moisture or the like into the insulating layer **280** or the like as much as possible.

[0449] Next, as illustrated in FIGS. **35**A to **35**C, an insulating film **225***f* to be the insulating layer **225** later is formed to cover the opening portion **290**. The insulating film **225***f* is formed in contact with an exposed part of the top surface of the insulating layer **186** (the bottom portion and the sidewall of the depressed portion **222** in the case where the insulating layer **186** includes the depressed portion **222** at a position overlapping with the opening portion **290**), the bottom portions and the sidewalls of the depressed portion **221***a* and the depressed portion **221***b*, the side surface of the insulating layer **280**, the side surface of the conductive layer **255**, the side surface of the insulating layer **281**, the side surface of the conductive film **240***f***1**, and the top surface and the side surface of the conductive film **240***f***2**.

[0450] Because the insulating film **225***f* is provided in the opening portion **290**, the insulating film

225*f* is preferably formed by a CVD method or an ALD method, further preferably formed by an ALD method. In this manner, the insulating film **225***f* can be formed with good coverage.

[0451] In this embodiment, a first insulating film and a second insulating film are formed in this order as the insulating film **225***f* by an ALD method. For example, a silicon nitride film is deposited by a PEALD method as the first insulating film, and a silicon oxide film is deposited by a PEALD method as the second insulating film. In that case, the first insulating film and the second insulating film are preferably successively deposited without exposure to the air. Forming the first insulating film and the second insulating film successively without exposure to the air can lead to an increase in productivity. Furthermore, impurities (typically, moisture or the like) that would be taken into the interface between the first insulating film and the second insulating film and the vicinity thereof can be reduced.

[0452] Then, as illustrated in FIGS. **36**A to **36**C, the insulating film **225***f* is processed so that the top surface of the conductive film **240***f***2** is exposed, and the conductive layer **220***a***2**, the conductive layer **220***b***2**, and the insulating layer **186** are exposed in the opening portion **290**. In the opening portion **290**, the bottom portion of the depressed portion **221***a* and the bottom portion of the depressed portion **221***b* are preferably exposed.

[0453] By processing the insulating film **225***f* by anisotropic etching, a region of the insulating film **225***f* that is positioned on the top surface of the conductive film **240***f***2** and a region of the insulating film **225***f* that is positioned on the bottom portion of the opening portion **290** are removed. In this manner, the insulating film **225***f* can remain only on the side surface of the opening portion **290**. In the opening portion **290**, the insulating layer **225** formed in this manner includes a region in contact with the top surface of the conductive layer **220***a*, a region in contact with the top surface of the conductive layer **220***b*, a region in contact with the side surface of the insulating layer **280**, a region in contact with the side surface of the conductive layer **255**, a region in contact with the side surface of the insulating layer **281**, and a region in contact with the side surface of the conductive film **240***f*, a region in contact with the top surface of the insulating layer **186**, a region in contact with the side surface of the conductive layer **220***a***1**, and a region in contact with the side surface of the conductive layer **220***b***1**, for example. The insulating film **225***f* is preferably processed by anisotropic etching using a dry etching method.

[0454] As described with reference to FIG. **6**B, in processing of the insulating film **225***f*, parts of the conductive layers **220***a***2** and **220***b***2** may be removed, and thus, depressed portions (the above-described first depressed portions) may be provided in the conductive layers **220***a***2** and **220***b***2**.

[0455] It is preferable to perform oxygen supply before processing the insulating film **225***f* that has been deposited (see FIGS. **35**A to **35**C). Accordingly, oxygen can be supplied to the second insulating film, and oxygen can be supplied from the second insulating film to the oxide semiconductor layer **230** owing to heat to be applied after the formation of the oxide semiconductor layer **230**, for example. Providing the first insulating film having a barrier property against oxygen can inhibit diffusion of oxygen into the conductive layer **220** and the conductive layer **240** to prevent reductions in conductivities of the conductive layer **220** and the conductive layer **240**. Accordingly, the range of choices for the materials of the conductive layer **220** and the conductive layer **240** can be widened.

[0456] Alternatively, oxygen may be supplied after the insulating film **225***f* is processed (see FIGS. **36**A to **36**C). Accordingly, oxygen can be supplied to the second insulating film, and oxygen can be supplied from the second insulating film to the oxide semiconductor layer **230** owing to heat to be applied after the formation of the oxide semiconductor layer **230**, for example. Furthermore, the use of oxide conductors for the conductive layer **220***a***2**, the conductive layer **220***b***2**, and the conductive film **240***f***2** can inhibit reductions in the conductivities of the conductive layer **220***a***2**, the conductive layer **220***b***2**, and the conductive film **240***f***2** even when oxygen is supplied after the second insulating film is processed.

[0457] Examples of the treatment for supplying oxygen include heat treatment in an oxygen-

containing atmosphere and plasma treatment in an oxygen-containing atmosphere (including microwave plasma treatment). Alternatively, an oxide film (preferably a metal oxide film) may be formed by a sputtering method in an oxygen-containing atmosphere to supply oxygen to the second insulating film. The formed oxide film may be removed immediately or left as it is. In the case where the formed oxide film is left as it is, the oxide film can be used as part of the oxide semiconductor layer. An oxygen-containing atmosphere can include not only an oxygen gas (O.sub.2) but also a gas of an oxygen-containing compound such as ozone (O.sub.3) or dinitrogen monoxide (N.sub.2O). The substrate temperature in the plasma treatment is higher than or equal to room temperature (25° C.) and lower than or equal to 450° C.

[0458] Then, as illustrated in FIGS. **37**A to **37**C, an oxide semiconductor film **230***f* to be the oxide semiconductor layers **230***a* and **230***b* later is formed to cover the opening portion **290**. The oxide semiconductor film **230***f* is provided in contact with the bottom portion and the sidewall of the depressed portion **221***a*, the bottom portion and the sidewall of the depressed portion **221***b*, the exposed part of the top surface of the insulating layer **186**, the side surface of the insulating layer **225**, the side surface of the conductive film **240***f***1**, and the top surface and the side surface of the conductive film **240***f***2**.

[0459] The description in Embodiment 2 can be referred to for the formation method of the oxide semiconductor film **230***f*.

[0460] In this embodiment, as the oxide semiconductor film **230***f*, a first oxide semiconductor film, a second oxide semiconductor film, and a third oxide semiconductor film are formed in this order. The first oxide semiconductor film is an oxide semiconductor film to be the oxide semiconductor layers **230***a***1** and **230***b***1** illustrated in FIG. **13**B, the second oxide semiconductor film is an oxide semiconductor film to be the oxide semiconductor layers **230***a***2** and **230***b***2** illustrated in FIG. **13**B, and the third oxide semiconductor film is an oxide semiconductor film to be the oxide semiconductor layer **230***a***3** and **230***b***3** illustrated in FIG. **13**B.

[0461] For example, an In—Ga—Zn oxide film is formed by a thermal ALD method as the first oxide semiconductor film. An indium oxide film is formed by a thermal ALD method as the second oxide semiconductor film. An In—Ga—Zn oxide film is formed by a sputtering method as the third oxide semiconductor film.

[0462] The first oxide semiconductor film and the second oxide semiconductor film are preferably successively formed without exposure to the air. When the first oxide semiconductor film and the second oxide semiconductor film are successively formed without exposure to the air, the productivity can be increased. Furthermore, impurities (typically, moisture or the like) taken into the interface between the first oxide semiconductor film and the second oxide semiconductor film and the vicinity of the interface can be reduced.

[0463] After formation of the second oxide semiconductor film, oxygen may be supplied to the second oxide semiconductor film. Accordingly, oxygen can be supplied to the oxide semiconductor layer **230** by heat or the like to be applied after the treatment. For the details of the treatment for supplying oxygen, the above description can be referred to.

[0464] Next, heat treatment is preferably performed. The heat treatment temperature is, for example, preferably higher than or equal to 100° C. and lower than or equal to 650° C., further preferably higher than or equal to 250° C. and lower than or equal to 600° C., still further preferably higher than or equal to 350° C. and lower than or equal to 550° C. For the details of the heat treatment, the above description can be referred to.

[0465] The gas used in the above heat treatment is preferably highly purified. The heat treatment using a highly purified gas can, for example, prevent entry of moisture or the like into the oxide semiconductor layer **230** as much as possible.

[0466] By the heat treatment, impurities such as carbon, hydrogen, and water in the oxide semiconductor layer **230** can be reduced. Impurities in the film are reduced in this manner, whereby the crystallinity of the oxide semiconductor layer **230** can be improved and a highly dense structure

can be obtained. Accordingly, the crystal region in the oxide semiconductor layer **230** can be increased, and an in-plane variation in the crystal region in the oxide semiconductor layer **230** can be reduced. Thus, in-plane variation in the electrical characteristics of the transistors can be reduced.

[0467] In the case where the second insulating film in the insulating layer **225** contains oxygen, oxygen is preferably supplied from an insulating layer containing the oxygen to the channel formation region of the oxide semiconductor layer **230** by the heat treatment. Accordingly, oxygen vacancies and V.sub.OH can be reduced.

[0468] As described above, excess oxygen is sometimes supplied from the insulating layer in contact with the oxide semiconductor layer **230** to the oxide semiconductor layer **230**. Since excess oxygen has a function of trapping electrons, a negative charge is likely to be formed. Accordingly, the threshold voltage of the transistor can be shifted positively to enable the transistor to have normally-off characteristics.

[0469] Note that microwave plasma treatment may be performed after formation of the second oxide semiconductor film or the third oxide semiconductor film. The microwave plasma treatment can reduce the concentration of impurities such as hydrogen and water contained in the oxide semiconductor layer **230**. In addition, the crystal region of the oxide semiconductor layer **230** grows in some cases. The details of the microwave plasma treatment will be described in Embodiment 2.

[0470] Next, as illustrated in FIGS. **38**A to **38**C, the oxide semiconductor film **230***f* is processed into an island shape to expose part of the top surface of the conductive film **240***f***2** and part of the top surface of the insulating layer **186** at a position overlapping with the opening portion **290**. Through this processing, the oxide semiconductor layer **230***a* and the oxide semiconductor layer **230***b* are formed.

[0471] As illustrated in FIGS. **38**A to **38**C, the above processing is preferably performed so that only the top surface of the insulating layer **186** and the insulating layer **225** are exposed in the opening portion **290**. In other words, the processing is preferably performed so that the conductive layer **220***a* and the conductive layer **220***b* are not exposed in the opening portion **290**. Accordingly, only the insulating layer **186** serves as a base film at the time of the above processing, in which case the oxide semiconductor film **230***f* can be processed relatively easily.

[0472] In order to remove impurities and the like attached to the surface of the oxide semiconductor layer **230** in the processing, cleaning treatment is preferably performed. Examples of the cleaning method include wet cleaning using a cleaning solution or the like (which can also be referred to as wet etching treatment), plasma treatment using plasma, and cleaning by heat treatment, and any of these cleaning methods may be combined as appropriate.

[0473] The wet cleaning may be performed using an aqueous solution in which one or more of ammonia water, oxalic acid, phosphoric acid, and hydrofluoric acid are diluted with carbonated water or pure water. The wet cleaning may be performed using pure water, carbonated water, or the like. Alternatively, ultrasonic cleaning using such an aqueous solution, pure water, or carbonated water may be performed, or such cleaning methods may be performed in combination as appropriate.

[0474] Note that in this specification and the like, in some cases, an aqueous solution in which hydrofluoric acid is diluted with pure water or carbonated water is referred to as diluted hydrofluoric acid, and an aqueous solution in which ammonia water is diluted with pure water is referred to as diluted ammonia water. The concentration, temperature, and the like of the aqueous solution are adjusted as appropriate in accordance with an impurity to be removed, the structure of a semiconductor device to be cleaned, or the like. The concentration of ammonia in the diluted ammonia water is preferably higher than or equal to 0.01% and lower than or equal to 5%, further preferably higher than or equal to 0.1% and lower than or equal to 0.5%. The concentration of hydrogen fluoride in the diluted hydrofluoric acid is preferably higher than or equal to 0.01 ppm

and lower than or equal to 100 ppm, further preferably higher than or equal to 0.1 ppm and lower than or equal to 10 ppm.

[0475] A frequency greater than or equal to 200 kHz is preferably used for the ultrasonic cleaning, and a frequency greater than or equal to 900 kHz is further preferably used. Employing such a frequency can reduce damage to the oxide semiconductor layer **230** and the like.

[0476] The cleaning treatment may be performed multiple times, and the cleaning solution may be changed in every cleaning treatment. For example, the first cleaning treatment may use diluted hydrofluoric acid or diluted ammonia water and the second cleaning treatment may use pure water or carbonated water.

[0477] Next, as illustrated in FIGS. **39**A to **39**C, the conductive film **240***f* is processed to form the conductive layer **240***a* (the conductive layers **240***a***1** and **240***a***2**) and the conductive layer **240***b* (the conductive layers **240***b***1** and **240***b***2**). Specifically, the conductive layers **240***a***2** and the **240***b***2** are formed from the conductive film **240***f***2**, and the conductive layers **240***a***1** and **240***b***1** are formed from the conductive film **240***f***1**.

[0478] Next, as illustrated in FIGS. **40**A to **40**C, the insulating layer **250** is formed to cover the opening portion **290**. The insulating layer **250** is provided in contact with the oxide semiconductor layer **230**. The insulating layer **250** is formed in the opening portion **290** having a high aspect ratio. Thus, the insulating layer **250** is preferably formed by a film formation method that provides favorable coverage, further preferably formed by a CVD method, an ALD method, or the like.

[0479] After formation of the insulating layer **250**, microwave plasma treatment is preferably performed. The microwave plasma treatment can reduce the concentration of impurities such as hydrogen and water contained in the oxide semiconductor layer **230**. In addition, the crystal region of the oxide semiconductor layer **230** grows in some cases. The details of the microwave plasma treatment will be described in Embodiment 2.

[0480] In the case where the insulating layer **250** has the four-layer structure of the fourth insulating layer, the third insulating layer over the fourth insulating layer, the first insulating layer over the third insulating layer, and the second insulating layer over the first insulating layer, microwave plasma treatment may be performed after formation of the third insulating layer. Furthermore, microwave plasma treatment may be performed again after formation of the first insulating layer. As described above, the microwave plasma treatment in an oxygen-containing atmosphere may be performed multiple times (at least twice).

[0481] After formation of the third insulating layer, oxygen may be supplied to the third insulating layer. Accordingly, oxygen can be supplied to the oxide semiconductor layer **230**. The above description can be referred to for the details of the treatment for supplying oxygen. In this embodiment, as the insulating layer **250**, an aluminum oxide film, a silicon oxide film, a hafnium oxide film, and a silicon nitride film are formed in this order by an ALD method.

[0482] Next, as illustrated in FIGS. **41**A to **41**C, the conductive layer **260** is formed over the insulating layer **250**. The conductive layer **260** is preferably provided to fill the opening portion **290**.

[0483] The conductive layer **260** is formed in the opening portion **290** having a high aspect ratio. Thus, the conductive layer **260** is preferably formed by a film formation method that provides favorable coverage, further preferably formed by a CVD method, an ALD method, or the like.

[0484] Through the above steps, the semiconductor device of one embodiment of the present invention can be manufactured.

[0485] This embodiment can be combined with any of the other embodiments as appropriate. In this specification, in the case where a plurality of structure examples are shown in one embodiment, the structure examples can be combined as appropriate.

Embodiment 2

[0486] In this embodiment, an oxide semiconductor layer that can be used as a semiconductor layer of a transistor will be described. As the oxide semiconductor layer of one embodiment of the

present invention, a single layer or stacked layers including a metal oxide can be used. Note that in an oxide semiconductor layer having a stacked-layer structure, a boundary between stacked films is sometimes difficult to observe as described later.

[Metal Oxide]

[0487] The metal oxide of one embodiment of the present invention preferably contains at least indium (In) or zinc (Zn), particularly preferably contains indium as its main component. The metal oxide preferably contains two or three selected from indium, an element M, and zinc, and particularly preferably contains indium and zinc as its main components. Here, the metal oxide contains indium and zinc as its main components, and can further contain the element M. The element M is a metal element or a metalloid element that has a high bonding energy with oxygen, e.g., a metal element or a metalloid element whose bonding energy with oxygen is higher than that of indium. Specific examples of the element M include aluminum, gallium, tin, yttrium, titanium, vanadium, chromium, manganese, iron, cobalt, nickel, zirconium, molybdenum, hafnium, tantalum, tungsten, lanthanum, cerium, neodymium, magnesium, calcium, strontium, barium, boron, silicon, germanium, and antimony. The element M included in the metal oxide is preferably one or more of the above elements, further preferably one or more selected from aluminum, gallium, tin, and yttrium, still further preferably one or more selected from gallium and tin. When the element M included in the metal oxide is gallium, the metal oxide of one embodiment of the present invention preferably includes one or more selected from indium, gallium, and zinc. In this specification and the like, a metal element and a metalloid element may be collectively referred to as a “metal element”, and a “metal element” in this specification and the like may include a metalloid element.

[0488] Examples of the metal oxide of one embodiment of the present invention include indium zinc oxide (also referred to as In—Zn oxide or IZO (registered trademark)), indium tin oxide (also referred to as In—Sn oxide or ITO), indium titanium oxide (In—Ti oxide), indium gallium oxide (In—Ga oxide), indium gallium aluminum oxide (In—Ga—Al oxide), indium gallium tin oxide (also referred to as In—Ga—Sn oxide or IGTO), indium aluminum zinc oxide (also referred to as In—Al—Zn oxide or IAZO), indium tin zinc oxide (also referred to as In—Sn—Zn oxide), indium titanium zinc oxide (In—Ti—Zn oxide), indium gallium zinc oxide (also referred to as In—Ga—Zn oxide or IGZO), indium tin oxide containing silicon (ITSO), indium gallium tin zinc oxide (also referred to as In—Ga—Sn—Zn oxide or IGZTO), and indium gallium aluminum zinc oxide (also referred to as In—Ga—Al—Zn oxide, IGAZO, or IAGZO). Alternatively, it is possible to use, for example, gallium zinc oxide (also referred to as Ga—Zn oxide or GZO), aluminum zinc oxide (also referred to as Al—Zn oxide or AZO), gallium tin oxide (Ga—Sn oxide), or aluminum tin oxide (Al—Sn oxide). As the metal oxide of one embodiment of the present invention, indium oxide can be used. Alternatively, as the metal oxide of one embodiment of the present invention, gallium oxide, zinc oxide, or the like can be used.

[0489] When the indium content percentage in the metal oxide is increased, the transistor can have a high on-state current and excellent frequency characteristics.

[0490] Instead of indium, the metal oxide may contain one or more kinds of metal elements with a large period number in the periodic table. Alternatively, in addition to indium, the metal oxide may contain one or more kinds of metal elements with a large period number in the periodic table. The larger the overlap between orbits of metal elements is, the more likely it is that the metal oxide will have high carrier conductivity. Thus, when a metal element with a large period number in the periodic table is contained in the metal oxide, the field-effect mobility of the transistor can be increased in some cases. Examples of the metal element with a large period number in the periodic table include metal elements belonging to Period **5** and metal elements belonging to Period **6**. Specific examples of the metal element include yttrium, zirconium, silver, cadmium, tin, antimony, barium, lead, bismuth, lanthanum, cerium, praseodymium, neodymium, promethium, samarium, and europium. Incidentally, lanthanum, cerium, praseodymium, neodymium, promethium, samarium, and europium are called light rare-earth elements.

[0491] The metal oxide may contain one or more kinds selected from nonmetallic elements. A transistor including the metal oxide containing a nonmetallic element can have high field-effect mobility in some cases. Examples of the nonmetallic element include carbon, nitrogen, phosphorus, sulfur, selenium, fluorine, chlorine, bromine, and hydrogen.
[0492] A metal oxide having a high zinc content percentage has high crystallinity, whereby diffusion of impurities in the metal oxide can be inhibited. Consequently, a change in electrical characteristics of the transistor is suppressed, and the transistor can have high reliability.
[0493] A high content percentage of the element M in a metal oxide can inhibit formation of oxygen vacancies in the metal oxide. Accordingly, generation of carriers due to oxygen vacancies is inhibited, which makes the off-state current of the transistor low. Furthermore, changes in the electrical characteristics of the transistor can be reduced to improve the reliability of the transistor.
[0494] Here is described a structure example of an oxide semiconductor layer that enables the field-effect mobility of a transistor to be increased. For example a stacked-layer structure of indium oxide and IGZO is preferably used. Specifically, the oxide semiconductor layer preferably contains indium oxide and IGZO over the indium oxide. Moreover, IGZO containing nitrogen is preferably used as the oxide semiconductor layer. For example, IGZO containing nitrogen can be formed by performing N.sub.2O plasma treatment during or after the deposition of IGZO. For the oxide semiconductor layer, at least one of indium oxide, In—Ga oxide, In—Zn oxide, and IGZTO is preferably used.
[0495] In this embodiment, In-M-Zn oxide is sometimes described as an example of the metal oxide.
[0496] The oxide semiconductor layer of one embodiment of the present invention preferably includes a metal oxide having crystallinity. Examples of the structure of a metal oxide having crystallinity include a c-axis-aligned crystalline (CAAC) structure, a polycrystalline structure, and a nanocrystalline (nc) structure. By using a metal oxide having crystallinity for the oxide semiconductor layer, the density of defect states in the oxide semiconductor layer can be reduced. This can improve the reliability of a transistor including the oxide semiconductor layer of one embodiment of the present invention, thereby improving the reliability of a semiconductor device including the transistor.
[0497] Note that there is no particular limitation on the crystallinity of the metal oxide included in the oxide semiconductor layer. The oxide semiconductor layer sometimes includes, for example, at least one of an amorphous semiconductor (a semiconductor having an amorphous structure), a single crystal semiconductor (a semiconductor having a single crystal structure), and a semiconductor having crystallinity other than single crystal (a microcrystalline semiconductor, a polycrystalline semiconductor, or a semiconductor partly including crystal regions). The oxide semiconductor layer having crystallinity can inhibit deterioration of the transistor characteristics in some cases.
[0498] The crystallinity of the oxide semiconductor layer can be analyzed with an X-ray diffraction (XRD) pattern, a transmission electron microscope (TEM) image, or an electron diffraction (ED) pattern, for example. Alternatively, these methods may be combined to be employed for analysis.
[0499] The oxide semiconductor layer of one embodiment of the present invention preferably includes a metal oxide having a CAAC structure. The CAAC structure is a crystal structure where a plurality of microcrystals (typically, a plurality of microcrystals each having a hexagonal crystal structure) have c-axis alignment and are connected on the a-b plane without alignment. According to a high-resolution TEM image (also referred to as a multi-wavelength interference image) of a cross section of an oxide semiconductor layer having the CAAC structure, metal atoms are arranged in a layered manner in crystal parts. Thus, the oxide semiconductor layer having the CAAC structure can be regarded as having a structure including the layered crystal parts.
[0500] The CAAC structure is formed such that the c-axis is perpendicular or substantially perpendicular to a formation surface or a surface of an oxide semiconductor layer, for example. In

the CAAC structure, metal atoms are arranged in a layered manner in the direction parallel or substantially parallel to the formation surface. In a region having the CAAC structure, an angle subtended by the c-axis and the formation surface is preferably within 90°±20° (greater than or equal to 70° and less than or equal to 110°), further preferably within 90°±15° (greater than or equal to 75° and less than or equal to 105°), still further preferably within 90°±10° (greater than or equal to 80° and less than or equal to 100°), yet further preferably within 90°±5° (greater than or equal to 85° and less than or equal to 95°).

[0501] In the case where the oxide semiconductor layer has the CAAC structure, a group of bright spots (specifically, bright spots arranged in a layered manner) reflecting a layered arrangement of metal atoms is observed in a cross-sectional TEM image of the oxide semiconductor layer. Specifically, a state where bright spots are arranged in a layered manner in the direction parallel or substantially parallel to the formation surface is observed.

[0502] When the oxide semiconductor layer having the CAAC structure is subjected to electron diffraction, spots indicating c-axis alignment (bright spots) are observed in the electron diffraction pattern.

[0503] A fast Fourier transform (FFT) pattern obtained by FFT processing on a TEM image reflects reciprocal lattice space information similar to that of an electron diffraction pattern.

[0504] When the cross-sectional TEM image of the oxide semiconductor layer having the CAAC structure is obtained and each region in the cross-sectional TEM image is subjected to FFT processing to form an FFT pattern, the crystal axis direction in each region can be calculated from the obtained FFT pattern. Specifically, the direction of a line segment connecting two spots that have high luminance and are at substantially the same distance from the center, among spots observed in the obtained FFT pattern, is referred to as a crystal axis direction. A region in which an angle subtended by the crystal axis direction calculated from the FFT pattern and the formation surface is preferably greater than or equal to 70° and less than or equal to 110° (within 90°±20°), further preferably greater than or equal to 75° and less than or equal to 105° (within 90°±15°), still further preferably greater than or equal to 80° and less than or equal to 100° (within 90°±10°), yet further preferably greater than or equal to 85° and less than or equal to 95° (within 90°±5°) can be regarded as having the CAAC structure.

[0505] When the oxide semiconductor layer having the CAAC structure is observed from the direction perpendicular to the formation surface by using the TEM image, a triangular or hexagonal atomic arrangement and crystallinity are observed in the a-b plane.

[Composition of Metal Oxide]

[0506] The metal oxide of one embodiment of the present invention preferably contains indium (In), and further preferably has a high In content percentage. The use of a metal oxide having a high In content percentage as the oxide semiconductor layer can increase the on-state current of the transistor and improve the frequency characteristics of the transistor. For example, indium oxide is preferably used as the oxide semiconductor layer.

[0507] The metal oxide of one embodiment of the present invention can contain zinc. The metal oxide containing zinc has high crystallinity, e.g., has the CAAC structure. For example, In—Zn oxide can be used for the oxide semiconductor layer. Specifically, it is possible to use a metal oxide having an atomic ratio of In:Zn=1:1 or the neighborhood thereof, In:Zn=2:1 or the neighborhood thereof, or In:Zn=4:1 or the neighborhood thereof. Note that the neighborhood of the atomic ratio includes ±30% of an intended atomic ratio.

[0508] The metal oxide of one embodiment of the present invention can contain the element M. When the metal oxide contains the element M, formation of oxygen vacancies in the metal oxide can be inhibited. Thus, the reliability of the transistor including the oxide semiconductor layer can be increased.

[0509] For example, In—Zn oxide containing a slight amount of the element M can be used for the oxide semiconductor layer. Specifically, it is possible to use a metal oxide having an atomic ratio of

In:Ga:Zn=4:0.1:1 or the neighborhood thereof, In:Ga:Zn=2:0.1:1 or the neighborhood thereof, or In:Ga:Zn=1:0.1:1 or the neighborhood thereof. It is also possible to use a metal oxide having an atomic ratio of In:Sn:Zn=4:0.1:1 or the neighborhood thereof, In:Sn:Zn=2:0.1:1 or the neighborhood thereof, or In:Sn:Zn=1:0.1:1 or the neighborhood thereof.

[0510] Moreover, In—Zn oxide containing the element M can be used for the oxide semiconductor layer. Specifically, it is possible to use a metal oxide having an atomic ratio of In:M:Zn=1:1:1 or the neighborhood thereof, In:M:Zn=1:1:1.2 or the neighborhood thereof, In:M:Zn=1:1:0.5 or the neighborhood thereof, In:M:Zn=1:1:2 or the neighborhood thereof, In:M:Zn=4:2:3 or the neighborhood thereof, In:M:Zn=1:3:2 or the neighborhood thereof, or In:M:Zn=1:3:4 or the neighborhood thereof.

[0511] Note that in the case where the metal oxide is formed by a sputtering method, the composition of the formed metal oxide may be different from that of a sputtering target. In particular, the zinc content percentage of the formed metal oxide may be reduced to approximately 50% of that of the sputtering target.

[0512] In the case where a metal oxide containing a plurality of kinds of metal elements, such as In—Ga—Zn oxide, is formed by an ALD method, the cycle ratio of precursors containing the metal elements can be set in accordance with a target composition. For example, to form an In—Ga—Zn oxide film having an atomic ratio of In:Ga:Zn=1:3:2, it is possible to perform one cycle of deposition using a precursor containing In and treatment with an oxidizer, three cycles of deposition using a precursor containing Ga and treatment with an oxidizer, and two cycles of deposition using a precursor containing Zn and treatment with an oxidizer. Note that the atomic ratio of the metal elements in the formed metal oxide film does not sometimes correspond with the cycle ratio of the precursors containing the metal elements.

[0513] Analysis of the composition of the metal oxide used for the oxide semiconductor layer can be performed by energy dispersive x-ray spectroscopy (EDX), XPS, inductively coupled plasma-mass spectrometry (ICP-MS), or inductively coupled plasma-atomic emission spectrometry (ICP-AES), for example. Alternatively, these methods may be combined to be employed for analysis. As for an element whose content percentage is low, the actual content percentage may be different from the content percentage obtained by analysis because of the influence of the analysis accuracy. For example, in the case where the content percentage of the element M is low, the content percentage of the element M obtained by analysis may be lower than the actual content percentage, quantification of the content percentage of the element M may become difficult, or the element M may be lower than the detection limit in some cases.

[0514] The oxide semiconductor layer of one embodiment of the present invention may have a stacked-layer structure of two or more layers. In the case where the oxide semiconductor layer has a two-layer structure of a first layer and a second layer over the first layer, the composition of the second layer is preferably different from that of the first layer. In the case where the oxide semiconductor layer has a three-layer structure of a first layer, a second layer over the first layer, and a third layer over the second layer, the composition of the second layer is preferably different from those of the first and third layers. Note that the composition of the first layer can be the same as that of the third layer. Alternatively, the first and third layers can have different compositions.

[0515] For each of the first to third layers, the above-described metal oxide can be used.

[0516] For the second layer, indium oxide, In—Zn oxide, In—Zn oxide containing a slight amount of the element M, or the like can be used, for example. Specifically, it is possible to use a metal oxide having an atomic ratio of In:Zn=1:1 or the neighborhood thereof, In:Zn=2:1 or the neighborhood thereof, or In:Zn=4:1 or the neighborhood thereof. For example, it is possible to use a metal oxide having an atomic ratio of In:Ga:Zn=4:0.1:1 or the neighborhood thereof, In:Ga:Zn=2:0.1:1 or the neighborhood thereof, or In:Ga:Zn=1:0.1:1 or the neighborhood thereof. As another example, it is possible to use a metal oxide having an atomic ratio of In:Sn:Zn=4:0.1:1 or the neighborhood thereof, In:Sn:Zn=2:0.1:1 or the neighborhood thereof, or In:Sn:Zn=1:0.1:1 or

the neighborhood thereof. Increasing the content percentage of In in the second layer can increase the on-state current and improve the frequency characteristics.

[0517] The conduction band minimum of each of the first and third layers is preferably positioned closer to the vacuum level than the conduction band minimum of the second layer is. In other words, the energy of the conduction band minimum of each of the first and third layers is preferably lower than the energy of the conduction band minimum of the second layer. In this case, the second layer is sandwiched between the first layer and the third layer, each of which has a conduction band minimum positioned closer to the vacuum level, and can function mainly as a current path (channel).

[0518] When the second layer is sandwiched between the first layer and the third layer, carriers trapped at and near the interfaces between the second layer and each of the first and third layers can be reduced. Moreover, the channel can be distanced from the surface of a gate insulating layer, so that the influence of surface scattering can be reduced. Accordingly, a buried-channel transistor where a channel is distanced from the interface with an insulating layer can be achieved, whereby the field-effect mobility can be increased. Furthermore, the influence of interface states that may be formed on the back gate electrode side (or the back channel side) of the oxide semiconductor layer is reduced, so that light deterioration (e.g., light negative bias deterioration) of the transistor can be inhibited and the reliability of the transistor can be increased.

[0519] For example, a band diagram of the oxide semiconductor layer **230** including the oxide semiconductor layers **230***a***1** to **230***a***3** and its vicinity illustrated in FIG. **13**B is as shown in FIG. **42**. In FIG. **42**, the vertical axis represents energy and the horizontal direction represents the thickness direction of a center portion of a channel formation region. FIG. **42** shows a valence band maximum (VBM) and a conduction band minimum (CBM) of each of the oxide semiconductor layers **230***a***1** to **230***a***3** and the insulating layers **225** and **250** in a state where no voltage is applied between the gate and the source. In FIG. **42**, a vacuum level Vac is denoted by a dashed line.

[0520] Note that energy of the valence band maximum and energy of the conduction band minimum change depending on constituent elements and compositions of the oxide semiconductor layers **230***a***1** to **230***a***3** and the insulating layers **225** and **250**; thus, the relation between energy levels of the valence band maximum and the relation between energy levels of the conduction band minimum are mainly described with reference to the band diagram in FIG. **42**.

[0521] With certain constituent elements and compositions of the oxide semiconductor layers **230***a***1** to **230***a***3**, the oxide semiconductor layer **230***a***2** is sandwiched between the oxide semiconductor layers **230***a***1** and **230***a***3** each of which has a conduction band minimum that is positioned closer to the vacuum level than that of the oxide semiconductor layer **230***a***2** is, as shown in FIG. **42**. This structure enables a buried channel. That is, in this structure, a path through which a larger amount of current (electrons are shown as carriers in FIG. **42**) flows is formed in the oxide semiconductor layer **230***a***2**. Accordingly, the on-state current or reliability can be increased. for example.

[0522] In the case where a buried channel is formed using the first to third layers, a metal oxide having a higher Ga content percentage than that for the second layer can be used for the first and third layers, for example. Specifically, for each of the first and third layers, it is possible to use a metal oxide having an atomic ratio of In:Ga:Zn=1:1:1 or the neighborhood thereof, In:Ga:Zn=1:3:2 or the neighborhood thereof, or In:Ga:Zn=1:3:4 or the neighborhood thereof. Alternatively, Ga—Zn oxide or gallium oxide can be used. When the Ga content percentage in the first and third layers is increased, the conduction band minimum of each of the first and third layers is sometimes positioned closer to the vacuum level than the conduction band minimum of the second layer is.

[0523] Increasing the Ga content percentage in the first and third layers can improve the barrier property against hydrogen in the first and third layers. Thus, diffusion of hydrogen into the second layer from below the first layer or above the third layer can be inhibited. In addition, increasing the Ga content percentage in the first and third layers enables impurities such as hydrogen and water

contained in the oxide semiconductor layer to be reduced by heat or the like applied after formation of the oxide semiconductor layer. Note that when a metal oxide having a lower In content percentage than that for the second layer is used for the first and third layers, a similar effect can be obtained in some cases.

[0524] For the third layer, it is preferable to use a metal oxide having an atomic ratio of In:Ga:Zn=1:1:1 or the neighborhood thereof, In:Ga:Zn=1:3:2 or the neighborhood thereof, or In:Ga:Zn=1:3:4 or the neighborhood thereof, for example. In this case, the third layer contains indium and gallium.

[0525] Increasing the Ga content percentage in the first and third layers can improve the barrier property against oxygen of the first and third layers. Thus, release of oxygen from the second layer where the channel is formed is inhibited, thereby inhibiting formation of oxygen vacancies in the second layer or an increase in the amount of oxygen vacancies in the second layer. Accordingly, the transistor can have favorable electrical characteristics.

[0526] When the Ga content percentage in the first layer is increased, the resistivity of the first layer can be higher than that of the second layer in some cases. In the case where the first layer is provided on the back channel side, providing a layer having high resistivity as the first layer can inhibit a negative shift of the threshold voltage or a decrease in the on-state current. Accordingly, the threshold voltage of the transistor shifts positively, so that the transistor can have normally-off characteristics. In the above manner, the electrical characteristics and reliability of the transistor can be improved.

[0527] The band gap of the metal oxide can be evaluated using optical evaluation with a spectrophotometer, spectroscopic ellipsometry, a photoluminescence method, X-ray photoelectron spectroscopy, or an X-ray absorption fine structure (XAFS). Alternatively, these methods can be combined as appropriate for analysis. The electron affinity or the conduction band minimum can be obtained from a band gap and an ionization potential, which is a difference in energy between the vacuum level and the valence band maximum. The ionization potential can be evaluated by ultraviolet photoelectron spectroscopy (UPS), for example.

[0528] Moreover, a metal oxide having a higher In content percentage than that for the second layer may be used for the first and third layers. Alternatively, a metal oxide having a higher In content percentage than that for the second layer may be used for one of the first and third layers, and a metal oxide having a higher Ga content percentage than that for the second layer may be used for the other.

[0529] Each of the first to third layers may include a stack of a plurality of layers each having the above-described composition. For example, the first layer may have a structure where a metal oxide with a high In content percentage is stacked over a metal oxide with a high Ga content percentage. As another example, the third layer may have a structure where a metal oxide with a high Ga content percentage is stacked over a metal oxide with a high In content percentage.

[Formation Method of Oxide Semiconductor Layer]

[0530] The oxide semiconductor layer of one embodiment of the present invention can be formed by a sputtering method, a chemical vapor deposition (CVD) method, a vacuum evaporation method, a molecular beam epitaxy (MBE) method, a pulsed laser deposition (PLD) method, an ALD method, or the like.

[0531] The oxide semiconductor layer of one embodiment of the present invention can be formed by forming metal oxides using two kinds of formation methods. For example, the oxide semiconductor layer of one embodiment of the present invention can be formed by forming metal oxides using a first formation method and a second formation method.

[0532] The oxide semiconductor layer of one embodiment of the present invention can have a two-layer structure of a first layer and a second layer over the first layer. In the case where the oxide semiconductor layer has a two-layer structure, the oxide semiconductor layer can be formed in the following manner: the first layer is formed over a formation surface by a first formation method,

and then the second layer is formed over the first layer by a second formation method.
[0533] As the first formation method, a formation method that causes less damage to the formation surface than the second formation method is preferably used. Accordingly, formation of a mixed layer at the interface between the oxide semiconductor layer and a layer over which the oxide semiconductor layer is formed (the formation surface of the oxide semiconductor layer) can be inhibited. Moreover, entry of impurities such as silicon into the second layer formed over the first layer can be inhibited, so that the crystallinity of the oxide semiconductor layer can be further increased in some cases.
[0534] Examples of the first formation method include an ALD method, a CVD method, and an MBE method. Examples of a CVD method include a plasma enhanced CVD (PECVD) method, a thermal CVD method, a photo CVD method, and an MOCVD method. An MBE method is a film formation method by which a thin film having a crystal structure reflecting a crystal system of a substrate is grown, and is one of film formation methods that cause less damage to a formation surface. A wet method can be used as the first formation method. A wet method is one of film formation methods that cause less damage to a formation surface. An example of a wet method is a spray coating method.
[0535] As the second formation method, a method that enables formation of a metal oxide having crystallinity is preferably used. The metal oxide formed at this time particularly preferably has the CAAC structure. Examples of the second formation method include a sputtering method and a PLD method. A metal oxide formed by a sputtering method is likely to have crystallinity; thus, a sputtering method is suitable as the second formation method.
[0536] When a metal oxide is formed over the formation surface by the second formation method, damage to the formation surface might cause alloying of a component contained in the metal oxide with a component contained in the layer serving as the formation surface. When alloying occurs, a mixed layer is sometimes formed at the interface between the metal oxide and the layer serving as the formation surface. The mixed layer can also be referred to as an alloyed region. The formation of the mixed layer can also be referred to as alloying.
[0537] For example, in the case where a sputtering method is used as the second formation method, a mixed layer is sometimes formed owing to particles ejected from a target or the like (also referred to as sputtered particles) or energy applied to the substrate side by sputtered particles or the like, for example. Specifically, in the case where a metal oxide is formed over an insulating layer containing silicon, e.g., a silicon oxide film as the formation surface by the second formation method, silicon might enter the metal oxide. There is a concern that the entry of impurities such as silicon into the metal oxide may hinder crystallization of the metal oxide. When an oxide semiconductor layer into which impurities enter is used for a transistor, the initial characteristics or reliability of the transistor may be adversely affected. It is difficult to increase the crystallinity of an alloyed region even when heat treatment described later is performed.
[0538] Accordingly, forming the metal oxide by the first formation method before forming the metal oxide by the second formation method as described above can inhibit entry of impurities into the oxide semiconductor layer. In addition, alloying with the layer serving as the formation surface can be inhibited. Thus, the initial characteristics and reliability of the transistor can be improved. Moreover, the crystallinity of the oxide semiconductor layer can be further increased.
[0539] In addition, a mixed layer is sometimes formed at the interface between the first layer and the second layer. The mixed layer includes a component contained in the first layer and a component contained in the second layer. For example, in the case where gallium oxide is used for the first layer and a metal oxide containing indium is used for the second layer, the mixed layer includes gallium and indium. For example, in the case where the indium content percentage of the second layer is higher than that of the first layer, the indium content percentage of the mixed layer is higher than or equal to that of the first layer and lower than or equal to that of the second layer.
[0540] An ALD method is suitable as the first formation method because damage to the formation

surface can be inhibited as compared with a sputtering method. An ALD method is a film formation method that gives higher coverage than a sputtering method, and the use of an ALD method as the formation method of the first layer can increase the coverage with the oxide semiconductor layer. Thus, the oxide semiconductor layer can suitably cover a step, an opening portion, or the like having a high aspect ratio.

[0541] As the first layer, a metal oxide having a microcrystalline structure or an amorphous structure that has lower crystallinity than the CAAC structure is formed in some cases, for example. Forming the second layer having high crystallinity on the first layer having low crystallinity or performing heat treatment after formation of the second layer can increase the crystallinity of the first layer with the second layer as a nucleus in some cases. Accordingly, in some cases, the crystallinity can be increased in the whole oxide semiconductor layer including the vicinity of the interface with the formation surface.

[0542] The layer serving as the formation surface is an insulating film such as a silicon oxide film, a silicon oxynitride film, a silicon nitride film, a silicon nitride oxide film, an aluminum oxide film, or a hafnium oxide film, for example. In addition, the layer serving as the formation surface may be a conductive film such as a titanium nitride film, a tungsten film, or an ITSO film in some transistor structures. The layer serving as the formation surface does not necessarily have crystallinity. In the case of having crystallinity, the layer serving as the formation surface may have a crystal structure with low lattice matching with the metal oxide included in the oxide semiconductor layer.

[0543] The first layer is preferably formed by an ALD method. Here, a method for forming In-M-Zn oxide for the first layer by an ALD method is described.

[0544] First, a source gas that contains a precursor containing indium is introduced into a reaction chamber (also referred to as a chamber) so that the precursor is adsorbed on the formation surface. Then, an oxidizer is introduced as a reactant into the reaction chamber to react with the adsorbed precursor, and components other than indium are released while indium is adsorbed on the substrate, whereby a layer in which indium and oxygen are bonded to each other is formed.

[0545] Subsequently, a source gas that contains a precursor containing the element M is introduced into the reaction chamber, and the precursor is adsorbed on the layer in which indium and oxygen are bonded to each other. Then, an oxidizer is introduced as a reactant into the reaction chamber to react with the adsorbed precursor, and components other than the element M are released while the element M is adsorbed on the substrate, whereby a layer in which the element M and oxygen are bonded to each other is formed.

[0546] Next, a source gas that contains a precursor containing zinc is introduced into the reaction chamber, and the precursor is adsorbed on the layer in which the element M and oxygen are bonded to each other. Then, an oxidizer is introduced as a reactant into the reaction chamber to react with the adsorbed precursor, and components other than zinc are released while zinc is adsorbed on the substrate, whereby a layer in which zinc and oxygen are bonded to each other is formed.

[0547] By repeating the above steps, In-M-Zn oxide can be formed by an ALD method as the oxide semiconductor layer over the layer serving as the formation surface.

[0548] When the oxide semiconductor layer is formed by an ALD method, ozone (O.sub.3), oxygen (O.sub.2), water (H.sub.2O), or the like can be used as the oxidizer. The use of an oxidizer without hydrogen, such as ozone (O.sub.3) or oxygen (O.sub.2), can reduce the amount of hydrogen entering the oxide semiconductor layer.

[0549] It is preferable that after the precursor is adsorbed in the above steps, introduction of the source gas containing the precursor be stopped and the reaction chamber be purged so that an excess precursor, a reaction product, and the like are removed from the reaction chamber. Moreover, it is preferable that after the adsorbed precursor reacts with the oxidizer in the above steps, introduction of the oxidizer be stopped and the reaction chamber be purged so that an excess reactant, a reaction product, and the like are removed from the reaction chamber.

[0550] In the description of this specification and the like, ozone, oxygen, and water that can be used as a reactant or an oxidizer include not only those in gas or molecular states but also those in plasma, radical, and ion states, unless otherwise specified.
[0551] The second layer is preferably formed by a sputtering method.
[0552] As a target used in a sputtering method, In-M-Zn oxide can be used. In the case where a metal oxide is formed by a sputtering method, oxygen or a mixed gas of oxygen and a noble gas can be used as a sputtering gas. An increase in the proportion of oxygen in the sputtering gas can increase the amount of excess oxygen in the oxide film to be formed.
[0553] A higher proportion of the flow rate of an oxygen gas to the flow rate of the whole film formation gas (also referred to as oxygen flow rate ratio) used at the time of forming the metal oxide enables the formed metal oxide to have higher crystallinity in some cases.
[0554] When the metal oxide is formed by a sputtering method and the proportion of oxygen in the sputtering gas is higher than 30% and lower than or equal to 100%, preferably higher than or equal to 70% and lower than or equal to 100%, an oxygen-excess metal oxide is formed in some cases. A transistor including an oxygen-excess metal oxide in a channel formation region can have relatively high reliability. However, one embodiment of the present invention is not limited thereto. When the proportion of oxygen in the sputtering gas is higher than or equal to 1% and lower than or equal to 30%, preferably higher than or equal to 5% and lower than or equal to 20%, an oxygen-deficient metal oxide is formed. A transistor including an oxygen-deficient metal oxide in a channel formation region can have relatively high field-effect mobility.
[0555] In the formation of the metal oxide by a sputtering method, substrate heating is preferably performed. Increasing the substrate temperature (e.g., stage temperature) at the time of forming the metal oxide enables a metal oxide with high crystallinity to be formed in some cases. In the formation of the metal oxide by a sputtering method, the substrate heating temperature is preferably higher than or equal to 100° C. and lower than or equal to 400° C., further preferably higher than or equal to 200° C. and lower than or equal to 300° C., for example.
[0556] With the above-described formation method, the thickness of the mixed layer formed at the interface between the layer serving as the formation surface and the metal oxide can be reduced or the thickness of the alloyed region formed at the interface between the layer serving as the formation surface and the metal oxide can be thin enough to be unobserved. For example, the thickness of the alloyed region can be greater than or equal to 0 nm and less than or equal to 3 nm, preferably greater than or equal to 0 nm and less than or equal to 2 nm, further preferably greater than or equal to 0 nm and less than or equal to 1 nm, still further preferably greater than or equal to 0 nm and less than 0.3 nm.
[0557] The thickness of the alloyed region can sometimes be calculated by performing SIMS or composition line analysis by EDX on the region and its vicinity.
[0558] For example, EDX line analysis is performed on the alloyed region and its vicinity with the direction perpendicular to the formation surface of the first layer regarded as the depth direction. Next, in the profile of quantitative values of the elements in the depth direction, which is obtained from the analysis, the depth at which the quantitative value of a metal (In when the first layer contains In) that is the main component of the first layer and that is not the main component of the layer serving as the formation surface becomes half is defined as the depth (position) of the interface between the region and the first layer. The depth at which the quantitative value of an element (e.g., Si) that is a main component of the layer serving as the formation surface and that is not a main component of the first layer becomes half is defined as the depth (position) of the interface between the region and the layer serving as the formation surface. In the above manner, the thickness of the alloyed region can be calculated.
[0559] When the thickness of the alloyed region in the oxide semiconductor layer of one embodiment of the present invention is observed by EDX analysis, the thickness is greater than or equal to 0 nm and less than or equal to 3 nm, preferably greater than or equal to 0 nm and less than

or equal to 2 nm, further preferably greater than or equal to 0 nm and less than or equal to 1 nm, still further preferably greater than or equal to 0 nm and less than 0.3 nm, for example.
[0560] For example, when SIMS analysis is performed on the oxide semiconductor layer formed over a silicon oxide film serving as the formation surface, the depth at which the silicon concentration is 50% of the maximum value of the silicon concentration in the silicon oxide film is defined as an interface, and the distance between the interface and the depth at which the silicon concentration decreases to 1.0×10.sup.21 atoms/cm.sup.3, preferably 5.0×10.sup.20 atoms/cm.sup.3, further preferably 1.0×10.sup.20 atoms/cm.sup.3 is defined as a thickness t. The thickness t is preferably less than or equal to 3 nm, further preferably less than or equal to 2 nm.
[0561] When the thickness of the alloyed region is reduced, the thickness t can be a value within the above range.
[0562] When the thickness of the alloyed region is reduced, the CAAC structure can be formed in the vicinity of the formation surface. Here, the vicinity of the formation surface refers to, for example, a region ranging from the formation surface of the oxide semiconductor layer to greater than 0 nm and less than or equal to 3 nm, preferably greater than 0 nm and less than or equal to 2 nm, further preferably greater than or equal to 1 nm and less than or equal to 2 nm in the direction substantially perpendicular to the formation surface.
[0563] Note that the CAAC structure in the vicinity of the formation surface can be confirmed in TEM observation in some cases. For example, in high-resolution TEM cross-sectional observation of the oxide semiconductor layer, bright spots arranged in a layered manner in the direction parallel to the formation surface are observed in the vicinity of the formation surface.
[0564] The oxide semiconductor layer of one embodiment of the present invention can have a three-layer structure of a first layer, a second layer over the first layer, and a third layer over the second layer.
[0565] In the case where the oxide semiconductor layer has a three-layer structure, the oxide semiconductor layer can be formed in the following manner: the first layer is formed over a formation surface by a first formation method, the second layer is formed by a second formation method, and then the third layer is formed by the first formation method.
[0566] Even when the first and third layers in the oxide semiconductor layer have a composition that is less likely to form the CAAC structure in the case of a single layer, crystal growth occurring with the second layer as a nucleus enables the whole oxide semiconductor layer including the first and third layers to have the CAAC structure. Alternatively, the oxide semiconductor layer can have the CAAC structure in a region that includes the second layer and at least part of each of the first and third layers.
[0567] In particular, even with a composition where the first and third layers have a high In content percentage, crystallinity suitable for a semiconductor layer of a transistor can be obtained. The oxide semiconductor layer of one embodiment of the present invention can achieve both high on-state characteristics owing to the increase in the In content percentage and high reliability of the transistor owing to the CAAC structure with high crystallinity.
[0568] The first and third layers may employ a metal oxide having the same composition as the second layer. By using the same composition, the oxide semiconductor layer may easily have the CAAC structure after heat treatment.
[0569] Since the second layer has high crystallinity, the crystal growth of the third layer can be achieved with the use of the crystal of the second layer as a nucleus or a seed. Thus, the third layer can be crystallized even when a film formation method that easily gives crystallinity is not employed as the formation method of the third layer. Here, for example, when a film formation method that gives higher coverage than that of the second layer is used to form the third layer, the whole oxide semiconductor layer can have both high crystallinity and high coverage.
[0570] When influence of the formation surface on the second layer is reduced by provision of the first layer, the crystallinity of the second layer is increased to an extremely high level. Thus, the

third layer whose crystal is grown with the second layer as a nucleus or a seed is also expected to have extremely excellent crystallinity.

[0571] In addition, in the case where an oxide semiconductor layer is used as a semiconductor layer of a transistor, the third layer, which is the uppermost layer of the oxide semiconductor layer, is in contact with a gate insulating layer in some cases. Increasing the crystallinity of the layer in contact with the gate insulating layer can increase the carrier mobility in an on state of the transistor.

[0572] The crystallinity of the first and third layers is increased with the use of the second layer having high crystallinity as a nucleus or a seed. Specifically, the crystallinity of the first layer may be increased at the time of formation of the second layer or by heat treatment after formation of the third layer. The crystallinity of the third layer may be increased at the time of formation of the third layer or by heat treatment after the formation of the third layer. The heat treatments have a function of assisting in increasing the crystallinity.

[0573] As described above, in the method for forming the oxide semiconductor layer of one embodiment of the present invention, with the use of the second layer including a metal oxide with high crystallinity, (i.e., CAAC), as a nucleus or a seed, the crystallinity of the metal oxides above and below the second layer (here, the first and third layers) can be increased. Accordingly, the crystallinity of the whole oxide semiconductor layer can be increased. In other words, the second layer serves as a nucleus or a seed to cause solid-phase growth of the metal oxides above and below the second layer, so that the oxide semiconductor layer with high crystallinity can be formed. An oxide semiconductor layer formed by such a formation method, here, a CAAC film, can be referred to as an axial growth CAAC (AG CAAC).

[0574] A region having the CAAC structure preferably spreads in the whole the oxide semiconductor layer. Crystals in the region having the CAAC structure in the first layer are connected to crystals in the region having the CAAC structure in the second layer. Crystals in the region having the CAAC structure in the third layer are connected to crystals in the region having the CAAC structure in the second layer. Accordingly, a boundary between the first layer and the second layer is not observed in some cases. In addition, a boundary between the second layer and the third layer is not observed in some cases. The oxide semiconductor layer may be expressed as one layer where interfaces are not clearly observed. The oxide semiconductor layer may be expressed as a single layer.

[0575] In the region having the CAAC structure in each of the first to third layers, bright spots arranged parallel or substantially parallel to the formation surface are observed in a high-resolution cross-sectional TEM image, for example. The c-axis of the CAAC structure included in each of the first to third layers is preferably parallel or substantially parallel to the normal direction of the formation surface or the surface of the oxide semiconductor layer.

[0576] Part of the first layer or the third layer is not crystallized in some cases.

[0577] In the case where the oxide semiconductor layer has a three-layer structure, the oxide semiconductor layer can also be formed in the following manner: a first layer is formed over a formation surface by a first formation method, a second layer is formed by the first formation method, and then a third layer is formed by a second formation method.

[0578] As described above, when a metal oxide with a high In content percentage is used for a transistor, the field-effect mobility of the transistor can be increased. On the other hand, a metal oxide with a high In content percentage tends to have a cubic crystal structure. Thus, when a metal oxide with a high In content percentage is used for the second layer in contact with the third layer, crystals reflecting the orientation of crystals included in the third layer can be formed.

[0579] The lattice mismatch between the crystals included in the third layer and the crystals included in the second layer is preferably small. Thus, crystals reflecting the orientation of the crystals included in the third layer can be formed in the second layer. At this time, for example, in high-resolution cross-sectional TEM observation of the oxide semiconductor layer, bright spots arranged in a layered manner in the direction parallel to the formation surface are observed in the

second layer.
[0580] There is no particular limitation on the crystal structure of the second layer as long as the crystals included in the third layer have a small lattice mismatch with the crystals included in the second layer. The crystal structure of the second layer may be any of a cubic crystal structure, a tetragonal crystal structure, an orthorhombic crystal structure, a hexagonal crystal structure, a monoclinic crystal structure, and a trigonal crystal structure.
[0581] In the above structure, typically, the first layer can be a layer including a metal oxide having an atomic ratio of In:Ga:Zn=1:3:2 or in the neighborhood thereof or a layer including gallium oxide, the second layer can be a layer including a metal oxide containing a slight amount of the element M or a layer including indium oxide, and the third layer can be a layer including a metal oxide having an atomic ratio of In:Ga:Zn=1:1:1 or in the neighborhood thereof. In this case, the first layer contains gallium. In the case where the first layer includes a metal oxide having an atomic ratio of In:Ga:Zn=1:3:2 or in the neighborhood thereof, the indium content percentage is lower than the gallium content percentage in the first layer. The indium content percentage in the second layer is higher than the indium content percentage in the third layer.
[0582] In the case where the first layer and the second layer are formed by the first formation method, the first layer and the second layer are preferably formed successively without exposure to the air. Forming the first layer and the second layer successively without exposure to the air can increase the productivity. Furthermore, impurities (typically, moisture or the like) taken into the interface between the first layer and the second layer and the vicinity thereof can be reduced.
[0583] One or more of the first to third layers may include a stack of a plurality of layers with different compositions. For example, the first layer may be formed in the following manner: a layer including a metal oxide with a high Ga content percentage is formed by the first formation method, and then a layer including a metal oxide with a higher In content percentage than the layer is formed by the first formation method.
[0584] After formation of the layers by the first formation method, microwave plasma treatment is preferably performed.
[0585] In this specification and the like, a microwave refers to an electromagnetic wave having a frequency greater than or equal to 300 MHz and less than or equal to 300 GHz. Microwave plasma treatment refers to, for example, treatment using an apparatus including a power source for generating high-density plasma using microwaves. Microwave plasma treatment can also be referred to as microwave-excited high-density plasma treatment.
[0586] By performing microwave plasma treatment in an oxygen-containing atmosphere, the impurity concentration in the oxide semiconductor layer **230** can be reduced. Specific examples of impurities include hydrogen and carbon. Although the microwave plasma treatment in an oxygen-containing atmosphere is performed on the metal oxide in the above example, one embodiment of the present invention is not limited thereto. For example, microwave plasma treatment in an oxygen-containing atmosphere may be performed on an insulating film, specifically a silicon oxide film, which is provided in the vicinity of the metal oxide. Furthermore, the crystallinity of the oxide semiconductor layer is sometimes increased by heat in the microwave plasma treatment.
[0587] The microwave plasma treatment is preferably performed under a reduced pressure, and the pressure is preferably higher than or equal to 10 Pa and lower than or equal to 1000 Pa, further preferably higher than or equal to 50 Pa and lower than or equal to 700 Pa, still further preferably higher than or equal to 100 Pa and lower than or equal to 400 Pa. The treatment temperature is preferably higher than or equal to room temperature (25° C.) and lower than or equal to 750° C., further preferably higher than or equal to 300° C. and lower than or equal to 500° C., and can be higher than or equal to 400° C. and lower than or equal to 450° C.
[0588] In the microwave plasma treatment, substrate heating may be performed. The substrate heating temperature is preferably higher than or equal to room temperature (e.g., 25° C.), higher than or equal to 100° C., higher than or equal to 200° C., higher than or equal to 300° C., or higher

than or equal to 400° C., and lower than or equal to 500° C. or lower than or equal to 450° C. For example, the substrate heating temperature is preferably higher than or equal to room temperature and lower than or equal to 500° C., further preferably higher than or equal to 100° C. and lower than or equal to 450° C., still further preferably higher than or equal to 200° C. and lower than or equal to 450° C., yet still further preferably higher than or equal to 300° C. and lower than or equal to 450° C., yet still further preferably higher than or equal to 400° C. and lower than or equal to 450° C.

[0589] The microwave plasma treatment can be performed using an oxygen gas and an argon gas, for example. In the microwave plasma treatment using an oxygen gas and an argon gas, oxygen radicals can be mainly in three states: triplet oxygen (O(.sup.3P.sub.j)), singlet oxygen (O(.sup.1D.sub.2)), and an oxygen ion (O.sub.2.sup.+). The oxygen ion effectively acts for reducing the hydrogen concentration in an oxide film by the microwave plasma treatment. The amount of oxygen radicals in each state changes depending on the oxygen flow rate ratio or a pressure in the microwave plasma treatment. For example, the amount of oxygen ions tends to increase under a condition with a low oxygen flow rate ratio and a low pressure. Meanwhile, an extremely low oxygen flow rate ratio or pressure might destabilize the control of the oxygen flow rate, thereby making stable discharging difficult or causing etching of an oxide film, for example. Therefore, for example, the oxygen flow rate ratio (O.sub.2/(O.sub.2+Ar)) in the microwave plasma treatment is preferably higher than 0% and lower than or equal to 10%, further preferably higher than or equal to 0.5% and lower than or equal to 5%, still further preferably higher than or equal to 0.5% and lower than or equal to 3%, and is typically preferably 1%.

[0590] As the microwave plasma treatment time is shorter, oxidation of the conductive layer **220**, the conductive layer **240**, or the like can be inhibited more. In addition, the productivity is improved. In view of this, the microwave plasma treatment time is preferably longer than or equal to 1 minute and shorter than or equal to 60 minutes, further preferably longer than or equal to 1 minute and shorter than or equal to 30 minutes, still further preferably longer than or equal to 1 minute and shorter than or equal to 10 minutes.

[0591] The microwave plasma treatment in an oxygen-containing atmosphere can convert an oxygen gas into plasma by using a high-frequency wave such as a microwave or an RF, and apply, to the oxide semiconductor layer, oxygen radicals that are generated by conversion of the oxygen gas into plasma. By the effects of plasma, a microwave, oxygen radicals, and the like, a defect in which hydrogen enters an oxygen vacancy (also referred to as V.sub.OH in some cases) in the oxide semiconductor layer can be divided into an oxygen vacancy and hydrogen, and hydrogen which is an impurity can be removed from the oxide semiconductor layer. In this manner, V.sub.OH contained in the oxide semiconductor layer can be reduced. At this time, carbon bonded to oxygen, hydrogen, or the like can also be removed in some cases. Performing the microwave plasma treatment in such a manner can reduce impurities such as carbon and hydrogen. Supplying the oxygen radicals to oxygen vacancies formed in the oxide semiconductor layer can further reduce oxygen vacancies in the oxide semiconductor layer.

[0592] The microwave plasma treatment can increase the crystallinity of the layers formed by the first formation method. Here, the principles of improving the crystallinity of the oxide semiconductor layer by the microwave plasma treatment will be described. First, active species excited by a microwave, such as oxygen radicals, reach the surface of the oxide semiconductor layer, and a substitution reaction between the active species and oxygen in the oxide semiconductor layer occurs. At this time, a nucleus or a seed is formed. In addition, lateral growth of the nucleus or the seed is caused. In addition, the active species excited by the microwave preferably contain oxygen (typically, oxygen ions) that is likely to be adsorbed onto a side surface of the nucleus or the seed, in which case the lateral growth is promoted. The microwave plasma treatment causes formation of a nucleus or a seed and lateral growth of the nucleus or the seed, so that the crystallinity of the oxide semiconductor layer is improved.

[0593] Meanwhile, when part of oxygen that is present in the oxide semiconductor layer before the microwave plasma treatment reacts with hydrogen in the oxide semiconductor layer, i.e., a reaction of “2H+O.fwdarw.H.sub.2O↑” occurs, the hydrogen can be removed as H.sub.2O (i.e., dehydration or dehydrogenation). H.sub.2O is a limiting factor in improving crystallinity and thus is preferably removed from the oxide semiconductor layer. Hydrogen in the oxide semiconductor layer is removed as H.sub.2O to reduce the hydrogen concentration in the oxide semiconductor layer, whereby an improvement in crystallinity can be promoted. When the temperature of the microwave plasma treatment is increased, the hydrogen concentration in the oxide semiconductor layer can be further reduced.

[0594] In addition, the microwave plasma treatment may be followed successively by heat treatment without exposure to the air. The heat treatment temperature is preferably higher than or equal to 100° C. and lower than or equal to 750° C., further preferably higher than or equal to 300° C. and lower than or equal to 500° C., still further preferably higher than or equal to 400° C. and lower than or equal to 450° C., for example.

[0595] Note that the crystallinity can also be improved by performing plasma treatment using an oxygen gas, instead of the microwave plasma treatment.

[0596] The increase in the crystallinity of the layer formed by the first formation method can further increase the crystallinity of a layer formed over the layer. Thus, the crystallinity of the whole oxide semiconductor layer can be increased.

[0597] Oxygen supplied to the oxide semiconductor layer is in any of a variety of forms such as an oxygen atom, an oxygen molecule, an oxygen ion (a charged oxygen atom or a charged oxygen molecule), and an oxygen radical (an oxygen atom, an oxygen molecule, or an oxygen ion having an unpaired electron). Oxygen injected into the oxide semiconductor layer preferably has one or more of the above forms. An oxygen radical is particularly preferable.

[0598] Heat treatment is preferably performed after formation of the oxide semiconductor layer. By performing the heat treatment, the crystallinity of the oxide semiconductor layer can be increased. The heat treatment here is not limited to heating. For example, the heat treatment may be performed with heat applied in the manufacturing process.

[0599] The heat treatment temperature can be higher than or equal to 100° C. and lower than or equal to 800° C., preferably higher than or equal to 250° C. and lower than or equal to 650° C., further preferably higher than or equal to 350° C. and lower than or equal to 550° C., for example. Typically, the temperature can be 400° C.±25° C. (higher than or equal to 375° C. and lower than or equal to 425° C.). The treatment time can be shorter than or equal to 10 hours and can be, for example, longer than or equal to 1 minute and shorter than or equal to 5 hours, or longer than or equal to 1 minute and shorter than or equal to 2 hours. In the case of using an RTA apparatus, the treatment time can be longer than or equal to 1 second and shorter than or equal to 5 minutes, for example. By the heat treatment, the third layer formed by the first formation method (in other words, crystal molecules deposited by an ALD method) is expected to fill an atomic-level space between crystal parts of the CAAC structure of the second layer formed by the second formation method.

[0600] The heating apparatus used for the heat treatment is not limited to a particular apparatus, and may be an apparatus for heating an object to be processed by heat conduction or heat radiation from a heating element such as a resistance heating element. For example, an electric furnace, or a rapid thermal annealing (RTA) apparatus such as a lamp rapid thermal annealing (LRTA) apparatus or a gas rapid thermal annealing (GRTA) apparatus can be used. An LRTA apparatus is an apparatus for heating an object to be processed by radiation of light (an electromagnetic wave) emitted from a lamp such as a halogen lamp, a metal halide lamp, a xenon arc lamp, a carbon arc lamp, a high pressure sodium lamp, or a high pressure mercury lamp. A GRTA apparatus is an apparatus for heat treatment using a high-temperature gas.

[0601] By the heat treatment step, the crystallinity of the region having the CAAC structure may be

increased in the third layer formed by the first formation method. In the case where the region is formed only in the lower portion of the third layer after the deposition by an ALD method, the region may be extended upward by the heat treatment step. That is, by the heat treatment, the region having the CAAC structure may be formed in the whole third layer.

[0602] As described above, in the case where the oxide semiconductor layer has a three-layer structure, the first layer is formed over a formation surface by the first formation method, the second layer is formed by the first formation method, and then the third layer is formed by the second formation method, whereby the oxide semiconductor layer can be formed. In this case, by heat treatment step after the formation of the oxide semiconductor layer, at least part of the first layer or the second layer formed by the first formation method preferably has the CAAC structure. The CAAC structure is expected to be easily generated when a mixed layer formed in the first layer or the second layer serves as a nucleus or a seed. The CAAC region in the first layer or the second layer is preferably large, and the CAAC region preferably extends to the vicinity of the formation surface.

[0603] Since the CAAC region extends from the upper portion to the lower portion of the first layer or the second layer, the CAAC region can extend to the vicinity of the layer serving as the formation surface, regardless of the material and crystallinity of the layer serving as the formation surface. For example, even when the layer serving as the formation surface has an amorphous structure, the crystallinity of the first layer or the second layer can be increased. Thus, the method for forming the oxide semiconductor layer of one embodiment of the present invention is suitable particularly for the case where the layer serving as the formation surface has an amorphous structure.

[0604] When one or both of the microwave plasma treatment and the heat treatment are performed as described above, the crystallinity of the whole oxide semiconductor layer can be increased. Moreover, impurities in the oxide semiconductor layer can be reduced. Crystal growth of the oxide semiconductor layer with a low impurity concentration can further make crystallinity higher.

[0605] Increasing the crystallinity of the oxide semiconductor layer can inhibit an increase in the electric resistance of the semiconductor layer of a transistor including the oxide semiconductor layer or improve the initial characteristics (in particular, the on-state current) of the transistor, and thus a transistor suitable for high-speed operation can be expected. In addition, the reliability and on-state current of the transistor can be increased.

[0606] Note that one or both of the microwave plasma treatment and the heat treatment may be performed directly on the oxide semiconductor layer or performed after an insulating film or the like is formed over the oxide semiconductor layer.

[0607] Before formation of the first layer or after formation of the first layer or the second layer by the first formation method, oxygen may be supplied to the first layer or the second layer. Accordingly, oxygen can be supplied to the oxide semiconductor layer by heat or the like applied after this treatment.

[0608] Examples of the treatment for supplying oxygen include heat treatment in an oxygen-containing atmosphere and plasma treatment (including microwave plasma treatment) in an oxygen-containing atmosphere. Moreover, an oxide film (preferably a metal oxide film) may be formed in an oxygen-containing atmosphere by a sputtering method, thereby supplying oxygen to the first layer or the second layer formed by the first formation method. The formed oxide film may be removed immediately or left as it is. In the case where the formed oxide film is left as it is, the oxide film can be used as the layer provided over the first layer or the second layer (i.e., used as the second layer or the third layer). An oxygen-containing atmosphere can include not only an oxygen gas (O.sub.2) but also a gas of an oxygen-containing compound such as ozone (O.sub.3) or dinitrogen monoxide (N.sub.2O). The substrate temperature in the plasma treatment is higher than or equal to room temperature (25° C.) and lower than or equal to 450° C.

[0609] The oxide semiconductor layer of one embodiment of the present invention has high

crystallinity throughout the whole layer. Thus, in the oxide semiconductor layer, boundaries between the stacked first to third layers are not observed in some cases. The boundaries between the stacked layers may be difficult to observe particularly after heat treatment is performed. Whether the boundaries between the stacked layers are present can be checked in cross-sectional observation with a TEM or a scanning transmission electron microscope (STEM), for example.

[0610] The oxide semiconductor layer that is formed by the above-described two kinds of formation methods and has the CAAC structure sometimes has one or more of a higher relative permittivity, a higher film density, and higher film hardness than an oxide semiconductor layer that is formed by one kind of formation method and has the CAAC structure.

[0611] When the oxide semiconductor layer that is formed by the above-described two kinds of formation methods and has the CAAC structure is used for a channel formation region of a transistor, the transistor can have excellent characteristics (e.g., a high on-state current, high field-effect mobility, a low S value, high frequency characteristics (also referred to as f characteristics), or high reliability).

[0612] The oxide semiconductor layer of one embodiment of the present invention can sometimes be formed by using the first formation method and one or both of microwave plasma treatment and heat treatment. In other words, the oxide semiconductor layer of one embodiment of the present invention can be formed without using the second formation method in some cases. For example, after the first layer is formed by the first formation method, one or both of microwave plasma treatment and heat treatment are performed, whereby the crystallinity of the first layer can be increased. Thus, the crystallinity of the second layer that is formed over the first layer by the first formation method can be increased using the first layer as a nucleus or a seed. When one or both of microwave plasma treatment and heat treatment are performed after formation of the second layer, the crystallinity of the oxide semiconductor layer can be increased. Accordingly, the CAAC structure can be formed in the oxide semiconductor layer.

[0613] As described above, even in the formation method not using the second formation method, the use of the first layer formed by the first formation method as a nucleus or a seed enables solid-phase growth of the layer above the first layer, whereby an oxide semiconductor with high crystallinity can be formed. An oxide semiconductor formed by such a formation method can also be referred to as an AG CAAC.

[0614] In the case where the oxide semiconductor layer has a stacked-layer structure of two or more layers, the oxide semiconductor layer can also be formed by forming metal oxides by one kind of formation method. In the case where the oxide semiconductor layer has a two-layer structure of a first layer and a second layer over the first layer, the oxide semiconductor layer can be formed by forming the first layer and the second layer in this order by a sputtering method, for example. A sputtering method, which achieves a higher deposition rate than an ALD method, can increase the productivity. As another example, in the case where the oxide semiconductor layer has a three-layer structure of a first layer, a second layer over the first layer, and a third layer over the second layer, the first to third layers can be formed by a sputtering method. Furthermore, some of the first to third layers can be formed by an ALD method. For example, one or both of the second layer and the third layer may be formed by an ALD method.

[Oxide Semiconductor Layer of Transistor]

[0615] The oxide semiconductor layer of this embodiment can be used as a semiconductor layer of a transistor.

[0616] The oxide semiconductor layer of this embodiment can be used as the oxide semiconductor layer **230** or the like included in the transistors described in Embodiment 1. The layer serving as the formation surface corresponds to the insulating layer **225** or the like described in e.g., Embodiment 1. For example, the first layer can be used as the oxide semiconductor layer **230***a***1** and the oxide semiconductor layer **230***b***1** illustrated in FIGS. **13**A and **13**B, the second layer can be used as the oxide semiconductor layer **230***a***2** and the oxide semiconductor layer **230***b***2** illustrated in FIGS.

13A and **13**B. Furthermore, the third layer can be used as the oxide semiconductor layer **230***a***3** and the oxide semiconductor layer **230***b***3** illustrated in FIG. **13**B.

[0617] The oxide semiconductor layer of this embodiment preferably has the CAAC structure. In the oxide semiconductor layer having the CAAC structure, metal atoms are arranged in a crystal part in a layered manner in the direction parallel or substantially parallel to the formation surface.

[0618] The oxide semiconductor layer having the CAAC structure is presumed to exhibit current anisotropy. For example, in an IGZO crystal, current flows more easily in the a-axis direction than in the c-axis direction. That is, in the oxide semiconductor layer having the CAAC structure, current is presumed to flow easily in the lateral direction rather than in the vertical direction.

[0619] In the oxide semiconductor layer **230** of the semiconductor device described in the foregoing embodiment, metal atoms are arranged in a layered manner in the direction parallel or substantially parallel to the formation surface. This can also be expressed that "the a-b plane of the CAAC structure is provided to be parallel or substantially parallel to the formation surface". With such a structure, the a-b plane of the CAAC structure can be provided along a current flow direction in a channel of the transistor. Accordingly, the transistor can have a high on-state current.

[0620] In the case where the oxide semiconductor layer of this embodiment is used as a semiconductor layer of a transistor, the thickness of the oxide semiconductor layer is preferably greater than or equal to 3 nm and less than or equal to 200 nm, further preferably greater than or equal to 3 nm and less than or equal to 100 nm, further preferably greater than or equal to 5 nm and less than or equal to 100 nm, still further preferably greater than or equal to 10 nm and less than or equal to 100 nm, still further preferably greater than or equal to 10 nm and less than or equal to 70 nm, yet further preferably greater than or equal to 15 nm and less than or equal to 70 nm, yet further preferably greater than or equal to 15 nm and less than or equal to 50 nm, yet still further preferably greater than or equal to 20 nm and less than or equal to 50 nm, for example. In a transistor used for a further downsized semiconductor device, the thickness of the oxide semiconductor layer **230** is preferably greater than or equal to 1 nm and less than or equal to 20 nm, further preferably greater than or equal to 3 nm and less than or equal to 15 nm, still further preferably greater than or equal to 5 nm and less than or equal to 12 nm, yet further preferably greater than or equal to 5 nm and less than or equal to 10 nm. The average thickness of the oxide semiconductor layer in a channel formation region of the transistor is particularly preferably greater than or equal to 2 nm and less than or equal to 15 nm, for example.

[0621] The thickness of the first layer is preferably greater than or equal to 0.5 nm and less than or equal to 50 nm, further preferably greater than or equal to 0.5 nm and less than or equal to 30 nm, further preferably greater than or equal to 0.5 nm and less than or equal to 20 nm, still further preferably greater than or equal to 1 nm and less than or equal to 50 nm, still further preferably greater than or equal to 1 nm and less than or equal to 30 nm, yet further preferably greater than or equal to 1 nm and less than or equal to 20 nm, yet still further preferably greater than or equal to 2 nm and less than or equal to 20 nm, for example. The thickness of the first layer is further preferably greater than or equal to 0.5 nm and less than or equal to 3.0 nm.

[0622] The first layer preferably includes a region with a thickness greater than or equal to 0.1 nm and less than or equal to 3 nm, and further preferably includes a region with a thickness greater than or equal to 0.1 nm and less than or equal to 2 nm. Alternatively, the first layer preferably includes a region with a thickness greater than or equal to 0.5 nm and less than or equal to 3 nm, and further preferably includes a region with a thickness greater than or equal to 0.5 nm and less than or equal to 2 nm.

[0623] The thickness of the second layer is preferably less than 200 nm, for example. In the case where the second layer is in the form of layer, the thickness of the second layer is preferably greater than or equal to 1 nm and less than or equal to 200 nm, further preferably greater than or equal to 1 nm and less than or equal to 100 nm, still further preferably greater than or equal to 2 nm and less than or equal to 100 nm, for example.

[0624] Alternatively, in some cases, the second layer is not in the form of layer but is an aggregate of island-shaped regions as long as the second layer can function as a crystal nucleus. In such a case, the island-shaped regions of the second layer are discretely present, for example.
[0625] The description of the thickness of the first layer can be referred to for the preferred range of the thickness of the third layer.
[Impurities in Oxide Semiconductor Layer]
[0626] The influence of impurities in the oxide semiconductor layer is described here.
[0627] As has been described in the foregoing embodiment, in a transistor using the oxide semiconductor as a semiconductor layer, the electrical characteristics may vary easily and the reliability may be decreased when oxygen vacancies (V.sub.O) and impurities are present in a channel formation region in the oxide semiconductor layer. Accordingly, in order to obtain stable electrical characteristics of the OS transistor, reducing the impurity concentration in the oxide semiconductor layer is effective. In order to reduce the impurity concentration in the oxide semiconductor layer, it is preferable that the impurity concentration in an adjacent film be also reduced. Examples of impurities include hydrogen, carbon, and nitrogen. Note that impurities in an oxide semiconductor layer refer to, for example, elements other than the main components of an oxide semiconductor. For example, an element whose concentration is lower than 0.1 atomic % is an impurity.
[0628] When an oxide semiconductor contains silicon or carbon, which is a Group 14 element, defect states are formed in the oxide semiconductor. Accordingly, the carbon concentration in the channel formation region of the oxide semiconductor, which is measured by SIMS, is lower than or equal to 1×10.sup.20 atoms/cm.sup.3, preferably lower than or equal to 5×10.sup.19 atoms/cm.sup.3, further preferably lower than or equal to 3×10.sup.19 atoms/cm.sup.3, further preferably lower than or equal to 1×10.sup.19 atoms/cm.sup.3, still further preferably lower than or equal to 3×10.sup.18 atoms/cm.sup.3, yet still further preferably lower than or equal to 1×10.sup.18 atoms/cm.sup.3. The silicon concentration in the channel formation region of the oxide semiconductor, which is measured by SIMS, is lower than or equal to 1×10.sup.20 atoms/cm.sup.3, preferably lower than or equal to 5×10.sup.19 atoms/cm.sup.3, further preferably lower than or equal to 3×10.sup.19 atoms/cm.sup.3, further preferably lower than or equal to 1×10.sup.19 atoms/cm.sup.3, still further preferably lower than or equal to 3×10.sup.18 atoms/cm.sup.3, yet still further preferably lower than or equal to 1×10.sup.18 atoms/cm.sup.3.
[0629] When the oxide semiconductor contains nitrogen, electrons serving as carriers are generated to increase the carrier concentration and thus the resistance is easily lowered. As a result, a transistor including, as a semiconductor, an oxide semiconductor that contains nitrogen tends to have normally-on characteristics. Alternatively, when the oxide semiconductor contains nitrogen, a trap state is sometimes formed. This may make the electrical characteristics of the transistor unstable. Accordingly, the nitrogen concentration in the channel formation region of the oxide semiconductor, which is measured by SIMS, is lower than or equal to 1×10.sup.20 atoms/cm.sup.3, preferably lower than or equal to 5×10.sup.19 atoms/cm.sup.3, further preferably lower than or equal to 1×10.sup.19 atoms/cm.sup.3, further preferably lower than or equal to 5×10.sup.18 atoms/cm.sup.3, still further preferably lower than or equal to 1×10.sup.18 atoms/cm.sup.3, yet still further preferably lower than or equal to 5×10.sup.17 atoms/cm.sup.3.
[0630] Hydrogen contained in the oxide semiconductor reacts with oxygen bonded to a metal atom to be water, and thus an oxygen vacancy is formed in some cases. Entry of hydrogen into the oxygen vacancy generates an electron serving as a carrier in some cases. Furthermore, bonding of part of hydrogen to oxygen bonded to a metal atom generates an electron serving as a carrier. Thus, a transistor including an oxide semiconductor that contains hydrogen tends to have normally-on characteristics. For this reason, hydrogen in the channel formation region of the oxide semiconductor is preferably reduced as much as possible. Specifically, the hydrogen concentration in the channel formation region of the oxide semiconductor, which is measured by SIMS, is lower

than 1×10.sup.20 atoms/cm.sup.3, preferably lower than 5×10.sup.19 atoms/cm.sup.3, further preferably lower than 1×10.sup.19 atoms/cm.sup.3, still further preferably lower than 5×10.sup.18 atoms/cm.sup.3, still further preferably lower than 1×10.sup.18 atoms/cm.sup.3, yet still further preferably lower than 1×10.sup.17 atoms/cm.sup.3.

[0631] When the oxide semiconductor contains an alkali metal or an alkaline earth metal, defect states are formed and carriers are generated in some cases. Accordingly, a transistor including an oxide semiconductor that contains an alkali metal or an alkaline earth metal tends to have normally-on characteristics. Thus, the concentration of an alkali metal or an alkaline earth metal in the channel formation region of the oxide semiconductor, which is measured by SIMS, is lower than or equal to 1×10.sup.18 atoms/cm.sup.3, preferably lower than or equal to 2×10.sup.16 atoms/cm.sup.3.

[0632] When an oxide semiconductor with sufficiently reduced impurities is used for a channel formation region of a transistor, the transistor can have stable electrical characteristics.

[0633] This embodiment can be combined with any of the other embodiments as appropriate. In this specification, in the case where a plurality of structure examples are shown in one embodiment, the structure examples can be combined as appropriate.

Embodiment 3

[0634] In this embodiment, a semiconductor device of one embodiment of the present invention will be described with reference to drawings. The semiconductor device of one embodiment of the present invention includes a memory cell. The memory cell includes a transistor and a capacitor.

Structure Example 1 of Semiconductor Device

[0635] FIGS. **43**A and **43**B are plan views each illustrating a structure example of the semiconductor device. FIG. **43**A illustrates a region including 2×2 memory cells **150***a* and 2×2 memory cells **150***b*. In addition, the conductive layer **255** functioning as the wiring WOL, the conductive layer **260** functioning as the wiring BGL, the conductive layer **240***a* functioning as the wiring BILa, the conductive layer **240***b* functioning as the wiring BILb, and the opening portion **290** are illustrated.

[0636] As illustrated in FIG. **43**A, the memory cell **150***a* is provided at an intersection portion of the conductive layer **255** extending in the X direction and the conductive layer **240***a* extending in the Y direction. The memory cell **150***b* is provided at an intersection portion of the conductive layer **255** extending in the X direction and the conductive layer **240***b* extending in the Y direction. As illustrated in FIG. **43**A, the width of the opening portion **290** can be smaller than the width of the short side of the conductive layer **255**. Thus, it can be said that the memory cell **150** can be highly integrated and miniaturized.

[0637] Although FIG. **43**A illustrates a structure in which the conductive layer **260** is provided to extend in the Y direction, the present invention is not limited to the structure. For example, as illustrated in FIG. **43**B, the conductive layer **260** may be provided to extend in the X direction. Thus, the conductive layer **260** intersects with the conductive layer **240***a* or **240***b*, so that the conductive layer **260** can function as the wiring WOL. In this case, the conductive layer **255** functions as the wiring BGL.

[0638] In the structure illustrated in FIG. **43**B, the conductive layer **255** may be provided to extend in the Y direction.

[0639] FIG. **44**A is a plan view illustrating a structure example of a semiconductor device of the case where the transistor **200**C described in Embodiment 1 is used as the transistor included in the memory cell **150**. FIG. **44**A illustrates a region including 2×2 memory cells **150***a* and 2×2 memory cells **150***b*. In addition, the conductive layer **255** functioning as the wiring WOL, the conductive layer **240***a* functioning as the wiring BILa, the conductive layer **240***b* functioning as the wiring BILb, and the opening portion **290** are illustrated.

[0640] As illustrated in FIG. **44**A, the memory cell **150***a* is provided at an intersection portion of the conductive layer **255** extending in the X direction and the conductive layer **240***a* extending in

the Y direction. The memory cell **150***b* is provided at an intersection portion of the conductive layer **255** extending in the X direction and the conductive layer **240***b* extending in the Y direction. As illustrated in FIG. **44**A, the width of the opening portion **290** can be smaller than the width of the short side of the conductive layer **255**. Thus, it can be said that the memory cell **150** can be highly integrated and miniaturized.

[0641] FIG. **44**B is a plan view illustrating a structure example of a semiconductor device of the case where the transistor **200**D described in Embodiment 1 is used as the transistor included in the memory cell **150**. FIG. **44**B illustrates a region including 2×2 memory cells **150***a* and 2×2 memory cells **150***b*. In addition, the conductive layer **260** functioning as the wiring WOL, the conductive layer **240***a* functioning as the wiring BILa, the conductive layer **240***b* functioning as the wiring BILb, and the opening portion **290** are illustrated.

[0642] As illustrated in FIG. **44**B, the conductive layers **240***a* and **240***b* are provided such that the extending directions thereof are inclined with respect to the Y direction. The memory cell **150***a* is provided at an intersection portion of the conductive layer **240***a* and the conductive layer **260** extending in the Y direction. The memory cell **150***b* is provided at an intersection portion of the conductive layer **260** extending in the Y direction and the conductive layer **240***b*. As illustrated in FIG. **44**B, the width of the opening portion **290** can be smaller than the width of the short side of the conductive layer **260**. Thus, it can be said that the memory cell **150** can be highly integrated and miniaturized.

Structure Example 2 of Semiconductor Device

[0643] In a semiconductor device of one embodiment of the present invention, a plurality of transistors can be stacked, for example. FIG. **45** illustrates an example in which n layers (n is an integer greater than or equal to 3) of the capacitors **100** and the transistors **200** illustrated in FIG. **2**A are stacked in the Z direction. The memory cells **150** are provided in a region between dashed triplicate-dotted lines C**1** and C**2** in FIG. **45**. Furthermore, a region between dashed triplicate-dotted lines C**1** and C**3** includes a region where the conductive layer **240** extends.

[0644] The semiconductor device illustrated in FIG. **45** includes n memory layers **170**. In FIG. **45**, the n memory layers **170** are distinguishably shown with reference numerals **170**[**1**] to **170**[*n]*.

[0645] Specifically, a memory layer **170**[**2**] is provided over a memory layer **170**[**1**], and (n−2) memory layers **170** are provided over the memory layer **170**[**2**]. A memory layer **170**[*n*] is provided as the uppermost layer. The memory cells **150** each including the capacitor **100** and the transistor **200** are provided in each memory layer **170**. The insulating layer **180** is provided under each of the memory layers **170**[**1**] to **170**[*n*]. The insulating layers **180** other than the insulating layer **180** positioned under the memory layer **170**[**1**] can each be provided to cover the conductive layer **260**.

[0646] There is no particular limitation on the number of memory cells **150** included in one memory layer **170**, and two or more memory cells **150** can be included. Through a conductive layer **253**, a conductive layer **254**, a conductive layer **256**, a conductive layer **257**, a conductive layer **258**, a conductive layer **259**, and the like, the memory cells **150** included in the n memory layers **170** are connected to a sense amplifier (not illustrated) provided below the n memory layers **170**. In this case, the conductive layers **253**, **254**, **256**, **257**, **258**, and **259** and the like function as parts of the wiring BIL illustrated in FIG. **2**E. Stacking the plurality of memory cells **150** in this manner can increase the memory capacity per unit area.

[0647] FIG. **45** illustrates an example in which the conductive layer **240** has a two-layer structure of a conductive layer **240_1** and a conductive layer **240_2**. For the conductive layer **240_1**, the description of the conductive layers **240***a***1** and **240***b***1** in Embodiment 1 can be referred to. For the conductive layer **240_2**, the description of the conductive layers **240***a***2** and **240***b***2** in Embodiment 1 can be referred to. In FIG. **45**, the conductive layers **240_1** and the conductive layers **240_2** provided in the memory layers **170**[**1**] to **170**[*n*] are distinguishably shown with reference numerals **240_1**[**1**] to **240_1**[*n*] and **240_2**[**1**] to **240_2**[*n*], respectively. Note that the conductive layer **240_1** and the conductive layer **240_2** may be collectively referred to as a conductive layer **240**. In FIG.

45, the conductive layers **240** provided in the memory layers **170**[**1**] to **170**[*n*] are distinguishably shown with reference numerals **240**[**1**] to **240**[*n*].
[0648] The conductive layers **253**, the conductive layers **256**, and the conductive layers **259** provided in the memory layers **170**[**1**] to **170**[*n*] are distinguishably shown with reference numerals **253**[**1**] to **253**[*n*], **256**[**1**] to **256**[*n*], and **259**[**1**] to **259**[*n*], respectively. Furthermore, the conductive layers **258** provided in the memory layers **170**[**1**] and **170**[**2**] are distinguishably shown with reference numerals **258**[**1**] and **258**[**2**].
[0649] The conductive layers **254**, **253**, **256**, **257**, **258**, **259**, and the like may function as plugs or wirings for connecting the memory cell **150** to a circuit element such as a switch, a transistor, a capacitor, an inductor, a resistor, or a diode, a wiring, an electrode, or a terminal.
[0650] FIG. **45** illustrates an example in which the conductive layer **258** is provided on the same formation surface as the conductive layer **110**. Furthermore, in the example illustrated in FIG. **45**, the conductive layer **259** is provided on the same formation surface as the conductive layers **220***a* and **220***b*. The conductive layer **259** includes a conductive layer **259_1** and a conductive layer **259_2** over the conductive layer **2591**. The conductive layer **259_1** is provided on the same formation surface as the conductive layers **220***a***1** and **220***b***1**. The conductive layer **259_2** is provided on the same formation surface as the conductive layers **220***a***2** and **220***b***2**. The conductive layer **258** can be formed in the same process as the conductive layer **110** and can include the same material as the conductive layer **110**. The conductive layer **259_1** can be formed in the same process as the conductive layers **220***a***1** and **220***b***1** and can include the same material as the conductive layers **220***a***1** and **220***b***1**. The conductive layer **2592** can be formed in the same process as the conductive layers **220***a***2** and **220***b***2** and can include the same material as the conductive layers **220***a***2** and **220***b***2**. In addition, the conductive layers **259_1** and the conductive layers **259_2** included in the conductive layers **259**[**1**] to **259**[*n*] are distinguishably shown with reference numerals **259_1**[**1**] to **259_1**[*n*] and **259_2**[**1**] to **259_2**[*n*], respectively.
[0651] FIG. **45** illustrates an example in which the conductive layer **254** is provided in an opening portion of the insulating layer **180** under the memory layer **170**[**1**]. In the illustrated example, the conductive layer **253** is provided in an opening portion in the insulating layers **160**, **185**, and **186**. Moreover, the conductive layer **256** is provided in an opening portion in the conductive layer **259_2**, the insulating layer **280**, and the insulating layer **281**. Furthermore, the conductive layer **257** is provided in an opening portion in the conductive layer **240_2**, the insulating layer **250**, and the insulating layer **180**.
[0652] FIG. **45** illustrates an example in which the insulating layer **121** functioning as the dielectrics of the capacitor **100***a* and the capacitor **100***b* is not provided in the region between the dashed triplicate-dotted lines C**1** and C**3**. Accordingly, the opening portion in which the conductive layer **253** is provided does not need to be provided in the insulating layer **121**, which makes it possible to easily form the opening portion.
[0653] The conductive layer **254** can be in contact with the bottom surface of the conductive layer **258**[**1**]. The conductive layer **253** can be in contact with the top surface of the conductive layer **258** and the bottom surface of the conductive layer **259_1**. The conductive layer **256** can be in contact with the top surface of the conductive layer **2591** and the bottom surface of the conductive layer **240_1**. The conductive layer **257** can be in contact with the top surface of the conductive layer **240_1** and the bottom surface of the conductive layer **258**. In the above-described manner, the conductive layers **240**[**1**] to **240**[*n*] can be connected to each other. In addition, the conductive layers **253**, **254**, **256**, and **257** can each be formed using a conductive material that is usable for the conductive layer **240**, for example.
[0654] In the case where the contact resistance between the conductive layer **259_1** and the conductive layer **256** is lower than the contact resistance between the conductive layer **259_2** and the conductive layer **256**, the opening portion in which the conductive layer **256** is provided is preferably provided also in the conductive layer **259_2** as illustrated in FIG. **45**. In the case where

the contact resistance between the conductive layer **240_1** and the conductive layer **257** is lower than the contact resistance between the conductive layer **240_2** and the conductive layer **257**, the opening portion in which the conductive layer **257** is provided is preferably provided also in the conductive layer **240_2** as illustrated in FIG. **45**.

[0655] When a plurality of memory cells **150** are stacked as illustrated in FIG. **45**, the memory cells **150** can be provided in an integrated manner without increasing the area occupied by the memory cell array. That is, a 3D memory cell array can be formed. This results in an increase in the memory capacity per unit area.

[0656] FIG. **46** illustrates a cross-sectional structure example of a semiconductor device in which a layer including the memory cells **150** is stacked over a layer in which a driver circuit including a sense amplifier is provided.

[0657] In FIG. **46**, the memory cells **150** (the transistors **200** and the capacitors **100**) are provided above a transistor **300**.

[0658] The transistor **300** is one of the transistors included in the sense amplifier.

[0659] When the sense amplifier is provided to overlap with the memory cells **150** as illustrated in FIG. **46**, the bit line can be shortened. Accordingly, the bit line capacitance can be reduced and the semiconductor device can be driven at high speed.

[0660] The semiconductor device illustrated in FIG. **46** can correspond to a semiconductor device **900** described in Embodiment 4. Specifically, the transistor **300** corresponds to a transistor included in a sense amplifier **927** in the semiconductor device **900**. The memory cell **150** corresponds to a memory cell **950**.

[0661] The transistor **300** is provided on a substrate **311** and includes a conductive layer **316** functioning as a gate, an insulating layer **315** functioning as a gate insulating layer, a semiconductor region **313** that is a part of the substrate **311**, and a low-resistance region **314***a* and a low-resistance region **314***b* functioning as a source region and a drain region. The transistor **300** may be either a p-channel transistor or an n-channel transistor. The substrate **311** preferably includes a silicon-based semiconductor, specifically, single crystal silicon.

[0662] In the transistor **300** illustrated in FIG. **46**, the semiconductor region **313** (part of the substrate **311**) where a channel is formed has a projecting shape. Furthermore, the conductive layer **316** is provided to cover the side surface and the top surface of the semiconductor region **313** with the insulating layer **315** therebetween. The conductive layer **316** may be formed using a material for adjusting the work function. The transistor **300** having such a structure is also referred to as a FIN transistor because the projecting portion of the semiconductor substrate is utilized. In addition, an insulating layer functioning as a mask for forming the projecting portion may be provided in contact with the top of the projecting portion. Although the case where the projecting portion is formed by processing part of the semiconductor substrate is described here, a semiconductor film having a projecting shape may be formed by processing an SOI substrate.

[0663] Note that the transistor **300** illustrated in FIG. **46** is just an example and is not limited to having the structure illustrated there; an appropriate transistor can be used in accordance with the circuit structure or the driving method.

[0664] A wiring layer including an interlayer film, a wiring, a plug, or the like may be provided between components. A plurality of wiring layers can be provided in accordance with the design. Here, a plurality of conductive layers functioning as plugs or wirings are collectively denoted by the same reference numeral in some cases. In this specification and the like, a wiring and a plug connected to the wiring may be a single component. That is, in some cases, part of a conductive layer functions as a wiring or another part of the conductive layer functions as a plug.

[0665] For example, an insulating layer **320**, an insulating layer **322**, an insulating layer **324**, and an insulating layer **326** are stacked over the transistor **300** in this order as interlayer films. A conductive layer **328** is embedded in the insulating layers **320** and **322**, and a conductive layer **330** is embedded in the insulating layers **324** and **326**. The conductive layers **328** and **330** each function

as a plug or a wiring.
[0666] The insulating layer functioning as an interlayer film may function as a planarization film that covers a roughness thereunder. For example, the top surface of the insulating layer **322** may be planarized by planarization treatment using a CMP method or the like to improve the flatness.
[0667] A wiring layer may be provided over the insulating layer **326** and the conductive layer **330**. For example, in FIG. **46**, an insulating layer **350**, an insulating layer **352**, and an insulating layer **354** are stacked sequentially. Furthermore, a conductive layer **356** is formed in the insulating layers **350**, **352**, and **354**. The conductive layer **356** functions as a plug or a wiring.
[0668] As the insulating layers **352** and **354** and the like functioning as interlayer films, any of the above-described insulating layers that can be used for the semiconductor device can be used.
[0669] As each of the conductive layers functioning as plugs or wirings, e.g., the conductive layers **328**, **330**, and **356**, a conductive material usable for the conductive layer **240** can be used. It is preferable to use a high-melting-point material, e.g., tungsten or molybdenum, that has both heat resistance and conductivity, and it is particularly preferable to use tungsten. Alternatively, a low-resistance conductive material such as aluminum or copper is preferably used. The use of a low-resistance conductive material can reduce wiring resistance.
[0670] The conductive layer **240** is connected to the low-resistance region **314***b* functioning as the source or drain region of the transistor **300** through the conductive layers **256**, **259**, **253**, **258**, **254**, **356**, **330**, and **328**. For the conductive layers **256**, **259**, **253**, **258**, and **254**, the description of FIG. **45** can be referred to.
[0671] This embodiment can be combined with any of the other embodiments as appropriate. In this specification, in the case where a plurality of structure examples are shown in one embodiment, the structure examples can be combined as appropriate.

Embodiment 4

[0672] In this embodiment, the semiconductor device **900** of one embodiment of the present invention will be described. The semiconductor device **900** can function as a memory device.
[0673] FIG. **47** is a block diagram illustrating a structure example of the semiconductor device **900**. The semiconductor device **900** illustrated in FIG. **47** includes a driver circuit **910** and a memory array **920**. The memory array **920** includes at least one memory cell **950**. FIG. **47** illustrates an example where the memory array **920** includes a plurality of memory cells **950** arranged in a matrix.
[0674] The memory device (e.g., the memory device **150**) described in Embodiment 3 can be used for the memory cell **950**.
[0675] The driver circuit **910** includes a power switch (PSW) **931**, a PSW **932**, and a peripheral circuit **915**. The peripheral circuit **915** includes a peripheral circuit **911**, a control circuit **912**, and a voltage generator circuit **928**.
[0676] In the semiconductor device **900**, the circuits, signals, and voltages can be appropriately selected as needed. Another circuit or another signal may be added. Signals BW, CE, GW, CLK, WAKE, ADDR, WDA, PON**1**, and PON**2** are signals input from the outside, and a signal RDA is a signal output to the outside. The signal CLK is a clock signal.
[0677] The signals BW, CE, and GW are control signals. The signal CE is a chip enable signal. The signal GW is a global write enable signal. The signal BW is a byte write enable signal. The signal ADDR is an address signal. The signal WDA is a write data signal, and the signal RDA is a read data signal. The signals PON**1** and PON**2** are power gating control signals. In addition, the signals PON**1** and PON**2** may be generated in the control circuit **912**.
[0678] The control circuit **912** is a logic circuit having a function of controlling the overall operation of the semiconductor device **900**. For example, the control circuit **912** performs logical operation on the signals CE, GW, and BW to determine the operating mode (e.g., write operation or read operation) of the semiconductor device **900**. The control circuit **912** generates a control signal for the peripheral circuit **911** so that the operating mode is executed.

[0679] The voltage generator circuit **928** has a function of generating a negative voltage. The signal WAKE has a function of controlling the input of the signal CLK to the voltage generator circuit **928**. For example, when an H-level signal is applied as the signal WAKE, the signal CLK is input to the voltage generator circuit **928**, and the voltage generator circuit **928** generates a negative voltage.
[0680] The peripheral circuit **911** is a circuit for writing and reading data to/from the memory cell **950**. The peripheral circuit **911** includes a row decoder **941**, a column decoder **942**, a row driver **923**, a column driver **924**, an input circuit **925**, an output circuit **926**, and the sense amplifier **927**.
[0681] The row decoder **941** and the column decoder **942** have a function of decoding the signal ADDR. The row decoder **941** is a circuit for specifying a row to be accessed. The column decoder **942** is a circuit for specifying a column to be accessed. The row driver **923** has a function of selecting the row specified by the row decoder **941**. The column driver **924** has a function of writing data to the memory cell **950**, reading data from the memory cell **950**, and retaining the read data, for example.
[0682] The input circuit **925** has a function of retaining the signal WDA. Data retained in the input circuit **925** is output to the column driver **924**. Data output from the input circuit **925** is data (Din) written to the memory cell **950**. Data (Dout) read from the memory cell **950** by the column driver **924** is output to the output circuit **926**. The output circuit **926** has a function of retaining Dout. Moreover, the output circuit **926** has a function of outputting Dout to the outside of the semiconductor device **900**. The data output from the output circuit **926** is the signal RDA.
[0683] The PSW **931** has a function of controlling the supply of V.sub.DD to the peripheral circuit **915**. The PSW **932** has a function of controlling the supply of V.sub.HM to the row driver **923**. Here, in the semiconductor device **900**, a high power supply potential is V.sub.DD and a low power supply potential is a ground potential (GND). In addition, V.sub.HM is a high power supply potential used for setting a word line at a high level, and is higher than V.sub.DD. The on/off state of the PSW **931** is controlled by the signal PON**1**, and the on/off state of the PSW **932** is controlled by the signal PON**2**. The number of power domains to which V.sub.DD is supplied is one in the peripheral circuit **915** in FIG. **47** but can be more than one. In that case, a power switch can be provided for each power domain.
[0684] Structure examples of memory cells each of which can be used as the memory cell **950** are described with reference to FIGS. **48**A to **48**D.
[DOSRAM]
[0685] FIG. **48**A illustrates a circuit structure example of a memory cell for a DRAM. In this specification and the like, a DRAM using an OS transistor is referred to as a dynamic oxide semiconductor random access memory (DOSRAM). A memory cell **951** includes a transistor M**1** and a capacitor CA.
[0686] The transistor M**1** includes a gate (sometimes referred to as a top gate) and a back gate. Here, the back gate may be connected to a wiring supplied with a constant potential or a signal, and the front gate and the back gate may be connected to each other.
[0687] A first terminal of the transistor M**1** is connected to a first terminal of the capacitor CA. A second terminal of the transistor M**1** is connected to the wiring BIL. A gate of the transistor M**1** is connected to the wiring WOL, and the back gate of the transistor M**1** is connected to a wiring BGL. A second terminal of the capacitor CA is connected to the wiring CAL.
[0688] The wiring BIL functions as a bit line, and the wiring WOL functions as a word line. The wiring CAL functions as a wiring for applying a predetermined potential to the second terminal of the capacitor CA. At the time of data writing and data reading, a low-level potential (sometimes referred to as a reference potential) is preferably applied to the wiring CAL. The wiring BGL functions as a wiring for applying a potential to the back gate of the transistor M**1**. The threshold voltage of the transistor M**1** can be increased or decreased by applying a given potential to the wiring BGL.

[0689] Data writing and data reading are performed in such a manner that a high-level potential is applied to the wiring WOL to turn on the transistor M**1** and establish electrical continuity between the wiring BIL and the first terminal of the capacitor CA (make a state where a current can flow therethrough).
[0690] The memory cell that can be used as the memory cell **950** is not limited to the memory cell **951**, and the circuit structure can be changed. For example, in the memory cell **950**, the back gate of the transistor M**1** is connected to the wiring WOL instead of the wiring BGL. In another example of the memory cell **950**, the transistor M**1** may be a single-gate transistor, that is, a transistor without a back gate. For example, the memory cell **951** does not necessarily include the capacitor CA or the wiring CAL, and the first terminal of the transistor M**1** may be in a floating state.
[0691] Note that an OS transistor is preferably used as the transistor M**1**. An OS transistor has a characteristic of an extremely low off-state current. The use of an OS transistor as the transistor M**1** enables an extremely low leakage current of the transistor M**1**. That is, with the use of the transistor M**1**, written data can be retained for a long time, and thus the frequency of refresh operation for the memory cell can be decreased or the refresh operation for the memory cell does not needed to be performed. In addition, owing to an extremely low leakage current, multilevel data or analog data can be retained in the memory cell **951**.
[NOSRAM]
[0692] FIG. **48**B illustrates a circuit structure example of a gain-cell memory cell including two transistors and one capacitor. A memory cell **953** includes a transistor M**2**, a transistor M**3**, and a capacitor CB. In this specification and the like, a memory device including a gain-cell memory cell using an OS transistor as the transistor M**2** is referred to as a nonvolatile oxide semiconductor RAM (NOSRAM).
[0693] A first terminal of the transistor M**2** is connected to a first terminal of the capacitor CB. A second terminal of the transistor M**2** is connected to the wiring WBL. A gate of the transistor M**2** is connected to the wiring WOL and a back gate of the transistor M**2** is connected to the wiring BGL. A second terminal of the capacitor CB is connected to the wiring CAL. A first terminal of the transistor M**3** is connected to a wiring RBL. A second terminal of the transistor M**3** is connected to a wiring SL. A gate of the transistor M**3** is connected to the first terminal of the capacitor CB.
[0694] The wiring WBL functions as a write bit line, the wiring RBL functions as a read bit line, and the wiring WOL functions as a word line. The wiring CAL functions as a wiring for applying a predetermined potential to the second terminal of the capacitor CB. At the time of data writing, data retention, and data reading, a low-level potential (sometimes referred to as a reference potential) is preferably applied to the wiring CAL.
[0695] Data writing is performed in such a manner that a high-level potential is applied to the wiring WOL to turn on the transistor M**2** and establish electrical continuity between the wiring WBL and the first terminal of the capacitor CB. Specifically, when the transistor M**2** is on, a potential corresponding to data to be stored is applied to the wiring WBL, and the potential is written to the first terminal of the capacitor CB and the gate of the transistor M**3**. Then, a low-level potential is applied to the wiring WOL to turn off the transistor M**2**, whereby the potential of the first terminal of the capacitor CB and the potential of the gate of the transistor M**3** are retained.
[0696] Data reading is performed by applying a predetermined potential to the wiring SL. A current flowing between the source and the drain of the transistor M**3** and the potential of the first terminal of the transistor M**3** are determined by the potential of the gate of the transistor M**3** and the potential of the second terminal of the transistor M**3**. Accordingly, by reading a potential of the wiring RBL connected to the first terminal of the transistor M**3**, a potential retained in the first terminal of the capacitor CB (or the gate of the transistor M**3**) can be read. That is, data written to the memory cell can be read on the basis of the potential retained in the first terminal of the capacitor CB (or the gate of the transistor M**3**).

[0697] As another example, one wiring BIL may be provided in place of the wiring WBL and the wiring RBL. A circuit structure example of the memory cell is illustrated in FIG. **48**C. In a memory cell **954**, one wiring BIL is provided in place of the wiring WBL and the wiring RBL in the memory cell **953**, and the second terminal of the transistor M**2** and the first terminal of the transistor M**3** are connected to the wiring BIL. In other words, one wiring BIL operates as the write bit line and the read bit line in the memory cell **954**.
[0698] An OS transistor is preferably used as at least the transistor M**2**. In particular, an OS transistor is preferably used as each of the transistors M**2** and M**3**.
[0699] Since the OS transistor has a characteristic of an extremely low off-state current, written data can be retained for a long time with the use of the transistor M**2**, and thus the frequency of refresh operation for the memory cell can be decreased or the refresh operation for the memory cell does not needed to be performed. In addition, owing to an extremely low leakage current, multilevel data or analog data can be retained in the memory cells **953** and **954**.
[0700] The memory cells **953** and **954** each using the OS transistor as the transistor M**2** are embodiments of a NOSRAM.
[0701] In addition, a Si transistor may be used as the transistor M**3**. The Si transistor can have high field-effect mobility and can be formed as a p-channel transistor, so that circuit design flexibility can be increased.
[0702] When an OS transistor is used as the transistor M**3**, the memory cell can be configured with transistors having the same conductivity type.
[0703] FIG. **48**D illustrates an example of a gain memory cell **957** including three transistors and one capacitor. The memory cell **957** includes transistors M**4** to M**6** and a capacitor CC.
[0704] A first terminal of the transistor M**4** is connected to a first terminal of the capacitor CC. A second terminal of the transistor M**4** is connected to the wiring BIL. A gate of the transistor M**4** is connected to the wiring WOL and a back gate of the transistor M**4** is connected to the wiring BGL. A second terminal of the capacitor CC is connected to a first terminal of the transistor M**5** and a wiring GNDL. A second terminal of the transistor M**5** is connected to a first terminal of the transistor M**6**. A gate of the transistor M**5** is connected to the first terminal of the capacitor CC. A second terminal of the transistor M**6** is electrically connected to the wiring BIL. A gate of the transistor M**6** is connected to a wiring RWL.
[0705] The wiring BIL functions as a bit line. The wiring WOL functions as a write word line. The wiring RWL functions as a read word line. The wiring GNDL is a wiring for supplying a low-level potential.
[0706] Data writing is performed in such a manner that a high-level potential is applied to the wiring WOL to turn on the transistor M**4** and establish electrical continuity between the wiring BIL and the first terminal of the capacitor CC. Specifically, when the transistor M**4** is on, a potential corresponding to data to be stored is applied to the wiring BIL, and the potential is written to the first terminal of the capacitor CC and the gate of the transistor M**5**. Then, a low-level potential is applied to the wiring WOL to turn off the transistor M**4**, whereby the potential of the first terminal of the capacitor CC and the potential of the gate of the transistor M**5** are retained.
[0707] Data reading is performed by precharging the wiring BIL with a predetermined potential, and then making the wiring BIL in an electrically floating state and applying a high-level potential to the wiring RWL. Since the wiring RWL has the high-level potential, the transistor M**6** is turned on, so that electrical continuity is established between the wiring BIL and the second terminal of the transistor M**5**. At this time, the potential of the wiring BIL is applied to the second terminal of the transistor M**5**; the potential of the second terminal of the transistor M**5** and the potential of the wiring BIL change depending on the potential retained in the first terminal of the capacitor CC (or the gate of the transistor M**5**). Here, the potential retained in the first terminal of the capacitor CC (or the gate of the transistor M**5**) can be read by reading the potential of the wiring BIL. That is, data written to the memory cell can be read on the basis of the potential retained in the first

terminal of the capacitor CC (or the gate of the transistor M**5**).
[0708] Note that an OS transistor is preferably used as at least the transistor M**4**.
[0709] Note that Si transistors may be used as the transistors M**5** and M**6**. As described above, a Si transistor may have higher field-effect mobility than an OS transistor depending on the crystal state of silicon used in a semiconductor layer, for example.
[0710] When OS transistors are used as the transistors M**5** and M**6**, the memory cell can be configured with the transistors having the same conductivity type.
[0711] The driver circuit **910** and the memory array **920** included in the semiconductor device **900** may be provided on the same plane. Alternatively, as illustrated in FIG. **49**A, the driver circuit **910** and the memory array **920** may be stacked. Stacking the driver circuit **910** and the memory array **920** can shorten a signal propagation distance. As illustrated in FIG. **49**B, a plurality of memory arrays **920** may be stacked over the driver circuit **910**.
[0712] Next, description is made on an example of an arithmetic processing device that can include the semiconductor device such as the memory device described above.
[0713] FIG. **50** is a block diagram of an arithmetic device **960**. The arithmetic device **960** illustrated in FIG. **50** can be used as a CPU, for example. The arithmetic device **960** can also be used as a processor including a larger number of (several tens to several hundreds of) processor cores capable of parallel processing than a CPU, such as a graphics processing unit (GPU), a tensor processing unit (TPU), or a neural processing unit (NPU).
[0714] The arithmetic device **960** illustrated in FIG. **50** includes, over a substrate **990**, an arithmetic logic unit (ALU) **991**, an ALU controller **992**, an instruction decoder **993**, an interrupt controller **994**, a timing controller **995**, a register **996**, a register controller **997**, a bus interface **998**, a cache **999**, and a cache interface **989**. A semiconductor substrate, an SOI substrate, a glass substrate, or the like is used as the substrate **990**. The arithmetic device **960** may also include a rewritable ROM and a ROM interface. The cache **999** and the cache interface **989** may be provided in a separate chip.
[0715] The cache **999** is connected via the cache interface **989** to a main memory provided in another chip. The cache interface **989** has a function of supplying part of data retained in the main memory to the cache **999**. The cache interface **989** also has a function of outputting part of data retained in the cache **999** to the ALU **991**, the register **996**, or the like through the bus interface **998**.
[0716] As described later, the memory array **920** can be stacked over the arithmetic device **960**. The memory array **920** can be used as a cache. Here, the cache interface **989** may have a function of supplying data retained in the memory array **920** to the cache **999**. Moreover, in this case, the driver circuit **910** is preferably included in part of the cache interface **989**.
[0717] It is also possible that the cache **999** is not provided and only the memory array **920** is used as a cache.
[0718] The arithmetic device **960** illustrated in FIG. **50** is just an example with a simplified structure, and the actual arithmetic device **960** has a variety of structures depending on the application. For example, what is called a multicore structure is preferably employed where a plurality of cores each including the arithmetic device **960** in FIG. **50** operate in parallel. The larger number of cores can further enhance the arithmetic performance. The number of cores is preferably larger; for example, the number is preferably 2, further preferably 4, still further preferably 8, yet still further preferably 12, yet still further preferably 16 or larger. For application requiring extremely high arithmetic performance, e.g., a server, it is preferable to employ the multicore structure including 16 or more cores, preferably 32 or more cores, further preferably 64 or more cores. The number of bits that the arithmetic device **960** can handle with an internal arithmetic circuit, a data bus, or the like can be 8, 16, 32, or 64, for example.
[0719] An instruction input to the arithmetic device **960** through the bus interface **998** is input to the instruction decoder **993** and decoded, and then input to the ALU controller **992**, the interrupt

controller **994**, the register controller **997**, and the timing controller **995**.
[0720] The ALU controller **992**, the interrupt controller **994**, the register controller **997**, and the timing controller **995** conduct various controls in accordance with the decoded instruction. Specifically, the ALU controller **992** generates signals for controlling the operation of the ALU **991**. The interrupt controller **994** judges and processes an interrupt request from an external input/output device, a peripheral circuit, or the like on the basis of its priority, a mask state, or the like while the arithmetic device **960** is executing a program. The register controller **997** generates the address of the register **996**, and reads/writes data from/to the register **996** in accordance with the state of the arithmetic device **960**.
[0721] The timing controller **995** generates signals for controlling operation timings of the ALU **991**, the ALU controller **992**, the instruction decoder **993**, the interrupt controller **994**, and the register controller **997**. For example, the timing controller **995** includes an internal clock generator for generating an internal clock signal on the basis of a reference clock signal, and supplies the internal clock signal to the above circuits.
[0722] In the arithmetic device **960** illustrated in FIG. **50**, the register controller **997** selects operation of retaining data in the register **996** in accordance with an instruction from the ALU **991**. That is, the register controller **997** selects whether data is retained by a flip-flop or by a capacitor in a memory cell included in the register **996**. When data retention by the flip-flop is selected, a power supply potential is supplied to the memory cell in the register **996**. When data retention by the capacitor is selected, the data is rewritten into the capacitor, and supply of the power supply potential to the memory cell in the register **996** can be stopped.
[0723] The memory array **920** and the arithmetic device **960** can be provided to overlap with each other. FIGS. **51**A and **51**B are perspective views of a semiconductor device **970**A. The semiconductor device **970**A includes a layer **930** provided with memory arrays over the arithmetic device **960**. A memory array **920**L**1**, a memory array **920**L**2**, and a memory array **920**L**3** are provided in the layer **930**. The arithmetic device **960** and each of the memory arrays overlap with each other. For easy understanding of the structure of the semiconductor device **970**A, the arithmetic device **960** and the layer **930** are separately illustrated in FIG. **51**B.
[0724] Stacking the arithmetic device **960** and the layer **930** provided with the memory arrays can shorten the connection distance therebetween. Accordingly, the communication speed therebetween can be increased. Moreover, the short connection distance leads to lower power consumption.
[0725] As a method for stacking the arithmetic device **960** and the layer **930** provided with the memory arrays, either of the following methods may be employed: a method in which the layer **930** provided with the memory arrays is stacked directly on the arithmetic device **960**, which is also referred to as monolithic stacking, and a method in which the arithmetic device **960** and the layer **930** are formed over two different substrates, the substrates are bonded to each other, and the arithmetic device **960** and the layer **930** are connected to each other with a through via or by a technique for bonding conductive films (e.g., Cu—Cu bonding). The former method does not require consideration of misalignment in bonding; thus, not only the chip size but also the manufacturing cost can be reduced.
[0726] Here, it is possible that the arithmetic device **960** does not include the cache **999** and the memory arrays **920**L**1**, **920**L**2**, and **920**L**3** provided in the layer **930** are each used as a cache. In this case, for example, the memory array **920**L**1**, the memory array **920**L**2**, and the memory array **920**L**3** can be used as an L**1** cache (also referred to as a level 1 cache), an L**2** cache (also referred to as a level 2 cache), and an L**3** cache (also referred to as a level 3 cache), respectively. Among the three memory arrays, the memory array **920**L**3** has the highest capacity and the lowest access frequency. The memory array **920**L**1** has the lowest capacity and the highest access frequency.
[0727] In addition, in the case where the cache **999** provided in the arithmetic device **960** is used as the L**1** cache, the memory arrays provided in the layer **930** can each be used as the lower-level cache or the main memory. The main memory has higher capacity and lower access frequency than

the cache.
[0728] As illustrated in FIG. **51**B, a driver circuit **910**L**1**, a driver circuit **910**L**2**, and a driver circuit **910**L**3** are provided. The driver circuit **910**L**1** is connected to the memory array **920**L**1** through a connection electrode **940**L**1**. Similarly, the driver circuit **910**L**2** is connected to the memory array **920**L**2** through a connection electrode **940**L**2**, and the driver circuit **910**L**3** is connected to the memory array **920**L**3** through a connection electrode **940**L**3**.
[0729] Although three memory arrays function as caches here, the number of memory arrays functioning as caches may be one, two, or four or more.
[0730] In the case where the memory array **920**L**1** is used as a cache, the driver circuit **910**L**1** may function as part of the cache interface **989** or the driver circuit **910**L**1** may be connected to the cache interface **989**. Similarly, each of the driver circuits **910**L**2** and **910**L**3** may function as part of the cache interface **989** or be connected thereto.
[0731] Whether the memory array **920** functions as the cache or the main memory is determined by the control circuit **912** included in each of the driver circuits **910**. The control circuit **912** can make some of the memory cells **950** in the semiconductor device **900** function as RAM in accordance with a signal supplied from the arithmetic device **960**.
[0732] In the semiconductor device **900**, some of the memory cells **950** can function as the cache and the other memory cells **950** can function as the main memory. That is, the semiconductor device **900** can have both the function of the cache and the function of the main memory. The semiconductor device **900** of one embodiment of the present invention can function as a universal memory, for example.
[0733] The layer **930** including one memory array **920** may be provided to overlap with the arithmetic device **960**. FIG. **52**A is a perspective view of a semiconductor device **970**B.
[0734] In the semiconductor device **970**B, one memory array **920** can be divided into a plurality of areas having different functions. FIG. **52**A illustrates an example where a region L**1**, a region L**2**, and a region L**3** are used as the L**1** cache, the L**2** cache, and the L**3** cache, respectively.
[0735] In the semiconductor device **970**B, the capacity of each of the regions L**1** to L**3** can be changed depending on circumstances. For example, the capacity of the L**1** cache can be increased by increasing the area of the region L**1**. With such a structure, the arithmetic processing efficiency can be improved and the processing speed can be improved.
[0736] Alternatively, a plurality of memory arrays may be stacked. FIG. **52**B is a perspective view of a semiconductor device **970**C.
[0737] In the semiconductor device **970**C, a layer **930**L**1** including the memory array **920**L**1**, a layer **930**L**2** including the memory array **920**L**2** over the layer **930**L**1**, and a layer **930**L**3** including the memory array **920**L**3** over the layer **930**L**2** are stacked. The memory array **920**L**1** physically closest to the arithmetic device **960** can be used as a high-level cache, and the memory array **920**L**3** physically farthest from the arithmetic device **960** can be used as a low-level cache or a main memory. Such a structure can increase the capacity of each memory array, leading to higher processing capability.
[0738] This embodiment can be combined with any of the other embodiments as appropriate. In this specification, in the case where a plurality of structure examples are shown in one embodiment, the structure examples can be combined as appropriate.

Embodiment 5

[0739] In this embodiment, an example of an application range of a semiconductor device of one embodiment of the present invention is described with reference to FIG. **53**.
[0740] A variety of memory devices are used in semiconductor devices such as computers in accordance with the intended use. FIG. **53** is a conceptual diagram showing a hierarchy of memory devices used in semiconductor devices. In the conceptual diagram in FIG. **53**, the hierarchy of memory devices is shown by a triangle; the memory devices at higher levels in the triangle require higher operation speed, and the memory devices at lower levels in the triangle require higher

storage capacity and higher record density.
[0741] In FIG. **53**, memories included as registers in arithmetic processing devices such as a CPU, a GPU, and an NPU, cache memories (sometimes simply referred to as caches, typically L**1**, L**2**, and L**3** caches), main memories typified by DRAMs, 3D NANDs, and storage memories typified by hard disks (also referred to as hard disk drives (HDDs)) are shown in this order from the highest level in the triangle.
[0742] A memory included as a register in an arithmetic processing device such as a CPU, a GPU, or an NPU is used for temporary storage of arithmetic operation results, for example, and thus is very frequently accessed by the arithmetic processing device. Accordingly, high operation speed is required rather than high storage capacity. The register also has a function of retaining settings of the arithmetic processing device, for example.
[0743] The cache memory has a function of duplicating and retaining part of data retained in the DRAM. Duplicating frequently used data and retaining the duplicated data in the cache memory facilitates rapid data access. The cache memory requires lower storage capacity but requires higher operation speed than the DRAM. Data that is rewritten in the cache memory is duplicated, and the duplicated data is supplied to the DRAM. Only L**1** to L**3** caches are shown as the cache memories in the example illustrated FIG. **53**, but one embodiment of the present invention is not limited to the example. For example, a memory device including the oxide semiconductor of one embodiment of the present invention can be suitably used as the last level cache (LLC) or a final level cache (FLC) positioned at the lowest level among the caches.
[0744] The DRAM has a function of retaining a program, data, or the like read from the 3D NAND.
[0745] The 3D NAND has a function of retaining data that needs to be stored for a long time, a variety of programs used in an arithmetic device (e.g., a model of an artificial neural network), and the like. Therefore, the 3D NAND requires high storage capacity and high record density rather than high operating speed.
[0746] The hard disk has high capacity and a nonvolatile function. Instead of the hard disk, a solid state drive (SSD) or the like can be used.
[0747] The memory device including the oxide semiconductor (OS memory) of one embodiment of the present invention can retain data for a long time. Thus, the memory device can be suitably used for devices in a region denoted as Target **1** in FIG. **53**. As indicated by hatching with oblique lines in FIG. **53**, Target **1** also includes part of the caches (L**1**, L**2**, and L**3**) and part of the 3D NAND. In other words, Target **1** includes a boundary region between the DRAM and the 3D NAND and a boundary region between the DRAM and the caches (L**1**, L**2**, and L**3**). The memory device including the oxide semiconductor of one embodiment of the present invention operates at high speed, and thus can achieve excellent writing operation and excellent reading operation. Thus, the memory device can be suitably used for a region denoted as Target **2** in FIG. **53**.
[0748] For example, the DRAM shown in FIG. **53** is suitably replaced with the memory device including the oxide semiconductor of one embodiment of the present invention. Refresh operation is essential for the DRAM, and the DRAM is a destructive read memory device and thus consumes higher power than other memory devices. Therefore, power consumption can be reduced with a structure not using the DRAM. With this structure, power consumption can be reduced to one-hundredth or less or one-thousandth or less that of a structure using the DRAM. Thus, global expansion of information processing devices, such as supercomputers (also referred to as a high performance computers (HPCs)), computers, and servers, having such a structure will lead to global warming mitigation.
[0749] As described above, the memory device including the oxide semiconductor of one embodiment of the present invention can be applied to a wide range of memories covering from a memory included as a register in an arithmetic processing device such as a CPU, a GPU, or an NPU to a memory in the boundary region between a DRAM and a 3D NAND.

[0750] This embodiment can be combined with any of the other embodiments as appropriate. In this specification, in the case where a plurality of structure examples are shown in one embodiment, the structure examples can be combined as appropriate.

Embodiment 6

[0751] In this embodiment, examples of a circuit structure including the OS transistor of one embodiment of the present invention and examples of electronic components using the semiconductor device of one embodiment of the present invention are described with reference to FIGS. **54**A to **54**C.

<Circuit Structure Example>

[0752] FIGS. **54**A and **54**B each illustrate an example of a circuit structure including the OS transistor of one embodiment of the present invention. The circuit diagram in FIG. **54**A illustrates a structure of an inverter circuit formed of what is called a complementary metal oxide semiconductor (CMOS) circuit in which an n-channel transistor **3102** and a p-channel transistor **3104** are connected in series and their gates are connected. The circuit diagram in FIG. **54**B illustrates a structure of a circuit that functions as what is called an analog switch, in which sources of the n-channel transistor **3102** and the p-channel transistor **3104** are connected to each other and drains of the n-channel transistor **3102** and the p-channel transistor **3104** are connected to each other.

<Transistor Structure>

[0753] Any of various types of transistors can be used as the n-channel transistor **3102** and the p-channel transistor **3104** illustrated in FIGS. **54**A and **54**B. Specifically, a planar transistor, a vertical transistor (also referred to as a vertical field effect transistor (VFET)), a Fin-type transistor, a gate all around (GAA) transistor, or the like can be used as the n-channel transistor **3102** and the p-channel transistor **3104**. A complementary field effect transistor (CFET) in which the n-channel transistor **3102** and the p-channel transistor **3104** are combined may be used. Note that a transistor having the same structure as or a different structure from the structure of any of the transistors described in the above embodiments may be used as the vertical transistor.

[0754] In this specification and the like, a planar transistor has a structure where a source electrode and a drain electrode are positioned at the same or substantially the same level and a current flowing through a semiconductor contains components in the lateral direction. In this specification and the like, a VFET has a structure where a source electrode and a drain electrode are positioned at different levels and a current flowing through a semiconductor contains components in the vertical direction. Since two or more of the source electrode, the semiconductor, and the drain electrode of the VFET can be provided to overlap with each other, the area occupied by the VFET can be much smaller than the area occupied by the planar transistor.

[0755] In this specification and the like, a Fin-type transistor has a structure where two or more surfaces of a channel are covered with a gate electrode with a gate insulating film therebetween in a cross-sectional view in the channel width direction. In particular, the channel height (H) is preferably larger than the channel width (W) in the cross-sectional view in the channel width direction, in which case the channel width per unit area can be increased. In this specification and the like, a GAA transistor has a structure where a gate electrode covers four surfaces of a channel with a gate insulating film therebetween in a cross-sectional view in the channel width direction.

<N-Channel Transistor>

[0756] An OS transistor of one embodiment of the present invention can be used as the n-channel transistor **3102** illustrated in FIGS. **54**A and **54**B. The OS transistor has an extremely low off-state current, and thus the leakage current of the n-channel transistor **3102** can be extremely low. In the n-channel transistor **3102**, a single element semiconductor such as silicon or germanium, a compound semiconductor such as gallium arsenide, a layered material functioning as a semiconductor, or the like can be used as a semiconductor material. In particular, a layered material functioning as a semiconductor is preferably used as a semiconductor material.

[0757] In this specification and the like, the layered material is a group of materials having a layered crystal structure. In the layered crystal structure, layers formed by covalent bonding or ionic bonding are stacked with bonding such as the van der Waals binding, which is weaker than covalent bonding or ionic bonding. The layered material has high electrical conductivity in a unit layer, that is, high two-dimensional electrical conductivity. When a material that functions as a semiconductor and has high two-dimensional electrical conductivity is used for a channel formation region, the transistor can have a high on-state current.

[0758] In this specification and the like, the above-described layered material is sometimes referred to as a two-dimensional material. Examples of a two-dimensional material that can be used for the n-channel transistor **3102** and the p-channel transistor **3104** in one embodiment of the present invention include graphene, silicene (a substance in which a carbon atom of graphene is replaced with a silicon atom), germanene (a substance in which a carbon atom of graphene is replaced with a germanium atom), transition metal chalcogenides or transition metal dichalcogenides (TMDs), boron nitride (BN), and black phosphorus. Using the above-described two-dimensional material can improve one or more physical properties of electron mobility, mechanical strength, and thermal conductivity, compared with the case of using a single element semiconductor such as silicon or germanium. The above-described two-dimensional material has excellent physical properties compared with a single element semiconductor such as silicon; thus, the two-dimensional material may be referred to as a new material channel (NMC).

[0759] Examples of the layered material include chalcogenide. Chalcogenide is a compound containing chalcogen. Chalcogen is a general term of elements belonging to Group 16, which includes oxygen, sulfur, selenium, tellurium, polonium, and livermorium. Examples of chalcogenide include transition metal chalcogenide and chalcogenide of Group 13 elements.

[0760] As a material that can be used for the n-channel transistor **3102**, a transition metal chalcogenide functioning as a semiconductor is preferably used, for example. Specific examples of the transition metal chalcogenide include molybdenum sulfide (typically MoS.sub.2), molybdenum selenide (typically MoSe.sub.2), molybdenum telluride (typically MoTe.sub.2), tungsten sulfide (typically WS.sub.2), tungsten selenide (typically WSe.sub.2), tungsten telluride (typically WTe.sub.2), hafnium sulfide (typically HfS.sub.2), hafnium selenide (typically HfSe.sub.2), zirconium sulfide (typically ZrS.sub.2), and zirconium selenide (typically ZrSe.sub.2).

<P-Channel Transistor>

[0761] In the p-channel transistor **3104** illustrated in FIGS. **54**A and **54**B, a single element semiconductor such as silicon or germanium, a compound semiconductor such as gallium arsenide, a layered material functioning as a semiconductor, or the like can be used as a semiconductor material. In particular, a layered material functioning as a semiconductor is preferably used as a semiconductor material.

[0762] As a material that can be used for the p-channel transistor **3104**, a transition metal chalcogenide functioning as a semiconductor is preferably used, for example. Specific examples of the transition metal chalcogenide include molybdenum sulfide (typically MoS.sub.2), molybdenum selenide (typically MoSe.sub.2), tungsten sulfide (typically WS.sub.2), and tungsten selenide (typically WSe.sub.2).

[0763] As the material that can be used for the p-channel transistor **3104**, other than the above-described two-dimensional material, a Group III-IV compound semiconductor (typically, a gallium-arsenic compound semiconductor, an indium-phosphorus compound semiconductor, an indium-gallium-arsenic compound semiconductor, an indium-arsenic compound semiconductor, or the like), a carbon nanotube (CNT), tin sulfide (typically, SnS), tin selenide (typically, SnSe), or the like can be used. In addition, a Group III-IV compound semiconductor may be used for the n-channel transistor **3102**.

<Electronic Component Example>

[0764] FIG. **54**C illustrates an example of an electronic component including the semiconductor

device of one embodiment of the present invention. An electronic component including the semiconductor device or the memory device of one embodiment of the present invention is effective in reducing power consumption and improving performance.

[0765] FIG. **54**C is a perspective view of a substrate (a circuit board **3210**) provided with an electronic component **3110**. The electronic component **3110** illustrated in FIG. **54**C includes a memory device **3112** in a mold **3111**. FIG. **54**C omits some components to show the inside of the electronic component **3110**. The electronic component **3110** includes a land **3113** outside the mold **3111**. The land **3113** is connected to an electrode pad **3114**, and the electrode pad **3114** is connected to the memory device **3112** through a wire **3115**. The electronic component **3110** is mounted on a printed wiring board **3212**, for example. A plurality of such electronic components are combined and electrically connected to each other on the printed circuit board **3212**, which results in formation of the circuit board **3210**.

[0766] The memory device **3112** includes a layer **3121** including an arithmetic core and a layer **3122** including a memory. For example, the above-described n-channel transistor and p-channel transistor can be used in both the layer **3121** and the layer **3122**. It is particularly preferable that a p-channel transistor be used in the layer **3121** and an n-channel transistor be used in the layer **3122** to form a CMOS circuit. However, one embodiment of the present invention is not limited thereto, and both an n-channel transistor and a p-channel transistor may be included in the layer **3121** and an n-channel transistor may be used in the layer **3122**.

[0767] Specifically, it is preferable that the layer **3121** include a p-channel transistor **3301** and the layer **3122** include an n-channel transistor **3302**. In FIG. **54**C, when a semiconductor layer **3311** included in the transistor **3301** is p-channel silicon and a semiconductor layer **3312** included in the transistor **3302** is an n-channel oxide semiconductor, a stacked-layer structure of a Si transistor and an OS transistor can be obtained.

[0768] Alternatively, in FIG. **54**C, when the semiconductor layer **3311** included in the transistor **3301** is a p-channel two-dimensional material (e.g., WS.sub.2) and the semiconductor layer **3312** included in the transistor **3302** is an n-channel oxide semiconductor, a stacked-layer structure of a WS.sub.2 transistor and an OS transistor can be obtained. With such a stacked-layer structure, a memory device with low power consumption and high performance can be provided.

[0769] Stacking the two kinds of transistors reduces the area occupied by the circuit, allowing a plurality of circuits to be arranged at high density. FIG. **54**C illustrates a structure where the transistor **3301** is a Fin-type transistor and the transistor **3302** is a VFET as a non-limiting example, but a Fin-type transistor may be used as the transistor **3301** and a Fin-type transistor may be used as the transistor **3302**. It is preferable that the transistor **3301** and the transistor **3302** have different structures, in which case characteristics according to the respective transistor structures can be obtained. It is also preferable that the transistor **3301** and the transistor **3302** have the same structure, in which case some manufacturing apparatuses can be used in common.

[0770] The layer **3122** including the memory has a structure where a plurality of memory cell arrays are stacked. The layer **3121** including the arithmetic core and the layer **3122** including the memory can be stacked monolithically. In the monolithic stacked-layer structure, layers can be connected to each other without using a through electrode technique such as a through silicon via (TSV) technique and a bonding technique such as Cu—Cu direct bonding. The monolithic stacked-layer structure of the layer **3121** including the arithmetic core and the layer **3122** including the memory enables, for example, what is called an on-chip memory structure where a memory is directly formed on a processor. The on-chip memory structure allows an interface portion between the processor and the memory to operate at high speed. In addition, part of the function (part of the arithmetic function) of the layer **3121** including the arithmetic core may be provided in part of the layer **3122** including the memory.

[0771] With the on-chip memory structure, the sizes of a connection wiring and the like can be smaller than those in the case where the through electrode technique such as TSV is employed;

thus, the number of connection pins can be increased. The increase in the number of connection pins enables parallel operations, which can improve the bandwidth of the memory (also referred to as a memory bandwidth).

[0772] It is preferable that the plurality of memory cell arrays included in the layer **3122** including the memory be formed with OS transistors and be monolithically stacked. The monolithic stacked-layer structure of memory cell arrays can improve the bandwidth of the memory and/or the access latency of the memory. The bandwidth refers to the data transfer volume per unit time, and the access latency refers to a period of time from data access to the start of data transmission. In the case where the layer **3122** including the memory is formed with Si transistors, the monolithic stacked-layer structure is difficult to form as compared with the case where the layer **3122** including the memory is formed with OS transistors. Therefore, an OS transistor is superior to a Si transistor in the monolithic stacked-layer structure.

[0773] This embodiment can be combined with any of the other embodiments as appropriate. In this specification, in the case where a plurality of structure examples are shown in one embodiment, the structure examples can be combined as appropriate.

Embodiment 7

[0774] In this embodiment, application examples of the semiconductor device or the memory device of one embodiment of the present invention are described with reference to FIG. **55**, FIGS. **56**A to **56**E, FIGS. **57**A to **57**F, FIGS. **58**A to **58**G, and FIGS. **59**A to **59**F.

[0775] The semiconductor device or the memory device of one embodiment of the present invention can be used for an electronic component, a large computer, space equipment, a data center (also referred to as DC), and a variety of electronic apparatuses, for example. With the use of the semiconductor device or the memory device of one embodiment of the present invention, an electronic component, a large computer, space equipment, a data center, and a variety of electronic apparatuses can have lower power consumption and higher performance.

[0776] Examples of the electronic apparatuses include a digital camera, a digital video camera, a digital photo frame, a mobile phone, a portable game console, a portable information terminal, and an audio reproducing device, in addition to electronic apparatuses with a relatively large screen, such as a television device, desktop and laptop personal computers, a monitor of a computer and the like, digital signage, and a large game machine such as a pachinko machine.

[0777] Examples of such an electronic apparatus include watch-type and bracelet-type information terminal devices (wearable devices) and wearable devices that can be worn on a head, such as a VR device like a head-mounted display, a glasses-type AR device, and an MR device.

[0778] The electronic apparatus in this embodiment may include a sensor (a sensor having a function of sensing, detecting, or measuring force, displacement, position, speed, acceleration, angular velocity, rotational frequency, distance, light, liquid, magnetism, temperature, a chemical substance, sound, time, hardness, electric field, current, voltage, electric power, radiation, flow rate, humidity, gradient, oscillation, a smell, or infrared rays).

[0779] The electronic apparatus in this embodiment can have a variety of functions. For example, the electronic apparatus in this embodiment can have a function of displaying a variety of information (a still image, a moving image, a text image, and the like) on the display portion, a touch panel function, a function of displaying a calendar, date, time, and the like, a function of executing a variety of software (programs), a wireless communication function, and a function of reading out a program or data stored in a recording medium.

[Electronic Component]

[0780] FIG. **55** is a perspective view of an electronic component **730**. The electronic component **730** is an example of a system in package (SiP) or a multi-chip module (MCM). In the electronic component **730**, an interposer **731** is provided over a package substrate **732** (printed circuit board), and a semiconductor device **735** and a plurality of semiconductor devices **710** are provided over the interposer **731**.

[0781] The memory device **3112** described in Embodiment 6 can be used for the semiconductor device **710**.
[0782] The electronic component **730** using the semiconductor device **710** as a high bandwidth memory (HBM) is illustrated as an example. The semiconductor device **735** can be used for an integrated circuit such as a CPU, a GPU, or a field programmable gate array (FPGA).
[0783] As the package substrate **732**, a ceramic substrate, a plastic substrate, or a glass epoxy substrate can be used, for example. As the interposer **731**, a silicon interposer or a resin interposer can be used, for example.
[0784] The interposer **731** includes a plurality of wirings and has a function of connecting a plurality of integrated circuits with different terminal pitches. The plurality of wirings are provided in a single layer or multiple layers. In addition, the interposer **731** has a function of connecting an integrated circuit provided on the interposer **731** to an electrode provided on the package substrate **732**. Accordingly, the interposer is referred to as a "redistribution substrate" or an "intermediate substrate" in some cases. Furthermore, a through electrode is provided in the interposer **731** and the through electrode is used to connect an integrated circuit and the package substrate **732** in some cases. Moreover, in the case of using a silicon interposer, a TSV can also be used as the through electrode.
[0785] An HBM needs to be connected to many wirings to achieve a wide memory bandwidth. Therefore, an interposer on which an HBM is mounted requires minute and densely formed wirings. For this reason, a silicon interposer is preferably used as the interposer on which an HBM is mounted.
[0786] In a SiP, an MCM, or the like using a silicon interposer, a decrease in reliability due to a difference in the coefficient of expansion between an integrated circuit and the interposer is less likely to occur. Furthermore, a surface of a silicon interposer has high flatness; thus, poor connection between the silicon interposer and an integrated circuit provided on the silicon interposer is less likely to occur. It is particularly preferable to use a silicon interposer for a 2.5D package (2.5-dimensional packaging) in which a plurality of integrated circuits are arranged side by side on the interposer.
[0787] In the case where a plurality of integrated circuits with different terminal pitches are connected with use of a silicon interposer, a TSV, and the like, a space for a width or the like of the terminal pitch is needed. Accordingly, in the case where the size of the electronic component **730** is reduced, the width of the terminal pitch becomes an issue, which sometimes makes it difficult to provide a large number of wirings for obtaining a wide memory bandwidth. For this reason, the above-described monolithic stacked-layer structure using OS transistors is suitable. A composite structure combining memory cell arrays stacked using a TSV and monolithically stacked memory cell arrays may be employed.
[0788] In addition, a heat sink (a radiator plate) may be provided to overlap with the electronic component **730**. In the case of providing a heat sink, the heights of integrated circuits provided on the interposer **731** are preferably equal to each other. For example, in the electronic component **730** described in this embodiment, the heights of the semiconductor devices **710** and the semiconductor device **735** are preferably equal to each other.
[0789] To mount the electronic component **730** on another substrate, an electrode **733** may be provided on a bottom portion of the package substrate **732**. FIG. **55** illustrates an example where the electrode **733** is formed of a solder ball. Solder balls are provided in a matrix on the bottom portion of the package substrate **732**, so that ball grid array (BGA) packaging can be achieved. Alternatively, the electrode **733** may be formed of a conductive pin. When conductive pins are provided in a matrix on the bottom portion of the package substrate **732**, pin grid array (PGA) packaging can be achieved.
[0790] The electronic component **730** can be mounted on another substrate by various packaging methods other than BGA and PGA. Examples of a packaging method include staggered pin grid

array (SPGA), land grid array (LGA), quad flat package (QFP), quad flat J-leaded package (QFJ), and quad flat non-leaded package (QFN).

[0791] The semiconductor device **710** may be called a die. Note that in this specification and the like, a die refers to a chip obtained by, for example, forming a circuit pattern on a disc-like substrate (also referred to as a wafer) or the like and cutting the substrate with the pattern into dices in a process of manufacturing a semiconductor chip. Examples of semiconductor materials that can be used for the die include silicon (Si), silicon carbide (SiC), and gallium nitride (GaN). For example, a die obtained from a silicon substrate (also referred to as a silicon wafer) is referred to as a silicon die in some cases.

[Large Computer]

[0792] FIG. **56**A is a perspective view of a large computer **5600**. In the large computer **5600** illustrated in FIG. **56**A, a plurality of rack mount computers **5620** are stored in a rack **5610**. Note that the large computer **5600** may be referred to as a supercomputer.

[0793] The computer **5620** can have a structure illustrated in a perspective view in FIG. **56**B, for example. In FIG. **56**B, the computer **5620** includes a motherboard **5630**, and the motherboard **5630** includes a plurality of slots **5631** and a plurality of connection terminals. A PC card **5621** is inserted in the slot **5631**. In addition, the PC card **5621** includes a connection terminal **5623**, a connection terminal **5624**, and a connection terminal **5625**, each of which is connected to the motherboard **5630**.

[0794] The PC card **5621** illustrated in FIG. **56**C is an example of a processing board provided with a CPU, a GPU, a memory device, and the like. The PC card **5621** includes a board **5622**. The board **5622** includes a connection terminal **5623**, a connection terminal **5624**, a connection terminal **5625**, a semiconductor device **5626**, a semiconductor device **5627**, a semiconductor device **5628**, and a connection terminal **5629**. FIG. **56**C also illustrates semiconductor devices other than the semiconductor devices **5626**, **5627**, and **5628**, and the following description of the semiconductor devices **5626**, **5627**, and **5628** can be referred to for the semiconductor devices.

[0795] The connection terminal **5629** has a shape with which the connection terminal **5629** can be inserted in the slot **5631** of the motherboard **5630**, and the connection terminal **5629** functions as an interface for connecting the PC card **5621** and the motherboard **5630**. An example of the standard for the connection terminal **5629** is PCIe.

[0796] The connection terminal **5623**, the connection terminal **5624**, and the connection terminal **5625** can each serve as, for example, an interface for performing power supply, signal input, or the like to the PC card **5621**. For another example, they can each serve as an interface for outputting a signal calculated by the PC card **5621**. Examples of the standard for each of the connection terminal **5623**, the connection terminal **5624**, and the connection terminal **5625** include Universal Serial Bus (USB), Serial ATA (SATA), and Small Computer System Interface (SCSI). In the case where video signals are output from the connection terminal **5623**, the connection terminal **5624**, and the connection terminal **5625**, an example of the standard therefor is HDMI (registered trademark).

[0797] The semiconductor device **5626** includes a terminal (not illustrated) for inputting and outputting signals, and when the terminal is inserted in a socket (not illustrated) of the board **5622**, the semiconductor device **5626** and the board **5622** can be electrically connected to each other.

[0798] The semiconductor device **5627** includes a plurality of terminals, and when the terminals are reflow-soldered, for example, to wirings of the board **5622**, the semiconductor device **5627** and the board **5622** can be connected to each other. Examples of the semiconductor device **5627** include an FPGA, a GPU, and a CPU. As the semiconductor device **5627**, the electronic component **730** can be used, for example.

[0799] The semiconductor device **5628** includes a plurality of terminals, and when the terminals are reflow-soldered, for example, to wirings of the board **5622**, the semiconductor device **5628** and the board **5622** can be connected to each other. An example of the semiconductor device **5628** is a

memory device or the like. As the semiconductor device **5628**, the electronic component **3110** can be used, for example.

[0800] The large computer **5600** can also function as a parallel computer. When the large computer **5600** is used as a parallel computer, large-scale computation necessary for artificial intelligence learning and inference can be performed, for example.

[Space Equipment]

[0801] The semiconductor device or the memory device of one embodiment of the present invention can be suitably used as space equipment.

[0802] The semiconductor device or the memory device of one embodiment of the present invention includes an OS transistor. A change in electrical characteristics of the OS transistor due to radiation irradiation is small. That is, the OS transistor is highly resistant to radiation, and thus can be suitably used in an environment where radiation can enter. For example, the OS transistor can be suitably used in outer space. Specifically, the OS transistor can be used as a transistor in a semiconductor device provided in a space shuttle, an artificial satellite, or a space probe. Examples of radiation include X-rays and a neutron beam. Note that outer space refers to, for example, space at an altitude of 100 km or higher, and outer space described in this specification can include one or more of thermosphere, mesosphere, and stratosphere.

[0803] FIG. **56**D illustrates an artificial satellite **6800** as an example of space equipment. The artificial satellite **6800** includes a body **6801**, a solar panel **6802**, an antenna **6803**, a secondary battery **6805**, and a control device **6807**. In FIG. **56**D, a planet **6804** in outer space is illustrated as an example.

[0804] Although not illustrated in FIG. **56**D, a battery management system (also referred to as BMS) or a battery control circuit may be provided in the secondary battery **6805**. The battery management system or the battery control circuit preferably uses the OS transistor, in which case low power consumption and high reliability are achieved even in outer space.

[0805] The amount of radiation in outer space is 100 or more times that on the ground. Examples of radiation include electromagnetic waves (electromagnetic radiation) typified by X-rays and gamma rays and particle radiation typified by alpha rays, beta rays, neutron beam, proton beam, heavy-ion beams, and meson beams.

[0806] When the solar panel **6802** is illuminated with sunlight, electric power required for operation of the artificial satellite **6800** is generated. However, for example, in the situation where the solar panel is not illuminated with sunlight or the situation where the amount of sunlight with which the solar panel is illuminated is small, the amount of generated electric power is small. Accordingly, a sufficient amount of electric power required for operation of the artificial satellite **6800** might not be generated. In order to operate the artificial satellite **6800** even with a small amount of generated electric power, the artificial satellite **6800** is preferably provided with the secondary battery **6805**. Incidentally, a solar panel is referred to as a solar cell module in some cases.

[0807] The artificial satellite **6800** can generate a signal. The signal is transmitted through the antenna **6803**, and can be received by a ground-based receiver or another artificial satellite, for example. When the signal transmitted by the artificial satellite **6800** is received, the position of a receiver that receives the signal can be measured. Thus, the artificial satellite **6800** can construct a satellite positioning system.

[0808] The control device **6807** has a function of controlling the artificial satellite **6800**. The control device **6807** is formed with one or more selected from a CPU, a GPU, and a memory device, for example. Moreover, the semiconductor device or the memory device including the OS transistor of one embodiment of the present invention is suitably used for the control device **6807**. A change in electrical characteristics due to radiation irradiation is smaller in an OS transistor than in a Si transistor. Accordingly, the OS transistor has high reliability and thus can be suitably used even in an environment where radiation can enter.

[0809] The artificial satellite **6800** can include a sensor. For example, with a structure including a visible light sensor, the artificial satellite **6800** can have a function of detecting sunlight reflected by a ground-based object. Alternatively, with a structure including a thermal infrared sensor, the artificial satellite **6800** can have a function of detecting thermal infrared rays emitted from the surface of the earth. Thus, the artificial satellite **6800** can function as an earth observing satellite, for example.

[0810] Although the artificial satellite is described as an example of space equipment in this embodiment, one embodiment of the present invention is not limited to this example. The semiconductor device or the memory device of one embodiment of the present invention can be suitably used for space equipment such as a spacecraft, a space capsule, or a space probe, for example.

[0811] As described above, the OS transistor has advantageous effects over the Si transistor, such as a wide memory bandwidth and high radiation resistance.

[Data Center]

[0812] The semiconductor device or the memory device of one embodiment of the present invention can be suitably used for, for example, a storage system in a data center or the like. Long-term management of data, such as guarantee of data immutability, is required for the data center. The long-term management of data needs setting a storage and a server for storing a huge amount of data, stable power supply for retaining data, cooling equipment for retaining data, an increase in building size, and the like.

[0813] With use of the semiconductor device or the memory device of one embodiment of the present invention for a storage system in a data center, electric power used for retaining data can be reduced and a semiconductor device for retaining data can be downsized. Accordingly, downsizing of the storage system and the power supply for retaining data, downscaling of the cooling equipment, and the like can be achieved. Therefore, a space of the data center can be reduced.

[0814] Since the semiconductor device or the memory device of one embodiment of the present invention has low power consumption, heat generation from a circuit can be reduced. Accordingly, adverse effects of the heat generation on the circuit itself, the peripheral circuit, and the module can be reduced. Furthermore, the use of the semiconductor device or the memory device of one embodiment of the present invention can achieve a data center that operates stably even in a high temperature environment. Thus, the reliability of the data center can be increased.

[0815] FIG. **56**E illustrates a storage system that can be used in a data center. A storage system **7010** illustrated in FIG. **56**E includes a plurality of servers **7001***sb* as a host **7001**. The storage system **7010** includes a plurality of memory devices **7003***md* as a storage **7003**. In the illustrated example, the host **7001** and the storage **7003** are connected to each other via a storage area network **7004** and a storage control circuit **7002**.

[0816] The host **7001** corresponds to a computer that accesses data stored in the storage **7003**. The host **7001** may be connected to another host **7001** through a network.

[0817] The data access speed, i.e., the time taken for storing and outputting data, of the storage **7003** is shortened by using a flash memory, but is still much longer than the data access speed of a DRAM that can be used as a cache memory in a storage. In the storage system, in order to solve the problem of low access speed of the storage **7003**, a cache memory is normally provided in the storage to shorten the time taken for storing and outputting data.

[0818] The above-described cache memory is used in the storage control circuit **7002** and the storage **7003**. The data transmitted between the host **7001** and the storage **7003** is stored in the cache memories in the storage control circuit **7002** and the storage **7003** and then output to the host **7001** or the storage **7003**.

[0819] With a structure where an OS transistor is used as a transistor for storing data in the cache memory to retain a potential based on data, the frequency of refreshing can be decreased, so that power consumption can be reduced. Furthermore, downscaling is possible by stacking memory cell

arrays.

[Electronic Apparatus]

[0820] Examples of a wearable device that can be worn on a head are described with reference to FIGS. **57**A to **57**F. The wearable device has at least one of a function of displaying AR contents, a function of displaying VR contents, a function of displaying SR contents, and a function of displaying MR contents. The electronic apparatus having a function of displaying contents of at least one of AR, VR, SR, MR, and the like enables the user to feel a higher level of immersion.

[0821] An electronic apparatus **700**A illustrated in FIG. **57**A includes a pair of display panels **751**, a pair of housings **721**, a communication portion (not illustrated), a pair of wearing portions **723**, a control portion **724**, an image capturing portion (not illustrated), a pair of optical members **753**, a frame **757**, and a pair of nose pads **758**.

[0822] The semiconductor device or the memory device of one embodiment of the present invention can be used for the control portion **724**. Thus, power consumption of the electronic apparatus can be reduced.

[0823] The electronic apparatus **700**A can project images displayed on the display panels **751** onto display regions **756** of the optical members **753**. Since the optical members **753** have a light-transmitting property, the user can see images displayed on the display regions, which are superimposed on transmission images seen through the optical members **753**. Accordingly, the electronic apparatus **700**A is an electronic apparatus capable of AR display.

[0824] In the electronic apparatus **700**A, a camera capable of capturing images of the front side may be provided as the image capturing portion. Furthermore, when the electronic apparatus **700**A is provided with an acceleration sensor such as a gyroscope sensor, the orientation of the user's head can be sensed and an image corresponding to the orientation can be displayed on the display regions **756**.

[0825] The communication portion includes a wireless communication device, and a video signal and the like can be supplied by the wireless communication device. Instead of or in addition to the wireless communication device, a connector that can be connected to a cable for supplying a video signal and a power supply potential may be provided.

[0826] The electronic apparatus **700**A is provided with a battery so that charging can be performed wirelessly and/or by wire.

[0827] A touch sensor module may be provided in the housing **721**. The touch sensor module has a function of detecting a touch on the outer surface of the housing **721**. Detecting a tap operation, a slide operation, or the like by the user with the touch sensor module enables various types of processing. For example, a video can be paused or restarted by a tap operation, and can be fast-forwarded or fast-reversed by a slide operation. When the touch sensor module is provided in each of the two housings **721**, the range of the operation can be increased.

[0828] An electronic apparatus **800**A illustrated in FIG. **57**B and an electronic apparatus **800**B illustrated in FIG. **57**C each include a pair of display portions **820**, a housing **821**, a communication portion **822**, a pair of wearing portions **823**, a control portion **824**, a pair of image capturing portions **825**, and a pair of lenses **832**.

[0829] The semiconductor device or the memory device of one embodiment of the present invention can be used for the control portion **824**. Thus, power consumption of the electronic apparatus can be reduced.

[0830] The display portions **820** are positioned inside the housing **821** so as to be seen through the lenses **832**. When the pair of display portions **820** display different images, three-dimensional display using parallax can be performed.

[0831] The electronic apparatuses **800**A and **800**B can be regarded as electronic apparatuses for VR. The user wearing the electronic apparatus **800**A or the electronic apparatus **800**B can see images displayed on the display portions **820** through the lenses **832**.

[0832] The electronic apparatuses **800**A and **800**B preferably include a mechanism for adjusting

horizontally the positions of the lenses **832** and the display portions **820** so that the lenses **832** and the display portions **820** are positioned optimally in accordance with the positions of the user's eyes. Moreover, the electronic apparatuses **800**A and **800**B preferably include a mechanism for adjusting focus by changing the distance between the lenses **832** and the display portions **820**.

[0833] The electronic apparatus **800**A or the electronic apparatus **800**B can be mounted on the user's head with the wearing portions **823**. FIG. **57**B and the like illustrate an example where the wearing portion **823** has a shape like a temple of glasses; however, one embodiment of the present invention is not limited thereto. The wearing portion **823** may have any shape with which the user can wear the electronic apparatus, such as a shape of a helmet or a band.

[0834] The image capturing portion **825** has a function of obtaining information on the external environment. Data obtained by the image capturing portion **825** can be output to the display portion **820**. An image sensor can be used for the image capturing portion **825**. Moreover, a plurality of cameras may be provided so as to cover a plurality of fields of view, such as a telescope field of view and a wide field of view.

[0835] An example where the image capturing portions **825** are provided is shown here, but the image capturing portions **825** may be omitted when a range sensor (hereinafter also referred to as a sensing portion) capable of measuring a distance between the user and an object is provided. In other words, the image capturing portion **825** is one mode of the sensing portion. As the sensing portion, an image sensor or a range image sensor such as a light detection and ranging (LiDAR) sensor can be used, for example. By using images obtained by the camera and images obtained by the range image sensor, more information can be obtained and a gesture operation with higher accuracy is possible.

[0836] The electronic apparatus **800**A may include a vibration mechanism that functions as bone-conduction earphones. For example, at least one of the display portion **820**, the housing **821**, and the wearing portion **823** can include the vibration mechanism. Thus, without additionally requiring an audio device such as headphones, earphones, or a speaker, the user can enjoy images and sound only by wearing the electronic apparatus **800**A.

[0837] The electronic apparatuses **800**A and **800**B may each include an input terminal. To the input terminal, a cable for supplying a video signal from a video output device or the like, power for charging the battery provided in the electronic apparatus, or the like can be connected.

[0838] The electronic apparatus of one embodiment of the present invention may have a function of performing wireless communication with earphones **750**. The earphones **750** include a communication portion (not illustrated) and have a wireless communication function. The earphones **750** can receive information (e.g., audio data) from the electronic apparatus with the wireless communication function. For example, the electronic apparatus **700**A in FIG. **57**A has a function of transmitting information to the earphones **750** with the wireless communication function.

[0839] The electronic apparatus may include an earphone portion. The electronic apparatus **800**B in FIG. **57**C includes earphone portions **827**. For example, the earphone portion **827** can be connected to the control portion **824** by wire. Part of a wiring that connects the earphone portion **827** and the control portion **824** may be positioned inside the housing **821** or the wearing portion **823**. Additionally, the earphone portions **827** and the wearing portions **823** may include magnets. This is preferable because the earphone portions **827** can be fixed to the wearing portions **823** with magnetic force and thus can be easily housed.

[0840] The electronic apparatus may include an audio output terminal to which earphones, headphones, or the like can be connected. The electronic apparatus may include one or both of an audio input terminal and an audio input mechanism. As the audio input mechanism, a sound collecting device such as a microphone can be used, for example. The electronic apparatus may have a function of a headset by including the audio input mechanism.

[0841] FIGS. **57**D and **57**E are perspective views of a goggles-type electronic apparatus **850**A for

VR. FIGS. **57**D and **57**E illustrate an example where a housing **845** includes a pair of curved display devices **840** (a display device **840**_R and a display device **840**_L). The electronic apparatus **850**A includes a motion detection portion **841**, an eye-gaze detection portion **842**, an arithmetic portion **843**, a communication portion **844**, lenses **848**, an operation button **851**, a wearing tool **854**, a sensor **855**, a dial **856**, and the like.

[0842] When the two display devices **840** are provided, the user's eyes can see the respective display devices. This allows a high-resolution image to be displayed even when three-dimensional display using parallax or the like is performed. In addition, the display device **840** is curved around an arc with an approximate center at the user's eye. This keeps a certain distance between the user's eye and the display surface of the display device **840**, enabling the user to see a more natural image. Even when having what is called viewing angle dependence where the luminance or chromaticity of light changes depending on a viewing angle, the display device **840** can have a structure where the user's eye is positioned in the normal direction of the display surface of the display device **840**; accordingly, the influence of the viewing angle dependence particularly in the horizontal direction can be practically ignored, enabling display of a more realistic video.

[0843] As illustrated in FIG. **57**E, the lenses **848** are positioned between the display devices **840** and the user's eyes. FIG. **57**E illustrates an example where the dial **856** for changing the positions of the lenses for visibility adjustment is provided. In addition, in the case where the electronic apparatus **850**A has an autofocus function, the dial **856** for visibility adjustment is not necessarily provided.

[0844] FIG. **57**F illustrates a goggles-type electronic apparatus **850**B including one display device **840**. Such a structure can reduce the number of components.

[0845] The display device **840** can display an image for the right eye and an image for the left eye side by side on a right region and a left region, respectively. Thus, a three-dimensional image using binocular parallax can be displayed. Note that the display device **840** may display two different images side by side using parallax, or may display two same images side by side without using parallax.

[0846] One image which can be seen with both eyes may be displayed on the entire display device **840**. Thus, a panorama image can be displayed from end to end of the field of view, which can provide a higher sense of reality.

[0847] An electronic apparatus **6500** illustrated in FIG. **58**A is a portable information terminal that can be used as a smartphone.

[0848] The electronic apparatus **6500** includes a housing **6501**, a display portion **6502**, a power button **6503**, buttons **6504**, a speaker **6505**, a microphone **6506**, a camera **6507**, a light source **6508**, a control device **6509**, and the like.

[0849] An electronic apparatus **6520** illustrated in FIG. **58**B is a portable information terminal that can be used as a tablet terminal.

[0850] The electronic apparatus **6520** includes the housing **6501**, the display portion **6502**, the buttons **6504**, the speaker **6505**, the microphone **6506**, the camera **6507**, the control device **6509**, a connection terminal **6519**, and the like.

[0851] In each of the electronic apparatus **6500** and the electronic apparatus **6520**, the display portion **6502** has a touch panel function. Note that the control device **6509** includes, for example, one or more selected from a CPU, a GPU, and a memory device. The semiconductor device or the memory device of one embodiment of the present invention can be used for the control device **6509**.

[0852] FIG. **58**C is a schematic cross-sectional view including an end portion of the housing **6501** included in the electronic apparatus **6500** or the electronic apparatus **6520** on the microphone **6506** side.

[0853] A protection member **6510** having a light-transmitting property is provided on the display surface side of the housing **6501**. A display panel **6511**, an optical member **6512**, a touch sensor

panel **6513**, a printed circuit board **6517**, a battery **6518**, and the like are provided in a space surrounded by the housing **6501** and the protection member **6510**.
[0854] The display panel **6511**, the optical member **6512**, and the touch sensor panel **6513** are fixed to the protection member **6510** with an adhesive layer (not illustrated).
[0855] Part of the display panel **6511** is folded back in a region outside the display portion **6502**, and an FPC **6515** is connected to the part that is folded back. An IC **6516** is mounted on the FPC **6515**. The FPC **6515** is connected to a terminal provided on the printed circuit board **6517**.
[0856] FIG. **58**D illustrates an example of a television device. In a television device **7100**, a display portion **7000** is incorporated in a housing **7101**. Here, the housing **7101** is supported by a stand **7103**.
[0857] Operation of the television device **7100** illustrated in FIG. **58**D can be performed with an operation switch provided in the housing **7101** and a separate remote controller **7111**. Alternatively, the display portion **7000** may include a touch sensor, and the television device **7100** may be operated by touch on the display portion **7000** with a finger or the like. The remote controller **7111** may be provided with a display portion for displaying information output from the remote controller **7111**. With operation keys or a touch panel provided in the remote controller **7111**, channels and volume can be controlled and videos displayed on the display portion **7000** can be controlled.
[0858] Note that the television device **7100** includes a receiver, a modem, and the like. A general television broadcast can be received with the receiver. When the television device is connected to a communication network by wire or wirelessly via the modem, one-way (from a transmitter to a receiver) or two-way (between a transmitter and a receiver or between receivers, for example) data communication can be performed.
[0859] FIG. **58**E illustrates an example of a laptop personal computer. The laptop personal computer **7200** includes a housing **7211**, a keyboard **7212**, a pointing device **7213**, an external connection port **7214**, a control device **7215**, and the like. The display portion **7000** is incorporated in the housing **7211**. The control device **7215** includes, for example, one or more selected from a CPU, a GPU, and a memory device. The semiconductor device or the memory device of one embodiment of the present invention can be used for the control device **7215**.
[0860] FIGS. **58**F and **58**G illustrate examples of digital signage.
[0861] Digital signage **7300** illustrated in FIG. **58**F includes a housing **7301**, the display portion **7000**, a speaker **7303**, and the like. The digital signage **7300** can also include an LED lamp, an operation key (including a power switch or an operation switch), a connection terminal, a variety of sensors, a microphone, and the like.
[0862] FIG. **58**G is digital signage **7400** attached to a cylindrical pillar **7401**. The digital signage **7400** includes the display portion **7000** provided along a curved surface of the pillar **7401**.
[0863] A larger area of the display portion **7000** can increase the amount of information that can be provided at a time. The display portion **7000** having a larger area attracts more attention, so that the effectiveness of the advertisement can be increased, for example.
[0864] A touch panel is preferably used in the display portion **7000**, in which case intuitive operation by a user is possible in addition to display of an image or a moving image on the display portion **7000**. Moreover, for an application for providing information such as route information or traffic information, usability can be enhanced by intuitive operation.
[0865] As illustrated in FIGS. **58**F and **58**G, it is preferable that the digital signage **7300** or the digital signage **7400** can work with an information terminal **7311** or an information terminal **7411**, such as a smartphone of a user, through wireless communication. For example, information of an advertisement displayed on the display portion **7000** can be displayed on a screen of the information terminal **7311** or the information terminal **7411**. By operation of the information terminal **7311** or the information terminal **7411**, display on the display portion **7000** can be switched.

[0866] It is possible to make the digital signage **7300** or the digital signage **7400** execute a game with use of the screen of the information terminal **7311** or the information terminal **7411** as an operation means (controller). Thus, an unspecified number of users can join in and enjoy the game concurrently.
[0867] The semiconductor device or the memory device of one embodiment of the present invention can be used around a driver's seat in a car, which is a vehicle.
[0868] FIG. **59**A illustrates the vicinity of a windshield inside a car. FIG. **59**A illustrates a display panel **9001***a*, a display panel **9001***b*, and a display panel **9001***c* attached to a dashboard and a display panel **9001***d* attached to a pillar.
[0869] The display panels **9001***a* to **9001***c* can provide various kinds of information by displaying navigation data, a speedometer, a tachometer, a mileage, a fuel meter, a gearshift state, air-conditioning settings, and the like. Items displayed on the display panel, their layout, and the like can be changed as appropriate to suit the user's preferences, resulting in more sophisticated design. The display panels **9001***a* to **9001***c* can also be used as lighting devices.
[0870] The display panel **9001***d* can complement a view hindered by the pillar (blind areas) by displaying an image taken by an imaging unit provided for the car body. That is, displaying an image taken by the imaging unit provided on the exterior of the car leads to elimination of blind areas and enhancement of safety. Moreover, showing an image to complement an area that a driver cannot see makes it possible for the driver to confirm safety more easily and comfortably. The display panel **9001***d* can also be used as a lighting device.
[0871] FIG. **59**B is a perspective view of a watch-type portable information terminal **9200**. The portable information terminal **9200** can be used as a Smartwatch (registered trademark), for example. The display surface of the display portion **9001** is curved, and an image can be displayed on the curved display surface. Furthermore, for example, mutual communication between the portable information terminal **9200** and a headset capable of wireless communication can be performed, and thus hands-free calling is possible. With a connection terminal **9006**, the portable information terminal **9200** can perform mutual data transmission with another information terminal and charging. Note that the charging operation may be performed by wireless power feeding.
[0872] The portable information terminal **9200** illustrated in FIG. **59**B includes a housing **9000**, the display portion **9001**, a speaker **9003**, an operation key **9005** (including a power switch or an operation switch), the connection terminal **9006**, a sensor **9007** (a sensor having a function of sensing, detecting, or measuring force, displacement, position, speed, acceleration, angular velocity, rotational frequency, distance, light, liquid, magnetism, temperature, a chemical substance, sound, time, hardness, electric field, current, voltage, electric power, radiation, flow rate, humidity, gradient, oscillation, a smell, or infrared rays), a microphone **9008**, and the like.
[0873] FIG. **59**C is a perspective view of a foldable portable information terminal **9201**. The portable information terminal **9201** includes a housing **9000***a*, a housing **9000***b*, the display portion **9001**, and operation buttons **9056**.
[0874] The housing **9000***a* and the housing **9000***b* are bonded to each other with a hinge **9055** that allows the display portion **9001** to be folded in half.
[0875] The display portion **9001** of the portable information terminal **9201** is supported by two housings (the housing **9000***a* and the housing **9000***b*) joined together with the hinge **9055**.
[0876] FIGS. **59**D to **59**F are perspective views illustrating a foldable portable information terminal **9202**. FIG. **59**D is a perspective view of an opened state of the portable information terminal **9202**, FIG. **59**F is a perspective view of a folded state thereof, and FIG. **59**E is a perspective view of a state in the middle of change from one of FIG. **59**D and FIG. **59**F to the other. In this manner, the portable information terminal **9202** can be folded in three.
[0877] The display portion **9001** of the portable information terminal **9202** is supported by three housings **9000** joined together with the hinges **9055**.
[0878] The portable information terminals **9201** and **9202** are highly portable when folded. When

the portable information terminals **9201** and **9202** are opened, a seamless large display region is highly browsable.

[0879] The use of the semiconductor device or the memory device of one embodiment of the present invention for one or more selected from an electronic component, a large computer, space equipment, a data center, and an electronic apparatus can reduce power consumption. While the demand for energy is expected to increase with higher performance or higher integration of semiconductor devices, the emission amount of greenhouse effect gases typified by carbon dioxide (CO.sub.2) can be reduced with use of the semiconductor device or the memory device of one embodiment of the present invention. Furthermore, the semiconductor device or the memory device of one embodiment of the present invention has low power consumption and thus is effective as a global warming countermeasure.

[0880] This embodiment can be combined with any of the other embodiments as appropriate. In this specification, in the case where a plurality of structure examples are shown in one embodiment, the structure examples can be combined as appropriate.

[0881] This application is based on Japanese Patent Application Serial No. 2024-022114 filed with Japan Patent Office on Feb. 16, 2024, the entire contents of which are hereby incorporated by reference.

Claims

1. A semiconductor device comprising: a first insulating layer; a second insulating layer; a first capacitor; a second capacitor; a first transistor; and a second transistor, wherein the first insulating layer comprises a first opening portion, wherein the second insulating layer comprises a second opening portion, wherein the second insulating layer is positioned over the first insulating layer, wherein the second opening portion comprises a region overlapping with the first opening portion, wherein the first capacitor comprises a first electrode positioned along a sidewall of the first opening portion, a dielectric over the first electrode, and a second electrode comprising a region facing the first electrode with the dielectric interposed therebetween in the first opening portion, wherein the second capacitor comprises the first electrode, the dielectric, and a third electrode comprising a region facing the first electrode with the dielectric interposed therebetween in the first opening portion, wherein the first transistor comprises a first oxide semiconductor layer, wherein the second transistor comprises a second oxide semiconductor layer, and wherein the first oxide semiconductor layer and the second oxide semiconductor layer each comprise a region positioned along a sidewall of the second opening portion.

2. A semiconductor device comprising: a first capacitor; a second capacitor; a first transistor; a second transistor; a first insulating layer; a second insulating layer; a third insulating layer; and a fourth insulating layer, wherein the first capacitor comprises a first conductive layer, a second conductive layer, and a fifth insulating layer, wherein the second capacitor comprises the first conductive layer, a third conductive layer, and the fifth insulating layer, wherein the first transistor comprises a first oxide semiconductor layer, a fourth conductive layer, a fifth conductive layer, a sixth conductive layer, and a sixth insulating layer, wherein the second transistor comprises a second oxide semiconductor layer, the fifth conductive layer, a seventh conductive layer, an eighth conductive layer, and the sixth insulating layer, wherein the first insulating layer comprises a first opening portion, wherein the first conductive layer comprises a region positioned in the first opening portion, wherein the fifth insulating layer is positioned over the first conductive layer, wherein the second conductive layer and the third conductive layer each comprise a region facing the first conductive layer with the fifth insulating layer interposed therebetween in the first opening portion, wherein the second insulating layer is positioned over the second conductive layer and the third conductive layer, wherein the fourth conductive layer and the seventh conductive layer are positioned over the second insulating layer, wherein the fourth conductive layer is electrically

connected to the second conductive layer, wherein the seventh conductive layer is electrically connected to the third conductive layer, wherein the third insulating layer is positioned over the fourth conductive layer and the seventh conductive layer, wherein the fifth conductive layer is positioned over the third insulating layer, wherein the fourth insulating layer is positioned over the third insulating layer and the fifth conductive layer, wherein the sixth conductive layer and the eighth conductive layer are positioned to be apart from each other over the fourth insulating layer, wherein the fourth insulating layer, the fifth conductive layer, and the third insulating layer comprise a second opening portion, wherein the second opening portion comprises a portion overlapping with the fourth conductive layer, a portion overlapping with the seventh conductive layer, and a portion overlapping with the second insulating layer positioned between the fourth conductive layer and the seventh conductive layer, wherein the sixth insulating layer covers a sidewall of the second opening portion, wherein the first oxide semiconductor layer comprises a region facing the fifth conductive layer with the sixth insulating layer interposed therebetween in the second opening portion, a region in contact with the fourth conductive layer in the second opening portion, and a region in contact with the sixth conductive layer outside the second opening portion, and wherein the second oxide semiconductor layer comprises a region facing the fifth conductive layer with the sixth insulating layer interposed therebetween in the second opening portion, a region in contact with the seventh conductive layer in the second opening portion, and a region in contact with the eighth conductive layer outside the second opening portion.

3. The semiconductor device according to claim 2, wherein the first conductive layer comprises a region along a sidewall of the first opening portion.

4. The semiconductor device according to claim 2, comprising: a ninth conductive layer; and a tenth conductive layer, wherein the second insulating layer comprises a third opening portion reaching the second conductive layer and a fourth opening portion reaching the third conductive layer, wherein the ninth conductive layer is positioned in the third opening portion, wherein the tenth conductive layer is positioned in the fourth opening portion, wherein the fourth conductive layer comprises a region in contact with a top surface of the ninth conductive layer, and wherein the seventh conductive layer comprises a region in contact with a top surface of the tenth conductive layer.

5. The semiconductor device according to claim 2, comprising: a seventh insulating layer, wherein the second insulating layer comprises a first depressed portion at a position overlapping with the first opening portion, and wherein the seventh insulating layer is positioned to fill at least a part of the first depressed portion.

6. The semiconductor device according to claim 2, wherein the sixth insulating layer in the second opening portion is circular in a plan view, and wherein the first oxide semiconductor layer and the second oxide semiconductor layer in the second opening portion are each arc-shaped in the plan view.

7. The semiconductor device according to claim 2, wherein the fourth conductive layer comprises a second depressed portion at a position overlapping with the second opening portion, wherein the sixth insulating layer is in contact with a sidewall of the second depressed portion, and wherein the first oxide semiconductor layer is in contact with at least a part of a bottom portion of the second depressed portion.

8. The semiconductor device according to claim 7, wherein the fourth conductive layer comprises a first layer and a second layer over the first layer, and wherein the second layer comprises the second depressed portion.

9. The semiconductor device according to claim 2, wherein the sixth insulating layer is in contact with a part of a side surface of the sixth conductive layer on the second opening portion side, and wherein the first oxide semiconductor layer is in contact with another part of the side surface of the sixth conductive layer on the second opening portion side.

10. The semiconductor device according to claim 9, wherein the sixth insulating layer is in contact

with a part of a side surface of the fourth conductive layer on the second opening portion side, and wherein the first oxide semiconductor layer is in contact with another part of the side surface of the fourth conductive layer on the second opening portion side.

11. The semiconductor device according to claim 2, wherein an end portion of the first oxide semiconductor layer outside the second opening portion is closer to the second opening portion than an end portion of the sixth conductive layer outside the second opening portion is.

12. The semiconductor device according to claim 2, comprising: an eighth insulating layer; and an eleventh conductive layer, wherein the eighth insulating layer is positioned over the first oxide semiconductor layer and the second oxide semiconductor layer, and wherein the eleventh conductive layer comprises, in the second opening portion, a region facing the fifth conductive layer with the eighth insulating layer, the first oxide semiconductor layer, and the sixth insulating layer interposed therebetween and a region facing the fifth conductive layer with the eighth insulating layer, the second oxide semiconductor layer, and the sixth insulating layer interposed therebetween.

13. The semiconductor device according to claim 12, wherein a height of a bottom surface of the eleventh conductive layer in a portion positioned between the fourth conductive layer and the seventh conductive layer is lower than a height of a top surface of the fourth conductive layer in a portion not overlapping with the second opening portion.

14. The semiconductor device according to claim 12, comprising: a ninth insulating layer; and a twelfth conductive layer, wherein the ninth insulating layer is positioned over the eighth insulating layer and comprises a fifth opening portion at a position overlapping with the second opening portion, and wherein the twelfth conductive layer is positioned over the ninth insulating layer and comprises a region in contact with the eleventh conductive layer.