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DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF

Abstract

According to one embodiment, a display device includes a first lower electrode, a partition which has a conductive lower portion and an upper portion, a first organic layer provided on the first lower electrode, and a first upper electrode provided on the first organic layer. The lower portion has a bottom layer and a stem layer. The bottom layer and the upper portion protrude from a side surface of the stem layer. The first organic layer has a first end portion and a second end portion located on a side opposite to the first end portion. A first length which protrudes from the stem layer in the bottom layer overlapping the first end portion is different from a second length which protrudes from the stem layer in the bottom layer overlapping the second end portion.

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2024-021256, filed Feb. 15, 2024, the entire contents of which are incorporated herein by reference.

FIELD

[0002] Embodiments described herein relate generally to a display device and a manufacturing method thereof.

BACKGROUND

[0003] Recently, display devices to which an organic light emitting diode (OLED) is applied as a display element have been put into practical use. This display element comprises a pixel circuit including a thin-film transistor, a lower electrode connected to the pixel circuit, an organic layer which covers the lower electrode, and an upper electrode which covers the organic layer. The organic layer includes functional layers such as a hole transport layer and an electron transport layer in addition to a light emitting layer.

[0004] In the process of manufacturing such a display element, a technique which prevents the reduction in reliability has been required.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. **1** is a diagram showing a configuration example of a display device DSP.

[0006] FIG. **2** is a diagram showing an example of the layout of subpixels SP**1**, SP**2** and SP**3**.

[0007] FIG. **3** is the schematic cross-sectional view of the display device DSP along the A-B line of FIG. **2**.

[0008] FIG. **4** is the schematic cross-sectional view of the major portion of the display device DSP along the C-D line of FIG. **2**.

[0009] FIG. **5** is the schematic cross-sectional view of the major portion of the display device DSP along the E-F line of FIG. **2**.

[0010] FIG. **6** is a diagram for explaining an evaporation device EV.

[0011] FIG. **7** is a diagram for explaining an example of an evaporation direction D when an upper electrode is formed in each subpixel.

[0012] FIG. **8** is a diagram for explaining another example of the evaporation direction D when an upper electrode is formed in each subpixel.

[0013] FIG. **9** is a diagram for explaining the manufacturing method of the display device DSP.

[0014] FIG. **10** is a diagram for explaining the manufacturing method of the display device DSP.

[0015] FIG. **11** is a diagram for explaining the manufacturing method of the display device DSP.

[0016] FIG. **12** is a diagram for explaining the manufacturing method of the display device DSP.

[0017] FIG. **13** is a diagram for explaining the manufacturing method of the display device DSP.

[0018] FIG. **14** is a diagram for explaining the manufacturing method of the display device DSP.

[0019] FIG. **15** is a cross-sectional view of subpixels SP**2** and SP**3** in which a stacked film FL**1** is formed.

[0020] FIG. **16** is a cross-sectional view of subpixels SP**2** and SP**3** from which the stacked film FL**1** is removed.

[0021] FIG. **17** is a diagram showing another example of the layout of subpixels SP**1**, SP**2** and SP**3**.

[0022] FIG. **18** is a diagram showing another example of the layout of subpixels SP**1**, SP**2** and SP**3**.

DETAILED DESCRIPTION

[0023] Embodiments described herein aim to provide a display device and a manufacturing method thereof such that the reduction in reliability can be prevented.
[0024] In general, according to one embodiment, a display device comprises a substrate, a first lower electrode provided above the substrate, an inorganic insulating layer which covers a peripheral portion of the first lower electrode, a partition which has a conductive lower portion provided on the inorganic insulating layer, and an upper portion provided on the lower portion, a first organic layer which is provided on the first lower electrode and includes a first light emitting layer, and a first upper electrode which is provided on the first organic layer and is in contact with the lower portion of the partition. The partition surrounds the first organic layer and the first upper electrode. The lower portion has a bottom layer provided on the inorganic insulating layer and a stem layer provided between the bottom layer and the upper portion. The bottom layer and the upper portion protrude from a side surface of the stem layer. The first organic layer has a first end portion overlapping the bottom layer, and a second end portion overlapping the bottom layer and located on a side opposite to the first end portion. A first length which protrudes from the stem layer in the bottom layer overlapping the first end portion is different from a second length which protrudes from the stem layer in the bottom layer overlapping the second end portion.
[0025] According to another embodiment, a display device comprises a substrate, first and second lower electrodes provided above the substrate, an inorganic insulating layer which covers a peripheral portion of each of the first and second lower electrodes, a partition which has a conductive lower portion provided on the inorganic insulating layer, and an upper portion provided on the lower portion, a first organic layer which is provided on the first lower electrode and includes a first light emitting layer, a first upper electrode which is provided on the first organic layer and is in contact with the lower portion of the partition, a second organic layer which is provided on the second lower electrode and includes a second light emitting layer formed of a material different from the first light emitting layer, and a second upper electrode which is provided on the second organic layer and is in contact with the lower portion of the partition. The partition surrounds the first organic layer, the first upper electrode, the second organic layer and the second upper electrode. The lower portion has a bottom layer provided on the inorganic insulating layer, and a stem layer provided between the bottom layer and the upper portion. The bottom layer and the upper portion protrude from a side surface of the stem layer. The first organic layer has a first end portion overlapping the bottom layer, and a second end portion overlapping the bottom layer and located on a side opposite to the first end portion. The second organic layer has a third end portion located on a side opposite to the second end portion across the intervening partition and overlapping the bottom layer, and a fourth end portion overlapping the bottom layer and located on a side opposite to the third end portion. A second thickness of the first upper electrode immediately above the second end portion is greater than a first thickness of the first upper electrode immediately above the first end portion. A fourth thickness of the second upper electrode immediately above the fourth end portion is greater than a third thickness of the second upper electrode immediately above the third end portion.
[0026] According to yet another embodiment, a manufacturing method of a display device comprises preparing a processing substrate in which a first lower electrode, a second lower electrode, a third lower electrode, an inorganic insulating layer and a partition are formed above a substrate, the inorganic insulating layer covering a peripheral portion of each of the first, second and third lower electrodes, the partition including a lower portion located on the inorganic insulating layer and an upper portion which is located on the lower portion and protrudes from a side surface of the lower portion, forming a first stacked film including a first organic layer and a first upper electrode on the first lower electrode, the first organic layer including a first light emitting layer, the first upper electrode being located on the first organic layer, forming a second stacked film including a second organic layer and a second upper electrode on the second lower electrode, the second organic layer including a second light emitting layer different from the first

light emitting layer, the second upper electrode being located on the second organic layer, and forming a third stacked film including a third organic layer and a third upper electrode on the third lower electrode, the third organic layer including a third light emitting layer different from the first light emitting layer and the second light emitting layer, the third upper electrode being located on the third organic layer. Each of the first, second and third upper electrodes is formed by emitting a conductive material from an evaporation source which inclines with respect to a normal of the processing substrate and depositing the conductive material using the partition as a mask while changing relative position of the evaporation source and the processing substrate. Evaporation directions for forming the first upper electrode, the second upper electrode and the third upper electrode are same as each other.

[0027] The embodiments can provide a display device and a manufacturing method thereof such that the reduction in reliability can be prevented.

[0028] Embodiments will be described with reference to the accompanying drawings.

[0029] The disclosure is merely an example, and proper changes in keeping with the spirit of the invention, which are easily conceivable by a person of ordinary skill in the art, come within the scope of the invention as a matter of course. In addition, in some cases, in order to make the description clearer, the widths, thicknesses, shapes, etc., of the respective parts are illustrated schematically in the drawings, rather than as an accurate representation of what is implemented. However, such schematic illustration is merely exemplary, and in no way restricts the interpretation of the invention. In addition, in the specification and drawings, structural elements which function in the same or a similar manner to those described in connection with preceding drawings are denoted by like reference numbers, detailed description thereof being omitted unless necessary.

[0030] In the drawings, in order to facilitate understanding, an X-axis, a Y-axis and a Z-axis orthogonal to each other are shown depending on the need. A direction parallel to the X-axis is referred to as a first direction X. A direction parallel to the Y-axis is referred to as a second direction Y. A direction parallel to the Z-axis is referred to as a third direction Z. When various elements are viewed parallel to the third direction Z, the appearance is defined as a plan view.

[0031] The display device of the present embodiment is an organic electroluminescent display device comprising an organic light emitting diode (OLED) as a display element, and could be mounted on a television, a personal computer, a vehicle-mounted device, a tablet, a smartphone, a mobile phone, etc.

[0032] FIG. **1** is a diagram showing a configuration example of a display device DSP.

[0033] The display device DSP comprises a display panel PNL having a display area DA which displays an image and a surrounding area SA located on an external side relative to the display area DA on an insulating substrate **10**. The substrate **10** may be glass or a resinous film having flexibility.

[0034] In the embodiment, the substrate **10** is rectangular in plan view. It should be noted that the shape of the substrate **10** in plan view is not limited to a rectangle and may be another shape such as a square, a circle or an oval.

[0035] The display area DA comprises a plurality of pixels PX arrayed in matrix in a first direction X and a second direction Y. Each pixel PX includes a plurality of subpixels SP. For example, each pixel PX includes subpixel SP**1** which exhibits a first color, subpixel SP**2** which exhibits a second color and subpixel SP**3** which exhibits a third color. The first color, the second color and the third color are different colors. Each pixel PX may include a subpixel SP which exhibits another color such as white in addition to subpixels SP**1**, SP**2** and SP**3** or instead of one of subpixels SP**1**, SP**2** and SP**3**.

[0036] Each subpixel SP comprises a pixel circuit **1** and a display element DE driven by the pixel circuit **1**. The pixel circuit **1** comprises a pixel switch **2**, a drive transistor **3** and a capacitor **4**. Each of the pixel switch **2** and the drive transistor **3** is, for example, a switching element consisting of a thin-film transistor.

[0037] The gate electrode of the pixel switch **2** is connected to a scanning line GL. One of the source electrode and the drain electrode of the pixel switch **2** is connected to a signal line SL. The other one is connected to the gate electrode of the drive transistor **3** and the capacitor **4**. In the drive transistor **3**, one of the source electrode and the drain electrode is connected to a power line PL and the capacitor **4**, and the other one is connected to the anode of the display element DE.
[0038] It should be noted that the configuration of the pixel circuit **1** is not limited to the example shown in the figure. For example, the pixel circuit **1** may comprise more thin-film transistors and capacitors.
[0039] The display element DE is an organic light emitting diode (OLED) as a light emitting element, and may be called an organic EL element.
[0040] The surrounding area SA has a plurality of terminals TE which are arranged along one direction. In the example shown in the figure, the terminals TE are arranged in the first direction X. Each of the terminals TE extends in the second direction Y. However, the configuration is not limited to this example. For example, these terminals TE are electrically connected to a flexible printed circuit or an IC chip.
[0041] FIG. **2** is a diagram showing an example of the layout of subpixels SP**1**, SP**2** and SP**3**.
[0042] In the example shown in the figure, subpixels SP**2** and SP**3** are arranged in the second direction Y. Subpixels SP**1** and SP**2** are arranged in the first direction X, and subpixels SP**1** and SP**3** are arranged in the first direction X.
[0043] When subpixels SP**1**, SP**2** and SP**3** are provided in line with this layout, a column in which subpixels SP**2** and SP**3** are alternately provided in the second direction Y and a column in which a plurality of subpixels SP**1** are provided in the second direction Y are formed in the display area DA. These columns are alternately arranged in the first direction X.
[0044] It should be noted that the layout of subpixels SP**1**, SP**2** and SP**3** is not limited to the example of FIG. **2**. As another example, subpixels SP**1**, SP**2** and SP**3** in each pixel PX may be arranged in order in the first direction X.
[0045] An inorganic insulating layer **5** and a partition **6** are provided in the display area DA. The inorganic insulating layer **5** has apertures AP**1**, AP**2** and AP**3** in subpixels SP**1**, SP**2** and SP**3**, respectively. The inorganic insulating layer **5** having these apertures AP**1**, AP**2** and AP**3** may be called a rib.
[0046] The partition **6** overlaps the inorganic insulating layer **5** in plan view. The partition **6** is formed into a grating shape surrounding the apertures AP**1**, AP**2** and AP**3**. In other words, the partition **6** has apertures in subpixels SP**1**, SP**2** and SP**3** in a manner similar to that of the inorganic insulating layer **5**. The partition **6** is conductive and is electrically connected to, of the terminals TE shown in FIG. **1**, the terminal TE having a common potential.
[0047] Subpixels SP**1**, SP**2** and SP**3** comprise display elements DE**1**, DE**2** and DE**3**, respectively, as the display elements DE.
[0048] The display element DE**1** of subpixel SP**1** comprises a lower electrode LE**1**, an upper electrode UE**1** and an organic layer OR**1** overlapping the aperture AP**1**. The peripheral portion of the lower electrode LE**1** is covered with the inorganic insulating layer **5**. The lower electrode LE**1**, the organic layer OR**1** and the upper electrode UE**1** are surrounded by the partition **6** in plan view. The peripheral portion of each of the organic layer OR**1** and the upper electrode UE**1** overlaps the inorganic insulating layer **5** in plan view. The organic layer OR**1** includes a light emitting layer which emits light in, for example, a blue wavelength range.
[0049] The display element DE**2** of subpixel SP**2** comprises a lower electrode LE**2**, an upper electrode UE**2** and an organic layer OR**2** overlapping the aperture AP**2**. The peripheral portion of the lower electrode LE**2** is covered with the inorganic insulating layer **5**. The lower electrode LE**2**, the organic layer OR**2** and the upper electrode UE**2** are surrounded by the partition **6** in plan view. The peripheral portion of each of the organic layer OR**2** and the upper electrode UE**2** overlaps the inorganic insulating layer **5** in plan view. The organic layer OR**2** includes a light emitting layer

which emits light in, for example, a green wavelength range.
[0050] The display element DE**3** of subpixel SP**3** comprises a lower electrode LE**3**, an upper electrode UE**3** and an organic layer OR**3** overlapping the aperture AP**3**. The peripheral portion of the lower electrode LE**3** is covered with the inorganic insulating layer **5**. The lower electrode LE**3**, the organic layer OR**3** and the upper electrode UE**3** are surrounded by the partition **6** in plan view. The peripheral portion of each of the organic layer OR**3** and the upper electrode UE**3** overlaps the inorganic insulating layer **5** in plan view. The organic layer OR**3** includes a light emitting layer which emits light in, for example, a red wavelength range.
[0051] In the example shown in the figure, the outer shapes of the lower electrodes LE**1**, LE**2** and LE**3** are shown by dotted lines, and the outer shapes of the organic layers OR**1**, OR**2** and OR**3** and the upper electrodes UE**1**, UE**2** and UE**3** are shown by dash-dot lines. It should be noted that the outer shape of each of the lower electrodes, organic layers and upper electrodes shown in the figure does not necessarily reflect the accurate shape.
[0052] The lower electrodes LE**1**, LE**2** and LE**3** correspond to, for example, the anodes of the display elements. The upper electrodes UE**1**, UE**2** and UE**3** correspond to the cathodes of the display elements or a common electrode and are in contact with the partition **6**.
[0053] The lower electrode LE**1** is electrically connected to the pixel circuit **1** (see FIG. **1**) of subpixel SP**1** in a contact hole CH**1**. The lower electrode LE**2** is electrically connected to the pixel circuit **1** of subpixel SP**2** in a contact hole CH**2**. The lower electrode LE**3** is electrically connected to the pixel circuit **1** of subpixel SP**3** in a contact hole CH**3**.
[0054] In the example shown in the figure, the area of the aperture AP**1**, the area of the aperture AP**2** and the area of the aperture AP**3** are different from each other. The area of the aperture AP**1** is greater than that of the aperture AP**2**, and the area of the aperture AP**2** is greater than that of the aperture AP**3**. In other words, the area of the lower electrode LE**1** exposed from the aperture AP**1** is greater than that of the lower electrode LE**2** exposed from the aperture AP**2**. The area of the lower electrode LE**2** exposed from the aperture AP**2** is greater than that of the lower electrode LE**3** exposed from the aperture AP**3**.
[0055] FIG. **3** is the schematic cross-sectional view of the display device DSP along the A-B line of FIG. **2**. A circuit layer **11** is provided on the substrate **10**. The circuit layer **11** includes various circuits such as the pixel circuit **1** shown in FIG. **1** and various lines such as the scanning line GL, the signal line SL and the power line PL. The circuit layer **11** is covered with an insulating layer **12**. The insulating layer **12** is an organic insulating layer which planarizes the irregularities formed by the circuit layer **11**.
[0056] The lower electrodes LE**1**, LE**2** and LE**3** are provided on the insulating layer **12** and are spaced apart from each other. The inorganic insulating layer **5** is provided on the insulating layer **12** and the lower electrodes LE**1**, LE**2** and LE**3**. The aperture AP**1** of the inorganic insulating layer **5** overlaps the lower electrode LE**1**. The aperture AP**2** overlaps the lower electrode LE**2**. The aperture AP**3** overlaps the lower electrode LE**3**. The peripheral portions of the lower electrodes LE**1**, LE**2** and LE**3** are covered with the inorganic insulating layer **5**. The lower electrodes LE**1**, LE**2** and LE**3** are connected to the pixel circuits **1** of subpixels SP**1**, SP**2** and SP**3**, respectively, through the contact holes provided in the insulating layer **12**. It should be noted that the contact holes of the insulating layer **12** are omitted in FIG. **3**.
[0057] The partition **6** has a conductive lower portion **61** provided on the inorganic insulating layer **5**, and an upper portion **62** provided on the lower portion **61**.
[0058] In the example shown in the figure, the lower portion **61** has a bottom layer **63** provided on the inorganic insulating layer **5**, and a stem layer **64** provided between the bottom layer **63** and the upper portion **62**. The bottom layer **63** is thinner than the stem layer **64**. The bottom layer **63** has a width greater than that of the stem layer **64**. The both end portions of the bottom layer **63** protrude from the side surfaces of the stem layer **64**.
[0059] The upper portion **62** has a first thin film **65** provided on the stem layer **64** and a second thin

film **66** provided on the first thin film **65**. The upper portion **62** has a width greater than that of the stem layer **64**. The both end portions of the upper portion **62** protrude from the side surfaces of the stem layer **64**.

[0060] In the example shown in the figure, the upper portion **62** has a width greater than that of the bottom layer **63**. It should be noted that the bottom layer **63** may have a width greater than that of the upper portion **62**.

[0061] The organic layer OR**1** is in contact with the lower electrode LE**1** through the aperture AP**1** and covers the lower electrode LE**1** exposed from the aperture AP**1**. The peripheral portion of the organic layer OR**1** is located on the inorganic insulating layer **5**. The upper electrode UE**1** covers the organic layer OR**1** and is in contact with the lower portion **61**.

[0062] The organic layer OR**2** is in contact with the lower electrode LE**2** through the aperture AP**2** and covers the lower electrode LE**2** exposed from the aperture AP**2**. The peripheral portion of the organic layer OR**2** is located on the inorganic insulating layer **5**. The upper electrode UE**2** covers the organic layer OR**2** and is in contact with the lower portion **61**.

[0063] The organic layer OR**3** is in contact with the lower electrode LE**3** through the aperture AP**3** and covers the lower electrode LE**3** exposed from the aperture AP**3**. The peripheral portion of the organic layer OR**3** is located on the inorganic insulating layer **5**. The upper electrode UE**3** covers the organic layer OR**3** and is in contact with the lower portion **61**.

[0064] In the example shown in the figure, subpixel SP**1** has a cap layer CP**1** and a sealing layer SE**1**. Subpixel SP**2** has a cap layer CP**2** and a sealing layer SE**2**. Subpixel SP**3** has a cap layer CP**3** and a sealing layer SE**3**. The cap layers CP**1**, CP**2** and CP**3** function as optical adjustment layers which improve the extraction efficiency of the light emitted from the organic layers OR**1**, OR**2** and OR**3**, respectively. It should be noted that the cap layers CP**1**, CP**2** and CP**3** may be omitted.

[0065] The cap layer CP**1** is provided on the upper electrode UE**1**.

[0066] The cap layer CP**2** is provided on the upper electrode UE**2**.

[0067] The cap layer CP**3** is provided on the upper electrode UE**3**.

[0068] The sealing layer SE**1** is provided on the cap layer CP**1**, is in contact with the partition **6** and continuously covers the members of subpixel SP**1**.

[0069] The sealing layer SE**2** is provided on the cap layer CP**2**, is in contact with the partition **6** and continuously covers the members of subpixel SP**2**.

[0070] The sealing layer SE**3** is provided on the cap layer CP**3**, is in contact with the partition **6** and continuously covers the members of subpixel SP**3**.

[0071] In the following explanation, a multilayer body including the organic layer OR**1**, the upper electrode UE**1** and the cap layer CP**1** is called a stacked film FL**1**. A multilayer body including the organic layer OR**2**, the upper electrode UE**2** and the cap layer CP**2** is called a stacked film FL**2**. A multilayer body including the organic layer OR**3**, the upper electrode UE**3** and the cap layer CP**3** is called a stacked film FL**3**.

[0072] In the example shown in the figure, part of the stacked film FL**1** is located on the partition **6** around subpixel SP**1** and spaced apart from the stacked film FL**1** located in the aperture AP**1** (in other words, the portion which constitutes the display element DE**1**).

[0073] Similarly, part of the stacked film FL**2** is located on the partition **6** around subpixel SP**2** and spaced apart from the stacked film FL**2** located in the aperture AP**2** (in other words, the portion which constitutes the display element DE**2**).

[0074] Similarly, part of the stacked film FL**3** is located on the partition **6** around subpixel SP**3** and spaced apart from the stacked film FL**3** located in the aperture AP**3** (in other words, the portion which constitutes the display element DE**3**).

[0075] It should be noted that the stacked films FL**1**, FL**2** and FL**3** located on the partition **6** may be omitted in some cases. In these cases, a cavity is formed between the sealing layers SE**1**, SE**2** and SE**3** and the partition **6**.

[0076] Each of the end portions of the sealing layers SE**1**, SE**2** and SE**3** is located above the

partition **6**. In the example shown in the figure, the stacked film FL**1** and sealing layer SE**1** located on the partition **6** between subpixels SP**1** and SP**2** are spaced apart from the stacked film FL**2** and sealing layer SE**2** located on this partition **6**. The stacked film FL**1** and sealing layer SE**1** located on the partition **6** between subpixels SP**1** and SP**3** are spaced apart from the stacked film FL**3** and sealing layer SE**3** located on this partition **6**.

[0077] The partition **6** and the sealing layers SE**1**, SE**2** and SE**3** are covered with a resin layer **13**. When cavities are formed between the sealing layers SE**1**, SE**2** and SE**3** and the partition **6**, these cavities are filled with the resin layer **13**. The resin layer **13** is covered with a sealing layer **14**. The sealing layer **14** is covered with a resin layer **15**.

[0078] Each of the inorganic insulating layer **5**, the sealing layers SE**1**, SE**2** and SE**3** and the sealing layer **14** is formed of, for example, an inorganic insulating material such as silicon nitride (SiNx), silicon oxide (SiOx), silicon oxynitride (SiON) or aluminum oxide (Al.sub.2O.sub.3).

[0079] The lower portion **61** of the partition **6** is formed of a conductive material and is electrically connected to the upper electrodes UE**1**, UE**2** and UE**3**. The bottom layer **63** is formed of, for example, a titanium-based material such as titanium or a titanium compound. The stem layer **64** is formed of a material which is different from the bottom layer **63** and the upper portion **62**, and is formed of, for example, an aluminum-based material such as aluminum or an aluminum compound.

[0080] The upper portion **62** of the partition **6** is formed of, for example, a conductive material. However, the upper portion **62** may be formed of an insulating material. The upper portion **62** is formed of a material which is different from that of the lower portion **61**. The first thin film **65** is formed of, for example, a titanium-based material such as titanium or a titanium compound. The second thin film **66** is formed of, for example, an oxide conductive material such as indium tin oxide (ITO).

[0081] Each of the lower electrodes LE**1**, LE**2** and LE**3** is, for example, a multilayer body including a transparent layer formed of an oxide conductive material such as indium tin oxide (ITO) and a reflective layer formed of a metal material such as silver. For example, each of the lower electrodes LE**1**, LE**2** and LE**3** is a multilayer body including a reflective layer between a pair of transparent layers.

[0082] The organic layer OR**1** includes a light emitting layer EM**1**. The organic layer OR**2** includes a light emitting layer EM**2**. The organic layer OR**3** includes a light emitting layer EM**3**. The light emitting layer EM**1**, the light emitting layer EM**2** and the light emitting layer EM**3** are formed of materials which are different from each other. For example, the light emitting layer EM**1** is formed of a material which emits light in a blue wavelength range. The light emitting layer EM**2** is formed of a material which emits light in a green wavelength range. The light emitting layer EM**3** is formed of a material which emits light in a red wavelength range.

[0083] Each of the organic layers OR**1**, OR**2** and OR**3** includes a plurality of functional layers such as a hole injection layer, a hole transport layer, an electron blocking layer, a hole blocking layer, an electron transport layer and an electron injection layer.

[0084] Each of the upper electrodes UE**1**, UE**2** and UE**3** is formed of, for example, a metal material such as an alloy of magnesium and silver (MgAg).

[0085] Each of the cap layers CP**1**, CP**2** and CP**3** is a multilayer body consisting of a plurality of thin films. All of the thin films are transparent and have refractive indices different from each other.

[0086] The circuit layer **11**, the insulating layer **12** and the inorganic insulating layer **5** shown in the figure are provided over the display area DA and the surrounding area SA.

[0087] FIG. **4** is the schematic cross-sectional view of the major portion of the display device DSP along the C-D line of FIG. **2**.

[0088] FIG. **4** shows the section of a plurality of subpixels SP**1** which are arranged in the second direction Y. In FIG. **4**, the illustrations of the substrate **10**, the circuit layer **11**, the resin layer **13**, the sealing layer **14** and the resin layer **15** shown in FIG. **3** are omitted.

[0089] This specification focuses attention on the subpixel SP**1** located in the center of the figure.

The organic layer OR**1** has an end portion P**1** in the second direction Y, and an end portion P**2** on a side opposite to the end portion P**1**. In FIG. **4**, each of an area including the end portion P**1** and an area including the end portion P**2** is enlarged. Each of the end portion P**1** and the end portion P**2** is located on the bottom layer **63** and is spaced apart from the stem layer **64**. The end portion P**1** and the end portion P**2** are located immediately under the upper portions **62**.

[0090] The lower electrode LE**1** has an electrode edge LE**1**A on the side on which the end portion P**1** is located, and an electrode edge LE**1**B on the side on which the end portion P**2** is located. The partition **6** overlaps the electrode edge LE**1**A and the electrode edge LE**1**B. In the example shown in the figure, each of the electrode edge LE**1**A and the electrode edge LE**1**B is located immediately under the stem layer **64**.

[0091] The bottom layer **63** overlapping the end portion P**1** has length L**1** which protrudes from the stem layer **64**. The bottom layer **63** overlapping the end portion P**2** has length L**2** which protrudes from the stem layer **64**. Length L**1** is different from length L**2**. In the example shown in the figure, length L**2** is greater than length L**1** (L**1**<L**2**).

[0092] The upper electrode UE**1** overlaps the organic layer OR**1**, goes beyond the end portion P**1** and the end portion P**2** and is directly in contact with the upper surfaces of the bottom layer **63**. In this specification, the upper surface of the bottom layer **63** is assumed to include, of the bottom layer **63**, the surface which is directly in contact with the stem layer **64**, and the surface which protrudes from the stem layer **64** and faces the upper portion **62**. In the example shown in the figure, the upper electrode UE**1** is directly in contact with the side surface of the stem layer **64** of the partition **6** facing the end portion P**2**. In this specification, the side surface of the stem layer **64** is assumed to be, of the stem layer **64**, the surface which extends between the bottom layer **63** and the upper portion **62**. The upper electrode UE**1** is spaced apart from the stem layer **64** of the partition **6** facing the end portion P**1**. However, the upper electrode UE**1** may be in contact with this stem layer **64**.

[0093] When the upper electrode UE**1** is spaced apart from the stem layer **64** of the partition **6** facing the end portion P**1**, the cap layer CP**1** is directly in contact with the upper surface of the bottom layer **63**. When the upper electrode UE**1** is spaced apart from the stem layer **64** of the partition **6** facing the end portion P**1**, the upper electrode UE**1** may be directly in contact with the upper surface of the bottom layer **63** or may not be in contact with the bottom layer **63**.

[0094] As shown in the enlarged view of each of the area including the end portion P**1** and the area including the end portion P**2**, in the upper electrode UE**1**, thickness T**2** immediately above the end portion P**2** is greater than thickness T**1** immediately above the end portion P**1** (T**1**<T**2**). The area of contact between the lower portion **61** facing the end portion P**2** and the upper electrode UE**1** is greater than that between the lower portion **61** facing the end portion P**1** and the upper electrode UE**1**.

[0095] The multilayer body consisting of the organic layer OR**1**, the upper electrode UE**1** and the cap layer CP**1** is provided over the entire surface of the upper portion **62** of the partition **6**. The sealing layer SE**1** covers the cap layer CP**1** and the partition **6**.

[0096] In the example shown in FIG. **4**, for example, the lower electrode LE**1** corresponds to the first lower electrode, and the electrode edge LE**1**A corresponds to the first electrode edge, and the electrode edge LE**1**B corresponds to the second electrode edge. The organic layer OR**1** corresponds to the first organic layer. The end portion P**1** corresponds to the first end portion. The end portion P**2** corresponds to the second end portion. Length L**1** corresponds to the first length. Length L**2** corresponds to the second length. The upper electrode UE**1** corresponds to the first upper electrode. Thickness T**1** corresponds to the first thickness. Thickness T**2** corresponds to the second thickness. The cap layer CP**1** corresponds to the first cap layer. The sealing layer SE**1** corresponds to the first sealing layer.

[0097] It should be noted that, in a case where subpixel SP**1** is firstly formed when subpixels SP**1**, SP**2** and SP**3** are formed, length L**1** is substantially equal to length L**2**.

[0098] FIG. **5** is the schematic cross-sectional view of the major portion of the display device DSP along the E-F line of FIG. **2**.
[0099] FIG. **5** shows the section of subpixels SP**2** and SP**3** which are alternately arranged in the second direction Y. In FIG. **5**, the illustrations of the substrate **10**, the circuit layer **11**, the resin layer **13**, the sealing layer **14** and the resin layer **15** shown in FIG. **3** are omitted.
[0100] First, this specification focuses attention on the subpixel SP**3** located on the left side of the figure. The organic layer OR**3** has an end portion P**11** in the second direction Y, and an end portion P**12** on a side opposite to the end portion P**11**. In FIG. **5**, each of an area including the end portion P**11** and an area including the end portion P**12** is enlarged. Each of the end portion P**11** and the end portion P**12** is located on the bottom layer **63** and is spaced apart from the stem layer **64**.
[0101] The bottom layer **63** overlapping the end portion P**11** has length L**11** which protrudes from the stem layer **64**. The bottom layer **63** overlapping the end portion P**12** has length L**12** which protrudes from the stem layer **64**. Length L**11** is different from length L**12**. In the example shown in the figure, length L**12** is greater than length L**11** (L**11**<L**12**).
[0102] The upper electrode UE**3** overlaps the organic layer OR**3**, goes beyond the end portion P**11** and the end portion P**12** and is directly in contact with the upper surfaces of the bottom layer **63**. In the example shown in the figure, the upper electrode UE**3** is directly in contact with the side surface of the stem layer **64** of the partition **6** facing the end portion P**12**. The upper electrode UE**3** is spaced apart from the stem layer **64** of the partition **6** facing the end portion P**11**. However, the upper electrode UE**3** may be in contact with this stem layer **64**.
[0103] When the upper electrode UE**3** is spaced apart from the stem layer **64** of the partition **6** facing the end portion P**11**, the cap layer CP**3** is directly in contact with the upper surface of the bottom layer **63**. When the upper electrode UE**3** is spaced apart from the stem layer **64** of the partition **6** facing the end portion P**11**, the upper electrode UE**3** may be directly in contact with the upper surface of the bottom layer **63** or may not be in contact with the bottom layer **63**.
[0104] As shown in the enlarged view of each of the area including the end portion P**11** and the area including the end portion P**12**, in the upper electrode UE**3**, thickness T**12** immediately above the end portion P**12** is greater than thickness T**11** immediately above the end portion P**11** (T**11**<T**12**). The area of contact between the lower portion **61** facing the end portion P**12** and the upper electrode UE**3** is greater than that between the lower portion **61** facing the end portion P**11** and the upper electrode UE**3**.
[0105] The multilayer body consisting of the organic layer OR**3**, the upper electrode UE**3** and the cap layer CP**3** is provided on the upper portion **62** of the partition **6**. The sealing layer SE**3** covers the cap layer CP**3** and the partition **6**. The sealing layer SE**3** is provided on the multilayer body located on the partition **6**.
[0106] It should be noted that the multilayer body located on the upper portion **62** of the partition **6** may be omitted in some cases. In these cases, a cavity is formed between the upper portion **62** of the partition **6** and the sealing layer SE**3**.
[0107] Now, this specification focuses attention on the subpixel SP**2** located on the right side of the figure. The organic layer OR**2** has an end portion P**13** in the second direction Y, and an end portion P**14** on a side opposite to the end portion P**13**. In FIG. **5**, each of an area including the end portion P**13** and an area including the end portion P**14** is enlarged. The end portion P**13** is located on a side opposite to the end portion P**12** across the intervening partition **6**. Each of the end portion P**13** and the end portion P**14** is located on the bottom layer **63** and is spaced apart from the stem layer **64**.
[0108] The bottom layer **63** overlapping the end portion P**13** has length L**13** which protrudes from the stem layer **64**. The bottom layer **63** overlapping the end portion P**14** has length L**14** which protrudes from the stem layer **64**. Length L**13** is different from length L**14**. In the example shown in the figure, length L**14** is greater than length L**13** (L**13**<L**14**).
[0109] The upper electrode UE**2** overlaps the organic layer OR**2**, goes beyond the end portion P**13** and the end portion P**14** and is directly in contact with the upper surfaces of the bottom layer **63**. In

the example shown in the figure, the upper electrode UE**2** is directly in contact with the side surface of the stem layer **64** of the partition **6** facing the end portion P**14**. The upper electrode UE**2** is spaced apart from the stem layer **64** of the partition **6** facing the end portion P**13**. However, the upper electrode UE**2** may be in contact with this stem layer **64**.

[0110] When the upper electrode UE**2** is spaced apart from the stem layer **64** of the partition **6** facing the end portion P**13**, the cap layer CP**2** is directly in contact with the upper surface of the bottom layer **63**. When the upper electrode UE**2** is spaced apart from the stem layer **64** of the partition **6** facing the end portion P**13**, the upper electrode UE**2** may be directly in contact with the upper surface of the bottom layer **63** or may not be in contact with the bottom layer **63**.

[0111] As shown in the enlarged view of each of the area including the end portion P**13** and the area including the end portion P**14**, in the upper electrode UE**2**, thickness T**14** immediately above the end portion P**14** is greater than thickness T**13** immediately above the end portion P**13** (T**13**<T**14**). The area of contact between the lower portion **61** facing the end portion P**14** and the upper electrode UE**2** is greater than that between the lower portion **61** facing the end portion P**13** and the upper electrode UE**2**.

[0112] The multilayer body consisting of the organic layer OR**2**, the upper electrode UE**2** and the cap layer CP**2** is provided on the upper portion **62** of the partition **6**. The sealing layer SE**2** covers the cap layer CP**2** and the partition **6**. The sealing layer SE**2** is provided on the multilayer body located on the partition **6**. On the partition **6**, the sealing layer SE**2** is spaced apart from the sealing layer SE**3**.

[0113] It should be noted that the multilayer body located on the upper portion **62** of the partition **6** may be omitted in some cases. In these cases, a cavity is formed between the upper portion **62** of the partition **6** and the sealing layer SE**2**.

[0114] Now, this specification focuses attention on the partition **6** located between subpixel SP**2** and subpixel SP**3**.

[0115] In the bottom layer **63**, length L**12** which protrudes from the stem layer **64** toward subpixel SP**3** is greater than length L**13** which protrudes from the stem layer **64** toward subpixel SP**2** (L**12**>L**13**).

[0116] Difference Δ**3** between length L**11** and length L**12** in subpixel SP**3** is different from difference Δ**2** between length L**13** and length L**14** in subpixel SP**2** (Δ**3**≠Δ**2**). Difference Δ**1** between length L**1** and length L**2** in subpixel SP**1** shown in FIG. **4** is different from each of differences A**2** and A**3**.

[0117] For example, in a case where subpixel SP**1**, subpixel SP**2** and subpixel SP**3** are formed in this order, the relationship of the differences could be as follows.

Δ3>Δ2>Δ1

[0118] Thickness T**12** of the upper electrode UE**3** immediately above the end portion P**12** is greater than thickness T**13** of the upper electrode UE**2** immediately above the end portion P**13** (T**12**>T**13**).

[0119] In the example shown in FIG. **5**, for example, the lower electrode LE**3** corresponds to the first lower electrode, and the lower electrode LE**2** corresponds to the second lower electrode. The organic layer OR**3** corresponds to the first organic layer. The end portion P**11** corresponds to the first end portion. The end portion P**12** corresponds to the second end portion. The organic layer OR**2** corresponds to the second organic layer. The end portion P**13** corresponds to the third end portion. The end portion P**14** corresponds to the fourth end portion. Length L**11** corresponds to the first length. Length L**12** corresponds to the second length. Length L**13** corresponds to the third length. Length L**14** corresponds to the fourth length. The upper electrode UE**3** corresponds to the first upper electrode. Thickness T**11** corresponds to the first thickness. Thickness T**12** corresponds to the second thickness. The upper electrode UE**2** corresponds to the second upper electrode. Thickness T**13** corresponds to the third thickness. Thickness T**14** corresponds to the fourth thickness. The cap layer CP**3** corresponds to the first cap layer. The cap layer CP**2** corresponds to

the second cap layer. The sealing layer SE**3** corresponds to the first sealing layer. The sealing layer SE**2** corresponds to the second sealing layer.
[0120] Now, this specification explains an evaporation device EV for forming each upper electrode.
[0121] FIG. **6** is a diagram for explaining the evaporation device EV.
[0122] The evaporation device EV comprises an evaporation source **110** configured to emit a conductive material M for forming each upper electrode. The processing substrate SUB shown in this figure is prepared by forming a circuit layer **11**, an insulating layer **12**, a lower electrode LE, an inorganic insulating layer **5**, a partition **6** and an organic layer OR on a substrate **10**. The processing substrate SUB has an end SUBA, and the other end SUBB on a side opposite to the end SUBA. In the example shown in the figure, the processing substrate SUB is conveyed such that the end SUBA is the leading end. The conveyance direction TD of the processing substrate SUB is shown by an arrow in the figure.
[0123] The extension direction of the evaporation source **110** is shown by the dotted line in the figure. The normal of the substrate **10** is shown by the dash-dot line in the figure. The extension direction of the evaporation source **110** inclines with respect to the normal of the substrate **10**. Here, the extension direction is, for example, the direction in which a nozzle **120** controlling the emission direction of the conductive material M extends. The evaporation direction D of the conductive material M by the evaporation source **110** is shown by an arrow in the figure. The evaporation direction D is the direction from the bottom portion **111** of the evaporation source **110** to the opening portion **112** of the evaporation source **110**. In other words, the bottom portion **111** is located on the upstream side of the evaporation direction D, and the opening portion **112** is located on the downstream side of the evaporation direction D. When the arrow indicating the evaporation direction D points right as shown in the figure, the conductive material M is emitted from the left side of the figure to the right side. In the example shown in the figure, the evaporation direction D is the opposite direction of the conveyance direction TD. However, the evaporation direction D may be the same direction as the conveyance direction TD.
[0124] In this evaporation source EV, the evaporation source **110** is fixed, and emits the conductive material M. The conductive material M is a mixture of magnesium and silver. The conductive material M emitted from the evaporation source **110** is deposited on the processing substrate SUB while the processing substrate SUB is conveyed such that the end SUBA is the leading end and the partition **6** is used as a mask. By this process, an upper electrode UE is formed on the organic layer OR.
[0125] As another example of the evaporation device EV, the evaporation source **110** may be configured to be movable while emitting the conductive material M. In such an evaporation device EV, the conductive material M is deposited on the processing substrate SUB as the evaporation source **110** emits the conductive material M to the fixed processing substrate SUB while moving.
[0126] As yet another example of the evaporation device EV, the evaporation source **110** moves while emitting the conductive material M, and the processing substrate may be conveyed.
[0127] In other words, the upper electrode is formed as the conductive material M emitted from the evaporation source **110** is deposited on the processing substrate SUB while the relative position of the processing substrate SUB and the evaporation source **110** is changed in the evaporation device EV.
[0128] When the evaporation direction D is the direction from left to right as shown in the figure, in the subpixel SPX located at the center of the figure, the conductive material M is not easily deposited near the left partition **6**L, and the conductive material M is easily deposited near the right partition **6**R. For this reason, the thickness of the upper electrode formed near the partition **6**R is greater than that of the upper electrode formed near the partition **6**L.
[0129] By this process, the upper electrode UE**1** having thicknesses T**1** and T**2** as explained with reference to FIG. **4** is formed. Further, the upper electrode UE**3** having thicknesses T**11** and T**12** and the upper electrode UE**2** having thicknesses T**13** and T**14** as explained with reference to FIG. **5**

are formed.
[0130] FIG. **7** is a diagram for explaining an example of the evaporation direction D when an upper electrode is formed in each subpixel.
[0131] In subpixel SP**1**, the aperture AP**1** of the inorganic insulating layer **5** overlaps the lower electrode LE**1**, and the organic layer OR**1** is provided on the lower electrode LE**1** in the aperture AP**1**. The evaporation direction D for forming the upper electrode UE**1** on the organic layer OR**1** is shown by an arrow in the figure. The end portion P**1** of the organic layer OR**1** is located on the upstream side of the evaporation direction D. The end portion P**2** of the organic layer OR**1** is located on the downstream side of the evaporation direction D.
[0132] Near the end portion P**1**, the conductive material forming the upper electrode UE**1** is not easily deposited because of the effect of the partition **6**. To the contrary, near the end portion P**2**, the conductive material forming the upper electrode UE**1** goes into the lower side of the partition **6**, and thus, the upper electrode UE**1** can be electrically connected to the partition **6**.
[0133] In subpixel SP**3**, the aperture AP**3** of the inorganic insulating layer **5** overlaps the lower electrode LE**3**, and the organic layer OR**3** is provided on the lower electrode LE**3** in the aperture AP**3**. The evaporation direction D for forming the upper electrode UE**3** on the organic layer OR**3** is shown by an arrow in the figure. The end portion P**11** of the organic layer OR**3** is located on the upstream side of the evaporation direction D. The end portion P**12** of the organic layer OR**3** is located on the downstream side of the evaporation direction D.
[0134] Near the end portion P**11**, the conductive material forming the upper electrode UE**3** is not easily deposited because of the effect of the partition **6**. To the contrary, near the end portion P**12**, the conductive material forming the upper electrode UE**3** goes into the lower side of the partition **6**, and thus, the upper electrode UE**3** can be electrically connected to the partition **6**.
[0135] In subpixel SP**2**, the aperture AP**2** of the inorganic insulating layer **5** overlaps the lower electrode LE**2**, and the organic layer OR**2** is provided on the lower electrode LE**2** in the aperture AP**2**. The evaporation direction D for forming the upper electrode UE**2** on the organic layer OR**2** is shown by an arrow in the figure. The end portion P**13** of the organic layer OR**2** is located on the upstream side of the evaporation direction D. The end portion P**14** of the organic layer OR**2** is located on the downstream side of the evaporation direction D.
[0136] Near the end portion P**13**, the conductive material forming the upper electrode UE**2** is not easily deposited because of the effect of the partition **6**. To the contrary, near the end portion P**14**, the conductive material forming the upper electrode UE**2** goes into the lower side of the partition **6**, and thus, the upper electrode UE**2** can be electrically connected to the partition **6**.
[0137] All of the evaporation directions D for forming the upper electrodes UE**1**, UE**2** and UE**3** are the same as In the example shown in the figure, the evaporation directions D are substantially parallel to the second direction Y in which subpixels SP**2** and SP**3** are arranged. The both end portions P**1** and P**2** of the organic layer OR**1** are located in the both end portions of subpixel SP**1** in the second direction Y. The both end portions P**11** and P**12** of the organic layer OR**3** are located in the both end portions of subpixel SP**3** in the second direction Y. The both end portions P**13** and P**14** of the organic layer OR**2** are located in the both end portions of subpixel SP**2** in the second direction Y.
[0138] FIG. **8** is a diagram for explaining another example of the evaporation direction D when an upper electrode is formed in each subpixel.
[0139] The example shown in FIG. **8** is different from that shown in FIG. **7** in respect that the evaporation directions D for forming the upper electrodes UE**1**, UE**2** and UE**3** are substantially parallel to the first direction X.
[0140] The both end portions P**1** and P**2** of the organic layer OR**1** are located in the both end portions of subpixel SP**1** in the first direction X. Near the end portion P**2** located on the downstream side of the evaporation direction D, the conductive material forming the upper electrode UE**1** goes into the lower side of the partition **6**, and thus, the upper electrode UE**1** can be

electrically connected to the partition **6**. The both end portions P**11** and P**12** of the organic layer OR**3** are located in the both end portions of subpixel SP**3** in the first direction X. Near the end portion P**12** located on the downstream side of the evaporation direction D, the conductive material forming the upper electrode UE**3** goes into the lower side of the partition **6**, and thus, the upper electrode UE**3** can be electrically connected to the partition **6**.

[0141] The both end portions P**13** and P**14** of the organic layer OR**2** are located in the both end portions of subpixel SP**2** in the first direction X. Near the end portion P**14** located on the downstream side of the evaporation direction D, the conductive material forming the upper electrode UE**2** goes into the lower side of the partition **6**, and thus, the upper electrode UE**2** can be electrically connected to the partition **6**.

[0142] In the example shown in FIG. **8**, for example, the lower electrode LE corresponds to the first lower electrode, and the lower electrode LE**2** or the lower electrode LE**3** corresponds to the second lower electrode. The organic layer OR**1** corresponds to the first organic layer. The end portion P**1** corresponds to the first end portion. The end portion P**2** corresponds to the second end portion. The organic layer OR**2** or the organic layer OR**3** corresponds to the second organic layer. The end portion P**11** or the end portion P**13** corresponds to the third end portion. The end portion P**12** or the end portion P**14** corresponds to the fourth end portion.

[0143] Now, this specification explains the manufacturing method of the display device DSP. Regarding each figure for explaining the manufacturing method, the illustration of the lower side of the insulating layer **12** is omitted. FIG. **9** to FIG. **14** which are referred to in the following explanation correspond to the section taken along the A-B line of FIG. **2**.

[0144] First, as shown in FIG. **9**, a processing substrate SUB comprising the lower electrodes LE**1**, LE**2** and LE**3**, the inorganic insulating layer **5** and the partition **6** is prepared. The process of preparing the processing substrate SUB includes the following processes. The circuit layer **11** and the insulating layer **12** are formed over the display area DA and the surrounding area SA on the substrate **10**. Subsequently, the lower electrode LE**1** of subpixel SP**1**, the lower electrode LE**2** of subpixel SP**2** and the lower electrode LE**3** of subpixel SP**3** are formed on the insulating layer **12**. Subsequently, the inorganic insulating layer **5** which covers the peripheral portions of the lower electrodes LE**1**, LE**2** and LE**3** is formed. Subsequently, the partition **6** which has the lower portion **61** located on the inorganic insulating layer **5** and the upper portion **62** located on the lower portion **61** is formed. The bottom layer **63** of the lower portion **61** and the upper portion **62** protrude from the side surfaces of the stem layer **64** of the lower portion **61**. The bottom layer **63** is formed of a titanium-based material, and the stem layer **64** is formed of an aluminum-based material.

[0145] It should be noted that the process of forming the apertures AP**1**, AP**2** and AP**3** in the inorganic insulating layer **5** may be performed either before the partition **6** is formed or after the partition **6** is formed.

[0146] Subsequently, the display element DE**1** is formed.

[0147] First, as shown in FIG. **10**, the stacked film FL**1** including the organic layer OR**1**, the upper electrode UE**1** and the cap layer CP**1** is formed. The process of forming the stacked film FL**1** includes the process of forming the organic layer OR**1** on the lower electrode LE**1** in the aperture AP**1**, the process of forming the upper electrode UE**1** which covers the organic layer OR**1** and is in contact with the lower portion **61** of the partition **6**, and the process of forming the cap layer CP**1** on the upper electrode UE**1**. The process of forming the organic layer OR**1** includes the process of forming each of the hole injection layer, the hole transport layer, the electron blocking layer, the light emitting layer EM**1**, the hole blocking layer, the electron transport layer, the electron injection layer and the like. The upper electrode UE**1** is formed of a mixture of magnesium and silver.

[0148] Each of the organic layer OR**1**, the upper electrode UE**1** and the cap layer CP**1** is formed by vapor deposition using the partition **6** as a mask. In particular, the upper electrode UE**1** is formed by depositing the conductive material emitted from the evaporation source **110** which inclines with respect to the normal of the processing substrate SUB in the evaporation device EV explained with

reference to FIG. **6**.
[0149] The stacked film FL**1** is divided into a plurality of portions by the partition **6** having an overhang shape. These organic layer OR**1**, the upper electrode UE**1** and the cap layer CP**1** are continuously formed while maintaining a vacuum environment. This stacked film FL**1** is formed on the lower electrode LE**2** and the lower electrode LE**3** as well.
[0150] Subsequently, the sealing layer SE**1** is formed on the stacked film FL**1** by depositing an inorganic insulating material. The sealing layer SE**1** is formed by chemical vapor deposition (CVD). The sealing layer SE**1** continuously covers the portions into which the stacked film FL**1** is divided, and the partition **6**.
[0151] Subsequently, as shown in FIG. **11**, a resist RS patterned into a predetermined shape is formed on the sealing layer SE**1**. The resist RS overlaps subpixel SP**1** and part of the partition **6** around subpixel SP**1**.
[0152] Subsequently, as shown in FIG. **12**, etching is performed using the resist RS as a mask. Thus, the sealing layer SE**1** exposed from the resist RS is removed by performing dry etching using the resist RS as a mask. Subsequently, the stacked film FL**1** exposed from the resist RS is removed. At this time, in the stacked film FL**1**, the cap layer CP**1**, the upper electrode UE**1** and the organic layer OR**1** are removed in this order. By this process, the stacked film FL**1** covered with the resist RS is left in subpixel SP**1**. Further, the upper portion **62** of the partition **6** is partly exposed, and the lower electrode LE**2** and the lower electrode LE**3** are exposed.
[0153] Subsequently, the resist RS is removed. By this process, the display element DE**1** is formed in subpixel SP**1**.
[0154] In the process of removing each of the sealing layer SE**1** and the stacked film FL**1** and further removing the resist RS, the stacked film FL**1** located on the upper portion **62** of the partition **6** may be removed in some cases. In these cases, a cavity is formed between the upper portion **62** and the sealing layer SE**1**. Subsequently, as shown in FIG. **13**, the display element DE**2** is formed. The procedure of forming the display element DE**2** is similar to that of forming the display element DE**1**. Specifically, the stacked film FL**2** is formed by forming the organic layer OR**2** including the light emitting layer EM**2**, the upper electrode UE**2** and the cap layer CP**2** in order on the lower electrode LE**2**. Subsequently, the sealing layer SE**2** is formed on the stacked film FL**2**. Subsequently, a resist is formed on the sealing layer SE**2**. The sealing layer SE**2**, the cap layer CP**2**, the upper electrode UE**2** and the organic layer OR**2** are patterned by etching using the resist as a mask. After this patterning, the resist is removed. In this manner, the display element DE**2** is formed in subpixel SP**2**, and the lower electrode LE**3** of subpixel SP**3** is exposed. It should be noted that, in the process of removing each of the sealing layer SE**2** and the stacked film FL**2** and further removing the resist, the stacked film FL**2** located on the upper portion **62** of the partition **6** may be removed in some cases. In these cases, a cavity is formed between the upper portion **62** and the sealing layer SE**2**.
[0155] Subsequently, as shown in FIG. **14**, the display element DE**3** is formed. The procedure of forming the display element DE**3** is similar to that of forming the display element DE**1**. Specifically, the stacked film FL**3** is formed by forming the organic layer OR**3** including the light emitting layer EM**3**, the upper electrode UE**3** and the cap layer CP**3** in order on the lower electrode LE**3**. Subsequently, the sealing layer SE**3** is formed on the stacked film FL**3**. Subsequently, a resist is formed on the sealing layer SE**3**. The sealing layer SE**3**, the cap layer CP**3**, the upper electrode UE**3** and the organic layer OR**3** are patterned by etching using the resist as a mask. After this patterning, the resist is removed. By this process, the display element DE**3** is formed in subpixel SP**3**. It should be noted that, in the process of removing each of the sealing layer SE**3** and the stacked film FL**3** and further removing the resist, the stacked film FL**3** located on the upper portion **62** of the partition **6** may be removed in some cases. In these cases, a cavity is formed between the upper portion **62** and the sealing layer SE**3**.
[0156] Subsequently, the resin layer **13**, the sealing layer **14** and the resin layer **15** shown in FIG. **3**

are formed in order. By this process, the display device DSP is completed.
[0157] In the manufacturing process described above, this specification assumes a case where the display element DE**1** is formed firstly, and the display element DE**2** is formed secondly, and the display element DE**3** is formed lastly. However, the formation order of the display elements DE**1**, DE**2** and DE**3** is not limited to this example.
[0158] In a case where each of the upper electrodes UE**1**, UE**2** and UE**3** is formed by the evaporation device EV explained with reference to FIG. **6**, as described above, the thickness differs near the both end portions of each of the upper electrodes. For example, in a case where the thickness near an end portion of an upper electrode is extremely thin, or the bottom layer is exposed from an upper electrode, when each of the sealing layers SE**1** and SE**2** is removed by dry etching, the upper electrode may not be able to exert the function as an etching stopper, and thus, there is a possibility that the bottom layer is damaged. This respect is specifically explained with reference to drawings.
[0159] FIG. **15** is a cross-sectional view of subpixels SP**2** and SP**3** in which the stacked film FL**1** is formed.
[0160] The evaporation direction D for forming the upper electrode UE**1** is the direction from left to right in the figure, and the direction from the end portion Pa of the organic layer OR**1** formed in subpixel SP**2** to the end portion Pb of the organic layer OR**1**.
[0161] Immediately after the stacked film FL**1** is formed, length La which protrudes from the stem layer **64** in the bottom layer **63** which overlaps the end portion Pa is substantially equal to length Lb which protrudes from the stem layer **64** in the bottom layer **63** which overlaps the end portion Pb. The thickness of the upper electrode UE**1** which covers the end portion Pa is less than that of the upper electrode UE**1** which covers the end portion Pb.
[0162] FIG. **16** is a cross-sectional view of subpixels SP**2** and SP**3** from which the stacked film FL**1** is removed.
[0163] The upper electrode UE**1** functions as an etching stopper when, of the stacked film FL**1**, for example, the sealing layer SE**1** is removed. However, when the thickness of the upper electrode UE**1** which covers the end portion Pa is extremely less, or the bottom layer **63** is exposed from the upper electrode UE**1**, the bottom layer **63** is damaged, thereby decreasing the thickness of the bottom layer **63**, and further, the bottom layer **63** is partly removed. In the example shown in the figure, the left bottom layer **63** is damaged and retracted. Thus, length La of the bottom layer **63** shown on the left side of the figure is less than length Lb of the bottom layer **63** shown on the right side of the figure.
[0164] In such a subpixel SP**2**, when the stacked film FL**2** is subsequently formed, the evaporation direction D of the upper electrode UE**2** is the same as the evaporation direction D of the upper electrode UE**1**. Therefore, the upper electrode UE**2** is in contact with the bottom layer **63** having length Lb substantially without being damaged in subpixel SP**2**. This configuration can prevent the defective connection between the upper electrode UE**2** and the partition **6**. Thus, compared to a case where the evaporation direction of the upper electrode UE**2** is the opposite direction of the evaporation direction of the upper electrode UE**1**, the reduction in reliability can be prevented.
[0165] In subpixel SP**3**, when each of the sealing layers SE**1** and SE**2** is removed by dry etching, the same portion of the bottom layer **63** is easily damaged, and the bottom layer **63** could be further retracted compared to the bottom layer **63** provided in subpixel SP**2**.
[0166] However, in such a subpixel SP**3**, similarly, when the stacked film FL**3** is subsequently formed, the evaporation direction D of the upper electrode UE**3** is the same as the evaporation directions D of the upper electrodes UE**1** and UE**2**. Therefore, the upper electrode UE**3** is in contact with the bottom layer **63** which is not substantially damaged in subpixel SP**3**. This configuration can prevent the defective connection between the upper electrode UE**3** and the partition **6**. Thus, compared to a case where the evaporation direction of the upper electrode UE**3** is the opposite direction of the evaporation directions of the upper electrodes UE**1** and UE**2**, the reduction in

reliability can be prevented.
[0167] Now, another configuration example is explained.
[0168] FIG. **17** is a diagram showing another example of the layout of subpixels SP**1**, SP**2** and SP**3**.
[0169] The example shown in FIG. **17** is different from that shown in FIG. **7** in respect that the electrode edge of part of each lower electrode does not overlap the partition **6** in plan view. All of the evaporation directions D for forming the upper electrodes UE**1**, UE**2** and UE**3** are substantially parallel to the second direction Y.
[0170] In the example shown in the figure, the lower electrode LE**1** has the electrode edge LE**1**A on the side on which the end portion P**1** of the organic layer OR**1** is located, and the electrode edge LE**1**B on the side on which the end portion P**2** is located. The electrode edge LE**1**A is located on the upstream side of the evaporation direction D, and the electrode edge LE**1**B is located on the downstream side of the evaporation direction D. The partition **6** does not overlap the electrode edge LE**1**A and overlaps the electrode edge LE**1**B.
[0171] To assuredly electrically connect the upper electrode UE**1** and the partition **6** to each other, it is important to prevent the break of the upper electrode UE**1** caused by the step of the inorganic insulating layer **5** which covers the lower electrode LE**1**. Thus, on the downstream side of the evaporation direction D, as the electrode edge LE**1**B of the lower electrode LE**1** overlaps the partition **6**, the formation of an undesired step in the inorganic insulating layer **5** is prevented. This configuration prevents the break of the upper electrode UE**1**.
[0172] To the contrary, the upstream side of the evaporation direction D does not have the restriction to assuredly connect the upper electrode UE**1** and the partition **6** to each other. For this reason, the electrode edge LE**1**A of the lower electrode LE**1** may not necessarily overlap the partition **6** on the upstream side of the evaporation direction D. Thus, compared to a case where the electrode edge overlaps the partition **6** over the whole circumference of the lower electrode LE**1**, the width of part of the partition **6** can be reduced, and further, the aperture AP**1** can be enlarged. In this manner, the area of light emission in subpixel SP**1** can be increased.
[0173] In the example shown in the figure, in the lower electrode LE**3** of subpixel SP**3**, similarly, the electrode edge located on the upstream side of the evaporation direction D does not overlap the partition **6**, and the electrode edge located on the downstream side of the evaporation direction D overlaps the partition **6**. Thus, in a manner similar to that of subpixel SP**1**, the upper electrode UE**3** and the partition **6** can be assuredly electrically connected to each other, and further, the area of light emission of subpixel SP**3** can be increased.
[0174] FIG. **18** is a diagram showing another example of the layout of subpixels SP**1**, SP**2** and SP**3**.
[0175] The example shown in FIG. **18** is different from that shown in FIG. **17** in respect that the evaporation directions D for forming the upper electrodes UE**1**, UE**2** and UE**3** are substantially parallel to the first direction X.
[0176] In the lower electrode LE**1** of subpixel SP**1**, the electrode edge LE**1**A located on the upstream side of the evaporation direction D does not overlap the partition **6**, and the electrode edge LE**1**B located on the downstream side of the evaporation direction D overlaps the partition **6**. Thus, the upper electrode UE**1** and the partition **6** can be assuredly electrically connected to each other, and further, the area of light emission of subpixel SP**1** can be increased.
[0177] In the example shown in the figure, in the lower electrode LE**2** of subpixel SP**2**, similarly, the electrode edge located on the upstream side of the evaporation direction D does not overlap the partition **6**, and the electrode edge located on the downstream side of the evaporation direction D overlaps the partition **6**. Thus, in a manner similar to that of subpixel SP**1**, the upper electrode UE**2** and the partition **6** can be assuredly electrically connected to each other, and further, the area of light emission of subpixel SP**2** can be increased.
[0178] Further, in the lower electrode LE**3** of subpixel SP**3**, similarly, the electrode edge located on the upstream side of the evaporation direction D does not overlap the partition **6**, and the electrode edge located on the downstream side of the evaporation direction D overlaps the partition **6**. Thus,

in a manner similar to that of subpixel SP**1**, the upper electrode UE**3** and the partition **6** can be assuredly electrically connected to each other, and further, the area of light emission of subpixel SP**3** can be increased.
[0179] As explained above, the present embodiment can provide a display device and a manufacturing method thereof such that the reduction in reliability can be prevented.
[0180] All of the display devices and manufacturing methods thereof that can be implemented by a person of ordinary skill in the art through arbitrary design changes to the display device and manufacturing method thereof described above as the embodiments of the present invention come within the scope of the present invention as long as they are in keeping with the spirit of the present invention.
[0181] Various modification examples which may be conceived by a person of ordinary skill in the art in the scope of the idea of the present invention will also fall within the scope of the invention. For example, even if a person of ordinary skill in the art arbitrarily modifies the above embodiments by adding or deleting a structural element or changing the design of a structural element, or by adding or omitting a step or changing the condition of a step, all of the modifications fall within the scope of the present invention as long as they are in keeping with the spirit of the invention.
[0182] Further, other effects which may be obtained from the above embodiments and are self-explanatory from the descriptions of the specification or can be arbitrarily conceived by a person of ordinary skill in the art are considered as the effects of the present invention as a matter of course.

Claims

1. A display device comprising: a substrate; a first lower electrode provided above the substrate; an inorganic insulating layer which covers a peripheral portion of the first lower electrode; a partition which has a conductive lower portion provided on the inorganic insulating layer, and an upper portion provided on the lower portion; a first organic layer which is provided on the first lower electrode and includes a first light emitting layer; and a first upper electrode which is provided on the first organic layer and is in contact with the lower portion of the partition, wherein the partition surrounds the first organic layer and the first upper electrode, the lower portion has a bottom layer provided on the inorganic insulating layer and a stem layer provided between the bottom layer and the upper portion, the bottom layer and the upper portion protrude from a side surface of the stem layer, the first organic layer has a first end portion overlapping the bottom layer, and a second end portion overlapping the bottom layer and located on a side opposite to the first end portion, and a first length which protrudes from the stem layer in the bottom layer overlapping the first end portion is different from a second length which protrudes from the stem layer in the bottom layer overlapping the second end portion.
2. The display device of claim 1, wherein the second length is greater than the first length, and a second thickness of the first upper electrode immediately above the second end portion is greater than a first thickness of the first upper electrode immediately above the first end portion.
3. The display device of claim 1, further comprising: a second lower electrode which has a peripheral portion covered with the inorganic insulating layer; a second organic layer which is provided on the second lower electrode and includes a second light emitting layer formed of a material different from the first light emitting layer; and a second upper electrode which is provided on the second organic layer and is in contact with the lower portion of the partition, wherein the partition surrounds the second organic layer and the second upper electrode, the second organic layer has a third end portion overlapping the bottom layer, and a fourth end portion overlapping the bottom layer and located on a side opposite to the third end portion, and a difference between a third length which protrudes from the stem layer in the bottom layer overlapping the third end portion and a fourth length which protrudes from the stem layer in the

bottom layer overlapping the fourth end portion is different from a difference between the first length and the second length.

4. The display device of claim 1, wherein the first lower electrode has a first electrode edge on a side on which the first end portion is located, and a second electrode edge on a side on which the second end portion is located, and the partition overlaps the first electrode edge and the second electrode edge.

5. The display device of claim 1, wherein the first lower electrode has a first electrode edge on a side on which the first end portion is located, and a second electrode edge on a side on which the second end portion is located, and the partition does not overlap the first electrode edge and overlaps the second electrode edge.

6. The display device of claim 1, further comprising: a first cap layer provided on the first upper electrode; and a first sealing layer which covers the first cap layer and the partition and is formed of an inorganic insulating material.

7. A display device comprising: a substrate; first and second lower electrodes provided above the substrate; an inorganic insulating layer which covers a peripheral portion of each of the first and second lower electrodes; a partition which has a conductive lower portion provided on the inorganic insulating layer, and an upper portion provided on the lower portion; a first organic layer which is provided on the first lower electrode and includes a first light emitting layer; a first upper electrode which is provided on the first organic layer and is in contact with the lower portion of the partition; a second organic layer which is provided on the second lower electrode and includes a second light emitting layer formed of a material different from the first light emitting layer; and a second upper electrode which is provided on the second organic layer and is in contact with the lower portion of the partition, wherein the partition surrounds the first organic layer, the first upper electrode, the second organic layer and the second upper electrode, the lower portion has a bottom layer provided on the inorganic insulating layer, and a stem layer provided between the bottom layer and the upper portion, the bottom layer and the upper portion protrude from a side surface of the stem layer, the first organic layer has a first end portion overlapping the bottom layer, and a second end portion overlapping the bottom layer and located on a side opposite to the first end portion, the second organic layer has a third end portion located on a side opposite to the second end portion across the intervening partition and overlapping the bottom layer, and a fourth end portion overlapping the bottom layer and located on a side opposite to the third end portion, a second thickness of the first upper electrode immediately above the second end portion is greater than a first thickness of the first upper electrode immediately above the first end portion, and a fourth thickness of the second upper electrode immediately above the fourth end portion is greater than a third thickness of the second upper electrode immediately above the third end portion.

8. The display device of claim 7, wherein the second thickness is greater than the third thickness.

9. The display device of claim 7, wherein a second length which protrudes from the stem layer in the bottom layer overlapping the second end portion is greater than a first length which protrudes from the stem layer in the bottom layer overlapping the first end portion.

10. The display device of claim 9, wherein a fourth length which protrudes from the stem layer in the bottom layer overlapping the fourth end portion is greater than a third length which protrudes from the stem layer in the bottom layer overlapping the third end portion.

11. The display device of claim 10, wherein the second length is greater than the third length.

12. The display device of claim 7, further comprising: a first cap layer provided on the first upper electrode; a first sealing layer which covers the first cap layer and the partition and is formed of an inorganic insulating material; a second cap layer provided on the second upper electrode; and a second sealing layer which covers the second cap layer and the partition and is formed of an inorganic insulating material, wherein the first sealing layer is spaced apart from the second sealing layer on the partition.

13. A manufacturing method of a display device, the method comprising: preparing a processing

substrate in which a first lower electrode, a second lower electrode, a third lower electrode, an inorganic insulating layer and a partition are formed above a substrate, the inorganic insulating layer covering a peripheral portion of each of the first, second and third lower electrodes, the partition including a lower portion located on the inorganic insulating layer and an upper portion which is located on the lower portion and protrudes from a side surface of the lower portion; forming a first stacked film including a first organic layer and a first upper electrode, on the first lower electrode, the first organic layer including a first light emitting layer, the first upper electrode being located on the first organic layer; forming a second stacked film including a second organic layer and a second upper electrode, on the second lower electrode, the second organic layer including a second light emitting layer different from the first light emitting layer, the second upper electrode being located on the second organic layer; and forming a third stacked film including a third organic layer and a third upper electrode, on the third lower electrode, the third organic layer including a third light emitting layer different from the first light emitting layer and the second light emitting layer, the third upper electrode being located on the third organic layer, wherein each of the first, second and third upper electrodes is formed by emitting a conductive material from an evaporation source which inclines with respect to a normal of the processing substrate and depositing the conductive material using the partition as a mask while changing relative position of the evaporation source and the processing substrate, and evaporation directions for forming the first upper electrode, the second upper electrode and the third upper electrode are same as each other.

14. The manufacturing method of claim 13, further comprising: forming a first sealing layer by an inorganic insulating material on the first stacked film after forming the first stacked film; forming a resist patterned into a predetermined shape on the first sealing layer; removing the first sealing layer and the first stacked film in order using the resist as a mask; and subsequently forming the second stacked film.

15. The manufacturing method of claim 13, wherein when each of the first, second and third upper electrodes is formed, the relative position is changed by conveying the processing substrate with respect to the fixed evaporation source.

16. The manufacturing method of claim 13, wherein when each of the first, second and third upper electrodes is formed, the relative position is changed by moving the evaporation source with respect to the fixed processing substrate.

17. The manufacturing method of claim 13, wherein when each of the first, second and third upper electrodes is formed, the relative position is changed by moving the evaporation source while conveying the processing substrate.