US Patent & Trademark Office
Patent Public Search | Text View

United States Patent	12394381
Kind Code	B2
Date of Patent	August 19, 2025
Inventor(s)	Shan; Zhenzhen et al.

Display substrate with metal layers and display device

Abstract

A display substrate includes a driving module arranged on the base substrate, the driving module includes a plurality of driving units, and the driving unit includes a plurality of stages of driving circuits; the driving unit includes a first signal line, and the driving circuit includes an output sub-circuit; the display substrate includes at least two metal layers stacked along a direction away from the base substrate; in at least one driving unit, an orthographic projection of the first signal line on the base substrate at least partially overlaps an orthographic projection of a first electrode or a second electrode of at least one transistor included in the output sub-circuit on the base substrate, the first electrode and the second electrode are arranged on the same metal layer, and the first electrode and the first signal line are arranged on different metal layers.

Inventors: **Shan; Zhenzhen (Beijing, CN), Lu; Jiangnan (Beijing, CN), Shang; Guangliang (Beijing, CN), Liu; Libin (Beijing, CN), Zhu; Jianchao (Beijing, CN), Yao; Xing (Beijing, CN)**

Applicant: **BOE TECHNOLOGY GROUP CO., LTD.** (Beijing, CN)

Family ID: **1000008764816**

Assignee: **BOE TECHNOLOGY GROUP CO., LTD. (Beijing, CN)**

Appl. No.: **18/044967**

Filed (or PCT Filed): **June 29, 2022**

PCT No.: **PCT/CN2022/102291**

PCT Pub. No.: **WO2024/000248**

PCT Pub. Date: January 04, 2024

Prior Publication Data

Document Identifier	Publication Date

Publication Classification

Int. Cl.: **G09G3/3258** (20160101)

U.S. Cl.:

CPC **G09G3/3258** (20130101); G09G2300/0426 (20130101)

Field of Classification Search

CPC: G09G (2300/0426)

References Cited

U.S. PATENT DOCUMENTS

Patent No.	Issued Date	Patentee Name	U.S. Cl.	CPC
2017/0345845	12/2016	Wu et al.	N/A	N/A
2020/0381461	12/2019	Lin et al.	N/A	N/A
2021/0312869	12/2020	Dai et al.	N/A	N/A
2022/0068212	12/2021	Yao et al.	N/A	N/A
2022/0310772	12/2021	Qing et al.	N/A	N/A
2022/0343856	12/2021	Yu et al.	N/A	N/A

FOREIGN PATENT DOCUMENTS

Patent No.	Application Date	Country	CPC
105807523	12/2015	CN	N/A
111816691	12/2019	CN	N/A
112838109	12/2020	CN	N/A
113097263	12/2020	CN	N/A
113471225	12/2020	CN	N/A
113870796	12/2020	CN	N/A
215771147	12/2021	CN	N/A
20070062742	12/2006	KR	N/A
2021203422	12/2020	WO	N/A

Primary Examiner: Polo; Gustavo

Attorney, Agent or Firm: McCoy Russell LLP

Background/Summary

CROSS REFERENCE TO RELATED APPLICATION

(1) The present disclosure is the U.S. national phase of PCT Application No. PCT/CN2022/102291 filed on Jun. 29, 2022, which is incorporated herein by reference in their entireties.

TECHNICAL FIELD

(2) The present disclosure relates to the field of display technology, in particular to a display substrate and a display device.

BACKGROUND

(3) Active-matrix organic light-emitting diode (AMOLED) display panel is widely used in various fields due to its advantages of low power consumption, low production cost, and wide color gamut.

(4) The AMOLED display panel includes a pixel circuit located in the display area and a driving module located in the edge area. The pixel circuit includes a plurality of pixel circuits arranged in an array. The arrangement of the driving modules determines the frame width of the AMOLED display panel.

SUMMARY

(5) In one aspect, the present disclosure provides in some embodiments a display substrate, including a driving module arranged on a base substrate, wherein the driving module includes a plurality of driving units, and the driving unit includes a plurality of stages of driving circuit; the driving circuit is used to provide a driving signal; the driving unit includes a first signal line, and the driving circuit includes an output sub-circuit configured to output the driving signal; the display substrate includes at least two metal layers stacked along a direction away from the base substrate; in at least one driving unit, an orthographic projection of the first signal line on the base substrate at least partially overlaps an orthographic projection of a first electrode of at least one transistor included in the output sub-circuit on the base substrate, the orthographic projection of the first signal line on the base substrate at least partially overlaps an orthographic projection of a second electrode of the at least one transistor included in the output sub-circuit on the base substrate; the first electrode and the second electrode are arranged on a same metal layer, and the first electrode and the first signal line are arranged on different metal layers.

(6) Optionally, an orthographic projection of a first signal line included in one driving circuit of the plurality of driving units on the base substrate at least partially overlaps an orthographic projection of a second signal line included in another driving unit of the plurality of driving units on the base substrate.

(7) Optionally, the first signal line and the second signal line are configured to provide a same signal.

(8) Optionally, the first signal line is a low voltage DC signal line, a high voltage DC signal line or a clock signal line; the second signal line is a low voltage DC signal line, a high voltage DC signal line or a clock signal line.

(9) Optionally, among the plurality of driving units, orthographic projections of at least three signal lines on the base substrate at least partially overlap.

(10) Optionally, the driving module includes a first driving unit; the first driving unit includes a plurality of stages of first driving circuits, and the first driving circuit is used to provide a first driving signal; the first driving unit includes a first first voltage line and a first second voltage line; the first driving circuit includes a first output sub-circuit; the first signal line is the first first voltage line; the first output sub-circuit includes a first driving transistor and a first driving reset transistor; a first electrode of the first driving transistor is electrically connected to the first second voltage line, a second electrode of the first driving transistor is electrically connected to a first electrode of the first driving reset transistor, and a second electrode of the first driving reset transistor is electrically connected to the first first voltage line; the display substrate includes a first metal layer and a second metal layer sequentially stacked along a direction away from the base substrate; the first electrode of the first driving transistor, the second electrode of the first driving transistor, the first electrode of the first driving reset transistor and the second electrode of the first driving reset transistor are both arranged on the first metal layer, and the first first voltage line is arranged on the second metal layer; an orthographic projection of the first electrode of the first driving transistor on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate; an orthographic projection of the second electrode of the first driving

transistor on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate; an orthographic projection of the first electrode of the first driving reset transistor on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate; an orthographic projection of the second electrode of the first driving reset transistor on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate.

(11) Optionally, the driving module includes a first driving unit; the first driving unit includes a plurality of stages of first driving circuits, and the first driving circuit is used to provide a first driving signal; the first driving unit includes a first first voltage line and a first second voltage line; the first driving circuit includes a first output sub-circuit; the first signal line is the first first voltage line; the first output sub-circuit includes a first driving transistor and a first driving reset transistor; a first electrode of the first driving transistor is electrically connected to the first second voltage line, a second electrode of the first driving transistor is electrically connected to a first electrode of the first driving reset transistor, and a second electrode of the first driving reset transistor is electrically connected to the first first voltage line; the display substrate includes a first metal layer, a second metal layer and a third metal layer which are sequentially stacked along a direction away from the base substrate; the first electrode of the first driving transistor, the second electrode of the first driving transistor, the first electrode of the first driving reset transistor, and the second electrode of the first driving reset transistor are all arranged on the first metal layer, and the first first voltage line is arranged on the third metal layer; an orthographic projection of the first electrode of the first driving transistor on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate; an orthographic projection of the second electrode of the first driving transistor on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate; an orthographic projection of the first electrode of the first driving reset transistor on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate; an orthographic projection of the second electrode of the first driving reset transistor on the base substrate at least partially overlaps with the orthographic projection of the first first voltage line on the base substrate.

(12) Optionally, the first driving unit further includes a second first voltage line, a first first clock signal line, a first second clock signal line, a first second voltage line, a first start signal line and a first reset line; the first first clock signal line, the first second clock signal line and the first reset line are all arranged on the first metal layer; the second first voltage line, the first start signal line and the first second voltage line are all arranged on the second metal layer.

(13) Optionally, the first driving circuit includes a first on-off control transistor and a second on-off control transistor; both a gate electrode of the first on-off control transistor and a gate electrode of the second on-off transistor are electrically connected to the second first voltage line; at least part of an orthographic projection of the second first voltage line on the base substrate is arranged between an orthographic projection of the gate electrode of the first on-off control transistor on the base substrate and an orthographic projection of a gate electrode of the second on-off control transistor on the base substrate.

(14) Optionally, an orthographic projection of the first start signal line on the base substrate is arranged between an orthographic projection of the second first voltage line on the base substrate and an orthographic projection of the first reset line on the base substrate.

(15) Optionally, the driving module includes a second driving unit; the first driving unit includes a plurality of stages of second driving circuits, and the second driving circuit is configured to provide a second driving signal; the second driving unit includes a third first voltage line; the second driving circuit includes a second output sub-circuit; the second output sub-circuit includes a second driving transistor; an orthographic projection of the third first voltage line on the base substrate is arranged on a side of an orthographic projection of the second driving transistor on the base

substrate away from a display area; the third first voltage line and the first first voltage line are arranged on different layers; an orthographic projection of the third first voltage line on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate.
(16) Optionally, the orthographic projection of the third first voltage line on the base substrate coincides with the orthographic projection of the first first voltage line on the base substrate.
(17) Optionally, the first driving circuit is configured to provide an N-type gate driving signal, and the second driving circuit is configured to provide a reset control signal.
(18) Optionally, the first first voltage line is arranged on the second metal layer, and the third first voltage line is arranged on the third metal layer; or, the first first voltage line is arranged on the third metal layer, and the third first voltage line is arranged on the second metal layer.
(19) Optionally, the first first voltage line and the third first voltage line are low-voltage DC signal lines; or, the first first voltage line and the third first voltage line are high-voltage DC signal lines.
(20) Optionally, the second output sub-circuit is arranged adjacent to the third first voltage line.
(21) Optionally, the second driving unit further comprises a second start signal line, a second first clock signal line, a second second clock signal line and a second second voltage line; the third first voltage line, the second start signal line, the second first clock signal line, the second second clock signal line and the second second voltage line are arranged in sequence along a direction close to the display area.
(22) Optionally, the second output sub-circuit further includes a second driving reset transistor; an orthographic projection of the second start signal line on the base substrate at least partially overlaps the orthographic projection of the first electrode of the second driving transistor on the base substrate, and the orthographic projection of the second start signal line on the base substrate at least partially overlaps the orthographic projection of the second electrode of the second driving transistor on the base substrate; the orthographic projection of the second start signal line on the base substrate at least partially overlaps an orthographic projection of a first electrode of the second driving reset transistor on the base substrate, and the orthographic projection of the second start signal line on the base substrate at least partially overlaps an orthographic projection of a second electrode of the second driving reset transistor on the base substrate.
(23) Optionally, an orthographic projection of a transistor included in the second driving circuit on the base substrate is arranged at a side of an orthographic projection of the third first voltage line on the base substrate close to the display area.
(24) Optionally, the second driving circuit further comprises a fifteenth transistor, a twentieth transistor, and a twenty-first transistor; a gate electrode of the fifteenth transistor is electrically connected to the second first clock signal line, and a second electrode of the fifteenth transistor is electrically connected to a second electrode of the twenty-first transistor; a first electrode of the twenty-first transistor is electrically connected to a second electrode of the twentieth transistor; a gate electrode of the twentieth transistor is electrically connected to the gate electrode of the second driving reset transistor, and a gate electrode of the twenty-first transistor is electrically connected to the second second clock signal line; an orthographic projection of the gate electrode of the fifteenth transistor on the base substrate, an orthographic projection of the gate electrode of the twentieth transistor on the base substrate, and an orthographic projection of the gate electrode of the twenty-first transistor on the base substrate are arranged between the orthographic projection of the second second clock signal line on the base substrate and the orthographic projection of the second second voltage line on the base substrate.
(25) Optionally, the second driving circuit further comprises a sixteenth transistor; a gate electrode of the sixteenth transistor is electrically connected to the second electrode of the fifteenth transistor, a first electrode of the sixteenth transistor is electrically connected to the second first clock signal line, and a second electrode of the sixteenth transistor is electrically connected to the gate electrode of the driving reset transistor; an orthographic projection of the gate electrode of the sixteenth

transistor on the base substrate is arranged between the orthographic projection of the second first clock signal line on the base substrate and the orthographic projection of the second second clock signal line on the base substrate.
(26) Optionally, the base substrate includes a peripheral area and a display area; the driving units included in the driving module are all arranged in the peripheral area of the base substrate; the first driving unit is arranged on a side of the second driving unit away from the display area.
(27) Optionally, the driving module comprises a third driving unit, the third driving circuit includes a plurality of stages of third driving circuits, the third driving circuit is configured to provide a third driving signal, the third driving unit is arranged at a side of the first driving unit far away from the second driving unit.
(28) Optionally, the driving module comprises a fourth driving unit, the driving unit comprises a plurality of stages of fourth driving circuits, the fourth driving circuit is configured to provide a fourth driving signal; the fourth driving unit is arranged on a side of the second driving unit close to the display area.
(29) In a second aspect, a display device includes the display substrate.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
(1) FIG. **1** is a circuit diagram of a first driving circuit in a display substrate according to at least one embodiment of the present disclosure;
(2) FIG. **2** is a circuit diagram of a first driving circuit in a display substrate according to at least one embodiment of the present disclosure;
(3) FIG. **3** is a layout diagram corresponding to the first driving circuit shown in FIG. **2**;
(4) FIG. **4** is a layout diagram of the semiconductor layer in FIG. **3**;
(5) FIG. **5** is a layout diagram of the first gate metal layer in FIG. **3**;
(6) FIG. **6** is a layout diagram of the second gate metal layer in FIG. **3**;
(7) FIG. **7** is a layout diagram of the first metal layer in FIG. **3**;
(8) FIG. **8** is a layout diagram of the second metal layer in FIG. **3**;
(9) FIG. **9** is a circuit diagram of a second driving circuit in the display substrate of at least one embodiment of the present disclosure;
(10) FIG. **10** is a circuit diagram of a second driving circuit in a display substrate according to at least one embodiment of the present disclosure;
(11) FIG. **11** is a layout diagram corresponding to the second driving circuit shown in FIG. **10**;
(12) FIG. **12** is a layout diagram of the semiconductor layer in FIG. **11**;
(13) FIG. **13** is a layout diagram of the first gate metal layer in FIG. **11**;
(14) FIG. **14** is a layout diagram of the second gate metal layer in FIG. **11**;
(15) FIG. **15** is a layout diagram of the first metal layer in FIG. **11**;
(16) FIG. **16** is a layout diagram of the second metal layer in FIG. **11**;
(17) FIG. **17** is a layout diagram of the third metal layer in FIG. **11**;
(18) FIG. **18**A is a layout diagram of a first driving circuit and a second driving circuit included in the display substrate according to at least one embodiment of the present disclosure;
(19) FIG. **18**B is A-A′ sectional view in FIG. **18**A;
(20) FIG. **18**C is a layout diagram of the second source-drain metal layer in FIG. **18**A;
(21) FIG. **18**D is a layout diagram of the third source-drain metal layer in FIG. **18**A;
(22) FIG. **19** is a structural diagram of a display substrate according to at least one embodiment of the present disclosure;
(23) FIG. **20** is another layout diagram corresponding to the second driving circuit shown in FIG. **10**;

(24) FIG. **21** is a layout diagram of the semiconductor layer in FIG. **20**;
(25) FIG. **22** is a layout diagram of the first gate metal layer in FIG. **20**;
(26) FIG. **23** is a layout diagram of the second gate metal layer in FIG. **20**;
(27) FIG. **24** is a layout diagram of the first metal layer in FIG. **22**;
(28) FIG. **25** is a layout diagram of the second metal layer in FIG. **22**;
(29) FIG. **26** is a schematic diagram of the arrangement relationship between the first driving circuit shown in FIG. **3** and the second driving circuit shown in FIG. **20**;
(30) FIG. **27**A is a circuit diagram of a third driving circuit in the display substrate of at least one embodiment of the present disclosure;
(31) FIG. **27**B is a circuit diagram of a third driving circuit in the display substrate of at least one embodiment of the present disclosure;
(32) FIG. **28** is a layout diagram corresponding to the third driving circuit shown in FIG. **27**B;
(33) FIG. **29** is a layout diagram of the semiconductor layer in FIG. **28**;
(34) FIG. **30** is a layout diagram of the first gate metal layer in FIG. **28**;
(35) FIG. **31** is a layout diagram of the second gate metal layer in FIG. **28**;
(36) FIG. **32** is a layout diagram of the first metal layer in FIG. **28**;
(37) FIG. **33**A is a circuit diagram of a fourth driving circuit in a display substrate according to at least one embodiment of the present disclosure;
(38) FIG. **33**B is a circuit diagram of a fourth driving circuit in the display substrate according to at least one embodiment of the present disclosure;
(39) FIG. **34** is a layout diagram corresponding to at least one embodiment of the fourth driving circuit shown in FIG. **33**B;
(40) FIG. **35** is a layout diagram of the semiconductor layer in FIG. **34**;
(41) FIG. **36** is a layout diagram of the first gate metal layer in FIG. **34**;
(42) FIG. **37** is a layout diagram of the second gate metal layer in FIG. **34**;
(43) FIG. **38** is a layout diagram of the first metal layer in FIG. **34**;
(44) FIG. **39** is a layout diagram of a second metal layer added on the layout diagram shown in FIG. **34**;
(45) FIG. **40** is a structural diagram of a display substrate according to at least one embodiment of the present disclosure;
(46) FIG. **41** is a structural diagram of a display substrate according to at least one embodiment of the present disclosure;
(47) FIG. **42** is a structural diagram of a display substrate according to at least one embodiment of the present disclosure;
(48) FIG. **43** is a structural diagram of a display substrate according to at least one embodiment of the present disclosure.

DETAILED DESCRIPTION

(49) The following will clearly and completely describe the technical solutions in the embodiments of the present disclosure with reference to the accompanying drawings. Apparently, the described embodiments are only some of the embodiments of the present disclosure, not all of them. Based on the embodiments in the present disclosure, all other embodiments obtained by persons of ordinary skill in the art without creative efforts belong to the protection scope of the present disclosure.
(50) The transistors used in all the embodiments of the present disclosure may be triodes, thin film transistors or field effect transistors or other devices with the same characteristics. In the embodiments of the present disclosure, in order to distinguish the two electrodes of the transistor except the gate electrode, one electrode is called the first electrode, and the other electrode is called the second electrode.
(51) In actual operation, when the transistor is a thin film transistor or a field effect transistor, the first electrode may be a drain electrode, and the second electrode may be a source electrode; or, the

first electrode may be a source electrode, the second electrode may be a drain electrode.
(52) The display substrate described in the embodiment of the present disclosure includes a driving module arranged on the base substrate, the driving module includes a plurality of driving units, and the driving unit includes a plurality of stages of driving circuit; the driving circuit is used to provide a driving signal;
(53) The driving unit includes a first signal line, and the driving circuit includes an output sub-circuit configured to output the driving signal;
(54) The display substrate includes at least two metal layers stacked along a direction away from the base substrate;
(55) In at least one driving unit, an orthographic projection of the first signal line on the base substrate at least partially overlaps an orthographic projection of a first electrode of at least one transistor included in the output sub-circuit on the base substrate, the orthographic projection of the first signal line on the base substrate at least partially overlaps an orthographic projection of a second electrode of the at least one transistor included in the output sub-circuit on the base substrate;
(56) The first electrode and the second electrode are arranged on the same metal layer, and the first electrode and the first signal line are arranged on different metal layers.
(57) The display substrate described in the embodiment of the present disclosure includes a driving module, and in at least one driving unit included in the driving module, the first electrode and the second electrode are arranged on the same metal layer, and the first electrode and the first signal line are arranged on different metal layers; the orthographic projection of the first signal line on the base substrate at least partially overlaps the orthographic projection of the first electrode of the at least one transistor included in the output sub-circuit on the base substrate, the orthographic projection of the first signal line on the base substrate at least partially overlaps the orthographic projection of the second electrode of the at least one transistor included in the output sub-circuit on the base substrate, so as to reduce the width of the display substrate in the first direction, which is conducive to realizing a narrow frame.
(58) In at least one embodiment of the present disclosure, the first direction may be an extending direction of the gate lines, for example, the first direction may be a horizontal direction, but not limited thereto.
(59) In at least one embodiment of the present disclosure, the orthographic projection of the first signal line included in one of the plurality of driving units on the base substrate at least partially overlaps the orthographic projection of the second signal lines included in another driving unit of the plurality of driving units on the base substrate.
(60) During specific implementation, the orthographic projection of the first signal line on the base substrate at least partially overlaps the orthographic projection of the second signal line on the base substrate, so as to reduce the width of the display substrate in the first direction, which is conducive to achieving narrow borders.
(61) Optionally, the first signal line and the second signal line are configured to provide the same signal.
(62) Optionally, the first signal line is a low-voltage DC signal line, a high-voltage DC signal line or a clock signal line;
(63) The second signal line is a low voltage DC signal line, a high voltage DC signal line or a clock signal line.
(64) In at least one embodiment of the present disclosure, the first signal line and the second signal line may be configured to provide the same signal, for example, the first signal line and the second signal line may both be low voltage DC signal line, or both the first signal line and the second signal line may be high-voltage DC signal lines, or both the first signal line and the second signal line may be clock signal lines; but not limited to this.
(65) In specific implementation, the first signal line and the second signal line can also be

configured to provide different signals, for example, the first signal line can be a low-voltage DC signal line, and the second signal line may be a high-voltage DC signal line; or, the first signal line may be a clock signal line, and the second signal line may be a high-voltage DC signal line; or, the first signal line may be a clock signal line, the second signal line may be a low-voltage DC signal line; but not limited thereto.

(66) In at least one embodiment of the present disclosure, among the plurality of driving units, orthographic projections of at least three signal lines on the base substrate at least partially overlap.

(67) In a specific implementation, among the plurality of driving units, the orthographic projections of at least three signal lines on the base substrate at least partially overlap, so as to reduce the width of the display substrate in the first direction, which facilitates the narrow frame.

(68) In at least one embodiment of the present disclosure, the driving module includes a first driving unit; the first driving unit includes a plurality of stages first driving circuit, and the first driving circuit is used to provide a first driving signal; the first driving unit includes a first first voltage line and a first second voltage line; the first driving circuit includes a first output sub-circuit; the first signal line is the first first voltage line;

(69) The first output sub-circuit includes a first driving transistor and a first driving reset transistor;

(70) A first electrode of the first driving transistor is electrically connected to the first second voltage line, a second electrode of the first driving transistor is electrically connected to the first electrode of the first driving reset transistor, and a second electrode of the first driving reset transistor is electrically connected to the first first voltage line;

(71) The display substrate includes a first metal layer and a second metal layer sequentially stacked along a direction away from the base substrate; the first electrode of the first driving transistor, the second electrode of the first driving transistor, the first electrode of the first driving reset transistor and the second electrode of the first driving reset transistor are both arranged on the first metal layer, and the first first voltage line is arranged on the second metal layer;

(72) The orthographic projection of the first electrode of the first driving transistor on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate; the orthographic projection of the second electrode of the first driving transistor on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate; the orthographic projection of the first electrode of the first driving reset transistor on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate; the orthographic projection of the second electrode of the first driving reset transistor on the base substrate at least partially overlaps with the orthographic projection of the first first voltage line on the base substrate.

(73) Optionally, the first driving unit is used to provide a first driving signal, the first driving signal may be an N-type gate driving signal, and the N-type gate driving signal may be provided to the N-type transistors included in the pixel circuit and having a valid high-level, but not limited thereto.

(74) In at least one embodiment of the present disclosure, the first driving transistor and the first driving reset transistor may be arranged along a second direction;

(75) The second direction may be the extending direction of the first first voltage line, for example, the second direction may be a vertical direction, but not limited thereto.

(76) Optionally, the first voltage line may be a low voltage line, and the second voltage line may be a high voltage line, but not limited thereto.

(77) In at least one embodiment of the present disclosure, the driving module includes a first driving unit; the first driving unit includes a plurality of stages of first driving circuits, and the first driving circuit is used to provide a first driving signal; the first driving unit includes a first first voltage line and a first second voltage line; the first driving circuit includes a first output sub-circuit; the first signal line is the first first voltage line;

(78) The first output sub-circuit includes a first driving transistor and a first driving reset transistor;

(79) The first electrode of the first driving transistor is electrically connected to the first second

voltage line, the second electrode of the first driving transistor is electrically connected to the first electrode of the first driving reset transistor, and the second electrode of the first driving reset transistor is electrically connected to the first first voltage line;

(80) The display substrate includes a first metal layer, a second metal layer and a third metal layer which are sequentially stacked along a direction away from the base substrate; the first electrode of the first driving transistor, the second electrode of the first driving transistor, the first electrode of the first driving reset transistor, and the second electrode of the first driving reset transistor are all arranged on the first metal layer, and the first first voltage line is arranged on the second metal layer or the third metal layer;

(81) The orthographic projection of the first electrode of the first driving transistor on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate; the orthographic projection of the second electrode of the first driving transistor on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate; the orthographic projection of the first electrode of the first driving reset transistor on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate; the orthographic projection of the second electrode of the first driving reset transistor on the base substrate at least partially overlaps with the orthographic projection of the first first voltage line on the base substrate, so as to reduce the width of the display substrate along the first direction, which is beneficial to realize a narrow frame.

(82) In specific implementation, the display substrate may include three metal layers, the first electrode of the first driving transistor, the second electrode of the first driving transistor, the first electrode of the first driving reset transistor, and the second electrode of the first driving reset transistor are all arranged on the first metal layer, and the first first voltage line can be arranged on the second metal layer or the third metal layer.

(83) In at least one embodiment of the present disclosure, the first metal layer may be a first source-drain metal layer, the second metal layer may be a second source-drain metal layer, and the third metal layer may be a third source-drain metal layer, but not limited thereto.

(84) As shown in FIG. **1**, at least one embodiment of the first driving circuit includes a first output sub-circuit **10**;

(85) The first output sub-circuit **10** includes a first driving transistor T**9** and a first driving reset transistor T**10**;

(86) The first driving circuit further includes a first transistor T**1**, a second transistor T**2**, a third transistor T**3**, a fourth transistor T**4**, a fifth transistor T**5**, a sixth transistor T**6**, a seventh transistor T**7**, an eighth transistor T**8**, an eleventh transistor T**11**, a twelfth transistor T**12**, a first on-off control transistor T**13**, a second on-off control transistor T**14**, a first capacitor C**1**, a second capacitor C**2** and a third capacitor C**3**;

(87) The gate electrode of T**1** is electrically connected to the first second clock signal line NCB, the first electrode of T**1** is electrically connected to the first input terminal I**1**, and the second electrode of T**1** is electrically connected to the gate electrode of T**2**;

(88) The first electrode of T**2** is electrically connected to the first second clock signal line NCB, and the second electrode of T**2** is electrically connected to the second electrode of T**3**;

(89) The gate electrode of T**3** is electrically connected to the first second clock signal line NCB, and the first electrode of T**3** is electrically connected to the second first voltage line VGL_N**2**;

(90) The gate electrode of T**4** is electrically connected to the gate electrode of T**5**, the first electrode of T**4** is electrically connected to the first first clock signal line NCK, the second electrode of T**4** is electrically connected to the first electrode plate of C**3**; the second electrode plate of C**3** is electrically connected to the gate electrode of T**5**;

(91) The gate electrode of T**5** is electrically connected to the first electrode of T**5**, and the second electrode of T**5** is electrically connected to the gate electrode of T**10**;

(92) The gate electrode of T**6** is electrically connected to the first electrode plate of C**1**, the first

electrode of T**6** is electrically connected to the first first clock signal line NCK, and the second electrode of T**6** is electrically connected to the second electrode plate of C**1**;
(93) The gate electrode of T**7** is electrically connected to the first first clock signal line NCK, the first electrode of T**7** is electrically connected to the second electrode plate of C**1**, and the second electrode of T**7** is electrically connected to the gate electrode of T**9**;
(94) The gate electrode of T**8** is electrically connected to the gate electrode of T**2**, the first electrode of T**8** is electrically connected to the first second voltage line VGH_N, and the second electrode of T**8** is electrically connected to the gate electrode of T**9**;
(95) The first electrode of T**9** is electrically connected to the first second voltage line VGH_N, and the second electrode of T**9** is electrically connected to the first driving signal output terminal O**1**;
(96) The first electrode of T**10** is electrically connected to the first driving signal output terminal O**1**, and the second electrode of T**10** is electrically connected to the first first voltage line VGL_N**1**;
(97) The gate electrode of T**11** is electrically connected to the second electrode of T**6**, the first electrode of T**11** is electrically connected to the first second voltage line VGH_N, and the second electrode of T**11** is electrically connected to the gate electrode of T**10**;
(98) The gate electrode of T**12** is electrically connected to the first reset line RST_N, the first electrode of T**12** is electrically connected to the first second voltage line VGH_N, and the second electrode of T**12** is electrically connected to the gate electrode of T**10**;
(99) The gate electrode of T**13** is electrically connected to the second first voltage line VGL_N**2**, the first electrode of T**13** is electrically connected to the gate electrode of T**2**, and the second electrode of T**13** is electrically connected to the gate electrode of T**4**;
(100) The gate electrode of T**14** is electrically connected to the second first voltage line VGL_N**2**, the first electrode of T**14** is electrically connected to the second electrode of T**2**, and the second electrode of T**14** is electrically connected to the gate electrode of T**6**;
(101) The first electrode plate of C**2** is electrically connected to the gate electrode of T**9**, and the second electrode plate of C**2** is electrically connected to the first second voltage line VGH_N.
(102) In at least one embodiment shown in FIG. **1**, T**9** may be the ninth transistor included in the first driving circuit, and T**10** may be the tenth transistor included in the first driving circuit; T**13** may be a thirteenth transistor included in the first driving circuit, and T**14** may be a fourteenth transistor included in the first driving circuit;
(103) All transistors included in at least one embodiment of the first driving circuit shown in FIG. **1** may be P-type transistors, but not limited thereto.
(104) In at least one embodiment of the present disclosure, each first voltage line may be a low-voltage DC signal line, and each second voltage line may be a high-voltage DC signal line, but not limited thereto.
(105) FIG. **2** is a schematic diagram of labeling each electrode and each electrode plate on the basis of FIG. **1**.
(106) As shown in FIG. **2**, the first driving circuit includes a first output sub-circuit **10**;
(107) The first output sub-circuit **10** includes a first driving transistor T**9** and a first driving reset transistor T**10**;
(108) The first driving circuit further includes a first transistor T**1**, a second transistor T**2**, a third transistor T**3**, a fourth transistor T**4**, a fifth transistor T**5**, a sixth transistor T**6**, a seventh transistor T**7**, an eighth transistor T**8**, an eleventh transistor T**11**, a twelfth transistor T**12**, a first on-off control transistor T**13**, a second on-off control transistor T**14**, a first capacitor C**1**, a second capacitor C**2** and a third capacitor C**3**;
(109) The gate electrode G**1** of T**1** is electrically connected to the first second clock signal line NCB, the first electrode S**1** of T**1** is electrically connected to the first input terminal I**1**, and the second electrode D**1** of T**1** is electrically connected to the gate electrode G**2** of T**2**;
(110) The first electrode S**2** of T**2** is electrically connected to the first second clock signal line NCB, and the second electrode D**2** of T**2** is electrically connected to the second electrode D**3** of T**3**;

(111) The gate electrode G**3** of T**3** is electrically connected to the first second clock signal line NCB, and the first electrode S**3** of T**3** is electrically connected to the second first voltage line VGL_N**2**;
(112) The gate electrode G**4** of T**4** is electrically connected to the gate electrode G**5** of T**5**, the first electrode S**4** of T**4** is electrically connected to the first first clock signal line NCK, and the second electrode D**4** of T**4** is electrically connected to the first electrode plate C**3***a* of C**3**; the second electrode plate C**3***b* of C**3** is electrically connected to the gate electrode G**5** of T**5**;
(113) The gate electrode G**5** of T**5** is electrically connected to the first electrode S**5** of T**5**, and the second electrode D**5** of T**5** is electrically connected to the gate electrode G**10** of T**10**;
(114) The gate electrode G**6** of T**6** is electrically connected to the first electrode plate C**1***a* of C**1**, the first electrode S**6** of T**6** is electrically connected to the first first clock signal line NCK, and the second electrode D**6** of T**6** is electrically connected to the second electrode plate C**1***b* of C**1**;
(115) The gate electrode G**7** of T**7** is electrically connected to the first first clock signal line NCK, the first electrode S**7** of T**7** is electrically connected to the second electrode plate C**1***b* of C**1**, and the second electrode D**7** of T**7** is electrically connected to the gate electrode G**9** of T**9**;
(116) The gate electrode G**8** of T**8** is electrically connected to the gate electrode G**2** of T**2**, the first electrode S**8** of T**8** is electrically connected to the first second voltage line VGH_N, and the second electrode D**8** of T**8** is electrically connected to the gate electrode G**9** of T**9**;
(117) The first electrode S**9** of T**9** is electrically connected to the first second voltage line VGH_N, and the second electrode D**9** of T**9** is electrically connected to the first driving signal output terminal O**1**;
(118) The first electrode S**10** of T**10** is electrically connected to the first driving signal output terminal O**1**, and the second electrode D**10** of T**10** is electrically connected to the first first voltage line VGL_N**1**;
(119) The gate electrode G**11** of T**11** is electrically connected to the second electrode of T**6**, the first electrode S**11** of T**11** is electrically connected to the first second voltage line VGH_N, and the second electrode D**11** of T**11** is electrically connected to the gate electrode of T**10**;
(120) The gate electrode G**12** of T**12** is electrically connected to the first reset line RST_N, the first electrode S**12** of T**12** is electrically connected to the first second voltage line VGH_N, and the second electrode D**12** of T**12** is electrically connected to the gate electrode G**10** of T**10**;
(121) The gate electrode G**13** of T**13** is electrically connected to the second first voltage line VGL_N**2**, the first electrode S**13** of T**13** is electrically connected to the gate electrode G**2** of T**2**, and the second electrode D**13** of T**13** is electrically connected to the gate electrode G**4** of T**4**;
(122) The gate electrode G**14** of T**14** is electrically connected to the second first voltage line VGL_N**2**, the first electrode S**14** of T**14** is electrically connected to the second electrode D**2** of T**2**, and the second electrode D**14** of T**14** is electrically connected to the gate electrode G**6** of T**6**;
(123) The first electrode plate C**2***a* of C**2** is electrically connected to the gate electrode G**9** of T**9**, and the second electrode plate C**2***b* of C**2** is electrically connected to the first second voltage line VGH_N.
(124) FIG. **3** is a layout diagram corresponding to the first driving circuit shown in FIG. **2**.
(125) In FIG. **3**, the one labeled VGL_N**1** is the first first voltage line, the one labeled VGL_N**2** is the second first voltage line, the one labeled VGH_N is the first second voltage line, and the one labeled NCK is the first first clock signal line, the one labeled NCB is the first second clock signal line, the one labeled NSTV is the first start signal line, and the one labeled RST_N is the first reset line.
(126) FIG. **4** is a layout diagram of the semiconductor layer in FIG. **3**, FIG. **5** is a layout diagram of the first gate metal layer in FIG. **3**, FIG. **6** is a layout diagram of the second gate metal layer in FIG. **3**, and FIG. **7** is the layout diagram of the first metal layer in FIG. **3**, FIG. **8** is the layout diagram of the second metal layer in FIG. **3**.
(127) In at least one embodiment of the first driving circuit shown in FIGS. **3-8**, T**2**, T**11** and T**12**

are double-gate transistors, but not limited thereto.
(128) In FIG. **7**, the one labeled S**9** is the first electrode of T**9**, the one labeled D**9** is the second electrode of T**9**, the one labeled S**10** is the first electrode of T**10**, and the one labeled D**10** is the second electrode of T**10**;
(129) As shown in FIG. **3**-FIG. **8**, the orthographic projection of S**9** on the base substrate partially overlaps the orthographic projection of VGL_N**1** on the base substrate, and the orthographic projection of D**9** on the base substrate partially overlaps the orthographic projection of VGL_N**1** on the base substrate, the orthographic projection of S**10** on the base substrate partially overlaps the orthographic projection of VGL_N**1** on the base substrate, and the orthographic projection of D**10** on the base substrate partially overlaps the orthographic projection of VGL_N**1** on the base substrate, so as to reduce the width of the display substrate along the horizontal direction, which is conducive to realizing a narrow frame.
(130) Optionally, the first driving unit further includes a second first voltage line, a first first clock signal line, a first second clock signal line, a first second voltage line, a first start signal line and the first reset line;
(131) The first first clock signal line, the first second clock signal line and the first reset line are all arranged on the first metal layer;
(132) The second first voltage line, the first start signal line and the first second voltage line are all arranged on the second metal layer.
(133) As shown in FIG. **8**, the first first voltage line VGL_N**1**, the second first voltage line VGL_N**2**, the first start signal line NSTV and the first second voltage line VGH_N are all arranged on the second metal layer;
(134) As shown in FIG. **7**, the first first clock signal line NCK, the first second clock signal line NCB and the first reset line RST_N are all arranged on the first metal layer;
(135) As shown in FIG. **3**-FIG. **8**, the orthographic projection of NCB on the base substrate, the orthographic projection of NCK on the base substrate, the orthographic projection of VGL_N**2** on the base substrate, the orthographic projection of NSTV on the base substrate, the orthographic projection of RST_N on the base substrate, the orthographic projection of VGH_N on the base substrate and the orthographic projection of VGL_N**1** on the base substrate are arranged in sequence along a direction close to the display area;
(136) NCB, NCK, VGL_N**2**, NSTV, RST_N, VGH_N and VGL_N**1** may all extend along the vertical direction, but not limited thereto.
(137) As shown in FIG. **3**-FIG. **8**, G**9** and G**10** are arranged along the vertical direction.
(138) Optionally, the first driving circuit includes a first on-off control transistor and a second on-off control transistor;
(139) Both the gate electrode of the first on-off control transistor and the gate electrode of the second on-off transistor are electrically connected to the second first voltage line;
(140) At least part of the orthographic projection of the second first voltage line on the base substrate is arranged between the orthographic projection of the gate electrode of the first on-off control transistor on the base substrate and the orthographic projection of the gate electrode of the on-off control transistor on the base substrate.
(141) As shown in FIGS. **3**-**8**, the gate electrode G**13** of the first on-off control transistor T**13** and the gate electrode G**14** of the second on-off control transistor T**14** are electrically connected to each other through the first conductive connection portion L**1**;
(142) The first conductive connection portion L**1** is electrically connected to VGL_N**2** through a via hole;
(143) The part of the orthographic projection of VGL_N**2** on the base substrate is arranged between the orthographic projection of G**13** on the base substrate and the orthographic projection of G**14** on the base substrate, so that G**13** and G**14** are electrically connected to VGL_N**2**, and VGL_N**2** is set in the space between G**13** and G**14**, to reduce the width of the display substrate along the horizontal

direction and realize the narrow frame.
(144) In at least one embodiment of the present disclosure, the orthographic projection of the first start signal line on the base substrate is set between the orthographic projection of the second first voltage line on the base substrate and the orthographic projection of the first reset line on the base substrate.
(145) As shown in FIG. **3**-FIG. **8**, the orthographic projection of NSTV on the base substrate is set between the orthographic projection of VGL_N**2** on the base substrate and the orthographic projection of RST_N on the base substrate, so as to utilize the space between VGL_N**2** and RST_N to set NSTV, which is beneficial to reducing the width of the display substrate along the horizontal direction and realizing narrow frame.
(146) As shown in FIG. **3**-FIG. **8**, the orthographic projection of the first electrode plate C**1***a* of C**1** on the base substrate partially overlaps the orthographic projection of NSTV on the base substrate, and the orthographic projection of the second electrode plate C**1***b* of C**1** on the base substrate partially overlaps the orthographic projection of the NSTV on the base substrate;
(147) The orthographic projection of the first electrode plate C**3***a* of C**3** on the base substrate partially overlaps the orthographic projection of NSTV on the base substrate, and the orthographic projection of the second electrode plate C**3***b* of C**3** on the base substrate partially overlaps the orthographic projection of NSTV on the base substrate;
(148) The orthographic projection of gate electrode G**6** of T**6** on the base substrate is included in the orthographic projection of NSTV on the base substrate.
(149) As shown in FIG. **3**-FIG. **8**, T**1**, T**3** and T**14** are arranged in sequence along the vertical direction, T**7**, T**8** and T**5** are arranged in sequence along the vertical direction, and T**9** and T**10** are arranged in sequence along the vertical direction.
(150) As shown in FIG. **3**-FIG. **8**, the first electrode plate of each capacitor and the gate electrode of each transistor are arranged on the first gate metal layer, the second electrode plate of each capacitor is arranged on the second gate metal layer, and the active layer of each transistor is arranged on the semiconductor layer.
(151) In FIG. **4**, the one labeled A**9** is the active layer of T**9**, the one labeled A**10** is the active layer of T**10**, the one labeled S**1** is the first electrode of T**1**, and the one labeled D**1** is the second electrode of T**1**; the one labeled S**2** is the first electrode of T**2**, the one labeled D**2** is the second electrode of T**2**; the one labeled S**3** is the first electrode of T**3**, the one labeled D**3** is the second electrode of T**3**; the one labeled S**4** is the first electrode of T**4**, the one labeled D**4** is the second electrode of T**4**; the one labeled S**5** is the first electrode of T**5**, the one labeled D**5** is the second electrode of T**5**; the one labeled S**6** is the first electrode of T**6**, the one labeled D**6** is the second electrode of T**6**; the one labeled S**7** is the first electrode of T**7**, the one labeled D**7** is the second electrode of T**7**; the one labeled S**8** is the first electrode of T**8**, and the one labeled D**8** is the second electrode of T**8**; the one labeled S**11** is the first electrode of T**11**, the one labeled D**11** is the second electrode of T**11**; the one labeled S**12** is the first electrode of T**12**, and the one labeled D**12** is the second electrode of T**12**; the one labeled S**13** is the first electrode of T**13**, the one labeled D**13** is the second electrode of T**13**, the one labeled S**14** is the first electrode of T**14**, the one labeled D**14** is the second electrode of T**14**.
(152) In FIG. **5**, the one labeled G**1** is the gate electrode of T**1**, the one labeled G**2** is the gate electrode of T**2**, the one labeled G**3** is the gate electrode of T**3**, the one labeled G**4** is the gate electrode of T**4**, and the one labeled G**5** is the gate electrode of T**5**, the one labeled G**6** is the gate electrode of T**6**, the one labeled G**7** is the gate electrode of T**7**, the one labeled G**8** is the gate electrode of T**8**, the one labeled G**9** is the gate electrode of T**9**, and the one labeled G**10** is the gate electrode of T**10**, the one labeled G**11** is the gate electrode of T**11**, the one labeled G**12** is the gate electrode of T**12**, the one labeled G**13** is the gate electrode of T**13**, the one labeled G**14** is the gate electrode of T**14**; the one labeled C**1***a* is the first electrode plate of C**1**, the one labeled C**2***a* is the first electrode plate of C**2**, and the one labeled C**3***a* is the first electrode plate of C**3**.

(153) In FIG. **6**, the one labeled C**1***b* is the second electrode plate of C**1**, the one labeled C**2***b* is the second electrode plate of C**2**, and the one labeled C**3***b* is the second electrode plate of C**3**.
(154) Optionally, the first driving circuit is a driving circuit that generates an N-type gate driving signal, and the first driving signal is the N-type gate driving signal.
(155) In at least one embodiment of the present disclosure, the driving module includes a second driving unit; the first driving unit includes a plurality of stages of second driving circuit, and the second driving circuit is configured to provide a second driving signal; the second driving unit includes a third first voltage line; the second driving circuit includes a second output sub-circuit; the second output sub-circuit includes a second driving transistor;
(156) The orthographic projection of the third first voltage line on the base substrate is arranged on a side of the orthographic projection of the second driving transistor on the base substrate away from the display area;
(157) The third first voltage line and the first first voltage line are arranged on different layers;
(158) The orthographic projection of the third first voltage line on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate.
(159) In at least one embodiment of the present disclosure, the first signal line may be a first first voltage line, and the second signal line may be a third first voltage line, but not limited thereto.
(160) In specific implementation, the driving module can also include a second driving unit, which can be used to provide a second driving signal, and the second driving signal can be provided to the P-type transistor in the pixel circuit; the third first voltage line included in the second driving unit is arranged on a different layer from the first first voltage line, and the orthographic projection of the third first voltage line on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate, so as to reduce the width of the display substrate in the first direction and facilitate the realization of a narrow frame.
(161) In at least one embodiment of the present disclosure, the orthographic projection of the third first voltage line on the base substrate coincide with the orthographic projection of the first first voltage line on the base substrate, so as to realize the narrow frame.
(162) Optionally, the first first voltage line is arranged on the second metal layer, and the third first voltage line is arranged on the third metal layer; or,
(163) The first first voltage line is arranged on the third metal layer, and the third first voltage line is arranged on the second metal layer.
(164) As shown in FIG. **9**, the second driving circuit includes a second output sub-circuit **90**; the second output sub-circuit **90** includes a second driving transistor T**19** and a second driving reset transistor T**18**;
(165) At least one embodiment of the second driving circuit further includes a fifteenth transistor T**15**, a sixteenth transistor T**16**, a seventeenth transistor T**17**, a twentieth transistor T**20**, a twenty-first transistor T**21**, and a twenty-second transistor T**22**, a fourth capacitor C**4** and a fifth capacitor C**5**;
(166) The gate electrode of T**15** is electrically connected to the second first clock signal line RCK, the first electrode of T**15** is electrically connected to the second input terminal I**2**, and the second electrode of T**15** is electrically connected to the gate electrode of T**17**;
(167) The first electrode of T**17** is electrically connected to the second first clock signal line RCK, and the second electrode of T**17** is electrically connected to the gate electrode of T**18**;
(168) The gate electrode of T**16** is electrically connected to the second first clock signal line RCK, the first electrode of T**16** is electrically connected to the third first voltage line VGL_R, and the second electrode of T**16** is electrically connected to the gate electrode of T**20**;
(169) The gate electrode of T**18** is electrically connected to the first electrode plate of C**4**, the first electrode of T**18** is electrically connected to the second second voltage line VGH_R, and the second electrode of T**18** is electrically connected to the second driving signal output terminal O**2**;
(170) The gate electrode of T**19** is electrically connected to the first electrode plate of C**5**, the first

electrode of T**19** is electrically connected to the second driving signal output terminal O**2**, and the second electrode of T**19** is electrically connected to the second second clock signal line RCB;
(171) The gate electrode of T**20** is electrically connected to the gate electrode of T**18**, the first electrode of T**20** is electrically connected to the second second voltage line VGH_R, and the second electrode of T**20** is electrically connected to the first electrode of T**21**;
(172) The gate electrode of T**21** is electrically connected to the second second clock signal line RCB, and the second electrode of T**21** is electrically connected to the gate electrode of T**17**;
(173) The gate electrode of T**22** is electrically connected to the third first voltage line VGL_R, the first electrode of T**22** is electrically connected to the gate electrode of T**17**, and the second electrode of T**22** is electrically connected to the gate electrode of T**19**;
(174) The second electrode of C**4** is electrically connected to the second second voltage line VGH_R;
(175) The second electrode of C**5** is electrically connected to the second driving signal output terminal O**2**.
(176) In at least one embodiment of the second driving circuit shown in FIG. **9**, each transistor is a P-type transistor, but not limited thereto.
(177) FIG. **10** is a schematic diagram of labeling the electrodes of each transistor and the electrode plates of each capacitor on the basis of FIG. **9**.
(178) As shown in FIG. **10**, the gate electrode G**15** of T**15** is electrically connected to the second second clock signal line RCB, the first electrode S**15** of T**15** is electrically connected to the second input terminal I**2**, the second electrode D**15** of T**15** is connected to the gate electrode G**17** of T**17**;
(179) The first electrode S**17** of T**17** is electrically connected to the second first clock signal line RCK, and the second electrode D**17** of T**17** is electrically connected to the gate electrode of T**18**;
(180) The gate electrode G**16** of T**16** is electrically connected to the second first clock signal line RCK, the first electrode S**16** of T**16** is electrically connected to the third first voltage line VGL_R, and the second electrode D**16** of T**16** is electrically connected to the gate electrode of T**20**;
(181) The gate electrode G**18** of T**18** is electrically connected to the first electrode plate C**4***a* of C**4**, the first electrode S**18** of T**18** is electrically connected to the second second voltage line VGH_R, and the second electrode D**18** of T**18** is electrically connected to the second driving signal output terminal O**2**;
(182) The gate electrode G**19** of T**19** is electrically connected to the first electrode plate C**5***a* of C**5**, the first electrode S**19** of T**19** is electrically connected to the second driving signal output terminal O**2**, and the second electrode D**19** of T**19** is electrically connected to the second second clock signal line RCB;
(183) The gate electrode G**20** of T**20** is electrically connected to the gate electrode G**18** of T**18**, the first electrode S**20** of T**20** is electrically connected to the second second voltage line VGH_R, and the second electrode D**20** of T**20** is electrically connected to the first electrode S**21** of T**21**;
(184) The gate electrode G**21** of T**21** is electrically connected to the second second clock signal line RCB, and the second electrode D**21** of T**21** is electrically connected to the gate electrode G**17** of T**17**;
(185) The gate electrode G**22** of T**22** is electrically connected to the third first voltage line VGL_R, the first electrode S**22** of T**22** is electrically connected to the gate electrode G**17** of T**17**, and the second electrode D**22** of T**22** is electrically connected to the gate electrode G**19** of T**19**;
(186) The second electrode plate C**4***b* of C**4** is electrically connected to the second second voltage line VGH_R;
(187) The second electrode plate C**5***b* of C**5** is electrically connected to the second driving signal output terminal O**2**.
(188) In at least one embodiment of the present disclosure, the second driving unit further includes a second start signal line, a second first clock signal line, a second second clock signal line, and a second second voltage line;

(189) The third first voltage line, the second start signal line, the second first clock signal line, the second second clock signal line and the second second voltage line are arranged in sequence along the direction close to the display area.
(190) FIG. **11** is a layout diagram corresponding to the second driving circuit shown in FIG. **10**. FIG. **12** is a layout diagram of the semiconductor layer in FIG. **11**, FIG. **13** is a layout diagram of the first gate metal layer in FIG. **11**, FIG. **14** is a layout diagram of the second gate metal layer in FIG. **11**, FIG. **15** is a layout diagram of the first metal layer in FIG. **11**, FIG. **16** is a layout diagram of the second metal layer in FIG. **11**, and FIG. **17** is a layout diagram of the third metal layer in FIG. **11**.
(191) As shown in FIGS. **11-17**, the gate electrode of each transistor and the first electrode plate of each capacitor are arranged on the first gate metal layer, the second electrode plate of each capacitor is arranged on the second gate metal layer, and the active layer of each transistor is arranged on the semiconductor layer.
(192) As shown in FIG. **11**-FIG. **17**, the second start signal line RSTV, the second first clock signal line RCK, the second second clock signal line RCB and the second second voltage line VGH_R are all arranged on the second metal layer;
(193) The third first voltage line VGL_R is arranged on the third metal layer.
(194) In at least one embodiment of the present disclosure, when VGL_R is arranged on the third metal layer, VGL_N**1** can be arranged on the second metal layer, and the orthographic projection of VGL_R on the base substrate at least partially overlaps the orthographic projection of VGL_N**1** on the base substrate, to reduce the width of the display substrate in the horizontal direction, which is beneficial to realize narrow frame.
(195) In specific implementation, VGL_R can also be arranged on the second metal layer, and at this time, VGL_N**1** can be arranged on the third metal layer.
(196) As shown in FIGS. **11-17**, the orthographic projection of the third first voltage line VGL_R on the base substrate is set at a side of the orthographic projection of the gate electrode G**19** of the second driving transistor T**19** on the base substrate away from the display area, so that VGL_R and VGL_N**1** overlap each other.
(197) Optionally, the second output sub-circuit further includes a second driving reset transistor;
(198) The orthographic projection of the second start signal line on the base substrate at least partially overlaps the orthographic projection of the first electrode of the second driving transistor on the base substrate, and the orthographic projection of the second start signal line on the base substrate at least partially overlaps the orthographic projection of the second electrode of the second driving transistor on the base substrate;
(199) The orthographic projection of the second start signal line on the base substrate at least partially overlaps the orthographic projection of the first electrode of the second driving reset transistor on the base substrate, and the orthographic projection of the second start signal line on the base substrate at least partially overlaps the orthographic projection of the second electrode of the second driving reset transistor on the base substrate.
(200) As shown in FIGS. **11-17**, the orthographic projection of the second start signal line RSTV on the base substrate partially overlaps the orthographic projection of the first electrode S**19** of the second driving transistor T**19** on the base substrate, and the orthographic projection of the second start signal line RSTV on the base substrate partially overlaps the orthographic projection of the second electrode D**19** of the second driving transistor T**19** on the base substrate, and the orthographic projection of the second start signal line RSTV on the base substrate partially overlaps the orthographic projection of the first electrode S**18** of the second driving reset transistor T**18** on the base substrate, and the orthographic projection of the second start signal line RSTV on the base substrate partially overlaps the orthographic projection of the second electrode D**18** of the second driving reset transistor T**18** on the base substrate, to reduce the width of the display substrate along the first direction, which is beneficial to realize narrow frame.

(201) Optionally, the second driving circuit further includes a fifteenth transistor, a twentieth transistor, and a twenty-first transistor;
(202) The gate electrode of the fifteenth transistor is electrically connected to the second first clock signal line, and the second electrode of the fifteenth transistor is electrically connected to the second electrode of the twenty-first transistor; the first electrode of the twenty-first transistor is electrically connected to the second electrode of the twentieth transistor;
(203) The gate electrode of the twentieth transistor is electrically connected to the gate electrode of the second driving reset transistor, and the gate electrode of the twenty-first transistor is electrically connected to the second second clock signal line;
(204) The orthographic projection of the gate electrode of the fifteenth transistor on the base substrate, the orthographic projection of the gate electrode of the twentieth transistor on the base substrate, and the orthographic projection of the gate electrode of the twenty-first transistor on the base substrate are arranged between the orthographic projection of the second second clock signal line on the base substrate and the orthographic projection of the second second voltage line on the base substrate.
(205) Optionally, the second driving circuit further includes a sixteenth transistor;
(206) The gate electrode of the sixteenth transistor is electrically connected to the second electrode of the fifteenth transistor, the first electrode of the sixteenth transistor is electrically connected to the second first clock signal line, and the second electrode of the sixteenth transistor is electrically connected to the gate electrode of the driving reset transistor;
(207) The orthographic projection of the gate electrode of the sixteenth transistor on the base substrate is arranged between the orthographic projection of the second first clock signal line on the base substrate and the orthographic projection of the second second clock signal line on the base substrate.
(208) As shown in FIGS. **11**-**17**, the orthographic projection of the gate electrode G**15** of T**15** on the base substrate, the orthographic projection of the gate electrode G**20** of T**20** on the base substrate, and the orthographic projection of the gate electrode G**21** of T**21** on the base substrate are arranged in sequence along the vertical direction;
(209) The orthographic projection of G**15** on the base substrate, the orthographic projection of G**20** on the base substrate and the orthographic projection of G**21** on the base substrate can all arranged between the orthographic projection of the second second clock signal line RCB on the base substrate and the orthographic projection of the second second voltage line VGH_R on the base substrate, to reduce the width of the display substrate in the horizontal direction, which is beneficial to realize a narrow frame.
(210) As shown in FIGS. **11**-**17**, the orthographic projection of the gate electrode G**16** of T**16** on the base substrate is arranged between the orthographic projection of the second first clock signal line RCK on the base substrate and the orthographic projections of the second second clock signal line RCB on the base substrate, to reduce the width of the display substrate in the horizontal direction, which facilitates the realization of a narrow frame.
(211) As shown in FIGS. **11**-**17**, the orthographic projection of the gate electrode G**22** of T**22** on the base substrate is set within the orthographic projection of the second first clock signal line RCK on the base substrate, and the orthographic projection of the gate electrode G**17** of T**17** on the base substrate is set within the orthographic projection of the second second clock signal line RCB on the base substrate;
(212) The orthographic projection of the first electrode plate C**4***a* of the fourth capacitor C**4** on the base substrate partially overlaps the orthographic projection of the second first clock signal line RCK on the base substrate, and the orthographic projection of the second electrode plate C**4***b* of the fourth capacitor C**4** on the base substrate partially overlaps the orthographic projection of the second first clock signal line RCK on the base substrate.
(213) In at least one embodiment of the present disclosure, the orthographic projection of the

transistor included in the second driving circuit on the base substrate is set at a side of the orthographic projection of the third first voltage line on the base substrate close to the display area.
(214) As shown in FIGS. **11**-**17**, the orthographic projection of the gate electrode G**15** of T**15** on the base substrate, the orthographic projection of the gate electrode G**16** of T**16** on the base substrate, the orthographic projection of the gate electrode G**17** of T**17** on the base substrate, the orthographic projection of gate electrode G**18** of T**18** on the base substrate, the orthographic projection of gate electrode G**19** of T**19** on the base substrate, the orthographic projection of the gate electrode G**20** of T**20** on the base substrate, the orthographic projection of the gate electrode G**21** of T**21** on the base substrate and the orthographic projection of the gate electrode G**22** of T**22** on the base substrate are all arranged at a side of the orthographic projection of the third first voltage line VGL_R on the base substrate close to the display area.
(215) As shown in FIG. **18**A, the orthographic projection of the third first voltage line VGL_R on the base substrate overlaps the orthographic projection of VGL_N**1** on the base substrate; VGL_N**1** is arranged on the second metal layer, and VGL_R is arranged on the third metal layer.
(216) FIG. **18**B is a cross-sectional view of A-A′ in FIG. **18**A.
(217) In FIG. **18**B, the reference number **180** is the base substrate, the reference number **181** is the semiconductor layer, the reference number **182** is the first insulating layer, the reference number **183** is the first gate metal layer, and the reference number **184** is the second insulating layer, the reference number **185** is the third insulating layer, the reference number **186** is the first metal layer, the reference number **187** is the fourth insulation layer, the reference number **188** is the second metal layer, and the reference number **189** is the fifth insulating layer, the reference number **810** is the third metal layer.
(218) FIG. **18**C is a layout diagram of the second metal layer in FIG. **18**A, and FIG. **18**D is a layout diagram of the third metal layer in **18**A.
(219) In at least one embodiment of the present disclosure, T**9**, T**10**, VGL_R overlap VGL_N**1**, so VGL_N**1** has a shielding effect, which can reduce the parasitic capacitance between T**9** and VGL_N**1**, and reduce the parasitic capacitance between T**10** and VGL_N**1**. VGL_N**1** and VGL_R are DC voltage lines, and the overlapping arrangement has little influence thereon.
(220) As shown in FIG. **12**, the one labeled A**18** is the active layer of T**18**, and the one labeled A**19** is the active layer of T**19**;
(221) The one labeled S**15** is the first electrode of T**15**, the one labeled D**15** is the second electrode of T**15**; the one labeled S**16** is the first electrode of T**16**, and the one labeled D**16** is the second electrode of T**16**; the one labeled S**17** is the first electrode of T**17**, the one labeled D**17** is the second electrode of T**17**; the one labeled S**20** is the first electrode of T**20**, the one labeled D**20** is the second electrode of T**20**; the one labeled S**21** is the first electrode of T**21**, the one labeled D**21** is the second electrode of T**21**; the one labeled S**22** is the first electrode of T**22**, and the one labeled D**22** is the second electrode of T**22**.
(222) As shown in FIG. **13**, the one labeled G**15** is the gate electrode of T**15**, the one labeled G**16** is the gate electrode of T**16**, the one labeled G**17** is the gate electrode of T**17**, the one labeled G**18** is the gate electrode of T**18**, and the one labeled G**19** is the gate electrode of T**19**, the one labeled G**20** is the gate electrode of T**20**, the one labeled G**21** is the gate electrode of T**21**, and the gate labeled G**22** is the gate electrode of T**22**;
(223) The one labeled C**4***a* is the first electrode plate of C**4**, and the one labeled C**5***a* is the first electrode plate of C**5**.
(224) As shown in FIG. **14**, the one labeled C**4***b* is the second electrode plate of C**4**, and the one labeled C**5***b* is the second electrode plate of C**5**.
(225) As shown in FIG. **15**, the one labeled S**18** is the first electrode of T**18**, the one labeled D**18** is the second electrode of T**18**; the one labeled S**19** is the first electrode of T**19**, and the one labeled D**19** is the second electrode of T**19**.
(226) Optionally, the base substrate includes a peripheral area and a display area; the driving units

included in the driving module are all arranged in the peripheral area of the base substrate;
(227) The first driving unit is arranged on a side of the second driving unit away from the display area.
(228) As shown in FIG. **19**, the base substrate includes a peripheral area B**0** and a display area A**0**;
(229) Both the first driving unit GA**1** and the second driving unit GA**2** are arranged in the peripheral area B**0**;
(230) The first driving unit GA**1** is arranged on a side of the second driving unit GA**2** away from the display area A**0**.
(231) FIG. **20** is another layout diagram corresponding to the second driving circuit shown in FIG. **10**.
(232) FIG. **21** is a layout diagram of the semiconductor layer in FIG. **20**, FIG. **22** is a layout diagram of the first gate metal layer in FIG. **20**, FIG. **23** is a layout diagram of the second gate metal layer in FIG. **20**, FIG. **24** is a layout diagram of the first metal layer in FIG. **22**, FIG. **25** is the layout diagram of the second metal layer in FIG. **22**.
(233) In FIG. **21**, the one labeled A**18** is the active layer of T**18**, and the one labeled A**19** is the active layer of T**19**;
(234) The one labeled S**15** is the first electrode of T**15**, the one labeled D**15** is the second electrode of T**15**; the one labeled S**16** is the first electrode of T**16**, and the one labeled D**16** is the second electrode of T**16**; the one labeled S**17** is the first electrode of T**17**, the one labeled D**17** is the second electrode of T**17**; the one labeled S**20** is the first electrode of T**20**, the one labeled D**20** is the second electrode of T**20**; the one labeled S**21** is the first electrode of T**21**, the one labeled D**21** is the second electrode of T**21**; the one labeled S**22** is the first electrode of T**22**, and the one labeled D**22** is the second electrode of T**22**.
(235) As shown in FIG. **22**, the one labeled G**15** is the gate electrode of T**15**, the one labeled G**16** is the gate electrode of T**16**, the one labeled G**17** is the gate electrode of T**17**, the one labeled G**18** is the gate electrode of T**18**, and the one labeled G**19** is the gate electrode of T**19**, the one labeled G**20** is the gate electrode of T**20**, the one labeled G**21** is the gate electrode of T**21**, and the one labeled G**22** is the gate electrode of T**22**;
(236) The one labeled C**4***a* is the first electrode plate of C**4**, and the one labeled C**5***a* is the first electrode plate of C**5**.
(237) As shown in FIG. **23**, the one labeled C**4***b* is the second electrode plate of C**4**, and the one labeled C**5***b* is the second electrode plate of C**5**.
(238) As shown in FIG. **24**, the one labeled S**18** is the first electrode of T**18**, the one labeled D**18** is the second electrode of T**18**; the one labeled S**19** is the first electrode of T**19**, and the one labeled D**19** is the second electrode of T**19**, the one labeled VGL_R is the third first voltage line VGL_R.
(239) In FIG. **25**, the one labeled VGH_R is the second second voltage line, the one labeled RCB is the second second clock signal line, the one labeled RCK is the second first clock signal line, and the one labeled RSTV is the second starting signal line.
(240) As shown in FIG. **20**-FIG. **25**, VGH_R, RCB, VGL_R, RCK and RSTV are arranged in sequence along the direction close to the display area.
(241) FIG. **26** is a schematic diagram of arrangement relationship between the first driving circuit shown in FIG. **3** and the second driving circuit shown in FIG. **20**.
(242) In at least one embodiment of the present disclosure, the driving module includes a third driving unit, the third driving unit includes a plurality of stages of third driving circuit, and the third driving circuit is configured to provide a third driving signal;
(243) The third driving unit is arranged on a side of the first driving unit away from the second driving unit.
(244) In a specific implementation, the driving module may further include a third driving unit, the third driving circuit included in the third driving unit is configured to provide a third driving signal, and the third driving unit may be arranged at a side of the first driving unit far away from the

second driving unit.
(245) Optionally, the third driving signal may be a light emitting control signal, but not limited thereto.
(246) As shown in FIG. **27**A, the third driving circuit includes a third output sub-circuit;
(247) The third output sub-circuit includes a third driving transistor T**31** and a third driving reset transistor T**32**;
(248) The third driving circuit further includes a twenty-third transistor T**23**, a twenty-fourth transistor T**24**, a twenty-fifth transistor T**25**, a twenty-sixth transistor T**26**, a twenty-seventh transistor T**27**, a twenty-eighth transistor T**28**, a twenty-ninth transistor T**29**, a thirtieth transistor T**30**, a thirty-third transistor T**33**, a thirty-fourth transistor T**34**, a third on-off control transistor T**35**, a fourth on-off control transistor T**36**, a sixth capacitor C**6**, a seventh capacitor C**7** and an eighth capacitor C**8**;
(249) The gate electrode of T**23** is electrically connected to the third second clock signal line ECB, the first electrode of T**23** is electrically connected to the third input terminal I**3**, and the second electrode of T**23** is electrically connected to the gate electrode G**24** of T**24**;
(250) The first electrode of T**24** is electrically connected to the third second clock signal line ECB, and the second electrode of T**24** is electrically connected to the second electrode D**25** of T**25**;
(251) The gate electrode of T**25** is electrically connected to the third second clock signal line ECB, and the first electrode of T**25** is electrically connected to the fifth first voltage line VGL_E**2**;
(252) The gate electrode of T**26** is electrically connected to the gate electrode of T**27**, the first electrode of T**26** is electrically connected to the third first clock signal line ECK, the second electrode of T**26** is electrically connected to the first electrode plate C**8***a* of C**8**; the second electrode plate of C**8** is electrically connected to the gate electrode of T**27**;
(253) The gate electrode of T**27** is electrically connected to the first electrode of T**27**, and the second electrode of T**27** is electrically connected to the gate electrode of T**32**;
(254) The gate electrode of T**28** is electrically connected to the first electrode plate of C**6**, the first electrode of T**28** is electrically connected to the third first clock signal line ECK, and the second electrode of T**28** is electrically connected to the second electrode plate of C**6**;
(255) The gate electrode of T**29** is electrically connected to the third first clock signal line ECK, the first electrode of T**29** is electrically connected to the second electrode plate of C**6**, and the second electrode of T**29** is electrically connected to the gate electrode of T**31**;
(256) The gate electrode of T**30** is electrically connected to the gate electrode of T**24**, the first electrode of T**30** is electrically connected to the third second voltage line VGH_E, and the second electrode of T**30** is electrically connected to the gate electrode G**31** of T**31**;
(257) The first electrode of T**31** is electrically connected to the third second voltage line VGH_E, and the second electrode of T**31** is electrically connected to the third driving signal output terminal O**3**;
(258) The first electrode of T**32** is electrically connected to the third driving signal output terminal O**3**, and the second electrode of T**32** is electrically connected to the fourth first voltage line VGL_E**1**;
(259) The gate electrode of T**33** is electrically connected to the second electrode of T**28**, the first electrode of T**33** is electrically connected to the third second voltage line VGH_E, and the second electrode of T**33** is electrically connected to the gate electrode of T**32**;
(260) The gate electrode of T**34** is electrically connected to the third reset line RST_, the first electrode of T**34** is electrically connected to the third second voltage line VGH_E, and the second electrode of T**34** is electrically connected to the gate electrode of T**32**;
(261) The gate electrode of T**35** is electrically connected to the fifth first voltage line VGL_E**2**, the first electrode of T**35** is electrically connected to the gate electrode of T**24**, and the second electrode of T**35** is electrically connected to the gate electrode of T**26**;
(262) The gate electrode of T**36** is electrically connected to the fifth first voltage line VGL_E**2**, the

first electrode of T**36** is electrically connected to the second electrode of T**24**, and the second electrode of T**36** is electrically connected to the gate electrode of T**28**;
(263) The first electrode plate of C**7** is electrically connected to the gate electrode of T**31**, and the second electrode plate of C**7** is electrically connected to the third second voltage line VGH_E.
(264) As shown in FIG. **27**B, the third driving circuit includes a third output sub-circuit;
(265) The third output sub-circuit includes a third driving transistor T**31** and a third driving reset transistor T**32**;
(266) The third driving circuit further includes a twenty-third transistor T**23**, a twenty-fourth transistor T**24**, a twenty-fifth transistor T**25**, a twenty-sixth transistor T**26**, a twenty-seventh transistor T**27**, a twenty-eighth transistor T**28**, a twenty-ninth transistor T**29**, a thirtieth transistor T**30**, a thirty-third transistor T**33**, a thirty-fourth transistor T**34**, a third on-off control transistor T**35**, a fourth on-off control transistor T**36**, a sixth capacitor C**6**, a seventh capacitor C**7** and an eighth capacitor C**8**;
(267) The gate electrode G**23** of T**23** is electrically connected to the third second clock signal line ECB, the first electrode S**23** of T**23** is electrically connected to the third input terminal I**3**, and the second electrode D**23** of T**23** is electrically connected to the gate electrode G**24** of T**24**;
(268) The first electrode S**24** of T**24** is electrically connected to the third second clock signal lines ECB, and the second electrode D**24** of T**24** is electrically connected to the second electrode D**25** of T**25**;
(269) The gate electrode G**25** of T**25** is electrically connected to the third second clock signal line ECB, and the first electrode S**25** of T**25** is electrically connected to the fifth first voltage line VGL_E**2**;
(270) The gate electrode G**26** of T**26** is electrically connected to the gate electrode G**27** of T**27**, the first electrode S**26** of T**26** is electrically connected to the third first clock signal line ECK, and the second electrode D**26** of T**26** is electrically connected to the first electrode plate C**8***a* of C**8**; the second electrode plate C**8***b* of C**8** is electrically connected to the gate electrode G**27** of T**27**;
(271) The gate electrode G**27** of T**27** is electrically connected to the first electrode S**27** of T**27**, and the second electrode D**27** of T**27** is electrically connected to the gate electrode G**32** of T**32**;
(272) The gate electrode G**28** of T**28** is electrically connected to the first electrode plate C**6***a* of C**6**, the first electrode S**28** of T**28** is electrically connected to the third first clock signal line ECK, the second electrode D**28** of T**28** is electrically connected to the second electrode plate C**6***b* of C**6**;
(273) The gate electrode G**29** of T**29** is electrically connected to the third first clock signal line ECK, the first electrode S**29** of T**29** is electrically connected to the second electrode plate C**6***b* of C**6**, and the second electrode D**29** of T**29** is electrically connected to the gate electrode G**31** of T**31**;
(274) The gate electrode G**30** of T**30** is electrically connected to the gate electrode G**24** of T**24**, the first electrode S**30** of T**30** is electrically connected to the third second voltage line VGH_E, and the second electrode D**30** of T**30** is electrically connected to the gate electrode G**31** of T**31**;
(275) The first electrode S**31** of T**31** is electrically connected to the third second voltage line VGH_E, and the second electrode D**31** of T**31** is electrically connected to the third driving signal output terminal O**3**;
(276) The first electrode S**32** of T**32** is electrically connected to the third driving signal output terminal O**3**, and the second electrode D**32** of T**32** is electrically connected to the fourth first voltage line VGL_E**1**;
(277) The gate electrode G**33** of T**33** is electrically connected to the second electrode D**28** of T**28**, the first electrode S**33** of T**33** is electrically connected to the third second voltage line VGH_E, and the second electrode D**33** of T**33** is electrically connected to the gate electrode G**32** of T**32**;
(278) The gate electrode G**34** of T**34** is electrically connected to the third reset line RST_E, the first electrode S**34** of T**34** is electrically connected to the third second voltage line VGH_E, and the second electrode D**34** of T**34** is electrically connected to the gate electrode G**32** of T**32**;
(279) The gate electrode G**35** of T**35** is electrically connected to the fifth first voltage line

VGL_E**2**, the first electrode S**35** of T**35** is electrically connected to the gate electrode G**24** of T**24**, and the second electrode D**35** of T**35** is electrically connected to the gate electrode G**26** of T**26**;
(280) The gate electrode G**36** of T**36** is electrically connected to the fifth first voltage line VGL_E**2**, the first electrode S**36** of T**36** is electrically connected to the second electrode D**24** of T**24**, and the second electrode D**36** of T**36** is electrically connected to the gate electrode G**28** of T**28**;
(281) The first electrode plate C**7***a* of C**7** is electrically connected to the gate electrode G**31** of T**31**, and the second electrode plate C**7***b* of C**7** is electrically connected to the third second voltage line VGH_E.
(282) In at least one embodiment of the third driving circuit shown in FIG. **27**A and FIG. **27**B, all transistors are P-type transistors, but not limited thereto.
(283) FIG. **28** is a layout diagram corresponding to the third driving circuit shown in FIG. **27**B, FIG. **29** is a layout diagram of the semiconductor layer in FIG. **28**, and FIG. **30** is a layout diagram of the first gate metal layer in FIG. **28**, FIG. **31** is a layout diagram of the second gate metal layer in FIG. **28**, and FIG. **32** is a layout diagram of the first metal layer in FIG. **28**.
(284) As shown in FIGS. **28-32**, the first electrode plate of each capacitor and the gate electrode of each transistor are arranged on the first gate metal layer, the second electrode plate of each capacitor is arranged on the second gate metal layer, and the active layer of each transistor is arranged on the semiconductor layer.
(285) In FIG. **28** and FIG. **32**, the one labeled ESTV is the third start signal line, the one labeled ECK is the third first clock signal line, and the one labeled ECB is the third second clock signal line, the one labeled RST_E is the third reset line, the one labeled VGH_E is the third second voltage line, the one labeled VGL_E**1** is the fourth first voltage line, and the one labeled VGL_E**2** is the fifth first voltage line.
(286) As shown in FIG. **32**, ESTV, ECK, ECB, RST_E, VGH_E, VGL_E**1** and VGL_E**2** are all arranged on the first metal layer.
(287) In at least one embodiment of the third driving circuit corresponding to FIGS. **28-32**, T**33** and T**34** are double-gate transistors, but not limited thereto.
(288) In FIG. **29**, the one labeled A**31** is the active layer of T**31**, the one labeled A**32** is the active layer of T**32**, the one labeled S**23** is the first electrode of T**23**, and the one labeled D**23** is the second electrode of T**23**; the one labeled S**24** is the first electrode of T**24**, the one labeled D**24** is the second electrode of T**24**; the one labeled S**25** is the first electrode of T**25**, the one labeled D**25** is the second electrode of T**25**; the one labeled S**26** is the first electrode of T**26**, the one labeled D**26** is the second electrode of T**26**; the one labeled S**27** is the first electrode of T**27**, and the one labeled D**27** is the second electrode of T**27**; the one labeled S**28** is the first electrode of T**28**, the one labeled D**28** is the second electrode of T**28**; the one labeled S**29** is the first electrode of T**29**, the one labeled D**29** is the second electrode of T**29**; the one labeled S**30** is the first electrode of T**30**, and the one labeled D**30** is the second electrode of T**30**; the one labeled S**33** is the first electrode of T**33**, the one labeled D**33** is the second electrode of T**33**; the one labeled S**34** is the first electrode of T**34**, the one labeled D**34** is the second electrode of T**34**; the one labeled S**35** is the first electrode of T**35**, the one labeled D**35** is the second electrode of T**35**; the one labeled S**36** is the first electrode of T**36**, and the one labeled D**36** is the second electrode of T**36**.
(289) In FIG. **30**, the one labeled G**23** is the gate electrode of T**23**, the one labeled G**24** is the gate electrode of T**24**, the one labeled G**25** is the gate electrode of T**25**, the one labeled G**26** is the gate electrode of T**26**, and the one labeled G**27** is the gate electrode of T**27**, the one labeled G**28** is the gate electrode of T**28**, the one labeled G**29** is the gate electrode of T**29**, the one labeled G**30** is the gate electrode of T**30**, the one labeled G**31** is the gate electrode of T**31**, and the one labeled G**32** is the gate electrode of T**32**, the one labeled G**33** is the gate electrode of T**33**, the one labeled G**34** is the gate electrode of T**34**, the one labeled G**35** is the gate electrode of T**35**, the one labeled G**36** is the gate electrode of T**36**, and the one labeled C**6***a* is the first electrode plate of C**6**, the one labeled

C**7***a* is the first electrode plate of C**7**, and the one labeled C**8***a* is the first electrode plate of C**8**.
(290) In FIG. **31**, the one labeled C**6***b* is the second electrode plate of C**6**, the one labeled C**7***b* is the second electrode plate of C**7**, and the one labeled C**8***b* is the second electrode plate of C**8**.
(291) In at least one embodiment of the present disclosure, the driving module includes a fourth driving unit, the driving unit includes a plurality of stages of fourth driving circuit, the fourth driving circuit is used to provide a fourth driving signal, and the fourth driving signal is a P-type gate driving signal;
(292) The fourth driving unit is arranged on a side of the second driving unit close to the display area.
(293) In a specific implementation, the P-type gate driving signal may be provided to a P-type transistor included in the pixel circuit and have a high-level as the valid level, but it is not limited thereto.
(294) As shown in FIG. **33**A, the fourth driving circuit includes a fourth output sub-circuit, and the fourth output sub-circuit includes a fourth driving transistor T**42** and a fourth driving reset transistor T**41**;
(295) The fourth driving circuit further includes a thirty-seventh transistor T**37**, a thirty-eighth transistor T**38**, a thirty-ninth transistor T**39**, a fortieth transistor T**40**, a forty-third transistor T**43**, a forty-fourth transistors T**44**, a forty-fifth transistor T**45**, a forty-sixth transistor T**46**, a ninth capacitor C**9** and a tenth capacitor C**10**;
(296) The gate electrode of T**37** is electrically connected to the first clock signal terminal GCK**1**, the first electrode of T**37** is electrically connected to the fourth input terminal I**4**, and the second electrode of T**37** is electrically connected to the first electrode of T**38**;
(297) The gate electrode of T**38** is electrically connected to the gate electrode of T**37**, and the second electrode of T**38** is electrically connected to the gate electrode of T**42**;
(298) The gate electrode of T**39** is electrically connected to the third clock signal terminal GCK**3**, the first electrode of T**39** is electrically connected to the first voltage terminal VGL_G, and the second electrode of T**39** is electrically connected to the gate electrode G**41** of T**41**;
(299) The gate electrode of T**40** is electrically connected to the fourth input terminal I**4**, the first electrode of T**40** is electrically connected to the second voltage terminal VGH_G, and the second electrode of T**40** is electrically connected to the gate electrode G**41** of T**41**;
(300) The gate electrode of T**41** is electrically connected to the first electrode of C**10**, the first electrode of T**41** is electrically connected to the second voltage terminal VGH_G, and the second electrode of T**41** is electrically connected to the fourth driving signal output terminal O**4**;
(301) The gate electrode of T**42** is electrically connected to the first electrode of C**9**, the first electrode of T**42** is electrically connected to the fourth driving signal output terminal O**4**; the second electrode of T**42** is electrically connected to the second clock signal terminal GCK**2**;
(302) The gate electrode of T**43** is electrically connected to the gate electrode of T**41**, the first electrode of T**43** is electrically connected to the second voltage terminal VGH_G, and the second electrode of T**43** is electrically connected to the first electrode of T**44**;
(303) The gate electrode of T**44** is electrically connected to the second electrode of T**40**; the second electrode of T**44** is electrically connected to the gate electrode of T**42**;
(304) The gate electrode of T**45** is electrically connected to the fourth driving signal output terminal O**4**, the first electrode of T**45** is electrically connected to the second clock signal terminal GCK**2**, and the second electrode of T**45** is electrically connected to the second electrode D**37** of T**37**;
(305) The gate electrode of T**46** is electrically connected to the gate electrode of T**42**, the first electrode of T**46** is electrically connected to the second electrode of T**43**, and the second electrode of T**46** is electrically connected to the first voltage terminal VGL_G;
(306) The second electrode plate of C**9** is electrically connected to the fourth driving signal output terminal O**4**, and the second electrode plate of C**10** is electrically connected to the second voltage

terminal VGH_G.
(307) As shown in FIG. **33**B, at least one embodiment of the fourth driving circuit includes a fourth output sub-circuit, and the fourth output sub-circuit includes a fourth driving transistor T**42** and a fourth driving reset transistor T**41**;
(308) At least one embodiment of the fourth driving circuit further includes a thirty-seventh transistor T**37**, a thirty-eighth transistor T**38**, a thirty-ninth transistor T**39**, a fortieth transistor T**40**, a forty-third transistor T**43**, a forty-fourth transistor T**44**, a forty-fifth transistor T**45**, a forty-sixth transistor T**46**, a ninth capacitor C**9** and a tenth capacitor C**10**;
(309) The gate electrode G**37** of T**37** is electrically connected to the first clock signal terminal GCK**1**, the first electrode S**37** of T**37** is electrically connected to the fourth input terminal I**4**, and the second electrode D**37** of T**37** is electrically connected to the first electrode S**38** of T**38**;
(310) The gate electrode G**38** of T**38** is electrically connected to the gate electrode G**37** of T**37**, and the second electrode D**38** of T**38** is electrically connected to the gate electrode G**42** of T**42**;
(311) The gate electrode G**39** of T**39** is electrically connected to the third clock signal terminal GCK**3**, the first electrode S**39** of T**39** is electrically connected to the first voltage terminal VGL_G, and the second electrode D**39** of T**39** is electrically connected to the gate electrode G**41** of T**41**;
(312) The gate electrode G**40** of T**40** is electrically connected to the fourth input terminal I**4**, the first electrode S**40** of T**40** is electrically connected to the second voltage terminal VGH_G, and the second electrode D**40** of T**40** is electrically connected to the gate electrode G**41** of T**41**;
(313) The gate electrode G**41** of T**41** is electrically connected to the first electrode plate C**10***a* of C**10**, the first electrode S**41** of T**41** is electrically connected to the second voltage terminal VGH_G, and the second electrode D**41** of T**41** is electrically connected to the fourth driving signal output terminal O**4**;
(314) The gate electrode G**42** of T**42** is electrically connected to the first electrode plate C**9***a* of C**9**, the first electrode S**42** of T**42** is electrically connected to the fourth driving signal output terminal O**4**; the second electrode D**42** of T**42** is electrically connected to the second clock signal terminal GCK**2**;
(315) The gate electrode G**43** of T**43** is electrically connected to the gate electrode G**411** of T**41**, the first electrode S**43** of T**43** is electrically connected to the second voltage terminal VGH_G, and the second electrode D**43** of T**43** is electrically connected to the first electrode S**44** of T**44**;
(316) The gate electrode G**44** of T**44** is electrically connected to the second electrode D**40** of T**40**; the second electrode D**44** of T**44** is electrically connected to the gate electrode G**42** of T**42**;
(317) The gate electrode G**45** of T**45** is electrically connected to the fourth driving signal output terminal O**4**, the first electrode S**45** of T**45** is electrically connected to the second clock signal terminal GCK**2**, and the second electrode D**45** of T**45** is electrically connected to the second electrode D**37** of T**37**;
(318) The gate electrode G**46** of T**46** is electrically connected to the gate electrode G**42** of T**42**, the first electrode S**46** of T**46** is electrically connected to the second electrode D**43** of T**43**, and the second electrode D**46** of T**46** is electrically connected to the first voltage terminal VGL_G;
(319) The second electrode plate C**9***b* of C**9** is electrically connected to the fourth driving signal output terminal O**4**, and the second electrode plate C**10***b* of C**10** is electrically connected to the second voltage terminal VGH_G.
(320) In at least one embodiment of the fourth driving circuit shown in FIG. **33**A and FIG. **33**B, all transistors are P-type transistors, but not limited thereto.
(321) FIG. **34** is a layout diagram corresponding to the fourth driving circuit shown in FIG. **33**B. FIG. **35** is a layout diagram of the semiconductor layer in FIG. **34**, FIG. **36** is a layout diagram of the first gate metal layer in FIG. **34**, FIG. **37** is a layout diagram of the second gate metal layer in FIG. **34**, and FIG. **38** is a layout diagram of the first metal layer in FIG. **34**.
(322) On the basis of the layout diagram of FIG. **34**, the display substrate may further include a second metal layer. FIG. **39** is a layout diagram of the added second metal layer.

(323) In FIG. **35**, the one labeled A**41** is the active layer of T**41**, the one labeled A**42** is the active layer of T**42**, S**37** is the first electrode of T**37**, D**37** is the second electrode of T**37**, and S**38** is the first electrode of T**38**. D**38** is the second electrode of T**38**, S**39** is the first electrode of T**39**, D**39** is the second electrode of T**39**, S**40** is the first electrode of T**40**, D**40** is the second electrode of T**40**, S**43** is the first electrode of T**43**, D**43** is the second electrode of T**43**, S**44** is the first electrode of T**44**, D**44** is the second electrode of T**44**, S**45** is the first electrode of T**45**, D**45** is the second electrode of T**45**, S**46** is the first electrode of T**46**, D**46** is the second electrode of T**46**.
(324) In FIG. **36**, the one labeled G**37** is the gate electrode of T**37**, the one labeled G**38** is the gate electrode of T**38**, the one labeled G**39** is the gate electrode of T**39**, the one labeled G**40** is the gate electrode of T**40**, the one labeled G**41** is the gate electrode of T**41**, the one labeled G**42** is the gate electrode of T**42**, the one labeled G**43** is the gate electrode of T**43**, the one labeled G**44** is the gate electrode of T**44**, the one labeled G**45** is the gate electrode of T**45**, the one labeled G**45** is the gate electrode of T**45**; the one labeled C**9***a* is the first electrode plate of C**9**, and the one labeled C**10***a* is the first electrode plate of C**10**.
(325) In FIG. **38**, the one labeled C**9***b* is the second electrode plate of C**9**, and the one labeled C**10***b* is the second electrode plate of C**10**.
(326) In FIG. **38**, the one labeled S**41** is the source electrode of T**41**, the one labeled D**41** is the drain electrode of T**41**, the one labeled S**42** is the source electrode of T**42**, and the one labeled D**42** is the drain electrode of T**42**.
(327) In FIG. **34** to FIG. **38**, the one labeled GCK**1**_E**1** is the first clock signal line in the first even-numbered row, the one labeled GCK**2**_E**1** is the second clock signal line in the first even-numbered row, and the one labeled GCK**3**_E**1** is the third clock signal line in the first even-numbered row, the one labeled GSTV_P**1** is the first fourth start signal line, the one labeled VGL_P**1** is the first third voltage line, the one labeled GCK**1**_O**1** is the first clock signal line in the first odd-numbered row, and the one labeled GCK**2**_O**1** is the second clock signal line in the first odd-numbered row, the one labeled GCK**3**_O**1** is the third clock signal line in the first odd-numbered row; the one labeled VGH_P**1** is the first fourth voltage line;
(328) As shown in FIG. **39**, the one labeled GCK**1**_E**2** is the first clock signal line in the second even-numbered row, the one labeled GCK**2**_E**2** is the second clock signal line in the second even-numbered row, the one labeled GCK**3**_E**2** is the third clock signal line in the second even-numbered row, the one labeled GSTV_P**2** is the second fourth start signal line, the one labeled VGL_P**2** is the second third voltage line, the one labeled GCK**1**_O**2** is the first clock signal line in the second odd-numbered row, and the one labeled GCK**2**_O**2** is the second clock signal line in the second odd-numbered, the one labeled GCK**3**_O**2** is the third clock signal line in the second odd-numbered row; the one labeled VGH_P**2** is the second fourth voltage line.
(329) In the embodiment corresponding to FIG. **34**, in the fourth driving circuit, the first voltage terminal VGL_G is electrically connected to the first third voltage line VGL_P**1**, and the second voltage terminal VGH_G is electrically connected to the first fourth voltage line VGH_P**1**;
(330) In the fourth driving circuit in the even-numbered row, the first clock signal terminal GCK**1** is electrically connected to the first clock signal line GCK**1**_E**1** in the first even-numbered row, the second clock signal terminal GCK**2** is electrically connected to the second clock signal line GCK**2**_E**1** in the first even-numbered row, and the second clock signal terminal GCK**2** is electrically connected to the second clock signal line GCK**2**_E**1** in the first even-numbered row, the third clock signal terminal GCK**3** is electrically connected to the third clock signal line GCK**3**_E**1** in the first even-numbered row;
(331) In the fourth driving circuit in the odd-numbered row, the first clock signal terminal GCK**1** is electrically connected to the first clock signal line GCK**1**_O**1** in the first odd-numbered row, the second clock signal terminal GCK**2** is electrically connected to the second clock signal line GCK**2**_O**1** in the first odd-numbered row, and the second clock signal terminal GCK**2** is electrically connected to the second clock signal line GCK**2**_O**1** in the first odd-numbered row, the

third clock signal terminal GCK**3** is electrically connected to the third clock signal line GCK**3**_O**1** in the first odd-numbered row.
(332) In at least one embodiment of the present disclosure, the first clock signal line GCK**1**_E**2** in the second even-numbered row is electrically connected to the first clock signal line GCK**1**_E**1** in the first even-numbered row through a via hole, and the second clock signal line GCK**2**_E**2** in the second even-numbered row is electrically connected to the second clock signal line GCK**2**_E**1** in the first even-numbered row through the via hole, and the third clock signal line GCK**3**_E**2** in the second even-numbered row is electrically connected with the third clock signal line GCK**3**_E**1** in the first even-numbered row through the via hole to reduce the loading of each clock signal line;
(333) The first clock signal line GCK**1**_O**2** in the second odd-numbered row is electrically connected to the first clock signal line GCK**1**_O**1** in the first odd-numbered row through a via hole, and the second clock signal line GCK**2**_O**2** in the second odd-numbered row is connected to the second clock signal line GCK**2**_O**1** in the first odd-numbered row through a via hole, and the third clock signal line GCK**3**_O**2** in the second odd-numbered row is electrically connected with the third clock signal line GCK**3**_O**1** in the first odd-numbered row through the via hole to reduce the loading of each clock signal line;
(334) The second third voltage line VGL_P**2** is electrically connected to the first third voltage line VGL_P**1** through a via hole, so as to reduce the loading of the third voltage line;
(335) The second fourth voltage line VGH_P**2** is electrically connected to the first fourth voltage line VGH_P**1** through a via hole, so as to reduce the loading of the fourth voltage line;
(336) The second fourth start signal line GSTV_P**2** is electrically connected to the first fourth start signal line GSTV_P**1** through a via hole, so as to reduce the loading of each clock signal line.
(337) In at least one embodiment of the present disclosure, on the basis of the layout diagram in FIG. **34**, the display substrate may further include a second metal layer and a third metal layer, and the first clock signal line in the third even-numbered row, the second clock signal line in the third even-numbered row, the third clock signal line in the third even-numbered row, the first clock signal line in the third odd-numbered row, the second clock signal line in the third odd-numbered row, the third clock signal line in the third odd-numbered row and the third third voltage line and a third fourth voltage line may be provided on the third metal layer;
(338) The first clock signal line in the third even-numbered row is electrically connected to the first clock signal line in the second even-numbered row through a via hole; the second clock signal line in the third even-numbered row is electrically connected to the second clock signal line in the second even-numbered row through a via hole; the third clock signal line in the third even-numbered row is electrically connected to the third clock signal line in the second even-numbered row through a via hole; the first clock signal line in the third odd-numbered row is electrically connected to the first clock signal line in the second odd-numbered row through a via hole; the second clock signal line in the third odd-numbered row is electrically connected to the second clock signal line in the second odd-numbered row through a via hole; the third clock signal line in the third odd-numbered row is electrically connected to the third clock signal line in the second odd-numbered row through a via hole; to reduce the loading of each clock signal line.
(339) The third third voltage line is electrically connected to the second third voltage line through a via hole, so as to reduce the loading of the third voltage line;
(340) The third fourth voltage line is electrically connected to the second fourth voltage line through the via hole, so as to reduce the loading of the fourth voltage line.
(341) In at least one embodiment of the present disclosure, each third voltage line may be a low-voltage DC signal line, and each fourth voltage line may be a high-voltage DC signal line, but not limited thereto.
(342) In at least one embodiment of the present disclosure, the orthographic projection of the first clock signal lines GCK**1**_E**2** in the second even-numbered row on the base substrate at least partially overlaps the orthographic projection of the first clock signal line GCK**1**_E**1** in the first

even-numbered row on the base substrate, the orthographic projection of the second clock signal line GCK**2**_E**2** in the second even-numbered row on the base substrate at least partially overlaps the orthographic projection of the second clock signal line GCK**2**_E**1** in the first even-numbered row on the base substrate, and the orthographic projection of third clock signal line GCK**3**_E**2** in the second even-numbered row on the base substrate at least partially overlaps the orthographic projection of the third clock signal line GCK**3**_E**1** in the first even-numbered row on the base substrate;

(343) The orthographic projection of the first clock signal line GCK**1**_O**2** in the second odd-numbered row on the base substrate at least partially overlaps the orthographic projection of the first clock signal line GCK**1**_O**1** in the first odd-numbered row on the base substrate, and the orthographic projection of the second clock signal line GCK**2**_O**2** in second odd-numbered row on the base substrate at least partially overlaps the orthographic projection of the second clock signal line GCK**2**_O**1** in the first odd-numbered row on the base substrate, and the orthographic projection of the third clock signal line GCK**3**_O**2** in the second odd-numbered row on the base substrate at least partially overlaps the orthographic projection of the third clock signal line GCK**3**_O**1** in the first odd-numbered row on the base substrate;

(344) The orthographic projection of the second third voltage line VGL_P**2** on the base substrate at least partially overlaps the orthographic projection of the first third voltage line VGL_P**1** on the base substrate;

(345) The orthographic projection of the second fourth voltage line VGH_P**2** on the base substrate at least partially overlaps the orthographic projection of the first fourth voltage line VGH_P**1** on the base substrate;

(346) The orthographic projection of the second fourth start signal line GSTV_P**2** on the base substrate at least partially overlaps the orthographic projection of the first fourth start signal line GSTV_P**1** on the base substrate.

(347) As shown in FIG. **40**, the base substrate includes a peripheral area B**0** and a display area A**0**;

(348) The first driving unit GA**1**, the second driving unit GA**2**, the third driving unit GA**3** and the fourth driving unit GA**4** are all arranged in the peripheral area B**0**;

(349) The third driving unit GA**3**, the first driving unit GA**1**, the second driving unit GA**2** and the fourth driving unit GA**4** are arranged in sequence along a direction close to the display area A**0**.

(350) As shown in FIG. **41**, the first driving unit GA**1** includes a first second voltage line VGH_N, and the second driving unit GA**2** includes a second second voltage line VGH_R;

(351) the orthographic projection of VGH_N on the base substrate at least partially overlaps an orthographic projection of VGH_R on the base substrate;

(352) VGH_N can be arranged on the second metal layer, and VGH_R can be arranged on the third metal layer, but not limited thereto.

(353) In at least one embodiment of the present disclosure, the first signal line is VGH_N, and the second signal line is VGH_R, but not limited thereto.

(354) In at least one embodiment shown in FIG. **41**, both VGH_N and VGH_R may be configured to provide high-voltage DC signals, and VGH_N and VGH_R are arranged on different metal layers. As shown in FIG. **42**, the first driving unit GA**1** includes a first second clock signal line NCB, and the second driving unit GA**2** includes a second second clock signal line RCB;

(355) an orthographic projection of the NCB on the base substrate at least partially overlaps an orthographic projection of the RCB on the base substrate;

(356) NCB can be arranged on the second metal layer, and RCB can be arranged on the third metal layer, but not limited thereto.

(357) In at least one embodiment shown in FIG. **42**, the NCB can be configured to provide a clock signal, and the RCB can be configured to provide a clock signal, and the NCB and RCB are arranged on different metal layers.

(358) In at least one embodiment of the present disclosure, the first signal line is NCB, and the

second signal line is RCB, but not limited thereto.
(359) As shown in FIG. **43**, the first driving unit GA**1** includes a second first voltage line VGL_N**1**, and the third driving unit GA**3** includes a third second voltage line VGH_E;
(360) the orthographic projection of VGL_R on the base substrate at least partially overlaps the orthographic projection of VGH_E on the base substrate;
(361) VGL_N**1** can be arranged on the second metal layer, and VGH_E can be arranged on the third metal layer.
(362) In at least one embodiment shown in FIG. **43**, VGL_N**1** can be configured as a low-voltage DC signal, VGH_E can be configured as a high-voltage DC signal, and VGL_N**1** and VGH_E are arranged on different metal layers.
(363) In at least one embodiment of the present disclosure, the first signal line is VGL_N**1**, and the second signal line is VGH_E, but not limited thereto.
(364) The display device described in the embodiment of the present disclosure includes the above-mentioned display substrate.
(365) The display device provided by the embodiments of the present disclosure may be any product or component with a display function, such as a mobile phone, a tablet computer, a television, a monitor, a notebook computer, a digital photo frame, a navigator, and the like.
(366) The above embodiments are for illustrative purposes only, but the present disclosure is not limited thereto. Obviously, a person skilled in the art may make further modifications and improvements without departing from the spirit of the present disclosure, and these modifications and improvements shall also fall within the scope of the present disclosure.

Claims

1. A display substrate, comprising a driving module arranged on a base substrate, wherein the driving module includes a plurality of driving units, and the driving unit includes a plurality of stages of driving circuit; the driving circuit is used to provide a driving signal; the driving unit includes a first signal line, and the driving circuit includes an output sub-circuit configured to output the driving signal; the display substrate includes at least two metal layers stacked along a direction away from the base substrate; in at least one driving unit, an orthographic projection of the first signal line on the base substrate at least partially overlaps an orthographic projection of a first electrode of at least one transistor included in the output sub-circuit on the base substrate, the orthographic projection of the first signal line on the base substrate at least partially overlaps an orthographic projection of a second electrode of the at least one transistor included in the output sub-circuit on the base substrate; the first electrode and the second electrode are arranged on a same metal layer, and the first electrode and the first signal line are arranged on different metal layers; wherein the driving module includes a first driving unit; the first driving unit includes a plurality of stages of first driving circuits, and the first driving circuit is used to provide a first driving signal; the first driving unit includes a first first voltage line and a first second voltage line; the first driving circuit includes a first output sub-circuit; the first signal line is the first first voltage line; the first output sub-circuit includes a first driving transistor and a first driving reset transistor; a first electrode of the first driving transistor is electrically connected to the first second voltage line, a second electrode of the first driving transistor is electrically connected to a first electrode of the first driving reset transistor, and a second electrode of the first driving reset transistor is electrically connected to the first first voltage line; the display substrate includes a first metal layer and a second metal layer sequentially stacked along a direction away from the base substrate; the first electrode of the first driving transistor, the second electrode of the first driving transistor, the first electrode of the first driving reset transistor and the second electrode of the first driving reset transistor are both arranged on the first metal layer, and the first first voltage line is arranged on the second metal layer; an orthographic projection of the first electrode of the first driving transistor on

the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate; an orthographic projection of the second electrode of the first driving transistor on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate; an orthographic projection of the first electrode of the first driving reset transistor on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate; an orthographic projection of the second electrode of the first driving reset transistor on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate.

2. The display substrate according to claim 1, wherein an orthographic projection of a first signal line included in one driving circuit of the plurality of driving units on the base substrate at least partially overlaps an orthographic projection of a second signal line included in another driving unit of the plurality of driving units on the base substrate.

3. The display substrate according to claim 2, wherein the first signal line and the second signal line are configured to provide a same signal.

4. The display substrate according to claim 2, wherein the first signal line is a low voltage DC signal line, a high voltage DC signal line or a clock signal line; the second signal line is a low voltage DC signal line, a high voltage DC signal line or a clock signal line.

5. The display substrate according to claim 1, wherein among the plurality of driving units, orthographic projections of at least three signal lines on the base substrate at least partially overlap.

6. The display substrate according to claim 1, wherein the driving module includes a first driving unit; the first driving unit includes a plurality of stages of first driving circuits, and the first driving circuit is used to provide a first driving signal; the first driving unit includes a first first voltage line and a first second voltage line; the first driving circuit includes a first output sub-circuit; the first signal line is the first first voltage line; the first output sub-circuit includes a first driving transistor and a first driving reset transistor; a first electrode of the first driving transistor is electrically connected to the first second voltage line, a second electrode of the first driving transistor is electrically connected to a first electrode of the first driving reset transistor, and a second electrode of the first driving reset transistor is electrically connected to the first first voltage line; the display substrate includes a first metal layer, a second metal layer and a third metal layer which are sequentially stacked along a direction away from the base substrate; the first electrode of the first driving transistor, the second electrode of the first driving transistor, the first electrode of the first driving reset transistor, and the second electrode of the first driving reset transistor are all arranged on the first metal layer, and the first first voltage line is arranged on the third metal layer; an orthographic projection of the first electrode of the first driving transistor on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate; an orthographic projection of the second electrode of the first driving transistor on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate; an orthographic projection of the first electrode of the first driving reset transistor on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate; an orthographic projection of the second electrode of the first driving reset transistor on the base substrate at least partially overlaps with the orthographic projection of the first first voltage line on the base substrate.

7. The display substrate according to claim 1, wherein the first driving unit further includes a second first voltage line, a first first clock signal line, a first second clock signal line, a first second voltage line, a first start signal line and a first reset line; the first first clock signal line, the first second clock signal line and the first reset line are all arranged on the first metal layer; the second first voltage line, the first start signal line and the first second voltage line are all arranged on the second metal layer.

8. The display substrate according to claim 7, wherein the first driving circuit includes a first on-off control transistor and a second on-off control transistor; both a gate electrode of the first on-off

control transistor and a gate electrode of the second on-off transistor are electrically connected to the second first voltage line; at least part of an orthographic projection of the second first voltage line on the base substrate is arranged between an orthographic projection of the gate electrode of the first on-off control transistor on the base substrate and an orthographic projection of a gate electrode of the second on-off control transistor on the base substrate, wherein an orthographic projection of the first start signal line on the base substrate is arranged between an orthographic projection of the second first voltage line on the base substrate and an orthographic projection of the first reset line on the base substrate.

9. The display substrate according to claim 1, wherein the driving module includes a second driving unit; the first driving unit includes a plurality of stages of second driving circuits, and the second driving circuit is configured to provide a second driving signal; the second driving unit includes a third first voltage line; the second driving circuit includes a second output sub-circuit; the second output sub-circuit includes a second driving transistor; an orthographic projection of the third first voltage line on the base substrate is arranged on a side of an orthographic projection of the second driving transistor on the base substrate away from a display area; the third first voltage line and the first first voltage line are arranged on different layers; an orthographic projection of the third first voltage line on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate.

10. The display substrate according to claim 9, wherein the orthographic projection of the third first voltage line on the base substrate coincides with the orthographic projection of the first first voltage line on the base substrate, or wherein the first driving circuit is configured to provide an N-type gate driving signal, and the second driving circuit is configured to provide a reset control signal.

11. The display substrate according to claim 9, wherein the first first voltage line is arranged on the second metal layer, and the third first voltage line is arranged on the third metal layer; or, the first first voltage line is arranged on the third metal layer, and the third first voltage line is arranged on the second metal layer, wherein the first first voltage line and the third first voltage line are low-voltage DC signal lines; or, the first first voltage line and the third first voltage line are high-voltage DC signal lines.

12. The display substrate according to claim 9, wherein the second output sub-circuit is arranged adjacent to the third first voltage line.

13. The display substrate according to claim 9, wherein the second driving unit further comprises a second start signal line, a second first clock signal line, a second second clock signal line and a second second voltage line; the third first voltage line, the second start signal line, the second first clock signal line, the second second clock signal line and the second second voltage line are arranged in sequence along a direction close to the display area.

14. The display substrate according to claim 13, wherein the second output sub-circuit further includes a second driving reset transistor; an orthographic projection of the second start signal line on the base substrate at least partially overlaps the orthographic projection of the first electrode of the second driving transistor on the base substrate, and the orthographic projection of the second start signal line on the base substrate at least partially overlaps the orthographic projection of the second electrode of the second driving transistor on the base substrate; the orthographic projection of the second start signal line on the base substrate at least partially overlaps an orthographic projection of a first electrode of the second driving reset transistor on the base substrate, and the orthographic projection of the second start signal line on the base substrate at least partially overlaps an orthographic projection of a second electrode of the second driving reset transistor on the base substrate.

15. The display substrate according to claim 13, wherein an orthographic projection of a transistor included in the second driving circuit on the base substrate is arranged at a side of an orthographic projection of the third first voltage line on the base substrate close to the display area.

16. The display substrate according to claim 14, wherein the second driving circuit further

comprises a fifteenth transistor, a twentieth transistor, and a twenty-first transistor; a gate electrode of the fifteenth transistor is electrically connected to the second first clock signal line, and a second electrode of the fifteenth transistor is electrically connected to a second electrode of the twenty-first transistor; a first electrode of the twenty-first transistor is electrically connected to a second electrode of the twentieth transistor; a gate electrode of the twentieth transistor is electrically connected to the gate electrode of the second driving reset transistor, and a gate electrode of the twenty-first transistor is electrically connected to the second second clock signal line; an orthographic projection of the gate electrode of the fifteenth transistor on the base substrate, an orthographic projection of the gate electrode of the twentieth transistor on the base substrate, and an orthographic projection of the gate electrode of the twenty-first transistor on the base substrate are arranged between the orthographic projection of the second second clock signal line on the base substrate and the orthographic projection of the second second voltage line on the base substrate, wherein the second driving circuit further comprises a sixteenth transistor; a gate electrode of the sixteenth transistor is electrically connected to the second electrode of the fifteenth transistor, a first electrode of the sixteenth transistor is electrically connected to the second first clock signal line, and a second electrode of the sixteenth transistor is electrically connected to the gate electrode of the driving reset transistor; an orthographic projection of the gate electrode of the sixteenth transistor on the base substrate is arranged between the orthographic projection of the second first clock signal line on the base substrate and the orthographic projection of the second second clock signal line on the base substrate.

17. The display substrate according to claim 9, wherein the base substrate includes a peripheral area and a display area; the driving units included in the driving module are all arranged in the peripheral area of the base substrate; the first driving unit is arranged on a side of the second driving unit away from the display area.

18. The display substrate according to claim 17, wherein the driving module comprises a third driving unit, the third driving circuit includes a plurality of stages of third driving circuits, the third driving circuit is configured to provide a third driving signal, the third driving unit is arranged at a side of the first driving unit far away from the second driving unit, wherein the driving module comprises a fourth driving unit, the driving unit comprises a plurality of stages of fourth driving circuits, the fourth driving circuit is configured to provide a fourth driving signal; the fourth driving unit is arranged on a side of the second driving unit close to the display area.

19. A display device comprising the display substrate according to claim 1.

20. A display substrate, comprising a driving module arranged on a base substrate, wherein the driving module includes a plurality of driving units, and the driving unit includes a plurality of stages of driving circuit; the driving circuit is used to provide a driving signal; the driving unit includes a first signal line, and the driving circuit includes an output sub-circuit configured to output the driving signal; the display substrate includes at least two metal layers stacked along a direction away from the base substrate; in at least one driving unit, an orthographic projection of the first signal line on the base substrate at least partially overlaps an orthographic projection of a first electrode of at least one transistor included in the output sub-circuit on the base substrate, the orthographic projection of the first signal line on the base substrate at least partially overlaps an orthographic projection of a second electrode of the at least one transistor included in the output sub-circuit on the base substrate; the first electrode and the second electrode are arranged on a same metal layer, and the first electrode and the first signal line are arranged on different metal layers; wherein the driving module includes a first driving unit; the first driving unit includes a plurality of stages of first driving circuits, and the first driving circuit is used to provide a first driving signal; the first driving unit includes a first first voltage line and a first second voltage line; the first driving circuit includes a first output sub-circuit; the first signal line is the first first voltage line; the first output sub-circuit includes a first driving transistor and a first driving reset transistor; a first electrode of the first driving transistor is electrically connected to the first second voltage line,

a second electrode of the first driving transistor is electrically connected to a first electrode of the first driving reset transistor, and a second electrode of the first driving reset transistor is electrically connected to the first first voltage line; the display substrate includes a first metal layer, a second metal layer and a third metal layer which are sequentially stacked along a direction away from the base substrate; the first electrode of the first driving transistor, the second electrode of the first driving transistor, the first electrode of the first driving reset transistor, and the second electrode of the first driving reset transistor are all arranged on the first metal layer, and the first first voltage line is arranged on the third metal layer; an orthographic projection of the first electrode of the first driving transistor on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate; an orthographic projection of the second electrode of the first driving transistor on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate; an orthographic projection of the first electrode of the first driving reset transistor on the base substrate at least partially overlaps the orthographic projection of the first first voltage line on the base substrate; an orthographic projection of the second electrode of the first driving reset transistor on the base substrate at least partially overlaps with the orthographic projection of the first first voltage line on the base substrate.