# MEMORY DEVICE AND MEMORY SYSTEM

## Abstract

A memory system, including a memory controller and a memory, wherein the memory controller selectively operates in a first mode and a second mode. In the first mode, the memory controller transmits a first command continuously during a plurality of clock cycles. In the second mode, the memory controller mixes a second command with the first command and transmits the mixture of the first command and the second command. The memory changes command latch timing depends on the first or second mode.

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**Family ID:** **1000008589560**

**Appl. No.:** **19/203735**

**Filed:** **May 09, 2025**

## Foreign Application Priority Data

| | | |
|---|---|---|
| KR | 10-2015-0126786 | Sep. 08, 2015 |

## Related U.S. Application Data

parent US continuation 18238232 20230825 parent-grant-document US 12300353 child US 19203735
parent US continuation 17862718 20220712 parent-grant-document US 11749326 child US 18238232
parent US continuation 17387036 20210728 parent-grant-document US 11715507 child US 17862718
parent US continuation 16874916 20200515 parent-grant-document US 11081152 child US 17387036
parent US continuation 16717742 20191217 parent-grant-document US 10930330 child US

16874916
parent US continuation 16169178 20181024 parent-grant-document US 10579263 child US
16717742
parent US continuation 15690379 20170830 parent-grant-document US 10114548 child US
16169178
parent US continuation 15180175 20160613 parent-grant-document US 9754649 child US
15690379

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## Publication Classification

**Int. Cl.:** **G11C8/06** (20060101); **G06F3/06** (20060101); **G06F13/16** (20060101); **G11C7/10**
(20060101); **G11C7/22** (20060101); **G11C8/10** (20060101); **G11C8/18** (20060101);
**G11C11/4076** (20060101)

**U.S. Cl.:**

CPC     **G11C8/06** (20130101); **G06F3/06** (20130101); **G06F13/1689** (20130101); **G11C7/10**
(20130101); **G11C7/1045** (20130101); **G11C7/22** (20130101); **G11C8/10** (20130101);
**G11C8/18** (20130101); **G11C11/4076** (20130101); G11C7/1057 (20130101)

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## Background/Summary

CROSS-REFERENCE TO RELATED APPLICATIONS [0001] This is a continuation application
of U.S. application Ser. No. 18/238,232 filed on Aug. 25, 2023, which is a continuation application
based on U.S. application Ser. No. 17/862,718, filed Jul. 12, 2022, which in turn is a continuation
of application Ser. No. 17/387,036, filed Jul. 28, 2021, now U.S. Pat. No. 11,715,507 B2, issued
Aug. 1, 2023, which in turn is a continuation of application Ser. No. 16/874,916, filed May 15,
2020, now U.S. Pat. No. 11,081,152 B2, issued Aug. 3, 2021, which in turn is a continuation of
application Ser. No. 16/717,742, filed Dec. 17, 2019, now U.S. Pat. No. 10,930,330 B2, issued Feb.
23, 2021, which in turn is a continuation of application Ser. No. 16/169,178, filed Oct. 24, 2018,
now U.S. Pat. No. 10,579,263 B2, issued Mar. 3, 2020, which in turn is a continuation of
application Ser. No. 15/690,379, filed Aug. 30, 2017, now U.S. Pat. No. 10,114,548 B2, issued Oct.
30, 2018, which in turn is a continuation of application Ser. No. 15/180,175, filed Jun. 13, 2016,
now U.S. Pat. No. 9,754,649 B 2, issued Sep. 5, 2017, the entire contents of all being hereby
incorporated by reference. [0002] Korean Patent Application No. 10-2015-0126786, filed on Sep.
8, 2015, and entitled, "Memory System," is incorporated by reference herein in its entirety.

BACKGROUND
1. Field
[0003] One or more embodiments described herein relate to a memory system.
2. Description of the Related Art
[0004] Efforts are continually being made to reduce the size and number of input/output pads of
memory devices. At the same time, attempts are being made to increase capacity and operation
speed in order to enhance performance.
[0005] Reducing the number of input/output pads of a memory device may involve decreasing the
number of pads for receiving commands. The commands may include, for example, addresses. As
memory capacity increases, the number of pads (e.g., address pads) may decrease, while the
number of bits of the address may increase. Thus, commands may be transferred over a plurality of
clock cycles.

[0006] When a command is transferred over a plurality of clock cycles, the time duration for transferring the command through a corresponding command pad may exceed the time duration for transferring data through data pads. This may cause inefficiencies or otherwise may disrupt performance.

SUMMARY

[0007] In accordance with one or more embodiments, a memory system includes a memory controller to selectively operate in a first mode and a second mode, the memory controller to transmit a first command continuously during a plurality of clock cycles in the first mode and the memory controller to mix a second command with the first command and transmit the mixture of the first command and the second command in the second mode; and a memory to change command latch timing depending on the first mode or the second mode.

[0008] The memory controller may insert the second command between the clock cycles of the first command in the second mode. The memory may receive flag information representing whether the second command is inserted between the clock cycles of the first command. When the flag information represents that the second command is inserted between the clock cycles of the first command, the memory may latch a second portion of the first command after a standby time from a time point of latching a first portion of the first command. The standby time may be determined based on mode register information provided from the memory controller and is to be stored in a mode register of the memory device. The memory controller may generate the first command including the flag information.

[0009] The memory controller may combine the first command and the second command as a third command to transmit the third command in the second mode. The third command may include a row address and a column address. The first command may be an active command including a row address, and the second command may be a column address strobe (CAS) command including a column address.

[0010] The memory controller may transmit the active command during 4 clock cycles and transmit the CAS command during 2 clock cycles after transmitting the active command in the first mode; and transmit a first portion of the active command during 2 clock cycles, transmit the CAS command during 2 clock cycles after transmitting the first portion of the active command, and transmit a second portion of the active command after transmitting the CAS command in the second mode. The memory controller may transmit the active command during 4 clock cycles and transmit the CAS command during 2 clock cycles after transmitting the active command in the first mode; and combine the first command and the second command as a third command and transmit the third command during 4 clock cycles in the second mode. A data transfer time for a single access operation may be substantially equal to a CAS-to-CAS delay time (tCCD) between two sequential CAS commands for two sequential access operations.

[0011] When a first access operation and a second access operation are performed successively, the memory controller may transmit a first active command for the first access operation; may transmit a first portion of a second active command for the second access operation after transmitting the first active command; may transmit a first CAS command for the first access operation after transmitting the first portion of the second active command; may transmit a second portion of the second active command after transmitting the first CAS command; and may transmit a second CAS command for the second access operation after transmitting the second portion of the second active command. The memory device may be a three-dimensional semiconductor memory device including a plurality of semiconductor dies that are stacked vertically.

[0012] In accordance with one or more other embodiments, a memory system includes a memory controller to selectively operate in a first mode and a second mode, the memory controller to transmit an active command including a row address continuously during a plurality of clock cycles in the first mode and the memory controller to mix a column address strobe (CAS) command including a column address with the active command and transmit a mixture of the active

command and the CAS command in the second mode; and a memory device to change command latch timing depending on the first mode or the second mode.

[0013] In accordance with one or more other embodiments, an apparatus includes an interface coupled to a memory; and a memory controller to selectively operate in a first mode and a second mode, the memory controller to transmit a first command continuously through the interface during a plurality of clock cycles in the first mode and to mix a second command with the first command and transmit the mixture of the first command and the second command through the interface in the second mode. The memory controller may insert the second command between the clock cycles of the first command in the second mode. The memory controller may include flag information in the first command transmitted through the interface to the memory, wherein the flag information is indicative of a change in command latch timing for the memory.

## Description

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Features will become apparent to those of skill in the art by describing in detail exemplary embodiments with reference to the attached drawings in which:

[0015] FIG. **1** illustrates an embodiment of a method for operating a memory system;

[0016] FIG. **2** illustrates an embodiment of a memory system;

[0017] FIG. **3** illustrates an embodiment of a memory device;

[0018] FIG. **4** illustrates an example of commands for a memory system;

[0019] FIG. **5** illustrates an example of date transfer and command transfer times;

[0020] FIG. **6** illustrates example operations in different modes of the memory system;

[0021] FIGS. **7** and **8** illustrate an example of signal transfer and command latch timing in a first mode;

[0022] FIGS. **9** and **10** illustrate examples of signal transfer and command latch timing in a second mode;

[0023] FIG. **11** illustrates an example of commands for a memory system;

[0024] FIG. **12** illustrates example operations in different modes of a memory system;

[0025] FIG. **13** illustrates an example of signal transfer in a second mode;

[0026] FIG. **14** illustrates an embodiment of a memory module;

[0027] FIG. **15** illustrates an embodiment of a stacked memory device;

[0028] FIG. **16** illustrates an embodiment of a memory system;

[0029] FIG. **17** illustrates an embodiment of a mobile system; and

[0030] FIG. **18** illustrates an embodiment of a computing system.

DETAILED DESCRIPTION

[0031] Example embodiments will now be described more fully hereinafter with reference to the accompanying drawings; however, they may be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey exemplary implementations to those skilled in the art. The embodiments may be combined to form additional embodiments.

[0032] In the drawings, the dimensions of layers and regions may be exaggerated for clarity of illustration. It will also be understood that when a layer or element is referred to as being "on" another layer or substrate, it may be directly on the other layer or substrate, or intervening layers may also be present. Further, it will be understood that when a layer is referred to as being "under" another layer, it may be directly under, and one or more intervening layers may also be present. In addition, it will also be understood that when a layer is referred to as being "between" two layers, it may be the only layer between the two layers, or one or more intervening layers may also be

present. Like reference numerals refer to like elements throughout.

[0033] It will be understood that, although the terms first, second, third etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are used to distinguish one element from another. Thus, a first element discussed below could be termed a second element without departing from the teachings of the present disclosure. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0034] It will be understood that when an element is referred to as being "connected" or "coupled" to another element, it may be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present. Other words used to describe the relationship between elements should be interpreted in a like fashion (e.g., "between" versus "directly between," "adjacent" versus "directly adjacent," etc.).

[0035] The terminology used herein is for the purpose of describing particular example embodiments only and is not intended to be limiting of the present disclosure. As used herein, the singular forms "a," "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0036] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0037] FIG. **1** illustrates an embodiment of a method for operating a memory system. Referring to FIG. **1**, in a first mode, a first command is continuously transferred from a memory controller and a memory device during a plurality of clock cycles (S**100**). In a second mode, a second command is mixed with the first command and the mixture of the first command and the second command is transferred from the memory controller to the memory device (S**200**).

[0038] The first command may be, for example, an active command including a row address. The second command may include, for example, a column address strobe (CAS) command including a column address. The CAS command may be a read command indicating a read operation or a write command indicating a write operation. In one embodiment, the memory device may perform row addressing based on the row address provided with or in the active command, and then may perform column addressing based on the column address provided with or in the CAS command. The first mode may correspond to an operation mode in which a plurality of commands for a single operation are transferred sequentially, in a predetermined order, from the memory controller to the memory device.

[0039] The second mode may correspond to an operation mode in which the first command and the second command are mixed. The mixed results are then transferred from the memory controller to the memory device. In some example embodiments, as described, for example, with reference to FIGS. **6** to **10**, the memory controller may insert the second command between the clock cycles of the first command in the second mode. In other example embodiments, as described, for example, with reference to FIGS. **11** to **13**, the memory controller may combine the first command and the second command as a third command and transmit the third command in the second mode.

[0040] In the memory device, command latch timing may be changed depending on the first mode or the second mode (S**300**). For example, the memory device may receive flag information representing whether the second command is inserted between the clock cycles of the first

command. In some example embodiments, as described, for example, with reference to FIG. **4**, the memory controller may incorporate the flag information into the first command and may provide the first command including the flag information to the memory device. The memory device may change the command latch timing depending on the first mode or the second mode based on the flag information in the first command. The change of the command latch timing may be performed, for example, as indicated in FIGS. **7** to **9**.

[0041] The memory system and the method of operating the memory system according to example embodiments may reduce the tCCD by adopting the second mode for mixing the two commands. Through the reduction of the tCCD, the DQ bubble, in which data transfer is not performed continuously, may be prevented and utilization of the data bus may be enhanced.

[0042] FIG. **2** illustrates an embodiment of a memory system **10**, and FIG. **3** illustrates an embodiment of a memory device **400** in the memory system **10** of FIG. **2**. Referring to FIG. **2**, the memory system **10** includes a memory controller **200** and a memory device **400**. The memory controller **200** and the memory device **400** includes respective interfaces for mutual communication. The interfaces may be connected through a control bus **21** for transferring a command CMD, an address ADDR, a clock signal CLK, etc. and a data bus **22** for transferring data.

[0043] According to some standards for memory devices, the address ADDR may be incorporated in the command CMD as illustrated in FIG. **4**. The memory controller **200** may generate the command CMD to control the memory device **400** and the data may be written in or read from the memory device **400** under the control of the memory controller **200**. According to example embodiments, the memory controller **200** may selectively operate in a first mode to transmit a first command continuously during a plurality of clock cycles or a second mode to mix a second command with the first command, and transmit a mixture of the first command and the second command. The memory device **400** may change command latch timing depending on the first mode or the second mode.

[0044] Referring to FIG. **3**, the memory device **400** may include a control logic **410**, an address register **420**, a bank control logic **430**, a row address multiplexer **440**, a refresh counter **445**, a column address latch **450**, a row decoder **460**, a column decoder **470**, a memory cell array **480**, a sense amplifier unit **485**, an input/output (I/O) gating circuit **490** and a data input/output (I/O) buffer **495**.

[0045] The memory cell array **480** may include a plurality of bank arrays **480**$a$~**480**$h$. The row decoder **460** may include a plurality of bank row decoders **460**$a$~**460**$h$ respectively coupled to the bank arrays **480**$a$~**480**$h$. The column decoder **470** may include a plurality of bank column decoders **470**$a$~**470**$h$ respectively coupled to the bank arrays **480**$a$~**480**$h$. The sense amplifier unit **485** may include a plurality of bank sense amplifiers **485**$a$~**485**$h$ respectively coupled to the bank arrays **480**$a$~**480**$h$.

[0046] The address register **420** may receive an address ADDR including a bank address BANK_ADDR, a row address ROW_ADDR, and a column address COL_ADDR from the memory controller. The address register **420** may provide the received bank address BANK_ADDR to the bank control logic **430**, the received row address ROW_ADDR to the row address multiplexer **440**, and the received column address COL_ADDR to the column address latch **450**.

[0047] The bank control logic **430** may generate bank control signals based on the bank address BANK_ADDR. One of the bank row decoders **460**$a$~**460**$h$ corresponding to the bank address BANK_ADDR may be activated based on the bank control signals. One of the bank column decoders **470**$a$~**470**$h$ corresponding to the bank address BANK_ADDR may be activated based on the bank control signals.

[0048] The row address multiplexer **440** may receive the row address ROW_ADDR from the address register **420** and may receive a refresh row address REF_ADDR from the refresh counter

**445**. The row address multiplexer **440** may selectively output the row address ROW_ADDR or the refresh row address REF_ADDR as a row address RA. The row address RA output from the row address multiplexer **440** may be applied to the bank row decoders **460***a*˜**460***h*.

[0049] The activated one of the bank row decoders **460***a*˜**460***h* may decode the row address RA output from the row address multiplexer **440** and may activate a word-line corresponding to the row address RA. For example, the activated bank row decoder may apply a word-line driving voltage to the word-line corresponding to the row address RA.

[0050] The column decoder **470** may include a column address latch (CAL) **450**. The column address latch may receive the column address COL_ADDR from the address register **420** and temporarily store the received column address COL_ADDR. In some embodiments, in a burst mode, the column address latch **450** may generate column addresses that increment from the received column address COL_ADDR. The column address latch **450** may apply the temporarily stored or generated column address to the bank column decoders **470***a*˜**470***h*.

[0051] The activated one of the bank column decoders **470***a*˜**470***h* may decode the column address COL_ADDR output from the column address latch **450** and may control the I/O gating circuit **490** in order to output data corresponding to the column address COL_ADDR.

[0052] The I/O gating circuit **490** may include circuitry for gating input/output data. The I/O gating circuit **490** may further include read data latches for storing data output from the bank arrays **480***a*˜**480***h* and write drivers for writing data to the bank arrays **480***a*˜**480***h*.

[0053] Data to be read from one bank array of the bank arrays **480***a*˜**480***h* may be sensed by a sense amplifier unit **485** coupled to the one bank array from which the data is to be read and may be stored in the read data latches. The data stored in the read data latches may be provided to the memory controller via the data I/O buffer **495**. Data DQ to be written in one bank array of the bank arrays **480***a*˜**480***h* may be provided to the data I/O buffer **495** from the memory controller. The write driver may write the data DQ in one bank array of the bank arrays **480***a*˜**480***h*.

[0054] The control logic **410** may control operations of the memory device **400**. For example, the control logic **410** may generate control signals for the memory device **400** in order to perform a write operation or a read operation. The control logic **410** may include a command decoder **411** that decodes a command CMD received from the memory controller **200** and a mode register set **412** that sets an operation mode of the memory device.

[0055] In some example embodiments, the control logic **410** may generate latch control signals LTR and LTC, for example, as illustrated in FIGS. **7** and **9**, to control operation of the address register **420**. The control logic may generate the latch control signals LTR and LTC based on the flag information representing whether the second command is inserted between the clock cycles of the first command.

[0056] FIG. **3** illustrates that the control logic **410** and the address register **420** are distinct from each other. In another embodiment, the control logic **410** and the address register **420** may be implemented as a single inseparable circuit. In addition, FIG. **3** illustrates that the command CMD and the address ADDR are provided as distinct signals. In another embodiment, the command CMD and the address ADDR may be provided as combined signals, for example, as illustrated in FIG. **4**.

[0057] FIG. **4** illustrates example commands which may be used in one embodiment of a memory system. In this embodiment, combinations of the chip selection signal CS and the command-address signals CA**0**˜CA**6** representing an active command ACT, a read command RD, a write command WR and a mode register write command MRW. Also, H indicates the logic high level, L indicates the logic low level, R**0**˜R**17** indicate bits of a row address RA, BA**0**˜BA**3** indicate bits of a bank address BA, V indicates any one of the logic low level and the logic high level, BL indicates a burst length, C**4**˜C**9** indicate bits of a column address CA, MA**0**˜MA**5** indicate a location of the mode register in which the mode register write operation is performed, OP**0**˜OP**7** indicate the mode information to be written in the mode register, and RE**1**˜RE**4** indicate first through fourth rising

edges of a clock signal CK.

[0058] The active command ACT may include a first portion ACTa and a second portion ACTb and the active command ACT may be transferred during a plurality of clock cycles, for example, during the four clock cycles as illustrated in FIG. **4**. The active command ACT may include the bank address bits BA**0**~BA**3** and the row address bits R**0**~R**17**. Also the active command ACT may include the flag information SPL representing whether the other command is inserted between the clock cycles of the active command ACT. The first logic level (e.g., logic low level L) of the flag information SPL may indicate the first mode or the normal mode in which the first portion ACTa and the second portion ACTb of the active command ACT are transferred continuously during a plurality of clock cycles. The second logic level (e.g., logic high level H) of the flag information SPL may indicate the second mode or the split mode in which the other command is inserted between the first portion ACT a and the second portion ACTb of the active command ACT and the mixture of the active command ACT and the other command is transferred.

[0059] Each of the read command RD and the write command WR may include the bank address bits BA**0**~BA**3** and the column address bits C**4**~C**9** and may be transferred during a plurality of clock cycles, for example, during the two clock cycles as in FIG. **4**.

[0060] The mode register write command MRW may include a first portion MRW a and a second portion MRWb. The mode register write command MRW may be transferred during a plurality of clock cycles, for example, during the four clock cycles as illustrated in FIG. **4**. The mode register write command MRW may include the mode register location bits MA**0**~MA**5** and the mode information bits OP**0**~OP**7**. Also, the mode register write command MRW may include the flag information SPL representing whether the other command is inserted between the clock cycles of the mode register write command MRW.

[0061] The first logic level (e.g., logic low level L) of the flag information SPL may indicate the first mode or the normal mode in which the first portion MRWa and the second portion MRWb of the mode register write command MRW are transferred continuously during a plurality of clock cycles. The second logic level (e.g., logic high level H) of the flag information SPL may indicate the second mode or the split mode in which the other command is inserted between the first portion MRWa and the second portion MRWb of the mode register write command MRW and the mixture of the mode register write command MRW and the other command is transferred.

[0062] FIG. **4** illustrates non-limiting examples of combinations of the chip selection signal CS and the command-address signals CA**0**~CA**6**. In at least one embodiment, combinations of signals representing the commands may be changed in various ways.

[0063] FIG. **5** illustrating a timing diagram describing an example of a data transfer time and a command transfer time. Referring to FIG. **5**, the commands ACT and RD may be transferred in synchronization with a main clock signal MCK of a memory system. For example, the transfer time of the active command ACT may correspond to the four clock cycles of the main clock signal MCK and the transfer time of the read command RD may correspond to the four clock cycles of the main clock signal MCK. As such, the transfer time of the commands ACT and RD for the read operation may correspond to the eight clock cycles of the main clock signal MCK.

[0064] The data transfer time may be changed depending on the clock frequency for the data transfer, the burst length BL, etc. For example, the data bits **0**~**31** may be transferred in synchronization with the main clock signal MCK or the data clock signal WCK having a doubled frequency according to the configuration of the memory system.

[0065] When the burst length BL is 16 and the data transfer is synchronized with the main clock signal MCK, the 16 data bits **0**~**16** may be transferred during the 8 clock cycles of the main clock signal MCK. Thus, the data transfer time may be equal to the command transfer time. When the burst length BL is 32 and the data transfer is synchronized with the data clock signal WCK, the 32 data bits **0**~**31** may be transferred during the 8 clock cycles of the main clock signal MCK. Thus, the data transfer time may be equal to the command transfer time. When the burst length BL is 16

and the data transfer is synchronized with the data clock signal WCK, the 16 data bits **0~16** may be transferred during the 4 clock cycles of the main clock signal MCK. Thus, the data transfer time may be shorter than the command transfer time.

[0066] The problem of utilization of the data bus may not be caused when the data transfer time is equal to the command transfer time. However, the problem of DQ bubble may be caused such that the data transfer may not be performed continuously when the data transfer time is shorter than the command transfer time.

[0067] FIG. **6** illustrates a timing diagram of example operations in a first mode and a second mode. Referring to FIG. **6**, the command may be determined as the combination of the chip selection signal CS and the command-address signals CA at the rising edges T**1**~T**9** of the main clock signal MCK. The examples of the combination of the chip selection signal CS and the command-address signals CA are illustrated in FIG. **4**. FIG. **6** illustrates the command-address signals CAn in the first mode and the command-address signals CAm in the second mode.

[0068] The first command may be transferred continuously during a plurality of clock cycles in the first mode. The mixture of the first command and the second command may be transferred in the second mode. As illustrated in FIG. **6**, the first command may be the active command ACT and the second command may be the CAS command. FIG. **6** illustrates the read command RD as an example of the CAS command and the CAS command may be the write command WR.

[0069] The memory controller **200** in FIG. **2** may transmit the active command ACT during the four clock cycles corresponding to the four rising edges T**3**, T**4**, T**5**, and T**6** of the main clock signal MCK. The memory controller **200** may then transmit the CAS command RD during the two clock cycles corresponding to the two rising edges T**7** and T**8** in the first mode. The flag information SPL in the active command ACT may be at logic low level L.

[0070] In contrast, the memory controller **200** may transmit the first portion ACT a of the active command ACT during the two clock cycles corresponding to the two rising edges T**1** and T**2**. The memory controller **200** may transmit the CAS command RD during the two clock cycles corresponding to the two rising edges T**3** and T**4**. The memory controller **200** may then transmit the second portion ACTb of the active command ACT during the two clock cycles corresponding to the two rising edges T**5** and T**6** in the second mode. The flag information SPL in the first portion ACT a of the active command ACT may be at logic high level H.

[0071] As illustrated in FIG. **6**, the CAS-to-CAS delay time (tCCD) corresponding to the time duration between the two successive CAS commands may be reduced by adopting the second mode for mixing the two commands. The tCCDn in the first mode corresponds to the 6 clock cycles but the tCCDm in the second mode may be reduced to the 4 clock cycles. Through the reduction of the tCCD, the DQ bubble, in which data transfer is not performed continuously, may be prevented and utilization of the data bus may be enhanced.

[0072] FIGS. **7** and **8** are timing diagrams illustrating an example of a signal transfer and a command latch timing in a first mode. In particular, FIG. **7** illustrates command transfer and command latch timing in the first mode or the normal mode when a first access operation and a second access operation are performed successively. FIG. **8** illustrates corresponding data transfer. As described above, the command may be determined as the combination of the chip selection signal CS and the command-address signals CA at the rising edges T**1**~T**15** of the main clock signal MCK.

[0073] Referring to FIG. **7**, a first active command ACT**1** and a first CAS command RD**1** for a first access operation may be transferred sequentially and then a second active command ACT**2** and a second CAS command RD**2** for a second access operation may be transferred sequentially. FIG. **7** illustrates the read command RD as an example of the CAS command and the CAS command may be the write command WR.

[0074] In the first mode, the memory controller **200** in FIG. **2** may transmit the first active command ACT**1** during the 4 clock cycles corresponding to the 4 rising edges T**1**, T**2**, T**3**, and T**4**

of the main clock signal MCK, transmit the first CAS command RD1 during the 2 clock cycles corresponding to the 2 rising edges T5 and T6 after transmitting the first active command ACT1, transmit the second active command ACT2 during the 4 clock cycles corresponding to the 4 rising edges T7, T8, T9, and T10 after transmitting the first CAS command RD1, and then transmit the second CAS command RD2 during the 2 clock cycles corresponding to the 2 rising edges T11 and T12 after transmitting the second active command ACT2. In this case, the flag information SPL in the first active command ACT1 and the second active command ACT2 may be at a first logic level (e.g., logic low level L) to indicate the first mode. As a result, the tCCD between the two consecutive CAS commands RD1 and RD2 may correspond to the 6 clock cycles 6tCK.

[0075] The control logic 410 in the memory device 400 of FIG. 3 may generate a row latch control signal LTR and a column latch control signal LTC and provide them to the address register 420. The address register 420 may latch the row addresses in the active commands ACT1 and ACT2 in response to the row latch control signal LTR. The address register 420 may latch the column addresses in the CAS commands RD1 and RD2 in response to the column latch control signal LTC. For example, as illustrated in FIG. 7, the control logic 410 may activate the row latch control signal LTR in a form of 4 pulses when the active command ACT corresponding to the 4 clock cycles is received. The control logic 410 may activate the column latch control signal LTC in a form of 2 pulses when the CAS command RD corresponding to the 2 clock cycles is received.

[0076] The control logic 410 may control the activation timing of the row latch control signal LTR based on the flag information SPL representing whether the CAS command is inserted between the clock cycles of the active command ACT. The control logic 410 may activate the row latch control signal LTR in synchronization with the 4 consecutive rising edges T1, T2, T3, and T4 when the flag information in the first active command ACT1 is the logic low level L to indicate the first mode. Also, the control logic 410 may activate the row latch control signal LTR in synchronization with the 4 consecutive rising edges T7, T8, T9, and T10 when the flag information in the second active command ACT2 is a logic low level L to indicate the first mode.

[0077] FIG. 8 illustrates an example of data transfer in the first mode performed in synchronization with the data clock signal WCK with the burst length of 16. In this case, the data transfer time tTR for one access operation corresponds to the 4 clock cycles 4tCK of the main clock signal MCK.

[0078] Referring to FIG. 8, transfer of the data bits 0~15 may begin through the data bus or the data pin DQ after a predetermined latency LAT from the respective time points T6 and T12 when the CAS commands RD1 and RD2 are received by the memory device through the control bus. The latency LAT may be the read latency when the CAS command is the read command RD and the latency LAT may be the write latency when the CAS command is the write command WR. FIG. 8 illustrates the latency LAT of the one clock cycle for convenience of illustration. The latency LAT may be determined variously depending on the configuration of the memory system and/or type of the access operation.

[0079] As illustrated in FIG. 8, the data transfer time tTR for the one access operation may be the four clock cycles 4tCK of the main clock signal MCK and the tCCD between the two consecutive CAS commands RD1 and RD2 may be the 6 clock cycles 6tCK of the main clock signal MCK. As such, a DQ bubble may be caused if the tCCD is longer than the data transfer time tTR. In this case, data transfer for the consecutive access operations may not be performed continuously due to the DQ bubble. The DQ bubble may degrade utilization of the data bus by increasing the enable time of the data clock signal.

[0080] FIGS. 9 and 10 are timing diagrams illustrating an example of a signal transfer and a command latch timing in a second mode. In particular, FIG. 9 illustrates command transfer and command latch timing in the second mode or the mixed mode when a first access operation and a second access operation are performed successively. FIG. 10 illustrates corresponding data transfer. As described above, the command may be determined as the combination of the chip selection signal CS and the command-address signals CA at the rising edges T1~T15 of the main clock signal

MCK.

[0081] Referring to FIG. **9**, a first active command ACT**1** and a first CAS command RD**1** for a first access operation may be transferred and a second active command ACT**2** and a second CAS command RD**2** for a second access operation may be transferred. FIG. **9** illustrates the read command RD as an example of the CAS command and the CAS command may be the write command WR.

[0082] The memory controller **200** in FIG. **2** may transmit the first active command ACT**1** during the 4 clock cycles corresponding to the 4 rising edges T**1**, T**2**, T**3**, and T**4** of the main clock signal MCK in the first mode. After transmitting the first active command ACT**1**, the memory controller **200** may transmit the second active command ACT**2** and the first CAS command RD**1** in the second mode.

[0083] For example, the memory controller **200** may transmit the first portion ACT**2***a* of the second active command ACT**2** during the 2 clock cycles corresponding to the 2 rising edges T**5** and T**6**, transmit the first CAS command RD**1** during the 2 clock cycles corresponding to the 2 rising edges T**7** and T**8** after transmitting the first portion ACT**2***a*, and transmit the second portion ACT**2***b* of the second active command ACT**2** during the 2 clock cycles corresponding to the 2 rising edges T**9** and T**10**. After transmitting the second portion ACT**2***b* of the second active command ACT**2**, the memory controller **200** may transmit the second CAS command RD**2** during the 2 clock cycles corresponding to the 2 rising edges T**11** and T**12**.

[0084] In this case, the flag information SPL in the first active command ACT**1** may be a first logic level (e.g., logic low level L) to indicate the first mode and the flag information in the second active command ACT**2** may be a second logic level (e.g., logic high level H) to indicate the second mode. As a result, the tCCD between the two consecutive CAS commands RD**1** and RD**2** may correspond to the 4 clock cycles 4tCK.

[0085] The control logic **410** in the memory device **400** of FIG. **3** may generate a row latch control signal LTR and a column latch control signal LTC and provide them to the address register **420**. The address register **420** may latch the row addresses in the active commands ACT**1** and ACT**2** in response to the row latch control signal LTR. The address register **420** may latch the column addresses in the CAS commands RD**1** and RD**2** in response to the column latch control signal LTC.

[0086] For example, as illustrated in FIG. **9**, the control logic **410** may activate the row latch control signal LTR in a form of 4 pulses when the active command ACT corresponding to the 4 clock cycles is received. The control logic **410** may activate the column latch control signal LTC in a form of 2 pulses when the CAS command RD corresponding to the 2 clock cycles is received. The control logic **410** may control the activation timing of the row latch control signal LTR based on the flag information SPL representing whether the CAS command is inserted between the clock cycles of the active command ACT. The control logic **410** may activate the row latch control signal LTR in synchronization with the 4 consecutive rising edges T**1**, T**2**, T**3**, and T**4** when the flag information in the first active command ACT**1** is a logic low level to indicate the first mode. In contrast, the control logic **410** may activate the row latch control signal LTR in synchronization with the 4 non-consecutive rising edges T**5**, T**6**, T**9**, and T**10** when the flag information in the second active command ACT**2** is a logic high level H to indicate the second mode.

[0087] The address register **420** in the memory device **400** may latch the second portion ACT**2***b* of the second active command ACT**2** after a standby time tWT from a time point T**6** of latching the first portion ACT**2***a* of the second active command ACT**2** in response to the row latch control signal LTR, when the flag information SPL represents that the other command (e.g., the first CAS command RD**1**) is inserted between the clock cycles of the second active command ACT**2**. The standby time tWT may be determined based on mode register information provided from the memory controller **200** and stored in the mode register set **412** in the memory device **400** of FIG. **3**. The mode register information may be provided through the mode register write command MRW. The mode register write command MRW may include the information OP**0**-OP**7** as illustrated in

FIG. **4** to be written in the mode register set **412**.

[0088] FIG. **10** illustrates an example of data transfer in the second mode performed in synchronization with the data clock signal WCK with the burst length of 16. In this case, the data transfer time tTR for one access operation corresponds to the 4 clock cycles 4tCK of the main clock signal MCK.

[0089] Referring to FIG. **10**, transfer of the data bits **0˜15** may begin through the data bus or the data pin DQ after a predetermined latency LAT from the respective time points T**8** and T**12** when the CAS commands RD**1** and RD**2** are received by the memory device through the control bus. The latency LAT may be the read latency when the CAS command is the read command RD and the latency LAT may be the write latency when the CAS command is the write command WR. FIG. **10** illustrates the latency LAT of the one clock cycle for convenience of illustration and the latency LAT may be determined in various ways depending on configuration of the memory system and/or type of the access operation.

[0090] As illustrated in FIG. **10**, the data transfer time tTR for the one access operation may be the four clock cycles 4tCK of the main clock signal MCK. The tCCD between the two consecutive CAS commands RD**1** and RD**2** may be the 4 clock cycles 4tCK of the main clock signal MCK. As such, a DQ bubble, for example, as illustrated in FIG. **8**, may be removed if the tCCD is equal to the data transfer time tTR, and the data transfer for the consecutive access operations may be performed continuously.

[0091] The memory system and the method of operating the memory system according to example embodiments may therefore reduce the tCCD by adopting the second mode for mixing the two commands. Through the reduction of the tCCD, the DQ bubble, in which data transfer is not performed continuously, may be prevented and utilization of the data bus may be enhanced.

[0092] FIG. **11** illustrating another example of commands that may be used in a memory system. In particular, FIG. **11** illustrates combinations of the chip selection signal CS and the command-address signals CA**0**˜CA**8** representing an active command ACT, a read command RD and a write command WR in the first mode or the normal mode and an active-read command ACT-RD and an active-write command ACT-WR in the second mode or the mixed mode. Also, H indicates a logic high level, L indicates a logic low level, R**0**˜R**16** indicate bits of a row address RA, BA**0**˜BA**3** indicate bits of a bank address BA, V indicates any one of the logic low level and the logic high level, AP indicates auto-precharge, BL indicates a burst length, C**4**˜C**9** indicate bits of a column address CA, and RE**1**˜RE**4** indicate first through fourth rising edges of clock signal CK.

[0093] The memory controller **200** in FIG. **2** may combine two commands as a single combined command to transmit the single combined command in the second mode. For example, as illustrated in FIG. **11**, the read command RD and the active command ACT in the normal mode may be combined as the active-read command ACT-RD in the mixed mode. The write command WR and the active command ACT in the normal mode may be combined as the active-write command ACT-WR in the mixed mode. Each of the active-read command ACT-RD and the active-write command ACT-WR may include both the row address R**0**˜R**16** and the column address C**4**˜C**9**.

[0094] FIG. **12** is a timing diagram illustrating example operations in a first mode and a second mode. Referring to FIG. **12**, the command may be determined as the combination of the chip selection signal CS and the command-address signals CA at the rising edges T**1**˜T**9** of the main clock signal MCK. The examples of the combination of the chip selection signal CS and the command-address signals CA are illustrated in FIG. **11**. FIG. **12** illustrates the command-address signals may in the first mode or the normal mode and the command-address signals CAm in the second mode or the mixed mode.

[0095] The first command may be transferred continuously during a plurality of clock cycles in the first mode. The mixture of the first command and the second command may be transferred in the second mode. As illustrated in FIG. **12**, the first command may be the active command ACT and

the second command may be the CAS command. FIG. **12** illustrates the read command RD as an example of the CAS command and the CAS command may be the write command WR.

[0096] The memory controller **200** in FIG. **2** may transmit the active command ACT during the four clock cycles corresponding to the four rising edges T**3**, T**4**, T**5**, and T**6** of the main clock signal MCK. The memory controller **200** may then transmit the CAS command RD during the two clock cycles corresponding to the two rising edges T**7** and T**8** in the first mode.

[0097] In one embodiment, the memory controller **200** may transmit the combined active-CAS command ACT-RD during the four clock cycles corresponding to the four rising edges T**1**, T**2**, T**3**, and T**4**, and may transmit the next combined active-CAS command ACT-RD during the four clock cycles corresponding to the four rising edges T**5**, T**6**, T**7** and T**8**.

[0098] As illustrated in FIG. **12**, the CAS-to-CAS delay time (tCCD) corresponding to the time duration between the two successive CAS commands may be reduced by adopting the second mode for mixing the two commands. The tCCDn in the first mode corresponds to the 6 clock cycles but the tCCDm in the second mode may be reduced to the 4 clock cycles. Through the reduction of the tCCD, a DQ bubble, in which data transfer is not performed continuously, may be prevented and utilization of the data bus may be enhanced.

[0099] FIG. **13** is a timing diagram illustrating an example of a signal transfer in a second mode. In particular, FIG. **13** illustrates command transfer and command latch timing in the second mode when a first access operation and a second access operation are performed successively. As described above, the command may be determined as the combination of the chip selection signal CS and the command-address signals CA at the rising edges T**1**˜T**13** of the main clock signal MCK.

[0100] Referring to FIG. **13**, a first active-CAS command ACT-RD**1** for a first access operation, a second active-CAS command ACT-RD**2** for a second access operation, and a third active-CAS command ACT-RD**3** for a third access operation may be transferred successively from the memory controller to the memory device. FIG. **13** illustrates the active-read command ACT-RD as an example of the combined command and the combined command may be the active-write command ACT-WR.

[0101] The memory controller **200** in FIG. **2** may transmit the first active-CAS command ACT-RD**1** during the 4 clock cycles corresponding to the 4 rising edges T**1**, T**2**, T**3**, and T**4** of the main clock signal MCK in the second mode, and may transmit the second active-CAS command ACT-RD**2** during the 4 clock cycles corresponding to the 4 rising edges T**5**, T**6**, T**7**, and T**8** of the main clock signal MCK in the second mode. The memory controller **200** may then transmit the third active-CAS command ACT-RD**3** during the 4 clock cycles corresponding to the 4 rising edges T**9**, T**10**, T**11**, and T**12** of the main clock signal MCK in the second mode. As a result, the tCCD between the two consecutive active-CAS commands ACT-RD**1** and ACT-RD**2** may correspond to the 4 clock cycles 4tCK.

[0102] FIG. **13** illustrates data transfer in the second mode which is performed in synchronization with the data clock signal WCK with the burst length of 16. In this case, the data transfer time tTR for one access operation corresponds to the 4 clock cycles 4tCK of the main clock signal MCK.

[0103] Transfer of the data bits **0**˜**15** may begin through the data bus or the data pin DQ after a predetermined latency LAT from the respective time points T**4**, T**8**, and T**12** when the active-CAS commands ACT-RD**1**, ACT-RD**2**, and ACT-RD**3** are received by the memory device through the control bus. The latency LAT may be the read latency when the combined command is the active-read command ACT-RD. The latency LAT may be the write latency when the combined command is the active-write command ACT-WR. FIG. **13** illustrates the latency LAT of the one clock cycle for convenience of illustration. The latency LAT may be determined in various ways depending on configuration of the memory system and/or type of the access operation.

[0104] As illustrated in FIG. **13**, the data transfer time tTR for each access operation may be the four clock cycles 4tCK of the main clock signal MCK and also the tCCD between the two

consecutive active-CAS commands ACT-RD**1** and ACT-RD**2** may be the 4 clock cycles 4tCK of the main clock signal MCK. As such, a DQ bubble, for example, as illustrated in FIG. **8**, may be removed if the tCCD is equal to the data transfer time tTR and the data transfer for the consecutive access operations may be performed continuously.

[0105] The memory system and the method of operating the memory system according to example embodiments may therefore reduce the tCCD by adopting the second mode for mixing the two commands. Through the reduction of the tCCD, the DQ bubble, in which data transfer is not performed continuously, may be prevented and utilization of the data bus may be enhanced.

[0106] FIG. **14** illustrates an embodiment of a memory module **800** which includes a module substrate **810**, a plurality of semiconductor memory chips SM C and a buffer chip BC. The semiconductor memory chips SM C may be mounted on the module substrate **810**. Each of the semiconductor memory chips SM C may receive data DQ from an external device such as a memory controller through a data bus **812** in a write mode, or may transmit the data DQ to the external device through the data bus **812** in a read mode.

[0107] The buffer chip BC may be mounted on the module substrate **810** and the buffer chip BC may receive command signals CMD and address signals ADD through a control bus **511**, to provide the received signals CMD and ADD to the semiconductor memory chips SMC through internal buses **513** and **514**. The buffer chip BC may include a register to store control information of the memory module **800**.

[0108] An external device, such as the memory controller, may selectively operate in a first mode or a second mode. In the first mode, the external device may transmit a first command continuously during a plurality of clock cycles. In the second mode, the external device may mix a second command with the first command and may transmit the mixture of the first command and the second command. Each of the semiconductor memory chips SMC may change command latch timing depending on the first mode or the second mode. The tCCD may be reduced by adopting the second mode for mixing the two commands. Through the reduction of the tCCD, a DQ bubble, in which data transfer is not performed continuously, may be prevented and utilization of the data bus may be enhanced.

[0109] FIG. **15** illustrates an embodiment of a stacked memory device **900** which includes first through kth semiconductor integrated circuit layers LA**1** through LAk. The lowest first semiconductor integrated circuit layer LA**1** may be a master layer. The other semiconductor integrated circuit layers LA**2** through LAk may be slave layers.

[0110] The first through kth semiconductor integrated circuit layers LA**1** through LAk may transmit and receive signals between the layers by through-substrate vias (e.g., through-silicon vias (TSVs)). The lowest first semiconductor integrated circuit layer LA**1**, as the master layer, may communicate with an external memory controller through a conductive structure formed on an external surface.

[0111] The first semiconductor integrated circuit layer **910** through the kth semiconductor integrated circuit layer **920** may include memory regions **921** and various peripheral circuits **922** for driving the memory regions **921**. For example, the peripheral circuits may include a row (X)-driver for driving word lines of a memory, a column (Y)-driver for driving bit lines of the memory, a data input/output unit for controlling input/output of data, a command buffer for receiving a command from an external device and buffering the command, and an address buffer for receiving an address from an external device and buffering the address.

[0112] The first semiconductor integrated circuit layer **910** may further include control logic which generates control signals to control the memory region **921** based on the command-address signals from the memory controller.

[0113] According to example embodiments, the stacked memory device **900** may change command latch timing depending on the first mode or the second mode as described above. The tCCD may be reduced by adopting the second mode for mixing the two commands. Through the reduction of the

tCCD, a DQ bubble, in which data transfer is not performed continuously, may be prevented and utilization of the data bus may be enhanced.

[0114] FIG. **16** illustrates an embodiment of a memory system **1000** which includes a memory module **1010** and a memory controller **1020**. The memory module **1010** may include at least one semiconductor memory device **1030** mounted on a module substrate. For example, the semiconductor memory device **1030** may be constructed as a DRAM chip. In addition, the semiconductor memory device **1030** may include a stack of semiconductor dies. In some example embodiments, the semiconductor dies may include the master die **1031** and the slave dies **1032**. Signal transfer between the semiconductor chips may occur via through-substrate vias (e.g., TSVs) and/or bonding wires.

[0115] The memory module **1010** may communicate with the memory controller **1020** via a system bus. Data DQ, a command/address CMD/ADD, and a clock signal CLK may be transmitted and received between the memory module **1010** and the memory controller **1020** via the system bus.

[0116] As described above, the memory controller **1020** may selectively operate in a first mode, to transmit a first command continuously during a plurality of clock cycles, or in a second mode to mix a second command with the first command and transmit the mixture of the first command and the second command. Each of the semiconductor memory devices **1030** may change command latch timing depending on the first mode or the second mode. The tCCD may be reduced by adopting the second mode for mixing the two commands. Through the reduction of the tCCD, a DQ bubble, in which data transfer is not performed continuously, may be prevented and utilization of the data bus may be enhanced.

[0117] FIG. **17** illustrates an embodiment of a mobile system **1200** which includes an application processor **1210**, a connectivity unit **1220**, a volatile memory device (VM) **1230**, a nonvolatile memory device **1240**, a user interface **1250**, and a power supply **1260**. In some embodiments, the mobile system **1200** may be a mobile phone, a smart phone, a personal digital assistant (PDA), a portable multimedia player (PMP), a digital camera, a music player, a portable game console, a navigation system, or another type of electronic device.

[0118] The application processor **1210** may execute applications such as a web browser, a game application, a video player, etc. In some embodiments, the application processor **1210** may include a single core or multiple cores. For example, the application processor **1210** may be a multi-core processor such as a dual-core processor, a quad-core processor, a hexa-core processor, etc. The application processor **1210** may include an internal or external cache memory.

[0119] The connectivity unit **1220** may perform wired or wireless communication with an external device. For example, the connectivity unit **1220** may perform Ethernet communication, near field communication (NFC), radio frequency identification (RFID) communication, mobile telecommunication, memory card communication, universal serial bus (USB) communication, etc. In some embodiments, connectivity unit **1220** may include a baseband chipset that supports communications, such as global system for mobile communications (GSM), general packet radio service (GPRS), wideband code division multiple access (WCDMA), high speed downlink/uplink packet access (HSxPA), etc.

[0120] The volatile memory device **1230** may store data processed by the application processor **1210**, or may operate as a working memory. For example, the volatile memory device **1230** may be a dynamic random access memory, such as DDR SDRAM, LPDDR SDRAM, GDDR SDRAM, RDRAM, etc. The nonvolatile memory device **1240** may store a boot image for booting the mobile system **1200**. For example, the nonvolatile memory device **1240** may be an electrically erasable programmable read-only memory (EEPROM), a flash memory, a phase change random access memory (PRA M), a resistance random access memory (RRAM), a nano floating gate memory (NFGM), a polymer random access memory (PoRAM), a magnetic random access memory (MRAM), a ferroelectric random access memory (FRAM), etc.

[0121] The application processor **1210** may generate commands for controlling the memory

devices **1230** and **1240**. The application processor **1210** may selectively operate in a first mode to transmit a first command continuously during a plurality of clock cycles or in a second mode to mix a second command with the first command and transmit a mixture of the first command and the second command. Each of the memory devices **1230** and **1240** may change command latch timing depending on the first mode or the second mode. The tCCD may be reduced by adopting the second mode for mixing the two commands. Through the reduction of the tCCD, the DQ bubble, in which data transfer is not performed continuously, may be prevented and utilization of the data bus may be enhanced.

[0122] The user interface **1250** may include at least one input device, such as a keypad, a touch screen, etc., and at least one output device, such as a speaker, a display device, etc. The power supply **1260** may supply a power supply voltage to the mobile system **1200**. In some embodiments, the mobile system **1200** may further include a camera image processor (CIS), and/or a storage device, such as a memory card, a solid state drive (SSD), a hard disk drive (HDD), a CD-ROM, etc.

[0123] In some embodiments, the mobile system **1200** and/or components of the mobile system **1200** may be packaged in various forms. Examples include package-on-package (PoP), ball grid arrays (BGAs), chip scale packages (CSPs), plastic leaded chip carrier (PLCC), plastic dual in-line package (PDIP), die-in-waffle pack, die-in-wafer form, chip-on-board (COB), ceramic dual in-line package (CERDIP), plastic metric quad flat pack (MQFP), thin quad flat pack (TQFP), small outline IC (SOIC), shrink small outline package (SSOP), thin small outline package (TSOP), system-in-package (SIP), multi-chip package (MCP), wafer-level fabricated package (WFP), wafer-level processed stack package (WSP), etc.

[0124] FIG. **18** illustrates an embodiment of a computing system **1300** which includes a processor **1310**, an input/output hub (IOH) **1320**, an input/output controller hub (ICH) **1330**, at least one memory module **1340**, and a graphics card **1350**. In some embodiments, the computing system **1300** may be a personal computer (PC), a server computer, a workstation, a laptop computer, a mobile phone, a smart phone, a personal digital assistant (PDA), a portable multimedia player (PMP), a digital camera), a digital television, a set-top box, a music player, a portable game console, navigation system, etc.

[0125] The processor **1310** may perform various computing functions such as executing specific software for performing specific calculations or tasks. For example, the processor **1310** may be a microprocessor, a central process unit (CPU), a digital signal processor, or the like. In some embodiments, the processor **1310** may include a single core or multiple cores. For example, the processor **1310** may be a multi-core processor, such as a dual-core processor, a quad-core processor, a hexa-core processor, etc. Although FIG. **18** illustrates the computing system **1300** including one processor **1310**, in some embodiments, the computing system **1300** may include a plurality of processors. The processor **1310** may include an internal or external cache memory.

[0126] The processor **1310** may include a memory controller **1311** for controlling operations of the memory module **1340**. The memory controller **1311** included in the processor **1310** may be referred to as an integrated memory controller (IMC). A memory interface between the memory controller **1311** and the memory module **1340** may be implemented with a single channel including a plurality of signal lines, or may bay be implemented with multiple channels, to each of which at least one memory module **1340** may be coupled. In some embodiments, the memory controller **1311** may be located inside the input/output hub **1320**, e.g., a memory controller hub (MCH).

[0127] The memory module **1340** may include at least one memory chip. The memory controller **1311** may selectively operate in a first mode to transmit a first command continuously during a plurality of clock cycles or in a second mode to mix a second command with the first command and transmit a mixture of the first command and the second command. The chip in the memory module **1340** may change command latch timing depending on the first mode or the second mode. The tCCD may be reduced by adopting the second mode for mixing the two commands. Through the reduction of the tCCD, a DQ bubble, in which data transfer is not performed continuously, may be

prevented and utilization of the data bus may be enhanced.

[0128] The input/output hub **1320** may manage data transfer between processor **1310** and devices, such as the graphics card **1350**. The input/output hub **1320** may be coupled to the processor **1310** via various interfaces. For example, the interface between the processor **1310** and the input/output hub **1320** may be a front side bus (FSB), a system bus, a HyperTransport, a lightning data transport (LDT), a QuickPath interconnect (QPI), a common system interface (CSI), etc.

[0129] Although FIG. **18** illustrates the computing system **1300** including one input/output hub **1320**, in some embodiments, the computing system **1300** may include a plurality of input/output hubs. The input/output hub **1320** may provide various interfaces with the devices. For example, the input/output hub **1320** may provide an accelerated graphics port (AGP) interface, a peripheral component interface-express (PCIe), a communications streaming architecture (CSA) interface, etc.

[0130] The graphics card **1350** may be coupled to the input/output hub **1320** via AGP or PCIe. The graphics card **1350** may control a display device (not shown) for displaying an image. The graphics card **1350** may include an internal processor for processing image data and an internal memory device. In some embodiments, the input/output hub **1320** may include an internal graphics device along with or instead of the graphics card **1350** outside the graphics card **1350**. The graphics device included in the input/output hub **1320** may be referred to as integrated graphics. Further, the input/output hub **1320** including the internal memory controller and the internal graphics device may be referred to as a graphics and memory controller hub (GMCH).

[0131] The input/output controller hub **1330** may perform data buffering and interface arbitration to efficiently operate various system interfaces. The input/output controller hub **1330** may be coupled to the input/output hub **1320** via an internal bus, such as a direct media interface (DMI), a hub interface, an enterprise Southbridge interface (ESI), PCIe, etc. The input/output controller hub **1330** may provide various interfaces with peripheral devices. For example, the input/output controller hub **1330** may provide a universal serial bus (USB) port, a serial advanced technology attachment (SATA) port, a general purpose input/output (GPIO), a low pin count (LPC) bus, a serial peripheral interface (SPI), PCI, PCIe, etc.

[0132] In some embodiments, the processor **1310**, the input/output hub **1320** and the input/output controller hub **1330** may be implemented as separate chipsets or separate integrated units. In other embodiments, at least two of the processor **1310**, the input/output hub **1320** and the input/output controller hub **1330** may be implemented as a single chipset. Also, while many features of the embodiments are disclosed as units, in other embodiments those features may be implemented as other forms of logic including but not limited to code-based operations performed by a processor.

[0133] The memory system and the method of operating the memory system according to example embodiments may reduce a CAS-to-CAS delay time (tCCD) or maintain the tCCD in a minimum value by adopting an operation for mixing two commands. Through the reduction of the tCCD, a DQ bubble, in which data transfer is not performed continuously, may be prevented and utilization of a data bus may be enhanced.

[0134] The embodiments described herein may be applied to arbitrary devices and systems including a memory device. For example, the embodiments may be applied to a mobile phone, a smart phone, a personal digital assistant (PDA), a portable multimedia player (PM P), a digital camera, a camcorder, personal computer (PC), a server computer, a workstation, a laptop computer, a digital TV, a set-top box, a portable game console, a navigation system, etc.

[0135] In accordance with another embodiment, an apparatus includes an interface coupled to a memory. The interface may be one or more of signal or bus lines corresponding to the aforementioned embodiments. The memory controller selectively operates in a first mode and a second mode. The memory controller transmits a first command continuously through the interface during a plurality of clock cycles in the first mode. The memory controller mixes a second command with the first command and transmits the mixture of the first command and the second command through the interface in the second mode. The memory controller may insert the second

command between the clock cycles of the first command in the second mode. The memory controller may include flag information in the first command transmitted through the interface to the memory, wherein the flag information is indicative of a change in command latch timing for the memory. The memory controller may correspond to the memory controller in any of the aforementioned embodiments.

[0136] The methods, processes, and/or operations described herein may be performed by code or instructions to be executed by a computer, processor, controller, or other signal processing device. The computer, processor, controller, or other signal processing device may be those described herein or one in addition to the elements described herein. Because the algorithms that form the basis of the methods (or operations of the computer, processor, controller, or other signal processing device) are described in detail, the code or instructions for implementing the operations of the method embodiments may transform the computer, processor, controller, or other signal processing device into a special-purpose processor for performing the methods herein.

[0137] The controllers, control logic, decoders, and other processing features of the embodiments described herein may be implemented in logic which, for example, may include hardware, software, or both. When implemented at least partially in hardware, the controllers, control logic, decoders, and processing features may be, for example, any one of a variety of integrated circuits including but not limited to an application-specific integrated circuit, a field-programmable gate array, a combination of logic gates, a system-on-chip, a microprocessor, or another type of processing or control circuit.

[0138] When implemented in at least partially in software, the controllers, control logic, decoders, and other processing features may include, for example, a memory or other storage device for storing code or instructions to be executed, for example, by a computer, processor, microprocessor, controller, or other signal processing device. The computer, processor, microprocessor, controller, or other signal processing device may be those described herein or one in addition to the elements described herein. Because the algorithms that form the basis of the methods (or operations of the computer, processor, microprocessor, controller, or other signal processing device) are described in detail, the code or instructions for implementing the operations of the method embodiments may transform the computer, processor, controller, or other signal processing device into a special-purpose processor for performing the methods herein.

[0139] Example embodiments have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. In some instances, as would be apparent to one of skill in the art as of the filing of the present application, features, characteristics, and/or elements described in connection with a particular embodiment may be used singly or in combination with features, characteristics, and/or elements described in connection with other embodiments unless otherwise indicated. Accordingly, it will be understood by those of skill in the art that various changes in form and details may be made without departing from the spirit and scope of the embodiments set forth in the claims.

## Claims

**1.** A memory device, comprising: a memory cell array including a plurality of memory cells; and a control logic configured to: receive an active command through a plurality of command-address signals and a chip select signal from a memory controller, the active command including a first portion and a second portion, the plurality of command-address signals of the first portion including a plurality of bank address bits, the plurality of command-address signals of the second portion including a plurality of row address bits; and receive a column address strobe (CAS) command between the first portion and the second portion, through the plurality of command-address signals and the chip select signal from the memory controller.

2. The memory device as claimed in claim 1, wherein the memory device is configured to receive a clock signal from the memory controller, and the control logic is configured to receive the second portion within predetermined clock cycles of the clock signal from the first portion.

3. The memory device as claimed in claim 1, wherein the memory device is configured to receive a clock signal from the memory controller, and the control logic is configured to receive the second portion within 4*N clock cycles of the clock signal from the first portion, N being a positive integer.

4. The memory device as claimed in claim 1, wherein the memory device is configured to activate a word line corresponding to the plurality of bank address bits and the plurality of row address bits.

5. The memory device as claimed in claim 1, wherein the plurality of bank address bits include at least three bank address bits.

6. The memory device as claimed in claim 1, wherein the CAS command is a read command or a write command.

7. The memory device as claimed in claim 6, wherein the plurality of command-address signals of the CAS command include the plurality of bank address bits and a plurality of column address bits.

8. The memory device as claimed in claim 1, wherein logic levels of the plurality of command-address signals and the chip select signal received at a rising edge of a clock signal from the memory controller indicate the first portion and the second portion.

9. The memory device as claimed in claim 2, wherein the control logic is configured to receive a second CAS command after the second portion of the active command, through the plurality of command-address signals and the chip select signal from the memory controller.

10. The memory device as claimed in claim 9, wherein: a CAS-to-CAS delay time (tCCD) indicates a time duration between the CAS command and the second CAS command, and the tCCD is about 4 clock cycles of the clock signal.

11. A memory device, comprising: a memory cell array including a plurality of memory cells; and a control logic configured to: receive a first active command through a plurality of command-address signals and a chip select signal from a memory controller, the first active command including a first portion and a second portion, the plurality of command-address signals of the first portion including a plurality of first bank address bits, the plurality of command-address signals of the second portion including a plurality of first row address bits; receive a second active command after the first active command through the plurality of command-address signals and the chip select signal from the memory controller, the second active command including a third portion and a fourth portion, the plurality of command-address signals of the third portion including a plurality of second bank address bits, the plurality of command-address signals of the fourth portion including a plurality of second row address bits; and receive a first column address strobe (CAS) command between the first portion and the second portion, through the plurality of command-address signals and the chip select signal from the memory controller.

12. The memory device as claimed in claim 11, wherein the memory device is configured to receive a clock signal from the memory controller, and the control logic is configured to receive the second portion within 4*N clock cycles of the clock signal from the first portion, and receive the fourth portion within the 4*N clock cycles from the third portion, N being a positive integer.

13. The memory device as claimed in claim 11, wherein the plurality of command-address signals of the first CAS command includes the plurality of first bank address bits and a plurality of first column address bits.

14. The memory device as claimed in claim 13, wherein the control logic is configured to receive a second CAS command after the fourth portion, through the plurality of command-address signals and the chip select signal from the memory controller, and wherein the plurality of command-address signals of the second CAS command includes the plurality of second bank address bits and a plurality of second column address bits.

15. The memory device as claimed in claim 11, wherein the plurality of first bank address bits

included in the first portion are equivalent to the plurality of second bank address bits included in the third portion.

**16**. The memory device as claimed in claim 11, wherein the memory device is configured to activate a first word line corresponding to the plurality of first bank address bits and the plurality of first row address bits, and activate a second word line corresponding to the plurality of second bank address bits and the plurality of second row address bits.

**17**. A memory system, comprising: a memory controller configured to generate a clock signal; and a memory device, including: a memory cell array having a plurality of memory cells; and a control logic configured to: receive an active command through a plurality of command-address signals and a chip select signal from the memory controller, the active command including a first portion and a second portion, the plurality of command-address signals of the first portion including a plurality of bank address bits, the plurality of command-address signals of the second portion including a plurality of row address bits; and receive a column address strobe (CAS) command between the first portion and the second portion, through the plurality of command-address signals and the chip select signal from the memory controller.

**18**. The memory system as claimed in claim 17, wherein the memory device is configured to receive the clock signal from the memory controller, and the control logic is configured to receive the second portion within 4*N clock cycles of the clock signal from the first portion, N being a positive integer.

**19**. The memory system as claimed in claim 17, wherein the memory device is configured to receive the clock signal from the memory controller, and the control logic is configured to receive the second portion within 8 clock cycles of the clock signal from the first portion.

**20**. The memory system as claimed in claim 17, wherein logic levels of the plurality of command-address signals and the chip select signal received at a rising edge of the clock signal indicate the first portion and the second portion.