US 20250266823A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2025/0266823 A1**

JANG et al. (43) **Pub. Date: Aug. 21, 2025**

(54) **SYSTEM-ON-CHIP FOR POWER MANAGEMENT IN MULTI-DIE STRUCTURE**

(71) Applicant: **Samsung Electronics Co., Ltd.**, Suwon-si (KR)

(72) Inventors: **Taehong JANG**, Suwon-si (KR); **Sungcheol PARK**, Suwon-si (KR); **Jehyun PARK**, Suwon-si (KR)

(73) Assignee: **Samsung Electronics Co., Ltd.**, Suwon-si (KR)

(21) Appl. No.: **19/014,859**

(22) Filed: **Jan. 9, 2025**

(30) **Foreign Application Priority Data**

Feb. 15, 2024 (KR) 10-2024-0021798
Apr. 11, 2024 (KR) 10-2024-0048933

Publication Classification

(51) **Int. Cl.**
H03K 17/20 (2006.01)
H03K 19/0175 (2006.01)
H03K 19/20 (2006.01)

(52) **U.S. Cl.**
CPC ***H03K 17/20*** (2013.01); ***H03K 19/017545*** (2013.01); ***H03K 19/20*** (2013.01)

(57) **ABSTRACT**

A system-on-chip (SoC) including a first die and a second die adjacent to a surface of the first die, the second die connected to the first die. The first die may include a first reset circuit configured to output a first reset signal to operate the first die based on a first voltage received from a power supply, and the second die may include a second reset circuit configured to output a second reset signal to operate the second die based on a second voltage received from the power supply.

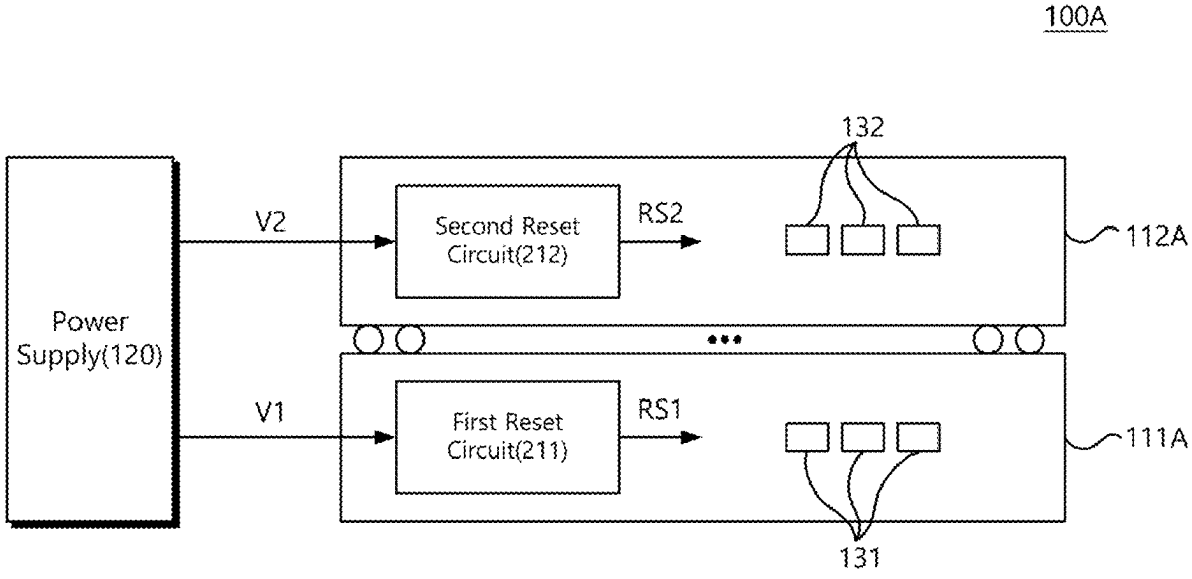


FIG. 1

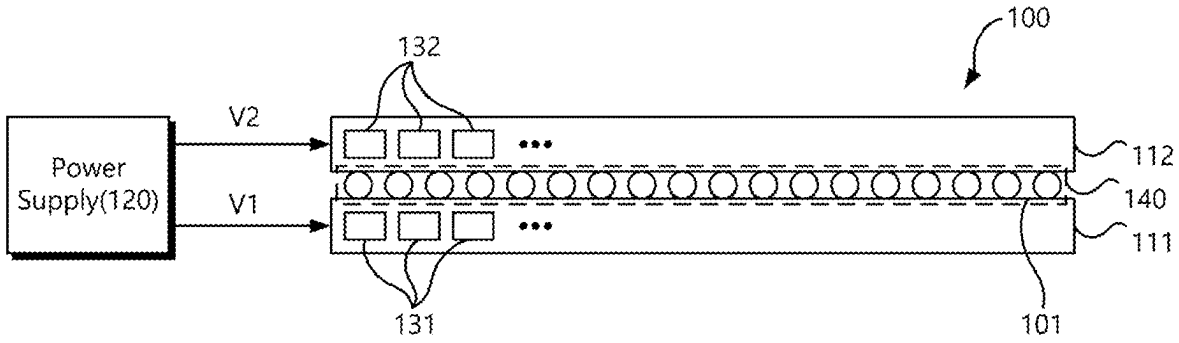


FIG. 2

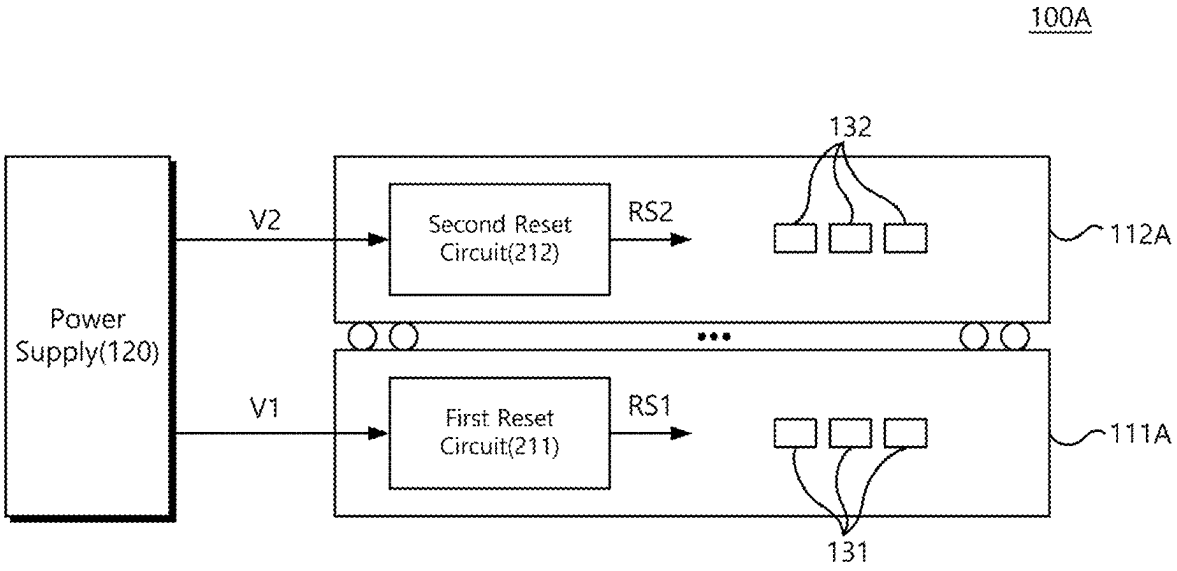

100A
132
Power Supply(120)
V2
Second Reset Circuit(212)
RS2
112A
V1
First Reset Circuit(211)
RS1
111A
131

FIG. 3

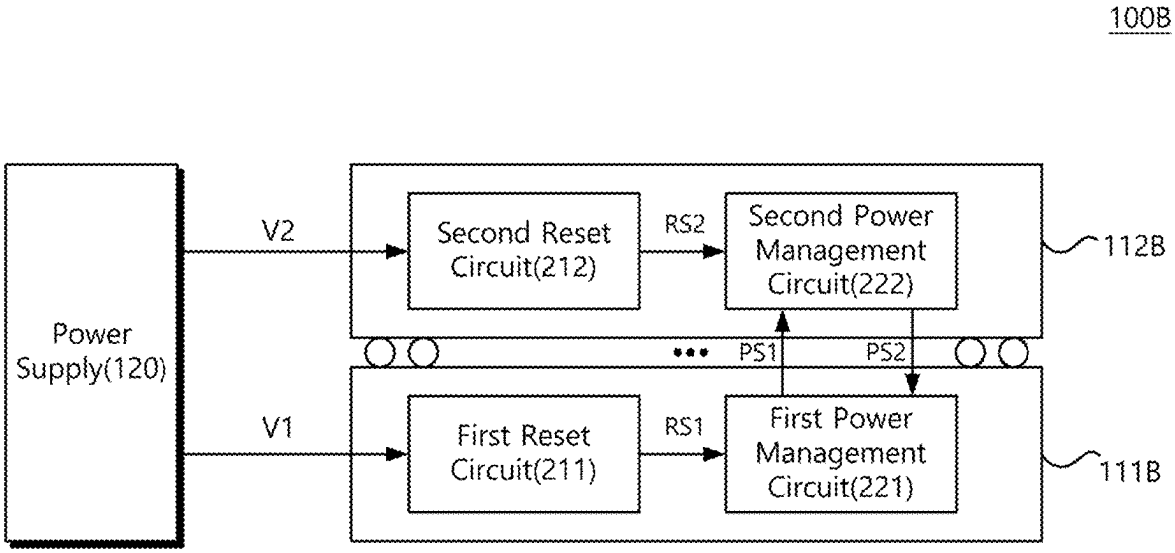

100B
Power Supply(120)
V2
V1
Second Reset Circuit(212)
RS2
Second Power Management Circuit(222)
112B
PS1
PS2
First Reset Circuit(211)
RS1
First Power Management Circuit(221)
111B

FIG. 4

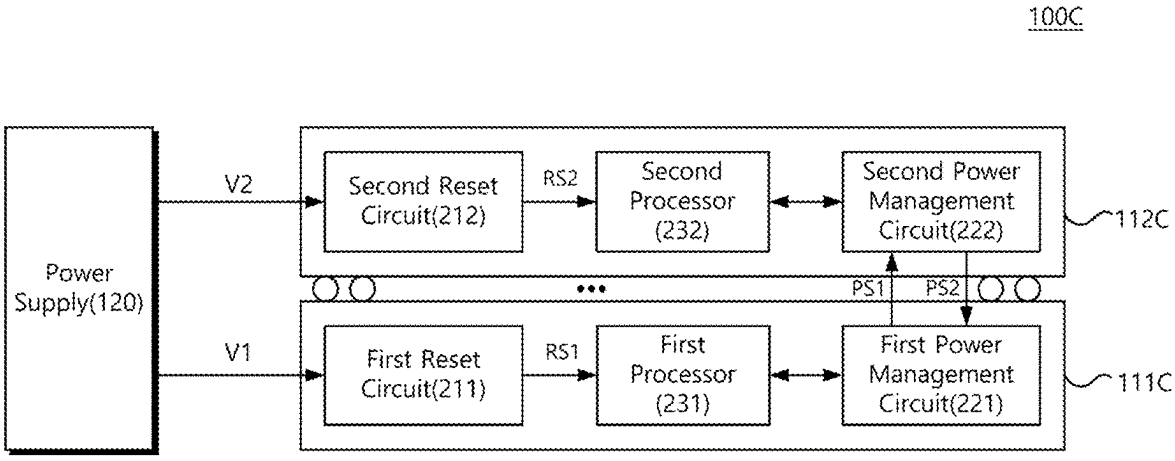

100C
Power Supply(120)
V2
V1
Second Reset Circuit(212)
RS2
Second Processor (232)
Second Power Management Circuit(222)
112C
PS1
PS2
First Reset Circuit(211)
RS1
First Processor (231)
First Power Management Circuit(221)
111C

FIG. 5A

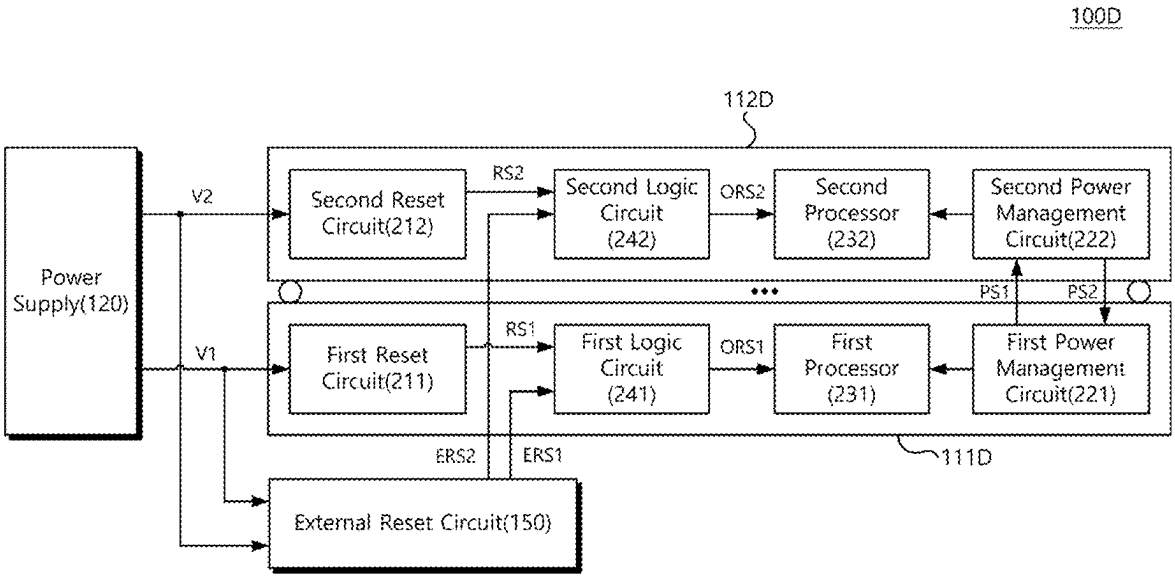

100D
112D
Power Supply(120)
V2
V1
Second Reset Circuit(212)
RS2
Second Logic Circuit (242)
ORS2
Second Processor (232)
Second Power Management Circuit(222)
PS1
PS2
First Reset Circuit(211)
RS1
First Logic Circuit (241)
ORS1
First Processor (231)
First Power Management Circuit(221)
111D
ERS2
ERS1
External Reset Circuit(150)

FIG. 5B

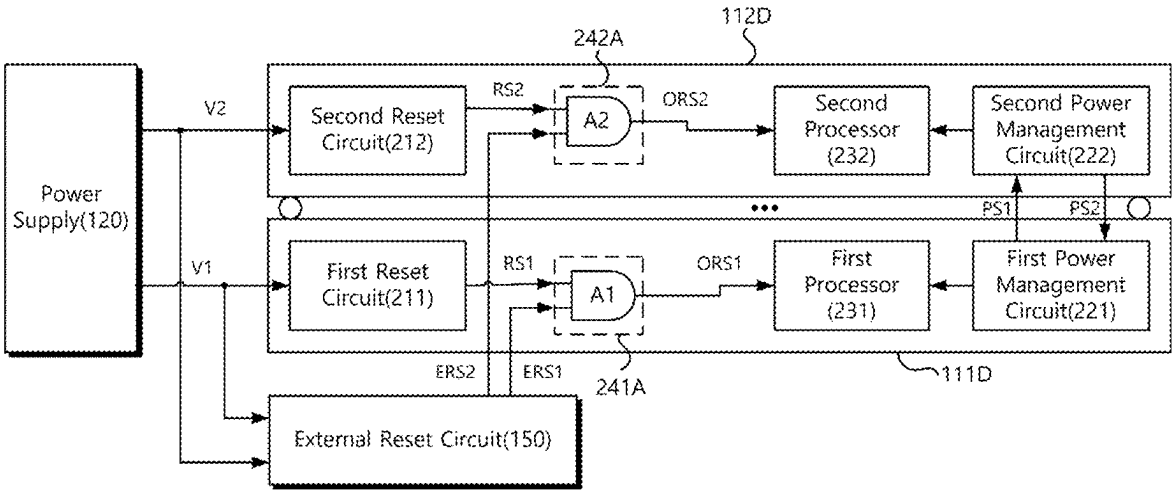

112D
242A
Power Supply(120)
V2
V1
Second Reset Circuit(212)
RS2
A2
ORS2
Second Processor (232)
Second Power Management Circuit(222)
PS1
PS2
First Reset Circuit(211)
RS1
A1
ORS1
First Processor (231)
First Power Management Circuit(221)
ERS2
ERS1
241A
111D
External Reset Circuit(150)

FIG. 5C

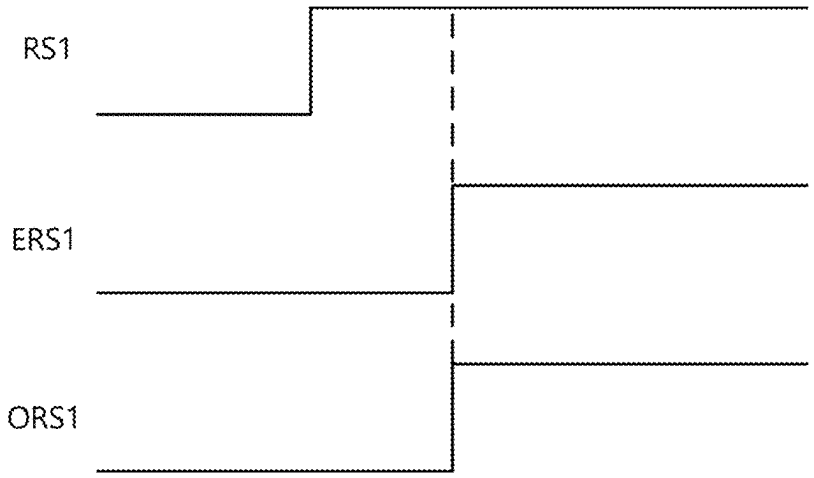


FIG. 5D

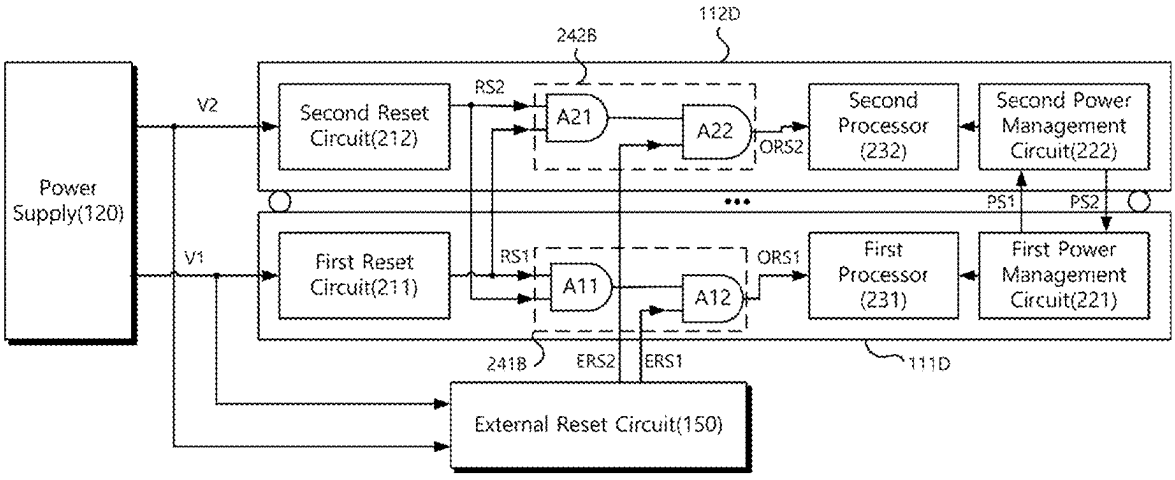

112D
242B
Power Supply(120)
V2
V1
Second Reset Circuit(212)
First Reset Circuit(211)
RS2
RS1
A21
A22
A11
A12
ORS2
ORS1
Second Processor (232)
First Processor (231)
Second Power Management Circuit(222)
First Power Management Circuit(221)
PS1
PS2
241B
ERS2
ERS1
111D
External Reset Circuit(150)

FIG. 6

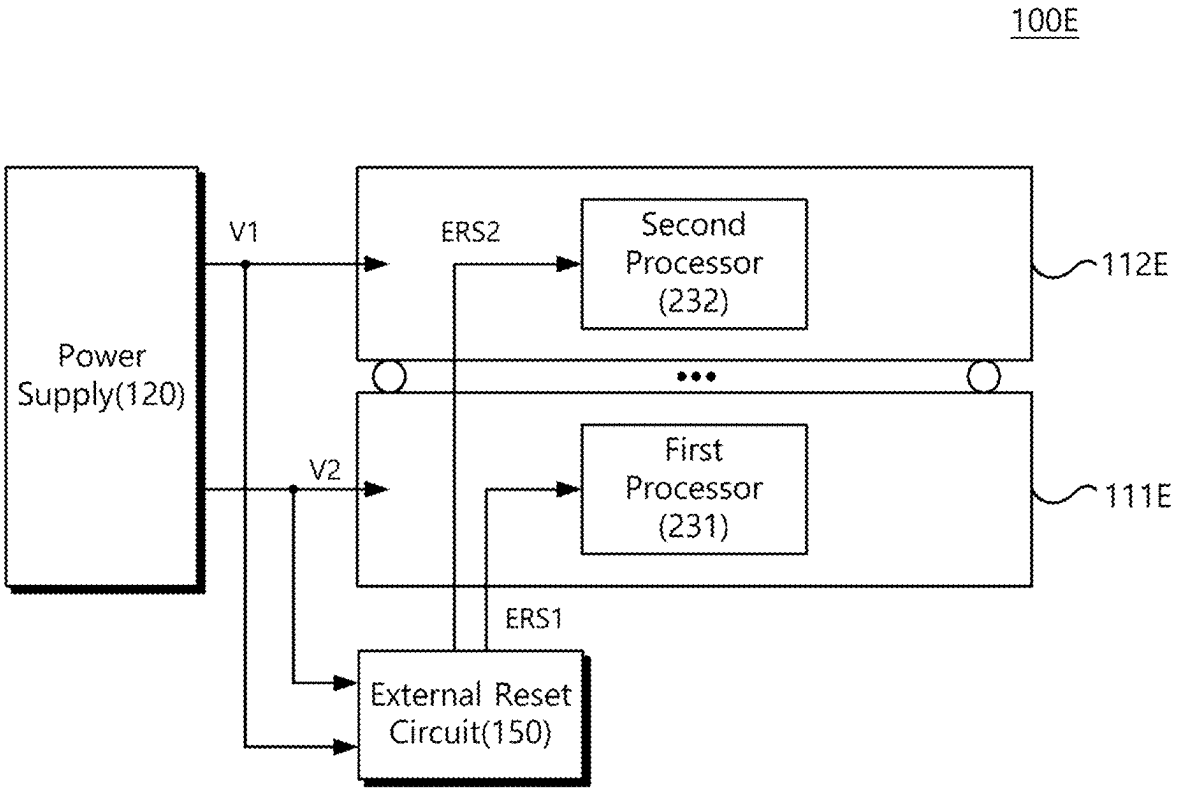

100E
Power Supply(120)
V1
V2
ERS2
ERS1
Second Processor (232)
First Processor (231)
112E
111E
External Reset Circuit(150)

FIG. 7

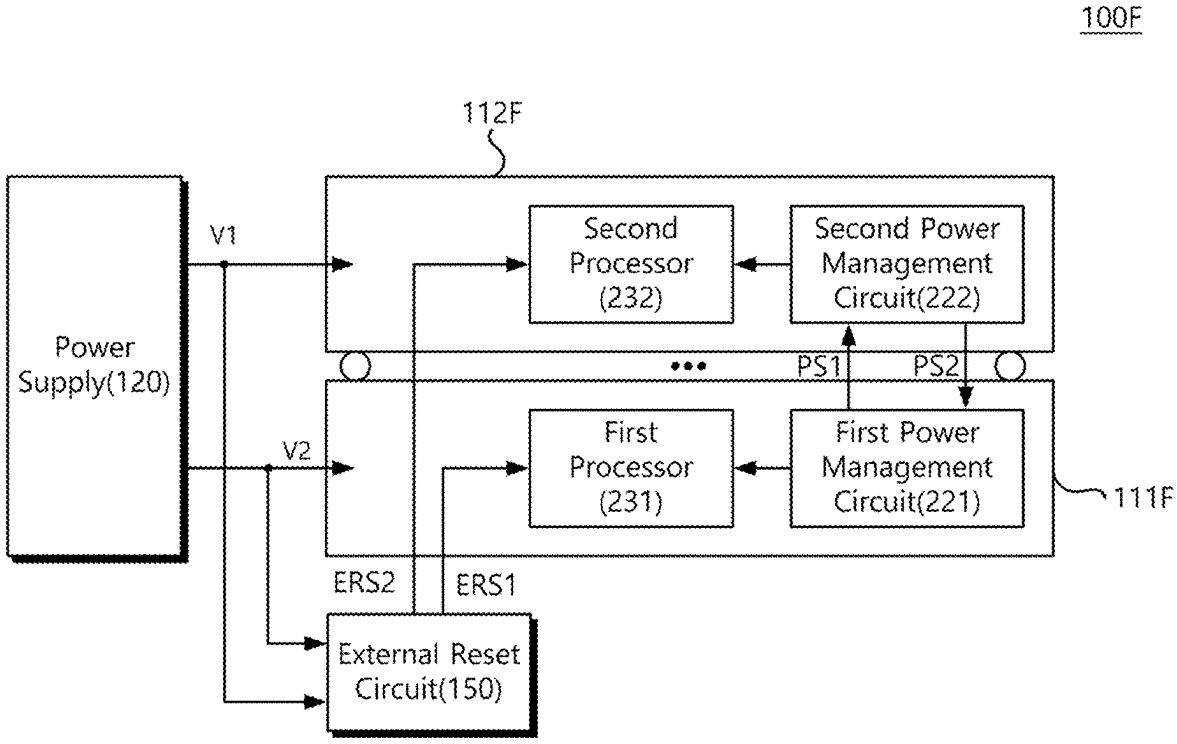

100F
112F
Power Supply(120)
V1
V2
Second Processor (232)
Second Power Management Circuit(222)
PS1
PS2
First Processor (231)
First Power Management Circuit(221)
111F
ERS2
ERS1
External Reset Circuit(150)

FIG. 8

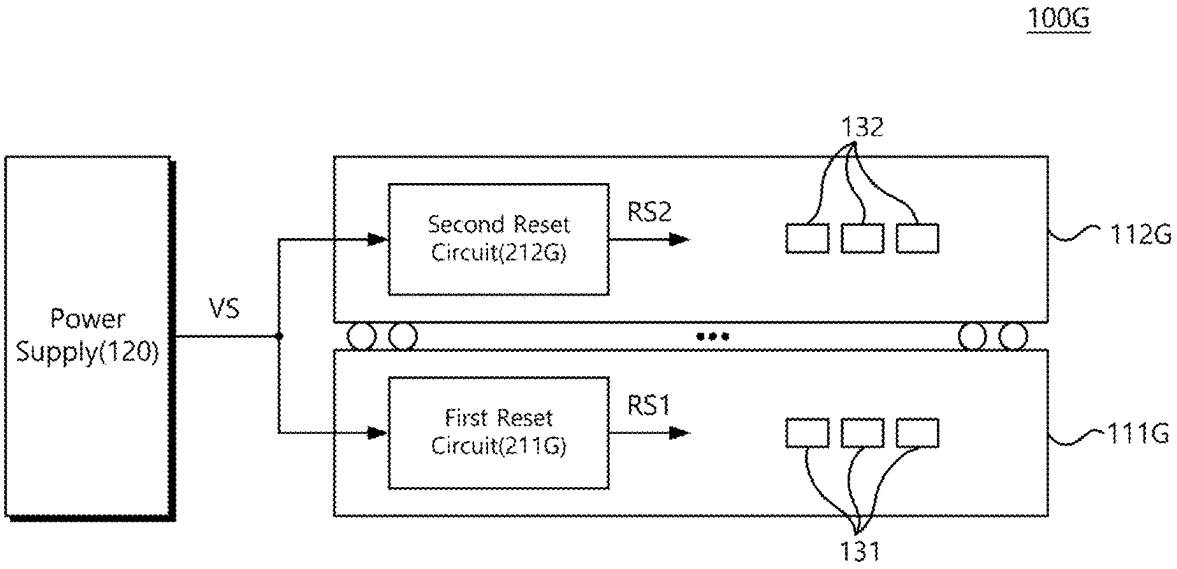

100G
132
Power Supply(120)
VS
Second Reset Circuit(212G)
RS2
112G
First Reset Circuit(211G)
RS1
111G
131

FIG. 9

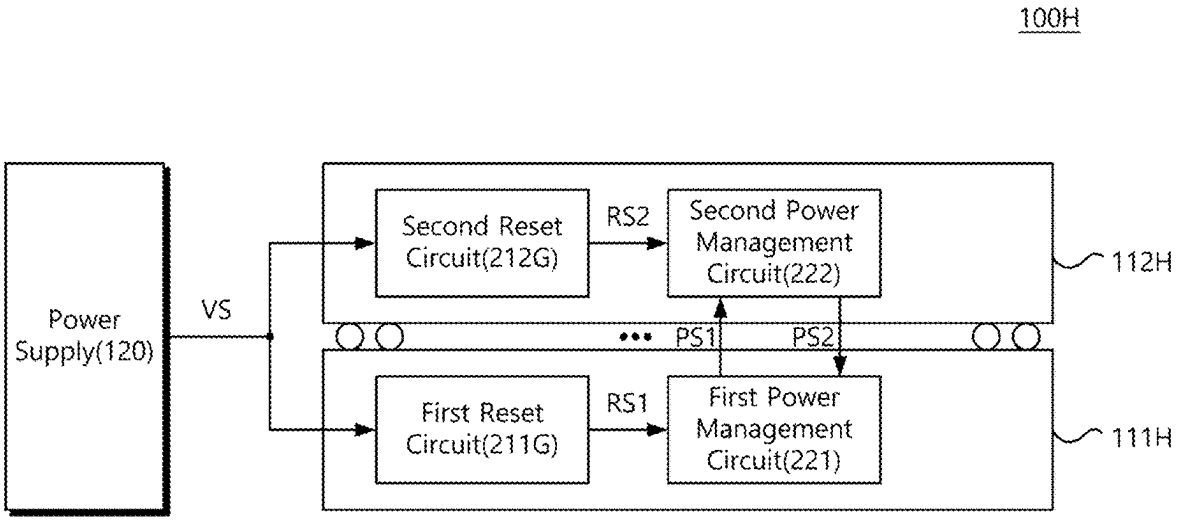

100H
Power Supply(120)
VS
Second Reset Circuit(212G)
RS2
Second Power Management Circuit(222)
112H
PS1
PS2
First Reset Circuit(211G)
RS1
First Power Management Circuit(221)
111H

FIG. 10

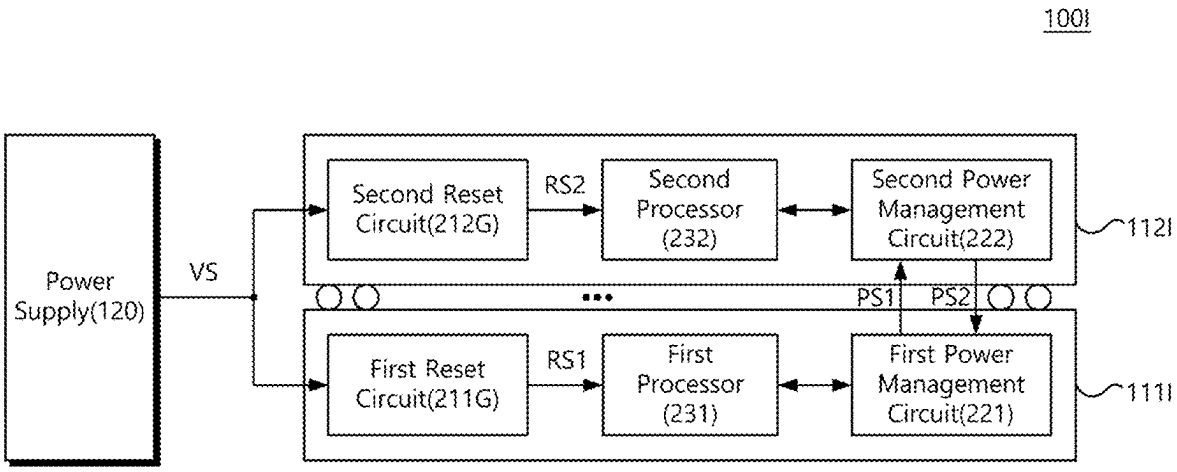

100I
Power Supply(120)
VS
Second Reset Circuit(212G)
RS2
Second Processor (232)
Second Power Management Circuit(222)
112I
PS1
PS2
First Reset Circuit(211G)
RS1
First Processor (231)
First Power Management Circuit(221)
111I

FIG. 11

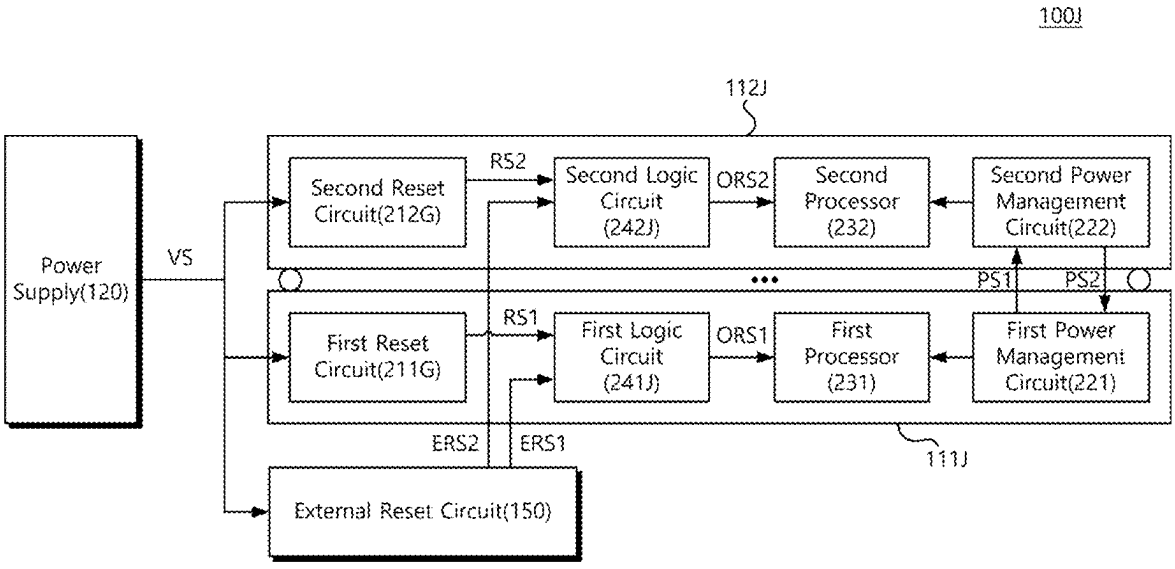

100J
112J
Power Supply(120)
VS
Second Reset Circuit(212G)
R52
Second Logic Circuit (242J)
ORS2
Second Processor (232)
Second Power Management Circuit(222)
PS1
PS2
First Reset Circuit(211G)
RS1
First Logic Circuit (241J)
ORS1
First Processor (231)
First Power Management Circuit(221)
111J
ERS2
ERS1
External Reset Circuit(150)

FIG. 12

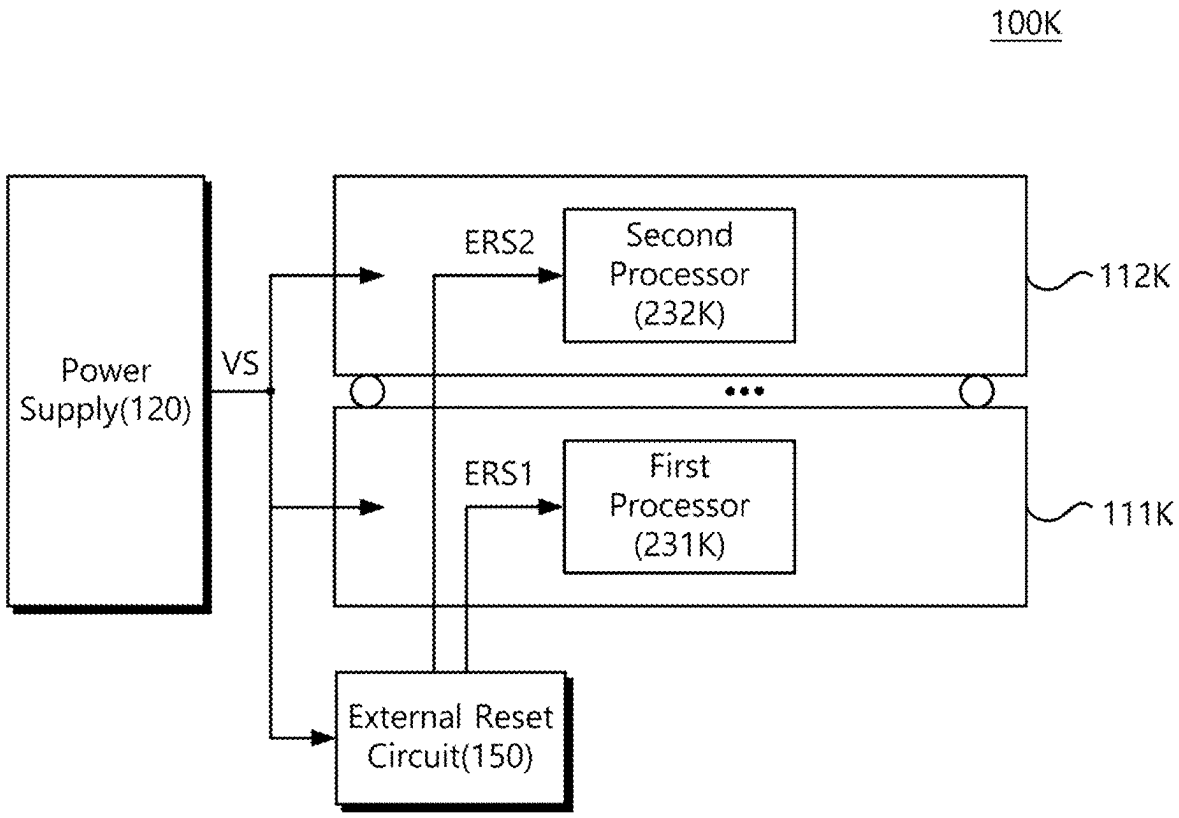

100K
Power Supply(120)
VS
ERS2
Second Processor (232K)
112K
ERS1
First Processor (231K)
111K
External Reset Circuit(150)

FIG. 13

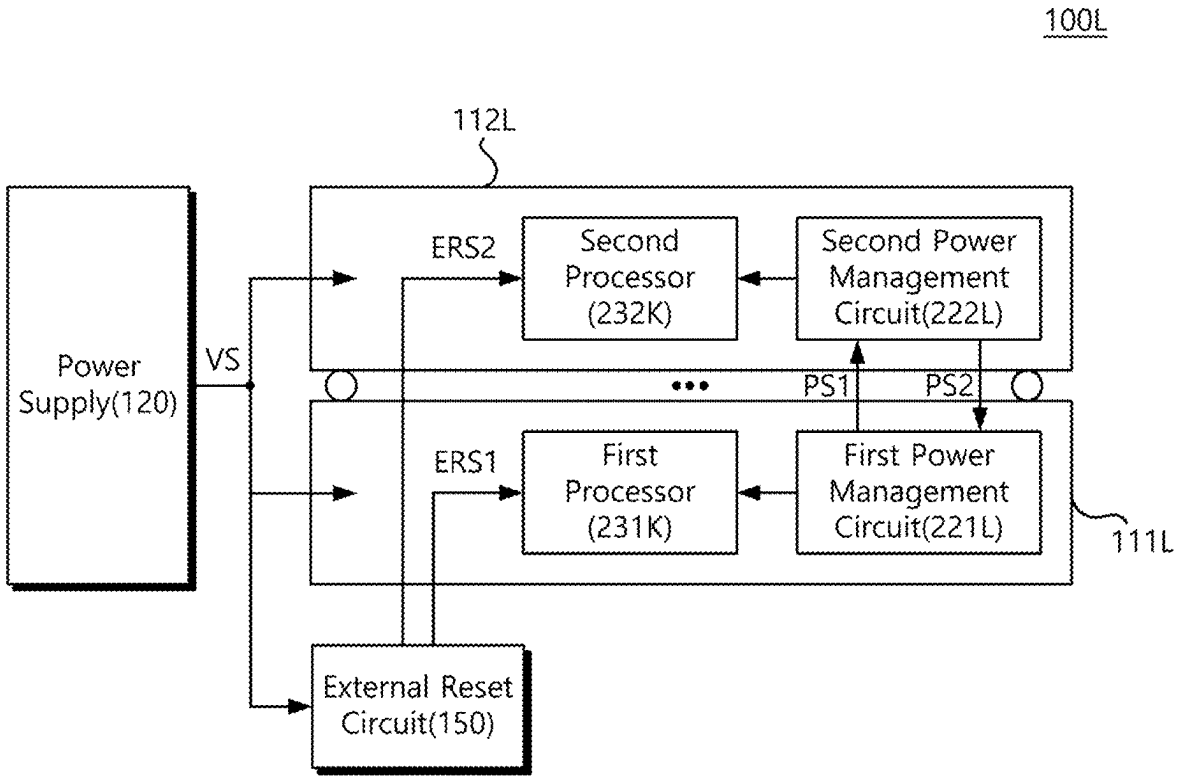

100L
112L
Power Supply(120)
VS
ERS2
Second Processor (232K)
Second Power Management Circuit(222L)
PS1
PS2
ERS1
First Processor (231K)
First Power Management Circuit(221L)
111L
External Reset Circuit(150)

FIG. 14A

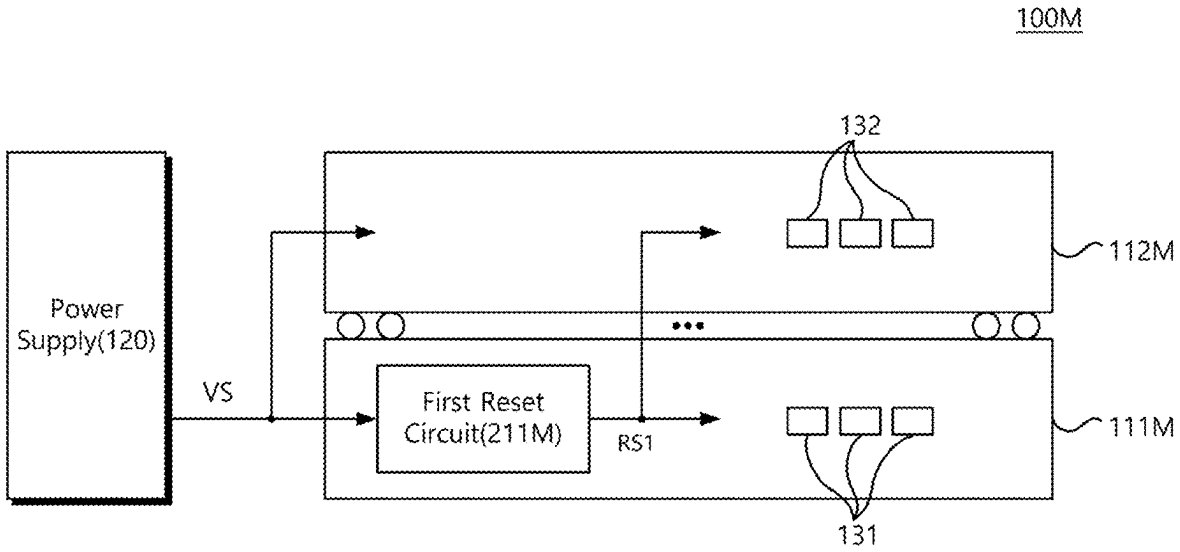

100M
132
112M
Power Supply(120)
VS
First Reset Circuit(211M)
RS1
111M
131

FIG. 14B

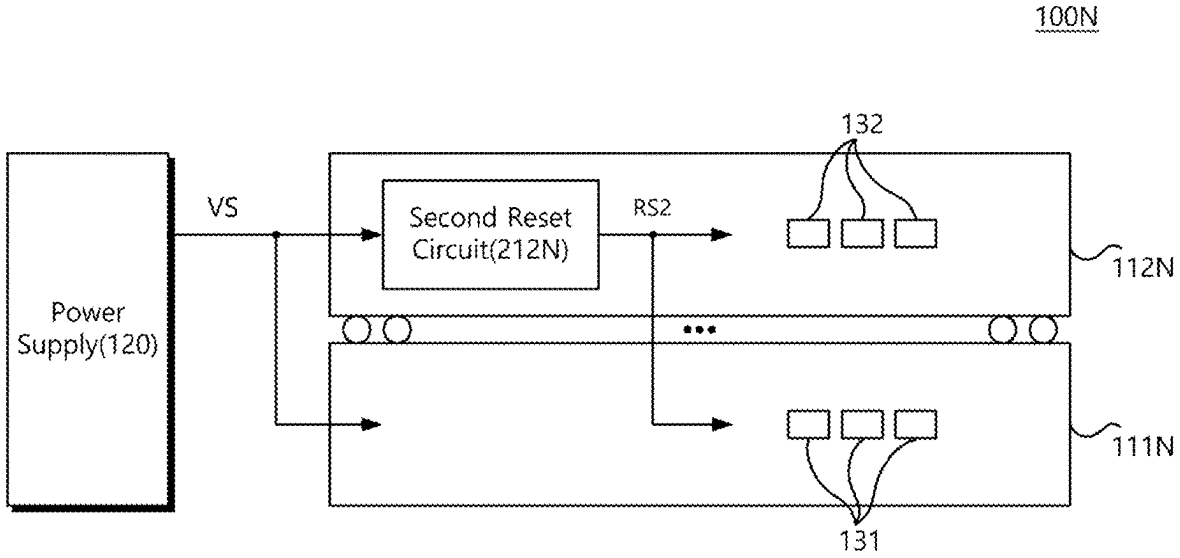

100N
132
VS
Second Reset Circuit(212N)
RS2
Power Supply(120)
112N
111N
131

FIG. 15A

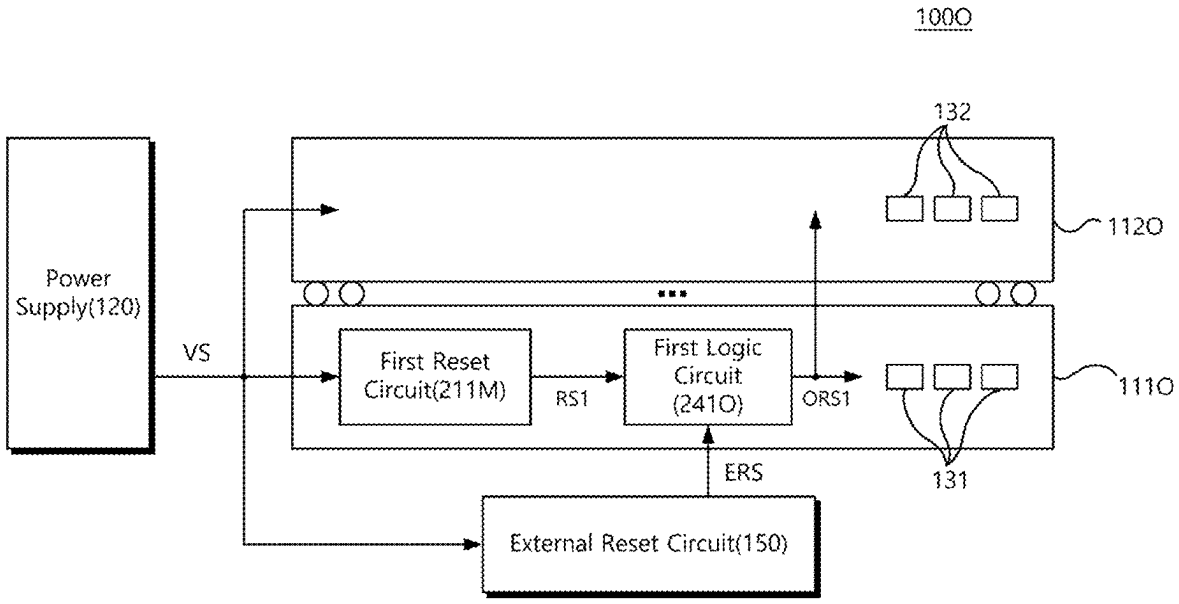

100O
132
112O
Power Supply(120)
VS
First Reset Circuit(211M)
RS1
First Logic Circuit (241O)
ORS1
111O
131
ERS
External Reset Circuit(150)

FIG. 15B

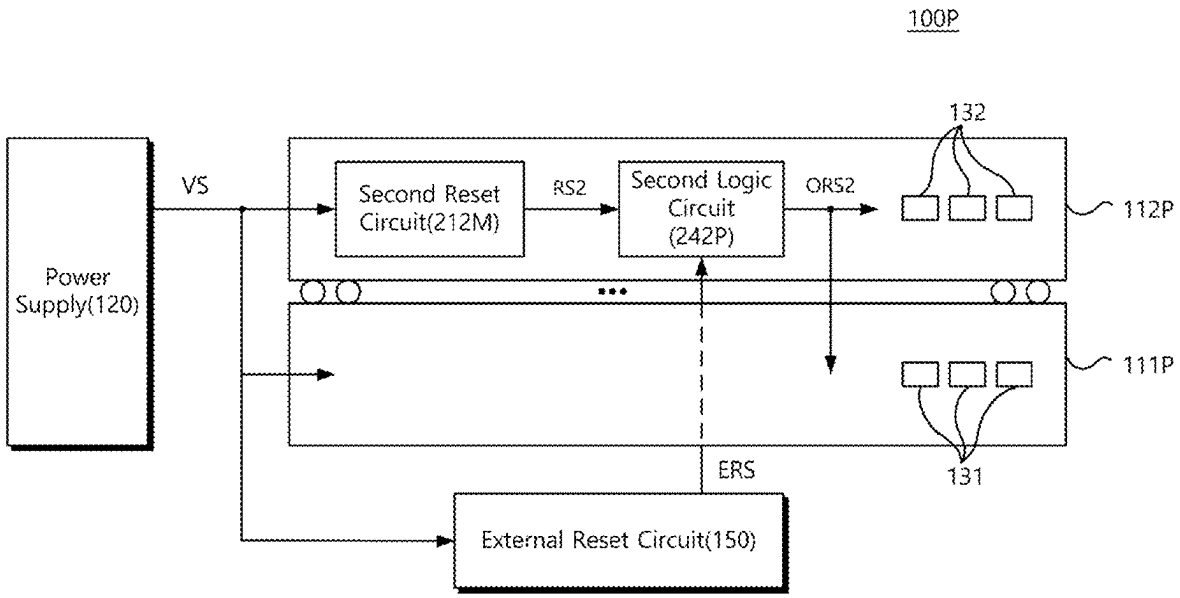
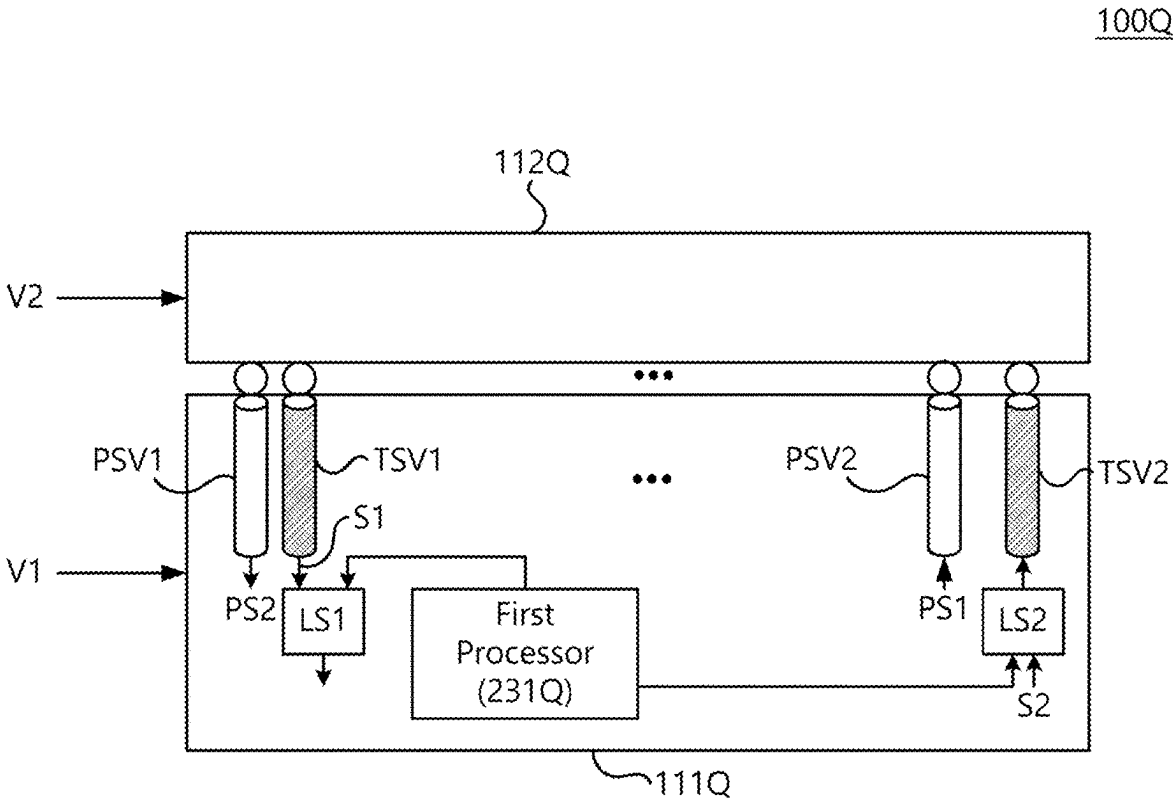

100P
132
VS
Second Reset Circuit(212M)
RS2
Second Logic Circuit (242P)
ORS2
112P
Power Supply(120)
111P
131
ERS
External Reset Circuit(150)

FIG. 16


100Q
112Q
V2
PSV1
TSV1
S1
V1
PS2
LS1
First
Processor
(231Q)
PSV2
TSV2
PS1
LS2
S2
111Q

SYSTEM-ON-CHIP FOR POWER MANAGEMENT IN MULTI-DIE STRUCTURE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This U.S. non-provisional application claims priority under 35 USC § 119 to Korean Patent Application No. 10-2024-0021798, filed on Feb. 15, 2024, and Korean Patent Application No. 10-2024-0048933, filed on Apr. 11, 2024, in the Korean Intellectual Property Office, the entire contents of each of which are herein incorporated by reference in their entirety.

BACKGROUND

[0002] Example embodiments relate to a system-on-chip for power management in a multi-die structure.

[0003] To meet the increasing market demand for higher performance in semiconductor devices, such as memory capacity or processing speed, research into three-dimensional integrated circuits (3D ICs) (or stacked memory devices) formed by stacking semiconductor dies is actively underway.

[0004] For example, research is being conducted to implement semiconductor devices formed by stacking a plurality of dies to include various functions in a smaller area.

[0005] In a 3D IC structure formed by stacking a plurality of dies, different levels of power (or voltage) may be supplied to the respective dies.

[0006] Due to the limitation of a configuration according to the related art to control power of a semiconductor device, it may be difficult to stably control power for the operation of each of the plurality of dies.

[0007] In addition, when different levels of power are supplied to the respective dies, issues may arise in an operation requiring an interaction between the plurality of dies.

SUMMARY

[0008] Example embodiments provide a system-on-chip for stably controlling power for the operation of each of a plurality of dies.

[0009] According to some example embodiments, a system-on-chip (SoC) includes a first die and a second die adjacent to a surface of the first die, the second die connected to the first die. The first die may include a first reset circuit configured to output a first reset signal to operate the first die based on a first voltage received from a power supply, and the second die may include a second reset circuit configured to output a second reset signal to operate the second die based on a second voltage received from the power supply.

[0010] According to some example embodiments, a system-on-chip (SoC) includes a first die, a second die adjacent to a surface of the first die, the second die connected to the first die through a plurality of pads on the surface of the first die, and an external reset circuit configured to output a first reset signal based on a first voltage received from a power supply, and output a second reset signal based on a second voltage received from the power supply. The first die may be configured to operate with the first voltage in response to the first reset signal, and the second die may be configured to operate with the second voltage in response to the second reset signal.

[0011] According to some example embodiments, a system-on-chip (SoC) includes a first die and a second die adjacent to a surface of the first die, the second die connected to the first die through a plurality of pads disposed on the surface of the first die. The first die may include a first reset circuit configured output a first reset signal to operate the first die based on a supply voltage received from a power supply, and the second die may include a second reset circuit configured to output a second reset signal, different from the first reset signal, to operate the second die based on the supply voltage.

BRIEF DESCRIPTION OF DRAWINGS

[0012] FIG. **1** is a diagram illustrating a system-on-chip having a multi-die structure according to some example embodiments.

[0013] FIG. **2** is a diagram illustrating a system-on-chip, in which a plurality of dies each include a reset circuit, according to some example embodiments.

[0014] FIG. **3** is a diagram illustrating a system-on-chip, in which a plurality of dies each further include a power management circuit, according to some example embodiments.

[0015] FIG. **4** is a diagram illustrating a system-on-chip, in which a plurality of dies each include a processor, according to some example embodiments.

[0016] FIG. **5**A is a diagram illustrating a system-on-chip, in which a plurality of dies each further include a logic circuit, according to some example embodiments.

[0017] FIG. **5**B is a diagram illustrating a system-on-chip, in which logic circuits each include an AND gate, according to some example embodiments.

[0018] FIG. **5**C is a diagram illustrating a configuration in which a first logic circuit of FIG. **5**B outputs a first output reset signal based on a first reset signal and a first external reset signal.

[0019] FIG. **5**D is a diagram illustrating a system-on-chip, in which logic circuits each includes a plurality of AND gates, according to some example embodiments.

[0020] FIG. **6** is a diagram illustrating a system-on-chip including an external reset circuit according to some example embodiments.

[0021] FIG. **7** is a diagram illustrating a system-on-chip, including an external reset circuit according to some example embodiments, in which a plurality of dies each include a power management circuit.

[0022] FIG. **8** is a diagram illustrating a system-on-chip, in which a reset circuit included in each die outputs different reset signals based on a supply voltage, according to some example embodiments.

[0023] FIG. **9** is a diagram illustrating a system-on-chip, in which a plurality of dies each further includes a power management circuit, according to some example embodiments.

[0024] FIG. **10** is a diagram illustrating a system-on-chip, in which each of the plurality of dies includes a processor, according to some example embodiments.

[0025] FIG. **11** is a diagram illustrating a system-on-chip, in which each of the plurality of dies further includes a logic circuit, according to some example embodiments.

[0026] FIG. **12** is a diagram illustrating a system-on-chip including an external reset circuit outputting an external reset signal based on a supply voltage according to some example embodiments.

[0027] FIG. **13** is a diagram illustrating a system-on-chip, including an external reset circuit according to some example embodiments, in which each die includes a power management circuit.

[0028] FIG. **14**A is a diagram illustrating a configuration in which a first die and a second die according to some example embodiments operate in response to a first reset signal generated from the first die.

[0029] FIG. **14**B is a diagram illustrating a configuration in which a first die and a second die according to some example embodiments operate in response to a second reset signal generated from the second die.

[0030] FIG. **15**A is a diagram illustrating a configuration in which a first die and a second die according to some example embodiments operate in response to a first output reset signal output from a first logic circuit.

[0031] FIG. **15**B is a diagram illustrating a configuration in which a first die and a second die according to some example embodiments operate in response to a second output reset signal output from a second logic circuit.

[0032] FIG. **16** is a diagram illustrating a system-on-chip in which a first die according to some example embodiments further includes a plurality of level shifters.

DETAILED DESCRIPTION

[0033] Hereinafter, some example embodiments will be described with reference to the accompanying drawings.

[0034] The terms, such as "first," "second," or the like, may represent various elements regardless of order and/or importance. Such terms may only be used to distinguish one element from another element, and do not limit the order and/or importance of the elements.

[0035] FIG. **1** is a diagram illustrating a system-on-chip having a multi-die structure according to some example embodiments.

[0036] Referring to FIG. **1**, a system-on-chip (SoC) **100** according to some example embodiments may include a first die **111** and a second die **112**.

[0037] For example, the system-on-chip **100** may include a first die **111** including a plurality of first intellectual property (IP) blocks **131**. In some example embodiments, the system-on-chip **100** may include a second die **112** including a plurality of second IP blocks **132**.

[0038] For example, the plurality of first IP blocks **131** and the plurality of second IP blocks **132** may each be understood as an electronic circuit performing a designated function or executing a designated application. In some example embodiments, any devices, electronic devices, modules, units, and/or portions thereof according to any of the example embodiments, and/or any portions thereof, including, without limitation, the plurality of first IP blocks **131** and the plurality of second IP blocks **132** may include, may be included in, and/or may be implemented by one or more instances of processing circuitry such as hardware including logic circuits; a hardware/software combination such as a processor executing software; or a combination thereof.

[0039] For example, a portion of the plurality of first IP blocks **131** and the plurality of second IP blocks **132** may be referred to as a processor or a power management unit (PMU), but example embodiments are not limited thereto.

[0040] For example, at least a portion of the plurality of first IP blocks **131** and the plurality of second IP blocks **132** may execute applications supported by the system-on-chip **100**. Accordingly, in some example embodiments, at least a portion of the plurality of first IP blocks **131** and the plurality of second IP blocks **132** may also be referred to as an application processor (AP), or the like.

[0041] According to some example embodiments, the second die **112** may be disposed adjacent to a first surface **101** of the first die **111**. For example, the second die **112** may be disposed adjacent to the first surface **101** of the first die **111** to be connected to the first die **111**.

[0042] For example, the second die **112** may be connected to the first die **111** through a plurality of pads **140** disposed on the first surface **101** of the first die **111**.

[0043] For example, the second die **112** may be stacked on the first surface **101** of the first die **111**.

[0044] Accordingly, in some example embodiments the system-on-chip **100** including a plurality of dies **111** and **112** implemented to be stacked may be understood to have a three-dimensional integrated circuit (3D IC) structure.

[0045] The plurality of dies **111** and **112** according to some example embodiments may operate using different voltages (or powers) V**1** and V**2** transmitted, transferred, or sent from a power supply **120**, respectively.

[0046] For example, the first die **111** may operate using a first voltage V**1** transmitted, transferred, or sent from the power supply **120**. For example, the first die **111** may operate at least a portion of the plurality of first IP blocks **131** using the first voltage V**1** transmitted, transferred, or sent from the power supply **120**.

[0047] The second die **112** may operate using a second voltage V**2** transmitted, transferred, or sent from the power supply **120**. For example, the second die **112** may operate at least a portion of the plurality of second IP blocks **132** using the second voltage V**2** transmitted, transferred, or sent from the power supply **120**.

[0048] For example, the first voltage V**1** and the second voltage V**2** may have different values, but example embodiments are not limited thereto.

[0049] For example, the stacked dies **111** and **112** may operate using different voltages V**1** and V**2** supplied from the power supply **120**, respectively.

[0050] Thus, in some example embodiments, the system-on-chip **100** may independently control power for the operation of each of the stacked dies **111** and **112** using different voltages.

[0051] FIG. **2** is a diagram illustrating a system-on-chip, in which a plurality of dies each include a reset circuit, according to some example embodiments.

[0052] Referring to FIG. **2**, a system-on-chip SoC **100**A may include a plurality of dies **111**A and **112**A, respectively including reset circuits **211** and **212**.

[0053] The system-on-chip **100**A illustrated in FIG. **2** may be understood as an example of the system-on-chip **100** illustrated in FIG. **1**. Therefore, the same or substantially the same components are denoted by the same or substantially the same reference numerals, and redundant descriptions are omitted to avoid repetition.

[0054] Elements and/or properties thereof that are "substantially identical" to, "substantially the same" as or "substantially equal" to other elements and/or properties thereof will be understood to include elements and/or properties thereof that are identical to, the same as, or equal to the other elements and/or properties thereof within manufacturing tolerances and/or material tolerances. Elements and/or properties thereof that are identical or substantially identical to and/or the same or substantially the same as other elements

and/or properties thereof may be structurally the same or substantially the same, functionally the same or substantially the same, and/or compositionally the same or substantially the same.

[0055] According to some example embodiments, the first die **111**A may include a first reset circuit **211**. For example, the first die **111**A may include a first reset circuit **211** outputting a first reset signal RS**1** in response to a first voltage V**1** transmitted, transferred, or sent from a power supply **120**.

[0056] According to some example embodiments, the first reset circuit **211** may output the first reset signal RS**1** in response to the first voltage V**1** being stabilized.

[0057] For example, the first reset circuit **211** may output the first reset signal RS**1** in response to a change amount (e.g., a change in an amount) of the first voltage V**1** being less than a threshold value for a unit time.

[0058] The second die **112**A may include a second reset circuit **212**. For example, the second die **112**A may include a second reset circuit **212** outputting a second reset signal RS**2** in response to a second voltage V**2** transmitted, transferred, or sent from the power supply **120**.

[0059] The second reset circuit **212** according to some example embodiments may output the second reset signal RS**2** in response to the second voltage V**2** being stabilized.

[0060] For example, the second reset circuit **212** may output the second reset signal RS**2** in response to a change amount of the second voltage V**2** being less than a threshold value for a unit time.

[0061] The multiple dies **111**A and **112**A according to some example embodiments may operate in response to the reset signals RS**1** and RS**2**, respectively.

[0062] For example, the first die **111**A may operate using the first voltage V**1** in response to the first reset signal RS**1**.

[0063] For example, the first die **111**A may operate at least a portion of the plurality of first IP blocks **131** using the first voltage V**1** in response to the first reset circuit **211** outputting a first reset signal RS**1** having a high level.

[0064] In some example embodiments, the second die **112**A may operate using the second voltage V**2** in response to the second reset signal RS**2**.

[0065] For example, the second die **112**A may operate at least a portion of the plurality of second IP blocks **132** using the second voltage V**2** in response to the second reset circuit **212** outputting a second reset signal RS**2** having a high level.

[0066] Referring to the above-described configurations, the system-on-chip **100**A according to some example embodiments may include reset circuits **211** and **212**, respectively provided in the plurality of dies **111**A and **112**A.

[0067] In some example embodiments, the system-on-chip **100**A may output different reset signals RS**1** and RS**2** for the plurality of dies **111**A and **112**A using reset circuits **211** and **212**.

[0068] As a result, the system-on-chip **100**A according to some example embodiments may independently and stably control a power-on reset operation for each of the plurality of dies **111**A and **112**A.

[0069] Furthermore, in some example embodiments, the system-on-chip **100**A may stably control power for the operation of each of the plurality of dies **111**A and **112**A through the above-described configurations.

[0070] FIG. **3** is a diagram illustrating a system-on-chip, in which a plurality of dies each further include a power management circuit, according to some example embodiments. FIG. **4** is a diagram illustrating a system-on-chip, in which a plurality of dies each include a processor, according to some example embodiments.

[0071] Referring to FIG. **3**, a system-on-chip **100**B according to some example embodiments may include a first die **111**B and a second die **112**B. The first die **111**B and the second die **112**B may include reset circuits **211** and **212** and power management circuits **221** and **222**, respectively.

[0072] The system-on-chip **100**B illustrated in FIG. **3** may be understood as an example embodiments that further includes power management circuits **221** and **222**, in addition to the configuration of the system-on-chip **100**A illustrated in FIG. **2**. Therefore, the same or substantially the same components are denoted by the same or substantially the same reference numerals, and redundant descriptions are omitted to avoid repetition.

[0073] According to some example embodiments, the first die **111**B may include a first power management circuit **221**.

[0074] For example, the first power management circuit **221** may transmit, transfer, or send first power information PS**1** to the second die **112**B. In some example embodiments, the first power management circuit **221** may receive second power information PS**2** from the second die **112**B.

[0075] The second die **112**B may include a second power management circuit **222**.

[0076] For example, the second power management circuit **222** may transmit, transfer, or send the second power information PS**2** to the first die **111**B. In some example embodiments, the second power management circuit **222** may receive first power information PS**1** from the first die **111**B.

[0077] For example, the first power information PS**1** may include information on whether the first die **111**B is operating. In some example embodiments, for example, the first power information PS**1** may include at least one of a magnitude of the first voltage V**1** supplied to the first die **111**B, an amount of power consumed by the first die **111**B, and state information of the first die **111**B.

[0078] However, the information included in the first power information PS**1** is not limited thereto, and, in some example embodiments, the first power information PS**1** may be understood to include various information on an operating state and a power state of the first die **111**B.

[0079] For example, the second power information PS**2** may include information on whether the second die **112**B is operating. In some example embodiments, for example, the second power information PS**2** may include at least one of a magnitude of the second voltage V**2** supplied to the second die **112**B, an amount of power consumed by the second die **112**B, and state information of the second die **112**B.

[0080] However, the information included in the second power information PS**2** is not limited thereto, and, in some example embodiments, the second power information PS**2** may be understood to include various information on an operating state and a power state of the second die **112**B.

[0081] For example, the first power management circuit **221** and the second power management circuit **222** may exchange the first power information PS**1** and the second power information PS**2** through a through-silicon via (TSV). The TSV may be formed to penetrate through at least a portion of each of the first die **111**B and the second die **112**B.

[0082] For example, the first power management circuit **221** may receive the second power information PS**2** from the second power management circuit **222**. In some example

embodiments, the second power management circuit **222** may receive the first power information PS**1** from the first power management circuit **221**.

[0083] Referring to FIG. **4**, a system-on-chip **100**C according to some example embodiments may include a first die **111**C and a second die **112**C. The first die **111**C and the second die **112**C may include reset circuits **211** and **212**, power management circuits **221** and **222**, and processors **231** and **232**, respectively.

[0084] The system-on-chip **100**C illustrated in FIG. **4** may be understood as an example that includes a first processor **231** and a second processor **232**, in addition to the configuration of the system-on-chip **100**B illustrated in FIG. **3**.

[0085] Therefore, the same or substantially the same components are denoted by the same or substantially the same reference numerals, and redundant descriptions are omitted to avoid repetition.

[0086] According to some example embodiments, the first die **111**C may include a first processor **231** controlling an operation of the first die **111**C. For example, the first processor **231** may be configured to control the operation of the first die **111**C.

[0087] The first processor **231** may be configured to execute software (or a program) to control at least a portion of one or more other components of the first die **111**C (for example, the first IP blocks **131** of FIG. **1**) and perform various data processing or operations. In some example embodiments, the first processor **231** may include a central processing unit (CPU), a microprocessor, or the like, and may control the overall operation of the first die **111**C. Therefore, an operation performed by the first die **111**C may be understood to be performed under the control of the first processor **231**.

[0088] The second die **112**C may include a second processor **232** controlling an operation of the second die **112**C. For example, the second processor **232** may be configured to control the operation of the second die **112**C.

[0089] The second processor **232** may be configured to execute software (or a program) to control at least portion of one or more other components of the second die **112**C (for example, the second IP blocks **132** of FIG. **1**) and perform various data processing or operations. In some example embodiments, the second processor **232** may include a central processing unit (CPU), a microprocessor, or the like, and may control the overall operation of the second die **112**C. Therefore, the operation performed by the second die **112**C may be understood to be performed under the control of the second processor **232**.

[0090] Referring to FIGS. **3** and **4**, the first processor **231** may determine whether the second die **112**C is operating, based on the second power information PS**2**.

[0091] The first processor **231** may operate based on whether the second die **112**C is operating while the first reset signal RS**1** is input.

[0092] For example, the first processor **231** may operate based on whether the second die **112**C is operating when an interaction (for example, data exchange) between the first die **111**C and the second die **112**C is required. In some example embodiments, the first processor **231** may operate based on whether the second die **112**C is operating when an interaction between the first die **111**C and the second die **112**C is desired.

[0093] For example, when receiving an execution request for an application that requires data exchange between the first die **111**C and the second die **112**C, the first processor **231** may determine whether the second die **112**C is operating, based on the second power information PS**2**.

[0094] When the second die **112**C is operating, the first processor **231** may control the operation of the first die **111**C based on a data signal received from the second die **112**C to execute an application that has received the execution request.

[0095] For example, when the second die **112**C is operating, the first processor **231** may operate at least a portion of the plurality of first IP blocks (for example, **131** of FIG. **1**) to execute an application that has received the execution request.

[0096] According to some example embodiments, when the second die **112**C is not operating, the first processor **231** may output a first operation request to operate the second die **112**C.

[0097] For example, when the second die **112**C is not operating, the first processor **231** may output the first operation request to at least one of the power supply **120** and the second reset circuit **212** to operate the second die **112**C.

[0098] The second processor **232** according to some example embodiments may determine whether the first die **111**C is operating, based on the first power information PS**1**.

[0099] In some example embodiments, the second processor **232** may operate based on whether the first die **111**C is operating while, or concurrently with, the second reset signal RS**2** is input.

[0100] For example, the second processor **232** may operate based on whether the first die **111**C is operating when an interaction (for example, data exchange) between the first die **111**C and the second die **112**C is required.

[0101] For example, when receiving an execution request for an application that requires data exchange between the first die **111**C and the second die **112**C, the second processor **232** may determine whether the first die **111**C is operating, based on the first power information PS**1**.

[0102] In some example embodiments, when the first die **111**C is operating, the second processor **232** may control the operation of the second die **112**C based on the data signal, received from the first die **111**C, to execute the application that has received the execution request.

[0103] For example, when the first die **111**C is operating, the second processor **232** may operate at least a portion of the plurality of second IP blocks (for example, **132** of FIG. **1**) to execute the application that has received the execution request.

[0104] According to some example embodiments, when the first die **111**C is not operating, the second processor **232** may output a second operation request to operate the first die **111**C.

[0105] For example, when the first die **111**C is not operating, the second processor **232** may output the second operation request to at least a portion of the power supply **120** and the first reset circuit **211** to operate the first die **111**C.

[0106] Referring to the above-described configurations, in some example embodiments, each of the first processor **231** and the second processor **232** may determine whether another die is operating, based on the power information PS**1** and PS**2** received through the power management circuit **221** and **222**. For example, the first processor **231** may determine whether the second die **112**C is operating based on the power information PS**2** received through the

power management circuit **221**. Similarly, in some example embodiments, the second processor **232** may determine whether the first die **111**C is operating based on the power information PS**1** received through the power management circuit **222**.

[0107] Furthermore, in some example embodiments, each of the first processor **231** and the second processor **232** may perform an operation, which may require an interaction between the first die **111**C and the second die **112**C, in response to another die being operating.

[0108] Thus, according to some example embodiments, the system-on-chip **100**C may reduce the time it takes to turn on the plurality of dies **111**C and **112**C when an interaction between the plurality of dies **111**C and **112**C is required.

[0109] In some example embodiments, the system-on-chip **100**C may stably control the power for the operation of each of the plurality of dies **111**C and **112**C when an interaction between the plurality of dies **111**C and **112**C is required.

[0110] FIG. **5**A is a diagram illustrating a system-on-chip, in which a plurality of dies each further include a logic circuit, according to some example embodiments. FIG. **5**B is a diagram illustrating a system-on-chip, in which logic circuits each include an AND gate, according some example embodiments. FIG. **5**C is a diagram illustrating a configuration in which a first logic circuit of FIG. **5**B outputs a first output reset signal based on a first reset signal and a first external reset signal according to some example embodiments. FIG. **5**D is a diagram illustrating a system-on-chip, in which logic circuits each includes a plurality of AND gates, according to some example embodiments.

[0111] Referring to FIGS. **5**A to **5**D, a system-on-chip **100**D according to some example embodiments may include an external reset circuit **150**, a first die **111**D, and a second die **112**D.

[0112] The system-on-chip **100**D illustrated in FIG. **5** may be understood as an example that includes an external reset circuit **150** and logic circuits **241** and **242**, in addition to the configuration of the system-on-chip **100**C illustrated in FIG. **4**.

[0113] Therefore, the same or substantially the same components are denoted by the same or substantially the same reference numerals, and redundant descriptions are omitted to avoid repetition.

[0114] According to some example embodiments, the system-on-chip **100**D may include an external reset circuit **150** outputting external reset signals ERS**1** and ERS**2** based on voltages V**1** and V**2** transmitted, transferred, or sent from the power supply **120**.

[0115] For example, the external reset circuit **150** may output a first external reset signal ERS**1** based on the first voltage V**1** transmitted, transferred, or sent from the power supply **120**. The first external reset signal ERS**1** may be understood as a signal for resetting the power of the first die **111**D to operate the first die **111**D.

[0116] In some example embodiments, the external reset circuit **150** may output a second external reset signal ERS**2** based on the second voltage V**2** transmitted, transferred, or sent from the power supply **120**. The second external reset signal ERS**2** may be understood as a signal for resetting the power of the second die **112**D to operate the second die **112**D.

[0117] The first die **111**D may include a first logic circuit **241** outputting a first output reset signal ORS**1** based on at least one of the first reset signal RS**1** and the first external reset signal ERS**1**.

[0118] In some example embodiments, the second die **112**D may include a second logic circuit **242** outputting a second output reset signal ORS**2** based on at least one of the second reset signal RS**2** and the second external reset signal ERS**2**.

[0119] For example, the first logic circuit **241** may output the first output reset signal ORS**1** through a logical operation between the first reset signal RS**1** and the first external reset signal ERS**1**. The second logic circuit **242** may output the second output reset signal ORS**2** through a logical operation between the second reset signal RS**2** and the second external reset signal ERS**2**.

[0120] Referring to FIG. **5**B, a first logic circuit **241**A according to some example embodiments may include a first AND gate A**1**. The first AND gate A**1** may perform a logical AND operation between a first reset signal RS**1** and a first external reset signal ERS**1**.

[0121] The first logic circuit **241**A may output the first output reset signal ORS**1** as a result of the logical AND operation between the first reset signal RS**1** and the first external reset signal ERS**1**.

[0122] Referring to FIGS. **5**A and **5**C, the first logic circuit **241**A may output a first output reset signal ORS**1** having a high level (e.g., a logic level "1") when both the input first reset signal RS**1** and the input first external reset signal ERS**1** are high (e.g., logic level "1").

[0123] The second logic circuit **242**A may include a second AND gate A**2**. The second AND gate A**2** may perform a logical AND operation between a second reset signal RS**2** and a second external reset signal ERS**2**.

[0124] The second logic circuit **242**A may output the second output reset signal ORS**2** as a result of the logical AND operation between the second reset signal RS**2** and the second external reset signal ERS**2**.

[0125] For example, the second logic circuit **242**A may output a second output reset signal ORS**2** having a high level when both the input second reset signal RS**2** and the input second external reset signal ERS**2** are high.

[0126] Referring to FIG. **5**D, a first logic circuit **241**B according to some example embodiments may include a plurality of AND gates A**11** and A**12**, and a second logic circuit **242**B may include a plurality of AND gates A**21** and A**22**.

[0127] For example, the first logic circuit **241**B may include a 1-1-th AND gate A**11** and a 1-2-th AND gate A**12**.

[0128] The first logic circuit **241**B may include a 1-1-th AND gate A**11** performing a logical AND operation between the first reset signal RS**1** and the second reset signal RS**2**.

[0129] In some example embodiments, the first logic circuit **241**B may include a 1-2-th AND gate A**12** performing a logical AND operation between a signal output from the 1-1-th AND gate A**11** and a first external reset signal ERS**1** output from the external reset circuit **150**.

[0130] The first logic circuit **241**B may output the first output reset signal ORS**1** as a result of the logical AND operation through the 1-1-th AND gate A**11** and the 1-2-th AND gate A**12**.

[0131] For example, the first logic circuit **241**B may output a first output reset signal ORS**1** having a high level

in response to the first reset signal RS1, the second reset signal RS2, and the first external reset signal ERS1 being all high.

[0132] In some example embodiments, the second logic circuit **242**B may include a 2-1-th AND gate A**21** and a 2-2-th AND gate A**22**.

[0133] The second logic circuit **242**B may include a 2-1-th AND gate A**21** performing a logical AND operation between the first reset signal RS**1** and the second reset signal RS**2**.

[0134] In some example embodiments, the second logic circuit **242**B may include a 2-2 AND gate A**22** performing a logical AND operation between a signal output from the 2-1-th AND gate A**21** and the second external reset signal ERS**2** output from the external reset circuit **150**.

[0135] The second logic circuit **242**B may output the second output reset signal ORS**2** as a result of the logical AND operation through the 2-1-th AND gate A**21** and the 2-2-th AND gate A**22**.

[0136] For example, the second logic circuit **242**B may output a second output reset signal ORS**2** having a high level in response to the first reset signal RS**1**, the second reset signal RS**2**, and the second external reset signal ERS**2** being all high.

[0137] For example, the first external reset signal ERS**1** and the second external reset signal ERS**2** may be referred to as the same.

[0138] According to some example embodiments, referring to FIG. **5**A, the logic circuits **241** and **242** may output the output reset signals ORS**1** and ORS**2** in response to one of the reset signals RS**1** and RS**2** or the external reset signals ERS**1** and ERS**2** based on a predetermined, or alternatively desired priority.

[0139] For example, the first logic circuit **241** may output the first output reset signal ORS**1** in response to the first reset signal RS**1**.

[0140] The first logic circuit **241** may output a first output reset signal ORS**1** having a high level when the first reset signal RS**1** is high (e.g., logic level "1") and the first external reset signal ERS**1** is low (e.g., logic level "0").

[0141] For example, the first logic circuit **241** may output the reset output signal ORS**1**, prioritizing the reset signal RS**1** over the external reset signal ERS**1**.

[0142] In some example embodiments, the second logic circuit **242** may output the second output reset signal ORS**2** in response to the second external reset signal ERS**2**.

[0143] For example, the second logic circuit **242** may output a second output reset signal ORS**2** having a high level when the second reset signal RS**2** is low and the second external reset signal ERS**2** is high.

[0144] For example, the second logic circuit **242** may output the second output reset signal ORS**2**, prioritizing the second external reset signal ERS**2** over the second reset signal RS**2**.

[0145] In some example embodiments, the first processor **231** may operate the first die **111**D in response to the first output reset signal ORS**1**.

[0146] For example, the first processor **231** may reset the power for the operation of the first die **111**D in response to the first output reset signal ORS**1**. Thus, the first processor **231** may operate the first die **111**D.

[0147] In some example embodiments, the second processor **232** may operate the second die **112**D in response to the second output reset signal ORS**2**.

[0148] For example, the second processor **232** may reset the power for the operation of the second die **112**D in response to the second output reset signal ORS**2**. Thus, the second processor **232** may operate the second die **112**D.

[0149] Referring to the above-described configurations, each of the plurality of dies **111**D and **112**D according to some example embodiments may operate based on at least a portion of signals, output from the reset circuits **211** and **212** included therein, and a signal output from the external reset circuit **150**.

[0150] Accordingly, in some example embodiments, the system-on-chip **100**D may stably control a power-on reset (POR) operation of each of the plurality of dies **111**D and **112**D.

[0151] Furthermore, in some example embodiments, the system-on-chip **100**D may stably control the power for the operation of each of the plurality of dies **111**D and **112**D through the above-described configurations.

[0152] FIG. **6** is a diagram illustrating a system-on-chip including an external reset circuit according to some example embodiments.

[0153] Referring to FIG. **6**, a system-on-chip **100**E may include a plurality of dies **111**E and **112**E and an external reset circuit **150**.

[0154] The system-on-chip **100**E illustrated in FIG. **6** may be understood as an example of the system-on-chip **100** illustrated in FIG. **1**. Therefore, the same or substantially the same components are denoted by the same or substantially the same reference numerals, and redundant descriptions are omitted to avoid repetition.

[0155] According to some example embodiments, the system-on-chip **100**E may include an external reset circuit **150** connected between the power supply **120** and the plurality of dies **111**E and **112**E.

[0156] For example, the external reset circuit **150** may output a first external reset signal ERS**1** in response to a first voltage V**1** transmitted, transferred, or sent from the power supply **120**.

[0157] According to some example embodiments, the external reset circuit **150** may output the first external reset signal ERS**1** in response to the first voltage V**1** being stabilized.

[0158] For example, the external reset circuit **150** may output the first external reset signal ERS**1** in response to a change amount of the first voltage V**1** being less than a threshold value for a unit time.

[0159] In some example embodiments, the external reset circuit **150** may output a second external reset signal ERS**2** in response to a second voltage V**2** transmitted, transferred, or sent from the power supply **120**.

[0160] According to some example embodiments, the external reset circuit **150** may output the second external reset signal ERS**2** in response to the second voltage V**2** being stabilized.

[0161] For example, the external reset circuit **150** may output the second external reset signal ERS**2** in response to a change amount of the second voltage V**2** being less than a threshold value for a unit time.

[0162] In addition, the plurality of dies **111**E and **112**E according to some example embodiments may operate in response to the external reset signals ERS**1** and ERS**2**, respectively.

[0163] According to some example embodiments, the first processor **231** may operate the first die **111**E in response to

the first external reset signal ERS1. For example, the first processor 231 may operate the first die 111E in response to a first external reset signal ERS1 having a high level.

[0164] For example, the first processor 231 may reset power for the operation of the first die 111E in response to the first external reset signal ERS1. Thus, the first processor 231 may operate the first die 111E.

[0165] For example, the first processor 231 may operate at least a portion of a plurality of first IP blocks (for example, 131 of FIG. 1), included in the first die 111E, using the first voltage V1 in response to the first external reset signal ERS1.

[0166] According to some example embodiments, the second processor 232 may operate the second die 112E in response to the second external reset signal ERS2. For example, the second processor 232 may operate the second die 112E in response to a second external reset signal ERS2 having a high level.

[0167] For example, the second processor 232 may reset power for the operation of the second die 112E in response to the second external reset signal ERS2. Thus, the second processor 232 may operate the second die 112E.

[0168] For example, the second processor 232 may operate at least one of a plurality of second IP blocks (for example, 132 of FIG. 1), included in the second die 112E, using the second voltage V2 in response to the second external reset signal ERS2.

[0169] Referring to the above-described configurations, the external reset circuit 150 according to some example embodiments may output different external reset signals ERS1 and ERS2 for the plurality of dies 111E and 112E using different voltages (or power) V1 and V2.

[0170] As a result, the system-on-chip 100E according to some example embodiments may independently and stably control a power-on reset operation for each of the plurality of dies 111E and 112E.

[0171] Furthermore, in some example embodiments, the system-on-chip 100E may stably control power for the operation of each of the plurality of dies 111E and 112E through the above-described configurations.

[0172] FIG. 7 is a diagram illustrating a system-on-chip, including an external reset circuit according to some example embodiments, in which a plurality of dies each include a power management circuit.

[0173] Referring to FIG. 7, a system-on-chip 100F according to some example embodiments may include a first die 111F and a second die 112F. The first die 111F and the second die 112F may include processors 231 and 232 and power management circuits 221 and 222, respectively.

[0174] The system-on-chip 100F illustrated in FIG. 7 may be understood as an example that further includes power management circuits 221 and 222, in addition to the configuration of the system-on-chip 100E illustrated in FIG. 6. Therefore, the same or substantially the same components are denoted by the same or substantially the same reference numerals, and redundant descriptions are omitted to avoid repetition.

[0175] According to some example embodiments, the first die 111F may further include a first power management circuit 221.

[0176] For example, the first power management circuit 221 may transmit, transfer, or send first power information PS1 to the second die 112F. In some example embodiments, the first power management circuit 221 may receive second power information PS2 from the second die 112F.

[0177] In some example embodiments, the second die 112F may further include a second power management circuit 222.

[0178] For example, the second power management circuit 222 may transmit, transfer, or send second power information PS2 to the first die 111F. In some example embodiments, the second power management circuit 222 may receive first power information PS1 from the first die 111F.

[0179] For example, the first power information PS1 may include information on whether the first die 111F is operating. For example, the second power information PS2 may include information on whether the second die 112F is operating.

[0180] For example, the first power management circuit 221 and the second power management circuit 222 may exchange first power information PS1 and second power information PS2 through a through-silicon via (TSV).

[0181] According to some example embodiments, the first processor 231 may determine whether the second die 112F is operating, based on the second power information PS2.

[0182] Furthermore, the first processor 231 may operate based on whether the second die 112F is operating while the first external reset signal ERS1 is input.

[0183] For example, the first processor 231 may operate based on whether the second die 112F is operating when an interaction (for example, data exchange) between the first die 111F and the second die 112F is required.

[0184] For example, when receiving an execution request for an application that requires data exchange between the first die 111F and the second die 112F, the first processor 231 may determine whether the second die 112F is operating, based on the second power information PS2.

[0185] Furthermore, when the second die 112F is operating, the first processor 231 may control the operation of the first die 111F based on a data signal, received from the second die 112F, to execute an application that have received an execution request.

[0186] The first processor 231 may operate the first die 111F using the first voltage V1 transmitted, transferred, or sent from the power supply 120.

[0187] In some example embodiments, the second processor 232 may determine whether the first die 111F is operating based on the first power information PS1.

[0188] The second processor 232 may operate based on whether the first die 111F is operating while the second reset signal RS2 is output.

[0189] For example, the second processor 232 may operate based on whether the first die 111F is operating when an interaction (for example, data exchange) between the first die 111F and the second die 112F is required.

[0190] For example, when receiving an execution request for an application that requires data exchange between the first die 111F and the second die 112F, the second processor 232 may determine whether the first die 111F is operating based on the first power information PS1.

[0191] When the first die 111F is operating, the second processor 232 may control the operation of the second die 112F based on a data signal, received from the first die 111F, to execute an application that has received an execution request.

[0192] The second processor **232** may operate the second die **112**F using the second voltage V**2** transmitted, transferred, or sent from the power supply **120**.

[0193] Referring to the above-described configurations according to some example embodiments, the first processor **231** and the second processor **232** may determine whether another die is operating, based on the power information PS**1** and PS**2** received through the power management circuits **221** and **222**, respectively.

[0194] Furthermore, in some example embodiments, each of the first processor **231** and the second processor **232** may perform an operation of requesting the first die **111**F and the second die **112**F to operate together in response to the other die being operating.

[0195] Accordingly, in some example embodiments, the system-on-chip **100**F may reduce the time it takes to operate the plurality of dies **111**F and **112**F when an interaction between the plurality of dies **111**F and **112**F is required.

[0196] FIG. **8** is a diagram illustrating a system-on-chip, in which a reset circuit included in each die outputs different reset signals based on a supply voltage, according to some example embodiments.

[0197] Referring to FIG. **8**, a system-on-chip **100**G may include a plurality of dies **111**G and **112**G, respectively including reset circuits **211**G and **212**G.

[0198] The system-on-chip **100**G and the reset circuits **211**G and **212**G illustrated in FIG. **8** may be understood as examples of the system-on-chip **100**A and the reset circuits **211** and **212** illustrated in FIG. **2**. Therefore, the same or substantially the same components are denoted by the same or substantially the same reference numerals, and redundant descriptions are omitted to avoid repetition.

[0199] According to some example embodiments, the first die **111**G may include a first reset circuit **211**G. For example, the first die **111**G may include a first reset circuit **211**G outputting a first reset signal RS**1** in response to a supply voltage VS transmitted, transferred, or sent from a power supply **120**.

[0200] According to some example embodiments, the first reset circuit **211**G may output the first reset signal RS**1** in response to the supply voltage VS being stabilized.

[0201] For example, the first reset circuit **211**G may output the first reset signal RS**1** in response to a change amount of the supply voltage VS being less than a threshold value for a unit time.

[0202] The second die **112**G may include a second reset circuit **212**G. For example, the second die **112**G may include a second reset circuit **212**G outputting a second reset signal RS**2** in response to the supply voltage VS transmitted, transferred, or sent from the power supply **120**.

[0203] The second reset circuit **212**G according to some example embodiments may output the second reset signal RS**2** in response to the supply voltage VS being stabilized.

[0204] For example, the second reset circuit **212**G may output the second reset signal RS**2** in response to a change amount of the supply voltage VS being less than a threshold value for a unit time.

[0205] In some example embodiments, the plurality of dies **111**G and **112**G may operate in response to the reset signals RS**1** and RS**2**, respectively.

[0206] For example, the first die **111**G may operate using the supply voltage VS in response to the first reset signal RS**1**.

[0207] For example, the first die **111**G may operate at least a portion of a plurality of first IP blocks **131** using the supply voltage VS in response to the first reset circuit **211**G outputting a first reset signal RS**1** having a high level.

[0208] The second die **112**G may operate using the supply voltage VS in response to the second reset signal RS**2**.

[0209] For example, the second die **112**G may operate at least a portion of a plurality of second IP blocks **132** using the supply voltage VS in response to the second reset circuit **212**G outputting a second reset signal RS**2** having a high level.

[0210] Referring to the above-described configurations, the system-on-chip **100**G according to some example embodiments may include reset circuits **211**G and **212**G, respectively provided in the plurality of dies **111**G and **112**G.

[0211] The reset circuits **211**G and **212**G may output the different reset signals RS**1** and RS**2** from the supply voltage VS transmitted, transferred, or sent from the power supply **120**.

[0212] The plurality of dies **111**G and **112**G may operate in response to the different reset signals RS**1** and RS**2**, respectively.

[0213] As a result, the system-on-chip **100**G according to some example embodiments may independently and stably control a power-on reset operation for each of the plurality of dies **111**G and **112**G.

[0214] Furthermore, in some example embodiments, the system-on-chip **100**G may stably control power for the operation of each of the plurality of dies **111**G and **112**G through the above-described configurations.

[0215] FIG. **9** is a diagram illustrating a system-on-chip, in which a plurality of dies each further includes a power management circuit, according to some example embodiments. FIG. **10** is a diagram illustrating a system-on-chip, in which each of the plurality of dies includes a processor, according to some example embodiments.

[0216] Referring to FIG. **9**, a system-on-chip **100**H according to some example embodiments may include a first die **111**H and a second die **112**H. The first die **111**H and the second die **112**H may include reset circuits **211**G and **212**G and power management circuits **221** and **222**, respectively.

[0217] The system-on-chip **100**H illustrated in FIG. **9** may be understood as a configuration in which the first and second dies **111**H and **112**H further include power management circuits **221** and **222**, respectively, in addition to the configuration of the system-on-chip **100**G illustrated in FIG. **8**. Therefore, the same or substantially the same components are denoted by the same or substantially the same reference numerals, and redundant descriptions are omitted to avoid repetition.

[0218] According to some example embodiments, the first die **111**H may further include a first power management circuit **221**.

[0219] For example, the first power management circuit **221** may transmit, transfer, or send first power information PS**1** to the second die **112**H. In some example embodiments, the first power management circuit **221** may receive second power information PS**2** from the second die **112**H.

[0220] According to some example embodiments, the second die **112**H may further include a second power management circuit **222**.

[0221] For example, the second power management circuit **222** may transmit, transfer, or send second power information PS**2** to the first die **111**H. In some example

embodiments, the second power management circuit **222** may receive first power information PS**1** from the first die **111**H.

[0222] For example, the first power information PS**1** may include information on whether the first die **111**H is operating. In some example embodiments, for example, the first power information PS**1** may include at least a portion of a magnitude of the supply voltage VS supplied to the first die **111**H, an amount of power consumed by the first die **111**H, and state information of the first die **111**H.

[0223] However, the information included in the first power information PS**1** is not limited thereto, and, in some example embodiments the first power information PS**1** may be understood as including various information on an operating state and a power state of the first die **111**H.

[0224] For example, the second power information PS**2** may include information on whether the second die **112**H is operating. In some example embodiments, for example, the second power information PS**2** may include at least a portion of a magnitude of the supply voltage VS supplied to the second die **112**H, an amount of power consumed by the second die **112**H, and state information of the second die **112**H.

[0225] However, the information included in the second power information PS**2** is not limited thereto, and, and in some example embodiments, the second power information PS**2** may be understood as including various types of information on an operating state and a power state of the second die **112**H.

[0226] Referring to FIG. **10**, a system-on-chip **100**I according to some example embodiments may include a first die **1111** and a second die **1121**. The first die **1111** and the second die **1121** may include reset circuits **211**G and **212**G, power management circuits **221** and **222**, and processors **231** and **232**, respectively.

[0227] The system-on-chip **100**I illustrated in FIG. **10** may be understood as an example that further includes a first processor **231** and a second processor **232**, in addition to the configuration of the system-on-chip **100**H illustrated in FIG. **9**.

[0228] Therefore, the same or substantially the same components are denoted by the same or substantially the same reference numerals, and redundant descriptions are omitted to avoid repetition.

[0229] According to some example embodiments, the first die **111**I may include a first processor **231** controlling an operation of the first die **111**I.

[0230] The first processor **231** may be configured to execute software (or a program) to control at least a portion of one or more other components of the first die **111**I (for example, the first IP blocks **131** of FIG. **8**) and perform various data processing or operations. In some example embodiments, the first processor **231** may include a central processing unit (CPU), a microprocessor, or the like, and may control the overall operation of the first die **111**I. Therefore, an operation performed by the first die **111**I may be understood to be performed under the control of the first processor **231**.

[0231] The second die **112**I may include a second processor **232** controlling an operation of the second die **112**I.

[0232] The second processor **232** may be configured to execute software (or a program) to control at least a portion of one or more other components of the second die **112**I (for example, the first IP blocks **132** of FIG. **8**) and perform various data processing or operations. In some example embodiments, the second processor **232** may include a central processing unit (CPU), a microprocessor, or the like, and may control the overall operation of the second die **112**I. Therefore, an operation performed by the second die **112**I may be understood to be performed under the control of the second processor **232**.

[0233] Referring to FIGS. **9** and **10**, the first processor **231** may determine whether the second die **112**I is operating, based on the second power information PS**2**.

[0234] The first processor **231** may operate based on whether the second die **1121** is operating while the first reset signal RS**1** is input.

[0235] For example, the first processor **231** may operate based on whether the second die **112**I is operating when an interaction (for example, data exchange) between the first die **111**I and the second die **1121** is required.

[0236] For example, when receiving an execution request for an application that requires data exchange between the first die **1111** and the second die **112**I, the first processor **231** may determine whether the second die **112**I is operating, based on the second power information PS**2**.

[0237] When the second die **112**I is operating, the first processor **231** may control the operation of the first die **1111** based on a data signal, received from the second die **112**I, to execute an application that has received an execution request.

[0238] For example, when the second die **1121** is operating, the first processor **231** may operate at least a portion of a plurality of first IP blocks (for example, **131** of FIG. **8**) using the supply voltage VS to execute an application that has received an execution request.

[0239] In some example embodiments, the second processor **232** may determine whether the first die **111**I is operating, based on the first power information PS**1**.

[0240] According to some example embodiments, the second processor **232** may operate based on whether the first die **1111** is operating while the second reset signal RS**2** is input.

[0241] For example, the second processor **232** may operate based on whether the first die **111**I is operating when an interaction (for example, data exchange) between the first die **111**I and the second die **112**I is required.

[0242] For example, when receiving an execution request for an application that requires data exchange between the first die **1111** and the second die **112**I, the second processor **232** may determine whether the first die **1111** is operating, based on the first power information PS**1**.

[0243] According to some example embodiments, when the first die **1111** is operating, the second processor **232** may control the operation of the second die **112**I based on a data signal, received from the first die **111**I, to execute an application that has received an execution request.

[0244] For example, when the first die **1111** is operating, the second processor **232** may operate at least a portion of a plurality of second IP blocks (for example, **132** of FIG. **8**) using the supply voltage VS to execute an application that has received an execution request.

[0245] Referring to the above-described configurations, in some example embodiments, the first processor **231** and the second processor **232** may determine whether the other die is operating, based on the power information PS**1** and PS**2** received through the power management circuit **221** and **222**, respectively.

[0246] According to some example embodiments, each of the first processor **231** and the second processor **232** may perform an operation of requesting the first die **1111** and the second die **112**I to operate together in response to the other die being operating.

[0247] As a result, in some example embodiments, the system-on-chip **100**I may reduce the time it takes to reset power of the plurality of dies **1111** and **1121** when an interaction between the plurality of dies **1111**, **112**I is required.

[0248] FIG. **11** is a diagram illustrating a system-on-chip, in which each of the plurality of dies further includes a logic circuit, according to some example embodiments.

[0249] Referring to FIG. **11**, a system-on-chip **100**J according to some example embodiments may include an external reset circuit **150**, a first die **111**J, and a second die **112**J.

[0250] The system-on-chip **100**J illustrated in FIG. **11** may be understood as an example that further includes logic circuits **241**J and **242**J, in addition to the configuration of the system-on-chip **100**I illustrated in FIG. **10**. Therefore, the same or substantially the same components are denoted by the same or substantially the same reference numerals, and redundant descriptions are omitted to avoid repetition.

[0251] The system-on-chip **100**J may include an external reset circuit **150** outputting external reset signals ERS**1** and ERS**2** based on a supply voltage VS transmitted from a power supply **120**.

[0252] For example, the external reset circuit **150** may output a first external reset signal ERS**1** based on the supply voltage VS transmitted, transferred, or sent from the power supply **120**. The first external reset signal ERS**1** may be understood as a signal for resetting power of the first die **111**J to operate the first die **111**J.

[0253] In some example embodiments, the external reset circuit **150** may output a second external reset signal ERS**2** based on the supply voltage VS transmitted, transferred, or sent from the power supply **120**. The second external reset signal ERS**2** may be understood as a signal for resetting power of the second die **112**J to operate the second die **112**J.

[0254] The system-on-chip **100**J may include a first logic circuit **241**J outputting a first output reset signal ORS**1** based on at least a portion of a first reset signal RS**1** and the first external reset signal ERS**1**.

[0255] In some example embodiments, the system-on-chip **100**J may include a second logic circuit **242**J outputting a second output reset signal ORS**2** based on at least a portion of a second reset signal RS**2** and the second external reset signal ERS**2**.

[0256] According to some example embodiments, each of the first and second logic circuits **241**J and **242**J may include an AND gate.

[0257] Thus, the first logic circuit **241**A may output the first output reset signal ORS**1** as a result of an AND operation between the first reset signal RS**1** and the first external reset signal ERS**1**.

[0258] According to some example embodiments, the second logic circuit **242**A may output the second output reset signal ORS**2** as a result of the AND operation between the second reset signal RS**2** and the second external reset signal ERS**2**.

[0259] In some example embodiments, each of the first and second logic circuits **241**J and **242**J may include a plurality of AND gates.

[0260] For example, the first logic circuit **241**J may include an AND gate performing an AND operation between the first reset signal RS**1** and the second reset signal RS**2**.

[0261] In some example embodiments, the first logic circuit **241**J may include an AND gate performing an AND operation between the result of the AND operation between the first reset signal RS**1** and the second reset signal RS**2** and the first external reset signal ERS**1**.

[0262] The above-described configurations may allow the first logic circuit **241**J to output the first output reset signal ORS**1** as a result of an AND operation between the first reset signal RS**1**, the second reset signal RS**2**, and the first external reset signal ERS**1**.

[0263] In some example embodiments, the second logic circuit **242**J may include an AND gate performing an AND operation between the first reset signal RS**1** and the second reset signal RS**2**.

[0264] In some example embodiments, the second logic circuit **242**J may include an AND gate performing an AND operation between the result of the AND operation between the first reset signal RS**1** and the second reset signal RS**2** and the second external reset signal ERS**2**.

[0265] The above-described configurations may allow the second logic circuit **242**J to output the second output reset signal ORS**2** as a result of an AND operation between the first reset signal RS**1**, the second reset signal RS**2**, and the second external reset signal ERS**2**.

[0266] In some example embodiments, the logic circuits **241**J and **242**J may output the output reset signals ORS**1** and ORS**2** in response to one of the reset signals RS**1** and RS**2** or external reset signals ERS**1** and ERS**2** based on a predetermined, or alternatively desired priority, respectively.

[0267] For example, the first logic circuit **241**J may output a first output reset signal ORS**1** having a high level when the first reset signal RS**1** is high and the first external reset signal ERS**1** is low.

[0268] For example, the first logic circuit **241**J may output the first output reset signal ORS**1**, prioritizing the first reset signal RS**1** over the first external reset signal ERS**1**.

[0269] For example, the second logic circuit **242**J may output a second output reset signal ORS**2** having a high level when the second reset signal RS**2** is low and the second external reset signal ERS**2** is high.

[0270] For example, the second logic circuit **242**J may output the second output reset signal ORS**2**, prioritizing the second external reset signal ERS**2** over the second reset signal RS**2**.

[0271] Furthermore, in some example embodiments, the first processor **231** may operate the first die **111**J in response to the first output reset signal ORS**1**.

[0272] For example, the first processor **231** may reset power for an operation of the first die **111**J in response to the first output reset signal ORS**1**. Thus, the first processor **231** may operate the first die **111**J.

[0273] In some example embodiments, the second processor **232** may operate the second die **112**J in response to the second output reset signal ORS**2**.

[0274] For example, the second processor **232** may reset power for an operation of the second die **112**J in response to the second output reset signal ORS**2**. Thus, the second processor **232** may operate the second die **112**J.

[0275] Referring to the above-described configurations, each of the plurality of dies **111**J and **112**J according to some example embodiments may operate based on at least a

portion of signals, output from the reset circuits **211**G and **212**G included therein, and signals output from the external reset circuit **150**.

[0276] As a result, the system-on-chip **100**J may stably control a power-on reset operation of each of the plurality of dies **111**J and **112**J.

[0277] According to some example embodiments, the system-on-chip **100**J may stably control the power for the operation of each of the plurality of dies **111**J and **112**J through the above-described configurations.

[0278] FIG. **12** is a diagram illustrating a system-on-chip including an external reset circuit outputting an external reset signal based on a supply voltage according to some example embodiments.

[0279] Referring to FIG. **12**, a system-on-chip **100**K according to some example embodiments may include a plurality of dies **111**K and **112**K and an external reset circuit **150**.

[0280] The system-on-chip **100**K illustrated in FIG. **12** may be understood as an example of the system-on-chip **100** illustrated in FIG. **1**. Therefore, the same or substantially the same components are denoted by the same or substantially the same reference numerals, and redundant descriptions are omitted to avoid repetition.

[0281] According to some example embodiments, the system-on-chip **100**K may include an external reset circuit **150** connected between a power supply **120** and the plurality of dies **111**K and **112**K.

[0282] For example, the external reset circuit **150** may output a first external reset signal ERS**1** and a second external reset signal ERS**2** in response to a supply voltage VS transmitted, transferred, or sent from the power supply **120**.

[0283] According to some example embodiments, the external reset circuit **150** may output a first external reset signal ERS**1** and a second external reset signal ERS**2** in response to the supply voltage VS being stabilized.

[0284] For example, the external reset circuit **150** may output the first external reset signal ERS**1** and the second external reset signal ERS**2** in response to a change amount of the supply voltage VS being less than a threshold value for a unit time.

[0285] In some example embodiments, the plurality of dies **111**K and **112**K may operate in response to the external reset signals ERS**1** and ERS**2**, respectively.

[0286] According to some example embodiments, the first processor **231**K may operate the first die **111**K in response to the first external reset signal ERS**1**. For example, the first processor **231**K may operate the first die **111**K in response to a first external reset signal ERS**1** having a high level.

[0287] For example, the first processor **231**K may reset power for an operation of the first die **111**K in response to the first external reset signal ERS**1**. Thus, the first processor **231**K may operate the first die **111**K.

[0288] For example, the first processor **231**K may operate at least a portion of a plurality of first IP blocks (for example, **131** of FIG. **1**), included in the first die **111**K, using the supply voltage VS in response to the first external reset signal ERS**1**.

[0289] According to some example embodiments, the second processor **232**K may operate the second die **112**K in response to the second external reset signal ERS**2**. For example, the second processor **232**K may operate the second die **112**K in response to a second external reset signal ERS**2** having a high level.

[0290] For example, the second processor **232**K may reset power for an operation of the second die **112**K in response to the second external reset signal ERS**2**. Thus, the second processor **232**K may operate the second die **112**K.

[0291] For example, the second processor **232**K may operate at least a portion of a plurality of second IP blocks (for example, **132** of FIG. **1**), included in the second die **112**K, using the supply voltage VS in response to the second external reset signal ERS**2**.

[0292] Referring to the above-described configurations, the external reset circuit **150** according to some example embodiments may output different external reset signals ERS**1** and ERS**2** for the plurality of dies **111**K and **112**K using the supply voltage VS.

[0293] As a result, the system-on-chip **100**K according to some example embodiments may independently and stably control a power-on reset operation for each of the plurality of dies **111**K and **112**K.

[0294] Furthermore, in some example embodiments the system-on-chip **100**K may stably control the power for the operation of each of the plurality of dies **111**K and **112**K through the above-described configurations.

[0295] FIG. **13** is a diagram illustrating a system-on-chip, including an external reset circuit according to some example embodiments, in which each die includes a power management circuit.

[0296] Referring to FIG. **13**, a system-on-chip **100**L according to some example embodiments may include a first die **111**L and a second die **112**L. The first die **111**L and the second die **112**L may include processors **231**K and **232**K and power management circuits **221**L and **222**L, respectively. For example, the first die **111**L may include a first processor **231**K and a first power management circuit **221**L, and the second die **112**L may include a second processor **232**K and a second power management circuit **222**L.

[0297] The system-on-chip **100**L illustrated in FIG. **13** may be understood as an example that further includes power management circuits **221**L and **222**L, in addition to the configuration of the system-on-chip **100**K illustrated in FIG. **12**. Therefore, the same or substantially the same components are denoted by the same or substantially the same reference numerals, and redundant descriptions are omitted to avoid repetition.

[0298] According to some example embodiments, the first die **111**L may further include the first power management circuit **221**L.

[0299] For example, the first power management circuit **221**L may transmit, transfer, or sned first power information PS**1** to the second die **112**L. In some example embodiments, the first power management circuit **221**L may obtain second power information PS**2** from the second die **112**L.

[0300] In some example embodiments, the second die **112**L may further include the second power management circuit **222**L.

[0301] For example, the second power management circuit **222**L may transmit, transfer, or send second power information PS**2** to the first die **111**L. In some example embodiments, the second power management circuit **222**L may acquire, obtain, or receive first power information PS**1** from the first die **111**L.

[0302] According to some example embodiments, the first processor **231**K may determine whether the second die **112**L is operating based on second power information PS**2**.

[0303] Furthermore, in some example embodiments, the first processor **231**K may operate based on whether the second die **112**L is operating while the first external reset signal ERS**1** is input.

[0304] For example, the first processor **231**K may operate based on whether the second die **112**L is operating when an interaction (for example, data exchange) between the first die **111**L and the second die **112**L is required.

[0305] For example, when receiving an execution request for an application that requires data exchange between the first die **111**L and the second die **112**L, the first processor **231**K may determine whether the second die **112**L is operating, based on the second power information PS**2**.

[0306] Furthermore, in some example embodiments, when the second die **112**L is operating, the first processor **231**K may control an operation of the first die **111**L based on the data signal received from the second die **112**L to execute an application that has received an execution request.

[0307] According to some example embodiments, the first processor **231**K may operate the first die **111**L using the supply voltage VS transmitted, transferred, or sent from a power supply **120**.

[0308] In some example embodiments, the second processor **232**K may determine whether the first die **111**L is operating based on the first power information PS**1**.

[0309] Furthermore, in some example embodiments, the second processor **232**K may operate based on whether the first die **111**L is operating while the second reset signal RS**2** is output.

[0310] For example, the second processor **232**K may operate based on whether the first die **111**L is operating when an interaction (for example, data exchange) between the first die **111**L and the second die **112**L is required.

[0311] For example, when receiving an execution request for an application that requires data exchange between the first die **111**L and the second die **112**L, the second processor **232**K may determine whether the first die **111**L is operating, based on the first power information PS**1**.

[0312] Furthermore, in some example embodiments, when the first die **111**L is operating, the second processor **232**K may control an operation of the second die **112**L based on a data signal, received from the first die **111**L, to execute an application that has received an execution request.

[0313] According to some example embodiments, the second processor **232**K may operate the second die **112**L using the supply voltage VS transmitted, transferred, or sent from the power supply **120**.

[0314] Referring to the above-described configurations according to some example embodiments, the first processor **231**K and the second processor **232**K may determine whether another die is operating, based on the power information PS**1** and PS**2** received through the power management circuit **221**L and **222**L

[0315] Furthermore, in some example embodiments, each of the first processor **231**K and the second processor **232**K may perform an operation of requesting the first die **111**L and the second die **112**L to operate together in response to the other die being operating.

[0316] As a result, the system-on-chip **100**L may reduce the time it takes to reset power of the plurality of dies **111**L and **112**L and operate the plurality of dies **111**L and **112**L when an interaction between the plurality of dies **111**L and **112**L is required.

[0317] FIG. **14**A is a diagram illustrating a configuration in which a first die and a second die according to some example embodiments operate in response to a first reset signal generated from the first die. FIG. **14**B is a diagram illustrating a configuration in which a first die and a second die according to some example embodiments operate in response to a second reset signal generated from the second die.

[0318] Referring to FIG. **14**A, a system-on-chip **100**M according to some example embodiments may include a first die **111**M and a second die **112**M. The first die **111**M may include a first reset circuit **211**M.

[0319] The system-on-chip **100**M illustrated in FIG. **14**A may be understood as an example of the system-on-chip **100** illustrated in FIG. **1**.

[0320] According to some example embodiments, the first die **111**M may include a first reset circuit **211**M outputting a first reset signal RS**1** based on a supply voltage VS.

[0321] For example, the first reset circuit **211**M may output the first reset signal RS**1** based on the supply voltage VS transmitted, transferred, or sent from a power supply **120**.

[0322] The first reset signal RS**1** may be understood as a signal for resetting power supplied to the first die **111**M to turn on the first die **111**M.

[0323] According to some example embodiments, the first die **111**M may operate in response to the first reset signal RS**1**.

[0324] For example, the first die **111**M may operate using the supply voltage VS in response to the first reset signal RS**1**.

[0325] For example, the first die **111**M may operate at least a portion of a plurality of first IP blocks **131** using the supply voltage VS in response to the first reset signal RS**1**.

[0326] In some example embodiments, the first die **111**M may transmit, transfer, or send the first reset signal RS**1** to the second die **112**M. For example, the first die **111**M may transmit, transfer, or send the first reset signal RS**1**, output from the first reset circuit **211**M, to the second die **112**M.

[0327] For example, the first die **111**M may transmit, transfer, or send the first reset signal RS**1** to the second die **112**M through a through-silicon via (TSV) formed to penetrate through at least a portion of the first die **111**M and the second die **112**M.

[0328] According to some example embodiments, the second die **112**M may operate in response to the first reset signal RS**1**.

[0329] For example, the second die **112**M may operate using the supply voltage VS in response to the first reset signal RS**1** received from the first die **111**M.

[0330] For example, the second die **112**M may operate at least a portion of a plurality of second IP blocks **132** using the supply voltage VS in response to the first reset signal RS**1**.

[0331] Referring to FIG. **14**B, a system-on-chip **100**N according to some example embodiments may include a first die **111**N and a second die **112**N. The second die **112**N may include a second reset circuit **212**N.

[0332] The system-on-chip **100**N illustrated in FIG. **14**B may be understood as an example of the system-on-chip **100** illustrated in FIG. **1**.

[0333] According to some example embodiments, the second die **112**N may include a second reset circuit **212**N outputting a second reset signal RS**2** based on a supply voltage VS.

[0334] For example, the second reset circuit **212**N may output the second reset signal RS**2** based on the supply voltage VS transmitted, transferred, or sent from a power supply **120**.

[0335] The second reset signal RS**2** may be understood as a signal for resetting power supplied to the second die **112**N to turn on the second die **112**N.

[0336] According to some example embodiments, the second die **112**N may operate in response to the second reset signal RS**2**.

[0337] For example, the second die **112**N may operate using the supply voltage VS in response to the second reset signal RS**2**.

[0338] For example, the second die **112**N may operate at least a portion of a plurality of second IP blocks **132** using the supply voltage VS in response to the second reset signal RS**2**.

[0339] In some example embodiments, the second die **112**N may transmit, transfer, or send the second reset signal RS**2** to the first die **111**N. For example, the second die **112**N may transmit, transfer, or send the second reset signal RS**2**, output from the second reset circuit **212**N, to the first die **111**N.

[0340] For example, the second die **112**N may transmit, transfer, or send the second reset signal RS**2** to the first die **111**N through a through-silicon via (TSV) formed to penetrate through at least a portion of the first die **111**N and the second die **112**N.

[0341] According to some example embodiments, the first die **111**N may operate in response to the second reset signal RS**2**.

[0342] For example, the first die **111**N may operate using the supply voltage VS in response to the second reset signal RS**2** received from the second die **112**N.

[0343] For example, the first die **111**N may operate at least a portion of a plurality of first IP blocks **131** using the supply voltage VS in response to the second reset signal RS**2**.

[0344] Referring to the above-described configurations, each of the system-on-chips **100**M and **100**N according to some example embodiments may reset power for an operation of the plurality of dies using a reset signal output from a single reset circuit.

[0345] As a result, the system-on-chips **100**M and **100**N may operate the plurality of dies.

[0346] The above-described configurations according to some example embodiments may allow the system-on-chips **100**M and **100**N to significantly reduce an area and costs required to implement a circuit resetting the power of the plurality of dies to operate the plurality of dies.

[0347] FIG. **15**A is a diagram illustrating a configuration in which a first die and a second die according to some example embodiments operate in response to a first output reset signal output from a first logic circuit. FIG. **15**B is a diagram illustrating a configuration in which a first die and a second die according to some example embodiments operate in response to a second output reset signal output from a second logic circuit.

[0348] Referring to FIG. **15**A, a system-on-chip **1000** according to some example embodiments may include a first die **1110**, a second die **1120**, and an external reset circuit **150**. The first die **1110** may include a first reset circuit **211**M and a first logic circuit **2410**.

[0349] The system-on-chip **1000** illustrated in FIG. **15**A may be understood as an example that further includes a first logic circuit **2410** and an external reset circuit **150**, in addition to the configuration of the system-on-chip **100**M illustrated in FIG. **14**A.

[0350] Therefore, the same or substantially the same components are denoted by the same or substantially the same reference numerals, and redundant descriptions are omitted to avoid repetition.

[0351] According to some example embodiments, the external reset circuit **150** may include an external reset signal ERS output based on a supply voltage VS transmitted, transferred, or sent from a power supply **120**. For example, the external reset circuit **150** may output the external reset signal ERS based on the supply voltage VS transmitted, transferred, or sent from the power supply **120**.

[0352] The first die **1110** may include a first logic circuit **2410** outputting a first output reset signal ORS**1** based on at least one of a first reset signal RS**1** and the external reset signal ERS.

[0353] For example, the first logic circuit **2410** may output the first output reset signal ORS**1** through a logical operation between the first reset signal RS**1** and the external reset signal ERS.

[0354] According to some example embodiments, the first logic circuit **2410** may include an AND gate. Accordingly, the first logic circuit **2410** may output the first output reset signal ORS**1** as a result of a logical AND operation between the first reset signal RS**1** and the external reset signal ERS.

[0355] Furthermore, in some example embodiments, the first die **1110** may operate in response to the first reset signal RS**1**.

[0356] For example, the first die **1110** may operate using the supply voltage VS in response to the first output reset signal ORS**1**.

[0357] For example, the first die **1110** may operate at least a portion of a plurality of first IP blocks **131** using the supply voltage VS in response to the first output reset signal ORS**1**.

[0358] In some example embodiments, the first die **1110** may transmit, transfer, or send the first output reset signal ORS**1** to the second die **1120**. For example, the first die **1110** may transmit, transfer, or send the first output reset signal ORS**1**, output from the first logic circuit **2410**, to the second die **1120**.

[0359] For example, the first die **1110** may transmit, transfer, or send the first output reset signal ORS**1** to the second die **1120** through a through-silicon via (TSV) formed to penetrate through at least a portion of the first die **1110** and the second die **1120**.

[0360] According to some example embodiments, the second die **1120** may operate in response to the first output reset signal ORS**1**.

[0361] For example, the second die **1120** may operate using the supply voltage VS in response to the first output reset signal ORS**1** received from the first die **1110**.

[0362] For example, the second die **1120** may operate at least a portion of a plurality of second IP blocks **132** using the supply voltage VS in response to the first output reset signal ORS**1**.

[0363] Referring to FIG. **15**B, a system-on-chip **100**P according to some example embodiments may include a first

die **111**P, a second die **112**P, and an external reset circuit **150**. The second die **112**P may include a second reset circuit **212**M and a second logic circuit **242**P.

[0364] The system-on-chip **100**P illustrated in FIG. **15**B may be understood as an example that further includes a second logic circuit **242**P and an external reset circuit **150**, in addition to the configuration of the system-on-chip **100**N illustrated in FIG. **14**B.

[0365] Therefore, the same or substantially the same components are denoted by the same or substantially the same reference numerals, and redundant descriptions are omitted to avoid repetition.

[0366] The second die **112**P may include a second logic circuit **242**P outputting a second output reset signal ORS**2** based on at least a portion of a second reset signal RS**2** and an external reset signal ERS.

[0367] For example, the second logic circuit **242**P may output the second output reset signal ORS**2** through a logical operation between the second reset signal RS**2** and the external reset signal ERS.

[0368] According to some example embodiments, the second logic circuit **242**P may include an AND gate. Therefore, the second logic circuit **242**P may output the second output reset signal ORS**2** as a result of a logical AND operation between the second reset signal RS**2** and the external reset signal ERS.

[0369] The second die **112**P may operate in response to the second reset signal RS**2**.

[0370] For example, the second die **112**P may operate using a supply voltage VS in response to the second output reset signal ORS**2**.

[0371] For example, the second die **112**P may operate at least a portion of a plurality of second IP blocks **132** using the supply voltage VS in response to the second output reset signal ORS**2**.

[0372] In some example embodiments, the second die **112**P may transmit, transfer, or send the second output reset signal ORS**2** to the first die **111**P. For example, the second die **112**P may transmit, transfer, or send the second output reset signal ORS**2**, output from the second logic circuit **242**P, to the first die **111**P.

[0373] For example, the second die **112**P may transmit, transfer, or send the second output reset signal ORS**2** to the first die **111**P through a through-silicon via (TSV) formed to penetrate through at least a portion of the first die **111**P and the second die **112**P.

[0374] According to some example embodiments, the first die **111**P may operate in response to the second output reset signal ORS**2**.

[0375] For example, the first die **111**P may operate using the supply voltage VS in response to the second output reset signal ORS**2** received from the second die **112**P.

[0376] For example, the first die **111**P may operate at least a portion of a plurality of first IP blocks **131** using the supply voltage VS in response to the second output reset signal ORS**2**.

[0377] Referring to the above-described configurations, the system-on-chips **1000** and **100**P according to some example embodiments may reset power for an operation of the plurality of dies using a reset signal output from a single reset circuit. As a result, the system-on-chips **1000** and **100**P may operate the plurality of dies.

[0378] The above-described configurations may allow the system-on-chips **1000** and **100**P to significantly reduce an area and costs required to implement a circuit for resetting power of the plurality of dies and operating the plurality of devices.

[0379] Referring to the above-described configurations, the system-on-chips **1000** and **100**P according to some example embodiments may use reset signals, respectively output from an internal reset circuit and an external reset circuit **150**, to reset power of each of the reset signals by using a logic circuit.

[0380] As a result, the system-on-chips **1000** and **100**P may improve stability of a power-on reset operation for each of the plurality of dies.

[0381] FIG. **16** is a diagram illustrating a system-on-chip in which a first die according to some example embodiments further includes a plurality of level shifters.

[0382] Referring to FIG. **16**, a system-on-chip **100**Q according to some example embodiments may include a first die **111**Q and a second die **112**Q.

[0383] The system-on-chip **100**Q illustrated in FIG. **16** may be understood as an example of the system-on-chip **100** illustrated in FIG. **1**. Therefore, the same or substantially the same components are denoted by the same or substantially the same reference numerals, and redundant descriptions are omitted to avoid repetition.

[0384] The system-on-chip **100**Q may include a plurality of through-silicon vias (TSVs) TSV**1** and TSV**1** and a plurality of power vias PSV**1** and PSV**2** formed to penetrate through at least a portion of the first die **111**Q and the second die **112**Q.

[0385] Each of the plurality of TSVs, e.g., TSV**1** and TSV**1**, may be referred to as a path through which the first die **111**Q and the second die **112**Q exchange signals S**1** and S**2**. In some example embodiments, each of the plurality of power vias PSV**1** and PSV**2** may be referred to as a path through which the first die **111**Q and the second die **112**Q exchange power information PS**1** and PS**2**.

[0386] In some example embodiments, the first die **111**Q may include level shifters LS**1** and LS**2**, respectively connected to the plurality of TSVs TSV**1** and TSV**2**.

[0387] According to some example embodiments, the system-on-chip **100**Q may include a first TSV TSV**1** and a second TSV TSV**2** formed to penetrate through at least a portion of the first die **111**Q and the second die **112**Q.

[0388] The first die **111**Q may include a first level shifter LS**1** connected to the first TSV TSV**1**.

[0389] For example, the first die **111**Q may include a first level shifter LS**1** receiving a first signal S**1** transmitted, transferred, or sent from the second die **112**Q through the first TSV TSV**1**.

[0390] According to some example embodiments, a first processor **231**Q may control an operation of the first level shifter LS**1** based on the second power information PS**2** transmitted, transferred, or sent through the first power via PSV**1**.

[0391] For example, the first processor **231**Q may determine whether the second die **112**Q is operating, based on the second power information PS**2**.

[0392] According to some example embodiments, when the second die **112**Q is operating, the first processor **231**Q may control the first level shifter LS**1** to adjust a power level of the first signal S**1**.

[0393] For example, the first signal S**1** may be understood as a data signal transmitted, transferred, or sent from the

second die **112**Q to the first die **111**Q, but example embodiments are not limited thereto.

[0394] For example, when the second die **112**Q is operating, the first processor **231**Q may adjust the power level of the first signal S**1** through the first level shifter LS**1** based on power levels of the first voltage V**1** and the second voltage V**2**.

[0395] For example, when the second die **112**Q is operating and the first voltage V**1** has a first power level and the second voltage V**2** has a second power level, the first processor **231**Q may control the first level shifter LS**1** such that the first signal S**1** has a power level corresponding to the first power level.

[0396] For example, each the first and second power levels may be understood as having absolute values. For example, each of the first and second power levels may be understood as representing a range of power magnitude.

[0397] In some example embodiments, the first die **111**Q may include a second level shifter LS**2** connected to the second TSV TSV**2**.

[0398] For example, the first die **111**Q may include a second level shifter LS**2** transmitting, transferring, or sending the second signal S**2** to the second die **112**Q through the second TSV TSV**2**.

[0399] According to some example embodiments, when the first die **111**Q and the second die **112**Q are operating, the second level shifter LS**2** may be controlled to adjust the power level of the second signal S**2**.

[0400] For example, the second signal S**2** may be understood as a data signal transmitted from the first die **111**Q to the second die **112**Q, but example embodiments are not limited thereto.

[0401] For example, when the first die **111**Q and the second die **112**Q are operating, the first processor **231**Q may adjust the power level of the second signal S**2** through the second level shifter LS**2** based on the power levels of the first voltage V**1** and the second voltage V**2**.

[0402] For example, when the second die **112**Q is operating and the first voltage V**1** has a first power level and the second voltage V**2** has a second power level, the first processor **231**Q may control the second level shifter LS**2** such that the second signal S**2** has a power level corresponding to the second power level.

[0403] Referring to the above-described configurations according to some example embodiments, the system-on-chip **100**Q may adjust the power levels of the signals S**1** and S**2** exchanged between the first die **111**Q and the second die **112**Q to correspond to a transmitted, transferred, or sent power level of a die using the level shifters LS**1** and LS**2**.

[0404] As a result, the system-on-chip **100**Q may significantly reduce leakage current that may be generated during signal exchange between the plurality of dies **111**Q and **112**Q.

[0405] According to some example embodiments, when the second die **112**Q is not operating, the first processor **231**Q may control the first level shifter LS**1** such that the first level shifter LS**1** outputs a predetermined, or alternatively desired value.

[0406] For example, when the second die **112**Q is not operating, the first processor **231**Q may control the first level shifter LS**1** such that the first level shifter LS**1** outputs a predetermined, or alternatively desired value regardless of a signal transmitted, transferred, or sent from the second die **112**Q.

[0407] For example, when an unknown signal from the non-operating second die **112**Q is introduced into the first die **111**Q, the first processor **231**Q may control the first level shifter LS**1** such that the first level shifter LS**1** outputs a predetermined value of "1."

[0408] In some example embodiments, the first processor **231**Q may control the second level shifter LS**2** such that the second level shifter LS**2** outputs a predetermined value when the first die **111**Q is not operating and the second die **112**Q is operating.

[0409] For example, if the second die **112**Q is operating and the first die **111**Q is not operating, the first processor **231**Q may control the second level shifter LS**2** such that the second level shifter LS**2** outputs a predetermined value of "0."

[0410] Referring to the above-described configurations, the first processor **231**Q according to some example embodiments may control the first level shifter LS**1** such that an unknown signal is not transmitted from a non-operating die to an operating die when only one of the plurality of dies **111**Q and **112**Q is operating.

[0411] As a result, the system-on-chip **100**Q may significantly reduce the likelihood of a malfunction in an operating die caused by an unknown signal introduced into the operating die from a non-operating die among the plurality of dies **111**Q and **112**Q.

[0412] As described above, the system-on-chip **100** according to some example embodiments may output different reset signals RS**1** and RS**2** for each of the plurality of dies **111** and **112** using the reset circuits **211** and **212**, respectively provided within the plurality of dies **111** and **112**.

[0413] As a result, the system-on-chip **100** according to some example embodiments may independently and reliably control a power-on reset operation on each of the plurality of dies **111** and **112**.

[0414] Furthermore, the system-on-chip **100** may reliably control power for the operation of each of the plurality of dies **111** and **112**.

[0415] According to some example embodiments, the first processor **231** and the second processor **232** may determine whether another die is operating based on the power information PS**1** and PS**2** received through the power management circuit **221** and **222**.

[0416] Furthermore, in some example embodiments each of the first and second processors **231** and **232** may perform an operation that requires an interaction between the first die **111** and the second die **112** in response to another die being operating.

[0417] As a result, the system-on-chip **100** may reduce the time it takes to turn on (or operate) the power of the plurality of dies **111** and **112** when an interaction between the plurality of dies **111** and **112** is required.

[0418] In some example embodiments, the system-on-chip **100** may reliably control the power for the operation of each of the plurality of dies **111** and **112** when an interaction between the plurality of dies **111** and **112** is required.

[0419] According to some example embodiments, the system-on-chip **100** may adjust power levels of the signals S**1** and S**2** exchanged between the first die **111** and the second die **112** to correspond to a transmitted, transferred, or sent power level of a die using the level shifters LS**1** and LS**2**.

[0420] As a result, the system-on-chip **100** may significantly reduce leakage current that may be generated during signal exchange between the plurality of dies **111** and **112**.

[0421] According to some example embodiments, the first processor **231** may control the first level shifter LS**1** such that an unknown signal is not transmitted from a non-operating die to an operating die when only one of the plurality of dies **111** and **112** is operating.

[0422] As a result, the system-on-chip **100** may significantly reduce the likelihood of a malfunction in the operating die caused by an unknown signal introduced from the non-operating die to the operating die among the plurality of dies **111** and **112**.

[0423] As set forth above, a system-on-chip according to some example embodiments may stably control power for the operation of each of a plurality of dies.

[0424] While some example embodiments have been shown and described above, it will be apparent to those skilled in the art that modifications and variations could be made without departing from the scope of the present inventive concepts as defined by the appended claims.

What is claimed is:

1. A system-on-chip (SoC), comprising:
a first die; and
a second die adjacent to a surface of the first die, the second die connected to the first die,
the first die including a first reset circuit configured to output a first reset signal to operate the first die based on a first voltage received from a power supply, and
the second die including a second reset circuit configured to output a second reset signal to operate the second die based on a second voltage received from the power supply.

2. The system-on-chip of claim **1**, wherein
the first die comprises a first power management circuit configured to send first power information of the first die to the second die, and receive second power information of the second die from the second die, and
the second die comprises a second power management circuit configured to send the second power information of the second die to the first die, and receive the first power information of the first die from the first die.

3. The system-on-chip of claim **2**, wherein
the first die comprises a first processor configured to operate the first die in response to the first reset signal, and
the first processor is configured to,
determine whether the second die is operating based on the second power information; and
control an operation of the first die, based on a data signal received from the second die, when the second die is operating.

4. The system-on-chip of claim **3**, wherein
the first processor is configured to output a first operation request to operate the second die to at least one of the power supply and the second reset circuit when the second die is not operating.

5. The system-on-chip of claim **3**, wherein
the second die comprises a second processor configured to operate the second die in response to the second reset signal, and
the second processor is configured to,
determine whether the first die is operating based on the first power information, and
control an operation of the second die based on a data signal received from the first die when the first die is operating.

6. The system-on-chip of claim **5**, wherein
an external reset circuit is configured to output an external first reset signal based on the first voltage received from the power supply,
the first die further comprises a first logic circuit configured to output a first output reset signal based on at least a portion of the first reset signal and the first external reset signal, and
the first processor is configured to operate the first die in response to the first output reset signal.

7. The system-on-chip of claim **6**, wherein
the first logic circuit is configured to output the first output reset signal through an AND operation between the first reset signal and the first external reset signal.

8. The system-on-chip of claim **6**, wherein
the external reset circuit is configured to output an external second reset signal based on the second voltage,
the second die further comprises a second logic circuit configured to output a second output reset signal based on at least a portion of the second reset signal and the second external reset signal, and
the second processor is configured to operate the second die in response to the second output reset signal.

9. The system-on-chip of claim **1**, wherein
the second die is connected to the first die through a plurality of pads on the surface of the first die.

10. The system-on-chip of claim **3**, wherein
the first die and the second die are connected through a plurality of through-silicon vias (TSVs),
the first die comprises a first level shifter configured to receive a first signal sent from the second die through a first through-silicon via, and
the first processor, based on the second power information, is configured to,
control the first level shifter such that the first signal has a power level corresponding to a first power level of the first voltage when the second die is operating; and
control the first level shifter such that the first level shifter outputs a value when the second die is not operating.

11. A system-on-chip (SoC), comprising:
a first die;
a second die adjacent to a surface of the first die, the second die connected to the first die through a plurality of pads on the surface of the first die; and
an external reset circuit configured to output a first reset signal based on a first voltage received from a power supply, and output a second reset signal based on a second voltage received from the power supply,
the first die configured to operate with the first voltage in response to the first reset signal, and
the second die configured to operate with the second voltage in response to the second reset signal.

12. The system-on-chip of claim **11**, wherein
the first die comprises,
a first processor configured to operate the first die in response to the first reset signal; and
a first power management circuit configured to send first power information of the first die to the second

die and receive second power information of the second die from the second die, and

the first processor is configured to,

determine whether the second die is operating based on the second power information; and

control the operation of the first die based on a data signal received from the second die when the second die is operating.

13. The system-on-chip of claim **12**, wherein

the first processor is configured to output a first operation request to operate the second die to at least a portion of the power supply and the external reset circuit when the second die is not operating.

14. The system-on-chip of claim **12**, wherein

the second die comprises,

a second processor configured to operate the second die in response to the second reset signal; and

a second power management circuit configured to receive the first power information from the first die and send the second power information to the first die, and

the second processor is configured to,

determine whether the first die is operating based on the first power information; and

control an operation of the second die based on a data signal received from the first die when the first die is operating.

15. The system-on-chip of claim **12**, wherein

the first die and the second die are connected through a plurality of through-silicon vias (TSVs),

the first die comprises a first level shifter configured to receive a first signal sent from the second die through a first through-silicon via, and

the first processor, based on the second power information, is configured to,

control the first level shifter such that the first signal has a power level corresponding to a first power level of the first voltage when the second die is operating; and

control the first level shifter such that the first level shifter outputs a value when the second die is not operating.

16. A system-on-chip (SoC), comprising:

a first die; and

a second die adjacent to a surface of the first die, the second die connected to the first die through a plurality of pads on the surface of the first die,

the first die including a first reset circuit configured to output a first reset signal to operate the first die based on a supply voltage received from a power supply, and

the second die including a second reset circuit configured to output a second reset signal, different from the first reset signal, to operate the second die based on the supply voltage.

17. The system-on-chip of claim **16**, wherein

the first die comprises a first power management circuit configured to send first power information of the first die to the second die, and receive second power information of the second die from the second die, and

the second die comprises a second power management circuit configured to send the second power information of the second die to the first die, and receive the first power information of the first die from the first die.

18. The system-on-chip of claim **17**, wherein

the first die comprises a first processor configured to operate the first die in response to the first reset signal, and

the first processor is configured to,

determine whether the second die is operating based on the second power information; and

control an operation of the first die based on a data signal received from the second die when the second die is operating.

19. The system-on-chip of claim **18**, further comprising:

an external reset circuit configured to output an external reset signal based on the supply voltage,

the first die further including a first logic circuit configured to output a first output reset signal through a logical AND operation between the first reset signal and the external reset signal, and

the first processor configured to operate the first die in response to the first output reset signal.

20. The system-on-chip of claim **19**, wherein

the second die further comprises,

a second processor configured to control an operation of the second die; and

a second logic circuit configured to output a second output reset signal through a logical AND operation between the second reset signal and the external reset signal, and

the second processor is configured to operate the second die in response to the second output reset signal.

* * * * *