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(54) **METHOD OF TRANSPORTING SEMICONDUCTOR DEVICE AND CARRIER TAPE**

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(52) **U.S. Cl.**
CPC ***H01L 21/6836*** (2013.01); *H01L 2221/68313* (2013.01)

(57) **ABSTRACT**

A method of transporting a semiconductor device includes: a step of placing a semiconductor device in a pocket portion, a step of attaching the cover tape to the carrier tape so as to cover the semiconductor device placed in the pocket portion, and a step of transporting the carrier tape containing the semiconductor device. Here, the pocket portion includes: a plurality of corner portions where a step section is formed, and a plurality of side portions located between these corner portions and having a first protruding portion and a second protruding portion formed thereon. Also, a width of a tip portion of the second protruding portion is smaller than a width of the tip portion of the first protruding portion. Furthermore, a protrusion amount of the second protruding portion from the side portion is larger than a protrusion amount of the first protruding portion from the side portion.

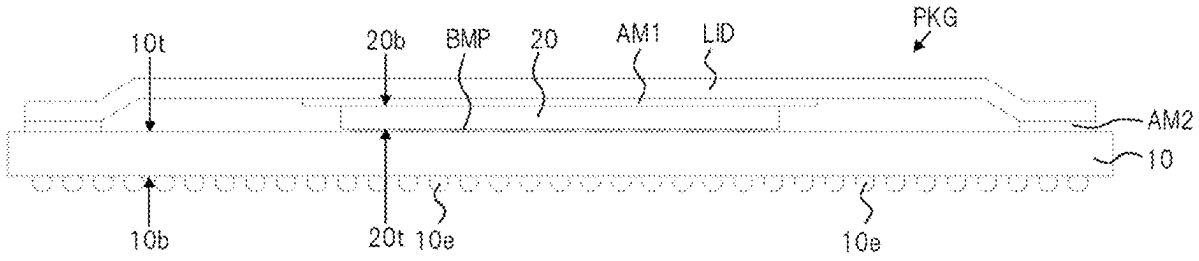


FIG. 1

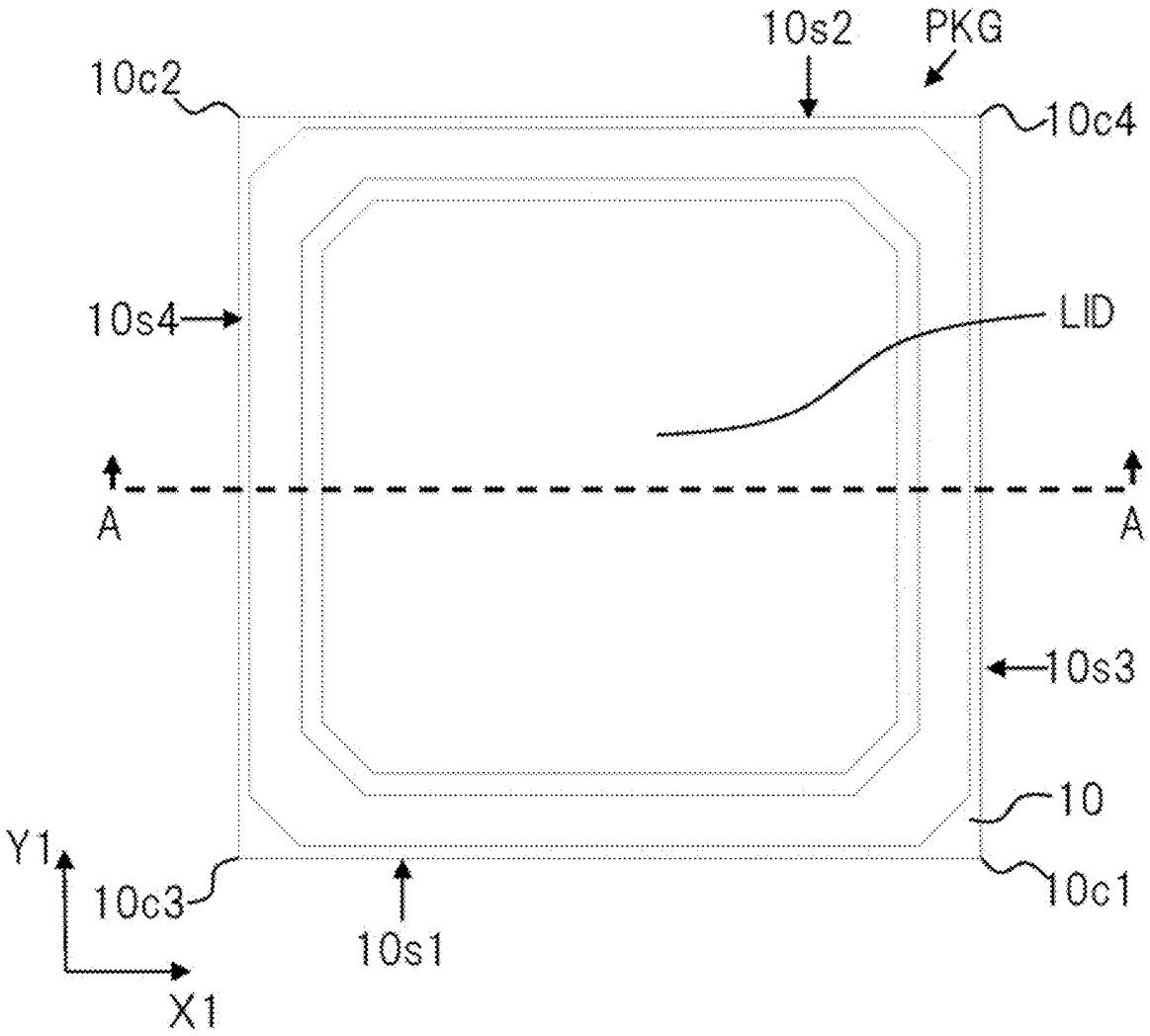


FIG. 2

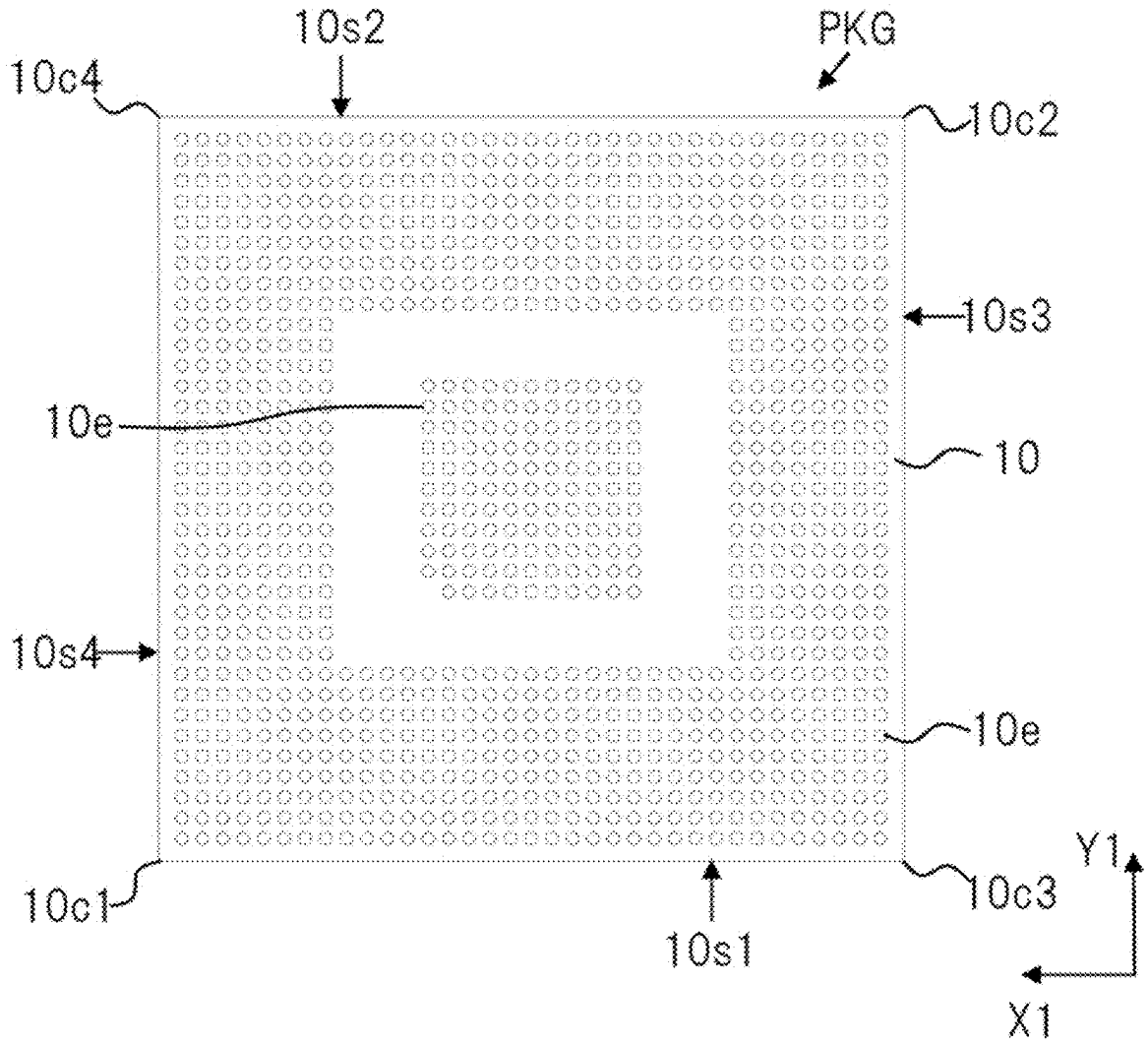


FIG. 3

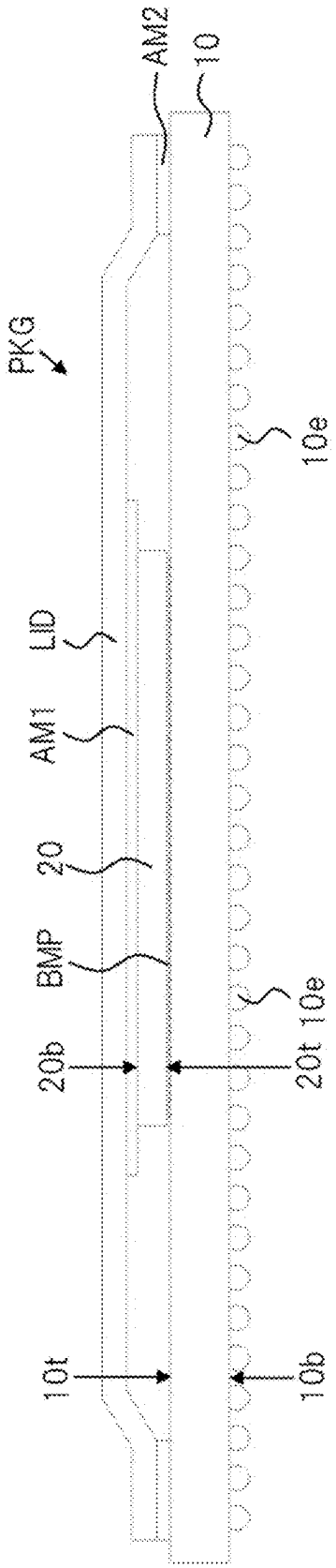
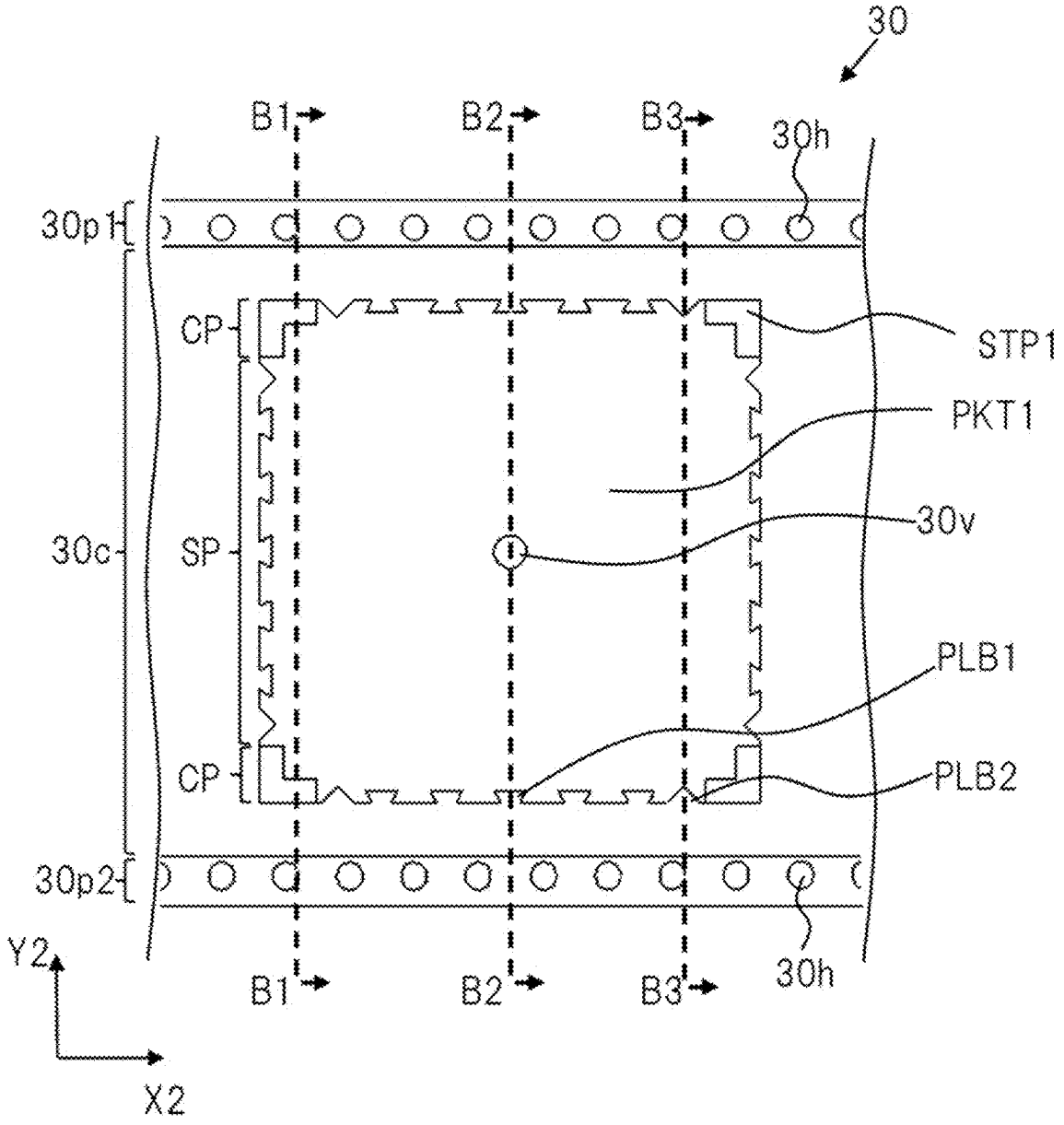


FIG. 4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B1
B2
B3
30h
30p1
CP
STP1
PKT1
30c
SP
30v
PLB1
CP
PLB2
30p2
B1
B2
B3
30h
Y2
X2

FIG. 5

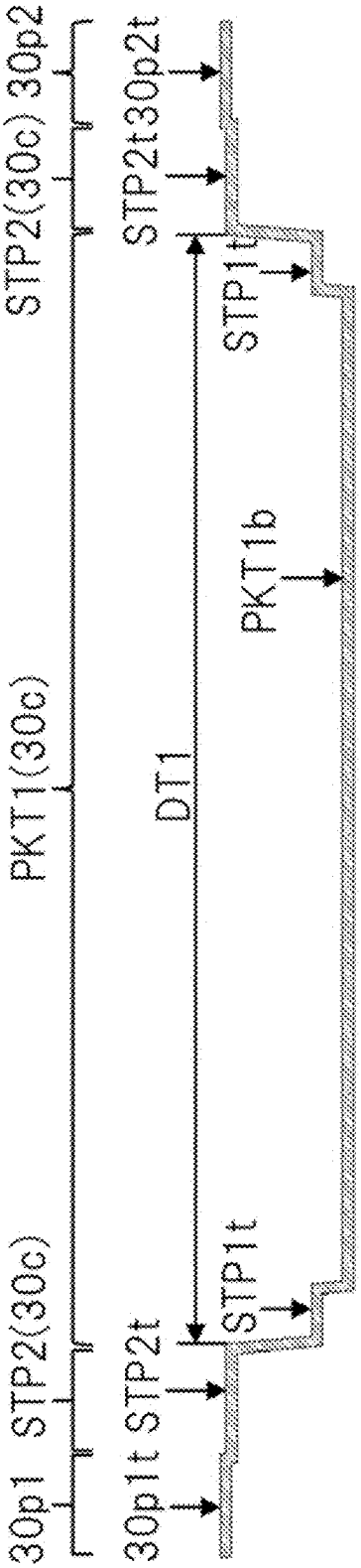
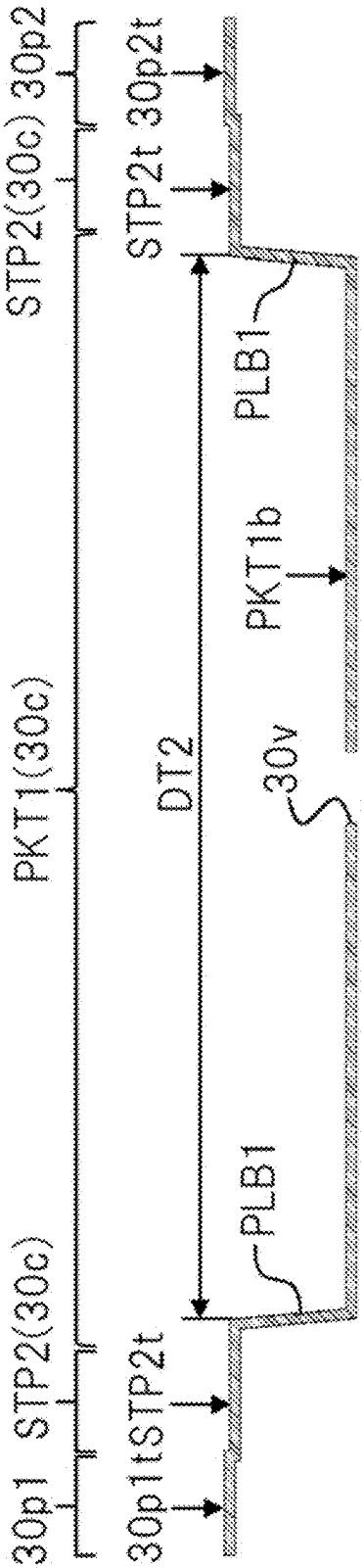

30p1
STP2(30c)
PKT1(30c)
STP2(30c) 30p2
30p1t
STP2t
DT1
STP1t
STP2t30p2t
STP1t
PKT1b

FIG. 6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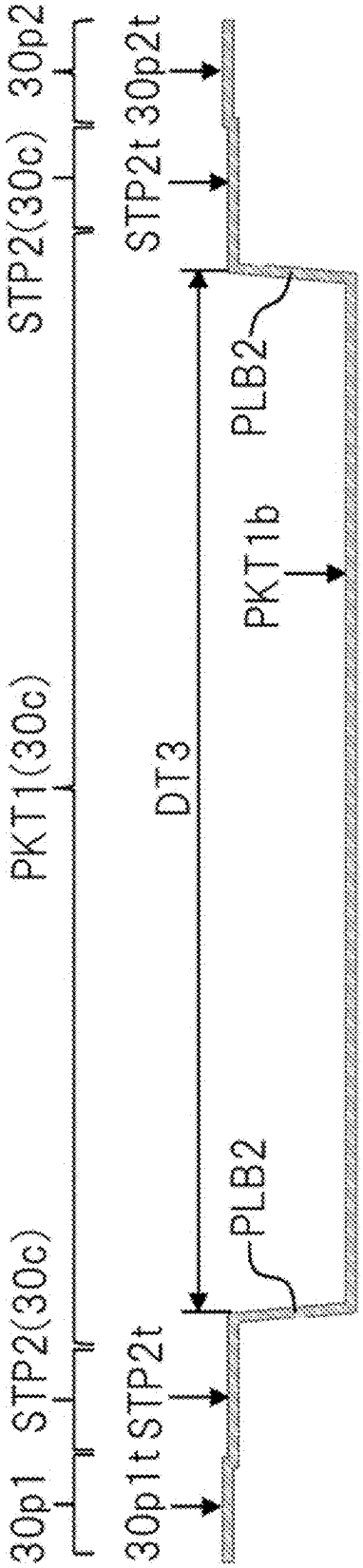
STP2(30c)
30p2
30p1t
STP2t
30p2t
PKT1(30c)
DT2
30v
PKT1b
PLB1
PLB1

FIG. 7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STP2(30c)
PKT1(30c)
STP2(30c)
30p2
30p1t
STP2t
DT3
PLB2
STP2t
30p2t
PKT1b
PLB2

FIG. 8

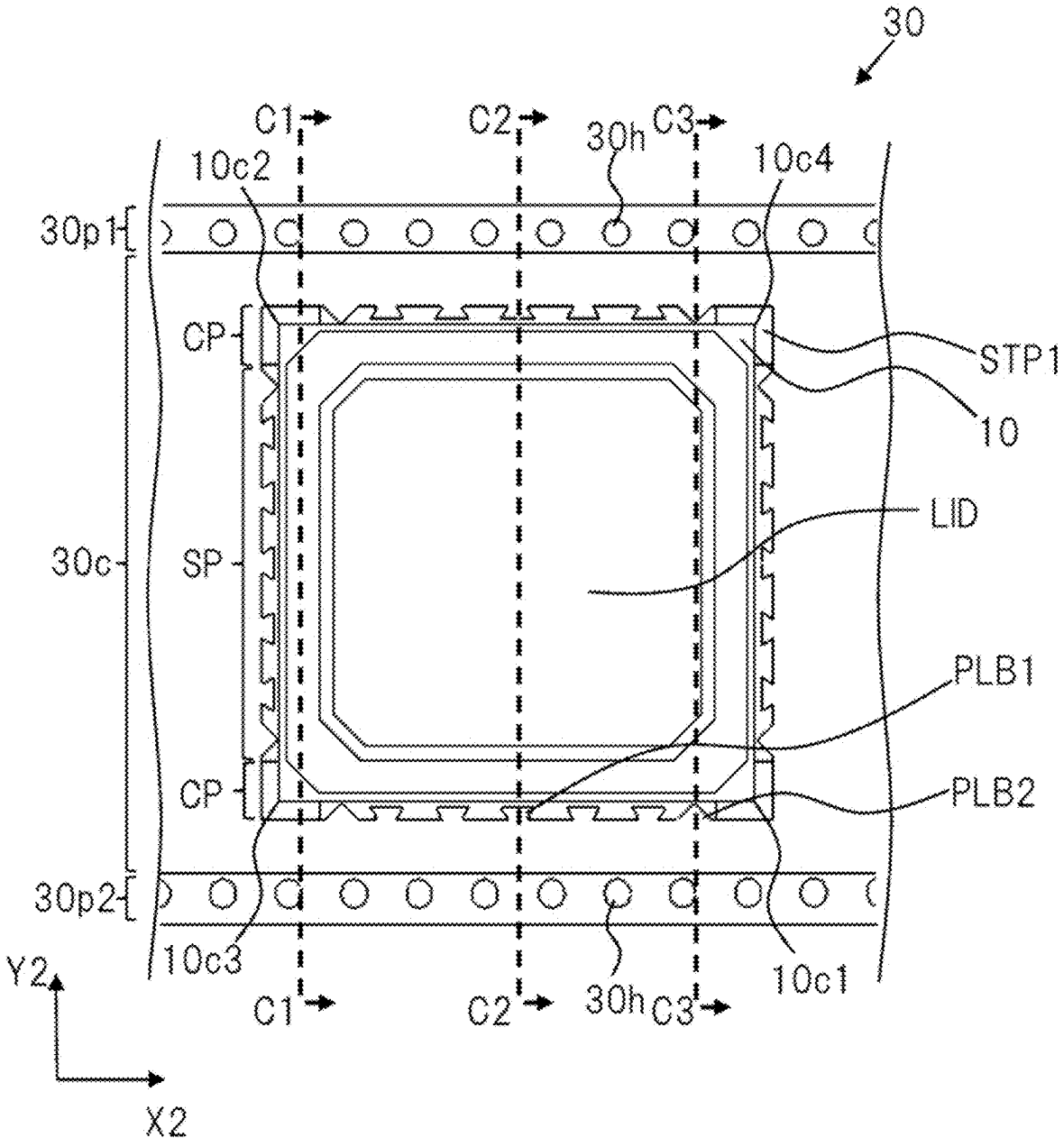
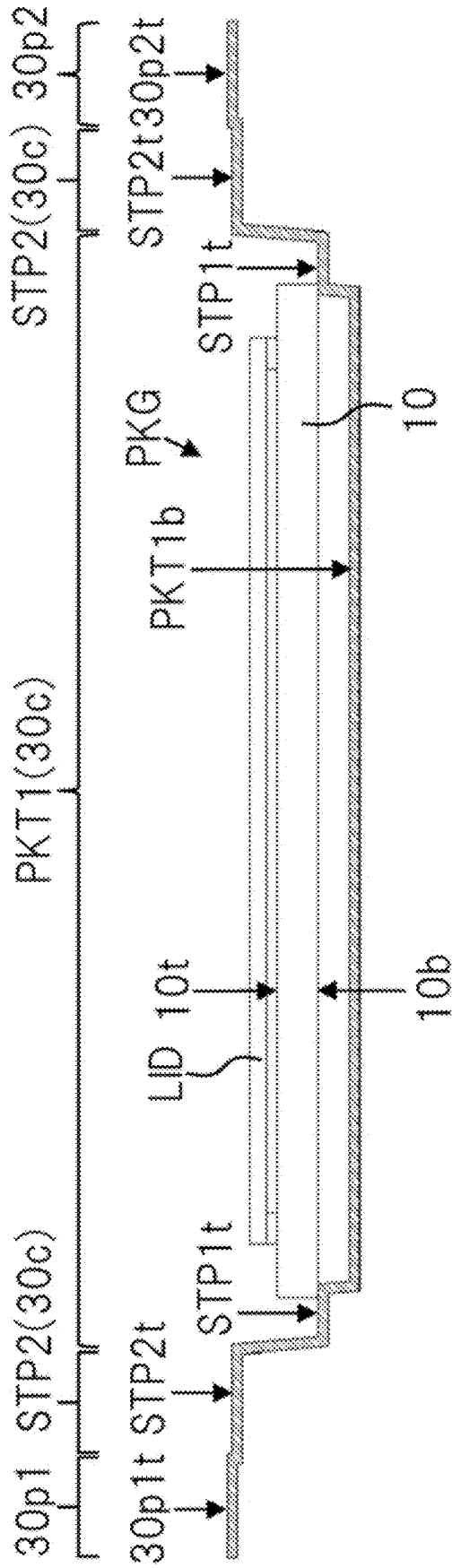

30
C1
C2
30h
C3
10c2
10c4
30p1
CP
STP1
10
30c
SP
LID
PLB1
CP
PLB2
30p2
10c3
10c1
C1
C2
30h
C3
Y2
X2

FIG. 9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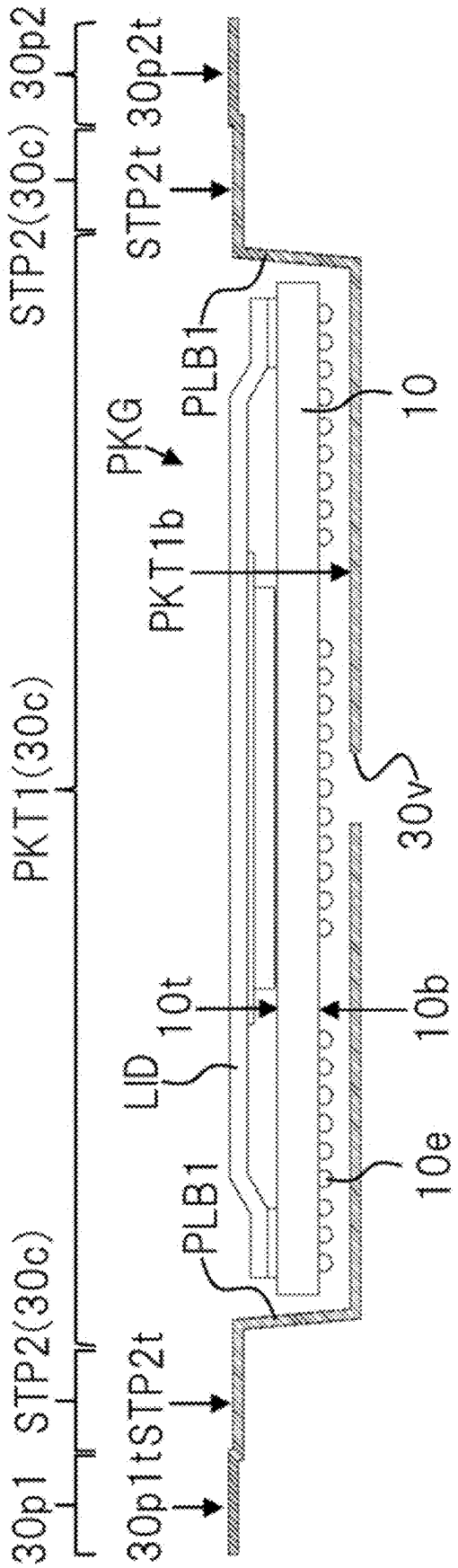
STP2(30c)
PKT1(30c)
STP2(30c)
30p2
30p1t
STP2t
STP1t
LID
10t
PKG
PKT1b
STP1t
STP2t
30p2t
10
10b

FIG. 10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STP2(30c)
30p1t
STP2t
PKT1(30c)
STP2(30c)
30p2
STP2t
30p2t
PLB1
PKG
PKT1b
LID
10t
PLB1
10
30v
10b
10e

FIG. 11

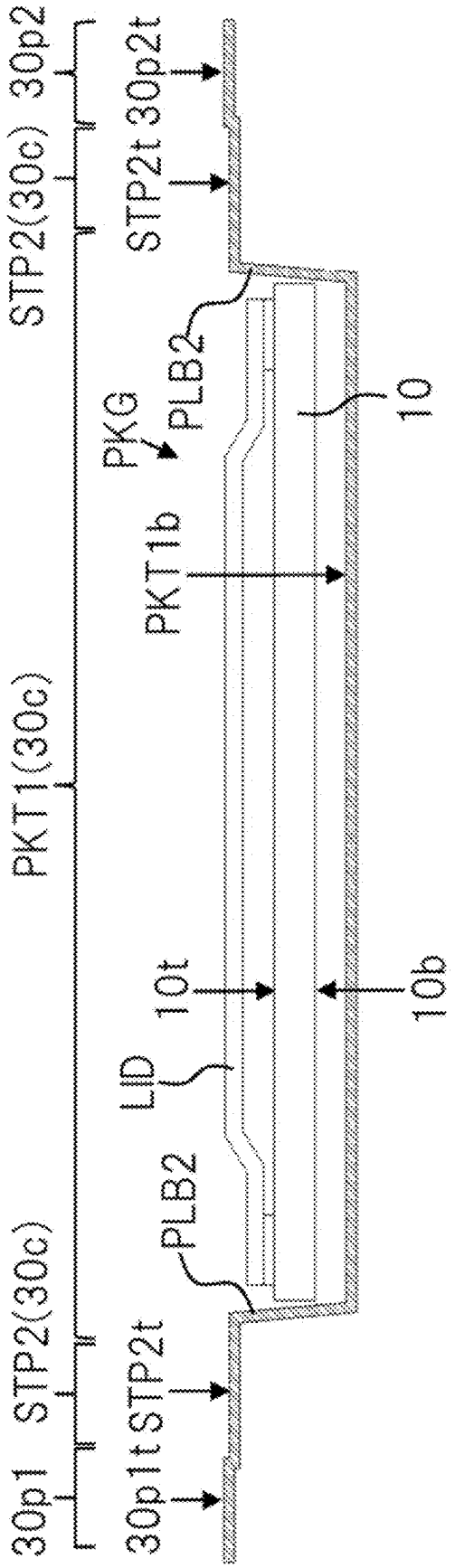

30p1
STP2(30c)
30p2
30p1t
STP2t
PLB2
PKT1(30c)
LID
10t
PKG
PKT1b
STP2(30c)
30p2
STP2t
30p2t
PLB2
10
10b

FIG. 12

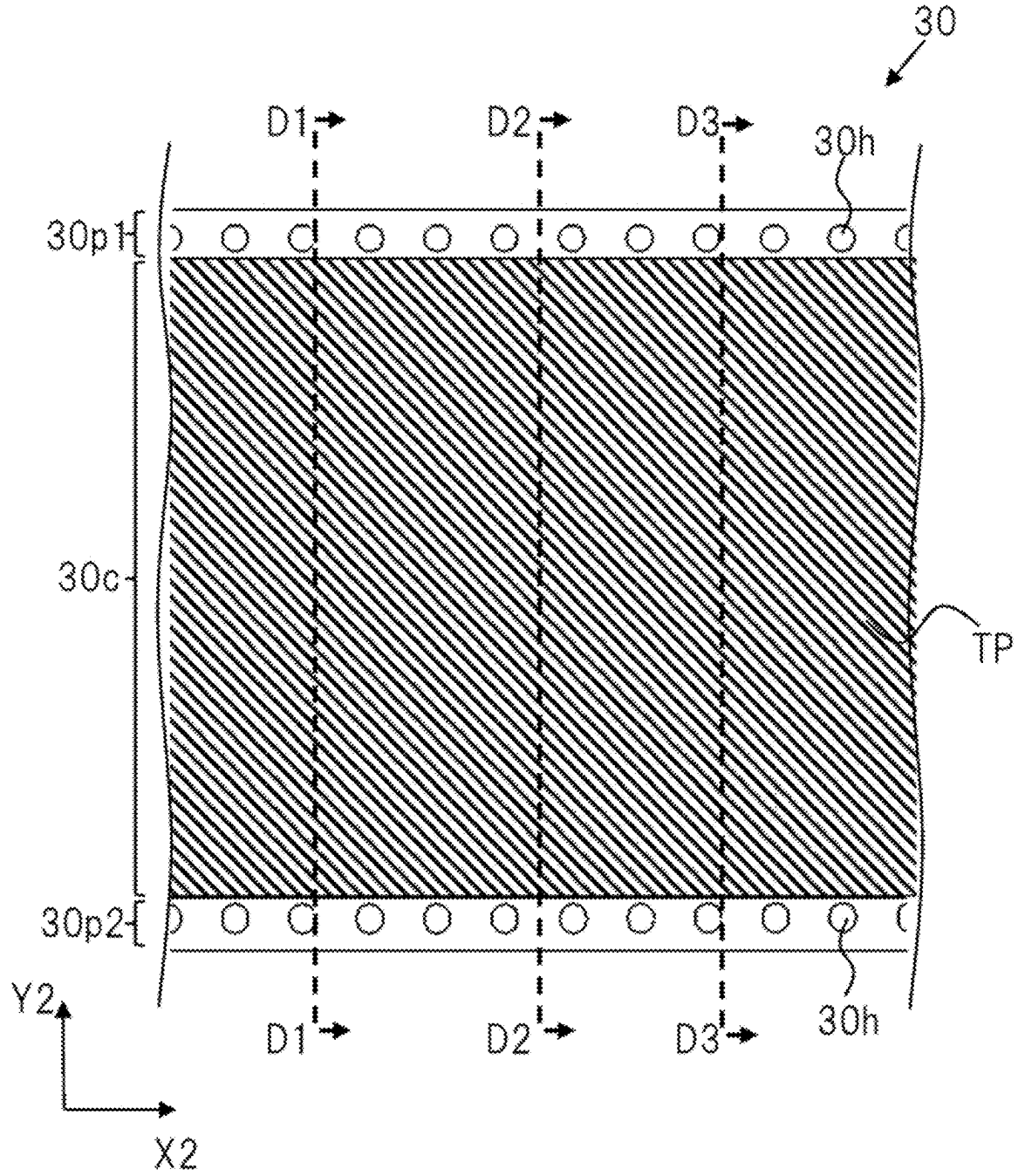


FIG. 13

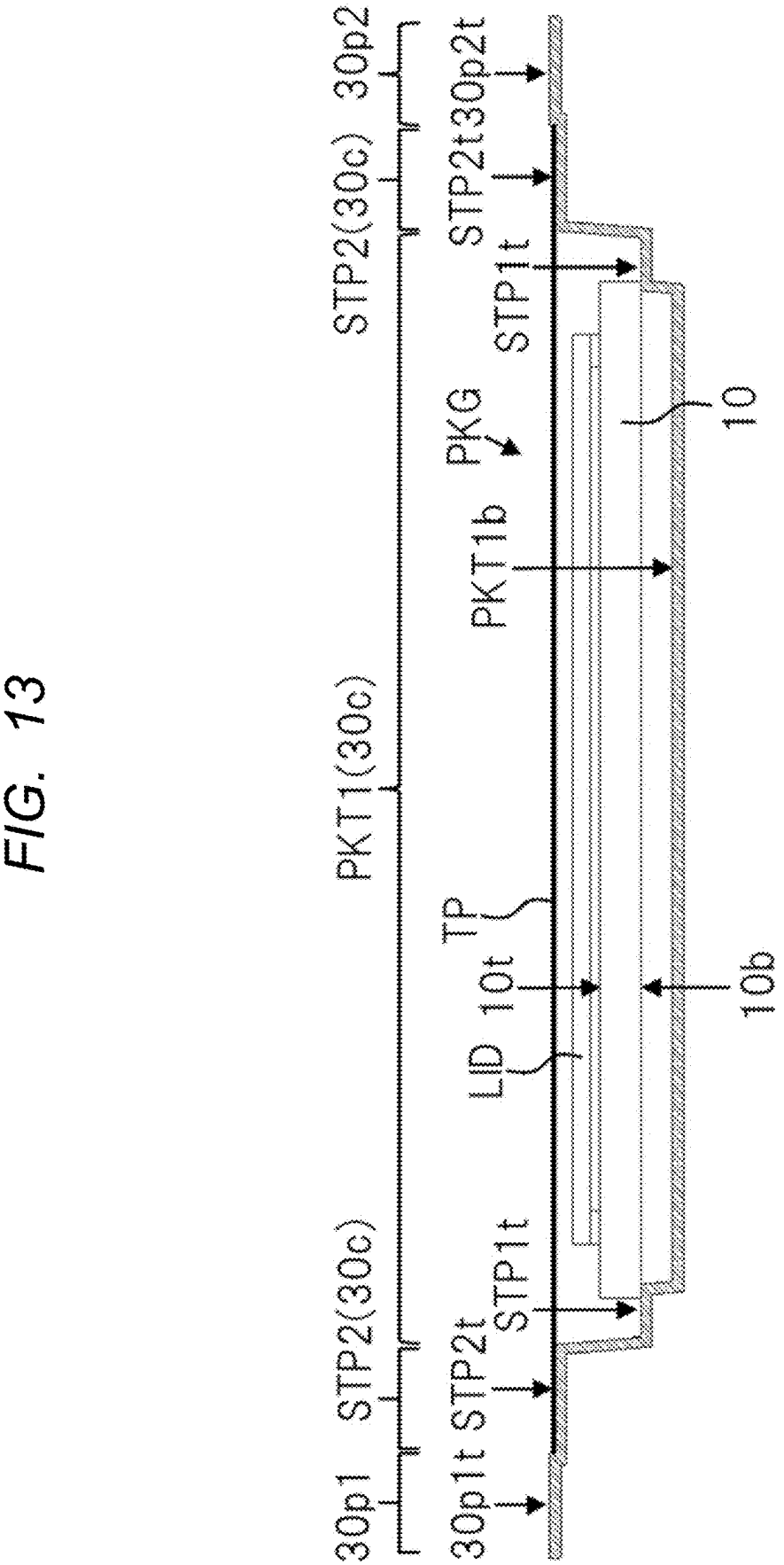

30p1
STP2(30c)
30p1t
STP2t
STP1t
LID
10t
TP
PKT1(30c)
PKT1b
PKG
STP1t
STP2t
30p2t
STP2(30c)
30p2
10
10b

FIG. 14

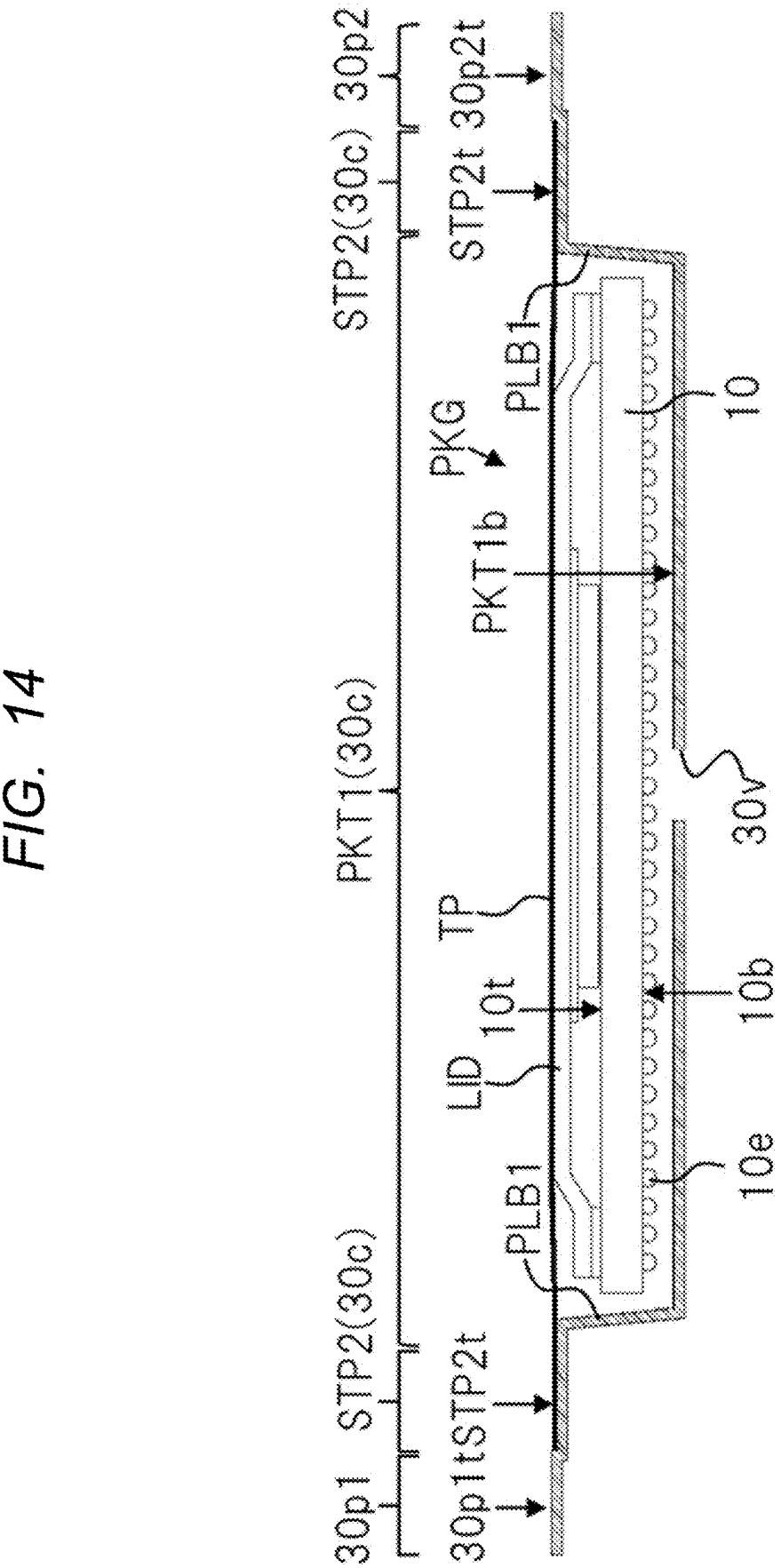

30p1
STP2(30c)
30p1t
STP2t
30p2
STP2(30c)
STP2t
30p2t
PKT1(30c)
PLB1
PKG
PLB1t
PKT1b
10
LID
10t
TP
30v
10b
10e

FIG. 15

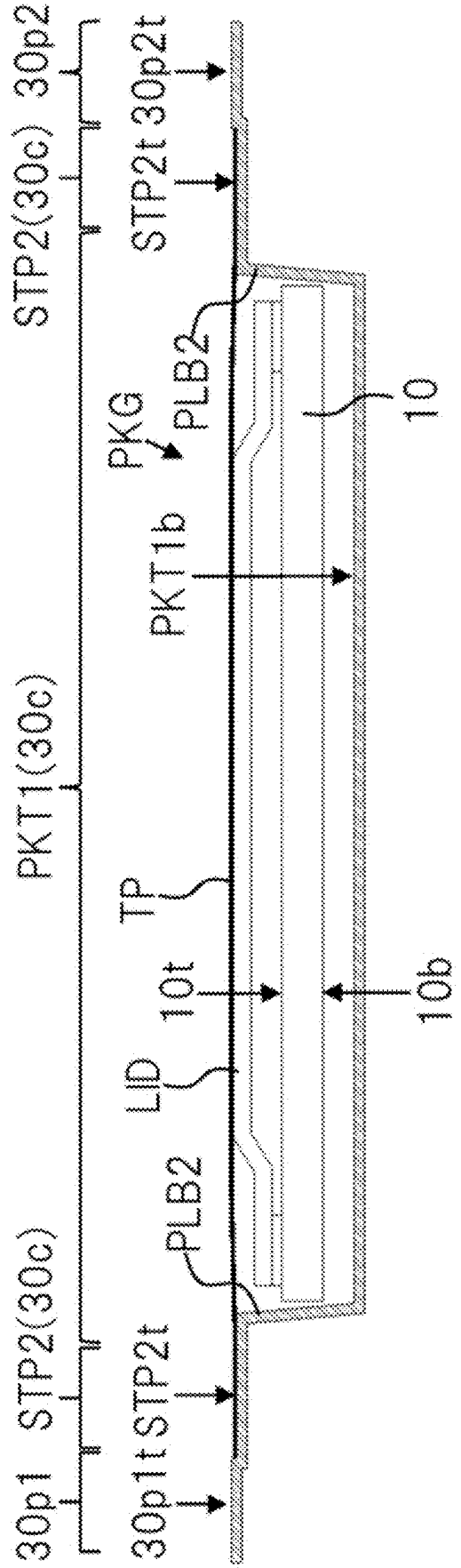

30p1
STP2(30c)
30p1t
STP2t
PLB2
LID
10t
TP
PKT1(30c)
PKT1b
PKG
PLB2
STP2t
STP2(30c)
30p2
30p2t
10
10b

FIG. 16

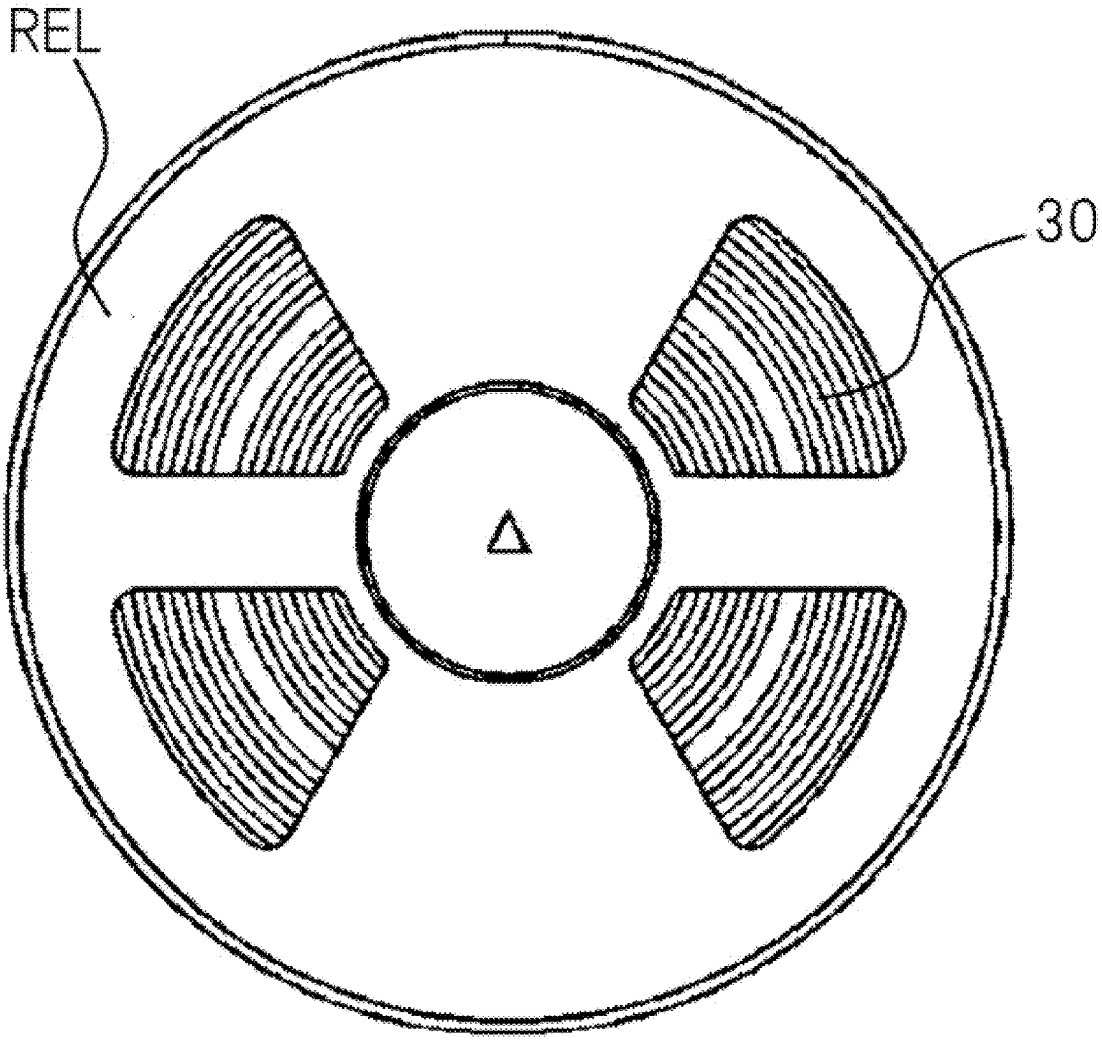


FIG. 17

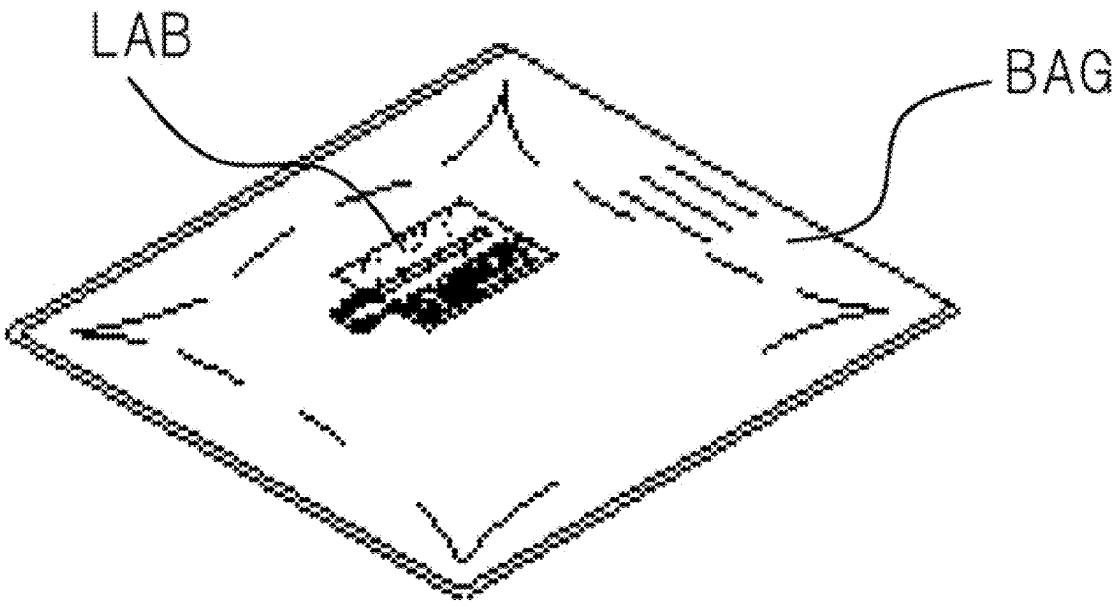


FIG. 18

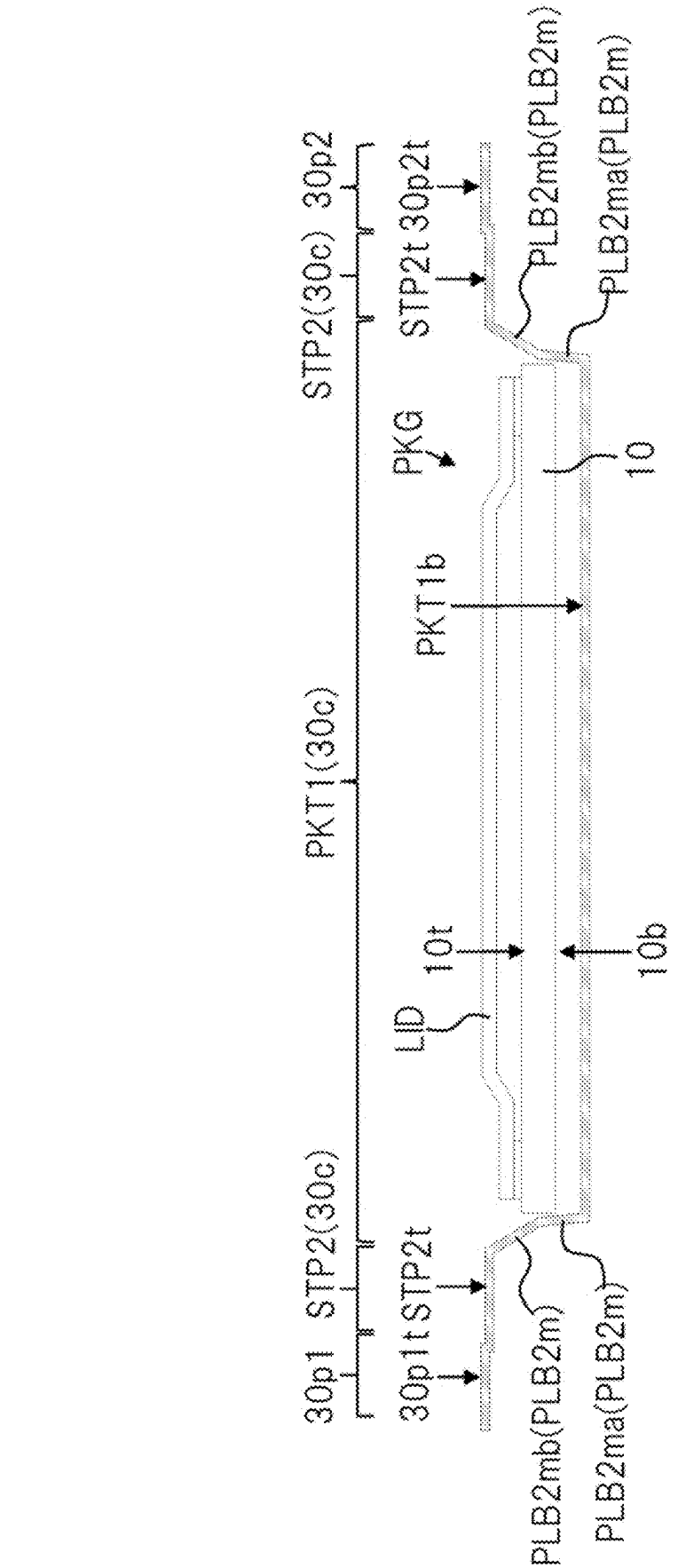

30p1
STP2(30c)
30p1t
STP2t
PLB2mb(PLB2m)
PLB2ma(PLB2m)
PKT1(30c)
LID
10t
10b
PKT1b
PKG
STP2(30c)
30p2
STP2t
30p2t
PLB2mb(PLB2m)
PLB2ma(PLB2m)
10

FIG. 19

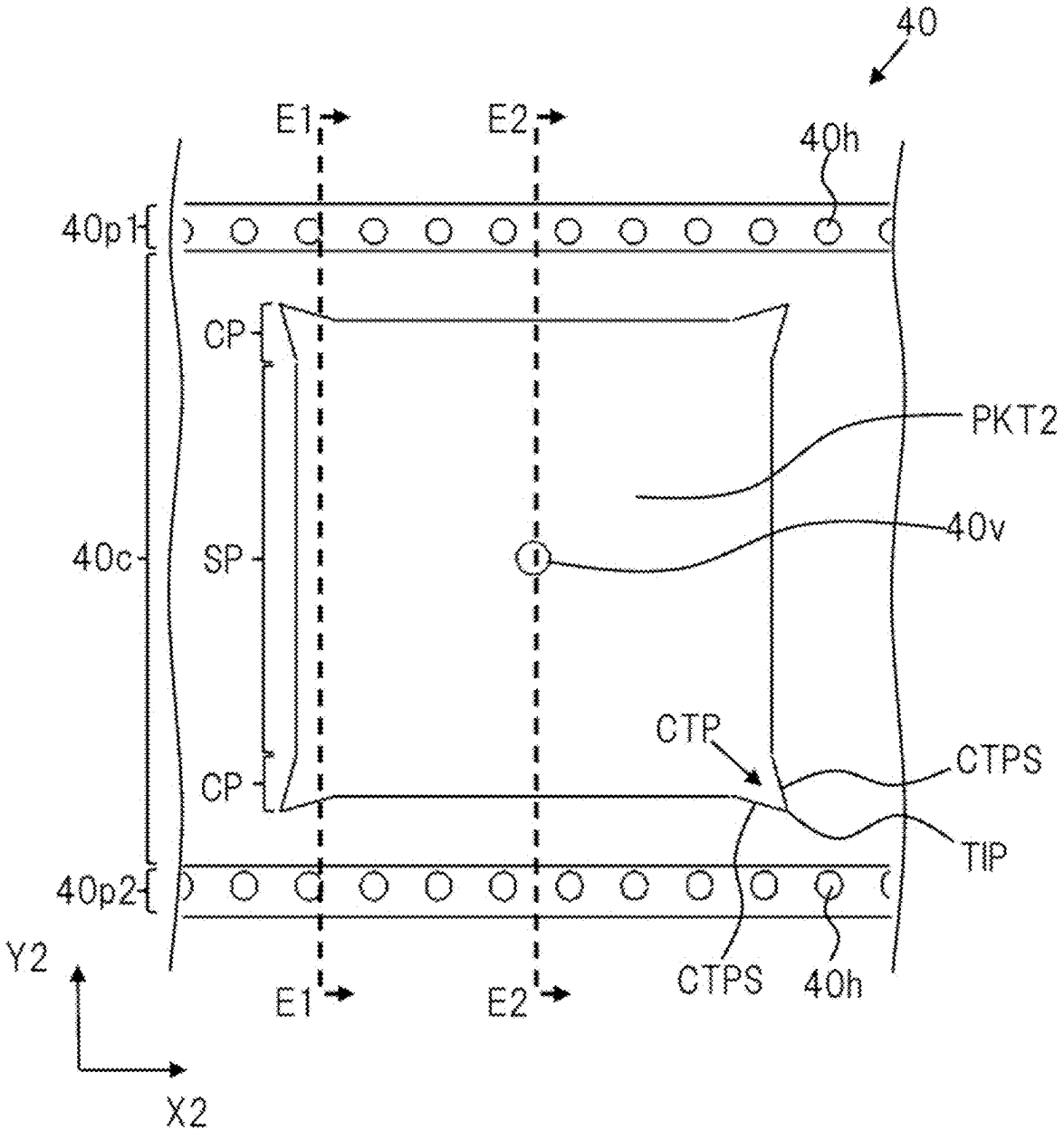

40
E1
E2
40h
40p1
CP
PKT2
40c
SP
40v
CTP
CTPS
CP
TIP
40p2
Y2
E1
E2
CTPS
40h
X2

FIG. 20

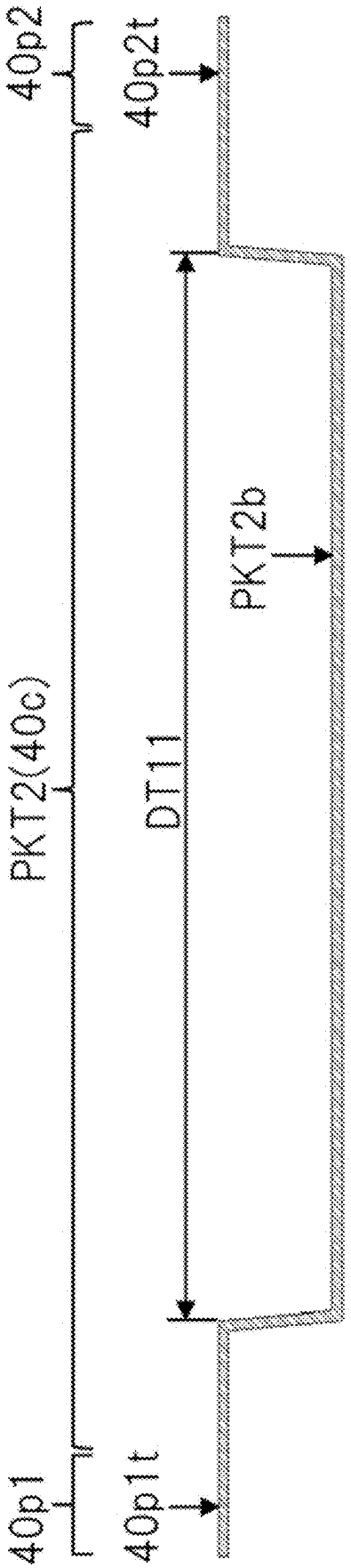


FIG. 21

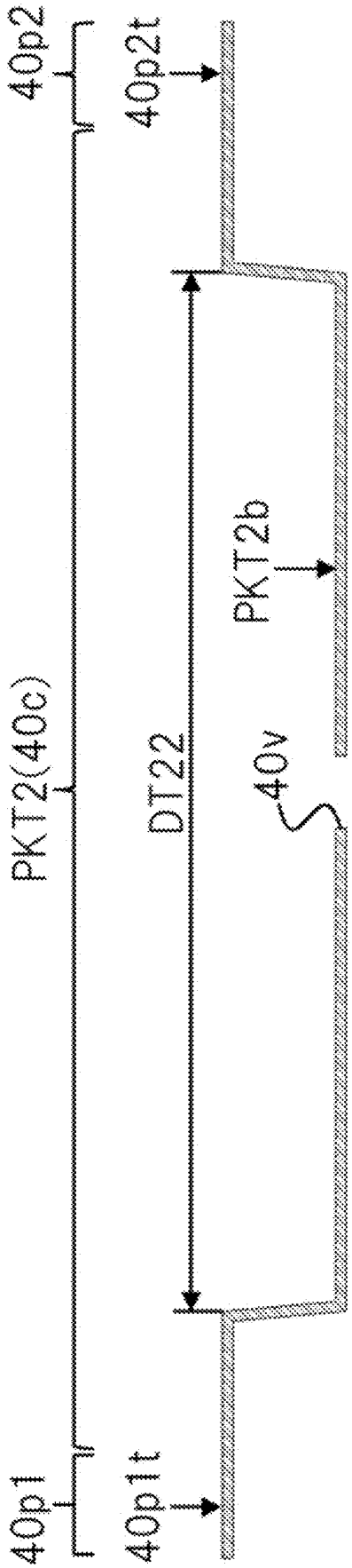


FIG. 22

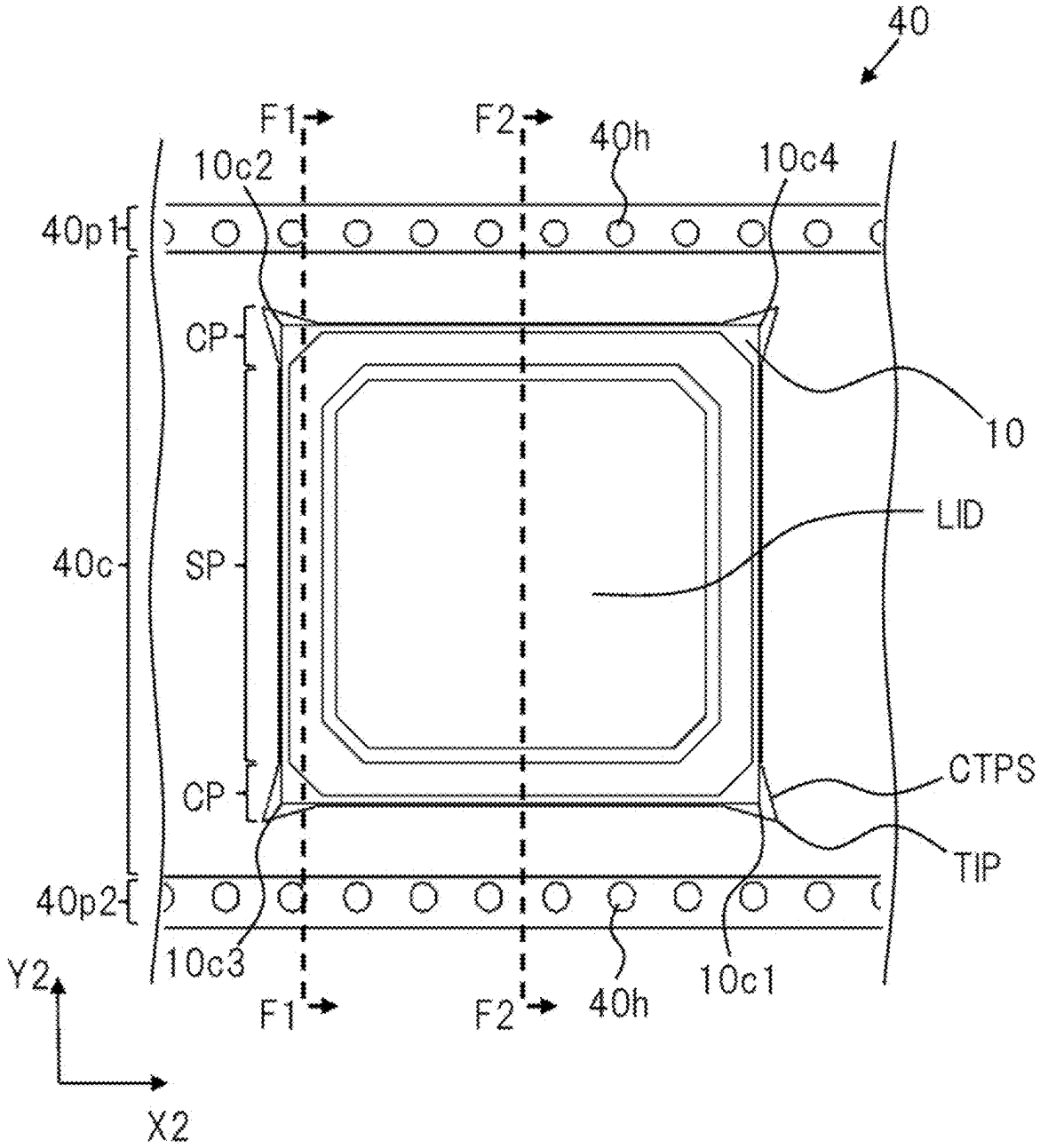

40
F1
F2
40h
10c2
10c4
40p1
CP
10
LID
40c
SP
CP
CTPS
TIP
40p2
10c3
10c1
F1
F2
40h
Y2
X2

FIG. 23

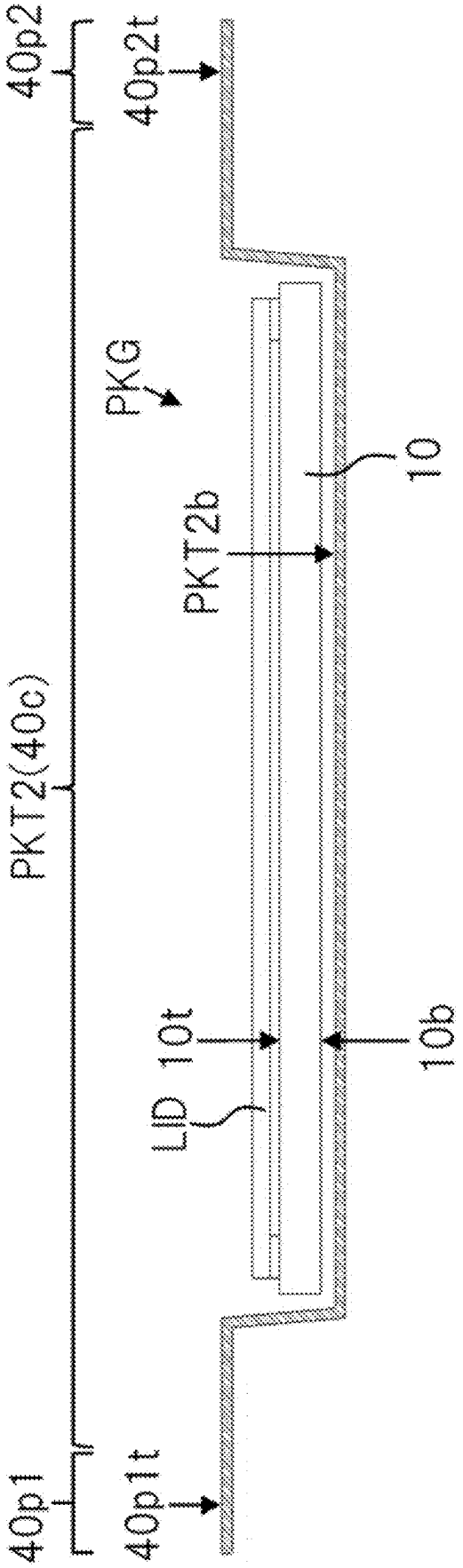


FIG. 24

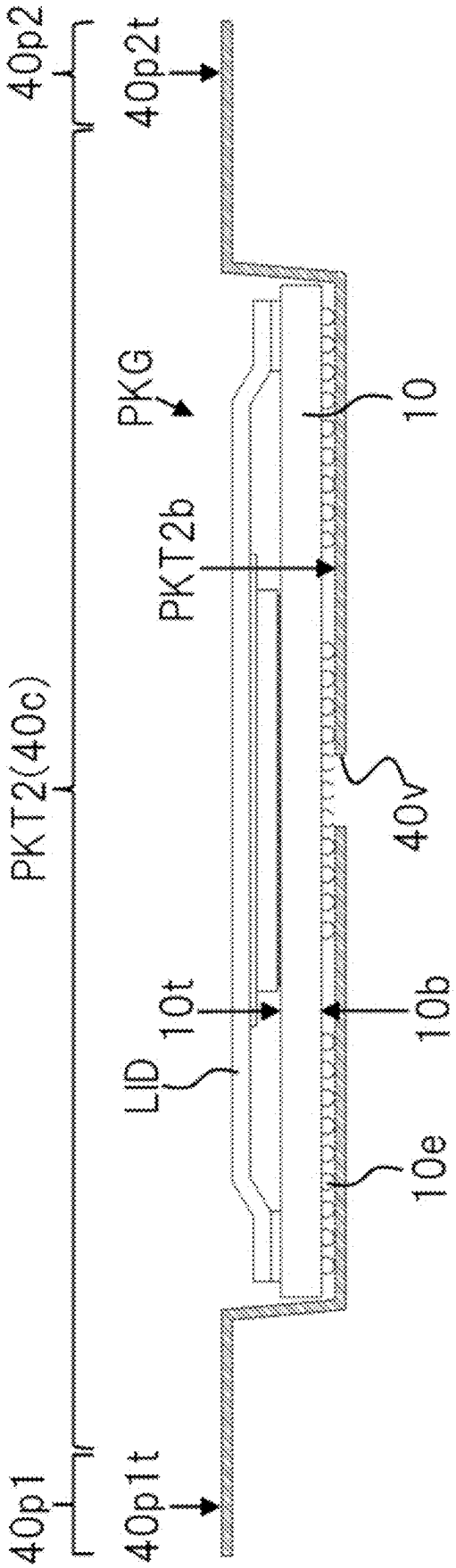

40p2
40p2t
PKG
10
PKT2b
PKT2(40c)
40v
LID
10t
10b
10e
40p1
40p1t

FIG. 25

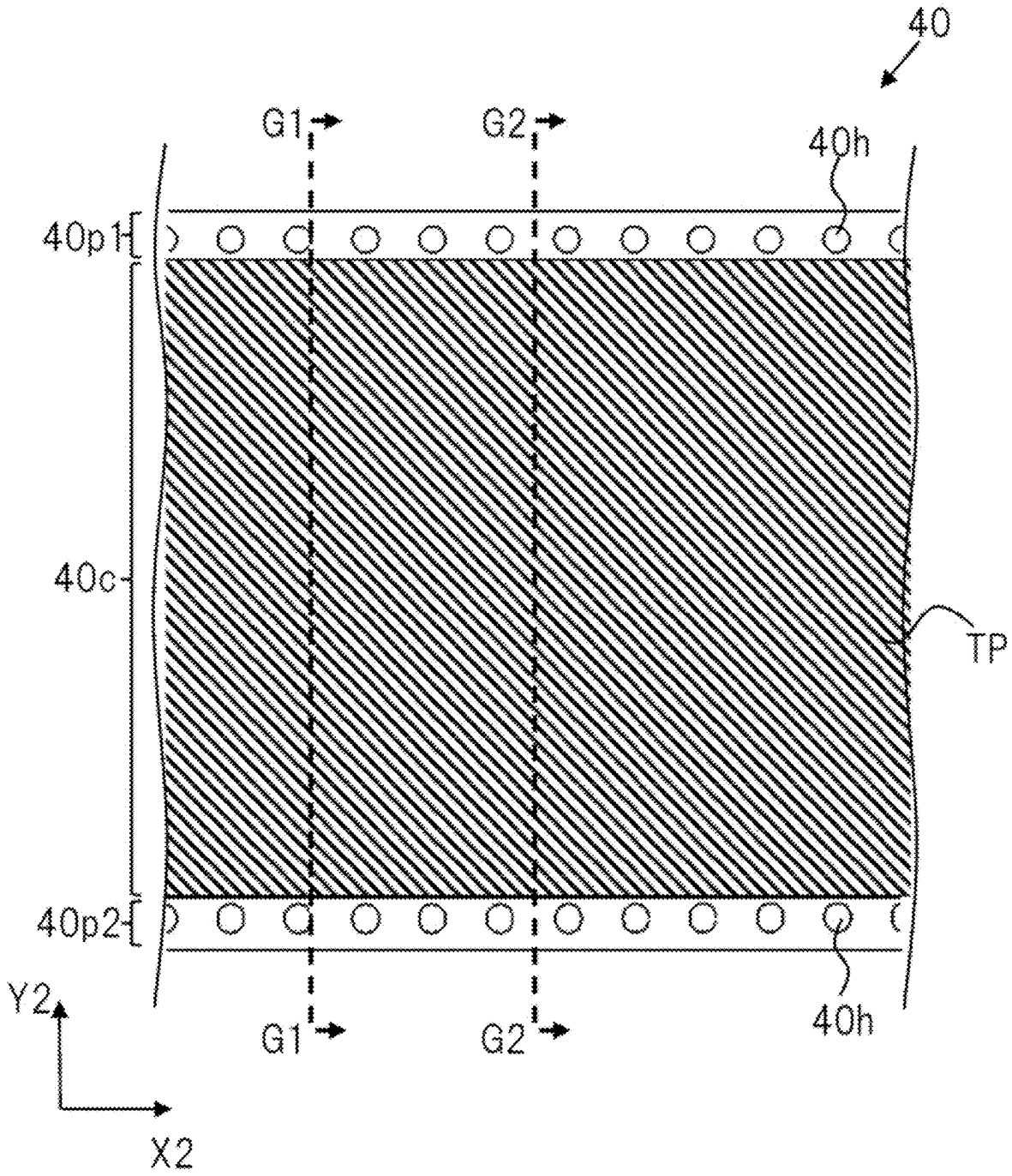


FIG. 26

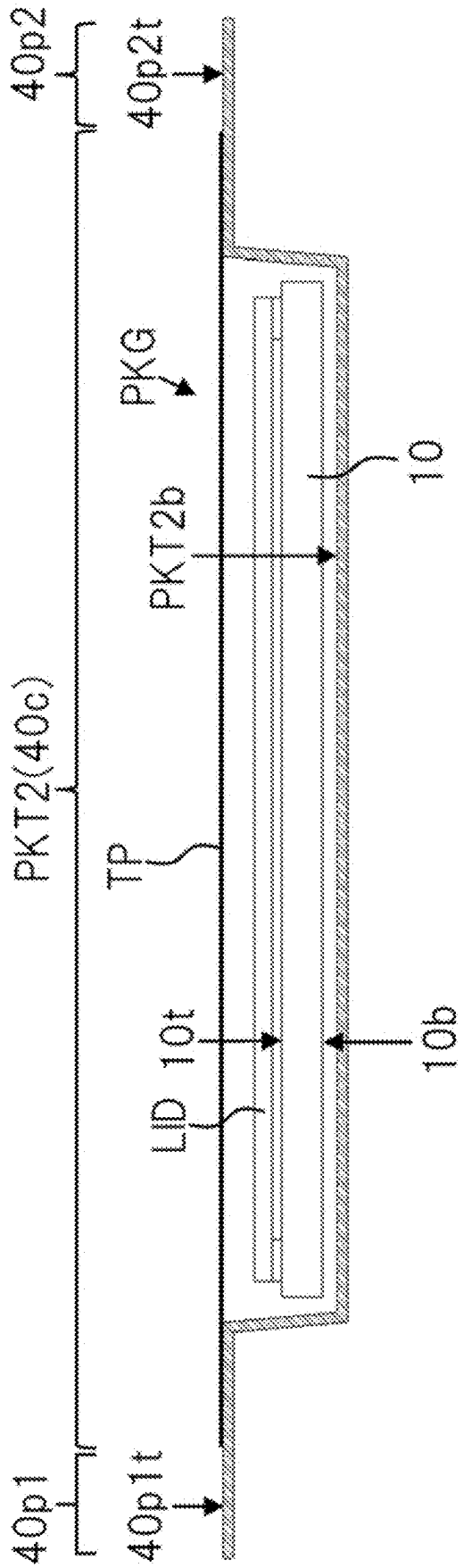


FIG. 27

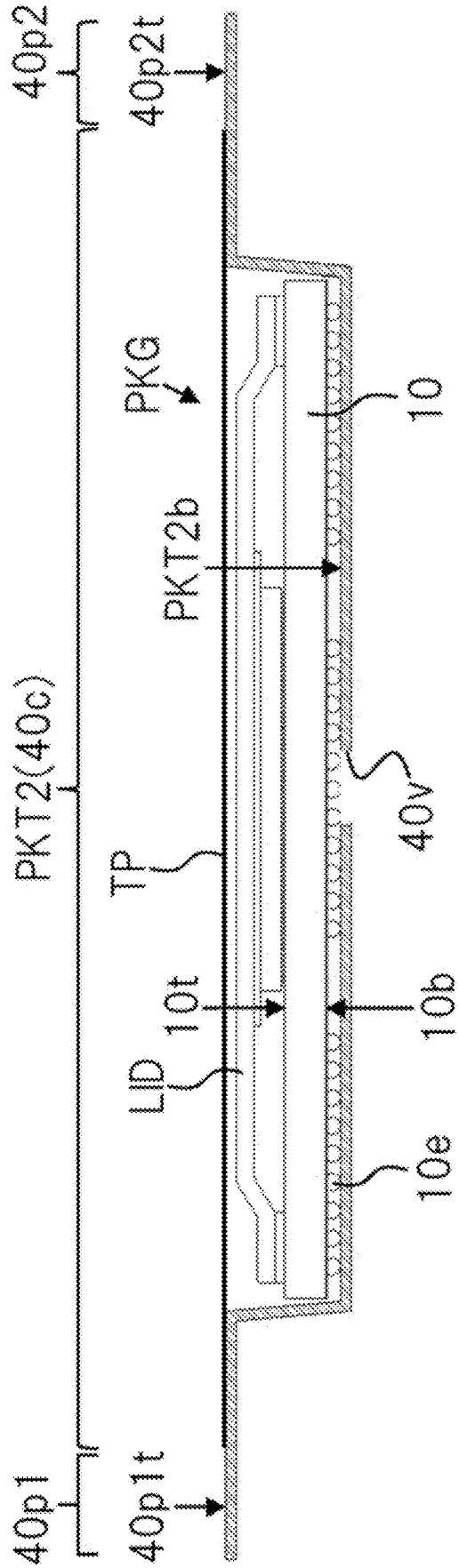

40p2
40p2t
PKG
10
PKT2b
PKT2(40c)
TP
40v
LID
10t
10b
10e
40p1
40p1t

FIG. 28

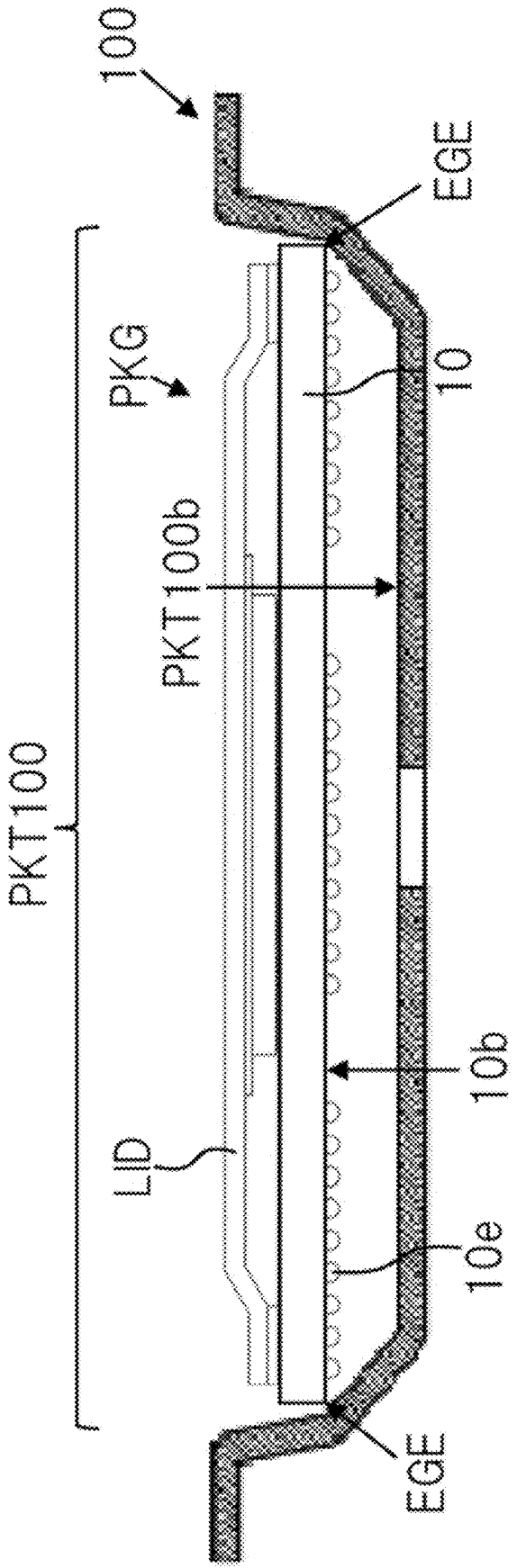
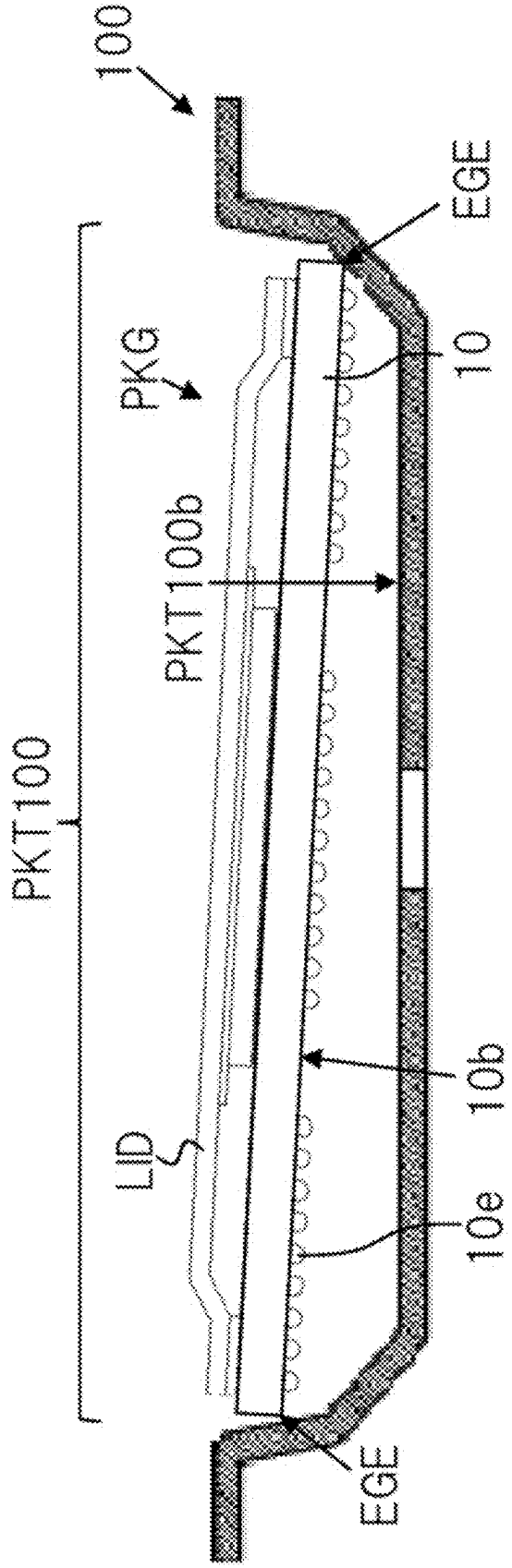


FIG. 29



METHOD OF TRANSPORTING SEMICONDUCTOR DEVICE AND CARRIER TAPE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The disclosure of Japanese Patent Application No. 2024-023986 filed on Feb. 20, 2024, including the specification, drawings and abstract is incorporated herein by reference in its entirety.

BACKGROUND

[0002] The present invention relates to a method of transporting a semiconductor device and to a carrier tape.

[0003] There are disclosed techniques listed below. [Patent Document 1] Japanese Unexamined Patent Application Publication No. 2018-002211

[0004] Patent Document 1 discloses accommodating a semiconductor device in an accommodating portion (pocket portion) of a carrier tape that has been embossed.

SUMMARY

[0005] As methods of transporting semiconductor devices, there are methods using a tray made of resin and using a carrier tape. In the method using the tray, a manufactured semiconductor device is accommodated in a plurality of accommodating portions (pocket portions) provided in a matrix array on a surface of the tray. To prevent the semiconductor device from popping out of the accommodating portions during transportation of this tray, another tray is placed over the tray containing the semiconductor device, and they are transported in this state. In contrast, in the method using the carrier tape, after accommodating the manufactured semiconductor device in the accommodating portions of the carrier tape, to prevent the semiconductor device from popping out of the accommodating portions during transportation of this carrier tape, the semiconductor device is covered with a cover tape. Then, the carrier tape having a surface to which the cover tape is attached is wound onto a reel, and transported in this state. If it is desired to increase the number of semiconductor devices to be transported, the length of the carrier tape wound onto the reel can be increased.

[0006] The present inventors have been considering to transport the semiconductor device including a wiring board, such as BGA (Ball Grid Array) or LGA (Land Grid Array), by using the carrier tape. According to the review of the present inventors, it has been found that when transporting the semiconductor device by using the carrier tape, vibrations and shocks during the transportation of the carrier tape containing the semiconductor devices may cause foreign substances to be generated. These foreign substances are a part of the material composing the carrier tape. The generation of foreign substances may lead to a decrease in the reliability of the semiconductor device or may cause a problem when mounting the semiconductor device taken out from the carrier tape onto a mounting board. Therefore, a shape (structure) of the accommodating portion that can suppress the generation of foreign substances as much as possible is desired.

[0007] Other objects and novel features will become apparent from the description of this specification and the accompanying drawings.

[0008] A method of transporting a semiconductor device according to one embodiment includes: a step of placing a semiconductor device in a pocket portion of a carrier tape, a step of attaching a cover tape to the carrier tape so as to cover the semiconductor device placed in the pocket portion, and a step of transporting the carrier tape containing the semiconductor device. Here, the pocket portion includes: a plurality of corner portions where a step section is formed, and a plurality of side portions located between these corner portions and having a first protruding portion and a second protruding portion formed thereon. Moreover, a width of a tip portion of the second protruding portion is smaller than a width of the tip portion of the first protruding portion. Furthermore, a protrusion amount of the second protruding portion from the side portion is larger than a protrusion amount of the first protruding portion from the side portion.

[0009] A carrier tape according to one embodiment includes a pocket portion including: a plurality of corner portions where a step portion is formed, and a plurality of side portions located between these corner portions and where the first protruding portion and the second protruding portion are formed. Furthermore, a width of the tip portion of the second protruding portion is smaller than a width of the tip portion of the first protruding portion. Moreover, a protrusion amount of the second protruding portion from the side portion is larger than a protrusion amount of the first protruding portion from the side portion.

[0010] A method of transporting a semiconductor device according to one embodiment includes: a step of placing a semiconductor device in a pocket portion of a carrier tape, a step pf attaching a cover tape to the carrier tape so as to cover the semiconductor device placed in the pocket portion, and a step of transporting the carrier tape containing the semiconductor device. Here, the pocket portion includes: a plurality of corner portions having a notch portion, and a plurality of side portions located between these corner portions. Furthermore, a planar shape of two sides forming the notch portion draws an arc so as to curve from each of the first side portion and the second side portion, which are adjacent to the notch portion, towards an apex of the notch portion. Moreover, the notch portion is provided such that a distance between the two sides of the notch portion gradually decreases towards the apex of the notch portion.

[0011] According to the above embodiment, it is possible to suppress the reduction in reliability of the semiconductor device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. **1** is an upper surface view of a semiconductor device according to one embodiment.

[0013] FIG. **2** is a lower surface view of the semiconductor device shown in FIG. **1**.

[0014] FIG. **3** is a cross-sectional view taken along line A-A in FIG. **1**.

[0015] FIG. **4** is an enlarged plan view at a portion of a carrier tape according to one embodiment.

[0016] FIG. **5** is a cross-sectional view taken along a line B**1**-B**1** in FIG. **4**.

[0017] FIG. **6** is a cross-sectional view taken along a line B**2**-B**2** in FIG. **4**.

[0018] FIG. **7** is a cross-sectional view taken along a line B**3**-B**3** in FIG. **4**.

[0019] FIG. **8** is an enlarged plan view at the portion of the carrier tape after a step shown in FIG. **4**.

[0020] FIG. **9** is a cross-sectional view taken along a line C**1**-C**1** in FIG. **8**.
[0021] FIG. **10** is a cross-sectional view taken along a line C**2**-C**2** in FIG. **8**.
[0022] FIG. **11** is a cross-sectional view taken along a line C**3**-C**3** in FIG. **8**.
[0023] FIG. **12** is an enlarged plan view at the portion of the carrier tape after a step shown in FIG. **8**.
[0024] FIG. **13** is a cross-sectional view taken along a line D**1**-D**1** in FIG. **12**.
[0025] FIG. **14** is a cross-sectional view taken along a line D**2**-D**2** in FIG. **12**.
[0026] FIG. **15** is a cross-sectional view taken along a line D**3**-D**3** in FIG. **12**.
[0027] FIG. **16** is a view showing a state in which the carrier tape is wound on a reel after a step shown in FIG. **12**.
[0028] FIG. **17** is a view showing a state in which the reel shown in FIG. **16** is accommodated in a moisture-proof bag.
[0029] FIG. **18** is a cross-sectional view of a carrier tape according to a modified example.
[0030] FIG. **19** is an enlarged plan view at a portion of a carrier tape according to another embodiment.
[0031] FIG. **20** is a cross-sectional view taken along a line E**1**-E**1** in FIG. **19**.
[0032] FIG. **21** is a cross-sectional view taken along a line E**2**-E**2** in FIG. **19**.
[0033] FIG. **22** is an enlarged plan view at the portion of the carrier tape after a step shown in FIG. **19**.
[0034] FIG. **23** is a cross-sectional view taken along a line F**1**-F**1** in FIG. **22**.
[0035] FIG. **24** is a cross-sectional view taken along a line F**2**-F**2** in FIG. **22**.
[0036] FIG. **25** is an enlarged plan view at the portion of the carrier tape after a step shown in FIG. **22**.
[0037] FIG. **26** is a cross-sectional view taken along a line G**1**-G**1** in FIG. **25**.
[0038] FIG. **27** is a cross-sectional view taken along a line G**2**-G**2** in FIG. **25**.
[0039] FIG. **28** is a cross-sectional view showing a state in which a semiconductor device is accommodated in an accommodating portion of a carrier tape according to an examined example.
[0040] FIG. **29** is a cross-sectional view showing a state of the carrier tape shown in FIG. **28** during transportation.

DETAILED DESCRIPTION

Description of Format, Basic Term and Usage in the Present Application

[0041] In this application, the description of embodiments is divided into multiple sections as necessary for convenience, but unless expressly stated otherwise, these are not independent and separate from each other, regardless of the order of description, and parts of a single example, where one part may be a detailed part of another or a part or all of a modified example. Also, in principle, descriptions of similar parts are omitted. Furthermore, each component in an embodiment is not essential, unless expressly stated otherwise, theoretically limited to that number, and obviously otherwise from the context.
[0042] Similarly, in the description of embodiments and the like, regarding materials, compositions, etc., saying "X consisting of A" does not exclude elements other than A, unless expressly stated otherwise and unless it is clear from the context that it is not the case. For example, regarding a component, it means "X including A as a main component" or the like. For instance, mentioning a "silicon member" does not limit it to pure silicon but includes members containing SiGe (Silicon Germanium) alloy and other multicomponent alloys with silicon as a main component, as well as other additives. Also, mentioning gold plating, Cu layer, nickel plating, etc., unless expressly stated otherwise, includes not only pure materials but also members containing gold, Cu, nickel, etc., as main components.
[0043] Furthermore, when specific values or quantities are mentioned, unless expressly stated otherwise, theoretically limited to that number, and obviously otherwise from the context, the values may exceed or be less than that specific number.
[0044] Also, in the figures of each embodiment, identical or similar parts are indicated by the same or similar symbols or reference numbers, and the description is not repeated in principle.
[0045] Moreover, in the attached drawings, hatching, etc., may be omitted in cross-sections when it would otherwise complicate the drawing or when the distinction from a void is clear. In this connection, even if the hole is closed in plan, the outline of the background may be omitted when it is obvious from the description or the like. Furthermore, even if not in cross-section, hatching or dot patterns may be applied to indicate that it is not a void or to indicate the boundary of a region.
[0046] The technology described in the following embodiments can be applied to a carrier tape in which a semiconductor device with a wiring substrate (a so-called substrate type semiconductor device) is accommodated. In this embodiment, as an example of the substrate type, a BGA typed semiconductor device is described, in which multiple solder balls are formed on multiple bump lands provided on the lower surface of the wiring substrate.

First Embodiment

Semiconductor Device

[0047] FIG. **1** is an upper surface view of a semiconductor device PKG of the first embodiment. FIG. **2** is a lower surface view of the semiconductor device PKG shown in FIG. **1**. FIG. **3** is a cross-sectional view along the line A-A shown in FIG. **1**.
[0048] As shown in FIG. **1**, the semiconductor device PKG according to the first embodiment includes: a wiring substrate **10** of a quadrangular shape having four sides **10***s***1**, **10***s***2**, **10***s***3**, **10***s***4** and four corners **10***c***1**, **10***c***2**, **10***c***3**, **10***c***4**, and a heat dissipation plate LID arranged to cover the upper surface of this wiring substrate **10**. Specifically, as shown in FIG. **1**, the wiring substrate **10** includes a side **10***s***1** extending in a first direction (referred to as "X1" direction in FIG. **1**), a side **10***s***2** facing the side **10***s***1** and extending in the first direction, a side **10***s***3** located between these two sides **10***s***1**, **10***s***2** and extending in a second direction (referred to as "Y1" direction in FIG. **1**) perpendicular to the first direction, and a side **10***s***4** facing the side **10***s***3** and extending in the second direction. Furthermore, as shown in FIG. **1**, the wiring substrate **10** includes a corner **10***c***1** where the side **10***s***1** and the side **10***s***3** intersect, a corner **10***c***2** where the side **10***s***2** and the side **10***s***4** intersect, a corner **10***c***3** where the side **10***s***4** and the side **10***s***1** intersect, and a corner **10***c***4** where the side **10***s***3** and the side **10***s***2** intersect. Although not

shown, the wiring substrate **10** corresponds to one of the multiple package areas provided on a single substrate. That is, the wiring substrate **10** is obtained by cutting this single substrate using a dicing blade (rotating cutting blade) or a punch (die). The heat dissipation plate LID is made of, for example, a metal member.

[0049] As shown in FIG. **2**, on the lower surface of the semiconductor device PKG according to the first embodiment, multiple external connection terminals **10***e* are provided. As shown in FIG. **2**, the multiple external connection terminals **10***e* are provided along each of the sides **10***s***1**, **10***s***2**, **10***s***3**, **10***s***4** of the wiring substrate **10** and across multiple rows. In the first embodiment, these external connection terminals **10***e* are solder balls. Specifically, multiple bump lands (not shown) are provided on the lower surface of the wiring substrate **10**, and each solder ball is formed on each bump land.

[0050] As shown in FIG. **3**, the wiring substrate **10** has an upper surface **10***t* and a lower surface **10***b* opposite to this upper surface **10***t*. Although not shown, multiple bonding fingers are provided on the upper surface **10***t* of the wiring substrate **10**. The multiple bonding fingers (terminals) are electrically connected to multiple bump lands (terminals) provided on the wiring substrate **10** via multiple wirings (not shown). More specifically, a solder resist film (not shown) is formed on the upper surface **10***t* of the wiring substrate **10**, and each bonding finger is exposed within an opening provided in this solder resist film. Similarly, a solder resist film is formed on the lower surface **10***b* of the wiring substrate **10**, and each bump land is exposed within an opening provided in this solder resist film. The wiring substrate **10** according to the first embodiment is, for example, a glass epoxy substrate made by impregnating glass fibers with resin.

[0051] Furthermore, as shown in FIG. **3**, a semiconductor chip **20** is mounted on the upper surface **10***t* of the wiring substrate **10**. In the first embodiment, the semiconductor chip **20** is mounted on the wiring substrate **10** via a plurality of bump electrodes BMP such that the main surface **20***t* of the semiconductor chip **20** faces the upper surface **10***t* of the wiring substrate **10**, as shown in FIG. **3**. That is, the semiconductor device PKG of the first embodiment is a so-called face down (flip chip) mounting type semiconductor device that electrically connects the semiconductor chip **20** to the wiring substrate **10** via a plurality of bump electrodes BMP. Although not shown, a plurality of electrode pads electrically connected to the semiconductor elements (for example, field-effect transistors) formed in the semiconductor chip **20** are provided on the main surface **20***t* of the semiconductor chip **20**, and in the first embodiment, each bump electrode BMP is pre-formed on each electrode pad.

[0052] Furthermore, in the first embodiment, as shown in FIG. **3**, a heat dissipation plate LID is arranged on the wiring substrate **10** so as to cover the semiconductor chip **20**. Also, as shown in FIG. **3**, a part (central portion) of the heat dissipation plate LID is fixed to the back surface **20***b* of the semiconductor chip **20** via a conductive adhesive material AM**1**. Moreover, as shown in FIG. **3**, another part (peripheral portion) of the heat dissipation plate LID is fixed to the wiring substrate **10** via an insulating adhesive material AM**2**. It should be noted that a conductive adhesive material may be used as the adhesive material AM**2**. And another part (peripheral portion) of the heat dissipation plate LID is located around the part (central portion) of the heat dissipation plate LID, as shown in FIG. **1**. Furthermore, the heat dissipation plate LID is bent so that another part (peripheral portion) of the heat dissipation plate LID is positioned closer to the wiring substrate **10** than a part (central portion) of the heat dissipation plate LID, as shown in FIG. **3**. This allows the thickness of the adhesive material AM**2** to be made almost the same as the thickness of the adhesive material AM**1**. And, if the adhesive material AM**2** is the same material as the adhesive material AM**1**, only one type of adhesive material needs to be prepared.

Carrier Tape

[0053] Next, the carrier tape **30** of the first embodiment will be described. FIG. **4** is an enlarged plan view at a portion of the carrier tape of the first embodiment. FIG. **5** is a cross-sectional view taken along the line B**1**-B**1** in FIG. **4**. FIG. **6** is a cross-sectional view taken along the line B**2**-B**2** in FIG. **4**. FIG. **7** is a cross-sectional view taken along the line B**3**-B**3** in FIG. **4**.

[0054] As shown in FIG. **4**, the carrier tape **30** of the first embodiment includes two peripheral portions **30***p***1**, **30***p***2** extending in a first direction (referred to as "X2" direction in FIG. **4**), and a central portion **30***c* extending in the first direction, located between these two peripheral portions **30***p***1**, **30***p***2** in a second direction perpendicular to the first direction (referred to as "Y2" direction in FIG. **4**). Furthermore, as shown in FIG. **4**, a plurality of through-holes (sprocket holes) **30***h* are provided in each peripheral portion **30***p***1**, **30***p***2** of the carrier tape **30**. These plurality of through-holes **30***h* are arranged in the first direction, as shown in FIG. **4**. In addition, a plurality of accommodating portions (storage portion, pocket portions) PKT**1** is provided in the central portion **30***c* of the carrier tape **30**. A through-hole **30***v* is provided in the center of each accommodating portion PKT**1**. Since each accommodating portion PKT**1** is formed by embossing the carrier tape **30** using, for example, a mold or air pressure, the carrier tape **30** of the first embodiment is also referred to as an embossed carrier tape (or blister tape). Moreover, in the present embodiment, the shapes of the plurality of accommodating portions PKT are the same as each other. Therefore, when explaining details about the accommodating portion PKT**1** in the present embodiment, one accommodating portion PKT**1** will be described.

[0055] Furthermore, the carrier tape **30** of the first embodiment is made from a resin material mixed with, for example, carbon. Specifically, the carrier tape **30** has a structure in which a layer made of conductive polystyrene or conductive polycarbonate is formed on both surfaces of a substrate (core layer) made of polystyrene resin, ABS resin, or polyethylene terephthalate resin. That is, the carrier tape **30** of the first embodiment has a certain degree of conductivity. This can suppress the charging of the carrier tape **30**. As a result, it is possible to suppress a decrease in the reliability of the semiconductor device PKG during the transportation of the carrier tape **30** with the semiconductor device PKG housed in the accommodating portion PKT**1**.

[0056] Next, the planar shape of the accommodating portion PKT**1** will be described using FIG. **4**. In the present embodiment 1, the accommodating portion PKT**1** includes four corner portions CP where a step portion STP**1** is formed, and four side portions SP each located between two corner portions CP that are adjacent to each other in either the first direction X2 or the second direction Y2 and where

the first protruding portion PLB**1** and the second protruding portion PLB**2** are formed. The planar shape of each step portion STP**1** is L-shaped. Furthermore, the tip portion of the first protruding portion PLB**1** protruding towards the inside of the accommodating portion PKT**1** from each side portion SP, and the tip portion of the second protruding portion PLB**2** protruding towards the inside from each side portion, are different from each other. Specifically, the width of the tip portion of the second protruding portion PLB**2** (i.e., the length along the adjacent side portion SP) is smaller than (less than) the width of the tip portion of the first protruding portion PLB**1** (i.e., the length along the adjacent side portion SP). That is, in plan view, the tip portion of the second protruding portion PLB**2** is more pointed than the tip portion of the first protruding portion PLB**1**. Moreover, the tip portion of the second protruding portion PLB**2** is located more towards the inside of the accommodating portion PKT**1** than the tip portion of the first protruding portion PLB**1**. That is, the protrusion amount of the second protruding portion PLB**2** from the side portion SP is larger than (greater than) the protrusion amount of the first protruding portion PLB**1** from the side portion SP. Here, the "protrusion amount" of each protruding portion refers to, for example, in the case of a protrusion extending from a side portion SP in the first direction X2 towards the inside of the accommodating portion PKT**1**, the length in the second direction Y2 from this side portion SP to the tip of the protruding portion. In the present embodiment 1, an example in which five of the first protruding portions PLB**1** and two of the second protruding portions PLB**2** are provided with each side portion SP is described, but the number of the first protruding portions PLB**1** is not limited to this. Furthermore, on each side portion SP, the five of the first protruding portions PLB**1** are provided between the two of the second protruding portions PLB**2**. In other words, the two of the second protruding portions PLB**2** are located at both end portions of each side portion SP so as to sandwich the first protruding portions PLB**1** therebetween.

[0057] Next, the cross-sectional shape of the accommodating portion PKT**1** will be described using FIGS. **5** to **7**. First, as shown in FIG. **5**, the step portion STP**1** is provided at each corner portion CP of the accommodating portion PKT**1** such that the upper surface STP**1***t* of this step portion STP**1** is positioned above the bottom surface PKT**1***b* of the accommodating portion PKT**1**, and the upper surface STP**1***t* of this step portion STP**1** is positioned below each upper surface **30***p***1***t*, **30***p***2***t* of the peripheral portions **30***p***1**, **30***p***2**. In the present embodiment 1, as shown in FIG. **5**, another step portion STP**2** is provided between the accommodating portion PKT**1** and the peripheral portions **30***p***1**, **30***p***2**. Furthermore, as shown in FIG. **5**, this other step portion STP**2** is provided between the two peripheral portions **30***p***1**, **30***p***2** such that the upper surface STP**2***t* of this other step portion STP**2** is positioned above the upper surface STP**1***t* of the step portion STP**1**, and the upper surface STP**2***t* of this other step portion STP**2** is positioned below each upper surface **30***p***1***t*, **30***p***2***t* of the peripheral portions **30***p***1**, **30***p***2**. Also, as shown in FIG. **5**, the upper surface STP**1***t* of the step portion STP**1**, the bottom surface PKT**1***b* of the accommodating portion PKT**1**, each upper surface **30***p***1***t*, **30***p***2***t* of the peripheral portions **30***p***1**, **30***p***2**, and the upper surface STP**2***t* of the other step portion STP**2** are substantially parallel to each other.

[0058] Furthermore, as described above, the cross-sectional view shown in FIG. **6** corresponds to the cross-sectional view along the line B**2**-B**2** shown in FIG. **4**. Therefore, although the aforementioned step portion STP**1** is not shown in FIG. **6**, the first protruding portion PLB**1** and the through-hole **30***v* can be confirmed. Also, the tip surface of the first protruding portion PLB**1** (the surface facing the side surface of the wiring substrate **10**) protrudes inward of the accommodating portion PKT**1** (towards the through-hole **30***v* side) more than the inner wall surface of the accommodating portion PKT**1** (the surface facing the side surface of the wiring substrate **10**) (refer to FIGS. **5** and **6** together). That is, as shown in FIGS. **5** and **6**, the distance DT**2** between the tip surfaces of the two of the first protruding portions PLB**1** facing each other in the second direction Y2 is smaller than the distance DT**1** between the inner wall surfaces of the two accommodating portions PKT**1** facing each other in the second direction Y2.

[0059] Furthermore, as described above, the cross-sectional view shown in FIG. **7** corresponds to the cross-sectional view along the line B**3**-B**3** shown in FIG. **4**. Therefore, although the aforementioned step portion STP**1** is not shown in FIG. **7**, the second protruding portion PLB**2** can be confirmed. Also, similar to the first protruding portion PLB**1**, the tip portion of the second protruding portion PLB**2** (portion facing side surface of wiring substrate **10**) protrudes inward of the accommodating portion PKT**1** more than the inner wall surface of the accommodating portion PKT**1** (refer to FIGS. **5** and **7** together). That is, as shown in FIGS. **5** and **7**, the distance DT**3** between the tip portions of the two of the second protruding portions PLB**2** facing each other in the second direction Y2 is smaller than the distance DT**1** between the inner wall surfaces of the two accommodating portions PKT**1** facing each other in the second direction Y2. Furthermore, the tip portion of the second protruding portion PLB**2** protrudes inward of the accommodating portions PKT**1** more than the tip surface of the first protruding portion PLB**1** (refer to FIGS. **6** and **7** together). That is, as shown in FIGS. **6** and **7**, the distance DT**3** between the tip portions of the two of the second protruding portions PLB**2** facing each other in the second direction Y2 is smaller than the distance DT**2** between the tip surfaces of the two of the first protruding portions PLB**1** facing each other in the second direction Y2.

Transportation Method of Semiconductor Device

[0060] Next, a method of transporting a semiconductor device of the first embodiment will be described. First, prepare the semiconductor device PKG described with reference to FIGS. **1** to **3**, and the carrier tape **30** described with reference to FIGS. **4** to **7**. It should be noted that the semiconductor device PKG prepared here is, for example, a product (shipment product) that has completed a series of assembly processes (subsequent processes) and has been determined to be a non-defective product by a testing process.

[0061] Next, as shown in FIGS. **8** to **11**, the semiconductor device PKG is placed (stored) in the accommodating portion (pocket portion) PKT**1** of the carrier tape **30**. Specifically, the semiconductor device PKG is placed inside the storage section PKT**1** so that the lower surface **10***b* of the wiring substrate **10** faces the bottom surface PKT**1***b* of the accommodating portion PKT**1**. At this time, the air inside the accommodating portion PKT**1** is suctioned through the

through-hole **30***v* formed in the bottom surface PKT**1***b* of the accommodating portion PKT**1**. This allows the semiconductor device PKG to be easily placed inside the accommodating portion PKT**1**. Furthermore, as shown in FIG. **8**, the semiconductor device PKG is placed inside the accommodating portion PKT**1** so that each corner **10***c***1**, **10***c***2**, **10***c***3**, **10***c***4** of the wiring substrate **10** is located at each corner portion CP of the accommodating portion PKT**1**. It should be noted that, as shown in FIG. **8**, at each corner portion CP of the accommodating portion PKT**1**, the wiring substrate **10** does not contact the carrier tape **30**.

[0062] The lower surface **10***b* of the peripheral portion of the wiring substrate **10** of the semiconductor device PKG placed in the accommodating portion PKT**1** is, at the position along the line C**1**-C**1** shown in FIG. **8**, in contact with the upper surface STP**1***t* of the step portion STP**1** of the carrier tape **30** (refer to FIG. **9**). It should be noted that the "peripheral portion" of the wiring substrate **10** mentioned here refers to the area located outside the outermost row of multiple external connection terminals **10***e* shown in FIG. **2**. Furthermore, as shown in FIG. **9**, the lower surface **10***b* of the wiring substrate **10** and the upper surface STP**1***t* of the step portion STP**1** are almost parallel to each other. Also, at the position along the line C**2**-C**2** shown in FIG. **8**, the wiring substrate **10** (namely, semiconductor device PKG) is spaced apart from the first protruding portions PLB**1** (refer to FIG. **10**). Similarly, the multiple external connection terminals **10***e* are also separated from the bottom surface PKT**1***b* of the accommodating portion PKT**1** (refer to FIG. **10**). That is, at the position along the line C**2**-C**2** shown in FIG. **8**, the semiconductor device PKG does not contact the carrier tape **30**. On the other hand, at the position along the line C**3**-C**3** shown in FIG. **8**, the wiring substrate **10** is in contact with the second protruding portion PLB**2** (refer to FIGS. **8** and **11**). That is, the distance between the second protruding portion PLB**2** and the wiring substrate **10** is smaller than the distance between the first protruding portion PLB**1** and the wiring substrate **10**. Here, as shown in FIGS. **10** and **11**, the semiconductor device PKG is placed inside the accommodating portion PKT**1** so that the surface (upper surface) of the heat dissipation plate LID is located above the upper surface STP**2***t* of another step portion STP**2**. Furthermore, in the first embodiment, although two of the second protruding portions PLB**2** are provided on each side portion SP of the accommodating portion PKT**1**, it is not necessary for all (in this case, a total of eight) of the second protrusions PLB**2** to be in contact with the wiring substrate **10** when the semiconductor device PKG is placed inside the accommodating portions PKT**1**.

[0063] Next, as shown in FIGS. **12** to **15**, a cover tape TP is attached to the carrier tape **30** so as to cover the semiconductor device PKG arranged (placed) in the accommodating portion PKT**1**. Specifically, as shown in FIG. **12**, the cover tape TP is attached to the carrier tape **30** along the central portion **30***c* extending in the first direction X2 between two peripheral portions **30***p***1**, **30***p***2**. At this time, at the position of the D**1**-D**1** line shown in FIG. **12**, the cover tape TP is spaced apart from the semiconductor device PKG (refer to FIG. **13**). On the other hand, at the positions of the D**2**-D**2** line and the D**3**-D**3** line shown in FIG. **12**, the cover tape TP is in contact with the surface (upper surface) of the heat dissipation plate LID (refer to FIGS. **14** and **15**). The cover tape TP used in the first embodiment is made of a stretchable material such as polyethylene resin or polyethylene terephthalate resin.

[0064] Here, the examined example of the carrier tape **100**, which was studied by the present inventors, will be described. FIG. **28** is a cross-sectional view showing the state in which the semiconductor device PKG is housed in the accommodating portions PKT**100** of the carrier tape **100** of the examined example. As shown in FIG. **28**, the inner wall surface of the accommodating portion PKT**100** of the carrier tape **100** of the examined example is inclined in two stages with respect to the bottom surface PKT**100***b* of the accommodating portion PKT**100**, and at least the step portion STP**1**, the first protruding portion PLB**1**, and the second protruding portion PLB**2** as in the first embodiment are not provided within the accommodating portion PKT**100**. Therefore, when the semiconductor device PKG is placed within the accommodating portion PKT**100**, as shown in FIG. **28**, the edges (namely, each side **10***s***1**, **10***s***2**, **10***s***3**, **10***s***4**) EGE of the lower surface **10***b* of the wiring substrate **10** are in contact with this inner wall surface (tapered surface). According to the study by the present inventors, in the case of the accommodating portion PKT**100**, because the structure does not support the lower surface **10***b* of the wiring substrate **10** on the upper surface STP**1***t* of the step portion STP**1** as in the first embodiment, it was found that the semiconductor device PKG is prone to tilting within the accommodating portion PKT**100** due to vibrations and impacts that occur during the transportation of the carrier tape **100** (refer to FIG. **29**). As a result, it was found that the inner wall surface of the accommodating portion PKT**100** is scraped off by the edges EGE of the wiring substrate **10**. A part of the scraped-off carrier tape **100** becomes foreign matter and scatters within the housing section, potentially adhering across several external connection terminals **10***e* of the semiconductor device PKG. Furthermore, if the carrier tape is conductive, a part of the carrier tape adhering across several external connection terminals **10***e* of the semiconductor device PKG may result in a defective product. As a countermeasure, the present inventors also considered using a carrier tape that does not have conductivity. However, even if an insulating carrier tape is used, if a part of the carrier tape becomes foreign matter and scatters within the housing section, it may adhere to the external connection terminals **10***e* of the semiconductor device PKG. And if foreign matter adheres to the external connection terminals **10***e*, even if the foreign matter is insulating, it may cause a mounting defect when, for example, mounting this semiconductor device PKG on a mounting substrate.

[0065] In contrast, in the case of the carrier tape **30** of the present embodiment 1, as shown in FIG. **9**, instead of the edge EGE of the wiring substrate **10**, the lower surface **10***b* of the wiring substrate **10** is supported by the step portions STP**1** wiring provided at each corner CP of the accommodating portion PKT**1**. Therefore, it is possible to suppress the movement of the semiconductor device PKG within the accommodating portion PKT**1** due to vibrations or shocks occurring during the transport of the carrier tape **30**, or due to the self-weight of the semiconductor device PKG.

[0066] Moreover, in the case of the carrier tape **30** of the first embodiment, as shown in FIGS. **9** and **10**, the wiring substrate **10** is supported by step portions STP**1** provided at each corner portion CP of the accommodating portion PKT**1** so that multiple external connection terminals **10***e* do not

contact the bottom surface PKT1*b* of the accommodating portion PKT1. Here, the planar shape of the step portion STP1 is an L-shape along two adjacent sides of the four sides of the wiring substrate, which is square, as shown in FIG. **4**. Therefore, when the semiconductor device PKG is placed within the accommodating portion PKT1, the lower surface **10***b* of the peripheral portion of the wiring substrate **10** contacts the step portion STP1, but the external connection terminals **10***e* do not contact this step portion STP1. As a result, it is possible to suppress the deformation of the external connection terminals **10***e* due to the self-weight of the semiconductor device PKG.

[0067] Moreover, in the case of the carrier tape **30** of the first embodiment, during the transport of the carrier tape **30**, the lower surface **10***b* of the wiring substrate **10** is supported by the step portion STP1, while the side surface of the wiring substrate **10** is supported by the second protruding portion PLB2 of the carrier tape. Specifically, during the transport of the carrier tape **30**, the tip portion of the first protruding portion PLB1, which is wider than the tip portion of the second protruding portion PLB2, does not contact the wiring substrate **10**. That is, in the case of the carrier tape **30** of the first embodiment, compared to the case using the examined example of the carrier tape **100**, the total area of the carrier tape contacting the semiconductor device PKG is smaller. Therefore, it is possible to reduce the amount of foreign matter (part of carrier tape that are shaved off) generated due to vibrations and shocks occurring during the transport of the carrier tape **30**, or due to the self-weight of the semiconductor device PKG.

[0068] Moreover, in the case of the carrier tape **30** of the first embodiment, two of the second protruding portions PLB2 are provided at both end portions of each side portion SP of the accommodating portion PKT1. Therefore, it is possible to suppress the rotation of the semiconductor device PKG within the accommodating portion PKT1 due to vibrations and shocks occurring during the transport of the carrier tape **30**, and the contact of the side surface of the wiring substrate **10** with the inner wall surface of the accommodating portion PKT1.

[0069] Furthermore, in the case of the carrier tape **30** of the first embodiment, as described above, at the stage of attaching the cover tape TP to the carrier tape **30**, the semiconductor device PKG is placed in the accommodating portion PKT1 so that the surface (upper surface) of the heat dissipation plate LID is positioned above the upper surface STP2*t* of another step portion STP2. Therefore, as shown in FIGS. **14** and **15**, when the cover tape TP is attached to the carrier tape **30**, the cover tape TP deforms by the amount the semiconductor device PKG protrudes outward from the accommodating portion PKT1. That is, a force pressing the semiconductor device PKG towards the bottom surface PKT1*b* of the accommodating portion PKT1 acts. This allows for more reliable suppression of the movement of the semiconductor device PKG within the accommodating portion PKT1 even if vibrations and shocks occur during the transport of the carrier tape **30**. As a result, it is possible to further reduce the amount of foreign matter generated.

[0070] Next, as shown in FIG. **16**, a carrier tape **30** with a cover tape TP attached thereto is wound onto a reel REL. It should be noted that the length of the carrier tape **30** that can be wound depends on the size of the reel REL used. Then, as shown in FIG. **17**, the reel REL with the wound carrier tape **30** is packaged in a moisture-proof bag BAG. It should be noted that after a label LAB, which includes the product name and model number, for example, is affixed to the surface of the moisture-proof bag BAG made of aluminum, the moisture-proof bag BAG with the reel REL packaged therein is transported (or shipped). At the destination, guide pins (not shown) are inserted into through-holes **30***h* provided at each peripheral portion **30***p***1**, **30***p***2** of the carrier tape **30** to feed the carrier tape **30** from the reel REL, and then semiconductor devices PKG are removed from each accommodating portion PKT1.

First Modified Example

[0071] Next, a modified example of the first embodiment will be explained using FIG. **18**. First, FIG. **18** corresponds to the position of the line C**3**-C**3** shown in FIG. **8** in the carrier tape **30** of the first embodiment, and the difference from FIG. **11** is in the shape of the second protruding portion PLB2. Specifically, as shown in FIG. **18**, the second protruding portion PLB2*m* of this first modified example has a first portion PLB2*ma* that connects to the bottom surface PKT1*b* of the accommodating portion PKT1 and a second portion PLB2*mb* that connects to this first portion PLB2*ma*, between the bottom surface PKT1*b* of the accommodating portion PKT1 and another step portion STP2. Also, as shown in FIG. **18**, the slope from the bottom surface PKT1*b* of the accommodating portion PKT1 to the inner wall surface of the second portion PLB2*mb* is greater than the slope from the bottom surface PKT1*b* of the accommodating portion PKT1 to the inner wall surface of the first portion PLB2*ma*. In other words, the inclination of the inner wall surface of the first portion PLB2*ma* relative to the bottom surface PKT1*b* of the accommodating portion PKT1 is smaller than the inclination of the inner wall surface of the second portion PLB2*mb* relative to the bottom surface PKT1*b* of the accommodating portion PKT1. Furthermore, as shown in FIG. **18**, the point where the first portion PLB2*ma* and the second portion PLB2*mb* intersect with each other (i.e., bending point of second protruding portions PLB2*m*) is positioned between the upper surface **10***t* and the lower surface **10***b* of the wiring board **10**, among the semiconductor devices PKG accommodated in the accommodating portion PKT1. That is, the second protruding portions PLB2 of the first embodiment had a cross-sectional shape that contacts a wide range of the side surface of the wiring board **10** in the thickness direction of this wiring board **10**. In contrast, because the second protruding portion PLB2*m* of this first modified example is inclined in two stages as shown in FIG. **18**, it is possible to reduce the area (length) in which this second protruding portion PLB2*m* contacts the side surface of the wiring board **10** in the thickness direction. As a result, it is possible to further reduce the amount of foreign matter generated.

Second Embodiment

[0072] Next, the second embodiment will be explained. It should be noted that the difference between this second embodiment and the first embodiment mentioned above lies in the shape (structure) of the storage section of the carrier tape, and other parts are the same as those explained in the first embodiment. Therefore, in this second embodiment, mainly the differences from the first embodiment will be explained.

Carrier Tape

[0073] FIG. **19** is an enlarged plan view at a portion of the carrier tape of the second embodiment. FIG. **20** is a cross-sectional view along the line E**1**-E**1** shown in FIG. **19**. FIG. **21** is a cross-sectional view along the line E**2**-E**2** shown in FIG. **19**. It should be noted that the position of the line E**1**-E**1** shown in FIG. **19** corresponds to the position of the line B**1**-B**1** shown in FIG. **4**. Also, the position of the line E**2**-E**2** shown in FIG. **19** corresponds to the position of the line B**2**-B**2** shown in FIG. **4**.

[0074] As shown in FIG. **19**, the accommodating portion PKT**2** of the second embodiment includes four corner portions CP each having a notch portion CTP formed therein, and four side portions SP each located between two corner portions CP adjacent to each other in either a first direction X2 or a second direction Y2. Furthermore, the planar shape of the two sides CTPS of each notch portion CTP draws an arc so as to curve from the adjacent side portions SP to the tip (apex) TIP of the notch portion CTP without having a bending point therebetween. That is, the accommodating portion PKT**2** does not have the bending point between the side portion SP (more specifically, boundary between each side portion SP and corner portion CP) and the tip TIP of the notch portion CTP provided in the corner portion CP adjacent to that side portion SP. Moreover, the side portions SP do not have the protruding portions PLB**1**, PLB**2** as described in the first embodiment. That is, the planar shape of each side portion SP is a straight line extending in the first direction X2 or the second direction Y2.

[0075] Next, the cross-sectional shape of the accommodating portion PKT**2** will be described using FIGS. **20** and **21**. First, as shown in FIG. **20**, since the carrier tape **40** of the second embodiment does not have the step portions STP**1**, STP**2** as in the first embodiment, the cross-sectional shape along the line E**1**-E**1** shown in FIG. **19** is almost the same as the cross-sectional shape along the line E**2**-E**2** shown in FIG. **19**. However, as mentioned above, each corner portion CP of the accommodating portion PKT**2** of the second embodiment is provided with a notch portion CTP. Therefore, as shown in FIGS. **20** and **21**, the distance DT**22** between two side portions SP facing each other in the second direction Y2 is smaller than the distance DT**11** between the inner wall surfaces of two notch portions CTP facing each other in the second direction Y2. Moreover, this distance DT**11** increases towards the tip (apex) TIP of the notch portion CTP.

Transporting Method of Semiconductor Device

[0076] Next, a method of transporting a semiconductor device of the second embodiment will be described. First, a semiconductor device PKG as described using FIGS. **1** to **3**, and a carrier tape **40** as described using FIGS. **19** to **21**, are prepared.

[0077] Next, as shown in FIGS. **22** to **24**, a semiconductor device PKG is placed (stored) in the accommodating portion (storage portion, pocket portion) PKT**2** of the carrier tape **40**. Specifically, the semiconductor device PKG is placed within the accommodating portion PKT**2** so that the lower surface **10***b* of the wiring substrate **10** faces the bottom surface PKT**2***b* of the accommodating portion PKT**2**. Moreover, as shown in FIG. **22**, the semiconductor device PKG is placed in the accommodating portion PKT**2** such that each corner **10***c***1**, **10***c***2**, **10***c***3**, **10***c***4** of the wiring substrate **10** is located at each corner portion CP of the accommodating portion PKT**2**. At this time, since each corner **10***c***1**, **10***c***2**, **10***c***3**, **10***c***4** of the wiring substrate **10** is located within each notch portion CTP, as shown in FIG. **22**, the wiring substrate **10** does not contact the carrier tape **40** at each corner portion CP of the accommodating portion PKT**2**, similar to the first embodiment.

[0078] The semiconductor device PKG (namely, peripheral portion of wiring substrate **10**) placed in the accommodating portion PKT**2** and including the wiring substrate **10** and the heat dissipation plate LID is not in contact with the carrier tape **40** at the position along the line F**1**-F**1** (refer to FIG. **23**). On the other hand, at the position on the line F**2**-F**2** shown in FIG. **22**, the wiring substrate **10** is in contact with the inner wall surface of the accommodating portion PKT**2** of the carrier tape **40** (see FIG. **24**). Specifically, as shown in FIG. **22**, the wiring substrate **10** is in contact with the carrier tape **40** (that is, the inner wall surface of the accommodating portion PKT**2**) over the entire region of each side portion SP of the accommodating portion PKT**2**. This is because, in the second embodiment, each side portion SP adjacent to each side **10***s***1**, **10***s***2**, **10***s***3**, **10***s***4** of the wiring substrate **10** does not have the protrusions PLB**1**, PLB**2** as in the first embodiment. Therefore, in plain view, the width (length) of the portion of the carrier tape that is in contact with the wiring substrate **10** is greater than the width (length) of the tips of the protrusions PLB**1**, PLB**2** that are in contact with the wiring substrate **10**. As a result, compared to the carrier tape **30** of the first embodiment, the area of contact between the carrier tape **40** and the semiconductor device PKG increases, while the impact per unit area generated by the contact between the carrier tape **40** and the semiconductor device PKG decreases. This allows for a reduction in the amount of foreign matter (parts of the carrier tape that are shaved off) generated by vibrations and impacts during the transport of the carrier tape **40** or by the weight of the semiconductor device PKG.

[0079] Furthermore, as mentioned above, the corner portions CP of the accommodating portion PKT**2** in the second embodiment are not provided with the step portion STP**1** as in the first embodiment (refer to FIG. **19**). This is because, as shown in FIG. **19**, each notch portion CTP is provided such that the distance between the two sides CTPS forming the notch portion CTP gradually decreases towards the tip (apex) TIP of the notch portion CTP. That is, the processing of each corner portion CP in the second embodiment is more difficult compared to the first embodiment. Therefore, as shown in FIG. **24**, the external connection terminals **10***e* of the semiconductor device PKG placed inside the accommodating portion PKT**2** are in contact with the bottom surface PKT**2***b* of the accommodating portion PKT**2**.

[0080] Next, as shown in FIGS. **25** to **27**, a cover tape TP is attached to the carrier tape **40** so as to cover the semiconductor device PKG arranged (placed) in the accommodating portion PKT**2**. Specifically, as shown in FIG. **25**, the cover tape TP is attached to the carrier tape **40** along the central portion **40***c* extending in the first direction X2 between two peripheral portions **40***p***1**, **40***p***2**. At this time, at the position on the line G**1**-G**1** shown in FIG. **25**, the cover tape TP is spaced apart from the semiconductor device PKG (refer to FIG. **26**). Also, at the position on the line G**2**-G**2** shown in FIG. **25**, the cover tape TP is spaced apart from the semiconductor device PKG (refer to FIG. **27**). This is

because the accommodating portion PKT**2** of the second embodiment does not have the step portion STP**2** described in the first embodiment.

[0081] As described above, the invention made by the present inventor has been specifically described based on the embodiment, but the present invention is not limited to the above embodiment, and it is needless to say that various modifications can be made without departing from the gist thereof.

[0082] For example, in the embodiments described above, as an example of the semiconductor device PKG, a semiconductor device of the so-called face-down (flip-chip) mounting type, which electrically connects the semiconductor chip **20** to the wiring substrate **10** via multiple bump electrodes BMP, has been described, but it may also be a semiconductor device of the so-called face-up mounting type using multiple bonding wires. That is, it may be a semiconductor device PKG that does not have a heat dissipation plate LID. On the other hand, in the case of the semiconductor device PKG of the embodiments described above, since it also includes a heat dissipation plate LID, the weight of the semiconductor device **10** is greater than the weight of the semiconductor device of the face-up mounting type. Therefore, the aforementioned foreign objects are also significant when transporting the semiconductor device PKG of the present embodiment.

[0083] Moreover, for example, in the embodiments described above, as shown in FIG. **3**, an example where the heat dissipation plate LID is bent so that another part (peripheral portion) of the heat dissipation plate LID is located closer to the wiring substrate **10** than a part (central portion) of the heat dissipation plate LID has been described, but a heat dissipation plate without bending processing may be used. However, when using a heat dissipation plate without bending processing, it is necessary to increase the thickness of the adhesive material AM**2**.

[0084] Furthermore, for example, in the embodiments described above, it has been described that the carrier tape has a certain degree of conductivity, but an insulating carrier tape may be used. However, even if an insulating carrier tape is used, if a part of the carrier tape becomes a foreign object and scatters inside the housing section, it may adhere to the external connection terminals **10***e* of the semiconductor device PKG. And if foreign objects adhere to the external connection terminals **10***e*, even if the foreign objects are insulating, there is a risk of causing mounting defects when, for example, mounting this semiconductor device PKG on a mounting substrate. On the other hand, with the structure of the accommodating portions PKT**1**, PKT**2** of the embodiments described above, since it is possible to suppress the scattering of a part of the carrier tape as foreign objects, the accommodating portions PKT**1**, PKT**2** of the embodiments described above are effective even for insulating carrier tapes.

[0085] Furthermore, for example, in the first embodiment, it was explained that another step portion STP**2** is provided between the accommodating portion PKT**1** and each peripheral portion **30***p***1**, **30***p***2**, but this another step portion STP**2** may not be provided. However, in order to prevent the semiconductor device from moving as much as possible during the transportation of the carrier tape **30**, it is preferable to provide this another step portion STP**2** as in the first embodiment. Similarly, in the second embodiment, it was explained that another step portion STP**2** is not provided between the accommodating portion PKT**2** and each peripheral portion **40***p***1**, **40***p***2**, but from the viewpoint of preventing the semiconductor device PKG from moving as much as possible during the transportation of the carrier tape **40**, it is preferable to provide another step portion STP**2** in the carrier tape **40** of the second embodiment, similar to the first embodiment. By doing so, it is possible to press the semiconductor device PKG, which is placed in the accommodating portion PKT**2** of the carrier tape **40**, towards the bottom surface PKT**2***b* of the accommodating portion PKT**2**, and more reliably prevent the semiconductor device PKG from moving within the accommodating portion PKT**2** during the transportation of the carrier tape **40**. However, from the viewpoint of suppressing deformation of the external connection terminal **10***e* as much as possible, in the carrier tape **40** of the second embodiment, which does not have a step portion STP**1** like the first embodiment, it is preferable not to provide another step portion STP**2**.

[0086] Furthermore, for example, in the second embodiment, it was explained that the step portion STP**1** described in the first embodiment is not provided at each corner portion CP of the accommodating portion PKT**2**, but this explanation does not exclude providing a step portion STP**1** at each corner portion CP of the accommodating portion PKT**2**.

What is claimed is:

1. A method of transporting a semiconductor device, comprising:

(a) preparing the semiconductor device including: a wiring substrate having an upper surface and a lower surface opposite the upper surface, a semiconductor chip mounted on the upper surface of the wiring substrate, and a plurality of external connection terminals provided on the lower surface of the wiring substrate;

(b) preparing a carrier tape having: a first peripheral portion and a second peripheral portion both extending in a first direction, and a plurality of pocket portions that is located between the first peripheral potion and the second peripheral portion in a second direction perpendicular to said first direction, and that is arranged in said first direction;

(c) after the (a) and the (b), placing the semiconductor device in a first pocket portion of the plurality of pocket portions such that the lower surface of the wiring substrate faces a bottom surface of the first pocket portion;

(d) after the (c), attaching a cover tape to the carrier tape so as to cover the semiconductor device placed in the first pocket portion; and

(e) after the (d), transporting the carrier tape containing the semiconductor device,

wherein a planar shape of the wiring substrate is quadrangular,

wherein, in plan view, the first pocket portion includes:

four corner portions where a first step portion is formed; and

four side portions each located between two of the four corner portions, and where a first protruding portion and a second protruding portion are formed, the two being adjacent to each other in either the first direction or the second direction,

wherein, in cross-sectional view, the first step portion has an upper surface positioned above the bottom surface

of the first pocket portion, and positioned below an upper surface of each of the first peripheral portion and the second peripheral portion,

wherein, in plan view, a tip portion of the first protruding portion protruding towards an inside of the first pocket portion from a first side portion of the four side portions and a tip portion of the second protruding portion protruding towards the inside of the second pocket portion from the first side portion are different from each other,

wherein, in plan view, a width of the tip portion of the second protruding portion is smaller than a width of the tip portion of the first protruding portion,

wherein, in plan view, a protrusion amount of the second protruding portion from the first side portion is larger than a protrusion amount of the first protruding portion from the first side portion, and

wherein the semiconductor device placed in the first pocket portion in the (c) is spaced apart from the first protruding portion, and the lower surface of the wiring substrate is in contact with the upper surface of the first step portion.

2. The method according to claim **1**,

wherein the semiconductor chip has a main surface, a plurality of electrode pads formed on the main surface, and a back surface opposite the main surface,

wherein the semiconductor chip is mounted on the wiring substrate via a plurality of bump electrodes such that the main surface of the semiconductor chip faces the upper surface of the wiring substrate, and

wherein a heat dissipation plate made of a metal member is fixed onto the back surface of the semiconductor chip.

3. The method according to claim **1**,

wherein the wiring substrate is a glass epoxy substrate, and

wherein the carrier tape is made of a resin material mixed with carbon.

4. The method according to claim **1**, wherein each of the first peripheral portion and the second peripheral portion has a plurality of through-holes arranged in the first direction

5. The method according to claim **1**,

wherein the carrier tape prepared in the (b) further includes a second step portion provided, in the second direction, between the first pocket portion in which the first step portion is formed and the first and second peripheral portions,

wherein, in cross-sectional view, the second step portion has an upper surface that is positioned above the upper surface of the first step portion, and that is positioned below the upper surfaces of the first and second peripheral portions, and

wherein in the (d), the cover tape is attached to the upper surface of the second step portion.

6. The method according to claim **1**, wherein a planar shape of the first step portion is an L-shape along two sides of four sides of the wiring substrate, the two sides being adjacent to each other.

7. The method according to claim **1**, wherein, in plain view, the second protruding portion is located at both end portions of the first side portion so as to sandwich the first protruding portion therebetween.

8. The method according to claim **1**,

wherein, in cross-sectional view, the second protruding portion has: a first portion that connects to the bottom surface of the first pocket portion; and a second portion that connects to the first portion,

wherein an inclination of the second portion relative to the bottom surface of the first pocket portion is smaller than an inclination of the first portion relative to the bottom surface of the first pocket portion, and

wherein after the (c), a bending point of the second protruding portion where the first portion and the second portion intersect with each other is positioned between the upper surface of the wiring substrate and the lower surface of the wiring substrate.

9. The method according to claim **1**, wherein, in the (e), the carrier tape containing the semiconductor device is transported in such a state that the carrier tape is wound on a reel.

10. A carrier tape comprising:

a first peripheral portion extending in a first direction;

a second peripheral portion extending first direction; and

a plurality of pocket portions located between the first peripheral portion and the second peripheral portion in a second direction perpendicular to the first direction, and arranged in the first direction,

wherein, in plan view, each of the plurality of pocket portions includes:

four corner portions where a first step portion is formed; and

four side portions each located between two of the four corner portions, and where a first protruding portion and a second protruding portion are formed, the two being adjacent to each other in either the first direction or the second direction,

wherein, in cross-sectional view, the first step portion has an upper surface positioned above the bottom surface of each of the plurality of pocket portions, and positioned below an upper surface of each of the first peripheral portion and the second peripheral portion,

wherein, in each of the plurality of pocket portions, a tip portion of the first protruding portion protruding towards an inside of the first pocket portion from a first side portion of the four side portions and a tip portion of the second protruding portion protruding towards the inside of the second pocket portion from the first side portion are different from each other,

wherein, in plan view, a width of the tip portion of the second protruding portion is smaller than a width of the tip portion of the first protruding portion, and

wherein, in plan view, a protrusion amount of the second protruding portion from the first side portion is larger than a protrusion amount of the first protruding portion from the first side portion.

11. The carrier tape according to claim **10** is made of a resin material mixed with carbon.

12. The carrier tape according to claim **10**, wherein each of the first peripheral portion and the second peripheral portion has a plurality of through-holes arranged in the first direction.

13. The carrier tape according to claim **10**, further comprising:

a second step portion provided, in the second direction, between the plurality of pocket portions in which the first step portion is formed and the first and second peripheral portions,

wherein, in cross-sectional view, the second step portion has an upper surface that is positioned above the upper surface of the first step portion, and that is positioned below the upper surfaces of the first and second peripheral portions,

14. The carrier tape according to claim **10**, wherein a planar shape of the first step portion is an L-shape.

15. The carrier tape according to claim **10**, wherein, in plain view, the second protruding portion is located at both end portions of the first side portion so as to sandwich the first protruding portion therebetween.

16. The carrier tape according to claim **10**,

wherein, in cross-sectional view, the second protruding portion has: a first portion that connects to the bottom surface of each of the plurality of pocket portions; and a second portion that connects to the first portion, and

wherein an inclination of the second portion relative to the bottom surface of each of the plurality of pocket portions is smaller than an inclination of the first portion relative to the bottom surface of each of the plurality of pocket portions.

17. A method of transporting a semiconductor device, comprising:

(a) preparing the semiconductor device including: a wiring substrate having an upper surface and a lower surface opposite the upper surface, a semiconductor chip mounted on the upper surface of the wiring substrate, and a plurality of external connection terminals provided on the lower surface of the wiring substrate;

(b) preparing a carrier tape having: a first peripheral portion and a second peripheral portion both extending in a first direction, and a plurality of pocket portions that is located between the first peripheral potion and the second peripheral portion in a second direction perpendicular to said first direction, and that is arranged in said first direction;

(c) after the (a) and the (b), placing the semiconductor device in a first pocket portion of the plurality of pocket portions such that the lower surface of the wiring substrate faces a bottom surface of the first pocket portion;

(d) after the (c), attaching a cover tape to the carrier tape so as to cover the semiconductor device placed in the first pocket portion; and

(e) after the (d), transporting the carrier tape containing the semiconductor device,

wherein a planar shape of the wiring substrate is quadrangular having a corner,

wherein, in plan view, the first pocket portion includes:

four corner portions each having a notch portion; and

four side portions each located between two of the four corner portions, the two being adjacent to each other in either the first direction or the second direction,

wherein a planar shape of two sides of the notch portion draws an arc so as to curve from each of a first side portion and a second side portion, which are adjacent to the notch portion, towards an apex of the notch portion,

wherein the notch portion is provided such that a distance between the two sides of the notch portion gradually decreases towards the apex of the notch portion, and

wherein the semiconductor device placed in the first pocket portion in the (c) is in contact with the four side portions, and the corner of the wiring substrate is located within the notch portion.

18. The method according to claim **17**,

wherein the semiconductor chip has a main surface, a plurality of electrode pads formed on the main surface, and a back surface opposite the main surface,

wherein the semiconductor chip is mounted on the wiring substrate via a plurality of bump electrodes such that the main surface of the semiconductor chip faces the upper surface of the wiring substrate, and

wherein a heat dissipation plate made of a metal member is fixed onto the back surface of the semiconductor chip.

19. The method according to claim **17**,

wherein the wiring substrate is a glass epoxy substrate, and

wherein the carrier tape is made of a resin material mixed with carbon.

20. The method according to claim **17**, wherein the planar shape of the two sides of the notch portion draws the arc so as to curve from each of the first side portion and the second side portion to the apex of the notch portion without having a bending point therebetween.

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