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INTEGRATED CIRCUIT DEVICE AND METHOD

Abstract

An integrated circuit (IC) device includes a first conductive line on a front side of a semiconductor wafer, a first power rail on a back side of the semiconductor wafer, a first gate structure extending in a first direction on the front side of the semiconductor wafer, first and second active regions adjacent to the first gate structure, a first via between and electrically connected to the first active region and the first conductive line, and a second via between and electrically connected to the first power rail and either the first active region or the second active region. A plane perpendicular to the first direction intersects each of the first conductive line, the first power rail, the first gate structure, and the first and second active regions.

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Background/Summary

PRIORITY CLAIM [0001] The present application is a continuation of U.S. application Ser. No. 18/522,980, filed Nov. 29, 2023, now U.S. Pat. No. 12,272,649, issued Apr. 8, 2025, which is a continuation of U.S. application Ser. No. 17/225,578, filed Apr. 8, 2021, now U.S. Pat. No. 11,842,963, issued Dec. 12, 2023, which claims the priority of U.S. Provisional Application No. 63/024,926, filed May 14, 2020, each of which is incorporated herein by reference in its entirety.

BACKGROUND
[0002] Integrated circuits have been widely used for various kinds of applications. The demand for faster processing speed, lower power consumption, and smaller size is increasing. Various cells including digital cells and analog cells are designed for manufacturing the integrated circuits. For the analog cells, the resistance of metal routing coupled between active devices in the integrated circuits and the power rail is significant due to small geometry size.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0003] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.
[0004] FIG. **1**A is a layout diagram in a plan view of a semiconductor device, in accordance with various embodiments.
[0005] FIG. **1**B is a cross-sectional view of part of the semiconductor device in FIG. **1**A along a line AA′, in accordance with various embodiments.
[0006] FIG. **1**C is an equivalent circuit corresponding to part of the semiconductor device of FIGS. **1**A-**1**B, in accordance with various embodiments.
[0007] FIG. **2**A is a layout diagram in a plan view of a semiconductor device, in accordance with various embodiments.
[0008] FIG. **2**B is a cross-sectional view of part of the semiconductor device in FIG. **2**A along a line BB′, in accordance with various embodiments.
[0009] FIG. **2**C is an equivalent circuit corresponding to part of the semiconductor device of FIGS. **2**A-**2**B, in accordance with various embodiments.
[0010] FIG. **3**A is a layout diagram in a plan view of a semiconductor device, in accordance with various embodiments.
[0011] FIG. **3**B is a cross-sectional view of part of the semiconductor device in FIG. **3**A along a line CC′, in accordance with various embodiments.
[0012] FIG. **3**C is an equivalent circuit corresponding to part of the semiconductor device of FIGS. **3**A-**3**B, in accordance with various embodiments.
[0013] FIG. **4** is a schematic diagram of an integrated circuit, in accordance with various

embodiments.
[0014] FIG. **5**A is a layout diagram in a plan view of a semiconductor device, in accordance with various embodiments.
[0015] FIG. **5**B is a cross-sectional view of part of the semiconductor device in FIG. **5**A along a line DD′, in accordance with various embodiments.
[0016] FIG. **6**A is a layout diagram in a plan view of a semiconductor device, in accordance with various embodiments.
[0017] FIG. **6**B is a cross-sectional view of part of the semiconductor device in FIG. **6**A along a line EE′, in accordance with various embodiments.
[0018] FIG. **6**C is an equivalent circuit corresponding to part of the semiconductor device of FIGS. **6**A-**6**B, in accordance with various embodiments.
[0019] FIG. **7**A is a layout diagram in a plan view of a semiconductor device, in accordance with various embodiments.
[0020] FIG. **7**B is a cross-sectional view of part of the semiconductor device in FIG. **7**A along a line FF′, in accordance with various embodiments.
[0021] FIG. **7**C is an equivalent circuit corresponding to part of the semiconductor device of FIGS. **7**A-**7**B, in accordance with various embodiments.
[0022] FIG. **8**A is another equivalent circuit corresponding to part of the semiconductor device of FIGS. **6**A-**6**B, in accordance with various embodiments.
[0023] FIG. **8**B is another equivalent circuit corresponding to part of the semiconductor device of FIGS. **7**A-**7**B, in accordance with various embodiments.
[0024] FIG. **9**A is a layout diagram in a plan view of a semiconductor device, in accordance with various embodiments.
[0025] FIG. **9**B is an equivalent circuit corresponding to part of the semiconductor device of FIG. **9**A, in accordance with various embodiments.
[0026] FIG. **10**A is a layout diagram in a plan view of a semiconductor device, in accordance with various embodiments.
[0027] FIG. **10**B is an equivalent circuit corresponding to part of the semiconductor device of FIG. **10**A, in accordance with various embodiments.
[0028] FIG. **11** is a layout diagram in a plan view of a semiconductor device, in accordance with various embodiments.
[0029] FIG. **12**A is a layout diagram in a plan view of a semiconductor device, in accordance with various embodiments.
[0030] FIG. **12**B is an equivalent circuit corresponding to part of the semiconductor device of FIG. **12**A, in accordance with various embodiments.
[0031] FIG. **13**A is a flow chart of a method of forming an integrated circuit, in accordance with some embodiments of the present disclosure.
[0032] FIG. **13**B is a flow chart of a method of fabricating a semiconductor device, in accordance with some embodiments of the present disclosure.
[0033] FIG. **14** is a block diagram of a system for designing the integrated circuit layout design, in accordance with some embodiments of the present disclosure.
[0034] FIG. **15** is a block diagram of an integrated circuit manufacturing system, and an integrated circuit manufacturing flow associated therewith, in accordance with some embodiments.

DETAILED DESCRIPTION

[0035] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0036] The terms used in this specification generally have their ordinary meanings in the art and in the specific context where each term is used. The use of examples in this specification, including examples of any terms discussed herein, is illustrative only, and in no way limits the scope and meaning of the disclosure or of any exemplified term. Likewise, the present disclosure is not limited to various embodiments given in this specification.

[0037] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper” and the like, may be used herein for case of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly. As used herein, the term “and/or” includes any and all combinations of one or more of the associated listed items.

[0038] As used herein, “around”, “about”, “approximately” or “substantially” shall generally refer to any approximate value of a given value or range, in which it is varied depending on various arts in which it pertains, and the scope of which should be accorded with the broadest interpretation understood by the person skilled in the art to which it pertains, so as to encompass all such modifications and similar structures. In some embodiments, it shall generally mean within 20 percent, preferably within 10 percent, and more preferably within 5 percent of a given value or range. Numerical quantities given herein are approximate, meaning that the term “around”, “about”, “approximately” or “substantially” can be inferred if not expressly stated, or meaning other approximate values.

[0039] In some layout designs of analog circuits, pick-up regions are positioned in a cell to conductively connect a particular dopant type well in the cell to a voltage source. More specifically, in various embodiments, an n-type pick-up region is used to conductively connect an n-type well in the cell to the first supply voltage VDD, and/or a p-type pick-up region is used to conductively connect a p-type well in the cell to the second supply voltage VSS. Embodiments described below provide analog cells including transistor structures to couple front-side metal layers to back-side power rails in order to reduce the cell area and parasitic resistance and capacitance that are contributed by the metal routing. In some embodiments, at least one of the transistor structure, constructed with vias coupling doped regions of the transistor to both of metal layers in front and back side, is referred to as a via pillar to connect back-side power components, such as bumps, super high-density metal-insulator-metal (SHD-MIM), and inductors to front-side components, such as metal-oxide-metal (MOM) capacitor, gates of MOSFET, and high-resistance elements. It significantly cuts the parasitic resistance of metal routing between the front-side and back-side metal layers. Moreover, tied-off grounded gates of the aforementioned transistor structure includes de-capacitor for area saving; whereas as the gates of the transistor structure are floating to obtain lowest parasitic capacitance for high operation speed. In another embodiment, differential pair switches of a current mirror circuit include another transistor structure having a first doped region coupled to the front side metal and a second doped region coupled to the back side power rail, while the other transistor structure functions as a current mirror switch in the current mirror circuit. In still another embodiment, standard cells, such as a cell including an inverter, consist of a combination of the analog cells which overlap at least two and half front-side metal tracks and different numbers of, for example, P-type MOS or N-type MOS. With the configurations of the present disclosure, operation speed of analog surges and the cell area shrinks, comparing to some approaches of back side power rail configuration.

[0040] FIGS. **1**A-**3**C depict semiconductor devices **100-300**, each of which is a component of one or more of IC **400** or semiconductor devices **500**, **600**, **700**, **900**, **1000**, **1100**, or **1200** discussed below with respect to FIGS. **4-12**B.

[0041] Reference is now made to FIG. **1**A. FIG. **1**A is a layout diagram in a plan view of the semiconductor device **100**, in accordance with various embodiments. In some embodiments, the semiconductor device **100** is implemented in, for example, an analog circuit that includes at least one output signal having an analog value that is a continuous function of an analog value of an input signal of the analog circuit. As illustratively shown in FIG. **1**A, the semiconductor device **100** includes a power rail (i.e., Back-side metal zero layer, BM**0**) **111**, active regions (i.e., oxide-diffusion, OD) **121-122**, gate structures **131-133**, conductive line (i.e., metal zero layer, MO) **141-143**, and vias VB**1**, VD**1**, and VG**1**. In some embodiments, the power rail **111** is arranged in a first layer. The active regions **121-122** and the gate structures **131-133** are arranged in a second layer above the first layer. The conductive lines **141-143** are arranged in a third layer above the second layer. The via VB**1** is arranged between the first layer and the second layer. The vias VD**1** and VG**1** are arranged between the second layer and the third layer.

[0042] For illustration, the power rail **111** extends in x direction. The gate structures **131-133** extend in y direction and cross the power rail **111** in a layout view. The gate structures **131-133** are separated from each other in x direction. The gate structure **132** is interposed between the active regions **121-122**. The conductive lines **141-143** extend in x direction and are separated from each other in y direction. In the layout view, at least one of the conductive lines **141-143** overlaps the power rail **111**. In other words, the power rail **111** and the conductive line **141** are on the opposite sides of the active regions **121-122**, and the gate structure **132**.

[0043] In some embodiments, as shown in FIG. **1**A, a width of the via VB**1** along y direction is substantially the same with a width of the active region **122**. In various embodiments, the width of the via VB**1** along y direction is between the width of the active region **122** and a width of the power rail **111**. In various embodiments, the via VB**1** has a tapered shape.

[0044] In some embodiments, the power rail **111**, the active regions **121-122**, the gate structures **131-133**, the vias VD**1** and VB**1**, the conductive lines **141-142**, and half of the conductive line **143** are included in an analog cell CELL**1**. In some embodiments, the conductive lines **141-143** are arranged in three metal tracks in the semiconductor device **100**. The configurations of the analog cell CELL**1** are given for illustrative purposes. Various implementations are within the contemplated scope of the present disclosure. For example, in some embodiments, the analog cell CELL**1** includes conductive line(s) arranged in 1, 1.5, 2, 2.5, 3 . . . or 100 metal tracks.

[0045] In some embodiments, the power rail **111** includes copper (Cu), aluminum (Al), ruthenium (Ru), cobalt (Co), molybdenum (Mo), nickel (Ni), tungsten (W), or the like. In various embodiments, the power rail **111** acts as a power rail (e.g., VDD or VSS) at the backside of the semiconductor device **100**, and thus the power rail **111** is interchangeably referred to as a backside power line or a backside power rail.

[0046] In some embodiments, the conductive lines **141-143** include copper (Cu), aluminum (Al), ruthenium (Ru), cobalt (Co), molybdenum (Mo), nickel (Ni), tungsten (W), or the like.

[0047] In some embodiments, the conductive lines **141-143** are included in a first conductive layer of a plurality of conductive layers. In some embodiments, the plurality of conductive layers includes one or more layers in which a material, referred to as a Hi R material in some embodiments, has a resistivity greater than or equal to about 5 micro-ohm-centimeters. In some embodiments, a Hi R material is included in a metal plate as part of a capacitive device. In some embodiments, one or more conductive layers of the plurality of conductive layers include W, TIN, TaN, Co, Mo, Mn, Ru, Ta, TiW, Ta—Si—N, TiZrN, CoTix, AlC, TiGeN, Cr, CrAsC, TiAlC, WNx, or another suitable material.

[0048] In some embodiments, the vias VD**1**, via VB**1**, and VG**1** include a conductive material, such as tungsten (W). Other conductive materials may be used for the vias VD**1**, via VB**1**, and VG**1**, such as copper (Cu), aluminum (Al), ruthenium (Ru), cobalt (Co), molybdenum (Mo), nickel (Ni), or the like.

[0049] In some embodiments, the active regions **121-122** include n-type dopants, including, such as phosphorus, arsenic, or a combination thereof or p-type dopants including, such as boron, indium, aluminum, gallium, or a combination thereof.

[0050] In some embodiments, the gate structures **131-133** includes channel regions **132***a*, spacer layers **132***b*, metal gate layers **132***c*, and inner spacer material layers **132***d*, as the gate structure **132** shown in FIG. **1**B. FIG. **1**B is a cross-sectional view of part of the semiconductor device **100** in FIG. **1**A along a line AA′, in accordance with various embodiments.

[0051] The channel regions **132***a* include nanosheet channels extending in x direction and separated in y direction. The term nanosheet is used herein to designate any material portion with nanoscale, or even microscale dimensions, and having an elongate shape, regardless of the cross-sectional shape of this portion. Thus, this term designates both circular and substantially circular cross-section elongate material portions, and beam or bar-shaped material portions including for example a cylindrical in shape or substantially rectangular cross-section. In various embodiments, the channel region **132***a* includes materials such as germanium, a compound semiconductor such as silicon carbide, gallium arsenide, gallium phosphide, indium phosphide, indium arsenide, and/or indium antimonide, an alloy semiconductor such as SiGe, GaAsP, AlInAs, AlGaAs, InGaAs, GaInP, and/or GaInAsP, or combinations thereof.

[0052] The spacer layers **132***b* are above the channel regions **132***a*. In some embodiments, the spacer layer **132***b* is disposed conformally on top and configured as sidewalls of the gate structure **132**. The spacer layer **132***b* includes a dielectric material such as silicon oxide, silicon nitride, silicon carbide, silicon oxynitride, SiCN films, silicon oxycarbide, SiOCN films, and/or combinations thereof.

[0053] The metal gate layers **132***c* are disposed between spacer layers **132***b* and surrounded by the channel regions **132***a*. In some embodiments, the metal gate layer **132***c* includes a p-type work function metal or an n-type work function metal, and is deposited by CVD, PVD, and/or other suitable process. Exemplary p-type work function metals include TiN, TaN, Ru, Mo, Al, WN, ZrSi.sub.2, MoSi.sub.2, TaSi.sub.2, NiSi.sub.2, WN, other suitable p-type work function materials, or combinations thereof. Exemplary n-type work function metals include Ti, Ag, TaAl, TaAlC, TiAlN, TaC, TaCN, TaSiN, Mn, Zr, other suitable n-type work function materials, or combinations thereof. The one or more metal layers use aluminum (Al), tungsten (W), copper (Cu), cobalt (Co), and/or other suitable materials; and are formed by CVD, PVD, plating, and/or other suitable processes.

[0054] The inner spacer material layers **132***d* are formed to isolate metal gate layers **132***c* from active regions **121-122**. In some embodiments, the inner spacer material layer **132***d* is a low-K dielectric material, such as SiO.sub.2, SiN, SiCN, or SiOCN, and may be formed by a suitable deposition method, such as ALD. In various embodiments, sidewalls of the inner spacer material layers **132***d* are aligned with sidewalls of the channel regions **132***a*.

[0055] In some embodiments, each of the gate structures **131-133** further includes interfacial layers (not shown) wrapping around each of the channel regions **132***a*, and gate dielectric layers (not shown) covers the interfacial layer. In various embodiments, the interfacial layer includes a dielectric material including, for example, silicon oxide (SiO.sub.2) or silicon oxynitride (SiON), and is able to be formed by chemical oxidation, thermal oxidation, atomic layer deposition (ALD), chemical vapor deposition (CVD), and/or other suitable methods. In some embodiments, the gate dielectric layer uses a high-k dielectric material including, for example, hafnium oxide (HfO.sub.2), Al.sub.2O.sub.3, lanthanide oxides, TiO.sub.2, HfZrO, Ta.sub.2O.sub.3, HfSiO.sub.4, ZrO.sub.2, ZrSiO.sub.2, combinations thereof, or other suitable material, and the gate dielectric layer is formed by ALD and/or other suitable methods. The metal gate layer includes a p-type work function metal or an n-type work function metal, and is deposited by CVD, PVD, and/or other suitable process. Exemplary p-type work function metals include TIN, TaN, Ru, Mo, Al, WN, ZrSi.sub.2, MoSi.sub.2, TaSi.sub.2, NiSi.sub.2, WN, other suitable p-type work function materials, or combinations thereof. Exemplary n-type work function metals include Ti, Ag, TaAl, TaAlC, TiAlN, TaC, TaCN, TaSiN, Mn, Zr, other suitable n-type work function materials, or combinations thereof. The one or more metal layers use aluminum (Al), tungsten (W), copper (Cu), cobalt (Co), and/or other suitable materials; and are formed by CVD, PVD, plating, and/or other suitable processes.

[0056] The formations and/or materials associated with the gate structures **131-133** are given for illustrative purposes. Various formations and/or materials associated with the gate structures **131-133** are within the contemplated scope of the present disclosure.

[0057] With continuing reference to FIG. **1**B, the semiconductor device **100** further includes conductive segments (i.e., metal on oxide-definition areas ("MOOD" or "MD")) **151-152**. In some embodiments, the conductive segments **151-152** are patterns formed over the active region patterns to define electrical connections from active devices formed by the active regions to outside circuitry.

[0058] As shown in FIG. **1**B, the conductive segments **151-152** are disposed on the active regions **121-122**, respectively. The via VD**1** is coupled between the conductive line **141** and the conductive segment **151**, and accordingly, the active region **121** is coupled to the conductive line **141** through the via VD**1** and the conductive segment **151**. The via VB**1** is coupled between the power rail **111** and active region **122**.

[0059] With reference to FIG. **1**C, FIG. **1**C is an equivalent circuit corresponding to part of the semiconductor device **100** of FIGS. **1**A-**1**B, in accordance with various embodiments. In some embodiments, the active regions **121-122**, and the gate structure **132** are included in a structure operating as a transistor Tr in FIG. **1**C. The conductive segment **151** corresponds to a first terminal (i.e., source or drain terminal) of the transistor Tr, and the conductive segment **152** corresponds to a second terminal (i.e., drain or source terminal) of transistor Tr. The gate structure **132** corresponds to a control terminal of the transistor Tr.

[0060] In some embodiments, a resistance unit R**1** represents a resistance contributed by part of the routing arranged to couple the first terminal of the transistor Tr to the conductive line **141**. The aforementioned part of routing includes, for example, the via VD**1** and the conductive segment **151**. Similarly, the resistance unit R**2** represents a resistance contributed by another part of the routing arranged to couple the second terminal of the transistor Tr to the power rail **111**. The aforementioned another part of routing includes, for example, the via VB**1**. The details of the configuration of the resistance units R**1** and R**2** will be discussed in the following paragraphs.

[0061] Based on discussions above, in operations, for example, a control signal CS is received by the gate structure **132** through the conductive line **143** and the via VG**1**. Accordingly, the transistor Tr is configured to transmit, in response to the control signal CS, a signal VS from the power rail **111** to the conductive line **141** through the via VB**1**, the conductive segment **151**, and via VD**1**. In some embodiments, the aforementioned signal VS is a voltage signal having a supply voltage level for operating a device coupled with the transistor Tr. In various embodiments, the aforementioned signal VS is a data signal transmitted from another element in the semiconductor device **100**. The configurations of the operations of the semiconductor device **100** are given for illustrative purposes. Various implementations are within the contemplated scope of the present disclosure. For example, in some embodiments, the signal VS received from other elements in the semiconductor device **100** is transmitted from the conductive line **141** to the power rail **111**.

[0062] In some approaches, additional pick-up regions are integrated in a semiconductor device to connect a particular dopant type well or the substrate (e.g., a bulk of an active device such as a transistor) of an active device to a voltage source. In such approaches, the pick-up regions are arranged abutting with the active device in the layout view. In contrast, with the configurations of the present disclosure, the active device is connected to the voltage source from the power rail **111** in the layer below the active device. Accordingly, the cell area is reduced and a total cell height is smaller than in such approaches.

[0063] Furthermore, in various approaches, supply voltages are transmitted in power metal layers (e.g., a metal ten layer disposed ten layers above the metal zero layer) above the active device. In such arrangements, voltage signals experience a parasitic resistance induced by the routing of layers. With configurations of the present disclosure, the power rail **111** is disposed at the back side of the active device and closer to the active device, compared with the approaches. Alternatively stated, the routing has been shortened, and the resistance represented by the resistance unit R**2** is reduced correspondingly. Furthermore, the parasitic capacitances between layers experienced by the metal layers decrease as well. Accordingly, the performance (i.e., the speed) of the semiconductor device **100** is improved.

[0064] The configurations of FIGS. **1**A-**1**C are given for illustrative purposes. Various implementations are within the contemplated scope of the present disclosure. For example, in some embodiments, the via VG**1** is coupled between the conductive line **142** and the gate structure **132**.

[0065] Reference is now made to FIGS. **2**A-**2**C. FIG. **2**A is a layout diagram in a plan view of the semiconductor device **200**, FIG. **2**B is a cross-sectional view of part of the semiconductor device **200** in FIG. **2**A along a line BB′, and FIG. **2**C is an equivalent circuit corresponding to part of the semiconductor device **200** of FIGS. **2**A-**2**B, in accordance with various embodiments. With respect to the embodiments of FIGS. **1**A-**1**C, like elements in FIGS. **2**A-**2**C are designated with the same reference numbers for case of understanding. The specific operations of similar elements, which are already discussed in detail in above paragraphs, are omitted herein for the sake of brevity, unless there is a need to introduce the co-operation relationship with the elements shown in FIGS. **2**A-**2**C.

[0066] Compared with FIG. **1**A, instead of having the via VB**1**, the semiconductor device **200** does not include the via VB**1**, as shown in FIGS. **2**A-**2**B. In some embodiments, the semiconductor device **200** receives signals transmitted from other semiconductor devices, for example, the semiconductor device **100** through the conductive line **141**. In various embodiments, the active region **122** of the semiconductor device **200** is coupled to other elements (i.e., other active regions or conductive lines) through the conductive segment **152**. As shown in FIG. **2**C, due to the absence of the via VB**1**, there is no equivalent resistance depicted between the transistor Tr and the power rail **111**.

[0067] Reference is now made to FIGS. **3**A-**3**C. FIG. **3**A is a layout diagram in a plan view of the semiconductor device **300**, FIG. **3**B is a cross-sectional view of part of the semiconductor device **300** in FIG. **3**A along a line CC′, and FIG. **3**C is an equivalent circuit corresponding to part of the semiconductor device **300** of FIGS. **3**A-**3**B, in accordance with various embodiments. With respect to the embodiments of FIGS. **1**A-**2**C, like elements in FIGS. **3**A-**3**C are designated with the same reference numbers for case of understanding.

[0068] Compared with FIG. **1**A, the semiconductor device **300** further includes vias VD**2** and VB**2**. In some embodiments, the vias VD**2** and VB**2** are configured with respect to, for example, the vias VD**1** and VB**2**, respectively. As shown in FIG. **3**A, the vias VD**1** and VB**2** overlap with each other. The vias VD**2** and VB**1** overlap with each other. For illustration, the vias VB**1**-VB**2** have the same width in y direction.

[0069] Compared with FIG. **1**B, the via VB**2** is coupled between the active region **121** and the power rail **111**, and accordingly, the active region **121** is further coupled to the power rail **111**. In some embodiments, a resistance contributed by the routing of the via VB**2** represents as another resistance unit R**2** in FIG. **3**C. The via VD**2** is coupled between the conductive segment **152** and the conductive line **141**, and accordingly, the active region **122** is further coupled to the conductive line **141**. In some embodiments, a resistance contributed by the routing of the via VD**2** represents as another resistance unit R**1** in FIG. **3**C.

[0070] Based on discussions above, in operations, independent of the transistor Tr being turned off in response to the control signal CS, the signal VS is transmitted from the power rail **111** to the conductive line **141** through a first path Path**1** including the via VB**1**, the conductive segment **152**, and via VD**2** and a second path Path**2** including the via VB**2**, the conductive segment **151**, and via VD**1**, as shown in FIG. **3**B. Alternatively stated, a total resistance of a resistance unit R**3** between the conductive line **141** and power rail **111**, represented by the resistance units R**1** and R**2** in FIG. **3**C, is reduced due to two transmission paths.
[0071] The configurations of FIGS. **2**A-**3**C are given for illustrative purposes. Various implementations are within the contemplated scope of the present disclosure. For example, in some embodiments, the resistances of the vias VB**1**-VB**2** and/or VD**1**-VD**2** are different from each other.
[0072] Reference is now made to FIG. **4**. FIG. **4** is a schematic diagram of the integrated circuit **400**, in accordance with various embodiments. In some embodiments, the integrated circuit **400** includes, for example, at least one of the semiconductor devices **100**-**300**. For illustration, the integrated circuit **400** includes differential pair switches T**1**-T**2**, a current mirror unit T**3**, and resistance units R**4**-R**5**. Each of the differential pair switches T**1**-T**2** has a first terminal coupled to one of resistance units R**5** and a second terminal coupled to the current mirror unit T**3**. Resistance units R**4** are coupled between a voltage terminal V**1** (i.e., the voltage terminal V**1** is referred to as a terminal supporting a voltage V**1**) and the resistance units R**5**. The current mirror unit T**3** is coupled between a voltage terminal V**2** (i.e., the voltage terminal V**2** is referred to as a terminal supporting a voltage V**2**) and the differential pair switches T**1**-T**2**. In some embodiments, the voltages V**1**-V**2** are different from each other. In various embodiments, the voltage V**1** is greater than the voltage V**2** (e.g., a ground.)
[0073] In some embodiments, the resistance unit R**4** includes a structure implemented by the semiconductor device **300**. For example, the resistance unit R**4** is implemented by the resistance unit R**3** in FIG. **3**C. Accordingly, the resistance units R**4** receive the voltage V**1** from the power rail **111** and transfer the corresponding signals VS to the differential pair switches T**1**-T**2** through the conductive line **141**, as shown in FIG. **3**B. In various embodiments, the resistance unit R**5** corresponds to metal routing between one of the resistance unit R**4** and one of the differential pair switches T**1**-T**2**.
[0074] The differential pair switches T**1**-T**2** are configured to receive the signals VS from the resistance units R**5** in response to control signals S**1**-S**2** respectively. In some embodiments, the differential pair switches T**1**-T**2** include structures implemented by the semiconductor device **200**. For example, the differential pair switches T**1**-T**2** are implemented by the transistor Tr in FIG. **2**C. Accordingly, the differential pair switches T**1**-T**2** receive the signals VS, in response to the control signals S**1**-S**2** received at the gate structures **132** thereof, from the conductive line **141** coupled to the resistance units R**5**. In some embodiments, the differential pair switches T**1**-T**2** are configured to output a corresponding output signal OS at the conductive segment **152** thereof, as shown in FIG. **2**B. The output signal OS is further transmitted to the current mirror unit T**3**.
[0075] The current mirror unit T**3** is configured to receive the output signal OS from the differential pair switches T**1**-T**2** in response to a control signal S**3**. In some embodiments, the current mirror unit T**3** includes a structure implemented by the semiconductor device **100**. For example, the current mirror unit T**3** is implemented as the transistor Tr in FIG. **1**C. Accordingly, the current mirror unit T**3** receives, in response to the control signal S**3** received at the gate structure **132** thereof, the signal OS from the differential pair switches T**1**-T**2** through the conductive line **141** coupled thereto, and transmits a corresponding signal to the voltage terminal V**2**.
[0076] The configurations of FIG. **4** are given for illustrative purposes. Various implementations are within the contemplated scope of the present disclosure. For example, in some embodiments, the current mirror unit T**3** is configured to operate as a current source.
[0077] Reference is now made to FIG. **5**A. FIG. **5**A is a layout diagram in a plan view of the semiconductor device **500**, in accordance with various embodiments. For illustration, the

semiconductor device **500** includes a power rail **511**, an active area **520**, gate strips **531**, conductive lines **541**-**542**, conductive segments **551**, vias VD**3**, VB**3**, and VG**2**. In some embodiments, the power rail **511** is configured with respect to, for example, the power rail **111**. The active area **520** includes multiple active regions which are configured with respect to, for example, the active regions **121**-**122**. The gate strips **531** are configured with respect to, for example, the gate structures **131**-**133**. The conductive line **541** is configured with respect to, for example, the conductive line **141**, and the conductive line **542** is configured with respect to, for example, the conductive line **143**. The conductive segments **551** are configured with respect to, for example, the conductive segments **151**-**152**. The via VD**3** is configured with respect to, for example, the vias VD**1**-VD**2**. The via VB**3** is configured with respect to, for example, the vias VB**1**-VB**2**. The vias VG**2** are configured with respect to, for example, the via VG**1**. In some embodiments, the power rail **511** is arranged in a first layer. The active area **520** and the gate strips **531** are arranged in a second layer above the first layer. The conductive segments **551** are over the active area **520**. The conductive lines **541**-**542** are arranged in a third layer above the second layer. The via VB**3** is arranged between the first layer and the second layer. The vias VD**3** and VG**2** are arranged between the second layer and the third layer.

[0078] In some embodiments, the conductive line **541** is referred to as the conductive line coupled to a node nd**3** (as shown in FIG. **6**C) and the power rail **511** is referred to as the power rail coupled to a node nd**4** (as shown in FIG. **6**C), in which the nodes nd**3**-nd**4** are nodes in an integrated circuit included in the semiconductor device. In some embodiments, the node nd**3** is configured to receive a supply voltage transmitted from the node nd**4**. In some embodiments, the conductive line **542** is configured to receive a control signal (for example, the control signal CS) in operation for controlling the transistor structure including the gate strips **531**. The detailed configurations will be discussed in the following paragraphs.

[0079] As shown in FIG. **5**A, the power rail **511** and the active area **520** extend in x direction, and the active area **520** overlaps the power rail **511** in the layout view. The gate strips **531** extend in y direction and cross the power rail **511**. The gate strips **531** are separated from each other in x direction. The conductive lines **541**-**542** extend in x direction and are separated from each other in y direction. The conductive lines **541**-**542** partially overlap the power rail **511**. In some embodiments, the power rail **511** has a width greater than width of the active area **520** and the conductive lines **541**-**542** in y direction.

[0080] In some embodiments, as shown in FIG. **5**A, a width of the via VB**3** along y direction is substantially the same with a width of the active area **520**. In various embodiments, the width of the via VB**3** along y direction is between the width of the active area **520** and a width of the power rail **511**. In various embodiments, the via VB**3** has a tapered shape.

[0081] Reference is now made to FIG. **5**B. FIG. **5**B is a cross-sectional view of part of the semiconductor device **500** in FIG. **5**A along a line DD′, in accordance with various embodiments. As shown in FIG. **5**B, the conductive segment **551** is disposed on an active region **521** of the active area **520**. The via VD**3** is coupled between the conductive line **541** and the conductive segment **551**, and accordingly, the active region **521** is coupled to the conductive line **541** through the via VD**3** and the conductive segment **551**. The via VB**3** is coupled between the power rail **511** and active region **521**.

[0082] In some embodiments, a resistance contributed by a structure of routing including, for example, the vias VD**3**, VB**3**, the active region **521**, and the conductive segment **551**, between the power rail **511** and the conductive line **541** is represented as a resistance unit R**6**. In some embodiments, the resistance unit R**6** corresponds the combinations of the resistance units R**1**-R**2** of FIG. **3**C.

[0083] The configurations of FIGS. **5**A-**5**B are given for illustrative purposes. Various implementations are within the contemplated scope of the present disclosure. For example, in some embodiments, the semiconductor device **500** further includes multiple vias which are configured with respect to the vias VD**3** and VB**3** and coupled to the conductive segments **551** and other active regions of the active area **520**. Accordingly, more than one conductive paths are created between the power rail **511** and the conductive line **541**.

[0084] Reference is now made to FIG. **6**A. FIG. **6**A is a layout diagram in a plan view of the semiconductor device **600**, in accordance with various embodiments. With respect to the embodiments of FIGS. **5**A-**5**B, like elements in FIG. **6**A are designated with the same reference numbers for ease of understanding.

[0085] Compared with FIG. **5**A, the semiconductor device **600** includes more gate strips **531** and conductive segments **551**. In addition, a power rail corresponding to the power rail **511** has two portions including power rails **511*a*-511*b*** in the semiconductor device **600**. As shown in FIG. **6**A, the power rails **511*a*-511*b*** are separated from each other in x direction. The conductive line **541** overlaps both the power rails **511*a*-511*b***. Instead of having one via VD**3** and one via VB**3**, the semiconductor device **600** further includes two vias VD**3** and two vias VB**2** disposed at two parts of the semiconductor device **600**. Furthermore, each of the gate strips **531** is coupled with the conductive line **542** through one via VG**2**.

[0086] Reference is now made to FIG. **6**B. FIG. **6**B is a cross-sectional view of part of the semiconductor device **600** in FIG. **6**A along a line EE′, in accordance with various embodiments. As shown in FIG. **6**B, the power rail **511*a*** is coupled to the conductive line **541** through the vias VD**3**, VB**3**, the active region **521**, and the conductive segment **551** above the power rail **511*a***. Similarly, the power rail **511*b*** is coupled to the conductive line **541** through the vias VD**3**, VB**3**, the active region **521**, and the conductive segment **551** above the power rail **511*b***. Alternatively stated, two conductive paths are created for transmitting signals from/to the conductive line **541** to/from the power rails **511*a*-511*b***.

[0087] As shown in FIG. **6**B, in some embodiments, the gate strip **531** and the active regions **521** on opposite sides of the gate strip **531** are included in a structure operating as a transistor Ts. With reference to FIGS. **6**B-**6**C, FIG. **6**C is an equivalent circuit corresponding to part of the semiconductor device **600** of FIGS. **6**A-**6**B, in accordance with various embodiments. As illustratively shown in FIG. **6**C, the semiconductor device **600** includes multiple transistor Ts coupled in series.

[0088] In some embodiments, the active region **521** in FIG. **6**B coupled to the via VB**3** above the power rail **511*a*** is included in a structure operating as a terminal of a first transistor of the transistors Ts in FIG. **6**C. Another active region **521** in FIG. **6**B coupled to the via VB**3** above the power rail **511*b*** is included in a structure operating as a terminal of a second transistor, different from the first transistor, of the transistors Ts in FIG. **6**C. The gate strip **531** corresponds to a gate terminal of the transistor Ts.

[0089] In some embodiments, during operation, the gate terminals of the transistors Ts are coupled to a ground through the vias VG**2** and the conductive line **542**. Accordingly, the structures of the transistors Ts are configured to include decoupling capacitances while the signals are transmitted between the conductive line **541** and the power rails **511*a*-511*b***. Alternatively stated, the transistors Ts disposed beside the resistance unit R**6** or the transistors Ts disposed between the resistance units R**6** are tied off to include decoupling capacitances with the resistance units R**6**.

[0090] In some approaches, the extra area is required in an integrated circuit for decoupling capacitance and transmitting voltage from front side metal layers. With the configurations of the present disclosure, the functions of transmitting and decoupling are integrated in the semiconductor device **600**.

[0091] Reference is now made to FIG. **7**A. FIG. **7**A is a layout diagram in a plan view of the semiconductor device **700**, in accordance with various embodiments. With respect to the embodiments of FIGS. **6**A-**6**B, like elements in FIG. **7**A are designated with the same reference numbers for ease of understanding.

[0092] Compared with FIG. **6**A, instead of having a continuing conductive line **541** and the twopiece power rails **511***a*-**511***b*, the semiconductor device **700** includes a conductive line, corresponding to the conductive line **541** of FIG. **6**A, having two portions including conductive lines **541***a*-**541***b*. As shown in FIG. **7**A, the conductive lines **541***a*-**541***b* are separated from each other in x direction. Both the conductive lines **541***a*-**541***b* overlaps the power rail **511**.

[0093] Reference is now made to FIGS. **7**B-**7**C. FIG. **7**B is a cross-sectional view of part of the semiconductor device **700** in FIG. **7**A along a line FF′, and FIG. **7**C is an equivalent circuit corresponding to part of the semiconductor device **700** of FIGS. **7**A-**7**B, in accordance with various embodiments. As shown in FIG. **7**B, the power rail **511** is coupled to the conductive line **541***a* through the vias VD**3**, VB**3**, the active region **521**, and the conductive segment **551** underneath the conductive line **541***a*. Similarly, the power rail **511** is also coupled to the conductive line **541***b* through the vias VD**3**, VB**3**, the active region **521**, and the conductive segment **551** underneath the conductive line **541***b*. Alternatively stated, in some embodiments, the power rail **511** outputs/receives a signal to two devices through the separated conductive lines **541***a*-**541***b*, as shown in FIG. **7**C.

[0094] The configurations of FIGS. **6**A-**7**C are given for illustrative purposes. Various implementations are within the contemplated scope of the present disclosure. Reference is now made to FIGS. **8**A-**8**B. FIGS. **8**A-**8**B are equivalent circuits corresponding to part of the semiconductor devices **600**-**700**, respectively, in accordance with various embodiments. For example, in some embodiments, as shown in FIGS. **8**A-**8**B, during operation, the gate terminals of the transistors Ts disposed beside the resistance units R**6** are floating. Accordingly, parasitic capacitances in the semiconductor devices **600**-**700** are minimized and the low parasitic capacitances result in high operating speed. In another embodiment, the gate terminals of the transistors Ts disposed between the resistance units R**6** are floating. In still another embodiment, the gate terminals of the transistors Ts of FIGS. **8**A-**8**B are coupled to high-resistance units.

[0095] Reference is now made to FIG. **9**A. FIG. **9**A is a layout diagram in a plan view of the semiconductor device **900**, in accordance with various embodiments. With respect to the embodiments of FIGS. **1**A-**8**B, like elements in FIG. **9**A are designated with the same reference numbers for case of understanding.

[0096] As shown in FIG. **9**A, the semiconductor device **900** includes the cell CELL**1** corresponding to one of FIG. **1**A and a cell CELL**2** abutting the cell CELL**1** in y direction. In some embodiments, the cell CELL**1** of FIG. **9**A includes an active area **921** including the active regions **121**-**122**. The cell CELL**2** includes an active area **922**. In some embodiments, the cell CELL**2** is a mirror image across a mirror line **910** extending in x direction. Alternatively stated, a power rail **112** is configured with respect to the power rail **111** in the cell CELL**1**, and the power rails **111**-**112** are at the opposite sides of the mirror line **910** and aligned with each other. The active area **922** is configured with respect to the active area **921** in the cell CELL**1**, and the active areas **921**-**922** are at the opposite sides of the mirror line **910** and aligned with each other. A via VD**4** is configured with respect to the via VD**1** in the cell CELL**1** and the vias VD**1** and VD**4** are at the opposite sides of the mirror line **910** and aligned with each other. A via VB**4** is configured with respect to the via VB**1** in the cell CELL**1** and the vias VB**1** and VB**4** are at the opposite sides of the mirror line **910** and aligned with each other. The conductive lines **144** and **145** are configured with respect to the conductive lines **142** and **141** respectively, and the conductive line **143** is shared by the cells CELL**1**-CELL**2**. The gate structures **131**-**133** are shared by the cells CELL**1**-CELL**2**.

[0097] In some embodiments, the abutting cells CELL**1**-CELL**2** are included in a cell CELL**3** (e.g., a standard cell) for transmitting signals between the power rails **111**-**112** and the conductive lines **141** and **145**. As shown in FIG. **9**A, the cell CELL**3** includes the conductive lines **141**-**145** arranged in 5 metal tracks, and each of the cells CELL**1**-CELL**2** includes conductive lines in 2.5 metal tracks. Alternatively stated, a number of metal tracks included in each of the cells CELL**1**-CELL**2** is not an integer, and a total number of metal tracks included in the cells CELL**1**-CELL**2** is an integer. The configurations of the cells CELL**1**-CELL**3** are given for illustrative purposes. Various implementations are within the contemplated scope of the present disclosure. For example, in some embodiments, a number of metal tracks included in each of the cells CELL**1**-CELL**2** is an integer.

[0098] In some embodiments, the active areas **921**-**922** have different conductivity types. The active area **921** is of first conductivity type, for example, P-type. The active area **922** is of second conductivity type, for example, N-type.

[0099] FIG. **9**B is an equivalent circuit corresponding to part of the semiconductor device **900** of FIG. **9**A, in accordance with various embodiments. Reference is now made to FIGS. **9**A-**9**B. In some embodiments, the cell CELL**1** corresponds to a P-type transistor P**1** coupled with the power rail **111** and the conductive line **141**, and the cell CELL**2** corresponds to an N-type transistor N**1** coupled with the power rail **112** and the conductive line **145**. In operation, according to some embodiments, the shared gate structure **132** corresponds to gate terminals of the transistors P**1** and N**1**. A control signal S**4** is transmitted to the transistors P**1** and N**1** by the conductive line **143**. In some embodiments, when the control signal S**4** has a high logic state (i.e., a logic 1), the transistor N**1** is turned on to receive a voltage (e.g., a voltage VSS, in some embodiments, a ground) and provides the voltage to other devices (not shown) coupled to the semiconductor device **900** through the conductive line **145**. Similarly, when the control signal S**4** has a low logic state (e.g., a logic 0), the transistor P**1** is turned on to receive another voltage (e.g., a voltage VDD, in some embodiments, a voltage greater than the voltage VSS) and provides the voltage to other devices (not shown) coupled to the semiconductor device **900**.

[0100] The configurations of FIGS. **9**A-**9**B are given for illustrative purposes. Various implementations are within the contemplated scopes of the present disclosure. For example, in some embodiments, the cells CELL**1**-CELL**2** in the cell CELL**3** are implemented by at least one of the semiconductor device **200** in FIGS. **2**A-**2**C, the semiconductor device **300** in FIGS. **3**A-**3**C, or the combinations thereof.

[0101] Reference is now made to FIG. **10**A. FIG. **10**A is a layout diagram in a plan view of the semiconductor device **1000**, in accordance with various embodiments. With respect to the embodiments of FIGS. **1**A-**9**B, like elements in FIG. **10**A are designated with the same reference numbers for case of understanding.

[0102] Compared with FIG. **9**A, instead of having one cell CELL**1** and one cell CELL**2** in the cell CELL**3**, the cell CELL**3** of the semiconductor device **1000** further includes multiple cells CELL**1** and multiple cells CELL**2**. For illustration, the cells CELL**1** and the cells CELL**2** are interlaced. As shown in FIG. **10**A, the semiconductor device **1000** further includes conductive lines **1001**-**1010** and power rails **113**-**114**. In some embodiments, the conductive lines **1001**-**1010** are configured with respect to, for example, the conductive lines **141**-**145**. The power rails **113**-**114** are configured with respect to, for example, the power rails **111**-**112**.

[0103] For illustration, the conductive lines **1001**-**1005** are included in the cells CELL**1**-CELL**2** of the upper part of the cell CELL**3**, and the conductive lines **1006**-**1010** are included in the cells CELL**1**-CELL**2** of the bottom part of the cell CELL**3**. The power rails **113**-**114** are included in the cells CELL**1**-CELL**2** of the bottom part of the cell CELL**3** respectively. The gate structures **131**-**133** are further shared by all cells in the cell CELL**3**.

[0104] As shown in FIG. **10**A, the semiconductor device **1000** further includes the active areas **921** in the cells CELL**1** and the active areas **922** in the cells CELL**2**. In some embodiments, the active areas **921** are P-type and the active areas **922** are N-type.

[0105] With reference to FIG. **10**B, FIG. **10**B is an equivalent circuit corresponding to part of the semiconductor device **1000** of FIG. **10**A, in accordance with various embodiments. Reference is now made to FIGS. **10**A-**10**B. In some embodiments, the cells CELL**1**-CELL**2** of the upper part of the cell CELL**3** correspond to, respectively the P-type transistor P**1** coupled with the power rail **111** and the conductive line **1001** and the N-type transistor N**1** coupled with the power rail **112** and the conductive line **1005**. Similarly, the cells CELL**1**-CELL**2** of the bottom part of the cell CELL**3** correspond to, respectively the P-type transistor P**2** coupled with the power rail **113** and the conductive line **1006** and the N-type transistor N**2** coupled with the power rail **114** and the conductive line **1010**.

[0106] In operation, according to some embodiments, the shared gate structure **132** corresponds to gate terminals of the transistors P**1**-P**2** and N**1**-N**2**. The control signal S**4** is transmitted to the transistors P**1**-P**2** and N**1**-N**2** by the conductive line **1003** and/or the conductive line **1008**. In some embodiments, when the control signal S**4** has a high logic state (e.g., a logic 1), the transistors N**1**-N**2** are turned on to receive a voltage (e.g., a voltage VSS, in some embodiments, a ground) and provides the voltage to other device (not shown) coupled to the semiconductor device **1000** through the conductive lines **1005** and **1010**. Similarly, when the control signal S**4** has a low logic state (e.g., a logic 0), the transistors P**1**-P**2** are turned on to receive another voltage (e.g., a voltage VDD, in some embodiments, a voltage greater than the voltage VSS) and provides the voltage to other device (not shown) coupled to the semiconductor device **1000** through the conductive lines **1001** and **1006**.

[0107] The configurations of FIGS. **10**A-**10**B are given for illustrative purposes. Various implementations are within the contemplated scope of the present disclosure. For example, in some embodiments, a number of the cells CELL**1** is equal to a number of the cells CELL**2** which ranges from two to four. In some embodiments, the number of the cells CELL**1** equal to the number of the cells CELL**2** is greater than four.

[0108] In various embodiments, the active areas **921-922** in the cells CELL**1**-CELL**2** of the upper part of the cell CELL**3** are P-type, and the active areas **921-922** in the cells CELL**1**-CELL**2** of the bottom part of the cell CELL**3** are N-type. Alternatively stated, the active areas **921-922** in the cell CELL**3** are combinations of P-type active areas and N-type active areas arranged in an arbitrary order. For example, in some embodiments, the sequence of types of the active areas **921-922**, from the top of the cell CELL**3** to the bottom of the cell CLEE**3**, can be PPNP, PNNP, PPPN, NPNP, NPPN, NPPP, or any other suitable arrangements.

[0109] Reference is now made to FIG. **11**. FIG. **11** is a layout diagram in a plan view of the semiconductor device **1100**, in accordance with various embodiments. With respect to the embodiments of FIGS. **1**A-**10**B, like elements in FIG. **11** are designated with the same reference numbers for case of understanding.

[0110] Compared with FIG. **9**A, instead of the cells CELL**1**-CELL**2** having conductive lines arranged in 2.5 metal tracks, cells CELL**1**-CELL**2** in a cell CELL**4** have conductive lines arranged in 3 metal tracks in the semiconductor device **1100**, as shown in FIG. **11**. For illustration, the cell CELL**1** includes the conductive lines **141**, **142**, half of the conductive line **143**, and half of the conductive line **146**. Similarly, the cell CELL**2** includes the conductive lines **144**, **145**, half of the conductive line **143**, and half of the conductive line **147**.

[0111] Reference is now made to FIG. **12**A. FIG. **12**A is a layout diagram in a plan view of the semiconductor device **1200**, in accordance with various embodiments. With respect to the embodiments of FIGS. **1**A-**11**, like elements in FIG. **12**A are designated with the same reference numbers for ease of understanding.

[0112] For illustration, compared with the semiconductor device **1000** and the cell CELL**4** of FIG. **11**, the semiconductor device **1200** further includes the conductive lines **1011-1013**. In some embodiments, the conductive lines **1001-1005**, and **1011-1012** of FIG. **12**A are configured with respect to, for example, the conductive lines **141-147** of FIG. **11**.

[0113] For illustration, the cell CELL**1** of the cell CELL**4** includes the conductive lines **1001**, **1002**, half of the conductive line **1003**, and half of the conductive line **1011**. Similarly, the cell CELL**2** of the cell CELL**4** includes the conductive lines **1004**, **1005**, half of the conductive line **1003**, and half of the conductive line **1012**.

[0114] In addition, the semiconductor device **1200** further includes another cell CELL**1** excluded from the cell CELL**4** and disposed at a side, opposing the cell CELL**1** included in the cell CELL**4**, of the cell CELL**2**, as shown in FIG. **12**A. For illustration, the another cell CELL**1** includes the conductive lines **1006**, **1007**, half of the conductive line **1008**, and half of the conductive line **1013**.

[0115] As mentioned above, compared with FIG. **10**A, instead of having equal proportions of the cells CELL**1** and CELL**2** in the cell CELL**3** in some embodiments, the semiconductor device **1200** includes different ratios of cells of different conductivity types. For illustration, the semiconductor device **1200** of FIG. **12**A includes two cells CELL**1** and one cell CELL**2**. In some embodiments, the active areas **921** are P-type and the active area **922** is N-type.

[0116] With reference to FIG. **12**B, FIG. **12**B is an equivalent circuit corresponding to part of the semiconductor device **1200** of FIG. **12**A, in accordance with various embodiments. Reference is now made to FIGS. **12**A-**12**B. In some embodiments, the cells CELL**1**-CELL**2** of the cell CELL**4** correspond to, respectively the P-type transistor P**1** coupled with the power rail **111** and the conductive line **1001** and the N-type transistor N**1** coupled with the power rail **112** and the conductive line **1005**. The cell CELL**1** excluded from the cell CELL**4** corresponds to the P-type transistor P**2** coupled with the power rail **113** and the conductive line **1006**.

[0117] In operation, according to some embodiments, the shared gate structure **132** corresponds to gate terminals of the transistors P**1**-P**2** and N**1**. The control signal S**4** is transmitted to the transistors P**1**-P**2** and N**1** by the conductive line **1003** and/or the conductive line **1008**. In some embodiments, when the control signal S**4** has a high logic state (e.g., a logic 1), the transistor N**1** is turned on to receive a voltage (e.g., a voltage VSS, in some embodiments, a ground) and provides the voltage to other device (not shown) coupled to the semiconductor device **1200** through the conductive line **1005**. Similarly, when the control signal S**4** has a low logic state (e.g., a logic 0), the transistors P**1**-P**2** are turned on to receive another voltage (e.g., a voltage VDD, in some embodiments, a voltage greater than the voltage VSS) and provides the voltage to other device (not shown) coupled to the semiconductor device **1200** through the conductive lines **1001** and **1006**.

[0118] The configurations of FIGS. **12**A-**12**B are given for illustrative purposes. Various implementations are within the contemplated scope of the present disclosure. For example, in some embodiments, the semiconductor device **1200** includes a number of P-type transistors greater than a number of N-type transistors or a number of N-type transistors greater than a number of P-type transistors. In some embodiments, the number of a first type of the P-type or N-type transistors ranges from two to four and the number of the second type of the P-type or N-type transistors ranges from one to three.

[0119] Reference is now made to FIG. **13**A. FIG. **13**A is a flow chart of a method **1300**A of forming an integrated circuit included in a semiconductor device, for example, **300-600**, or **700**, in accordance with some embodiments of the present disclosure. It is understood that additional operations can be provided before, during, and/or after the processes shown by FIG. **13**A, and some of the operations described below can be replaced or eliminated, for additional embodiments of the method. The order of the operations/processes may be interchangeable. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements. The method **1300**A includes operations **1310**, **1320**, and **1321-1325** that are described below with reference to the integrated circuit **400** of FIG. **4** and the semiconductor device **600** of FIGS. **6**A-**6**C, as a non-limiting example.

[0120] In some embodiments, some or all of method **1300**A is executed by a processor of a computer. In some embodiments, some or all of method **1300**A is executed by a processor **1402** of an electronic design automation (EDA) system **1400**, discussed below with respect to FIG. **14**.

[0121] In operation **1310**, the connection configuration between a node nd**1** and a node nd**2** in the integrated circuit **400** shown in FIG. **4** is identified. For illustration, the node nd**1** receives the voltage V**1** and is coupled to the nd**2** through the resistance unit R**4**.

[0122] In operation **1320**, in response to the connection configuration indicating that the node nd**2** is configured to receive the voltage V**1** transmitted from the node nd**1**, a layout design of the integrated circuit is generated, for example, as shown in part in FIG. **3**A.

[0123] Moreover, in some embodiments, the generating the layout design includes the operation

1321, in which the conductive line **141** extending along x direction in the first layer at the front side of the integrated circuit **400** is generated to be coupled to the node nd**2**, as shown FIG. **3**A.

[0124] Subsequently, in some embodiments, the generating the layout design further includes the operation **1322**, in which the power rail **111** extending along x direction in a second layer, below the first layer, at the back side of the integrated circuit **400** is generated to be coupled to the node nd**1**.

[0125] The generating the layout design further includes the operation **1323**, in some embodiments, in which the active area **120** is generated extending along x direction in a third layer, between the first and second layers.

[0126] The generating the layout design further includes the operation **1324**, in some embodiments, in which the via VD**1** is generated to be coupled between the active region **121** and the conductive line **141**, and in some embodiments, the via VD**2** is generated to be coupled between the active region **122** and the conductive line **141**, as shown in FIGS. **3**A-**3**B.

[0127] The generating the layout design further includes the operation **1325**, in some embodiments, in which the via VB**1** is generated to be coupled between the active region **122** and the power rail **111**, and in some embodiments, the via VB**2** is generated to be coupled between the active region **121** and the power rail **111**, as shown in FIGS. **3**A-**3**B. In some embodiments, along the y direction, the active area **120** and the vias VB**1**-VB**2** have a same width. In some embodiments, as shown in FIG. **3**A, the via VD**1** overlaps the via VB**2**, and the via VD**2** overlaps the via VB**1**.

[0128] In some embodiments, the generating the layout design of the method **1300**A further includes generating multiple gate strips **531** which extend in y direction and generating the conductive line **542**, as shown in FIG. **6**A. For illustration, the gate strips **531** extend in y direction and are interposed between the vias VD**3** which couples the active regions **521** to the conductive line **541**. The gate strips **531** are coupled to the conductive line **542** through the vias VG**2**.

[0129] In some embodiments, as shown in FIG. **6**A, the generating the power rail **511** includes generating the power rail **511***a* (the first portion of the power rail **511**) and the power rail **511***b* (the second portion of the power rail **511**, separated from the first portion). In some embodiments, patterns corresponding to the power rail **511***a*, the vias VD**3**, VB**3** that are above the power rail **511***a* are overlapped with each other in FIG. **6**A. Similarly, in some embodiments, patterns corresponding to the power rail **511***b*, and the vias VD**3**, VB**3** that are above the power rail **511***b* are overlapped with each other in FIG. **6**A.

[0130] In some embodiments, the method **1300**A further includes one or more operations of manufacturing at least one element of the integrated circuit, for example, the integrated circuit **400**, based on the layout design, as part of an IC manufacturing flow, e.g., an IC manufacturing flow corresponding to an IC manufacturing system **1500** discussed below with respect to FIG. **15**.

[0131] Reference is now made to FIG. **13**B. FIG. **13**B is a flow chart of a method **1300**B of fabricating the semiconductor devices **100-700**, or **900-1200**, in accordance with some embodiments of the present disclosure. It is understood that additional operations can be provided before, during, and/or after the processes shown by FIG. **13**B, and some of the operations described below can be replaced or eliminated, for additional embodiments of the method. The order of the operations/processes may be interchangeable. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements. The method **1300**B includes operations **1301-1305** that are described below with reference to the semiconductor device **500** as a non-limiting example.

[0132] In some embodiments, method **1300**B is usable by an IC manufacturing system as part of an IC manufacturing flow, e.g., IC manufacturing system **1500** discussed below with respect to FIG. **15**.

[0133] In operation **1301**, an active area, e.g., the active area **520**, is formed at a first side (e.g., a front side above the via VB) of the semiconductor device **500** and extends in x direction, as shown in FIG. **5**B.

[0134] In some embodiments, the method **1300**B further includes forming one or more conductive segments, e.g., the conductive segments **551**, on the active area, e.g., the active area **520**.

[0135] In operation **1302**, a via, e.g., the via VD**3**, is formed on the conductive segment, e.g., the conductive segment **551**, above an active region of the active area, e.g., the active region **521** of the active area **520**.

[0136] In operation **1303**, a conductive line, e.g., the conductive line **541**, is formed above and coupled to the active area through the via, e.g., the active area **520** through the via VD**3**. The conductive line, e.g., conductive line **541** extends in x direction.

[0137] In some embodiments, after the manufacturing processes for components (i.e., active devices) at the front side of the semiconductor device, e.g., the semiconductor device **500**, is complete, a substrate (not shown) is removed and the wafer is flipped upside down for manufacturing process performing at the backside of the semiconductor device, e.g., the semiconductor device **500**.

[0138] In operation **1304**, a back-side via, e.g., the via VB**3**, is formed at a second side (i.e., a back side below the active area **520**) opposing the first side of the semiconductor device **500**.

[0139] In operation **1305**, a power rail, e.g., the power rail **511**, is formed below the back-side via, e.g., the via VB**3**, and coupled to the active area, e.g., the active area **520**, through the back-side via, as shown in FIG. **5**B. In some embodiments, after the wafer is flipped, the power rail is formed above the back-side via.

[0140] In some embodiments, the method **1300**B further includes forming multiple back-side vias, e.g., the multiple vias VB**3**, in operation **1304**. As shown in FIG. **6**B, one of the vias VB**3** is formed to couple the active region **521** and the power rail **511***a*, and the other is formed to couple another active region **510** and the power rail **511***b*. In some embodiments, the method **1300**B further includes forming gate strips, e.g., the gate strips **531**, between the back-side vias.

[0141] In some embodiments, the method **1300**B further includes forming conductive lines that are arranged in multiple, e.g., three metal tracks above the power rail. For example, as shown in FIG. **11**, the conductive lines **141-142** and **146** are arranged in three metal tracks above the power rail **111**. Similarly, the conductive lines **144-145** and **147** are arranged in three metal tracks above the power rail **112**.

[0142] In some embodiments, the method **1300**B further includes forming multiple active areas of a first conductivity type and multiple active areas of a second conductivity type different from the first conductivity type. For example, as shown in FIG. **12**A, the active areas **921** are P-type and the active area **922** is N-type. A number of the active areas **921** (e.g., 2) is greater than a number of the active areas **922** (e.g., 1.)

[0143] Reference is now made to FIG. **14**. FIG. **14** is a block diagram of EDA system **1400** capable of designing an integrated circuit layout design, in accordance with some embodiments of the present disclosure. EDA system **1400** is configured to implement one or more operations of the method **1300**A disclosed in FIG. **13**A, and further explained in conjunction with FIGS. **1**A-**12**B. In some embodiments, EDA system **1400** includes an APR system.

[0144] In some embodiments, EDA system **1400** is a general purpose computing device including a hardware processor **1402** and a non-transitory, computer-readable storage medium **1404**. Storage medium **1404**, amongst other things, is encoded with, i.e., stores, computer program code (instructions) **1406**, i.e., a set of executable instructions. Execution of instructions **1406** by hardware processor **1402** represents (at least in part) an EDA tool which implements a portion or all of a method, e.g., the method **1300**A.

[0145] The processor **1402** is electrically coupled to computer-readable storage medium **1404** via a bus **1408**. The processor **1402** is also electrically coupled to an I/O interface **1410** and a fabrication tool **1416** by bus **1408**. A network interface **1412** is also electrically connected to processor **1402** via bus **1408**. Network interface **1412** is connected to a network **1414**, so that processor **1402** and computer-readable storage medium **1404** are capable of connecting to external elements via network **1414**. The processor **1402** is configured to execute computer program code **1406** encoded in computer-readable storage medium **1404** in order to cause EDA system **1400** to be usable for performing a portion or all of the noted processes and/or methods. In one or more embodiments, processor **1402** is a central processing unit (CPU), a multi-processor, a distributed processing system, an application specific integrated circuit (ASIC), and/or a suitable processing unit.

[0146] In one or more embodiments, computer-readable storage medium **1404** is an electronic, magnetic, optical, electromagnetic, infrared, and/or a semiconductor system (or apparatus or device). For example, computer-readable storage medium **1404** includes a semiconductor or solid-state memory, a magnetic tape, a removable computer diskette, a random access memory (RAM), a read-only memory (ROM), a rigid magnetic disk, and/or an optical disk. In one or more embodiments using optical disks, computer-readable storage medium **1404** includes a compact disk-read only memory (CD-ROM), a compact disk-read/write (CD-R/W), and/or a digital video disc (DVD).

[0147] In one or more embodiments, storage medium **1404** stores computer program code **1406** configured to cause EDA system **1400** (where such execution represents (at least in part) the EDA tool) to be usable for performing a portion or all of the noted processes and/or methods. In one or more embodiments, storage medium **1404** also stores information which facilitates performing a portion or all of the noted processes and/or methods. In one or more embodiments, storage medium **1404** stores IC layout diagram **1420** of standard cells including such standard cells as disclosed herein, for example, a cell(s) including in the semiconductor devices **100-700** and **900-1200** discussed above with respect to FIGS. **1**A-**12**B.

[0148] EDA system **1400** includes I/O interface **1410**. I/O interface **1410** is coupled to external circuitry. In one or more embodiments, I/O interface **1410** includes a keyboard, keypad, mouse, trackball, trackpad, touchscreen, and/or cursor direction keys for communicating information and commands to processor **1402**.

[0149] EDA system **1400** also includes network interface **1412** coupled to processor **1402**. Network interface **1412** allows EDA system **1400** to communicate with network **1414**, to which one or more other computer systems are connected. Network interface **1412** includes wireless network interfaces such as BLUETOOTH, WIFI, WIMAX, GPRS, or WCDMA; or wired network interfaces such as ETHERNET, USB, or IEEE-1364. In one or more embodiments, a portion or all of noted processes and/or methods, is implemented in two or more systems **1400**.

[0150] In some embodiments, EDA system **1400** also includes the fabrication tool **1416** coupled to processor **1402**. The fabrication tool **1416** is configured to fabricate integrated circuits, e.g., the semiconductor device **100-700** and **900-1200** illustrated in FIGS. **1**A-**12**B, according to the design files processed by the processor **1402**.

[0151] EDA system **1400** is configured to receive information through I/O interface **1410**. The information received through I/O interface **1410** includes one or more of instructions, data, design rules, libraries of standard cells, and/or other parameters for processing by processor **1402**. The information is transferred to processor **1402** via bus **1408**. EDA system **1400** is configured to receive information related to a UI through I/O interface **1410**. The information is stored in computer-readable medium **1404** as design specification **1422**.

[0152] In some embodiments, a portion or all of the noted processes and/or methods is implemented as a standalone software application for execution by a processor. In some embodiments, a portion or all of the noted processes and/or methods is implemented as a software application that is a part of an additional software application. In some embodiments, a portion or all of the noted processes and/or methods is implemented as a plug-in to a software application. In some embodiments, at least one of the noted processes and/or methods is implemented as a software application that is a portion of an EDA tool. In some embodiments, a portion or all of the noted processes and/or methods is implemented as a software application that is used by EDA system **1400**. In some embodiments, a layout diagram which includes standard cells is generated using a tool such as VIRTUOSO® available from CADENCE DESIGN SYSTEMS, Inc., or another suitable layout generating tool.

[0153] In some embodiments, the processes are realized as functions of a program stored in a non-transitory computer readable recording medium. Examples of a non-transitory computer readable recording medium include, but are not limited to, external/removable and/or internal/built-in storage or memory unit, for example, one or more of an optical disk, such as a DVD, a magnetic disk, such as a hard disk, a semiconductor memory, such as a ROM, a RAM, a memory card, and the like.

[0154] FIG. **15** is a block diagram of IC manufacturing system **1500**, and an IC manufacturing flow associated therewith, in accordance with some embodiments. In some embodiments, based on a layout diagram, at least one of (A) one or more semiconductor masks or (B) at least one component in a layer of a semiconductor integrated circuit is fabricated using IC manufacturing system **1500**.

[0155] In FIG. **15**, IC manufacturing system **1500** includes entities, such as a design house **1520**, a mask house **1530**, and an IC manufacturer/fabricator ("fab") **1550**, that interact with one another in the design, development, and manufacturing cycles and/or services related to manufacturing an IC device **1560**. The entities in IC manufacturing system **1500** are connected by a communications network. In some embodiments, the communications network is a single network. In some embodiments, the communications network is a variety of different networks, such as an intranet and the Internet. The communications network includes wired and/or wireless communication channels. Each entity interacts with one or more of the other entities and provides services to and/or receives services from one or more of the other entities. In some embodiments, two or more of design house **1520**, mask house **1530**, and IC fab **1550** is owned by a single larger company. In some embodiments, two or more of design house **1520**, mask house **1530**, and IC fab **1550** coexist in a common facility and use common resources.

[0156] Design house (or design team) **1520** generates an IC design layout diagram **1522**. IC design layout diagram **1522** includes various geometrical patterns, for example, an layout design depicted in FIGS. **1**B, **2**B, **3**B, **5**A, **6**A, **7**A, **9**A, **10** A, **11**, and/or **12**A, designed for an IC device **1560**, for example, the semiconductor devices **100-700** and **900-1200** in FIGS. **1**A-**12**B. The geometrical patterns correspond to patterns of metal, oxide, or semiconductor layers that make up the various components of IC device **1560** to be fabricated. The various layers combine to form various IC features. For example, a portion of IC design layout diagram **1522** includes various IC features, such as an active region, gate electrode, source and drain, conductive segments or vias of an interlayer interconnection, to be formed in a semiconductor substrate (such as a silicon wafer) and various material layers disposed on the semiconductor substrate. Design house **1520** implements a proper design procedure to form IC design layout diagram **1522**. The design procedure includes one or more of logic design, physical design or place and route. IC design layout diagram **1522** is presented in one or more data files having information of the geometrical patterns. For example, IC design layout diagram **1522** can be expressed in a GDSII file format or DFII file format.

[0157] Mask house **1530** includes data preparation **1532** and mask fabrication **1544**. Mask house **1530** uses IC design layout diagram **1522** to manufacture one or more masks **1545** to be used for fabricating the various layers of IC device **1560** according to IC design layout diagram **1522**. Mask house **1530** performs mask data preparation **1532**, where IC design layout diagram **1522** is translated into a representative data file ("RDF"). Mask data preparation **1532** provides the RDF to mask fabrication **1544**. Mask fabrication **1544** includes a mask writer. A mask writer converts the RDF to an image on a substrate, such as a mask (reticle) **1545** or a semiconductor wafer **1553**. The IC design layout diagram **1522** is manipulated by mask data preparation **1532** to comply with particular characteristics of the mask writer and/or requirements of IC fab **1550**. In FIG. **15**, data preparation **1532** and mask fabrication **1544** are illustrated as separate elements. In some embodiments, data preparation **1532** and mask fabrication **1544** can be collectively referred to as mask data preparation.

[0158] In some embodiments, data preparation **1532** includes optical proximity correction (OPC) which uses lithography enhancement techniques to compensate for image errors, such as those that can arise from diffraction, interference, other process effects and the like. OPC adjusts IC design layout diagram **1522**. In some embodiments, data preparation **1532** includes further resolution enhancement techniques (RET), such as off-axis illumination, sub-resolution assist features, phase-shifting masks, other suitable techniques, and the like or combinations thereof. In some embodiments, inverse lithography technology (ILT) is also used, which treats OPC as an inverse imaging problem.
[0159] In some embodiments, data preparation **1532** includes a mask rule checker (MRC) that checks the IC design layout diagram **1522** that has undergone processes in OPC with a set of mask creation rules which contain certain geometric and/or connectivity restrictions to ensure sufficient margins, to account for variability in semiconductor manufacturing processes, and the like. In some embodiments, the MRC modifies the IC design layout diagram **1522** to compensate for limitations during mask fabrication **1544**, which may undo part of the modifications performed by OPC in order to meet mask creation rules.
[0160] In some embodiments, data preparation **1532** includes lithography process checking (LPC) that simulates processing that will be implemented by IC fab **1550** to fabricate IC device **1560**. LPC simulates this processing based on IC design layout diagram **1522** to create a simulated manufactured device, such as IC device **1560**. The processing parameters in LPC simulation can include parameters associated with various processes of the IC manufacturing cycle, parameters associated with tools used for manufacturing the IC, and/or other aspects of the manufacturing process. LPC takes into account various factors, such as aerial image contrast, depth of focus (DOF), mask error enhancement factor (MEEF), other suitable factors, and the like or combinations thereof. In some embodiments, after a simulated manufactured device has been created by LPC, if the simulated device is not close enough in shape to satisfy design rules, OPC and/or MRC are be repeated to further refine IC design layout diagram **1522**.
[0161] It should be understood that the above description of data preparation **1532** has been simplified for the purposes of clarity. In some embodiments, data preparation **1532** includes additional features such as a logic operation (LOP) to modify the IC design layout diagram **1522** according to manufacturing rules. Additionally, the processes applied to IC design layout diagram **1522** during data preparation **1532** may be executed in a variety of different orders.
[0162] After data preparation **1532** and during mask fabrication **1544**, a mask **1545** or a group of masks **1545** are fabricated based on the modified IC design layout diagram **1522**. In some embodiments, mask fabrication **1544** includes performing one or more lithographic exposures based on IC design layout diagram **1522**. In some embodiments, an electron-beam (e-beam) or a mechanism of multiple e-beams is used to form a pattern on a mask (photomask or reticle) **1545** based on the modified IC design layout diagram **1522**. Mask **1545** can be formed in various technologies. In some embodiments, mask **1545** is formed using binary technology. In some embodiments, a mask pattern includes opaque regions and transparent regions. A radiation beam, such as an ultraviolet (UV) beam, used to expose the image sensitive material layer (for example, photoresist) which has been coated on a wafer, is blocked by the opaque region and transmits through the transparent regions. In one example, a binary mask version of mask **1545** includes a transparent substrate (for example, fused quartz) and an opaque material (for example, chromium) coated in the opaque regions of the binary mask. In another example, mask **1545** is formed using a phase shift technology. In a phase shift mask (PSM) version of mask **1545**, various features in the pattern formed on the phase shift mask are configured to have proper phase difference to enhance the resolution and imaging quality. In various examples, the phase shift mask can be attenuated PSM or alternating PSM. The mask(s) generated by mask fabrication **1544** is used in a variety of processes. For example, such a mask(s) is used in an ion implantation process to form various doped regions in semiconductor wafer **1553**, in an etching process to form various etching regions

in semiconductor wafer **1553**, and/or in other suitable processes.

[0163] IC fab **1550** includes wafer fabrication **1552**. IC fab **1550** is an IC fabrication business that includes one or more manufacturing facilities for the fabrication of a variety of different IC products. In some embodiments, IC Fab **1550** is a semiconductor foundry. For example, there may be a manufacturing facility for the front end fabrication of a plurality of IC products (front-end-of-line (FEOL) fabrication), while a second manufacturing facility may provide the back end fabrication for the interconnection and packaging of the IC products (back-end-of-line (BEOL) fabrication), and a third manufacturing facility may provide other services for the foundry business.

[0164] In some embodiments, IC fab **1550** includes fabrication tools configured to execute various manufacturing operations on semiconductor wafer **1553** such that IC device **1560** is fabricated in accordance with the mask(s), e.g., mask **1545**. In various embodiments, fabrication tools include one or more of a wafer stepper, an ion implanter, a photoresist coater, a process chamber, e.g., a CVD chamber or LPCVD furnace, a CMP system, a plasma etch system, a wafer cleaning system, or other manufacturing equipment capable of performing one or more suitable manufacturing processes as discussed herein.

[0165] IC fab **1550** uses mask(s) **1545** fabricated by mask house **1530** to fabricate IC device **1560**. Thus, IC fab **1550** at least indirectly uses IC design layout diagram **1522** to fabricate IC device **1560**. In some embodiments, semiconductor wafer **1553** is fabricated by IC fab **1550** using mask(s) **1545** to form IC device **1560**. In some embodiments, the IC fabrication includes performing one or more lithographic exposures based at least indirectly on IC design layout diagram **1522**. Semiconductor wafer **1553** includes a silicon substrate or other proper substrate having material layers formed thereon. Semiconductor wafer **1553** further includes one or more of various doped regions, dielectric features, multilevel interconnects, and the like (formed at subsequent manufacturing steps).

[0166] As described above, semiconductor devices in the present disclosure provide a backside power rail(s) in analog cells to transmit power signals to active devices at front side. With the configurations of the present disclosure, shorter routing between the active devices and the power rail results in faster performance speed. Moreover, by disposing the power rails at the back side of the semiconductor devices, front side area can be utilized more effectively.

[0167] In some embodiments, an IC device includes a first conductive line on a front side of a semiconductor wafer, a first power rail on a back side of the semiconductor wafer, a first gate structure extending in a first direction on the front side of the semiconductor wafer, first and second active regions adjacent to the first gate structure, a first via between and electrically connected to the first active region and the first conductive line, and a second via between and electrically connected to the first power rail and either the first active region or the second active region, wherein a plane perpendicular to the first direction intersects each of the first conductive line, the first power rail, the first gate structure, and the first and second active regions. In some embodiments, the second via is between and electrically connected to the first power rail and the second active region and the IC device includes at least one channel region extending through the first gate structure between the first and second active regions. In some embodiments, the second via is between and electrically connected to the first power rail and the first active region and the IC device includes a third via between and electrically connected to the second active region and the first conductive line and a fourth via between and electrically connected to the first power rail and the second active region. In some embodiments, the second via is between and electrically connected to the first power rail and the first active region and the first active region and the first and second vias are aligned in the plane in a second direction perpendicular to the first direction. In some embodiments, the IC device includes a second gate structure extending in the first direction on the front side of the semiconductor wafer, a third active region adjacent to the second gate structure, and third and fourth vias electrically connected to the third active region and aligned in the plane with the third active region in the second direction, wherein one of the IC device includes a second power rail on the back side of the semiconductor wafer, the third via is between and electrically connected to the third active region and the first conductive line, and the fourth via is between and electrically connected to the third active region and the second power rail, or the IC device includes a second conductive line on the front side of the semiconductor wafer, the third via is between and electrically connected to the third active region and the second conductive line, and the fourth via is between and electrically connected to the third active region and the first power rail. In some embodiments, the first gate structure and the second gate structure are between the first active region and the third active region and each of the first gate structure and the second gate structure is coupled to a ground voltage connection. In some embodiments, the first gate structure and the second gate structure are between the first active region and the third active region and each of the first gate structure and the second gate structure is configured to float. In some embodiments, the second via has a width in the first direction greater than a width of the first via in the first direction. In some embodiments, the width of the second via in the first direction is substantially the same as a width of the first and second active regions in the first direction. In some embodiments, the IC device includes a conductive segment between and electrically connected to the first active region and the first via.

[0168] In some embodiments, a method of manufacturing an IC device includes forming a first gate structure extending in a first direction on a front side of a semiconductor wafer, forming first and second active regions adjacent to the first gate structure, forming a first conductive segment on the first active region, forming a first via on the first conductive segment, forming a first conductive line on the first via, forming a second via on one of the first active region or the second active region and extending toward a back side of the semiconductor wafer, and forming a first power rail on the second via on the back side of the semiconductor wafer, wherein a plane perpendicular to the first direction intersects each of the first conductive line, the first power rail, the first gate structure, and the first and second active regions. In some embodiments, forming the second via includes forming the second via on the first active region and aligned with the first via in the plane in a second direction perpendicular to the first direction. In some embodiments, forming the first gate structure includes forming a second gate structure extending in the first direction on the front side of the semiconductor wafer, forming the first and second active regions includes forming a third active region adjacent to the second gate structure, forming the first conductive segment on the first active region includes forming a second conductive segment on the third active region, forming the first via on the first conductive segment includes forming a third via on the second conductive segment, forming the second via on the first active region includes forming a fourth via on the third active region and extending toward the back side of the semiconductor wafer, and one of forming the first conductive line on the first via includes forming the first conductive line on the third via and forming the first power rail includes forming a second power rail on the fourth via on the back side of the semiconductor wafer, or forming the first conductive line on the first via includes forming a second conductive line on the third via and forming the first power rail includes forming the first power rail on the fourth via on the back side of the semiconductor wafer. In some embodiments, forming the first via includes forming the first via having a first width in the first direction and forming the second via includes forming the second via having a second width in the first direction greater than the first width. In some embodiments, forming the first active region includes forming the first active region having a first width in the first direction and forming the second via includes forming the second via having a second width in the first direction substantially the same as the first width.

[0169] In some embodiments, a method includes generating a first conductive line in a first front side layer of an IC layout diagram, generating a first power rail in a back side layer of the IC layout diagram, generating a first gate structure extending in a first direction in a second front side layer of the IC layout diagram between the first front side layer and the back side layer, generating, in the second front side layer, an active area including first and second active regions adjacent to the first

gate structure, generating a first via overlapping and electrically connected to the first active region and the first conductive line, generating a second via overlapping and electrically connected to the first power rail and either the first active region or the second active region, and storing the IC layout diagram including the first conductive line, the first power rail, the first gate structure, the active area, and the first and second vias in a storage medium, wherein a plane perpendicular to the first direction intersects each of the first conductive line, the first power rail, the first gate structure, and the first and second active regions. In some embodiments, generating the second via includes generating the second via overlapping and electrically connected to the second active region and generating the active area includes generating at least one channel region overlapping the first gate structure between the first and second active regions. In some embodiments, generating the second via includes generating the second via overlapping and electrically connected to the first active region, generating the first via includes generating a third via overlapping and electrically connected to the second active region and the first conductive line, and generating the second via includes generating a fourth via overlapping and electrically connected to the first power rail and the second active region. In some embodiments, generating the second via includes generating the second via overlapping and electrically connected to the first active region, generating the first gate structure includes generating a second gate structure extending in the first direction in the second front side layer, generating the active area includes generating the active area further comprising a third active region adjacent to the second gate structure, and one of generating the first power rail includes generating a second power rail in the back side layer, generating the first via includes generating a third via overlapping and electrically connected to the third active region and the first conductive line, and generating the second via includes generating a fourth via overlapping and electrically connected to the second power rail and the third active region, or generating the first conductive line includes generating a second conductive line in the first front side layer, generating the first via includes generating the third via overlapping and electrically connected to the third active region and the second conductive line, and generating the second via includes generating the fourth via overlapping and electrically connected to the first power rail and the third active region. In some embodiments, generating the first gate structure and the second gate structure includes positioning the first and second gate structures between the first active region and the third active region and configuring each of the first gate structure and the second gate structure either to float or to be coupled to a ground voltage connection.
[0170] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

Claims

1. An integrated circuit (IC) device comprising: a first conductive line on a front side of a semiconductor wafer; a first power rail on a back side of the semiconductor wafer; a first gate structure extending in a first direction on the front side of the semiconductor wafer; first and second active regions adjacent to the first gate structure; a first via between and electrically connected to the first active region and the first conductive line; and a second via between and electrically connected to the first power rail and either the first active region or the second active region, wherein a plane perpendicular to the first direction intersects each of the first conductive line, the first power rail, the first gate structure, and the first and second active regions.

2. The IC device of claim 1, wherein the second via is between and electrically connected to the first power rail and the second active region, and the IC device further comprises at least one channel region extending through the first gate structure between the first and second active regions.
3. The IC device of claim 1, wherein the second via is between and electrically connected to the first power rail and the first active region, and the IC device further comprises: a third via between and electrically connected to the second active region and the first conductive line; and a fourth via between and electrically connected to the first power rail and the second active region.
4. The IC device of claim 1, wherein the second via is between and electrically connected to the first power rail and the first active region, and the first active region and the first and second vias are aligned in the plane in a second direction perpendicular to the first direction.
5. The IC device of claim 4, further comprising: a second gate structure extending in the first direction on the front side of the semiconductor wafer; a third active region adjacent to the second gate structure; and third and fourth vias electrically connected to the third active region and aligned in the plane with the third active region in the second direction, wherein one of: the IC device further comprises a second power rail on the back side of the semiconductor wafer, the third via is between and electrically connected to the third active region and the first conductive line, and the fourth via is between and electrically connected to the third active region and the second power rail; or the IC device further comprises a second conductive line on the front side of the semiconductor wafer, the third via is between and electrically connected to the third active region and the second conductive line, and the fourth via is between and electrically connected to the third active region and the first power rail.
6. The IC device of claim 5, wherein the first gate structure and the second gate structure are between the first active region and the third active region, and each of the first gate structure and the second gate structure is coupled to a ground voltage connection.
7. The IC device of claim 5, wherein the first gate structure and the second gate structure are between the first active region and the third active region, and each of the first gate structure and the second gate structure is configured to float.
8. The IC device of claim 1, wherein the second via has a width in the first direction greater than a width of the first via in the first direction.
9. The IC device of claim 8, wherein the width of the second via in the first direction is substantially the same as a width of the first and second active regions in the first direction.
10. The IC device of claim 1, further comprising: a conductive segment between and electrically connected to the first active region and the first via.
11. A method of manufacturing an integrated circuit (IC) device, the method comprising: forming a first gate structure extending in a first direction on a front side of a semiconductor wafer; forming first and second active regions adjacent to the first gate structure; forming a first conductive segment on the first active region; forming a first via on the first conductive segment; forming a first conductive line on the first via; forming a second via on one of the first active region or the second active region and extending toward a back side of the semiconductor wafer; and forming a first power rail on the second via on the back side of the semiconductor wafer, wherein a plane perpendicular to the first direction intersects each of the first conductive line, the first power rail, the first gate structure, and the first and second active regions.
12. The method of claim 11, wherein the forming the second via comprises forming the second via on the first active region and aligned with the first via in the plane in a second direction perpendicular to the first direction.
13. The method of claim 12, wherein the forming the first gate structure comprises forming a second gate structure extending in the first direction on the front side of the semiconductor wafer; the forming the first and second active regions comprises forming a third active region adjacent to the second gate structure; the forming the first conductive segment on the first active region

comprises forming a second conductive segment on the third active region; the forming the first via on the first conductive segment comprises forming a third via on the second conductive segment, the forming the second via on the first active region comprises forming a fourth via on the third active region and extending toward the back side of the semiconductor wafer, and one of: the forming the first conductive line on the first via comprises forming the first conductive line on the third via, and the forming the first power rail comprises forming a second power rail on the fourth via on the back side of the semiconductor wafer; or the forming the first conductive line on the first via comprises forming a second conductive line on the third via, and the forming the first power rail comprises forming the first power rail on the fourth via on the back side of the semiconductor wafer.

14. The method of claim 11, wherein the forming the first via comprises forming the first via having a first width in the first direction, and the forming the second via comprises forming the second via having a second width in the first direction greater than the first width.

15. The method of claim 11, wherein the forming the first active region comprises forming the first active region having a first width in the first direction, and the forming the second via comprises forming the second via having a second width in the first direction substantially the same as the first width.

16. A method comprising: generating a first conductive line in a first front side layer of an integrated circuit (IC) layout diagram; generating a first power rail in a back side layer of the IC layout diagram; generating a first gate structure extending in a first direction in a second front side layer of the IC layout diagram between the first front side layer and the back side layer; generating, in the second front side layer, an active area comprising first and second active regions adjacent to the first gate structure; generating a first via overlapping and electrically connected to the first active region and the first conductive line; generating a second via overlapping and electrically connected to the first power rail and either the first active region or the second active region; and storing the IC layout diagram comprising the first conductive line, the first power rail, the first gate structure, the active area, and the first and second vias in a storage medium, wherein a plane perpendicular to the first direction intersects each of the first conductive line, the first power rail, the first gate structure, and the first and second active regions.

17. The method of claim 16, wherein the generating the second via comprises generating the second via overlapping and electrically connected to the second active region, and the generating the active area comprises generating at least one channel region overlapping the first gate structure between the first and second active regions.

18. The method of claim 16, wherein the generating the second via comprises generating the second via overlapping and electrically connected to the first active region, the generating the first via comprises generating a third via overlapping and electrically connected to the second active region and the first conductive line, and the generating the second via comprises generating a fourth via overlapping and electrically connected to the first power rail and the second active region.

19. The method of claim 16, wherein the generating the second via comprises generating the second via overlapping and electrically connected to the first active region, the generating the first gate structure comprises generating a second gate structure extending in the first direction in the second front side layer, the generating the active area comprises generating the active area further comprising a third active region adjacent to the second gate structure, and one of: the generating the first power rail comprises generating a second power rail in the back side layer, the generating the first via comprises generating a third via overlapping and electrically connected to the third active region and the first conductive line, and the generating the second via comprises generating a fourth via overlapping and electrically connected to the second power rail and the third active region; or the generating the first conductive line comprises generating a second conductive line in the first front side layer, the generating the first via comprises generating the third via overlapping and electrically connected to the third active region and the second conductive line, and the generating the second via comprises generating the fourth via overlapping and electrically connected to the first power rail and the third active region.

20. The method of claim 19, wherein the generating the first gate structure and the second gate structure comprises: positioning the first and second gate structures between the first active region and the third active region, and configuring each of the first gate structure and the second gate structure either to float or to be coupled to a ground voltage connection.