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Inventor(s) KIM; KEEWON et al.

IMAGE SENSOR AND METHOD OF FABRICATING THE SAME

Abstract

An image sensor includes a substrate having first and second surfaces opposite to each other, an antireflection structure on the second surface, a substrate isolation part separating the substrate, and a backside contact in a backside contact trench that penetrates the antireflection structure. The backside contact includes a contact conductive pattern on a sidewall of the backside contact trench, and a contact metal pattern on the contact conductive pattern. The antireflection structure includes a first dielectric layer, a high-refractive layer on the first dielectric layer, and a contact break between the high-refractive layer and the backside contact.

Inventors: **KIM; KEEWON (Suwon-si, KR), Yoon; Ki Joong (Suwon-si, KR), Jeon; Jongmin (Suwon-si, KR), Hur; Jaesung (Suwon-si, KR)**

Applicant: **SAMSUNG ELECTRONICS CO., LTD.** (Suwon-si, KR)

Family ID: **1000008419014**

Assignee: **SAMSUNG ELECTRONICS CO., LTD. (Suwon-si, KR)**

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This U.S. nonprovisional application claims priority under 35 U.S.C § 119 to Korean Patent Application No. 10-2024-0024374 filed on Feb. 20, 2024 in the Korean Intellectual Property Office, the disclosure of which is herein incorporated by reference in its entirety.

BACKGROUND

[0002] One or more example embodiments of the disclosure relate to an image sensor and a method of fabricating the same, and more particularly, to a complementary metal oxide semiconductor (CMOS) image sensor and a method of fabricating the same.

[0003] An image sensor is a semiconductor device to transform optical images into electrical signals. Recent advances in computer and communication industries have led to strong demands in high performance image sensors in various consumer electronic devices such as digital cameras, camcorders, PCSs (Personal Communication Systems), game devices, security cameras, medical micro-cameras, etc.

[0004] As semiconductor devices become highly integrated, image sensors may also be highly integrated. Thus, the size of individual pixels may also be reduced. Accordingly, there is a need for an image sensor with reduced crosstalk and increased sensitivity in a fine area.

[0005] In an image sensor in which a high-refractive material is applied to a bottom antireflective layer (BARL), there is a need for a reduction in leakage current from adjacent wiring lines.

SUMMARY

[0006] Some embodiments of the disclosure provide an image sensor advantageous to pixel miniaturization and a method of fabricating the same.

[0007] Some embodiments of the disclosure provide an image sensor with increased sensitivity and a method of fabricating the same.

[0008] Some embodiments of the disclosure provide an image sensor favorable for high integration and a method of fabricating the same.

[0009] According to some embodiments of the disclosure, an image sensor may comprise: a substrate that has a first surface and a second surface that are opposite to each other, the substrate including a pixel array area and an edge area; an antireflection structure on the second surface; a substrate isolation part in the substrate, the substrate isolation part separating the substrate; a microlens on the antireflection structure; and a backside contact in a backside contact trench, the backside contact trench penetrating the antireflection structure, the backside contact being in contact with the substrate isolation part. The backside contact may include: a contact conductive pattern on a sidewall of the backside contact trench; and a contact metal pattern on the contact conductive pattern. The antireflection structure may include: a first dielectric layer; a high-refractive layer on the first dielectric layer; and a contact break between the high-refractive layer and the backside contact.

[0010] According to some embodiments of the disclosure, an image sensor may comprise: a substrate that has a first surface and a second surface that are opposite to each other, the substrate including a pixel array area and an edge area; an antireflection structure on the second surface; a microlens on the antireflection structure; a first backside via pattern that penetrates the antireflection structure and the substrate on the edge area; a first interlayer dielectric layer on the first surface of the substrate; a first interlayer wiring line in the first interlayer dielectric layer; a second interlayer dielectric layer on or below the first interlayer dielectric layer; and a second interlayer wiring line in the second interlayer dielectric layer. The antireflection structure may

include: a first dielectric layer; a high-refractive layer on the first dielectric layer; and a first via break between the high-refractive layer and the first backside via pattern.
[0011] According to some embodiments of the disclosure, an image sensor may comprise: a substrate that has a first surface and a second surface that are opposite to each other, the substrate including a pixel array area and an edge area; a transfer gate on the first surface; an antireflection structure on the second surface; a substrate isolation part in the substrate, the substrate isolation part separating the substrate; a microlens on the antireflection structure; and a backside contact in a backside contact trench, the backside contact trench penetrating the antireflection structure, the backside contact being in contact with the substrate isolation part. The backside contact may include: a contact conductive pattern on a sidewall of the backside contact trench; and a contact metal pattern on the contact conductive pattern. The antireflection structure may include: a first dielectric layer; a high-refractive layer on the first dielectric layer; and a contact break between the high-refractive layer and the backside contact. The backside contact may include a contact protrusion that protrudes toward the contact break.

Description

BRIEF DESCRIPTION OF DRAWINGS
[0012] Example embodiments will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings.
[0013] FIG. **1** illustrates a simplified block diagram showing an image sensor according to some embodiments of the disclosure.
[0014] FIG. **2** illustrates a circuit diagram showing an active pixel sensor array of an image sensor according to some embodiments of the disclosure.
[0015] FIG. **3** illustrates a plan view showing an image sensor according to some embodiments of the disclosure.
[0016] FIG. **4** illustrates a cross-sectional view taken along line A-A′ of FIG. **3**.
[0017] FIG. **5** illustrates an enlarged view showing section X of FIG. **4**.
[0018] FIG. **6** illustrates an enlarged plan view showing section Y of FIG. **4**.
[0019] FIG. **7**A illustrates an enlarged cross-sectional view of section X of FIG. **4**, showing an image sensor according to some embodiments of the disclosure.
[0020] FIG. **7**B illustrates an enlarged cross-sectional view of section Y of FIG. **4**, showing an image sensor according to some embodiments of the disclosure.
[0021] FIGS. **8** to **13**C illustrate cross-sectional views corresponding to line A-A′ of FIG. **3** and sections X and Y of FIG. **4**, showing a method of fabricating an image sensor according to some embodiments of the disclosure.
DETAILED DESCRIPTION
[0022] The following will now describe in detail some example embodiments of the disclosure with reference to the accompanying drawings.
[0023] FIG. **1** illustrates a simplified block diagram showing an image sensor according to some embodiments of the disclosure.
[0024] Referring to FIG. **1**, an image sensor may include an active pixel sensor array **1001**, a row decoder **1002**, a row driver **1003**, a column decoder **1004**, a timing generator **1005**, a correlated double sampler (CDS) **1006**, an analog-to-digital converter (ADC) **1007**, and an input/output buffer **1008**.
[0025] The active pixel sensor array **1001** may include a plurality of two-dimensionally arranged unit pixels, each of which is configured to convert optical signals into electrical signals. The active pixel sensor array **1001** may be driven by a plurality of driving signals such as a pixel selection signal, a reset signal, and a charge transfer signal from the row driver **1003**. The correlated double

sampler **1006** may be provided with the converted electrical signals.
[0026] The row driver **1003** may provide the active pixel sensor array **1001** with several driving signals for driving several unit pixels in accordance with a decoded result obtained from the row decoder **1002**. When the unit pixels are arranged in a matrix shape, the driving signals may be provided for each row.
[0027] The timing generator **1005** may provide timing and control signals to the row decoder **1002** and the column decoder **1004**.
[0028] The correlated double sampler **1006** may receive the electrical signals generated from the active pixel sensor array **1001**, and may hold and sample the received electrical signals. The correlated double sampler **1006** may perform a double sampling operation to sample a specific noise level and a signal level of the electrical signal, and then may output a difference level corresponding to a difference between the noise and signal levels.
[0029] The analog-to-digital converter **1007** may convert analog signals, which correspond to the difference level received from the correlated double sampler **1006**, into digital signals, and then output the converted digital signals.
[0030] The input/output buffer **1008** may latch the digital signals and then sequentially output the latched digital signals to an image signal processing unit (not shown) in response to the decoded result obtained from the column decoder **1004**.
[0031] FIG. **2** illustrates a circuit diagram showing an active pixel sensor array of an image sensor according to some embodiments of the disclosure.
[0032] Referring to FIGS. **1** and **2**, the active pixel sensor array **1001** may include a plurality of pixel regions PX, and the plurality of pixel regions PX may be arranged in a matrix shape. Each pixel region PX may include a transfer transistor TX. Each pixel region PX may further include logic transistors RX, SX, and DX. The logic transistors RX, SX, and DX may include a reset transistor RX, a selection transistor SX, and a source follower transistor DX. The transfer transistor TX may include a transfer gate TG. Each of the pixel regions PX may further include a photoelectric conversion element PD and a floating diffusion region FD. The logic transistors RX, SX, and DX may be shared by a plurality of pixel regions PX.
[0033] The photoelectric conversion element PD may create and accumulate photo- charges in proportion to an amount of externally incident light. The photoelectric conversion element PD may include a photodiode, a phototransistor, a photogate, a pinned photodiode, or any combination thereof. The transfer transistor TX may transfer charges generated in the photoelectric conversion element PD into the floating diffusion region FD. The floating diffusion region FD may accumulate and store charges that are generated and transferred from the photoelectric conversion element PD. The source follower transistor DX may be controlled by an amount of photo-charges accumulated in the floating diffusion region FD.
[0034] The reset transistor RX may periodically reset the charges accumulated in the floating diffusion region FD. The reset transistor RX may have a drain electrode electrically connected to the floating diffusion region FD and a source electrode electrically connected to a power voltage V.sub.DD. When the reset transistor RX is turned on, the floating diffusion region FD may be supplied with the power voltage V.sub.DD electrically connected to the source electrode of the reset transistor RX. Accordingly, when the reset transistor RX is turned on, the charges accumulated in the floating diffusion region FD may be exhausted and thus the floating diffusion region FD may be reset.
[0035] The source follower transistor DX including a source follower gate SF may serve as a source follower buffer amplifier. The source follower transistor DX may amplify a variation in electrical potential of the floating diffusion region FD and may output the amplified electrical potential to an output line V.sub.OUT.
[0036] The selection transistor SX including a selection gate SEL may select each row of the pixel region PX to be readout. When the selection transistor SX is turned on, the power voltage

V.sub.DD may be applied to a drain electrode of the source follower transistor DX.
[0037] FIG. **3** illustrates a plan view showing an image sensor according to some embodiments of the disclosure. FIG. **4** illustrates a cross-sectional view taken along line A-A′ of FIG. **3**. FIG. **5** illustrates an enlarged view showing section X of FIG. **4**. FIG. **6** illustrates an enlarged cross-sectional view showing section Y of FIG. **4**.
[0038] Referring to FIGS. **3** and **4**, an image sensor **500** according to some embodiments of the disclosure may have a structure in which first and second sub-chips CH**1** and CH**2** are bonded to each other. The first sub-chip CH**1** may be disposed on the second sub-chip CH**2**. The first sub-chip CHI may include a substrate **100**. The substrate **100** may be, for example, a single-crystalline silicon wafer, a silicon epitaxial layer, or a silicon-on-insulator (SOI) substrate. The substrate **100** may be doped with impurities having a first conductivity type. For example, the first conductivity type may be a p-type.
[0039] The substrate **100** may have a first surface **100***a* and a second surface **100***b* that are opposite to each other. The first surface **100***a* may face a second direction D**2**, and the second surface **100***b* may face a first direction D**1**. The first direction D**1** and the second direction D**2** may be opposite to each other. The substrate **100** may include a pixel array area APS, an optical black area OB, and an edge area ER.
[0040] The pixel array area APS and the optical black area OB may each include a plurality of unit pixels UP. The unit pixels UP may be arranged along a third direction D**3** and a fourth direction D**4**. The optical black area OB may surround the pixel array area APS. The edge area ER may surround the pixel array area APS and the optical black area OB. The edge area ER may include a contact region BR**1**, a via region BR**2**, and a pad region PR. The via region BR**2** may be positioned between the contact region BR**1** and the pad region PR. The pad region PR may be positioned on an outermost section of the edge area ER.
[0041] On the pixel array area APS and the optical black area OB, the substrate **100** may be provided therein with a substrate isolation part DTI that separates and/or limits the unit pixels UP on the pixel array area APS and separates and/or limits regions of the substrate **100** on the optical black area OB. The substrate isolation part DTI may extend to the contact region BR**1** of the edge area ER. The substrate isolation part DTI may have a mesh shape when viewed in plan.
[0042] On the edge area ER, the substrate **100** may be provided on its second surface **100***b* with backside contacts BCA, backside via patterns BVS**1** and BVS**2**, and backside conductive pads PAD. The backside via patterns BVS**1** and BVS**2** may include a first backside via pattern BVS**1** and a second backside via pattern BVS**2**. One or more of column and row signals may be transmitted between the first and second sub-chips CH**1** and CH through the backside via patterns BVS**1** and BVS**2**.
[0043] The substrate isolation part DTI may be positioned in the substrate **100**. The substrate isolation part DTI may separate the unit pixels UP from each other. The substrate isolation part DTI may penetrate in the second direction D**2** through the substrate **100** between the unit pixels UP.
[0044] The substrate isolation part DTI may penetrate only a portion of the substrate **100**. In this case, the substrate **100** may include a region aligned with the substrate isolation part DTI and doped opposite to a photoelectric conversion element PD which will be discussed below, thereby defining a pixel.
[0045] The substrate isolation part DTI may extend from the first surface **100***a* toward the second surface **100***b*. When viewed in plan, the substrate isolation part DTI may have a mesh shape in which lines extending in the third and fourth directions D**3** and D**4** intersect each other. The substrate isolation parts DTI may have a width that decreases in a direction from the first surface **100***a* toward the second surface **100***b* of the substrate **100**.
[0046] The substrate isolation part DTI may extend from the second surface **100***b* toward the first surface **100***a*. The substrate isolation part DTI may have a width that decreases in a direction from the second surface **100***b* toward the first surface **100***a* of the substrate **100**.

[0047] The substrate isolation part DTI may include a buried dielectric pattern **115**, an isolation dielectric pattern **111**, and an isolation conductive pattern **113**. The buried dielectric pattern **115** may be interposed between the isolation conductive pattern **113** and a first interlayer dielectric layer ILD**1** which will be discussed below. The isolation dielectric pattern **111** may be interposed between the isolation conductive pattern **113** and the substrate **100** and between the buried dielectric pattern **115** and the substrate **100**.
[0048] The buried dielectric pattern **115** and the isolation dielectric pattern **111** may be formed of a dielectric material whose refractive index is different from that of the substrate **100**. The buried dielectric pattern **115** and the isolation dielectric pattern **111** may include, for example, silicon oxide. The isolation conductive pattern **113** may be spaced apart from the substrate **100**. The isolation conductive pattern **113** may include an impurity-doped polysilicon layer or a silicon-germanium layer. For example, one of boron, phosphorus, and arsenic may be chosen as impurities doped into the polysilicon layer or the silicon-germanium layer. Alternatively, the isolation conductive pattern **113** may include a metal layer.
[0049] A shallow device isolation pattern STI may be positioned in the substrate **100**. The shallow device isolation pattern STI may extend from the first surface **100***a* into the substrate **100**, and may be disposed in a corresponding one of a plurality of unit pixels UP. The shallow device isolation pattern STI may limit active sections adjacent to the first surface **100***a* of the substrate **100** on the pixel array area APS. The active sections may be provided for the transistors TX, RX, DX, and SX of FIG. **2**.
[0050] The unit pixels UP may correspondingly include photoelectric conversion elements PD in the substrate **100**. The photoelectric conversion elements PD may be doped with impurities having a second conductivity type opposite to the first conductivity type. The second conductivity type may be, for example, an n-type. The n-type impurities doped in the photoelectric conversion element PD and the p-type impurities doped in the substrate **100** therearound may constitute a PN junction to provide a photodiode.
[0051] Referring to FIG. **4**, on the unit pixel UP, a transfer gate TG may be disposed on the first surface **100***a* of the substrate **100**. A portion of the transfer gate TG may extend into the substrate **100**. The transfer gate TG may have a vertical type. Alternatively, the transfer gate TG may be a planar type that does not extend into the substrate **100**. A gate dielectric layer GI may be interposed between the transfer gate TG and the substrate **100**. A floating diffusion region FD may be disposed in the substrate **100** on one side of the transfer gate TG. The floating diffusion region FD may be doped with impurities having, for example, the second conductivity type.
[0052] A first unit pixel UP**1** and a second unit pixel UP**2** may be disposed on the optical black area OB of the substrate **100**. On the first unit pixel UP**1**, a black photoelectric conversion element PD′ may be provided in the substrate **100**. On the second unit pixel UP**2**, a dummy element PD″ may be provided in the substrate **100**. The black photoelectric conversion element PD′ may be doped with impurities having, for example, the second conductivity type different from the first conductivity type. The second conductivity type may be, for example, an n-type. The black photoelectric conversion element PD′ may have a similar structure to that of the photoelectric conversion element PD, but may not perform the same operation (e.g., conversion of light into electrical signals) as that of the photoelectric conversion element PD. A signal generated from the black photoelectric conversion element PD′ may be used to produce a dark level reference signal. The dummy element PD″ may not be doped with impurities. A signal generated from the dummy element PD″ may be used as information to remove subsequent process noise.
[0053] The substrate **100** may be provided on its first surface **100***a* with a first interlayer dielectric layer ILD**1** and first interlayer wiring lines MCL.
[0054] The first interlayer dielectric layer ILD**1** may be provided on and cover the first surface **100***a* of the substrate **100**. The first interlayer dielectric layer ILD**1** may be a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, a porous low-dielectric layer, or a composite layer

including at least one of any combination thereof. The first interlayer wiring lines MCL may be provided in the first interlayer dielectric layer ILD**1**. The floating diffusion region FD may be electrically connected to the first interlayer wiring lines MCL.

[0055] A second interlayer dielectric layer ILD**2** may be provided on or underneath the first interlayer dielectric layer ILD**1**. Second interlayer wiring lines **217** may be provided in the second interlayer dielectric layer ILD**2**. The second interlayer dielectric layer ILD**2** may be provided with peripheral transistors PTR therein.

[0056] A sub-substrate BSB may be provided on or underneath the second interlayer dielectric layer ILD**2**. The sub-substrate BSB may be provided therein with circuits that constitute blocks other than the active pixel sensor array **1001** of FIG. **1**.

[0057] An antireflection structure AL may be provided on the second surface **100***b* of the substrate **100**. The antireflection structure AL may cover the second surface **100***b*.

[0058] Light-shield patterns **48** may be disposed on the antireflection structure AL. Low-refractive patterns **50** may be correspondingly disposed on the light-shield patterns **48**. The light-shield pattern **48** and the low-refractive pattern **50** may overlap the substrate isolation part DTI and have a grid shape when viewed in plan. The light-shield pattern **48** may include, for example, titanium. The low-refractive patterns **50** may have the same thickness and include the same organic material. The low-refractive patterns **50** may have a refractive index less than that of color filters CF**1** and CF**2** which will be discussed below. The light-shield pattern **48** and the low-refractive pattern **50** may prevent crosstalk between neighboring unit pixels UP.

[0059] A protection layer **56** may be provided on the low-refractive pattern **50**. The protection layer **56** may conformally cover the low-refractive pattern **50**.

[0060] On the pixel array area APS, color filters CF**1** and CF**2** may be disposed between the low-refractive patterns **50**. The color filters CF**1** and CF**2** may each have one of blue, green, and red colors. Alternatively, the color filters CF**1** and CF**2** may have different colors such as cyan, magenta, or yellow. In an image sensor according to the present embodiment, the color filters CF**1** and CF**2** may be arranged in Bayer pattern. Alternatively, the color filters CF**1** and CF**2** may be arranged in one of 2×2 Tetra pattern, 3×3 Nona pattern, and 4×4 Hexadeca pattern.

[0061] On the pixel array area APS, microlenses ML may be disposed on the color filters CF**1** and CF**2**. The microlenses ML may have edges in contact with and connected to each other.

[0062] On the optical black area OB, an optical black liner **52***p* may be disposed. The optical black liner **52***p* may include a conductive material. The optical black liner **52***p* may have a single-layered or multi-layered structure including at least one selected from a titanium layer, a titanium nitride layer, and a tungsten layer.

[0063] On the edge area ER, an optical black pattern CFB may be provided. The optical black pattern CFB may include, for example, the same material as that of a blue color filter.

[0064] On the edge area ER, a lens residual layer MLR may be disposed on the optical black pattern CFB. The lens residual layer MLR may include the same material as that of the microlenses ML. On the pad region PR, the lens residual layer MLR may have an opening **35** that exposes the backside conductive pad PAD.

[0065] The antireflection structure AL may include a first dielectric layer **31**, a high-refractive layer **32** on the first dielectric layer **31**, a second dielectric layer **33** on the high-refractive layer **32**, a third dielectric layer **34** on the second dielectric layer **33**, a contact break VC**1** between the high-refractive layer **32** and the backside contact BCA, a first via break VC**2** between the high-refractive layer **32** and the first backside via pattern BVS**1**, a pad break VC**3** between the backside conductive pad PAD and the high-refractive layer **32**, and a second via break VC**4** between the second backside via pattern BVS**2** and the high-refractive layer **32**. The first, second, and third dielectric layers **31**, **33**, and **34** may include different materials from each other.

[0066] The first dielectric layer **31** may be in contact with the second surface **100***b* of the substrate **100**. The first dielectric layer **31** may include, for example, aluminum oxide. The second dielectric

layer **33** may include, for example, silicon, silicon oxide, or plasma enhanced silicon oxide (PEOX). The third dielectric layer **34** may include, for example, hafnium oxide. The third dielectric layer **34** may serve as an etch stop layer.

[0067] The high-refractive layer **32** may include titanium oxide. For example, the high-refractive layer **32** may include TiO.sub.2.

[0068] The substrate **100** may have a substrate refractive index (n0), the first dielectric layer **31** may have a first refractive index (n1), the high-refractive layer **32** may have a second refractive index (n2), and the second dielectric layer **33** may have a third refractive index (n3).

[0069] The substrate refractive index (n0) may be greater than the first refractive index (n1). The second refractive index (n2) of the high-refractive layer **32** may be greater than the third refractive index (n3) of the second dielectric layer **33**.

[0070] The substrate refractive index (n) may range, for example, from about 4.0 to about 4.4. The first refractive index (n1) may range from about 2.0 to about 3.0. The second refractive index (n2) may range from about 2.2 to about 2.8. The third refractive index (n3) may range from about 1.0 to about 1.9. As used herein, the term “about” will be understood as referring to an approximate range of a numerical value by a person of ordinary skill in the art and will vary in some extent depending on the context in which it is used. For example, “about” may mean plus or minus a certain percentage (e.g., 10% or less) of a particular range or value. However, these are merely examples and the disclosure is not limited thereto.

[0071] On the contact region BR**1**, the backside contact BCA may be disposed in a backside contact trench **46** that penetrates the antireflection structure AL and a portion of the substrate **100**. The backside contact BCA may be in contact with the substrate isolation part DTI. The backside contact BCA may include a contact conductive pattern **52**A on a sidewall of the backside contact trench **46** and a contact metal pattern **54**A on the contact conductive pattern **52**A.

[0072] The contact conductive pattern **52**A may conformally cover an inner wall of the backside contact trench **46**. The contact conductive pattern **52**A may be in contact with the first dielectric layer **31**, the second dielectric layer **33**, and the third dielectric layer **34**. The contact conductive pattern **52**A may be spaced apart from the high-refractive layer **32**.

[0073] The contact metal pattern **54**A may fill the backside contact trench **46**. The contact metal pattern **54**A may include, for example, aluminum.

[0074] The backside contact BCA may be in contact with the isolation conductive pattern **113** of the substrate isolation part DTI. A negative bias may be applied through the backside contact BCA to the isolation conductive pattern **113** of the substrate isolation part DTI. The isolation conductive pattern **113** may serve as a common bias line. Therefore, holes possibly present on a surface of the substrate **100** in contact with the substrate isolation part DTI may be trapped to improve dark current properties.

[0075] The contact break VC**1** may be provided between the contact conductive pattern **52**A and the high-refractive layer **32**.

[0076] In an embodiment, the contact break VC**1** may have a configuration in which an empty space is provided therein. The contact break VC**1** may form an empty space therein. The contact break VC**1** may include an empty space therein.

[0077] In an embodiment, the contact break VC**1** may include a dielectric material. For example, the contact break VC**1** may include SiO.sub.2 or Al.sub.2O.sub.3.

[0078] Referring to FIG. **5**, the contact break VC**1** and the backside contact BCA will be illustrated in detail.

[0079] The contact conductive pattern **52**A of the backside contact BCA may include a first contact conductive pattern **521**A in contact with an inner wall of the backside contact trench **46**, and may also include a second contact conductive pattern **522**A on the first contact conductive pattern **521**A. The first contact conductive pattern **521**A may be in contact with the first dielectric layer **31**, the second dielectric layer **33**, and the third dielectric layer **34**. The first contact conductive pattern

521A may be in direct contact with the substrate isolation part DTI. The second contact conductive pattern **522**A may be in contact with the contact metal pattern **54**A. The second contact conductive pattern **522**A may be in contact with the protection layer **56**.

[0080] The first contact conductive pattern **521**A and the second contact conductive pattern **522**A may include different materials from each other. The first contact conductive pattern **521**A may include, for example, titanium or titanium nitride. The second contact conductive pattern **522**A may include, for example, tungsten.

[0081] The first contact conductive pattern **521**A may be spaced apart from the high-refractive layer **32**. The contact break VC**1** may be provided between the first contact conductive pattern **521**A and the high-refractive layer **32**.

[0082] When the contact break VC**1** includes an empty space therein, one sidewall **32**SS of the high-refractive layer **32** may be exposed.

[0083] The contact break VC**1** may be surrounded by the high-refractive layer **32**, the second dielectric layer **33**, the first dielectric layer **31**, and the first contact conductive pattern **521**A. The second dielectric layer may be continuously interposed between the backside contact BCA and the first backside via pattern BVS**1**.

[0084] Referring back to FIG. **4**, on the via region BR**2**, the first backside via patterns BVS**1** may be disposed on the second surface **100***b* of the substrate **100**. On the pad region PR, the backside conductive pads PAD and the second backside via patterns BVS**2** may be disposed on the second surface **100***b* of the substrate **100**. Several of the second backside via patterns BVS**2** may form a group, and a plurality of groups may be disposed around corresponding backside conductive pads PAD. An external signal may be input and/or output through the backside conductive pads PAD. The backside conductive pads PAD may become interfaces of external signals.

[0085] The backside conductive pad PAD may be disposed in a backside pad trench **60**. The backside conductive pad PAD may include a pad conductive pattern **52**C and a pad metal pattern **54**C. The pad conductive pattern **52**C may conformally cover a lateral surface and a bottom surface of the backside pad trench **60**.

[0086] The pad conductive pattern **52**C may include the same material as that of the contact conductive pattern **52**A and have the same thickness as that of the contact conductive pattern **52**A. The pad conductive pattern **52**C may have a single-layered or multi-layered structure of at least one selected from a titanium layer, a titanium nitride layer, and a tungsten layer. The pad metal pattern **54**C may include, for example, aluminum. The pad metal pattern **54**C may fill the backside pad trench **60**.

[0087] The pad break VC**3** may be provided between the pad conductive pattern **52**C and the high-refractive layer **32**. The pad break VC**3** may be similar to the contact break VC**1**. The pad break VC**3** may include an empty space therein or include a dielectric material such as SiO.sub.2 or Al.sub.2O.sub.3. The pad break VC**3** may separate the pad conductive pattern **52**C and the high-refractive layer **32** from each other.

[0088] The first via break VC**2** may be provided between the first backside via pattern BVS**1** and the high-refractive layer **32**. The first via break VC**2** may be similar to the contact break VC**1**. The first via break VC**2** may include an empty space therein or include a dielectric material such as SiO.sub.2 or Al.sub.2O.sub.3. The first via break VC**2** may separate the first backside via pattern BVS**1** and the high-refractive layer **32** from each other.

[0089] The second via break VC**4** may be provided between the second backside via pattern BVS**2** and the high-refractive layer **32**. The second via break VC**4** may be similar to the contact break VC**1**. The second via break VC**4** may include an empty space therein or include a dielectric material such as SiO.sub.2 or Al.sub.2O.sub.3. The second via break VC**4** may separate the second backside via pattern BVS**2** and the high-refractive layer **32** from each other.

[0090] The backside contact BCA and the first backside via pattern BVS**1** may be electrically connected through a connection conductive pattern **52**B.

[0091] The first backside via pattern BVS**1** may be provided on the second surface **100***b* of the substrate **100**. The first backside via pattern BVS**1** may be disposed in a first backside via hole H**1** that penetrates the antireflection structure AL and a portion of the substrate **100**. The first backside via pattern BVS**1** may conformally cover a sidewall of the first backside via hole H**1**.
[0092] The first backside via pattern BVS**1** may be in contact with the first dielectric layer **31**, the second dielectric layer **33**, and the third dielectric layer **34**. The first backside via pattern BVS**1** may be spaced apart from the high-refractive layer **32**.
[0093] A first low-refractive protection pattern **51**B may be disposed on the first backside via pattern BVS**1**. The first low-refractive protection pattern **51**B may have a refractive index less than that of the color filters CF**1** and CF**2**. For example, the first low-refractive protection pattern **51**B may have a refractive index equal to or less than about 1.3.
[0094] Although not shown, a low-refractive capping pattern (not shown) may be disposed on the first low-refractive protection pattern **51**B. In this case, the first low-refractive protection pattern **51**B may have a concave top surface.
[0095] The first backside via pattern BVS**1** and the contact conductive pattern **52**A may be electrically connected through the connection conductive pattern **52**B. The connection conductive pattern **52**B may be disposed on the third dielectric layer **34**, and may be placed between the first backside via pattern BVS**1** and the contact conductive pattern **52**A. The first backside via pattern BVS**1**, the connection conductive pattern **52**B, and the contact conductive pattern **52**A may be continuous. The first backside via pattern BVS**1** may electrically connect the first interlayer wiring lines MCL to the second interlayer wiring lines **217**.
[0096] The first backside via pattern BVS**1** may include a stepwise part STP. On the stepwise part STP, the first backside via pattern BVS**1** may be electrically connected to the first interlayer wiring lines MCL. A bottommost surface of the first backside via pattern BVS**1** may be electrically connected to the second interlayer wiring lines **217**.
[0097] The second backside via pattern BVS**2** may be disposed in a second backside via hole H**2** that penetrates the antireflection structure AL and a portion of the substrate **100**. The second backside via pattern BVS**2** may penetrate the antireflection structure AL, the substrate **100**, the first interlayer dielectric layer ILD**1**, and a portion of the second interlayer dielectric layer ILD**2**. The second backside via pattern BVS**2** may be electrically connected to portions of the second interlayer wiring lines **217**. Although not shown, the second backside via pattern BVS**2** may be electrically connected to portions of the first interlayer wiring lines MCL. The second backside via pattern BVS**2** may conformally cover an inner wall and a bottom surface of the second backside via hole H**2**. The second backside via pattern BVS**2** may include the same material as that of the contact conductive pattern **52**A and have the same thickness as that of the contact conductive pattern **52**A. The second backside via pattern BVS**2** may have a single-layered or multi-layered structure of at least one selected from a titanium layer, a titanium nitride layer, and a tungsten layer. One of the second backside via patterns BVS**2** may be electrically connected through one of via connection lines **52**D to one of the backside conductive pads PAD.
[0098] Referring to FIG. **6**, the first backside via pattern BVS**1** will be illustrated in detail. The first backside via pattern BVS**1** may include a first outer via pattern BVS**11** that conformally covers an inner wall of the first backside via hole H**1**, and may also include a first inner via pattern BVS**12** on the first outer via pattern BVS**11**.
[0099] The connection conductive pattern **52**B may include a first connection conductive pattern **521**B connected to the first outer via pattern BVS**11**, and may also include a second connection conductive pattern **522**B electrically connected to the first inner via pattern BVS**12**.
[0100] The first connection conductive pattern **521**B may include the same material as that of the first outer via pattern BVS**11** and that of the first contact conductive pattern **521**A. The first connection conductive pattern **521**B may include, for example, titanium or titanium nitride.
[0101] The second connection conductive pattern **522**B may include the same material as that of

the first inner via pattern BVS**12** and that of the second contact conductive pattern **522**A. The second connection conductive pattern **522**B may include, for example, tungsten.
[0102] The first outer via pattern BVS**11** may be in direct contact with the first interlayer wiring lines MCL and the second interlayer wiring lines **217**. The first outer via pattern BVS**11** may electrically connect the first interlayer wiring lines MCL to the second interlayer wiring lines **217**.
[0103] The first via break VC**2** may be provided between the first outer via pattern BVS**11** and the high-refractive layer **32**. The first via break VC**2** may separate the first outer via pattern BVS**11** and the high-refractive layer **32** from each other.
[0104] As discussed above, the high-refractive layer **32** may be spaced apart from the backside contact BCA, the first backside via pattern BVS**11**, the backside conductive pad PAD, and the second backside via pattern BVS**2**.
[0105] An empty internal space or an insulating material may be included in the contact break VC**1** between the high-refractive layer **32** and the backside contact BCA, the first via break VC**2** between the high-refractive layer **32** and the first backside via pattern BVS**1**, the pad break VC**3** between the high-refractive layer **32** and the backside conductive pad PAD, and the second via break VC**4** between the high-refractive layer **32** and the second backside via pattern BVS**2**, and thus an electrical short structure may be formed between the high-refractive layer **32** and each of the backside contact BCA, the backside conductive pad PAD, and the first backside via pattern BVS**1**, and the second backside via pattern BVS**2**. Accordingly, an image sensor may have improved optical performance.
[0106] FIG. **7**A illustrates an enlarged cross-sectional view of section X of FIG. **4**, showing an image sensor according to some embodiments of the disclosure. FIG. **7**B illustrates an enlarged cross-sectional view of section Y of FIG. **4**, showing an image sensor according to some embodiments of the disclosure. For brevity of description, a repetitive explanation will be omitted.
[0107] Referring to FIGS. **7**A and **7**B, there will be described in detail enlarged cross-sections showing sections X and Y of the image sensor depicted in FIG. **4**.
[0108] Referring to FIG. **7**A, the contact conductive pattern **52**A of the backside contact BCA may include a contact protrusion **52**APS that protrudes toward the high-refractive layer **32**. The contact metal pattern **54**A of the backside contact BCA may include a protrusion that protrudes toward the high-refractive layer **32**. The contact break VC**1** may have a contact break lateral surface VC**1**S where the contact break VC**1** meets the contact conductive pattern **52**A, and the contact break lateral surface VC**1**S may include a curved surface.
[0109] The contact conductive pattern **52**A may include a first contact conductive pattern **521**A in contact with the inner wall of the backside contact trench **46**, and may also include a second contact conductive pattern **522**A on the first contact conductive pattern **521**A.
[0110] As the contact metal pattern **54**A has a sidewall whose portion protrudes toward the high-refractive layer **32**, a lateral surface of the contact metal pattern **54**A may include a contact metal curved surface **54**ACS.
[0111] As the first contact conductive pattern **521**A has a sidewall whose portion protrudes toward the high-refractive layer **32**, a lateral surface of the first contact conductive pattern **521**A may include a first contact conductive lateral surface **521**ACS that is curved. The first contact conductive lateral surface **521**ACS may be in direct contact with the contact break VC**1**. When the contact break VC**1** includes an empty space therein, the first contact conductive lateral surface **521**ACS may be exposed.
[0112] As the second contact conductive pattern **522**A has a sidewall whose portion protrudes toward the high-refractive layer **32**, a lateral surface of the second contact conductive pattern **522**A may include a second contact conductive lateral surface **522**ACS that is curved. The second contact conductive lateral surface **522**ACS may be in contact with the first contact conductive pattern **521**A.
[0113] Referring to FIG. **7**B, the first backside via pattern BVS**1** may include a first via protrusion

52BPS that protrudes toward the high-refractive layer **32**.
[0114] The first outer via pattern BVS**11** of the first backside via pattern BVS**1** may include a protrusion that protrudes toward the high-refractive layer **32**. The first via break VC**2** may have a first via break lateral surface VC**2**S where the first via break VC**2** meets the first backside via pattern BVS**1**, and the first via lateral surface VC**2**S may include a curved surface.
[0115] The first backside via pattern BVS**1** may include the first outer via pattern BVS**11** that conformally covers an inner wall of the first backside via hole H**1**, and may also include the first inner via pattern BVS**12** on the first outer via pattern BVS**11**.
[0116] As the first backside via pattern BVS**1** has a sidewall whose portion protrudes toward the high-refractive layer **32**, a lateral surface of the first backside via pattern BVS**1** may include a curved surface.
[0117] As the first outer via pattern BVS**11** has a sidewall whose portion protrudes toward the high-refractive layer **32**, a lateral surface of the first outer via pattern BVS**11** may include a curved surface. The first outer via pattern BVS**11** may be in direct contact with the first via break VC**2**. When the first via break VC**2** includes an empty space therein, the lateral surface of the first outer via pattern BVS**11** may be exposed.
[0118] As the first inner via pattern BVS**12** has a sidewall whose portion protrudes toward the high-refractive layer **32**, a lateral surface of the first inner via pattern BVS**12** may include a curved surface.
[0119] An image sensor according to some embodiments of the disclosure may include the contact break VC**1** and the first via break VC**2**, and the contact conductive pattern **52**A and the first backside via pattern BVS**1** may have their sidewalls that protrude toward the high-refractive layer **32**. The same may apply to the pad break VC**3** between the backside conductive pad PAD and the high-refractive layer **32** and the second via break VC**4** between the second backside via pattern BVS**2** and the high-refractive layer **32**.
[0120] FIGS. **8** to **13**C illustrate cross-sectional views corresponding to line A-A′ of FIG. **3** and sections X and Y of FIG. **4**, showing a method of fabricating an image sensor according to some embodiments of the disclosure.
[0121] Referring to FIG. **8**, there may be prepared a second sub-chip CH**2** having the structure discussed with reference to FIG. **4** and a first sub-chip CHI bonded to the second sub-chip CH**2**. The bonding of the first sub-chip CH**1** to the second sub-chip CH**2** may include connecting the first sub-chip CH**1** to the second sub-chip CH**2** to allow a first interlayer dielectric layer ILD**1** to contact a second interlayer dielectric layer ILD**2**.
[0122] Referring to FIG. **9**, a second surface **100***b* of the substrate **100** may undergo a grinding process to reduce a thickness of the substrate **100** to a desired thickness. In this step, substrate isolation parts DTI may have an exposed top surface. A first dielectric layer **31**, a high-refractive layer **32**, a second dielectric layer **33**, and a third dielectric layer **34** may be conformally formed on the second surface **100***b* of the substrate **100**. An antireflection structure AL may be formed on the second surface **100***b* of the substrate **100**.
[0123] Referring to FIG. **10**, the first dielectric layer **31**, the high-refractive layer **32**, the second dielectric layer **33**, the third dielectric layer **34**, and a portion of the substrate **100** may be etched to form a backside contact trench **46** and a backside pad trench **60**. The backside contact trench **46** may expose the substrate isolation part DTI. The substrate **100** may be exposed by the backside pad trench **60**.
[0124] The first dielectric layer **31**, the high-refractive layer **32**, the second dielectric layer **33**, the third dielectric layer **34**, the substrate **100**, the first interlayer dielectric layer ILD**1**, and a portion of the second interlayer dielectric layer ILD**2** may be etched to form a first backside via hole H**1** and a second backside via hole H**2**.
[0125] The first backside via hole H**1** may expose a first interlayer wiring line MCL and a second interlayer wiring line **217**. The second interlayer wiring line **217** may be exposed by the second

backside via hole H**2**.
[0126] Referring to FIG. **11**, a portion of the high-refractive layer **32** may be selectively recessed through the backside contact trench **46**. Therefore, a first recess RS**1** may be formed.
[0127] A portion of the high-refractive layer **32** may be selectively recessed through the first backside via hole H**1**. Therefore, a second recess RS**2** may be formed.
[0128] A portion of the high-refractive layer **32** may be selectively recessed through the backside pad trench **60**. Therefore, a third recess RS**3** may be formed.
[0129] A portion of the high-refractive layer **32** may be selectively recessed through the second backside via hole H**2**. Therefore, a fourth recess RS**4** may be formed.
[0130] Referring to FIGS. **12**A, **12**B, and **12**C, a conductive layer may be conformally stacked on the third dielectric layer **34**, and the conductive layer may be etched to form an optical black liner **52***p*, a contact conductive pattern **52**A, a connection conductive pattern **52**B, a first backside via pattern BVS**1**, a second backside via pattern BVS**2**, a pad conductive pattern **52**C, and via connection lines **52**D.
[0131] In this step, the conductive layer may be stacked in a state where the first, second, third, and fourth recesses RS**1**, RS**2**, RS**3**, and RS**4** are empty. In an embodiment, the conductive layer may be stacked in a state where the first to fourth recesses RS**1**-RS**4** include a dielectric material. In an embodiment, the conductive layer may be stacked in a state where at least one of the first to fourth recesses RS**1**-RS**4** is empty and remaining ones of the first to fourth recesses RS**1**-RS**4** include a dielectric material.
[0132] Thus, a contact break VC**1**, a first via break VC**2**, a pad break VC**3**, and a second via break VC**4** (collectively referred to as “VC” in FIGS. **12**A-**12**C) may be formed.
[0133] Referring to FIGS. **13**A, **13**B, and **13**C, a light-shield layer and a low-refractive layer may be sequentially conformally stacked on the third dielectric layer **34**, and the light-shield layer and the low-refractive layer may be etched to form a light-shield pattern **48** and a low-refractive pattern **50**.
[0134] A protection layer **56** may be formed to cover the third dielectric layer **34**, the optical black liner **52***p*, the contact conductive pattern **52**A, the connection conductive pattern **52**B, the first backside via pattern BVS**1**, the second backside via pattern BVS**2**, the pad conductive pattern **52**C, the via connection lines **52**D, the light-shield pattern **48**, and the low-refractive pattern **50**.
[0135] Afterwards, referring back to FIG. **4**, color filters CF**1** and CF**2** may be formed between the low-refractive patterns **50**. An optical black pattern CFB may be formed on the optical black liner **52***p*. Microlenses ML may be formed on the color filters CF**1** and CF**2**. A lens residual layer MLR may be formed on the optical black pattern CFB. On the pad region PR, an opening **35** may be formed in the lens residual layer MLR to expose the backside conductive pad PAD. An image sensor may be fabricated as shown in FIGS. **3** and **4**.
[0136] According to the disclosure, an image sensor may include a break, which includes an empty space or a dielectric material, disposed between a backside contact and a high-refractive layer. In this case, the backside contact and the high-refractive layer may be spaced apart from each other, and an electrical short structure may be formed.
[0137] According to the disclosure, as the break is disposed between the backside contact and the high-refractive layer, an electrical leakage path may be interrupted when a high-refractive material is applied to a bottom antireflective layer (BARL), and thus the image sensor may have improved performance. In addition, since an additional process step for avoiding a leakage current is not required, a manufacturing cost of the image sensor may be reduced.
[0138] The aforementioned description provides some example embodiments for explaining the disclosure. Therefore, the disclosure are not limited to the embodiments described above, and it will be understood by one of ordinary skill in the art that variations in form and detail may be made therein without departing from the spirit and essential features of the disclosure.

Claims

1. An image sensor, comprising: a substrate that has a first surface and a second surface that are opposite to each other, the substrate including a pixel array area and an edge area; an antireflection structure on the second surface; a substrate isolation part in the substrate, the substrate isolation part separating the substrate; a microlens on the antireflection structure; and a backside contact in a backside contact trench, the backside contact trench penetrating the antireflection structure, the backside contact being in contact with the substrate isolation part, wherein the backside contact includes: a contact conductive pattern on a sidewall of the backside contact trench; and a contact metal pattern on the contact conductive pattern, and wherein the antireflection structure includes: a first dielectric layer; a high-refractive layer on the first dielectric layer; and a contact break between the high-refractive layer and the backside contact.
2. The image sensor of claim 1, wherein the high-refractive layer includes titanium oxide, and wherein the contact break includes an empty space therein.
3. The image sensor of claim 1, wherein a refractive index of the substrate is greater than a refractive index of the high-refractive layer.
4. The image sensor of claim 1, wherein the antireflection structure includes: a second dielectric layer on the high-refractive layer; and a third dielectric layer on the second dielectric layer, and wherein a refractive index of the second dielectric layer is less than a refractive index of the high-refractive layer and is about 1 or greater than 1.
5. The image sensor of claim 1, wherein the high-refractive layer includes titanium oxide, and wherein the contact break includes SiO.sub.2 or Al.sub.2O.sub.3.
6. The image sensor of claim 1, further comprising: a first interlayer dielectric layer on the first surface of the substrate; a first interlayer wiring line in the first interlayer dielectric layer; a second interlayer dielectric layer on or below the first interlayer dielectric layer; a second interlayer wiring line in the second interlayer dielectric layer; a first backside via pattern that penetrates the antireflection structure on the edge area; and a connection conductive pattern that continuously connects the first backside via pattern and the contact conductive pattern to each other, wherein the first backside via pattern electrically connects the first interlayer wiring line and the second interlayer wiring line to each other.
7. The image sensor of claim 1, further comprising: a first backside via pattern that penetrates the antireflection structure on the edge area; and a first via break between the high-refractive layer and the first backside via pattern.
8. The image sensor of claim 1, wherein the contact break has a contact break lateral surface in contact with the contact conductive pattern, the contact break lateral surface including a curved surface.
9. An image sensor, comprising: a substrate that has a first surface and a second surface that are opposite to each other, the substrate including a pixel array area and an edge area; an antireflection structure on the second surface; a microlens on the antireflection structure; a first backside via pattern that penetrates the antireflection structure and the substrate on the edge area; a first interlayer dielectric layer on the first surface of the substrate; a first interlayer wiring line in the first interlayer dielectric layer; a second interlayer dielectric layer on or below the first interlayer dielectric layer; and a second interlayer wiring line in the second interlayer dielectric layer, wherein the antireflection structure includes: a first dielectric layer; a high-refractive layer on the first dielectric layer; and a first via break between the high-refractive layer and the first backside via pattern.
10. The image sensor of claim 9, wherein the first backside via pattern includes a first via protrusion that protrudes toward the high-refractive layer.
11. The image sensor of claim 9, wherein a refractive index of the high-refractive layer is between

about 2.0 to about 2.3.

12. The image sensor of claim 9, further comprising: a substrate isolation part in the substrate, the substrate isolation part separating the substrate; and a backside contact in a backside contact trench the backside contact trench penetrating the antireflection structure, the backside contact being in contact with the substrate isolation part, wherein the backside contact includes: a contact conductive pattern on a sidewall of the backside contact trench; and a contact metal pattern on the contact conductive pattern, wherein the antireflection structure further includes a contact break that is between the high-refractive layer and a sidewall of the contact conductive pattern.

13. The image sensor of claim 12, wherein the backside contact includes a contact protrusion that protrudes toward the contact break.

14. The image sensor of claim 12, further comprising a connection conductive pattern that continuously connects the first backside via pattern and the contact conductive pattern to each other.

15. The image sensor of claim 9, wherein the high-refractive layer includes titanium oxide, and wherein the via break includes an empty space.

16. The image sensor of claim 9, wherein the via break includes SiO.sub.2 or Al.sub.2O.sub.3.

17. The image sensor of claim 9, further comprising a backside contact in a backside contact trench, the backside contact trench penetrating the antireflection structure, wherein the antireflection structure further includes a second dielectric layer on the high-refractive layer, and wherein the second dielectric layer is continuously interposed between the backside contact and the first backside via pattern.

18. An image sensor, comprising: a substrate that has a first surface and a second surface that are opposite to each other, the substrate including a pixel array area and an edge area; a transfer gate on the first surface; an antireflection structure on the second surface; a substrate isolation part in the substrate, the substrate isolation part separating the substrate; a microlens on the antireflection structure; and a backside contact in a backside contact trench, the backside contact trench penetrating the antireflection structure, the backside contact being in contact with the substrate isolation part, wherein the backside contact includes: a contact conductive pattern on a sidewall of the backside contact trench; and a contact metal pattern on the contact conductive pattern, wherein the antireflection structure includes: a first dielectric layer; a high-refractive layer on the first dielectric layer; and a contact break between the high-refractive layer and the backside contact, and wherein the backside contact includes a contact protrusion that protrudes toward the contact break.

19. The image sensor of claim 18, wherein the contact break includes an empty space therein.

20. The image sensor of claim 18, wherein the contact conductive pattern includes: a first contact conductive pattern in contact with the substrate; and a second contact conductive pattern on the first contact conductive pattern, wherein the first contact conductive pattern includes titanium, and wherein the second contact conductive pattern includes tungsten.