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(54) **DISPLAY PANEL, REPAIRING METHOD  
AND DISPLAY DEVICE**

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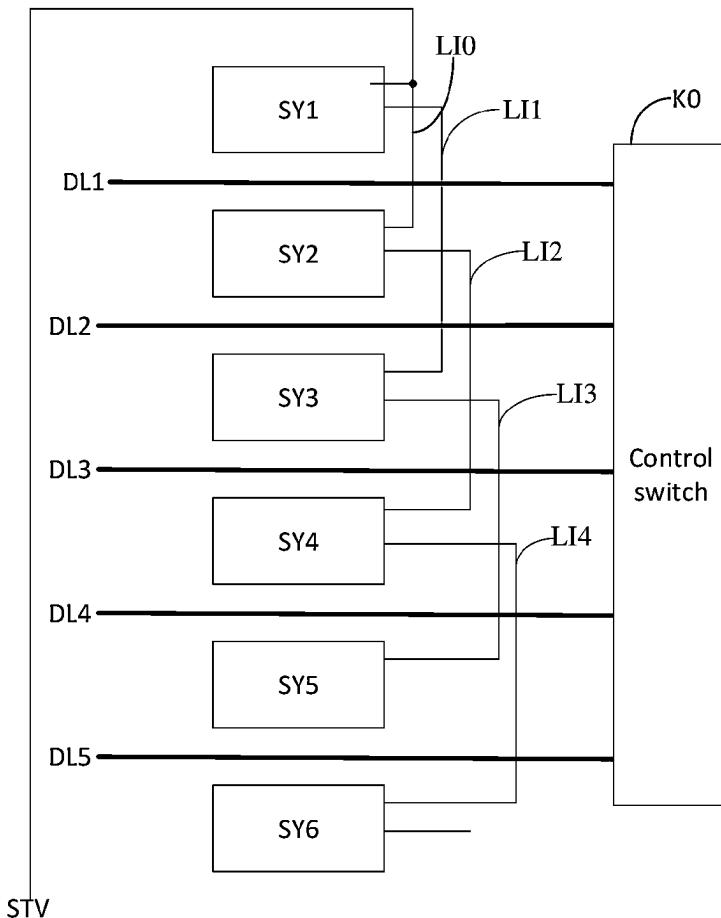
**Publication Classification**

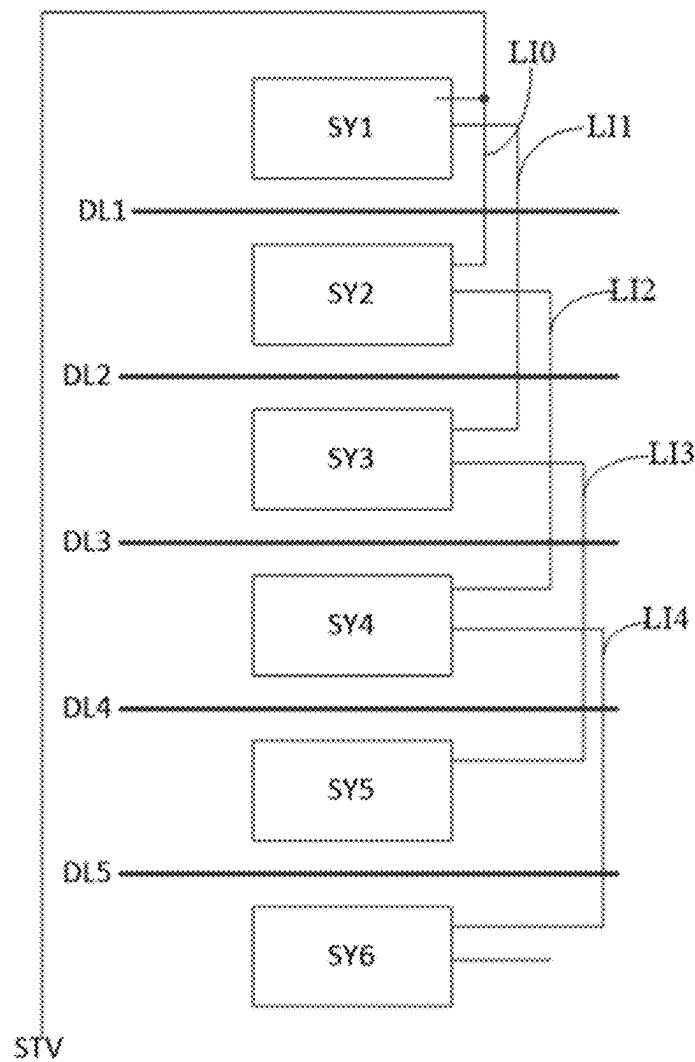
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**H10D 86/40** (2025.01)

(52) **U.S. Cl.**  
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(2013.01); **G09G 2310/0286** (2013.01); **G09G  
2330/08** (2013.01); **H10D 86/441** (2025.01)

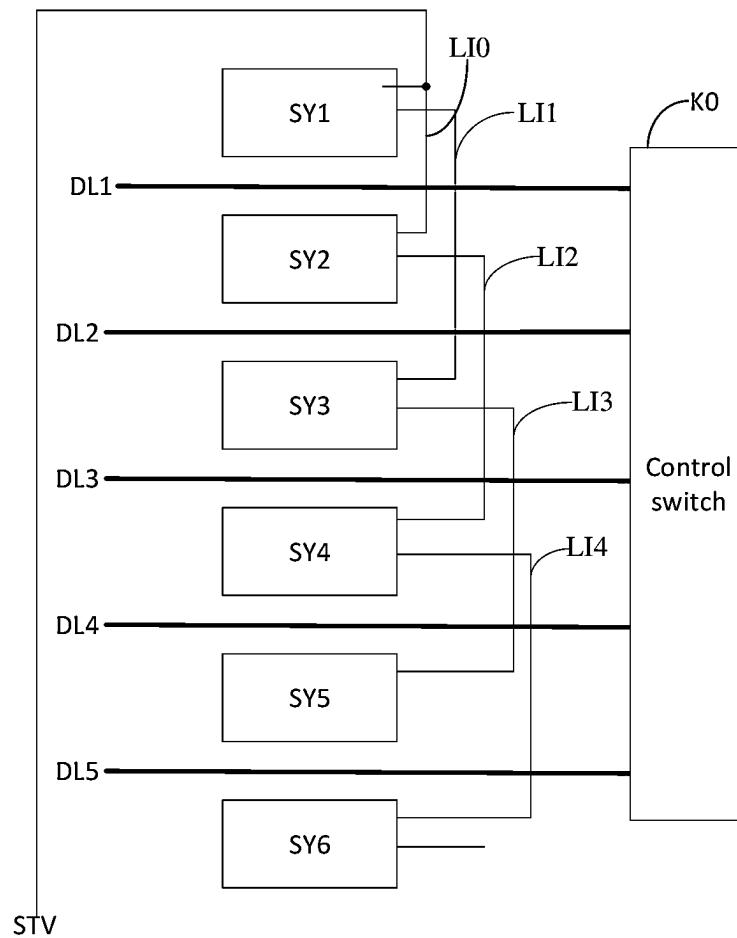
(57) **ABSTRACT**

A display substrate includes a base substrate and a driving module arranged on the base substrate; the driving module includes a control switch and a driving circuit; an input terminal of an nth stage of driving circuit included in the driving module is electrically connected to an output terminal of an (n-m)th stage of driving circuit included in the driving module through an input cascade line; n and m are positive integers, and m is less than n; the driving module further includes at least one connection line, the connection line extends along a first direction; there is an overlapping area between an orthographic projection of the connection line on the base substrate and an orthographic projection of the start voltage line and/or the input cascade line on the base substrate; the control switch is electrically connected to the connection line.





**FIG. 1**



**FIG. 2**

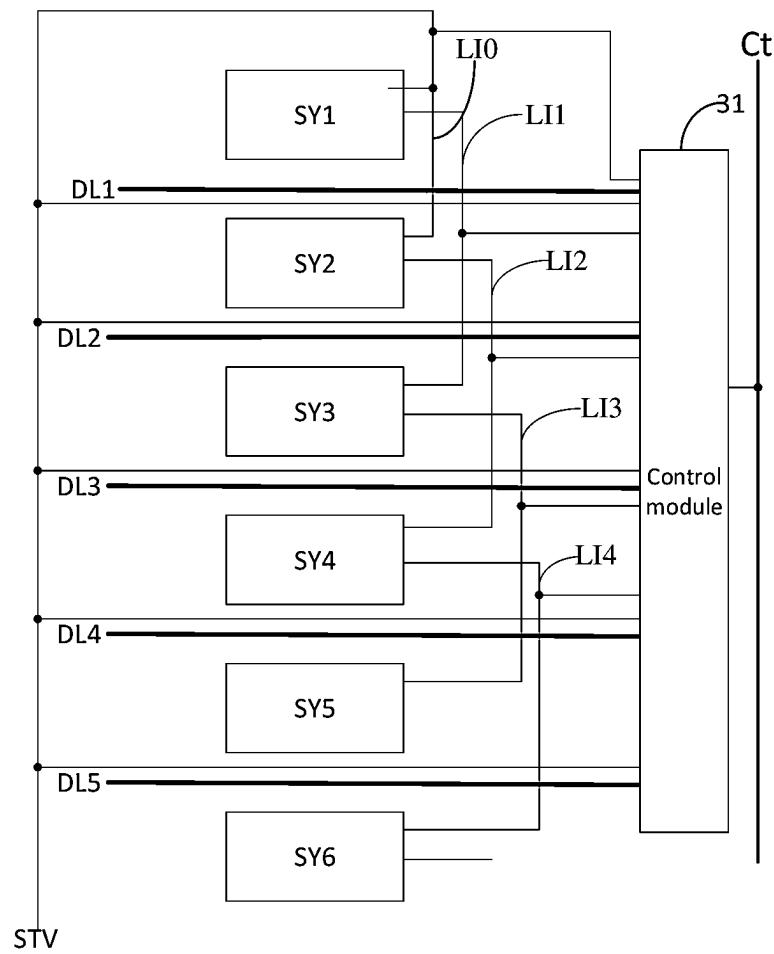


FIG. 3

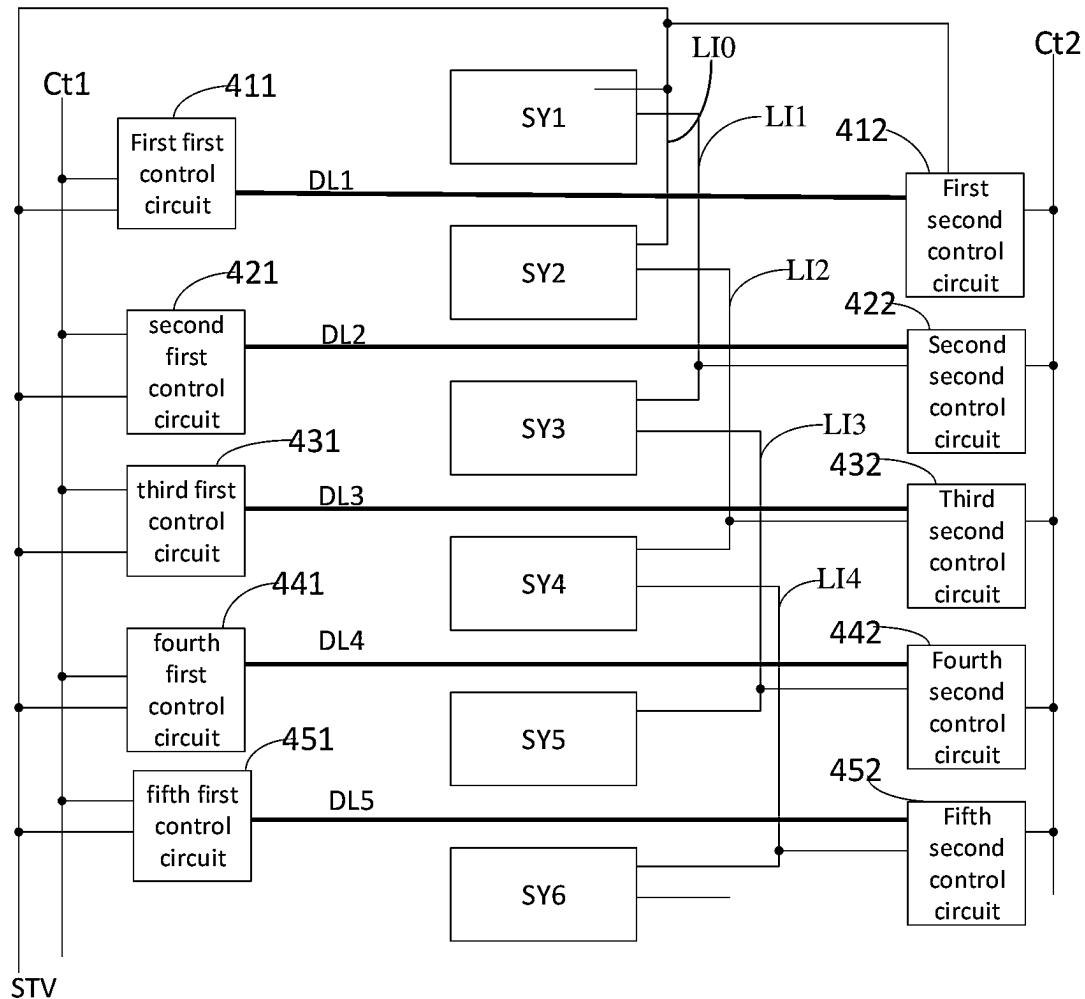


FIG. 4

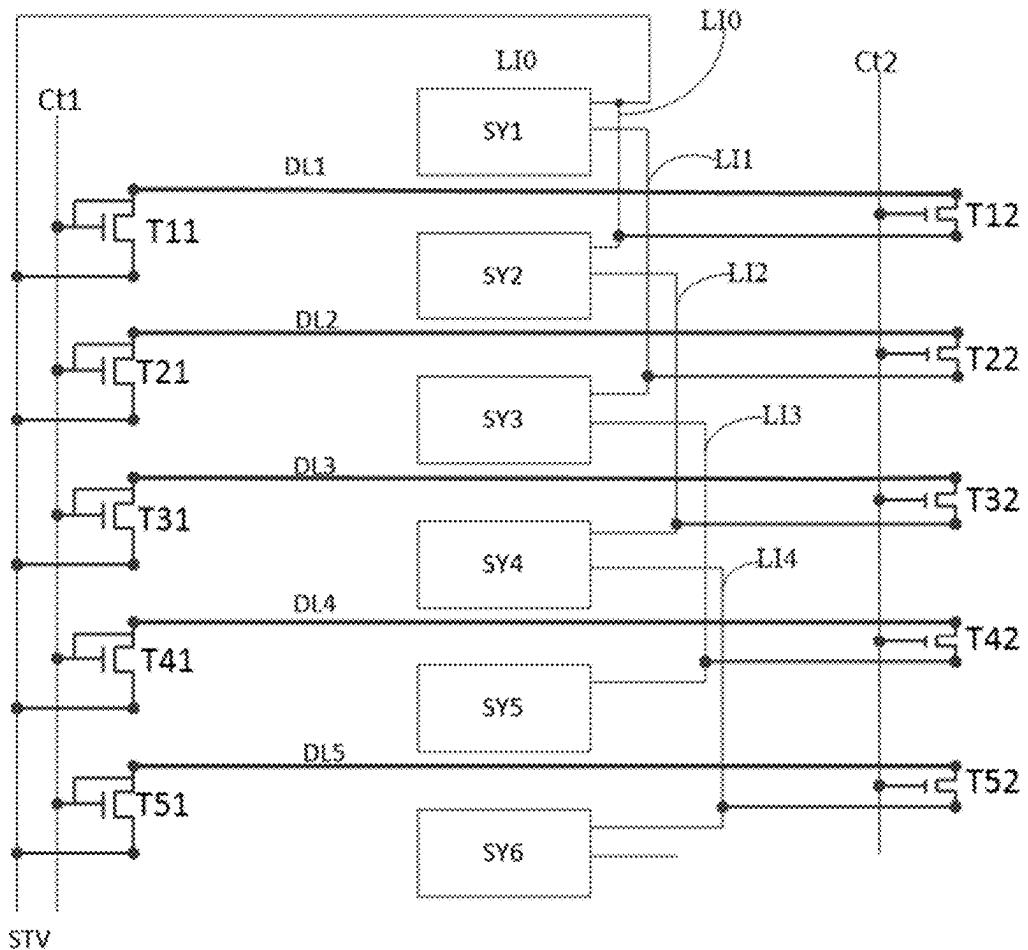


FIG. 5A

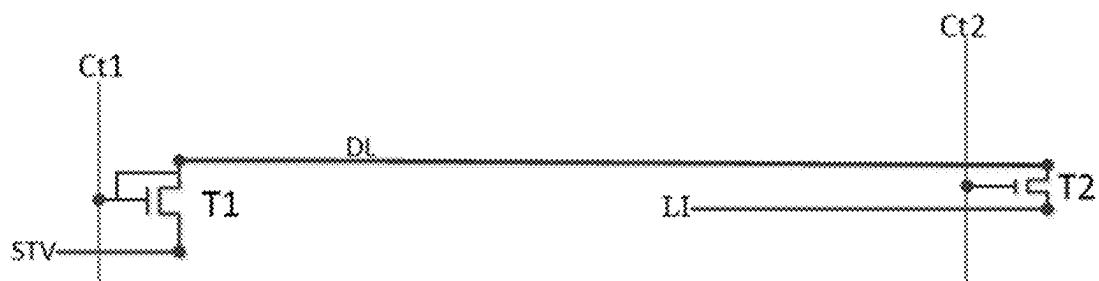


FIG. 5B

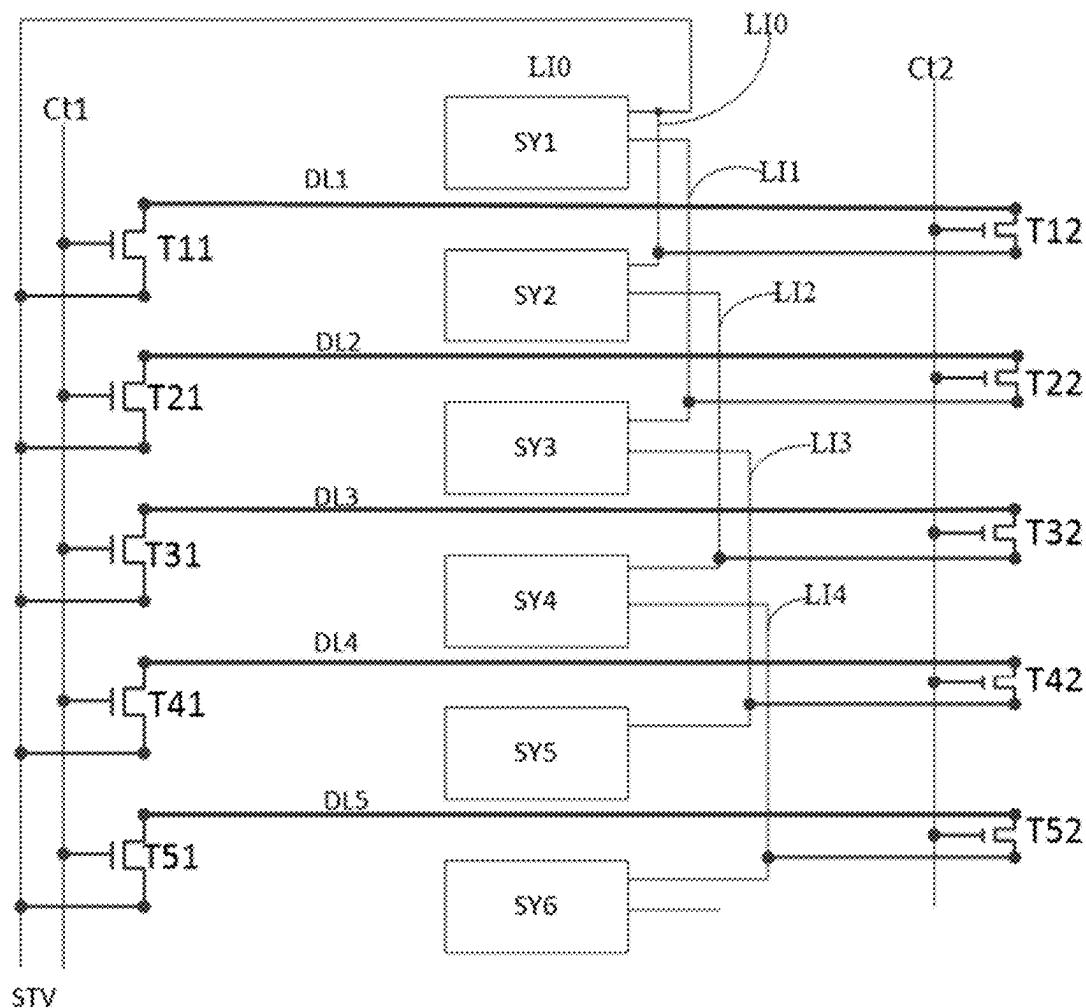


FIG. 6A

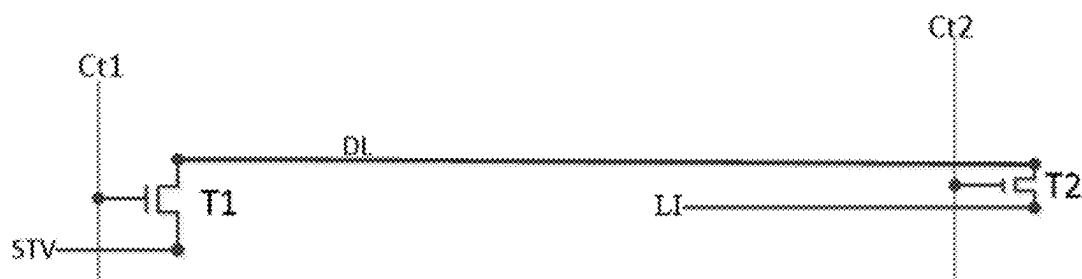


FIG. 6B

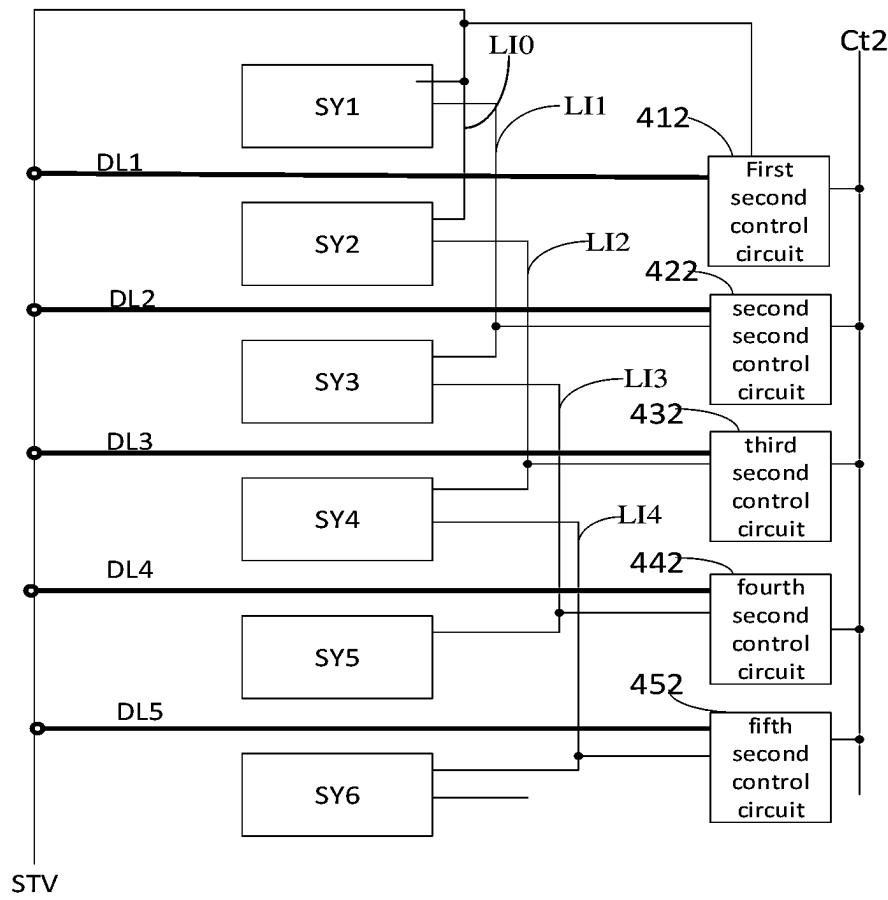


FIG. 7

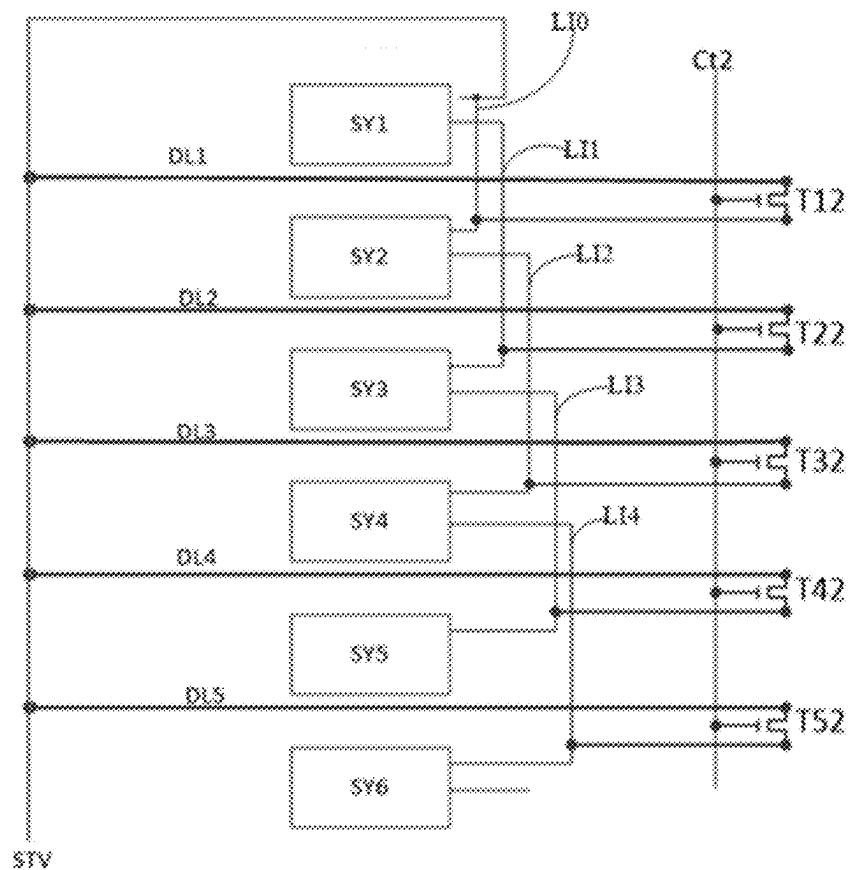


FIG. 8A

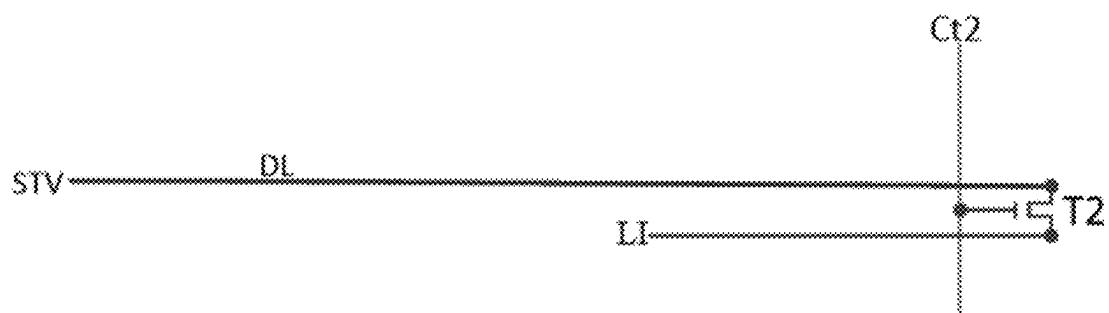
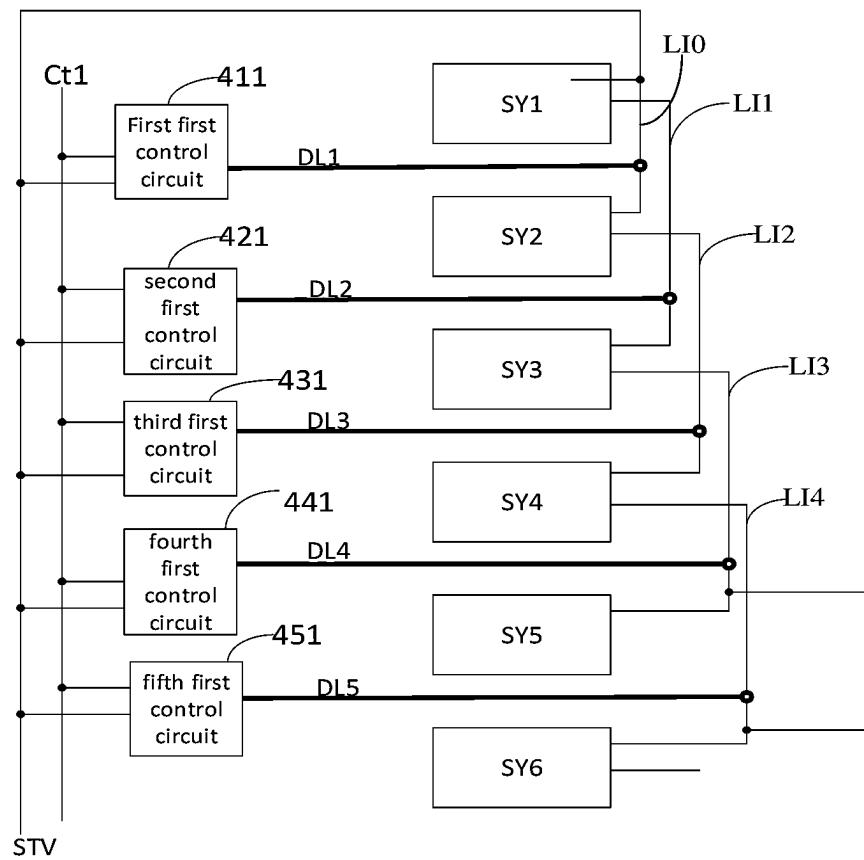


FIG. 8B



**FIG. 9**

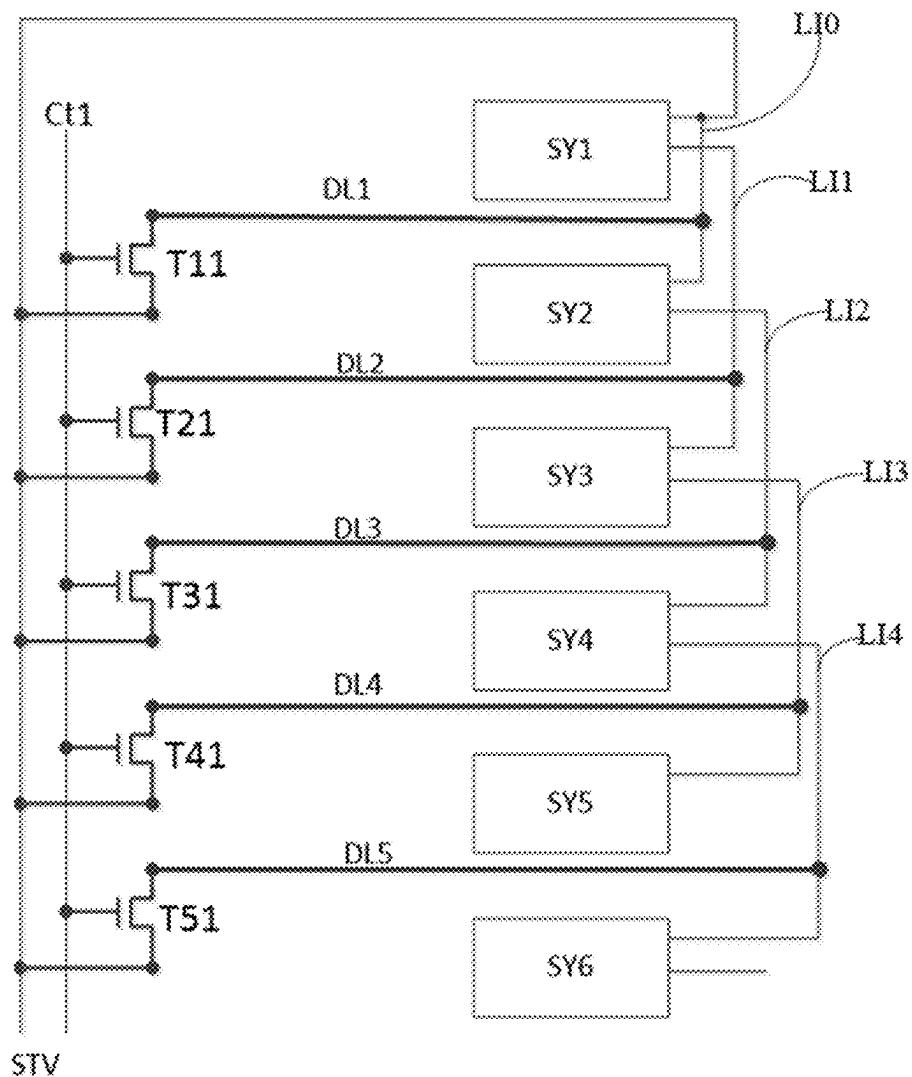


FIG. 10A

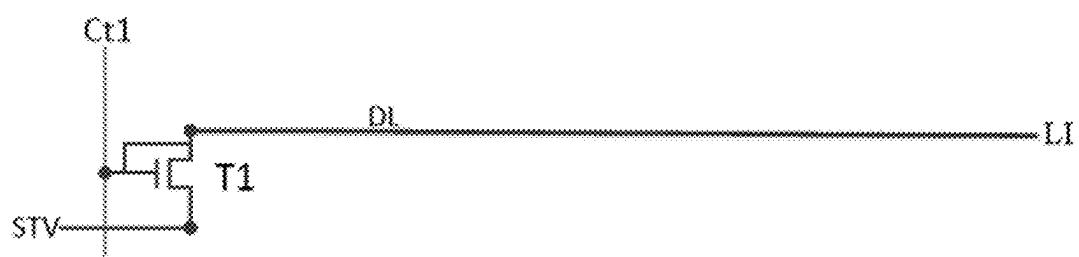


FIG. 10B

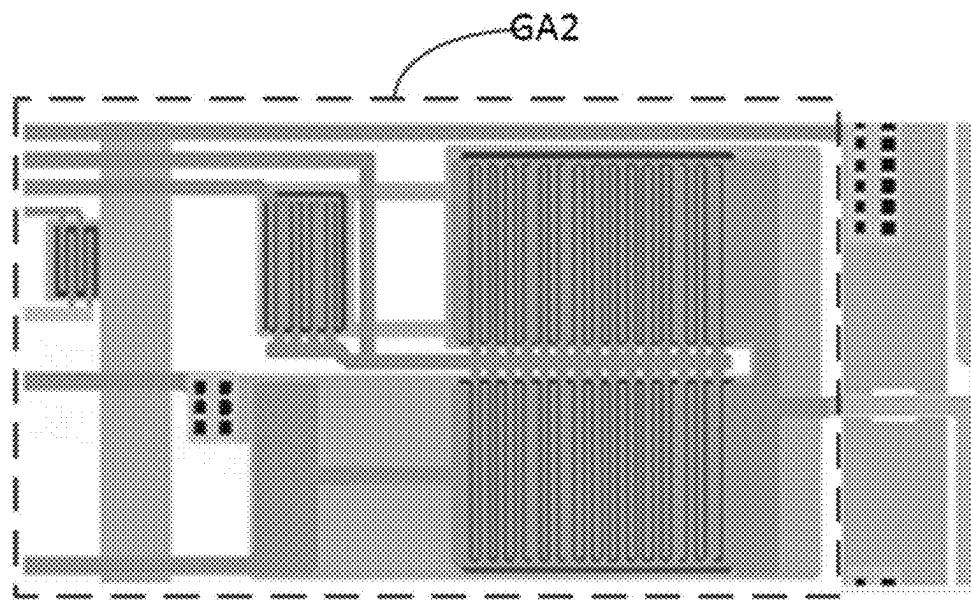


FIG. 11

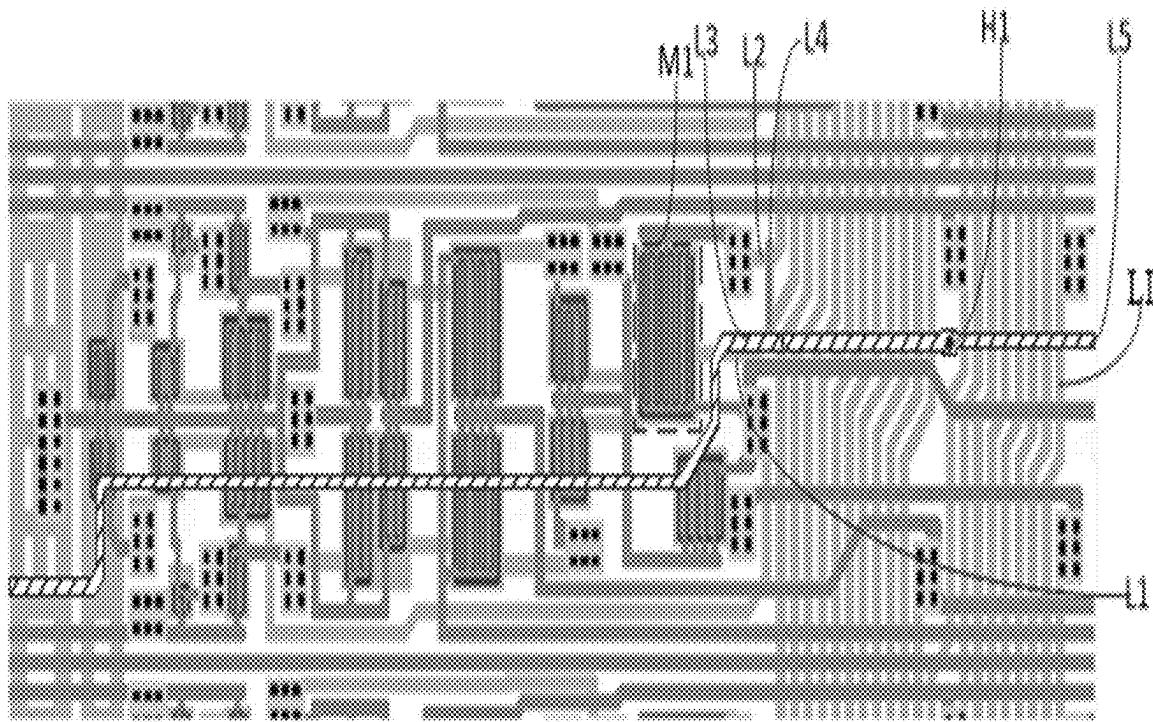
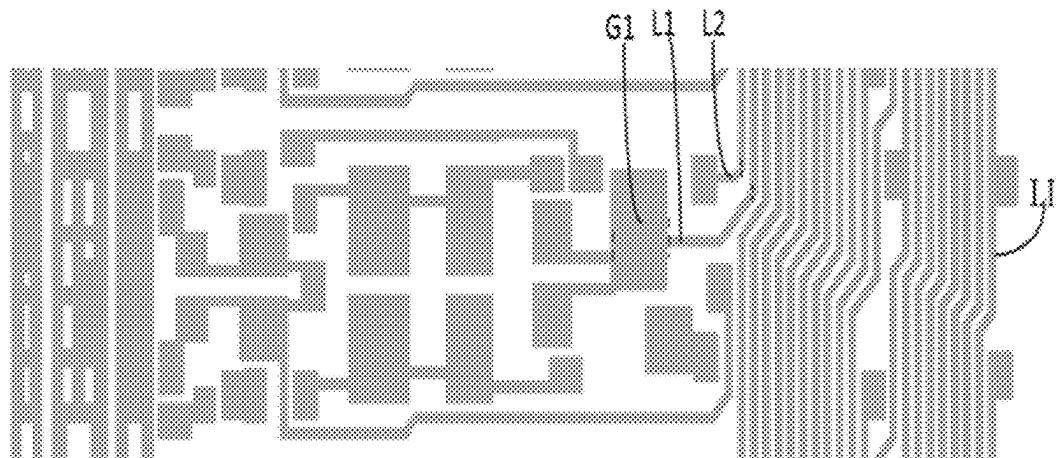
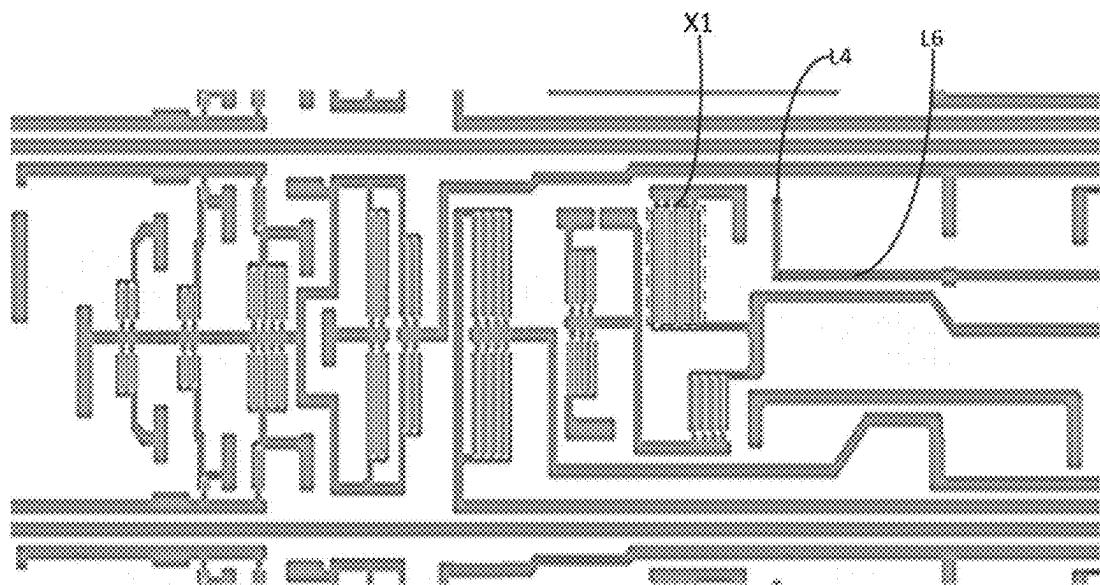


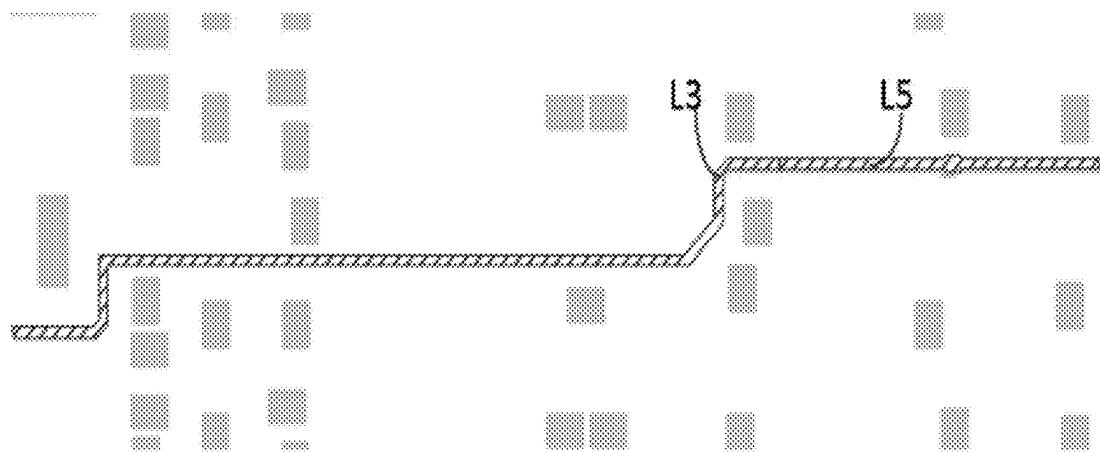
FIG. 12



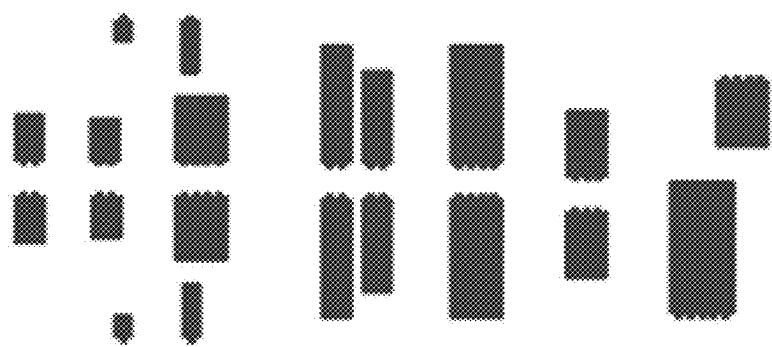
**FIG. 13**



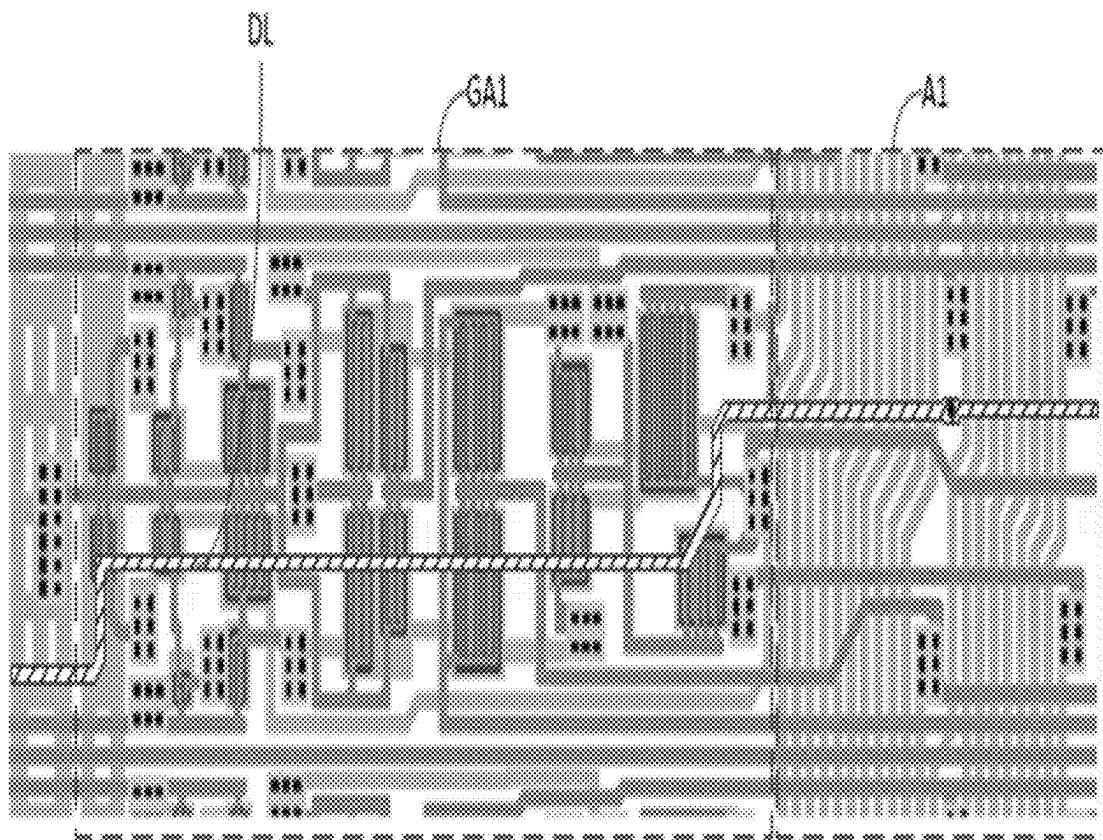
**FIG. 14**



**FIG. 15**



**FIG. 16**



**FIG. 17**

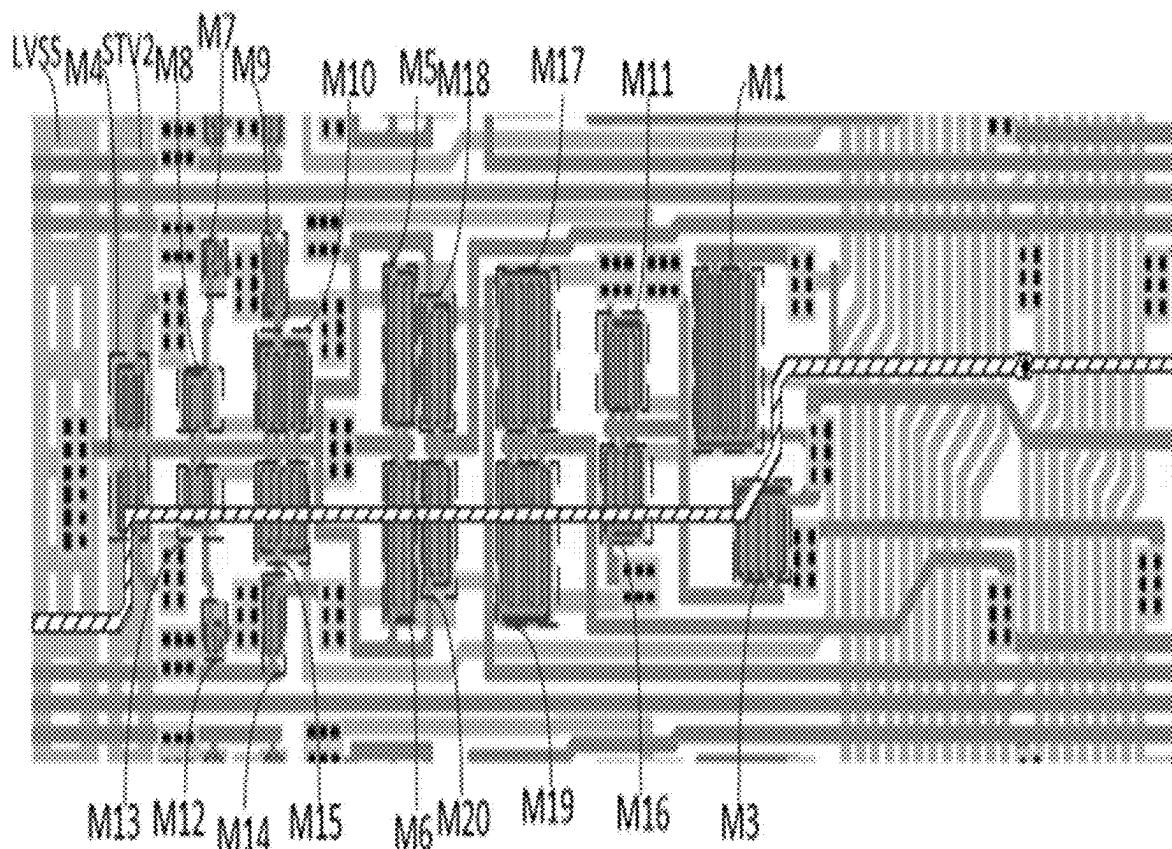


FIG. 18

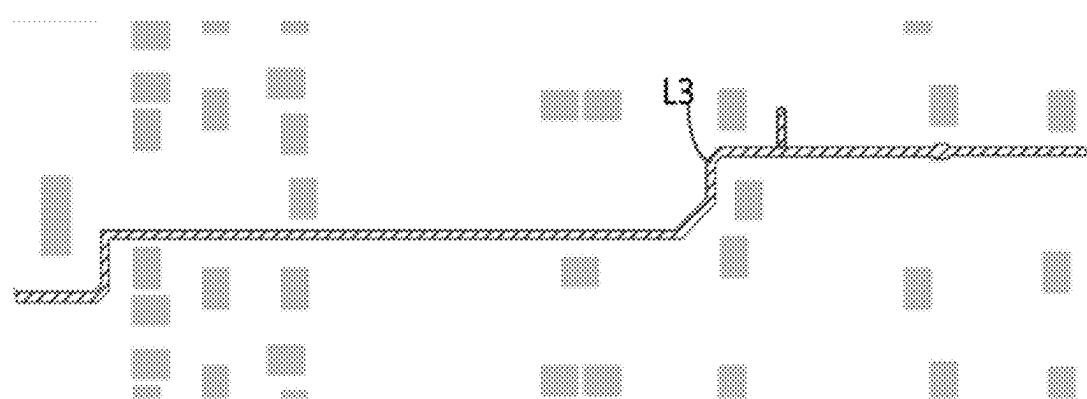


FIG. 19

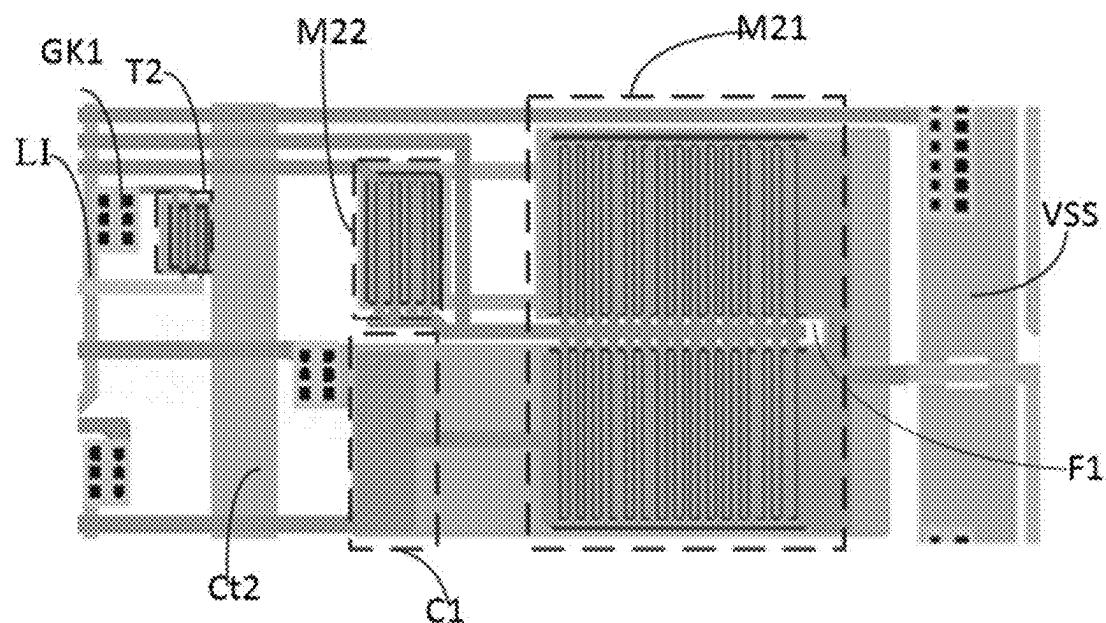


FIG. 20

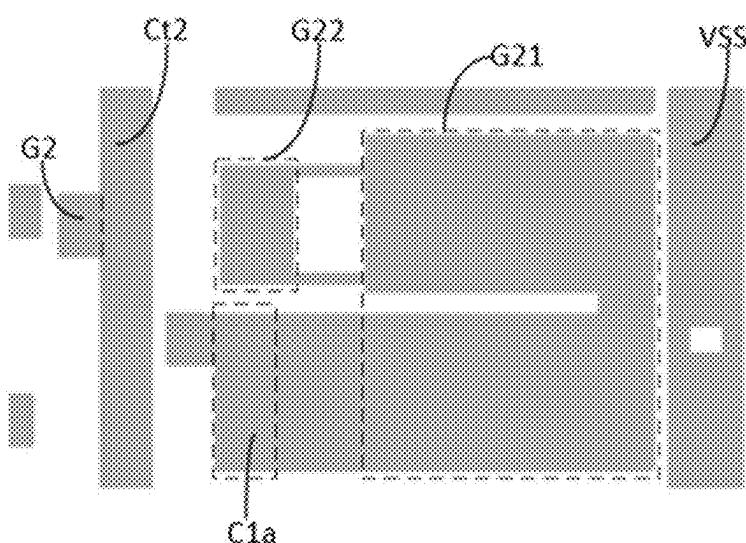


FIG. 21

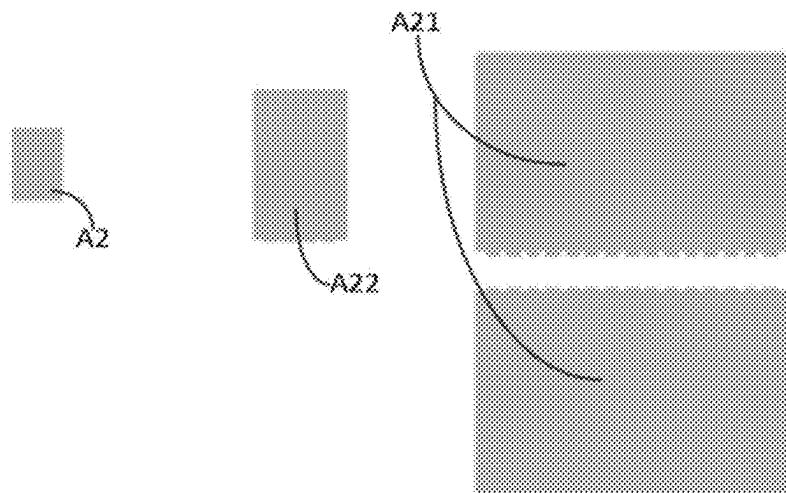


FIG. 22

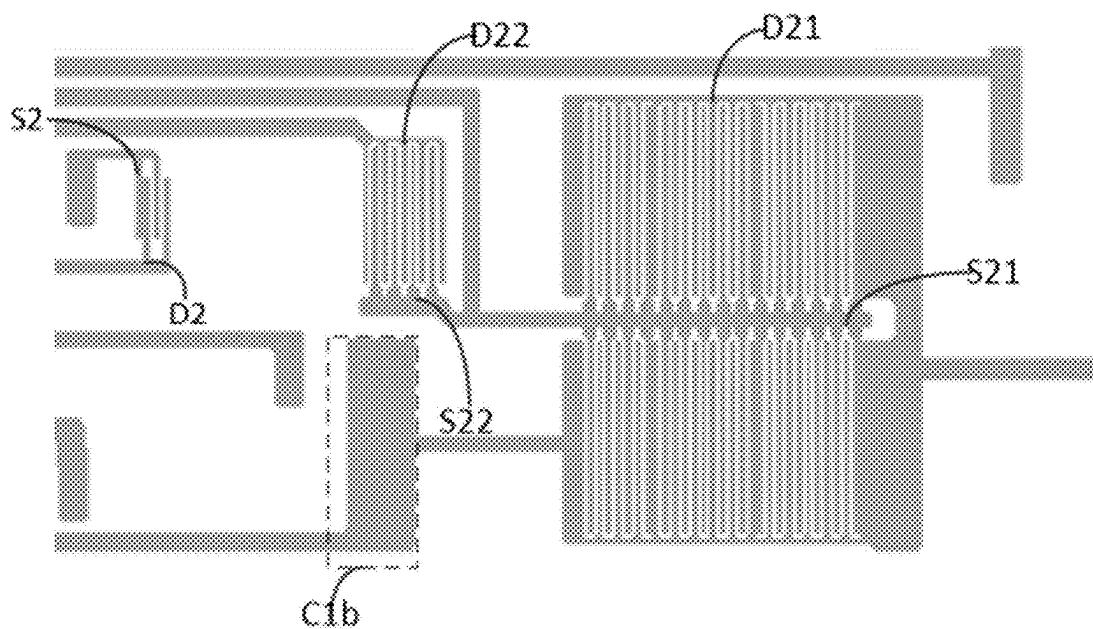
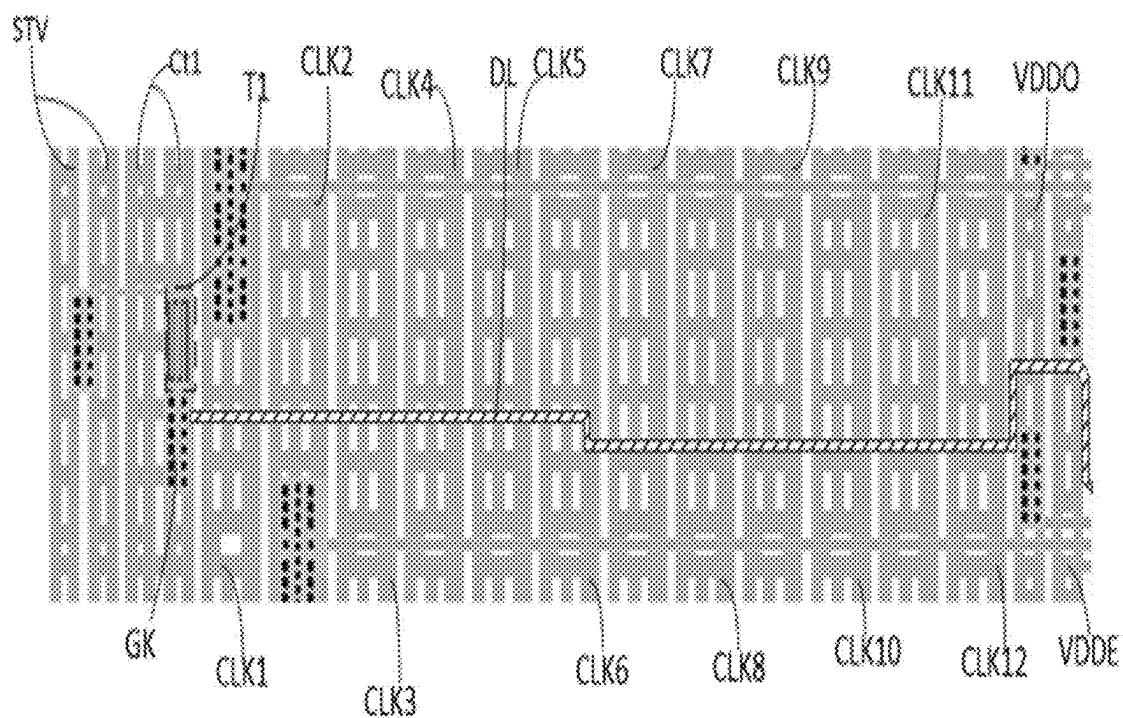


FIG. 23



**FIG. 24**



**FIG. 25**

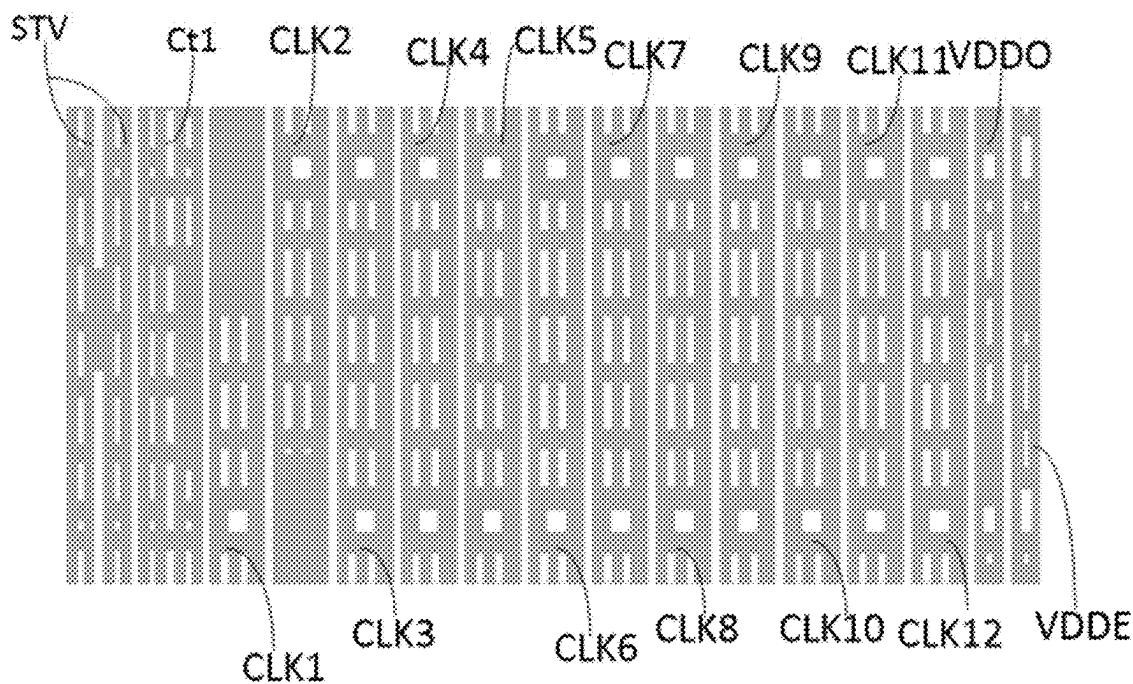


FIG. 26

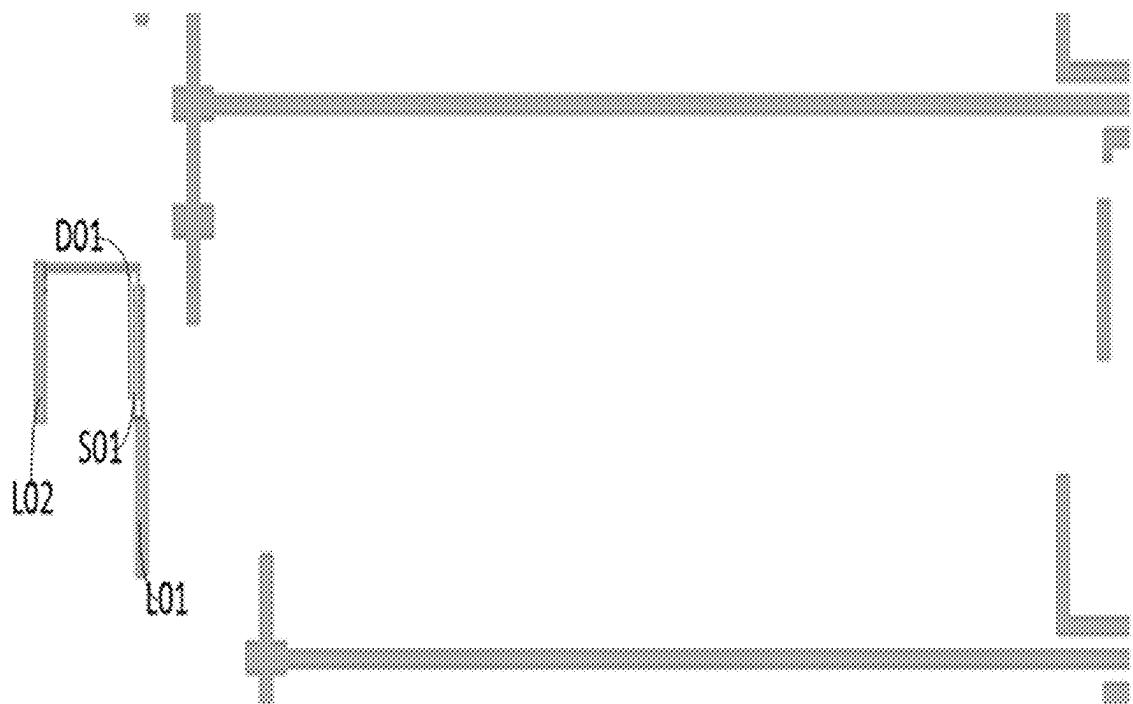
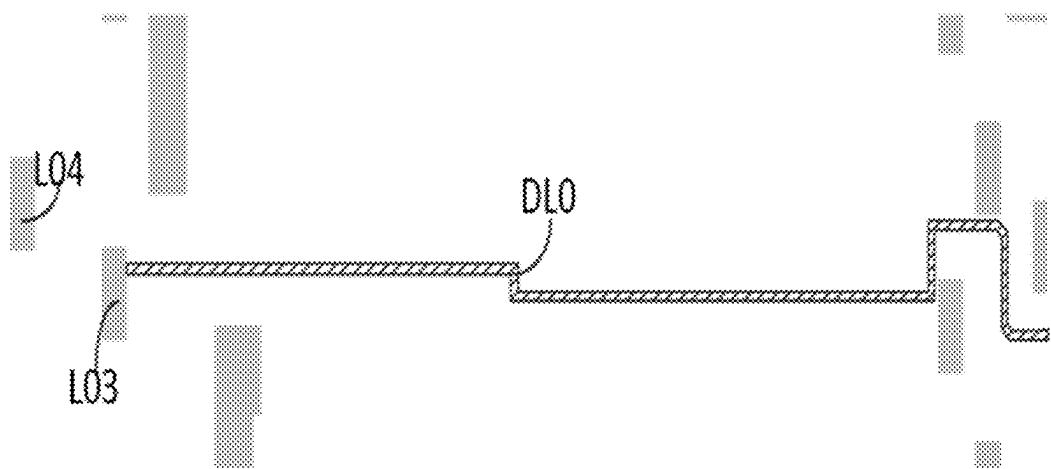
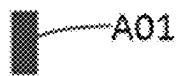


FIG. 27



**FIG. 28**



**FIG. 29**

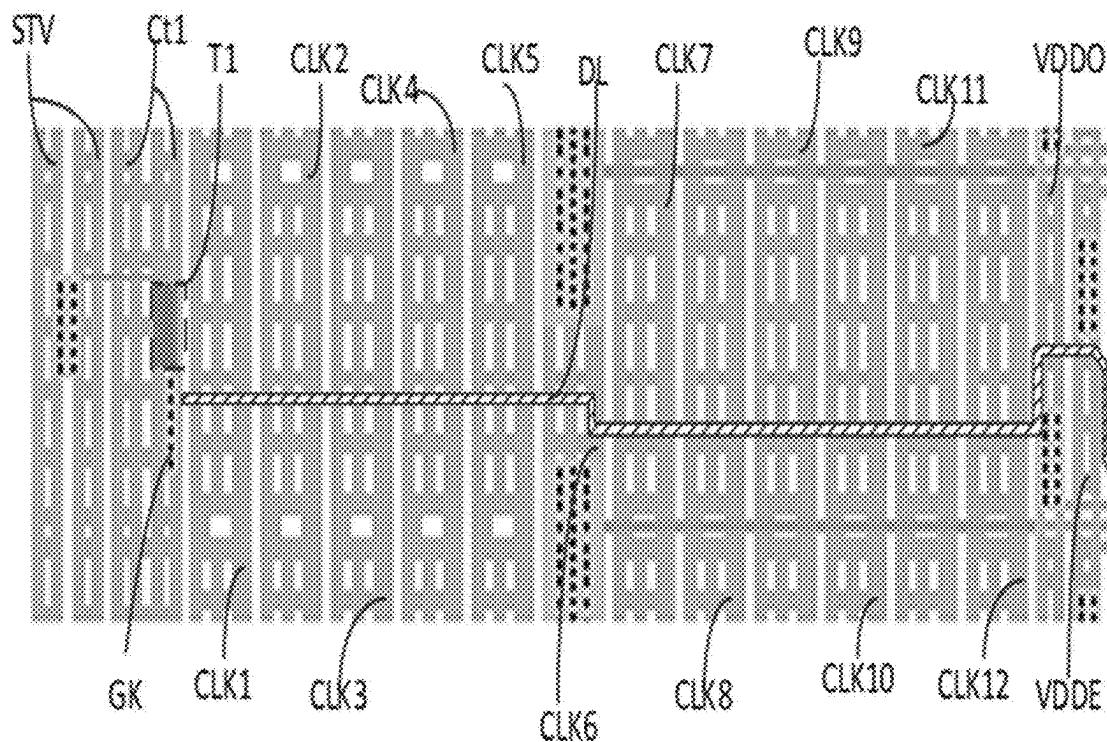


FIG. 30

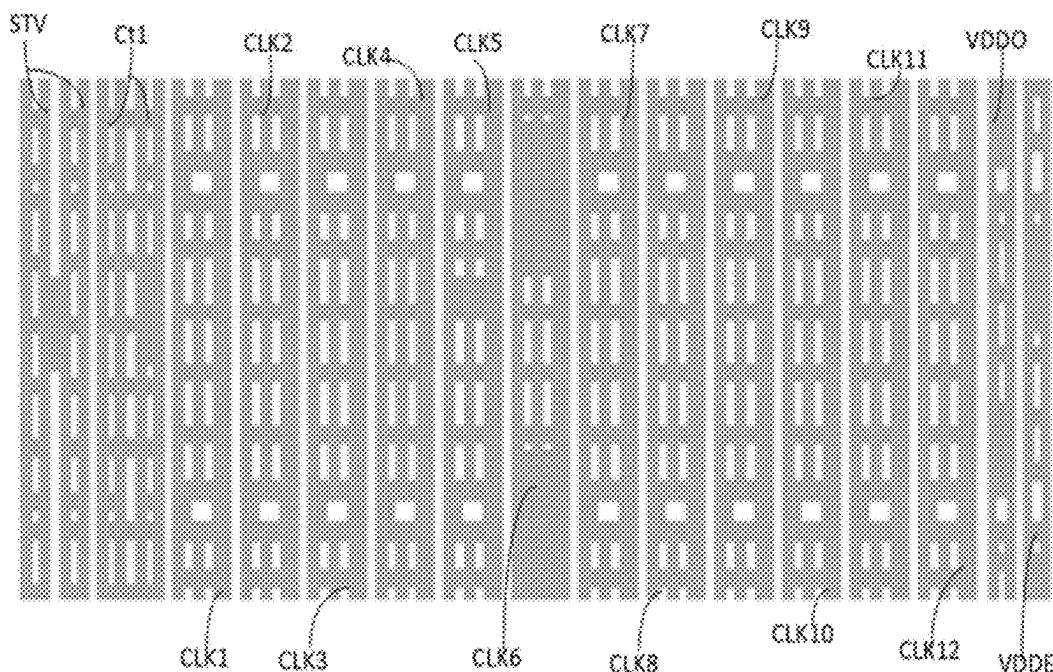


FIG. 31



FIG. 32

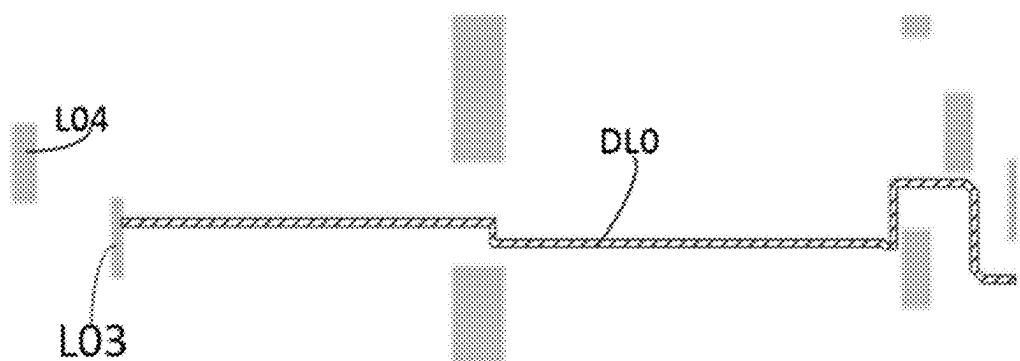


FIG. 33



FIG. 34

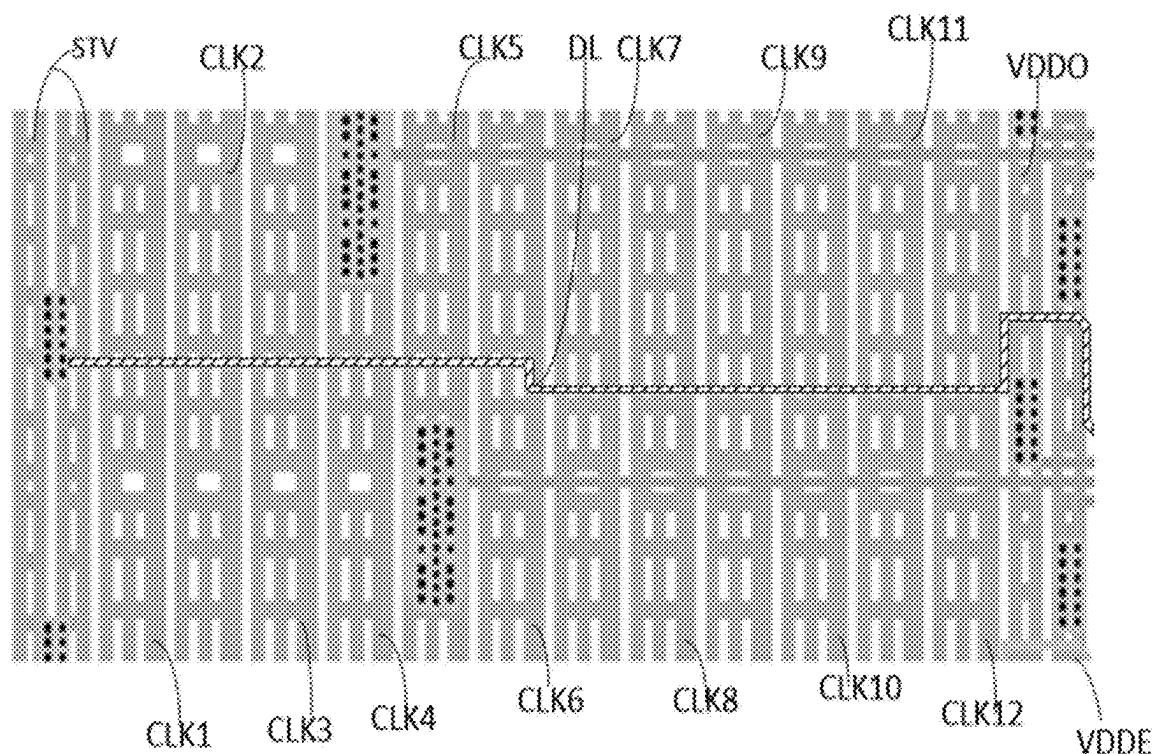
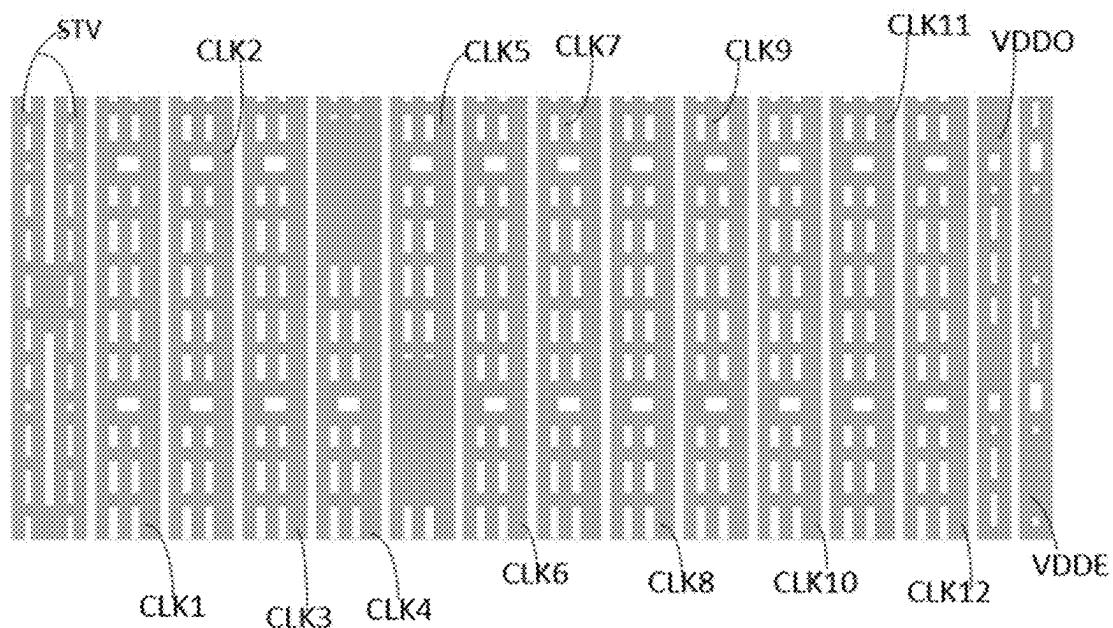


FIG. 35

FIG. 36



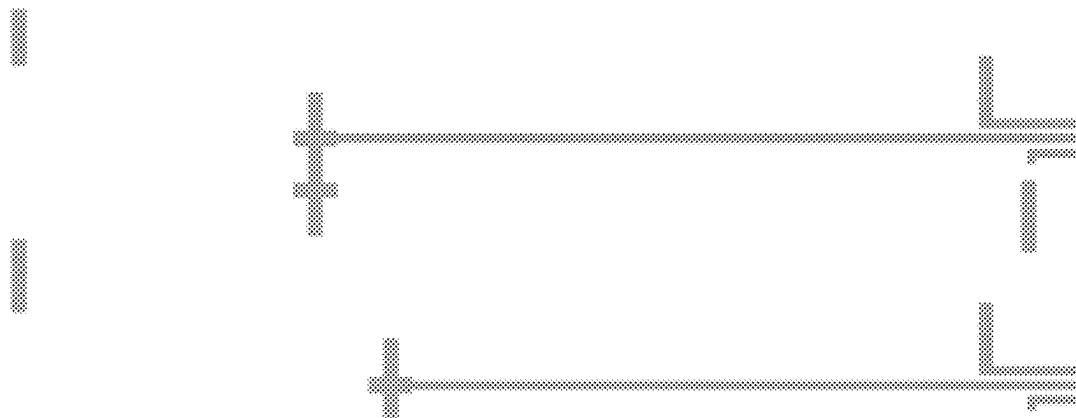


FIG. 37

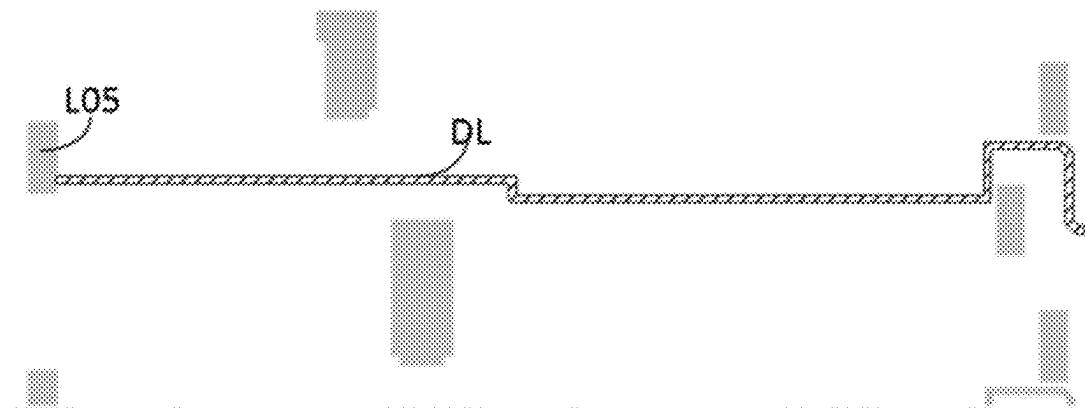


FIG. 38

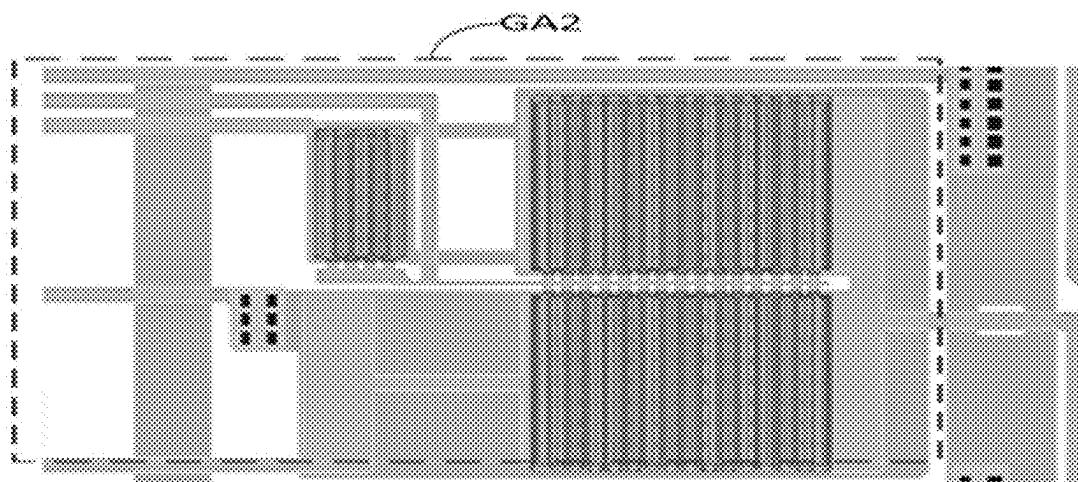


FIG. 39

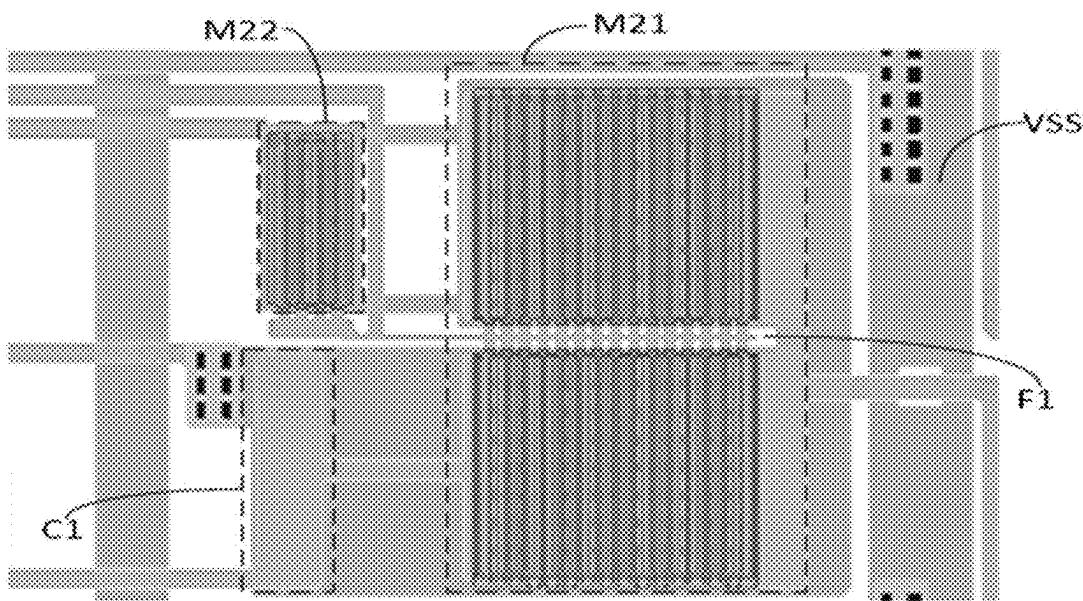
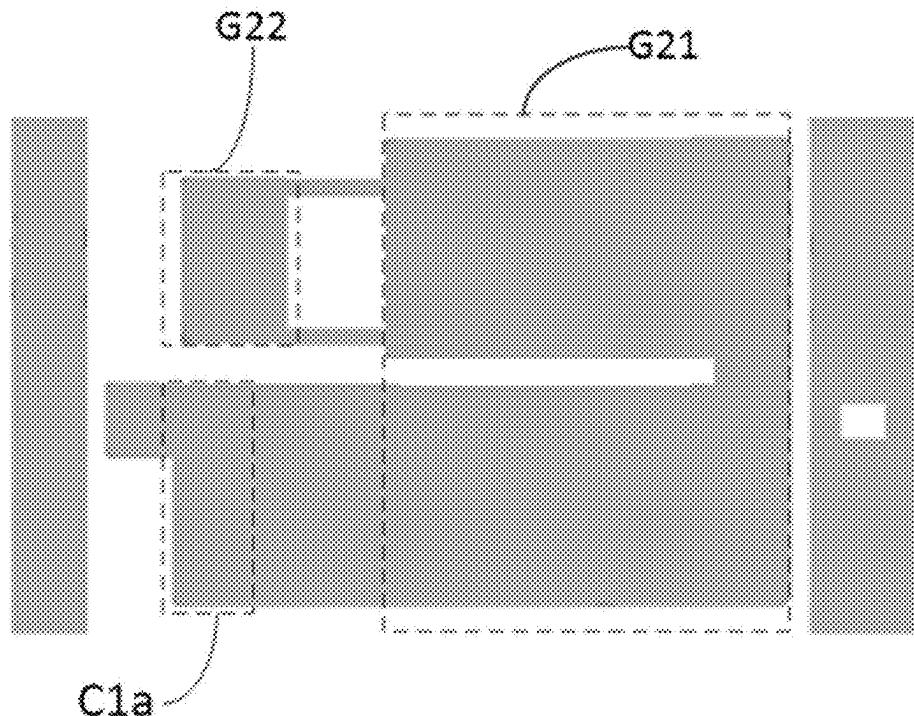
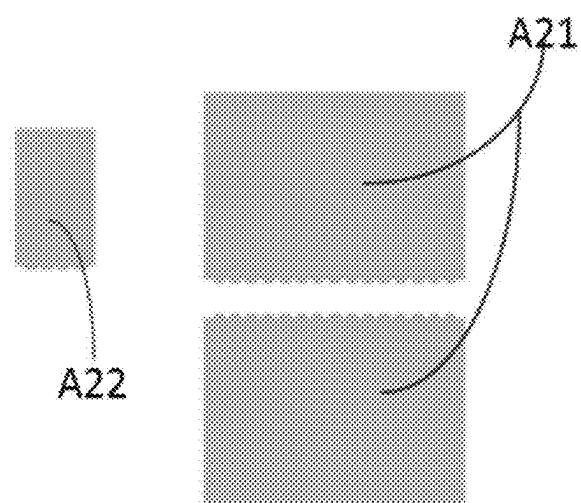


FIG. 40



**FIG. 41**



**FIG. 42**

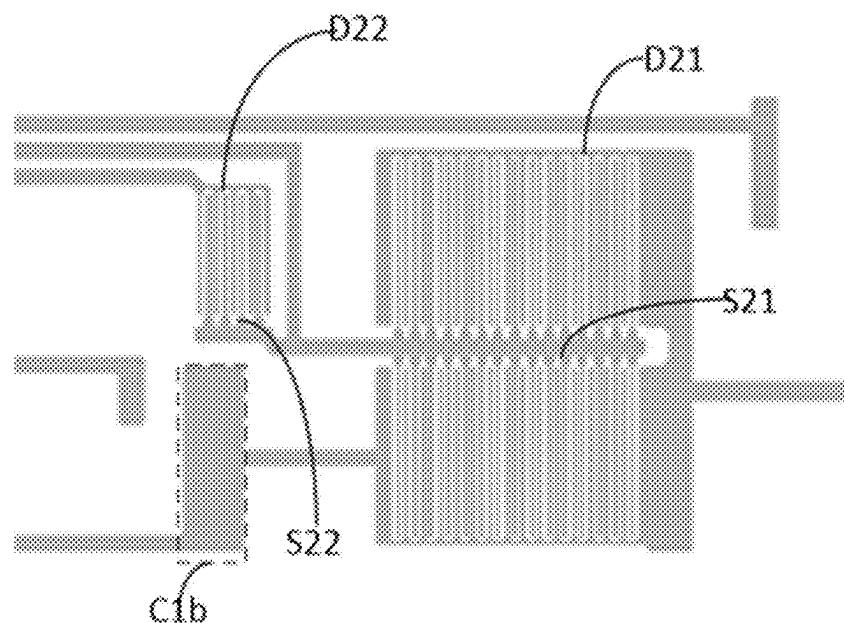


FIG. 43



FIG. 44

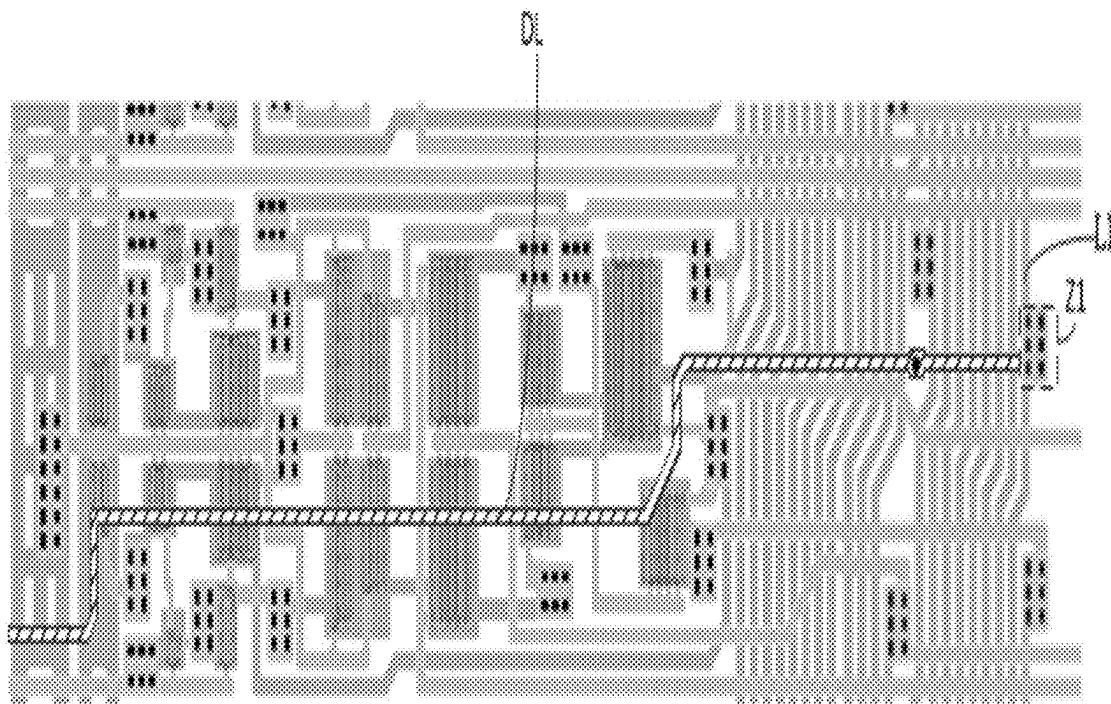


FIG. 45

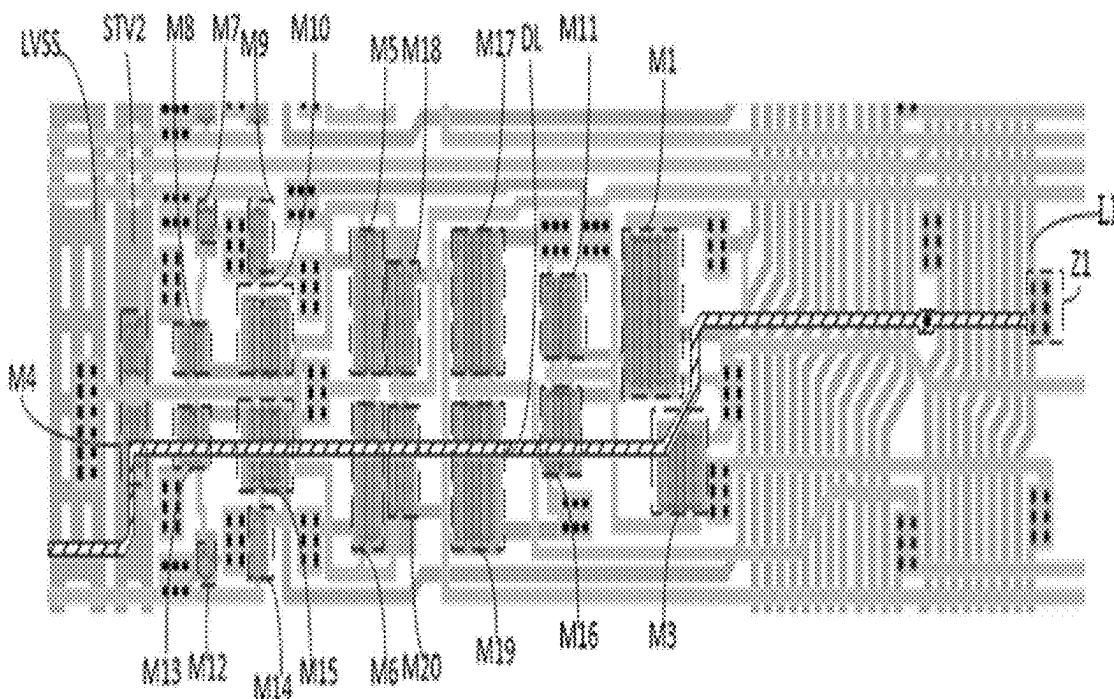


FIG. 46

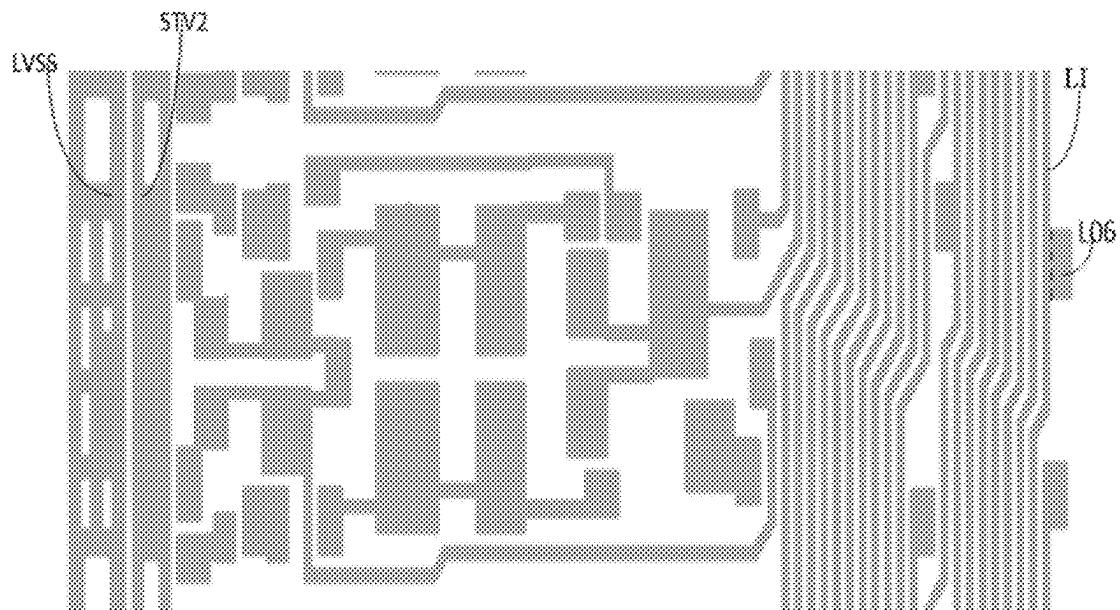


FIG. 47

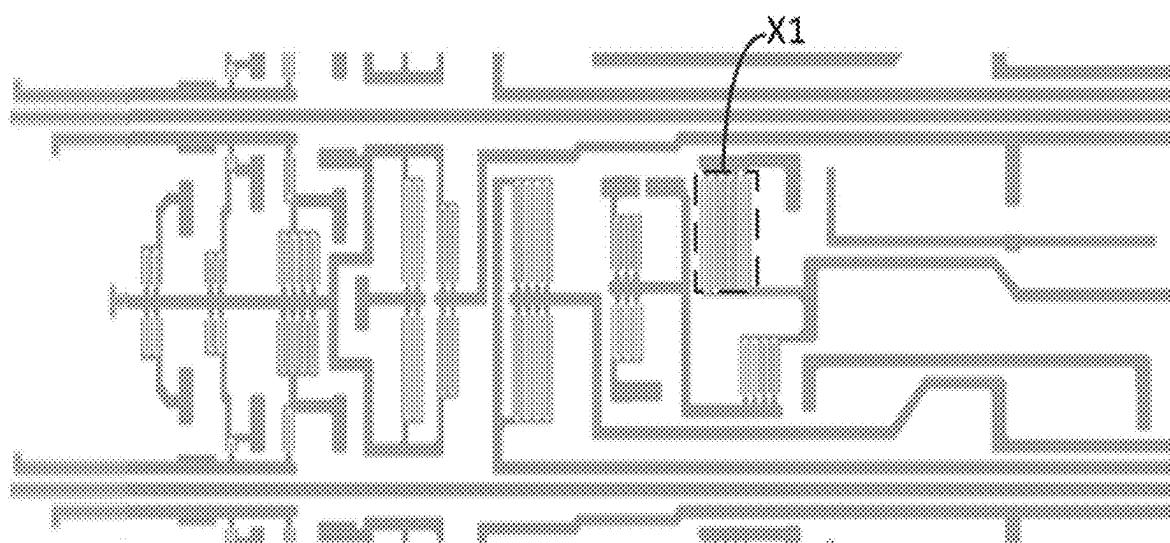


FIG. 48

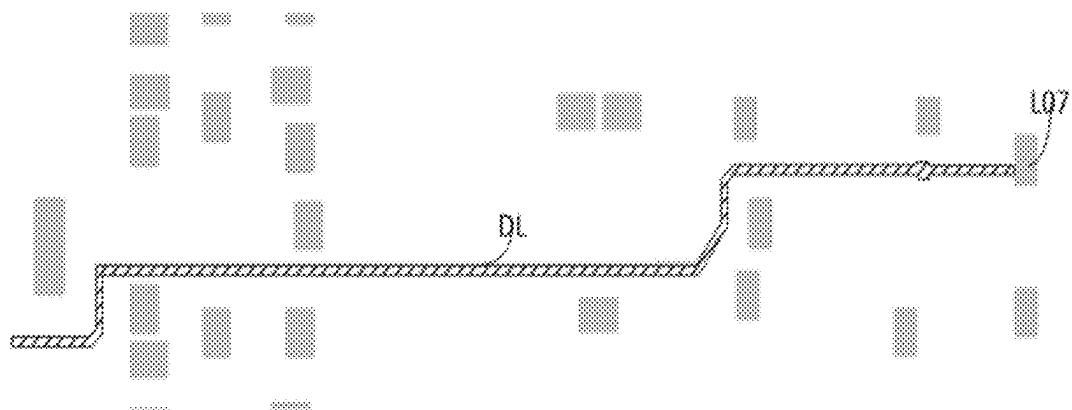


FIG. 49

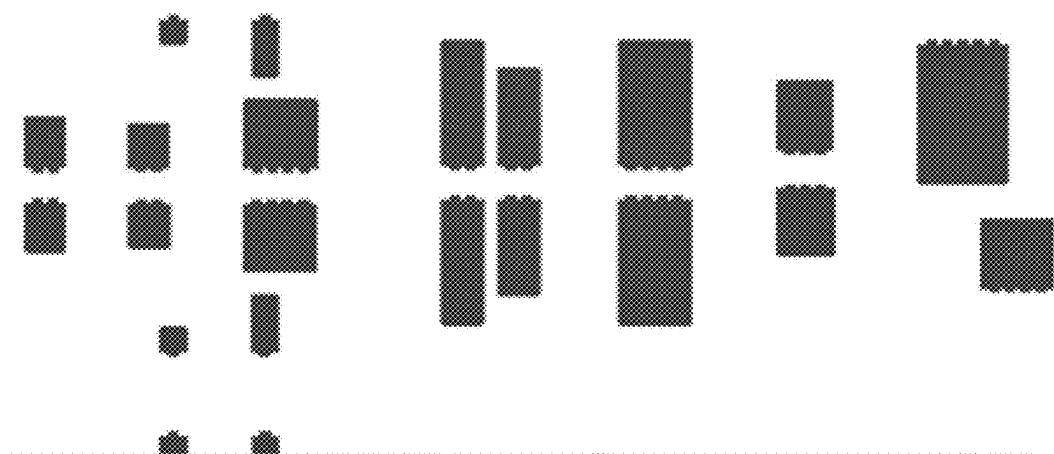


FIG. 50

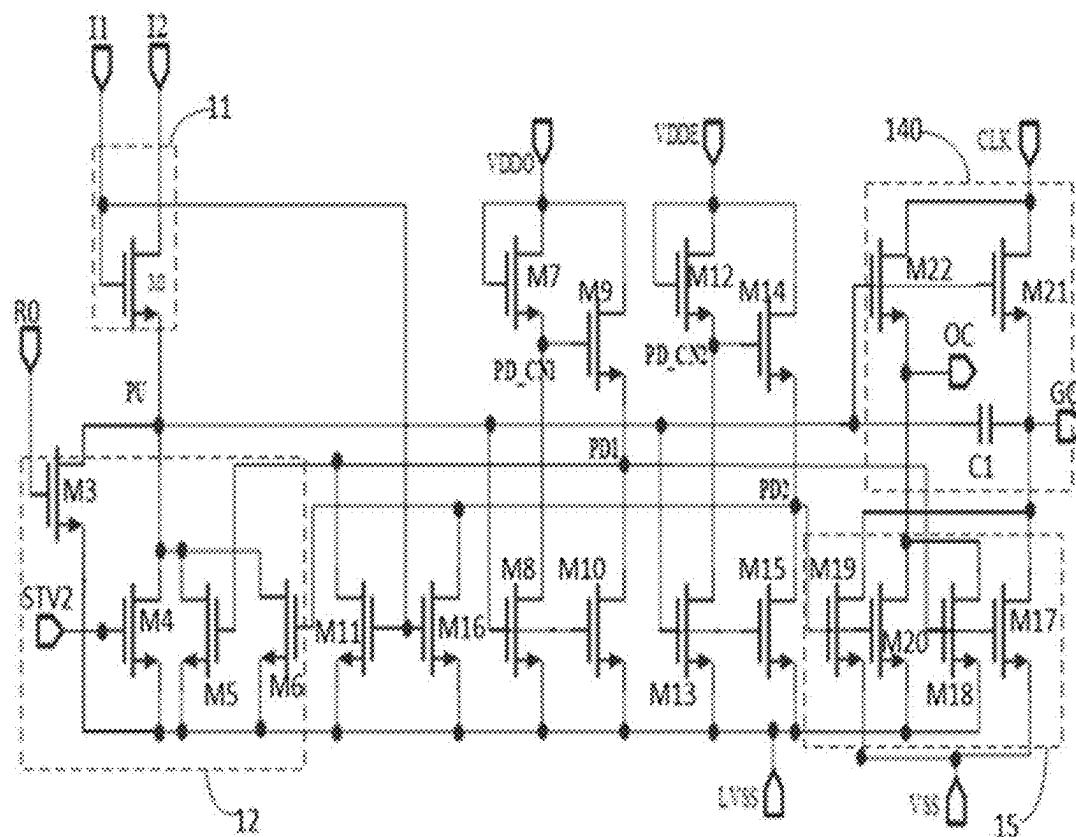


FIG. 51

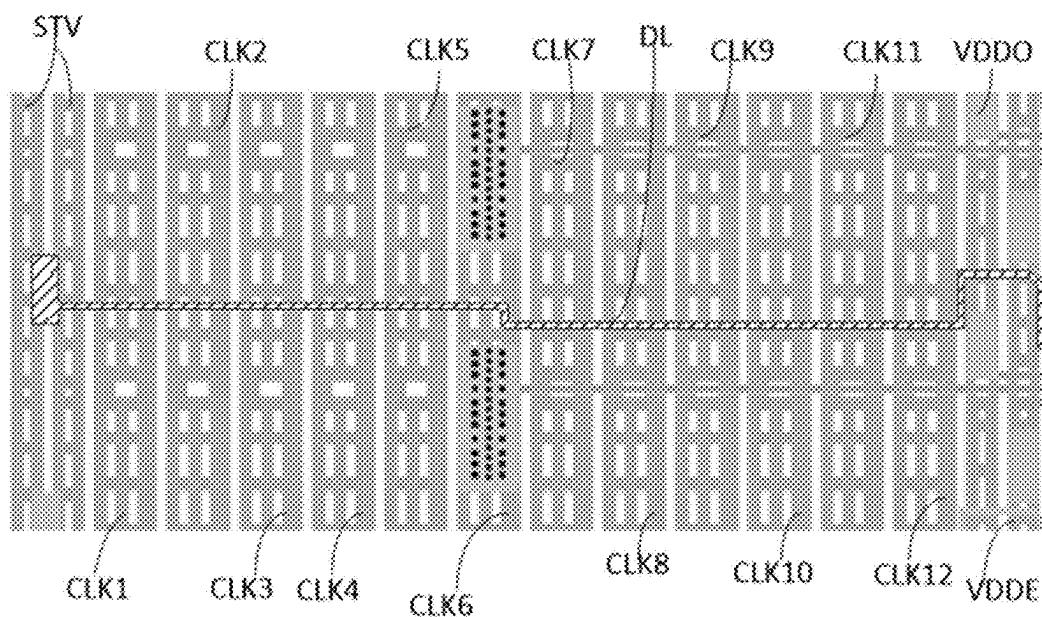


FIG. 52

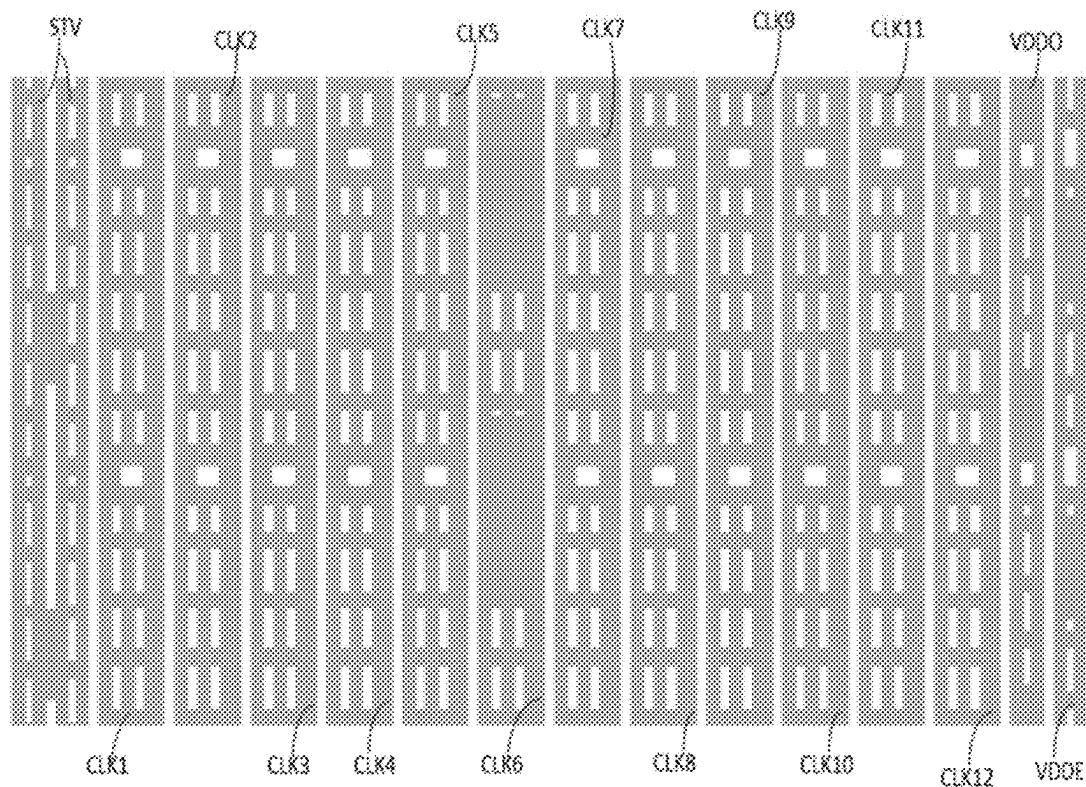
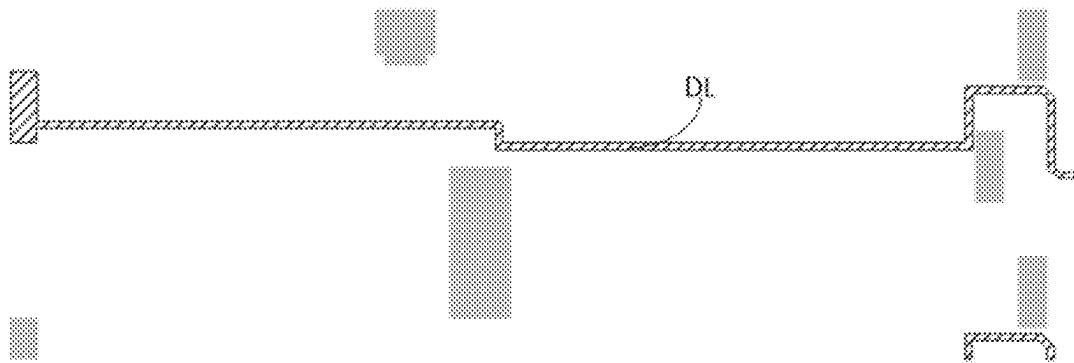


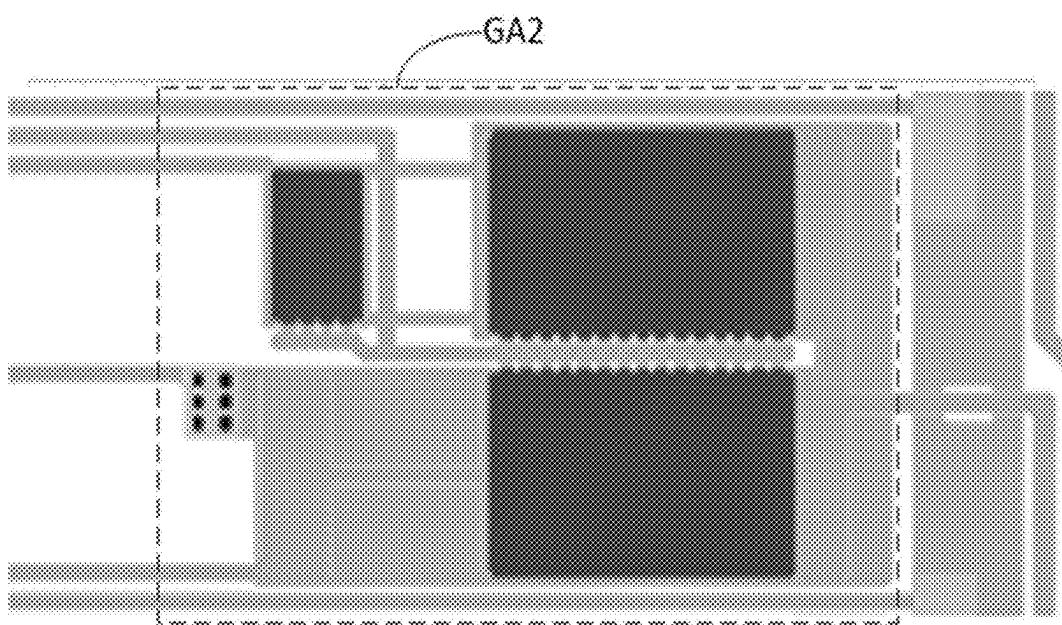
FIG. 53



FIG. 54



**FIG. 55**



**FIG. 56**

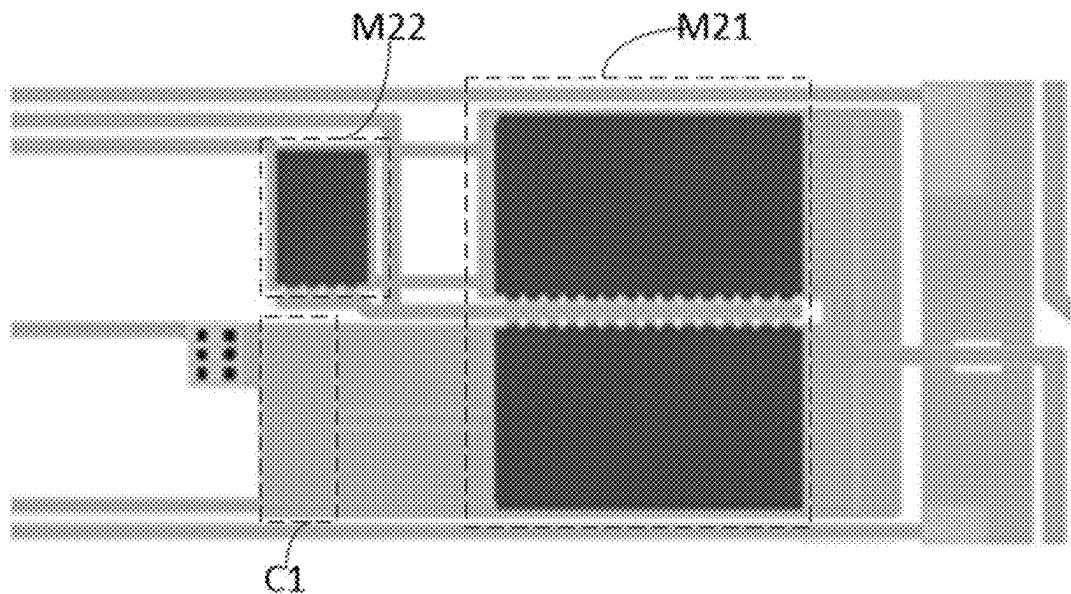


FIG. 57

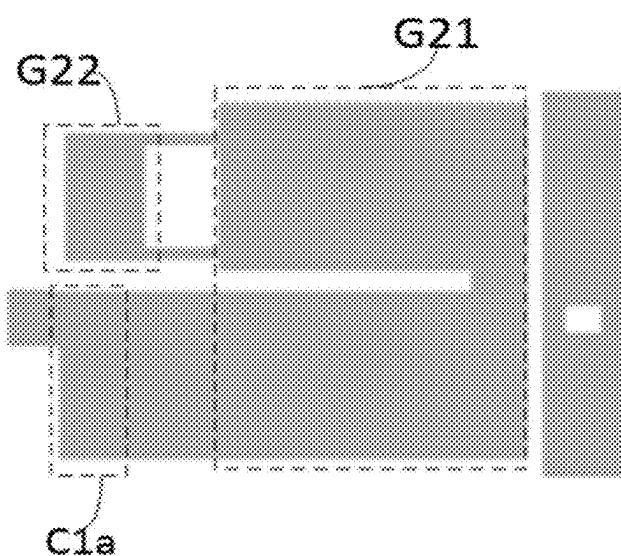
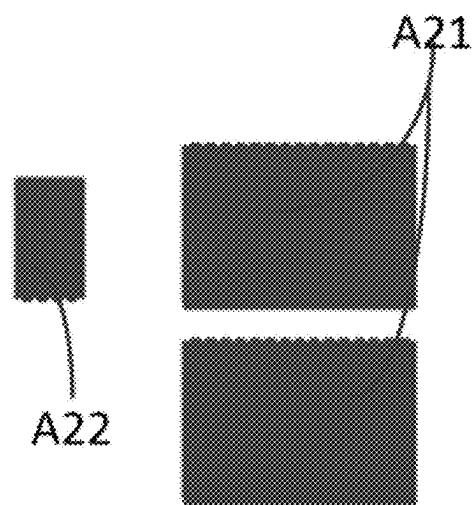
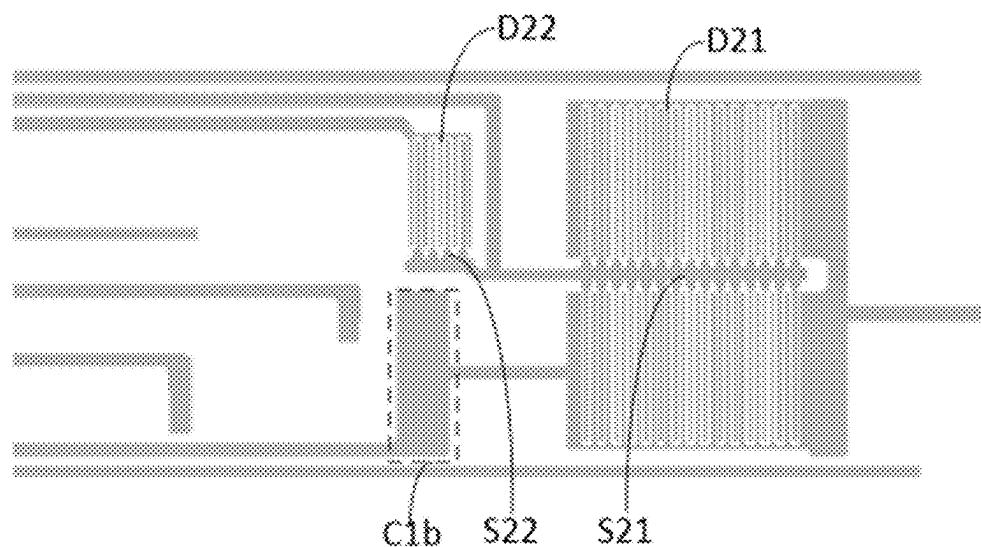


FIG. 58



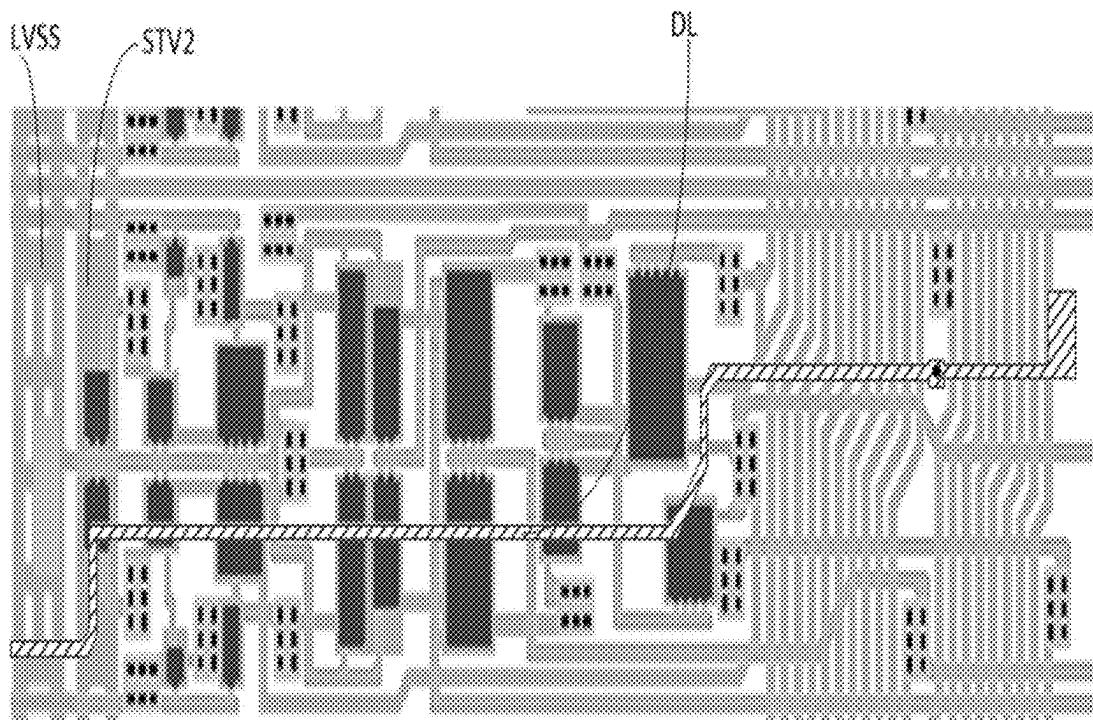
**FIG. 59**



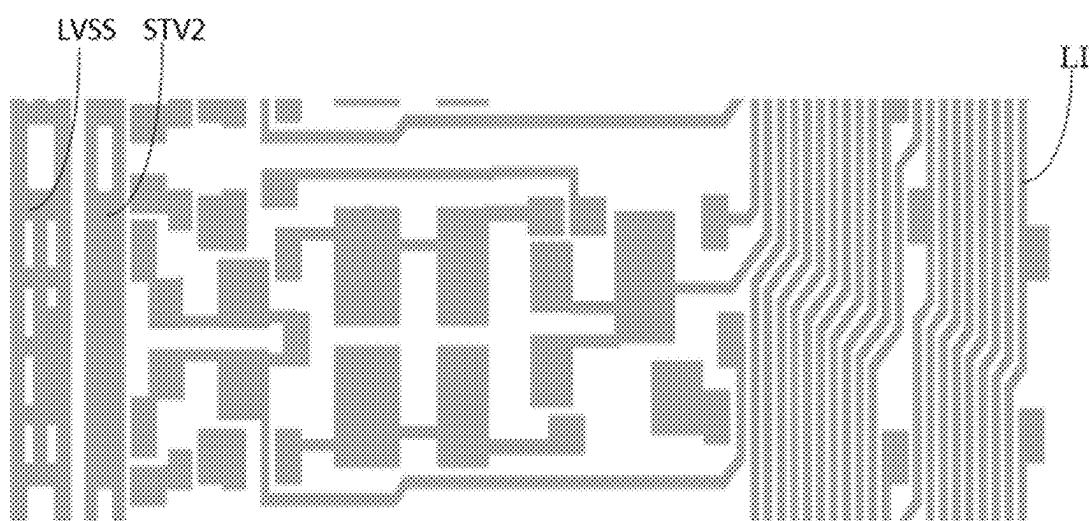
**FIG. 60**



**FIG. 61**



**FIG. 62**



**FIG. 63**

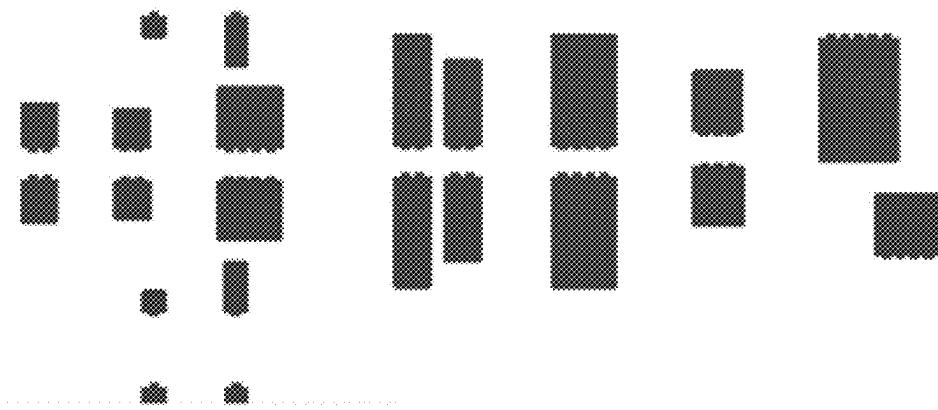


FIG. 64

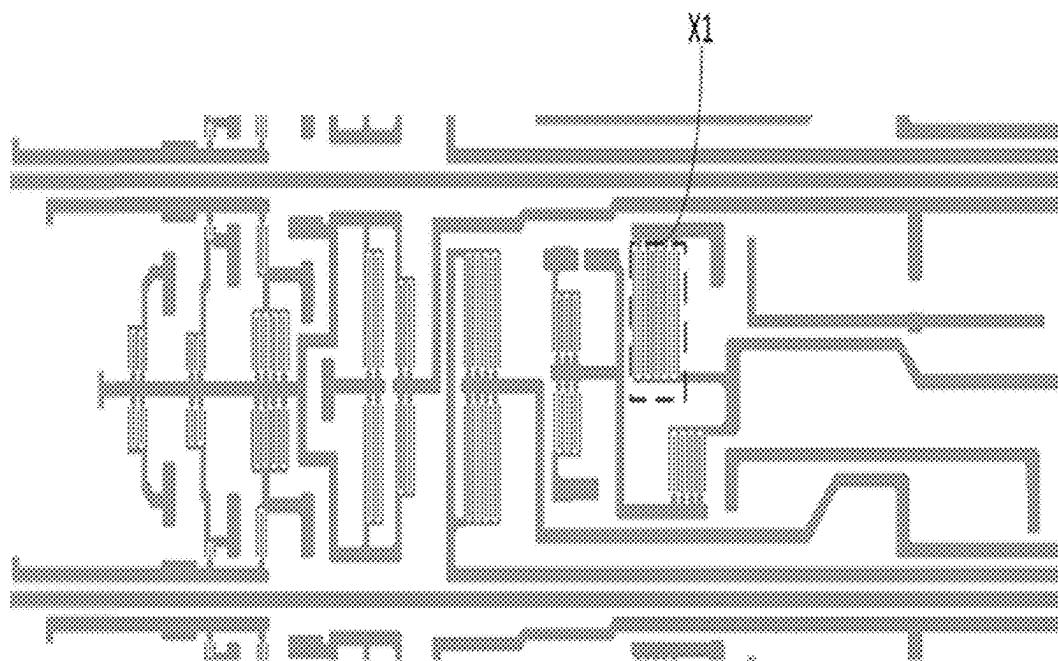
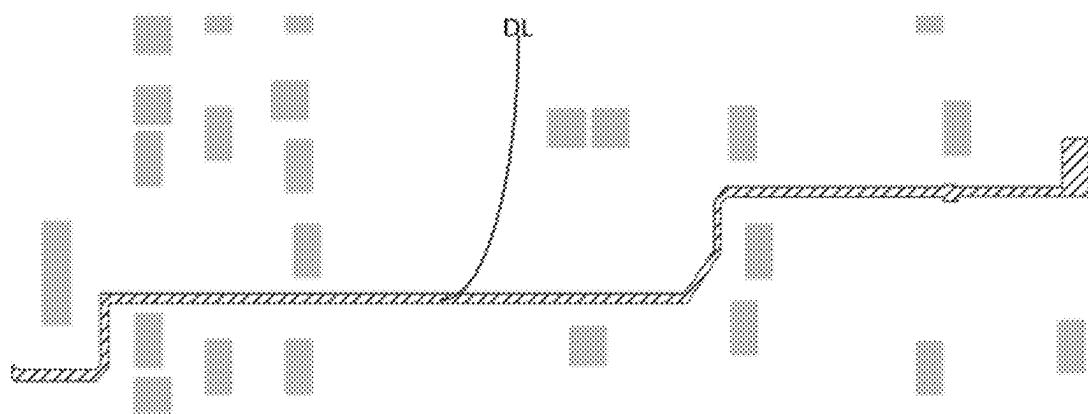


FIG. 65



**FIG. 66**

## DISPLAY PANEL, REPAIRING METHOD AND DISPLAY DEVICE

### TECHNICAL FIELD

[0001] The present disclosure relates to the field of display technology, in particular to a display panel, a repairing method and a display device.

### BACKGROUND

[0002] In the related art, when a large-sized display substrate needs to be cut to form a small-sized display substrate, the start voltage is output by the timing controller (TCON) and then output to the level shifter. The start voltage line is used to provide an start signal to the gate driving circuit of the display panel. TCON is set in the driving integrated circuit (IC). The start voltage line extends from the side of the driving IC to the side away from the driving IC, then if horizontal cutting is performed (the horizontal direction is the extension direction of the gate lines), the start voltage line will be cut off, so that the display substrate obtained after cutting cannot work properly.

### SUMMARY

[0003] In one aspect, the present disclosure provides in some embodiments a display substrate, including a base substrate and a driving module arranged on the base substrate; wherein the driving module includes a control switch and N cascaded driving circuits; the driving circuit includes an input terminal; N is a positive integer; input terminals of previous a stages of driving circuits included in the driving module is electrically connected to a start voltage line; a is a positive integer; an input terminal of an nth stage of driving circuit included in the driving module is electrically connected to an output terminal of an  $(n-m)$ th stage of driving circuit included in the driving module through an input cascade line; n and m are positive integers, and m is less than n; the driving module further includes at least one connection line, the connection line extends along a first direction; there is an overlapping area between an orthographic projection of the connection line on the base substrate and an orthographic projection of the start voltage line on the base substrate; and/or, there is an overlapping area between the orthographic projection of the connection line on the base substrate and an orthographic projection of the input cascade line on the base substrate; the control switch is electrically connected to the connection line.

[0004] Optionally, at least part of the connection line and the start voltage line are located on different layers, and at least part of the connection line and the input cascade line are located on different layers.

[0005] Optionally, the connection line is provided between two adjacent driving circuits; or the connection line penetrates at least part of the driving circuit.

[0006] Optionally, the driving module includes a plurality of clock signal lines, a plurality of stages of driving circuits and a line collection portion; the driving circuit includes a first driving circuit portion and a second driving circuit portion; the plurality of clock signal lines, the first driving circuit portion, the line collection portion and the second driving circuit portion are arranged in sequence along a direction close to a display area; the input cascade line is

provided in the line collection portion; the driving circuit includes the first driving circuit portion and the second driving circuit portion.

[0007] Optionally, the control switch includes a control line and a control module; the control module is electrically connected to the control line, the start voltage line, the connection line and the line collection portion respectively, and is configured to control to connect or disconnect the connection line and the line collection portion under the control of a control signal provided by the control line; there is an overlapping area between the orthographic projection of the connection line on the base substrate and the orthographic projection of the line collection portion on the base substrate.

[0008] Optionally, the control module is electrically connected to the input cascade line in the line collection portion; the control module includes at least one control sub-module; a control sub-module corresponding to the nth stage of driving circuit included in the driving module is electrically connected to an input terminal of the  $(n+j)$ th stage of driving circuit through the input cascade line; j is a positive integer.

[0009] Optionally, the control line includes a first control line and a second control line, and the control sub-module includes a first control circuit and a second control circuit; the first control circuit is electrically connected to the first control line, the start voltage line and the connection line respectively, and is configured to control to connect or disconnect the start voltage line and the connection line under the control of a first control signal provided by the first control line; the second control circuit is electrically connected to the second control line, the connection line and the input cascade line respectively, and is configured to control to connect or disconnect the connection line and the input cascade line under the control of a second control signal provided by the second control line.

[0010] Optionally, the driving module includes a plurality of connection lines; the connection lines are provided between adjacent two stage of driving circuits; a first terminal of the connection line is electrically connected to the first control circuit, and a second terminal of the connection line is electrically connected to the second control circuit; the first terminal and the second terminal are opposite terminals.

[0011] Optionally, the first control circuit includes a first control transistor, and the second control circuit includes a second control transistor; a gate electrode of the first control transistor is electrically connected to a first electrode of the first control transistor, the gate electrode of the first control transistor is electrically connected to the first control line, and the first electrode of the first control transistor is electrically connected to the first terminal of the connection line, and a second electrode of the first control transistor is electrically connected to the start voltage line; a gate electrode of the second control transistor is electrically connected to the second control line, a first electrode of the second control transistor is electrically connected to the second terminal of the connection line, and a second electrode of the second control transistor is electrically connected to the input cascade line.

[0012] Optionally, the first control circuit includes a first control transistor, and the second control circuit includes a second control transistor; a gate electrode of the first control transistor is electrically connected to the first control line, a first electrode of the first control transistor is electrically

connected to the first terminal of the connection line, and a second electrode of the first control transistor is electrically connected to the start voltage line; a gate electrode of the second control transistor is electrically connected to the second control line, a first electrode of the second control transistor is electrically connected to the second terminal of the connection line, and a second electrode of the second control transistor is electrically connected to the input cascade line.

[0013] Optionally, the control line includes a second control line, and the control sub-module includes a second control circuit; the connection line is electrically connected to the start voltage line; the second control circuit is electrically connected to the second control line, the connection line and the input cascade line respectively, and is configured to control to connect or disconnect the connection line and the input cascade line under the control of the second control signal provided by the second control line.

[0014] Optionally, the driving module includes a plurality of connection lines; the plurality of connection lines are arranged between adjacent two stage of driving circuits; a first terminal of the connection line is electrically connected to the start voltage line, and a second terminal of the connection line is electrically connected to the second control circuit; the first terminal and the second terminal are opposite terminals.

[0015] Optionally, the second control circuit includes a second control transistor; a gate electrode of the second control transistor is electrically connected to the second control line, a first electrode of the second control transistor is electrically connected to the second terminal of the connection line, and a second electrode of the second control transistor is electrically connected to the input cascade line.

[0016] Optionally, the control line includes a first control line, and the control sub-module includes a first control circuit; the first control circuit is electrically connected to the first control line, the start voltage line and the connection line respectively, and is configured to control to connect or disconnect the connection line and the start voltage line under the control of the first control signal provided by the first control line; the connection line is electrically connected to the input cascade line.

[0017] Optionally, the driving module includes a plurality of connection lines; the plurality of connection lines are arranged between adjacent two stage of driving circuits; the first terminal of the connection line is electrically connected to the first control circuit, and the second terminal of the connection line is electrically connected to the input cascade line; the first terminal and the second terminal are opposite terminals.

[0018] Optionally, the first control circuit includes a first control transistor; a gate electrode of the first control transistor is electrically connected to the first control line, a first electrode of the first control transistor is electrically connected to the start voltage line, and a second electrode of the first control transistor is electrically connected to the first terminal of the connection line.

[0019] Optionally, the connection line included in the driving module penetrates the clock signal line included in the driving circuit, the first driving circuit portion and the line collection portion in a direction from away from the display area to close to the display area.

[0020] Optionally, the display substrate includes a first metal layer and an electrode layer sequentially arranged in

a direction away from the base substrate; the connection line includes a first line portion formed on the electrode layer and a second line portion formed on the first metal layer; the first line portion and the second line portion are electrically connected; at least part of the first line portion is provided in a clock signal line area, the first driving circuit portion and the line collection portion; the clock signal line area is an area where the plurality of clock signal lines are provided; at least part of the second line portion is provided on the line collection portion.

[0021] Optionally, the driving circuit includes an input circuit; the input circuit includes a control terminal, a first terminal and a second terminal; the control terminal of the input circuit is electrically connected to the input terminal, and the second terminal of the input circuit is electrically connected to a pull-up node; the input circuit is configured to control a potential of the pull-up node under the control of an input signal provided by the input terminal.

[0022] Optionally, the input circuit includes a first transistor; a gate electrode of the first transistor is electrically connected to the first input terminal, a first electrode of the first transistor is electrically connected to the second input terminal, and a second electrode of the first transistor is electrically connected to the pull-up node; the first input terminal and the second input terminal are electrically connected or not electrically connected.

[0023] Optionally, the gate electrode of the first transistor is formed on the second metal layer, and the first electrode of the first transistor is formed on the first metal layer; the gate electrode of the first transistor is electrically connected to the first connection line portion formed on the second metal layer; the first electrode of the first transistor is electrically connected to the second connection line portion formed in the second metal layer through a via hole; the connection line includes a third connection line portion formed on the electrode layer and a fourth connection line portion formed on the first metal layer; the third connection line portion and the fourth connection line portion are electrically connected; there is an overlapping area between an orthographic projection of the third connection line portion on the base substrate and an orthographic projection of the first connection line portion on the base substrate; there is an overlapping area between an orthographic projection of the fourth connection line portion on the base substrate and an orthographic projection of the second connection line portion on the base substrate.

[0024] Optionally, the display substrate further includes a fifth connection line portion and a sixth connection line portion; the fifth connection line portion is formed on the electrode layer, and the fifth connection line portion is connected to the third connection line portion; the sixth connection line portion is formed on the first metal layer, and the sixth connection line portion is connected to the fourth connection line portion; the fifth connection line portion and the sixth connection line portion are electrically connected.

[0025] Optionally, the driving circuit includes a first driving circuit portion; the first driving circuit portion includes an input circuit, a pull-up node control circuit, a first pull-down node control circuit, a second pull-down node control circuit and a reset circuit; the input circuit is configured to control a potential of the pull-up node under the control of an input signal provided by the input terminal; the pull-up node control circuit is configured to control the potential of the pull-up node; the first pull-down node

control circuit is configured to control a potential of the first pull-down node; the second pull-down node control circuit is configured to control a potential of the second pull-down node; the reset circuit is configured to reset the driving signal provided by the driving signal output terminal of the current stage under the control of the potential of the first pull-down node and the potential of the second pull-down node.

[0026] In a second aspect, an embodiment of the present disclosure provides a display substrate, including a base substrate and a driving module arranged on the base substrate; wherein the driving module includes N cascaded driving circuits; the driving circuit includes an input terminal; N is a positive integer; input terminals of previous a stages of driving circuits included in the driving module are electrically connected to a start voltage line; a is a positive integer; an input terminal of an nth stage of driving circuit included in the driving module is electrically connected to an output terminal of the  $(n-m)$ th stage of driving circuit included in the driving module through an input cascade line; n and m are positive integers, and m is less than n; the driving module also includes at least one connection line, the connection line extends along a first direction; there is an overlapping area between an orthographic projection of the connection line on the base substrate and an orthographic projection of the start voltage line on the base substrate; there is an overlap area between the orthographic projection of the connection line on the base substrate and an orthographic projection of the input cascade line on the base substrate.

[0027] In a third aspect, an embodiment of the present disclosure provides a repairing method, applied to the display substrate and includes: when previous c stages of driving circuits included in the driving module in the display substrate are cut off, controlling, by the control switch, to connect the connection line and the input cascade line; the input cascade line being electrically connected to an input terminal of a  $(c+k)$ th stage of driving circuit; both c and k are positive integers.

[0028] Optionally, the control switch includes a control module and a control line; the control line includes a first control line and the second control line, the control module includes at least one control sub-module, the control sub-module includes a first control circuit and a second control circuit; the repairing method includes: when the first c stages of driving circuits included in the driving module in the display substrate are cut off, a connection line close to the  $(c+p)$ th stage of driving circuit being used to transmit the start voltage signal; disconnecting a first control line between a first control circuit corresponding to a  $(c+p)$ th stage of driving circuit from a first control circuit corresponding to a  $(c+p+1)$ th stage of driving circuit; disconnecting the second control line between the second control circuit corresponding to the  $(c+p)$ th stage of driving circuit from the second control circuit corresponding to the  $(c+p+1)$ th stage of driving circuit; p is a positive integer greater than or equal to 1.

[0029] Optionally, the control switch includes a control module and a control line; the control line includes a second control line, and the control module includes at least one control sub-module, the control sub-module includes a second control circuit; the repair method includes: when the first c stages of driving circuits included in the driving module in the display substrate are cut off, the connection line close to the  $(c+p)$ th stage of driving circuit being used

to transmit the start voltage signal; disconnecting the second control line between the second control circuit corresponding to the  $(c+p)$ th stage of driving circuit and the second control circuit corresponding to the  $(c+p+1)$ th stage of driving circuit; p is a positive integer greater than or equal to 1.

[0030] Optionally, the control switch includes a control module and a control line; the control line includes a first control line, and the control module includes at least one control sub-module, the control sub-module includes a first control circuit; the repair method includes: when the first c stages of driving circuits included in the driving module in the display substrate are cut off, the connection line close to the  $(c+p)$ th stage of driving circuit being used to transmit the start voltage signal; disconnecting the first control line between the first control circuit corresponding to the  $(c+p)$ th stage of driving circuit and the first control circuit corresponding to the  $(c+p+1)$ th stage of driving circuit; p is a positive integer greater than or equal to 1.

[0031] In a fourth aspect, an embodiment of the present disclosure provides a display device, including the display substrate.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0032] FIG. 1 is a structural diagram of six stages of driving circuits included in a related driving module;

[0033] FIG. 2 is a structural diagram of a driving module in a display substrate according to at least one embodiment of the present disclosure;

[0034] FIG. 3 is a structural diagram of a driving module in a display substrate according to at least one embodiment of the present disclosure;

[0035] FIG. 4 is a structural diagram of a driving module in a display substrate according to at least one embodiment of the present disclosure;

[0036] FIG. 5A is a structural diagram of a driving module in a display substrate according to at least one embodiment of the present disclosure;

[0037] FIG. 5B is a structural diagram of a control module in a display substrate according to at least one embodiment of the present disclosure;

[0038] FIG. 6A is a structural diagram of a driving module in a display substrate according to at least one embodiment of the present disclosure;

[0039] FIG. 6B is a structural diagram of a control module in a display substrate according to at least one embodiment of the present disclosure;

[0040] FIG. 7 is a structural diagram of a driving module in a display substrate according to at least one embodiment of the present disclosure;

[0041] FIG. 8A is a structural diagram of a driving module in a display substrate according to at least one embodiment of the present disclosure;

[0042] FIG. 8B is a structural diagram of a control module in a display substrate according to at least one embodiment of the present disclosure;

[0043] FIG. 9 is a structural diagram of a driving module in a display substrate according to at least one embodiment of the present disclosure;

[0044] FIG. 10A is a structural diagram of a driving module in a display substrate according to at least one embodiment of the present disclosure;

- [0045] FIG. 10B is a structural diagram of a control module in a display substrate according to at least one embodiment of the present disclosure;
- [0046] FIG. 11 is a layout diagram of the second driving circuit portion in the driving module shown in FIG. 5B;
- [0047] FIG. 12 is a layout diagram of the first driving circuit portion and the line collection portion of the driving module included in the display substrate according to at least one embodiment of the present disclosure;
- [0048] FIG. 13 is a layout diagram of the gate metal layer in FIG. 12;
- [0049] FIG. 14 is a layout diagram of the source-drain metal layer in FIG. 12;
- [0050] FIG. 15 is a layout diagram of the electrode layer in FIG. 12.
- [0051] FIG. 16 is a layout diagram of the active layer in FIG. 12;
- [0052] FIG. 17 is a schematic diagram showing labels for the first driving circuit portion, the line collection portion and the connection lines added on the basis of FIG. 12;
- [0053] FIG. 18 is a schematic diagram showing labels for each transistor added on the basis of FIG. 12;
- [0054] FIG. 19 is a layout diagram of the electrode layer in the first driving circuit portion of the driving module included in the display substrate according to at least one embodiment of the present disclosure;
- [0055] FIG. 20 is a layout diagram of the second driving circuit portion;
- [0056] FIG. 21 is a layout diagram of the gate metal layer in FIG. 20;
- [0057] FIG. 22 is a layout diagram of the active layer in FIG. 20;
- [0058] FIG. 23 is a layout diagram of the source-drain metal layer in FIG. 20;
- [0059] FIG. 24 is a layout diagram of the electrode layer in FIG. 20;
- [0060] FIG. 25 is a layout diagram of each clock signal line of the driving module included in the display substrate according to at least one embodiment of the present disclosure;
- [0061] FIG. 26 is a layout diagram of the gate metal layer in FIG. 25;
- [0062] FIG. 27 is a layout diagram of the source-drain metal layers in FIG. 25;
- [0063] FIG. 28 is a layout diagram of the electrode layer in FIG. 25;
- [0064] FIG. 29 is a layout diagram of the active layer in FIG. 25;
- [0065] FIG. 30 is a layout diagram of each clock signal line of the driving module included in the display substrate according to at least one embodiment of the present disclosure;
- [0066] FIG. 31 is a layout diagram of the gate metal layer in FIG. 30;
- [0067] FIG. 32 is a layout diagram of the source-drain metal layers in FIG. 30;
- [0068] FIG. 33 is a layout diagram of the electrode layer in FIG. 30;
- [0069] FIG. 34 is a layout diagram of the active layer in FIG. 30;
- [0070] FIG. 35 is a layout diagram of each clock signal line of the driving module included in the display substrate according to at least one embodiment of the present disclosure;
- [0071] FIG. 36 is a layout diagram of the gate metal layer in FIG. 35;
- [0072] FIG. 37 is a layout diagram of the source-drain metal layers in FIG. 35;
- [0073] FIG. 38 is a layout diagram of the electrode layer in FIG. 35;
- [0074] FIGS. 39 and 40 are layout diagrams of the second driving circuit portion in the driving module shown in FIG. 10B;
- [0075] FIG. 41 is a layout diagram of the gate metal layer in FIG. 40;
- [0076] FIG. 42 is a layout diagram of the active layer in FIG. 40;
- [0077] FIG. 43 is a layout diagram of the source-drain metal layers in FIG. 40;
- [0078] FIG. 44 is a layout diagram of the electrode layer in FIG. 40;
- [0079] FIG. 45 is a layout diagram of the first driving circuit portion and the wiring portion in the driving module shown in FIG. 10B;
- [0080] FIG. 46 is a schematic diagram showing labels of each transistor added based on the layout diagram shown in FIG. 45;
- [0081] FIG. 47 is a layout diagram of the gate metal layer in FIG. 46;
- [0082] FIG. 48 is a layout diagram of the source-drain metal layers in FIG. 46;
- [0083] FIG. 49 is a layout diagram of the electrode layer in FIG. 46;
- [0084] FIG. 50 is a layout diagram of the active layer in FIG. 46;
- [0085] FIG. 51 is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;
- [0086] FIG. 52 is a layout diagram of each clock signal line of the driving module included in the display substrate when the display substrate does not include a control switch;
- [0087] FIG. 53 is a layout diagram of the gate metal layer in FIG. 52;
- [0088] FIG. 54 is a layout diagram of the source-drain metal layers of FIG. 52;
- [0089] FIG. 55 is a layout diagram of the electrode layer in FIG. 52;
- [0090] FIGS. 56 and 57 are layout diagrams of the second driving circuit portion of the driving module included in the display substrate when the display substrate does not include a control switch;
- [0091] FIG. 58 is a layout diagram of the gate metal layer in FIG. 57;
- [0092] FIG. 59 is a layout diagram of the active layer in FIG. 57;
- [0093] FIG. 60 is a layout diagram of the source-drain metal layers in FIG. 57;
- [0094] FIG. 61 is a layout diagram of the electrode layer in FIG. 57;
- [0095] FIG. 62 is a layout diagram of the first driving circuit portion and the line collection portion of the driving module included in the display substrate when the display substrate does not include a control switch;
- [0096] FIG. 63 is a layout diagram of the gate metal layer in FIG. 62;
- [0097] FIG. 64 is a layout diagram of the active layer in FIG. 62;

[0098] FIG. 65 is a layout diagram of the source-drain metal layers in FIG. 62;

[0099] FIG. 66 is a layout diagram of the electrode layer in FIG. 62.

#### DETAILED DESCRIPTION

[0100] The technical solutions in the embodiments of the present disclosure will be clearly and completely described below with reference to the accompanying drawings in the embodiments of the present disclosure. Obviously, the described embodiments are only some of the embodiments of the present disclosure, rather than all of the embodiments. Based on the embodiments in the present disclosure, all other embodiments obtained by those of ordinary skill in the art without making creative efforts fall within the scope of protection of the present disclosure.

[0101] The transistors used in all embodiments of the present disclosure may be thin film transistors, field effect transistors, or other devices with the same characteristics. In the embodiment of the present disclosure, in order to distinguish the two electrodes of the transistor except the gate electrode, one electrode is called the first electrode and the other electrode is called the second electrode.

[0102] In actual operation, when the transistor is a thin film transistor or a field effect transistor, the first electrode may be a drain electrode, and the second electrode may be a source electrode; or, the first electrode may be a source electrode, the second electrode may be a drain electrode.

[0103] The display substrate according to the embodiment of the present disclosure includes a base substrate and a driving module arranged on the base substrate; the driving module includes a control switch and N cascaded driving circuits; the driving circuit includes an input terminal; N is a positive integer;

[0104] The input terminals of the previous a stages of driving circuits included in the driving module is electrically connected to an start voltage line; a is a positive integer;

[0105] The input terminal of the nth stage of driving circuit included in the driving module is electrically connected to an output terminal of the (n-m)th stage of driving circuit included in the driving module through an input cascade line; n and m are positive integers, and m is less than n;

[0106] The driving module also includes at least one connection line, the connection line extending along a first direction;

[0107] There is an overlapping area between an orthographic projection of the connection line on the base substrate and an orthographic projection of the start voltage line on the base substrate; and/or, there is an overlapping area between the orthographic projection of the connection line on the base substrate and an orthographic projection of the input cascade line on the base substrate;

[0108] The control switch is electrically connected to the connection line.

[0109] In at least one embodiment of the present disclosure, the control switch may include a control module and a control line.

[0110] In specific implementation, when the first c stages of driving circuits included in the driving module in the display substrate is cut off, the control switch controls the connection line and the input cascade line to communicate

with each other, so that the start voltage line can be connected to an input terminal of the (c+k)th stage of driving circuit;

[0111] The input cascade line is electrically connected to the input terminal of the (c+k)th stage of driving circuit;

[0112] Both c and k are positive integers.

[0113] In at least one embodiment of the present disclosure, when k is greater than 1, no input signal is connected from the input terminal of the (c+1)th stage of driving circuit to the input terminal of the (c+k-1)th stage of driving circuit. A frame sealing glue is provided at the position from the (c+1)th stage of driving circuit to the (c+k-1)th stage of driving circuit.

[0114] In at least one embodiment of the present disclosure, the start voltage line includes a portion extending along the second direction, and the start signal on the start voltage line is transmitted from a side close to the Nth stage of driving circuit in the driving module to the side close to the first stage of driving circuit in the driving module; the second direction is the direction from the Nth stage of driving circuit to the first stage of driving circuit.

[0115] In at least one embodiment of the present disclosure, the first direction may intersect with the second direction.

[0116] In at least one embodiment of the present disclosure, the driving module may be a gate driving module, and the driving circuit may be a gate driving circuit, but is not limited thereto.

[0117] In specific implementation, the start voltage is output by TCON (timing controller) and then output to the start voltage line through the level shifter. TCON is set in the driver IC. The start voltage line extends from the side of the driver IC to the side away from the driver IC.

[0118] In at least one embodiment of the present disclosure, at least part of the connection lines and the start voltage line are located on different layers, and at least part of the connection lines and the input cascade line are located on different layers.

[0119] In specific implementation, at least part of the connection lines and the start voltage line are located on different layers, so that when repair is required, the connection lines and the start voltage line can be electrically connected by welding or other means; at least part of the connection lines and the input cascade lines are located on different layers, so that when repair is required, the connection lines can be electrically connected to the input cascade lines by welding or other means.

[0120] Optionally, the connection line is provided between two adjacent driving circuits; or, the connection line penetrates at least part of the driving circuit.

[0121] It should be noted that in the present disclosure, the connection line is arranged between two adjacent driving circuits, which may include the case where the connection line is arranged between the two driving circuits and does not overlap with the two driving circuits, and also includes the case where the connection line partially overlaps one driving circuit, and may include the case where the driving circuit partially overlaps one driving circuit and partially overlaps the other driving circuit at the same time. The overlap here refers to the overlap with the transistors or signal lines included in the driving circuit.

[0122] As shown in FIG. 1, the one labeled SY1 is the first stage of driving circuit in the driving module, the one labeled SY2 is the second stage of driving circuit in the

driving module, and the one labeled SY3 is the third stage of driving circuit in the driving module, the one labeled SY4 is the fourth stage of driving circuit in the driving module, the one labeled SY5 is the fifth stage of driving circuit in the driving module, and the one labeled SY6 is the sixth stage of driving circuit in the driving module.

[0123] In at least one embodiment shown in FIG. 1, the line labeled STV is the start voltage line;

[0124] A first connection line DL1 is provided between SY1 and SY2, a second connection line DL2 is provided between SY2 and SY3, a third connection line DL3 is provided between SY3 and SY4, and a fourth connection line DL4 is provided between SY4 and SY5 and the fifth connection line DL5 is provided between SY5 and SY6.

[0125] The input terminals of SY1 and SY2 are electrically connected to the start voltage line STV through the start voltage input line LI0 (here it is only shown that the start voltage input line is electrically connected to the first two stages of gate driving circuits, and it can also be only electrically connected to the first stage of gate driving circuit, or to other multiple stages of gate driving circuits, such as the first 3 stages, the first 4 stages, etc., which are not limited here);

[0126] The input terminal of SY3 is electrically connected to the output terminal of SY1 through the first input cascade line LI1;

[0127] The input terminal of SY4 is electrically connected to the output terminal of SY2 through the second input cascade line LI2;

[0128] The input terminal of SY5 is electrically connected to the output terminal of SY3 through the third input cascade line LI3;

[0129] The input terminal of SY6 is electrically connected to the output terminal of SY4 through the fourth input cascade line LI4;

[0130] It should be noted that the input terminal here may refer to the gate electrode of the input transistor of the gate driving circuit, and/or, the first electrode of the input transistor, and the second electrode of the input transistor is electrically connected to the pull-up node of the gate driving circuit; the output terminal here can refer to the output terminal of the gate driving circuit, which can be GO (GO is the current stage of driving signal output terminal, that is, the output terminal that is electrically connected to the gate line of the display area), it can also be the output terminal OC responsible for cascading, carry and reset (OC is the current stage of carry signal output terminal). For example, refer to the gate driving circuit in FIG. 51, which is not limited here.

[0131] There is an overlapping area between the orthographic projection of DL1 on the base substrate and the orthographic projection of LI1 on the base substrate;

[0132] There is an overlapping area between the orthographic projection of DL2 on the base substrate and the orthographic projection of LI1 on the base substrate, and there is an overlapping area between the orthographic projection of DL2 on the base substrate and the orthographic projection of LI2 on the base substrate;

[0133] There is an overlapping area between the orthographic projection of DL3 on the base substrate and the orthographic projection of LI2 on the base substrate, and there is an overlapping area between the orthographic projection of DL3 on the base substrate and the orthographic projection of LI3 on the base substrate;

[0134] There is an overlapping area between the orthographic projection of DL4 on the base substrate and the orthographic projection of LI3 on the base substrate, and there is an overlapping area between the orthographic projection of DL3 on the base substrate and the orthographic projection of LI4 on the base substrate;

[0135] There is an overlapping area between the orthographic projection of DL5 on the base substrate and the orthographic projection of LI4 on the base substrate.

[0136] It should be noted that the number of start voltage lines, the number of driving circuits, the cascade relationship, etc. in FIG. 1 are schematic illustrations, and the specific number and cascade relationship can be set according to actual conditions.

[0137] It should be noted that in this case, connection lines can be set between two adjacent stages of driving circuits, or the display can be divided into areas, and connection lines can be set between areas and areas. For example, when the driving module includes forty stages of driving circuits, (the first stage of driving circuit SY1 to the fortieth stage of driving circuit SY40), there can be no connection line between SY1-SY20 (SY20 is the twentieth stage of driving circuit), and there is no connection line between SY21 (SY21 is the twenty-first stage of driving circuit)-SY40, there is connection line between SY20 and SY21, that is, the display panel is divided into multiple areas according to actual needs. Each area includes at least two driving circuits, and there are connection lines between areas, the division of specific areas and the number of connection lines can be set according to actual needs, and are not limited here.

[0138] In this case, by cutting the large-size display panel into small-size display panels, that is, the large display panel and the small display panel share a set of design solutions and the same mask, which can reduce the cost of development and mask, such as small-size display panels realized by cutting, without the need to redesign and re-mask. The present disclosure can achieve normal display when a large-sized panel is cut into a small-sized panel.

[0139] In the embodiment shown in FIG. 1, the driving module can be electrically connected to four clock signal lines, but is not limited to this.

[0140] In actual operation, the driving module can be electrically connected to 2 m clock signal lines. At this time, the first m stages of driving circuits included in the driving module are electrically connected to the start voltage line;

[0141] The output terminal of the nth stage of driving circuit of the driving module is electrically connected to the input terminal of the (n+m)th stage of driving circuit;

[0142] Both n and m are positive integers.

[0143] For example, when m is equal to 6, the driving module is electrically connected to twelve clock signal lines, and the output terminal of the nth stage of driving circuit included in the driving module is electrically connected to the input terminal of the (n+6)th stage of driving circuit.

[0144] As shown in FIG. 2, based on at least one embodiment of the display substrate shown in FIG. 1, the driving module may further include a control switch K0;

[0145] The control switch K0 is electrically connected to DL1, DL2, DL3, DL4 and DL5 respectively. In this case, a control switch is set up to connect and disconnect the connection line. When the screen is cut or the STV signal line cannot provide the start signal to the gate driving circuit, the start voltage line is electrically connected to the control switch through the electrical connection between the control

switch and the connection line. When the control switch and the input cascade line are electrically connected, the start voltage signal can be transmitted to any row to achieve normal display.

[0146] In at least one embodiment of the display substrate shown in FIG. 2, K0 is electrically connected to the right terminal of each connection line, but is not limited to this. In actual operation, K0 can also be electrically connected to the left terminal of each connection line, or K0 can also be electrically connected to the left terminal of each connection line and the right terminal of each connection line respectively. The electrical connection in the present disclosure may be a direct electrical connection or an indirect electrical connection, that is, an electrical connection realized through other components such as transistors, resistors, inductors, etc.

[0147] In at least one embodiment of the present disclosure, the driving module includes a plurality of clock signal lines, a plurality of stages of driving circuits and a line collection portion; the driving circuit includes a first driving circuit portion and a second driving circuit portion;

[0148] The plurality of clock signal lines, the first driving circuit portion, the line collection portion and the second driving circuit portion are arranged in sequence along a direction close to the display area;

[0149] The input cascade line is provided in the line collection portion;

[0150] The driving circuit includes the first driving circuit portion and the second driving circuit portion.

[0151] In specific implementation, the driving module may include a plurality of clock signal lines, a multiple stages of driving circuit and a line collection portion. The driving circuit may include a first driving circuit portion and a second driving circuit portion. The plurality of clock signal lines, the first driving circuit portion, the line collecting portion and the second driving circuit portion are arranged in sequence along the direction close to the display area.

[0152] Optionally, the second driving circuit portion includes an output transistor in the driving circuit;

[0153] The first driving circuit portion includes a pull-up node control sub-circuit, a pull-down node control sub-circuit and an output reset sub-circuit; the pull-up node control sub-circuit is used to control the potential of the pull-up node, and the pull-down node control sub-circuit is used to control the potential of the pull-down node, and the output reset sub-circuit is used to reset the driving signal under the control of the potential of the pull-down node.

[0154] In specific implementation, the second driving circuit portion may include a first output transistor and a second output transistor;

[0155] The gate electrode of the first output transistor is electrically connected to the pull-up node, the first electrode of the first output transistor is electrically connected to the output clock signal line, and the second electrode of the first output transistor is electrically connected to the current stage of driving signal output terminal;

[0156] The gate electrode of the second output transistor is electrically connected to the pull-up node, the first electrode of the second output transistor is electrically connected to the output clock signal line, and the second electrode of the second output transistor is connected to the current stage of carry signal output terminal.

[0157] In at least one embodiment of the present disclosure, the connection lines included in the driving module can

penetrate the clock signal lines included in the driving circuit, the first driving circuit portion and the line collection portion in a direction from away from the display area to close to the display area.

[0158] Optionally, the control switch includes a control line and a control module;

[0159] The control module is electrically connected to the control line, the start voltage line, the connection line and the line collection portion respectively, and is used to control to connect or disconnect the connection line and the line collection portion under the control of the control signal provided by the control line;

[0160] There is an overlapping area between the orthographic projection of the connection line on the base substrate and the orthographic projection of the line collection portion on the base substrate.

[0161] As shown in FIG. 3, based on at least one embodiment of the display substrate shown in FIG. 2, the control switch may include a control module 31 and a control line Ct;

[0162] The control module 31 is electrically connected to the control line Ct, the start voltage line STV, the right terminal of DL1, the right terminal of DL2, the right terminal of DL3, the right terminal of DL4 and the right terminal of DL5 respectively;

[0163] The control module 31 can also be electrically connected to the start voltage input line Li0, the first input cascade line Li1, the second input cascade line Li2, the third input cascade line Li3 and the fourth input cascade line Li4 respectively.

[0164] In at least one embodiment of the display substrate shown in FIG. 3, the control line Ct is provided on the right side of the each stage of driving circuit, but is not limited to this. In actual operation, the control line Ct can also be set on the left side of each stage of driving circuit, or the control line can include a first control line and a second control line, and the first control line can be set on the left side of each stage of driving circuit, the second control line may be provided on the right side of each stage of driving circuit.

[0165] In at least one embodiment of the present disclosure, the control module is electrically connected to the input cascade line in the line collection portion; the control module includes at least one control sub-module;

[0166] The control sub-module corresponding to the nth stage of driving circuit included in the driving module is electrically connected to the input terminal of the (n+j)th stage of driving circuit through an input cascade line; j is a positive integer.

[0167] In specific implementation, the control module may include at least one control sub-module, and the control sub-module corresponding to the nth stage of driving circuit may be electrically connected to the input terminal of the (n+j)th stage of driving circuit through an input cascade line, so that when the first n-1 stages of driving circuits in the driving module is cut off, the control sub-module corresponding to the nth stage of driving circuit can be electrically connected to the input terminal of the (n+j)th stage of driving circuit, so that the input terminal of the (n+j)th stage of driving circuit is connected to the start voltage line.

[0168] In at least one embodiment of the present disclosure, the control module may include N control sub-modules, and each stage of driving circuit is provided with one control sub-module; or, the control module may include at least one control sub-module. A control sub-module is

provided corresponding to portion of the driving circuit included in the driving module.

[0169] Optionally, the control line includes a first control line and a second control line, and the control sub-module includes a first control circuit and a second control circuit; [0170] The first control circuit is electrically connected to the first control line, the start voltage line and the connection line respectively, and is used to control to connect or disconnect the start voltage line and the connection line under the control of a first control signal provided by the first control line.

[0171] The second control circuit is electrically connected to the second control line, the connection line and the input cascade line respectively, and is used to control to connect or disconnect the connection line and the input cascade line under the control of the second control signal provided by the second control line.

[0172] As shown in FIG. 4, based on at least one embodiment of the display substrate shown in FIG. 1, the control switch includes a control module and a control line, and the control line includes a first control line Ct1 and a second control line Ct2; The control module includes a first control sub-module, a second control sub-module, a third control sub-module, a fourth control sub-module and a fifth control sub-module;

[0173] The first control sub-module includes a first first control circuit 411 and a first second control circuit 412;

[0174] The second control sub-module includes a second first control circuit 421 and a second second control circuit 422;

[0175] The third control sub-module includes a third first control circuit 431 and a third second control circuit 432;

[0176] The fourth control sub-module includes a fourth first control circuit 441 and a fourth second control circuit 442;

[0177] The fifth control sub-module includes a fifth first control circuit 451 and a fifth second control circuit 452;

[0178] The first first control circuit 411 is electrically connected to the first control line Ct1, the start voltage line STV and the first connection line DL1 respectively, and is configured to control to connect or disconnect the start voltage line STV and the first connection line DL1 under the control of the first control signal provided by the first control line Ct1;

[0179] The first second control circuit 412 is electrically connected to the second control line Ct2, the first connection line DL1 and the start voltage input line LI0 respectively, and is configured to control to connect or disconnect the first connection line DL1 and the start voltage input line LI0 under the control of the second control signal provided by the second control line Ct2;

[0180] The second first control circuit 421 is electrically connected to the first control line Ct1, the start voltage line STV and the second connection line DL2 respectively, is configured to control to connect or disconnect the start voltage line STV and the second connection line DL2 under the control of the first control signal provided by the first control line Ct1;

[0181] The second second control circuit 422 is electrically connected to the second control line Ct2, the second connection line DL2 and the first input cascade line LI1 respectively, is configured to control to connect or disconnect the second connection line DL2 and the first input

cascade line LI1 under the control of the second control signal provided by the second control line Ct2;

[0182] The third first control circuit 431 is electrically connected to the first control line Ct1, the start voltage line STV and the third connection line DL3 respectively, is configured to control to connect or disconnect the start voltage line STV and the third connection line DL3 under the first control signal provided by the first control line Ct1;

[0183] The third second control circuit 432 is electrically connected to the second control line Ct2, the third connection line DL3 and the second input cascade line LI2 respectively, is configured to control to connect or disconnect the third connection line DL3 and the second input cascade line LI2 under the control of the second control signal provided by the second control line Ct2;

[0184] The fourth first control circuit 441 is electrically connected to the first control line Ct1, the start voltage line STV and the fourth connection line DL4 respectively, is configured to control to connect or disconnect the start voltage line STV and the fourth connection line DL4 under the control of the first control signal provided by the first control line Ct1;

[0185] The fourth second control circuit 442 is electrically connected to the second control line Ct2, the fourth connection line DL4 and the third input cascade line LI3 respectively, is configured to control to connect or disconnect the fourth connection line DL4 and the third input cascade line LI3 under the control of the second control signal provided by the second control line Ct2;

[0186] The fifth first control circuit 451 is electrically connected to the first control line Ct1, the start voltage line STV and the fifth connection line DL5 respectively, is configured to control to connect or disconnect the start voltage line STV and the fifth connection line DL5 under the control of the first control signal provided by the first control line Ct1;

[0187] The fifth second control circuit 452 is electrically connected to the second control line Ct2, the fifth connection line DL5 and the fourth input cascade line LI4 respectively, is configured to control to connect or disconnect the fifth connection line DL5 and the fourth input cascade line LI4 under the control of the second control signal provided by the second control line Ct2.

[0188] In at least one embodiment of the display substrate shown in FIG. 4, the second stage of driving circuit to the sixth stage of driving circuit respectively correspond to a control sub-module, and the control sub-module includes a first control circuit and a second control circuit. In actual operation, some of the driving circuits from the second stage of driving circuit to the sixth stage of driving circuit can also be provided with corresponding control sub-modules.

[0189] In at least one embodiment of the display substrate shown in FIG. 4, when the first stage of driving circuit to the third stage of driving circuit are cut off, the third first control circuit 431 can control to connect the start voltage line STV and the third connection line DL3 under the control of the first control signal, and the third second control circuit 432 controls to connect the third connection line DL3 and the second input cascade line LI2 under the control of the second control signal, so that the start voltage line STV is connected to the input terminal of SY4 through the second input cascade line LI2;

[0190] When cutting off the first stage of driving circuit to the third stage of driving circuit, it is necessary to cut off the

first control line Ct1 and the second control line Ct2 so that the control sub-module corresponding to the driving circuits after the fourth stage of driving circuit included in the driving module cannot receive the first control signal and the second control signal.

[0191] In at least one embodiment of the display substrate shown in FIG. 4, when the first stage of driving circuit to the third stage of driving circuit are cut off, the fourth first control circuit 441 can also be used to control to connect the start voltage line STV and the fourth connection line DL4 under the control of the first control signal provided by the first control line Ct1, and the fourth second control circuit 442 is configured to control to connect the fourth connection line DL4 and the third input cascade line LI3 under the control of the second control signal provided by the second control line Ct2, so that the start voltage line STV is connected to the input terminal of SY5 through the third input cascade line LI3, and the first control line Ct1 and the second control line Ct2 need to be cut off, so that the control sub-module corresponding to the driving circuit after the fifth stage of driving circuit included in the driving module cannot receive the first control signal and a second control signal.

[0192] In at least one embodiment of the present disclosure, the driving module includes a plurality of connection lines; the connection lines are provided between adjacent two stage of driving circuits;

[0193] The first terminal of the connection line is electrically connected to the first control circuit, and the second terminal of the connection line is electrically connected to the second control circuit; the first terminal and the second terminal are opposite terminals.

[0194] Optionally, the first terminal may be the left terminal, and the second terminal may be the right terminal, but is not limited thereto.

[0195] As shown in FIG. 4, the left terminal of the first connection line DL1 is electrically connected to the first first control circuit 411, and the right terminal of the first connection line DL1 is electrically connected to the first second control circuit 412;

[0196] The left terminal of the second connection line DL2 is electrically connected to the second first control circuit 421, and the right terminal of the second connection line DL2 is electrically connected to the second second control circuit 422;

[0197] The left terminal of the third connection line DL3 is electrically connected to the third first control circuit 431, and the right terminal of the third connection line DL3 is electrically connected to the third second control circuit 432;

[0198] The left terminal of the fourth connection line DL4 is electrically connected to the fourth first control circuit 441, and the right terminal of the fourth connection line DL4 is electrically connected to the fourth second control circuit 442;

[0199] The left terminal of the fifth connection line DL5 is electrically connected to the fifth first control circuit 451, and the right terminal of the fifth connection line DL5 is electrically connected to the fifth second control circuit 452.

[0200] Optionally, the first control circuit includes a first control transistor, and the second control circuit includes a second control transistor;

[0201] a gate electrode of the first control transistor is electrically connected to a first electrode of the first control transistor, the gate electrode of the first control

transistor is electrically connected to the first control line, and the third electrode of the first control transistor is electrically connected to the first terminal of the connection line, and a second electrode of the first control transistor is electrically connected to the start voltage line;

[0202] a gate electrode of the second control transistor is electrically connected to the second control line, a first electrode of the second control transistor is electrically connected to the second terminal of the connection line, and a second electrode of the second control transistor is electrically connected to the input cascade line.

[0203] As shown in FIG. 5A, based on at least one embodiment of the display substrate shown in FIG. 4, the first first control circuit may include a first first control transistor T11, and the first second control circuit may include first second control transistor T12;

[0204] The gate electrode of T11 is electrically connected to the first electrode of T11, the gate electrode of T11 is electrically connected to the first control line Ct1, the first electrode of T11 is electrically connected to the left terminal of the first connection line DL1, and the second electrode of T11 is electrically connected to the start voltage line STV;

[0205] The gate electrode of T12 is electrically connected to the second control line Ct2, the first electrode of T12 is electrically connected to the right terminal of the first connection line DL1, and the second electrode of T12 is electrically connected to the start voltage input line LI0;

[0206] The second first control circuit includes a second first control transistor T21, and the second second control circuit includes a second second control transistor T22;

[0207] The gate electrode of the second first control transistor T21 is electrically connected to the first electrode of the second first control transistor T21, and the gate electrode of the second first control transistor T21 is connected to the first control line Ct1, the first electrode of the second first control transistor T21 is electrically connected to the left terminal of the second connection line DL2, and the second electrode of the second first control transistor T21 is electrically connected to the start voltage line STV;

[0208] The gate electrode of the second second control transistor T22 is electrically connected to the second control line Ct2, and the first electrode of the second second control transistor T22 is electrically connected to the right terminal of the second connection line DL2, the second electrode of the second second control transistor T22 is electrically connected to the first input cascade line LI1;

[0209] The third first control circuit includes a third first control transistor T31, and the third second control circuit includes a third second control transistor T32;

[0210] The gate electrode of the third first control transistor T31 is electrically connected to the first electrode of the third first control transistor T31, and the gate electrode of the third first control transistor T31 is connected to the first control line Ct1, the first electrode of the third first control transistor T31 is electrically connected to the left terminal of the third connection line DL3, and the second electrode of the third first control transistor T31 is electrically connected to the start voltage line STV;

[0211] The gate electrode of the third second control transistor T32 is electrically connected to the second control line Ct2, and the first electrode of the third second control transistor T32 is electrically connected to the right terminal

of the third connection line DL3, the second electrode of the third second control transistor T32 is electrically connected to the second input cascade line LI2; other control transistors are connected in the same manner, and will not be described in detail here.

[0212] In FIG. 5A, T41 is the fourth first control transistor included in the fourth first control circuit, T42 is the fourth second control transistor included in the fourth second control circuit, T51 is the fifth first control transistor included in the fifth first control circuit, and T52 is the fifth second control transistor included in the fifth second control circuit.

[0213] In at least one embodiment of the display substrate shown in FIG. 5A, all control transistors are n-type transistors, but are not limited to this.

[0214] In at least one embodiment of the display substrate shown in FIG. 5A, when the first three rows of driving circuits are cut off, T11, T12, T21 and T22 are cut off. Optionally, Ct1 controls T31 to turn on, and Ct2 controls T32 to turn on, to control to electrically connect the start voltage line STV and the second input cascade line LI2, so that the input terminal of SY4 is connected to the start voltage provided by the start voltage line STV;

[0215] Moreover, Ct1 and Ct2 need to be cut off so that the gate electrodes of T41 and T51 are not electrically connected to Ct1, so that the gate electrodes of T42 and T52 are not electrically connected to Ct2. For example, Ct1 between T31 and T41 can be cut off. Ct2 between T32 and T42 are cut off. Of course, when cutting off the first three rows of driving circuits, the T41 and T42 can be turned on, or the T51 and T52 can be turned on, which is not limited. When the T41 and T42 are turned on, the Ct1 between T41 and T51 can be cut off. Ct2 between T42 and T52 are cut off; and so on, no details will be given here.

[0216] In at least one embodiment shown in FIG. 5A, the driving module is electrically connected to four clock signal lines, but is not limited to this.

[0217] As shown in FIG. 5B, a control sub-module included in the control module may include a first control transistor T1 and a second control transistor T2;

[0218] The gate electrode of the first control transistor T1 is electrically connected to the first control line Ct1, the first electrode of the first control transistor T1 is electrically connected to the left terminal of the connection line DL, and the second electrode of the first control transistor T1 is electrically connected to the first electrode of the first control transistor T1;

[0219] The gate electrode of the second control transistor T2 is electrically connected to the second control line Ct2, the first electrode of the second control transistor T2 is electrically connected to the right terminal of the connection line DL, and the second electrode of the second control transistor T2 is connected to the input cascade line LI.

[0220] Optionally, the first control circuit includes a first control transistor, and the second control circuit includes a second control transistor;

[0221] a gate electrode of the first control transistor is electrically connected to the first control line, a first electrode of the first control transistor is electrically connected to the first terminal of the connection line, and a second electrode of the first control transistor is electrically connected to the start voltage line;

[0222] a gate electrode of the second control transistor is electrically connected to the second control line, a

first electrode of the second control transistor is electrically connected to the second terminal of the connection line, and a second electrode of the second control transistor is electrically connected to the input cascade line.

[0223] As shown in FIG. 6A, based on at least one embodiment of the display substrate shown in FIG. 4, the first first control circuit may include a first first control transistor T11, and the first second control circuit may include first second control transistor T12;

[0224] The gate electrode of T11 is electrically connected to the first control line Ct1, the first electrode of T11 is electrically connected to the left terminal of the first connection line DL1, and the second electrode of T11 is electrically connected to the start voltage line STV;

[0225] The gate electrode of T12 is electrically connected to the second control line Ct2, the first electrode of T12 is electrically connected to the right terminal of the first connection line DL1, and the second electrode of T12 is electrically connected to the start voltage input line LI0;

[0226] The second first control circuit includes a second first control transistor T21, and the second second control circuit includes a second second control transistor T22;

[0227] The gate electrode of the second first control transistor T21 is electrically connected to the first control line Ct1, and the first electrode of the second first control transistor T21 is electrically connected to the left terminal of the second connection line DL2, the second electrode of the second first control transistor T21 is electrically connected to the start voltage line STV;

[0228] The gate electrode of the second second control transistor T22 is electrically connected to the second control line Ct2, and the first electrode of the second second control transistor T22 is electrically connected to the right terminal of the second connection line DL2, the second electrode of the second second control transistor T22 is electrically connected to the first input cascade line LI1;

[0229] The third first control circuit includes a third first control transistor T31, and the third second control circuit includes a third second control transistor T32;

[0230] The gate electrode of the third first control transistor T31 is electrically connected to the first control line Ct1, and the first electrode of the third first control transistor T31 is electrically connected to the left terminal of the third connection line DL3, the second electrode of the third first control transistor T31 is electrically connected to the start voltage line STV;

[0231] The gate electrode of the third second control transistor T32 is electrically connected to the second control line Ct2, and the first electrode of the third second control transistor T32 is electrically connected to the right terminal of the third connection line DL3, the second electrode of the third second control transistor T32 is electrically connected to the second input cascade line LI2;

[0232] The fourth first control circuit includes a fourth first control transistor T41, and the fourth second control circuit includes a fourth second control transistor T42;

[0233] The gate electrode of the fourth first control transistor T41 is electrically connected to the first control line Ct1, and the first electrode of the fourth first control transistor T41 is electrically connected to the left terminal of the fourth connection line DL4, the second electrode of the fourth first control transistor T41 is electrically connected to the start voltage line STV;

[0234] The gate electrode of the fourth second control transistor T<sub>42</sub> is electrically connected to the second control line Ct<sub>2</sub>, and the first electrode of the fourth second control transistor T<sub>42</sub> is electrically connected to the right terminal of the fourth connection line DL<sub>4</sub>, the second electrode of the fourth second control transistor T<sub>42</sub> is electrically connected to the third input cascade line LI<sub>3</sub>;

[0235] The fifth first control circuit includes a fifth first control transistor T<sub>51</sub>, and the fifth second control circuit includes a fifth second control transistor T<sub>52</sub>;

[0236] The gate electrode of the fifth first control transistor T<sub>51</sub> is electrically connected to the first control line Ct<sub>1</sub>, and the first electrode of the fifth first control transistor T<sub>51</sub> is electrically connected to the left terminal of the fifth connection line DL<sub>5</sub>, the second electrode of the fifth first control transistor T<sub>51</sub> is electrically connected to the start voltage line STV;

[0237] The gate electrode of the fifth second control transistor T<sub>52</sub> is electrically connected to the second control line Ct<sub>2</sub>, and the first electrode of the fifth second control transistor T<sub>52</sub> is electrically connected to the right terminal of the fifth connection line DL<sub>5</sub>, the second electrode of the fifth second control transistor T<sub>52</sub> is electrically connected to the fourth input cascade line LI<sub>4</sub>.

[0238] In at least one embodiment of the display substrate shown in FIG. 6A, all control transistors are n-type transistors, but are not limited to this.

[0239] In at least one embodiment of the display substrate shown in FIG. 6A, when the first three rows of driving circuits are cut off, T<sub>11</sub>, T<sub>12</sub>, T<sub>21</sub> and T<sub>22</sub> are cut off, Ct<sub>1</sub> controls T<sub>31</sub> to open, and Ct<sub>2</sub> controls T<sub>32</sub> to turn on to control the start voltage line STV to be electrically connected to the second input cascade line LI<sub>2</sub>, so that the input terminal of SY<sub>4</sub> is connected to the start voltage provided by the start voltage line STV;

[0240] Furthermore, Ct<sub>1</sub> and Ct<sub>2</sub> need to be cut off so that the gates of T<sub>41</sub> and T<sub>51</sub> are not electrically connected to Ct<sub>1</sub>, so that the gates of T<sub>42</sub> and T<sub>52</sub> are not electrically connected to Ct<sub>2</sub>.

[0241] As shown in FIG. 6B, a control sub-module included in the control module may include a first control transistor T<sub>1</sub> and a second control transistor T<sub>2</sub>;

[0242] The gate electrode of the first control transistor T<sub>1</sub> is electrically connected to the first control line Ct<sub>1</sub>, the first electrode of the first control transistor T<sub>1</sub> is electrically connected to the left terminal of the connection line DL, and the second electrode of the first control transistor T<sub>1</sub> is electrically connected to the start voltage line STV;

[0243] The gate electrode of the second control transistor T<sub>2</sub> is electrically connected to the second control line Ct<sub>2</sub>, the first electrode of the second control transistor T<sub>2</sub> is electrically connected to the right terminal of the connection line DL, and the second electrode of the second control transistor T<sub>2</sub> is connected to the input cascade line LI.

[0244] In at least one embodiment of the present disclosure, the control line includes a second control line, and the control sub-module includes a second control circuit;

[0245] The connection line is electrically connected to the start voltage line;

[0246] The second control circuit is electrically connected to the second control line, the connection line and the input cascade line respectively, and is used to control to connect

or disconnect the connection line and the input cascade line under the control of the second control signal provided by the second control line.

[0247] As shown in FIG. 7, based on at least one embodiment of the display substrate shown in FIG. 1, the control switch includes a control module and a control line, the control line includes a second control line Ct<sub>2</sub>; the control module includes the first control sub-module, the second control sub-module, the third control sub-module, the fourth control sub-module and the fifth control sub-module; the first control sub-module includes a first second control circuit 412, the second control sub-module includes a second second control circuit 422, the third control sub-module includes a third second control circuit 432, the fourth control sub-module includes a fourth second control circuit 442, the fifth control sub-modules include a fifth second control circuit 452;

[0248] The first connection line DL<sub>1</sub>, the second connection line DL<sub>2</sub>, the third connection line DL<sub>3</sub>, the fourth connection line DL<sub>4</sub> and the fifth connection line DL<sub>5</sub> are all electrically connected to the start voltage line STV;

[0249] The first second control circuit 412 is electrically connected to the second control line Ct<sub>2</sub>, the first connection line DL<sub>1</sub> and the start voltage input line LI<sub>0</sub> respectively, and is used to control to connect or disconnect the first connection line DL<sub>1</sub> and the start voltage input line LI<sub>0</sub> under the control of the second control signal provided by the second control line Ct<sub>2</sub>;

[0250] The second second control circuit 422 is electrically connected to the second control line Ct<sub>2</sub>, the second connection line DL<sub>2</sub> and the first input cascade line LI<sub>1</sub> respectively, is configured to control to connect or disconnect the second connection line DL<sub>2</sub> and the first input cascade line LI<sub>1</sub> under the control of the second control signal provided by the second control line Ct<sub>2</sub>;

[0251] The third second control circuit 432 is electrically connected to the second control line Ct<sub>2</sub>, the third connection line DL<sub>3</sub> and the second input cascade line LI<sub>2</sub> respectively, is configured to control to connect or disconnect the third connection line DL<sub>3</sub> and the second input cascade line LI<sub>2</sub> under the control of the second control signal provided by the second control line Ct<sub>2</sub>;

[0252] The fourth second control circuit 442 is electrically connected to the second control line Ct<sub>2</sub>, the fourth connection line DL<sub>4</sub> and the third input cascade line LI<sub>3</sub> respectively, is configured to control to connect or disconnect the fourth connection line DL<sub>4</sub> and the third input cascade line LI<sub>3</sub> under the control of the second control signal provided by the second control line Ct<sub>2</sub>;

[0253] The fifth second control circuit 452 is electrically connected to the second control line Ct<sub>2</sub>, the fifth connection line DL<sub>5</sub> and the fourth input cascade line LI<sub>4</sub> respectively, is configured to control to connect or disconnect the fifth connection line DL<sub>5</sub> and the fourth input cascade line LI<sub>4</sub> under the control of the second control signal provided by the second control line Ct<sub>2</sub>.

[0254] Optionally, the driving module includes a plurality of connection lines; the connection lines are arranged between adjacent two stage of driving circuits;

[0255] a first terminal of the connection line is electrically connected to the start voltage line, and a second terminal of the connection line is electrically connected to the second control circuit; the first terminal and the second terminal are opposite terminals.

[0256] In specific implementation, when the control line includes a second control line and the control sub-module includes a second control circuit, the first terminal of the connection line may be electrically connected to the start voltage line, and the second terminal of the connection line may be electrically connected to the second control circuit.

[0257] For example, the first terminal may be the left terminal, and the second terminal may be the right terminal, but is not limited thereto.

[0258] Optionally, the second control circuit includes a second control transistor;

[0259] a gate electrode of the second control transistor is electrically connected to the second control line, a first electrode of the second control transistor is electrically connected to the second terminal of the connection line, and a second electrode of the second control transistor is electrically connected to the input cascade line.

[0260] As shown in FIG. 8A, based on at least one embodiment of the pixel circuit shown in FIG. 7,

[0261] The first second control circuit may include a first second control transistor T12;

[0262] The left terminal of the first connection line DL1 is electrically connected to the start voltage line STV; the gate electrode of T12 is electrically connected to the second control line Ct2, the first electrode of T12 is electrically connected to the right terminal of the first connection line DL1, and the second electrode of T12 is electrically connected to the start voltage input line LI0;

[0263] The second second control circuit includes a second second control transistor T22;

[0264] The left terminal of the second connection line DL2 is electrically connected to the start voltage line STV; the gate electrode of the second second control transistor T22 is electrically connected to the second control line Ct2, and the first electrode of the second second control transistor T22 is electrically connected to the right terminal of the second connection line DL2, and the second electrode of the second second control transistor T22 is electrically connected to the first input cascade line LI1;

[0265] The third second control circuit includes a third second control transistor T32;

[0266] The left terminal of the third connection line DL3 is electrically connected to the start voltage line STV; the gate electrode of the third second control transistor T32 is electrically connected to the second control line Ct2, and the first electrode of the third second control transistor T32 is electrically connected to the right terminal of the third connection line DL3, and the second electrode of the third second control transistor T32 is electrically connected to the second input cascade line LI2;

[0267] The fourth second control circuit includes a fourth second control transistor T42;

[0268] The left terminal of the fourth connection line DL4 is electrically connected to the start voltage line STV; the gate electrode of the fourth second control transistor T42 is electrically connected to the second control line Ct2, and the first electrode of the fourth second control transistor T42 is electrically connected to the right terminal of the fourth connection line DL4, and the second electrode of the fourth second control transistor T42 is electrically connected to the third input cascade line LI3;

[0269] The fifth second control circuit includes a fifth second control transistor T52;

[0270] The left terminal of the fifth connection line DL5 is electrically connected to the start voltage line STV; the gate electrode of the fifth second control transistor T52 is electrically connected to the second control line Ct2, and the first electrode of the fifth second control transistor T52 is electrically connected to the right terminal of the fifth connection line DL5, and the second electrode of the fifth second control transistor T52 is electrically connected to the fourth input cascade line LI4.

[0271] In at least one embodiment of the display substrate shown in FIG. 8A, all control transistors are n-type transistors, but are not limited to this.

[0272] In at least one embodiment of the display substrate shown in FIG. 8A, when the first three rows of driving circuits are cut off, T21 and T22 are cut off, and Ct2 controls T32 to turn on to control the voltage connection between the start voltage line STV and the second input cascade line LI2, so that the input terminal of SY4 is connected to the start voltage provided by the start voltage line STV;

[0273] Furthermore, Ct2 needs to be cut off so that the gate electrodes of T42 and T52 are not electrically connected to Ct2.

[0274] As shown in FIG. 8B, a control sub-module included in the control module may include a second control transistor T2;

[0275] The left terminal of the connection line DL is electrically connected to the start voltage line STV;

[0276] The gate electrode of the second control transistor T2 is electrically connected to the second control line Ct2, the first electrode of the second control transistor T2 is electrically connected to the right terminal of the connection line DL, and the second electrode of the second control transistor T2 is connected to the input cascade line LI.

[0277] In at least one embodiment of the present disclosure, the control line includes a first control line, and the control sub-module includes a first control circuit;

[0278] The first control circuit is electrically connected to the first control line, the start voltage line and the connection line respectively, and is configured to control to connect or disconnect the connection line and the start voltage line under the control of the first control signal provided by the first control line;

[0279] The connection line is electrically connected to the input cascade line.

[0280] In specific implementation, the control line may include a first control line, and the control sub-module may include a first control circuit. The first control circuit controls to connect or disconnect the connection line and the start voltage line under the control of the first control signal, so as to control the connection or disconnection between the start voltage line and the input cascade line.

[0281] As shown in FIG. 9, based on at least one embodiment of the display substrate shown in FIG. 1, the control switch includes a control module and a control line, the control line includes a first control line Ct1; the control module includes a first control sub-module, a second control sub-module, a third control sub-module, a fourth control sub-module and a fifth control sub-module; the first control sub-module includes a first first control circuit 411, the second control sub-module includes a second first control circuit 421, the third control sub-module includes a third first control circuit 431, the fourth control sub-module includes a fourth first control circuit 441, the fifth control sub-modules include the fifth first control circuit 451;

[0282] The first first control circuit **411** is electrically connected to the first control line Ct1, the start voltage line STV and the first connection line DL1 respectively, is configured to control to connect or disconnect the first connection line DL1 and the start voltage line STV under the control of the first control signal provided by the first control line Ct1;

[0283] The first connection line DL1 is electrically connected to the start voltage input line L10;

[0284] The second first control circuit **421** is electrically connected to the first control line Ct1, the start voltage line STV and the second connection line DL2 respectively, is configured to control to connect or disconnect the second connection line DL2 and the start voltage line STV under the control of the first control signal provided by the first control line Ct1;

[0285] The second connection line DL2 is electrically connected to the first input cascade line LI1;

[0286] The third first control circuit **431** is electrically connected to the first control line Ct1, the start voltage line STV and the third connection line DL3 respectively, is configured to control to connect or disconnect the third connection line DL3 and the start voltage line STV under the control of the first control signal provided by the first control line Ct1;

[0287] The third connection line DL3 is electrically connected to the second input cascade line LI2;

[0288] The fourth first control circuit **441** is electrically connected to the first control line Ct1, the start voltage line STV and the fourth connection line DL4 respectively, is configured to control to connect or disconnect the fourth connection line DLA and the start voltage line STV under the control of the first control signal provided by the first control line Ct1;

[0289] The fourth connection line DLA is electrically connected to the third input cascade line LI3;

[0290] The fifth first control circuit **451** is electrically connected to the first control line Ct1, the start voltage line STV and the fifth connection line DL5 respectively, is configured to control to connect or disconnect the fifth connection line DL5 and the start voltage line STV under the control of the first control signal provided by the first control line Ct1;

[0291] The fifth connection line DL5 is electrically connected to the fourth input cascade line LI4.

[0292] In at least one embodiment of the display substrate shown in FIG. 10A, when the first three rows of driving circuits are cut off, T11 and T12 are cut off, and Ct1 controls T31 to turn on to control the electrical connection between the start voltage line STV and the second input cascade line LI2;

[0293] Furthermore, Ct1 needs to be cut off so that the gate electrodes of T41 and T51 are not electrically connected to Ct1.

[0294] Optionally, the driving module includes a plurality of connection lines; the connection lines are arranged between adjacent two stage of driving circuits;

[0295] The first terminal of the connection line is electrically connected to the first control circuit, and the second terminal of the connection line is electrically connected to the input cascade line; the first terminal and the second terminal are opposite terminals.

[0296] In specific implementation, the first terminal of the connection line may be electrically connected to the corre-

sponding first control circuit, and the second terminal of the connection line may be electrically connected to the input cascade line, but is not limited to this.

[0297] For example, the first terminal may be the left terminal, and the second terminal may be the right terminal, but is not limited thereto.

[0298] Optionally, the first control circuit includes a first control transistor;

[0299] a gate electrode of the first control transistor is electrically connected to the first control line, a first electrode of the first control transistor is electrically connected to the start voltage line, and a second electrode of the first control transistor is electrically connected to the first terminal of the connection line.

[0300] As shown in FIG. 10A, based on at least one embodiment of the display substrate shown in FIG. 9, the first first control circuit may include a first first control transistor T11;

[0301] The gate electrode of T11 is electrically connected to the first control line Ct1, the source electrode of T11 is electrically connected to the left terminal of the first connection line DL1, and the drain electrode of T11 is electrically connected to the start voltage line STV;

[0302] The right terminal of the first connection line DL1 is electrically connected to the start voltage input line L10;

[0303] The second first control circuit includes a second first control transistor T21;

[0304] The gate electrode of the second first control transistor T21 is electrically connected to the first control line Ct1, and the source electrode of the second first control transistor T21 is electrically connected to the left terminal of the second connection line DL2, the drain electrode of the second first control transistor T21 is electrically connected to the start voltage line STV;

[0305] The right terminal of the second connection line DL2 is electrically connected to the first input cascade line LI1;

[0306] The third first control circuit includes a third first control transistor T31;

[0307] The gate electrode of the third first control transistor T31 is electrically connected to the first control line Ct1, and the source electrode of the third first control transistor T31 is electrically connected to the left terminal of the third connection line DL3, the drain electrode of the third first control transistor T31 is electrically connected to the start voltage line STV;

[0308] The right terminal of the third connection line DL3 is electrically connected to the second input cascade line LI2;

[0309] The fourth first control circuit includes a fourth first control transistor T41;

[0310] The gate electrode of the fourth first control transistor T41 is electrically connected to the first control line Ct1, and the source electrode of the fourth first control transistor T41 is electrically connected to the left terminal of the fourth connection line DL4, the drain electrode of the fourth first control transistor T41 is electrically connected to the start voltage line STV;

[0311] The right terminal of the fourth connection line DL4 is electrically connected to the third input cascade line LI3;

[0312] The fifth first control circuit includes a fifth first control transistor T51;

[0313] The gate electrode of the fifth first control transistor T<sub>51</sub> is electrically connected to the first control line Ct<sub>1</sub>, and the source electrode of the fifth first control transistor T<sub>51</sub> is electrically connected to the left terminal of the fifth connection line DL<sub>5</sub>, the drain electrode of the fifth first control transistor T<sub>51</sub> is electrically connected to the start voltage line STV;

[0314] The right terminal of the fifth connection line DL<sub>5</sub> is electrically connected to the fourth input cascade line LI<sub>4</sub>.

[0315] In at least one embodiment of the display substrate shown in FIG. 10A, all control transistors are n-type transistors, but are not limited to this.

[0316] As shown in FIG. 10B, a control sub-module included in the control module may include a first control transistor T<sub>1</sub>:

[0317] The gate electrode of the first control transistor T<sub>1</sub> is electrically connected to the first control line Ct<sub>1</sub>, the first electrode of the first control transistor T<sub>1</sub> is electrically connected to the left terminal of the connection line DL, and the second electrode of the first control transistor T<sub>1</sub> is electrically connected to the start voltage line STV;

[0318] The right terminal of the connection line DL is electrically connected to the input cascade line LI.

[0319] In at least one embodiment of the present disclosure, the connection line included in the driving module penetrates the clock signal line included in the driving circuit, the first driving circuit portion and the line collection portion in a direction from away from the display area to close to the display area.

[0320] Optionally, the display substrate includes a first metal layer and an electrode layer sequentially arranged in a direction away from the base substrate;

[0321] The connection line includes a first line portion formed on the electrode layer and a second line portion formed on the first metal layer; the first line portion and the second line portion are electrically connected;

[0322] At least part of the first line portion is provided in the clock signal line area, the first driving circuit portion and the line collection portion; the clock signal line area is an area where the plurality of clock signal lines are provided;

[0323] At least part of the second line portion is provided on the line collection portion.

[0324] In at least one embodiment of the present disclosure, the electrode layer may be an indium tin oxide (ITO) layer, and the first metal layer may be a source-drain metal layer, but is not limited thereto.

[0325] In specific implementation, the connection line may include a first line portion and a second line portion, the first line portion is formed on the electrode layer, and the second line portion is formed on the first metal layer; at least part of the first line portion is provided on the clock signal line area, the first driving circuit portion and the line collection portion, at least part of the second line portion is provided in the line collection portion, but is not limited to this.

[0326] In at least one embodiment of the present disclosure, the display panel includes an electrode layer and a first metal layer arranged on one side of the base substrate;

[0327] The connection line is formed by the electrode layer or the first metal layer.

[0328] In specific implementation, the connection lines may also be routed in a single layer, and the connection lines may be formed on the electrode layer or the first metal layer.

[0329] Optionally, the driving circuit includes an input circuit; the input circuit includes a control terminal, a first terminal and a second terminal;

[0330] The control terminal of the input circuit is electrically connected to the input terminal, and the second terminal of the input circuit is electrically connected to the pull-up node;

[0331] The input circuit is used to control the potential of the pull-up node under the control of an input signal provided by the input terminal.

[0332] In at least one embodiment of the present disclosure, the first terminal of the input circuit may be electrically connected to the input terminal; or, the first terminal of the input circuit may not be electrically connected to the input terminal.

[0333] Optionally, the input circuit includes a first transistor;

[0334] The gate electrode of the first transistor is electrically connected to the first input terminal, the first electrode of the first transistor is electrically connected to the second input terminal, and the second electrode of the first transistor is electrically connected to the pull-up node;

[0335] The first input terminal and the second input terminal may be electrically connected or not.

[0336] In specific implementation, the first input terminal and the second input terminal may both be the adjacent previous stage of driving signal output terminals, or the first input terminal may be the adjacent previous stage of the carry signal output terminal, the second output terminal may be an adjacent previous stage of driving signal output terminal, but is not limited to this.

[0337] In at least one embodiment of the present disclosure, the input circuit may include a first transistor;

[0338] a gate electrode of the first transistor is electrically connected to the input terminal, a first electrode of the first transistor is electrically connected to the high voltage terminal, a the second electrode of the first transistor is electrically connected to the pull-up node.

[0339] Optionally, the gate electrode of the first transistor is formed on the second metal layer, and the first electrode of the first transistor is formed on the first metal layer;

[0340] The gate electrode of the first transistor is electrically connected to the first connection line portion formed on the second metal layer;

[0341] The first electrode of the first transistor is electrically connected to the second connection line portion formed in the second metal layer through a via hole;

[0342] The connection line includes a third connection line portion formed on the electrode layer and a fourth connection line portion formed on the first metal layer; the third connection line portion and the fourth connection line portion are electrically connected;

[0343] There is an overlapping area between the orthographic projection of the third connection line portion on the base substrate and the orthographic projection of the first connection line portion on the base substrate; there is an overlapping area between an orthographic projection of the fourth connection line portion on the base substrate and an orthographic projection of the second connection line portion on the base substrate.

[0344] In at least one embodiment of the present disclosure, the second metal layer may be a gate metal layer, but is not limited thereto.

[0345] In at least one embodiment of the present disclosure, the first connection line portion is electrically connected to an input cascade line provided in the line collection area, and/or the second connection line portion is electrically connected to an input cascade line provided in the line collection area.

[0346] In FIG. 11, the one labeled GA2 is the second driving circuit portion. FIG. 11 is a layout diagram of the second driving circuit portion GA2; the layout diagram shown in FIG. 11 corresponds to the second driving circuit portion of the driving module shown in FIG. 5B.

[0347] Optionally, the second driving circuit portion includes an output transistor in the driving circuit;

[0348] The first driving circuit portion includes a pull-up node control sub-circuit, a pull-down node control sub-circuit and an output reset sub-circuit; the pull-up node control sub-circuit is used to control the potential of the pull-up node, and the pull-down node control sub-circuit is used to control the potential of the pull-down node, and the output reset sub-circuit is used to reset the driving signal under the control of the potential of the pull-down node.

[0349] In specific implementation, the second driving circuit portion may include a first output transistor and a second output transistor;

[0350] The gate electrode of the first output transistor is electrically connected to the pull-up node, the first electrode of the first output transistor is electrically connected to the output clock signal line, and the second electrode of the first output transistor is electrically connected to the current stage of the driving signal output terminal;

[0351] The gate electrode of the second output transistor is electrically connected to the pull-up node, the first electrode of the second output transistor is electrically connected to the output clock signal line, and the second electrode of the second output transistor is connected to the current stage of carry signal output terminal.

[0352] FIG. 12 is a layout diagram of the first driving circuit portion and the line collection portion of the driving module included in the display substrate according to at least one embodiment of the present disclosure;

[0353] FIG. 13 is a layout diagram of the gate metal layer in FIG. 12;

[0354] FIG. 14 is a layout diagram of the source-drain metal layers in FIG. 12;

[0355] FIG. 15 is a layout diagram of the electrode layer in FIG. 12.

[0356] FIG. 16 is a layout diagram of the active layer in FIG. 12;

[0357] FIG. 17 is a schematic diagram showing labels for the first driving circuit portion, the line collection portion and the connection lines added based on FIG. 12.

[0358] In FIG. 17, the one labeled GA1 is the first driving circuit portion, the one labeled A1 is the collection line portion, and the one labeled DL is the connection line.

[0359] FIG. 18 is a schematic diagram showing labels for each transistor added based on FIG. 12.

[0360] In at least one embodiment of the present disclosure, the driving module is arranged on the base substrate, and the gate metal layer, the active layer, the source-drain metal layer and the electrode layer are sequentially arranged in a direction away from the base substrate.

[0361] The layout diagram shown in FIG. 12 corresponds to the first driving circuit portion and the line collection portion of the driving module shown in FIG. 5B.

[0362] As shown in FIG. 12, the gate electrode G1 of the first transistor M1 is formed on the gate metal layer; the first electrode of the first transistor M1 and the second electrode of the first transistor M1 are formed on the source-drain metal layer. The gate electrode G1 of the first transistor M1 is electrically connected to the first connection line portion L1 formed on the gate metal layer. The first electrode of the first transistor M1 is electrically connected to the second connection line portion L2 formed on the gate metal layer through a via hole. Optionally, through the deposited electrode layer, such as an ITO (indium tin oxide) layer, the electrical connection between the first electrode of the first transistor M1 and the second connection line portion L2 are realized. That is, the electrode layer is equivalent to a bridge structure and is filled in the via hole to connect the gate metal layer and the source-drain metal layer. The connection line includes a third connection line portion L3 formed on the electrode layer, and a fourth connection line portion L4 formed on the source-drain metal layer. As shown in FIG. 14, the one labeled X1 is the electrode portion of M1, the electrode portion X1 of M1 includes the first electrode and the second electrode of M1, the first electrode is one of the source electrode and the drain electrode, the second electrode is the other one of the source electrode and the drain electrode. Referring to FIGS. 12 to 14, in this case, optionally, when the connection line overlaps the first connection line portion L1 and the second connection line portion L2, when it is necessary to transmit the start signal provided by the STV, the transmission of the start signal to the input transistor (first transistor M1) of the gate driving circuit is realized through welding at the overlapping area.

[0363] In FIG. 13, the one labeled G1 is the gate electrode of M1.

[0364] As shown in FIG. 12, there is an overlapping area between the orthographic projection of the third connection line portion L3 on the base substrate and the orthographic projection of the first connection line portion L1 on the base substrate, there is an overlapping area between the orthographic projection of the fourth connection line portion L4 on the base substrate and the orthographic projection of the second connection line portion L2 on the base substrate.

[0365] In at least one embodiment of the present disclosure, there is an overlapping area between the orthographic projection of the fourth connection line portion L4 on the base substrate and the orthographic projection of the second connection line portion L2 on the base substrate, in actual operation, the fourth connection line portion L4 and the second connection line portion L2 can be connected through welding, so that the start voltage line is electrically connected to the first electrode of M1.

[0366] The display substrate according to at least one embodiment of the present disclosure may further include a fifth connection line portion and a sixth connection line portion;

[0367] The fifth connection line portion is formed on the electrode layer, and the fifth connection line portion is connected to the third connection line portion;

[0368] The sixth connection line portion is formed on the first metal layer, and the sixth connection line portion is connected to the fourth connection line portion;

[0369] The fifth connection line portion and the sixth connection line portion are electrically connected.

[0370] In specific implementation, since the thickness of the electrode layer is thin, the fifth connection line portion

formed on the electrode layer and the sixth connection line portion formed on the first metal layer can be used in the line collection area. An orthographic projection of the fifth connection line portion on the base substrate may at least partially overlap an orthographic projection of the sixth connection line portion on the base substrate.

[0371] As shown in FIGS. 12 to 18, the display substrate according to at least one embodiment of the present disclosure further includes a fifth connection line portion L5 and a sixth connection line portion L6;

[0372] As shown in FIG. 15, the fifth connection line portion L5 is formed on the electrode layer; the fifth connection line portion L5 and the third connection line portion L3 are connected. Optionally, the fifth connection line portion L5 and the third connection line portion L3 are arranged at the same layer and made of the same material;

[0373] As shown in FIG. 14, the sixth connection line portion L6 is formed on the source-drain metal layer; the sixth connection line portion L6 is connected to the fourth connection line portion L4. Optionally, the sixth connection line portion L6 and the fourth connection line portion L4 are arranged at the same layer and made of the same material;

[0374] As shown in FIGS. 12 to 18, the fifth connection line portion L5 and the sixth connection line portion L6 are electrically connected through a first via hole H1, and the first via hole H1 is provided on the insulating layer between the fifth connection line portion L5 and the sixth connection line portion L6, when the fifth connection line portion L5 is deposited, it will fall on the first via hole H1, and then the fifth connection line portion L5 and the sixth connection line portion L6 are electrically connected through the first via hole H1.

[0375] In at least one embodiment shown in FIGS. 12 to 18, the fifth connection line portion L5 and the sixth connection line portion L6 may both be provided in the line collection area A1, but are not limited thereto.

[0376] In FIG. 18, the one labeled STV2 is the start signal line, and the one labeled LVSS is the second low voltage line;

[0377] The one labeled M1 is the first transistor, the one labeled M3 is the third transistor, the one labeled M4 is the fourth transistor, the one labeled M5 is the fifth transistor, the one labeled M6 is the sixth transistor, the one labeled M7 is the seventh transistor, the one labeled M8 is the eighth transistor, the one labeled M9 is the ninth transistor, the one labeled M10 is the tenth transistor, the one labeled M11 is the eleventh transistor, the one labeled M12 is the twelfth transistor, the one labeled M13 is the thirteenth transistor, the one labeled M14 is the fourteenth transistor, the one labeled M15 is the fifteenth transistor, the one labeled M16 is the sixteenth transistor, and the one labeled M17 is the seventeenth transistor, the one labeled M18 is the eighteenth transistor, the one labeled M19 is the nineteenth transistor, and the one labeled M20 is the twentieth transistor.

[0378] In at least one embodiment of the present disclosure, STV is used to provide a start signal for the driving module included in the display panel, and STV2 is used to provide a total reset signal for the driving module. The total reset signal can be a control signal for resetting the pull-up node PU in the driving circuit in the display panel before the display starts or before the start of one frame time.

[0379] In at least one embodiment shown in FIG. 12, when the driving circuit is an nth stage of driving circuit, the input

cascade line L1 is electrically connected to the (n-j)th stage of driving circuit output terminal, and n and j are positive integers.

[0380] In specific implementation, when the driving module is electrically connected to twelve clock signal lines, j may be 6, or j may be 5, but is not limited to this; j may also be other positive integers.

[0381] The display substrate according to at least one embodiment of the present disclosure further includes a fifth connection line portion;

[0382] The fifth connection line portion is formed on the electrode layer, and the fifth connection line portion communicates with the third connection line portion.

[0383] In specific implementation, the display substrate may further include a fifth connection line portion formed on the electrode layer, and the fifth connection line portion is connected to the third connection line portion. That is, in at least one embodiment shown in FIGS. 12 to 18, the sixth connection line portion formed on the source-drain metal layers may not be provided, and only the fifth connection line portion L5 formed on the electrode layer may be provided in the line collection area A1.

[0384] Optionally, the gate electrode of the first transistor is formed on the second metal layer, and the first electrode of the first transistor is formed on the first metal layer;

[0385] The gate electrode of the first transistor is electrically connected to the first connection line portion formed on the second metal layer;

[0386] The first electrode of the first transistor is electrically connected to the second connection line portion formed in the second metal layer through the via hole;

[0387] The connection line includes a third connection line portion formed on the electrode layer;

[0388] There is an overlapping area between the orthographic projection of the third connection line portion on the base substrate and the orthographic projection of the first connection line portion on the base substrate; there is an overlapping area between an orthographic projection of the third connection line portion on the base substrate and an orthographic projection of the second connection line portion on the base substrate.

[0389] In specific implementation, the gate electrode of the first transistor may be formed on the gate metal layer, and the first electrode of the first transistor may be formed on the source-drain metal layer;

[0390] The gate electrode of the first transistor is electrically connected to the first connection line portion formed on the gate metal layer, and the first electrode of the first transistor is electrically connected to the second connection line portion formed on the gate metal layer through the via hole;

[0391] The connection line includes a third connection line portion, and the third connection line portion is formed on the electrode layer.

[0392] In at least one embodiment of the present disclosure, as shown in FIG. 19, the connection line may include a third connection line portion L3 formed on the electrode layer. There is an overlapping area between the orthographic projection of the third connection line portion L3 on the base substrate and the orthographic projection of the first connection line portion L1 on the base substrate in FIG. 13; there is an overlapping portion between the orthographic projection of the third connection line portion L3 on the base substrate and the orthographic projection of the second

connection line portion L2 on the base substrate in FIG. 13, that is, the connection line layers are all made of electrode layers.

[0393] In at least one embodiment of the present disclosure, the gate electrode of the first transistor and the first electrode of the first transistor are electrically connected;

[0394] There is an overlapping area between the orthographic projection of the connection line on the base substrate and the orthographic projection of the gate electrode of the first transistor on the base substrate; or,

[0395] There is an overlapping area between the orthographic projection of the connection line on the base substrate and an orthographic projection of the first electrode of the first transistor on the base substrate.

[0396] During specific implementation, the gate electrode of the first transistor and the first electrode of the first transistor may be electrically connected to each other. In this way, the orthographic projection of the connection line on the base substrate may only overlap the orthographic projection of the gate electrode of the first transistor on the base substrate; or the orthographic projection of the connection line on the base substrate may only overlap the orthographic projection of the first electrode of the first transistor on the base substrate, the repair can be achieved.

[0397] FIG. 20 is a layout diagram of the second driving circuit portion. FIG. 20 corresponds to at least one embodiment of the driving module shown in FIG. 5B.

[0398] In FIG. 20, the one labeled M21 is the twenty-first transistor, the one labeled M22 is the twenty-second transistor, the one labeled C1 is the first capacitor, and the one labeled F1 is the groove F1 provided between the first electrode of the transistor M21 and the second electrode of the twenty-first transistor M21. The groove F1 can prevent the first electrode of the transistor M21 from being connected or short-circuited with the second electrode of the transistor M21.

[0399] In FIG. 20, the one labeled VSS is the first low voltage line.

[0400] In FIG. 20, the one labeled T2 is the second control transistor, and the one labeled Ct2 is the second control line;

[0401] The gate electrode of T2 is electrically connected to the second control line Ct2. Optionally, the gate electrode of T2 and the second control line are integrally formed. The first electrode of T2 is electrically connected to the right terminal of the connection line DL in FIG. 17. The second electrode of T2 is electrically connected to the input cascade line LI in FIG. 12. The first electrode of T2 is set on the source-drain metal layer, and the connection line DL is set on the electrode layer. The first electrode of T2 and the right terminal of the connection line DL are electrically connected through the first via H1 (refer to FIG. 12). The specific location of the connection via hole can be determined according to the actual design and is not limited here. The second electrode of T2 is set on the source-drain metal layer, and the input cascade line LI is set on the gate metal layer. The electrical connection between the second electrode of T2 and the input cascade line LI in FIG. 12 can be achieved through via hole GK1. At the position corresponding to GK1, an electrode layer is provided on the side of the second electrode of T2 away from the input cascade line LI. The electrode layer realizes the electrical connection between the second electrode of T2 and the input cascade line LI through the via hole GK1.

[0402] FIG. 21 is a layout diagram of the gate metal layer in FIG. 20, in which G21 is the gate electrode of M21, G22 is the gate electrode of M22, and C1a is the first electrode plate of C1.

[0403] In FIG. 21, the one labeled G2 is the gate electrode of T2, and the one labeled Ct2 is the second control line.

[0404] As shown in FIG. 21, C1a and G21 are connected, and C1a and G21 are arranged on the same layer and made of the same material;

[0405] G2 and Ct2 are connected, and G2 and Ct2 are arranged on the same layer and made of the same material.

[0406] FIG. 22 is a layout diagram of the active layer in FIG. 20. In FIG. 22, the one labeled A21 is the active layer pattern of M21, the one labeled A22 is the active layer pattern of M22, and the one labeled A2 is the active layer pattern of M2.

[0407] FIG. 23 is a layout diagram of the source-drain metal layers in FIG. 20.

[0408] In FIG. 23, the one labeled S21 is the first electrode of M21, the one labeled D21 is the second electrode of M21, the one labeled S22 is the first electrode of M22, the one labeled D22 is the second electrode of M22, the one labeled S2 is the first electrode of T2, the one labeled D2 is the second electrode of T2; the one labeled C1b is the second electrode plate of C1, and C1b and the source-drain electrode layer are arranged at the same layer and made of a same material.

[0409] As shown in FIG. 23, C1b and D21 are connected.

[0410] FIG. 24 is a layout diagram of the electrode layer in FIG. 20. The electrode layer on the left side of FIG. 24 is used to electrically connect the gate signal of M21 with the signal line corresponding to PU. The electrode layer on the right side of FIG. 24 is used to transmit the signal provided by a low-voltage line VSS to the noise reduction transistor in the driving circuit. For example, referring to FIG. 51, the first low-voltage line VSS is electrically connected to one electrode of M17 to reduce noise at the current stage of the driving signal output terminal GO.

[0411] FIG. 25 is a layout diagram of clock signal lines of the driving module included in the display substrate according to at least one embodiment of the present disclosure; FIG. 25 corresponds to at least one embodiment of the driving module shown in FIG. 5B.

[0412] In FIG. 25, the one labeled STV is the start voltage line. It should be noted that the number of start voltage lines can be one or more, and this is not limited. For example, it can be 2, and the driving circuits corresponding to odd-numbered rows is connected to one of the start voltage lines, and the driving circuit corresponding to the even-numbered row is connected to the other start voltage line. The drawing shows a start voltage line as an example. The one labeled Ct1 is the first control line, and the one labeled CLK1 is the first clock signal line, the one labeled CLK2 is the second clock signal line, the one labeled CLK3 is the third clock signal line, the one labeled CLK4 is the fourth clock signal line, the one labeled CLK5 is the fifth clock signal line, the one labeled CLK6 is the sixth clock signal line, the one labeled CLK7 is the seventh clock signal line, the one labeled CLK8 is the eighth clock signal line, the one labeled CLK9 is the ninth clock signal line, the one labeled CLK10 is the tenth clock signal line, the one labeled CLK11 is the eleventh clock signal line, and the one labeled CLK12 is the twelfth clock signal line;

[0413] The one labeled VDDO is the first control voltage line, and the one labeled VDDE is the second control voltage line;

[0414] The one labeled DL is the connection line.

[0415] In at least one embodiment of the present disclosure, the STV is used to provide a start signal for a driving module included in the display panel.

[0416] In FIG. 25, the one labeled T1 is the first control transistor;

[0417] The first control line Ct1 is multiplexed as the gate electrode of the first control transistor T1, and the gate electrode of the first control transistor T1 is electrically connected to the first electrode of the first control transistor T1; the first electrode of the first control transistor T1 is electrically connected to the left terminal of the connection line DL, and the second electrode of the first control transistor T1 is electrically connected to the start voltage line STV.

[0418] FIG. 26 is a layout diagram of the gate metal layer in FIG. 25. FIG. 27 is a layout diagram of the source-drain metal layers in FIG. 25. FIG. 28 is a layout diagram of the electrode layer in FIG. 25. FIG. 29 is a layout diagram of the active layer in FIG. 25.

[0419] In FIG. 29, the one labeled A01 is the active layer of the first control transistor. It should be noted that the active layer in this case can be any one of an oxide semiconductor layer, an amorphous silicon layer or a low-temperature polysilicon layer, which is not limited.

[0420] In FIG. 27, the one labeled S01 is the first electrode of the first control transistor T1, and the one labeled D01 is the second electrode of the first control transistor T1;

[0421] The one labeled L01 is the first connection portion, and the one labeled L02 is the second connection portion;

[0422] The first connection portion L01 is electrically connected to the first electrode S01 of T1, and the second connection portion L02 is electrically connected to the second electrode D01 of T1.

[0423] In FIG. 28, the third connection portion is labeled L03, and the fourth connection portion is labeled L04.

[0424] As shown in FIGS. 25 to 29, the first connection portion L01 is electrically connected to the third connection portion L03 through the via hole, and the second connection portion L02 is electrically connected to the fourth connection portion L04 through the via hole;

[0425] The third connection portion L03 is electrically connected to the left terminal of the connection line DL; the third connection portion L03 is electrically connected to the first connection portion L01 and the gate electrode of the first control transistor T1 through via holes respectively, so that the first electrode S01 of the first control transistor T1 is electrically connected to the left terminal of the connection line DL, and the first electrode S01 of the first control transistor T1 is electrically connected to the gate electrode of the first control transistor T1; referring to FIG. 25, two columns of via holes GK are provided at the position adjacent to the first control transistor T1 and the first connection portion L01, the left column of via holes realize the electrical connection between the third connection portion L03 and the gate electrode of T1, and the right column of via holes realize the electrical connection between the third connection portion L03 and the gate electrode of T1. The overall electrical connection among the gate electrode of the transistor, the first electrode of the transistor and the connection line is realized. Here, the connection line and the

third connection portion L03 can be provided on an electrode layer, for example, it can be an ITO (indium tin oxide) electrode layer, which can be provided on the same layer as the pixel electrode or the common electrode in the display area of the display panel.

[0426] The second connection portion L02 is electrically connected to the fourth connection portion L04 through a via hole, so that the second electrode D01 of the first control transistor T1 is electrically connected to the start voltage line STV.

[0427] FIG. 30 is a layout diagram of clock signal lines of the driving module included in the display substrate according to at least one embodiment of the present disclosure; FIG. 30 corresponds to at least one embodiment of the driving module shown in FIG. 6B.

[0428] FIG. 31 is a layout diagram of the gate metal layer in FIG. 30. FIG. 32 is a layout diagram of the source-drain metal layers in FIG. 30. FIG. 33 is a layout diagram of the electrode layer in FIG. 30. FIG. 34 is a layout diagram of the active layer in FIG. 30.

[0429] In FIG. 30, the line labeled STV is the start voltage line, the line labeled Ct1 is the first control line, the line labeled CLK1 is the first clock signal line, the line labeled CLK2 is the second clock signal line, and the line labeled CLK3 is the third clock signal line, the one labeled CLK4 is the fourth clock signal line, the one labeled CLK5 is the fifth clock signal line, the one labeled CLK6 is the sixth clock signal line, and the one labeled CLK7 is the seventh clock signal line, the one labeled CLK8 is the eighth clock signal line, the one labeled CLK9 is the ninth clock signal line, the one labeled CLK10 is the tenth clock signal line, the one labeled CLK11 is the eleventh clock signal line, the one labeled CLK12 is the twelfth clock signal line; the one labeled VDDO is the first control voltage line, the one labeled VDDE is the second control voltage line; the one labeled DL is the connection line.

[0430] In FIG. 30, the one labeled T1 is the first control transistor;

[0431] The first control line Ct1 is multiplexed as the gate electrode of the first control transistor T1. The first electrode of the first control transistor T1 is electrically connected to the left terminal of the connection line DL. The second electrode of the first control transistor T1 is connected to the start voltage line STV.

[0432] As shown in FIG. 31, STV, Ct1, CLK1, CLK2, CLK3, CLK4, CLK5, CLK6, CLK7, CLK8, CLK9, CLK10, CLK11, CLK12, VDDO and VDDE are all formed on the gate metal layer.

[0433] In FIG. 32, the one labeled S01 is the first electrode of the first control transistor T1, and the one labeled D01 is the second electrode of the first control transistor T1;

[0434] The one labeled L01 is the first connection portion, and the one labeled L02 is the second connection portion;

[0435] The first connection portion L01 is electrically connected to the first electrode S01 of T1, and the second connection portion L02 is electrically connected to the second electrode D01 of T1.

[0436] In FIG. 33, the third connection portion is labeled L03, and the fourth connection portion is labeled L04.

[0437] As shown in FIGS. 30 to 34, the first connection portion L01 is electrically connected to the third connection portion L03 through the via hole GK, and the second connection portion L02 is electrically connected to the fourth connection portion L04 through the via hole GK. As

shown in FIG. 30, a row of via holes GK are set to realize the electrical connection between the connecting line and the first connection portion L01;

[0438] The third connection portion L03 is electrically connected to the left terminal of the connection line DL; the third connection portion L03 is electrically connected to the first connection portion L01 through a via hole, so that the first electrode S01 of the first control transistor T1 is electrically connected to the left terminal of the connection line DL;

[0439] The second connection portion L02 is electrically connected to the fourth connection portion L04 through a via hole, so that the second electrode D01 of the first control transistor T1 is electrically connected to the start voltage line STV.

[0440] The layout diagram of the first driving circuit portion and the line collection portion in at least one embodiment of the driving module shown in FIG. 6B is shown in FIG. 12; the second driving circuit portion in at least one embodiment of the driving module shown in FIG. 6B is shown in FIG. 20.

[0441] FIG. 35 is a layout diagram of clock signal lines of the driving module included in the display substrate according to at least one embodiment of the present disclosure; FIG. 30 corresponds to at least one embodiment of the driving module shown in FIG. 8B.

[0442] FIG. 36 is a layout diagram of the gate metal layer in FIG. 35, FIG. 37 is a layout diagram of the source-drain metal layers in FIG. 35, and FIG. 38 is a layout diagram of the electrode layer in FIG. 35.

[0443] In FIG. 35, the line labeled STV is the start voltage line, the line labeled Ct1 is the first control line, the line labeled CLK1 is the first clock signal line, the line labeled CLK2 is the second clock signal line, and the line labeled CLK3 is the third clock signal line, the one labeled CLK4 is the fourth clock signal line, the one labeled CLK5 is the fifth clock signal line, the one labeled CLK6 is the sixth clock signal line, and the one labeled CLK7 is the seventh clock signal line, the one labeled CLK8 is the eighth clock signal line, the one labeled CLK9 is the ninth clock signal line, the one labeled CLK10 is the tenth clock signal line, the one labeled CLK11 is the eleventh clock signal line, the one labeled CLK12 is the twelfth clock signal line; the one labeled VDDO is the first control voltage line, the one labeled VDDE is the second control voltage line; the one labeled DL is the connection line.

[0444] In FIG. 38, the one labeled DL is the connection line, and the one labeled L05 is the fifth connection portion;

[0445] The fifth connection portion L05 is connected to the connection line DL.

[0446] As shown in FIGS. 35 to 38, the fifth connection portion L05 is electrically connected to the start voltage line STV through the via hole, so that the left terminal of the connection line DL is electrically connected to the start voltage line.

[0447] The layout diagram of the first driving circuit portion and the line collection portion in at least one embodiment of the driving module shown in FIG. 8B is shown in FIG. 12; the second driving circuit portion in at least one embodiment of the driving module shown in FIG. 8B is shown in FIG. 20.

[0448] The layout diagrams of the second driving circuit portion in at least one embodiment of the driving module shown in FIG. 10B are shown in FIG. 39 and FIG. 40.

[0449] In FIG. 39, the one labeled GA2 is the second driving circuit portion.

[0450] In FIG. 40, the one labeled M21 is the twenty-first transistor, the one labeled M22 is the twenty-second transistor, the one labeled C1 is the first capacitor, and the one labeled VSS is the first low voltage line;

[0451] The one labeled C1 is the first capacitor, the one labeled F1 is the groove provided between the first electrode of the twenty-first transistor M21 and the second electrode of the twenty-first transistor M21. The groove F1 can prevent the first electrode of the twenty-first transistor M21 from being connected or short-circuited with the second electrode of M21.

[0452] FIG. 41 is a layout diagram of the gate metal layer in FIG. 40, FIG. 42 is a layout diagram of the active layer in FIG. 40, FIG. 43 is a layout diagram of the source-drain metal layers in FIG. 40, FIG. 44 is a layout diagram of the electrode layer in FIG. 40.

[0453] In FIG. 41, the one labeled G21 is the gate electrode of M21, the one labeled G22 is the gate electrode of M22, and the one labeled C1a is the first electrode plate of C1.

[0454] In FIG. 42, the one labeled A21 is the active layer pattern of M21, and the one labeled A22 is the active layer pattern of M22.

[0455] In FIG. 43, the one labeled C1b is the second electrode of C1, the one labeled S21 is the first electrode of M21, the one labeled D21 is the second electrode of M21, the one labeled S22 is the first electrode of M22, the one labeled D22 is the second electrode of M22.

[0456] The layout diagram of the first driving circuit portion and the line collection portion in at least one embodiment of the driving module shown in FIG. 10B is shown in FIG. 45;

[0457] In FIG. 45, the one labeled DL is the connection line, the one labeled LI is the input cascade line, and the one labeled Z1 is the first transfer portion;

[0458] The right terminal of the connection line DL is electrically connected to the input cascade line LI through the first transfer portion Z1 (at the position of the first transfer portion, the connection line and the input cascade line LI are electrically connected through the electrode layer and the via hole).

[0459] FIG. 46 is a schematic diagram showing labels for each transistor added based on the layout diagram shown in FIG. 45.

[0460] In FIG. 46, the line labeled STV2 is the start signal line, and the line labeled LVSS is the second low voltage line;

[0461] The one labeled M1 is the first transistor, the one labeled M3 is the third transistor, the one labeled M4 is the fourth transistor, the one labeled M5 is the fifth transistor, the one labeled M6 is the sixth transistor, and the one labeled M7 is the seventh transistor, the one labeled M8 is the eighth transistor, the one labeled M9 is the ninth transistor, the one labeled M10 is the tenth transistor, the one labeled M11 is the eleventh transistor, the one labeled M12 is the twelfth transistor, the one labeled M13 is the thirteenth transistor, the one labeled M14 is the fourteenth transistor, the one labeled M15 is the fifteenth transistor, the one labeled M16 is the sixteenth transistor, and the one labeled M17 is the seventeenth transistor, the one labeled M18 is the eighteenth transistor, the one labeled M19 is the nineteenth transistor, and the one labeled M20 is the twentieth transistor.

[0462] FIG. 47 is a layout diagram of the gate metal layer in FIG. 46. FIG. 48 is a layout diagram of the source-drain metal layers in FIG. 46. FIG. 49 is a layout diagram of the electrode layer in FIG. 46. FIG. 50 is a layout diagram of the active layer in FIG. 46.

[0463] In FIG. 47, the one labeled LI is the input cascade line, and the one labeled L06 is the sixth connection portion; [0464] The input cascade line LI is connected to the sixth connection portion L06.

[0465] As shown in FIG. 48, the one labeled X1 is the electrode portion of M1. The electrode portion X1 of M1 includes the first electrode of M1 and the second electrode of M1. The first electrode is one of the source electrode and the drain electrode, and the second electrode is the other one of the source electrode and the drain electrode.

[0466] In FIG. 49, the one labeled DL is the connection line, and the one labeled L07 is the seventh connection portion; the seventh connection portion L07 is connected with the connection line DL.

[0467] As shown in FIGS. 46 to 50, the seventh connection portion L07 is electrically connected to the sixth connection portion L06 through the via hole, so that the right terminal of the connection line DL is electrically connected to the input cascade line LI.

[0468] The layout diagram of each clock signal line in at least one embodiment of the driving module shown in FIG. 10B is shown in FIG. 30.

[0469] In at least one embodiment shown in FIG. 45, when the driving circuit is an nth stage of driving circuit, the input cascade line LI is electrically connected to the output terminal of the (n-j)th stage of driving circuit, and n and j are positive integers.

[0470] In specific implementation, when the driving module is electrically connected to twelve clock signal lines, j may be 6, or j may be 5, but is not limited to this; j may also be other positive integers.

[0471] Optionally, the driving circuit includes a first driving circuit portion; the first driving circuit portion includes an input circuit, a pull-up node control circuit, a first pull-down node control circuit, a second pull-down node control circuit and a reset circuit;

[0472] The input circuit is used to control a potential of the pull-up node under the control of an input signal provided by the input terminal;

[0473] The pull-up node control circuit is used to control the potential of the pull-up node;

[0474] The first pull-down node control circuit is used to control a potential of the first pull-down node;

[0475] The second pull-down node control circuit is used to control a potential of the second pull-down node;

[0476] The reset circuit is used to reset the driving signal provided by the driving signal output terminal of the current stage under the control of a potential of the first pull-down node and a potential of the second pull-down node.

[0477] In specific implementation, the driving circuit may include a first driving circuit portion, and the first driving circuit portion may include an input circuit, an output reset circuit, a pull-up node control circuit, a first pull-down node control circuit, a second pull-down node control circuit and a reset circuit, the input circuit controls the potential of the pull-up node under the control of the input signal; the pull-up node control circuit controls the potential of the pull-up node, and the first pull-down node control circuit is used to control the potential of the first pull-down node, the

second pull-down node control circuit is used to control the potential of the second pull-down node, and the reset circuit controls to reset the driving signal provided by the current stage of the driving signal output terminal.

[0478] In at least one embodiment of the present disclosure, the driving circuit may also include only one pull-down node and one pull-down node control circuit. The pull-down node control circuit is used to control the potential of the pull-down node. The reset circuit is configured to control the potential of the pull-down node under the control of the potential of the pull-down node.

[0479] Optionally, the input circuit includes a first transistor;

[0480] a gate electrode of the first transistor is electrically connected to the first input terminal, a first electrode of the first transistor is electrically connected to the second input terminal, and a second electrode of the first transistor is electrically connected to the pull-up node;

[0481] The pull-up node control circuit includes a third transistor, a fourth transistor, a fifth transistor and a sixth transistor;

[0482] a gate electrode of the third transistor is electrically connected to the reset terminal, a first electrode of the third transistor is electrically connected to the pull-up node, and a second electrode of the third transistor is electrically connected to the second voltage line;

[0483] a gate electrode of the fourth transistor is electrically connected to the start signal line, a first electrode of the fourth transistor is electrically connected to the pull-up node, and a second electrode of the fourth transistor is electrically connected to the second voltage line;

[0484] a gate electrode of the fifth transistor is electrically connected to the first pull-down node, a first electrode of the fifth transistor is electrically connected to the pull-up node, and a second electrode of the fifth transistor is electrically connected to the second voltage line;

[0485] a gate electrode of the sixth transistor is electrically connected to the second pull-down node, a first electrode of the sixth transistor is electrically connected to the pull-up node, and a second electrode of the sixth transistor is electrically connected to the second voltage line.

[0486] The first pull-down node control circuit includes a seventh transistor, an eighth transistor, a ninth transistor, a tenth transistor and an eleventh transistor;

[0487] a gate electrode of the seventh transistor and a first electrode of the seventh transistor are both electrically connected to the first control voltage line, and a second electrode of the seventh transistor is electrically connected to the first pull-down control node;

[0488] a gate electrode of the eighth transistor is electrically connected to the pull-up node, a first electrode of the eighth transistor is electrically connected to the first pull-down control node, and a second electrode of the eighth transistor is electrically connected to the second voltage line;

[0489] a gate electrode of the ninth transistor is electrically connected to the first pull-down control node, a first electrode of the ninth transistor is electrically connected to the first control voltage line, and a second

electrode of the ninth transistor is electrically connected to the first pull-down node;

[0490] a gate electrode of the tenth transistor is electrically connected to the pull-up node, a first electrode of the tenth transistor is electrically connected to the first pull-down node, and a second electrode of the tenth transistor is electrically connected to the second voltage line;

[0491] a gate electrode of the eleventh transistor is electrically connected to the first input terminal, a first electrode of the eleventh transistor is electrically connected to the first pull-down node, and a second electrode of the eleventh transistor is electrically connected to the second voltage line;

[0492] The second pull-down node control circuit includes a twelfth transistor, a thirteenth transistor, a fourteenth transistor, a fifteenth transistor and a sixteenth transistor;

[0493] a gate electrode of the twelfth transistor and a first electrode of the twelfth transistor are both electrically connected to the second control voltage line, and a second electrode of the twelfth transistor is electrically connected to the second pull-down control node;

[0494] a gate electrode of the thirteenth transistor is electrically connected to the pull-up node, a first electrode of the thirteenth transistor is electrically connected to the second pull-down control node, and a second electrode of the thirteenth transistor is electrically connected to the second voltage line;

[0495] a gate electrode of the fourteenth transistor is electrically connected to the second pull-down control node, a first electrode of the fourteenth transistor is electrically connected to the second control voltage line, and a second electrode of the fourteenth transistor is electrically connected to the second pull-down node;

[0496] a gate electrode of the fifteenth transistor is electrically connected to the pull-up node, a first electrode of the fifteenth transistor is electrically connected to the second pull-down node, and a second electrode of the fifteenth transistor is electrically connected to the second voltage line;

[0497] a gate electrode of the sixteenth transistor is electrically connected to the first input terminal, a first electrode of the sixteenth transistor is electrically connected to the second pull-down node, and a second electrode of the sixteenth transistor is electrically connected to the second voltage line;

[0498] The reset circuit includes a seventeenth transistor, an eighteenth transistor, a nineteenth transistor and a twentieth transistor;

[0499] a gate electrode of the seventeenth transistor is electrically connected to the first pull-down node, a first electrode of the seventeenth transistor is electrically connected to the current stage of driving signal output terminal, and a second electrode of the seventeenth transistor is electrically connected to the first voltage line;

[0500] a gate electrode of the eighteenth transistor is electrically connected to the first pull-down node, a first electrode of the eighteenth transistor is electrically connected to the current stage of carry signal output terminal, and the second electrode of the eighteenth transistor electrically connected to the second voltage line;

[0501] a gate electrode of the nineteenth transistor is electrically connected to the second pull-down node, a first electrode of the nineteenth transistor is electrically connected to the current stage of driving signal output terminal, and the second electrode of the nineteenth transistor is electrically connected to the first voltage line;

[0502] a gate electrode of the twentieth transistor is electrically connected to the second pull-down node, a first electrode of the twentieth transistor is electrically connected to the current stage of carry signal output terminal, and a second electrode of the twentieth transistor is electrically connected to the second voltage line.

[0503] In at least one embodiment of the present disclosure, the first voltage line may be a first low voltage line, and the second voltage line may be a second low voltage line, but is not limited thereto.

[0504] In at least one embodiment of the present disclosure, the orthographic projection of the connection line on the base substrate partially overlaps the orthographic projection of the gate electrode of the fourth transistor on the base substrate;

[0505] The orthographic projection of the connection line on the base substrate partially overlaps the orthographic projection of the gate electrode of the thirteenth transistor on the base substrate;

[0506] The orthographic projection of the connection line on the base substrate partially overlaps the orthographic projection of the gate electrode of the fifteenth transistor on the base substrate;

[0507] The orthographic projection of the connection line on the base substrate partially overlaps the orthographic projection of the gate electrode of the sixteenth transistor on the base substrate;

[0508] The orthographic projection of the connection line on the base substrate partially overlaps the orthographic projection of the gate electrode of the twentieth transistor on the base substrate;

[0509] The orthographic projection of the connection line on the base substrate partially overlaps the orthographic projection of the gate electrode of the nineteenth transistor on the base substrate;

[0510] The orthographic projection of the connection line on the base substrate partially overlaps the orthographic projection of the gate electrode of the sixteenth transistor on the base substrate.

[0511] Optionally, the driving circuit also includes a second driving circuit portion;

[0512] The second driving circuit portion includes a twenty-first transistor and a twenty-second transistor;

[0513] a gate electrode of the twenty-first transistor is electrically connected to the pull-up node, a first electrode of the twenty-first transistor is electrically connected to the output clock signal terminal, and a second electrode of the twenty-second transistor is electrically connected to the current stage of driving signal output terminal;

[0514] a gate electrode of the twenty-second transistor is electrically connected to the pull-up node, a first electrode of the twenty-first transistor is electrically connected to the output clock signal terminal, and a

second electrode of the twenty-second transistor is electrically connected to the current stage of carry signal output terminal.

[0515] As shown in FIG. 51, at least one embodiment of the driving circuit may include a first driving circuit portion and a second driving circuit portion; at least one embodiment of the first driving circuit portion may include an input circuit 11, a pull-up node control circuit 12, the first pull-down node control circuit 13, the second pull-down node control circuit 14 and the reset circuit 15;

[0516] The input circuit 11 includes a first transistor M1; [0517] The gate electrode of the first transistor M1 is electrically connected to the first input terminal I1, the first electrode of the first transistor M1 is electrically connected to the second input terminal I2, and the second electrode of the first transistor M1 is connected to the pull-up node PU; optionally, the first input terminal I1 of the nth stage of gate driving circuit can be electrically connected to the current stage of carry signal output terminal OC of the (n-i)th stage of gate driving circuit, and the second input terminal I2 of the nth stage of gate driving circuit can be electrically connected to the driving signal output terminal of the (n-j)th stage of gate driving circuit, where i can be equal to j, that is, the current stage of carry signal output terminal OC and the current stage of driving signal output terminal GO of the same stage of the gate driving circuit provide an input signal to the first transistor of the nth stage of gate driving circuit. Optionally, the first input terminal I1 and the second input terminal I2 of the nth stage of gate driving circuit can both be electrically connected to the current stage of carry signal output terminal OC of the (n-i) stage of gate driving circuit; i is a positive integer.

[0518] The pull-up node control circuit 12 includes a third transistor M3, a fourth transistor M4, a fifth transistor M5 and a sixth transistor M6;

[0519] The gate electrode of the third transistor M3 is electrically connected to the reset terminal R0, the first electrode of the third transistor M3 is electrically connected to the pull-up node PU, and the second electrode of the third transistor M3 is electrically connected to the second low voltage line LVSS;

[0520] The gate electrode of the fourth transistor M4 is electrically connected to the start signal line STV2, the first electrode of the fourth transistor is electrically connected to the pull-up node PU, and the second electrode of the fourth transistor M4 is electrically connected to the second low voltage line LVSS;

[0521] The gate electrode of the fifth transistor M5 is electrically connected to the first pull-down node PD1, the first electrode of the fifth transistor M5 is electrically connected to the pull-up node PU, and the second electrode of the fifth transistor M5 is electrically connected to the second low voltage line LVSS;

[0522] The gate electrode of the sixth transistor M6 is electrically connected to the second pull-down node PD2, the first electrode of the sixth transistor M6 is electrically connected to the pull-up node PU, and the second electrode of the sixth transistor M6 is electrically connected to the second low voltage line LVSS;

[0523] The first pull-down node control circuit includes a seventh transistor M7, an eighth transistor M8, a ninth transistor M9, a tenth transistor M10, and an eleventh transistor M11;

[0524] The gate electrode of the seventh transistor M7 and the first electrode of the seventh transistor M7 are both electrically connected to the first control voltage line VDDO, and the second electrode of the seventh transistor M7 is electrically connected to the first pull-down control node PD\_CN1;

[0525] The gate electrode of the eighth transistor M8 is electrically connected to the pull-up node PU, the first electrode of the eighth transistor M8 is electrically connected to the first pull-down control node PD\_CN1, and the second electrode of the eighth transistor M8 is electrically connected to the second low voltage line LVSS;

[0526] The gate electrode of the ninth transistor M9 is electrically connected to the first pull-down control node PD\_CN1, the first electrode of the ninth transistor M9 is electrically connected to the first control voltage line VDDO, the second electrode of the ninth transistor M9 is electrically connected to the first pull-down node PD1;

[0527] The gate electrode of the tenth transistor M10 is electrically connected to the pull-up node PU, the first electrode of the tenth transistor M10 is electrically connected to the first pull-down node PD1, and the second electrode of the tenth transistor M10 is electrically connected to the second low voltage line LVSS;

[0528] The gate electrode of the eleventh transistor M11 is electrically connected to the first input terminal I1, the first electrode of the eleventh transistor M11 is electrically connected to the first pull-down node PD1, and the second electrode of the eleventh transistor M11 is electrically connected to the second low voltage line LVSS;

[0529] The second pull-down node control circuit includes a twelfth transistor M12, a thirteenth transistor M13, a fourteenth transistor M14, a fifteenth transistor M15, and a sixteenth transistor M16;

[0530] The gate electrode of the twelfth transistor M12 and the first electrode of the twelfth transistor M12 are both electrically connected to the second control voltage line VDDE, and the second electrode of the twelfth transistor M12 is connected to the second pull-down control node PD\_CN2;

[0531] The gate electrode of the thirteenth transistor M13 is electrically connected to the pull-up node PU, and the first electrode of the thirteenth transistor M13 is electrically connected to the second pull-down control node PD\_CN2, the second electrode of the thirteenth transistor M13 is electrically connected to the second low voltage line LVSS;

[0532] The gate electrode of the fourteenth transistor M14 is electrically connected to the second pull-down control node PD\_CN2, and the first electrode of the fourteenth transistor M14 is electrically connected to the second control voltage line VDDE, the second electrode of the fourteenth transistor M14 is electrically connected to the second pull-down node PD2;

[0533] The gate electrode of the fifteenth transistor M15 is electrically connected to the pull-up node PU, the first electrode of the fifteenth transistor M15 is electrically connected to the second pull-down node PD2, the second electrode of the fifteenth transistor M15 is electrically connected to the second low voltage line LVSS;

[0534] The gate electrode of the sixteenth transistor M16 is electrically connected to the first input terminal I1, the first electrode of the sixteenth transistor M16 is electrically connected to the second pull-down node PD2, and the

second electrode of the sixteenth transistor M<sub>16</sub> is electrically connected to the second low voltage line LVSS;

[0535] The reset circuit 15 includes a seventeenth transistor M<sub>17</sub>, an eighteenth transistor M<sub>18</sub>, a nineteenth transistor M<sub>19</sub> and a twentieth transistor M<sub>20</sub>;

[0536] The gate electrode of the seventeenth transistor M<sub>17</sub> is electrically connected to the first pull-down node PD<sub>1</sub>, and the first electrode of the seventeenth transistor M<sub>17</sub> is electrically connected to the current stage of driving signal output terminal GO, the second electrode of the seventeenth transistor M<sub>17</sub> is electrically connected to the first low voltage line;

[0537] The gate electrode of the eighteenth transistor M<sub>18</sub> is electrically connected to the first pull-down node PD<sub>1</sub>, and the first electrode of the eighteenth transistor M<sub>18</sub> is electrically connected to the current stage of carry signal output terminal OC, the second electrode of the eighteenth transistor M<sub>18</sub> is electrically connected to the second low voltage line LVSS;

[0538] The gate electrode of the nineteenth transistor M<sub>19</sub> is electrically connected to the second pull-down node PD<sub>2</sub>, and the first electrode of the nineteenth transistor M<sub>19</sub> is electrically connected to the current stage of driving signal output terminal GO, the second electrode of the nineteenth transistor M<sub>19</sub> is electrically connected to the first low voltage line VSS;

[0539] The gate electrode of the twentieth transistor M<sub>20</sub> is electrically connected to the second pull-down node PD<sub>2</sub>, and the first electrode of the twentieth transistor M<sub>20</sub> is electrically connected to the current stage of carry signal output terminal OC, the second electrode of the twentieth transistor M<sub>20</sub> is electrically connected to the second low voltage line LVSS;

[0540] The second driving circuit portion 140 includes a twenty-first transistor M<sub>21</sub>, a twenty-second transistor M<sub>22</sub> and a first capacitor C<sub>1</sub>;

[0541] The gate electrode of the twenty-first transistor M<sub>21</sub> is electrically connected to the pull-up node PU, the first electrode of the twenty-first transistor M<sub>21</sub> is electrically connected to the output clock signal terminal CLK, and the second electrode of the twenty-first transistor M<sub>21</sub> is electrically connected to the current stage of driving signal output terminal GO;

[0542] The gate electrode of the twenty-second transistor M<sub>22</sub> is electrically connected to the pull-up node PU, and the first electrode of the twenty-second transistor M<sub>22</sub> is electrically connected to the output clock signal terminal CLK, the second electrode of twenty-second transistor M<sub>22</sub> is electrically connected to the current stage of carry signal output terminal GO;

[0543] The first electrode plate of the first capacitor C<sub>1</sub> is electrically connected to the pull-up node PU, and the second electrode plate of the first capacitor C<sub>1</sub> is electrically connected to the current stage of driving signal output terminal GO.

[0544] In at least one embodiment of the driving circuit shown in FIG. 51, the first input terminal I<sub>1</sub> is electrically connected to the adjacent previous stage of carry signal output terminal, and the second input terminal I<sub>2</sub> is electrically connected to the adjacent previous stage of driving signal output terminal, but it is not limited to this.

[0545] In at least one embodiment of the driving circuit shown in FIG. 51, the eleventh transistor M<sub>11</sub> and the sixteenth transistor M<sub>16</sub> used for total reset may not be provided.

[0546] In at least one embodiment of the driving circuit shown in FIG. 51, only one pull-down node may be used, that is, the second pull-down node control circuit may not be provided; and when only the first pull-down node P<sub>U1</sub> is provided, M<sub>6</sub>, M<sub>16</sub>, M<sub>19</sub> and M<sub>20</sub> whose gate electrodes are electrically connected to the second pull-down node PD<sub>2</sub> may not be provided.

[0547] Optionally, the second driving circuit portion also includes a second transistor;

[0548] a gate electrode of the second transistor is electrically connected to the reset control terminal, a first electrode of the second transistor is electrically connected to the current stage of driving signal output terminal, and a second electrode of the second transistor is electrically connected to the first voltage line.

[0549] In at least one embodiment of the present disclosure, a groove is provided between the first electrode of the twenty-first transistor and the second electrode of the twenty-first transistor, so that the first electrode of the twenty-first transistor is not connected to the second electrodes of the twenty-first transistor;

[0550] The first electrode of the twenty-first transistor and the second electrode of the twenty-first transistor are both formed on the first metal layer.

[0551] The display substrate according to at least one embodiment of the present disclosure includes a base substrate and a driving module arranged on the base substrate; the driving module includes N cascaded driving circuits; the driving circuit includes an input terminal; N is a positive integer;

[0552] The input terminal of the previous a stages of driving circuits included in the driving module is electrically connected to the start voltage line; a is a positive integer;

[0553] The input terminal of the n<sup>th</sup> stage of driving circuit included in the driving module is electrically connected to the output terminal of the (n-m)<sup>th</sup> stage of driving circuit included in the driving module through an input cascade line; n and m are positive integers, and m is less than n;

[0554] The driving module also includes at least one connection line, the connection line extends along the first direction;

[0555] There is an overlapping area between the orthographic projection of the connection line on the base substrate and the orthographic projection of the start voltage line on the base substrate; there is an overlap area between the orthographic projection of the connection line on the base substrate and the orthographic projection of the input cascade line on the base substrate;

[0556] The connection line is electrically connected to the input cascade line.

[0557] In at least one embodiment of the present disclosure, the display substrate may not include a control switch, and there is an overlapping area between the orthographic projection of the connection line on the base substrate and the orthographic projection of the start voltage line on the base substrate; there is an overlapping area between the orthographic projection of the connection line on the base substrate and the orthographic projection of the input cas-

cade line on the base substrate; the connection line is electrically connected to the input cascade line.

[0558] When it is necessary to cut off the first c stages of driving circuits included in the driving module (c is a positive integer), the connection line corresponding to the (c+1)th stage of driving circuit and the start voltage line are electrically connected through welding or tungsten powder, so that the start voltage line is electrically connected to the input cascade line.

[0559] When the display substrate does not include a control switch, the layout diagram of each clock signal line of the driving module included in the display substrate may be as shown in FIG. 52.

[0560] FIG. 53 is a layout diagram of the gate metal layer in FIG. 52, FIG. 54 is a layout diagram of the source-drain metal layers in FIG. 52, and FIG. 55 is a layout diagram of the electrode layer in FIG. 52.

[0561] In FIG. 52, the line labeled STV is the start voltage line, the line labeled CLK1 is the first clock signal line, the line labeled CLK2 is the second clock signal line, the line labeled CLK3 is the third clock signal line, and the line labeled CLK4 is the fourth clock signal line, the line labeled CLK5 is the fifth clock signal line, the line labeled CLK6 is the sixth clock signal line, the line labeled CLK7 is the seventh clock signal line, and the line labeled CLK8 is the eighth clock signal lines, the one labeled CLK9 is the ninth clock signal line, the one labeled CLK10 is the tenth clock signal line, the one labeled CLK11 is the eleventh clock signal line, the one labeled CLK12 is the twelfth clock signal line;

[0562] The one labeled VDDO is the first control voltage line, and the one labeled VDDE is the second control voltage line;

[0563] The one labeled DL is the connection line.

[0564] As shown in FIG. 52, the orthographic projection of the start voltage line STV on the base substrate partially overlaps the orthographic projection of the connection line DL on the base substrate.

[0565] When the display substrate does not include a control switch, the layout diagram of each clock signal line of the driving module included in the display substrate may be as shown in FIG. 52.

[0566] When the display substrate does not include a control switch, the layout diagram of the first driving circuit portion and the line collection portion of the driving module included in the display substrate is as shown in FIG. 62.

[0567] In FIG. 62, the one labeled DL is the connection line, the one labeled LI is the input cascade line, the one labeled STV2 is the start signal line, and the one labeled LVSS is the second low voltage line.

[0568] FIG. 63 is a layout diagram of the gate metal layer in FIG. 62. FIG. 64 is a layout diagram of the active layer in FIG. 62. FIG. 65 is a layout diagram of the source-drain metal layer in FIG. 62. FIG. 66 is a layout diagram of the electrode layer in FIG. 62.

[0569] In FIG. 65, the one labeled X1 is the electrode portion of M1.

[0570] As shown in FIG. 62, the orthographic projection of the connection line DL on the base substrate overlaps the orthographic projection of the input cascade line LI on the base substrate.

[0571] In specific implementation, when the start voltage line STV in FIG. 52 needs to be electrically connected to the input cascade line LI in FIG. 62, welding or tungsten powder

can be used to electrically connect the start voltage line STV to the connection line DL, and electrically connect the connection line DL and the input cascade line LI.

[0572] When the display substrate does not include a control switch, the second driving circuit portion of the driving module included in the display substrate is as shown in FIGS. 56 and 57.

[0573] In FIG. 56, the one labeled GA2 is the second driving circuit portion.

[0574] In FIG. 57, the one labeled M21 is the twenty-first transistor, the one labeled M22 is the twenty-second transistor, and the one labeled C1 is the first capacitor.

[0575] FIG. 58 is a layout diagram of the gate metal layer in FIG. 57, FIG. 59 is a layout diagram of the active layer in FIG. 57, FIG. 60 is a layout diagram of the source-drain metal layer in FIG. 57, FIG. 61 is a layout diagram of the electrode layer in FIG. 57.

[0576] The repair method described in the embodiment of the present disclosure is applied to the above-mentioned display substrate; the repair method includes:

[0577] When the previous c stages of driving circuits included in the driving module in the display substrate are cut off, controlling, by the control switch, to connect the connection line and the input cascade line;

[0578] The input cascade line is electrically connected to the input terminal of the (c+k)th stage of driving circuit; both c and k are positive integers.

[0579] In specific implementation, when the first c stages of driving circuits included in the driving module are cut off, the control switch controls to connect the connection line and the input cascade line, so that the start voltage line is connected to the input terminal of the (c+k)th stage of driving circuit.

[0580] In at least one embodiment of the present disclosure, the control switch includes a control line and a control module, the control line includes a first control line and a second control line, and the control module includes at least one control sub-module, so the control sub-module includes a first control circuit and a second control circuit;

[0581] The repair methods include:

[0582] When the first c stages of driving circuits included in the driving module in the display substrate are cut off, the connection line close to the (c+p)th stage of driving circuit being used to transmit the start voltage signal; disconnecting the first control line between the first control circuit corresponding to the (c+p)th stage of driving circuit from the first control circuit corresponding to the (c+p+1)th stage of driving circuit; disconnecting the second control line between the second control circuit corresponding to the (c+p)th stage of driving circuit from the second control circuit corresponding to the (c+p+1)th stage of driving circuit;

[0583] p is a positive integer greater than or equal to 1.

[0584] In at least one embodiment of the present disclosure, the control switch includes a control line and a control module, the control line includes a second control line, the control module includes at least one control sub-module, and the control sub-module includes a second control circuit;

[0585] The repair method includes: when the first c stages of driving circuits included in the driving module in the display substrate are cut off, the connection line close to the (c+p)th stage of driving circuit being used to transmit the start voltage signal; disconnecting the second control line

between the second control circuit corresponding to the  $(c+p)$ th stage of driving circuit and the second control circuit corresponding to the  $(c+p+1)$  stage of driving circuit;

[0586]  $p$  is a positive integer greater than or equal to 1.  
[0587] In at least one embodiment of the present disclosure, the control switch includes a control line and a control module, the control line includes a first control line, the control module includes at least one control sub-module, and the control sub-module includes a first control circuit;

[0588] The repair method includes: when the first  $c$  stages of driving circuits included in the driving module in the display substrate are cut off, the connection line close to the  $(c+p)$ th stage of driving circuit being used to transmit the start voltage signal; disconnecting the first control line between the first control circuit corresponding to the  $(c+p)$ th stage of driving circuit and the first control circuit corresponding to the  $(c+p+1)$ th stage of driving circuit;

[0589]  $p$  is a positive integer greater than or equal to 1.  
[0590] The display device according to the embodiment of the present disclosure includes the above-mentioned display substrate.

[0591] The above descriptions are implementations of the present disclosure. It should be pointed out that those skilled in the art can make some improvements and modifications without departing from the principle of the present disclosure. These improvements and modifications shall also fall within the scope of the present disclosure.

1. A display substrate, comprising a base substrate and a driving module arranged on the base substrate; wherein the driving module includes a control switch and  $N$  cascaded driving circuits; the driving circuit includes an input terminal;  $N$  is a positive integer;

input terminals of previous  $n$  stages of driving circuits included in the driving module is electrically connected to a start voltage line;  $n$  is a positive integer;

an input terminal of an  $n$ th stage of driving circuit included in the driving module is electrically connected to an output terminal of an  $(n-m)$ th stage of driving circuit included in the driving module through an input cascade line;  $n$  and  $m$  are positive integers, and  $m$  is less than  $n$ ;

the driving module further includes at least one connection line, the connection line extends along a first direction;

there is an overlapping area between an orthographic projection of the connection line on the base substrate and an orthographic projection of the start voltage line on the base substrate; and/or, there is an overlapping area between the orthographic projection of the connection line on the base substrate and an orthographic projection of the input cascade line on the base substrate;

the control switch is electrically connected to the connection line.

2. The display substrate according to claim 1, wherein at least part of the connection line and the start voltage line are located on different layers, and at least part of the connection line and the input cascade line are located on different layers.

3. The display substrate according to claim 1, wherein the connection line is provided between two adjacent driving circuits; or the connection line penetrates at least part of the driving circuit.

4. The display substrate according to claim 1, wherein the driving module includes a plurality of clock signal lines, a

plurality of stages of driving circuits and a line collection portion; the driving circuit includes a first driving circuit portion and a second driving circuit portion;

the plurality of clock signal lines, the first driving circuit portion, the line collection portion and the second driving circuit portion are arranged in sequence along a direction close to a display area;

the input cascade line is provided in the line collection portion;

the driving circuit includes the first driving circuit portion and the second driving circuit portion.

5. The display substrate according to claim 4, wherein the control switch includes a control line and a control module; the control module is electrically connected to the control line, the start voltage line, the connection line and the line collection portion respectively, and is configured to control to connect or disconnect the connection line and the line collection portion under the control of a control signal provided by the control line;

there is an overlapping area between the orthographic projection of the connection line on the base substrate and the orthographic projection of the line collection portion on the base substrate.

6. The display substrate according to claim 5, wherein the control module is electrically connected to the input cascade line in the line collection portion; the control module includes at least one control sub-module;

a control sub-module corresponding to the  $n$ th stage of driving circuit included in the driving module is electrically connected to an input terminal of the  $(n+j)$ th stage of driving circuit through the input cascade line;  $j$  is a positive integer.

7. The display substrate according to claim 6, wherein the control line includes a first control line and a second control line, and the control sub-module includes a first control circuit and a second control circuit;

the first control circuit is electrically connected to the first control line, the start voltage line and the connection line respectively, and is configured to control to connect or disconnect the start voltage line and the connection line under the control of a first control signal provided by the first control line;

the second control circuit is electrically connected to the second control line, the connection line and the input cascade line respectively, and is configured to control to connect or disconnect the connection line and the input cascade line under the control of a second control signal provided by the second control line.

8. The display substrate according to claim 7, wherein the driving module includes a plurality of connection lines; the connection lines are provided between adjacent two stages of driving circuits;

a first terminal of the connection line is electrically connected to the first control circuit, and a second terminal of the connection line is electrically connected to the second control circuit; the first terminal and the second terminal are opposite terminals.

9. The display substrate according to claim 8, wherein the first control circuit includes a first control transistor, and the second control circuit includes a second control transistor; a gate electrode of the first control transistor is electrically connected to a first electrode of the first control transistor, the gate electrode of the first control transistor is electrically connected to the first control line, and the

first electrode of the first control transistor is electrically connected to the first terminal of the connection line, and a second electrode of the first control transistor is electrically connected to the start voltage line; a gate electrode of the second control transistor is electrically connected to the second control line, a first electrode of the second control transistor is electrically connected to the second terminal of the connection line, and a second electrode of the second control transistor is electrically connected to the input cascade line.

**10.** The display substrate according to claim 7, wherein the first control circuit includes a first control transistor, and the second control circuit includes a second control transistor;

a gate electrode of the first control transistor is electrically connected to the first control line, a first electrode of the first control transistor is electrically connected to the first terminal of the connection line, and a second electrode of the first control transistor is electrically connected to the start voltage line;

a gate electrode of the second control transistor is electrically connected to the second control line, a first electrode of the second control transistor is electrically connected to the second terminal of the connection line, and a second electrode of the second control transistor is electrically connected to the input cascade line.

**11.** The display substrate according to claim 6, wherein the control line includes a second control line, and the control sub-module includes a second control circuit;

the connection line is electrically connected to the start voltage line;

the second control circuit is electrically connected to the second control line, the connection line and the input cascade line respectively, and is configured to control to connect or disconnect the connection line and the input cascade line under the control of the second control signal provided by the second control line,

wherein the driving module includes a plurality of connection lines; the plurality of connection lines are arranged between adjacent two stage of driving circuits;

a first terminal of the connection line is electrically connected to the start voltage line, and a second terminal of the connection line is electrically connected to the second control circuit; the first terminal and the second terminal are opposite terminals,

wherein the second control circuit includes a second control transistor;

a gate electrode of the second control transistor is electrically connected to the second control line, a first electrode of the second control transistor is electrically connected to the second terminal of the connection line, and a second electrode of the second control transistor is electrically connected to the input cascade line.

**12.-13.** (canceled)

**14.** The display substrate according to claim 6, wherein the control line includes a first control line, and the control sub-module includes a first control circuit;

the first control circuit is electrically connected to the first control line, the start voltage line and the connection line respectively, and is configured to control to connect or disconnect the connection line and the start voltage line under the control of the first control signal provided by the first control line;

the connection line is electrically connected to the input cascade line,

the driving module includes a plurality of connection lines; the plurality of connection lines are arranged between adjacent two stage of driving circuits;

the first terminal of the connection line is electrically connected to the first control circuit, and the second terminal of the connection line is electrically connected to the input cascade line; the first terminal and the second terminal are opposite terminals,

the first control circuit includes a first control transistor; a gate electrode of the first control transistor is electrically connected to the first control line, a first electrode of the first control transistor is electrically connected to the start voltage line, and a second electrode of the first control transistor is electrically connected to the first terminal of the connection line.

**15.-16.** (canceled)

**17.** The display substrate according to claim 4, wherein the connection line included in the driving module penetrates the clock signal line included in the driving circuit, the first driving circuit portion and the line collection portion in a direction from away from the display area to close to the display area.

**18.** The display substrate according to claim 4, wherein the display substrate includes a first metal layer and an electrode layer sequentially arranged in a direction away from the base substrate;

the connection line includes a first line portion formed on the electrode layer and a second line portion formed on the first metal layer; the first line portion and the second line portion are electrically connected;

at least part of the first line portion is provided in a clock signal line area, the first driving circuit portion and the line collection portion; the clock signal line area is an area where the plurality of clock signal lines are provided;

at least part of the second line portion is provided on the line collection portion.

**19.** The display substrate according to claim 1, wherein the driving circuit includes an input circuit; the input circuit includes a control terminal, a first terminal and a second terminal;

the control terminal of the input circuit is electrically connected to the input terminal, and the second terminal of the input circuit is electrically connected to a pull-up node;

the input circuit is configured to control a potential of the pull-up node under the control of an input signal provided by the input terminal,

wherein the input circuit includes a first transistor;

a gate electrode of the first transistor is electrically connected to the first input terminal, a first electrode of the first transistor is electrically connected to the second input terminal, and a second electrode of the first transistor is electrically connected to the pull-up node; the first input terminal and the second input terminal are electrically connected or not electrically connected,

the gate electrode of the first transistor is formed on the second metal layer, and the first electrode of the first transistor is formed on the first metal layer;

the gate electrode of the first transistor is electrically connected to the first connection line portion formed on the second metal layer;

the first electrode of the first transistor is electrically connected to the second connection line portion formed in the second metal layer through a via hole; the connection line includes a third connection line portion formed on the electrode layer and a fourth connection line portion formed on the first metal layer; the third connection line portion and the fourth connection line portion are electrically connected; there is an overlapping area between an orthographic projection of the third connection line portion on the base substrate and an orthographic projection of the first connection line portion on the base substrate; there is an overlapping area between an orthographic projection of the fourth connection line portion on the base substrate and an orthographic projection of the second connection line portion on the base substrate, wherein the display substrate further comprises a fifth connection line portion and a sixth connection line portion; the fifth connection line portion is formed on the electrode layer, and the fifth connection line portion is connected to the third connection line portion; the sixth connection line portion is formed on the first metal layer, and the sixth connection line portion is connected to the fourth connection line portion; the fifth connection line portion and the sixth connection line portion are electrically connected.

**20.-22.** (canceled)

**23.** The display substrate according to claim 1, wherein the driving circuit includes a first driving circuit portion; the first driving circuit portion includes an input circuit, a pull-up node control circuit, a first pull-down node control circuit, a second pull-down node control circuit and a reset circuit;

the input circuit is configured to control a potential of the pull-up node under the control of an input signal provided by the input terminal; the pull-up node control circuit is configured to control the potential of the pull-up node; the first pull-down node control circuit is configured to control a potential of the first pull-down node; the second pull-down node control circuit is configured to control a potential of the second pull-down node; the reset circuit is configured to reset the driving signal provided by the driving signal output terminal of the current stage under the control of the potential of the first pull-down node and the potential of the second pull-down node.

**24.** A display substrate, comprising a base substrate and a driving module arranged on the base substrate; wherein the driving module includes N cascaded driving circuits; the driving circuit includes an input terminal; N is a positive integer;

input terminals of previous a stages of driving circuits included in the driving module are electrically connected to a start voltage line; a is a positive integer; an input terminal of an nth stage of driving circuit included in the driving module is electrically connected to an output terminal of the (n-m)th stage of driving circuit included in the driving module through an input cascade line; n and m are positive integers, and m is less than n;

the driving module also includes at least one connection line, the connection line extends along a first direction;

there is an overlapping area between an orthographic projection of the connection line on the base substrate and an orthographic projection of the start voltage line on the base substrate; there is an overlap area between the orthographic projection of the connection line on the base substrate and an orthographic projection of the input cascade line on the base substrate.

**25.** A repairing method, applied to the display substrate according to claim 1, comprising:

when previous c stages of driving circuits included in the driving module in the display substrate are cut off, controlling, by the control switch, to connect the connection line and the input cascade line; the input cascade line being electrically connected to an input terminal of a (c+k)th stage of driving circuit; both c and k are positive integers.

**26.** The repairing method according to claim 25, wherein the control switch includes a control module and a control line;

the control line includes a first control line and the second control line, the control module includes at least one control sub-module, the control sub-module includes a first control circuit and a second control circuit;

the repairing method includes:

when the first c stages of driving circuits included in the driving module in the display substrate are cut off, a connection line close to the (c+p)th stage of driving circuit being used to transmit the start voltage signal; disconnecting a first control line between a first control circuit corresponding to a (c+p)th stage of driving circuit from a first control circuit corresponding to a (c+p+1)th stage of driving circuit; disconnecting the second control line between the second control circuit corresponding to the (c+p)th stage of driving circuit from the second control circuit corresponding to the (c+p+1)th stage of driving circuit;

p is a positive integer greater than or equal to 1;

or

the control switch includes a control module and a control line; the control line includes a second control line, and the control module includes at least one control sub-module, the control sub-module includes a second control circuit;

the repair method includes: when the first c stages of driving circuits included in the driving module in the display substrate are cut off, the connection line close to the (c+p)th stage of driving circuit being used to transmit the start voltage signal; disconnecting the second control line between the second control circuit corresponding to the (c+p)th stage of driving circuit and the second control circuit corresponding to the (c+p+1)th stage of driving circuit;

p is a positive integer greater than or equal to 1;

or

the control switch includes a control module and a control line; the control line includes a first control line, and the control module includes at least one control sub-module, the control sub-module includes a first control circuit;

the repair method includes: when the first c stages of driving circuits included in the driving module in the display substrate are cut off, the connection line close to the (c+p)th stage of driving circuit being used to transmit the start voltage signal; disconnecting the first

control line between the first control circuit corresponding to the  $(c+p)$ th stage of driving circuit and the first control circuit corresponding to the  $(c+p+1)$ th stage of driving circuit;

$p$  is a positive integer greater than or equal to 1.

**27.-28.** (canceled)

**29.** A display device, comprising the display substrate according to claim 1.

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