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**TOUZARD et al.**(10) **Pub. No.: US 2025/0264902 A1**(43) **Pub. Date: Aug. 21, 2025**(54) **BIASING DEVICE FOR VARIABLE CAPACITANCE**(52) **U.S. Cl.**CPC ..... *G05F 3/267* (2013.01); *H03L 7/099* (2013.01)(71) Applicant: **STMicroelectronics International N.V.**, Geneva (CH)(72) Inventors: **Olivier TOUZARD**, Grenoble (FR);  
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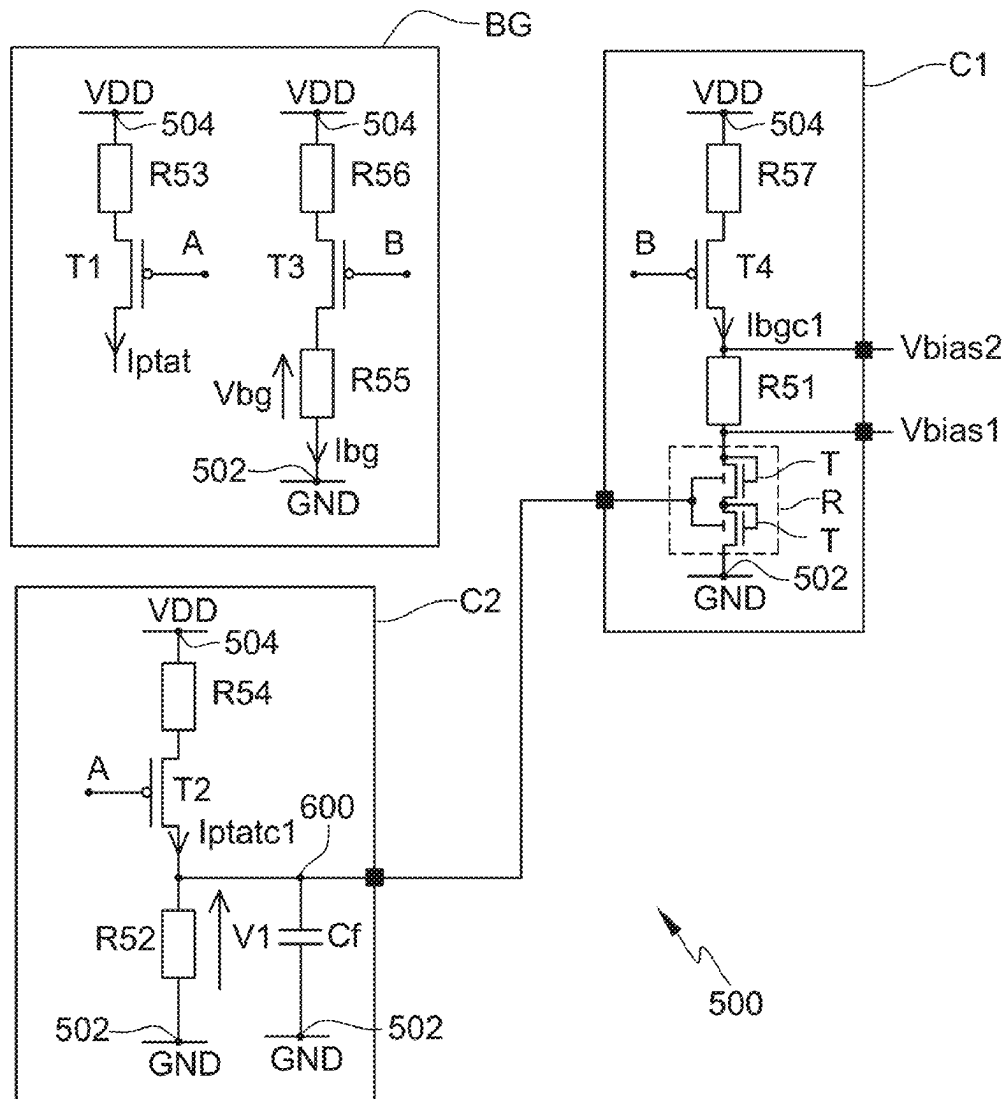
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**ABSTRACT**(21) Appl. No.: **19/047,239**(22) Filed: **Feb. 6, 2025**(30) **Foreign Application Priority Data**

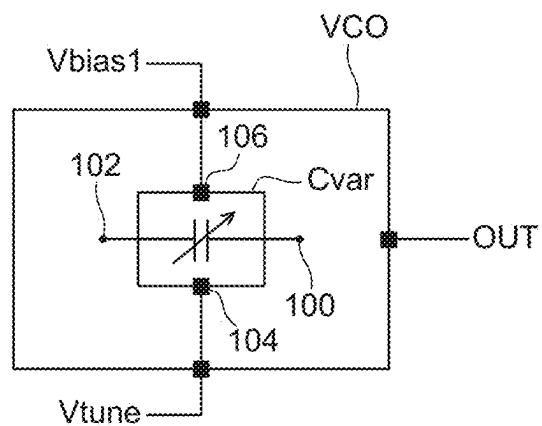
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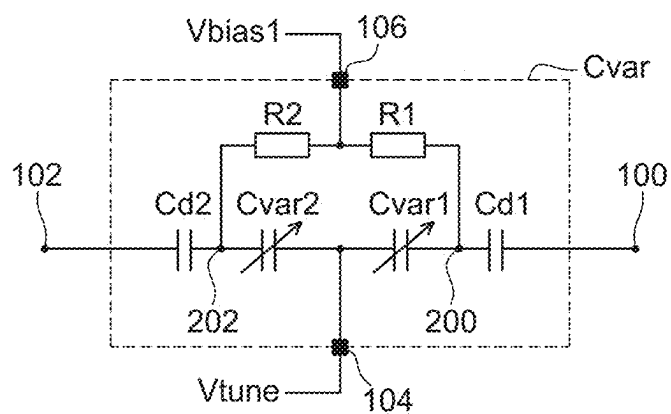
A biasing device for variable capacitance is provided. An example device comprises a first circuit. The first circuit delivers a first current flowing through a first resistive element receiving a temperature-stable voltage, and a second current proportional to temperature. A second resistive element comprises MOS transistors in series and connected as a diode, and has a first terminal connected to a reference potential and a second terminal coupled to a power supply potential. A second circuit delivers, in the second resistive element, a copy of the first current. A third circuit applies a voltage to a back gate of the transistors, determined by the second current.



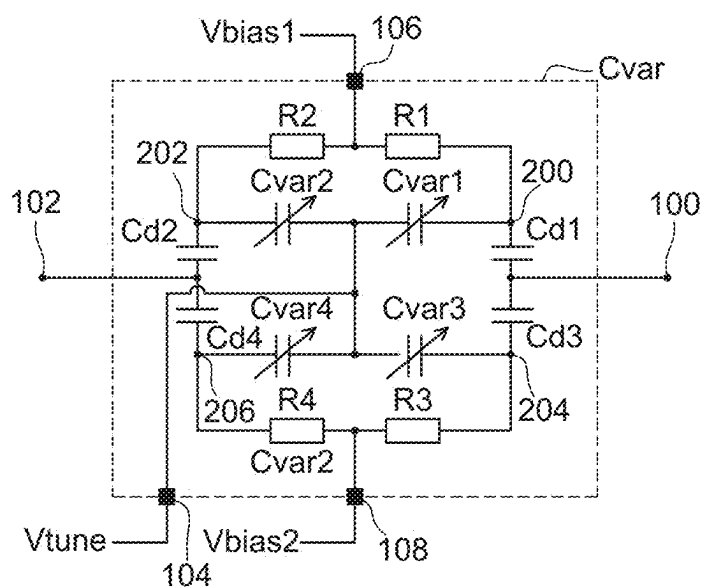
**Fig. 1**

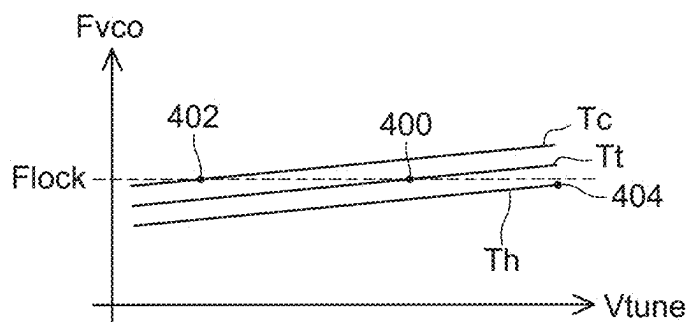


**Fig. 2**

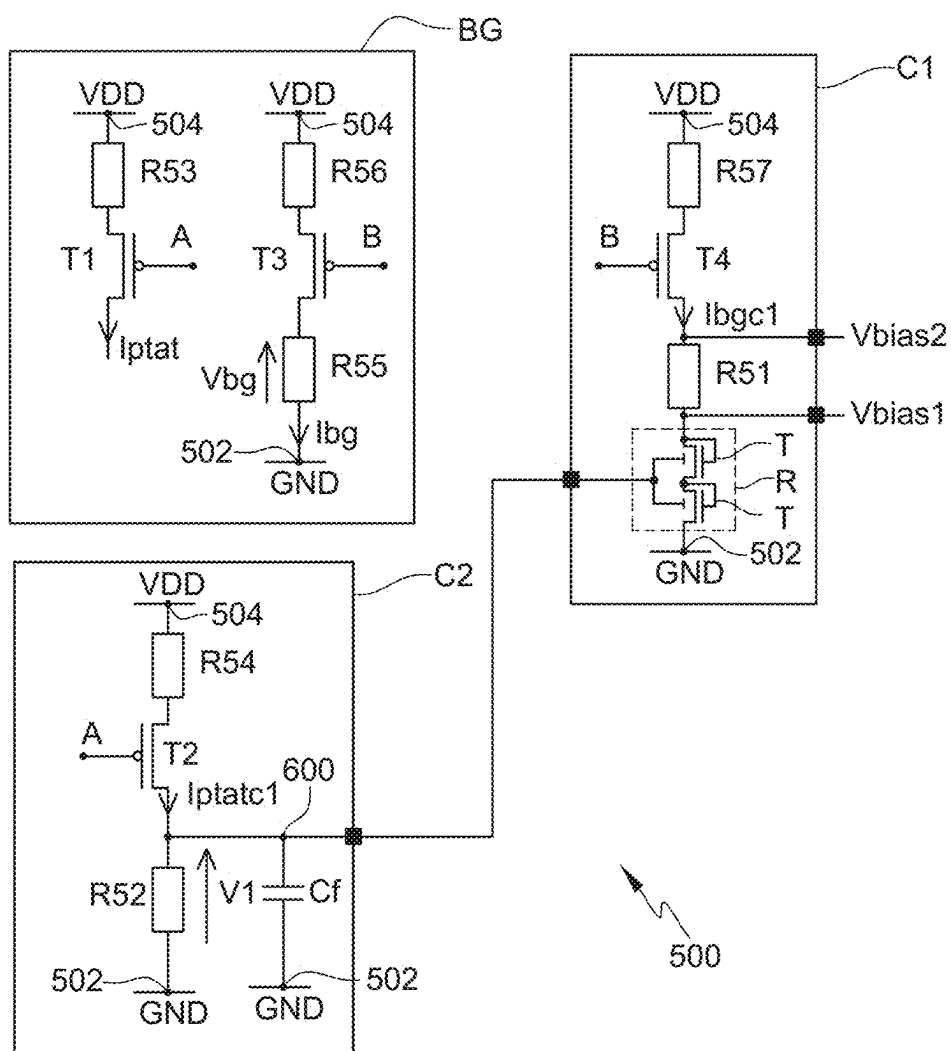


**Fig. 3**





**Fig. 4**



**Fig. 5**

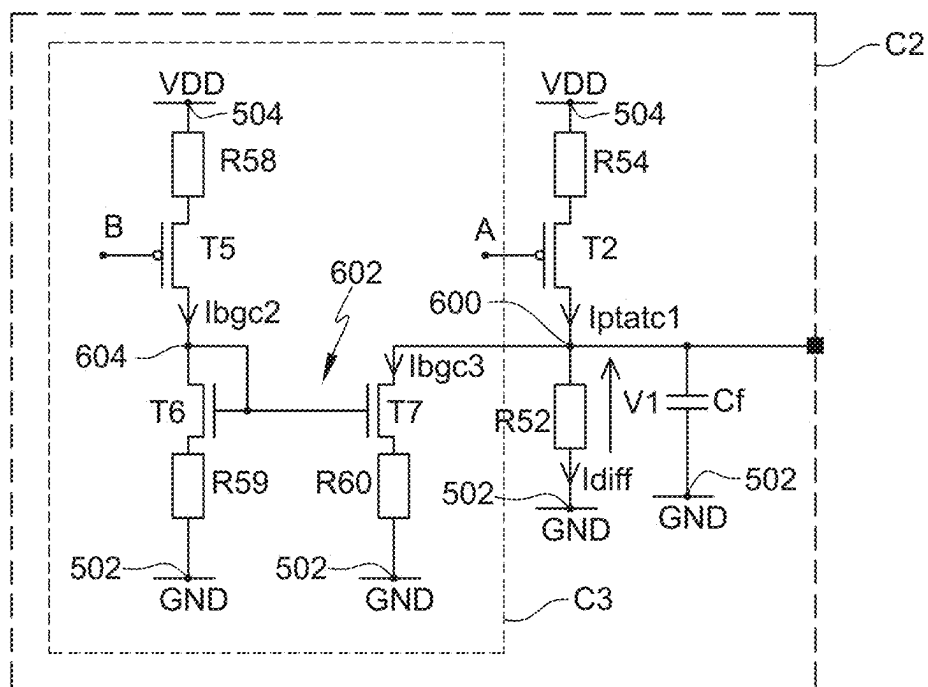


Fig. 6

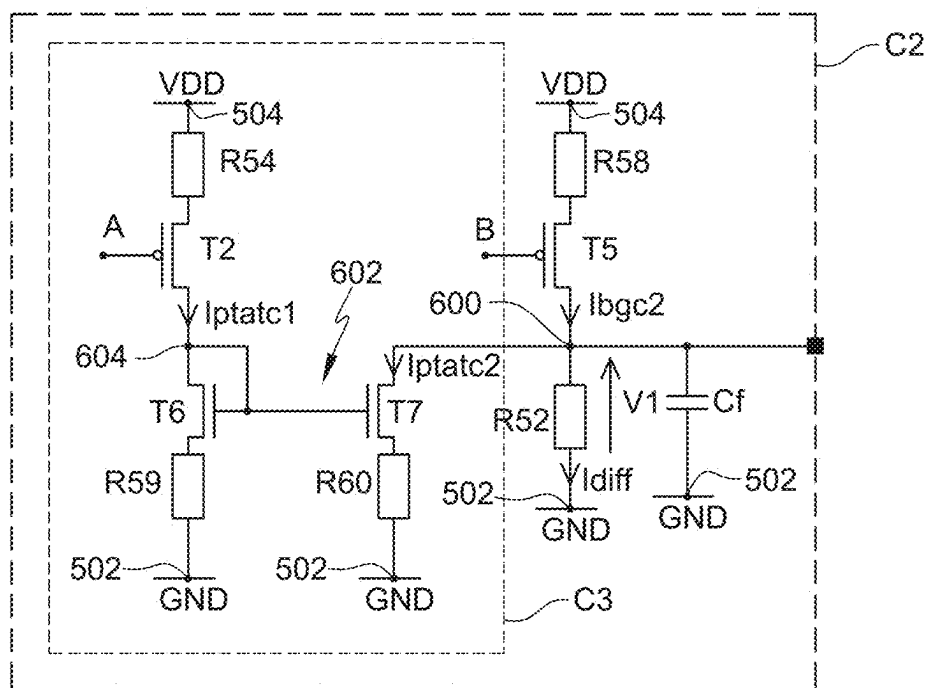
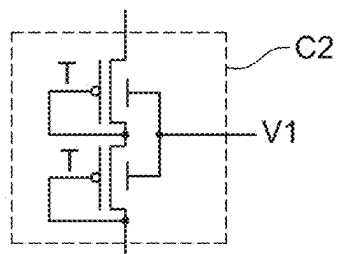
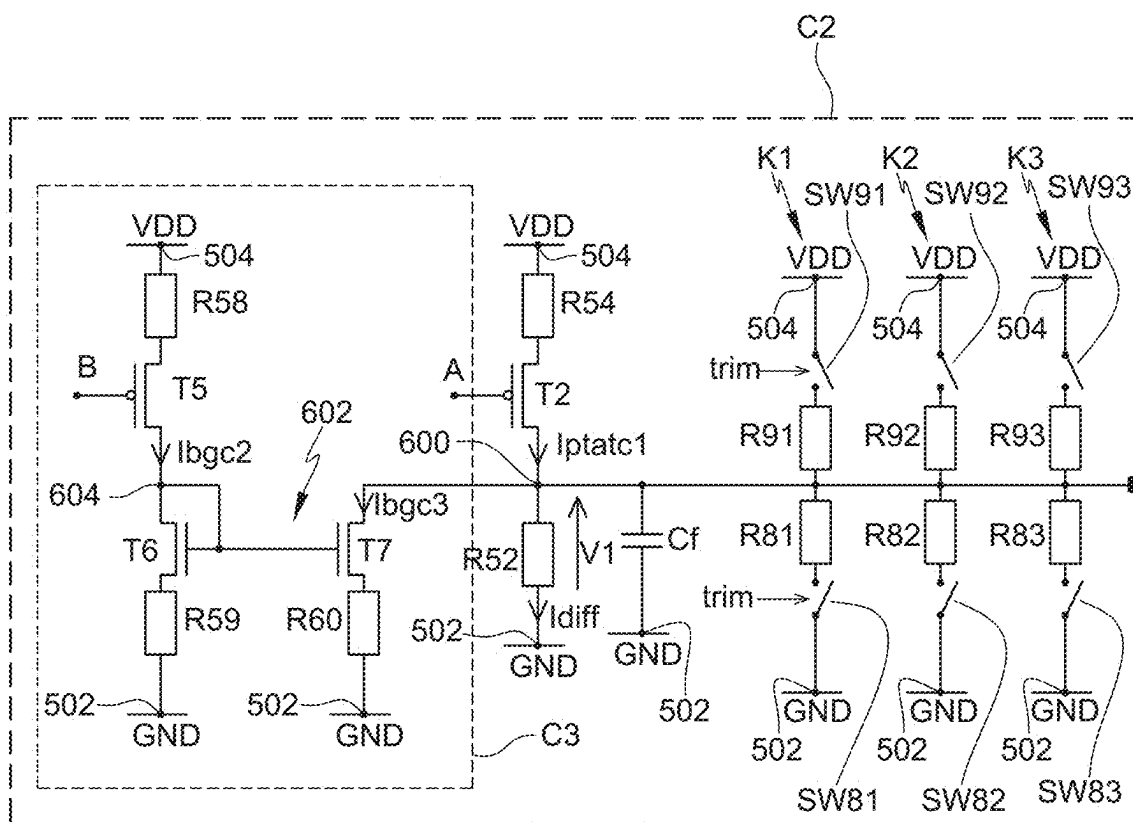


Fig. 7



**Fig. 8**



**Fig. 9**



## BIASING DEVICE FOR VARIABLE CAPACITANCE

### CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of French patent application number 2401637, filed on Feb. 20, 2024, entitled “Dispositif de Polarisation d'une Capacité Variable,” which is hereby incorporated by reference to the maximum extent allowable by law.

### TECHNICAL FIELD

[0002] The present disclosure generally concerns electronic circuits, and more particularly electronic circuits comprising a variable capacitor.

### BACKGROUND

[0003] Many electronic circuits comprise a variable capacitor, that is, a capacitive component having an adjustable capacitance value. As an example, voltage-controlled oscillators are electronic circuits comprising a variable capacitor.

[0004] Electronic circuits comprising a variable capacitor have various disadvantages. For example, their operation may depend on temperature in addition to the value of their variable capacitance, which poses a problem. This is for example the case in voltage-controlled oscillators comprising a variable capacitor, such as voltage-controlled oscillators configured to deliver a radio frequency signal having, for example, a frequency greater than 1 GHz, or even greater than 10 GHz, for example approximately equal to 20 GHz.

### BRIEF SUMMARY

[0005] There exists a need to overcome all or part of the disadvantages of electronic circuits comprising a variable capacitor.

[0006] For example, there is a need for a device delivering a voltage to a variable capacitor of an electronic circuit, which enables to at least partly compensate for the effect of temperature on an operating parameter of the electronic circuit.

[0007] For example, there exists a need for a device enabling to deliver a voltage to a variable capacitor of a voltage-controlled oscillator which enables to at least partially compensate for the effect of temperature on the oscillator frequency, for example when the oscillator frequency is controlled by a phase-locked loop (PLL).

[0008] An embodiment overcomes all or part of the disadvantages of known electronic circuits comprising a variable capacitor.

[0009] For example, an embodiment overcomes all or part of the disadvantages of known devices delivering a voltage to a variable capacitor of an electronic circuit.

[0010] For example, an embodiment overcomes all or part of the disadvantages of known devices delivering a voltage to a variable capacitor of a voltage-controlled oscillator, for example a voltage-controlled oscillator controlled by a phase-locked loop.

[0011] An embodiment provides a device comprising: a first bandgap circuit configured to apply a temperature-stable voltage across a first resistive element so that a first current flows therethrough, and to deliver a second current proportional to absolute temperature;

[0012] a second resistive element comprising one or a plurality of MOS transistors in series and each connected as a diode, the second resistive element having a first terminal connected to a node of application of a reference potential and a second terminal coupled to a node of application of a power supply potential;

[0013] a second circuit connected to the first circuit and configured to deliver a first copy of the first current and so that the first copy flows through the second resistive element; and

[0014] a third circuit connected to the first circuit and configured to:

[0015] deliver a copy of the second current, deliver a first control voltage from the copy of the second current, and apply the first control voltage to a back gate of the transistors of the resistive element, or

[0016] deliver a second copy of the first current and a copy of the second current, deliver a first control voltage from a difference between the second copy of the second current and the copy of the first current, and apply the first control voltage to a back gate of the transistors of the second resistive element.

[0017] According to an embodiment, the second terminal of the second resistive element is configured to deliver a bias voltage to a variable capacitor.

[0018] According to an embodiment, the device comprises the variable capacitor, the variable capacitor is configured to receive a tuning voltage and the bias voltage, and a difference between the tuning voltage and the bias voltage determines a value of the capacitance.

[0019] According to an embodiment, the second resistive element is in series with a resistor, the second terminal of the second resistive element is configured to deliver a first bias voltage to a variable capacitor and is connected to a first terminal of the resistor, and a second terminal of the resistor is configured to deliver a second bias voltage to the variable capacitor.

[0020] According to an embodiment, the device comprises the variable capacitor, the variable capacitor is configured to receive a tuning voltage and the first and second bias voltages, and a difference between the tuning voltage and the first bias voltage and a difference between the tuning voltage and the second bias voltage determine a value of the capacitance.

[0021] According to an embodiment, the device comprises a voltage-controlled oscillator comprising variable the capacitor.

[0022] According to an embodiment, the device comprises a circuit for delivering the tuning voltage, the circuit comprising, for example, a phase-locked loop.

[0023] According to an embodiment, the third circuit comprises a resistor having a first terminal connected to the node of application of the reference potential or to the node of application of the power supply potential, a second terminal of the resistor being configured to deliver the first control voltage and being connected to the back gate of the transistors of the second resistive element.

[0024] According to an embodiment, the third circuit comprises a smoothing capacitor connected between the back gate of the transistors of the second resistive element and the node of application of the reference potential.

[0025] According to an embodiment, the transistors of the second resistive element all are N-channel transistors or all are P-channel MOS transistors.

[0026] According to an embodiment, the transistors of the second resistive element are all implemented on silicon on insulator.

[0027] According to an embodiment, the third circuit comprises a circuit for adjusting a slope of the first control voltage with temperature.

[0028] According to an embodiment, the adjustment circuit comprises one or a plurality of assemblies, each comprising:

[0029] a first resistor and a first switch in series between the node of application of the power supply potential and the second terminal of the resistor delivering the first control voltage, and

[0030] a second resistor and a second switch in series between the second terminal of the resistor delivering the first control voltage and the node of application of the reference potential, a value of the second resistor of the assembly being identical to a value of the first resistor of the assembly.

[0031] According to an embodiment, the adjustment circuit comprises a plurality of the assemblies, and a value of the first resistance is different in each of the assemblies.

[0032] According to an embodiment, the first control voltage is determined by the difference between the second copy of the first current and the copy of the second current, and the slope adjustment circuit comprises a fourth circuit configured to deliver the second copy of the first current, and a fifth circuit configured to deliver the second copy of the second current, a gain of the fourth circuit and a gain of the fifth circuit being adjustable in such a way as to allow the adjustment of the slope of the first control voltage with temperature.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0033] The foregoing features and advantages, as well as others, will be described in detail in the rest of the disclosure of specific embodiments given as an illustration and not limitation with reference to the accompanying drawings, in which:

[0034] FIG. 1 shows, schematically and in the form of blocks, an example of a circuit comprising a variable capacitor;

[0035] FIG. 2 schematically shows an example of a variable capacitor;

[0036] FIG. 3 schematically shows another example of a variable capacitor;

[0037] FIG. 4 shows with curves an example of operation of a circuit comprising a variable capacitor;

[0038] FIG. 5 shows, schematically and partly in the form of blocks, an embodiment of a device;

[0039] FIG. 6 shows an example of another embodiment of a circuit of the device of FIG. 5;

[0040] FIG. 7 shows an example of still another embodiment of the circuit of FIG. 6;

[0041] FIG. 8 shows another embodiment of a resistive component of the device of FIG. 5;

[0042] FIG. 9 shows alternative embodiment of the circuit of FIG. 5; and

[0043] FIG. 10 shows an example of embodiment of another circuit of the device of FIG. 5.

#### DETAILED DESCRIPTION

[0044] Like features have been designated by like references in the various figures. In particular, the structural and/or functional features that are common among the various embodiments may have the same references and may dispose identical structural, dimensional and material properties.

[0045] For clarity, only those steps and elements which are useful to the understanding of the described embodiments have been shown and are described in detail.

[0046] Unless indicated otherwise, when reference is made to two elements connected together, this signifies a direct connection without any intermediate elements other than conductors, and when reference is made to two elements coupled together, this signifies that these two elements can be connected or they can be coupled via one or more other elements.

[0047] In the following description, where reference is made to absolute position qualifiers, such as “front”, “back”, “top”, “bottom”, “left”, etc., “right”, or relative position qualifiers, such as “top”, “bottom”, “upper”, “lower”, etc., or orientation qualifiers, such as “horizontal”, “vertical”, etc., reference is made unless otherwise specified to the orientation of the drawings.

[0048] Unless specified otherwise, the expressions “about”, “approximately”, “substantially”, and “in the order of” signify plus or minus 10% or 10°, preferably of plus or minus 5% or 5°.

[0049] FIG. 1 shows, schematically and in the form of blocks, an example of a circuit VCO comprising a variable capacitor Cvar.

[0050] Circuit VCO is a voltage-controlled oscillator. Circuit VCO is configured to deliver a signal OUT at a frequency Fvco having a value determined by the value of a tuning voltage Vtune. More particularly, tuning voltage Vtune is a voltage for adjusting the capacitance value of variable capacitor Cvar, and the value of the frequency Fvco of signal OUT is at least partly determined by the capacitance value of component Cvar. Voltage Vtune is, for example, received by a terminal 104 of capacitor Cvar.

[0051] In this example, capacitor Cvar also receives a bias voltage Vbias1. Voltage Vbias1 is, for example, received by a terminal 106 of capacitor Cvar. The capacitance value of capacitor Cvar, for example between two terminals 100 and 102 of component Cvar, is then determined by the difference between voltages Vtune and Vbias1.

[0052] Although this is not illustrated in FIG. 1, in other examples, capacitor Cvar is configured to receive, in addition to voltages Vtune and Vbias1, another bias voltage Vbias2. In these other examples, the capacitance value of component Cvar is then determined by the difference between voltages Vtune and Vbias1 and by the difference between voltages Vtune and Vbias2, the difference between voltages Vbias1 and Vbias2 being kept constant.

[0053] As an example, the frequency Fvco of signal OUT is controlled by a phase-locked loop (not shown in FIG. 1). The phase-locked loop is, for example, configured to deliver, or control, voltage Vtune so that frequency Fvco is equal to a set point frequency Flock.

[0054] As an example, the VCO circuit and the phase-locked loop controlling the frequency Fvco of signal OUT form part of a radio frequency circuit and are configured so that the frequency Fvco of signal OUT is greater than 1 GHZ, preferably greater than 10 GHZ, for example approxi-



mately equal to 20 GHz. As an example, the radio frequency circuit is a clock signal generation circuit. As an alternative or complementary example, the radio frequency circuit forms part of a circuit for transmitting and/or receiving a wireless radio frequency signal.

[0055] FIG. 2 schematically shows an example of a variable capacitor Cvar.

[0056] In this example, capacitor Cvar comprises two variable-capacitance components Cvar1 and Cvar2, for example two varactors (or variable-capacitance diodes). The capacitance value of each of components Cvar1 and Cvar2 is determined by the voltage across this component. Each of components Cvar1 and Cvar2 has one electrode coupled, preferably connected, to the terminal 104 receiving voltage Vtune, and another terminal coupled to the terminal 106 receiving voltage Vbias1. For example, dipole Cvar1 is connected between terminal 104 and a node 200 coupled to terminals 106 and 100, dipole Cvar2 being connected between terminal 104 and a node 202 coupled to terminals 106 and 102. For example, node 200, respectively 202, is coupled to terminal 106 by a resistor R1, respectively R2, resistor R1, respectively R2, being for example connected between nodes 200 and 106, respectively between nodes 202 and 106. For example, node 200, respectively 202, is coupled to terminal 100, respectively 102, by a decoupling capacitor Cd1, respectively Cd2, capacitor Cd1, respectively Cd2, being for example connected between nodes 200 and 100, respectively between nodes 202 and 102.

[0057] Voltage Vbias1 is a voltage for biasing component Cvar, and generally has a constant value. By varying the value of voltage Vtune, the voltage across each of components Cvar1 and Cvar2 is modified, which results in a change in the capacitance value of each of components Cvar1 and Cvar2, and thus in the capacitance value of component Cvar.

[0058] FIG. 3 schematically shows another example of a variable capacitor Cvar.

[0059] The capacitor Cvar of FIG. 3 comprises all the elements of the capacitor Cvar of FIG. 2. Thus, unless otherwise indicated, all that has been described for the capacitor Cvar of FIG. 2 applies to the capacitor Cvar of FIG. 3.

[0060] Further, the capacitor Cvar of FIG. 3 comprises two variable-capacitance components Cvar3 and Cvar4, for example two varactors. The capacitance value of each of components Cvar3 and Cvar4 is determined by the voltage across this component. Each of components Cvar3 and Cvar4 has one electrode coupled, preferably connected, to the terminal 104 receiving voltage Vtune, and another terminal coupled to a terminal 108 of component Cvar, terminal 108 receiving voltage Vbias2. For example, dipole Cvar3 is connected between terminal 104 and a node 204 coupled to terminals 108 and 100, dipole Cvar4 being connected between terminal 104 and a node 206 coupled to terminals 108 and 102. For example, node 204, respectively 206, is coupled to terminal 108 by a resistor R3, respectively R4, resistor R3, respectively R4, being for example connected between nodes 204 and 108, respectively between nodes 206 and 108. For example, node 204, respectively 206, is coupled to terminal 100, respectively 102, by a decoupling capacitor Cd3, respectively Cd4, capacitor Cd3, respectively Cd4, being for example connected between nodes 204 and 100, respectively between nodes 206 and 102.

[0061] Voltage Vbias2 is a voltage for biasing component Cvar, and generally has a constant value. Further, the difference between voltages Vbias1 and Vbias2 is preferably constant. By varying the value of the voltage Vtune, the voltage across each of the components Cvar1, Cvar2, Cvar3, and Cvar4 is then modified, which results in a change in the capacitance value of each of components Cvar1, Cvar2, Cvar3, and Cvar4, and thus in the capacitance value of component Cvar.

[0062] The capacitor Cvar of FIG. 3, due to the presence of two bias voltages Vbias1 and Vbias2 rather than of bias voltage Vbias1 only as in FIG. 2, exhibits a variation in its capacitance value with voltage Vtune, which is more linear than that of the capacitor Cvar of FIG. 2. Thus, when capacitor Cvar is used to adjust the frequency of a voltage-controlled oscillator, the variation of the oscillator frequency with voltage Vtune is more linear when the capacitor Cvar of FIG. 3 is used than when the capacitor Cvar of FIG. 2 is used.

[0063] As mentioned hereabove, circuits comprising a variable capacitor have an operation which may depend on temperature in addition to the value of their variable capacitance, which poses a problem. This is for example the case in voltage-controlled oscillators, such as the VCO oscillator of FIG. 1, which have their frequency controlled by a phase-locked loop.

[0064] FIG. 4 illustrates with curves an example of operation of the VCO oscillator of FIG. 1 when the oscillator has its frequency Fvco controlled by a phase-locked loop to set point value Flock.

[0065] A curve Tt illustrates the variation, at a nominal operating temperature, for example room temperature, of the frequency Fvco of the signal OUT of the VCO oscillator as a function of voltage Vtune.

[0066] In this example, frequency Fvco increases, for example substantially linearly, with the value of voltage Vtune.

[0067] The phase-locked loop controls voltage Vtune to a value such that frequency Fvco is equal to frequency Flock (point 400 in FIG. 4). The phase-locked loop is then the to be locked.

[0068] A curve Tc illustrates the variation of the frequency Fvco of the signal OUT of the VCO oscillator as a function of voltage Vtune, at a low temperature lower than the nominal temperature. A curve Th illustrates the variation of the frequency Fvco of the signal OUT of the VCO oscillator as a function of voltage Vtune, at a high temperature, higher than the ambient temperature.

[0069] In this example, for a given voltage value Vtune, frequency Fvco decreases when the temperature rises. Curve Tc then corresponds to a translation of curve Tt towards higher frequencies Fvco, and curve Th then corresponds to a translation of curve Tt towards lower frequencies Fvco.

[0070] Since the frequency Fvco of the VCO oscillator is controlled by the value Flock by the phase-locked loop, in this example where frequency Fvco increases with the increase of voltage Vtune and decreases with the temperature rise, the loop decreases the value of voltage Vtune when the temperature decreases to maintain frequency Fvco equal to frequency Flock. In particular, at the low temperature corresponding to curve Tc, voltage Vtune is decreased to a value corresponding to a point 402 in FIG. 4, for which curve Tc takes value Flock. Symmetrically, the loop increases the value of voltage Vtune when the temperature

risers to maintain frequency  $F_{vco}$  equal to frequency  $F_{lock}$ . In particular, at the high temperature corresponding to curve  $T_c$ , voltage  $V_{tune}$  is increased to a value corresponding to a point **404** of curve  $T_h$ . However, as shown in FIG. 4, at the point **404** corresponding to the maximum value that voltage  $V_{tune}$  can take, frequency  $F_{vco}$  is lower than frequency  $F_{lock}$ , and the phase-locked loop is no longer locked.

**[0071]** The fact that the phase-locked loop can no longer be locked when the temperature varies with respect to the nominal operating temperature may arise when the temperature rises or decreases with respect to the nominal temperature, in circuits where frequency  $F_{vco}$  increases when voltage  $V_{tune}$  increases as illustrated in FIG. 4, but also in circuits where frequency  $F_{vco}$  decreases when voltage  $V_{tune}$  increases, and/or in circuits where frequency  $F_{vco}$  increases when the temperature decreases as shown in FIG. 4, but also in circuits where frequency  $F_{vco}$  decreases when the temperature decreases.

**[0072]** For example, the variation of frequency  $F_{vco}$  with temperature is at least partly linked to the variation of the capacitance value of component  $C_{var}$  with temperature, and, more generally, to the variation with temperature of the values of the components of the oscillator tank.

**[0073]** To decrease the temperature dependency of frequency  $F_{vco}$ , that is, to bring curves  $T_c$  and  $T_h$  closer to curve  $T_t$ , it could be envisaged to replace the component  $C_{var}$  of the VCO circuit with two components  $C_{var}$  in parallel, one being controlled by voltage  $V_{tune}$  as previously described, and the other being controlled by a voltage determined by temperature to compensate for the variation of frequency  $F_{vco}$  with temperature.

**[0074]** However, in addition to increasing the surface area of capacitor  $C_{var}$ , and thus of the VCO circuit, this also increases the number of parasitic capacitors, which poses a problem, particularly in the radio frequency field.

**[0075]** While usually the bias voltage(s)  $V_{bias1}$  and  $V_{bias2}$  of a variable capacitor are constant and do not depend on temperature, it is here provided to make them temperature-dependent.

**[0076]** For example, it is here provided to make the bias voltage  $V_{bias1}$  of a variable capacitor receiving only one bias voltage, or the two bias voltages  $V_{bias1}$  and  $V_{bias2}$  of a variable capacitor receiving two bias voltages, temperature-dependent. The way in which this or these bias voltages are temperature-dependent (increasing with temperature) is determined in such a way as to compensate for the effect of temperature variation on the operation of an electronic circuit comprising a variable capacitor having its capacitance value determined by the difference between a control voltage  $V_{tune}$  and each bias voltage that it receives. According to an embodiment where the variable capacitor receives two bias voltages, it is provided for the difference between the two bias voltages to remain constant when the temperature varies.

**[0077]** Thus, there is here provided a device configured to deliver one or a plurality of voltages for biasing a variable capacitor, each of which is temperature-dependent, for example in such a way as to compensate for the effect of the temperature variation on the operation of a circuit comprising such a variable capacitor. The choice of the way in which each of the variable capacitor bias voltages varies with temperature, for example increases as the temperature rises or decreases as the temperature rises, depends on the application. For example, the choice of the way in which each of

the bias voltages varies according to temperature is made so as to compensate for temperature variations of a parameter having a value at least partly determined by that of the capacitor.

**[0078]** As an example, the circuit is an oscillator, for example configured to deliver a radio frequency signal, and the variable capacitor forms part of the oscillator “tank”. The variation of the bias voltages of the variable capacitor with temperature is then configured to compensate for a variation of the oscillator frequency  $F_{vco}$  with temperature. Indeed, frequency  $F_{vco}$  depends on the value of the capacitance of the oscillator tank and, more generally, on the value of each of the components of this tank, and the values of these components vary with temperature.

**[0079]** FIG. 5 shows, schematically and partly in the form of blocks, an embodiment of such a device **500**.

**[0080]** Device **500** comprises a bandgap circuit designated with reference BG in FIG. 5.

**[0081]** Circuit BG comprises a resistive element **R55** and is configured to apply a temperature-stable voltage across resistive element **R55**, so that a current  $I_{bg}$  flows there-through. In other words, circuit BG is configured to generate the temperature-stable voltage  $V_{bg}$ , and to impose this voltage across resistive element **R55**. A detailed example of circuit BG will be described hereafter in relation with FIG. 10. In addition to current  $I_{bg}$ , circuit BG is further configured to deliver a current  $I_{ptat}$  depending on temperature, preferably linearly with temperature. Current  $I_{ptat}$  is a current proportional to absolute temperature (PTAT) which increases when the temperature rises.

**[0082]** Device **500** also comprises a circuit **C1**. Circuit **C1** comprises a resistive element **R**. Resistive element **R** has a terminal connected to a node **502** configured to receive a reference potential GND, for example the ground. Element **R** is configured to deliver voltage  $V_{bias1}$ , this voltage  $V_{bias1}$  then being available across element **R**. Voltage  $V_{bias1}$  is a bias voltage of a variable capacitor, for example of a variable capacitor  $C_{var}$ .

**[0083]** Element **R** comprises, preferably is formed of, one or a plurality of MOS (Metal Oxide Semiconductor) transistors in series between the conduction terminals of resistive element **R**. Each of these transistors **T** is diode-assembled, that is, has its drain connected to its gate. When component **R** comprises a plurality of transistors **T**, the latter are all of the same type, for example, they are all NMOS transistors, as is the case in the example of FIG. 5, where component **R** comprises exactly two N-channel (or NMOS) transistors **T**. Preferably, transistors **T** are all identical. As an example, an advantage of implementing resistive element **R** with  $Q$  transistors **T** in series, each diode-assembled, is that the small-signal resistance is in  $Q/g_m$  and is thus low,  $Q$  being an integer greater than or equal to 1, and  $g_m$  being the transconductance of a transistor **T**. This result in low noise on the voltages available across the terminals of resistive element **R**.

**[0084]** Circuit **C1** is connected to circuit BG and is configured to deliver a copy  $I_{bgc1}$  of current  $I_{bg}$  to resistive element **R**. In other words, circuit **C1** is configured to deliver a current  $I_{bgc1}$  which is a copy of current  $I_{bg}$ , and so that this current  $I_{bgc1}$  flows between the conduction terminals of component **R**.

**[0085]** In the remainder of the present disclosure, unless otherwise specified, when it is indicated that a first current

is a copy of a second current, this means that the first current is equal to the second current to within a multiplication factor.

[0086] Device 500 further comprises a circuit C2. Circuit C2 is connected to circuit BG. Circuit C2 is configured to deliver a temperature-dependent bias voltage V1 to the back gates of the transistors T of element R. Thus, when the temperature varies, voltage V1 varies, which modifies the resistance value of each of transistors T, and thus the value of the voltage Vbias1 available across element R, that is, the voltage Vbias1 available across the terminal of element R which is not connected to node 502.

[0087] Since transistors T have back gates, they are thus implemented on SOI (Semiconductor On Insulator), for example on FDSOI (Fully Depleted Silicon On Insulator).

[0088] In the embodiment of FIG. 5, circuit C2 is more particularly configured to deliver a copy Iptatc1 of current Iptat and so that voltage V1 is determined by current Iptatc1, for example, varies linearly with this current Iptatc1. Thus, when the temperature varies, current Iptat varies, whereby current Iptatc1 varies, resulting in a corresponding variation of voltage V1. The variation of voltage V1 results in a variation of the resistance value of component R, and thus in a corresponding variation of voltage Vbias1. Accordingly, by not changing the value of voltage Vtune, the capacitance value of a variable capacitor such as that of FIG. 2 is modified when the temperature varies.

[0089] In the embodiment shown in FIG. 5, device 500 is configured to also deliver bias voltage Vbias2 in addition to voltage Vbias1. Voltages Vbias1 and Vbias2 are bias voltages of a variable capacitor, for example of the variable capacitor Cvar of FIG. 3. For this purpose, in circuit C1, resistive element R is connected in series with a resistor R51. Thus, a terminal of element R is connected to node 502, another terminal of element R is connected to a terminal of resistor R51 and delivers voltage Vbias1, and the other terminal of resistor R51 delivers voltage Vbias2. Preferably, resistor R51 is matched to resistor R55, whereby the difference between voltages Vbias1 and Vbias2 is constant and, in particular, does not depend on temperature, since current Ibgc1 is a copy of current Ibg equal to Vbg/R55.

[0090] According to an embodiment, when device 500 is configured to deliver both voltages Vbias1 and Vbias2, device 500 comprises a variable capacitor (not shown in FIG. 5) configured to receive bias voltages Vbias1 and Vbias2 and tuning voltage Vtune and having its capacitance value determined by the difference between voltages Vbias1 and Vtune and by the difference between voltages Vbias2 and Vtune. As an example, this variable capacitor is the capacitor Cvar described in relation with FIG. 3. According to an embodiment, the device further comprises a voltage-controlled oscillator, for example the VCO oscillator of FIG. 1, comprising this variable capacitor. According to an embodiment, the device comprises a circuit for delivering voltage Vtune, for example a phase-locked loop.

[0091] In another embodiment, non-illustrated, device 500 is configured to only deliver bias voltage Vbias1. In this other embodiment, resistor R51 may be omitted.

[0092] According to an embodiment, when device 500 is configured to only deliver bias voltage Vbias1, device 500 comprises a variable capacitor configured to receive voltage Vbias1 and a control voltage Vtune, and having its capacitance value determined by the difference between voltages Vbias1 and Vtune. As an example, this variable capacitor is

the capacitor Cvar described in relation with FIG. 2. According to an embodiment, the device further comprises a voltage-controlled oscillator, for example the VCO oscillator of FIG. 1, comprising this variable capacitor. According to an embodiment, the device comprises a circuit for delivering voltage Vtune, for example a phase-locked loop.

[0093] According to an embodiment, as illustrated in FIG. 5, circuit C2 comprises a resistor R52 configured to deliver voltage V1. Resistor R52 has a terminal connected to node 502 and another terminal connected to the back gate of transistors T (or node 600), voltage V1 being available on this other terminal. In the example of embodiment of FIG. 5, circuit C2 is configured to deliver current Iptatc1 to node 600. Current Iptatc1 then flows between the terminals of resistor R52, which converts current Iptatc1 into voltage V1.

[0094] As an example, resistor R52 has a value such that, at the nominal operating temperature, voltage V1 is equal to half a power supply potential VDD of device 500, potential VDD being preferably positive and referenced to potential GND.

[0095] Preferably, circuit C2 comprises a smoothing capacitor Cf connected between node 600 and node 502.

[0096] As an example, circuit BG comprises a P-channel MOS transistor T1 configured so that current Iptat flows therethrough, and circuit C2 comprises a P-channel MOS transistor T2 mirror-assembled with transistor T1 so that transistor T2 delivers current Iptatc1 to node 600. Transistor T2 is, in the example shown in FIG. 5, connected to node 600 and in series with resistor R52 configured to deliver voltage V1.

[0097] As a more detailed example, transistor T1 has its source coupled to a node 504 configured to receive power supply potential VDD, for example via a resistor R53, resistor R53 preferably having one terminal connected to transistor T1 and one terminal connected to node 504. The gate of transistor T1 is connected to node A. Transistor T2 then has its gate connected to node A and its source coupled to node 504, for example by a resistor R54, resistor R54 preferably having one terminal connected to transistor T2 and one terminal connected to node 504.

[0098] As an example, circuit BG further comprises a P-channel MOS transistor T3 configured so that current Ibg flows therethrough, and circuit C1 comprises a P-channel MOS transistor T4 mirror-assembled with transistor T3 so that transistor T4 delivers current Ibgc1. Transistor T4 is series-connected with resistive element R. Transistor T3 is, for example, series-connected with resistive element R55, across which circuit BG applies temperature-stable voltage Vbg. Resistive element R55, for example a resistor, has a terminal connected to node 502. As a result, current Ibg flows between the terminals of element R55, that is, through element R55, and through transistor T3 series-connected with element R55 between nodes 504 and 502. Transistor T3 has its source coupled to node 504, for example via a resistor R56, resistor R56 having one terminal connected to transistor T3 and one terminal connected to node 504. The gate of transistor T3 is connected to node B. Transistor T4 then has its gate connected to node B and its source coupled to node 504, for example by a resistor R57, resistor R57 preferably having one terminal connected to transistor T4 and one terminal connected to node 504. Transistor T4 is in series with resistor R57 between nodes 504 and 502.

[0099] In the example of embodiment described in relation with FIG. 5, circuit C2 is configured to deliver current

Iptatc1, which is a copy of current Iptat, to deliver the voltage V1 determined by current Iptatc1, and to apply voltage V1 to the back gate of the transistors T of resistive element R.

[0100] In other examples of embodiments, as will be described in relation with FIGS. 6 and 7, circuit C2 is configured to deliver a copy of current Ibg to node 600 and a copy of current Iptat to node 600, to deliver voltage V1 which is then determined by a difference between these two current copies, and to apply voltage V1 to the back gate of the transistors T of resistive element R.

[0101] FIG. 6 shows an example of such an embodiment of circuit C2.

[0102] The circuit C2 of FIG. 6 comprises, like the example of circuit C2 described in relation with FIG. 5, transistor T2 configured to deliver current Iptatc1. Transistor T2 has its source coupled to node 504, for example by resistor R54, and its drain coupled, for example connected, to node 600, corresponding to the node of connection of transistor T2 to resistor R52.

[0103] Circuit C2 further comprises a circuit C3 configured to deliver a copy Ibgc3 of current Ibg.

[0104] Current Ibgc3 is delivered to node 600 so that a current Idiff flowing through resistor R52 is equal to the difference between currents Iptatc1 and Ibgc3. More precisely, in the example of FIG. 6, circuit C3 is configured so that current Idiff is equal to current Iptatc1 minus current Ibgc3. Thus, when the temperature rises, current Idiff increases, whereby voltage V1 increases.

[0105] As an example, circuit C3 comprises a P-channel MOS transistor T5 configured to deliver a copy Ibgc2 of current Ibg, transistor T5 being mirror-assembled with transistor T3. For example, transistor T5 has its source coupled to node 504, for example via a resistor R58, resistor R58 preferably having one terminal connected to transistor T5 and one terminal connected to node 504. The gate of transistor T5 is connected to node B. The drain of transistor T5 is coupled to node 600.

[0106] In the example of FIG. 6, transistor T5 is coupled to node 600 by a current mirror 602 comprising an N-channel MOS transistor, current mirror 602 here being configured to deliver current Ibgc3 based on current Ibgc2. For example, current mirror 602 comprises an N-channel MOS transistor T6 having its drain connected to a node 604 and its source coupled to node 502, for example by a resistor R59, resistor R59 for example having one terminal connected to node 502 and one terminal connected to the source of transistor T6. The gate of transistor T6 is connected to the drain of transistor T6. Current mirror 602 further comprises an N-channel MOS transistor T7 having its drain connected to node 600 and its source coupled to node 502, for example by a resistor R60, resistor R60 having for example one terminal connected to node 502 and one terminal connected to the source of transistor T7. The gate of transistor T7 is connected to the gate of transistor T6. In the example of FIG. 6, transistor T5 is connected to node 604 by its drain.

[0107] FIG. 7 shows an example of another embodiment of circuit C2.

[0108] As compared with FIG. 6, in the example of FIG. 7, circuit C2 is configured so that the current Idiff through resistor R52 is equal to the difference between the copy Ibgc2 of current Ibg and a copy Iptatc2 of current Iptat, and, more precisely, so that current Idiff is equal to current Ibgc2

minus current Iptatc2. Thus, when the temperature rises, current Idiff decreases, whereby voltage V1 decreases.

[0109] The circuit C2 of FIG. 7 thus differs from the circuit C2 of FIG. 6 in that:

[0110] the transistor T2 configured to deliver current Iptatc1 to node 600 in the circuit C2 of FIG. 6 has been replaced with the transistor T5 configured to deliver current Ibgc2 in the circuit C2 of FIG. 7, so that current Ibgc2 is delivered to node 600; and

[0111] the circuit C3 of the circuit C2 of FIG. 7 is not configured to deliver current Ibgc3 to node 600, as was the case in FIG. 6, but to deliver current Iptatc2 to node 600.

[0112] For example, transistor T5 remains mirror-assembled with transistor T3, with its gate connected to node B, its source coupled to node 504, for example via resistor R58, but its drain is connected to node 600 rather than to node 604 as was the case in FIG. 6. Symmetrically, transistor T2 remains mirror-assembled with transistor T1, with its gate connected to node A, its source coupled to node 504, for example via resistor R54, but its drain is connected to node 604 coupled to node 600 by current mirror 602. Current mirror 602 then delivers current Iptatc2 from current Iptatc1.

[0113] In the device 500 described hereabove in relation with FIGS. 5 to 7, the resistive element is formed of MOS transistors in series, each diode-assembled. This enables to decrease the noise on voltage Vbias1 as compared with a device in which a temperature-dependent current would have been directly supplied to a resistor to obtain voltage Vbias across this resistor.

[0114] Further, the provision of the component R such as described enables to adapt the gain between a temperature variation and a corresponding variation of voltage Vbias1 by modifying the number of transistors T in component R.

[0115] In the examples and variants described hereabove, component R comprises, preferably is formed of, one or a plurality of N-channel MOS transistors T.

[0116] FIG. 8 shows another example of the resistive component R of the device of FIG. 5.

[0117] In the component R of the embodiment of FIG. 8, each transistor T of component R has a P channel rather than an N channel as previously described.

[0118] Although this is not illustrated in FIG. 8, the drain of transistors T is then on the side of node 502. For example, the transistor T of the resistive element R which has a terminal connected to node 502 has its drain connected to node 502.

[0119] As compared with the case where transistors T have an N channel, the variation direction of voltage V1 with temperature is reversed for a corresponding case where transistors T have a P channel, so that the variation direction of voltage Vbias1 with temperature remains the same.

[0120] FIG. 9 shows an alternative embodiment of circuit C2. In FIG. 9, the alternative embodiment is applied to the circuit C2 of FIG. 6, although this variant may also be applied to the circuit C2 of FIG. 7, this last implementation being within the abilities of those skilled in the art based on the description made hereafter in relation with FIG. 9.

[0121] In this variant, circuit C2 comprises a circuit for adjusting the slope of voltage V1 with temperature, and thus the slope of voltage Vbias1 with temperature. This enables to adjust the way in which the variation of frequency Fvco with temperature is compensated for by the variation of voltage Vbias1 with temperature, for example so that, for a

given voltage  $V_{tune}$ , the variation of frequency  $F_{vco}$  with temperature is as small as possible.

[0122] More specifically, in the example of FIG. 9, this adjustment circuit comprises a plurality of assemblies  $K_i$ , where  $i$  is a positive integer. In the example of FIG. 9,  $i$  is equal to 3.

[0123] Each assembly  $K_i$  ( $K_1$ ,  $K_2$ ,  $K_3$  in FIG. 9) comprises:

[0124] a resistor  $R_{8i}$  ( $R_{81}$ ,  $R_{82}$ ,  $R_{83}$  in FIG. 9) and a switch  $SW_{8i}$  ( $SW_{81}$ ,  $SW_{82}$ ,  $SW_{83}$  in FIG. 9) series-connected between node 600 and node 502; and

[0125] a resistor  $R_{9i}$  ( $R_{91}$ ,  $R_{92}$ ,  $R_{93}$  in FIG. 9) and a switch  $SW_{9i}$  ( $SW_{91}$ ,  $SW_{92}$ ,  $SW_{93}$  in FIG. 9) series-connected between node 600 and node 504.

[0126] For example, in each assembly  $K_i$ , switch  $SW_{8i}$  is connected to node 502 and switch  $sw_{9i}$  is connected to node 504.

[0127] In each assembly  $K_i$ , the resistor  $R_{8i}$  of the assembly is identical to the resistor  $R_{9i}$  of this assembly  $K_i$ . For example, each resistor  $R_{8i}$  is matched to the corresponding resistor  $R_{9i}$ . Further, for each assembly  $K_i$ , the value of the resistors  $R_{8i}$  and  $R_{9i}$  of assembly  $K_i$  is preferably different from that of the resistors  $R_{8i}$  and  $R_{9i}$  of the other assemblies  $K_i$ .

[0128] For example, in a configuration the to be “binary”, for  $i$  greater than or equal to 2, the value of the resistor  $R_{9i}$ , respectively  $R_{8i}$ , of index  $i$  is equal to twice the value of the resistor  $R_{9i-1}$ , respectively  $R_{8i-1}$ , of index  $i-1$ . For example, in each assembly  $K_i$ , the value of the resistors  $R_{8i}$  and  $R_{9i}$  in the assembly is a multiple of the value of resistor  $R_{52}$ . For example, in each assembly  $K_i$ , the value of resistors  $R_{8i}$  and  $R_{9i}$  is equal to 2 ( $i-1$ ) times the value of resistor  $R_{52}$ .

[0129] As another example, in a configuration the to be “thermometric”, the value of each resistor  $R_{8i}$ , respectively  $R_{9i}$ , is determined, for example during an adjustment or calibration phase, independently from the value of the other resistors  $R_{8i}$ , respectively  $R_{9i}$ .

[0130] The switches  $SW_{8i}$  and  $SW_{9i}$  of assemblies  $K_i$  are controlled by a digital signal trim delivered by a circuit, not shown. For example, signal trim comprises  $i$  bits, each bit of signal trim controlling a corresponding assembly  $K_i$ . Signal trim is configured so that the switches  $SW_{9i}$  and  $SW_{8i}$  of the same assembly  $K_i$  are in the same on or off state.

[0131] In another non-illustrated example of implementation of the circuit for adjusting the slope of voltage  $V_{bias1}$  with temperature, the adjustment circuit comprises:

[0132] a circuit configured to deliver the copy of current  $I_{ptat}$  to node 600, that is, the transistor  $T_2$  delivering copy  $I_{ptatc1}$  in the embodiment of FIG. 6 and the circuit  $C_3$  delivering the copy  $I_{ptatc2}$  in the embodiment of FIG. 7; and

[0133] a circuit configured to deliver the copy of current  $I_{bg}$  to the node 600, that is, the circuit  $C_3$  delivering copy  $I_{bgc3}$  in the embodiment of FIG. 6, and the transistor  $T_5$  delivering copy  $I_{bgc2}$  in the embodiment of FIG. 7, and, further, the gain of the circuit delivering the copy of current  $I_{bg}$  to node 600 is adjustable, just as the gain of the circuit delivering the copy of current  $I_{ptat}$  to node 600.

[0134] Thereby, the adjustment of the gains of these two circuits enables to adjust or set the slope of voltage  $V_1$ , and thus of voltage  $V_{bias1}$ , with temperature.

[0135] In the described embodiments, when the copy  $I_{ptatc1}$  of current  $I_{ptat}$  which is delivered to node 600

corresponds to a positive current (as in FIG. 6), voltage  $V_1$  increases with temperature. Conversely, when the copy  $I_{ptatc2}$  of the current  $I_{ptat}$  supplied to node 600 corresponds to a negative current, that is, a positive current  $I_{ptatc2}$  drawn from node 600 (case of FIG. 7), voltage  $V_1$  decreases with temperature.

[0136] There is considered as an example the case where the circuit configured to deliver the copy of current  $I_{ptat}$  to node 600 comprises transistor  $T_2$  in series with resistor  $R_{52}$  (FIG. 6), and where the circuit configured to deliver the copy of current  $I_{bg}$  to node 600 corresponds to the circuit  $C_3$  of FIG. 6. In this example, transistor  $T_2$  is implemented by a plurality of P-channel MOS transistors selectively connected in parallel with one another by switches controlled by a first control signal, so that the current  $I_{ptatc1}$  delivered by transistor  $T_2$  to node 600 is equal to  $\alpha \cdot I_{ptatunit}$ , with  $\alpha$  a factor, preferably integer, having its value depending on the state of the first control signal, and  $I_{ptatunit}$  a current determined by current  $I_{ptat}$ , for example proportional or equal to current  $I_{ptat}$ . Still in this example, transistor  $T_7$  (or alternatively transistor  $T_5$ , although this may result in the source drain saturation voltage of transistor  $T_7$  not being constant, which causes saturation problems for transistor  $T_7$  at high currents) is implemented by a plurality of N-channel MOS transistors (P-channel when this concerns transistor  $T_5$ ) selectively connected in parallel with one another by switches controlled by a second control signal, so that the current  $I_{bgc3}$  delivered by transistor  $T_7$  to node 600 is equal to  $\beta \cdot I_{bgunit}$ , with  $\beta$  a factor, preferably integer, having its value depending on the state of the second control signal, and  $I_{bgunit}$  a current determined by current  $I_{bg}$ , for example proportional or equal to current  $I_{bg}$ . The modification of the values of gains  $\alpha$  and  $\beta$  then enables to adjust the slope of voltage  $V_1$ , and thus of voltage  $V_{bias1}$ , with temperature.

[0137] Preferably, in the above example, the values of gains  $\alpha$  and  $\beta$  and of currents  $I_{bgunit}$  and  $I_{ptatunit}$  are configured so that, at the nominal operating temperature, voltage  $V_1$  is equal to  $V_{DD}/2$ . In other words, gains  $\alpha$  and  $\beta$  are selected so that, at the nominal operating temperature,  $\alpha \cdot I_{ptatunit} - \beta \cdot I_{bgunit} = V_{DD}/(2 \cdot R_{52})$ , which sets the relationship between  $\alpha$  and  $\beta$ , for example because the currents  $I_{ptatunit}$  and  $I_{bgunit}$  at the nominal temperature are known. For example, when, at the nominal operating temperature  $I_{ptatunit}$ , is equal to  $I_{bgunit}$  and to current  $I_{diff}$  with  $V_1$  equal to  $V_{DD}/2$ , gains  $\alpha$  and  $\beta$  verify  $\alpha - \beta = 1$ .

[0138] The case where the circuit configured to deliver the copy of current  $I_{ptat}$  to node 600 corresponds to circuit  $C_3$  (FIG. 7) and where the circuit configured to deliver the copy of current  $I_{bg}$  to node 600 comprises transistor  $T_5$  in series with resistor  $R_{52}$  (FIG. 7) is considered as another example. In this example, transistor  $T_5$  is implemented by a plurality of P-channel MOS transistors selectively connected in parallel with one another by switches controlled by a first control signal, so that the current  $I_{bgc2}$  delivered by transistor  $T_5$  to node 600 is equal to  $\beta \cdot I_{bgunit}$ , with  $\beta$  a factor, preferably integer, having its value depending on the state of the first control signal, and  $I_{bgunit}$  a current determined by current  $I_{bg}$ , for example proportional or equal to current  $I_{bg}$ . Still in this example, transistor  $T_7$  (or alternatively transistor  $T_2$ , although this may result in the source drain saturation voltage of transistor  $T_7$  not being constant, which results in saturation problems for transistor  $T_7$  at high currents) is implemented by a number of N-channel MOS transistors (P-channel when this concerns transistor  $T_2$ ) selectively

connected in parallel with one another by switches controlled by a second control signal, so that the current  $I_{ptc2}$  supplied by transistor T7 to node 600 is equal to  $\alpha \cdot I_{ptatunit}$ , with  $\alpha$  a factor, preferably integer, having its value depending on the state of the second control signal, and  $I_{ptatunit}$  a current determined by current  $I_{ptat}$ , for example proportional or equal to current  $I_{ptat}$ . The modification of the values of gains  $\alpha$  and  $\beta$  then enables to adjust the slope of voltage V1, and thus of voltage Vbias1, with temperature.

[0139] Preferably, in the above example, the values of gains  $\alpha$  and  $\beta$  and of currents  $I_{bgunit}$  and  $I_{ptatunit}$  are configured so that, at the nominal operating temperature, voltage V1 is equal to  $VDD/2$ . In other words, gains  $\alpha$  and  $\beta$  are selected so that, at the nominal operating temperature,  $\beta \cdot I_{bgunit} - \alpha \cdot I_{ptatunit} = VDD/(2 \cdot R52)$ , which sets the relationship between  $\alpha$  and  $\beta$ , for example because the currents  $I_{ptatunit}$  and  $I_{bgunit}$  at the nominal temperature are known. For example, when, at the nominal operating temperature,  $I_{ptatunit}$  is equal to  $I_{bgunit}$  and to current  $I_{diff}$  with V1 equal to  $VDD/2$ , the gains  $\alpha$  and  $\beta$  verify  $\beta - \alpha = 1$ .

[0140] In the above-described embodiments and variants, resistor R52 is connected between node 600 and node 502. In other embodiments and variants, as compared with what has been previously described, resistor R52 is connected between node 600 and node 504. The implementation of these other embodiments and variants is within the abilities of those skilled in the art based on the functional indications given hereabove.

[0141] FIG. 10 illustrates an example of a circuit BG that can be used to implement device 500, it being understood that those skilled in the art may provide using other circuits BG.

[0142] In this example, circuit BG comprises transistor T1 having its source coupled to node 504, for example by resistor R53, its gate connected to node A, and its drain connected to its gate, and transistor T3 having its source coupled to node 504, for example by resistor R56, its gate connected to node B, and its drain connected to a terminal 1000 of resistor R55, the other terminal 1002 of resistor R55 being connected to node 502. As an example, a compensation capacitor is connected between the gate B of transistor T3 and node 504, to improve the stability.

[0143] Circuit BG further comprises an NPN bipolar transistor T8 coupling the drain A of transistor T1 to node 502. Transistor T8 has, for example, its collector connected to node A, and its emitter coupled to node 502 by a resistor R61. The base of transistor T8 is connected to terminal 1000 of resistor R55.

[0144] Circuit BG also comprises a P-channel MOS transistor T9 mirror-assembled with transistor T1. Transistor T9 has, for example, its gate connected to node A, its source coupled to node 502, for example via a resistor R62 preferably connected between node 504 and transistor T9. An NPN bipolar transistor T10 of circuit BG couples the drain of transistor T9 to resistor R61. Transistor T10 has its base connected to the base of transistor T8, and, for example, its collector connected to the drain of transistor T9 and its emitter coupled to resistor R61, for example via a resistor R63 preferably having one terminal connected to transistor T10 and another terminal connected to resistor R61.

[0145] Transistors T1, T8, T9, and T10, and resistors R53, R61, R62, and R63 are sized so that the voltage Vbg on terminal 1000 of resistor R55 is temperature-stable, that is constant with temperature. Further, bipolar transistors T8

and T10 are, for example, sized so that the current in transistor T8 is of PTAT type. For example, transistor T10 is implemented by a parallel connection of a plurality of transistors identical to transistor T8, so that the voltage across resistor R63 is of PTAT type.

[0146] Those skilled in the art will understand that certain features of these various embodiments and variants may be combined, and other variants will occur to those skilled in the art.

[0147] Finally, the practical implementation of the described embodiments and variants is within the abilities of those skilled in the art based on the functional indications given hereabove.

1. A device comprising:

a first bandgap circuit configured to apply a temperature-stable voltage across a first resistive element so that a first current flows therethrough, and to deliver a second current proportional to absolute temperature;

a second resistive element comprising one or a plurality of MOS transistors in series and each connected as a diode, the second resistive element having a first terminal connected to a node of application of a reference potential and a second terminal coupled to a node of application of a power supply potential;

a second circuit connected to the first circuit and configured to deliver a first copy of the first current and so that the first copy of the first current flows through the second resistive element; and

a third circuit connected to the first circuit and configured to:

deliver a copy of the second current, deliver a first control voltage from the copy of the second current, and apply the first control voltage to a back gate of the transistors of the second resistive element, or deliver a second copy of the first current and a copy of the second current, supply a first control voltage from a difference between the second copy of the second current and the first copy of the first current, and apply the first control voltage to a back gate of the transistors of the second resistive element.

2. The device of claim 1, wherein the second terminal of the second resistive element is configured to deliver a bias voltage to a variable capacitor.

3. The device of claim 2, wherein the device comprises the variable capacitor;

wherein the variable capacitor is configured to receive a tuning voltage and the bias voltage; and

wherein a difference between the tuning voltage and the bias voltage determines a value of a capacitance of the variable capacitor.

4. The device of claim 3, wherein the device comprises a voltage-controlled oscillator comprising the variable capacitor.

5. The device of claim 4, wherein the device comprises a circuit for delivering the tuning voltage, the circuit comprising, for example, a phase-locked loop.

6. The device of claim 1, wherein the second resistive element is in series with a resistor;

wherein the second terminal of the second resistive element is configured to deliver a first bias voltage to a variable capacitor and is connected to a first terminal of the resistor; and

wherein a second terminal of the resistor is configured to deliver a second bias voltage to the variable capacitor.

7. The device of claim 6, wherein the device comprises the variable capacitor;

wherein the variable capacitor is configured to receive a tuning voltage and the first and second bias voltages; and

wherein a difference between the tuning voltage and the first bias voltage and a difference between the tuning voltage and the second bias voltage determine a value of a capacitance of the variable capacitor.

8. The device of claim 7, wherein the device comprises a voltage-controlled oscillator comprising the variable capacitor.

9. The device of claim 8, wherein the device comprises a circuit for delivering the tuning voltage, the circuit comprising, for example, a phase-locked loop.

10. The device of claim 1, wherein the third circuit comprises a resistor having a first terminal connected to the node of application of the reference potential or to the node of application of the power supply potential, a second terminal of the resistor being configured to deliver the first control voltage and being connected to the back gate of the transistors of the second resistive element.

11. The device of claim 8, wherein the third circuit comprises a smoothing capacitor connected between the back gate of the transistors of the second resistive element and the node of application of the reference potential.

12. The device of claim 1, wherein the transistors of the second resistive element all are N-channel transistors or all are P-channel MOS transistors.

13. The device of claim 1, wherein the transistors of the second resistive element are all implemented on silicon on insulator.

14. The device of claim 1, wherein the third circuit comprises a circuit for adjusting a slope of the first control voltage with temperature.

15. The device of claim 14, wherein the third circuit comprises a resistor having a first terminal connected to the node of application of the reference potential or to the node of application of the power supply potential, a second terminal of the resistor being configured to deliver the first control voltage and being connected to the back gate of the transistors of the second resistive element;

wherein an adjustment circuit comprises one or a plurality of assemblies, each comprising:

a first resistor and a first switch in series between the node of application of the power supply potential and the second terminal of the resistor delivering the first control voltage; and

a second resistor and a second switch in series between the second terminal of the resistor delivering the first control voltage and the node of application of the reference potential, a value of the second resistor of the assembly being identical to a value of the first resistor of the assembly.

16. The device of claim 15, wherein the adjustment circuit comprises a plurality of the assemblies; and wherein a value of the first resistor is different in each of the assemblies.

17. The device of claim 14, wherein the first control voltage is determined by the difference between the second copy of the first current and the copy of the second current; and

wherein a slope adjustment circuit comprises a fourth circuit configured to deliver the second copy of the first current, and a fifth circuit configured to deliver the second copy of the second current, a gain of the fourth circuit and a gain of the fifth circuit being adjustable in such a way as to allow the adjustment of the slope of the first control voltage with temperature.

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