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(54) **GATE DRIVER AND DISPLAY APPARATUS INCLUDING THE SAME**

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(57) **ABSTRACT**

A gate driver and a display apparatus including the same are discussed. The gate driver can include a plurality of stages. An n^{th} stage among the plurality of stages includes a pull-up transistor configured to control a flow of a current between an output node and an input terminal for an n^{th} clock based on a voltage of a Q node, a pull-down transistor configured to control a flow of a current between the output node and an input terminal of a first low power source based on a voltage of a QB node, and a QB node controller configured to control the voltage of the QB node based on a voltage of a control power source and the voltage of the Q node, where n is an integer.

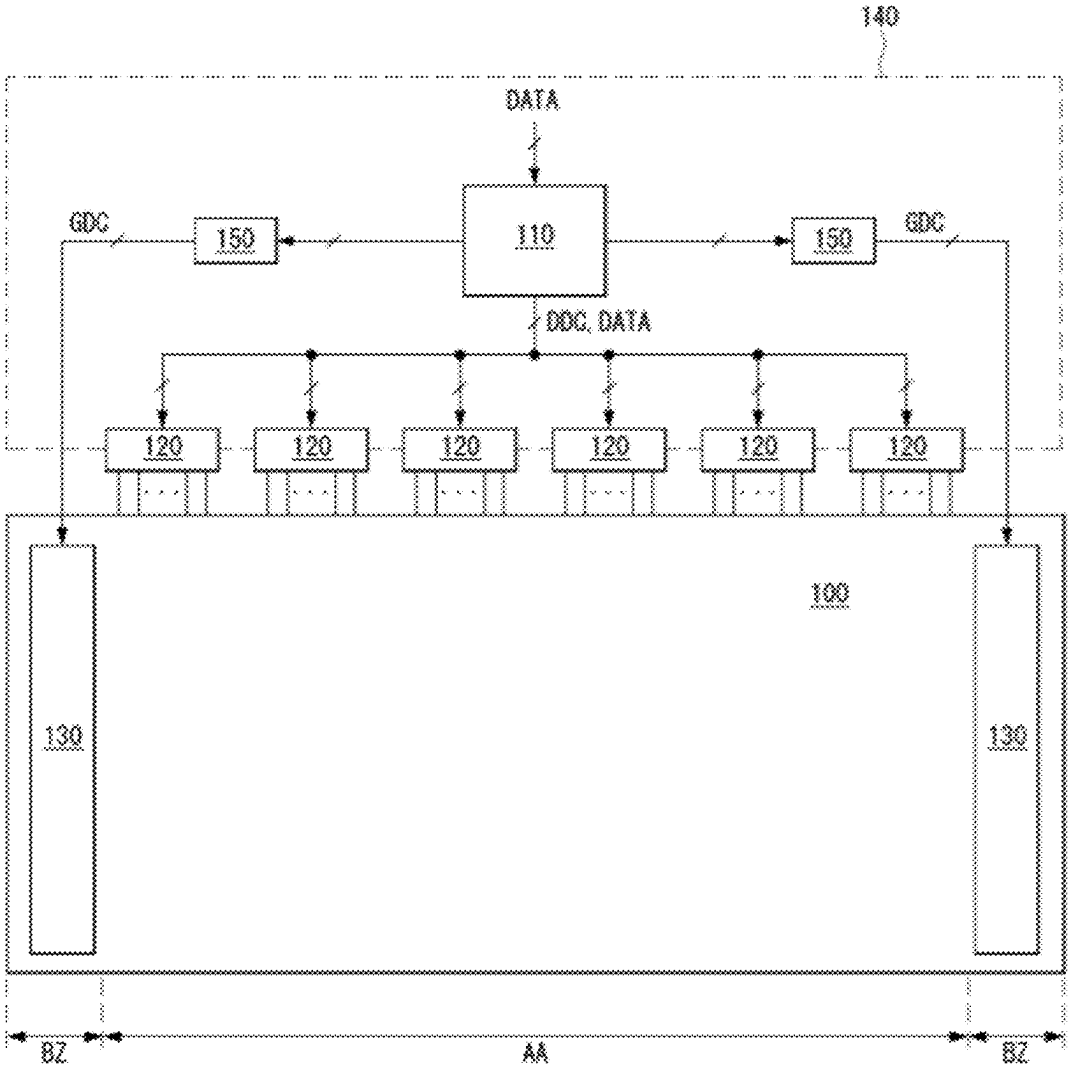


FIG. 1

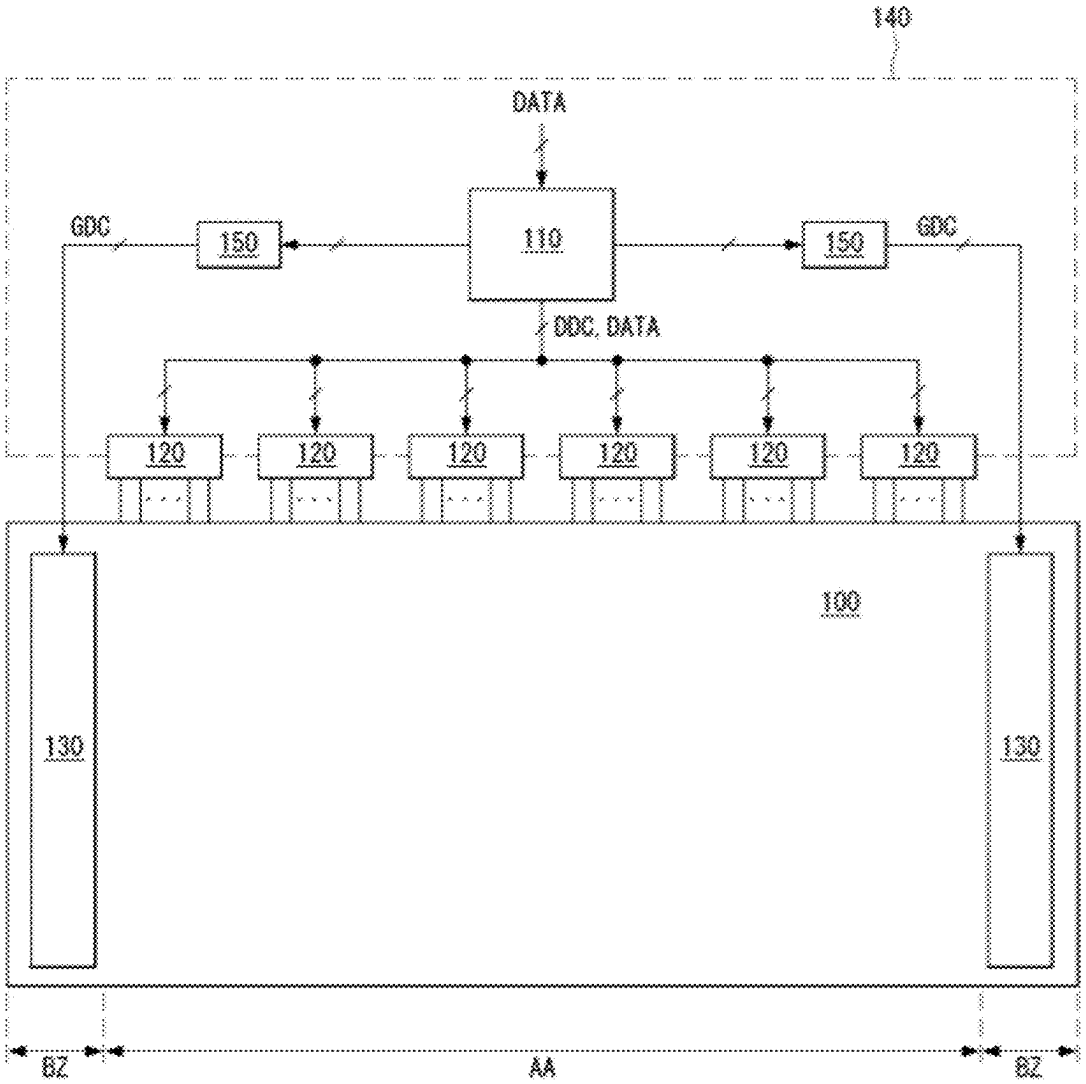

140
DATA
GDC
150
110
150
GDC
DDC, DATA
120
120
120
120
120
120
100
130
130
BZ
AA
BZ

FIG. 2

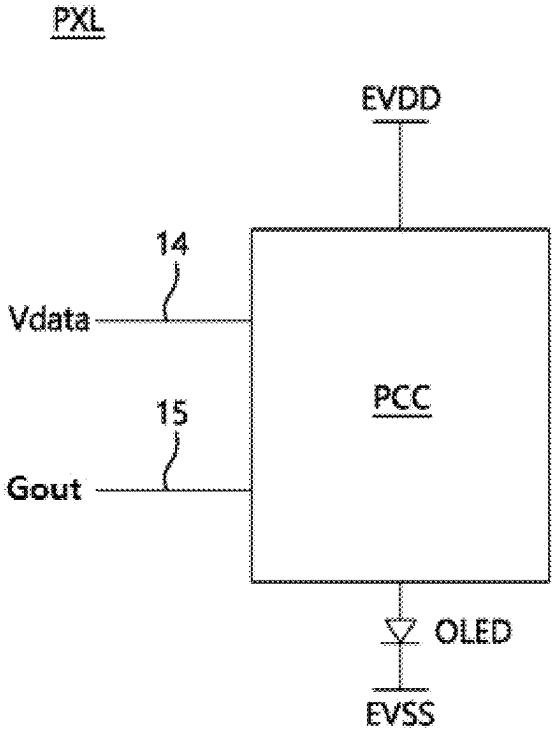


FIG. 3

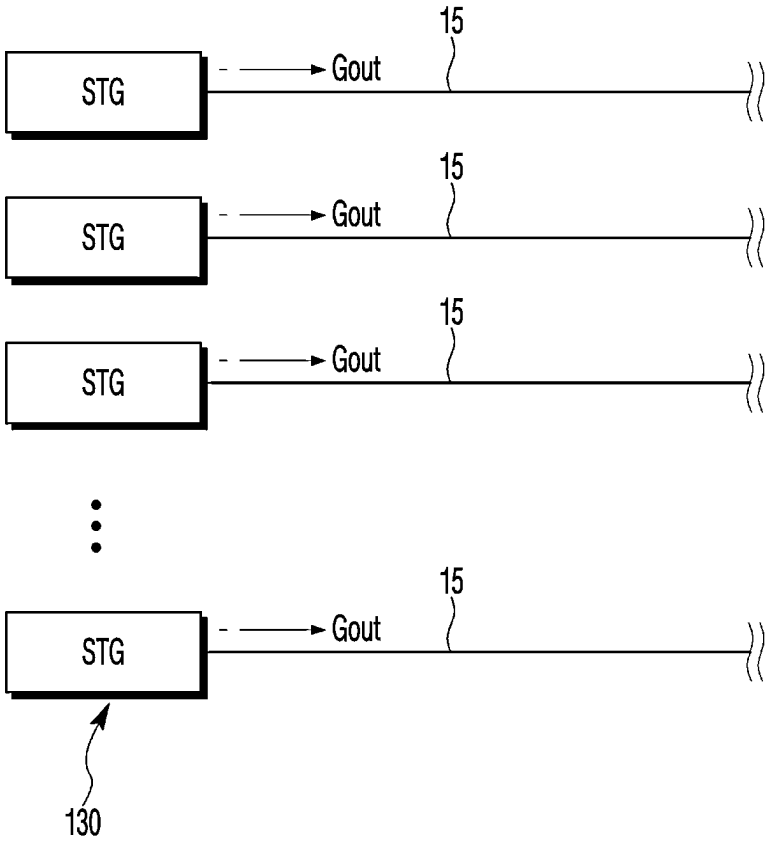


FIG. 4

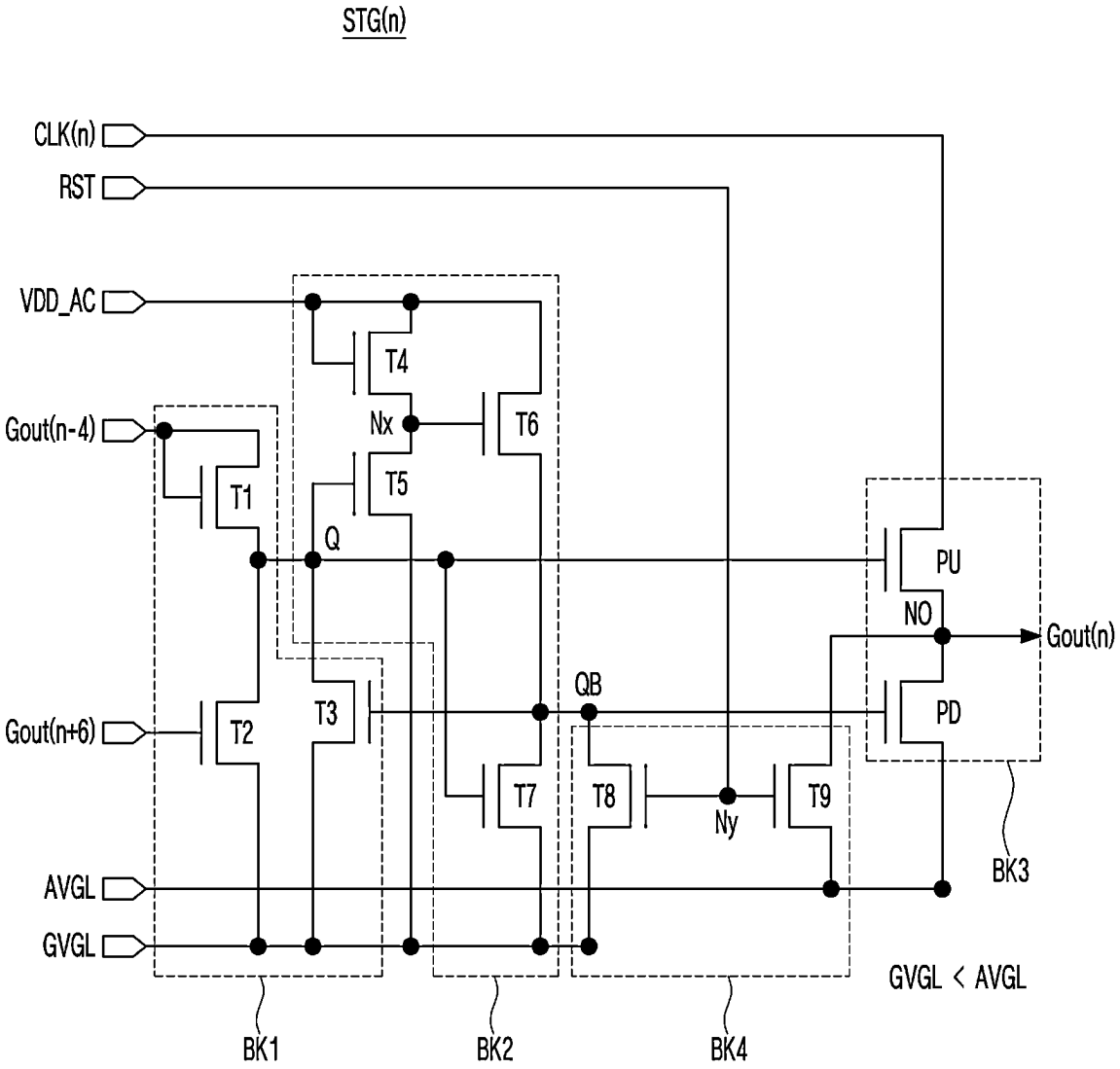

STG(n)
CLK(n)
RST
VDD_AC
Gout(n-4)
Gout(n+6)
AVGL
GVGL
T1
T2
T3
T4
T5
T6
T7
T8
T9
Nx
Ny
Q
QB
PU
PD
NO
Gout(n)
BK1
BK2
BK3
BK4
GVGL < AVGL

FIG. 5

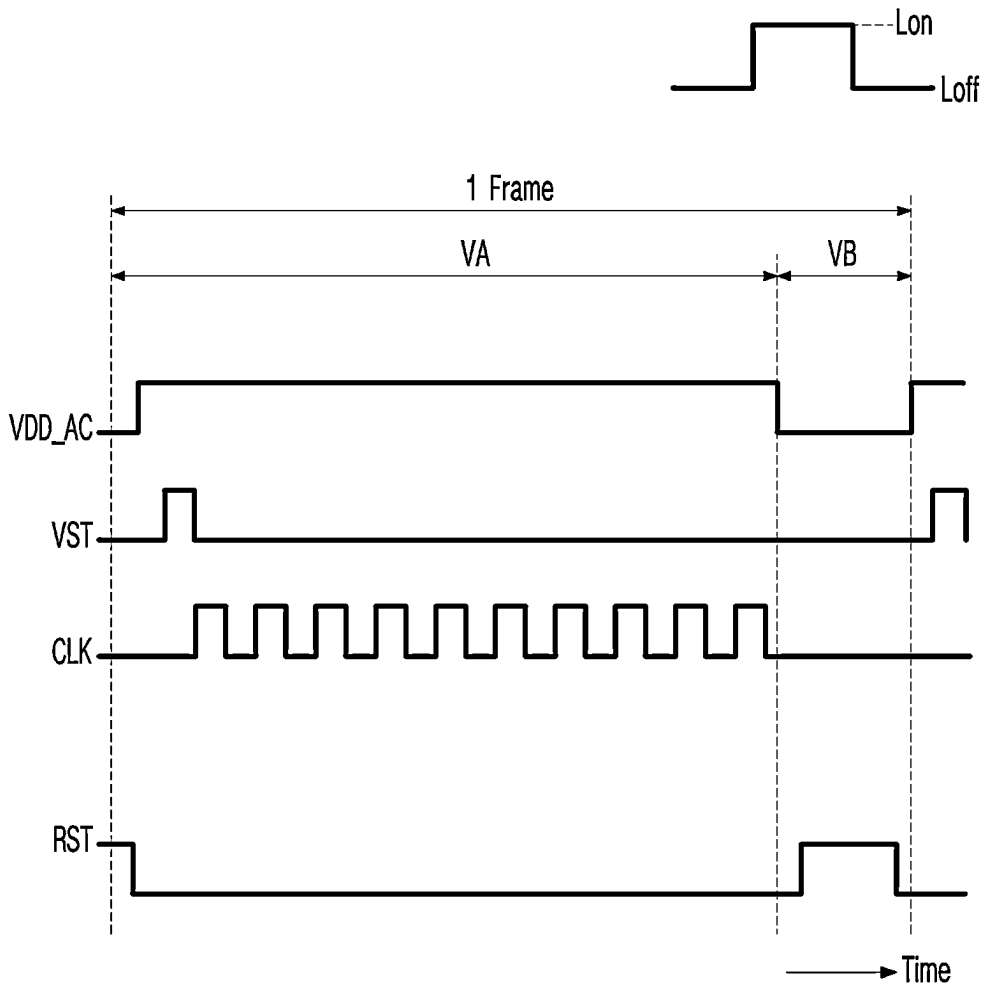


FIG. 6

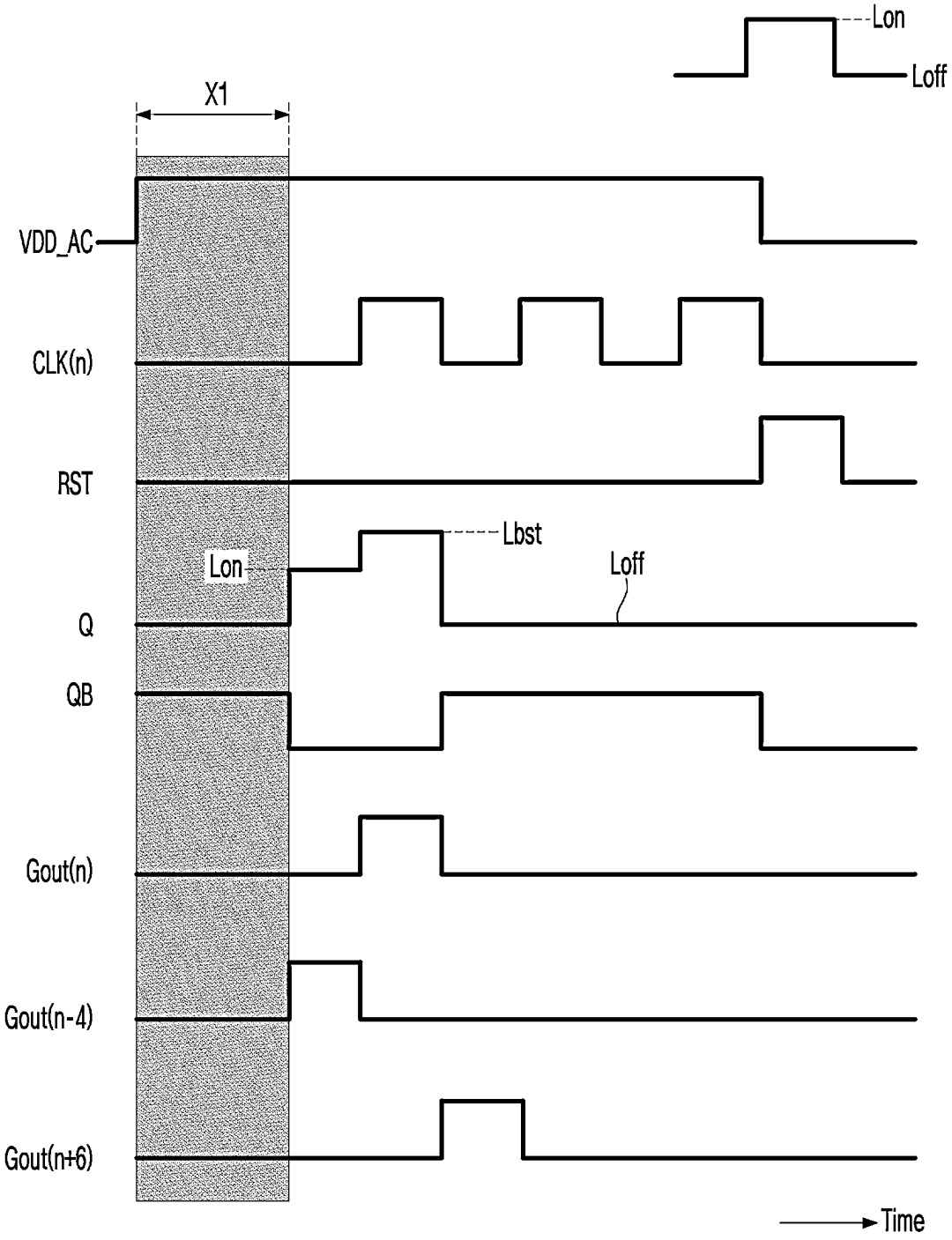

Lon
Loff
X1
VDD_AC
CLK(n)
RST
Lbst
Lon
Loff
Q
QB
Gout(n)
Gout(n-4)
Gout(n+6)
Time

FIG. 7

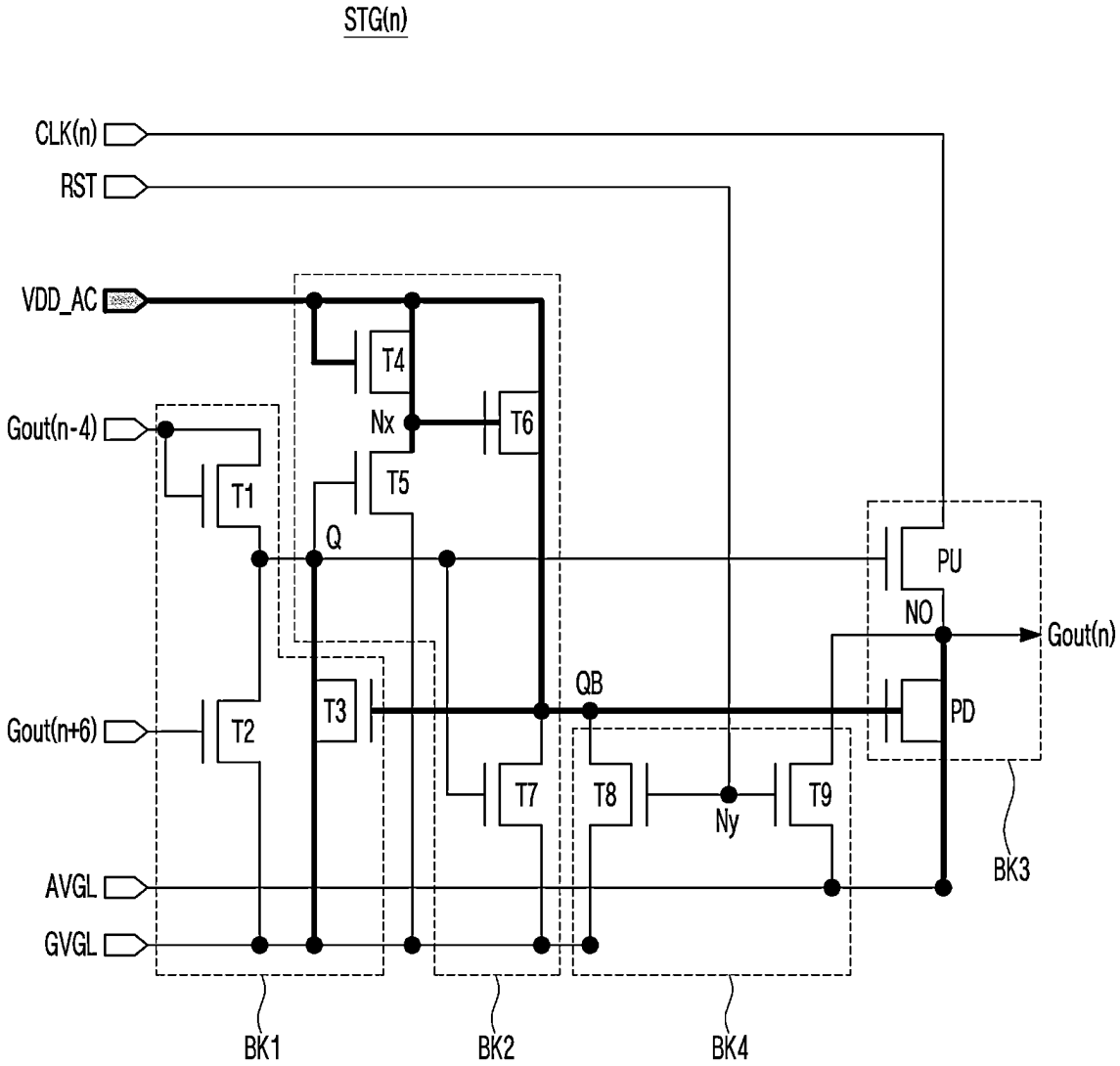

STG(n)
CLK(n)
RST
VDD_AC
Gout(n-4)
Gout(n+6)
AVGL
GVGL
T1
T2
T3
T4
T5
T6
T7
T8
T9
Nx
Ny
Q
QB
PU
PD
NO
Gout(n)
BK1
BK2
BK3
BK4

FIG. 8

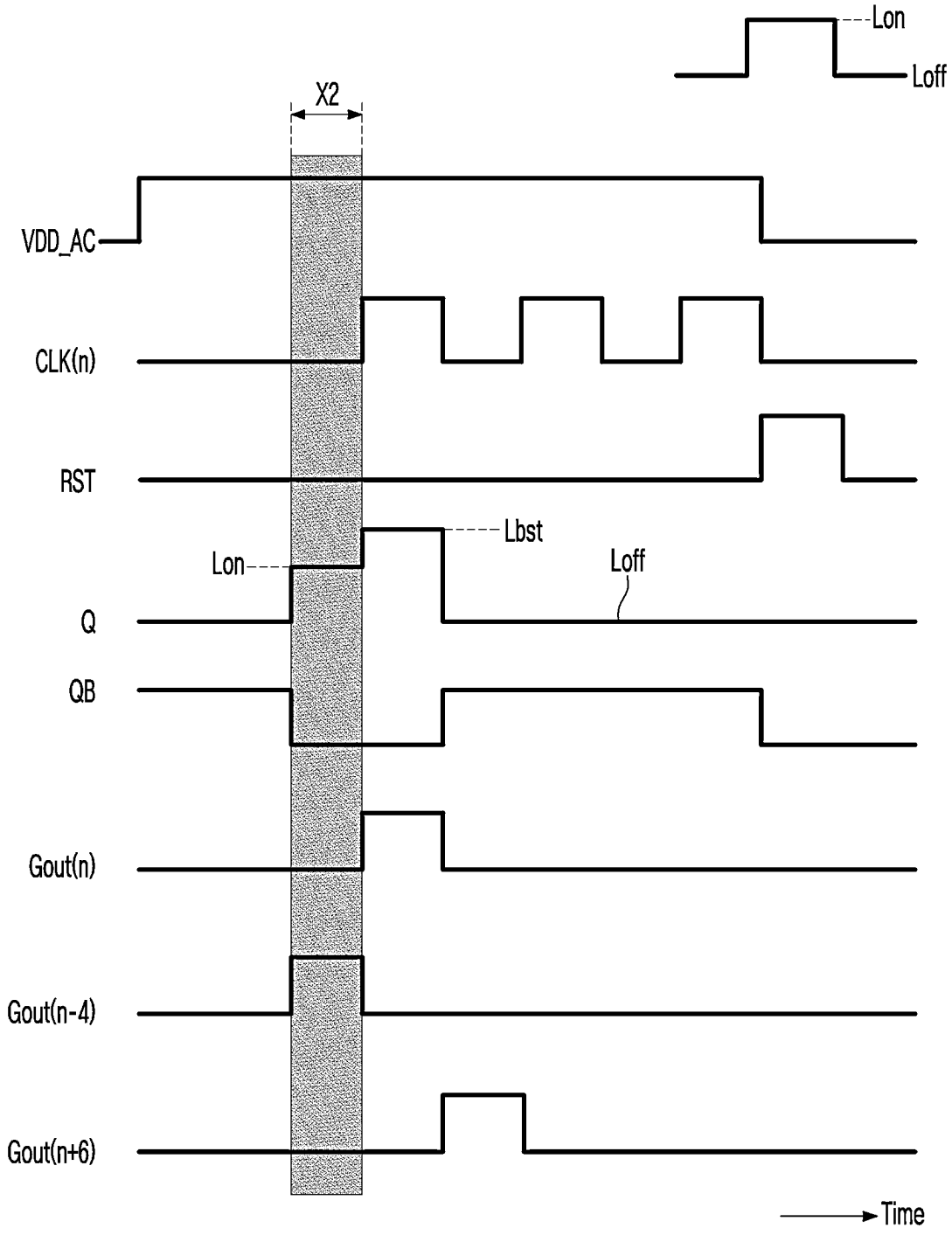

Lon
Loff
X2
VDD_AC
CLK(n)
RST
Lbst
Lon
Loff
Q
QB
Gout(n)
Gout(n-4)
Gout(n+6)
Time

FIG. 9

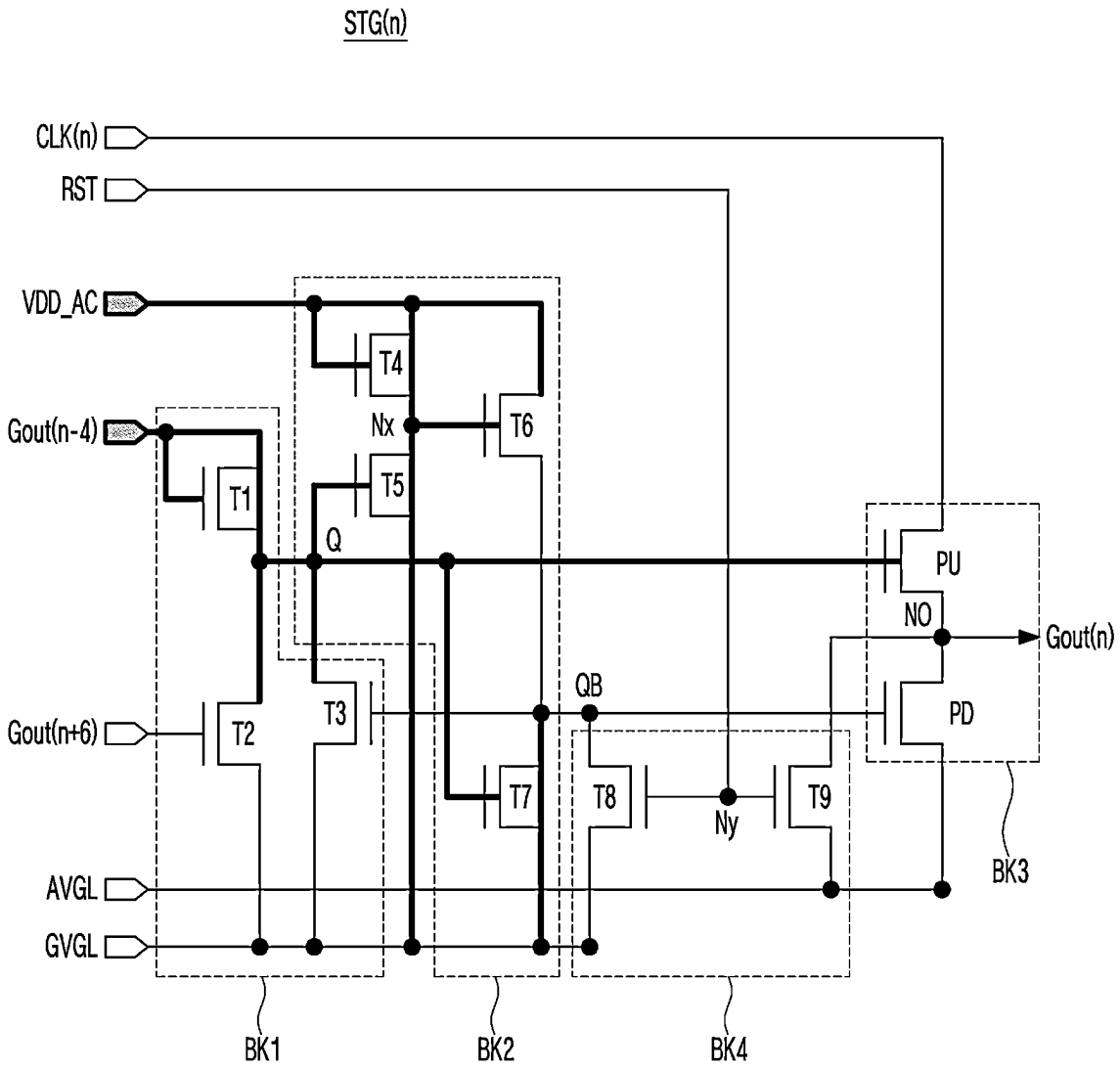

STG(n)
CLK(n)
RST
VDD_AC
Gout(n-4)
Gout(n+6)
AVGL
GVGL
T1
T2
T3
T4
T5
T6
T7
T8
T9
Nx
Ny
Q
QB
PU
PD
NO
Gout(n)
BK1
BK2
BK3
BK4

FIG. 10

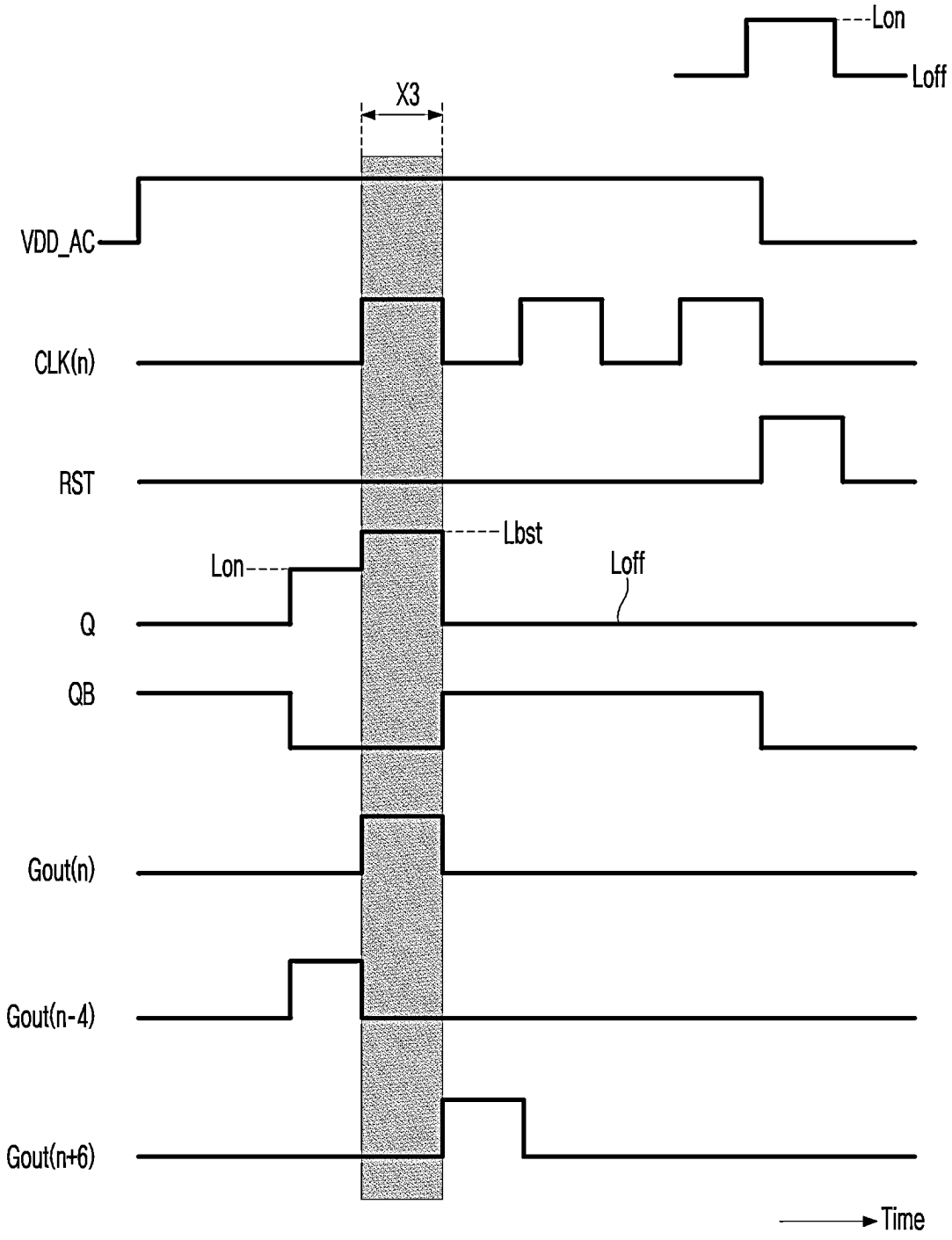

Lon
Loff
X3
VDD_AC
CLK(n)
RST
Lbst
Lon
Loff
Q
QB
Gout(n)
Gout(n-4)
Gout(n+6)
Time

FIG. 11

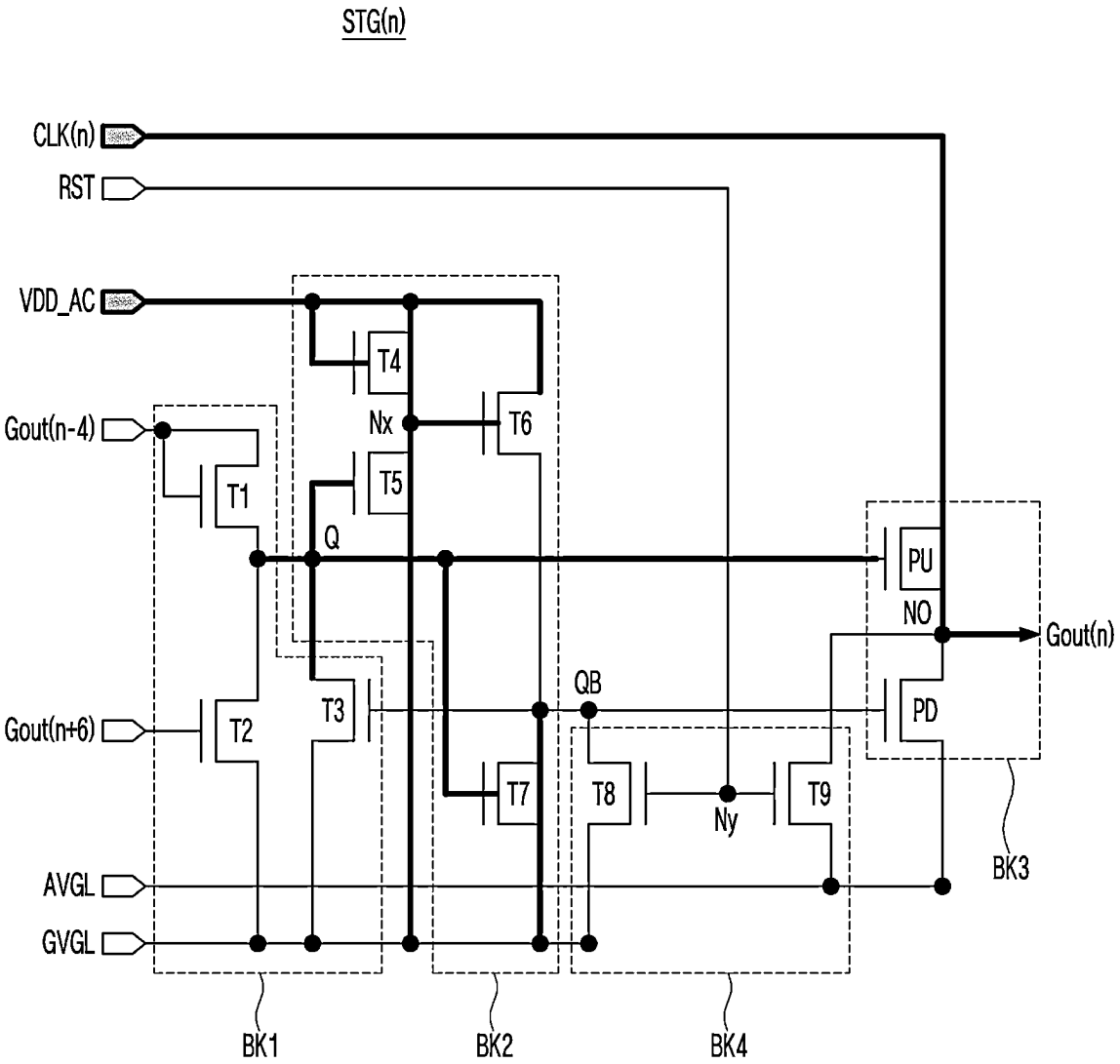

STG(n)
CLK(n)
RST
VDD_AC
Gout(n-4)
Gout(n+6)
AVGL
GVGL
T1
T2
T3
T4
T5
T6
T7
T8
T9
PU
PD
Nx
Ny
Q
QB
NO
Gout(n)
BK1
BK2
BK3
BK4

FIG. 12

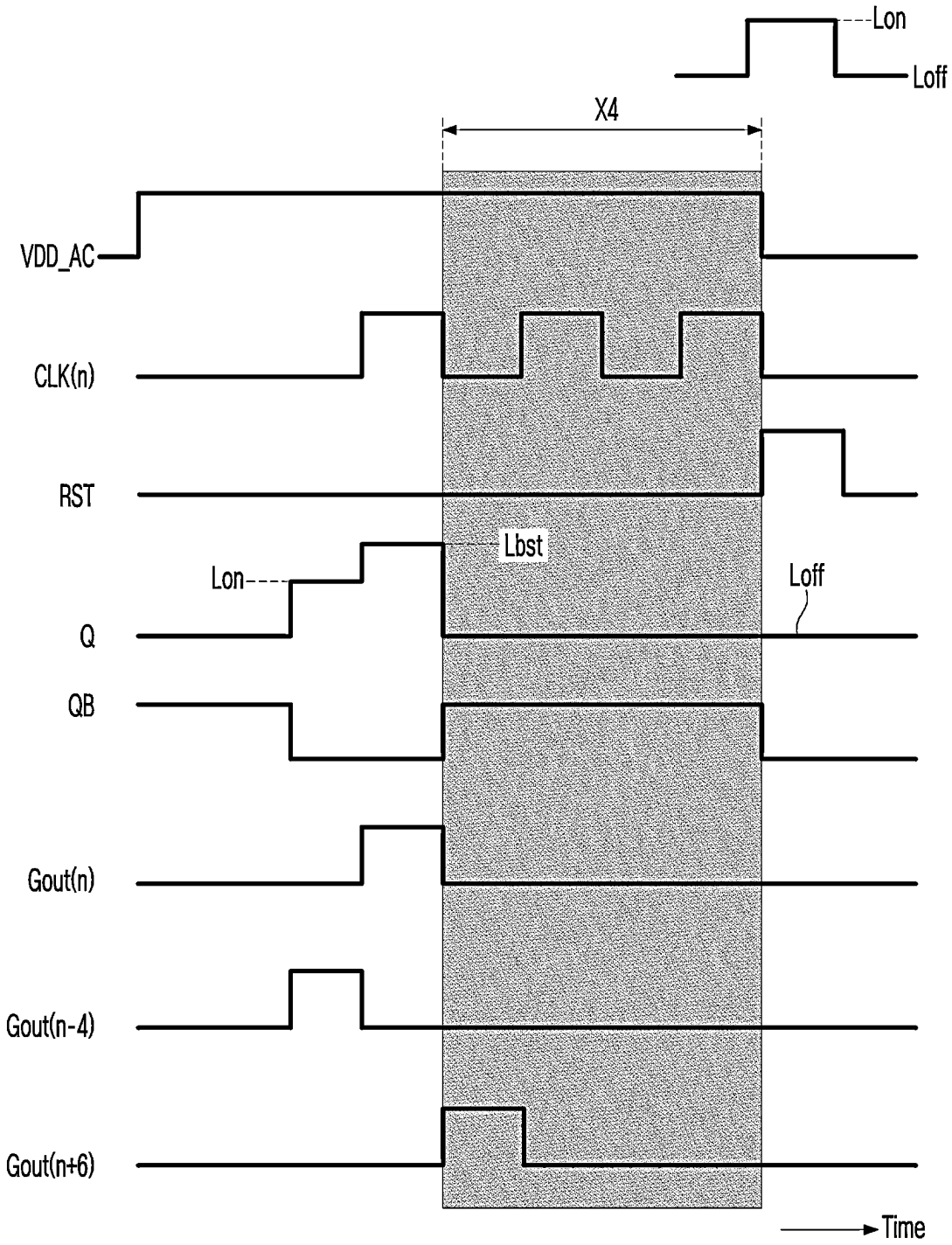

Lon
Loff
X4
VDD_AC
CLK(n)
RST
Lbst
Lon
Loff
Q
QB
Gout(n)
Gout(n-4)
Gout(n+6)
Time

FIG. 13

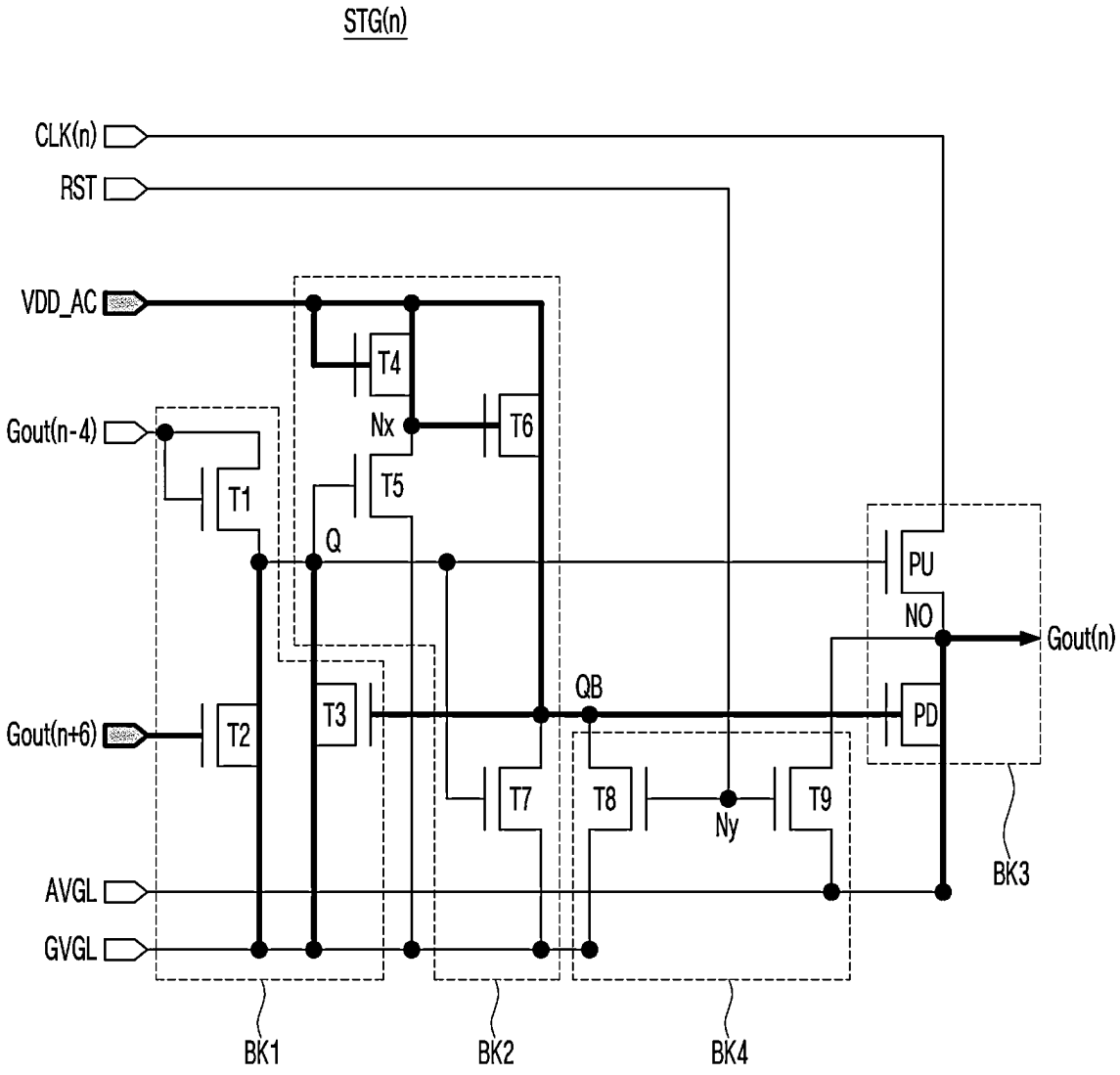

STG(n)
CLK(n)
RST
VDD_AC
Gout(n-4)
Gout(n+6)
AVGL
GVGL
T1
T2
T3
T4
T5
T6
T7
T8
T9
Nx
Ny
Q
QB
PU
PD
NO
Gout(n)
BK1
BK2
BK3
BK4

FIG. 14

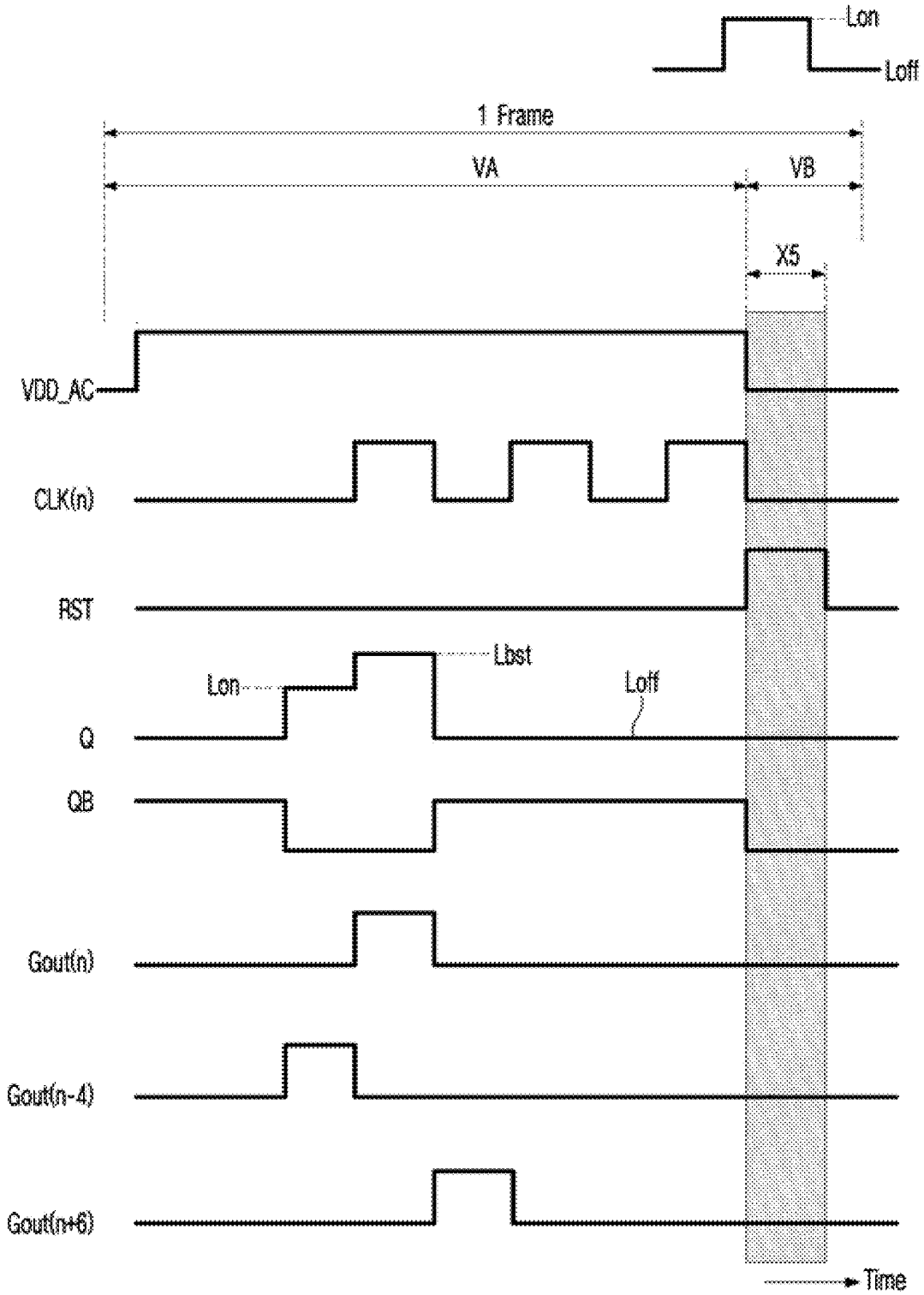
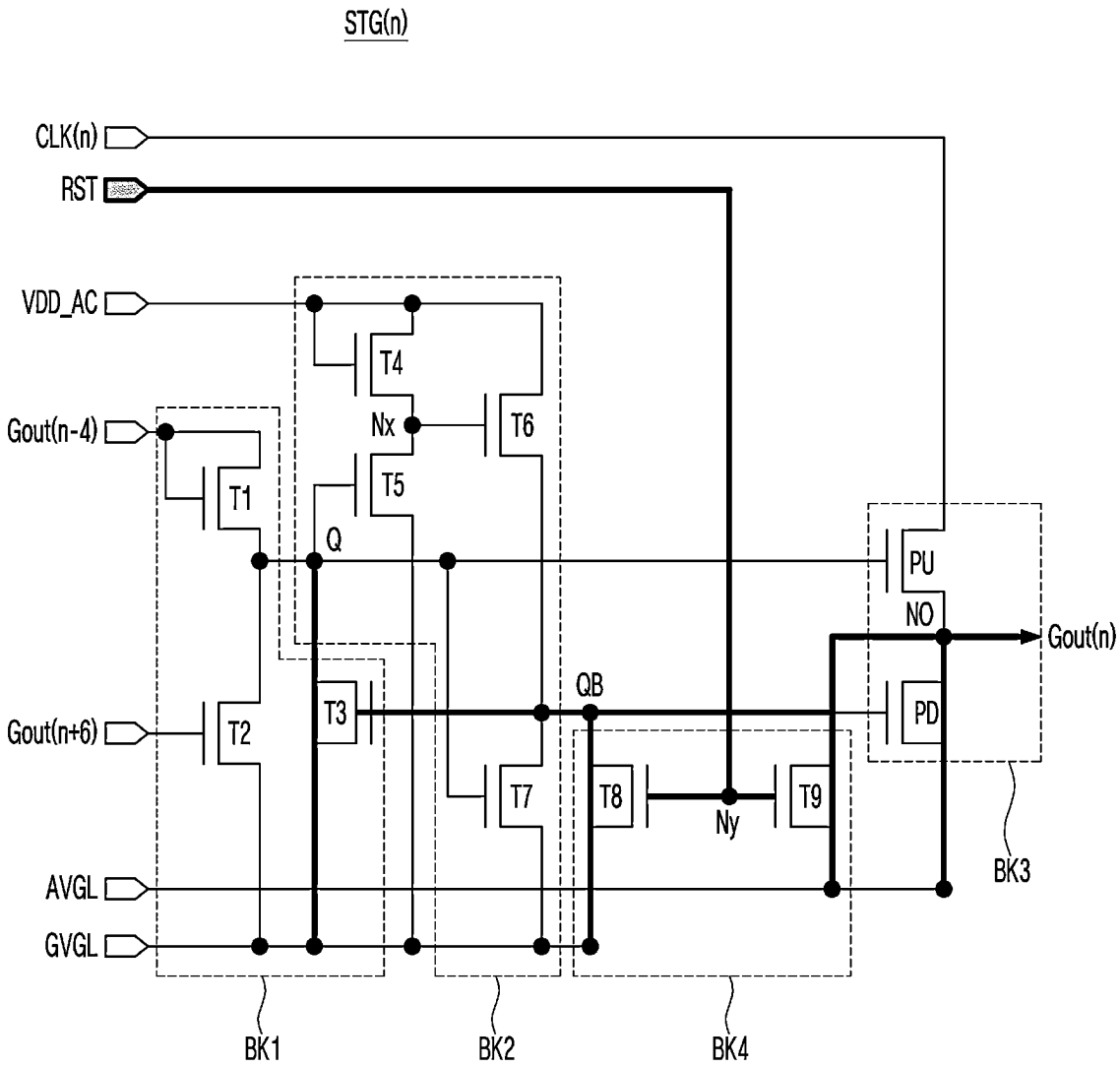

Lon
Loff
1 Frame
VA
VB
X5
VDD_AC
CLK(n)
RST
Lbst
Lon
Loff
Q
QB
Gout(n)
Gout(n-4)
Gout(n+6)
Time

FIG. 15


STG(n)
CLK(n)
RST
VDD_AC
Gout(n-4)
Gout(n+6)
AVGL
GVGL
T1
T2
T3
T4
T5
T6
T7
T8
T9
Nx
Ny
Q
QB
PU
PD
NO
Gout(n)
BK1
BK2
BK3
BK4

GATE DRIVER AND DISPLAY APPARATUS INCLUDING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to Korean Patent Application No. 10-2024-0020502, filed in the Republic of Korea on Feb. 13, 2024, the entirety of which is hereby expressly incorporated by reference into the present application.

BACKGROUND

Technical Field

[0002] The present disclosure relates to a gate driver and a display apparatus including the same.

Discussion of the Related Art

[0003] Display apparatuses include a plurality of pixels arranged as a matrix type and supply pixels with image data synchronized with a scan signal and thus, adjust the luminance of the pixels. The display apparatuses generate the scan signal by using a gate driver including a plurality of gate stages. Each of the gate stages of the gate driver is connected to a gate line of the display panel. Each gate stage includes a plurality of transistors and outputs the scan signal, swinging between a scan on voltage and a scan off voltage, to the gate line of the display panel.

[0004] Since the number of gate lines increases as a resolution increases in a display screen having a certain size, the number of gate stages can increase in a high-resolution display apparatus. When the number of gate stages increases, however, an area of a bezel area including the gate stages can inevitably increase. As such, there can be a limitation in reducing a bezel in the display apparatuses.

SUMMARY OF THE DISCLOSURE

[0005] To overcome the aforementioned problem and other limitations of the related art, the present disclosure can provide a gate driver and a display apparatus including the same, in which configurations of gate stages can be simplified and thus, a narrow bezel can be implemented.

[0006] To achieve these objects and other advantages and in accordance with the purpose of the disclosure, as embodied and broadly described herein, a gate driver includes a plurality of stages. An n^{th} stage of the plurality of stages includes a pull-up transistor configured to control a flow of a current between an output node and an input terminal for an n^{th} clock, based on a voltage of a Q node, a pull-down transistor configured to control a flow of a current between the output node and an input terminal of a first low power source, based on a voltage of a QB node, and a QB node controller configured to control the voltage of the QB node, based on a voltage of a control power source and the voltage of the Q node, wherein the voltage of the control power source has an on level in a vertical active period of one frame and has an off level in a vertical blank period of the one frame, where n is an integer. For example, n can be an integer greater than 4.

[0007] In another aspect of the present disclosure, a display apparatus is provided which comprises a display panel including a plurality of gate lines; and a gate driver including a plurality of stages connected to the plurality of gate lines, wherein an n^{th} stage of the plurality of stages comprises: a pull-up transistor configured to control a flow of a current between an output node and an input terminal for an n^{th} clock, based on a voltage of a Q node; a pull-down transistor configured to control a flow of a current between the output node and an input terminal of a first low power source, based on a voltage of a QB node; and a QB node controller configured to control the voltage of the QB node, based on a voltage of a control power source and the voltage of the Q node, wherein the voltage of the control power source has an on level in a vertical active period of one frame and has an off level in a vertical blank period of the one frame, where n is an integer. For example, n can be an integer greater than 4.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The accompanying drawings, which are included to provide a further understanding of the disclosure and are incorporated in and constitute a part of this application, illustrate embodiment(s) of the disclosure and together with the description serve to explain the principle of the disclosure. In the drawings:

[0009] FIG. **1** is a diagram illustrating a display apparatus according to one or more embodiments of the present disclosure;

[0010] FIG. **2** is a diagram schematically illustrating an equivalent circuit of a pixel provided in a display panel of FIG. **1**;

[0011] FIG. **3** is a diagram illustrating gate stages connected to gate lines according to an example of the present disclosure;

[0012] FIG. **4** is a diagram illustrating an n^{th} gate stage connected to an n^{th} gate line according to aspects of the present disclosure;

[0013] FIG. **5** is a diagram illustrating driving signals for driving the n^{th} gate stage according to aspects of the present disclosure;

[0014] FIGS. **6** and **7** are diagrams illustrating an operation of the n^{th} gate stage during a first period according to aspects of the present disclosure;

[0015] FIGS. **8** and **9** are diagrams illustrating an operation of the n^{th} gate stage during a second period according to aspects of the present disclosure;

[0016] FIGS. **10** and **11** are diagrams illustrating an operation of the n^{th} gate stage during a third period according to aspects of the present disclosure;

[0017] FIGS. **12** and **13** are diagrams illustrating an operation of the n^{th} gate stage during a fourth period according to aspects of the present disclosure; and

[0018] FIGS. **14** and **15** are diagrams illustrating an operation of the n^{th} gate stage during a fifth period according to aspects of the present disclosure.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0019] Hereinafter, the present disclosure will be described more fully with reference to the accompanying drawings, in which exemplary embodiments of the disclosure are shown. The disclosure may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be

thorough and complete, and will fully convey the concept of the disclosure to those skilled in the art.

[0020] Advantages and features of the present disclosure, and implementation methods thereof will be clarified through following embodiments described with reference to the accompanying drawings. The present disclosure may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the present disclosure to those skilled in the art.

[0021] The shapes, sizes, ratios, angles, numbers and the like disclosed in the drawings for description of various embodiments of the present disclosure to describe embodiments of the present disclosure are merely exemplary and the present disclosure is not limited thereto. Like reference numerals refer to like elements throughout. Throughout this specification, the same elements are denoted by the same reference numerals. As used herein, the terms "comprise", "having," "including" and the like suggest that other parts can be added unless the term "only" is used. As used herein, the singular forms "a", "an", and "the" are intended to include the plural forms as well, unless context clearly indicates otherwise.

[0022] Elements in various embodiments of the present disclosure are to be interpreted as including margins of error even without explicit statements. Further, the term "can" fully encompasses all the meanings and coverages of the term "may."

[0023] In describing a position relationship, for example, when a position relation between two parts is described as "on", "over", "under", and "next", one or more other parts can be disposed between the two parts unless "just" or "direct" is used.

[0024] It will be understood that, although the terms "first", "second", etc. can be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another and may not define order or sequence. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present disclosure.

[0025] In the present disclosure, a pixel circuit and a gate driver provided on a substrate of a display panel can be implemented with a transistor having an N metal oxide semiconductor field effect transistor (MOSFET) type, but are not limited thereto. A transistor can be a three-electrode element which includes a gate, a source, and a drain. The source can be an electrode which supplies a carrier to a transistor. In the transistor, a carrier can start to flow from the source. The drain can be an electrode which enables the carrier to flow out from the transistor. That is, in a MOSFET, the carrier flows from the source to the drain. In N MOS, because a carrier is a hole, a source voltage can be higher than a drain voltage so that the hole flows from the source to the drain. In N MOS, because the hole flows from the drain to the source, a current can flow from the drain to the source. It should be noted that a source and a drain of a MOSFET are not fixed. For example, the source and the drain of the MOSFET can switch therebetween. Therefore, in describing an embodiment of the present disclosure, one of a source and a drain can be described as a first electrode, and the other of the source and the drain can be described as a second electrode.

[0026] Hereinafter, embodiments of the present disclosure will be described in detail with reference to the accompanying drawings. All the components of each device/apparatus according to all embodiments of the present disclosure are operatively coupled and configured. In the following description, in an electroluminescent display apparatus, an organic light emitting display apparatus including an organic light emitting material will be mainly described. However, it should be noted that the inventive concept is not limited to the organic light emitting display apparatus and can be applied to an inorganic light emitting display apparatus including an inorganic light emitting material.

[0027] FIG. **1** is a diagram illustrating a display apparatus according to one or more embodiments of the present disclosure. FIG. **2** is a diagram schematically illustrating an equivalent circuit of a pixel provided in a display panel of FIG. **1**. FIG. **3** is a diagram illustrating gate stages connected to gate lines according to an example of the present disclosure.

[0028] Referring to FIG. **1**, the display apparatus according to the present embodiment can include a display panel **100**, a timing controller **110**, a data driver **120**, a gate driver **130**, and a level shifter **150**. The display apparatus according to the present embodiment can be implemented as an electroluminescence display apparatus, but is not limited thereto.

[0029] In the display panel **100**, as in FIG. **2**, pixels PXL connected to a data line **14** and a gate line **15** can be arranged as a matrix type to configure a pixel array. A plurality of horizontal pixel lines can be included in the pixel array, and a plurality of pixels PXL which are horizontally adjacent to one another and are connected to the gate line **15** in common can be arranged in each horizontal pixel line. Here, a horizontal pixel line can denote a set of pixels of one horizontal line implemented by pixels PXL horizontally adjacent to one another, instead of a physical signal line. The pixel array can include a power line which transfers a high-level pixel source voltage EVDD to the pixels PXL. Also, the pixels PXL can be further connected to a low-level pixel source voltage EVSS.

[0030] Each of the pixels PXL, as shown in FIG. **2**, can include a light emitting device OLED and a pixel driving circuit PCC for driving the light emitting device OLED. The pixel driving circuit PCC can include a driving element which generates a driving current which is to be applied to the light emitting device OLED and a switch circuit connected to the driving element. The switch circuit can set and maintain a gate-source voltage of the driving element. To this end, the switch circuit can be supplied with a data voltage Vdata through the data line **14**, supplied with a gate signal Gout through the gate line **15**, and supplied with the high-level pixel source voltage EVDD through a power line, thereby setting the gate-source voltage of the driving element. A gate electrode of a switch element included in the switch circuit can be connected to the gate line **15**, and a first electrode (or a second electrode) of the switch element included in the switch circuit can be connected to a data line.

[0031] Each of the pixels PXL can be one of a red pixel, a green pixel, a blue pixel, and a white pixel. The red pixel, the green pixel, the blue pixel, and the white pixel can configure one unit pixel and can implement various colors.

A color implemented in a unit pixel can be determined based on an emission rate of each of the red pixel, the green pixel, the blue pixel, and the white pixel. Furthermore, the white pixel can be omitted, and in this case, the unit pixel can be configured with the red pixel, the green pixel, and the blue pixel. Also, the number of gate lines **15** connected to the pixel PXL can be singular or plural.

[0032] Referring to FIG. **1**, the data driver **120** can receive image data DATA and a source timing control signal DDC from the timing controller **110**. In response to the source timing control signal DDC from the timing controller **110**, the data driver **120** can convert the image data DATA into a gamma compensation voltage to generate a data voltage Vdata and can supply the data voltage Vdata to the data lines **14** of the display panel **100**, based on a supply timing of the gate signal Gout. The data driver **120** can be connected to the data lines **14** of the display panel **100** through a chip on glass (COG) process or a tape automated bonding (TAB) process. The data driver **120** can be divisionally disposed in plurality, but is not limited thereto and can be provided as one data driver.

[0033] Referring to FIG. **1**, the level shifter **150** can generate a gate timing control signal GDC for driving a switch element of a pixel, based on an on/off control clock which has a transistor-transistor-logic (TTL) level and is input from the timing controller **110**. The gate timing control signal GDC can include a start signal and a clock signal, which swing between an on level and an off level. The level shifter **150** can supply the gate timing control signal GDC to the gate driver **130**.

[0034] Referring to FIGS. **1** to **3**, the gate driver **130** can operate based on the gate timing control signal GDC input from the level shifter **150** to generate the gate signal Gout needed for driving of the pixel PXL. Also, the gate driver **130** can supply the gate signal Gout to the gate lines **15**.

[0035] The gate driver **130** can be directly provided on a lower substrate of the display panel **100** by using a gate driver in panel (GIP) type. The gate driver **130** can be provided in a non-display area (i.e., a bezel area BZ) outside a screen in the display panel **100**. The non-display area or the bezel area BZ can be disposed adjacent to a display area or active area AA. The bezel area BZ can surround the display area AA entirely or only in part(s). In the GIP type, the level shifter **150** can be mounted on a printed circuit board (PCB) **140** along with the timing controller **110**.

[0036] The gate driver **130** can include a plurality of gate stages STG which are connected to one another, based on a cascading scheme. Each of the plurality of gate stages STG can be connected to a corresponding gate line **15** and can output the gate signal Gout to the corresponding gate line **15**.

[0037] Some gate stages of the plurality of gate stages STG can start to operate based on a start signal (VST of FIG. **5**). Also, each of the other gate stages except the some gate stages can start to operate based on an output (i.e., a previous carry signal) of a previous gate stage which has operated prior thereto.

[0038] The gate driver **130** can be disposed in both bezel areas BZ facing the display panel **100** and can supply the scan signal to each gate line, based on a double feeding scheme, thereby minimizing signal distortion caused by a load deviation of each gate line.

[0039] Referring to FIG. **1**, the timing controller **110** can be connected to an external host system by various interface types known to those skilled in the art. The timing controller **110** can receive video data DATA from the host system, correct the video data DATA to compensate for a luminance deviation caused by an electrical characteristic difference, and transfer the corrected video data to the data driver **120**.

[0040] The timing controller **110** can receive a timing signal such as a vertical synchronization signal Vsync, a horizontal synchronization signal Hsync, a data enable signal DE, and a main clock MCLK from the host system and can generate an on/off control clock based on the source timing control signal DDC and the gate timing control signal GDC, based on the timing signal.

[0041] FIG. **4** is a diagram illustrating an n^{th} gate stage STG(n) connected to an n^{th} gate line according to aspects of the present disclosure, and FIG. **5** is a diagram illustrating driving signals for driving the n^{th} gate stage STG(n) according to aspects of the present disclosure.

[0042] Referring to FIGS. **4** and **5**, in the n^{th} gate stage STG(n), a voltage of a control power source VDD applied to a second block BK**2** can use an alternating current (AC) voltage instead of a direct current (DC) voltage, so as to reduce the number of transistors included in the second block BK**2**, where n is an integer.

[0043] In a related art, additional transistors which are driven based on a VDD_DC voltage and an AC control signal to precharge a QB node are needed for controlling the QB node.

[0044] In contrast, an AC-type control power source VDD according to the present embodiment can replace the VDD_DC voltage and the AC control signal. According to the present embodiment, the additional transistors of the related art used to precharge the QB node can be omitted. In the present embodiment, the AC-type control power source VDD having an on level can be applied to the QB node through transistors T**4** and T**6**.

[0045] A voltage of the AC-type control power source VDD (VDD_AC) according to the present embodiment can be input at an on level Lon in a vertical active period VA of one frame and can be input at an off level Loff in a vertical blank period VB of the one frame.

[0046] A configuration of the n^{th} gate stage STG(n) according to an example of the present disclosure will be described below in detail.

[0047] The n^{th} gate stage STG(n) can include a first block BK**1**, the second block BK**2**, a third block BK**3**, and a fourth block BK**4**.

[0048] The first block BK**1** can be a Q node controller for controlling a voltage of a Q node. The Q node controller can be configured to control the voltage of the Q node, based on a carry signal and the voltage of the QB node. The first block BK**1** can include a transistor T**1** which is connected to the Q node and an input terminal for a previous carry signal Gout(n−4) input from an $(n-4)^{th}$ stage, a transistor T**2** which connects the Q node to an input terminal of a second low power source GVGL according to a next carry signal Gout (n+6) input from an $(n+6)^{th}$ stage, and a transistor T**3** which connects the Q node to the input terminal of the second low power source GVGL according to a next carry signal Gout (n+6) input from an $(n+6)^{th}$ stage. The previous carry signal can be for charging the Q node with an on voltage, and the next carry signal can be for discharging the Q node to an off voltage. In the present embodiment, an output of the $(n-4)^{th}$ stage can be provided as the previous carry signal, and an output of the $(n+6)^{th}$ stage can be provided as the next carry signal, but the inventive concept is not limited thereto.

However, when the output of the $(n+6)^{th}$ stage instead of the output of the $(n-4)^{th}$ stage is applied as the next carry signal, a Q node charge maintenance time can increase, and thus, the stability of an operation can be secured.

[0049] A gate electrode and a drain electrode of the transistor T**1** can be connected to the input terminal for the previous carry signal Gout(n−4), and a source electrode of the transistor T**1** can be connected to the Q node. A gate electrode of the transistor T**2** can be connected to an input terminal for the next carry signal Gout(n+6), a drain electrode of the transistor T**2** can be connected to the Q node, and a source electrode of the transistor T**2** can be connected to the input terminal of the second low power source GVGL. A gate electrode of the transistor T**3** can be connected to the QB node, a drain electrode of the transistor T**3** can be connected to the Q node, and a source electrode of the transistor T**3** can be connected to the input terminal of the second low power source GVGL.

[0050] The second block BK**2** can be a QB node controller for controlling the voltage of the QB node. The second block BK**2** can include a transistor T**4** which is connected to a first control node Nx and the input terminal of the control power source VDD, a transistor T**5** which connects the first control node Nx to the input terminal of the second low power source GVGL with the voltage of the Q node, a transistor T**6** which applies the voltage of the control power source VDD to the QB node with a voltage of the first control node Nx, and a transistor T**7** which connects the QB node to the input terminal of the second low power source GVGL with the voltage of the Q node.

[0051] A gate electrode and a drain electrode of the transistor T**4** can be connected to the input terminal of the control power source VDD, and a source electrode of the transistor T**4** can be connected to the first control node Nx. A gate electrode of the transistor T**5** can be connected to the Q node, a drain electrode of the transistor T**5** can be connected to the first control node Nx, and a source electrode of the transistor T**5** can be connected to the input terminal of the second low power source GVGL. A gate electrode of the transistor T**6** can be connected to the first control node Nx, a drain electrode of the transistor T**6** can be connected to the input terminal of the control power source VDD, and a source electrode of the transistor T**6** can be connected to the QB node. A gate electrode of the transistor T**7** can be connected to the Q node, a drain electrode of the transistor T**7** can be connected to the QB node, and a source electrode of the transistor T**7** can be connected to the input terminal of the second low power source GVGL.

[0052] The third block BK**3** can be an output unit for outputting the gate signal Gout(n). The third block BK**3** can include a pull-up transistor PU which controls a flow of a current between an input terminal for an n^{th} clock CLK(n) and an output node NO, based on the voltage of the Q node, and a pull-down transistor PD which controls a flow of a current between an input terminal of a first low power source AVGL and the output node NO, based on the voltage of the QB node.

[0053] A gate electrode of the pull-up transistor PU can be connected to the Q node, a drain electrode of the pull-up transistor PU can be connected to the input terminal for the n^{th} clock CLK(n), and a source electrode of the pull-up transistor PU can be connected to the output node NO. A gate electrode of the pull-down transistor PD can be connected to the QB node, a drain electrode of the pull-down transistor PD can be connected to the output node NO, and a source electrode of the pull-down transistor PD can be connected to the input terminal of the first low power source AVGL.

[0054] The fourth block BK**4** can be a reset unit which resets a voltage of the output node NO to a voltage of the first low power source AVGL and resets the voltage of the QB node to the voltage of the second low power source GVGL, during the vertical blank period VB.

[0055] The fourth block BK**4** can include a transistor T**8** which connects the QB node to the input terminal of the second low power source GVGL, based on a reset signal RST, and a transistor T**9** which connects the output node NO to the input terminal of the first low power source AVGL, based on the reset signal RST.

[0056] A gate electrode of the transistor T**8** can be connected to a second control node Ny, a drain electrode of the transistor T**8** can be connected to the QB node, and a source electrode of the transistor T**8** can be connected to the input terminal of the second low power source GVGL. A gate electrode of the transistor T**9** can be connected to the second control node Ny, a drain electrode of the transistor T**9** can be connected to the output node NO, and a source electrode of the transistor T**9** can be connected to the input terminal of the first low power source AVGL.

[0057] A time for which the QB node is maintained at an on voltage level is longer than that for which the Q node is maintained at an on voltage level, and due to this, the pull-down transistor PD can be easily degraded. The fourth block BK**4** can reset the voltage of the QB node to the voltage of the second low power source GVGL in the vertical blank period VB, based on the reset signal RST, thereby decreasing a degradation in the pull-down transistor PD.

[0058] To this end, the reset signal RST can be input at an on level Lon for a partial time of the vertical blank period VB and can be input at an off level Loff in the vertical active period VA and the other time of the vertical blank period VB.

[0059] When the pull-down transistor PD is degraded, an off current can flow through the pull-down transistor PD having an off state. Such an off current can distort a waveform of the gate signal Gout(n). To prevent an off current of the pull-down transistor PD, the voltage of the first low power source AVGL can be set to be greater than the voltage of the second low power source GVGL. In a state where the pull-down transistor PD is turned off, the second low power source GVGL can be connected to the gate electrode of the pull-down transistor PD, and the first low power source AVGL can be connected to the source electrode of the pull-down transistor PD. At this time, when the voltage of the first low power source AVGL is greater than the voltage of the second low power source GVGL, an off current may not flow in the pull-down transistor PD, based on a reverse bias applied between the gate electrode and the source electrode of the pull-down transistor PD.

[0060] An operation of the n^{th} gate stage STG(n) can be divided into first to fifth periods (X**1** to X**5** of FIGS. **6** to **15**). Here, the first to fourth periods (X**1** to X**4** of FIGS. **6** to **15**) can correspond to the vertical active period VA, and the fifth period (X**5** of FIGS. **6** to **15**) can correspond to the vertical blank period VB.

[0061] FIGS. **6** and **7** are diagrams illustrating an operation of the n^{th} gate stage STG(n) during a first period X**1** according to aspects of the present disclosure.

[0062] Referring to FIGS. **6** and **7**, during the first period X**1**, the voltage of the control power source VDD can be input at the on level Lon, and thus, the transistor T**4** and the transistor T**6** can be turned on. Based on the voltage of the control power source VDD having the on level Lon, the voltage of the QB node can have the on level Lon. Based on the voltage of the QB node having the on level Lon, the transistor T**3** and the pull-down transistor PD can be turned on. Based on the second low power source GVGL connected through the transistor T**3**, the voltage of the Q node can have the off level Loff. Based on the first low power source AVGL connected through the pull-down transistor PD, the voltage of the output node NO can have the off level Loff.

[0063] FIGS. **8** and **9** are diagrams illustrating an operation of the n^{th} gate stage STG(n) during a second period X**2** according to aspects of the present disclosure.

[0064] Referring to FIGS. **8** and **9**, during the second period X**2**, the transistor T**1** can be turned on by the previous carry signal Gout(n−4) having the on level Lon, and the Q node can be charged at the on level Lon. Based on the voltage of the Q node having the on level Lon, the transistor T**5**, the transistor T**7**, and the pull-up transistor PU can be turned on. As the transistor T**5** is turned on, the second low power source GVGL can be connected to the first control node Nx, and thus, the transistor T**6** can be turned off. Even when the voltage of the control power source VDD having the on level Lon is applied to the first control node Nx through the transistor T**4** during the second period X**2**, the voltage of the control power source VDD having the on level Lon can be discharged to the voltage of the second low power source GVGL through the transistor T**5**. As the transistor T**7** is turned on, the voltage of the QB node can have the off level Loff. As the pull-up transistor PU is turned on, the clock signal CLK(n) having the off level Loff can be output to the output node NO.

[0065] FIGS. **10** and **11** are diagrams illustrating an operation of the n^{th} gate stage STG(n) during a third period X**3** according to aspects of the present disclosure.

[0066] Referring to FIGS. **10** and **11**, when the clock signal CLK(n) having the on level Lon is input during the third period X**3**, the voltage of the Q node can be up-shifted from the on level Lon to a bootstrapping level Lbst, based on coupling of a parasitic capacitor connected between the gate electrode and the drain electrode of the pull-up transistor PU. The bootstrapping level Lbst can be a voltage which is higher than the on level Lon. When the voltage of the Q node is up-shifted to the bootstrapping level Lbst, an on-response characteristic of the pull-up transistor PU can be quickened. When the voltage of the Q node is up-shifted to the bootstrapping level Lbst, a gate-source voltage of the pull-up transistor PU can increase, and thus, the amount of current flowing in the pull-up transistor PU can increase. At this time, the clock signal CLK(n) having the on level Lon can be output to the output node NO, based on the turn-on of the pull-up transistor PU, and thus, can be the gate signal Gout(n) having the on level Lon.

[0067] FIGS. **12** and **13** are diagrams illustrating an operation of the n^{th} gate stage STG(n) during a fourth period X**4** according to aspects of the present disclosure.

[0068] Referring to FIGS. **12** and **13**, during the fourth period X**4**, the transistor T**2** can be turned on by the next carry signal Gout(n+6) having the on level Lon, and the Q node can be discharged to the off level Loff. Based on the voltage of the Q node having the off level Loff, the transistor T**5**, the transistor T**7**, and the pull-up transistor PU can be turned off. As the transistor T**5** is turned off, the transistor T**6** can be turned on, and thus, the voltage of the QB node can have the on level Lon. Based on the voltage of the QB node having the on level Lon, the transistor T**3** and the pull-down transistor PD can be turned on. Based on the second low power source GVGL connected through the transistor T**3**, the voltage of the Q node can maintain the off level Loff while the transistor T**3** is being turned on. Based on the first low power source AVGL connected through the pull-down transistor PD, the voltage of the output node NO can have the off level Loff.

[0069] FIGS. **14** and **15** are diagrams illustrating an operation of the n^{th} gate stage STG(n) during a fifth period X**5** according to aspects of the present disclosure.

[0070] Referring to FIGS. **14** and **15**, during the fifth period X**5**, the voltage of the control power source VDD can be input at the off level Loff, and the reset signal RST can be input at the on level Lon. The transistor T**8** and the transistor T**9** can be turned on by the reset signal RST having the on level Lon. As a result, the voltage of the QB node can be reset to the voltage of the second low power source GVGL, and the output node NO can be reset to the first low power source AVGL, thereby preventing an operation (i.e., the waveform distortion of the gate signal Gout(n)) of an abnormal operation caused by coupling of an external source voltage during the vertical blank period VB. When the voltage of the QB node is reset to the voltage of the second low power source GVGL at every vertical blank period VB, a degradation in the transistors T**3** and PD including the gate electrodes connected to the QB node can be reduced.

[0071] In the gate driver and the display apparatus including the same according to the embodiments of the present disclosure, configurations of gate stages can be simplified, and thus, a narrow bezel can be implemented

[0072] The effects according to the present disclosure are not limited to the above examples, and other various effects can be included in the specification.

[0073] While the present disclosure has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details can be made therein without departing from the spirit and scope of the present disclosure as defined by the following claims.

What is claimed is:

1. A gate driver comprising:

a plurality of stages including an n^{th} stage, where n is an integer,

wherein the n^{th} stage comprises:

a pull-up transistor configured to control a flow of a current between an output node and an input terminal for an n^{th} clock, based on a voltage of a Q node;

a pull-down transistor configured to control a flow of a current between the output node and an input terminal of a first low power source, based on a voltage of a QB node; and

a QB node controller configured to control the voltage of the QB node, based on a voltage of a control power source and the voltage of the Q node, and

wherein the voltage of the control power source has an on level in a vertical active period of one frame and has an off level in a vertical blank period of the one frame.

2. The gate driver of claim **1**, wherein the QB node controller comprises:

a fourth transistor connected to an input terminal of the control power source and a first control node;

a fifth transistor configured to connect the first control node to an input terminal of a second low power source, based on the voltage of the Q node;

a sixth transistor configured to apply the voltage of the control power source to the QB node, based on the voltage of the first control node; and

a seventh transistor configured to connect the QB node to the input terminal of the second low power source, based on the voltage of the Q node.

3. The gate driver of claim **2**, wherein a voltage of the first low power source is greater than a voltage of the second low power source.

4. The gate driver of claim **1**, further comprising a Q node controller configured to control the voltage of the Q node, based on a carry signal and the voltage of the QB node.

5. The gate driver of claim **4**, wherein the Q node controller comprises:

a first transistor connected to the Q node and an input terminal for a previous carry signal input from an $(n-4)^{th}$ stage;

a second transistor configured to connect the Q node to an input terminal of a second low power source, based on a next carry signal input from an $(n+6)^{th}$ stage; and

a third transistor configured to connect the Q node to the input terminal of the second low power source, based on the voltage of the QB node.

6. The gate driver of claim **5**, wherein a voltage of the first low power source is greater than a voltage of the second low power source.

7. The gate driver of claim **1**, further comprising:

an eighth transistor configured to connect the QB node to an input terminal of a second low power source, based on a reset signal; and

a ninth transistor configured to connect the output node to the input terminal of the first low power source, based on the reset signal.

8. The gate driver of claim **7**, wherein the reset signal is input at an on level for a partial time of the vertical blank period of the one frame, and is input at an off level in the vertical active period and the other time of the vertical blank period of the one frame.

9. The gate driver of claim **7**, wherein a voltage of the first low power source is greater than a voltage of the second low power source.

10. A display apparatus comprising:

a display panel including a plurality of gate lines; and

a gate driver including a plurality of stages connected to the plurality of gate lines,

wherein an n^{th} stage of the plurality of stages comprises:

a pull-up transistor configured to control a flow of a current between an output node and an input terminal for an n^{th} clock, based on a voltage of a Q node;

a pull-down transistor configured to control a flow of a current between the output node and an input terminal of a first low power source, based on a voltage of a QB node; and

a QB node controller configured to control the voltage of the QB node, based on a voltage of a control power source and the voltage of the Q node,

wherein the voltage of the control power source has an on level in a vertical active period of one frame and has an off level in a vertical blank period of the one frame, where n is an integer.

11. The display apparatus of claim **10**, further comprising a Q node controller configured to control the voltage of the Q node, based on a carry signal and the voltage of the QB node.

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