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INTEGRATED CIRCUIT

Abstract

An integrated circuit includes a first conductive structure including a root portion of the first conductive structure, tine portions that are arranged in a first semiconductor layer, a neck portion surrounded by a film structure. The integrated circuit further includes a second conductive structure having first and second portions that are stacked along a first direction. The first portion of the second conductive structure is surrounded by the film structure and the second portion of the second conductive structure is in the first semiconductor layer. A third conductive structure in the integrated circuit has horizontal and vertical structures. The horizontal structure extends in a second semiconductor layer and the vertical structure passes through the second semiconductor layer and the film structure to contact a first conductive rail. The first conductive rail and the tine portions are apart from the horizontal structure along the first direction by a same distance.

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Background/Summary

CROSS-REFERENCE [0001] The present application is a continuation of U.S. application Ser. No. 18/474,822,filed Sep. 26, 2023, which is a continuation application of U.S. application Ser. No. 17/035,160, filed Sep. 28, 2020, now U.S. Pat. No. 11,817,392, issued Nov. 14, 2023, the full disclosures of which are incorporated herein by reference.

BACKGROUND
[0002] Integrated circuits (ICs) have experienced exponential growth. The design of the ICs has produced generations with smaller size and having more complicated circuits. Increasingly dense ICs result in benefits in terms of speed, functionality and cost, but cause increasingly difficult design and fabrication issues.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0003] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.
[0004] FIGS. **1**A to **1**B are layout diagrams of an integrated circuit (IC), in accordance with some embodiments of the present disclosure.
[0005] FIG. **2** is a cross-section schematic diagram of a layout diagram corresponding to the layout diagram of FIG. **1**A or **1**B, in accordance with some embodiments of the present disclosure.
[0006] FIGS. **3**A to **3**C are layout diagrams of an IC, in accordance with some embodiments of the present disclosure.
[0007] FIG. **4** is a layout diagram of an IC, in accordance with some embodiments of the present disclosure.
[0008] FIGS. **5**A to **5**C are cross-section schematic diagrams of layout diagrams corresponding to the layout diagram of FIG. **4**, in accordance with some embodiments of the present disclosure.
[0009] FIG. **6** is a flow chart of a method for manufacturing an IC, in accordance with some embodiments of the present disclosure.
[0010] FIGS. **7**A to **7**G are schematic diagrams, in cross-sectional view of part of an IC corresponding to the IC of FIG. **4**, illustrating various processes of the method of FIG. **6**, in accordance with some embodiments of the present disclosure.
[0011] FIG. **8** is a layout diagram of an IC, in accordance with some embodiments of the present disclosure.
[0012] FIGS. **9**A to **9**C are cross-section schematic diagrams of layout diagrams corresponding to the layout diagram of FIG. **8**, in accordance with some embodiments of the present disclosure.

[0013] FIGS. **10**A to **10**C are schematic diagrams, in cross-sectional view of part of an IC corresponding to the IC of FIG. **8**, illustrating various processes of the method of FIG. **6**, in accordance with some embodiments of the present disclosure.
[0014] FIG. **11**A is a circuit diagram of an IC, in accordance with some embodiments of the present disclosure.
[0015] FIG. **11**B is a layout diagram of an IC corresponding to the IC of FIG. **11**A, in accordance with some embodiments of the present disclosure.
[0016] FIG. **12**A is a circuit diagram of an IC, in accordance with some embodiments of the present disclosure.
[0017] FIG. **12**B is a layout diagram of an IC corresponding to the IC of FIG. **12**A, in accordance with some embodiments of the present disclosure.
[0018] FIG. **13**A is a circuit diagram of an IC, in accordance with some embodiments of the present disclosure.
[0019] FIG. **13**B is a layout diagram of an IC corresponding to the IC of FIG. **13**A, in accordance with some embodiments of the present disclosure.
[0020] FIG. **14**A is a circuit diagram of an IC, in accordance with some embodiments of the present disclosure.
[0021] FIG. **14**B is a layout diagram of an IC corresponding to the IC of FIG. **14**A, in accordance with some embodiments of the present disclosure.
[0022] FIG. **15**A is a circuit diagram of an IC, in accordance with some embodiments of the present disclosure.
[0023] FIG. **15**B is a layout diagram of an IC corresponding to the IC of FIG. **15**A, in accordance with some embodiments of the present disclosure.
[0024] FIG. **16**A is a circuit diagram of an IC, in accordance with some embodiments of the present disclosure.
[0025] FIG. **16**B is a layout diagram of an IC corresponding to the IC of FIG. **16**A, in accordance with some embodiments of the present disclosure.
[0026] FIG. **17**A is a circuit diagram of an IC, in accordance with some embodiments of the present disclosure.
[0027] FIGS. **17**B to **17**E is a layout diagram of an IC corresponding to the IC of FIG. **17**A, in accordance with some embodiments of the present disclosure.
[0028] FIG. **18**A is a circuit diagram of an IC, in accordance with some embodiments of the present disclosure.
[0029] FIG. **18**B is a layout diagram of an IC corresponding to the IC of FIG. **18**A, in accordance with some embodiments of the present disclosure.
[0030] FIG. **19**A is a circuit diagram of an IC, in accordance with some embodiments of the present disclosure.
[0031] FIG. **19**B is a layout diagram of an IC corresponding to the IC of FIG. **19**A, in accordance with some embodiments of the present disclosure.
[0032] FIG. **20** is a flow chart of a method for fabricating an IC, in accordance with some embodiments of the present disclosure.
[0033] FIG. **21** is a block diagram of a system for designing an IC layout design, in accordance with some embodiments of the present disclosure.
[0034] FIG. **22** is a block diagram of an IC manufacturing system, and an IC manufacturing flow associated therewith, in accordance with some embodiments.

DETAILED DESCRIPTION

[0035] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0036] The terms used in this specification generally have their ordinary meanings in the art and in the specific context where each term is used. The use of examples in this specification, including examples of any terms discussed herein, is illustrative, and in no way limits the scope and meaning of the disclosure or of any exemplified term. Likewise, the present disclosure is not limited to various embodiments given in this specification.

[0037] Although the terms “first,” “second,” etc., may be used herein to describe various elements, these elements should not be limited by these terms. These terms are used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the embodiments. As used herein, the term “and/or” includes any and all combinations of one or more of the associated listed items.

[0038] In this document, the term “coupled” may also be termed as “electrically coupled”, and the term “connected” may be termed as “electrically connected”. “Coupled” and “connected” may also be used to indicate that two or more elements cooperate or interact with each other.

[0039] Furthermore, spatially relative terms, such as “underlying,” “below,” “lower,” “overlying,” “upper” and the like, may be used throughout the description for ease of understanding to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The structure may be otherwise oriented (e.g., rotated **90** degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0040] As used herein, “around”, “about”, “approximately” or “substantially” shall generally refer to any approximate value of a given value or range, in which it is varied depending on various arts in which it pertains, and the scope of which should be accorded with the broadest interpretation understood by the person skilled in the art to which it pertains, so as to encompass all such modifications and similar structures. In some embodiments, it shall generally mean within 20 percent, preferably within 10 percent, and more preferably within 5 percent of a given value or range. Numerical quantities given herein are approximate, meaning that the term “around”, “about”, “approximately” or “substantially” can be inferred if not expressly stated, or meaning other approximate values.

[0041] Reference is now made to FIGS. **1**A and **1**B. FIG. **1**A is a layout diagram **100**A of an integrated circuit (IC), and FIG. **1**B is a layout diagram **100**B of an IC, in accordance with some embodiments of the present disclosure. For simplicity of illustration of the layout diagram **100**A or **100**B, it is merely illustrates a few patterns disposed in one metal layer which, for example, in some embodiments, is a metal-zero (M**0**) layer hereinafter.

[0042] For illustration in FIG. **1**A, the layout diagram **100**A includes conductive rails P**01**, P**02**, S**01**, S**02**, S**03** and S**04**, conductive segments **111**, **112**, **121**, **122** and **123**, and cut segments CT. For simplicity, each of the conductive rails S**01**, S**02**, S**03** and S**04** is referenced as S**0** hereinafter for illustration, because each of the conductive rails S**01**, S**02**, S**03** and S**04** operates in a similar way in some embodiments.

[0043] The conductive rails P**01**, P**02** and S**0** are disposed in the same metal layer which, in some embodiments, the M**0** layer, and are separated from each other in a layout view. The conductive rails S**0** are disposed between the conductive rails P**10** and P**20** in a layout view. The conductive segment **111** is disposed on the conductive rail P**01**, and the conductive segment **112** is disposed on the conductive rail P**02**. The conductive segments **121-123** are disposed on and between at least two adjacent conductive rails S**0**. Specifically, the conductive segment **121** is disposed on and disposed between the conductive rails S**03** and S**04**. The conductive segment **122** is disposed on and disposed between the conductive rails S**02** and S**03**. The conductive segment **123** is disposed on and disposed between the conductive rails S**01** and S**02**. Alternatively stated, in a layout view, the conductive segment **121** is partially overlapped with the conductive rails S**03** and S**04**; the conductive segment **122** is partially overlapped with the conductive rails S**02** and S**03**; and the conductive segment **123** is partially overlapped with the conductive rails S**01** and S**02**. Each of the cut segments CT is disposed across one of the conductive rails S**0**. For example, with reference to FIG. **1**A, the cut segment CT with labeling is disposed across the conductive rail S**02**.

[0044] In some embodiments, the conductive rails P**01** and P**02** are configured to receive power signals (which are discussed at least with reference to FIGS. **4** and **5**A to **5**C) that are disposed in another metal layer which, for example, in some embodiments, is a first metal (M**1**) layer hereinafter. The M**1** layer is disposed above the M**0** layer where disposed the conductive rails P**01** and P**02**. In various embodiments, the conductive rails P**01** and P**02** are indicated as power conductive rails, for transmitting the power signals including, for example, supply voltage signals (which is indicated as VDD discussed with reference to FIG. **4**) or reference voltage signals (which is indicated as VSS discussed with reference to FIG. **4**). In some other embodiments, the conductive rails P**01** and P**02** are referred to as a pair of power conductive rails, and are configured to transmit power signals with voltages that are different from one another.

[0045] In some embodiments, the conductive rails S**0** are configured to receive data signals that are disposed in a same metal layer where the conductive rails P**01** and P**02** are disposed (i.e., the M**0** layer). In various embodiments, the conductive rails S**0** are indicated as signal conductive rails, for transmitting the data signals including, for example, signals (which is indicated as D**1** and D**2** shown in FIG. **4**). In some other embodiments, at least two conductive rails S**0** are coupled to each other, for transmitting the same data signals.

[0046] In some embodiments, each of the cut segments CT is configured to cut off at least one pattern in the layout diagram **100**A, for separating this pattern into two portions. In various embodiments, the cut segments CT are removed before generating a layout diagram for fabricating the IC.

[0047] In some embodiments, the conductive segments **111** and **112** are shaped as extending rails that are similar to the conductive rails P**01** and P**02**. In various embodiments, the conductive segment **111** is coupled to the conductive rail P**01**, and is spaced apart from the power signal that is disposed in M**1** layer and is coupled to the conductive rail P**01**. In further embodiments, the conductive segment **111** contacts the conductive rail P**01**. Similarly, the conductive segment **112** is coupled to the conductive rail P**02**, and is spaced apart from the power signal that is disposed in M**1** layer and is coupled to the conductive rail P**02**. In further embodiments, the conductive segment **112** contacts the conductive rail P**02**. In various embodiments, the conductive segments **111** and **112** are indicated as “V**0** rail”, for forming additional conductive segments/traces/tracks/patterns on the conductive rails P**01** and P**02**. Alternatively stated, a height of the conductive rails P**01** or P**02** in the M**0** layer is increased by disposing the conductive segments **111** or **112** on and above the conductive rails P**01** or P**02**. In some other embodiments, the conductive rails P**01** and P**02**, and the conductive segments **111** and **112** are made of a metal material that is same as one another.

[0048] In some embodiments, the conductive segments **121**, **122** and **123** are shaped as a block. In various embodiments, the conductive segment **121** is coupled between the conductive rails S**03** and S**04**, and is spaced apart from the data signal (which is discussed at least with reference to FIGS. **4** and **5**A to **5**C) that is disposed in M**1** layer. In further embodiments, the conductive segment **121** contacts the conductive rails S**03** and S**04**. Similarly, the conductive segment **122** is coupled between the conductive rails S**02** and S**03**, and the conductive segment **123** is coupled between the conductive rails S**01** and S**02**. Each of the conductive segments **122** and **123** is spaced apart from the data signal that is disposed in M**1** layer. In further embodiments, the conductive segment **122** contacts the conductive rails S**02** and S**03**; and the conductive segment **123** contacts the conductive rails S**01** and S**02**. In various embodiments, the conductive segments **121**, **122** and **123** are indicated as "M**0** jumper", for forming additional conductive segments/traces/tracks/patterns on the conductive rails S**0**, and disposing across at least two adjacent conductive rails S**0**. Alternatively stated, a height of the conductive rails S**0** in the M**0** layer is increased by disposing the conductive segments **121**, **122** or **123** on and above the conductive rails S**0**. In some other embodiments, the conductive rails S**0**, and the conductive segments **121**, **122** and **123** are made of a metal material that is same as one another.

[0049] The layout diagram **100**B of the IC has a configuration similar to that of the layout diagram **100**A of the IC as illustrated in FIG. **1**A, and similar detailed description is therefore omitted. Compared to FIG. **1**A, the layout diagram **100**B shown in FIG. **1**B includes a conductive segment **124**, rather than the conductive segments **121-123**, disposed on the conductive rails S**0**. The conductive segment **124** is disposed on and disposed between the conductive rails S**02** and S**03**. Alternatively stated, in a layout view, the conductive segment **124** is partially overlapped with the conductive rails S**02** and S**03**. In some embodiments, the conductive segment **124** has a configuration or arrangement similar to the conductive segments **121-123** shown in FIG. **1**A.

[0050] The number and arrangement of conductive segments or conductive rails shown in FIGS. **1**A and **1**B are given for illustrative purposes. Various numbers and arrangements of conductive segments or conductive rails to implement the layout diagram **100**A in FIG. **1**A or the layout diagram **100**B in FIG. **1**B are within the contemplated scope of the present disclosure. For example, in some embodiments, in addition to the conductive segments **121**, **122** and **123** or the conductive rails P**01**, P**02** and S**0** shown in FIG. **1**A, the layout diagram **100**A further includes the conductive rails disposed between the conductive rails P**01**, P**02** and next to the conductive rails S**0**, in a layout view.

[0051] Reference is now made to FIG. **2**. FIG. **2** is a cross-section schematic diagram of a layout diagram **200** corresponding to the layout diagram **100**A of FIG. **1**A or the layout diagram **100**B of FIG. **1**B, taken along a line **10-10**, in accordance with some embodiments of the present disclosure. The layout diagram **200** with respect to the embodiments of FIG. **1**A or **1**B, like elements in FIG. **2** are designated with the same reference numbers for ease of understanding.

[0052] For illustration in FIG. **2**, the conductive segments **211** and **212** are disposed on the conductive rails P**10** and P**20**, respectively, as discussed with embodiments shown in FIGS. **1**A and **1**B. The conductive segment **213** is disposed on two adjacent conductive rails S**02** and S**03**. Furthermore, a part of the conductive segment **213** is disposed in a space between the conductive rails S**02** and S**03**, in a direction along the line **10-10** which is also referred to as a column direction with reference to FIGS. **1**A-**1**B. Alternatively stated, the conductive segment **213** is disposed stuck between the conductive rails S**02** and S**03**.

[0053] Reference is now made to FIGS. **3**A to **3**C. FIGS. **3**A to **3**C are layout diagrams **300**A, **300**B and **300**C of an IC, in accordance with some embodiments of the present disclosure. Each of the layout diagrams **300**A, **300**B and **300**C of the IC has a configuration similar to that of the layout diagram **100**A of the IC as illustrated in FIG. **1**A or the layout diagram **100**B of the IC as illustrated in FIG. **1**B, and similar detailed description is therefore omitted. Each of the layout diagrams **300**A, **300**B and **300**C with respect to the embodiments of FIG. **1**A or **1**B, like elements in FIGS. **3**A to **3**C are designated with the same reference numbers for ease of understanding.

[0054] Compared to FIG. **1**A or **1**B, each of the layout diagrams **300**A, **300**B and **300**C shown in FIGS. **3**A to **3**C further includes gate segments **311** and **312** disposed across the conductive rails P**01** and P**02** and the conductive rails S**0**, in a layout view. As illustrated in FIGS. **3**A to **3**C, the conductive rails P**01**, P**02** and S**0** extend along a row direction, and the gate segments **311** and **312** extend along a column direction that is substantially perpendicular to the row direction.

[0055] In some embodiments, the gate segments **311** and **312** are formed in an active area that is below the M**0** layer, for forming gate terminals of transistors included in the IC. In various embodiments, the gate segments **311** and **312** include polysilicon (P**0**), and are formed by a gate forming process, which is also referred to as an "P**0** process" using a polysilicon mask.
[0056] In some embodiments, a distance between two adjacent gates which are, for example, with reference to FIGS. **3**A to **3**C, the gate segments **311** and **312**, is indicated as a gate pitch D**1**. The gate pitch D**1** is also referred to as a poly pitch D**1** hereinafter. In some other embodiments, a distance between two adjacent conductive rails which are, for example, with reference to FIGS. **3** A to **3**C, the rail segments S**01** and S**02**, is indicated as a M**0** pitch D**2**. In alternative embodiments, at least one of the poly pitch D**1** or the M**0** pitch D**2** is limited by design rules in the layout diagram of the IC, and the design rules are associated with the fabrication processes or technologies of the IC.
[0057] For illustration in FIG. **3**A, the layout diagram **300**A includes conductive segments **121**, **122** and **123** shaped as blocks and disposed on and between the conductive rails S**0**. The layout diagram **300**A also includes a pair of conductive segments **111** and **112** shaped as extending rails and disposed on a pair of conductive rails P**01** and P**02**, respectively. For each of the conductive segments **121**, **122** and **123**, it is shaped as a square, and a width of each of the conductive segments **121**, **122** and **123** is approximately equal to one M**0** pitch D**2**. Alternatively stated, a size of each of the conductive segments **121**, **122** and **123** is approximately equal to a square of M**0** pitch D**2** (i.e., M**0** pitch D**2***M**0** pitch D**2**).
[0058] A distance between corresponding corners of two adjacent conductive segments is about in a range of half of one poly pitch D**1** to one poly pitch D**1** (i.e., 0.5*poly pitch D**1**˜**1***poly pitch D**1**). As illustrated in FIG. **3**A, a corner of the conductive segments **121** is separated from a corresponding corner of the conductive segments **122** by a distance C**1**, and the distance C**1** is about in a range discussed above.
[0059] Furthermore, a width of each of the conductive segments **111** and **112** is substantially equal to or smaller than a width of each of the conductive rails P**01** and P**02**. In some embodiments, a length of each of the conductive segments **111** and **112** is also substantially equal to or smaller than a length of each of the conductive rails P**01** and P**02**.
[0060] A distance between one conductive segment indicated as the V**0** rail and one conductive segment indicated as the M**0** jumper is about in a range of half of the poly pitch D**1** to 1.2 times of the poly pitch D**1** (i.e., 0.5*poly pitch D**1**˜1.2*poly pitch D**1**), in some embodiments. As illustrated in FIG. **3**A, the conductive segment **111** is indicated as the V**0** rail that is disposed on one of the conductive rails P**01** and P**02**. The conductive segment **123** is indicated as the M**0** jumper that is disposed on at least two adjacent conductive rails S**0**. The conductive segment **111** is separated from the conductive segment **123**, which is disposed adjacent to the conductive segment **111**, by a distance C**2**. The distance C**2** is about in a range discussed above.
[0061] Compared to embodiments illustrated in FIG. **3**A, the layout diagram **300**B includes one conductive segment **124** shaped as a railed block and disposed on and between the conductive rails S**0**. The conductive segment **124**, it is shaped as a rectangular block, and a length L**1** of the conductive segment **124** is greater than twice of the poly pitch D**1** (i.e., L**1**>2*poly pitch D**1**), in some embodiments.
[0062] A distance between one conductive segment indicated as the V**0** rail and one conductive segment indicated as the M**0** jumper is about in a range of half of the poly pitch D**1** to one of the poly pitch D**1** (i.e., 0.5*poly pitch D**1**˜1*poly pitch D**1**), in some embodiments. For example, with reference to FIG. **3**B, the conductive segment **111** disposed the conductive rail P**01** is separated from the conductive segment **124**, that is disposed adjacent to the conductive segment **111** and disposed on the conductive rail S**01**, by a distance C**3**. The distance C**3** is about in a range discussed above.
[0063] Compared to embodiments illustrated in FIG. **3**A, the layout diagram **300**C further includes one conductive segment **124** shaped as a railed block and disposed on and between the conductive

rails S**0**. In some embodiments, the layout diagram **300**C is an alternative embodiment combining with the layout diagrams **300**A and **300**B.

[0064] Each of the conductive segments **121**, **122** and **123** is shaped as a square, and a width of the same is approximately equal to one M**0** pitch D**2**. Alternatively stated, a size of each of the conductive segments **121**, **122** and **123** is approximately equal to a square of M**0** pitch D**2** (i.e., M**0** pitch D**2***M**0** pitch D**2**). Similar to that illustrated in FIG. **3**A, a distance between two adjacent conductive segments **121**, **122** or **123** is about in a range of half of one poly pitch D**1** to one poly pitch D**1** (i.e., 0.5*poly pitch D**1**˜1*poly pitch D**1**). For example, with reference to FIG. **3**C, a distance between a corner of the conductive segments **121** and a corresponding corner of the conductive segment **122** is indicated as a distance C**4**. The distance C**4** is in a range of 0.5*poly pitch D**1** to 1*poly pitch D**1**. Furthermore, a length or width of the conductive segments **111** or **112** is also substantially equal to or smaller than a length or a width of the conductive rails P**01** or P**02**.

[0065] In some embodiments, a distance between one conductive segment indicated as the V**0** rail and another conductive segment indicated as the M**0** jumper is not limited in the layout diagram **300**C. For example, with reference to FIG. **3**C, a distance between the conductive segment **111** indicated as the V**0** rail and the conductive segment **124** indicated as the M**0** jumper may be smaller than 0.5*poly pitch D**1**.

[0066] In some embodiments, the layout diagram **300**C is generated by at least one mask (which is discussed with reference to FIG. **22**). For example, the conductive segments **111** and **112** are patterned by utilizing a first mask. The remaining conductive segments **121**, **122** and **123** are patterned by utilizing a second mask. Accordingly, the layout diagram **300**C has less design limitations compared to the layout diagram **300**A or **300**B that is patterned by one mask.

[0067] The configuration and arrangement of the layout diagrams **300**A, **300**B and **300**C shown in FIGS. **3**A to **3**C is given for illustrative purposes. Various configurations and arrangements of the layout diagrams **300**A, **300**B and **300**C to implement the IC are within the contemplated scope of the present disclosure. For example, in some embodiments, in a layout view, at least one of the conductive segments **121**, **122**, **123** or **124** is disposed on and between or across more than three conductive rails S**0**.

[0068] Reference is now made to FIG. **4**. FIG. **4** is a layout diagram **400** of an IC, in accordance with some embodiments of the present disclosure. The layout diagram **400** with respect to the embodiments of FIG. **1**A or **1**B, like elements in FIG. **4** are designated with the same reference numbers for ease of understanding.

[0069] For illustration in FIG. **4**, the layout diagram **400** includes conductive rails P**01**, P**02** and P**03**, and conductive rails S**01**, S**02**, S**03** and S**04** disposed in the M**0** layer and extending along a row direction. In some embodiments, the conductive rails S**01**, S**02**, S**03** and S**04** are referenced as S**0** hereinafter for simplicity of illustration. In a layout view, the conductive rails P**01** and P**02** are separated from one another by the conductive rails S**0**, and the conductive rails P**02** and P**03** are separated from one another by additional conductive rails that are not shown in FIG. **4**. In some embodiments, the conductive rail P**01** is identical to the conductive rail P**03**. The conductive rails P**01**, P**02**, and S**0** of the layout diagram **400** have configurations similar to that of the layout diagram as illustrated in FIG. **1**A, and similar detailed description is therefore omitted.

[0070] The layout diagram **400** further includes conductive segments **411***a*, **411***b*, **412***a*, **412***b* and **421** disposed on the conductive rails P**01**, P**02**, and S**0**, signal rails P**11**, P**12**, S**11** and S**12** disposed in the M**1** layer, and vias **431**, **432**, **433** and **434** disposed between the M**0** layer and the M**1** layer. The signal rails P**11**, P**12**, S**11** and S**12** are separated from each other, and extend along a column direction, in a layout view. Alternatively stated, in a layout view, the signal rails P**11**, P**12**, S**11** and S**12** are disposed above and across the conductive rails P**01**, P**02**, P**03** and S**0**. The vias **431**, **432**, **433** and **434** are overlapped with at least two of the conductive rails P**01**, P**02** and S**0** and the signal rails P**11**, P**12**, S**11** and S**12**, in a layout view. Specifically, in a layout view, the via **431** is overlapped with the conductive rail P**01** and the signal rail P**11**; the via **434** is overlapped with the conductive rail P**02** and the signal rail P**12**; the via **432** is overlapped with the conductive rail S**01** and the signal rail S**11**; and the via **433** is overlapped with the conductive rail S**03** and the signal rail S**12**.

[0071] The conductive segments **411***a* and **411***b* are disposed on the conductive rail P**01** and are separated from each other, in a layout view. The via **431** is disposed between the conductive segments **411***a* and **411***b*, in a layout view. Alternatively stated, one conductive segment indicated as the V**0** rail is disposed on the conductive rail P**01**. Such conductive segment includes several separated portions including, for example, with reference to FIG. **4**, the conductive segments **411***a* and **411***b*. In addition, at least one via is disposed between these separated portions, in a layout view. With reference to FIG. **4**, the via **431** is disposed between the separated portions which are the conductive segments **411***a* and **411***b*, in a layout view. Similarly, the conductive segments **412***a* and **412***b* are disposed on the conductive rail P**02**, and are separated from each other in a layout view. The via **434** is disposed between the conductive segments **412***a* and **412***b*, in a layout view.

[0072] The conductive segment **421** is disposed on and disposed between the conductive rails S**02** and S**03**. The conductive segment **421** is shaped as a railed block and extends along the row direction. Alternatively stated, at least one conductive segment indicated as the M**0** jumper extends parallel to the conductive rails S**0**. Such conductive segment is disposed on and between the conductive rails S**0**, and is separated from another conductive segment indicated as the V**0** rail in a layout view, in some embodiments. For example, the conductive segment **421** that is indicated as the M**0** jumper is separated from the conductive segment **411***b* or **412***b* that is indicated as the V**0** rail, in a layout view.

[0073] In some embodiments, the signal rails P**11** and P**12** are configured to provide power signals to the conductive rails P**01** and P**02**. In various embodiments, the signal rail P**11** is configured to provide a voltage signal that is different from that of the signal rail P**12**. For example, the signal rail P**11** is configured to provide the supply voltage signal with voltage VDD, and the signal rail P**12** is configured to provide the reference voltage signal with voltage VSS. The voltage VDD is higher than the voltage VSS which, in some embodiments, is referred to as a ground. In alternative embodiments, the signal rails P**11** and P**12** are indicated as power rails, for providing the power signals (e.g., VDD or VSS) to the power conductive rails including, for example, the conductive rails P**01**, P**02** and P**03**.

[0074] In some embodiments, the signal rails S**11** and S**12** are configured to provide data signals to the conductive rails S**0**. In various embodiments, the signal rail S**11** is configured to provide a data signal that is different from that of the signal rail S**12**. For example, the signal rail S**11** is configured to provide a control signal for controlling first transistors, and the signal rail S**12** is configured to provide another control signal for controlling second transistors. In alternative embodiments, the signal rails S**11** and S**12** are indicated as data rails, for providing the data signals to the signal conductive rails including, for example, the conductive rails S**01** to S**04**.

[0075] Reference is now made to FIGS. **5**A to **5**C. FIG. **5**A is a cross-section schematic diagram of a layout diagram **500**A corresponding to the layout diagram **400** of FIG. **4**, taken along a line A-A′; FIG. **5**B is a cross-section schematic diagram of a layout diagram **500**B corresponding to the layout diagram **400** of FIG. **4**, taken along a line B-B′; and FIG. **5**C is a cross-section schematic diagram of a layout diagram **500**C corresponding to the layout diagram **400** of FIG. **4**, taken along a line C-C′, in accordance with some embodiments of the present disclosure. The layout diagrams **500**A to **500**C with respect to the embodiments of FIG. **4**, like elements in FIGS. **5**A to **5**C are designated with the same reference numbers for ease of understanding.

[0076] For illustration in FIG. **5**A, the signal rail P**11** extends along the line A-A′ and across from the conductive rails P**01**, S**0** to the conductive rail P**02**. The via **431** is disposed between the conductive rail P**01** and the signal rail P**11** without extra spacing. The conductive segment **412***a* is disposed on the conductive rail P**02** and is spaced apart from the signal rail P**11**. With above configurations, a height of the conductive segment **412***a* is smaller than a height of the via **431**.

[0077] In some embodiments, the conductive rail POI is coupled through the via **431** to the signal rail P**11**, for receiving the supply voltage signal with voltage VDD. With the above configurations, since the conductive segment **412***a* is separated from the signal rail P**11**, the conductive segment **412***a* or the conductive rail P**02** is not coupled to or does not contact the signal rail P**11**. In various embodiments, both of the conductive segment **412***a* and the conductive rail P**02** are coupled to the ground by separating from the signal rail P**11**. In addition, the conductive rail P**02** is not coupled to any signal rails disposed in the M**1** layer, and is indicated as a ground rail. Similarly, since the conductive rails S**0** are separated from the signal rail P**11**, these conductive rails S**0** are not coupled to the signal rail P**11**.

[0078] For illustration in FIG. **5**B, the signal rail S**11** extends along the line B-B′ and across from the conductive rails P**01**, S**0** to the conductive rail P**02**. The conductive segment **411***b* is disposed on the conductive rail P**01** and is spaced apart from the signal rail S**11**. Similarly, the conductive segment **412***b* is disposed on the conductive rail P**02** and is spaced apart from the signal rail S**11**. The conductive segment **421** is disposed on two adjacent conductive rails S**02** and S**03** and is also spaced apart from the signal rail S**11**. Alternatively stated, each of the conductive segments **411***b*, **412***b* and **421** is separated from the signal rail S**11** along a vertical direction that is perpendicular to the line B-B′ illustrated in FIG. **5**B. In addition, the via **432** is disposed between the conductive rail S**01** and the signal rail S**11** without extra spacing. With above configurations, a height of the conductive segment **411***b*, **421** or **412***b* is smaller than a height of the via **432**.

[0079] Compared to embodiments illustrated in FIG. **5**A, the layout diagram **500**B further illustrates conductive segments **511** and **512**, and vias **521** and **522**. The conductive segments **511** and **512** are disposed in the active area (not shown) that is below the M**0** layer, and the vias **521** and **522** are disposed between the active area and the M**0** layer. Specifically, the via **521** is disposed between the conductive segment **511** and the conductive rail S**01** without extra spacing. The via **522** is disposed between the conductive segment **512** and the conductive rail S**03** without extra spacing.

[0080] In some embodiments, the conductive segment **511** is coupled through the via **521** to the conductive rail S**01**. The conductive rail S**01** is further coupled through the via **432** to the signal rail S**11**, for receiving the data signal provided to the conductive segment **511**. Furthermore, the conductive segment **512** is coupled through the via **522** to the conductive rail S**03**, and the conductive rail S**03** is further coupled through the conductive segment **421** to the conductive rail S**02**. Alternatively stated, at least two adjacent conductive rails including, for example, the conductive rails S**02** and S**03**, are coupled together through the conductive segment indicated as the M**0** jumper including, for example, the conductive segment **421**.

[0081] In some embodiments, the conductive segments **511** and **512** are disposed in the active area, for forming source or drain terminals of transistors included in the IC. In various embodiments, the conductive segments **511** and **512** are referred to as a metal-like defined (MD) segments hereinafter. In alternative embodiments, the vias **521** and **522**, coupled from the MD segments **511** and **512** to other elements of the IC, are referred to as via-defined (VD) vias hereinafter.

[0082] In some embodiments, the MD segment includes a portion of at least one metal layer, e.g., one or more of copper (Cu), silver (Ag), tungsten (W), titanium (Ti), nickel (Ni), tin (Sn), aluminum (Al) or another metal or material suitable for providing a low resistance electrical connection between elements included in the IC, i.e., a resistance level below a predetermined threshold corresponding to one or more tolerance levels of a resistance-based effect on circuit performance. In some other embodiments, the MD segment includes a section of the semiconductor substrate and/or an epitaxial layer having a doping level, e.g., based on an implantation process, sufficient to cause the segment to have the low resistance level. In various embodiments, a doped MD segment includes one or more of silicon (Si), SiGe, silicon-carbide (SiC), boron (B), phosphorous (P), arsenic (As), gallium (Ga), a metal as discussed above, or another material suitable for providing the low resistance level. In some embodiments, an MD segment includes a

dopant having a doping concentration of about 1*1016 per cubic centimeter (cm.sup.−3) or greater.
[0083] For illustration in FIG. 5C, the signal rail S**12** extends along the line C-C′ and across from the conductive rails P**01**, S**0** to the conductive rail P**02**. The conductive segment **411***b* is disposed on the conductive rail P**01** and is spaced apart from the signal rail S**12**. Similarly, the conductive segment **412***b* is disposed on the conductive rail P**02** and is spaced apart from the signal rail S**12**. Alternatively stated, each of the conductive segments **411***b* and **412***b* is separated from the signal rail S**12** along a vertical direction that is perpendicular to the line C-C′ illustrated in FIG. **5**C. In addition, the via **433** is disposed between the conductive rail S**03** and the signal rail S**12** without extra spacing. With above configurations, a height of the conductive segment **411***b* or **412***b* is smaller than a height of the via **433**.
[0084] In some embodiments, the conductive rail S**03** is coupled through the via **433** to the signal rail S**12**, for receiving the data signal provided to the conductive rail S**03**. The conductive rail P**01** or P**02** is not coupled to the signal rail P**12**, for receiving the signal that is equivalently indicated as the ground.
[0085] Compared to embodiments illustrated in FIG. **5**A, the layout diagram **500**C further illustrates MD segments **513** and **514**, and VD vias **523** and **524**. The via **523** is disposed between the MD segment **513** and the conductive rail S**01** without extra spacing, and the via **524** is disposed between the MD segment **514** and the conductive rail P**02** without extra spacing. The MD segments **513** and **514** or the vias **523** and **524** have configurations similar to that of the MD segments **511** and **512** or the vias **521** and **522**, correspondingly, as illustrated in FIG. **5**B, and similar detailed description is therefore omitted.
[0086] In some approaches, no other conductive segments disposed on the conductive rails in the M**0** layer. With such configuration, a resistance coupled between the conductive rails and the signal rails in the M**1** layer is substantially contributed to a height of the conductive rail and a size of the via coupled between the M**0** and M**1** layers. It affects IR-drop issue and further slows down a working speed of the IC.
[0087] Compared to the above approaches, additional conductive segment including, for example, the conductive segment **412***a*, is disposed on the conductive rails including, for example, the conductive rail P**02**, in the M**0** layer. This additional conductive segment **412***a* is spaced apart from the M**1** layer, for increasing a height of the conductive rail P**02** in the M**0** layer without changing a cell height of the corresponding layout diagram **400**. Accordingly, a resistance of the conductive rail P**02** that is also referred to as the power conductive rail is reduced. It is reduced by disposing the conductive segment **412***a* indicated as the V**0** rail on the top surface of the conductive rail P**02**.
[0088] Furthermore, additional conductive segment including, for example, the conductive segment **421**, is disposed on and between at least two adjacent conductive rails including, for example, the conductive rails S**02** and S**03**. This additional conductive segment **421** is also spaced apart from the MI layer, for coupling these two adjacent conductive rails S**02** and S**03** together as a local interconnection. Accordingly, routings for coupling more than two conductive rails S**0** are reduced by disposing the conductive segment **421** that is indicated as the M**0** jumper. It further improves the electromagnetic bottleneck of the date signals transmitted in these conductive rails S**0** and the IC performance.
[0089] Reference is now made to FIG. **6** and FIGS. **7**A to **7**G. FIG. **6** is a flow chart of a method **600** for manufacturing an IC including the conductive rails P**01**, P**02** and S**0**, the conductive segments **411***a*, **411***b*, **412***a*, **412***b* and **421**, and vias **431** to **434** shown in FIG. **4**, or an IC shown in FIGS. **7**A to **7**G, in accordance with some embodiments of the present disclosure. FIGS. **7**A to **7**G are schematic diagrams, in cross-sectional view of part of the IC **700** corresponding to the IC of FIG. **4** along the column direction as illustrated in FIG. **4**, illustrating various processes of the method **600** of FIG. **6**, in accordance with some embodiments of the present disclosure. It is understood that additional operations can be provided before, during, and after the processes shown by FIG. **6** and FIGS. **7**A to **7**G, and some of the operations described below can be replaced or

eliminated, for additional embodiments of the method. The order of the operations/processes may be interchangeable. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements.

[0090] In operation S**610** of FIG. **6**, multiple conductive rails are formed within the M**0** layer of the IC **700**. The conductive rails include the conductive rails P**01**, P**02** and S**0** illustrated in FIG. **4**, and dielectric material stack between these conductive rails.

[0091] In operation S**620**, a film structure is formed on the conductive rails. Accordingly, the film structure is formed on the M**0** layer of the IC **700**. Alternatively stated, the film is deposited on the M**0** layer. The operations S**610**-S**620** are performed as illustrated in FIG. **7**A.

[0092] For illustration, as shown in FIG. **7**A, the IC **700** includes conductive rails P**02**, S**02**, S**03** and S**04**, and dielectric structure **710** formed in the M**0** layer, and includes a film structure **720** formed on the M**0** layer. The conductive rails P**02**, S**02**, S**03** and S**04** are separated from each other by the dielectric structure **710**. In some embodiments, a material of the dielectric structure **710** is different from a material of the film structure **720**. In various embodiments, the dielectric structure **710** and the film structure **720** are isolated from each other. In alternative embodiments, a thickness of the film structure **720** is substantially equal to a distance between the M**0** layer and the M**1** layer (which is at least shown in FIG. **7**E).

[0093] In operation S**630**, the film structure is patterned to form patterns. In some embodiments, the patterning operation is utilized photolithography and etching, for spacing a specific pattern in the film structure. The operation S**630** is processed as illustrated in FIG. **7**B.

[0094] For illustration, as shown in FIG. **7**B, patterns **731** and **732** are formed in the film structure **720**. Specifically, the pattern **731** is formed in the film structure **720** and formed above and between the conductive rails S**03** and S**04**. At a surface of the M**0** layer and a bottom of the film structure **720**, a part of the conductive rails S**03** and S**04** and a part of the film structure **720** are removed to form the pattern **731**. Moreover, the pattern **732** is formed in the film structure **720** and formed above and between the conductive rail P**02**. Similarly, around the surface of the M**0** layer, part of the film structure **720** is removed to form the pattern **732**.

[0095] In operation S**640**, the patterns are filled with a conductive material, to form a first conductive structure that includes a first conductive segment contacting a first conductive rail of the conductive rails. In some embodiments, the first conductive segment corresponds to at least one of the conductive segment **411***a* or **411***b* illustrated in FIG. **4** and the first conductive rail corresponds to the conductive rail P**01** illustrated in FIG. **4**. In other embodiments, the first conductive segment corresponds to at least one of the conductive segment **412***a* or **412***b* illustrated in FIG. **4** and the first conductive rail corresponds to the conductive rail P**02** illustrated in FIG. **4**. The operation S**640** is processed as illustrated in FIGS. **7**C-**7**D.

[0096] In some embodiments, the filling operation in S**640** is also indicated as a multi-metal gap fill process. In various embodiments, the patterns are filled with the conductive material, for forming interconnect structures between two adjacent metal layers which, for example, are the M**0** layer and the M**1** layer.

[0097] For illustration, as shown in FIG. **7**C, a conductive structure **740** is formed on the film structure **720**, and is further filled in the patterns **731** and **732**.

[0098] In some embodiments, a material of the conductive structure **740** is the same as a material of the conductive segments S**02** to S**04** and P**02** formed in the M**0** layers. Alternatively stated, a material of the pattern **731** or **732** is the same as a material of the conductive segment S**04** or P**02**. In various embodiments, if the conductive structure **740** physically contacts the conductive segments S**02** to S**04** and P**02** formed in the M**0** layers, the conductive structure **740** and the conductive segments S**02** to S**04** and P**02** are coupled to each other. In alternative embodiments, the conductive material is copper (Cu), cobalt (Co), tungsten (W), Ruthenium (Ru), aluminum (Al), graphene, or any other suitable conductive material.

[0099] For illustration, as shown in FIG. **7**D, conductive segments **751** and **752** are formed. In some embodiments, the conductive segments **752** corresponds to at least one of the conductive segment **411**_a_, **411**_b_, **412**_a_ or **412**_b_ that contacts the conductive rail P**01** or P**02**, illustrated in FIG. **4**. Thereby, the conductive segment **752** is able to form the first conductive segment that contacts the first conductive rail, as discussed in the operation S**640**. In other embodiments, the conductive segments **751** corresponds to the conductive segment **421** that contacts two adjacent conductive rails S**0**, illustrated in FIG. **4**.

[0100] As illustrated in FIG. **7**D, the conductive segment **751** is formed on the M**0** layer, and is formed on the part of the conductive rail S**03**, the film structure **720**, and the part of the conductive rail S**04**. Alternatively stated, the conductive segment **751** is formed above and between the conductive rails S**03** and S**04**. In addition, conductive segment **752** is formed on the M**0** layer, and is also formed on the conductive rail P**02**. Furthermore, the conductive segments **751** and **752**, and the film structure **720** have a same surface that is substantially parallel to the surface of the M**0** layer. Alternatively stated, all of the conductive segments **751** and **752** and the film structure **720** form a substantially plat surface above the M**0** layer. In some embodiments, the conductive segments **751** and **752** are made of the same conductive material as the conductive structure **740** is made.

[0101] In some embodiments, the operation S**640** further includes the following operations. The patterns filled with the conductive material and the film structure are polished. In some other embodiments, the polishing operation in S**640** is performed by chemical mechanical polishing (CMP) to remove extra conductive material on the top of surface. In various embodiments, part of the structures is removed with a combination of CMP and dry etch.

[0102] In operation S**650**, a dielectric structure covering the first conductive segment is formed. In some embodiments, the dielectric structure is formed and stacked on the remaining structure after performing the operation S**640**. In other embodiments, the M**1** layer is generated by forming the dielectric structure on the film structure, and is processed as illustrated in FIG. **7**E.

[0103] For illustration, as shown in FIG. **7**E, a dielectric structure **760** is generated by forming on the film structure **720** and the conductive segments **751** and **752**. In some embodiments, a material of dielectric structure **710** is the same as a material of the dielectric structure **760**. In various embodiments, a thickness of the dielectric structure **760** is substantially equal to a distance between the M**1** layer and a second metal layer (M**2**, not shown) above the M**1** layer.

[0104] In operation S**660**, part of the film structure and part of the dielectric structure are removed, to expose part of a second conductive rail of the conductive rails. In some embodiments, the second conductive rail corresponds to one of the conductive rails S**0** illustrated in FIG. **4**.

[0105] In operation S**670**, the conductive material is filled in the removed part of the film structure and the removed part of the dielectric structure, to form a second conductive structure that includes a via contacting the exposed part of the second conductive rail and a signal rail contacting the via. In some embodiments, the via included in the second conductive structure corresponds to the via **432** illustrated in FIG. **4**, and the signal rail included in the second conductive structure corresponds to the data rail S**11** illustrated in FIG. **4**. The operations S**660**-S**670** are processed as illustrated in FIGS. **7**F-**7**G.

[0106] For illustration, as shown in FIG. **7**F, part of the film structure **720** and part of the dielectric structure **760** are removed, and a structure **781** is exposed. Furthermore, the conductive material (not shown) are filled in the removed structures **720** and **760**, to form a via **771** and the structure **781** which corresponds to a signal rail. The via **771** and the structure **781** are contacted to each other, and correspond to the via **432** and the signal rail S**11** respectively, as shown in FIG. **4**, in some embodiments. Also illustrated in FIG. **7**G, part of the film structure **720** and part of the dielectric structure **760** are removed, and a structure **782** is exposed. Furthermore, the removed structures **720** and **760** are filled in the conductive material (not shown), to form a via **772** and the structure **782** which corresponds to a signal rail. The via **772** and the structure **782** are contacted to each other.

[0107] As illustrated in FIG. 7F, the IC **700** further includes via **771** formed on the M**0** layer and connected to a structure **781** formed in the M**1** layer. One terminal of the via **771** is formed on the conductive rail S**02**, and the other terminal of the via **771** is formed in the M**1** layer. With the operations discussed above, a height of via **771** is substantially equal to or slightly greater than a distance between the conductive rail S**02** and the structure **781**. Alternatively stated, a height of via **771** is substantially equal to or slightly greater than a distance between the M**0** layer and the M**1** layer.
[0108] In some embodiments, the via **771** is configured to be coupled between the conductive rail S**02** and the structure **781** formed in the M**1** layer. In various embodiments, the structure **781** is a signal rail that is configured to providing data signals. In some other embodiments, the via **771** is coupled between the conductive rail S**02** and the data rail S**11**, and corresponds to the via **432** shown in FIG. **4** or **5**B.
[0109] Moreover, the conductive segment **751** is formed on the M**0** layer as discussed above, and is separated from the M**1** layer by the dielectric structure **760**. Alternatively stated, the conductive segment **751** is spaced apart from the M**1** layer. With the operations discussed above, a height of the conductive segment **751** is smaller than a height of the via **771**. Similar to configurations of the conductive segment **751**, the conductive segment **752** is formed on the M**0** layer and is spaced apart from the M**1** layer. Also, a height of the conductive segment **752** is smaller than a height of the via **771**.
[0110] In some embodiments, the conductive segment **751** is coupled between the conductive rails S**03** and S**04**. In some other embodiments, the conductive segment **751** is referred to as the M**0** jumper, and corresponds to the conductive segment **421** shown in FIG. **4** or **5**B. In various embodiments, the conductive segment **752** is coupled to the conductive rail P**02**. In some other embodiments, the conductive segment **752** is referred to as the V**0** rail, and corresponds to the conductive segment **412***a* shown in FIG. **4** or **5**A.
[0111] In some embodiments, the operation for forming the conductive segments **751** and **752** and the via **771** with the above arrangement between the M**0** and MI layers is referred to as a dual damascene process. It makes connections between the conductive segments **751** and **752** and the structure **781** formed in the M**1** layer. In some other embodiments, the operation for forming the conductive segments **751** and **752** and the via **771** with the above arrangement between the M**0** and M**1** layers is referred to as a single damascene process. Compared to embodiments performed by the dual damascene process, the via **771** performed by the single damascene process has a greater height.
[0112] For illustration, as shown in FIG. 7G, the IC **700** includes via **772** formed on the M**0** layer and connected to a structure **782** formed in the M**1** layer. One terminal of the via **772** is formed on the conductive rail P**02**, and the other terminal of the via **772** is formed in the M**1** layer. With the operations discussed above, similar to configurations of the via **771**, a height of via **772** is substantially equal to or slightly greater than a distance between the conductive rail P**02** and the structure **782**.
[0113] In some embodiments, the via **772** is configured to couple between the conductive rail P**02** and the structure **782** formed in the M**1** layer. In various embodiments, the structure **782** is a power rail that is configured to providing power signals. In some other embodiments, the via **772** is coupled between the conductive rail P**02** and the power rail P**11**, and corresponds to the via **431** shown in FIG. **4** or **5**A.
[0114] As described above, the integrated circuit in the present disclosure is provided with conductive segments formed on the M**0** layer and is spaced apart from the M**1** layer. The conductive segment indicated as the V**0** rail is disposed on the power conductive rail, and the conductive segment indicated as the M**0** jumper is disposed on at least two signal conductive rails. Accordingly, routing between the M**0** layer and the M**1** layer is reduced, and resistances of the power conductive rails or the signal conductive rails are also reduced by additional arrangements of

the conductive segment.

[0115] The configuration of FIGS. **7**A-**7**G is given for illustrative purposes. Various configurations of the elements mentioned above in FIGS. **7**A-**7**G are within the contemplated scope of the present disclosure.

[0116] Reference is now made to FIG. **8**. FIG. **8** is a layout diagram **800** of an IC, in accordance with some embodiments of the present disclosure. The layout diagram **800** has configurations similar to that of the layout diagram **400** as illustrated in FIG. **4**, and similar detailed description is therefore omitted. The patterns shown in the layout diagram **800** with respect to the embodiments of FIG. **4**, like elements in FIG. **8** are designated with the same reference numbers for ease of understanding.

[0117] Compared to embodiments illustrated in FIG. **4**, the layout diagram **800** includes conductive segments **811** and **812** disposed on the conductive rails P**01** and P**02** respectively. The layout diagram **800** also includes conductive segment **821** disposed on and between the conductive rails S**02** and S**03**. The layout diagram **800** further includes vias **831**, **832** and **433** disposed between the M**0** layer and the M**1** layer. Specifically, in a layout view, the via **831** is overlapped with the conductive rail P**01**, the conductive segment **811** and the signal rail P**11**; the via **832** is overlapped with a conductive rail S**02**, the conductive rail S**03**, the conductive segment **821** and the signal rail S**11**; and the via **433** has similar configuration to that is shown in FIG. **4**.

[0118] In some embodiments, the conductive segment **811** corresponds to the conductive segment **411***a* or **411***b* shown in FIG. **4**. Compared to the conductive segment **411***a* or **411***b* of FIG. **4**, the conductive segment **811** is not separated into multiple portions. Similarly, the conductive segment **812** corresponds to the conductive segment **412***a* or **412***b* shown in FIG. **4**. In various embodiments, the conductive segment **811** has similar configuration/arrangement to the conductive segment **812**. In some other embodiments, the conductive segment **821** corresponds to the conductive segment **421** shown in FIG. **4**, and has similar configuration/arrangement to the conductive segment **421**.

[0119] Reference is now made to FIGS. **9**A to **9**C. FIG. **9**A is a cross-section schematic diagram of a layout diagram **900**A corresponding to the layout diagram **800** of FIG. **8**, taken along a line A-A′; FIG. **9**B is a cross-section schematic diagram of a layout diagram **900**B corresponding to the layout diagram **800** of FIG. **8**, taken along a line B-B′; and FIG. **9**C is a cross-section schematic diagram of a layout diagram **900**C corresponding to the layout diagram **800** of FIG. **8**, taken along a line C-C′, in accordance with some embodiments of the present disclosure. The layout diagram **900**A has configurations similar to that of the layout diagram **500**A as illustrated in FIG. **5**A; the layout diagram **900**B has configurations similar to that of the layout diagram **500**B as illustrated in FIG. **5**B; and the layout diagram **900**C has similar configuration/arrangement to the layout diagram **500**C shown in FIG. **5**C, and similar detailed description is therefore omitted. The layout diagrams **900**A to **900**C with respect to the embodiments of FIG. **8**, like elements in FIGS. **9**A to **9**C are designated with the same reference numbers for ease of understanding.

[0120] For illustration in FIG. **9**A, the conductive segment **811** is disposed on the conductive rail P**01**. The via **831** is disposed between the conductive segment **811** and the signal rail P**11** without extra spacing. The conductive segment **812** is disposed on the conductive rail P**02** and is spaced apart from the signal rail P**11**.

[0121] In some embodiments, the conductive rail P**01** is coupled to the conductive segment **811**, and is further coupled through the via **831** to the signal rail P**11**, for receiving the supply voltage signal with voltage VDD. With the above configurations, since the conductive segment **812** is separated from the signal rail P**11**, the conductive segment **812** or the conductive rail P**02** is not coupled to the signal rail P**11**.

[0122] For illustration in FIG. **9**B, the conductive segment **811** is disposed on the conductive rail P**01** and is spaced apart from the signal rail S**11**. The conductive segment **812** is disposed on the conductive rail P**02** and is spaced apart from the signal rail S**11**. The conductive segment **821** is disposed on two adjacent conductive rails S**02** and S**03**. In addition, the via **832** is disposed between the conductive segment **821** and the signal rail S**11** without extra spacing.

[0123] Compared to embodiments illustrated in FIG. **9**A, the layout diagram **900**B further illustrates conductive segments **911** and **912**, and vias **921** and **922**. In some embodiments, the conductive segments **911** and **912** correspond to the MD segments **511** and **512** in FIG. **5**B respectively, and the vias **921** and **922** correspond to the VD vias **521** and **522** in FIG. **5**B respectively. The conductive segments **911** and **912** are indicated as the MD segments hereinafter, and the vias **921** and **922** are indicated as the VD vias hereinafter.

[0124] With reference to FIG. **9**B, the VD via **921** is disposed between the MD segment **911** and the conductive rail S**01** without extra spacing. The VD via **922** is disposed between the MD segments **912** and the conductive rail S**03** without extra spacing.

[0125] In some embodiments, the MD segment **911** is coupled through the VD via **921** to the conductive rail S**01**. Furthermore, the MD segment **912** is coupled through the VD via **922** to the conductive rail S**03**. The conductive rail S**03** is further coupled to the conductive segment **821**, and is further coupled through the via **832** to the signal rail S**11**, for receiving the data signal provided to the conductive rail S**03** and further to the MD segment **912**. On the other hand, the conductive rail S**03** is also coupled through the conductive segment **821** to the conductive rail S**02**. Accordingly, the conductive rail S**02** is also configured to receive the data signal transmitted from the signal rail S**11**.

[0126] For illustration in FIG. **9**C, conductive segments **913** and **914**, and vias **923** and **924** are disposed below the conductive rails P**01**, P**02** and S**0**. In some embodiments, the conductive segments **913** and **914** correspond to the MD segments **513** and **514** in FIG. **5**C respectively, and the vias **923** and **924** correspond to the VD vias **523** and **524** in FIG. **5**C respectively.

[0127] Reference is now made to FIGS. **10**A to **10**C and back to FIG. **6**. FIGS. **10**A to **10**C are schematic diagrams, in cross-sectional view of part of the IC **1000** corresponding to the IC of FIG. **8** along the column direction as illustrated in FIG. **8**, illustrating some processes of the method of FIG. **6**, in accordance with some embodiments of the present disclosure. FIG. **10**A illustrates the operation S**650** in FIG. **6**, and has configurations similar to that is illustrated in FIG. **7**E. FIG. **10**B illustrates the operations S**660**-S**670** in FIG. **6**, and have configurations similar to that are illustrated in FIGS. **7**F and **7**G As such, similar detailed description is therefore omitted.

[0128] As illustrated in FIG. **10**A, a conductive segment **1051** is disposed on the part of the conductive rail S**03**, the film structure **720** and the part of the conductive rail S**04**, and is disposed on and above the M**0** layer. A conductive segment **1052** is disposed on the conductive rail P**02** and is disposed on and above the M**0** layer. Similar to the conductive segments **751** and **752** shown in FIG. **7**E, the conductive segments **1051** and **1052** and the film structure **720** form a substantially plat surface above the M**0** layer. In some embodiments, the conductive segments **1052** corresponds to at least one of the conductive segment **811** or **812** that contacts the conductive rail P**01** or P**02**, illustrated in FIG. **8**. In other embodiments, the conductive segments **1051** corresponds to the conductive segment **821** that contacts two adjacent conductive rails S**0**, illustrated in FIG. **8**.

[0129] For illustration of the operations shown in FIG. **6**, as shown in FIG. **10**A, the conductive rail P**02** corresponds to the first conductive rail, and the conductive segment **1052** corresponds to the first conductive segment that contacts the first conductive rail. With reference to the operation S**650** in FIG. **6** and FIG. **10**A, the dielectric structure **760** is formed and covers the conductive segment **1052**. The dielectric structure **760** also covers the conductive segment **1051**.

[0130] Regarding the operations S**660**-S**670** in FIG. **6** and FIG. **10**B, part of structures are removed and are filled with the conductive material, to form a via **771** and the structure **781** which corresponds to a signal rail, as discussed with reference to FIGS. **6** and **7**F-**7**G. The via **771** and the structure **781** correspond to the via **832** and the signal rail S**11** respectively, as shown in FIG. **8**, in some embodiments. As shown in FIG. **10**B, the via **771** is formed on the M**0** layer and is connected to the structure **781** formed in the M**1** layer, which is similar to the embodiments illustrated in FIG.

7F.

[0131] In some embodiments, the conductive segment **1051** is referred to as the M**0** jumper, and corresponds to the conductive segment **821** shown in FIG. **8** or **9**B. In some other embodiments, the conductive segment **1052** is referred to as the V**0** rail, and corresponds to the conductive segment **812** shown in FIG. **8** or **9**B. In various embodiments, the via **771** corresponds to the via **433** shown in FIG. **8** or **9**C.

[0132] In some embodiments, the method further includes the following operations. The dielectric structure is further patterned to form other patterns other than that are formed in the operation S**630**. These patterns are subsequently filled with the conductive material, to form a via that contacts the first conductive segment formed in the operation S**640**. Such via contacts the first conductive segment and a power rail disposed next to the second conductive rail. For illustration in FIG. **10**C, in some embodiments, the first conductive segment corresponds to the conductive segment **1052**, and the power rail corresponds to the structure **782** which corresponds to a power rail, thereby, the via corresponds to the via **1072** that contacts the first conductive segment and the power rail.

[0133] As shown in FIG. **10**C, a via **1072** is formed on the conductive segment **1052** and is connected to the structure **782** formed in the M**1** layer. One terminal of the via **1072** is formed on the conductive segment **1052**, and the other terminal of the via **1072** is formed in the M**1** layer. With the operations discussed above, a height of via **1072** is smaller than a distance between the conductive rail P**02** and the structure **782**. Also, a height of via **1072** is smaller than a height of via **771** shown in at least one of FIG. **7**F, **7**G or **10**B.

[0134] In some embodiments, the via **1072** is configured to couple between the conductive segment **1052** and the structure **782** formed in the M**1** layer. In various embodiments, the structure **782** is referred to as the power rail, for providing power signals. The conductive segment **1052** is referred to as the V**0** rail, and corresponds to the conductive segment **811** shown in FIG. **9**A. Also, the via **1072** corresponds to the via **831** shown in FIG. **9**A. Accordingly, the via **1072** is coupled between the conductive segment **1052** and the power rail P**11** shown in FIG. **8** or **9**A.

[0135] The configuration of FIGS. **10**A, **10**B, and **10**C is given for illustrative purposes. Various configurations of the elements mentioned above in FIGS. **10**A, **10**B, and **10**C are within the contemplated scope of the present disclosure.

[0136] To implement various devices, the layout diagrams as discussed above with respect to FIGS. **1**A, **1**B, **2**, **3**A to **3**C, **4**, **5**A to **5**C, **8** and **9**A to **9**C are used or modified to be used, as illustrated by the non-limiting examples discussed below with respect to FIGS. **11**A to **19**B. In the various embodiments discussed below, the IC of the present disclosure is implemented through the use of layout diagrams depicted in FIGS. **11**A, **12**A, **13**A, **14**A, **15**A, **16**A, **17**A, **18**A and **19**A that correspond to circuit diagrams depicted in FIGS. **11**B, **12**B, **13**B, **14**B, **15**B, **16**B, **17**B to **17**E, **18**B and **19**B, as indicated. To indicate correspondence between a given layout diagram feature formed based on the given layout diagram feature, a same reference designator is used in each of the layout diagram and structure depictions, as discussed below.

[0137] Reference is now made to FIG. **11**A. FIG. **11**A is a circuit diagram of an IC **1100**A, in accordance with some embodiments of the present disclosure. For illustration of the IC **1100**A, a gate terminal of a p-type metal oxide semiconductor (PMOS) transistor P**1** is coupled to a gate terminal of an n-type metal oxide semiconductor (NMOS) transistor N**1**. A source/drain terminal of the PMOS transistor P**1** is coupled to a source/drain terminal of a PMOS transistor P**2** at a node A**1**. A source/drain terminal of the NMOS transistor N**1** is coupled to a source/drain terminal of an NMOS transistor N**2** at a node B**1**. The node Al is further coupled to the node B**1** as indicated by connection ZA shown in FIG. **11**A. To implement the IC **1100**A including the connection ZA between the nodes A**1** and B**1** in the embodiments of the present disclosure, embodiments of layout designs and/or structures are provided and discussed below as illustrated with reference to FIG. **11**B.

[0138] In some embodiments, the IC **1100**A is used as a unit cell or unit circuit, in which the unit cell or unit circuit is capable of being used as a basic unit or as part of a device or circuit, in order to implement various devices or circuits. Alternatively stated, in some embodiments, the IC **1100**A is implemented in various devices or circuits, including, for example, an inverter, a NAND gate, an AND-OR-invert (AOI) logic gate, a flip-flop, or the like.

[0139] FIG. **11**B is a layout diagram **1100**B of an IC corresponding to the IC **1100**A of FIG. **11**A, in accordance with some embodiments of the present disclosure. For simplicity of illustration of the layout diagram **1100**B, it is merely illustrates a part of layout diagram for implement the IC **1100**A of FIG. **11**A.

[0140] In the illustration of FIG. **11**B, gates **1111**, **1112** and **1113** are arranged in an active area (not shown) and extend along the column direction. In some embodiments, the gates **1111**, **1112** and **1113** correspond to the gate segments **311** and **312** shown in FIGS. **3**A to **3**C. In various embodiments, the gates **1111**, **1112** and **1113** are patterned as “Poly” illustrated in FIG. **11**B. Conductive segments **1121**, **1122**, **1123**, **1124** and **1125** extend along the column direction and are referred to as MD segments hereinafter. In various embodiments, the conductive segments **1121**, **1122**, **1123**, **1124** and **1125** are patterned as “MD” illustrated in FIG. **11**B.

[0141] The MD segments **1121** and **1122** are arranged in the active area, as sources/drains of the PMOS transistor P**1** and P**2**. The gate **1112** and the MD segments **1121** and **1122** together correspond to the PMOS transistor P**1**. The gate **1113**, the MD segment **1122** and another MD segment (not shown) arranged next to the MD segment **1122** together correspond to the PMOS transistor P**2**. In such embodiments, the PMOS transistors P**1** and P**2** share the MD segment **1122**, which corresponds to the PMOS transistors P**1** and P**2** being coupled at the node A**1** as discussed above with respect to FIG. **11**A. The MD segments **1123**, **1124** and **1125** are arranged in the active area, as sources/drains of the NMOS transistor N**1** and N**2**. The gate **1111** and the MD segments **1123** and **1124** together correspond to the NMOS transistor N**1**. The gate **1112** and the MD segments **1124** and **1125** together correspond to the NMOS transistor N**2**. In such embodiments, the NMOS transistors N**1** and N**2** share the MD segment **1124**, which corresponds to the NMOS transistors N**1** and N**2** being coupled at the node B**1** as discussed above with respect to FIG. **11**A.

[0142] Vias **1131** and **1132** are arranged between the active area and the M**0** layer. In various embodiments, the vias **1131** and **1132** are patterned as “VD” illustrated in FIG. **11**B. The vias **1131** and **1132** are also referred to as VD vias hereinafter, which are discussed above at least with reference to FIG. **5**B, for coupling between the MD segments **1121-1125** in the active area and conductive rails **1141-1143** in the M**0** layer. In the illustration of FIG. **11**B, the VD via **1131** is arranged between the MD segment **1122** and the conductive rail **1141**, and the VD via **1132** is arranged between the MD segment **1124** and the conductive rail **1142**. The VD via **1131** couples the MD segment **1122** to the conductive rail **1141**. The VD via **1132** couples the MD segment **1124** to the conductive rail **1142**.

[0143] In some embodiments, the layout diagram **1100**B further includes a data rail (not shown) arranged in the M**1** layer above the M**0** layer, and the data rail extends in the column direction and is coupled to the conductive rail **1141**. With such configuration, a data signal provided from the data rail is transmitted through the conductive rail **1141**, and is further transmitted through the via **1131** to the MD segment **1122**. In such embodiments, the node Al as discussed above with respect to FIG. **11**A is further coupled to the data rail, for receiving the data signal at the node A**1**.

[0144] The Conductive rails **1141**, **1142** and **1143** are arranged in the M**0** layer which is above the active area and extend along the row direction. In some embodiments, the conductive rails **1141**, **1142** and **1143** are patterned as “M**0**” illustrated in FIG. **11**B. In some other embodiments, the conductive rails **1141**, **1142** and **1143** are also referred to as signal conductive rails which are discussed above at least with reference to FIG. **4**.

[0145] A conductive segment **1151** is arranged in the M**0** layer, and is arranged below the MI layer. In various embodiments, the conductive segment **1151** is patterned as “M**01**” illustrated in FIG.

11B. The conductive segment **1151** is shaped as a block and is also referred to as the M**0** jumper corresponding to the conductive segments **121-124** as illustrated in FIGS. **3**A-**3**C, in some embodiments. In a layout view, the conductive segment **1151** is partially overlapped with the conductive rails **1141** and **1142**, the gate **1111** and the VD via **1132**. The conductive segment **1151** couples the conductive rails **1141** and **1142** together. Accordingly, the MD segment **1122** is coupled through the VD via **1131** to the conductive rail **1141**, and the conductive rail **1141** is further coupled through the conductive segment **1151** to the conductive rail **1142**. The conductive rail **1142** is coupled through the VD via **1132** to the MD segment **1124**. With the above configurations, the MD segments **1122** and **1124** together are coupled to the conductive segment **1151**, which corresponds to the nodes A**1** and B**1** being coupled between the connection ZA as discussed above with respect to FIG. **11**A.

[0146] Reference is now made to FIG. **12**A. FIG. **12**A is a circuit diagram of an IC **1200**A, in accordance with some embodiments of the present disclosure. For illustration of the IC **1200**A, a gate terminal of a PMOS transistor P**1** is coupled to a gate terminal of a NMOS transistor N**1**; a gate terminal of a PMOS transistor P**2** is coupled to a gate terminal of a NMOS transistor N**2**; a gate terminal of a PMOS transistor P**3** is coupled to a gate terminal of a NMOS transistor N**3**; and a gate terminal of a PMOS transistor P**4** is coupled to a gate terminal of a NMOS transistor N**4**.

[0147] A source/drain terminal of the PMOS transistor P**1** is coupled to a node A**1**; a source/drain terminal of the PMOS transistor P**1** is coupled to a source/drain terminal of the PMOS transistor P**2** at a node A**2**; a source/drain terminal of the PMOS transistor P**2** is coupled to a source/drain terminal of the PMOS transistor P**3** at a node A**3**; a source/drain terminal of the PMOS transistor P**3** is coupled to a source/drain terminal of the PMOS transistor P**4** at a node A**4**; and a source/drain terminal of the PMOS transistor P**4** is coupled to a node A**5** which is further coupled to the nodes A**1** and A**3**.

[0148] Furthermore, a source/drain terminal of the NMOS transistor N**1** is coupled to a node B**1**; a source/drain terminal of the NMOS transistor N**1** is coupled to a source/drain terminal of a NMOS transistor N**2**; a source/drain terminal of the NMOS transistor N**2** is coupled to a source/drain terminal of a NMOS transistor N**3** at a node B**2**; a source/drain terminal of the NMOS transistor N**3** is coupled to a source/drain terminal of a NMOS transistor N**4**; and a source/drain terminal of the NMOS transistor N**4** is coupled to a node B**3**. The node A**3** is further coupled to a power rail referenced as VDD. Each of the nodes B**1** and B**3** is further coupled to another power rail referenced as VSS, and a voltage of the power rail VSS is lower than that of the power rail VDD. The node A**4** is further coupled to the node B**2** as indicated by connection ZN shown in FIG. **12**A. To implement the IC **1200**A including the connection ZN between the nodes A**4** and B**2** in the embodiments of the present disclosure, embodiments of layout designs and/or structures are provided and discussed below as illustrated with reference to FIG. **12**B.

[0149] FIG. **12**B is a layout diagram **1200**B of an IC corresponding to the IC **1200**A of FIG. **12**A, in accordance with some embodiments of the present disclosure.

[0150] In the illustration of FIG. **12**B, gates **1211**, **1212**, **1213** and **1214** are arranged as gate terminals of PMOS transistors P**1**-P**4** or NMOS transistors N**1**-N**4** in FIG. **12**A. MD segments **1220**, **1221**, **1222**, **1223**, **1224**, **1225**, **1226**, **1227**, **1228** and **1229** are arranged as sources/drains of PMOS transistors P**1**-P**4** or NMOS transistors N**1**-N**4** in FIG. **12**A.

[0151] The gate **1211** and the MD segments **1220** and **1221** together correspond to the PMOS transistor P**1**. The gate **1212** and the MD segments **1221** and **1222** together correspond to the PMOS transistor P**2**. The gate **1213** and the MD segments **1222** and **1223** together correspond to the PMOS transistor P**3**. The gate **1214** and the MD segments **1223** and **1224** together correspond to the PMOS transistor P**4**. In such embodiments, the PMOS transistors P**1** and P**2** share the MD segment **1221**, which corresponds to the PMOS transistors P**1** and P**2** being coupled at the node A**2** illustrated in FIG. **12**A. The PMOS transistors P**2** and P**3** share the MD segment **1222**, which corresponds to the PMOS transistors P**2** and P**3** being coupled at the node A**3** illustrated in FIG.

12A. The PMOS transistors P3 and P4 share the MD segment 1223, which corresponds to the PMOS transistors P3 and P4 being coupled at the node A4 illustrated in FIG. 12A.

[0152] Furthermore, the gate 1211 and the MD segments 1225 and 1226 together correspond to the NMOS transistor N1. The gate 1212 and the MD segments 1226 and 1227 together correspond to the NMOS transistor N2. The gate 1213 and the MD segments 1227 and 1228 together correspond to the NMOS transistor N3. The gate 1214 and the MD segments 1228 and 1229 together correspond to the NMOS transistor N4. In such embodiments, the NMOS transistors N2 and N3 share the MD segment 1227, which corresponds to the NMOS transistors N2 and N3 being coupled at the node B2 illustrated in FIG. 12A.

[0153] Conductive rails 1241, 1242, 1243, 1244, 1245, 1246, 1247, 1248 and 1249 are arranged. The conductive rails 1242, 1243, 1244, 1245, 1246, 1248 and 1249 are arranged between the conductive rails 1241 and 1247. A width of the conductive rails 1242, 1243, 1244, 1245, 1246, 1248 or 1249 is smaller than a width of the conductive rails 1241 or 1247. In some embodiments, the conductive rails 1242, 1243, 1244, 1245, 1246, 1248 and 1249 are referred to as the signal conductive rails, and the conductive rails 1241 and 1247 are referred to as the power conductive rails, which are discussed above at least with reference to FIG. 4.

[0154] VD vias 1231, 1232, 1233, 1234, 1235, 1236, 1237 and 1238 are arranged. The VD via 1231 couples the MD segment 1220 to the conductive rail 1242. The VD via 1232 couples the MD segment 1221 to the conductive rail 1241 which is further coupled to a power rail (not shown) arranged in the M1 layer. The MD segment 1221 and the conductive rail 1241 together are coupled to the power rail, which corresponds to the node A3 being coupled to the power rail VDD as discussed above with respect to FIG. 12A. The VD via 1233 couples the MD segment 1222 to the conductive rail 1242. The VD via 1234 couples the MD segment 1223 to the conductive rail 1244. The VD via 1235 couples the MD segment 1224 to the conductive rail 1242. With such configurations, the MD segments 1220, 1222 and 1224 are coupled together, which corresponds to the nodes A1, A3 and A5 being coupled together as discussed above with respect to FIG. 12A.

[0155] Moreover, the VD via 1236 couples the MD segment 1225 to the conductive rail 1247 which is further coupled to another power rail (not shown) arranged in the M1 layer. The MD segment 1225 and the conductive rail 1247 together are coupled to the power rail, which corresponds to the node B1 being coupled to the power rail VSS as discussed above with respect to FIG. 12A. The VD via 1237 couples the MD segment 1227 to the conductive rail 1245. The VD via 1238 couples the MD segment 1229 to the conductive rail 1247 which is further coupled to the power rail as same as that is coupled to the MD segment 1225. The MD segment 1229 and the conductive rail 1247 together are coupled to the power rail, which corresponds to the node B3 being coupled to the power rail VSS as discussed above with respect to FIG. 12A.

[0156] VG vias 1251, 1252, 1253 and 1254 are arranged. The VG via 1251 couples the gate 1211 to the conductive rail 1243. The VG via 1252 couples the gate 1212 to the conductive rail 1246. The VG via 1253 couples the gate 1213 to the conductive rail 1249. The VG via 1254 couples the gate 1214 to the conductive rail 1248.

[0157] Conductive segments 1261, 1262 and 1263 are arranged. The conductive segment 1261 is also referred to as the M0 jumper, and corresponds to the conductive segment 121, 122 or 123 as illustrated in FIG. 3A or 3C, in some embodiments. The conductive segment 1261 couples the conductive rails 1244 and 1245 together. With such configurations, the MD segments 1223 and 1227 are coupled together, which corresponds to the nodes A4 and B2 being coupled between the connection ZN as discussed above with respect to FIG. 12A.

[0158] Moreover, the conductive segments 1262 and 1263 are also referred to as the V0 rails, and correspond to the conductive segments 111 and 112 as illustrated in FIGS. 3A-3C, in some embodiments. As discussed above with reference to the VD vias 1231-1238, the conductive segment 1262 couples to both of the conductive rail 1241 and the MD segment 1221, which is further coupled to the power rail VDD. The conductive segment 1263 couples to both of the conductive rail **1247** and the MD segments **1225** and **1229**, which is further coupled to the power rail VSS.

[0159] Reference is now made to FIG. **13**A. FIG. **13**A is a circuit diagram of an IC **1300**A, in accordance with some embodiments of the present disclosure. In some embodiments, the IC **1300**A is used as one unit cell/circuit for implementing two different logic functions, which is also indicated as a two stage cell. For illustration of the IC **1300**A, a gate terminal of a PMOS transistor P**1** is coupled to a gate terminal of a NMOS transistor N**1** at a node E**1**; a gate terminal of a PMOS transistor P**2** is coupled to a gate terminal of a NMOS transistor N**2**; and a gate terminal of a PMOS transistor P**3** is coupled to a gate terminal of a NMOS transistor N**3**.

[0160] Furthermore, a source/drain terminal of the PMOS transistor P**1** is coupled to a node A**1**; a source/drain terminal of the PMOS transistor P**1** is coupled to a source/drain terminal of a PMOS transistor P**2** at a node A**2**; a source/drain terminal of the PMOS transistor P**2** is coupled to a source/drain terminal of a PMOS transistor P**3** at a node A**3**; a source/drain terminal of the PMOS transistor P**3** is coupled to a node A**4**. A source/drain terminal of the NMOS transistor N**1** is coupled to a node B**1**; a source/drain terminal of the NMOS transistor N**1** is coupled to a source/drain terminal of a NMOS transistor N**2** at a node B**2**; a source/drain terminal of the NMOS transistor N**2** is coupled to a source/drain terminal of a NMOS transistor N**3**; and a source/drain terminal of the NMOS transistor N**3** is coupled to a node B**3**. The nodes A**2** and A**4** are further coupled to a power rail referenced as VDD. The nodes B**2** is further coupled to another power rail referenced as VSS. With reference to FIG. **13**A, the node A**1** is further coupled to the node B**1** as indicated by connection Z. The node A**3** is further coupled to the node E**1** at a node E**2** as indicated by connection ZE. The node A**3** is also further coupled to the node B**3** as indicated by connection ZN. To implement the IC **1300**A including the connection Z between the nodes A**1** and B**1**, the connection ZE between the nodes E**1** and E**2**, and connection ZN between the nodes A**3** and B**3** in the embodiments of the present disclosure, embodiments of layout designs and/or structures are provided and discussed below as illustrated with reference to FIG. **13**B.

[0161] FIG. **13**B is a layout diagram **1300**B of an IC corresponding to the IC **1300**A of FIG. **13**A, in accordance with some embodiments of the present disclosure.

[0162] In the illustration of FIG. **13**B, gates **1311**, **1312** and **1313** are arranged as gate terminals of PMOS transistors P**1**-P**3** or NMOS transistors N**1**-N**3** in FIG. **13**A. MD segments **1321**, **1322**, **1323**, **1324**, **1325**, **1326** and **1327** are arranged as sources/drains of PMOS transistors P**1**-P**3** or NMOS transistors N**1**-N**3** in FIG. **13**A.

[0163] The gate **1311** and the MD segments **1321** and **1322** together correspond to the PMOS transistor P**1**. The gate **1312** and the MD segments **1322** and **1333** together correspond to the PMOS transistor P**2**. The gate **1313** and the MD segments **1323** and **1324** together correspond to the PMOS transistor P**3**. In such embodiments, the PMOS transistors P**1** and P**2** share the MD segment **1322**, which corresponds to the PMOS transistors P**1** and P**2** being coupled at the node A**2** illustrated in FIG. **13**A. The PMOS transistors P**2** and P**3** share the MD segment **1323**, which corresponds to the PMOS transistors P**2** and P**3** being coupled at the node A**3** illustrated in FIG. **13**A.

[0164] Furthermore, the gate **1311** and the MD segments **1321** and **1325** together correspond to the NMOS transistor N**1**. The gate **1312** and the MD segments **1325** and **1326** together correspond to the NMOS transistor N**2**. The gate **1313** and the MD segments **1326** and **1327** together correspond to the NMOS transistor N**3**. In such embodiments, the NMOS transistors N**1** and N**2** share the MD segment **1325**, which corresponds to the NMOS transistors N**1** and N**2** being coupled at the node B**2** illustrated in FIG. **13**A. The PMOS transistor P**1** and the NMOS transistor N**1** share the MD segment **1321**, which corresponds to the PMOS transistor P**1** and the NMOS transistor N**1** coupled at the nodes A**1** and B**1** together. It also corresponds to the nodes A**1** and B**1** being coupled between the connection Z illustrated in FIG. **13**A.

[0165] Conductive rails **1341**, **1342**, **1343**, **1344**, **1345**, **1346** and **1347** are arranged. In some embodiments, the conductive rails **1342**, **1343**, **1344**, **1345** and **1346** are referred to as the signal conductive rails, and the conductive rails **1341** and **1347** are referred to as the power conductive rails, which are discussed above at least with reference to FIG. **4**.

[0166] VD vias **1331**, **1332**, **1333**, **1334**, **1335** and **1336** are arranged. The VD via **1331** couples the MD segment **1321** to the conductive rail **1344**. The VD via **1332** couples the MD segment **1322** to the conductive rail **1341** which is further coupled to a power rail (not shown) arranged in the M**1** layer. The MD segment **1322** and the conductive rail **1341** together are coupled to the power rail, which corresponds to the node A**2** being coupled to the power rail VDD as discussed above with respect to FIG. **13**A. The VD via **1333** couples the MD segment **1323** to the conductive rail **1343**. The VD via **1334** couples the MD segment **1324** to the conductive rail **1341**. Similarly, the MD segment **1324** and the conductive rail **1341** together are coupled to the power rail, which corresponds to the node A**4** being coupled to the power rail VDD as discussed above with respect to FIG. **13**A. The VD via **1335** couples the MD segment **1325** to the conductive rail **1347** which is further coupled to another power rail (not shown) arranged in the M**1** layer. The MD segment **1325** and the conductive rail **1347** together are coupled to the power rail, which corresponds to the node B**2** being coupled to the power rail VSS as discussed above with respect to FIG. **13**A. The VD via **1336** couples the MD segment **1327** to the conductive rail **1346**.

[0167] VG vias **1351**, **1352** and **1353** are arranged. The VG via **1351** couples the gate **1311** to the conductive rail **1343**. With such configurations, the gate **1311** is further coupled through the conductive rail **1343** to the MD segment **1323**, which corresponds to the nodes E**1** and A**3** being coupled between the connection ZE as discussed above with respect to FIG. **13**A. The VG via **1352** couples the gate **1312** to the conductive rail **1345**. The VG via **1353** couples the gate **1313** to the conductive rail **1342**.

[0168] Conductive segments **1361**, **1362** and **1363** are arranged. The conductive segment **1361** is also referred to as the M**0** jumper, and corresponds to the conductive segment **121**, **122** or **123** as illustrated in FIG. **3**A or **3**C, in some embodiments. The conductive segment **1361** couples the conductive rails **1343** and **1346** together. With such configurations, the MD segments **1323** and **1327** are coupled together, which corresponds to the nodes A**3** and B**3** being coupled between the connection ZN as discussed above with respect to FIG. **13**A.

[0169] Moreover, the conductive segments **1362** and **1363** are also referred to as the V**0** rails, and correspond to the conductive segments **111** and **112** as illustrated in FIGS. **3**A-**3**C, in some embodiments. As discussed above with reference to the VD vias **1331**-**1336**, the conductive segment **1362** couples to both of the conductive rail **1341** and the MD segments **1322** and **1324**, which is further coupled to the power rail VDD. The conductive segment **1263** couples to both of the conductive rail **1347** and the MD segment **1325**, which is further coupled to the power rail VSS.

[0170] Reference is now made to FIG. **14**A. FIG. **14**A is a circuit diagram of an IC **1400**A, in accordance with some embodiments of the present disclosure. For illustration of the IC **1400**A, a gate terminal of a PMOS transistor P**1** is coupled to a gate terminal of a NMOS transistor N**1** as indicated by connection I. In some embodiments, the connection I is indicated as an input terminal, for providing a control signal to both of the PMOS transistor P**1** and the NMOS transistor N**1**.

[0171] Furthermore, a source/drain terminal of the PMOS transistor P**1** is coupled to a node A**1**. A source/drain terminal of the PMOS transistor P**1** is coupled to a node A**2**. A source/drain terminal of the NMOS transistor N**1** is coupled to a node B**1**. A source/drain terminal of the NMOS transistor N**2** is coupled to a node B**2**. The nodes A**1** is further coupled to a power rail referenced as VDD. The nodes B**1** is further coupled to another power rail referenced as VSS. The node A**2** is further coupled to the node B**2** as indicated by connection ZN. To implement the IC **1400**A including the connection ZN between the nodes A**2** and B**2** in the embodiments of the present disclosure, embodiments of layout designs and/or structures are provided and discussed below as illustrated with reference to FIG. **14**B.

[0172] FIG. **14**B is a layout diagram **1400**B of an IC corresponding to the IC **1400**A of FIG. **14**A, in accordance with some embodiments of the present disclosure.

[0173] In the illustration of FIG. **14**B, a gate **1411** is arranged as the gate terminal of PMOS transistor P**1** and NMOS transistor N**1** in FIG. **14**A. MD segments **1421**, **1422** and **1423** are arranged as sources/drains of PMOS transistor P**1** or NMOS transistor N**1** in FIG. **14**A.

[0174] The gate **1411** and the MD segments **1421** and **1422** together correspond to the PMOS transistor P**1**. The gate **1411** and the MD segments **1423** and **1422** together correspond to the NMOS transistor N**1**. In such embodiments, the PMOS transistor P**1** share the MD segment **1422**, which corresponds to the PMOS transistor P**1** being coupled at the nodes A**2** and B**2** together illustrated in FIG. **14**A. It also corresponds to the nodes A**2** and B**2** being coupled between the connection ZN illustrated in FIG. **14**A.

[0175] Conductive rails **1441**, **1442**, **1443**, **1444**, **1445** and **1446** are arranged. In some embodiments, the conductive rails **1442**, **1443**, **1444** and **1445** are referred to as the signal conductive rails, and the conductive rails **1441** and **1446** are referred to as the power conductive rails, which are discussed above at least with reference to FIG. **4**.

[0176] VD vias **1431**, **1432** and **1433** are arranged. The VD via **1431** couples the MD segment **1421** to the conductive rail **1441** which is further coupled to a power rail (not shown) arranged in the M**1** layer. The MD segment **1421** and the conductive rail **1441** together are coupled to the power rail, which corresponds to the node A**1** being coupled to the power rail VDD as discussed above with respect to FIG. **14**A. The VD via **1432** couples the MD segment **1422** to the conductive rail **1444**. The VD via **1433** couples the MD segment **1423** to the conductive rail **1446** which is further coupled to another power rail (not shown) arranged in the M**1** layer. The MD segment **1423** and the conductive rail **1446** together are coupled to the power rail, which corresponds to the node B**1** being coupled to the power rail VSS as discussed above with respect to FIG. **14**A.

[0177] VG via **1451** is arranged. The VG via **1451** couples the gate **1411** to the conductive rail **1445** which is further coupled to a signal rail (not shown) arranged in the M**1** layer. The gate **1411** and the conductive rail **1445** together are coupled to the signal rail, which corresponds to the gate of the PMOS transistor P**1** or NMOS transistor N**1** being coupled between the connection I as discussed above with respect to FIG. **14**A.

[0178] Conductive segments **1461**, **1462** and **1463** are arranged. The conductive segment **1461** is also referred to as the M**0** jumper, and corresponds to the conductive segment **121**, **122** or **123** as illustrated in FIG. **3**A or **3**C, in some embodiments. The conductive segment **1461** couples the conductive rails **1443** and **1444** together.

[0179] Moreover, the conductive segments **1462** and **1463** are also referred to as the V**0** rails, and correspond to the conductive segments **111** and **112** as illustrated in FIGS. **3**A-**3**C, in some embodiments. As discussed above with reference to the VD vias **1431-1433**, the conductive segment **1462** couples to both of the conductive rail **1441** and the MD segment **1421**, which is further coupled to the power rail VDD. The conductive segment **1463** couples to both of the conductive rail **1446** and the MD segment **1423**, which is further coupled to the power rail VSS.

[0180] Reference is now made to FIG. **15**A. FIG. **15**A is a circuit diagram of an IC **1500**A, in accordance with some embodiments of the present disclosure. For illustration of the IC **1500**A, a gate terminal of a PMOS transistor P**1** is coupled to a gate terminal of a NMOS transistor N**1** as indicated by connection I. A gate terminal of a PMOS transistor P**2** is coupled to a gate terminal of a NMOS transistor N**2** as also indicated by the connection I. In some embodiments, the connection I has a similar configuration/arrangement to the connection I illustrated in FIG. **14**A.

[0181] Furthermore, a source/drain terminal of the PMOS transistor P**1** is coupled to a node A**1**; a source/drain terminal of the PMOS transistor P**1** is coupled to a source/drain terminal of a PMOS transistor P**2** at a node A**2**; and a source/drain terminal of the PMOS transistor P**2** is coupled to a node A**3**. A source/drain terminal of the NMOS transistor N**1** is coupled to a node B**1**; a source/drain terminal of the NMOS transistor N**1** is coupled to a source/drain terminal of a NMOS transistor N**2** at node B**2**; and a source/drain terminal of the NMOS transistor N**2** is coupled to a node B**3**. The nodes A**1** and A**3** are further coupled to a power rail referenced as VDD. The nodes B**1** and B**3** are further coupled to another power rail referenced as VSS. The node A**2** is further coupled to the node B**2** as indicated by connection ZN shown in FIG. **15**A. To implement the IC **1500**A including the connection ZN between the nodes A**2** and B**2** in the embodiments of the present disclosure, embodiments of layout designs and/or structures are provided and discussed below as illustrated with reference to FIG. **15**B.

[0182] FIG. **15**B is a layout diagram **1500**B of an IC corresponding to the IC **1500**A of FIG. **15**A, in accordance with some embodiments of the present disclosure.

[0183] In the illustration of FIG. **15**B, gates **1511** and **1512** are arranged as gate terminals of PMOS transistors P**1**-P**2** or NMOS transistors N**1**-N**2** in FIG. **15**A. MD segments **1521**, **1522**, **1523**, **1524** and **1525** are arranged as source/drain terminals of PMOS transistors P**1**-P**2** or NMOS transistors N**1**-N**2** in FIG. **15**A.

[0184] The gate **1511** and the MD segments **1521** and **1522** together correspond to the PMOS transistor P**1**. The gate **1512** and the MD segments **1522** and **1523** together correspond to the PMOS transistor P**2**. In such embodiments, the PMOS transistors P**1** and P**2** share the MD segment **1522**, which corresponds to the PMOS transistors P**1** and P**2** being coupled at the node A**2** illustrated in FIG. **15**A. The gate **1511** and the MD segments **1524** and **1522** together correspond to the NMOS transistor N**1**. The gate **1512** and the MD segments **1522** and **1525** together correspond to the NMOS transistor N**2**. In such embodiments, the NMOS transistors N**1** and N**2** share the MD segment **1522**, which corresponds to the NMOS transistors N**1** and N**2** being coupled at the node B**2** illustrated in FIG. **15**A. Also, the NMOS transistor N**1**/N**2** and the PMOS transistor P**1**/P**2** share the MD segment **1522**, which corresponds to the nodes A**2** and B**2** being coupled between the connection ZN illustrated in FIG. **15**A.

[0185] Conductive rails **1541**, **1542**, **1543**, **1544**, **1545** and **1546** are arranged. In some embodiments, the conductive rails **1542**, **1543**, **1544** and **1545** are referred to as the signal conductive rails, and the conductive rails **1541** and **1546** are referred to as the power conductive rails, which are discussed above at least with reference to FIG. **4**.

[0186] VD vias **1531**, **1532**, **1533**, **1534** and **1535** are arranged. The VD via **1531** couples the MD segment **1521** to the conductive rail **1541** which is further coupled to a power rail (not shown) arranged in the M**1** layer. The MD segment **1521** and the conductive rail **1541** together are coupled to the power rail, which corresponds to the node Al being coupled to the power rail VDD as discussed above with respect to FIG. **15**A. The VD via **1532** couples the MD segment **1522** to the conductive rail **1543**. The VD via **1533** couples the MD segment **1523** to the conductive rail **1541**. Similarly, the MD segment **1523** and the conductive rail **1541** together are coupled to the power rail, which corresponds to the node A**3** being coupled to the power rail VDD as discussed above with respect to FIG. **15**A.

[0187] Moreover, the VD via **1534** couples the MD segment **1524** to the conductive rail **1546** which is further coupled to another power rail (not shown) arranged in the M**1** layer. The MD segment **1524** and the conductive rail **1546** together are coupled to the power rail, which corresponds to the node B**1** being coupled to the power rail VSS as discussed above with respect to FIG. **15**A. The VD via **1535** couples the MD segment **1525** to the conductive rail **1546**. Similarly, the MD segment **1525** and the conductive rail **1546** together are coupled to the power rail, which corresponds to the node B**3** being coupled to the power rail VSS as discussed above with respect to FIG. **15**A.

[0188] VG vias **1551** and **1552** are arranged. The VG via **1551** couples the gate **1511** to the conductive rail **1545** which is further coupled to a signal rail (not shown) arranged in the M**1** layer. Also, the VG via **1552** couples the gate **1512** to the conductive rail **1545**. The gate **1511** and the conductive rail **1545** together are coupled to the signal rail, which corresponds to the gate of the PMOS transistor P**1** or NMOS transistor N**1** being coupled between the connection I as discussed above with respect to FIG. **15**A. Similarly, the gate **1512** and the conductive rail **1545** together are coupled to the same signal rail that is also coupled to the gate **1511**, which corresponds to the gate of the PMOS transistor P**2** or NMOS transistor N**2** being coupled between the connection that is also indicated as the connection I.

[0189] Conductive segments **1561**, **1562** and **1563** are arranged. The conductive segment **1561** is also referred to as the M**0** jumper, and corresponds to the conductive segment **124** as illustrated in FIG. **3**B or **3**C, in some embodiments. The conductive segment **1561** couples the conductive rails **1542** and **1543** together.

[0190] Moreover, the conductive segments **1562** and **1563** are also referred to as the V**0** rails, and correspond to the conductive segments **111** and **112** as illustrated in FIGS. **3**A-**3**C, in some embodiments. As discussed above with reference to the VD vias **1531**-**1535**, the conductive segment **1562** couples to both of the conductive rail **1541** and the MD segments **1521** and **1523**, which is further coupled to the power rail VDD. The conductive segment **1563** couples to both of the conductive rail **1546** and the MD segments **1524** and **1525**, which is further coupled to the power rail VSS.

[0191] Reference is now made to FIG. **16**A. FIG. **16**A is a circuit diagram of an IC **1600**A, in accordance with some embodiments of the present disclosure. For illustration of the IC **1600**A, a gate terminal of a PMOS transistor P**1** is coupled to a gate terminal of a NMOS transistor N**1** as indicated by connection I**1**. A gate terminal of a PMOS transistor P**2** is coupled to a gate terminal of a NMOS transistor N**2** as indicated by connection I**2**; and a gate terminal of a PMOS transistor P**3** is coupled to a gate terminal of a NMOS transistor N**3** as indicated by connection I**3**. In some embodiments, the connection I**1**, I**2** or I**3** has a similar configuration/arrangement to the connection I illustrated in FIG. **14**A. In some other embodiments, the connections I**1**, I**2** and I**3** are further coupled to signal rails (not shown) that are different from one another, for transmitting different data signals. For example, the connection I**1** is coupled to a first signal rail; the connection I**2** is coupled to a second signal rail; and the connection I**3** is coupled to a third signal rail.

[0192] Furthermore, a source/drain terminal of the PMOS transistor P**1** is coupled to a node A**1**; a source/drain terminal of the PMOS transistor P**1** is coupled to a source/drain terminal of a PMOS transistor P**2** at a node A**2**; a source/drain terminal of the PMOS transistor P**2** is coupled to a source/drain terminal of a PMOS transistor P**3** at a node A**3**. A source/drain terminal of the PMOS transistor P**3** is coupled to a node A**4**. A source/drain terminal of the NMOS transistor N**1** is coupled to a node B**1**; a source/drain terminal of the NMOS transistor N**1** is coupled to a source/drain terminal of a NMOS transistor N**2**; a source/drain terminal of the NMOS transistor N**2** is coupled to a source/drain terminal of a NMOS transistor N**3**; and a source/drain terminal of the NMOS transistor N**3** is coupled to a node B**2**. The nodes A**1** and A**3** are further coupled to a power rail referenced as VDD. The node B**2** is further coupled to another power rail referenced as VSS. The node A**2** is further coupled to the node A**4**. The node A**2** is further coupled to the node B**1** as indicated by connection ZN shown in FIG. **16**A. To implement the IC **1600**A including the connection ZN between the nodes A**2** and B**1** in the embodiments of the present disclosure, embodiments of layout designs and/or structures are provided and discussed below as illustrated with reference to FIG. **16**B.

[0193] FIG. **16**B is a layout diagram **1600**B of an IC corresponding to the IC **1600**A of FIG. **16**A, in accordance with some embodiments of the present disclosure.

[0194] In the illustration of FIG. **16**B, gates **1611**, **1612** and **1613** are arranged as gate terminals of PMOS transistors P**1**-P**3** or NMOS transistors N**1**-N**3** in FIG. **16**A. MD segments **1621**, **1622**, **1623**, **1624**, **1625**, **1626**, **1627** and **1628** are arranged as source/drain terminals of PMOS transistors P**1**-P**3** or NMOS transistors N**1**-N**3** in FIG. **16**A.

[0195] The gate **1611** and the MD segments **1621** and **1622** together correspond to the PMOS transistor P**1**. The gate **1612** and the MD segments **1622** and **1623** together correspond to the PMOS transistor P**2**. In such embodiments, the PMOS transistors P**1** and P**2** share the MD segment

1622, which corresponds to the PMOS transistors P**1** and P**2** being coupled at the node A**2** illustrated in FIG. **16**A. The gate **1613** and the MD segments **1623** and **1624** together correspond to the PMOS transistor P**3**. In such embodiments, the PMOS transistors P**2** and P**3** share the MD segment **1623**, which corresponds to the PMOS transistors P**2** and P**3** being coupled at the node A**3** illustrated in FIG. **16**A. The gate **1611** and the MD segments **1625** and **1626** together correspond to the NMOS transistor N**1**. The gate **1612** and the MD segments **1626** and **1627** together correspond to the NMOS transistor N**2**. The gate **1613** and the MD segments **1627** and **1628** together correspond to the NMOS transistor N**3**.

[0196] Conductive rails **1641**, **1642**, **1643**, **1644**, **1645**, **1646** and **1647** are arranged. In some embodiments, the conductive rails **1642**, **1643**, **1644**, **1645** and **1646** are referred to as the signal conductive rails, and the conductive rails **1641** and **1647** are referred to as the power conductive rails, which are discussed above at least with reference to FIG. **4**.

[0197] VD vias **1631**, **1632**, **1633**, **1634**, **1635** and **1636** are arranged. The VD via **1631** couples the MD segment **1621** to the conductive rail **1641** which is further coupled to a power rail (not shown) arranged in the M**1** layer. The MD segment **1621** and the conductive rail **1641** together are coupled to the power rail, which corresponds to the node A**1** being coupled to the power rail VDD as discussed above with respect to FIG. **16**A. The VD via **1632** couples the MD segment **1622** to the conductive rail **1643**. The VD via **1633** couples the MD segment **1623** to the conductive rail **1641** which is further coupled to the power rail. Similarly, the MD segment **1623** and the conductive rail **1641** together are coupled to the power rail, which corresponds to the node A**3** being coupled to the power rail VDD as discussed above with respect to FIG. **16**A. The VD via **1634** couples the MD segment **1624** to the conductive rail **1643**. With such configurations, the MD segments **1622**, and **1624** are coupled together, which corresponds to the nodes A**2** and A**4** being coupled together as discussed above with respect to FIG. **16**A.

[0198] Furthermore, the VD via **1635** couples the MD segment **1625** to the conductive rail **1644**. The VD via **1636** couples the MD segment **1628** to the conductive rail **1647** which is further coupled to another power rail (not shown) arranged in the M**1** layer. The MD segment **1628** and the conductive rail **1647** together are coupled to the power rail, which corresponds to the node B**2** being coupled to the power rail VSS as discussed above with respect to FIG. **16**A.

[0199] VG vias **1651**, **1652** and **1653** are arranged. The VG via **1651** couples the gate **1611** to the conductive rail **1645** which is further coupled to a first signal rail (not shown) arranged in the M**1** layer. The gate **1611** and the conductive rail **1645** together are coupled to the first signal rail, which corresponds to the connection I**1** being coupled to the first signal rail as discussed above with respect to FIG. **16**A, in some embodiments. The VG via **1652** couples the gate **1612** to the conductive rail **1642** which is further coupled to a second signal rail (not shown) arranged in the M**1** layer. The gate **1612** and the conductive rail **1642** together are coupled to the second signal rail, which corresponds to the connection I**2** being coupled to the second signal rail as discussed above with respect to FIG. **16**A, in some embodiments. The VG via **1653** couples the gate **1613** to the conductive rail **1646** which is further coupled to a third signal rail (not shown) arranged in the M**1** layer. The gate **1613** and the conductive rail **1646** together are coupled to the third signal rail, which corresponds to the connection I**3** being coupled to the third signal rail as discussed above with respect to FIG. **16**A, in some embodiments.

[0200] Conductive segments **1661**, **1662** and **1663** are arranged. The conductive segment **1661** is shaped as a railed block, and is also referred to as the M**0** jumper, corresponding to the conductive segment **124** as illustrated in FIG. **3**B or **3**C, in some embodiments. The conductive segment **1661** couples the conductive rails **1643** and **1644** together. With such configurations, the MD segments **1625** and **1622** are coupled together, which corresponds to the nodes B**1** and A**2** being coupled between the connection ZN as discussed above with respect to FIG. **16**A. In addition, the MD segments **1625**, **1622** and **1624** are further coupled together, which corresponds to the nodes B**1**, A**2** and A**4** being coupled to each other as discussed above with respect to FIG. **16**A.

[0201] Moreover, the conductive segments **1662** and **1663** are also referred to as the V**0** rails, and correspond to the conductive segments **111** and **112** as illustrated in FIGS. **3**A-**3**C, in some embodiments. As discussed above with reference to the VD vias **1631-1636**, the conductive segment **1662** couples to both of the conductive rail **1641** and the MD segments **1621** and **1623**, which is further coupled to the power rail VDD. The conductive segment **1663** couples to both of the conductive rail **1647** and the MD segment **1628**, which is further coupled to the power rail VSS.
[0202] Reference is now made to FIG. **17**A. FIG. **17**A is a circuit diagram of an IC **1700**A, in accordance with some embodiments of the present disclosure. For illustration of the IC **1700**A, a PMOS transistor P**1** includes a gate terminal A**1**, a drain (D) terminal and a source(S) terminal. A NMOS transistor N**1** includes a gate terminal B**2**, a D terminal and an S terminal. The S terminal of the PMOS transistor P**1** is coupled to the D terminal of the NMOS transistor N**1** to form a first transistor pair. A PMOS transistor P**2** includes a gate terminal B**1**, a D terminal and an S terminal. A NMOS transistor N**2** includes a gate terminal A**2**, a D terminal and an S terminal. The D terminal of the PMOS transistor P**2** is coupled to the S terminal of the NMOS transistor N**2** to form a second transistor pair.
[0203] The gate terminal A**1** of the PMOS transistor P**1** is coupled to the gate terminal A**2** of the NMOS transistor N**2**. The gate terminal B**1** of the PMOS transistor P**2** is coupled to the gate terminal B**2** of the NMOS transistor N**1**. The S terminal of the PMOS transistor P**1** and the D terminal of the NMOS transistor N**1** are coupled to the D terminal of the PMOS transistor P**2** and the S terminal of the NMOS transistor N**2**, to indicate a connection Z as shown in FIG. **17**A, in order to operate as a transmission gate circuit **1700**A. In some embodiments, the connection Z is further coupled to a signal rail and operated as an output terminal of the circuit **1700**A, for transmitting a data signal. In some embodiments, the transmission gate circuit **1700**A is in a single cell. To implement the transmission gate circuit **1700**A including the connection Z in the embodiments of the present disclosure, embodiments of layout designs and/or structures are provided as discussed in more detail below as illustrated with reference to FIG. **17**B, **17**C or **17**D.
[0204] Reference is now made to FIGS. **17**B and **17**C. FIGS. **17**B and **17**C are layout diagrams **1700**B and **1700**C of ICs corresponding to the IC **1700**A of FIG. **17**A, in accordance with some embodiments of the present disclosure. For simplicity of illustration of the layout diagram **1700**B or **1700**C, it is merely illustrates a part of layout diagram for implement the IC **1700**A of FIG. **17**A.
[0205] In some embodiments, the layout diagram **1700**B or **1700**C illustrates a unit pattern, in which the unit pattern is capable of being fabricated as a basic unit or as part of a device or circuit including the transmission gate as discussed above with respect to FIG. **17**A, in order to implement various layout diagrams. Alternatively stated, in some embodiments, the layout diagram **1700**B or **1700**C is implemented in various layout diagrams for implementing the devices or circuits including the transmission gate.
[0206] As illustrated in FIG. **17**B, the layout diagram **1700**B includes gates **1711** and **1712**, MD segments (not labelled), conductive rails **1741**, **1742** and **1743**, VG vias **1751** and **1752**, a conductive segment **1761**, and cut segments **1771** and **1772**.
[0207] The cut segments **1771** and **1772** arranged in the active area and extend along the row direction, patterned as “CT” in FIG. **17**B, for cutting off conductive segments in the layout diagram **1700**B. For example, the cut segment **1771** is configured to cut off the gate **1711**, and the cut segment **1772** is configured to cut off the gate **1712**. Alternatively stated, the cut segments **1771** and **1772** are configured to separate one gate **1711** or **1712** to two separated portions. In some embodiments, the cut segments **1771** and **1772** correspond to the cut segments CT at least shown in FIG. **1**A.
[0208] The VG via **1751** couples the gate **1711** with the VG via **1751** to the conductive rail **1743**, and VG via **1752** couples the gate **1712** with the VG via **1752** to the conductive rail **1741**.
[0209] The conductive segment **1761** is partially overlapped with the gate **1711**, the cut segment

1771, the conductive rails **1741** and **1743**, and the VG via **1751**. The conductive segment **1761** is also referred to as the M**0** jumper, and corresponds to the conductive segment **121**, **122** or **123** as illustrated in FIG. **3**A or **3**C, in some embodiments. The conductive segment **1761** couples the conductive rails **1741** and **1743** together.

[0210] In the illustration of FIG. **17**B, a poly pitch D**1** is referred to as a distance between two adjacent gates **1711** and **1712**. A M**0** pitch D**2** is referred to as a distance between two adjacent conductive rails **1741** and **1742**. In some embodiments, the poly pitch D**1** corresponds to the poly pitch D**1** shown in FIGS. **3**A to **3**C, and the M**0** pitch D**2** corresponds to the M**0** pitch D**2** shown in FIGS. **3**A to **3**C.

[0211] The cut segments **1771** and **1772** are separated by a distance D**3** in the column direction. The distance D**3** is referred to as a jog interval between two adjacent edges of these two adjacent cut segments **1771** and **1772**, as illustrated in FIG. **17**B. In addition, the gate **1711** is separated from the cut segment **1772** by a distance D**4** in the row direction. The cut segment **1772** is not arranged across the gate **1711** and is arranged next to the gate **1711**. The distance D**4** is referred to as an interval between an edge of the cut segment **1772** and an edge of the gate **1711**. The edge of the cut segment **1772** and the edge of the gate **1711** are arranged next to each other.

[0212] In some embodiments, a minimum of the distance D**3** is about in a range of 0.3 times of the M**0** pitch D**2** to 0.6 times of the M**0** pitch D**2** (i.e., 0.3*M**0** pitch D**2**˜1*M**0** pitch D**2**). In various embodiments, the distance D**4** is about in a range of 0.4 times of the poly pitch D**1** to 0.6 times of the poly pitch D**1** (i.e., 0.4*poly pitch D**1**˜0.6*poly pitch D**1**).

[0213] As illustrated in FIG. **17**C, the layout diagram **1700**C includes gates **1713**, **1714** and **1715**, MD segments (not labelled), conductive rails **1744** and **1745**, VG vias **1753** and **1754**, a conductive segment **1762**, and cut segments **1773** and **1774**.

[0214] The cut segment **1773** is partially overlapped with the gate **1713** and is configured to cut off the gate **1713**. The cut segment **1774** is partially overlapped with the gate **1715** and is configured to cut off the gate **1715**. In some embodiments, the cut segments **1773** and **1774** correspond to the cut segments CT at least shown in FIG. **1**A.

[0215] The VG via **1753** is overlapped with the gate **1713** and the conductive rail **1745**, for coupling the gate **1713** with the VG via **1753** to the conductive rail **1745**. The VG via **1754** is overlapped with the gate **1715** and the conductive rail **1744**, for coupling the gate **1715** with the VG via **1754** to the conductive rail **1744**.

[0216] The conductive segment **1762** is partially overlapped with the gate **1715**, the cut segment **1774**, the conductive rails **1744** and **1745**, and the VG via **1754**. The conductive segment **1762** is also referred to as the M**0** jumper, and corresponds to the conductive segment **121**, **122** or **123** as illustrated in FIG. **3**A or **3**C, in some embodiments. The conductive segment **1762** couples the conductive rails **1744** and **1745** together.

[0217] In the illustration of FIG. **17**C, the poly pitch D**1** and the M**0** pitch D**2** correspond to the poly pitch D**1** and the M**0** pitch D**2** shown in FIG. **17**B. The cut segments **1773** and **1774** are separated by a distance D**5** in the column direction. The distance D**5** is referred to as a jog interval between two adjacent edges of these two adjacent cut segments **1773** and **1774**, as illustrated in FIG. **17**C. The gate **1714** is separated from the cut segment **1774** by a distance D**6** in the row direction. The cut segment **1775** is not arranged across the gate **1714** and is arranged next to the gate **1714**. The distance D**6** is referred to as an interval between two adjacent edges of the cut segment **1774** and the gate **1714**.

[0218] In some embodiments, the distance D**5** corresponds to the distance D**3** shown in FIG. **17**B, and has a similar range scope. In some other embodiments, the distance D**6** corresponds to the distance D**4** shown in FIG. **17**B, and has a similar range scope.

[0219] Reference is now made to FIG. **17**D. FIG. **17**D is a layout diagram **1700**D of ICs corresponding to the IC **1700**A of FIG. **17**A, in accordance with some embodiments of the present disclosure.

[0220] In the illustration of FIG. **17**D, gates **1711** and **1712** are arranged as gate terminals of PMOS transistors P**1**-P**2** or NMOS transistors N**1**-N**2** in FIG. **17**A. MD segments **1721**, **1722**, **1723**, **1724** and **1725** are arranged as source/drain terminals of PMOS transistors P**1**-P**2** or NMOS transistors N**1**-N**2** in FIG. **17**A.
[0221] Cut segments **1771** and **1772** are arranged and will be removed for fabricating the layout diagram **1700**D. The cut segment **1771** is arranged across the gate **1711** for separating the gate **1711** to two portions including the gate **1711** with a VG **1751** and the gate **1711** with a VG **1753**. The cut segment **1771** is partially overlapped with a conductive rail **1743** and the gate **1711**. The cut segment **1772** is arranged across the gate **1712** for separating the gate **1712** to two portions including the gate **1712** with a VG **1752** and the gate **1712** with a VG **1754**. The cut segment **1772** is partially overlapped with a conductive rail **1744** and the gate **1712**.
[0222] The gate **1711** with the VG **1751** and the MD segments **1721** and **1722** together correspond to the PMOS transistor P**1**. The gate **1712** with the VG **1752** and the MD segments **1722** and **1723** together correspond to the PMOS transistor P**2**. The gate **1711** with the VG **1753** and the MD segments **1724** and **1722** together correspond to the NMOS transistor N**1**. The gate **1712** with the VG **1754** and the MD segments **1722** and **1725** together correspond to the NMOS transistor N**2**. In such embodiments, the PMOS transistors P**1** and P**2** and the NMOS transistors N**1** and N**2** share the MD segment **1722**, which corresponds to the PMOS transistors P**1** and P**2** and the NMOS transistors N**1** and N**2** being coupled between the connection Z illustrated in FIG. **17**A.
[0223] Conductive rails **1741**, **1742**, **1743**, **1744**, **1745** and **1746** are arranged. In some embodiments, the conductive rails **1741**, **1742**, **1743**, **1744**, **1745** and **1746** are referred to as the signal conductive rails, which are discussed above at least with reference to FIG. **4**.
[0224] VD via **1731** is arranged. The VD via **1731** couples the MD segment **1722** to the conductive rail **1746** which is further coupled to a signal rail (not shown) arranged in the M**1** layer. In some embodiments, the signal rail is indicated as the output terminal for transmitting the signal transmitted from the connection Z as discussed above with respect to FIG. **17**A.
[0225] VG vias **1751**, **1752**, **1753** and **1754** are arranged. The VG via **1751** couples the gate **1711** with the VG via **1751** to the conductive rail **1741** which is further coupled to a first signal rail (not shown) arranged in the MI layer. The VG via **1752** couples the gate **1712** with the VG via **1752** to the conductive rail **1743** which is further coupled to a second signal rail (not shown) arranged in the M**1** layer. The VG via **1753** couples the gate **1711** with the VG via **1753** to the conductive rail **1744** which is further coupled to the second signal rail. The VG via **1754** couples the gate **1712** with the VG via **1754** to the conductive rail **1745** which is further coupled to the first signal rail. In such configurations, it corresponds to the gate terminal A**1** of the PMOS transistor P**1** and the gate terminal A**2** of the NMOS transistor N**2** being coupled together to receive a first signal transmitted from the first signal rail, as discussed above with respect to FIG. **17**A. Similarly, it corresponds to the gate terminal B**1** of the PMOS transistor P**2** and the gate terminal N**2** of the NMOS transistor B**2** being coupled together to receive a second signal transmitted from the second signal rail, as discussed above with respect to FIG. **17**A.
[0226] Conductive segment **1761** is arranged. The conductive segment **1761** is shaped as a block, and is also referred to as the M**0** jumper, corresponding to the conductive segment **121**, **122** or **123** as illustrated in FIG. **3**A or **3**C, in some embodiments. The conductive segment **1761** is partially overlapped with the gate **1711**, the cut segment **1771**, two adjacent conductive rails **1743** and **1744**, and the VG via **1753**. The conductive segment **1761** couples the conductive rails **1743** and **1744** together. As discussed above, the conductive rails **1743** and **1744** are further coupled to the second signal rail by having the arrangement of the conductive segment **1761**.
[0227] Reference is now made to FIG. **17**E. FIG. **17**E is a layout diagram **1700**E of ICs corresponding to the IC **1700**A of FIG. **17**A, in accordance with some embodiments of the present disclosure.
[0228] In the illustration of FIG. **17**E, compared to the embodiments in FIG. **17**D, the cut segment

1771 is partially overlapped with a conductive rail **1744** and the gate **1711**, and the cut segment **1772** is partially overlapped with a conductive rail **1745**′ and the gate **1712**. The VG via **1753** couples the MD segment **1722** to the conductive rail **1743** which is further coupled to the signal rail (not shown) as an output rail for transmitting the signal transmitted from the connection Z as discussed above with respect to FIG. **17**A. The VG via **1752** couples the gate **1712** with the VG via **1752** to the conductive rail **1744** which is further coupled to the second signal rail. The VG via **1753** couples the gate **1711** with the VG via **1753** to the conductive rail **1744** which is further coupled to the second signal rail. The VG via **1754** couples the gate **1712** with the VG via **1754** to the conductive rail **1745** which is further coupled to the first signal rail. In such configurations, it also corresponds to the connections illustrated in FIG. **17**A, as discussed with reference FIG. **17**D. The conductive segment **1761** is partially overlapped with the gate **1711**, the cut segment **1771**, two adjacent conductive rails **1744** and **1745**, and the VG via **1753**.

[0229] Reference is now made to FIG. **18**A. FIG. **18**A is a circuit diagram of an IC **1800**A that is equivalent to the transmission gate circuit **1700**A in FIG. **17**A, in accordance with some embodiments of the present disclosure. In the illustration of FIG. **18**A, compared to FIG. **17**A, the IC **1800**A further includes a PMOS transistor P**3** and a NMOS transistor N**3**. A gate terminal of the PMOS transistor P**1** is coupled to a node A**1**; a gate terminal of the PMOS transistor P**2** is coupled to a node B**1**; a gate terminal of the PMOS transistor P**3** is coupled to a gate of the NMOS transistor N**2**. A gate terminal of the NMOS transistor N**1** is coupled to a node B**2**; a gate terminal of the NMOS transistor N**3** is coupled to the gate of the PMOS transistor P**2**; the gate terminal of the NMOS transistor N**2** is coupled to a node A**2**. The node A**2** is further coupled to the gate terminal of the PMOS transistor P**3**. The node B**1** is further coupled to the node B**2** as indicated by connection Z shown in FIG. **18**A. To implement the IC **1800**A including the connection Z between the nodes B**1** and B**2** in the embodiments of the present disclosure, embodiments of layout designs and/or structures are provided and discussed below as illustrated with reference to FIG. **18**B.

[0230] Furthermore, a source/drain terminal of the PMOS transistor P**1** is coupled to a source/drain terminal of the PMOS transistor P**2** at a node S**1**; a source/drain terminal of the PMOS transistor P**2** is coupled to a source/drain terminal of the PMOS transistor P**3** at a node S**2**; and a source/drain terminal of the PMOS transistor P**3** is coupled to a node S**2**′. A source/drain terminal of the NMOS transistor N**1** is coupled to a source/drain terminal of the NMOS transistor N**3** at a node S**3**; a source/drain terminal of the NMOS transistor N**3** is coupled to a source/drain terminal of the NMOS transistor N**2** at a node S**3**′. The node S**1** is further coupled to the node S**3** as indicated by connection Z′ shown in FIG. **18**A. To implement the IC **1800**A including the connection Z′ between the nodes S**1** and S**3** in the embodiments of the present disclosure, embodiments of layout designs and/or structures are provided and discussed below as illustrated with reference to FIG. **18**B.

[0231] The node S**2** is further coupled to the node S**2**′, corresponding to the source terminal and the drain terminal of the PMOS transistor P**3** coupled together. The source and drain terminal of the PMOS transistor P**3** are coupled together in a short-circuit configuration such that the PMOS transistor P**3** is inoperative. In addition, the node S**3** is further coupled to the node S**3**′, corresponding to the source terminal and the drain terminal of the NMOS transistor N**3** coupled together. The source and drain terminal of the NMOS transistor N**3** are coupled together in a short-circuit configuration such that the NMOS transistor N**3** is inoperative. With the connections of the PMOS transistor P**3** and the NMOS transistor N**3**, as illustrated in FIG. **18**A, the IC **1800**A is able to operate as a circuit equivalent to the transmission gate circuit **1700**A in FIG. **17**A.

[0232] FIG. **18**B is a layout diagram **1800**B of an IC corresponding to the IC **1800**A of FIG. **18**A, in accordance with some embodiments of the present disclosure.

[0233] In the illustration of FIG. **18**B, gates **1811**, **1812** and **1813** are arranged as gate terminals of PMOS transistors P**1**-P**3** or NMOS transistors N**1**-N**3** in FIG. **18**A. MD segments **1821**, **1822**, **1823**, **1824**, **1825**, **1826** and **1827** are arranged as source/drain terminals of PMOS transistors P**1**-P**3** or NMOS transistors N**1**-N**3** in FIG. **18**A.

[0234] A cut segment **1871** is arranged and will be removed for fabricating the IC **1800**A. The cut segment **1871** is arranged across the gate **1811** for separating the gate **1811** to two portions including the gate **1811** with a VG **1851** and the gate **1811** with a VG **1853**.
[0235] The gate **1811** with the VG **1851** and the MD segments **1821** and **1822** together correspond to the PMOS transistor P**1**. The gate **1812** and the MD segments **1822** and **1823** together correspond to the PMOS transistor P**2**. In such embodiments, the PMOS transistors P**1** and P**2** share the MD segment **1822**, which corresponds to the PMOS transistors P**1** and P**2** being coupled at the node S**1** illustrated in FIG. **18**A. The gate **1813** and the MD segments **1823** and **1824** together correspond to the PMOS transistor P**3**. In such embodiments, the PMOS transistors P**2** and P**3** share the MD segment **1823**, which corresponds to the PMOS transistors P**2** and P**3** being coupled at the node S**2** illustrated in FIG. **18**A. The gate **1811** with the VG **1853** and the MD segments **1825** and **1822** together correspond to the NMOS transistor N**1**. The gate **1812** and the MD segments **1822** and **1826** together correspond to the NMOS transistor N**3**. In such embodiments, the NMOS transistors N**1** and N**3** share the MD segment **1822**, which corresponds to the NMOS transistors N**1** and N**3** being coupled at the node S**3** illustrated in FIG. **18**A. Furthermore, the PMOS transistors P**1** and P**2** and the NMOS transistors N**1** and N**3** share the MD segment **1822**, which corresponds to the PMOS transistors P**1** and P**2** and the NMOS transistors N**1** and N**3** being coupled between the connection Z′ illustrated in FIG. **18**A. The gate **1813** and the MD segments **1826** and **1827** together correspond to the NMOS transistor N**2**. In such embodiments, the NMOS transistors N**3** and N**2** share the MD segment **1826**, which corresponds to the NMOS transistors N**3** and N**2** being coupled at the node S**3**′ illustrated in FIG. **18**A.
[0236] Conductive rails **1841**, **1842**, **1843**, **1844**, **1845**, **1846**, **1847** and **1848** are arranged. In some embodiments, the conductive rails **1842**, **1843**, **1844**, **1846**, **1847** and **1848** are referred to as the signal conductive rails, and the conductive rails **1841** and **1845** are referred to as the power conductive rails, which are discussed above at least with reference to FIG. **4**.
[0237] VD vias **1831**, **1832**, **1833**, **1834** and **1835** are arranged. The VD via **1831** couples the MD segment **1822** to the conductive rail **1842**. The VD via **1832** couples the MD segment **1823** to the conductive rail **1846**, and the VD via **1833** couples the MD segment **1824** to the conductive rail **1846**. In such embodiments, the source terminal of the PMOS transistor P**3** and the drain terminal of the PMOS transistor P**3** are coupled together, which corresponds to the source/drain terminals of the PMOS transistor P**3** being coupled at the nodes S**2** and S**2**′ as the short-circuit configuration illustrated in FIG. **18**A. Similarly, the VD via **1834** couples the MD segment **1822** to the conductive rail **1845**, and the VD via **1835** couples the MD segment **1826** to the conductive rail **1846**. In such embodiments, the source terminal of the NMOS transistor N**2** and the drain terminal of the NMOS transistor N**2** are coupled together, which corresponds to the source/drain terminals of the NMOS transistor N**2** being coupled together at the nodes S**3** and S**3**′ as the short-circuit configuration illustrated in FIG. **18**A.
[0238] VG vias **1851**, **1852**, **1853** and **1854** are arranged. The VG via **1851** couples the gate **1811** with the VG **1851** to the conductive rail **1841** which is further coupled to a first signal rail (not shown) arranged in the M**1** layer. It corresponds to the PMOS transistor P**1** being coupled at the node A**1** in FIG. **18**A. The VG via **1852** couples the gate **1812** to the conductive rail **1843**. The VG via **1853** couples the gate **1812** with the VG **1853** to the conductive rail **1844**. The VG via **1854** couples the gate **1813** to the conductive rail **1847** which is further coupled to a second signal rail (not shown) arranged in the M**1** layer. It corresponds to the NMOS transistor N**2** being coupled at the node A**2** in FIG. **18**A.
[0239] A conductive segment **1861** is arranged, and is partially overlapped with the cut segment **1871**, the gate **1811**, the conductive rails **1843** and **1844**, and the VG via **1853**. The conductive segment **1861** is shaped as a block, and is also referred to as a M**0** jumper, corresponding to the conductive segment **121**, **122** or **123** as illustrated in FIG. **3**A or **3**C, in some embodiments. The conductive segment **1861** couples the conductive rails **1843** and **1844** together. With such

configurations, the gate **1811** with the VG via **1853** and the gate **1812** are coupled together, which corresponds to the nodes B**1** and B**2** being coupled between the connection Z as discussed above with respect to FIG. **18**A.

[0240] Reference is now made to FIG. **19**A. FIG. **19**A is a circuit diagram of an IC **1900**A that is equivalent to the transmission gate circuit **1700**A in FIG. **17**A, in accordance with some embodiments of the present disclosure. In the illustration of FIG. **19**A, compared to FIG. **17**A, the IC **1900**A further includes PMOS transistor P**3**, P**4**, P**5** and P**6** and NMOS transistors N**3**, N**4**, N**5** and N**6**. A gate terminal of the PMOS transistor P**1** is coupled to a gate terminal of the NMOS transistor N**1** at a node C**1**; a gate terminal of the PMOS transistor P**2** is coupled to a gate terminal of the NMOS transistor N**2** as indicated by connection I**1**; a gate terminal of the PMOS transistor P**3** is coupled to a node SB**1**; a gate terminal of the PMOS transistor P**4** is coupled to a gate terminal of the NMOS transistor N**4** as indicated by connection I**2**; a gate terminal of the PMOS transistor P**5** is coupled to a node S**1**; a gate terminal of the PMOS transistor P**6** is coupled to a gate terminal of the NMOS transistor N**6** as indicated by connection S**2**; a gate terminal of the NMOS transistor N**3** is coupled to a node S**3**; and a gate terminal of the NMOS transistor N**5** is coupled to a node SB**3**.

[0241] In some embodiments for illustrating the FIGS. **19**A and **19**B, the nodes SB**1**, SB**2** and the connection SB**3** are further coupled to a first signal rail indicated as SB (not shown), for receiving a first signal transmitted from the first signal rail. The nodes S**1**, S**2** and S**3** are further coupled to a second signal rail indicated as S (not shown), for receiving a second signal, other than the first signal, transmitted from the signal rail. The connection I**1** is further coupled to a third signal rail indicated as I**1** (not shown), for receiving a third signal transmitted from the third signal rail. The connection I**2** is further coupled to a fourth signal rail indicated as I**2** (not shown), for receiving a fourth signal transmitted from the fourth signal rail.

[0242] Furthermore, a source/drain terminal of the PMOS transistor P**1** is coupled to a node A**1**; a source/drain terminal of the PMOS transistor P**1** is coupled to a source/drain terminal of a PMOS transistor P**2** at a node A**2**; a source/drain terminal of the PMOS transistor P**2** is coupled to a source/drain terminal of a PMOS transistor P**3**; a source/drain terminal of the PMOS transistor P**3** is coupled to a source/drain terminal of a PMOS transistor P**4** at a node A**3**; a source/drain terminal of the PMOS transistor P**4** is coupled to a source/drain terminal of a PMOS transistor P**5**; a source/drain terminal of the PMOS transistor P**5** is coupled to a source/drain terminal of a PMOS transistor P**6** at a node A**4**; and a source/drain terminal of the PMOS transistor P**6** is coupled to a node A**5**. A source/drain terminal of the NMOS transistor N**1** is coupled to a node B**1**; a source/drain terminal of the NMOS transistor N**1** is coupled to a source/drain terminal of a NMOS transistor N**2** at a node B**2**; a source/drain terminal of the NMOS transistor N**2** is coupled to a source/drain terminal of a NMOS transistor N**3**; a source/drain terminal of the NMOS transistor N**3** is coupled to a source/drain terminal of a NMOS transistor N**4** at a node B**3**; a source/drain terminal of the NMOS transistor N**4** is coupled to a source/drain terminal of a NMOS transistor N**5**; a source/drain terminal of the NMOS transistor N**5** is coupled to a source/drain terminal of a NMOS transistor N**6** at a node B**4**; and a source/drain terminal of the NMOS transistor N**6** is coupled to a node B**5**.

[0243] The nodes A**2** and A**4** are further coupled to a power rail referenced as VDD. The nodes B**2** and B**4** are further coupled to another power rail referenced as VSS. The node C**2** is further coupled to the node C**1**. The node A**1** is further coupled to the node B**1** as indicated by connection Z. The node A**3** is further coupled to the node B**3** at a node C**2**. The node C**2** is further coupled to the node C**1** as indicated by connection S**4**. The node A**5** is further coupled to the node B**5** as indicated by connection SB**2**. To implement the IC **1900**A including the connection Z between the nodes A**1** and B**1**, the connection S**4** between the nodes C**1** and C**2**, and the connection SB**2** between the nodes A**5** and B**5**, in the embodiments of the present disclosure, embodiments of layout designs and/or structures are provided and discussed below as illustrated with reference to FIG. **19**B.

[0244] FIG. **19**B is a layout diagram **1900**B of an IC corresponding to the IC **1900**A of FIG. **19**A, in accordance with some embodiments of the present disclosure. Compared to the layout **1800**B in FIG. **18**B, less conductive rails are arranged in the layout diagram **1900**B.

[0245] In the illustration of FIG. **19**B, gates **1911**, **1912**, **1913**, **1914**, **1915** and **1916** are arranged as gate terminals of PMOS transistors P**1**-P**6** or NMOS transistors N**1**-N**6** in FIG. **18**A. MD segments **1920**, **1920**′, **1921**, **1922**, **1923**, **1924**, **1925**, **1926**, **1927**, **1928** and **1929** are arranged as source/drain terminals of PMOS transistors P**1**-P**6** or NMOS transistors N**1**-N**6** in FIG. **19**A. Cut segments **1971** and **1972** are arranged. The cut segment **1971** is arranged across the gate **1913** for separating the gate **1913** to two portions including the gate **1913** with a VG **1953** and the gate **1913** with a VG **1954**. The cut segment **1972** is arranged across the gate **1915** for separating the gate **1915** to two portions including the gate **1915** with a VG **1956** and the gate **1915** with a VG **1957**.

[0246] The gate **1911** and the MD segments **1920** and **1921** together correspond to the PMOS transistor P**1**. The gate **1912** and the MD segments **1921** and **1922** together correspond to the PMOS transistor P**2**. In such embodiments, the PMOS transistors P**1** and P**2** share the MD segment **1921**, which corresponds to the PMOS transistors P**1** and P**2** being coupled at the node A**2** illustrated in FIG. **19**A. The gate **1913** with the VG **1953** and the MD segments **1922** and **1923** together correspond to the PMOS transistor P**3**. The gate **1914** and the MD segments **1923** and **1924** together correspond to the PMOS transistor P**4**. In such embodiments, the PMOS transistors P**3** and P**4** share the MD segment **1923**, which corresponds to the PMOS transistors P**3** and P**4** being coupled at the node A**3** illustrated in FIG. **19**A. The gate **1915** with the VG **1956** and the MD segments **1924** and **1925** together correspond to the PMOS transistor P**5**. The gate **1916** and the MD segments **1925** and **1926** together correspond to the PMOS transistor P**6**. In such embodiments, the PMOS transistors P**5** and P**6** share the MD segment **1925**, which corresponds to the PMOS transistors P**5** and P**6** being coupled at the node A**4** illustrated in FIG. **19**A.

[0247] Furthermore, the gate **1911** and the MD segments **1920** and **1927** together correspond to the NMOS transistor N**1**. In such embodiments, the NMOS transistor N**1** and the PMOS transistor P**1** share the MD segment **1920**, which corresponds to the NMOS transistor N**1** and the PMOS transistor P**1** being coupled between illustrated the connection Z in FIG. **19**A. The gate **1912** and the MD segments **1927** and **1928** together correspond to the NMOS transistor N**2**. In such embodiments, the NMOS transistors N**1** and N**2** share the MD segment **1927**, which corresponds to the NMOS transistors N**1** and N**2** being coupled at the node B**2** in FIG. **19**A. The gate **1913** and the MD segments **1928** and **1923** together correspond to the NMOS transistor N**3**. The gate **1914** and the MD segments **1923** and **1929** together correspond to the NMOS transistor N**4**. In such embodiments, the NMOS transistors N**3**-N**4** and the PMOS transistors P**3**-P**4** share the MD segment **1923**, which corresponds to the NMOS transistors N**3**-N**4** and the PMOS transistors P**3**-P**4** being coupled between the nodes A**3** and B**3** in FIG. **19**A. The gate **1915** with the VG **1957** and the MD segments **1929** and **1920**′ together correspond to the NMOS transistor N**5**. The gate **1916** and the MD segments **1920**′ and **1926** together correspond to the NMOS transistor N**6**. In such embodiments, the NMOS transistors N**5** and N**6** share the MD segment **1920**′, which corresponds to the NMOS transistors N**5** and N**6** being coupled at the node B**4** in FIG. **19**A. in addition, the NMOS transistor N**6** and the PMOS transistor P**6** share the MD segment **1926**, which corresponds to the NMOS transistor N**6** and the PMOS transistor P**6** being coupled between the nodes A**5** and B**5** in FIG. **19**A.

[0248] Conductive rails **1940**, **1940**′, **1941**, **1942**, **1943**, **1944**, **1945**, **1946**, **1947**. **1948** and **1949** are arranged. In some embodiments, the conductive rails **1940**, **1940**′, **1942**, **1943**, **1944**, **1945**, **1947**. **1948** and **1949** are referred to as signal conductive rails, and the conductive rails **1941** and **1946** are referred to as power conductive rails, which are discussed above at least with reference to FIG. **4**.

[0249] VD vias **1931**, **1932**, **1933**, **1934**, **1935**, **1936** and **1937** are arranged. The VD via **1931** couples the MD segment **1920** to the conductive rail **1942**. The VD via **1932** couples the MD segment **1921** to the conductive rail **1941** which is further coupled to a power rail (not shown) arranged in the M**1** layer. The MD segment **1921** and the conductive rail **1941** together are coupled to the power rail, which corresponds to the node A**2** being coupled to the power rail VDD as discussed above with respect to FIG. **19**A. The VD via **1933** couples the MD segment **1923** to the conductive rail **1944**. The VD via **1934** couples the MD segment **1925** to the conductive rail **1941**. The MD segment **1925** and the conductive rail **1941** together are coupled to the power rail, which corresponds to the node A**4** being coupled to the power rail VDD as discussed above with respect to FIG. **19**A.

[0250] Moreover, the VD via **1935** couples the MD segment **1927** to the conductive rail **1946** which is further coupled to another power rail (not shown) arranged in the M**1** layer. The MD segment **1927** and the conductive rail **1946** together are coupled to such power rail, which corresponds to the node B**2** being coupled to the power rail VD VSS as discussed above with respect to FIG. **19**A. The VD via **1936** couples the MD segment **1920**′ to the conductive rail **1946** which is further coupled to the power rail (not shown) that is same as the conductive rail **1946** is coupled to. The MD segment **1920**′ and the conductive rail **1946** together are coupled to such power rail, which corresponds to the node B**4** being coupled to the power rail VD VSS as discussed above with respect to FIG. **19**A. The VD via **1937** couples the MD segment **1926** to the conductive rail **1940** which is further coupled to the first signal rail (not shown) arranged in the M**1** layer.

[0251] VG vias **1951**, **1952**, **1953**, **1954**, **1955**, **1957**, **1958** and **1959** are arranged. The VG via **1951** couples the gate **1911** to the conductive rail **1944** which is further coupled to a signal rail (not shown) arranged in the M**1** layer. It corresponds to the PMOS transistor P**1** and the NOMS transistor N**1** being coupled at the node C**11** in FIG. **19**A. In such configurations, the MD segment **1923** coupled to the conductive rail **1944** is further coupled to the gate **1911**. It corresponds to the nodes C**1** and C**2** which is also coupled to the nodes A**3** and B**3** being coupled between the connection S**4** in FIG. **19**A. The VG via **1952** couples the gate **1912** to the conductive rail **1945** which is further coupled to the third signal rail (not shown) arranged in the M**1** layer. It corresponds to the PMOS transistor P**2** and the NOMS transistor N**2** being between the connection I**1** in FIG. **19**A. The VG via **1953** couples the gate **1913** with the VG via **1953** to the conductive rail **1949** which is further coupled to the first signal rail. It corresponds to the PMOS transistor P**3** being coupled at the node SB**1** in FIG. **19**A. The VG via **1954** couples the gate **1913** with the VG via **1954** to the conductive rail **1940**′ which is further coupled to the second signal rail (not shown) arranged in the M**1** layer, in some embodiments. It corresponds to the NMOS transistor N**3** being coupled at the node S**3** in FIG. **19**A.

[0252] Moreover, the VG via **1955** couples the gate **1914** to the conductive rail **1947** which is further coupled to the fourth signal rail (not shown) arranged in the MI layer, in some embodiments. It corresponds to the PMOS transistor P**4** and the NOMS transistor N**4** being between the connection I**2** in FIG. **19**A. The VG via **1956** couples the gate **1915** with the VG via **1956** to the conductive rail **1948** which is further coupled to the second signal rail. It corresponds to the PMOS transistor P**5** being coupled at the node S**1** in FIG. **19**A. The VG via **1957** couples the gate **1915** with the VG via **1957** to the conductive rail **1940** which is further coupled to the first signal rail. It corresponds to the NMOS transistor N**5** being coupled at the node SB**3** in FIG. **19**A. The VG via **1958** couples the gate **1916** to the conductive rail **1948** which is further coupled to the second signal rail. Also, the VG via **1959** couples the gate **1916** to the conductive rail **1940**′ which is further coupled to the second signal rail as well. It corresponds to the PMOS transistor P**6** and the NOMS transistor N**6** being between the connection S**2** in FIG. **19**A.

[0253] Conductive segments **1961**, **1962**, **1963** and **1964** are arranged. The conductive segment **1961** is shaped as a railed block, and is also referred to as a M**0** jumper, corresponding to the conductive segment **124** as illustrated in FIG. **3**B or **3**C, in some embodiments. The conductive segment **1961** couples the conductive rails **1942** and **1943** together.

[0254] Moreover, the conductive segment **1962** is shaped as a block, and is also referred to as a M**0** jumper, corresponding to the conductive segment **121**, **122** or **123** as illustrated in FIG. **3**A or **3**C,

in some embodiments. The conductive segment **1962** is partially overlapped with the gate **1915**, the cut segment **1972**, the conductive rails **1949** and **1940**, and the VG via **1957**. The conductive segment **1962** couples the conductive rails **1949** and **1940** together. With such configurations, the gate **1913**, the gate **1915** with the VG via **1957** and the MD segment **1926** are coupled together, which corresponds to the PMOS transistor P**3**, the NMOS transistor N**5**, and the nodes B**1** and A**2** coupled between the connection SB**2** being coupled to a same signal rail which, in some embodiments, is the first signal rail, as discussed above with respect to FIG. **19**A.
[0255] Furthermore, the conductive segments **1963** and **1964** are also referred to as the V**0** rails, and correspond to the conductive segments **111** and **112** as illustrated in FIGS. **3**A-**3**C, in some embodiments. As discussed above with reference to the VD vias **1931**-**1937**, the conductive segment **1963** couples to both of the conductive rail **1941** and the MD segments **1921** and **1925**, which is further coupled to the power rail VDD. The conductive segment **1964** couples to both of the conductive rail **1946** and the MD segments **1927** and **1920**′, which is further coupled to the power rail VSS.
[0256] As illustrated by the non-limiting examples depicted in FIGS. **1**A to **19**B and discussed above, the various embodiments include conductive segments formed on conductive rails and disposed above the M**0** layer and below the M**1** layer, thereby increasing routing flexibility compared to approaches in which lack of these conductive segments.
[0257] Reference is now made to FIG. **20**. FIG. **20** is a flow chart of a method **2000** for fabricating an IC, in accordance with some embodiments of the present disclosure. In some embodiments, the IC is manufactured based on an IC layout diagram includes one of layout diagrams **100**A, **100**B, **200**, **300**A-**300**C, **400**, **500**A-**500**C, **800**, **1100**B, **1200**B, **1300**B, **1400**B, **1500**B, **1600**B, **1700**B-**1700**E, **1800**B, or **1900**B, corresponding to an IC structure, e.g., one of ICs **700**, or **1000**, discussed above with respect to FIGS. **1**A-**19**B. In some embodiments, the operations of method **2000** are performed in the order depicted in FIG. **20**. In some embodiments, the operations of method **2000** are performed simultaneously and/or in an order other than the order depicted in FIG. **20**. In some embodiments, one or more operations are performed before, between, during, and/or after performing one or more operations of method **2000**.
[0258] At operation **2010**, conductive rails are formed in a first metal layer. In some embodiments, the conductive rails correspond to the conductive rails P**01**, P**02** and S**01**-S**04** discussed above with respect to FIGS. **1**A to **19**B. The first metal layer correspond to the M**0** layer discussed above with respect to FIGS. **1**A to **19**B.
[0259] In some embodiments, the conductive rails include a pair of first conductive rails. In various embodiments, the pair of first conductive rails correspond to the conductive rails P**01** and P**02**, that are also indicated as power conductive rails, discussed above with respect to FIGS. **1**A to **19**B.
[0260] At operation **2020**, signal rails are formed in a second metal layer above the first metal layer. In some embodiments, the signal rails correspond to the signal rails P**11**, P**12** and S**11**-S**4** or rails not shown discussed above with respect to FIGS. **1**A to **19**B. The second metal layer correspond to the M**1** layer discussed above with respect to FIGS. **1**A to **19**B.
[0261] At operation **2030**, a first conductive segment is formed between the first metal layer and the second metal layer, and is spaced apart from the signal rails. In some embodiments, the first conductive segment is overlapped with the pair of first conductive rails in a layout view. In some embodiments, the first conductive segment corresponds to the conductive segment indicated as the V**0** rail discussed above with respect to FIGS. **1**A to **19**B. For example, the first conductive segment corresponds to the conductive segment **111** or **112** shown in FIGS. **1**A, **1**B, **3**A to **3**C, or the conductive segment **411***a*, **411***b*, **412***a*. **412***b* in FIGS. **4**, **5**A to **5**C, etc.
[0262] In some embodiments, the method **2000** further includes the operations as follows. A second conductive segment is also formed between the first metal layer and the second metal layer, and is also spaced apart from the signal rails. The second conductive segment is overlapped with at least two adjacent conductive rails between the pair of first conductive rail in a layout view. In some

embodiments, the second conductive segment corresponds to the conductive segment indicated as the M**0** jumper discussed above with respect to FIGS. **1**A to **19**B. For example, the second conductive segment corresponds to the conductive segment **121**, **122**, **123** or **124** shown in FIGS. **1**A, **1**B, **3**A to **3**C, or the conductive segment **421** in FIGS. **4**, **5**A to **5**C, etc. In various embodiments, the adjacent conductive rails disposed with the second conductive segment corresponds to the conductive rails S**0**, that are also indicated as signal conductive rails, discussed above with respect to FIGS. **1**A to **19**B.

[0263] Reference is now made to FIG. **21**. FIG. **21** is a block diagram of an electronic design automation (EDA) system **2100** for designing the integrated circuit layout design, in accordance with some embodiments of the present disclosure. EDA system **2100** is configured to implement one or more operations of the method **600** disclosed in FIG. **6** and the method **2000** disclosed in FIG. **20**, and further explained in conjunction with FIGS. **1**A-5C and **7**A-**19**B. In some embodiments, EDA system **2100** includes an APR system.

[0264] In some embodiments, EDA system **2100** is a general purpose computing device including a hardware processor **2120** and a non-transitory, computer-readable storage medium **2160**. Storage medium **2160**, amongst other things, is encoded with, i.e., stores, computer program code (instructions) **2161**, i.e., a set of executable instructions. Execution of instructions **2161** by hardware processor **2120** represents (at least in part) an EDA tool which implements a portion or all of, e.g., the method **600** or **2000**.

[0265] The processor **2120** is electrically coupled to computer-readable storage medium **2160** via a bus **2150**. The processor **2120** is also electrically coupled to an I/O interface **2110** and a fabrication tool **2170** by bus **2150**. A network interface **2130** is also electrically connected to processor **2120** via bus **2150**. Network interface **2130** is connected to a network **2140**, so that processor **2120** and computer-readable storage medium **2160** are capable of connecting to external elements via network **2140**. The processor **2120** is configured to execute computer program code **2161** encoded in computer-readable storage medium **2160** in order to cause EDA system **2100** to be usable for performing a portion or all of the noted processes and/or methods. In one or more embodiments, processor **2120** is a central processing unit (CPU), a multi-processor, a distributed processing system, an application specific integrated circuit (ASIC), and/or a suitable processing unit.

[0266] In one or more embodiments, computer-readable storage medium **2160** is an electronic, magnetic, optical, electromagnetic, infrared, and/or a semiconductor system (or apparatus or device). For example, computer-readable storage medium **2160** includes a semiconductor or solid-state memory, a magnetic tape, a removable computer diskette, a random access memory (RAM), a read-only memory (ROM), a rigid magnetic disk, and/or an optical disk. In one or more embodiments using optical disks, computer-readable storage medium **2160** includes a compact disk-read only memory (CD-ROM), a compact disk-read/write (CD-R/W), and/or a digital video disc (DVD).

[0267] In one or more embodiments, storage medium **2160** stores computer program code **2161** configured to cause EDA system **2100** (where such execution represents (at least in part) the EDA tool) to be usable for performing a portion or all of the noted processes and/or methods. In one or more embodiments, storage medium **2160** also stores information which facilitates performing a portion or all of the noted processes and/or methods. In one or more embodiments, storage medium **2160** stores library **2162** of standard cells including such standard cells as disclosed herein, for example, a cell including conductive segments **111**, **112** or **121-123** discussed above with respect to FIG. **1**A.

[0268] EDA system **2100** includes I/O interface **2110**. I/O interface **2110** is coupled to external circuitry. In one or more embodiments, I/O interface **2110** includes a keyboard, keypad, mouse, trackball, trackpad, touchscreen, and/or cursor direction keys for communicating information and commands to processor **2120**.

[0269] EDA system **2100** also includes network interface **2130** coupled to processor **2120**.

Network interface **2130** allows EDA system **2100** to communicate with network **2140**, to which one or more other computer systems are connected. Network interface **2130** includes wireless network interfaces such as BLUETOOTH, WIFI, WIMAX, GPRS, or WCDMA; or wired network interfaces such as ETHERNET, USB, or IEEE-1364. In one or more embodiments, a portion or all of noted processes and/or methods, is implemented in two or more systems **2100**.

[0270] EDA system **2100** also includes the fabrication tool **2170** coupled to the processor **2120**. The fabrication tool **2170** is configured to fabricate integrated circuits, including, for example, the integrated circuit **700** illustrated in FIGS. **7**A-**7**G or the integrated circuit **1000** illustrated in FIGS. **10**A-**10**C, based on the design files processed by the processor **2120** and/or the IC layout designs as discussed above.

[0271] EDA system **2100** is configured to receive information through I/O interface **2110**. The information received through I/O interface **2110** includes one or more of instructions, data, design rules, libraries of standard cells, and/or other parameters for processing by processor **2120**. The information is transferred to processor **2120** via bus **2150**. EDA system **2100** is configured to receive information related to a UI through I/O interface **2110**. The information is stored in computer-readable medium **2160** as user interface (UI) **2163**.

[0272] In some embodiments, a portion or all of the noted processes and/or methods is implemented as a standalone software application for execution by a processor. In some embodiments, a portion or all of the noted processes and/or methods is implemented as a software application that is a part of an additional software application. In some embodiments, a portion or all of the noted processes and/or methods is implemented as a plug-in to a software application. In some embodiments, at least one of the noted processes and/or methods is implemented as a software application that is a portion of an EDA tool. In some embodiments, a portion or all of the noted processes and/or methods is implemented as a software application that is used by EDA system **2100**. In some embodiments, a layout diagram which includes standard cells is generated using a tool such as VIRTUOSO® available from CADENCE DESIGN SYSTEMS, Inc., or another suitable layout generating tool.

[0273] In some embodiments, the processes are realized as functions of a program stored in a non-transitory computer readable recording medium. Examples of a non-transitory computer readable recording medium include, but are not limited to, external/removable and/or internal/built-in storage or memory unit, for example, one or more of an optical disk, such as a DVD, a magnetic disk, such as a hard disk, a semiconductor memory, such as a ROM, a RAM, a memory card, and the like.

[0274] FIG. **22** is a block diagram of IC manufacturing system **2200**, and an IC manufacturing flow associated therewith, in accordance with some embodiments. In some embodiments, based on a layout diagram, at least one of (A) one or more semiconductor masks or (B) at least one component in a layer of a semiconductor integrated circuit is fabricated using IC manufacturing system **2200**.

[0275] In FIG. **22**, IC manufacturing system **2200** includes entities, such as a design house **2210**, a mask house **2220**, and an IC manufacturer/fabricator ("fab") **2230**, that interact with one another in the design, development, and manufacturing cycles and/or services related to manufacturing an IC device **2240**. The entities in IC manufacturing system **2200** are connected by a communications network. In some embodiments, the communications network is a single network. In some embodiments, the communications network is a variety of different networks, such as an intranet and the Internet. The communications network includes wired and/or wireless communication channels. Each entity interacts with one or more of the other entities and provides services to and/or receives services from one or more of the other entities. In some embodiments, two or more of design house **2210**, mask house **2220**, and IC fab **2230** is owned by a single larger company. In some embodiments, two or more of design house **2210**, mask house **2220**, and IC fab **2230** coexist in a common facility and use common resources.

[0276] Design house (or design team) **2210** generates an IC design layout diagram **2211**. IC design layout diagram **2211** includes various geometrical patterns, for example, an IC layout design depicted in FIGS. **1**A-**1**B, FIG. **2**, FIGS. **3**A-**3**C, FIG. **4**, FIGS. **5**A-**5**C, FIG. **8**, FIGS. **9**A-**9**C, FIG. **11**B, FIG. **12**B, FIG. **13**B, FIG. **14**B, FIG. **15**B, FIG. **16**B, FIG. **17**B, FIG. **18**B, and/or FIG. **19**B, designed for an IC device **2240**, for example, integrated circuits **700** and **1000**, discussed above with respect to FIGS. **7**A-**7**G and/or FIGS. **10**A-**10**C. The geometrical patterns correspond to patterns of metal, oxide, or semiconductor layers that make up the various components of IC device **2240** to be fabricated. The various layers combine to form various IC features. For example, a portion of IC design layout diagram **2211** includes various IC features, such as an active area, gate electrode, source and drain, conductive segments or vias of an interlayer interconnection, to be formed in a semiconductor substrate (such as a silicon wafer) and various material layers disposed on the semiconductor substrate. Design house **2210** implements a proper design procedure to form IC design layout diagram **2211**. The design procedure includes one or more of logic design, physical design or place and route. IC design layout diagram **2211** is presented in one or more data files having information of the geometrical patterns. For example, IC design layout diagram **2211** can be expressed in a GDSII file format or DFII file format.

[0277] Mask house **2220** includes data preparation **2221** and mask fabrication **2222**. Mask house **2220** uses IC design layout diagram **2211** to manufacture one or more masks **2223** to be used for fabricating the various layers of IC device **2240** according to IC design layout diagram **2211**. Mask house **2220** performs mask data preparation **2221**, where IC design layout diagram **2211** is translated into a representative data file ("RDF"). Mask data preparation **2221** provides the RDF to mask fabrication **2222**. Mask fabrication **2222** includes a mask writer. A mask writer converts the RDF to an image on a substrate, such as a mask (reticle) **2223** or a semiconductor wafer **2233**. The IC design layout diagram **2211** is manipulated by mask data preparation **2221** to comply with particular characteristics of the mask writer and/or requirements of IC fab **2230**. In FIG. **22**, data preparation **2221** and mask fabrication **2222** are illustrated as separate elements. In some embodiments, data preparation **2221** and mask fabrication **2222** can be collectively referred to as mask data preparation.

[0278] In some embodiments, data preparation **2221** includes optical proximity correction (OPC) which uses lithography enhancement techniques to compensate for image errors, such as those that can arise from diffraction, interference, other process effects and the like. OPC adjusts IC design layout diagram **2211**. In some embodiments, data preparation **2221** includes further resolution enhancement techniques (RET), such as off-axis illumination, sub-resolution assist features, phase-shifting masks, other suitable techniques, and the like or combinations thereof. In some embodiments, inverse lithography technology (ILT) is also used, which treats OPC as an inverse imaging problem.

[0279] In some embodiments, data preparation **2221** includes a mask rule checker (MRC) that checks the IC design layout diagram **2211** that has undergone processes in OPC with a set of mask creation rules which contain certain geometric and/or connectivity restrictions to ensure sufficient margins, to account for variability in semiconductor manufacturing processes, and the like. In some embodiments, the MRC modifies the IC design layout diagram **2211** to compensate for limitations during mask fabrication **2222**, which may undo part of the modifications performed by OPC in order to meet mask creation rules.

[0280] In some embodiments, data preparation **2221** includes lithography process checking (LPC) that simulates processing that will be implemented by IC fab **2230** to fabricate IC device **2240**. LPC simulates this processing based on IC design layout diagram **2211** to create a simulated manufactured device, such as IC device **2240**. The processing parameters in LPC simulation can include parameters associated with various processes of the IC manufacturing cycle, parameters associated with tools used for manufacturing the IC, and/or other aspects of the manufacturing process. LPC takes into account various factors, such as aerial image contrast, depth of focus ("DOF"), mask error enhancement factor ("MEEF"), other suitable factors, and the like or combinations thereof. In some embodiments, after a simulated manufactured device has been created by LPC, if the simulated device is not close enough in shape to satisfy design rules, OPC and/or MRC are be repeated to further refine IC design layout diagram **2211**.

[0281] It should be understood that the above description of data preparation **2221** has been simplified for the purposes of clarity. In some embodiments, data preparation **2221** includes additional features such as a logic operation (LOP) to modify the IC design layout diagram **2211** according to manufacturing rules. Additionally, the processes applied to IC design layout diagram **2211** during data preparation **2221** may be executed in a variety of different orders.

[0282] After data preparation **2221** and during mask fabrication **2222**, a mask **2223** or a group of masks **2223** are fabricated based on the modified IC design layout diagram **2211**. In some embodiments, mask fabrication **2222** includes performing one or more lithographic exposures based on IC design layout diagram **2211**. In some embodiments, an electron-beam (e-beam) or a mechanism of multiple e-beams is used to form a pattern on a mask (photomask or reticle) **2223** based on the modified IC design layout diagram **2211**. Mask **2223** can be formed in various technologies. In some embodiments, mask **2223** is formed using binary technology. In some embodiments, a mask pattern includes opaque regions and transparent regions. A radiation beam, such as an ultraviolet (UV) beam, used to expose the image sensitive material layer (for example, photoresist) which has been coated on a wafer, is blocked by the opaque region and transmits through the transparent regions. In one example, a binary mask version of mask **2223** includes a transparent substrate (for example, fused quartz) and an opaque material (for example, chromium) coated in the opaque regions of the binary mask. In another example, mask **2223** is formed using a phase shift technology. In a phase shift mask (PSM) version of mask **2223**, various features in the pattern formed on the phase shift mask are configured to have proper phase difference to enhance the resolution and imaging quality. In various examples, the phase shift mask can be attenuated PSM or alternating PSM. The mask(s) generated by mask fabrication **2222** is used in a variety of processes. For example, such a mask(s) is used in an ion implantation process to form various doped regions in semiconductor wafer **2233**, in an etching process to form various etching regions in semiconductor wafer **2233**, and/or in other suitable processes.

[0283] IC fab **2230** includes wafer fabrication **2232**. IC fab **2230** is an IC fabrication business that includes one or more manufacturing facilities for the fabrication of a variety of different IC products. In some embodiments, IC Fab **2230** is a semiconductor foundry. For example, there may be a manufacturing facility for the front end fabrication of a plurality of IC products (front-end-of-line (FEOL) fabrication), while a second manufacturing facility may provide the back end fabrication for the interconnection and packaging of the IC products (back-end-of-line (BEOL) fabrication), and a third manufacturing facility may provide other services for the foundry business.

[0284] IC fab **2230** uses mask(s) **2223** fabricated by mask house **2220** to fabricate IC device **2240**. Thus, IC fab **2230** at least indirectly uses IC design layout diagram **2211** to fabricate IC device **2240**. In some embodiments, semiconductor wafer **2233** is fabricated by IC fab **2230** using mask(s) **2223** to form IC device **2240**. In some embodiments, the IC fabrication includes performing one or more lithographic exposures based at least indirectly on IC design layout diagram **2211**. Semiconductor wafer **2233** includes a silicon substrate or other proper substrate having material layers formed thereon. Semiconductor wafer **2233** further includes one or more of various doped regions, dielectric features, multilevel interconnects, and the like (formed at subsequent manufacturing steps).

[0285] Moreover, various circuits or devices to implement the transistors in the aforementioned embodiments are within the contemplated scope of the present disclosure. In some embodiments of this document, at least one of the transistors is implemented with at least one MOS transistor, at least one bipolar junction transistor (BJT), etc., or the combination thereof. Various circuits or devices to implement the transistors in the aforementioned embodiments are within the contemplated scope of the present disclosure.

[0286] In some embodiments, an integrated circuit is disclosed and includes a first conductive structure having a fork shape in a film structure and in a first semiconductor layer, including: a root portion of the first conductive structure and multiple tine portions of the first conductive structure that are arranged in the first semiconductor layer; and a neck portion of the first conductive structure surrounded by the film structure. The integrated circuit further includes a second conductive structure that is adjacent to the first conductive structure and has first and second portions that are stacked along a first direction. The first portion of the second conductive structure is surrounded by the film structure and the second portion of the second conductive structure is in the first semiconductor layer. A third conductive structure in the integrated circuit has a horizontal structure and a vertical structure. The horizontal structure extends in a second direction in a second semiconductor layer above the film structure and the first semiconductor layer and the vertical structure passes through the second semiconductor layer and the film structure to contact a first conductive rail in the first semiconductor layer. The first conductive rail and the tine portions are apart from the horizontal structure along the first direction by a same distance.
[0287] In some embodiments, along the second direction a width of the first portion of the second conductive structure is smaller than a width of the second portion of the second conductive structure.
[0288] In some embodiments, the first conductive structure is interposed between the second conductive structure and the third conductive structure.
[0289] In some embodiments, a width of the neck portion of the first conductive structure is greater than a distance between a boundary of a first portion in the tine portions and a boundary of a second portion in the tine portions. The first and second portions in the tine portions are separated from each other.
[0290] In some embodiments, the tine portions are configured to transmit signals.
[0291] In some embodiments, the second portion of the second conductive structure is configured to transmit a power supply voltage.
[0292] In some embodiments, the integrated circuit further includes multiple dielectric structures disposed between the tine portions, the second conductive structure, and the first conductive rail.
[0293] In some embodiments, an integrated circuit is also disclosed. The integrated circuit includes a first pair of conductive rails configured to transmit supply voltages and arranged in a first semiconductor layer; a second pair of conductive rails arranged in the first semiconductor layer and interposed between the first pair of conductive rails, configured to transmit a data signal; and a first conductive structure disposed on the second pair of conductive rails and having a protrusion in the first semiconductor layer. The protrusion has a first surface contacting a first rail in the second pair of conductive rails and a second surface contacting a second rail in the second pair of conductive rails.
[0294] In some embodiments, the integrated circuit further includes a first conductive segment arranged on a first rail in the first pair of conductive rails a second conductive segment arranged on a second rail in the first pair of conductive rails. The protrusion has a third surface below surfaces where the first and second conductive segments contact the first pair of conductive rails.
[0295] In some embodiments, widths of the first and second conductive segments are smaller than a width of the first pair of conductive rails long a horizontal direction.
[0296] In some embodiments, widths of the second pair of conductive rails are different from widths of the first pair of conductive rails.
[0297] In some embodiments, widths of the second pair of conductive rails are smaller from widths of the first pair of conductive rails.
[0298] In some embodiments, the integrated circuit further includes a second conductive structure disposed on one of rail in the second pair of conductive rails and a signal rail. A corner of the first conductive structure is separated from a corresponding corner of the second conductive structure by a distance that is in a range of half of a poly pitch to one poly pitch in the integrated circuit.

[0299] In some embodiments, the first and second conductive structures are in shape of a square.
[0300] In some embodiments, an integrated circuit is provided and includes a first signal rail extending in a first direction; multiple conductive rails extending in a second direction and each arranged apart from the first signal rail by a first distance along a third direction; and a first conductive segment electrically coupled to at least two rails, having smaller width, in the conductive rails and having a height smaller than the first distance. The first conductive segment is interposed between the first signal rail and the at least two rails and disposed at a central point of the conductive rails along the first direction.
[0301] In some embodiments, the integrated circuit further includes a via coupled between the first signal rail and one rail in the conductive rails. A height of the via along the third direction is greater than the height of the first conductive segment.
[0302] In some embodiments, the integrated circuit further includes multiple second segments disposed on two rails in the conductive rails, wherein a height of the second segments is smaller than the first distance.
[0303] In some embodiments, widths of the second segments are smaller than widths of the two rails in the conductive rails.
[0304] In some embodiments, the widths of the two rails in the conductive rails are greater than widths of the at least two rails in the conductive rails.
[0305] In some embodiments, a second distance between first and second boundaries of the at least two rails in the conductive rails is greater than a width of the first conductive segment.
[0306] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

Claims

1-20. (canceled)
21. An integrated circuit, comprising: a first conductive structure in a film structure and in a first metal layer, comprising: a plurality of first conductive rails that are arranged in the first metal layer; and a conductive segment surrounded by the film structure; a second conductive structure that is adjacent to the first conductive structure and has first and second portions that are stacked along a first direction, wherein the first portion of the second conductive structure is surrounded by the film structure and the second portion of the second conductive structure is in the first metal layer; and a third conductive structure having a first structure in a second metal layer and a second structure and surrounded by the film structure, wherein the second structure is coupled between the first structure and a second conductive rail in the first metal layer, wherein along a second direction, a width of the first structure is greater than a width of the second structure.
22. The integrated circuit of claim 21, wherein along the second direction, the width of the first structure is greater than a width of the second conductive rail.
23. The integrated circuit of claim 21, wherein along the second direction, a width of the first portion of the second conductive structure is smaller than a width of the second portion of the second conductive structure.
24. The integrated circuit of claim 21, wherein the first conductive structure is interposed between the second conductive structure and the third conductive structure.
25. The integrated circuit of claim 21, wherein a width of the conductive segment of the first

conductive structure is greater than a distance between a boundary of a first rail in the plurality of first conductive rails and a boundary of a second rail in the plurality of first conductive rails, wherein the first rail and the second rail in the plurality of first conductive rails are separated from each other.

26. The integrated circuit of claim 21, wherein the plurality of first conductive rails are configured to transmit signals, wherein the second portion of the second conductive structure is configured to transmit a power supply voltage.

27. The integrated circuit of claim 21, further comprising: a plurality of dielectric structures disposed between the plurality of first conductive rails, the second conductive structure, and the second conductive rail.

28. An integrated circuit, comprising: a first pair of conductive rails configured to transmit supply voltages and arranged in a first metal layer; a second pair of conductive rails arranged in the first metal layer and interposed between the first pair of conductive rails, configured to transmit a data signal; and a first conductive structure disposed on the second pair of conductive rails and having a part interposed into the first metal layer, wherein the part of the first conductive structure is disposed in a space between the second pair of conductive rails.

29. The integrated circuit of claim 28, further comprising: a third conductive rail arranged between the a first rail of the first pair of conductive rails and a first rail of the second pair of conductive rails; and a fourth conductive rail arranged between the a second rail of the first pair of conductive rails and a second rail of the second pair of conductive rails.

30. The integrated circuit of claim 29, further comprising: a first conductive segment arranged on a first rail in the first pair of conductive rails; and a second conductive segment arranged on a second rail in the first pair of conductive rails.

31. The integrated circuit of claim 30, wherein widths of the first and second conductive segments are smaller than a width of the first pair of conductive rails long a horizontal direction.

32. The integrated circuit of claim 30, wherein each of the first conductive segment and the second conductive segment is in shape of a square.

33. The integrated circuit of claim 28, wherein widths of the second pair of conductive rails are different from widths of the first pair of conductive rails.

34. The integrated circuit of claim 33, wherein the widths of the second pair of conductive rails are smaller from the widths of the first pair of conductive rails.

35. An integrated circuit, comprising: a first signal rail extending in a first direction; a plurality of conductive rails extending in a second direction and each arranged apart from the first signal rail by a first distance along a third direction; a first conductive segment electrically coupled to at least two rails; and a via overlapped with the first signal rail and one of the plurality of conductive rails, wherein a height of the first conductive segment along the third direction is smaller than a height of the via.

36. The integrated circuit of claim 35, wherein a width of the first conductive segment along the second direction is greater than a width of the via.

37. The integrated circuit of claim 36, further comprising: a plurality of second segments disposed on two rails in the plurality of conductive rails, wherein a height of the plurality of second segments is smaller than the first distance.

38. The integrated circuit of claim 37, wherein widths of the plurality of second segments are smaller than widths of the two rails in the plurality of conductive rails.

39. The integrated circuit of claim 38, wherein the widths of the two rails in the plurality of conductive rails are greater than widths of the at least two rails in the plurality of conductive rails.

40. The integrated circuit of claim 35, wherein a second distance between first and second boundaries of the at least two rails in the plurality of conductive rails is greater than a width of the first conductive segment.