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(54) **DATA PROCESSING DEVICE, DATA DRIVING DEVICE, AND DISPLAY DEVICE INCLUDING THE SAME**

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(57) **ABSTRACT**

A data processing device includes a first main communication circuit configured to transmit configuration data and image data via a first communication line; a first auxiliary communication circuit configured to send and receive a lock signal via a second communication line; and a register configured to store configuration data based on vendor identification information. The first main communication circuit is configured to transmit a first request packet requesting vendor identification information, select configuration data based on the received vendor identification information, and transmit the selected configuration data via the first communication line.

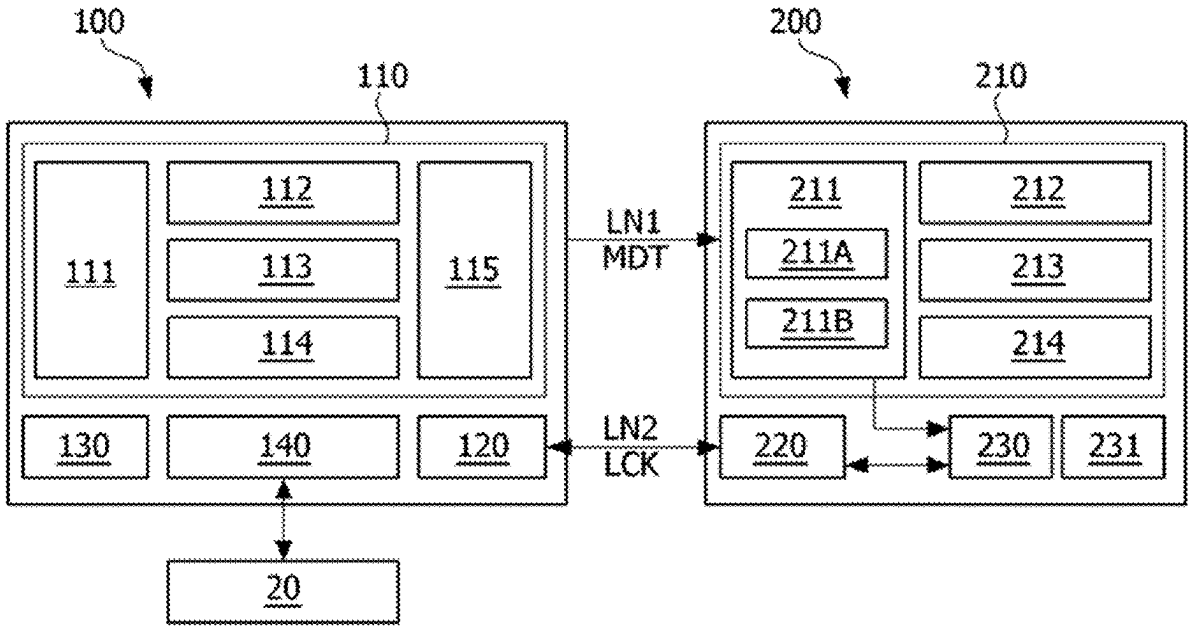


FIG. 1

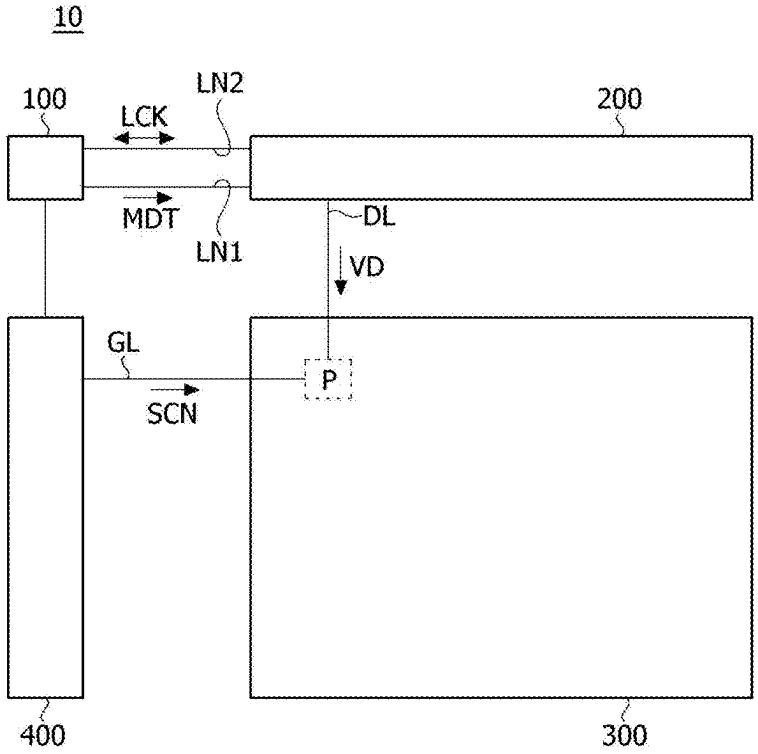


FIG. 2

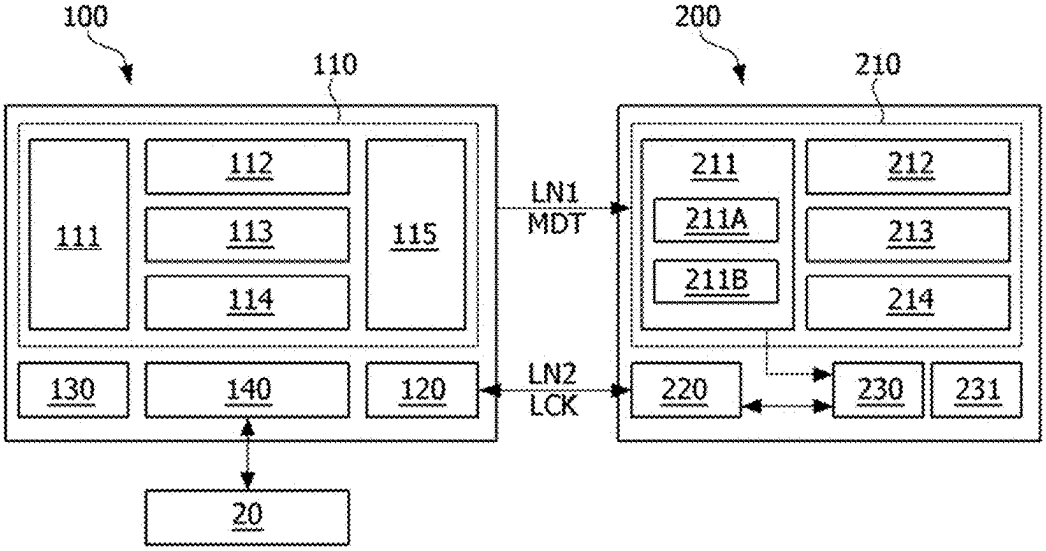

100
110
200
210
111
112
113
114
115
LN1
MDT
211
211A
211B
212
213
214
130
140
120
LN2
LCK
220
230
231
20

FIG. 3

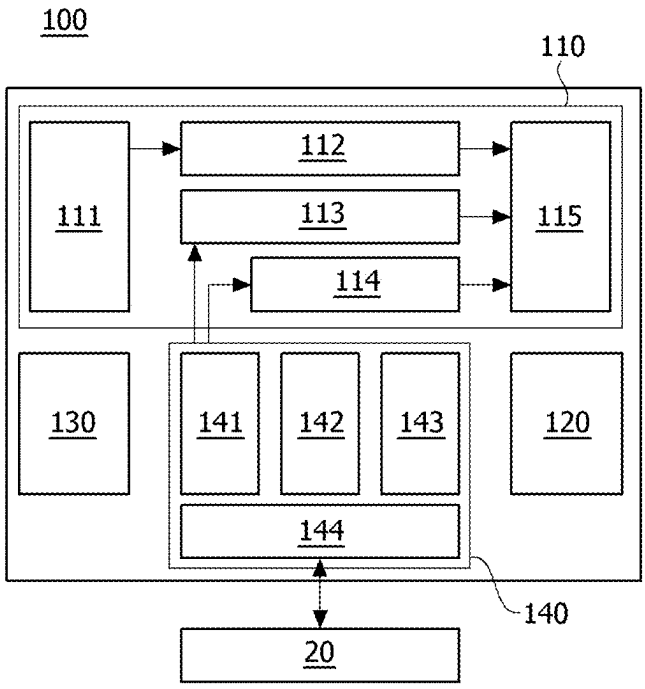


FIG. 4

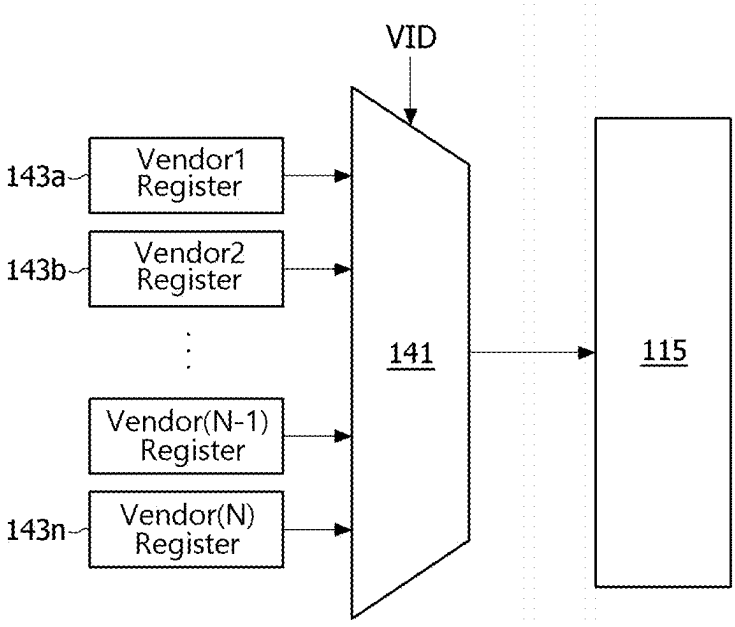

VID
143a
Vendor1 Register
143b
Vendor2 Register
Vendor(N-1) Register
143n
Vendor(N) Register
141
115

FIG. 5

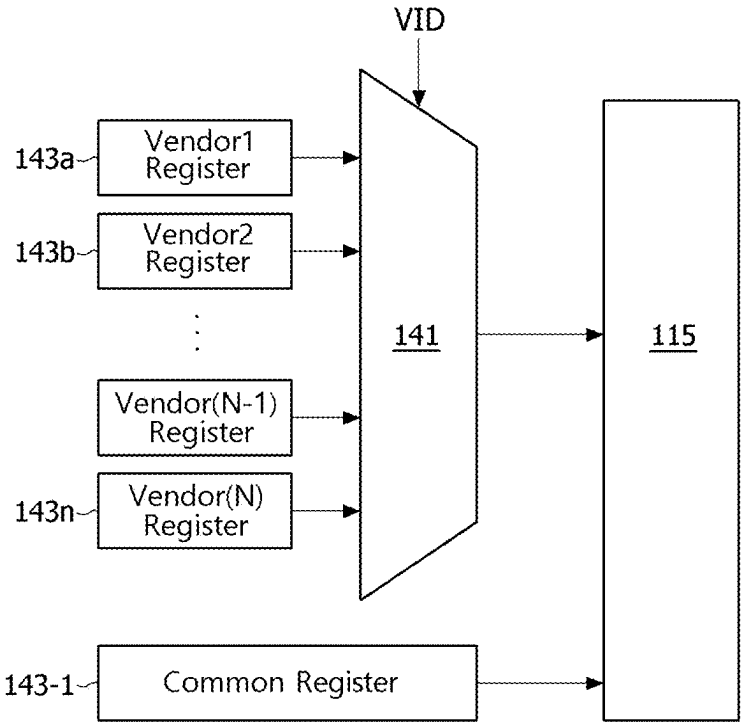

VID
143a
Vendor1 Register
143b
Vendor2 Register
Vendor(N-1) Register
143n
Vendor(N) Register
141
115
143-1
Common Register

FIG. 6

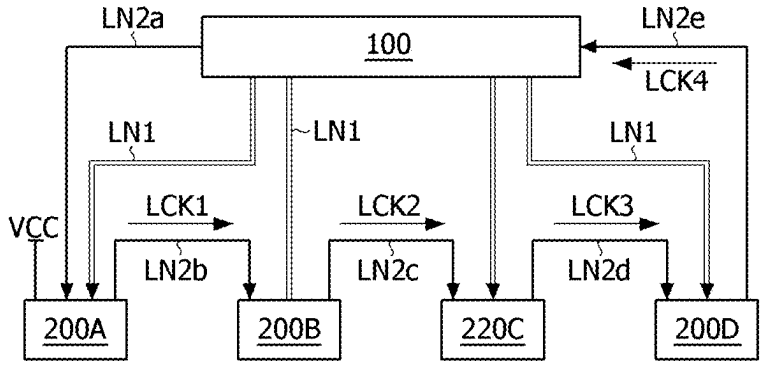

LN2a
100
LN2e
LCK4
LN1
LN1
LN1
LCK1
LCK2
LCK3
VCC
LN2b
LN2c
LN2d
200A
200B
220C
200D

FIG. 7

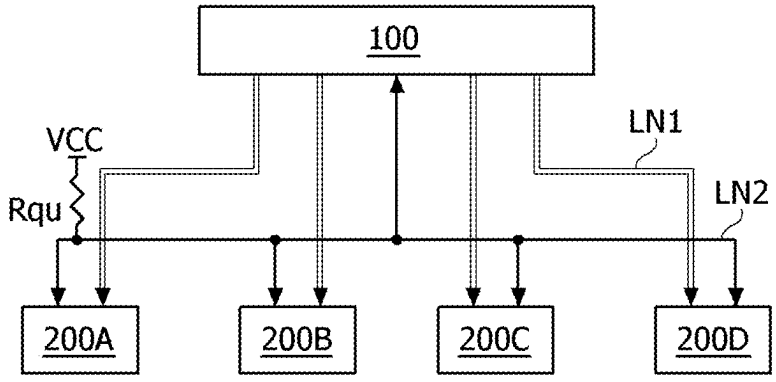

100
LN1
VCC
Rqu
LN2
200A
200B
200C
200D

FIG. 8

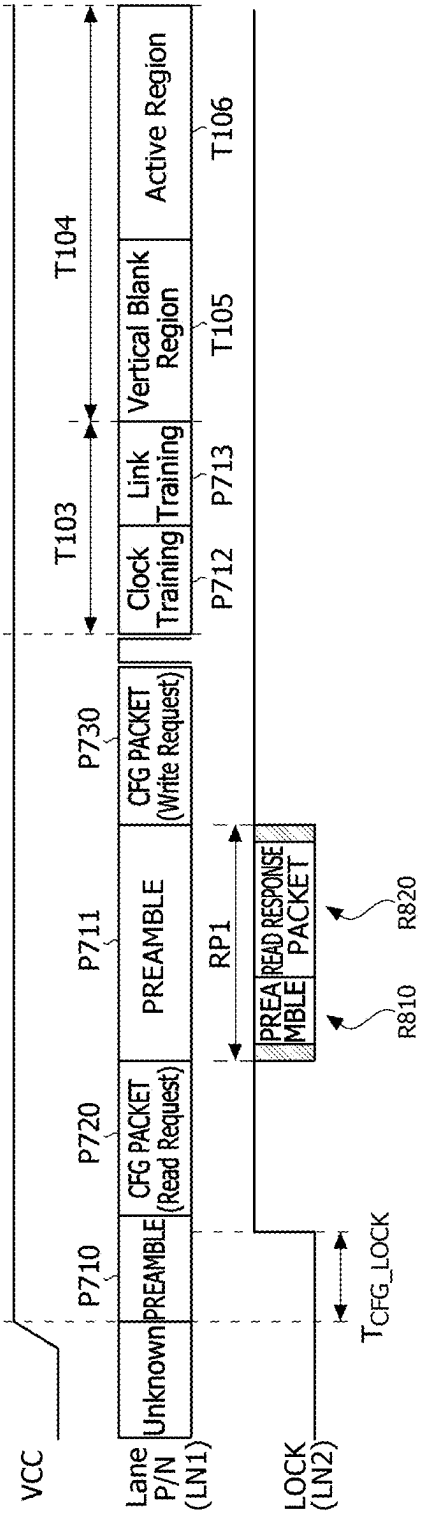

Display Mode (T102)
CFG Mode (T101)
T103
T104
T105
T106
Active Region
Vertical Blank Region
Link Training
Clock Training
P712
P713
P730
CFG PACKET (Write Request)
P711
PREAMBLE
RP1
P720
CFG PACKET (Read Request)
P710
PREAMBLE
Unknown
READ RESPONSE PACKET
PREA MBLE
R820
R810
VCC
Lane P/N (LN1)
LOCK (LN2)
TCFG_LOCK

FIG. 9

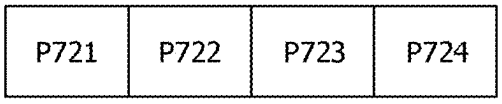


FIG. 10

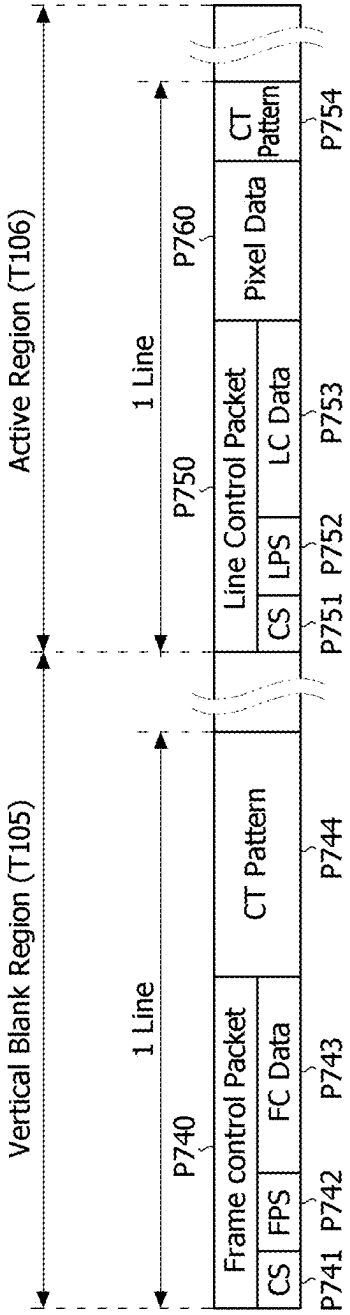
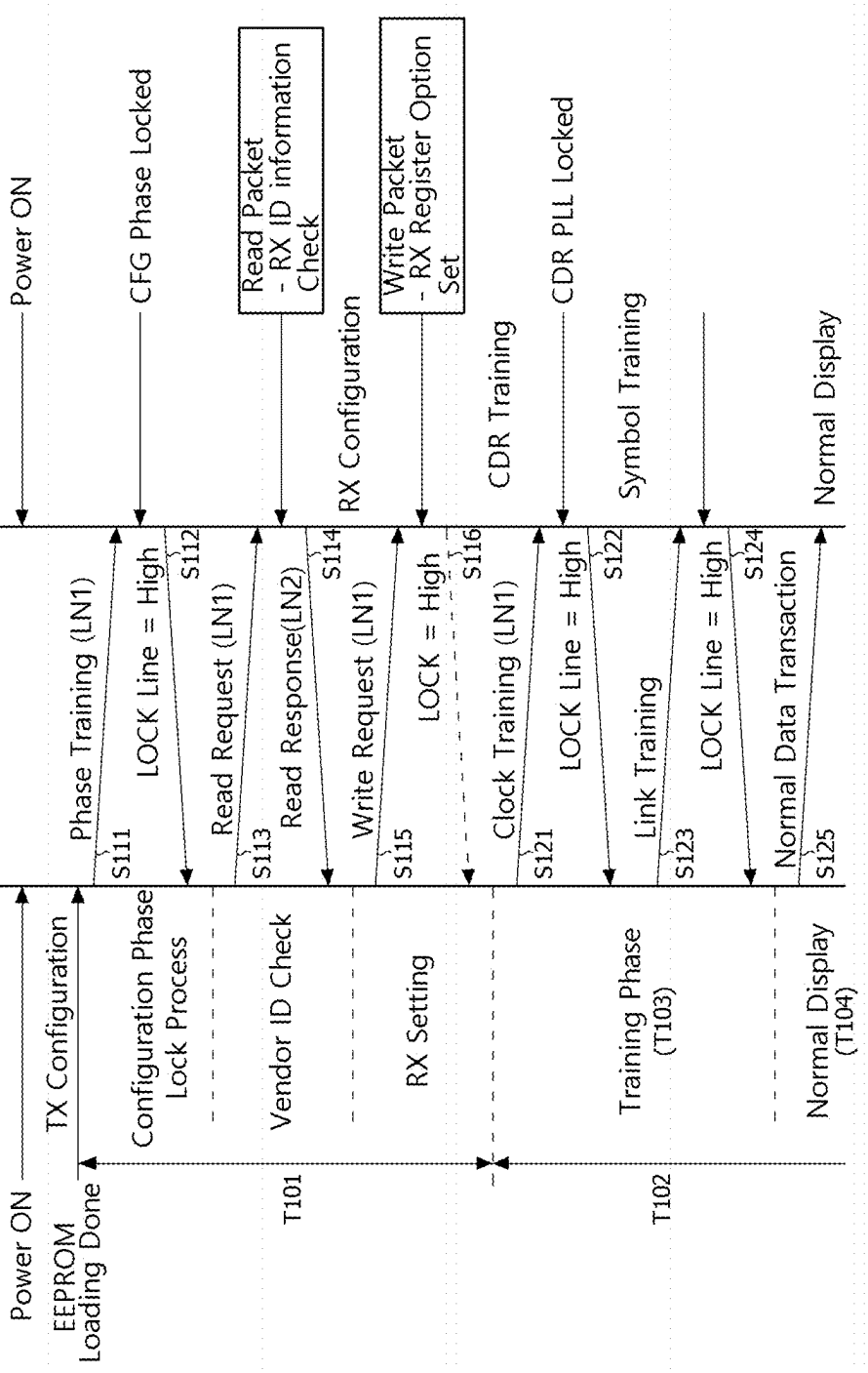

Vertical Blank Region (T105)
Active Region (T106)
1 Line
P740
1 Line
P750
P760
Frame control Packet
CT Pattern
Line Control Packet
Pixel Data
CT Pattern
CS
FPS
FC Data
CS
LPS
LC Data
P741
P742
P743
P744
P751
P752
P753
P754

FIG. 11


100
200
Power ON
EEPROM Loading Done
TX Configuration
Configuration Phase
Lock Process
Vendor ID Check
RX Setting
Training Phase (T103)
Normal Display (T104)
T101
T102
Power ON
CFG Phase Locked
Read Packet - RX ID information Check
RX Configuration
Write Packet - RX Register Option Set
CDR Training
CDR PLL Locked
Symbol Training
Normal Display
Phase Training (LN1)
S111
LOCK Line = High
S112
Read Request (LN1)
S113
Read Response(LN2)
S114
Write Request (LN1)
S115
LOCK = High
S116
Clock Training (LN1)
S121
LOCK Line = High
S122
Link Training
S123
LOCK Line = High
S124
Normal Data Transaction
S125

DATA PROCESSING DEVICE, DATA DRIVING DEVICE, AND DISPLAY DEVICE INCLUDING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priorities of Korean Patent Applications No. 10-2024-0022499, filed on Feb. 16, 2024 and No. 10-2025-0019220, filed on Feb. 14, 2025, which are hereby incorporated by reference in their entirety.

BACKGROUND

Field of the Disclosure

[0002] The present disclosure relates to techniques for driving a display device.

Description of the Background

[0003] Display panels are composed of a plurality of pixels arranged in a matrix. Each pixel may have colors such as R (red), G (green), and B (blue), and displays images on the display panel by emitting light according to the grayscale based on image data.

[0004] The image data is transferred from a data processing device, such as a timing controller, to a data driving device, such as a source driver. While the image data is transmitted as digital values, the data driving device converts the image data into analog voltages to drive each pixel.

[0005] Unlike the timing controller, source drivers do not have an external memory for setting options, so the options are set using the pins or the timing controller. In general, panel manufacturers or set manufacturers employ a single set of configuration option values regardless of the type of the source drivers, and the configuration options of the source drivers for each vendor (manufacturer) are not separately managed.

[0006] However, for various reasons, the configuration options of the source drivers are manufactured differently by each vendor (manufacturer). Therefore, it is necessary to set the options differently, depending on which vendor produced the source drivers that make up the system.

SUMMARY

[0007] The present disclosure is to provide a data processing device, a data driving device, and a display device including the same, which are capable of setting the options of the source drivers differently by vendors.

[0008] The problems to be solved by the present disclosure are not limited to those mentioned above, and other problems not mentioned will be clearly understood by those skilled in the art from the following description.

[0009] A data processing device according to one aspect of the present disclosure includes: a first main communication circuit configured to transmit configuration data and image data via a first communication line; a first auxiliary communication circuit configured to send and receive signals via a second communication line; and a plurality of registers configured to store configuration data for each vendor, wherein the first main communication circuit is configured to: transmit a first configuration packet requesting vendor identification information, select configuration data from the plurality of registers based on received vendor identification information, and transmit the selected configuration data via the first communication line.

[0010] A data driving device according to one aspect of the present disclosure includes: a second main communication circuit configured to receive configuration data and image data via a first communication line; a second auxiliary communication circuit configured to send and receive signals via a second communication line; and a reception control part (reception controller) configured to control the second main communication circuit and the second auxiliary communication circuit, wherein the reception control part is configured to: transmit its own vendor identification packet via the second communication line in response to receiving a first configuration packet requesting vendor identification information via the first communication line.

[0011] A display device according to one aspect of the present disclosure includes: a data processing device; and a plurality of data driving devices, wherein the data processing device is configured to send a first configuration packet that requests vendor identification information to each of the plurality of data driving devices, the plurality of data driving devices each is configured to transmit its vendor identification information to the data processing device in response to the first configuration packet, and the data processing device is configured to transmit selected configuration data based on received vendor identification information to each of the plurality of data driving devices.

[0012] According to the aspects, the option of the source driver may be set differently for each vendors by confirming the vendor identification information. As a result, a high-speed data transmission environment may be optimized.

[0013] In addition, it is possible to manage options for each vendor without increasing production cost and complexity.

[0014] The effects of the present disclosure are not limited to the above-mentioned effects, and other effects that are not mentioned will be apparently understood by those skilled in the art from the following description and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The above and other objects, features, and advantages of the present disclosure will become more apparent to those of ordinary skill in the art by describing exemplary aspects thereof in detail with reference to the attached drawings, in which:

[0016] FIG. **1** is a conceptual diagram of a display device according to an aspect of the present disclosure;

[0017] FIG. **2** is a configuration diagram of a data processing device and a data driving device according to an aspect of the present disclosure;

[0018] FIG. **3** is a diagram illustrating a display device according to an aspect of the present disclosure;

[0019] FIG. **4** is a diagram illustrating an option selection circuit of the data processing device according to an aspect of the present disclosure;

[0020] FIG. **5** is a modified example of FIG. **4**;

[0021] FIG. **6** is a diagram illustrating the main communication and the auxiliary communication between the data processing device and the data driving device according to an aspect of the present disclosure;

[0022] FIG. **7** is a diagram illustrating the main communication and the auxiliary communication between the data

processing device and the data driving device according to another aspect of the present disclosure;

[0023] FIG. **8** is a diagram illustrating the sequence of transmission signals according to an aspect of the present disclosure;

[0024] FIG. **9** is a diagram illustrating a structure of a first configuration packet according to an aspect of the present disclosure;

[0025] FIG. **10** is a configuration diagram of blank data and line data according to an aspect of the present disclosure; and

[0026] FIG. **11** is a diagram showing the data flow of the data processing device and the data driving device according to an aspect of the present disclosure.

DETAILED DESCRIPTION

[0027] The advantages and features of the present disclosure, and methods of achieving them will be apparent from the aspects described in detail below in conjunction with the accompanying drawings. However, the present disclosure is not limited to the following aspects, which may be implemented in various different forms; rather, the present aspects are provided to make the disclosure of the present disclosure complete and to allow those skilled in the art to fully understand the scope of the present disclosure, and the present disclosure is defined only within the scope of the appended claims.

[0028] The shapes, sizes, proportions, angles, numbers and the like shown in the accompanying drawings for the purpose of describing the aspects of the present disclosure are merely examples, and the present disclosure is not limited thereto. Like reference numerals generally denote like elements throughout the present specification. Further, in describing the present disclosure, detailed descriptions of known related technologies may be omitted so as not to unnecessarily obscure the subject matter of the present disclosure.

[0029] The following aspects may be combined or associated with each other in whole or in part, and various types of interlocking and driving are technically possible. The aspects may be implemented independently of each other or together in an interrelated relationship.

[0030] Hereinafter, various aspects of the present disclosure will be described in detail with reference to the accompanying drawings.

[0031] FIG. **1** is a conceptual diagram of a display device according to an aspect of the present disclosure.

[0032] Referring to FIG. **1**, a display device **10** may include a data processing device **100**, a data driving device **200**, a display panel **300**, and a gate driving device **400**.

[0033] The data processing device **100** may receive image data from the other device. The other device may be a host that generates the image data.

[0034] The data processing device **100** may process the image data received from the other device to be suitable for the data driving device **200**, and transmit the processed image data to the data driving device **200**. The data processing device **100** may perform digital gamma correction processing on a greyscale value of each pixel included in the image data or may perform compensation processing on the greyscale value to match the characteristics of the pixel.

[0035] The data driving device **200** may receive the image data from the data processing device **100**, generate data voltages VD according to the greyscale values of the pixels included in the image data, and supply the data voltages VD to the pixels P.

[0036] A plurality of pixels P may be arranged on the display panel **300**. In addition, each pixel P may be connected to the data driving device **200** via a data line DL and to the gate driving device **400** via a gate line GL.

[0037] The display panel **300** may be a panel of a flat-panel display device, such as a liquid crystal display (LCD), a field emission display (FED), a plasma display panel (PDP), an organic light-emitting display (OLED), or a non-organic light-emitting display.

[0038] Each pixel P may include a transistor, where the gate terminal of the transistor may be connected to the gate line GL, and the source terminal thereof may be connected to the data line DL. When the gate driving device **400** supplies a scan signal SCN to the gate line GL, the transistor turns on, connecting the data line DL to the pixel P. After the data line DL is connected to the pixel P, the data voltage VD supplied by the data driving device **200** is transferred to the pixel P.

[0039] To synchronize the timing of the gate driving device **400** and the data driving device **200**, the data processing device **100** may send a timing control signal to the gate driving device **400** and the data driving device **200**.

[0040] The data processing device **100** may send a gate control signal to the gate driving device **400**. The gate control signal may include the aforementioned timing control signal. The gate driving device **400** may generate the scan signal SCN based on the gate control signal and supply the scan signal SCN to the pixel P via the gate line GL.

[0041] At least two types of communication lines LN**1** and LN**2** may be arranged between the data processing device **100** and the data driving device **200**. The data processing device **100** may send a first communication signal MDT via the first communication line LN**1** and may send or receive a second communication signal LCK via the second communication line LN**2**.

[0042] The first communication line LN**1** may be defined as a main communication line, and the second communication line LN**2** may be defined as an auxiliary communication line. The first communication signal MDT may be defined as a main communication signal, and the second communication signal LCK may be defined as an auxiliary communication signal.

[0043] The data processing device **110** may send the image data and the timing control signals to the data driving device **120** via the main communication signal MDT, and the data driving device **120** may send status information to the data processing device **110** via the auxiliary communication signal LCK.

[0044] When the data processing device **100** or the data driving device **200** performs a specific operation, it may mean that various hardware included in the data processing device **100** or the data driving device **200**, for example, a controller such as a micro controlling unit (MCU), a field programmable gate array (FPGA), an application specific integrated circuit (ASIC), and/or a microprocessor, performs a specific operation. When the data processing device **100** or the data driving device **200** performs a specific operation, it may mean that the controller controls the other hardware to perform a specific operation.

[0045] FIG. **2** is a configuration diagram of the data processing device and the data driving device according to

an aspect. FIG. **3** is a diagram illustrating a display device according to an aspect of the present disclosure. FIG. **4** is a diagram illustrating an option selection circuit of the data processing device according to an aspect of the present disclosure. FIG. **5** is a modified example of FIG. **4**.

[0046] Referring to FIGS. **2** and **3**, the data processing device **100** may include a first main communication circuit **110**, a first auxiliary communication circuit **120**, and a transmission control part **130**. The data driving device **200** may include a second main communication circuit **210**, a second auxiliary communication circuit **220**, and a reception control part **230**. The first main communication circuit **110** may communicate with the second main communication circuit **210** via the first communication line LN**1**, and the first auxiliary communication circuit **120** may communicate with the second auxiliary communication circuit **220** via the second communication line LN**2**.

[0047] The first main communication circuit **110** may send the main communication signal MDT to the data driving device **200** via the first communication line LN**1**. The first main communication circuit **110** may send image data and first control data during an active interval via the first communication line LN**1** and may send second control data during a blank interval via the first communication line LN**1**.

[0048] The data driving device **200** may drive the pixels of the display panel according to the image data. The first control data may include control values applied on a line-by-line or pixel-by-pixel basis to the display panel, while the second control data may include control values applied over longer cycles than line-by-line or pixel-by-pixel, or control values applied on a frame-by-frame basis.

[0049] The first main communication circuit **110** may send configuration data at a first data rate via the first communication line LN**1**. Subsequently, the first main communication circuit **110** may send the image data, the first control data, and the second control data at a second data rate, higher than the first data rate, via the first communication line LN**1**. The mode in which communication is performed at the first data rate may be defined as a low-speed communication mode, and the mode in which communication is performed at the second data rate may be defined as a high-speed communication mode.

[0050] The first main communication circuit **110** may receive image data, control data, and configuration data, convert the received image data, control data, and configuration data according to different encoding methods, and output the converted data. The first main communication circuit **110** may include a first high-speed communication circuit for converting image data and control data, and a second low-speed communication circuit for converting configuration data.

[0051] The first high-speed communication circuit may receive image data and control data, convert the received image data and control data according to different encoding methods, and output the converted data. The first high-speed communication circuit may include a receiver **111** that receives image data from an external source, a first data converter **112**, a second data converter **113**, and a transmitter **115**.

[0052] The first data converter **112** may encode the image data and transmit it to the transmitter **115**. The second data converter **113** may encode the control data and transmit it to the transmitter **115**. The encoding method of the first data converter **112** and the encoding method of the second data converter **113** may be different from each other, but they are not limited thereto.

[0053] The first low-speed communication circuit may be configured to include a third data converter **114** and the transmitter **115**. The first high-speed communication circuit and the first low-speed communication circuit may share the transmitter **115**. The transmitter **115** may achieve the effect of transmitting at a low speed by using various methods such as increasing data transmitted from the first low-speed communication circuit. However, the aspect is not limited to that described above. For example, the high-speed transmitter of the first high-speed communication circuit and the low-speed transmitter of the first low-speed communication circuit may be provided separately from each other.

[0054] The third data converter **114** of the first low-speed communication circuit may encode the configuration data in a predetermined manner and then transmit the same through the transmitter **115**. The configuration data, which is transmitted at a low speed, may include the configuration values for the data driving device **200** required before high-speed communication. For example, the configuration data may include configuration values for the circuits in the data driving device **200** that perform high-speed communication.

[0055] Referring to FIG. **3**, the data processing device **100** may include an option selection circuit **140**. The option selection circuit **140** may include a plurality of registers **143** in which a plurality of configuration data are respectively stored for each vendor, and a first data selector **141** for selecting one of the configuration data stored in the plurality of registers **143** according to a vendor identification number from the data driving device **200**.

[0056] The option selection circuit **140** may be configured as a separate circuit from the first main communication circuit **110** or may be included in the first main communication circuit **110**. The option selection circuit **140** may further include an option storage part in which configuration options of the receiver **111**, the data converter **112**, **113**, **114**, and the transmitter **115** are stored.

[0057] The plurality of registers **143** may each store configuration data for each vendor. The configuration data may be set differently for each vendor. This is because even for the same products, their internal configurations may be newly developed and applied for each vendor, and even for the same specifications, their characteristics may differ due to differences in analog circuit design methods for each vendor. For example, different vendors may have different bias voltages, different equalizer design techniques, different design techniques of a clock recovery part, and different internal configurations of driver ICs (e.g., digital-to-analog converters). As a result, it may be difficult to optimize if a high-speed data environment is built with uniform configuration data without considering vendor-specific options.

[0058] The optional selection circuit **140** may further include an input/output interface **144** that is connected to the external memory **20**. The input/output interface **144** may load configuration values stored in the external memory **20** when power is applied. Data loaded through the input/output interface **144** may be stored in each of the plurality of registers **143**. The input/output interface **144** may be any one of I2C, SPI, UART, or various memory interfaces.

[0059] The external memory **20** may include any one of a wide range of volatile or nonvolatile memories, including a random access memory (RAM), a read-only memory

(ROM), a non-volatile random access memory (NVRAM), an electrically erasable and programmable ROM (EEPROM), a FLASH memory, and the like.

[0060] The data processing device **100** may transmit a first configuration packet requesting identification information to the data driving device **200** in configuration mode. For example, the transmission control part **130** may control the first main communication circuit **110** and the option selection circuit **140**. The transmission control part **130** may control the first main communication circuit **110** to transmit the first configuration packet in the configuration mode.

[0061] The identification information may include vendor identification information, product codes, and the like. The vendor identification information may be unique identification information (vendor specific information) of the vendor (manufacturer) that manufactures the data driving devices.

[0062] The product codes are unique identification information (product specific information or product identification information) for a specific vendor's products to distinguish between the data driving devices from the same vendor.

[0063] The first auxiliary communication circuit **120** may receive vendor identification information and/or product code information transmitted from the data driving device **200**. The transmission control part **130** may control the first data selector **141** based on the received vendor identification information and/or product code information. For example, when each configuration data of a first vendor, a second vendor, and a third vendor are stored in the plurality of registers **143**, and the identification information of the second vendor is received, the transmission control part **130** may select a register **143** in which the configuration data of the second vendor is stored, and transmit the configuration data stored in that register **143** to the data driving device **200**.

[0064] According to an aspect, the selected configuration data based on the vendor identification information may be transmitted to the third data converter **114**. The third data converter **114** may encode the configuration data and transmit the same to the transmitter **115**. The third data converter **114** may transmit the configuration data by encoding it with a Menchester code, but the encoding method is not limited to this. However, the aspects are not limited thereto. If the configuration data is not encoded, the configuration data may be transmitted directly to the data driving device **200** through the transmitter **115** without passing through the second data converter **113**. In this case, a clock bit and a data error check bit may be added.

[0065] Referring to FIG. **4**, a plurality of registers **143***a* **143***b*, **143***n* may be connected to the first data selector **141** for each vendor. The first data selector **141** may include a multiplexer. The transmission control part **130** may input a control signal VID to the first data selector **141** so that a register **143** matching the received vendor identification information is selected. Therefore, the configuration data stored in the selected register **143** may be forwarded to the transmitter **115**.

[0066] Referring to FIG. **5**, the register **143** may be provided with a plurality of registers **143***a* **143***b*, and **143***n* in which individual configuration data are respectively stored, and a common register **143-1** in which common configuration data are stored.

[0067] The configuration data may include common configuration data applied equally to all vendors and individual configuration data set differently for each vendor.

[0068] The common configuration data may include data corresponding to basic operation options such as resolution, color depth, timing control, scramble enable/disable, and test mode.

[0069] The individual configuration data may be data that varies depending on each vendor's design techniques and processes, such as receiving PHY (e.g., clock data restoration method/equalizer), bias/current control, and buffer operating current (Amp Current), etc.

[0070] The common configuration data may be stored in the common register **143-1**, and the individual configuration data may be stored in a plurality of registers **143***a* **143***b*, **143***n*.

[0071] Upon receiving the vendor identification information, the transmission control part **130** may first transmit the common configuration data stored in the common register **143-1**. Subsequently, it may input a control signal VID to the first data selector **141** so that a register matching the vendor identification information is selected among the plurality of registers **143***a* **143***b*, **143***n*, and secondly transmit the configuration data stored in the selected register.

[0072] According to an aspect, some of the common configuration data stored in the external memory may be updated to specific vendor-only configuration data using firmware and then transmitted. For example, if the system environment changes, the changed information may be updated in the external memory **20** and then the updated configuration data may be stored in the common register **143-1**. By transmitting the updated configuration data in the common register **143-1** to the data driving device **200**, it is possible to set the communication environment with the latest updated information for the changed environment.

[0073] However, the aspect is not limited to that described above. For example, after confirming the vendor identification information, the configuration data stored in the common register **143-1** may be transmitted first, and then the configuration data in the individual register **143** may be updated using firmware and transmitted second. MCUs and MCU BUSs may be designed as ASICs to update data by applying such firmware.

[0074] Referring to FIGS. **2** and **3**, not only configuration data but also control data may be selected for each vendor based on the vendor identification information. Since not only the configuration data but also the frame control method and the line control method may be different for each vendor, it is necessary to optimize the control data together with the configuration data according to the vendor.

[0075] The control data as well as the configuration data may be stored in the plurality of registers **143**. Alternatively, the configuration data for each vendor and the control data for each vendor may be stored in different registers **143**.

[0076] The control data may include first control data and second control data. The first control data may include control values applied on a line-by-line or pixel-by-pixel basis to the display panel, while the second control data may include control values applied over longer cycles than line-by-line or pixel-by-pixel, or control values applied on a frame-by-frame basis. The first control data and the second control data may be stored in the plurality of registers **143** for each vendor. However, the aspect is not limited to that described above. The first control data and the second control data may be stored in different registers **143**.

[0077] The option selection circuit **140** may include a second data selector **142** for selecting control data matching

the vendor identification information from among a plurality of registers **143** in which the control data are stored. The second data selector **142** may include, but is not limited to, the same multiplexer as the first data selector **141**.

[0078] The control data selected by the second data selector **142** may be converted into packets by the second data converter **113** and encoded with predetermined rules. The encoded control data may be transmitted to the data driving device **200** through the transmitter **115**. However, the aspects are not limited thereto. If the control data is not encoded, the control data may be transmitted directly to the data driving device **200** through the transmitter **115** without passing through the second data converter **113**.

[0079] The first auxiliary communication circuit **120** may receive the auxiliary communication signal LCK or send the auxiliary communication signal LCK to the second communication line LN**2**.

[0080] The first auxiliary communication circuit **120** may confirm the auxiliary communication signal LCK received from the second communication line LN**2** and send a signal having the same form as the auxiliary communication signal LCK to the second communication line LN**2** when the auxiliary communication signal LCK indicates an abnormality of the data driving device **200**.

[0081] The data driving device **200** may include a second main communication circuit **210**, a second auxiliary communication circuit **220**, and a reception control part **230**.

[0082] The second main communication circuit **210** may receive the main communication signal MDT via the first communication line LN**1**. The second main communication circuit **210** may receive optimized configuration data for each vendor via the first communication line LN**1** in the configuration mode to establish a high-speed environment.

[0083] Subsequently, the second main communication circuit **210** may receive the image data, the first control data, and the second control data at a second data rate, which is higher than the first data rate, via the first communication line LN**1**. The second main communication circuit **210** may receive the image data and the first control data optimized for each vendor during the active interval in the display mode, and may receive the second control data optimized for each vendor during the blank interval in the display mode.

[0084] The second main communication circuit **210** may include a clock data recovery part **211**A and a parallelizer **211**B. The clock data recovery part **211**A may perform clock training on signals that contain a training pattern. The clock data recovery part **211**A may recover the clock by performing the clock training. The clock recovery part **211**A may recover data using the recovered clock, and when the recovered data matches the reference data, the recovered clock may be used for communication with the data processing device **100**.

[0085] The clock data recovery part **211**A may receive clock training pattern signals as its input, generate output signals, and invert a lock signal from a low logic level to a high logic level when the phase and frequency of the output match those of the input clock, and then recover the clock to generate internal clocks having multi-phases. The clock data recovery part **211**A may generate and output these multi-phase internal clocks using a phase-locked loop (PLL) technique or a delay-locked loop (DLL) technique.

[0086] The clock data recovery part **211**A may synchronize the rising edge of the multi-phase internal clocks with each bit of control data packets and image data packets to recover the bits of the control and image data.

[0087] The parallelizer **211**B may convert serial data into parallel data. The parallelizer **211**B may receive the clock recovered by the clock data recovery part **211**A and parallelize the data received from the data processing device **100** through the use of the recovered clock.

[0088] The second auxiliary communication circuit **220** may confirm abnormal states of the main communication signal MDT, the main communication circuit, and/or other components, and generate a status signal.

[0089] The reception control part **230** may transmit its vendor identification information to the data processing device **100** via the second communication line LN**2** in response to a request to confirm the vendor identification information. The vendor identification information may be stored in internal registers or may be generated in the form of a one-time password (OTP). This means that the vendor identification information is not restricted to any storage method or storage medium, as long as it is in a form that may be transferred at least once upon request.

[0090] When the clock training is completed, the reception control part **230** may control the second auxiliary communication circuit **220** to output the lock signal at a high level. When a lock-fail occurs, the reception control part **230** may control the second auxiliary communication circuit **220** to output the lock signal at a low level. Further, upon receiving a first configuration packet requesting the vendor identification information from the data processing device **100**, the reception control part **230** may control the second auxiliary communication circuit **220** to output its own vendor identification information stored in the register **143** to the second communication line LN**2**.

[0091] FIG. **6** is a diagram illustrating the main communication and the auxiliary communication between the data processing device and the data driving device according to an aspect of the present disclosure. FIG. **7** is a diagram illustrating the main communication and the auxiliary communication between the data processing device and the data driving device according to another aspect of the present disclosure.

[0092] Referring to FIG. **6**, the data driving device **200** may be composed of a plurality of data driving devices **120**A, **120**B, **200**C, and **200**D. The first communication line LN**1** may be connected one-to-one to each data driving part **200**A, **200**B, **200**C, and **200**D. The data processing device **100** and the plurality of data driving devices **200**A, **200**B, **200**C, and **200**D may send and receive various information via the second communication line LN**2**.

[0093] Between the plurality of data driving devices **200**A, **200**B, **200**C, and **200**D, the second communication line LN**2** may be connected in cascade forming a plurality of lock links. The first data driving device **200**A may receive signals from the data processing device **100** via a first lock line LN**2***a*. The first data driving device **200**A and the second data driving device **200**B may be connected via a second lock line LN**2***b*, while the second data driving device **200**B and the third data driving device **200**C may be connected via a third lock line LN**2***c*. The third data driving device **200**C and the fourth data driving device **200**D may be connected via a fourth lock link LN**2***d*, and the fourth data driving device **200**D may be connected to the data processing device **100** via a feedback link LN**2***e*.

[0094] The first to fourth data driving devices **200**A to **200**D may transmit lock signals using the lock lines. A lock signal is used to indicate whether or not clock training is complete. If the lock signal is at a high level (or low level), it may signify that clock training is complete. If the lock signal is at a low level (or high level), it may signify that clock training is incomplete. A lock-fail may signify either that clock training has not been completed or that the link between the data processing device **100** and the data driving device **200** has been broken.

[0095] The data processing device **100** may transmit a first configuration packet to the first data driving device **200**A via the first communication line LN**1**. Upon receipt of the first configuration packet, the first data driving device **200**A may forward its vendor identification information to the second data driving device **200**B. The vendor identification information of the first data driving device **200**A may be sequentially transmitted to the second data driving device **200**B, the third data driving device **200**C, and the fourth data driving device **200**D. The fourth data driving device **200**D may transmit to the data processing device **100** the vendor identification information of the first data driving device **200**A. Thereafter, the data processing device **100** may transmit the first configuration packet to the second data driving device **200**B. In this manner, the vendor identification information may be received from the plurality of data driving devices **200**A to **200**D by forwarding the first configuration packet to each of the data driving devices **200**A to **200**D in sequence.

[0096] Referring to FIG. **7**, the data processing device **100** and the plurality of data driving devices **200**A, **200**B, **200**C, and **200**D may be connected in one-to-one via a plurality of first communication lines LN**1**. Further, the data processing device **100** and the plurality of data driving devices **200**A, **200**B, **200**C, and **200**D may be connected via a second communication line LN**2**, configured as a common bus.

[0097] The second communication line LN**2** may be a single signal line driven by an open-drain configuration. A pull-up resistor Rqu may be connected to the second communication line LN**2**, where one side of the pull-up resistor Rqu is connected to the second communication line LN**2**, and the other side is supplied with a driving voltage VCC.

[0098] A plurality of data driving devices **200**A to **200**D may be connected to the second communication line LN**2**, and a multi-drop may be implemented by such connection.

[0099] In this case, the data processing device **100** may transmit a first configuration packet to the first data driving device **200**A via the first communication line LN**1**. The first data driving device **200**A may transmit its vendor identification information via the second communication line LN**2**, which is configured as a common bus. In this manner, the data processing device **100** may receive vendor identification information of the plurality of data driving devices **200**A, **200**B, **200**C, and **200**D by time-division control.

[0100] According to an aspect, a first configuration packet requesting vendor identification information may be transmitted via the first communication line LN**1**, and the vendor identification information of each data driving device **200**A to **200**D may be received via the second communication line LN**2**. However, the aspects are not limited thereto. For example, the data processing device **100** may request vendor identification information for each of the data driving devices **200**A to **200**D over the second communication line LN**2**.

[0101] FIG. **8** is a diagram illustrating the sequence of transmission signals according to an aspect of the present disclosure. FIG. **9** is a diagram illustrating a structure of a vendor identification information requesting packet according to an aspect of the present disclosure. FIG. **10** is a configuration diagram of blank data and line data according to an aspect of the present disclosure. FIG. **11** is a diagram showing the data flow of the data processing device and the data driving device according to an aspect of the present disclosure.

[0102] Referring to FIGS. **8** to **11**, the driving voltage VCC may initially maintain its waveform at a low-level voltage and then transition its waveform to a high-level voltage waveform at a certain point in time. The time at which the driving voltage VCC transitions to a high-level voltage may correspond to the driving timing of the display driving device.

[0103] After the driving timing, the data processing device **100** and the data driving device **200** may operate in the configuration mode, CFG mode (T**101**). After the operation in the configuration mode T**101** is completed, the data processing device **100** and the data driving device **200** may operate in the display mode, Display Mode (T**102**).

[0104] In the configuration mode T**101**, the data processing device **100** may send a preamble packet P**710**, on the main communication signal MDT. The data driving device **200** may train a low-speed communication clock for receiving the configuration packet P**720**, using the preamble packet P**710**, which is configured with a clock training pattern. The preamble packet may be defined as a low-speed clock training pattern or a first clock training pattern. The data driving device **200** may train the low-speed communication clock using the preamble packets P**710** (S**111**).

[0105] When the low-speed communication clock is trained within a predefined time period TCFG_LOCK, the data driving device **200** may inform the data processing device **100** of the clock training status on the auxiliary communication signal. For example, once the low-speed communication clock has been trained, the data driving device **200** may alter the voltage level of the auxiliary communication signal from low to high (S**112**).

[0106] After confirming from the auxiliary communication signal that the data driving device **200** has trained the low-speed communication clock, the data processing device **100** may transmit a first configuration packet P**720** (S**113**).

[0107] The first configuration packet P**720** may be composed of a start bit P**721**, a header P**722**, body data P**723**, and an end bit P**724**. The header P**722** may include mode selection information and read mode information, and the body data P**723** may include read address information and read length information.

[0108] The mode selection information may include a default mode, a bypass mode, a test mode, and a read mode. The default mode may be a normal mode that operates as a configuration mode and a display mode. The read mode may be a mode that receives vendor identification information from the data driving device. The test mode may be a mode that perform different kinds of tests. The bypass mode may be a mode that skips a relevant step. The data driving device that needs to be tested during the test may operate in the test mode, and the remaining data driving devices may operate in the bypass mode. The mode selection information may be composed of four bits to implement four modes. For example, the default mode may be **0000**, the bypass mode

may be **0011**, the test mode may be **1100**, and the read mode may be **1111**. However, the aspects are not limited thereto.

[0109] The read mode information may be a 1-bit signal consisting of either high or low levels. The read address information may be information about a start address to be read from a register map of the data driving device **200**. The read length information may be the length of information to be read. Therefore, it is possible to obtain vendor identification information by reading a predetermined length from a predetermined location.

[0110] The plurality of data driving device **200** may operate according to the command defined in the first configuration packet P**720**.

[0111] When driving in the read mode, the data processing device **100** may transmit the first configuration packet SPI in which the mode selection information is in the read mode to the plurality of data driving devices **200**. In this case, to sequentially receive the vendor identification packet, the data processing device **100** may transmit read mode information at a high level to only one of the data driving devices **200** and transmit read mode information at a low level to the remaining data driving devices **200**.

[0112] When the received read mode information is at a high level, the corresponding data driving device **200** may transmit its own vendor identification packet via the second communication line LN**2**. The remaining data driving device **200** in which the received read mode information is at a low level may maintain the second communication line at a high level and wait.

[0113] As such, the data processing device **100** may receive the vendor identification packet by sequentially transmitting the read mode information to the plurality of data driving devices **200** at a high level.

[0114] When receiving the vendor identification packet from all the data driving devices **200**, the data processing device **100** may change the mode selection information to the default mode and operate in the configuration mode. Thereafter, when the configuration mode ends, the data processing device **100** may switch to the display mode.

[0115] When the data driving device **200** receives the first configuration packet P**720** instructing it to operate in the read mode, it may transmit its own vendor identification packet R**820** together with a preamble pattern R**810**, via the second communication line LN**2** (S**114**).

[0116] When certain pattern information is transmitted together with the preamble pattern R**810** from the data driving device **200**, the data processing device **100** may recognize it as a vendor identification packet R**820** for that data driving device **200**.

[0117] According to an aspect, during the read mode, the data processing device **100** may transmit a preamble pattern P**711**, to the data processing device **100** via the first communication line LN**1**, and the data driving device **200** may transmit a preamble pattern R**810**, and a vendor identification packet R**820**, to the data processing device **100** via the second communication line LN**2**. During a read mode period RP**1**, a clock signal sent by the data processing device **100** and a clock signal transmitted by the data driving device **200** may be asynchronous with each other.

[0118] The first communication line LN**1** has a lower transmission speed than the second communication line LN**2**, and has a pull-up resistor or the like, which that makes it difficult to drive at high speed. Accordingly, the data driving device **200** may be configured to transmit the vendor identification information using a default clock generated by an internal oscillator. According to this configuration, since the data processing device **110** uses a clock that is not synchronized with the clock of the preamble pattern P**711** received via the first communication line LN**1**, a data phase lock time for synchronizing the preamble clock received by the data processing device **100** may be increased.

[0119] However the aspects are not limited thereto. For example, the data driving device **200** may be configured to transmit the vendor identification packet R**820** using a clock of a preamble pattern that has completed training. For example, the data driving device **200** may transmit the vendor identification packet R**820** after slowly modulating the clock frequency of the preamble pattern by dividing the clock frequency. In this case, information about how much to divide the clock frequency of the preamble pattern may be stored in advance in the body data P**723** of the first configuration packet P**720**.

[0120] Accordingly, the data driving device **200** may adjust the clock frequency of the preamble pattern according to the frequency of the transmission clock stored in the body data P**723** of the first configuration packet P**720** and transmit the vendor identification packet R**820** according to the adjusted clock. Such a configuration may allow the data processing device **100** to reduce the clock synchronization time.

[0121] However, the aspects are not limited thereto. When the preamble pattern P**711** is a Manchester code, the data driving device may transmit the preamble pattern R**810** and the vendor identification packet R**820** using the preamble pattern P**711** as a clock. The transmitted vendor identification packet R**820** may be half as long as the preamble. In this case, there is an advantage in that a separate frequency divider circuit may be omitted.

[0122] When receiving the vendor identification packet R**820**, the data driving device **200** may read the value stored in one of the plurality of registers **143** that matches the vendor identification information, and store the value as the configuration data.

[0123] The data driving device **200** may transmit configuration data P**730** matching the vendor identification information to the data driving device **200** (S**115**). When the data driving device **200** receives the configuration data P**730**, it may maintain a lock signal at a high level (S**116**). The data driving device **200** may read the received configuration data P**730** to establish a high-speed communication environment according to the settings therein.

[0124] After the configuration mode T**101** ends, the data processing device **100** and the data driving device **200** may transition to the display mode T**102**. The display mode T**102** may be composed of a clock training period T**103** and a frame period T**104**. Once the high-speed communication clock P**730** has been trained during the clock training period T**103**, the frame period T**104** may occur repeatedly.

[0125] During the clock training period T**103**, the data processing device **100** may send a clock training pattern P**712**, to the data driving device **200** at the second data rate. The data driving device **200** may train high-speed communication clock corresponding to the second data rate according to the clock training pattern P**712**. Here, the second data rate may have a higher frequency than the first data rate.

[0126] Once the clock training for the high-speed communication clock is complete, the data driving device **200** may maintain the lock signal at a high level (S**122**). Once the

clock training for the high-speed communication clock is complete, the data processing device **100** may transmit a link training pattern P**713**. Once the link training is complete, the data driving device **200** may maintain the lock signal at a high level. Once the link training is complete, the data processing device **100** may enter a normal data transmission period where control data and image data are transmitted (S**125**).

[0127] In the display mode, the frame period T**104** may include an active interval T**106** and a blank interval T**105**. The active interval T**106** may be a period during which image data and control data are sent on a line-by-line basis, while the blank interval T**105** may be a period during which line-by-line image data is not sent. The blank interval T**105** may be divided into a horizontal blank interval and a vertical blank interval.

[0128] The frame period T**104** may include an active interval T**106** and a blank interval T**105**. The active interval T**106** may be a period during which image data and control data are sent on a line-by-line basis, while the blank interval T**105** may be a period during which line-by-line image data is not sent. The blank interval T**105** may be divided into a horizontal blank interval and a vertical blank interval, and for ease of explanation, it will be described that the blank interval T**105** is a vertical blank interval.

[0129] As shown in FIG. **10**, during the blank interval T**105**, the data processing device **100** may send a frame control packet P**740** on a line-by-line basis. The frame control packet P**740** may include a control start packet, CS, P**741**, a frame start packet, FPS, P**742**, and a frame data packet, FC Data, P**743**.

[0130] The control start packet P**741** may indicate the start of a control packet. The frame start packet P**742** may indicate the start of transmission of frame data. Therefore, it is possible to distinguish whether the data to be transmitted after the control start signal is frame data or line data.

[0131] The frame data packet P**743** may contain configuration values that are changed on a frame-by-frame basis or may not be changed from time to time. The frame clock training pattern may contain pattern signals to train the high-speed communication clock. According to an aspect, the configuration values in the frame data packet may be set differently depending on the vendor identification information.

[0132] During the blank interval T**105**, the data processing device **100** may enter the active interval T**106** after sending blank data packets for all lines.

[0133] During the active interval T**106**, the data processing device **100** may send a line control packet P**750**, an image packet P**760**, and a line clock training pattern P**754**, on a line-by-line basis.

[0134] The line control packet P**750** may be composed of a control start packet P**751**, a line start packet P**752**, and a line data packet P**753**. The control start packet P**751** may indicate the start of the line control packet P**750**, and the line start packet P**752** may indicate the start of the transmission of the line data.

[0135] The line data packet P**753** may contain configuration values that are changed on a line-by-line basis or may be changed from time to time. For example, the line data packet P**753** may include a polarity value indicating the polarity of each pixel, may include a value indicating whether or not a scrambler **414** has been reset, and may include control information indicating whether the video data is valid data or dummy data. According to an aspect, the configuration values in the line data packet may be set differently depending on the vendor identification information.

[0136] The image packet P**760** may contain the grayscale values of the pixels disposed on a line. The line clock training pattern P**754** may include a pattern signal to train the high-speed communication clock.

[0137] During the active interval T**106**, the data processing device **100** may enter the blank interval T**105** again after sending the line control packets for all lines.

[0138] The term "~part" used in the aspects refers to software or hardware components such as field-programmable gate arrays (FPGA) or ASIC, where the "~part" performs certain roles. However, "~part" is not limited to software or hardware. The "~part" may be configured to be on an addressable storage medium or may be configured to play one or more processors. Thus, as an example, "~part" includes software components, components such as object-oriented software components, class components, and task components, processes, functions, properties, procedures, subroutines, segments of program code, drivers, firmware, microcode, circuits, data, databases, data structures, tables, arrays, and variables. The functions provided within the components and "~parts" may be combined into fewer components and "~parts", or further separated into additional components and "~parts". In addition, the components and "~parts" may be implemented to play one or more CPUs within the device or secure multimedia card.

[0139] While aspects of the present disclosure have been described in more detail with reference to the accompanying drawings, the present disclosure is not necessarily limited to these aspects and may be practiced in various modifications without departing from the spirit of the present disclosure. Therefore, the aspects disclosed in the present disclosure are provided for illustrative purposes only and are not intended to limit the technical concept of the present disclosure, and the scope of the technical concept of the present disclosure is not limited thereto. Therefore, it should be understood that the aspects described above are illustrative in all aspects and do not limit the present disclosure.

LIST OF REFERENCE NUMBERS

[0140] **100**: Data processing device
[0141] **110**: First main communication circuit
[0142] **120**: First auxiliary communication circuit
[0143] **130**: Transmission control part
[0144] **140**: Option selection circuit
[0145] **200**: Data driving device
[0146] **210**: Second main communication circuit
[0147] **220**: Second auxiliary communication circuit
[0148] **230**: Reception control part

What is claimed is:

1. A data processing device comprising:

a first main communication circuit configured to transmit configuration data and image data via a first communication line;

a first auxiliary communication circuit configured to send and receive signals via a second communication line; and

a plurality of registers configured to store configuration data for each vendor,

wherein the first main communication circuit is configured to:

transmit a first configuration packet requesting vendor identification information, select configuration data from the plurality of registers based on received vendor identification information, and transmit the selected configuration data via the first communication line.

2. The data processing device of claim **1**, wherein the first main communication circuit is configured to: transmit a preamble pattern via the first communication line and transmit the first configuration packet via the first communication line when receiving a lock signal of the preamble pattern via the second communication line.

3. The data processing device of claim **2**, wherein the first main communication circuit is configured to: receive the vendor identification information via the second communication line.

4. The data processing device of claim **2**, wherein the data processing device is configured to transmit a preamble pattern via the first communication line during read mode period after requesting the first configuration packet.

5. The data processing device of claim **1**, wherein the first main communication circuit is configured to transmit control data and image data at a second communication rate different from the first communication rate after the transmission of the selected configuration data is completed; and

the control data is set based on the received vendor identification information.

6. The data processing device of claim **1**, wherein each of the plurality of registers stores configuration data for each vendor.

7. The data processing device of claim **1**, wherein:

different individual configuration data for each vendor are stored in the plurality of registers,

common configuration data common to the vendors is stored in a common register, and

the first main communication circuit is configured to transmit the common configuration data stored in the common register when receive the vendor identification information, and transmit the different individual configuration data based on the vendor identification information.

8. The data processing device of claim **1**, wherein the first main communication circuit further includes an input/output interface connected to an external memory; and

the first main communication circuit is configured to store configuration data stored in the external memory in the plurality of registers through the input/output interface.

9. A data driving device comprising:

a second main communication circuit configured to receive configuration data and image data via a first communication line;

a second auxiliary communication circuit configured to send and receive signals via a second communication line; and

a reception controller configured to control the second main communication circuit and the second auxiliary communication circuit,

wherein the reception controller is configured to transmit its own vendor identification packet via the second communication line in response to receiving a first configuration packet requesting vendor identification information via the first communication line.

10. The data driving device of claim **9**, wherein the reception controller is configured to receive configuration data based on the vendor identification information to establish a high-speed transmission environment.

11. A display device comprising:

a data processing device; and

a plurality of data driving devices,

wherein the data processing device is configured to send a first configuration packet that requests vendor identification information to each of the plurality of data driving devices;

the plurality of data driving devices each is configured to transmit its vendor identification information to the data processing device in response to the first configuration packet; and

the data processing device is configured to transmit selected configuration data based on received vendor identification information to each of the plurality of data driving devices.

12. The display device of claim **11**, wherein the data processing device is configured to transmit the first configuration packet via the first communication line; and

the plurality of data driving devices is configuration transmit the vendor identification information via the second communication line.

13. The display device of claim **12**, wherein the data processing device is configured to transmit control data selected according to the vendor identification information to the plurality of data driving devices via the first communication line.

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