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LIGHT EMITTING DIODES AND METHODS WITH ENCAPSULATION

Abstract

Solid state lighting apparatuses, systems, and related methods are provided. An example apparatus can include one or more light emitting diodes (LEDs) and a dark or black encapsulation layer surrounding and/or disposed between the one or more LEDs. The apparatus can include, e.g., a substrate or a leadframe for mounting the LEDs. A method for producing a panel of LEDs can include joining the LEDs to the panel, e.g., by bump bonding, and flooding the panel with dark or black encapsulation material so that the LED chips are surrounded by the dark or black encapsulation material.

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Background/Summary

RELATED APPLICATIONS [0001] This application is a division of U.S. patent application Ser. No. 15/087,641, filed Mar. 31, 2016, which claims the benefit of provisional patent application Ser. No. 62/141,065, filed Mar. 31, 2015, the disclosures of which are hereby incorporated herein by reference in their entirety.

TECHNICAL FIELD

[0002] The present subject matter relates generally to lighting apparatuses and related methods and, more particularly, to solid state lighting apparatuses and related methods.

BACKGROUND

[0003] In recent years, there have been dramatic improvements in light emitting diode (LED) technology such that LEDs of increased luminance and color fidelity have been introduced. Due to these improved LEDs and improved image processing technology, large format, full color LED video screens have become available and are now in common use. LED displays typically comprise a combination of individual LED panels providing image resolution determined by the distance between adjacent pixels or “pixel pitch”.

[0004] Displays that are intended for viewing from great distances, such as for example outdoor displays, have relatively large pixel pitches and usually comprise discrete LED arrays. In the discrete LED arrays, a cluster of individually mounted red, green, and blue LEDs are driven to form what appears to the viewer as a full color pixel. On the other hand, indoor screens, which require smaller pixel pitches such as 3 mm or less, typically comprise panels carrying red, green, and blue LEDs mounted on a single electronic device attached to a printed circuit board (PCB) that controls the output of each electronic device.

[0005] Some conventional LED packages have transparent encapsulant covering LED chips to protect the LED chip assembly and so that light emitted from LED packages can be used efficiently. Those skilled in the art routinely engineer package components to be light transparent and not to absorb any light generated by the LED or irradiating the package from external sources. When used in LED displays, however, the transparent encapsulant and other elements of the housing such as metal traces and structural elements in conventional LED packages can reflect too much ambient light. When viewing displays including conventional LED packages, customers experience lower contrast and have difficulty viewing the displayed content if the display reflects too much ambient background light. For example, a customer may find it difficult to read displayed text in daylight conditions if the reflection from the sun is not minimalized. Minimalizing the reflection of the LED source is useful in other lighting applications, as well. For spot lights and other fixtures using lenses, it is helpful to make the source site appear smaller, limiting the reflection around the chip(s).

SUMMARY

[0006] Solid state lighting apparatuses, systems, and related methods are provided. An example apparatus can comprise, for example: a substrate; a plurality of electrically conductive traces disposed over the substrate; one or more light emitting diodes (LEDs) each electrically connected to at least two of the electrically conductive traces; and a dark or black encapsulation layer

surrounding the one or more LEDs. Other aspects, features and embodiments of the subject matter will be more fully apparent from the ensuing disclosure and appended claims.

Description

BRIEF DESCRIPTION OF DRAWINGS

[0007] A full and enabling disclosure of the present subject matter is set forth more particularly in the remainder of the specification, including reference to the accompanying figures, relating to one or more embodiments, in which:

[0008] FIGS. **1**A through **1**O are various illustrations of an example solid state lighting apparatus;

[0009] FIG. **2**A is a diagram illustrating an example panel of LEDs;

[0010] FIG. **2**B is a cross-section side view of a portion of panel;

[0011] FIG. **3** is a flow diagram of an example process for fabricating a panel of LEDs;

[0012] FIG. **4** is a flow diagram of an example process for fabricating a panel of LEDs;

[0013] FIG. **5**A is a diagram illustrating an LED chip **502** being attached using Ag epoxy;

[0014] FIG. **5**B is a perspective view of an LED chip **502** being attached using Ag epoxy to trace material **512** having trenches **518***a-b* in the trace material;

[0015] FIG. **5**C is a side view of the LED chip **502** being attached; and

[0016] FIG. **5**D is a diagram illustrating the n-pad and the p-pad and LED chip **502** as coplanar.

[0017] FIGS. **6** and **7** are flow diagrams of example methods for producing LED devices.

DETAILED DESCRIPTION

[0018] In some aspects, solid state lighting apparatuses and methods described herein can comprise various solid state light emitter electrical configurations, color combinations, and/or circuitry components for providing solid state lighting apparatuses having improved efficiency, improved color mixing, and/or improved color rendering. Apparatuses and methods such as those disclosed herein advantageously cost less, are more efficient, vivid, and/or brighter than some other solutions.

[0019] Unless otherwise defined, terms used herein should be construed to have the same meaning as commonly understood by one of ordinary skill in the art to which this subject matter belongs. It will be further understood that terms used herein should be interpreted as having a meaning that is consistent with the respective meaning in the context of this specification and the relevant art, and should not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0020] Aspects of the subject matter are described herein with reference to sectional, perspective, elevation, and/or plan view illustrations that are schematic illustrations of idealized aspects of the subject matter. Variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected, such that aspects of the subject matter should not be construed as limited to particular shapes illustrated herein. This subject matter can be embodied in different forms and should not be construed as limited to the specific aspects or embodiments set forth herein. In the drawings, the size and relative sizes of layers and regions can be exaggerated for clarity.

[0021] Unless the absence of one or more elements is specifically recited, the terms “comprising,” “including,” and “having” as used herein should be interpreted as open-ended terms that do not preclude the presence of one or more elements. Like numbers refer to like elements throughout this description.

[0022] It will be understood that when an element such as a layer, region, or substrate is referred to as being “on” another element, it can be directly on the other element or intervening elements can be present. Moreover, relative terms such as “on”, “above”, “upper”, “top”, “lower”, or “bottom” are used herein to describe one structure's or portion's relationship to another structure or portion as illustrated in the figures. It will be understood that relative terms such as “on”, “above”, “upper”,

"top", "lower" or "bottom" are intended to encompass different orientations of the apparatus in addition to the orientation depicted in the figures. For example, if the apparatus in the figures is turned over, structure or portion described as "above" other structures or portions would now be oriented "below" the other structures or portions.

[0023] The terms "electrically activated emitter(s)" and "emitter(s)" as used herein are synonymous terms and refer to any device capable of producing visible or near visible (e.g., from infrared to ultraviolet) wavelength radiation, including for example but not limited to, xenon lamps, mercury lamps, sodium lamps, incandescent lamps, and solid state emitters, including LEDs or LED chips, organic light emitting diodes (OLEDs), and lasers.

[0024] The terms "solid state light emitter(s)", "solid state emitter(s)", and "light emitter(s)" are synonymous terms and refer to an LED chip, a laser diode, an organic LED chip, and/or any other semiconductor device preferably arranged as a semiconductor chip that comprises one or more semiconductor layers, which can comprise silicon, silicon carbide, gallium nitride and/or other semiconductor materials, a substrate which can comprise sapphire, silicon, silicon carbide and/or other microelectronic substrates, and one or more contact layers which can comprise metal and/or other conductive materials.

[0025] The terms "groups", "segments", "strings", and "sets" as used herein are synonymous terms. As used herein, these terms generally describe how multiple LED chips are electrically connected, such as in series, in parallel, in mixed series/parallel, in common anode, or in common anode configurations among mutually exclusive groups/segments/sets. The segments of LED chips can be configured in a number of different ways and may have circuits of varying functionality associated therewith (e.g. driver circuits, rectifying circuits, current limiting circuits, shunts, bypass circuits, etc.), as discussed, for example, in U.S. patent application Ser. No. 12/566,195, filed on Sep. 24, 2009, now U.S. Pat. No. 8,713,211, U.S. patent application Ser. No. 13/769,273, filed on Feb. 15, 2013, now U.S. Pat. No. 8,970,131, U.S. patent application Ser. No. 13/769,277 filed on Feb. 15, 2013, now U.S. Pat. No. 9,414,454, U.S. patent application Ser. No. 13/235,103, filed on Sep. 16, 2011, now U.S. Pat. No. 9,131,561, U.S. patent application Ser. No. 13/235,127, filed on Sep. 16, 2011, now U.S. Pat. Nos. 9,277,605, and 8,729,589, which issued on May 20, 2014, the disclosure of each of which is hereby incorporated by reference herein in the entirety.

[0026] The term "targeted" refers to configurations of LED chip segments that are configured to provide a pre-defined lighting characteristic that is a specified parameter for the lighting apparatus. For example, the targeted spectral power distribution can describe the characteristic of the light that is generated at a particular power, current, or voltage level.

[0027] Apparatuses, systems, and methods as disclosed herein can utilize red chips, green chips, and blue chips. In some aspects, chips for use in blue-shifted yellow light (BSY) devices can target different bins as set forth in Table 1 of commonly owned, assigned, and co-pending U.S. patent application Ser. No. 12/257,804, published as U.S. Pat. Pub. No. 2009/0160363, the disclosure of which is incorporated by reference herein in the entirety. Apparatuses, systems, and methods herein can utilize, for example, ultraviolet (UV) chips, cyan chips, blue chips, green chips, red chips, amber chips, and/or infrared chips.

[0028] The term "substrate" as used herein in connection with lighting apparatuses refers to a mounting member or element on which, in which, or over which, multiple solid state light emitters (e.g., LED chips) can be arranged, supported, and/or mounted. A substrate can be, e.g., a component substrate, a chip substrate (e.g., an LED substrate), or a sub-panel substrate. Exemplary substrates useful with lighting apparatuses as described herein can for example comprise printed circuit boards PCBs and/or related components (e.g., including but not limited to metal core printed circuit boards (MCPCBs), flexible circuit boards, dielectric laminates, ceramic based substrates, and the like, or ceramic boards having FR4 and/or electrical traces arranged on one or multiple surfaces thereof, high reflectivity ceramics (e.g., alumina) support panels, and/or mounting elements of various materials and conformations arranged to receive, support, and/or conduct

electrical power to solid state emitters. Electrical traces described herein provide electrical power to the emitters for electrically activating and illuminating the emitters. Electrical traces may be visible and/or covered via a reflective covering, such as a solder mask material, Ag, or other suitable reflector.

[0029] In some aspects, a single, unitary substrate can be used to support multiple groups of solid state light emitters in addition to at least some other circuits and/or circuit elements, such as a power or current driving components and/or current switching components. In other aspects, two or more substrates (e.g., at least a primary substrate and one or more secondary substrate or substrates) can be used to support multiple groups of solid state light emitters in addition to at least some other circuits and/or circuit elements, such as a power or current driving components and/or temperature compensation components. The first and second (e.g., primary and secondary) substrates can be disposed above and/or below each other and along different planes, adjacent (e.g., side-by-side) to each other, have one or more co-planar surfaces disposed adjacent each other, arranged vertically, arranged horizontally, and/or arranged in any other orientation with respect to each other.

[0030] Solid state lighting apparatuses according to aspects of the subject matter herein can comprise III-V nitride (e.g., gallium nitride) based LED chips or laser chips fabricated on a silicon, silicon carbide, sapphire, or III-V nitride growth substrate, including (for example) chips manufactured and sold by Cree, Inc. of Durham, N.C. Such LED chips and/or lasers can be configured to operate such that light emission occurs through the substrate in a so-called “flip chip” orientation. Such LED and/or laser chips can also be devoid of growth substrates (e.g., following growth substrate removal). In some cases, LED chips can comprise red-III-V chips, but not nitride such as InGaAIP, GaAsP, and the like.

[0031] LED chips useable with lighting apparatuses as disclosed herein can comprise horizontal structures (with both electrical contacts on a same side of the LED chip) and/or vertical structures (with electrical contacts on opposite sides of the LED chip). A horizontally structured chip (with or without the growth substrate), for example, can be flip chip bonded (e.g., using solder) to a carrier substrate or printed circuit board (PCB), or wire bonded. A vertically structured chip (without or without the growth substrate) can have a first terminal solder bonded to a carrier substrate, mounting pad, or printed circuit board (PCB), and have a second terminal wire bonded to the carrier substrate, electrical element, or PCB.

[0032] Electrically activated light emitters, such as solid state emitters, can be used individually or in groups to emit light to stimulate emissions of one or more lumiphoric materials (e.g., phosphors, scintillators, lumiphoric inks, quantum dots), and generate light at one or more peak wavelengths, or of at least one desired perceived color (including combinations of colors that can be perceived as white). Inclusion of lumiphoric (also called ‘luminescent’) materials in lighting apparatuses as described herein can be accomplished by an application of a direct coating of the material on lumiphor support elements or lumiphor support surfaces (e.g., by powder coating, inkjet printing, or the like), adding such materials to lenses, and/or by embedding or dispersing such materials within lumiphor support elements or surfaces. Methods for fabricating LED chips having a planarized coating of phosphor integrated therewith are discussed by way of example in U.S. Patent Application Publication No. 2008/0179611, filed on Sep. 7, 2007, to Chitnis et al., the disclosure of which is hereby incorporated by reference herein in the entirety.

[0033] Other materials, such as light scattering elements (e.g., particles) and/or index matching materials can be associated with a lumiphoric material-containing element or surface. Apparatuses and methods as disclosed herein can comprise LED chips of different colors, one or more of which can be white emitting (e.g., including at least one LED chip with one or more lumiphoric materials).

[0034] In some aspects, one or more short wavelength solid state emitters (e.g., blue and/or cyan LED chips) can be used to stimulate emissions from a mixture of lumiphoric materials, or discrete

layers of lumiphoric material, including red, yellow, and green lumiphoric materials. LED chips of different wavelengths can be present in the same group of solid state emitters, or can be provided in different groups of solid state emitters. A wide variety of wavelength conversion materials (e.g., luminescent materials, also known as lumiphors or lumiphoric media, e.g., as disclosed in U.S. Pat. No. 6,600,175, issued on Jul. 29, 2003, and U.S. Patent Application Publication No. 2009/0184616, filed on Oct. 9, 2008, each disclosure of which is hereby incorporated by reference herein in the entirety, are well-known and available to persons of skill in the art. Utilizing multiple layers of phosphor with LED chips is discussed by way of example in U.S. patent application Ser. No. 14/453,482, filed Aug. 6, 2014, now U.S. Pat. No. 11,251,164, the disclosure of which is hereby incorporated by reference herein in the entirety. In some aspects, lighting apparatuses and systems as described herein comprise multiple sets of solid state light emitters targeting different colors (e.g., one set targeting a first color and at least a second set targeting a second color that is different than the first color. In some aspects, each set of the multiple sets comprises at least two solid state light emitters of a same color (e.g., the peak wavelengths coincide). In some aspects, each set of the multiple sets of solid state emitters is adapted to emit one or more different color(s) of light. In some aspects, each set of the multiple sets of solid state emitters is adapted to emit one or more color(s) of light that differ relative to one another (e.g., with each set of solid state emitters emitting at least one peak wavelength that is not emitted by another set of solid state emitters). Aspects of targeting and selective activating sets of solid state emitters according to the present subject matter may be provided using the circuitry and/or techniques described in U.S. patent application Ser. No. 14/221,839, and published as U.S. Patent Application Publication No. 2015/0257211 A1, the disclosure of which is incorporated herein by reference.

[0035] The term “color” in reference to a solid state emitter refers to the color and/or wavelength of light that is emitted by the chip upon passage of electrical current therethrough.

[0036] Some embodiments of the present subject matter may use solid state emitters, emitter packages, fixtures, luminescent materials/elements, power supply elements, control elements, and/or methods such as described in U.S. Pat. Nos. 7,564,180; 7,456,499; 7,213,940; 7,095,056; 6,958,497; 6,853,010; 6,791,119; 6,600,175, 6,201,262; 6,187,606; 6,120,600; 5,912,477; 5,739,554; 5,631,190; 5,604,135; 5,523,589; 5,416,342; 5,393,993; 5,359,345; 5,338,944; 5,210,051; 5,027,168; 5,027,168; 4,966,862, and/or 4,918,497, and U.S. Patent Application Publication Nos. 2009/0184616; 2009/0080185; 2009/0050908; 2009/0050907; 2008/0308825; 2008/0198112; 2008/0179611, 2008/0173884, 2008/0121921; 2008/0012036; 2007/0253209; 2007/0223219; 2007/0170447; 2007/0158668; 2007/0139923, and/or 2006/0221272; U.S. patent application Ser. No. 11/566,440, filed on Dec. 4, 2006, now U.S. Pat. No. 7,213,940; with the disclosures of the foregoing patents, published patent applications, and patent application serial numbers being hereby incorporated by reference as if set forth fully herein.

[0037] The terms “lighting apparatus” and “module” as used herein are synonymous, and are not limited, except that it is capable of emitting light. That is, a lighting apparatus can be a device or apparatus that illuminates an area or volume, e.g., a structure, a swimming pool or spa, a room, a warehouse, an indicator, a road, a parking lot, a vehicle, signage, e.g., road signs, a billboard, a ship, a toy, a mirror, a vessel, an electronic device, a boat, an aircraft, a stadium, a computer, a remote audio device, a remote video device, a cell phone, a tree, a window, an LCD display, a cave, a tunnel, a yard, a lamppost, or a device or array of devices that illuminate an enclosure, or a device that is used for edge or back-lighting (e.g., backlight poster, signage, LCD displays), light bulbs, bulb replacements (e.g., for replacing AC incandescent lights, low voltage lights, fluorescent lights, etc.), outdoor lighting, security lighting, exterior residential lighting (wall mounts, post/column mounts), ceiling fixtures/wall sconces, under cabinet lighting, lamps (floor and/or table and/or desk), landscape lighting, track lighting, task lighting, specialty lighting, rope lights, ceiling fan lighting, archival/art display lighting, high vibration/impact lighting-work lights, etc., mirrors/vanity lighting, spotlighting, high-bay lighting, low-bay lighting, or any other light emitting

device.
[0038] Various illustrative features are described below in connection with the accompanying figures.
[0039] FIGS. **1**A to **11** are various illustrations of an example solid state lighting apparatus **100**. Apparatus **100** is illustrated as being mounted on a substrate with conductive traces, but in some examples, apparatus **100** could be based on a leadframe construction where no traces are on top, or any other appropriate construction.
[0040] FIG. **1**A is a top view of an example solid state lighting apparatus **100**. Apparatus **100** includes three LEDs **102***a-c*. LEDs **102***a-c* can each have a different targeted color. Although three LEDs are illustrated, apparatus **100** may include a different number of LEDs, e.g., one or more LEDs. For example, apparatus **100** can be a 2×2 component with four red LEDs, four blue LEDs, and four green LEDs.
[0041] In some examples, LEDs **102***a-c* have different targeted colors selected so that apparatus **100** can operate as a pixel and produce a range of colors within its color gamut by energizing different combinations of LEDs **102***a-c*. For example, one or more of LEDs **102***a-c* may include: a UV, blue or green LED chip, such as a group Ill nitride based LED chip comprising negatively doped (n-type) epitaxial layer(s) of gallium nitride or its alloys and positively doped (p-type) epitaxial layers of gallium nitride or its alloys surrounding a light emitting active region; a red LED chip, such as an AlInGaP based red LED chip; a white LED chip (e.g., blue LED chip with phosphor(s) layer(s)), and/or a non-white phosphor based LED chip.
[0042] FIG. **1**B is a perspective view of apparatus **100**. Apparatus **100** can include a substrate **104**, which may support one or more electrical circuitry components for driving LEDs. LEDs **102***a-c* can be mounted on the substrate **104** and then encapsulated in an encapsulation layer **106**. The encapsulation layer **106** can be formed from, e.g., a substantially dark, such as black for example, material, which can be useful, e.g., for improving the contrast of apparatus **100** when used in an array of solid state lighting apparatuses.
[0043] In some examples, the LEDs **102***a-c* are attached to a sub-structure first, and then an encapsulant can be applied to create the encapsulation layer **106**. The encapsulation layer **106** can surround the LEDs **102***a-c*, e.g., surround the LEDs **102***a-c* on four or more sides of the LEDs **102***a-c*. As illustrated, the encapsulation layer **106** can surround the LEDs **102***a-c* on all, such as four, sides, e.g., in a horizontal plane. The encapsulation layer **106** can also be disposed between the LEDs **102***a-c* or disposed so as to be both between the LEDs **102***a-c* and surrounding the LEDs **102***a-c*. As illustrated, for example and without limitation, the encapsulation layer **106** is shown surrounding and between the LEDs **102***a-c*. In some aspects, the encapsulant or encapsulation layer can be applied, such as by dispensing or by any other suitable technique, to or around one or more light emitting diode (LED) such as the LEDs **102***a-c*. After application of the encapsulant, the encapsulant can be planarized to expose or nearly or almost expose the one or more light emitting diode (LED). The planarizing of the encapsulant can be performed such that a top surface of the one or more light emitting diode (LED) is completely or fully exposed, or such that the top surface of the one or more light emitting diode (LED) such as the LEDs **102***a-c* is substantially exposed so that the top surface is exposed to within 25 μm or less of being fully exposed.
[0044] The encapsulation layer **106** can be in contact with the LEDs **102***a-c* or near to the LEDs **102***a-c*. The encapsulation layer **106** is considered near to the LEDs **102***a-c* if the encapsulation layer **106** is at or less than a threshold distance from the LEDs **102***a-c*. The threshold distance can, for example and without limitation, be 200 μm or less, 150 μm or less, 100 μm or less, or 50 μm or less. The threshold distance can be the smallest distance between the LEDs **102***a-c* and the encapsulation layer, so that some portions of the encapsulation layer **106** can be further from the LEDs **102***a-c* and the encapsulation layer **106** is still near to the LEDs **102***a-c*.
[0045] In some aspects, a light emitting diode (LED) apparatus can comprise at least one or more light emitting diode (LED), and each of the one or more LED can comprise a light emitting surface.

The apparatus can comprise an encapsulation layer including an inner layer or an outer layer substantially coplanar with the LED by at least 25 μm or less. In some aspects, the apparatus can include an LED substrate on or over which the one or more LED can be disposed. In some aspects, the apparatus can comprise the encapsulation layer including an inner layer or an outer layer substantially coplanar with a top side of the LED by at least 25 μm or less. In some aspects, the encapsulation layer can comprise a black encapsulation layer.

[0046] As used in this document, the term “dark” or “black” refers to a material having a reflectivity below a threshold and a transmittance below a threshold. For example and without limitation, the material can have a reflectivity below 70% or below 50%, or the material can have a reflectivity below 4%. The material can have a transmittance of 20% per mm of thickness or less and a reflectivity below 70% or below 50%.

[0047] Although the encapsulation layer **106** is depicted as being flush with the top of apparatus **100**, in some examples, the encapsulation layer **106** may not be flush with the tops of LEDs **102***a-c*. For example, in some cases, the encapsulation layer **106** could cover LEDs **102***a-c*, e.g., in a thin layer. In some cases, LEDs **102***a-c* may stick out from the encapsulation layer **106**, e.g., to some small degree. The top of apparatus **100** in some examples may not be flat, e.g., the top can curve up or curve down or be textured, e.g., as a result of grinding, lapping, and/or sandblasting.

[0048] FIG. **1**C is a cross-sectional view of apparatus **100**. A number of electrical traces **108***a-c* can be disposed over substrate **104**. Traces **108***a-c* can comprise a mounting area for LEDs, and traces **108***a-c* may be provided over substrate **104** for passing electrical current to any number of LEDs, which may be customized in number, color, shape, size, and/or chip spacing for providing any desired emissions (e.g., any desired brightness, intensity, and/or color). Apparatus **100** can also include a number of bottom traces **110***a-b*. Bottom traces **110***a-b* can be useful for, e.g., integrating apparatus **100** into an array of multiple solid state lighting apparatuses.

[0049] Traces **108***a-c* can comprise any suitable electrically conductive material, e.g., Cu, finished with electroless Ag, Ni—Ag, ENIG, ENIPIG, HASL, OSP, or the like. Traces **108***a-c* can be applied over one or more surfaces of substrate **104** via plating (e.g., via electroplating or electroless plating), depositing (e.g., physical, chemical, and/or plasma deposition, CVD, PECVD, etc.), sputtering, or via any other suitable technique. In some aspects, traces **108***a-c* can comprise a metal or metal alloy which may contain (in whole or part) copper (Cu), silver (Ag), gold (Au), titanium (Ti), palladium (Pd), aluminum (Al), tin (Sn), combinations thereof, and/or any other suitable conductor.

[0050] In some aspects, substrate **104** can comprise a printed circuit board (PCB), a metal core printed circuit board (MCPCB), a flexible printed circuit board, a dielectric laminate (e.g., FR-4 boards as known in the art), a ceramic based substrate, or any other suitable substrate for mounting LED chips and/or LED packages. In some aspects substrate **104** can comprise one or more materials arranged to provide desired electrical isolation and high thermal conductivity. For example, at least a portion of substrate **104** may comprise a dielectric to provide the desired electrical isolation between electrical traces and/or sets of solid state emitters. In some aspects, substrate **104** can comprise ceramic such as alumina (Al.sub.2O.sub.3), aluminum nitride (AlN), silicon carbide (SIC), silicon, or a plastic or polymeric material such as polyimide, polyester etc. In some aspects, substrate **104** comprises a flexible circuit board, which can allow the substrate to take a non-planar or curved shape allowing for providing directional light emission with the solid state emitters also being arranged in a non-planar manner.

[0051] In some aspects, LEDs **102***a-c* can be horizontally structured so that LEDs **102***a-c* can be electrically connected to traces **108***a-b* without the use of wire bonding. For example, each of LEDs **102***a-c* can be a horizontally structured device where each electrical contact (e.g., the anode and cathode) can be disposed on a bottom surface of the LED **102***a-c*. Apparatus **100** includes die attach material **130**, e.g., solder bumps. Die attaching LEDs **102***a-c* using any suitable material and/or technique (e.g., solder attachment, preform attachment, flux or no-flux eutectic attachment,

silicone epoxy attachment, metal epoxy attachment, thermal compression attachment, bump bonding, and/or combinations thereof) can directly electrically connect LEDs **102***a-c* to traces **108***a-b* without requiring wire bonds.

[0052] In some aspects, each of LEDs **102***a-c* can be a device that does not comprise angled or beveled surfaces. For example, each of LEDs **102***a-c* can be an LED device that comprises coplanar electrical contacts on one side of the LED (bottom side) with the majority of the light emitting or transmitting surface being located on the opposite side (upper side). In the example of FIG. **1**C, LEDs **102***a-b* are bump bonded to traces **108***a-c*, e.g., using bumps of solder (or other appropriate conductive material) and force, energy (e.g., ultrasonic), and/or heat.

[0053] In some aspects, apparatus **100** can have a size less than 1.6 mm.sup.2 square with reference to the length and width illustrated in FIG. **1**A. For example, the dimensions of apparatus **100** can be between 0.8 mm×0.8 mm and 1 mm×1 mm. Apparatus **100** can be made using bump bonding of small die, e.g., less than 0.1 mm.sup.2, or between 0.01 mm.sup.2 per die and 0.03 mm.sup.2 per die or 0.05 mm.sup.2 per die. Apparatus **100** can have a thickness of 1.0 mm or less with reference to the height illustrated in FIG. **1**B. For example, apparatus **100** can have a height of 0.8 mm or 0.5 mm. The LEDs **102** can have a length or a width less than 0.3 mm, e.g., so that apparatus **100** is 0.1 mm by 0.195 mm, or 0.13 mm by 0.21, or 0.18 mm by 0.255 mm.

[0054] FIG. **1**C also illustrates one or more optional layer or layers **124** on top of LEDs **102***a-b*. For example, optional layers **124** can include diffuse layers for optics, lenses, polarizers, anti-reflective (AR) coating, anti glare, micro lenses, light steering, parallax barrier, lenticular arrays, and so on. Phosphor or other light converting elements can be added to some or all of optional layers **124**. In some examples, the height **140** of the LED chips can be about 10 μm. The height **142** of optional layers **124** can be about or less than 50 μm, so that the substrates of the LED chips are less than 50 μm from the top of apparatus **100**. As a result, the diffuse reflection of apparatus **100** can be 5% or less in the visible part of the spectrum. Layer **124** can comprise a diffuse top layer over the LEDs or the dark or black encapsulation layer or both, resulting in a matte finish or a modified light emission pattern.

[0055] FIG. **1**D illustrates apparatus **100** with an optional layer **112** of reflective coating, which can be referred to as a reflective element or elements on or at the sides of the LEDs **102***a-b*. Layer or layers **112** taper from the sides of apparatus **100** towards the LEDs **102***a-b* and between the LEDs **102***a-b*. The reflective coating can be, e.g., silicone or epoxy filled with titania or titanium dioxide white material that can be wetted underneath and on the sides of the chip. In some examples, the reflective coating can be grey, e.g., having a reflectivity between 20 and 80%. The shade of grey can be selected to tune balance and contrast. Greater reflectivity results in brighter light from apparatus **100**, but will generally decrease contrast. FIG. **1**J illustrates apparatus **100** with optional layer **112** of reflective coating having a different profile than that illustrated in FIG. **1**D. In FIG. **1**J, optional layer **112** turns up sharply close to the LEDs **102***a-b* and fills in the space between the LEDs **102***a-b* completely, so that optional layer **112** is flush with the tops of LEDs **102***a-b*.

[0056] FIG. **1**E illustrates apparatus **100** with optional bottom traces **110***a-b* that extend all the way to the edges. Gaps between the bottom traces **110***a-b* and the edges can use a lot of real estate on apparatus **100**, so extending bottom traces **110***a-b* can improve space usage on the bottom side of apparatus **100**, e.g., to improve mounting of apparatus **100**. For example, bottom traces **110***a-b* can have an area of 45% or greater of the substrate area of apparatus **100**.

[0057] FIG. **1**F illustrates apparatus **100** with optional conductive vias **114***a* and **114***c* that extend through the substrate **112**. For example, vias **114***a* and **114***c* can extend from top traces **108***a* and **108***c* to bottom traces **110***a* and **110***b*. In some examples, vias can be on an edge of substrate **104**. By placing vias on an edge of substrate **104**, vias can be shared between devices and cut in half or in quarters during singulation.

[0058] In some examples, vias are hollow, and it can be useful to prevent encapsulant from leaking from the top of apparatus **100** to the bottom side by flowing through the via. When LEDs **102***a-c*

are bonded over the vias so that the electrically conductive bump bond material seals the vias, the bump bond material can prevent the encapsulant from flowing through the via. This can be useful, e.g., to save costs associated with filling the vias.

[0059] FIG. **1**G is a top view of apparatus **100** illustrating example electrical connections between LEDs **102***a-c* and traces **108***a-d*. Trace **108***b* can be, e.g., a common electrical node for connection to anodes of LEDs **102***a-c*. Traces **108***a*, **108***c*, and **108***d* can be electrically coupled to the cathodes of LEDs **102***a-c* so that each LED can be individually controlled.

[0060] FIG. **1**H is a top view of apparatus **100** illustrating example conductive vias **114***a-d* and openings **116***a-f* in solder mask layer. Vias **114***a-d* can be configured to electrically couple traces **108***a-d* to traces on the bottom of the substrate **112** or traces within the substrate or elsewhere. Openings **116***a-f* permit conductive material to be applied to traces **108***a-d* so that, when LEDs **102***a-c* are mounted, LEDs **102***a-c* become electrically coupled as illustrated in FIG. **1**G. In some examples, the solder mask can be dark or black (higher contrast), and sidewalls of LEDs **102***a-c* can be made white (increased brightness with less impact on contrast). The white sidewalls may also help broaden the viewing angle.

[0061] FIG. **1**I is a side view of apparatus **100** where the substrate is an optional multilayer substrate. The substrate includes inner trace layers **120** and **122**. Via **114***e* can bypass inner trace layer **122** to electrically couple to inner trace layer **120**. Using inner trace layers can be useful, e.g., for signal routing, particularly with multi-pixel arrays. Various via technologies such as plated through-hole, buried, blind, and microvias can be used.

[0062] FIG. **1**K is a diagram illustrating example relative distances between LED chip **102***a* and traces **108***a-b*. The distance **150** between the pads on LED chip **102** can be, e.g., between 40-60 μm. The distance between the traces (in a panel, the panel trace gap) can be about or less than 70 μm. In some examples, the distance **152** between the traces is larger than the distance **150** between the pads on LED chip **102***a*.

[0063] FIG. **1**L illustrates apparatus **100** with a sidewall **160**. Apparatus **100** includes an optional coating **124** and an encapsulation layer **106** that can be, e.g., white, dark or black, clear, or any appropriate color. Sidewall **160** can be any appropriate color and is typically white or black. In some examples, sidewall **160** is formed as a solder mask layer.

[0064] FIG. **1**M illustrates apparatus **100** with an optional coating **124** and an encapsulation layer **106**. Encapsulation layer **106** can be any appropriate color, e.g., white or dark or black. Encapsulation layer **106** is not flush with the tops of the LED chips. This may happen when the removal of the encapsulation is faster than the chips, which can naturally result in encapsulation layer **106** being lower than the chip surfaces.

[0065] The back side of the LED chips depicted in any of the figures (the top side when viewing FIGS. **1**A-M) can be roughened at the water level. Roughening the back side of the LED chips can make the addition of an additional matte finish layer unnecessary. For example, roughening a side, such as the back side, of the LED chips can reduce or eliminate the specular reflection of the LED chips.

[0066] FIG. **1**N illustrates apparatus **100** with a white encapsulation layer **170** that is in contact with the LED chips and a dark or black encapsulation layer **106**. The white encapsulation layer **170** surrounds the LED chips and is between the LED chips. The black encapsulation layer **170** surrounds both the LED chips and the white encapsulation layer **170**. The black encapsulation layer **106** is near to the LED chips even though it may not be in contact with the LED chips. For example and without limitation, the smallest distance between any portion of the black encapsulation layer **106** and any of the LED chips may be less than a threshold distance of 200 μm or less, 150 μm or less, 100 μm or less, or 50 μm or less.

[0067] FIG. **1**O illustrates apparatus **100** with an optional light blocking feature **172**. In general, the light blocking feature **172** can protrude from or be disposed above a surface of apparatus **100**, e.g., from a top-most optional layer **124**. The light blocking feature **172** can be any appropriate shape for

blocking light from a certain direction for the LED chips. For example, the light blocking feature **172** can be a rectangle or a rectangle with an edge opposite the LED chips that tapers away from apparatus **100**, as illustrated in FIG. **1**O.

[0068] The light blocking feature **172**, which can also be called a light blocking element or elements, can be made of any appropriate material and process. For example, epoxy or silicone can be molded or otherwise dispensed, e.g., as described with reference to layers **124** and **106**. Solder mask material can be used. Light blocking feature **172** can be screen printed on, dispensed on, molded on, or rigid piece(s) can be assembled with a suitable adhesive. Solder mask material can have a screen print followed by a pattern exposure and develop.

[0069] FIG. **2**A is a diagram illustrating an example panel **200** of LEDs. Panel **200** can be constructed using arrays of solid state lighting apparatuses such as those illustrated in FIGS. **1**A-I as pixels. A controller **202** is configured to provide power to panel **200** and to control individual LEDs to display, e.g., pictures and video on panel **200**.

[0070] By using apparatus **100** in panel **200**, panel **200** can be made suitable for applications such as signs and indoor/outdoor panels. Using a matte dark or black finish for apparatus **100** allows for high contrast within panel **200** as apparatus **100** can reflect a relatively low amount of light. Opaque sidewalls around apparatus **100** can reduce crosstalk, so that light from one pixel does not leak into neighboring pixels. Since a louver/mesh light barrier can be avoided within panel **200**, the overall pitch of panel **200** can be decreased relative to a panel having a louver/mesh light barrier. Panel **200** can have an improved viewing angle, e.g., as a result of placement of the LEDs chips within the encapsulation layer.

[0071] Panel **200** can be made using materials known not to degrade to improve reliability of panel **200** and to make panel **200** resistant to corrosion, which can be useful, e.g., for outdoor applications. Since panel **200** may be used in places where people may touch it, panel **200** can be made using robust soldering and robust panel assembly. For example, the soldering can use comparatively large pads with better adhesion to ceramic than FR-4, and panel assembly can be prepared with reduced damage to edge components when mating panels or sub-panels. Lack of wire bonds can also improve reliability.

[0072] FIG. **2**B is a cross-section side view of a portion of panel **200**. Panel **200** includes Red Green Blue ("RGB") arrays **204**, which can be made using arrays of solid state lighting apparatuses such as those illustrated in FIGS. **1**A-I as pixels. The areas **206** between RGB arrays **204** can be filled, e.g., at a sub-panel assembly stage or during full panel assembly. RGB arrays **204** can be mounted on a layer **208** that can be, e.g, a motherboard or a sub-panel, which can be flat, or curved convex, concave, cylindrical, spherical, or other shapes. Panel **200** can include one or more sheets **210** of material added for, e.g., protection, anti glare, contrast, consistent look, filtering, light direction, 3D, parallax barrier, lenticular arrays, and so on. For example, sheets **210** can include a protective layer. The protective layer can have a matte finish for reducing specular reflection. The matte finish layer can be roughening on top sides of the LEDs or the black encapsulation layer or both. The protective layer can include optics layers. The protective layer can include diffractive elements. The protective layer can include liquid crystal elements or polarizing elements or both. The protective layer can include light blocking elements.

[0073] Panel **200** can be produced by applying electrically conductive bumps to the panel or the LED chips, joining the panel and the LED chips, and flooding the panel with encapsulation material so that the LED chips are surrounded by the encapsulation material. The electrically conductive bumps can be made from tin-silver-copper (SAC) on Ag. Applying the electrically conductive bumps can include using electroless plating or electrolytic plating. For example, the apparatus **100** illustrated in FIG. **1**I can be extended to a larger array to be used in panel **200**.

[0074] FIG. **3** is a flow diagram of an example process **300** for fabricating a panel of LEDs, e.g., apparatus **100**. In block **302**, the panel or the LEDs chips are bumped, e.g., by adding bumps of solder or Au or any appropriate material. In this case, the panel can be an array of the substrate with

traces, gaps, solder mask vias, and the like already formed. For example, the panel can come from a PCB manufacturer.

[0075] The solder can include eutectic metals. For example, AuSn or low cost die attach (LCDA) metals can applied to the pads of the LEDs; in some examples, tin-silver-copper (SAC) or other Pb free solder can be used, e.g., SAC 305. The pads on the LED chips can be a eutectic or non-eutectic solder. The shape of the pads on the LED chips can be, e.g., round, square, or other. The pads can be substantially flat. The LCDA can be a low temperature die attach metal, e.g., that melts at a temperature below 250° C.

[0076] In block **304**, the panel and the LED chips are joined, creating an electrical connection between the panel and the chips. The joint is established by providing energy (force, temperature, ultrasonic). In block **306**, the chips are optionally underfilled, e.g., using any appropriate underfill material. The underfill material can be clear, white, or dark or black; white and black are both opaque and can block light leakage through the substrate. Mirrors made of metal or a dielectric can be used on the sides and/or the bottom of the chips to increase brightness with a low impact on contrast. In some examples, diffuse reflectors can be used on sides of the chips—e.g., using the same material as a white underfill, wetting up the sides of the chips.

[0077] In block **308**, the surface is optionally coated with white encapsulation. In block **310**, the panel is flooded with dark or black encapsulation. In some examples, the dark or black encapsulation layer can cover the LED chips, e.g., if the dark or black encapsulation layer is thin enough. In some examples, the LED chips are configured so that the dark or black encapsulation layer does not wet to the LED chips. For example, the LED chips can be configured using an adjustment to the surface tension of the LED chips, e.g., to have a high surface angle.

[0078] In block **312**, the panel is cured. In block **314**, an optional surface treatment or coating is performed, e.g., grinding, lapping, and the like. In block **316**, the panel is tested, e.g., using any appropriate electrical testing equipment, and the panel is diced, e.g., into sub-panels or into full individual components. In block **318**, the components are sorted, taped, and packaged. In some examples, the whole panel or individual sub-panels can be buffed and/or lapped and/or bead blasted to create a visually appealing finish lacking seams. The order of the process flow can be switched or otherwise reordered. For example, the components can be singulated before test.

[0079] FIG. **4** is a flow diagram of an example process **400** for fabricating a panel of LEDs, e.g., apparatus **100**. In block **402**, Ag epoxy dots are dispensed on the panel. In block **404**, the LED chips are placed on the dots and the panel is cured to join the chips to the panel.

[0080] In some implementations, using Ag epoxy can result in smearing out. One solution is to use a solder mask with appropriate openings, e.g., as illustrated in FIG. **1**H. The openings can be squeegeed over to dispense the Ag epoxy and place the chip. The openings can be made in various shapes and have paths cutout so that excess epoxy will be squeezed away from the chip when the chip is placed. The Ag epoxy can be dispensed in any appropriate manner, e.g., such as with jet printing. In that case, the desired spot may be overfilled, slightly, and the excess goes into a weeping path as the chip is placed. This can be useful, e.g., to keep the Ag epoxy dots from squeezing together and shorting the device. Larger particles can be added to the Ag epoxy dots, e.g., to help control the rheometry and thickness of the LED chips and/or the panel itself.

[0081] In block **406**, the chips are optionally underfilled, e.g., using any appropriate underfill material. In block **408**, the surface is optionally coated with white encapsulation. In block **410**, the panel is flooded with dark or black encapsulation. In block **412**, the panel is cured. In block **414**, an optional surface treatment or coating is performed, e.g., grinding, lapping, and the like. In block **416**, the panel is tested, e.g., using any appropriate electrical testing equipment, and the panel is diced, e.g., into sub-panels or into full individual panels. In block **418**, the panel is sorted, taped, and packaged.

[0082] FIG. **5**A is a diagram illustrating an LED chip **502** being attached using Ag epoxy. The chip includes a substrate **504**, e.g., made using sapphire, an n-type layer **506**, a p-type layer **508**, and a

passivation layer **510**. The contacts for LED chip **502** face conductive trace material **512** on a panel **514**. Ag epoxy **516** is applied to the trace material **512**, and then LED chip **502** is placed on the Ag epoxy **516**. In some circumstances, the Ag epoxy may flow during the mounting process, resulting in a short between the p-type contact and the n-type layer **506**, which can interfere with the operation of LED chip **502**.

[0083] FIG. **5**B is a perspective view of an LED chip **502** being attached using Ag epoxy to trace material **512** having trenches **518***a-b* in the trace material. FIG. **5**C is a side view of the LED chip **502** being attached.

[0084] By carving trenches **518***a-b* into trace material **512**, the Ag epoxy **516** can flow into trenches **518***a-b* instead of upwards around LED chip **502**, thereby preventing a short between the p-type contact and the n-type layer **506** or other types of short circuits. Trenches **518***a-b* can be any appropriate shape and depth for receiving an amount of Ag epoxy **516** to prevent short circuits.

[0085] FIG. **5**D is a diagram illustrating that the n-pad and the p-pad an LED chip **502** can be coplanar. The n-pad and the p-pad can be coplanar or substantially coplanar, i.e., so that the bottoms of both the n-pad and the p-pad extend to a same plane **520**. The pads would be considered substantially coplanar if they would be exactly coplanar except for normal manufacturing variance, e.g., differences between the targeted and actual thicknesses of the individual n and p pads. In some examples, the term substantially coplanar includes a maximum variation of +/−25 μm. The average variation may be smaller, e.g., about 5 μm.

[0086] Direct attach chips can be made so that the pads are nearly coplanar, but they do not necessarily need to be made that way. For example, solder bumps can be used for attachment so that differences in the solder compensate for differences in the thicknesses of the n-pad and the p-pad while keeping LED chip **502** substantially level. In some examples, the polarity of LED chip **502** can be reversed from the polarity illustrated in FIG. **5**D. As illustrated, LED chip **502** is a typical blue and green structure, but other examples such as red LED chips can have the n-pad on the mesa **508**.

[0087] FIG. **6** is a flow diagram of an example method **600** for producing LED devices. A number of LED die are fabricated on a wafer using any appropriate LED fabrication technique (**602**). While the LED die are on the wafer, die attach material is incorporated to each of the LEDs (**604**). Incorporating the die attach material can include providing or forming AuSn bondpads on the LED die. In some examples, incorporating the die attach material includes forming bond pads as low cost die attach (LCDA) bond pads. Solder such as SAC305 can also be used for example.

[0088] The wafer is diced to separate the LED die (**606**). For example, the wafer can be diced using a wafer saw. The LED die are attached to at least one substrate, and possibly one substrate for each of the diced LED die, using the die attach material incorporated while the LED die were on the wafer (**608**). Attaching the LED die can include performing a flux-eutectic bonding process using AuSn or other solder-bumped bondpads.

[0089] FIG. **7** is a flow diagram of an example method **700** for producing LED devices. Solder bumps are stencil printed onto LEDs or the substrate (**702**). The LED chips are placed onto a panel (**704**). For example, the LED chips can placed over electrical traces that run through the panel. The solder bumps are reflowed to electrically connect the LED chips to the panel (**706**).

[0090] While the subject matter has been has been described herein in reference to specific aspects, features, and illustrative embodiments, it will be appreciated that the utility of the subject matter is not thus limited, but rather extends to and encompasses numerous other variations, modifications and alternative embodiments, as will suggest themselves to those of ordinary skill in the field of the present subject matter, based on the disclosure herein.

[0091] Aspects disclosed herein can, for example and without limitation, provide one or more of the following beneficial technical effects: reduced cost of providing solid state lighting apparatuses; reduced size, volume, or footprint of solid state lighting apparatuses; improved efficiency; improved color rendering; improved thermal management; simplified circuitry; improved contrast,

improved viewing angle; improved color mixing; improved reliability; and/or simplified DC or AC operability.

[0092] Various combinations and sub-combinations of the structures and features described herein are contemplated and will be apparent to a skilled person having knowledge of this disclosure. Any of the various features and elements as disclosed herein can be combined with one or more other disclosed features and elements unless indicated to the contrary herein. Correspondingly, the subject matter as hereinafter claimed is intended to be broadly construed and interpreted, as including all such variations, modifications and alternative embodiments, within its scope and including equivalents of the claims.

Claims

1. A method of producing a panel of light emitting diodes (LEDs), the method comprising: applying a plurality of electrically conductive bumps to the panel or to at least one of a plurality of LED chips; joining the panel and the plurality of LED chips; and flooding the panel with a dark encapsulation material so that the plurality of LED chips are surrounded by the dark encapsulation material.

2. The method of claim 1, further comprising coating the panel with a white encapsulation material prior to flooding the panel with the dark encapsulation material.

3. The method of claim 1, further comprising grinding, lapping, sanding, polishing, burnishing, and/or media blasting a surface of the panel resulting in the plurality of LED chips being coplanar with or within 25 μm or less of the dark encapsulation material.

4. The method of claim 1, further comprising grinding, lapping, sanding, polishing, burnishing, and/or media blasting a surface of the panel resulting in the plurality of LED chips being below the dark encapsulation material.

5. The method of claim 4, wherein the surface of the panel comprises a matte finish after the grinding, lapping, sanding, polishing, burnishing, and/or media blasting.

6. The method of claim 1, further comprising using a material removal process causing a plurality of top surfaces of the plurality of LED chips to be coplanar or within 25 μm or less of the dark encapsulation material.

7. The method of claim 1, wherein the plurality of electrically conductive bumps comprise solder paste.

8. The method of claim 7, wherein the solder paste is stencil printed on the panel.

9. The method of claim 1, further comprising adding a diffuse top layer over the plurality of LED chips or the dark encapsulation material or both, resulting in a matte finish or a modified light emission pattern.

10. The method of claim 9, further comprising curing the panel before adding the diffuse top layer.

11. The method of claim 1, wherein: the panel comprises a substrate and a plurality of electrically conductive top traces on the substrate; the plurality of electrically conductive top traces are entirely external to the substrate; and joining the panel and the plurality of LED chips comprises electrically connecting the plurality of LED chips to the plurality of electrically conductive top traces by the plurality of electrically conductive bumps.

12. A method for producing a panel of light emitting diodes (LEDs), the method comprising: applying a plurality of electrically conductive bumps or solder paste to the panel or to at least one LED chip, wherein the electrically conductive bumps comprise tin-silver-copper (SAC) on silver (Ag); joining the panel and the at least one LED chip; and flooding the panel with a dark encapsulation material so that the at least one LED chip is surrounded by the dark encapsulation material.

13. The method of claim 12, further comprising coating the panel with a white encapsulation material prior to flooding the panel with the dark encapsulation material.

14. The method of claim 12, further comprising grinding, lapping, sanding, polishing, burnishing, and/or media blasting a surface of the panel resulting in the at least one LED chip being coplanar with or within 25 μm or less of the dark encapsulation material.

15. The method of claim 12, wherein: the panel comprises a substrate and a plurality of electrically conductive top traces on the substrate; the plurality of electrically conductive top traces are entirely external to the substrate; and joining the panel and the at least one LED chip comprises electrically connecting the at least one LED chip to the plurality of electrically conductive top traces by the plurality of electrically conductive bumps.

16. The method of claim 15, wherein Ag is applied to the plurality of electrically conductive traces using immersion plating, electroless plating, or electrolytic plating.

17. A method for producing a light emitting diode (LED) apparatus, the method comprising: applying an encapsulant to or around one or more LEDs; and after application of the encapsulant, planarizing the encapsulant to expose the one or more LEDs.

18. The method of claim 17, comprising planarizing the encapsulant such that a top surface of the one or more LEDs is coplanar or within 25 μm or less of the encapsulant.

19. The method of claim 17, wherein: the apparatus comprises a substrate and a plurality of electrically conductive top traces on the substrate; and the plurality of electrically conductive top traces are entirely external to the substrate.

20. The method of claim 19, wherein: the encapsulant is a dark encapsulation layer that surrounds side surfaces of the one or more LEDs; the dark encapsulation layer is less than 200 μm away from each of the side surfaces of the one or more LEDs; a reflective layer is formed on the side surfaces of the one or more LEDs such that the reflective layer is arranged between the side surfaces of the one or more LEDs and the dark encapsulation layer; and the reflective layer extends on a surface of the substrate adjacent the one or more LEDs, and the reflective layer is between a bottom surface of the one or more LEDs and the substrate.