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Lin et al.

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(54) **ISOLATION WITH MULTI-STEP STRUCTURE**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 149 days.

(21) Appl. No.: **18/343,947**

(22) Filed: **Jun. 29, 2023**

(65) **Prior Publication Data**

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Related U.S. Application Data

(60) Continuation of application No. 17/583,707, filed on Jan. 25, 2022, now Pat. No. 11,728,206, which is a (Continued)

(51) **Int. Cl.**
H01L 21/762 (2006.01)
H10D 30/62 (2025.01)
(Continued)

(52) **U.S. Cl.**
CPC .. ***H01L 21/76232*** (2013.01); ***H01L 21/76224*** (2013.01); ***H10D 30/6211*** (2025.01);
(Continued)

(58) **Field of Classification Search**
CPC H01L 21/76232; H10D 84/0151–0153; H10D 84/0158; H10D 84/038; H10D 84/834; H10D 84/853; H10D 84/859
See application file for complete search history.

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Primary Examiner — Daniel P Shook

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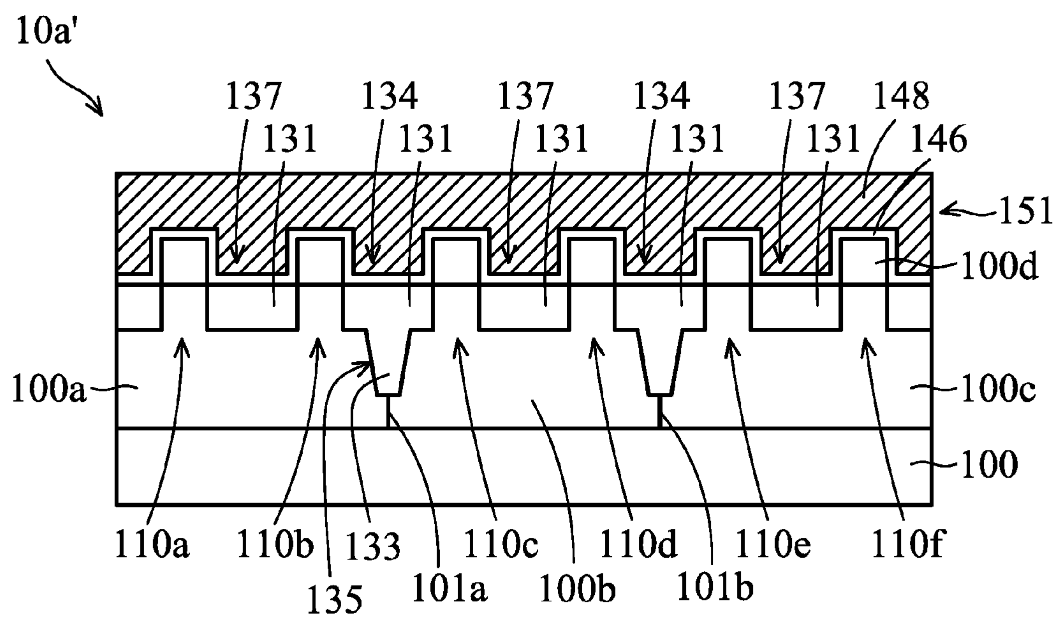
(57) **ABSTRACT**

A semiconductor device structure is provided. The semiconductor device structure includes a semiconductor substrate including a first well region of a first conductivity type. The semiconductor device structure also includes a first fin structure and an adjacent second fin structure formed in and protruding from the first well region. The semiconductor device structure also includes a first isolation structure formed in the first well region between the first fin structure and the second fin structure. A first sidewall surface of the first fin structure faces to a second sidewall surface of the second fin structure. The first sidewall surface and the second sidewall surface each extend along at least two directions from a bottom of the first isolation structure to a top of the first isolation structure.

20 Claims, 20 Drawing Sheets



Related U.S. Application Data

continuation of application No. 17/018,397, filed on Sep. 11, 2020, now Pat. No. 11,251,069, which is a division of application No. 16/211,949, filed on Dec. 6, 2018, now Pat. No. 10,790,184.

(60) Provisional application No. 62/738,305, filed on Sep. 28, 2018.

(51) **Int. Cl.**

H10D 62/10	(2025.01)
H10D 64/01	(2025.01)
H10D 84/01	(2025.01)
H10D 84/03	(2025.01)
H10D 84/83	(2025.01)
H10D 84/85	(2025.01)

(52) **U.S. Cl.**

CPC ***H10D 62/115*** (2025.01); ***H10D 64/015*** (2025.01); ***H10D 64/017*** (2025.01); ***H10D 84/0151*** (2025.01); ***H10D 84/0158*** (2025.01); ***H10D 84/0188*** (2025.01); ***H10D 84/0191*** (2025.01); ***H10D 84/0193*** (2025.01); ***H10D 84/038*** (2025.01); ***H10D 84/834*** (2025.01); ***H10D 84/853*** (2025.01); ***H10D 84/859*** (2025.01)

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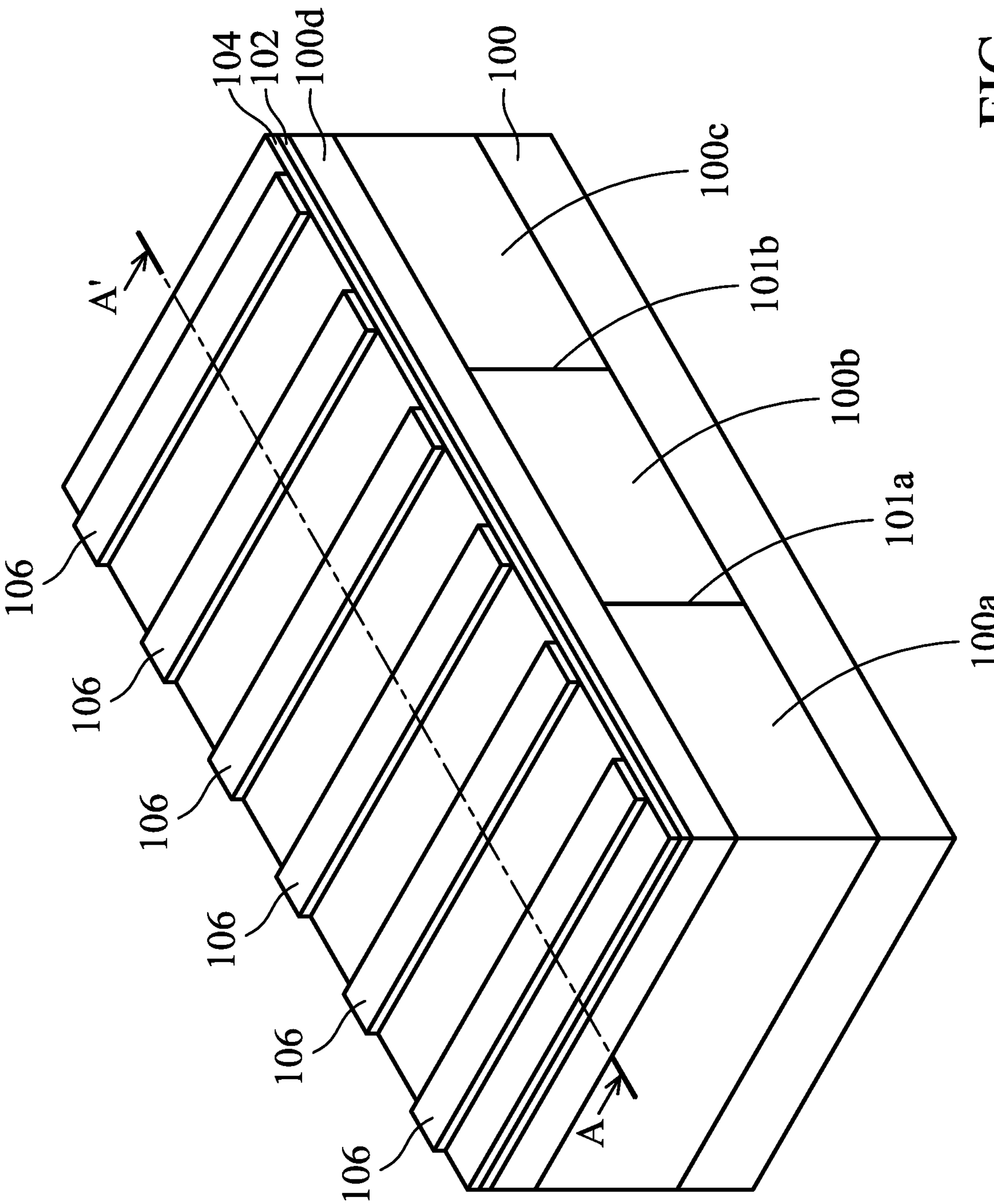
104
102
100d
100
100c
101b
100b
101a
100a
A'
A
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106
106
106
106
106

FIG. 1A

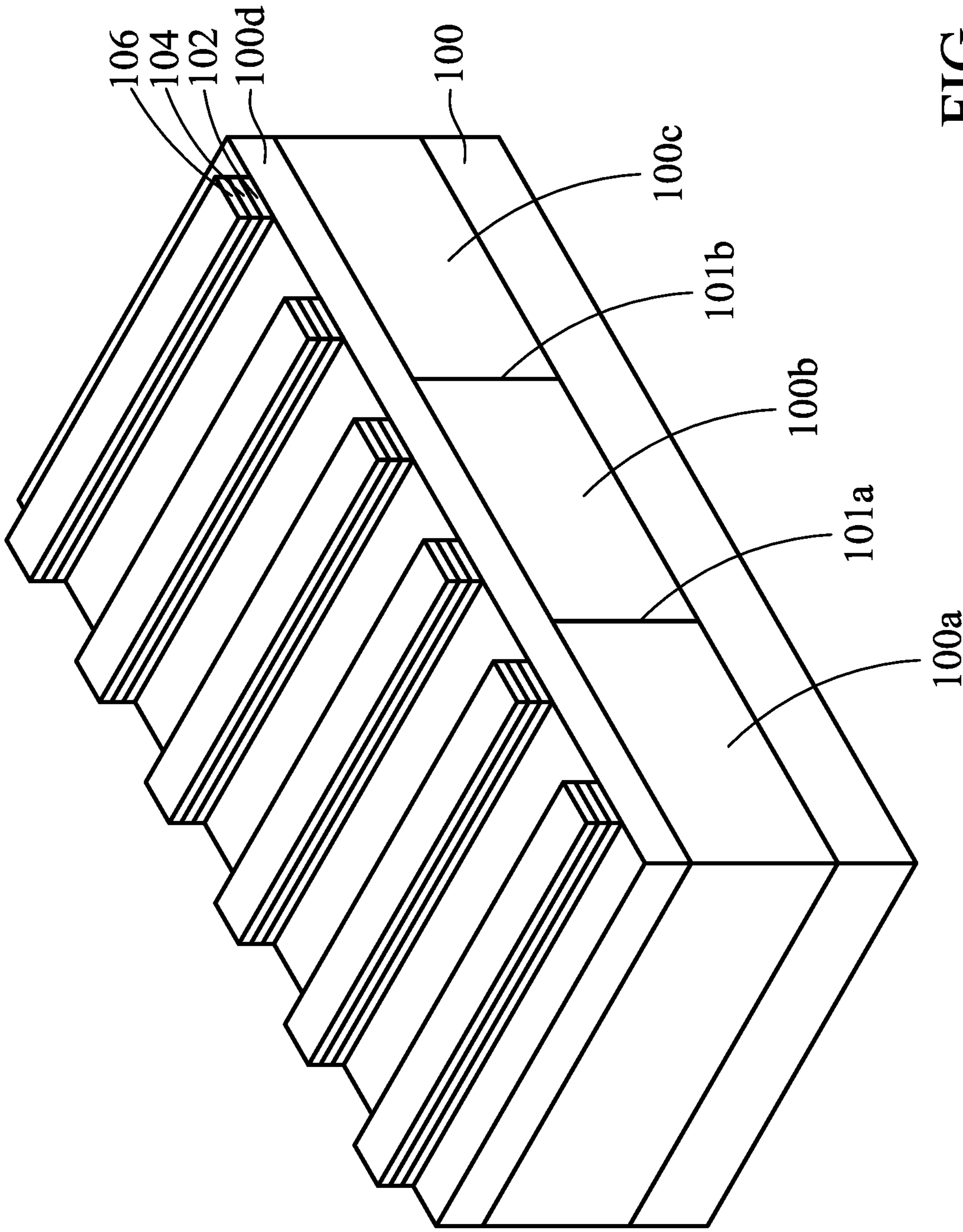
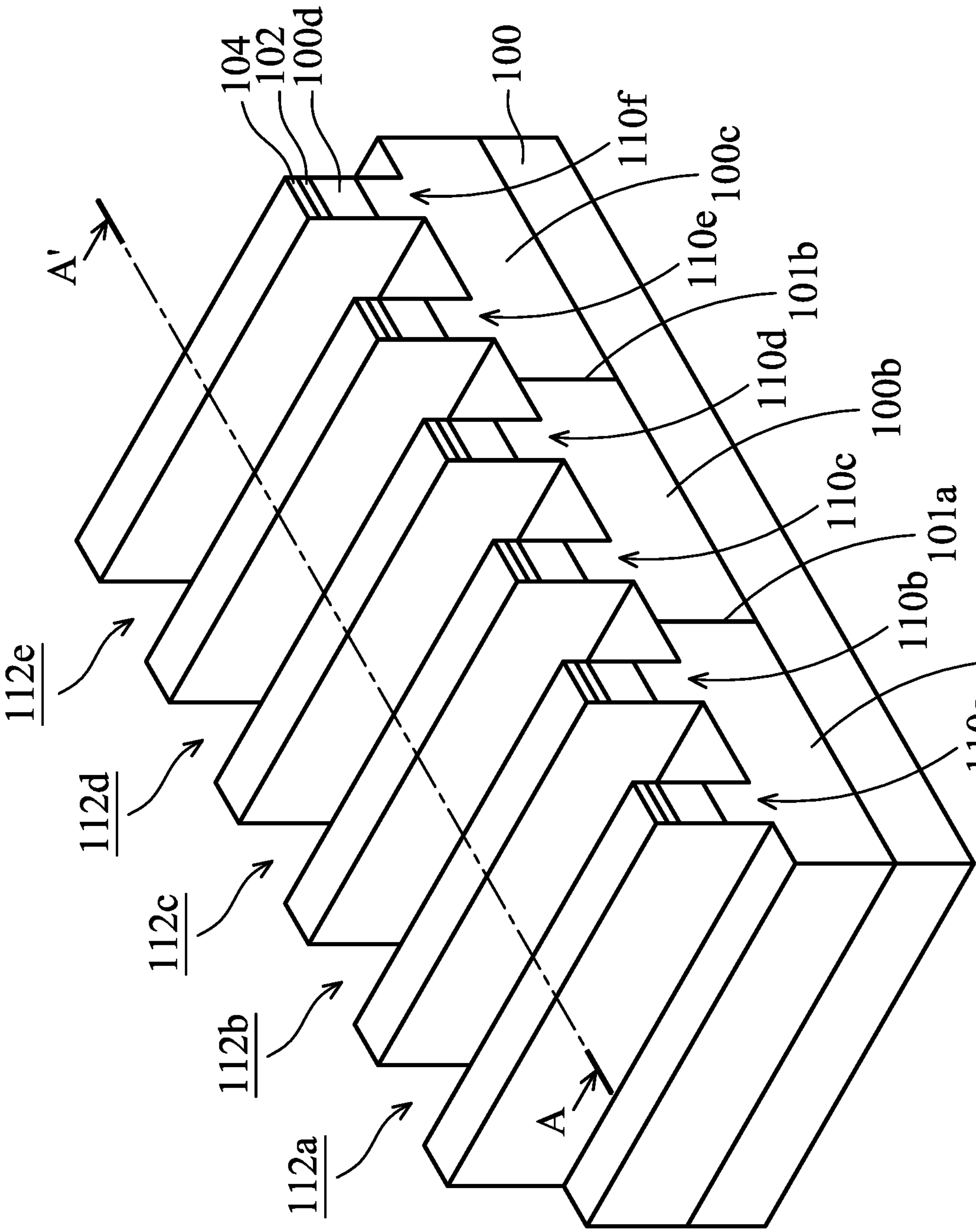


FIG. 1B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110e
101b
110d
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110c
101a
110b
100a
110a
A'
A
112e
112d
112c
112b
112a

FIG. 1C

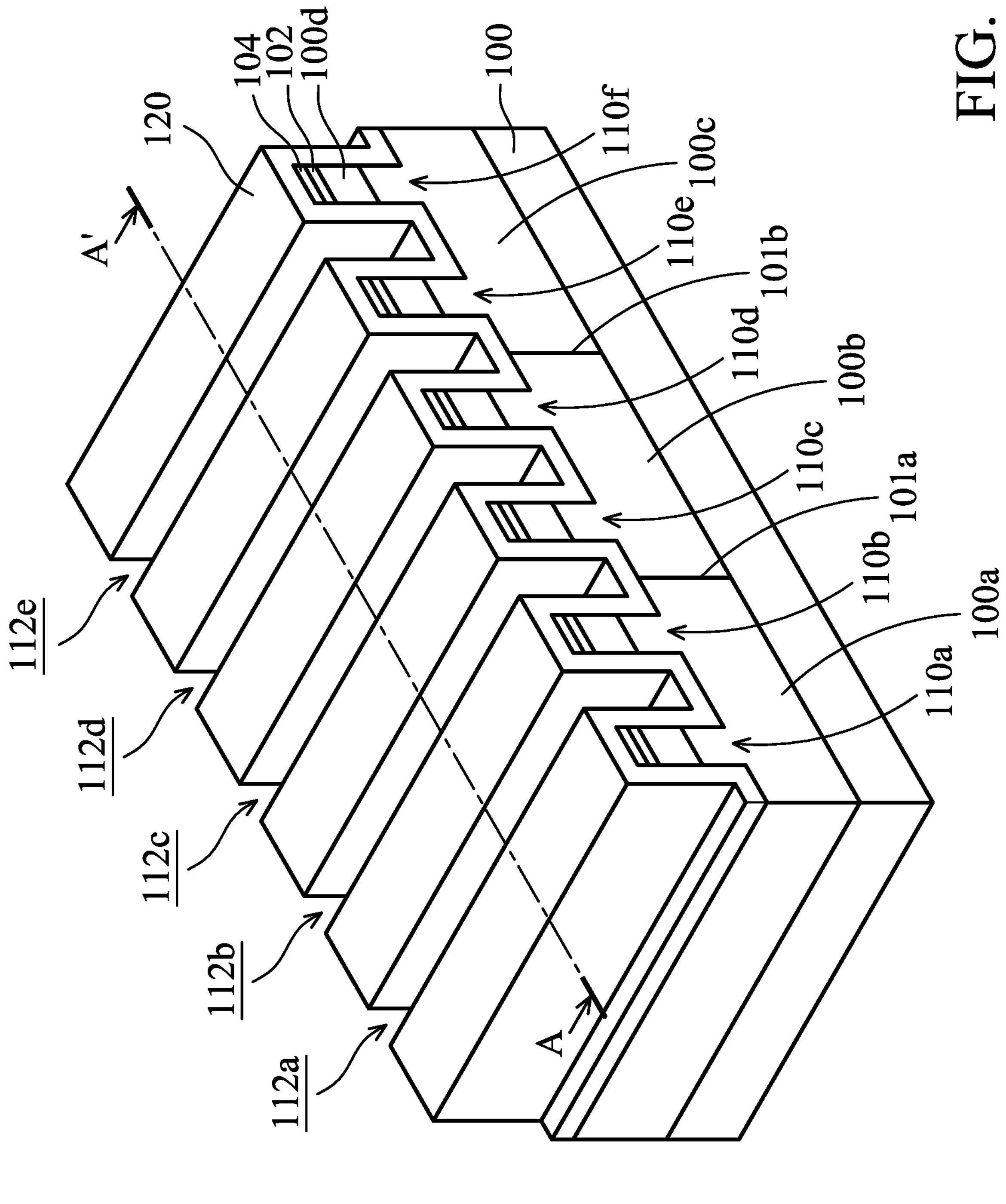

120
104
102
100d
100
110f
100c
110e
101b
110d
100b
110c
101a
110b
100a
110a
A'
A
112e
112d
112c
112b
112a

FIG. 1D

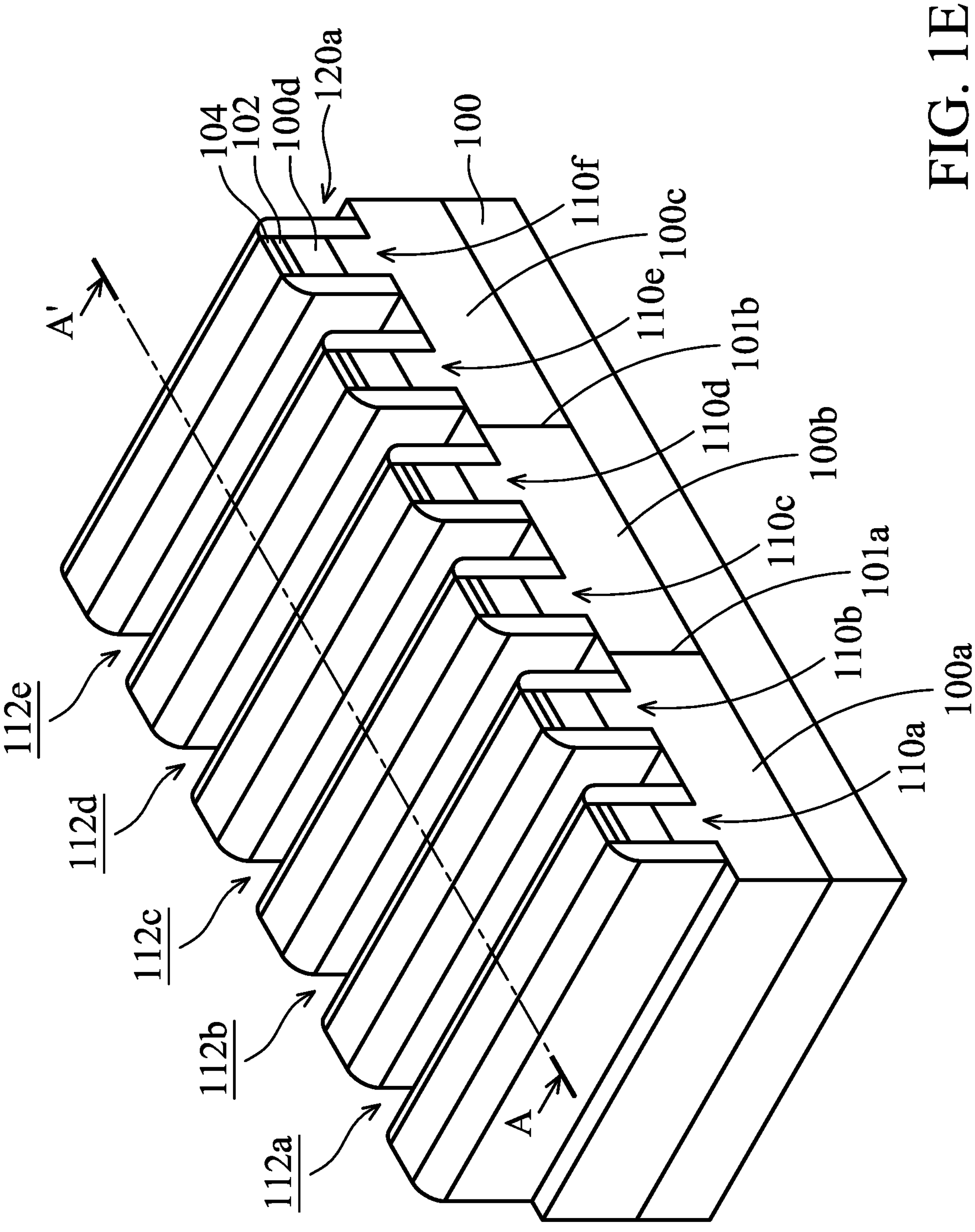

104
102
100d
120a
100
110f
100c
110e
101b
110d
100b
110c
101a
110b
100a
110a
A'
A
112e
112d
112c
112b
112a

FIG. 1E

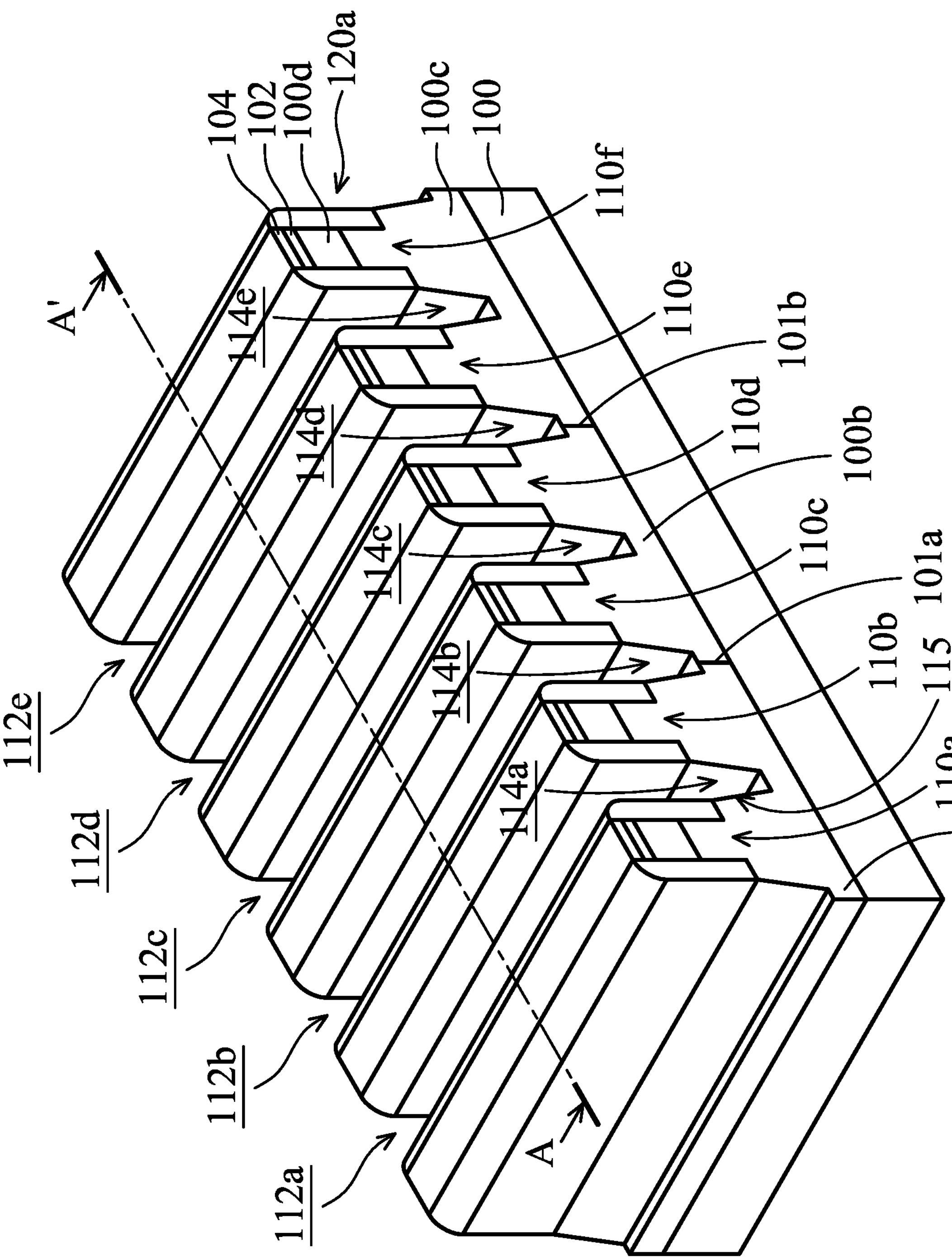
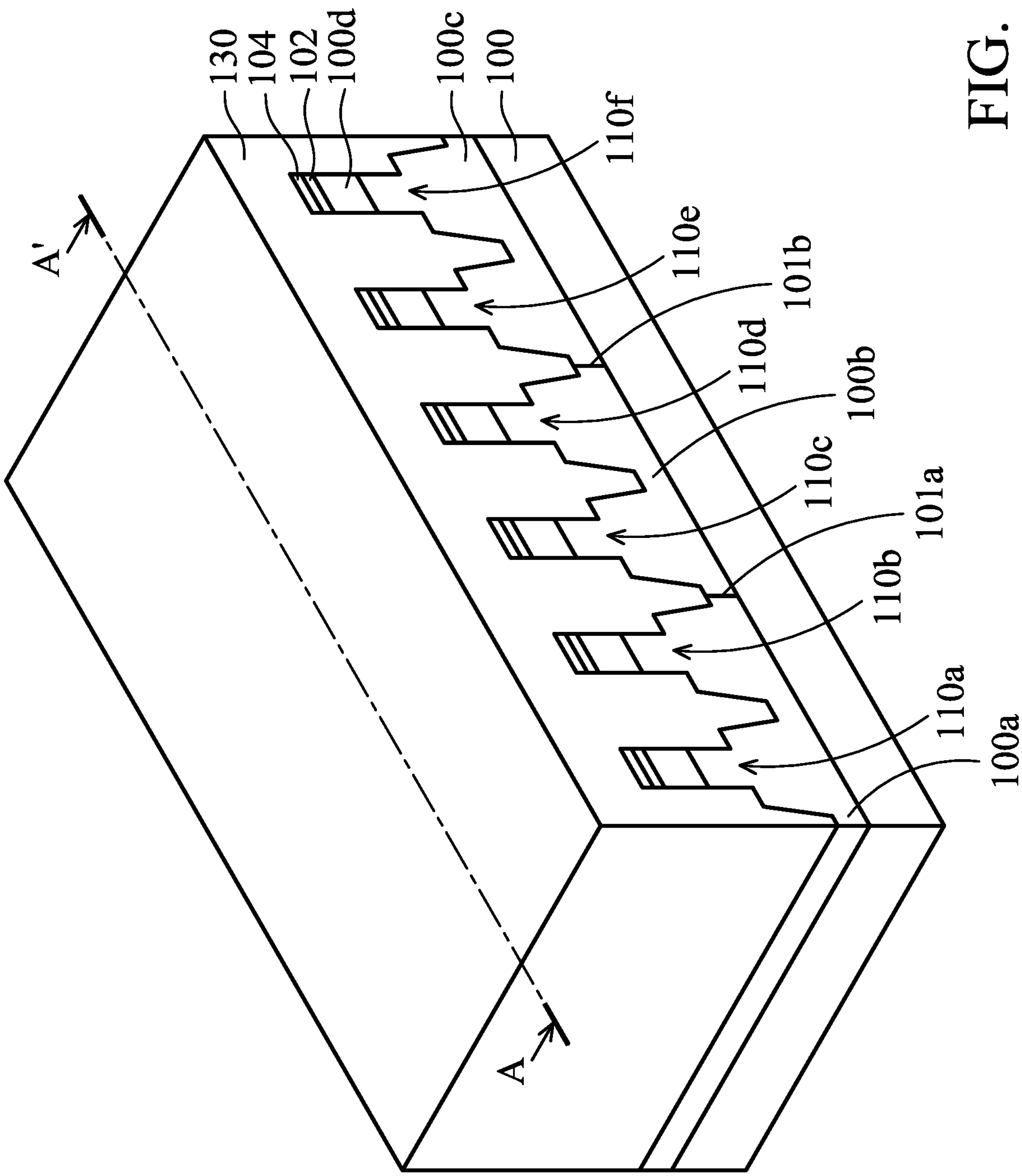

104
102
100d
120a
100c
100
110f
A'
114e
110e
101b
114d
110d
100b
114c
110c
101a
114b
110b
115
114a
110a
100a
112e
112d
112c
112b
112a
A

FIG. 1F



A'
A
130
104
102
100d
100c
100
110f
110e
101b
110d
100b
110c
101a
110b
110a
100a

FIG. 1G

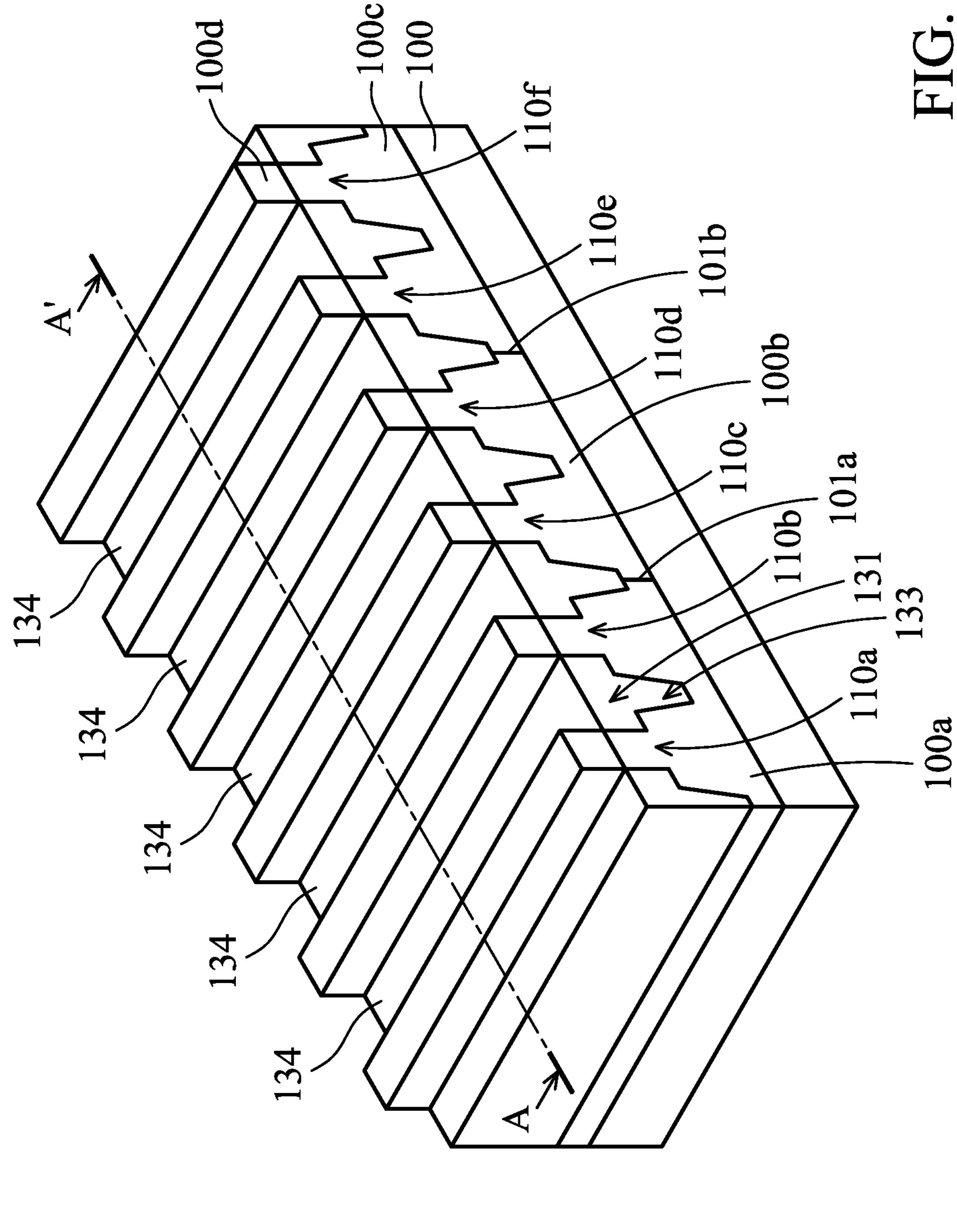

100d
100c
100
110f
110e
101b
A'
110d
100b
110c
101a
110b
131
133
110a
100a
134
134
134
134
134
A

FIG. 1H

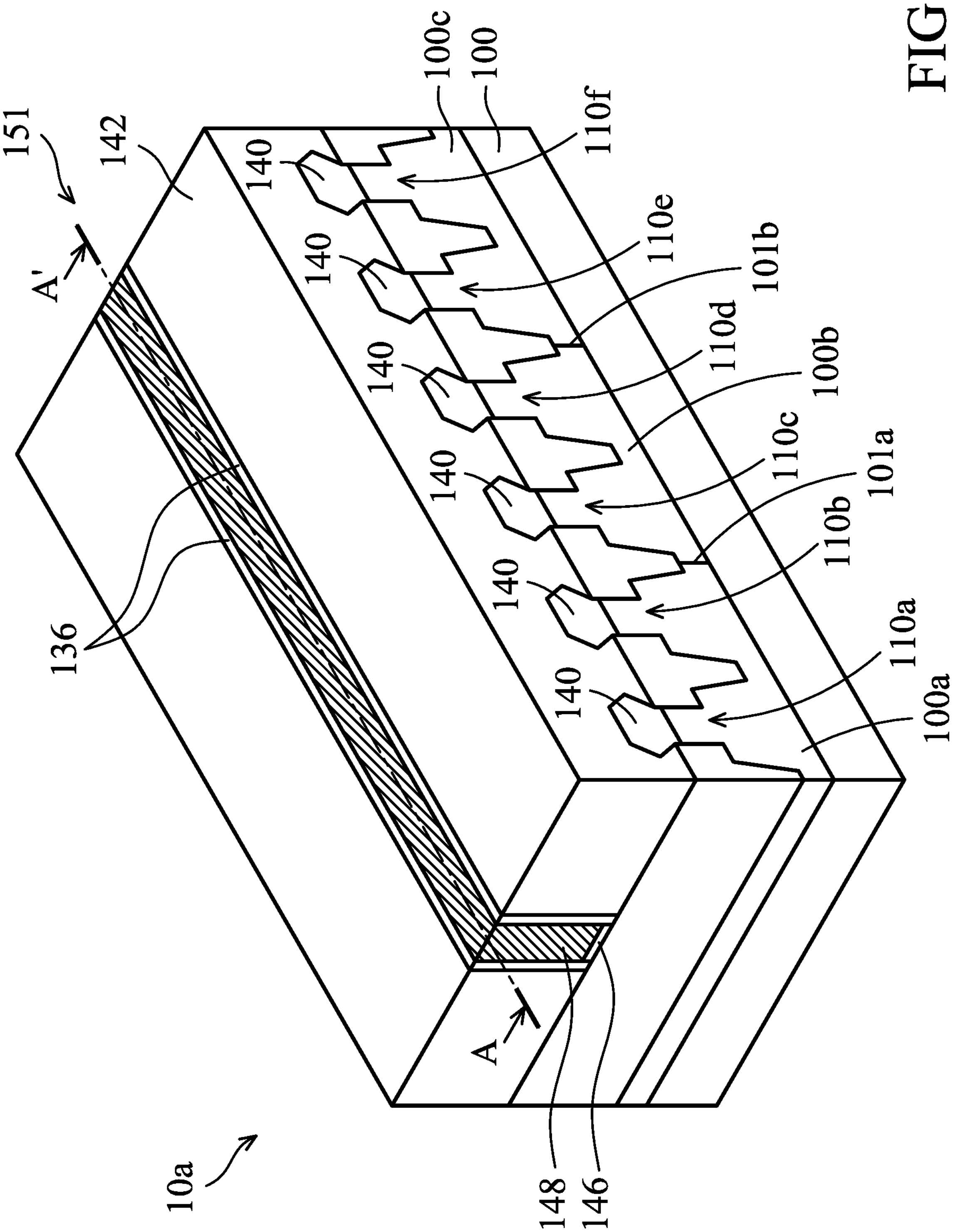
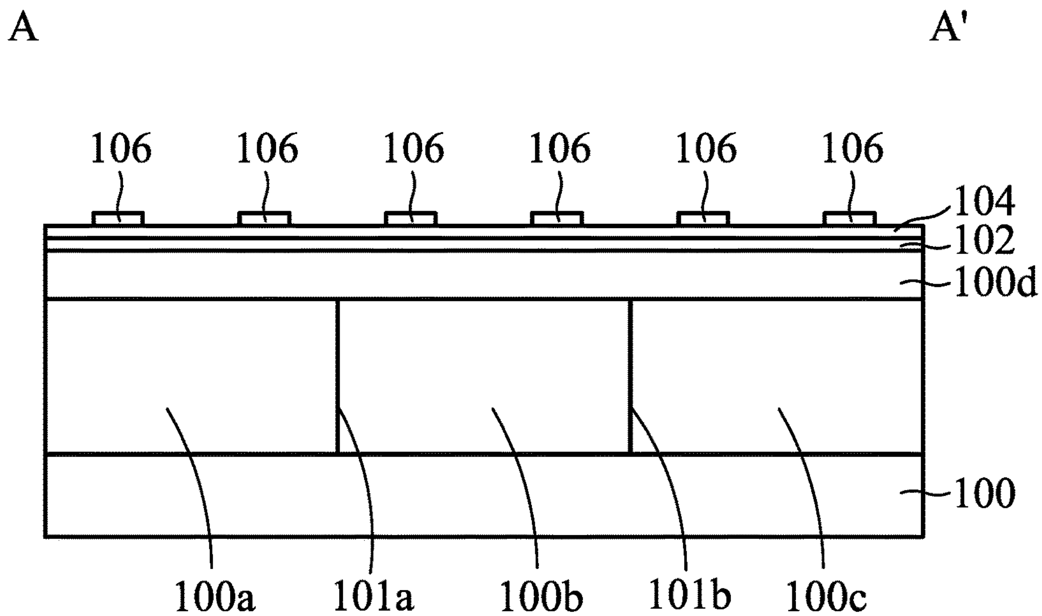

151
142
A'
136
100c
100
110f
140
110e
101b
110d
100b
110c
101a
110b
110a
100a
A
10a
148
146

FIG. 1I


A
A'
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106
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106
104
102
100d
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101a
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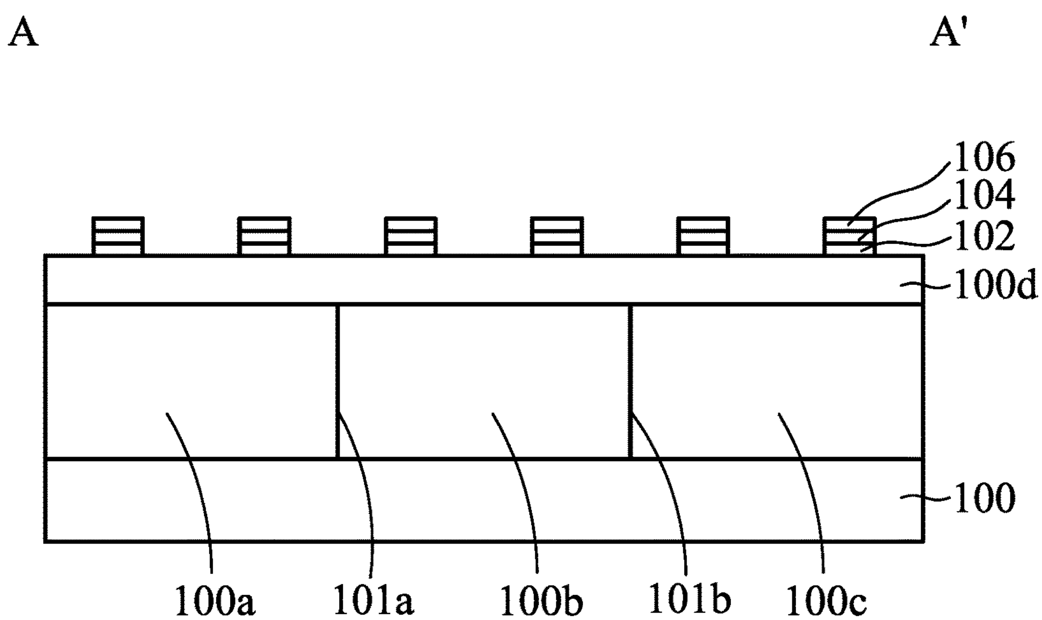
100c

FIG. 2A


A
A'
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104
102
100d
100
100a
101a
100b
101b
100c

FIG. 2B

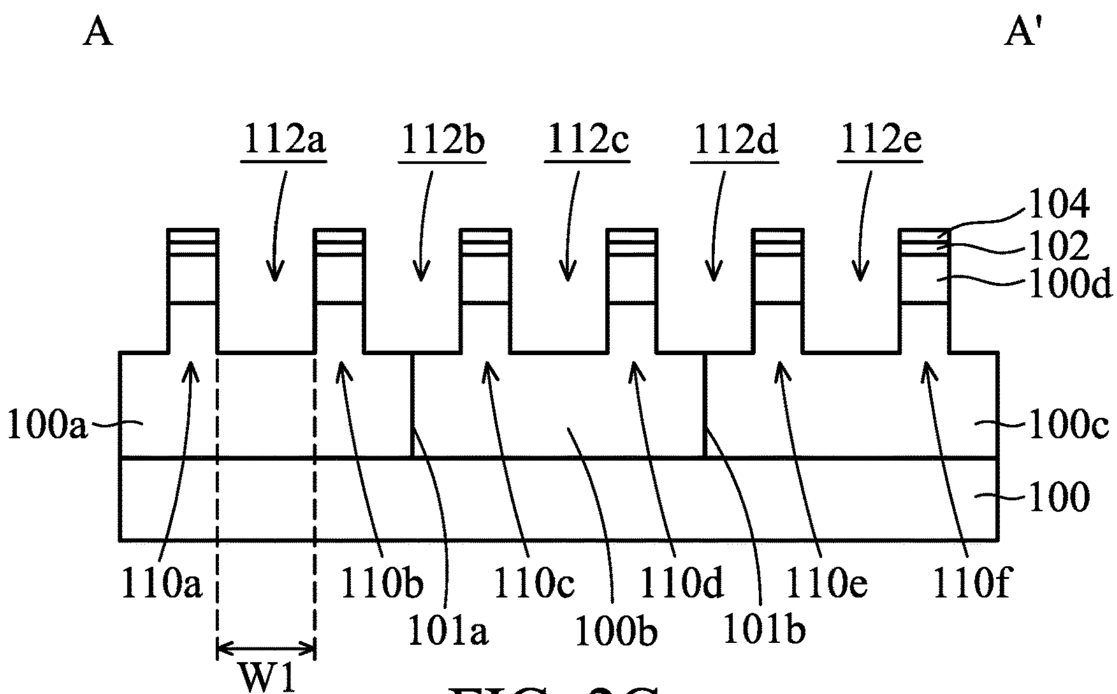
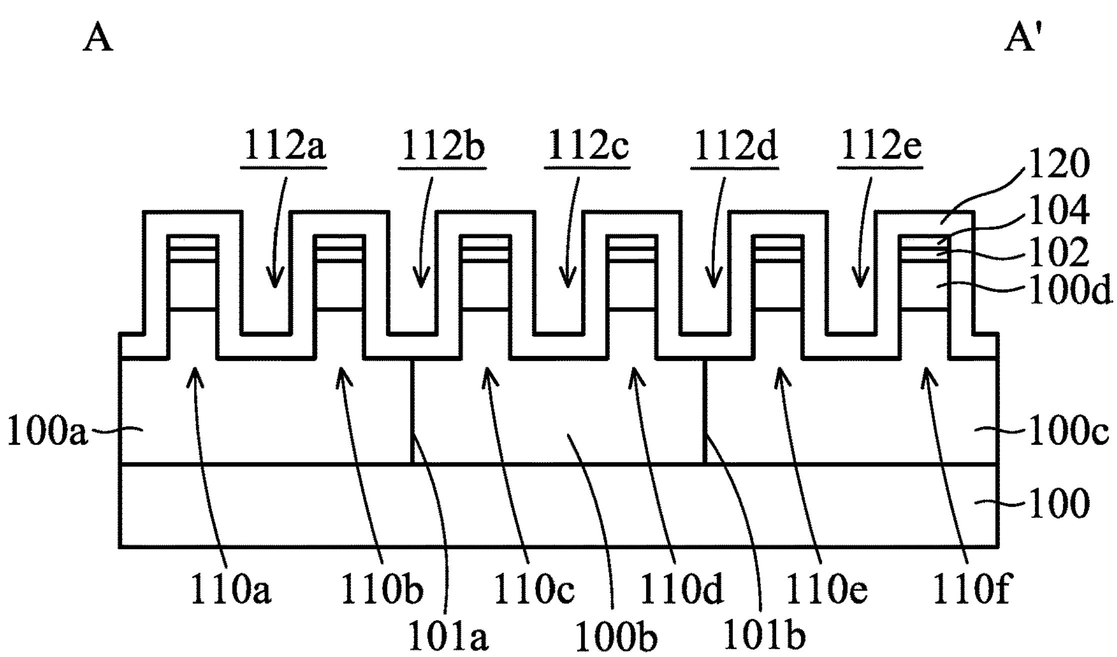

A
A'
112a
112b
112c
112d
112e
104
102
100d
100a
100c
100
110a
110b
110c
110d
110e
110f
101a
100b
101b
W1

FIG. 2C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A'
112a
112b
112c
112d
112e
120
104
102
100d
100a
100c
100
110a
110b
110c
110d
110e
110f
101a
100b
101b

FIG. 2D

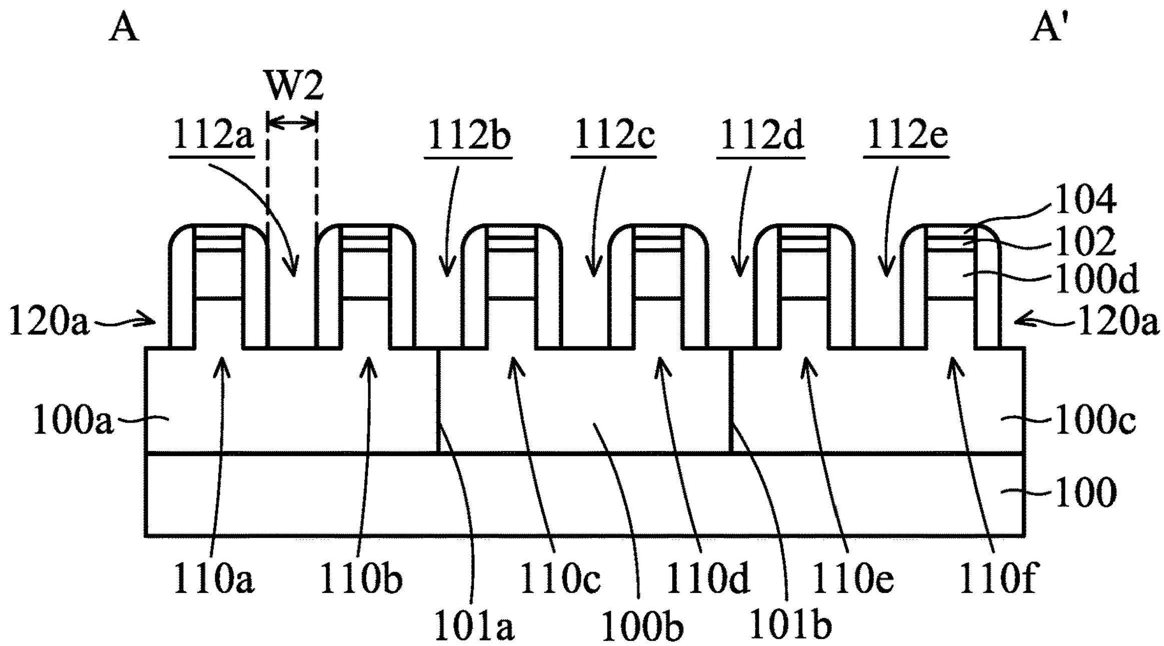

A
A'
W2
112a
112b
112c
112d
112e
104
102
100d
120a
120a
100a
100c
100
110a
110b
110c
110d
110e
110f
101a
100b
101b

FIG. 2E

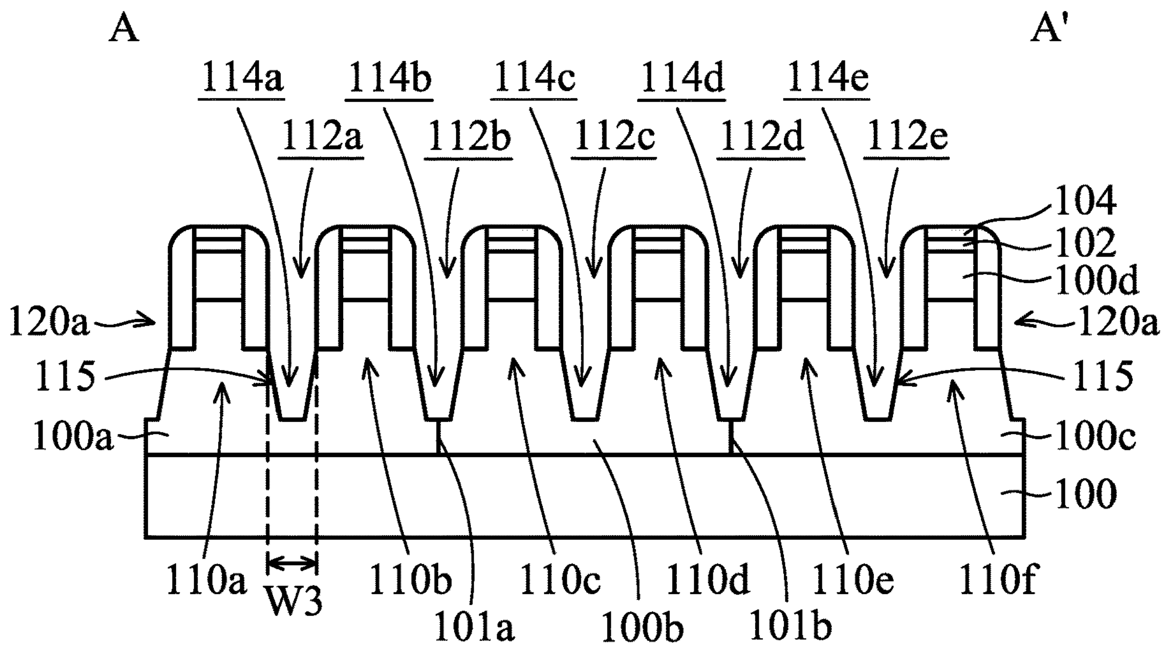
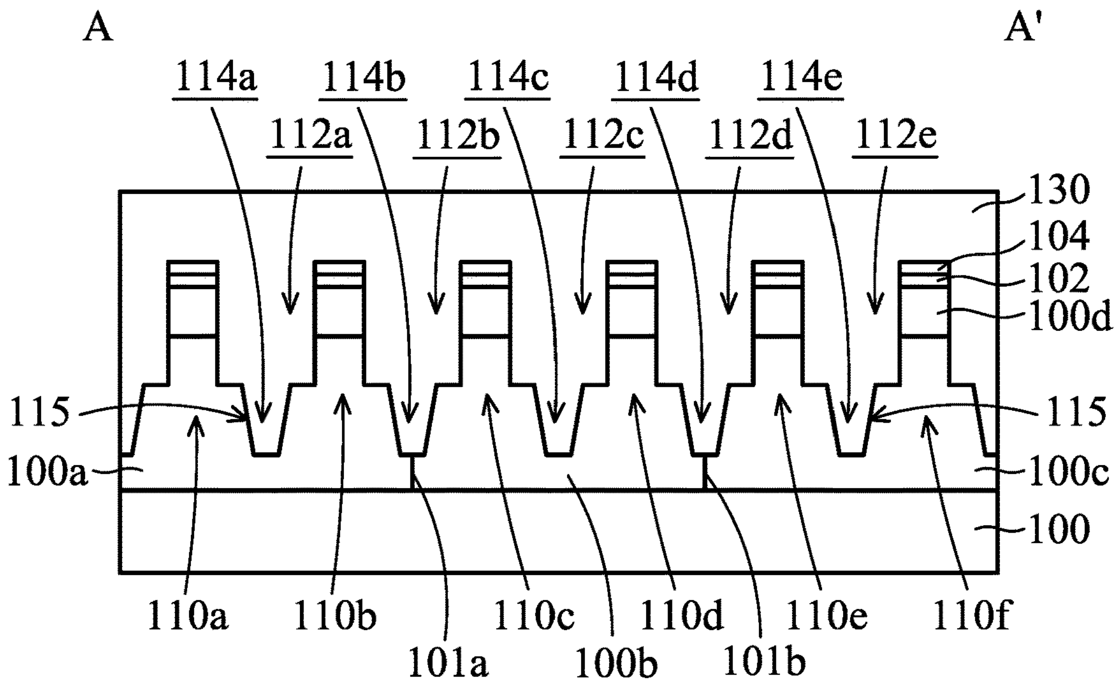

A
A'
114a
114b
114c
114d
114e
112a
112b
112c
112d
112e
104
102
100d
120a
120a
115
115
100a
100c
100
110a
W3
110b
110c
110d
110e
110f
101a
100b
101b

FIG. 2F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A'
114a
114b
114c
114d
114e
112a
112b
112c
112d
112e
130
104
102
100d
115
115
100a
100c
100
110a
110b
110c
110d
110e
110f
101a
100b
101b

FIG. 2G

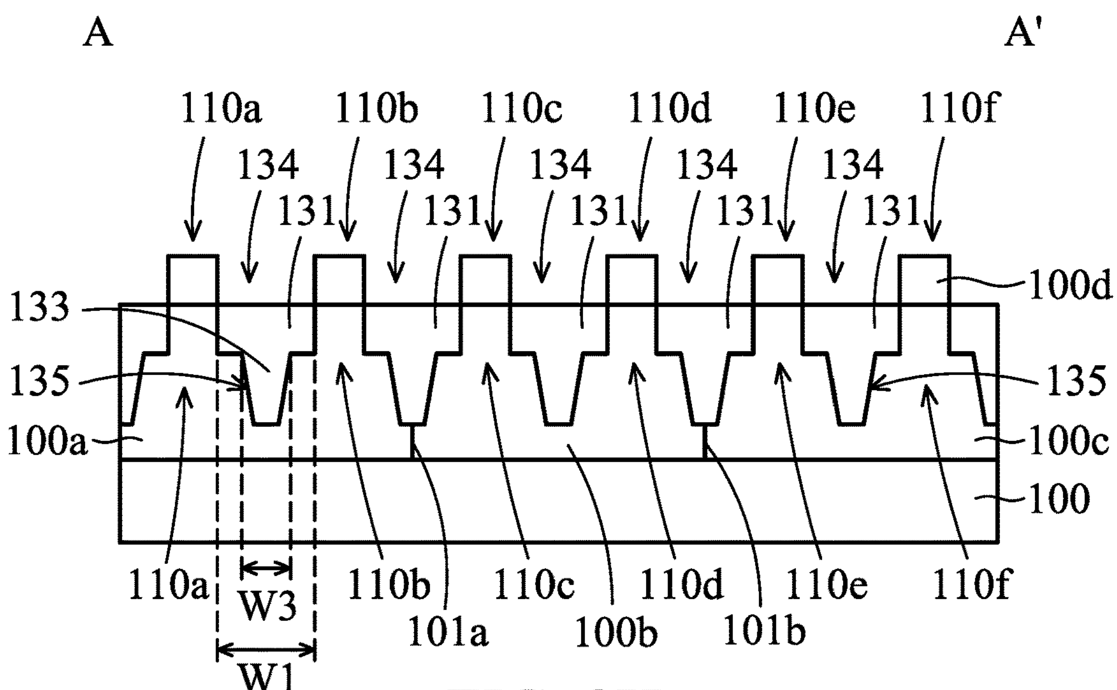
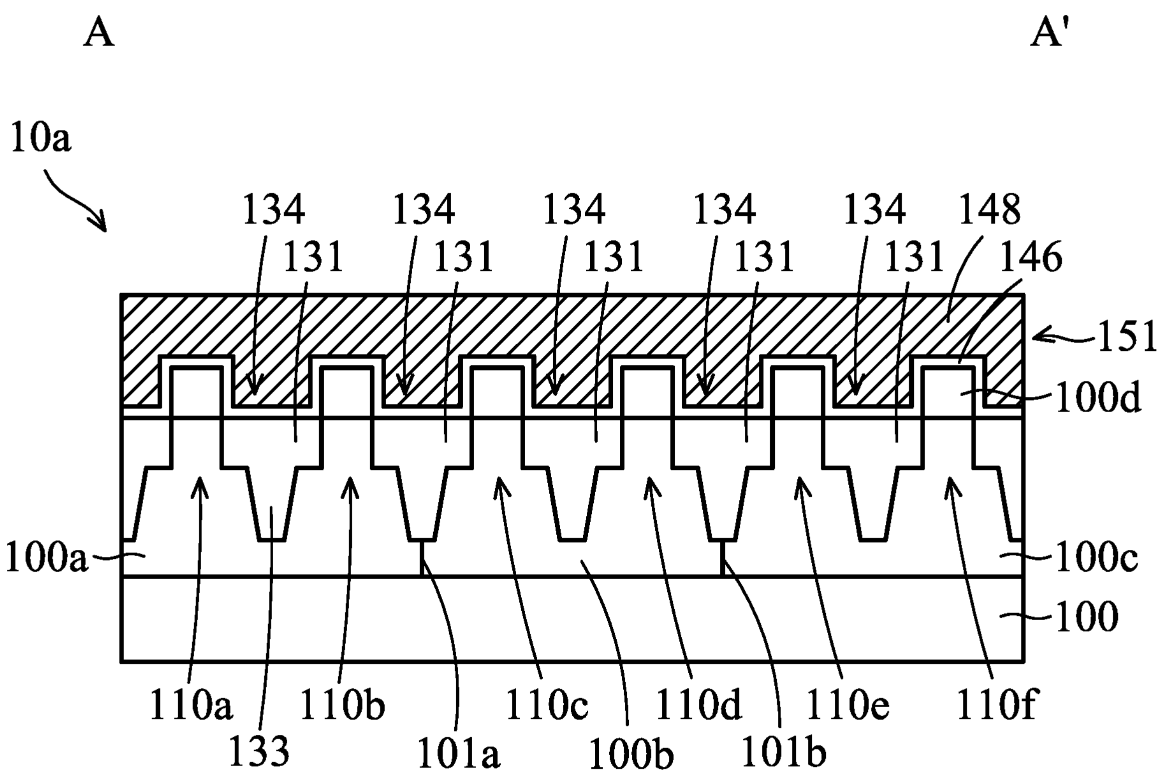

A
A'
110a
110b
110c
110d
110e
110f
134
131
133
135
135
100d
100a
100c
100
101a
100b
101b
W3
W1

FIG. 2H


A
A'
10a
134
134
134
134
134
148
131
131
131
131
131
146
151
100d
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100c
100
110a
110b
110c
110d
110e
110f
133
101a
100b
101b

FIG. 2I

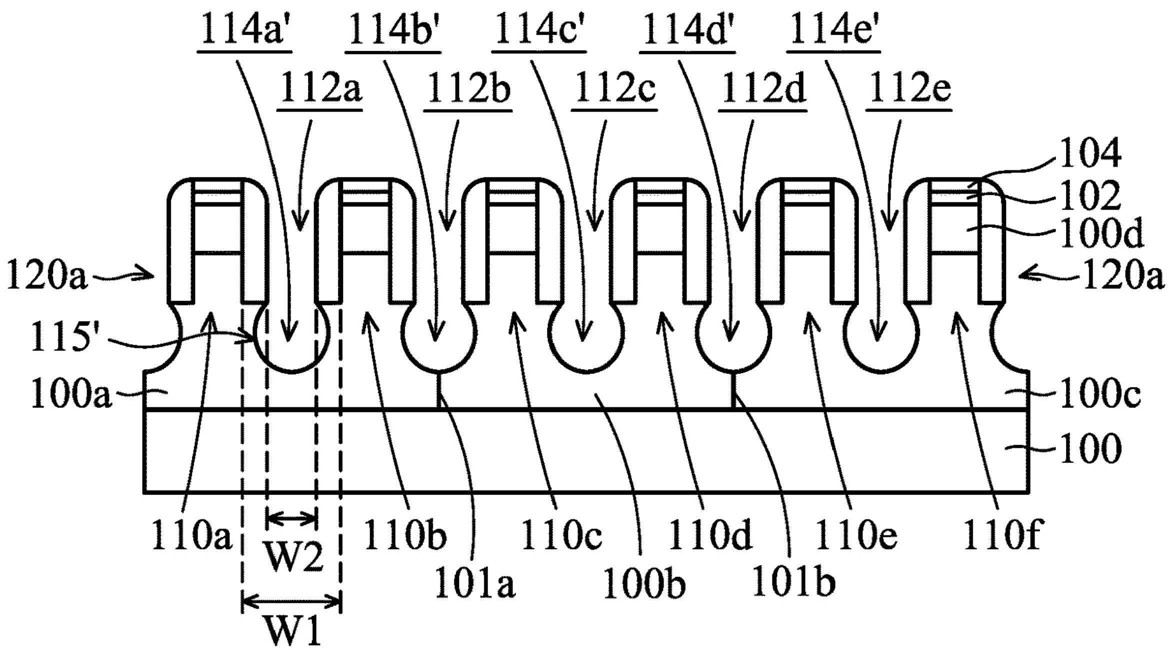
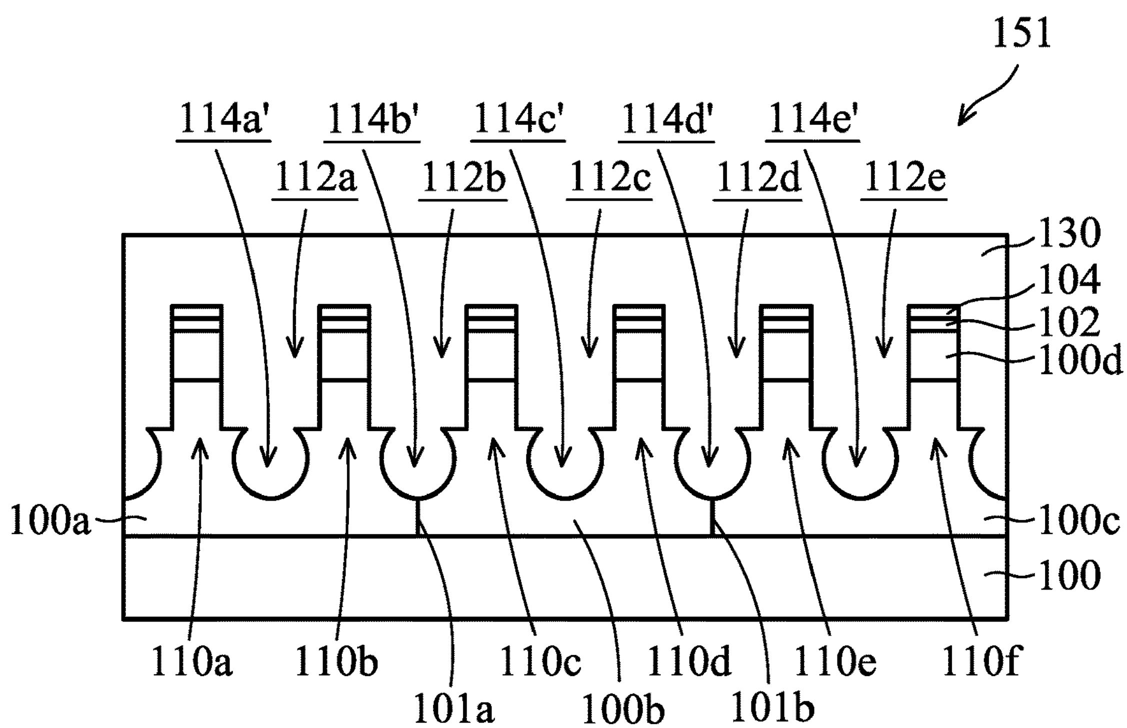

114a'
114b'
114c'
114d'
114e'
112a
112b
112c
112d
112e
104
102
100d
120a
120a
115'
100a
100c
100
110a
W2
110b
110c
110d
110e
110f
101a
100b
101b
W1

FIG. 3A


151
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114c'
114d'
114e'
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112b
112c
112d
112e
130
104
102
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110b
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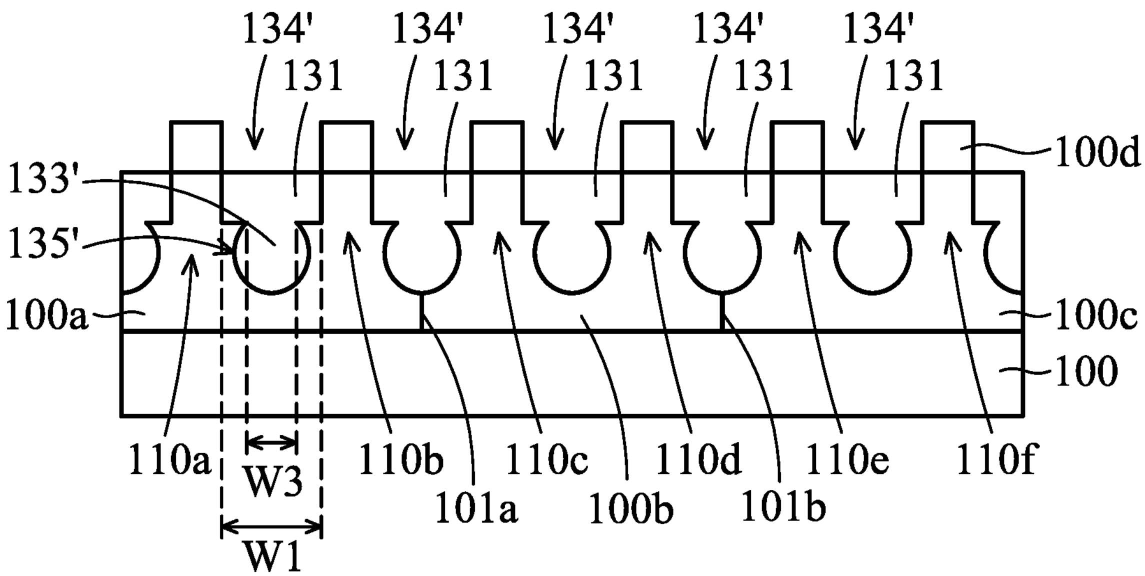
110f
101a
100b
101b

FIG. 3B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133'
135'
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100c
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W3
W1
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110c
110d
110e
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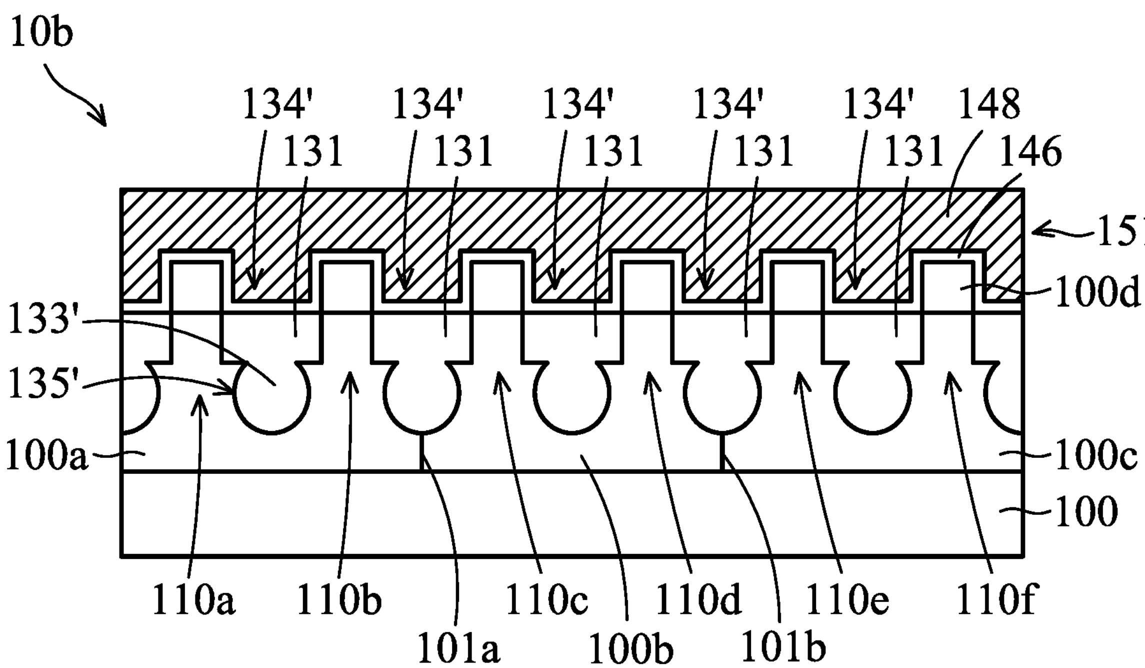
100b
101b

FIG. 3C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148
146
151
100d
133'
135'
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100c
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110c
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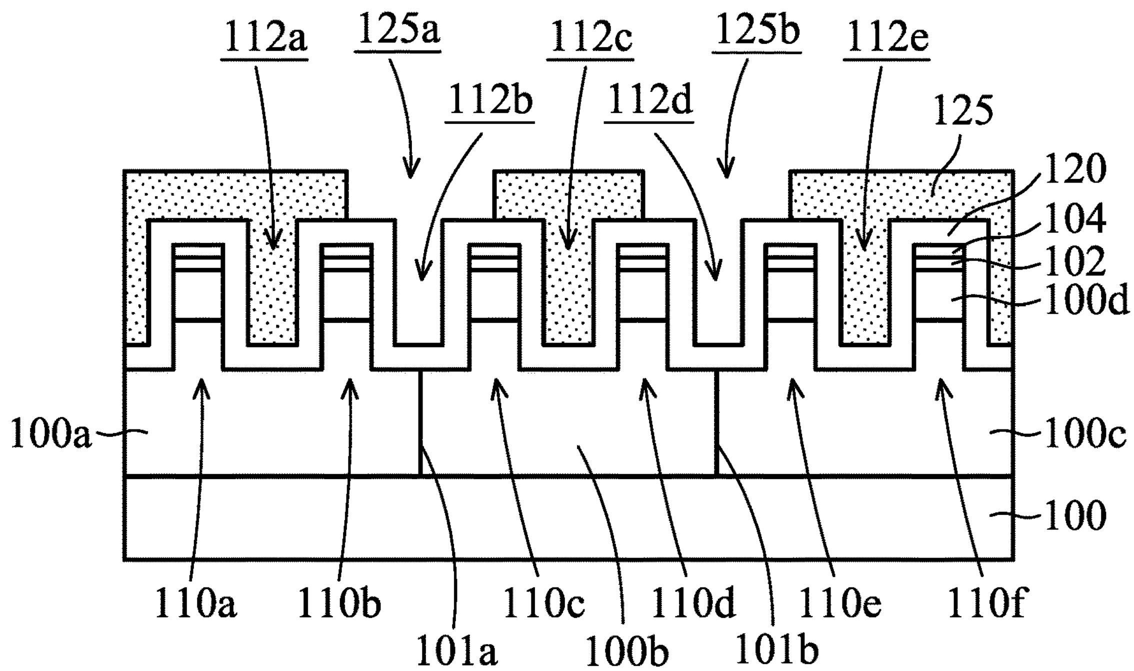
110e
110f
101a
100b
101b

FIG. 3D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125a
112c
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112b
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125
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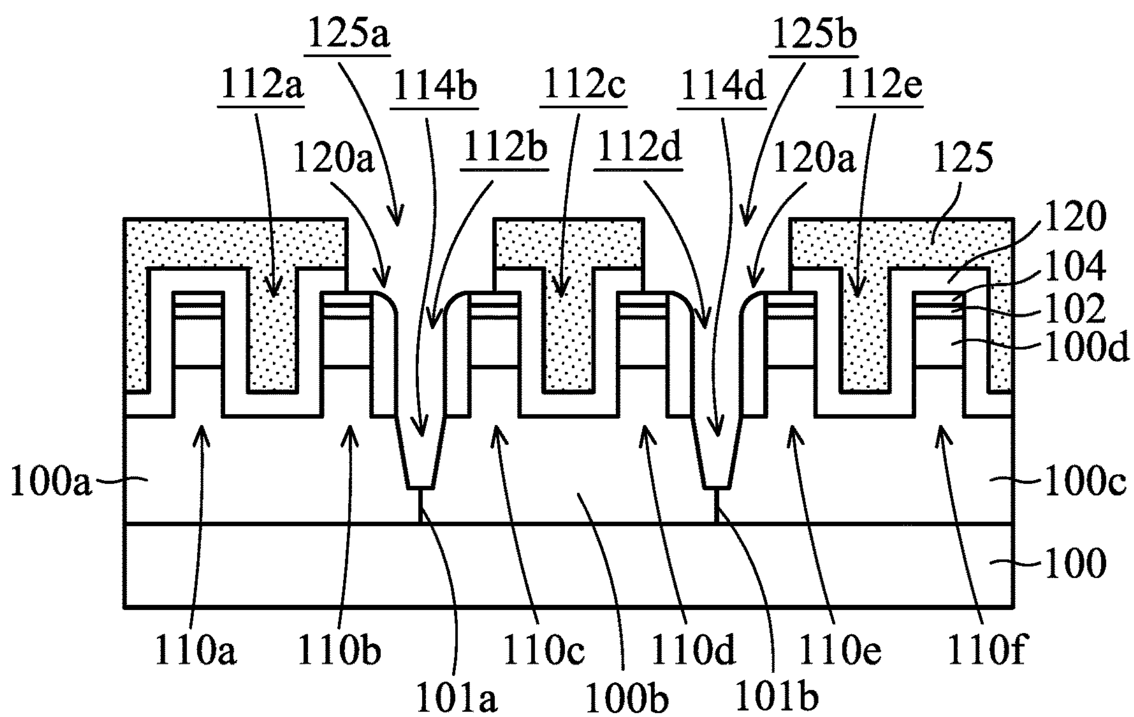
110d
110e
110f
101a
100b
101b

FIG. 4A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125
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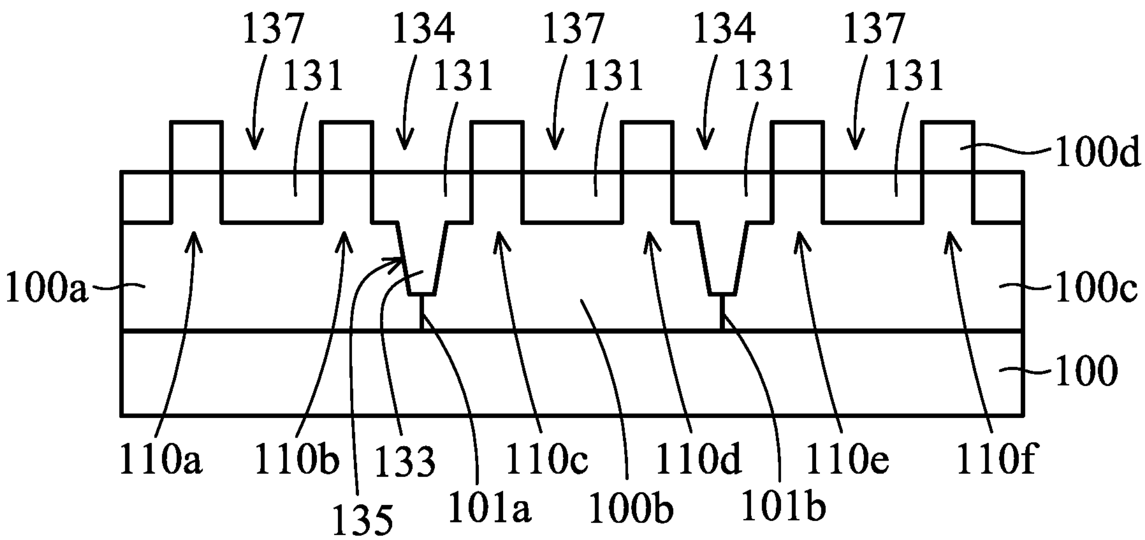
FIG. 4B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110b
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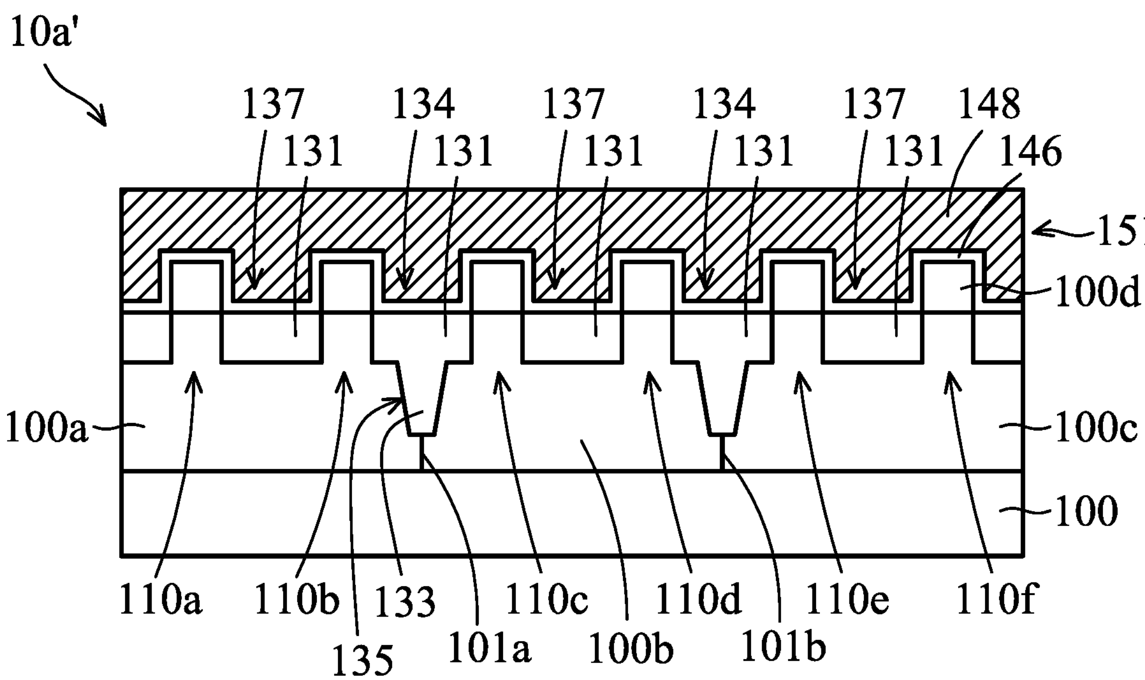
110d
110e
110f
135
101a
100b
101b

FIG. 4C


10a'
137
134
137
134
137
148
131
131
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131
131
146
151
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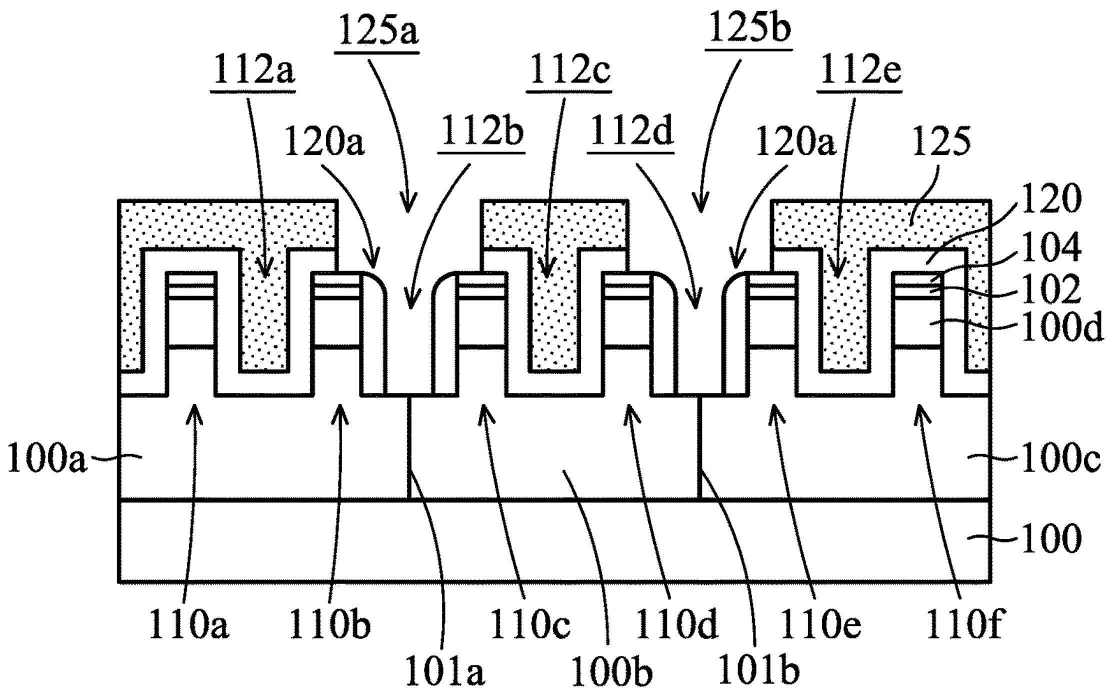
135
101a
100b
101b

FIG. 4D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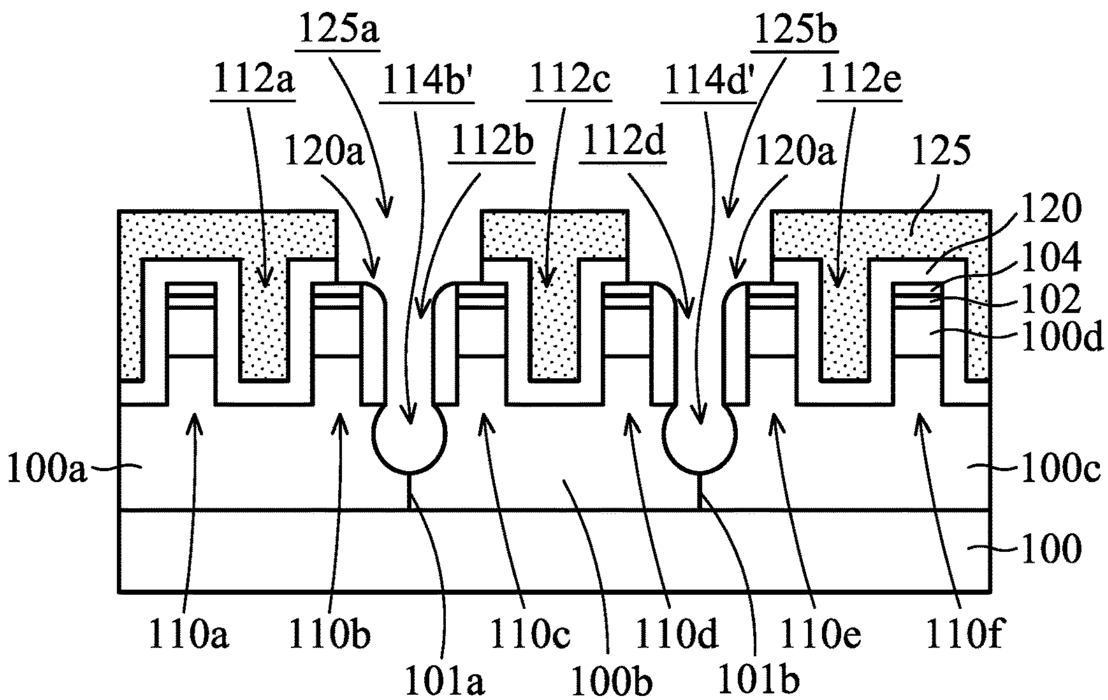
100b
101b

FIG. 5A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125
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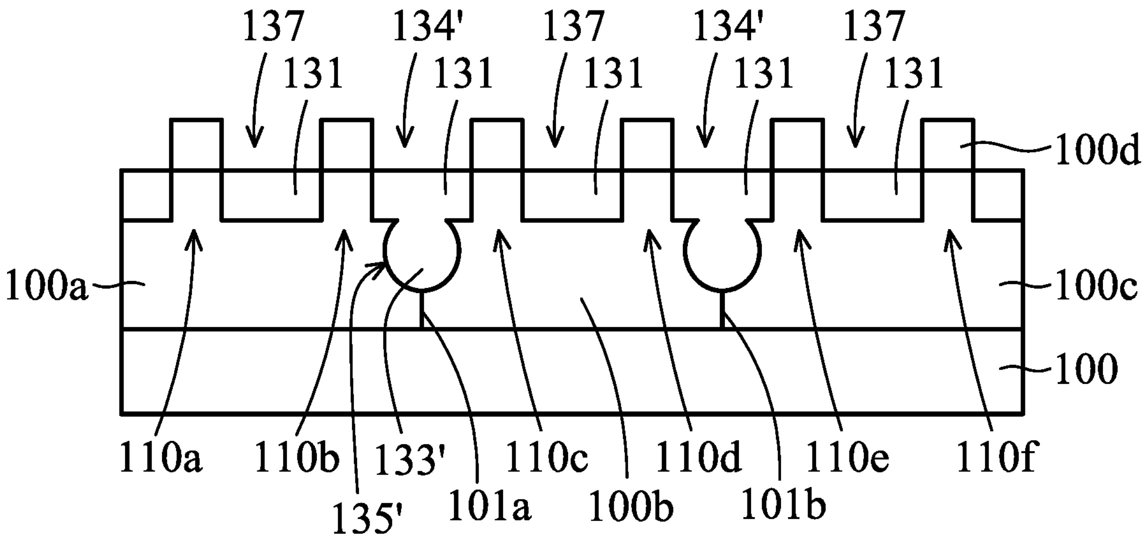
110e
110f
101a
100b
101b

FIG. 5B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134'
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134'
137
131
131
131
131
131
100d
100a
100c
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110a
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133'
110c
110d
110e
110f
135'
101a
100b
101b

FIG. 5C

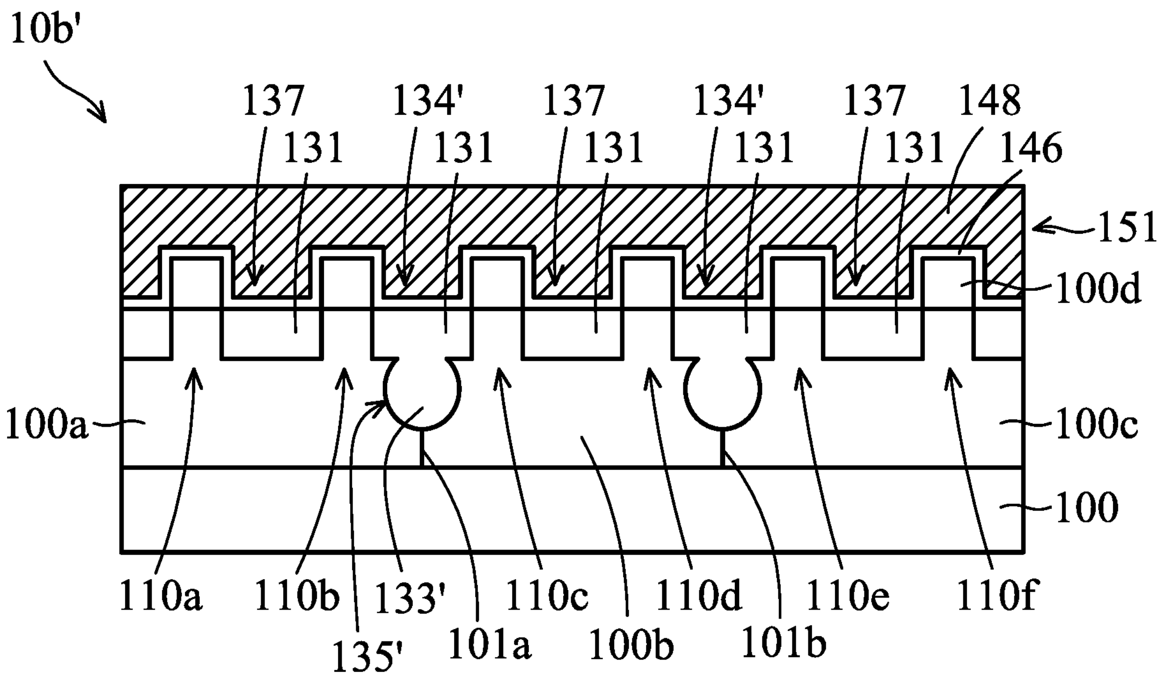
10b'
137
134'
137
134'
137
148
131
131
131
131
131
146
151
100d
100a
100c
100
110a
110b
133'
110c
110d
110e
110f
135'
101a
100b
101b

FIG. 5D

ISOLATION WITH MULTI-STEP STRUCTURE

PRIORITY CLAIM AND CROSS-REFERENCE

This Application is a Continuation of pending U.S. patent application Ser. No. 17/583,707, filed Jan. 25, 2022, which a Continuation of pending U.S. patent application Ser. No. 17/018,397, filed Sep. 11, 2020, which is Divisional of pending U.S. patent application Ser. No. 16/211,949, filed Dec. 6, 2018, which claims the benefit of U.S. Provisional Application No. 62/738,305, filed on Sep. 28, 2018, the entirety of which is incorporated by reference herein.

BACKGROUND

The semiconductor integrated circuit (IC) industry has experienced rapid growth. Technological advances in IC materials and design have produced generations of ICs where each generation has smaller and more complex circuits than the previous generation.

As the semiconductor industry has progressed into nanometer technology process nodes in pursuit of higher device density, higher performance, and lower costs, challenges from both fabrication and design issues have resulted in the development of three-dimensional designs, such as the fin field effect transistor (FinFET). FinFETs are fabricated with a thin vertical "fin" (or fin structure) extending from a substrate. The advantages of a FinFET include a reduction of the short-channel effect and a higher current flow.

Although existing FinFET manufacturing processes have generally been adequate for their intended purposes, they have not been entirely satisfactory in all respects, especially as device scaling-down continues. For example, well leakage (which can cause latch-up) becomes increasingly important as the fin structure and the shallow trench isolation (STI) are shrunk. It is a challenge to form reliable FinFET device at smaller and smaller sizes.

BRIEF DESCRIPTION OF THE DRAWINGS

Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It should be noted that, in accordance with standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIGS. **1**A to **1**I illustrate perspective views of various stages of manufacturing a semiconductor device structure in accordance with some embodiments.

FIGS. **2**A to **2**I illustrate cross-sectional representations of various stages of manufacturing a semiconductor device structure in accordance with some embodiments.

FIGS. **3**A to **3**D illustrate cross-sectional representations of various stages of manufacturing a semiconductor device structure in accordance with some embodiments.

FIGS. **4**A to **4**D illustrate cross-sectional representations of various stages of manufacturing a semiconductor device structure in accordance with some embodiments.

FIGS. **5**A to **5**D illustrate cross-sectional representations of various stages of manufacturing a semiconductor device structure in accordance with some embodiments.

DETAILED DESCRIPTION

The following disclosure provides many different embodiments, or examples, for implementing different features of the subject matter provided. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

Furthermore, spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly. It should be understood that additional operations can be provided before, during, and after the method, and some of the operations described can be replaced or eliminated for other embodiments of the method.

Embodiments for manufacturing semiconductor device structures are provided. The semiconductor device structures may include a semiconductor substrate having a first well region and a second well region that have different conductivity types and are adjacent to each other. A first fin structure and a second fin structure are respectively formed in the first well region and the second well region. The first fin structure and the second fin structure protrude from the semiconductor substrate and are adjacent to each other. Afterwards, a multi-step isolation structure is formed between the first fin structure and the second fin structure. The multi-step isolation structure includes a first isolation portion corresponding to the upper portions of the first fin structure and the second fin structure, and a second isolation portion extending from the bottom surface of the first isolation portion. The second isolation portion has a top width that is narrower than the bottom width of the first isolation portion, so that the fin structures on opposite sides of the multi-step isolation structure have a reverse T-like shape.

FIGS. **1**A to **1**I illustrate perspective views of various stages of manufacturing a semiconductor device structure **10***a* and FIGS. **2**A to **2**I illustrate cross-sectional representations of various stages of manufacturing the semiconductor device structure **10***a* in accordance with some embodiments. In addition, FIGS. **2**A to **2**I illustrate the cross-sectional representations of the semiconductor device structure shown along line A-A' in FIGS. **1**A to **1**I in accordance with some embodiments. In some embodiments, the semiconductor device structure is implemented as a fin field effect transistor (FinFET) structure. As shown in FIGS. **1**A and **2**A, a substrate **100** is provided. In some embodiments, the substrate **100** is a semiconductor substrate, such as a bulk semiconductor, a semiconductor-on-insulator (SOI) substrate, or the like, which may be doped (e.g. with a P-type or an N-type dopant) and/or undoped. In some embodiments, the substrate **100** is a wafer, such as a silicon wafer. Generally, an SOI substrate includes a layer of a semiconductor material formed on an insulator layer. The insulator layer may be, for example, a buried oxide (BOX) layer, a silicon oxide layer, or the like. The insulator layer is provided on a substrate, typically a silicon or glass substrate.

Other substrates, such as a multi-layered or gradient substrate may also be used. In some embodiments, the semiconductor material of the substrate **100** includes silicon; germanium; a compound semiconductor including silicon carbide, gallium arsenic, gallium phosphide, indium phosphide, indium arsenide, and/or indium antimonide; an alloy semiconductor including SiGe, GaAsP, AlInAs, AlGaAs, GaInAs, GaInP, and/or GaInAsP; or a combination thereof. In some embodiments, the substrate **100** includes silicon. In some embodiments, the substrate **100** includes an epitaxial layer. For example, the substrate **100** has an epitaxial layer overlying a bulk semiconductor.

In some embodiments, the substrate **100** includes a PMOS region for P-type FinFETs formed thereon. The PMOS region of the substrate **100** may include Si, SiGe, SiGeB, or an III-V group semiconductor material (such as InSb, GaSb, or InGaSb). In some embodiments, the substrate **100** includes an NMOS region for N-type FinFETs formed thereon. The NMOS region of the substrate **100** may include Si, SiP, SiC, SiPC, or an III-V group semiconductor material (such as InP, GaAs, AlAs, InAs, InAlAs, or InGaAs).

In some other embodiments, the substrate **100** includes one or more PMOS regions and one or more NMOS regions. For example, the substrate **100** may include well regions **100***a*-**100***c* adjacent to each other. The well region **100***b* may have a first conductivity type (e.g., N-type) and be formed between and adjacent to the well region **100***a* and the well region **100***c* that have a second conductivity type (e.g., P-type), so that a well interface **101***a* is formed between the well region **100***a* and the well region **100***b*, and a well interface **101***b* is formed between the well region **100***c* and the well region **100***b*. In those cases, the well region **100***b* serves as the NMOS region and the well region **100***b* serve as the PMOS region. In some other embodiments, the substrate **100** includes an undoped region **100***d* formed on the well regions **100***a*-**100***c*. The undoped region **100***d* may be used as channel regions for FinFETs formed on the substrate **100**.

Afterwards, a mask structure is formed over the substrate **100** in accordance with some embodiments. More specifically, a first masking layer **102** and a second masking layer **104** of the mask structure are successively stacked over the substrate **100** for the subsequent patterning process. In some embodiments, the first masking layer **102** may be used as an etch stop layer when the second masking layer **104** is patterned. The first masking layer **102** may also be used as an adhesion layer that is formed between the undoped region **100***d* of the substrate **100** and the second masking layer **104**.

In some embodiments, the first masking layer **102** is made of silicon oxide and is formed by a deposition process, such as a chemical vapor deposition (CVD) process, a low-pressure chemical vapor deposition (LPCVD) process, a plasma enhanced chemical vapor deposition (PECVD) process, a high-density plasma chemical vapor deposition (HDPCVD) process, a spin-on process, or another applicable process.

In some embodiments, the second masking layer **104** is made of silicon oxide, silicon nitride, silicon oxynitride, or another applicable material. In some other embodiments, more than one second masking layer **104** is formed over the first masking layer **102**. In some embodiments, the second masking layer **104** is formed by a deposition process, such as a chemical vapor deposition (CVD) process, a low-pressure chemical vapor deposition (LPCVD) process, a plasma enhanced chemical vapor deposition (PECVD) process, a high-density plasma chemical vapor deposition (HDPCVD) process, a spin-on process, or another applicable process.

After formation of the first masking layer **102** and the second masking layer **104** of the mask structure, a patterned photoresist layer **106** may be formed over the second masking layer **104** for subsequent definition of one or more fin structures in the substrate **100**. In some embodiments, the patterned photoresist layer **106** is formed by a photolithography process. The photolithography process may include photoresist coating (e.g., spin-on coating), soft baking, mask aligning, exposure, post-exposure baking, developing the photoresist, rinsing and drying (e.g., hard baking).

The first masking layer **102** and the second masking layer **104** of the mask structure are patterned by using the patterned photoresist layer **106** as an etch mask, as shown in FIGS. **1**B and **2**B in accordance with some embodiments. After the first masking layer **102** and the overlying second masking layer **104** are etched, a patterned first masking layer **102** and a patterned second masking layer **104** are formed, so that portions of the undoped region **100***d* of the substrate **100** are exposed.

After the portions of the undoped region **100***d* of the substrate **100** are exposed by forming the patterned first masking layer **102** and the patterned second masking layer **104**, the patterned photoresist layer **106** is removed, in accordance with some embodiments. Afterwards, the substrate **100** is patterned by one or more etching processes using the patterned first masking layer **102** and the patterned second masking layer **104** as an etch mask, as shown in FIGS. **1**C and **2**C in accordance with some embodiments.

More specifically, the exposed portions of the undoped region **100***d* of the substrate **100** are removed, and the well regions **100***a*-**100***c* below the exposed portions of the undoped region **100***d* of the substrate **100** are partially removed by an etching process using the patterned second masking layer **104** and the patterned first masking layer **102** as an etch mask. As a result, fin structures and trenches in the substrate **100** are formed. In order to simplify the diagram, fin structures **110***a*-**110***f* protruding from the substrate **100** and trenches **112***a*-**112***e* are depicted as an example. In some embodiments, each of the fin structures **110***a*-**110***f* has a width that gradually increases from the top portion to the bottom portion, so that each of the fin structures **110***a*-**110***f* has a tapered fin width and sidewall. In some embodiments, each of the trenches **112***a*-**112***e* has substantially the same width (e.g., the width W1 shown in FIG. **2**C).

In some embodiments, the fin structure **110***a* and the fin structure **110***b* are defined in the well region **100***a* by forming the trench **112***a* in the well region **100***a* between the fin structure **110***a* and the fin structure **110***b*. The fin structure **110***c* and the fin structure **110***d* are defined in the well region **100***b* by forming the trench **112***c* in the well region **100***b* between the fin structure **110***c* and the fin structure **110***d*. The fin structure **110***e* and the fin structure **110***f* are defined in the well region **100***c* by forming the trench **112***e* in the well region **100***c* between the fin structure **110***e* and the fin structure **110***f*.

In addition, the trench **112***b* is formed between the fin structure **110***b* and the fin structure **110***c* and directly above the interface **110***a* between the well region **100***a* and the well region **100***b*, so that the interface **110***a* is exposed from the trench **112***b*. Similarly, the trench **112***d* is formed between the fin structure **110***d* and the fin structure **110***e* and directly above the interface **110**b between the well region **100**b and the well region **100**c, so that the interface **110**b is exposed from the trench **112**d.

In some embodiments, the etching process for formation of fin structures **110**a-**110**f is a dry etching process or a wet etching process. For example, the substrate **100** is etched by a dry etching process, such as a reactive ion etching (RIE), neutral beam etching (NBE), the like, or a combination thereof. The etching process may be a time-controlled process, and continue until the fin structures **110**a-**110**f are formed and reach a predetermined height. A person of ordinary skill in the art will readily understand other methods of forming the fin structures, which are contemplated within the scope of some embodiments.

After the fin structures **110**a-**110**f are formed, an insulating layer **120** is formed over the substrate **100** to conformally cover the sidewalls and the top surfaces of the fin structures **110**a-**100**f, and the bottom of the trenches **112**a-**112**e, as shown in FIGS. **1**D and **2**D in accordance with some embodiments. In some embodiments, the insulating layer **120** is made of silicon oxide, silicon nitride, silicon oxynitride, silicon carbide (SiC), fluorosilicate glass (FSG), a low-k dielectric material, or another suitable dielectric material. The insulating layer **120** may be deposited by a chemical vapor deposition (CVD) process, a flowable CVD (FCVD) process, a spin-on-glass process, or another applicable process.

Afterwards, an insulating layer **120** is formed over the substrate **100** to cover the fin structures **110**, as shown in FIG. **1**D in accordance with some embodiments. In some embodiments, the insulating layer **120** is made of silicon oxide, fluorosilicate glass (FSG), a low-k dielectric material, and/or another suitable dielectric material or another low-k dielectric material. The insulating layer **120** may be deposited by a chemical vapor deposition (CVD) process, a flowable CVD (FCVD) process, an atomic layer deposition (ALD) process, or another applicable process.

After the insulating layer **120** is formed, the insulating layer **120** is etched to form insulating spacers **120**a over the substrate **100**, as shown in FIGS. **1**E and **2**E in accordance with some embodiments. In some embodiments, the insulating layer **120** is anisotropic etched using, for example, a dry etching process, so as to remove the insulating layer **120** on the top surfaces of the fin structures **110**a-**110**f and the bottom of the trenches **112**a-**112**e. As a result, the insulating spacers **120**a are formed on opposite sidewalls of each of the trenches **112**a-**112**e, so that portions of the well regions **110**a-**110**c including the well interfaces **101**a and **101**b are exposed through the trenches **112**a-**112**e. In some embodiments, each of the trenches **112**a-**112**e having insulating spacers **120**a formed therein has substantially the same width (e.g., the width W2 shown in FIG. **2**E) that is less than the width W1 shown in FIG. **2**C.

After the insulating spacers **120**a are formed, trenches **114**a-**114**e are formed in the well regions **100**a-**100**c of the substrate **100** and respectively below the trenches **112**a-**112**e, as shown in FIGS. **1**F and **2**F in accordance with some embodiments. In some embodiments, the exposed portions of the well regions **110**a-**110**c below the trenches **112**a-**112**e are etched by an anisotropic etching process using the insulating spacers **120**a as an etch mask. For example, the well regions **110**a-**110**c of the substrate **100** are etched by a dry etching process, such as a reactive ion etching (RIE), neutral beam etching (NBE), the like, or a combination thereof.

After the anisotropic etching process, the trenches **114**a-**114**e with tilted sidewalls **115** are respectively extended from the bottom surface of the trenches **112**a-**112**e into the well regions of substrate **100**, so that each of the trenches **114**a-**114**e has a top width W3 that is substantially equal to the width W2 shown in FIG. **2**E and less than the width W1 shown in FIG. **2**C. As shown in FIGS. **1**F and **2**F, the trench **114**b is formed between the well region **100**a and the well region **110**b and directly above the interface **110**a in accordance with some embodiments, so that the interface **110**a is exposed from the trench **114**b. Similarly, the trench **114**d is formed between the well region **100**b and the well region **100**c and directly above the interface **110**b in accordance with some embodiments, so that the interface **110**b is exposed from the trench **114**d.

After the trenches **114**a-**114**e are formed, an insulating material **130** is formed over the substrate **100** to cover the patterned second masking layers **104** over fin structures **110**a-**110**f and fill the trenches **114**a-**114**e and the trenches **112**a-**112**e, as shown in FIGS. **1**G and **2**G in accordance with some embodiments. In some embodiments, the insulating material **130** is made of silicon oxide, fluorosilicate glass (FSG), a low-k dielectric material, and/or another suitable dielectric material or another low-k dielectric material. The insulating material **130** may be deposited by a chemical vapor deposition (CVD) process, a flowable CVD (FCVD) process, a spin-on-glass process, or another applicable process.

In some embodiments, the insulating spacers **120**a are removed from the opposite sidewalls of the trenches **112**a-**112**e prior to the formation of the insulating material **130**, as shown in FIGS. **1**G and **2**G. In some other embodiments, the insulating spacers **120**a are remained in the trenches **112**a-**112**e during the formation of the insulating material **130**. In those cases, the insulating spacer **120**a may be made of a material that is the same as or similar to the insulating material **130**.

Afterwards, the insulating material **130** is recessed to expose the top surface of the patterned second masking layer **104**, in accordance with some embodiments. For example, the insulating material **130** over the top surface of the patterned second masking layer **104** is etched back or removed by a chemical mechanical polishing (CMP) process. After the top surface of the patterned second masking layer **104** is exposed, the patterned second masking layer **104** and the patterned first masking layer **102** are removed by one or more etching processes, so as to expose the top surfaces of the fin structures **110**a-**110**f. For example, the patterned second masking layer **104** and the patterned first masking layer **102** are removed by a dry etching process, a wet etching process, or a combination thereof.

Afterwards, the insulating material **130** is further recessed to form an isolation feature over the substrate **100** and surrounding the fin structures **110**a-**110**f, as shown in FIGS. **1**H and **2**H in accordance with some embodiments. In some embodiments, the insulating material **130** is recessed by an etching process (such as a dry etching process or a wet etching process, or a combination thereof), so that the top surface of the isolation feature is substantially level with the interfaces between the undoped region **100**d and the well regions **100**a-**100**c.

In some embodiments, the isolation feature made of the remaining insulating material **130** includes multi-step isolation structures **134**. More specifically, each of the multi-step isolation structures **134** is formed between the corresponding two adjacent fin structures formed over the substrate **100**. The multi-step isolation structure **134** includes a first isolation portion **131** (which may also be referred to an upper isolation portion) and a second isolation portion **133** (which may also be referred to a lower isolation portion). The first isolation portion **131** is formed in the corresponding trench (such as the trenches **112**a-**112**f indicated in FIG. **2**F) to correspond to the upper portions of the fin structures **110**a-**110**f. The second isolation portion **133** is formed in the corresponding trench (such as the trenches **114**a-**114**f indicated in FIG. **2**F) to extend from the bottom surface of the first isolation portion **131** and to correspond to the lower portions of the fin structures **110**a-**110**f. As a result, the second isolation portion **133** between the fin structure **110**b and the fin structure **110**c is formed directly above the well interface **101**a. Also, the second isolation portion **133** between the fin structure **110**d and the fin structure **110**c is formed directly above the well interface **101**b.

In some embodiments, the second isolation portion **133** has tilted sidewalls **135** and a top width (which is substantially equal to the top width W3 of the trenches **114**a-**114**e shown in FIG. **2**F) that is narrower than the bottom width of the first isolation portion **131** (which is substantially equal to the width W1 shown in FIG. **2**C). Therefore, the first isolation portion **131** has a bottom area that is greater than the top area of the second isolation portion **133**. As a result, the multi-step isolation structures **134** have a T-like shape and each of the fin structures **110**a-**110**f has a reverse T-like shape corresponding to the T-like shape of the multi-step isolation structure **134**.

The isolation feature that includes multi-step isolation structures **134** prevents electrical interference or crosstalk. A portion of each of the fin structures **110**a-**110**f is embedded in and surrounded by the isolation feature. Compared to the use of a shallow trench isolation (STI) structure for prevention of electrical interference or crosstalk, the use of the multi-step isolation structure **134** can increase the isolation depth between the well regions (e.g., between the well region **100**a and the well region **100**b, or between the well region **100**b and the well region **100**c), thereby increasing the well leakage path. As a result, the latch-up phenomenon can be improved or prevented. Compared to the use of a deep trench isolation (DTI) structure for prevention of electrical interference or crosstalk, the use of the multi-step isolation structure **134** reduces the loss of the volume of the well regions **100**a-**100**c near the well interfaces **101**a and **101**b. As a result, it can prevent the resistance of the well regions **100**a-**100**c from being increased, and therefore the device's performance can be maintained or improved. In addition, the fin structures **110**a-**110**f with the reverse T-like shape provide good mechanical strength, and therefore the fin collapse can be prevented. As a result, the yield of the semiconductor device can be increased.

After the isolation feature including the multi-step isolation structures **134** are formed, source/drain features **140** are formed in the fin structures **110**a-**110**f, and a gate structure **151** is formed across the fin structures **110**a-**110**f, so as to form the semiconductor device structure **10**a, as shown in FIGS. **1**I and **2**I in accordance with some embodiments. In some embodiments, a dummy gate structure (not shown) is formed across the fin structures **110**a-**110**f and over the isolation feature including the multi-step isolation structures **134** before the formation of the source/drain features **140** and the gate structure **151**.

In some embodiments, the dummy gate structure includes a dummy gate dielectric layer and a dummy gate electrode layer formed over the dummy gate dielectric layer. The dummy gate dielectric layer and the dummy gate electrode layer may be made of silicon oxide and polysilicon, respectively. Afterwards, gate spacers **136** are formed on the opposite sidewalls of the dummy gate structure in accordance with some embodiments. The gate spacer **136** may be made of low-K dielectric materials, silicon nitride, silicon oxide, silicon oxynitride, silicon carbide, or another applicable dielectric material.

After formation of the gate spacers **136**, the source/drain features **140** are formed in the fin structures **110**a-**110**f laterally adjacent to and exposed from the dummy gate structure, in accordance with some embodiments. In some embodiments, the source/drain structures **140** are formed by recessing the portions of the fin structures **110**a-**110**f laterally adjacent to the dummy gate structure and growing semiconductor materials in the formed recesses in the fin structures **110**a-**110**f by performing epitaxial (epi) growth processes.

After the source/drain features **140** are formed, an insulating layer **142** is formed over the fin structures **110**a-**110**f and covers the isolation feature and the source/drain features **140**, as shown in FIG. **1**I in accordance with some embodiments. The insulating layer **142** may serve as an interlayer dielectric (ILD) layer and may be a single layer or include multiple dielectric layers with the same or different dielectric materials. For example, the insulating layer **142** may be a single layer made of silicon oxide, tetraethyl orthosilicate (TEOS), phosphosilicate glass (PSG), borosilicate glass (BSG), boron-doped phosphosilicate Glass (BPSG), fluorosilicate glass (FSG), undoped silicate glass (USG), or the like. The insulating layer **142** may be deposited using any suitable method, such as a chemical vapor deposition (CVD) process, a plasma enhanced CVD (PECVD) process, flowable CVD (FCVD) process, the like, or a combination thereof.

Afterwards, the dummy gate structure is removed and replaced by the gate structure **151**, as shown in FIGS. **1**I and **2**I in accordance with some embodiments. In some embodiments, the gate structure **151** includes a gate dielectric layer **146**, a gate electrode layer **148**, and the gate spacers **136**. The gate dielectric layer **146** may be made of metal oxides, metal nitrides, metal silicates, transition metal-oxides, transition metal-nitrides, transition metal-silicates, oxynitrides of metals, or other applicable dielectric materials. The gate electrode layer **148** may be made of a conductive material, such as aluminum, copper, tungsten, titanium, tantalum, or another applicable material. The gate structure may further include a work functional metal layer (not shown) between the gate dielectric layer **146** and the gate electrode layer **148**, so that the gate structure has the proper work function values. The work function metal layer may be made of TiN, TaN, Ru, Mo, Al, WN, $ZrSi_2$, $MoSi_2$, $TaSi_2$, $NiSi_2$, WN, or a combination thereof. Alternatively, the work function metal layer may be made of Ti, Ag, TaAl, TaAlC, TiAlN, TaC, TaCN, TaSiN, Mn, Zr, or a combination thereof.

Many variations and/or modifications can be made to embodiments of the disclosure. FIGS. **3**A to **3**D illustrate cross-sectional representations of various stages of manufacturing a semiconductor device structure **10**b in accordance with some embodiments. The semiconductor device structure **10**b shown in FIG. **3**D is similar to the semiconductor device structure **10**a shown in FIG. **2**I. In some embodiments, the materials, formation methods, and/or benefits of the semiconductor device structure **10**a shown in FIGS. **2**A to **2**I may also be applied in the embodiments illustrated in FIGS. **3**A to **3**D, and therefore may not be repeated.

In some embodiments, a structure as shown in FIG. **2**E is provided. Afterwards, the exposed portions of the well regions **110**a-**110**c below the trenches **112**a-**112**e are etched using the insulating spacers **120**a as an etch mask. Unlike the anisotropic etching process shown in FIG. **2**F, the well regions **110**a-**110**c of the substrate **100** are etched by an isotropic etching process, such as a wet etching process. After the isotropic etching process, each of the trenches **114**a'-**114**e' has convex sidewalls **115'**. Similar to the trenches **114**a-**114**e shown in FIG. **2**F, each of the trenches **114**a'-**114**e' has a top width W**3** that is substantially equal to the width W**2** shown in FIG. **2**E and less than the width W**1** shown in FIG. **2**C.

After the trenches **114**a'-**114**e' are formed, an insulating material **130** is formed over the substrate **100** by a method that is the same as or similar to that shown in FIG. **2**G, so as to cover the patterned second masking layers **104** over fin structures **110**a-**110**f and fill the trenches **114**a'-**114**e' and the trenches **112**a-**112**e, as shown in FIG. **3**B in accordance with some embodiments. In some embodiments, the insulating spacers **120**a are removed from the opposite sidewalls of the trenches **112**a-**112**e prior to the formation of the insulating material **130**, as shown in FIG. **3**B. In some other embodiments, the insulating spacers **120**a are remained in the trenches **112**a'-**112**e' during the formation of the insulating material **130**.

Afterwards, the insulating material **130** is recessed by a method that is the same as or similar to that shown in FIG. **2**H, so as to form an isolation feature over the substrate **100** and surrounding the fin structures **110**a-**110**f, as shown in FIG. **3**C in accordance with some embodiments. In some embodiments, the isolation feature made of the remaining insulating material **130** includes multi-step isolation structures **134'**. Unlike the multi-step isolation structures **134** shown in FIG. **2**H, the multi-step isolation structure **134'** includes a first isolation portion **131** and a second isolation portion **133'** (which may also be referred to a lower isolation portion). The second isolation portion **133'** has convex sidewalls **135'** and a top width W**3** (which is substantially equal to the top width W**2** of the trenches **114**a'-**114**e' shown in FIG. **3**A) that is narrower than the bottom width of the first isolation portion **131** (which is substantially equal to the width W**1** shown in FIG. **3**A). Therefore, the first isolation portion **131** has a bottom area that is greater than the top area of the second isolation portion **133'**. As a result, the multi-step isolation structures **134'** have a T-like shape and each of the fin structures **110**a-**110**f has a reverse T-like shape corresponding to the T-like shape of the multi-step isolation structure **134'**.

Similar to the multi-step isolation structure **134** shown in FIG. **2**H, the multi-step isolation structure **134'** also can increase the well leakage path and reducing the loss of the volume of the well regions **100**a-**100**c near the well interfaces **101**a and **101**b. Moreover, the fin structures **110**a-**110**f with the reverse T-like shape provide good mechanical strength. In addition, the second isolation portion **133'** with convex sidewalls **135'** in the multi-step isolation structure **134'** can prevent the reduction of the well leakage path when the well junctions (i.e., the well interfaces **101**a and **101**b) shifts in the formation of the well regions **110**a-**110**c.

After the isolation feature including the multi-step isolation structures **134'** is formed, a gate structure **151** is formed across the fin structures **110**a-**110**f by a method that is the same as or similar to that shown in FIG. **2**I, so as to form the semiconductor device structure **10**b, as shown in FIG. **3**D in accordance with some embodiments.

Many variations and/or modifications can be made to embodiments of the disclosure. FIGS. **4**A to **4**D illustrate cross-sectional representations of various stages of manufacturing a semiconductor device structure **10**a' in accordance with some embodiments. The semiconductor device structure **10**a' shown in FIG. **4**D is similar to the semiconductor device structure **10**a shown in FIG. **2**I. In some embodiments, the materials, formation methods, and/or benefits of the semiconductor device structure **10**a shown in FIGS. **2**A to **2**I may also be applied in the embodiments illustrated in FIGS. **4**A to **4**D, and therefore may not be repeated.

In some embodiments, a structure as shown in FIG. **2**D is provided. Afterwards, such a structure is covered by a patterned photoresist layer **125**, as shown in FIG. **4**A in accordance with some embodiments. In some embodiments, the patterned photoresist layer **125** includes trench openings **125**a and **125**b to respectively expose the trench **112**b and the trench **112**d which are covered by the insulating layer **120** and located respectively and directly above the well interface **101**a and the well interface **101**b.

The insulating layer **120** exposed from the trench openings **125**a and **125**b is etched by a method that is the same as or similar to that shown in FIG. **2**E, so as to form insulating spacers **120**a on opposite sidewalls of the trench **112**b and the trench **112**d and expose portions of the well regions **110**a-**110**c including the well interfaces **101**a and **101**b under the trench **112**b and the trench **112**d, in accordance with some embodiments.

Afterwards, the exposed portions of the well regions **110**a-**110**c under the trench **112**b and the trench **112**d are etched by a method that is the same as or similar to that shown in FIG. **2**F, so as to respectively form the trench **114**b and the trench **114**d below the trench **112**b and the trench **112**d, as shown in FIG. **4**B.

In some embodiments, the patterned photoresist layer **125** is removed after trench **114**b and the trench **114**d are formed. Afterwards, an isolation feature is formed over the substrate **100**, as shown in FIG. **4**C in accordance with some embodiments. In some embodiments, the isolation feature includes isolation structures **137** and multi-step isolation structures **134**. More specifically, each of the isolation structures **137** includes a first isolation portion **131**, and each of the multi-step isolation structures **134** includes a first isolation portion **131** and a second isolation portion **133** that has tilted sidewalls **135**. In some embodiments, the isolation structures **137** are formed in the trench **112**a, the trench **112**c, and the trench **112**e. Moreover, the multi-step isolation structures **134** are formed in the trenches **112**b and **114**b and the trenches **112**d and **114**d. As a result, the isolation structures **137** have a bottom surface that is substantially level with the bottom surface of the first isolation portion **131** of the multi-step isolation structures **134**. The isolation structures **137** and the multi-step isolation structures **134** are formed by methods that are the same as or similar to those shown in FIGS. **2**G and **2**H, in accordance with some embodiments.

After the isolation feature including the isolation structures **137** and the multi-step isolation structures **134'** is formed, a gate structure **151** is formed across the fin structures **110**a-**110**f by a method that is the same as or similar to that shown in FIG. **2**I, so as to form the semiconductor device structure **10**a', as shown in FIG. **4**D in accordance with some embodiments.

Many variations and/or modifications can be made to embodiments of the disclosure. FIGS. **5**A to **5**D illustrate cross-sectional representations of various stages of manufacturing a semiconductor device structure **10**b' in accordance with some embodiments. The semiconductor device structure **10**b' shown in FIG. **5**D is similar to the semiconductor device structure **10**b shown in FIG. **3**D and the semiconductor device structure **10**a' shown in FIG. **4**D. In some embodiments, the materials, formation methods, and/

or benefits of the semiconductor device structure **10***b* shown in FIGS. **3**A to **3**D and the semiconductor device structure **10***a*' shown in FIGS. **4**A to **4**D may also be applied in the embodiments illustrated in FIGS. **5**A to **5**D, and therefore may not be repeated.

In some embodiments, a structure as shown in FIG. **4**A is provided. Afterwards, the insulating layer **120** exposed from the trench openings **125***a* and **125***b* are etched by a method that is the same as or similar to that shown in FIG. **4**B, so as to form insulating spacers **120***a* on opposite sidewalls of the trench **112***b* and the trench **112***d* and expose portions of the well regions **110***a*-**110***c* including the well interfaces **101***a* and **101***b* under the trench **112***b* and the trench **112***d*, as shown in FIG. **5**A in accordance with some embodiments.

After the insulating spacers **120***a* are formed, the exposed portions of the well regions **110***a*-**110***c* under the trench **112***b* and the trench **112***d* are etched by a method that is the same as or similar to that shown in FIG. **3**A, so as to respectively form the trench **114***b*' and the trench **114***d*' below the trench **112***b* and the trench **112***d*, as shown in FIG. **5**B.

In some embodiments, the patterned photoresist layer **125** is removed after trench **114***b*' and the trench **114***d*' are formed. Afterwards, an isolation feature is formed over the substrate **100**, as shown in FIG. **5**C in accordance with some embodiments. In some embodiments, the isolation feature includes isolation structures **137** and multi-step isolation structures **134**'. In some embodiments, similar to the semiconductor device structure **10***a*' shown in FIG. **4**D, each of the isolation structures **137** includes a first isolation portion **131**, and the isolation structures **137** are formed in the trench **112***a*, the trench **112***c*, and the trench **112***e*. In some embodiments, similar to the semiconductor device structure **10***b* shown in FIG. **3**D, each of the multi-step isolation structures **134**' includes a first isolation portion **131** and a second isolation portion **133**' that has convex sidewalls **135**', and the multi-step isolation structures **134** are formed in the trenches **112***b* and **114***b* and the trenches **112***d* and **114***d*. As a result, the isolation structures **137** have a bottom surface that is substantially level with the bottom surface of the first isolation portion **131** of the multi-step isolation structures **134**'. The isolation structures **137** and the multi-step isolation structures **134**' are formed by methods that are the same as or similar to those shown in FIGS. **3**B and **3**C, in accordance with some embodiments.

After the isolation feature including the isolation structures **137** and the multi-step isolation structures **134**' is formed, a gate structure **151** is formed across the fin structures **110***a*-**110***f* by a method that is the same as or similar to that shown in FIG. **3**D, so as to form the semiconductor device structure **10***a*', as shown in FIG. **5**D in accordance with some embodiments.

Embodiments of semiconductor device structures and methods for forming the same are provided. The formation of the semiconductor device structure includes forming a first fin structure over a semiconductor substrate and in a first well region of first conductivity type in the semiconductor substrate, and a second fin structure over the semiconductor substrate and in the second well region of an opposite second conductivity type in the semiconductor substrate. Afterwards, a multi-step isolation structure is formed between the first fin structure and the second fin structure. The multi-step isolation structure includes a first isolation portion and a second isolation portion extending from a bottom surface of the first isolation portion. The second isolation portion has a top width that is narrower than the bottom width of the first isolation portion. In the multi-step isolation structure, since the isolation depth increases between the adjacent well regions, leakage (which may cause latch-up) between the adjacent well regions can be reduced. Since the lower portion (i.e., the second isolation portion) of the multi-step isolation structure has a top width that is narrower than the bottom width of the upper portion (i.e., the first isolation portion) of the multi-step isolation structure first isolation feature, the fins can have a reverse T-like shape. As a result, the mechanical strength of the fin structures can be increased, thereby preventing fin collapse, and therefore the yield of the semiconductor device can be improved. In addition, compared to one-step deep trench isolation technology for latch-up prevention, the loss of the well volume can be mitigated by the use of the multi-step isolation structure. As a result, it can prevent the resistance of the well region from being increased, and therefore the device's performance can be maintained or improved.

In some embodiments, a semiconductor device structure is provided. The semiconductor device structure includes a first fin structure and an adjacent second fin structure protruding from the semiconductor substrate. The semiconductor device structure includes an isolation structure formed in the semiconductor substrate and in direct contact with the first fin structure and the second fin structure. The first fin structure and the second fin structure each includes: a first portion protruding above a top surface of the isolation structure; a second portion in direct contact with a bottom surface of the first portion, so that an interface is formed between the first portion and the second portion; and a third portion extending from a bottom of the second portion. The top width of the third portion is different than the bottom width of the third portion and the bottom width of the second portion.

In some embodiments, a semiconductor device structure is provided. The semiconductor device structure includes fin structures protruding from a semiconductor substrate. The semiconductor device structure also includes isolation structures formed in the semiconductor substrate and alternately arranged with the plurality of fin structures. Each of the fin structures has an upper region and a lower region with different doping concentrations and the upper region protrudes above a top surface of the isolation structures. The bottom of each of the fin structures is substantially level with the bottom of each of the isolation structures. The bottom width of each of the fin structures is greater than the bottom width of each of the isolation structures.

In some embodiments, a semiconductor device structure is provided. The semiconductor device structure includes a semiconductor substrate having a lower region and a plurality of upper regions extending from the lower region and having a doping concentration different from that of the lower region. The semiconductor device structure also includes first isolation structures formed in a semiconductor substrate and exposed from the upper regions. The semiconductor device structure further includes second isolation structures formed in the semiconductor substrate, alternately arranged with the first isolation structures, and exposed from the upper regions. Each of the first isolation structures has a vertical thickness greater than that of each of the second isolation structures and includes a first isolation portion having a bottom that is substantially level with the bottom of each of the second isolation structures, and a second isolation portion extending from the bottom of the first isolation portion. The second isolation portion has a top width that is different than the bottom width of the second isolation portion and the bottom width of the first isolation portion.

In some embodiments, a semiconductor device structure is provided. The semiconductor device structure includes a semiconductor substrate including a first well region of a first conductivity type. The semiconductor device structure also includes a first fin structure and an adjacent second fin structure formed in and protruding from the first well region. The semiconductor device structure also includes a first isolation structure formed in the first well region between the first fin structure and the second fin structure. A first sidewall surface of the first fin structure faces to a second sidewall surface of the second fin structure. The first sidewall surface and the second sidewall surface each extend along at least two directions from a bottom of the first isolation structure to a top of the first isolation structure.

In some embodiments, a semiconductor device structure is provided. The semiconductor device structure includes a first fin structure formed in a first well region of a semiconductor substrate and extending above a top of the first well region. The semiconductor device structure also includes a second fin structure formed in a second well region of a semiconductor substrate, extending above a top of the second well region, and in contact with the first fin structure. The first well region and second well region have different conductivity types. The semiconductor device structure further includes a first isolation structure formed in the first well region and the second region, including an upper portion having a first vertical sidewall surface in the first well region and a second vertical sidewall surface in the second well region, and a lower region extending from a bottom of the upper portion and having an outer surface with a curved contour. The first fin structure extending above the top of the first well region and the second fin structure extending above the top of the second well region are undoped regions. A distance between the undoped regions is greater than a top width of the lower portion of the first isolation structure.

In some embodiments, a semiconductor device structure is provided. The semiconductor device structure includes a semiconductor substrate having a first well region, a second well region, and a third well region between the first well region and the second well region. The semiconductor device structure also includes a first isolation structure formed in the first well region and the third well region, a second isolation structure formed in the second well region and the third well region, and a third isolation structure formed in the third well region between the first isolation structure and the second isolation structure. An outer surface contour of the third isolation structure is different than outer surface contours of the first isolation structure and the second isolation structure. A first fin structure and a second fin structure formed in the third well region, and protruding above and separated from each other by the third isolation structure.

The fins described above may be patterned by any suitable method. For example, the fins may be patterned using one or more photolithography processes, including double-patterning or multi-patterning processes. Generally, double-patterning or multi-patterning processes combine photolithography and self-aligned processes, allowing patterns to be created that have, for example, pitches smaller than what is otherwise obtainable using a single, direct photolithography process. For example, in one embodiment, a sacrificial layer is formed over a substrate and patterned using a photolithography process. Spacers are formed alongside the patterned sacrificial layer using a self-aligned process. The sacrificial layer is then removed, and the remaining spacers may then be used to pattern the fins.

The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A semiconductor device structure, comprising:

a semiconductor substrate comprising a first well region of a first conductivity type;

a first fin structure and an adjacent second fin structure formed in and protruding from the first well region, wherein a first sidewall surface of the first fin structure faces to a second sidewall surface of the second fin structure; and

a first isolation structure formed in the first well region between the first fin structure and the second fin structure;

wherein the first sidewall surface and the second sidewall surface each extend along at least two directions from a bottom of the first isolation structure to a top of the first isolation structure.

2. The semiconductor device structure as claimed in claim **1**, further comprising:

a second isolation structure separated from the first isolation structure by the first fin structure; and

a third isolation structure separated from the first isolation structure by the second fin structure.

3. The semiconductor device structure as claimed in claim **2**, wherein the first fin structure has a third sidewall surface opposite to the first sidewall surface and the second fin structure has a fourth sidewall surface opposite to the second sidewall surface, wherein the third sidewall surface extends along at least two directions from a bottom of the second isolation structure to a top of the second isolation, and wherein the fourth sidewall surface extends along at least two directions from a bottom of the third isolation structure to a top of the third isolation structure.

4. The semiconductor device structure as claimed in claim **2**, wherein the semiconductor further comprises a second well region of a second conductivity type different than the first conductivity type.

5. The semiconductor device structure as claimed in claim **4**, wherein the third isolation structure is formed in the second well region of the semiconductor substrate.

6. The semiconductor device structure as claimed in claim **5**, wherein a bottom of the third isolation structure is directly on a well interface between the first well region and the second well region.

7. The semiconductor device structure as claimed in claim **4**, further comprising:

a third fin structure formed in and protruding from the second well region, wherein a third sidewall surface of the third fin structure is in direct to the third isolation structure, wherein the third sidewall surface extends along at least two directions from a bottom of the third isolation structure to a top of the third isolation.

8. The semiconductor device structure as claimed in claim **1**, wherein the first fin structure and the second fin structure each comprise:

a first portion with a top surface that is substantially level with a top surface of the first isolation structure; and a second portion extending from a bottom of the first portion.

9. The semiconductor device structure as claimed in claim 8, wherein portions of the first sidewall surface and the second sidewall surface corresponding to the first portion are vertical sidewall surfaces and portions of the first sidewall surface and the second sidewall surface corresponding to the second portion are tilted sidewall surfaces.

10. The semiconductor device structure as claimed in claim 8, wherein the first fin structure and the second fin structure each further comprise a third portion formed over the first portion, and wherein the third portion is an undoped region.

11. The semiconductor device structure as claimed in claim 10, wherein a bottom width of the third portion is substantially equal to a bottom width of the first portion and less than a top width of the second portion.

12. The semiconductor device structure as claimed in claim 1, further comprising a gate structure over the first fin structure and the second fin structure, wherein the gate structure comprises:

a gate dielectric layer; and

a gate electrode layer formed over the gate dielectric layer.

13. A semiconductor device structure, comprising:

a first fin structure formed in a first well region of a semiconductor substrate and extending above a top of the first well region;

a second fin structure formed in a second well region of a semiconductor substrate, extending above a top of the second well region, and in contact with the first fin structure, wherein the first well region and second well region have different conductivity types; and

a first isolation structure formed in the first well region and the second well region, comprising:

an upper portion having a first vertical sidewall surface in the first well region and a second vertical sidewall surface in the second well region; and

a lower region extending from a bottom of the upper portion and having an outer surface with a curved contour;

wherein the first fin structure extending above the top of the first well region and the second fin structure extending above the top of the second well region are undoped regions, and wherein a distance between the undoped regions is greater than a top width of the lower region of the first isolation structure.

14. The semiconductor device structure as claimed in claim 13, further comprising:

a second isolation structure formed in the first well region and separated from the first isolation structure by the first fin structure; and

a third isolation structure formed in the second well region and separated from the first isolation structure by the second fin structure,

wherein the first isolation structure, the second isolation structure, and the third isolation structure have a same outer surface contour.

15. The semiconductor device structure as claimed in claim 13, wherein each of the first fin structure and the second fin structure comprises:

a first portion formed above the top of the first well region and the top of the first well region; and

a second portion extending from a bottom of the first portion,

wherein the second portion has a first width that is greater than a top width of the first portion and a second width that is substantially equal to the top width of the first portion.

16. The semiconductor device structure as claimed in claim 15, further comprising:

a gate dielectric layer lining the first portion of the first fin structure and the first portion of the second fin structure; and

a gate electrode layer over the gate dielectric layer.

17. A semiconductor device structure, comprising:

a semiconductor substrate having a first well region, a second well region, and a third well region between the first well region and the second well region;

a first isolation structure formed in the first well region and the third well region;

a second isolation structure formed in the second well region and the third well region;

a third isolation structure formed in the third well region between the first isolation structure and the second isolation structure, wherein an outer surface contour of the third isolation structure is different than outer surface contours of the first isolation structure and the second isolation structure; and

a first fin structure and a second fin structure formed in the third well region, and protruding above and separated from each other by the third isolation structure.

18. The semiconductor device structure as claimed in claim 17, wherein each of the first isolation structure and the second isolation structure comprises:

a first portion; and

a second portion extending from a bottom of the first portion,

wherein a top width of the second portion is less than a bottom width of the first portion, and wherein the bottom width of the first portion is substantially equal to a bottom width of the third isolation structure.

19. The semiconductor device structure as claimed in claim 17, wherein the first well region and the second well region have a first conductivity type and the third well region has a second conductivity type.

20. The semiconductor device structure as claimed in claim 17, further comprising:

a gate dielectric layer formed over the first fin structure; and

a gate electrode layer formed over the gate dielectric layer.

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