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SEMICONDUCTOR DEVICE

Abstract

A semiconductor device includes: a second intermediate concentration region of a first conductivity type formed in the surface layer of a drift region in an outer peripheral area; a second high concentration region of the same conductivity type, serving as a channel stop, located closer to the surface and with higher impurity concentration than the intermediate region; a channel stop contact region of opposite conductivity type formed within the intermediate region near the high concentration region; a channel stop electrode disposed on the surface and covering the contact region; and a connection electrode that electrically links the channel stop electrode to the contact region.

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATIONS [0001] The present application is a continuation application of PCT Application No. PCT/JP2023/034189, filed on Sep. 21, 2023, which corresponds to Japanese Patent Application No. 2022-178475 filed on Nov. 7, 2022, with the Japan Patent Office, and the entire disclosure of these applications are incorporated herein by reference.

TECHNICAL FIELD
[0002] The present disclosure relates to a semiconductor device.
BACKGROUND ART
[0003] United States Patent Application Publication No. 2017/0040423 discloses a semiconductor device that includes a semiconductor substrate, a plurality of trench structures, and a gate pad portion. The plurality of trench structures are formed in a front surface of the semiconductor substrate. The gate pad portion is disposed on the semiconductor substrate such as to cover the plurality of trench structures.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0004] FIG. **1** is a plan view showing a semiconductor device according to a preferred embodiment.
[0005] FIG. **2** is a plan view showing a layout of a first principal surface.
[0006] FIG. **3** is an enlarged plan view showing an active region and an outer peripheral region.
[0007] FIG. **4** is a cross-sectional view taken along line IV-IV shown in FIG. **3**.
[0008] FIG. **5** is a cross-sectional view taken along line V-V shown in FIG. **3**.
[0009] FIG. **6** is a cross-sectional view taken along line VI-VI shown in FIG. **3**.
[0010] FIG. **7** is an enlarged plan view showing the active region and a boundary region.
[0011] FIG. **8** is a cross-sectional view taken along line VIII-VIII shown in FIG. **7**.
[0012] FIG. **9** is a cross-sectional view taken along line IX-IX shown in FIG. **7**.
[0013] FIG. **10**A is a diagrammatic cross-sectional view showing a structure of an inner peripheral portion of the outer peripheral region.
[0014] FIG. **10**B is a diagrammatic cross-sectional view showing a structure of a portion further to an outer side than FIG. **10**A.
[0015] FIG. **10**C is an enlarged cross-sectional view showing a detailed structure of a region XC of FIG. **10**B.
[0016] FIG. **10**D is an enlarged cross-sectional view showing a detailed structure of a region XD of FIG. **10**B.
[0017] FIG. **10**E is an enlarged cross-sectional view showing a part of a semiconductor device according to a comparative example and is an enlarged cross-sectional view corresponding to FIG. **10**D.

[0018] FIG. **11** is an enlarged plan view showing a pad region.
[0019] FIG. **12** is an enlarged plan view showing a gate resistive structure shown in FIG. **11**.
[0020] FIG. **13** is an enlarged plan view showing an inner portion of a gate resistive structure shown in FIG. **12**.
[0021] FIG. **14** is an enlarged plan view showing one end portion of the gate resistive structure shown in FIG. **12**.
[0022] FIG. **15** is an enlarged plan view showing another end portion of the gate resistive structure shown in FIG. **12**.
[0023] FIG. **16** is a cross-sectional view taken along line XVI-XVI shown in FIG. **13**.
[0024] FIG. **17** is a cross-sectional view taken along line XVII-XVII shown in FIG. **13**.
[0025] FIG. **18** is a cross-sectional view taken along line XVIII-XVIII shown in FIG. **13**.
[0026] FIG. **19** is a cross-sectional view taken along line XIX-XIX shown in FIG. **13**.
[0027] FIG. **20** is a cross-sectional view taken along line XX-XX shown in FIG. **14**.
[0028] FIG. **21** is a cross-sectional view taken along line XXI-XXI shown in FIG. **15**.
[0029] FIG. **22** is a cross-sectional view taken along line XXII-XXII shown in FIG. **12**.
[0030] FIG. **23** is a plan view showing a layout of a resistive film, a gate electrode film, and a gate wiring film.
[0031] FIG. **24** is an electric circuit diagram showing the gate resistive structure, a gate terminal electrode, and a gate wiring electrode.
[0032] FIG. **25** is a graph showing simulation results of leak current Ices [A] with respect to collector-emitter voltage Vce [V] respectively for the semiconductor device according to the present preferred embodiment and a semiconductor device according to the comparative example.

DESCRIPTION OF EMBODIMENTS

[0033] Hereinafter, preferred embodiments shall be described in detail with reference to attached drawings. The attached drawings are schematic views and are not strictly illustrated, and scales and the like thereof do not always match. Also, identical reference signs are given to corresponding structures among the attached drawings and duplicate descriptions thereof shall be omitted or simplified. For the structures whose description have been omitted or simplified, the description given before the omission or simplification shall apply.
[0034] When the wording “substantially equal” is used in a description in which a comparison target is present, the wording includes a numerical value (shape) equal to a numerical value (shape) of the comparison target and also includes numerical errors (shape errors) in a range of ±10% on a basis of the numerical value (shape) of the comparison target. Although the wordings “first,” “second,” “third,” etc., are used with the preferred embodiments, these are symbols attached to names of respective structures in order to clarify the order of description and are not attached with an intention of restricting the names of the respective structures.
[0035] FIG. **1** is a plan view showing a semiconductor device **1**A according to a first preferred embodiment. FIG. **2** is a plan view showing a layout of a first principal surface **3**. FIG. **3** is an enlarged plan view showing an active region **6** and an outer peripheral region **9**. FIG. **4** is a cross-sectional view taken along line IV-IV shown in FIG. **3**. FIG. **5** is a cross-sectional view taken along line V-V shown in FIG. **3**.
[0036] FIG. **6** is a cross-sectional view taken along line VI-VI shown in FIG. **3**. FIG. **7** is an enlarged plan view showing the active region **6** and a boundary region **8**. FIG. **8** is a cross-sectional view taken along line VIII-VIII shown in FIG. **7**. FIG. **9** is a cross-sectional view taken along line IX-IX shown in FIG. **7**.
[0037] FIG. **10**A is a diagrammatic cross-sectional view showing a structure of an inner peripheral portion of the outer peripheral region. FIG. **10**B is a diagrammatic cross-sectional view showing a structure of a portion further to an outer side than FIG. **10**A. FIG. **10**C is an enlarged cross-sectional view showing a detailed structure of a region XC of FIG. **10**B. FIG. **10**D is an enlarged cross-sectional view showing a detailed structure of a region XD of FIG. **10**B.

[0038] The semiconductor device **1**A is an IGBT semiconductor device having an IGBT (insulated gate bipolar transistor). With reference to FIGS. **1** to **10**D, the semiconductor device **1**A includes a chip **2** having a hexahedral shape (specifically, a rectangular parallelepiped shape). The chip **2** may be referred to as a "semiconductor chip." In this embodiment, the chip **2** has a single layer structure constituted of a silicon single crystal substrate (semiconductor substrate).

[0039] The chip **2** has the first principal surface **3** on one side, a second principal surface **4** on another side, and first to fourth side surfaces **5**A to **5**D connecting the first principal surface **3** and the second principal surface **4**. The first principal surface **3** and the second principal surface **4** are each formed in a quadrangle shape in plan view as viewed in a normal direction Z thereto (hereinafter, simply referred to as "plan view"). The normal direction Z is also a thickness direction of the chip **2**.

[0040] The first side surface **5**A and the second side surface **5**B extend in a first direction X along the first principal surface **3** and face each other in a second direction Y intersecting the first direction X along the first principal surface **3**. Specifically, the second direction Y is orthogonal to the first direction X. The third side surface **5**C and the fourth side surface **5**D extend in the second direction Y and face each other in the first direction X.

[0041] The semiconductor device **1**A includes a plurality of the active regions **6** provided at an interval in the first principal surface **3**. The plurality of active regions **6** include a first active region **6**A and a second active region **6**B. The first active region **6**A is provided in a region at the first side surface **5**A side with respect to a straight line crossing a center of the first principal surface **3** in the first direction X. The second active region **6**B is provided in a region at the second side surface **5**B side with respect to the straight line crossing the center of the first principal surface **3** in the first direction X. In this embodiment, each of the active regions **6** is formed in a polygonal shape having four sides parallel to a peripheral edge of the chip **2** in plan view. A planar shape of each of the active regions **6** is arbitrary.

[0042] The semiconductor device **1**A includes a non-active region **7** provided in a region outside the plurality of active regions **6** on the first principal surface **3**. The non-active region **7** includes the boundary region **8** and the outer peripheral region **9**. The boundary region **8** is provided in a band shape extending in the first direction X in a region between the first active region **6**A and the second active region **6**B. In this embodiment, the boundary region **8** is positioned on the straight line crossing the center of the first principal surface **3** in the first direction X.

[0043] The boundary region **8** includes a pad region **10** having a comparatively large width in the second direction Y and a street region **11** having a width smaller than the width of the pad region **10** in the second direction Y. The pad region **10** may be referred to as a "first boundary region" or a "wide region." The street region **11** may be referred to as a "second boundary region," a "line region," or a "narrow region."

[0044] The pad region **10** is provided in a region at one side (the third side surface **5**C side) in the first direction X. In this embodiment, the pad region **10** is positioned on the straight line crossing the center of the first principal surface **3** in the first direction X in plan view and is provided in a quadrangular shape in a vicinity of a central portion of the third side surface **5**C. The street region **11** is provided in a region at another side (the fourth side surface **5**D side) in the first direction X with respect to the pad region **10**. In this embodiment, the street region **11** is led out in a band shape from the pad region **10** toward the fourth side surface **5**D side and is positioned on the straight line crossing the center of the first principal surface **3** in the first direction X.

[0045] The outer peripheral region **9** is provided in a peripheral edge portion of the chip **2** such as to surround the plurality of active regions **6** entirely. The outer peripheral region **9** is provided in an annular shape (in this embodiment, a quadrangular annular shape) extending along the peripheral edge (the first to fourth side surfaces **5**A to **5**D) of the chip **2**. The outer peripheral region **9** is connected to the pad region **10** at one side (the third side surface **5**C side) of the first principal surface **3** and is connected to the street region **11** at the other side (the fourth side surface **5**D side)

of the first principal surface **3**.
[0046] The semiconductor device **1**A includes a drift region **12** of an n-type (first conductivity type) that is formed in an interior of the chip **2**. The drift region **12** is formed in an entire region of the interior of the chip **2**. In this embodiment, the chip **2** is constituted of a semiconductor substrate of the n-type (semiconductor chip of the n-type), and the drift region **12** is formed using the n-type chip **2**.
[0047] The semiconductor device **1**A includes a buffer region **13** of the n-type formed in a surface layer portion of the second principal surface **4**. In this embodiment, the buffer region **13** is formed in a layer shape extending along the second principal surface **4** in an entire region of the second principal surface **4**. The buffer region **13** has a higher n-type impurity concentration than the drift region **12**. The presence or absence of the buffer region **13** is arbitrary, and an embodiment without the buffer region **13** may be adopted instead.
[0048] The semiconductor device **1**A includes a collector region **14** of a p-type (second conductivity type) formed in a surface layer portion of the second principal surface **4**. The collector region **14** is formed in a surface layer portion of the buffer region **13** at the second principal surface **4** side. In this embodiment, the collector region **14** is formed in a layer shape extending along the second principal surface **4** in the entire region of the second principal surface **4**. The collector region **14** is exposed from the second principal surface **4** and a part of the first to fourth side surfaces **5**A to **5**D.
[0049] The semiconductor device **1**A includes a plurality of trench separation structures **15** formed in the first principal surface **3** such as to demarcate the plurality of active regions **6**. A gate potential is applied to the plurality of trench separation structures **15**. The trench separation structures **15** may be referred to as “trench gate separating structures” or “trench gate connection structures.” The plurality of trench separation structures **15** include a first trench separation structure **15**A at the first active region **6**A side and a second trench separation structure **15**B at the second active region **6**B side.
[0050] The first trench separation structure **15**A surrounds the first active region **6**A and demarcates the first active region **6**A from the boundary region **8** and the outer peripheral region **9**. In this embodiment, the first trench separation structure **15**A is formed in a polygonal annular shape having four sides parallel to the peripheral edge of the chip **2** in plan view. The first trench separation structure **15**A has portions that are bent such as to demarcate the pad region **10** and the street region **11** of the boundary region **8** in plan view.
[0051] The second trench separation structure **15**B surrounds the second active region **6**B and demarcates the second active region **6**B from the boundary region **8** and the outer peripheral region **9**. In this embodiment, the second trench separation structure **15**B is formed in a polygonal annular shape having four sides parallel to the peripheral edge of the chip **2** in plan view. The second trench separation structure **15**B has portions that are bent such as to demarcate the pad region **10** and the street region **11** of the boundary region **8** in plan view.
[0052] Each trench separation structure **15** preferably has a width less than the width of the street region **11**. The width of the trench separation structure **15** is a width in a direction orthogonal to a direction in which the trench separation structure **15** extends. The width of the trench separation structure **15** may be not less than 0.1 μm and not more than 2.5 μm. The width of the trench separation structure **15** is preferably not less than 0.3 μm and not more than 1 μm. The width of the trench separation structure **15** is preferably not less than 0.4 μm and not more than 0.7 μm. The trench separation structure **15** may have a depth of not less than 1 μm and not more than 20 μm. The depth of the trench separation structure **15** is preferably not less than 4 μm and not more than 10 μm.
[0053] Hereinafter, the arrangement of a single trench separation structure **15** shall be described. The trench separation structure **15** includes a separation trench **16**, a separation insulation film **17**, and a separation embedded electrode **18**. The separation trench **16** is formed in the first principal

surface **3** and demarcates a wall surface of the trench separation structure **15**. The separation insulation film **17** covers a wall surface of the separation trench **16** in a film shape. The separation insulation film **17** may include at least one among a silicon oxide film, a silicon nitride film, and an aluminum oxide film.

[0054] The separation insulation film **17** preferably has a single layer structure constituted of a single insulating film. The separation insulation film **17** particularly preferably includes a silicon oxide film that is constituted of an oxide of the chip **2**. The separation embedded electrode **18** is embedded in the separation trench **16** with the separation insulation film **17** interposed therebetween. The separation embedded electrode **18** may contain a conductive polysilicon. The gate potential is applied to the separation embedded electrode **18**.

[0055] The semiconductor device **1**A includes an IGBT structure Tr (transistor structure) formed in each active region **6**. The IGBT structure Tr is not formed in the non-active region **7**. Since the arrangement (the arrangement of the IGBT structure Tr) at the second active region **6**B side is substantially the same as the arrangement (the arrangement of the IGBT structure Tr) at the first active region **6**A side, the arrangement at the first active region **6**A side is described below. In this embodiment, the arrangement at the second active region **6**B side is line-symmetric to the arrangement at the first active region **6**A side across the boundary region **8**. The description of the structure at the first active region **6**A side is applied to the description of the structure at the second active region **6**B side, which shall be omitted.

[0056] The semiconductor device **1**A includes a first intermediate concentration region **19** of the n-type as a carrier accumulation region formed in a surface layer portion of the first principal surface **3** in the first active region **6**A. The first intermediate concentration region **19** is formed in a surface layer portion of the drift region **12** at the first principal surface **3** side. The first intermediate concentration region **19** extends in a layer shape along the first principal surface **3** and is connected to an inner peripheral wall of the trench separation structure **15**. The first intermediate concentration region **19** is formed shallower than the trench separation structure **15** and has a bottom portion positioned further to the first principal surface **3** side than a bottom wall of the trench separation structure **15**. The bottom portion of the first intermediate concentration region **19** is preferably positioned further to the first principal surface **3** side than a depth range intermediate portion of the trench separation structure **15**. A thickness of the first intermediate concentration region **19** may be approximately 2 μm.

[0057] The first intermediate concentration region **19** has a higher n-type impurity concentration than the drift region **12**. The drift region **12** may be referred to as a “first drift region” and the first intermediate concentration region **19** may be referred to as a “second drift region.” The first intermediate concentration region **19** accumulates holes from the collector region **14** of the p-type to decrease an apparent resistivity of the drift region **12** and is formed to reduce conduction loss.

[0058] In this embodiment, the n-type impurity concentration of the drift region **12** varies such as to decrease gradually from a surface of the drift region **12** at the first principal surface **3** side toward a surface at the second principal surface **4** side. The n-type impurity concentration of the drift region **12** is preferably, for example, not less than 1.0×1013 cm.sup.−3 and not more than 1.0×10.sup.15 cm.sup.−3. The n-type impurity concentration of the first intermediate concentration region **19** is preferably, for example, not less than 1.0×10.sup.15 cm.sup.−3. The n-type impurity concentration of the first intermediate concentration region **19** may, for example, be not less than 1.0×10.sup.15 cm.sup.−3 and not more than 1.0×10.sup.17 cm.sup.−3.

[0059] The semiconductor device **1**A includes a channel region **20** of the p-type formed in the surface layer portion of the first principal surface **3** in the first active region **6**A. The channel region **20** may be referred to as a “body region” or a “base region.” The channel region **20** is formed in a surface layer portion of the first intermediate concentration region **19** at the first principal surface **3** side. The channel region **20** extends in a layer shape along the first principal surface **3** and is connected to the inner peripheral wall of the trench separation structure **15**. The channel region **20**

is formed shallower than the trench separation structure **15** and has a bottom portion positioned further to the first principal surface **3** side than the bottom wall of the trench separation structure **15**. The bottom portion of the channel region **20** is preferably positioned closer to the first principal surface **3** than the depth range intermediate portion of the trench separation structure **15**. A thickness of the channel region **20** may be approximately 1 μm.

[0060] The semiconductor device **1**A includes a plurality of first trench structures **21** formed in the first principal surface **3** in the first active region **6**A. The gate potential is applied to the plurality of first trench structures **21**. The first trench structures **21** may be referred to as "trench gate structures." The plurality of first trench structures **21** penetrate through the channel region **20** such as to reach the drift region **12**. The plurality of first trench structures **21** are aligned at intervals in the first direction X in plan view and are each formed in a band shape extending in the second direction Y. That is, the plurality of first trench structures **21** are aligned in a stripe shape extending in the second direction Y.

[0061] In regard to a length direction (the second direction Y), each of the first trench structures **21** has one end portion at the boundary region **8** side and another end portion at the outer peripheral region **9** side. The one end portions and the other end portions of the plurality of first trench structures **21** are mechanically and electrically connected to the trench separation structure **15**. That is, the plurality of first trench structures **21**, together with the trench separation structure **15**, constitute a single trench structure of ladder shape. A connection portion of a first trench structure **21** and the trench separation structure **15** may be considered to be a part of the trench separation structure **15** and/or a part of the first trench structure **21**.

[0062] Each of the intervals between the plurality of first trench structures **21** is preferably less than the width of the street region **11**. A width of each first trench structure **21** is preferably less than the width of the street region **11**. The width of the first trench structure **21** is a width in a direction orthogonal to the direction in which the first trench structure **21** extends. The width of the first trench structure **21** may be not less than 0.1 μm and not more than 2.5 μm. The width of the first trench structure **21** is preferably not less than 0.3 μm and not more than 1 μm.

[0063] The width of the first trench structure **21** is particularly preferably not less than 0.4 μm and not more than 0.7 μm. The width of the first trench structure **21** is preferably substantially equal to the width of the trench separation structure **15**. The first trench structure **21** may have a depth of not less than 1 μm and not more than 20 μm. The depth of the first trench structure **21** is preferably not less than 4 μm and not more than 10 μm. The depth of the first trench structure **21** is preferably substantially equal to the depth of the trench separation structure **15**.

[0064] Hereinafter, the arrangement of a single first trench structure **21** shall be described. The first trench structure **21** includes a first trench **22**, a first insulating film **23**, and a first embedded electrode **24**. The first trench **22** is formed in the first principal surface **3** and demarcates a wall surface of the first trench structure **21**. In this embodiment, the first trench **22** is in communication with the separation trench **16** at both end portions in the second direction Y. Specifically, a side wall of the first trench **22** is in communication with a side wall of the separation trench **16**, and a bottom wall of the first trench **22** is in communication with a bottom wall of the separation trench **16**.

[0065] The first insulating film **23** covers a wall surface of the first trench **22** in a film shape. The first insulating film **23** may include at least one among a silicon oxide film, a silicon nitride film, and an aluminum oxide film. The first insulating film **23** preferably has a single layer structure constituted of a single insulating film.

[0066] The first insulating film **23** particularly preferably includes a silicon oxide film that is constituted of the oxide of the chip **2**. In this embodiment, the first insulating film **23** is constituted of the same insulating film as the separation insulation film **17**. The first insulating film **23** is connected to the separation insulation film **17** at communicating portions of the separation trench **16** and the first trench **22**.

[0067] The first embedded electrode **24** is embedded in the first trench **22** with the first insulating film **23** interposed therebetween. The first embedded electrode **24** may contain a conductive polysilicon. The gate potential is applied to the first embedded electrode **24**. The first embedded electrode **24** is mechanically and electrically connected to the separation embedded electrode **18** at the communicating portions of the separation trench **16** and the first trench **22**.
[0068] The semiconductor device **1**A includes a plurality of second trench structures **25** each formed in a region between mutually adjacent ones of the plurality of first trench structures **21** in the first principal surface **3** of the first active region **6**A. The second trench structures **25** may be referred to as “emitter trench structures.” In plan view, each second trench structure **25** is formed at intervals in the first direction X from the plurality of first trench structures **21** and is formed in a quadrangular annular shape extending in the second direction Y.
[0069] A width of the second trench structure **25** is preferably less than the width of the street region **11**. The width of the second trench structure **25** is a width in a direction orthogonal to the direction in which the second trench structure **25** extends. The width of the second trench structure **25** may be not less than 0.1 μm and not more than 2.5 μm. The width of the second trench structure **25** is preferably not less than 0.3 μm and not more than 1 μm.
[0070] The width of the second trench structure **25** is particularly preferably not less than 0.4 μm and not more than 0.7 μm. The width of the second trench structure **25** is preferably substantially equal to the width of the first trench structure **21**. The second trench structure **25** may have a depth of not less than 1 μm and not more than 20 μm. The depth of the second trench structure **25** is preferably not less than 4 μm and not more than 10 μm. The depth of the second trench structure **25** is preferably substantially equal to the depth of the first trench structure **21**.
[0071] Hereinafter, the arrangement of a single second trench structure **25** shall be described. The second trench structure **25** includes a second trench **26**, a second insulating film **27**, and a second embedded electrode **28**. The second trench **26** is formed in the first principal surface **3** and demarcates a wall surface of the second trench structure **25**.
[0072] The second insulating film **27** covers a wall surface of the second trench **26** in a film shape. The second insulating film **27** may include at least one among a silicon oxide film, a silicon nitride film, and an aluminum oxide film. The second insulating film **27** preferably has a single layer structure constituted of a single insulating film. The second insulating film **27** particularly preferably includes a silicon oxide film that is constituted of the oxide of the chip **2**. In this embodiment, the second insulating film **27** is constituted of the same insulating film as the first insulating film **23**.
[0073] The second embedded electrode **28** is embedded in the second trench **26** with the second insulating film **27** interposed therebetween. The second embedded electrode **28** may contain a conductive polysilicon. An emitter potential is applied to the second embedded electrode **28**.
[0074] The semiconductor device **1**A includes a plurality of emitter regions **29** of the n-type formed in a surface layer portion of the channel region **20** in the first active region **6**A. The emitter regions **29** are an example of “first high concentration regions” in the present disclosure and may be referred to as the “first high concentration regions.” Each of the plurality of emitter regions (the first high concentration regions) **29** has a higher n-type impurity concentration than the first intermediate concentration region **19**. The plurality of emitter regions **29** are respectively formed on both sides of the plurality of first trench structures **21**. The n-type impurity concentration of the emitter regions **29** is preferably, for example, not less than 1.0×10.sup.19 cm.sup.−3 and not more than 1.0×10.sup.21 cm.sup.−3.
[0075] The plurality of emitter regions **29** are each formed in a band shape extending along the plurality of first trench structures **21** in plan view. As a matter of course, the plurality of emitter regions **29** may be formed at intervals along the plurality of first trench structures **21** in plan view. In this embodiment, the plurality of emitter regions **29** are each formed in a region between a first trench structure **21** and a second trench structure **25** such as to be connected to the first trench

structure **21** and the second trench structure **25**. The emitter regions **29** are preferably not formed in a region between the trench separation structure **15** and the outermost second trench structure **25**.
[0076] The semiconductor device **1**A includes a plurality of contact holes **30** formed in the first principal surface **3** such as to expose the emitter regions **29** in the first active region **6**A. The contact holes **30** are an example of “first contact holes” in the present disclosure. The plurality of contact holes **30** are respectively formed on both sides of the plurality of first trench structures **21** at intervals from the plurality of first trench structures **21**. Each of the plurality of contact holes **30** may be formed in a tapered shape in which an opening width narrows from an opening toward a bottom wall.
[0077] The plurality of contact holes **30** penetrate through the emitter regions **29** such as to reach the channel region **20**. The plurality of contact holes **30** may be separated to the first principal surface **3** side from bottom portions of the emitter regions **29** such as not to reach the channel region **20**. The plurality of contact holes **30** are each formed in a band shape extending along the plurality of first trench structures **21** in plan view. The plurality of contact holes **30** are preferably shorter than the plurality of first trench structures **21** in a length direction (the second direction Y). The plurality of contact holes **30** are particularly preferably shorter than the plurality of second trench structures **25**.
[0078] The semiconductor device **1**A includes a plurality of channel contact regions **31** of the p-type formed in regions different from the plurality of emitter regions **29** in the surface layer portion of the channel region **20** of the first active region **6**A. The plurality of channel contact regions **31** have a higher p-type impurity concentration than the channel region **20**. Each of the plurality of channel contact regions **31** is formed in a band shape extending along the corresponding contact hole **30** in plan view. Bottom portions of the plurality of channel contact regions **31** are each formed in a region between the bottom wall of the corresponding contact hole **30** and the bottom portion of the channel region **20**.
[0079] The p-type impurity concentration of the channel region **20** is preferably, for example, not less than 1.0×1016 cm.sup.−3 and not more than 1.0×10.sup.18 cm.sup.−3. The p-type impurity concentration of the channel contact regions **31** is preferably, for example, not less than 1.0×10.sup.18 cm.sup.−3 and not more than 1.0×10.sup.20 cm.sup.−3.
[0080] The semiconductor device **1**A includes a plurality of floating regions **32** of the p-type respectively formed in regions surrounded by the plurality of second trench structures **25** in the surface layer portion of the first principal surface **3** in the first active region **6**A. The plurality of floating regions **32** are formed in an electrically floating state. As a matter of course, the emitter potential may be applied to the plurality of floating regions **32**. The plurality of floating regions **32** preferably have a higher p-type impurity concentration than the channel region **20**.
[0081] Each floating region **32** extends in a layer shape along the first principal surface **3** and is connected to an inner peripheral wall of each second trench structure **25**. Each floating region **32** is preferably formed deeper than a depth range intermediate portion of the second trench structure **25**. In this embodiment, each floating region **32** is formed deeper than the second trench structure **25** and has a portion that covers a bottom wall of the second trench structure **25**.
[0082] As described above, the first active region **6**A includes, as the IGBT structure Tr, the channel region **20**, the plurality of first trench structures **21**, the plurality of second trench structures **25**, the plurality of emitter regions **29**, the plurality of contact holes **30**, the plurality of channel contact regions **31**, and the plurality of floating regions **32**. Also, as with the first active region **6**A, the second active region **6**B includes, as the IGBT structure Tr, the channel region **20**, the plurality of first trench structures **21**, the plurality of second trench structures **25**, the plurality of emitter regions **29**, the plurality of contact holes **30**, the plurality of channel contact regions **31**, and the plurality of floating regions **32**.
[0083] The semiconductor device **1**A includes a boundary well region **40** of the p-type formed in a surface layer portion of the first principal surface **3** in the boundary region **8**. In this embodiment,

the boundary well region **40** has a higher p-type impurity concentration than the channel region **20**. As a matter of course, the boundary well region **40** may have a lower p-type impurity concentration than the channel region **20**.

[0084] The boundary well region **40** is formed in a band shape extending along the boundary region **8** in the first direction X in plan view. That is, the boundary well region **40** is formed in a layer shape extending along the first principal surface **3** in a region sandwiched by the first trench separation structure **15**A and the second trench separation structure **15**B and is exposed from the first principal surface **3**. The boundary well region **40** is formed in a region sandwiched by the plurality of first trench structures **21** at the first active region **6**A side and the plurality of first trench structures **21** at the second active region **6**B side.

[0085] The boundary well region **40** includes a first boundary well region **40**A formed in the pad region **10** and a second boundary well region **40**B formed in the street region **11**. The first boundary well region **40**A has a comparatively large region width in the second direction Y. The first boundary well region **40**A is formed in a polygonal shape (in this embodiment, a quadrangular shape) in plan view. The first boundary well region **40**A is preferably formed in an entire region of the pad region **10**.

[0086] The second boundary well region **40**B has a region width smaller than the region width of the first boundary well region **40**A in the second direction Y and is led out in a band shape from the first boundary well region **40**A toward the street region **11**. In this embodiment, the second boundary well region **40**B is positioned on the straight line crossing the center of the first principal surface **3** in the first direction X. The second boundary well region **40**B extends in a band shape such as to be positioned in a region at one side (the third side surface **5**C side) and a region at the other side (the fourth side surface **5**D side) in the first direction X with respect to a straight line crossing the center of the first principal surface **3** in the second direction Y.

[0087] The boundary well region **40** is preferably formed deeper than the channel region **20**. The boundary well region **40** is particularly preferably formed deeper than the plurality of trench separation structures **15** (the plurality of first trench structures **21**). In this embodiment, the boundary well region **40** has a width larger than the width of the boundary region **8** in the second direction Y and is led out from the boundary region **8** into the plurality of active regions **6**.

[0088] The boundary well region **40** is connected to the plurality of trench separation structures **15** that are mutually adjacent in the second direction Y. The boundary well region **40** has a portion that covers the bottom walls of the plurality of trench separation structures **15**. The boundary well region **40** has a portion that covers the bottom walls of the plurality of first trench structures **21** across the plurality of trench separation structures **15**.

[0089] The boundary well region **40** covers the side walls of the trench separation structures **15** and the side walls of the plurality of trench structures in the plurality of active regions **6** and is connected to each channel region **20** in the surface layer portion of the first principal surface **3**. The depth of the boundary well region **40** may be not less than 1 μm and not more than 20 μm. The depth of the boundary well region **40** is preferably not less than 5 μm and not more than 10 μm.

[0090] The semiconductor device **1**A includes an outer peripheral well region **41** of the p-type formed in a surface layer portion of the first principal surface **3** in the outer peripheral region **9**. In this embodiment, the outer peripheral well region **41** has a higher p-type impurity concentration than the channel region **20**. As a matter of course, the outer peripheral well region **41** may have a lower p-type impurity concentration than the channel region **20**. The p-type impurity concentration of the outer peripheral well region **41** is preferably substantially equal to the p-type impurity concentration of the boundary well region **40**.

[0091] The outer peripheral well region **41** is formed in a layer shape extending along the first principal surface **3** and is exposed from the first principal surface **3**. The outer peripheral well region **41** is formed at an interval inward from the peripheral edge (the first to fourth side surfaces **5**A to **5**D) of the first principal surface **3**. The outer peripheral well region **41** is formed in a band

shape extending along the plurality of active regions **6** in plan view. In this embodiment, the outer peripheral well region **41** is formed in an annular shape (in this embodiment, a quadrangular annular shape) surrounding the plurality of active regions **6** entirely in plan view.

[0092] The outer peripheral well region **41** is preferably formed deeper than the channel region **20**. The outer peripheral well region **41** is particularly preferably formed deeper than the plurality of trench separation structures **15** (the plurality of first trench structures **21**). The outer peripheral well region **41** preferably has a depth substantially equal to the boundary well region **40**.

[0093] The outer peripheral well region **41** is connected to the plurality of trench separation structures **15**. The outer peripheral well region **41** has a portion that covers the bottom walls of the plurality of trench separation structures **15**. The outer peripheral well region **41** is led out from the outer peripheral region **9** into the plurality of active regions **6**. The outer peripheral well region **41** has a portion that covers the bottom walls of the plurality of first trench structures **21** across the plurality of trench separation structures **15**.

[0094] The outer peripheral well region **41** covers the side wall of the trench separation structure **15** and the side walls of the plurality of first trench structures **21** in each active region **6** and is connected to the channel region **20** in the surface layer portion of the first principal surface **3**. The outer peripheral well region **41** is connected to the boundary well region **40** at a connection portion of the boundary region **8** and the outer peripheral region **9**. That is, the outer peripheral well region **41**, together with the boundary well region **40**, demarcates the plurality of active regions **6**.

[0095] With reference to FIG. **10**A and FIG. **10**B, the semiconductor device **1**A includes at least one (in this embodiment, a plurality) of field regions **42** of the p-type formed in the surface layer portion of the first principal surface **3** in the outer peripheral region **9**. The number of the field regions **42** is arbitrary and may be not less than 1 and not more than 20 (typically not less than 3 and not more than 10).

[0096] The plurality of field regions **42** may have a higher p-type impurity concentration than the channel region **20**. The plurality of field regions **42** may have a higher p-type impurity concentration than the outer peripheral well region **41**. The plurality of field regions **42** may have a lower p-type impurity concentration than the outer peripheral well region **41**. The plurality of field regions **42** may have a p-type impurity concentration substantially equal to that of the outer peripheral well region **41**. The plurality of field regions **42** are formed in an electrically floating state.

[0097] The plurality of field regions **42** are formed in a region between the peripheral edge of the chip **2** and the outer peripheral well region **41** at intervals from the peripheral edge of chip **2** and the outer peripheral well region **41**. The plurality of field regions **42** are formed in band shapes extending along the outer peripheral well region **41** in plan view. In this embodiment, the plurality of field regions **42** are formed in annular shapes (quadrangular annular shapes) surrounding the outer peripheral well region **41** in plan view.

[0098] The plurality of field regions **42** are preferably formed to be deeper than the channel region **20**. The plurality of field regions **42** may be formed to be of a depth substantially equal to that of the outer peripheral well region **41**. The plurality of field regions **42** may be formed to be shallower than the outer peripheral well region **41**. The plurality of field regions **42** may be formed to be of a constant depth.

[0099] The intervals between the plurality of field regions **42** may gradually increase toward the peripheral edge side of the chip **2**. Each of the plurality of field regions **42** has a width smaller than the width of the outer peripheral well region **41**. The outermost field region **42** among the plurality of field regions **42** may be formed to be wider than the other field regions **42**.

[0100] With reference to FIG. **10**C, the semiconductor device **1**A includes at least one (in this embodiment, a plurality) of field contact regions **111** of the p-type formed in a surface layer portion of each field region **42** at the first principal surface **3** side. In this embodiment, two field contact regions **111** are formed per single field region **42**. In this embodiment, the field contact regions **111**

have the same p-type impurity concentration as the channel contact regions **31**. Such field contact regions **111** can be formed, for example, at the same time as the channel contact regions **31** in a step of forming the channel contact regions **31**.

[0101] With reference to FIG. **10**B and FIG. **10**D, the semiconductor device **1**A includes a second intermediate concentration region **121** of the n-type formed in the surface layer portion of the first principal surface **3** in the outer peripheral region **9** at intervals to the peripheral edge side of the chip **2** from the plurality of field regions **42**. The second intermediate concentration region **121** has a higher n-type impurity concentration than the drift region **12**. In this embodiment, the second intermediate concentration region **121** has the same n-type impurity concentration as the first intermediate concentration region **19** as the carrier accumulation region.

[0102] The second intermediate concentration region **121** is formed in a band shape extending along the peripheral edge of the chip **2** in plan view. In this embodiment, the second intermediate concentration region **121** is formed in an annular shape (quadrangular annular shape) surrounding the plurality of field regions **42** in plan view. The second intermediate concentration region **121** may be exposed from the first to fourth side surfaces **5**A to **5**D. The second intermediate concentration region **121** is formed in an electrically floating state.

[0103] In this embodiment, a depth position of a bottom surface of the second intermediate concentration region **121** is equal to a depth position of a bottom surface of the first intermediate concentration region **19**. Such a second intermediate concentration region **121** can be formed, for example, at the same time as the first intermediate concentration region **19** in a step of forming the first intermediate concentration region **19**.

[0104] The semiconductor device **1**A includes a second high concentration region **43** of the n-type formed as a channel stop region in a surface layer portion of the second intermediate concentration region **121** at the first principal surface **3** side. A surface of the second high concentration region **43** at the second principal surface **4** side is covered by the second intermediate concentration region **121**. In other words, the second high concentration region **43** is disposed in the surface layer portion of the first principal surface **3** at the first principal surface **3** side with respect to the second intermediate concentration region **121**.

[0105] The second high concentration region **43** has a higher n-type impurity concentration than the second intermediate concentration region **121**. In this embodiment, the second high concentration region **43** has the same n-type impurity concentration as the emitter region (the first high concentration region) **29**. Such a second high concentration region **43** can be formed, for example, at the same time as the emitter region **29** in a step of forming the emitter region **29**.

[0106] The second high concentration region **43** is formed in a band shape extending along the peripheral edge of the chip **2** in plan view. In this embodiment, the second high concentration region **43** is formed in an annular shape (quadrangular annular shape) surrounding the plurality of field regions **42** in plan view. The second high concentration region **43** may be exposed from the first to fourth side surfaces **5**A to **5**D.

[0107] In this embodiment, an inner peripheral edge portion of a bottom surface of the second intermediate concentration region **121** is covered by the second high concentration region **43**. An inner peripheral edge of the second intermediate concentration region **121** is positioned further to the field region **42** side than an inner peripheral edge of the second high concentration region **43**. The second high concentration region **43** is formed in an electrically floating state.

[0108] With reference to FIG. **10**D, the semiconductor device **1**A includes at least one (in this embodiment, a plurality) of channel stop contact regions **122** of the p-type each formed in a region differing from the second high concentration region **43** in the surface layer portion of the second intermediate concentration region **121** at the first principal surface **3** side. In this embodiment, the channel stop contact regions **122** are formed in a surface layer portion of the second intermediate concentration region **121** at the second high concentration region **43** side.

[0109] A part of each channel stop contact region **122** may be formed in the second high

concentration region **43**. That is, the channel stop contact region **122** may be formed across the second high concentration region **43** and the second intermediate concentration region **121** at a boundary portion therebetween. A bottom surface of the channel stop contact region **122** is covered by the second intermediate concentration region **121**. In this embodiment, two channel stop contact regions **122** are formed.

[0110] In this embodiment, the channel stop contact regions **122** have the same p-type impurity concentration as the channel contact regions **31**. Such channel stop contact regions **122** can be formed, for example, at the same time as the channel contact regions **31** in the step of forming the channel contact regions **31**.

[0111] The semiconductor device **1**A includes a principal surface insulating film **45** selectively covering the first principal surface **3**. The principal surface insulating film **45** selectively covers the first principal surface **3** in the active regions **6**, the boundary region **8**, and the outer peripheral region **9**. The principal surface insulating film **45** may include at least one among a silicon oxide film, a silicon nitride film, and an aluminum oxide film.

[0112] The principal surface insulating film **45** preferably has a single layer structure constituted of a single insulating film. The principal surface insulating film **45** particularly preferably includes a silicon oxide film that is constituted of the oxide of the chip **2**. In this embodiment, the principal surface insulating film **45** is constituted of the same insulating film as the first insulating films **23** (separation insulation films **17**). The principal surface insulating film **45** covers the first principal surface **3** such as to expose the trench separation structures **15**, the first trench structures **21**, and the second trench structures **25**.

[0113] Specifically, the principal surface insulating film **45** is connected to the separation insulation films **17**, the first insulating films **23**, and the second insulating films **27** and exposes the separation embedded electrodes **18**, the first embedded electrodes **24**, and the second embedded electrodes **28**. The principal surface insulating film **45** selectively covers the boundary well region **40**, the outer peripheral well region **41**, the field regions **42**, the second high concentration region **43**, and the second intermediate concentration region **121** in the boundary region **8** and the outer peripheral region **9**.

[0114] The semiconductor device **1**A includes a field insulating film **46** that selectively covers the first principal surface **3** in the outer peripheral region **9**. The principal surface insulating film **45** and the field insulating film **46** are an example of a “surface insulating film” in the present disclosure. The field insulating film **46** may include at least one among a silicon oxide film, a silicon nitride film, and an aluminum oxide film.

[0115] The field insulating film **46** is thicker than the principal surface insulating film **45**. The field insulating film **46** includes a first field insulating film **131**, a plurality of second field insulating films **132**, and a third field insulating film **133**.

[0116] The first field insulating film **131** is formed on the first principal surface **3** across an outer peripheral edge portion of the outer peripheral well region **41** and an inner peripheral edge portion of the field region **42** at the innermost side. In this embodiment, the first field insulating film **131** is formed in a band shape extending along the outer peripheral well region **41**.

[0117] Each second field insulating film **132** is formed on the first principal surface **3** across an outer peripheral edge portion of the field region **42** at the inner side and an inner peripheral edge portion of the field region **42** at the outer side among two mutually adjacent field regions **42**. Each second field insulating film **132** is formed in a band shape extending along the field region **42** at the inner side among the two corresponding field regions **42**.

[0118] The third field insulating film **133** is formed on the first principal surface **3** such as to cover a region from a position near an outer peripheral edge of the field region **42** at the outermost side to a vicinity of the second intermediate concentration region **121**. The third field insulating film **133** is formed at an interval to the outermost field region **42** side from the second intermediate concentration region **121**. In this embodiment, the third field insulating film **133** is formed in a

band shape extending along the field region **42** at the outermost side.
[0119] An inner peripheral edge of the first field insulating film **131** is connected to an outer peripheral edge of the principal surface insulating film **45** on the outer peripheral well region **41**. An outer peripheral edge of the first field insulating film **131** is connected to an inner peripheral edge of the principal surface insulating film **45** that covers a width intermediate portion of the field region **42** at the innermost side.
[0120] An inner peripheral edge of each second field insulating film **132** that crosses two mutually adjacent field regions **42** is connected to an outer peripheral edge of the principal surface insulating film **45** that covers a width intermediate portion of the field region **42** at the inner side and an outer peripheral edge of the second field insulating film **132** is connected to an inner peripheral edge of the principal surface insulating film **45** that covers a width intermediate portion of the field region **42** at the outer side.
[0121] An inner peripheral edge of the third field insulating film **133** is connected to an outer peripheral edge of the principal surface insulating film **45** that covers a width intermediate portion of the field region **42** at the outermost side. An outer peripheral edge of the third field insulating film **133** is connected to an inner peripheral edge of the principal surface insulating film **45** that is formed further to the peripheral edge side of the chip **2**.
[0122] With reference to FIG. **3** and FIG. **5**, the semiconductor device **1**A includes a plurality of emitter electrode films **47** disposed on the first principal surface **3** such as to cover the plurality of second trench structures **25** in the active regions **6**. Specifically, the plurality of emitter electrode films **47** are disposed on the principal surface insulating film **45**. The plurality of emitter electrode films **47** may contain a conductive polysilicon.
[0123] The plurality of emitter electrode films **47** cover both end portions of the plurality of second trench structures **25** in the second direction Y, respectively. In this embodiment, the plurality of emitter electrode films **47** are each formed in a band shape extending in the second direction Y in a region between the corresponding second trench structure **25** and the trench separation structure **15**. The plurality of emitter electrode films **47** are formed at intervals toward the second trench structure **25** side from the trench separation structure **15**. The plurality of emitter electrode films **47** face the channel region **20** with the principal surface insulating film **45** interposed therebetween.
[0124] The plurality of emitter electrode films **47** are respectively formed integrally with the second embedded electrodes **28** of the plurality of second trench structures **25**. That is, each of the plurality of emitter electrode films **47** is constituted of a portion where a part of the second embedded electrode **28** is led out in a film shape onto the first principal surface **3** (the principal surface insulating film **45**). As a matter of course, the plurality of emitter electrode films **47** may be formed separately from the second embedded electrodes **28** instead.
[0125] FIG. **11** is an enlarged plan view showing the pad region **10**. FIG. **12** is an enlarged plan view showing a gate resistive structure **50** shown in FIG. **11**. FIG. **13** is an enlarged plan view showing an inner portion of the gate resistive structure **50** shown in FIG. **12**. FIG. **14** is an enlarged plan view showing one end portion of the gate resistive structure **50** shown in FIG. **12**. FIG. **15** is an enlarged plan view showing another end portion of the gate resistive structure **50** shown in FIG. **12**.
[0126] FIG. **16** is a cross-sectional view taken along line XVI-XVI shown in FIG. **13**. FIG. **17** is a cross-sectional view taken along line XVII-XVII shown in FIG. **13**. FIG. **18** is a cross-sectional view taken along line XVIII-XVIII shown in FIG. **13**. FIG. **19** is a cross-sectional view taken along line XIX-XIX shown in FIG. **13**. FIG. **20** is a cross-sectional view taken along line XX-XX shown in FIG. **14**.
[0127] FIG. **21** is a cross-sectional view taken along line XXI-XXI shown in FIG. **15**. FIG. **22** is a cross-sectional view taken along line XXII-XXII shown in FIG. **12**. FIG. **23** is a plan view showing a layout of a resistive film **60**, a gate electrode film **64**, and a gate wiring film **65**. FIG. **24** is an electric circuit diagram showing the gate resistive structure **50**, a gate terminal electrode **90**, and a

gate wiring electrode **93**.

[0128] With reference to FIG. **11** to FIG. **24**, the semiconductor device **1**A includes the gate resistive structure **50** formed in the pad region **10**. The gate resistive structure **50** constitutes a gate resistance RG for a gate of the IGBT (the first trench structures **21** of the IGBT structure Tr). The gate resistive structure **50** includes a plurality of trench resistive structures **51** formed in the first principal surface **3** in the pad region **10**. The gate potential is applied to the plurality of trench resistive structures **51**, however, the plurality of trench resistive structures **51** do not contribute to control of channels.

[0129] In this embodiment, the plurality of trench resistive structures **51** constitute a first trench group **52** and a second trench group **53**. The first trench group **52** includes a plurality of first trench resistive structures **51**A that constitute a part of the plurality of trench resistive structures **51** and is provided at one side (the first side surface **5**A side) in the second direction Y. The number of the first trench resistive structures **51**A is arbitrary and is adjusted based on a resistance value to be achieved.

[0130] For example, the first trench group **52** may include not less than 2 and not more than 100 first trench resistive structures **51**A. The number of the first trench resistive structures **51**A is preferably not more than 50. The number of the first trench resistive structures **51**A may be not more than 25. The number of the first trench resistive structures **51**A is preferably not less than 5. As a matter of course, the gate resistive structure **50** may include a single first trench resistive structure **51**A instead of the first trench group **52**.

[0131] In this embodiment, the first trench group **52** is provided in a region at one side (the first side surface **5**A side) in the second direction Y with respect to the straight line crossing the center of the first principal surface **3** in the first direction X. The first trench group **52** is preferably disposed such as to be shifted further to the active region **6** side (the street region **11** side) than the outer peripheral region **9** in the pad region **10**. In this embodiment, the first trench group **52** is disposed at an interval to the active region **6** side (the street region **11** side) from a central portion of the pad region **10**. These arrangements are effective in suppressing electric field concentration on the plurality of first trench resistive structures **51**A.

[0132] The plurality of first trench resistive structures **51**A are formed in the first principal surface **3** at intervals from the plurality of trench separation structures **15** (the plurality of first trench structures **21**). The plurality of first trench resistive structures **51**A are aligned at intervals in the first direction X in plan view and are each formed in a band shape extending in the second direction Y. That is, the plurality of first trench resistive structures **51**A are aligned in a stripe shape extending in the second direction Y. The plurality of first trench resistive structures **51**A have one end portions at one side (the first side surface **5**A side) in the second direction Y and other end portions at another side (the second side surface **5**B side) in the second direction Y.

[0133] The plurality of first trench resistive structures **51**A are formed at intervals to the first principal surface **3** side from a bottom portion of the boundary well region **40** (the first boundary well region **40**A) such as to be positioned inside the boundary well region **40** (the first boundary well region **40**A) and face the drift region **12** with a part of the boundary well region **40** interposed therebetween. That is, the plurality of first trench resistive structures **51**A do not penetrate through the boundary well region **40** (the first boundary well region **40**A).

[0134] The intervals between the plurality of first trench resistive structures **51**A are preferably less than the width of the street region **11**. The intervals between the plurality of first trench resistive structures **51**A are preferably substantially equal to the interval between a first trench structure **21** and a second trench structure **25**. The intervals between the plurality of first trench resistive structures **51**A may be smaller than the interval between the first trench structure **21** and the second trench structure **25**. The intervals between the plurality of first trench resistive structures **51**A may be larger than the interval between the first trench structure **21** and the second trench structure **25**.

[0135] The width of each first trench resistive structure **51**A is preferably less than the width of the

street region **11**. The width of the first trench resistive structure **51**A is a width in a direction orthogonal to the direction in which the first trench resistive structure **51**A extends. The width of the first trench resistive structure **51**A may be not less than 0.1 μm and not more than 2.5 μm. The width of the first trench resistive structure **51**A is preferably not less than 0.3 μm and not more than 1 μm.

[0136] The width of the first trench resistive structure **51**A is particularly preferably not less than 0.4 μm and not more than 0.7 μm. The width of the first trench resistive structure **51**A is preferably substantially equal to the width of each first trench structure **21**. The first trench resistive structure **51**A may have a depth of not less than 1 μm and not more than 20 μm. The depth of the first trench resistive structure **51**A is preferably not less than 4 μm and not more than 10 μm. The depth of the first trench resistive structure **51**A is preferably substantially equal to the depth of the first trench structure **21**.

[0137] The second trench group **53** includes a plurality of second trench resistive structures **51**B that constitute a part of the plurality of trench resistive structures **51** and is provided at an interval to the other side (the second side surface **5**B side) in the second direction Y from the first trench group **52**. The number of the second trench resistive structures **51**B is arbitrary and is adjusted based on a resistance value to be achieved. For example, when a resistance value substantially equal to the resistance value at the first trench group **52** side is to be realized, the second trench group **53** may include the second trench resistive structures **51**B of the same number as the number of the first trench resistive structures **51**A.

[0138] For example, when a resistance value different from the resistance value at the first trench group **52** side is to be realized, the second trench group **53** may include the second trench resistive structures **51**B of a different number from the number of first trench resistive structures **51**A. For example, when the resistance value at the second trench group **53** side is larger than the resistance value at the first trench group **52** side, the number of the second trench resistive structures **51**B may be smaller than the number of the first trench resistive structures **51**A. For example, when the resistance value at the second trench group **53** side is less than the resistance value at the first trench group **52** side, the number of the second trench resistive structures **51**B may be larger than the number of the first trench resistive structures **51**A.

[0139] For example, the second trench group **53** may include not less than 2 and not more than 100 second trench resistive structures **51**B. The number of the second trench resistive structures **51**B is preferably not more than 50. The number of the second trench resistive structures **51**B may be not more than 25. The number of the second trench resistive structures **51**B is preferably not less than 5. As a matter of course, the semiconductor device **1**A may include a single second trench resistive structure **51**B instead of the second trench group **53**.

[0140] In this embodiment, the second trench group **53** is provided in a region at the other side (the second side surface **5**B side) in the second direction Y with respect to the straight line crossing the center of the first principal surface **3** in the first direction X. The second trench group **53** faces the first trench group **52** in the second direction Y. The second trench group **53** is preferably disposed such as to be shifted further to the active region **6** side (the street region **11** side) than the outer peripheral region **9** in the pad region **10**. In this embodiment, the second trench group **53** is disposed at an interval to the active region **6** side (the street region **11** side) from the central portion of the pad region **10**. These arrangements are effective in suppressing electric field concentration on the plurality of second trench resistive structures **51**B.

[0141] The plurality of second trench resistive structures **51**B are formed in the first principal surface **3** at intervals from the plurality of trench separation structures **15** (the plurality of first trench structures **21**). The plurality of second trench resistive structures **51**B are aligned at intervals in the first direction X in plan view and are each formed in a band shape extending in the second direction Y.

[0142] That is, the plurality of second trench resistive structures **51**B are aligned in a stripe shape

extending in the second direction Y. The plurality of second trench resistive structures **51**B respectively face the plurality of first trench resistive structures **51**A in a one-to-one correspondence in the second direction Y. That is, the plurality of second trench resistive structures **51**B are respectively disposed in the same straight lines as the plurality of first trench resistive structures **51**A. The plurality of second trench resistive structures **51**B have one end portions at one side (the first side surface **5**A side) in the second direction Y and other end portions at the other side (the second side surface **5**B side) in the second direction Y.

[0143] The plurality of second trench resistive structures **51**B are formed at intervals to the first principal surface **3** side from the bottom portion of the boundary well region **40** (the first boundary well region **40**A) such as to be positioned inside the boundary well region **40** (the first boundary well region **40**A) and face the drift region **12** with a part of the boundary well region **40** interposed therebetween. That is, the plurality of second trench resistive structures **51**B do not penetrate through the boundary well region **40** (the first boundary well region **40**A).

[0144] The intervals between the plurality of second trench resistive structures **51**B are preferably less than the width of the street region **11**. The intervals between the plurality of second trench resistive structures **51**B are preferably substantially equal to the interval between a first trench structure **21** and a second trench structure **25** that are mutually adjacent. The intervals between the plurality of second trench resistive structures **51**B may be smaller than the interval between the first trench structure **21** and the second trench structure **25**. The intervals between the plurality of second trench resistive structures **51**B may be larger than the interval between the first trench structure **21** and the second trench structure **25**.

[0145] The intervals between the plurality of second trench resistive structures **51**B may be smaller than the intervals between the plurality of first trench resistive structures **51**A. The intervals between the plurality of second trench resistive structures **51**B may be larger than the intervals between the plurality of first trench resistive structures **51**A. The intervals between the plurality of second trench resistive structures **51**B are preferably substantially equal to the intervals between the plurality of first trench resistive structures **51**A.

[0146] The width of each second trench resistive structure **51**B is preferably less than the width of the street region **11**. The width of the second trench resistive structure **51**B is a width in a direction orthogonal to the direction in which the second trench resistive structure **51**B extends. The width of the second trench resistive structure **51**B may be not less than 0.1 μm and not more than 2.5 μm. The width of the second trench resistive structure **51**B is preferably not less than 0.3 μm and not more than 1 μm. The width of the second trench resistive structure **51**B is particularly preferably not less than 0.4 μm and not more than 0.7 μm. The width of the second trench resistive structure **51**B is preferably substantially equal to the width of each first trench resistive structure **51**A.

[0147] In this embodiment, each second trench resistive structure **51**B has a length substantially equal to a length of each first trench resistive structure **51**A in the second direction Y. As a matter of course, the second trench resistive structure **51**B may be longer than the first trench resistive structure **51**A in the second direction Y. Also, the second trench resistive structure **51**B may be shorter than the first trench resistive structure **51**A in the second direction Y. The length of the first trench resistive structure **51**A and the length of the second trench resistive structure **51**B are adjusted according to the resistance values to be achieved.

[0148] Each second trench resistive structure **51**B may have a depth of not less than 1 μm and not more than 20 μm. The depth of the second trench resistive structure **51**B is preferably not less than 4 μm and not more than 10 μm. The depth of the second trench resistive structure **51**B is preferably substantially equal to the depth of each first trench resistive structure **51**A (the first trench structure **21**).

[0149] Hereinafter, the arrangement of a single trench resistive structure **51** (first trench resistive structure **51**A or second trench resistive structure **51**B) is described. The trench resistive structure **51** includes a resistance trench **54**, a resistance insulation film **55**, and a resistance embedded

electrode **56**. The resistance trench **54** is formed in the first principal surface **3** and demarcates a wall surface of the trench resistive structure **51**.

[0150] The resistance insulation film **55** covers a wall surface of the resistance trench **54** in a film shape. The resistance insulation film **55** is connected to the principal surface insulating film **45** on the first principal surface **3**. The resistance insulation film **55** may include at least one among a silicon oxide film, a silicon nitride film, and an aluminum oxide film. The resistance insulation film **55** preferably has a single layer structure constituted of a single insulating film. The resistance insulation film **55** particularly preferably includes a silicon oxide film that is constituted of the oxide of the chip **2**.

[0151] The resistance embedded electrode **56** is embedded in the resistance trench **54** with the resistance insulation film **55** interposed therebetween. The resistance embedded electrode **56** may contain a conductive polysilicon. The gate potential is applied to the resistance embedded electrode **56**.

[0152] In this embodiment, the gate resistive structure **50** includes a space region **57** demarcated in a region of the pad region **10** between the first trench group **52** and the second trench group **53**. The space region **57** is formed by a flat portion of the first principal surface **3** in a region between the other end portions of the plurality of first trench resistive structures **51**A and the one end portions of the plurality of second trench resistive structures **51**B.

[0153] In this embodiment, the space region **57** is demarcated in a quadrangular shape in plan view. The space region **57** exposes the boundary well region **40** from the first principal surface **3**. In this embodiment, the space region **57** is formed on the straight line crossing the center of the first principal surface **3** in the first direction X in plan view and faces the street region **11** in the first direction X.

[0154] The space region **57** has a space width along the second direction Y. The space width is larger than the width of the first trench resistive structure **51**A (the second trench resistive structure **51**B) in the first direction X. The space width is larger than the interval between two first trench resistive structures **51**A (the second trench resistive structures **51**B) that are mutually adjacent in the first direction X. The space width is preferably larger than the width of the first trench group **52** (the second trench group **53**) in the first direction X. The space width may be smaller than the width of the first trench group **52** (the second trench group **53**) in the first direction X.

[0155] The space width is preferably smaller than the length of the first trench group **52** (the second trench group **53**) in the second direction Y. The space width may be substantially equal to the width of the street region **11** in the second direction Y. The space width may be larger than the width of the street region **11** in the second direction Y. The space width may be smaller than the width of the street region **11** in the second direction Y.

[0156] The gate resistive structure **50** includes the resistive film **60** disposed on the first principal surface **3** such as to cover the plurality of trench resistive structures **51** in the pad region **10**. Specifically, the resistive film **60** is disposed on the principal surface insulating film **45**. The resistive film **60** includes at least one among a conductive polysilicon film and an alloy film.

[0157] The alloy film may contain an alloy crystal constituted of a metal element and a non-metal element. The alloy film may include at least one among a CrSi film, a CrSiN film, a CrSiO film, a TaN film, and a TiN film. In this embodiment, the resistive film **60** contains a conductive polysilicon.

[0158] A thickness of the resistive film **60** is adjusted as appropriate in accordance with the resistance value to be attained. The thickness of the resistive film **60** is preferably not more than the depth of the first trench resistive structures **51**A (the second trench resistive structures **51**B). The thickness of the resistive film **60** is particularly preferably less than the depth of the first trench resistive structures **51**A (the second trench resistive structures **51**B).

[0159] The thickness of the resistive film **60** is preferably not less than 0.5 times the width of the first trench resistive structures **51**A (the second trench resistive structures **51**B). The thickness of

the resistive film **60** may be not less than 0.05 μm and not more than 2.5 μm. The thickness of the resistive film **60** is preferably not less than 0.5 μm and not more than 1.5 μm. When the resistive film **60** is constituted of the alloy film, the thickness of the resistive film **60** may be not less than 0.1 nm and not more than 100 nm.

[0160] The resistive film **60** is formed in a band shape extending in the second direction Y and has a first end portion **60**A at one side (the first side surface **5**A side) in the second direction Y and a second end portion **60**B at the other side (the second side surface **5**B side) in the second direction Y. In regard to the first direction X, the resistive film **60** has a width larger than the width of the first trench group **52** (the second trench group **53**) in the first direction X. The width of the resistive film **60** may be less than the space width. As a matter of course, the width of the resistive film **60** may be not less than the space width. The resistive film **60** preferably has a uniform width in regard to the first direction X.

[0161] The resistive film **60** has a portion positioned at one side (the first side surface **5**A side) and a portion positioned at the other side (the second side surface **5**B side) in the second direction Y with respect to the straight line crossing the center of the first principal surface **3** in the first direction X. The resistive film **60** faces the first active region **6**A, the second active region **6**B, and the street region **11** in the first direction X. That is, the resistive film **60** faces the plurality of trench separation structures **15**, the plurality of first trench structures **21**, and the plurality of second trench structures **25** in the first direction X.

[0162] The resistive film **60** includes a first covering portion **61** that covers the space region **57**, a second covering portion **62** that covers the first trench group **52**, and a third covering portion **63** that covers the second trench group **53**. The first covering portion **61** is a portion that covers the first principal surface **3** in a region outside the first trench group **52** (the plurality of first trench resistive structures **51**A) and the second trench group **53** (the plurality of second trench resistive structures **51**B). The first covering portion **61** is positioned at an intermediate portion between the first end portion **60**A and the second end portion **60**B and faces the boundary well region **40** with the principal surface insulating film **45** interposed therebetween in the thickness direction.

[0163] The second covering portion **62** forms the first end portion **60**A of the resistive film **60** and covers all of the first trench resistive structures **51**A. The second covering portion **62** forms the first end portion **60**A further to an outer side (a peripheral edge side of the pad region **10**) than the one end portions of the plurality of first trench resistive structures **51**A. That is, the first end portion **60**A faces the first covering portion **61** with the first trench group **52** interposed therebetween in plan view. The second covering portion **62** is connected to the resistance embedded electrodes **56** of the plurality of first trench resistive structures **51**A and faces the boundary well region **40** with the principal surface insulating film **45** interposed therebetween in the thickness direction.

[0164] The third covering portion **63** forms the second end portion **60**B of the resistive film **60** and covers all of the second trench resistive structures **51**B. The third covering portion **63** forms the second end portion **60**B further to an outer side (a peripheral edge side of the pad region **10**) than the other end portions of the plurality of second trench resistive structures **51**B. That is, the second end portion **60**B faces the first covering portion **61** with the second trench group **53** interposed therebetween in plan view. The third covering portion **63** is connected to the resistance embedded electrode **56** of the plurality of second trench resistive structures **51**B and faces the boundary well region **40** with the principal surface insulating film **45** interposed therebetween in the thickness direction.

[0165] The resistive film **60** is integrally formed with the resistance embedded electrodes **56** of the plurality of first trench resistive structures **51**A in the second covering portion **62** and is integrally formed with the resistance embedded electrodes **56** of the plurality of second trench resistive structures **51**B in the third covering portion **63**. That is, the resistive film **60** is constituted of a portion where a part of each resistance embedded electrode **56** is led out in a film shape onto the first principal surface **3** (the principal surface insulating film **45**). As a matter of course, the

resistive film **60** may be formed separately from the resistance embedded electrodes **56** instead.
[0166] The semiconductor device **1**A includes the gate electrode film **64** disposed on the first principal surface **3** such as to be mutually adjacent to the resistive film **60**. Specifically, the gate electrode film **64** is disposed on the principal surface insulating film **45**. The gate electrode film **64** includes at least one among a conductive polysilicon film and an alloy film. The alloy film may contain an alloy crystal constituted of a metal element and a non-metal element.
[0167] The alloy film may include at least one among a CrSi film, a CrSiN film, a CrSiO film, a TaN film, and a TiN film. The gate electrode film **64** is preferably formed of the same resistance material as the resistive film **60**. In this embodiment, the gate electrode film **64** contains a conductive polysilicon. The gate electrode film **64** preferably has a thickness substantially equal to the thickness of the resistive film **60**.
[0168] The gate electrode film **64** is disposed on the principal surface insulating film **45** at an interval to an inner portion side (the third side surface **5**C side) of the pad region **10** from the resistive film **60** and is physically separated from the resistive film **60**. The gate electrode film **64** is formed at an interval to the inner portion side of the pad region **10** from the plurality of trench separation structures **15** in plan view.
[0169] The gate electrode film **64** faces the boundary well region **40** (the first boundary well region **40**A) with the principal surface insulating film **45** interposed therebetween. The gate electrode film **64** is formed in a polygonal shape (in this embodiment, a quadrangular shape) in plan view. In this embodiment, the gate electrode film **64** is formed in a rectangular shape extending in the second direction Y along the resistive film **60**.
[0170] With reference to FIG. **11**, FIG. **12**, and FIG. **24**, the semiconductor device **1**A includes the gate wiring film **65** disposed on the first principal surface **3** to be mutually adjacent to the resistive film **60** such as to face the gate electrode film **64** with the resistive film **60** interposed therebetween. Specifically, the gate wiring film **65** is disposed on the principal surface insulating film **45**. The gate wiring film **65** includes at least one among a conductive polysilicon film and an alloy film. The alloy film may contain an alloy crystal constituted of a metal element and a non-metal element.
[0171] The alloy film may include at least one among a CrSi film, a CrSiN film, a CrSiO film, a TaN film, and a TiN film. The gate wiring film **65** is preferably formed of the same resistance material as the resistive film **60**. In this embodiment, the gate wiring film **65** contains a conductive polysilicon. The gate wiring film **65** preferably has a thickness substantially equal to the thickness of the resistive film **60**.
[0172] The gate wiring film **65** is disposed on the principal surface insulating film **45** at an interval from the gate electrode film **64** and is physically separated from the gate electrode film **64**. The gate wiring film **65** has a first connection portion connected to the first end portion **60**A of the resistive film **60** and a second connection portion connected to the second end portion **60**B of the resistive film **60**.
[0173] That is, the gate wiring film **65** is electrically connected to the plurality of trench resistive structures **51** via the resistive film **60**. Specifically, the gate wiring film **65** is electrically connected, at a portion between the first covering portion **61** and the second covering portion **62** of the resistive film **60**, to the plurality of first trench resistive structures **51**A and is electrically connected, at a portion between the first covering portion **61** and the third covering portion **63** of the resistive film **60**, to the plurality of second trench resistive structures **51**B.
[0174] In this embodiment, the gate wiring film **65** includes a first lower wiring portion **66**, a second lower wiring portion **67**, and a third lower wiring portion **68**. The first lower wiring portion **66** is routed to the pad region **10**. Specifically, the first lower wiring portion **66** surrounds the resistive film **60** and the gate electrode film **64** from a plurality of directions (in this embodiment, three directions) in the pad region **10**.
[0175] The first lower wiring portion **66** includes a first lower line portion **69** and a plurality of

second lower line portions **70**A and **70**B. The first lower line portion **69** is disposed at the street region **11** side with respect to the resistive film **60** in the pad region **10**. The first lower line portion **69** is disposed on the first principal surface **3** to be mutually adjacent to the resistive film **60** such as to face the gate electrode film **64** with the resistive film **60** interposed therebetween in plan view. The first lower line portion **69** faces the boundary well region **40** (the first boundary well region **40**A) with the principal surface insulating film **45** interposed therebetween in the thickness direction.

[0176] The first lower line portion **69** is formed in a band shape extending in the second direction Y along the resistive film **60**. The first lower line portion **69** has a length larger than a length of the resistive film **60** and a length of the gate electrode film **64** in the second direction Y. The first lower line portion **69** has one end portion at one side (the first side surface **5**A side) in the second direction Y and another end portion at the other side (the second side surface **5**B side) in the second direction Y.

[0177] The plurality of second lower line portions **70**A and **70**B include the second lower line portion **70**A at one side and the second lower line portion **70**B at another side. The second lower line portion **70**A is disposed in a region at one side (the first side surface **5**A side) in the second direction Y with respect to the resistive film **60** and the gate electrode film **64** in the pad region **10**. The second lower line portion **70**B is disposed in a region at the other side (the second side surface **5**B side) in the second direction Y with respect to the resistive film **60** and the gate electrode film **64** in the pad region **10**.

[0178] The second lower line portion **70**A is formed in a band shape extending in the first direction X and has one end portion connected to the one end portion of the first lower line portion **69** and another end portion positioned at the peripheral edge side (the third side surface **5**C side) of the chip **2**. The second lower line portion **70**A is further connected to the first end portion **60**A of the resistive film **60** and formed at an interval from the gate electrode film **64**. That is, the second lower line portion **70**A constitutes the first connection portion with respect to the first end portion **60**A. The second lower line portion **70**A faces the boundary well region **40** (the first boundary well region **40**A) with the principal surface insulating film **45** interposed therebetween in the thickness direction.

[0179] The second lower line portion **70**B is formed in a band shape extending in the first direction X and has one end portion connected to the other end portion of the first lower line portion **69** and another end portion positioned at the peripheral edge side (the third side surface **5**C side) of the chip **2**. The second lower line portion **70**B at the other side is further connected to the second end portion **60**B of the resistive film **60** and formed at an interval from the gate electrode film **64**.

[0180] That is, the second lower line portion **70**B constitutes the second connection portion with respect to the second end portion **60**B. The second lower line portion **70**B at the other side faces the second lower line portion **70**A at one side with the gate electrode film **64** interposed therebetween. The second lower line portion **70**B at the other side faces the boundary well region **40** (the first boundary well region **40**A) with the principal surface insulating film **45** interposed therebetween in the thickness direction.

[0181] The second lower wiring portion **67** is routed to the street region **11**. Specifically, the second lower wiring portion **67** is led out from the first lower wiring portion **66** to the street region **11**. More specifically, the second lower wiring portion **67** is led out from an inner portion (in this embodiment, a central portion) of the first lower line portion **69** to the street region **11** and is formed in a band shape extending in the first direction X.

[0182] In this embodiment, the second lower wiring portion **67** crosses a center of the chip **2**. The second lower wiring portion **67** extends in a band shape such as to be positioned in a region at one side (the third side surface **5**C side) and a region at the other side (the fourth side surface **5**D side) in the first direction X with respect to the straight line crossing the center of the first principal surface **3** in the second direction Y. The second lower wiring portion **67** has one end portion

connected to the first lower line portion **69** (the first lower wiring portion **66**) at one side in the first direction X and another end portion at the other side in the first direction X.

[0183] The second lower wiring portion **67** faces the boundary well region **40** (the second boundary well region **40**B) with the principal surface insulating film **45** interposed therebetween in the thickness direction. The second lower wiring portion **67** has a width larger than the width of the street region **11** in the second direction Y and is led out from the street region **11** to the plurality of active regions **6**. The second lower wiring portion **67** covers the plurality of trench separation structures **15** in the plurality of active regions **6**.

[0184] Also, the second lower wiring portion **67** covers the end portions of the plurality of first trench structures **21** in the plurality of active regions **6**. Consequently, the second lower wiring portion **67** is electrically connected to the plurality of separation embedded electrodes **18** and the plurality of first embedded electrodes **24** and transmits the gate potential to the plurality of separation embedded electrodes **18** and the plurality of first embedded electrodes **24**.

[0185] In this embodiment, the second lower wiring portion **67** is integrally formed with the plurality of separation embedded electrodes **18** and the plurality of first embedded electrodes **24**. That is, the second lower wiring portion **67** is constituted of a portion where a part of the plurality of separation embedded electrodes **18** and a part of the plurality of first embedded electrodes **24** are led out in film shapes onto the first principal surface **3** (the principal surface insulating film **45**). As a matter of course, the second lower wiring portion **67** may be formed separately from the plurality of separation embedded electrodes **18** and the plurality of first embedded electrodes **24** instead.

[0186] The third lower wiring portion **68** is routed to the outer peripheral region **9**. Specifically, the third lower wiring portion **68** is led out from the first lower wiring portion **66** to the outer peripheral region **9**. More specifically, the third lower wiring portion **68** is led out from the other end portions of the plurality of second lower line portions **70**A and **70**B to one side (the first side surface **5**A side) and the other side (the second side surface **5**B side) of the outer peripheral region **9** and is formed in a band shape extending along the outer peripheral region **9**.

[0187] The third lower wiring portion **68**, together with the second lower wiring portion **67**, sandwiches the plurality of active regions **6**. Specifically, the third lower wiring portion **68** extends along the peripheral edge (the first to fourth side surfaces **5**A to **5**D) of the chip **2** such as to surround the plurality of active regions **6** in plan view and is connected to the other end portion of the second lower wiring portion **67**. Thereby, the third lower wiring portion **68**, together with the second lower wiring portion **67**, surrounds the plurality of active regions **6**.

[0188] The third lower wiring portion **68** faces an inner portion of the outer peripheral well region **41** with the principal surface insulating film **45** interposed therebetween. Specifically, the third lower wiring portion **68** faces the inner portion of the outer peripheral well region **41** at an interval inward from an inner edge and an outer edge of the outer peripheral well region **41** in plan view.

[0189] With reference to FIG. **3**, the third lower wiring portion **68** has, in portions extending along the first side surface **5**A, a plurality of lead-out portions **68***a* that are led out to the plurality of active regions **6** from the outer peripheral region **9**. The plurality of lead-out portions **68***a* cover the first trench separation structure **15**A at the first active region **6**A side and covers the second trench separation structure **15**B at the second active region **6**B side.

[0190] That is, the plurality of lead-out portions **68***a* cover the end portions of the plurality of first trench structures **21**. Consequently, in the first active region **6**A, the third lower wiring portion **68** is electrically connected to the plurality of separation embedded electrodes **18** and the plurality of first embedded electrodes **24** and transmits the gate potential to the plurality of separation embedded electrodes **18** and the plurality of first embedded electrodes **24**.

[0191] As a matter of course, a single lead-out portion **68***a* extending in a band shape along the first trench separation structure **15**A may be formed at the first active region **6**A side instead. Also, a single lead-out portion **68***a* extending in a band shape along the second trench separation structure **15**B may be formed on the second active region **6**B side.

[0192] In this embodiment, the third lower wiring portion **68** is integrally formed with the plurality of separation embedded electrodes **18** and the plurality of first embedded electrodes **24**. That is, the third lower wiring portion **68** is constituted of a portion where a part of the plurality of separation embedded electrodes **18** and a part of the plurality of first embedded electrodes **24** are led out in film shapes onto the first principal surface **3** (the principal surface insulating film **45**). As a matter of course, the third lower wiring portion **68** may be formed separately from the plurality of separation embedded electrodes **18** and the plurality of first embedded electrodes **24** instead.
[0193] With reference to FIG. **11** to FIG. **15**, the semiconductor device **1**A includes a first slit **71** demarcated in a region between the resistive film **60** and the gate electrode film **64**. The first slit **71** is formed in a band shape extending in the second direction Y in plan view and demarcates the first to third covering portions **61** to **63** of the resistive film **60**.
[0194] The first slit **71** exposes the principal surface insulating film **45**. The first slit **71** is formed outside the plurality of trench resistive structures **51** in plan view and faces the boundary well region **40** (the first boundary well region **40**A) in the thickness direction. That is, the first slit **71** does not face the trench resistive structures **51** in the thickness direction.
[0195] The first slit **71** has a first length in the second direction Y. The first slit **71** is formed to be narrower than the gate electrode film **64** in the first direction X. The first slit **71** is preferably formed to be narrower than the resistive film **60** in the first direction X. The first slit **71** is preferably formed to be narrower than the first trench group **52** in the first direction X. The first slit **71** is preferably formed to be wider than each trench resistive structure **51** in the first direction X.
[0196] A width of the first slit **71** may be not less than 0.1 μm and not more than 10 μm. The width of the first slit **71** may be not less than 0.1 μm and not more than 0.5 μm, not less than 0.5 μm and not more than 1 μm, not less than 1 μm and not more than 2.5 μm, not less than 2.5 μm and not more than 5 μm, not less than 5 μm and not more than 7.5 μm, or not less than 7.5 μm and not more than 10 μm. The width of the first slit **71** is preferably not less than 3 μm and not more than 7 μm.
[0197] With reference to FIG. **11** to FIG. **15**, the semiconductor device **1**A includes a second slit **72** demarcated in a region between the resistive film **60** and the gate wiring film **65**. Specifically, the second slit **72** is demarcated in a region between the resistive film **60** and the first lower line portion **69**. The second slit **72** faces the first slit **71** with the resistive film **60** interposed therebetween.
[0198] The second slit **72** is formed in a band shape extending in the second direction Y in plan view and demarcates the first to third covering portions **61** to **63** of the resistive film **60**. That is, the second slit **72** extends in parallel to the first slit **71** and, together with the first slit **71**, demarcates the resistive film **60**. The second slit **72** exposes the principal surface insulating film **45**.
[0199] The second slit **72** is formed outside the plurality of trench resistive structures **51** in plan view and faces the boundary well region **40** (the first boundary well region **40**A) in the thickness direction. That is, the second slit **72** does not face the trench resistive structures **51** in the thickness direction. The second slit **72** faces the first slit **71** with the plurality of first trench resistive structures **51**A and the plurality of second trench resistive structures **51**B interposed therebetween in plan view.
[0200] The second slit **72** has a second length in the second direction Y. The second length may be different from the first length of the first slit **71**. The second length is preferably not more than the first length from the viewpoint of appropriately connecting the resistive film **60** and the gate wiring film **65**. In this embodiment, the second length is less than the first length. As a matter of course, the second length may be substantially equal to the first length instead. Also, the second length may be larger than the first length.
[0201] The second slit **72** is formed to be narrower than the gate electrode film **64** in the first direction X. The second slit **72** is preferably formed to be narrower than the first lower line portion **69** in the first direction X. The second slit **72** is particularly preferably formed to be narrower than

the resistive film **60** in the first direction X. The second slit **72** is preferably formed to be narrower than the first trench group **52** in the first direction X. The second slit **72** is preferably formed to be wider than each trench resistive structure **51**.

[0202] A width of the second slit **72** may be not less than 0.1 μm and not more than 10 μm. The width of the second slit **72** may be not less than 0.1 μm and not more than 0.5 μm, not less than 0.5 μm and not more than 1 μm, not less than 1 μm and not more than 2.5 μm, not less than 2.5 μm and not more than 5 μm, not less than 5 μm and not more than 7.5 μm, or not less than 7.5 μm and not more than 10 μm. The width of the second slit **72** is preferably not less than 3 μm and not more than 7 μm. The width of the second slit **72** may be not less than the width of the first slit **71**. The width of the second slit **72** may be less than the width of the first slit **71**. The width of the second slit **72** may be substantially equal to the width of the first slit **71**.

[0203] With reference to FIG. **11** to FIG. **15**, the semiconductor device **1**A includes a plurality of third slits **73** demarcated in regions between the gate electrode film **64** and the gate wiring film **65**. Specifically, the plurality of third slits **73** are demarcated in regions between the gate electrode film **64** and the plurality of second lower line portions **70**A and **70**B, respectively.

[0204] Each of the plurality of third slits **73** is formed in a band shape extending in the first direction X in plan view and exposes the principal surface insulating film **45**. The plurality of third slits **73** are connected to the first slit **71** and face each other in the second direction Y with the gate electrode film **64** interposed therebetween. That is, the plurality of third slits **73** demarcates the gate electrode film **64** together with the first slit **71**. Also, the plurality of third slits **73**, together with the first slit **71**, physically and electrically separate the gate electrode film **64** from the gate wiring film **65**.

[0205] The third slit **73** is formed to be narrower than the gate electrode film **64**. The third slit **73** is preferably formed to be narrower than the second lower line portions **70**A and **70**B. The third slit **73** is particularly preferably formed to be narrower than the resistive film **60**. The third slit **73** is preferably formed to be narrower than the first trench group **52** (the second trench group **53**). The third slit **73** is preferably formed to be wider than each trench resistive structure **51**.

[0206] A width of each third slit **73** may be not less than 0.1 μm and not more than 10 μm. The width of the third slit **73** may be not less than 0.1 μm and not more than 0.5 μm, not less than 0.5 μm and not more than 1 μm, not less than 1 μm and not more than 2.5 μm, not less than 2.5 μm and not more than 5 μm, not less than 5 μm and not more than 7.5 μm, or not less than 7.5 μm and not more than 10 μm. The width of the third slit **73** is preferably not less than 3 μm and not more than 7 μm. The width of the third slit **73** may be not less than the width of the first slit **71**. The width of the third slit **73** may be less than the width of the first slit **71**. The width of the third slit **73** may be substantially equal to the width of the first slit **71**.

[0207] The semiconductor device **1**A includes an interlayer insulating film **74** that covers the principal surface insulating film **45** and field insulating film **46**. The interlayer insulating film **74** is thicker than the principal surface insulating film **45**. The interlayer insulating film **74** may have a single layer structure including a single insulating film or a laminated structure including a plurality of insulating films. The interlayer insulating film **74** may include at least one among a silicon oxide film, a silicon nitride film, and an aluminum oxide film.

[0208] The interlayer insulating film **74** may have a laminated structure including a plurality of silicon oxide films. In this case, the interlayer insulating film **74** may include at least one among an NSG (non-doped silicate glass) film, a PSG (phosphor silicate glass) film, and a BPSG (boron phosphor silicate glass) film as an example of a silicon oxide film. The order of lamination of the NSG film, the PSG film, and the BPSG film is arbitrary.

[0209] The interlayer insulating film **74** covers the principal surface insulating film **45** in the active regions **6**, the boundary region **8**, and the outer peripheral region **9**. In the active regions **6**, the interlayer insulating film **74** covers the plurality of trench separation structures **15**, the plurality of first trench structures **21**, and the plurality of second trench structures **25**. In the outer peripheral

region **9**, the interlayer insulating film **74** covers the field insulating film **46**.

[0210] In the pad region **10**, the interlayer insulating film **74** covers the plurality of trench resistive structures **51** (resistance embedded electrodes **56**), the resistive film **60**, the gate electrode film **64**, and the gate wiring film **65**. In the pad region **10**, the interlayer insulating film **74** covers the boundary well region **40** (the first boundary well region **40**A) with the principal surface insulating film **45** interposed therebetween. In the outer peripheral region **9**, the interlayer insulating film **74** selectively covers the outer peripheral well region **41**, the field regions **42**, the second high concentration region (channel stop region) **43**, and the second intermediate concentration region **121** with the principal surface insulating film **45** and the field insulating film **46** interposed therebetween.

[0211] The interlayer insulating film **74** enters into the first slit **71** from above the resistive film **60** and the gate electrode film **64** and has a portion that covers the principal surface insulating film **45** inside the first slit **71**. That is, inside the first slit **71**, the interlayer insulating film **74** faces the boundary well region **40** (the first boundary well region **40**A) with the principal surface insulating film **45** interposed therebetween in the thickness direction. Inside the first slit **71**, the interlayer insulating film **74** electrically insulates the resistive film **60** and the gate electrode film **64**.

[0212] The interlayer insulating film **74** enters into the second slit **72** from above the resistive film **60** and the gate wiring film **65** (the first lower line portion **69**) and has a portion that covers the principal surface insulating film **45** inside the second slit **72**. That is, inside the second slit **72**, the interlayer insulating film **74** faces the boundary well region **40** (the first boundary well region **40**A) with the principal surface insulating film **45** interposed therebetween in the thickness direction. Inside the second slit **72**, the interlayer insulating film **74** electrically insulates the resistive film **60** and the gate wiring film **65** (the first lower line portion **69**).

[0213] The interlayer insulating film **74** enter into the plurality of third slits **73** from above the gate electrode film **64** and the gate wiring film **65** (the second lower line portions **70**A and **70**B) and has portions that cover the principal surface insulating film **45** inside the plurality of third slits **73**. That is, inside the plurality of third slits **73**, the interlayer insulating film **74** faces the boundary well region **40** (the first boundary well region **40**A) with the principal surface insulating film **45** interposed therebetween in the thickness direction.

[0214] Inside the plurality of third slits **73**, the interlayer insulating film **74** electrically insulates the gate electrode film **64** and the gate wiring film **65**. The interlayer insulating film **74** has an insulating principal surface **75** extending along the first principal surface **3** (the principal surface insulating film **45**). The insulating principal surface **75** has, in the pad region **10**, a first recess portion **76**, a second recess portion **77**, and a plurality of third recess portions **78** (see FIG. **16** to FIG. **22**). The first recess portion **76** is formed in a portion that covers the first slit **71**. The first recess portion **76** is recessed toward the first slit **71** and is formed in a band shape extending in the second direction Y along the first slit **71** in plan view.

[0215] The second recess portion **77** is formed in a portion that covers the second slit **72**. The second recess portion **77** is recessed toward the second slit **72** and is formed in a band shape extending in the second direction Y along the second slit **72** in plan view. The plurality of third recess portions **78** are formed in portions covering the plurality of third slits **73**, respectively. Each of the plurality of third recess portions **78** is recessed toward the corresponding third slit **73** and is formed in a band shape extending in the first direction X along the corresponding third slit **73** in plan view.

[0216] With reference to FIG. **11** to FIG. **22**, the semiconductor device **1**A includes at least one (in this embodiment, a plurality) of first resistance connection electrodes **81** embedded in the interlayer insulating film **74** such as to be electrically connected to the resistive film **60**. The first resistance connection electrodes **81** may be referred to as “first resistance via electrodes.” Each first resistance connection electrode **81** may include at least one type among a Ti film, a TiN film, a W film, an Al film, a Cu film, an Al alloy film, a Cu alloy film, and a conductive polysilicon film. In this

embodiment, the first resistance connection electrode **81** has a laminated structure including a Ti film and a W film.

[0217] In this embodiment, the plurality of first resistance connection electrodes **81** are connected to the first covering portion **61** of the resistive film **60**. That is, the plurality of first resistance connection electrodes **81** are connected to a portion of the resistive film **60** covering a region outside the plurality of trench resistive structures **51**. Specifically, the plurality of first resistance connection electrodes **81** are connected to a portion of the resistive film **60** covering the space region **57** between the first trench group **52** (the plurality of first trench resistive structures **51**A) and the second trench group **53** (the plurality of second trench resistive structures **51**B).

[0218] The plurality of first resistance connection electrodes **81** are formed in regions at intervals from the plurality of trench resistive structures **51** in the second direction Y in plan view and do not face the plurality of trench resistive structures **51** in the first direction X. In this embodiment, the plurality of first resistance connection electrodes **81** are each formed in a band shape extending in the first direction X in plan view and are disposed at intervals in the second direction Y. That is, the plurality of first resistance connection electrodes **81** are aligned in a stripe shape extending in the first direction X in plan view.

[0219] The plurality of first resistance connection electrodes **81** extend in a direction intersecting (in this embodiment, orthogonal to) the extending direction of the resistive film **60** (the plurality of trench resistive structures **51**). That is, the plurality of first resistance connection electrodes **81** intersect (are orthogonal to) a current direction of the resistive film **60**. As a result, a current can be spread appropriately with respect to the resistive film **60** from the plurality of first resistance connection electrodes **81**. That is, current constriction caused by the layout of the plurality of first resistance connection electrodes **81** is suppressed, and an undesirable variation (increase) in the resistance value caused by the current constriction is suppressed.

[0220] The plurality of first resistance connection electrodes **81** face only the flat portion of the first principal surface **3** with the resistive film **60** interposed therebetween and do not face the trench resistive structures **51** with the resistive film **60** interposed therebetween. The plurality of first resistance connection electrodes **81** face the boundary well region **40** (the first boundary well region **40**A) with the resistive film **60** and the principal surface insulating film **45** interposed therebetween. The plurality of first resistance connection electrodes **81** are formed in a region sandwiched by the first slit **71** and the second slit **72** at intervals from the first slit **71** and the second slit **72** in plan view.

[0221] That is, the plurality of first resistance connection electrodes **81** are each formed to be narrower than the resistive film **60** in the first direction X. In plan view, the plurality of first resistance connection electrodes **81** face one or a plurality of first trench resistive structures **51**A at one side (the first side surface **5**A side) in the second direction Y and face one or a plurality of second trench resistive structures **51**B at the other side (the second side surface **5**B side) in the second direction Y.

[0222] The plurality of first resistance connection electrodes **81** suffice to face at least two of the plurality of first trench resistive structures **51**A in the second direction Y and do not have to face all of the first trench resistive structures **51**A. In this embodiment, the plurality of first resistance connection electrodes **81** face a part of the plurality of first trench resistive structures **51**A in the second direction Y. As a matter of course, the plurality of first resistance connection electrodes **81** may face all of the first trench resistive structures **51**A in the second direction Y instead.

[0223] Similarly, the plurality of first resistance connection electrodes **81** suffice to face at least two of the plurality of second trench resistive structures **51**B in the second direction Y and do not have to face all of the second trench resistive structures **51**B. In this embodiment, the plurality of first resistance connection electrodes **81** face a part of the plurality of second trench resistive structures **51**B in the second direction Y. As a matter of course, the plurality of first resistance connection electrodes **81** may face all of the second trench resistive structures **51**B in the second

direction Y instead.
[0224] The plurality of first resistance connection electrodes **81** have a first connection area S**1** with respect to the resistive film **60**. The first connection area S**1** is defined by a total plane area of the plurality of first resistance connection electrodes **81**. When a single first resistance connection electrode **81** is formed, the first connection area S**1** is defined by a plane area of the single first resistance connection electrode **81**. The first connection area S**1** is adjusted according to a first current I**1** flowing through the first resistance connection electrodes **81** (see FIG. **12**).
[0225] With reference to FIG. **11** to FIG. **22**, the semiconductor device **1**A includes at least one (in this embodiment, a plurality) of second resistance connection electrodes **82** embedded in the interlayer insulating film **74** such as to be electrically connected to the resistive film **60** at a location different from the first resistance connection electrode **81**. The second resistance connection electrodes **82** may be referred to as "second resistance via electrodes."
[0226] Each second resistance connection electrode **82** may include at least one type among a Ti film, a TiN film, a W film, an Al film, a Cu film, an Al alloy film, a Cu alloy film, and a conductive polysilicon film. In this embodiment, the second resistance connection electrode **82** has a laminated structure including a Ti film and a W film.
[0227] In this embodiment, the plurality of second resistance connection electrodes **82** are connected to the second covering portion **62** of the resistive film **60**. That is, the plurality of second resistance connection electrodes **82** are embedded in a portion of the resistive film **60** covering the first trench group **52** (the plurality of first trench resistive structures **51**A).
[0228] The plurality of second resistance connection electrodes **82**, with the plurality of first resistance connection electrodes **81**, form a first gate resistance R**1**. The first gate resistance R**1** is constituted of a portion of the resistive film **60** and the plurality of first trench resistive structures **51**A that is positioned in a region between the plurality of first resistance connection electrodes **81** and the plurality of second resistance connection electrodes **82**. A resistance value of the first gate resistance R**1** is adjusted by a distance between the plurality of first resistance connection electrodes **81** and the plurality of second resistance connection electrodes **82**.
[0229] The plurality of second resistance connection electrodes **82** are formed in regions facing the plurality of first trench resistive structures **51**A in the first direction X in plan view. In this embodiment, the plurality of second resistance connection electrodes **82** extend in a different direction from the first resistance connection electrodes **81** in plan view. Specifically, the plurality of second resistance connection electrodes **82** are each formed in a band shape extending in the second direction Y in plan view and are aligned at intervals in the first direction X. That is, the plurality of second resistance connection electrodes **82** are aligned in a stripe shape extending in the second direction Y in plan view.
[0230] In plan view, the plurality of second resistance connection electrodes **82** are respectively disposed, at intervals from the plurality of first trench resistive structures **51**A, in regions between the plurality of first trench resistive structures **51**A that are mutually adjacent. That is, the plurality of second resistance connection electrodes **82** are aligned alternately with the plurality of first trench resistive structures **51**A in the first direction X.
[0231] Also, in this embodiment, the plurality of second resistance connection electrodes **82** face only the flat portion of the first principal surface **3** with the resistive film **60** interposed therebetween and do not face the trench resistive structure **51** with the resistive film **60** interposed therebetween. The plurality of second resistance connection electrodes **82** face the boundary well region **40** (the first boundary well region **40**A) with the resistive film **60** and the principal surface insulating film **45** interposed therebetween.
[0232] The plurality of second resistance connection electrodes **82** suffice to be disposed in a part of the regions between the plurality of first trench resistive structures **51**A and do not necessarily have to be disposed in all of the regions between the plurality of first trench resistive structures **51**A. The plurality of second resistance connection electrodes **82** suffice to be disposed in at least

one region positioned at the active region **6** side among the regions between the plurality of first trench resistive structures **51**A and do not have to be disposed in at least one region positioned at the gate electrode film **64** side.

[0233] It is preferable that at least one of the plurality of second resistance connection electrodes **82** faces the plurality of first resistance connection electrodes **81** in the second direction Y in plan view. In this case, at least one of the plurality of second resistance connection electrodes **82** that is positioned at the gate electrode film **64** side preferably faces the plurality of first resistance connection electrodes **81** in the second direction Y.

[0234] At least one of the plurality of second resistance connection electrodes **82** that is positioned at the active region **6** side does not have to face the plurality of first resistance connection electrodes **81** in the second direction Y. As a matter of course, all of the second resistance connection electrodes **82** may be disposed such as to face the plurality of first resistance connection electrodes **81** in the second direction Y.

[0235] The plurality of second resistance connection electrodes **82** have a length less than the length of the plurality of first trench resistive structures **51**A in the second direction Y. The plurality of second resistance connection electrodes **82** are preferably disposed in regions at the other end portion side of the plurality of first trench resistive structures **51**A with respect to length direction intermediate portions of the plurality of first trench resistive structures **51**A.

[0236] The length of the plurality of second resistance connection electrodes **82** is preferably not less than 1/100 and not more than ½ of the length of the plurality of first trench resistive structures **51**A. The length of the plurality of second resistance connection electrodes **82** may be not less than 1/20 and not more than ¼ of the length of the plurality of first trench resistive structures **51**A.

[0237] The plurality of second resistance connection electrodes **82** have a second connection area S**2** with respect to the resistive film **60**. The second connection area S**2** is defined by a total plane area of the plurality of second resistance connection electrodes **82**. When a single second resistance connection electrode **82** is formed, the second connection area S**2** is defined by a plane area of the single second resistance connection electrode **82**.

[0238] The second connection area S**2** may be substantially equal to the first connection area S**1**. The second connection area S**2** may be larger than the first connection area S**1**. The second connection area S**2** may be less than the first connection area S**1**. The second connection area S**2** is adjusted according to a current ratio I**2**/I**1** (shunt ratio) of a second current I**2** flowing through the second resistance connection electrodes **82** to the first current I**1** flowing through the first resistance connection electrodes **81** (see FIG. **12**).

[0239] In this case, a value of an area ratio S**2**/S**1** of the second connection area S**2** to the first connection area S**1** is preferably set to be not less than the value of the current ratio I**2**/I**1**. For example, when the current ratio I**2**/I**1** is 1, the area ratio S**2**/S**1** is preferably set to not less than 1. For example, when the current ratio I**2**/I**1** is ½, the area ratio S**2**/S**1** is preferably set to not less than ½.

[0240] When the current ratio I**2**/I**1** is ¼, the area ratio S**2**/S**1** is preferably set to not less than ¼. In this embodiment, the current ratio I**2**/I**1** is substantially ½, and the second connection area S**2** is not less than ½ times the first connection area S**1**. The second connection area S**2** is preferably not more than twice the first connection area S**1**.

[0241] With reference to FIG. **11** to FIG. **22**, the semiconductor device **1**A includes at least one (in this embodiment, a plurality) of third resistance connection electrodes **83** embedded in the interlayer insulating film **74** such as to be electrically connected to the resistive film **60** at a location different from the first resistance connection electrodes **81** and the second resistance connection electrodes **82**. The third resistance connection electrodes **83** may be referred to as “third resistance via electrodes.”

[0242] Each third resistance connection electrode **83** may include at least one type among a Ti film, a TiN film, a W film, an Al film, a Cu film, an Al alloy film, a Cu alloy film, and a conductive

polysilicon film. In this embodiment, the third resistance connection electrode **83** has a laminated structure including a Ti film and a W film.

[0243] In this embodiment, the plurality of third resistance connection electrodes **83** are connected to the third covering portion **63** of the resistive film **60**. That is, the plurality of third resistance connection electrodes **83** are embedded in a portion of the resistive film **60** covering the second trench group **53** (the plurality of second trench resistive structures **51**B).

[0244] The plurality of third resistance connection electrodes **83**, with the plurality of first resistance connection electrodes **81**, form a second gate resistance R**2**. The second gate resistance R**2** is constituted of a portion of the resistive film **60** and the plurality of second trench resistive structures **51**B that is positioned in a region between the plurality of first resistance connection electrodes **81** and the plurality of third resistance connection electrodes **83**.

[0245] A resistance value of the second gate resistance R**2** is adjusted by a distance between the plurality of first resistance connection electrodes **81** and the plurality of third resistance connection electrodes **83**. In this embodiment, the resistance value of the second gate resistance R**2** is substantially equal to the resistance value of the first gate resistance R**1**. Also, the distance between the plurality of first resistance connection electrodes **81** and the plurality of third resistance connection electrodes **83** is substantially equal to the distance between the plurality of first resistance connection electrodes **81** and the plurality of second resistance connection electrodes **82**.

[0246] As a matter of course, the resistance value of the second gate resistance R**2** may be different from the resistance value of the first gate resistance R**1**. In this case, the distance between the plurality of first resistance connection electrodes **81** and the plurality of third resistance connection electrodes **83** may be different from the distance between the plurality of first resistance connection electrodes **81** and the plurality of second resistance connection electrodes **82**.

[0247] For example, the resistance value of the second gate resistance R**2** may be less than the resistance value of the first gate resistance R**1**. In this case, the distance between the plurality of first resistance connection electrodes **81** and the plurality of third resistance connection electrodes **83** may be set to be less than the distance between the plurality of first resistance connection electrodes **81** and the plurality of second resistance connection electrodes **82**.

[0248] For example, the resistance value of the second gate resistance R**2** may be larger than the resistance value of the first gate resistance R**1**. In this case, the distance between the plurality of first resistance connection electrodes **81** and the plurality of third resistance connection electrodes **83** may be set to be larger than the distance between the plurality of first resistance connection electrodes **81** and the plurality of second resistance connection electrodes **82**.

[0249] The plurality of third resistance connection electrodes **83** are formed in regions facing the plurality of second trench resistive structures **51**B in the first direction X in plan view. In this embodiment, the plurality of third resistance connection electrodes **83** extend in a different direction from the first resistance connection electrodes **81** in plan view. Specifically, the plurality of third resistance connection electrodes **83** are each formed in a band shape extending in the second direction Y in plan view and are aligned at intervals in the first direction X. That is, the plurality of third resistance connection electrodes **83** are aligned in a stripe shape extending in the second direction Y in plan view.

[0250] In plan view, the plurality of third resistance connection electrodes **83** are respectively disposed, at intervals from the plurality of second trench resistive structures **51**B, in regions between the plurality of second trench resistive structures **51**B that are mutually adjacent. That is, the plurality of third resistance connection electrodes **83** are aligned alternately with the plurality of second trench resistive structures **51**B in the first direction X.

[0251] Also, in this embodiment, the plurality of third resistance connection electrodes **83** face only the flat portion of the first principal surface **3** with the resistive film **60** interposed therebetween and do not face the trench resistive structure **51** with the resistive film **60** interposed therebetween. The plurality of third resistance connection electrodes **83** face the boundary well region **40** (the first

boundary well region **40**A) with the resistive film **60** and the principal surface insulating film **45** interposed therebetween.

[0252] The plurality of third resistance connection electrodes **83** suffice to be disposed in a part of the regions between the plurality of second trench resistive structures **51**B and do not necessarily have to be disposed in all of the regions between the plurality of second trench resistive structures **51**B. The plurality of third resistance connection electrodes **83** suffice to be disposed in at least one region positioned at the active region **6** side among the regions between the plurality of second trench resistive structures **51**B and do not have to be disposed in at least one region positioned at the gate electrode film **64** side.

[0253] It is preferable that at least one of the plurality of third resistance connection electrodes **83** faces the plurality of first resistance connection electrodes **81** in the second direction Y in plan view. In this case, at least one of the plurality of third resistance connection electrodes **83** that is positioned at the gate electrode film **64** side preferably faces the plurality of first resistance connection electrodes **81** in the second direction Y.

[0254] At least one of the plurality of third resistance connection electrodes **83** that is positioned at the active region **6** side does not have to face the plurality of first resistance connection electrodes **81** in the second direction Y. As a matter of course, all of the third resistance connection electrodes **83** may be disposed such as to face the plurality of first resistance connection electrodes **81** in the second direction Y.

[0255] It is preferable that at least one of the plurality of third resistance connection electrodes **83** faces the plurality of second resistance connection electrodes **82** in the second direction Y in plan view. In this embodiment, the number of the plurality of third resistance connection electrodes **83** is set to be equal to the number of the plurality of second resistance connection electrodes **82**, and all of the third resistance connection electrodes **83** face all of the second resistance connection electrodes **82** in the second direction Y in a one-to-one correspondence. As a matter of course, the number of third resistance connection electrodes **83** may be larger than the number of second resistance connection electrodes **82** or may be smaller than the number of second resistance connection electrodes **82**.

[0256] The plurality of third resistance connection electrodes **83** have a length less than the length of the plurality of second trench resistive structures **51**B in the second direction Y. The plurality of third resistance connection electrodes **83** are preferably disposed in regions at the other end portion side of the plurality of second trench resistive structures **51**B with respect to length direction intermediate portions of the plurality of second trench resistive structures **51**B.

[0257] The length of the plurality of third resistance connection electrodes **83** is preferably not less than 1/100 and not more than ½ of the length of the plurality of second trench resistive structures **51**B. The length of the plurality of third resistance connection electrodes **83** may be not less than 1/20 and not more than ¼ of the length of the plurality of second trench resistive structures **51**B. The length of the third resistance connection electrodes **83** may be substantially equal to the length of the second trench resistive structures **51**B. The length of the third resistance connection electrodes **83** may be larger than the length of the second trench resistive structures **51**B. The length of the third resistance connection electrodes **83** may be smaller than the length of the second trench resistive structures **51**B.

[0258] The plurality of third resistance connection electrodes **83** have a third connection area S**3** with respect to the resistive film **60**. The third connection area S**3** is defined by a total plane area of the plurality of third resistance connection electrodes **83**. When a single third resistance connection electrode **83** is formed, the third connection area S**3** is defined by a plane area of the single third resistance connection electrode **83**. The third connection area S**3** is adjusted according to a current ratio I**3**/I**1** (shunt ratio) of a third current I**3** flowing through the third resistance connection electrodes **83** to the first current I**1** flowing through the first resistance connection electrodes **81** (see FIG. **12**).

[0259] In this case, a value of an area ratio S**3**/S**1** of the third connection area S**3** to the first connection area S**1** is preferably set to be not less than the value of the current ratio I**3**/I**1**. For example, when the current ratio I**3**/I**1** is 1, the area ratio S**3**/S**1** is preferably set to not less than 1. For example, when the current ratio I**3**/I**1** is ½, the area ratio S**3**/S**1** is preferably set to not less than ½.

[0260] When the current ratio I**3**/I**1** is ¼, the area ratio S**3**/S**1** is preferably set to not less than ¼. In this embodiment, since the third current I**3** is substantially equal to the second current I**2** and the current ratio I**3**/I**1** is substantially ½, the third connection area S**3** is set to not less than ½ times the first connection area S**1**. The third connection area S**3** is preferably not more than twice the first connection area S**1**. As a matter of course, the third current I**3** may be larger than the second current I**2** or may be smaller than the second current I**2**.

[0261] With reference to FIG. **3** to FIG. **10**A, the semiconductor device **1**A includes a plurality of gate connection electrodes **84** embedded in the interlayer insulating film **74** such as to be electrically connected to the gate wiring film **65** in the non-active region **7**. The gate connection electrodes **84** may be referred to as "gate via electrodes." The plurality of gate connection electrodes **84** may each include at least one type among a Ti film, a TiN film, a W film, an Al film, a Cu film, an Al alloy film, a Cu alloy film, and a conductive polysilicon film. In this embodiment, each of the plurality of gate connection electrodes **84** has a laminated structure including a Ti film and a W film.

[0262] The plurality of gate connection electrodes **84** include at least one (in this embodiment, a plurality) of first gate connection electrodes **84**A and at least one (in this embodiment, a plurality) of second gate connection electrodes **84**B. The plurality of first gate connection electrodes **84**A are embedded in a portion of the interlayer insulating film **74** covering the second lower wiring portion **67** in the street region **11** and are electrically connected to the second lower wiring portion **67** (see FIG. **7** to FIG. **9**). In this embodiment, the plurality of first gate connection electrodes **84**A are formed at intervals in the second direction Y and are each formed in a band shape extending in the first direction X.

[0263] The plurality of second gate connection electrodes **84**B are embedded in a portion of the interlayer insulating film **74** covering the third lower wiring portion **68** in the outer peripheral region **9** and are electrically connected to the third lower wiring portion **68** (see FIG. **3** to FIG. **6**). In this embodiment, the plurality of second gate connection electrodes **84**B are formed at intervals from an inner edge side toward an outer edge side of the third lower wiring portion **68** and are each formed in a band shape extending along the third lower wiring portion **68**.

[0264] With reference to FIG. **3** and FIG. **4**, the semiconductor device **1**A includes a plurality of first emitter connection electrodes **85** that penetrate through the principal surface insulating film **45** and are embedded in the interlayer insulating film **74** such as to be electrically connected to the plurality of emitter regions **29** in the active region **6**. The first emitter connection electrodes **85** may be referred to as "first emitter via electrodes." The first emitter connection electrodes **85** are an example of a "first connection electrode" in the present disclosure.

[0265] The plurality of first emitter connection electrodes **85** may each include at least one type among a Ti film, a TiN film, a W film, an Al film, a Cu film, an Al alloy film, a Cu alloy film, and a conductive polysilicon film. In this embodiment, each of the plurality of first emitter connection electrodes **85** has a laminated structure including a Ti film and a W film.

[0266] The plurality of first emitter connection electrodes **85** penetrate through the interlayer insulating film **74** and the principal surface insulating film **45** and are respectively embedded in the plurality of contact holes **30**. The plurality of first emitter connection electrodes **85** are respectively formed in band shapes extending in the second direction Y along the plurality of first trench structures **21** in plan view. That is, in this embodiment, the plurality of first emitter connection electrodes **85** extend in the same direction as the extending direction of the plurality of second resistance connection electrodes **82** and the extending direction of the plurality of third resistance

connection electrodes **83**. The plurality of first emitter connection electrodes **85** are each electrically connected to the emitter region **29** and the channel contact region **31** inside the corresponding contact hole **30**.

[0267] With reference to FIG. **3** and FIG. **5**, the semiconductor device **1**A includes a plurality of second emitter connection electrodes **86** that penetrate through the principal surface insulating film **45** and are embedded in the interlayer insulating film **74** such as to be electrically connected to the plurality of emitter electrode films **47** in the active region **6**. The second emitter connection electrodes **86** may be referred to as "second emitter via electrodes."

[0268] The plurality of second emitter connection electrodes **86** may each include at least one type among a Ti film, a TiN film, a W film, an Al film, a Cu film, an Al alloy film, a Cu alloy film, and a conductive polysilicon film. In this embodiment, the plurality of second emitter connection electrodes **86** each have a laminated structure including a Ti film and a W film. The plurality of second emitter connection electrodes **86** are electrically connected to the second embedded electrodes **28** via the plurality of emitter electrode films **47**.

[0269] With reference to FIG. **3** to FIG. **6**, the semiconductor device **1**A includes at least one (in this embodiment, a plurality) of first well connection electrodes **87** that penetrate through the principal surface insulating film **45** and are embedded in the interlayer insulating film **74** such as to be electrically connected to the inner edge of the outer peripheral well region **41**. The first well connection electrodes **87** may be referred to as "first well via electrodes."

[0270] The plurality of first well connection electrodes **87** may each include at least one type among a Ti film, a TiN film, a W film, an Al film, a Cu film, an Al alloy film, a Cu alloy film, and a conductive polysilicon film. In this embodiment, the plurality of first well connection electrodes **87** each have a laminated structure including a Ti film and a W film.

[0271] In this embodiment, the plurality of first well connection electrodes **87** are disposed at intervals to the outer edge side from the inner edge side of the outer peripheral well region **41**. The plurality of first well connection electrodes **87** are disposed at the inner edge side of the outer peripheral well region **41** with respect to a width direction intermediate portion of the outer peripheral well region **41** and are electrically connected to regions at the inner edge side of the outer peripheral well region **41**. Specifically, the plurality of first well connection electrodes **87** are disposed in regions between the inner edge of the outer peripheral well region **41** and the third lower wiring portion **68** of the gate wiring film **65**. Each of the plurality of first well connection electrodes **87** extends in a band shape along the inner edge of the outer peripheral well region **41**.

[0272] Each of the plurality of first well connection electrodes **87** has a plurality of segment portions **87***a* at portions extending in the first direction X (see FIG. **3**). The plurality of segment portions **87***a* are respectively disposed, at intervals from the plurality of lead-out portions **68***a* of the gate wiring film **65** (the third lower wiring portion **68**), in regions between the plurality of lead-out portions **68***a*. When the single lead-out portion **68***a* extending in the band shape is formed along each trench separation structure **15**, the plurality of segment portions **87***a* are omitted.

[0273] With reference to FIG. **3** to FIG. **6**, the semiconductor device **1**A includes at least one (in this embodiment, a plurality) of second well connection electrodes **88** that penetrate through the principal surface insulating film **45** and are embedded in the interlayer insulating film **74** such as to be electrically connected to the outer edge of the outer peripheral well region **41**. The second well connection electrodes **88** may be referred to as "second well via electrodes."

[0274] The plurality of second well connection electrodes **88** may each include at least one type among a Ti film, a TiN film, a W film, an Al film, a Cu film, an Al alloy film, a Cu alloy film, and a conductive polysilicon film. In this embodiment, the plurality of second well connection electrodes **88** each have a laminated structure including a Ti film and a W film.

[0275] The plurality of second well connection electrodes **88** are disposed at intervals to the outer edge side from the inner edge side of the outer peripheral well region **41**. The plurality of second well connection electrodes **88** are disposed at the outer edge side of the outer peripheral well region

41 with respect to the width direction intermediate portion of the outer peripheral well region **41** and are electrically connected to regions at the outer edge side of the outer peripheral well region **41**. Specifically, the plurality of second well connection electrodes **88** are disposed in regions between the outer edge of the outer peripheral well region **41** and the third lower wiring portion **68** of the gate wiring film **65**. Each of the plurality of second well connection electrodes **88** extends in a band shape along the outer edge of the outer peripheral well region **41**.

[0276] With reference to FIG. **10**C, the semiconductor device **1**A includes, in the outer peripheral region **9**, a plurality of field contact holes **112** that penetrate continuously through the interlayer insulating film **74** and the principal surface insulating film **45** such as to respectively expose the plurality of field contact regions **111**. In this embodiment, two field contact holes **112** are formed per single field region **42**.

[0277] The plurality of field contact holes **112** are each formed in a band shape extending along the corresponding field region **42** in plan view. In this embodiment, the plurality of field contact holes **112** are each formed in an annular shape (quadrangular annular shape) extending along the corresponding field region **42**.

[0278] The semiconductor device **1**A includes at least one (in this embodiment, a plurality) of field connection electrodes **89** each embedded in a field contact hole **112** such as to be electrically connected to the field contact region **111** of the corresponding field region **42**. The field connection electrodes **89** penetrate through the interlayer insulating film **74** and the principal surface insulating film **45** and are electrically connected to the field contact regions **111**.

[0279] In this embodiment, each of the two field contact regions **111** formed in a single field region **42** has a single field connection electrode **89** connected thereto. As a matter of course, a single field contact region **111** may be formed per single field region **42** and a single field connection electrode **89** may be connected to the single field contact region **111** instead. The field connection electrodes **89** may be referred to as “field via electrodes.”

[0280] The plurality of field connection electrodes **89** may each include at least one type among a Ti film, a TiN film, a W film, an Al film, a Cu film, an Al alloy film, a Cu alloy film, and a conductive polysilicon film. In this embodiment, the plurality of field connection electrodes **89** each have a laminated structure including a Ti film and a W film.

[0281] Each of the plurality of field connection electrodes **89** is formed in a band shape extending along the corresponding field region **42**. In this embodiment, each of the plurality of field connection electrodes **89** is formed in an annular shape (quadrangular annular shape) extending along the corresponding field region **42**. In this embodiment, the plurality of field connection electrodes **89** are formed in an electrically floating state.

[0282] With reference to FIG. **10**D, the semiconductor device **1**A includes, in the outer peripheral region **9**, a plurality of channel stop contact holes **123** that penetrate continuously through the interlayer insulating film **74**, the principal surface insulating film **45**, and the second high concentration region **43** such as to respectively expose the plurality of channel stop contact regions **122**. In this embodiment, two channel stop contact holes **123** are formed. The channel stop contact holes **123** are an example of a “second contact hole” in the present disclosure.

[0283] The plurality of channel stop contact holes **123** are each formed in a band shape extending along the second high concentration region **43** in plan view. In this embodiment, the plurality of channel stop contact holes **123** are each formed in an annular shape (quadrangular annular shape) extending along the second high concentration region **43**.

[0284] The semiconductor device **1**A includes at least one (in this embodiment, a plurality) of channel stop connection electrodes **124** embedded in the channel stop contact holes **123** such as to be electrically connected to the channel stop contact regions **122** of the second high concentration region **43**. In this embodiment, each of the two channel stop contact regions **122** has a single channel stop connection electrode **124** connected thereto. As a matter of course, a single channel stop contact region **122** may be formed with respect to the second high concentration region **43** and

a single channel stop connection electrode **124** may be connected to the single channel stop contact region **122** instead. The channel stop connection electrodes **124** may be referred to as "channel stop via electrodes."

[0285] The plurality of channel stop connection electrodes **124** may each include at least one type among a Ti film, a TiN film, a W film, an Al film, a Cu film, an Al alloy film, a Cu alloy film, and a conductive polysilicon film. In this embodiment, the plurality of channel stop connection electrodes **124** each have a laminated structure including a Ti film and a W film.

[0286] Each of the plurality of channel stop connection electrodes **124** is formed in a band shape extending along the second high concentration region **43**. In this embodiment, each of the plurality of channel stop connection electrodes **124** is formed in an annular shape (quadrangular annular shape) extending along the second high concentration region **43**. In this embodiment, the plurality of channel stop connection electrodes **124** are formed in an electrically floating state.

[0287] With reference to FIG. **1** and FIG. **11** to FIG. **22**, the semiconductor device **1**A includes the gate terminal electrode **90** disposed on the first principal surface **3** such as to be electrically connected to the gate resistive structure **50** in the pad region **10** (non-active region **7**). Specifically, the gate terminal electrode **90** is disposed on the interlayer insulating film **74**. The gate terminal electrode **90** may be referred to as a "gate pad" or a "gate pad electrode."

[0288] The gate terminal electrode **90** is preferably constituted of a conductive material different from the resistive film **60**. The gate terminal electrode **90** is preferably constituted of a conductive material different from the gate electrode film **64**. The gate terminal electrode **90** has a lower resistance value than the trench resistive structures **51** and the resistive film **60** and is electrically connected to the trench resistive structures **51** via the resistive film **60**. The gate terminal electrode **90** has a lower resistance value than the gate electrode film **64**.

[0289] In this embodiment, the gate terminal electrode **90** is constituted of a metal film. The gate terminal electrode **90** may also be referred to as a "gate metal terminal." The gate terminal electrode **90** may include at least one type among a Ti film, a TiN film, a W film, an Al film, a Cu film, an Al alloy film, a Cu alloy film, and a conductive polysilicon film.

[0290] The gate terminal electrode **90** may include at least one among a pure Cu film (Cu film having a purity of 99% or more), a pure Al film (Al film having a purity of 99% or more), an AlCu alloy film, an AlSi alloy film, and an AlSiCu alloy film. In this embodiment, the gate terminal electrode **90** has a laminated structure that includes a Ti film and an Al alloy film (in this embodiment, an AlCu alloy film) laminated in that order from the chip **2** side.

[0291] The gate terminal electrode **90** preferably has a thickness larger than the thickness of the resistive film **60** (the thickness of the gate electrode film **64**). The thickness of the gate terminal electrode **90** may be not less than 1 μm and not more than 10 μm. The gate terminal electrode **90** preferably has a plane area of not less than 1% and not more than 30% of the plane area of the first principal surface **3**. The plane area of the gate terminal electrode **90** is particularly preferably not more than 25% of the plane area of the first principal surface **3**. The plane area of the gate terminal electrode **90** may be not more than 10% of the plane area of the first principal surface **3**.

[0292] The gate terminal electrode **90** is disposed on the interlayer insulating film **74** such as to cover the resistive film **60** and the gate electrode film **64** in the pad region **10**. The gate terminal electrode **90** covers the plurality of first resistance connection electrodes **81** in a portion that covers the resistive film **60** and is electrically connected to the plurality of first resistance connection electrodes **81**. That is, the gate terminal electrode **90** is electrically connected to the resistive film **60** (the first covering portion **61**) via the plurality of first resistance connection electrodes **81**.

[0293] With reference to FIG. **11** to FIG. **22** (particularly FIG. **11** to FIG. **13**), the gate terminal electrode **90** includes a first electrode portion **91** and a second electrode portion **92**. The first electrode portion **91** has a comparatively wide electrode width in the second direction Y. The first electrode portion **91** is a portion that forms a terminal main body of the gate terminal electrode **90** and is positioned in a region outside the first resistance connection electrodes **81** in plan view. The

first electrode portion **91** may be referred to as a "terminal main body portion."
[0294] For example, a bonding wire is connected to the first electrode portion **91**. Therefore, the first electrode portion **91** is formed to be wider than a bonding portion of the bonding wire. The first electrode portion **91** is formed in a polygonal shape (in this embodiment, quadrangular shape) having four sides parallel to the peripheral edge of the chip **2** (a peripheral edge of the pad region **10**) in plan view. The first electrode portion **91** is disposed in a region facing the gate electrode film **64** with the interlayer insulating film **74** interposed therebetween.
[0295] The first electrode portion **91** preferably covers not less than 50% of the region of the gate electrode film **64** in plan view. The first electrode portion **91** particularly preferably covers not less than 90% of the region of the gate electrode film **64** in plan view. In this embodiment, the first electrode portion **91** has a wider electrode width than the gate electrode film **64** and covers the entire region of the gate electrode film **64**.
[0296] Flatness of the first electrode portion **91** is enhanced by the gate electrode film **64**. The first electrode portion **91** may be electrically insulated from the gate electrode film **64** by the interlayer insulating film **74**. The first electrode portion **91** may be electrically connected to the gate electrode film **64** via one or a plurality of the gate connection electrodes **84** embedded in the interlayer insulating film **74**.
[0297] The first electrode portion **91** covers the first slit **71** with the interlayer insulating film **74** interposed therebetween and backfills the first recess portion **76** of the interlayer insulating film **74** (the insulating principal surface **75**). When the gate terminal electrode **90** (the first electrode portion **91**) that partially exposes the first recess portion **76** is formed, an electrode residue generated during a step of forming the gate terminal electrode **90** is liable to remain in the first recess portion **76**.
[0298] When the electrode residue is present, the gate terminal electrode **90** (the first electrode portion **91**) is liable to become electrically connected to another electrode via the electrode residue. Therefore, the gate terminal electrode **90** (the first electrode portion **91**) preferably covers an entire region of the first slit **71** with the interlayer insulating film **74** interposed therebetween.
[0299] That is, the gate terminal electrode **90** (the first electrode portion **91**) preferably fills an entire region of the first recess portion **76** of the interlayer insulating film **74** (the insulating principal surface **75**). According to this arrangement, a layout that avoids the problem of electrode residue in the first recess portion **76** is provided. The present disclosure does not exclude an embodiment including the gate terminal electrode **90** (the first electrode portion **91**) that partially exposes the first recess portion **76**.
[0300] The first electrode portion **91** is led out from above the gate electrode film **64** to above the resistive film **60** across the first slit **71** in plan view. In this embodiment, the first electrode portion **91** covers an edge portion of the resistive film **60** with the interlayer insulating film **74** interposed therebetween. Specifically, the first electrode portion **91** covers the edge portion of the resistive film **60** at an interval toward the gate electrode film **64** side with respect to the straight line crossing the center portion of the resistive film **60** in the second direction Y.
[0301] In a portion covering the resistive film **60**, the first electrode portion **91** may cover one or a plurality of the trench resistive structures **51** with the resistive film **60** interposed therebetween. The first electrode portion **91** may cover one or a plurality of the first trench resistive structures **51**A with the resistive film **60** interposed therebetween. The first electrode portion **91** may cover one or a plurality of the second trench resistive structures **51**B with the resistive film **60** interposed therebetween. In this embodiment, the first electrode portion **91** covers one first trench resistive structure **51**A and one second trench resistive structure **51**B with the resistive film **60** interposed therebetween.
[0302] The first electrode portion **91** covers the plurality of third slits **73** with the interlayer insulating film **74** interposed therebetween and backfills the plurality of third recess portions **78** of the interlayer insulating film **74** (the insulating principal surface **75**). When the gate terminal

electrode **90** (the first electrode portion **91**) that partially exposes the plurality of third recess portions **78** is formed, electrode residues generated during the step of forming the gate terminal electrode **90** are liable to remain in the plurality of third recess portions **78**.

[0303] When the electrode residues are present, the gate terminal electrode **90** (the first electrode portion **91**) is liable to become electrically connected to another electrode via the electrode residues. Therefore, the gate terminal electrode **90** (the first electrode portion **91**) preferably covers entire regions of the plurality of third recess portions **78** with the interlayer insulating film **74** interposed therebetween.

[0304] That is, the gate terminal electrode **90** (the first electrode portion **91**) preferably fills the entire regions of the third recess portions **78** of the interlayer insulating film **74** (the insulating principal surface **75**). According to this arrangement, a layout that avoids the problem of electrode residues in the plurality of third recess portions **78** is provided. The present disclosure does not exclude an embodiment including the gate terminal electrode **90** (the first electrode portion **91**) that partially exposes the plurality of third recess portions **78**.

[0305] The first electrode portion **91** is led out from above the gate electrode film **64** to above the plurality of second lower line portions **70**A and **70**B across the plurality of third slits **73** in plan view. In this embodiment, the first electrode portion **91** covers edge portions of the plurality of second lower line portions **70**A and **70**B with the interlayer insulating film **74** interposed therebetween.

[0306] The second electrode portion **92** has a smaller electrode width than the first electrode portion **91** in the second direction Y and is constituted of a lead-out portion led out in the second direction Y such as to protrude from the first electrode portion **91** toward the plurality of first resistance connection electrodes **81**. The second electrode portion **92** may be referred to as a "terminal lead-out portion." For example, a bonding wire is not connected to the second electrode portion **92**. Therefore, the second electrode portion **92** is formed to be narrower than the bonding portion of the bonding wire.

[0307] A protruding direction of the second electrode portion **92** is the same as the extending direction of the plurality of first resistance connection electrodes **81**. In this embodiment, the second electrode portion **92** is led out from a central portion of the first electrode portion **91** and covers all of the first resistance connection electrodes **81**.

[0308] In plan view, the second electrode portion **92** is formed at an interval to the second slit **72** side from the first slit **71** and does not intersect the first slit **71**. Further, in plan view, the second electrode portion **92** is formed at an interval to the first slit **71** side from the second slit **72** and does not intersect the second slit **72**. That is, the second electrode portion **92** has a width smaller than the width of the resistive film **60** in the first direction X and is disposed only in a region directly above the resistive film **60**.

[0309] The second electrode portion **92** faces the space region **57** with the principal surface insulating film **45**, the resistive film **60**, and the interlayer insulating film **74** interposed therebetween. That is, the second electrode portion **92** faces the flat portion of the first principal surface **3** in the thickness direction. Also, the second electrode portion **92** faces the boundary well region **40** (the first boundary well region **40**A) in the thickness direction.

[0310] In regard to the first direction X, the second electrode portion **92** has a width larger than the width of each trench resistive structure **51** in the first direction X. In regard to the second direction Y, the second electrode portion **92** has a width smaller than the length of each trench resistive structure **51** in the second direction Y. In regard to the second direction Y, the second electrode portion **92** preferably has a width smaller than the space width of the space region **57**.

[0311] In this embodiment, the second electrode portion **92** is formed at intervals to the space region **57** side from the other end portions (the first trench group **52**) of the plurality of first trench resistive structures **51**A. Also, in this embodiment, the second electrode portion **92** is formed at intervals to the space region **57** side from the one end portions (the second trench group **53**) of the

plurality of second trench resistive structures **51**B. That is, the second electrode portion **92** faces only the space region **57** in the thickness direction and does not face the plurality of trench resistive structures **51** in the thickness direction.

[0312] As a matter of course, the second electrode portion **92** may face the other end portions (the first trench group **52**) of the plurality of first trench resistive structures **51**A in the thickness direction. Also, the second electrode portion **92** may face the one end portions (the second trench group **53**) of the plurality of second trench resistive structures **51**B in the thickness direction. In view of the flatness of the second electrode portion **92**, the second electrode portion **92** is preferably formed in a region outside the plurality of trench resistive structures **51** at intervals from the plurality of trench resistive structures **51** in plan view.

[0313] With reference to FIG. **11** to FIG. **23**, the semiconductor device **1**A includes the gate wiring electrode **93** disposed on the first principal surface **3** such as to be electrically connected to the gate resistive structure **50** in the pad region **10** (non-active region **7**). Specifically, the gate wiring electrode **93** is disposed on the interlayer insulating film **74**. The gate wiring electrode **93** may be referred to as a "gate finger" or a "gate finger electrode." The gate terminal electrode **90** and the gate wiring electrode **93** are an example of a "gate electrode" in the present disclosure.

[0314] The gate wiring electrode **93** is preferably constituted of a conductive material different from the resistive film **60**. The gate wiring electrode **93** is preferably constituted of a conductive material different from the gate wiring film **65**. The gate wiring electrode **93** has a lower resistance value than the trench resistive structure **51** and the resistive film **60** and is electrically connected to the gate terminal electrode **90** via the trench resistive structure **51** and the resistive film **60**. The gate wiring electrode **93** has a lower resistance value than the gate wiring film **65**.

[0315] In this embodiment, the gate wiring electrode **93** is constituted of a metal film. The gate wiring electrode **93** may be referred to as a "gate metal wiring." The gate wiring electrode **93** may include at least one type among a Ti film, a TiN film, a W film, an Al film, a Cu film, an Al alloy film, a Cu alloy film, and a conductive polysilicon film.

[0316] The gate wiring electrode **93** may include at least one among a pure Cu film, a pure Al film, an AlCu alloy film, an AlSi alloy film, and an AlSiCu alloy film. In this embodiment, the gate wiring electrode **93** has a laminated structure that includes a Ti film and an Al alloy film (in this embodiment, an AlCu alloy film) laminated in that order from the chip **2** side. That is, the gate wiring electrode **93** has the same electrode constitution as the gate terminal electrode **90**.

[0317] The gate wiring electrode **93** preferably has a thickness larger than the thickness of the resistive film **60** (the thickness of the gate wiring film **65**). The thickness of the gate wiring electrode **93** may be not less than 1 μm and not more than 10 μm. The thickness of the gate wiring electrode **93** is preferably substantially equal to the thickness of the gate terminal electrode **90**.

[0318] The gate wiring electrode **93** is routed in a region between the active region **6** and the non-active region **7**, is electrically connected to the first trench structures **21** (trench separation structures **15**) in the active region **6**, and is electrically connected to the resistive film **60** in the non-active region **7**. Specifically, the gate wiring electrode **93** is electrically connected to the first end portion **60**A and the second end portion **60**B of the resistive film **60** via the gate wiring film **65**.

[0319] That is, the gate wiring electrode **93** forms, between itself and the gate terminal electrode **90**, a parallel resistance circuit PR that includes the first gate resistance R**1** and the second gate resistance R**2** (see also FIG. **24**). The parallel resistance circuit PR constitutes the gate resistance RG interposed between the gate terminal electrode **90** and the gate wiring electrode **93**. The parallel resistance circuit PR is also established between the gate electrode film **64** and the gate wiring film **65**. A resistance value of the gate resistance RG (the parallel resistance circuit PR) is calculated by a combined resistance (=(R**1**+R**2**)/R**1**.Math.R**2**) of the first gate resistance R**1** and the second gate resistance R**2**.

[0320] In this embodiment, the gate wiring electrode **93** includes a first upper wiring portion **94**, a second upper wiring portion **95**, and a third upper wiring portion **96**. The first upper wiring portion

94 is disposed in the pad region **10** such as to surround the gate terminal electrode **90** from a plurality of directions (in this embodiment, three directions), and is disposed on the first lower wiring portion **66** of the gate wiring film **65** with the interlayer insulating film **74** interposed therebetween.

[0321] The first upper wiring portion **94** includes a first upper line portion **97** and a plurality of second upper line portions **98**A and **98**B. In the pad region **10**, the first upper line portion **97** is disposed in a region covering the first lower line portion **69** of the gate wiring film **65** with the interlayer insulating film **74** interposed therebetween and is formed in a band shape extending in the second direction Y.

[0322] The first upper line portion **97** has one end portion at one side (the first side surface **5**A side) in the second direction Y and another end portion at another side (the second side surface **5**B side) in the second direction Y. The first upper line portion **97** covers the second slit **72** with the interlayer insulating film **74** interposed therebetween and backfills the second recess portion **77** of the interlayer insulating film **74** (the insulating principal surface **75**).

[0323] When the gate terminal electrode **90** (the first electrode portion **91** and/or the second electrode portion **92**) that intersects the second recess portion **77** and the gate wiring electrode **93** (the first upper line portion **97**) that partially exposes the second recess portion **77** are formed, an electrode residue generated during the step of forming the gate terminal electrode **90** is liable to remain in the second recess portion **77**.

[0324] When the electrode residue is present, the gate wiring electrode **93** (the first upper line portion **97**) is liable to become electrically connected to the gate terminal electrode **90** via the electrode residue. In this case, the gate wiring electrode **93** (the first upper line portion **97**), together with the gate terminal electrode **90** (the first electrode portion **91**), forms a short circuit without interposition of the gate resistive structure **50**. Therefore, the gate wiring electrode **93** (the first upper line portion **97**) preferably covers an entire region of the second slit **72** with the interlayer insulating film **74** interposed therebetween.

[0325] That is, the gate wiring electrode **93** (the first upper line portion **97**) preferably fills an entire region of the second recess portion **77** of the interlayer insulating film **74** (the insulating principal surface **75**). According to this arrangement, a layout that avoids the problem of electrode residue in the second recess portion **77** is provided. The present disclosure does not exclude an embodiment including the gate terminal electrode **90** (the first electrode portion **91** and/or the second electrode portion **92**) that intersects the second recess portion **77** and the gate wiring electrode **93** (the first upper line portion **97**) that partially exposes the second recess portion **77**.

[0326] The first upper line portion **97** is led out from above the gate wiring film **65** (the first lower line portion **69**) to above the resistive film **60** across the second slit **72** in plan view. The first upper line portion **97** covers an edge portion of the resistive film **60** with the interlayer insulating film **74** interposed therebetween. The first upper line portion **97** may further cross the straight line crossing the center portion of the resistive film **60** in the second direction Y to cover a portion of the resistive film **60** positioned in a region at the gate electrode film **64** side with respect to the straight line.

[0327] The first upper line portion **97** is formed at intervals from the first electrode portion **91** and the second electrode portion **92** of the gate terminal electrode **90** in the first direction X. In this embodiment, the first upper line portion **97** has, in a portion along the second electrode portion **92** of the gate terminal electrode **90**, a recess portion **97***a* recessed in the first direction X along the second electrode portion **92**.

[0328] The first upper line portion **97** includes a first connection region **101** and a second connection region **102**. The first connection region **101** is formed in a region at one side (the first side surface **5**A side) in the second direction Y with respect to the recess portion **97***a* and faces the second electrode portion **92** in the second direction Y. The first connection region **101** covers the second covering portion **62** of the resistive film **60** with the interlayer insulating film **74** interposed

therebetween. That is, the first connection region **101** covers the first trench group **52** (the plurality of first trench resistive structures **51**A) with the interlayer insulating film **74** and the second covering portion **62** of the resistive film **60** interposed therebetween.

[0329] The first connection region **101** further covers the plurality of second resistance connection electrodes **82** and is electrically connected to the plurality of second resistance connection electrodes **82**. The first connection region **101** is thereby electrically connected to the second covering portion **62** of the resistive film **60** and the first trench group **52** (the plurality of first trench resistive structures **51**A) via the plurality of second resistance connection electrodes **82**.

[0330] The first connection region **101** suffices to cover one or a plurality of the first trench resistive structures **51**A mutually adjacent to one or a plurality of the second resistance connection electrodes **82** and does not have to cover all of the first trench resistive structures **51**A. As a matter of course, the first connection region **101** may cover all of the first trench resistive structures **51**A.

[0331] The second connection region **102** is formed in a region at the other side (the second side surface **5**B side) in the second direction Y with respect to the recess portion **97***a* and faces the second electrode portion **92** in the second direction Y. The second connection region **102** covers the third covering portion **63** of the resistive film **60** with the interlayer insulating film **74** interposed therebetween. That is, the second connection region **102** covers the second trench group **53** (the plurality of second trench resistive structures **51**B) with the interlayer insulating film **74** and the third covering portion **63** of the resistive film **60** interposed therebetween.

[0332] The second connection region **102** further covers the plurality of third resistance connection electrodes **83** and is electrically connected to the plurality of third resistance connection electrodes **83**. The second connection region **102** is thereby electrically connected to the third covering portion **63** of the resistive film **60** and the second trench group **53** (the plurality of second trench resistive structures **51**B) via the plurality of third resistance connection electrodes **83**.

[0333] The second connection region **102** suffices to cover one or a plurality of the second trench resistive structures **51**B mutually adjacent to one or a plurality of the third resistance connection electrodes **83** and does not have to cover all of the second trench resistive structures **51**B. As a matter of course, the second connection region **102** may cover all of the second trench resistive structures **51**B.

[0334] A facing area of the gate wiring electrode **93** (the first upper line portion **97**) with respect to the resistive film **60** is preferably larger than a facing area of the gate terminal electrode **90** (the first electrode portion **91** and the second electrode portion **92**) with respect to the resistive film **60**. As a matter of course, the facing area of the gate wiring electrode **93** may be smaller than the facing area of the gate terminal electrode **90**.

[0335] When the gate terminal electrode **90** (the first electrode portion **91**) that partially exposes the first recess portion **76** and the first upper line portion **97** that intersects the first recess portion **76** are formed, an electrode residue generated during the step of forming the gate terminal electrode **90** is liable to remain in the first recess portion **76**.

[0336] When the electrode residue is present, the gate wiring electrode **93** (the first upper line portion **97**) is liable to become electrically connected to the gate terminal electrode **90** (the first electrode portion **91**) via the electrode residue. In this case, the gate wiring electrode **93** (the first upper line portion **97**), together with the gate terminal electrode **90** (the first electrode portion **91**), forms a short circuit without interposition of the gate resistive structure **50**.

[0337] Therefore, it is preferable that, in plan view, the first upper line portion **97** is formed at an interval to the second recess portion **77** (the second slit **72**) side from the first recess portion **76** (the first slit **71**) and does not intersect the first recess portion **76** (the first slit **71**). In this embodiment, the gate terminal electrode **90** (the first electrode portion **91**) covers the entire region of the first recess portion **76**.

[0338] That is, in a region above the resistive film **60**, the first upper line portion **97** faces the first electrode portion **91** and the second electrode portion **92** of the gate terminal electrode **90** in the

first direction X. According to this arrangement, a layout that avoids the problem of electrode residue in the first recess portion **76** is provided. The present disclosure does not exclude an embodiment including the gate terminal electrode **90** (the first electrode portion **91**) that partially exposes the first recess portion **76** and the first upper line portion **97** that intersects the first recess portion **76**.

[0339] The first current I**1** applied to the gate terminal electrode **90** (the second electrode portion **92**) is transmitted to the first covering portion **61** of the resistive film **60** via the plurality of first resistance connection electrodes **81**. The first current I**1** transmitted to the first covering portion **61** is divided into the second current I**2** at the second covering portion **62** (the first trench group **52**) side of the resistive film **60** and the third current I**3** at the third covering portion **63** (the second trench group **53**) side of the resistive film **60**.

[0340] The second current I**2** is transmitted to the first connection region **101** of the first upper line portion **97** via the plurality of second resistance connection electrodes **82**, and the third current I**3** is transmitted to the second connection region **102** of the first upper line portion **97** via the plurality of third resistance connection electrodes **83**. Thus, the gate wiring electrode **93** (the first upper line portion **97**) forms, between itself and the gate terminal electrode **90** (the second electrode portion **92**), the parallel resistance circuit PR that includes the first gate resistance R**1** and the second gate resistance R**2** (see also FIG. **24**).

[0341] The plurality of second upper line portions **98**A and **98**B include the second upper line portion **98**A at one side and the second upper line portion **98**B at the other side. In the pad region **10**, the second upper line portion **98**A is disposed in a region at one side (the first side surface **5**A side) in the second direction Y with respect to the gate terminal electrode **90**. In the pad region **10**, the second upper line portion **98**B is disposed in a region at the other side (the second side surface **5**B side) in the second direction Y with respect to the gate terminal electrode **90**.

[0342] The second upper line portion **98**A is formed in a band shape extending in the first direction X and has one end portion connected to the one end portion of the first upper line portion **97** and another end portion positioned at the peripheral edge side (the third side surface **5**C side) of the chip **2**. The second upper line portion **98**A covers the second lower line portion **70**A of the gate wiring film **65** with the interlayer insulating film **74** interposed therebetween. The second upper line portion **98**A is formed at an interval to one side in the second direction Y from the first electrode portion **91** of the gate terminal electrode **90**.

[0343] The second upper line portion **98**B is formed in a band shape extending in the first direction X and has one end portion connected to the other end portion of the first upper line portion **97** and another end portion positioned at the peripheral edge side (the third side surface **5**C side) of the chip **2**. The second upper line portion **98**B covers the second lower line portion **70**B of the gate wiring film **65** with the interlayer insulating film **74** interposed therebetween. The second upper line portion **98**B is formed at an interval to the other side in the second direction Y from the first electrode portion **91** of the gate terminal electrode **90** and faces the second upper line portion **98**A with the first electrode portion **91** interposed therebetween.

[0344] When the gate terminal electrode **90** (the first electrode portion **91**) that partially exposes the first recess portion **76** and the second upper line portions **98**A and **98**B that intersect the first recess portion **76** are formed, an electrode residue generated during the step of forming the gate terminal electrode **90** is liable to remain in the first recess portion **76**. When the electrode residue is present, the gate wiring electrode **93** (the second upper line portions **98**A and **98**B) is liable to become electrically connected to the gate terminal electrode **90** (the first electrode portion **91**) via the electrode residue.

[0345] In this case, the gate wiring electrode **93** (the second upper line portions **98**A and **98**B), together with the gate terminal electrode **90** (the first electrode portion **91**), forms a short circuit without interposition of the gate resistive structure **50**. Therefore, it is preferable that the second upper line portions **98**A and **98**B are disposed at intervals from the first recess portion **76** and do

not have a portion that covers the first recess portion **76** (a portion intersecting the first recess portion **76**).

[0346] According to this arrangement, a layout that avoids the problem of electrode residue in the first recess portion **76** is provided. The present disclosure does not exclude an embodiment including the gate terminal electrode **90** (the first electrode portion **91**) that partially exposes the first recess portion **76** and the second upper line portions **98**A and **98**B that intersect the first recess portion **76**. Also, when the gate terminal electrode **90** (the first electrode portion **91**) that partially exposes the plurality of third recess portions **78** and the second upper line portions **98**A and **98**B that intersect the plurality of third recess portions **78** are formed, electrode residues generated during the step of forming the gate terminal electrode **90** are liable to remain in the plurality of third recess portions **78**. In this case, the gate wiring electrode **93** (the second upper line portions **98**A and **98**B), together with the gate terminal electrode **90** (the first electrode portion **91**), forms a short circuit without interposition of the gate resistive structure **50**.

[0347] Therefore, it is preferable that the second upper line portions **98**A and **98**B are disposed at intervals from the plurality of third recess portions **78** and do not have a portion that covers the plurality of third recess portions **78** (a portion that intersects the plurality of third recess portions **78**). According to this arrangement, a layout that avoids the problem of electrode residues in the plurality of third recess portions **78** is provided. In this embodiment, the gate terminal electrode **90** (the first electrode portion **91**) covers the entire regions of the plurality of third recess portions **78**.

[0348] That is, in regions above the second lower line portions **70**A and **70**B, the second upper line portions **98**A and **98**B face the first electrode portion **91** of the gate terminal electrode **90** in the second direction Y. The present disclosure does not exclude an embodiment including the gate terminal electrode **90** (the first electrode portion **91**) that partially exposes the plurality of third recess portions **78** and the second upper line portions **98**A and **98**B that intersect the plurality of third recess portions **78**.

[0349] The second upper line portions **98**A and **98**B preferably cover inner portions of the second lower line portions **70**A and **70**B at intervals from peripheral edges of the second lower line portions **70**A and **70**B in plan view. That is, it is preferable that the second upper line portions **98**A and **98**B face only the second lower line portions **70**A and **70**B with the interlayer insulating film **74** interposed therebetween and do not face the principal surface insulating film **45** with the interlayer insulating film **74** interposed therebetween.

[0350] The second upper wiring portion **95** is led out from the first upper wiring portion **94** to the street region **11** and covers the second lower wiring portion **67** of the gate wiring film **65** with the interlayer insulating film **74** interposed therebetween. Specifically, the second upper wiring portion **95** is led out from an inner portion (in this embodiment, a central portion) of the first upper line portion **97** and is formed in a band shape extending in the first direction X.

[0351] In this embodiment, the second upper wiring portion **95** crosses the center of the chip **2**. The second upper wiring portion **95** extends in a band shape such as to be positioned in a region at one side (the third side surface **5**C side) and a region at the other side (the fourth side surface **5**D side) in the first direction X with respect to the straight line crossing the center of the first principal surface **3** in the second direction Y. The second upper wiring portion **95** has one end portion connected to the first upper wiring portion **94** at one side in the first direction X and another end portion at the other side in the first direction X. In this embodiment, the other end portion of the second upper wiring portion **95** is constituted of an open end.

[0352] The second upper wiring portion **95** covers the plurality of first gate connection electrodes **84**A and is electrically connected to the second lower wiring portion **67** via the plurality of first gate connection electrodes **84**A. The second upper wiring portion **95** has a width smaller than the width of the street region **11** in the second direction Y and is formed at intervals inward of the street region **11** from the plurality of active regions **6**. That is, the second upper wiring portion **95** is formed at intervals from the plurality of trench separation structures **15** (the plurality of first trench

structures **21**) in plan view.
[0353] The third upper wiring portion **96** is led out from the first upper wiring portion **94** to the outer peripheral region **9** and covers the third lower wiring portion **68** of the gate wiring film **65** with the interlayer insulating film **74** interposed therebetween. Specifically, the third upper wiring portion **96** is led out from the other end portions of the plurality of second upper line portions **98**A and **98**B to one side (the first side surface **5**A side) and the other side (the second side surface **5**B side) of the outer peripheral region **9** and is formed in a band shape extending along the outer peripheral region **9**.
[0354] The third upper wiring portion **96**, together with the second upper wiring portion **95**, sandwiches the plurality of active regions **6**. Specifically, the third upper wiring portion **96** extends along the peripheral edge (the first side surfaces **5**A to **5**D) of the chip **2** such as to surround the plurality of active regions **6** in plan view. Thereby, the third upper wiring portion **96**, together with the second upper wiring portion **95**, surrounds the plurality of active regions **6**. In this embodiment, the third upper wiring portion **96** is formed at an interval from the second upper wiring portion **95**. The third upper wiring portion **96** may be connected to the second upper wiring portion **95**.
[0355] The third upper wiring portion **96** covers the plurality of second gate connection electrodes **84**B and is electrically connected to the third lower wiring portion **68** via the plurality of second gate connection electrodes **84**B. The third upper wiring portion **96** preferably has a width smaller than the width of the third lower wiring portion **68** in plan view. The third upper wiring portion **96** preferably covers the inner portion of the third lower wiring portion **68** at an interval from the peripheral edge of the third lower wiring portion **68** in plan view.
[0356] With reference to FIG. **1** and FIG. **11** to FIG. **22**, the semiconductor device **1**A includes, in the active regions **6**, an emitter terminal electrode **103** disposed on the first principal surface **3** at intervals from the gate terminal electrode **90** and the gate wiring electrode **93**. Specifically, the emitter terminal electrode **103** is disposed on the interlayer insulating film **74**. The emitter terminal electrode **103** may be referred to as an “emitter pad” or an “emitter pad electrode.” The emitter terminal electrode **103** is preferably constituted of a conductive material different from the resistive film **60**. The emitter terminal electrode **103** is preferably constituted of a conductive material different from the emitter electrode film **47**.
[0357] The emitter terminal electrode **103** has a lower resistance value than the trench resistive structures **51** and the resistive film **60**. In this embodiment, the emitter terminal electrode **103** is constituted of a metal film. The emitter terminal electrode **103** may be referred to as an “emitter metal terminal.” The emitter terminal electrode **103** may include at least one type among a Ti film, a TiN film, a W film, an Al film, a Cu film, an Al alloy film, a Cu alloy film, and a conductive polysilicon film.
[0358] The emitter terminal electrode **103** may include at least one among a pure Cu film, a pure Al film, an AlCu alloy film, an AlSi alloy film, and an AlSiCu alloy film. In this embodiment, the emitter terminal electrode **103** has a laminated structure that includes a Ti film and an Al alloy film (in this embodiment, an AlCu alloy film) laminated in that order from the chip **2** side. That is, the emitter terminal electrode **103** has the same electrode constitution as the gate terminal electrode **90**.
[0359] The emitter terminal electrode **103** preferably has a thickness larger than the thickness of the resistive film **60** (the thickness of the gate electrode film **64**). The thickness of the emitter terminal electrode **103** may be not less than 1 μm and not more than 10 μm. The thickness of the emitter terminal electrode **103** is preferably substantially equal to the thickness of the gate terminal electrode **90**.
[0360] The emitter terminal electrode **103** has a plane area larger than the plane area of the gate terminal electrode **90**. The plane area of the emitter terminal electrode **103** is preferably not less than 50% and not more than 90% of the plane area of the first principal surface **3**. The plane area of the emitter terminal electrode **103** is particularly preferably not less than 70% or more of the plane area of the first principal surface **3**.

[0361] In this embodiment, the emitter terminal electrode **103** includes a first emitter terminal electrode **103**A and a second emitter terminal electrode **103**B. The first emitter terminal electrode **103**A is disposed in a region, between the second upper wiring portion **95** and the third upper wiring portion **96**, on a portion of the interlayer insulating film **74** covering the first active region **6**A. The first emitter terminal electrode **103**A is led out from the first active region **6**A to the outer peripheral region **9** in plan view.

[0362] The first emitter terminal electrode **103**A covers the plurality of first emitter connection electrodes **85** and the plurality of second emitter connection electrodes **86** in the first active region **6**A and covers the plurality of first well connection electrodes **87** in the outer peripheral region **9**. The first emitter terminal electrode **103**A is electrically connected to the plurality of second trench structures **25**, the plurality of emitter regions **29**, and the plurality of channel contact regions **31** via the plurality of first emitter connection electrodes **85** and the plurality of second emitter connection electrodes **86**. The first emitter terminal electrode **103**A is electrically connected to an inner edge portion of the outer peripheral well region **41** via the plurality of first well connection electrodes **87**.

[0363] The second emitter terminal electrode **103**B is disposed in a region, between the second upper wiring portion **95** and the third upper wiring portion **96**, on a portion of the interlayer insulating film **74** covering the second active region **6**B. The second emitter terminal electrode **103**B is led out from the second active region **6**B to the outer peripheral region **9** in plan view.

[0364] The second emitter terminal electrode **103**B covers the plurality of first emitter connection electrodes **85** and the plurality of second emitter connection electrodes **86** in the second active region **6**B and covers the plurality of first well connection electrodes **87** in the outer peripheral region **9**. The second emitter terminal electrode **103**B is electrically connected to the plurality of second trench structures **25**, the plurality of emitter regions **29**, and the plurality of channel contact regions **31** via the plurality of first emitter connection electrodes **85** and the plurality of second emitter connection electrodes **86**. The second emitter terminal electrode **103**B is electrically connected to an inner edge portion of the outer peripheral well region **41** via the plurality of first well connection electrodes **87**.

[0365] The semiconductor device **1**A includes an emitter wiring electrode **104** that, on the interlayer insulating film **74**, is led out from the emitter terminal electrode **103** to a region outside the gate wiring electrode **93**. The emitter wiring electrode **104** may be referred to as an “emitter finger” or an “emitter finger electrode.” The emitter wiring electrode **104** is preferably constituted of a conductive material different from the resistive film **60**. The emitter wiring electrode **104** is preferably constituted of a conductive material different from the emitter electrode film **47**. The emitter terminal electrode **103** and the emitter wiring electrode **104** are an example of a “first main electrode” in the present disclosure.

[0366] The emitter wiring electrode **104** has a lower resistance value than the trench resistive structures **51** and the resistive film **60**. In this embodiment, the emitter wiring electrode **104** is constituted of a metal film. The emitter wiring electrode **104** may be referred to as an “emitter metal wiring.” The emitter wiring electrode **104** may include at least one type among a Ti film, a TiN film, a W film, an Al film, a Cu film, an Al alloy film, a Cu alloy film, and a conductive polysilicon film.

[0367] The emitter wiring electrode **104** may include at least one among a pure Cu film, a pure Al film, an AlCu alloy film, an AlSi alloy film, and an AlSiCu alloy film. In this embodiment, the emitter wiring electrode **104** has a laminated structure that includes a Ti film and an Al alloy film (in this embodiment, an AlCu alloy film) laminated in that order from the chip **2** side. That is, the emitter wiring electrode **104** has the same electrode constitution as the emitter terminal electrode **103**.

[0368] The emitter wiring electrode **104** preferably has a thickness larger than the thickness of the resistive film **60** (the thickness of the gate electrode film **64**). The thickness of the emitter wiring

electrode **104** may be not less than 1 μm and not more than 10 μm or less. The thickness of the emitter wiring electrode **104** is preferably substantially equal to the thickness of the gate terminal electrode **90** (the emitter terminal electrode **103**).

[0369] The emitter wiring electrode **104** is connected to both the first emitter terminal electrode **103**A and the second emitter terminal electrode **103**B and is led out to a region further outward than the gate wiring electrode **93** (the third upper wiring portion **96**) from the first emitter terminal electrode **103**A and the second emitter terminal electrode **103**B.

[0370] The emitter wiring electrode **104** is formed in a band shape extending along the peripheral edge of the chip **2** such as to surround the gate terminal electrode **90**, the gate wiring electrode **93**, the first emitter terminal electrode **103**A, and the second emitter terminal electrode **103**B. In this embodiment, the emitter wiring electrode **104** is formed in an annular shape (specifically, a quadrangular annular shape) extending along the peripheral edge (the first to fourth side surfaces **5**A to **5**D) of the chip **2** and surrounds the gate terminal electrode **90**, the gate wiring electrode **93**, the first emitter terminal electrode **103**A, and the second emitter terminal electrode **103**B entirely.

[0371] The emitter wiring electrode **104** is routed in a portion of the interlayer insulating film **74** covering an outer edge portion of the outer peripheral well region **41**. The emitter wiring electrode **104** covers the plurality of second well connection electrodes **88** and is electrically connected to the outer edge portion of the outer peripheral well region **41** via the plurality of second well connection electrodes **88**.

[0372] With reference to FIG. **10**A to FIG. **10**C, the semiconductor device **1**A includes, in the outer peripheral region **9**, a plurality of field electrodes **105** disposed on the interlayer insulating film **74**. The plurality of field electrodes **105** may include at least one type among a Ti film, a TiN film, a W film, an Al film, a Cu film, an Al alloy film, a Cu alloy film, and a conductive polysilicon film.

[0373] The plurality of field electrodes **105** may include at least one among a pure Cu film, a pure Al film, an AlCu alloy film, an AlSi alloy film, and an AlSiCu alloy film. As shown FIG. **10**C, in this embodiment, the plurality of field electrodes **105** each have a laminated structure that includes a barrier metal film **105**A and a main metal film **105**B laminated in that order from the chip **2** side . . .

[0374] The barrier metal film **105**A is constituted, for example, of a laminated film that includes a Ti film and a TiN film that are laminated in that order from the chip **2** side. The main metal film **105**B is constituted, for example, of an Al alloy film (in this embodiment, an AlCu alloy film).

[0375] The plurality of field electrodes **105** covers the corresponding field regions **42** in a one-to-one correspondence. Each field electrodes **105** covers the corresponding plurality of field connection electrodes **89** entirely. The field electrodes **105** are each electrically connected to the corresponding field region **42** via the corresponding plurality of corresponding field connection electrodes **89**. The plurality of field electrodes **105** are formed in an electrically floating state.

[0376] The plurality of field electrodes **105** are each formed in a band shape extending along the corresponding field region **42**. In this embodiment, the plurality of field electrodes **105** are each formed in an annular shape (quadrangular annular shape) extending along the corresponding field region **42**. In this embodiment, the outermost field electrode **105** includes a field lead-out portion **105***a* led out toward the peripheral edge side of the chip **2** and is formed to be wider than the other field electrodes **105**. As a matter of course, the outermost field electrode **105** may have the same width as the other field electrodes **105**.

[0377] With reference to FIG. **10**B and FIG. **10**D, the semiconductor device **1**A includes, in the outer peripheral region **9**, a field plate **141** disposed between the principal surface insulating film **45** with the third field insulating film **133** and the interlayer insulating film **74**. The field plate **141** may include a conductive polysilicon film.

[0378] In plan view, the field plate **141** is selectively disposed in a region between the outermost field electrode **105** and the innermost channel stop connection electrode **124**. In this embodiment, the field plate **141** is disposed such as to cover an outer peripheral edge portion of the third field

insulating film **133** and an in-between portion of the principal surface insulating film **45** from the outer peripheral edge of the third field insulating film **133** to the inner peripheral edge of the second high concentration region **43**. The field plate **141** is covered by the interlayer insulating film **74**.

[0379] The field plate **141** is formed in a band shape extending along the second high concentration region **43**. In this embodiment, the field plate **141** is formed in an annular shape (quadrangular annular shape) extending along the second high concentration region **43**. In this embodiment, the inner peripheral edge of the second intermediate concentration region **121** is positioned between an inner peripheral edge of the field plate **141** and an outer peripheral edge of the field plate **141** in plan view. The field plate **141** is covered by the interlayer insulating film **74**.

[0380] The semiconductor device **1**A includes at least one (in this embodiment, a plurality) of plate contact holes **142** each penetrating through the interlayer insulating film **74** such as to expose a portion of the field plate **141**. In this embodiment, two plate contact holes **142** are formed.

[0381] The plurality of plate contact holes **142** are each formed in a band shape extending along the field plate **141** in plan view. In this embodiment, the plurality of plate contact holes **142** are each formed in an annular shape (quadrangular annular shape) extending along the field plate **141**.

[0382] The semiconductor device **1**A includes at least one (in this embodiment, a plurality) of plate connection electrodes **143** embedded in the plate contact holes **142** such as to be electrically connected to the field plate **141**. In this embodiment, two plate connection electrodes **143** that are respectively embedded in the two plate contact holes **142** are provided. As a matter of course, a single plate contact hole **142** may be formed and a single plate connection electrode **143** may be embedded in the single plate contact hole **142** instead. The plate connection electrodes **143** may be referred to as “plate via electrodes.”

[0383] The plurality of plate connection electrodes **143** may each include at least one type among a Ti film, a TiN film, a W film, an Al film, a Cu film, an Al alloy film, a Cu alloy film, and a conductive polysilicon film. In this embodiment, the plurality of plate connection electrodes **143** each have a laminated structure including a Ti film and a W film.

[0384] Each of the plurality of plate connection electrodes **143** is formed in a band shape extending along the field plate **141**. In this embodiment, each of the plurality of plate connection electrodes **143** is formed in an annular shape (quadrangular annular shape) extending along the field plate **141**.

[0385] The semiconductor device **1**A includes, in the outer peripheral region **9**, a channel stop electrode **106** disposed on the interlayer insulating film **74**. The channel stop electrode **106** may be referred to as an “EQR (equipotential ring) electrode.” The channel stop electrode **106** may include at least one type among a Ti film, a TiN film, a W film, an Al film, a Cu film, an Al alloy film, a Cu alloy film, and a conductive polysilicon film.

[0386] The channel stop electrode **106** may include at least one among a pure Cu film, a pure Al film, an AlCu alloy film, an AlSi alloy film, and an AlSiCu alloy film. As shown FIG. **10**D, in this embodiment, the channel stop electrode **106** has a laminated structure that includes a barrier metal film **106**A and a main metal film **106**B laminated in that order from the chip **2** side. The barrier metal film **106**A is constituted, for example, of a laminated film that includes a Ti film and a TiN film that are laminated in that order from the chip **2** side. The main metal film **106**B is constituted, for example, of an Al alloy film (in this embodiment, an AlCu alloy film).

[0387] The channel stop electrode **106** is disposed on the interlayer insulating film **74** such as to cover the field plate **141** and the plurality of channel stop connection electrodes **124**. The channel stop electrode **106** is formed in a band shape extending along the peripheral edge of the chip **2**. In this embodiment, the channel stop electrode **106** is formed in an annular shape (quadrangular annular shape) extending along the peripheral edge of the chip **2**. The channel stop electrode **106** is disposed at an interval from the peripheral edge of the chip **2**.

[0388] The channel stop electrode **106** is electrically connected to the second high concentration region **43** and the channel stop contact regions **122** via the plurality of channel stop connection

electrodes **124**. Also, the channel stop electrode **106** is electrically connected to the field plate **141** via the plurality of plate connection electrodes **143**. The channel stop electrode **106** is formed in an electrically floating state.

[0389] The semiconductor device **1**A includes a collector electrode **107** that covers the second principal surface **4**. The collector electrode **107** is an example of a "second main electrode" in the present disclosure. The collector electrode **107** is electrically connected to the collector region **14** exposed from the second principal surface **4**. The collector electrode **107** forms an ohmic contact with the collector region **14**. The collector electrode **107** may cover an entire region of the second principal surface **4** such as to be continuous with the peripheral edge of the chip **2** (the first to fourth side surfaces **5**A to **5**D).

[0390] A parasitic thyristor, constituted of a parasitic npn transistor having the emitter regions **29** as an emitter, the drift region **12** and the first intermediate concentration region **19** as a collector, and the channel region **20** as a base and a parasitic pnp transistor having the collector region **14** as an emitter, the channel region **20** as a collector, and the drift region **12** and the first intermediate concentration region **19** as a base, is formed in the semiconductor device **1**A.

[0391] The parasitic thyristor operates when the parasitic npn transistor is turned on by a voltage drop due to a resistance component of the channel region **20** corresponding to the base of the parasitic npn transistor when the semiconductor device **1**A (the IGBT) is switched from on to off. A phenomenon (latch-up) in which the IGBT does not turn off and a large current flows is liable to occur in this case.

[0392] With the semiconductor device **1**A, in the active regions **6**, the channel contact regions **31** that are higher in p-type impurity concentration than the channel region **20** of the p-type are formed inside the channel region **20**. Thus, when the semiconductor device **1**A (the IGBT) is switched from on to off, a current flows to the channel contact regions **31** of low resistance value, and turning on of the parasitic npn transistor can thus be suppressed. A latch-up tolerance can thus be improved.

[0393] With the semiconductor device **1**A, as shown in FIG. **10**B and FIG. **10**D, in a peripheral edge portion of the outer peripheral region **9**, the second intermediate concentration region **121** of the n-type of higher n-type impurity concentration than the drift region **12** of the n-type is formed in the surface layer portion at the first principal surface **3** side of the drift region **12**. Also, in the outer peripheral region **9**, the second high concentration region **43** of the n-type is formed, as a channel stop region of higher n-type impurity concentration than the second intermediate concentration region **121**, in the surface layer portion of the first principal surface **3** at the first principal surface **3** side with respect to the second intermediate concentration region **121**. Also, the channel stop contact regions **122** of the p-type are formed in the surface layer portion at the second high concentration region **43** side of the second intermediate concentration region **121**.

[0394] Thus, with the semiconductor device **1**A, since the second intermediate concentration region **121** of the n-type is formed at the second principal surface **4** side with respect to the second high concentration region **43** of the n-type as the channel stop region, a leak current can be reduced. A reason for this shall be described below.

[0395] FIG. **10**E is an enlarged cross-sectional view showing a part of a semiconductor device **201** according to a comparative example and is an enlarged cross-sectional view corresponding to FIG. **10**D. In FIG. **10**E, portions corresponding to respective portions of FIG. **10**D have the same reference symbols attached as in FIG. **10**D.

[0396] With the semiconductor device **201** according to the comparative example, a structure in a vicinity of the second high concentration region (channel stop layer) **43** shown in FIG. **10**E differs from that of the semiconductor device **1**A according to the present preferred embodiment. Specifically, with the semiconductor device **201** according to the comparative example, in the outer peripheral region **9**, the second intermediate concentration region **121** is not formed in the surface layer portion at the first principal surface **3** side of the drift region **12**.

[0397] More specifically, with the semiconductor device **201** according to the comparative example, in the peripheral edge portion of the outer peripheral region **9**, the second high concentration region **43** of the n-type as the channel stop region is formed in the surface layer portion at the first principal surface **3** side of the drift region **12**. Also, the channel stop contact regions **122** of the p-type are formed in a surface layer portion at the second high concentration region **43** side of the drift region **12**.
[0398] With the semiconductor device **201** according to the comparative example, the bottom surfaces of the channel stop contact regions **122** are in contact with the drift region **12**. Thus, when the semiconductor device **201** (the IGBT) is off, holes are easily injected from the channel stop contact regions **122** of the p-type into the drift region **12** and a leak current Ices is thus liable to increase.
[0399] On the other hand, with the semiconductor device **1**A according to the present preferred embodiment, since the bottom surfaces of the channel stop contact regions **122** are in contact with the second intermediate concentration region **121** that is higher in n-type impurity than the drift region **12**, hole injection from the channel stop contact regions **122** of the p-type to the drift region **12** is suppressed when the semiconductor device **1**A (the IGBT) is off. Thereby, with the semiconductor device **1**A according to the present preferred embodiment, the leak current Ices can be reduced in comparison to the semiconductor device **201** according to the comparative example.
[0400] FIG. **25** is a graph showing simulation results of leak current Ices [A] with respect to collector-emitter voltage Vce [V] respectively for the semiconductor device **1**A according to the present preferred embodiment and the semiconductor device **201** according to the comparative example.
[0401] FIG. **25** is a graph showing the simulation results when junction temperature Tj=175° C. In FIG. **25**, a curve Q**1** is the graph showing the simulation result for the semiconductor device **1**A according to the present preferred embodiment and a curve Q**2** is the graph showing the simulation result for the semiconductor device **201** according to the comparative example.
[0402] From FIG. **25**, it can be understood that with the semiconductor device **1**A according to the present preferred embodiment, the leak current Ices is decreased in comparison to the semiconductor device **201** according to the comparative example.
[0403] It is possible to form the second intermediate concentration region **121** at the same time as the first intermediate concentration region **19** as the carrier accumulation region in the step of forming the first intermediate concentration region **19**. Therefore, with the semiconductor device **1**A according to the present preferred embodiment, it is made possible to suppress the leak current without increasing manufacturing steps in comparison to the comparative example.
[0404] The semiconductor device **1**A includes the chip **2**, the trench resistive structures **51**, the resistive film **60**, the gate terminal electrode **90**, and the gate wiring electrode **93**. The chip **2** has the first principal surface **3**. The trench resistive structures **51** are formed in the first principal surface **3**. The resistive film **60** is electrically connected to the trench resistive structures **51** on the first principal surface **3**.
[0405] The gate terminal electrode **90** has a lower resistance value than the resistive film **60** and, on the first principal surface **3**, is electrically connected to the trench resistive structures **51** via the resistive film **60**. The gate wiring electrode **93** has a lower resistance value than the resistive film **60** and, on the first principal surface **3**, is electrically connected to the gate terminal electrode **90** via the trench resistive structures **51** and the resistive film **60**.
[0406] According to this arrangement, the gate resistance RG that includes the trench resistive structures **51** and the resistive film **60** can be interposed between the gate terminal electrode **90** and the gate wiring electrode **93**. Particularly, according to this arrangement, since the trench resistive structures **51** are incorporated inside the chip **2** in a region between the gate terminal electrode **90** and the gate wiring electrode **93**, an increase in an occupied area of the gate resistance RG with respect to the first principal surface **3** can be suppressed. Therefore, it is possible to provide the

semiconductor device **1**A having a novel layout that contributes to miniaturization in the arrangement including the gate resistance RG.

[0407] The semiconductor device **1**A preferably includes the gate electrode film **64** and the gate wiring film **65**. The gate electrode film **64** is disposed, mutually adjacent to the resistive film **60**, on the first principal surface **3**. The gate wiring film **65** is disposed, mutually adjacent to the resistive film **60**, on the first principal surface **3** such as to face the gate electrode film **64** with the resistive film **60** interposed therebetween.

[0408] In such a structure, the gate terminal electrode **90** preferably covers the gate electrode film **64**. Also, the gate wiring electrode **93** preferably covers the gate wiring film **65**. According to this arrangement, in the arrangement including resistive film **60**, the gate electrode film **64**, and the gate wiring film **65** on the first principal surface **3**, it is possible to provide the semiconductor device **1**A having a novel layout that contributes to miniaturization.

[0409] The resistive film **60** preferably has the first end portion **60**A at one side and the second end portion **60**B at the other side. In this case, the gate wiring film **65** preferably includes the first connection portion connected to the first end portion **60**A of the resistive film **60** and the second connection portion connected to the second end portion **60**B of the resistive film **60**. In this case, the gate wiring electrode **93** is preferably electrically connected to the resistive film **60** via the gate wiring film **65**.

[0410] According to this arrangement, since the gate wiring electrode **93** can be electrically connected to the resistive film **60** via the gate wiring film **65**, it is not necessary to directly connect the gate wiring electrode **93** to the resistive film **60**. Consequently, a design rule of the gate wiring electrode **93** can be relaxed, and a degree of freedom of design of the gate wiring electrode **93** can be improved.

[0411] The semiconductor device **1**A preferably includes the first slit **71** demarcated between the resistive film **60** and the gate electrode film **64** and the second slit **72** demarcated between the resistive film **60** and the gate wiring film **65**. According to this arrangement, the resistive film **60** can be appropriately separated (demarcated) from the gate electrode film **64** and the gate wiring film **65** by the first slit **71** and the second slit **72**. Thereby, the precision of the resistance value of the resistive film **60** can be improved.

[0412] The gate terminal electrode **90** preferably covers the resistive film **60** and the gate electrode film **64** across the first slit **71** in plan view. The gate wiring film **65** preferably covers the resistive film **60** and the gate electrode film **64** across the second slit **72** in plan view. The first slit **71** is preferably formed to be narrower than the resistive film **60**. The second slit **72** is preferably formed to be narrower than the resistive film **60**.

[0413] The trench resistive structures **51** preferably extend in band shapes in the second direction Y (one direction) in plan view. In this case, the resistive film **60** preferably extends in a band shape in the second direction Y (the one direction) in plan view. Also, the first slit **71** preferably extends in a band shape in the second direction Y (the one direction) in plan view. Also, the second slit **72** preferably extends in a band shape in the second direction Y (the one direction) in plan view. The first slit **71** may have the first length in the second direction Y (the one direction), and the second slit **72** may have the second length smaller than the first length in the second direction Y (the one direction).

[0414] The semiconductor device **1**A preferably includes the third slits **73** demarcated between the gate electrode film **64** and the gate wiring film **65**. According to this arrangement, the gate wiring film **65** can be appropriately separated (demarcated) from the gate electrode film **64** by the third slits **73**. Thereby, the gate wiring film **65** can be suppressed from forming, together with the gate electrode film **64**, a short circuit without interposition of the resistive film **60**. The gate terminal electrode **90** preferably covers the gate electrode film **64** and the gate wiring film **65** across the third slits **73** in plan view.

[0415] The plurality of trench resistive structures **51** are preferably formed at an interval in the first

principal surface **3**. In this case, the resistive film **60** preferably covers the plurality of trench resistive structures **51**. According to this arrangement, the resistance value of the gate resistance RG can be adjusted using the plurality of trench resistive structures **51**.

[0416] The resistive film **60** preferably includes the first covering portion **61** covering the first principal surface **3** outside the trench resistive structures **51** and the second covering portion **62** covering the trench resistive structures **51**. In this case, the gate terminal electrode **90** is preferably electrically connected to the resistive film **60** at a portion that covers the first covering portion **61**. Also, the gate wiring electrode **93** is preferably electrically connected to the resistive film **60** at a portion that covers the second covering portion **62**. According to this arrangement, a part of the resistive film **60** and a part of the trench resistive structures **51** can be appropriately interposed in the region between the gate terminal electrode **90** and the gate wiring electrode **93**.

[0417] The semiconductor device **1**A preferably includes the interlayer insulating film **74**, the first resistance connection electrodes **81**, and the second resistance connection electrodes **82**. The interlayer insulating film **74** covers the resistive film **60**. The first resistance connection electrodes **81** are embedded in the interlayer insulating film **74** such as to be electrically connected to the resistive film **60**. The second resistance connection electrodes **82** are embedded in the interlayer insulating film **74** such as to be electrically connected to the resistive film **60** at different positions from the first resistance connection electrodes **81**.

[0418] In such an arrangement, the gate terminal electrode **90** is preferably disposed on the interlayer insulating film **74** such as to be electrically connected to the resistive film **60** via the first resistance connection electrodes **81**. Also, the gate wiring electrode **93** is preferably disposed on the interlayer insulating film **74** such as to be electrically connected to the resistive film **60** via the second resistance connection electrodes **82**. According to this arrangement, the gate resistance RG can be arranged in a region between the first resistance connection electrodes **81** and the second resistance connection electrodes **82**. The resistance value of the gate resistance RG can be adjusted by adjusting the distance between the first resistance connection electrodes **81** and the second resistance connection electrodes **82**.

[0419] The second resistance connection electrodes **82** may extend in a different direction from the first resistance connection electrodes **81**. For example, the first resistance connection electrodes **81** may extend in the first direction X (one direction) in plan view, and the second resistance connection electrodes **82** may extend in the second direction Y (intersecting direction) intersecting the first direction X (the one direction) in plan view.

[0420] The plurality of first resistance connection electrodes **81** are preferably embedded in the interlayer insulating film **74**. The plurality of second resistance connection electrodes **82** are preferably embedded in the interlayer insulating film **74**. The second connection area S**2** of the second resistance connection electrodes **82** with respect to the resistive film **60** may be smaller than the first connection area S**1** of the first resistance connection electrodes **81** with respect to the resistive film **60**.

[0421] The gate terminal electrode **90** preferably has the first electrode portion **91** positioned outside the first resistance connection electrodes **81** in plan view and the second electrode portion **92** protruding more narrowly than the first electrode portion **91** from the first electrode portion **91** to the first resistance connection electrodes **81**. In this case, the first electrode portion **91** is preferably formed as the terminal main body portion of the gate terminal electrode **90**. Also, the second electrode portion **92** is preferably formed as the terminal lead-out portion led out from the terminal main body portion.

[0422] According to these arrangements, a region to which the gate potential is applied can be secured by the first electrode portion **91**, and a region electrically connected to the resistive film **60** can be secured by the second electrode portion **92**. For example, when a conductive bonding material such as a bonding wire is bonded to the gate terminal electrode **90**, the conductive bonding material can be bonded to the first electrode portion **91**. Thereby, stress due to the conductive

bonding material can be suppressed from arising in the resistive film **60** and the trench resistive structures **51**. Therefore, it is possible to suppress degradation of electrical characteristics of the gate resistance RG.

[0423] The semiconductor device **1**A preferably includes the boundary well region **40** of the p-type formed in the surface layer portion of the first principal surface **3**. According to this arrangement, a breakdown voltage can be improved by the boundary well region **40**. In this case, the trench resistive structures **51** are preferably formed at an interval to the first principal surface **3** side from the bottom portion of the boundary well region **40**. According to this arrangement, electric field concentration at bottom walls of the trench resistive structures **51** can be suppressed by the boundary well region **40**. Therefore, the breakdown voltage can be improved appropriately.

[0424] The semiconductor device **1**A preferably includes the active regions **6** provided in the first principal surface **3**, the non-active region **7** provided outside the active regions **6** in the first principal surface **3**, and the first trench structures **21** (the trench gate structures) formed in the active regions **6**. In this case, the trench resistive structures **51** are preferably formed in the non-active region **7**. Also, the resistive film **60** preferably covers the trench resistive structures **51** in the non-active region **7**.

[0425] Also, the gate terminal electrode **90** is preferably electrically connected to the resistive film **60** in the non-active region **7**. Also, the gate wiring electrode **93** is preferably electrically connected to the first trench structures **21** in the active regions **6** and electrically connected to the resistive film **60** in the non-active region **7**. According to these arrangements, since the gate resistance RG is formed in the non-active region **7**, reduction of the active regions **6** can be suppressed.

[0426] The preferred embodiment described above can be implemented in still other embodiments. For example, in the preferred embodiment described above, an example in which the chip **2** is constituted of a silicon single crystal substrate was described. However, the chip **2** may be constituted of an SiC (silicon carbide) single crystal substrate instead.

[0427] In the preferred embodiment described above, the semiconductor regions of the n-type may be replaced with semiconductor regions of the p-type, and the semiconductor regions of the p-type may be replaced with semiconductor regions of the n-type. A specific configuration in this case can be obtained by replacing the “n-type” with the “p-type” at the same time as replacing the “p-type” with the “n-type” in the above descriptions and accompanying drawings.

[0428] In the above preferred embodiment, the collector region **14** of the p-type was described. However, a drain region of the n-type may be adopted instead of collector region **14** of the p-type. In this case, the buffer region **13** is omitted. The drain region of the n-type may be formed by a semiconductor substrate of the n-type, and the drift region **12** and the first intermediate concentration region **19** of the n-type may be formed by an epitaxial layer of the n-type. The n-type impurity concentrations of the drift region **12** and the first intermediate concentration region **19** are preferably less than the n-type impurity concentration of the drain region.

[0429] In this case, a MISFET (metal insulator semiconductor field effect transistor) structure is formed instead of the IGBT. The specific configuration in this case can be obtained by replacing “emitter” with “source” and “collector” with “drain” in the above description. In each preferred embodiment described above, the first direction X and the second

[0430] direction Y were defined by the extending directions of the first to fourth side surfaces **5**A to **5**D. However, the first direction X and the second direction Y may be arbitrary directions as long as the directions maintain an intersecting (specifically, orthogonal) relationship with each other. For example, the first direction X may be an extending direction of the third side surface **5**C (fourth side surface **5**D), and the second direction Y may be an extending direction of the first side surface **5**A (second side surface **5**B). Also, the first direction X may be a direction intersecting the first to fourth side surfaces **5**A to **5**D, and the second direction Y may be a direction intersecting the first to fourth side surfaces **5**A to **5**D.

[0431] Hereinafter, examples of features extracted from the present Description and the attached

drawings shall be indicated below. Hereinafter, the alphanumeric characters, etc., in parentheses represent the corresponding components, etc., in the preferred embodiment described above, but are not intended to limit the scope of each clause to the preferred embodiment. The “semiconductor device” according to the following clauses may be replaced with a “semiconductor switching device,” an “IGBT semiconductor device,” an “RC-IGBT semiconductor device,” or a “MISFET semiconductor device.”

[0432] [A1] A semiconductor device including a chip (**2**) that has a first principal surface (**3**) and a second principal surface (**4**) at an opposite side thereto, [0433] an active region (**6**) that is provided in the first principal surface (**3**), [0434] an outer peripheral region (**9**) that is provided in an outer peripheral portion of the first principal surface (**3**) outside the active region (**6**), [0435] a drift region (**12**) of a first conductivity type that is formed in an interior of the chip (**2**), [0436] a first intermediate concentration region (**19**) of the first conductivity type as a carrier accumulation region that, in the active region (**6**), is formed in a surface layer portion of the drift region (**12**) at the first principal surface (**3**) side and is higher in first conductivity type impurity concentration than the drift region (**12**), [0437] a channel region (**20**) of a second conductivity type that, in the active region (**6**), is disposed in a surface layer portion of the first principal surface (**3**) at the first principal surface (**3**) side with respect to the first intermediate concentration region (**19**), [0438] a first high concentration region (**29**) of the first conductivity type that is disposed in a surface layer portion of the channel region (**20**) and is higher in first conductivity type impurity concentration than the first intermediate concentration region (**19**), [0439] a trench gate structure (**21**) that, in the active region (**6**), reaches the drift region (**12**) from the first principal surface (**3**) through the first high concentration region (**29**), the channel region (**20**), and the first intermediate concentration region (**19**), [0440] a second intermediate concentration region (**121**) of the first conductivity type that, in the outer peripheral region (**9**), is selectively formed in a surface layer portion of the drift region (**12**) at the first principal surface (**3**) side and is higher in first conductivity type impurity concentration than the drift region (**12**), [0441] a second high concentration region (**43**) of the first conductivity type as a channel stop region that, in the outer peripheral region (**9**), is disposed in a surface layer portion of the first principal surface (**3**) at the first principal surface (**3**) side with respect to the second intermediate concentration region (**121**) and is higher in first conductivity type impurity concentration than the second intermediate concentration region (**121**), [0442] a channel stop contact region (**122**) of the second conductivity type that is formed in a surface layer portion of the second intermediate concentration region (**121**) at the second high concentration region (**43**) side, [0443] a channel stop electrode (**106**) that, in the outer peripheral region (**9**), is disposed on the first principal surface (**3**) such as to cover the channel stop contact region (**122**), and [0444] a channel stop connection electrode (**124**) that electrically connects the channel stop electrode (**106**) and the channel stop contact region (**122**).

[0445] [A2] The semiconductor device according to [A1], where the second high concentration region (**43**) has the same first conductivity type impurity concentration as the first high concentration region (**29**).

[0446] [A3] The semiconductor device according to [A2], where the first conductivity type impurity concentration of the first high concentration region (**29**) and the second high concentration region (**43**) is not less than 1.0×10.sup.19 cm.sup.−3 and not more than 1.0×10.sup.21 cm.sup.−3.

[0447] [A4] The semiconductor device according to [A1], where the second intermediate concentration region (**121**) has the same first conductivity type impurity concentration as the first intermediate concentration region (**19**).

[0448] [A5] The semiconductor device according to [A4], where the first conductivity type impurity concentration of the drift region (**12**) is not less than 1.0×1013 cm.sup.−3 and not more than 1.0×10.sup.15 cm.sup.−3 and

the first conductivity type impurity concentration of the first intermediate concentration region (**19**) and the second intermediate concentration region (**121**) is not less than 1.0×10.sup.15 cm.sup.−3.

[0449] [A6] The semiconductor device according to any one of [A1] to [A5], including a channel contact region (**31**) of the second conductivity type that is formed in a region differing from the first high concentration region (**29**) in a surface layer portion at the first principal surface (**3**) side of the channel region (**20**) of the active region (**6**) and has a higher second conductivity type impurity concentration than the channel region (**20**) and [0450] a first connection electrode (**85**) that is electrically connected to the channel contact region (**31**).
[0451] [A7] The semiconductor device according to [A6], where the channel contact region (**31**) has the same second conductivity type impurity concentration as the channel stop contact region (**122**).
[0452] [A8] The semiconductor device according to [A7], where the second conductivity type impurity concentration of the channel region (**20**) is not less than 1.0×1016 cm.sup.−3 and not more than 1.0×10.sup.18 cm.sup.−3 and [0453] the second conductivity type impurity concentration of the channel contact region (**31**) and the channel stop contact region (**122**) is not less than 1.0×10.sup.18 cm.sup.−3 and not more than 1.0×10.sup.20 cm.sup.−3.
[0454] [A9] The semiconductor device according to [A6], including a surface insulating film (**45**, **46**) that is formed selectively on the first principal surface (**3**), [0455] an interlayer insulating film (**74**) that is formed on the first principal surface (**3**) such as to cover the surface insulating film (**45**, **46**), and [0456] a first contact hole (**30**) that, in the active region (**6**), reaches the channel contact region (**31**) from the first principal surface (**3**) through the first high concentration region (**29**), and [0457] where the first connection electrode (**85**) penetrates through the interlayer insulating film (**74**) and the surface insulating film (**45**, **46**) and is embedded in the first contact hole (**30**).
[0458] [A10] The semiconductor device according to [A9], including a first main electrode (**103**, **104**) that, in the active region (**6**), is disposed on the interlayer insulating film (**74**) and is electrically connected to the first connection electrode (**85**).
[0459] [A11] The semiconductor device according to [A10], including a gate electrode (**90**, **93**) that is disposed on the interlayer insulating film (**74**) and is electrically connected to the trench gate structure (**21**).
[0460] [A12] The semiconductor device according to [A11], including a second main electrode (**107**) that is formed on the second principal surface (**4**).
[0461] [A13] The semiconductor device according to [A12], where the first high concentration region (**29**) is an emitter region, [0462] the first main electrode (**103**, **104**) is an emitter electrode, and [0463] the second main electrode (**107**) is a collector electrode.
[0464] [A14] The semiconductor device according to any one of [A1] to [A13], including a surface insulating film (**45**, **46**) that is formed selectively on the first principal surface (**3**), [0465] an interlayer insulating film (**74**) that is formed on the first principal surface (**3**) such as to cover the surface insulating film (**45**, **46**), and [0466] a second contact hole (**123**) that, in the outer peripheral region (**9**), reaches the channel stop contact region (**122**) from the first principal surface (**3**) through the second high concentration region (**43**), and [0467] where the channel stop connection electrode (**124**) penetrates through the interlayer insulating film (**74**) and the surface insulating film (**45**, **46**) and is embedded in the second contact hole (**123**).
[0468] [A15] The semiconductor device according to [A14], where the channel stop electrode (**106**) is disposed on the interlayer insulating film (**74**) in the outer peripheral region (**9**).
[0469] [A16] The semiconductor device according to [A15], including a field plate (**141**) that, in a region of the outer peripheral region (**9**) further inward than the channel stop connection electrode (**124**) in plan view, is disposed on the surface insulating film (**45**, **46**) and is covered by the channel stop electrode (**106**) via the interlayer insulating film (**74**) and [0470] a field plate connection electrode (**143**) that penetrates through the interlayer insulating film (**74**) and electrically connects the field plate (**141**) and the channel stop electrode (**106**).
[0471] [A17] The semiconductor device according to [A16], where the field plate (**141**) contains a conductive polysilicon.

[0472] [A18] The semiconductor device according to [A17], including a field region (**42**) of the second conductivity type that, in a region of the outer peripheral region (**9**) further inward than the channel stop electrode (**106**) in plan view, is formed in a surface layer portion at the first principal surface (**3**) side of the drift region (**12**), [0473] a field contact region (**111**) of the second conductivity type that is formed in a surface layer portion at the first principal surface (**3**) side of the field region (**42**), [0474] a field electrode (**105**) that is formed on the interlayer insulating film (**74**) such as to cover the field contact region (**111**), and [0475] a field connection electrode (**89**) that penetrates through the interlayer insulating film (**74**) and the surface insulating film (**45**, **46**) and electrically connects the field contact region (**111**) and the field electrode (**105**).
[0476] [A19] The semiconductor device according to any one of [A1] to [A18], where the second intermediate concentration region (**121**) and the second high concentration region (**43**) are formed in annular shapes extending along a peripheral edge of the chip (**2**).
[0477] [A20] The semiconductor device according to [A19], where the channel stop contact region (**122**) is formed an annular shape extending along the second intermediate concentration region (**121**). **10**
[0478] While the preferred embodiment was described in detail above, this is merely a specific example used to clarify the technical contents and the present disclosure should not be interpreted as being limited to this specific example and the scope of the present disclosure is limited only by the appended claims.

Claims

1. A semiconductor device comprising: a chip that has a first principal surface and a second principal surface at an opposite side thereto; an active region that is provided in the first principal surface; an outer peripheral region that is provided in an outer peripheral portion of the first principal surface outside the active region; a drift region of a first conductivity type that is formed in an interior of the chip; a first intermediate concentration region of the first conductivity type as a carrier accumulation region that, in the active region, is formed in a surface layer portion of the drift region at the first principal surface side and is higher in first conductivity type impurity concentration than the drift region; a channel region of a second conductivity type that, in the active region, is disposed in a surface layer portion of the first principal surface at the first principal surface side with respect to the first intermediate concentration region; a first high concentration region of the first conductivity type that is disposed in a surface layer portion of the channel region and is higher in first conductivity type impurity concentration than the first intermediate concentration region; a trench gate structure that, in the active region, reaches the drift region from the first principal surface through the first high concentration region, the channel region, and the first intermediate concentration region; a second intermediate concentration region of the first conductivity type that, in the outer peripheral region, is selectively formed in a surface layer portion of the drift region at the first principal surface side and is higher in first conductivity type impurity concentration than the drift region; a second high concentration region of the first conductivity type as a channel stop region that, in the outer peripheral region, is disposed in a surface layer portion of the first principal surface at the first principal surface side with respect to the second intermediate concentration region and is higher in first conductivity type impurity concentration than the second intermediate concentration region; a channel stop contact region of the second conductivity type that is formed in a surface layer portion of the second intermediate concentration region at the second high concentration region side; a channel stop electrode that, in the outer peripheral region, is disposed on the first principal surface such as to cover the channel stop contact region; and a channel stop connection electrode that electrically connects the channel stop electrode and the channel stop contact region.
2. The semiconductor device according to claim 1, wherein the second high concentration region

has the same first conductivity type impurity concentration as the first high concentration region.
3. The semiconductor device according to claim 2, wherein the first conductivity type impurity concentration of the first high concentration region and the second high concentration region is not less than 1.0×10.sup.19 cm.sup.−3 and not more than 1.0×10.sup.21 cm.sup.−3.
4. The semiconductor device according to claim 1, wherein the second intermediate concentration region has the same first conductivity type impurity concentration as the first intermediate concentration region.
5. The semiconductor device according to claim 4, wherein the first conductivity type impurity concentration of the drift region is not less than 1.0×1013 cm.sup.−3 and not more than 1.0×10.sup.15 cm.sup.−3 and the first conductivity type impurity concentration of the first intermediate concentration region and the second intermediate concentration region is not less than 1.0×10.sup.15 cm.sup.−3.
6. The semiconductor device according to claim 1, comprising: a channel contact region of the second conductivity type that is formed in a region differing from the first high concentration region in a surface layer portion at the first principal surface side of the channel region of the active region and has a higher second conductivity type impurity concentration than the channel region and a first connection electrode that is electrically connected to the channel contact region.
7. The semiconductor device according to claim 6, wherein the channel stop contact region has the same second conductivity type impurity concentration as the channel contact region.
8. The semiconductor device according to claim 7, wherein the second conductivity type impurity concentration of the channel region is not less than 1.0×1016 cm.sup.−3 and not more than 1.0×10.sup.18 cm.sup.−3 and the second conductivity type impurity concentration of the channel contact region and the channel stop contact region is not less than 1.0×10.sup.18 cm.sup.−3 and not more than 1.0×10.sup.20 cm.sup.−3.
9. The semiconductor device according to claim 6, comprising: a surface insulating film that is formed selectively on the first principal surface; an interlayer insulating film that is formed on the first principal surface such as to cover the surface insulating film; and a first contact hole that, in the active region, reaches the channel contact region from the first principal surface through the first high concentration region; and where the first connection electrode penetrates through the interlayer insulating film and the surface insulating film and is embedded in the first contact hole.
10. The semiconductor device according to claim 9, comprising: a first main electrode that, in the active region, is disposed on the interlayer insulating film and is electrically connected to the first connection electrode.
11. The semiconductor device according to claim 10, comprising: a gate electrode that is disposed on the interlayer insulating film and is electrically connected to the trench gate structure.
12. The semiconductor device according to claim 11, comprising: a second main electrode that is formed on the second principal surface.
13. The semiconductor device according to claim 12, wherein the first high concentration region is an emitter region, the first main electrode is an emitter electrode, and the second main electrode is a collector electrode.
14. The semiconductor device according to claim 1, comprising: a surface insulating film that is formed selectively on the first principal surface; an interlayer insulating film that is formed on the first principal surface such as to cover the surface insulating film; and a second contact hole that, in the outer peripheral region, reaches the channel stop contact region from the first principal surface through the second high concentration region; and wherein the channel stop connection electrode penetrates through the interlayer insulating film and the surface insulating film and is embedded in the second contact hole.
15. The semiconductor device according to claim 14, wherein the channel stop electrode is disposed on the interlayer insulating film in the outer peripheral region.
16. The semiconductor device according to claim 15, comprising: a field plate that, in a region of

the outer peripheral region further inward than the channel stop connection electrode in plan view, is disposed on the surface insulating film and is covered by the channel stop electrode via the interlayer insulating film and a field plate connection electrode that penetrates through the interlayer insulating film and electrically connects the field plate and the channel stop electrode.

17. The semiconductor device according to claim 16, wherein the field plate contains a conductive polysilicon.

18. The semiconductor device according to claim 17, comprising: a field region of the second conductivity type that, in a region of the outer peripheral region further inward than the channel stop electrode in plan view, is formed in a surface layer portion at the first principal surface side of the drift region; a field contact region of the second conductivity type that is formed in a surface layer portion at the first principal surface side of the field region; a field electrode that is formed on the interlayer insulating film such as to cover the field contact region; and a field connection electrode that penetrates through the interlayer insulating film and the surface insulating film and electrically connects the field contact region and the field electrode.

19. The semiconductor device according to claim 1, wherein the second intermediate concentration region and the second high concentration region are formed in annular shapes extending along a peripheral edge of the chip.

20. The semiconductor device according to claim 19, wherein the channel stop contact region is formed an annular shape extending along the second intermediate concentration region.