US 20250266000A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2025/0266000 A1**

ZHAO et al. (43) **Pub. Date: Aug. 21, 2025**

(54) **VOLTAGE-INPUT PIXEL DRIVING CIRCUIT FOR MICRODISPLAY PANEL**

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(21) Appl. No.: **18/871,819**

(22) PCT Filed: **Feb. 29, 2024**

(86) PCT No.: **PCT/CN2024/079254**

§ 371 (c)(1),
(2) Date: **Dec. 5, 2024**

(30) **Foreign Application Priority Data**

Mar. 3, 2023 (CN) 202310196354.7

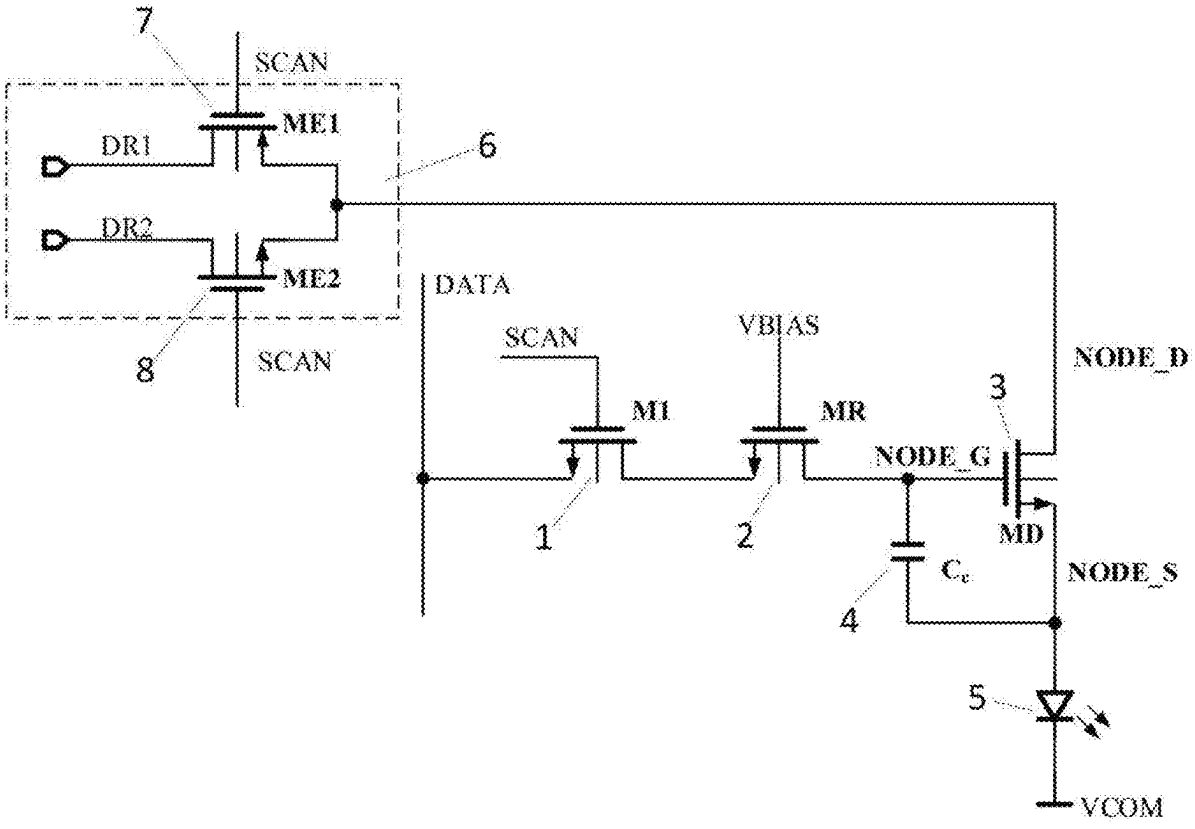
Publication Classification

(51) **Int. Cl.**
G09G 3/3258 (2016.01)
G09G 3/32 (2016.01)

(52) **U.S. Cl.**
CPC ***G09G 3/3258*** (2013.01); ***G09G 3/32*** (2013.01); *G09G 2300/043* (2013.01); *G09G 2330/021* (2013.01)

(57) **ABSTRACT**

Provided is a voltage-input input pixel driving circuit for a microdisplay panel. The voltage-input pixel driving circuit includes: a first transistor, a second transistor, a driving transistor, a coupling capacitor, a light-emitting element, and a MUX signal gating unit. The first transistor includes a gate connected to a scan signal line (SCAN) of the microdisplay panel, a source connected to a data signal line (DATA) of the microdisplay panel, and a drain connected to a source of the second transistor; a gate of the second transistor is connected to an external bias voltage (VBIAS), a drain of the second transistor is connected to a gate of the driving transistor, a source of the driving transistor is connected to one end of the light-emitting element, the other end of the light-emitting element is connected to a common voltage (VCOM).



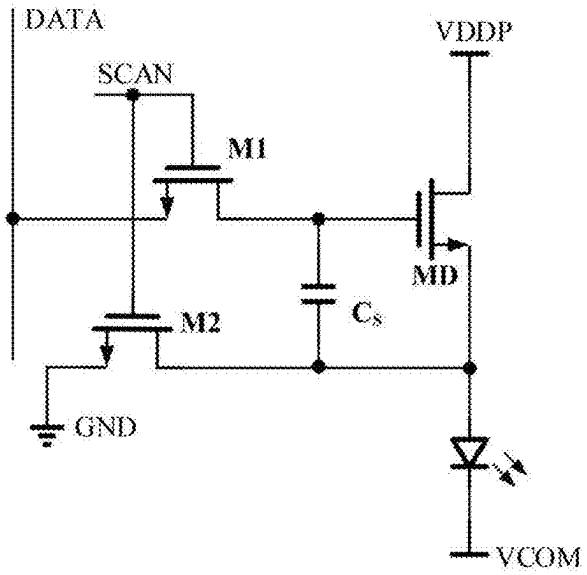


FIG. 1 (Prior Art)

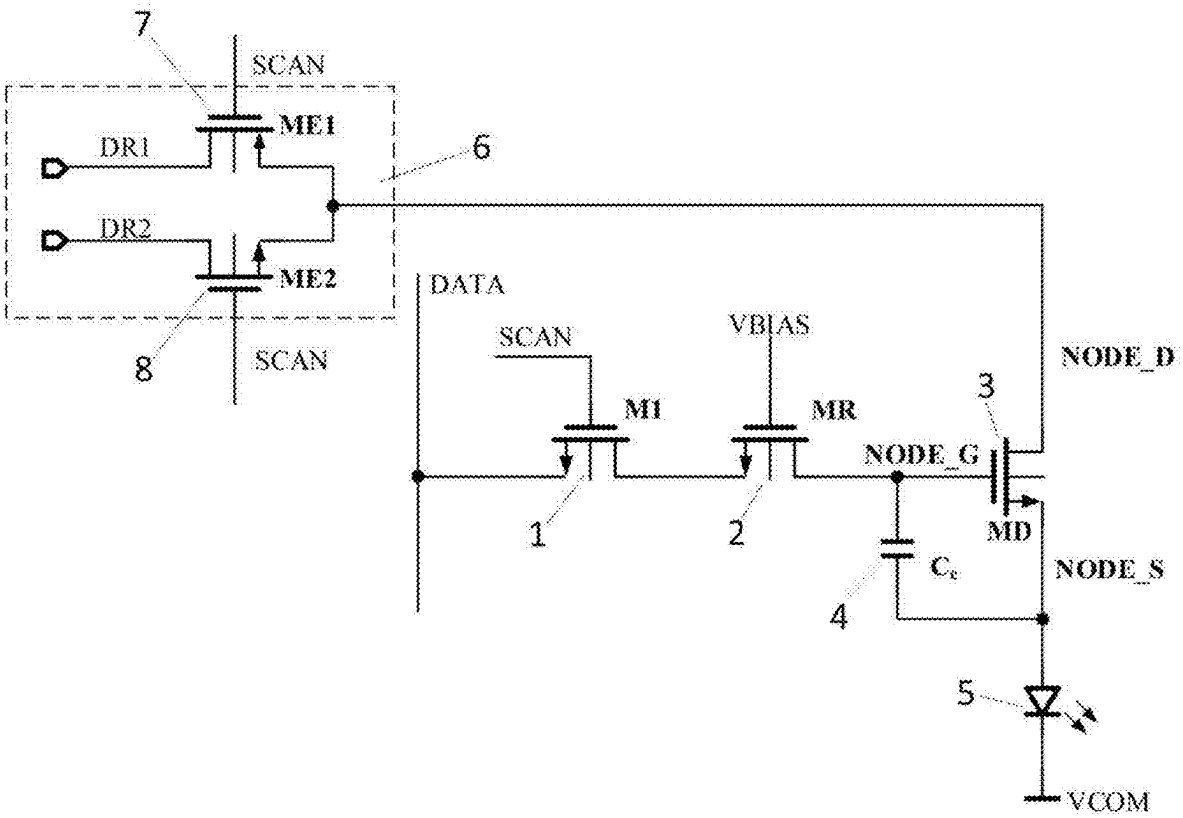


FIG. 2

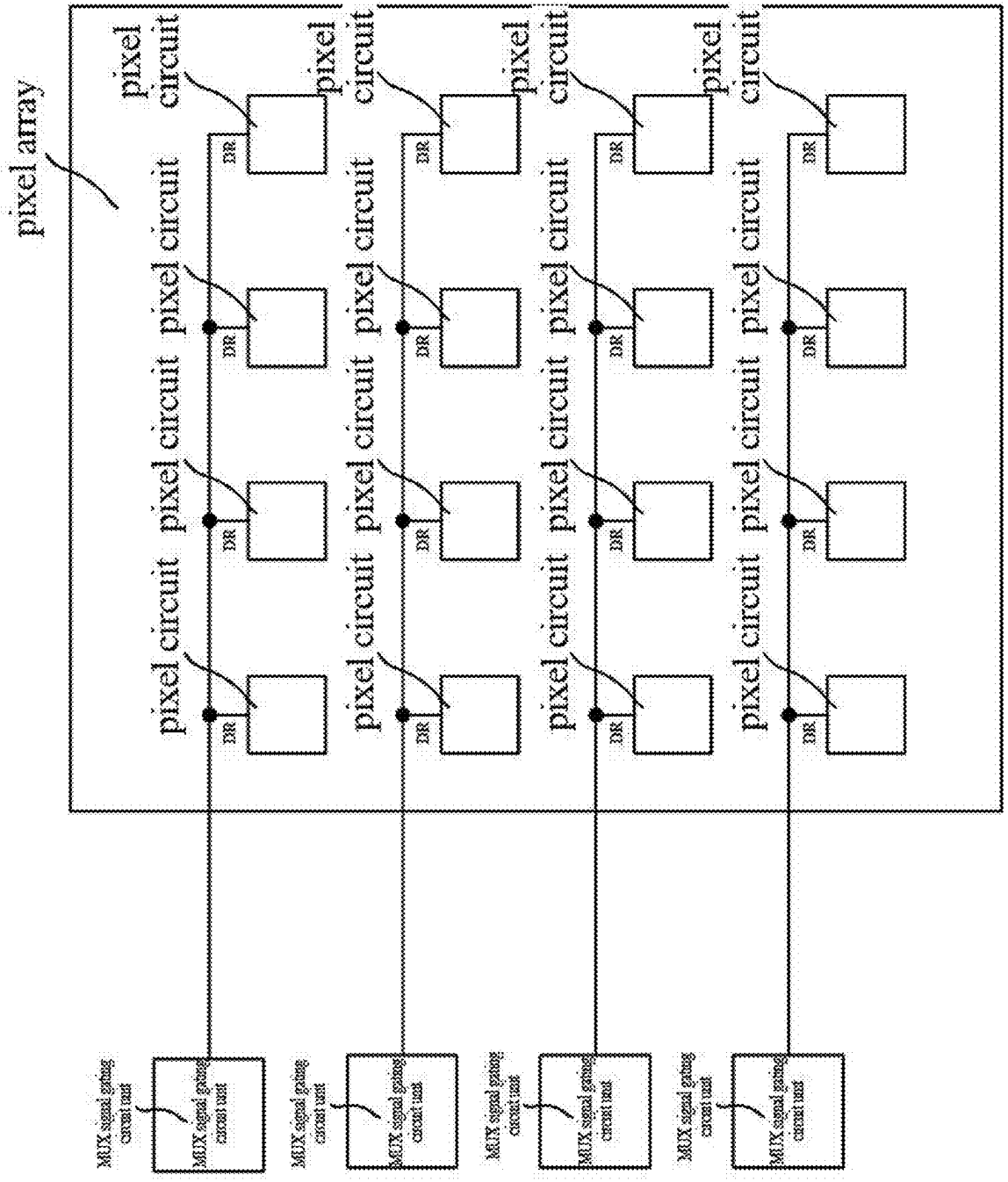

pixel array
pixel circuit
DR
MUX signal gating circuit unit

FIG. 3

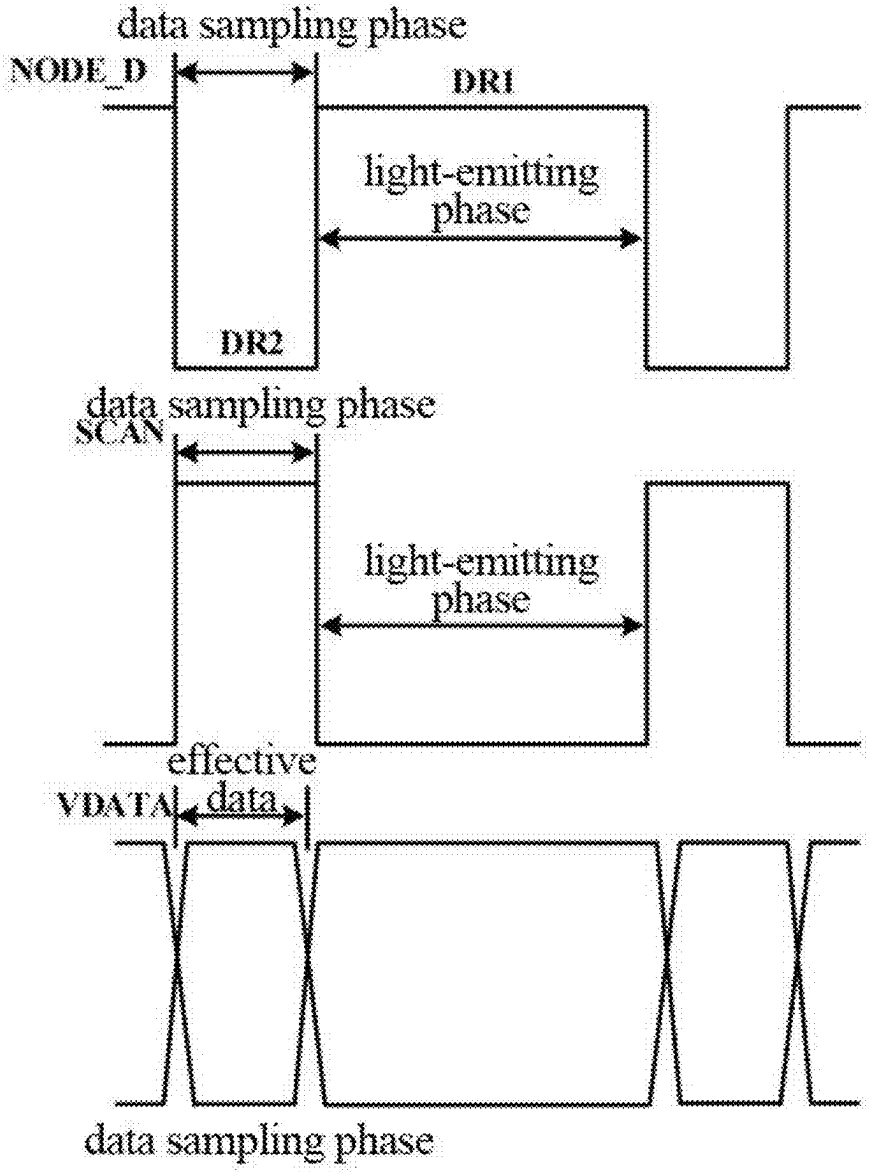

data sampling phase
NODE_D
DR1
light-emitting phase
DR2
data sampling phase
SCAN
light-emitting phase
effective data
VDATA
data sampling phase

FIG. 4

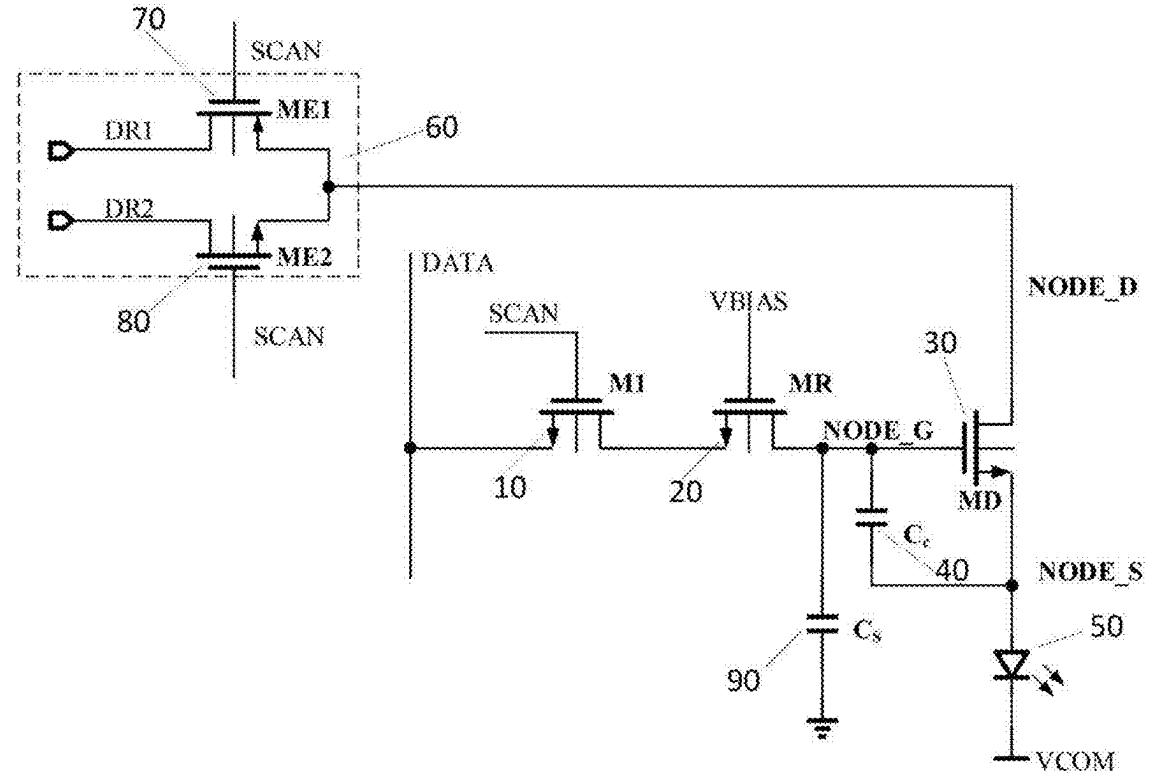

70
SCAN
ME1
DR1
60
DR2
ME2
80
SCAN
DATA
SCAN
VBIAS
NODE_D
30
M1
MR
NODE_G
10
20
MD
C_s
40
NODE_S
C_s
50
90
VCOM

FIG. 5

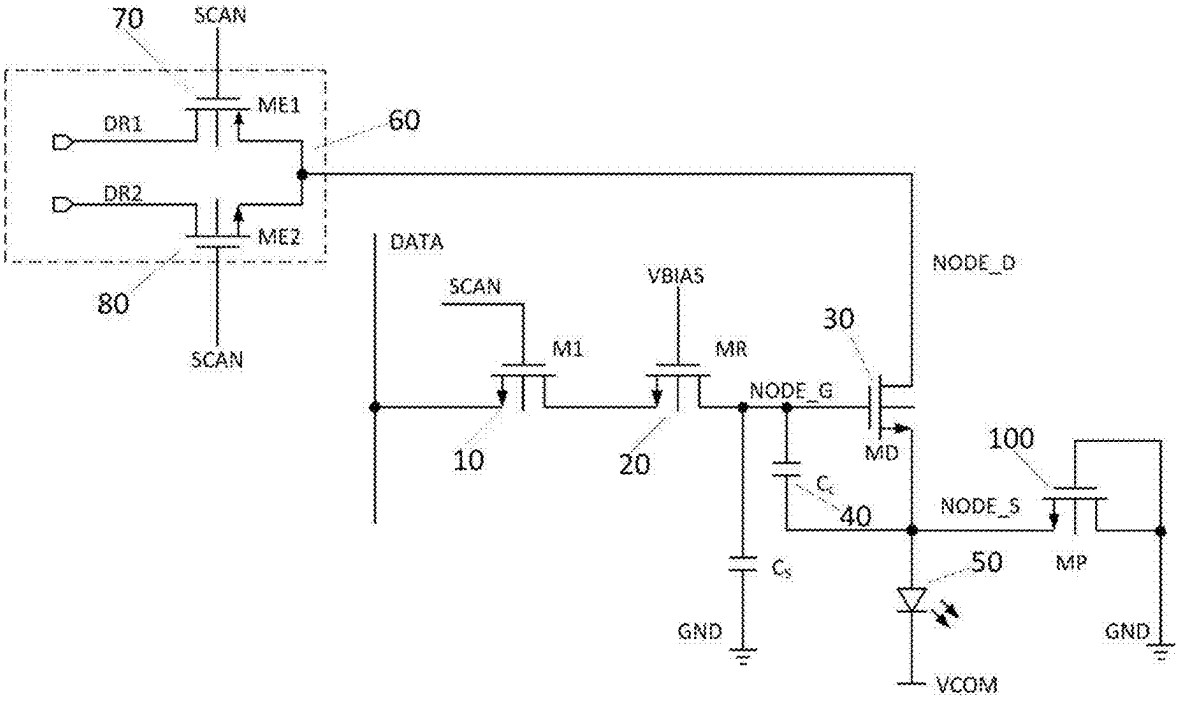

70
SCAN
ME1
DR1
60
DR2
ME2
80
SCAN
DATA
SCAN
VBIAS
NODE_D
30
M1
MR
NODE_G
10
20
MD
100
C_s
40
NODE_S
C_s
50
MP
GND
GND
VCOM

FIG. 6

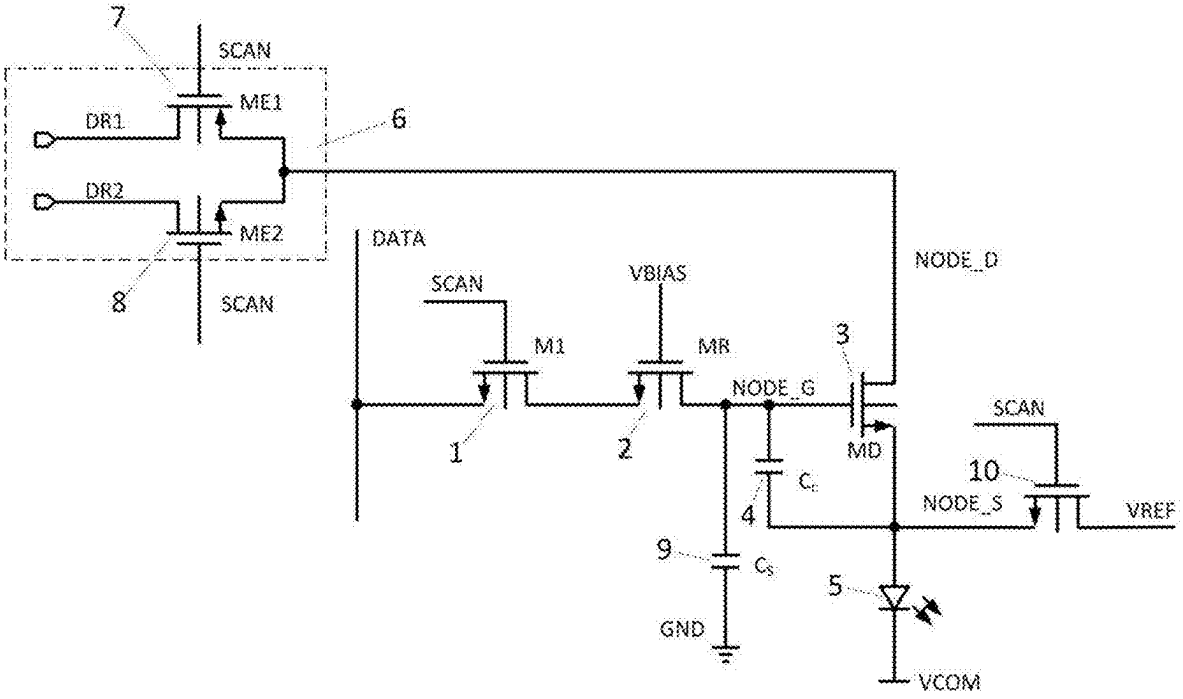

7
SCAN
ME1
DR1
6
DR2
ME2
8
SCAN
DATA
SCAN
VBIAS
NODE_D
M1
MR
3
NODE_G
SCAN
1
2
MD
10
C_c
NODE_S
VREF
4
9
C_s
5
GND
VCOM

FIG. 7

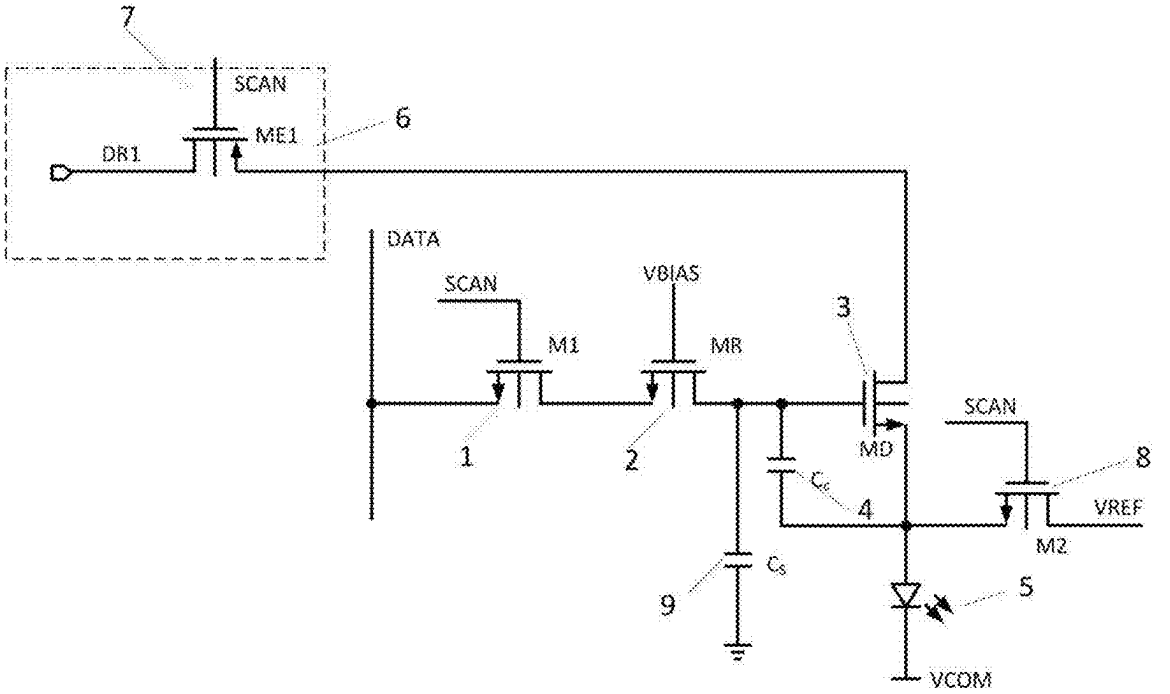

7
SCAN
ME1
DR1
6
DATA
SCAN
VBIAS
M1
MR
3
SCAN
1
2
MD
8
C_c
4
VREF
M2
9
C_s
5
VCOM

FIG. 8

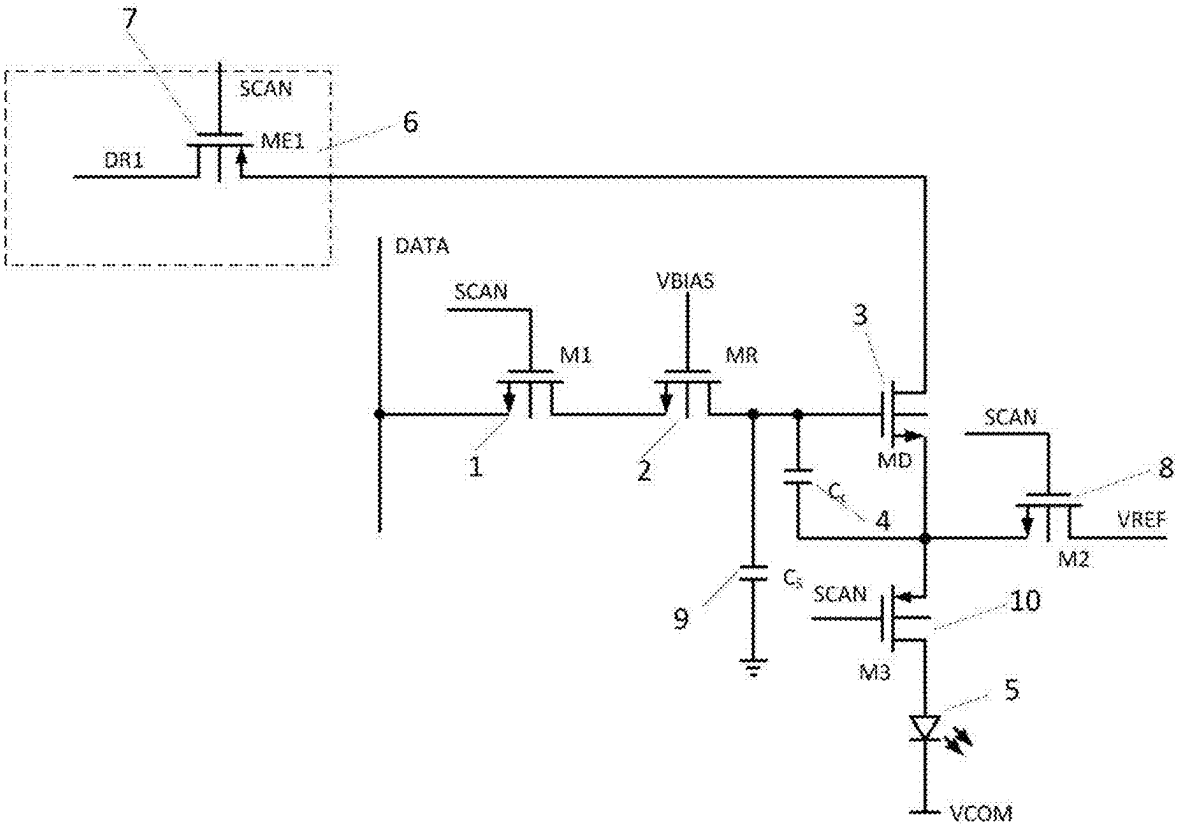

7
SCAN
ME1
6
DR1
DATA
SCAN
VBIAS
M1
MR
3
1
2
MD
SCAN
8
C_s
4
VREF
M2
9
C_s
SCAN
10
M3
5
VCOM

FIG. 9A

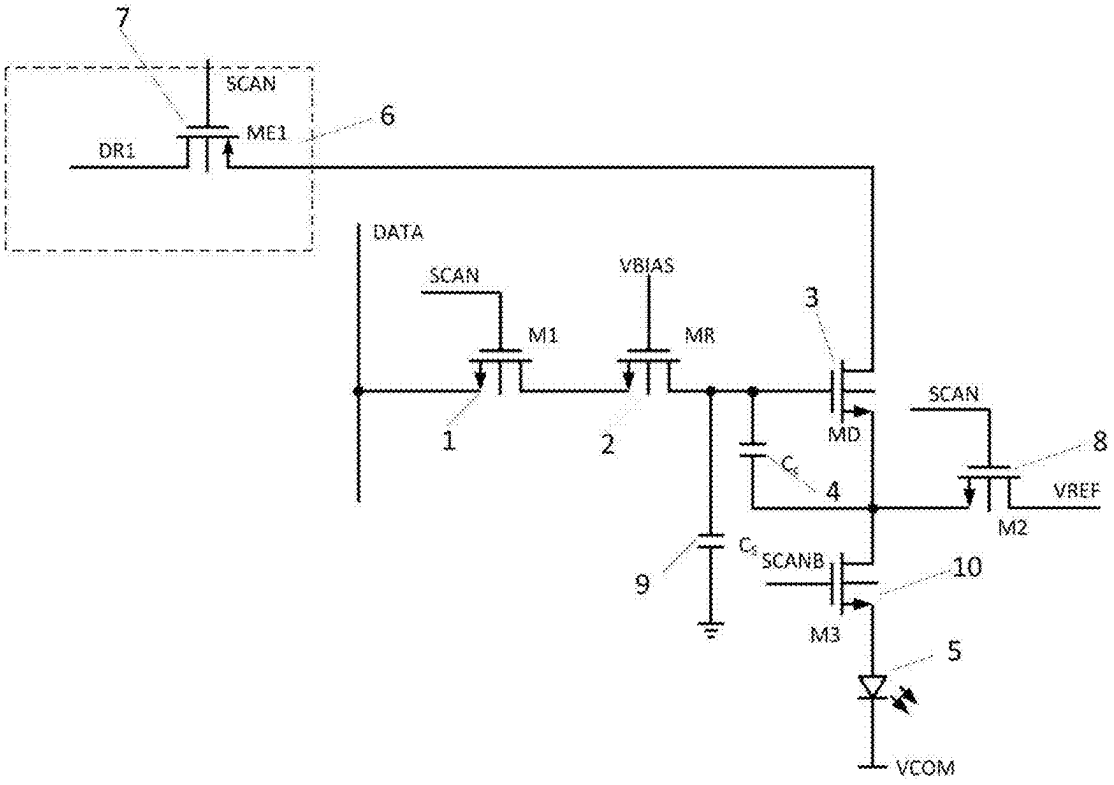

7
SCAN
ME1
6
DR1
DATA
SCAN
VBIAS
M1
MR
3
1
2
MD
SCAN
8
C_s
4
VREF
M2
9
C_s
SCANB
10
M3
5
VCOM

FIG. 9B

VOLTAGE-INPUT PIXEL DRIVING CIRCUIT FOR MICRODISPLAY PANEL

CROSS-REFERENCE TO THE RELATED APPLICATIONS

[0001] This application is the national phase entry of International Application No. PCT/CN2024/079254, filed on Feb. 29, 2024, which is based upon and claims priority to Chinese Patent Application No. 202310196354.7, filed on Mar. 3, 2023, the entire contents of which are incorporated herein by reference.

TECHNICAL FIELD

[0002] The present invention relates to the field of microdisplay technology, and in particular to a voltage-input pixel driving circuit for a microdisplay panel.

BACKGROUND

[0003] In recent years, with the development of AR (Augmented Reality) and VR (Virtual Reality) technologies, their closely related microdisplay technology has also drawn extensive attention. Microdisplay technology (Microdisplay) is a branch of the technical field of display. Generally, displays with a diagonal size less than 1 inch (2.54 cm) or those small enough to require optical magnification are called microdisplays. Currently, common microdisplay technologies include the following 4 types: OLEDoS (Organic Light-Emitting Diode on Silicon), LEDoS (Light Emitting Diode on Silicon), LCoS (Liquid Crystal on Silicon), and DMD (Digital Micromirror Device). Among them, OLEDoS and LEDoS are both active light-emitting techniques, while LCoS and DMD are both passive light-emitting techniques. Since OLEDoS and LEDoS further have the advantages of low power consumption, high contrast, and fast response, they are more suitable for application in AR and VR technologies.

[0004] Different from conventional processes using amorphous silicon, microcrystalline silicon, or low-temperature polysilicon, OLEDoS and LEDoS microdisplays use monocrystalline silicon chips as substrates, meaning that they can use the existing mature integrated circuit CMOS (Complementary Metal-Oxide-Semiconductor) process. Hence, OLEDoS and LEDoS microdisplays can not only realize active matrix for display pixel addressing, but also achieve driving control circuits of various functions, such as scan chain circuits, digital-to-analog conversion circuits, and bandgap references, thereby significantly reducing the external connections, increasing reliability, and achieving weight reduction of the device.

[0005] Currently, the pixel unit circuit structure in OLED/LED displays often employs an analog driving method, which generally includes data voltage input and data current input. These two driving methods have their own advantages and disadvantages. For example, the main problem of the voltage input method is a display consistency problem caused by the deviation of the driving transistor parameters or a problem of a small output voltage range (source follower structure), whereas the current input method has a problem of slow writing speed. Therefore, the present invention proposes a new driving structure that can increase its output voltage range with respect to the existing voltage-input pixel unit circuit (source follower structure).

[0006] As shown in FIG. **1**, a pixel driving circuit of a source follower structure in the prior art is composed of three transistors, a SCAN control signal line, a coupling capacitor C_s, and an OLED/LED light-emitting device. Its basic operation principle involves the following phases.

[0007] Data voltage writing phase: a SCAN signal is at a high level, a NMOS transistor M**1** and a NMOS transistor M**2** are turned on, and thus the gate voltage and source voltage of a driving MOS transistor MD are V_{DATA} and 0 level, respectively, namely, the voltage across the coupling capacitor C_s is V_{DATA}.

[0008] Light-emitting phase of display device: the SCAN signal is at a low level, and the NMOS transistor M**1** and NMOS transistor M**2** are turned off. Given that the gate voltage of the driving MOS transistor MD is V_{DATA}, the driving MOS transistor MD is turned on to charge the source of the driving MOS transistor MD. Assuming that the final voltage of the source of the driving MOS transistor MD is V_{ANODE}, and taking the capacitive coupling into consideration and assuming that the parasitic capacitance of the gate of the driving MOS transistor MD is C_p, then the gate voltage is $V_{DATA}+k\times V_{ANODE}$, where $k=C_s/(C_s+C_p)$.

[0009] The above-mentioned pixel driving circuit in the prior art has the following disadvantages. Static power consumption occurs during the input voltage data writing, and the NMOS transistor M**1** and the NMOS transistor M**2** are turned on, leading to a current loop of the path VDDP→MD→M**2**→GND. In addition, the source voltage of the driving MOS transistor MD cannot reach VDDP, because if the source voltage of the driving MOS transistor MD is VDDP, then the gate voltage must be $V_{DATA}+k\times$ VDDP at this time; since the gate SCAN of the NMOS transistor M**1** in the light-emitting phase is 0, then the gate-source voltage of the NMOS transistor M**1** is $V_{DATA}+k\times$VDDP at this time, which may cause an excessively high gate-source voltage, thereby causing a reliability problem of gate breakdown. Furthermore, the coupling of the source to the gate of the driving MOS transistor MD is close to 1:1, leading to an excessively low input voltage range.

SUMMARY

[0010] A technical object to be achieved by the present invention is to solve the problem of static power consumption in writing in the existing pixel driving circuit of a source follower structure and to ensure that the voltage output range is as close to VDD as possible without the problem of gate breakdown caused by an excessively high gate-source voltage.

[0011] Based on the above technical object, the present invention provides a voltage-input pixel driving circuit for a microdisplay panel, the voltage-input pixel driving circuit including: a first transistor M**1**, a second transistor MR, a driving transistor MD, a coupling capacitor C_C, a light-emitting element, and a MUX signal gating unit;

[0012] wherein the first transistor M**1** includes a gate connected to a scan signal line SCAN of the microdisplay panel, a source connected to a data signal line DATA of the microdisplay panel, and a drain connected to a source of the second transistor MR; a gate of the second transistor MR is connected to an external bias voltage VBIAS, a drain of the second transistor MR is connected to a gate of the driving transistor MD, a source of the driving transistor MD is connected to one end of the light-emitting element, the other end of the light-emitting element is connected to a common

voltage VCOM, and a drain of the driving transistor MD is connected to the MUX signal gating unit;

[0013] the MUX signal gating unit outputs a low level signal when the scan signal line SCAN transmits a high level signal, and the MUX signal gating unit outputs a high level signal when the scan signal line SCAN transmits a low level signal; and

[0014] the second transistor MR is in a normally-on state under the action of the external bias voltage VBIAS.

[0015] In one embodiment, the MUX signal gating unit includes a third transistor ME**1** and a fourth transistor ME**2**, in which the third transistor ME**1** includes a gate connected to the scan signal line SCAN of the microdisplay panel, a source connected to the drain of the driving transistor MD, and a drain connected to a first driving signal DR**1**; and the fourth transistor ME**2** includes a gate connected to the scan signal line SCAN of the microdisplay panel, a source connected to the drain of the driving transistor MD, and a drain connected to a second driving signal DR**2**.

[0016] In one embodiment, the first transistor M**1**, the second transistor MR, the driving transistor MD, and the fourth transistor are all NMOS transistors; and the third transistor ME**1** is a PMOS transistor.

[0017] In one embodiment, the external bias voltage VBIAS connected to the gate of the second transistor MR satisfies VBIAS>MAX_V_{DATA}+V_{TH}, where MAX_V_{DATA} is the maximum voltage value of a signal transmitted by the data signal line of the microdisplay panel, and V_{TH} is the threshold voltage of the first transistor M**1**.

[0018] In one embodiment, the voltage value of the first driving signal DR**1** is greater than the voltage value of the second driving signal DR**2**, the first driving signal DR**1** is set to be an external driving voltage VDDP, and the second driving signal DR**2** is set to be grounded (GND).

[0019] In another aspect, the present invention provides a voltage-input pixel driving circuit for a microdisplay panel, the voltage-input pixel driving circuit including: a first transistor M**1**, a second transistor MR, a driving transistor MD, a coupling capacitor C_C, a light-emitting element, a MUX signal gating unit, and an adjustment capacitor C_S;

[0020] wherein the first transistor M**1** includes a gate connected to a scan signal line SCAN of the microdisplay panel, a source connected to a data signal line DATA of the microdisplay panel, and a drain connected to a source of the second transistor MR, a gate of the second transistor MR is connected to an external bias voltage VBIAS, a drain of the second transistor MR is connected to a gate of the driving transistor MD, a source of the driving transistor MD is connected to one end of the light-emitting element, the other end of the light-emitting element is connected to a common voltage VCOM, and a drain of the driving transistor MD is connected to the MUX signal gating unit; and one end of the adjustment capacitor C_S is connected to the gate of the driving transistor MD, and the other end thereof is connected to a fixed level;

[0021] the MUX signal gating unit outputs a low level signal when the scan signal line SCAN transmits a high level signal, and the MUX signal gating unit outputs a high level signal when the scan signal line SCAN transmits a low level signal; and

[0022] the second transistor MR is in a normally-on state under the action of the external bias voltage VBIAS.

[0023] In one embodiment, the MUX signal gating unit includes a third transistor ME**1** and a fourth transistor ME**2**, in which the third transistor MEI includes a gate connected to the scan signal line SCAN of the microdisplay panel, a source connected to the drain of the driving transistor MD, and a drain connected to a first driving signal DR**1**; and the fourth transistor ME**2** includes a gate connected to the scan signal line SCAN of the microdisplay panel, a source connected to the drain of the driving transistor MD, and a drain connected to a second driving signal DR**2**.

[0024] In one embodiment, the first transistor M**1**, the second transistor MR, the driving transistor MD, and the fourth transistor are all NMOS transistors; and the third transistor ME**1** is a PMOS transistor.

[0025] In one embodiment, the external bias voltage VBIAS connected to the gate of the second transistor MR satisfies VBIAS>MAX_V_{DATA}+V_{TH}, where MAX_V_{DATA} is the maximum voltage value of a signal transmitted by the data signal line of the microdisplay panel, and V_{TH} is the threshold voltage of the first transistor M**1**.

[0026] In one embodiment, the capacitance value of the adjustment capacitor C_S is greater than the capacitance value of the gate parasitic capacitance C_P of the driving transistor MD.

[0027] In comparison with the prior art, the inventive points of the present invention described in one or more embodiments of the present invention include the following.

[0028] 1. The voltage of drain of the pixel circuit driving transistor MD is adjusted from the fixed voltage connected to VDDP (power supply voltage) in the prior art to such a manner that the voltage of the drain is at a low level in the data writing phase and switched to a high level in the holding phase, thereby eliminating the static power consumption in the data writing phase.

[0029] 2. A MOS transistor MR is connected in series behind a switch transistor M**1**. The MOS transistor MR is in a normally-on state. Setting the gate voltage of the MOS transistor MR can ensure that the MOS transistor still works in a safe range when the gate voltage of the driving transistor MD exceeds VDDP.

[0030] 3. The pixel driving circuit of the present invention can expand the voltage range of the input data signal V_{DATA}.

[0031] The above-mentioned inventive points are throughout the technical solution of the present invention, and other features and advantages of the present invention will be described in the following description, and partly become obvious from the description or be understood by practicing the present invention. The objects and other advantages of the present invention can be achieved and obtained by the structures particularly indicated in the description, claims, and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032] The accompanying drawings are used to provide a further understanding of the present invention and constitute a part of the specification. Along with the examples of the present invention, the accompanying drawings are used to explain the present invention and are not a limitation of the present invention. In the accompanying drawings:

[0033] FIG. **1** is a schematic diagram of the circuit structure of a pixel driving circuit of a source follower structure in the prior art.

[0034] FIG. **2** is a schematic diagram of the circuit structure of a voltage-input pixel driving circuit in a first example of the present invention.

[0035] FIG. **3** is a schematic diagram of a common circuit structure of a MUX signal gating unit in the first example of the present invention.

[0036] FIG. **4** is a schematic diagram of the working time sequence of the voltage-input pixel driving circuit in the first example of the present invention.

[0037] FIG. **5** is a schematic diagram of the circuit structure of a voltage-input pixel driving circuit in a second example of the present invention.

[0038] FIG. **6** is a schematic diagram of the circuit structure of a voltage-input pixel driving circuit in a third example of the present invention.

[0039] FIG. **7** is a schematic diagram of the circuit structure of a voltage-input pixel driving circuit in a fourth example of the present invention.

[0040] FIG. **8** is a schematic diagram of the circuit structure of a voltage-input pixel driving circuit in a fifth example of the present invention.

[0041] FIGS. **9**A and **9**B are schematic diagrams of the circuit structure of a voltage-input pixel driving circuit in a sixth example of the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0042] In order to further clarify the objects, technical solutions, and advantages of the present invention, the present invention is further described in detail below with reference to the accompanying drawings.

[0043] Before the following detailed description, it may be advantageous to describe the definitions of some words and phrases used throughout the present invention. The terms "couple", "connect" and their derivatives refer to any direct or indirect communication or connection between two or more elements, regardless of whether these elements are in physical contact with each other. The terms "transmit", "receive", "communicate", and their derivatives encompass direct and indirect communication. The terms "include", "comprise", and their derivatives refer to including but being not limited to. The term "or" is inclusive and means and/or. The phrase "associated with" and its derivatives refer to including, being included in, interconnecting, comprising, being comprised in, connecting or connecting with, coupling or coupling with, communicating with, cooperating, interweaving, being in parallel, approaching, binding or binding with, having, having attributes of, having a relation or having a relation with, etc. The term "controller" refers to any device, system, or a part thereof that controls at least one operation. Such a controller can be implemented with hardware or a combination of hardware and software and/or firmware. The functions associated with any particular controller can be centralized or distributed, regardless of whether it is local or remote. The phrase "at least one", when used with a list of items, means that various combinations of one or more of the listed items may be used, and may involve only one of the items in the list. For example, "at least one of A, B, and C" includes any of the following combinations: A; B; C; A and B; A and C; B and C; and A, B, and C.

[0044] The first end and the second end of a resistor, capacitor, or inductor in the present invention are described only to distinguish the two connection ends of the device, so as to facilitate the description of the connection relationship between the device and other devices, and do not specifically indicate a certain end of the resistor, capacitor, or inductor in actual situations. Those skilled in the art should know that, when constructing an actual circuit, any end of the resistor, capacitor, or inductor in an actual device can be defined as the first end, and when the first end is defined, the other end of the device is automatically defined as the second end.

[0045] Definitions of other specific words and phrases are provided throughout the present invention. Those of ordinary skill in the art should understand that in many, if not most instances, such definitions apply to prior and future uses of such defined words and phrases.

[0046] In the present invention, the application combination of modules and the division level of sub-modules are merely used for illustration, and the application combination of modules and the division level of sub-modules may have various modes without departing from the scope of the present disclosure.

Example 1

[0047] FIG. **2** shows a voltage-input pixel driving circuit for a microdisplay panel according to the present example. The voltage-input pixel driving circuit includes a first transistor M**1** (**1**), a second transistor MR (**2**), a driving transistor MD (**3**), a coupling capacitor C_C (**4**), a light-emitting element (**5**), and a MUX signal gating unit (**6**).

[0048] In the pixel driving circuit, the first transistor M**1** (**1**) includes a gate connected to a scan signal line SCAN of the microdisplay panel, a source connected to a data signal line DATA of the microdisplay panel, and a drain connected to a source of the second transistor MR (**2**), a gate of the second transistor MR (**2**) is connected to an external bias voltage VBIAS, a drain of the second transistor MR (**2**) is connected to a gate of the driving transistor MD (**3**), a source of the driving transistor MD (**3**) is connected to one end of the light-emitting element (**5**), the other end of the light-emitting element (**5**) is connected to a common voltage VCOM, and a drain of the driving transistor MD (**3**) is connected to the MUX signal gating unit (**6**).

[0049] The MUX signal gating unit (**6**) includes a third transistor ME**1** (**7**) and a fourth transistor ME**2** (**8**), in which the third transistor ME**1** (**7**) includes a gate connected to the scanning signal line of the microdisplay panel, a source connected to the drain of the driving transistor MD (**3**), and a drain connected to a first driving signal DR**1**; and the fourth transistor ME**2** (**8**) includes a gate connected to the scanning signal line of the microdisplay panel, a source connected to the drain of the driving transistor MD (**3**), and a drain connected to a second driving signal DR**2**. As shown in FIG. **3**, the MUX signal gating unit (**6**) in the present example is configured such that each row of pixels shares one MUX signal gating unit (**6**), thereby saving the area of the integrated circuit layout occupied by the MUX signal gating unit (**6**). Namely, the MUX signal gating unit (**6**) is located outside the pixel array, and each row of pixel units shares one MUX signal gating unit, and thus the area of the pixel unit circuit is not increased additionally.

[0050] In the present example, the first transistor M**1** (**1**), the second transistor MR (**2**), the driving transistor MD (**3**), and the fourth transistor (**8**) are all NMOS transistors; and the third transistor ME**1** (**7**) is a PMOS transistor.

[0051] In the present example, the external bias voltage VBIAS connected to the gate of the second transistor MR (**2**) satisfies VBIAS>MAX_V_{DATA}+V_{TH}, where MAX_V_{DATA} is the maximum voltage value of a signal transmitted by the

data signal line of the microdisplay panel, and V_{TH} is the threshold voltage of the first transistor M1 (1). The threshold voltage is the turn-on voltage defined by the MOS transistor. Only when the gate-source voltage is greater than the threshold voltage, the MOS transistor has a significant current; when the gate-source voltage is less than the threshold voltage, the MOS transistor works in the subthreshold region or the turn-off region, and the current of the MOS transistor is very small at this time.

[0052] In the present example, the voltage value of the first driving signal DR1 is greater than the voltage value of the second driving signal DR2. In the present example, the first driving signal DR1 is set to be the external driving voltage VDDP, and the second driving signal DR2 is set to be grounded (GND).

[0053] In the present example, one end of the coupling capacitor C_C (4) is connected to the gate of the driving transistor MD (3), and the other end thereof is connected to the source of the driving transistor MD (3). The coupling capacitor C_C (4) is a capacitor of various types such as a MIM capacitor, a MOM capacitor, or a MOS capacitor.

[0054] The working process of the voltage-input pixel driving circuit in the present example is as follows.

[0055] Data voltage writing phase: at this time, the signal of the scanning signal line SCAN is at a high level, the first transistor M1 (1) and the fourth transistor ME2 (8) are turned on, and the third transistor ME1 (7) is turned off because it is a PMOS transistor; since the external bias voltage VBIAS connected to the gate of the second transistor MR (2) satisfies VBIAS>MAX_V_{DATA}+V_{TH}, the second transistor MR (2) is also turned on; at this time, the gate voltage (NODE_G) of the driving transistor MD (3) is V_{DATA}, and its source voltage (NODE_S) and drain voltage (NODE_D) are both grounded (GND) (the second driving signal DR2 is GND at this time), and thus static writing power consumption is not caused at this time;

[0056] Light-emitting phase of display device: at this time, the signal of the scanning signal line SCAN is at a low level, the first transistor M1 (1) is turned off, the fourth transistor ME2 (8) is turned off, and the third transistor ME1 (7) is turned on; in this situation, the drain (NODE_D) of the driving transistor MD (3) is equivalent to being short-circuited with the first driving signal DR1 (the first driving signal DR1 is connected to the external driving voltage VDDP); at the initial stage, the gate voltage of the driving transistor MD (3) is V_{DATA}, the source voltage of the driving transistor MD (3) is GND, and thus the driving transistor MD (3) is turned on and the source of the driving transistor MD (3) is charged;

[0057] Assuming that the final source voltage of the driving transistor MD (3) is V_{ANODE}, and taking the capacitive coupling into consideration and assuming that the parasitic capacitance of the gate of the driving transistor MD (3) is C_p, the gate voltage is V_{DATA}+k×V_{ANODE} (where k=C_C/(C_C+C_p), k<1); at this time, if V_{ANODE}≈VDDP, then the gate voltage of the driving transistor MD (3) is k×VDDP+V_{DATA}. Since the gate voltage of the second transistor MR (2) is VBIAS>MAX_V_{DATA}+V_{TH}, the voltage difference between the gate of the second transistor MR (2) and the gate of the driving transistor MD (3) is less than k×VDDP−V_{TH}, namely, the voltage difference therebetween does not exceed VDDP.

[0058] The pixel driving scheme in the present example can improve the display consistency problem caused by the variation of the threshold voltage V_{th} of the driving transistor MD (3). Assuming that the threshold voltage V_{th} of the driving transistor MD (3) increases due to its process, the current I_{MD} of the driving transistor MD (3) would decrease, so that V_{ANODE} would decrease. Since the voltage difference of the gate of the driving transistor MD (3) is V_{GS}(MD) =V_{DATA}−(1−)×V_{ANODE}, V_{GS}(MD) increases to offset current reduction caused by the increase of the threshold voltage V_{th}; conversely, assuming that the threshold voltage V_{th} of the driving transistor MD (3) decreases due to its process, V_{GS}(MD) decreases to offset current increase caused by the decrease of V_{th}.

[0059] In addition, since the second transistor MR (2) isolates the first transistor M1 (1) and the gate of the driving transistor MD (3), the leakage between the first transistor M1 (1) and the driving transistor MD (3) is prevented, and the coupling effect on the gate of the driving transistor MD (3) when the signal of the scanning signal line SCAN of the display panel jumps from a high level to a low level.

Example 2

[0060] FIG. 5 shows a voltage-input pixel driving circuit for a microdisplay panel according to the present example. The voltage-input pixel driving circuit includes a first transistor M1 (10), a second transistor MR (20), a driving transistor MD (30), a coupling capacitor C_C (40), a light-emitting element (50), a MUX signal gating unit (60), and an adjustment capacitor C_S (90).

[0061] In the pixel driving circuit, the first transistor M1 (10) includes a gate connected to a scan signal line SCAN of the microdisplay panel, a source connected to a data signal line DATA of the microdisplay panel, and a drain connected to a source of the second transistor MR (20), a gate of the second transistor MR (20) is connected to an external bias voltage VBIAS, a drain of the second transistor MR (20) is connected to a gate of the driving transistor MD (30), a source of the driving transistor MD (30) is connected to one end of the light-emitting element (50), the other end of the light-emitting element (50) is connected to a common voltage VCOM, and a drain of the driving transistor MD (30) is connected to the MUX signal gating unit (60).

[0062] The MUX signal gating unit (60) includes a third transistor ME1 (70) and a fourth transistor ME2 (80), in which the third transistor ME1 (70) includes a gate connected to the scanning signal line of the microdisplay panel, a source connected to the drain of the driving transistor MD (30), and a drain connected to a first driving signal DR1; and the fourth transistor ME2 (80) includes a gate connected to the scanning signal line of the microdisplay panel, a source connected to the drain of the driving transistor MD (30), and a drain connected to a second driving signal DR2. Namely, the MUX signal gating unit (60) is located outside the pixel array, and each row of pixel units shares one MUX signal gating unit, and thus the area of the pixel unit circuit is not increased additionally.

[0063] In the present example, the first transistor M1 (10), the second transistor MR (20), the driving transistor MD (30), and the fourth transistor (80) are all NMOS transistors; and the third transistor ME1 (70) is a PMOS transistor.

[0064] In the present example, the external bias voltage VBIAS connected to the gate of the second transistor MR (20) satisfies VBIAS>MAX_V_{DATA}+V_{TH}, where MAX_V_{DATA} is the maximum voltage value of a signal transmitted

by the data signal line of the microdisplay panel, and V_{TH} is the threshold voltage of the first transistor M1 (10).

[0065] In the present example, the voltage value of the first driving signal DR1 is greater than the voltage value of the second driving signal DR2. In the present example, the first driving signal DR1 is set to be the external driving voltage VDDP, and the second driving signal DR2 is set to be grounded (GND).

[0066] In the present example, one end of the coupling capacitor C_C (40) is connected to the gate of the driving transistor MD (30), and the other end thereof is connected to the source of the driving transistor MD (30). The coupling capacitor C_C (40) is a capacitor of various types such as a MIM capacitor, a MOM capacitor, or a MOS capacitor.

[0067] In the present example, an adjustment capacitor C_S (90) is provided at the gate of the driving transistor MD (30), one end of the adjustment capacitor C_S (90) is connected to the gate of the driving transistor MD (30), and the other end thereof is connected to a fixed level. In the present example, the other end thereof is grounded.

[0068] With addition of the adjustment capacitor C_S (90), the gate voltage increase amount of the driving transistor MD (30) resulting from source coupling of the driving transistor MD (30) becomes $C_C/C_C+C_S+C_p)\times V_{ANODE}$. By adjusting the capacitance ratio of the coupling capacitor C_C (40) and the adjustment capacitor C_S (90), the range of the gate input voltage of the driving transistor MD (30) can be adjusted.

Example 3

[0069] FIG. 6 shows a voltage-input pixel driving circuit for a microdisplay panel according to the present example. The voltage-input pixel driving circuit includes a first transistor M1 (10), a second transistor MR (20), a driving transistor MD (30), a coupling capacitor C_C (40), a light-emitting element (50), a MUX signal gating unit (60), an adjustment capacitor C_S (90), and a third transistor MP (100).

[0070] Compared with Example 2, a third transistor MP (100) is added in the present example. The source of the third transistor MP (100) is connected to the source of the driving transistor MD (30), and the gate of the third transistor MP (100) is connected to the drain of the third transistor MP (100) and grounded. The third transistor MP (100) has a function of protecting the source (NODE_S) of the driving transistor MD (30) from having an excessively low level. Namely, when the common voltage VCOM is at a negative level, the third transistor MP (100) prevents the source of the driving transistor MD (30) from having an excessively small negative level.

[0071] In addition to the embodiment provided in the example, the third transistor MP (100) can be incorporated in all other embodiments of the present invention. Since VCOM is generally a negative voltage, when the anode of the light-emitting element has a negative voltage, a large voltage difference is caused between the gate and source or the source and drain of the driving transistor MD, which affects the reliability of the driving transistor MD. With addition of the third transistor MP, if NODE_S has a relatively low negative voltage, the third transistor MP is turned on to change the level of NODE_S to close to GND, thereby avoiding a large voltage difference at any two ends of the transistor MD. In the process of normal light emission of the diode, since NODE_S is generally a positive voltage, the transistor MP is in the off state, and its normal operation is not affected.

Example 4

[0072] FIG. 7 shows a voltage-input pixel driving circuit for a microdisplay panel according to the present example. The voltage-input pixel driving circuit includes a first transistor M1 (1), a second transistor MR (2), a driving transistor MD (3), a coupling capacitor C_C (4), a light-emitting element (5), and a MUX signal gating unit (6).

[0073] In the pixel driving circuit, the first transistor M1 (1) includes a gate connected to a scan signal line SCAN of the microdisplay panel, a source connected to a data signal line DATA of the microdisplay panel, and a drain connected to a source of the second transistor MR (2), a gate of the second transistor MR (2) is connected to an external bias voltage VBIAS, a drain of the second transistor MR (2) is connected to a gate of the driving transistor MD (3), a source of the driving transistor MD (3) is connected to one end of the light-emitting element (5), the other end of the light-emitting element (5) is connected to a common voltage VCOM, and a drain of the driving transistor MD (3) is connected to the MUX signal gating unit (6).

[0074] The MUX signal gating unit (6) includes a third transistor ME1 (7) and a fourth transistor ME2 (8), in which the third transistor ME1 (7) includes a gate connected to the scanning signal line of the microdisplay panel, a source connected to the drain of the driving transistor MD (3), and a drain connected to a first driving signal DR1; and the fourth transistor ME2 (8) includes a gate connected to the scanning signal line of the microdisplay panel, a source connected to the drain of the driving transistor MD (3), and a drain connected to a second driving signal DR2. As shown in FIG. 3, the MUX signal gating unit (6) in the present example is configured such that each row of pixels shares one MUX signal gating unit (6), thereby saving the area of the integrated circuit layout occupied by the MUX signal gating unit (6). Namely, the MUX signal gating unit (6) is located outside the pixel array, and each row of pixel units shares one MUX signal gating unit, and thus the area of the pixel unit circuit is not increased additionally.

[0075] In the present example, the first transistor M1 (1), the second transistor MR (2), the driving transistor MD (3), and the fourth transistor (8) are all NMOS transistors; and the third transistor ME1 (7) is a PMOS transistor.

[0076] In the present example, the external bias voltage VBIAS connected to the gate of the second transistor MR (2) satisfies $VBIAS>MAX\_V_{DATA}+V_{TH}$, where MAX V_{DATA} is the maximum voltage value of a signal transmitted by the data signal line of the microdisplay panel, and V_{TH} is the threshold voltage of the first transistor M1 (1). The threshold voltage is the turn-on voltage defined by the MOS transistor. Only when the gate-source voltage is greater than the threshold voltage, the MOS transistor has a significant current; when the gate-source voltage is less than the threshold voltage, the MOS transistor works in the subthreshold region or the turn-off region, and the current of the MOS transistor is very small at this time.

[0077] In the present example, the voltage value of the first driving signal DR1 is greater than the voltage value of the second driving signal DR2. In the present example, the first

driving signal DR1 is set to be the external driving voltage VDDP, and the second driving signal DR2 is set to be grounded (GND).

[0078] In the present example, one end of the coupling capacitor C_C (4) is connected to the gate of the driving transistor MD (3), and the other end thereof is connected to the source of the driving transistor MD (3). The coupling capacitor C_C (4) is a capacitor of various types such as a MIM capacitor, a MOM capacitor, or a MOS capacitor.

[0079] In the present example, an adjustment capacitor C_S (9) is provided at the gate of the driving transistor MD (3), one end of the adjustment capacitor C_S (9) is connected to the gate of the driving transistor MD (3), and the other end thereof is connected to a fixed level. In the present example, the other end thereof is grounded.

[0080] In the present example, the pixel driving circuit further includes a third transistor M2 (10). The third transistor M2 (10) includes a source connected to the source of the driving transistor MD (3), a drain connected to an external reference voltage VREF, and a gate connected to the scan signal line SCAN of the microdisplay panel.

[0081] The working process of the voltage-input pixel driving circuit in the present example is as follows.

[0082] Data voltage writing phase: at this time, the signal of the scanning signal line SCAN is at a high level, the first transistor M1 (1) and the fourth transistor ME2 (8) are turned on, and the third transistor ME1 (7) is turned off because it is a PMOS transistor; since the external bias voltage VBIAS connected to the gate of the second transistor MR (2) satisfies VBIAS>MAX V_{DATA}+V_{TH}, the second transistor MR (2) is also turned on; at this time, the gate voltage (NODE_G) of the driving transistor MD (3) is V_{DATA}, its source voltage (NODE_S) is initialized to the VREF level, and its drain (NODE_D) is grounded (GND) (the second driving signal DR2 is GND at this time), and thus static writing power consumption is not caused at this time. The external reference voltage VREF may vary depending on application requirements. For example, in the present example, the external reference voltage VREF may be connected to the ground terminal GND.

[0083] Light-emitting phase of display device: at this time, the signal of the scanning signal line SCAN is at a low level, the first transistor M1 (1) is turned off, the fourth transistor ME2 (8) is turned off, and the third transistor ME1 (7) is turned on; in this situation, the drain (NODE_D) of the driving transistor MD (3) is equivalent to being short-circuited with the first driving signal DR1 (the first driving signal DR1 is connected to the external driving voltage VDDP); at the initial stage, the gate voltage of the driving transistor MD (3) is V_{DATA}, the source voltage of the driving transistor MD (3) is the external reference voltage VREF, and thus the driving transistor MD (3) is turned on and the source of the driving transistor MD (3) is charged;

[0084] Assuming that the final source voltage of the driving transistor MD (3) is V_{ANODE}, and taking the capacitive coupling into consideration and assuming that the parasitic capacitance of the gate of the driving transistor MD (3) is C_p, the gate voltage is V_{DATA}+k×V_{ANODE} (where k=C_C/(C_C+C_p), k<1); at this time, if V_{ANODE}≈VDDP, then the gate voltage of the driving transistor MD (3) is k×VDDP+V_{DATA}. Since the gate voltage of the second transistor MR (2) is VBIAS>MAX_V_{DATA}+V_{TH}, the voltage difference between the gate of the second transistor MR (2) and the gate of the driving transistor MD (3) is less than k×VDDP−V_{TH}, namely, the voltage difference therebetween does not exceed VDDP.

[0085] In addition, the second transistor MR (2) isolates the first transistor M1 (1) and the gate of the driving transistor MD (3), thus preventing the leakage between the first transistor M1 (1) and the driving transistor MD (3), and reducing the coupling effect on the gate of the driving transistor MD (3) when the signal of the scanning signal line SCAN of the display panel jumps from a high level to a low level.

Example 5

[0086] FIG. 8 shows a voltage-input pixel driving circuit for a microdisplay panel according to the present example. The voltage-input pixel driving circuit includes a first transistor M1 (1), a second transistor MR (2), a driving transistor MD (3), a coupling capacitor C_C (4), a light-emitting element (5), a MUX signal gating unit (6), and an adjustment capacitor C_S (9).

[0087] In the pixel driving circuit, the first transistor M1 (1) includes a gate connected to a scan signal line SCAN of the microdisplay panel, a source connected to a data signal line DATA of the microdisplay panel, and a drain connected to a source of the second transistor MR (2), a gate of the second transistor MR (2) is connected to an external bias voltage VBIAS, a drain of the second transistor MR (2) is connected to a gate of the driving transistor MD (3), a source of the driving transistor MD (3) is connected to one end of the light-emitting element (5), the other end of the light-emitting element (5) is connected to a common voltage VCOM, and a drain of the driving transistor MD (3) is connected to the MUX signal gating unit (6).

[0088] The MUX signal gating unit (6) includes a third transistor ME1 (7), in which the third transistor ME1 (7) includes a gate connected to the scanning signal line of the microdisplay panel, a source connected to the drain of the driving transistor MD (3), and a drain connected to a first driving signal DR1. As shown in FIG. 3, the MUX signal gating unit (6) in the present example is configured such that each row of pixels shares one MUX signal gating unit (6), thereby saving the area of the integrated circuit layout occupied by the MUX signal gating unit (6). Namely, the MUX signal gating unit (6) is located outside the pixel array, and each row of pixel units shares one MUX signal gating unit, and thus the area of the pixel unit circuit is not increased additionally.

[0089] In the present example, the first transistor M1 (1), the second transistor MR (2), and the driving transistor MD (3) are all NMOS transistors; and the third transistor ME1 (7) is a PMOS transistor.

[0090] In the present example, the external bias voltage VBIAS connected to the gate of the second transistor MR (2) satisfies VBIAS>MAX_V_{DATA}+V_{TH}, where MAX V_{DATA} is the maximum voltage value of a signal transmitted by the data signal line of the microdisplay panel, and V_{TH} is the threshold voltage of the first transistor M1 (1). The threshold voltage is the turn-on voltage defined by the MOS transistor. Only when the gate-source voltage is greater than the threshold voltage, the MOS transistor has a significant current; when the gate-source voltage is less than the threshold voltage, the MOS transistor works in the subthreshold region or the turn-off region, and the current of the MOS transistor is very small at this time.

[0091] In the present example, the first driving signal DR**1** is set to be the external driving voltage VDDP.

[0092] In the present example, one end of the coupling capacitor C_C (**4**) is connected to the gate of the driving transistor MD (**3**), and the other end thereof is connected to the source of the driving transistor MD (**3**). The coupling capacitor C_C (**4**) is a capacitor of various types such as a MIM capacitor, a MOM capacitor, or a MOS capacitor.

[0093] In the present example, an adjustment capacitor C_S (**9**) is provided at the gate of the driving transistor MD (**3**), one end of the adjustment capacitor C_S (**9**) is connected to the gate of the driving transistor MD (**3**), and the other end thereof is connected to a fixed level. In the present example, the other end thereof is grounded

[0094] In the present example, the pixel driving circuit further includes a third transistor M**2** (**8**), in which the third transistor M**2** (**8**) includes a source connected to the source of the driving transistor MD (**3**), a drain connected to an external reference voltage VREF, and a gate connected to the scanning signal line SCAN of the microdisplay panel. The external reference voltage VREF may vary depending on application requirements. For example, in the present example, the external reference voltage VREF may be connected to the ground terminal GND.

Example 6

[0095] As shown in FIGS. **9**A and **9**B, in the present example, a third transistor M**3** (**10**) is added based on the above-mentioned example 5.

[0096] As shown in FIG. **9**A, when the third transistor M**3** (**10**) is a PMOS transistor, the source of the driving transistor MD (**3**) is connected to the source of the third transistor M**3** (**10**), the drain of the third transistor M**3** (**10**) is connected to one end of the light-emitting element (**5**), and the other end of the light-emitting element (**5**) is connected to the common voltage VCOM. The gate of the third transistor M**3** (**10**) is connected to a first scan signal line SCAN.

[0097] As shown in FIG. **9**B, the drain of the third transistor M**3** (**10**) is connected to the source of the driving transistor MD (**3**), the source of the third transistor M**3** (**10**) is connected to one end of the light-emitting element (**5**), and the other end of the light-emitting element (**5**) is connected to the common voltage VCOM. The gate of the third transistor M**3** (**10**) is connected to a second scan signal line SCANB.

[0098] The second scan signal line SCANB has a high or low level opposite to that of the first scan signal line SCAN. Namely, when the first scan signal line SCAN is at a high level, the second scan signal line SCANB is at a low level; and when the first scan signal line SCAN is at a low level, the second scan signal line SCANB is at a high level.

[0099] The above description is merely specific implementations of the present invention, and the protective scope of the present invention is not limited thereto. Any modification or replacement of the present invention made by a skilled person who is familiar with the present technology and pertaining to the technical specifications described in the present invention should fall within the protective scope of the present invention.

What is claimed is:

1. A voltage-input pixel driving circuit for a microdisplay panel, comprising: a first transistor M**1**, a second transistor MR, a driving transistor MD, a coupling capacitor C_C, a light-emitting element, and a MUX signal gating unit;

wherein the first transistor M**1** comprises a gate connected to a scan signal line SCAN of the microdisplay panel, a source connected to a data signal line DATA of the microdisplay panel, and a drain connected to a source of the second transistor MR; a gate of the second transistor MR is connected to an external bias voltage VBIAS, a drain of the second transistor MR is connected to a gate of the driving transistor MD, a source of the driving transistor MD is connected to one end of the light-emitting element, the other end of the light-emitting element is connected to a common voltage VCOM, and a drain of the driving transistor MD is connected to the MUX signal gating unit;

the MUX signal gating unit outputs a low level signal when the scan signal line SCAN transmits a high level signal, and the MUX signal gating unit outputs a high level signal when the scan signal line SCAN transmits a low level signal; and

the second transistor MR is in a normally-on state under an the-action of the external bias voltage VBIAS.

2. The voltage-input pixel driving circuit according to claim **1**, wherein the MUX signal gating unit comprises a third transistor ME**1** and a fourth transistor ME**2**, wherein the third transistor ME**1** comprises a gate connected to the scan signal line SCAN of the microdisplay panel, a source connected to the drain of the driving transistor MD, and a drain connected to a first driving signal DR**1**; and the fourth transistor ME**2** comprises a gate connected to the scan signal line SCAN of the microdisplay panel, a source connected to the drain of the driving transistor MD, and a drain connected to a second driving signal DR**2**.

3. The voltage-input pixel driving circuit according to claim **2**, wherein the first transistor M**1**, the second transistor MR, the driving transistor MD, and the fourth transistor are all NMOS transistors; and the third transistor ME**1** is a PMOS transistor.

4. The voltage-input pixel driving circuit according to claim **1**, wherein the external bias voltage VBIAS connected to the gate of the second transistor MR satisfies $VBIAS>MAX\_V_{DATA}+V_{TH}$, where MAX_V_{DATA} is a maximum voltage value of a signal transmitted by the data signal line of the microdisplay panel, and V_{TH} is a threshold voltage of the first transistor M**1**.

5. The voltage-input pixel driving circuit according to claim **3**, wherein a voltage value of the first driving signal DR**1** is greater than a voltage value of the second driving signal DR**2**, the first driving signal DR**1** is set to be an external driving voltage VDDP, and the second driving signal DR**2** is set to be grounded, that is, to be GND.

6. A voltage-input pixel driving circuit for a microdisplay panel, comprising: a first transistor M**1**, a second transistor MR, a driving transistor MD, a coupling capacitor C_C, a light-emitting element, a MUX signal gating unit, and an adjustment capacitor C_S;

wherein the first transistor M**1** comprises a gate connected to a scan signal line SCAN of the microdisplay panel, a source connected to a data signal line DATA of the microdisplay panel, and a drain connected to a source of the second transistor MR, a gate of the second transistor MR is connected to an external bias voltage VBIAS, a drain of the second transistor MR is connected to a gate of the driving transistor MD, a source of the driving transistor MD is connected to one end of the light-emitting element, the other end of the light-

emitting element is connected to a common voltage VCOM, and a drain of the driving transistor MD is connected to the MUX signal gating unit; and one end of the adjustment capacitor C_S is connected to the gate of the driving transistor MD, and the other end thereof is connected to a fixed level;

the MUX signal gating unit outputs a low level signal when the scan signal line SCAN transmits a high level signal, and the MUX signal gating unit outputs a high level signal when the scan signal line SCAN transmits a low level signal; and

the second transistor MR is in a normally-on state under an action of the external bias voltage VBIAS.

7. The voltage-input pixel driving circuit according to claim **6**, wherein the MUX signal gating unit comprises a third transistor ME**1** and a fourth transistor ME**2**, wherein the third transistor ME**1** comprises a gate connected to the scan signal line SCAN of the microdisplay panel, a source connected to the drain of the driving transistor MD, and a drain connected to a first driving signal DR**1**; and the fourth transistor ME**2** comprises a gate connected to the scan signal line SCAN of the microdisplay panel, a source connected to the drain of the driving transistor MD, and a drain connected to a second driving signal DR**2**.

8. The voltage-input pixel driving circuit according to claim **7**, wherein the first transistor M**1**, the second transistor MR, the driving transistor MD, and the fourth transistor are all NMOS transistors; and the third transistor ME**1** is a PMOS transistor.

9. The voltage-input pixel driving circuit according to claim **6**, wherein the external bias voltage VBIAS connected to the gate of the second transistor MR satisfies VBIAS>MAX_V_{DATA}+V_{TH}, where MAX_V_{DATA} is a maximum voltage value of a signal transmitted by the data signal line of the microdisplay panel, and V_{TH} is a threshold voltage of the first transistor M**1**.

10. A display panel, wherein the display panel is a silicon-based LED panel or a silicon-based OLED panel, and the display panel uses the voltage-input pixel driving circuit according to claim **1** to drive pixels for display.

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