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INTEGRATED CIRCUIT COMPRISING AT LEAST ONE BIPOLAR TRANSISTOR AND A CORRESPONDING METHOD OF PRODUCTION

Abstract

A bipolar transistor includes a common collector region comprising a buried semiconductor layer and an annular well. A well region is surrounded by the annular well and delimited by the buried semiconductor layer. A first base region and a second base region are formed by the well region and separated from each other by a vertical gate structure. A first emitter region is implanted in the first base region, and a second emitter region is implanted in the second base region. A conductor track electrically couples the first emitter region and the second base region to configure the bipolar transistor as a Darlington-type device. Structures of the bipolar transistor may be fabricated in a co-integration with a non-volatile memory cell.

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Background/Summary

CROSS REFERENCE TO RELATED APPLICATIONS [0001] This application is a divisional of U.S. patent application Ser. No. 17/747,540, filed May 18, 2022, which claims the priority benefit of France Application for U.S. Pat. No. 2,105,334, filed on May 21, 2021, the contents of which are hereby incorporated by reference in their entireties to the maximum extent allowable by law.

TECHNICAL FIELD
[0002] The embodiments and implementations relate to integrated circuits, in particular bipolar transistors, and methods for the production of bipolar transistors.
BACKGROUND
[0003] A bipolar transistor generally includes a doped semiconductor base region of a first type, for example the p-type, a doped semiconductor collector region of a second type, for example the n-type, adjacent to the base region, and a doped semiconductor emitter region of the second type, adjacent to the base region.
[0004] When the semiconductor substrate in which the bipolar transistor is formed is doped with the first type, a doped well of the second type forming the collector region typically surrounds the base region, which makes it possible to electrically insulate the base region and the substrate with two opposite PN junctions.
[0005] Integrated circuits including principally “digital” electronic devices, such as logic circuits in complementary technology CMOS (Complementary Metal Oxide Semiconductors) and non-volatile memory circuits for storing digital data, may include bipolar transistors found, for example, in generator circuits (like a band gap circuit) with a reference voltage independent of the temperature.
[0006] The steps for manufacturing bipolar transistors in this type of integrated circuit are typically cointegrated with manufacturing steps of digital electrical devices, i.e., the steps executed simultaneously with steps provided for other digital elements, and not specifically dedicated to bipolar transistors.
[0007] For example, the formation of the collector region may be cointegrated in a step of forming an insulation region buried in the depth of the semiconductor substrate, as part of a triple well type structure.
[0008] The formation of the base region may be cointegrated in a step of forming a logic circuit transistor well.
[0009] The formation of the emitter region may be cointegrated into a step of forming source regions and drain regions of CMOS transistors.
[0010] Pooling the manufacturing steps can reduce manufacturing costs, but the resulting semiconductor regions of bipolar transistors are typically poorly optimized. The bipolar transistors may perform poorly as a result, in particular with a “beta” current gain β which may be less than 10, whereas a comparable bipolar transistor made by dedicated and optimized steps may have a current gain β of between 100 and 200.
[0011] The “Darlington” transistor configuration, i.e., a common collector configuration of at least

two bipolar transistors, wherein the emitter of an upstream bipolar transistor is connected to the base of a downstream bipolar transistor, makes it possible to form an equivalent bipolar transistor whose current gain β is greater. The equivalent current gain β of the Darlington configuration is given by a polynomial of order “n” of the value of the current gain β of a single bipolar transistor, “n” being the number of bipolar transistors in the Darlington configuration.

[0012] However, this type of configuration has the disadvantage of multiplying by “n” the space occupied by the Darlington configuration compared to a single bipolar transistor and multiplying by “n” the activation voltage (base-emitter voltage) relative to a single bipolar transistor. This becomes particularly problematic when “n” is greater than or equal to three ($n \geq 3$).

[0013] Consequently, there is a need for embodiments of bipolar transistors which perform well, in particular have a high current gain β, without increasing the space occupied by a bipolar transistor and limiting the value of the activation voltage.

SUMMARY

[0014] In this respect, according to one aspect an integrated circuit is proposed including at least one bipolar transistor arranged in and/or on a doped semiconductor substrate of a first type. The bipolar transistor includes: a common collector region comprising a buried semiconductor layer in the depth of the doped substrate of a second type opposite the first type, and a doped annular well of the second type joining the buried semiconductor layer; a doped semiconductor well of the first type surrounded by the annular well and delimited by the buried semiconductor layer, the doped semiconductor well of the first type containing a first base region and a second base region; a doped first emitter region of the second type located in the first base region, and a doped second emitter region of the second type located in the second base region; a conductor track for electrically coupling the first emitter region with the second base region; and a vertical gate structure extending vertically across the semiconductor well containing the base regions to the buried semiconductor layer so as to electrically insulate the first base region and the second base region.

[0015] In other words, a Darlington transistor type configuration with two bipolar transistors is proposed, but with a single “triple well” containing the two base regions, i.e., having the size of a standard form of a single bipolar transistor.

[0016] Indeed, the space occupied by the vertical gate structure, for mutually insulating the first base region and the second base region inside the well, is negligible in relation to the size of bipolar transistors. In particular, the space occupied by the vertical gate structure is much smaller than the space occupied for insulating the base regions in the standard manner of wells doped opposite the type of doping of the base regions.

[0017] According to one embodiment, the vertical gate structure comprises a trench filled with a conductive material electrically insulated by a dielectric shell on the bottom and sides of the trench.

[0018] According to one embodiment, the vertical gate structure further comprises a region implanted at the bottom of the trench, doped by the second type, occupying a space between the bottom of the trench and the buried semiconductor layer in the semiconductor well containing the base regions.

[0019] Indeed, it is possible that the trench filled with a conductive material in a dielectric shell reaches the buried semiconductor layer, in which case the electrical insulation between the two base regions is fully formed by the trench, in particular by the dielectric shell. In this case, in practice, it is possible that the trench does not reach the buried semiconductor layer, and in this case the vertical gate structure advantageously includes said region implanted between the bottom of the trench and the buried semiconductor layer. The electrical insulation between the two base regions is thus formed by the region implanted in the bottom of the trench and by the dielectric shell.

[0020] According to one embodiment, the vertical gate structure extends vertically into the semiconductor well containing the base regions from a front face of the semiconductor well containing the base regions and extends longitudinally, in a direction of the plane of the front face,

diametrically from one edge of the annular well surrounding the semiconductor well containing the base regions to the other.
[0021] According to one embodiment, the integrated circuit also includes said at least bipolar transistor, at least one non-volatile memory cell including a floating gate transistor and a buried access transistor with vertical gate, and wherein the semiconductor well containing the base regions has the same depth, the same composition and the same concentration of dopants as a well of the memory cell containing a region for forming the channel of the floating gate transistor.
[0022] The channel region of the floating gate transistor is generally the region between the source and drain regions of the floating gate transistor.
[0023] Apart from the fact that the semiconductor well containing the base regions of the bipolar transistor may be formed in cointegration with the well of the memory cell, the depth of the memory cell wells is advantageously lower than the triple wells of other types of embodiments. Furthermore, the concentration of dopants in the well of the memory cell is advantageously lower than the concentrations of triple wells of other types of embodiments, making it possible to increase the resistance of the base region, and consequently increase the voltage resistance of PN junctions formed with the well.
[0024] This results in an increase in the current gain β of the bipolar transistors formed in each base region. Indeed, the current gain β is inversely proportional to the concentration of dopants of the base and inversely proportional to the depth of the base (emitter-collector distance). However, the cointegration of the bipolar transistor with a non-volatile memory cell makes it possible to reduce the depth and the concentration of dopants in the well containing base regions.
[0025] According to one embodiment: the buried semiconductor layer of the common collector region has the same composition and the same depth as a buried semiconductor layer forming a source plane extending below the well of the memory cell; the annular well of the common collector region has the same composition and the same structure as an annular well surrounding the well of the memory cell and permitting electrical contact with the buried semiconductor layer forming the source plane; and the vertical gate structure electrically insulating the first base region and the second base region has the same structure and the same size as a gate structure of the buried access transistor with vertical gate.
[0026] According to one embodiment, said at least one bipolar transistor belongs to a temperature-independent reference voltage generating circuit.
[0027] According to another aspect, a method is proposed for manufacturing an integrated circuit in a doped semiconductor substrate of a first type, comprising producing at least one bipolar transistor, comprising: forming a common collector region comprising an implantation in the depth of the substrate of a buried semiconductor layer doped by second type opposite the first type, and an implantation of a doped semiconductor annular well of the second type joining the buried semiconductor layer; implanting a doped semiconductor well of the first type in a region surrounded by the annular well and delimited by the buried semiconductor layer; forming a vertical gate structure extending vertically through the doped semiconductor well of the first type to the buried semiconductor layer, so as to electrically insulate a first base region and a second base region in the doped semiconductor well of the first type; implanting a doped first emitter region of the second type in the first base region, and a doped second emitter region of the second type in the second base region; and forming a conductor track electrically coupling the first emitter region to the second base region.
[0028] In one embodiment, forming the vertical gate structure comprises etching a trench, forming a dielectric shell on the bottom and sides of the trench and filling the trench with an electrically conductive material.
[0029] In one embodiment, forming the vertical gate structure also comprises implanting a doped implanted region of the second type at the bottom of the trench, so as to occupy a space in the doped semiconductor well of the first type between the bottom of the trench and the buried

semiconductor layer.
[0030] In one embodiment, the vertical gate structure is formed so as to extend vertically in the doped semiconductor well of the first type from a front face of the doped semiconductor well of the first type, and to extend longitudinally in a direction of the plane of the front face, diametrically from one edge of the annular well surrounding the doped semiconductor well of the first type to the other.
[0031] In one embodiment, the method also includes manufacturing at least one non-volatile memory cell including a floating gate transistor and a buried access transistor with vertical gate, wherein implanting the doped semiconductor well of the first type is performed at the same time as implanting a well of the memory cell containing a channel region of the floating gate transistor.
[0032] In one embodiment: implanting the common collector region in the depth of the buried semiconductor layer is performed at the same time as implanting a buried semiconductor layer in the depth of a buried semiconductor layer which forms a source plane extending below the well of the memory cell; implanting the annular well of the common collector region is performed at the same time as implanting an annular well surrounding the well of the memory cell and permitting electrical contact with the buried semiconductor layer forming the source plane; and forming the vertical gate structure electrically insulating the first base region and the second base region is performed at the same time as forming a gate structure of the buried access transistor with vertical gate.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0033] Other advantages and features of the invention are given in the following detailed description of an embodiment and implementation, which are not to be considered limiting, and accompanying drawings, in which:
[0034] FIGS. **1** and **2** illustrate an exemplary embodiment of a bipolar transistor;
[0035] FIG. **3** illustrates a Darlington configuration with two transistors equivalent to the bipolar transistor;
[0036] FIG. **4** illustrates a temperature-independent voltage generator circuit (of a bandgap type); and
[0037] FIGS. **5** to **9** illustrate steps in the manufacture of a bipolar transistor carried out in cointegration with the manufacture of a non-volatile memory cell.
DETAILED DESCRIPTION
[0038] FIGS. **1** and **2** illustrate an exemplary embodiment of a bipolar transistor TBP of an integrated circuit CI. FIG. **1** illustrates a cross-sectional view of the bipolar transistor TPB in plane I-I of FIG. **2**, whereas FIG. **2** illustrates a top view of the bipolar transistor TBP in plane II-II of FIG. **1**.
[0039] The bipolar transistor TBP is formed in a doped semiconductor substrate PSUB of a first type, for example the p-type.
[0040] The bipolar transistor TBP is designed in the manner of a Darlington type configuration with two-bipolar-transistors, wherein a single “triple well” contains the two base regions, i.e., a Darlington configuration with two transistors with the size of a standard form of single bipolar transistor.
[0041] Reference is made to FIG. **3** which illustrates the Darlington configuration with two transistors equivalent to the bipolar transistor TBP. Each transistor includes a collector region C, a base region B**1**, B**2** and an emitter region E**1**, E**2**. The collector regions C of the two transistors are coupled together, the emitter region E**1** of the “upstream” transistor is coupled to the base region of the “downstream” transistor (the terms “upstream” and “downstream” are defined by this

coupling). The common collector region C forms the equivalent collector region of the bipolar transistor TBP, the base region B**1** of the upstream transistor forms the equivalent base region of the bipolar transistor TBP, and the emitter region E**2** of the transistor downstream forms the equivalent emitter region of the bipolar transistor TBP.

[0042] When the upstream transistor and the downstream transistor of the Darlington configuration each have the same current gain β.sub.0, so the equivalent current gain β of the bipolar transistor TBP can be expressed by β=β.sub.0.sup.2+2*β.sub.0. The equivalent base-emitter threshold voltage Vbe of the bipolar transistor TBP is the sum of the threshold voltages Vbe.sub.0 of the upstream and downstream transistors, i.e., Vbe=Vbe.sub.0+Vbe.sub.0. For example β=168 if β.sub.0=12, and Vbe=1.2V if Vbe.sub.0=0.6V.

[0043] Reference is once again made FIGS. **1** and **2**. The two base regions B**1**, B**2** are formed in the same well PW of a triple well structure. A triple well structure which makes it possible to electrically insulate the well PW with the same type of doping as the substrate PSUB (for example the p-type) by means of a doped insulation well NISO-NW of the opposite type (for example the n-type) encompassing the insulated well PW. Thus, PN junctions with opposite polarities formed with the insulation well NISO-NW make it possible to electrically insulate the well PW from the substrate PSUB.

[0044] The well PW containing the two base regions B**1**, B**2** is thus surrounded laterally, i.e., in x and y directions, by a doped annular well NW of the second type, and is delimited in depth, i.e., in vertical direction z, by a doped buried semiconductor layer NISO of the second type. The annular well NW extends in depth until it joins the buried semiconductor layer NISO.

[0045] The term “annular” denotes a ring form which is not necessarily circular, i.e. a geometric area delimited by an inner perimeter and an outer perimeter parallel to one another. In the view from above (FIG. **2**), the annular form of the well NW corresponds to a substantially square frame.

[0046] Furthermore, the buried semiconductor region NISO and the doped annular well NW both of the second type form the common collector region C. Highly doped contact zones C+ are formed in the annular well NW at a front face (in an xy plane), which make it possible to connect a metal terminal of collector C.

[0047] To electrically insulate the first base region B**1** contained in the well PW and the second base region B**2** also contained in the well PW, the bipolar transistor includes a vertical gate structure SGV extending vertically through the semiconductor well PW between the base regions B**1**, B**2** to the buried semiconductor layer NISO.

[0048] The vertical gate structure SGV comprises a trench filled with a conductive material GV electrically insulated by a dielectric shell OX on the bottom and sides of the trench.

[0049] This type of vertical gate structure SGV corresponds to a vertical gate structure of a buried transistor, used in particular as an access transistor TA (see, FIG. **9**) in non-volatile memory cells CEL (see, FIG. **9**) of integrated circuits.

[0050] The vertical gate structure SGV can thus be advantageously manufactured “free of charge” in conjunction with the corresponding manufacturing steps of the memory cell CEL. The vertical gate structure SGV will thus have the same structure (i.e., the same layout, and the same materials) and the same size (in particular the depth) as the gate of the buried access transistor with vertical gate TA (see, FIG. **9**).

[0051] In a first alternative (not explicitly shown in FIG. **1**), the trench filled with a conductive material GV has a depth which extends vertically through the well PW until it reaches, or penetrates, the buried semiconductor layer NISO. In this case, the dielectric shell OX and the conductive material GV which is left at a floating potential, allow the first base region B**1** and the second base region B**2** to be electrically insulated from one another.

[0052] In a second alternative (represented in FIGS. **1** and **2**), the trench filled with a conductive material GV has a depth which extends vertically into the well PW but does not reach the buried semiconductor region NISO. However, the vertical gate structure SGV may include an implanted

region NIMP at and about (for example extending from) the bottom of the trench, doped by the second type, joining the buried semiconductor layer NISO.
[0053] The implanted region NIMP thus occupies a space left in the semiconductor well PW containing the base regions, between the bottom of the trench and the buried semiconductor layer NISO and makes it possible to achieve electrical insulation between the two base regions B**1**, B**2**.
[0054] This second alternative corresponds in particular to the case of cointegrated manufacture with a buried access transistor TA with a vertical gate of a non-volatile memory cell CEL (see, FIG. **9**).
[0055] Thus, the vertical gate structure SGV extends vertically into the semiconductor well PW from the front face FA to the buried semiconductor layer NISO (visible in FIG. **1**).
[0056] Longitudinally, i.e., in a direction of the plane of the front face FA, for example in y-direction, the vertical gate structure SGV extends diametrically from one edge of the annular well NW to the other (visible in FIG. **2**).
[0057] Thus, the vertical gate structure SGV occupies a very small space in the well PW to mutually insulate two base regions B**1**, B**2** in the same well PW. This makes it possible to form two transistors arranged in a Darlington configuration in an area corresponding to a conventional design of a single bipolar transistor.
[0058] Lastly, a doped first emitter region E**1** of the second type is located in the first base region B**1**, and a doped second emitter region E**2** of the second type is located in the second base region B**2**.
[0059] A conductor track M**1**, for example formed by a metal track in a metal level of an interconnection part of the integrated circuit CI, makes it possible to form the Darlington configuration by electrically coupling the first emitter region E**1** (for example belonging to the "upstream" transistor of the Darlington configuration) with the second base region B**2** (for example belonging to the "downstream" transistor of the Darlington configuration).
[0060] The emitter regions E**1**, E**2**, as well as the contact zones B**1**+, B**2**+ of the respective base regions B**1**, B**2**, and the contact zones C+ of the common collector region C, are formed locally by highly concentrated implantations of dopants, at the front face FA in openings of lateral insulation regions STI.
[0061] The lateral insulation regions STI are, for example, of standard shallow trench insulation (STI) designs, which are not shown in the top view of FIG. **2** to improve readability.
[0062] Furthermore, as described in the following, in connection with FIGS. **5** to **9**, the manufacture of the bipolar transistor TBP can be carried out in cointegration with other manufacturing steps of the non-volatile memory cell CEL.
[0063] On the one hand, the cointegration has the economic advantage of manufacturing the bipolar transistor TBP without an additional step, i.e., without additional cost.
[0064] On the other hand, the cointegration with non-volatile memory technologies makes it possible to improve the performance of the bipolar transistor TBP, in addition and in combination with the quadratic increase of the current gain β of the Darlington configuration.
[0065] Indeed, the current gain β.sub.0 of one of the two transistors of the Darlington configuration, may be expressed as a function of (μ.sub.n/ μ.sub.p.Math.1/W.sub.b.Math.N.sub.e/N.sub.b), where μ.sub.n is the mobility of n-type carriers, μ.sub.p is the mobility of p-type carriers, W.sub.b is the width of the base region, N.sub.e is the concentration of the dopants of the emitter region, and N.sub.b is the concentration of dopants of the base region.
[0066] In other words, the current gain β.sub.0 is inversely proportional to the concentration of dopants of the base N.sub.b and inversely proportional to the width of the base W.sub.b (emitter-collector distance).
[0067] In the embodiment of the bipolar transistor TBP as represented in FIG. **1**, the width of the base W.sub.b corresponds substantially to the depth of the well PW, i.e. the distance between the

buried semiconductor layer NISO and the front face FA.
[0068] However, the depth of the memory cell wells is typically smaller than the depth of triple wells of other types of embodiments, in particular due to the size of the vertical gate region of the access transistors. In practice, a second depth implantation of a buried semiconductor layer is made above the buried semiconductor layer NISO. In the representations of the drawings, this second buried semiconductor layer belongs to the layer NISO. In addition, the concentration of dopants of the memory cells wells is typically lower than the concentrations in the triple wells of other embodiments, in particular in order to increase the voltage resistance of the PN junctions formed with the well.
[0069] Thus, by reducing the width of the base W.sub.b and by reducing the concentration of the base dopants N.sub.b due to the cointegration with the memory cell formation CEL, the current gain β.sub.0 of each of the two transistors of the Darlington configuration is increased.
[0070] For example, the current gain β.sub.0 may be substantially 12 in the case of cointegration with a memory cell CEL, representing more than 2 times the current gain of a bipolar transistor generally cointegrated with CMOS (Complementary Metal Oxide Semiconductors) logic transistors.
[0071] The equivalent current gain β of the bipolar transistor TBP, as previously expressed in relation to FIG. **3**, benefits from this gain proportionally and quadratically, which may be in the order of 30 times the current gain of a conventional bipolar transistor mentioned above.
[0072] The value of the current gain β≈170 of the bipolar transistor TBP described in relation to FIGS. **1** to **3**, can be obtained by a Darlington type configuration of three standard bipolar transistors, each having a current gain substantially equal to 5 and each having the same size as the bipolar transistor TBP. The base-emitter threshold voltage of the Darlington configuration with three conventional transistors is therefore 3*0.6V=1.8V.
[0073] Consequently, the bipolar transistor TBP described in relation to FIGS. **1** to **3** makes it possible to divide by three the size of such a standard design, while limiting the base-emitter threshold voltage Vbe to 1.2V.
[0074] In addition to the immediate advantage of reducing the size of the bipolar transistor TBP, this also has an advantage in terms of reliability, in particular in terms of the transistors matching. Indeed, matching errors may be the result of distant positions of corresponding transistors; however, having three times fewer transistors within a group of transistors also makes it possible to reduce the distance between the most distant transistors in the group and thus improve the matching.
[0075] In particular, the temperature-independent reference voltage generating circuits need high current gain and are sensitive to matching errors.
[0076] Reference is made in this respect to FIG. **4** which illustrates a circuit BGC adapted to generate a temperature-independent voltage (usually a bandgap voltage generator circuit). The circuit BGC includes two input branches of an adder ADD, each branch including bipolar transistors. A first branch includes a current generator injecting current into a collector of a diode-connected bipolar transistor, the emitter to ground. As a result, the base-emitter voltage V.sub.BE of this transistor provides a signal that decreases with temperature at one input of the adder ADD. A temperature-proportional current generator circuit V.sub.PTAT Gen generates a signal increasing with temperature on the other input of the adder ADD. The sum of the two signals V.sub.BE, KV.sub.T is substantially constant with the temperature and constitutes the temperature-independent reference voltage signal V.sub.REF(T).
[0077] In this type of circuit BGC, a low current gain β affects the accuracy, the precision, and variations with temperature quite significantly.
[0078] Consequently, the bipolar transistor TBP as described in relation to FIGS. **1** to **3** belongs advantageously to a temperature-independent reference voltage generating circuit BGC.
[0079] FIGS. **5** to **9** illustrate the steps and results of steps of an example of the method of

production of the bipolar transistor TBP as described above in connection with FIGS. **1** to **3**.
[0080] In this example, the bipolar transistor TBP is made entirely in cointegration with the manufacturing steps of memory cells CEL, made in the same semiconductor substrate PSUB, for example in doped silicon of the first type, typically the p-type.
[0081] FIG. **5** illustrates a result **500** of steps of manufacturing shallow insulation trenches STI, comprising typically the etching of openings referred to as “trenches” from the front face FA of the PSUB substrate and filling the trenches with a dielectric material such as silicon oxide.
[0082] The result **500** also illustrates the result of implantation steps of a “triple well” type structure in the bipolar transistor part TBP and in the memory cell part CEL.
[0083] The implantation steps of the “triple wells” thus include: [0084] a depth implantation of the buried semiconductor layer NISO of the common collector region C of the bipolar transistor TBP, at the same time as a depth implantation of a buried semiconductor layer NISOnvm for forming a source plane extending below a well PWnvm containing the memory cell CEL. The buried semiconductor layers NISO, NISOnvm are doped by a second type, opposite the first type, for example the n-type; [0085] an implantation of the annular well NW of the common collector region C of the bipolar transistor, at the same time as an implantation of an annular well NWnvm surrounding the well containing the memory cell PWnvm. The annular wells NW, NWnvm are implanted with energy making it possible to reach the depth of the semiconductor layers NISO, so as to form an insulating structure in continuity with said buried semiconductor layers NISO, NISOnvm.
[0086] The annular wells NW, NWnvm are doped by the second type, for example n-type; and
[0087] an implantation of the doped semiconductor well PW of the first type intended to contain the base regions B**1**, B**2** (see, FIG. **6**), at the same time as an implantation of a well of the memory cell PWnvm intended to contain in particular a channel region of the floating gate transistor FGT**1**, FGT**2** (see, FIG. **9**).
[0088] In particular, the dopants of doped wells PW, PWnvm of the first type, respectively, intended to contain the base regions B**1**, B**2** and the memory cell CEL, have a concentration between 2*10.sup.12 cm.sup.−3 and 3*10.sup.13 cm.sup.−3. This relatively low concentration is intended in particular to ensure a high avalanche voltage of the PN junctions in the part of the memory cell CEL, which advantageously makes it possible to increase the current gain β of the bipolar transistor TBP.
[0089] Furthermore, the depth of said wells PW, PWnvm, delimited by the vertical position of the buried semiconductor layers NISO, NISOnvm, is for example between 300 nm and 700 nm. This relatively small depth is provided in order to limit the etching time of the trenches TR, TRta (FIG. **6**) to approximately this depth, which advantageously makes it possible to increase the current gain β of the bipolar transistor TBP.
[0090] FIG. **6** illustrates the result of an etching step **600** to open the trenches TR, TRta in which the vertical gate structure electrically insulating the first base region B**1** and the second base region B**2** of the bipolar transistor and the vertical gate of the access transistor TA (FIG. **9**) of the memory cell CEL are formed.
[0091] An implantation is also performed at and about (for example, from the bottom of) the trenches TR, TRta, in the respective wells PW, PWnvm. Thus, respective implanted regions NIMP, NIMPta, doped by the second type, for example the n-type, occupy a space between the bottom of the trenches TR, TRta and the buried semiconductor layers NISO, NISOnvm.
[0092] The implantation of the implanted region NIMPta at the bottom of the trench TRta of the memory cell CEL makes it possible, in particular, to form a source region contacting the source plane NISOnvm, and this advantageously makes it possible to ensure the electrical insulation between the two base regions B**1**, B**2** in the well PW of the bipolar transistor TBP.
[0093] On the one hand, in the representation of FIG. **6**, the trenches TR, TRta are represented with the same depth. However, strictly speaking, the trench TR of the bipolar transistor TBP is slightly

deeper than the trench TRta of the memory cell CEL. Indeed, the trench TR of the bipolar transistor TBP passes through a lateral insulation region STI, and the anisotropic etching used to form the trenches TR, TRta may be faster in the dielectric material of the lateral insulation regions STI than in the crystalline silicon of the well PWnvm.

[0094] On the other hand, the implanted region NIMP initially from the bottom of the trench TR in the well PW of the bipolar transistor TBP is represented after diffusion, and thus extends from the bottom of the shallow insulation trenches STI to the buried semiconductor layer NISO.

[0095] This effectively provides electrical insulation between the first base region B**1** and the second base region B**2**. However, the structure within the trench TR, i.e., in particular the dielectric shell OX formed at step **700** described in relation to FIG. **7**, could by itself provide electrical insulation between the first base region B**1** and the second base region B**2** in the case where the deeper depth of the trench TR extends through to reach the buried semiconductor layer NISO region.

[0096] FIG. **7** illustrates a step **700** comprising a formation of a dielectric shell OX on the bottom and sides of the trench TR of the bipolar transistor TBP, at the same as forming a gate dielectric shell of OXta of the access transistor of the memory cell CEL.

[0097] Step **700** also includes filling to excess trenches TR, TRta with an electrically conductive material PO, for example polycrystalline silicon.

[0098] FIG. **8** illustrates the result **800** of a removal of the excess conductive material PO, i.e., the portion of conductive material PO covering the front face FA of the semiconductor substrate PSUB, typically by chemical-mechanical polishing.

[0099] Furthermore, floating gate structures SGF**1**, SGF**2** have been formed in the memory cell part CEL.

[0100] The floating gate structures SGF**1**, SGF**2** typically include a tunnel dielectric layer on the front face FA of the well PWnvm, a floating gate region on the tunnel dielectric, an inter-gate dielectric layer on the floating gate and a control gate region on the inter-gate dielectric layer.

[0101] FIG. **9** illustrates the result **900** of a step of implanting the second type of dopants, for example n-type, emitter regions E**1**, E**2**, collector contact zones C+ into openings of the shallow insulation trenches STI provided for this purpose, at the same time as a self-aligned implantation of source regions S and drain regions D on both sides of the floating gate structures FGT**1**, FGT**2**, and source plane contact zones SL NISOnvm.

[0102] Furthermore, an implantation of the first type of dopants, for example p-type, base region contact zones B**1**+, B**2**+ are formed in openings of the shallow insulation trench STI provided for this purpose in the respective base regions B**1**, B**2**, together with an implantation of substrate contact zones P+ in openings of the shallow insulation trench STI provided for this purpose in the substrate PSUB.

[0103] Furthermore, contact pillars are made on the strongly implanted regions B**1**+, B**2**+, C+, E**1**, E**2** in order to couple the first emitter region E**1** with the second base region B**2**+, for example by means of a metal track M**1**; and to form a base terminal B of the bipolar transistor TBP on the first base region B**1**+, an emitter terminal E of the bipolar transistor TBP on the second emitter region E**2**, and a collector terminal C of the bipolar transistor TBP on the collector contact zone C+.

[0104] At the same time, contact pillars are formed in the memory cell CEL in order to form bit line terminals BL**1**, BL**2** on the drain regions D, word line terminals WL on the conductive gate of the access transistor TA, control gate line terminals CGL**1**, CGL**2** on the control gates of the floating gate structures SGF**1**, SGF**2**, and a source plane terminal SL on the source plane contact area NWnvm, NISOnvm.

Claims

1. A method for manufacturing an integrated circuit in a semiconductor substrate doped by a first type, comprising: manufacturing a Darlington type bipolar transistor, comprising: forming a common collector region for a first transistor and a second transistor of said Darlington type bipolar transistor by implanting a buried semiconductor layer doped by a second type opposite the first type in the semiconductor substrate, and implanting a doped annular well of the second type joining the buried semiconductor layer; implanting a doped semiconductor well of the first type in a region surrounded by the annular well and delimited by the buried semiconductor layer; forming a vertical structure extending vertically through the doped semiconductor well to the buried semiconductor layer so as to electrically insulate a first base region of the first transistor and a second base region of the second transistor; implanting of a doped first emitter region of the second type for the first transistor in the first base region; implanting a doped second emitter region of the second type for the second transistor in the second base region; and forming a conductor track electrically coupling the first emitter region for the first transistor with the second base region for the second transistor.

2. The method according to claim 1, wherein forming the vertical structure comprises: etching a trench; forming a dielectric shell on a bottom and sides of the trench; and filling the trench with an electrically conductive material.

3. The method according to claim 2, wherein forming the vertical structure further comprises implanting a doped region of the second type in the doped semiconductor well to occupy a space between the bottom of the trench and the buried semiconductor layer.

4. The method according to claim 1, wherein the vertical structure extends vertically into the doped semiconductor well from a front face of the doped semiconductor well, and extends longitudinally, in a direction of a plane of the front face, diametrically from one edge to another edge of the doped annular well surrounding the doped semiconductor well.

5. The method according to claim 1, further comprising manufacturing a non-volatile memory cell including a floating gate transistor and a buried access transistor with a vertical gate: wherein implanting the doped semiconductor well is performed at a same time as implanting a well of the non-volatile memory cell containing a channel region of the floating gate transistor.

6. The method according to claim 5, wherein: implanting the buried semiconductor layer of the common collector region is performed at a same time as implanting a buried semiconductor layer forming a source plane extending below the well of the non-volatile memory cell; implanting the doped annular well of the common collector region is performed at a same time as implanting an annular well surrounding the well of the non-volatile memory cell which allows for electrical contact to be made with the buried semiconductor layer forming the source plane; and forming the vertical structure electrically insulating the first base region and the second base region is performed at a same time as forming the vertical gate of the buried access transistor.

7. A method for manufacturing an integrated circuit in a semiconductor substrate doped by a first type, comprising: forming trench isolations surrounding an area; forming a triple well structure in the semiconductor substrate including an annular well and a buried layer each doped by a second type and surrounding a well doped by the first type; etching a trench into the well doped by the first type; implanting in the well doped by the first type a region at the bottom of the trench doped by the second type; wherein the trench and region divide the well doped by the first type into first region and a second region; lining sidewalls and a bottom of the trench with an insulating layer; and filling the trench lined by the insulating layer with a conductive material.

8. The method of claim 7, further comprising forming a Darlington type bipolar transistor as the integrated circuit by: implanting first and second emitter regions doped by the second type in the first and second regions, respectively; implanting a collector contact region doped by the second type in the annular well; implanting first and second base regions doped by the first type in the first and second regions, respectively; electrically connecting the first emitter region to the second base

region; electrically connecting a collector terminal of the Darlington type bipolar transistor to the collector contact region; electrically connecting an emitter terminal of the Darlington type bipolar transistor to the second emitter region; and electrically connecting a control terminal of the Darlington type bipolar transistor to the first base region.

9. The method of claim 7, further comprising forming a non-volatile memory cell as the integrated circuit by: forming first and second floating gate structures over the first and second regions, respectively; implanting source and drain regions doped by the second type in each of the first and second regions on either side of the first and second floating gate structures, respectively; electrically connecting a word line to the conductive material in the trench; electrically connecting first and second bit lines to the drain regions in the first and second regions, respectively; and electrically connection first and second control gate lines to the first and second floating gate structures, respectively.

10. A method for manufacturing an integrated circuit in a semiconductor substrate doped by a first type which cointegrates a Darlington type bipolar transistor and a non-volatile memory cell as the integrated circuit, comprising: forming trench isolations surrounding a first area and a second area; forming, in each of the first and second areas, a triple well structure in the semiconductor substrate including an annular well and a buried layer each doped by a second type and surrounding a well doped by the first type; etching, in each of the first and second areas, a trench into the well doped by the first type; implanting, in each of the first and second areas, in the well doped by the first type a region at the bottom of the trench doped by the second type; wherein the trench and region divide the well doped by the first type into first region and a second region; lining sidewalls and a bottom of the trench in each of the first and second areas with an insulating layer; filling the trench lined by the insulating layer in each of the first and second areas with a conductive material; forming first and second floating gate structures for the non-volatile memory cell over the first and second regions, respectively, in the second area; implanting regions doped by the second type which form: first and second emitter regions in the first and second regions, respectively, in the first area; a collector contact region in the annular well in the first area; and source and drain regions in each of the first and second regions on either side of the first and second floating gate structures, respectively, in the second area; implanting regions doped by the first type which form: first and second base regions in the first and second regions, respectively, in the first area; for the Darlington type bipolar transistor: electrically connecting the first emitter region to the second base region; electrically connecting a collector terminal to the collector contact region; electrically connecting an emitter terminal to the second emitter region; and electrically connecting a control terminal to the first base region; and for the non-volatile memory cell: electrically connecting a word line to the conductive material in the trench; electrically connecting first and second bit lines to the drain regions in the first and second regions, respectively; and electrically connection first and second control gate lines to the first and second floating gate structures, respectively.