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Bank to bank data transfer

Abstract

The present disclosure includes apparatuses and methods to transfer data between banks of memory cells. An example includes a plurality of banks of memory cells and a controller coupled to the plurality of subarrays configured to cause transfer of data between the plurality of banks of memory cells via internal data path operations.

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Background/Summary

PRIORITY INFORMATION (1) This application is a Continuation of U.S. application Ser. No. 17/178,889, filed Feb. 18, 2021, which issues as U.S. Pat. No. 11,755,206, on Sep. 12, 2023, which is a Continuation of U.S. application Ser. No. 16/541,764, filed Aug. 15, 2019, which issued as U.S. Pat. No. 10,929,023 on Feb. 23, 2021, which is a Continuation of U.S. application Ser. No. 15/189,900, filed Jun. 22, 2016, which issued as U.S. Pat. No. 10,387,046 on Aug. 20, 2019, the contents of which are included herein by reference.

TECHNICAL FIELD
(1) The present disclosure relates generally to semiconductor memory and methods, and more particularly, to apparatuses and methods to bank to bank data transfer.
BACKGROUND
(2) Memory devices are typically provided as internal, semiconductor, integrated circuits in computers or other electronic systems. There are many different types of memory including volatile and non-volatile memory. Volatile memory can require power to maintain its data (e.g., host data, error data, etc.) and includes random access memory (RAM), dynamic random access memory (DRAM), static random access memory (SRAM), synchronous dynamic random access memory (SDRAM), and thyristor random access memory (TRAM), among others. Non-volatile memory can provide persistent data by retaining stored data when not powered and can include NAND flash

memory, NOR flash memory, and resistance variable memory such as phase change random access memory (PCRAM), resistive random access memory (RRAM), and magnetoresistive random access memory (MRAM), such as spin torque transfer random access memory (STT RAM), among others.

(3) Electronic systems often include a number of processing resources (e.g., one or more processors), which may retrieve and execute instructions and store the results of the executed instructions to a suitable location. A processor can comprise a number of functional units such as arithmetic logic unit (ALU) circuitry, floating point unit (FPU) circuitry, and a combinatorial logic block, for example, which can be used to execute instructions by performing an operation on data (e.g., one or more operands). As used herein, an operation can be, for example, a Boolean operation, such as AND, OR, NOT, NAND, NOR, and XOR, and/or other operations (e.g., invert, shift, arithmetic, statistics, among many other possible operations). For example, functional unit circuitry may be used to perform the arithmetic operations, such as addition, subtraction, multiplication, and division on operands, via a number of operations.

(4) A number of components in an electronic system may be involved in providing instructions to the functional unit circuitry for execution. The instructions may be executed, for instance, by a processing resource such as a controller and/or host processor. Data (e.g., the operands on which the instructions will be executed) may be stored in a memory array that is accessible by the functional unit circuitry. The instructions and/or data may be retrieved from the memory array and sequenced and/or buffered before the functional unit circuitry begins to execute instructions on the data. Furthermore, as different types of operations may be executed in one or multiple clock cycles through the functional unit circuitry, intermediate results of the instructions and/or data may also be sequenced and/or buffered. A sequence to complete an operation in one or more clock cycles may be referred to as an operation cycle. Time consumed to complete an operation cycle costs in terms of processing and computing performance and power consumption, of a computing apparatus and/or system.

(5) In many instances, the processing resources (e.g., processor and associated functional unit circuitry) may be external to the memory array, and data is accessed via a bus between the processing resources and the memory array to execute a set of instructions. Processing performance may be improved in a processor-in-memory device, in which a processor may be implemented internally and near to a memory (e.g., directly on a same chip as the memory array). A processing-in-memory device may save time by reducing and eliminating external communications and may also conserve power.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

(1) FIG. **1**A is a block diagram of an apparatus in the form of a computing system including a memory device in accordance with a number of embodiments of the present disclosure.

(2) FIG. **1**B is another block diagram of an apparatus in the form of a computing system including a memory device in accordance with a number of embodiments of the present disclosure.

(3) FIG. **1**C is a block diagram of a number of banks of a memory device in accordance with a number of embodiments of the present disclosure.

(4) FIG. **1**D is a block diagram of a bank section of a memory device in accordance with a number of embodiments of the present disclosure.

(5) FIG. **1**E is a block diagram of a number of bank sections of a memory device in accordance with a number of embodiments of the present disclosure.

(6) FIG. **2** is a schematic diagram illustrating sensing circuitry of a memory device in accordance with a number of embodiments of the present disclosure.

(7) FIG. **3** is a schematic diagram illustrating circuitry for data transfer in a memory device in accordance with a number of embodiments of the present disclosure.

DETAILED DESCRIPTION

(8) The present disclosure includes apparatuses and methods to transfer data between banks of memory cells. An example includes a plurality of banks of memory cells and a controller coupled to the plurality of subarrays configured to cause transfer of data between the plurality of banks of memory cells via internal data path operations.

(9) As described in more detail below, the embodiments can allow for data transfer between banks of memory cells on a data bus that is internal to a memory device. The data bus that is internal to a memory device, hereinafter referred to as “an internal data bus” can couple the memory cells together. The data transfer between banks of memory cells can occur on the internal data bus without using an external data bus. An external data bus can be used to transfer data between the banks of memory cells and other apparatuses external to the banks of memory cells, such as a host and/or another memory device, for example. The transfer of data between the banks of memory cells and other apparatuses external to the banks of memory cells can use a data path that includes the internal data bus and the external data bus. Embodiments of the present disclosure can allow for data transfer between banks of memory cells on an internal data bus without transferring data on an external data bus.

(10) In the following detailed description of the present disclosure, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration how one or more embodiments of the disclosure may be practiced. These embodiments are described in sufficient detail to enable those of ordinary skill in the art to practice the embodiments of this disclosure, and it is to be understood that other embodiments may be utilized and that process, electrical, and structural changes may be made without departing from the scope of the present disclosure.

(11) As used herein, designators such as “X”, “Y”, “N”, “M”, etc., particularly with respect to reference numerals in the drawings, indicate that a number of the particular feature so designated can be included. It is also to be understood that the terminology used herein is for the purpose of describing particular embodiments only, and is not intended to be limiting. As used herein, the singular forms “a”, “an”, and “the” can include both singular and plural referents, unless the context clearly dictates otherwise. In addition, “a number of”, “at least one”, and “one or more” (e.g., a number of memory arrays) can refer to one or more memory arrays, whereas a “plurality of” is intended to refer to more than one of such things. Furthermore, the words “can” and “may” are used throughout this application in a permissive sense (i.e., having the potential to, being able to), not in a mandatory sense (i.e., must). The term “include,” and derivations thereof, means “including, but not limited to”. The terms “coupled” and “coupling” mean to be directly or indirectly connected physically or for access to and movement (transmission) of commands and/or data, as appropriate to the context. The terms “data” and “data values” are used interchangeably herein and can have the same meaning, as appropriate to the context.

(12) The figures herein follow a numbering convention in which the first digit or digits correspond to the figure number and the remaining digits identify an element or component in the figure. Similar elements or components between different figures may be identified by the use of similar digits. For example, 108 may reference element “08” in FIG. **1**, and a similar element may be referenced as 208 in FIG. **2**. As will be appreciated, elements shown in the various embodiments herein can be added, exchanged, and/or eliminated so as to provide a number of additional embodiments of the present disclosure. In addition, the proportion and/or the relative scale of the elements provided in the figures are intended to illustrate certain embodiments of the present disclosure and should not be taken in a limiting sense.

(13) FIG. **1**A is a block diagram of an apparatus in the form of a computing system **100** including a memory device **120** in accordance with a number of embodiments of the present disclosure. As

used herein, a memory device **120**, controller **140**, channel controller **143**, bank arbiter **145**, high speed interface (HSI) **141**, memory array **130**, sensing circuitry **150**, and/or a number of additional latches **170** might also be separately considered an "apparatus."

(14) As used herein, the additional latches are intended to provide additional functionalities (e.g., peripheral amplifiers) that sense (e.g., read, store, cache) data values of memory cells in an array and that are distinct from the sense amplifiers of the sensing component stripes described herein (e.g., as shown at **206** in FIG. **2** and at corresponding reference number in FIG. **3**). As such, the additional latches can be included in a "latch component **170**". For example, latches of the latch component **170** can be located on a periphery of a bank **121** of the memory device, as shown for latch stripe **172** in FIG. **1**D and latch component **170** in FIG. **1**E. In contrast, the sense amplifiers located in a plurality of sensing component stripes **124** are physically associated with each subarray **125** of memory cells in the bank **121**, as shown in FIGS. **1**D and **1**E.

(15) System **100** in FIG. **1**A includes the host **110** coupled (e.g., connected) to memory device **120**, which includes a memory array **130**. Host **110** can be a host system such as a personal laptop computer, a desktop computer, a digital camera, a smart phone, or a memory card reader, among various other types of hosts. Host **110** can include a system motherboard and/or backplane and can include a number of processing resources (e.g., one or more processors, microprocessors, or some other type of controlling circuitry). The system **100** can include separate integrated circuits or both the host **110** and the memory device **120** can be on the same integrated circuit. The system **100** can be, for instance, a server system and/or a high performance computing (HPC) system and/or a portion thereof. Although the examples shown in FIGS. **1**A-**1**D illustrate a system having a Von Neumann architecture, embodiments of the present disclosure can be implemented in non-Von Neumann architectures, which may not include one or more components (e.g., CPU, ALU, etc.) often associated with a Von Neumann architecture.

(16) For clarity, the system **100** has been simplified to focus on features with particular relevance to the present disclosure. The memory array **130** can be a DRAM array, SRAM array, STT RAM array, PCRAM array, TRAM array, RRAM array, NAND flash array, and/or NOR flash array, among other types of arrays. The array **130** can include memory cells arranged in rows coupled by access lines (which may be referred to herein as word lines or select lines) and columns coupled by sense lines (which may be referred to herein as data lines or digit lines). Although a single array **130** is shown in FIG. **1**, embodiments are not so limited. For instance, memory device **120** may include a number of arrays **130** (e.g., a number of banks of DRAM cells, NAND flash cells, etc.).

(17) The memory device **120** can include address circuitry **142** to latch address signals provided over a combined data/address bus **156** (e.g., an I/O bus connected to the host **110**) by I/O circuitry **144** (e.g., provided to external ALU circuitry and/or to DRAM DQs via local I/O lines and global I/O lines). As used herein, DRAM DQs can enable input of data to and/or output of data from a bank (e.g., from and/or to the controller **140** and/or host **110**) via a bus (e.g., data bus **156**). During a write operation, a voltage (high=1, low=0) can be applied to a DQ (e.g., a pin). This voltage can be translated into an appropriate signal and stored in a selected memory cell. During a read operation, a data value read from a selected memory cell can appear at the DQ once access is complete and the output enable signal is asserted (e.g., by the output enable signal being low). At other times, DQs can be in a high impedance state, such that the DQs do not source or sink current and do not present a signal to the system. This also may reduce DQ contention when two or more devices (e.g., banks) share a combined data/address bus, as described herein.

(18) Status and exception information can be provided from the controller **140** of the memory device **120** to a channel controller **143** (shown in FIG. **1**B), for example, through a HSI out-of-band (OOB) bus **157**, which in turn can be provided from the channel controller **143** to the host **110**. The channel controller **143** can include a logic component **160** to allocate a plurality of locations (e.g., controllers for subarrays) in the arrays of each respective bank to store bank commands, application instructions (e.g., for sequences of operations), and arguments (PIM commands) for the various

banks associated with operations of each of a plurality of memory devices (e.g., **120-1**, . . . , **120**-N as shown in FIG. **1**B). The channel controller **143** can send commands (e.g., PIM commands) to the plurality of memory devices **120-1**, . . . , **120-**N to store those program instructions within a given bank of a memory device.

(19) Address signals are received through address circuitry **142** and decoded by a row decoder **146** and a column decoder **152** to access the memory array **130**. Data can be sensed (read) from memory array **130** by sensing voltage and/or current changes on sense lines (digit lines) using a number of sense amplifiers, as described herein, of the sensing circuitry **150**. A sense amplifier can read and latch a page (e.g., a row) of data from the memory array **130**. Additional compute circuitry, as described herein, can be coupled to the sensing circuitry **150** and can be used in combination with the sense amplifiers to sense, store (e.g., cache and/or buffer), perform compute functions (e.g., operations), and/or move data. The I/O circuitry **144** can be used for bi-directional data communication with host **110** over the data bus **156** (e.g., a 64 bit wide data bus). The write circuitry **148** can be used to write data to the memory array **130**.

(20) Controller **140** (e.g., bank control logic and sequencer) can decode signals (e.g., commands) provided by control bus **154** from the host **110**. These signals can include chip enable signals, write enable signals, and/or address latch signals that can be used to control operations performed on the memory array **130**, including data sense, data store, data movement (e.g., copying, transferring, and/or transporting data values), data write, and/or data erase operations, among other operations. In various embodiments, the controller **140** can be responsible for executing instructions from the host **110** and accessing the memory array **130**. The controller **140** can be a state machine, a sequencer, or some other type of controller. The controller **140** can control shifting data (e.g., right or left) in a row of an array (e.g., memory array **130**).

(21) Examples of the sensing circuitry **150** are described further below (e.g., in FIGS. **2** and **3**). For instance, in a number of embodiments, the sensing circuitry **150** can include a number of sense amplifiers and a number of compute components, which may serve as an accumulator and can be used to perform operations in each subarray (e.g., on data associated with complementary sense lines).

(22) In a number of embodiments, the sensing circuitry **150** can be used to perform operations using data stored in memory array **130** as inputs and participate in movement of the data for copy, transfer, writing, logic, and/or storage operations to a different location in the memory array **130** without transferring the data via a sense line address access (e.g., without firing a column decode signal). As such, various compute functions can be performed using, and within, sensing circuitry **150** rather than (or in association with) being performed by processing resources external to the sensing circuitry **150** (e.g., by a processor associated with host **110** and/or other processing circuitry, such as ALU circuitry, located on device **120**, such as on controller **140** or elsewhere).

(23) In various previous approaches, data associated with an operand, for instance, would be read from memory via sensing circuitry and provided to external ALU circuitry via I/O lines (e.g., via local I/O lines and/or global I/O lines) and/or an external data bus (e.g., data bus **156** in FIG. **1**B). The external ALU circuitry could include a number of registers and would perform compute functions using the operands, and the result would be transferred back to the array via the I/O lines. In contrast, in a number of embodiments of the present disclosure, sensing circuitry **150** is configured to perform operations on data stored in memory array **130** and store the result back to the memory array **130** without enabling an I/O line (e.g., a local I/O line) coupled to the sensing circuitry **150**. In various embodiments, methods, and apparatuses are provided which can function as a PIM RAM. In PIM RAM operation it is useful to transfer data between banks without using a data bus external to the die. The sensing circuitry **150** can be formed on pitch with the memory cells of the array. The latch component **170** can include latches, as described herein, and can be coupled to the sensing circuitry **150** via a shared I/O line, but be distinct from the sensing circuitry **150**. In various embodiments, methods and apparatuses are provided to achieve internal data

movement using a minimum column to column delay (tCCD)
(24) As such, in a number of embodiments, circuitry external to array **130** and sensing circuitry **150** is not needed to perform compute functions as the sensing circuitry **150** can perform the appropriate operations to perform such compute functions without the use of an external processing resource. Therefore, the sensing circuitry **150** may be used to complement or to replace, at least to some extent, such an external processing resource (or at least the bandwidth consumption of such an external processing resource).
(25) However, in a number of embodiments, the sensing circuitry **150** may be used to perform operations (e.g., to execute instructions) in addition to operations performed by an external processing resource (e.g., host **110**). For instance, host **110** and/or sensing circuitry **150** may be limited to performing only certain operations and/or a certain number of operations.
(26) Enabling an I/O line can include enabling (e.g., turning on, activating) a transistor having a gate coupled to a decode signal (e.g., a column decode signal) and a source/drain coupled to the I/O line. However, embodiments are not limited to not enabling an I/O line. For instance, in a number of embodiments, the sensing circuitry (e.g., **150**) can be used to perform operations without enabling column decode lines of the array; however, the local I/O line(s) may be enabled in order to transfer a result to a suitable location other than back to the array **130** (e.g., to an external register). Enabling (e.g., firing) a DQ pin can similarly consume significant power and time (e.g., require additional clock cycles (tck) for data transfers).
(27) FIG. **1**B is a block diagram of another apparatus architecture in the form of a computing system **100** including a plurality of memory devices **120-1**, . . . **120-**N coupled to a host **110** via a channel controller **143** in accordance with a number of embodiments of the present disclosure. In at least one embodiment, the channel controller **143** may be coupled to and integrated with the plurality of banks of the memory device **120** and/or the channel controller **143** may be coupled to and integrated with the host **110**. The channel controller **143** can be coupled to each of the plurality of banks of the memory device via an address and control (A/C) bus **154**, which in turn can be coupled to the host **110**. The channel controller **143** can also be coupled to each of the plurality of banks via a combined data/address bus **156**, which in turn can be coupled to the host **110**. In addition, the channel controller **143** can be coupled to each of the plurality of banks via an OOB bus **157** associated with the HSI **141**, also referred to herein as a status channel interface, which is configured to report status, exception and other data information to the channel controller **143** to exchange with the host **110**.
(28) The channel controller **143** can receive the status and exception information from the HSI **141** associated with a bank arbiter **145** associated with each of the plurality of banks. The bank arbiter **145** can sequence and control data movement within the plurality of banks (e.g., Bank zero (0), Bank one (1), . . . , Bank six (6), Bank seven (7), etc., as shown in FIG. **1**B). A controller **140** can be associated with each particular bank (e.g., Bank 0, . . . , Bank 7) in a given memory device **120** and can decode signals provided by control bus **154** from the host **110**. Each of the plurality of banks can include the controller **140** and other components, including an array of memory cells **130** and sensing circuitry **150**, and/or latch component **170**, etc.
(29) For example, each of the plurality of banks (e.g., in a plurality of memory devices **120-1**, **120-2**, . . . , **120-**N each having a plurality of banks as shown in FIG. **1**B) can include address circuitry **142** to latch address signals provided over a portion of a combined data/address bus **156** (e.g., an I/O bus) through I/O circuitry **144**. Status and/or exception information can be provided from the controller **140** associated with (e.g., on pitch and/or on chip with) each bank to the channel controller **143**, using the OOB bus **157**, which in turn can be provided from the plurality of banks to the host **110**. For each of the plurality of banks (e.g., Bank 0, . . . , Bank 7) address signals can be received through address circuitry **142** and decoded by a row decoder **146** and a column decoder **152** to access the memory array **130**. Data can be read from memory array **130** by sensing voltage and/or current changes on the sense lines using sensing circuitry **150**. The sensing circuitry **150** can

read and latch a page (e.g., row) of data from the memory array **130**. The I/O circuitry **144** can be used for bi-directional data communication with host **110** over the data bus **156**. The write circuitry **148** is used to write data to the memory array **130** and the OOB bus **157** can be used to report status and/or exception information to the channel controller **143**.

(30) In some embodiments, the channel controller **143** can send commands to the plurality of banks (e.g., Bank 0, . . . , Bank 7) and field return results and/or data from such operations. As described herein, the return results and/or data can be returned to the channel controller **143** via the OOB bus **157** associated with the status channel interface on each of the plurality of banks.

(31) As shown in FIG. **1**B, the channel controller **143** can receive the status and/or exception information from a HSI **141** (also referred to herein as a status channel interface) associated with a bank arbiter **145** in each of the plurality of memory devices **120-1**, . . . , **120**-N. In the example of FIG. **1**B, each of the plurality of memory devices **120-1**, . . . , **120**-N can include a bank arbiter **145** to sequence control and data with a plurality of banks (e.g., Bank 0, . . . , Bank 7, etc.). Each of the plurality of banks can include a controller **140** and other components, including an array of memory cells **130** and sensing circuitry **150**, logic circuitry **170**, etc., as described in connection with FIG. **1**A.

(32) The channel controller **143** can include one or more local buffers **159** to store program instructions and can include logic **160** to allocate a plurality of locations (e.g., subarrays or portions of subarrays) in the arrays of each respective bank to store bank commands, and arguments (e.g., PIM commands) for the various banks associated with operation of each of the plurality of memory devices **120-1**, . . . , **120**-N. The channel controller **143** can send commands (e.g., PIM commands) to the plurality of memory devices **120-1**, . . . , **120**-N to store those program instructions within a given bank of a memory device. These program instructions and PIM commands may need to be moved in a bank to bank data transfer (BBT) within a memory device.

(33) As in FIG. **1**A, a controller **140** (e.g., bank control logic and/or sequencer) associated with any subarray in a particular bank (e.g., Bank 0, . . . , Bank 7, etc.) in a given memory device (e.g., **120-1**, . . . , **120**-N) can decode signals provided by control bus **154** from the host **110**. These signals can include chip enable signals, write enable signals, and/or address latch signals that are used to control operations performed on the memory array **130**, including data read, data write, data copy, data movement, and/or data erase operations. In various embodiments, the controller **140** is responsible for executing instructions from the host **110**.

(34) FIG. **1**C is a block diagram of a number of banks of a memory device in accordance with a number of embodiments of the present disclosure. In FIG. **1**C, banks **121-0**, . . . , **121-7** are coupled together via internal data bus **186**. Internal data bus **186** can include a number of data paths that allow for data transfer between banks **121-0**, . . . , **121-7**. Internal data bus **186** can include a number of buffers (e.g., a number of bidirectional buffers **180-1**, . . . , **180**-T) for managing data transfers between banks **121-0**, . . . , **121-7** and a number of data multiplexer (mux) buffers **182-1** and **182-2** for temporarily storing data as it is transferred between banks **121-0**, . . . , **121-7**). Internal data bus **186** can be coupled to an external data bus (e.g. data bus **156** in FIG. **1**B) and/or a shared I/O line (e.g., shared I/O line **355** in FIG. **3**) via a number of DQs **184-0**, . . . , **184-7**. In various embodiments, data can be transferred between banks **121-0**, . . . , **121-7** via internal data bus **186**. Previously data could be transferred on an external data bus from banks **121-0**, . . . , **121-7** to other apparatuses external to banks **121-0**, . . . , **121-7** via the number of DQs **184-0**, . . . , **184-7**. Thus, in a number of embodiments, data can be transferred between banks **121-0**, . . . , **121-7** without operation the number of DQs **184-0**, . . . , **184-7**.

(35) Data can be transferred via internal data bus **186** by performing internal data path operations that include a bank to bank data transfer command that is sent to the banks **121-0**, . . . , **121-7** from the channel controller. The bank to bank data transfer command can include source bank information and destination bank information. The source bank information and destination bank information can be included on any of the address bits of a command. For example, the source

bank information can be included in a first number of bits, such as bank address bits (e.g., BA<2:0>) of the command, and the destination bank information can be included in a second number of bits, such as column address bits (e.g., CA<2:0>) of the command. Also, a number of additional address pins can be added allowing the source bank information and/or the destination bank information to be included in address bits on the additional address pins. In various embodiments, the bank to bank data transfer commands can be sent from the channel controller to banks **121-0**, . . . , **121-7** with reduced latency as compared to performing a silent read command followed by a silent write command. The reduced latency with performing the bank to bank data transfer commands can be associated with knowing the source bank and the destination bank when the command is issued. For example, a bank to bank data transfer command can be performed every 4 clock cycles when performing a number of bank to bank data transfers from a same source bank because the bank to bank data transfer commands do not have latency or burst length delays caused by firing the number of DQs **184-0**, . . . , **184-7**. The latency associated with performing a number of bank to bank data transfers from a same source bank can be 4 clock cycles because the bank to bank data transfer command latency is due to time for write to read (tWTR) delay and does not include read latency.

(36) In various embodiments, data can be transferred between banks **121-0**, . . . , **121-7** via internal data bus **186** by performing a silent read command followed by a silent write command. A silent read command can cause data to be transferred from one of the banks **121-0**, . . . , **121-7** (e.g., a source bank) via internal data bus **186** to one of the data mux **182-1** and **182-2** and/or a number of bidirectional buffers **180-1**, . . . , **180-**T. The silent read command can include performing a read operation from a bank that is shunted from providing the data to the DQs **184-0**, . . . , **184-7**. The silent read operation can be performed without firing the DQs **184-0**, . . . , **184-7**. The silent read command transfers data only on internal data bus **186** and not on data paths external to internal data bus **186**. The silent write command can be performed following the silent read command to transfer the data stored in one of the data mux **182-1** and **182-2** and/or a number of bidirectional buffers **180-1**, . . . , **180-**T to one of the banks **121-0**, . . . , **121-7** (e.g., a destination bank). The silent write command can be performed without firing the DQs **184-0**, . . . , **184-7**. The silent write command transfers data only on internal data bus **186** and not on data paths external to internal data bus **186**. The silent write command that follows the silent read command can be performed with reduced latency by redefining the silent write commands to bypass the write latency. The column select can be fired during the silent write command similarly to filing the column select during the silent read command. For example, the silent read to silent write command delay can be 4 clock cycles and the silent write to silent read command delay can be 4 clock cycles resulting in a silent read command being performed every 8 clock cycles. The reduced latency when performing a silent read command and silent write command sequence can include a silent read to silent write command delay and a silent write to silent read command delay and can be due to a reduction in latency due to the DQs not being fired during performance of the silent read command.

(37) FIG. **1**D is a block diagram of a bank section **123** of a memory device in accordance with a number of embodiments of the present disclosure. For example, bank section **123** can represent an example section of a number of bank sections of a memory device. As shown in FIG. **1**D, a bank section **123** can include a plurality of memory columns **122** shown horizontally as X (e.g., 4096, 8192, or 16,384 columns, among various possibilities, in an example DRAM bank and bank section). Additionally, the bank section **123** may be divided into subarray 0, subarray 1, . . . , and subarray N−1 (e.g., 32, 64, or 128 subarrays, among various possibilities) shown at **125-0**, **125-1**, . . . , **125-**N−1, respectively, that are separated by amplification regions configured to be coupled to a data path. As such, the subarrays **125-0**, **125-1**, . . . , **125-**N−1 can each have amplification regions **124-0**, **124-1**, . . . , **124-**N−1 that correspond to sensing component stripe 0, sensing component stripe 1, . . . , and sensing component stripe N−1, respectively.

(38) Each column **122** is configured to be coupled to sensing circuitry **150**, as described in

connection with FIG. **1**A and elsewhere herein. As such, each column in a subarray can be coupled individually to a sense amplifier that contributes to a sensing component stripe for that subarray. For example, as shown in FIG. **1**D, the bank section **123** can include sensing component stripe 0, sensing component stripe 1, . . . , sensing component stripe N−1 that each have sensing circuitry **150** with sense amplifiers that can, in various embodiments, be used as registers, cache and/or data buffering and that are coupled to each column **122** in the subarrays **125-0**, **125-1**, . . . , **125**-N−1.

(39) Each of the of the subarrays **125-0**, **125-1**, . . . , **125**-N−1 can include a plurality of rows **119** shown vertically as Y (e.g., each subarray may include 256, 512, 1024 rows, among various possibilities, in an example DRAM bank). Example embodiments are not limited to the example horizontal and vertical orientation of columns and rows described herein or the example numbers thereof.

(40) The latch component **170** associated with the sensing circuitry **150** coupled to the memory array **130**, as shown in FIG. **1**A, can complement and can be connected (e.g., selectably coupled) to the controller **140**. The sense amplifiers that sense data values in memory cells of the subarrays are located in a plurality of sensing component stripes **124** that are each physically associated with a subarray **125** of memory cells in the bank section **123** shown in FIG. **1**D.

(41) In contrast, the latch component **170** is configured to receive moved data values, store the moved data values, and/or enable access to and further movement of the data values (e.g., by and/or to the controller **140** and/or the host **110**) from the bank section **123** includes a plurality of latches located in a number of latch stripes **172** (e.g., 1-8 latch stripes, among other possibilities, as described herein) on a periphery of the bank section **123**. The plurality of latches can each be configured with a store (cache) for data values. For example, the data values (e.g., some or all of the data values in a row) can be moved from a row **119** in response to access of the row during a read and/or write operation. Each column **122** can be configured to be coupled to latches in the latch stripe **172** (e.g., via a plurality of shared I/O lines, as described herein). As such, each column in the bank can be coupled individually to a latch that contributes to a latch stripe **172** for that bank. Each bank **121-0**, . . . , **121-7** of the memory array **130** can be configured to include at least one of its own latch stripes **172**.

(42) As shown in FIG. **1**D, the bank section **123** can be associated with controller **140**. The controller **140** shown in FIG. **1**D can, in various examples, represent at least a portion of the functionality embodied by and contained in the controllers **140** shown in FIGS. **1**A and **1**B. The controller **140** can direct (e.g., control) input of commands and data **141** to the section **123** and output (e.g., movement) of data from the bank section **123** to another bank, along with control of data movement in the section **123**, as described herein. The bank section **123** can include an internal data bus (e.g., a 64 bit wide data bus) that can also be connected to DRAM DQs, which can correspond to the internal data bus **186** described in connection with FIG. **1**C. Internal data bus **186** for each bank (e.g., **121-0**, . . . , **121-7**) of subarrays (e.g., **125-0**, **125-1**, . . . , **125**-N−1) can be referred to as a portion of a data bus that contributes to formation of a combined data bus (e.g., as described in connection with FIG. **1**B for a plurality of banks and/or memory devices). As such, in some embodiments, eight 64 bit wide data bus portions for eight banks can contribute to a 512 bit wide combined data bus.

(43) FIG. **1**E is a block diagram of a number of bank sections **123-1**, . . . , **123**-N of a memory device in accordance with a number of embodiments of the present disclosure. For example, bank **121-1** can represent an example bank of a memory device **120**, such as Bank 0, . . . , Bank 7 (**121-0**, . . . , **121-7**) described in connection with FIG. **1**B. As shown in FIG. **1**E, a bank **121-1** can include a plurality of main memory columns (shown horizontally as X) (e.g., 16,384 columns in an example DRAM bank). Additionally, the bank **121-1** may be divided up into bank sections (e.g., of subarrays), **123-1**, **123-2**, . . . , **123**-N, separated by amplification regions for a data path (e.g., amplification regions **124-0**, **124-1**, . . . , **124**-N−1 that correspond to sensing component stripe 0, sensing component stripe 1, . . . , and sensing component stripe N−1 in FIG. **1**C). Each of the of the

bank sections **123-1**, . . . , **123-**N can include a plurality of rows (shown vertically as Y) (e.g., each section may include 16 subarrays that each may include 256, 512, or 1024 rows in an example DRAM bank). The bank section **123-1** can include an internal data bus (e.g., a 64 bit wide data bus) that can also be connected to DRAM DQs, which can correspond to the internal data bus **186** described in connection with FIG. **1**C. Example embodiments are not limited to the example horizontal and/or vertical orientation of columns and rows described here or the example numbers thereof.

(44) As shown in FIG. **1**E, the bank **121-1** can include a latch component **170**, including latches that each can operate as a cache for data values, and that is coupled to the bank sections **123-1**, . . . , **123-**N. The latch component **170** can represent another example of the latch component **170** selectably coupled to the sensing circuitry **150** coupled to the memory array **130** (e.g., a bank thereof) and the controller **140** shown in FIG. **1**A and/or the latch stripe **172** associated with the subarrays **125-0**, **125-1**, . . . , **125-**N−1 and the controller **140** shown in FIG. **1**D. Further, as shown in FIG. **1**E, the bank **121-1** can be associated with bank control (e.g., controller **140**). The bank control shown in FIG. **1**E can, for example, represent at least a portion of the functionality embodied by and contained in the controller **140**.

(45) FIG. **2** is a schematic diagram illustrating sensing circuitry **250** in accordance with a number of embodiments of the present disclosure. The sensing circuitry **250** can correspond to sensing circuitry **150** shown in FIG. **1**A.

(46) A memory cell can include a storage element (e.g., capacitor) and an access device (e.g., transistor). For instance, a first memory cell can include transistor **202-1** and capacitor **203-1**, and a second memory cell can include transistor **202-2** and capacitor **203-2**, etc. In this embodiment, the memory array **230** is a DRAM array of 1T1C (one transistor one capacitor) memory cells, although other embodiments of configurations can be used (e.g., 2T2C with two transistors and two capacitors per memory cell). In a number of embodiments, the memory cells may be destructive read memory cells (e.g., reading the data stored in the cell destroys the data such that the data originally stored in the cell is refreshed after being read).

(47) The cells of the memory array **230** can be arranged in rows coupled by access (word) lines **204-**X (Row X), **204-**Y (Row Y), etc., and columns coupled by pairs of complementary sense lines (e.g., digit lines DIGIT(D) and DIGIT(D)_ shown in FIG. **2** and DIGIT_0 and DIGIT_0* shown in FIG. **3**). The individual sense lines corresponding to each pair of complementary sense lines can also be referred to as digit lines **205-1** for DIGIT (D) and **205-2** for DIGIT (D)_, respectively, or corresponding reference numbers in FIG. **3**. Although only one pair of complementary digit lines are shown in FIG. **2**, embodiments of the present disclosure are not so limited, and an array of memory cells can include additional columns of memory cells and digit lines (e.g., 4,096, 8,192, 16,384, etc.).

(48) Although rows and columns are illustrated as orthogonally oriented in a plane, embodiments are not so limited. For example, the rows and columns may be oriented relative to each other in any feasible three-dimensional configuration. For example, the rows and columns may be oriented at any angle relative to each other, may be oriented in a substantially horizontal plane or a substantially vertical plane, and/or may be oriented in a folded topology, among other possible three-dimensional configurations.

(49) Memory cells can be coupled to different digit lines and word lines. For example, a first source/drain region of a transistor **202-1** can be coupled to digit line **205-1** (D), a second source/drain region of transistor **202-1** can be coupled to capacitor **203-1**, and a gate of a transistor **202-1** can be coupled to word line **204-**Y. A first source/drain region of a transistor **202-2** can be coupled to digit line **205-2** (D)_, a second source/drain region of transistor **202-2** can be coupled to capacitor **203-2**, and a gate of a transistor **202-2** can be coupled to word line **204-**X. A cell plate, as shown in FIG. **2**, can be coupled to each of capacitors **203-1** and **203-2**. The cell plate can be a common node to which a reference voltage (e.g., ground) can be applied in various memory array

configurations.
(50) The memory array **230** is configured to couple to sensing circuitry **250** in accordance with a number of embodiments of the present disclosure. In this embodiment, the sensing circuitry **250** comprises a sense amplifier **206** and a compute component **231** corresponding to respective columns of memory cells (e.g., coupled to respective pairs of complementary digit lines). The sense amplifier **206** can be coupled to the pair of complementary digit lines **205-1** and **205-2**. The compute component **231** can be coupled to the sense amplifier **206** via pass gates **207-1** and **207-2**. The gates of the pass gates **207-1** and **207-2** can be coupled to operation selection logic **213**.
(51) The operation selection logic **213** can be configured to include pass gate logic for controlling pass gates that couple the pair of complementary digit lines un-transposed between the sense amplifier **206** and the compute component **231** and swap gate logic for controlling swap gates that couple the pair of complementary digit lines transposed between the sense amplifier **206** and the compute component **231**. The operation selection logic **213** can also be coupled to the pair of complementary digit lines **205-1** and **205-2**. The operation selection logic **213** can be configured to control continuity of pass gates **207-1** and **207-2** based on a selected operation.
(52) The sense amplifier **206** can be operated to determine a data value (e.g., logic state) stored in a selected memory cell. The sense amplifier **206** can comprise a cross coupled latch, which can be referred to herein as a primary latch. In the example illustrated in FIG. **2**, the circuitry corresponding to sense amplifier **206** comprises a latch **215** including four transistors coupled to a pair of complementary digit lines D **205-1** and (D)_ **205-2**. However, embodiments are not limited to this example. The latch **215** can be a cross coupled latch (e.g., gates of a pair of transistors) such as n-channel transistors (e.g., NMOS transistors) **227-1** and **227-2** are cross coupled with the gates of another pair of transistors, such as p-channel transistors (e.g., PMOS transistors) **229-1** and **229-2**).
(53) In operation, when a memory cell is being sensed (e.g., read), the voltage on one of the digit lines **205-1** (D) or **205-2** (D)_ will be slightly greater than the voltage on the other one of digit lines **205-1** (D) or **205-2** (D)_. An ACT signal and an RNL* signal can be driven low to enable (e.g., fire) the sense amplifier **206**. The digit lines **205-1** (D) or **205-2** (D)_ having the lower voltage will turn on one of the PMOS transistor **229-1** or **229-2** to a greater extent than the other of PMOS transistor **229-1** or **229-2**, thereby driving high the digit line **205-1** (D) or **205-2** (D)_ having the higher voltage to a greater extent than the other digit line **205-1** (D) or **205-2** (D)_ is driven high.
(54) Similarly, the digit line **205-1** (D) or **205-2** (D)_ having the higher voltage will turn on one of the NMOS transistor **227-1** or **227-2** to a greater extent than the other of the NMOS transistor **227-1** or **227-2**, thereby driving low the digit line **205-1** (D) or **205-2** (D)_ having the lower voltage to a greater extent than the other digit line **205-1** (D) or **205-2** (D)_ is driven low. As a result, after a short delay, the digit line **205-1** (D) or **205-2** (D)_ having the slightly greater voltage is driven to the voltage of the supply voltage V.sub.CC through a source transistor, and the other digit line **205-1** (D) or **205-2** (D)_ is driven to the voltage of the reference voltage (e.g., ground) through a sink transistor. Therefore, the cross coupled NMOS transistors **227-1** and **227-2** and PMOS transistors **229-1** and **229-2** serve as a sense amplifier pair, which amplify the differential voltage on the digit lines **205-1** (D) and **205-2** (D)_ and operate to latch a data value sensed from the selected memory cell.
(55) Embodiments are not limited to the sense amplifier **206** configuration illustrated in FIG. **2**. As an example, the sense amplifier **206** can be a current-mode sense amplifier and a single-ended sense amplifier (e.g., sense amplifier coupled to one digit line). Also, embodiments of the present disclosure are not limited to a folded digit line architecture such as that shown in FIG. **2**.
(56) The sense amplifier **206** can, in conjunction with the compute component **231**, be operated to perform various operations using data from an array as input. In a number of embodiments, the result of an operation can be stored back to the array without transferring the data via a digit line address access and/or moved between banks without using an external data bus (e.g., without firing

a column decode signal such that data is transferred to circuitry external from the array and sensing circuitry via local I/O lines). As such, a number of embodiments of the present disclosure can enable performing operations and compute functions associated therewith using less power than various previous approaches. Additionally, since a number of embodiments eliminate the need to transfer data across local and global I/O lines and/or external data buses in order to perform compute functions (e.g., between memory and discrete processor), a number of embodiments can enable an increased (e.g., faster) processing capability as compared to previous approaches.
(57) The sense amplifier **206** can further include equilibration circuitry **214**, which can be configured to equilibrate the digit lines **205-1** (D) and **205-2** (D)_. In this example, the equilibration circuitry **214** comprises a transistor **224** coupled between digit lines **205-1** (D) and **205-2** (D)_. The equilibration circuitry **214** also comprises transistors **225-1** and **225-2** each having a first source/drain region coupled to an equilibration voltage (e.g., V.sub.DD/2), where V.sub.DD is a supply voltage associated with the array. A second source/drain region of transistor **225-1** can be coupled digit line **205-1** (D), and a second source/drain region of transistor **225-2** can be coupled digit line **205-2** (D)_. Gates of transistors **224**, **225-1**, and **225-2** can be coupled together, and to an equilibration (EQ) control signal line **226**. As such, activating EQ enables the transistors **224**, **225-1**, and **225-2**, which effectively shorts digit lines **205-1** (D) and **205-2** (D)_together and to the equilibration voltage (e.g., V.sub.DD/2).
(58) Although FIG. **2** shows sense amplifier **206** comprising the equilibration circuitry **214**, embodiments are not so limited, and the equilibration circuitry **214** may be implemented discretely from the sense amplifier **206**, implemented in a different configuration than that shown in FIG. **2**, or not implemented at all.
(59) As described further below, in a number of embodiments, the sensing circuitry **250** (e.g., sense amplifier **206** and compute component **231**) can be operated to perform a selected operation and initially store the result in one of the sense amplifier **206** or the compute component **231** without transferring data from the sensing circuitry via a local or global I/O line and/or moved between banks without using an external data bus (e.g., without performing a sense line address access via activation of a column decode signal, for instance).
(60) Performance of operations (e.g., Boolean logical operations involving data values) is fundamental and commonly used. Boolean logical operations are used in many higher level operations. Consequently, speed and/or power efficiencies that can be realized with improved operations, can translate into speed and/or power efficiencies of higher order functionalities.
(61) As shown in FIG. **2**, the compute component **231** can also comprise a latch, which can be referred to herein as a secondary latch **264**. The secondary latch **264** can be configured and operated in a manner similar to that described above with respect to the primary latch **215**, with the exception that the pair of cross coupled p-channel transistors (e.g., PMOS transistors) included in the secondary latch can have their respective sources coupled to a supply voltage (e.g., V.sub.DD), and the pair of cross coupled n-channel transistors (e.g., NMOS transistors) of the secondary latch can have their respective sources selectively coupled to a reference voltage (e.g., ground), such that the secondary latch is continuously enabled. The configuration of the compute component **231** is not limited to that shown in FIG. **2**, and various other embodiments are feasible.
(62) As described herein, a memory device (e.g., **120** in FIG. **1**A) can be configured to couple to a host (e.g., **110**) via a data bus (e.g., **156**) and a control bus (e.g., **154**). A bank **121** in the memory device (e.g., bank section **123** in FIG. **1**C) can include a plurality of subarrays (e.g., **125-0**, **125-1**, . . . , **125-**N−1 in FIG. **1**C) of memory cells. The bank **121** can include sensing circuitry (e.g., **150** in FIG. **1**A and corresponding reference numbers in FIGS. **2** and **3**) coupled to the plurality of subarrays via a plurality of columns (e.g., **122** in FIG. **1**C) of the memory cells. The sensing circuitry can include a sense amplifier and a compute component (e.g., **206** and **231**, respectively, in FIG. **2**) coupled to each of the columns.
(63) The bank **121** can include a plurality of sensing component stripes (e.g., **124-0**, **124-1**, . . . ,

124-N−1 in FIG. **1**C) each with sensing circuitry coupled to a respective subarray of the plurality of the subarrays. A controller (e.g., **140** in FIGS. **1**A-**1**C) coupled to the bank can be configured to direct, as described herein, movement of data values stored in a first subarray (e.g., from data values in a row of the subarray sensed (cached) by the coupled sensing component stripe) to be stored in latches of a latch stripe (e.g., **172** in FIG. **1**C) and/or a latch component (e.g., **170** in FIG. **1**D). Moving (e.g., copying, transferring, and/or transporting) data values between sense amplifiers and/or compute components (e.g., **206** and **231**, respectively, in FIG. **2**) in a sensing component stripe and corresponding sense amplifiers and/or compute components that form latches in a latch stripe can be enabled by a number of selectably coupled shared I/O lines (e.g., **355** in FIG. **3**) shared by the sensing component stripe and the latch stripe, as described herein.

(64) The memory device can include a sensing component stripe (e.g., **124** in FIG. **1**C) configured to include a number of a plurality of sense amplifiers and compute components (e.g., **306-0**, **306-1**, . . . , **306-7** and **331-0**, **331-1**, . . . , **331-7**, respectively, as shown in FIG. **3**) that can correspond to a number of the plurality of columns (e.g., **122** in FIG. **1**C and **305-1** and **305-2** in FIG. **3**) of the memory cells, where the number of sense amplifiers and/or compute components can be selectably coupled to the plurality of shared I/O lines (e.g., via column select circuitry **358-1** and **358-2**). The column select circuitry can be configured to selectably sense data in a particular column of memory cells of a subarray by being selectably coupled to a plurality of (e.g., four, eight, and sixteen, among other possibilities) sense amplifiers and/or compute components.

(65) In some embodiments, a number of a plurality of sensing component stripes (e.g., **124-0**, . . . , **124**-N−1 in FIG. **1**C) in the bank can correspond to a number of the plurality of subarrays (e.g., **125-0**, **125-1**, . . . , **125**-N−1 in FIG. **1**C) in the bank. A sensing component stripe can include a number of sense amplifiers and/or compute components configured to move (e.g., copy, transfer, and/or transport) an amount of data sensed from a row of the first subarray in parallel to a plurality of shared I/O lines. In some embodiments, the amount of data can correspond to at least a thousand bit width of the plurality of shared I/O lines.

(66) As described herein, the array of memory cells can include an implementation of DRAM memory cells where the controller is configured, in response to a command, to move (e.g., copy, transfer, and/or transport) data from the source location to the destination location via a shared I/O line. In various embodiments, the source location can be in a first bank and the destination location can be in a second bank in the memory device and/or the source location can be in a first subarray of one bank in the memory device and the destination location can be in a second subarray of a different bank. According to embodiments, the data can be moved as described in connection with FIG. **1**C. The first subarray and the second subarray can be in the same section of the bank or the subarrays can be in different sections of the bank.

(67) As described herein, the apparatus can be configured to move (e.g., copy, transfer, and/or transport) data from a source location, including a particular row (e.g., **319** in FIG. **3**) and column address associated with a first number of sense amplifiers and compute components) to a shared I/O line. In addition, the apparatus can be configured to move the data to a destination location, including a particular row and column address associated with a second number of sense amplifiers and compute components. As the reader will appreciate, each shared I/O line can actually include a complementary pair of shared I/O lines (e.g., shared I/O line and shared I/O line* as shown in the example configuration of FIG. **3**). In some embodiments described herein, 2048 shared I/O lines (e.g., complementary pairs of shared I/O lines) can be configured as a 2048 bit wide shared I/O line.

(68) FIG. **3** is a schematic diagram illustrating circuitry for data transfer in a memory device in accordance with a number of embodiments of the present disclosure. FIG. **3** shows eight sense amplifiers (e.g., sense amplifiers 0, 1, . . . , 7 shown at **306-0**, **306-1**, . . . , **306-7**, respectively) each coupled to a respective pair of complementary sense lines (e.g., digit lines **305-1** and **305-2**). FIG. **3** also shows eight compute components (e.g., compute components 0, 1, . . . , 7 shown at **331-0**,

331-1, . . . , **331-7**) each coupled to a respective sense amplifier (e.g., as shown for sense amplifier 0 at **306-0**) via respective pass gates **307-1** and **307-2** and digit lines **305-1** and **305-2**. For example, the pass gates can be connected as shown in FIG. **2** and can be controlled by an operation selection signal, Pass. For example, an output of the selection logic can be coupled to the gates of the pass gates **307-1** and **307-2** and digit lines **305-1** and **305-2**. Corresponding pairs of the sense amplifiers and compute components can contribute to formation of the sensing circuitry indicated at **350-0**, **350-1**, . . . , **350-7**.

(69) Data values present on the pair of complementary digit lines **305-1** and **305-2** can be loaded into the compute component **331-0** as described in connection with FIG. **2**. For example, when the pass gates **307-1** and **307-2** are enabled, data values on the pair of complementary digit lines **305-1** and **305-2** can be passed from the sense amplifiers to the compute component (e.g., **306-0** to **331-0**). The data values on the pair of complementary digit lines **305-1** and **305-2** can be the data value stored in the sense amplifier **306-0** when the sense amplifier is fired.

(70) The sense amplifiers **306-0**, **306-1**, . . . , **306-7** in FIG. **3** can each correspond to sense amplifier **206** shown in FIG. **2**. The compute components **331-0**, **331-1**, . . . , **331-7** shown in FIG. **3** can each correspond to compute component **231** shown in FIG. **2**. A combination of one sense amplifier with one compute component can contribute to the sensing circuitry (e.g., **350-0**, **350-1**, . . . , **350-7**) of a portion of a DRAM memory subarray **325** configured to an I/O line **355** shared by a number of sensing component stripes for subarrays and/or latch components, as described herein. The paired combinations of the sense amplifiers **306-0**, **306-1**, . . . , **306-7** and the compute components **331-0**, **331-1**, . . . , **331-7**, shown in FIG. **3**, can be included in the sensing component stripe, as shown at **124** in FIG. **1**C.

(71) The configurations of embodiments illustrated in FIG. **3** are shown for purposes of clarity and are not limited to these configurations. For instance, the configuration illustrated in FIG. **3** for the sense amplifiers **306-0**, **306-1**, . . . , **306-7** in combination with the compute components **331-0**, **331-1**, . . . , **331-7** and the shared I/O line **355** is not limited to half the combination of the sense amplifiers **306-0**, **306-1**, . . . , **306-7** with the compute components **331-0**, **331-1**, . . . , **331-7** of the sensing circuitry being formed above the columns **322** of memory cells (not shown) and half being formed below the columns **322** of memory cells. Nor are the number of such combinations of the sense amplifiers with the compute components forming the sensing circuitry configured to couple to a shared I/O line limited to eight. In addition, the configuration of the shared I/O line **355** is not limited to being split into two for separately coupling each of the two sets of complementary digit lines **305-1** and **305-2**, nor is the positioning of the shared I/O line **355** limited to being in the middle of the combination of the sense amplifiers and the compute components forming the sensing circuitry (e.g., rather than being at either end of the combination of the sense amplifiers and the compute components).

(72) The circuitry illustrated in FIG. **3** also shows column select circuitry **358-1** and **358-2** that is configured to implement data movement operations with respect to particular columns **322** of a subarray **325**, the complementary digit lines **305-1** and **305-2** associated therewith, and the shared I/O line **355** (e.g., as directed by the controller **140** shown in FIGS. **1**A-**1**D). For example, column select circuitry **358-1** has select lines 0, 2, 4, and 6 that are configured to couple with corresponding columns, such as column 0 (**332-0**), column 2, column 4, and column 6. Column select circuitry **358-2** has select lines 1, 3, 5, and 7 that are configured to couple with corresponding columns, such as column 1, column 3, column 5, and column 7.

(73) Controller **140** can be coupled to column select circuitry **358** to control select lines (e.g., select line 0) to access data values stored in the sense amplifiers, compute components, and/or present on the pair of complementary digit lines (e.g., **305-1** and **305-2** when selection transistors **359-1** and **359-2** are activated via signals from select line 0). Activating the selection transistors **359-1** and **359-2** (e.g., as directed by the controller **140**) enables coupling of sense amplifier **306-0**, compute component **331-0**, and/or complementary digit lines **305-1** and **305-2** of column 0 (**322-0**) to move

data values on digit line 0 and digit line 0* to shared I/O line **355**. For example, the moved data values may be data values from a particular row **319** stored (cached) in sense amplifier **306-0** and/or compute component **331-0**. Data values from each of columns 0 through 7 can similarly be selected by controller **140** activating the appropriate selection transistors.
(74) Moreover, enabling (e.g., activating) the selection transistors (e.g., selection transistors **359-1** and **359-2**) can enable a particular sense amplifier and/or compute component (e.g., **306-0** and/or **331-0**, respectively) to be coupled with a shared I/O line **355** such that data values stored by an amplifier and/or compute component can be moved to (e.g., placed on and/or transferred to) the shared I/O line **355**. In some embodiments, one column at a time is selected (e.g., column **322-0**) to be coupled to a particular shared I/O line **355** to move (e.g., copy, transfer, and/or transport) the stored data values. In the example configuration of FIG. **3**, the shared I/O line **355** is illustrated as a shared, differential I/O line pair (e.g., shared I/O line and shared I/O line*). Hence, selection of column 0 (**322-0**) could yield two data values (e.g., two bits with values of 0 and/or 1) from a row (e.g., row **319**) and/or as stored in the sense amplifier and/or compute component associated with complementary digit lines **305-1** and **305-2**. These data values could be input in parallel to each shared, differential I/O pair (e.g., shared I/O and shared I/O*) of the shared differential I/O line **355**.
(75) While example embodiments including various combinations and configurations of sensing circuitry, sense amplifiers, compute components, sensing component stripes, shared I/O lines, column select circuitry, multiplexers, latch components, latch stripes, and/or latches, etc., have been illustrated and described herein, embodiments of the present disclosure are not limited to those combinations explicitly recited herein. Other combinations and configurations of the sensing circuitry, sense amplifiers, compute components, sensing component stripes, shared I/O lines, column select circuitry, multiplexers, latch components, latch stripes, and/or latches, etc., disclosed herein are expressly included within the scope of this disclosure.
(76) Although specific embodiments have been illustrated and described herein, those of ordinary skill in the art will appreciate that an arrangement calculated to achieve the same results can be substituted for the specific embodiments shown. This disclosure is intended to cover adaptations or variations of one or more embodiments of the present disclosure. It is to be understood that the above description has been made in an illustrative fashion, and not a restrictive one. Combination of the above embodiments, and other embodiments not specifically described herein will be apparent to those of skill in the art upon reviewing the above description. The scope of the one or more embodiments of the present disclosure includes other applications in which the above structures and processes are used. Therefore, the scope of one or more embodiments of the present disclosure should be determined with reference to the appended claims, along with the full range of equivalents to which such claims are entitled.
(77) In the foregoing Detailed Description, some features are grouped together in a single embodiment for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as reflecting an intention that the disclosed embodiments of the present disclosure have to use more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive subject matter lies in less than all features of a single disclosed embodiment. Thus, the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment.

Claims

1. An apparatus, comprising: a processor in memory device (PIM) comprising a plurality of banks of memory cells, each bank of memory cells of the plurality of banks of memory cells is in communication with a respective sense amplifier and compute component, wherein the PIM receives one or more commands including instructions to transfer data between the plurality banks,

and the PIM is configured to: transfer the data between the plurality of banks of memory cells, via at least the respective compute components, by executing the one of more commands, wherein the one or more commands include source bank information used to identify a source bank to read the data from and destination bank information used to identify a destination bank to write the data to.
2. The apparatus of claim 1, wherein the data transferred between the plurality of banks includes program instructions for the PIM device to perform operations on data stored in the plurality of banks.
3. The apparatus of claim 1, wherein the source bank is identified by a first number of bits and the destination bank is identified by a second number of bits.
4. The apparatus of claim 1, wherein, to transfer the data between the plurality of banks of memory cells, the PIM device is configured to perform a read command that transfers the data from the plurality of banks to a number of buffers isolated from a number of DQs.
5. The apparatus of claim 1, wherein the PIM device is coupled to a host via a bus.
6. The apparatus of claim 5, wherein the host is configured to send another command to the PIM device to perform an operation using the data transferred between the plurality of banks.
7. The apparatus of claim 1, wherein the PIM device is configured to cause the transfer of the data on an internal data bus that couples the plurality of banks of memory cells together and wherein the internal data bus is coupled to an external data bus that is configured to transfer the data between the plurality of banks of memory cells and a host.
8. The apparatus of claim 7, wherein the internal data bus that couples the plurality of banks of memory cells together is coupled to a number of DQs to transfer the data from the plurality of banks of memory cells.
9. A system, comprising: a host configured to provide instructions for transferring data; and a processor in memory (PIM) device, coupled to the host, comprising: a plurality of banks of memory cells, wherein each bank of the plurality of banks is in communication with a respective sense amplifier and a respective compute component, and wherein the PIM device, via the respective compute components, is configure to: transfer the data between the plurality of banks of memory cells by: performing a number of read commands that transfer the data from the plurality of banks to a number of buffers and a number of write commands that transfer the data from the number of buffers to the plurality of banks, wherein source bank information is used to identify a source bank to read the data from and destination bank information is used to identify a destination bank to write the data to.
10. The system of claim 9, wherein the PIM device is configured to perform an operation on data stored in the plurality of banks using program instructions in the data transferred between the plurality of banks according to the instructions from the host.
11. The system of claim 10, wherein a result of the operation is transferred from the PIM device to the host.
12. The system of claim 10, wherein the host includes a channel controller configured to send a command to the PIM device to perform the operation.
13. A method of operating a processor in memory (PIM) device, comprising: receiving one or more commands to transfer data between a plurality of banks of the PIM device, wherein each bank of the plurality of banks is in communication with a respective sense amplifier and a respective compute component; and transferring the data from a first bank of memory cells in the PIM device to a second bank of memory cells in the PIM device via a first compute component in communication with the first bank of memory cells and a second compute component in communication with the second bank of memory cells by executing the one or more commands, wherein the one or more commands include source bank information identifying a source bank to read the data from and destination bank information identifying a destination bank to write the data to.
14. The method of claim 13, wherein transferring the data from the first bank to the second bank

stores program instructions for performing an operation on the PIM device using one of the respective compute components of the PIM device.

15. The method of claim 14, further including performing the operation on the PIM device using the program instructions stored on the second bank.

16. The method of claim 13, wherein transferring the data from the first bank to the second bank includes transferring the data on an internal data bus without transferring the data on an external data bus.

17. The method of claim 13, wherein the method further comprises performing a silent read command to transfer the data from the first bank to a number of buffers isolated from a number of DQs on an internal data bus.

18. The method of claim 17, wherein the method further comprises performing a write command to transfer the data from the number of buffers isolated from the number of DQs on the internal data bus to the second bank.

19. The method of claim 13, wherein transferring the data from the first bank of memory cells to the second bank of memory cells comprises performing a bank to bank data transfer command that identifies, simultaneously, the first bank as the source bank and the second bank as the destination bank.

20. The method of claim 13, wherein transferring the data from the first bank of memory cells in the PIM device to the second bank of memory cells in the PIM device includes enabling bidirectional buffers for transferring the data on an internal data path based on the source bank information and the destination bank information.