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MEMORY INCLUDING BIT LINE PILLAR

Abstract

A memory may include a plurality of word lines formed of N layers, M word lines being arranged in each layer, among the plurality of word lines, where each of N and M is an integer of 2 or more; a plurality of bit line pillars; and a plurality of memory cells disposed at intersections between the plurality of word lines and the plurality of bit line pillars, respectively. Among the plurality of word lines, two or more word lines of the plurality of word lines may be grouped and driven together.

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority under 35 U.S.C. § 119(a) to Korean Patent Application No. 10-2024-0021609 filed on Feb. 15, 2024, which is incorporated herein by reference in its entirety.

BACKGROUND

1. Technical Field

[0002] Embodiments of the present disclosure relate to a memory, and more particularly, to a memory including a three-dimensional memory cell.

2. Related Art

[0003] Recently, in order to cope with an increase in capacity and miniaturization of a memory, a technology for implementing a three-dimensional (3D) memory in which a plurality of memory cells are stacked has been studied.

SUMMARY

[0004] In an embodiment of the present disclosure, a memory may include a plurality of word lines formed of N layers, M word lines being arranged in each layer, among the plurality of word lines, where each of N and M is an integer of 2 or more; a plurality of bit line pillars; and a plurality of memory cells disposed at intersections between the plurality of word lines and the plurality of bit line pillars, respectively, wherein two or more word lines of the plurality of word lines may be grouped and driven together.

[0005] In an embodiment of the present disclosure, a memory may include a plurality of word lines; a plurality of bit lines; and a plurality of memory cells connected to one of the plurality of word lines and one of the plurality of bit lines, wherein two or more word lines of the plurality of word lines may be grouped and driven together.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIGS. **1** and **2** are diagrams illustrating the structure of word lines in a cell array of a memory in accordance with an embodiment of the present disclosure.

[0007] FIG. **3** is a diagram illustrating bit lines for electrical connection among bit line pillars in FIGS. **1** and **2**.

[0008] FIG. **4** is a side view of the cell array illustrated in FIGS. **1** to **3**.

[0009] FIG. **5** is a circuit diagram illustrating electrical connection among word lines, the bit line pillars, and memory cells of an Nth layer in the cell array illustrated in FIGS. **1** to **4**.

[0010] FIG. **6** is a diagram illustrating the structure of word lines in a cell array of a memory in accordance with another embodiment of the present disclosure.

[0011] FIG. **7** is a diagram illustrating bit lines for electrical connection among bit line pillars in FIG. **6**.

[0012] FIG. **8** is a side view of the cell array illustrated in FIGS. **6** and **7**.

[0013] FIG. **9** is a circuit diagram illustrating electrical connection among word lines, the bit line pillars, and memory cells of an Nth layer in the cell array illustrated in FIGS. **6** to **8**.

DETAILED DESCRIPTION

[0014] Various embodiments of the present disclosure are directed to providing a more highly integrated memory with a reduced area.

[0015] Embodiments of the present disclosure may reduce an area of a memory and further integrate the memory.

[0016] Hereafter, embodiments in accordance with the technical spirit of the present disclosure will be described with reference to the accompanying drawings.

[0017] FIGS. **1** and **2** are diagrams illustrating the structure of word lines in a cell array **100** of a

memory in accordance with an embodiment of the present disclosure. The cell array **100** may be formed of N layers, where N is an integer of 2 or more, and may include M word lines WL arranged in each layer, where M is an integer of 2 or more and is 12 herein, FIG. **1** may be a plan view illustrating an N.sup.th layer, and FIG. **2** may be a plan view illustrating a third layer. In FIGS. **1** and **2**, a first direction 'I' may be perpendicular to a second direction 'II'.

[0018] Referring to FIG. **1**, the cell array **100** may include word lines WL**0**_N to WL**11**_N and bit line pillars BLP**0** to BLP**35**. The bit line pillars BLP**0** to BLP**35** may refer to pillar-shaped bit lines. The bit line pillars BLP**0** to BLP**35** may be disposed to pass and intersect between two word lines in each of the word line layers. For example, the bit line pillars BLP**0** to BLP**5** may pass between the word lines WL**0_3** and WL**1_3** in the third layer (FIG. **2**) and between the word lines WL**0**_N and WL**1**_N in the N.sup.th layer (FIG. **1**).

[0019] Memory cells (not illustrated) may be disposed at intersections between the word lines WL and the bit line pillars BLP, respectively. Because the bit line pillars BLP intersect with two word lines WL for each word line layer, the cell array **100** may include [number of bit line pillars]×[number of word line layers]×two memory cells. For example, a memory cell may be disposed at an intersection between the bit line pillar BLP**0** and the word line WL**0_1** of the first layer, and a memory cell may be disposed at an intersection between the bit line pillar BLP**0** and the word line WL**1_1** of the first layer. Likewise, memory cells may be disposed at intersections between the bit line pillar BLP**0** and the word lines WL**0_2** to WL**0**_N and WL**1_2** to WL**1**_N of the second to N.sup.th layers, respectively.

[0020] Two or more word lines of each layer may be grouped and driven together. In FIGS. **1** and **2**, two word lines connected by arrows may be shorted to each other and driven together. That is, the word lines WL**0** and WL**2** may be shorted to each other and driven together, the word lines WL**1** and WL**3** may be shorted to each other and driven together, the word lines WL**4** and WL**6** may be shorted to each other and driven together, the word lines WL**5** and WL**7** may be shorted to each other and driven together, the word lines WL**8** and WL**10** may be shorted to each other and driven together, and the word lines WL**9** and WL**11** may be shorted to each other and driven together. This may be the same for not only the word lines WL**0**_N to WL**11**_N of the N.sup.th layer illustrated in FIG. **1** and the word lines WL**0_3** to WL**11_3** of the third layer illustrated in FIG. **2**, but also the word lines of all layers.

[0021] FIG. **1** illustrates the word lines WL**0**_N to WL**11**_N of the N.sup.th layer, and FIG. **2** illustrates the word lines WL**0_3** to WL**11_3** of the third layer. The word lines of the remaining layers may also have the same structure as the structure in FIGS. **1** and **2**.

[0022] FIG. **3** is a diagram illustrating bit lines BL**0** to BL**11** for electrical connection among the bit line pillars BLP**0** to BLP**35** of FIGS. **1** and **2**. FIG. **3** also illustrates bit line sense amplifier arrays **310** and **320** around the cell array **100**.

[0023] The bit lines BL**0** to BL**11** may be disposed below the word lines WL**0_1** to WL**11_1** of the first layer. The bit lines BL**0** to BL**11** may be lines for connecting the bit line pillars BLP**0** to BLP**35** and the bit line sense amplifier arrays **310** and **320**.

[0024] Referring to contacts of FIG. **3**, bit line pillars BLP**0**, BLP**12**, and BLP**24** may be connected to the bit line BL**0**. Accordingly, the bit line pillars BLP**0**, BLP**12**, and BLP**24** may be electrically identical bit lines. Bit line pillars BLP**6**, BLP**18**, and BLP**30** may be connected to the bit line BL**1**. Accordingly, the bit line pillars BLP**6**, BLP**18**, and BLP**30** may be electrically identical bit lines. Likewise, because the bit line pillars BLP**1**, BLP**13**, and BLP**25** are connected to the bit line BL**2**, the bit line pillars BLP**1**, BLP**13**, and BLP**25** may be identical bit lines, and because the bit line pillars BLP**7**, BLP**19**, and BLP**31** are connected to the bit line BL**3**, the bit line pillars BLP**7**, BLP**19**, and BLP**31** may be identical bit lines.

[0025] That is, in FIG. **3**, bit line pillars BLPX, BLPX+12, and BLPX+24, where X is an integer between 0 and 11, may be identical bit lines electrically connected.

[0026] Half of the bit lines BL**0** to BL**11**, for example, even-numbered bit lines BL**0**, BL**2**, BL**4**,

BL**6**, BL**8**, and BL**10** may be connected to the bit line sense amplifier array **310**, and the other half, for example, odd-numbered bit lines BL**1**, BL**3**, BL**5**, BL**7**, BL**9**, and BL**11** may be connected to the bit line sense amplifier array **320**. The bit line sense amplifier arrays **310** and **320** may sense and amplify data transmitted to connected bit lines. Each of the bit line sense amplifier arrays **310** and **320** may include a plurality of bit line sense amplifiers.

[0027] FIG. **4** is a side view of the cell array **100** illustrated in FIGS. **1** to **3**. In FIG. **4**, a third direction 'III' may be a direction orthogonal to a plane defined by the first direction 'I' and the second direction 'II' in FIGS. **1** to **3**.

[0028] Referring to FIG. **4**, it may be seen that each of the bit line pillars BLP**0**, BLP**6**, BLP**12**, BLP**18**, BLP**24**, and BLP**30** intersects with two word lines in each layer from the first layer to the N.sup.th layer. For example, it may be seen that the bit line pillar BLP**0** intersects with the word lines WL**0**_**1** to WL**0**_N and WL**1**_**1** to WL**1**_N in the first layer to the N.sup.th layer. That is, each of the bit line pillars BLP**0**, BLP**6**, BLP**12**, BLP**18**, BLP**24**, and BLP**30** may intersect with 2×N word lines.

[0029] Below the word lines WL**0**_**1** to WL**11**_**1** of the first layer, the bit line BL**0** may be provided to electrically connect some (BLP**0**, BLP**12**, and BLP**24**, see FIG. **3**) of the bit line pillars BLP**0**, BLP**6**, BLP**12**, BLP**18**, BLP**24**, and BLP**30**.

[0030] FIG. **5** is a circuit diagram illustrating electrical connection among the word lines WL**0**_N to WL**11**_N, the bit line pillars BLP**0** to BLP**35**, and memory cells MC**0**_N to MC**71**_N of the N.sup.th layer in the cell array **100** illustrated in FIGS. **1** to **4**.

[0031] The memory cells MC**0**_N to MC**71**_N may be disposed at intersections between the bit line pillars BLP**0** to BLP**35** and the word lines WL**0**_N to WL**11**_N, respectively. Because each of the bit line pillars BLP**0** to BLP**35** intersects with two bit lines, the number of memory cells MC**0**_N to MC**71**_N in the N.sup.th layer may be twice the number of bit line pillars BLP**0** to BLP**35**. Each of the memory cells MC**0**_N to MC**71**_N may include a capacitor for storing data and a transistor for transmitting data stored in the capacitor to a bit line pillar under the control of the word line.

[0032] The following describes an operation when the word lines WL**0**_N and WL**2**_N shorted to each other are simultaneously activated. As the word line WL**0** is activated, the transistors of the memory cells MC**0**_N to MC**5**_N may be turned on, so that data stored in the capacitors of the memory cells MC**0**_N to MC**5**_N may be transmitted to the bit line pillars BLP**0** to BLP**5**. As the word line WL**2** is activated, the transistors of the memory cells MC**12**_N to MC**17**_N are turned on, so that data stored in the capacitors of the memory cells MC**12**_N to MC**17**_N may be transmitted to the bit line pillars BLP**6** to BLP**11**. The data of the bit line pillars BLP**0** to BLP**5** may be transmitted to the bit line sense amplifier array **310** through the bit lines BL**0**, BL**2**, BL**4**, BL**6**, BL**8**, and BL**10** and sensed and amplified, and the data of the bit line pillars BLP**6** to BLP**11** may be transmitted to the bit line sense amplifier array **320** through the bit lines BL**1**, BL**3**, BL**5**, BL**7**, BL**9**, and BL**11** and sensed and amplified. That is, even though the two word lines WL**0**_N and WL**2**_N are simultaneously activated, the data of the memory cells MC**0**_N to MC**5**_N and MC**12**_N to MC**17**_N may be transmitted to the bit lines BL**0** to BL**11** different from one another and sensed and amplified.

[0033] Likewise, when the word lines WL**1**_N and WL**3**_N are simultaneously activated, data of the memory cells MC**6**_N to MC**11**_N corresponding to the word line WL**1**_N may be transmitted to the bit line sense amplifier array **310** through the bit line pillars BLP**0** to BLP**5** and the bit lines BL**0**, BL**2**, BL**4**, BL**6**, BL**8**, and BL**10** and sensed and amplified. Data of the memory cells MC**18**_N to MC**23**_N corresponding to the word line WL**3**_N may be transmitted to the bit line sense amplifier array **320** through the bit line pillars BLP**6** to BLP**11** and the bit lines BL**1**, BL**3**, BL**5**, BL**7**, BL**9**, and BL**11** and sensed and amplified.

[0034] In the cell array **100** illustrated in FIGS. **1** to **5**, because the word lines WL are shorted by the two, the word lines WL may form a pair by the two and be simultaneously driven. With such a

structure, the number of word lines WL that need to be driven may be reduced by half, which may mean that an area of a word line driving circuit (not illustrated) may be reduced by half. Because the word line driving circuit is a circuit that occupies a large area in the memory, when the area of the word line driving circuit is reduced by half, the area of the memory may be reduced and a more highly integrated memory may be manufactured.

[0035] FIG. **6** is a diagram illustrating the structure of word lines in a cell array **600** of a memory in accordance with another embodiment of the present invention. The cell array **600** may be formed of N layers and include M word lines WL arranged in each layer. FIG. **6** may be a plan view illustrating an N.sup.th layer. In FIG. **6**, the first direction 'I' may be perpendicular to the second direction 'II'.

[0036] Referring to FIG. **6**, the cell array **600** may include word lines WL**0**_N to WL**11**_N and bit line pillars BLP**0** to BLP**35**, similar to FIG. **1**. The bit line pillars BLP**0** to BLP**35** may refer to pillar-shaped bit lines. The bit line pillars BLP**0** to BLP**35** may be disposed to pass and intersect between two word lines in each of the word line layers. For example, the bit line pillars BLP**0** to BLP**5** may pass between the word lines WL**0**_N and WL**1**_N in the N.sup.th layer (FIG. **1**).

[0037] The word lines of each layer may form a group by three and be simultaneously driven. In FIG. **6**, word lines connected by arrows may be shorted to one another and driven together. The word lines WL**0**_N, WL**2**_N, and WL**4**_N may be shorted to one another and driven together, the word lines WL**1**_N, WL**3**_N, and WL**5**_N may be shorted to one another and driven together, the word lines WL**6**_N, WL**8**_N, and WL**10**_N may be shorted to one another and driven together, and the word lines WL**7**_N, WL**9**_N, and WL**11**_N may be shorted to one another and driven together.

[0038] FIG. **6** illustrates the word lines WL**0**_N to WL**11**_N of the N.sup.th layer, and the word lines of the remaining layers may also have the same structure as the structure in FIG. **6**.

[0039] FIG. **7** is a diagram illustrating bit lines BL**0** to BL**17** for electrical connection among the bit line pillars BLP**0** to BLP**35** of FIG. **6**. FIG. **7** also illustrates bit line sense amplifier arrays **710** and **720** around the cell array **600**.

[0040] The bit lines BL**0** to BL**17** may be disposed below the word lines WL**0_1** to WL**11_1** of the first layer. The bit lines BL**0** to BL**17** may be lines for connecting the bit line pillars BLP**0** to BLP**35** and the bit line sense amplifier arrays **710** and **720**.

[0041] Referring to contacts of FIG. **7**, bit line pillars BLP**0** and BLP**18** may be connected to the bit line BL**0**. Accordingly, the bit line pillars BLP**0** and BLP**18** may be electrically identical bit lines. Bit line pillars BLP**6** and BLP**24** may be connected to the bit line BL**1**. Accordingly, the bit line pillars BLP**6** and BLP**24** may be electrically identical bit lines. Likewise, because the bit line pillars BLP**12** and BLP**30** are connected to the bit line BL**2**, the bit line pillars BLP**12** and BLP**30** may be identical bit lines.

[0042] That is, in FIG. **7**, bit line pillars BLPK and BLPK+18, where K is an integer between 0 and 17, may be identical bit lines electrically connected.

[0043] Half of the bit lines BL**0** to BL**17**, for example, even-numbered bit lines BL**0**, BL**2**, BL**4**, BL**6**, BL**8**, BL**10**, BL**12**, BL**14**, and BL**16** may be connected to the bit line sense amplifier array **710**, and the other half, for example, odd-numbered bit lines BL**1**, BL**3**, BL**5**, BL**7**, BL**9**, BL**11**, BL**13**, BL**15**, and BL**17** may be connected to the bit line sense amplifier array **720**. The bit line sense amplifier arrays **710** and **720** may sense and amplify data transmitted to connected bit lines. Each of the bit line sense amplifier arrays **710** and **720** may include a plurality of bit line sense amplifiers.

[0044] FIG. **8** is a side view of the cell array **600** illustrated in FIGS. **6** and **7**. In FIG. **8**, a third direction 'III' may be a direction orthogonal to a plane defined by the first direction 'I' and the second direction 'II' in FIGS. **6** and **8**.

[0045] Referring to FIG. **8**, it may be seen that each of the bit line pillars BLP**0**, BLP**6**, BLP**12**, BLP**18**, BLP**24**, and BLP**30** intersects with two word lines in each layer from the first layer to the N.sup.th layer. For example, it may be seen that the bit line pillar BLP**0** intersects with the word

lines WL**0**_**1** to WL**0**_N and WL**1**_**1** to WL**1**_N in the first layer to the N.sup.th layer. That is, each of the bit line pillars BLP**0**, BLP**6**, BLP**12**, BLP**18**, BLP**24**, and BLP**30** may intersect with 2×N word lines.

[0046] Below the word lines WL**0**_**1** to WL**11**_**1** of the first layer, the bit line BL**0** may be provided to electrically connect some (BLP**0** and BLP**18**, see FIG. **7**) of the bit line pillars BLP**0**, BLP**6**, BLP**12**, BLP**18**, BLP**24**, and BLP**30**.

[0047] FIG. **9** is a circuit diagram illustrating electrical connection among the word lines WL**0**_N to WL**11**_N, the bit line pillars BLP**0** to BLP**35**, and memory cells MC**0**_N to MC**71**_N of the N.sup.th layer in the cell array **600** illustrated in FIGS. **6** to **8**.

[0048] The memory cells MC**0**_N to MC**71**_N may be disposed at intersections between the bit line pillars BLP**0** to BLP**35** and the word lines WL**0**_N to WL**11**_N, respectively. Because each of the bit line pillars BLP**0** to BLP**35** intersects with two bit lines, the number of memory cells MC**0**_N to MC**71**_N in the N.sup.th layer may be twice the number of bit line pillars BLP**0** to BLP**35**. Each of the memory cells MC**0**_N to MC**71**_N may include a capacitor for storing data and a transistor for transmitting data stored in the capacitor to the bit line pillar under the control of the word line.

[0049] The following describes an operation when the word lines WL**0**_N, WL**2**_N, and WL**4**_N shorted to one another are simultaneously activated. As the word line WL**0**_N is activated, the transistors of the memory cells MC**0**_N to MC**5**_N may be turned on, so that data stored in the capacitors of the memory cells MC**0**_N to MC**5**_N may be transmitted to the bit line pillars BLP**0** to BLP**5**. As the word line WL**2**_N is activated, the transistors of the memory cells MC**12**_N to MC**17**_N are turned on, so that data stored in the capacitors of the memory cells MC**12**_N to MC**17**_N may be transmitted to the bit line pillars BLP**6** to BLP**11**. As the word line WL**4**_N is activated, the transistors of the memory cells MC**24**_N to MC**29**_N are turned on, so that data stored in the capacitors of the memory cells MC**24**_N to MC**29**_N may be transmitted to the bit line pillars BLP**12** to BLP**17**. The data of the bit line pillars BLP**0** to BLP**5** may be transmitted to the bit lines BL**0**, BL**3**, BL**6**, BL**9**, BL**12**, and BL**15**, the data of the bit line pillars BLP**6** to BLP**11** may be transmitted to the bit lines BL**1**, BL**4**, BL**7**, BL**10**, BL**13**, and BL**16**, and the data of the bit line pillars BLP**12** to BLP**17** may be transmitted to the bit lines BL**2**, BL**5**, BL**8**, BL**11**, BL**14**, and BL**17**. The data of the bit lines BL**0** to BL**17** may be sensed and amplified by the bit line sense amplifier arrays **710** and **720**.

[0050] Even when the word lines WL**1**_N, WL**3**_N, and WL**5**_N are simultaneously activated, even when the word lines WL**6**_N, WL**8**_N, and WL**10**_N are simultaneously activated, and even when the word lines WL**7**_N, WL**9**_N, and WL**11**_N are simultaneously activated, data of 18 memory cells may be transmitted to the bit line sense amplifier arrays **710** and **720** through 18 bit line pillars and 18 bit lines and be sensed and amplified as described above.

[0051] In the cell array **600** illustrated in FIGS. **6** to **9**, because the word lines WL are shorted by the three, the word lines WL may form a group by three and be simultaneously driven. With such a structure, the number of word lines WL that need to be driven may be reduced by ⅓, which may mean that an area of a word line driving circuit may be greatly reduced.

[0052] Although embodiments according to the technical idea of the present disclosure have been described above with reference to the accompanying drawings, this is only for describing the embodiments according to the concept of the present disclosure, and the present disclosure is not limited to the above embodiments. Various types of substitutions, modifications, and changes for the embodiments may be made by those skilled in the art, to which the present disclosure pertains, without departing from the technical idea of the present disclosure defined in the following claims, and it should be construed that these substitutions, modifications, and changes belong to the scope of the present disclosure. Furthermore, the embodiments may be combined to form additional embodiments.

Claims

1. A memory comprising: a plurality of word lines formed of N layers, M word lines being arranged in each layer, among the plurality of word lines, where each of N and M is an integer of 2 or more; a plurality of bit line pillars; and a plurality of memory cells disposed at intersections between the plurality of word lines and the plurality of bit line pillars, respectively, wherein two or more word lines of the plurality of word lines are grouped and driven together.
2. The memory of claim 1, wherein, among the plurality of word lines, the grouped word lines word lines are included in a same layer.
3. The memory of claim 2, wherein the plurality of bit line pillars are mutually electrically connected while forming a group in units of L, where L is an integer of 2 or more.
4. The memory of claim 3, wherein, among the bit line pillars, bit line pillars intersecting the grouped word lines are not mutually electrically connected.
5. The memory of claim 1, wherein each of the plurality of memory cells includes a transistor and a capacitor.
6. The memory of claim 1, wherein a first-half of the plurality of bit line pillars are connected to first bit line sense amplifiers disposed on a first side in a direction perpendicular to the plurality of bit line pillars, and a second-half of the plurality of bit line pillars are connected to second bit line sense amplifiers disposed on a second side in the direction perpendicular to the plurality of bit line pillars.
7. The memory of claim 1, wherein the grouped word lines among the plurality of word lines are shorted to each other.
8. The memory of claim 1, wherein each of the plurality of bit line pillars is disposed to pass between two word lines in each of the N layers.
9. A memory comprising: a plurality of word lines; a plurality of bit lines; and a plurality of memory cells connected to one of the plurality of word lines and one of the plurality of bit lines, wherein two or more word lines of the plurality of word lines are grouped and driven together.
10. The memory of claim 9, wherein the grouped word lines include a first word line and a second word line, and among the plurality of bit lines, first bit lines connected to memory cells connected to the first word line and second bit lines connected to memory cells connected to the second word line do not overlap each other.
11. The memory of claim 9, wherein each of the plurality of memory cells includes a transistor and a capacitor.