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(54) **ADAPTIVE CLOCK SIGNAL FREQUENCY SCALING**

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G06F 1/08	(2006.01)
G06F 1/324	(2019.01)
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G06F 1/3203	(2019.01)

(52) **U.S. Cl.**

CPC ***G06F 1/324*** (2013.01); ***G06F 1/08*** (2013.01); ***H03K 5/135*** (2013.01); *G06F 1/3203* (2013.01)

(58) **Field of Classification Search**

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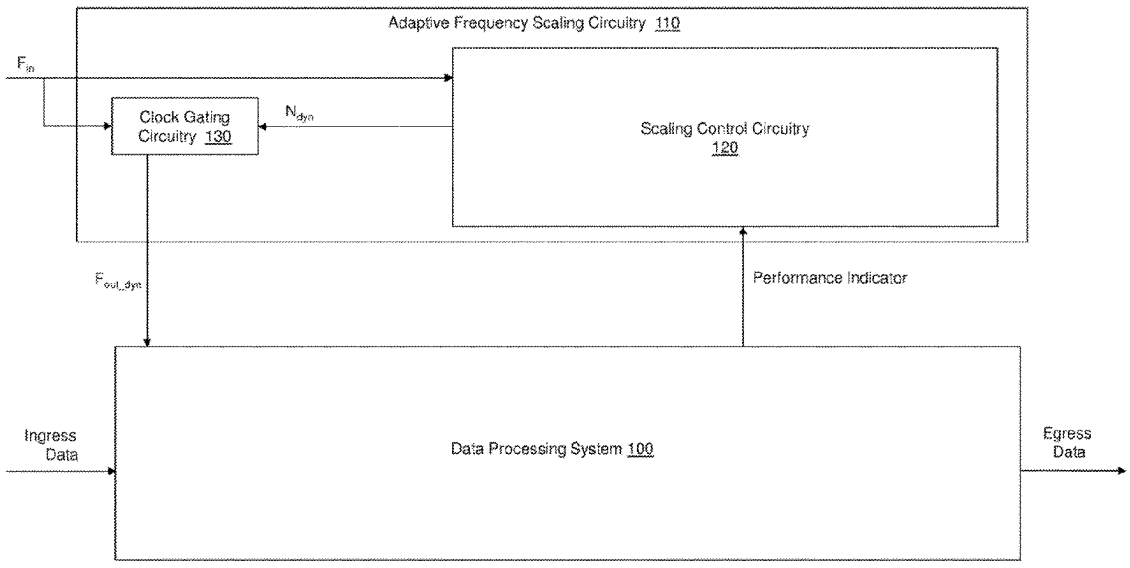
(57) **ABSTRACT**

Systems, methods, and circuitries are disclosed generating a dynamic clock signal having a dynamic clock signal frequency for a data processing system from an input clock signal having an input clock signal frequency. In one example, adaptive frequency scaling circuitry includes scaling control circuitry and clock gating circuitry. The scaling control circuitry includes hardware configured to receive a performance indicator value indicative of an operating parameter of the data processing system and select a dynamic clock gating control value based at least on the performance indicator value. The clock gating circuitry is configured to receive the dynamic clock gating control value, and in response, selectively gate the input clock signal based on the dynamic clock gating control value to generate the dynamic clock signal.

18 Claims, 5 Drawing Sheets



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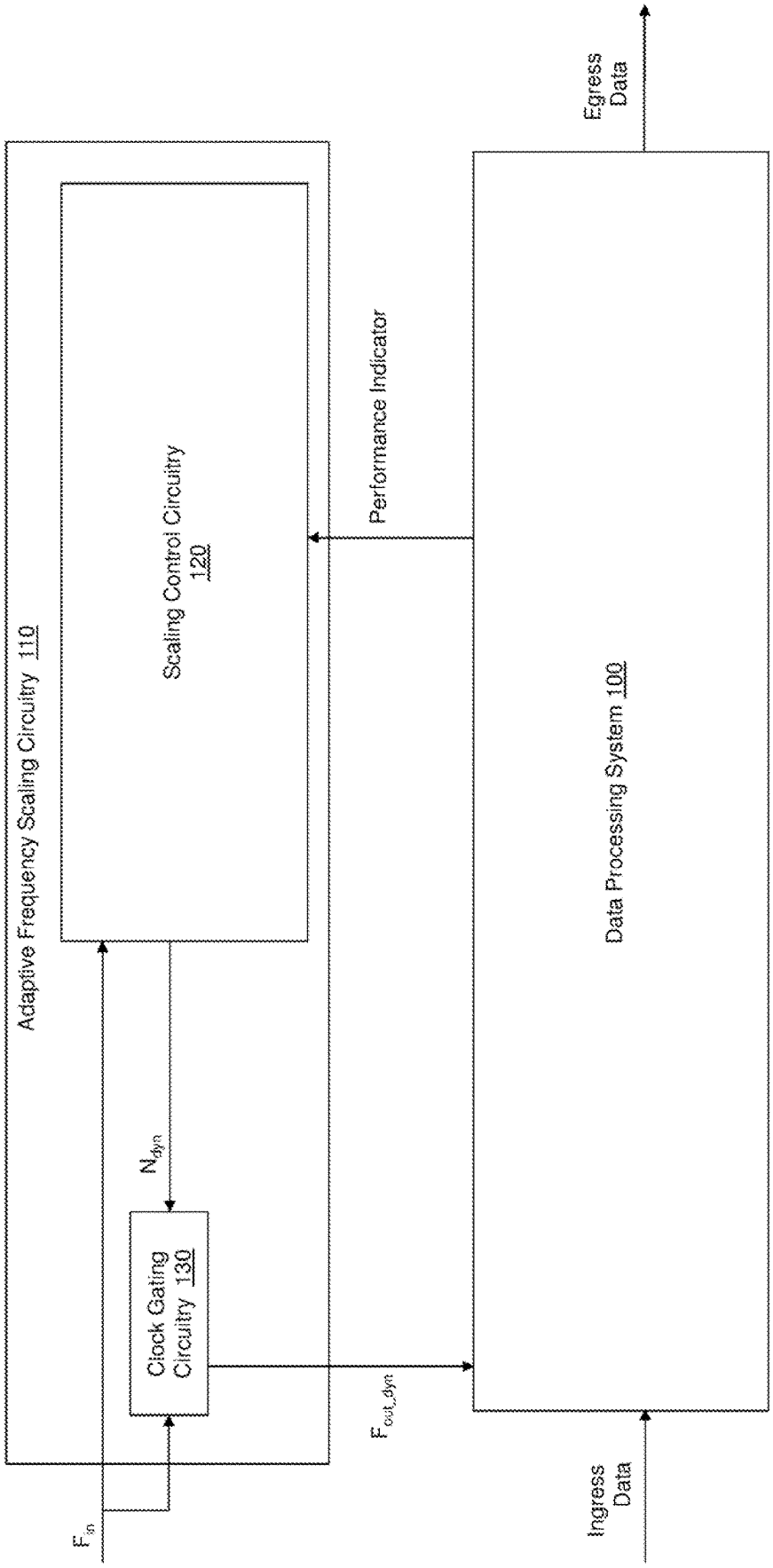
Egress Data
Adaptive Frequency Scaling Circuitry 110
Scaling Control Circuitry 120
Performance Indicator
Data Processing System 100
N_{dyn}
Clock Gating Circuitry 130
F_{out_dyn}
F_{in}
Ingress Data

FIG. 1

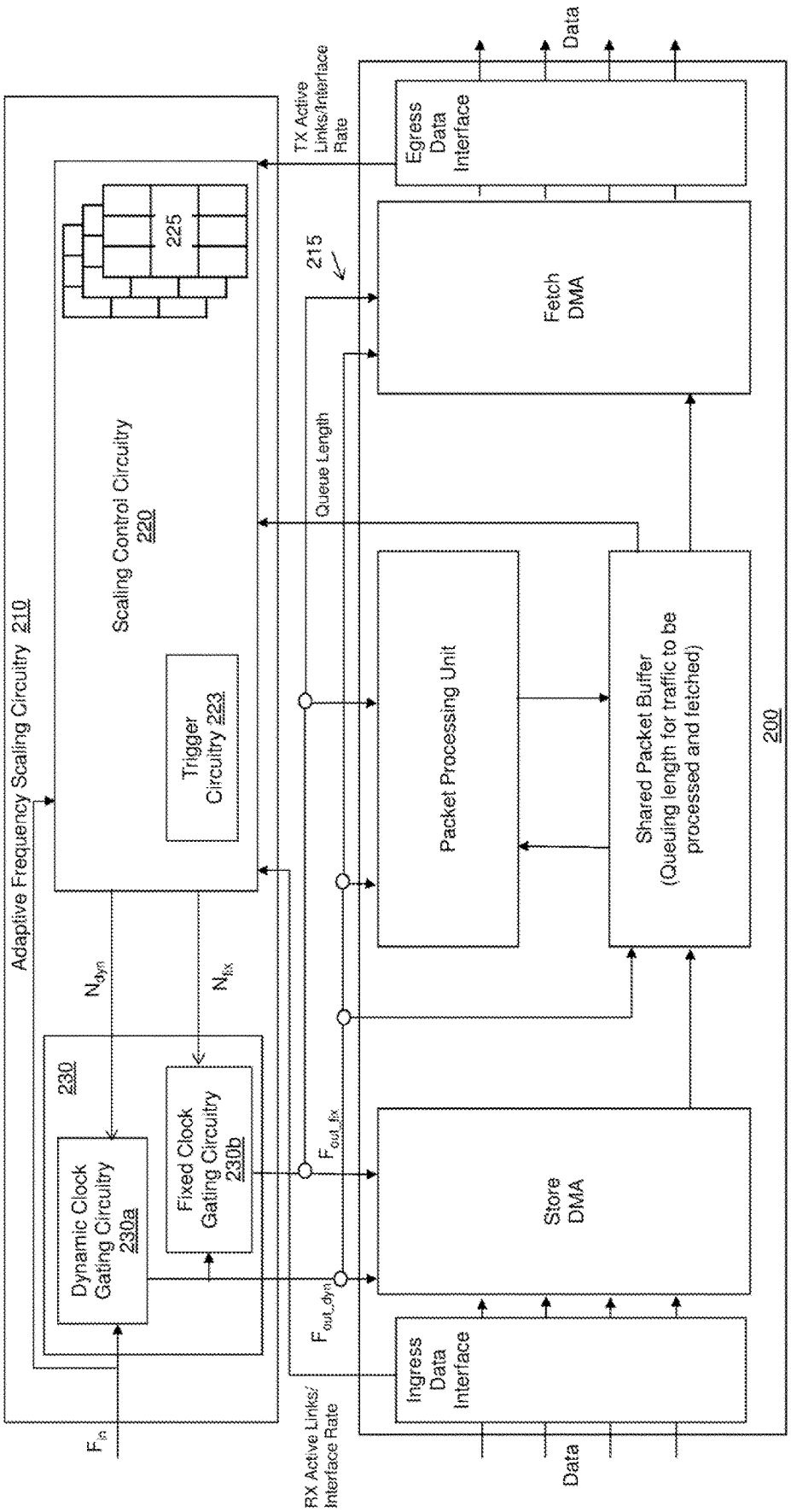
Adaptive Frequency Scaling Circuitry 210
Scaling Control Circuitry 220
225
Trigger Circuitry 223
230
Dynamic Clock Gating Circuitry 230a
Fixed Clock Gating Circuitry 230b
N_{dyn}
N_{fix}
F_{in}
F_{out_fix}
F_{out_dyn}
TX Active Links/Interface Rate
RX Active Links/ Interface Rate
Queue Length
215
Egress Data Interface
Fetch DMA
Packet Processing Unit
Shared Packet Buffer (Queuing length for traffic to be processed and fetched)
Store DMA
Ingress Data Interface
Data
Data
200

FIG. 2

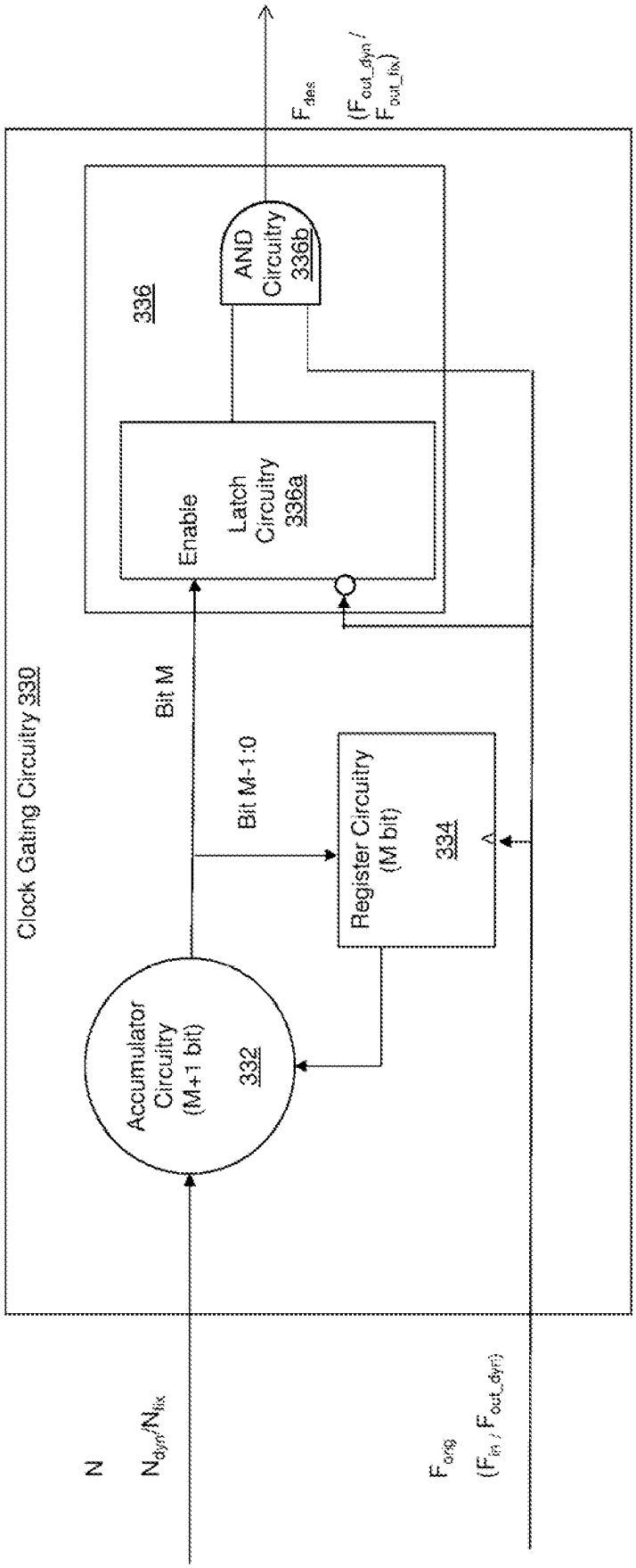
Clock Gating Circuitry 330
Accumulator Circuitry (M+1 bit) 332
Register Circuitry (M bit) 334
336
Enable
Latch Circuitry 336a
AND Circuitry 336b
Bit M
Bit M-1:0
N
N_{dyn}/N_{fix}
F_{orig}
(F_{in}, F_{out_dyn})
F_{des}
$(F_{out_dyn}, F_{out_fix})$

FIG. 3

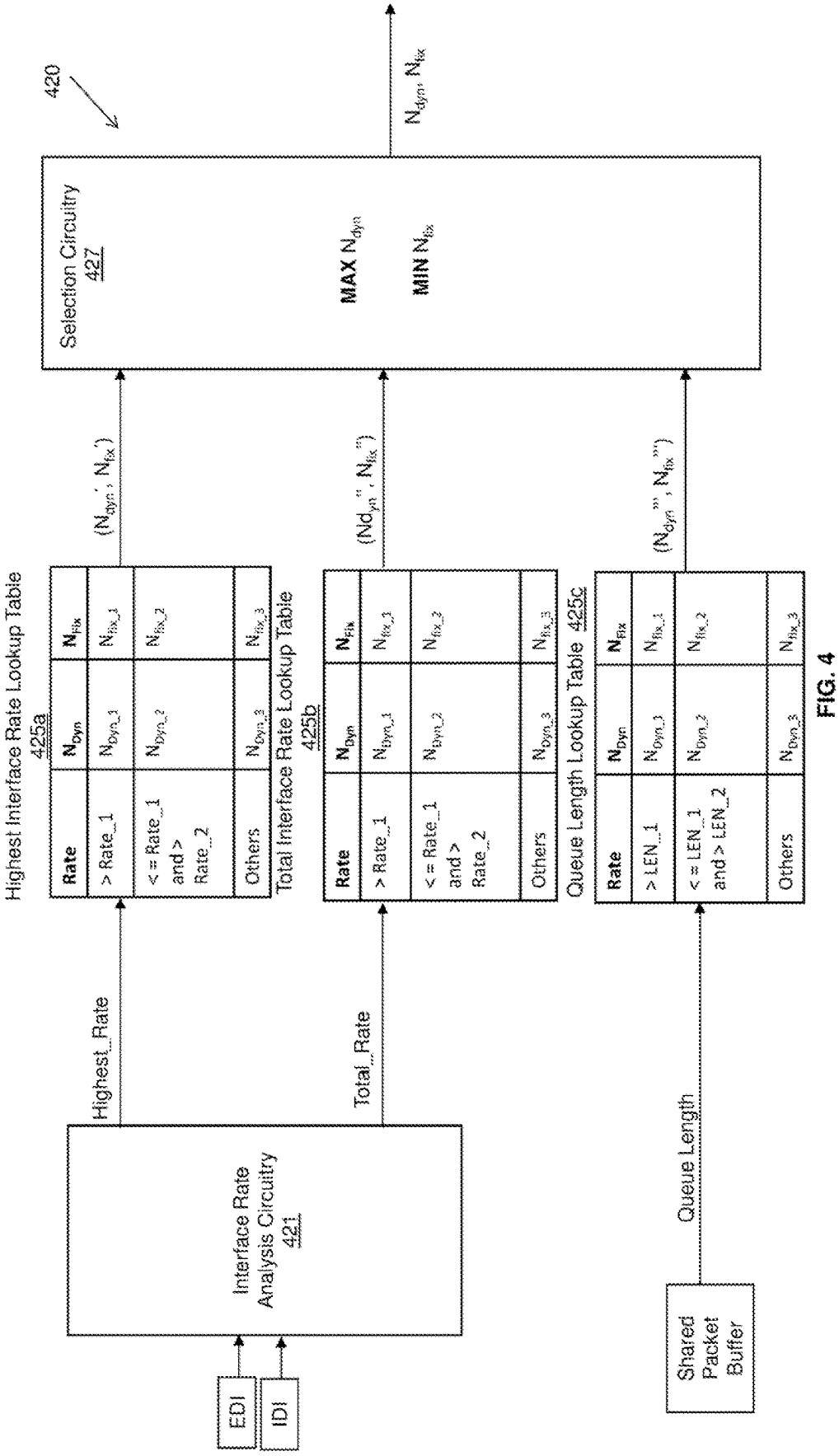
420
N_{dyn}, N_{fix}
Selection Circuitry
427
MAX N_{dyn}
MIN N_{fix}
(N_{dyn}', N_{fix}')
(Nd_{yn}", N_{fix}")
(N_{dyn}"', N_{fix}"')
Highest Interface Rate Lookup Table
425a
Total Interface Rate Lookup Table
425b
Queue Length Lookup Table
425c
Rate
N_{Dyn}
N_{Fix}
> Rate_1
< = Rate_1 and > Rate_2
Others
> LEN_1
< = LEN_1 and > LEN_2
N_{dyn_1}
N_{dyn_2}
N_{dyn_3}
N_{fix_1}
N_{fix_2}
N_{fix_3}
Highest_Rate
Total_Rate
Queue Length
Interface Rate Analysis Circuitry
421
EDI
IDI
Shared Packet Buffer

FIG. 4

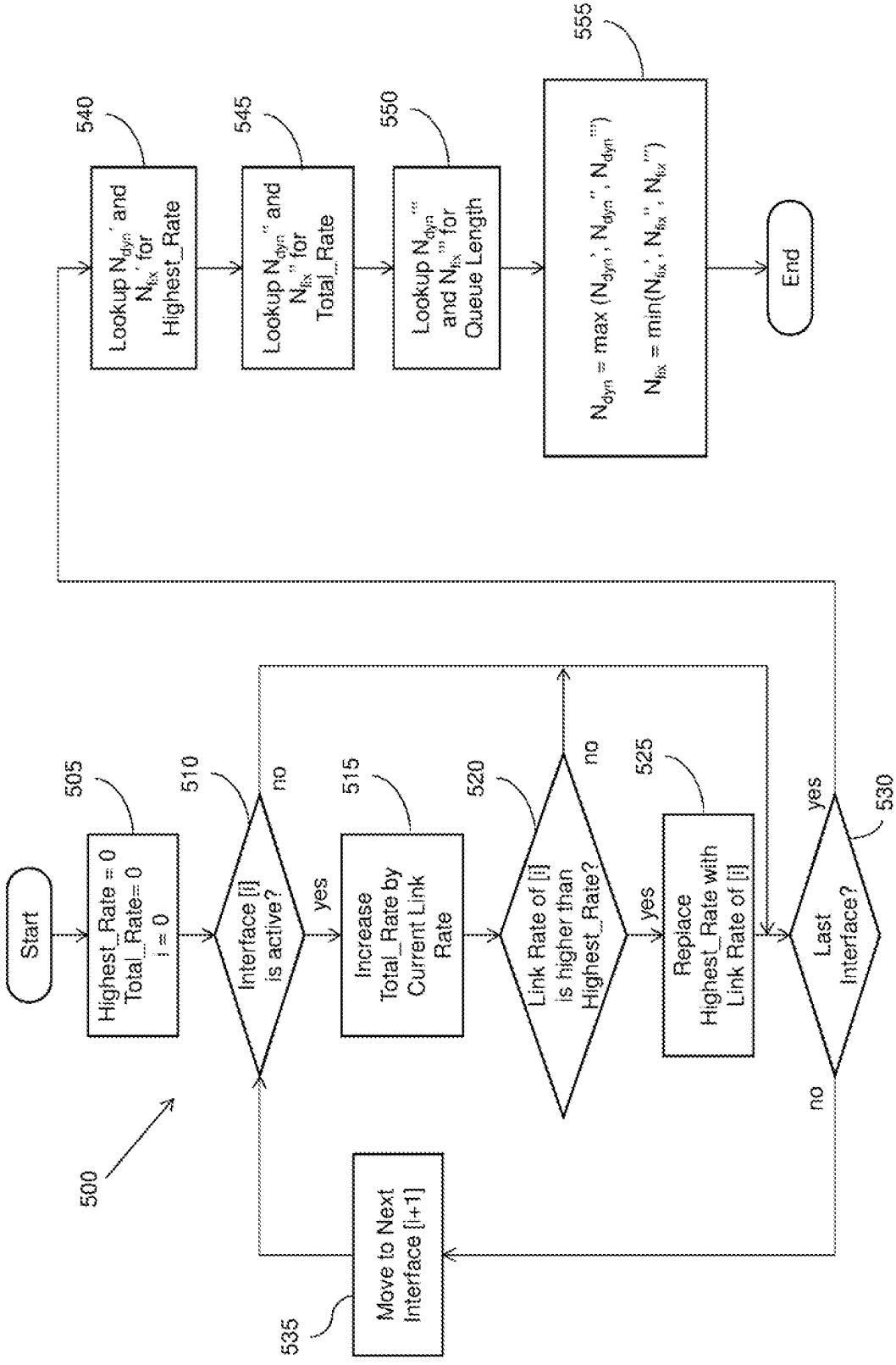
Start
Highest_Rate = 0
Total_Rate= 0
i = 0
505
Interface [i] is active?
510
no
yes
Increase Total_Rate by Current Link Rate
515
Link Rate of [i] is higher than Highest_Rate?
520
no
yes
Replace Highest_Rate with Link Rate of [i]
525
Last Interface?
530
yes
no
Move to Next Interface [i+1]
535
500
Lookup N_{dyn}' and N_{fix}' for Highest_Rate
540
Lookup N_{dyn}'' and N_{fix}'' for Total_Rate
545
Lookup N_{dyn}''' and N_{fix}''' for Queue Length
550
$N_{dyn} = \max(N_{dyn}', N_{dyn}'', N_{dyn}''')$
$N_{fix} = \min(N_{fix}', N_{fix}'', N_{fix}''')$
555
End

FIG. 5

ADAPTIVE CLOCK SIGNAL FREQUENCY SCALING

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 17/806,934, filed Jun. 14, 2022, titled ADAPTIVE CLOCK SIGNAL FREQUENCY SCALING, which is a continuation of U.S. patent application Ser. No. 16/134,174, filed Sep. 18, 2018, titled ADAPTIVE CLOCK SIGNAL FREQUENCY SCALING, each of which is incorporated herein by reference in their entireties.

BACKGROUND

Power optimization has become an important goal in integrated circuit design as integrated circuits are called upon to provide increasing functionality as the electronic devices that include the integrated circuits shrink in physical size. Clock tree power consumes up to 70% of total integrated circuit power and modern integrated circuit designs at 40 nm and below experience significantly increased clock tree power consumption. Power consumption is directly proportional to the voltage and frequency of the clock tree.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** illustrates an exemplary adaptive frequency scaling circuitry generating a dynamic clock signal from an input clock signal for a data processing system in accordance with various aspects described.

FIG. **2** illustrates an exemplary adaptive frequency scaling circuitry generating a dynamic clock signal and a fixed clock signal from an input clock signal for a data processing system in accordance with various aspects described.

FIG. **3** illustrates an exemplary clock gating circuitry for use in generating the dynamic clock signal in accordance with various aspects described.

FIG. **4** illustrates an exemplary scaling circuitry for use in generating the dynamic clock signal in accordance with various aspects described.

FIG. **5** illustrates an exemplary flow diagram of an exemplary method of adaptively scaling an input clock signal frequency in accordance with various aspects described.

DESCRIPTION

Because power consumption is directly related to clock signal frequency, many devices include means for reducing clock signal frequency when operating conditions of the device allow for satisfactory device performance at the reduced clock signal frequency. In many existing solutions, software is used to adjust the clock signal frequency according to the activity level of hardware components in the device. However, software-based control of clock signal frequency has a slow response time and may result in a drop in performance (e.g., packet loss in a networking device) in fast changing scenarios. Another disadvantage is that these solutions often rely on multiple phase locked loops (PLLs) to generate clock signals with different frequencies or divider circuits that can generate clocks signals with frequencies that are an integer fractions (e.g., ½, ⅓, . . . , and so on) of the original clock signal frequency.

Described herein are systems, circuitries, and methods that adaptively and dynamically generate a clock signal having a dynamic clock signal frequency that is determined based on operating conditions. The described adaptive clock signal generation systems, circuitries, and methods are hardware based rather than software based, meaning that the response time can be immediate (i.e., a single input clock signal cycle). Further, only a single PLL is needed and clock signal frequencies can be generated with a much finer granularity as compared to simple divider-based solutions.

The present disclosure will now be described with reference to the attached figures, wherein like reference numerals are used to refer to like elements throughout, and wherein the illustrated structures and devices are not necessarily drawn to scale. As utilized herein, terms "module", "component," "system," "circuit," "element," "slice," "circuitry," and the like are intended to refer to a set of one or more electronic components, a computer-related entity, hardware, software (e.g., in execution), and/or firmware. For example, circuitry or a similar term can be a processor, a process running on a processor, a controller, an object, an executable program, a storage device, and/or a computer with a processing device. By way of illustration, an application running on a server and the server can also be circuitry. One or more circuits can reside within the same circuitry, and circuitry can be localized on one computer and/or distributed between two or more computers. A set of elements or a set of other circuits can be described herein, in which the term "set" can be interpreted as "one or more."

As another example, circuitry or similar term can be an apparatus with specific functionality provided by mechanical parts operated by electric or electronic circuitry, in which the electric or electronic circuitry can be operated by a software application or a firmware application executed by one or more processors. The one or more processors can be internal or external to the apparatus and can execute at least a part of the software or firmware application. As yet another example, circuitry can be an apparatus that provides specific functionality through electronic components without mechanical parts; the electronic components can include one or more processors therein to execute executable instructions stored in computer readable storage medium and/or firmware that confer(s), at least in part, the functionality of the electronic components.

It will be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be physically connected or coupled to the other element such that current and/or electromagnetic radiation (e.g., a signal) can flow along a conductive path formed by the elements. Intervening conductive, inductive, or capacitive elements may be present between the element and the other element when the elements are described as being coupled or connected to one another. Further, when coupled or connected to one another, one element may be capable of inducing a voltage or current flow or propagation of an electro-magnetic wave in the other element without physical contact or intervening components. Further, when a voltage, current, or signal is referred to as being "applied" to an element, the voltage, current, or signal may be conducted to the element by way of a physical connection or by way of capacitive, electro-magnetic, or inductive coupling that does not involve a physical connection.

As used herein, a signal that is "indicative of" a value or other information may be a digital or analog signal that encodes or otherwise communicates the value or other information in a manner that can be decoded by and/or cause a responsive action in a component receiving the signal. The signal may be stored or buffered in computer readable storage medium prior to its receipt by the receiving com-

ponent and the receiving component may retrieve the signal from the storage medium. Further, a "value" that is "indicative of" some quantity, state, or parameter may be physically embodied as a digital signal, an analog signal, or stored bits that encode or otherwise communicate the value.

Use of the word example is intended to present concepts in a concrete fashion. The terminology used herein is for the purpose of describing particular examples only and is not intended to be limiting of examples. As used herein, the singular forms "a," "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes" and/or "including," when used herein, specify the presence of stated features, integers, steps, operations, elements and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components and/or groups thereof.

In the following description, a plurality of details is set forth to provide a more thorough explanation of the embodiments of the present disclosure. However, it will be apparent to one skilled in the art that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form rather than in detail in order to avoid obscuring embodiments of the present disclosure. In addition, features of the different embodiments described hereinafter may be combined with each other, unless specifically noted otherwise.

FIG. **1** illustrates a data processing system **100** that receives a dynamic clock signal having a frequency F_{out_dyn} from an exemplary adaptive frequency scaling circuitry **110**. The data processing system **100** includes digital electronic components such as integrated circuits (not shown) that input and operate according to the dynamic clock signal. In some of the examples below, the data processing system **105** is a network processing system. However, the data processing system can be any system that includes components clocked by the dynamic clock signal and that receives ingress data, manipulates the data, and produces egress data.

The adaptive frequency scaling circuitry **110** generates the dynamic clock signal from an input clock signal having a frequency F_{in}. The adaptive frequency scaling circuitry **110** includes scaling control circuitry **120** and clock gating circuitry **130**. The scaling control circuitry **120** includes hardware configured to receive a performance indicator value indicative of an operating parameter of the data processing system. The operating parameter is some characteristic of the data processing system (e.g., number of active links, buffer usage, and so on) that can be used to determine an appropriate clock signal frequency. The scaling control circuitry **120** hardware selects a dynamic clock gating control value N_{dyn} based at least on the performance indicator value, where N is an integer. The clock gating circuitry **130** receives the dynamic clock gating control value and, in response, selectively gates the input clock signal based on the dynamic clock gating control value to generate the dynamic clock signal.

FIG. **2** illustrates an exemplary adaptive frequency scaling circuitry **210** that generates a dynamic clock signal and a fixed clock signal for a network processing system **200**. The network processing system **200** includes an ingress data interface that receives packets from external components and an egress interface that transmits packets to external components. A store direct memory access (DMA) receives packets from the ingress data interface and stores the packets to shared packet buffer. The shared packet buffer stores and queues the packets to be processed and to be fetched. A packet processing unit reads full or partial packets and classifies the packets. The packet processing unit may also modify packets in the shared packet buffer. A fetch DMA fetches the packets from the shared packet buffer and transmits the packets to an egress data interface.

The various functional components of the network processing system **100** are implemented with several ICs (shown as the boxes). The distribution of the functional components of the network processing system amongst ICs may be different that that shown in FIG. **2** in other examples (i.e., some functional components may be provided on the same IC while other functional components are distributed amongst several ICs). Some electronic components in a given IC may require a fixed clock frequency while other components may be capable of operating at different clock frequencies. Because of this, the adaptive frequency scaling circuitry **210** generates a dynamic clock signal having a dynamic clock frequency that changes according to the performance indicator value and a fixed clock signal that has a constant clock frequency regardless of the performance indicator value. For the purposes of this description, the dynamic clock signal has a dynamic clock frequency that is changed by adaptive frequency scaling circuitry according to operating conditions of the data processing system, while the fixed clock signal has a fixed clock frequency that remain constant to provide an unchanging clock signal for IC components that require a constant clock. The scaling control circuitry **220** generates a dynamic clock gating control value N_{dyn} based on the performance indicator value. The scaling control circuitry **220** generates a fixed clock gating signal Nfix that will result in the frequency of the fixed clock signal remaining the same regardless of the performance indicator value.

The adaptive frequency scaling circuitry **210** includes a dynamic clock gating circuitry **230***a* that generates the dynamic clock signal and a fixed clock gating circuitry **230***b* that generates the fixed clock signal. As will be described in more detail with reference to FIG. **3**, the dynamic clock gating circuitry **230***a* selectively gates the input clock signal based on the dynamic clock gating control value to generate the dynamic clock signal. The fixed clock gating circuitry **230***b* selectively gates the dynamic clock signal based on the fixed clock gating control value to generate the fixed clock signal. The fixed clock gating circuitry **230***b* gates the dynamic clock signal, rather than the input clock signal, so that the dynamic clock signal and fixed clock signal remain in synchronization. Both clock signals are provided by way of a clock tree **215** to the ICs in the network processing system.

The scaling control circuitry **220** determines the clock gating control value for each clock gating circuitry based on performance indicators that include the link rate of the ingress interface and the egress interface, the link activity of the ingress interface and the egress interface, and one or several queue lengths in the shared packet buffer. Of course, in other examples different or additional performance indicators are used. As will be described in more detail with reference to FIG. **4**, the scaling control circuitry **220** includes pre-configured lookup tables that each map dynamic clock gating control values and fixed clock gating control values to values for one of the performance indicators.

In some examples, the scaling control circuitry **220** includes trigger circuitry **223** that causes the scaling control circuitry to generate new clock gating control values based on the current value of the performance indicator. For

example, the trigger circuitry **223** may be configured to count a predetermined integer number x of input clock cycles and cause the scaling control circuitry **220** to generate new clock gating control values on every xth input clock cycle. In other examples, the trigger circuitry **223** be configured to detect a change in the performance indicator value and cause the scaling circuitry to generate new clock gating control values when a performance indicator value change of a given significance occurs. In another example, the hardware of the scaling control circuitry **220** is clocked by the input clock signal and the clock gating control values are generated every cycle of the input clock signal.

FIG. **3** illustrates an exemplary M bit clock gating circuitry **330** that scales an original clock frequency F_{orig} (which can be either the input clock frequency Fin or the dynamic clock frequency F_{out_dyn}) to a desired clock frequency F_{des}. Over every 2^M original clock signal cycles, the clock gating circuitry passes N original clock signal pulses of the original clock signal to generate a desired (e.g., dynamic or fixed) clock signal having the desired clock frequency.

The clock gating circuitry **330** includes accumulator circuitry **332**, register circuitry **334**, and gate circuitry **336**. The accumulator circuitry **332** has M+1 bits with the most significant bit (MSB) M being an overflow bit. On every original clock signal cycle, the accumulator circuitry **332** receives M+1 bits corresponding to the value of N by way of a first input and M bits from the register circuitry **334** by way of a second input. The register circuitry **334** stores the values of the M−1:0 bits of the accumulator circuitry **332** in the prior clock cycle. Thus, with every cycle of the original clock signal, the content of accumulator circuitry **332** is increased by N. The gate circuitry **336** includes latch circuitry **336***a* and AND circuitry **336***b*. The latch circuitry **336***a* stores a value of 1 for every 0 value in the original clock signal. The MSB (bit M) of the accumulator is the clock enable of the latch circuitry **336***a* that causes the latch circuitry **336***a* to output the stored 1 value. The AND circuitry **336***b* outputs an original clock signal pulse when the output value of the latch circuitry **336***a* is 1 to generate the desired clock signal.

The desired clock signal has a desired clock frequency Fdes corresponding to F_{orig} $N/2^M$. With M being fixed by the size of the accumulator, the clock gating control value that will produce a desired clock frequency from a known original clock frequency can be determined as $F_{des} \cdot 2^M / F_{orig}$. For example given an 8 bit accumulator circuitry **332**, when $F_{des}=F_{orig}$ then N is 256 (2^8). This means that with every cycle of the original clock, the accumulator circuitry adds 0x100 (N) to 0x00 (contents of register circuitry **334**) and the output of the accumulator is 0x100. Since the MSB of the accumulator content is 1 on every original clock cycle, the gate circuitry will pass every pulse of the original clock signal. With the same 8 bit accumulator circuitry **332**, when $F_{des}=½ F_{orig}$ then N is 128 (0x80). This means that with every even cycle of the original clock, the accumulator circuitry adds 0x80 (N) to 0x00 (contents of register circuitry **334**) and the output of the accumulator is 0x80 meaning that the gate circuitry **334** does not pass an original clock signal pulse. With odd even cycle of the original clock, the accumulator circuitry adds 0x80 (N) to 0x80 (contents of register circuitry **334**) and the output of the accumulator is 0x100 meaning that the gate circuitry **334** does pass an original clock signal pulse. Since the MSB is 1 on every other original clock signal cycle, the gate circuitry **334** will pass every other pulse of the original clock signal.

With the illustrated clock gating circuitry **330**, the desired frequency granularity is very fine. For example, with M=7, +/−1% adjustment of the original clock frequency can be achieved. Also, the clock pulses in the desired clock signal are evenly enabled such that, for example, when M=7 and N=96, 75% of the clock frequency can be achieved.

FIG. **4** illustrates an exemplary scaling control circuitry **420** that generates the dynamic clock gating control value N_{dyn} and the fixed clock gating control circuitry N_{fix}. The scaling control circuitry includes an interface rate analysis circuitry **421** that receives performance indicator values corresponding to an interface rate from the ingress data interface (IDI) and the egress data interface (EDI) (see FIG. **2**). The interface rate analysis circuitry **421** finds the highest interface rate (Highest_Rate) from all the active links between the network processing system and external devices. For example, the interface rate for each link may be the link speed obtained via an auto negotiation process or an auto polling process. The activity status of each link may be indicated by RX_DV (Receive Data Valid) signals from a GMII/MII ingress data interface, RXC (Receive Control) signals from an XGMI ingress data interface, TX_EN (Transmit Enable) signals from a GMII/MII egress data interface, and/or TXC (Transmit Control) signals from an XGMII egress data interface which are analyzed by the interface rate analysis circuitry **421** to identify the highest interface rate.

The scaling control circuitry **420** includes a highest interface rate lookup table **425***a* that maps a dynamic clock gating control value N_{dyn}' and a fixed clock gating control value N_{fix}' to ranges of values for the highest interface rate determined by the interface rate analysis circuitry **421**. In the lookup table **425***a*, there are multiple entries. The highest interface rate is compared with the rate range defined in each entry, once match is found, then the dynamic clock gating control value N_{dyn}' and the fixed clock gating control value N_{fix}' for the match entry are selected.

The interface rate analysis circuitry **421** also tabulates the total interface rate (Total_Rate) from all the active links. For example, the interface rate for each link may be the link speed obtained via an auto negotiation process or an auto polling process. The activity status of each link may be indicated by RX_DV (Receive Data Valid) signals from a GMII/MII ingress data interface, RXC (Receive Control) signals from an XGMI ingress data interface, TX_EN (Transmit Enable) signals from a GMII/MII egress data interface, and/or TXC (Transmit Control) signals from an XGMII egress data interface which are combined by the interface rate analysis circuitry to calculate the total interface rate. The scaling control circuitry **420** includes a total interface rate lookup table **425***b* that maps a dynamic clock gating control value N_{dyn}" and a fixed clock gating control value N_{fix}" to ranges of values for the total interface rate determined by the interface rate analysis circuitry **421**. In the lookup table **425***b*, there are multiple entries. The total interface rate is compared with the range defined in each entry, once match is found, then the dynamic clock gating control value N_{dyn}" and the fixed clock gating control value N_{fix}" for the match entry are selected.

The scaling control circuitry **420** includes a queue length lookup table **425***c* that maps a dynamic clock gating control value N_{dyn}'" and a fixed clock gating control value N_{fix}'" to ranges of values a queue length for one or more queues in the shared packet buffer (see FIG. **2**). In the lookup table **425***c*, there are multiple entries. The queue length is compared with the range defined in each entry, once match is found, then the dynamic clock gating control value N_{dyn}'"

and the fixed clock gating control value N_{fix}''' for the match entry are selected. While only a single queue length is illustrated as a performance indicator in FIG. **4**, in some examples, the lengths of multiple queues in the shared packet buffer may each be a performance indicator, the lengths of multiple queues may be combined as a single performance indicator, and/or a length of the longest queue may be a performance indicator.

The scaling control circuitry **420** includes selection circuitry **427** that finds the maximum value of the clock gating control values output by the lookup tables **425***a*-**425***c* and the minimum value of the fixed clock gating control values output by the lookup tables **425***a*-**425***c*. The minimum fixed clock gating control value and the maximum dynamic clock gating control value are selected because the fixed clock frequency does not change but the fixed clock signal is derived from the dynamic clock signal which does change. In this manner the product of N_{dyn} and N_{fix} remains the same and the fixed clock signal will have a constant frequency. The selection circuitry **427** outputs the selected dynamic clock gating control value N_{dyn} and fixed clock gating control value N_{fix} to the dynamic clock gating circuitry and the fixed clock gating circuitry (see FIG. **2**), respectively.

FIG. **5** illustrates a flow diagram outlining an exemplary method **500** for generating a dynamic clock gating control value N_{dyn} and fixed clock gating control value N_{fix} for clock gating circuitries based on performance indicators. The method **500** may be performed by the scaling control circuitry **220** and/or **420** of FIGS. **2** and **4**, respectively. The method includes, at **505** initializing a value for Highest_Rate, Total_Rate, and a link identifier [i] to 0. Values for Highest_Rate, Total_Rate, and [i] may be stored in registers. At **510** a determination is made as to whether a next interface [i] is active. If the interface [i] is not active, the method continues to **530** where a check is made as to whether there are any interfaces that have not been analyzed. If at **510** the next interface [i] is active, at **515** the Total_Rate value is increase by the link rate of the interface [i]. At **520** a determination is made as to whether the link rate of interface [i] is higher than the value for Highest_Rate, and if so, at **525** the value for Highest_Rate is replaced with the link rate of interface [i]. At **530** if the last interface has not been analyzed, the method moves to **535** where a next interface [i+1] is identified and **510**-**530** are performed again.

Once all active interfaces have been analyzed, at **540** N_{dyn}' and N_{fix}' are selected based on the value for Highest_Rate. At **550** N_{dyn}'' and N_{fix}'' are selected based on the value for Total_Rate. At **550** N_{dyn}''' and N_{fix}''' are selected based on a value for queue length in a shared packet buffer. At **555**, the method includes selecting a maximum of N_{dyn}', N_{dyn}'', and N_{dyn}''' as dynamic clock gating control value N_{dyn} and a minimum of N_{fix}', N_{fix}'', and N_{fix}''' as fixed clock gating control value N_{fix}.

While the invention has been illustrated and described with respect to one or more implementations, alterations and/or modifications may be made to the illustrated examples without departing from the spirit and scope of the appended claims. In particular regard to the various functions performed by the above described components or structures (assemblies, devices, circuits, systems, etc.), the terms (including a reference to a "means") used to describe such components are intended to correspond, unless otherwise indicated, to any component or structure which performs the specified function of the described component (e.g., that is functionally equivalent), even though not structurally equivalent to the disclosed structure which performs the function in the herein illustrated exemplary implementations of the invention.

Examples can include subject matter such as a method, means for performing acts or blocks of the method, at least one machine-readable medium including instructions that, when performed by a machine cause the machine to perform acts of the method or of an apparatus or system for dynamically generating a clock signal for a data processing system according to embodiments and examples described herein.

Example 1 is an adaptive frequency scaling circuitry configured to generate a dynamic clock signal having a dynamic clock signal frequency for a data processing system from an input clock signal having an input clock signal frequency. The adaptive frequency scaling circuitry includes scaling control circuitry and clock gating circuitry. The scaling control circuitry including hardware is configured to receive a performance indicator value indicative of an operating parameter of the data processing system and select a dynamic clock gating control value based at least on the performance indicator value. The clock gating circuitry is configured to receive the dynamic clock gating control value, and in response, selectively gate the input clock signal based on the dynamic clock gating control value to generate the dynamic clock signal.

Example 2 includes the subject matter of example 1, including or omitting optional elements, wherein the scaling control circuitry includes interface rate analysis circuitry and lookup table. The interface rate analysis circuitry is configured to receive signals indicative of interface rates of active links between the data processing system and external devices; identify a highest interface rate; and output the performance indicator value indicative of the highest interface rate. The lookup table is configured to input the performance indicator value and output a dynamic clock gating control value mapped to the highest interface rate.

Example 3 includes the subject matter of example 1, including or omitting optional elements, wherein the scaling control circuitry includes interface rate analysis circuitry and a lookup table. The interface rate analysis circuitry is configured to receive signals indicative of interface rates of active links between the data processing system and external devices; compute a total interface rate based on the interface rates; and output the performance indicator value indicative of the total interface rate. The lookup table is configured to input the performance indicator value and output a dynamic clock gating control value mapped to the total interface rate.

Example 4 includes the subject matter of example 1, including or omitting optional elements, wherein the scaling circuitry further includes a lookup table configured to input a performance indicator value indicative of a length of a queue in a shared packet buffer of the data processing system and output a dynamic clock gating control value mapped to the queue length.

Example 5 includes the subject matter of example 1, including or omitting optional elements, wherein the scaling circuitry includes a plurality of lookup tables and selection circuitry. The plurality of lookup tables input a respective plurality of performance indicator values and output a respective plurality of dynamic clock gating control values. The selection circuitry is configured to select one of the plurality of dynamic clock gating control values and provide the selected dynamic clock gating control value to the clock gating circuitry.

Example 6 includes the subject matter of example 1, including or omitting optional elements, wherein the dynamic clock gating control value is indicative of an

integer N and the clock gating circuitry includes: accumulator circuitry having M+1 bits, wherein the accumulator is configured to combine a first input value and a second input value and output M+1 bits corresponding to a sum of the first value and the second value, further wherein the first input value is N; register circuitry configured to store bits M−1 to 0 of the output M+1 bits from the accumulator and provide the stored bits to the accumulator as the second value; and gate circuitry configured to output the dynamic clock signal by passing an input clock signal pulse in response to bit M in the output M+1 bits from the accumulator being 1; and the scaling control circuitry is configured to determine N based at least on a desired frequency and M.

Example 7 includes the subject matter of example 1, including or omitting optional elements, wherein the scaling control circuitry generates the dynamic clock gating signal and a fixed clock gating signal, the clock gating circuitry includes a first clock gating circuitry configured to receive the dynamic clock gating control value, and in response, selectively gate the input clock signal based on the dynamic clock gating control value to generate a dynamic clock signal having a desired dynamic clock frequency. A second clock gating circuitry is configured to receive the fixed clock gating control value, and in response, selectively gate the dynamic clock signal based on the fixed clock gating control value to generate a fixed clock signal having a fixed clock frequency, wherein the fixed clock signal frequency remains constant regardless of the performance indicator value.

Example 8 includes the subject matter of example 7, including or omitting optional elements, wherein the scaling circuitry includes a plurality of lookup tables and selection circuitry. The plurality of lookup tables input a respective plurality of performance indicator values and output a respective plurality of dynamic clock gating control values and a respective plurality of fixed clock gating control values. The selection circuitry configured to select one of the plurality of dynamic clock gating control values; select one of the plurality of fixed clock gating control values, such that the selected fixed clock gating control value, when used to gate the dynamic clock signal, will generate a fixed clock signal having the fixed clock signal frequency; and provide the selected dynamic clock gating control value and the selected fixed clock gating control value to the clock gating circuitry.

Example 9 includes the subject matter of example 1, including or omitting optional elements, wherein the scaling control circuitry further includes trigger circuitry configured to cause the scaling control circuitry to determine a subsequent desired dynamic clock frequency for the data processing system on every xth cycle of the input clock signal, where x is a predetermined integer.

Example 10 is a method, including receiving a performance indicator value indicative of an operating parameter of a data processing system; selecting a dynamic clock gating control value based at least on the performance indicator value; and gating an input clock signal based at least on the dynamic clock gating control value to generate a dynamic clock signal.

Example 11 includes the subject matter of example 10, including or omitting optional elements, wherein selecting a dynamic clock gating control value includes inputting the performance indicator value to a lookup table and selecting an output of the lookup table as the clock gating control value.

Example 12 includes the subject matter of example 10, including or omitting optional elements, further including: selecting a fixed clock gating control value based on the dynamic clock gating control value and a fixed clock frequency; and gating the dynamic clock signal based at least on the fixed clock gating control value to generate a fixed clock signal having the fixed clock frequency.

Example 13 includes the subject matter of example 10, including or omitting optional elements, wherein gating the input clock signal to generate the dynamic clock signal includes, for each cycle of the input clock signal: inputting M+1 bits corresponding to the dynamic clock gating control value to an accumulator having M+1 bits; inputting M bits corresponding to bits M−1:0 of the accumulator at a prior input clock cycle to the accumulator; and passing an input clock signal pulse in response to bit M of the accumulator being 1.

Example 14 includes the subject matter of example 13, including or omitting optional elements, further including determining the dynamic clock gating control value as a product of a desired dynamic clock signal frequency and 2M divided by an input clock frequency of the input clock signal.

Example 15 includes the subject matter of example 10, including or omitting optional elements, further including: receiving a performance indicator value indicative of a plurality of operating parameters of a data processing system; determining a plurality of dynamic clock gating control values, wherein each of the determined dynamic clock gating control values in the plurality of dynamic clock gating control values is based a different one of the plurality performance indicator values; selecting a maximum dynamic clock gating control value from amongst the determined dynamic clock gating control values; and gating an input clock signal based at least on the maximum dynamic clock gating control value to generate the dynamic clock signal.

Example 16 includes the subject matter of example 10, including or omitting optional elements, wherein the performance indicator value is indicative of one or more of a highest interface rate amongst active links between the data processing system and external devices, a highest interface rate amongst active links between the data processing system and the external devices, and a queue length in a shared packet buffer in the data processing system.

Example 17 is a clock gating circuitry configured to gate an original clock signal having an original clock frequency to generate a desired clock signal having a desired clock frequency based on a clock gating control value N. The clock gating circuitry includes accumulator circuitry having M+1 bits, wherein the accumulator is configured to combine a first input value and a second input value and output M+1 bits corresponding to a sum of the first value and the second value, further wherein the first input value is N; register circuitry configured to store bits M−1 to 0 of the output M+1 bits from the accumulator and provide the stored bits to the accumulator as the second value; and gate circuitry configured to output the desired clock signal by passing an original clock signal pulse in response to bit M in the output M+1 bits from the accumulator being 1.

Example 18 includes the subject matter of example 17, including or omitting optional elements, wherein the original clock signal is a clock signal that is output by another clock gating circuitry.

Example 19 is a method, including, until all active interfaces have been analyzed: identifying an active interface between a data processing system and an external device; increasing a total rate value by a link rate of the active interface; and replacing a highest rate value with the link rate when the link rate is higher than the highest rate value;

selecting a first dynamic clock gating control value based on the total rate value; selecting a second dynamic clock gating control value based on the highest rate value; selecting a third dynamic clock gating control value based on a queue length value; and providing, to a clock gating circuitry, a maximum of the first dynamic clock gating control value, the second dynamic clock gating control value, and the third dynamic clock gating control value as a dynamic clock gating control value, wherein the clock gating circuitry generates a dynamic clock signal from an input clock signal based at least on the maximum dynamic clock gating control value.

Example 20 includes the subject matter of example 19, including or omitting optional elements, further including: selecting a first fixed clock gating control value based on the total rate value; selecting a second fixed clock gating control value based on the highest rate value; selecting a third fixed clock gating control value based on a queue length value; and providing, to a second clock gating circuitry, a minimum of the first fixed clock gating control value, the second fixed clock gating control value, and the third fixed clock gating control value as a fixed clock gating control value, wherein a second clock gating circuitry generates a fixed clock signal from the dynamic clock signal based at least on the minimum fixed clock gating control value.

Various illustrative logics, logical blocks, modules, and circuits described in connection with aspects disclosed herein can be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform functions described herein. A general-purpose processor can be a microprocessor, but, in the alternative, processor can be any conventional processor, controller, microcontroller, or state machine. The various illustrative logics, logical blocks, modules, and circuits described in connection with aspects disclosed herein can be implemented or performed with a general purpose processor executing instructions stored in computer readable medium.

The above description of illustrated embodiments of the subject disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosed embodiments to the precise forms disclosed. While specific embodiments and examples are described herein for illustrative purposes, various modifications are possible that are considered within the scope of such embodiments and examples, as those skilled in the relevant art can recognize.

In this regard, while the disclosed subject matter has been described in connection with various embodiments and corresponding Figures, where applicable, it is to be understood that other similar embodiments can be used or modifications and additions can be made to the described embodiments for performing the same, similar, alternative, or substitute function of the disclosed subject matter without deviating therefrom. Therefore, the disclosed subject matter should not be limited to any single embodiment described herein, but rather should be construed in breadth and scope in accordance with the appended claims below.

In particular regard to the various functions performed by the above described components (assemblies, devices, circuits, systems, etc.), the terms (including a reference to a "means") used to describe such components are intended to correspond, unless otherwise indicated, to any component or structure which performs the specified function of the described component (e.g., that is functionally equivalent), even though not structurally equivalent to the disclosed structure which performs the function in the herein illustrated exemplary implementations of the disclosure. In addition, while a particular feature may have been disclosed with respect to only one of several implementations, such feature may be combined with one or more other features of the other implementations as may be desired and advantageous for any given or particular application. The use of the phrase "one or more of A, B, or C" is intended to include all combinations of A, B, and C, for example A, A and B, A and B and C, B, and so on.

What is claimed is:

1. Adaptive frequency scaling circuitry having synchronizing dynamic and fixed clock signals, the circuitry comprising:

dynamic clock gating circuitry configured to modulate an input clock signal based on one or more performance values to produce a dynamic clock signal with an adjustable frequency;

fixed clock gating circuitry coupled to the dynamic clock gating circuitry and configured to output a fixed clock signal from the dynamic clock signal, wherein the fixed clock gating circuitry maintains the output of the fixed clock signal when the dynamic clock gating circuitry modulates the input clock signal for causing a frequency change to the adjustable frequency; and

packet processing circuitry including a shared packet buffer, wherein the one or more performance values includes a queue length of the shared packet buffer.

2. The circuitry of claim **1**, wherein the fixed clock gating circuitry is further configured to maintain the frequency of the fixed clock signal by gating the dynamic clock signal based on a fixed clock gating control value, thereby synchronizing the fixed clock signal with the dynamic clock signal during the frequency change.

3. The circuitry of claim **1**, wherein the dynamic clock gating circuitry is further configured to selectively gate the input clock signal based on a dynamic clock gating control value, the dynamic clock control value based on one or more performance indicators.

4. The circuitry of claim **3**, wherein the one or more performance indicators include one or more of: a link rate, a link activity status, one or more queue lengths in a buffer, a total interface rate from at least one link, a buffer link activity of a total interface rate, a minimum interface rate, a maximum interface rate, a link activity, or a buffer queue length.

5. The circuitry of claim **4**, further comprising a trigger circuitry configured for dynamic adjustment of clock frequencies, the trigger circuitry configured for:

determining a change to the one or more performance indicators; and

causing the scaling circuitry to output a new clock gating control value based the change to the one or more performance indicators.

6. The circuitry of claim **4**, further comprising a trigger circuitry configured for:

determining a number of cycles (n); and

causing, when the number of cycles (n) corresponds to a predetermined integer number, the scaling circuitry to output a new dynamic clock gating control value.

7. The circuitry of claim **1**, wherein the dynamic clock gating circuitry is configured for frequency change adjustments corresponding to +/−1% of an original clock frequency.

8. A circuitry for adaptive clock frequency scaling in a data processing system having a dynamic clock configured to output a dynamic clock signal and a fixed clock configured to output a fixed clock signal, the circuitry comprising:

an interface rate circuitry configured to determine rates of data transfer across one or more interfaces of the data processing system and determine clock gating control values based on the rates of data transfer;

a plurality of lookup tables configured to correlate one or more performance indicators to the clock gating control values; and

a selection circuitry configured to utilize the plurality of look up tables to determine the clock gating control values to be applied to dynamic and fixed clock gating circuitries, thereby synchronizing the fixed clock signal to the dynamic clock signal.

9. The circuitry of claim 8, further comprising a scaling control circuitry, the scaling control circuitry comprising an interface rate analysis circuitry configured to:

determine the highest interface rate from active links between the data processing system and/or one or more external devices; and

determine a dynamic clock gating control value based on this highest interface rate.

10. The circuitry of claim 9, wherein the scaling control circuitry includes a highest interface rate lookup table configured to correlate the highest interface rate to a corresponding dynamic clock gating control value, for selecting the control value based on the determined highest interface rate.

11. The circuitry of claim 9, wherein the scaling control circuitry includes a total interface rate lookup table configured to correlate a total interface rate, based on a plurality of active links, to a dynamic clock gating control value, thereby allowing a frequency of the dynamic clock signal to be adjusted based on a cumulative data transfer rate of the system.

12. The circuitry of claim 11, wherein the total interface rate is based on a plurality of active links of the data processing system and/or external devices.

13. The circuitry of claim 11, wherein the scaling control circuitry includes a queue length lookup table configured to correlate a queue length value to dynamic clock gating control values, thereby facilitating an adjustment of the frequency of the dynamic clock signal based on a data processing load.

14. The circuitry of claim 13, further comprising a packet processing circuitry having a shared packet buffer, wherein the queue length value corresponds to a number of packets in the shared packet buffer.

15. The circuitry of claim 9, wherein the scaling control circuitry comprises a selection circuitry configured to determine a final dynamic clock gating control value based on a maximum value of performance metrics corresponding to the dynamic clock gating control.

16. The circuitry of claim 15, wherein the maximum value of performance metrics are based on one or more of: the highest interface rate, total interface rate, and queue length lookup tables.

17. A method for synchronizing clocks in adaptive frequency scaling for a data processing system, the method comprising:

modulating, using a dynamic clock gating circuitry, an input clock signal to produce a dynamic clock signal with an adjustable frequency;

outputting a fixed clock signal from the dynamic clock signal using a fixed clock gating circuitry, wherein the fixed clock signal is constant when the adjustable frequency undergoes an adjustment

determining one or more performance indicators based on one or more of an interface rate or a queue length;

determining a clock gating control value based on the one or more performance indicators;

outputting the clock gating control value to cause the adjustment of the dynamic clock signal; and

outputting the fixed clock signal, the fixed clock signal being synchronized to the dynamic clock signal.

18. The method of claim 17, wherein selecting clock gating control values based on analyzed performance indicators includes:

determining, utilizing a first lookup table, a highest interface rate;

determining, utilizing a second lookup table, a total interface rate;

determining, utilizing a third lookup table, a queue length value;

determining, based on the highest interface rate, the total interface rate, and the queue length value, a maximum clock gating control value; and

outputting a clock control signal based on the maximum clock gating control value.

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