US 20250261383A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2025/0261383 A1**

Lee et al. (43) **Pub. Date: Aug. 14, 2025**

(54) **CAPACITOR STRUCTURE**

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(21) Appl. No.: **19/193,888**

(22) Filed: **Apr. 29, 2025**

Related U.S. Application Data

(62) Division of application No. 17/946,048, filed on Sep. 16, 2022, now Pat. No. 12,324,170.

(30) **Foreign Application Priority Data**

Jul. 21, 2022 (TW) 111127294

Publication Classification

(51) **Int. Cl.**

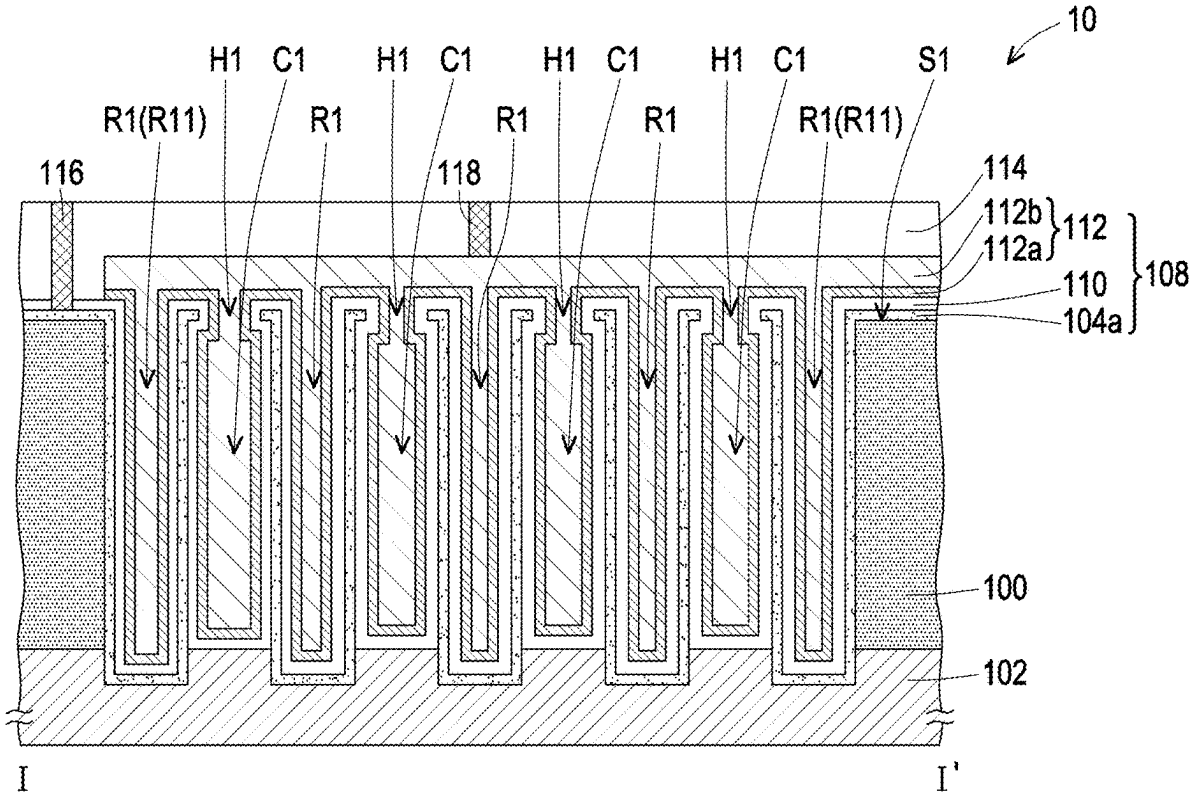
H10D 1/62 (2025.01)
H10D 1/00 (2025.01)
H10D 64/01 (2025.01)

(52) **U.S. Cl.**

CPC ***H10D 1/62*** (2025.01); ***H10D 1/045*** (2025.01); ***H10D 64/01*** (2025.01)

(57) **ABSTRACT**

A capacitor structure including a silicon material layer, a support frame layer, and a capacitor is provided. The support frame layer is disposed in the silicon material layer. The support frame layer has recesses. There is a cavity between two adjacent recesses. The support frame layer is located between the cavity and the recess. The support frame layer has a through hole directly above the cavity. The capacitor is disposed in the silicon material layer. The capacitor includes a first insulating layer and a first electrode layer. The first insulating layer is disposed on the support frame layer. The first electrode layer is disposed on the first insulating layer and fills the recess and the cavity.



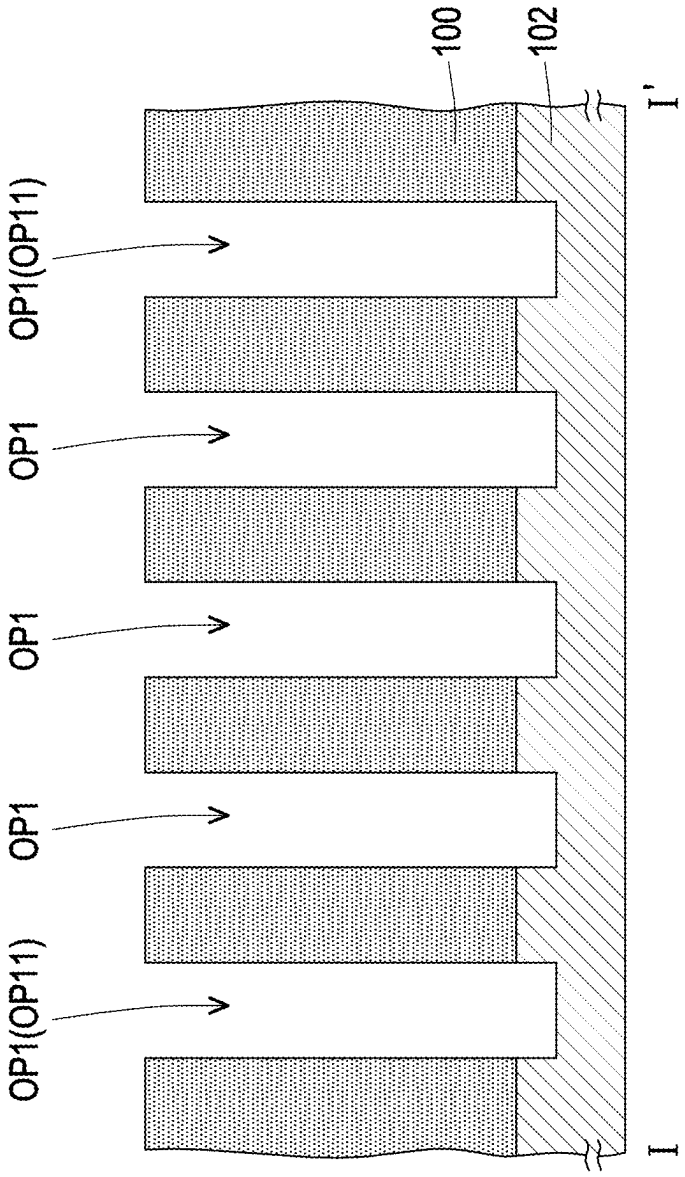


FIG. 1A

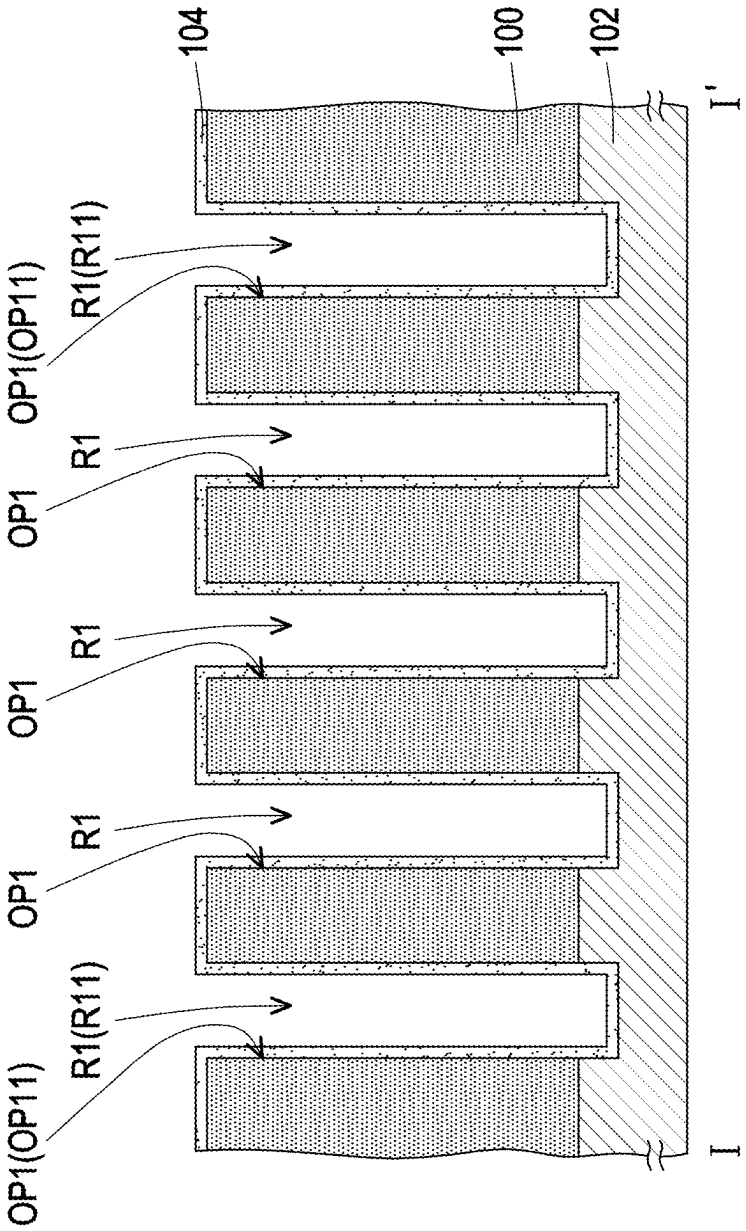

104
100
102
I'
I
OP1(OP11)
R1(R11)
OP1
R1
OP1
R1
OP1
R1
OP1(OP11)
R1(R11)

FIG. 1B

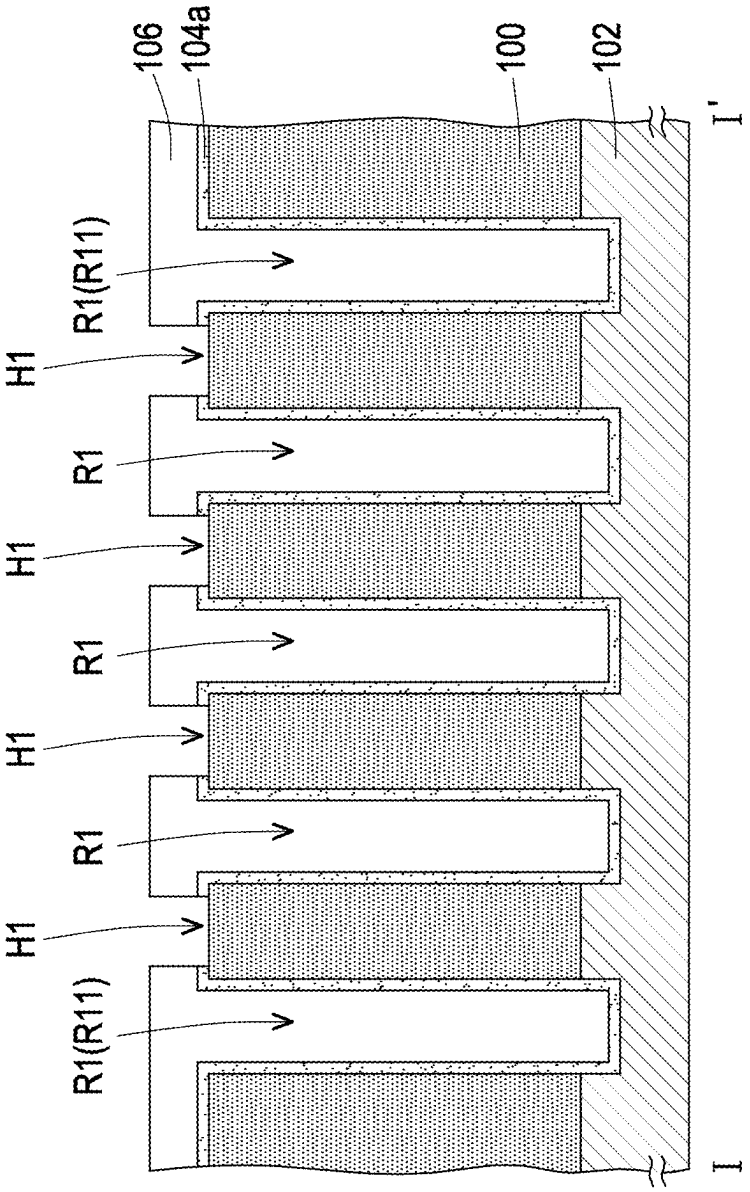


FIG. 1C

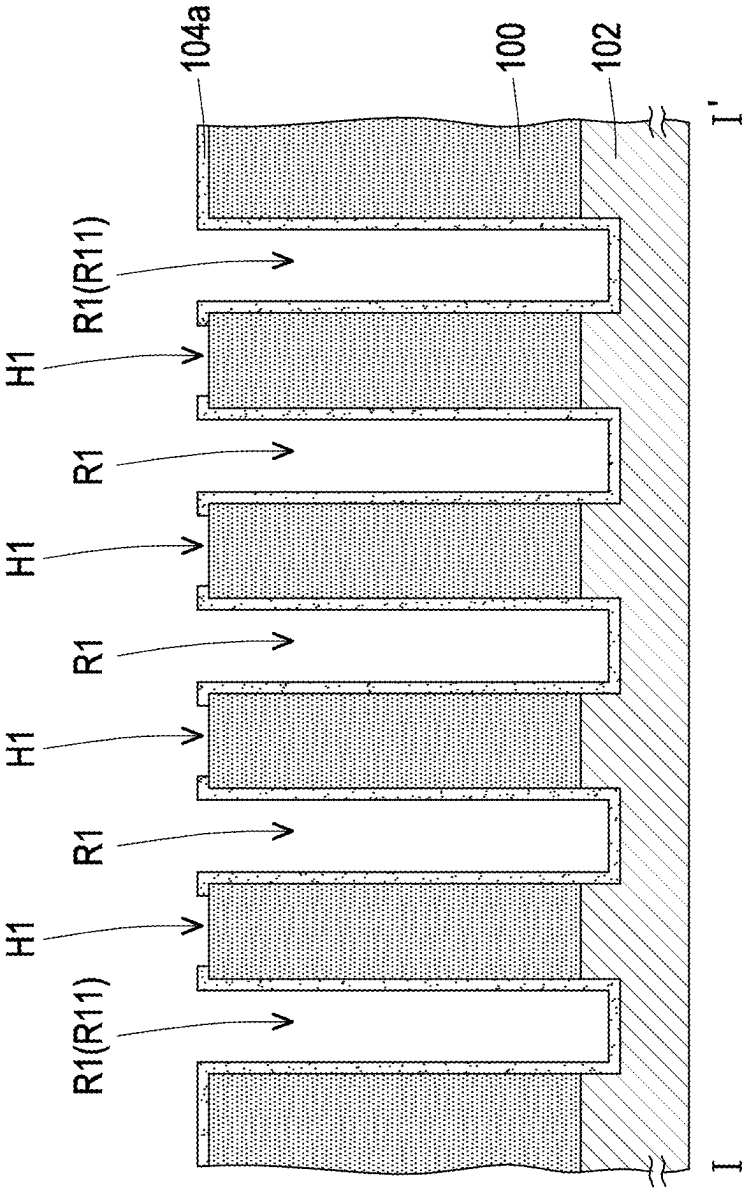


FIG. 1D

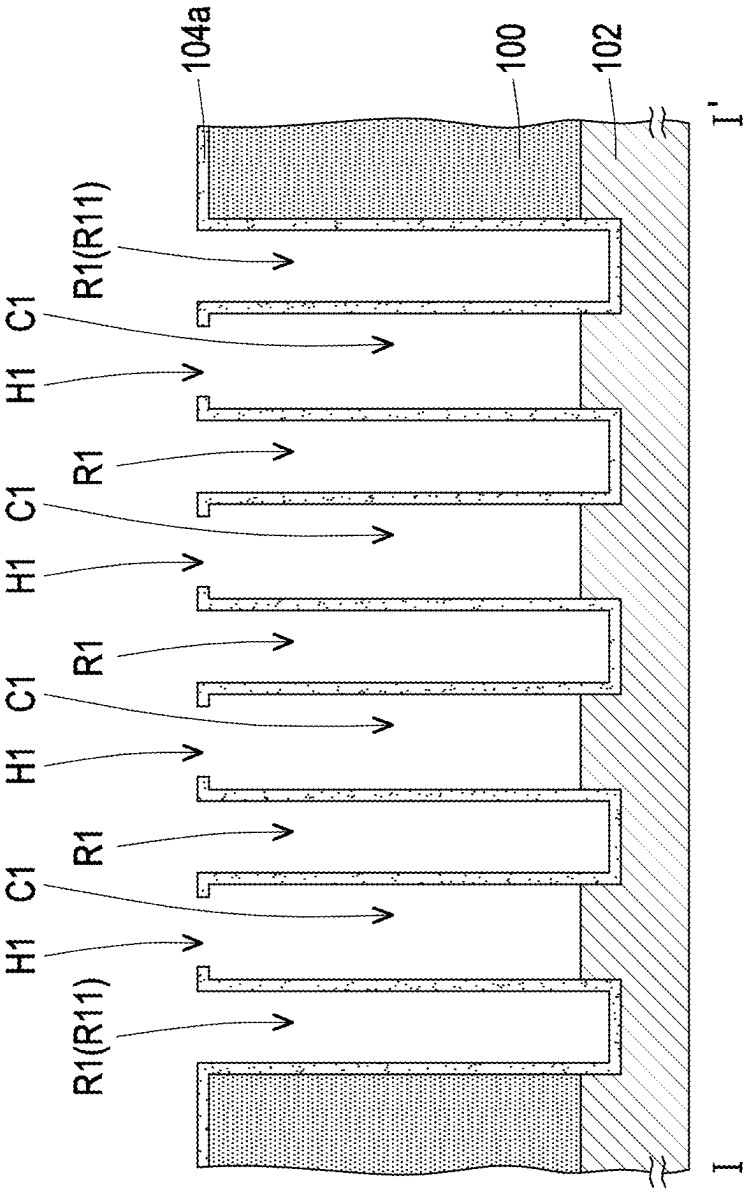


FIG. 1E

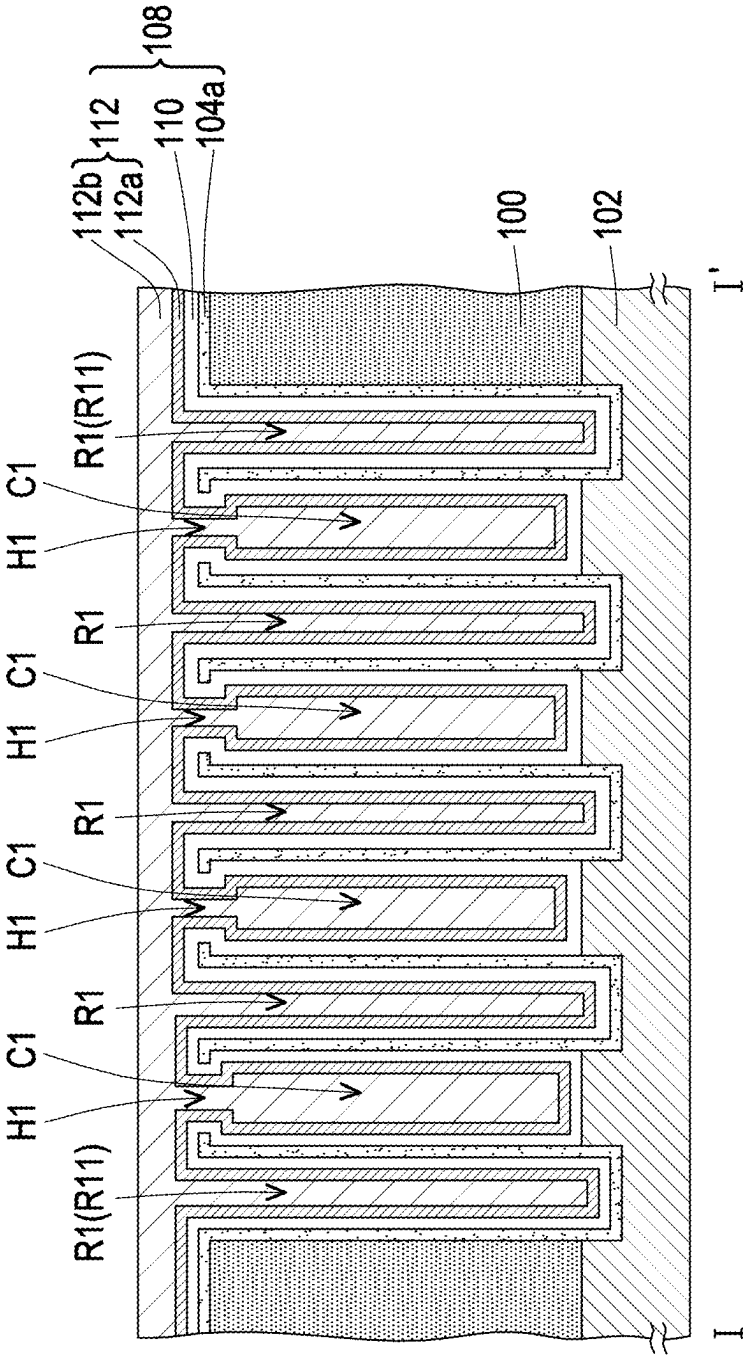

108
112
110
104a
112b
112a
100
102
I'
I
R1(R11)
C1
H1
R1
C1
H1
R1
C1
H1
R1
C1
H1
R1(R11)

FIG. 1F

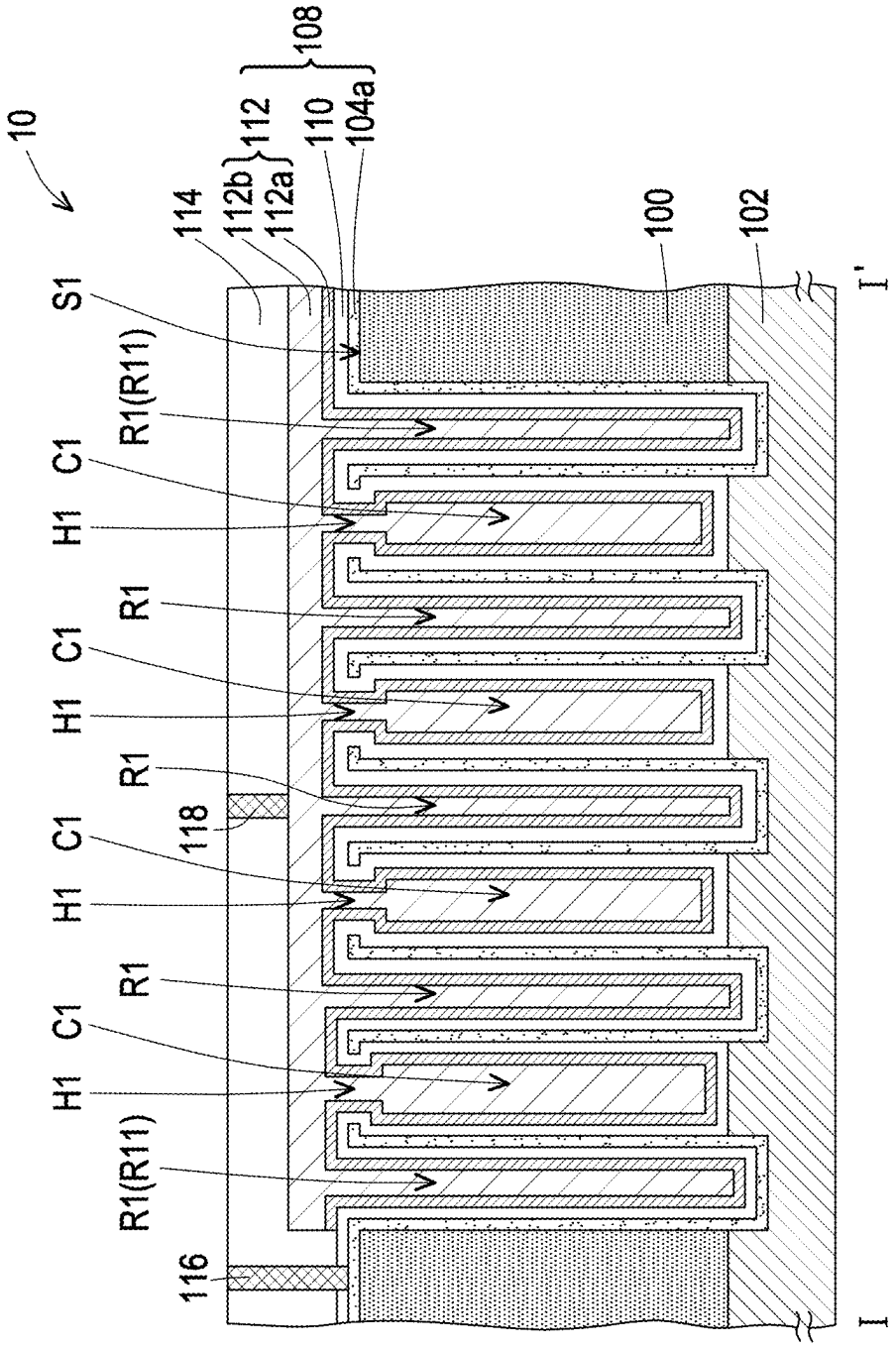

10
108
112
110
104a
112b
112a
114
100
102
I'
S1
R1(R11)
C1
H1
R1
C1
H1
R1
118
C1
H1
R1
C1
H1
R1(R11)
116
I

FIG. 1G

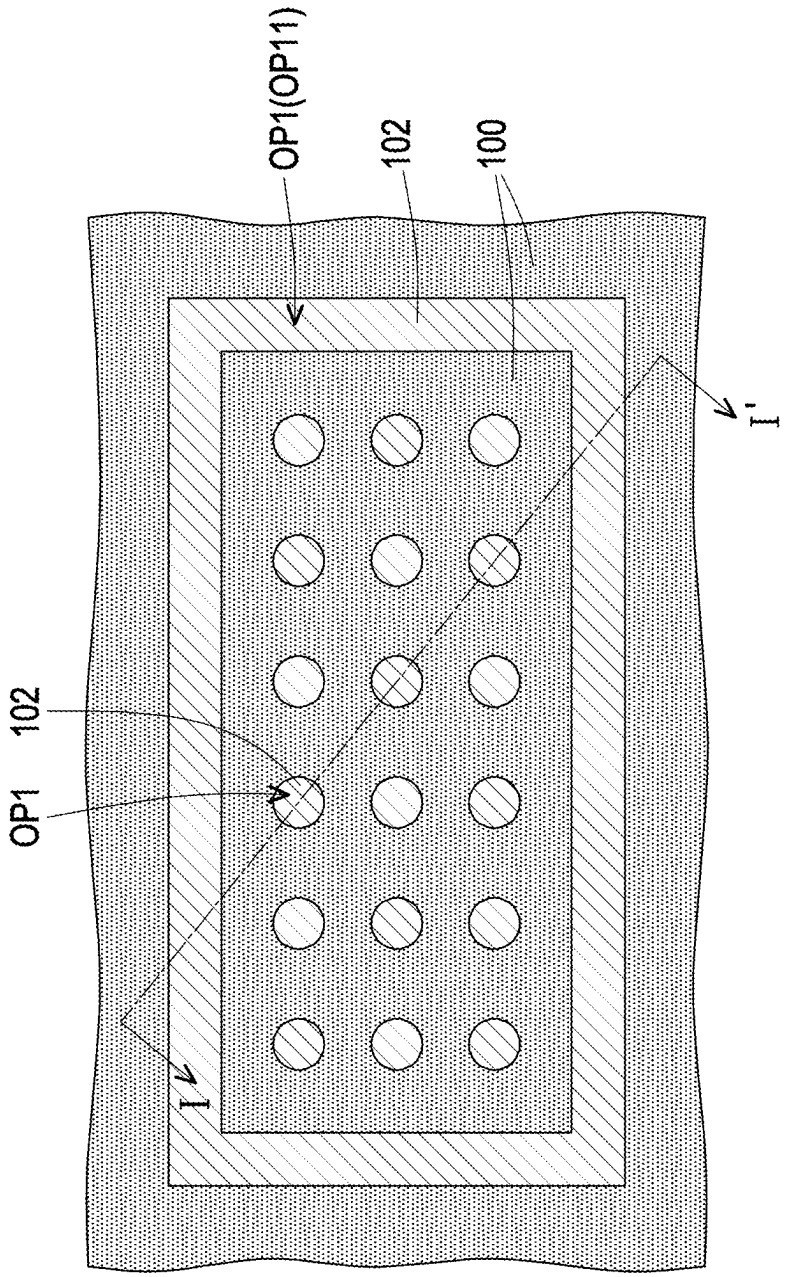


FIG. 2A

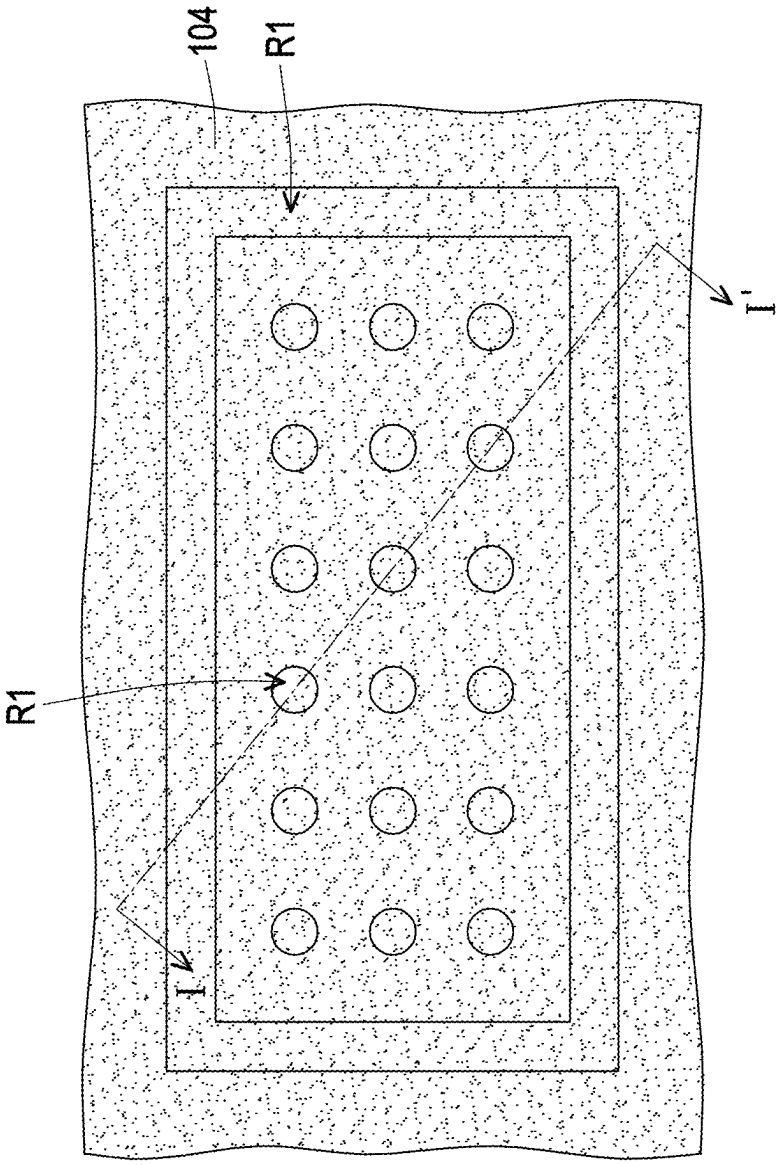


FIG. 2B

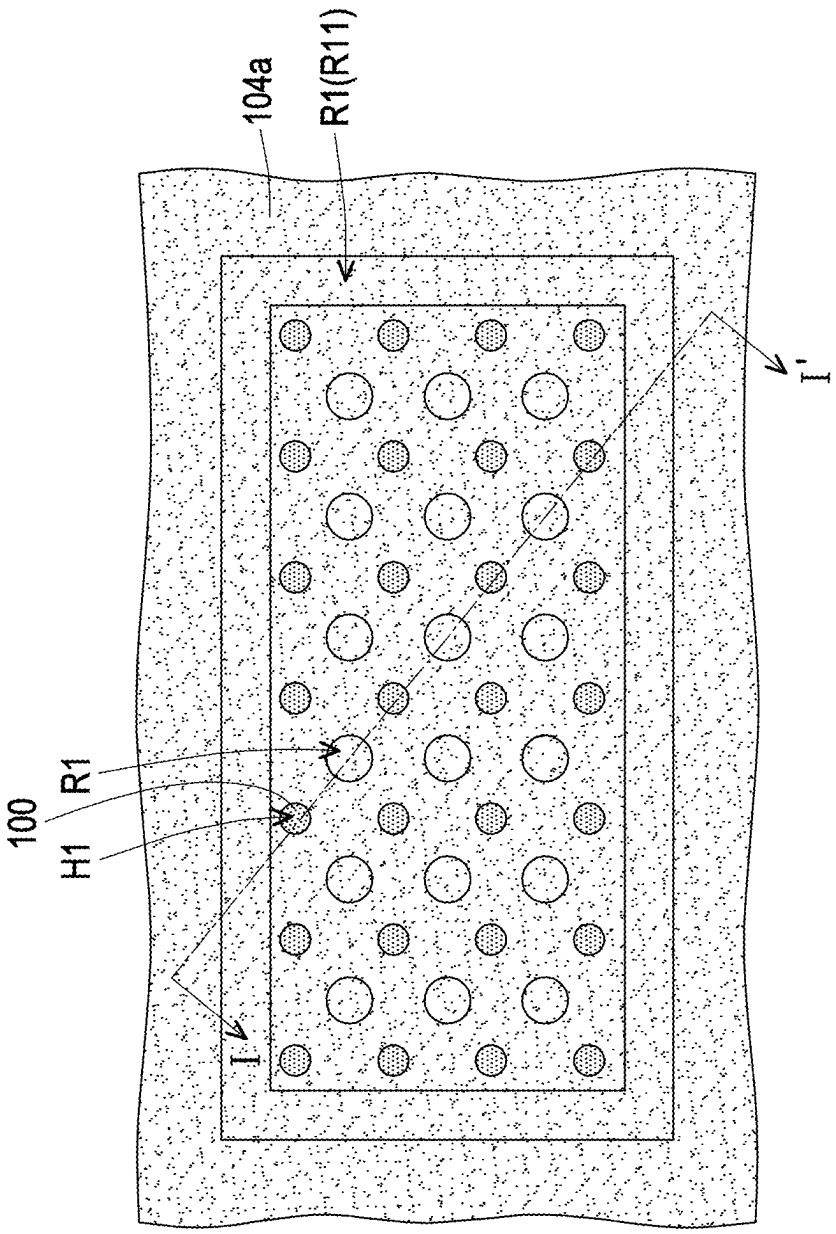


FIG. 2C

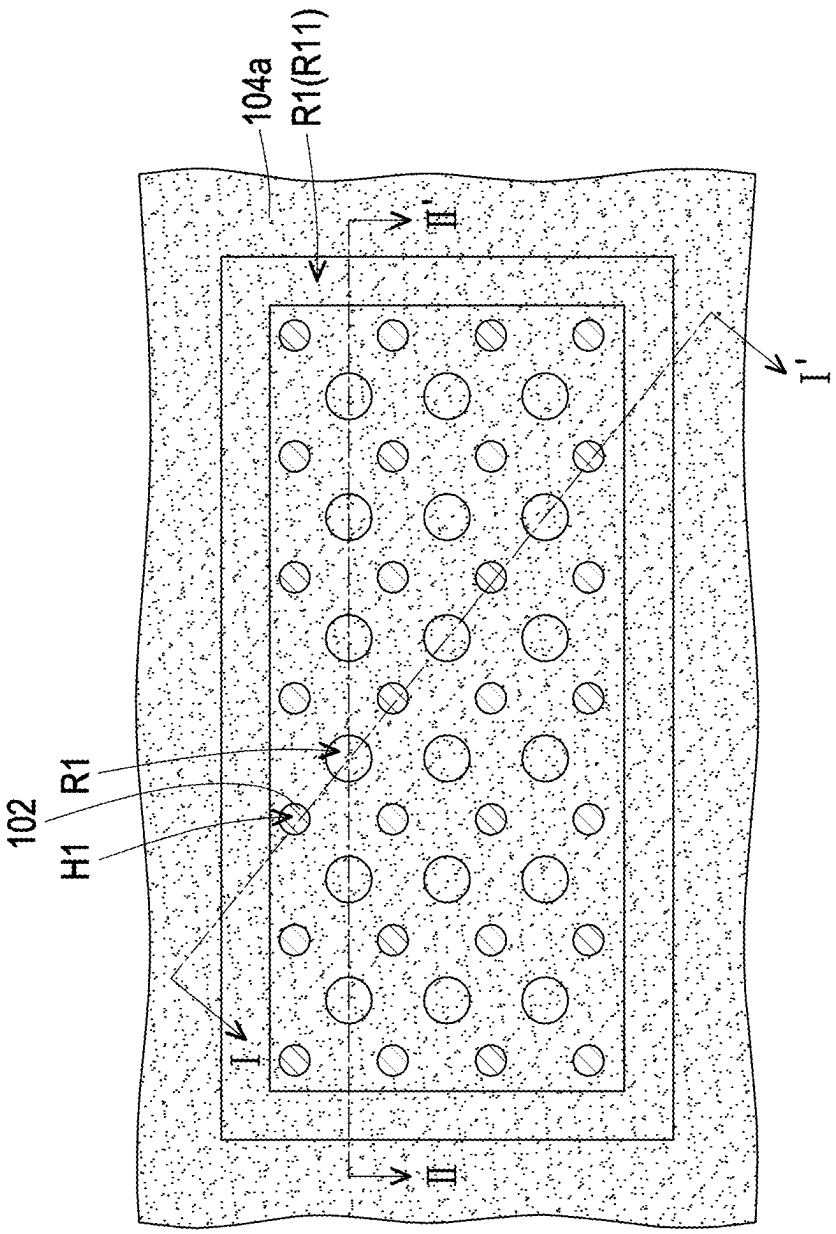


FIG. 2D

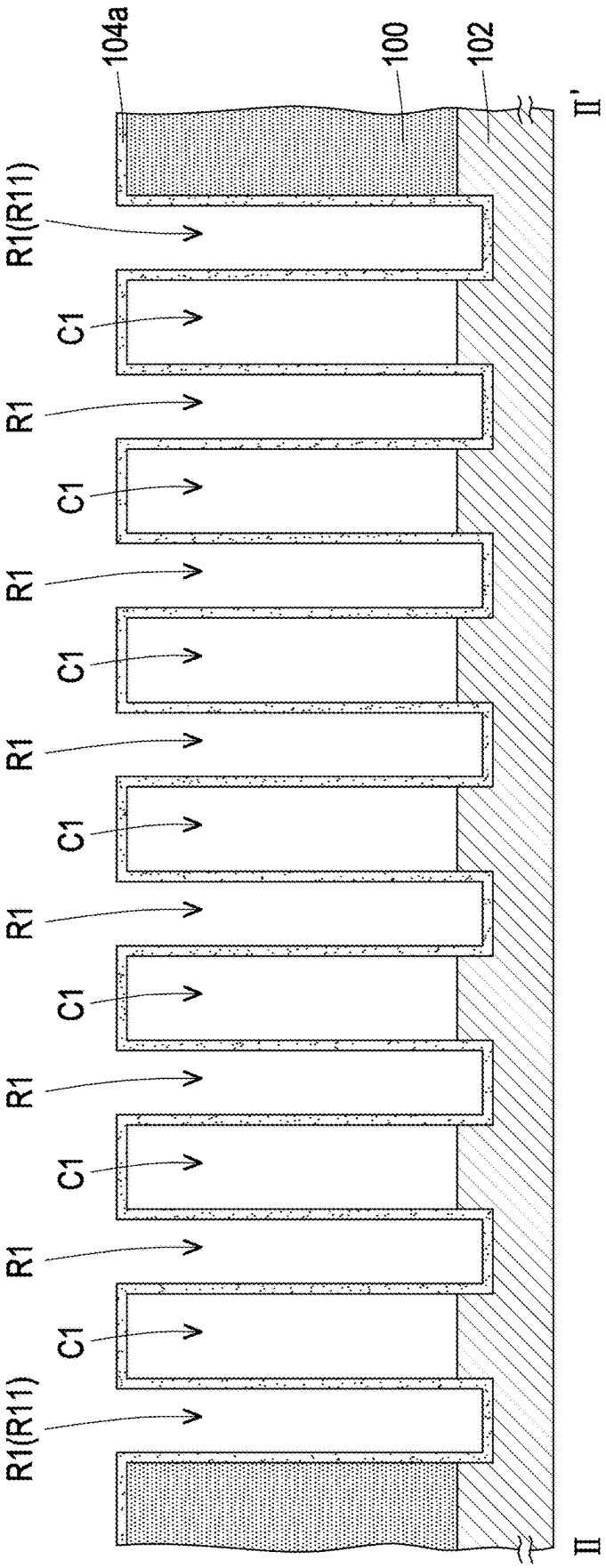

104a
100
102
II'
R1(R11)
C1
R1
C1
R1
C1
R1
C1
R1
C1
R1
C1
R1
C1
R1(R11)
II

FIG. 3A

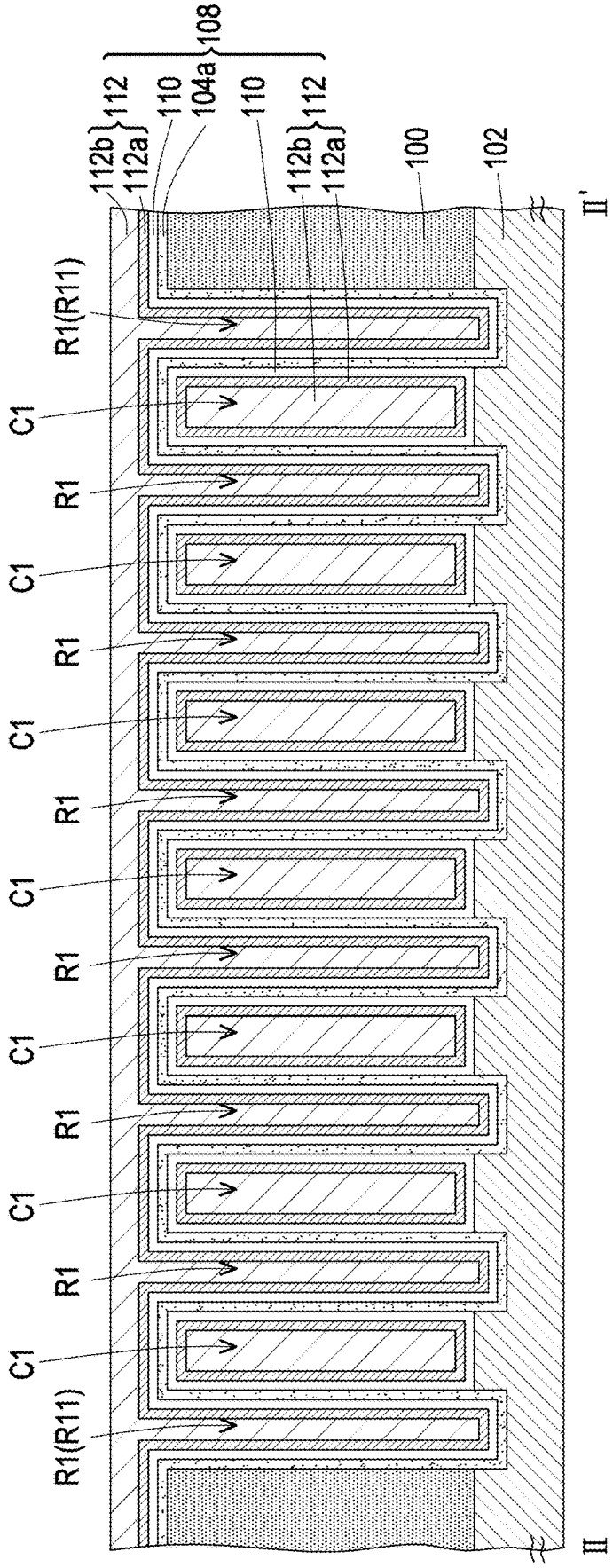

108
112
110
104a
110
112
112b
112a
112b
112a
100
102
II'
R1(R11)
C1
R1
C1
R1
C1
R1
C1
R1
C1
R1
C1
R1
C1
R1(R11)
II

FIG. 3B

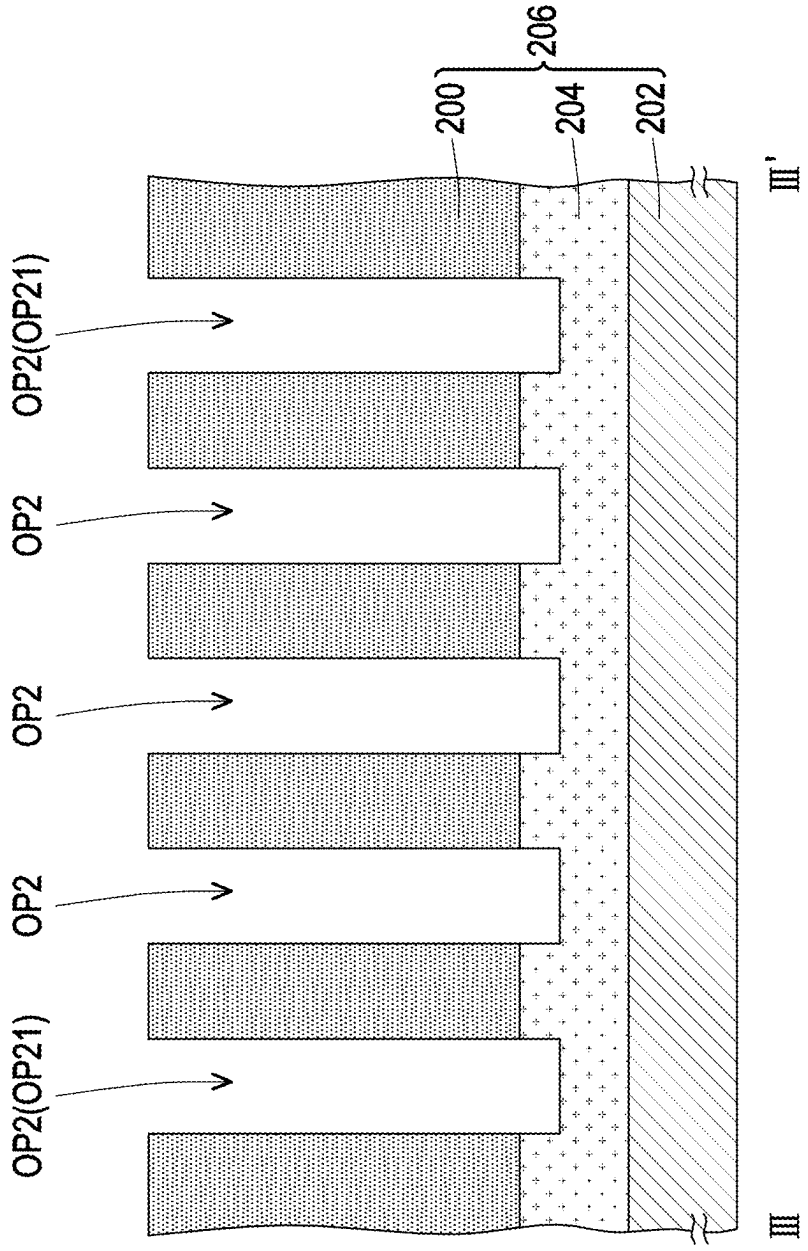


FIG. 4A

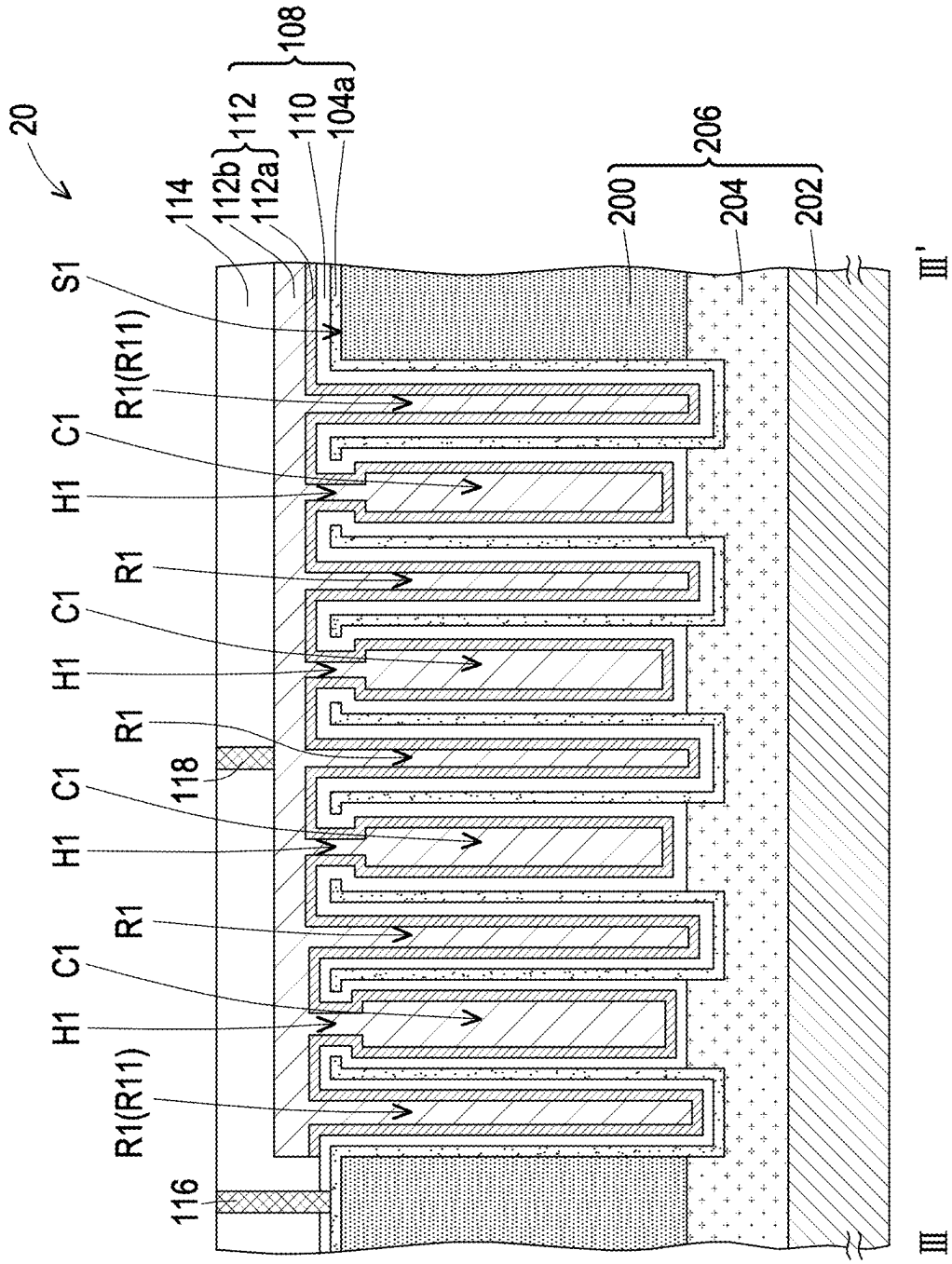

20
108
112
110
104a
112b
112a
114
206
200
204
202
III'
S1
R1(R11)
C1
H1
R1
C1
H1
R1
118
C1
H1
R1
C1
H1
R1(R11)
116
III

FIG. 4B

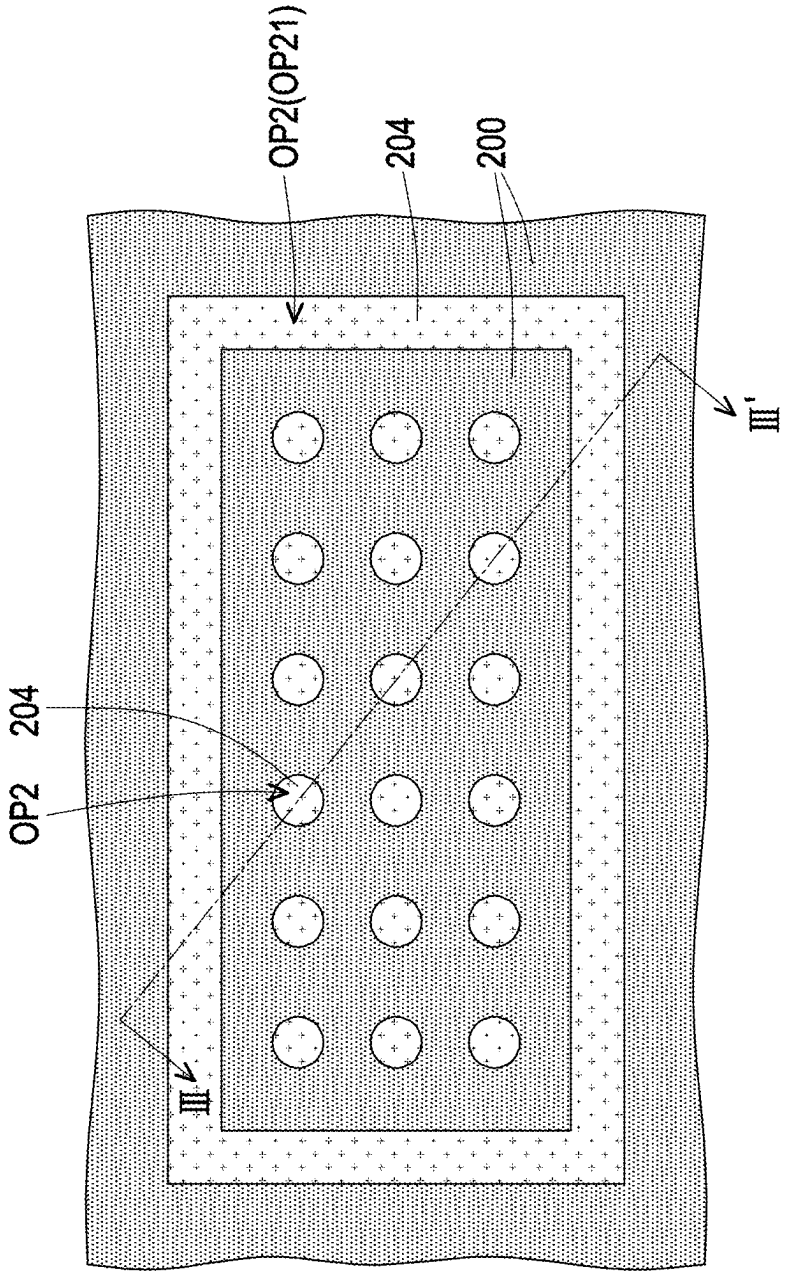


FIG. 5

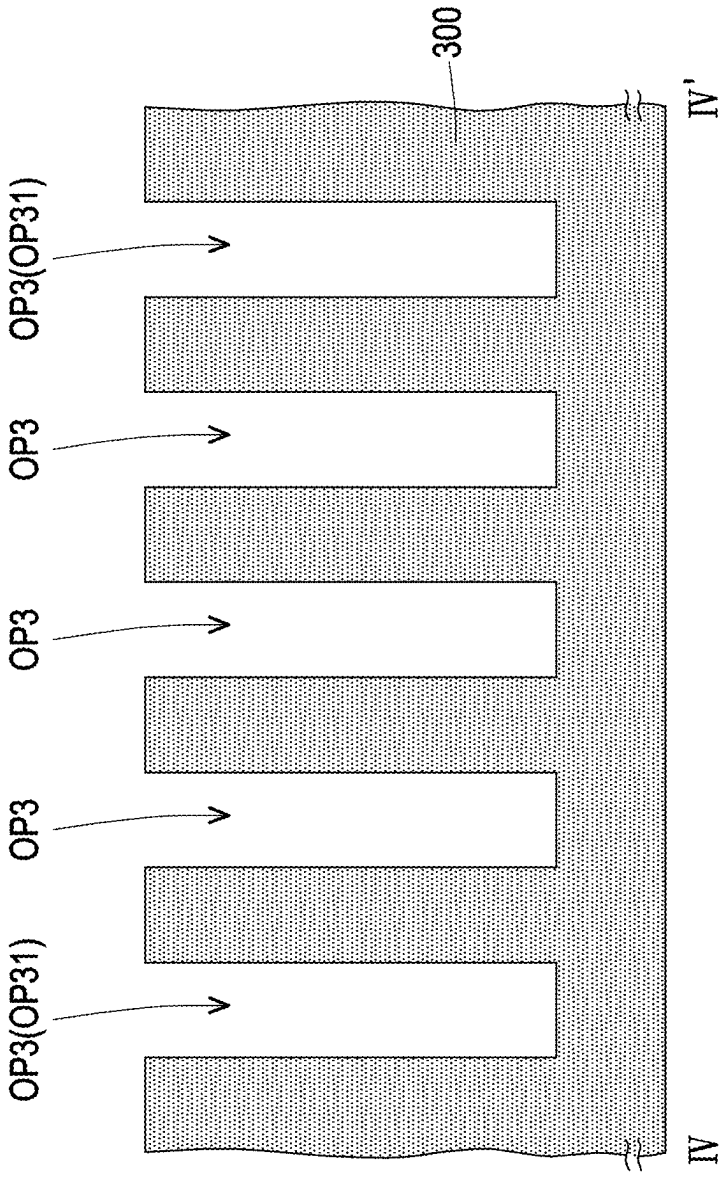


FIG. 6A

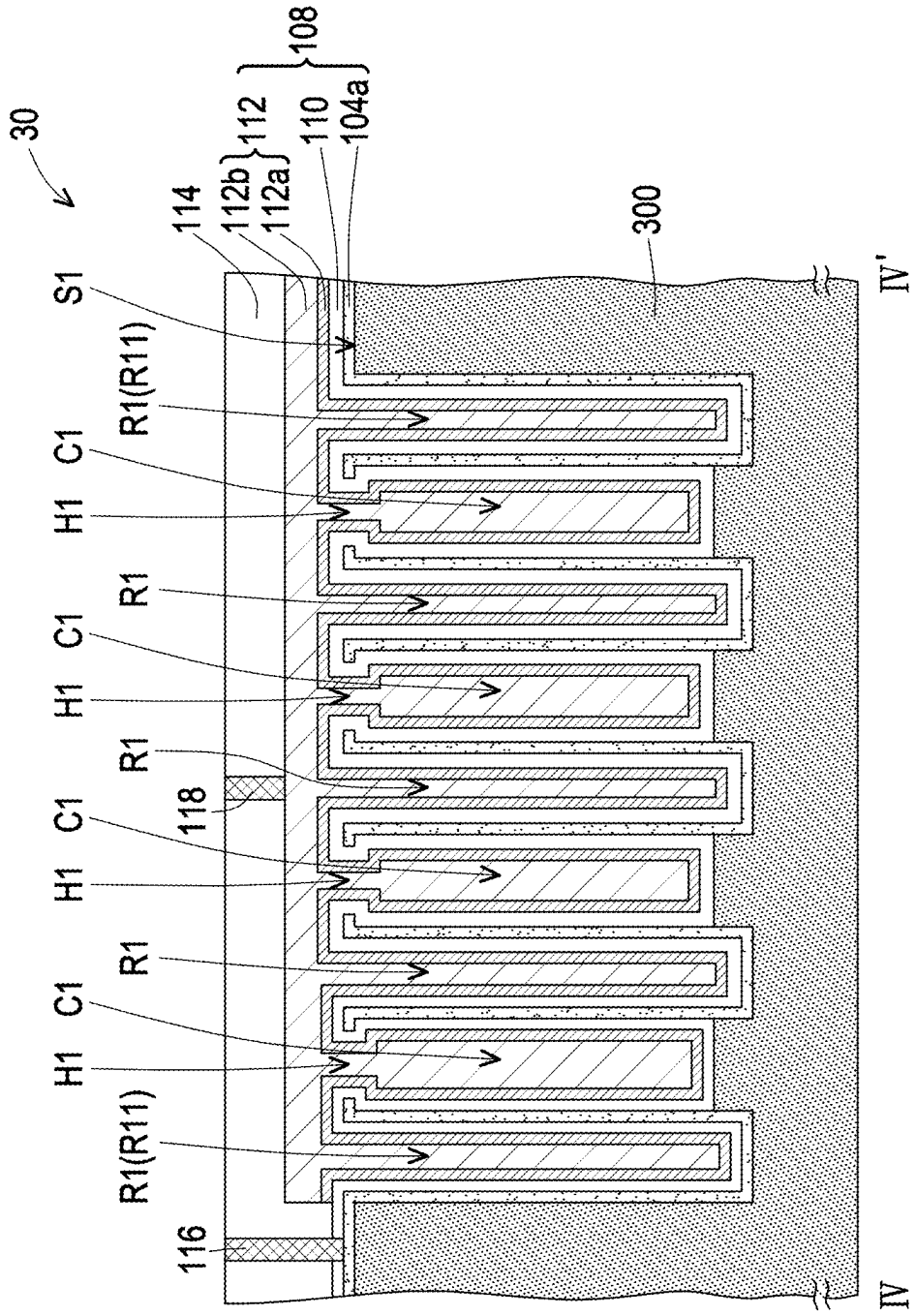

30
108
112
112b
112a
110
104a
114
300
IV'
IV
S1
R1(R11)
C1
H1
R1
C1
H1
R1
118
C1
H1
R1
C1
H1
R1(R11)
116

FIG. 6B

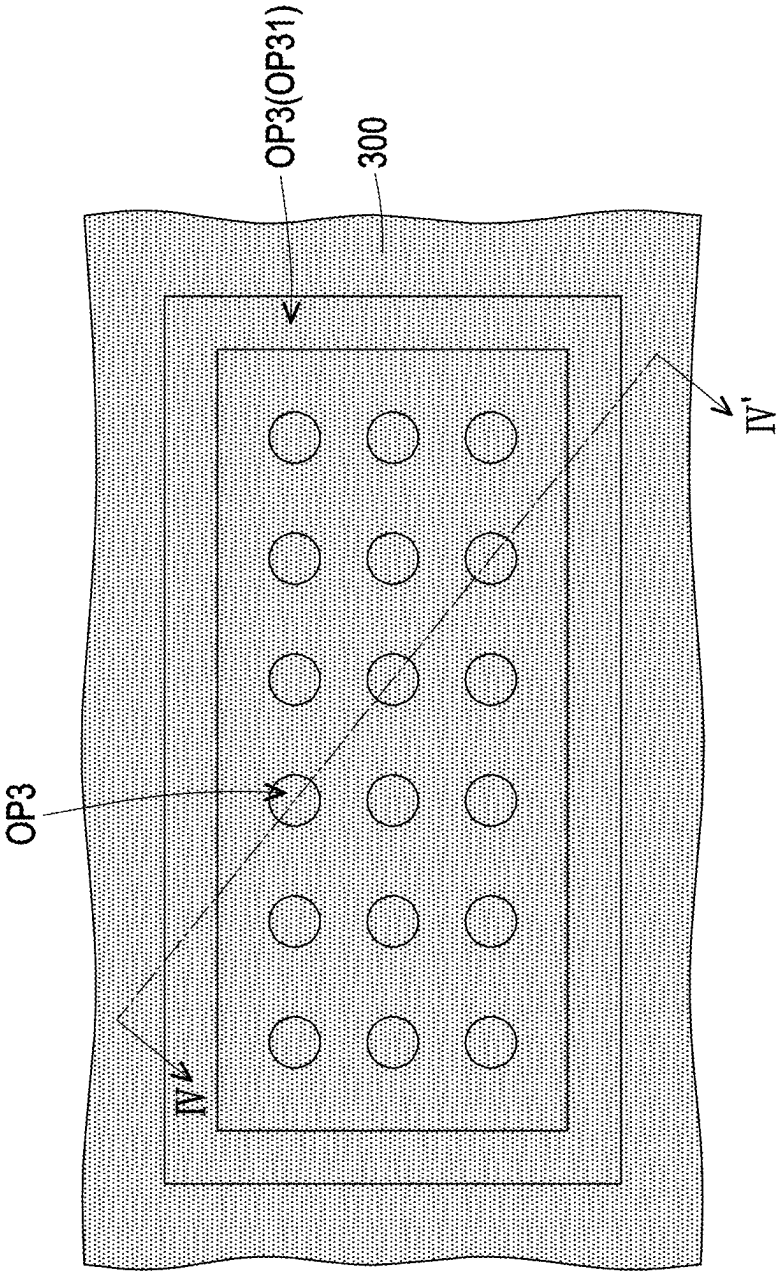


FIG. 7

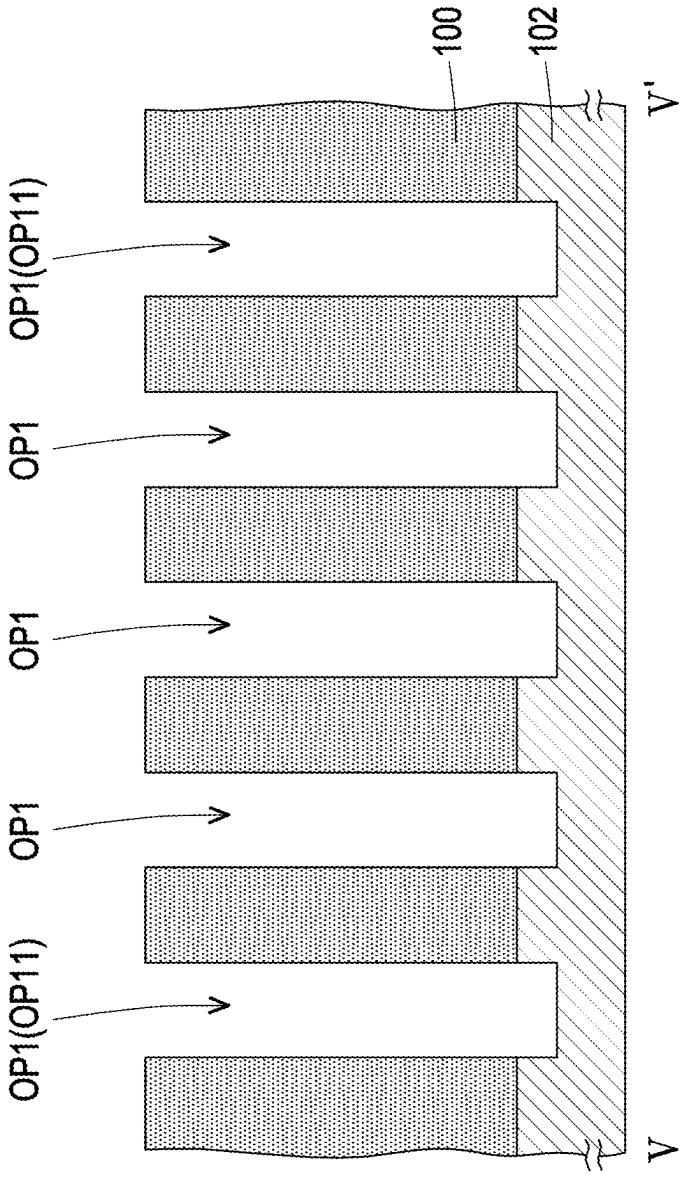


FIG. 8A

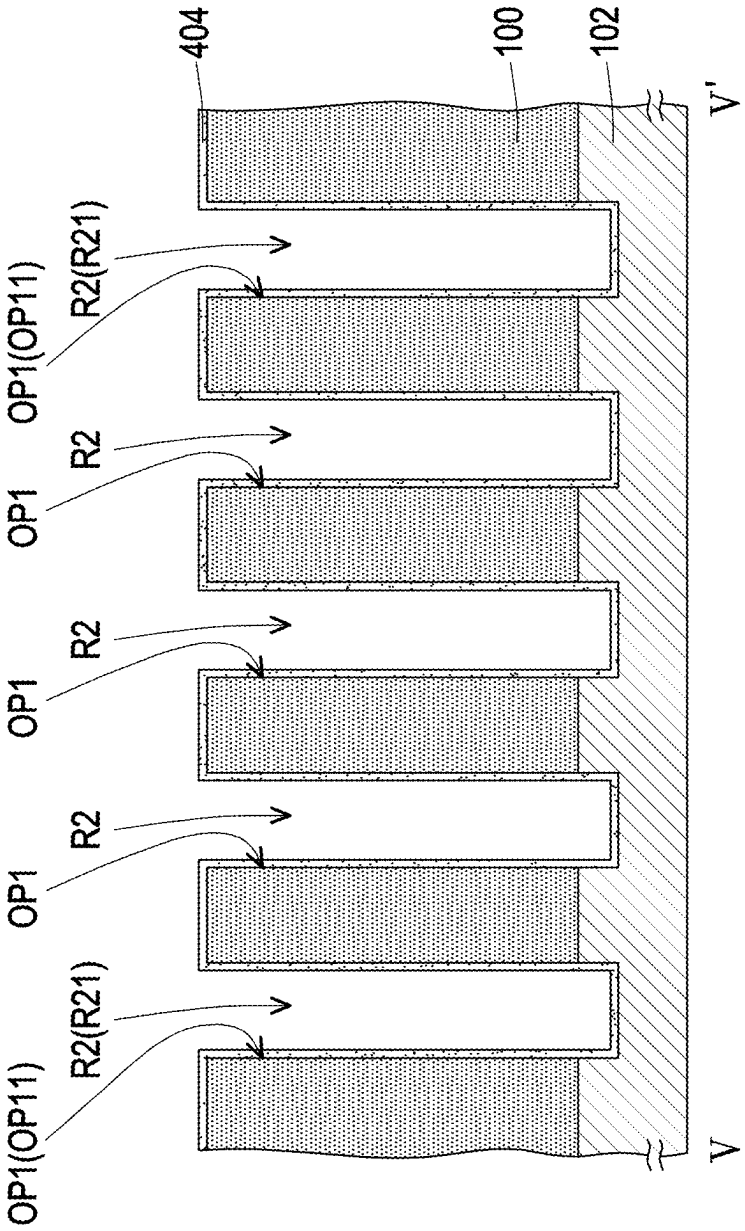

404
100
102
V'
OP1(OP11)
R2(R21)
OP1
R2
OP1
R2
OP1
R2
OP1(OP11)
R2(R21)
V

FIG. 8B

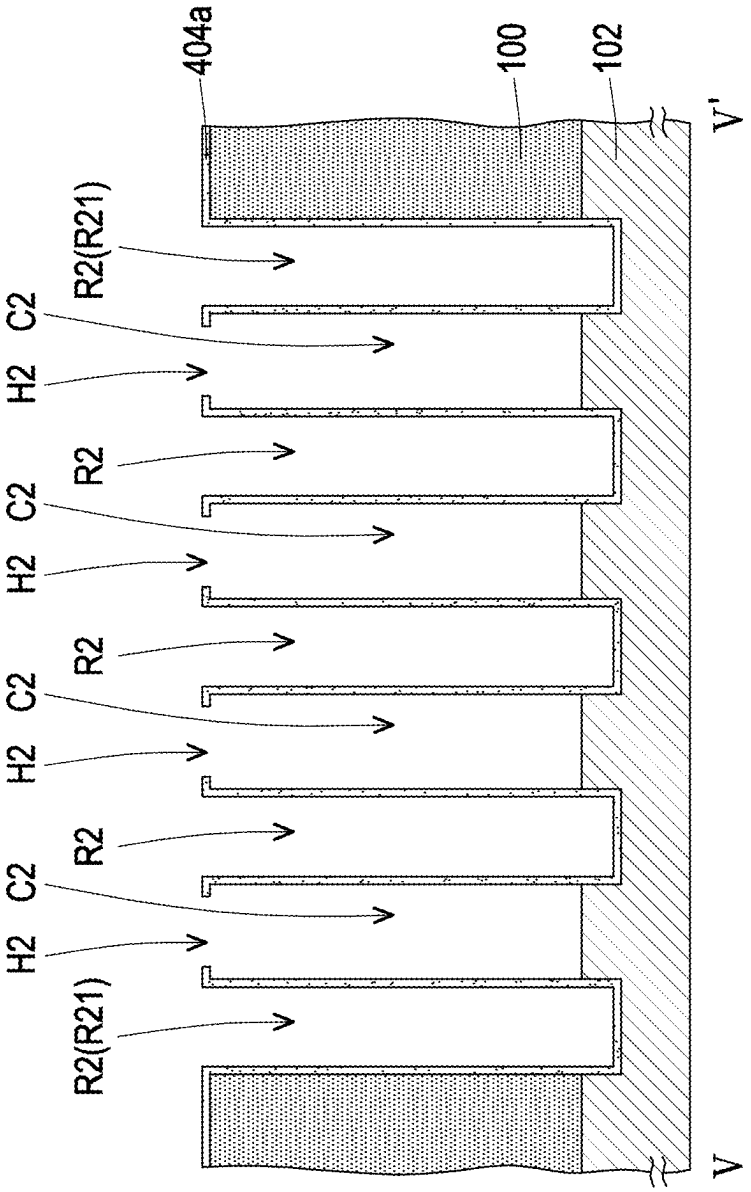


FIG. 8C

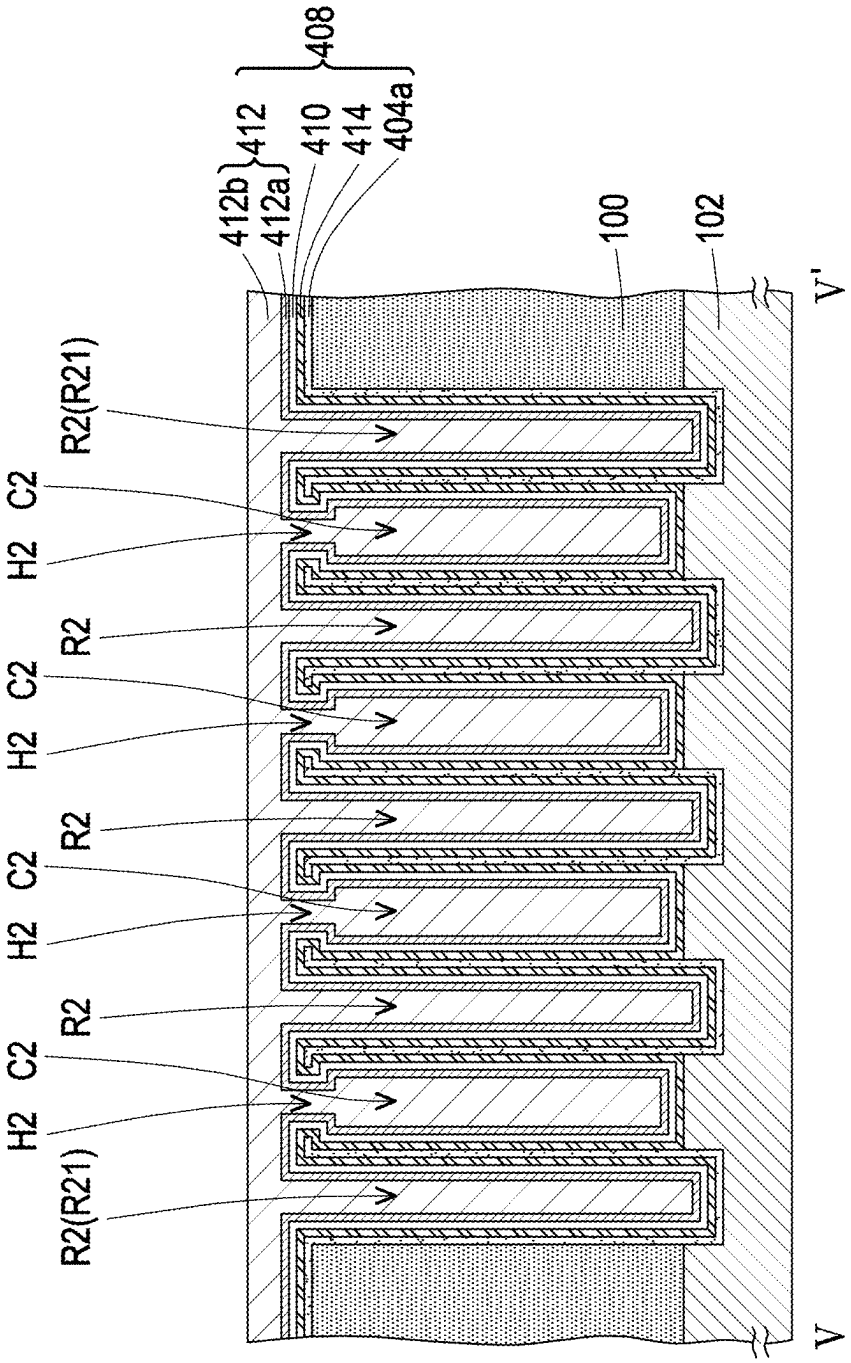

408
412
410
414
404a
412b
412a
100
102
V'
V
R2(R21)
C2
H2
R2
C2
H2
R2
C2
H2
R2
C2
H2
R2(R21)

FIG. 8D

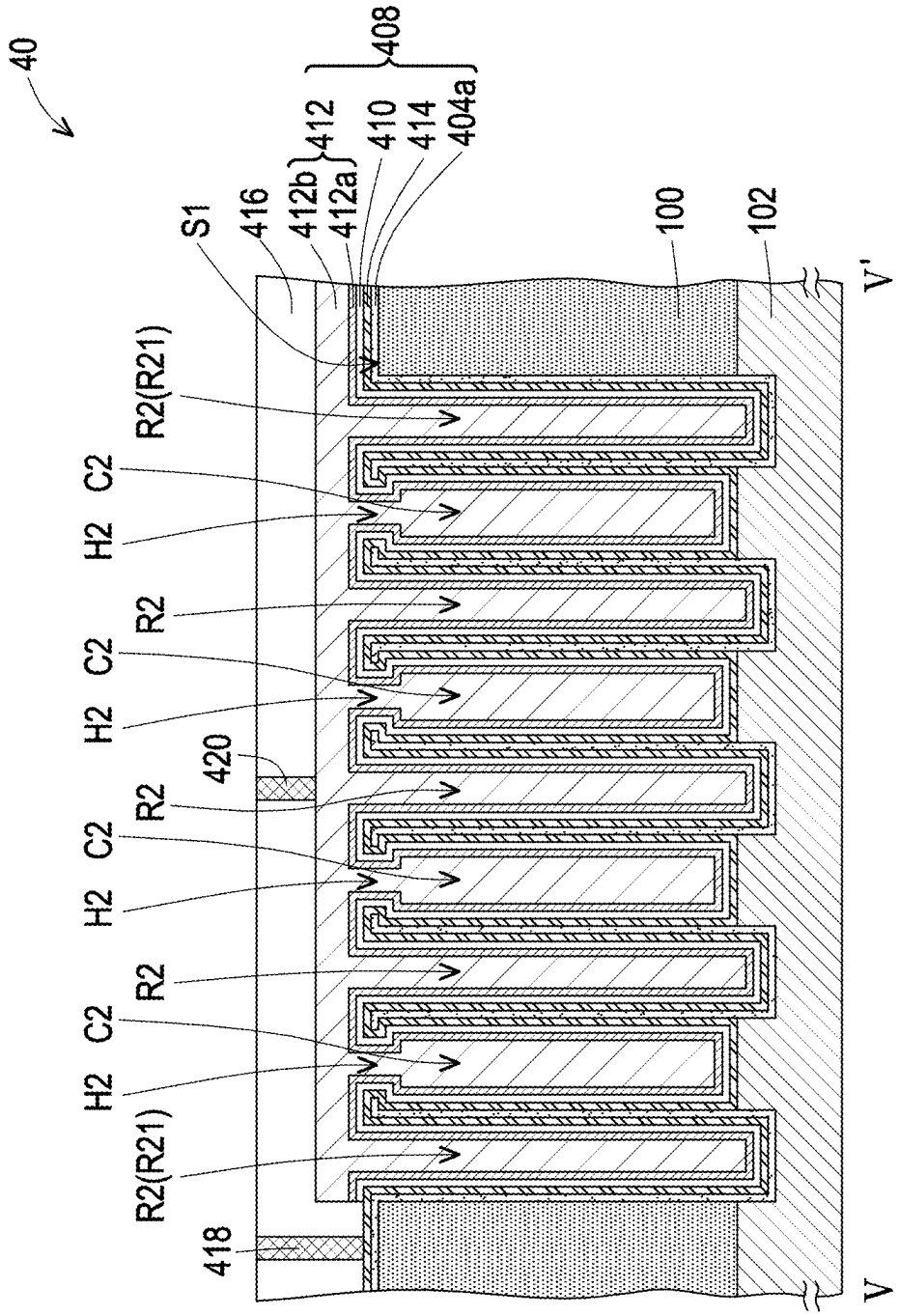

40
408
404a
414
410
412
412a
412b
416
S1
100
102
V'
V
R2(R21)
C2
H2
R2
420
418

FIG. 8E

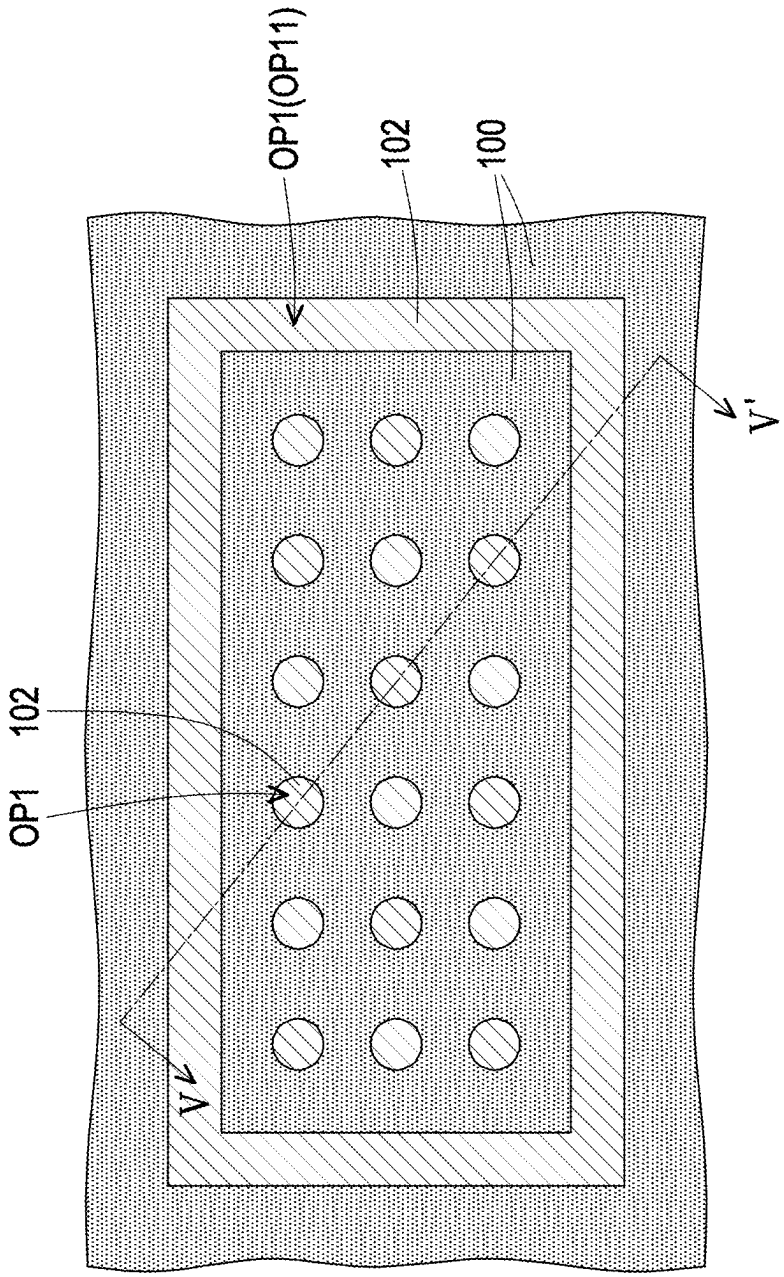


FIG. 9A

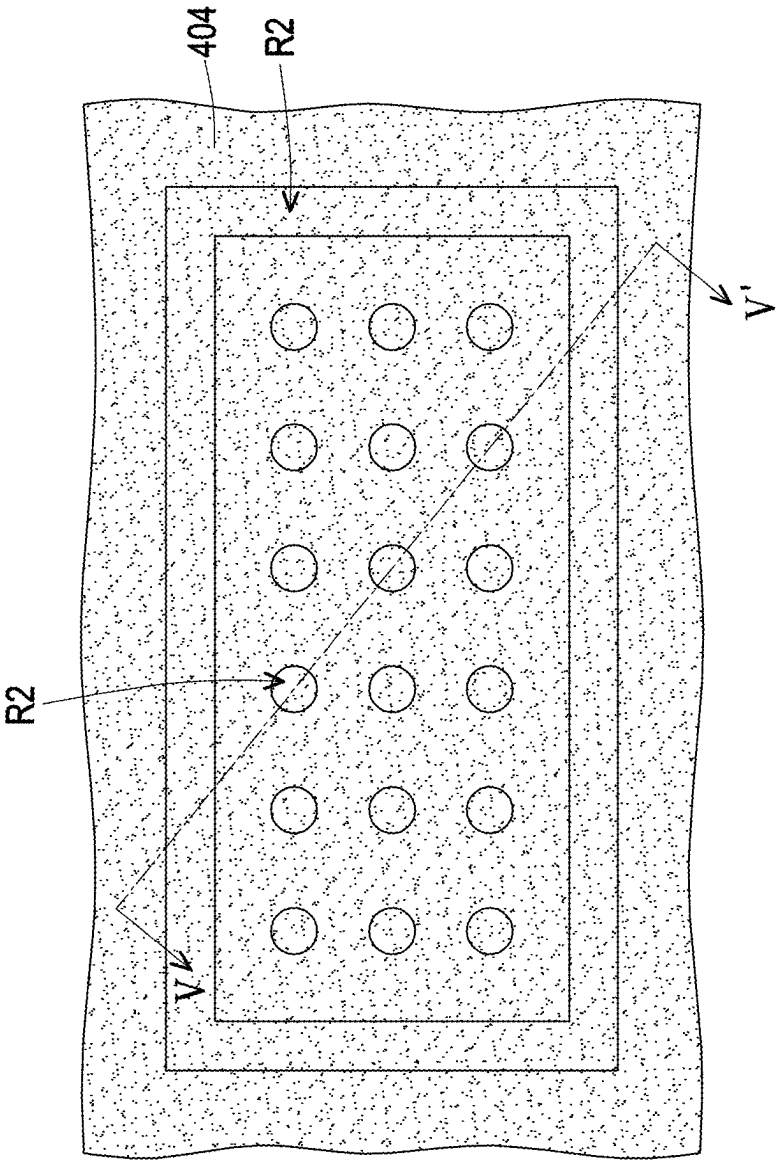


FIG. 9B

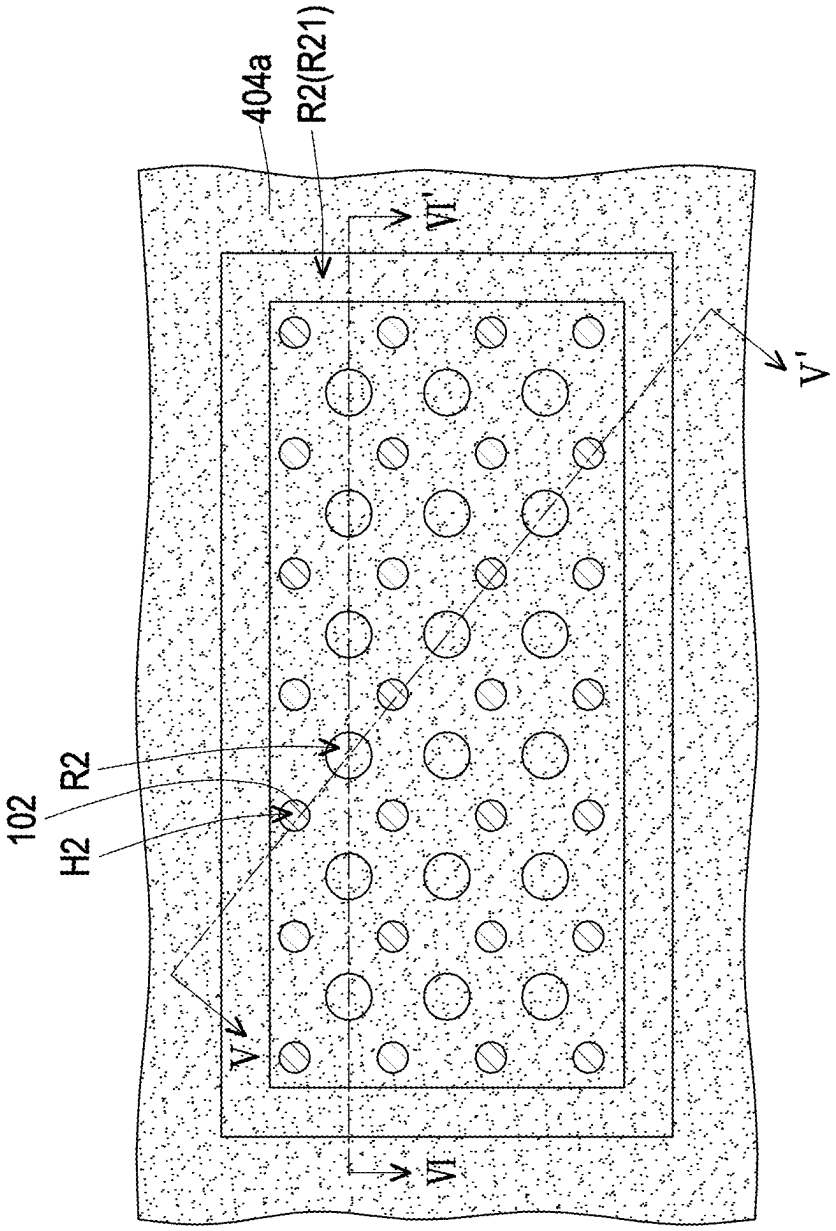


FIG. 9C

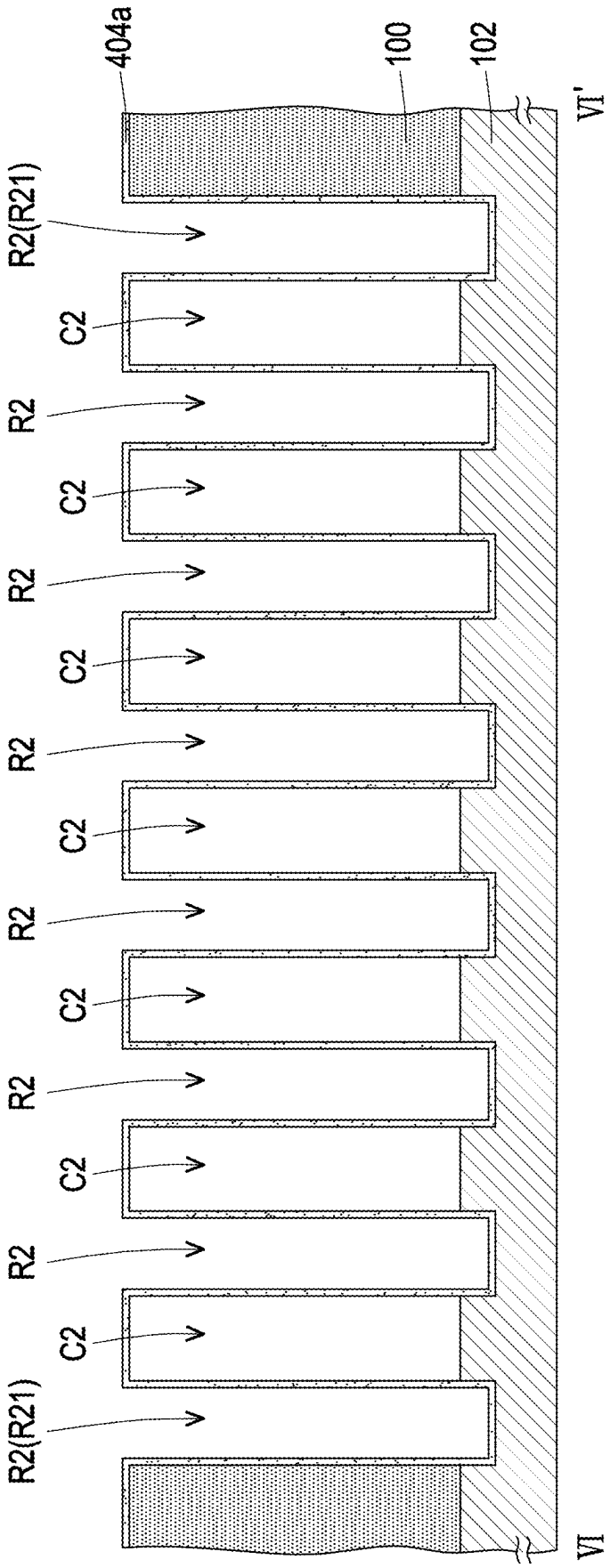

404a
100
102
VI'
R2(R21)
C2
R2
C2
R2
C2
R2
C2
R2
C2
R2
C2
R2
C2
R2
C2
R2(R21)
VI

FIG. 10A

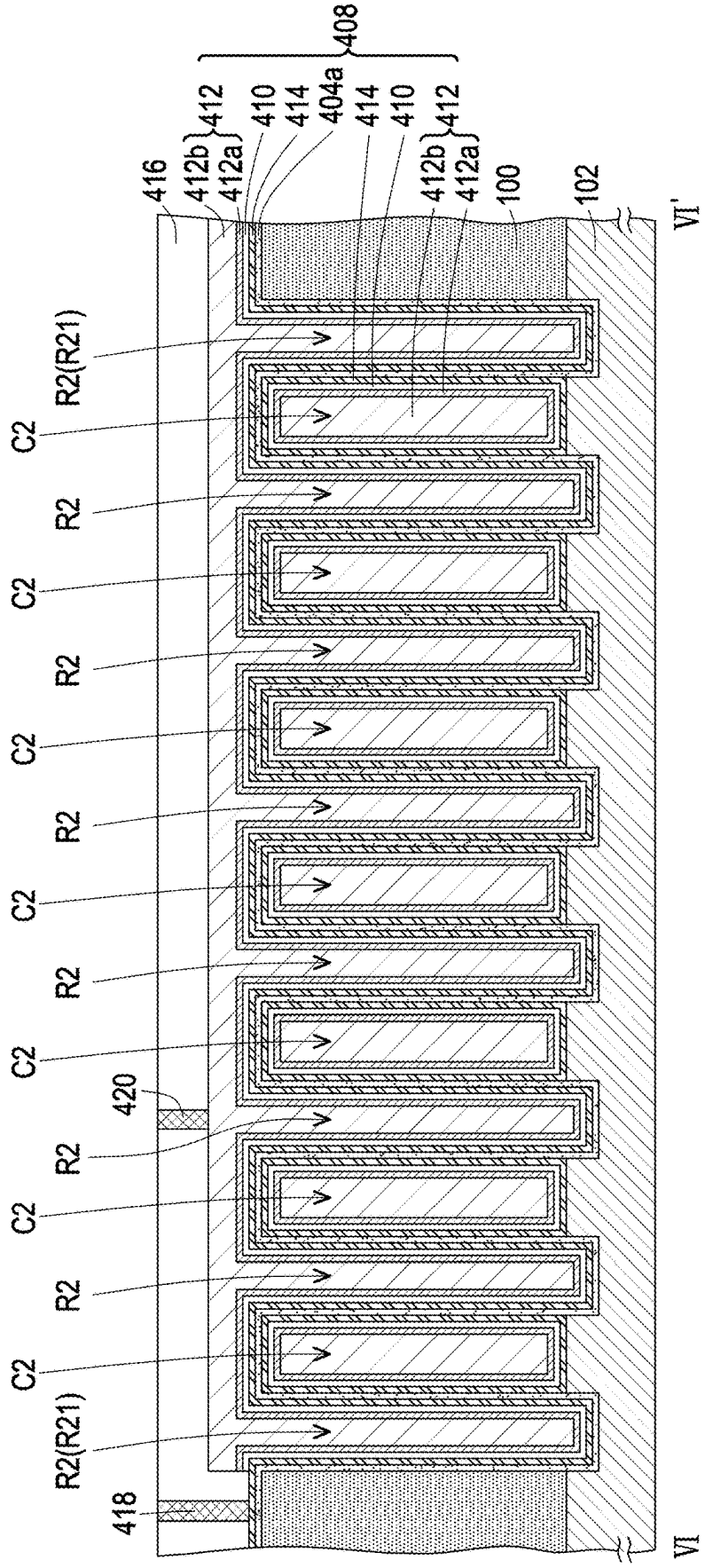

408
412
410
414
404a
414
410
412
416
412b
412a
412b
412a
100
102
VI'
R2(R21)
C2
R2
C2
R2
C2
R2
C2
R2
C2
420
R2
C2
R2
C2
R2(R21)
418
VI

FIG. 10B

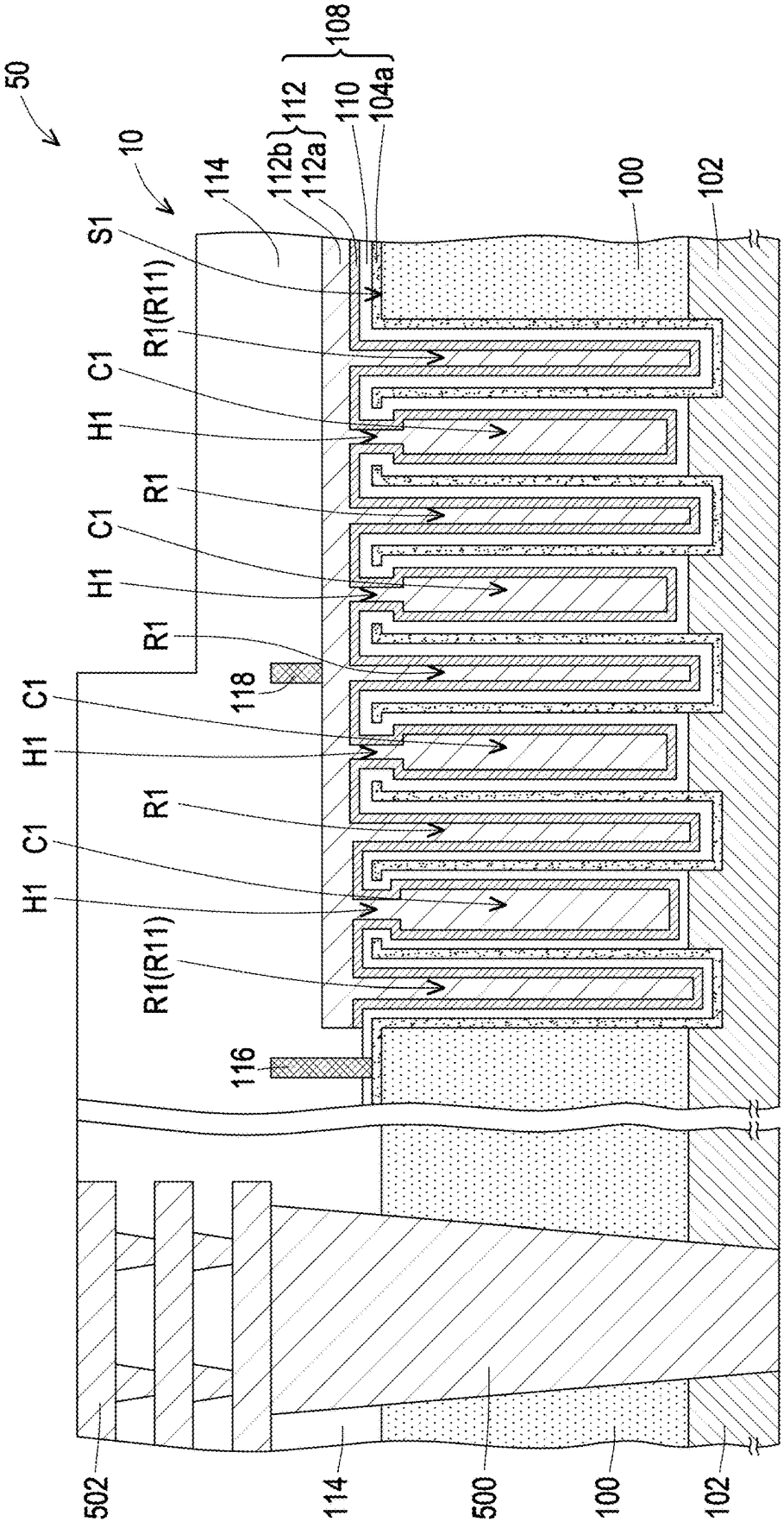

50
10
108
112
112b
112a
110
104a
114
100
102
S1
R1(R11)
C1
H1
R1
C1
H1
R1
118
C1
H1
R1
C1
H1
R1(R11)
116
502
114
500
100
102

FIG. 11

CAPACITOR STRUCTURE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is a divisional application of and claims the priority benefit of U.S. application Ser. No. 17/946,048, filed on Sep. 16, 2022, which claims the priority benefit of Taiwan application serial no. 111127294, filed on Jul. 21, 2022. The entirety of each of the above-mentioned patent applications is hereby incorporated by reference herein and made a part of this specification.

BACKGROUND

Technical Field

[0002] The invention relates to a semiconductor structure and a manufacturing method thereof, and particularly relates to a capacitor structure and a manufacturing method thereof.

Description of Related Art

[0003] In the current semiconductor industry, the capacitor is a very important basic device. For example, the basic design of a common capacitor structure is to insert an insulating material between electrode plates, so that two adjacent electrode plates and the insulating material therebetween form a capacitor unit. However, how to effectively increase the capacitance value of the capacitor is the goal of continuous efforts.

SUMMARY

[0004] The invention provides a capacitor structure and a manufacturing method thereof, which can effectively increase the capacitance value of the capacitor.

[0005] The invention provides a capacitor structure, which includes a silicon material layer, a support frame layer, and a capacitor. The support frame layer is disposed in the silicon material layer. The support frame layer has recesses. There is a cavity between two adjacent recesses. The support frame layer is located between the cavity and the recess. The support frame layer has a through hole directly above the cavity. The capacitor is disposed in the silicon material layer. The capacitor includes a first insulating layer and a first electrode layer. The first insulating layer is disposed on the support frame layer. The first electrode layer is disposed on the first insulating layer and fills the recess and the cavity.

[0006] According to an embodiment of the invention, in the capacitor structure, the material of the silicon material layer is, for example, epitaxial silicon, polysilicon, or single crystal silicon.

[0007] According to an embodiment of the invention, in the capacitor structure, a portion of the support frame layer may be located outside the silicon material layer.

[0008] According to an embodiment of the invention, in the capacitor structure, a portion of the capacitor may be located outside the silicon material layer.

[0009] According to an embodiment of the invention, in the capacitor structure, the recesses may include a ring-shaped recess, and the ring-shaped recess may surround the rest of the recesses.

[0010] According to an embodiment of the invention, in the capacitor structure, the material of the support frame layer may be a conductive material, and the capacitor may further include the support frame layer.

[0011] According to an embodiment of the invention, in the capacitor structure, the material of the support frame layer may be a dielectric material, and the capacitor may further include a second electrode layer. The second electrode layer is disposed between the first insulating layer and the support frame layer.

[0012] According to an embodiment of the invention, in the capacitor structure, the first electrode layer may include a first conductive layer and a second conductive layer. The first conductive layer is disposed on the first insulating layer. The second conductive layer is disposed on the first conductive layer and fills the recess and the cavity.

[0013] According to an embodiment of the invention, the capacitor structure may further include a substrate. The silicon material layer is disposed on the substrate. The silicon material layer and the substrate may have the same conductivity type. The dopant concentration of the silicon material layer may be less than the dopant concentration of the substrate.

[0014] According to an embodiment of the invention, the capacitor structure may further include a substrate and a second insulating layer. The silicon material layer is disposed on the substrate. The second insulating layer is disposed between the silicon material layer and the substrate.

[0015] The invention provides a manufacturing method of a capacitor structure, which includes the following steps. A silicon material layer is provided. A support frame layer is formed in the silicon material layer. The support frame layer has recesses. There is a cavity between two adjacent recesses. The support frame layer is located between the cavity and the recess. The support frame layer has a through hole directly above the cavity. A capacitor is formed in the silicon material layer. The capacitor includes a first insulating layer and a first electrode layer. The first insulating layer is disposed on the support frame layer. The first electrode layer is disposed on the first insulating layer and fills the recess and the cavity.

[0016] According to an embodiment of the invention, in the manufacturing method of the capacitor structure, the method of forming the support frame layer may include the following steps. Openings are formed in the silicon material layer. A support frame material layer is conformally formed on the silicon material layer and in the openings. The support frame material layer is patterned to form the support frame layer and the through hole. The through holes may expose the silicon material layer.

[0017] According to an embodiment of the invention, in the manufacturing method of the capacitor structure, the openings may include a ring-shaped opening, and the ring-shaped opening may surround the rest of the openings.

[0018] According to an embodiment of the invention, in the manufacturing method of the capacitor structure, the method of forming the cavity may include removing a portion of the silicon material layer exposed by the through hole. The method of removing the portion of the silicon material layer exposed by the through hole is, for example, a wet etching method.

[0019] According to an embodiment of the invention, the manufacturing method of the capacitor structure may further include the following steps. A substrate is provided. The silicon material layer may be formed on the substrate. The silicon material layer and the substrate may have the same

conductivity type. The dopant concentration of the silicon material layer may be less than the dopant concentration of the substrate.

[0020] According to an embodiment of the invention, in the manufacturing method of the capacitor structure, the portion of the silicon material layer exposed by the through hole may be removed by using the substrate as a stop layer.

[0021] According to an embodiment of the invention, the manufacturing method of the capacitor structure may further include the following steps. A substrate is provided. A second insulating layer is provided. The second insulating layer is located between the silicon material layer and the substrate.

[0022] According to an embodiment of the invention, in the manufacturing method of the capacitor structure, the portion of the silicon material layer exposed by the through hole may be removed by using the second insulating layer as a stop layer.

[0023] According to an embodiment of the invention, in the manufacturing method of the capacitor structure, the material of the support frame layer may be a conductive material, and the capacitor may further include the support frame layer.

[0024] According to an embodiment of the invention, in the manufacturing method of the capacitor structure, the material of the support frame layer may be a dielectric material, and the capacitor may further include a second electrode layer. The second electrode layer is disposed between the first insulating layer and the support frame layer.

[0025] Based on the above description, in the capacitor structure and the manufacturing method thereof according to the invention, the support frame layer has the recesses, there is the cavity between two adjacent recesses, the support frame layer is located between the cavity and the recess, the support frame layer has the through hole directly above the cavity, the first insulating layer is disposed on the support frame layer, and the first electrode layer is disposed on the first insulating layer and fills the recess and the cavity. Therefore, the first electrode layer can have a larger area, thereby effectively increasing the capacitance value of the capacitor.

[0026] In order to make the aforementioned and other objects, features and advantages of the invention comprehensible, several exemplary embodiments accompanied with drawings are described in detail below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0028] FIG. **1**A to FIG. **1**G are cross-sectional views illustrating a manufacturing process of a capacitor structure according to some embodiments of the invention.

[0029] FIG. **2**A to FIG. **2**D are top views illustrating some stages of a manufacturing process of a capacitor structure according to some embodiments of the invention.

[0030] FIG. **3**A and FIG. **3**B are cross-sectional views illustrating some stages of a manufacturing process of a capacitor structure according to some embodiments of the invention.

[0031] FIG. **4**A to FIG. **4**B are cross-sectional views illustrating a manufacturing process of a capacitor structure according to other embodiments of the invention.

[0032] FIG. **5** is a top view illustrating one stage of a manufacturing process of a capacitor structure according to other embodiments of the invention.

[0033] FIG. **6**A to FIG. **6**B are cross-sectional views illustrating a manufacturing process of a capacitor structure according to other embodiments of the invention.

[0034] FIG. **7** is a top view illustrating one stage of a manufacturing process of a capacitor structure according to other embodiments of the invention.

[0035] FIG. **8**A to FIG. **8**E are cross-sectional views illustrating a manufacturing process of a capacitor structure according to other embodiments of the invention.

[0036] FIG. **9**A to FIG. **9**C are top views illustrating some stages of a manufacturing process of a capacitor structure according to other embodiments of the invention.

[0037] FIG. **10**A and FIG. **10**B are cross-sectional views illustrating some stages of a manufacturing process of a capacitor structure according to other embodiments of the invention.

[0038] FIG. **11** is a cross-sectional view illustrating a semiconductor structure according to some embodiments of the invention.

DESCRIPTION OF THE EMBODIMENTS

[0039] The embodiments are described in detail below with reference to the accompanying drawings, but the embodiments are not intended to limit the scope of the invention. For the sake of easy understanding, the same components in the following description will be denoted by the same reference symbols. In addition, the drawings are for illustrative purposes only and are not drawn to the original dimensions. Furthermore, the features in the top view and the features in the cross-sectional view are not drawn to the same scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0040] FIG. **1**A to FIG. **1**G are cross-sectional views illustrating a manufacturing process of a capacitor structure according to some embodiments of the invention. FIG. **2**A to FIG. **2**D are top views illustrating some stages of a manufacturing process of a capacitor structure according to some embodiments of the invention. FIG. **1**A to FIG. **1**G are cross-sectional views taken along section line I-I' in FIG. **2**A to FIG. **2**D. FIG. **3**A and FIG. **3**B are cross-sectional views illustrating some stages of a manufacturing process of a capacitor structure according to some embodiments of the invention. FIG. **3**A to FIG. **3**B are cross-sectional views taken along section line II-II' in FIG. **2**D. In the top view of the present embodiment, some components in the cross-sectional view are omitted to clearly illustrate the configuration relationship between the components in the top view.

[0041] Referring to FIG. **1**A and FIG. **2**A, a silicon material layer **100** is provided. In some embodiments, the material of the silicon material layer **100** is, for example, epitaxial silicon or polysilicon, but the invention is not limited thereto. In some embodiments, a substrate **102** may be further provided. The substrate **102** may be a semiconductor substrate such as a single crystal silicon substrate. Furthermore, the silicon material layer **100** may be formed on the substrate **102**. The silicon material layer **100** and the substrate **102** may have the same conductivity type. In some

embodiments, the silicon material layer **100** and the substrate **102** may have a P-type conductivity type. In other embodiments, the silicon material layer **100** and the substrate **102** may have an N-type conductivity type. The dopant concentration of the silicon material layer **100** may be less than the dopant concentration of the substrate **102**. For example, the silicon material layer **100** and the substrate **102** may have the P-type conductivity type, and the P-type dopant concentration of the silicon material layer **100** may be less than the P-type dopant concentration of the substrate **102**. The method of forming the silicon material layer **100** is, for example, an epitaxial growth method or a chemical vapor deposition method.

[0042] Openings OP**1** may be formed in the silicon material layer **100**. In some embodiments, the silicon material layer **100** may be patterned by a lithography process and an etching process (e.g., dry etching process) to form the openings OP**1**. The openings OP**1** may include a ring-shaped opening OP**11**, and the ring-shaped opening OP**11** may surround the rest of the openings OP**1**. In some embodiments, during the process of forming the opening OP**1**, a portion of the substrate **102** may be removed, so that the opening OP**1** may extend into the substrate **102**.

[0043] Referring to FIG. **1**B and FIG. **2**B, a support frame material layer **104** may be conformally formed on the silicon material layer **100** and in the openings OP**1**. The support frame material layer **104** may have recesses R**1**. In some embodiments, the material of the support frame material layer **104** may be a conductive material such as titanium nitride, but the invention is not limited thereto. The method of forming the support frame material layer **104** is, for example, a chemical vapor deposition (CVD) method, a physical vapor deposition (PVD) method, or an atomic layer deposition (ALD) method.

[0044] Referring to FIG. **1**C and FIG. **2**C, a patterned photoresist layer **106** may be formed on the support frame material layer **104**. The patterned photoresist layer **106** may expose a portion of the support frame material layer **104**. In some embodiments, the patterned photoresist layer **106** may be formed by a lithography process.

[0045] A portion of the support frame material layer **104** may be removed by using the patterned photoresist layer **106** as a mask. Therefore, the support frame material layer **104** may be patterned to form a support frame layer **104***a* and a through hole H**1**. The through hole H**1** may expose the silicon material layer **100**. In addition, the support frame layer **104***a* may be formed in the silicon material layer **100** by the above method. The support frame layer **104***a* has recesses R**1**. The recesses R**1** may include a ring-shaped recess R**11**, and the ring-shaped recess R**11** may surround the rest of the recesses R**1**. The material of the support frame layer **104***a* may be a conductive material such as titanium nitride, but the invention is not limited thereto. In some embodiments, the method of removing the portion of the support frame material layer **104** is, for example, a dry etching method such as a reactive ion etching (RIE) method.

[0046] Referring to FIG. **1**D, the patterned photoresist layer **106** may be removed. The method of removing the patterned photoresist layer **106** is, for example, a dry stripping method or a wet stripping method.

[0047] Referring to FIG. **1**E and FIG. **2**D, a portion of the silicon material layer **100** exposed by the through hole H**1** may be removed to form a cavity C**1** between two adjacent recesses R**1**. The method of removing the portion of the silicon material layer **100** exposed by the through hole H**1** is, for example, a wet etching method. The etchant used in the wet etching method may include tetramethylammonium hydroxide (TMAH), potassium hydroxide (KOH), ethylenediamine pyrocatechol (EDP), hydrofluoric acid-nitric acid-acetic acid (HNA), or a combination thereof. In some embodiments, the portion of the silicon material layer **100** exposed by the through hole H**1** may be removed by using the substrate **102** as a stop layer. For example, when TMAH is used as the etchant of the wet etching method and the dopant concentration (e.g., P-type dopant concentration) of the silicon material layer **100** is less than the dopant concentration (e.g., P-type dopant concentration) of the substrate **102**, since the removal rate of TMAH to the silicon material layer **100** is greater than the removal rate of TMAH to the substrate **102**, the portion of the silicon material layer **100** exposed by the through hole H**1** may be removed by using the substrate **102** as a stop layer.

[0048] In some embodiments, as shown in FIG. **3**A, in the wet etching process of removing the portion of the silicon material layer **100** exposed by the through hole H**1**, a portion of the silicon material layer **100** located between the recesses R**1** and not located directly below the through hole H**1** may be further removed to form the cavity C**1** between two adjacent recesses R**1**.

[0049] In addition, there is a cavity C**1** between two adjacent recesses R**1**. The support frame layer **104***a* is located between the cavity C**1** and the recess R**1**. In some embodiments, the cavity C**1** and the recess R**1** are separated from each other by the support frame layer **104***a*. The support frame layer **104***a* has a through hole H**1** directly above the cavity C**1**.

[0050] Referring to FIG. **1**F and FIG. **3**B, a capacitor **108** is formed in the silicon material layer **100**. The capacitor **108** includes an insulating layer **110** and an electrode layer **112**. In the present embodiment, the material of the support frame layer **104***a* may be a conductive material, and the capacitor **108** may further include the support frame layer **104***a*. The insulating layer **110** is disposed on the support frame layer **104***a*. In some embodiments, the insulating layer **110** may be conformally disposed on the support frame layer **104***a*. The material of the insulating layer **110** is, for example, a high dielectric constant material. The method of forming the insulating layer **110** is, for example, a CVD method, a PVD method, or an ALD method. The electrode layer **112** is disposed on the insulating layer **110** and fills the recess R**1** and the cavity C**1**. The electrode layer **112** may be a single-layer structure or a multilayer structure. In some embodiments, the electrode layer **112** may include a conductive layer **112***a* and a conductive layer **112***b*, but the invention is not limited thereto. The conductive layer **112***a* is disposed on the insulating layer **110**. In some embodiments, the conductive layer **112***a* may be conformally disposed on the insulating layer **110**. The material of the conductive layer **112***a* is, for example, titanium nitride, ruthenium (Ru), or platinum (Pt). The method of forming the conductive layer **112***a* is, for example, a CVD method, a PVD method, or an ALD method. The conductive layer **112***b* is disposed on the conductive layer **112***a* and fills the recess R**1** and the cavity C**1**. The material of the conductive layer **112***b* is, for example, tungsten. The method of forming the conductive layer **112***b* is, for example, a CVD method or a PVD method.

[0051] Referring to FIG. **1**G, the electrode layer **112** may be patterned to define the pattern of the electrode layer **112**. In some embodiments, after the electrode layer **112** is patterned, a portion of the insulating layer **110** may be exposed. A portion of the capacitor **108** may be located outside the silicon material layer **100**. A portion of the support frame layer **104***a* may be located outside the silicon material layer **100**. For example, a portion of the support frame layer **104***a* may be located on the top surface S**1** of the silicon material layer **100**. A portion of the insulating layer **110** may be located outside the silicon material layer **100**. A portion of the electrode layer **112** may be located outside the silicon material layer **100**. In some embodiments, the electrode layer **112** may be patterned by a lithography process and an etching process. In some embodiments, according to the product requirement, the insulating layer **110** and the support frame layer **104***a* may be further patterned to define the pattern of the insulating layer **110** and the pattern of the support frame layer **104***a*. In some embodiments, the insulating layer **110** and the support frame layer **104***a* may be patterned by a lithography process and an etching process.

[0052] A dielectric layer **114** may be formed on the capacitor **108**. The material of the dielectric layer **114** is, for example, silicon oxide. The method of forming the dielectric layer **114** is, for example, a CVD method.

[0053] A contact **116** and a contact **118** may be formed in the dielectric layer **114**. The contact **116** may pass through the insulating layer **110** to be electrically connected to the support frame layer **104***a*. The contact **118** is electrically connected to the electrode layer **112**. The material of the contact **116** and the material of the contact **118** are, for example, tungsten. In some embodiments, the contact **116** and the contact **118** may be formed by a damascene process. In some embodiments, a barrier layer (not shown) may be formed between the contact **116** and the dielectric layer **114** and between the contact **116** and the support frame layer **104***a*, and a barrier layer (not shown) may be formed between the contact **118** and the dielectric layer **114** and between the contact **118** and the electrode layer **112**, and the description thereof is omitted here.

[0054] Hereinafter, the capacitor structure **10** of the above embodiments is described with reference to FIG. **1**G. In addition, although the method for forming the capacitor structure **10** is described by taking the above method as an example, the invention is not limited thereto.

[0055] Referring to FIG. **1**G, a capacitor structure **10** includes a silicon material layer **100**, a support frame layer **104***a*, and a capacitor **108**. The support frame layer **104***a* is disposed in the silicon material layer **100**. The support frame layer **104***a* has recesses R**1**. There is a cavity C**1** between two adjacent recesses R**1**. The support frame layer **104***a* is located between the cavity C**1** and the recess R**1**. In some embodiments, the cavity C**1** and the recess R**1** are separated from each other by the support frame layer **104***a*. The support frame layer **104***a* has a through hole H**1** directly above the cavity C**1**. The capacitor **108** is disposed in the silicon material layer **100**. The capacitor **108** includes an insulating layer **110** and an electrode layer **112**. The insulating layer **110** is disposed on the support frame layer **104***a*. The electrode layer **112** is disposed on the insulating layer **110** and fills the recess R**1** and the cavity C**1**. In the present embodiment, the material of the support frame layer **104***a* may be a conductive material, and the capacitor **108** may further include the support frame layer **104***a*. That is, the support frame layer **104***a* may be used as a portion of the capacitor **108**. For example, the support frame layer **104***a* may be used as another electrode layer of the capacitor **108**. In some embodiments, the capacitor structure **10** may further include a substrate **102**. The silicon material layer **100** is disposed on the substrate **102**. The silicon material layer **100** and the substrate **102** may have the same conductivity type. The dopant concentration of the silicon material layer **100** may be less than the dopant concentration of the substrate **102**.

[0056] In addition, the remaining components in the capacitor structure **10** may refer to the description of the above embodiments. Moreover, the details (e.g., the material, the arrangement, and the forming method) of each component in the capacitor structure **10** have been described in detail in the above embodiments, and the description thereof is not repeated here.

[0057] Based on the above embodiments, in the capacitor structure **10** and the manufacturing method thereof, the support frame layer **104***a* has the recesses R**1**, and there is the cavity C**1** between two adjacent recesses R**1**, the support frame layer **104***a* is located between the cavity C**1** and the recess R**1**, the support frame layer **104***a* has the through hole H**1** directly above the cavity C**1**, the insulating layer **110** is disposed on the support frame layer **104***a*, and the electrode layer **112** is disposed on the insulating layer **110** and fills the recess R**1** and the cavity C**1**. Therefore, the electrode layer **112** can have a larger area, thereby effectively increasing the capacitance value of the capacitor **108**.

[0058] FIG. **4**A to FIG. **4**B are cross-sectional views illustrating a manufacturing process of a capacitor structure according to other embodiments of the invention. FIG. **5** is a top view illustrating one stage of a manufacturing process of a capacitor structure according to other embodiments of the invention. FIG. **4**A to FIG. **4**B are cross-sectional views taken along section line III-III' in FIG. **5**.

[0059] Referring to FIG. **4**A and FIG. **5**, a silicon material layer **200** is provided. In some embodiments, the material of the silicon material layer **200** is, for example, single crystal silicon, but the invention is not limited thereto. In some embodiments, a substrate **202** may be further provided. The substrate **202** may be a semiconductor substrate such as a single crystal silicon substrate. In some embodiments, an insulating layer **204** may be further provided. The insulating layer **204** is located between the silicon material layer **200** and the substrate **202**. The material of the insulating layer **204** is, for example, silicon oxide. That is, in the present embodiment, a semiconductor-on-insulator (SOI) substrate **206** may be provided, and the SOI substrate **206** may include the silicon material layer **200**, the substrate **202**, and the insulating layer **204**.

[0060] Opening OP**2** may be formed in the silicon material layer **200**. In some embodiments, the silicon material layer **200** may be patterned by a lithography process and an etching process (e.g., dry etching process) to form the openings OP**2**. The openings OP**2** may include a ring-shaped opening OP**21**, and the ring-shaped opening OP**21** may surround the rest of the openings OP**2**. In some embodiments, during the process of forming the opening OP**2**, a portion of the insulating layer **204** may be removed, so that the opening OP**2** may extend into the insulating layer **204**.

[0061] Referring to FIG. **4**B, the steps as shown in FIG. **1**B to FIG. **1**G may be performed to form a capacitor structure **20**, and the description thereof is not repeated here.

In the present embodiment, in the process of forming the cavity C1, the portion of the silicon material layer **200** exposed by the through hole H1 may be removed by using the insulating layer **204** as a stop layer.

[0062] Hereinafter, the capacitor structure **20** of the above embodiments is described with reference to FIG. **4**B. In addition, although the method for forming the capacitor structure **20** is described by taking the above method as an example, the invention is not limited thereto.

[0063] Referring to FIG. **4**B, a capacitor structure **20** includes a silicon material layer **200**, a support frame layer **104***a*, and a capacitor **108**. The support frame layer **104***a* is disposed in the silicon material layer **200**. The support frame layer **104***a* has recesses R1. There is a cavity C1 between two adjacent recesses R1. The support frame layer **104***a* is located between the cavity C1 and the recess R1. In some embodiments, the cavity C1 and the recess R1 are separated from each other by the support frame layer **104***a*. The support frame layer **104***a* has a through hole H1 directly above the cavity C1. The capacitor **108** is disposed in the silicon material layer **200**. The capacitor **108** includes an insulating layer **110** and an electrode layer **112**. The insulating layer **110** is disposed on the support frame layer **104***a*. The electrode layer **112** is disposed on the insulating layer **110** and fills the recess R1 and the cavity C1. In the present embodiment, the material of the support frame layer **104***a* may be a conductive material, and the capacitor **108** may further include the support frame layer **104***a*. That is, the support frame layer **104***a* may be used as a portion of the capacitor **108**. For example, the support frame layer **104***a* may be used as another electrode layer of the capacitor **108**. In some embodiments, the capacitor structure **20** may further include a substrate **202** and an insulating layer **204**. The silicon material layer **200** is disposed on the substrate **202**. The insulating layer **204** is disposed between the silicon material layer **200** and the substrate **202**.

[0064] In addition, the remaining components in the capacitor structure **20** may refer to the description of the above embodiments. Moreover, the details (e.g., the material, the arrangement, and the forming method) of each component in the capacitor structure **20** have been described in detail in the above embodiments, and the description thereof is not repeated here.

[0065] Based on the above embodiments, in the capacitor structure **20** and the manufacturing method thereof, the support frame layer **104***a* has the recesses R1, and there is the cavity C1 between two adjacent recesses R1, the support frame layer **104***a* is located between the cavity C1 and the recess R1, the support frame layer **104***a* has the through hole H1 directly above the cavity C1, the insulating layer **110** is disposed on the support frame layer **104***a*, and the electrode layer **112** is disposed on the insulating layer **110** and fills the recess R1 and the cavity C1. Therefore, the electrode layer **112** can have a larger area, thereby effectively increasing the capacitance value of the capacitor **108**.

[0066] FIG. **6**A to FIG. **6**B are cross-sectional views illustrating a manufacturing process of a capacitor structure according to other embodiments of the invention. FIG. **7** is a top view illustrating one stage of a manufacturing process of a capacitor structure according to other embodiments of the invention. FIG. **6**A to FIG. **6**B are cross-sectional views taken along section line IV-IV' in FIG. **7**.

[0067] Referring to FIG. **6**A and FIG. **7**, a silicon material layer **300** is provided. In some embodiments, the material of the silicon material layer **300** is, for example, single crystal silicon, but the invention is not limited thereto. In some embodiments, the silicon material layer **300** may be a semiconductor substrate such as a single crystal silicon substrate.

[0068] Opening OP**3** may be formed in the silicon material layer **300**. In some embodiments, the silicon material layer **300** may be patterned by a lithography process and an etching process (e.g., dry etching process) to form the openings OP**3**. The openings OP**3** may include a ring-shaped opening OP**31**, and the ring-shaped opening OP**31** may surround the rest of the openings OP**3**.

[0069] Referring to FIG. **6**B, the steps as shown in FIG. **1**B to FIG. **1**G may be performed to form a capacitor structure **30**, and the description thereof is not repeated here. In the present embodiment, in the process of forming the cavity C1, the depth of the cavity C1 may be controlled by controlling the time of the etching process (e.g., wet etching process).

[0070] Hereinafter, the capacitor structure **30** of the above embodiments is described with reference to FIG. **6**B. In addition, although the method for forming the capacitor structure **30** is described by taking the above method as an example, the invention is not limited thereto.

[0071] Referring to FIG. **6**B, a capacitor structure **30** includes a silicon material layer **300**, a support frame layer **104***a*, and a capacitor **108**. The support frame layer **104***a* is disposed in the silicon material layer **300**. The support frame layer **104***a* has recesses R1. There is a cavity C1 between two adjacent recesses R1. The support frame layer **104***a* is located between the cavity C1 and the recess R1. In some embodiments, the cavity C1 and the recess R1 are separated from each other by the support frame layer **104***a*. The support frame layer **104***a* has a through hole H1 directly above the cavity C1. The capacitor **108** is disposed in the silicon material layer **300**. The capacitor **108** includes an insulating layer **110** and an electrode layer **112**. The insulating layer **110** is disposed on the support frame layer **104***a*. The electrode layer **112** is disposed on the insulating layer **110** and fills the recess R1 and the cavity C1. In the present embodiment, the material of the support frame layer **104***a* may be a conductive material, and the capacitor **108** may further include the support frame layer **104***a*. That is, the support frame layer **104***a* may be used as a portion of the capacitor **108**. For example, the support frame layer **104***a* may be used as another electrode layer of the capacitor **108**.

[0072] In addition, the remaining components in the capacitor structure **30** may refer to the description of the above embodiments. Moreover, the details (e.g., the material, the arrangement, and the forming method) of each component in the capacitor structure **30** have been described in detail in the above embodiments, and the description thereof is not repeated here.

[0073] Based on the above embodiments, in the capacitor structure **30** and the manufacturing method thereof, the support frame layer **104***a* has the recesses R1, and there is the cavity C1 between two adjacent recesses R1, the support frame layer **104***a* is located between the cavity C1 and the recess R1, the support frame layer **104***a* has the through hole H1 directly above the cavity C1, the insulating layer **110** is disposed on the support frame layer **104***a*, and the electrode layer **112** is disposed on the insulating layer **110** and fills the recess R1 and the cavity C1. Therefore, the electrode layer

112 can have a larger area, thereby effectively increasing the capacitance value of the capacitor 108.

[0074] FIG. 8A to FIG. 8E are cross-sectional views illustrating a manufacturing process of a capacitor structure according to other embodiments of the invention. FIG. 9A to FIG. 9C are top views illustrating some stages of a manufacturing process of a capacitor structure according to other embodiments of the invention. FIG. 8A to FIG. 8E are cross-sectional views taken along section line V-V' in FIG. 9A to FIG. 9C. FIG. 10A and FIG. 10B are cross-sectional views illustrating some stages of a manufacturing process of a capacitor structure according to other embodiments of the invention. FIG. 10A and FIG. 10B are cross-sectional views taken along section line VI-VI' in FIG. 9C. In the top view of the present embodiment, some components in the cross-sectional view are omitted to clearly illustrate the configuration relationship between the components in the top view.

[0075] Referring to FIG. 8A and FIG. 9A, the structure of FIG. 1A and FIG. 2A is provided. The structure of FIG. 1A and FIG. 2A and the manufacturing method thereof have been described in detail in the above embodiments, and the description thereof is not repeated here.

[0076] Referring to FIG. 8B and FIG. 9B, a support frame material layer 404 may be conformally formed on the silicon material layer 100 and in the openings OP1. The support frame material layer 404 may have recesses R2. In some embodiments, the material of the support frame material layer 404 may be a dielectric material such as silicon nitride, but the invention is not limited thereto. The method of forming the support frame material layer 404 is, for example, a CVD method, a PVD method, or an ALD method.

[0077] Referring to FIG. 8C, FIG. 9C, and FIG. 10A, the steps as shown in FIG. 1C to FIG. 1E may be performed to form a support frame layer 404 a in the silicon material layer 100, and the description thereof is not repeated here. The support frame layer 404*a* has recesses R2. The recesses R2 may include a ring-shaped recess R21, and the ring-shaped recesses R21 may surround the rest of recesses R2. There is a cavity C2 between two adjacent recesses R2. The support frame layer 404*a* is located between the cavity C2 and the recess R2. In some embodiments, the cavity C2 and the recess R2 are separated from each other by the support frame layer 404*a*. The support frame layer 404*a* has a through hole H2 directly above the cavity C2. The material of the support frame layer 404*a* may be a dielectric material such as silicon nitride, but the invention is not limited thereto.

[0078] Referring to FIG. 8D and FIG. 10B, a capacitor 408 is formed in the silicon material layer 100. The capacitor 408 includes an insulating layer 410 and an electrode layer 412. The insulating layer 410 is disposed on the support frame layer 404*a*. The material of the insulating layer 410 is, for example, a high dielectric constant material. The method for forming the insulating layer 410 is, for example, a CVD method, a PVD method, or an ALD method. The electrode layer 412 is disposed on the insulating layer 410 and fills the recess R2 and the cavity C2. The electrode layer 412 may be a single-layer structure or a multilayer structure. In some embodiments, the electrode layer 412 may include a conductive layer 412*a* and a conductive layer 412*b*, but the invention is not limited thereto. The conductive layer 412*a* is disposed on the insulating layer 410. The material of the conductive layer 412*a* is, for example, titanium nitride, ruthenium (Ru), or platinum (Pt). The method of forming the conductive layer 412*a* is, for example, a CVD method, a PVD method, or an ALD method. The conductive layer 412*b* is disposed on the conductive layer 412*a* and fills the recess R2 and the cavity C2. The material of the conductive layer 412*b* is, for example, tungsten. The method of forming the conductive layer 412*b* is, for example, a CVD method or a PVD method. In the present embodiment, the material of the support frame layer 404*a* may be a dielectric material, and the capacitor 408 may further include an electrode layer 414. The electrode layer 414 is disposed between the insulating layer 410 and the support frame layer 404*a*. The material of the electrode layer 414 is, for example, titanium nitride. The method of forming the electrode layer 414 is, for example, a CVD method, a PVD method, or an ALD method. In some embodiments, the electrode layer 414 may be conformally disposed on the support frame layer 404*a*. In some embodiments, the insulating layer 410 may be conformally disposed on the electrode layer 414. In some embodiments, the conductive layer 412*a* may be conformally disposed on the insulating layer 410.

[0079] Referring to FIG. 8E, the electrode layer 412 and the insulating layer 410 may be patterned to define the pattern of the electrode layer 412 and the pattern of the insulating layer 410. In some embodiments, after the electrode layer 412 and the insulating layer 410 are patterned, a portion of the electrode layer 414 may be exposed. A portion of the capacitor 408 may be located outside the silicon material layer 100. A portion of the support frame layer 404*a* may be located outside the silicon material layer 100. For example, a portion of the support frame layer 404*a* may be located above the top surface S1 of the silicon material layer 100. A portion of the insulating layer 410 may be located outside the silicon material layer 100. A portion of the electrode layer 412 may be located outside the silicon material layer 100. A portion of the electrode layer 414 may be located outside the silicon material layer 100. In some embodiments, the electrode layer 412 and the insulating layer 410 may be patterned by a lithography process and an etching process. In some embodiments, according to the product requirement, the electrode layer 414 may be further patterned to define the pattern of the electrode layer 414. In some embodiments, the electrode layer 414 may be patterned by a lithography process and an etching process.

[0080] A dielectric layer 416 may be formed on the capacitor 408. The material of the dielectric layer 416 is, for example, silicon oxide. The method of forming the dielectric layer 416 is, for example, a CVD method.

[0081] A contact 418 and a contact 420 may be formed in the dielectric layer 416. The contact 418 is electrically connected to the electrode layer 414. The contact 420 is electrically connected to the electrode layer 412. The material of the contact 418 and the material of the contact 420 are, for example, tungsten. In some embodiments, the contact 418 and the contact 420 may be formed by a damascene process. In some embodiments, a barrier layer (not shown) may be formed between the contact 418 and the dielectric layer 416 and between the contact 418 and the electrode layer 414, and a barrier layer (not shown) may be formed between the contact 420 and the dielectric layer 416 and between the contact 420 and the electrode layer 412, and the description thereof is omitted here.

[0082] Hereinafter, the capacitor structure 40 of the above embodiments is described with reference to FIG. 8E. In addition, although the method for forming the capacitor

structure **40** is described by taking the above method as an example, the invention is not limited thereto.

[0083] Referring to FIG. **8**E, a capacitor structure **40** includes a silicon material layer **100**, a support frame layer **404***a*, and a capacitor **408**. The support frame layer **404***a* is disposed in the silicon material layer **100**. The support frame layer **404***a* has recesses R**2**. There is a cavity C**2** between two adjacent recesses R**2**. The support frame layer **404***a* is located between the cavity C**2** and the recess R**2**. In some embodiments, the cavity C**2** and the recess R**2** are separated from each other by the support frame layer **404***a*. The support frame layer **404***a* has a through hole H**2** directly above the cavity C**2**. The capacitor **408** is disposed in the silicon material layer **100**. The capacitor **408** includes an insulating layer **410** and an electrode layer **412**. The insulating layer **410** is disposed on the support frame layer **404***a*. The electrode layer **412** is disposed on the insulating layer **410** and fills the recess R**2** and the cavity C**2**. The material of the support frame layer **404***a* may be a dielectric material, and the capacitor **408** may further include an electrode layer **414**. The electrode layer **414** is disposed between the insulating layer **410** and the support frame layer **404***a*. In some embodiments, the capacitor structure **40** may further include a substrate **102**. The silicon material layer **100** is disposed on the substrate **102**. The silicon material layer **100** and the substrate **102** may have the same conductivity type. The dopant concentration of the silicon material layer **100** may be less than the dopant concentration of the substrate **102**.

[0084] In addition, the remaining components in the capacitor structure **40** may refer to the description of the above embodiments. Moreover, the details (e.g., the material, the arrangement, and the forming method) of each component in the capacitor structure **40** have been described in detail in the above embodiments, and the description thereof is not repeated here.

[0085] Based on the above embodiments, in the capacitor structure **40** and the manufacturing method thereof, the support frame layer **404***a* has the recesses R**2**, and there is the cavity C**2** between two adjacent recesses R**2**, the support frame layer **404***a* is located between the cavity C**2** and the recess R**2**, the support frame layer **404***a* has the through hole H**2** directly above the cavity C**2**, the insulating layer **410** is disposed on the support frame layer **404***a*, and the electrode layer **412** is disposed on the insulating layer **410** and fills the recess R**2** and the cavity C**2**. Therefore, the electrode layer **412** can have a larger area, thereby effectively increasing the capacitance value of the capacitor **408**.

[0086] In other embodiments, the silicon material layer **100** and the substrate **102** in the capacitor structure **40** may be replaced with the SOI substrate **206** in FIG. **4**B. In other embodiments, the silicon material layer **100** and the substrate **102** in the capacitor structure **40** may be replaced with the silicon material layer **300** in FIG. **6**B.

[0087] FIG. **11** is a cross-sectional view illustrating a semiconductor structure according to some embodiments of the invention.

[0088] Referring to FIG. **11**, the capacitor structure **10** of FIG. **1**G may be integrated into a semiconductor structure **50**. In some embodiments, the semiconductor structure **50** may be an interposer structure, but the invention is not limited thereto. The semiconductor structure **50** may include a capacitor structure **10**, a through-substrate via (TSV) **500**, and an interconnect structure **502**. In some embodiments, the dielectric layer **114** may be a multilayer structure. The TSV **500** may pass through the silicon material layer **100** and the substrate **102**. Furthermore, a portion of the TSV **500** may be located in the dielectric layer **114**. The interconnect structure **502** is disposed in the dielectric layer **114** and is electrically connected to the TSV **500**. In addition, the contact **116** and the contact **118** may be electrically connected to different interconnect structures (not shown).

[0089] On the other hand, the capacitor structure **20** of FIG. **4**B, the capacitor structure **30** of FIG. **6**B, and the capacitor structure **40** of FIG. **8**E may also be integrated into semiconductor structures such as interposer structures.

[0090] In summary, in the capacitor structure and the manufacturing method thereof in aforementioned embodiments, the support frame layer has the recesses, there is the cavity between two adjacent recesses, the support frame layer is located between the cavity and the recess, the support frame layer has the through hole directly above the cavity, the insulating layer is disposed on the support frame layer, and the electrode layer is disposed on the insulating layer and fills the recess and the cavity. Therefore, the electrode layer can have a larger area, thereby effectively increasing the capacitance value of the capacitor.

[0091] Although the invention has been described with reference to the above embodiments, it will be apparent to one of ordinary skill in the art that modifications to the described embodiments may be made without departing from the spirit of the invention. Accordingly, the scope of the invention is defined by the attached claims not by the above detailed descriptions.

What is claimed is:

1. A capacitor structure, comprising:

a silicon material layer;

a support frame layer disposed in the silicon material layer, wherein the support frame layer has recesses, and there is a cavity between two adjacent recesses, the support frame layer is located between the cavity and the recess, and the support frame layer has a through hole directly above the cavity; and

a capacitor disposed in the silicon material layer and comprising:

a first insulating layer disposed on the support frame layer; and

a first electrode layer disposed on the first insulating layer and filling the recess and the cavity.

2. The capacitor structure according to claim **1**, wherein a material of the silicon material layer comprises epitaxial silicon, polysilicon, or single crystal silicon.

3. The capacitor structure according to claim **1**, wherein a portion of the support frame layer is located outside the silicon material layer.

4. The capacitor structure according to claim **1**, wherein a portion of the capacitor is located outside the silicon material layer.

5. The capacitor structure according to claim **1**, wherein the recesses comprise a ring-shaped recess, and the ring-shaped recess surrounds the rest of the recesses.

6. The capacitor structure according to claim **1**, wherein a material of the support frame layer is a conductive material, and the capacitor further comprises the support frame layer.

7. The capacitor structure according to claim **1**, wherein a material of the support frame layer is a dielectric material, and the capacitor further comprises:

a second electrode layer disposed between the first insulating layer and the support frame layer.

8. The capacitor structure according to claim **1**, wherein the first electrode layer comprises:

a first conductive layer disposed on the first insulating layer; and

a second conductive layer disposed on the first conductive layer and filling the recess and the cavity.

9. The capacitor structure according to claim **1**, further comprising:

a substrate, wherein the silicon material layer is disposed on the substrate, the silicon material layer and the substrate have the same conductivity type, and a dopant concentration of the silicon material layer is less than a dopant concentration of the substrate.

10. The capacitor structure according to claim **1**, further comprising:

a substrate, wherein the silicon material layer is disposed on the substrate; and

a second insulating layer disposed between the silicon material layer and the substrate.

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