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(54) **METHODS FOR MODELING CMOS TRANSISTOR CHARACTERISTICS IN CRYOGENIC CONDITIONS**

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(52) **U.S. Cl.**

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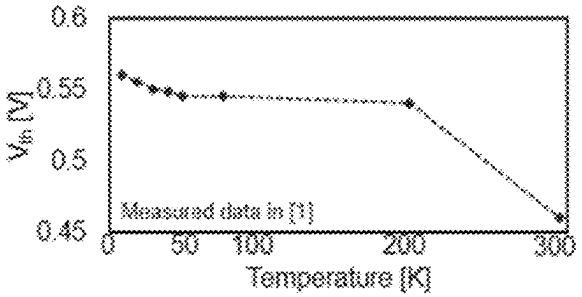
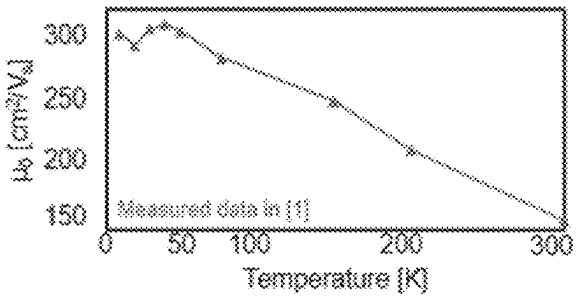
(57) **ABSTRACT**

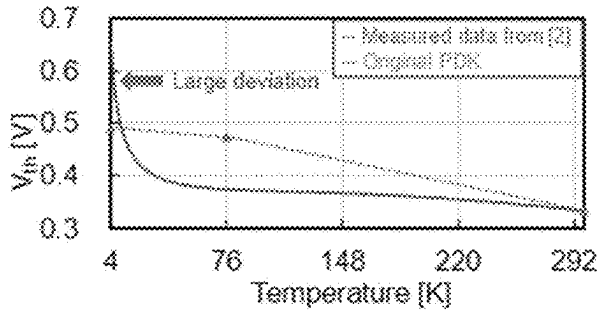
Proposed is a method of modeling characteristics of a CMOS transistor in cryogenic conditions on the basis of a PSP model, and the method includes receiving a process design kit (PDK) comprising device information and process information, which are required for designing and implementing an integrated circuit, extracting at least one parameter for modeling a prediction model for predicting characteristic values of a device comprised in the integrated circuit in cryogenic conditions from the PDK, and modeling the prediction model by adjusting the at least one parameter, so as to predict the characteristic values of the device in cryogenic conditions.



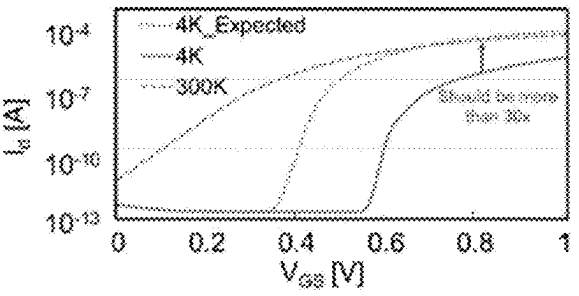
(a) Threshold voltage redrawn from [1]



(b) Mobility redrawn form [1]



(a) Simulated V_{th} of commercial PDK & measurement results in [2]



(b) I_d-V_{GS} of commercial PDK and expected I_d @ 4K

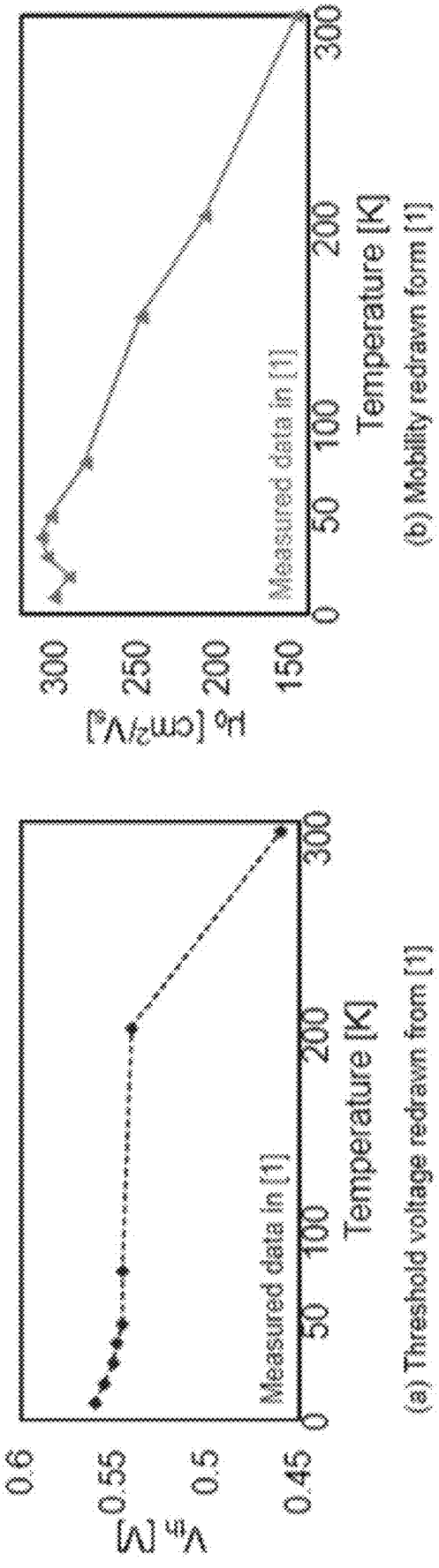
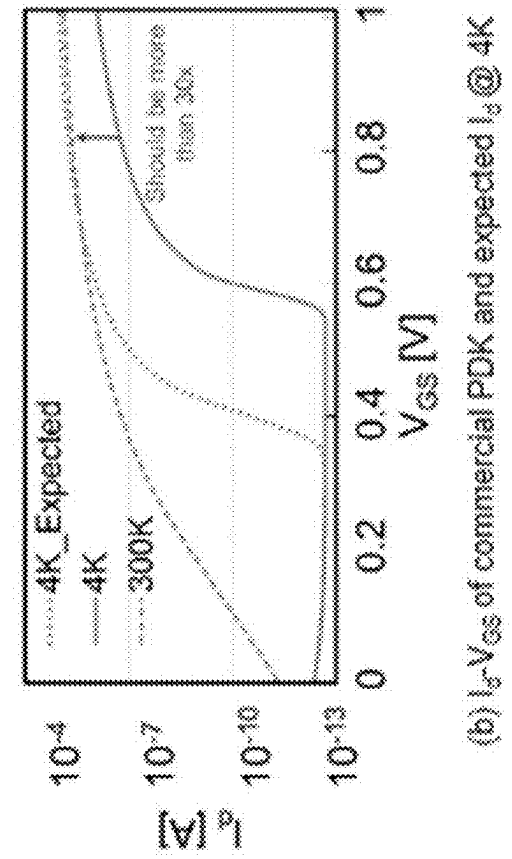
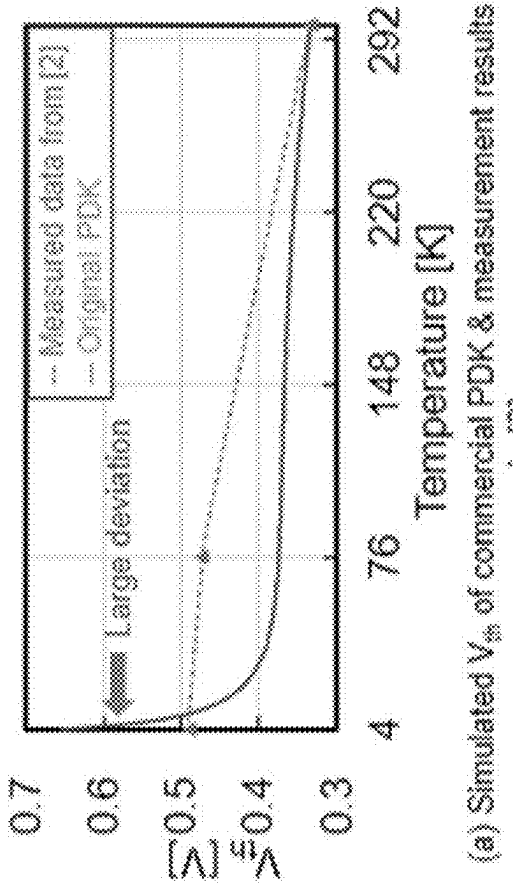

(a) Threshold voltage redrawn from [1]
Measured data in [1]
Temperature [K]
0
50
100
200
300
0.45
0.5
0.55
0.6
V_{th} [V]
(b) Mobility redrawn from [1]
Measured data in [1]
Temperature [K]
0
50
100
200
300
150
200
250
300
μ_0 [cm²/V.s]

FIG. 1A



(b) I_d-V_{GS} of commercial PDK and expected I_d @ 4K



(a) Simulated V_{th} of commercial PDK & measurement results in [2]

FIG. 1B

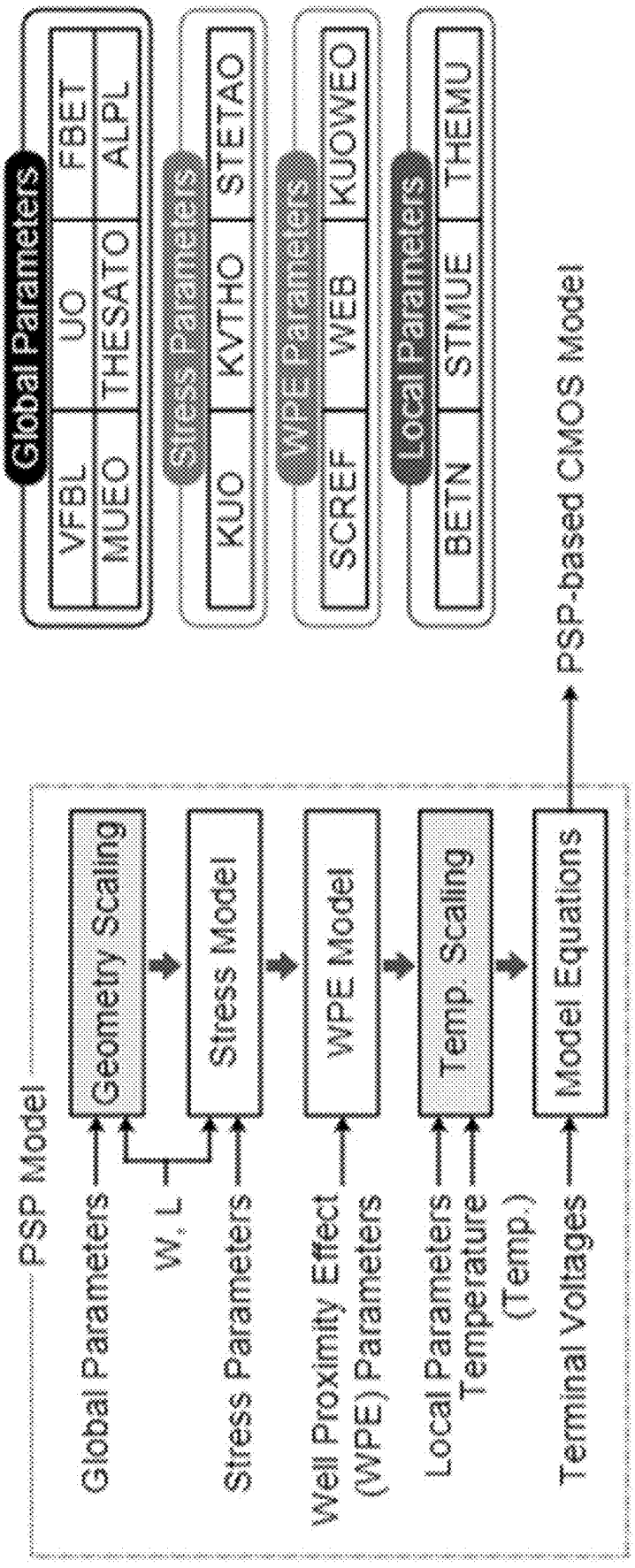

PSP Model
Global Parameters
W, L
Stress Parameters
Well Proximity Effect (WPE) Parameters
Local Parameters
Temperature (Temp.)
Terminal Voltages
Geometry Scaling
Stress Model
WPE Model
Temp Scaling
Model Equations
PSP-based CMOS Model
Global Parameters
VFBL
MUEO
UO
THESATO
FBET
ALPL
Stress Parameters
KUO
KVTHO
STETAO
WPE Parameters
SCREF
WEB
KUOWEO
Local Parameters
BETN
STMUE
THEMU

FIG. 1C

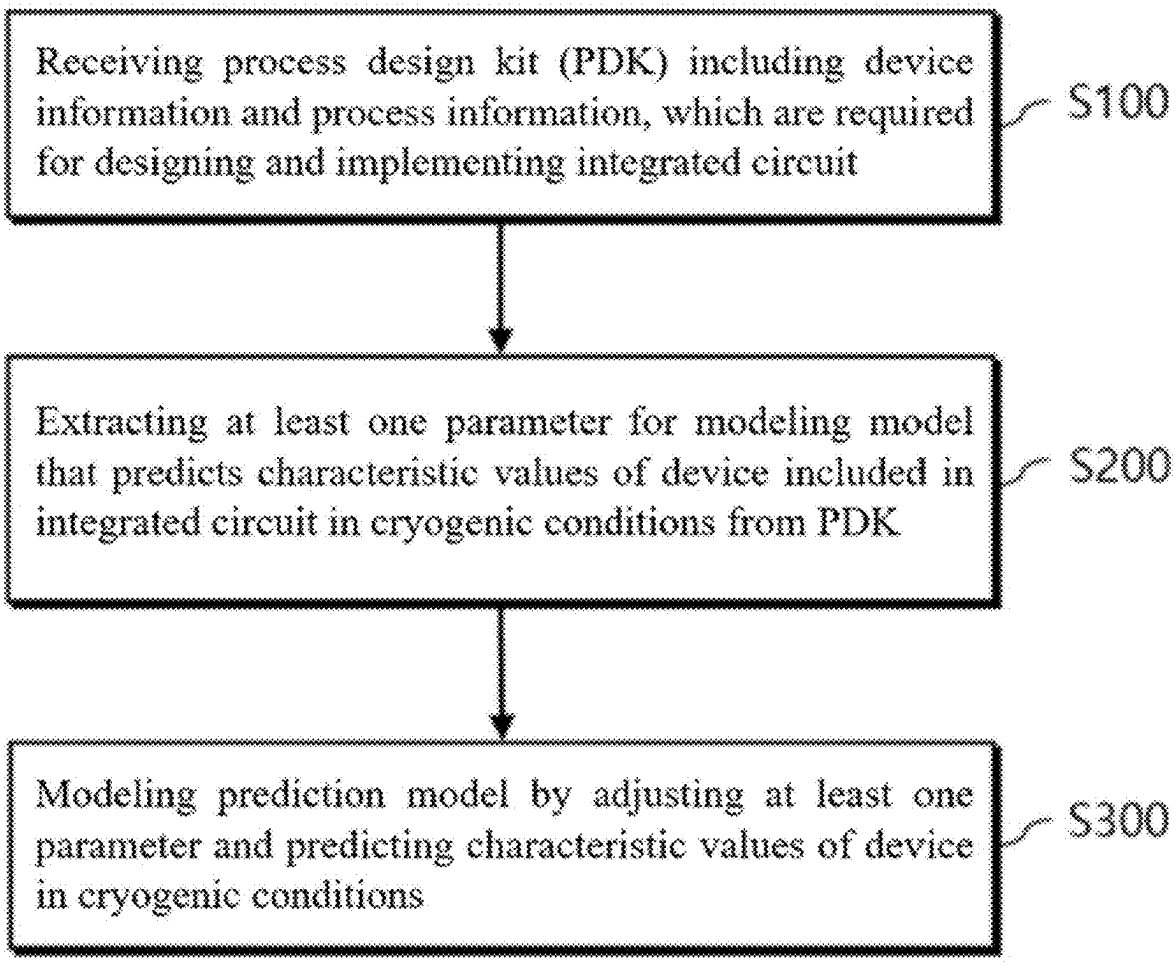

Receiving process design kit (PDK) including device information and process information, which are required for designing and implementing integrated circuit
S100
Extracting at least one parameter for modeling model that predicts characteristic values of device included in integrated circuit in cryogenic conditions from PDK
S200
Modeling prediction model by adjusting at least one parameter and predicting characteristic values of device in cryogenic conditions
S300

FIG. 2

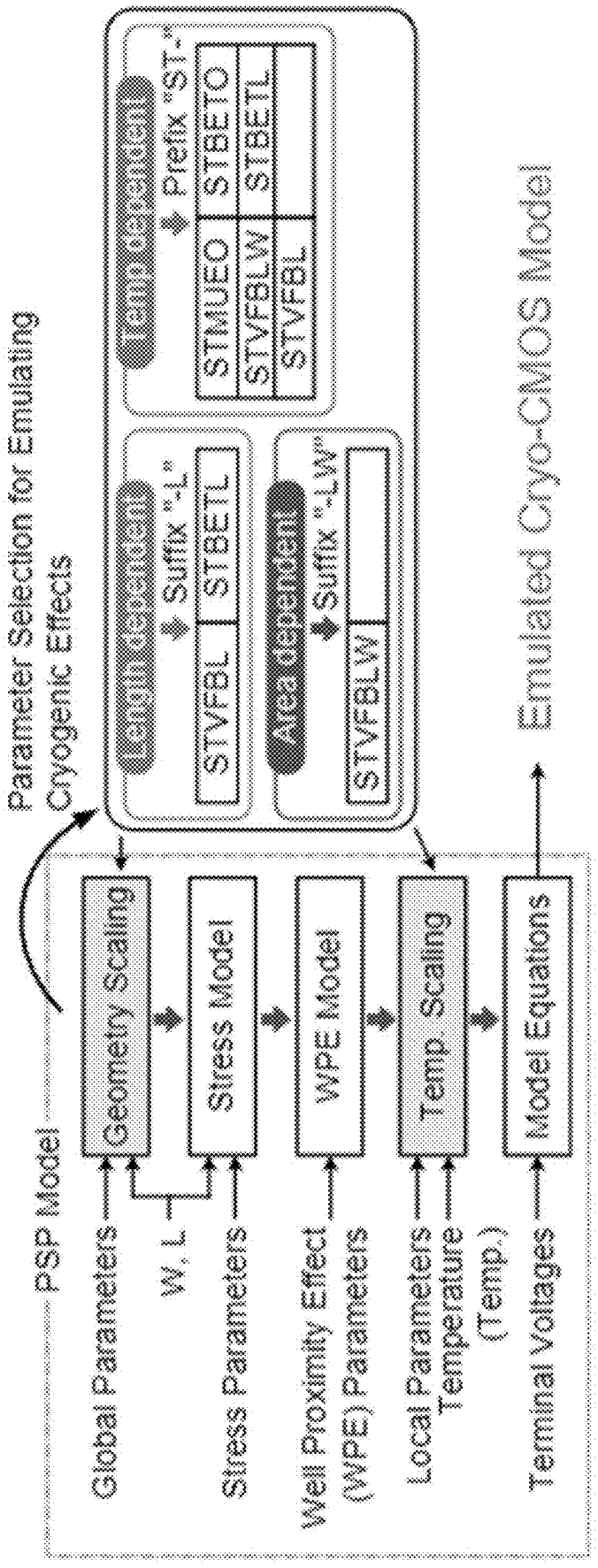

PSP Model
Parameter Selection for Emulating Cryogenic Effects
Emulated Cryo-CMOS Model
Geometry Scaling
Stress Model
WPE Model
Temp Scaling
Model Equations
Global Parameters
W, L
Stress Parameters
Well Proximity Effect (WPE) Parameters
Local Parameters
Temperature (Temp.)
Terminal Voltages
Temp dependent
Prefix "ST-"
STMUEO
STVFBLW
STVFBL
STBETO
STBETL
Temp dependent
Suffix "-L"
STVFBL
STBETL
Area dependent
Suffix "-LW"
STVFBLW

FIG. 3

	[JEDS 2018] A. Beckers	[JEDS 2018] R. M. Incandela	This Work
Technology	28 nm	40 nm	28 nm
Transistor Type	Bulk CMOS	Bulk CMOS	Bulk CMOS
Model	Physics-based	PSP	PSP
Consider Higher V_{th}	Yes	Yes	Yes
Consider Higher μ	Yes	Yes	Yes
# of Modified Parameters	-	9	6
Consider Geometry-dependent Effects?	-	No	Yes

FIG. 4

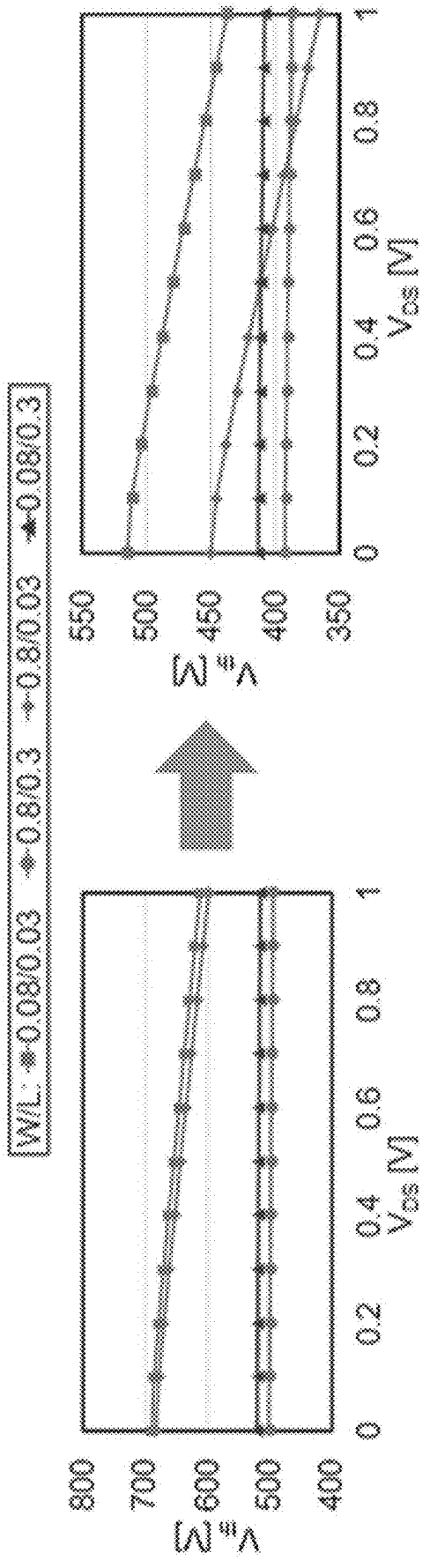

W/L: 0.08/0.03 0.8/0.3 0.8/0.03 0.08/0.3
V_{in} [V]
V_{out} [V]
0 0.2 0.4 0.6 0.8 1
800 700 600 500 400
550 500 450 400 350

FIG. 5A

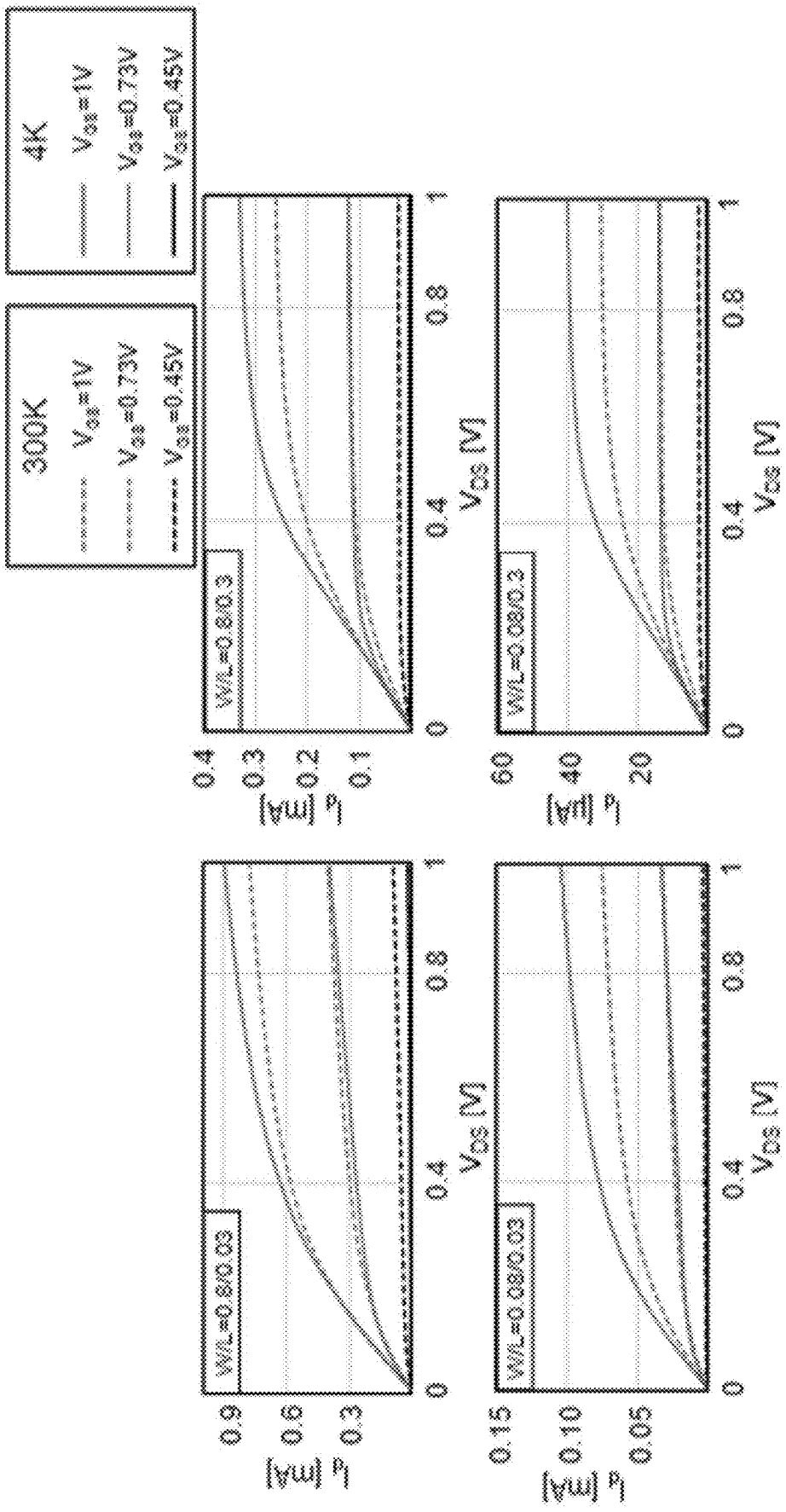

4K
V_{GS}=1V
V_{GS}=0.73V
V_{GS}=0.45V
300K
V_{GS}=1V
V_{GS}=0.73V
V_{GS}=0.45V
W/L=0.8/0.3
W/L=0.08/0.3
W/L=0.8/0.03
W/L=0.08/0.03
I_d [mA]
I_d [μA]
V_{DS} [V]
0
0.4
0.8
1
0.1
0.2
0.3
0.4
20
40
60
0.3
0.6
0.9
0.05
0.10
0.15

FIG. 5B

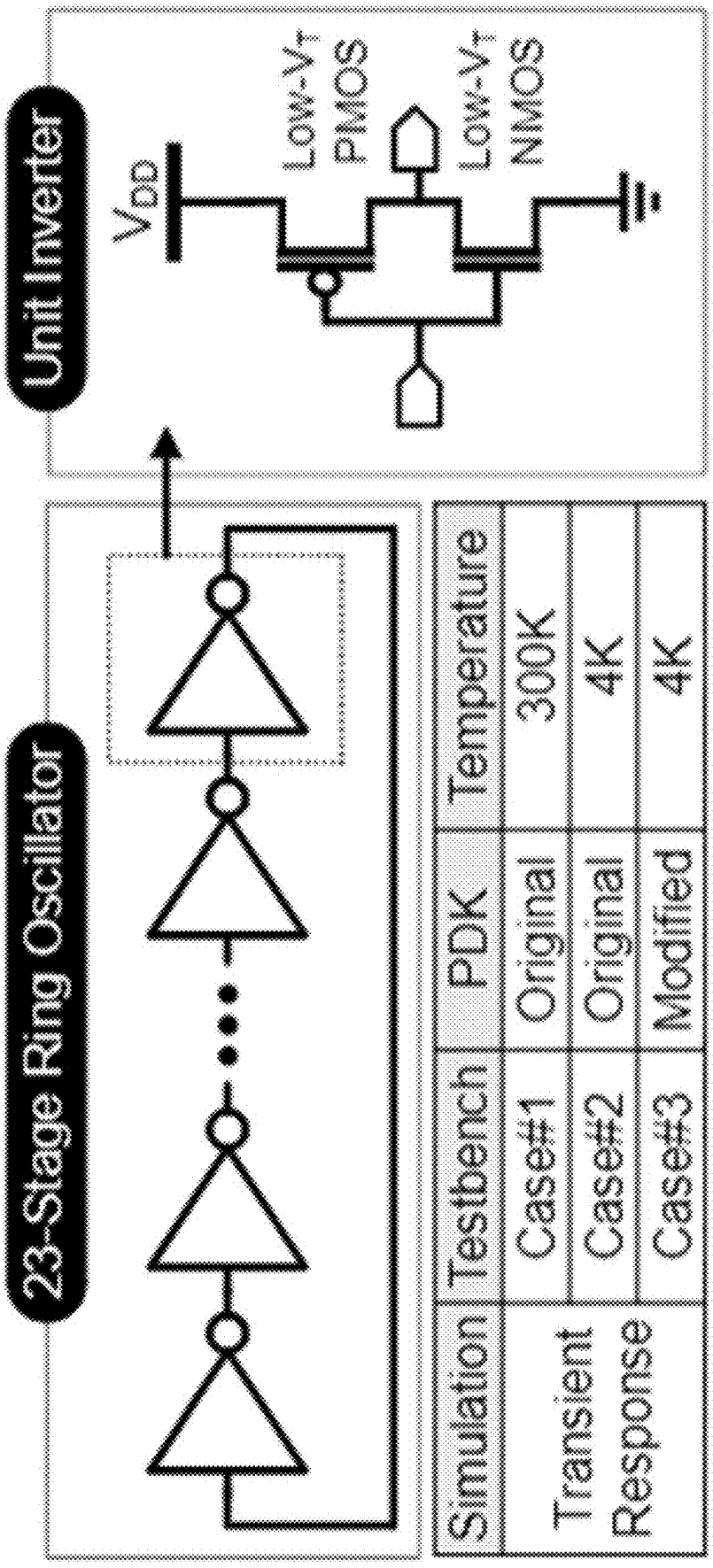

23-Stage Ring Oscillator
Unit Inverter
V_{DD}
Low-V_T PMOS
Low-V_T NMOS
Simulation
Testbench
PDK
Temperature
Transient Response
Case#1
Original
300K
Case#2
Original
4K
Case#3
Modified
4K

FIG. 6A

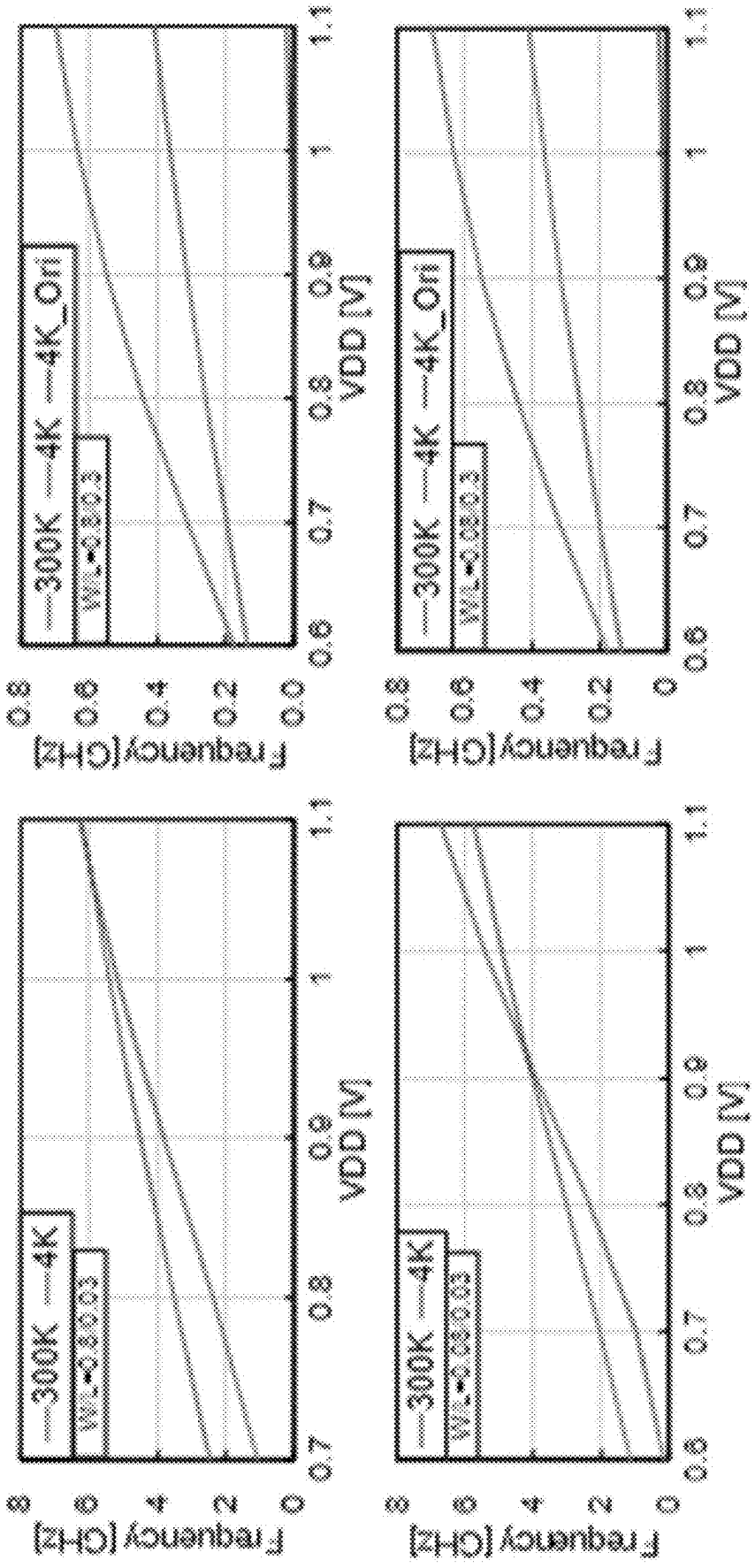

—300K —4K —4K_Ori
WL=2.0803
Frequency [GHz]
VDD [V]
—300K —4K
WL=2.0803
Frequency [GHz]
VDD [V]

FIG. 6B

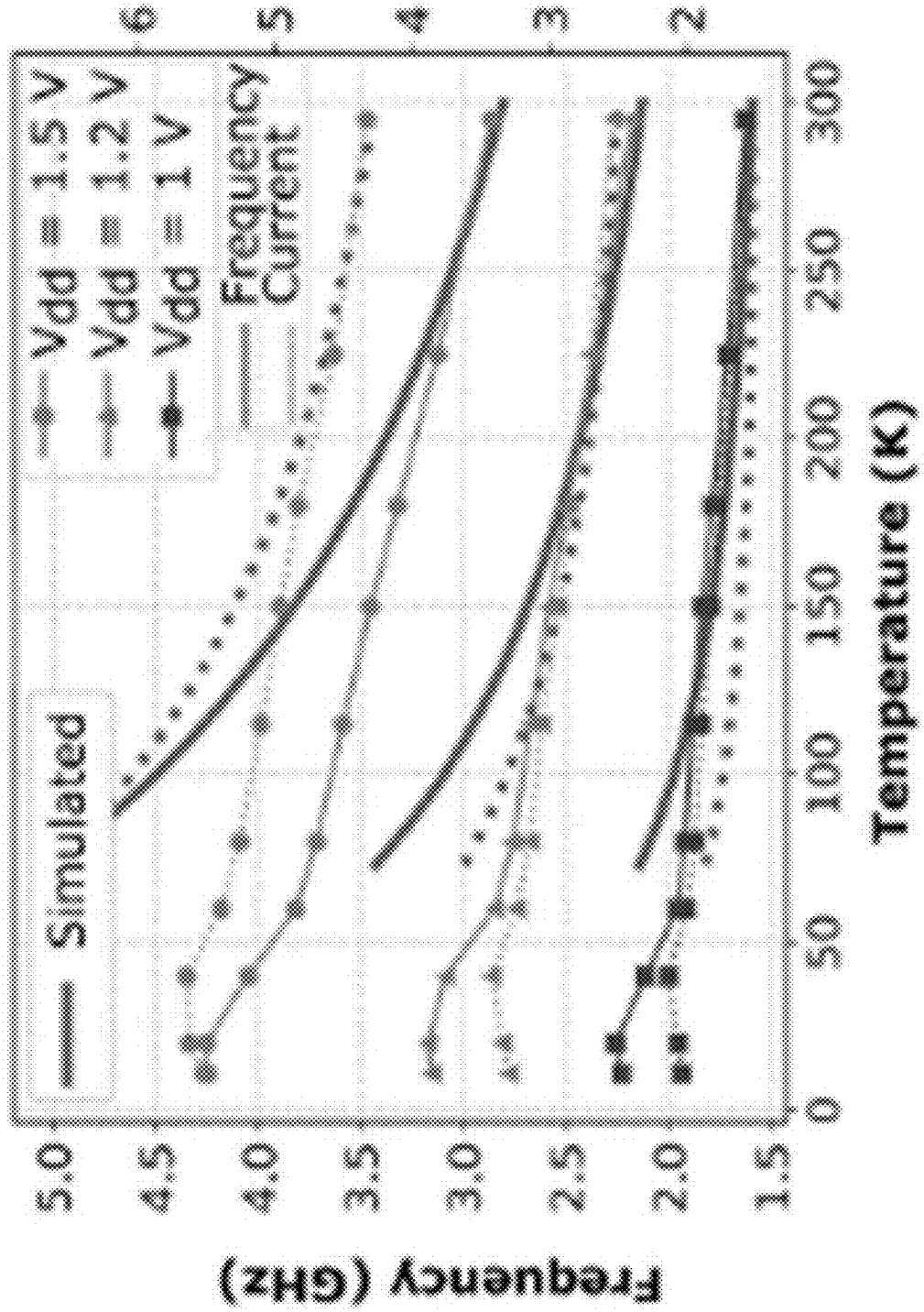

Frequency (GHz)
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
Temperature (K)
0
50
100
150
200
250
300
Frequency
Current
2
3
4
5
6
Simulated
Vdd = 1.5 V
Vdd = 1.2 V
Vdd = 1 V

FIG. 6C

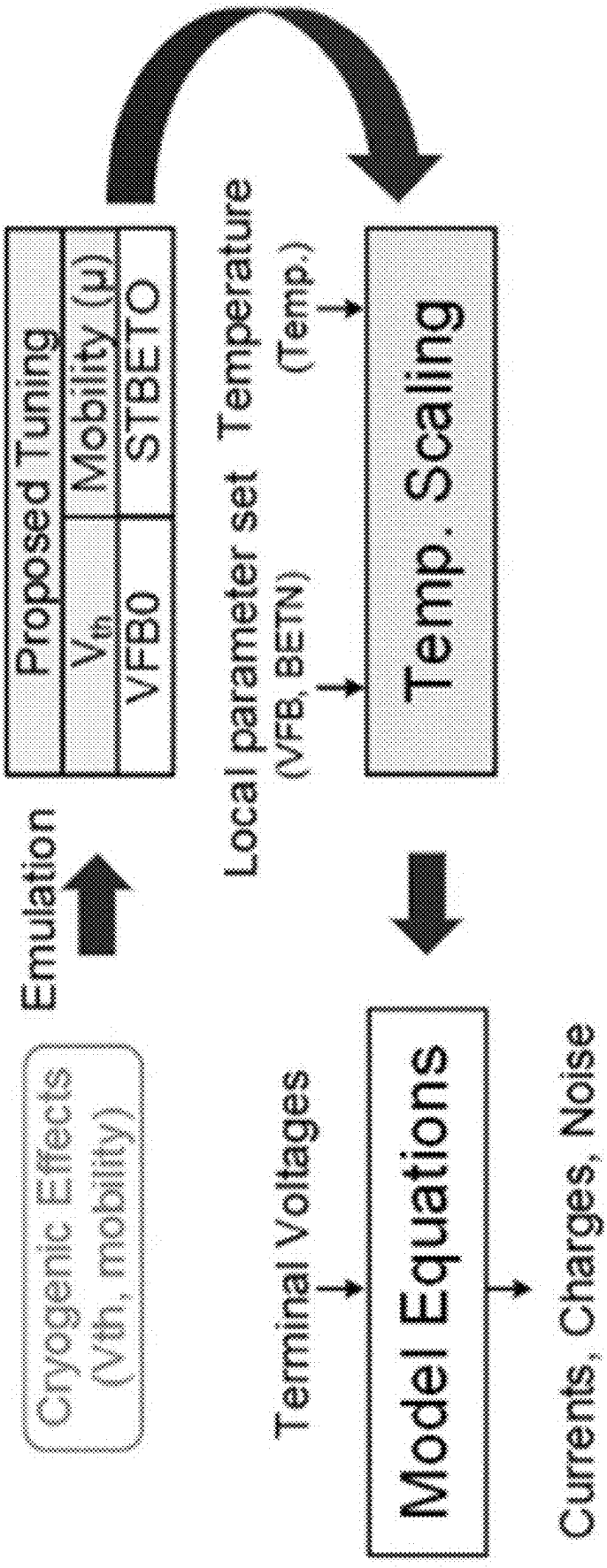

Proposed Tuning
V_{th}
Mobility (μ)
VFB0
STBETO
Emulation
Local parameter set
(VFB, BETN)
Temperature
(Temp.)
Temp. Scaling
Cryogenic Effects
(Vth, mobility)
Terminal Voltages
Model Equations
Currents, Charges, Noise

FIG. 7A

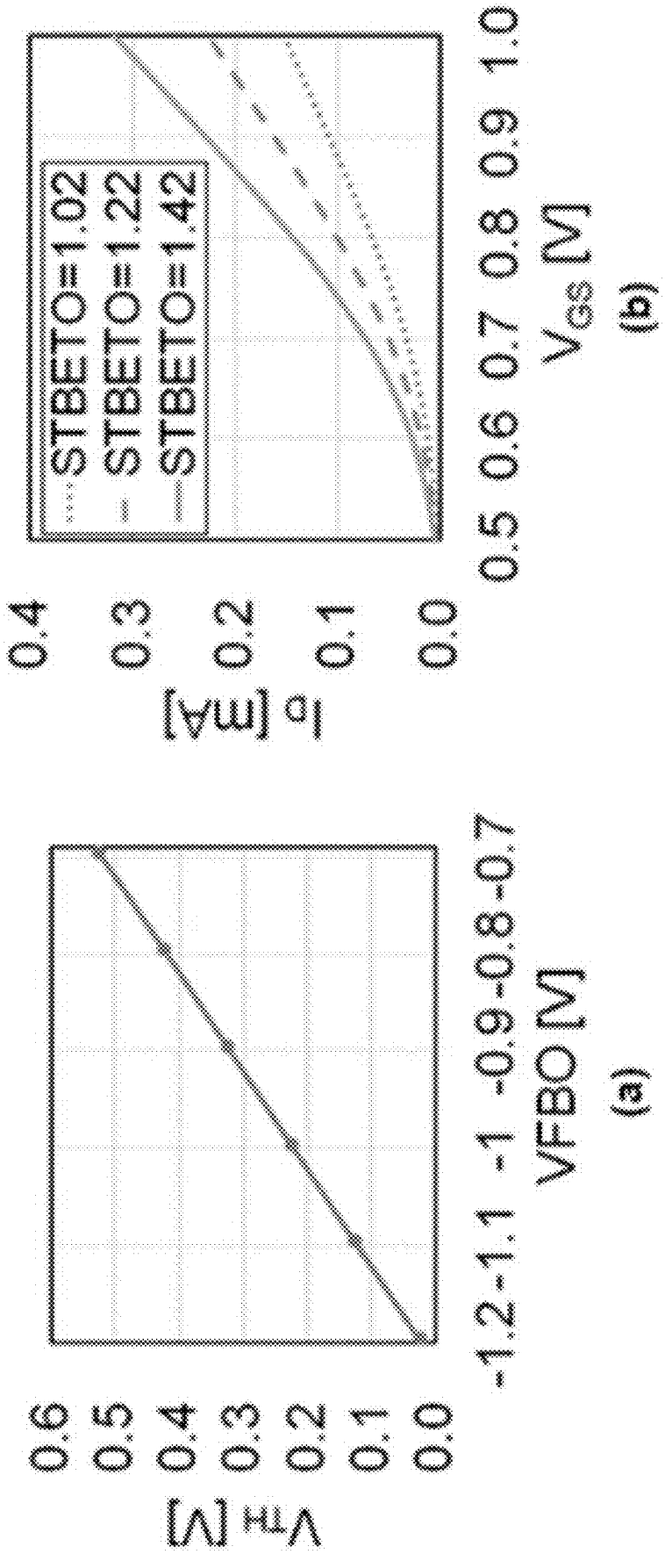

STBETO=1.02
STBETO=1.22
STBETO=1.42
I_D [mA]
0.4
0.3
0.2
0.1
0.0
0.5 0.6 0.7 0.8 0.9 1.0
V_{GS} [V]
(b)
V_{TH} [V]
0.6
0.5
0.4
0.3
0.2
0.1
0.0
-1.2 -1.1 -1 -0.9 -0.8 -0.7
VFBO [V]
(a)

FIG. 7B

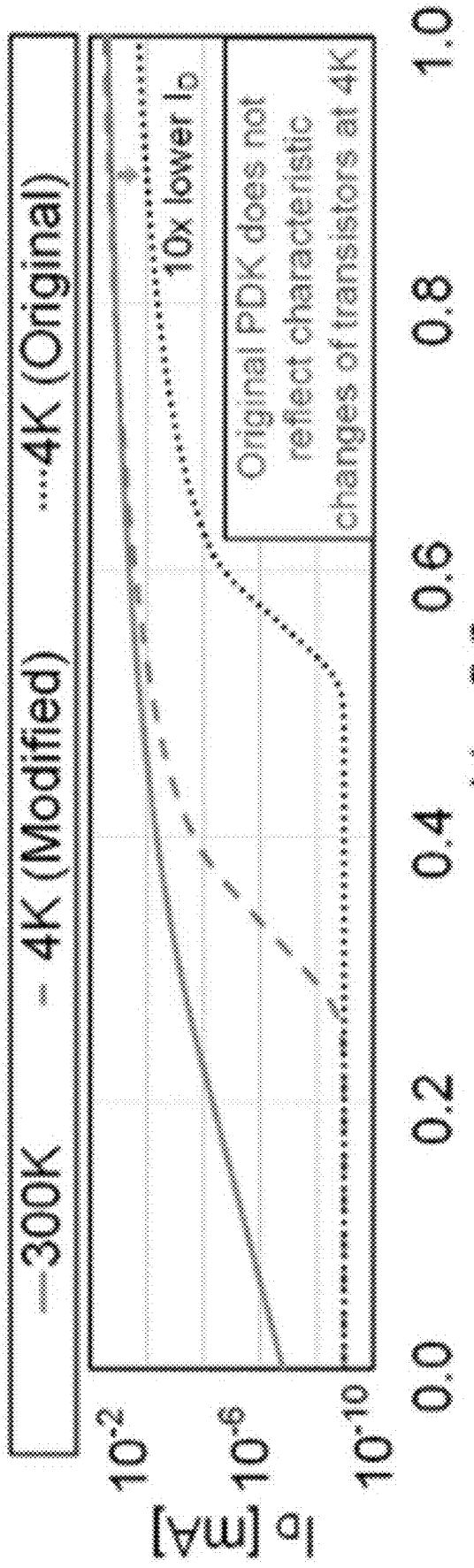

300K
4K (Modified)
4K (Original)
10x lower I_D
Original PDK does not reflect characteristic changes of transistors at 4K
I_D [mA]
10^{-2}
10^{-6}
10^{-10}
0.0
0.2
0.4
0.6
0.8
1.0
V_{GS} [V]

FIG. 7C

METHODS FOR MODELING CMOS TRANSISTOR CHARACTERISTICS IN CRYOGENIC CONDITIONS

CROSS REFERENCE TO RELATED APPLICATION

[0001] The present application claims priority to Korean Patent Application No. 10-2024-0022639, filed Feb. 16, 2024 the entire contents of which are incorporated herein for all purposes by this reference.

BACKGROUND

Field of the Invention

[0002] The present disclosure relates to a system and a method thereof for modeling characteristics of a CMOS transistor in cryogenic conditions on the basis of a PSP model and a method for simulating and correcting characteristics of a CMOS transistor in cryogenic conditions on the basis of a PSP model.

Description of the Related Art

[0003] Quantum computing is a computing method that utilizes quantum phenomena, and has excellence (quantum superiority) that may solve certain types of problems including large-scale data and the like more quickly than classical computing. The basic unit of quantum computing is called a qubit, and although there are some differences according to qubit types and physical implementation methods, a quantum computer operates in a cryogenic range of a few Kelvin or less. The methods of implementing a quantum computer may be largely divided according to the qubit types, the physical implementation methods, and the methods of controlling qubit operations. Among these methods, a method of controlling the qubit operations based on complementary metal-oxide-semiconductor (CMOS) transistors utilizing commercial foundry process is suitable for implementing high-integration, high-scalability quantum computers, but there is a technical difficulty in that the CMOS transistors should also operate in the cryogenic range for qubit control.

[0004] Process design kits (PDKs) provided by foundries are typically based on the results of transistor characteristic measurement over a temperature range of −40 to 125 degrees Celsius, ensuring reliable simulation data over the corresponding temperature range. That is, in cryogenic conditions where quantum computing is performed, the characteristic simulation data is unreliable for complementary metal-oxide-semiconductor (CMOS) transistors.

[0005] There are various previous studies to overcome such a problem, but the reality is that the reliability of characteristic prediction for each transistor size in cryogenic conditions is low.

SUMMARY

[0006] An objective of the present disclosure for solving the technical problem is to provide a method including: extracting global parameters related to characteristic values that vary depending on geometry of a complementary metal-oxide-semiconductor (CMOS) transistor; modeling a characteristic value prediction model by adjusting the global parameters; and predicting the characteristic values of the CMOS transistor in cryogenic conditions.

[0007] In addition, another objective of the present disclosure for solving the technical problem is to provide a method including: extracting parameters related to characteristic values that vary depending on cryogenic conditions of a complementary metal-oxide-semiconductor (CMOS) transistor; modeling a characteristic value prediction model by adjusting the parameters; and predicting the characteristic values of the CMOS transistor in cryogenic conditions.

[0008] According to exemplary embodiments, there is provided a method of modeling characteristics of a CMOS transistor in cryogenic conditions on the basis of a PSP model, the method including: receiving a process design kit (PDK) including device information and process information, which are required for designing and implementing an integrated circuit; extracting at least one parameter for modeling a prediction model for predicting characteristic values of a device included in the integrated circuit in the cryogenic conditions from the PDK on the basis of the PSP model; and modeling the prediction model by adjusting the at least one parameter, so as to predict the characteristic values of the device in the cryogenic conditions.

[0009] Here, the device may be the complementary metal-oxide-semiconductor (CMOS) transistor.

[0010] Here, the model may be the PSP model and may be configured to perform steps including: performing geometry scaling for setting global parameters; modeling a stress model by setting stress parameters; modeling a well proximity effect model by setting well proximity effect parameters; performing temperature scaling by setting local parameters; and predicting the characteristic values of the device by inputting terminal voltages into equations for the model.

[0011] Here, the extracting of the at least one parameter may include: extracting at least one first parameter dependent on geometric properties of the device among the parameters utilized in the PSP model; and extracting at least one second parameter dependent on temperature properties of the device among the parameters utilized in the PSP model.

[0012] Here, the modeling of the prediction model may include: adjusting the first and second parameters so as to be suitable for predicting the characteristic values of the device in the cryogenic conditions; and implementing the performing of the geometry scaling, the modeling of the stress model, the modeling of the well proximity effect model, and the performing of the temperature scaling on the basis of the adjusted first and second parameters.

[0013] Here, the extracting of the at least one parameter may include: extracting device characteristics that are affected and changed by the cryogenic conditions; extracting at least one third parameter dependent on the characteristics among the parameters utilized in the PSP model; adjusting the third parameters so as to be suitable for predicting the characteristic values of the device in the cryogenic conditions; and implementing the performing of the geometry scaling, the modeling of the stress model, the modeling of the well proximity effect model, and the performing of the temperature scaling on the basis of the adjusted third parameters.

[0014] Here, there is provided a computer-readable recording medium, including a program recorded thereon for executing a method for modeling characteristics of a CMOS transistor in cryogenic conditions on the basis of a PSP model.

[0015] According to the exemplary embodiments, there is provided a system for modeling characteristics of a CMOS transistor in cryogenic conditions on the basis of a PSP model, the system including: at least one processor for implementing the system, wherein the at least one processor may be configured to receive a process design kit (PDK) including device information and process information, which are required for designing and implementing an integrated circuit, extract at least one parameter for modeling a prediction model for predicting characteristic values of a device included in the integrated circuit in the cryogenic conditions from the PDK, and model the prediction model by adjusting the at least one parameter, so as to predict the characteristic values of the device in the cryogenic conditions.

[0016] According to the exemplary embodiments, there is provided a method for simulating and correcting characteristics of a CMOS transistor in cryogenic conditions on the basis of a PSP model, the method including: receiving a process design kit (PDK) including device information and process information, which are required for designing and implementing an integrated circuit; extracting at least one parameter for modeling a prediction model capable of simulating and correcting a geometry dependent effect according to changes in characteristic values of a device included in the integrated circuit in the cryogenic conditions from the PDK on the basis of the PSP model; and modeling the prediction model by adjusting the at least one parameter, so as to simulate and correct a geometry dependent effect in the cryogenic conditions.

[0017] According to the present disclosure, the system and the method thereof for modeling the characteristics of the CMOS transistor in cryogenic conditions on the basis of the PSP model and the method for simulating and correcting the characteristics of the CMOS transistor in cryogenic conditions on the basis of the PSP model may extract the global parameters related to the characteristic values that vary depending on the geometry of the complementary metal-oxide-semiconductor (CMOS) transistor, model the characteristic value prediction model by adjusting the global parameters, and predict the characteristic values of the CMOS transistor in cryogenic conditions.

[0018] In addition, according to the present disclosure, the system and the method thereof for modeling the characteristics of the CMOS transistor in cryogenic conditions on the basis of the PSP model and the method for simulating and correcting the characteristics of the CMOS transistor in cryogenic conditions on the basis of the PSP model may extract the parameters related to the characteristic values that vary depending on cryogenic conditions of the complementary metal-oxide-semiconductor (CMOS) transistor, model the characteristic value prediction model by adjusting the parameters, and predict the characteristic values of the CMOS transistor in cryogenic conditions.

[0019] In this way, the embodiment of the present disclosure may not only accurately predict the characteristic values of a CMOS transistor by controlling a smaller number of parameters in cryogenic conditions, but also utilize existing circuit design methods and processes, as they are, on the basis of the existing process design kits (PDKs).

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] FIGS. **1**A, **1**B and **1**C are views illustrating a PSP model and an operation of a CMOS transistor in cryogenic conditions according to an exemplary embodiment of the present disclosure.

[0021] FIG. **2** is a flowchart illustrating a method for modeling characteristics of a CMOS transistor in cryogenic conditions on the basis of a PSP model according to the exemplary embodiment of the present disclosure.

[0022] FIG. **3** is a view illustrating a parameter extraction process and control for the characteristic modeling in cryogenic conditions according to the exemplary embodiment of the present disclosure.

[0023] FIG. **4** is a table illustrating comparisons between other modeling methods and the characteristic modeling method according to the exemplary embodiment of the present disclosure.

[0024] FIGS. **5**A and **5**B are views illustrating an example of experimental results regarding the characteristics of the CMOS transistor according to adjusted parameters according to the exemplary embodiment of the present disclosure.

[0025] FIGS. **6**A, **6**B and **6**C are views illustrating a CMOS modeling method using a ring oscillator and experimental results thereof according to the exemplary embodiment of the present disclosure.

[0026] FIGS. **7**A, **7**B and **7**C are views illustrating a parameter extraction process and control for characteristic modeling in cryogenic conditions according to another exemplary embodiment of the present disclosure.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0027] Hereinafter, various exemplary embodiments of the present disclosure will be described in detail with reference to the accompanying drawings so that those skilled in the art may easily implement the present disclosure. The embodiments of the present disclosure are not limited to the exemplary embodiments described herein and may be embodied in many different forms.

[0028] In order to clearly describe the present disclosure, parts irrelevant to the description are omitted, and the same reference numerals designate the same or similar components throughout the specification. Therefore, the reference symbols described above may also be used in other drawings.

[0029] In addition, the size and thickness of each component shown in the drawings or views are arbitrarily represented for convenience of description, so the embodiments of the present disclosure are not necessarily limited to the illustrated drawings or views. The thickness may be exaggerated to clearly represent multiple layers and areas in the drawings.

[0030] In addition, the expression "same" in the description may mean "substantially the same". That is, this may be meant to be an expression on semantic sameness to the extent that a person with common knowledge may be convinced that it is the same. Other expressions may also be expressions that omit "substantially".

[0031] In addition, when a part is said to "include" or "comprise" a certain component in the description herein, it means that the part may further include or comprise another component, rather than excluding another component unless the context clearly indicates otherwise. As used in the

present specification, the term "~part/unit" refers to a unit for processing at least one function or operation, and may mean, for example, software, an FPGA, or a hardware component. The functions provided by "~unit" may be performed separately by a plurality of components, or may also be integrated with other additional components. The term "~part" or "~unit" is not necessarily limited to software or hardware, and may be configured to reside in an addressable storage medium or may also be configured to operate one or more processors. Hereinafter, the exemplary embodiments of the present disclosure will be described in detail with reference to the drawings.

[0032] FIGS. **1**A to **1**C are views illustrating a PSP model and an operation of a CMOS transistor in cryogenic conditions according to an exemplary embodiment of the present disclosure.

[0033] View (a) in FIG. **1**A shows how threshold voltage V_th changes depending on temperature. Referring to view (a) in FIG. **1**A, it may be seen that the threshold voltage increases as the temperature [K] decreases.

[0034] View (a) in FIG. **1**A shows how mobility μ changes depending on temperature. Referring to view (a) in FIG. **1**A, the mobility tends to increase as the temperature decreases.

[0035] That is, the characteristics of a CMOS transistor change more significantly as temperature therefor changes from a room temperature of 300K to cryogenic conditions (a temperature of 4K or less), meaning that this fact is an important consideration in circuit design based on CMOS transistors for the qubit control.

[0036] Typical existing process design kits (PDKs) ensure reliable simulation data in a temperature range of −40° C. to 125° C. However, referring to view (a) in FIG. **1**B, it may be seen that threshold voltage V_th of the existing process design kits (Original PDKs) increases excessively near at 4K. This causes a difference from actual measured data (Measured data from [2]).

[0037] Referring to view (a) in FIG. **1**B, it may be seen that predicted data (a red dotted line) shows a large deviation at low temperatures (around 4K) compared to the typical existing process design kits (PDKs, a blue solid line). That is, it may be seen that the existing PDK model is unable to accurately predict current Id of a CMOS transistor at cryogenic temperatures.

[0038] Meanwhile, referring to the red dotted line and blue solid line in view (b) in FIG. **1**B together, it may be seen that although the increase (4K Expected) in expected mobility μ should be approximately 30 times or more in values of current, there are large differences between the actual measured data (a blue curve) and the expected data (a red dotted line).

[0039] As described above, the existing process design kits (PDKs) have difficulty in accurately predicting how the CMOS transistor operates at the cryogenic temperatures, and thus, it may be seen that the method of simulating and modeling the cryogenic characteristics, the method enabling correction for this difficulty, is required. In particular, this is especially important when designing CMOS-based controller ICs that should operate at cryogenic conditions.

[0040] FIG. **1**C is a view illustrating a model called a PSP model among CMOS transistor compact models. The PSP model is available for 40 nanometer (nm) or smaller process technology in commercial process design kits (PDKs).

[0041] The PSP model may be composed of several parameters, such as global parameters (Global Parameters), stress parameters (Stress Parameters), well proximity effect parameters (WPE Parameters), and local parameters (Local Parameters).

[0042] The global parameters (Global Parameters) are parameters that determine the fundamental characteristics and operation of a transistor, and may include geometry scaling (Width W and Length L), threshold voltage variation, etc.

[0043] The stress parameters are parameters that model the impact of mechanical stress on the characteristics of the transistor, and may have a significant impact on the reliability and performance of a device.

[0044] The well proximity effect parameters (WPE Parameters) are parameters that indicate well proximity effects and may describe electrical characteristics that change depending on proximity to a well of a transistor.

[0045] The local parameters (Local Parameters) are parameters that indicate changes in the transistor characteristics depending on temperatures, and are applied to a model through temperature scaling (Temp and Scaling).

[0046] Such parameters may ultimately be used in model equations that affect the terminal voltages of a transistor. In this way, the actual behavior of the transistor becomes predictable, and characteristic changes due to temperature changes may also be predicted through a temperature scaling model that considers temperature-dependent changes.

[0047] However, as described above, in the case of such a PSP model of commercial foundry CMOS process PDKs, the characteristic changes of a CMOS transistor at cryogenic temperatures are not properly modeled, and the previous studies to solve this problem also have limitations in applying differences in geometry dependent characteristics according to the size (Width and Length) of the CMOS transistor at the cryogenic temperatures.

[0048] In addition, in the previous studies, a large number of parameters should be adjusted in order to apply the characteristics of a CMOS transistor in cryogenic conditions, so there is a disadvantage in that the number of required measurements and the number of repetitions increase.

[0049] FIG. **2** is a flowchart illustrating a method for modeling characteristics of a CMOS transistor in cryogenic conditions on the basis of a PSP model according to the exemplary embodiment of the present disclosure. FIG. **3** is a view illustrating a parameter extraction process and control for characteristic modeling in cryogenic conditions according to the exemplary embodiment of the present disclosure.

[0050] The method and the system thereof for modeling the characteristics of the CMOS transistor in cryogenic conditions on the basis of the PSP model according to the exemplary embodiment of the present disclosure may be implemented or operated by at least one processor.

[0051] Hereinafter, the following description will be given with reference to FIGS. **2** and **3**.

[0052] In step S**100**, there may be provided a PDK requiring device information and process information, which are required for designing and implementing an integrated circuit.

[0053] In this case, a device may be a complementary metal-oxide-semiconductor (CMOS) transistor.

[0054] In step S**200**, at least one parameter for modeling a model that predicts characteristic values of the device

included in the integrated circuit in cryogenic conditions may be extracted from the PDK on the basis of a PSP model.

[0055] Referring to FIG. **3**, at least one processor may extract at least one parameter (hereinafter referred to as first parameters), which is dependent on geometric properties (e.g., Width W and Length L) of the device, among the parameters utilized in the PSP model.

[0056] For example, the at least one processor may extract at least one first parameter related to a length dependent effect. In order to apply such an effect, the first parameters may be parameters using a "-L" suffix, and are illustrated as STVFBL and STBETL in FIG. **3**, but are not limited thereto.

[0057] Alternatively, the at least one processor may extract at least one first parameter related to an area dependent effect. In order to apply such an effect, the first parameters may be parameters using a "-LW" suffix, and are illustrated as "STVFBLW" in FIG. **3**, but are not limited thereto.

[0058] Alternatively, the at least one processor may extract at least one second parameter related to a temperature dependent effect. In order to apply such an effect, the second parameters may be parameters using a "ST-" prefix, and are illustrated as "STMUEO, STBETO, STVFBL, and STBETL" in FIG. **3**, but are not limited thereto.

[0059] The at least one processor may adjust the at least one first parameter related to the length dependent effect, the at least one first parameter related to the area dependent effect, and the at least one second parameter related to the temperature dependent effect. These parameters may affect steps including: performing geometry scaling, modeling a stress model, modeling a well proximity effect model, performing temperature scaling, and predicting device characteristic values by inputting equations for the models.

[0060] Specifically, the at least one processor is capable of adjusting the first and second parameters so as to be suitable for predicting characteristics of a CMOS transistor at cryogenic temperatures, and may perform the various steps based thereon.

[0061] FIG. **4** is a table illustrating comparisons between other modeling methods and the characteristic modeling method according to the exemplary embodiment of the present disclosure.

[0062] As a result of conducting an experiment according to the system and the method thereof for modeling the characteristics of the CMOS transistor in cryogenic conditions on the basis of the PSP model of the present disclosure, it may be seen that the number of parameters (# of Modified Parameters) required to predict the characteristic values of the CMOS transistor in cryogenic conditions is smaller than that of other existing models (i.e., a model of A. Beckers and a model of R.M. Incandela).

[0063] For example, the model of A. Beckers is not suitable for predicting the characteristics of a CMOS transistor in cryogenic conditions even when the parameters are adjusted. In addition, in the case of the model of R.M. Incandela, it may be seen that the number of parameters, which is nine, required to be adjusted to predict the characteristic values of the CMOS transistor in cryogenic conditions is more than the number of parameters, which is six, required to be adjusted in the system and the method thereof for modeling the characteristics of the CMOS transistor in cryogenic conditions on the basis of the PSP model of the present disclosure.

[0064] In addition, as the result of conducting the experiment in accordance with the system and the method thereof for modeling the characteristics of the CMOS transistor in cryogenic conditions on the basis of the PSP model of the present disclosure, it may be seen that the embodiment of the present disclosure considers geometry dependent effects at the cryogenic temperatures in order to predict the characteristics of the CMOS transistor in cryogenic conditions compared to other existing models (i.e., the models of A. Beckers and R.M. Incandela).

[0065] That is, the embodiment of present disclosure requires a fewer number of parameter modifications when compared to other methods, and may apply a geometry dependent effect and a temperature dependent effect. In this way, it may be seen that the embodiment of the present disclosure is a more concise and efficient modeling method and may be useful for designs using CMOS technology in cryogenic environments.

[0066] FIGS. **5**A and **5**B are views illustrating an example of experimental results regarding the characteristics of the CMOS transistor according to adjusted parameters according to the exemplary embodiment of the present disclosure.

[0067] FIG. **5**A illustrates an experimental result for threshold voltage V_th among characteristic values of a CMOS transistor, and FIG. **5**B illustrates an experimental result for mobility μ among the characteristic values of the CMOS transistor.

[0068] Referring to FIG. **5**A, the at least one processor adjusts the first and second parameters respectively related to geometric properties (e.g., Width W and Length L) and a temperature dependent effect of a device, so that changes in Vth depending on Vds voltage occur for CMOS transistors having various ratios of widths W to lengths L.

[0069] Compared to a graph on the left (for an existing PDK-based simulation result) where threshold voltage Vth is predicted to be excessively high, it may be confirmed that in a graph on the right (in a case of being applied with the embodiment of the present disclosure), threshold voltage Vth is predicted to be similar to an actual measurement result shown in the results of previous study.

[0070] In this way, it may be seen that in a case where the embodiment of the present disclosure is applied to the commercial foundry CMOS process PDKs, the threshold voltage Vth predicted to be excessively high in the simulation assuming cryogenic conditions may be corrected, so that more realistic CMOS transistor characteristics is predictable.

[0071] Referring to FIG. **5**B, the at least one processor adjusts parameters STBETO and STMUEO related to the geometry independent effect affecting mobility μ in cryogenic conditions and adjusts parameters STBETL dependent on length L, thereby showing a change in drain current Id depending on drain voltage Vds at temperatures of 300K and 4K.

[0072] The characteristic values of transistors with W/L ratios different from each other may be compared with each other at 300K and 4K (in cryogenic conditions). Referring to the four graphs in FIG. **5**B, a higher drain current Id is measured in the case of 4K compared to the case of 300K at the same drain voltage Vds. It may be seen that this shows the improved electrical performance of the CMOS transistors at the cryogenic temperatures.

[0073] That is, when the parameters STBETO and STMUEO related to the geometry independent effect and the

parameter STBETL dependent to length L are adjusted, such as a case where W/L ratios are 0.8/0.03, 0.08/0.03, 0.8/0.3, and 0.08/0.3, it may be seen that it is suitable to predict the characteristic values of the CMOS transistors in cryogenic conditions

[0074] FIGS. **6**A to **6**C are views illustrating a CMOS modeling method using a ring oscillator and experimental results thereof according to the exemplary embodiment of the present disclosure.

[0075] FIG. **6**A is a view illustrating a 23-stage ring oscillator (RO) designed on the basis of a CMOS transistor.

[0076] FIG. **6**A shows experiment results conducted on the 23-stage ring oscillator at 300K (room temperature) and 4K (cryogenic conditions) in two divided cases: a case of simulation using typical process design kits (PDKs, Original); and a case of simulation using a model corrected according to the system and the method thereof for modeling the characteristics of the CMOS transistor in the cryogenic conditions on the basis of the PSP model according to the present disclosure (Modified PDK).

[0077] Referring to FIG. **6**B, the two graphs on the left show oscillation frequencies according to VDD at W/L ratios different from each other. In the case where the simulation is performed at 4K (the cryogenic conditions) using the typical process design kits (PDKs, Original), it may be confirmed that the ring oscillator (RO) does not oscillate. This may be due to the threshold voltage Vth of a transistor being predicted excessively high in an existing PDK.

[0078] The two graphs on the right in FIG. **6**B are the experimental results of the simulation (red lines in the graphs) using the typical process design kits (PDKs, Original) at 300K (the room temperature) and simulation (green lines in the graphs) using the typical process design kits (PDKs, Original) at 4K (the cryogenic conditions) in FIG. **6**A, and the simulation (blue lines in the graphs) using the embodiment of the present disclosure at 4K (the cryogenic conditions). In the case where the simulation is performed at 4K (the cryogenic conditions) using the typical process design kits (PDKs, Original), it may be confirmed that the oscillation frequencies of the ring oscillator (RO) are predicted to be excessively low. This may be due to the existing PDK that predicts the threshold voltage Vth of the transistor too high or predict the mobility too low.

[0079] Meanwhile, in the case of applying the geometry dependent effects according to the present disclosure, it may be seen that the ring oscillator (RO) oscillates at 4K (the cryogenic conditions) (indicated in the blue lines in the graphs), and this may solve problems that may occur when simulation is performed by using only the existing typical process design kits (PDKs, Original).

[0080] Referring to the measurement results in FIG. **6**C, which are the results of the previous studies, it may be seen that the frequency increases as the temperature decreases. That is, since the frequency is relatively high at low temperatures, it may be seen that the lower the temperature, the faster the speed of the oscillator. It may be confirmed that the simulation method according to the present disclosure allows that matching is performed well with actual measurement data.

[0081] FIGS. **7**A to **7**C are views illustrating a parameter extraction process and control for characteristic modeling in cryogenic conditions according to another exemplary embodiment of the present disclosure.

[0082] Referring to FIG. **7**A, the at least one processor may extract at least one parameter (hereinafter referred to as third parameters), which are dependent on cryogenic effects, among the parameters utilized in the PSP model.

[0083] For example, the at least one processor may extract at least one third parameter (VFB0 in FIGS. **7**A to **7**C) related to threshold voltage V_th. The at least one processor may extract at least one third parameter (STBETO in FIGS. **7**A to **7**C) related to mobility μ.

[0084] The at least one processor may adjust the at least one third parameter (VFB0 and STBETO in FIGS. **7**A to **7**C) related to the cryogenic effects, and this may affect the performing of the temperature scaling.

[0085] Specifically, the at least one processor is capable of adjusting the third parameters so as to be suitable for predicting characteristics of a CMOS transistor in cryogenic conditions, and may perform the various steps based thereon.

[0086] Referring to view (a) in FIG. **7**B, threshold voltage Vth may be linearly changed by adjusting the VFBO parameter. Referring to view (b) in FIG. **7**B, it may be seen that drain current I_D increases as the STBETO parameter increases. That is, the higher the mobility, the higher the drain current flows at the same gate voltage V_GS.

[0087] Referring to FIG. **7**C, there are shown the results (4K, Original) of simulation using existing commercial process design kits (PDKs) at 4K (cryogenic conditions) and the results (4K, Modified) of simulation according to the present disclosure.

[0088] It may be seen that at 4K (the cryogenic conditions), the existing commercial process design kits (PDKs) are not applied with the characteristic changes of the CMOS transistor in the cryogenic conditions, whereby the threshold voltage Vth is predicted to be excessively high and the mobility μ is predicted to be excessively low.

[0089] In contrast, it may be seen that the results (4K, Modified) of the simulation according to the present disclosure are relatively well applied with the characteristic changes of the CMOS transistor in the cryogenic conditions.

[0090] As described above in FIGS. **7**A to **7**C, compared to the exemplary embodiment of the present disclosure described above in FIG. **4**, another exemplary embodiment of the present disclosure has a smaller number of parameters (# of Modified Parameters) required to predict the characteristic values of a CMOS transistor in cryogenic conditions.

[0091] That is, compared to FIG. **4**, there are effects shown in FIGS. **7**A to **7**C that the changes in the characteristic values of the CMOS transistor in cryogenic conditions may be relatively accurately simulated by adjusting only two parameters (VFB0 and STBETO).

[0092] The drawings referenced so far and the detailed description of the disclosure are merely illustrative of the present disclosure, which are only used for the purpose of describing the present disclosure, and it is not used to limit the meaning or the scope of the present disclosure described in the claims. Accordingly, those skilled in the art will appreciate that various modifications and other equivalent embodiments are possible. Therefore, the true technical protection scope of the present disclosure will be defined by the technical idea of the appended patent claims.

[0093] The exemplary embodiments described above may be implemented as a hardware component, a software component, and/or a combination of the hardware component and the software component. For example, devices and

components described in the exemplary embodiments may be implemented by using one or more general purpose computers or special purpose computers, including, for example, a processor, a controller, an arithmetic logic unit (ALU), a digital signal processor, a microcomputer, a field programmable gate array (FPGA), programmable logic unit (PLU), microprocessor, or any other device capable of executing and responding to instructions.

[0094] The processing device may execute an operating system (OS) and one or more software applications running on the operating system. In addition, the processing device may also access, store, operate, process, and generate data in response to the execution of the software. Sometimes it is described such that one processing device is used for convenience of understanding, but those skilled in the art will recognize that the processing device may include a plurality of processing elements and/or a plurality of types of processing elements.

[0095] For example, the processing device may include a plurality of processors, or include one processor and one controller. In addition, other processing configurations with such as parallel processors are also possible. The software may include a computer program, a code, an instruction, or a combination of one or more thereof, and may be configured to enable the processing device to operate as desired or to instruct the processing device independently or collectively.

[0096] In order to be interpreted by or to provide instructions or data to the processing device, software and/or data may be embodied in any type of machine, component, physical device, virtual equipment, computer storage medium, or computer storage device. Software may be distributed over networked computer systems, and stored or executed in a distributed manner. Software and data may be stored in one or more computer-readable recording media.

[0097] The methods according to the exemplary embodiments may be implemented in the form of program instructions that may be executed through various computer means, and may be recorded in a computer-readable media. The computer-readable media may include program instructions, data files, data structures, and the like alone or in combination thereof. The program instructions recorded on the media may be designed and configured specifically for the exemplary embodiments or may be publicly known and available to those skilled in the art regarding computer software.

[0098] Examples of the computer-readable recording media include: magnetic media, such as a hard disk, a floppy disk, and a magnetic tape; optical media, such as a compact disc read-only memory (CD-ROM), a digital versatile disc (DVD), etc.; and hardware devices specially configured to store and perform program instructions, for example, a read-only memory (ROM), a random access memory (RAM), a flash memory, etc. Examples of the computer instructions include not only machine language code generated by a compiler, but also high-level language code executable by a computer using an interpreter or the like. The hardware device described above may be configured to operate by one or more software modules to perform the operations of the exemplary embodiments, and vice versa.

[0099] As described above, although the exemplary embodiments have been described with reference to the limited exemplary embodiments and drawings, various modifications and variations are possible from the above description by those skilled in the art. For example, appropriate results may be achieved even when the described techniques are performed in a different order than that of the described method, and/or the described components of the system, structure, device, circuit, and the like are coupled to each other or combined in a different form than the described method, or replaced or substituted by other components or equivalents. Therefore, other implementation, other exemplary embodiments, and equivalents to the claims also fall within the scope of the following claims.

What is claimed is:

1. A method of modeling characteristics of a CMOS transistor in cryogenic conditions on the basis of a PSP model, the method comprising:

receiving a process design kit (PDK) comprising device information and process information, which are required for designing and implementing an integrated circuit;

extracting at least one parameter for modeling a prediction model for predicting characteristic values of a device comprised in the integrated circuit in the cryogenic conditions from the PDK on the basis of the PSP model; and

modeling the prediction model by adjusting the at least one parameter, so as to predict the characteristic values of the device in the cryogenic conditions.

2. The method of claim **1**, wherein the device is the complementary metal-oxide-semiconductor (CMOS) transistor.

3. The method of claim **1**, wherein the model is the PSP model and is configured to perform steps comprising:

performing geometry scaling for setting global parameters;

modeling a stress model by setting stress parameters;

modeling a well proximity effect model by setting well proximity effect parameters;

performing temperature scaling by setting local parameters; and

predicting the characteristic values of the device by inputting terminal voltages into equations for the model.

4. The method of claim **3**, wherein the extracting of the at least one parameter comprises:

extracting at least one first parameter dependent on geometric properties of the device among the parameters utilized in the PSP model; and

extracting at least one second parameter dependent on temperature properties of the device among the parameters utilized in the PSP model.

5. The method of claim **4**, wherein the modeling of the prediction model comprises:

adjusting the first and second parameters so as to be suitable for predicting the characteristic values of the device in the cryogenic conditions; and

implementing the performing of the geometry scaling, the modeling of the stress model, the modeling of the well proximity effect model, and the performing of the temperature scaling on the basis of the adjusted first and second parameters.

6. The method of claim **3**, wherein the extracting of the at least one parameter comprises:

extracting device characteristics that are affected and changed by the cryogenic conditions;

extracting at least one third parameter dependent on the characteristics among the parameters utilized in the PSP model;

adjusting the third parameters so as to be suitable for predicting the characteristic values of the device in the cryogenic conditions; and

implementing the performing of the geometry scaling, the modeling of the stress model, the modeling of the well proximity effect model, and the performing of the temperature scaling on the basis of the adjusted third parameters.

7. A system for modeling characteristics of a CMOS transistor in cryogenic conditions on the basis of a PSP model, the system comprising:

at least one processor for implementing the system,

wherein the at least one processor is configured to receive a process design kit (PDK) comprising device information and process information, which are required for designing and implementing an integrated circuit, extract at least one parameter for modeling a prediction model for predicting characteristic values of a device comprised in the integrated circuit in the cryogenic conditions from the PDK, and model the prediction model by adjusting the at least one parameter, so as to predict the characteristic values of the device in the cryogenic conditions.

8. A computer-readable recording medium, comprising:

a program recorded thereon for executing a method for modeling characteristics of a CMOS transistor in cryogenic conditions on the basis of a PSP model of claim **1**.

9. A method for simulating and correcting characteristics of a CMOS transistor in cryogenic conditions on the basis of a PSP model, the method comprising:

receiving a process design kit (PDK) comprising device information and process information, which are required for designing and implementing an integrated circuit;

extracting at least one parameter for modeling a prediction model capable of simulating and correcting a geometry dependent effect according to changes in characteristic values of a device comprised in the integrated circuit in the cryogenic conditions from the PDK on the basis of the PSP model; and

modeling the prediction model by adjusting the at least one parameter, so as to simulate and correct a geometry dependent effect in the cryogenic conditions.

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