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United States Patent	12394242
Kind Code	B2
Date of Patent	August 19, 2025
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Fingerprint sensor device and method

Abstract

A fingerprint sensor package and method are provided. Embodiments include a sensor and a sensor surface material encapsulated within the fingerprint sensor package. An array of electrodes of the sensor are electrically connected using through vias that are located either in the sensor, in connection blocks separated from the sensor, or through connection blocks, or else connected through other connections such as wire bonds. A high voltage die is attached in order to increase the sensitivity of the fingerprint sensor.

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Appl. No.: **18/343036**

Filed: **June 28, 2023**

Prior Publication Data

Document Identifier	Publication Date
US 20230343133 A1	Oct. 26, 2023

Related U.S. Application Data

continuation parent-doc US 17522610 20211109 US 11727714 child-doc US 18343036
continuation parent-doc US 15898871 20180219 US 10268872 20190423 child-doc US 16390704
continuation parent-doc US 15053357 20160225 US 9898645 20180220 child-doc US 15898871

division parent-doc US 16390704 20190422 US 11194990 20211207 child-doc US 17522610 us-provisional-application US 62256237 20151117

Publication Classification

Int. Cl.: **G06V40/13** (20220101); **H01L21/56** (20060101); **H01L23/00** (20060101); **H01L23/498** (20060101)

U.S. Cl.:

CPC **G06V40/1329** (20220101); **H01L21/561** (20130101); **H01L23/49827** (20130101); **H01L24/19** (20130101); H01L21/568 (20130101); H01L24/13 (20130101); H01L24/16 (20130101); H01L24/32 (20130101); H01L24/45 (20130101); H01L24/48 (20130101); H01L24/73 (20130101); H01L24/81 (20130101); H01L2224/0401 (20130101); H01L2224/04105 (20130101); H01L2224/12105 (20130101); H01L2224/13111 (20130101); H01L2224/16227 (20130101); H01L2224/18 (20130101); H01L2224/32225 (20130101); H01L2224/45144 (20130101); H01L2224/48091 (20130101); H01L2224/48227 (20130101); H01L2224/73204 (20130101); H01L2224/73267 (20130101); H01L2224/81005 (20130101); H01L2224/81024 (20130101); H01L2224/81815 (20130101); H01L2224/81911 (20130101); H01L2224/83005 (20130101); H01L2224/85005 (20130101); H01L2224/92125 (20130101); H01L2224/92244 (20130101); H01L2224/97 (20130101); H01L2924/15311 (20130101); H01L2224/48091 (20130101); H01L2924/00014 (20130101); H01L2224/97 (20130101); H01L2224/83 (20130101); H01L2224/97 (20130101); H01L2224/81 (20130101); H01L2224/97 (20130101); H01L2224/85 (20130101)

Field of Classification Search

CPC: G06V (40/1329); G06V (40/13); H01L (21/561); H01L (21/568); H01L (21/50); H01L (24/19); H01L (23/49827); H01L (25/16)

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATIONS (1) This application is a continuation of U.S. patent application Ser. No. 17/522,610 filed Nov. 9, 2021, entitled “Fingerprint Sensor Device and Method,” which is a divisional of U.S. patent application Ser. No. 16/390,704 filed on Apr. 22, 2019, entitled “Fingerprint Sensor Device and Method,” now U.S. Pat. No. 11,194,990, issued on Dec. 7, 2021, which is a continuation of U.S. patent application Ser. No. 15/898,871 filed on Feb. 19, 2018, entitled “Fingerprint Sensor Device and Method,” now U.S. Pat. No. 10,268,872, issued on Apr. 23, 2019, which is a continuation of U.S. patent application Ser. No. 15/053,357, filed on Feb. 25, 2016, now U.S. Pat. No. 9,898,645, issued on Feb. 20, 2018, entitled “Fingerprint Sensor Device and Method,” which application claims priority to and the benefit of U.S. Provisional Application No. 62/256,237, filed on Nov. 17, 2015, entitled “Low Cost Interconnect of Fingerprint Sensor Chip in INFO Structure,” which applications are hereby incorporated herein by reference in their entirety.

BACKGROUND
(1) As user devices become smaller and more portable, it has become easier for people with ill intentions to steal user devices. When such devices bear sensitive information of the user, thieves may be able to access such information unless barriers have been placed into the user device. Once such barrier is a fingerprint sensor which can be used to read the fingerprint of the person attempting to access the device and, if the fingerprint is not the same fingerprint of the user, access may be denied.
(2) However, as user devices such as cell phones become smaller, there is a pressure on each of the individual components within the user device to also see a concurrent reduction in size. As such, there is a pressure to reduce the size of the fingerprint package that contains the fingerprint sensor without seeing a reduction in performance. As such, improvements are needed to see the desired reduction in size.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
(1) Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.
(2) FIGS. **1**A-**1**E illustrate a fingerprint sensor package which uses through vias located within a sensor in accordance with some embodiments.
(3) FIGS. **2**A-**2**D illustrate an embodiment which uses through vias separated from the sensor in accordance with some embodiments.
(4) FIGS. **3**A-**3**B illustrate an embodiment which uses wire bonds in accordance with some embodiments.
(5) FIGS. **4**A-**4**D illustrate an embodiment which utilizes connection blocks in accordance with some embodiments.
DETAILED DESCRIPTION
(6) The following disclosure provides many different embodiments, or examples, for implementing different features of the invention. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in

direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

(7) Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper” and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

(8) Embodiments will now be described with respect to a fingerprint sensor in a system in package solution or else an integrated fan out (InFO) structure. However, embodiments may be used in any suitable package.

(9) With reference now to FIG. **1**A, there is illustrated a carrier substrate **101** to which a sensor surface material **103** and a sensor **105** are attached. The carrier substrate **101** comprises, for example, silicon based materials, such as glass or silicon oxide, or other materials, such as aluminum oxide, combinations of any of these materials, or the like. The carrier substrate **101** is planar in order to accommodate an attachment of devices such as the sensor surface material **103** and the sensor **105**.

(10) To help secure the sensor surface material **103** to the carrier substrate **101**, a protective layer **107** and an adhesive layer **109** may be placed onto the carrier substrate **101** prior to the placement of the sensor surface material **103**. In an embodiment the protective layer **107** may be a light-to-heat conversion (LTHC) layer, although any suitable material may be utilized. The protective layer **107** may be dispensed as a liquid and cured, may be a laminate film laminated onto the carrier substrate **101**, or the like, depending upon the material chosen.

(11) The adhesive layer **109** may be placed over the protective layer **107** in order to assist in the attachment of the sensor surface material **103** to the carrier substrate **101**. In an embodiment the adhesive layer **109** is a die attached film (DAF), such as an epoxy resin, a phenol resin, acrylic rubber, silica filler, or a combination thereof, and is applied using a lamination technique. However, any other suitable material and method of formation may be utilized.

(12) The sensor surface material **103** is placed in contact with the adhesive layer **109** and is used to separate the sensor **105** from an overlying finger (not separately illustrated in FIG. **1**A). In an embodiment the sensor surface material **103** is a material such as sapphire or glass that allows for the measurement of capacitive changes between the sensor **105** and an overlying finger to determine contours of a fingerprint on the finger. In an embodiment the sensor surface material **103** may have a first width W.sub.1 of between about 5 mm and about 15 mm, such as about 10 mm, and may be placed using a physical placing process. Additionally, the sensor surface material **103** may have a first thickness T.sub.1 of between about 50 μm and about 1000 μm, such as about 100 μm.

(13) FIG. **1**B illustrates a close up view of the sensor **105** that is placed in conjunction with sensor surface material **103** in FIG. **1**A. In an embodiment the sensor **105** comprises a semiconductor substrate **111** with a face side **113** and a back side **115**, an array of electrodes **120** located adjacent to the face side **113**, and first through substrate vias (TSVs) **117** connecting the array of electrodes **120** from the face side **113** to the back side **115**. In an embodiment the semiconductor substrate **111** may comprise bulk silicon, doped or undoped, or an active layer of a silicon-on-insulator (SOI) substrate. Generally, an SOI substrate comprises a layer of a semiconductor material such as silicon, germanium, silicon germanium, SOI, silicon germanium on insulator (SGOI), or combinations thereof. Other substrates that may be used include multi-layered substrates, gradient substrates, or hybrid orientation substrates.

(14) Additionally, while not separately illustrated in FIG. **1**B, the sensor **105** may also comprise

active devices and metallization layers in order to control and receive the input of signals from the array of electrodes **120** or else otherwise control the functionality and eventual output of the sensor **105**. In an embodiment the active devices for the sensor **105** comprise a wide variety of active devices and passive devices such as capacitors, resistors, inductors and the like that may be used to generate the desired structural and functional requirements of the design for the sensor **105**. The first active devices may be formed using any suitable methods either within or else on the semiconductor substrate **111**.

(15) The metallization layers are formed over the semiconductor substrate **111** and the active devices of the sensor **105** and are designed to connect the various active devices to form functional circuitry. In an embodiment the metallization layers are formed of alternating layers of dielectric and conductive material and may be formed through any suitable process (such as deposition, damascene, dual damascene, etc.). In an embodiment there may be four layers of metallization separated from the second semiconductor substrate by at least one interlayer dielectric layer (ILD), but the precise number of metallization layers is dependent upon the design of the sensor **105**.

(16) The array of electrodes **120** is electrically connected to the metallization layers of the sensor **105** and are used to measure the difference in capacitance between different areas of an overlying finger in order to measure the fingerprint. In an embodiment the array of electrodes **120** comprises a conductive material such as aluminum or copper, and is formed using, e.g., a deposition and patterning process whereby a blanket layer of conductive material is deposited using a process such as CVD, PVD, ALD, or the like, and the blanket layer of material is then patterned using a photolithographic masking and etching process. However, any suitable material or method of manufacture may be utilized to form the array of electrodes **120**.

(17) Once the array of electrodes **120** has been formed, a protective layer **122** is formed over the array of electrodes **120** in order to protect the array of electrodes **120** from defects caused by further processing or usage. In an embodiment the protective layer **122** may be a protective material such as polybenzoxazole (PBO) or polyimide (PI), silicon oxide, silicon nitride, silicon oxynitride, benzocyclobutene (BCB), or any other suitable protective material. The protective layer **122** may be formed using a method such as a spin-on process, a deposition process (e.g., chemical vapor deposition), or other suitable process based upon the chosen material, and may be formed to a thickness of between about 1 μm and about 100 μm, such as about 20 μm.

(18) Additionally, while the formation of the array of electrodes **120** and the protective layer **122** has been described using a blanket deposition followed by a subsequent patterning and protection, this process is merely intended to be illustrative and is not intended to be limiting. Rather, any suitable process of manufacturing the array of electrodes **120**, such as using a damascene or dual damascene process, may also be used. All such processes are fully intended to be included within the scope of the embodiments.

(19) The first TSVs **117** are utilized to electrically connect the array of electrodes **120** and the metallization layers which are located on the face side **113** of the sensor **105** to the back side **115** of the sensor **105**. The first TSVs **117** may be formed through the semiconductor substrate **111** prior to the sensor being adhered or bonded to the sensor surface material **103**, and the process for forming them may start by initially applying and developing a suitable photoresist to the semiconductor substrate **111** prior to the formation of the metallization layers, and then etching the semiconductor substrate **111** to generate TSV openings. The openings for the first TSVs **117** at this stage may be formed so as to extend into the semiconductor substrate **111** to a depth at least greater than the eventual desired height of the finished semiconductor substrate **111**.

(20) Once the openings for the first TSVs **117** have been formed, the openings for the first TSVs **117** may be filled with, e.g., a barrier layer and a conductive material. The barrier layer may comprise a conductive material such as titanium nitride, although other materials, such as tantalum nitride, titanium, a dielectric, or the like may be utilized. The barrier layer may be formed using a CVD process, such as PECVD. However, other processes, such as sputtering or metal organic

chemical vapor deposition (MOCVD), may be used. The barrier layer may be formed so as to contour to the underlying shape of the opening for the first TSVs **117**.

(21) The conductive material may comprise copper, although other suitable materials such as aluminum, alloys, doped polysilicon, combinations thereof, and the like, may be utilized. The conductive material may be formed by depositing a seed layer and then electroplating copper onto the seed layer, filling and overfilling the openings for the first TSVs **117**. Once the openings for the first TSVs **117** have been filled, excess barrier layer and excess conductive material outside of the openings for the first TSVs **117** may be removed through a grinding process such as chemical mechanical polishing (CMP), although any suitable removal process may be used.

(22) Once the conductive material is within the openings for the first TSVs **117**, a thinning of the semiconductor substrate **111** may be performed in order to expose the openings for the first TSVs **117** and form the first TSVs **117** from the conductive material that extends through the semiconductor substrate **111**. In an embodiment, the thinning of the semiconductor substrate **111** may be performed by a planarization process such as CMP or etching, leaving the first TSVs **117** planar with the semiconductor substrate **111**.

(23) However, as one of ordinary skill in the art will recognize, the above described process for forming the first TSVs **117** is merely one method of forming the first TSVs **117**, and other methods are also fully intended to be included within the scope of the embodiments. For example, forming the openings for the first TSVs **117**, filling the openings for the first TSVs **117** with a dielectric material, thinning the semiconductor substrate **111** to expose the dielectric material, removing the dielectric material, and filling the openings for the first TSVs **117** with a conductor may also be used. This and all other suitable methods for forming the first TSVs **117** into the semiconductor substrate **111** are fully intended to be included within the scope of the embodiments.

(24) On the back side **115** of the sensor **105**, and in electrical connection with the first TSVs **117**, optional contact pads **119** are formed to provide an electrical connection to a subsequently formed first redistribution layer **131** (not illustrated in FIG. **1**A or **1**B but illustrated and described below with respect to FIG. **1**C). In an embodiment the contact pads **119** are formed of a conductive material such as aluminum, although other suitable materials, such as copper, tungsten, or the like, may be utilized. The contact pads **119** may be formed using a process such as CVD or PVD, although other suitable materials and methods may be utilized. Once the material for the contact pads **119** has been deposited, the material may be shaped into the contact pads **119** using, e.g., a photolithographic masking and etching process.

(25) Once the contact pads **119** have been formed, a first protective layer **123** may be placed and patterned. In an embodiment the first protective layer **123** may be a protective material such as polybenzoxazole (PBO) or polyimide (PI), silicon oxide, silicon nitride, silicon oxynitride, benzocyclobutene (BCB), or any other suitable protective material. The first protective layer **123** may be formed using a method such as a spin-on process, a deposition process (e.g., chemical vapor deposition), or other suitable process based upon the chosen material, and may be formed to a thickness of between about 1 μm and about wo μm, such as about 20 μm.

(26) Once formed the first protective layer **123** is patterned to form openings and expose the contact pads **119**. In an embodiment the first protective layer **123** may be patterned using, e.g., a photolithographic masking and etching process. In such a process, a first photoresist (not individually illustrated in FIG. **1**B) is applied to the first protective layer **123** and then exposed to a patterned light source. The light source will impinge upon the first photoresist and induce a change in a property of the first photoresist, which is then utilized to selectively remove either the exposed portion or the unexposed portion and expose the first protective layer **123**. The first photoresist is then utilized as a mask during, e.g., an etching process which removes portions of the first protective layer **123** to expose the contact pads **119**. Once the first protective layer **123** has been patterned, the first photoresist may be removed using, e.g., an ashing process.

(27) In another embodiment the first protective layer **123** may be thinned in order to expose the

contact pads **119**. In this embodiment a planarization process such as a chemical mechanical polishing process, whereby chemicals and abrasives are applied to the first protective layer **123** while a polishing pad grinds away material, may be utilized to remove the material of the first protective layer **123** from over the contact pads **119**, thereby exposing the contact pads **119** while also planarizing the first protective layer **123** with the contact pads **119**.

(28) Returning now to FIG. **1**A, the sensor **105** may be placed onto and adhered to the sensor surface material **103** with the assistance of a first glue layer **127**. In an embodiment the first glue layer **127** is a color film or adhesive glue, such as an epoxy resin, a phenol resin, acrylic rubber, silica filler, or a combination thereof, and is applied using a lamination or spin coating technique. However, any other suitable material and method of formation may be utilized. The first glue layer **127** may be applied to have a second thickness T.sub.2 of between about 2 μm and about 20 μm, such as about 10 μm.

(29) Once the first glue layer **127** has been applied to either the sensor **105** or to the sensor surface material **103**, the sensor **105** may be adhered to the first glue layer **127** or the sensor surface material **103** using, e.g., a pick-and-place process, whereby the sensor **105** is aligned with the desired position and then lowered such that the first glue layer **127** is in contact with both the sensor **105** and the sensor surface material **103**. Additionally, in an embodiment the sensor **105** may have a second width W.sub.2 that is less than the first width W.sub.1 (of the sensor surface material **103**). For example, the sensor **105** may have the second width W.sub.2 of between about 5 mm and about 10 mm, such as about 7 mm. The sensor **105** may also have a third thickness T.sub.3 of between about 50 μm and about 250 μm, such as about 100 μm. However, any suitable width or other dimension may be used.

(30) Once the sensor **105** has been placed and adhered onto the sensor surface material **103**, the sensor **105** and the sensor surface material **103** are encapsulated with an encapsulant **125**. In an embodiment the encapsulant **125** may be a molding compound and may be placed using a molding device (not illustrated in FIG. **1**C). For example, the sensor surface material **103** and the sensor **105** may be placed within a cavity of the molding device, and the cavity may be hermetically sealed. The encapsulant **125** may be placed within the cavity either before the cavity is hermetically sealed or else may be injected into the cavity through an injection port. In an embodiment the encapsulant **125** may be a molding compound resin such as polyimide, PPS, PEEK, PES, a heat resistant crystal resin, combinations of these, or the like.

(31) Once the encapsulant **125** has been placed into the cavity such that the encapsulant **125** encapsulates the region around the sensor surface material **103** and the sensor **105**, the encapsulant **125** may be cured in order to harden the encapsulant **125** for optimum protection. While the exact curing process is dependent at least in part on the particular material chosen for the encapsulant **125**, in an embodiment in which molding compound is chosen as the encapsulant **125**, the curing could occur through a process such as heating the encapsulant **125** to between about 100° C. and about 130° C., such as about 125° C. for about 60 sec to about 3000 sec, such as about 600 sec. Additionally, initiators and/or catalysts may be included within the encapsulant **125** to better control the curing process.

(32) However, as one having ordinary skill in the art will recognize, the curing process described above is merely an exemplary process and is not meant to limit the current embodiments. Other curing processes, such as irradiation or even allowing the encapsulant **125** to harden at ambient temperature, may be used. Any suitable curing process may be used, and all such processes are fully intended to be included within the scope of the embodiments discussed herein.

(33) FIG. **1**A additionally illustrates a thinning of the encapsulant **125** in order to expose the contact pads **119** of the sensor **105**. In an embodiment the thinning may be performed, e.g., using a mechanical grinding or chemical mechanical polishing (CMP) process whereby chemical etchants and abrasives are utilized to react and grind away the encapsulant **125**. The encapsulant **125** may be thinned until the contact pads **119** have been exposed.

(34) However, while the CMP process described above is presented as one illustrative embodiment, it is not intended to be limiting to the embodiments. Any other suitable removal process may be used to encapsulate the sensor **105** while exposing the contact pads **119**. For example, a chemical etch or a series of chemical etches may be utilized, or an encapsulation process that does not cover the contact pads **119** may be utilized. These processes and any other suitable process may be utilized to thin the encapsulant **125**, and all such processes are fully intended to be included within the scope of the embodiments.

(35) FIG. **1**C illustrates a formation of first redistribution layers **131** over the back side **115** of the sensor **105** and the encapsulant **125**. In an embodiment the first redistribution layers **131** comprises a series of conductive layers **133** (such as two conductive layers) embedded within a series of dielectric layer **135** (such as three dielectric layers). In an embodiment, a first one of the series of dielectric layer **135** is formed over the encapsulant **125** and the contact pads **119** in order to provide protection and isolation for the encapsulant **125** and the contact pads **119** and the other underlying structures. In an embodiment the first one of the series of dielectric layer **135** may be a material such as polybenzoxazole (PBO), although any suitable material, such as polyimide or a polyimide derivative, may be utilized. The first one of the series of dielectric layers **135** may be placed using, e.g., a spin-coating process, although any suitable method may be used.

(36) After the first one of the series of dielectric layer **135** has been formed, openings may be made through the first one of the series of dielectric layers **135** by removing portions of the first one of the series of dielectric layers **135** to expose at least a portion of the contact pads **119** underlying the first one of the series of dielectric layer **135**. The openings allow for contact between the contact pads **119** and the subsequently formed series of conductive layers **133**. The openings may be formed using a suitable photolithographic mask and etching process, although any suitable process to expose the underlying contact pads **119** may be used.

(37) In another embodiment in which the contact pads **119** are not formed in connection with the first TSVs **117**, the first one of the series of dielectric layers **135** may be formed over the encapsulant **125** and directly over and in contact with the first TSVs **117**. In this embodiment, rather than patterning the first one of the series of dielectric layers **135** to expose the contact pad **119** (because it is not present), the first one of the series of dielectric layers **135** are patterned to expose portions of the first TSVs **117**. This and all other embodiments of electrically connecting the first TSVs **117** to the first redistribution layers **131** are fully intended to be included within the scope of the embodiments.

(38) Once the first one of the series of dielectric layers **135** has been formed and patterned, a first one of the series of conductive layers **133** is formed over the first one of the series of dielectric layers **135** and through the openings formed within the first one of the series of dielectric layers **135** in order to make electrical connection with the first TSVs **117** (either directly or through intervening structures such as the optional contact pads **119**). In an embodiment the first one of the series of conductive layers **133** may be formed by initially forming a seed layer (not shown) of a titanium copper alloy through a suitable formation process such as CVD or sputtering. A photoresist (also not shown) may then be formed to cover the seed layer, and the photoresist may then be patterned to expose those portions of the seed layer that are located where the first one of the series of conductive layers **133** is desired to be located.

(39) Once the photoresist has been formed and patterned, a conductive material, such as copper, may be formed on the seed layer through a deposition process such as plating. The conductive material may be formed to have a thickness of between about 1 μm and about 10 μm, such as about 5 μm. However, while the material and methods discussed are suitable to form the conductive material, these materials are merely exemplary. Any other suitable materials, such as AlCu or Au, and any other suitable processes of formation, such as CVD or PVD, may be used to form the first one of the series of conductive layers **133**. Once the conductive material has been formed, the photoresist may be removed through a suitable removal process such as ashing. Additionally, after

the removal of the photoresist, those portions of the seed layer that were covered by the photoresist may be removed through, for example, a suitable etch process using the conductive material as a mask.

(40) Once the first one of the series of conductive layers **133** has been formed, a second one of the series of dielectric layers **135** and a second one of the series of conductive layers **133** may be formed by repeating steps similar to the first one of the series of dielectric layers **135** and the first one of the series of conductive layers **133**. These steps may be repeated as desired in order to electrically connect each of the series of conductive layers **133** to an underlying one of the series of conductive layers **133**, and may be repeated as often as desired until an uppermost one of the series of conductive layers **133** and an uppermost one of the series of dielectric layers **131** has been formed. In an embodiment the deposition and patterning of the series of conductive layers **133** and the series of dielectric layers **135** may be continued until the first redistribution layers **131** have a fourth thickness T.sub.4 of between about 10 μm and about 50 μm, such as about 35 μm, although any suitable number of individual layers and any suitable thickness may be utilized.

(41) Once the uppermost one of the series of conductive layers **133** has been covered by the uppermost one of the series of dielectric layers **135**, and the uppermost one of the series of dielectric layers **135** has been patterned to expose a portion of the uppermost one of the series of dielectric layers **135**, underbump metallization layers **137** may be formed through the uppermost one of the series of dielectric layers **135** to be in physical and/or electrical contact with a portion of the uppermost one of the series of conductive layers **133**. In an embodiment the underbump metallization layers **137** may comprise three layers of conductive materials, such as a layer of titanium, a layer of copper, and a layer of nickel. However, one of ordinary skill in the art will recognize that there are many suitable arrangements of materials and layers, such as a n arrangement of chrome/chrome-copper alloy/copper/gold, an arrangement of titanium/titanium tungsten/copper, or an arrangement of copper/nickel/gold, that are suitable for the formation of the underbump metallization layers **137**. Any suitable materials or layers of material that may be used for the underbump metallization layers **137** are fully intended to be included within the scope of the current application.

(42) The underbump metallization layers **137** may be created by forming each layer over the uppermost one of the series of dielectric layers **135** and in electrical and/or physical contact with the uppermost one of the conductive layers **133**. The forming of each layer may be performed using a plating process, such as electrochemical plating, although other processes of formation, such as sputtering, evaporation, or PECVD process, may be used depending upon the desired materials. The underbump metallization layers **137** may be formed to have a thickness of between about 0.7 μm and about 10 μm, such as about 5 μm. Once the desired layers have been formed, portions of the layers may then be removed through a suitable photolithographic masking and etching process to remove the undesired material and to leave the underbump metallization layers **137** in a desired shape, such as a circular, octagonal, square, or rectangular shape, although any desired shape may be formed.

(43) Once the underbump metallization layers **137** have been formed, first external connections **139** may be utilized to provide an external connection point for electrical connection to the first redistribution layer **131** and may be, for example, a contact bump as part of a ball grid array (BGA), although any suitable connection may be utilized. In an embodiment in which the first external connections **139** are contact bumps, the first external connections **139** may comprise a material such as tin, or other suitable materials, such as silver, lead-free tin, or copper. In an embodiment in which the first external connections **139** are tin solder bumps, the first external connections **139** may be formed by initially forming a layer of tin through such commonly used methods such as evaporation, electroplating, printing, solder transfer, ball placement, etc, to a thickness of, e.g., about 250 μm. Once a layer of tin has been formed on the structure, a reflow may be performed in order to shape the material into the desired bump shape.

(44) The first external connections **139** maybe formed to have a first pitch P.sub.1 of between about 200 μm and about 600 μm, such as about 400 μm. Additionally, in an embodiment in which the first external connections **139** are solder balls, the first external connections **139** may have a first height H.sub.1 after the reflow of between about 60 μm and about 250 μm, such as about 180 μm, and, once the first external connections **139** have been bonded to another device (e.g., a printed circuit board), the first external connections **139** may have a joint height of about 140 μm.
(45) FIG. **1**C additionally illustrates a placement and bonding of a high voltage chip **141** in electrical connection with the first redistribution layers **131** through the underbump metallization layers **137**. In an embodiment the high voltage chip **141** is designed and connected in order to supply a high voltage, such as between about 5 V and about 50 V, such as about 33 V, to the sensor **105** in order to amplify the sensor's sensitivity. For example, by integrating the high voltage chip **141** with the sensor **105** such that a high voltage can be supplied to the sensor **105**, the sensitivity of the sensor **105** may be increased ten times by raising the input voltage to 33 V from, e.g., 3.3 V.
(46) In an embodiment the high voltage chip **141** may comprise a second semiconductor substrate (not separately illustrated), active devices (not separately illustrated), metallization layers (not separately illustrated) utilized to interconnect the active devices of the high voltage chip **141**, and second external connections **143** in order to interconnect the high voltage chip **141** to the sensor **105**. The second semiconductor substrate may comprise bulk silicon, doped or undoped, or an active layer of a silicon-on-insulator (SOI) substrate. Generally, an SOI substrate comprises a layer of a semiconductor material such as silicon, germanium, silicon germanium, SOI, silicon germanium on insulator (SGOI), or combinations thereof. Other substrates that may be used include multi-layered substrates, gradient substrates, or hybrid orientation substrates.
(47) The active devices comprise a wide variety of active devices and passive devices such as capacitors, resistors, inductors and the like that may be used to generate the desired structural and functional requirements of the design for the high voltage chip **141**. The active devices may be formed using any suitable methods either within or else on the second semiconductor substrate.
(48) The metallization layers are formed over the second semiconductor substrate and the active devices of the high voltage chip **141** and are designed to connect the various active devices to form functional circuitry. In an embodiment the metallization layers are formed of alternating layers of dielectric and conductive material and may be formed through any suitable process (such as deposition, damascene, dual damascene, etc.). In an embodiment there may be four layers of metallization separated from the second semiconductor substrate by at least one interlayer dielectric layer (ILD), but the precise number of metallization layers is dependent upon the design of the high voltage chip **141**.
(49) The second external connections **143** may be formed to interconnect the high voltage chip **141** to the sensor **105** and may be, for example, contact bumps, although any suitable connection may be utilized. In an embodiment in which the second external connections **143** are contact bumps, the second external connections **143** may comprise a material such as tin, or other suitable materials, such as silver, lead-free tin, or copper. In an embodiment in which the second external connections **143** are tin solder bumps, the second external connections **143** may be formed by initially forming a layer of tin through such commonly used methods such as evaporation, electroplating, printing, solder transfer, ball placement, etc, to a thickness of, e.g., about 100 μm. Once a layer of tin has been formed on the structure, a reflow may be performed in order to shape the material into the desired bump shape.
(50) The high voltage chip **141** may be connected to the underbump metallization layers **137**, for example, by initially applying a solder paste to the exposed underbump metallization layers **137** and then flip chip bonding the high voltage chip **141** to the underbump metallization layers **137**. In an embodiment the high voltage chip **141** may be bonded by sequentially dipping the second external connections **143** of the high voltage chip **141** into flux, and then using a pick-and-place tool in order to physically align the second external connections **143** of the high voltage chip **141**

with individual ones of the underbump metallization layers **137**. In an embodiment in which the second external connections **143** are solder balls, once the high voltage chip **141** has been placed a reflow process may be performed in order to physically bond the high voltage chip **141** with the underlying underbump metallization layers **137** and a flux clean may be performed. However, any other suitable connector or connection process may be utilized, such as metal-to-metal bonding or the like.

(51) In an embodiment the high voltage chip **141** is sized in order to sufficiently fit in conjunction with the first external connections **139**. For example, in an embodiment in which the sensor **105** has an area of about 6.5×6.5 mm.sup.2, the high voltage chip **141** may be formed as a square with an area of between about 4 mm.sup.2 and about 16 mm.sup.2, such as about 6 mm.sup.2. Additionally, after the high voltage chip **141** has been bonded, the high voltage chip **141** may have a fifth thickness T.sub.5 extending away from the first redistribution layer **131** of between about 100 μm and about 200 μm, such as about 125 μm. In a particular embodiment, the second external connections **143** may have a thickness of about 50 μm while the remainder of the high voltage chip **141** may have a thickness of about 75 μm. However, any suitable dimensions may be utilized for the high voltage chip **141**.

(52) Once the high voltage chip **141** has been bonded to the underbump metallization layers **137**, an underfill material **147** may be placed between the high voltage chip **141** and the sensor **105** in order to help protect and isolate the devices. In an embodiment the underfill material **147** is a protective material used to cushion and support the high voltage chip **141** from operational and environmental degradation, such as stresses caused by the generation of heat during operation. The underfill material **147** may comprise, for example, a liquid epoxy or other protective material, and then cured to harden and may be dispensed by, e.g., injection.

(53) FIG. **1**D illustrates a debonding of the carrier substrate **101** from the sensor surface material **103**. In an embodiment the first external connections **139** and, hence, the structure including the sensor **105** and the sensor surface material **103**, may be attached to a ring structure **151**. The ring structure **151** may be a metal ring intended to provide support and stability for the structure during and after the debonding process. In an embodiment the first external connections **139** are attached to the ring structure using, e.g., an ultraviolet tape **153**, although any other suitable adhesive or attachment may be used.

(54) Once the first external connections **139** are attached to the ring structure **151**, the carrier substrate **101** may be debonded from the structure using, e.g., a thermal process to alter the adhesive properties of the adhesive layer **109**. In a particular embodiment an energy source such as an ultraviolet (UV) laser, a carbon dioxide (CO.sub.2) laser, or an infrared (IR) laser, is utilized to irradiate and heat the adhesive layer **109** until the adhesive layer **109** loses at least some of its adhesive properties. Once performed, the carrier substrate **101** and the adhesive layer **109** may be physically separated and removed from the structure comprising the first external connections **139**, the sensor **105**, and the sensor surface material **103**.

(55) Once the carrier substrate **101** has been removed, the sensor surface material **103** and the sensor **105** may be separated from other devices formed using a single substrate to form a first sensor package **160**. In an embodiment the singulation may be performed by using a saw blade (not shown) to slice through the encapsulant **125**, thereby separating one section from another to form the first sensor package **160** with the sensor **105** and the sensor surface material **103**. However, as one of ordinary skill in the art will recognize, utilizing a saw blade for the singulation process is merely one illustrative embodiment and is not intended to be limiting. Alternative methods for singulation, such as utilizing one or more etches to separate the first sensor package **160**, may be utilized. These methods and any other suitable methods may be utilized to singulate the first sensor package **160**.

(56) In an embodiment the first sensor package **160** may be singulated such that the first sensor package **160** has a third width W.sub.3 that is greater than the first width W.sub.1 (of the sensor

surface material **103**) or the second width W.sub.2 (of the sensor **105**), such as having the third width W.sub.3 of between about 5 mm and about 15 mm, such as about 12 mm. Additionally, the first sensor package **160** may be singulated to have a package area of between about 5*5 mm.sup.2 and about 15*15 mm.sup.2, such as about 7.6*7.6 mm.sup.2. Additionally, after the removal of the carrier substrate **101**, the first sensor package **160** may have a second height H.sub.2 of between about 200 μm and about Boo μm, such as about 435 μm. In an embodiment in which the first sensor package **160** has the second height H.sub.2, of 435 μm, the second height H.sub.2 comprises the sensor surface material **103** being 100 μm, the first glue layer **127** being 10 μm, the sensor **105** being 100 μm, the first redistribution layer **131** being 35 μm, and the first external connections **139** being 190 μm. As such, the overall height of the first sensor package **160** may be reduced from about 1 mm to less than about 0.45 mm, such as about 0.435 mm, while also having a gap between the sensor **105** and the sensor surface material **103** of between about 10 and about 30 μm, such as about 10 μm (the thickness of the first glue layer **127**).

(57) By forming the first sensor package **160** as described above, a low cost, high performance system with a small form factor system in package (SIP) solution may be manufactured. Such a small form factor along with the small distance between the array of electrodes **120** and an overlying finger increases the sensitivity of the sensor **105**. Such a package may be integrated into a user equipment such as cellular phones, personal digital assistants, tablet computers, or the like, including such cellular phones that utilize the IOS system.

(58) FIG. **1**E illustrates another embodiment which uses the first TSVs **117** in order to help interconnect the array of electrodes **120**. In this embodiment, however, instead of having the sensor surface material **103** have the first width W.sub.1 which is less than the third width W.sub.3 (the width of the first sensor package **160**), the sensor surface material **103** has the third width W.sub.3 as well. By having the sensor surface material **103** be the same width as the first sensor package **160**, the sensor surface material **103** may extend the width of the first sensor package **160**.

(59) FIG. **2**A illustrates an embodiment which utilizes second TSVs **201** that are formed not within the sensor **105** (as described above with respect to FIGS. **1**A-**1**E), but are formed laterally removed from the location of the sensor **105**. In this embodiment, prior to placement of the sensor **105**, a passivation layer **202** is initially formed over the adhesive layer **109**. In an embodiment the passivation layer **202** may be made of one or more suitable dielectric materials such as silicon oxide, silicon nitride, low-k dielectrics such as carbon doped oxides, extremely low-k dielectrics such as porous carbon doped silicon dioxide, combinations of these, or the like. The passivation layer **202** may be formed through a process such as chemical vapor deposition (CVD), although any suitable process may be utilized, and may have a thickness between about 0.5 μm and about 5 μm, such as about 9.25 KA.

(60) Once the passivation layer **202** has been formed, the underbump metallization layers **137** and the first redistribution layers **131** may be formed over the passivation layer **202**. In an embodiment the underbump metallization layers **137** and the first redistribution layers **131** are formed as described above with respect to FIGS. **1**A-**1**D, although they are formed in reverse order so that the underbump metallization layers **137** are formed between the carrier substrate **101** and the first redistribution layers **131**. However, any suitable process, materials, or order of steps, may be utilized.

(61) Once the underbump metallization layers **137** and the first redistribution layers **131** have been formed over the carrier substrate **101**, the second TSVs **201** are formed in electrical connection with the first redistribution layers **131**. In an embodiment the second TSVs **201** may be formed by initially forming a seed layer (not separately illustrated in FIG. **2**A). In an embodiment the seed layer is a thin layer of a conductive material that aids in the formation of a thicker layer during subsequent processing steps. The seed layer may comprise a layer of titanium about 1,000 Å thick followed by a layer of copper about 5,000 Å thick. The seed layer may be created using processes such as sputtering, evaporation, or PECVD processes, depending upon the desired materials. The

seed layer may be formed to have a thickness of between about 0.3 μm and about 1 μm, such as about 0.5 μm.

(62) Once the seed layer has been formed, a photoresist (also not illustrated in FIG. **2**A) is placed over the seed layer. In an embodiment the photoresist may be placed on the seed layer using, e.g., a spin coating technique to a height of between about 50 μm and about 250 μm, such as about 120 μm. Once in place, the photoresist may then be patterned by exposing the photoresist to a patterned energy source (e.g., a patterned light source) so as to induce a chemical reaction, thereby inducing a physical change in those portions of the photoresist exposed to the patterned light source. A developer is then applied to the exposed photoresist to take advantage of the physical changes and selectively remove either the exposed portion of the photoresist or the unexposed portion of the photoresist, depending upon the desired pattern. In an embodiment the pattern formed into the photoresist is a pattern for the second TSVs **201**. The second TSVs **201** are formed in such a placement as to be located on different sides of subsequently attached devices such as the sensor **105**. However, any suitable arrangement for the pattern of second TSVs **201** may be utilized.

(63) In an embodiment the second TSVs **201** are formed within the photoresist. In an embodiment the second TSVs **201** comprise one or more conductive materials, such as copper, tungsten, other conductive metals, or the like, and may be formed, for example, by electroplating, electroless plating, or the like. In an embodiment, an electroplating process is used wherein the seed layer and the photoresist are submerged or immersed in an electroplating solution. The seed layer surface is electrically connected to the negative side of an external DC power supply such that the seed layer functions as the cathode in the electroplating process. A solid conductive anode, such as a copper anode, is also immersed in the solution and is attached to the positive side of the power supply. The atoms from the anode are dissolved into the solution, from which the cathode, e.g., the seed layer, acquires the dissolved atoms, thereby plating the exposed conductive areas of the seed layer within the opening of the photoresist.

(64) Once the second TSVs **201** have been formed using the photoresist and the seed layer, the photoresist may be removed using a suitable removal process. In an embodiment, a plasma ashing process may be used to remove the photoresist, whereby the temperature of the photoresist may be increased until the photoresist experiences a thermal decomposition and may be removed. However, any other suitable process, such as a wet strip, may be utilized. The removal of the photoresist may expose the underlying portions of the seed layer.

(65) Once exposed a removal of the exposed portions of the seed layer may be performed. In an embodiment the exposed portions of the seed layer (e.g., those portions that are not covered by the second TSVs **201**) may be removed by, for example, a wet or dry etching process. For example, in a dry etching process reactants may be directed towards the seed layer using the second TSVs **201** as masks. In another embodiment, etchants may be sprayed or otherwise put into contact with the seed layer in order to remove the exposed portions of the seed layer. After the exposed portion of the seed layer has been etched away, a portion of the first redistribution layers **131** is exposed between the second TSVs **201**.

(66) Once the second TSVs **201** have been formed, the sensor **105** is placed on the first redistribution layer **131** between the second TSVs **201** using, e.g., a second adhesive layer **208**. In an embodiment the second adhesive layer **208** may be a similar material and applied in a similar fashion as the adhesive layer **109**, although any suitable material may be used. In this embodiment, however, the sensor **105** is placed face up such that the face side **113** is facing away from the carrier substrate **101**. Additionally, because the sensor **105** is placed face up, the first TSVs **117** are not needed, and may be removed such that the contact pads **119** are connected to the array of electrodes **120** and the metallization layers of the sensor **105** on the face side **113** of the sensor **105**.

(67) In a particular embodiment, the array of electrodes **120** is formed over the face side **113** of the sensor **105**, and, once the array of electrodes **120** is formed, the contact pads **119** are formed over and in electrical connection with the array of electrodes **120**, for example, by being connected to

the metallization layers of the sensor **105** instead of being connected to the first TSVs **117**. However, any suitable method of forming both the array of electrodes **120** as well as the contact pads **119** over the face side **113** of the sensor **105** may be utilized, and all such methods are fully intended to be included in the scope of the embodiments.

(68) FIG. **2**B illustrates an encapsulation of the sensor **105** and the second TSVs **201** with the encapsulant **125**. In an embodiment the encapsulant **125** may be applied as described above with respect to FIG. **1**A and, once applied, the encapsulant **125** may be thinned in order to expose the contact pads **119** of the sensor **105** as well as expose the second TSVs **201**. However, any suitable encapsulant and method of application may be utilized.

(69) In another embodiment the encapsulant **125** may be applied in an exposed molding process, wherein the sensor **105** is exposed directly after the molding process has been finished and without any extra thinning processes. In this embodiment there may be a height difference between the sensor **105** and the surface of the encapsulant **125**. As such, a recessing process may be performed in order to form a planar surface for further processing.

(70) FIG. **2**B also illustrates a formation of a second redistribution layer **203** in order to electrically interconnect the second TSVs **201** with the contact pads **119** of the sensor **105**. In an embodiment the second redistribution layer **203** may be similar to the first redistribution layer **131** described above with respect to FIG. **1**C. In a particular embodiment, there may be a single one of the series of conductive layers **133** sandwiched between two of the series of dielectric layers **135**. However, any suitable combination of conductive layers and dielectric layers may be utilized to interconnect the contact pads **119** of the sensor **105** with the second TSVs **201**. In an embodiment the second redistribution layer **203** may be formed to have a sixth thickness T.sub.6 of between about 10 μm and about 50 μm, such as about 17 μm, although any suitable thickness may be utilized.

(71) Once the second redistribution layer **203** has been formed, the sensor surface material **103** may be attached to the second redistribution layer **203** using, e.g., a second glue layer **205**. In an embodiment the sensor surface material **103** may be attached by initially applying the second glue layer **205** to the second redistribution layer **203** and then applying the sensor surface material **103** to the second glue layer **205**. The second glue layer **205** may be similar to the first glue layer **127** described above with respect to FIG. **1**A, although any suitable material may be used. Additionally, in this embodiment the sensor surface material **103** may be formed to have the third width W.sub.3 (the width of the eventual package), although any suitable width may be utilized.

(72) FIG. **2**C illustrates a debonding of the carrier substrate **101** and a patterning of the passivation layer **202** in order to expose the underbump metallization layers **137**. In an embodiment the carrier substrate **101** may be debonded by initially bonding the sensor surface material **103** to, e.g., the ring structure **151**. Once attached, the carrier substrate **101** may be debonded from the structure using, e.g., a thermal process to alter the adhesive properties of the adhesive layer **109** as described above with respect to FIG. **1**D, although any suitable method for debonding the carrier substrate **101** may be utilized.

(73) Once debonded, the passivation layer **202** is patterned in order to expose the underlying underbump metallization layers **137**. In an embodiment the passivation layer **202** may be patterned using, e.g., a laser drilling method. In such a method a protective layer, such as a light-to-heat conversion (LTHC) layer or a hogomax layer (not separately illustrated in FIG. **2**C) is first deposited over the passivation layer **202**. Once protected, a laser is directed towards those portions of the passivation layer **202** which are desired to be removed in order to expose the underlying underbump metallization layers **137**. During the laser drilling process the drill energy may be in a range from 0.1 mJ to about 30 mJ, and a drill angle of about 0 degree (perpendicular to the passivation layer **202**) to about 85 degrees to normal of the passivation layer **202**. In an embodiment the patterning may be formed to form openings over the underbump metallization layers **137** to have a width of between about 100 μm and about 300 μm, such as about 200 μm.

(74) In another embodiment, the passivation layer **202** may be patterned by initially applying a

photoresist (not individually illustrated in FIG. **2**C) to the passivation layer **202** and then exposing the photoresist to a patterned energy source (e.g., a patterned light source) so as to induce a chemical reaction, thereby inducing a physical change in those portions of the photoresist exposed to the patterned light source. A developer is then applied to the exposed photoresist to take advantage of the physical changes and selectively remove either the exposed portion of the photoresist or the unexposed portion of the photoresist, depending upon the desired pattern, and the underlying exposed portion of the passivation layer **202** are removed with, e.g., a dry etch process. However, any other suitable method for patterning the passivation layer **202** may be utilized.

(75) FIG. **2**D illustrates that, once the passivation layer **202** has been patterned to expose the underbump metallization layers **137**, the high voltage chip **141** may be bonded to the underbump metallization layers **137** through the passivation layer **202**, the underfill material **147** may be placed, and the first external connections **139** may be placed in physical and/or electrical connection with the underbump metallization layers **137**. In an embodiment the first external connections **139** may be placed and the high voltage chip **141** may be bonded as described above with respect to FIG. **1**C. However, any suitable process may be utilized.

(76) FIG. **2**D additionally illustrates the singulation of the encapsulant **125** and the sensor surface material **103** to form a second sensor package **207**. In an embodiment the singulation to form the second sensor package **207** may be performed as described above with respect to FIG. **1**D. For example, a saw blade may be used to cut through the encapsulant **125** and the sensor surface material **103** to separate the second sensor package **207** from other sensor packages. However, any suitable method may be utilized.

(77) In this embodiment the singulation process may be performed to form the second sensor package **207** to have an area of between about 5*5 mm.sup.2 and about 15*15 mm.sup.2, such as about 8.36*7.6 mm.sup.2. Additionally, the second sensor package **207** with the second redistribution layer **203** may have a third height H.sub.3 of between about 200 μm and about 800 μm, such as about 452 μm. In an embodiment in which the second sensor package **207** has the third height H.sub.3, of 452 μm, the third height H.sub.3 comprises the sensor surface material **103** being wo μm, the second glue layer **205** being 10 μm, the second redistribution layer **203** being 17 μm, the sensor **105** being wo μm, the first redistribution layer **131** being 35 μm, and the first external connections **139** being 190 μm. As such, the gap between the sensor **105** and the sensor surface material **103** may be between about 10 μm and about 30 μm, such as about 27 μm (the thickness of the second glue layer **205** and the layers of the second redistribution layer **203**).

(78) By manufacturing the second sensor package **207** as described above with respect to FIGS. **2**A-**2**D, a low cost interconnect of the sensor **105** may be manufactured with the integrated fan out structure. Additionally, with the integration of the high voltage chip **141**, the sensitivity of the sensor **105** can be increased while also reducing the overall thickness. Such a sensor package may be incorporated into similar cell phones, personal digital assistants, tablet computers, or the like, such as devices that operate using an Android operating system.

(79) FIG. **3**A illustrates another embodiment in which the sensor **105** is placed face up and in which the contact pads **119** are formed over the face side **113** of the sensor **105** similar to the embodiment described in FIGS. **2**A-**2**D. In this embodiment, however, instead of using the second TSVs **201** to interconnect the contact pads **119** with the first redistribution layer **131**, wire bonds **301** are utilized to interconnect the contact pads **119** with the first redistribution layer **131**. In this embodiment, once the first redistribution layer **131** has been formed over the carrier substrate **101**, the sensor **105** is attached to the first redistribution layer **131** without the formation of the second TSVs **201**.

(80) Additionally in this embodiment, the sensor surface material **103** has either already been attached to the sensor **105** or else is attached to the sensor **105** after the sensor **105** has been attached to the first redistribution layer **131**. In an embodiment the sensor surface material **103** is attached using, e.g., the first glue layer **127**, although any suitable method or material for adhering

the sensor surface material **103** to the sensor **105** may be utilized. In this embodiment, so as not to cover the contact pads **119** of the sensor **105**, the sensor surface material **103** may have a fourth width W.sub.4 of between about 5 mm and about 10 mm, such as about 7 mm.

(81) FIG. **3**A also illustrates a formation of the wire bonds **301** between the contact pads **119** of the sensor **105** and the first redistribution layer **131**. In an embodiment an electronic flame off (EFO) wand may be used to raise the temperature of a gold wire (not individually illustrated in FIG. **3**A) within a capillary controlled by a wire clamp (also not individually illustrated in FIG. **3**A). Once the temperature of the gold wire is raised to between about 150° C. and about 250° C., the gold wire is contacted to the contact pads **119** of the sensor **105** to form a first connection and then the gold wire is moved to the first redistribution layer **131** to form a second connection. Once connected, the remainder of the gold wire is separated from the connected portions to form the wire bonds **301**. The connection process may be repeated to form as many connections as desired.

(82) FIG. **3**A additionally illustrates that, after the wire bonds **301** have been formed, the wire bonds **301**, the sensor **105**, and the sensor surface material **103** may be encapsulated with the encapsulant **125**. In an embodiment the encapsulant **125** may be applied as described above with respect to FIG. **1**A and, once applied, the encapsulant **125** may be thinned in order to expose the sensor surface material **103**. In another embodiment the encapsulant **125** may be initially applied such that the encapsulant does not cover the sensor surface material **103**. Any suitable encapsulant and method of application may be utilized.

(83) FIG. **3**B illustrates a debonding of the carrier substrate **101**, a patterning of the passivation layer **202** to expose the underbump metallization layer **137**, a bonding of the high voltage chip **141**, and a placement of the first external connections **139**. In an embodiment the carrier substrate **101** may be debonded by initially bonding the sensor surface material **103** and the encapsulant **125** to, e.g., the ring structure **151**. Once attached, the carrier substrate **101** may be debonded from the structure using, e.g., a thermal process to alter the adhesive properties of the adhesive layer **109** as described above with respect to FIGS. **1**A-**1**D, although any suitable method for debonding the carrier substrate **101** may be utilized.

(84) Once the carrier substrate **101** has been removed, the passivation layer **202** may be patterned, the high voltage chip **141** may be bonded, and the first external connections **139** may be placed. In an embodiment the passivation layer **202** may be patterned, the high voltage chip **141** may be bonded, and the first external connections **139** may be placed as described above with respect to FIGS. **2**C-**2**D. However, any other suitable methods and materials may be utilized.

(85) FIG. **3**B additionally illustrates the singulation of the encapsulant **125** to form a third sensor package **303**. In an embodiment the singulation to form the third sensor package **303** may be performed as described above with respect to FIG. **1**D. For example, a saw blade may be used to cut through the encapsulant **125** and separate the third sensor package **303** from other sensor packages. However, any suitable method may be utilized.

(86) By connecting the contact pads **119** to the first redistribution layer **131** through the wire bonds **301** (and without the second redistribution layer **203**), the third sensor package **303** may be formed to have an area of between about 5*5 mm.sup.2 and about 15*15 mm.sup.2, such as about 8.5*7.6 mm.sup.2. Additionally, the third sensor package **303** with the second redistribution layer **203** may have a fourth H.sub.4 of between about 200 μm and about 800 μm, such as about 435 μm. In an embodiment in which the third sensor package **303** has the fourth height H.sub.4 of 435 μm, the fourth height H.sub.4 comprises the sensor surface material **103** being 100 μm, the first glue layer **127** being 10 μm, the sensor **105** being 100 μm, the first redistribution layer **131** being 35 μm, and the first external connections **139** being 190 μm. As such, the gap between the sensor **105** and the sensor surface material **103** may be between about 10 μm and about 30 μm, such as about 10 μm (the thickness of the first glue layer **127**).

(87) By manufacturing the third sensor package **303** as described above with respect to FIGS. **3**A-**3**B, a low cost interconnect package for the sensor **105** may be manufactured with a smaller height

with the use of the second TSVs **201**. Additionally, with the integration of the high voltage chip **141**, the sensitivity of the sensor **105** can be increased while also reducing the overall thickness. Such a sensor package may be incorporated into similar cell phones, personal digital assistants, tablet computers, or the like, such as devices that operate using an Android operating system.

(88) FIGS. **4**A-**4**D illustrate yet another embodiment in which connection blocks **401**, such as silicon interposers, are utilized to connect the contact pads **119** of the sensor **105** to the first redistribution layer **131**. In this embodiment the sensor **105** is initially placed onto the adhesive layer **109** over the carrier substrate **101**. In this embodiment the sensor **105** is placed face up such that the face side **113** of the sensor **105** faces away from the carrier substrate **101**. Additionally, with the sensor **105** being placed face-up, the array of electrodes **120** and the contact pads **119** of the sensor **105** face away from the carrier substrate **101** as well.

(89) Additionally in this embodiment, rather than forming the second TSVs **201**, connection blocks **401**, such as silicon interposers, are attached to the adhesive layer **109** over the carrier substrate **101**. In an embodiment the connection blocks **401** comprise a structural material, such as a semiconductor material or dielectric material that allows for the formation of a higher density of structures, such as through vias or integrated passive devices, to be formed therein. In particular embodiments the structural material comprises a material such as silicon, silicon dioxide, glass, combinations of these, or the like.

(90) Within the connection blocks **401**, third through substrate vias (TSVs) **403** may already be partially formed prior to the attachment of the sensor **105** to the adhesive layer **109**. The third TSVs **403** may be formed through the structural material prior to the connection blocks **401** being adhered or bonded to the adhesive layer **109**, and the process for forming them may start by initially applying and developing a suitable photoresist to the structural material, and then etching the structural material to generate third TSV openings. The openings for the third TSVs **403** at this stage may be formed so as to extend into the structural material to a depth at least greater than the eventual desired height of the finished connection block **401**.

(91) Once the openings for the third TSVs **403** have been formed, the openings for the third TSVs **403** may be filled with, e.g., a barrier layer and a conductive material. The barrier layer may comprise a conductive material such as titanium nitride, although other materials, such as tantalum nitride, titanium, a dielectric, or the like may be utilized. The barrier layer may be formed using a CVD process, such as PECVD. However, other processes, such as sputtering or metal organic chemical vapor deposition (MOCVD), may be used. The barrier layer may be formed so as to contour to the underlying shape of the opening for the third TSVs **403**.

(92) The conductive material may comprise copper, although other suitable materials such as aluminum, alloys, doped polysilicon, combinations thereof, and the like, may be utilized. The conductive material may be formed by depositing a seed layer and then electroplating copper onto the seed layer, filling and overfilling the openings for the third TSVs **403**. Once the openings for the third TSVs **403** have been filled, excess barrier layer and excess conductive material outside of the openings for the third TSVs **403** may be removed through a grinding process such as chemical mechanical polishing (CMP), although any suitable removal process may be used.

(93) Once the connection blocks **401** with the partially formed third TSVs **403** have been placed along with the sensor **105**, the sensor **105** and the connection blocks **401** are encapsulated with the encapsulant **125**. In an embodiment the encapsulant **125** may be applied as described above with respect to FIG. **1**A and, once applied, the encapsulant **125** may be thinned in order to expose the contact pads **119** and the partially formed third TSVs **403**. In another embodiment the encapsulant **125** may be initially applied such that the encapsulant **125** does not cover the contact pads **119** and the partially formed third TSVs **403**. Any suitable encapsulant and method of application may be utilized.

(94) FIG. **4**B illustrates that, once the encapsulation has been performed, the carrier substrate **101** may be removed. In an embodiment the carrier substrate **101** may be debonded as described above

with respect to FIG. **1**D. For example, a thermal process may be used to alter the adhesive properties of the adhesive layer **109**, and the carrier substrate **101** may be physically removed.

(95) Once the carrier substrate **101** has been removed, the second redistribution layer **203** may be formed in order to interconnect the contact pads **119** with the partially formed third TSVs **403**. In an embodiment the second redistribution layer **203** may be formed without the presence of the carrier substrate **101** and prior to the bonding of the structure to another carrier. Additionally, the second redistribution layer **203** may be formed as described above with respect to FIG. **2**B. For example, the second redistribution layer **203** in this embodiment may be formed with a first dielectric layer, a first conductive layer, and a second dielectric layer. However, any suitable number of layers or method of manufacture may be utilized.

(96) Once the second redistribution layer **203** has been formed, the second redistribution layer **203** may be bonded to a second carrier substrate **405** using, e.g., a second protective layer **407** and a third adhesive layer **409**. In an embodiment the second carrier substrate **405**, the second protective layer **407**, and the third adhesive layer **409** may be similar to the carrier substrate **101**, the protective layer **107**, and the adhesive layer **109** described above with respect to FIG. **1**A, although they may also be different.

(97) Once the second redistribution layer **203** has been bonded to the second carrier substrate **405**, the thinning of the connection blocks **401** may be performed in order to expose the openings for the third TSVs **403** and form the third TSVs **403** from the conductive material that extends through the structural material of the connection blocks **401**, as well as to remove any of the adhesive layer **109** (e.g., the DAF) that may remain. In an embodiment, the thinning of the connection blocks **401** may be performed by a planarization process such as CMP or etching, leaving the third TSVs **403** planar with the structural material of the connection blocks **401**. Additionally, the same planarization process will also thin both the encapsulant **125** and the sensor **105**, such that the sensor **105**, the encapsulant **125**, the structural material of the connection blocks **401**, and the third TSVs **403** are planar with each other.

(98) FIG. **4**C illustrates that, after the connection blocks **401** have been thinned, the first redistribution layer **131** and the underbump metallization layers **137** may be formed in electrical connection with the now exposed third TSVs **403**. In an embodiment the first redistribution layer **131** and the underbump metallization layers **137** may be formed as described above with respect to FIG. **1**C, although any suitable materials and methods of manufacture may be utilized to form the first redistribution layer **131** and the underbump metallization layers **137**.

(99) FIG. **4**C additionally illustrates that, once the underbump metallization layers **137** have been formed, the high voltage chip **141** may be bonded to the underbump metallization layers **137**, the underfill material **147** may be placed, and the first external connections **139** may be placed in physical and/or electrical connection with the underbump metallization layers **137**. In an embodiment the first external connections **139** may be placed and the high voltage chip **141** may be bonded as described above with respect to FIG. **1**C. However, any suitable process may be utilized.

(100) FIG. **4**D illustrates a removal of the second carrier substrate **405** and a placement of the sensor surface material **103**. In an embodiment the second carrier substrate **405** may be debonded by initially bonding the first external connections **139** to, e.g., the ring structure **151**. Once attached, the second carrier substrate **405** may be debonded from the structure using, e.g., a thermal process to alter the adhesive properties of the third adhesive layer **409** as described above with respect to FIGS. **1**A-**1**D, although any suitable method for debonding the second carrier substrate **405** may be utilized.

(101) Once the second carrier substrate **401** has been removed to expose the second redistribution layer **203**, the sensor surface material **103** may be adhered to the second redistribution layer **203**. In an embodiment the sensor surface material **103** is attached using, e.g., the first glue layer **127**. However, any suitable method or material for adhering the sensor surface material **103** to the second redistribution layer **203** may be utilized.

(102) FIG. **4**D additionally illustrates the singulation of the encapsulant **125** to form a fourth sensor package **411**. In an embodiment the singulation to form the fourth sensor package **411** may be performed as described above with respect to FIG. **1**D. For example, a saw blade may be used to cut through the encapsulant **125** and separate the fourth sensor package **411** from other sensor packages. However, any suitable method may be utilized.
(103) By connecting the contact pads **119** to the first redistribution layer **131** through the third TSVs **403** within the connection blocks **401**, the fourth sensor package **411** may be formed to have an area of between about 5*5 mm.sup.2 and about 15*15 mm.sup.2, such as about 8.6*7.6 mm.sup.2. Additionally, the fourth sensor package **411** with the second redistribution layer **203** may have a fifth H.sub.5 of between about 200 μm and about 800 μm, such as about 452 μm. In an embodiment in which the fourth sensor package **411** has the fifth height H.sub.5 of 452 μm, the fifth height H.sub.5 comprises the sensor surface material **103** being 100 μm, the first glue layer **127** being 10 μm, the second redistribution layer **203** being 17 μm, the sensor **105** being 100 μm, the first redistribution layer **131** being 35 μm, and the first external connections **139** being 190 μm. As such, the gap between the sensor **105** and the sensor surface material **103** may be between about 10 μm and about 30 μm, such as about 27 μm (the thickness of the first glue layer **127** and the layers of the second redistribution layer **203**).
(104) By manufacturing the fourth sensor package **411** as described above with respect to FIGS. **4**A-**4**D, a low cost interconnect package for the sensor **105** may be manufactured with a larger density of interconnections. Additionally, with the integration of the high voltage chip **141**, the sensitivity of the sensor **105** can be increased while also reducing the overall thickness. Such a sensor package may be incorporated into similar cell phones, personal digital assistants, tablet computers, or the like, such as devices that operate using an Android operating system.
(105) In accordance with an embodiment, a method of manufacturing a fingerprint scanner comprising adhering a sensor to a sensor surface material, wherein the sensor comprises through substrate vias, is provided. The sensor and the sensor surface material are encapsulated with an encapsulant. A redistribution layer is formed on a surface of the sensor and in electrical connection with the through substrate vias, the surface facing away from the sensor surface material, and a high voltage die is attached in electrical connection with the redistribution layer.
(106) In accordance with another embodiment, a method of manufacturing a fingerprint scanner comprising electrically connecting a contact pad to a conductive region of a first redistribution layer, wherein the contact pad is located on a first surface of a sensor, wherein the conductive region of the first redistribution layer is laterally separated from the sensor is provided. A sensor surface material is attached over the contact pad, and a high-voltage chip is connected to the first redistribution layer.
(107) In accordance with yet another embodiment, a semiconductor device comprising a sensor comprising a semiconductor substrate and conductive vias extending through the semiconductor substrate is provided. A sensor surface material is attached to the sensor and a redistribution layer is electrically connected to the conductive vias and located on an opposite side of the sensor than the sensor surface material. A high voltage die is electrically connected to the redistribution layer.
(108) The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

Claims

1. A method comprising: forming a through via in a first substrate, wherein a first side of the through via is exposed and a second side of the through via is covered by the first substrate, wherein the second side is opposite the first side; attaching the first substrate to a carrier substrate; attaching a fingerprint sensor device to the carrier substrate adjacent the first substrate; encapsulating the fingerprint sensor device and the first substrate with an encapsulant, wherein the encapsulant separates the fingerprint sensor device and the first substrate; forming a first redistribution structure over a first side of the fingerprint sensor device, a first side of the first substrate, and the first side of the through via wherein the first redistribution structure electrically connects the fingerprint sensor device and the through via of the first substrate; after forming the first redistribution structure, thinning the first substrate to expose the second side of the through via; forming a second redistribution structure over a second side of the fingerprint sensor device, a second side of the first substrate, and the second side of the through via, wherein the second redistribution structure is electrically connected to the through via of the first substrate; and attaching a high voltage device to the second redistribution structure, wherein the high voltage device is electrically connected to the second redistribution structure.
2. The method of claim 1 further comprising, after forming the first redistribution structure, performing a planarization process on the first substrate, the encapsulant, and the second side of the fingerprint sensor device.
3. The method of claim 2, wherein the planarization process removes a portion of the first substrate to expose the through via.
4. The method of claim 1, wherein the first substrate and the encapsulant have the same thickness.
5. The method of claim 1, wherein the first substrate is laterally surrounded by the encapsulant.
6. The method of claim 1, wherein the fingerprint sensor is laterally surrounded by the encapsulant.
7. The method of claim 1, wherein the first substrate is a silicon substrate.
8. The method of claim 1 further comprising forming a sensor surface material over the first side of the fingerprint sensor.
9. A method comprising: placing an interposer and a sensor on a first carrier, wherein the interposer is adjacent the sensor, wherein the interposer comprises a through via having a first height within a structural material having a second height greater than the first height; depositing an encapsulant between the interposer and the sensor; forming a plurality of first conductive layers over the encapsulant, the interposer, and the sensor, wherein the plurality of first conductive layers is electrically connected to the interposer and the sensor; after forming the plurality of first conductive layers, performing a planarization process, wherein after performing the planarization process, the through via, the structural material, the sensor, and the encapsulant have a third height; forming a plurality of second conductive layers over the encapsulant, the interposer, and the sensor opposite the plurality of first conductive layers, wherein the plurality of second conductive layers is electrically connected to the interposer; and forming a sensor surface material over the plurality of first conductive layers.
10. The method of claim 9, wherein the plurality of first conductive layers electrically couples the interposer to the sensor.
11. The method of claim 9, wherein a vertical distance between the sensor and the sensor surface material is in the range of 10 μm and 30 μm.
12. The method of claim 9, wherein a width of the interposer less than a width of the sensor.
13. The method of claim 9 further comprising connecting a high voltage device to the plurality of second conductive layers.
14. The method of claim 9, wherein sensor comprises a plurality of electrodes, wherein the region directly above the plurality of electrodes is free of the first conductive layers of the plurality of first

conductive layers.
15. The method of claim 9, wherein the third height and the first height are the same.
16. A method comprising: forming a connection block, comprising: etching a recess in a substrate; and filling the recess with conductive material to form a through via; forming a first redistribution structure on the connection block; forming a second redistribution structure over the first redistribution structure; forming a fingerprint sensor on the first redistribution structure, wherein the fingerprint sensor is sandwiched between a first redistribution structure and a second redistribution structure, wherein the fingerprint sensor is electrically connected to the second redistribution structure, wherein the connection block is sandwiched between the first redistribution structure and the second redistribution structure, wherein the through via of the connection block is electrically connected to the first redistribution structure and the second redistribution structure; and depositing an encapsulant on the second redistribution structure, wherein the encapsulant separates the fingerprint sensor from the connection block.
17. The method of claim 16, wherein sidewalls of the encapsulant, the first redistribution structure, and the second redistribution structure are coplanar.
18. The method of claim 16 further comprising depositing a sensor surface material on the second redistribution structure.
19. The method of claim 16 further comprising attaching a semiconductor chip to the first redistribution structure.
20. The method of claim 16, wherein the connection block comprises an integrated passive device.