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Inventor(s)	Im; Seoyeon

Thin-Film Transistor and Display Device Including the Same

Abstract

Disclosed is a thin-film transistor in which a carrier mobility of a first active layer connected to a first electrode is lower than a carrier mobility of a second active layer connected to a second electrode. Thus, even when the second active layer is made of a high-carrier mobility material, occurrence of hot carrier stress in the first active layer is reduced. Further, a display device including the thin-film transistor is disclosed.

Inventors: **Im; Seoyeon (Seoul, KR)**

Applicant: **LG Display Co., Ltd.** (Seoul, KR)

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority from Republic of Korea Patent Application No. 10-2024-0023447 filed on Feb. 19, 2024 in the Korean Intellectual Property Office, which is incorporated by reference in its entirety.

BACKGROUND

Field

[0002] The present disclosure relates to a thin-film transistor and a display device including the thin-film transistor.

Description of Related Art

[0003] A display device is used in a variety of devices such as televisions, monitors, smart phones, tablet personal computers (PCs), laptops, and wearable devices.

[0004] The display device may display an image through a number of pixels included in a display area.

[0005] In this case, each pixel may include at least one thin-film transistor that may individually control each pixel.

[0006] Recently, consumer demand for an ultra-high resolution display device is increasing, and thus, the display area is required to include a larger number of pixels.

[0007] When an area size occupied by each pixel included in the display area is reduced, a size of an element such as the thin-film transistor included in the pixel may be reduced.

SUMMARY

[0008] As a specification of the display devices increases, it is also required that a high current be applied to the thin-film transistor that operates to control each pixel.

[0009] In one of schemes for applying high current to the thin-film transistor, an active layer of the thin-film transistor may be made of a high-carrier mobility oxide semiconductor material.

[0010] However, when the active layer is made of the high-carrier mobility oxide semiconductor material, hot carrier stress (HCS) may occur in a channel area adjacent to a drain electrode of the thin-film transistor.

[0011] The hot carrier stress may be described as follows.

[0012] When the drain voltage applied to the thin-film transistor increases beyond a certain value, electrons migrating through the channel area have strong migration energy, thereby causing strong collisions of the electrons in the channel area near the drain area.

[0013] Due to such strong collisions of the electrons, defects may occur in the channel area near the drain area, or a hot carrier stress phenomenon in which the electrons are trapped may occur.

[0014] When the hot carrier stress phenomenon occurs, current characteristics of the thin-film transistor element decreases, which may lead to a defect in which a certain pixel in the display panel does not properly operates.

[0015] In particular, when the active layer is made of the high-carrier mobility oxide semiconductor material, a possibility at which the hot carrier stress occurs may increase due to a high carrier concentration.

[0016] In this way, when the active layer of the thin-film transistor is made of a high-carrier mobility oxide semiconductor material, the high current may be imparted to the thin-film transistor, while the occurrence of the hot carrier stress phenomenon may lead to reduced current characteristics of the transistor or the defect of the transistor.

[0017] Accordingly, through various experiments, the inventors of the present disclosure have invented a thin-film transistor that may reduce the occurrence of the hot carrier stress phenomenon while including a high-carrier mobility active layer, and a display device including the same.

[0018] A purpose according to an embodiment of the present disclosure is to provide a thin-film transistor that may reduce the occurrence of the hot carrier stress phenomenon and a display device including the same.

[0019] In addition, a purpose according to an embodiment of the present disclosure is to provide a thin-film transistor with high luminance and a display device including the same.
[0020] In addition, a purpose according to an embodiment of the present disclosure is to provide a thin-film transistor that may facilitate control of a threshold voltage and a display device including the same.
[0021] In addition, a purpose according to an embodiment of the present disclosure is to provide a thin-film transistor that may increase productivity and reliability of the active layer and achieve production energy saving via process optimization, and a display device including the same.
[0022] In addition, a purpose according to an embodiment of the present disclosure is to provide a thin-film transistor that is advantageous in terms of grayscale expression and a display device including the same.
[0023] Purposes according to the present disclosure are not limited to the above-mentioned purpose. Other purposes and advantages according to the present disclosure that are not mentioned may be understood based on following descriptions, and may be more clearly understood based on embodiments according to the present disclosure. Further, it will be easily understood that the purposes and advantages according to the present disclosure may be realized using means shown in the claims or combinations thereof.
[0024] A thin-film transistor according to an embodiment of the present disclosure includes an active layer, a first electrode connected to one side of the active layer, a second electrode connected to an opposite side of the active layer to one side, and a gate electrode disposed on top of the active layer.
[0025] In this case, the active layer includes a first active layer connected to the first electrode and a second active layer connected to the second electrode, and a carrier mobility of the first active layer is lower than a carrier mobility of the second active layer.
[0026] In addition, a display device according to an embodiment of the present disclosure includes a light-emitting element; and a driving thin-film transistor including an active layer, a first electrode, a second electrode, and a gate electrode and configured to drive the light-emitting element.
[0027] In this case, a carrier mobility of a first area of the active layer connected to the first electrode is lower than a carrier mobility of a second area of the active layer connected to the second electrode.
[0028] According to an embodiment of the present disclosure, the carrier mobility of the first active layer connected to the first electrode is lower than the carrier mobility of the second active layer connected to the second electrode. Thus, even when the second active layer is made of a high-carrier mobility material, the occurrence of the hot carrier stress in the first active layer may be reduced.
[0029] Further, according to an embodiment of the present disclosure, a significant area of an effective channel area of the active layer constituting the main channel may be made of a relatively high carrier mobility material. Thus, high current may be allowed to flow through the thin-film transistor, such that a display device with high luminance may be realized.
[0030] Further, according to an embodiment of the present disclosure, as the active layer is formed as a stack of a plurality of layers with different carrier mobility, it is easier to control a threshold voltage in the active layer based on high current characteristics.
[0031] In addition, according to an embodiment of the present disclosure, as the active layer is formed as a stack of a plurality of layers with different carrier mobility, a limited range on process conditions as required in a process of forming the active layer may be expanded, compared to forming the active layer as a single layer.
[0032] Accordingly, not only may the productivity and reliability of the active layer be improved, but production energy savings may be achieved through process optimization.
[0033] Further, according to an embodiment of the present disclosure, the S-factor value may be

increased by electrically connecting the light blocking layer disposed under the thin-film transistor to the source electrode thereof. Thus, the display device may express sufficient gradations. This may be advantageous in terms of the gradation expression.
[0034] Effects of the present disclosure are not limited to the effects mentioned above, and other effects not mentioned will be clearly understood by those skilled in the art from the descriptions below.

Description

BRIEF DESCRIPTION OF DRAWINGS
[0035] FIG. **1** is a schematic plan view of a display device according to an embodiment of the present disclosure.
[0036] FIG. **2** is a circuit diagram of one sub-pixel of a display device according to an embodiment of the present disclosure.
[0037] FIG. **3** is a cross-sectional view of a thin-film transistor according to a first embodiment of the present disclosure.
[0038] FIG. **4** is a cross-sectional view of a thin-film transistor according to a second embodiment of the present disclosure.
[0039] FIG. **5** is a cross-sectional view of a thin-film transistor according to a third embodiment of the present disclosure.
[0040] FIG. **6** is a cross-sectional view of a thin-film transistor according to a fourth embodiment of the present disclosure.
[0041] FIG. **7** is a cross-sectional view of a thin-film transistor according to a fifth embodiment of the present disclosure.
[0042] FIG. **8** is a cross-sectional view of a thin-film transistor according to a sixth embodiment of the present disclosure.
[0043] FIG. **9** is a cross-sectional view of a thin-film transistor according to a seventh embodiment of the present disclosure.
DETAILED DESCRIPTIONS
[0044] Advantages and features of the present disclosure, and a method of achieving the advantages and features will become apparent with reference to embodiments described later in detail together with the accompanying drawings. However, the present disclosure is not limited to the embodiments as disclosed under, but may be embodied in various different forms. Thus, these embodiments are set forth only to make the present disclosure complete, and to completely inform the scope of the present disclosure to those of ordinary skill in the technical field to which the present disclosure belongs, and the present disclosure is only defined by the scope of the claims.
[0045] A shape, a size, a ratio, an angle, a number, etc. disclosed in the drawings for illustrating embodiments of the present disclosure are illustrative, and the present disclosure is not limited thereto. For simplicity and clarity of illustration, elements in the drawings are not necessarily drawn to scale. The same reference numbers in different drawings represent the same or similar elements, and as such perform similar functionality. Further, descriptions and details of well-known steps and elements are omitted for simplicity of the description. Furthermore, in the following detailed description of the present disclosure, numerous specific details are set forth in order to provide a thorough understanding of the present disclosure. However, it will be understood that the present disclosure may be practiced without these specific details. In other instances, well-known methods, procedures, components, and circuits have not been described in detail so as not to unnecessarily obscure aspects of the present disclosure. The terminology used herein is directed to the purpose of describing particular embodiments only and is not intended to be limiting of the present disclosure. As used herein, the singular constitutes “a” and “an” are intended to include the

plural constitutes as well, unless the context clearly indicates otherwise. It will be further understood that the terms “comprise”, “comprising”, “include”, and “including” when used in this specification, specify the presence of the stated features, integers, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, operations, elements, components, and/or portions thereof.

[0046] In interpreting a numerical value, the value is interpreted as including an error range unless there is no separate explicit description thereof.

[0047] Further, as used herein, when a layer, film, region, plate area, or the like is be disposed “on” or “on a top” of another layer, film, region, plate area, or the like, the former may directly contact the latter or still another layer, film, region, plate area, or the like may be disposed between the former and the latter. As used herein, when a layer, film, region, plate area, or the like is directly disposed “on” or “on a top” of another layer, film, region, plate area, or the like, the former directly contacts the latter and still another layer, film, region, plate area, or the like is not disposed between the former and the latter. Further, as used herein, when a layer, film, region, plate area, or the like is disposed “below” or “under” another layer, film, region, plate area, or the like, the former may directly contact the latter or still another layer, film, region, plate area, or the like may be disposed between the former and the latter. As used herein, when a layer, film, region, plate area, or the like is directly disposed “below” or “under” another layer, film, region, plate area, or the like, the former directly contacts the latter and still another layer, film, region, plate area, or the like is not disposed between the former and the latter.

[0048] In descriptions of temporal relationships, for example, temporal precedent relationships between two events such as “after”, “subsequent to”, “before”, etc., another event may occur therebetween unless “directly after”, “directly subsequent” or “directly before” is not indicated.

[0049] It will be understood that, although the terms “first”, “second”, “third”, and so on may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are used to distinguish one element, component, region, layer or section from another element, component, region, layer or section. Thus, a first element, component, region, layer or section described under could be termed a second element, component, region, layer or section, without departing from the spirit and scope of the present disclosure.

[0050] The features of the various embodiments of the present disclosure may be partially or entirely combined with each other, and may be technically associated with each other or operate with each other. The embodiments may be embodied independently of each other and may be embodied together in an association relationship.

[0051] Hereinafter, with reference to FIG. **1** to FIG. **2**, a display device according to an exemplary embodiment of the present disclosure will be described in detail.

[0052] FIG. **1** is a schematic plan view of a display device according to an exemplary embodiment of the present disclosure.

[0053] An example in which a display device **1** is embodied as an organic electroluminescent display device (for example, organic light-emitting diode display device) is described below. However, embodiments of the present disclosure are not limited thereto.

[0054] The display device **1** may include a substrate **10** including a display area AA and a non-display area NA that surrounds the display area AA.

[0055] In the display area AA of the substrate **10**, a plurality of data lines DL extending in a first direction and a plurality of gate lines GL extending in a second direction that intersects the first direction may be arranged.

[0056] Each of a plurality of sub-pixels such as sub-pixels SP**1**, SP**2**, and SP**3** may be disposed in each of intersections of the data lines DL and the gate lines GL.

[0057] The sub-pixels SP**1**, SP**2**, and SP**3** may emit light of the same color, such as white (W) light, or red (R), green (G), or blue (B) light, or may emit light beams of different colors.

[0058] A combination of the plurality of sub-pixels SP**1**, SP**2**, and SP**3** as described above may constitute one pixel P, without being limited thereto. More or less sub-pixels may constitute one pixel P.
[0059] The plurality of sub-pixels SP**1**, SP**2**, and SP**3** may be arranged in a plurality of rows and columns in a matrix format.
[0060] As used herein, the first direction may be a column or vertical direction and may be defined as a Y-axis direction, and the second direction may be a row or horizontal direction and may be defined as a X-axis direction, without being limited thereto. In another example, the first direction may be the row or horizontal direction, and the second direction may be the column or vertical direction.
[0061] A number of lines and pads that supply various signals and powers to the pixel may be disposed on the non-display area NA of the substrate **10**, without being limited thereto.
[0062] A data driver circuit (D-IC) **20** may be disposed in one side area of the non-display area NA.
[0063] The data driver circuit **20** may be a circuit for driving the plurality of data lines, and may apply a data signal to the data line DL, and may apply a driving voltage such as a high potential voltage VDD or a low potential voltage VSS to the pixel P.
[0064] A power line **30** may extend along an edge of the display area AA and in an side area of the non-display area NA other than the side area in which the data driver circuit **20** is disposed, without being limited thereto.
[0065] For example, a gate driver **40** that applies a gate signal to the gate line GL may be disposed in the non-display area NA and located on each of both opposing sides of the display area AA. For example, the gate driver **40** may be a circuit for driving a plurality of gate lines. The power line **30** capable of applying a voltage to an anode electrode or a cathode electrode in the pixel P may extend along an outer edge of the gate driver **40** and in the non-display area NA.
[0066] The power line **30** may include a low-potential voltage line capable of applying a low-potential voltage VSS to the cathode electrode of the pixel P. However, embodiments of the present disclosure are not limited thereto. For example, the power line **30** may further include a high-potential voltage line capable of applying a high-potential voltage VDD to a thin-film transistor of the pixel P.
[0067] A plurality of power connection lines **31** may be disposed in the display area AA and may electrically connect the power line **30** to the plurality of sub-pixels SP**1**, SP**2**, and SP**3** and may be disposed between the power line **30** and the plurality of sub-pixels SP**1**, SP**2**, and SP**3** and may apply the low potential voltage to the plurality of sub-pixels SP**1**, SP**2**, and SP**3**.
[0068] For example, the plurality of power connection lines **31** may extend in the first direction in which the plurality of data lines DL extend by an equal length, without being limited thereto.
[0069] FIG. **2** is a circuit diagram of one sub-pixel of a display device according to an exemplary embodiment of the present disclosure.
[0070] An example in which the sub-pixel is implemented based on a 4T (transistor) 2C (capacitor) structure is described. However, embodiments of the present disclosure are not limited thereto. For example, 3T1C, 4TIC, 5TIC, 3T2C, 5T2C, 6T2C, 7TIC, 7T2C, 8T2C structures, etc. are also possible. And more or less transistors and capacitors could be included.
[0071] For example, the sub-pixel includes a first storage capacitor Cst**1**, a second storage capacitor Cst**2**, a switching transistor SW, a light-emission control transistor ET, a sensing transistor ST, a driving transistor DR, and light-emitting element OLED, as shown in FIG. **2**. However, embodiments of the present disclosure are not limited thereto. More or less elements are also possible.
[0072] Each of the switching transistor SW, the light-emission control transistor ET, and the sensing transistor ST may act as a switch.
[0073] A first scan signal SCAN**1**, a second scan signal SCAN**2**, and a third scan signal EM may be provided to the sub-pixel via the gate line GL, and a data voltage Vdata may be provided to the

sub-pixel via the data line DL.
[0074] The switching transistor SW may be used to apply the voltage of the data line DL to a node A. For example, when the switching transistor SW is turned on in response to the first scan signal SCAN**1**, the voltage of the data line DL is applied to the node A.
[0075] The switching transistor SW may be turned on or turned off based on the first scan signal SCAN**1**.
[0076] The node A may be connected to a gate electrode of the driving transistor DR. That is, the node A may be between the switching transistor SW and the driving transistor DR.
[0077] The sensing transistor ST may be used to apply an initialization voltage Vini to a node B to initialize a circuit while a compensation operation is performed. For example, when the sensing transistor ST is turned on in response to the second scan signal SCAN**2**, the initialization voltage Vini is applied to the node B.
[0078] The sensing transistor ST may be turned on or turned off based on the second scan signal SCAN**2**.
[0079] The light-emission control transistor ET may be turned on or off based on the third scan signal EM.
[0080] The driving transistor DR may be turned on or off based on the data voltage.
[0081] The switching transistor SW may perform a switching operation to store the data voltage Vdata in the first capacitor Cst**1** in response to the first scan signal SCAN**1**. The first capacitor Cst**1** may be disposed between the node A and the node B.
[0082] The driving transistor DR may operate so that a driving current flows between a high-potential power line VDDEL and a low-potential power line VSSEL based on the data voltage stored in the first capacitor Cst**1**.
[0083] The driving transistor DR may be turned on based on the data voltage to control current flowing through the light-emitting element OLED to display an image.
[0084] The light-emitting element OLED may emit light based on a current of a high potential voltage transmitted via the driving transistor DR.
[0085] One side of the light-emitting element OLED may be connected to the node B, and the other side thereof may be connected to the low-potential power line VSSEL. For example, the anode electrode of the light-emitting element OLED may be connected to the node B, and the cathode electrode thereof may be connected to the low-potential power line VSSEL.
[0086] In the present disclosure, the light-emitting element OLED may be embodied as an organic light-emitting diode. However, embodiments of the present disclosure are not limited thereto. Various types of light-emitting elements may be used as the light-emitting element.
[0087] The second capacitor Cst**2** may be a compensation capacitor and, for example, may compensate for a threshold voltage of the driving transistor DR.
[0088] One side of the second capacitor Cst**2** may be connected to one side of the driving transistor DR, and the other side thereof may be connected to the other side of the light-emission control transistor ET. The other side of the driving transistor DR may be connected to one side of light-emission control transistor ET.
[0089] Each of the switching transistor SW and the sensing transistor ST may have a double gate structure in which gate electrodes are located on top of and under one active layer, respectively.
[0090] As each of the switching transistor SW and the sensing transistor ST has the double gate structure, switching performance may be improved by improving on-off characteristics of the transistor.
[0091] Hereinafter, with reference to FIG. **3**, a thin-film transistor according to a first exemplary embodiment of the present disclosure will be described in detail.
[0092] The thin-film transistor described in the present disclosure may be a driving thin-film transistor as the driving transistor DR. However, embodiments of the present disclosure are not limited thereto.

[0093] Referring to FIG. **3**, a substrate **10** may be disposed, and the substrate **10** may be referred to as a thin-film transistor substrate.
[0094] Glass, plastic such as polyimide, or a flexible polymer film may be used as a material of the substrate **10**. However, embodiments of the present disclosure are not limited thereto.
[0095] A light blocking layer **210** may be disposed on the substrate **10**. Specifically, the light blocking layer **210** may be disposed on a portion of the substrate **10**.
[0096] The light blocking layer **210** may protect an active layer **220** of the thin-film transistor by blocking light incident from an outside.
[0097] Accordingly, the light blocking layer **210** may be disposed to overlap the active layer **220** in a vertical direction.
[0098] The vertical direction in FIG. **3** may mean a Z-axis direction, without being limited thereto.
[0099] The light blocking layer **210** may be formed to have a larger area than that of the active layer **220**, and thus may effectively protect the active layer **220** of the thin-film transistor by blocking light incident from a position under the active layer **220**.
[0100] A buffer layer **150** may be disposed on the light blocking layer **210**. Specifically, the buffer layer **150** may be disposed on the light blocking layer **210** and the portion of the substrate **10** that is exposed by the light blocking layer **210**.
[0101] The buffer layer **150** may be composed of a single or double layer made of silicon oxide (SiOx) or silicon nitride (SiNx). However, embodiments of the present disclosure are not limited thereto.
[0102] The buffer layer **150** may protect the active layer **220** by blocking air and moisture.
[0103] The active layer **220** may be disposed on the buffer layer **150**. Specifically, the active layer **220** may be disposed on a portion of the buffer layer **150**.
[0104] The active layer **220** may include a first active layer **221** and a second active layer **222** having different carrier mobility, without being limited thereto.
[0105] The first active layer **221** and the second active layer **222** may be arranged side by side and may be disposed in the same plane, without being limited thereto.
[0106] For example, the first active layer **221** and the second active layer **222** may be arranged side by side and may be disposed on the buffer layer **150**, without being limited thereto.
[0107] Each of the first active layer **221** and the second active layer **222** may be formed as a single layer, without being limited thereto. In another example, the active layer **220** may be formed as a double layer stack composed of two layers, that, lower and upper level layers, as shown in FIG. **4**.
[0108] As shown in FIG. **3**, a length in a left-right direction of the second active layer **222** may be larger than a length in the left-right direction of the first active layer **221**.
[0109] The left-right direction as indicated in FIG. **3** may refer to the X-axis direction.
[0110] Each of the first active layer **221** and the second active layer **222** may include an oxide semiconductor material, without being limited thereto.
[0111] As one example, the first active layer **221** may have lower carrier mobility than that of the second active layer **222**.
[0112] Accordingly, the first active layer **221** may be made of an oxide semiconductor material with a first carrier mobility, and the second active layer **222** may be made of an oxide semiconductor material with a second carrier mobility higher than the first carrier mobility. For example, the first active layer **221** may be made of an oxide semiconductor material with low carrier mobility, and the second active layer **222** may be made of an oxide semiconductor material with high carrier mobility.
[0113] As used herein, the low carrier mobility and the high carrier mobility are relative concepts. Mobility values of the first active layer **221** and the second active layer **222** are compared to each other, and a relatively lower carrier mobility value may be referred to as the low carrier mobility, and a relatively higher carrier mobility value may be referred as the high carrier mobility.
[0114] In one example, the first active layer **221** of the low carrier mobility may include at least

one of an IGZO (InGaZnO)-based oxide semiconductor material [Ga concentration≥In concentration], a GZO (GaZnO)-based oxide semiconductor material, an IGO (InGaO)-based oxide semiconductor material, and a GZTO (GaZnSnO)-based oxide semiconductor material. However, embodiments of the present disclosure are not limited thereto.

[0115] For example, the first active layer **221** may have a carrier mobility ranging from approximately 5 cm.sup.2/V.Math.s to 12 cm.sup.2/V.Math.s. However, embodiments of the present disclosure are not limited thereto.

[0116] In one example, the second active layer **222** of the high carrier mobility may include at least one of an IGZO (InGaZnO)-based oxide semiconductor material [In concentration>Ga concentration], an IZO (InZnO)-based oxide semiconductor material, an IGZTO (InGaZnSnO)-based oxide semiconductor material, a ITZO (InSnZnO)-based oxide semiconductor material, a FIZO (FeInZnO)-based oxide semiconductor material, a ZnO-based oxide semiconductor material, a SIZO (SiInZnO)-based oxide semiconductor material, and a ZnON (Zn-Oxynitride)-based oxide semiconductor material. However, embodiments of the present disclosure are not limited thereto.

[0117] For example, the second active layer **222** may have a carrier mobility ranging from approximately 20 cm.sup.2/V.Math.s to 50 cm.sup.2/V.Math.s. However, embodiments of the present disclosure are not limited thereto.

[0118] A gate insulating layer **160** may be disposed on the active layer **220**. Specifically, the gate insulating layer **160** may be disposed on the active layer **220** and the portion of the buffer layer **150** that is exposed by the active layer **220**. The gate insulating layer **160** may be composed of a single or double layer of silicon oxide (SiOx) or silicon nitride (SiNx). However, embodiments of the present disclosure are not limited thereto.

[0119] A gate electrode **230** may be disposed on the gate insulating layer **160**. Specifically, the gate electrode **230** may be disposed on a portion of the gate insulating layer **160**.

[0120] The gate electrode **230** may be disposed to overlap the active layer **220** in the vertical direction.

[0121] The gate electrode **230** may be formed to have a smaller area than that of the active layer **220**, without being limited thereto.

[0122] An interlayer insulating layer **170** may be disposed on the gate electrode **230**. Specifically, the interlayer insulating layer **170** may be disposed on the gate electrode **230** and the portion of the gate insulating layer **160** exposed by the gate electrode **230**.

[0123] The interlayer insulating layer **170** may be composed of a single or double layer of silicon oxide (SiOx) or silicon nitride (SiNx). However, embodiments of the present disclosure are not limited thereto.

[0124] A first electrode **241** and a second electrode **242** may be disposed on the interlayer insulating layer **170**. Specifically, the first electrode **241** and the second electrode **242** may be disposed on a portion of the interlayer insulating layer **170**.

[0125] The first electrode **241** may be connected to the first active layer **221** as one portion of the active layer **220** via a first contact hole **241***h* extending through the interlayer insulating layer **170** and the gate insulating layer **160**.

[0126] One area of the active layer **220** where the first active layer **221** is located may be defined as a first area. That is, the first electrode **241** may be connected to the first area via the first contact hole **241***h* extending through the interlayer insulating layer **170** and the gate insulating layer **160**.

[0127] In addition, the second electrode **242** may be connected to the second active layer **222** as the other portion of the active layer **220** via a second contact hole **242***h* extending through the interlayer insulating layer **170** and the gate insulating layer **160**.

[0128] The other area of the active layer **220** where the second active layer **222** is located may be defined as a second area. That is, the second electrode **242** may be connected to the second area via the second contact hole **242***h* extending through the interlayer insulating layer **170** and the gate insulating layer **160**.

[0129] In addition, the second electrode **242** may be connected to the light blocking layer **210** via a third contact hole **243***h* extending through the interlayer insulating layer **170**, the gate insulating layer **160**, and the buffer layer **150**, without being limited thereto.
[0130] Accordingly, the active layer **220** and the light blocking layer **210** may be electrically connected to each other via the second electrode **242**.
[0131] Therefore, the light blocking layer **210** according to an exemplary embodiment of the present disclosure may be electrically connected to the second electrode **242**. However, embodiments of the present disclosure are not limited thereto. In another embodiment, the light blocking layer **210** may not be in contact with the second electrode **242**, but may be connected to another electrode or line so as to be connected to a ground electrode.
[0132] According to an exemplary embodiment of the present disclosure, electrically connecting the second electrode **242** and the light blocking layer **210** disposed under the thin-film transistor to each other may allow a S-factor value to be increased. Thus, the display device may express sufficient gradations, which may be advantageous in terms of gradation expression.
[0133] The S-factor is referred to as “subthreshold slope” and indicates a voltage required when the current increases by 10 times. In a graph (I-V curve) showing characteristics of a drain current relative to a gate voltage, the S-factor value is a reciprocal value of a slope of the graph (I-V curve) in a range below the threshold voltage.
[0134] A small S-factor value means that the slope of the characteristic graph I-V of the drain current relative to the gate voltage is large.
[0135] Therefore, the thin-film transistor may be turned on even under a small voltage, and the switching characteristics of the thin-film transistor may be improved.
[0136] On the other hand, since the voltage reaches the threshold voltage in a short time, it may be difficult to express sufficient gray levels.
[0137] Conversely, a large S-factor value means that the slope of the characteristic graph I-V of the drain current relative to the gate voltage is small.
[0138] Therefore, the switching characteristics of the thin-film transistor may deteriorate due to decrease in an on/off response speed of the thin-film transistor, while sufficient grayscale expression may be achieved because the voltage reaches the threshold voltage over a relatively long period of time.
[0139] When the light blocking layer **210** disposed under the active layer **220** is not connected to the second electrode **242**, the light blocking layer **210** plays the same role as that of the gate electrode, such that the switching characteristics of the transistor may be improved.
[0140] However, as described above, when the switching characteristics are improved, the voltage reaches the threshold voltage in a short time, thus making it difficult to express sufficient grayscale. Therefore, the light blocking layer **210** according to an exemplary embodiment of the present disclosure may be electrically connected to the second electrode **242**, such that the thin-film transistor may provide for sufficient grayscale expression.
[0141] In another embodiment, the light blocking layer **210** may not be in contact with the second electrode **242**, but may be connected to another electrode or line so as to be connected to a ground electrode.
[0142] The first electrode **241** may be a drain electrode, and the second electrode **242** may be a source electrode. However, embodiments of the present disclosure are not limited thereto. In another embodiment, the first electrode **241** may be the source electrode, and the second electrode **242** may be the drain electrode.
[0143] The thin-film transistor may include the active layer **220**, the gate electrode **230**, the first electrode **241**, and the second electrode **242** formed in this way.
[0144] The thin-film transistor according to an exemplary embodiment of the present disclosure is constructed so that the first electrode **241** and the second electrode **242** have an asymmetric structure with each other, and may be configured as a unidirectional element in which current flows

only in a direction from the second electrode **242** to the first electrode **241**. However, embodiments of the present disclosure are not limited thereto.

[0145] As shown in FIG. **3**, an area of the active layer **220** that overlaps the gate electrode **230** in the vertical direction may be a channel area CA.

[0146] Accordingly, an area of each of the first active layer **221** and the second active layer **222** constituting the active layer **220** overlapping the gate electrode **230** in the vertical direction may be the channel area CA. For example, the channel area CA may comprise a first channel area CA**1** and a second channel area CA**2**.

[0147] As discussed above, the length in a left-right direction of the second active layer **222** may be larger than a length in the left-right direction of the first active layer **221**. For example, a length of the second channel area CA**2** may be larger than a length of the first channel area CA**1**.

[0148] For example, an area where the first active layer **221** of the active layer **220** and the gate electrode **230** overlap each other in the vertical direction may be the first channel area CA**1**. An area where the second active layer **222** of the active layer **220** and the gate electrode **230** overlap each other in the vertical direction may be the second channel area CA**2**.

[0149] An area of the active layer **220** that does not overlap the gate electrode **230** in the vertical direction may be a conductivized area CDA**1** and CDA**2**. For example, the channel area CA may be disposed between the conductivized area CDA**1** and conductivized area CDA**2**.

[0150] For example, the channel area CA and the conductivized area CDA**1** and CDA**2** may be formed in the active layer **220** by plasma treatment or hydrogen treatment using the gate electrode **230** as a mask.

[0151] The first active layer **221** connected to the first electrode **241** may act as the first conductivized area CDA**1** in an area thereof that does not overlap with the gate electrode **230**. The first active layer **221** connected to the first electrode **241** may act as the first channel area CA**1** in an area thereof that overlaps with the gate electrode **230**.

[0152] The first active layer **221** may be positioned so that a partial area thereof overlaps the gate electrode **230** in the vertical direction so as to act as the first channel area CA**1**. The first active layer **221** may be positioned so that a partial area thereof does not overlap with the gate electrode **230** in the vertical direction so as to act as the first conductivized area CDA**1**.

[0153] The second active layer **222** connected to the second electrode **242** may act as the second conductivized area CDA**2** in an area thereof that does not overlap with the gate electrode **230**. The second active layer **222** connected to the second electrode **242** may act as the second channel area CA**2** in an area thereof that overlaps with the gate electrode **230**.

[0154] The second active layer **222** may be positioned such that a partial area thereof overlaps the gate electrode **230** in the vertical direction so as to act as the second channel area CA**2**. The second active layer **222** may be positioned such that a partial area thereof does not overlap with the gate electrode **230** in the vertical direction so as to act as the second conductivized area CDA**2**.

[0155] In this case, the second active layer **222** may be formed to have a larger overlapping area with the gate electrode **230** than an area of the first active layer **221** overlapping with the gate electrode **230**. That is, the area of the second channel area CA**2** may be larger than that of the first channel area CA**1**.

[0156] Accordingly, a length of the second channel area CA**2** of the high carrier mobility may be larger than the length of the first channel area CA**1** of the low carrier mobility.

[0157] A main portion of the channel area CA through which a larger number of carriers migrate may be referred to as a main channel area. A portion of the channel area CA through which a smaller number of carriers migrate may be referred to as a sub-channel area.

[0158] However, depending on a stacking type of the active layer **220**, the channel area may include the sub-channel area in addition to the main channel area.

[0159] The carriers may migrate in the sub-channel area. However, a smaller number of carriers may migrate in the sub-channel area, compared to the main channel area.

[0160] When the active layer **220** is formed as a single layer, both the second channel area CA**2** and the first channel area CA**1** arranged side by side and disposed in the same plane may be the main channel areas.
[0161] The first channel area CA**1** and the second channel area CA**2** may be arranged so as not to overlap each other in the vertical direction, without being limited thereto.
[0162] Accordingly, main current MC flowing may flow from the second electrode **242** to the first electrode **241** via the second channel area CA**2** and the first channel area CA**1**. For example, main current MC flowing may flow from the source electrode to the drain electrode via the second channel area CA**2** and the first channel area CA**1**, without being limited thereto.
[0163] In this case, since the length of the second channel area CA**2** of the high carrier mobility is larger than the length of the first channel area CA**1** of the low carrier mobility, the second channel area CA**2** of the high carrier mobility may occupy a significant portion of the main channel area.
[0164] According to an exemplary embodiment of the present disclosure, the significant portion of the main channel area in the channel area CA of the active layer **220** may be made of a relatively high carrier mobility material, so that high current may be allowed to flow through the thin-film transistor. Thus, a display device with high luminance may be realized.
[0165] A first boundary area ΔL**1** and a second boundary area ΔL**2** may be disposed at one side of the channel area CA adjacent to the first conductivized area CDA**1** and the other side of the channel area CA adjacent to the second conductivized area CDA**2**, respectively.
[0166] As previously described, each of the first conductivized area CDA**1** and the second conductivized area CDA**2** may be formed by conductivizing the area of the active layer **220** excluding the channel area CA. For example, the first conductivized area CDA**1** may be formed by conductivizing the area of the first active layer **221** excluding the channel area CA, and the second conductivized area CDA**2** may be formed by conductivizing the area of the second active layer **222** excluding the channel area CA.
[0167] However, in a process of conductivizing the portion of the active layer **220** into the conductive portion, a portion of the channel area CA adjacent to each of the first conductivized area CDA**1** and the second conductivized area CDA**2** may be partially subjected to the conductivizing process into the conductive portion.
[0168] Thus, the portion of the channel area CA adjacent to the first conductivized area CDA**1** may be partially subjected to the conductivizing process into the conductive portion and thus may become the first boundary area ΔL**1**.
[0169] The first boundary area ΔL**1** may be disposed in the first channel area CA**1** of the first active layer **221**. The first channel area CA**1** may be adjacent to the first conductivized area CDA**1**.
[0170] Further, the portion of the channel area CA adjacent to the second conductivized area CDA**2** may be partially subjected to the conductivizing process into the conductive portion and thus may become the second boundary area ΔL**2**.
[0171] The second boundary area ΔL**2** may be disposed in the second channel area CA**2** of the second active layer **222**. The second channel area CA**2** may be adjacent to the second conductivized area CDA**2**.
[0172] Each of the first boundary area ΔL**1** and the second boundary area ΔL**2** may have a higher carrier concentration than that of the channel area CA. However, embodiments of the present disclosure are not limited thereto.
[0173] The first boundary area ΔL**1** and the second boundary area ΔL**2** may have a Fermi level similar to those of the first conductivized area CDA**1** and the second conductivized area CDA**2**, respectively. However, embodiments of the present disclosure are not limited thereto.
[0174] In this way, the conductivity of the first boundary area ΔL**1** and the second boundary area ΔL**2** as both opposing edges of the channel area CA may increase in the process in which the portion of the active layer **220** is converted into the first conductivized area CDA**1** and the second conductivized area CDA**2**.

[0175] Lengths of the first boundary area ΔL**1** and the second boundary area ΔL**2** may be referred to as a first conductivization penetration length ΔL**1** and a second conductivization penetration length ΔL**2**, respectively.
[0176] An area corresponding to a portion of the channel area CA excluding the first conductivization penetration length ΔL**1** and the second conductivization penetration length ΔL**2** in a total length of the channel area CA may be defined as an effective channel area.
[0177] The length of the first channel area CA**1** may exceed at least the first conductivization penetration length ΔL**1**.
[0178] Accordingly, in the first active layer **221**, an area corresponding to a length excluding the first conductivization penetration length ΔL**1** in a total length of the first channel area CA**1** may become a first effective channel area. Thus, in the first active layer **221**, the effective channel area with the low carrier mobility may be secured.
[0179] Similarly, in the second active layer **222**, an area corresponding to a length excluding the second conductivization penetration length ΔL**2** in a total length of the second channel area CA**2** may become a second effective channel area. Thus, in the second active layer **222**, the effective channel area with the high carrier mobility may be secured.
[0180] In this way, in the first active layer **221**, the effective channel area with the low carrier concentration and thus the low carrier mobility may be secured. Thus, even when current flows from the second electrode **242** to the first electrode **241**, the possibility at which the hot carrier stress occurs may be greatly reduced.
[0181] In this way, in the second active layer **222**, the effective channel area with the high carrier concentration and thus the high carrier mobility may be secured.
[0182] According to an exemplary embodiment of the present disclosure as described as above, the carrier mobility of the first active layer **221** connected to the first electrode **241** is lower than that of the second active layer **222** connected to the second electrode **242**. Thus, even when the second active layer **222** is made of the high-carrier mobility material, the occurrence of the hot carrier stress in the first active layer **221** may be reduced.
[0183] That is, the first active layer **221** connected to the first electrode **241** may be formed to have the low carrier mobility, the carrier concentration in the first channel area CA**1** may be reduced. Even when current flows in the unidirectional direction from the second electrode **242** to the first electrode **241**, the occurrence of the hot carrier stress in the first active layer **221** near the first channel area CA**1** may be reduced.
[0184] Further, according to an exemplary embodiment of the present disclosure, the first active layer **221** and the second active layer **222** having different carrier mobilities may be arranged side by side and may be disposed in the same layer, and each thereof may be formed as a single layer, without being limited thereto. Specifically, the carrier mobility of the first active layer **221** connected to the first electrode **241** is lower than that of the second active layer **222** connected to the second electrode **242**. Thus, deterioration of a step coverage of the gate insulating layer **160** formed on the first active layer **221** and the second active layer **222** may be reduced.
[0185] As the degradation of the step coverage of the gate insulating layer **160** is reduced, the stabilization effect of device characteristics may be obtained.
[0186] Hereinafter, FIG. **4** to FIG. **9** will be referred to respectively to describe thin-film transistors according to some further embodiment of the present disclosure.
[0187] However, in second to seventh embodiments as described below, the descriptions of contents duplicate with those about the thin-film transistor according to the first exemplary embodiment as described above with reference to FIG. **3** will be omitted or briefly given. Rather, following descriptions focus on different configurations thereof therefrom.
[0188] Referring to FIG. **4**, in the thin-film transistor according to the second exemplary embodiment, the first active layer **221** may extend toward the second electrode **242** so that the first active layer **221** covers a top surface of the second active layer **222**, without being limited thereto.

In the first exemplary embodiment of FIG. **3**, the first active layer **221** and the second active layer **222** may be arranged side by side and may be disposed in the same plane.

[0189] Therefore, the active layer **220** may be formed as a double layer stack composed of two layers, that, lower and upper-level layers, without being limited thereto. In the first exemplary embodiment of FIG. **3**, each of the first active layer **221** and the second active layer **222** may be formed as a single layer.

[0190] For example, a portion of the first active layer **221** and the second active layer **222** may be disposed in a lower-level layer of the stack. The other portion of the first active layer **221** may extend from the first active layer **221** of the lower-level layer and may be disposed in an upper level layer of the stack. That is, the other portion of the first active layer **221** of the upper level layer may cover a top surface of the second active layer **222** of the lower level layer.

[0191] In this case, the first channel area CA**1** of the first active layer **221** may become larger by a length by which the first active layer **221** extends from the first active layer **221** of the lower-level layer so as to be disposed in the upper level layer of the stack.

[0192] As the first active layer **221** is disposed to cover the top surface of the second active layer **222**, the top surface of the first active layer **221** may be closer to the gate electrode than the top surface of the second active layer **222** may be.

[0193] As the first active layer **221** of the upper level layer is located closer to the gate electrode **230** than the second active layer **222** is, a gate field may be strongly applied to the first active layer **221**, so that the first channel area CA**1** of the active layer **221** may act as the main channel area.

[0194] In this way, when the first channel area CA**1** of the low carrier mobility becomes the main channel area, it may be difficult to achieve the high current characteristic effect of the thin-film transistor.

[0195] Accordingly, according to an exemplary embodiment of the present disclosure, a difference between the carrier mobility of the second active layer **222** and the carrier mobility of the first active layer **221** may be set to be larger, and thus the second channel area CA**2** of the second active layer **222** relatively further away from the gate electrode **230** may act as the main channel area. However, embodiments of the present disclosure are not limited thereto. As another example, a thickness d**2** of the second active layer **222** may be set be larger than a thickness d**1** of the first active layer **221**, as shown in FIG. **5**.

[0196] As one example, the carrier mobility of the second active layer **222** may be set to be higher by at least approximately 10 cm.sup.2/V.Math.s than the carrier mobility of the first active layer **221**. However, embodiments of the present disclosure are not limited thereto.

[0197] Accordingly, instead of the first channel area CA**1** of the first active layer **221** closer to the gate electrode **230** than the second active layer **222** is, the second channel area CA**2** of the second active layer **222** relatively further away from the gate electrode **230** may act as the main channel area. Thus, it is possible to achieve the high current characteristic effect of the thin-film transistor.

[0198] Therefore, referring to FIG. **4**, the main current MC flowing from the second electrode **242** may flow through the second channel area CA**2** and the first channel area CA**1** in the lower level layer of the stack and then may flow to the first electrode **241**.

[0199] In one example, the first channel area CA**1** located in the upper-level layer may function as a protective capping layer that protects the second channel area CA**2** located in the lower level layer, and thus the reliability of the thin-film transistor may be improved.

[0200] During a process of forming the thin-film transistor, the active layer **220** constituting the channel area CA may be damaged during many processes for forming the thin-film transistor.

[0201] In this case, a portion of the first channel area CA**1** of the first active layer **221** in the upper level layer which does not constitute the main channel area covers the upper of the second channel area CA**2**. Thus, the first channel area CA**1** of the first active layer **221** of the upper level layer may function to prevent the damage to the second channel area CA**2** of the lower level layer acting as the main channel area.

[0202] As the damage to the second channel area CA**2** acting as the main channel area may be reduced, the reliability of the thin-film transistor may be improved.
[0203] Further, referring to FIG. **5**, in the thin-film transistor according to the third exemplary embodiment of the present disclosure, a thickness d**2** of the second active layer **222** may be larger than a thickness d**1** of the first active layer **221**, and thus the second channel area CA**2** of the second active layer **222** relatively further away from the gate electrode **230** may act as the main channel area. Thus, it is possible to achieve the high current characteristic effect of the thin-film transistor.
[0204] When the thickness d**2** of the second active layer **222** is larger than the thickness d**1** of the first active layer **221**, the second channel area CA**2** of the second active layer **222** disposed under the first channel area CA**1** of the first active layer **221** may act as the main channel area even though the difference between the carrier mobility of the second active layer **222** and the carrier mobility of the first active layer **221** is not set to be larger. However, embodiments of the present disclosure are not limited thereto. As another example, the thickness d**2** of the second active layer **222** may be set to be larger than the thickness d**1** of the first active layer **221**, and the difference between the carrier mobility of the second active layer **222** and the carrier mobility of the first active layer **221** may be set to be larger, thereby further achieving the high current characteristic effect of the thin-film transistor.
[0205] As the thickness of the second channel area CA**2** of the second active layer **222** increases, a stronger gate field may be applied to the second channel area CA**2**.
[0206] Accordingly, instead of the first channel area CA**1** of the first active layer **221** closer to the gate electrode **230** than the second active layer **222** is, the second channel area CA**2** of the second active layer **222** relatively further away from the gate electrode **230** may act as the main channel area. Thus, it is possible to achieve the high current characteristic effect of the thin-film transistor.
[0207] Therefore, referring to FIG. **5**, the main current MC flowing from the second electrode **242** may flow through the second channel area CA**2** of the lower-level layer and the first channel area CA**1** of the lower level layer and then may flow to the first electrode **241**.
[0208] Referring to FIG. **6**, the thin-film transistor according to the fourth exemplary embodiment of the present disclosure may include a multi-layer active layer **220** composed of a stack of three layers.
[0209] The second active layer **222** may include a second lower active layer **222***b* disposed so that a partial area thereof is covered with the first active layer **221**, and a second upper active layer **222***t* extending from the second lower active layer **222***b* so as to cover at least a partial area of the first active layer **221** covering the second lower active layer **222***b*. That is, a portion of the first active layer **221** may be disposed between the second lower active layer **222***b* and the second upper active layer **222***t*, without being limited thereto.
[0210] For example, the first active layer **221** and the second active layer **222** may be disposed in a lower level layer, the first active layer **221** may be disposed in a middle level layer, and the second active layer **222** may be disposed in a upper level layer. Specifically, a portion of the first active layer **221** and the second lower active layer **222***b* may be disposed in the lower level layer, the other portion of the first active layer **221** may be disposed in the middle level layer, and the second upper active layer **222***t* may be disposed in the upper level layer, without being limited thereto.
[0211] The first active layer **221** of the lower-level layer and the first active layer **221** of the middle level layer may be connected to each other along a side surface of the second active layer **222** of the lower level layer. The second active layer **222** of the lower-level layer and the second active layer **222** of the upper level layer may be connected to each other along a side surface of the first active layer **221** of the middle level layer.
[0212] In this case, the second upper active layer **222***t* and the second lower active layer **222***b* may be formed to have the same carrier mobility. However, embodiments of the present disclosure are not limited thereto.

[0213] For example, the first active layer **221** may be made of an oxide semiconductor material with low carrier mobility, and the second active layer **222** may be made of an oxide semiconductor material with high carrier mobility.
[0214] Additionally, the second upper active layer **222***t* and the second lower active layer **222***b* may be formed in different processes.
[0215] For example, after forming the second lower active layer **222***b* and forming the first active layer **221**, the second upper active layer **222***t* may be additionally formed.
[0216] The second upper active layer **222***t* may not cover a partial area of the first channel area CA**1** of the first active layer **221**, so that a partial area of the first channel area CA**1** of the first active layer **221** may be directly exposed to the gate electrode **230**, without being limited thereto.
[0217] For example, the second upper active layer **222***t* may extend as much as possible such that an end thereof may not invade the first boundary area ΔL**1**.
[0218] The active layer **220** is constructed such that the first active layer **221** of the low carrier mobility is surrounded with the second active layer **222** of the high carrier mobility in a sandwiched manner, and the first active layer **221** of the low carrier mobility spaces upper and lower portions of the second active layer **222** of the high carrier mobility from each other.
[0219] That is, the active layer **220** may be constructed such that the active layers having different carrier mobilities are alternately stacked on top of each other in the vertical direction.
[0220] Since the second upper active layer **222***t* is located closest to the gate electrode **230** and has the high carrier mobility, the second upper active layer **222***t* may constitute the main channel area. Thus, it is possible to achieve the high current characteristic effect of the thin-film transistor.
[0221] Therefore, referring to FIG. **6**, the main current MC flowing from the second electrode **242** may flow through the partial area of the second channel area CA**2** of the second lower active layer **222***b* of the lower level layer and then may flow through the second channel area CA**2** of the second upper active layer **222***t* of the upper level layer, and may flow through the first channel area CA**1** of the first active layer **221** of the middle and lower level layers and then may flow to the first electrode **241**.
[0222] The second lower active layer **222***b* located in the lower-level layer may function as a carrier support layer that supplements the carriers into the second upper active layer **222***t*.
[0223] In order to increase the intensity of the current passing through the second channel area CA**2** of the second upper active layer **222***t*, the carrier mobility of the second upper active layer **222***t* may be further increased or the thickness thereof may be increased. As the thickness of the second upper active layer **222***t* increases, a stronger gate field may be applied to the second channel area CA**2** of the second upper active layer **222***t*.
[0224] However, when the carrier mobility of the second upper active layer **222***t* is excessively increased, the influence of the main channel area adjacent to the gate electrode **230** may become excessively large.
[0225] Accordingly, a threshold voltage of the thin-film transistor may change, and it may be difficult to control an interface between the second upper active layer **222***t* constituting the main channel area and the gate insulating layer **160**.
[0226] Therefore, instead of directly increasing the carrier mobility of the second upper active layer **222***t*, a scheme of indirectly increasing the carrier mobility of the second upper active layer **222***t*, for example, transferring the carrier of the second lower active layer **222***b* to the second upper active layer **222***t* may be applied to the thin-film transistor according to the present disclosure. That is, the second lower active layer **222***b* located in the lower level layer may function as a carrier support layer that supplements the carriers into the second upper active layer **222***t*.
[0227] For example, the strong gate field acts in an area where the voltage applied to the gate electrode **230** is high. Thus, the gate field is affected by the second lower active layer **222***b* of the lower level layer. Thus, as the carriers in the second lower active layer **222***b* migrate to the second upper active layer **222***t*, the carriers may be supplemented to the second upper active layer **222***t*.

[0228] As the carriers are supplemented to the second upper active layer **222***t*, the carrier mobility of the second upper active layer **222***t* indirectly increases. Thus, the intensity of the current passing through the second channel area CA**2** of the second upper active layer **222***t* may be increased while maintaining the stability of the threshold voltage of the thin-film transistor.
[0229] Accordingly, a portion of the first active layer **221** between the second upper active layer **222***t* and the second lower active layer **222***b* may act as a isolation layer that structurally isolates the second upper active layer **222***t* and the second lower active layer **222***b* from each other.
[0230] As the first active layer **221** structurally isolates the second upper active layer **222***t* and the second lower active layer **222***b* from each other, the thickness of the second upper active layer **222***t* may be prevented from directly increasing significantly.
[0231] According to an exemplary embodiment of the present disclosure as described above, the active layer **220** is embodied as the stack of the plurality of layers with different carrier mobility, thereby allowing the threshold voltage to be more easily controlled in the active layer **220** based on high current characteristics.
[0232] Further, according to an exemplary embodiment of the present disclosure, a significant area of an effective channel area of the active layer **220** constituting the main channel may be made of a relatively high carrier mobility material. Thus, high current may be allowed to flow through the thin-film transistor, such that a display device with high luminance may be realized.
[0233] Referring to FIG. **7**, in the thin-film transistor according to the fifth exemplary embodiment, the second active layer **222** extends toward the first electrode **241** so as to cover a top surface of the first active layer **221**. Specifically, the second active layer **222** covers a portion of the top surface of the first active layer **221**.
[0234] Therefore, the active layer **220** may be formed as a double layer composed of two layers, that is, a lower-level layer and an upper level layer. For example, the active layer **220** comprises the first active layer **221** and the second active layer **222** of the lower level layer and the second active layer **222** of the upper level layer.
[0235] For example, the first active layer **221** and the second active layer **222** may be disposed in the lower level layer, and the second active layer **222** may be disposed in the upper level layer. Specifically, the first active layer **221** and a portion of the second active layer **222** may be disposed in the lower level layer, and the other portion of the second active layer **222** may be disposed in the upper level layer.
[0236] In this case, a length of the first channel area CA**1** of the first active layer **221** disposed in the lower level layer is larger than a length of the second channel area CA**2** of the second active layer **222** disposed in the lower level layer.
[0237] However, as the second channel area CA**2** of the second active layer **222** disposed in the upper-level layer extends toward the first electrode **241**, a total length of the second active layer **222** may increase.
[0238] The second active layer **222** extends so as not to cover a partial area of the first channel area CA**1** of the first active layer **221**. Thus, the partial area of the first channel area CA**1** of the first active layer **221** may be directly exposed to the gate electrode **230**, without being limited thereto.
[0239] For example, the second active layer **222** in the upper-level layer may extend as much as possible such an end thereof does not invade the first boundary area ΔL**1**.
[0240] As the second active layer **222** in the upper level layer is disposed to cover the top surface of the first active layer **221**, the top surface of the second active layer **222** may be closer to the gate electrode **230** than a top surface of the first active layer **221** may be.
[0241] As the second active layer **222** of the high carrier mobility is located closer to the gate electrode **230** than the first active layer **221** of the low carrier mobility is, a strong gate field is applied to the second active layer **222**. Thus, the second channel area CA**2** of the second active layer **222** of the upper-level layer may act as the main channel area. Therefore, it is possible to achieve the high current characteristic effect of the thin-film transistor.

[0242] Therefore, referring to FIG. **7**, the main current MC flowing from the second electrode **242** may flow through the second channel area CA**2** of the lower-level layer and then the second channel area CA**2** of the upper level layer and then may flow to the first electrode **241** through the first channel area CA**1** of the lower level layer.
[0243] Referring to FIG. **8**, the thin-film transistor according to the sixth embodiment of the present disclosure may include a multi-layer active layer **220** composed of a stack of three layers.
[0244] The first active layer **221** is constructed to include a first lower active layer **221***b* whose a partial area is covered with the second active layer **222**, and a first upper active layer **221***t* extending from the first lower active layer **221***b* so as to cover at least a partial area of the second active layer **222** covering the first lower active layer **221***b*.
[0245] For example, the first active layer **221** and the second active layer **222** may be disposed in a lower level layer, the second active layer **222** may be disposed in a middle level layer, and the first active layer **221** may be disposed in a upper level layer.
[0246] As the first upper active layer **221***t* is disposed to cover a top surface of the second active layer **222**, a top surface of the first upper active layer **221***t* may be closer to the gate electrode **230** than the top surface of the second active layer **222** may be.
[0247] As the first upper active layer **221***t* is located closer to the gate electrode **230** than the second active layer **222** is, the strong gate field is applied to the first active layer **221**. Thus, the first channel area CA**1** of the first active layer **221** may act as the main channel area.
[0248] When the first channel area CA**1** of the low carrier mobility acts as the main channel area, it may be difficult to achieve the high current characteristic effect of the thin-film transistor.
[0249] Accordingly, according to an exemplary embodiment of the present disclosure, the difference between the carrier mobility of the second active layer **222** and the carrier mobility of the first active layer **221** may be set to be larger, and thus the second channel area CA**2** of the second active layer **222** relatively further away from the gate electrode **230** may act as the main channel area. However, embodiments of the present disclosure are not limited thereto.
[0250] In this case, the carrier mobility of the second active layer **222** may be set to be higher by approximately 10 cm.sup.2/V.Math.s than the carrier mobility of the first active layer **221**. However, embodiments of the present disclosure are not limited thereto.
[0251] Accordingly, instead of the first channel area CA**1** of the first upper active layer **221***t* closer to the gate electrode **230** than the second active layer **222**, the second channel area CA**2** of the second active layer **222** that is relatively further away from the gate electrode **230** may act as the main channel area. Thus, it is possible to achieve the high current characteristic effect of the thin-film transistor.
[0252] Therefore, referring to FIG. **8**, the main current MC flowing from the second electrode **242** may flow through the second active layer **222** of the lower-level layer and then the first channel area CA**1** of the middle level layer and then the first active layer **221** of the lower level layer and then may flow to the first electrode **241**.
[0253] The first channel area CA**1** of the first upper active layer **221***t* located in the upper level layer and the first lower active layer **221***b* located in the lower-level layer may function as a protective capping layer that protects the second channel area CA**2** located in the middle level layer, and thus the reliability of the thin-film transistor may be improved.
[0254] During the process of forming the thin-film transistor, the active layer **220** constituting the channel area CA may be damaged during the process.
[0255] In this case, the first channel area CA**1** of the first upper active layer **221***t* located in the upper level layer which does not constitute the main channel area and the first channel area CA**1** of the first lower active layer **221***b* located in the lower level layer which does not constitute the main channel area may cover the upper and lower surfaces of the second channel area CA**2**, respectively and thus may function to prevent the damage to the second channel area CA**2** of the middle level layer constituting the main channel area.

[0256] The active layer **220** is constructed such that the second active layer **222** of the high carrier mobility is surrounded with the first active layer **221** of the low carrier mobility in a sandwiched manner, and the second active layer **222** of the high carrier mobility spaces upper and lower portions of the first active layer **221** of the low carrier mobility from each other.
[0257] As the damage to the second channel area CA**2** constituting the main channel area is reduced, the reliability of the thin-film transistor may be improved.
[0258] Further, referring to FIG. **9**, the thin-film transistor according to the seventh embodiment of the present disclosure has a stack structure according to FIG. **8**, and further has a structure in which the thickness d**2** of the second active layer **222** is larger than the thickness d**1** of the first upper active layer **221***t*.
[0259] Thus, when the thickness d**2** of the second active layer **222** is larger than the thickness d**1** of the first upper active layer **221***t*, the second channel area CA**2** of the second active layer **222** may act as the main channel area even though the difference between the carrier mobility of the second active layer **222** and the carrier mobility of the first upper active layer **221***t* is not set to be large. However, embodiments of the present disclosure are not limited thereto. As another example, the thickness d**2** of the second active layer **222** may be set to be larger than the thickness d**1** of the first upper active layer **221***t*, and the difference between the carrier mobility of the second active layer **222** and the carrier mobility of the first upper active layer **221***t* may be set to be larger, thereby further achieving the high current characteristic effect of the thin-film transistor.
[0260] As the thickness of the second channel area CA**2** of the second active layer **222** increases, a stronger gate field may be applied to the second channel area CA**2**. Thus, instead of the first channel area CA**1** of the first upper active layer **221***t* closer to the gate electrode **230**, the second channel area CA**2** of the second active layer **222** relatively further away from the gate electrode **230** may act as the main channel area. Thus, it is possible to achieve the high current characteristic effect of the thin-film transistor.
[0261] Therefore, referring to FIG. **9**, the main current MC flowing from the second electrode **242** may flow through the second channel area CA**2** of the upper-level layer and the first channel area CA**1** of the lower level layer, and then may flow to the first electrode **241**.
[0262] A thin-film transistor and a display device according to various aspects and embodiment of the present disclosure may be described as follows.
[0263] One aspect of the present disclosure provides a thin-film transistor comprising: an active layer; a first electrode connected to one side of the active layer; a second electrode connected to an opposite side of the active layer opposite to the one side thereof; and a gate electrode disposed on top of the active layer, wherein the active layer includes a first active layer connected to the first electrode and a second active layer connected to the second electrode, wherein a carrier mobility of the first active layer is lower than a carrier mobility of the second active layer.
[0264] In accordance with some embodiments of the thin-film transistor, the active layer includes a channel area formed in an area thereof overlapping the gate electrode in a vertical direction, wherein the first active layer and the second active layer include a first channel area and a second channel area, respectively, wherein each of the first channel area and the second channel area is located in the channel area, wherein at least a partial area of the first channel area non-overlaps the second channel area in the vertical direction.
[0265] In accordance with some embodiments of the thin-film transistor, the first active layer and the second active layer are located in the same layer.
[0266] In accordance with some embodiments of the thin-film transistor, a length of the second channel area is larger than a length of the first channel area.
[0267] In accordance with some embodiments of the thin-film transistor, the first active layer extends so as to cover a portion of an upper surface of the second active layer.
[0268] In accordance with some embodiments of the thin-film transistor, a top surface of the first active layer covering the portion of the upper surface of the second active layer is closer to the gate

electrode than a top surface of the second active layer is.
[0269] In accordance with some embodiments of the thin-film transistor, a thickness of the second active layer is larger than a thickness of the first active layer.
[0270] In accordance with some embodiments of the thin-film transistor, the second active layer includes: a second lower active layer whose a partial area is covered with the first active layer; and a second upper active layer extending from the second lower active layer so as to cover at least a partial area of the first active layer covering the second lower active layer.
[0271] In accordance with some embodiments of the thin-film transistor, the second lower active layer is used as a carrier support layer that supplements the carriers into the second upper active layer.
[0272] In accordance with some embodiments of the thin-film transistor, a portion of the first active layer between the second upper active layer and the second lower active layer is used as a isolation layer that structurally isolates the second upper active layer and the second lower active layer from each other.
[0273] In accordance with some embodiments of the thin-film transistor, a top surface of the second upper active layer is closer to the gate electrode than a top surface of the first active layer is.
[0274] In accordance with some embodiments of the thin-film transistor, the second active layer extends so as to cover an upper surface of the first active layer.
[0275] In accordance with some embodiments of the thin-film transistor, a top surface of the second active layer is closer to the gate electrode than a top surface of the first active layer is.
[0276] In accordance with some embodiments of the thin-film transistor, the first active layer includes: a first lower active layer whose a partial area is covered with the second active layer; and a first upper active layer extending from the first lower active layer so as to cover at least a partial area of the second active layer covering the first lower active layer.
[0277] In accordance with some embodiments of the thin-film transistor, a top surface of the first upper active layer is closer to the gate electrode than a top surface of the second active layer is.
[0278] In accordance with some embodiments of the thin-film transistor, a thickness of the second active layer is larger than a thickness of the first active layer.
[0279] In accordance with some embodiments of the thin-film transistor, the first electrode acts as a drain electrode, and the second electrode acts as a source electrode.
[0280] In accordance with some embodiments of the thin-film transistor, the active layer includes an oxide semiconductor material.
[0281] In accordance with some embodiments of the thin-film transistor, a light blocking layer is disposed under the active layer, wherein the light blocking layer is electrically connected to the second electrode.
[0282] In accordance with some embodiments of the thin-film transistor, the thin-film transistor acts as a driving thin-film transistor.
[0283] In accordance with some embodiments of the thin-film transistor, the carrier mobility of the second active layer is set to be higher by at least 10 cm.sup.2/V.Math.s than the carrier mobility of the first active layer.
[0284] In accordance with some embodiments of the thin-film transistor, the thin-film transistor is configured to allow current to flow therethrough in a unidirectional manner.
[0285] Another aspect of the present disclosure provides a display device comprising: a light-emitting element; and a driving thin-film transistor including an active layer, a first electrode, a second electrode, and a gate electrode and configured to drive the light-emitting element, wherein a carrier mobility of a first area of the active layer connected to the first electrode is lower than a carrier mobility of a second area of the active layer connected to the second electrode.
[0286] In accordance with some embodiments of the display device, a first channel area and a second channel area are disposed between the first area and the second area, wherein a carrier mobility of the first channel area is lower than a carrier mobility of the second channel area.

[0287] In accordance with some embodiments of the display device, the first channel area includes an area overlapping the gate electrode in a vertical direction and non-overlapping the second channel area in the vertical direction.
[0288] In accordance with some embodiments of the display device, the active layer is composed of a single layer.
[0289] In accordance with some embodiments of the display device, the active layer is composed of a stack of multiple active layers.
[0290] In accordance with some embodiments of the display device, the multiple active layers having different carrier mobilities are alternately stacked in at least a portion of an area overlapping with the gate electrode.
[0291] In accordance with some embodiments of the display device, the driving thin-film transistor is configured to allow current to flow therethrough in a unidirectional manner.
[0292] Another aspect of the present disclosure provides a thin-film transistor comprising: an active layer; a first electrode connected to one side of the active layer; a second electrode connected to an opposite side of the active layer opposite to the one side thereof; and a gate electrode disposed on top of the active layer, wherein the active layer includes a first active layer connected to the first electrode and a second active layer connected to the second electrode, wherein a thickness of the second active layer is larger than a thickness of the first active layer.
[0293] Although exemplary embodiments of the present disclosure have been described with reference to the accompanying drawings, the present disclosure is not limited to the above embodiments, but may be implemented in various different forms. A person skilled in the art may appreciate that the present disclosure may be practiced in other concrete forms without changing the technical spirit or essential characteristics of the present disclosure. Therefore, it should be appreciated that the embodiments as described above is not restrictive but illustrative in all respects.

Claims

1. A thin-film transistor comprising: an active layer; a first electrode connected to one side of the active layer; a second electrode connected to an opposite side of the active layer that is opposite to the one side of the active layer; and a gate electrode on top of the active layer, wherein the active layer includes a first active layer connected to the first electrode and a second active layer connected to the second electrode, wherein a carrier mobility of the first active layer is less than a carrier mobility of the second active layer.
2. The thin-film transistor of claim 1, wherein the active layer includes a channel area in an area of the active layer that overlaps the gate electrode in a vertical direction, wherein the first active layer and the second active layer include a first channel area and a second channel area, respectively, wherein each of the first channel area and the second channel area is located in the channel area, wherein at least a partial area of the first channel area is non-overlapping with the second channel area in the vertical direction.
3. The thin-film transistor of claim 2, wherein the first active layer and the second active layer are located in a same layer.
4. The thin-film transistor of claim 3, wherein a length of the second channel area is greater than a length of the first channel area.
5. The thin-film transistor of claim 2, wherein the first active layer covers a portion of an upper surface of the second active layer.
6. The thin-film transistor of claim 5, wherein a top surface of the first active layer is closer to the gate electrode than a top surface of the second active layer.
7. The thin-film transistor of claim 5, wherein a thickness of the second active layer is greater than a thickness of the first active layer.

8. The thin-film transistor of claim 5, wherein the second active layer includes: a second lower active layer including a partial area that is covered with the first active layer; and a second upper active layer extending from the second lower active layer and covering at least a partial area of the first active layer that covers the second lower active layer.
9. The thin-film transistor of claim 8, wherein a top surface of the second active layer is closer to the gate electrode than a top surface of the first active layer.
10. The thin-film transistor of claim 2, wherein the second active layer covers an upper surface of the first active layer.
11. The thin-film transistor of claim 10, wherein a top surface of the second active layer is closer to the gate electrode than a top surface of the first active layer.
12. The thin-film transistor of claim 10, wherein the first active layer includes: a first lower active layer including a partial area that is covered with the second active layer; and a first upper active layer extending from the first lower active layer and covers at least a partial area of the second active layer that covers the first lower active layer.
13. The thin-film transistor of claim 12, wherein a top surface of the first active layer is closer to the gate electrode than a top surface of the second active layer.
14. The thin-film transistor of claim 12, wherein a thickness of the second active layer is greater than a thickness of the first active layer.
15. The thin-film transistor of claim 1, wherein the first electrode is a drain electrode, and the second electrode is a source electrode.
16. The thin-film transistor of claim 1, wherein the active layer includes an oxide semiconductor material.
17. The thin-film transistor of claim 1, wherein a light blocking layer is under the active layer and is electrically connected to the second electrode.
18. The thin-film transistor of claim 1, wherein the thin-film transistor is a driving thin-film transistor.
19. A display device comprising: a light-emitting element; and a driving thin-film transistor including an active layer, a first electrode, a second electrode, and a gate electrode, the driving thin-film transistor configured to drive the light-emitting element, wherein a carrier mobility of a first area of the active layer that is connected to the first electrode is less than a carrier mobility of a second area of the active layer that is connected to the second electrode.
20. The display device of claim 19, wherein a first channel area and a second channel area are between the first area and the second area, wherein a carrier mobility of the first channel area is less than a carrier mobility of the second channel area.
21. The display device of claim 20, wherein the first channel area includes an area that overlaps the gate electrode in a vertical direction and is non-overlapping the second channel area in the vertical direction.
22. The display device of claim 19, wherein the active layer includes a single layer.
23. The display device of claim 19, wherein the active layer includes a stack of multiple active layers.
24. The display device of claim 23, wherein the multiple active layers in the stack have different carrier mobilities are alternately stacked on top of each other in at least a portion of an area that overlaps with the gate electrode.
25. The display device of claim 19, wherein the driving thin-film transistor is configured to allow current to flow therethrough in a unidirectional manner.