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United States Patent Application Publication	20250266107
Kind Code	A1
Publication Date	August 21, 2025
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### STORAGE APPARATUS INCLUDING WORD LINE GROUPING DEVICE AND OPERATING METHOD THEREOF

#### Abstract

A storage apparatus includes a memory device including a plurality of word lines; and a word line grouping device configured to group the plurality of word lines into a certain number of groups each serving as a memory block so that a read performance value, obtained by reading data of word lines included in a same group by using a representative read voltage, is satisfied with a set tolerance value.

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Family ID:	1000008047477
Appl. No.:	18/774938
Filed:	July 17, 2024

#### Foreign Application Priority Data

KR	10-2024-0022408	Feb. 16, 2024
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#### Publication Classification

Int. Cl.:	G11C16/34 (20060101); G11C16/08 (20060101); G11C16/26 (20060101)
U.S. Cl.:	
CPC	G11C16/3418 (20130101); G11C16/08 (20130101); G11C16/26 (20130101);

#### Background/Summary

##### CROSS-REFERENCES TO RELATED APPLICATION

[0001] The present application claims priority under 35 U.S.C. § 119(a) to Korean Patent Application Number 10-2024-0022408, filed on Feb. 16, 2024, which is incorporated herein by reference in its entirety.

##### BACKGROUND

###### 1. Technical Field

[0002] Various embodiments of the present disclosure generally relate to a semiconductor integrated apparatus, and more particularly, to a storage apparatus including a word line grouping device and an operation method thereof.

###### 2. Related Art

[0003] A semiconductor memory device may include a plurality of memory cells coupled between a plurality of word lines and a plurality of bit lines.

[0004] To store data in the semiconductor memory device or to read data stored in the semiconductor memory device, voltages set according to operation modes are applied to the word lines and the bit lines.

[0005] A flash memory device such as a nonvolatile memory device may have a hierarchical structure which extends to pages (i.e., word lines), memory blocks, planes, and dies. The number of word lines per block may be increased to scale down a chip size of the flash memory device, and thus, an access count per each block may be increased to cause read disturbance.

[0006] A read retry method may be adopted to cope with variation of a threshold voltage of a memory cell due to the read disturbance. The read retry method performs a read operation again by changing a read voltage level when the read operation for a read target word line failed. The semiconductor memory device may retry the read operation based on a read retry table in which read voltage information to be changed in a read retry operation is stored in units of memory blocks or dies.

[0007] As the number of word lines stacked within a block is increased, threshold voltages of word lines included in the same block

may have various distributions due to iterative read operations. Accordingly, read characteristics of the word lines included in the same block may be different from each other.

## SUMMARY

[0008] Embodiments of the present disclosure are provided for a storage apparatus capable of grouping a plurality of word lines in a memory block according to a threshold voltage distribution, and an operating method thereof.

[0009] In an embodiment of the present disclosure, a storage apparatus may include a memory device including a plurality of word lines; and a word line grouping device configured to group the plurality of word lines into a certain number of groups, so that a read performance value, obtained by reading data of word lines included in a same group by using a representative read voltage, is satisfied with a set tolerance value.

[0010] In an embodiment of the present disclosure, an operating method of a storage apparatus which includes a memory device including a plurality of word lines; and a storage controller configured to control the memory device, the method comprising: the storage controller grouping a plurality of word lines into a certain number of groups; and the storage controller regrouping the plurality of word lines so that a read performance value obtained by reading data of word lines included in a same group by using a representative read voltage, is satisfied with a set tolerance value.

[0011] According to embodiments of the present technology, a successful read operation may be guaranteed by grouping word lines having similar threshold voltage distributions and applying a read voltage to the word lines in units of groups.

[0012] These and other features, aspects, and embodiments are described in more detail below.

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## Description

### BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The above and other aspects, features and advantages of the embodiments of the present disclosure will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

[0014] FIG. 1 is a diagram illustrating a configuration of a storage apparatus according to an embodiment of the present disclosure;

[0015] FIG. 2 is a diagram illustrating a configuration of a memory device according to an embodiment of the present disclosure;

[0016] FIG. 3 is a diagram illustrating a configuration of a word line grouping device according to an embodiment of the present disclosure;

[0017] FIG. 4 is a diagram illustrating a configuration of a representative read voltage decision circuit according to an embodiment of the present disclosure;

[0018] FIG. 5 is a diagram for describing a calculation concept of a maximum fail bit count according to an embodiment of the present disclosure;

[0019] FIG. 6 is a diagram for describing a calculation concept of a maximum fail bit count according to an embodiment of the present disclosure;

[0020] FIGS. 7A and 7B are diagrams for describing a group size adjustment concept according to a read performance value according to an embodiment of the present disclosure;

[0021] FIGS. 8A to 8C are diagrams for describing a group size adjustment concept according to a read performance value according to an embodiment of the present disclosure;

[0022] FIGS. 9A to 9D are diagrams for describing a group size adjustment concept according to a read performance value according to an embodiment of the present disclosure;

[0023] FIG. 10 is a diagram for describing a group size adjustment concept according to a read performance value according to an embodiment of the present disclosure; and

[0024] FIG. 11 is a flowchart for describing a method of grouping word lines in a memory device of a storage apparatus according to an embodiment of the present disclosure.

### DETAILED DESCRIPTION

[0025] Various embodiments of the present disclosure are described in detail with reference to the accompanying drawings. The drawings are schematic illustrations of various embodiments and intermediate structures. As such, variations from the configurations and shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, the described embodiments should not be construed as being limited to the particular configurations and shapes illustrated herein but may include deviations in configurations and shapes which do not depart from the spirit and scope of the present teachings as defined in the appended claims.

[0026] The present teachings are described herein with reference to cross-section and/or plan illustrations of embodiments of the present disclosure. However, the embodiments of the present disclosure should not be construed as being limited to the disclosed embodiments. Although a few embodiments of the present disclosure are shown and described, it will be appreciated by those of ordinary skill in the art that changes may be made to these embodiments without departing from the principles and spirit of the present disclosure.

[0027] FIG. 1 is a diagram illustrating a configuration of a storage apparatus 10 according to an embodiment of the present disclosure.

[0028] Referring to FIG. 1, the storage apparatus 10 may include a storage controller 110 and a memory device 120. The memory device 120 may include at least a plurality of nonvolatile memory devices 121, 123, and 125.

[0029] The storage controller 110 and the memory device 120 may be coupled through a plurality of channels CH1, CH2, and CHn.

[0030] In response to a write request of an external apparatus (not shown), the storage apparatus 10 may program write-requested data in the memory device 120 according to control of the storage controller 110.

[0031] In response to a read request of the external apparatus, the storage apparatus 10 may read data stored in the memory device 120 and provide the read data to the external apparatus according to control of the storage controller 110.

[0032] The storage apparatus 10 may read data of the memory device 120 or program data in the memory device 120 to perform the read request of the external apparatus as well an internal operation of the storage apparatus 10. The internal operation may include a house-keeping operation such as garbage collection and wear levelling.

[0033] The storage controller 110 may provide interfacing between the external apparatus and the memory device 120. The storage controller 110 according to an embodiment may include a word line grouping device 20.

[0034] The memory device 120 may have a hierarchical structure which extends to pages as a set of memory cells sharing a word line,

memory blocks as a set of a certain number of pages, planes as a set of a certain number of memory blocks, and dies as a set of a certain number of planes.

[0035] The word line grouping device **20** may group word lines of blocks by a certain number. Specifically, the word line grouping device **20** according to the present technology may group the word lines so that the read performance value is satisfied with a set threshold value when data stored in the plurality of word lines included in the same group are read by a representative read voltage for each logic level.

[0036] In an embodiment, the word line grouping device **20** may classify the word lines within each block into a certain number of initial groups (hereinafter, referred to as initial group number), and determine a read voltage, by which the read performance value is optimized, as a representative read voltage of each initial group. Further, the word line grouping device **20** may regroup the word lines by adjusting (extending or reducing) a size of a group so that the read performance value, obtained by reading data of the word lines in each group by using the representative read voltage to the group, is satisfied with the set threshold value.

[0037] Therefore, the word lines within the block may be classified into the groups, and the representative read voltage for each group may be determined. The storage controller **110** may generate the representative read voltage for each group and an offset voltage determined according to the representative read voltage as a read retry table.

[0038] Single-bit data or multi-bit data may be stored in the memory cells constituting the memory device **120**.

[0039] When the memory cell stores the single-bit data, the representative read voltage of each group may be a read voltage which optimizes the read performance value which distinguishes a logic level of the single-bit data.

[0040] When the memory cell stores the multi-bit data, logic levels of the data stored in the memory cell may be distinguished by different read voltages according to bit positions of the multi-bit data. The read voltage for distinguishing the data stored in the memory cell, which stores the multi-bit data, may be configured of a set of read voltages classified according to bit positions, and the representative read voltages of the groups may be a set of read voltages in which the read performance value is optimized.

[0041] In an embodiment, the read performance value may be determined as at least one of a maximum fail bit count (MAX FBC) and a read pass rate (RPR).

[0042] The maximum fail bit count (MAX FBC) may be a maximum value of a fail bit count (FBC) of each word line for each of a plurality of candidate read voltages when data of word lines in each group are read by using the candidate read voltage. The representative read voltage which optimizes the maximum fail bit count (MAX FBC) may be determined as the candidate read voltage which minimizes the maximum fail bit count (MAX FBC).

[0043] The read pass rate (RPR) may be defined as a ratio of the number of word lines (hereinafter, referred to as 'word line number') having the fail bit count (FBC) within error correction capability to the total number of word lines (hereinafter, referred to as 'total word line number') within the group for each candidate read voltage when data of the word lines in each group are read by using the plurality of candidate read voltages. The representative read voltage which optimizes the read pass rate (RPR) may be determined as the candidate read voltage which maximizes the read pass rate (RPR).

[0044] The word line grouping device **20** according to the present technology may improve the read pass rate (RPR) of each group by determining (deriving) the representative read voltage for the group based on at least one read performance value of the maximum fail bit count (MAX FBC) and the read pass rate (RPR) and adjusting the group size so that the read performance value is satisfied with the set threshold value.

[0045] FIG. 2 is a diagram illustrating a configuration of a memory device **120** according to an embodiment of the present disclosure.

[0046] The memory device **120** in FIG. 2 may be an embodiment of the nonvolatile memory devices **121**, **123** and **125** in FIG. 1.

[0047] Referring to FIG. 2, the memory device **120** may include plural dies DIE0 and DIE1, and each of the dies DIE0 and DIE1 may include plural planes PLANE00/PLANE01 and PLANE10/PLANE11. Each of the planes PLANE00/PLANE01 and PLANE10/PLANE11 may include a plurality of memory blocks BLOCK000 to BLOCK00N/BLOCK010 to BLOCK01N and BLOCK100 to BLOCK10N/BLOCK110 to BLOCK11N. Each of the memory blocks BLOCK000 to BLOCK00N/BLOCK010 to BLOCK01N and BLOCK100 to BLOCK10N/BLOCK110 to BLOCK11N may include a plurality of pages PAGE 0 to PAGE M. The pages PAGE 0 to PAGE M may be equivalent to the word lines.

[0048] The memory device **120** may input/output data through channels CHa and CHb. The channels CHa and CHb may input/output data through an interleaving manner. Each of channels CHa and CHb may be branched into a plurality of ways WAY0/WAY1 and WAY2/WAY3 which share the channels CHa and CHb, respectively. The plurality of ways WAY0/WAY1 and WAY2/WAY3 may be coupled, for example, to dies DIE2/DIE0 and DIE1/DIE3, respectively.

[0049] It has been illustrated in FIG. 2 that the dies DIE0/DIE2 and DIE1/DIE3 are coupled to the ways WAY1/WAY0 and WAY2/WAY3 branched from the channels CHa and CHb, respectively, but the embodiments are not limited thereto.

[0050] The storage controller **110** may be configured to form a super block by grouping simultaneously selectable blocks from among the plurality of memory blocks.

[0051] The super block may be configured of a set of simultaneously selectable blocks. For example, the word line grouping device **20** may be configured to form super blocks A1 and A2 by grouping memory blocks included in different planes within the same die or to form a super block B by grouping memory blocks in different planes within a plurality of dies.

[0052] Based on a result that data of the plurality of pages PAGE 0 to PAGE M included in each of the memory blocks BLOCK000 to BLOCK00N/BLOCK010 to BLOCK01N and BLOCK100 to BLOCK10N/BLOCK110 to BLOCK11, for example, data of the word lines are read by using the plurality of candidate read voltages, the word line grouping device **20** may group the memory blocks according to the representative read voltage which is satisfied with the required read performance value. The read performance may be improved by applying an offset voltage corresponding to the representative read voltage determined (derived) for each group to the read retry operation.

[0053] FIG. 3 is a diagram illustrating a configuration of the word line grouping device **20** of FIG. 1, according to an embodiment of the present disclosure.

[0054] Referring to FIG. 3, the word line grouping device **20** may include an initialization circuit **210**, a representative read voltage decision circuit **220**, a performance determination circuit **230**, a group size adjustment circuit **240**, and a group decision circuit **250**.

[0055] The initialization circuit **210** may set an initial parameter for word line grouping.

[0056] In an embodiment, the initial parameter may include a default read voltage, an initial group number N, a first threshold value TH1, a second threshold value TH2, a third threshold value TH3, and a search direction.

[0057] The default read voltage may be a threshold voltage distribution data of the memory blocks included in the specification of the memory device **120**. The default read voltage may be stored in a special block of the memory device **120**, and the initialization circuit **210** may acquire the default read voltage from the special block.

[0058] The initial group number N may be an initial group number of each block. The initialization circuit **210** may initially group the word lines of each block according to the initial group number N. In an embodiment, the initialization circuit **210** may generate the initial group by dividing the word lines included in the block by the initial group number N.

[0059] The first threshold value TH1 may be an error correction capability of the storage controller **110**.

[0060] The second threshold value TH2 may be a tolerance value for the read performance value of each group.

[0061] The third threshold value TH3 may be a criterion value for terminating group size adjustment and fixing a group size.

[0062] The search direction may be a selection direction of a search target group when adjusting the group size. Addresses may be assigned to the word lines within the memory block in an ascending order along a specific direction, and the group search direction may be selected from among a direction that the word line address is increased and a direction that the word line address is reduced.

[0063] Based on the read result obtained when the plurality of candidate read voltages are applied to the initial groups of each block, which are determined through the initialization circuit **210**, respectively, the representative read voltage decision circuit **220** may determine (derive) the representative read voltage by which the read performance value (e.g., at least one of the maximum fail bit count (MAX FBC) and the read pass rate (RPR)) is optimized.

[0064] In an embodiment, the candidate read voltage may include a default read voltage acquired through the initialization circuit **210** and a plurality of offset voltages in which the default read voltage is shifted by a set amount.

[0065] In an embodiment, the read performance value may be determined as at least one of the maximum fail bit count (MAX FBC) and the read pass rate (RPR).

[0066] The maximum fail bit count (MAX FBC) may be defined as the maximum value of the fail bit count (FBC) of each word line for the plurality of candidate read voltages when the data of the word lines in each group are read by using the plurality of candidate read voltages. The representative read voltage, which optimizes the maximum fail bit number (MAX FBC), may be determined as the candidate read voltage which minimizes the maximum fail bit count (MAX FBC).

[0067] The read pass rate (RPR) may be defined as a ratio of the word line number having the fail bit count (FBC) within the error correction capability (TH1) to the total word line number within the group for the candidate read voltages when the data of the word lines of each group are read by using the plurality of candidate read voltages. The representative read voltage, which optimizes the read pass rate (RPR), may be determined as the candidate read voltage which maximizes the read pass rate (RPR).

[0068] The performance determination circuit **230** may determine whether or not the read performance value, obtained by reading the data of the word lines of each group by using the representative read voltage, is satisfied with the second threshold value TH2. The performance determination circuit **230** may determine whether or not the read performance value of the group, by which the read performance value is satisfied with the second threshold value TH2, is satisfied with the third threshold value TH3 as a group fixing condition.

[0069] The group size adjustment circuit **240** may fix a performance determination target group or may extend or reduce a size of the performance determination target group, based on the determination result of the performance determination circuit **230**.

[0070] For example, when the read performance value of the search target group is satisfied with the second threshold value TH2 and simultaneously is satisfied with the third threshold value TH3, the group size adjustment circuit **240** may fix the size of the corresponding group without adjustment of the size of the group.

[0071] A fact that the read performance value of the group is satisfied with the second threshold value TH2 may mean that the read pass rate (RPR) obtained by data stored in the corresponding group by using the representative read voltage is guaranteed over a certain level or that the maximum fail bit count (MAX FBC) is guaranteed below a certain level.

[0072] A fact that the read performance value of the group is satisfied with the third threshold value TH3 may mean that the read performance value of the corresponding group is very close to the second threshold value TH2.

[0073] When the read performance value of the search target group is satisfied with the second threshold value TH2, but is not satisfied with the third threshold value TH3, for example, when the degree that the read performance value is satisfied with the second threshold value TH2 is equal to or larger than the third threshold value TH3, the group size adjustment circuit **240** may extend the size of the group through a method of adding a word line physically adjacent to the corresponding search target group. The group size adjustment circuit **240** may fix the group just before the extended group as a final group, when the read performance value of the extended group is not satisfied with the second threshold value TH2.

[0074] When the read performance value of the search target group is not satisfied with the second threshold value TH2, the group size adjustment circuit **240** may reduce the group size through a method of eliminating a portion of word lines included in a corresponding group from the corresponding group. For example, the word lines eliminated from the corresponding group may be word lines adjacent to a physical boundary of the corresponding group, but the embodiments are not limited thereto. When the read performance value of the reduced group is satisfied with the second threshold value TH2, the group size adjustment circuit **240** may fix or extend the group size according to whether or not the read performance value of the reduced group is satisfied with the third threshold value TH3.

[0075] The group size adjustment circuit **240** may terminate the group size adjustment and fix the group when the read performance values of all groups are satisfied with the second threshold value TH2.

[0076] When the group size is fixed by the group size adjustment circuit **240**, the group decision circuit **250** may output the maximum value or the minimum value of the word line addresses included in the fixed group as a separator for each group.

[0077] For example, word line addresses which are increased from a word line located adjacent to a semiconductor substrate toward a word line located far away from the semiconductor substrate may be assigned to word lines of a stacked (three-dimensional, 3D) memory device. The word line grouping may be performed from an upper word line toward a lower word line or from the lower word line toward the upper word line, according to the search direction for grouping the word lines. When the groups are fixed, the group decision circuit **250** may output the word line address corresponding to a boundary between physically adjacent groups as a separator.

[0078] FIG. 4 is a diagram illustrating a configuration of the representative read voltage decision circuit **220** of FIG. 3, according to an embodiment of the present disclosure.

[0079] Referring to FIG. 4, the representative read voltage decision circuit **220** may include a MAX FBC-based decision circuit **221** and a RPR-based decision circuit **223**.

[0080] The MAX FBC-based decision circuit **221** may calculate the maximum fail bit count (MAX FBC), which is the maximum value of the fail bit count (FBC) of each word line for the candidate read voltages, when the data of the word lines in each group are read by using at least a portion of the plurality of candidate read voltages. The MAX FBC-based decision circuit **221** may determine the candidate read voltage, which minimizes the maximum fail bit count (MAX FBC), as the representative read voltage.

[0081] The RPR-based decision circuit **223** may calculate the read pass rate (RPR), which is the ratio of the word line number having the fail bit count (FBC) within the error correction capability to the total word line number within the group, when the data of the word lines in each group are read by using at least a portion of the plurality of candidate read voltages. The RPR-based decision circuit **223** may determine the candidate read voltage, which maximizes the read pass rate (RPR), as the representative read voltage.

[0082] For example, in a case where an i-th candidate read voltage is applied, the read pass rate (RPR) may be calculated as the following Equation 1.

$$[00001] \text{WLpassrate}_i = \frac{\text{\#WLsamplesrecoveredbyithRR}}{\text{\#totalWLsamples}} \quad [\text{Equation1}]$$

[0083] When the memory cell operates to store multi-bit data, the word line number covered by each candidate read voltage (#WL samples recovered by an i-th RR) may be derived from the following Equation 2.

[00002]

$$\text{\#WLs(maxFBC} \leq \text{th1)} / \text{\#totalWLs} := \min\{\text{\#LSBs(maxFBC} \leq \text{th1)}, \text{\#CSBs(maxFBC} \leq \text{th1)}, \text{\#MSBs(maxFBC} \leq \text{th1)}\} / \text{\#totalWLs} \quad [\text{Equation2}]$$

[0084] FIG. 5 is a diagram for describing a calculation concept of a maximum fail bit count (MAX FBC) according to an embodiment of the present disclosure.

[0085] Referring to FIG. 5, when data of a plurality of word lines WL0, WL1, WL2, . . . , WLj included in a specific group Group 0 are read by using a plurality of candidate read voltages OFFSET0, OFFSET1, OFFSET2, . . . , OFFSETk, the fail bit count (FBC) (FBC.sub.0,0, FBC.sub.1,0, FBC.sub.2,0, . . . , FBC.sub.j,0), (FBC.sub.0,1, . . . , FBC.sub.j,1) (FBC.sub.0,2, . . . , FBC.sub.j,2), . . . , (FBC.sub.0,k, . . . , FBC.sub.j,k) of the word lines for the candidate read voltages may be derived.

[0086] The MAX FBC-based decision circuit **221** may determine (derive) maximum values among the fail bit counts (FBCs) of the word line WO0, WL1, WL2, . . . , WLj for the candidate read voltages OFFSET0, OFFSET1, OFFSET2, . . . , OFFSETk as the maximum fail bit counts (MAX FBCs). For example, the maximum fail bit counts (MAX FBCs) of the word lines WO0, WL1, WL2, . . . , WLj for the candidate read voltage OFFSET0 may be MAX{FBC.sub.0,0, FBC.sub.1,0, FBC.sub.2,0, . . . , FBC.sub.j,0}.

[0087] The MAX FBC-based decision circuit **221** may determine the candidate read voltage corresponding to the minimum value among the maximum fail bit counts (MAX FBCs) for the candidate read voltages, as the representative read voltage.

[0088] When a memory cell stores multi-bit data, the logic levels of the data stored in the memory cell may be distinguished by different read voltages according to bit positions of the data. The maximum fail bit count (MAX FBC) of the memory cell which stores the multi-bit data may be a sum of the fail bit counts (FBCs) according to the bit positions.

[0089] FIG. 6 is a diagram for describing a calculation concept of a maximum fail bit count (MAX FBC) according to an embodiment of the present disclosure.

[0090] Referring to FIG. 6, a portion of the candidate read voltages may be selected as sample read voltages Sample RV, and the minimum value of the maximum fail bit count (MAX FBC) may be estimated based on the fail bit counts (FBCs) of the word lines for the sample read voltages Sample RV.

[0091] In an embodiment, the max FBC-based decision circuit **221** may calculate the maximum values of the fail bit counts (FBCs) of the word lines for the sample read voltages Sample RV, and determine the sample read voltage, which minimizes the maximum fail bit count (MAX FBC), as the representative read voltage.

[0092] In an embodiment, the MAX FBC-based decision circuit **221** may calculate a voltage corresponding to the minimum MAX FBC, which is estimated based on the maximum fail bit counts (MAX FBCs) of the word lines for the sample read voltages Sample RV, as the representative read voltage.

[0093] For example, the MAX FBC-based decision circuit **221** may determine an average of two read voltages A and B by which the maximum fail bit counts (MAX FBCs) are relatively small among the sample read voltage Sample RV as the representative read voltage Rep. RV.

[0094] For example, the MAX FBC-based decision circuit **221** may additionally calculate the maximum fail bit counts (MAX FBCs) for the offset sample read voltages and determine the voltage, which minimizes the maximum fail bit count (MAX FBC), from the read result corresponding to the sample read voltage and the offset sample read voltage, as the representative read voltage.

[0095] In an embodiment, the offset sample read voltage may include at least one read voltage A by which the maximum fail bit count (MAX FBC) is relatively small, among the sample read voltages Sample RV is increased or reduced by a certain amount. In another example, the offset sample read voltage may be a voltage corresponding to an average voltage of at least two read voltages A and B by which the maximum fail bit counts (MAX FBC) are relatively small.

[0096] In a further example, the MAX FBC-based decision circuit **221** may calculate a vertex by fitting coordinates of three points A, B, C having the relatively small maximum fail bit counts (MAX FBCs) among the sample read voltages to a two dimensional (2D) curve and determine a voltage corresponding to the vertex as the representative voltage Rep. RV.

[0097] The method of determining the representative read voltage based on the max fail bit count (MAX FBC) is not limited thereto, but the method of determining the read voltage which minimizes the fail bit count (FBC) as the representative read voltage may be variously modified.

[0098] FIGS. 7A and 7B are diagrams for describing a group size adjustment concept according to a read performance value according to an embodiment of the present disclosure.

[0099] Referring to FIG. 7A, a memory block including word lines having word line addresses WLN of 1 to 1400 may be classified into four initial groups WLG1, WLG2, WLG3, and WLG4. The word line addresses WLN corresponding to boundaries between the initial groups WLG1, WLG2, WLG3, and WLG4 may be set as WLN.sub.g1(1), WLN.sub.g2(350), WLN.sub.g3(700), WLN.sub.g4(1050) based on the initial group number (N=4).

[0100] The representative read voltage decision circuit **220** may determine (derive) the representative read voltages of the groups WLG1, WLG2, WLG3, and WLG4 as OSRV1, OSRV4, OSRV2, and OSRV2 based on the read performance value (MAX FBC and/or RPR).

[0101] The performance determination circuit **230** may determine whether or not the read performance values of the groups WLG1,

WLG3, and WLG4 are satisfied with the second threshold value TH2.

[0102] The group size adjustment circuit 240 may be configured to extend the group size until the read performance values of the groups WLG1 to WLG4 are satisfied with the third threshold value TH3 when the read performance values of the groups WLG1 to WLG4 are satisfied with the second threshold value TH2, and to reduce the group size when the read performance values of the groups WLG1 to WLG4 are not satisfied with the second threshold value TH2.

[0103] In an embodiment, the group size adjustment circuit 240 may sequentially select the group according to the search direction determined based on the physical positions of the word lines to adjust the group size. For example, the group size adjustment circuit 240 may adjust the group size while sequentially selecting the group in a direction that the word line address is increased, for example, to a direction of from the first group WLG1 toward the fourth group WLG4. In another example, the group size adjustment circuit 240 may adjust the group size while sequentially selecting the group in a direction that the word line address is reduced, for example, a direction from the fourth group WLG4 towards the first group WLG1.

[0104] FIG. 7A illustrates a case where the fourth group WLG4 is satisfied with the second threshold value TH2 when grouping by selecting the group in a descending direction of the word line address.

[0105] The group size adjustment circuit 240 may extend the size of the fourth group WLG4 according to a set criterion as shown in FIG. 7B. As the size of the fourth group WLG4 is extended, the word line address corresponding to the boundary between the fourth group WLG4 and the third group WLG3 may be changed from WLN<sub>g4</sub>(1050) to WLN<sub>g4,new</sub>(1000). As the size of the fourth group WLG4 is extended, the word line addresses included in the new fourth group WLG4<sub>N</sub> may be adjusted as 1000 to 1400, and the word line addresses included in the third group WLG3 may be adjusted as 700 to 1000.

[0106] Subsequently, the group size adjustment circuit 240 may determine whether or not the read performance value of the third group WLG3 is satisfied with the second threshold value TH2. When it is determined that the read performance value of the third group WLG3 is not satisfied with the second threshold value TH2, the group size adjustment circuit 240 may reduce the size of the third group WLG3.

[0107] As the size of the third group WLG3 is reduced, the word line address corresponding to the boundary between the third group WLG3 and the second group WLG2 may be changed from WLN<sub>g3</sub>(700) to WLN<sub>g3,new</sub>(750). As the size of the third group WLG3 is reduced, the word line addresses included in the new third group WLG3<sub>N</sub> may be adjusted as 750 to 1000, and the word line addresses included in the second group WLG2 may be adjusted as 350 to 750.

[0108] Subsequently, although not shown in drawings, the sizes of the first group WLG1 and the second group WLG2 may also be adjusted according to whether or not the read performance values of the first and second groups WLG1 and WLG2 are satisfied with the second and third threshold values TH2 and TH3.

[0109] When the read performance value of the group is satisfied with the second threshold value TH2 and simultaneously satisfied with the third threshold value TH3, the group size adjustment circuit 240 may fix the size of the corresponding group without adjustment of the group size.

[0110] When the read performance values of all groups WLG1 to WLG4 are satisfied with the second threshold value TH2, the group size adjustment circuit 240 may terminate the group size adjustment.

[0111] As described above, the second threshold value TH2 may be a criterion for determining the read performance value of the finally fixed group.

[0112] As the initial group number N is increased, the word line number included in each group may be reduced, and thus the second threshold value TH2 may be set to be small. For example, the initial group number N and the second threshold value TH2 may be inversely proportional to each other.

[0113] To extend or reduce the group size, the following Equation 3 may be used, but the embodiments are not limited thereto.

[00003] • Foreachiteration, [Equation3] ForeachWLG, -EmploytheMAXFBCorRPR

-WLNsetupdate: SelectaccordingtoTH2satisfaction \* Reward(E):  $WLN_{gi,new} = WLN_{g(i-1)} \times a1 + WLN_{gi} \times b1$

\* Penalty(R):  $WLN_{gi,new} = WLN_{g(i+1)} \times a2 + WLN_{gi} \times b2$  \* Penalty(R)  $S < \text{Reward}(E)S = > a1 > a2, b1 < b2$

\* Penalty(R)  $S > \text{Reward}(E)S = > a1 < a2, b1 > b2$  \*  $a_i + b_i = 1, 0 \leq a_i, b_i \leq 1$  wherein E is "extend", R is "reduce", and S is "size"

[0114] Equation 3 is an example that the search direction is a direction that the word line address is reduced from an upper side to a lower side. When the search direction is reversely set, the extension/reduction equation may be reversely used.

[0115] Search convergence speed and an overall read performance value may be changed according to setting values of a1, a2, b1, and b2.

[0116] The group search may be iterated until all groups are satisfied with the second threshold value TH2.

[0117] As described above, the group size adjustment circuit 240 may sequentially select a group according to the search direction, extend the group size so that the read performance value of the selected group is satisfied with the third threshold value TH3 when the read performance value of the selected group is satisfied with the second threshold value TH2, and reduce the group size when the read performance value of the selected group is not satisfied with the second threshold value TH2. Further, when the read performance values of all groups are satisfied with the second threshold value TH2, the group size adjustment circuit 240 may terminate the group size adjustment.

[0118] FIGS. 8A to 8C are diagrams for describing a group size adjustment concept according to a read performance value according to an embodiment of the present disclosure.

[0119] In the present embodiment, the group size adjustment circuit 240 may select a group as a search target according to the search direction, extend the size of the selected group until the read performance value of the selected group is satisfied with the second threshold value TH2, and fix the size of the search target group to a size just before the read performance value of the group is not satisfied with the second threshold value TH2.

[0120] When the size of the search target group is fixed, the group size adjustment circuit 240 may perform a new group search on the remaining word lines.

[0121] Referring back to FIG. 7A, the memory block including the word lines having the word line addresses WLN of 1 to 1400 may be classified into the four initial groups WLG1, WLG2, WLG3, and WLG4. The word line addresses WLN corresponding to the boundaries between the initial groups WLG1, WLG2, WLG3, and WLG4 may be set as WLN.sub.g1(1), WLN.sub.g2(350), WLN.sub.g3(700), WLN.sub.g4(1050) based on the initial group number (N=4). The representative read voltages for the groups WLG1, WLG2, WLG3, and WLG4 may be derived as OSRV1, OSRV4, OSRV2, and OSRV2, respectively.

[0122] Referring to FIG. 8A, the performance determination circuit 230 may set at least one word line group WLG4 as the search group and set the remaining word line groups WLG1 to WLG3 as a standby group, according to the search direction, and determine whether or not the read performance value of the search group WLG4 is satisfied with the second threshold value TH2.

[0123] Referring to FIG. 8B, the group size adjustment circuit 240 may extend the group size while the read performance value of the search group WLG4 is satisfied with the second threshold value TH2.

[0124] As the size of the search group WLG4 is extended, the word line address corresponding to a boundary between the fourth group WLG4 as the search group and the standby group WLG1 to WLG3 may be changed from WLN<sub>g4</sub>(1050) to WLN<sub>g4,new</sub>(1000). As the size of the search group WLG4 is extended, the word line addresses included in the standby group WLG1 to WLG4\_N may be adjusted as 1 to 1400.

[0125] When the read performance value of the search group WLG4 is satisfied with the second threshold value TH2, the group size adjustment circuit 240 may set the boundary word line address WLN<sub>g4</sub> of the search group WLG4 to 1000, and then extend the size of the search group WLG4 again as shown in FIG. 8C.

[0126] As the size of the search group WLG4 is extended, the word line address corresponding to the boundary between the search group WLG4 and the standby group WLG1 to WLG3 may be changed from WLN<sub>g4</sub>(1000) to WLN<sub>g4,new</sub>(950). As the size of the search group WLG4 is extended, the word line addresses included in the standby group WLG1 to WLG3 may be adjusted as 1 to 950.

[0127] When the read performance value of the extended search group WLG4 is not satisfied with the second threshold value TH2, the group size adjustment circuit 240 may fix the size of the corresponding group according to just before word line address WLN<sub>g4</sub>=1000.

[0128] In another example, when the read performance value of the extended search group WLG4 is not satisfied with the second threshold value TH2, the group size adjustment circuit 240 may reduce the size of the search target group WLG4 so that the read performance value of the search target group WLG4 is satisfied with the second threshold value TH2.

[0129] Similarly, the group size adjustment circuit 240 may iterate the group size adjustment on the standby group WLG1 to WLG3.

[0130] In every iteration process, the following Equation 4 may be used to extend or reduce the size of the group according to the read performance value of the search group, but the embodiments are not limited thereto.

[00004] • Foreachiteration, [Equation4] ForWLG4(searchtargetgroup)-EmploytheMAXFBCorRPR

-WLNsetupdate: SelectaccordingtoTH2satisfaction \* Reward<sup>(R)</sup>:  $WLN_{g4,new} = WLN_{g4} \times a1, 0 < a1 < 1$   
\* Penalty<sup>(E)</sup>:  $WLN_{g4,new} = WLN_{g4} \times a2 + WLN_{g4} \times b2$  WLN<sub>g4,prep</sub>: WLGboundaryinprioriteration  $0 < a2, b2 < 1$ ,  
 $a2 + b2 = 1$ ,

whereinEis“extend”, andRis“reduce”.

[0131] Equation 4 is an example that the search direction is a direction that the word line address is reduced from an upper side to a lower side. When the search direction is reversely set, the extension/reduction equation may be reversely used.

[0132] Search convergence speed and an overall read performance value may be changed according to setting values of a1, a2, b1, and b2.

[0133] FIGS. 9A to 9D are diagrams for describing a group size adjustment concept according to a read performance value according to an embodiment of the present disclosure.

[0134] In the embodiment, the group size adjustment circuit 240 may classify the word lines of the memory block into two search groups WLGA and WLGB, determine whether or not the read performance values of the two search groups WLGA and WLGB are satisfied with the second threshold value TH2, and fix the group sizes when the read performance values of the two groups are satisfied with the second threshold value TH2.

[0135] When only the read performance value of one search group of the two search groups is satisfied with the second threshold value TH2 and simultaneously is satisfied with the third threshold value TH3, the group size adjustment circuit 240 may fix the size of the corresponding search group, divide the remaining search group into two search groups, and determine whether or not both the read performance values of the two divided search groups are satisfied with the second threshold value TH2.

[0136] When only the read performance value of one search group of the two divided search groups is satisfied with the second threshold value TH2 and is not satisfied with the third threshold value TH3, the group size adjustment circuit 240 may extend the size of the corresponding divided search group, and determine whether or not both the read performance values of the two divided search groups are satisfied with the second threshold value TH2.

[0137] When both read performance values of the two divided search groups are not satisfied with the second threshold value TH2, the group size adjustment circuit 240 may change the boundary between the two divided search groups according to a designated criterion and determine whether or not both the read performance values of the two divided search groups are satisfied with the second threshold values TH2.

[0138] Referring to FIG. 9A, the group size adjustment circuit 240 may set the representative read voltages of the initial groups, and then classify the initial groups into a search group A WLGA and a search group B WLGB. A boundary word line address of the search group A may be WLN.sub.gA, and a boundary word line address of the search group B may be WLN.sub.gB.

[0139] When the read performance value of the search group A WLGA is satisfied with the second threshold value TH2, the group size adjustment circuit 240 may determine whether or not the read performance value of the search group A WLGA is satisfied with the third threshold value TH3 as shown in FIG. 9B.

[0140] When the read performance value of the search group A WLGA is satisfied with the third threshold value TH3, the group size adjustment circuit 240 may fix the size of the search group A WLGA and classify the search group B WLGB into two search groups WLGB and WLGC. Here, a boundary word line address between the search group B WLGB and the search group C WLGC may be WLN.sub.gB,new. Further, the group size adjustment circuit 240 may determine whether or not the read performance values of two search groups WLGB and WLGC are satisfied with the second threshold value TH2.

[0141] When the read performance value of the search group WLGA of FIG. 9A is not satisfied with the third threshold value TH3, the group size adjustment circuit 140 may extend the size of the search group WLGA as shown in FIG. 9C. Accordingly, the boundary word line address of the search group A WLGA may be changed to WLN.sub.gA,new.

[0142] Subsequently, the group size adjustment circuit 240 may determine whether or not the read performance values of the extended search group A WLGA and the search group B WLGB are satisfied with the second threshold value TH2.

[0143] When both read performance values of the search group A WLGA and the search group B WLGB of FIG. 9A are not satisfied with the second threshold value TH2, the group size adjustment circuit 240 may reduce a size of one search group, for example, the size

of the search group WLGA, and determine whether or not the read performance values of the two search groups WLGB and WLGC are satisfied with the second threshold value TH2, as shown in FIG. 9D.

[0144] FIG. 9D illustrates the example that the size of the search group WLGA is reduced and the boundary word line address of the search group WLGA is changed to WLN.sub.gA,new.

[0145] In every iteration process, the following Equation 5 may be used to extend or reduce the size of the group according to whether or not the read performance values of two search groups are satisfied with the second threshold value TH2, but the embodiments are not limited thereto.

[00005] • Foreachiteration, [Equation5] EmploytheMAXFBCorRPRforWLGAandWLGB

ifbothWLGAandWLGBsatisfyTH2atthesametime, thenstop: WLGsearchtermination(overalliterationtermination)

elseifonlyWLGAisatisfiesTH2ifWLGAisatisfiesTH3, thenstopWLGupdateanddivideWLGB:WLGASearch(extension)termination

$WLN_{gA,new} = WLN_{gA} \times a0, 0 < a0 \leq a1 \# WLGs = \# WLGs + 1; WLN_{new} = [ WLN_{gA,new} \quad WLN_{gA} ]$  else

Reward: $WLN_{gA,new} = WLN_{gA} \times a1, 0 < a1 < 1$  else: Penalty: $WLN_{gA,new} = WLN_{gA} \times a2 + WLN_{gA,new} \times b2$   $a2 + b2 = 1, 0 < a2, b2 < 1$

[0146] Equation 5 is an example that the search direction is a direction that the word line address is reduced from an upper side to a lower side. When the search direction is reversely set, the extension/reduction equation may be reversely used.

[0147] Search convergence speed and an overall read performance value may be changed according to setting values of a1, a2, b1, and b2.

[0148] FIG. 10 is a diagram for describing a group size adjustment concept according to a read performance value according to an embodiment of the present disclosure.

[0149] In the embodiment, the group size adjustment circuit 240 may classify the word line initial groups of the memory block into two search groups having the optimal read performance values in every search iteration process. For example, the group size adjustment circuit 240 may classify the word line initial groups into the two search groups having the optimal read performance values so that the read performance value of at least one search group of the two search groups is satisfied with the second threshold value TH2. Then, the group size adjustment circuit 240 may iterate the above-described search process for the search group, by which the read performance value is not satisfied with the second threshold value TH2.

[0150] Referring to FIG. 10, the group size adjustment circuit 240 may classify all word lines k+m WLs within the memory block into two search groups k WLs and m WLs. For example, the group size adjustment circuit 240 may classify the word lines k+m WLs so that overall read performance values is optimized and a read performance value 1 of one search group k WLs (WLG1) of the search groups k WLs and m WLs is satisfied with the second threshold value TH2. The size of the search groups k WLs (WLG1) by which the read performance value is satisfied with the second threshold value TH2 may be fixed.

[0151] The group size adjustment circuit 240 may divide the search group m WLs by which the read performance value is not satisfied with the second threshold value TH2 into two search groups again. For example, the group size adjustment circuit 240 may iterate a process of classifying the word lines so that the overall read performance value is optimized and a read performance value of one search group WLG2 is satisfied with the second threshold value TH2. The group size adjustment concept according to the present embodiment may be a tree-based size adjustment method and a tree may be generated in a depth that the group number N to be grouped minus 1.

[0152] FIG. 11 is a flowchart for describing a word line grouping method according to an embodiment of the present disclosure.

[0153] Referring to FIG. 11, the word line grouping device 20 may acquire a default read voltage, which is threshold voltage distribution data for memory blocks included in the specification of the memory device 120, from the memory device 120 (at operation S101).

[0154] The word line grouping device 20 may set the initial group number N, the first threshold value TH1, the second threshold value TH2, the third threshold value TH3, and the search direction (at operation S103).

[0155] The initial group number N may be the initial group number of each memory block.

[0156] The first threshold value TH1 may be an error correction capability of the storage controller 110. The second threshold value TH2 may be a tolerance value for the read performance value of each group. The third threshold value may be a criterion value for terminating the group size adjustment and fixing the group size.

[0157] The search direction may be a selection direction of a search target group when adjusting the group size. Addresses may be assigned to the word lines of the memory block in an ascending order along a specific direction, and the group search direction may be selected from a direction that the word line address is increased or a direction that the word line address is reduced.

[0158] The word line grouping device 20 may perform initial grouping on the word lines of each memory block according to the initial group number N (at operation S105). In an embodiment, the initialization circuit 210 may divide the word lines included within the memory block by the initial group number N to generate the initial groups.

[0159] The word line grouping device 20 may determine (derive) the representative read voltage by which the read performance (e.g., at least one of MAX FBC and RPR) is optimized, based on the result read by using the plurality of candidate read voltages to the initial groups of the memory block, respectively (at operation S107).

[0160] In an embodiment, the candidate read voltage may include the default read voltage and the plurality of offset voltages by which the default read voltage is shifted by a certain amount.

[0161] In an embodiment, the read performance value may be determined as at least one of the maximum fail bit count (MAX FBC) and the read pass rate (RPR), and the representative read voltage may be determined from the candidate read voltage by which the maximum fail bit count (MAX FBC) is minimized and the candidate read voltage by which the read pass rate (RPR) is maximized.

[0162] The word line grouping device 20 may determine whether or not the read performance value obtained by reading the data of the word lines of each group by using the representative read voltage is satisfied with the second threshold value TH2 (at operation S109).

[0163] When the read performance value is not satisfied with the second threshold value (i.e., 'N' at the operation S109), the word line grouping device 20 may change a size of the corresponding group, for example, may reduce the group size (at operation S111). Further, the word line grouping device 20 may determine whether or not the read performance value of the size-changed group is satisfied with the second threshold value TH2 (at the operation S109). A fact that the read performance value of the group is satisfied with the second threshold value TH2 may mean that the read pass rate (RPR) obtained by reading the data stored in the corresponding group by using the representative read voltage is guaranteed above a certain level or that the maximum fail bit count (MAX FBC) is guaranteed below the certain level.



[0164] When the read performance value is satisfied with the second threshold value TH2 (i.e., ‘Y’ at the operation S109), the word line grouping device 20 may determine whether or not the read performance value of the corresponding group is satisfied with the third threshold value TH3 which is a group fixing criterion (at operation S113). The fact that the read performance value of the group is satisfied with the third threshold value TH3 may mean that the read performance value of the corresponding group is very close to the second threshold value TH2.

[0165] When the read performance value is satisfied with the third threshold value TH3 (i.e., ‘Y’ at the operation S113), the word line grouping device 20 may fix the size of the corresponding group and output the boundary word line address of the fixed group (at operation S115).

[0166] When the read performance value of the search target group is satisfied with the second threshold value TH2, but is not satisfied with the third threshold value TH3 (i.e., ‘N’ at the operation S113), for example, when the degree that the read performance value is satisfied with the second threshold value TH2 is larger than the third threshold value TH3, the word line grouping device 20 may change the size of the corresponding group, for example, extend the size of the corresponding group (at the operation S111). The word line grouping device 20 may determine whether or not the read performance value of the size-changed group is satisfied with the second threshold value TH2 (at the operation S109).

[0167] The word line grouping device 20 may add or delete the word line physically adjacent to the corresponding group to change the group size.

[0168] When the read performance value of the extended group is not satisfied with the second threshold value TH2 in operation S109 after the group size is fixed, the word line grouping device 20 may fix the group just before extension as the final group.

[0169] The word line grouping device 20 may terminate the group size adjustment and fix the group when the read performance values of all groups are satisfied with the second threshold value TH2.

[0170] The maximum value or the minimum value of the word line addresses included in each fixed group may be output a separator of each group.

[0171] Accordingly, the word line grouping device 20 may group the plurality of word lines included in the memory block so that data of the word lines are read by using the representative read voltage.

[0172] The above described embodiments of the present disclosure are intended to illustrate and not to limit the embodiments of the present disclosure. Various alternatives and equivalents are possible. The invention is not limited by the embodiments described herein. Nor is the invention limited to any specific type of semiconductor device. Other additions, subtractions, or modifications are obvious in view of the present disclosure and are intended to fall within the scope of the appended claims. Furthermore, the embodiments may be combined to form additional embodiments.

## Claims

1. A storage apparatus comprising: a memory device including a plurality of word lines; and a word line grouping device configured to group the plurality of word lines into a certain number of groups, so that a read performance value, obtained by reading data of word lines included in a same group by using a representative read voltage, is satisfied with a set tolerance value.
2. The storage apparatus of claim 1, wherein the word line grouping device includes: a representative read voltage decision circuit configured to determine the representative read voltage of each group, by which the read performance value is optimized; and a group size adjustment circuit configured to adjust a size of each group so that the read performance value of each group is satisfied with the set tolerance value.
3. The storage apparatus of claim 1, wherein the read performance value includes a maximum fail bit count among fail bit counts of word lines of each group for a plurality of candidate read voltages when data of the word lines in each group are read by using at least a portion of the plurality of candidate read voltages.
4. The storage apparatus of claim 3, wherein the word line grouping device is configured to determine, as the representative read voltage, a candidate read voltage which minimizes the maximum fail bit count.
5. The storage apparatus of claim 1, wherein the read performance value includes a read pass rate which is a ratio of a word line number having a fail bit count within error correction capability to a total word line number of each group for a plurality of candidate read voltages when data of the word lines in each group are read by using at least a portion of the plurality of candidate read voltages.
6. The storage apparatus of claim 5, wherein the word line grouping device is configured to determine, as the representative read voltage, a candidate read voltage which maximizes the read pass rate.
7. The storage apparatus of claim 1, wherein the word line grouping device is configured to fix a size of a first group of the groups when a read performance value of the first group is satisfied with the set tolerance value and the read performance value of the first group is satisfied with a criterion value which is set to terminate group size adjustment.
8. The storage apparatus of claim 1, wherein the word line grouping device is configured to extend a size of a second group of the groups when a read performance value of a second group is satisfied with the set tolerance value and a read performance value of the second group is not satisfied with a criterion value which is set to terminate group size adjustment.
9. The storage apparatus of claim 1, wherein the word line grouping device is configured to reduce a size of a third group of the groups when a read performance value of the third group is not satisfied with the set tolerance value.
10. The storage apparatus of claim 1, wherein the word line grouping device is configured to fix sizes of all groups when read performance values of all groups are satisfied with the set tolerance value.
11. An operating method of a storage apparatus which includes a memory device including a plurality of word lines; and a storage controller configured to control the memory device, the method comprising: the storage controller grouping a plurality of word lines into a certain number of groups; and the storage controller regrouping the plurality of word lines so that a read performance value obtained by reading data of word lines included in a same group by using a representative read voltage, is satisfied with a set tolerance value.
12. The method of claim 11, further comprising determining the representative read voltage by which the read performance value of each group is optimized, wherein the regrouping of the plurality of word lines includes adjusting a size of each group so that the read performance value of the group is satisfied with the set tolerance value when the data are read by using the representative read voltage.
13. The method of claim 11, wherein the read performance value is determined to include a maximum fail bit count among fail bit

counts of word lines of each group for a plurality of candidate read voltages when data of the word lines in each group are read by using at least a portion of the plurality of candidate read voltages.

**14.** The method of claim 13, further comprising determining, as the representative read voltage, a candidate read voltage which minimizes the maximum fail bit count.

**15.** The method of claim 11, wherein the read performance value is determined to include a read pass rate which is a ratio of a word line number having a fail bit count within error correction capability to a total word line number in each group for a plurality of candidate read voltages when data of the word lines in each group are read by using at least a portion of the plurality of candidate read voltages.

**16.** The method of claim 15, further comprising determining a candidate read voltage which maximizes the read pass rate as the representative read voltage.

**17.** The method of claim 11, further comprising fixing a size of a first group of the groups when a read performance value of the first group is satisfied with the set tolerance value and the read performance value of the first group is satisfied with a criterion value which is set to terminate group size adjustment.

**18.** The method of claim 11, further comprising extending a size of a second group of the groups when a read performance value of a second group is satisfied with the set tolerance value and a read performance value of the second group is not satisfied with a criterion value which is set to terminate group size adjustment.

**19.** The method of claim 11, further comprising reducing a size of a third group of the groups when a read performance value of the third group is not satisfied with the set tolerance value.

**20.** The method of claim 11, further comprising fixing sizes of all groups when read performance values of all groups are satisfied with the set tolerance value.

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