DRIVING SIGNAL-BASED REDUCTION OF GATE SWITCHING INSTABILITY FOR SEMICONDUCTOR POWER SWITCH

Abstract

An electrical circuit is usable as part of an electric drive system having a direct current (DC) power supply, a DC link capacitor, and an inverter circuit for powering an electric machine. The electrical circuit includes a driver circuit connected to a gate terminal of a power switch, e.g., a silicon carbide power metal-oxide semiconductor field effect transistor (SiC power MOSFET). The power switch has a gate-to-source voltage responsive to a driving voltage, and a degradation interval during which the gate-to-source voltage increases from a relatively low voltage level below a threshold voltage toward a relatively high voltage level above the threshold voltage. The driver circuit is operable to shape a trajectory of the driving voltage over the degradation interval such that the driving voltage is non-linear across over a full duration of the degradation interval.

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATIONS [0001] The present application claims the benefit of priority to U.S. Provisional Application No. 63/555,563 filed on Feb. 20, 2024, which is hereby incorporated by reference in its entirety.

TECHNICAL FIELD
[0002] The present disclosure relates generally to the switching control of a voltage-controlled semiconductor power switch, and in particular to a gate drive circuit and associated methodology for controlling a conductive state of the power switch.

BACKGROUND
[0003] High-voltage electric drive systems typically include a direct current (DC) voltage bus connected to a DC power supply, for instance a lithium-ion or nickel-metal hydride battery pack. One or more single-phase or polyphase electric motors may be driven by inverter circuitry connected to the DC voltage bus. Resident semiconductor power switches of the inverter circuitry, as well as of other circuits of the electric drive system such as voltage rectifiers and DC-DC converters, employ voltage-controlled semiconductor switches to generate a desired voltage or current waveform.

[0004] Voltage-controlled power switches are available in various constructions for use in a wide range of power electronic applications. For instance, switching circuits of an electric drive system typically use metal-oxide semiconductor field effect transistors (MOSFETs) as high-frequency switching devices having drain, source, and gate terminals, with the gate terminal acting as a control terminal when operating the power switch. That is, a gate-to-source voltage is determined via provision of a driving voltage to the gate terminal by a driver circuit. This action alters a drain-to-source resistance level of the power switch and changes its ON/OFF conductive state.

SUMMARY
[0005] The solutions described herein are intended to reduce gate switching instability (GSI) of a semiconductor power switch in an electrical circuit. According to JEDEC® Publication No. JEP195, "Guideline for Evaluating Gate Switching Instability of Silicon Carbide Metal-Oxide-Semiconductor Devices for Power Electronic Conversion", published on Feb. 1, 2023 by the JEDEC® Solid State Technology Association, GSI refers to the undesirable phenomenon of a "threshold instability of a MOS device operating in a gate switching mode between a voltage much above the threshold voltage and below the flatband voltage", and thus "describes the degradation in the conduction path of the device driven by the switching event." This phenomenon is referred to in the art by different terms, including "alternating current (AC) gate-bias stress" and "gate-switching stress", with the term "GSI" used herein for illustrative consistency. Reduction of GSI is accomplished in various manners using the solutions as described below.

[0006] In particular, an electrical circuit is described herein that includes a semiconductor power switch and an associated driver circuit. The power switch, which may be optionally constructed as a metal-oxide semiconductor field-effect transistor (MOSFET), for instance a silicon carbide (SiC) power MOSFET, has a threshold voltage (V_{TH}), a gate-to-source voltage (V_{GS}) responsive to a driving voltage (V_{DR}), and a degradation interval (t_{deg}). During the degradation internal, the gate-to-source voltage increases from a relatively low voltage level (V_{GS_L}) that has a lower magnitude than/is below the threshold voltage. In response to the driving voltage, the gate-to-source voltage increases toward a relatively high voltage level

(V.sub.GS_H) having a magnitude that exceeds the threshold voltage. The driver circuit, which is connected to a gate terminal of the power switch, is used to shape or generate a non-linear trajectory of the driving voltage over a full duration of the degradation interval.

[0007] The driver circuit may be optionally constructed as a multi-level driver circuit, e.g., one having three or more driver circuits.

[0008] The non-linear trajectory of the driving voltage over the full duration of the degradation interval may include multiple ramped or stepped segments, or the trajectory may be constructed as a periodic oscillating trajectory. The latter implementation may be accomplished using a resonant tank in one or more embodiments.

[0009] The electrical circuit may also include a reducing circuit configured to reduce a rate of change

[00001]$(\frac{d_{V_{Gs}}}{dt})$

of the above-noted gate-to-source voltage during the degradation interval. A possible implementation of the reducing circuit includes a bleeding resistor (R.sub.B) coupled to a gate terminal of an N-type MOSFET, a diode connected to a drain terminal of the N-type MOSFET, and a capacitance divider connected to the bleeding resistor and the N-type MOSFET.

[0010] Also disclosed herein is an electric drive system. The electric drive system may include a direct current (DC) power supply connected in parallel with a DC link capacitor, an inverter circuit connected to the DC link capacitor, a polyphase electric machine connected to the inverter circuit, a rotary output member coupled to the polyphase electric machine, and a load coupled to the rotary output member.

[0011] In a possible embodiment, the inverter circuit includes a plurality of silicon carbide (SiC) power MOSFETs. Each respective one of the SiC power MOSFETs has a threshold voltage, a gate-to-source voltage responsive to a driving voltage, and a degradation interval during which the gate-to-source voltage increases from the relatively low voltage level toward the relatively high voltage level as summarized above. In this particular implementation, a plurality of driver circuits are connected to a respective gate terminal of a different one of the SiC power MOSFETs. The driver circuits are collectively operable to shape or generate a non-linear trajectory of the driving voltage over the full duration of the degradation interval.

[0012] The above summary is not intended to represent every embodiment or aspect of the present disclosure. Rather, the foregoing summary exemplifies certain novel aspects and features as set forth herein. The above noted and other features and advantages of the present disclosure will be readily apparent from the following detailed description of representative embodiments and modes for carrying out the present disclosure when taken in connection with the accompanying drawings and the appended claims.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The drawings described herein are for illustrative purposes only, are schematic in nature, and are intended to be exemplary rather than to limit the scope of the disclosure.

[0014] FIG. **1** illustrates an exemplary inverter circuit for energizing a polyphase electric machine, with the inverter circuit using voltage-controlled power switches controlled in accordance with the present disclosure to reduce gate switching instability (GSI).

[0015] FIG. **2** is a time plot of a gate-to-source voltage (V.sub.GS) and a gate current (I.sub.G) describing degradation intervals as used herein.

[0016] FIG. **3** illustrates a baseline driving voltage (V.sub.R) and gate-to-source voltage as it might appear absent the present teachings.

[0017] FIGS. **3**A, **3**B, and **3**C illustrate an exemplary driving signal, driver circuit, and voltage

pulses for reducing GSI in accordance with an aspect of the disclosure.

[0018] FIGS. **4**A, **4**B, and **4**C illustrate an exemplary driving signal, driver circuit, and voltage pulses for reducing GSI via one or more ramped segments in accordance with another aspect of the disclosure.

[0019] FIGS. **5**A, **5**B, and **5**C illustrate an exemplary driving signal, driver circuit, and voltage pulse for reducing GSI via a succession of stepped segments in accordance with another aspect of the disclosure.

[0020] FIG. **6** illustrates an exemplary driving signal and driver circuit for reducing GSI via a periodic oscillatory signal.

[0021] FIGS. **7**A and **7**B are a respective half-bridge circuit diagram and pulse train in accordance with an aspect of the disclosure.

[0022] The present disclosure may be modified or embodied in alternative forms, with representative embodiments shown in the drawings and described in detail below. Inventive aspects of the present disclosure are not limited to the disclosed embodiments. Rather, the present disclosure is intended to cover alternatives falling within the scope of the disclosure as defined by the appended claims.

DETAILED DESCRIPTION

[0023] With reference to the drawings, wherein like reference numbers refer to the same or similar components throughout the several views, an electric drive system **10** is illustrated in FIG. **1** having an exemplary polyphase rotary electric machine (M.sub.E) **12**. The electric drive system **10** may include semiconductor power switches **20** each driven by gate-to-source voltage (V.sub.GS) from a corresponding driver circuit **15** as set forth herein, with the driver circuits (DR) **15** and power switches **20** together forming an electrical circuit **21** (e.g., FIG. **3**B). For simplicity, the power switch **20** labeled S**3** is shown driven by a driver circuit **15**. In an actual implementation, each of the power switches **20** will be driven by a corresponding driver circuit **15**, as appreciated in the art. Also, although the power switches **20** are shown as part of an exemplary alternating current (AC)-to-direct current (DC) inverter circuit **11** in FIG. **1**, those skilled in the art will appreciate that other power electronic devices may benefit from use of the power switches **20**, including for instance voltage rectifiers, DC-DC converters, and the like, and therefore the present teachings are not limited to the representative use illustrated in FIG. **1**.

[0024] The power switches **20** may be embodied as any voltage-controlled switch that is susceptible, absent the present teachings, to undesirable effects of gate switching instability (GSI). The power switches **20** as contemplated herein may be embodied as wide bandgap (WBG) switches, for instance silicon carbide (SiC) power MOSFETs. Other voltage-controlled power switches that may benefit from the present teachings include, by way of example and not of limitation, gallium nitride (GaN) switches, insulated gate bipolar transistors (IGBTs), and silicon-controlled rectifiers (SCRs). For illustrative consistency, the power switches **20** will be described hereinbelow in a representative embodiment as SiC power MOSFETs without limiting the power switches **20** to any particular construction unless otherwise specified.

[0025] The rotary electric machine **12** may be embodied as an electric traction motor for powering a load in a stationary or mobile system in one or more embodiments, includes the phase leads **14**, with each of the phase leads **14** being connectable to the inverter circuit **11**. For example, a typical three-phase embodiment of the electric machine **12** includes three phase leads **14**, which in turn are individually labeled "a", "b", and "c" to indicate nominal a, b, and c phases. The electric drive system **10** also includes a positive voltage rail **16**.sup.+, a negative voltage rail **16**.sup.− (electrical ground), and a DC link capacitor **17**. The DC link capacitor **17** is connected to the respective positive and negative voltage rails (**16**.sup.+, **16**.sup.−) and configured to receive a DC voltage waveform from a DC voltage supply **18**, for instance a multi-cell electrochemical battery pack of an application-suitable battery chemistry such as lithium-ion, lithium-metal, nickel-metal hydride, etc.

[0026] Within the inverter circuit **11** of FIG. **1**, a plurality of the power switches **20**, also individually labeled S**1**, S**2**, S**3**, S**4**, S**5**, and S**6**, are arranged in multiple switching pairs SP**1**, SP**2**, and SP**3**, i.e., power switches (S**1**, S**2**), (S**3**, S**4**), and (S**5**, S**6**), respectively. Each respective switching pair SP**1**, SP**2**, and SP**3** is connected to the DC link capacitor **17** and a corresponding one of the phase leads **14** of the electric machine **12**. That is, the switching pairs SP**1**, SP**2**, and SP**3** are respectively connected to the nominal a, b, and c phase leads **14** at nodes N**1**, N.sub.2, and N.sub.3. Each power switch **20** is voltage-controlled by a corresponding gate drive circuit, one of which is schematically illustrated in FIG. **1** for simplicity.

[0027] During normal switching operations, the phase leads **14** are energized by switching control operation of the inverter circuit **11** to generate motor output torque (To) on a rotary output member **120**. Being voltage-controlled devices, however, the power switches **20** may experience GSI during operation. Such a condition may be more prevalent in certain constructions of the power switches **20**, with trench gate SiC MOSFETs in particular being susceptible to the effects of GSI. However, GSI appears to at least some extent in all voltage-controlled power switches, and therefore the present teachings are not limited to SiC MOSFETs in general or trench gate SiC MOSFETs in particular.

[0028] Referring briefly to FIG. **2**, in which time in seconds (s) is illustrated on the horizontal axis and voltage and current magnitude in volts (V) and amps (A) are illustrated on the vertical axis, gate switching instability (GSI) is a significant degradation mechanism for long term operation of voltage-controlled power switches. GSI as contemplated herein is a dynamic effect occurring during regular gate driving, when the gate-to-source voltage (V.sub.GS) has fast ramp times of less than about 200 nanoseconds (ns), a

[00002] $\frac{d_{V_{GS}}}{dt}$

of about 0.1 volts/ns (V/ns) to 0.3 V/ns, and a peak gate current (I.sub.PK) of about 1 ampere or more. Among other potential issues, GSI can cause permanent shifts in threshold voltage (V.sub.TH) and drain-source ON state resistance (R.sub.dson) (not depicted in FIG. **2**) with operational time, with the shift being recoverable only at annealing temperatures exceeding about 400° Celsius (C). Practically speaking, however, a junction temperature of 400° C. will never be reached during real applications, and thus degradation is non-recoverable.

[0029] Degradation occurs in the turn-on, and is defined by the interval (t.sub.deg) where the gate-to-source voltage V.sub.GS (trace **24**) ramps from a relatively low voltage level (V.sub.GS_L) to the threshold voltage V.sub.TH, i.e., the particular value of V.sub.GS that is needed to turn on the power switch **20** for linear and saturation regions of operation as appreciated in the art, and continues toward a relatively high voltage level (V.sub.GS_H). Threshold voltages (V.sub.TH) of about 3V to about 6V are typical. The relatively high voltage level, V.sub.GS_H, lies between the relatively low voltage level (V.sub.GS_L) and the threshold voltage (V.sub.TH). During the degradation interval (t.sub.deg), a more negative value of V.sub.GS_L and a larger value of

[00003] $\frac{d_{V_{GS}}}{dt}$

enhances the above-noted degradation. Gate current I.sub.G (trace **25**) is likewise shown in FIG. **2**, with peak gate current (I.sub.PK) and minimum gate current (I.sub.MIN) also illustrated. Solutions to reducing

[00004] $\frac{d_{V_{GS}}}{dt}$,

such as increasing gate resistance, tend to penalize transient power loss and are therefore suboptimal. In contrast, the present solutions incorporate a new driving method to reduce

[00005] $\frac{d_{V_{GS}}}{dt}$

without impacting switching losses, thereby reducing GSI in the controlled power switches **20** illustrated in FIG. **1**.

[0030] Referring briefly to FIG. **3**, which illustrates a driving voltage (V.sub.DR) signal as trace **31** and a gate-to-source voltage (V.sub.GS) signal (trace **33**) at gate and source terminals of a

controlled power switch when not connected to a load, the driving voltage (V_{DR}) is shown rising linearly from a relatively low voltage level (V_{DR_L}), e.g., about −3V to about −8V, toward a relatively high voltage level (V_{DR_H}), typically about 15V to about 20V. This rise occurs over a rising ramp interval (t_r). The driving voltage (V_{DR}) is sustained at the relatively high voltage level (V_{DR_H}) for a calibrated duration before returning to the relatively low voltage level (V_{DR_L}), with the trajectory occurring over a falling ramp interval (t_f).

[0031] The corresponding gate-to-source voltage (V_{GS}) is illustrated as rising parabolically from the relatively low voltage level (V_{GS}) through the defined threshold voltage (V_{TH}) over the above-noted degradation interval (t_{deg}), with V_{GS_L} being about −3V to about −8V (as with V_{DR_L} as noted above), continuing in this manner until reaching the relatively high voltage level (V_{GS_H}), e.g., about 15V to about 20V. The gate-to-source voltage (V_{GS}) thereafter drops rapidly back to the relatively low voltage level (V_{GS_L}) when the power switch **20** is commanded OFF, i.e., with the start of the falling ramp interval (t_f) of the driving voltage signal (V_{DR}).

[0032] In contrast, trace **30** of FIG. **3**A represents an alternative driving voltage (V_{DR}) signal from the driver circuit **15** of FIG. **1** to a gate contact of a corresponding power switch **20**. The driving voltage (V_{DR}) rises from the level of the relatively low voltage (V_{DR_L}) to that of the relatively high voltage (V_{DR_H}) over the above noted degradation interval (t_{deg}), i.e., the turn-on interval of the power switch **20**. In accordance with the disclosure, the ramp from V_{DR_L} to V_{DR_H} is non-linear over the full duration of the degradation interval (t_{deg}), and thus is not constant. That is, while portions or segments of the generated trajectory may increase linearly during the degradation interval (t_{deg}), the trajectory as a whole—taken over the full duration of the degradation interval (t_{deg})—is non-linear. Instead, the degradation interval (t_{deg}) is separated into several intervals t_{r1}, t_{relax}, and t_{r2} as shown, with r in this instance indicating a rising trajectory. The relatively high voltage level (V_{DR_H}) is then maintained for a predetermined duration until the driving voltage (V_{DR}) indicated by trace **30** ramps back down to the level of the relatively low voltage (V_{DR_L}), which occurs over the falling duration t_f, with f here representing a falling trajectory.

[0033] Trace **32** of FIG. **3**A represents the gate-to-source voltage (V_{GS}), likewise with representative low and high voltages V_{GS_L} and V_{GS_H}, respectively. The threshold voltage (V_{TH}) is also illustrated as the minimum voltage required to turn on the power switch **20** and thereby cause a current to flow between source and drain terminals. The non-linear trajectory of trace **30** over the full duration of the degradation interval (t_{deg}) may include a plateau segment **34**, with a pair of ramped segments (R**1**, R**2**) are connected by the plateau segment **34**. Relative to trace **33** of FIG. **3**, therefore, the resulting trajectory of trace **32** provides a reduced level of GSI.

[0034] Implementation of traces **30** and **32** of FIG. **3**A may proceed by adding a relax time interval (t_{relax}) to a scheme in which $V_{TH} > V_{DR\_R} > V_{DR\_L}$. The time to ramp the driving voltage V_{DR} from V_{DR_L} to V_{DR_R} (i.e., t_{r1}) added to the $V_{DR\text{-}R}$ plateau time (t_{relax}), is longer than the time normally taken to ramp directly from V_{DR_L} to V_{DR_H}, i.e., $t_{r1} + t_{relax} > t_r$, with the actual extent of the increase being application dependent and customizable. The time to ramp the driving voltage (V_{DR}) from V_{DR_R} to V_{DR_H}, i.e., t_{r2}, is typically not longer than t_r, i.e., $t_{r2} \leq t_r$. Moreover, the time to ramp V_{GS} from V_{GS_L} to V_{TH}, i.e., t_{deg}, is longer relative to that of FIG. **3**, thus reducing GSI. The time to ramp the driving voltage (V_{DR}) from V_{TH} to V_{GS_H} is also equal to or less than the baseline level of FIG. **3**, which ensures that switching losses are not increased when the power switches **20** of FIG. **1** operate on a load. In general terms, $t_r \sim t_f \sim t_{r2} \sim 1\text{-}20$ ns, while $t_{r1} \sim t_{relax} \sim 10\text{-}200$ ns.

[0035] A representative embodiment of the driver circuit **15** suitable for providing the trajectories

of FIG. **3**A is shown in FIG. **3**B. In lieu of a single driver, in this embodiment the driver circuit **15** is constructed as respective first and second driver circuits **150** and **250** (DR**1** and D**2**). For the power switch **20** having a gate terminal (G), a source terminal (S), and a drain terminal (D), the respective first and second driver circuits **150** and **250** are connected to the respective gate terminal (G) and source terminal (S), with the connection to the gate terminal (G) being through a gate resistor (R.sub.G) **35** of the electrical circuit **21** (see FIG. **3**B), possibly as part of the driver circuit **15**.

[0036] The first and second driver circuits **150** and **250** each have a corresponding local voltage source **180** or **280**. For example, V.sub.DR_R of FIG. **3**A may be provided by the local voltage source **280**, with the low voltage (V.sub.DR_L) provided by another local voltage source **380**. Voltage source **180** has a corresponding voltage level of V.sub.DR_H-V.sub.DR_R. Input pulses (V.sub.IN1 and V.sub.IN2) are provided to the respective driver circuits **150** and **250** to generate the pulses **36**A and **36**B of FIG. **3**C. Note that pulse **36**A, i.e., V.sub.IN1, lags pulse V.sub.IN2 by the duration of t.sub.relax shown in FIG. **3**A and described above. An optional resonant tank **46** may be added to the driver circuit **15** to produce an oscillatory signal as described below with reference to FIG. **6**.

[0037] The approach of FIGS. **3**A-C may be modified in other embodiments within the scope of the disclosure. For instance, as shown by trajectories of traces **300** and **320** (V.sub.DR and V.sub.GS, respectively) in FIG. **4**A one may implement the approach of FIG. **3**A with the interval t.sub.relax tending to zero, such that there is a resulting lack of a plateau in the trajectories of V.sub.DR and V.sub.GS. In other words, the interval t.sub.r1 forms most of the degradation interval t.sub.deg, with the remainder of t.sub.deg being the duration t.sub.r2.

[0038] A representative driver circuit **15**A suitable for providing the trajectories of FIG. **4**A is shown in FIG. **4**B. The driver circuit **15**A is constructed as the first driver circuit **150** as shown. For the power switch **20** having a gate terminal (G), a source terminal (S), and a drain terminal (D), the first driver circuit **150** is connected to the gate terminal (G) through the gate resistor (R.sub.G) **35**. Voltage source **480** provides the relatively high voltage (V.sub.DR_H) to the first driver circuit **150**, with the low voltage (V.sub.DR_L) provided via the voltage source **380**. In this single-driver implementation, a

[00006] $\frac{d_{V_{GS}}}{dt}$

reducing circuit **38** is included to reduce

[00007] $\frac{d_{V_{GS}}}{dt}$

when V.sub.GS<V.sub.TH.

[0039] As shown in FIG. **4**C, the reducing circuit **38** of FIG. **4**B for reducing

[00008] $\frac{d_{V_{GS}}}{dt}$

may be implemented as a reducing circuit **380** having various circuit components. For example, the reducing circuit **380** may include a MOSFET **200**, e.g., a low-voltage N-type MOSFET, configured to interrupt the V.sub.GS ramp rate to the power switch **20** for a short interval, thus generating t.sub.relax. A low-voltage diode **40** may be used to help avoid current to the first driver circuit **150** of FIG. **4**B, with the low-voltage diode **40** acting as a parasitic element when the driver signal is negative. A capacitance divider **42**, shown as capacitors C.sub.1 and C.sub.2, are used to adapt the amplitude of the driver signal to activate the power switch **20**. A bleeding resistor (R.sub.B) **44** may be connected to the gate (G) as shown to ensure the power switch **20** is only in an ON state for a short time interval. Other implementations of the reducing circuit **38** of FIG. **4**B may be contemplated within the scope of the disclosure, and therefore the approach of FIG. **4**C is exemplary and non-limiting of the present teachings.

[0040] Referring now to FIG. **5**A, traces **300**A and **320**A represent yet another alternative implementation for shaping trajectories of the driving voltage (V.sub.DR) and the gate-to-source voltage (V.sub.GS). In this approach, the rise in the driving voltage (V.sub.DR) occurs over the

degradation interval (t.sub.deg) as a series of steps and ramps. That is, for trace **300**A, i.e., the low-to-high voltage transition from V.sub.DR_L to V.sub.DR_H, intermediate voltage levels V.sub.DR_R1 may be attained over duration t.sub.r1, with the interval t.sub.relax being used to complete multiple step increases, possibly at different voltage levels and different time intervals, i.e., to levels V.sub.DR_R2 and V.sub.DR_R3. Trace **300**A may then be ramped to the relatively high voltage, V.sub.DR_H, over the interval t.sub.r2, with the driving voltage (V.sub.DR) thereafter plateauing until the power switch **20** is turned off over falling interval t.sub.f. The corresponding effect on trace **320**A over the degradation interval (t.sub.deg) is a series of lobes or curved steps as the gate-to-source voltage (V.sub.GS) increases from the relatively low voltage (V.sub.GS_L) to the threshold voltage (V.sub.TH).

[0041] Any driving voltage levels (V.sub.DR_Ri) used to execute the series of steps should fulfill the condition V.sub.TH>V.sub.DR_Ri>V.sub.DR_L. The sum of the times needed to ramp between such steps and the plateau times for each V.sub.DR_Ri may be defined as follows:

[00009]$t_{relax} : t_{r1} + t_{relax} > t_r$

[0042] A possible hardware implementation usable for achieving the trajectories of traces **300**A and **320**A of FIG. **5**A is shown in FIG. **5**B. Here, the driver circuit **15**B may be constructed as multiple driver circuits **150**, **250**, . . . , **250***n*, i.e., DR**1**, DR**2**, . . . DRn. As explained above, the first driver circuit **150** is connected to the power switch **20** via the gate resistor **35**. Individual voltage sources **480** and **580** may be connected to respective driver circuits **150**, **250**, . . . , **250***n* as shown, with the voltage sources **480** and **580** having the indicated voltage values, i.e., V.sub.DR_Ri (for voltage sources **480**) and V.sub.DR_H- . . . -V.sub.DR_Ri-1-V.sub.DR_Ri. Use of the driver circuit **15**B will result in pulses **36**A, **36**B, and **36***n* of FIG. **5**C, i.e., V.sub.IN1, V.sub.INi-1, and V.sub.INi, for a non-limiting embodiment using three drivers. The pulses **36**A, **36**B, . . . , **36***n* initiate at different times to provide the desired trajectories of FIG. **5**A, for instance with pulse **36**A commencing after t.sub.relax, and pulse **36**B commencing earlier than pulse **36**A, i.e., after a duration t.sub.relaxi after initiation of pulse **36***n*.

[0043] Referring now to traces **300**B and **320**B of FIG. **6**, the present teachings may be implemented as a periodic oscillatory signal in lieu of the above-described stepped and/or ramped profiles of FIGS. **3**A, **4**A, and **5**A. That is, rather than using a driving voltage (V.sub.DR) and gate-to-source voltage (V.sub.GS) with linear trajectories over the full duration of the degradation interval (t.sub.deg), it is possible to generate the periodic oscillatory signal with a medium driving voltage, i.e., V.sub.DR_R.

[0044] By way of an example and not of limitation, and referring briefly again to FIG. **3**B, the driver circuit **15**B may be used to produce the oscillatory signal of FIG. **6** by adding the resonant tank **46** to its topology. The output of the second driver circuit **250** may be connected to the resonant tank **46** in this embodiment, such that the resonant tank **46** is connected to the second driver circuit **250** and to the source terminal (S) of the power switch **20**. Gain control of the resonant tank **46** may be used to generate the oscillatory signal of FIG. **6**, as appreciated in the art, by filtering out harmonics and outputting a sine wave.

[0045] As appreciated in the art, the resonant tank **46** (also referred to in the art as a resonant circuit or tuned circuit) is an inductor-capacitor (LC) circuit that can determine the oscillation frequency and sustain oscillation via positive feedback. The resonant tank **46** may be constructed, for example, from a capacitor, a resonant inductor, a magnetizing inductor, and a transformer. The resonant inductor in a possible implementation is arranged in series with the resonant capacitor and transformer, while the magnetizing inductor is connected in parallel with the resonant capacitor and transformer. The resonant tank **46** has the ability to resonate at a resonant frequency

[00010]$f_{res} = \frac{1}{(2 \ \sqrt{LC})}$.

At the resonant frequency, the inductive and capacitive reactance are equal in magnitude and opposite in sign, thus canceling each other out. As a result, the impedance of the resonant tank **46** is

purely resistive and determined solely by losses in the inductors and capacitor.

[0046] Referring now to FIG. **7**A, a half-bridge **50** may be used to implement a DC-DC converter in lieu of the inverter circuit **11** of FIG. **1**, with the half-bridge circuit **50** controlled via any of the present driving signal methodologies described above. A signal may be generated as the driving voltage (V.sub.DR1, V.sub.DR2) for each of the power switches **20** used in the half-bridge **50**, in this instance the power switches **20**A and **20**B. Driver circuits **15-1** and **15-2** may be used to provide a driving voltage (V.sub.DR1, V.sub.DR2) to the respective power switches **20**A and **20**B. A load resistance (R.sub.L) **135** represents the resistance of a coupled load. Other components of the representative half-bridge **50** include an inductor (L) **37** and the voltage source **18**.

[0047] The half-bridge **50** of FIG. **7**A may therefore be used to generate the pulse trains **35**D and **35**E of FIG. **7**B. Here, t.sub.r1 and t.sub.relax are embedded within the deadtime (DT), i.e., the period during which neither of the power switches **20**A and **20**B of the half-bridge circuit **50** conducts. As noted above, representative values for tri and t.sub.relax are about 10 ns to about 200 ns. By comparison, deadtime (DT) may be on the order of about 300 ns to about 800 ns. Thus, FIG. **7**B is not drawn to scale, but rather is exaggerated for clarity.

[0048] The solutions set forth above are therefore usable for reducing GSI in SiC power MOSFETs and other voltage-controlled power switches **20**. By implementing the various drive methodologies of FIGS. **3**A, **4**A, **5**A, and **6**, e.g., in a half-bridge **50** as shown in FIG. **7**A, aboard the electric drive system **10** of FIG. **1**, or in other electrical systems, one can avoid permanent shifts in threshold voltage (V.sub.TH) and on-state resistance (R.sub.dson). This is accomplished by reducing

[00011]$\frac{d_{V_{Gs}}}{dt}$

without impacting switching losses. These and other attendant benefits will be appreciated by those skilled in the art having the benefit of the present teachings.

[0049] While several modes for carrying out the many aspects of the present teachings have been described in detail, those familiar with the art to which these teachings relate will recognize various alternative aspects for practicing the present teachings that are within the scope of the appended claims. The above description and accompanying drawings are illustrative and exemplary of the entire range of alternative embodiments that an ordinarily skilled artisan would recognize as implied by, structurally and/or functionally equivalent to, or otherwise rendered obvious based upon the included content, and not as limited solely to those explicitly depicted and/or described embodiments.

[0050] Moreover, the present concepts expressly include combinations and sub-combinations of the described elements and features. The detailed description and the drawings are supportive and descriptive of the present teachings, with the scope of the present teachings defined solely by the claims. Words of approximation, such as "about," "almost," "substantially," "generally," "approximately," and the like, may each be used herein to denote "at, near, or nearly at," or "within 0-5% of," or "within acceptable manufacturing tolerances," or any logical combination thereof, for example.

Claims

1. An electrical circuit comprising: a power switch having a threshold voltage (V.sub.TH), a gate-to-source voltage (V.sub.GS) that is responsive to a driving voltage (V.sub.DR) to the power switch, and a degradation interval (t.sub.deg) during which the gate-to-source voltage (V.sub.GS) increases from a relatively low voltage level (V.sub.GS_L) below the threshold voltage (V.sub.TH) toward a relatively high voltage level (V.sub.GS_H) above the threshold voltage (V.sub.TH); and a driver circuit connected to a gate terminal of the power switch, wherein the driver circuit is operable to generate a non-linear trajectory of the driving voltage (V.sub.DR) over a full duration of the degradation interval (t.sub.deg).

2. The electrical circuit of claim 1, wherein the driver circuit is constructed as a multi-level driver circuit.

3. The electrical circuit of claim 2, wherein the multi-level driver circuit includes a three or more driver circuits.

4. The electrical circuit of claim 1, wherein the power switch includes a metal-oxide semiconductor field-effect transistor (MOSFET).

5. The electrical circuit of claim 4, wherein the MOSFET is a silicon carbide (SiC) power MOSFET.

6. The electrical circuit of claim 1, wherein the trajectory of the driving voltage (V.sub.DR) over the full duration of the degradation interval (t.sub.deg) includes multiple ramped segments.

7. The electrical circuit of claim 6, wherein a pair of the multiple ramped segments are connected by a plateau segment.

8. The electrical circuit of claim 1, wherein the trajectory of the driving voltage over the full duration of the degradation interval (t.sub.deg) includes multiple stepped segments.

9. The electrical circuit of claim 1, wherein the driver circuit includes a reducing circuit configured to reduce a rate of change ($\frac{d_{V_{GS}}}{dt}$) of the gate-to-source voltage (V.sub.GS) during the degradation interval (t.sub.deg).

10. The electrical circuit of claim 9, wherein the reducing circuit includes an N-type metal-oxide semiconductor field-effect transistor (MOSFET), a bleeding resistor (R.sub.B) coupled to a gate terminal of the N-type MOSFET, a diode connected to a drain terminal of the N-type MOSFET, and a capacitance divider that is connected to the bleeding resistor and the N-type MOSFET.

11. The electrical circuit of claim 1, wherein the driver circuit includes a resonant tank, and is operable to shape the trajectory of the driving voltage via the resonant tank such that the driving voltage (V.sub.DR) has a periodic oscillating trajectory over the full duration of the degradation interval (t.sub.deg).

12. An electric drive system, comprising: a direct current (DC) power supply; a DC link capacitor connected in parallel with the DC power supply; an inverter circuit connected to the DC link capacitor and having: a plurality of silicon carbide (SiC) power metal-oxide semiconductor field-effect transistors (MOSFETs), each respective one of the SiC power MOSFETs having a threshold voltage (V.sub.TH), a gate-to-source voltage (V.sub.GS) that is responsive to a driving voltage (V.sub.DR), and a degradation interval (t.sub.deg) during which the gate-to-source voltage (V.sub.GS) increases from a relatively low voltage level (V.sub.GS_L) below the threshold voltage (V.sub.TH) toward a relatively high voltage level (V.sub.GS_L) above the threshold voltage (V.sub.TH); and a plurality of driver circuits, each driver circuit of the plurality of driver circuits being connected to a respective gate terminal of a different one of the SiC power MOSFETs, wherein the driver circuits are collectively operable to generate a non-linear trajectory of the driving voltage (V.sub.DR) over a full duration of the degradation interval (t.sub.deg); a polyphase electric machine connected to the inverter circuit; a rotary output member coupled to the polyphase electric machine; and a load coupled to the rotary output member.

13. The electric drive system of claim 12, wherein the plurality of driver circuits are coupled to the respective gate terminal via a gate resistor.

14. The electric drive system of claim 12, wherein the trajectory of the driving voltage (V.sub.DR) over the full duration of the degradation interval (t.sub.deg) includes multiple ramped segments.

15. The electric drive system of claim 12, wherein the trajectory of the driving voltage (V.sub.DR) over the full duration of the degradation interval (t.sub.deg) includes multiple stepped segments.

16. The electric drive system of claim 12, wherein the plurality of driver circuits include a reducing circuit configured to reduce a rate of change ($\frac{d_{V_{GS}}}{dt}$) of the gate-to-source voltage (V.sub.GS) during the degradation interval (t.sub.deg).

17. The electric drive system of claim 12, wherein at least one of the driver circuits includes a

resonant tank that operable to generate the trajectory of the driving voltage (V.sub.DR) as a periodic oscillating trajectory over the full duration of the degradation interval (t.sub.deg).

18. An electrical circuit for use with a silicon carbide (SiC) power metal-oxide semiconductor field-effect transistor (MOSFET), comprising: a gate resistor; and a plurality of driver circuits coupled to a gate terminal of the SiC power MOSFET via the gate resistor, wherein the driver circuits are collectively operable to generate a driving voltage (V.sub.DR) to the SiC power MOSFET over a degradation interval (t.sub.deg) during which a gate-to-source voltage (V.sub.GS) increases from a relatively low voltage level (V.sub.GS_L) below a threshold voltage (V.sub.TH) of the SiC power MOSFET toward a relatively high voltage level (V.sub.GS_H) above the threshold voltage (V.sub.TH) of the SiC power MOSFET, such that a trajectory of the driving voltage (V.sub.DR) is non-linear across over a full duration of the degradation interval (t.sub.deg) and includes multiple ramped segments or multiple stepped segments.

19. The electrical circuit of claim 18, wherein the electrical circuit includes a reducing circuit configured to reduce a rate of change ($\frac{d_{V_{GS}}}{dt}$) of the gate-to-source voltage (V.sub.GS) during the degradation interval (t.sub.deg), and wherein the reducing circuit includes an N-type MOSFET, a bleeding resistor (R.sub.B) coupled to a gate terminal of the N-type MOSFET, a diode connected to a drain terminal of the N-type MOSFET, and a capacitance divider that is connected to the bleeding resistor and the N-type MOSFET.

20. The electrical circuit of claim 18, further comprising: a resonant tank, wherein the plurality of driver circuits is operable to output the driving voltage (V.sub.DR) with a periodic oscillating trajectory over the full duration of the degradation interval (t.sub.deg) via the resonant tank.