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(54) **POLYPHASE FILTER BANKS WITH RATIONAL DECIMATION / INTERPOLATION FACTOR**

(71) Applicant: **RAMON SPACE LTD.**, Yokneam Illit (IL)

(72) Inventors: **Hai Morgenstern**, Tel Aviv-Yafo (IL); **Eviatar Ohayon**, Shoham (IL)

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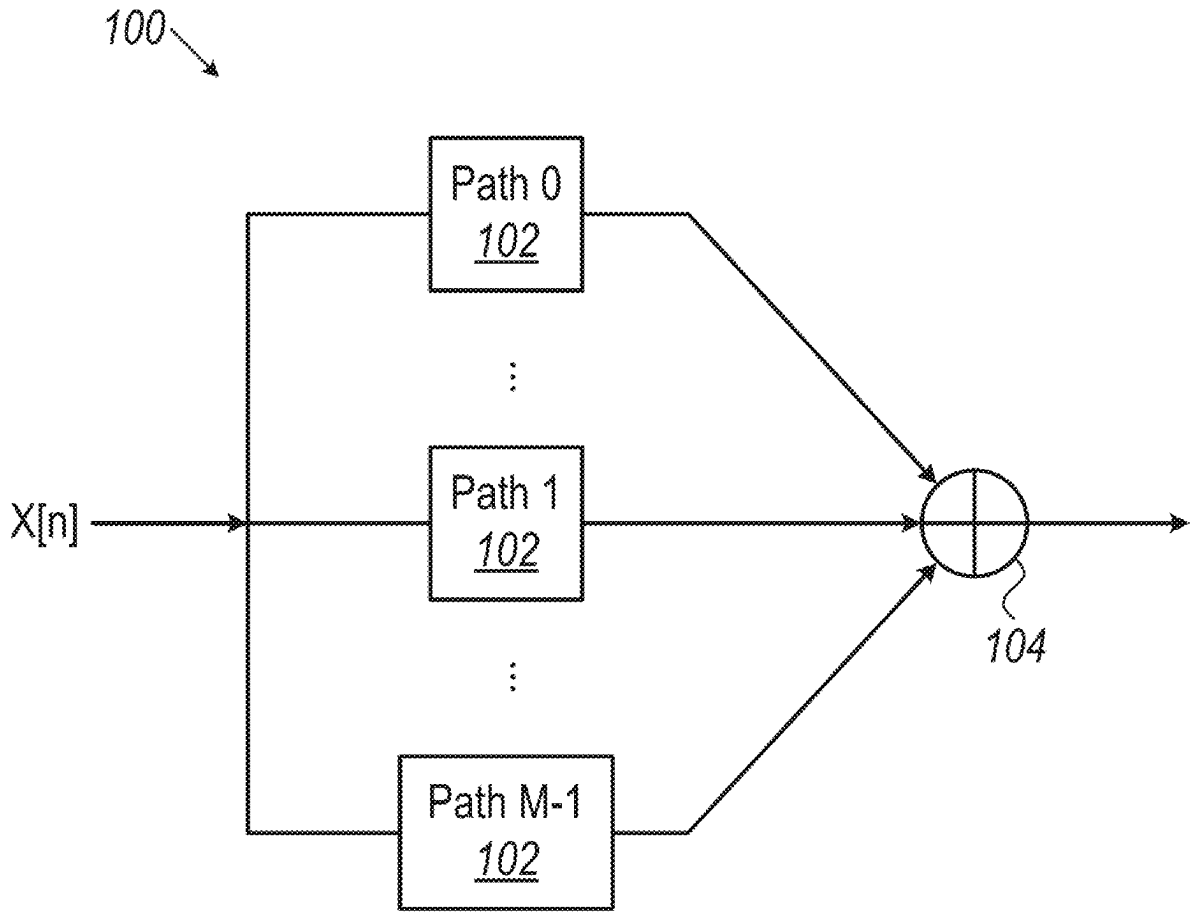
(57) **ABSTRACT**

An Analysis Polyphase Filter (APPF) for shifting a selected passband of an input signal to a passband signal, having a Q=M·B/A decimation factor, B and A being co-primes, the APPF comprising M·B Paths. Each path includes (i) M·B/A multiplication Sub-paths, and (ii) a Sub-path Fusion Circuit, which is configured to generate fused multiplication products responsively to a sum of the multiplication n products generated by each of the multiplication sub-paths.



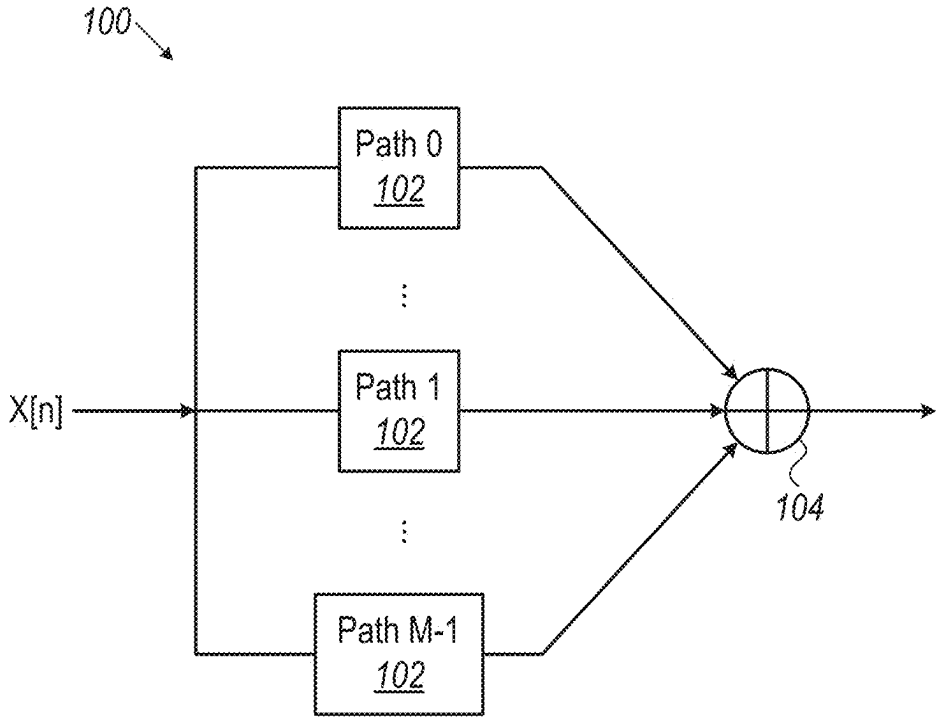


FIG. 1

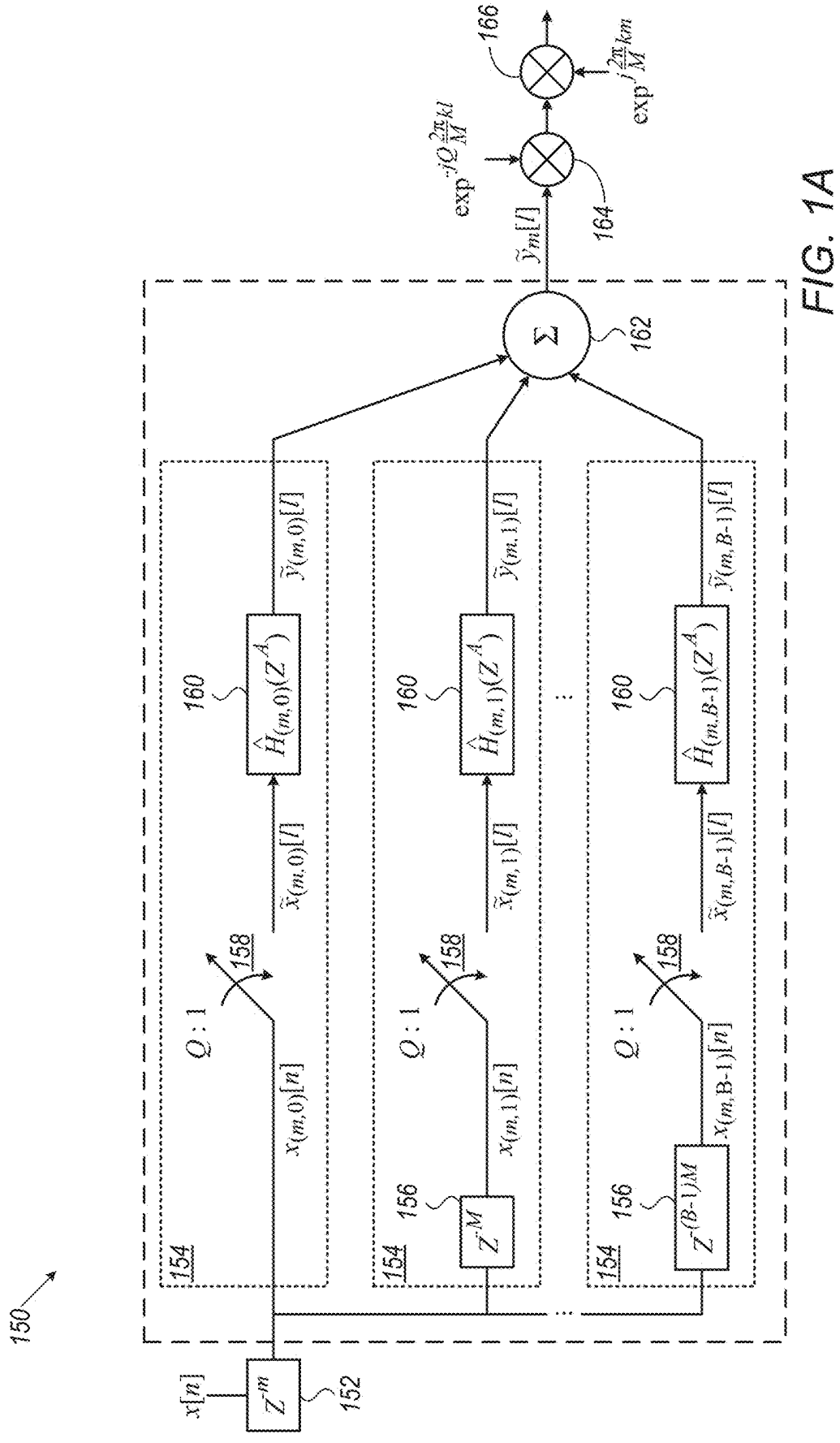

150
x[n]
Z^{-m}
152
154
156
158
160
162
164
166
Q : 1
Z^{M}
$Z^{(B-1)M}$
$\hat{H}_{(m,0)}(Z^{A})$
$\hat{H}_{(m,1)}(Z^{A})$
$\hat{H}_{(m,B-1)}(Z^{A})$
$x_{(m,0)}[n]$
$x_{(m,1)}[n]$
$x_{(m,B-1)}[n]$
$\tilde{x}_{(m,0)}[l]$
$\tilde{x}_{(m,1)}[l]$
$\tilde{x}_{(m,B-1)}[l]$
$\tilde{y}_{(m,0)}[l]$
$\tilde{y}_{(m,1)}[l]$
$\tilde{y}_{(m,B-1)}[l]$
$\tilde{y}_{m}[l]$
$\exp^{-jQ\frac{2\pi}{M}kl}$
$\exp^{j\frac{2\pi}{M}km}$

FIG. 1A

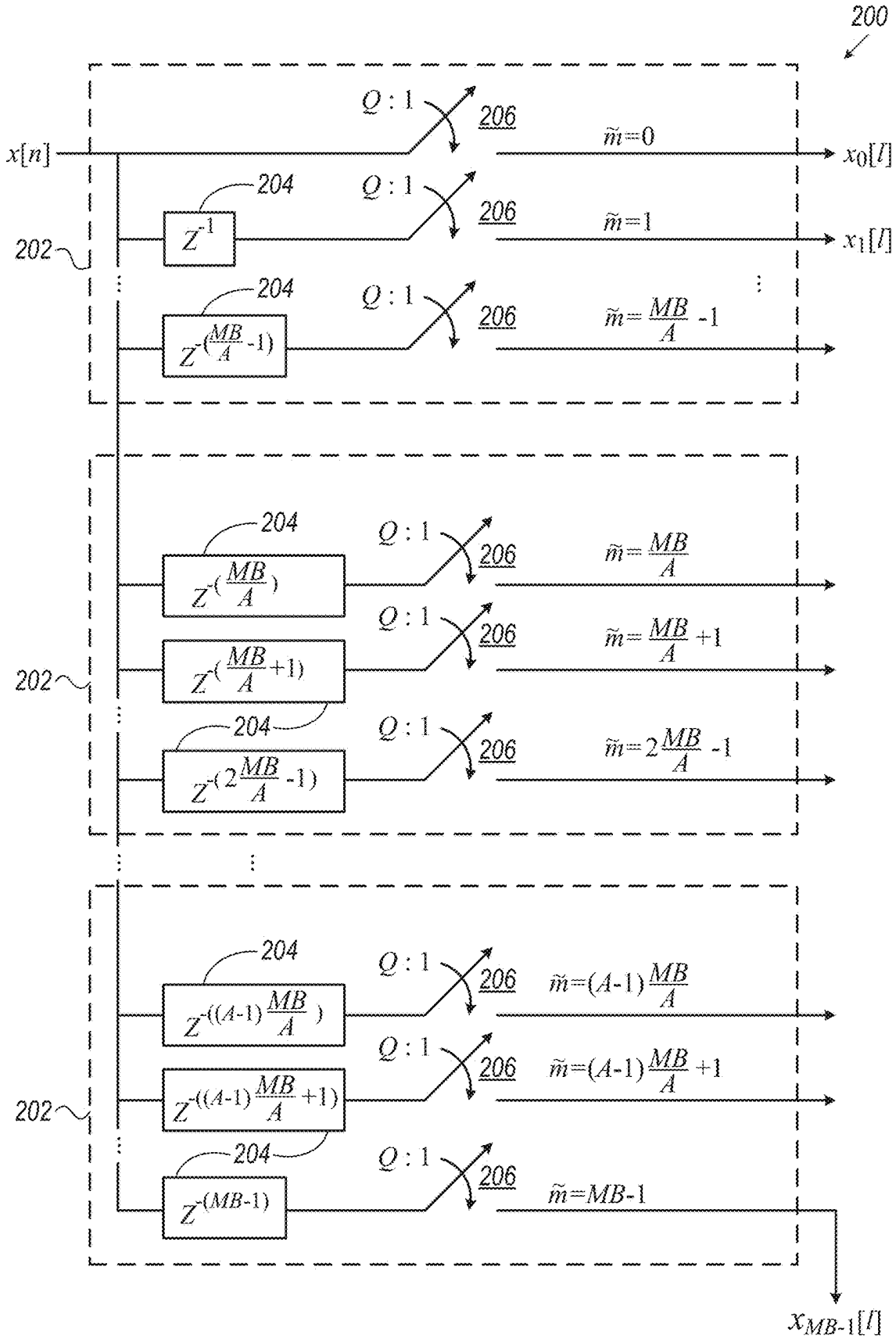

200
x[n]
202
202
202
204
206
Q : 1
$\tilde{m}=0$
$\tilde{m}=1$
$\tilde{m}=\frac{MB}{A}-1$
$\tilde{m}=\frac{MB}{A}$
$\tilde{m}=\frac{MB}{A}+1$
$\tilde{m}=2\frac{MB}{A}-1$
$\tilde{m}=(A-1)\frac{MB}{A}$
$\tilde{m}=(A-1)\frac{MB}{A}+1$
$\tilde{m}=MB-1$
Z^{-1}
$Z^{-(\frac{MB}{A}-1)}$
$Z^{-(\frac{MB}{A})}$
$Z^{-(\frac{MB}{A}+1)}$
$Z^{-(2\frac{MB}{A}-1)}$
$Z^{-((A-1)\frac{MB}{A})}$
$Z^{-((A-1)\frac{MB}{A}+1)}$
$Z^{-(MB-1)}$
$x_0[l]$
$x_1[l]$
$x_{MB-1}[l]$

FIG. 2

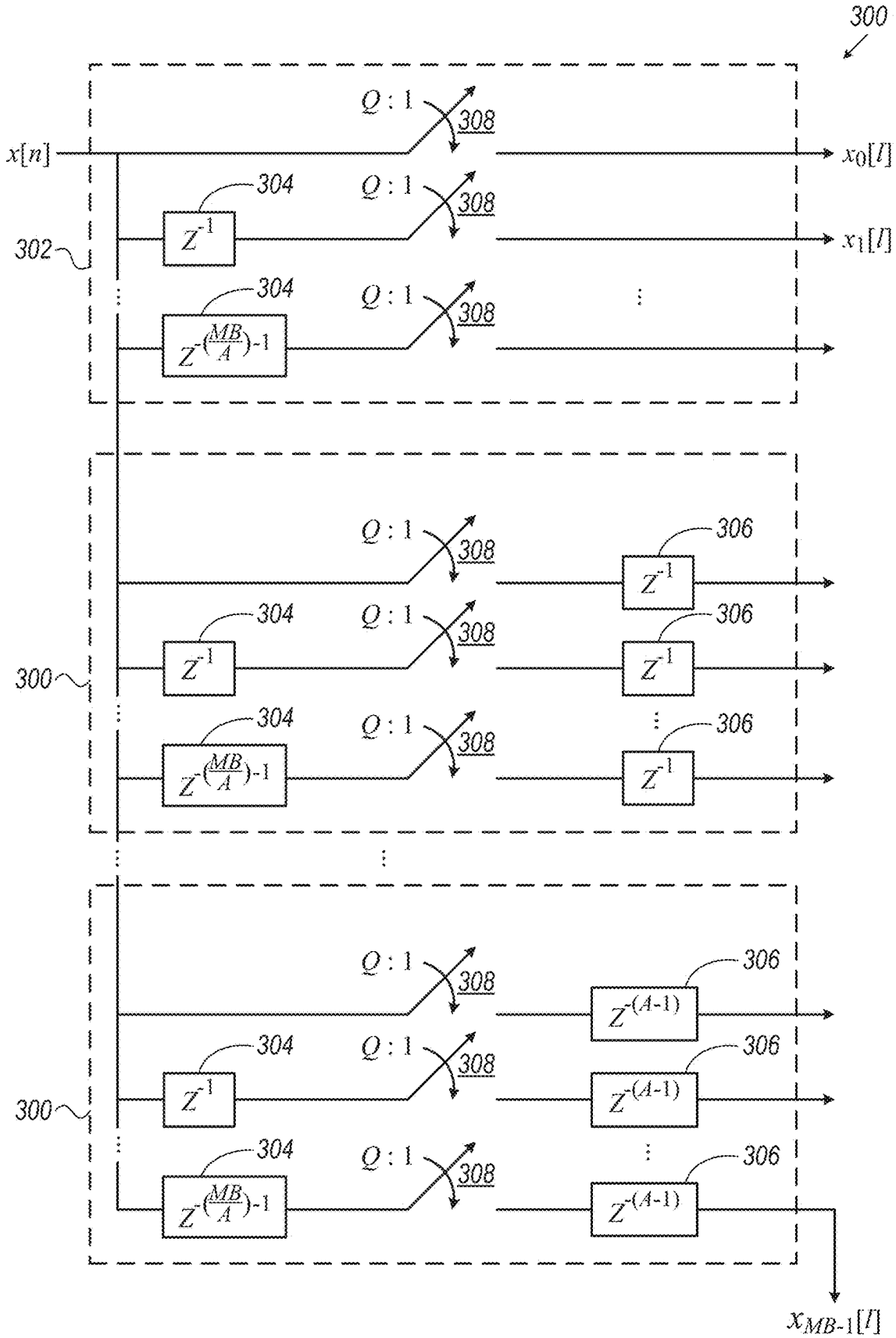


FIG. 3

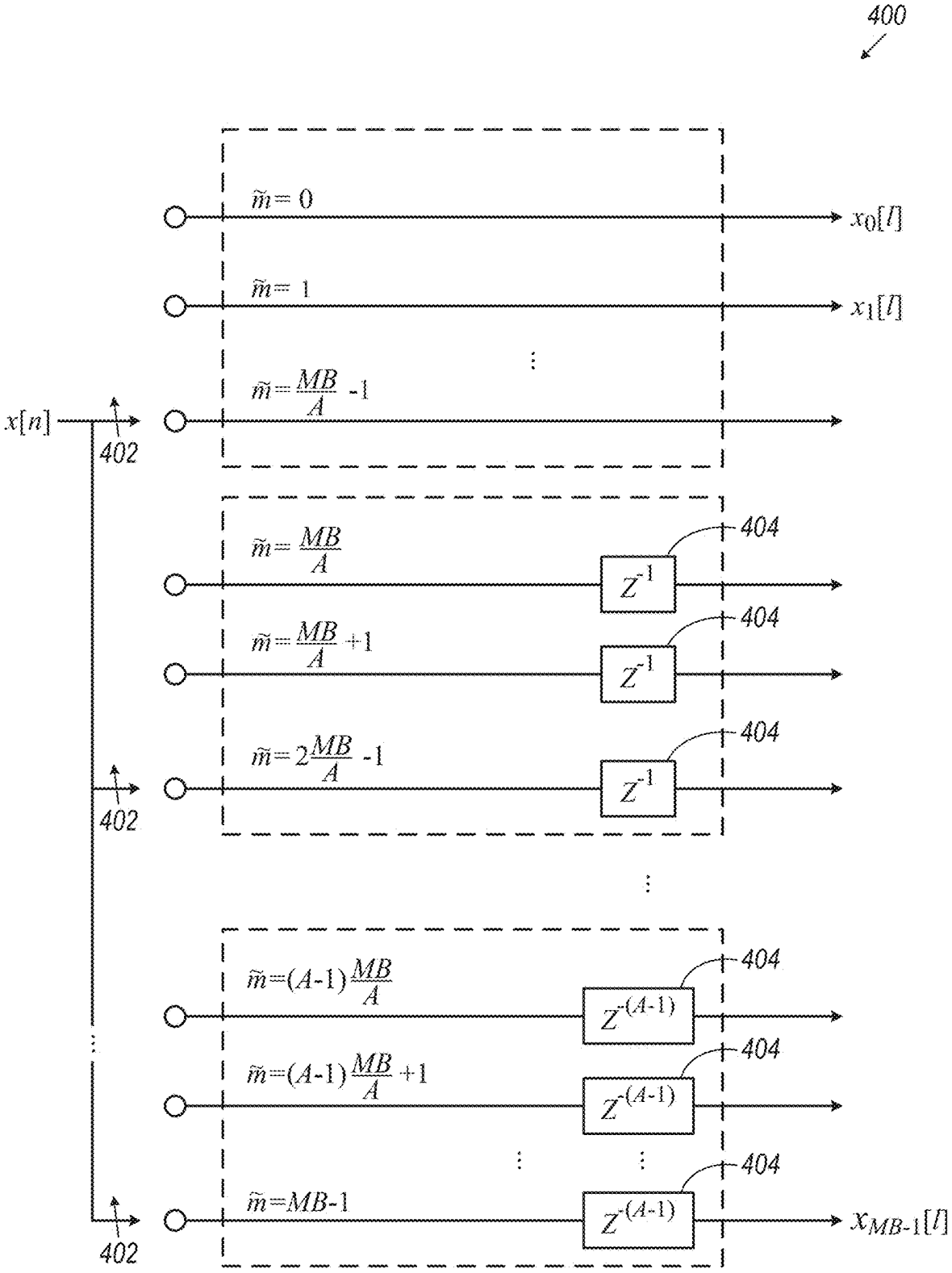

400
$\tilde{m}=0$
$x_0[l]$
$\tilde{m}=1$
$x_1[l]$
$\tilde{m}=\frac{MB}{A}-1$
$x[n]$
402
$\tilde{m}=\frac{MB}{A}$
Z^{-1}
404
$\tilde{m}=\frac{MB}{A}+1$
Z^{-1}
404
$\tilde{m}=2\frac{MB}{A}-1$
Z^{-1}
404
402
$\tilde{m}=(A-1)\frac{MB}{A}$
$Z^{-(A-1)}$
404
$\tilde{m}=(A-1)\frac{MB}{A}+1$
$Z^{-(A-1)}$
404
$\tilde{m}=MB-1$
$Z^{-(A-1)}$
404
$x_{MB-1}[l]$
402

FIG. 4

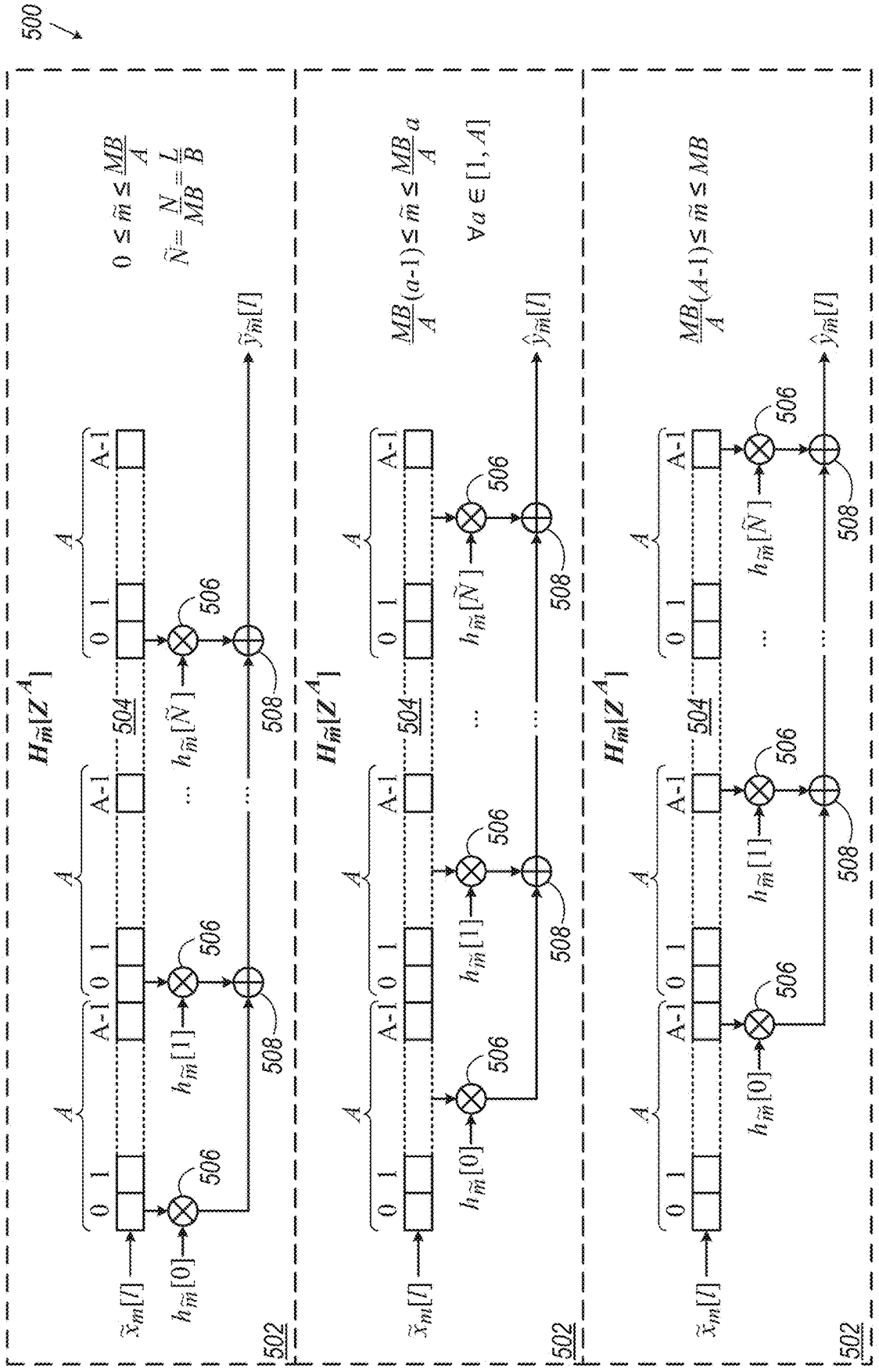

500
502
504
506
508
A
A-1
0 1
$H_{\tilde{m}}[Z^A]$
$\tilde{x}_m[l]$
$h_{\tilde{m}}[0]$
$h_{\tilde{m}}[1]$
$h_{\tilde{m}}[\tilde{N}]$
$\hat{y}_m[l]$
$0 \le \tilde{m} \le \frac{MB}{A}$
$\tilde{N} = \frac{N}{MB} = \frac{L}{B}$
$\frac{MB}{A}(a-1) \le \tilde{m} \le \frac{MB}{A}a$
$\forall a \in [1, A]$
$\frac{MB}{A}(A-1) \le \tilde{m} \le MB$

FIG. 5

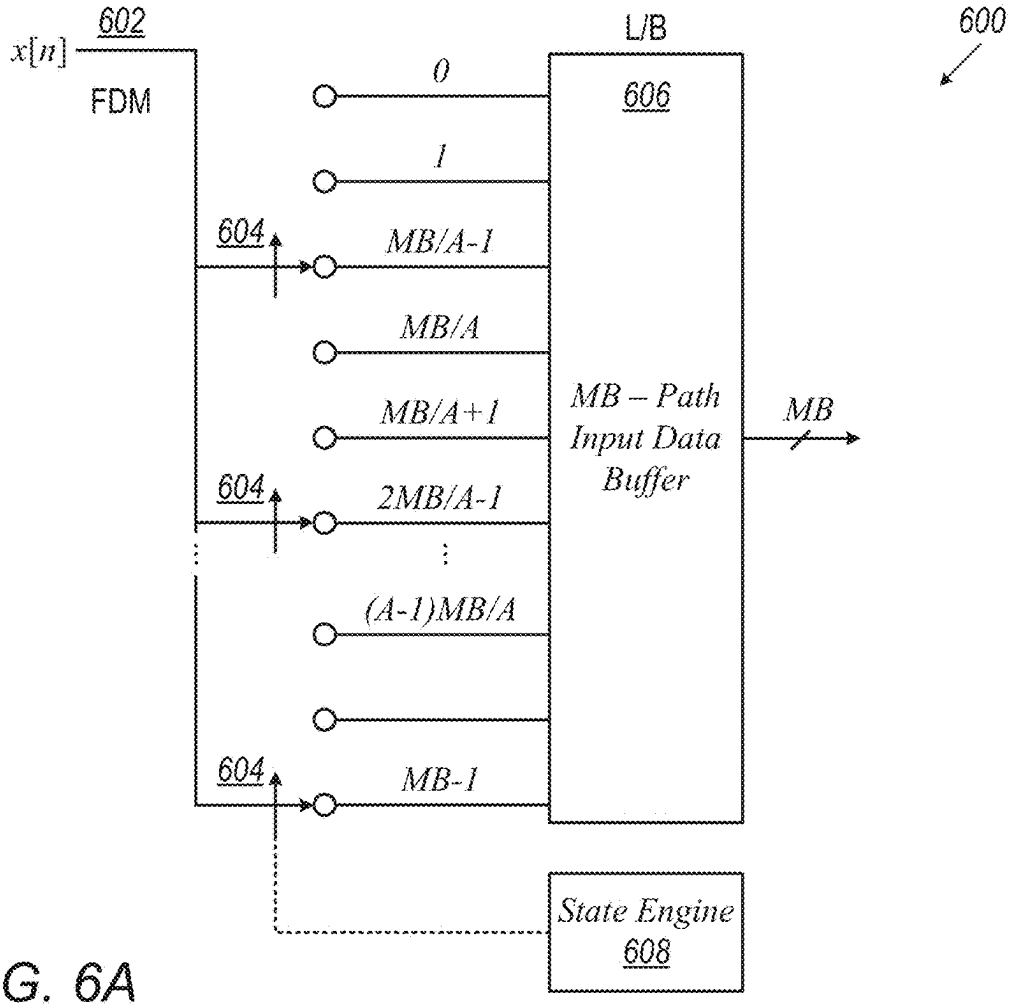

602
x[n]
FDM
L/B
606
600
0
1
604
MB/A-1
MB/A
MB/A+1
MB – Path Input Data Buffer
MB
604
2MB/A-1
(A-1)MB/A
604
MB-1
State Engine 608

FIG. 6A

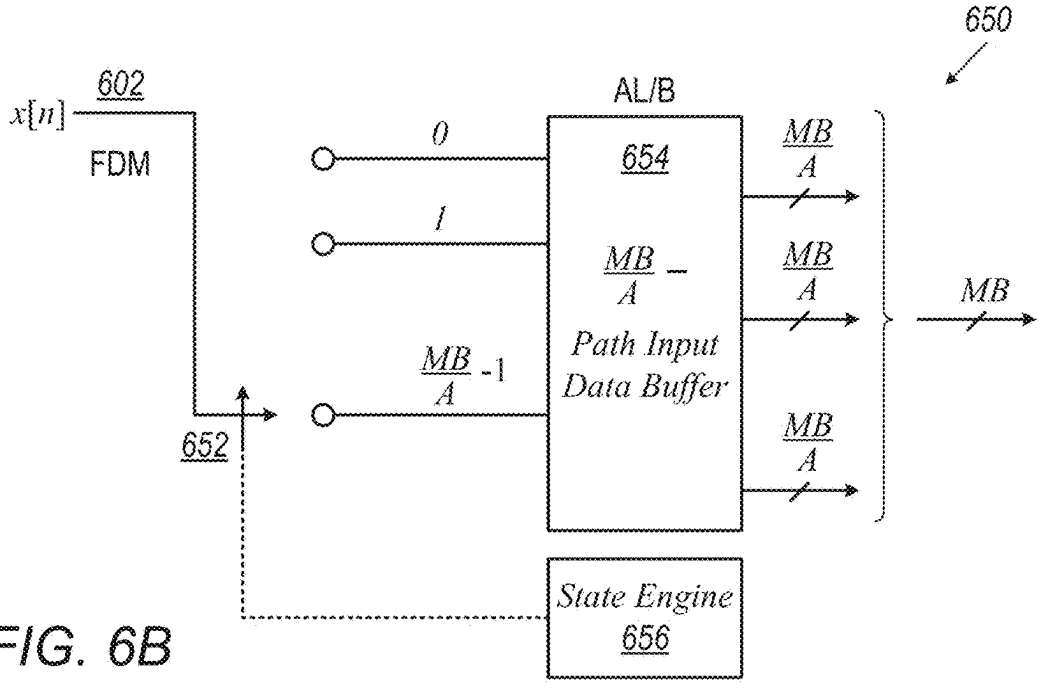

650
602
x[n]
FDM
AL/B
654
0
1
MB/A -1
652
MB/A
MB/A
MB/A
MB
MB/A – Path Input Data Buffer
State Engine 656

FIG. 6B

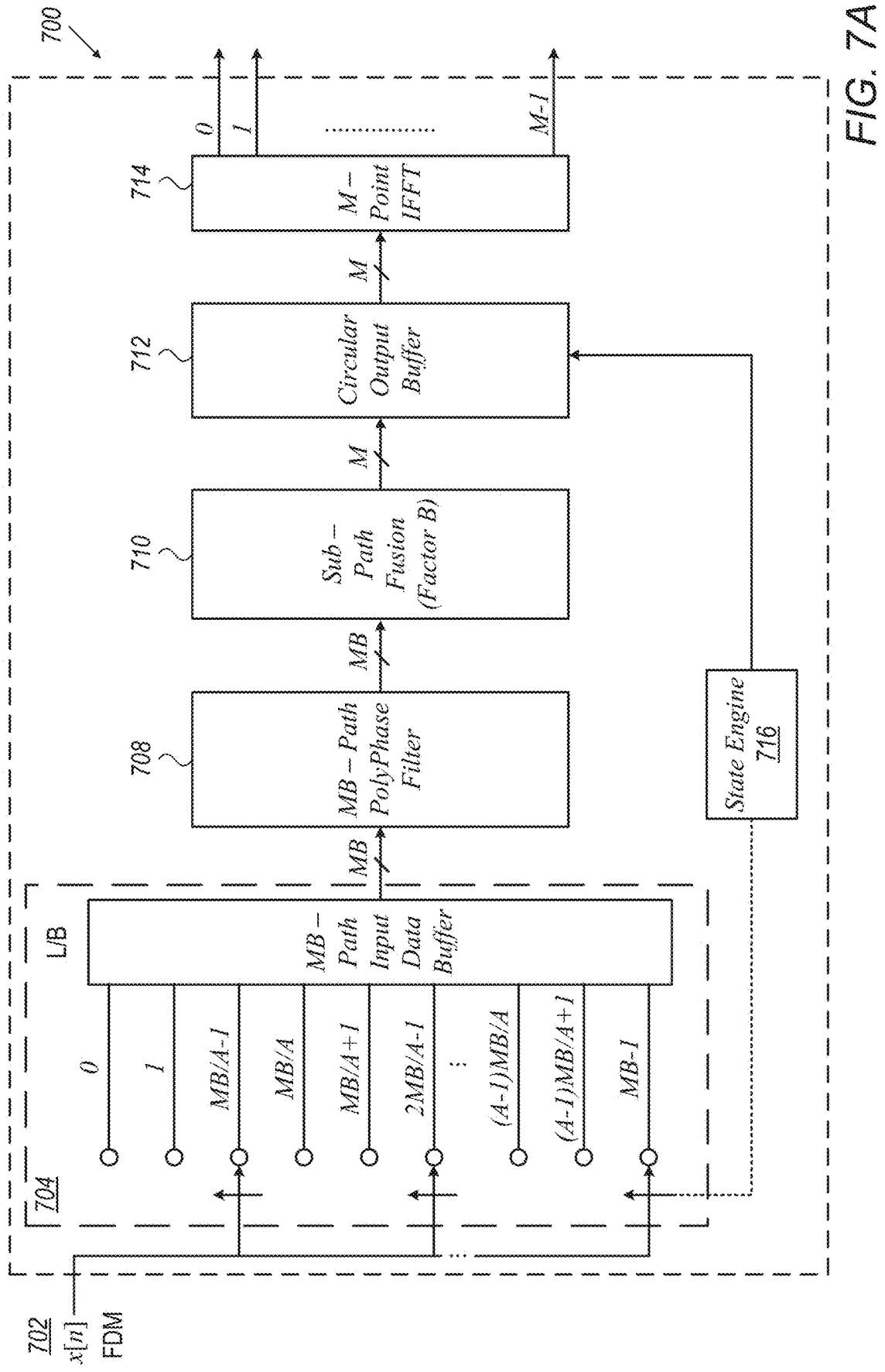

700
702
x[n]
FDM
704
L/B
MB – Path Input Data Buffer
0
1
MB/A-1
MB/A
MB/A+1
2MB/A-1
(A-1)MB/A
(A-1)MB/A+1
MB-1
MB
708
MB – Path PolyPhase Filter
MB
710
Sub – Path Fusion (Factor B)
M
712
Circular Output Buffer
M
714
M – Point IFFT
0
1
M-1
State Engine 716

FIG. 7A

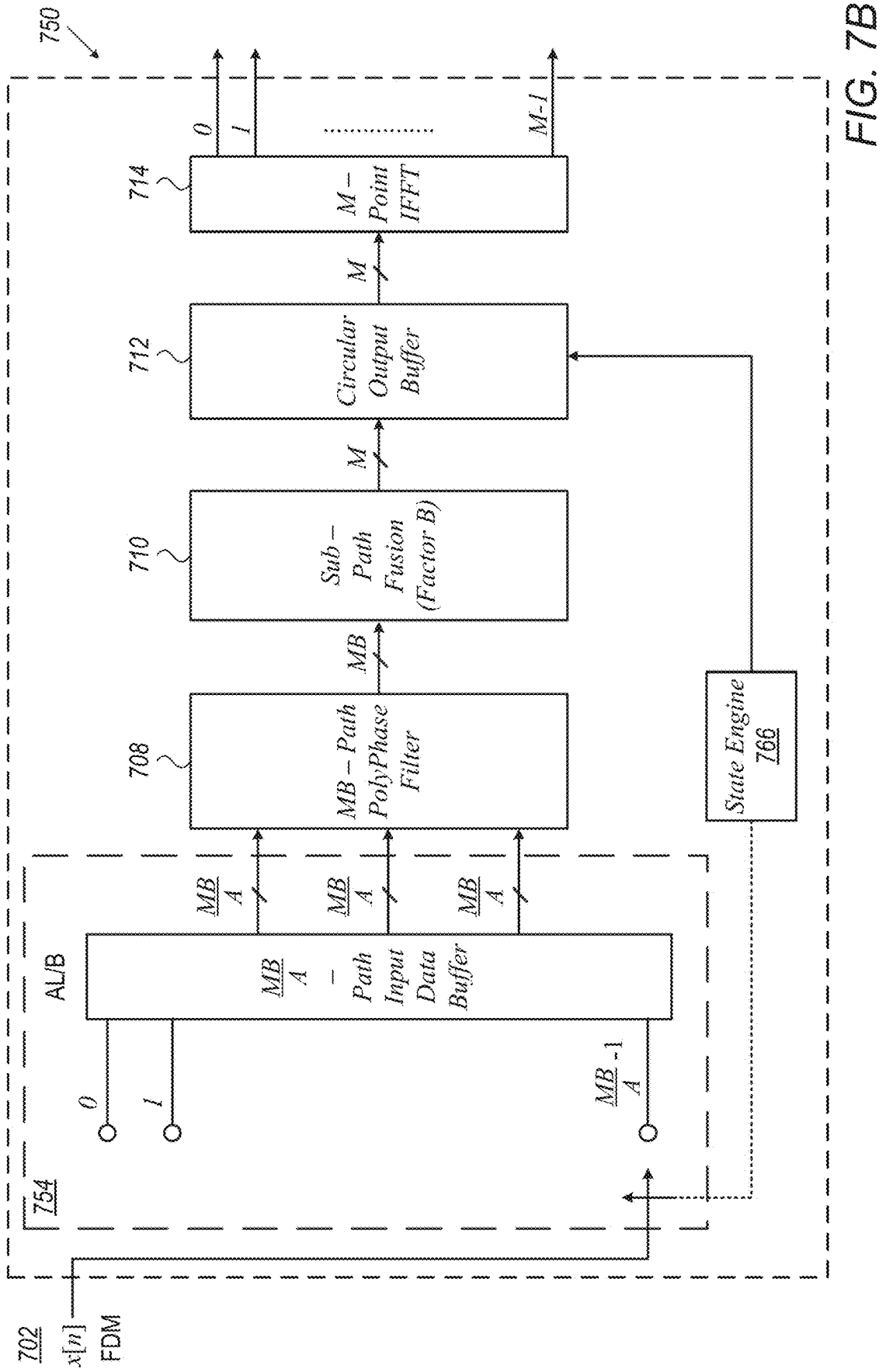

750
714
M – Point IFFT
0
1
M-1
712
Circular Output Buffer
M
710
Sub – Path Fusion (Factor B)
M
708
MB – Path PolyPhase Filter
MB
MB/A
MB/A
MB/A
MB/A – Path Input Data Buffer
AL/B
754
0
1
MB/A -1
State Engine 766
702
x[n] FDM

FIG. 7B

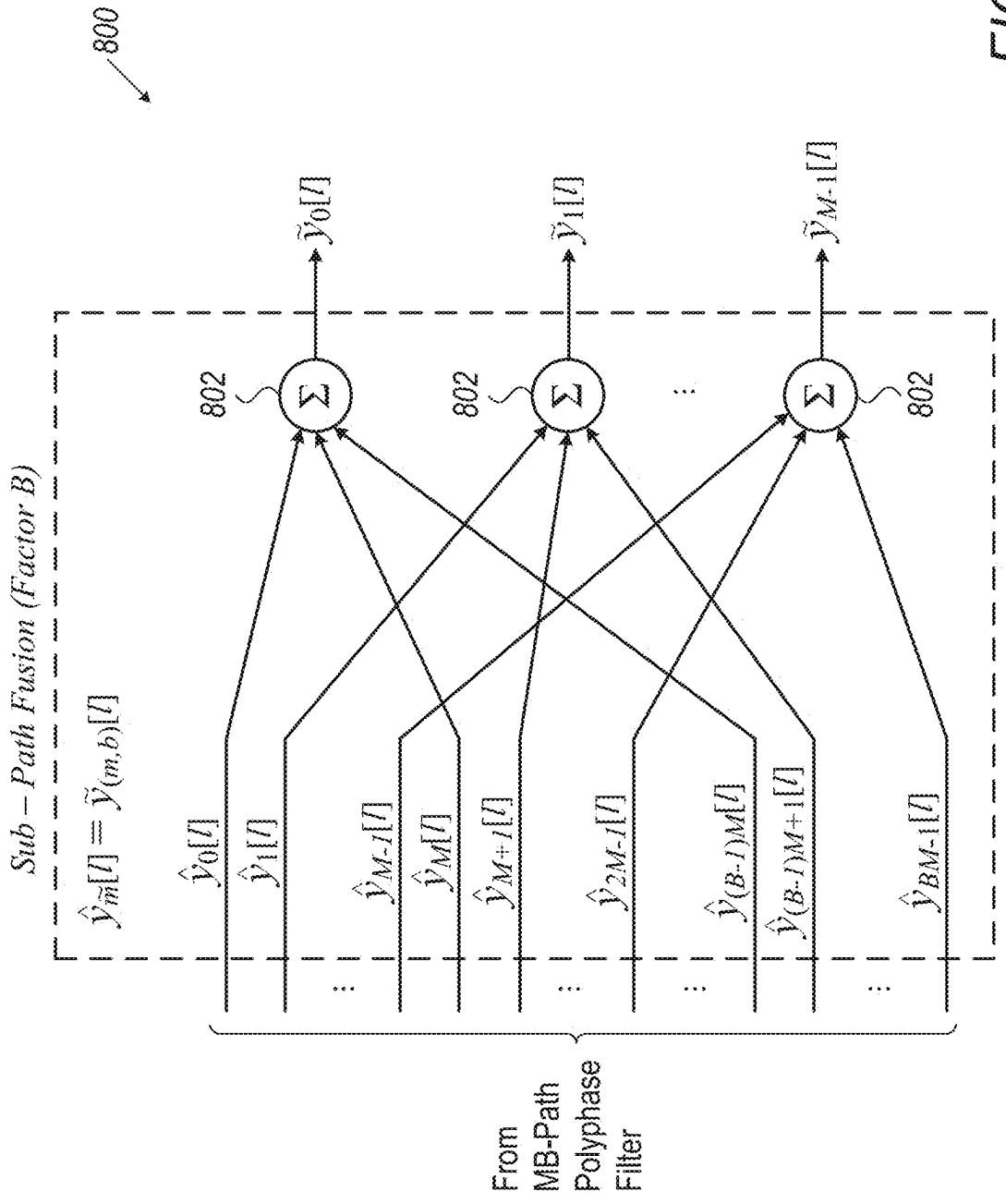

800
Sub – Path Fusion (Factor B)
$\hat{y}_{\tilde{m}}[l] = \tilde{y}_{(m,b)}[l]$
802
802
802
$\tilde{y}_0[l]$
$\tilde{y}_1[l]$
$\tilde{y}_{M-1}[l]$
$\hat{y}_0[l]$
$\hat{y}_1[l]$
$\hat{y}_{M-1}[l]$
$\hat{y}_M[l]$
$\hat{y}_{M+1}[l]$
$\hat{y}_{2M-1}[l]$
$\hat{y}_{(B-1)M}[l]$
$\hat{y}_{(B-1)M+1}[l]$
$\hat{y}_{BM-1}[l]$
From MB-Path Polyphase Filter

FIG. 8

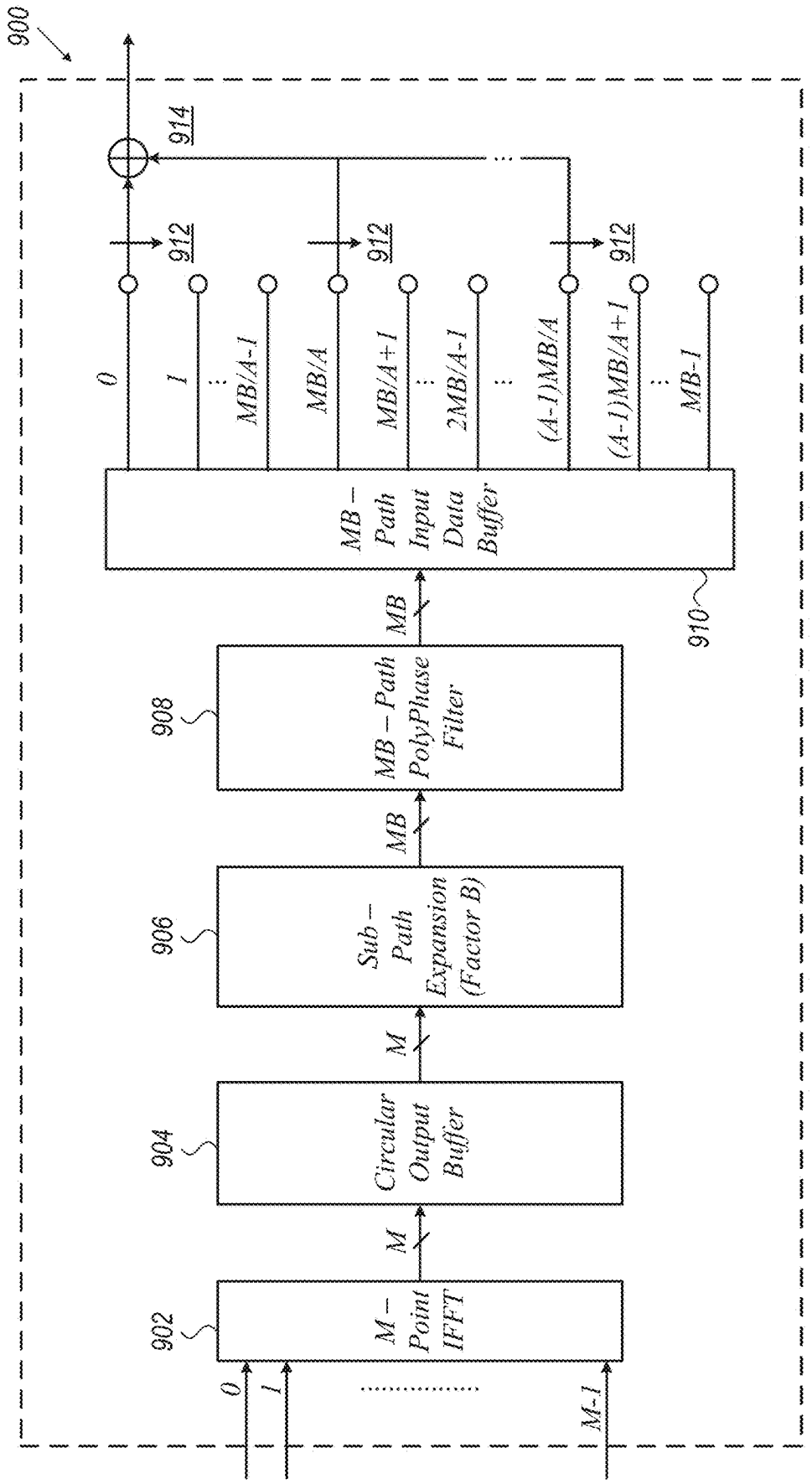

900
902
M – Point IFFT
0
1
M-1
M
904
Circular Output Buffer
M
906
Sub – Path Expansion (Factor B)
MB
908
MB – Path PolyPhase Filter
MB
910
MB – Path Input Data Buffer
0
1
MB/A-1
MB/A
MB/A+1
2MB/A-1
(A-1)MB/A
(A-1)MB/A+1
MB-1
912
912
912
914

FIG. 9

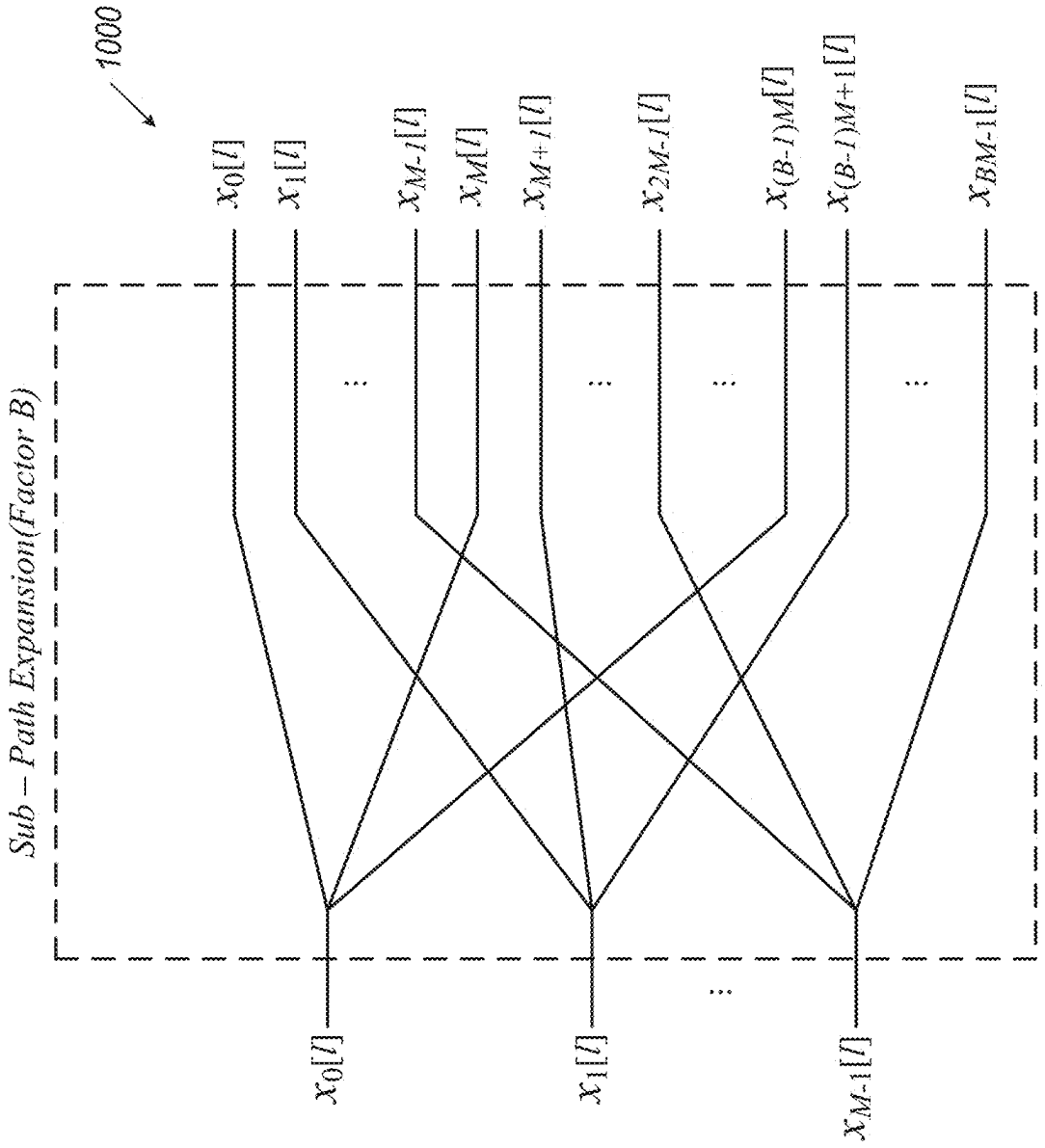

1000
Sub – Path Expansion(Factor B)
$x_0[l]$
$x_1[l]$
$x_{M-1}[l]$
$x_M[l]$
$x_{M+1}[l]$
$x_{2M-1}[l]$
$x_{(B-1)M}[l]$
$x_{(B-1)M+1}[l]$
$x_{BM-1}[l]$
$x_0[l]$
$x_1[l]$
$x_{M-1}[l]$

FIG. 10

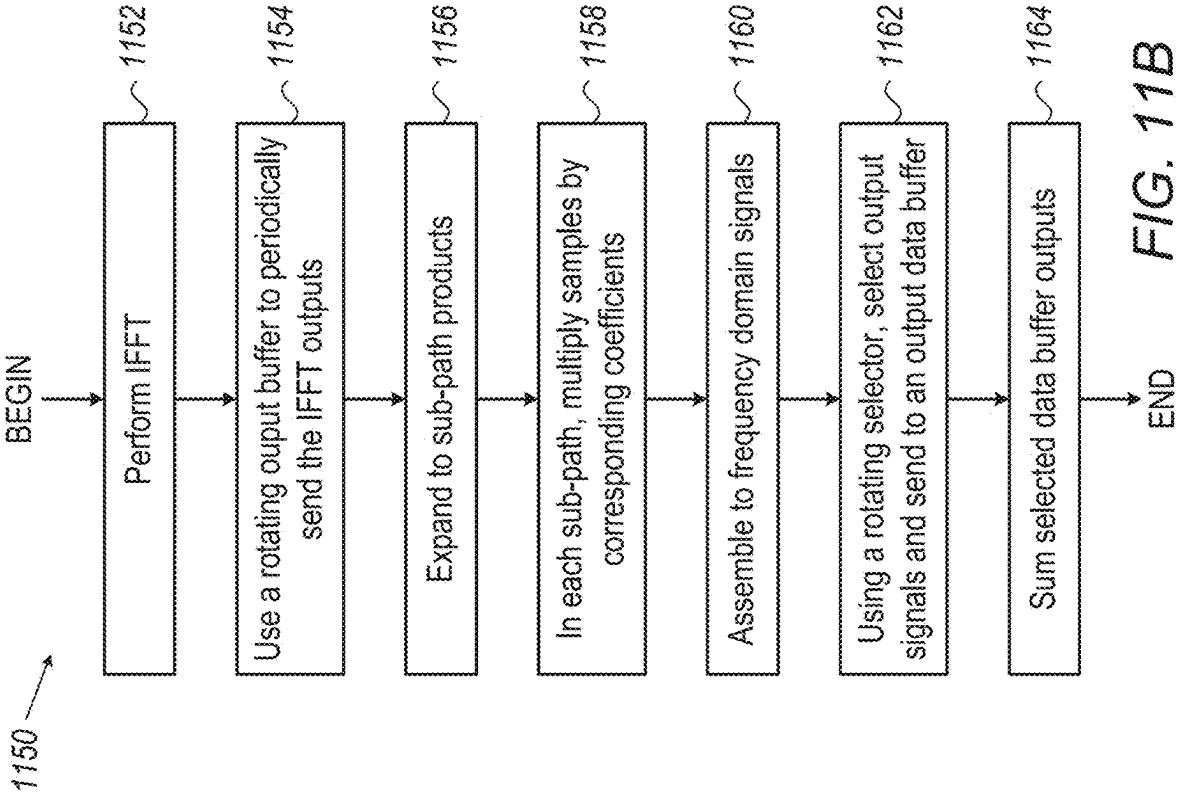


FIG. 11B

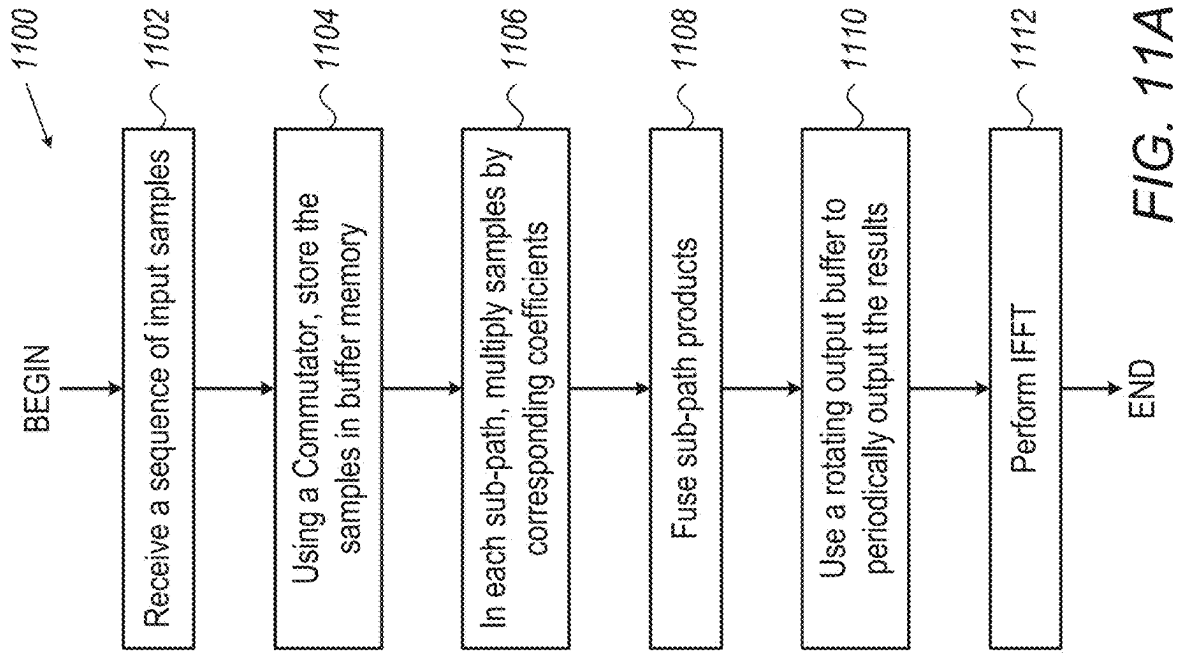


FIG. 11A

POLYPHASE FILTER BANKS WITH RATIONAL DECIMATION / INTERPOLATION FACTOR

FIELD OF THE INVENTION

[0001] The present invention relates generally to signal processing, and particularly to digital filters.

CROSS REFERENCE TO RELATED APPLICATIONS

[0002] This application claims the benefit of U.S. Provisional Patent Application, 63/553,180, filed Feb. 14, 2024, whose disclosure is incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0003] In modern communication systems, efficient frequency division and signal separation are essential for processing multiple channels simultaneously. One of the most critical tasks in such systems is the ability to divide a wideband signal into its constituent narrowband channels, a process known as channelization. This is crucial in applications such as software-defined radios (SDRs), cognitive radio, satellite communications, and other wireless systems, where multiple signals must be analyzed or transmitted simultaneously over the same frequency spectrum.

[0004] A key technique for performing channelization efficiently is the use of polyphase filters, which allow efficient implementation of the channelization process with reduced computational and complexity lower power consumption.

[0005] Background on polyphase filters can be found, for example, in "Multirate Signal Processing for Communication Systems", by F. J. Harris (Upper Saddle River, NJ, USA: Prentice-Hall, 2004). Chapter 6 therein (pp. 139-165) presents resampling low-pass and band-pass Finite Impulse Response (FIR) filters for which the noble identity has been applied to interchange the operations of resampling and filtering, and examines up-sampling, down-sampling, and cascade up-down sampling filters.

[0006] Additional background can be found in U.S. Pat. No. 10,050,607, which discloses a polyphase decimation FIR filter apparatus including a modulo integrator circuit configured to integrate input samples and to provide integrated input samples; and a polyphase FIR filter circuit configured to process the integrated input samples, the polyphase FIR filter circuit including a plurality of multiplier accumulator circuits, each configured to accumulate products of coefficients and respective integrated signal samples, to form outputs corresponding to different channels.

SUMMARY OF THE INVENTION

[0007] An embodiment of the present invention that is described herein provides an Analysis Polyphase Filter (APPF) for shifting a selected passband of an input signal to a passband signal, having a Q=M·B/A decimation factor, B and A being co-primes, the APPF comprising M·B Paths. Each path includes (i) M·B/A multiplication Sub-paths, and (ii) a Sub-path Fusion Circuit, which is configured to generate fused multiplication products responsively to a sum of the multiplication products generated by each of the multiplication sub-paths.

[0008] In some embodiments, the APPF further includes an input circuit, configured to receive and temporarily store input samples of the input signal at a subsampling ratio of Q:1. In an example embodiment, the input circuit includes a commutator, configured to sample the input signal according to an input commutation indication.

[0009] In some embodiments, the APPF further includes a circular output buffer, configured to output the fused multiplication products in a circular manner according to an output selection indication. In some embodiments, the APPF further includes an M-point Inverse-Fast-Fourier-Transform (IFFT) circuit, configured to convert the fused multiplication products into a polyphase-filtered output signal. In some embodiments, the APPF further includes a state engine, configured to generate an input commutation indication and an output selection indication.

[0010] There is additionally provided, in accordance with an embodiment that is described herein, a Synthesis Polyphase Filter (SPPF) for shifting a baseband signal to a passband of an output signal, having a Q=M·B/A interpolation factor, B and A being co-primes. The SPPF includes (i) M·B Paths, each path including M·B/A multiplication Sub-paths, and (ii) a Sub-path Expansion Circuit, which is configured to split multiplication products from the multiplication sub-paths.

[0011] In some embodiments, the SPPF further includes an M-point Inverse-Fast-Fourier-Transform (IFFT) circuit, configured to perform an Inverse-Fourier-Transform of the baseband signal, thereby producing an IFFT-transformed baseband signal. In an embodiment, the SPPF further includes a Circular Output Buffer, configured to receive, buffer and periodically output the IFFT-transformed baseband signal according to an output selection indication. In some embodiments, the SPPF further includes a state engine, to generate an output selection indication.

[0012] There is also provided, in accordance with an embodiment that is described herein, a Channelizer for shifting a passband in an input signal to a baseband signal. The channelizer includes an Analysis polyphase Filter (APPF), having a Q=M·B/A decimation/interpolation factor, B and A being co-primes. The APPF includes M·B Paths, each path including (i) M·B/A multiplication Sub-paths and (ii) a Sub-path Fusion Circuit, which is configured to generate fused multiplication products responsively to a sum of the multiplication products generated by each of the multiplication sub-paths.

[0013] There is further provided, in accordance with an embodiment that is described herein, an Up-Converter for shifting a baseband signal to a passband within an output signal. The Up-Converter includes a Synthesis Polyphase Filter (SPPF), having a Q=M·B/A decimation/interpolation factor, B and A being co-primes. The SPPF includes M·B Paths, each path including (i) M·B/A multiplication Sub-paths and (ii) a Sub-path Expansion Circuit, which is configured to split multiplication products from the multiplication sub-paths.

[0014] The present invention will be more fully understood from the following detailed description of the embodiments thereof, taken together with the drawings in which:

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] FIG. **1** is a block diagram that schematically illustrates a Polyphase (PP) FIR filter with rational decimation factor, in accordance with an embodiment that is disclosed herein.

[0016] FIG. **1**A is a block diagram that schematically illustrates an index-m PP Path of the PP FIR Filter of FIG. **1**, in accordance with an embodiment that is disclosed herein;

[0017] FIG. **2** is a block diagram that schematically illustrates an Input Stage of a Polyphase FIR Filter, in accordance with an embodiment that is disclosed herein;

[0018] FIG. **3** is a block diagram that schematically illustrates a Rearranged Input Stage of a Polyphase FIR Filter, in accordance with an embodiment that is disclosed herein;

[0019] FIG. **4** is a block diagram that schematically illustrates an MB/A-path Gatling-Gun Input buffer, in accordance with an embodiment that is disclosed herein;

[0020] FIG. **5** is a block diagram that schematically illustrates a Group of MB/A FIR Filter Paths, in accordance with an embodiment that is disclosed herein;

[0021] FIG. **6**A is a block diagram that schematically illustrates an MB-Path Input Data Buffer, in accordance with an embodiment that is disclosed herein;

[0022] FIG. **6**B is a block diagram that schematically illustrates an MB/A-Path Input Data Buffer, in accordance with an embodiment that is disclosed herein;

[0023] FIG. **7**A is a block diagram that schematically illustrates a complete MB-Path Analysis Polyphase Filter (APPF), in accordance with an embodiment that is disclosed herein;

[0024] FIG. **7**B is a block diagram that schematically illustrates a complete MB/A-Path Analysis Polyphase Filter (APPF), in accordance with an embodiment that is disclosed herein;

[0025] FIG. **8** is a block diagram that schematically illustrates a Sub-Path Fusion Circuit, in accordance with an embodiment that is disclosed herein;

[0026] FIG. **9** is a block diagram that schematically illustrates a Synthesis Polyphase Filter, in accordance with an embodiment that is disclosed herein;

[0027] FIG. **10** is a block diagram that schematically illustrates a Sub-Path Expansion Circuit, in accordance with an embodiment that is disclosed herein;

[0028] FIG. **11**A is a flowchart that schematically illustrates a method for rational decimation-rate polyphase FIR analysis, in accordance with an embodiment that is disclosed herein; and

[0029] FIG. **11**B is a flowchart **1150** that schematically illustrates a method for rational decimation-rate polyphase FIR synthesis, in accordance with an embodiment that is disclosed herein.

DETAILED DESCRIPTION OF EMBODIMENTS

Overview

[0030] Polyphase filtering is a technique used to efficiently implement filter operations and sampling frequency changes. The M-path polyphase analysis filter bank (AFB) channelizer in its simplest realization—the maximally decimated filter bank—Given a wideband signal with sampling frequency f_s, outputs M baseband time series from translated spectral bands centered at integer multiples of f_s/M and with an equal bandwidth of f_s/M. Similarly, the synthesis filter bank (SFB) up-converter, in its simplest realization—the maximally interpolated filter bank—given M baseband time series with a bandwidth f_s/M, outputs a single wideband signal with sampling frequency, f_s, and comprising the baseband signals now positioned at integer multiples of f_s/M.

[0031] A polyphase-based implementation reduces the workload by a factor of M, rendering this algorithm attractive for applications with limited computational resources. Standard modifications to the channelizers include non-maximal decimation/interpolation with oversampling factor A/M, where A is a positive, non-zero integer. Specifically, a typical choice is A=2, which yields M/2-to-1 downsampling instead of M-to-1 at the AFB, or 1-to-M/2 up-sampling instead of 1-to-M at the SFB. When such a design is paired with a raised cosine prototype filter, neighboring channels construct coherently, which is referred to as Perfect Reconstruction filter banks. This enables a design suitable for channels with variable center frequencies and variable bandwidths. However, the non-maximal decimation/interpolation requires, when A=2, doubling the number of samples due to the doubled sampling rate, which can be a limiting factor (more than doubling samples may be required when A>2).

[0032] Embodiments that are disclosed hereinbelow adapt the M-path polyphase-based analysis and synthesis filter banks to rational oversampling factors of the form Af_s/BM, where both A and B are natural numbers. In embodiments, perfect reconstruction for almost perfect reconstruction, according to the selected resolution and the accuracy of the raised-cosine filter) is achieved, with a relatively small amount of computing resources and power consumption.

[0033] In an embodiment, an AFB comprises an input buffer, to store input samples at locations according to an input commutation indication that is generated by State-Engine, followed by a multiplier bank. The Multiplier bank comprises Paths, each Path comprising Sub-Paths, wherein each Sub-Path multiplies an input sample by a corresponding coefficient. A Fusion circuit then sums products pertaining to the same Sub-Path; a Circular Output Buffer, timed by an output selection indication (generated by the State-Engine), periodically sends sums to an IFFT circuit, that outputs the band-pass signals.

[0034] In another embodiment, an SFB comprises an input IFFT circuit, followed by a circular buffer that stores IFFT samples. A Sub-Path Expansion circuit next splits the sample according to sub-paths, and an MB-Path filter multiplies the samples by corresponding coefficients. An MB-Path Output Buffer selectively sends the products to an A-part Gatling gun distributor, followed by adders, which outputs the pass-band signal.

[0035] Further embodiments disclose a Channelizer and a Channel-Up-Converter, that comprise, respectively, rational decimation and interpolation polyphase filters.

System Description

[0036] A standard analysis filter pipeline comprises a Finite Impulse Response (FIR) Low-Pass Filter (LPF) followed by downsampling by a factor of Q.

[0037] Initially, an input signal x[n] that is sampled at a rate of f_s, wherein n is a corresponding discrete time index, is fed to an FIR filter h[n] that comprises N filter taps. The output is:

$$y[n] = \sum_{t=0}^{N-1} h[t]x[n-1] \quad (1)$$

[0038] y[n] is then downsampled (decimated) at a factor of Q, to give

$$\tilde{y}[l] = y[lQ] \quad (2)$$

[0039] where l is the discrete time index at reduced sample rate f_s/Q. Q is typically selected based on the characteristics of filter h[n]. From this point henceforth, we consider, without loss of generality, an LPF with a passband of $2\pi/M$, for which $Q \leq M$ facilitates aliasing-free low-rate signals and Q=M gives the maximally decimated pipeline. The LPF Decimation pipeline is extended to a band-pass filter (BPF) by initially multiplying the input signal with a modulation series, in order to shift the input signal to baseband, prior to filtering. To avoid complex notation in the case of a BPF, the same notation of x[n] is updated also after multiplication by the modulator prior to the filter: i.e., x[n] is replaced by

$$e^{-\frac{j2\pi k}{M}},$$

where k=0, 1, . . . , M−**1** is the channels index, spanning a total of M channels.

[0040] The pipeline above may be implemented using an M-path polyphase filter. For the case of integer multiples of the maximally decimated pipeline, i.e., for Q=M/A, where A is an integer and for channels at $2\pi k/M$ for k=0, 1 . . . , M−1, the implementation follows a two-dimensional partition of the sum in Equation (1), and the application of the Noble Identity (NI) for each path. The two-dimensional partition maps the N filter taps in h[n] into M paths, each with L=N/M taps. It is assumed that M divides N without a remainder (when this is not the case, zero-padding can be applied). y[n] in this case is derived as:

$$y[n] = \sum_{m=0}^{M-1} y_m[n] \quad (3)$$

Where

$$y_m[n] = \sum_{t=0}^{N-1} h_m[t]x_m[n-t] \quad (4)$$

[0041] and hm[n] is defined, via its Z transform as

$$H_m(Z) = \hat{H}(Z^M) \quad (5)$$

[0042] where $\hat{H}(Z)$ is the Z transform of the maximally decimated polyphase partition given by

$$\hat{h_m}[n] = h[nM+m] \quad (6)$$

[0043] and with z^M in equation (5) signifying that the filter coefficients $\hat{h}_m[n]$ are separated by M samples (or, equivalently, there are M−1 zeros between every two coefficients).

[0044] The signals in each path are defined as

$$x_m[n] = x[n-m]. \quad (7)$$

The output of the filters in each path, $\{y_m[n]\}$ (m=0. . . M−1), are then downsampled, given as

$$\tilde{y}_m[l] = y_m[lQ]. \quad (8)$$

[0045] The NI is applied to each of the paths separately and identically, exploiting the fact that the filter coefficients of $h_m[n]$ are separated by M samples (see equation (5)).

[0046] Initially, the $x_m[n]$ on each path are downsampled by a factor of Q, to give:

$$\tilde{x}_m[l] = x_m[lQ] \quad (9)$$

with the updated filters now applied after the down-sampler, defined using the inverse Z transform of $\tilde{H}(Z)$ as

$$\tilde{H}_m(Z) = \hat{H}_m(Z^{M/Q}) \quad (10)$$

[0047] which is well-defined when Q=M/A is an integer. The output $\tilde{y}_m[1]$ of each filter path is then given as

$$\tilde{y}_m[l] = \sum_{t=0}^{L-1} \tilde{h}_m[t]\,\tilde{x}_m[l-t] \quad (11)$$

[0048] which is equivalent to $\tilde{y}_m[l]$ from equation (8). This equivalence shows a reduced computation of L filter coefficients instead of a multiplication of N filter coefficients as in equation (4) followed by downsampling in equation (8).

$$\{\tilde{y}_m[l]\}_{m=0}^{M-1}$$

are now summed in a similar manner to equation (3), but now over the output signals at $\tilde{f}_s$, i.e.,

$$\tilde{y}[l] = \sum_{m=0}^{M-1} \tilde{y}_m[l] \quad (12)$$

[0049] Finally, the pipeline is extended to the case of bandpass by modulating the filters to passband and then modulating the filter output back to baseband.

[0050] An M-path polyphase filter design, with channels at $2\pi k/M$, with k=0, . . . , M−1, comprises M paths, each path comprising a delay z^{-k} followed by a $\hat{H}_m(Z)$ filter and two exponential functions. The first exponential function is a time series

$$\left\{\exp\left\{\left(-jQ\frac{2\pi kl}{M}\right\}\right\}\right\}_{k=0}^{M-1}=\left\{\exp\left\{\left(-j\frac{2\pi kl}{A}\right\}\right\}\right\}_{k=0}^{M-1} \tag{13}$$

[0051] That is identical for all paths modulating the filter output to baseband (Note that for A=1, this exponent equal unity for all 1, and is, thus, omitted).

[0052] The second exponential function is a constant in each path, given by exp (−j*(2πkm/M)) and charged with modulating the filters to passband.

[0053] Note that modulating the filters typically requires multiplying the filter t with a modulation series. However, as the modulation series are periodic over M for all k=0, . . . , M−1, the modulation series in each path is a constant; furthermore, as it is constant, it is typically positioned at the end of the pipeline and implemented using an inverse fast Fourier transform (IFFT) for all k=0, . . . , M−1 simultaneously, to reduce computation.

[0054] For more details regarding an M-path polyphase implementation including a frequency domain interpretation of the signals in each path, the reader is referred to Chapter 6 of "Multirate Signal Processing for Communication Systems", by F. J. Harris et al, cited above.

[0055] The polyphase presented above facilitates the design of perfect-reconstruction (PR) (or nearly PR) filter banks when setting A≥2, which facilitates application-specific requirements of variable center frequency and variable bandwidths.

[0056] Specifically, A=2 or, alternatively, Q−M/2 is a common solution for facilitating PR filter banks.

[0057] Using Equation (10), $\hat{H}_m(Z)$ in this case are given as $\hat{H}_m(Z)=H_m^{max}(Z^2)$, which can be interpreted as a separation of the filter coefficients (in each path) by two samples. This requires storing double the number of registers (for each path) compared to the case of A=1.

[0058] Furthermore, in this case, the first exponential function reduces to exp (−jπkl), which means phase shifts of π for odd values of k.

[0059] These shifts are typically treated by applying circular shifts to time-domain signals to avoid multiplication with complex exponential functions.

Rational Decimation/Interpolation Factors

[0060] Embodiments to be disclosed herein comprise polyphase filters with rational multiples of the maximally decimated pipeline, i.e., for Q=MB/A, where B is also an integer value, and wherein B and A are co-primes. We decompose each of the M paths to B polyphase sub-paths prior to the application of NI, while exploiting the knowledge that the filter taps in each path prior to the NI application are separated by M samples (see Equation 5).

[0061] This is applied to each path separately and identically. Without loss of generality, the solution is now derived for path m.

[0062] The filter in path m is partitioned into B sub-paths prior to the application of the NI:

$$y_m[n]=\sum_{b=0}^{B-1} y_{(m,b)}[n] \tag{14}$$

where

$$y_{(m,b)}[n]=\sum_{t=0}^{N-1} h_{(m,b)}[t]x_{(m,b)}[n-t] \tag{15}$$

[0063] the signals in each of the B sub-paths, $\{x_{(m,b)}[n]\}_{b=0}^{B-1}$, are defined similarly to $x_m[n]$ from Equation (7), but with shift of M (see Equation 5), as

$$x_{(m,b)}[n]=x_m[n-bM], \tag{16}$$

[0064] and $h_{(m,b)}[n]$ are defined as in the case of $h_m[n]$ from Equation (4), via its Z-transform, $H_{(m,b)}(z)$ similarly to Equation (5) as

$$H_{(m,b)}(Z)=\hat{H}_{(m,b)}(Z^B), \tag{17}$$

[0065] with $\hat{H}_{(m,b)}$ being the z transform of the maximally-decimated polyphase path, defined similarly to Equation (6)

$$\hat{H}_{(m,b)}[n]=\overleftarrow{h_m}[nB+b]. \tag{18}$$

[0066] The NI for Q=MB/A can now be applied in order to reduce the computations, as compared to the direct implementation.

[0067] Initially, the downsampled signals and filters are defined for each of the sub-paths $x_{(m,b)}[n]$ on each path are downsampled by a factor of Q, similarly to Equation (9), as

$$\tilde{x}_{(m,b)}[l]=x_{(m,b)}[lQ] \tag{19}$$

[0068] and with the updated filters derived similarly to equation (10), but with respect to $\hat{H}_{(m)}(Z^M)$ (see equation (5)). Following equation (17), this gives

$$\hat{H}_{(m,b)}(Z^M)=\hat{H}_{(m,b)}(Z^{MB/Q})=\hat{H}_{(m,b)}(Z^A) \tag{20}$$

[0069] which is well-defined for integer values of A, and indicates that the filter taps in each path are separated by A samples (or A−1 zeros).

[0070] The output of the filter in each sub-path after the application of the NI, $\tilde{y}_{(m,b)}[l]$, is given similarly to equation (11) as

$$\tilde{y}_{(m,b)}[l]=\sum_{t=0}^{L-1}\tilde{h}_{(m,b)}[t]\tilde{x}_{(m,b)}[l-t], \tag{21}$$

[0071] where L, is the number of non-zero taps of the filter in each sub-path, which, in this case, equal N/(MB).

[0072] The last equation is equivalent to first calculating $y_{(m,b)}[n]$ from Equation (15) and then downsampling by a factor of Q, i.e., $\tilde{y}_{(m,b)}[l]=y_{(m,b)}[lB]$, similarly to equation (8).

[0073] $\{\tilde{y}_{(m,b)}[l]\}_{b=0}^{B-1}$ are now summed in a similar manner to equation (14), i.e.,

$$\tilde{y}_m[l] = \sum_{b=0}^{B-1} \tilde{y}_{(m,b)}[l]. \tag{22}$$

[0074] The extension to the case of bandpass signals is similar to the extension presented in the case of downsampling factors of the form Q=M/A shown above, with the first exponential now adjusted to the new downsampling factor, i.e., as in equation (13), but with Q=MB/A.

Architecture of a Rational Decimation/Interpolation Ratio PP Filter with Gatling-Gun Input Buffer

[0075] Based on the analysis above and adding a novel circuit for fusing sub-paths (in the case of an analysis pipeline) or for expanding the sub-paths (in the case of a synthesis pipeline), we will now disclose an M-path, MB-sub-path PP filter.

[0076] We define a new index, $\tilde{m}$ as:

$$\tilde{m} = m + bM, \tilde{m} = 0, \ldots, MB - 1. \tag{23}$$

[0077] We also note that given $\tilde{m}$, indices m and b, which were defined above for an M-path-based design, can be extracted using:

$$m = \mathrm{mod}(\tilde{m}, M) \tag{24}$$

and

$$b = \mathrm{floor}(\tilde{m}, M) \tag{25}$$

[0078] The paths and sub-paths of an M-path-based design presented above are now arranged according to index $\tilde{m}$ and use suitable MB-sub-paths.

[0079] FIG. **1** is a block diagram that schematically illustrates an Analysis Polyphase (PP) Filter (APP) **100** with rational decimation factor, in accordance with an embodiment that is disclosed herein.

[0080] APP Filter **100** comprises M−1 PP Paths **102** that are driven by the signal x[n], and an Adder **104**, configured to generate the PP filter outputs y[n] according to the sum of the M paths.

[0081] FIG. **1**A is a block diagram that schematically illustrates an index-m PP Path **150** of the APP Filter **100**, in accordance with an embodiment that is disclosed herein. The Path comprises a Path-Delay circuit **152**, which is configured to delay the input signal x[n] by m clock cycles. The delayed input signal then splits to B Sub-Paths **154**. Each Sub-Path **154** comprises a Sub-Path-Delay **156**, a Down-sampler **158**, a FIR Filter **160**, and a Summation circuit **162**.

[0082] Sub-Path-Delay **156** delays the signal by m*M, where m is 0 for the first sub-path (and, hence, the Sub-Path-Delay for the first Sub-Path, with m=0, is not shown), 1 for the next Sub-Path and so on. Sub-Sampler **158** sub-samples the output of the Sub-Path-Delay circuits by a ratio of Q:1. The sub-sampled outputs are denoted $\tilde{x}_{(m,\ i)}[l]$ and the outputs of filter **160** are denoted $\tilde{y}_{(m,i)}[l]$, where m is the path index, ranging from 0 to M−1 and i is the sub-path index, spanning from 0 to B−1.

[0083] PP Path **150** further comprises a First-Exponent circuit **164**, configured to multiply $\tilde{y}_{(m,i)}[l]$ by exp (−jQ*2π/M*kl), and a Second-exponent circuit **166**, configured to multiply the output of First Exponent Circuit **164** by exp (j*2π/M*km).

[0084] FIG. **2** is a block diagram that schematically illustrates an Input Stage **200** of Analysis Polyphase Filter (APP), in accordance with an embodiment that is disclosed herein. Input Stage **200** is identical to Analysis Polyphase Filter (APP) **100** (FIG. **1**), but without the Filters **160**, the Summation Circuits **162**, the First Exponent Circuits **164** and the Second Exponent Circuits **166**. Delay Circuits **204** delay the input signals according to the Path and Sub-Path, and Sub-Samplers **206** sub-sample the delayed signals by a ratio of Q:1.

[0085] FIG. **3** is a block diagram that schematically illustrates a Rearranged Input Stage **300** of a Polyphase FIR Filter, in accordance with an embodiment that is disclosed herein. (Note that both FIG. **2** and FIG. **3** follow the same rearranged input stage; the main difference between them is the application of the Noble Identity on a common group delay over A blocks) The Rearranged Input Stage comprises Paths **300**. The delay circuits **204** (FIG. **2**) are now divided to two—a First Delay **304**, and, where applicable, a Second Delay **306**. The two delays in each path are separated by Sub-Samplers **308**.

[0086] As can be observed in FIG. **3**, only MB/A paths at high-sampling rate are required, while the rest of the paths in the MB-path design can be defined as delayed versions of the first MB/A. This is useful for the construction of an MB-path input data buffer that uses an MB/A-path Gatling gun input buffer.

[0087] FIG. **4** is a block diagram that schematically illustrates an MB/A-path Gatling-Gun Input buffer **400**, in accordance with an embodiment that is disclosed herein.

[0088] Gatling-Gun Input buffer **400** is like Rearranged Input Stage **300**, but the input delays **304** and the Down-Samplers **308** are now replaced with MB/A A-factor commutators **402**, that send selected inputs according to a commutation selection indication, to Delay Lines **404**. We note that a single input data register of dimensions A×N/B is sufficient for computation of all paths using shifts.

[0089] FIG. **5** is a block diagram that schematically illustrates a Group **500** of MB/A FIR Filter Paths **502**, in accordance with an embodiment that is disclosed herein.

[0090] Each FIR Filter Paths **502** comprises a Shift Register **504** that stores the input samples $\tilde{x}_m[l]$, multipliers **506** that multiply taps of the Shift Register **504** by set of respective coefficients and adders **508** that add the multipliers outputs, to generate $\tilde{y}_m[l]$. Note that in various embodiments, Shift Register **504** may be common to all FIR Filter Paths **502**; in other embodiments, two or more of FIR Filter Paths **502** may share a single copy of Shift Register **504**.

[0091] The top MB/A filters use input-signal indices with mod(n,A)=0, and, in general, α group x of MB/A paths uses indices mod(n,A)=α−1.

[0092] FIG. **6**A is a block diagram that schematically illustrates an MB/A-Path Input Data Buffer **600**, in accordance with an embodiment that is disclosed herein.

[0093] FIG. **6**B is a block diagram that schematically illustrates an MB-Path Input Data Buffer **650**, in accordance with an embodiment that is disclosed herein. In both MB/A-Path Input Data Buffer **600** and MB-Path Input Data Buffer **650**, an Input Signal x[n] **602** is stored in an input data buffer. In the case of Input Data Buffer **600**, Commutators **604** send the input data samples to storage cells in an MB-Path Input Data Buffer **606**, and, in the case of Input Data Buffer **650**, a single commutator **652** sends the data samples for storage in an MB/A-Path Input Data Buffer **654**. A State-Engine **608** and a State Engine **656** change state with a periodicity of MB clock cycles, and generate input commutation indications, which governs commutators **604** and **652**, respectively.

[0094] FIG. **7**A is a block diagram that schematically illustrates a complete MB-Path Analysis Polyphase Filter (APPF) **700**, in accordance with an embodiment that is disclosed herein. The MB-Path APPF **700** comprises an Input Data Buffer **704** (which is identical to MB/A-Path Input Data Buffer **600**, FIG. **6**A), an MB-path polyphase filter **708** with a rational decimation factor Q=MB/A, an MB-Path Polyphase Filter **708** (comprising the Group of MB/A FIR Filter Paths **500** (FIG. **5**)), A Sub-Path Fusion Circuit **710**, configured to add the partial sub-path products (producing fused multiplication products), a Circular Output Buffer **712**, configured to periodically output the filtered samples according to an output selection indication, and an M-Point Inverse-Fast-Fourier-Transform (IFFT) circuit **714**, configured to execute the exponent functions **164**, **166** (FIG. **1**B) and generate all the time-domain signals for all M channels. To control both the Input Buffer **704** and the Circular Buffer **712**, APPF **700** further comprises a State-Engine **716** that changes state with a periodicity of MB clock cycles and sends suitable control signals to the Input Buffer and to the Circular Output Buffer.

[0095] In a similar manner, FIG. **7**B is a block diagram that schematically illustrates a complete MB/A-Path Analysis Polyphase Filter (APPF) **750**, in accordance with an embodiment that is disclosed herein. MB/A-Path APPF **750** is like M-Path APPF **700** and comprises the same sub-units, except that the Polyphase Filter **750** comprises an Input Data Buffer **754**, which is identical to MB-Path Input Data Buffer **650**, FIG. **6**B), and except that MB/A-Path APPF **750** comprises a State Engine **766**, to control the Input Data Buffer **754**.

[0096] FIG. **8** is a block diagram that schematically illustrates a Sub-Path Fusion Circuit **800**, in accordance with an embodiment at is disclosed herein. The Sub-Path Fusion Circuit **800** executes the summation of Equation 22, using M Adders **802**, to sum the MB products output from the MB-Path Polyphase Filter into fused multiplication products, which are then input to the circular buffer, according to the output indices $\hat{y}_i[l]$. (We define for $\hat{y}$ anew index $\tilde{m}$, where m scans all m*B m,b combinations.)

Synthesis

[0097] While the Analysis filter decomposes an input signal to sub-bands, the Synthesis filter reconstructs the signal from its M narrowband signals. Rational ratio synthesis polyphase filter can be built from the Analysis design using the Duality Principle.

[0098] FIG. **9** is a block diagram that schematically illustrates a Synthesis Polyphase Filter **900**, in accordance with an embodiment that is disclosed herein. The Polyphase Filter **900** comprises an IFFT circuit **902** that receives a baseband signal and generates an IFTT-transformed baseband signal, a Circular Output Buffer **904** that periodically forwards samples of the input signal according to an output selection indication (sent by the State Engine), a Sub-Path Expansion Circuit **906**, which is the dual counterpart of Sub-Path Fusion Circuit **710** (FIG. **7**A), an MB-Path Polyphase Filter **908**, (which is like MB-Path Polyphase Filter **708**, FIG. **7**A), an MB-Path Input Data Buffer **910**, Rotating-Selectors **912**, which selectively select outputs of the Input Data Buffer **910**, according to a repetitive order, and, an Adder **914**, which sums the outputs of the Rotating Selectors.

[0099] FIG. **10** is a block diagram that schematically illustrates a Sub-Path Expansion Circuit **1000**, in accordance with an embodiment that is disclosed herein. The Sub-Path Expansion Circuit splits the $X_i[l]$ (l is the path index, and i is the signal index, from 0 to B−1), to suitable MB-Path Polyphase Filter inputs, inversely to the operation of Sub-Path Fusion Circuit **800** (FIG. **8**).

[0100] Thus, according to the embodiments disclosed herein above, M-path Polyphase analysis and synthesis filter banks with rational decimation filters can be built; the filters include traditional pipeline stages along with novel fusing/expansion circuits. The filters facilitate a reduced computation load due to the use of an M-path IFFT. The total number of computations is BM for fusing sub-paths M times, plus M*log (M) computations in the IFFT.

Channelizer and Up-Converter

[0101] The rational down/up sampling polyphase filter banks described above can be used, for example, in a Channelizer that separates a broadband input signal into multiple narrow passbands, or in an up-converter, that shifts a baseband channel to a passband within a higher frequency signal. In an embodiment, a Channelizer comprises some or all of the sub-modules of Analysis Polyphase Filter **700** or **750** (FIGS. **7**A, **7**B). In another embodiment, an Up-converter comprises some or all of the sub-modules of a Synthesis Polyphase filter **900** (FIG. **9**).

Methods

[0102] FIG. **11**A is a flowchart **1100** that schematically illustrates a method for rational decimation-rate polyphase FIR analysis, in accordance with an embodiment that is disclosed herein. The flowchart is executed by Analysis Polyphase Filter (APPF) **700** (FIG. **7**A). As described above, an Analysis filter, in the present contents, moves a selected band withing a wideband signal to the baseband.

[0103] The flowchart starts at a Receive Input Sequence operation **1102**, wherein the APPF receives a sequence of input samples X_i, for example, from an Analog to Digital Converter (ADC). Next, at a Store-Input-In-Buffer operation **1104**, the APPF stores the input samples in an input buffer, using a Commutator that is governed by an input commutation indication, sent by the State Engine. The Commutator distributes the samples to buffer cells that will then be accessed for filtering, as described above, with reference to FIGS. **6**A and **6**B.

[0104] Now, at a Multiply-by-Coefficient operation **1106**, the APPF multiplies the samples from the input buffer by corresponding coefficients, separately in each of the A sub-paths of the MB/A paths.

[0105] Next, at a Fuse-Sub-Path operation **1108**, the APPF sums up the products that correspond to the same index i of outputs $\tilde{y}_i[l]$, using Fusion Circuit **800** (FIG. **8**).

[0106] Now, at a Rotating-Output operation **1110**, The APPF, sends the fused results, from the Circular Output Buffer **712** (FIG. **7**) that is governed by the output selection indication (generated by State-Engine **766**), to the IFFT circuit **714**.

[0107] Lastly, at an IFFT operation **1112**, the IFFT circuit **714** (FIG. **7**A) executes an M-point IFFT conversion, to transform the fused results into the APPF outputs 0 through M−1.

[0108] FIG. **11**B is a flowchart **1150** that schematically illustrates a method for rational decimation-rate polyphase FIR synthesis, in accordance with an embodiment that is disclosed herein. The flowchart is executed by Synthesis Polyphase Filter (SPPF) **900** (FIG. **9**), and by sub-unit thereof (all illustrated in FIG. **9**). As described above, a Synthesis filter, in the present contents, moves a baseband signal to a band withing a wideband signal.

[0109] The flowchart starts at an IFFT operation **1152**, wherein IFFT circuit **902** converts the M inputs to a time-domain series. Next, at a Periodic-Sample-Output operation **1154**, the Circular Output Buffer **904** outputs IFFT-converted samples, according to a rotating scheme.

[0110] Now, at an Expand operation **1156**, the Sub-Path-Expansion circuit **906** expands the samples by a ratio of 1:B.

[0111] Next, at a Multiply-by-Coefficients, the samples are multiplied, in separately in each of the A sub-paths of the MB/A paths, and, at a subsequent Assemble-to-Frequencies operation **1160**, groups of products pertaining to the same frequency bands are assembled.

[0112] Now, at a Rotating-Select operation **1162**, Rotating-Selectors **912** select outputs on a rotating order (according to a State-Engine that counts clocks). Lastly, at a Sum Outputs operation **1164**, Adder **924** adds the selected outputs, to form Y[n].

[0113] Although the apparatuses and methods disclosed hereinabove mainly refer to polyphase FIR filter analysis and synthesis, the present invention is not limited to polyphase FIR filters; any other suitable filters may be used in alternative embodiments.

[0114] The configurations of Analysis Filter-Banks **700** and **750**, including Input Data Buffers **704** and **754**, MB-Path Polyphase Filter **708**, Sub-Path Fusion circuit **710** and Circular Output Buffer **712**; the configuration of Synthesis Filter Bank **900**, including Circular Output Buffer **904**, Sub-Path Expansion circuit **906**, MB-Path Polyphase Filter **908**, MB-Path Input Data Buffer **910**, Selector **912** and Adder **914**, including all subcircuits thereof, the methods of flowcharts **1100**, **1150**, illustrated in FIGS. **1** through **11** and described hereinabove, are example configurations and methods that are shown purely for the sake of conceptual clarity. Any other suitable configurations and methods can be used in alternative embodiments.

[0115] The different elements of Analysis Polyphase Filter **700**, **750** and Synthesis Polyphase Filter **900** may be implemented in an integrated circuit, such as an application specific integrated circuit (ASIC) or a field-programmable gate-array (FPGA).

[0116] It will thus be appreciated that the embodiments described above are cited by way of example, and that the present invention is not limited to what has been particularly shown and described hereinabove. Rather, the scope of the present invention includes both combinations and sub-combinations of the various features described hereinabove, as well as variations and modifications thereof which would occur to persons skilled in the art upon reading the foregoing description and which are not disclosed in the prior art. Documents incorporated by reference in the present patent application are to be considered an integral part of the application except that to the extent any terms are defined in these incorporated documents in a manner that conflicts with the definitions made explicitly or implicitly in the present specification, only the definitions in the present specification should be considered.

1. An Analysis Polyphase Filter (APPF) for shifting a selected passband of an input signal to a passband signal, having a Q=M·B/A decimation factor, B and A being co-primes, the APPF comprising M·B Paths, each path comprising (i) M·B/A multiplication Sub-paths, and (ii) a Sub-path Fusion Circuit, which is configured to generate fused multiplication products responsively to a sum of the multiplication products generated by each of the multiplication sub-paths.

2. The APPF according to claim **1**, further comprising an input circuit, configured to receive and temporarily store input samples of the input signal at a subsampling ratio of Q:1.

3. The APPF according to claim **2**, wherein the input circuit comprises a commutator, configured to sample the input signal according to an input commutation indication.

4. The APPF according to claim **1**, further comprising a circular output buffer, configured to output the fused multiplication products in a circular manner according to an output selection indication.

5. The APPF according to claim **1**, further comprising an M-point Inverse-Fast-Fourier-Transform (IFFT) circuit, configured to convert the fused multiplication products into a polyphase-filtered output signal.

6. The APPF according to claim **1**, further comprising a state engine, configured to generate an input commutation indication and an output selection indication.

7. A Synthesis Polyphase Filter (SPPF) for shifting a baseband signal to a passband of an output signal, having a Q=M·B/A interpolation factor, B and A being co-primes, the SPPF comprising (i) M·B Paths, each path comprising M·B/A multiplication Sub-paths, and (ii) a Sub-path Expansion Circuit, which is configured to split multiplication products from the multiplication sub-paths.

8. The SPPF according to claim **7**, further comprising an M-point Inverse-Fast-Fourier-Transform (IFFT) circuit, configured to perform an Inverse-Fourier-Transform of the baseband signal, thereby producing an IFFT-transformed baseband signal.

9. The SPPF according to claim **8**, further comprising a Circular Output Buffer, configured to receive, buffer and periodically output the IFFT-transformed baseband signal according to an output selection indication.

10. The SPPF according to claim **7**, further comprising a state engine, to generate an output selection indication.

11. A Channelizer for shifting a passband in an input signal to a baseband signal, the channelizer comprising an Analysis polyphase Filter (APPF), having a Q=M·B/A decimation/interpolation factor, B and A being co-primes, the APPF comprising M·B Paths, each path comprising (i) M·B/A multiplication Sub-paths and (ii) a Sub-path Fusion Circuit, which is configured to generate fused multiplication

products responsively to a sum of the multiplication products generated by each of the multiplication sub-paths.

12. An Up-Converter for shifting a baseband signal to a passband within an output signal, the Up-Converter comprising a Synthesis Polyphase Filter (SPPF), having a Q=M·B/A decimation/interpolation factor, B and A being co-primes, the SPPF comprising M·B Paths, each path comprising (i) M·B/A multiplication Sub-paths and (ii) a Sub-path Expansion Circuit, which is configured to split multiplication products from the multiplication sub-paths.

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