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SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

Abstract

A semiconductor device and a method for manufacturing the semiconductor device are provided. The semiconductor device includes a first back metal structure, a first conductive structure, a metal layer structure and a second metal structure. The first back metal structure belongs to a first power domain, and the first back metal structure is formed on a back side of the wafer. The first conductive structure extends in a first direction, is formed above the first back metal structure, and is P-type. The metal layer structure extends in a second direction vertical to the first direction and is formed above the first conductive structure. The second metal structure belongs to a second power domain different from the first power domain.

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Background/Summary

BACKGROUND

[0001] The present disclosure relates, in general, to semiconductor devices and methods for manufacturing the same. Specifically, the present disclosure relates to semiconductor devices and methods for manufacturing semiconductor devices with a header cell for power delivery.

[0002] Integrated circuits that involve semiconductor devices are essential for many modern applications. Technological advances in materials and design have produced semiconductor devices composed of smaller and more complex elements each generation. Although power consumption per element is reduced by miniaturization and reductions in voltage of elements, power consumption of the entire integrated circuit is rising due to increase in the number of elements. Therefore, a novel design of a header cell as a power switch cell is needed to control power delivery and improve compatibility with other functional cells.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Aspects of the embodiments of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It should be noted that, in accordance with standard practice in the industry, various structures are not drawn to scale. In fact, the dimensions of the various structures can be arbitrarily increased or reduced for clarity of discussion.

[0004] FIG. **1**A is a schematic view of a semiconductor device on a wafer, in accordance with some embodiments of the present disclosure.

[0005] FIG. **1**B is a schematic view of a design layout of another semiconductor device, in accordance with some embodiments of the present disclosure.

[0006] FIG. **1**C is a schematic view of a design layout of another semiconductor device, in accordance with some embodiments of the present disclosure.

[0007] FIG. **1**D is a schematic view of a design layout of another semiconductor device, in accordance with some embodiments of the present disclosure.

[0008] FIG. **2**A is a schematic diagram of a semiconductor device, in accordance with some embodiments of the present disclosure.

[0009] FIG. **2**B is a schematic diagram of a design layout of a semiconductor device, in accordance with some embodiments of the present disclosure.

[0010] FIG. **2**C illustrates cross-section views of a semiconductor device along the section lines C**2** and D**2** in FIG. **2**B, in accordance with some embodiments of the present disclosure.

[0011] FIG. **3**A is a schematic diagram of a semiconductor device, in accordance with some embodiments of the present disclosure.

[0012] FIG. **3**B is a schematic diagram of a design layout of a semiconductor device, in accordance with some embodiments of the present disclosure.

[0013] FIG. **3**C illustrates cross-section views of a semiconductor device along the section lines C**3** and D**3** in FIG. **3**B, in accordance with some embodiments of the present disclosure.

[0014] FIG. **4**A is a schematic diagram of a design layout of a semiconductor device, in accordance with some embodiments of the present disclosure.

[0015] FIG. **4**B illustrates cross-section views of a semiconductor device along the section lines C**4** and D**4** in FIG. **4**A, in accordance with some embodiments of the present disclosure.

[0016] FIG. **5**A is a schematic diagram of a design layout of a semiconductor device, in accordance with some embodiments of the present disclosure.

[0017] FIG. **5**B illustrates cross-section views of a semiconductor device along the section lines C**5** and D**5** in FIG. **5**A, in accordance with some embodiments of the present disclosure.
[0018] FIG. **6**A is a schematic diagram of a semiconductor device, in accordance with some embodiments of the present disclosure.
[0019] FIG. **6**B illustrates cross-section views of two semiconductor devices along the section lines C**61** and C**62**, in accordance with some embodiments of the present disclosure.
[0020] FIG. **7**A is a schematic diagram of a design layout of a semiconductor device, in accordance with some embodiments of the present disclosure.
[0021] FIG. **7**B is a schematic diagram of a design layout of another semiconductor device, in accordance with some embodiments of the present disclosure.
[0022] FIG. **8**A is a schematic diagram of a semiconductor device, in accordance with some embodiments of the present disclosure.
[0023] FIG. **8**B is a schematic diagram of a design layout of a semiconductor device, in accordance with some embodiments of the present disclosure.
[0024] FIG. **8**C illustrates cross-section views of a semiconductor device along the section lines C**8** and D**8** in FIG. **8**B, in accordance with some embodiments of the present disclosure.
[0025] FIG. **9**A is a schematic diagram of a design layout of a semiconductor device, in accordance with some embodiments of the present disclosure.
[0026] FIG. **9**B illustrates cross-section views of a semiconductor device along the section lines C**9** and D**9** in FIG. **9**A, in accordance with some embodiments of the present disclosure.
[0027] FIG. **10**A is a schematic diagram of a design layout of a semiconductor device, in accordance with some embodiments of the present disclosure.
[0028] FIG. **10**B illustrates cross-section views of a semiconductor device along the section lines C**10** and D**10** in FIG. **10**A, in accordance with some embodiments of the present disclosure.
[0029] FIG. **11**A is a schematic diagram of a design layout of a semiconductor device, in accordance with some embodiments of the present disclosure.
[0030] FIG. **11**B illustrates cross-section views of a semiconductor device along the section lines C**11** and D**11** in FIG. **11**A, in accordance with some embodiments of the present disclosure.
[0031] FIG. **12**A is a schematic diagram of a design layout of a semiconductor device, in accordance with some embodiments of the present disclosure.
[0032] FIG. **12**B illustrates cross-section views of a semiconductor device along the section lines C**12** and D**12** in FIG. **12**A, in accordance with some embodiments of the present disclosure.
[0033] FIG. **13**A is a schematic diagram of a design layout of a semiconductor device, in accordance with some embodiments of the present disclosure.
[0034] FIG. **13**B illustrates cross-section views of a semiconductor device along the section lines C**13** and D**13** in FIG. **13**A, in accordance with some embodiments of the present disclosure.

DETAILED DESCRIPTION

[0035] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of elements and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features can be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.
[0036] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “over,” “upper,” “on” and the like, can be used herein for ease of description to describe one element or

feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus can be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0037] As used herein, although terms such as “first,” “second” and “third” describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms may only be used to distinguish one element, component, region, layer or section from another. Terms such as “first,” “second” and “third” when used herein do not imply a sequence or order unless clearly indicated by the context.

[0038] Notwithstanding that the numerical ranges and parameters setting forth the broad scope of the disclosure are approximations, the numerical values set forth in the specific examples are reported as precisely as possible. Any numerical value, however, inherently contains certain errors necessarily resulting from the standard deviation found in the respective testing measurements. Also, as used herein, the terms “substantially,” “approximately” and “about” generally mean within a value or range that can be contemplated by people having ordinary skill in the art. Alternatively, the terms “substantially,” “approximately” and “about” mean within an acceptable standard error of the mean when considered by one of ordinary skill in the art. People having ordinary skill in the art can understand that the acceptable standard error may vary according to different technologies. Other than in the operating/working examples, or unless otherwise expressly specified, all of the numerical ranges, amounts, values and percentages such as those for quantities of materials, durations of times, temperatures, operating conditions, ratios of amounts, and the likes thereof disclosed herein should be understood as modified in all instances by the terms “substantially,” “approximately” or “about.” Accordingly, unless indicated to the contrary, the numerical parameters set forth in the present disclosure and attached claims are approximations that can vary as desired. At the very least, each numerical parameter should at least be construed in light of the number of reported significant digits and by applying ordinary rounding techniques. Ranges can be expressed herein as from one endpoint to another endpoint or between two endpoints. All ranges disclosed herein are inclusive of the endpoints, unless specified otherwise.

[0039] FIG. **1**A is a schematic view of a semiconductor device **10** on a wafer **10***w*, in accordance with some embodiments of the present disclosure. The semiconductor device **10** can include, for example, an N-type metal-oxide-semiconductor (NMOS) device, a P-type metal-oxide-semiconductor (PMOS) device, a complementary metal-oxide-semiconductor (CMOS) device, and can be implemented using a planar field-effect transistor (FET) device, a fin-type FET (FinFET) device, a gate-all-around (GAA) device, a nanowire device, a fully-depleted silicon-on-isolator (FDSOI) device, or the like. The wafer **10***w* includes a semiconductor substrate and optionally various layers formed thereon.

[0040] Referring to FIG. **1**A, the semiconductor device **10** includes a header cell **102**, multiple conductive contacts **104** for receiving power supplies and multiple metal structures M**11** to BM**1**N each extending along the X direction substantially parallel with each other. The header cell **102** spans the front side **10**FS and the back side **10**BS of the wafer **10***w*. The front side **10**FS is opposite to the back side **10**BS. The conductive contacts **104** can be electrically connected to a power source for providing power to the semiconductor device **10**. In FIG. **1**, the header cell **102** is represented by an empty dotted-box, without content therein. The details of the header cell **102** will be discussed later in accordance with FIGS. **1**B, **1**C, and **1**D.

[0041] The metal structures M**11** and M**10**, the latter of which includes two metal structures M**10**V and M**10**T, are formed on the front side **10**FS of the wafer **10***w*. The metal structure M**11** is formed above the header cell **102** and the metal structures M**10**V and M**10**T. The conductive contacts **104** and the metal structures BM**10**, BM**11** to BM**1**N-**1** and BM**1**N are formed on the back side **10**BS of the wafer **10***w*. The metal structure BM**10** includes two metal structures BM**10**V and BM**10**T

separated by the header cell **102**. The via structure **106**A is formed between the metal structures BM**10**T and BM**11**. The via structures **106**B are formed between the metal structures BM**1**N-**1** and BM**1**N. The via structures **106**A and **106**B extend along the Z direction vertical to the X direction.
[0042] The header cell **102** can include a power switch cell to control power delivery of the semiconductor device **10**. The technique of power gating may reduce power leakage when a system is not actively operating. The header cell **102** may provide a positive supply voltage VDD to other cells or elements of the semiconductor device **10**. The metal structures M**11** to BM**1**N, the conductive contacts **104**, and the via structures **106**A and **106**B are made of metal, such as copper, aluminum, tungsten, titanium, tantalum, an alloy thereof or the like, and are electrically insulated by dielectric materials (not separately shown) such as oxide, nitride, oxynitride and the like.
[0043] In some embodiments, the metal structures M**10**V and BM**10**V belong to a virtual power domain. The virtual power domain is configured to transmit power from the header cell **102** to a standard cell or a functional cell which includes various kinds of logic gates or electronic elements. In some embodiments, the metal structures M**10**T, BM**10**T, BM**11** to BM**1**N-**1** and BM**1**N belong to a true power domain. The true power domain is configured to transmit power from a power supply or a power source to the header cell **102**. The semiconductor device **10** can belong to a super power rail (SPR) chip design which includes or provides a power delivery network through the front side **10**FS and the back side **10**BS of the wafer **10***w*.
[0044] FIG. **1**B is a schematic view of a design layout of the semiconductor device **10**A, in accordance with some embodiments of the present disclosure. The semiconductor device **10**A of FIG. **1**B can correspond to a top view of the header cell **102** of the semiconductor device **10** of FIG. **1**A.
[0045] The semiconductor device **10**A includes several metal structures BM**10**V and BM**10**T extending along the X direction. The semiconductor device **10**A includes multiple conductive structures POD**1**A, POD**1**B, POD**1**C and POD**1**D extending along the X direction. The conductive structures POD**1**A to POD**1**D can include a P-type active region, also referred to herein as oxide-diffusion ("OD") regions. The active region may be used to form source/drain regions and a channel region between the source/drain regions of a transistor device. The semiconductor device **10**A includes multiple PMOS devices without NMOS devices to reduce turn-on resistance.
[0046] The metal structures BM**10**T can partially overlap with the conductive structures POD**1**B and POD**1**C from a top-view perspective of the design layout. The header cell height CH**1**A can be defined as the distance between the two metal structures BM**10**V. The header cell width CW**1**A can be defined as the length of the conductive structures POD**1**A to POD**1**D along the X direction. In some embodiments, the header cell height CH**1**A can be twice the standard cell height, which is determined as the distance between two successive conductive structures, such as the conductive structures POD**1**A and POD**1**B. The header cell width CW**1**A can be greater than the header cell height CH**1**A.
[0047] FIG. **1**C is a schematic view of a design layout of the semiconductor device **10**B, in accordance with some embodiments of the present disclosure. The semiconductor device **10**B of FIG. **1**C can correspond to a top view of the header cell **102** of the semiconductor device **10** of FIG. **1**A. The semiconductor device **10**B of FIG. **1**C can be similar to the semiconductor device **10**A of FIG. **1**B. The semiconductor device **10**B has a header cell height CH**1**B and a header cell width CW**1**B.
[0048] In some embodiments, the semiconductor device **10**B includes multiple PMOS devices and NMOS devices. The semiconductor device **10**B includes conductive structures POD**1**A and POD**1**B. The semiconductor device **10**B includes conductive structures NOD**1**A and NOD**1**B. The conductive structures POD**1**A and POD**1**B can be P-type, which means including a P-type active region. The conductive structures NOD**1**A and NOD**1**B can be N-type, which means including a N-type active region. The metal structures BM**10**T can partially overlap with the conductive structures NOD**1**A and NOD**1**B from a top-view perspective of the design layout.

[0049] FIG. **1**D is a schematic view of a design layout of the semiconductor device **10**C, in accordance with some embodiments of the present disclosure. The semiconductor device **10**C can correspond to a portion of a functional cell or a standard cell. The semiconductor device **10**C has a cell height CH**1**C and a cell width CW**1**C.
[0050] In some embodiments, the semiconductor device **10**C includes multiple PMOS devices and NMOS devices. The semiconductor device **10**C includes conductive structures POD**1**C and NOD**1**C. The conductive structure POD**1**C can include a P-type active region. The conductive structures NOD**1**C can include an N-type active region. The cell width CW**1**C can be substantially identical to the header cell widths CW**1**A and CW**1**B. The cell height CH**1**C can be smaller than the header cell heights CH**1**A and CH**1**B. The cell height CH**1**C can be substantially half of the header cell heights CH**1**A and CH**1**B.
[0051] In some embodiments, the header cell of the semiconductor device **10**A of FIG. **1**B including PMOS device is exclusive to or not compatible with the standard cell of the semiconductor device **10**C of FIG. **1**D including both PMOS device and NMOS device. In some embodiments, the header cell of the semiconductor device **10**B of FIG. **1**C including both PMOS device and NMOS device is compatible with the standard cell of the semiconductor device **10**C of FIG. **1**D including both PMOS device and NMOS device. The header cell of the semiconductor device **10**B of FIG. **1**C shares the same configuration of both PMOS device and NMOS device as the standard cell of the semiconductor device **10**C of FIG. **1**D. Therefore, the header cell of the semiconductor device **10**B of FIG. **1**C provides an advantage of higher capacity of integrating with other standard cells on the same chip.
[0052] FIG. **2**A is a schematic diagram of a semiconductor device **201**, in accordance with some embodiments of the present disclosure. The semiconductor device **201** can correspond to the header cell as illustrated in the embodiments of FIG. **1**A and FIG. **1**C.
[0053] The semiconductor device **201** includes a PMOS transistor T**21** and an NMOS transistor T**22**. The PMOS transistor T**21** includes drain D**21**, gate G**21** and source S**21**. The NMOS transistor T**22** includes drain D**22**, gate G**22** and source S**22**. A source/drain region(s) may refer to a source or a drain, individually or collectively depending upon the context. In some embodiments, the gate G**21** can be used to receive a control signal. The gate G**22** and source S**22** are floating without being electrically connected to other signals and elements. The NMOS transistor T**22** can be used as a dummy transistor for providing a signal path or a current path between drain D**22** and source S**21**.
[0054] FIG. **2**B is a schematic diagram of a design layout of a semiconductor device **202**, in accordance with some embodiments of the present disclosure. The semiconductor device **202** of FIG. **2**B can correspond to the semiconductor device **201** of FIG. **2**A.
[0055] The semiconductor device **202** includes several metal structures BM**21**, BM**22** and BM**23**, several conductive structures POD**21**, NOD**21**, NOD**22** and POD**22**, several gates PO**2**, several via structures VB**21**, several metal layer structures MD**21**, and several isolating structures CPO**2**. The conductive structures POD**21** to NOD**22**, the gates PO**1**, the metal layer structures MD**21**, and the isolating structures CPO**2** are formed within the boundary BD**2**. The isolating structures CPO**2** are used to avoid short-circuiting so that the conductive structure POD**21** is void of electrically connected to the conductive structure NOD**21**. The voltage structures VS**21** and VS**22** are formed outside the boundary BD**2**. The voltage structures VS**21** and VS**22** are spaced apart from the metal structure BM**22**. The metal structure BM**21** can be electrically connected to the drain D**21** of the PMOS transistor T**21** of FIG. **2**A. The metal structure BM**22** can be electrically connected to the drain D**22** of the NMOS transistor T**22** of FIG. **2**A. The voltage structures VS**21** and VS**22** can be grounded or electrically connected to a voltage source VSS.
[0056] As shown in FIG. **2**B, the metal structures BM**21**, BM**22** and BM**23** extend along the X direction. The metal structure BM**21** is spaced apart or separated from the metal structure BM**22** along the Y direction. The metal structure BM**22** is spaced apart or separated from the metal

structure BM**23** along the Y direction. The conductive structures POD**21**, NOD**21**, NOD**22** and POD**22** extend along the X direction. The gates PO**2** extend along the Y direction. The metal layer structures MD**21** extend along the Y direction. The conductive structures POD**21** and POD**22** are P-type active regions, and the conductive structures NOD**21** and NOD**22** are N-type active regions. The metal layer structures MD**21** can have material similar to that of the metal structures BM**21** to BM**23**.

[0057] In some embodiments, the metal structures BM**21** and BM**23** belong to a true power domain. The metal structure BM**22** belongs to virtual power domain. In some embodiments, the conductive structure POD**21** overlaps with the metal structure BM**21** from a top-view perspective of the design layout. The conductive structure POD**22** overlaps with the metal structure BM**23** from a top-view perspective of the design layout. The conductive structures NOD**21** and NOD**22** partially overlap with the metal structure BM**22** from a top-view perspective of the design layout. The conductive structures NOD**21** and NOD**22** are within the metal structure BM**22** from a top-view perspective of the design layout.

[0058] The semiconductor device **202** has a header cell height CH**2** along the Y direction and a header cell width CW**2** along the X direction. The header cell height CH**2** can be twice the standard cell height, which is determined as the distance between two successive conductive structures, such as the conductive structures POD**21** and NOD**21**. The header cell width CW**2** can be in a range of 3 to 256 pitches, and the pitch is defined as the distance between two successive gates PO**2**. The width of the metal structure BM**22** along the Y direction is greater than the width of the conductive structures NOD**21** and NOD**22** along the Y direction. The width of the metal structure BM**22** along the Y direction is greater than twice the width of the conductive structures NOD**21** and NOD**22** along the Y direction.

[0059] FIG. **2**C illustrates cross-section views of the semiconductor device **203** along the section lines C**2** and D**2** in FIG. **2**B, in accordance with some embodiments of the present disclosure. The semiconductor device **203** of FIG. **2**C can correspond to a portion of the semiconductor device **202** of FIG. **2**B.

[0060] Referring to FIG. **2**C, along the section line C**2**, the conductive structure NOD**21** is formed above the metal structure BM**22** along the Z direction. The via structure VB**22** is formed on the metal structure BM**21** along the Z direction, and the conductive structure POD**21** is formed on the via structure VB**22** along the Z direction. The conductive structure POD**21** can be in direct contact with the via structure VB**22**, and a hetero-junction interface can be formed therebetween.

[0061] In some embodiments, along the section line D**2**, the via structure VB**23** is formed on the metal structure BM**22** along the Z direction. The conductive structure NOD**21** is formed on the via structure VB**23** along the Z direction. The conductive structure NOD**21** can be in direct contact with the via structure VB**23**, and a hetero-junction interface can be formed therebetween. The metal layer structure MD**21** is formed on the conductive structures NOD**21** and POD**21** along the Z direction. The metal layer structure MD**21** can be in direct contact with the conductive structures NOD**21** and POD**21**. In some embodiments, the metal structures BM**21** and BM**22** are formed on the back side of the wafer. The conductive structures NOD**21** and POD**21** are formed on the front side of the wafer. The metal layer structure MD**22** is formed on the front side of the wafer. In some embodiments, a path can be provided to electrically connect the metal structure BM**22** (corresponding to the drain D**22**) to the source S**21** through the via structure VB**23**, the conductive structure NOD**21** and the metal layer structure MD**22**.

[0062] FIG. **3**A is a schematic diagram of a semiconductor device **301**, in accordance with some embodiments of the present disclosure. The semiconductor device **301** of FIG. **3**A can be similar to the semiconductor device **201** of FIG. **2**A.

[0063] The semiconductor device **301** includes a through via structure FT**3** and a PMOS transistor T**31** with gate G**31**, drain D**31** and source S**31**. The through via structure FT**3** is electrically connected between the source S**31** and the node N**31**. The through via structure FT**3** is used to

replace NMOS transistor T**22** of FIG. **2**A to decrease the turn-on resistance of the semiconductor device **301**. The through via structure FT**3** is made of metal, such as copper, aluminum, tungsten, titanium, tantalum, an alloy thereof or the like, and is electrically insulated by dielectric materials (not separately shown) such as oxide, nitride, oxynitride and the like.

[0064] FIG. **3**B is a schematic diagram of a design layout of a semiconductor device **302**, in accordance with some embodiments of the present disclosure. The semiconductor device **302** of FIG. **3**B can correspond to the semiconductor device **301** of FIG. **3**A. The metal structure BM**31** can be electrically connected to the drain D**31** of FIG. **3**A. The metal structure BM**32** can be electrically connected to the node N**31** of FIG. **3**A.

[0065] The semiconductor device **302** includes the metal structures BM**31**, BM**32** and BM**33** along the X direction, the conductive structures POD**31** and POD**32** along the X direction, several metal layer structures MD**31** along the Y direction, and a through via structure FT**3** extending along the X direction. The semiconductor device **302** has a header cell height CH**3** and a header cell width CW**3**. The metal structures BM**31** and BM**33** belong to a virtual power domain. The metal structure BM**32** belongs to a true power domain.

[0066] In some embodiments, the through via structure FT**3** overlaps a portion of the metal structure BM**32** from a top-view perspective of the design layout. The through via structure FT**3** is formed within the metal structure BM**32** from a top-view perspective of the design layout. The length of the through via structure FT**3** along the X direction is smaller than the length of the metal structure BM**32** along the X direction. The width of the through via structure FT**3** along the Y direction is smaller than the width of the metal structure BM**32** along the Y direction.

[0067] FIG. **3**C illustrates cross-section views of a semiconductor device **303** along the section lines C**3** and D**3** in FIG. **3**B, in accordance with some embodiments of the present disclosure. The semiconductor device **303** of FIG. **3**C can correspond to a portion of the semiconductor device **302** of FIG. **3**B and can be similar to the semiconductor device **203** of FIG. **2**C.

[0068] Along the section line C**3**, the through via structure FT**3** is formed on the metal structure BM**32** along the Z direction. The conductive structure POD**32** and the via structure VB**31** are formed on the metal structure BM**31** along the Z direction. Along the section line D**3**, the through via structure FT**3** is formed on the metal structure BM**32** along the Z direction. The metal layer structure MB**32** is formed on the through via structure FT**3** and the conductive structure POD**32**. The through via structure FT**3** is formed between the metal structure BM**23** and the metal layer structure MD**32**. In some embodiments, the size of the through via structure FT**3** is greater than the size of the via structure VB**31** to reduce the resistance. The metal structures BM**31** and BM**32** are formed on the back side of the wafer. The through via structure FT**3** can be formed on the front side of the wafer.

[0069] FIG. **4**A is a schematic diagram of a design layout of a semiconductor device **401**, in accordance with some embodiments of the present disclosure. The semiconductor device **401** of FIG. **4**A can be similar to the semiconductor device **202** of FIG. **2**B and correspond to the semiconductor device **201** of FIG. **2**A.

[0070] Referring to FIG. **4**A, the semiconductor device **401** includes the metal structures M**41**, M**42** and BM**41** along the X direction, the conductive structures POD**41**, POD**42**, NOD**41** and NOD**42** along the X direction, and multiple via structures VD**41**. The metal structures M**41** and M**42** belong to a virtual power domain. The metal structure BM**41** belongs to a true power domain.

[0071] In some embodiments, the conductive structures NOD**41** and NOD**42** overlap a portion of the metal structure BM**41** from a top-view perspective of the design layout. The conductive structures NOD**41** and NOD**42** are formed within the metal structure BM**41** from a top-view perspective of the design layout. The width of the conductive structures NOD**41** and NOD**42** along the Y direction is smaller than the width of the metal structure BM**41** along the Y direction. The width of the metal structure BM**41** along the Y direction is greater than twice the width of the conductive structures NOD**41** and NOD**42** along the Y direction.

[0072] In some embodiments, the width of the conductive structures POD**41** and POD**42** along the Y direction is smaller than the width of the metal structures M**41** and M**42** along the Y direction. The conductive structure POD**41** is formed between and spaced apart from the metal structures M**41** and BM**41**. The conductive structure POD**42** is formed between and spaced apart from the metal structures M**42** and BM**41**.

[0073] FIG. **4**B illustrates cross-section views of a semiconductor device **402** along the section lines C**4** and D**4** in FIG. **4**A, in accordance with some embodiments of the present disclosure. The semiconductor device **402** of FIG. **4**B can be similar to the semiconductor device **203** of FIG. **2**C and correspond to a portion of the semiconductor device **201** of FIG. **2**A.

[0074] Along the section line C**4**, the metal layer structure MD**41** is formed on the conductive structure POD**41** along the Z direction. The via structure VD**42** is formed between the metal structure M**41** and the metal layer structure MD**41**. Along the section line D**4**, the metal layer structure MD**42** is formed on the conductive structures NOD**41** and POD**41** along the Z direction. The metal structures BM**41** and BM**42** are formed on the back side of the wafer. The POD**41**, POD**42**, NOD**41** and NOD**42** are formed on the front side of the wafer. The metal structure M**41** is formed on the front side of the wafer.

[0075] FIG. **5**A is a schematic diagram of a design layout of a semiconductor device **501**, in accordance with some embodiments of the present disclosure. The semiconductor device **501** of FIG. **5**A can be similar to the semiconductor device **302** of FIG. **3**B and the semiconductor device **401** of FIG. **4**A, and correspond to the semiconductor device **301** of FIG. **3**A.

[0076] The semiconductor device **501** includes the metal structures M**51**, M**52** and BM**51** along the X direction, the conductive structures POD**51** and POD**52** along the X direction, and the through via structure FT**5** extending along the X direction. The metal structures M**51** and M**52** belong to a virtual power domain. The metal structure BM**51** belongs to a true power domain.

[0077] FIG. **5**B illustrates cross-section views of a semiconductor device **502** along the section lines C**5** and D**5** in FIG. **5**A, in accordance with some embodiments of the present disclosure. The semiconductor device **502** of FIG. **5**B can be similar to the semiconductor device **303** of FIG. **3**C and the semiconductor device **402** of FIG. **4**B.

[0078] Along the section line C**5**, the through via structure FT**5** is formed on the metal structure BM**51** along the Z direction. The metal layer structure MD**51** is formed on the conductive structure POD**51** along the Z direction. The via structure VD**52** is formed between the metal structure M**51** and the metal layer structure MD**51**. Along the section line D**5**, the metal layer structure MD**52** is formed on the conductive structures POD**51** and the through via structure FT**5** along the Z direction. The metal structures BM**51** and BM**52** are formed on the back side of the wafer. The conductive structure POD**51** and the through via structure FT**5** are formed on the front side of the wafer. The metal structure M**51** is formed on the front side of the wafer.

[0079] FIG. **6**A is a schematic diagram of a semiconductor device **601**, in accordance with some embodiments of the present disclosure. The semiconductor device **601** of FIG. **6**A can be similar to the semiconductor device **201** of FIG. **2**A. The semiconductor device **601** includes a PMOS transistor T**61** including gate G**61**, drain D**61** and source S**61**. The drain D**61** is electrically connected to two nodes N**61** and N**62**.

[0080] FIG. **6**B illustrates cross-section views of two semiconductor devices **602** and **603** along the section lines C**61** and C**62**, in accordance with some embodiments of the present disclosure. The embodiment of the section line C**61** can correspond to both embodiments of the section line C**2** in FIG. **2**C and the section line C**4** in FIG. **4**B. The embodiment of the section line C**62** can correspond to both embodiments of the section line C**3** in FIG. **3**C and the section line C**5** in FIG. **5**B.

[0081] Along the section line C**61**, the metal structure BM**61** can be electrically connected to the source S**61** of FIG. **6**A. The metal structure BM**62** can be electrically connected to the node N**61** of FIG. **6**A. The metal structure M**61** can be electrically connected to the node N**62** of FIG. **6**A. The

metal structures BM**61** and BM**61** are formed on the back side of the wafer. The conductive structure POD**6**, the metal layer structure MD**6**, the via structures VB**6** and VD**6** and the metal structure M**61** are formed on the front side of the wafer.

[0082] Along the section line C**62**, the metal structure BM**61** can be electrically connected to the source S**61** of FIG. **6**A. The metal structure BM**62** can be electrically connected to the node N**61** of FIG. **6**A. The metal structure M**61** can be electrically connected to the node N**62** of FIG. **6**A. The metal structures BM**61** and BM**61** are formed on the back side of the wafer. The through via structure FTV**6**, the conductive structure POD**6**, the metal layer structure MD**6**, the via structures VB**6** and VD**6** and the metal structure M**61** are formed on the front side of the wafer.

[0083] FIG. **7**A is a schematic diagram of a design layout of a semiconductor device **701**, in accordance with some embodiments of the present disclosure. The semiconductor device **701** of FIG. **7**A can be similar to the semiconductor device **202** of FIG. **2**B.

[0084] The semiconductor device **701** includes several metal structures BM**71** and BM**71**, several conductive structures POD**71**, NOD**71**, NOD**72** and POD**72**, and a control circuit C**71**. The control circuit C**71** can include an inverter chain or a buffer chain to control the turn-on and turn-off of the semiconductor device **701** including or correspond to a header cell. The control circuit C**71** includes two inverters IV**71** and IV**72**. Each of the inverters IV**71** and IV**72** can include a NMOS transistor and a PMOS transistor. The inverters IV**71** and IV**72** can be used to generate the control signal to the gate, such as the gate G**21** in FIG. **2**A. The control circuit C**71** is built-in or embedded within the header cell of the semiconductor device **701**.

[0085] FIG. **7**B is a schematic diagram of a design layout of another semiconductor device **702**, in accordance with some embodiments of the present disclosure. The semiconductor device **702** of FIG. **7**B can be similar to the semiconductor device **302** of FIG. **3**B and the semiconductor device **701** of FIG. **7**A. The semiconductor device **701** includes a control circuit C**72** and a through via structure FTV**7**. The control circuit C**72** can include an inverter chain or a buffer chain to control the turn-on and turn-off of the semiconductor device **702** as a header cell. The control circuit C**72** includes two inverters IV**71** and IV**72**. Each of the inverters IV**71** and IV**72** can include a NMOS transistor and a PMOS transistor. The inverters IV**71** and IV**72** can be used to generate the control signal to the gate, such as the gate G**21** in FIG. **2**A. The control circuit C**72** is built-in or embedded within the header cell of the semiconductor device **702**.

[0086] FIG. **8**A is a schematic diagram of a semiconductor device **801**, in accordance with some embodiments of the present disclosure. The semiconductor device **801** can correspond to or belong to a portion of the header cell. The semiconductor device **801** includes a PMOS transistor T**81**. The semiconductor device **801** is void of NMOS transistors. The PMOS transistor T**81** includes drain D**81**, gate G**81** and source S**81**. The gate G**81** is used to receive a control signal.

[0087] FIG. **8**B is a schematic diagram of a design layout of a semiconductor device **802**, in accordance with some embodiments of the present disclosure. The semiconductor device **802** can correspond to the semiconductor device **801** of FIG. **8**A or be similar to the semiconductor device **202** of FIG. **2**B.

[0088] The semiconductor device **802** includes two metal structures BM**81** and BM**82** extending along the X direction, and a conductive structure POD**8** extending along the Y direction. The metal structure BM**82** is electrically connected to drain D**81** of FIG. **8**A. The metal structure BM**81** is electrically connected to source S**81** of FIG. **8**A. The conductive structure POD**8** partially overlaps the metal structure BM**81** from a top-view perspective of the design layout. The conductive structure POD**8** partially overlaps the metal structure BM**82** from a top-view perspective of the design layout. The metal structure BM**81** belongs to a true power domain. The metal structure BM**82** belongs to a virtual power domain.

[0089] The header cell of the semiconductor device **802** can have more flexibility than a standard cell and have more additional layout structures. The header cell of the semiconductor device **802** can be used, for example, as a static random-access memory (SRAM) circuit or an input-output

(I/O) circuit. The widths of the metal structures BM**81** and BM**82** along the Y direction can be increased to enhance the IR drop, which is proportional to resistance. In addition, NMOS transistors is unnecessary for the header cell of the semiconductor device **802**.

[0090] FIG. **8**C illustrates cross-section views of a semiconductor device **803** along the section lines C**8** and D**8** in FIG. **8**B, in accordance with some embodiments of the present disclosure. The semiconductor device **803** can correspond to the semiconductor device **802** of FIG. **8**B.

[0091] Along the section line C**8**, the metal layer structure MD**8**, the conductive structure POD**8** and the via structure VB**81** are formed on the metal structure BM**81** along the Z direction. The metal structure BM**81** is formed on the back side of the wafer. The metal layer structure MD**8**, the conductive structure POD**8** and the via structure VB**81** are formed on the front side of the wafer. The conductive structure POD**8** include P-type active regions. Along the section line D**8**, the conductive structure POD**8** and the via structure VB**82** are formed on the metal structure BM**82** along the Z direction. The metal structure BM**82** is formed on the back side of the wafer. The conductive structure POD**8** and the via structure VB**82** are formed on the front side of the wafer.

[0092] FIG. **9**A is a schematic diagram of a design layout of a semiconductor device **901**, in accordance with some embodiments of the present disclosure. The semiconductor device **901** can correspond to the semiconductor device **801** of FIG. **8**A or be similar to the semiconductor device **802** of FIG. **8**B. The semiconductor device **901** includes four metal structures M**91**, M**92**, BM**91** and BM**92** extending along the X direction. The metal structures M**91** and M**92** belong to a virtual power domain. The metal structures BM**91** and BM**92** belong to a true power domain. The metal structures M**91** and M**92** are electrically connected to drain D**81** of FIG. **8**A. The metal structures BM**91** and BM**92** are electrically connected to source S**81** of FIG. **8**A.

[0093] FIG. **9**B illustrates cross-section views of a semiconductor device **902** along the section lines C**9** and D**9** in FIG. **9**A, in accordance with some embodiments of the present disclosure. The semiconductor device **902** can correspond to the semiconductor device **901** of FIG. **9**A.

[0094] Along the section line C**9**, the metal layer structure MD**9** is formed on the conductive structures POD**91** and POD**92**. The metal layer structure MD**9** extends along the Y direction. The metal structure M**92** and the via structure VD**92** are formed on the metal layer structure MD**9**. The metal structure M**91** and the via structure VD**91** are formed on the metal layer structure MD**9**. The metal structures M**91** and M**92** are formed on the front side of the wafer. Along the section line D**9**, the conductive structure POD**92** and the via structure VB**92** are formed on the metal structure BM**92**. The conductive structure POD**91** and the via structure VB**91** are formed on the metal structure BM**91**. The metal structures BM**91** and BM**91** are formed on the back side of the wafer.

[0095] FIG. **10**A is a schematic diagram of a design layout of a semiconductor device **1001**, in accordance with some embodiments of the present disclosure. The semiconductor device **1001** can correspond to the semiconductor device **801** of FIG. **8**A.

[0096] The semiconductor device **1001** includes two metal structures BM**101** and BM**102** extending along the X direction. The semiconductor device **1001** includes two conductive structures POD**101** and POD**102** that extend along the X direction and include P-type active regions. The semiconductor device **1001** includes a metal structure M**10** extending along the Y direction. The semiconductor device **1001** includes a metal layer structure MD**10** extending along the Y direction. The metal structure M**10** belongs to virtual power domain. The metal structures BM**101** and BM**102** belong to a true power domain. The metal structure M**10** is electrically connected to drain D**81** of FIG. **8**A. The metal structures BM**101** and BM**102** are electrically connected to source S**81** of FIG. **8**A.

[0097] FIG. **10**B illustrates cross-section views of a semiconductor device **1002** along the section lines C**10** and D**10** in FIG. **10**A, in accordance with some embodiments of the present disclosure. The semiconductor device **1002** can correspond to the semiconductor device **1001** of FIG. **10**A.

[0098] Along the section line C**10**, the via structures VD**101** and VD**102** are formed between the metal structure M**101** and the metal layer structure MD**10**. The metal layer structure MD**10** is

formed on the conductive structures POD**101** and POD**102**. The metal structure M**101**, the via structures VD**101** and VD**102** and the metal layer structure MD**10** can be formed on the front side of the wafer. Along the section line D**10**, the conductive structure POD**102** and the via structure VB**102** are formed on the metal structure BM**102**. The conductive structure POD**101** and the via structure VB**101** are formed on the metal structure BM**101**. The metal structures BM**101** and BM**102** are formed on the back side of the wafer.

[0099] FIG. **11**A is a schematic diagram of a design layout of a semiconductor device **1101**, in accordance with some embodiments of the present disclosure. The semiconductor device **1101** can correspond to the semiconductor device **801** of FIG. **8**A. The semiconductor device **1101** includes two conductive structures POD**111** and POD**112** that extend along the X direction and include P-type active regions. The semiconductor device **1001** includes a metal structure BM**112** extending along the Y direction.

[0100] FIG. **11**B illustrates cross-section views of a semiconductor device **1102** along the section lines C**11** and D**11** in FIG. **11**A, in accordance with some embodiments of the present disclosure. The semiconductor device **1102** can correspond to the semiconductor device **1101** of FIG. **11**A.

[0101] Along the section line C**11**, the conductive structures POD**111** and POD**112**, and the via structures VB**111** and VB**112** are formed on the metal structure BM**111**. Along the section line D**11**, the conductive structures POD**111** and POD**112**, and the via structures VB**113** and VB**114** are formed on the metal structure BM**112**. The metal structures BM**111** and BM**112** are formed on the back side of the wafer. The metal structure BM**111** is electrically connected to the source S**81** of FIG. **8**A. The metal structure BM**112** is electrically connected to the drain D**81** of FIG. **8**A.

[0102] FIG. **12**A is a schematic diagram of a design layout of a semiconductor device **1201**, in accordance with some embodiments of the present disclosure. The semiconductor device **1201** can correspond to the semiconductor device **801** of FIG. **8**A. The semiconductor device **1201** includes two conductive structures POD**121** and POD**122** that extend along the X direction and include P-type active regions. The semiconductor device **1201** includes two metal structures M**121** and M**122** extending along the X direction. The semiconductor device **1001** includes a metal structure BM**12** extending along the Y direction.

[0103] FIG. **12**B illustrates cross-section views of a semiconductor device **1202** along the section lines C**12** and D**12** in FIG. **12**A, in accordance with some embodiments of the present disclosure. The semiconductor device **1202** can correspond to the semiconductor device **1201** of FIG. **12**A.

[0104] Along the section line C**12**, the metal layer structure MD**12** is formed on the conductive structures POD**121** and POD**122**. The metal layer structure MD**12** extends along the Y direction. The metal structure M**122** and the via structure VD**122** are formed on the metal layer structure MD**12**. The metal structure M**121** and the via structure VD**121** are formed on the metal layer structure MD**12**. The metal structures M**121** and M**122** are formed on the front side of the wafer. Along the section line D**12**, the conductive structure POD**122** and the via structure VB**122** are formed on the metal structure BM**12**. The conductive structure POD**121** and the via structure VB**121** are formed on the metal structure BM**12**. The metal structure BM**12** is formed on the back side of the wafer. The metal structures M**121** and M**122** are formed on the front side of the wafer. The metal structure BM**12** is electrically connected to the source S**81** of FIG. **8**A. The metal structures M**121** and M**122** are electrically connected to the drain D**81** of FIG. **8**A.

[0105] FIG. **13**A is a schematic diagram of a design layout of a semiconductor device **1301**, in accordance with some embodiments of the present disclosure. The semiconductor device **1301** can correspond to the semiconductor device **801** of FIG. **8**A. The semiconductor device **1301** includes two conductive structures POD**131** and POD**132** that extend along the X direction and include P-type active regions. The semiconductor device **1301** includes a metal structure BM**13** extending along the Y direction. The semiconductor device **1301** includes a metal structure M**13** extending along the Y direction. The semiconductor device **1301** includes a metal layer structure MD**13** extending along the Y direction.

[0106] FIG. **13**B illustrates cross-section views of a semiconductor device **1302** along the section lines C**13** and D**13** in FIG. **13**A, in accordance with some embodiments of the present disclosure. The semiconductor device **1302** can correspond to the semiconductor device **1301** of FIG. **13**A.
[0107] Along the section line C**13**, the via structures VD**131** and VD**132** are formed between the metal layer structure M**13** and the metal layer structure MD**13**. The metal layer structure MD**13** are formed on the conductive structures POD**131** and POD**132**. The metal layer structure M**131**, the via structures VD**131** and VD**132** and the metal layer structure MD**13** can be formed on the front side of the wafer. Along the section line D**13**, the conductive structure POD**132** and the via structure VB**132** are formed on the metal structure BM**13**. The conductive structure POD**131** and the via structure VB**131** are formed on the metal structure BM**13**. The metal structure BM**13** is formed on the back side of the wafer.
[0108] Some embodiments of the present disclosure provide a semiconductor device formed on a wafer having a front side and a back side. The semiconductor device includes a first back metal structure, a second back metal structure, a first conductive structure and a metal layer structure. The first back metal structure is formed on the back side of the wafer and extends in a first direction. The second back metal structure is formed on the back side of the wafer and extends in the first direction. The second back metal structure is spaced apart from the first back metal structure along a second direction vertical to the first direction. The first conductive structure is formed on the front side of the wafer, which extends in the first direction and is formed above the second back metal structure. The metal layer structure extends in the second direction and is formed above the first conductive structure. The first back metal structure belongs to a first power domain and the second back metal structure belongs to a second power domain different from the first power domain.
[0109] Some embodiments of the present disclosure provide a semiconductor device formed on a wafer. The semiconductor device includes a first back metal structure, a first conductive structure, a metal layer structure and a second metal structure. The first back metal structure belongs to a first power domain, and the first back metal structure is formed on a back side of the wafer. The first conductive structure extends in a first direction and is formed above the first back metal structure, and the first conductive structure is P-type. The metal layer structure extends in a second direction vertical to the first direction and is formed above the first conductive structure. The second metal structure belongs to a second power domain different from the first power domain.
[0110] Some embodiments of the present disclosure provide a method for manufacturing a semiconductor device. The method includes forming a first back metal structure, extending in a first direction and belonging to a first power domain; forming a second back metal structure, extending in the first direction and belonging to a second power domain different from the first power domain, wherein the second back metal structure is spaced apart from the first back metal structure along a second direction vertical to the first direction; forming a first conductive structure, extending in the first direction and formed above the second back metal structure; and forming a metal layer structure, extending in the second direction and formed above the first back metal structure and the first conductive structure, wherein the first back metal structure and the second back metal structure are formed on a back side of the wafer.
[0111] The foregoing outlines structures of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

Claims

1. A semiconductor device formed on a wafer having a front side and a back side, comprising: a first back metal structure formed on the back side of the wafer and extending in a first direction; a second back metal structure formed on the back side of the wafer and extending in the first direction, wherein the second back metal structure is spaced apart from the first back metal structure along a second direction vertical to the first direction; a first conductive structure formed on the front side of the wafer, extending in the first direction and formed above the second back metal structure; and a metal layer structure, extending in the second direction and formed above the first conductive structure, wherein the first back metal structure belongs to a first power domain and the second back metal structure belongs to a second power domain different from the first power domain.
2. The semiconductor device of claim 1, further comprising: a second conductive structure formed on the front side of the wafer and extending in the first direction, wherein the second conductive structure is formed between the first back metal structure and the metal layer structure; and a first via structure, formed between the first back metal structure and the second conductive structure.
3. The semiconductor device of claim 2, wherein the first conductive structure is P-type, and the second conductive structure is N-type.
4. The semiconductor device of claim 3, further comprising: a first front metal structure, extending in the first direction and belonging to the second power domain, wherein the first front metal structure is formed above the metal layer structure and the first conductive structure, and the first front metal structure is formed on the front side of the wafer.
5. The semiconductor device of claim 1, further comprising: a through via structure, extending in the first direction, wherein the through via structure is formed above the first back metal structure.
6. The semiconductor device of claim 5, further comprising: a second front metal structure, extending in the first direction and belonging to the second power domain, wherein the second front metal structure is formed above the metal layer structure and the first conductive structure, and the second front metal structure is formed on a front side of the wafer.
7. The semiconductor device of claim 6, further comprising: a third conductive structure, extending in the first direction and formed between the second back metal structure and the metal layer structure, wherein the third conductive structure is P-type.
8. The semiconductor device of claim 1, wherein the first power domain is configured to transmit power from a power supply to a switch cell, the second power domain is configured to transmit power from the switch cell to a standard cell, and the second power domain can be cut off by the switch cell.
9. A semiconductor device formed on a wafer, comprising: a first back metal structure, belonging to a first power domain, and the first back metal structure is formed on a back side of the wafer; a first conductive structure, extending in a first direction and formed above the first back metal structure, wherein the first conductive structure is P-type; a metal layer structure, extending in a second direction vertical to the first direction and formed above the first conductive structure; and a second metal structure, belonging to a second power domain different from the first power domain.
10. The semiconductor device of claim 9, wherein the second metal structure comprises a second back metal structure formed on the back side of the wafer, and the first conductive structure is formed above the second back metal structure.
11. The semiconductor device of claim 10, wherein the first back metal structure and the second back metal structure extend in the first direction.
12. The semiconductor device of claim 10, wherein the first back metal structure and the second back metal structure extend in a second direction perpendicular to the first direction.
13. The semiconductor device of claim 9, wherein the second metal structure comprises a second

front metal structure formed on a front side of the wafer, and the second front metal structure is formed above the metal layer structure.

14. The semiconductor device of claim 13, wherein the first back metal structure and the second front metal structure extend in the first direction.

15. The semiconductor device of claim 13, wherein the first back metal structure extends in the first direction, and the second front metal structure extends in the second direction.

16. The semiconductor device of claim 13, wherein the first back metal structure extends in the second direction, and the second front metal structure extends in the first direction.

17. The semiconductor device of claim 13, wherein the first back metal structure and the second front metal structure extend in the second direction.

18. A method for manufacturing a semiconductor device on a wafer, comprising: forming a first back metal structure, extending in a first direction and belonging to a first power domain; forming a second back metal structure, extending in the first direction and belonging to a second power domain different from the first power domain, wherein the second back metal structure is spaced apart from the first back metal structure along a second direction vertical to the first direction; forming a first conductive structure, extending in the first direction and formed above the second back metal structure; and forming a metal layer structure, extending in the second direction and formed above the first back metal structure and the first conductive structure, wherein the first back metal structure and the second back metal structure are formed on a back side of the wafer.

19. The method of claim 18, further comprising: forming a second conductive structure, extending in the first direction, wherein the second conductive structure is formed between the first back metal structure and the metal layer structure; and forming a first via structure, formed between the first back metal structure and the second conductive structure.

20. The method of claim 18, further comprising: forming a through via structure, extending in the first direction, wherein the through via structure is formed above the first back metal structure.