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Zhao; Yucai et al.

Power supply with dual inputs

Inventors: Zhao; Yucai (Shanghai, CN), Fan; Bing (Shanghai, CN), Dong; Kai (Shanghai,

CN), Che; Liangsong (Shanghai, CN), Huang; Junlai (Shanghai, CN)

Applicant: Delta Electronics (Shanghai) Co., Ltd. (Shanghai, CN)

Assignee: Delta Electronics (Shanghai) Co., Ltd. (Shanghai, CN)

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Description

- (1) FIG. **1** is a perspective view of a first embodiment of a power supply with dual inputs showing our new design;
- (2) FIG. **2** is another perspective view of the power supply with dual inputs of FIG. **1**;
- (3) FIG. **3** is a front view of the power supply with dual inputs of FIG. **1**;
- (4) FIG. **4** is a rear view of the power supply with dual inputs of FIG. **1**;
- (5) FIG. **5** is a left view of the power supply with dual inputs of FIG. **1**;
- (6) FIG. **6** is a right view of the power supply with dual inputs of FIG. **1**;
- (7) FIG. **7** is a top view of the power supply with dual inputs of FIG. **1**;
- (8) FIG. **8** is a bottom view of the power supply with dual inputs of FIG. **1**;
- (9) FIG. **9** is an enlarged view of Part C of FIG. **1**;
- (10) FIG. 10 is an enlarged view of Part D of FIG. 2;
- (11) FIG. **11** is a perspective view of a second embodiment of a power supply with dual inputs showing our new design;
- (12) FIG. **12** is another perspective view of the power supply with dual inputs of FIG. **11**;
- (13) FIG. **13** is a left view of the power supply with dual inputs of FIG. **11**;
- (14) FIG. **14** is a perspective view of a third embodiment of a power supply with dual inputs showing our new design;
- (15) FIG. **15** is another perspective view of the power supply with dual inputs of FIG. **14**;
- (16) FIG. **16** is a left view of the power supply with dual inputs of FIG. **14**;
- (17) FIG. **17** is a perspective view of a fourth embodiment of a power supply with dual inputs showing our new design;
- (18) FIG. 18 is another perspective view of the power supply with dual inputs of FIG. 17; and,
- (19) FIG. **19** is a left view of the power supply with dual inputs of FIG. **17**.
- (20) The broken lines shown in FIG. **6** contain lightly shaded areas that depict the portions of the power supply with dual inputs that form no part of the claimed design.
- (21) The dash-dot broken lines that encase portions of FIGS. **1** and **2** and that border the FIGS. **9** and **10** indicate the boundary of the enlarged areas of the figures and form no part of the claimed design.

Claims

The ornamental design for a power supply with dual inputs as shown and described.