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(54) **EMBEDDED FERROELECTRIC MEMORY CELL**

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(60) Provisional application No. 62/724,289, filed on Aug. 29, 2018.

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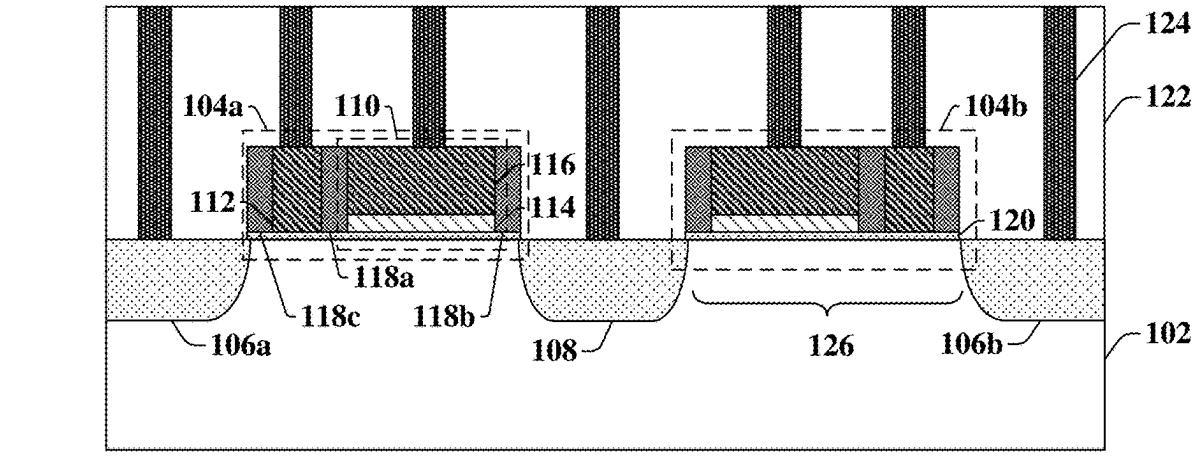
H10D 64/68	(2025.01)

(52) **U.S. Cl.**

CPC ***G11C 11/2259*** (2013.01); ***G11C 11/223*** (2013.01); ***G11C 11/2255*** (2013.01); ***G11C 11/2257*** (2013.01); ***H10B 51/30*** (2023.02); ***H10B 51/40*** (2023.02); ***H10D 64/689*** (2025.01)

(57) **ABSTRACT**

The present disclosure relates to an integrated chip structure. The integrated chip structure includes a first select gate and a second select gate disposed over a substrate. A first ferroelectric random access memory (FeRAM) stack and a second FeRAM stack disposed over the substrate and laterally between the first select gate and the second select gate. An inter-level dielectric disposed over the substrate and laterally surrounding the first select gate, the second select gate, the first FeRAM stack, and the second FeRAM stack. A conductive contact extends through the inter-level dielectric. The first select gate and the second select gate are substantially symmetrically disposed along opposing sides of the conductive contact and the first FeRAM stack and the second FeRAM stack are substantially symmetrically disposed along opposing sides of the conductive contact.



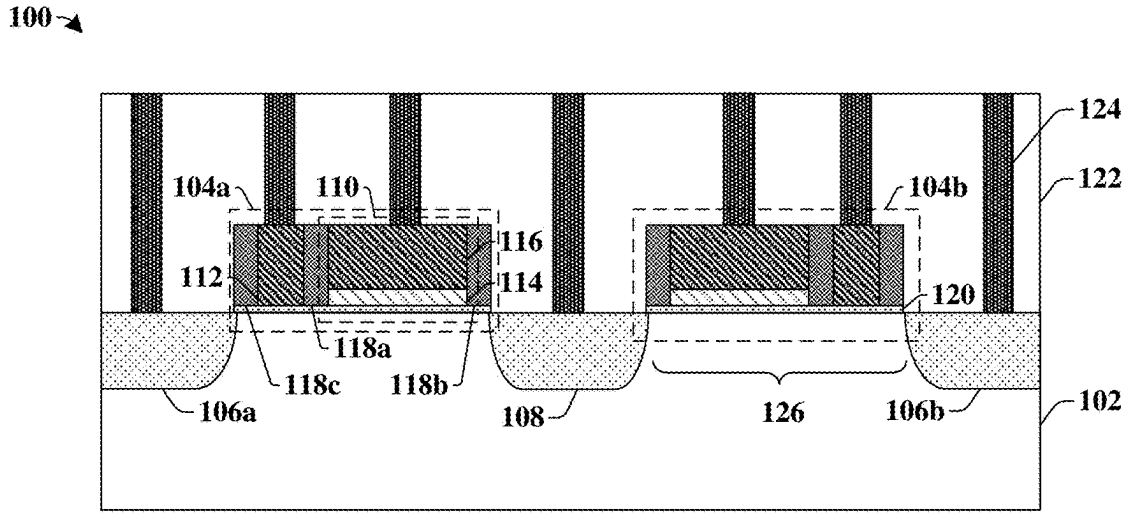

100
124
122
104a
110
104b
116
112
114
120
118a
118c
118b
106a
108
126
106b
102

Fig. 1

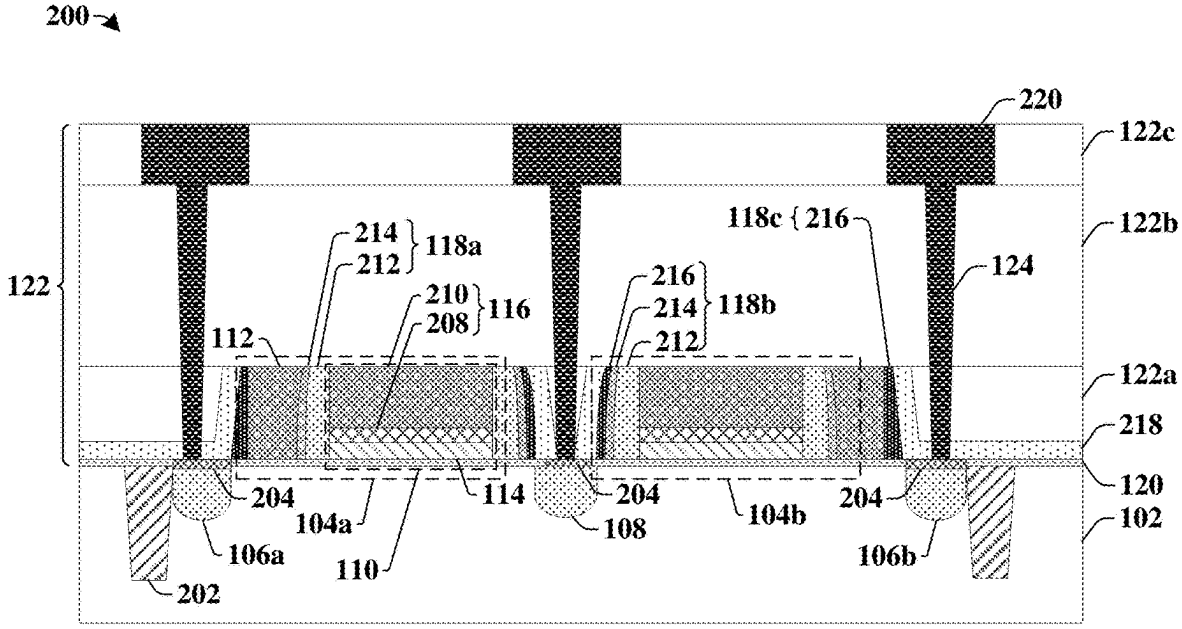

200
220
122c
122
214
212
118a
118c
216
122b
210
208
116
216
214
118b
212
124
112
122a
218
120
204
114
204
204
104a
104b
106a
108
106b
110
102
202

Fig. 2A

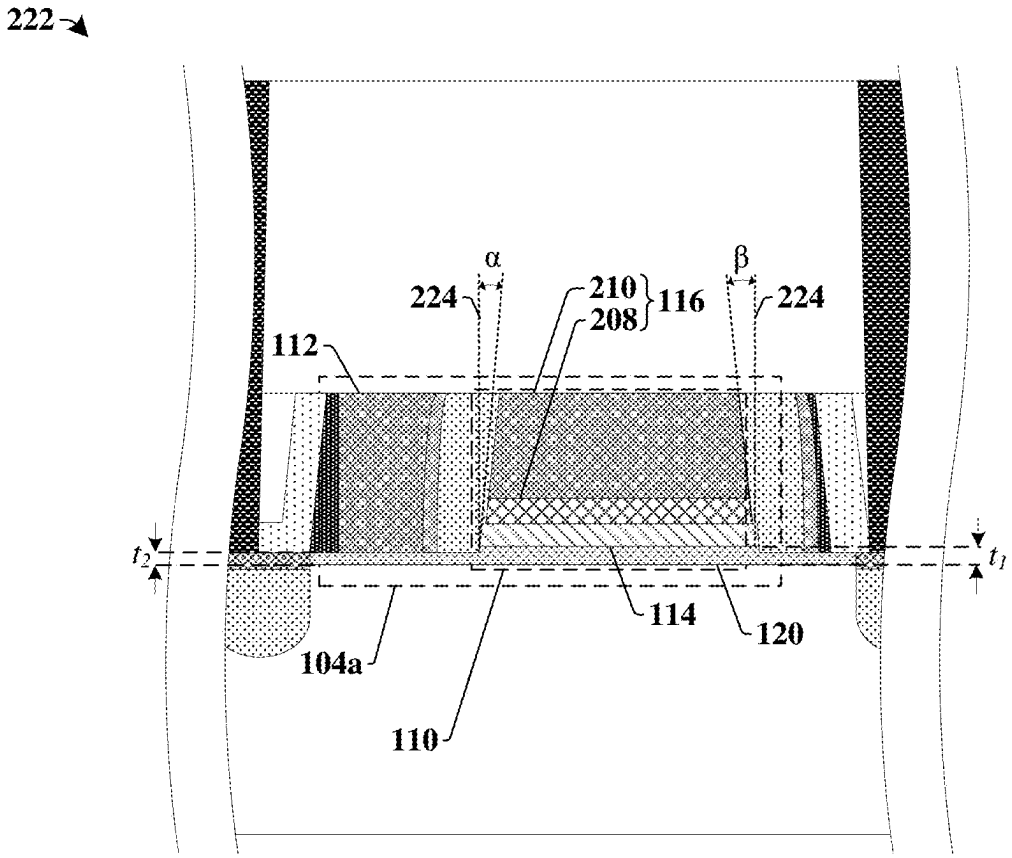
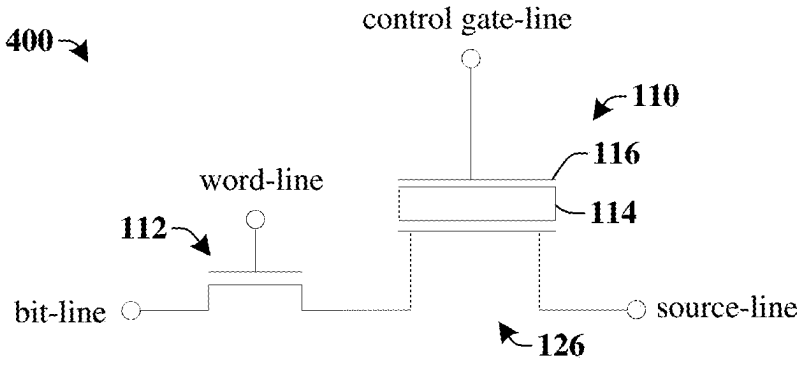

222
α
β
224
210
208
116
224
112
t_2
t_1
114
120
104a
110

Fig. 2B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control gate-line
110
116
word-line
114
112
bit-line
source-line
126

Fig. 4A

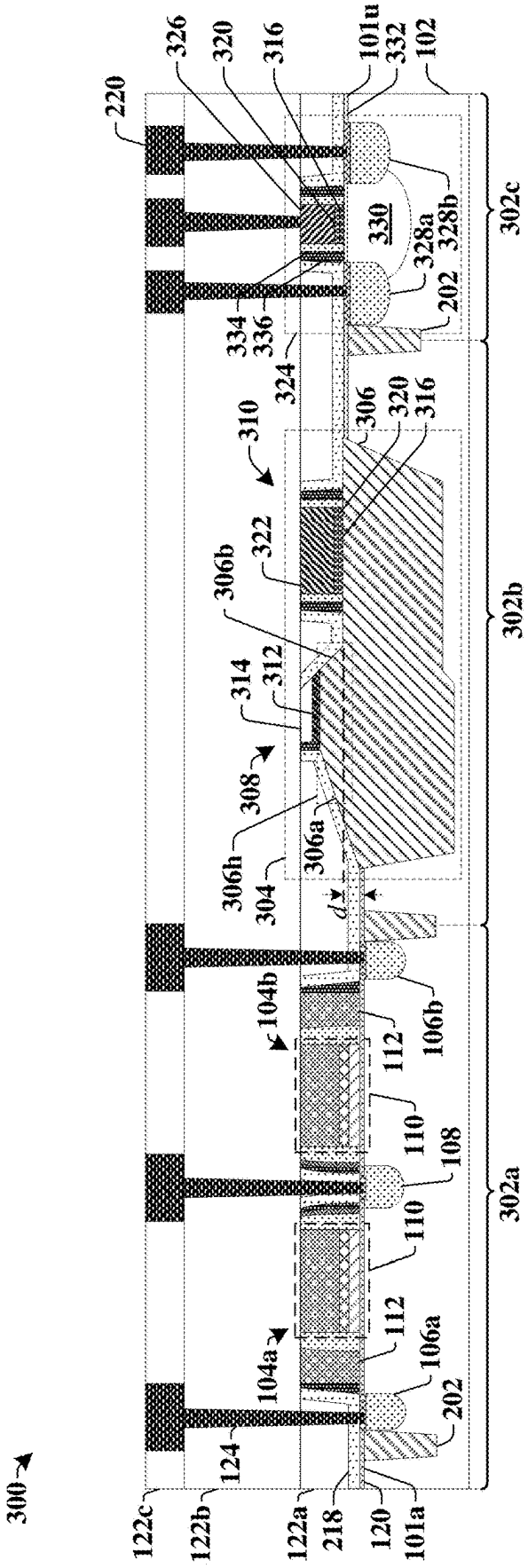

300
122c
122b
122a
218
120
101a
124
104a
104b
112
110
108
106a
106b
202
220
326
320
316
101u
332
102
330
328a
328b
334
336
324
310
306
322
306b
314
312
308
306a
306h
304
d
302a
302b
302c

Fig. 3

402

	WL(SG)	SL	BL	CGL
Program	0-1 V	0 V	0 V	V_{prog}
Erase	0 V	V_{prog}	V_{prog}	0 V
Read	0.5-1.8V	0.5-V_{dd}	0 V	0-V_{dd}

404 406 408

Fig. 4B

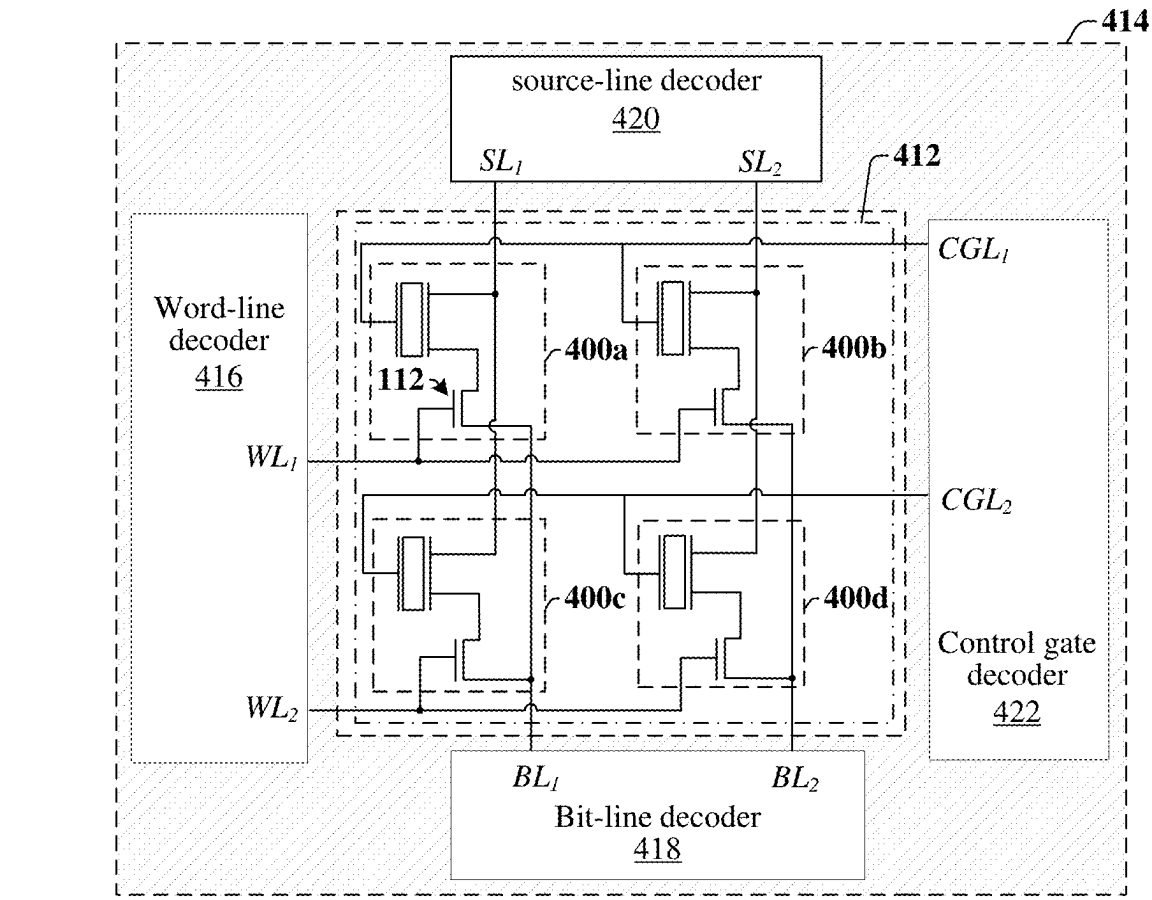


Fig. 4C

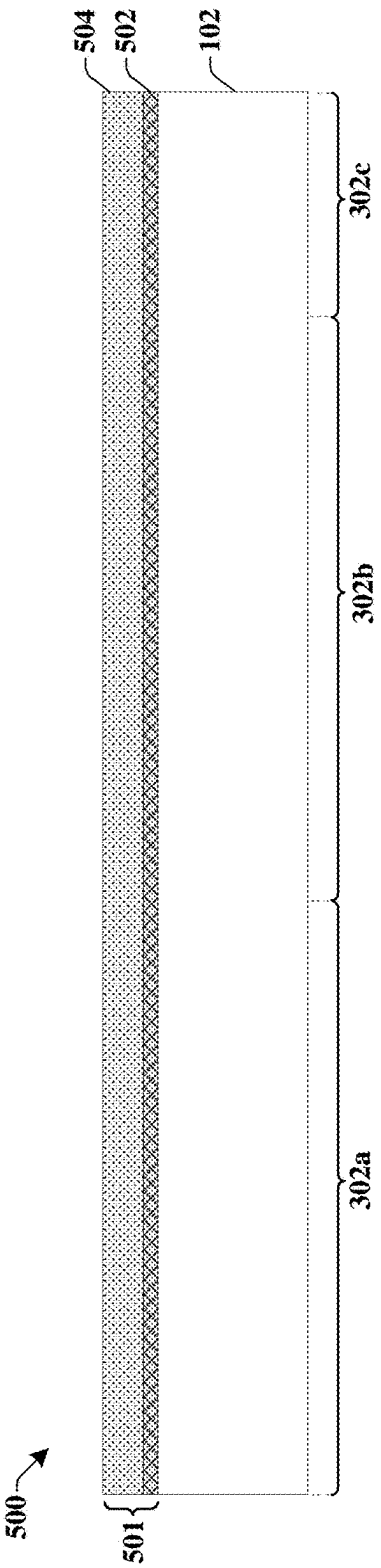

500
501
504
502
102
302a
302b
302c

Fig. 5

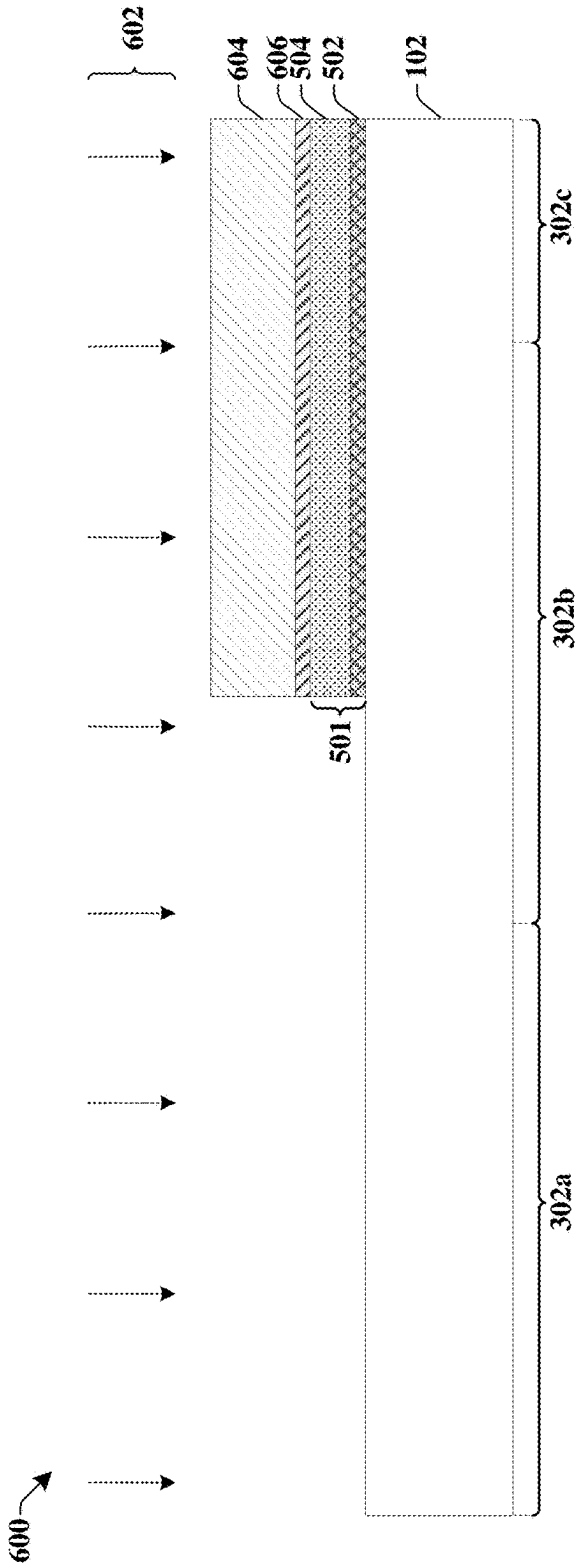

600
602
604
606
504
502
102
501
302a
302b
302c

Fig. 6

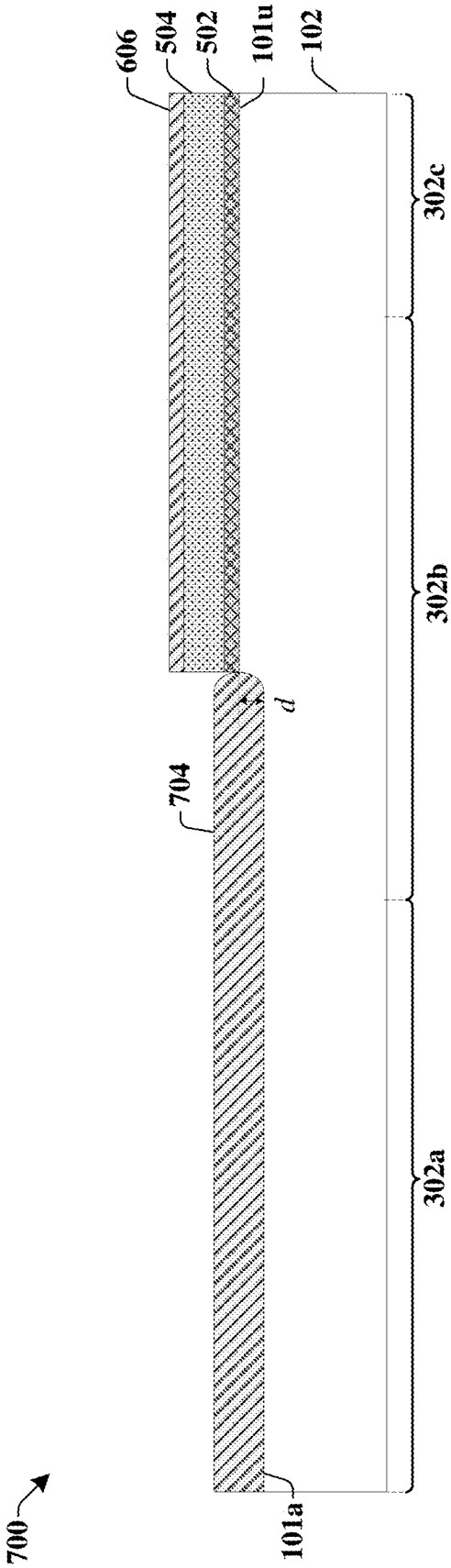

606
504
502
101u
102
302c
302b
704
d
302a
700
101a

Fig. 7

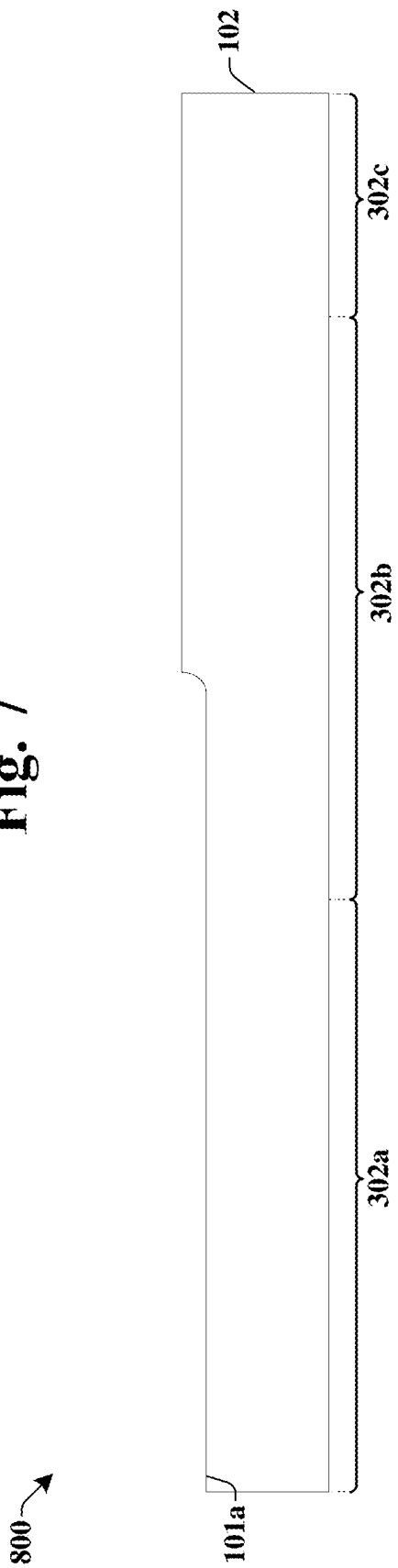

102
302c
302b
302a
800
101a

Fig. 8

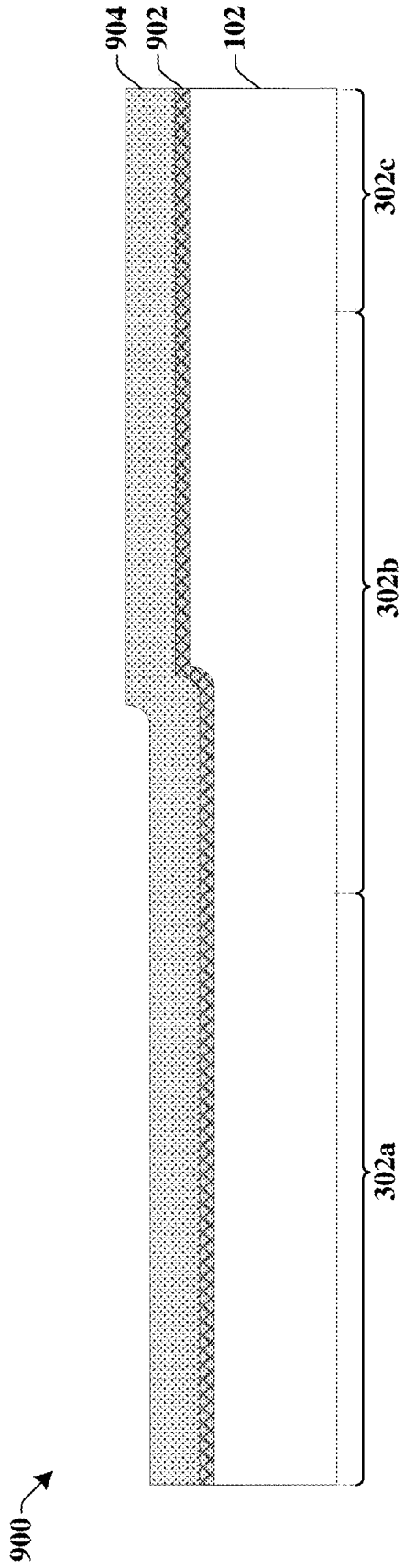

900
904
902
102
302c
302b
302a

Fig. 9

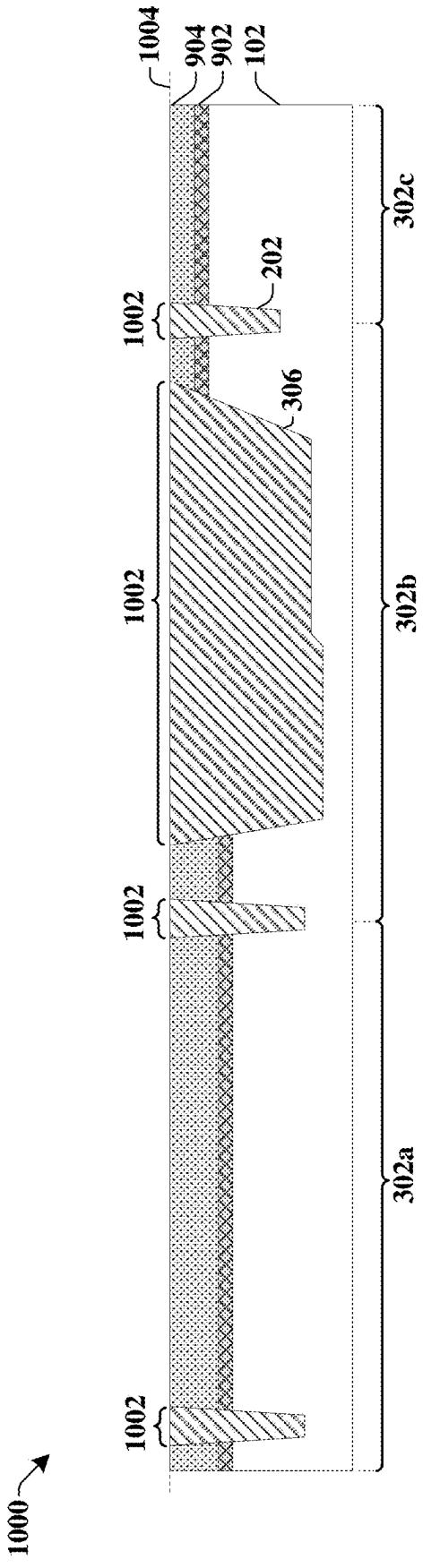

1000
1004
904
902
102
202
306
1002
1002
1002
302c
302b
302a

Fig. 10

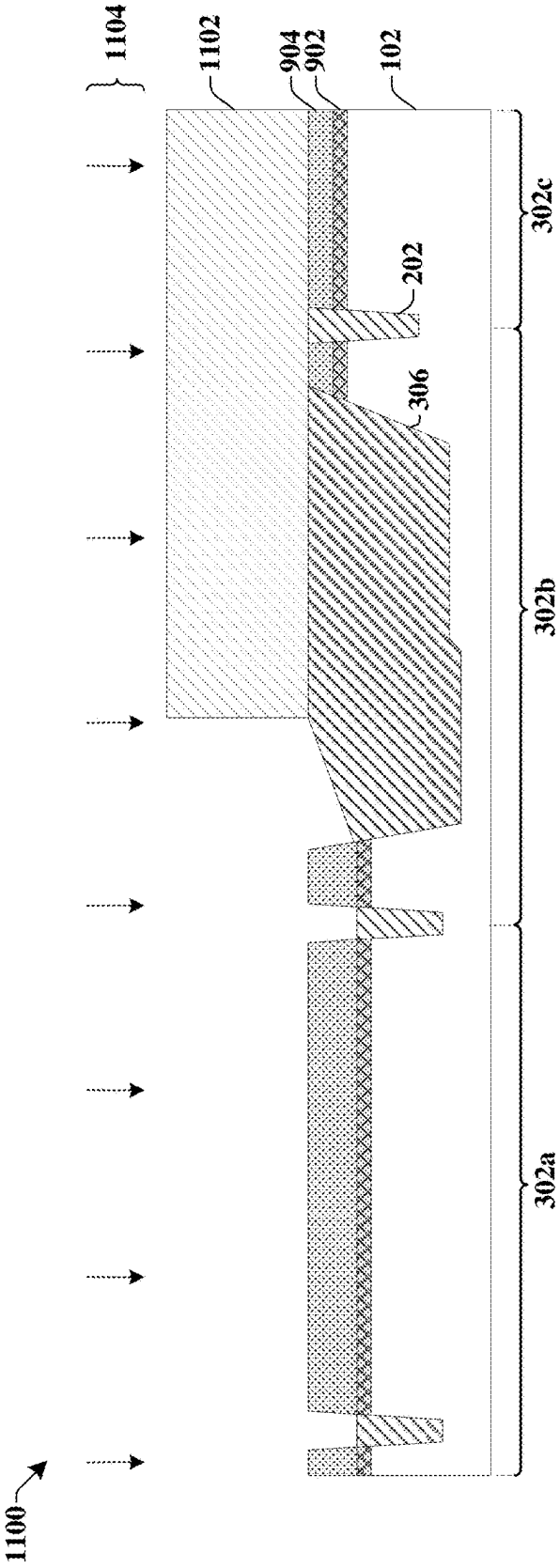

1104
1102
904
902
102
202
306
302c
302b
302a
1100

Fig. 11

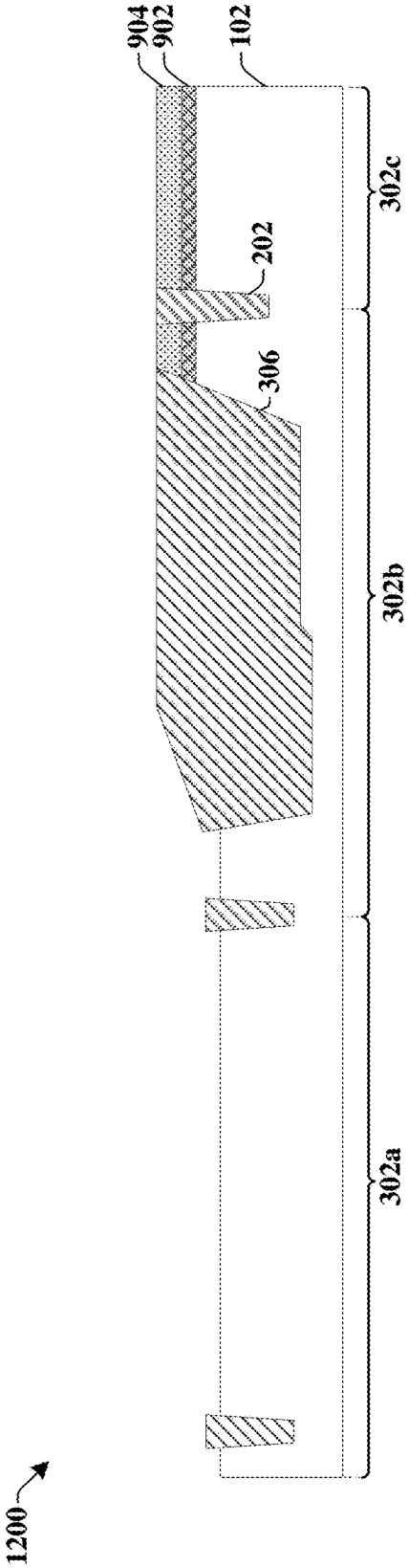

904
902
102
202
306
302c
302b
302a
1200

Fig. 12

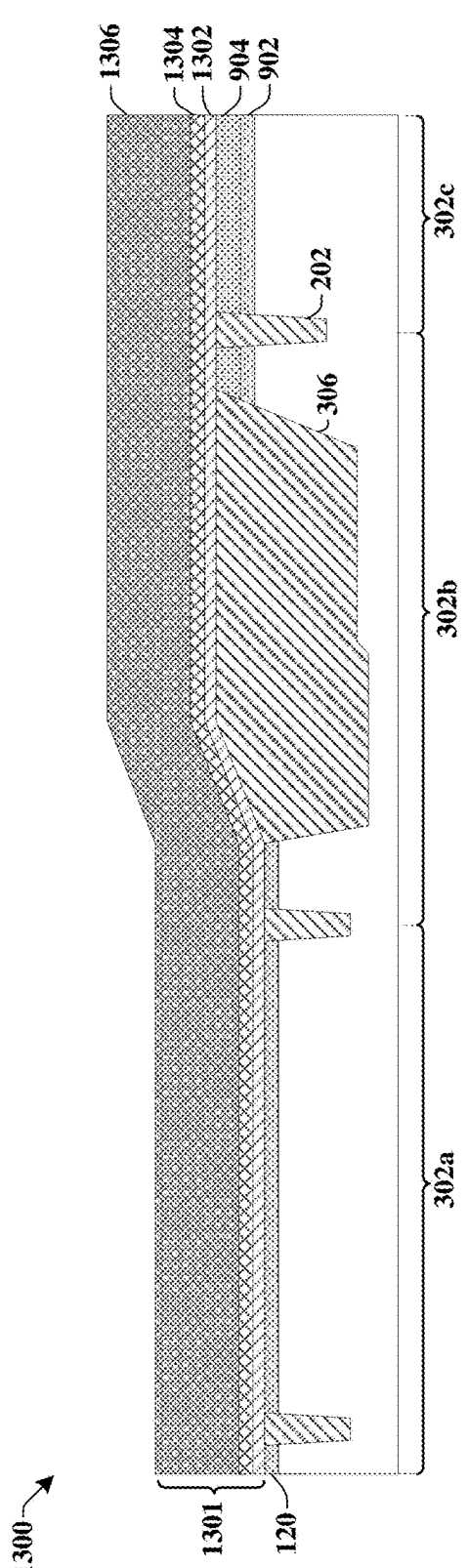
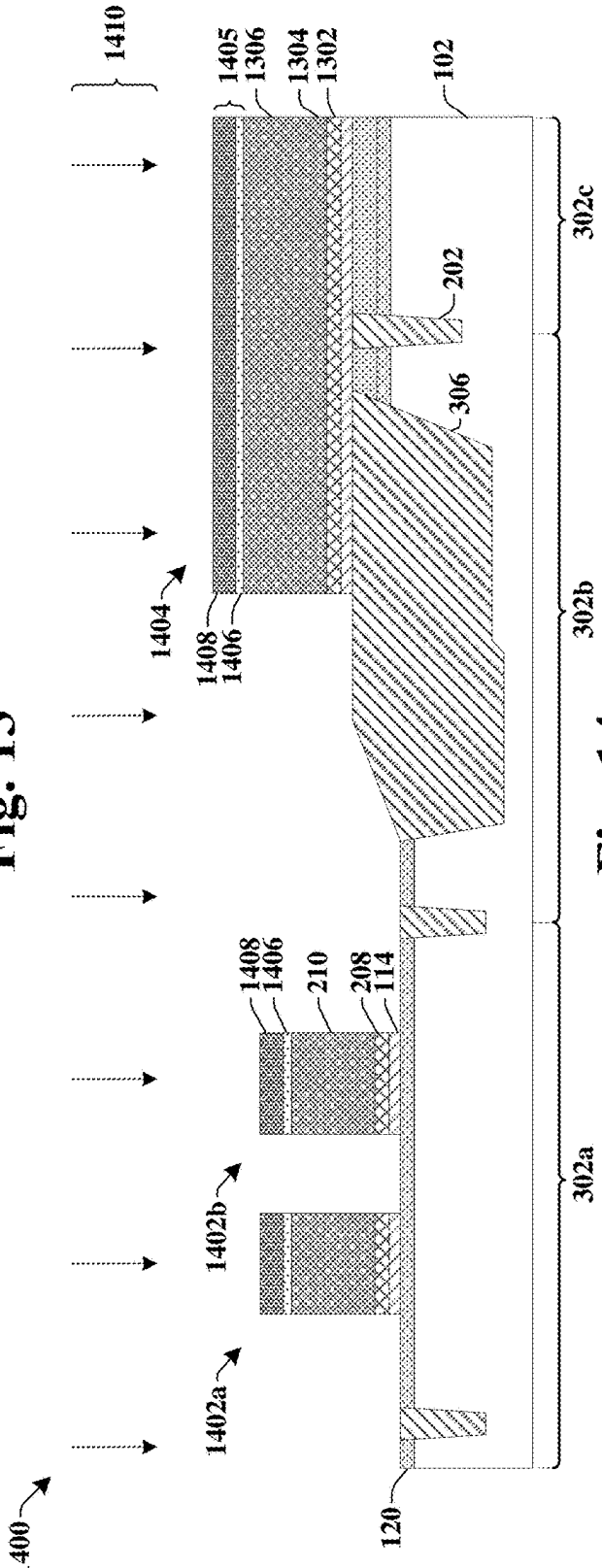

1306
1304
1302
904
902
202
306
302c
302b
302a
1300
1301
120

Fig. 13


1410
1405
1306
1304
1302
102
202
306
302c
302b
1404
1408
1406
1408
1406
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208
114
1402b
1402a
302a
1400
120

Fig. 14

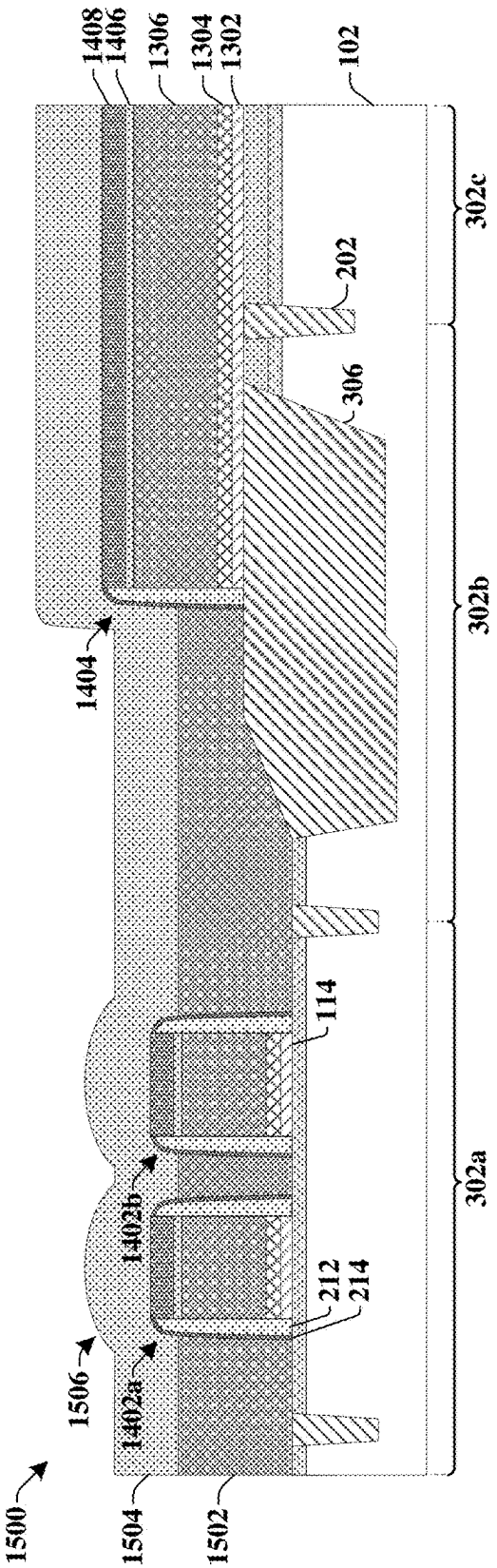

1500
1504
1502
1506
1402a
1402b
1404
1408
1406
1306
1304
1302
102
202
306
114
212
214
302a
302b
302c

Fig. 15

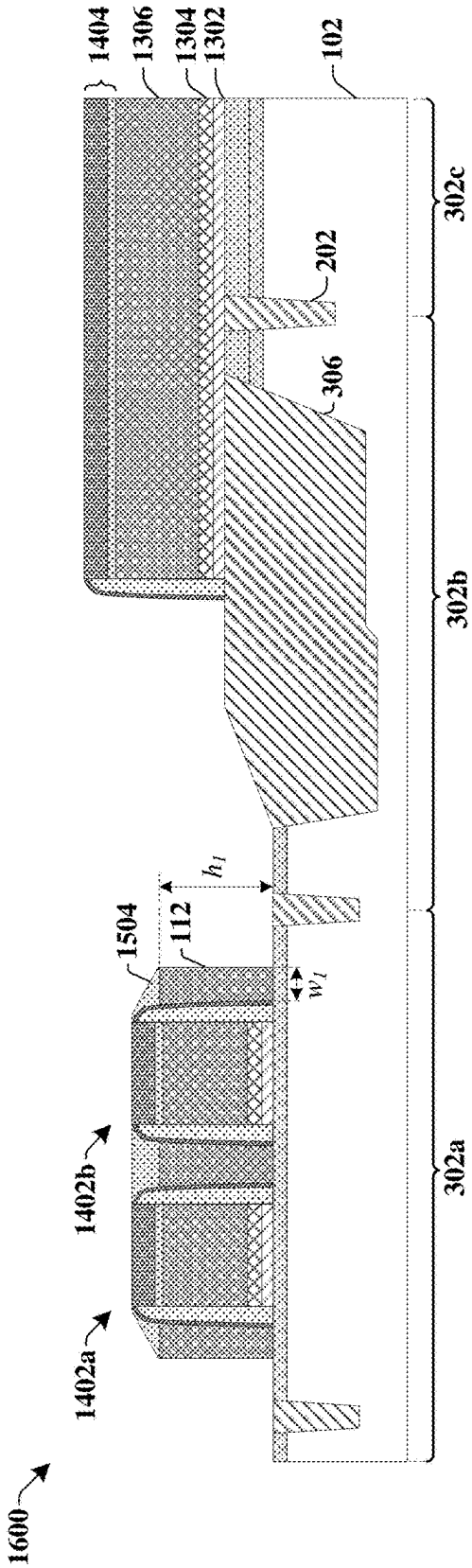

1600
1402a
1402b
1504
112
h_1
w_1
1404
1306
1304
1302
102
202
306
302a
302b
302c

Fig. 16

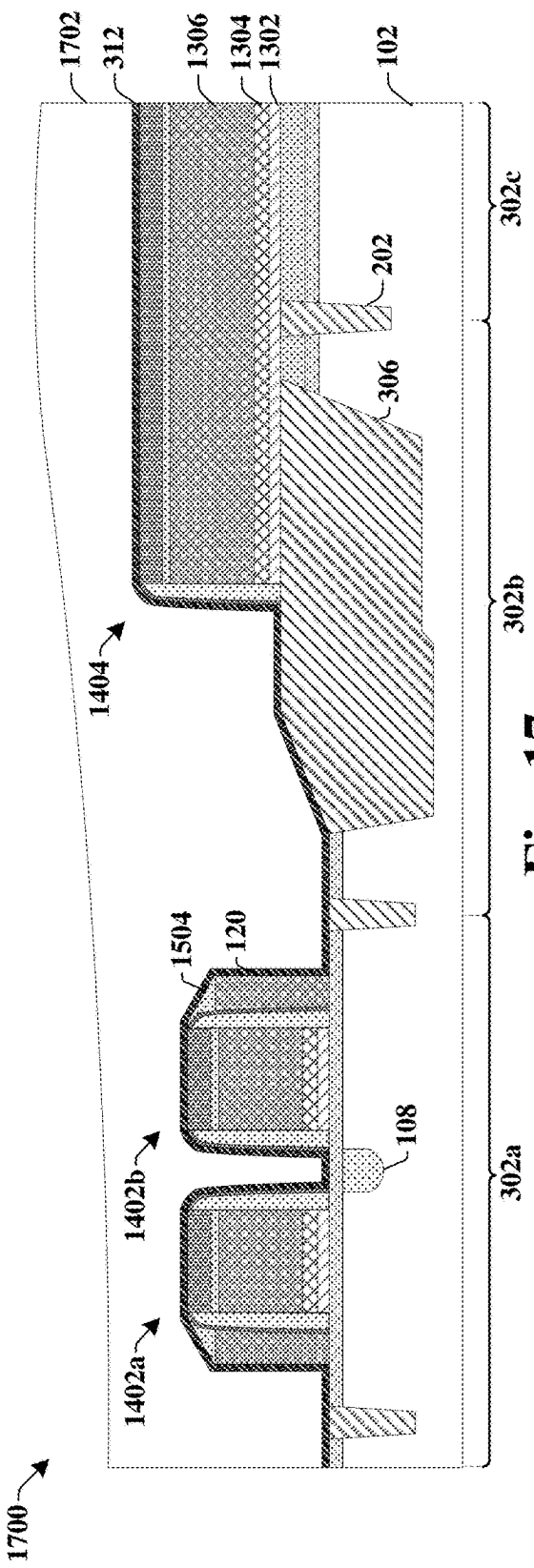

1700
1702
312
1306
1304
1302
102
202
306
1404
1504
120
1402b
108
1402a
302a
302b
302c

Fig. 17

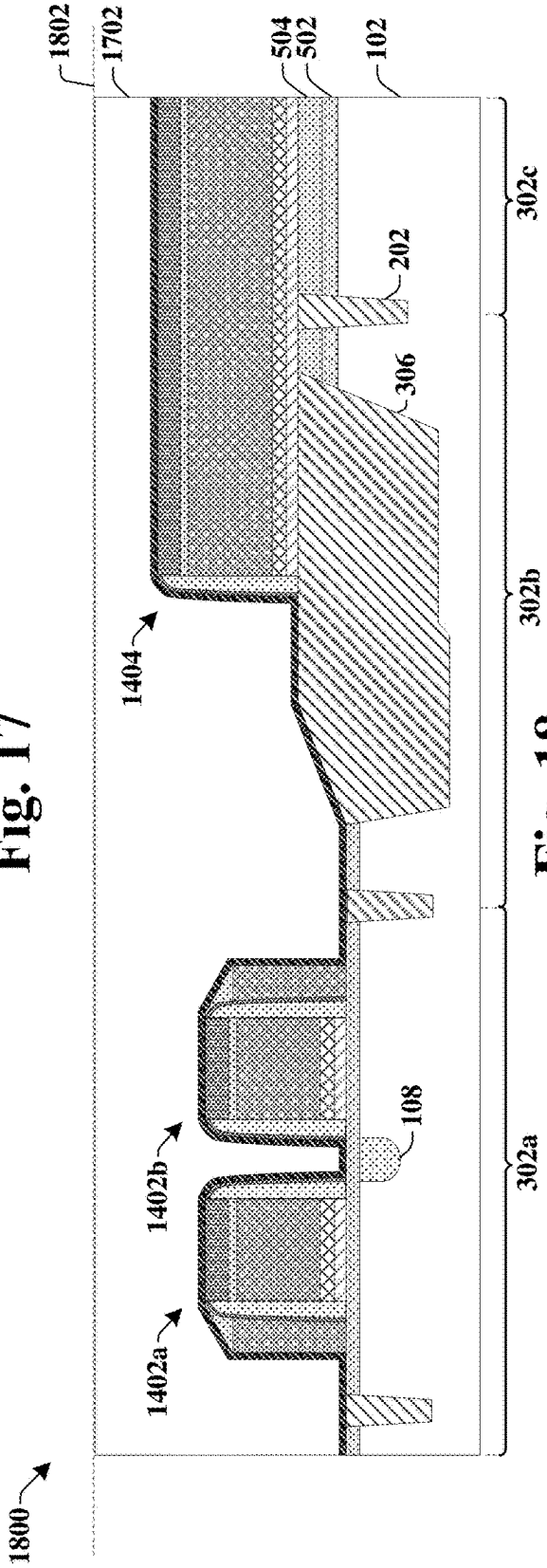

1800
1802
1702
504
502
102
202
306
1404
1402b
108
1402a
302a
302b
302c

Fig. 18

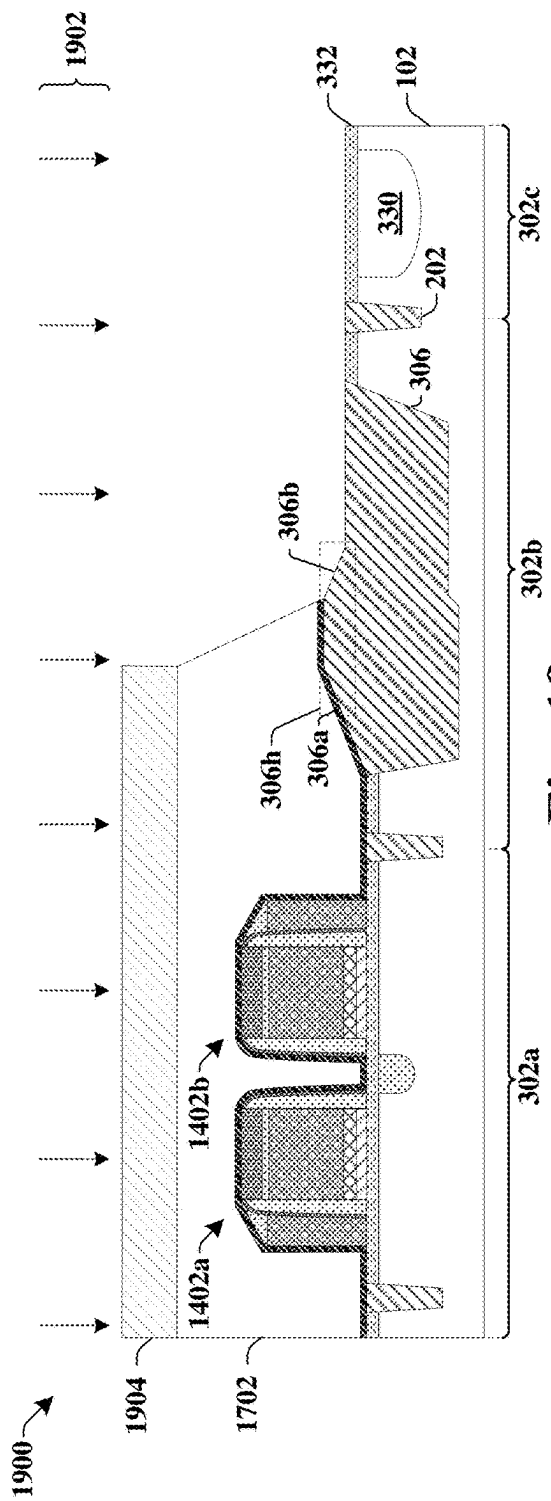

1900
1902
1904
1702
1402a
1402b
306h
306a
306b
306
202
330
332
102
302a
302b
302c

Fig. 19

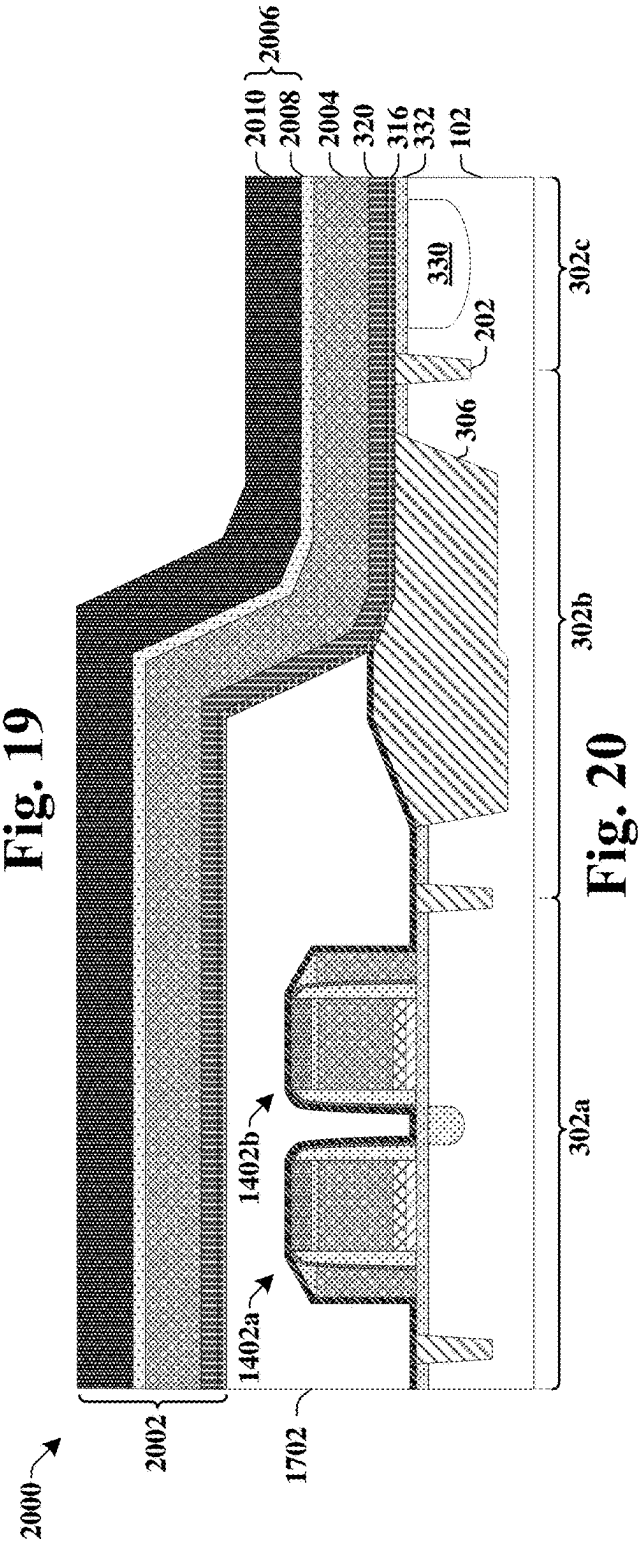

2000
2002
2006
2010
2008
2004
320
316
332
102
1702
1402a
1402b
306
202
330
302a
302b
302c

Fig. 20

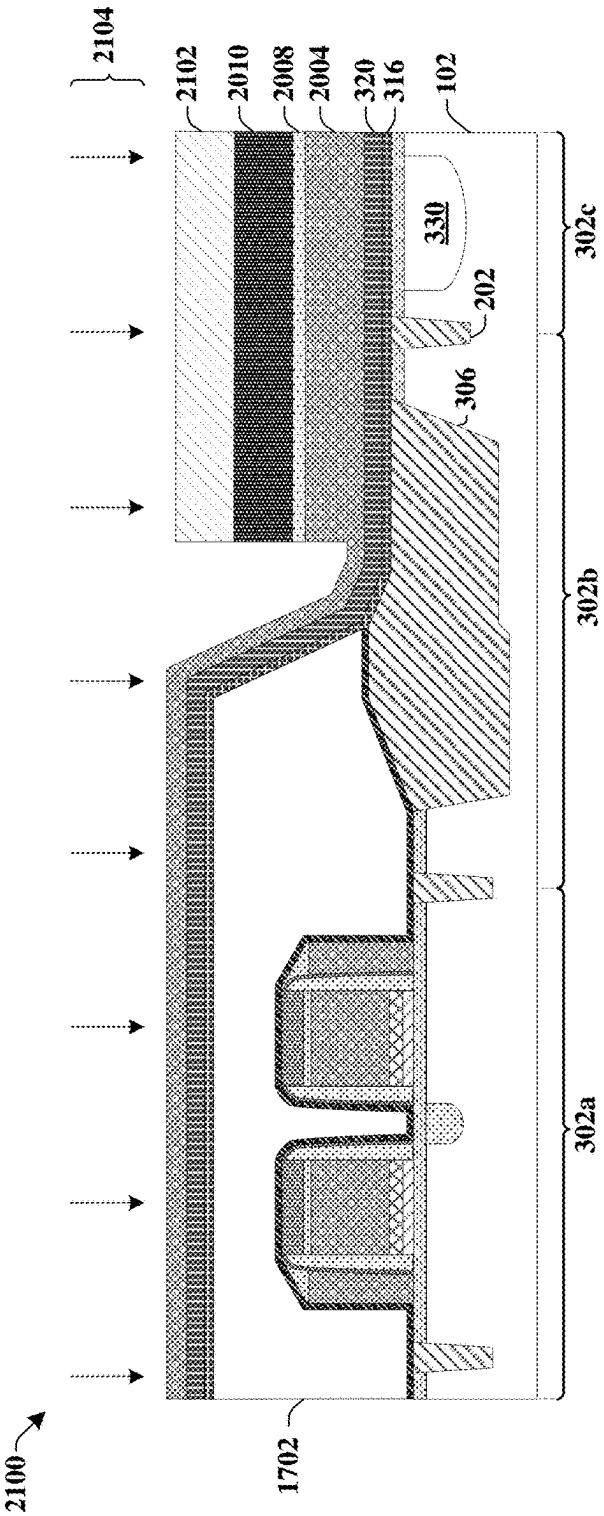
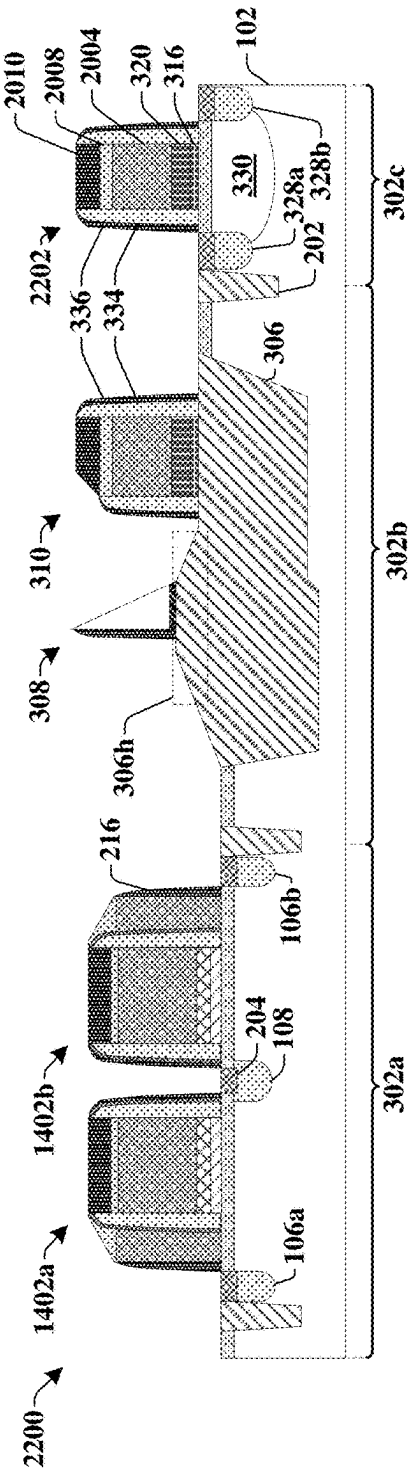

2100
1702
2104
2102
2010
2008
2004
320
316
102
330
202
306
302c
302b
302a

Fig. 21


2200
1402a
1402b
2010
2008
2004
320
316
102
330
328a
328b
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334
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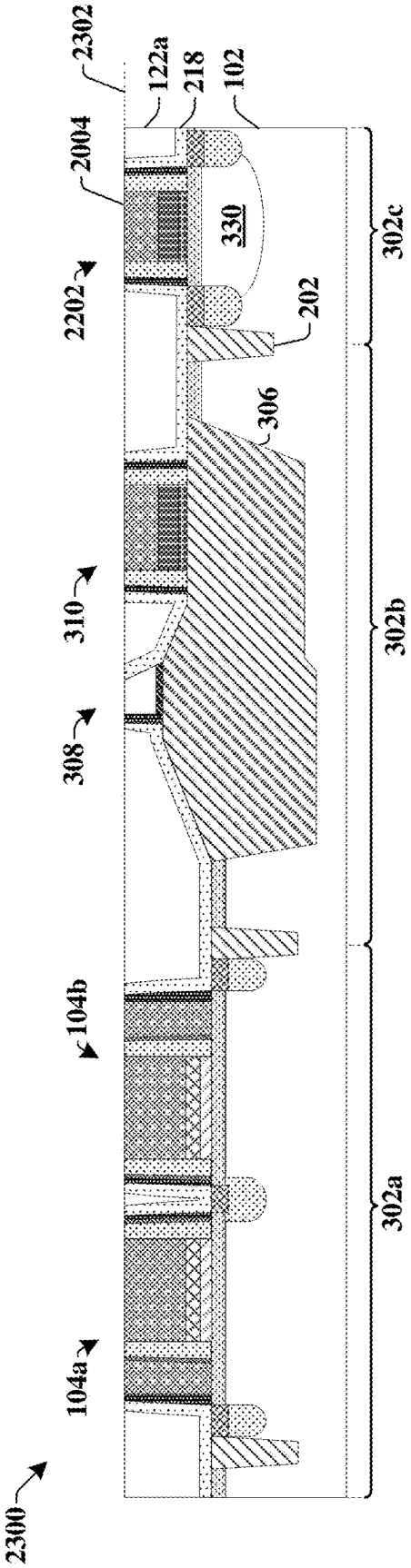
310
308
306h
216
106b
204
108
106a
302c
302b
302a

Fig. 22


2300
104a
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2202
2004
2302
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330
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302a
302b
302c

Fig. 23

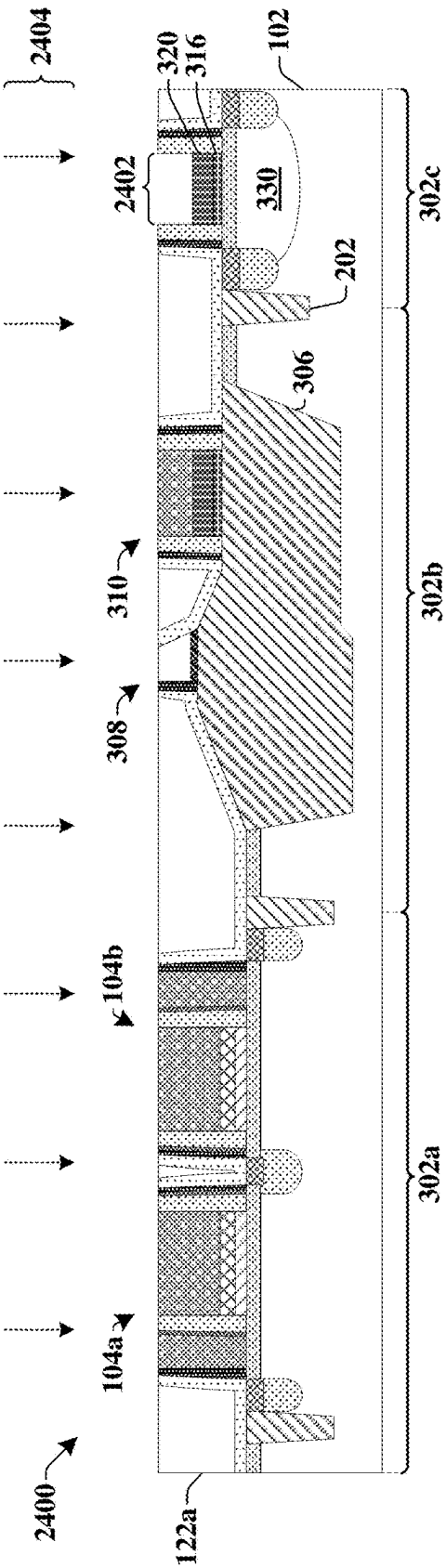
2400
104a
104b
308
310
2402
2404
320
316
102
330
202
306
122a
302a
302b
302c

Fig. 24

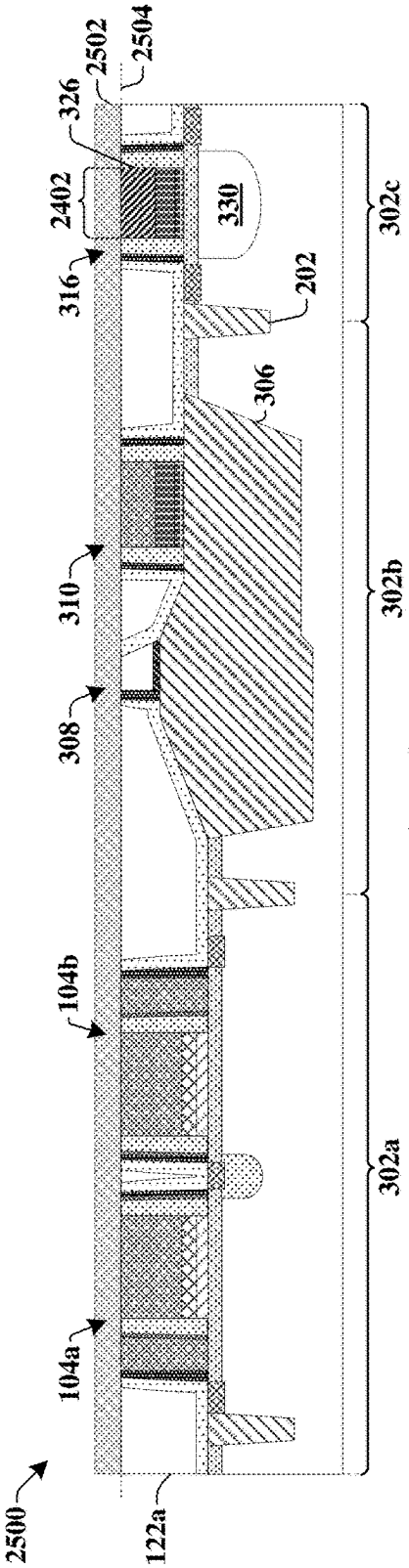
2500
122a
104a
104b
308
310
316
2402
326
2502
2504
330
202
306
302a
302b
302c

Fig. 25

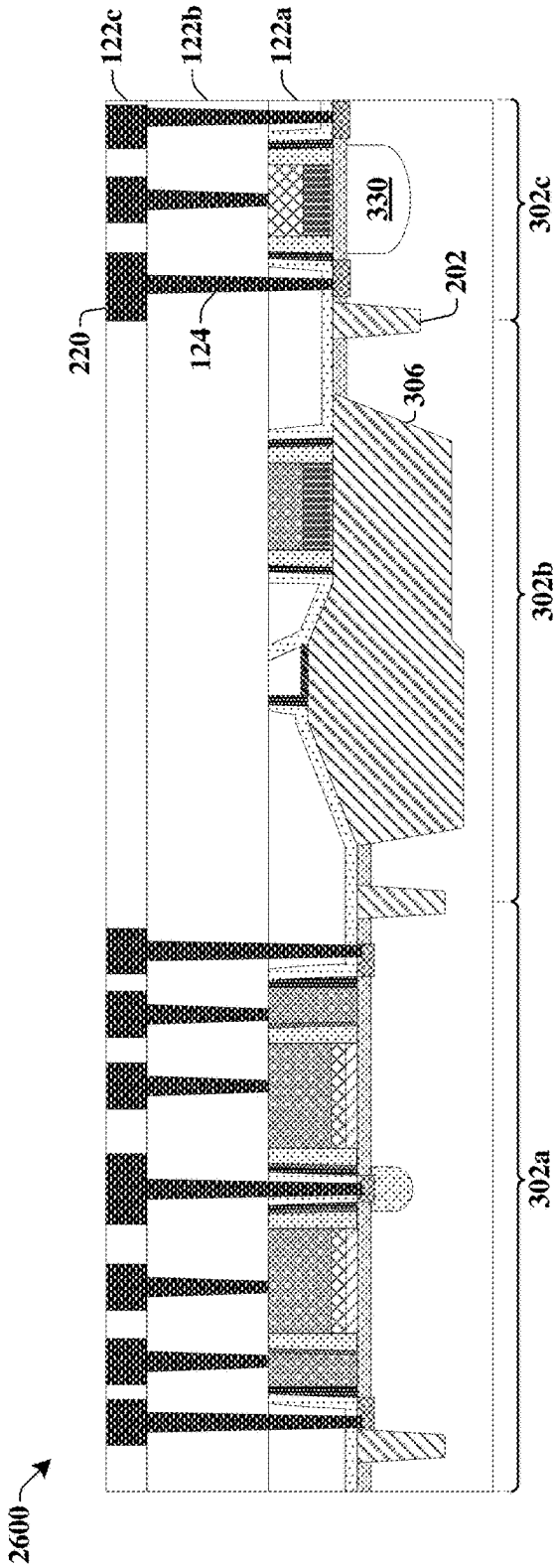
2600
220
124
122c
122b
122a
330
202
306
302a
302b
302c

Fig. 26

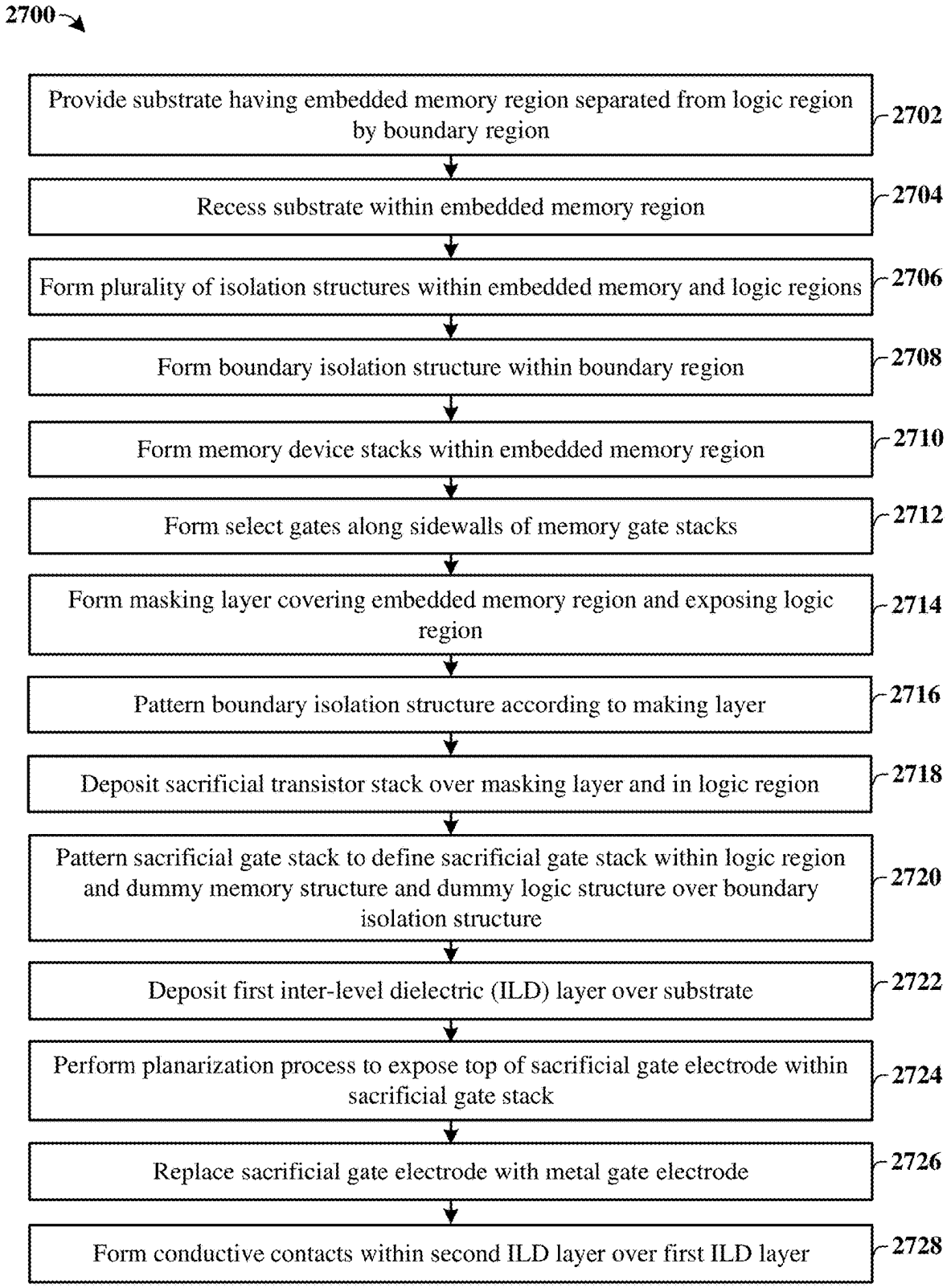
2700
Provide substrate having embedded memory region separated from logic region by boundary region
2702
Recess substrate within embedded memory region
2704
Form plurality of isolation structures within embedded memory and logic regions
2706
Form boundary isolation structure within boundary region
2708
Form memory device stacks within embedded memory region
2710
Form select gates along sidewalls of memory gate stacks
2712
Form masking layer covering embedded memory region and exposing logic region
2714
Pattern boundary isolation structure according to making layer
2716
Deposit sacrificial transistor stack over masking layer and in logic region
2718
Pattern sacrificial gate stack to define sacrificial gate stack within logic region and dummy memory structure and dummy logic structure over boundary isolation structure
2720
Deposit first inter-level dielectric (ILD) layer over substrate
2722
Perform planarization process to expose top of sacrificial gate electrode within sacrificial gate stack
2724
Replace sacrificial gate electrode with metal gate electrode
2726
Form conductive contacts within second ILD layer over first ILD layer
2728

Fig. 27

EMBEDDED FERROELECTRIC MEMORY CELL

REFERENCE TO RELATED APPLICATIONS

[0001] This Application is a Continuation of U.S. application Ser. No. 18/506,177, filed on Nov. 10, 2023, which is a Continuation of U.S. application Ser. No. 17/866,946, filed on Jul. 18, 2022 (now U.S. Pat. No. 11,869,564, issued on Jan. 9, 2024), which is a Continuation of U.S. application Ser. No. 17/177,627, filed on Feb. 17, 2021 (now U.S. Pat. No. 11,437,084, issued on Sep. 6, 2022), which is a Divisional of U.S. application Ser. No. 16/267,668, filed on Feb. 5, 2019 (now U.S. Pat. No. 10,930,333, issued on Feb. 23, 2021), which claims the benefit of U.S. Provisional Application No. 62/724,289, filed on Aug. 29, 2018. The contents of the above-referenced Patent Applications are hereby incorporated by reference in their entirety.

BACKGROUND

[0002] Many modern day electronic devices contain electronic memory configured to store data. Electronic memory may be volatile memory or non-volatile memory. Volatile memory stores data while it is powered, while non-volatile memory is able to store data when power is removed. Ferroelectric random-access memory (FeRAM) devices are one promising candidate for a next generation non-volatile memory technology. This is because FeRAM devices provide for many advantages, including a fast write time, high endurance, low power consumption, and low susceptibility to damage from radiation.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0004] FIG. **1** illustrates a cross-sectional view of some embodiments of a memory structure having a ferroelectric random-access memory (FeRAM) cell.

[0005] FIG. **2**A illustrates a cross-sectional view of some additional embodiments of a memory structure having an FeRAM cell.

[0006] FIG. **2**B illustrates a cross-sectional view of some alternative embodiments of an FeRAM cell.

[0007] FIG. **3** illustrates a cross-sectional view of some embodiments of an integrated chip having an embedded FeRAM cell.

[0008] FIG. **4**A illustrates a schematic diagram of some embodiments of the disclosed FeRAM cell.

[0009] FIG. **4**B illustrates a graph showing some embodiments of exemplary operating conditions of the disclosed FeRAM cell.

[0010] FIG. **4**C illustrates a schematic diagram of some embodiments of a memory structure having a plurality of FeRAM cells.

[0011] FIGS. **5-26** illustrate cross-sectional views of some embodiments of a method of forming an integrated chip having an embedded FeRAM cell.

[0012] FIG. **27** illustrates a flow diagram of some embodiments of a method of forming an integrated chip having an embedded FeRAM cell.

DETAILED DESCRIPTION

[0013] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0014] Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated **90** degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0015] Embedded memory has become common in modern day integrated chips. Embedded memory is electronic memory devices that are located on a same integrated chip die as logic devices (e.g., a processor or ASIC). By embedding memory devices and logic devices on a same integrated chip die, the conductive interconnects between the memory devices and the logic devices can be shortened, thereby reducing power and/or increasing performance of an integrated chip.

[0016] FeRAM (ferroelectric random access memory) devices are a promising candidate for embedded memory applications. FeRAM devices may be integrated in an FeRAM array as plurality of IT (one transistor) cells. The plurality of IT cells respectively comprise a channel region laterally disposed between a source region and a drain region. A ferroelectric material is vertically arranged between the channel region and an overlying conductive electrode. The ferroelectric material is able to store a data state (e.g., corresponding to a logic '0' or '1') depending upon charges accumulated within the channel region and/or a bias voltage applied to the conductive electrode.

[0017] However, it has been appreciated that unwanted currents may flow in channel regions of unselected IT FeRAM cells. The unwanted currents can increase a power consumption of an FeRAM array and/or negatively impact read operations of the FeRAM array. It has been further appreciated that the unwanted currents in channel regions of unselected IT FeRAM cells may have a larger impact on the power consumption and/or read operations of an FeRAM array as a size of the IT FeRAM cells decreases.

[0018] The present disclosure, in some embodiments, relates to an integrated chip having an embedded FeRAM cell. The embedded FeRAM cell comprises a source region and a drain region disposed within a substrate. A select gate is disposed over the substrate between the source region and the drain region, and an FeRAM device is disposed over the substrate between the select gate and the source region. The FeRAM device comprises a ferroelectric layer arranged between the substrate and a conductive electrode. The select gate and/or the conductive electrode are configured to selectively provide access (e.g., read and/or write data) to the FeRAM device. By using a select gate to selectively provide access to the FeRAM device, the memory cell effectively operates as a 1.5 transistor FERAM cell (e.g., an FE RAM cell that is configured to switch provide access to the FeRAM device based upon gate voltages received at more than one conductive electrode), causing a relatively low current to be achieved in channel regions of unselected FeRAM cells and thereby improving the power consumption and/or read operations of an FeRAM array.

[0019] FIG. **1** illustrates a cross-sectional view of some embodiments of a memory structure **100** comprising a ferroelectric random-access memory (FeRAM) cell.

[0020] The memory structure **100** comprises a plurality of FeRAM cells **104***a*-**104***b* configured to respectively store a data state (e.g., a logic '0' or '1'). The plurality of FeRAM cells **104***a*-**104***b* are arranged over a substrate **102** between drain regions **106***a*-**106***b* and a common source region **108** within the substrate **102**. For example, in some embodiments the plurality of FeRAM cells **104***a*-**104***b* comprise a first FeRAM cell **104***a* arranged between a first drain region **106***a* and the common source region **108** and a second FeRAM cell **104***b* arranged between a second drain region **106***b* and the common source region **108**.

[0021] The plurality of FeRAM cells **104***a*-**104***b* respectively comprise an FeRAM device **110** and a select gate **112**. The FeRAM device **110** has a ferroelectric material **114** arranged between the substrate **102** and an overlying conductive electrode **116**. The select gate **112** is arranged along a first side of the FeRAM device **110**, between the FeRAM device **110** and a closest one of the drain regions **106***a*-**106***b*.

[0022] In some embodiments, a first side of the select gate **112** is laterally separated from the first side of the FeRAM device **110** by way of a first sidewall spacer **118***a*. In some embodiments, a second sidewall spacer **118***b* is arranged along a second side of the FeRAM device **110** and a third sidewall spacer **118***c* is arranged along a second side of the select gate **112**. In some embodiments, the first sidewall spacer **118***a*, the second sidewall spacer **118***b*, and the third sidewall spacer **118***c* comprise one or more of the same materials. In some embodiments, the first sidewall spacer **118***a*, the second sidewall spacer **118***b*, and the third sidewall spacer **118***c* comprise one or more different materials.

[0023] In some embodiments, the ferroelectric material **114** and the select gate **112** are separated from the substrate **102** by way of an interfacial dielectric layer **120**. In some embodiments, the interfacial dielectric layer **120** continuously extends from directly below the ferroelectric material **114** to directly below the select gate **112**. An inter-level dielectric (ILD) structure **122** is arranged over the substrate **102** and laterally surrounds the plurality of FeRAM cells **104***a*-**104***b*. Conductive contacts **124** extend through the ILD structure **122** to contact the drain regions **106***a*-**106***b*, the common source region **108**, the conductive electrode **116**, and the select gate **112**.

[0024] During operation, one or more bias voltages can be applied to the conductive electrode **116** and the select gate **112**. The one or more bias voltages cause charge carriers (e.g., electrons and/or holes) to accumulate within a channel region **126** between the drain regions **106***a*-**106***b* and the common source region **108**. The bias voltages and/or charge carriers generate electric fields, which extend through the ferroelectric material **114**. The electric fields are configured to change positions of electric dipoles within the ferroelectric material **114** depending on the applied bias voltages and/or charge carriers. If the magnetic polarization of the ferroelectric material **114** has a first polarization, the FeRAM device **110** will digitally store data as a first bit value (e.g., a logical "0"). Alternatively, if the magnetic polarization of the ferroelectric material **114** has a second polarization, the FeRAM device **110** will digitally store data as a second bit value (e.g., a logical "1").

[0025] Typically, FeRAM cells may experience a small leakage current within channel regions of unselected FeRAM cells. However, the select gate **112** is configured to reduce the channel current for unselected FeRAM cells, thereby decreasing a power consumption of an FeRAM array. Furthermore, the relatively simple operation of the FeRAM device **110** enables the FeRAM device **110** to be formed by way of a relatively simple fabrication process compared to other commonly used embedded memory types (e.g., such as embedded flash memory, which may utilize an erase gate), thereby allowing the FeRAM device **110** to be formed at a low cost.

[0026] FIG. **2**A illustrates a cross-sectional view of some additional embodiments of a memory structure **200** comprising an FeRAM cell.

[0027] The memory structure **200** comprises a plurality of FeRAM cells **104***a*-**104***b* arranged over a substrate **102**. In some embodiments, isolation structures **202** may be arranged within the substrate **102** on opposing sides of the plurality of FeRAM cells **104***a*-**104***b*. The isolation structures **202** may comprise one or more dielectric materials arranged within trenches defined by interior surfaces of the substrate **102**. In some embodiments, the isolation structures **202** may comprise shallow trench isolation (STI) structures. In some such embodiments, the isolation structures **202** may comprise a same isolation structure continuously extending in a closed loop around a perimeter of the plurality of FeRAM cells **104***a*-**104***b*.

[0028] The plurality of FeRAM cells **104***a*-**104***b* respectively comprise an FeRAM device **110** and a select gate **112** arranged between drain regions **106***a*-**106***b* and a common source region **108**. In some embodiments, the select gate **112** may comprise a conductive material, such as doped polysilicon, a metal, or the like. In some embodiments, the drain regions **106***a*-**106***b* and the common source region **108** may have a first doping type that is opposite a second doping type of the substrate **102**. In some embodiments, the common source region **108** continuously extends perpendicular to (e.g., into) the plane of the paper between two or more FeRAM cells (not shown) to form a source line. In some embodiments, a silicide layer **204** is arranged over the drain regions **106***a*-**106***b* and the common source region **108**. The silicide layer **204** may comprise nickel, cobalt, or the like.

[0029] In some embodiments, the drain regions **106***a*-**106***b* may have a different doping concentration and/or shape than the common source region **108**. For example, in some embodiments, the drain regions **106***a*-**106***b* may have a lower doping concentration than the common source region **108**. The lower doping concentration of the drain regions **106***a*-**106***b* mitigates gate induced drain leakage (GIDL) current in the FeRAM cells **104***a*-**104***b*.

[0030] The FeRAM device **110** comprises a ferroelectric material **114** and a conductive electrode **116** disposed over the ferroelectric material **114**. In some embodiments, the ferroelectric material **114** is separated from the substrate **102** by way of an interfacial dielectric layer **120**. In some embodiments, the interfacial dielectric layer **120** has a substantially flat surface between the first FeRAM cell **104***a* and the second FeRAM cell **104***b*. In some embodiments, the interfacial dielectric layer **120** may comprise an oxide, a nitride, a carbide, or the like. In some embodiments, the conductive electrode **116** may comprise etch stop layer **208** and a conductive material **210**. In various embodiments, the ferroelectric material **114** may comprise silicon doped hafnium oxide (Si-doped HfO_2), lead titanate, lead zirconate titanate (PZT), lead lanthanum zirconate titanate, strontium bismuth tantalate (SBT), bismuth lanthanum titanate (BLT), bismuth neodymium titanate (BNT), or the like. In some embodiments, etch stop layer **208** may comprise aluminum, ruthenium, palladium, hafnium, zirconium, titanium, or the like. In some embodiments, the conductive material **210** may comprise polysilicon, aluminum, copper, or the like. In some embodiments, the conductive material **210** may be a same material (e.g., polysilicon) as the select gate **112**.

[0031] A first sidewall spacer material **212** is arranged along opposing sides of the FeRAM device **110**. In some embodiments, the first sidewall spacer material **212** continuously extends to directly contact sidewalls of the conductive material **210**, etch stop layer **208**, and the ferroelectric material **114**. In some embodiments, the first sidewall spacer material **212** may continuously extends to directly contact and completely cover the sidewalls of the conductive material **210**, etch stop layer **208**, and the ferroelectric material **114**. A second sidewall spacer material **214** is separated from the opposing sides of the FeRAM device **110** by way of the first sidewall spacer material **212**. The second sidewall spacer material **214** also separates the first sidewall spacer material **212** from the select gate **112**. A third sidewall spacer material **216** is arranged along a side of the FeRAM device **110** facing away from a closest select gate **112** and along a side of the select gate **112** facing away from a closest FeRAM device **110**.

[0032] The first sidewall spacer material **212**, the second sidewall spacer material **214**, and the third sidewall spacer material **216** have substantially equal heights. In some embodiments, the first sidewall spacer material **212**, the second sidewall spacer material **214**, and the third sidewall spacer material **216** respectively extend from a first horizontal plane extending along a bottom of the ferroelectric material **114** to a second horizontal plane extending along a top of the conductive material **210**. In some embodiments, the first sidewall spacer material **212**, the second sidewall spacer material **214**, and the third sidewall spacer material **216** comprise different materials. For example, the first sidewall spacer material **212** may comprise a nitride (e.g., silicon nitride), the second sidewall spacer material **214** may comprise an oxide (e.g., silicon oxide), and the third sidewall spacer material **216** may comprise a carbide (e.g., silicon carbide).

[0033] A contact etch stop layer (CESL) **218** is arranged over the substrate **102** and along sidewalls of the third sidewall spacer material **216**. The CESL **218** laterally separates the third sidewall spacer material **216** from a first inter-level dielectric (ILD) layer **122***a* laterally surrounding the plurality of FeRAM cells **104***a*-**104***b*. In some embodiments, the CESL **218** has an uppermost surface that is substantially planar with upper surfaces of the conductive electrode **116**, the select gate **112**, and the first ILD layer **122***a*. In some embodiments, the CESL **218** may comprise a carbide (e.g., silicon carbide), a nitride (e.g., silicon nitride), or the like. In some embodiments, the first ILD layer **122***a* may comprise an oxide (e.g., silicon oxide), borosilicate glass (BSG), phosphosilicate glass (PSG), or the like.

[0034] A second ILD layer **122***b* is arranged over the first ILD layer **122***a* and an IMD (inter-metal dielectric) layer **122***c* is arranged over the second ILD layer **122***b*. In some embodiments, the second ILD layer **122***b* and/or IMD layer **122***c* may comprise borophosphosilicate glass (BPSG), borosilicate glass (BSG), phosphosilicate glass (PSG), fluorine doped silicon dioxide, carbon doped silicon dioxide, or the like. Conductive contacts **124** extend from a top of the second ILD layer **122***b* to the drain regions **106***a*-**106***b*, the common source region **108**, the select gates **112** (not shown), and the conductive electrode **116** (not shown). Conductive interconnect wires **220** are disposed within IMD layer **122***c*. The conductive interconnect wires **220** are electrically coupled to the conductive contacts **124**. In some embodiments, the conductive contacts **124** and/or the conductive interconnect wires **220** may comprise a metal such as tungsten, copper or the like.

[0035] In some embodiments, one of the conductive contacts **124** that is directly over the common source region **108** may laterally contact the first ILD layer **122***a* (e.g., so that the conductive contact is separated from the CESL **218** by the first ILD layer **122***a*). In other embodiments (not shown), an interface between the one of the conductive contacts **124** that is directly over the common source region **108** and the CESL **218** vertically extends to a horizontal plane extending along a top of the FeRAM devices **110**.

[0036] FIG. **2**B illustrates a cross-sectional view of some alternative embodiments of an FeRAM cell **222**.

[0037] The FeRAM cell **222** comprises a ferroelectric material **114** and a conductive electrode **116**. In some embodiments, the FeRAM cell **222** may be formed by depositing a layer of conductive material over a layer of ferroelectric material and subsequently patterning the layers of conductive and ferroelectric materials. Such patterning causes widths of the ferroelectric material **114** and the conductive electrode **116** to decrease as a distance from a substrate **102** increases due to a selective etching process that is used to define the FeRAM cell **222**. In some embodiments sidewalls of the ferroelectric material **114** and the conductive electrode **116** are angled at one or more non-zero angles with respect to lines **224** that are normal to an upper surface of the substrate **102**. For example, in some embodiments, sidewalls of the ferroelectric material **114** are angled at an angle α with respect to a line **224** that is normal to an upper surface of the substrate **102** and sidewalls of the conductive electrode **116** are angled at an angle β with

respect to a line **224** that is normal to an upper surface of the substrate **102**. In some embodiments, α and β may be substantially equal. In other embodiments, α and β may be different. In some embodiments, α and β may be in a range of approximately 0° and approximately 30°. In some embodiments, α and β may be in a range of between 0° and 30°.

[0038] In some embodiments, the selectivity of etchants used to etch the conductive electrode **116** and the ferroelectric material **114** may be different, so that the conductive electrode **116** and the ferroelectric material **114** etch at different rates. The different etching selectivities may cause the etchants to etch the conductive electrode and the ferroelectric material at different lateral etch rates, causing a bottom surface of the conductive electrode **116** to have a smaller width than a top surface of the ferroelectric material **114**. The smaller width of the bottom surface of the conductive electrode **116** causes the top surface of the ferroelectric material to continuously extends past opposing sides of the conductive electrode **116** by non-zero distances. In other embodiments, the bottom surface of the conductive electrode **116** may have a width that is substantially equal to a width of the top surface of the ferroelectric material **114**.

[0039] In some embodiments, an interfacial dielectric layer **120** may have a first thickness t_1 directly below the ferroelectric material **114** and a second thickness t_2 directly below the select gate **112**. In some embodiments, the first thickness t_1 is different (e.g., larger) than the second thickness t_2. For example, in some embodiments, the first thickness t_1 may be between in a range of between approximately 0 nm and approximately 5 nm larger than the second thickness t_2. In such embodiments, the first sidewall spacer material **212**, the second sidewall spacer material **214**, and the third sidewall spacer material **216** respectively extend from below the ferroelectric material **114** to a top of the conductive electrode **116**. In other embodiments (not shown), the first thickness t_1 is substantially equal to the second thickness t_2. In yet other embodiments (not shown), the interfacial dielectric layer **120** may have a first thickness directly below the ferroelectric material **114**, a second thickness directly below the select gate **112**, and a third thickness outside of the select gate **112** and ferroelectric material **114**. In such embodiments, the first thickness may be larger than the second thickness (e.g., by between approximately 0 nm and approximately 5 nm), and the second thickness may be larger than the third thickness (e.g., by between approximately 0 nm and approximately 5 nm).

[0040] FIG. **3** illustrates a cross-sectional view of some additional embodiments of an integrated chip **300** comprising an embedded FeRAM cell.

[0041] The integrated chip **300** comprises a substrate **102** having an embedded memory region **302***a* separated from a logic region **302***c* by way of a boundary region **302***b*. In some embodiments, the substrate **102** may have a recessed surface **101***a* within the embedded memory region **302***a*. The recessed surface **101***a* is recessed below an upper surface **101***u* of the substrate **102** by a non-zero distance d. In some embodiments, isolation structures **202** may be arranged in trenches in the substrate **102** within the embedded memory region **302***a* and the logic region **302***c*.

[0042] A plurality of FeRAM cells **104***a*-**104***b* are arranged over the recessed surface **101***a*. The plurality of FeRAM cells **104***a*-**104***b* respectively comprise an FeRAM device **110** and a select gate **112**. In some embodiments, the FeRAM device **110** has a height that is in a range of between approximately 500 angstroms and approximately 1000 angstroms. In other embodiments, the FeRAM device **110** has a height that is in a range of between approximately 600 angstroms and approximately 900 angstroms. In some embodiments, the non-zero distance d is in a range of between approximately 100 angstroms and approximately 200 angstroms. The height of the FeRAM device **110** and the non-zero distance d increase a chemical mechanical planarization (CMP) window of the FeRAM device **110** during formation of transistor devices (e.g., high-k metal gate transistor devices) within the logic region **302***c*.

[0043] In some embodiments, the boundary region **302***b* comprises a boundary structure **304** arranged over the substrate **102** and separating the embedded memory region **302***a* from the logic region **302***c*. The boundary structure **304** comprises a boundary isolation structure **306**, a dummy memory structure **308**, and a dummy logic structure **310**.

[0044] The boundary isolation structure **306** extends into a trench disposed between the upper surface **101***u* of the substrate **102** and the recessed surface **101***a* of the substrate **102**. The boundary isolation structure **306** may comprise one or more dielectric materials (e.g., an oxide, a nitride, a carbide, and/or the like) disposed within the trench. The boundary isolation structure **306** comprises a first slanted sidewall **306***a* and a second slanted sidewall **306***b* that define a hillock **306***h* along a top of the boundary isolation structure **306**. In some embodiments, the hillock **306***h* may be closer to the embedded memory region **302***a* than to the logic region **302***c*. In some embodiments, the first slanted sidewall **306***a* is slanted at a shallower angle than the second slanted sidewall **306***b*.

[0045] The dummy memory structure **308** overlies the hillock **306***h*. The dummy memory structure **308** comprises a lower dummy memory layer **312** and an upper dummy memory layer **314** over the lower dummy memory layer **312**. In some embodiments, lower dummy memory layer **312** may comprise, for example, silicon oxide, silicon nitride, silicon oxynitride, silicon carbide, polysilicon, aluminum copper, tantalum, tantalum nitride, titanium nitride, or the like. The lower dummy memory layer **312** is a different material than the upper dummy memory layer **314**, and may be or comprise, for example, silicon oxide, silicon nitride, or the like. In some embodiments, the lower dummy memory layer **312** comprises silicon oxide and the upper dummy memory layer **314** comprises polysilicon. In some embodiments, the dummy memory structure **308** has a substantially vertical sidewall facing the embedded memory region **302***a* and a slanted sidewall facing the logic region **302***c*. In some embodiments, a third sidewall spacer material **216** is arranged between the substantially vertical sidewall and a CESL **218**, while the slanted sidewall directly contacts the CESL **218**.

[0046] The dummy logic structure **310** overlies the boundary isolation structure **306**, between the dummy memory structure **308** and the logic region **302***c*. The dummy logic structure **310** comprises a gate dielectric layer **316** and an overlying upper dummy logic layer **322**. In some embodiments, an etch stop layer **320** may be arranged between the gate dielectric layer **316** and the upper dummy logic layer **322**. In some embodiments, the upper dummy logic layer **322** may comprise polysilicon or some other suitable material.

[0047] The logic region **302***c* comprises a transistor device **324**. The transistor device **324** has a gate electrode **326** arranged over the upper surface **101***u* of the substrate **102** between a second source region **328***a* and a second drain region **328***b*. In some embodiments, the second source region **328***a* and the second drain region **328***b* may contact a well region **330** underlying the gate electrode **326** and having the doping type different than the second source region **328***a* and the second drain region **328***b*. In some embodiments, the gate electrode **326** is separated from the substrate **102** by a gate dielectric layer **316**. In some embodiments, an etch stop layer **320** may be arranged between the gate dielectric layer **316** and the gate electrode **326**. In some embodiments, an interfacial dielectric layer **332** may be arranged between the gate dielectric layer **316** and the substrate **102**.

[0048] In some embodiments, the gate electrode **326** may comprise a metal gate electrode (e.g., comprising aluminum, ruthenium, palladium, or the like) and the gate dielectric layer **316** may comprise a high-k dielectric (e.g., comprising aluminum oxide, hafnium oxide, or the like). In some embodiments, the etch stop layer **320** may comprise tantalum nitride, or the like. In some embodiments, the interfacial dielectric layer **332** may comprise an oxide (e.g., silicon oxide or the like). In other embodiments (not shown), the gate electrode **326** may comprise polysilicon and the gate dielectric layer **316** may comprise an oxide or high-k dielectric (e.g., silicon dioxide). In such embodiments, the etch stop layer **320** may be omitted.

[0049] A first logic sidewall spacer material **334** is arranged along opposing sides of the transistor device **324**. In some embodiments, a second logic sidewall spacer material **336** is arranged along opposing sides of the transistor device **324**. In some embodiments, the first logic sidewall spacer material **334** may comprise a different dielectric material (e.g., silicon nitride) than the second logic sidewall spacer material **336** (e.g., silicon oxide). In some embodiments, the first logic sidewall spacer material **334** may comprise a same material as a first sidewall spacer material (**212** of FIG. **2**A) within the embedded memory region **302***a* and the second logic sidewall spacer material **336** may comprise a same material as a third sidewall spacer material (**216** of FIG. **2**A).

[0050] FIG. **4**A illustrates a schematic diagram of a disclosed FeRAM cell **400**.

[0051] The FeRAM cell **400** comprises a select gate **112** and an FeRAM device **110** arranged between a bit-line (e.g., corresponding to first drain region **106***a* of FIG. **1**) and a source-line (e.g., corresponding to common source region **108** of FIG. **1**). The FeRAM device **110** comprises a ferroelectric material **114** arranged between a channel region **126** and a conductive electrode **116**. The select gate **112** is coupled to a word-line, while the conductive electrode **116** is coupled to a control gate-line that is configured to be biased independently from the word-line.

[0052] FIG. **4**B illustrates a graph **402** showing some embodiments of exemplary operating conditions of the disclosed FeRAM cell **400** of FIG. **4**A. It will be appreciated that data states are written to an FeRAM cell based upon an applied voltage. For example, the application of a positive voltage across the FeRAM cell writes a first data state to the FeRAM cell, while the application of a negative voltage across the FeRAM cell writes a second data state to the FeRAM cell.

[0053] As shown in line **404** of graph **402**, to write a first data state (e.g., corresponding to a logical '1') to an FeRAM device (**110** of FIG. **4**A), the source-line (SL) and the bit-line (BL) are held at approximately 0 V, a word-line (WL) coupled to the select gate (**112** of FIG. **4**A) is held at between approximately 0 V and approximately IV, and the control-gate-line (CGL) is held at a non-zero bias voltage V_{prog}. As shown in line **406** of graph **402**, to write a second data state (e.g., corresponding to a logical '0') to an FeRAM device (**110** of FIG. **4**A), the source-line (SL) and the bit-line (BL) are held at non-zero bias voltages V_{prog}, and the word-line (WL) and the control-gate-line (CGL) are held at approximately 0 V.

[0054] Polarization of the ferroelectric material (**114** of FIG. **4**A) is able to change the threshold voltage of the FeRAM device (**110** of FIG. **4**A), such that a data state can be read from the FeRAM device (**110** of FIG. **4**A) by detecting a change in the threshold voltage of the FeRAM device (**110** of FIG. **4**A). As shown in line **408** of graph **402**, to read a data state from the FeRAM device (**110** of FIG. **4**A) the bit-line (BL) is held at approximately 0 V, the word-line (WL) is held at between approximately 0.5 V and 1.8 V, the source-line (SL) is held at between approximately 0.5 V and V_{dd}, and the control-gate-line (CGL) is held at between approximately 0 V and V_{dd}.

[0055] It will be appreciated that the value of the non-zero bias voltage V_{prog} may vary depending on the ferroelectric material of the FeRAM device (**110** of FIG. **4**A). For example, an FeRAM device having a ferroelectric material of hafnium oxide may use a different non-zero bias voltage V_{prog} (e.g., V_{prog} is approximately equal to 6 V) than a FeRAM device having a ferroelectric material of PZT.

[0056] FIG. **4**C illustrates a memory structure **410** comprising a plurality of FeRAM cells **400***a*-**400***d*.

[0057] The plurality of FeRAM cells **400***a*-**400***d* are arranged within a memory array **412** in rows and/or columns. The plurality of FeRAM cells **400***a*-**400***d* within a row are operably coupled to word-lines WL_1-WL_2 by way of a select gate **112** and to control-gate-lines CGL_1-CGL_2. The plurality of FeRAM cells **400***a*-**400***d* within a column are operably coupled to bit-lines BL_1-BL_2 and source-lines SL_1-SL_2.

[0058] The word-lines WL_1-WL_2, the bit-lines BL_1-BL_2, the source-lines SL_1-SL_2, and the control-gate-lines CGL_1-CGL_2 are coupled to control circuitry **414**. In some embodiments, the control circuitry **414** comprises a word-line decoder **416** coupled to the word-lines WL_1-WL_2, a bit-line decoder **418** coupled to the bit-lines BL_1-BL_2, a source-line decoder **420** coupled to the source-lines SL_1-SL_2, and a control gate decoder **422** coupled to the control-gate-lines CGL_1-CGL_2. The word-line decoder **416** is configured to selectively apply a bias voltage to one of the word-lines WL_1-WL_2. Concurrently, the bit-line decoder **418** is configured to selectively apply a bias voltage to one of the bit-lines BL_1-BL_2. the source-line decoder **420** is configured to selectively apply a bias voltage to one of the source-lines SL_1-SL_2, and the control gate decoder **422** is configured to selectively apply a bias voltage to one of the control-gate-lines CGL_1-CGL_2. By applying bias voltages to selective ones of the word-lines WL_1-WL_2, the bit-lines BL_1-BL_2, the source-lines SL_1-SL_2, and the control-gate-lines CGL_1-CGL_2, the plurality of FeRAM cells **400***a*-**400***d* can be operated to store different data states.

[0059] FIGS. **5-25** illustrate cross-sectional views **500-2500** of some embodiments of a method of forming an integrated chip having an embedded FeRAM cell. Although FIGS. **5-25** are described in relation to a method, it will be appreciated that the structures disclosed in FIGS. **5-25** are not limited to such a method, but instead may stand alone as structures independent of the method.

[0060] As shown in cross-sectional view **500** of FIG. **5**, a substrate **102** is provided. In various embodiments, the substrate **102** may comprise any type of semiconductor body (e.g., silicon/CMOS bulk, SiGe, SOI, etc.) such as a semiconductor wafer or one or more die on a wafer, as well as any other type of semiconductor and/or epitaxial layers formed thereon and/or otherwise associated therewith. The substrate **102** has an embedded memory region **302***a* and a logic region **302***c* laterally separated by a boundary region **302***b*.

[0061] A first masking structure **501** is formed over the substrate **102**. In some embodiments the first masking structure **501** may comprise a multi-layer masking structure comprising a first masking layer **502** and a second masking layer **504**. In some embodiments, the first masking layer **502** may comprise an oxide (e.g., silicon oxide) and the second masking layer **504** may comprise a nitride (e.g., silicon nitride), for example.

[0062] As shown in cross-sectional view **600** of FIG. **6**, the first masking structure **501** is selectively patterned so that the first masking structure **501** covers the logic region **302***c* and exposes the embedded memory region **302***a*. In some embodiments, the first masking structure **501** further covers a part of the boundary region **302***b*. In some embodiments, the first masking structure **501** is selectively patterned by forming a photoresist layer **604** over the first masking structure **501** and subsequently exposing the first masking structure **501** to a first etchant **602** in areas not covered by the photoresist layer **604**. In some embodiments, a resist protective oxide **606** may be deposited over a part of the first masking structure **501** prior to formation of the photoresist layer **604**.

[0063] As shown in cross-sectional view **700** of FIG. **7**, a thermal oxidation process is performed on the substrate **102**. The thermal oxidation process forms a thermal oxide **704** on a surface of the substrate **102** not covered by the first masking structure **501**. The formation of the thermal oxide **704** consumes a part of the substrate **102** within the embedded memory region **302***a*, thereby forming a depressed region having a recessed surface **101***a* of the substrate **102** within the embedded memory region **302***a*. The recessed surface **101***a* is depressed below an upper surface **101***u* of the substrate **102** by a non-zero distance d.

[0064] As shown in cross-sectional view **800** of FIG. **8**, the thermal oxide (**704** of FIG. **7**) is removed. Removal of the thermal oxide (**704** of FIG. **7**) exposes the recessed surface **101***a* of the substrate **102**. Although FIGS. **6-8** recess the embedded memory region **302***a* of the substrate using a thermal oxidation process, it will be appreciated that in alternative embodiments, the substrate **102** may be recessed within the embedded memory region **302***a* by selectively etching the substrate **102** in regions not covered by the first masking structure **501**.

[0065] As shown in cross-sectional view **900** of FIG. **9**, a pad dielectric layer **902** is formed over the substrate **102** and a first protective layer **904** is formed over the pad dielectric layer **902**. In some embodiments, the pad dielectric layer **902** may comprise an oxide formed by a thermal oxidation process. In some embodiments, the first protective layer **904** may comprise a nitride, a carbide, or the like. In some embodiments, the first protective layer **904** may be formed by way of a deposition process (e.g., a physical vapor deposition (PVD) process, a chemical vapor deposition (CVD) process, a plasma enhanced chemical vapor deposition (PE-CVD) process, an atomic layer deposition (ALD) process, or the like).

[0066] As shown in cross-sectional view **1000** of FIG. **10**, a plurality of isolation structures **202** are formed within the embedded memory region **302***a* and the logic region **302***c*. A boundary isolation structure **306** is also formed within the boundary region **302***b*.

[0067] In some embodiments, the plurality of isolation structures **202** and the boundary isolation structure **306** may be formed by selectively patterning the pad dielectric layer **902** and the first protective layer **904** to form a plurality of openings extending through the pad dielectric layer **902** and the first protective layer **904**. The substrate **102** is subsequently etched according to the plurality of openings to form a plurality of trenches **1002** within the substrate **102**. The plurality of trenches **1002** are filled with one or more dielectric materials. In some embodiments, the one or more dielectric materials may be formed by way of a deposition process to fill the plurality of trenches **1002** and to extend over an uppermost surface of the first protective layer **904**. A first planarization process (e.g., a chemical mechanical planarization process) may subsequently be performed (along line **1004**) to remove the one or more dielectric materials from over an uppermost surface of the first protective layer **904** and to define the plurality of isolation structures **202** and the boundary isolation structure **306**. In some embodiments, the one or more dielectric materials may comprise an oxide (e.g., silicon oxide), a nitride, and/or the like.

[0068] As shown in cross-sectional view **1100** of FIG. **11**, a third masking layer **1102** is formed over the embedded memory region **302***a* and a part of the boundary region **302***b*. The isolation structures **202** and a part of the boundary isolation structure **306** not covered by the third masking layer **1102** are subsequently exposed to a second etchant **1104**. The second etchant **1104** recesses the isolation structures **202** and the part of the boundary isolation structure **306** not covered by the third masking layer **1102**. In some embodiments, the second etchant **1104** gives the boundary isolation structure a first slanted sidewall. The third masking layer **1102** retains the first protective layer **904** in the logic region **302***c*, so that the first protective layer **904** can be subsequently removed during a separate etch during formation of logic devices in the logic region **302***c*. This gives more control over formation of the logic devices, thereby increasing logic device compatibility with the embedded memory region **302***a*.

[0069] As shown in cross-sectional view **1200** of FIG. **12**, the pad dielectric layer **902** and the first protective layer **904** are removed from within the embedded memory region **302***a*. In some embodiments, the pad dielectric layer **902** and the first protective layer **904** may be removed by selectively etching the pad dielectric layer **902** and the first protective layer **904** according to the third masking layer (**1102** of FIG. **11**).

[0070] As shown in cross-sectional view **1300** of FIG. **13**, an interfacial dielectric layer **120** is formed within the

embedded memory region **302***a* over the substrate **102**. In some embodiments, the interfacial dielectric layer **120** may comprise an oxide formed by a thermal oxidation process. In other embodiments, the interfacial dielectric layer **120** may comprise a different dielectric layer (e.g., a nitride and/or a carbide) formed by a deposition process.

[0071] An FeRAM stack **1301** is formed over the interfacial dielectric layer **120** within the embedded memory region **302***a*, the boundary region **302***b*, and the logic region **302***c*. The FeRAM stack **1301** comprises a ferroelectric layer **1302** and one or more conductive layers over the ferroelectric layer **1302**. In some embodiments, the one or more conductive layers may comprise an etch stop layer **1304** and a conductive electrode layer **1306**. In some embodiments, the ferroelectric layer **1302** and the one or more conductive layers may be formed by way of a plurality of separate deposition process (e.g., PVD, CVD, PE-CVD, ALD, or the like).

[0072] In various embodiments, the ferroelectric layer **1302** may comprise silicon doped hafnium oxide (Si-doped HfO_2), lead titanate, lead zirconate titanate (PZT), lead lanthanum zirconate titanate, strontium bismuth tantalate (SBT), bismuth lanthanum titanate (BLT), bismuth neodymium titanate (BNT), or the like. In some embodiments, the etch stop layer **1304** may comprise aluminum, ruthenium, palladium, hafnium, zirconium, titanium, or the like. In some embodiments, the conductive electrode layer **1306** may comprise, polysilicon or the like.

[0073] As shown in cross-sectional view **1400** of FIG. **14**, the FeRAM stack (**1301** of FIG. **13**) is selectively patterned to form a plurality of FeRAM device stacks **1402***a*-**1402***b* within the embedded memory region **302***a*. The plurality of FeRAM device stacks **1402***a*-**1402***b* respectively comprise a ferroelectric material **114**, an etch stop layer **208**, and a conductive material **210**. The FeRAM stack (**1301** of FIG. **13**) is selectively etched to also form a sacrificial dummy stack **1404** within the boundary region **302***b* and the logic region **302***c*. The sacrificial dummy stack **1404** is configured to increase a process window of subsequent planarization processes (e.g., CMP processes) by providing structural support to the planarization process.

[0074] In some embodiments, the FeRAM stack (**1301** of FIG. **13**) may be selectively patterned by forming a hard mask **1405** over the FeRAM stack. The FeRAM stack may subsequently be exposed to a third etchant **1410** that removes the FeRAM stack in areas not covered by the hard mask **1405**. In some embodiments, the hard mask **1405** may comprise a multi-layer hard mask having a first hard mask layer **1406** and a second hard mask layer **1408** over the first hard mask layer **1406**. In some embodiments, the first hard mask layer **1406** may comprise a dielectric, such as silicon nitride, silicon carbide, or the like. In some embodiments, the second hard mask layer **1408** may comprise silicon oxide or the like.

[0075] As shown in cross-sectional view **1500** of FIG. **15**, a first sidewall spacer material **212** is formed along opposing sidewalls of the plurality of FeRAM device stacks **1402***a*-**1402***b*. A second sidewall spacer material **214** is subsequently formed along opposing sidewalls of the first sidewall spacer material **212**. In some embodiments, the first sidewall spacer material **212** and the second sidewall spacer material **214** may be formed by depositing separate spacer layers onto the plurality of FeRAM device stacks **1402***a*-**1402***b*. The separate spacer layers are subsequently etched to remove the separate spacer layers from horizontal surfaces, leaving the first sidewall spacer material **212** and the second sidewall spacer material **214** along opposing sides of the plurality of FeRAM device stacks **1402***a*-**1402***b*. In various embodiments, the separate spacer layers may comprise silicon nitride, a silicon dioxide (SiO_2), silicon oxy-nitride (e.g., SiON), or a similar material.

[0076] A select gate layer **1502** is formed over the substrate **102** and along sidewalls of the second sidewall spacer material **214**. In various embodiments, the select gate layer **1502** may comprise doped polysilicon, a metal, or another conductive material. The select gate layer **1502** may be formed to a height that is less than a height of the plurality of FeRAM device stacks **1402***a*-**1402***b*. For example, in some embodiments the select gate layer **1502** may be formed using a deposition process (e.g., PVD, CVD, ALD, PE-CVD, or the like) to deposit a select gate material (e.g., doped polysilicon) covering the plurality of FeRAM device stacks **1402***a*-**1402***b*. The select gate material is subsequently etched back to a height that is less than the select gate layer **1502** (e.g., a height that is in a range of between approximately 50 nm and approximately 150 nm). In some embodiments, a planarization layer (e.g., a bottom layer anti-reflective coating (BARC)) may be formed to cover the select gate material prior to performing the etch back. The planarization layer forms a planar upper surface over the plurality of FeRAM device stacks **1402***a*-**1402***b*, and causes the resulting select gate layer **1502** to have substantially flat upper surfaces adjacent to the plurality of FeRAM device stacks **1402***a*-**1402***b*. In some embodiments, the etch back may be performed using a dry etching process.

[0077] A hard mask layer **1504** is formed over the select gate layer **1502**. The hard mask layer **1504** may be formed by way of a deposition process (e.g., PVD, CVD, ALD, PE-CVD, or the like) to a thickness that is in a range of between approximately 30 nm and approximately 80 nm. In some embodiments, the hard mask layer **1504** comprises protrusions **1506** directly over the plurality of FeRAM device stacks **1402***a*-**1402***b*. In some embodiments, the hard mask layer **1504** may comprise silicon nitride, silicon carbide, or the like.

[0078] As shown in cross-sectional view **1600** of FIG. **16**, the hard mask layer **1504** is selectively patterned and the select gate layer (**1502** of FIG. **15**) is subsequently patterned according to the hard mask layer **1504** to define select gates **112** arranged along first sides of the FeRAM device stacks **1402***a*-**1402***b*. In some embodiments, the hard mask layer **1504** and the select gate layer (**1502** of FIG. **15**) may be patterned by a blanket (e.g., unmasked) etch which removes the select gate layer (**1502** of FIG. **15**) from areas that are covered by a thinner layer of the hard mask layer **1504**. In some embodiments, the select gates **112** may have a height h_1 that is in a range of between approximately 50 nm and approximately 150 nm, and a width w/that is in a range of between approximately between approximately 30 nm and approximately 80 nm. The height of the select gate **112** defines an electrical performance (e.g., a device leakage, on current, or the like) of the select gates **112***a*.

[0079] As shown in cross-sectional views **1700** of FIG. **17**, a remainder of the select gate layer (**1502** of FIG. **15**) is removed between second sides of the FeRAM device stacks **1402***a*-**1402***b*. In some embodiments, the remainder of the select gate layer (**1502** of FIG. **15**) may be removed by a photolithography process followed by a selective etching

process. For example, a masking layer (e.g., a photoresist layer) may be formed over the substrate **102** and have sidewalls that define an opening that is directly over the select gate layer (**1502** of FIG. **15**) between the second sides of the FeRAM device stacks **1402***a*-**1402***b*. The select gate layer (**1502** of FIG. **15**) is subsequently exposed to an etchant according to the opening in the masking layer to remove the remainder of the select gate layer (**1502** of FIG. **15**). After the etching process is completed the masking layer may be removed.

[0080] After removing the remainder of the select gate layer (**1502** of FIG. **15**), a common source region **108** is formed within the substrate **102** between the second sides of the FeRAM device stacks **1402***a*-**1402***b*. In some embodiments, the common source region **108** is formed by selectively implanting a dopant species into the substrate **102**.

[0081] A lower dummy memory layer **312** is formed over the substrate **102**. The lower dummy memory layer **312** continuously extends over the FeRAM device stacks **1402***a*-**1402***b* and the sacrificial dummy stack **1404**. In some embodiments, the lower dummy memory layer **312** may comprise an oxide, such as silicon dioxide, for example. In other embodiments, the lower dummy memory layer **312** may comprise polysilicon.

[0082] A fourth masking layer **1702** is formed over the substrate **102**. The fourth masking layer **1702** covers the embedded memory region **302***a*, the boundary region **302***b*, and the logic region **302***c*. In some embodiments, fourth masking layer **1702** may have an upper surface with a curve between a first height over the embedded memory region **302***a* and a second height over the logic region **302***c*. In some embodiments, the fourth masking layer **1702** may comprise a polysilicon layer.

[0083] As shown in cross-sectional views **1800** of FIG. **18**, a planarization process is performed on the fourth masking layer **1702**. The planarization process is performed along line **1802**, so as to form a planar surface extending from over the embedded memory region **302***a* to over the logic region **302***c*. In some embodiments, the planarization process may comprise a CMP process.

[0084] As shown in cross-sectional views **1900** of FIG. **19**, the fourth masking layer **1702** is selectively etched to remove the fourth masking layer **1702** from within the logic region **302***c* and a part of the boundary region **302***b*. The boundary isolation structure **306** is subsequently etched to form a second slanted sidewall **306***b*. The first slanted sidewall and the second slanted sidewall define a hillock **306***h* along a top of the boundary isolation structure **306**.

[0085] In some embodiments, the fourth masking layer **1702** and the boundary isolation structure **306** may be selectively exposed to one or more etchants **1902** according to a fifth masking layer **1904** formed over the embedded memory region **302***a* and a part of the boundary region **302***b*. In some embodiments, the fourth masking layer **1702** and the boundary isolation structure **306** may be selectively etched using a same etchant. In other embodiments, the fourth masking layer **1702** may be selectively etched using a fourth etchant and the boundary isolation structure **306** may be selectively etched using a fifth etchant that is different than the fourth etchant. For example, in some embodiments, fourth masking layer **1702** may be selectively etched using an etchant comprising phosphoric acid (HP_3O_4) or the like. The boundary isolation structure **306** may be subsequently etched using a wet etchant comprising hydrofluoric acid (HF) or the like.

[0086] In some embodiments, the one or more etchants **1902** may also remove the sacrificial dummy stack (**1404** of FIG. **18**), the first masking layer (**502** of FIG. **18**), and the second masking layer (**504** of FIG. **18**). In some embodiments, an interfacial dielectric layer **332** may be formed over the substrate **102** within the logic region **302***c* after removal of the first masking layer **502** and the second masking layer **504**. In some embodiments, the interfacial dielectric layer **332** may comprise an oxide (e.g., silicon oxide or the like). In some embodiments, the interfacial dielectric layer **332** within the logic region **302***c* may have a different thickness than an interfacial dielectric layer (**120** of FIG. **13**) within the embedded memory region **302***a*. In some embodiments, a well region **330** may also be formed within the substrate **102** in the logic region **302***c* after removal of the first masking layer **502** and the second masking layer **504**.

[0087] As shown in cross-sectional views **2000** of FIG. **20**, a sacrificial gate stack **2002** is formed over the substrate **102**. The sacrificial gate stack **2002** continuously extends from within the logic region **302***c* to over the fourth masking layer **1702** within the embedded memory region **302***a*. In some embodiments, the sacrificial gate stack **2002** may comprise a gate dielectric layer **316**, a sacrificial gate electrode layer **2004**, and a hard mask **2006**. In some embodiments, an etch stop layer **320** may be arranged between the gate dielectric layer **316** and the sacrificial gate electrode layer **2004**. In some embodiments, the sacrificial gate electrode layer **2004** may comprise polysilicon. In some embodiments, the hard mask **2006** may comprise a multi-layer hard mask having a first hard mask layer **2008** (e.g., SiN) and a second hard mask layer **2010** (e.g., silicon oxide) over the first hard mask layer **2008**.

[0088] In some embodiments, the gate dielectric layer **316** may comprise a high-k dielectric, such as, aluminum oxide, hafnium oxide, or the like. In some embodiments, the etch stop layer **320** may comprise tantalum nitride, or the like. In some embodiments, the first hard mask layer **2008** may comprise a dielectric, such as silicon nitride, silicon carbide, or the like. In some embodiments, the second hard mask layer **2010** may comprise silicon oxide or the like.

[0089] As shown in cross-sectional view **2100** of FIG. **21**, a thickness of the sacrificial gate electrode layer **2004** is reduced within the embedded memory region **302***a* and within a part of the boundary region **302***b*. In some embodiments, the thickness of the sacrificial gate electrode layer **2004** may be reduced by between approximately 50% and approximately 75%. In some embodiments, the thickness of the sacrificial gate electrode layer **2004** is reduced by forming a sixth masking layer **2102** over the hard mask **2006** within the logic region **302***c* and a part of the boundary region **302***b*. The hard mask **2006** and the sacrificial gate electrode layer **2004** arc subsequently exposed to a sixth etchant **2104** in areas not covered by the sixth masking layer **2102**.

[0090] As shown in cross-sectional view **2200** of FIG. **22**, the sacrificial gate stack **2002** is patterned according to a patterning process to define a dummy gate structure **2202** within the logic region **302***c* and to define a dummy logic structure **310** over the boundary isolation structure. In some embodiments, the patterning process will vertically and laterally etch the second hard mask layer **2010**. In some such embodiments, the proximity of the dummy logic structure

310 to an edge of the second hard mask layer 2010 will cause the second hard mask layer 2010 that remains along a top of the dummy logic structure 310 (after the patterning process) to have outer sidewalls oriented at different angles. The fourth masking layer (1702 of FIG. 21) is also etched to define dummy memory structure 308 over the hillock 306*h* in the boundary isolation structure 306.

[0091] In some embodiments, a first logic sidewall spacer material 334 may be formed along sidewalls of the sacrificial gate stack 2002 and the dummy memory structure 308. A third sidewall spacer material 216 may also be formed along sidewalls of the FeRAM device stacks 1402*a*-1402*b*, and a second logic sidewall spacer material 336 may be formed along sidewalls of the sacrificial gate stack 2002, the dummy memory structure 308, the dummy logic structure 310, and the select gate 112. In some embodiments, the first logic sidewall spacer material 334, the second logic sidewall spacer material 336, and the third sidewall spacer material 216 may be formed by depositing one or more dielectric materials over the substrate 102 and subsequently etching the one or more dielectric materials to remove the one or more dielectric materials from horizontal surfaces. In some embodiments, etching the one or more dielectric materials may also remove the one or more dielectric materials from a sidewall of the second hard mask layer 2010 facing the FeRAM device stacks 1402*a*-1402*b*. In some such embodiments, the first logic sidewall spacer material 334 and/or the second logic sidewall spacer material 336 have different heights along opposing sidewalls of the dummy memory structure 308. In some embodiments, the one or more dielectric materials may comprise an oxide, a nitride, a carbide, or the like.

[0092] Drain regions 106*a*-106*b* are formed within the embedded memory region 302*a* and a second source region 328*a* and a second drain region 328*b* are formed within the logic region 302*c*. In some embodiments, the drain regions 106*a*-106*b* are formed by way of a first implantation process, while the second source region 328*a* and the second drain region 328*b* are formed by way of a second implantation process. In some embodiments, the first and second implantation processes are a same implantation process. In some embodiments, the drain regions 106*a*-106*b* have a same doping type as the common source region 108, while the second source region 328*a* and the second drain region 328*b* have an opposite doping type as the well region 330.

[0093] A silicidation process is performed to form a silicide layer 204 along upper surfaces of the drain regions 106*a*-106*b*, the common source region 108, the second source region 328*a*, and the second drain region 328*b*. In some embodiments, the silicidation process may also form a silicide on the conductive electrode 116 and/or the select gate 112. In some embodiments, the silicidation process may be performed by depositing a metal layer (e.g., a nickel layer) and then performing a thermal annealing process (e.g., a rapid thermal anneal) to form the silicide layer 204.

[0094] As shown in cross-sectional view 2300 of FIG. 23, a first inter-level dielectric (ILD) layer 122*a* is formed over the substrate 102. The first ILD layer 122*a* laterally surrounds the plurality of FeRAM device stacks (1402*a*-1402*b* of FIG. 22), the dummy memory structure 308, the dummy logic structure 310, and the dummy gate structure 2202. In various embodiments, the first ILD layer 122*a* may be deposited onto the substrate 102 by a chemical vapor deposition (CVD) process using high aspect ratio process (i.e., a HARP oxide). For example, in some embodiments, the first ILD layer 122*a* may comprise an oxide or boron-phosphor-silicate glass deposited by a CVD process. After formation of the first ILD layer 122*a*, a fourth planarization process may be performed along line 2302 to expose upper surfaces of the dummy gate structure 2202 within the logic region 302*c* and to define FeRAM cells 104*a*-104*b* within the embedded memory region 302*a*.

[0095] As shown in cross-sectional view 2400 of FIG. 24, the sacrificial gate electrode layer (2004 of FIG. 23) is removed from the dummy gate structure (2202 of FIG. 23) to define a gate electrode cavity 2402. In some embodiments, the sacrificial gate electrode layer (2004 of FIG. 23) may be removed by selectively exposing the sacrificial gate electrode layer (2004 of FIG. 23) to a seventh etchant 2404.

[0096] As shown in cross-sectional view 2500 of FIG. 25, a gate electrode 326 is formed within the gate electrode cavity 2402. In some embodiments, the gate electrode 326 may be formed by forming one or more metal gate materials 2502 within the gate electrode cavity 2402 and over the first ILD layer 122*a*. In some embodiments, the one or more metal gate materials 2502 may be formed using a deposition process (e.g., PVD, CVD, ALD, PE-CVD, or the like). A fifth planarization process is subsequently performed along line 2504. The fifth planarization process removes a part of the one or more metal gate materials 2502 from over the first ILD layer 122*a* to define a gate electrode 326. In some embodiments, the one or more metal gate materials 2502 may comprise an n-type gate metal such as aluminum, tantalum, titanium, hafnium, zirconium, titanium silicide, tantalum nitride, tantalum silicon nitride, chromium, tungsten, cooper, titanium aluminum, or the like. In other embodiments, the one or more metal gate materials 2502 may comprise a p-type gate metal such as nickel, cobalt, molybdenum, platinum, lead, gold, tantalum nitride, molybdenum silicide, ruthenium, chromium, tungsten, copper, or the like.

[0097] As shown in cross-sectional view 2600 of FIG. 26, conductive contacts 124 are formed within a second ILD layer 122*b* overlying the first ILD layer 122*a*. Conductive interconnect wires are also formed within an IMD layer 122*c* overlying the second ILD layer 122*b*.

[0098] In some embodiments, the conductive contacts 124 and/or the conductive interconnect wires 220 may be formed using a damascene process. For example, in some embodiments, the conductive contacts 124 may be formed by forming the second ILD layer 122*b* over the first ILD layer 122*a*, selectively etching the second ILD layer 122*b* to form via holes, and subsequently depositing a first conductive material within the via holes. In some embodiments, the first conductive material may comprise tungsten (W) or titanium nitride (TiN), for example. Similarly, in some embodiments, the conductive interconnect wires 220 may be formed by forming an IMD layer 122*c* over the second ILD layer 122*b*, selectively etching IMD layer 122*c* to form trenches, and subsequently depositing a second conductive material within the trenches. In some embodiments, the second conductive material may comprise copper (Cu) and/or aluminum (Al), for example.

[0099] FIG. 27 illustrates a flow diagram of some embodiments of a method 2700 of forming an integrated chip having an embedded FeRAM cell.

[0100] While method 2700 is illustrated and described below as a series of acts or events, it will be appreciated that

the illustrated ordering of such acts or events are not to be interpreted in a limiting sense. For example, some acts may occur in different orders and/or concurrently with other acts or events apart from those illustrated and/or described herein. In addition, not all illustrated acts may be required to implement one or more aspects or embodiments of the description herein. Further, one or more of the acts depicted herein may be carried out in one or more separate acts and/or phases.

[0101] At **2702**, a substrate is provided. The substrate has an embedded memory region separated from a logic region by a boundary region. FIG. **5** illustrates a cross-sectional view **500** of some embodiments corresponding to act **2702**.

[0102] At **2704**, the substrate is recessed within the embedded memory region. FIGS. **6-8** illustrate cross-sectional views **600-800** of some embodiments corresponding to act **2704**.

[0103] At **2706**, a plurality of isolation structures are formed within the embedded memory region and the logic region. FIGS. **9-12** illustrate cross-sectional views **900-1200** of some embodiments corresponding to act **2706**.

[0104] At **2708**, a boundary isolation structure is formed within the boundary region. FIGS. **9-12** illustrate cross-sectional views **900-1200** of some embodiments corresponding to act **2708**.

[0105] At **2710**, a plurality of memory device stacks are formed within the embedded memory region. FIGS. **13-14** illustrate cross-sectional views **1300-1400** of some embodiments corresponding to act **2710**.

[0106] At **2712**, select gates are formed along sidewalls of the memory device stacks. FIGS. **15-16** illustrate cross-sectional views **1500-1600** of some embodiments corresponding to act **2712**.

[0107] At **2714**, a masking layer is formed over the embedded memory region. The masking layer exposes the logic region and a part of the embedded memory region. FIGS. **17-18** illustrate cross-sectional views **1700-1800** of some embodiments corresponding to act **2714**.

[0108] At **2716**, the boundary isolation structure is patterned according to the masking layer. FIG. **19** illustrates a cross-sectional view **1900** of some embodiments corresponding to act **2716**.

[0109] At **2718**, a sacrificial transistor stack is formed over the masking layer and within the logic region. The sacrificial transistor stack comprises a sacrificial gate electrode. FIGS. **20-22** illustrate cross-sectional views **2000-2200** of some embodiments corresponding to act **2718**.

[0110] At **2720**, the sacrificial gate stack is patterned to define a sacrificial transistor stack within the logic region and a dummy memory structure and a dummy logic structure over the boundary isolation structure. FIGS. **20-22** illustrate cross-sectional views **2000-2200** of some embodiments corresponding to act **2720**.

[0111] At **2722**, a first inter-level dielectric (ILD) layer is deposited over the substrate. FIG. **23** illustrates a cross-sectional view **2300** of some embodiments corresponding to act **2722**.

[0112] At **2724**, a planarization process is performed to expose a top of a sacrificial gate electrode within the sacrificial gate stack. FIG. **23** illustrates a cross-sectional view **2300** of some embodiments corresponding to act **2724**.

[0113] At **2726**, the sacrificial gate electrode is replaced with a metal gate. FIGS. **24-25** illustrate cross-sectional views **2400-2500** of some embodiments corresponding to act **2726**.

[0114] At **2728**, conductive contacts are formed within a second ILD layer over the substrate. FIG. **26** illustrates a cross-sectional view **2600** of some embodiments corresponding to act **2728**.

[0115] Accordingly, in some embodiments, the present disclosure relates to an integrated chip having an embedded FeRAM cell comprising a select gate configured to selectively provide access to an FeRAM device. The select gate provides for a relatively low current in channel regions of unselected FeRAM cells, thereby improving the power consumption and/or read operations of an FeRAM array.

[0116] In some embodiments, the present disclosure relates to a memory structure. The memory structure includes a source region and a drain region disposed within a substrate; a select gate disposed over the substrate between the source region and the drain region; and a ferroelectric random access memory (FeRAM) device disposed over the substrate between the select gate and the source region, the FeRAM device including a ferroelectric material arranged between the substrate and a conductive electrode. In some embodiments, the select gate and the conductive electrode include polysilicon. In some embodiments, the conductive electrode has an etch stop layer contacting an upper surface of the ferroelectric material. In some embodiments, the memory structure further includes a sidewall spacer arranged between the select gate and the FeRAM device. In some embodiments, the sidewall spacer includes a dielectric material that continuously extends to directly contact and completely cover a sidewall of the conductive electrode and a sidewall of the ferroelectric material. In some embodiments, the memory structure further includes an interfacial dielectric layer continuously extending from between the select gate and the substrate to between the ferroelectric material and the substrate. In some embodiments, the interfacial dielectric layer has a first thickness directly below the ferroelectric material and a second thickness directly below the select gate; the first thickness is different than the second thickness. In some embodiments, the memory structure further includes an inter-level dielectric (ILD) layer arranged over the substrate; a first conductive contact extending from a top of the ILD layer to the select gate; and a second conductive contact extending from the top of the ILD layer to the conductive electrode. In some embodiments, the substrate has a recessed surface extending between a first sidewall and a second sidewall of the substrate to define a depressed region within an upper surface of the substrate; the FeRAM device is arranged over the recessed surface and directly between the first sidewall and the second sidewall. In some embodiments, the memory structure further includes a word-line decoder coupled to the select gate by a word-line; and a control gate decoder coupled to the conductive electrode by a control-gate-line extending in parallel to the word-line.

[0117] In other embodiments, the present disclosure relates to an integrated chip. The integrated chip includes a common source region disposed within a recessed surface of a substrate between a first drain region and a second drain region, the recessed surface is recessed below an upper surface of the substrate by a non-zero distance; a boundary isolation structure arranged laterally between the recessed

surface and the upper surface; a first ferroelectric random access memory (FeRAM) cell having a first select gate disposed over the recessed surface between the common source region and the first drain region and a first FeRAM device disposed over the recessed surface between the first select gate and the common source region; and a second FeRAM cell having a second select gate disposed over the recessed surface between the common source region and the second drain region and a second FeRAM device disposed over the recessed surface between the second select gate and the common source region. In some embodiments, the first FeRAM device includes a conductive material separated from a ferroelectric material by an etch stop layer. In some embodiments, the first FeRAM device and the first select gate include a same material. In some embodiments, the first FeRAM device includes a ferroelectric material and a conductive electrode disposed over the ferroelectric material. In some embodiments, the first select gate is coupled to a word-line and the conductive electrode is coupled to a control-gate line that is configured to be biased independently from the word-line. In some embodiments, the integrated chip further includes a sidewall spacer laterally disposed between the first select gate and the first FeRAM device. In some embodiments, the sidewall spacer includes a first sidewall spacer material directly contacting the ferroelectric material and the conductive electrode; and a second sidewall spacer material directly contacting the first select gate, the first sidewall spacer material and the second sidewall spacer material having substantially equal heights. In some embodiments, the sidewall spacer extends from a first horizontal plane extending along a bottom of the first FeRAM device to a second horizontal plane extending along a top of the first FeRAM device.

[0118] In yet other embodiments, the present disclosure relates to a method of forming a memory structure. The method includes forming an interfacial dielectric layer over a substrate; depositing a ferroelectric random access memory (FeRAM) stack over the interfacial dielectric layer, the FeRAM stack having a ferroelectric layer and one or more conductive layers over the ferroelectric layer; patterning the FeRAM stack to define an FeRAM device stack; forming a select gate layer laterally surrounding the FeRAM device stack; patterning the select gate layer to define a select gate along a second side of the FeRAM device stack; forming a common source region within the substrate along a first side of the FeRAM device stack; and forming a drain region within the substrate, wherein the drain region is separated from the FeRAM device stack by the select gate. In some embodiments, the method further includes recessing a part of the substrate to form a recessed surface of the substrate that is depressed below an upper surface of the substrate, the FeRAM device stack and the select gate are formed directly over the recessed surface.

[0119] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. An integrated chip structure, comprising:

a first select gate and a second select gate disposed over a substrate;

a first ferroelectric random access memory (FeRAM) stack and a second FeRAM stack disposed over the substrate and laterally between the first select gate and the second select gate;

an inter-level dielectric disposed over the substrate and laterally surrounding the first select gate, the second select gate, the first FeRAM stack, and the second FeRAM stack; and

a conductive contact extending through the inter-level dielectric, wherein the first select gate and the second select gate are substantially symmetrically disposed along opposing sides of the conductive contact and wherein the first FeRAM stack and the second FeRAM stack are substantially symmetrically disposed along opposing sides of the conductive contact.

2. The integrated chip structure of claim **1**, wherein the conductive contact has a larger height than the first FeRAM stack and the second FeRAM stack.

3. The integrated chip structure of claim **1**, wherein a bottommost surface of the first FeRAM stack is vertically separated from the substrate by a first distance and a bottommost surface of the first select gate is vertically separated from the substrate by a second distance that is different than the first distance.

4. The integrated chip structure of claim **1**, wherein the first FeRAM stack has a greater maximum width than the first select gate.

5. The integrated chip structure of claim **1**, further comprising:

a dielectric spacer arranged laterally between the first FeRAM stack and the first select gate, wherein the dielectric spacer laterally contacts the first FeRAM stack and the first select gate.

6. The integrated chip structure of claim **1**, further comprising:

a dielectric spacer arranged laterally between the first FeRAM stack and the first select gate, wherein the dielectric spacer has a topmost surface that is substantially co-planar with topmost surfaces of the first FeRAM stack and the first select gate.

7. The integrated chip structure of claim **1**, further comprising:

a dielectric spacer arranged laterally between the first FeRAM stack and the first select gate, wherein the dielectric spacer comprises dielectric layers laterally contacting one another along a vertical interface extending between a top and a bottom of the first FeRAM stack.

8. The integrated chip structure of claim **1**, wherein the first select gate vertically extends from below a first height of a bottommost surface of the first FeRAM stack to a second height of a topmost surface of the first FeRAM stack.

9. The integrated chip structure of claim **1**, further comprising:

a first sidewall spacer arranged between the first FeRAM stack and the conductive contact;

a second sidewall spacer arranged between the second FeRAM stack and the conductive contact; and

a shared source region disposed within the substrate, wherein the shared source region continuously and laterally extends from below the first sidewall spacer to below the second sidewall spacer.

10. An integrated chip structure, comprising:

a first select gate and a second select gate disposed over a substrate;

a first ferroelectric random access memory (FeRAM) stack and a second FeRAM stack disposed over the substrate laterally between the first select gate and the second select gate;

a dielectric disposed over the substrate and laterally between the first FeRAM stack and the second FeRAM stack; and

a conductive contact extending through the dielectric, wherein the first select gate and the second select gate are separated from opposing sides of the conductive contact by first distances and wherein the first FeRAM stack and the second FeRAM stack are separated from opposing sides of the conductive contact by second distances that are smaller than the first distances.

11. The integrated chip structure of claim **10**, wherein the first distances between the opposing sides of the conductive contact and the first select gate and the second select gate are substantially equal.

12. The integrated chip structure of claim **10**, further comprising:

a first sidewall spacer arranged laterally between a first side of the first FeRAM stack and the first select gate, wherein the first sidewall spacer comprises one or more first dielectric layers; and

a second sidewall spacer arranged laterally between a second side of the first FeRAM stack and the conductive contact, wherein the second sidewall spacer comprises one or more second dielectric layers that are different than the one or more first dielectric layers.

13. The integrated chip structure of claim **12**, wherein the one or more first dielectric layers consist of a first number of dielectric layers and the one or more second dielectric layers consists of a second number of dielectric layers that is different than the first number of dielectric layers.

14. The integrated chip structure of claim **10**, wherein the first FeRAM stack comprises a ferroelectric material and a conductive material over the ferroelectric material.

15. The integrated chip structure of claim **10**, further comprising:

a transistor device disposed on the substrate; and

a boundary isolation structure extending into a trench within the substrate, wherein the boundary isolation structure comprises a first dummy structure arranged over a first upper surface of the boundary isolation structure and a second dummy structure arranged over a second upper surface of the boundary isolation structure.

16. The integrated chip structure of claim **15**, wherein the first upper surface is laterally between the second upper surface and the first FeRAM stack, the first upper surface being vertically above the second upper surface.

17. An integrated chip structure, comprising:

a select gate disposed over a substrate;

a ferroelectric random access memory (FeRAM) stack disposed over the substrate;

a first sidewall spacer comprising one or more first dielectric materials arranged laterally between a first side of the select gate and the FeRAM stack;

a second sidewall spacer comprising one or more second dielectric materials arranged along a second side of the select gate and laterally separated from the first sidewall spacer by the select gate; and

an interfacial dielectric layer continuously extending from directly between the select gate and the substrate to directly between the FeRAM stack and the substrate.

18. The integrated chip structure of claim **17**, wherein the FeRAM stack comprises a ferroelectric material, an etch stop layer over the ferroelectric material, and a conductive material over the ferroelectric material.

19. The integrated chip structure of claim **17**, wherein a thickness of the interfacial dielectric layer varies between opposing outermost sidewalls of the interfacial dielectric layer.

20. The integrated chip structure of claim **17**, wherein the interfacial dielectric layer continuously extends below the first sidewall spacer and the second sidewall spacer.

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