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Variable gain optical modulator with open collector driver amplifier and method of operation

Abstract

A distributed amplifier system comprising an impedance matching network configured to match an input impedance to an output impedance of the signal source, and a DC block configured to block DC components in the input signal. A variable gain amplifier adjusts the gain applied to the input signal based on a gain control signal to generate a gain adjusted signal. An emitter follower circuit receives and processes the gain adjusted signal to introduce gain peaking to create a modified signal. A distributed amplifier receives and amplifies the modified signal from the emitter follower circuit, to create an amplified signal. The distributed amplifier includes a termination network and one or more impedance matching elements configured for gain shaping the amplified signal. The gain peaking introduced by the emitter follower circuit is controlled by a variable current source. The distributed amplifier may be an open collector distributed amplifier.

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Background/Summary

1. FIELD OF THE INVENTION

(1) The innovation relates to driver circuits and in particular a distributed amplifier with associated circuitry.

2. RELATED ART

(2) Signal drivers may be used in numerous different types of systems such as, but not limited to, wireline communication systems, wireless communication systems, and optical systems, such as systems that utilize fiber optic cable as a signal medium. In numerous different environments of use, a signal must be driven or amplified as part of the transmit process.

(3) A distributed driver architecture is chosen to address bandwidth and return-loss limitations of an equivalent traditional lumped driver approach. A block diagram illustrating the differences between the lumped and distributed driver is shown in FIG. **1**.

(4) Most prior art distributed amplifiers include a pair of transmission lines with characteristic impedances of Z.sub.0 which connect the inputs and outputs of the amplifiers. An input signal is provided to the input path of the first device. As the input signal propagates down the input path, the signal is amplified, and the amplified output signal provided on the output path. The combination of FET capacitance with the high-impedance connection lines (input and output paths) resembles a lumped-element version of a fifty-ohm line.

(5) The bandwidth of the lumped driver, if only a single stage, is dictated by the termination resistance and the loading capacitance from the lumped stages. The loading capacitance can be quite substantial because of the large current required in the stage, which dictates the use of large transistor devices. This large capacitance, from the driver stage devices and the associated routing parasitics, will limit the bandwidth. Hence, the benefit of moving to a distributed approach is that the parasitic capacitance loading is now reduced or spread over the chosen number of stages. An example 4-stage distributed driver architecture is shown in FIGS. **1** and **2**, which are described below. The number of stages is chosen to meet gain, bandwidth, power, and complexity concerns. For this example, each of the four distributed stages would carry a quarter of the load current in the

equivalent lumped stage.

(6) The distributed driver incorporates artificial input and output inductor-capacitor (LC) transmission lines. The transmission line L and C components are chosen to meet both impedance and delay requirements, thereby minimizing reflections from impedance mismatch, and ensuring in-phase addition of the distributed output stages. The impedance requirement is defined in equation (1) and the delay is defined in equation (2). The L and C product, shown in equation (3), must also be chosen small enough so that the line approximates ideal behavior over the desired bandwidth.

(7) $Z = (L / C)^{1/2}$ (1) $\text{Tau} = (L * C)^{1/2}$ (2) $\text{CutoffFrequency} = 1 / (\quad * (L * C)^{1/2})$ (3)

(8) FIG. **1** illustrates a block diagram of an exemplary prior art distributed amplifier. A singled ended arrangement is shown. The laser or optical modulator driver **104** includes an input node **108** and an output node **112**. The input node **108** receives an outgoing electrical signal to be transmitted as an optic signal. In one embodiment, the input node receives data for high-speed transmission over the optic fiber. The output node **112** connects to a conductor, such as a trace, that provides the output signal to an optic signal generator.

(9) Connected to the input node **108** is an inductor **124**A and a first amplifier cell **120**A. A capacitance, shown as capacitor **132**, **136**, associated with each amplifier cell **120**A, is parasitic capacitance and is part of the first gain stage. This capacitance is inherently part of the amplifier cell, and not a separate physical capacitor, although it may be implemented with a physical capacitor. This arrangement repeats through one or more additional gain stages **120**B, **120**C, **120**D as shown. Four exemplary gain stages are shown in FIG. **1**, but in other embodiments a greater or lesser number of gain stages may be implemented subject to the target bandwidth and/or gain of the amplifier.

(10) As shown in FIG. **1**, the input of a first gain cell **120**A is connected to the input of a second gain cell **120**B through a first inductor **124**B or a transmission line, the input of the second gain cell **120**B is connected to the input of a third gain cell **120**C through a second inductor **124**C or a transmission line and so on through the fourth gain cell **120**D and inductor **124**D. The inductors may be actual elements, or inductance that is part of or built into, the conductive path. The input of the last gain cell **120**D is connected to a termination element **150** directly or through an inductor/transmission line **124**E as shown. The termination element **150** can be a resistor.

(11) The input node **108** of the first gain cell **120**A is connected to the output of a pre-driver directly (as shown) or through an inductor/transmission line. The output of the first gain cell **120**A is connected to the output of the second gain cell **120**B through another inductor **148**B or a transmission line, the output of the second gain cell **120**B is connected to the output of the third gain cell **120**C through another inductor **148**C or a transmission line. The output of the third gain cell **120**C is connected to the output of the fourth gain cell **120**D through another inductor **148**D or a transmission line. The output of the last gain cell **120**D is connected to output node **112** directly (as shown) or through an inductor/transmission line. The output node **112** connects to the optic signal generator, such as a laser or an optical modulator. In other embodiments, a greater or fewer number of amplifier (gain) cells may be implemented.

(12) The output of the first gain cell **120**A is connected to a termination element **140** directly (as shown) and/or through an inductor/transmission line **148**A. Termination resistors **140**, **150** are associated with the first gain cell (amplifier stage) **120**A output and the last gain cell (amplifier stage) **120**D input. In other embodiments, additional resistors may be placed in the driver circuit. The resistors **140**, **150** may be selected based on various design constraints and preferences such as power consumption, maximum operating frequency, input and output impedance, and the return losses. The resistance typically ranges from 20 ohms to 100 ohms but are driven and determined by system requirements. The signal propagates through the gain cells **120**A, **120**B, **120**C, **120**D towards the output node **112**.

(13) FIG. **2** illustrates an example embodiment of a distributed driver arranged in a differential pair configuration. In relation to FIG. **1**, similar elements are labeled with identical reference numbers. Elements previously described are not described again. In this embodiment, the distributed amplifiers are configured as a differential pair. A pair of FET devices **370**, **372** are arranged as shown with a current source **380** or path located below the FET device **370**. Although shown as FET devices, it is contemplated and disclosed that the devices may be heterojunction bipolar transistor, (HBT), FET, bipolar junction transistor (BJT), junction field effect transistor (JFET) or any other type of device or process. Operation of this circuit configuration is known in the art and not described herein. Parasitic capacitance **332**, **336** is also shown. More than one differential pair may be provided in each cell **320**. Additional differential pairs **380**B, **380**C, **380**D are also provided as shown.

(14) Additional inductors **324**A, **324**B, **324**C, **324**D, **324**E are provided and associated with the second leg of the differential pair along the input path at the bottom of FIG. **2**. Additional inductors **348**A, **348**B, **348**C, **348**D, **348**E are provided and associated with the second leg of the differential pair along the output path at the top of FIG. **2**. Similarly, termination resistors **340**, **350** are arranged as shown in the second leg of the differential pair. Resistor **340** is the termination resistor at the output, while resistor **350** is the termination resistor at the input. Operation and function are generally similar to the embodiment shown in FIG. **1**, with the differential signal provided on input nodes **108** and **308**. Output nodes **112** and **312** provide a differential signal to an optical modulator or a laser.

(15) These prior art designs suffered from several drawbacks. One drawback is limited output swing and excessive power consumption for a given output signal magnitude. Some prior art amplifiers were also excessively large. For output circuits with large output swings to drive the downstream modulator requires a large device area for the output stages. Due to the sizeable device, capacitance is then also high, which reduces bandwidth, as discussed above. The resulting circuit creates parasitic capacitance issues and loading causing it to be too slow, thus limiting bandwidth.

SUMMARY

(16) To overcome the drawbacks of the prior art and provide additional benefits, a distributed amplifier system is disclosed. In one embodiment, the distributed amplifier comprises an input configured to receive an input signal from a signal source and an impedance matching network configured to match an input impedance to an output impedance of the signal source. A DC block is provided and configured to block DC components in the input signal while a variable gain amplifier is configured to adjust the gain applied to the input signal based on a gain control signal to generate a gain adjusted signal. An emitter follower circuit is configured to receive and process the gain adjusted signal to introduce gain peaking to create a modified signal. A distributed amplifier is configured to receive the modified signal from the emitter follower circuit such that the distributed amplifier is configured to amplify the modified signal to create an amplified signal.

(17) This system may further comprise an emitter follower stage located between the DC block and the variable gain amplifier. In one embodiment, the distributed amplifier is configured as an open collector distributed amplifier. The distributed amplifier may also include a termination network and one or more impedance matching elements in the input path which are configured to perform gain shaping in the amplified signal. It is contemplated that the distributed amplifier may include two or more amplifier cells configured as cascode differential pair circuits. It is also contemplated that the input signal to the distributed amplifier system may be a differential input signal. The gain peaking introduced by the emitter follower circuit may be controlled by a variable current source. The distributed amplifier system may be part of an optic signal transmitter.

(18) Also disclosed is a method for processing and amplifying an input signal prior to transmission. In one embodiment, this method comprises impedance matching the input signal with an impedance matching network to reduce signal return loss, and then reducing or eliminating DC

signal components in the input signal with a DC block circuit. Thereafter, adjusting the gain applied to the input signal with a variable gain amplifier to create a modified input signal. Processing of the modified input signal with an emitter follower circuit to establish gain peaking into the modified input signal. Then, receiving and amplifying the modified input signal with gain peaking with a distributed amplifier to create an amplified signal.

(19) The distributed amplifier may be configured with an open collector. In addition, this method may further comprise performing impedance matching and gain peaking control with an emitter follower stage prior to adjusting the gain with the variable gain amplifier. In one embodiment, the DC block circuit comprises one or more capacitors. In addition, the amount of gain performed by the variable gain amplifier is based on a control signal provided to a variable current source. It is contemplated that the input signal may be a differential signal and the output signal may be a differential signal. In one configuration, the distributed amplifier includes two or more amplifier cells each configured as cascode differential pair circuits.

(20) Also disclosed is an optic signal transmitter with distributed amplifier comprising an input configured to receive an input signal from a data source. A driver and biasing module is part of the transmitter and includes one or more biasing circuits configured to generate one or more bias signals for the transmitter, an impedance matching network configured to match an input impedance of the transmitter to an output impedance of the data source, a variable gain amplifier configured to adjust a magnitude of the input signal based on a gain control signal to generate a gain adjusted signal, an emitter follower circuit configured to receive and process the gain adjusted signal to introduce gain peaking, and a distributed amplifier configured to receive and amplify the gain adjusted signal with gain peaking, from the emitter follower circuit, to create an amplified signal. The modulator and optic signal generator are configured to receive the amplified signal and convert the amplified signal to a modulated optic signal for transmission over an optic channel.

(21) The transmitter may further comprise a DC block connected to an output of the impedance matching network such that the DC block is configured to block DC components in the input signal. The distributed amplifier may be configured with an open collector. In one embodiment, the gain of the variable gain amplifier is based on a control signal provided to a variable current source. In one configuration, the distributed amplifier includes two or more amplifier cells each configured as cascode differential pair circuits.

(22) To overcome the drawbacks of the prior art and provide additional benefits, disclosed is a distributed amplifier for an optic signal generator. In one embodiment, the distributed amplifier comprises two or more amplifier cells such that each amplifier cell has one or more emitter follower circuits having an emitter follower input and an emitter follower output configured to perform frequency specific gain adjustment. The cells also include two or more amplifiers comprising in a cascode connected transistors configurated to amplify the received signal to create an amplified signal. An amplifier cell output is provided and configured to carry the amplified signal from the amplifier cell. Also part of the distributed amplifier is an input path and an output path. The input path is configured to receive and distribute the input signal to the two or more amplifier cells. The input path includes one or more inductors that cancel parasitic capacitance from the two or more amplifier cells. The output path connects to the amplifier cell output of the two or more amplifier cells to receive the amplified signal. The output path includes one or more inductors that cancel parasitic capacitance from the two or more amplifier cells.

(23) In one embodiment, an inductor from the input path and an inductor from the output path is associated with each amplifier cell. In one configuration, the combination of the amplifier parasitic capacitance and the inductors in the input path and the output path form a transmission line that tunes out the parasitic capacitance from the two or more amplifier cells. It is contemplated that the two or more amplifier cells may be configured in an open collector configuration. In one embodiment, the emitter follower circuit further comprises a variable current source configured to control the frequency specific gain adjustment. The distributed amplifier may further comprise a

termination network and gain shaping network, connected to or part of the input path, which is configured to perform gain shaping. In one configuration, the amplifier cell input comprises a first input and a second input such that the first and second inputs are configured to accept a differential signal, and the first input connects to a first emitter follower circuit and the second input connects to a second emitter follower circuit.

(24) Also disclosed is a method for amplifying, with a distributed amplifier, an input signal for use in an optic signal communication system. In one embodiment, this method comprises receiving the input signal such that the input signal to be transmitted on an optic fiber as an optic signal. Then, distributing the input signal to two or more emitter follower circuits over an input path having an inductance. The input path has an inductance that cancels a parasitic capacitance of the two or more amplifier cells. The two or more emitter follower circuits introduce frequency specific adjustment to the input signal for gain peaking, gain shaping, or both. Then, amplifying the input signal, after frequency specific adjustment, with two or more amplifier cells to generate amplified output signals. This method of operation combines the amplified output signals from the two or more amplifier cells on an output path as a combined output signal. The output path has an inductance that cancels a parasitic capacitance of the two or more amplifier cells. The combined output signal is presented on an output from the distributed amplifier such that the output connects to the output path.

(25) In one embodiment, an inductor from the input path and an inductor from the output path is associated with each amplifier cell, and the inductors are realized as integrated transmission line elements. The combination of the amplifier parasitic capacitance and the inductors in the input path and the output path form a transmission line that tunes out the parasitic capacitance from the two or more amplifier cells. It is contemplated that the two or more amplifier cells may be configured in an open collector configuration. The emitter follower circuit may include a variable current source configured to control the frequency specific gain control. In addition, this method may further comprise providing a control signal to a variable current source that is part of the emitter follower circuit. The control signal determines the amount of frequency specific gain adjustment. In one embodiment, the two or more amplifier cells further comprise a first input and a second input, the first and second inputs are configured to accept a differential signal, and the first input connects to a first emitter follower circuit and the second input connects to a second emitter follower circuit.

(26) Also disclosed is a distributed driver for an optic signal generator. The driver may comprise a driver input configured to receive an input signal and an output configured to provide an output signal to the optic signal generator or modulator. This embodiment also includes a first amplifier cell comprising a first amplifier cell input, one or more emitter follower circuits, one or more amplifiers, and a first amplifier cell output. The first amplifier cell is configured to receive and amplify the input signal to create a first amplified signal on the first amplifier cell output. A second amplifier cell is provided and comprises a second amplifier cell input, one or more emitter follower circuits, one or more amplifiers, and a second amplifier cell output. The second amplifier cell configured to receive and amplify the input signal to create a second amplified signal on the second amplifier cell output. A first conductive path is provided which connects the driver input to the first amplifier cell input and the second amplifier cell input. The first conductive path carries the input signal to the first amplifier cell and the second amplifier cell such that an inductance of the first conductive path counteracts a capacitance associated with the first and second amplifier cells. Also part of this embodiment is a second conductive path connecting the driver output to the first and second amplifier cell outputs. The second conductive path carries the first amplified signal and the second amplifier signal to the driver output, such that an inductance of the second conductive path counteracts the capacitance associated with the first amplifier cell and the second amplifier cell.

(27) In one embodiment, the one or more amplifiers are configured as a cascode connected differential pair. In addition, the distributed driver may further comprise additional amplifiers cells having a configuration that is the same as the first and second amplifier cells. It is contemplated

that the first and second amplifier cell may have an open collector configuration. The one or more emitter follower circuits may further comprise a variable current source configured to control a frequency specific gain adjustment. In addition, the distributed driver may further comprise a termination network and gain shaping network, connected to or part of the first conductive path, that is configured to perform frequency specific gain shaping.

(28) To overcome the drawbacks of the prior art and provide additional advantages, a distributed amplifier with variable gain control stage is disclosed. In one embodiment, this distributed amplifier with variable gain control stage comprises a variable gain amplifier comprising a signal input configured to receive a data signal and a gain control input configured to receive a gain control signal. A gain controlled amplifier is configured to receive the data signal and the gain control signal to create a gain adjusted signal, such that an amount gain adjustment is determined by the gain control signal. Also part of this embodiment is one or more gain peaking control elements, connected to the gain controlled amplifier, that are configured to establish gain peaking in the gain adjusted signal. A variable gain control stage output is configured to provide the gain adjusted signal from the one or more gain peaking control elements to the distributed amplifier. Furthermore, two or more amplifier cells are provided such that each amplifier cell comprises an amplifier cell input configured to receive the gain adjusted signal, two or more amplifiers, connected in a cascode configuration, to amplify the gain adjusted signal to create an amplified signal, and an amplifier cell output configured to carry the amplified signal. Also provided are an input path and an output path. The input path receives the input signal and distributes the input signal to the two or more amplifier cells. The input path includes one or more inductors that cancel input parasitic capacitance from the two or more amplifier cells. The output path connects to the amplifier cell output of the two or more amplifier cells to receive the amplified signal. The output path including one or more inductors that cancel output parasitic capacitance from the two or more amplifier cells.

(29) In one embodiment, the one or more gain peaking control elements comprise inductors. The distributed amplifier may further comprise one or more emitter follower circuits having an emitter follower input connected to the input path and an emitter follower output connected to the amplifier cell input. The one or more emitter follower circuits are configured to perform frequency specific gain adjustment in the amplified signal created by the one or more amplifier cells. In one configuration, an inductor from the input path and an inductor from the output path are associated with each amplifier cell. It is contemplated that the distributed driver may further comprise a degeneration network connected to the gain controlled amplifier such that the degeneration network is configured to adjust low frequency gain. The variable gain amplifier may further comprise one or more termination resistors configured to establish the gain of the gain controlled amplifier and set the output impedance of the variable gain amplifier. In one embodiment, the two or more amplifier cells are configured in an open collector configuration. The emitter follower circuit may further comprise a variable current source configured to control the frequency specific gain adjustment.

(30) Also disclosed is a distributed amplifier with variable gain control comprising a gain control circuit that includes a gain control circuit input, a gain control circuit output, one or more gain control amplifiers, and one or more gain peaking control elements located between the variable gain amplifier and the output. An amount gain adjustment is determined by the gain control signal which is received on a gain control signal input of the gain control circuit which causes the gain control circuit to generate a gain adjusted signal. The distributed amplifier comprises an input path configured to receive and distribute the input signal to two or more amplifier cells. The input path includes one or more inductors that cancel input parasitic capacitance from the two or more amplifier cells. Two or more amplifier cells are provided and configured with amplifiers in a cascode configuration to amplify the received signal to create the amplified signal. An output path is connected to the amplifier cell output of the two or more amplifier cells to receive the amplified signal. The output path includes one or more inductors that cancel output parasitic capacitance

from the two or more amplifier cells.
(31) In one embodiment, the gain peaking control elements comprise inductors. The distributed amplifier may further comprise a termination load connected between the gain peaking control elements and the gain control circuit output. In one configuration, the distributed amplifier further comprises one or more emitter follower circuits, associated with each amplifier cell, that are located between the input path and the two or more amplifier cells, wherein the emitter follower circuits are configured to perform frequency specific gain adjustment in the amplified signal. It is contemplated that the emitter follower circuit may further comprise a variable current source configured to control the frequency specific gain adjustment. It is contemplated that the gain control circuit may further comprise a degeneration network connected to the gain control amplifier such that the degeneration network is configured to adjust low frequency gain. In one embodiment, the two or more amplifier cells are configured in an open collector configuration.
(32) Also disclosed is a method for creating an amplified signal with frequency specific magnitude adjustment. In one embodiment, this method includes receiving the input signal, which is a signal to be transmitted on an optic fiber as an optic signal, and then adjusting gain applied to the input signal with a variable gain amplifier, based on a control gain signal. This creates a gain adjusted signal, such that adjusting the gain includes introducing frequency specific magnitude adjustment to the input signal for gain peaking, gain shaping, or both. Then, receiving the gain adjusted signal on an amplifier input path, the amplifier input path having an inductance that cancels input parasitic capacitance of two or more amplifier cells. The input signal is amplified after frequency specific magnitude adjustment with the two or more amplifier cells, and the amplified output signals from the two or more amplifier cells are combined on an output path as a combined output signal. The output path has an inductance that cancels output parasitic capacitance of the two or more amplifier cells. The combined output signal is then presented on an output.
(33) In one embodiment, an inductor from the input path and an inductor from the output path are associated with each amplifier cell, and the inductors are realized as integrated transmission line elements. The two or more amplifier cells may be configured in an open collector configuration. It is contemplated that this method further includes introducing frequency specific gain control with an emitter follower circuit that is associated with at least one of the two or more amplifier cells, such that the emitter follower circuit including a variable current source configured to control an amount of frequency specific gain control. The two or more amplifier cells may further comprise a first input and a second input. The first and second inputs are configured to accept a differential signal, and the first input connects to a first emitter follower circuit and the second input connects to a second emitter follower circuit.
(34) Also disclosed is a distributed driver for an optic signal generator comprising a driver input configured to receive an input signal and a driver output configured to provide an amplified output signal to the optic signal generator or modulator. Also disclosed is a first amplifier cell comprising a first amplifier cell input, one or more amplifiers, and a first amplifier cell output. The first amplifier cell is configured to receive and amplify the input signal to create a first amplified signal on the first amplifier cell output. A second amplifier cell comprises a second amplifier cell input, one or more amplifiers, and a second amplifier cell output. The second amplifier cell is configured to receive and amplify the input signal to create a second amplified signal on the second amplifier cell output. A first conductive path has a first end and a second end, and the first end is connected to the driver input. The first conductive path connects the driver input to the first and the second amplifier cell inputs, to thereby carry the input signal to the first and second amplifier cells. In addition, one or more inductances in the first conductive path counteracts a capacitance associated with the first amplifier cell and the second amplifier cell. A gain shaping termination network is connected to, or part of, the second end of the first conductive path and is configured to perform frequency specific gain shaping. A second conductive path is also provided such that the second conductive path connects the driver output to the first amplifier cell output and the second amplifier

cell output, to thereby carry the amplified output signal created by the first amplifier cell and the second amplifier cell to the driver output. In addition, one or more inductances in the second conductive path counteracts a capacitance associated with the first amplifier cell and the second amplifier cell.

(35) The one or more amplifiers may be configured as a cascode differential pair. The distributed driver may further comprise additional amplifier cells having the same configuration as the first and second amplifier cells. The distributed driver of claim **1** wherein the first and second amplifier cells have an open collector configuration. It is contemplated that the distributed driver may further comprise one or more emitter follower circuits connected between the first conductive path and the first amplifier cell input, and one or more emitter follower circuits connected between the first conductive path and the second amplifier cell input.

(36) The emitter follower circuits may further comprise one or more variable current sources, within each emitter follower circuit, that are configured to control a frequency specific gain adjustment performed by the one or more emitter follower circuits. The gain shaping termination network may comprise one or more inductors and one or more resistors. In one embodiment, the gain shaping termination network comprises one or more inductors, one or more resistors, and one or more capacitors connected in series between a ground and an inductor in the input path.

(37) Also disclosed is a method for amplifying, with a distributed amplifier, an input signal. In one configuration, this method comprises receiving the input signal on an input path, the input path having a first end and a second end, such that the first end receives the input signal, and the second end is terminated with a gain shaping termination network. The input path further comprises one or more inductors. This method also distributes the input signal to two or more amplifier cells through the input path that has one or more inductors and a termination network. The step of distributing includes introducing frequency specific gain shaping into the input signal with the gain shaping termination network, canceling parasitic capacitance associated with two or more amplifiers, in the distributed amplifier, with the one or more inductors, amplifying the input signal after frequency specific gain adjustment with the two or more amplifier cells to generate amplified output signals, combining the amplified output signals from the two or more amplifier cells on an output path as a combined output signal, the output path having one or more inductors that cancel output parasitic capacitance of the two or more amplifier cells, and presenting the combined output signal on an output from the distributed amplifier, the output connected to the output path.

(38) In one embodiment, the gain shaping termination network consists of one or more resistors, one or more inductors and one or more capacitors, and the gain shaping termination network is located at an end of the input path that is opposite an end of the input path that receives the input signal. In one configuration, an inductor from the input path and an inductor from the output path is associated with each amplifier cell, and the inductors are realized as integrated transmission line elements. The gain shaping termination network may comprise series connected inductors, resistors, and capacitors, which connect to an inductor in the input path. In one embodiment, the two or more amplifier cells are configured in an open collector configuration. This method of operation may further comprise performing additional frequency specific gain adjustment with one or more emitter follower circuits in at least one of the two or more amplifier cells.

(39) The distributed driver may further comprise providing a control signal to a variable current source that is part of the at least one emitter follower circuit, such that the control signal determines the amount of frequency specific gain adjustment introduced by the at least one emitter follower circuit. The distributed amplifier may be configured to accept and amplify a differential signal and the input signal is a differential signal.

(40) Also disclosed is a distributed amplifier for an optic signal generator comprising two or more amplifier cells, each cell having two or more amplifiers that include cascode connected transistors, configured to amplify a received signal to then create an amplified signal, and an output port configured to carry the amplified signal. Also provided is an input path which has a first end and a

second end. The input path is configured to receive the input signal at the first end and distribute the input signal to the two or more amplifier cells. The input path includes one or more inductors that cancel parasitic capacitance from the two or more amplifier cells. An output path connects to the amplifier cell output of the two or more amplifier cells to receive and output the amplified signal from two or more amplifier cells, the output path including one or more inductors that cancel parasitic capacitance from the two or more amplifier cells. Also part of this embodiment is a gain shaping network at the second end of the input path, the gain shaping network configured to introduce frequency specific gain shaping in the amplified signal from two or more amplifier cells.
(41) An inductor from the input path and an inductor from the output path may be associated with each amplifier cell. In one embodiment, the gain shaping network comprises series connected inductors, resistors, and capacitors, which connect to an inductor in the input path. The distributed amplifier may be configured to amplify a differential signal, the input path comprises a first input path and a second input path, and the first input path and the second input path connect through one or more resistor at the second end.
(42) Other systems, methods, features, and advantages of the invention will be or will become apparent to one with skill in the art upon examination of the following figures and detailed description. It is intended that all such additional systems, methods, features, and advantages be included within this description, be within the scope of the invention, and be protected by the accompanying claims.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
(1) The components in the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention. In the figures, like reference numerals designate corresponding parts throughout the different views.
(2) FIG. **1** illustrates a block diagram of an exemplary prior art distributed amplifier.
(3) FIG. **2** illustrates an example embodiment of a distributed driver arranged in a differential pair configuration.
(4) FIG. **3**A illustrates an exemplary optic fiber communication link.
(5) FIG. **3**B illustrates an example environment of use of the distributed driver disclosed herein.
(6) FIG. **4** illustrates a block diagram of an example embodiment of a distributed driver amplifier output stage with associated circuitry.
(7) FIG. **5** illustrates a block diagram of an example embodiment of a distributed amplifier output stage.
(8) FIG. **6** illustrates an exemplary emitter follower (EF) stage and an exemplary cascode differential pair output stage.
(9) FIG. **7** illustrates a block diagram of the exemplary amplifier circuit.
(10) FIG. **8** illustrates a block diagram of an example embodiment of a termination network with gain shaping.
(11) FIG. **9** illustrates an exemplary circuit diagram of a termination network with gain shaping.
(12) FIG. **10** illustrates a block diagram of an example embodiment of a variable gain amplifier (VGA).
(13) FIG. **11** illustrates a circuit diagram of an example embodiment of a variable gain amplifier (VGA).
(14) FIG. **12**A and FIG. **12**B illustrate exemplary signal plots showing the improvements of the disclosed system over prior art designs.
DETAILED DESCRIPTION
(15) One example environment of use of the innovation disclosed herein is in an optical

communication system that utilizes optical fiber links and lasers/LED or some other form of optic signal generator (light source). FIG. **3**A illustrates an exemplary optic fiber communication link. To enable communication between remote networking equipment **304**A, **304**B, a fiber optic transmitter **308** and receiver **328** are provided. Driver amplifier **312**, which is part of a transmitter **308**, drives the modulator **314**. The modulator **314** also receives an optic signal, from a laser **316** as shown. The output of the modulator **314** is a modulated optic signal which is coupled to the fiber **320** for signal transmission. Other embodiments may not include the modulator **314**, such as direct drive system which connects the driver directly to the laser **316**.

(16) At the receiving side of the optical fiber link is a receiver **328**. The receiver **328** includes a photodiode (photodetector) **332** and one or more amplifiers (although only one amplifier is shown to simplify FIG. **3**A). The amplifier **336** may be a TIA or any other type of amplifier or amplifiers. As used herein, the term amplifier means one or more amplifiers. Optical energy is converted into an electrical signal by the photodiode **332** and processed further by the one or more amplifiers **336** to set the signal magnitude to a level suitable for further processing. It is contemplated that the innovation disclosed herein may be used in other environments of use than that shown in FIG. **3**A and FIG. **3**B.

(17) FIG. **3**B illustrates an example environment of use of the distributed driver disclosed herein. This is but one possible embodiment, and it is contemplated and understood that the innovation disclosed herein may be used in other environments than disclosed below. As shown, an exemplary optic signal transmitter **354** includes a data source **358** that provides data for transmission as an optic signal. The data source **358** may be another system or device, either on chip or off chip, or a memory. The data source **358** provides the data to a driver and biasing module **362** that is part of the transmitter **354**. The driver and biasing module **362** prepare the data for transmission to a level suitable for downstream processing. The output of the driver and biasing module **362** connects to a modulator and optic signal generator **366**. The modulator and optic signal generator **366** are configured to generate a modulated optic signal for transmission over an optic channel **370**. In other embodiment, wireline or wireless transmission may occur. In this embodiment, the driver and biasing module **362** is configured as a distributed driver, as described herein, with optional distributed biasing associated with each amplifier cell.

(18) Optical signal generators that may be used with the driver disclosed herein are direct modulated lasers (DMLs), EMLs (Electroabsorptive Modulated Lasers), VCSELs (Vertical Cavity Surface Emitting Lasers), LEDs (Light Emitting diodes), PICs (photonic integrated circuits) and other optical modulators such as, but not limited to, Mach-Zehnder modulator or ring modulator. The generated optic signal is provided to a fiber optic cable **370**, which carries the optic signal to a remotely located receiver **374**.

(19) FIG. **4** illustrates a block diagram of an example embodiment of a distributed driver amplifier output stage with associated circuitry. This is but one possible example embodiment and other configurations are possible. In this embodiment differential inputs **404**, carrying differential signals, connect to an input matching network **408**. The input matching network **408** is configured to impedance match with an upstream source or stage to maximize power transfer by reducing unwanted reflections. The input matching network **408** may comprise an inductor-capacitor network with distributed elements, although in other embodiments other circuit arrangements may be used which may include resistor, capacitors, inductors, or any combination of passive or active elements. The input matching network **408** or the impedance matching elements of FIG. **5**, may be configured in whole or in part as a transmission line with passive elements that change in size (length and/or width) based on position within the transmission line.

(20) The output of the input matching network **408** connects to a DC blocking circuit **412**. The DC blocking circuit **412** is configured to prevent unwanted DC signal components from subsequent stages. The DC blocking circuit **412** may comprise series connected capacitors or an RC network, although in other embodiments other circuit arrangements may be used.

(21) The output of the DC blocking circuit **412** connects to an optional emitter follower stage **416**. The optional emitter follower stage **416** is configured to transform the impedance between the DC block output and a subsequent element, such as VGA stage **420**. The emitter follower stage **416** may comprise any type of emitter follower stage design, with one example being shown in FIG. **6**. Other embodiments, other circuit arrangements may be used. The emitter follower stage **416** is also configured to provide peaking (gain) control. The emitter follower stage **416** should be considered optional and should not be confused with the emitter follower circuits that are part of the distributed amplifier **424**.

(22) The output of the emitter follower stage **416** connects to a variable gain amplifier (VGA) **420**. The VGA **420** is configured to provide variable gain control to the system of FIG. **4**. The VGA **420** may comprise any type of VGA design with one novel design as shown in FIG. **10** and FIG. **11**, although in other embodiments other circuit arrangements may be used.

(23) The output of the VGA **420** connects to a distributed amplifier output stage **424**. The output stage **424** is configured to amplify the signal to a level suitable for downstream elements, such as to drive an optic signal generator. The output stage **424** may comprise any type multiple stage distributed amplifier, although in other embodiments or other circuit arrangements may be used. At the front end of the distributed amplifier output stage **424** are emitter follower circuits which improve bandwidth by reducing capacitance and allows for gain peaking, such as for example at high frequencies. The output from the distributed amplifier output stage **424** may be provided to a modulator or a laser, in a direct driver configuration. FIG. **6** provides an example embodiment of a distributed amplifier output stage **424** with emitter follower circuits **422**.

(24) FIG. **5** illustrates a block diagram of an example embodiment of a distributed amplifier output stage (DAOS) shown as element **424** in FIG. **4**. This is but one possible configuration for a DAOS and as such, other embodiments are contemplated. As shown in FIG. **5**, the differential inputs **504**A, **504**B (collectively **504**) are provided to inductor elements **508**A, **508**B. The inductor elements **508**A, **508**B may comprise any type of device or circuit. This may include inductors, or a transmission line element configured to behave as inductor.

(25) The output of the inductor elements **508**A, **508**B connect to amplifiers (gain cells) **512**A, **512**B, **512**C, **512**D as shown and to subsequent inductor elements **508**A, **508**B along the input lines. The amplifiers **512**A, **512**B amplify the signals from the inductor elements **508**A, **508**B to generate amplified signals suitable for driving a downstream element, such as an optic signal generator or modulator, such as for driving the signal over a transmission line. The amplifiers **512**A, **512**B, **512**C, **512**D may comprise any type of amplifier, such as but not limited to, an emitter follower combined with a cascode differential pair. The amplifiers **512** may be configured as shown in FIG. **6** and include the emitter follower circuits.

(26) The input line extends to include additional input line inductor elements **508**A, **508**B and associated amplifiers **512**A, **512**B, . . . as shown. Any number of input line inductor elements **508**A, **508**B and associated amplifiers **512**A, **512**B, . . . may be provided based on the number of amplification stages. Each of the input line inductor elements **508**A, **508**B may be the same, such as in length and width, or different sizes/dimensions. In one embodiment, the input line inductor elements **508**A, **508**B become smaller as the input line progresses. The inductor elements **508**A, **508**B may be inductors configured as transmission line elements.

(27) At the end of the input line is a termination network **524** including one or more termination elements **528**. The termination network **524** is configured to establish and improve gain shaping to counter any frequency based attenuation in the signal, such as in the high frequency range. FIG. **8** and FIG. **9**, and the associated description, illustrate exemplary termination networks in greater detail.

(28) The output of the amplifiers **512**A, **512**B provide the amplified signal to an output line having output line inductor elements **520**A, **520**B. The output line inductor elements **520**A, **520**B are configured to cancel capacitances in each amplifier cell **512**A, **512**B, . . . or any other unwanted

capacitance in the distributed amplifier. Any number of output line inductor elements **520**A, **520**B may be provided based on the number of amplification stages. Each of the output line inductor elements **520**A, **520**B may be the same, such as in length and width, or different. In one embodiment, the output line inductor elements **520**A, **520**B become smaller as the output line progresses. Providing multiple amplifier stages **512** distributes the capacitance associated with each amplifier to establish multiple small capacitances along the distributed amplifier. The inductor elements **508**, **520** are selected and sided to cancel or counteract the capacitance associated with each amplifier stage.

(29) The differential signal outputs **532**A, **532**B are located at the end of each output line as shown to provide the signal to downstream elements. It is contemplated that this embodiment could be implemented in a single ended (non-differential configuration). To aid in understanding, the letters A, B, C, & D are shown within circles in FIG. **5** to correspond to circuit locations in FIG. **6** to identify related connection points. Also differing from the embodiment of FIG. **2** is the open collector configuration of FIG. **5**, which omits the resistors **140**, **340** and associated connections as shown in FIG. **2**.

(30) FIG. **6** illustrates an exemplary distributed amplifier and emitter follower (EF) stage, as referenced in element **424**, **422** of FIG. **4**, and as element **512** in FIG. **5**. This is but one possible configuration for a distributed amplifier with EF stage and as such, other embodiments are contemplated. As shown in FIG. **6**, inputs **604**, **606** are configured to receive incoming differential signals from the VGA stage. The input **604**, which receives in the In1 signal, connects to a base of a transistor **612**A configured as a first emitter follower stage **614**. A collector of the transistor **612** connects to a supply voltage, such as VCC **620**. The emitter of the transistor **612** connects to a current source **624** which also connects to ground. The current source **624**A, **624**B is configured to be a tunable current source for gain peaking control purposes.

(31) A second emitter follower **614**B is configured generally similar to, or the same as, the first emitter follower **614**A and as such is not described in detail. For example, an In2 signal connects to input **606**. As can be seen elements **612**B, **620**B, **624**B are provided in a similar or same arrangement.

(32) Between the two emitter follower stages is a cascode differential pair **640**. The emitter terminals of transistor **612**A connects to a base terminal of transistor **644**A. Transistor is arranged as cascoded with transistor **650**A such that the collector terminal of transistor **644**A connects to the emitter terminal of transistor **650**A. The collector terminal of transistor **650**A connects to a first output terminal **654**A. Also provided are transistors **644**B, **650**B which are arranged in a similar or same configuration as transistors **644**A, **650**A to form a cascode differential pair **640**. The transistor **650**A, **650**B are arranged in an open collector output. As a result, in this example embodiment, the collector terminals are not terminated on the chip or integrated circuit, but instead directly connect to a modulator or a subsequent device. This is in contrast to the prior art which provides a termination resistor between the outputs **654**A, **654**B. Output power is lost in the prior art termination resistor, so the proposed design is more power efficient resulting in better performance.

(33) Also part of, or associated with, the cascode differential pair **640** is a common mode shunt to ground capacitors **660** that is connected between the base terminals of transistors **650**A, **650**B. The ground shunt **660** is configured to function as a virtual ground to shunt AC signals to ground. To ensure stability during differential mode operation (as is configured), the shunt to ground through each capacitor is established.

(34) Connected to the emitter terminals of transistors **644**A, **644**B is a degeneration network **664**, which in turn connects to a current tail source **668**. The degeneration network **664** is configured to allow for control of gain as a function of frequency, such as a DC gain control which in turn improves linearity. The DC gain response or behavior is dominated by the resistor values in the degeneration network **664**, while the capacitor in the degeneration network is selected to control AC gain. Other configurations of the degeneration network **664** are contemplated other than the

series connected resistors and parallel connected capacitor as shown. In addition, the combination of the capacitor and resistors provide gain peaking such that at higher frequencies the gain goes up, which is preferred. Absent the capacitor, the gain at high frequencies will roll off faster, which will detrimentally affect circuit performance.

(35) Also part of this embodiment are one or more variable current sources **624**A, **624**B configured to bias the emitter follower stages **614**, **616**, as well as other associated elements. The variable current sources also assist with or control the gain peaking and/or gain shaping such that increasing the current source output increases gain. The variable current source will receive a control signal input to control its output current. In addition, emitter follower (EF) circuits provide a better impedance looking into the EF circuit than if directly connected to the cascode differential pair **640**, which improves impedance matching. The resistors are implemented in HBT (heterojunction bipolar transistor) technology, but also could be implemented in BJT, FET devices, such as silicon (Si), silicon carbide (SiC), silicon germanium (SiGe), aluminum phosphide, aluminum arsenide, gallium arsenide, gallium nitride, indium phosphide, and all families of III-V and II-VI semiconductor materials for structural support, or any other process or material. The outputs **654**A, **654**B of the differential pair **640** are the outputs of the distributed amplifier **424** in FIG. **4**, or the output nodes C & D as shown in FIG. **5** and FIG. **6**.

(36) The configuration of FIG. **6** provides a benefit over the prior art by configuring the cascode differential pair **640** with the emitter follower stage **614**A, **614**B on each side of the differential pair. Unlike the prior art where an emitter follower stage is paired with a VGA, in this embodiment the emitter follower stage is paired with the output gain cell creating a novel combination. This configuration provides several benefits. One such benefit is that this arrangement improves bandwidth because looking into the first device, there is a series capacitance which may appear as two capacitances in series. As a result, the overall capacitance is reduced by placing the emitter follower stage in the distributed output stage instead of the VGA, which in turn increases bandwidth. An additional benefit of this configuration is the added flexibility to tune the gain peaking to a higher frequency than would otherwise be difficult in a prior art configuration. Gain peaking is tuned by adjusting the current output of the variable current sources **624**B.

(37) In operation, the circuit of FIG. **6** is configured such that the emitter follower circuits are used as gain peaking elements that establish an increase in gain or a decrease in gain at particular frequencies, such as for example, higher frequencies. The amount of gain peaking is controlled by the variable current source **624**B. A control signal, from or controlled by a current mirror, is provided to the variable current source to control its current. The control signal may be provided by a digital circuit/signal based on a reference current or some other control values. The value of the control signal may be set by the user with a digital interface, by an analog signal, or feedback. In one embodiment, the DC voltage at each stage may be for example, 2.2 volts and/or 1.3 volts. The emitter follower circuits are also used for impedance matching. The gain peaking control improves bandwidth.

(38) The emitter follower circuits also present a better impedance than looking into the cascode differential pair, particularly as to capacitance. The capacitance will be less than if looking directly into the cascode differential pair, which in turn provides increased bandwidth.

(39) FIG. **7** illustrates a block diagram of the exemplary amplifier circuit shown in FIG. **6** and as would correspond to the amplifier output stage **424** of FIG. **4**. In this simplified block diagram, inputs **708**A, **708**B are configured to receive a differential input signal. The input signals are provided to emitter follower circuits **712**A, **712**B which are configured to transform or match the impedance between the proceeding and subsequent elements or stages and provide for gain shaping/peaking. The output of the emitter follower circuits **712**A, **712**B feed into an amplifier **716**, which in this embodiment is a cascode differential pair circuit. In other embodiments, other types of amplifier circuits may be used including, but not limited to, a single ended amplifier, differential pair, or a differential cascode amplifier with RC degeneration. Stated another way, given the

following elements: 1) Differential amplifier, 2) cascode differential pair, and 3) RC degeneration, the contemplated combination could be elements 1 or elements 1+3 or elements 1+2, or single ended configuration such that only one signal output is used (which avoids the use of element **712**B. The amplifier **716** is configured to amplify the receive signals and generate a differential signal output on outputs **730**A, **730**B. In this embodiment, the amplifier **716** includes a degeneration network **724** and a virtual ground node circuit **720**, as are described above in connection with FIG. **6**.

(40) FIG. **8** illustrates a block diagram of an example embodiment of a termination network with gain shaping. This is but one possible example embodiment and as such, other embodiments are contemplated. In this embodiment, the transmission line **804**A, **804**B, as shown in FIG. **5**, include an impedance matching element **808**A, **808**B. A gain shaping network **812**A, **812**B connects to the impedance matching elements (transmission line inductor) **808**A, **808**B via the conductive path. The impedance matching networks **804**A, **804**B also connects to a termination network **820**. In some embodiments, the matching network elements **804**A, **804**B may be considered as part of the gain shaping network **812**A, **812**B or work in connection with the gain shaping network such that the values of all the elements may be adjusted to achieve the desired gain shaping.

(41) In this embodiment, the gain shaping network connects not at an end terminal **824** of the impedance matching networks **804**A, but instead at location **830** that is between the input and output **824** of the impedance matching networks **804**A. This provides the benefit of improved gain shaping. By moving the connection point **830** or tap in point along the impedance matching element **808**A, the gain shaping can be adjusted for frequency, intensity, or both. This can be used to establish a more linear frequency response or supplement gain at frequencies which may otherwise be attenuated. The gain shaping network **812**A, **812**B may comprise any combination of resistors, inductors, and/or capacitors arranged to gain shape. The termination network may comprise active or passive elements, such as resistors, capacitors, or inductors configured to control as power consumption, maximum operating frequency, and input and output impedance. The resistance typically ranges from 20 ohms to 100 ohms but are driven and determined by system requirements. In one embodiment, the impedance matching element **808**A, **808**B is an inductor(s), which may be configured as an integrated transmission line element.

(42) FIG. **9** illustrates an exemplary circuit diagram of a termination network with gain shaping. This is but one possible example embodiment and as such other embodiments are contemplated. In this embodiment, the transmission line **904**A, **904**B, as shown in FIG. **5**, include an impedance matching element **908**A, **908**B. A gain shaping network **912**A, **912**B connects to the impedance matching elements **908**A, **908**B via the transmission line conductive path. The impedance matching networks **912**A, **912**B also connect to a termination network **916**, that comprises one or more termination resistors **920**A, **920**B configured to provide a termination resistance and for impedance matching/balancing. The inductor **930**A, **930**B may connect to the midpoint or at any point between the start and end of the transmission line inductors **950**A, **950**B such as shown in FIG. **8**. The connection may occur between the inductor end terminals.

(43) In this example embodiment, the gain shaping network comprises an inductor **930**A in series with a resistor **934**A in series with a capacitor **938**A. The capacitor connects to a ground node Vss **942**. Selection of the values for the inductor **930**A, resistor **934**A, and capacitor **938**A control the frequency affected by the gain shaping and its magnitude. The gain shaping overcomes the challenges associated with optical network modulator, which has a gain profile that dips at certain frequencies, typically high frequencies. Using the gain shaping associated with the termination network can be used to increase the gain at the frequencies that are otherwise attenuated by the optical network modulator.

(44) FIG. **10** illustrates a block diagram of an example embodiment of a variable gain amplifier (VGA). This is but one possible embodiment and as such, other configurations are possible. In this embodiment of the VGA **1004**, inputs **1008**A, **1008**B are configured to receive the differential

signal as inputs. The inputs **1008**A, **1008**B connect to a cascode VGA **1012**. The cascode VGA is configured to amplify the received signal.

(45) The output of the cascode VGA **1012** connects to gain peaking control elements **1016** to adjust or control gain peaking. As discussed herein, gain peaking is beneficial to provide additional gain for specific frequencies, which may otherwise be attenuated by the system or channel. The gain peaking control elements **1016** may comprise any type elements or structure configured to increase or decrease gain in one or more frequency bands. The output of the gain peaking control elements **1016** connect to a termination load **1020**. The termination load **1020** is configured to set the gain of the VGA and to provide matching with the output stage of the distributed amplifier. In one embodiment, the termination load comprises a combination of resistors and inductors selected to increase gain at a high frequency.

(46) The termination load **1020** is biased from a bias signal source **1024**, which may be any bias signal source, such as one or more bias circuits, configured to bias the VGA system **1004**. The termination load **1020** also connects to output path gain peaking elements **1030**. The output path gain peaking elements **1030** may comprise active elements, passive elements, or a combination of both active and passive elements configured to establish or control gain and certain frequencies.

(47) The outputs **1044**A, **1044**B are on the opposing side of the output path gain peaking elements **1030** as shown and are configured to output the differential signal. The outputs **1044**A, **1044**B of the VGA **1004** may connect to the distributed amplifier output stage.

(48) Also shown in FIG. **10** is a second bias source **1038** configured to provide a bias signal to the VGA **1004** as shown. The second bias source **1038** connects to a degeneration network **1034**, which in turn connects to the cascode VGA **1012**. The degeneration network **1034** may comprise one or more active elements, passive elements, or a combination of active and passive elements. The degeneration network **1034** is configured to control or adjust low frequency gain, such as a DC gain control which in turn improves linearity.

(49) FIG. **11** illustrates a circuit diagram of an example embodiment of a variable gain amplifier (VGA) as shown by element **420** in FIG. **4**. This is but one possible circuit level configuration and one of ordinary skill in the art may develop other embodiments which do not depart from the claims. In this embodiment, at the bottom of FIG. **11** is a bias signal input **1108** which is provided to a common mode rejection element **1112**, which in this embodiment is an inductor. The bias signal may be provided by a current source (not shown) or any other type of bias signal source. The benefit gained through use of the common mode rejection elements **1112** rejects the common mode signal. When the signal on the + and − inputs are in phase, the common mode rejection elements **1112** will reject those common mode signal components. Common mode signal components can appear from noise in the signal or noise in the supply voltage.

(50) An additional bias signal node **1116** is provided at the top of the circuit shown in FIG. **11**. The bias signal node **1116** connects a voltage regulator to obtain a bias voltage and to termination resistors **1120**A, **1120**B. Instead of the open collector configuration as shown in FIG. **6**, this embodiment includes termination resistors **1120**A, **1120**B, which may also be referred to as load or load resistors. The termination resistors **1120**A, **1120**B are configured to set the gain of the VGA and to provide matching with the output stage.

(51) On the opposing terminals of the resistors **1120**A, **1120**B are the output paths **1128**A, **1128**B which connect to output node peaking control elements **1124**A, **1124**B. In addition, peaking control elements **1132** are provided as being attached to the termination resistors **1120**A, **1120**B as shown.

(52) The peaking control elements **1124**A, **1124**B, **1132** may comprise inductors configured and selected to provide peaking (gain) at frequencies. The value of the peaking control elements **1124**A, **1124**B, **1132** are selected to control the amount of peaking (magnitude) and the frequency or frequency range at which peaking occurs. In one embodiment, the peaking control elements **1124**A, **1124**B, **1132** comprise inductors but in other embodiments, other elements, passive, active, or a combination of both, may be used.

(53) Shown in dashed lined boxes are the gain control elements **1180** that is configured to control the gain of the VGA. In addition, the termination load **1184**A, **1184**B are configured as described above.
(54) Also shown in FIG. **11** is a cascode amplifier stage with a differential pair that includes differential pair transistors **1140**A, **1140**B which have a collector terminal connected to the peaking control elements **1132** as shown. The base terminals of the differential pair transistors **1140**A, **1140**B are connected as shown. A Vcontrol signal is provided to one set of base terminals as shown such that the Vcontrol signal controls gain. The other base terminals of differential pair transistors **1140**A, **1140**B are connected to shunt capacitors **1170** as shown to provide a common rail for symmetrical configuration. Connected to the emitter terminals of the differential pair transistors **1140**A, **1140**B are cascode connected transistors **1144**A, **1144**B as shown to provide additional amplification. The input signals In+, In− is provided to input terminals **1160**A, **1160**B, which are the base terminals of transistors **1144**A, **1144**B.
(55) A degeneration network **1150** connects in parallel with resistors **1158**A, **1158**B to a collector terminal of the transistors **1144**A, **1144**B as shown. In this embodiment, the degeneration network **1150** includes capacitors **1154** and optionally the resistors **1158**A, **1158**B. The degeneration network **1150** is configured to control or adjust low frequency gain, such as a DC gain control which in turn improves linearity. The DC gain response or behavior is dominated by the resistor values **1158**A, **1158**B, while the capacitor **1154** in the degeneration network **1150** is selected to control AC gain. Other configurations of the degeneration network **1150** are contemplated other than as shown. In addition, the combination of the capacitor and resistor value may be selected to provide gain peaking such that at higher frequencies the gain goes up, which is preferred. Absent the capacitors **1154**, the gain at high frequencies will roll off faster.
(56) The configuration of FIG. **11** provides benefits over the prior art. The terminated output (termination resistors/load) in combination with the peaking elements provide improved impedance matching between the VGA and the subsequent distributed amplifier. The improved impedance matching resulting in greater power transfer and reduces reflections.
(57) FIG. **12**A and FIG. **12**B illustrate exemplary signal plots showing the improvements of the disclosed system over prior art designs. FIG. **12**A shows improved bandwidth and gain peaking due to the innovation disclosed herein. As shown in FIG. **12**A signal, plots **1208** are shown with frequency on the horizontal axis **1212** and gain, in dB, on the vertical axis **1216**. The prior art gain plot **1220** shows a drop in gain in the 50 to 65 GHz frequency range as compared to the current system signal plot **1224**. The current system signal plot **1224** also exhibits higher gain at higher frequencies than the prior art plot **1220**.
(58) FIG. **12**B shows gain shaping due to the innovation disclosed herein. As shown in FIG. **12**B signal, plots **1208** are shown with frequency on the horizontal axis **1212** and gain, in dB, on the vertical axis **1216**. The prior art signal plot **1240** is shows with a drop in gain in the 60 to 70 GHz frequency range. Using the gain shaping disclosed herein, the gain in shaped in the frequency region to create a more linear gain function as shown in signal plot **1244**. The current system signal plot **1244** also exhibits lower gain in the 10 to 50 GHz frequency range as compared to the prior art signal plot **1240**, further increasing linearly.
(59) Other systems, methods, features and advantages of the invention will be or will become apparent to one with skill in the art upon examination of the following figures and detailed description. It is intended that all such additional systems, methods, features and advantages be included within this description, be within the scope of the invention, and be protected by the accompanying claims.
(60) While various embodiments of the invention have been described, it will be apparent to those of ordinary skill in the art that many more embodiments and implementations are possible that are within the scope of this invention. In addition, the various features, elements, and embodiments described herein may be claimed or combined in any combination or arrangement.

Claims

1. A distributed amplifier with variable gain control stage comprising: a variable gain amplifier comprising: a signal input configured to receive a data signal; a gain control input configured to receive a gain control signal; a gain controlled amplifier configured to receive the data signal and the gain control signal to create a gain adjusted signal, such that an amount gain adjustment is determined by the gain control signal; one or more gain peaking control elements, connected to the gain controlled amplifier, configured to establish gain peaking in the gain adjusted signal; and an output configured to provide the gain adjusted signal from the one or more gain peaking control elements to the distributed amplifier; two or more amplifier cells, each amplifier cell comprising: an amplifier cell input configured to receive the gain adjusted signal; two or more amplifiers, connected in a cascode configuration, to amplify the gain adjusted signal to create an amplified signal; and an amplifier cell output configured to carry the amplified signal; an input path configured to receive an input signal and distribute the input signal to the two or more amplifier cells, the input path including one or more inductors that cancel input parasitic capacitance from the two or more amplifier cells; and an output path connected to the amplifier cell output of the two or more amplifier cells to receive the amplified signal, the output path including one or more inductors that cancel output parasitic capacitance from the two or more amplifier cells.
2. The distributed amplifier of claim 1 wherein the one or more gain peaking control elements comprise inductors.
3. The distributed amplifier of claim 1 further comprising one or more emitter follower circuits having an emitter follower input connected to the input path and an emitter follower output connected to the amplifier cell input, the one or more emitter follower circuits configured to perform frequency specific gain adjustment in the amplified signal created by the one or more amplifier cells.
4. The distributed driver of claim 1 wherein an inductor from the input path and an inductor from the output path are associated with each amplifier cell.
5. The distributed driver of claim 1 further comprising a degeneration network connected to the gain controlled amplifier, the degeneration network configured to adjust low frequency gain.
6. The distributed driver of claim 1 wherein the variable gain amplifier further comprises one or more termination resistors configured to establish the gain of the gain controlled amplifier and set the output impedance of the variable gain amplifier.
7. The distributed driver of claim 1 wherein the two or more amplifier cells are configured in an open collector configuration.
8. The distributed driver of claim 3 wherein the emitter follower circuit further comprises a variable current source configured to control the frequency specific gain adjustment.
9. A distributed amplifier with variable gain control comprising: a gain control circuit comprising a gain control circuit input, a gain control circuit output, one or more gain control amplifiers, and one or more gain peaking control elements located between a variable gain amplifier and an output, such that an amount gain adjustment is determined by a gain control signal which is received on a gain control signal input of the gain control circuit and the gain control circuit generating a gain adjusted signal; and the distributed amplifier comprising: an input path configured to receive an input signal including the gain adjusted signal and distribute the input signal to two or more amplifier cells, the input path including one or more inductors that cancel input parasitic capacitance from the two or more amplifier cells; two or more amplifier cells configured with amplifiers in a cascode configuration to amplify a received signal to create an amplified signal; an output path connected to the amplifier cell output of the two or more amplifier cells to receive the amplified signal, the output path including one or more inductors that cancel output parasitic capacitance from the two or more amplifier cells.

10. The distributed amplifier of claim 9 wherein gain peaking control elements comprise inductors.
11. The distributed amplifier of claim 9 further comprising a termination load connected between the gain peaking control elements and the gain control circuit output.
12. The distributed amplifier of claim 9 further comprising one or more emitter follower circuits, associated with each amplifier cell, that are located between the input path and the two or more amplifier cells, wherein the emitter follower circuits are configured to perform frequency specific gain adjustment in the amplified signal.
13. The distributed driver of claim 12 wherein the emitter follower circuit further comprises a variable current source configured to control the frequency specific gain adjustment.
14. The distributed amplifier of claim 9 wherein the gain control circuit further comprises a degeneration network connected to the gain control amplifier, the degeneration network configured to adjust low frequency gain.
15. The distributed driver of claim 1 wherein the two or more amplifier cells are configured in an open collector configuration.
16. A method for creating an amplified signal with frequency specific magnitude adjustment comprising: receiving the input signal, an input signal to be transmitted on an optic fiber as an optic signal; adjusting gain applied to the input signal with a variable gain amplifier, based on a control gain signal, to create a gain adjusted signal, such that adjusting of the gain includes introducing frequency specific magnitude adjustment to the input signal for gain peaking, gain shaping, or both; receiving the gain adjusted signal on an amplifier input path, the amplifier input path having an inductance that cancels input parasitic capacitance of two or more amplifier cells; amplifying the input signal after frequency specific magnitude adjustment with the two or more amplifier cells; combining the amplified output signals from the two or more amplifier cells on an output path as a combined output signal, the output path having an inductance that cancels output parasitic capacitance of the two or more amplifier cells; and presenting the combined output signal on an output.
17. The method of claim 16 wherein an inductor from the input path and an inductor from the output path are associated with each amplifier cell, and the inductors are realized as integrated transmission line elements.
18. The method of claim 16 wherein the two or more amplifier cells are configured in an open collector configuration.
19. The method of claim 16 further introducing frequency specific gain control with an emitter follower circuit that is associated with at least one of the two or more amplifier cells, the emitter follower circuit including a variable current source configured to control an amount of frequency specific gain control.
20. The method of claim 16 wherein the two or more amplifier cells further comprise a first input and a second input, the first and second inputs are configured to accept a differential signal, and the first input connects to a first emitter follower circuit and the second input connects to a second emitter follower circuit.