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High electron mobility transistor and method for fabricating the same

Abstract

A semiconductor device includes a substrate having a high electron mobility transistor (HEMT) region and a capacitor region, a first mesa isolation on the HEMT region, a HEMT on the first mesa isolation, a second mesa isolation on the capacitor region, and a capacitor on the second mesa isolation. The semiconductor device further includes buffer layer between the substrate, the first mesa isolation, and the second mesa isolation, in which bottom surfaces of the first mesa isolation and the second mesa isolation are coplanar.

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Background/Summary

CROSS REFERENCE TO RELATED APPLICATIONS (1) This application is a continuation application of U.S. application Ser. No. 18/144,811, filed on May 8, 2023, which is a division of U.S. application Ser. No. 16/994,646, filed on Aug. 16, 2020. The contents of these applications are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

(1) The invention relates to a semiconductor device, and more particularly to a semiconductor device having integrated a high electron mobility transistor (HEMT) and a capacitor.

2. Description of the Prior Art

(2) High electron mobility transistor (HEMT) fabricated from GaN-based materials have various advantages in electrical, mechanical, and chemical aspects of the field. For instance, advantages including wide band gap, high break down voltage, high electron mobility, high elastic modulus, high piezoelectric and piezoresistive coefficients, and chemical inertness. All of these advantages allow GaN-based materials to be used in numerous applications including high intensity light emitting diodes (LEDs), power switching devices, regulators, battery protectors, display panel drivers, and communication devices.

SUMMARY OF THE INVENTION

(3) A semiconductor device includes a substrate having a high electron mobility transistor (HEMT) region and a capacitor region, a first mesa isolation on the HEMT region, a HEMT on the first mesa isolation, a second mesa isolation on the capacitor region, and a capacitor on the second mesa isolation. The semiconductor device further includes buffer layer between the substrate, the first mesa isolation, and the second mesa isolation, in which bottom surfaces of the first mesa isolation and the second mesa isolation are coplanar.

(4) According to another aspect of the present invention, a semiconductor device includes a substrate having a high electron mobility transistor (HEMT) region and a capacitor region, a mesa isolation on the HEMT region, a HEMT on the mesa isolation, a capacitor on the capacitor region, and a buffer layer between the mesa isolation, the capacitor, and substrate.

(5) According to yet another aspect of the present invention, a semiconductor device includes a substrate having a high electron mobility transistor (HEMT) region and a capacitor region, a mesa isolation on the HEMT region, a HEMT on the mesa isolation, a hard mask around the HEMT and extending to the capacitor region, and a capacitor on the hard mask.

(6) These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

(1) FIGS. 1-3 illustrate a method for fabricating a HEMT according to an embodiment of the present invention.

(2) FIGS. 4-6 illustrate a method for fabricating a HEMT according to an embodiment of the present invention.

(3) FIGS. 7-9 illustrate a method for fabricating a HEMT according to an embodiment of the present invention.

DETAILED DESCRIPTION

(4) Referring to the FIGS. 1-3, FIGS. 1-3 illustrate a method for fabricating a HEMT according to an embodiment of the present invention. As shown in the FIG. 1, a substrate 12 such as a substrate made from silicon, silicon carbide, or aluminum oxide (or also referred to as sapphire) is provided, in which the substrate 12 could be a single-layered substrate, a multi-layered substrate, gradient substrate, or combination thereof. According to other embodiment of the present invention, the substrate 12 could also include a silicon-on-insulator (SOI) substrate. Next, a HEMT region 14 and a capacitor region 16 are defined on the substrate 12.

(5) Next, a buffer layer 18 is formed on the surface of the substrate 12. According to an embodiment of the present invention, the buffer layer 18 is preferably made of III-V semiconductors such as gallium nitride (GaN), in which a thickness of the buffer layer 18 could be between 0.5 microns to 10 microns. According to an embodiment of the present invention, the formation of the buffer layer 18 could be accomplished by a molecular-beam epitaxy (MBE) process, a metal organic chemical vapor deposition (MOCVD) process, a chemical vapor deposition (CVD) process, a hydride vapor phase epitaxy (HVPE) process, or combination thereof.

(6) Next, a barrier layer 20 is formed on the surface of the buffer layer 18. In this embodiment, the barrier layer 20 is preferably made of III-V semiconductor such as aluminum gallium nitride ($\text{Al}_{\text{sub}}\text{xGa}_{\text{sub}}\text{1-xN}$), in which $0 < x < 1$, x being less than or equal to 20%, and the barrier layer 20 preferably includes an epitaxial layer formed through epitaxial growth process. Similar to the buffer layer 18, the formation of the barrier layer 20 on the buffer layer 18 could be accomplished by a molecular-beam epitaxy (MBE) process, a metal organic chemical vapor deposition (MOCVD) process, a chemical vapor deposition (CVD) process, a hydride vapor phase epitaxy (HVPE) process, or combination thereof. It should be noted that even though the barrier layer 20 is formed directly on the surface of the buffer layer 18, according to another embodiment of the present invention, it would also be desirable to form an extra metal nitride layer (not shown) including but not limited to for example aluminum nitride (AlN) between the buffer layer 18 and the barrier layer 20, which is also within the scope of the present invention.

(7) Next, a p-type semiconductor layer 22 is formed on the barrier layer 20. In this embodiment, the p-type semiconductor layer 22 preferably is a III-V compound layer including p-type GaN (p-GaN) and the formation of the p-type semiconductor layer 22 on the surface of the barrier layer 20 could be accomplished by a molecular-beam epitaxy (MBE) process, a metal organic chemical vapor deposition (MOCVD) process, a chemical vapor deposition (CVD) process, a hydride vapor phase

epitaxy (HVPE) process, or combination thereof.

(8) Next, a MESA isolation process is conducted to form mesa isolations **24**, **26** on the HEMT region **14** and capacitor region **16** respectively so that devices could be isolated to operate independently without affecting each other. In this embodiment, the MESA isolation process could be accomplished by conducting a photo-etching process to remove part of p-type semiconductor layer **22**, part of the barrier layer **20**, and part of the buffer layer **18**, in which the patterned p-type semiconductor layer **22**, the patterned barrier layer **20**, and the patterned buffer layer **18** preferably share equal widths and edges of the three layers are aligned. The width of the remaining un-patterned buffer layer **18** is preferably equal to the width of the substrate **12**. Preferably, each of the mesa isolations **24**, **26** includes a patterned buffer layer **18**, in which the thickness of the patterned buffer layer **18** is approximately 300 nm, the thickness of the patterned barrier layer **20** is approximately 10 nm, and the thickness of the patterned p-type semiconductor layer **22** is approximately 100 nm.

(9) Next, as shown in FIG. 2, a photo-etching process is conducted to remove part of the p-type semiconductor layer **22** on the HEMT region **14** and all of the p-type semiconductor layer **22** on the capacitor region **16** so that the remaining p-type semiconductor layer **22** is only disposed on the barrier layer **20** on HEMT region **14** while none of the p-type semiconductor layer **22** is remained on the surface of the barrier layer **20** on capacitor region **16**, in which the patterned p-type semiconductor layer **22** preferably serves as part of the gate structure for the HEMT device in the later process. Next, a hard mask **28** is conformally formed on the buffer layer **18** to cover the mesa isolations **24**, **26** on the HEMT region **14** and the capacitor region **16**. In this embodiment, the hard mask **28** preferably includes silicon nitride and the thickness of the hard mask **28** is approximately 200 nm, but not limited thereto.

(10) Next, one or more photo-etching process is conducted to remove part of the hard mask **28** and part of the barrier layer **20** on the HEMT region **14** for forming a plurality of recesses (not shown), a conductive material is formed into the recesses and on the surface of the hard mask **28** on both HEMT region **14** and capacitor region **16**, and a pattern transfer process is conducted to remove part of the conductive material. Preferably, the conductive material deposited into the recesses on the HEMT region **14** serves as a source electrode **30** and drain electrode **32**, the conductive material disposed on the source electrode **30** and drain electrode **32** and extended to the surface of the hard mask **28** adjacent to two sides of the source electrode **30** and drain electrode **32** serves as a source electrode extension **34** and drain electrode extension **36**, and the conductive material being patterned on the surface of the hard mask **28** on the capacitor region **16** preferably serves as a bottom electrode **38** for the capacitor. Next, another hard mask **40** is formed on the surface of hard mask **28** on the HEMT region **14** and extending to the bottom electrode **38** on the capacitor region **16**, in which the hard mask **40** on the capacitor region **16** preferably serves as a capacitor dielectric layer **42**. In this embodiment, the thickness of the capacitor dielectric layer **42** is between 20-100 nm, but not limited thereto.

(11) Next, as shown in FIG. 3, one or more photo-etching process is conducted to remove part of the hard mask **40** and part of the hard mask **28** on the HEMT region **14** for forming a recess exposing the p-type semiconductor layer **22**, another conductive material is formed on the hard mask **40** on HEMT region **14** to fill the recess completely while covering the surface of the hard mask **40** on the capacitor region **16**, and a pattern transfer process is conducted to remove part of the conductive material, in which the conductive material deposited into the recess and part of the conductive material on the surface of the hard mask **40** on the HEMT region **14** preferably serves as a gate electrode **44** while the patterned conductive material layer on the capacitor region **16** serves as a top electrode for the capacitor.

(12) In this embodiment, the gate electrode **44**, source electrode **30**, and drain electrode **32** are preferably made of metal, in which gate electrode **44** preferably includes Schottky metal while the source electrode **30** and the drain electrode **32** are preferably made of ohmic contact metals.

According to an embodiment of the present invention, each of the gate electrode **44**, source electrode **30**, and drain electrode **32** could include gold (Au), silver (Ag), platinum (Pt), titanium (Ti), aluminum (Al), tungsten (W), palladium (Pd), or combination thereof. Moreover, it would be desirable to conduct an electroplating process, sputtering process, resistance heating evaporation process, electron beam evaporation process, physical vapor deposition (PVD) process, chemical vapor deposition (CVD) process, or combination thereof to form conductive materials in the aforementioned recesses and then pattern the conductive materials through single or multiple etching processes for forming the gate electrode **44**, the source electrode **30**, and the drain electrode **32**.

(13) Next, a contact plug formation could be conducted to form contact plugs **50** electrically connected to the gate electrode **44**, source electrode **30**, and drain electrode **32** on the HMET region **14** and the bottom electrode **38** and top electrode **46** on the capacitor region **16**. In this embodiment, the formation of contact plugs **50** could be accomplished by first forming an interlayer dielectric (ILD) layer **48** on the hard mask **40** on both HMET region **14** and capacitor region **16**, removing part of the ILD layer **48** and part of the hard mask **40** to form contact holes (not shown), and then depositing a barrier layer (not shown) and a metal layer (not shown) into the contact holes. A planarizing process, such as chemical mechanical polishing (CMP) process is then conducted to remove part of the metal layer, part of the barrier layer, and even part of the ILD layer **48** to form contact plugs **50** in the contact holes, in which the top surface of the contact plugs **50** is even with the top surface of the ILD layer **48**. In this embodiment, the barrier layer is selected from the group consisting of Ti, Ta, TiN, TaN, and WN and the metal layer is selected from the group consisting of Al, Ti, Ta, W, Nb, Mo, and Cu.

(14) Referring again to FIG. 3, FIG. 3 further illustrates a structural view of a semiconductor device according to an embodiment of the present invention. As shown in FIG. 3, the semiconductor device preferably includes a HMET region **14** and a capacitor region **16** defined on the substrate **12**, a mesa isolation **24** disposed on the HMET region **14**, a HEMT **52** disposed on the mesa isolation **24**, another mesa isolation **26** disposed on the capacitor region **16**, a buffer layer **18** disposed on the substrate **12** and between the mesa isolations **24**, **26**, and a capacitor **54** disposed on the mesa isolation **26**, in which the bottom surfaces of the mesa isolations **24**, **26** are coplanar and both mesa isolations **24**, **26** includes GaN.

(15) The HEMT **52** includes a barrier layer **20** disposed on the mesa isolation **24**, a p-type semiconductor layer **22** disposed on the barrier layer **20**, a gate electrode **44** disposed on the p-type semiconductor layer **22**, a source electrode **30** and drain electrode **32** adjacent to two sides of the gate electrode **44**, a source electrode extension **34** disposed on the source electrode **30**, a drain electrode extension **36** disposed on the drain electrode **32**, and a hard mask **28** disposed on the mesa isolations **24**, **26** and surrounding the source electrode **30** and drain electrode **32**.

(16) The capacitor **54** includes a bottom electrode **38** disposed on the hard mask **28**, a capacitor dielectric layer **42** disposed on the bottom electrode **38** and extending to the top surface and sidewall of the hard mask **28** on the HMET region **14**, and a top electrode **46** disposed on the capacitor dielectric layer **42**, in which the bottom surface of the bottom electrode **38** is even with the bottom surface of the source electrode extension **34** while the top surface of the top electrode **46** is even with the top surface of the gate electrode **44**.

(17) Referring to FIGS. 4-6, FIGS. 4-6 illustrate a method for fabricating a HEMT according to an embodiment of the present invention. For simplicity purpose, elements from the aforementioned embodiments are labeled with same numberings. As shown in the FIG. 4, a substrate **12** such as a substrate made from silicon, silicon carbide, or aluminum oxide (or also referred to as sapphire) is provided, in which the substrate **12** could be a single-layered substrate, a multi-layered substrate, gradient substrate, or combination thereof. According to other embodiment of the present invention, the substrate **12** could also include a silicon-on-insulator (SOI) substrate. Next, a HEMT region **14** and a capacitor region **16** are defined on the substrate **12**.

(18) Next, a buffer layer **18** is formed on the surface of the substrate **12**. According to an embodiment of the present invention, the buffer layer **18** is preferably made of III-V semiconductors such as gallium nitride (GaN), in which a thickness of the buffer layer **18** could be between 0.5 microns to 10 microns. According to an embodiment of the present invention, the formation of the buffer layer **18** could be accomplished by a molecular-beam epitaxy (MBE) process, a metal organic chemical vapor deposition (MOCVD) process, a chemical vapor deposition (CVD) process, a hydride vapor phase epitaxy (HVPE) process, or combination thereof.

(19) Next, a barrier layer **20** is formed on the surface of the buffer layer **18**. In this embodiment, the barrier layer **20** is preferably made of III-V semiconductor such as aluminum gallium nitride (Al.sub.xGa.sub.1-xN), in which $0 < x < 1$, x being less than or equal to 20%, and the barrier layer **20** preferably includes an epitaxial layer formed through epitaxial growth process. Similar to the buffer layer **18**, the formation of the barrier layer **20** on the buffer layer **18** could be accomplished by a molecular-beam epitaxy (MBE) process, a metal organic chemical vapor deposition (MOCVD) process, a chemical vapor deposition (CVD) process, a hydride vapor phase epitaxy (HVPE) process, or combination thereof. It should be noted that even though the barrier layer **20** is formed directly on the surface of the buffer layer **18**, according to another embodiment of the present invention, it would also be desirable to form an extra metal nitride layer (not shown) including but not limited to for example aluminum nitride (AlN) between the buffer layer **18** and the barrier layer **20**, which is also within the scope of the present invention.

(20) Next, a p-type semiconductor layer **22** is formed on the barrier layer **20**. In this embodiment, the p-type semiconductor layer **22** preferably is a III-V compound layer including p-type GaN (p-GaN) and the formation of the p-type semiconductor layer **22** on the surface of the barrier layer **20** could be accomplished by a molecular-beam epitaxy (MBE) process, a metal organic chemical vapor deposition (MOCVD) process, a chemical vapor deposition (CVD) process, a hydride vapor phase epitaxy (HVPE) process, or combination thereof.

(21) Next, a MESA isolation process is conducted to form a mesa isolation **24** on the HEMT region **14**. In this embodiment, the MESA isolation process could be accomplished by conducting a photo-etching process to remove part of p-type semiconductor layer **22**, part of the barrier layer **20**, and part of the buffer layer **18**, in which the patterned p-type semiconductor layer **22**, the patterned barrier layer **20**, and the patterned buffer layer **18** preferably share equal widths and edges of the three layers are aligned. The width of the remaining un-patterned buffer layer **18** is preferably equal to the width of the substrate **12**. Preferably, the mesa isolation **24** includes a patterned buffer layer **18**, in which the thickness of the patterned buffer layer **18** is approximately 300 nm, the thickness of the patterned barrier layer **20** is approximately 10 nm, and the thickness of the patterned p-type semiconductor layer **22** is approximately 100 nm.

(22) Next, as shown in FIG. 5, a photo-etching process is conducted to remove part of the p-type semiconductor layer **22** on the HEMT region **14**, in which the patterned p-type semiconductor layer **22** preferably serves as part of the gate structure for the HEMT device in the later process. Next, a hard mask **28** is conformally formed on the buffer layer **18** to cover the mesa isolation **24** on the HEMT region **14** while extending to the buffer layer **18** on the capacitor region **16**. In this embodiment, the hard mask **28** preferably includes silicon nitride and the thickness of the hard mask **28** is approximately 200 nm, but not limited thereto.

(23) Next, one or more photo-etching process is conducted to remove part of the hard mask **28** and part of the barrier layer **20** on the HEMT region **14** and majority of the hard mask **28** on the capacitor region **16** for forming a plurality of recesses (not shown), a conductive material is formed into the recesses on both HEMT region **14** and capacitor region **16**, and a pattern transfer process is conducted to remove part of the conductive material. Preferably, the conductive material deposited into the recesses on the HEMT region **14** serves as a source electrode **30** and drain electrode **32**, the conductive material disposed on the source electrode **30** and drain electrode **32** and extended to the surface of the hard mask **28** adjacent to two sides of the source electrode **30** and drain electrode **32**

serves as a source electrode extension **34** and drain electrode extension **36**, and the conductive material being formed into the recess or trench on the capacitor region **16** preferably serves as a bottom electrode **38** for the capacitor. Next, another hard mask **40** is formed on the surface of hard mask **28** on the HEMT region **14** and extending to the bottom electrode **38** on the capacitor region **16**, in which the hard mask **40** on the capacitor region **16** preferably serves as a capacitor dielectric layer **42**. In this embodiment, the thickness of the capacitor dielectric layer **42** is between 20-100 nm, but not limited thereto.

(24) Next, as shown in FIG. **6**, one or more photo-etching process is conducted to remove part of the hard mask **40** and part of the hard mask **28** on the HEMT region **14** for forming a recess exposing the p-type semiconductor layer **22**, another conductive material is formed on the hard mask **40** on HEMT region **14** to fill the recess completely while covering the surface of the hard mask **40** on the capacitor region **16**, and a pattern transfer process is conducted to remove part of the conductive material, in which the conductive material deposited into the recess and part of the conductive material on the surface of the hard mask **40** on the HEMT region **14** preferably serves as a T-shape gate electrode **44** while the patterned conductive material layer on the capacitor region **16** serves as a top electrode **46** for the capacitor.

(25) Similar to the aforementioned embodiment, the gate electrode **44**, source electrode **30**, and drain electrode **32** are preferably made of metal, in which gate electrode **44** preferably includes Schottky metal while the source electrode **30** and the drain electrode **32** are preferably made of ohmic contact metals. According to an embodiment of the present invention, each of the gate electrode **44**, source electrode **30**, and drain electrode **32** could include gold (Au), silver (Ag), platinum (Pt), titanium (Ti), aluminum (Al), tungsten (W), palladium (Pd), or combination thereof. Moreover, it would be desirable to conduct an electroplating process, sputtering process, resistance heating evaporation process, electron beam evaporation process, physical vapor deposition (PVD) process, chemical vapor deposition (CVD) process, or combination thereof to form conductive materials in the aforementioned recesses and then pattern the conductive materials through single or multiple etching processes for forming the gate electrode **44**, the source electrode **30**, and the drain electrode **32**.

(26) Next, a contact plug formation could be conducted to form contact plugs **50** electrically connected to the gate electrode **44**, source electrode **30**, and drain electrode **32** on the HMET region **14** and the bottom electrode **38** and top electrode **46** on the capacitor region **16**. In this embodiment, the formation of contact plugs **50** could be accomplished by first forming an interlayer dielectric (ILD) layer **48** on the hard mask **40** on both HEMT region **14** and capacitor region **16**, removing part of the ILD layer **48** and part of the hard mask **40** to form contact holes (not shown), and then depositing a barrier layer (not shown) and a metal layer (not shown) into the contact holes. A planarizing process, such as chemical mechanical polishing (CMP) process is then conducted to remove part of the metal layer, part of the barrier layer, and even part of the ILD layer **48** to form contact plugs **50** in the contact holes, in which the top surface of the contact plugs **50** is even with the top surface of the ILD layer **48**. In this embodiment, the barrier layer is selected from the group consisting of Ti, Ta, TiN, TaN, and WN and the metal layer is selected from the group consisting of Al, Ti, Ta, W, Nb, Mo, and Cu.

(27) Referring again to FIG. **6**, FIG. **6** further illustrates a structural view of a semiconductor device according to an embodiment of the present invention. As shown in FIG. **6**, the semiconductor device preferably includes a HEMT region **14** and a capacitor region **16** defined on the substrate **12**, a mesa isolation **24** disposed on the HEMT region **14**, a HEMT **52** disposed on the mesa isolation **24**, a capacitor **54** disposed on the capacitor region **16**, and a buffer layer **18** disposed between the mesa isolation **24**, the capacitor **54**, and the substrate **12**, in which the mesa isolation **24** and the buffer layer **18** both include GaN.

(28) The HEMT **52** includes a barrier layer **20** disposed on the mesa isolation **24**, a p-type semiconductor layer **22** disposed on the barrier layer **20**, a gate electrode **44** disposed on the p-type

semiconductor layer **22**, a source electrode **30** and drain electrode **32** adjacent to two sides of the gate electrode **44**, a source electrode extension **34** disposed on the source electrode **30**, a drain electrode extension **36** disposed on the drain electrode **32**, and a hard mask **28** disposed on the mesa isolation **24** and surrounding the source electrode **30** and drain electrode **32**.

(29) The capacitor **54** on the other hand includes a bottom electrode **38** disposed on the hard mask **28**, a capacitor dielectric layer **42** disposed on the bottom electrode **38** while extending to the top surface and sidewall of the hard mask **28** on the HEMT region **14**, and a top electrode **46** disposed on the capacitor dielectric layer **42**. In contrast to the aforementioned embodiment having mesa isolations **24**, **26** on both HEMT region **14** and capacitor region **16**, only a mesa isolation **24** is disposed on the HEMT region **14** in this embodiment while the capacitor region **16** includes no mesa isolation so that the bottom electrode **38** would contact the top surface of the buffer layer **18** directly while having a T-shape cross-section. Moreover, the overall thickness of the bottom electrode **38** is substantially equal to the combined thickness of the source electrode **30** and source electrode extension **34** or the combined thickness of the drain electrode **32** and drain electrode extension **36** on the HEMT region **14**. Preferably, the overall thickness of the bottom electrode **38** is about 300 nm, the thickness of the capacitor dielectric layer **42** is between 20-100 nm, and the thickness of the top electrode **46** is about 100 nm.

(30) Referring to FIGS. 7-9, FIGS. 7-9 illustrate a method for fabricating a HEMT according to an embodiment of the present invention. For simplicity purpose, elements from the aforementioned embodiments are labeled with same numberings. As shown in the FIG. 7, a substrate **12** such as a substrate made from silicon, silicon carbide, or aluminum oxide (or also referred to as sapphire) is provided, in which the substrate **12** could be a single-layered substrate, a multi-layered substrate, gradient substrate, or combination thereof. According to other embodiment of the present invention, the substrate **12** could also include a silicon-on-insulator (SOI) substrate. Next, a HEMT region **14** and a capacitor region **16** are defined on the substrate **12**.

(31) Next, a buffer layer **18** is formed on the surface of the substrate **12**. According to an embodiment of the present invention, the buffer layer **18** is preferably made of III-V semiconductors such as gallium nitride (GaN), in which a thickness of the buffer layer **18** could be between 0.5 microns to 10 microns. According to an embodiment of the present invention, the formation of the buffer layer **18** could be accomplished by a molecular-beam epitaxy (MBE) process, a metal organic chemical vapor deposition (MOCVD) process, a chemical vapor deposition (CVD) process, a hydride vapor phase epitaxy (HVPE) process, or combination thereof.

(32) Next, a barrier layer **20** is formed on the surface of the buffer layer **18**. In this embodiment, the barrier layer **20** is preferably made of III-V semiconductor such as aluminum gallium nitride ($\text{Al}_{\text{sub.x}}\text{Ga}_{\text{sub.1-x}}\text{N}$), in which $0 < x < 1$, x being less than or equal to 20%, and the barrier layer **20** preferably includes an epitaxial layer formed through epitaxial growth process. Similar to the buffer layer **18**, the formation of the barrier layer **20** on the buffer layer **18** could be accomplished by a molecular-beam epitaxy (MBE) process, a metal organic chemical vapor deposition (MOCVD) process, a chemical vapor deposition (CVD) process, a hydride vapor phase epitaxy (HVPE) process, or combination thereof. It should be noted that even though the barrier layer **20** is formed directly on the surface of the buffer layer **18**, according to another embodiment of the present invention, it would also be desirable to form an extra metal nitride layer (not shown) including but not limited to for example aluminum nitride (AlN) between the buffer layer **18** and the barrier layer **20**, which is also within the scope of the present invention.

(33) Next, a p-type semiconductor layer **22** is formed on the barrier layer **20**. In this embodiment, the p-type semiconductor layer **22** preferably is a III-V compound layer including p-type GaN (p-GaN) and the formation of the p-type semiconductor layer **22** on the surface of the barrier layer **20** could be accomplished by a molecular-beam epitaxy (MBE) process, a metal organic chemical vapor deposition (MOCVD) process, a chemical vapor deposition (CVD) process, a hydride vapor phase epitaxy (HVPE) process, or combination thereof.

(34) Next, a MESA isolation process is conducted to form a mesa isolation **24** on the HEMT region **14**. In this embodiment, the MESA isolation process could be accomplished by conducting a photo-etching process to remove part of p-type semiconductor layer **22**, part of the barrier layer **20**, and part of the buffer layer **18**, in which the patterned p-type semiconductor layer **22**, the patterned barrier layer **20**, and the patterned buffer layer **18** preferably share equal widths and edges of the three layers are aligned. The width of the remaining un-patterned buffer layer **18** is preferably equal to the width of the substrate **12**. Preferably, the mesa isolation **24** includes a patterned buffer layer **18**, in which the thickness of the patterned buffer layer **18** is approximately 300 nm, the thickness of the patterned barrier layer **20** is approximately 10 nm, and the thickness of the patterned p-type semiconductor layer **22** is approximately 100 nm.

(35) Next, a photo-etching process is conducted to remove part of the p-type semiconductor layer **22** on the HEMT region **14**, in which the patterned p-type semiconductor layer **22** preferably serves as part of the gate structure for the HEMT device in the later process. Next, a hard mask **28** is conformally formed on the buffer layer **18** to cover the mesa isolation **24** on the HEMT region **14** while extending to the buffer layer **18** on the capacitor region **16**. In this embodiment, the hard mask **28** preferably includes silicon nitride and the thickness of the hard mask **28** is approximately 200 nm, but not limited thereto.

(36) Next, as shown in FIG. **8**, one or more photo-etching process is conducted to remove part of the hard mask **28** and part of the barrier layer **20** on the HEMT region **14** for forming a plurality of recesses (not shown), a conductive material is formed into the recesses on the HEMT region **14** and onto the surface of the hard mask **28** on the capacitor region **16**, and a pattern transfer process is conducted to remove part of the conductive material. Preferably, the conductive material deposited into the recesses on the HEMT region **14** serves as a source electrode **30** and drain electrode **32**, the conductive material disposed on the source electrode **30** and drain electrode **32** and extended to the surface of the hard mask **28** adjacent to two sides of the source electrode **30** and drain electrode **32** serves as a source electrode extension **34** and drain electrode extension **36**, and the conductive material formed on the surface of the hard mask **28** on the capacitor region **16** preferably serves as a bottom electrode **38** for the capacitor. Next, another hard mask **40** is formed on the surface of hard mask **28** on the HEMT region **14** and extending to the bottom electrode **38** on the capacitor region **16**, in which the hard mask **40** on the capacitor region **16** preferably serves as a capacitor dielectric layer **42**. In this embodiment, the thickness of the capacitor dielectric layer **42** is between 20-100 nm, but not limited thereto.

(37) Next, as shown in FIG. **9**, one or more photo-etching process is conducted to remove part of the hard mask **40** and part of the hard mask **28** on the HEMT region **14** for forming a recess exposing the p-type semiconductor layer **22**, another conductive material is formed on the hard mask **40** on HEMT region **14** to fill the recess completely while covering the surface of the hard mask **40** on the capacitor region **16**, and a pattern transfer process is conducted to remove part of the conductive material, in which the conductive material deposited into the recess and part of the conductive material on the surface of the hard mask **40** on the HEMT region **14** preferably serves as a T-shape gate electrode **44** while the patterned conductive material layer on the capacitor region **16** serves as a top electrode **46** for the capacitor.

(38) Similar to the aforementioned embodiment, the gate electrode **44**, source electrode **30**, and drain electrode **32** are preferably made of metal, in which gate electrode **44** preferably includes Schottky metal while the source electrode **30** and the drain electrode **32** are preferably made of ohmic contact metals. According to an embodiment of the present invention, each of the gate electrode **44**, source electrode **30**, and drain electrode **32** could include gold (Au), silver (Ag), platinum (Pt), titanium (Ti), aluminum (Al), tungsten (W), palladium (Pd), or combination thereof. Moreover, it would be desirable to conduct an electroplating process, sputtering process, resistance heating evaporation process, electron beam evaporation process, physical vapor deposition (PVD) process, chemical vapor deposition (CVD) process, or combination thereof to form conductive

materials in the aforementioned recesses and then pattern the conductive materials through single or multiple etching processes for forming the gate electrode **44**, the source electrode **30**, and the drain electrode **32**.

(39) Next, a contact plug formation could be conducted to form contact plugs **50** electrically connected to the gate electrode **44**, source electrode **30**, and drain electrode **32** on the HMET region **14** and the bottom electrode **38** and top electrode **46** on the capacitor region **16**. In this embodiment, the formation of contact plugs **50** could be accomplished by first forming an interlayer dielectric (ILD) layer **48** on the hard mask **40** on both HMET region **14** and capacitor region **16**, removing part of the ILD layer **48** and part of the hard mask **40** to form contact holes (not shown), and then depositing a barrier layer (not shown) and a metal layer (not shown) into the contact holes. A planarizing process, such as chemical mechanical polishing (CMP) process is then conducted to remove part of the metal layer, part of the barrier layer, and even part of the ILD layer **48** to form contact plugs **50** in the contact holes, in which the top surface of the contact plugs **50** is even with the top surface of the ILD layer **48**. In this embodiment, the barrier layer is selected from the group consisting of Ti, Ta, TiN, TaN, and WN and the metal layer is selected from the group consisting of Al, Ti, Ta, W, Nb, Mo, and Cu.

(40) Referring again to FIG. **9**, FIG. **9** further illustrates a structural view of a semiconductor device according to an embodiment of the present invention. As shown in FIG. **9**, the semiconductor device preferably includes a HMET region **14** and a capacitor region **16** defined on the substrate **12**, a mesa isolation **24** disposed on the HMET region **14**, a HEMT **52** disposed on the mesa isolation **24**, a hard mask **28** surrounding the HEMT **52** and extending to the capacitor region **16**, a capacitor **54** disposed on the capacitor region **16**, and a buffer layer **18** disposed between the mesa isolation **24**, the capacitor **54**, and the substrate **12**, in which the mesa isolation **24** and the buffer layer **18** both include GaN.

(41) The HEMT **52** includes a barrier layer **20** disposed on the mesa isolation **24**, a p-type semiconductor layer **22** disposed on the barrier layer **20**, a gate electrode **44** disposed on the p-type semiconductor layer **22**, a source electrode **30** and drain electrode **32** adjacent to two sides of the gate electrode **44**, a source electrode extension **34** disposed on the source electrode **30**, and a drain electrode extension **36** disposed on the drain electrode **32**.

(42) The capacitor **54** on the other hand includes a bottom electrode **38** disposed on the hard mask **28**, a capacitor dielectric layer **42** disposed on the bottom electrode **38** while extending to the top surface and sidewall of the hard mask **28** on the HMET region **14**, and a top electrode **46** disposed on the capacitor dielectric layer **42**. In contrast to the bottom electrode **38** disposed directly on the buffer layer **18** while the overall thickness of the bottom electrode **38** is equivalent to the combined thickness of the source electrode **30** and source electrode extension **34** or the combined thickness of drain electrode **32** and drain electrode extension **36** on HMET region **14** in the aforementioned embodiment, the thickness of the bottom electrode **38** in this embodiment is only equal to the overall thickness of the source electrode extension **34** or drain electrode extensions **36** on the HMET region **14**. Preferably, the overall thickness of the bottom electrode **38** is about 100 nm, the thickness of the capacitor dielectric layer **42** is between 20-100 nm, and the thickness of the top electrode **46** is about 100 nm.

(43) Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

Claims

1. A semiconductor device, comprising: a substrate having a high electron mobility transistor (HEMT) region and a capacitor region; a mesa isolation on the HMET region; a HEMT on the

mesa isolation; a capacitor on the capacitor region, wherein bottom surfaces of the mesa isolation and a bottom electrode of the capacitor are coplanar; a buffer layer between the mesa isolation, the capacitor, and substrate; and a hard mask on the mesa isolation and extending to directly contact a sidewall of the bottom electrode of the capacitor.

2. The semiconductor device of claim 1, wherein the mesa isolation and the buffer layer comprise gallium nitride (GaN).

3. The semiconductor device of claim 1, wherein the HEMT comprises: a barrier layer on the mesa isolation; a p-type semiconductor layer on the barrier layer; a gate electrode on the p-type semiconductor layer; a source electrode and a drain electrode adjacent to two sides of the gate electrode; a source electrode extension on the source electrode; and a drain electrode extension on the drain electrode.

4. The semiconductor device of claim 3, further comprising the hard mask on the mesa isolation and around the source electrode and the drain electrode.

5. The semiconductor device of claim 4, wherein the capacitor comprises: the bottom electrode on the buffer layer; a capacitor dielectric layer on the bottom electrode and extending to the hard mask on the HEMT region; and a top electrode on the capacitor dielectric layer.
