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(54) **FERROELECTRIC FIELD EFFECT TRANSISTOR WITH DOUBLE SPACER AND METHOD OF MANUFACTURING THE SAME**

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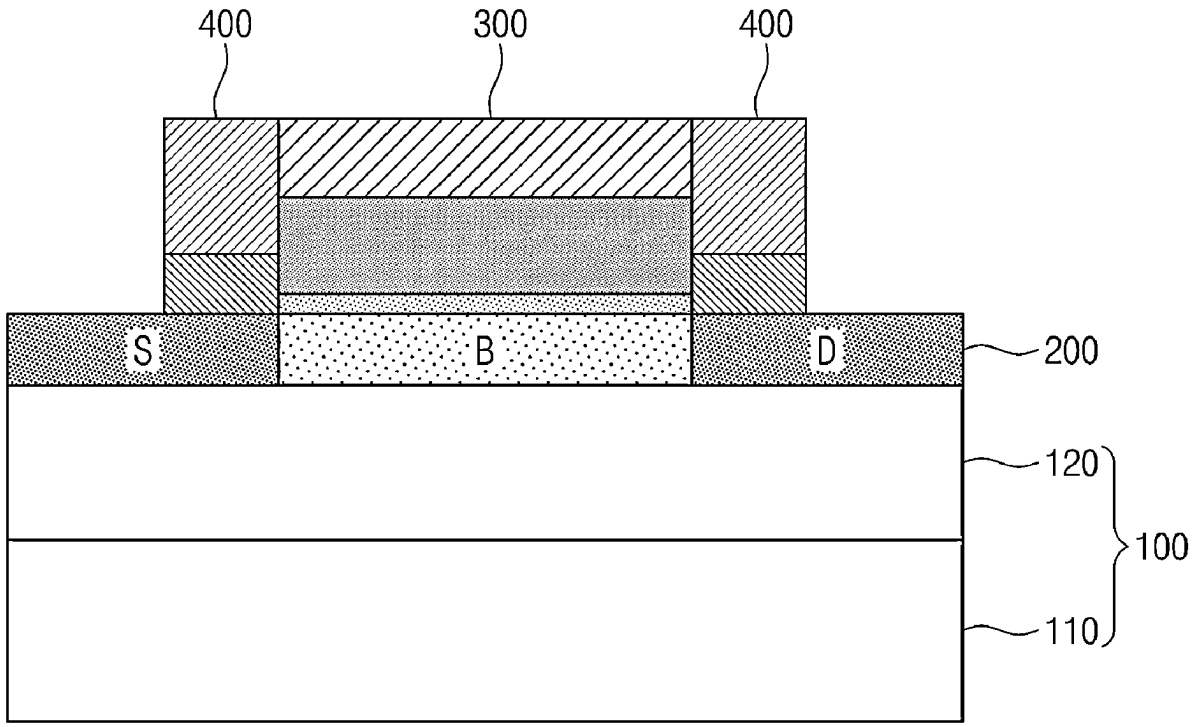
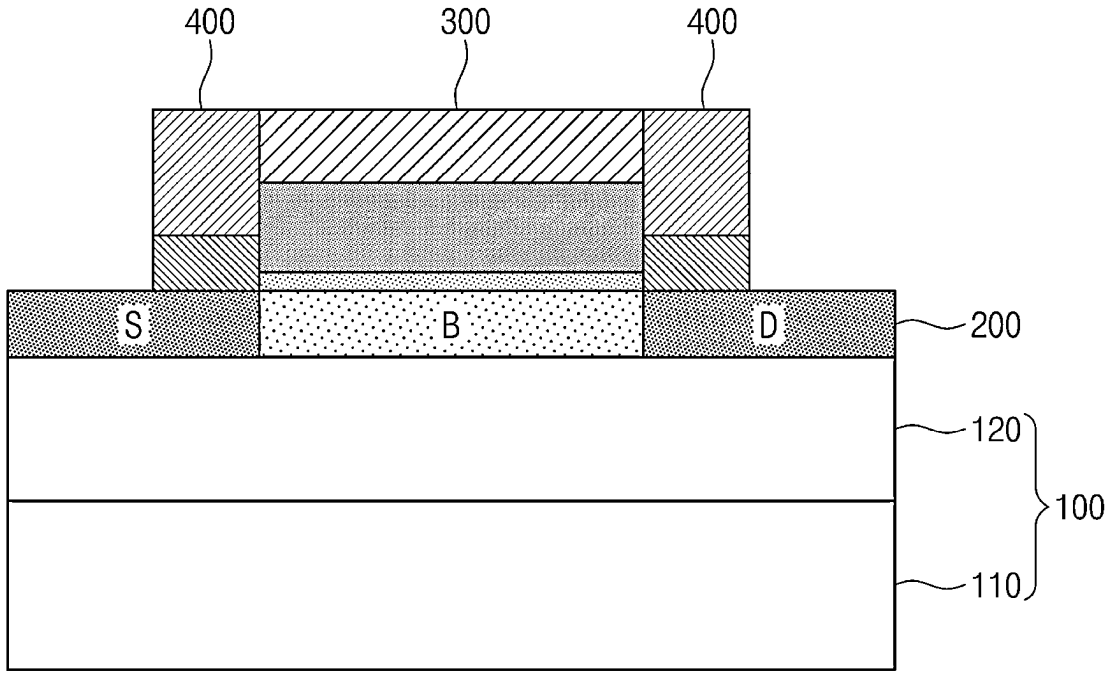
(57) **ABSTRACT**

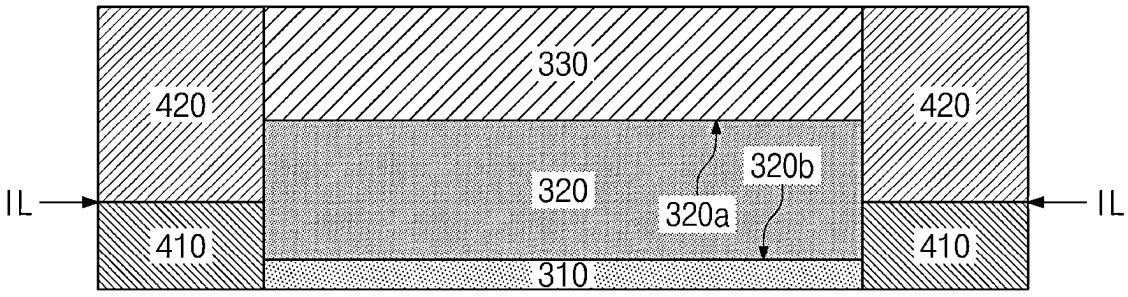
Provided is a ferroelectric field effect transistor. The ferroelectric field effect transistor includes: a body layer including a source region, a drain region spaced apart from the source region, and an intermediate region disposed between the source region and the drain region; a gate structure including a gate dielectric layer, a ferroelectric layer, and a gate electrode which are sequentially stacked on the intermediate region of the body layer; and a double spacer disposed on a side wall of the gate structure, in which the double spacer includes a high-k lower spacer and a low-k upper spacer disposed on the lower spacer.



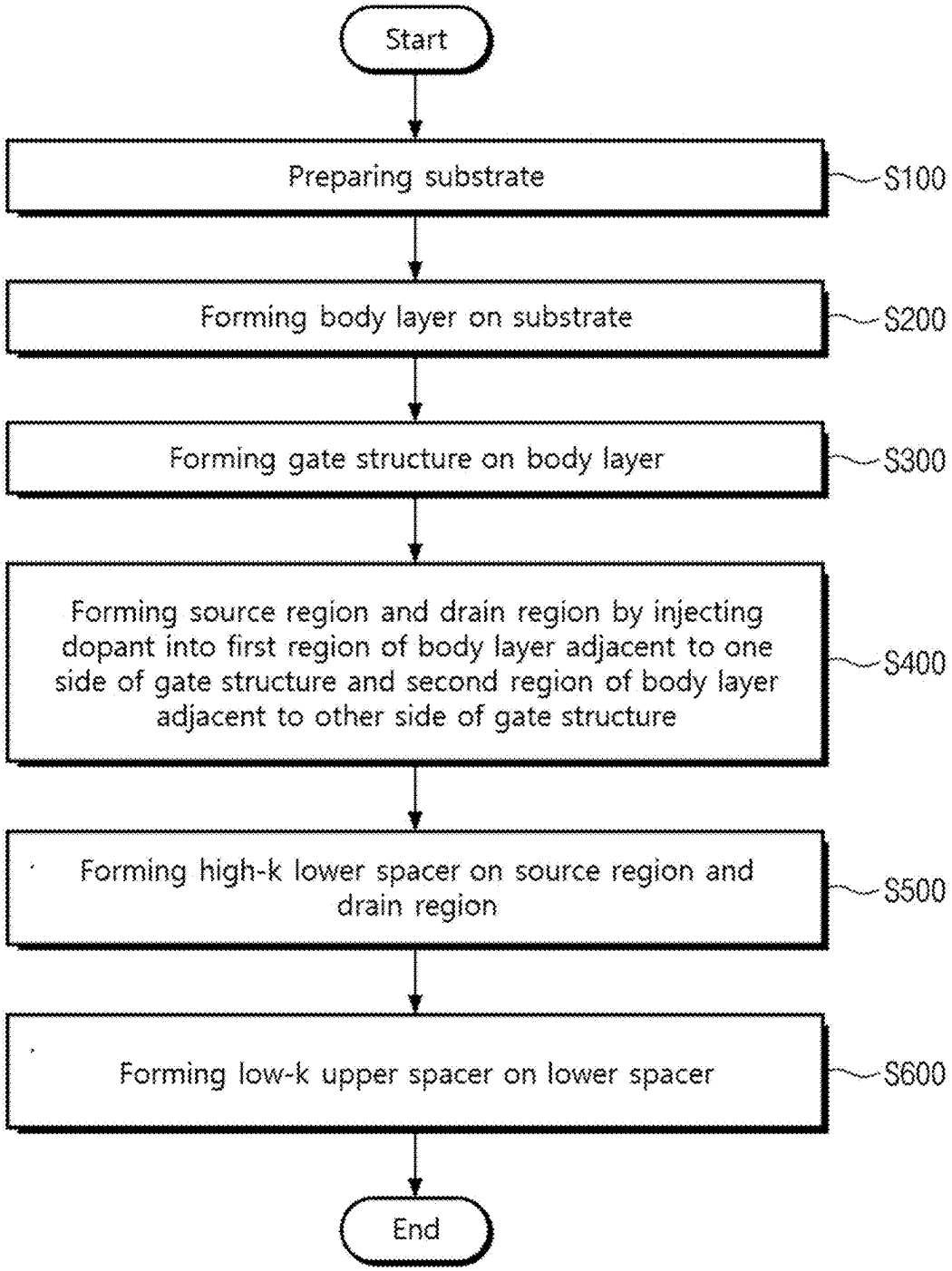
【Fig. 1】


400
300
400
S
B
D
200
120
100
110

【Fig. 2】


330
420
420
320b
320
320a
IL
IL
410
410
310

【Fig. 3】

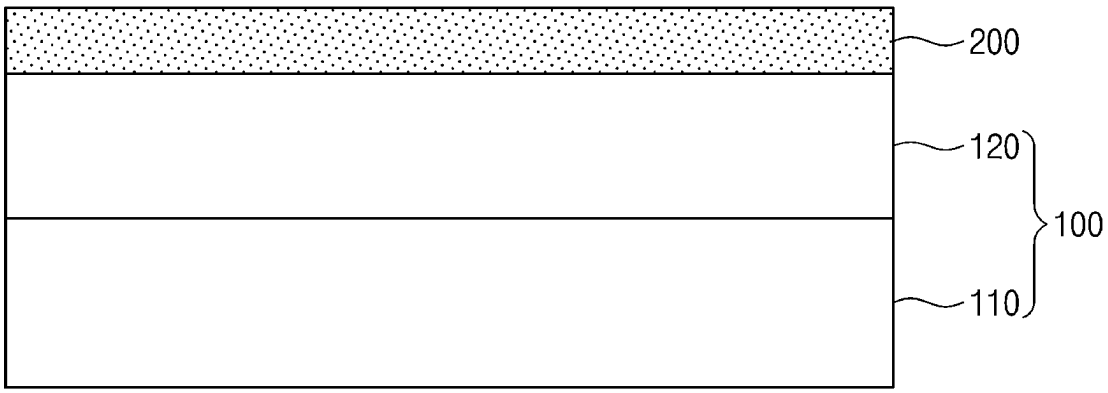

Start
Preparing substrate
S100
Forming body layer on substrate
S200
Forming gate structure on body layer
S300
Forming source region and drain region by injecting dopant into first region of body layer adjacent to one side of gate structure and second region of body layer adjacent to other side of gate structure
S400
Forming high-k lower spacer on source region and drain region
S500
Forming low-k upper spacer on lower spacer
S600
End

【Fig. 4】

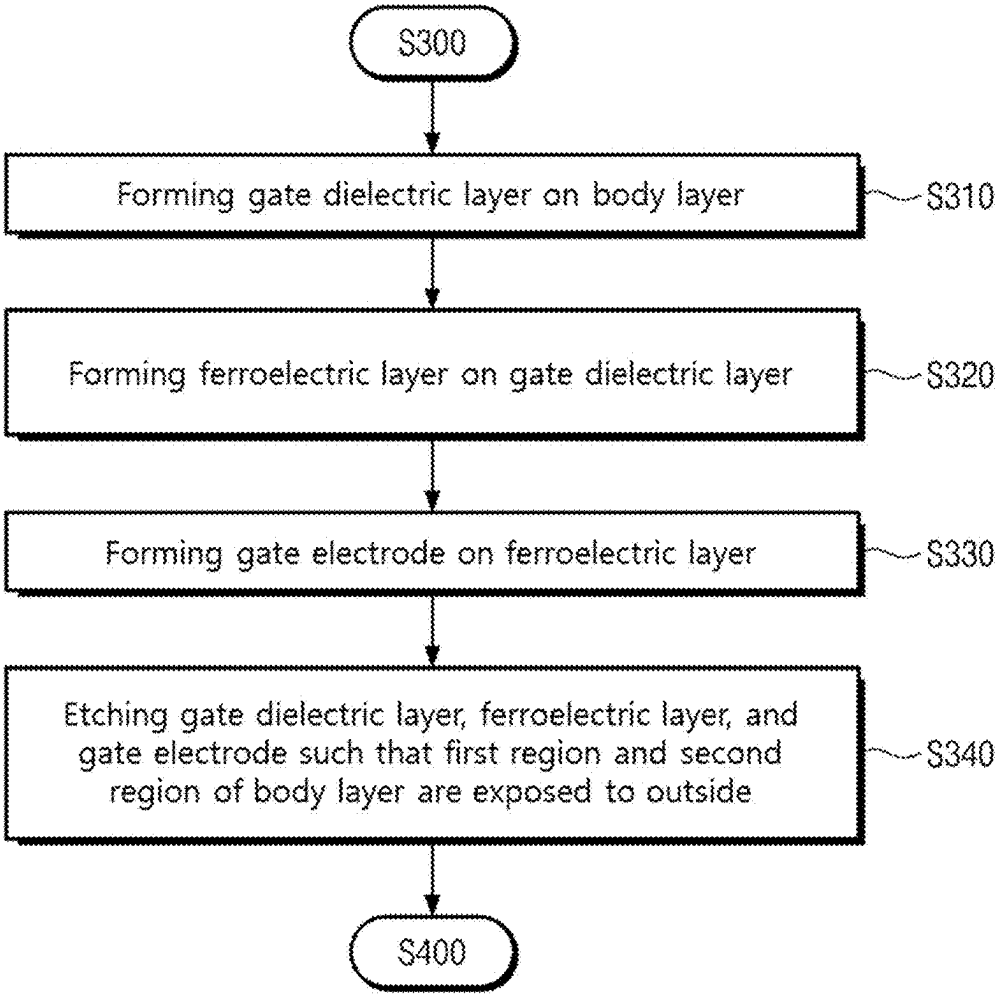
S100

【Fig. 5】

S200

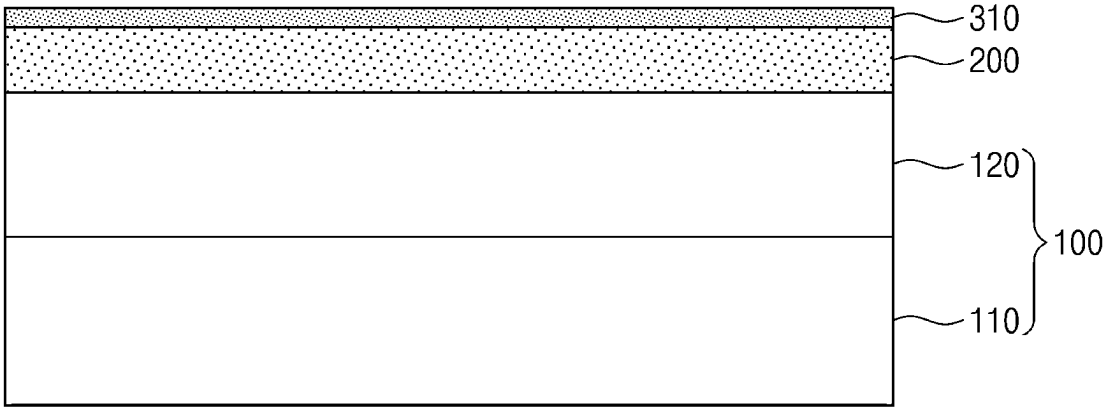


【Fig. 6】


S300
Forming gate dielectric layer on body layer
S310
Forming ferroelectric layer on gate dielectric layer
S320
Forming gate electrode on ferroelectric layer
S330
Etching gate dielectric layer, ferroelectric layer, and gate electrode such that first region and second region of body layer are exposed to outside
S340
S400

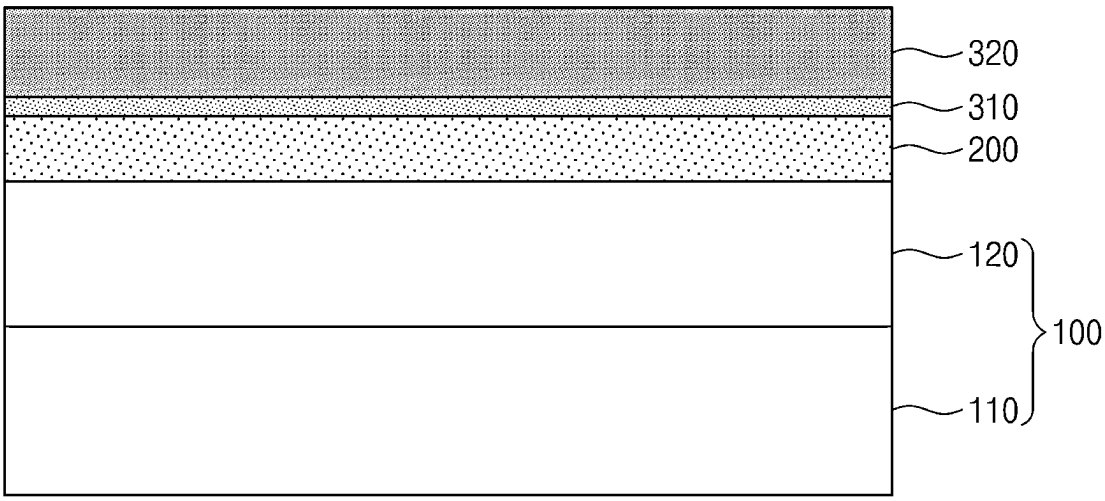
【Fig. 7】

S310



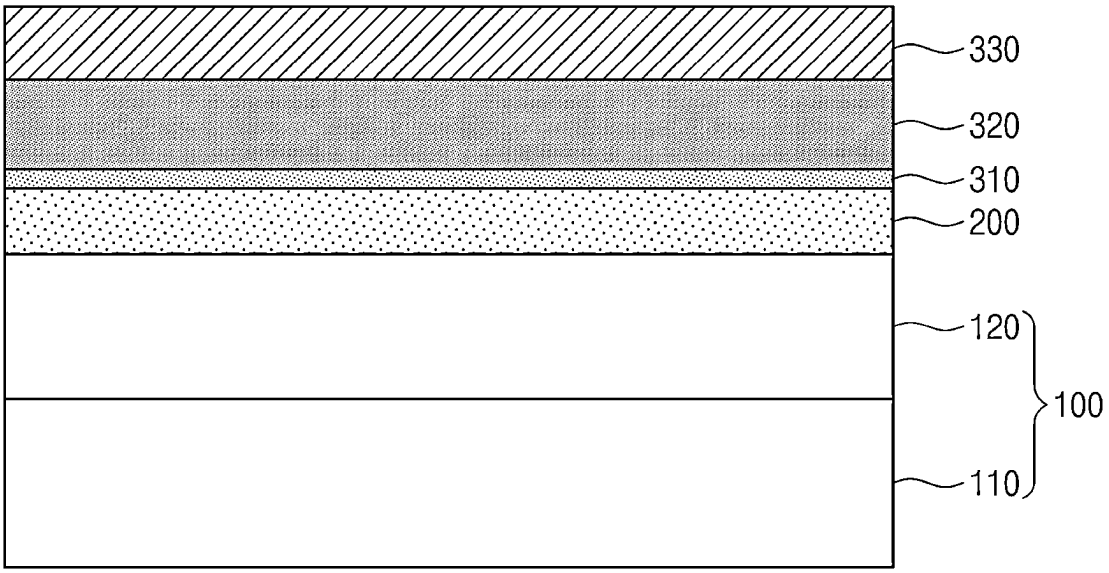
【Fig. 8】

S320



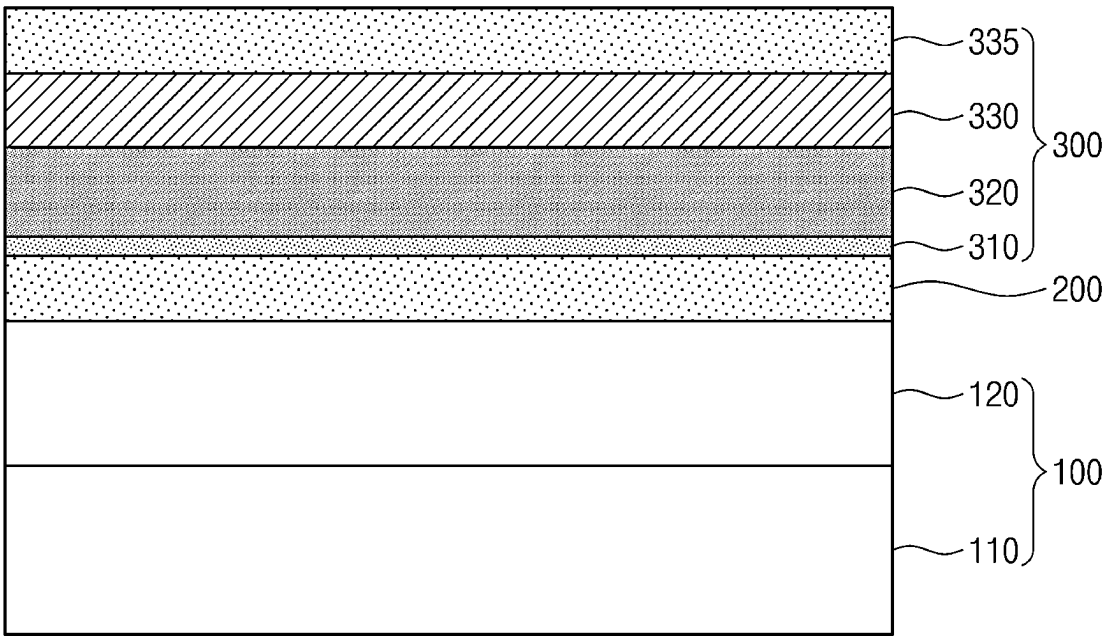
【Fig. 9】

S330



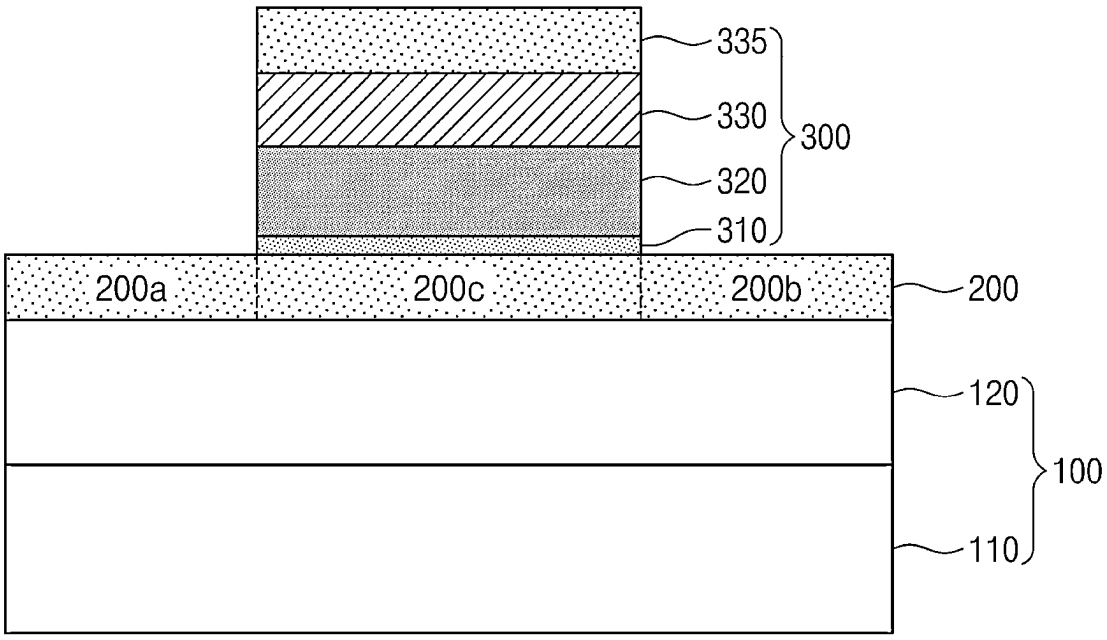
【Fig. 10】

S335



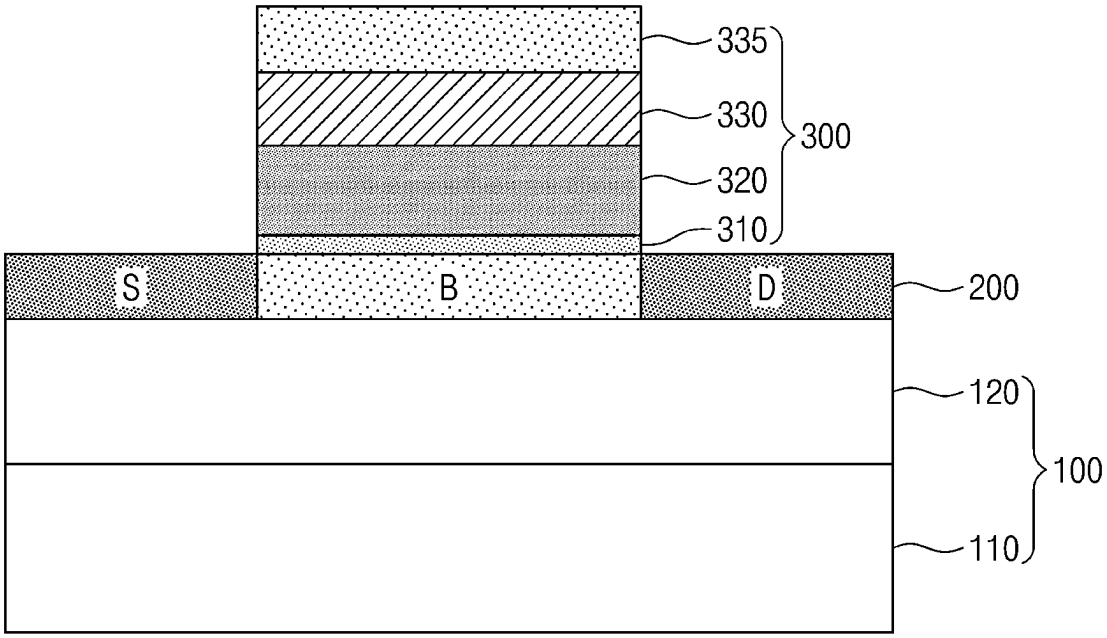
【Fig. 11】

S340

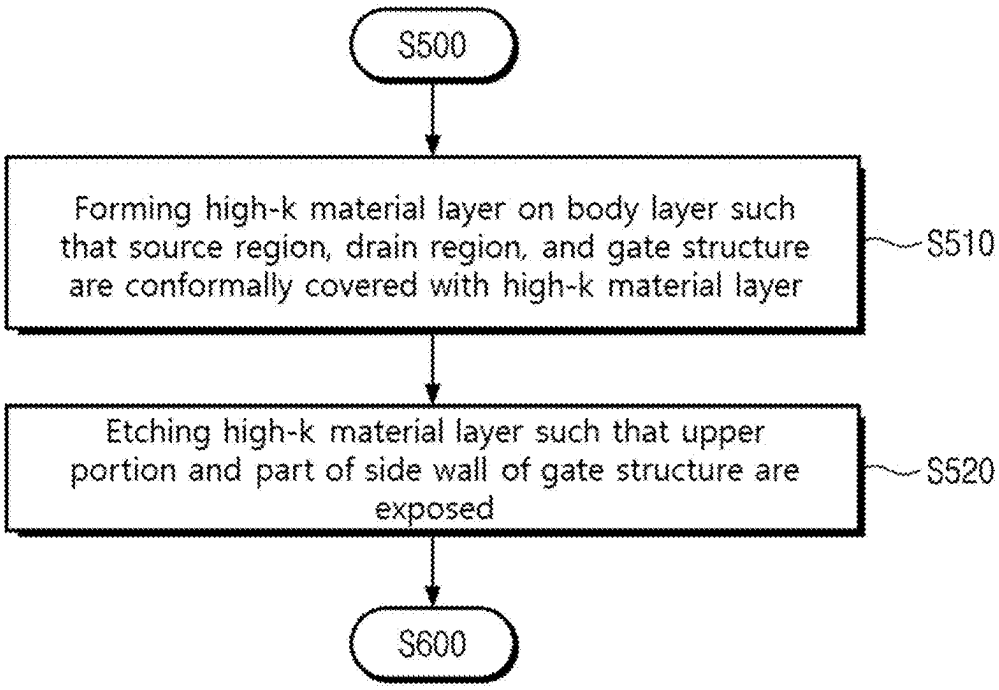


【Fig. 12】

S400

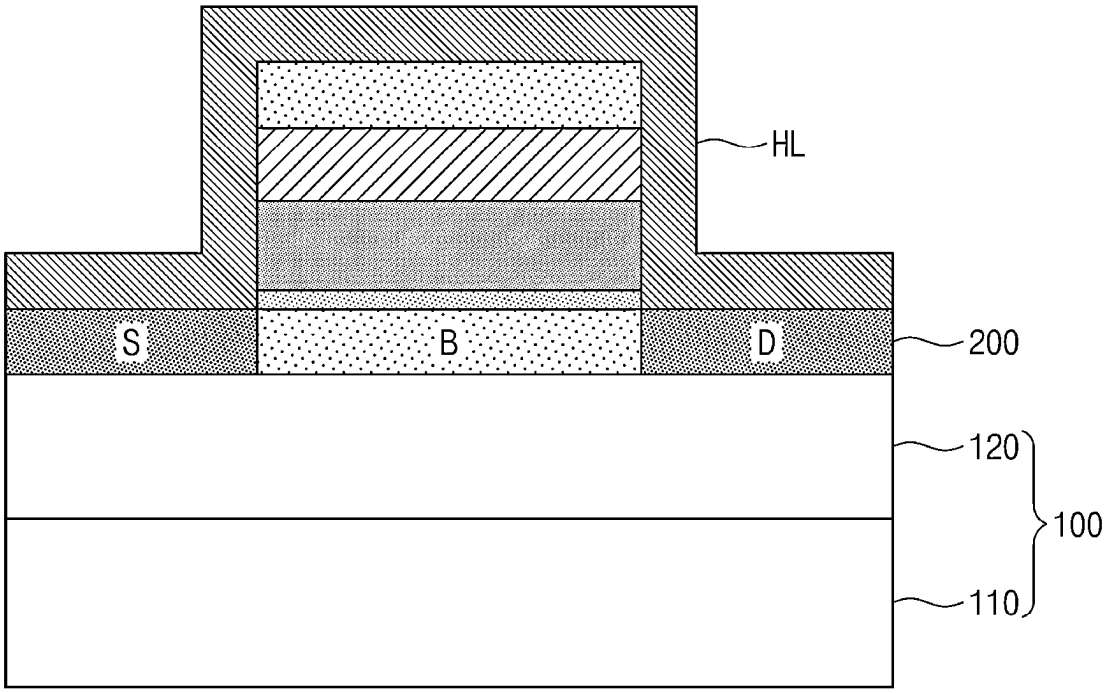


【Fig. 13】

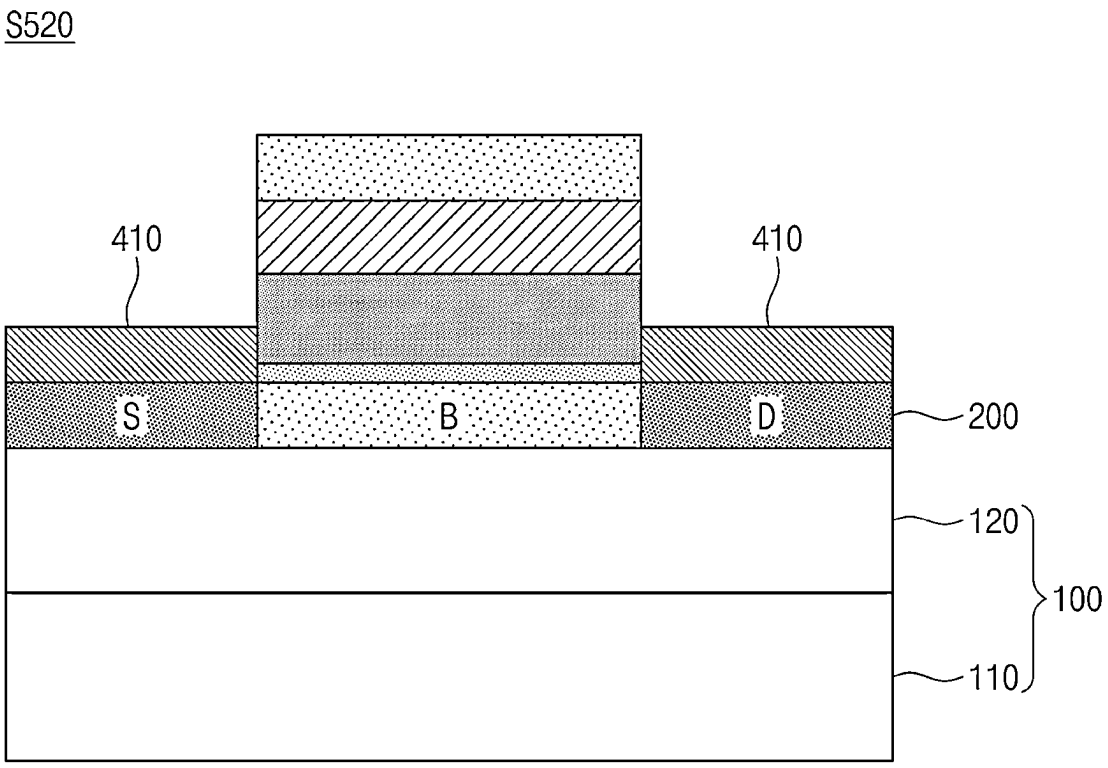

S500
Forming high-k material layer on body layer such that source region, drain region, and gate structure are conformally covered with high-k material layer
S510
Etching high-k material layer such that upper portion and part of side wall of gate structure are exposed
S520
S600

【Fig. 14】

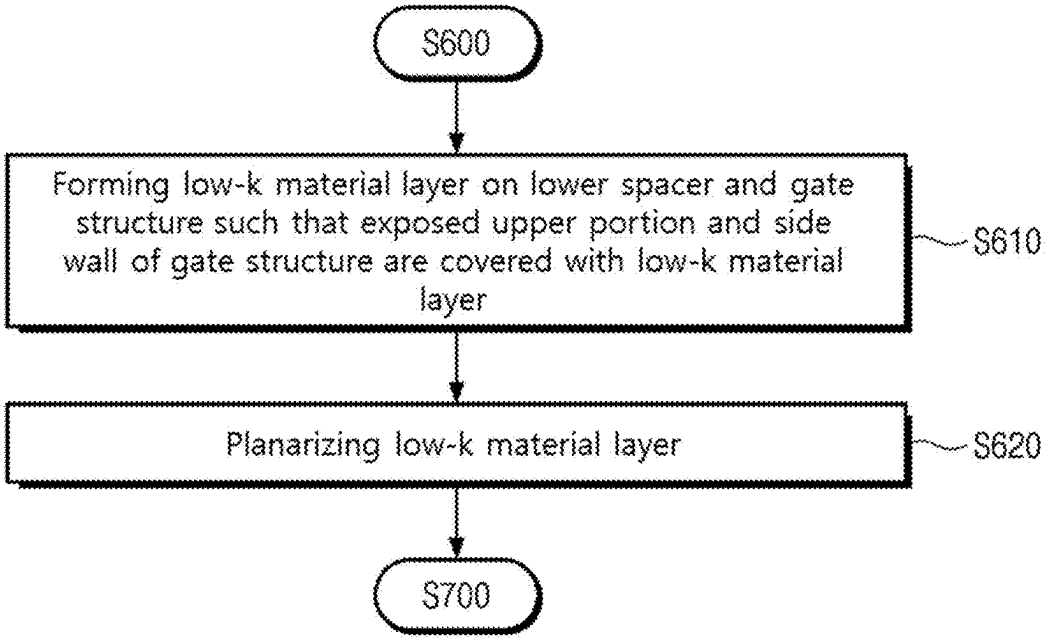
S510



【Fig. 15】

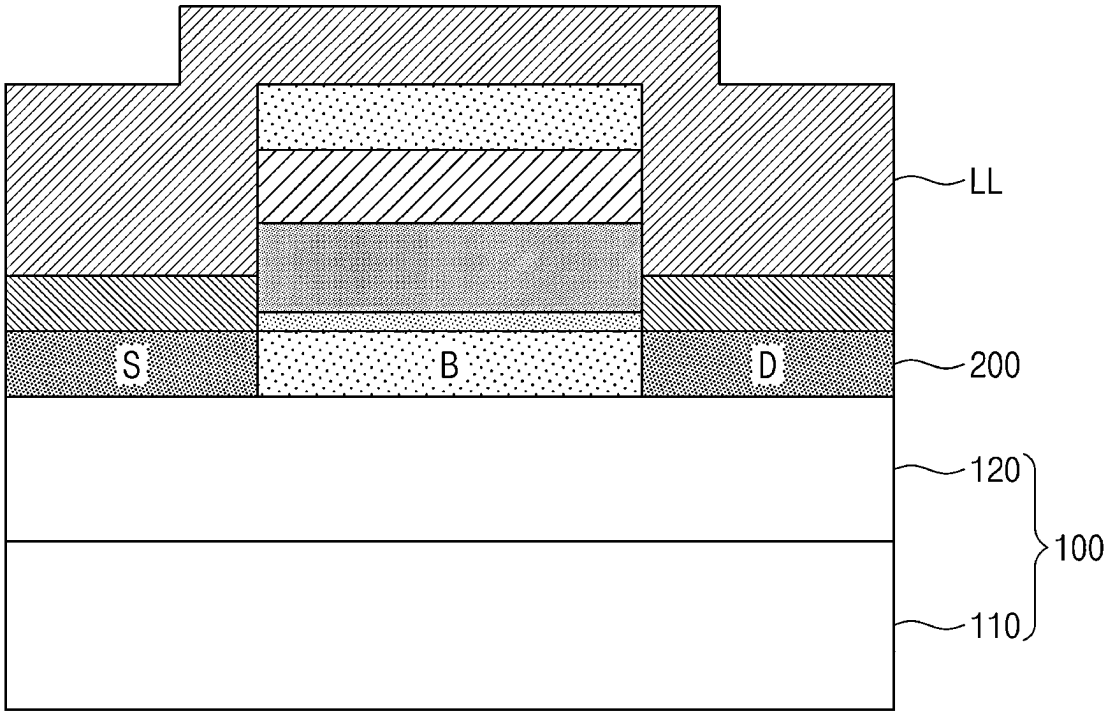


【Fig. 16】


S600
Forming low-k material layer on lower spacer and gate structure such that exposed upper portion and side wall of gate structure are covered with low-k material layer
S610
Planarizing low-k material layer
S620
S700

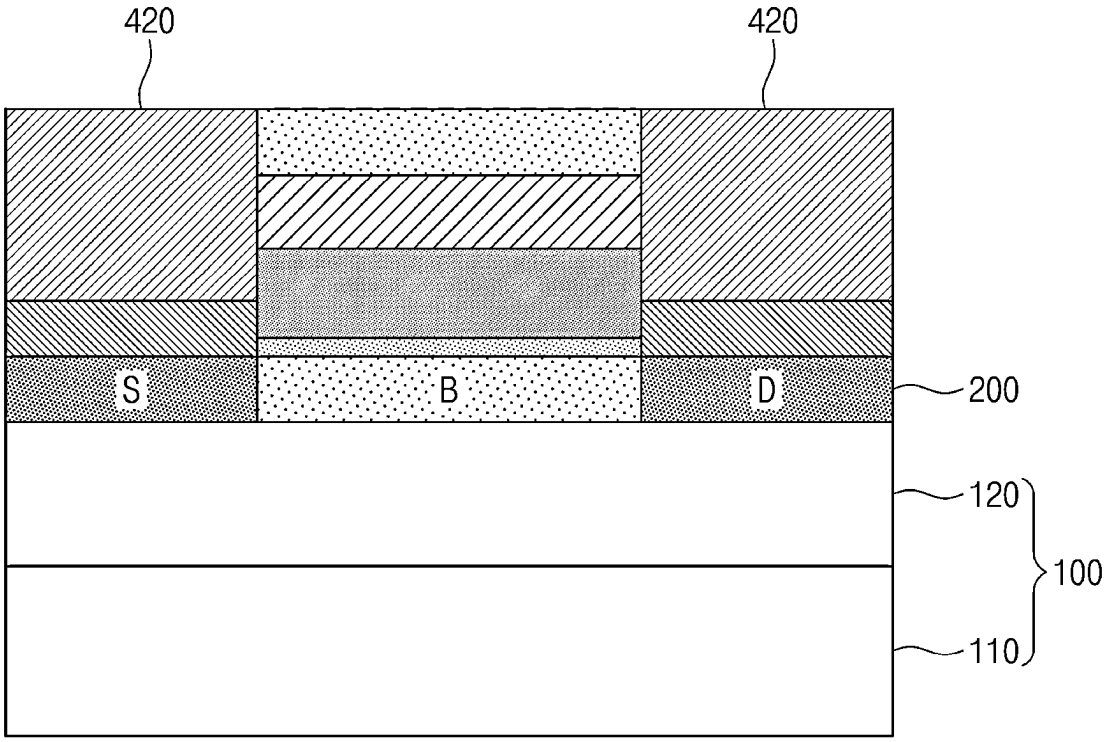
【Fig. 17】

S610

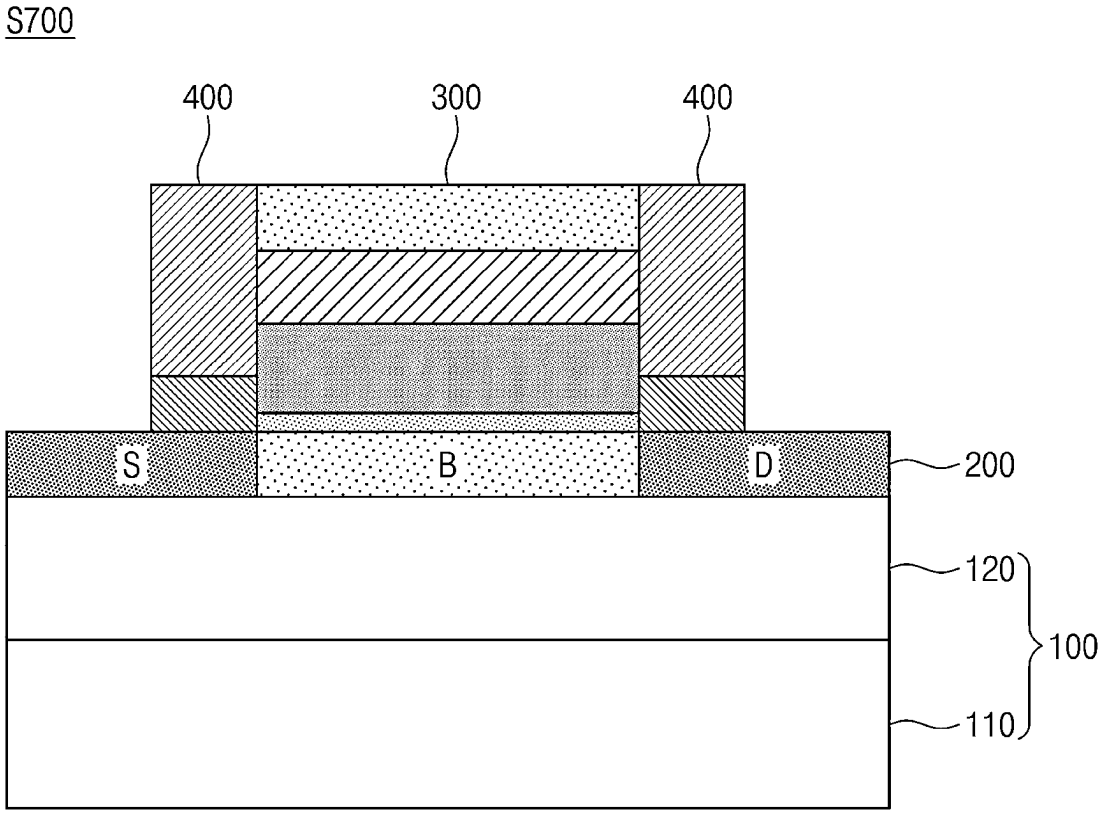


【Fig. 18】

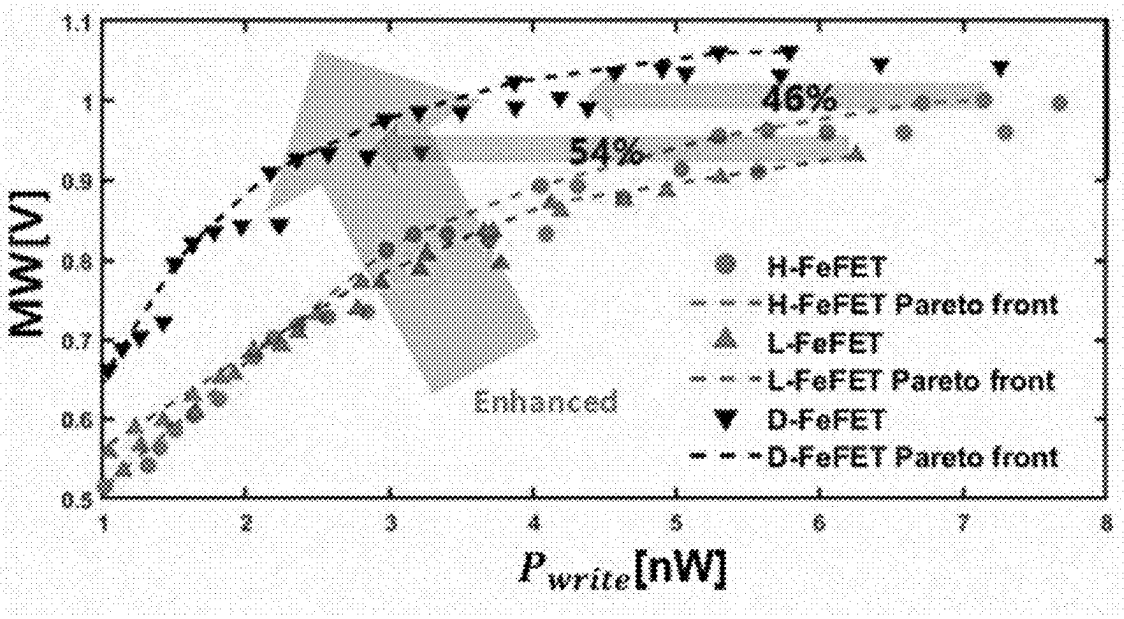
S620



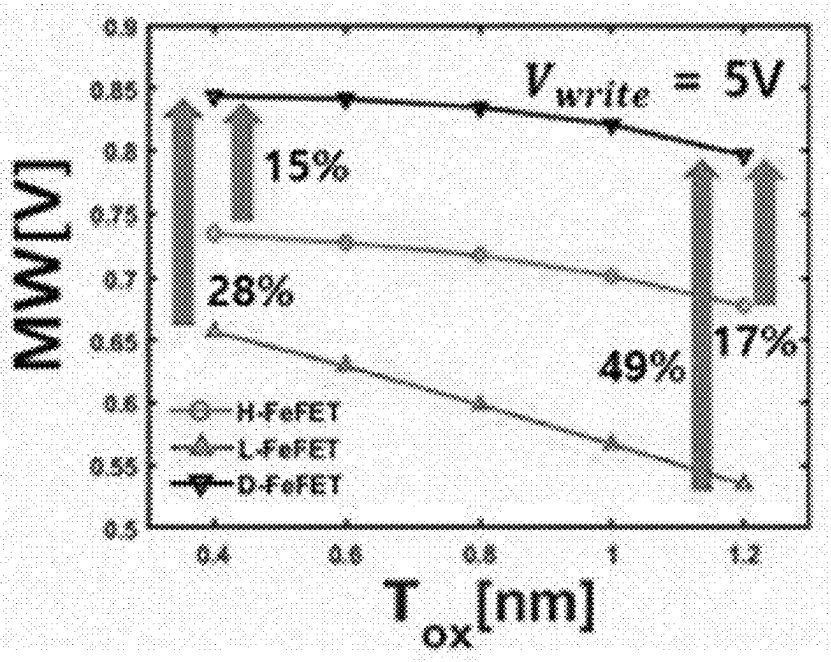
【Fig. 19】



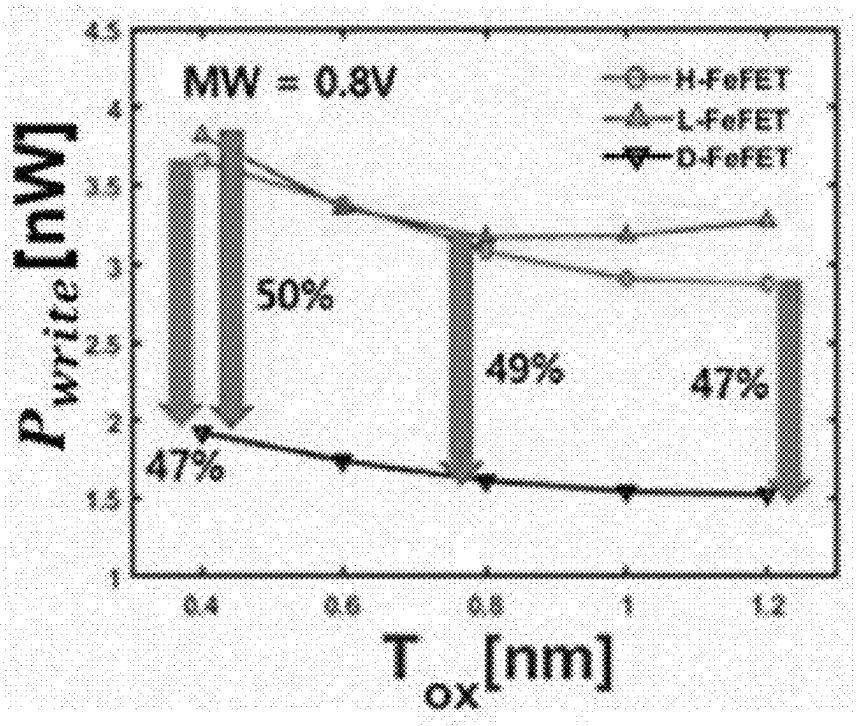
【Fig. 20(a)】



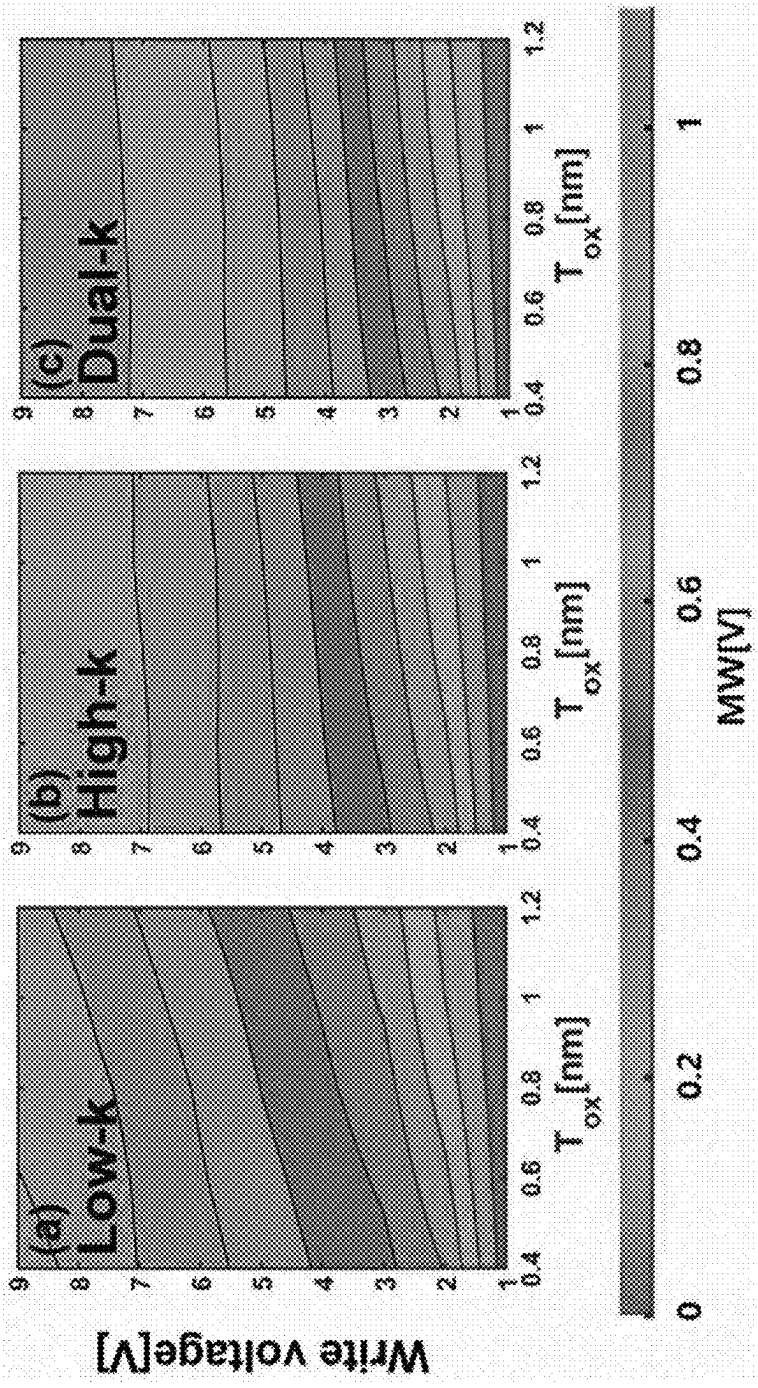
【Fig. 20(b)】



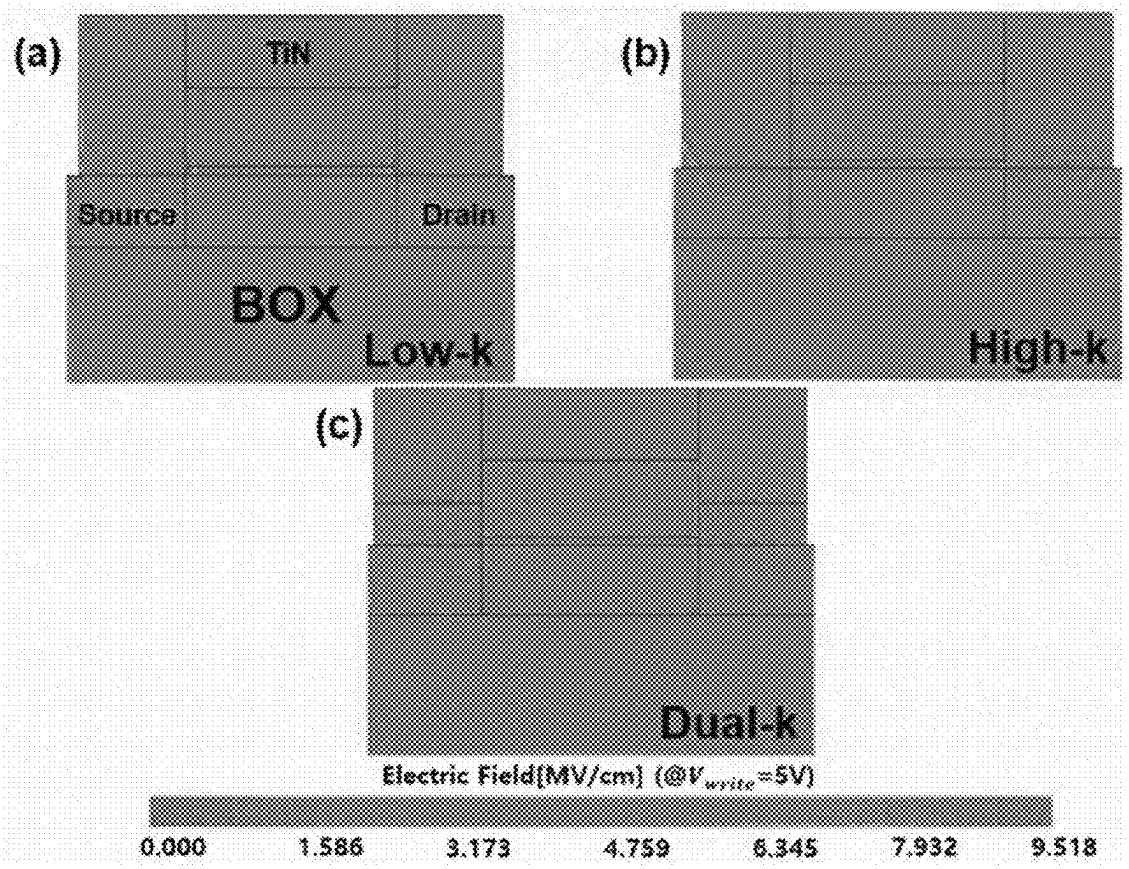
【Fig. 20(c)】


MW = 0.8V
H-FeFET
L-FeFET
D-FeFET
50%
49%
47%
47%
P_{write}[nW]
T_{ox}[nm]
4.5
4
3.5
3
2.5
2
1.5
1
0.4
0.6
0.8
1
1.2

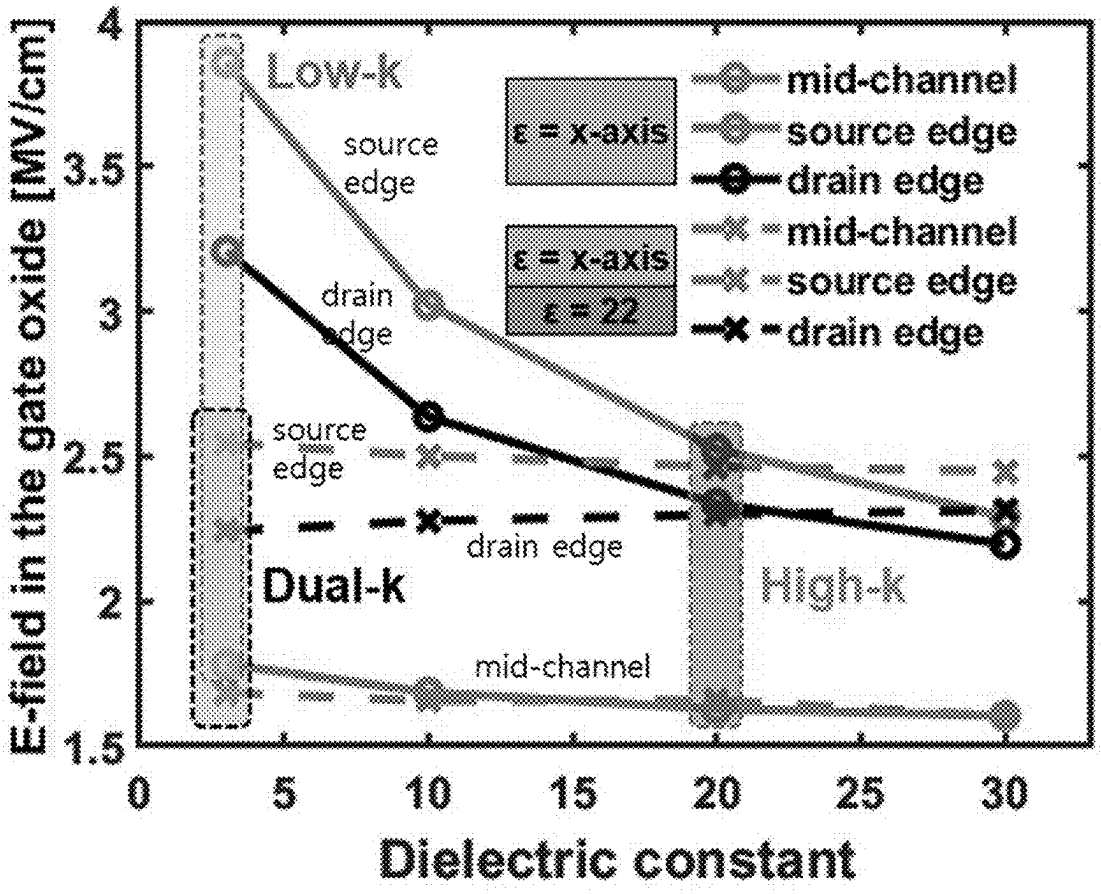
[Fig. 21]



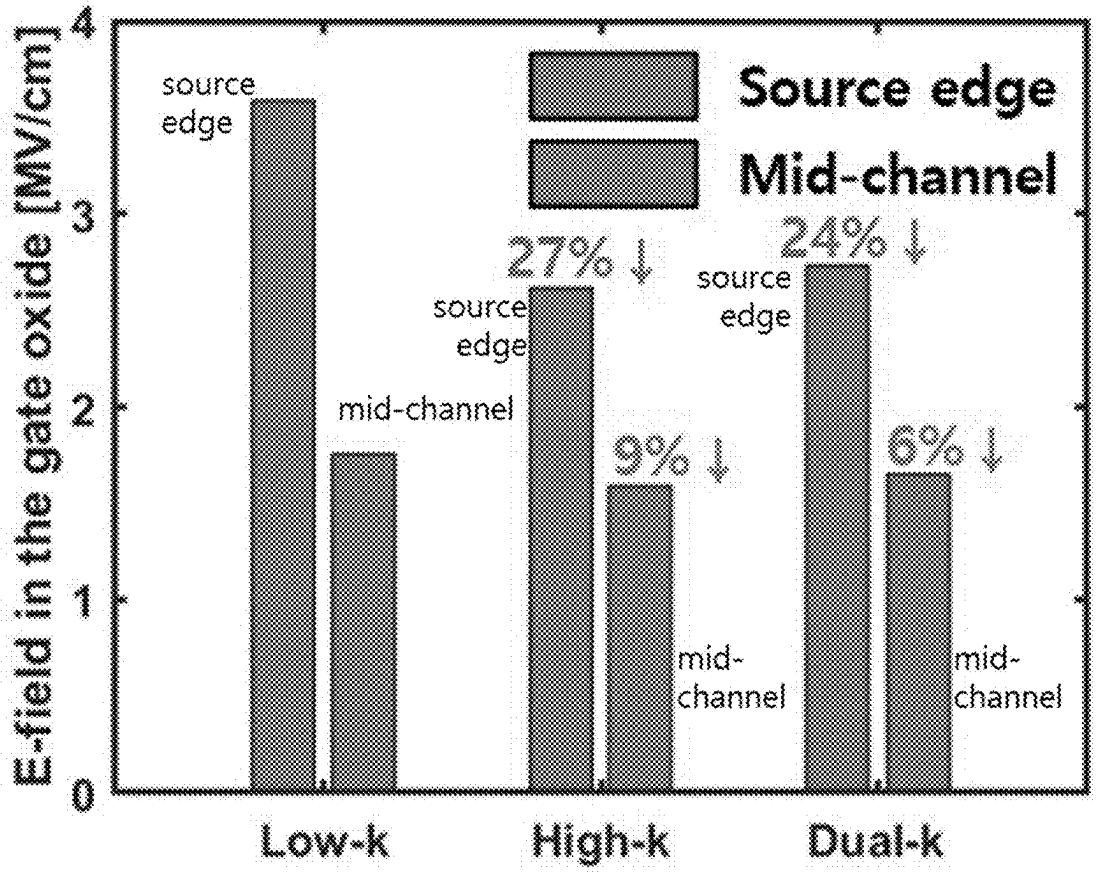
【Fig. 22】


(a)
TiN
Source
Drain
BOX
Low-k
(b)
High-k
(c)
Dual-k
Electric Field[MV/cm] (@V_{write}=5V)
0.000
1.586
3.173
4.759
6.345
7.932
9.518

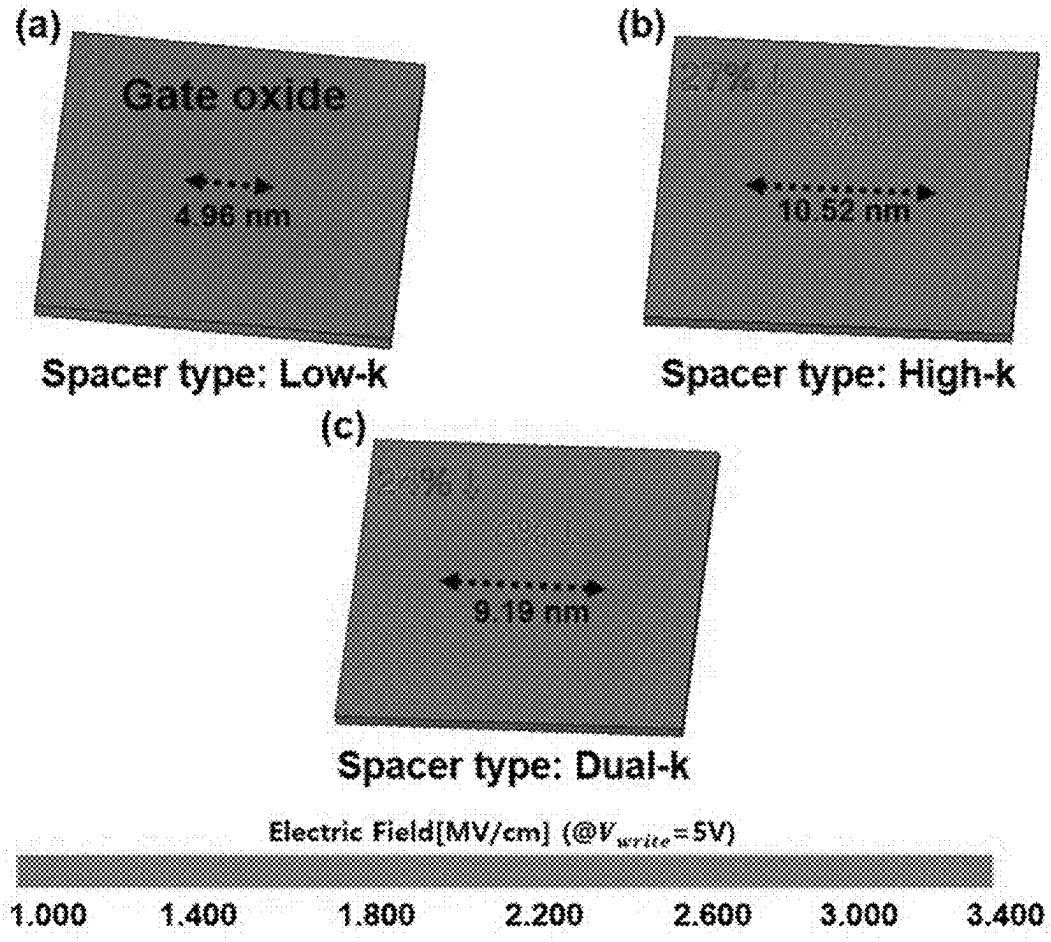
【Fig. 23】


E-field in the gate oxide [MV/cm]
Dielectric constant
Low-k
Dual-k
High-k
source edge
drain edge
mid-channel
ε = x-axis
ε = x-axis
ε = 22
mid-channel
source edge
drain edge
mid-channel
source edge
drain edge
4
3.5
3
2.5
2
1.5
0
5
10
15
20
25
30

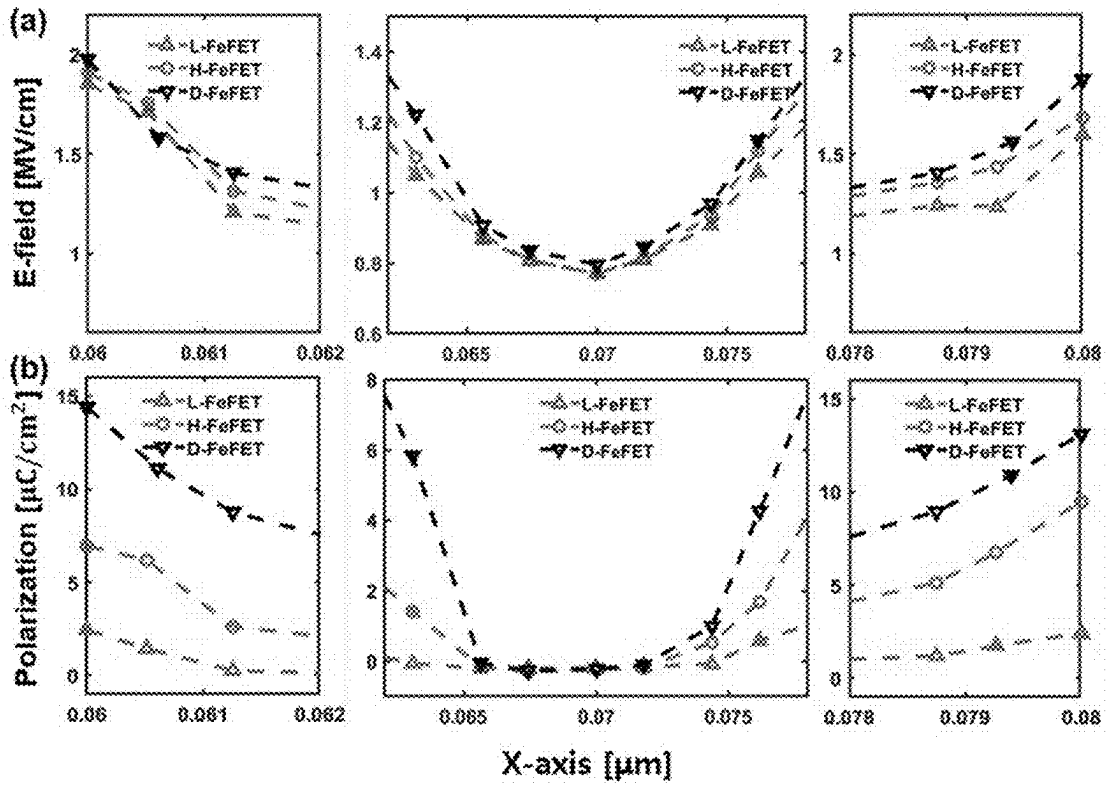
【Fig. 24】


E-field in the gate oxide [MV/cm]
0
1
2
3
4
Source edge
Mid-channel
source edge
mid-channel
27% ↓
source edge
9% ↓
mid-channel
24% ↓
source edge
6% ↓
mid-channel
Low-k
High-k
Dual-k

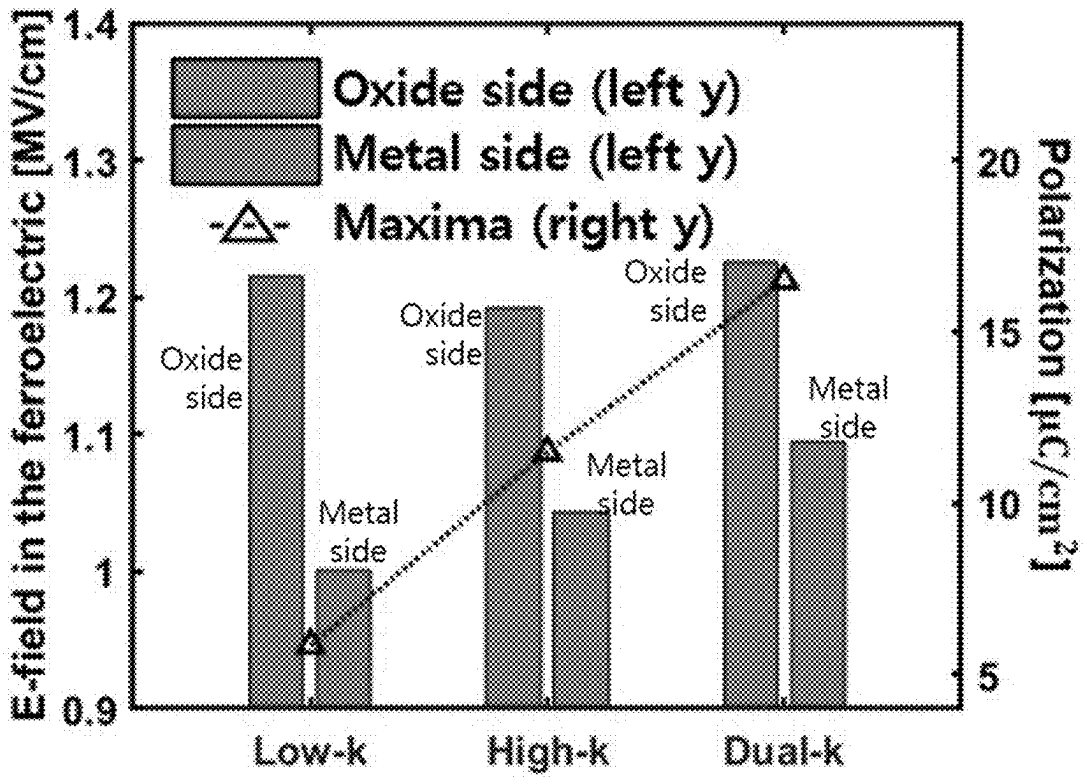
【Fig. 25】


(a)
Gate oxide
4.96 nm
Spacer type: Low-k
(b)
10.52 nm
Spacer type: High-k
(c)
9.19 nm
Spacer type: Dual-k
Electric Field[MV/cm] (@V_{write}=5V)
1.000
1.400
1.800
2.200
2.600
3.000
3.400

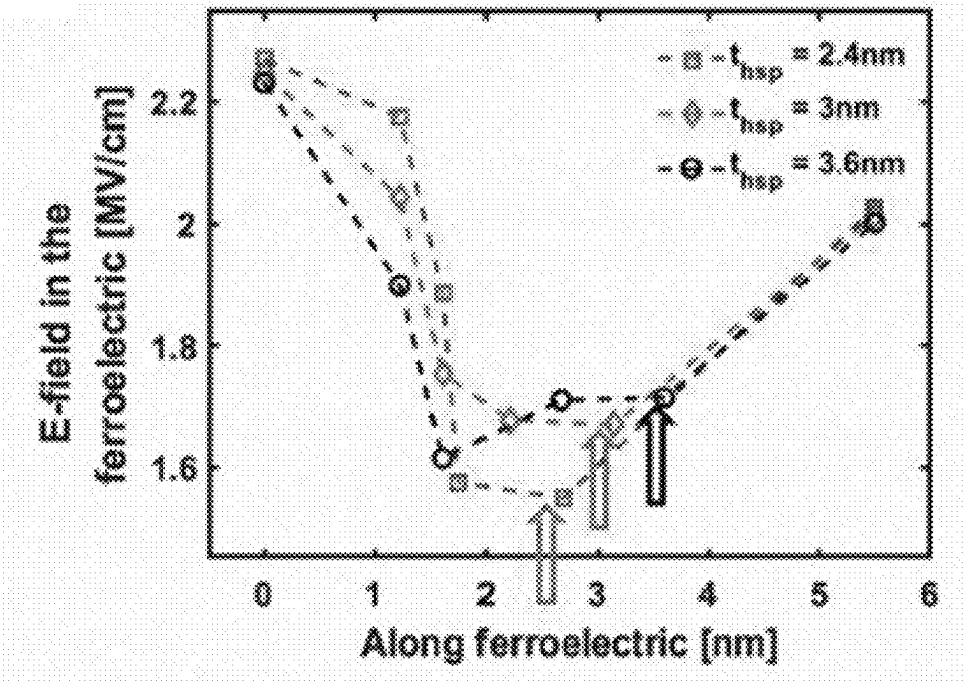
【Fig. 26】


(a)
E-field [MV/cm]
L-FeFET
H-FeFET
D-FeFET
(b)
Polarization [μC/cm²]
X-axis [μm]

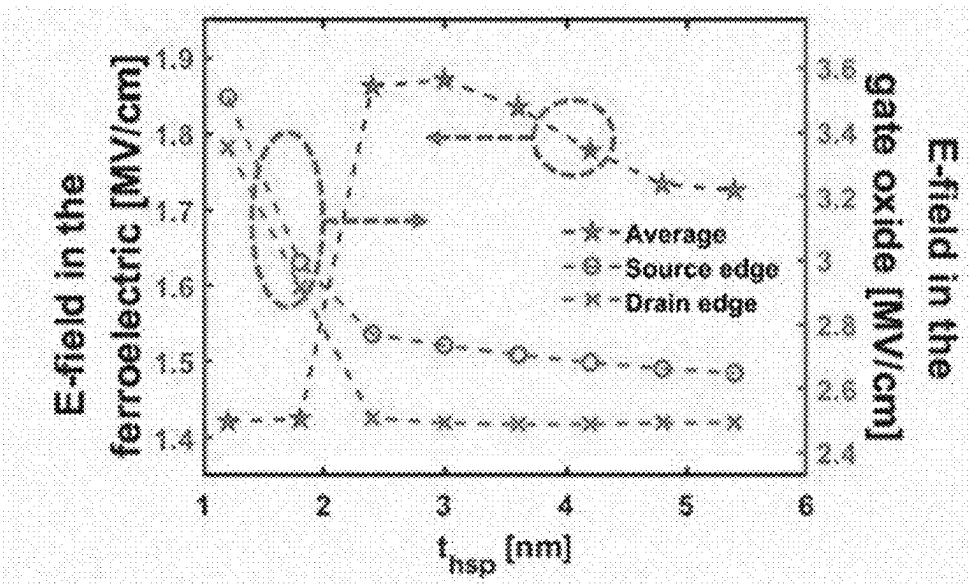
【Fig. 27】


E-field in the ferroelectric [MV/cm]
1.4
1.3
1.2
1.1
1
0.9
Polarization [μC/cm²]
20
15
10
5
Oxide side (left y)
Metal side (left y)
Maxima (right y)
Oxide side
Metal side
Oxide side
Metal side
Oxide side
Metal side
Low-k
High-k
Dual-k

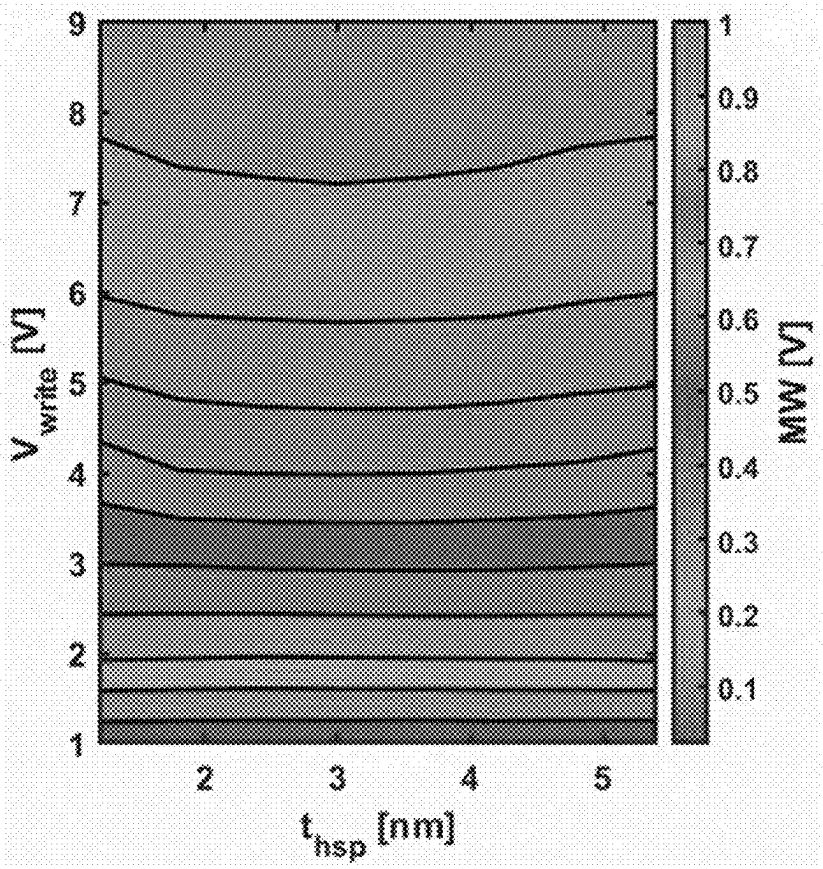
【Fig. 28(a)】



【Fig. 28(b)】



【Fig. 29】



FERROELECTRIC FIELD EFFECT TRANSISTOR WITH DOUBLE SPACER AND METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a ferroelectric field effect transistor and a method of manufacturing the same, and more specifically, to a ferroelectric field effect transistor equipped with a double spacer and a method of manufacturing the same.

2. Description of the Related Art

[0002] A ferroelectric field effect transistor is a memory device that adjusts a threshold voltage of the device using polarization recorded in a ferroelectric. In the initial ferroelectric field effect transistor, a perovskite material has been used as a ferroelectric layer, but the thickness of the ferroelectric layer exceeding hundreds of nm has acted as a limitation. Thereafter, as the ferroelectric property of hafnium oxide has been found, sufficient performance may be obtained even with the thickness of 1 to 10 nm. Accordingly, all the recent ferroelectric field effect transistors have been studied based on the hafnium oxide ferroelectric layer, and many studies have been conducted to maintain polarization due to repetition of a write operation and to improve power consumption and latency.

[0003] In the ferroelectric field effect transistor, a value of the threshold voltage of the device varies depending on the polarization of the ferroelectric layer. When the directions of the polarization are aligned from a gate to a channel, the threshold voltage is increased by deteriorating the ability to form an inversion layer of the channel, and when the directions of the polarization are aligned from the channel to the gate, the threshold voltage is decreased by improving the ability to form the inversion layer of the channel. In this case, a difference between two threshold voltages when the threshold voltage is maximally increased and when the threshold voltage is maximally decreased is referred to as a memory window. In the ferroelectric field effect transistor, the memory window is one of important performance indicators.

[0004] The polarization of the ferroelectric is determined by a write or erase operation. When a program (including writing and erasing) pulse is applied to the gate, an electric field is formed in the ferroelectric layer, and the polarization is aligned according to the magnitude and direction of the electric field. Thereafter, when the pulse application is stopped, the aligned polarization is maintained unlike general dielectrics. This may be represented by drawing a gap curve with the electric field and the polarization as a horizontal axis and a vertical axis, respectively. For this reason, the pulse application is inevitable in a program operation of the ferroelectric field effect transistor, and most of power is consumed when the pulse is applied. Accordingly, power consumption of the ferroelectric field effect transistor may be reduced by reducing the size and application time of the pulse. However, it is necessary to increase the magnitude and application time of the pulse in order to obtain a sufficient memory window, which is in deadlock with a method of reducing power consumption.

[0005] In studies that change the spacer of the existing ferroelectric field effect transistor, the material of the spacer has been changed from a silicon oxide-based low dielectric constant to a hafnium oxide-based high dielectric constant. Accordingly, a fringe electric field developed through the spacer has been suppressed, and an electric field of the gate dielectric film has been lowered. In particular, an electric field near the source and drain of the gate dielectric film has been significantly lowered. The electric field of the ferroelectric layer has been improved due to the lowered electric field of the gate dielectric film, and the polarization of the ferroelectric layer showed a greater value at the same write voltage. Accordingly, a high-k spacer ferroelectric field effect transistor may obtain a memory window that is larger than a low-k spacer field effect transistor, and there is an effect of reducing write energy due to a decrease in the write voltage in a situation where the same memory window is obtained. However, the high-k spacer increases a parasitic capacitance of the device, which is disadvantageous to the memory device that needs to perform a high-speed operation. In addition, the increased parasitic capacitance acts adversely on the write energy despite the decrease in the write voltage, and thus, when the thickness of the gate dielectric film is small, the amount of decrease in the write energy is not large.

SUMMARY OF THE INVENTION

[0006] One technical problem to be solved by the present invention is to provide a ferroelectric field effect transistor equipped with a double spacer and a method of manufacturing the same.

[0007] Another technical problem to be solved by the present invention is to provide a ferroelectric field effect transistor having a suppression effect and a method of manufacturing the same.

[0008] Still another technical problem to be solved by the present invention is to provide a ferroelectric field effect transistor having a relocation effect and a method of manufacturing the same.

[0009] Still another technical problem to be solved by the present invention is to provide a ferroelectric field effect transistor having a suppression effect and a relocation effect and a method of manufacturing the same.

[0010] Still another technical problem to be solved by the present invention is to provide a ferroelectric field effect transistor in which an electric field of a gate dielectric layer decreases, whereas an electric field of a ferroelectric layer increases, and a method of manufacturing the same.

[0011] Still another technical problem to be solved by the present invention is to provide a ferroelectric field effect transistor having an improved memory window and a method of manufacturing the same.

[0012] Still another technical problem to be solved by the present invention is to provide a ferroelectric field effect transistor having a decreased parasitic capacitance and a method of manufacturing the same.

[0013] Still another technical problem to be solved by the present invention is to provide a ferroelectric field effect transistor capable of decreasing a write voltage and write energy, and a method of manufacturing the same.

[0014] The technical problems to be solved by the present invention are not limited to those described above.

[0015] To solve the above-described technical problems, the present invention provides a ferroelectric field effect transistor.

[0016] According to one embodiment, the ferroelectric field effect transistor may include: a body layer including a source region, a drain region spaced apart from the source region, and an intermediate region disposed between the source region and the drain region; a gate structure including a gate dielectric layer, a ferroelectric layer, and a gate electrode which are sequentially stacked on the intermediate region of the body layer; and a double spacer disposed on a side wall of the gate structure, in which the double spacer includes a high-k lower spacer and a low-k upper spacer disposed on the lower spacer.

[0017] According to one embodiment, when a voltage is applied to the gate electrode, a relatively high electric field may be formed in the ferroelectric layer and a relatively low electric field may be formed in the gate dielectric layer.

[0018] According to one embodiment, a boundary surface between the lower spacer and the upper spacer may be located adjacent to the ferroelectric layer of the gate structure.

[0019] According to one embodiment, a side wall of the lower spacer may make contact with both a side wall of the gate dielectric layer and a side wall of the ferroelectric layer.

[0020] According to one embodiment, a side wall of the upper spacer may make contact with both a side wall of the ferroelectric layer and a side wall of the gate electrode.

[0021] According to one embodiment, a lower surface of the lower spacer may make contact with any one of the source region and the drain region.

[0022] According to one embodiment, the lower spacer may include hafnium oxide (HfO_2), and the upper spacer may include silicon oxide (SiO_2).

[0023] According to one embodiment, the gate dielectric layer may include silicon oxide (SiO_2).

[0024] According to one embodiment, the ferroelectric layer may include hafnium zirconium oxide (HZO).

[0025] According to one embodiment, the lower spacer may have a thickness greater than 2.4 nm and less than 3.6 nm.

[0026] To solve the above-described technical problems, the present invention provides a method of manufacturing a ferroelectric field effect transistor.

[0027] According to one embodiment, the method of manufacturing a ferroelectric field effect transistor may include: preparing a substrate; forming a body layer on the substrate; forming a gate structure, in which a gate dielectric layer, a ferroelectric layer, and a gate electrode are sequentially stacked, on an intermediate region of the body layer; forming a source region and a drain region by injecting a dopant into a first region of the body layer adjacent to one side of the gate structure and a second region of the body layer adjacent to the other side of the gate structure; forming a high-k lower spacer on the source region and the drain region; and forming a low-k upper spacer on the lower spacer.

[0028] According to one embodiment, the lower spacer may be formed such that a level of an upper surface of the lower spacer is located between levels of an upper surface and a lower surface of the ferroelectric layer.

[0029] According to one embodiment, the forming of the gate structure may include: forming the gate dielectric layer on the body layer; forming the ferroelectric layer on the gate dielectric layer; forming the gate electrode on the ferroelectric layer; and etching the gate dielectric layer, the ferroelectric layer, and the gate electrode such that the first region and the second region of the body layer are exposed to an outside.

[0030] According to one embodiment, the forming of the lower spacer may include: forming a high-k material layer on the body layer such that the source region, the drain region, and the gate structure are conformally covered with the high-k material layer; and etching the high-k material layer such that an upper portion and a part of a side wall of the gate structure are exposed.

[0031] The ferroelectric field effect transistor according to the embodiment of the present invention may include: a body layer including a source region, a drain region spaced apart from the source region, and an intermediate region disposed between the source region and the drain region; a gate structure including a gate dielectric layer, a ferroelectric layer, and a gate electrode which are sequentially stacked on the intermediate region of the body layer; and a double spacer disposed on a side wall of the gate structure, in which the double spacer includes a high-k lower spacer and a low-k upper spacer disposed on the lower spacer.

[0032] Accordingly, the electric field of the gate dielectric layer may decrease, whereas the electric field of the ferroelectric layer may increase, so that a memory window may be improved, a parasitic capacitance may be decreased, and a write voltage and write energy may be decreased.

BRIEF DESCRIPTION OF THE DRAWINGS

[0033] FIG. **1** is a flowchart for explaining a ferroelectric field effect transistor according to an embodiment of the present invention.

[0034] FIG. **2** is a view for specifically explaining a gate structure and a double spacer of the ferroelectric field effect transistor according to the embodiment of the present invention.

[0035] FIG. **3** is a flowchart for explaining a method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention.

[0036] FIG. **4** is a schematic view for explaining step S**100** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention.

[0037] FIG. **5** is a schematic view for explaining step S**200** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention.

[0038] FIG. **6** is a flowchart for more specifically explaining step S**300** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention.

[0039] FIG. **7** is a schematic view for explaining step S**310** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention.

[0040] FIG. **8** is a schematic view for explaining step S**320** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention.

[0041] FIG. **9** is a schematic view for explaining step S**330** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention.

[0042] FIG. **10** is a schematic view for explaining step S**335** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention.

[0043] FIG. **11** is a schematic view for explaining step S**340** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention.

[0044] FIG. **12** is a schematic view for explaining step S**400** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention.

[0045] FIG. **13** is a flowchart for more specifically explaining step S**500** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention.

[0046] FIG. **14** is a schematic view for explaining step S**510** in the method of manufacturing the ferroelectric field effect transistor to the embodiment of the present invention.

[0047] FIG. **15** is a schematic view for explaining step S**520** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention.

[0048] FIG. **16** is a flowchart for more specifically explaining step S**600** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention.

[0049] FIG. **17** is a schematic view for explaining step S**610** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention.

[0050] FIG. **18** is a schematic view for explaining step S**620** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention.

[0051] FIG. **19** is a schematic view for explaining step S**700** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention.

[0052] FIGS. **20**(*a*), **20**(*b*), **20**(*c*) and **21** are views comparing memory windows of ferroelectric field effect transistors according to an experimental example and comparative examples of the present invention.

[0053] FIG. **22** is a view for explaining an electric field distribution of the ferroelectric field effect transistors according to the experimental example and the comparative examples of the present invention.

[0054] FIGS. **23** and **24** are views for explaining electric fields shown in gate dielectric layers of the ferroelectric field effect transistors according to the experimental example and the comparative examples of the present invention.

[0055] FIG. **25** is a view for explaining a state where information of FIG. **23** is recorded together with a portion of the gate dielectric layer of FIG. **22**.

[0056] FIGS. **26** and **27** are views for explaining electric fields and polarization shown in ferroelectric layers of the ferroelectric field effect transistors according to the experimental example and the comparative examples of the present invention.

[0057] FIGS. **28**(*a*), **28**(*b*) and **29** are views comparing characteristics according to a thickness of a lower spacer of the ferroelectric field effect transistor according to the experimental example of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0058] Hereinafter, preferred embodiments of the present invention will be described in detail with reference to the accompanying drawings. However, the present invention may be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, the embodiments introduced herein are provided so that the disclosed contents may be thorough and complete and the spirit of the present invention may be sufficiently conveyed to those skilled in the art.

[0059] In the present specification, it will be understood that when an element is referred to as being "on" another element, it can be formed directly on the other element or intervening elements may be present. In the drawings, the thicknesses of layers and regions are exaggerated for clarity.

[0060] In addition, it will be also understood that although the terms first, second, third, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another element. Thus, a first element in some embodiments may be termed a second element in other embodiments without departing from the teachings of the present invention. Embodiments explained and illustrated herein include their complementary counterparts. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed elements.

[0061] The singular expression also includes the plural meaning as long as it does not differently mean in the context. In addition, the terms "comprise", "have" etc., of the description are used to indicate that there are features, numbers, steps, elements, or combination thereof, and they should not exclude the possibilities of combination or addition of one or more features, numbers, operations, elements, or a combination thereof. Furthermore, it will be understood that when an element is referred to as being "connected" or "coupled" to another element, it may be directly connected or coupled to the other element or intervening elements may be present.

[0062] In addition, when detailed descriptions of related known functions or constitutions are considered to unnecessarily cloud the gist of the present invention in describing the present invention below, the detailed descriptions will not be included.

[0063] FIG. **1** is a flowchart for explaining a ferroelectric field effect transistor according to an embodiment of the present invention, and FIG. **2** is a view for specifically explaining a gate structure and a double spacer of the ferroelectric field effect transistor according to the embodiment of the present invention.

[0064] Referring to FIGS. **1** and **2**, the ferroelectric field effect transistor to the embodiment may include a substrate **100**, a body layer **200**, a gate structure **300**, and a double spacer **400**. Hereinafter, the respective components will be described.

[0065] According to one embodiment, the substrate **100** may be a silicon semiconductor substrate. More specifically, the substrate **100** may be a substrate in which a silicon oxide (SiO_2) layer **120** is formed on a silicon (Si) substrate **110**. Alternatively, according to another embodiment, the substrate **100** may be a compound semiconductor substrate. Alternatively, according to still another embodiment, the substrate **100** may be a glass substrate. Alternatively, accord-

ing to still another embodiment, the substrate **100** may be a plastic substrate. The type of the substrate **100** is not limited.

[0066] The body layer **200** may be disposed on the substrate **100**. For example, the body layer **200** may include silicon (Si). According to one embodiment, the body layer **200** may include a source region S, a drain region D spaced apart from the source region S, and an intermediate region B disposed between the source region S and the drain region D. For example, the source region S may be a region in which a first dopant is injected into the body layer **200**, and the drain region D may be a region in which a second dopant is injected into the body layer **200**. Alternatively, the intermediate region B may be a region into which no dopant is injected.

[0067] The gate structure **300** may be disposed on the intermediate region B of the body layer **200**. The gate structure **300** may have a structure in which a gate dielectric layer **310**, a ferroelectric layer **320**, and a gate electrode **330** are sequentially stacked. That is, the gate dielectric layer **310** may be disposed on the intermediate region B of the body layer **200**, the ferroelectric layer **320** may be disposed on the gate dielectric layer **310**, and the gate electrode **330** may be disposed on the ferroelectric layer **320**. According to one embodiment, the gate dielectric layer **310** may include silicon oxide (SiO_2). According to one embodiment, the ferroelectric layer **320** may include hafnium zirconium oxide (HZO) or a material in which hafnium oxide is doped with silicon. According to one embodiment, the gate electrode **330** may include titanium nitride (TiN). In addition, although not shown, a capping layer including poly-Si may be disposed on the gate electrode **330**.

[0068] The double spacer **400** may be disposed on the source region S and/or the drain region D of the body layer **200**. In addition, the double spacer **400** may be disposed on a side wall of the gate structure **300**.

[0069] The double spacer **400** may include a lower spacer **410** and an upper spacer **420** disposed on the lower spacer **410**. According to one embodiment, the lower spacer **410** may include a high-k material. For example, the lower spacer **410** may include hafnium oxide (HfO_2). Alternatively, the upper spacer **420** may include a low-k material. For example, the upper spacer **420** may include silicon oxide (SiO_2).

[0070] According to one embodiment, a boundary surface IL between the lower spacer **410** and the upper spacer **420** may be located adjacent to the ferroelectric layer **200** of the gate structure **300**. That is, a level of the boundary surface IL between the lower spacer **410** and the upper spacer **420** may be located between levels of an upper surface **320***a* and a lower surface **320***b* of the ferroelectric layer **320**.

[0071] In addition, a side wall of the lower spacer **410** may make contact with both a side wall of the gate dielectric layer **310** and a side wall of the ferroelectric layer **320**, and a side wall of the upper spacer **420** may make contact with the side wall of the ferroelectric layer **320** and a side wall of the gate electrode **330**.

[0072] Through the structure as described above, in the ferroelectric field effect transistor according to the embodiment, an electric field of the gate dielectric layer **310** may decrease, but an electric field of the ferroelectric layer **320** may increase. Accordingly, a memory window may be improved, a parasitic capacitance may be decreased, and a write voltage and write energy may be decreased.

[0073] More specifically, the high-k lower spacer **410** may suppress a fringe electric field, so that it is possible to suppress the increase in the electric field of the gate dielectric layer **310** adjacent to the source region S and the drain region D. In describing the present specification, the above-described effect is defined as a "suppression effect".

[0074] In addition, as the level of the boundary surface IL between the lower spacer **410** and the upper spacer **420** is located between the levels of the upper surface **320***a* and the lower surface **320***b* of the ferroelectric layer **320**, the fringe electric field caused by the upper spacer **420** may be developed to a high value around the ferroelectric layer **320**, so that the electric field of the ferroelectric layer **320** may be increased. In describing the present specification, the above-described effect is defined as a "relocation effect".

[0075] That is, in the ferroelectric field effect transistor according to the embodiment, since the suppression effect and the relocation effect may be applied, the electric field of the gate dielectric layer **310** may decrease, whereas the electric field of the ferroelectric layer **320** may increase. Accordingly, a memory window may be improved, a parasitic capacitance may be decreased, and a write voltage and write energy may be decreased.

[0076] Hereinabove, the ferroelectric field effect transistor according to the embodiment of the present invention have been described. Hereinafter, a method of manufacturing a ferroelectric field effect transistor according to the embodiment of the present invention will be described.

[0077] FIG. **3** is a flowchart for explaining a method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention, FIG. **4** is a schematic view for explaining step S**100** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention, FIG. **5** is a schematic view for explaining step S**200** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention, FIG. **6** is a flowchart for more specifically explaining step S**300** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention, FIG. **7** is a schematic view for explaining step S**310** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention, FIG. **8** is a schematic view for explaining step S**320** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention, FIG. **9** is a schematic view for explaining step S**330** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention, FIG. **10** is a schematic view for explaining step S**335** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention, FIG. **11** is a schematic view for explaining step S**340** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention, FIG. **12** is a schematic view for explaining step S**400** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention, FIG. **13** is a flowchart for more specifically explaining step S**500** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention, FIG. **14** is a schematic view for explaining step S**510** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present

invention, FIG. **15** is a schematic view for explaining step S**520** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention, FIG. **16** is a flowchart for more specifically explaining step S**600** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention, FIG. **17** is a schematic view for explaining step S**610** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention, FIG. **18** is a schematic view for explaining step S**620** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention, FIG. **19** is a schematic view for explaining step S**700** in the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention.

[0078] Referring to FIGS. **3** and **4**, a substrate **100** may be prepared (S**100**). According to one embodiment, the substrate **100** may be a silicon semiconductor substrate. More specifically, the substrate **100** may be a substrate in which a silicon oxide (SiO_2) layer **120** is formed on a silicon (Si) substrate **110**. Alternatively, according to another embodiment, the substrate **100** may be a compound semiconductor substrate. Alternatively, according to still another embodiment, the substrate **100** may be a glass substrate. Alternatively, according to still another embodiment, the substrate **100** may be a plastic substrate. The type of the substrate **100** is not limited.

[0079] Referring to FIGS. **3** and **5**, a body layer **200** may be formed on the substrate **100** (S**200**). According to one embodiment, the body layer **200** may include silicon (Si).

[0080] Referring to FIGS. **6** and **7**, a ferroelectric layer **310** may be formed on the gate electrode **200** (S**310**). According to one embodiment, the gate dielectric layer **310** may include silicon oxide (SiO_2). According to one embodiment, the gate dielectric layer **310** may be formed by rapid thermal oxidation of the body layer **200**.

[0081] Referring to FIGS. **6** and **8**, a ferroelectric layer **320** may be formed on the gate dielectric layer **310** (S**320**). According to one embodiment, the ferroelectric layer **320** may include hafnium zirconium oxide (HZO). Alternatively, according to another embodiment, the ferroelectric layer **320** may be a material in which hafnium oxide is doped with silicon. According to one embodiment, the ferroelectric layer **320** may be formed by atomic layer deposition (ALD).

[0082] Referring to FIGS. **6** and **9**, a gate electrode **330** may be formed on the ferroelectric layer **320**. According to one embodiment, the gate electrode **330** may include titanium nitride (TiN). According to one embodiment, the gate electrode **330** may be formed by plasma vapor deposition (PVD).

[0083] Referring to FIG. **10**, a capping layer **335** may be formed on the gate electrode **330** (S**335**). Accordingly, a gate structure **300**, in which the gate dielectric layer **310**, the ferroelectric layer **320**, the gate electrode **330**, and the capping layer **335** are sequentially stacked, may be formed on the body layer **200**. According to one embodiment, the capping layer **335** may include poly-Si. According to one embodiment, the gate electrode **335** may be formed by chemical vapor deposition (CVD).

[0084] Referring to FIGS. **6** and **11**, the gate dielectric layer **310**, the ferroelectric layer **320**, the gate electrode **330**, and the capping layer **335** may be etched such that a first region **200***a* and a second region **200***b* of the body layer **200** are exposed to the outside. Accordingly, the first region **200***a* and the second region **200***b* of the body layer **200** may be exposed to the outside, whereas a region **200***c* between the first region **200***a* and the second region **200***b* may not be exposed by the gate structure **300**. According to one embodiment, the first region **200***a* may be a region adjacent to one side of the body layer **200**. On the other hand, the second region **200***b* may be a region adjacent to the other side of the body layer **200**.

[0085] Referring to FIGS. **3** and **12**, dopants may be injected into the first region **200***a* of the body layer **200** adjacent to one side of the gate structure **300** and the second region **200***b* of the body layer **200** adjacent to the other side of the gate structure **300**, respectively. Therefore, a source region S and a domain region D may be formed (S**400**). In other words, the first region **200***a* may be converted into the source region S by injecting the dopant into the first region **200***a*, and the second region **200***b* may be converted into the drain region D by injecting the dopant into the second region **200***b*. The region **200***c* between the first region **200***a* and the second region **200***b* may maintain the original state of the body layer **200** because the dopant is not injected, which may be defined as an intermediate region B.

[0086] Referring to FIGS. **13** and **14**, a high-k material layer HL may be formed on the body layer **200** such that the source region S, the drain region D, and the gate structure **300** are conformally covered with the high-k material layer HL (S**510**). According to one embodiment, the high-k material layer HL may include hafnium oxide (HfO_2). According to one embodiment, the high-k material layer HL may be formed by atomic layer deposition (ALD).

[0087] Referring to FIGS. **13** and **15**, the high-k material layer HL may be etched such that an upper portion and a part of the side wall of the gate structure **300** are exposed (S**520**). Accordingly, the high-k material layer HL may remain only on the source region S and the drain region D of the body layer **200**, and the remaining high-k material layer HL may be defined as a lower spacer **410**. According to one embodiment, the lower spacer **410** may be formed such that a level of an upper surface of the lower spacer is located between levels of an upper surface and a lower surface of the ferroelectric layer **320**.

[0088] Referring to FIGS. **16** and **17**, a low-k material layer LL may be formed on the lower spacer **410** and the gate structure **300** such that the exposed upper portion and side wall of the gate structure **300** are covered with the low-k material layer LL (S**610**). According to one embodiment, the low-k material layer LL may include silicon oxide (SiO_2). According to one embodiment, the low-k material layer LL may be formed by atomic layer deposition (ALD).

[0089] Referring to FIGS. **16** and **18**, the low-k material layer LL may be planarized (S**620**). According to one embodiment, the low-k material layer LL disposed on the gate structure **300** may be removed, and a level of the upper surface of the low-k material layer LL may be planarized to be the same as the level of the upper surface of the gate structure **300**. Accordingly, the low-k material layer LL may remain only on the lower spacer **410**, and the low dielectric material layer LL remaining on the lower spacer **410** may be defined as an upper spacer **420**.

[0090] Referring to FIG. **19**, the upper spacer **420** and the lower spacer **410** may be etched to expose a part of the source region S and a part of the drain region D (S**700**).

Accordingly, the ferroelectric field effect transistor according to the embodiment may be manufactured.

[0091] Hereinabove, the ferroelectric field effect transistor and the method of manufacturing the ferroelectric field effect transistor according to the embodiment of the present invention have been described. Hereinafter, specific experimental examples and characteristic evaluation results of the ferroelectric field effect transistor according to the embodiment of the present invention will be described.

Experimental Example 1: Manufacture of Ferroelectric Field Effect Transistor

[0092] A ferroelectric field effect transistor was manufactured by the method described with reference to FIGS. **3** to **19**. Materials used as respective components of the ferroelectric field effect transistor are summarized through <Table 1> below, and various parameters of the ferroelectric field effect transistor according to an experimental example are summarized through <Table 2>. below.

TABLE 1

Classification	Material
Substrate	SOI (Si/SiO_2)
Body layer	Si
Gate dielectric layer	SiO_2
Ferroelectric layer	HZO
Gate electrode	TiN
Lower spacer	HfO_2
Upper spacer	SiO_2

TABLE 2

Parameter	Value
Length of gate electrode (L_g, nm)	20
Width of channel (W_{ch}, nm)	20
Thickness of channel (T_{ch}, nm)	5
Thickness of substrate (T_{BOX}, nm)	25
*** (L_{sp}, nm)	10
Thickness of gate dielectric layer (T_{ox}, nm)	0.6
Thickness of ferroelectric layer (T_{fe}, nm)	5.5
WF (eV)	4.38
S/D doping (cm^{-3})	4e20
Channel doping (cm^{-3})	2e14
Substrate doping (cm^{-3})	2e20
Remanent polarization (P_r, $\mu C/cm^2$)	19.5
Saturation polarization (Ps, $\mu C/cm^2$)	19.8
Coercive electric field (E_c, MV/cm)	1.45

Experimental Example 2: Confirmation of Memory Window of Ferroelectric Field Effect Transistor

[0093] To confirm memory window superiority of the ferroelectric field effect transistor according to the experimental example, the ferroelectric field effect transistor according to the experimental was compared with the example ferroelectric field effect transistors according to comparative examples. Specifically, as the ferroelectric field effect transistor according to Comparative Example 1, a transistor having the same structure as the ferroelectric field effect transistor according to the above-described experimental example and using a high-k single spacer (HfO_2) instead of a double spacer was prepared. In addition, as the ferroelectric field effect transistor according to Comparative Example 2, a transistor having the same structure as the ferroelectric field effect transistor according to the above-described experimental example and using a low-k single spacer (SiO_2) instead of a double spacer was prepared. In describing Experimental Example 2, the ferroelectric field effect transistor according to the experimental example is defined as D-FeFET, the ferroelectric field effect transistor according to Comparative Example 1 is defined as H-FeFET, and the ferroelectric field effect transistor according to Comparative Example 2 is defined as L-FeFET.

[0094] FIGS. **20**(*a*), **20**(*b*), **20**(*c*) and **21** are views comparing memory windows of ferroelectric field effect transistors according to the experimental example and the comparative examples of the present invention.

[0095] FIG. **20**(*a*) shows a memory window, a write energy distribution, and a pareto front of each of the ferroelectric transistor field effect transistors according to the experimental example and the comparative examples, FIG. **20**(*b*) shows comparison of memory windows according to a thickness of a gate dielectric layer of each of the ferroelectric field effect transistors at the same write voltage, and FIG. **20**(*c*) shows comparison of write energy consumption according to a thickness of the gate dielectric layer of each of the ferroelectric field effect transistors in order to secure the same memory window.

[0096] In addition, a memory window obtained under the condition of a thickness of a gate dielectric layer of 0.6 nm and a write voltage of 5 V, a maximum memory window that may be obtained, write energy for obtaining a memory window at 0.8 V, and write energy for obtaining a maximum memory window were measured from each ferroelectric field effect transistor, and the measured results thereof are summarized in <Table 3> below.

TABLE 3

Classification	Comparative Example 2 (L-FeFET)	Comparative Example 1 (H-FeFET)	Experimental Example (D-FeFET)	Enhancement [L/H]
MW (@V_{write} = 5 V) [V]	0.63	0.73	0.84	33.3%/15.1%
MW (maximum) [V]	0.90	0.98	1.05	16.7%/7.14%

TABLE 3-continued

Classification	Comparative Example 2 (L-FeFET)	Comparative Example 1 (H-FeFET)	Experimental Example (D-FeFET)	Enhancement [L/H]
E_{write} (@MW = 0.8 V) [nJ]	3.35	3.38	1.74	48.1%/48.5%
E_{write} (@maimum MW) [nJ]	5.31	8.34	6.42	−20.9%/23.0%

[0097] As can be seen from FIGS. **20**(*a*) to **20**(*c*), it can be seen that the ferroelectric field effect transistor (double spacer) according to the experimental example may acquire the highest memory window at the same write voltage as compared to the ferroelectric field effect transistors (single spacers) according to the comparative examples, and the same memory window may be secured at the lowest write voltage. In addition, it can be seen that the pareto front between the memory window and the write energy is expanded in the ferroelectric field effect transistor (double spacer) according to the experimental example as compared to the ferroelectric field effect transistors (single spacers) according to the comparative examples.

[0098] More specifically, as can be seen from FIG. **20**(*a*), it can be seen that the ferroelectric field effect transistor according to the experimental example has the widest pareto front. In addition, in the case of the maximum memory window that may be obtained from the ferroelectric field effect transistors (single spacers) according to the comparative examples, it can be seen that the ferroelectric field effect transistor (double spacer) according to the experimental example may be obtained using write energy that is decreased by 46% and 54%.

[0099] As can be seen in FIG. **20**(*b*), it can be quantitatively seen that the ferroelectric field effect transistor (double spacer) according to the experimental example has a memory window that is improved by at least 15% as compared to the ferroelectric field effect transistors (single spacers) according to the comparative examples, and particularly, has a memory window that is improved by 28% to 49% as compared to the ferroelectric field effect transistor according to Comparative Example 2 (low-k single spacer).

[0100] In addition, in the ferroelectric field effect transistor (low-k single spacer) according to Comparative Example 2 in which a suppression effect is not effective, it can be seen that the memory window is clearly attenuated according to the thickness of the gate dielectric layer. On the other hand, it can be seen that the ferroelectric field effect transistor (high-k single spacer) according to Comparative Example 1 and the ferroelectric field effect transistor (double spacer) according to the experimental example have an effective suppression effect, so that the memory window is gradually attenuated according to the thickness of the gate dielectric film, and the two structures are attenuated in a similar tendency.

[0101] As can be seen in FIG. **20**(*c*), it can be seen that the ferroelectric field effect transistor (double spacer) according to the experimental example has a lowered write voltage, the write energy is significantly reduced by the lowered gate capacitance as compared to the ferroelectric field effect transistor (high-k single spacer) according to Comparative Example 1, and the write energy is decreased by 47% or greater as compared to the ferroelectric field effect transistors (single spacers) according to the comparative examples.

[0102] It can be seen that the ferroelectric field effect transistor (high-k single spacer) according to Comparative Example 1 has a little decrease in write energy at a thickness of a gate dielectric layer of 0.8 nm or less as compared to the ferroelectric field effect transistor (low-k single spacer) according to Comparative Example 2, and at 1 nm or greater, the write voltage increase dominantly acts as compared to a decrease in gate capacitance of the ferroelectric field effect transistor (low-k single spacer) according to Comparative Example 2, so that the write energy decreases only 11.9% due to the increase in write energy.

[0103] Referring to FIG. **21**, a read operation is performed after a write operation, the read operation is performed after an erase operation, a threshold voltage according to a state of the transistor is measured during the read operation, and a size of the memory window according to the thickness of the gate dielectric layer and a magnitude of the write voltage is indicated by a contour. In more detail, FIG. **21**(*a*) shows a memory window size of the ferroelectric field effect transistor according to Comparative Example 2, FIG. **21**(*b*) shows a memory window size of the ferroelectric field effect transistor according to Comparative Example 1, and FIG. **21**(*c*) shows a memory window size of the ferroelectric field effect transistor according to the experimental example.

[0104] As can be seen from FIGS. **21**(*a*) to **21**(*c*), in the field effect transistor (low-k single spacer) according to Comparative Example 2, it can be seen that the memory window is clearly attenuated according to the thickness of the gate dielectric layer as compared to the other two structures. This is because the electric field of the gate dielectric layer varies depending on the thickness of the gate dielectric layer due to characteristics of the low-k single spacer structure in which the suppression effect is not effective.

[0105] In the two structures in which the suppression effect is effective (Comparative Example 1 and the experimental example), it can be seen that the influence on the memory window according to the thickness of the gate dielectric layer is reduced. In addition, the memory window may be obtained the highest in the ferroelectric field effect transistor (double spacer) according to the experimental example due to the relocation effect, and it can be seen that a change in the memory window according to an increase in the write voltage is the clearest. It can be seen that the ferroelectric field effect transistor (double spacer) according to the experimental example is the only one having a memory window at 1 V or greater, the ferroelectric field (low-k single spacer) according to effect transistor Comparative Example 1 requires a write voltage of 7-8 V to have a memory window at 0.8 V, the ferroelectric field effect

transistor (high-k single spacer) according to Comparative Example 2 requires a write voltage of 6 V, and the ferroelectric field effect transistor (double spacer) according to the experimental example requires a write voltage of 5 V.

Experimental Example 3: Confirmation of Electric Field Distribution and Polarization of Ferroelectric Field Effect Transistor

[0106] FIG. **22** is a view for explaining an electric field distribution of the ferroelectric field effect transistors according to the experimental example and the comparative examples of the present invention, FIGS. **23** and **24** are views for explaining electric fields shown in gate dielectric layers of the ferroelectric field effect transistors according to the experimental example and the comparative examples of the present invention, FIG. **25** is a view for explaining a state where information of FIG. **23** is recorded together with a portion of the gate dielectric layer of FIG. **22**, and FIGS. **26** and **27** are views for explaining electric fields and polarization shown in ferroelectric layers of the ferroelectric field effect transistors according to the experimental example and the comparative examples of the present invention.

[0107] FIG. **22** shows an electric field distribution during the application of the write voltage of the ferroelectric field effect transistors according to the experimental example and the comparative examples. In more detail, FIG. **22**(*a*) shows an electric field distribution of the ferroelectric field effect transistor according to Comparative Example 2, FIG. **22**(*b*) shows an electric field distribution of the ferroelectric field effect transistor according to Comparative Example 1, and FIG. **22**(*c*) shows an electric field distribution of the ferroelectric field effect transistor according to the experimental example.

[0108] FIGS. **22** to **25** show an electric field of the gate dielectric layer that is divided into the vicinity of a source/drain and the vicinity of the center of a channel while changing a dielectric constant, and FIGS. **26** and **27** show an electric field (upper side) of the ferroelectric layer and polarization (lower side) of the ferroelectric layer.

[0109] As can be seen from FIGS. **22** to **27**, it can be seen that the ferroelectric field effect transistor (high-k single spacer) according to Comparative Example 1 and the ferroelectric field effect transistor (double spacer) according to the experimental example have a low electric field in the vicinity of the source/drain and the vicinity of the center of the channel due to the suppression effect. However, in the ferroelectric field effect transistor (low-k single spacer) according to Comparative Example 2, it can be seen that the electric field of the gate dielectric layer in the vicinity of the source/drain is high and the electric field in the vicinity of the center of the channel is also increased by a certain value. Accordingly, it can be seen that the ferroelectric field effect transistor (high-k single spacer) according to Comparative Example 1 and the ferroelectric field effect transistor (double spacer) according to the experimental example have an effective suppression effect.

[0110] In addition, it can be seen that the gate dielectric layer electric fields of the ferroelectric field effect transistor (high-k single spacer) according to Comparative Example 1 and the ferroelectric field effect transistor (double spacer) according to the experimental example are similar, but the electric field of the ferroelectric layer is higher in the field effect transistor (double spacer) according to the experimental example. This is due to the relocation effect, that the electric field of the and it can be seen ferroelectric layer is formed higher, so the that polarization is also formed high.

Experimental Example 4: Confirmation of Optimal Thickness of Lower Spacer of Ferroelectric Field Effect Transistor

[0111] FIGS. **28** and **29** are views comparing characteristics according to a thickness of a lower spacer of the ferroelectric field effect transistor according to the experimental example of the present invention.

[0112] FIG. **28**(*a*) shows changes in electric fields (E-field in the ferroelectric, MV/cm) according to a thickness of the lower spacer (t_{hsp}=2.4 nm, 3 nm, and 3.6 nm) within a thickness range (Along ferroelectric, nm) of the ferroelectric layer.

[0113] As can be seen in FIG. **28**(*a*), it can be seen that the electric field is rapidly decreased until the thickness of the ferroelectric layer is equal to the thickness of the lower spacer, and the substantially constant electric field is maintained, and then the electric field gradually increases from a range in which the thickness of the ferroelectric layer becomes thicker than the thickness of the lower spacer. That is, it can be seen that the electric field of the ferroelectric layer is improved as the relocation effect occurs at a position where a boundary surface between the lower spacer and the upper spacer is located.

[0114] FIG. **28**(*b*) shows changes in the electric field in the ferroelectric layer (E-filed in the ferroelectric, MV/cm) and electric fields in the gate dielectric layer (E-filed in the gate oxide, MV/cm) according to a thickness of the lower spacer (t_{hsp}, nm). The electric field change in the gate dielectric layer represents a value measured at a source edge and a value measured at a drain edge, and the electric field change in the ferroelectric layer represents an average value.

[0115] As can be seen in FIG. **28**(*b*), it can be seen that the electric field in the gate dielectric layer is rapidly increased as the thickness of the lower spacer is about 2 nm or greater, and then is decreased again as the thickness of the lower spacer exceeds 3 nm. In addition, it can be seen that the electric field change in the gate dielectric layer continuously decreases until the thickness of the lower spacer is about 2.4 nm and then becomes saturated (substantially constant electric field is maintained).

[0116] FIG. **29** shows a relationship between a write voltage (V_{write}, V) and a thickness (t_{hsp}, nm) of the lower spacer. Specific values between the write voltage (V_{write}, V) and the thickness (t_{hsp}, nm) of the lower spacer are summarized in <Table 4> and <Table 5>.

TABLE 4

Classification	t_{hsp} = 1.2 nm	t_{hsp} = 1.8 nm	t_{hsp} = 2.4 nm	t_{hsp} = 3.0 nm
V_{write} = 1 V	0.029524	0.028121	0.027394	0.028304
V_{write} = 2 V	0.323524	0.318116	0.312221	0.313915
V_{write} = 3 V	0.502151	0.505131	0.512569	0.515983
V_{write} = 4 V	0.649411	0.695688	0.701264	0.703189
V_{write} = 5 V	0.794197	0.82459	0.836832	0.841625
V_{write} = 6 V	0.905018	0.925618	0.927013	0.929314
V_{write} = 7 V	0.963076	0.98403	0.991746	0.991238
V_{write} = 8 V	1.014427	1.02492	1.029965	1.034247
V_{write} = 9 V	1.038599	1.047153	1.044365	1.046164

TABLE 5

Classification	t_{hsp} = 3.6 nm	t_{hsp} = 4.2 nm	t_{hsp} = 4.8 nm	t_{hsp} = 5.4 nm
V_{write} = 1 V	0.02549	0.02871	0.025589	0.023459
V_{write} = 2 V	0.316829	0.318818	0.319879	0.326007
V_{write} = 3 V	0.517176	0.515179	0.50856	0.50125
V_{write} = 4 V	0.7008	0.69188	0.68364	0.65991
V_{write} = 5 V	0.8418	0.83272	0.81748	0.80675
V_{write} = 6 V	0.92642	0.92518	0.911745	0.9013
V_{write} = 7 V	0.988747	0.98255	0.97364	0.976434
V_{write} = 8 V	1.030703	1.028557	1.016731	1.008829
V_{write} = 9 V	1.04722	1.044336	1.038088	1.03558

[0117] As can be seen from FIG. **29**, <Table 4>, and <Table 5>, it can be seen that when the thickness of the lower spacer is 3 nm, an increase rate of the memory window according to the increase in the write voltage is the highest.

[0118] As a result, it is found through Experimental Example 4 that optimization for the thickness of the lower spacer is required. Specifically, it can be seen that the optimal thickness of the lower spacer for improving characteristics of the ferroelectric layer field effect transistor is 3 nm, a lower limit value is 2.4 nm, and an upper limit value is 3.6 nm.

[0119] While the present invention has been described in connection with the embodiments, it is not to be limited thereto but will be defined by the appended claims. In addition, it is to be understood that those skilled in the art can substitute, change, or modify the embodiments in various forms without departing from the scope and spirit of the present invention.

What is claimed is:

1. A ferroelectric field effect transistor comprising:

a body layer including a source region, a drain region spaced apart from the source region, and an intermediate region disposed between the source region and the drain region;

a gate structure including a gate dielectric layer, a ferroelectric layer, and a gate electrode which are sequentially stacked on the intermediate region of the body layer; and

a double spacer disposed on a side wall of the gate structure,

wherein the double spacer includes a high-k lower spacer and a low-k upper spacer disposed on the lower spacer.

2. The ferroelectric field effect transistor of claim **1**, wherein, when a voltage is applied to the gate electrode, a relatively high electric field is formed in the ferroelectric layer and a relatively low electric field is formed in the gate dielectric layer.

3. The ferroelectric field effect transistor of claim **1**, wherein a boundary surface between the lower spacer and the upper spacer is located adjacent to the ferroelectric layer of the gate structure.

4. The ferroelectric field effect transistor of claim **1**, wherein a side wall of the lower spacer makes contact with both a side wall of the gate dielectric layer and a side wall of the ferroelectric layer.

5. The ferroelectric field effect transistor of claim **1**, wherein a side wall of the upper spacer makes contact with both a side wall of the ferroelectric layer and a side wall of the gate electrode.

6. The ferroelectric field effect transistor of claim **1**, wherein a lower surface of the lower spacer makes contact with any one of the source region and the drain region.

7. The ferroelectric field effect transistor of claim **1**, wherein the lower spacer includes hafnium oxide (HfO_2), and the upper spacer includes silicon oxide (SiO_2).

8. The ferroelectric field effect transistor of claim **1**, wherein the gate dielectric layer includes silicon oxide (SiO_2).

9. The ferroelectric field effect transistor of claim **1**, wherein the ferroelectric layer includes hafnium zirconium oxide (HZO).

10. The ferroelectric field effect transistor of claim **1**, wherein the lower spacer has a thickness greater than 2.4 nm and less than 3.6 nm.

11. A method of manufacturing a ferroelectric field effect transistor, the method comprising:

preparing a substrate;

forming a body layer on the substrate;

forming a gate structure, in which a gate dielectric layer, a ferroelectric layer, and a gate electrode are sequentially stacked, on an intermediate region of the body layer;

forming a source region and a drain region by injecting a dopant into a first region of the body layer adjacent to one side of the gate structure and a second region of the body layer adjacent to the other side of the gate structure;

forming a high-k lower spacer on the source region and the drain region; and

forming a low-k upper spacer on the lower spacer.

12. The method of claim **11**, wherein the lower spacer is formed such that a level of an upper surface of the lower spacer is located between levels of an upper surface and a lower surface of the ferroelectric layer.

13. The method of claim **11**, wherein the forming of the gate structure includes:

forming the gate dielectric layer on the body layer;

forming the ferroelectric layer on the gate dielectric layer;

forming the gate electrode on the ferroelectric layer; and

etching the gate dielectric layer, the ferroelectric layer, and the gate electrode such that the first region and the second region of the body layer are exposed to an outside.

14. The method of claim **11**, wherein the forming of the lower spacer includes:

forming a high-k material layer on the body layer such that the source region, the drain region, and the gate structure are conformally covered with the high-k material layer; and

etching the high-k material layer such that an upper portion and a part of a side wall of the gate structure are exposed.

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