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(54) **COLOR CONVERSION SUBSTRATE, DISPLAY DEVICE INCLUDING THE SAME, AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE**

(71) Applicant: **Samsung Display Co., LTD.**, Yongin-si (KR)

(72) Inventors: **KANGMOON JO**, Yongin-si (KR); **SUNKWANG KIM**, Yongin-si (KR); **SEUNGHYUN PARK**, Yongin-si (KR); **HYUNGJIN SONG**, Yongin-si (KR); **DONG-YOON LEE**, Yongin-si (KR); **SEONGYOUNG LEE**, Yongin-si (KR)

(73) Assignee: **Samsung Display Co., LTD.**, Yongin-si (KR)

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CPC ***H10K 59/38*** (2023.02); ***H10K 59/8792*** (2023.02)

(57) **ABSTRACT**

The color conversion substrate includes a first color filter having a first opening defining a second opening area, a second color filter having a second opening defining a third opening area, and a third color filter having a third opening defining a first opening area, and the first color filter does not overlap a light blocking area surrounding the third opening area.

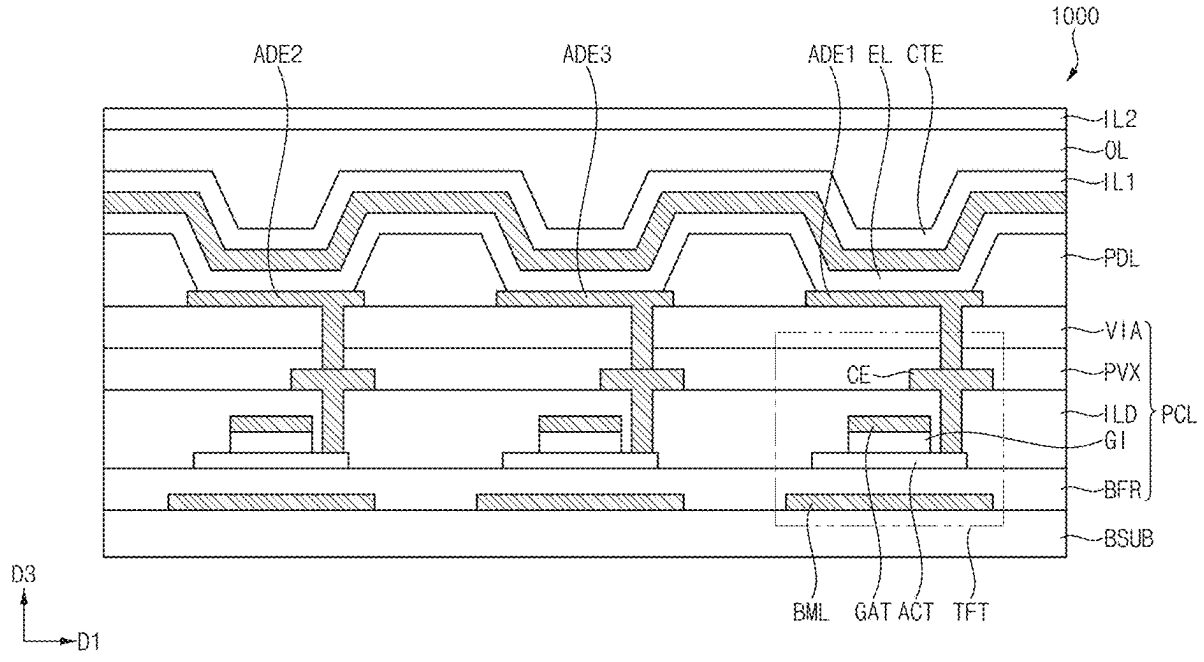


FIG. 1

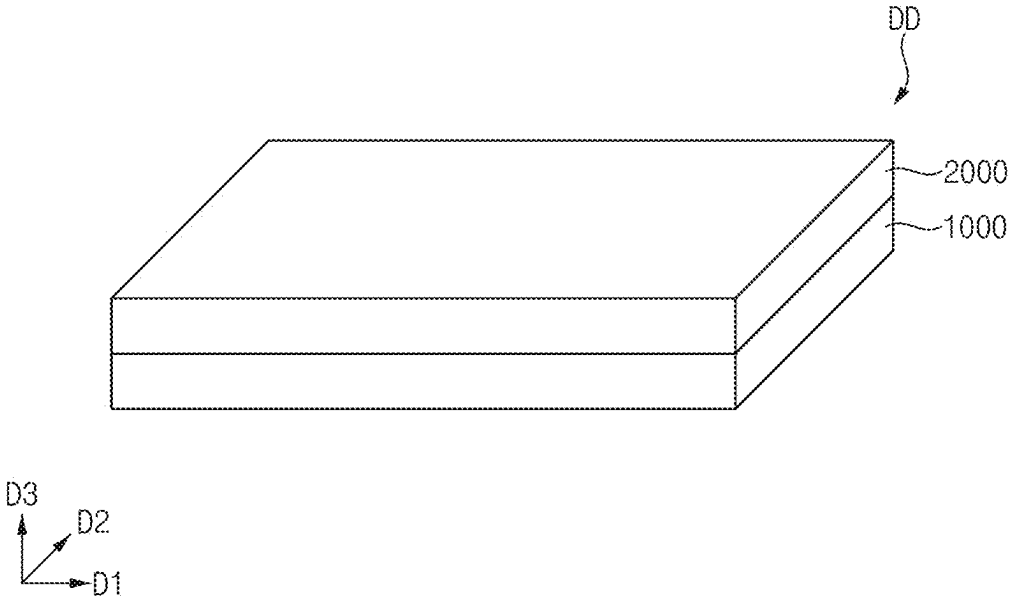


FIG. 2

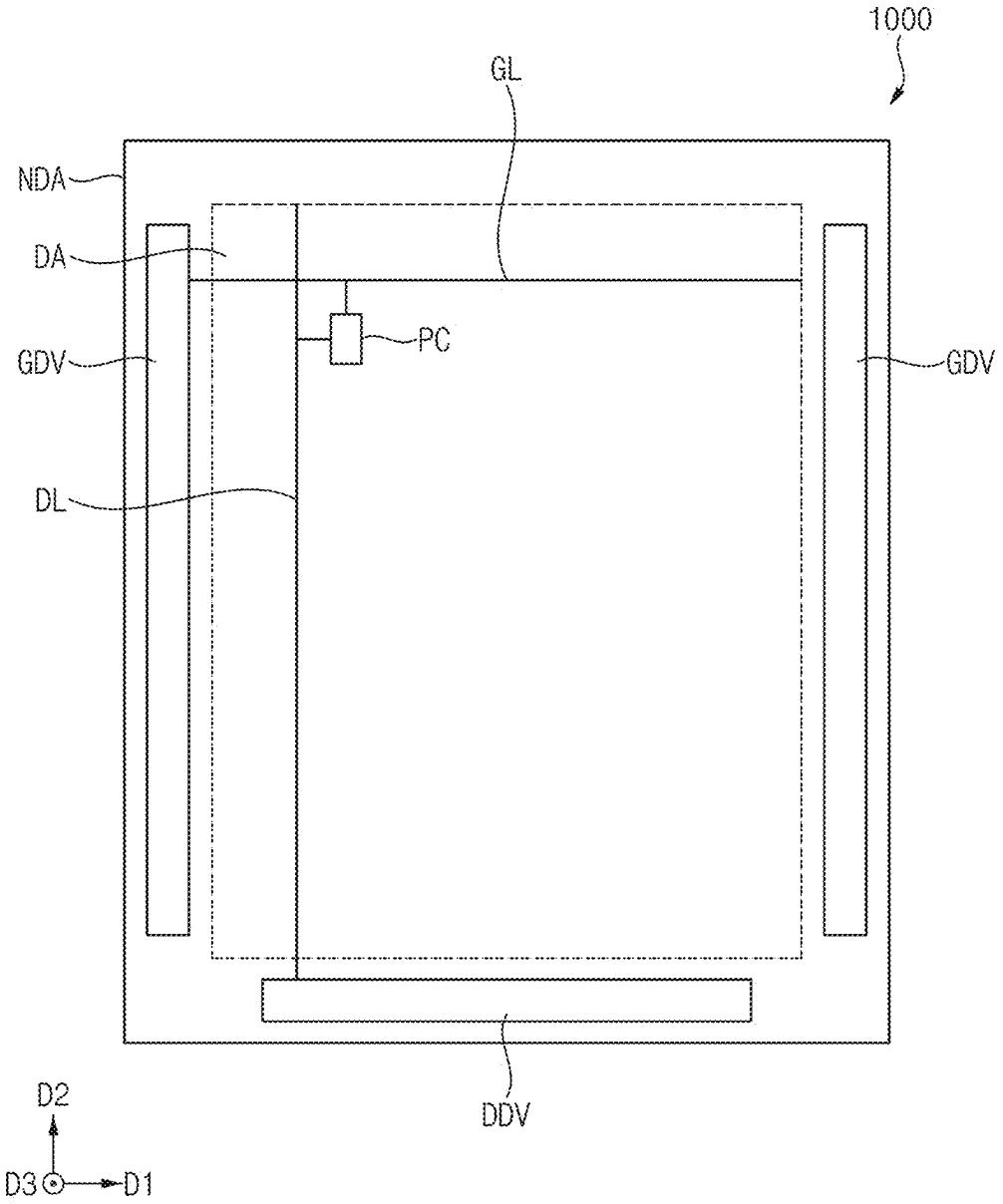


FIG. 3

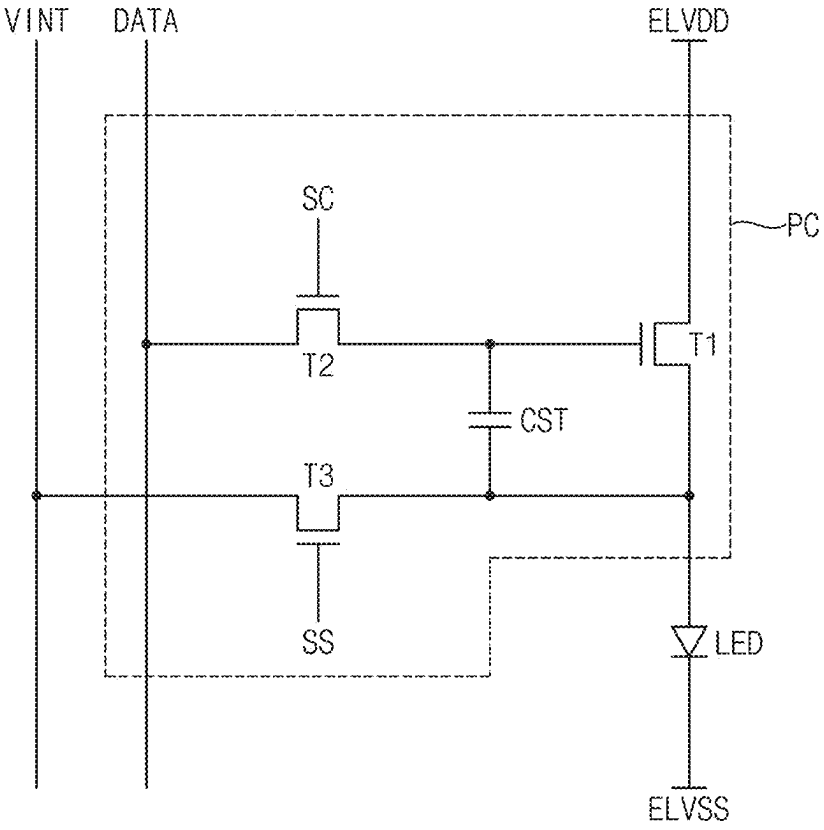
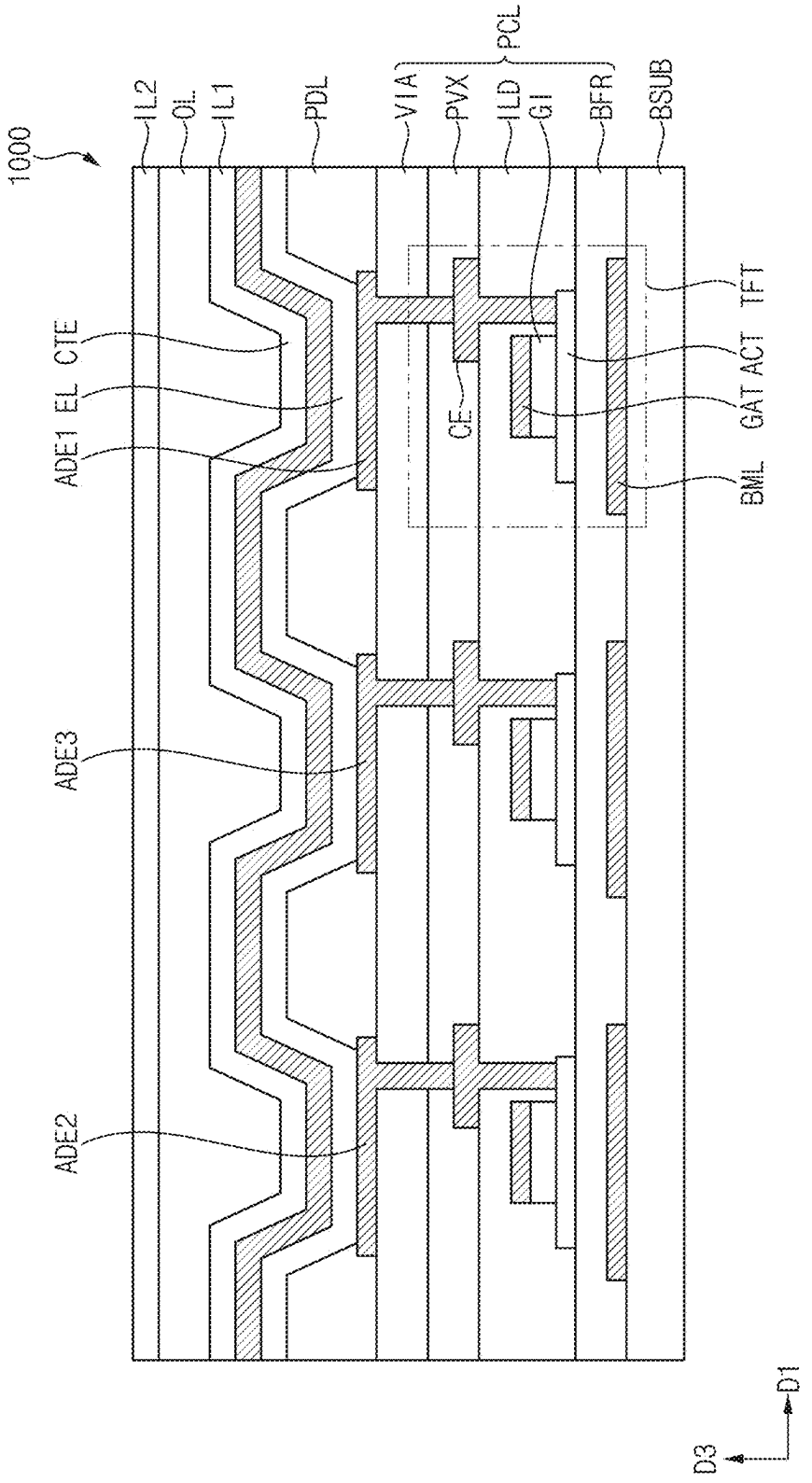


FIG. 4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IL1
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PVX
ILD
GI
PCL
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ADE3
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ACT
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D1
D3

FIG. 5

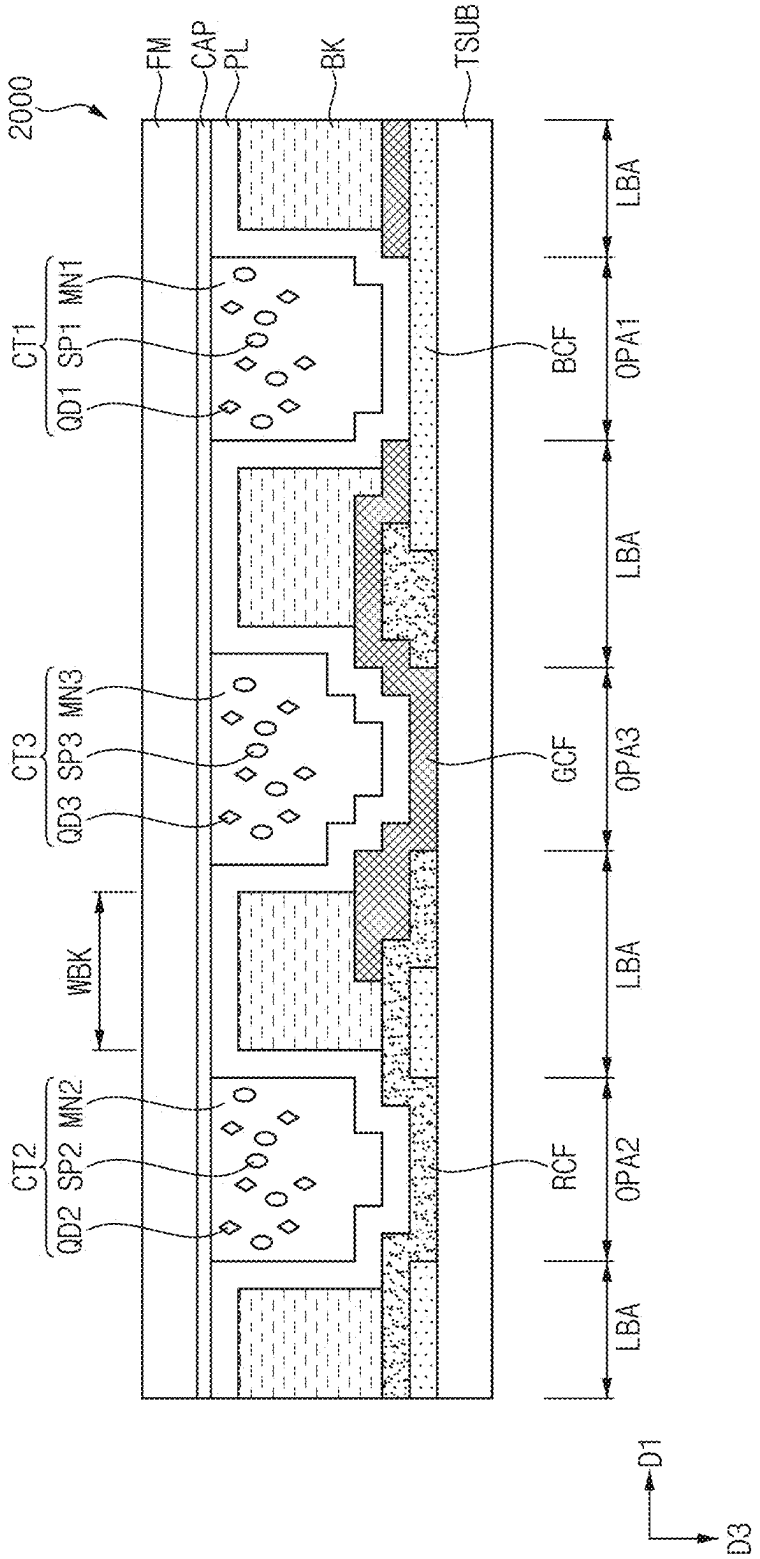
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FIG. 6

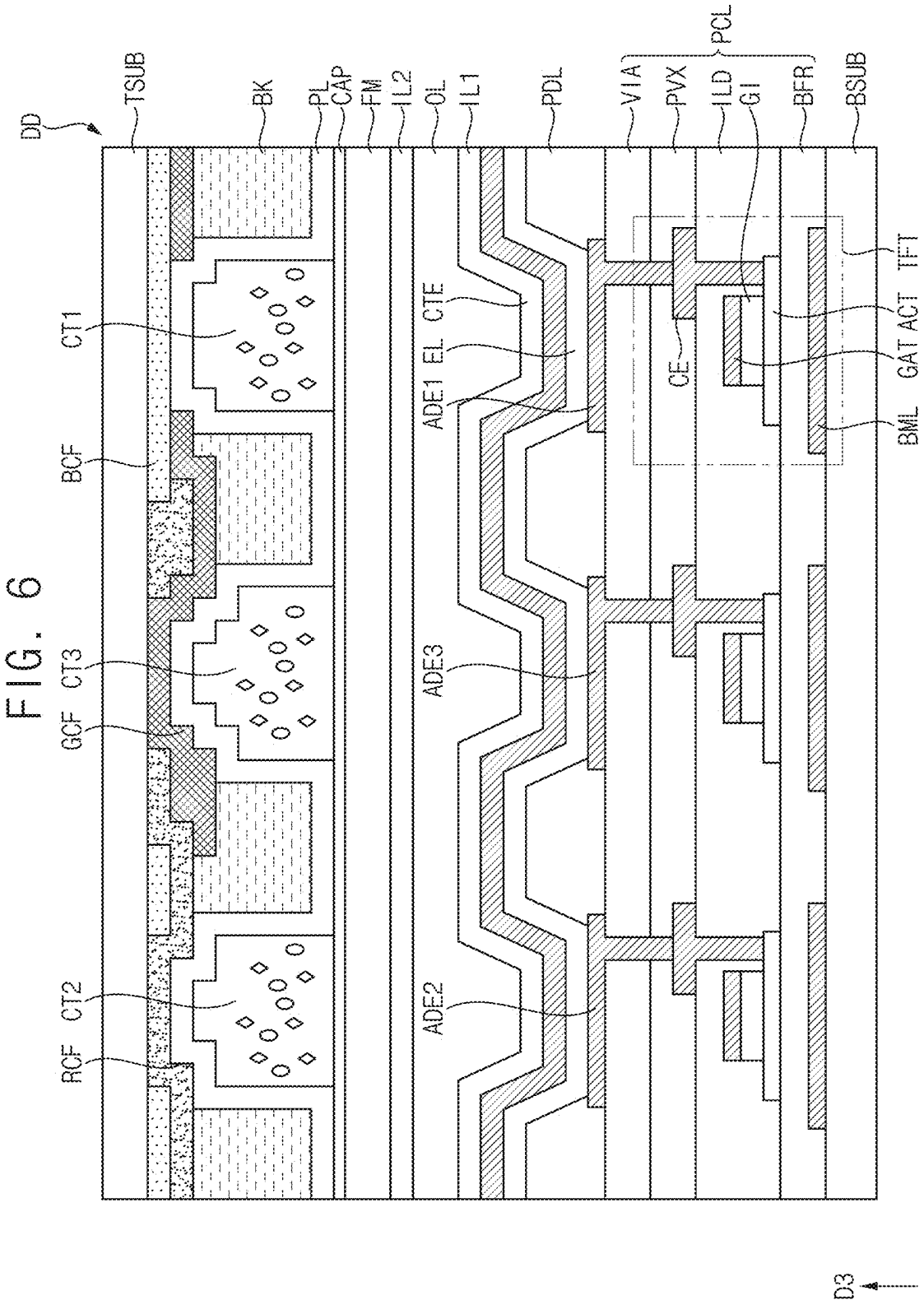
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FIG. 7

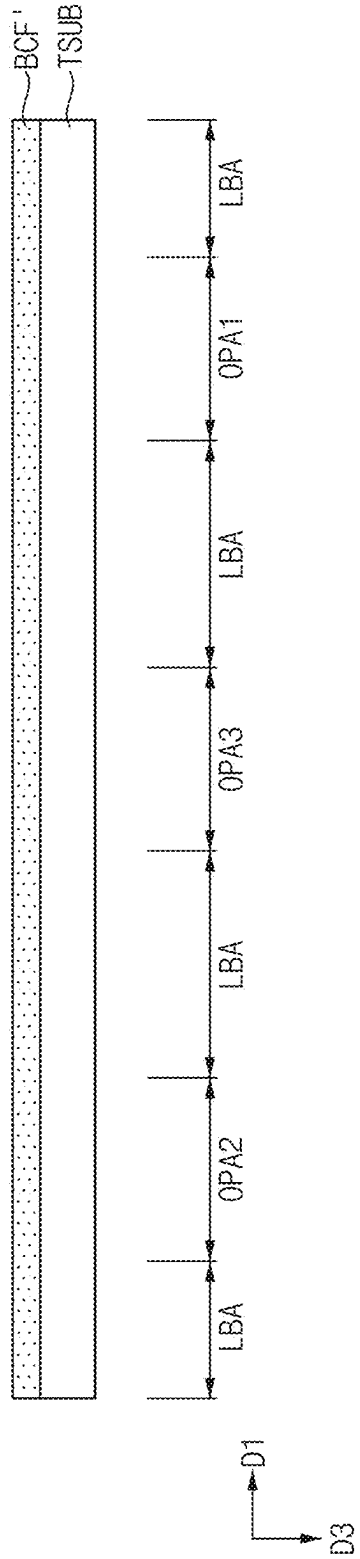

FIG. 8

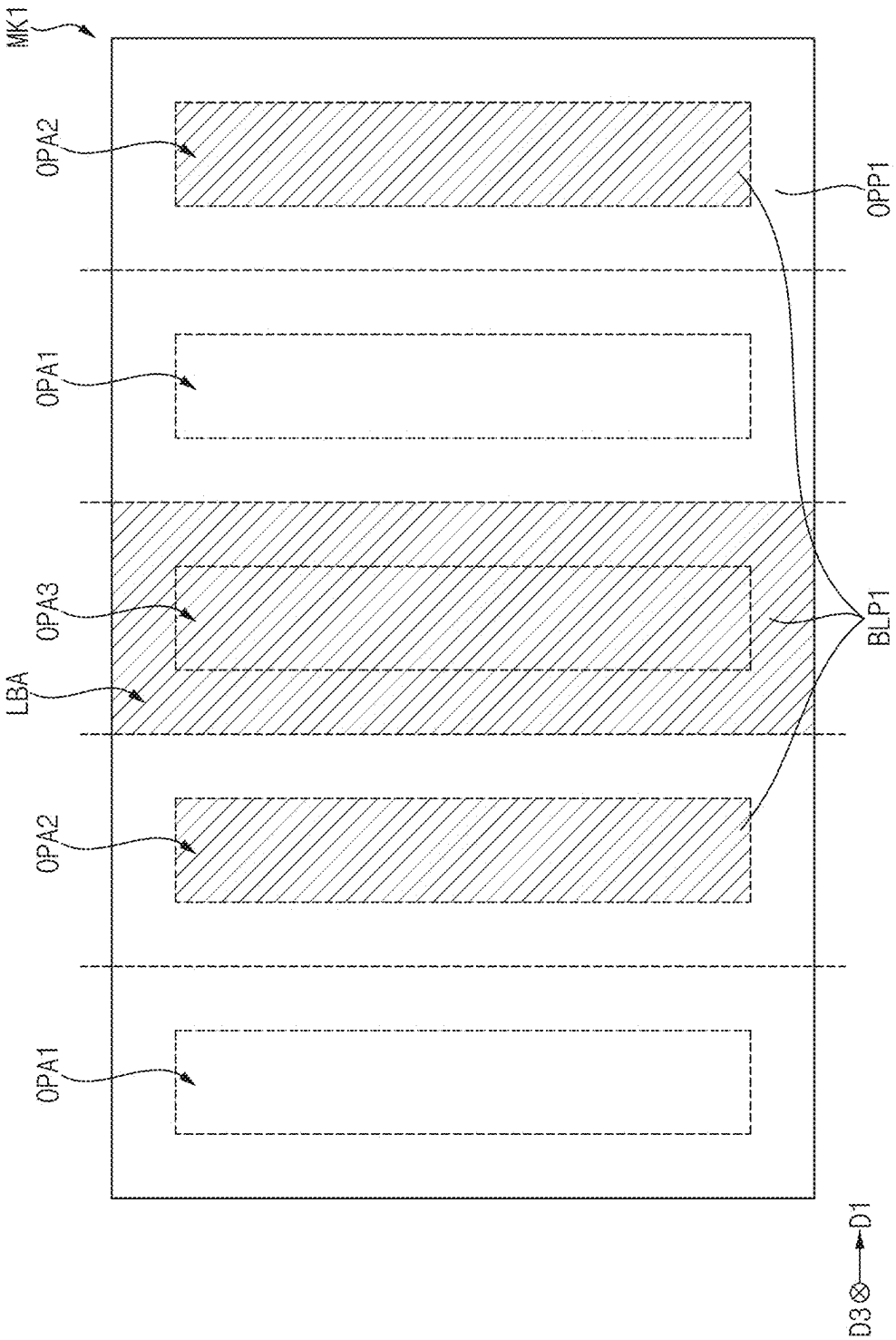

FIG. 9

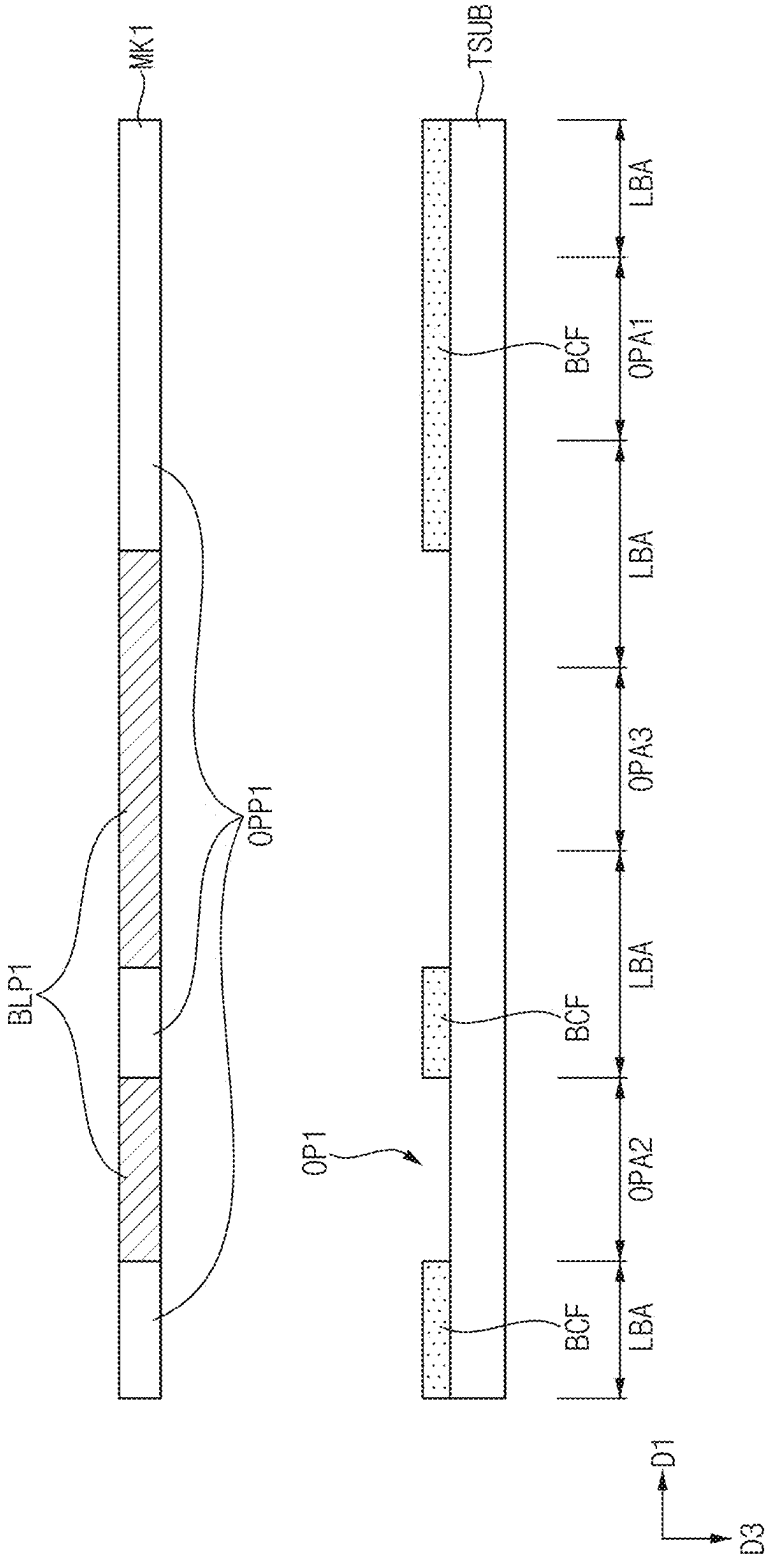
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FIG. 10

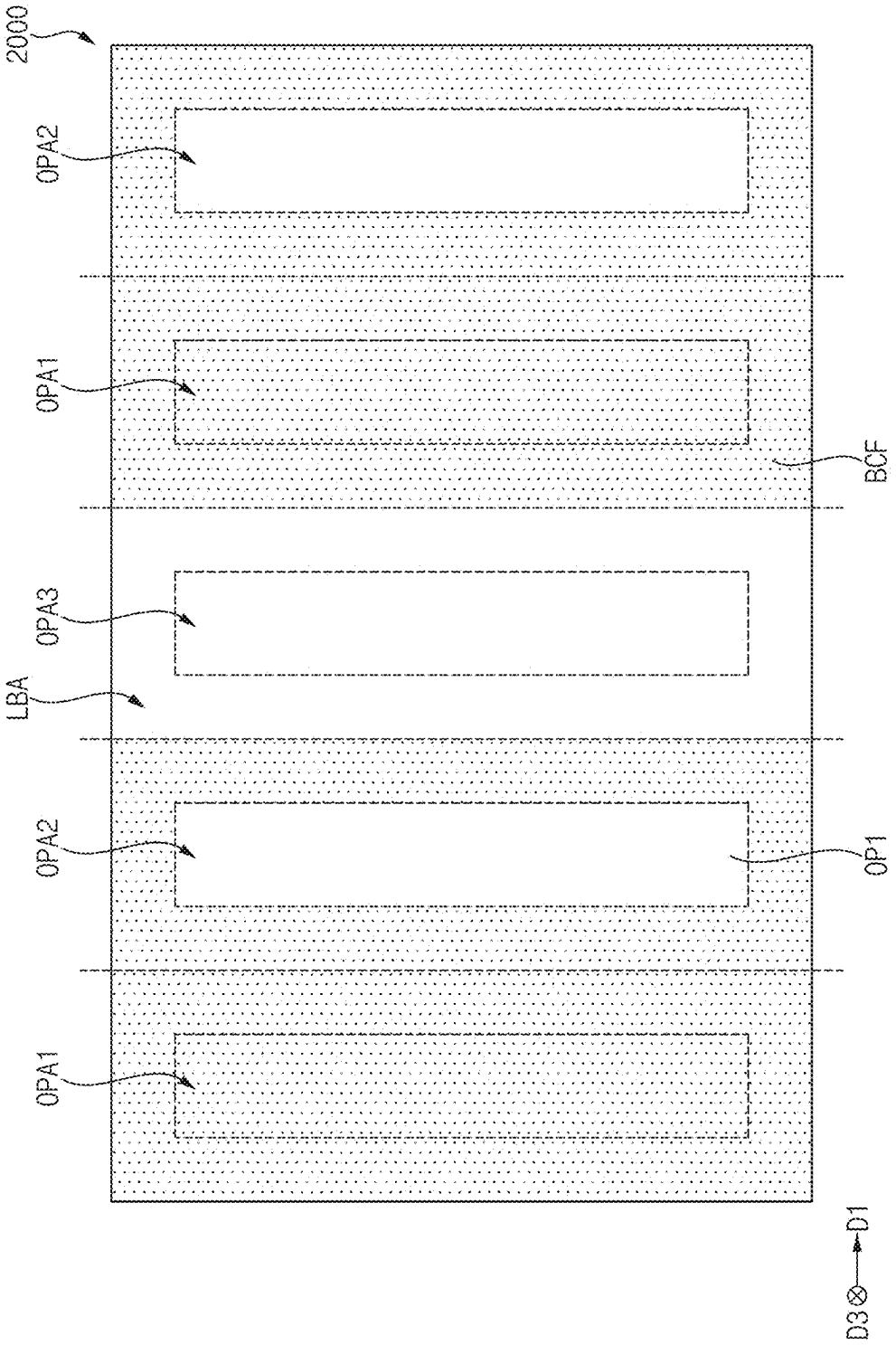

FIG. 11

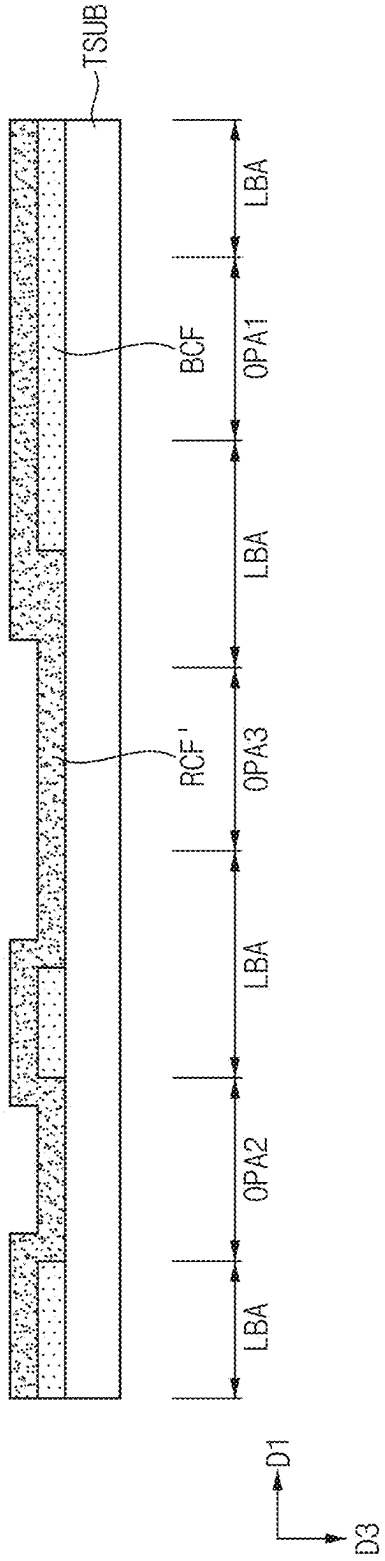

FIG. 12

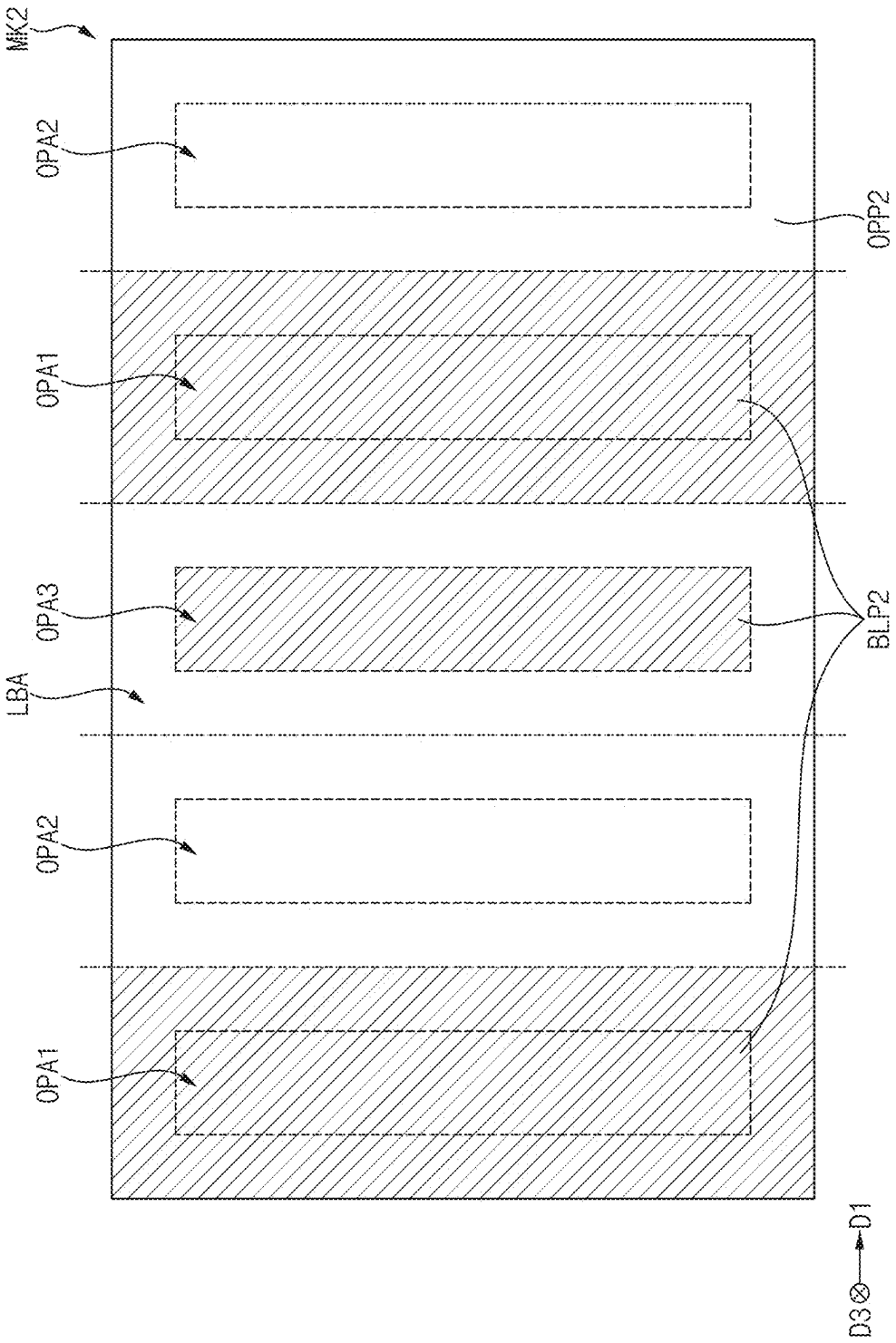

FIG. 13

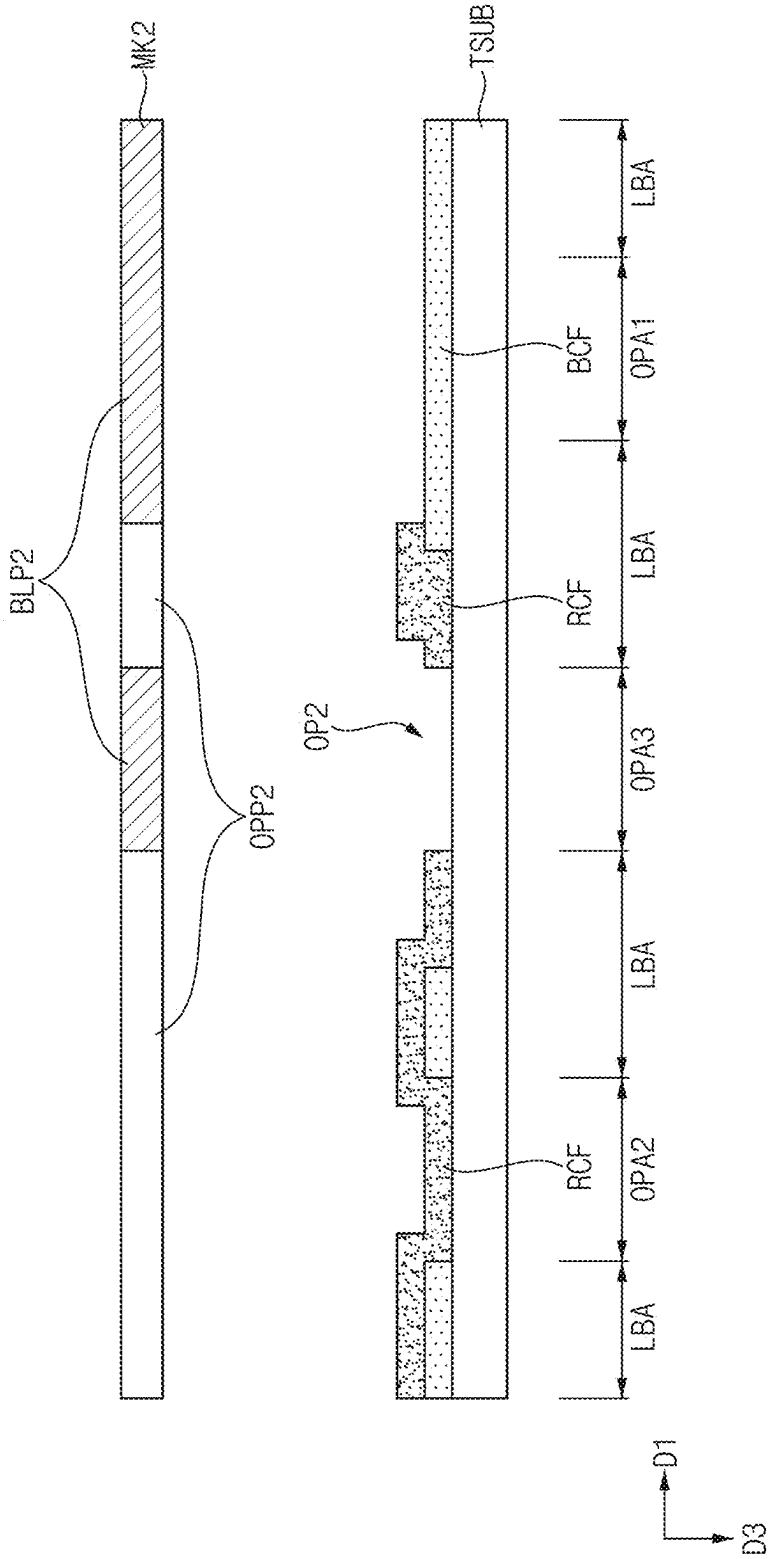
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FIG. 14

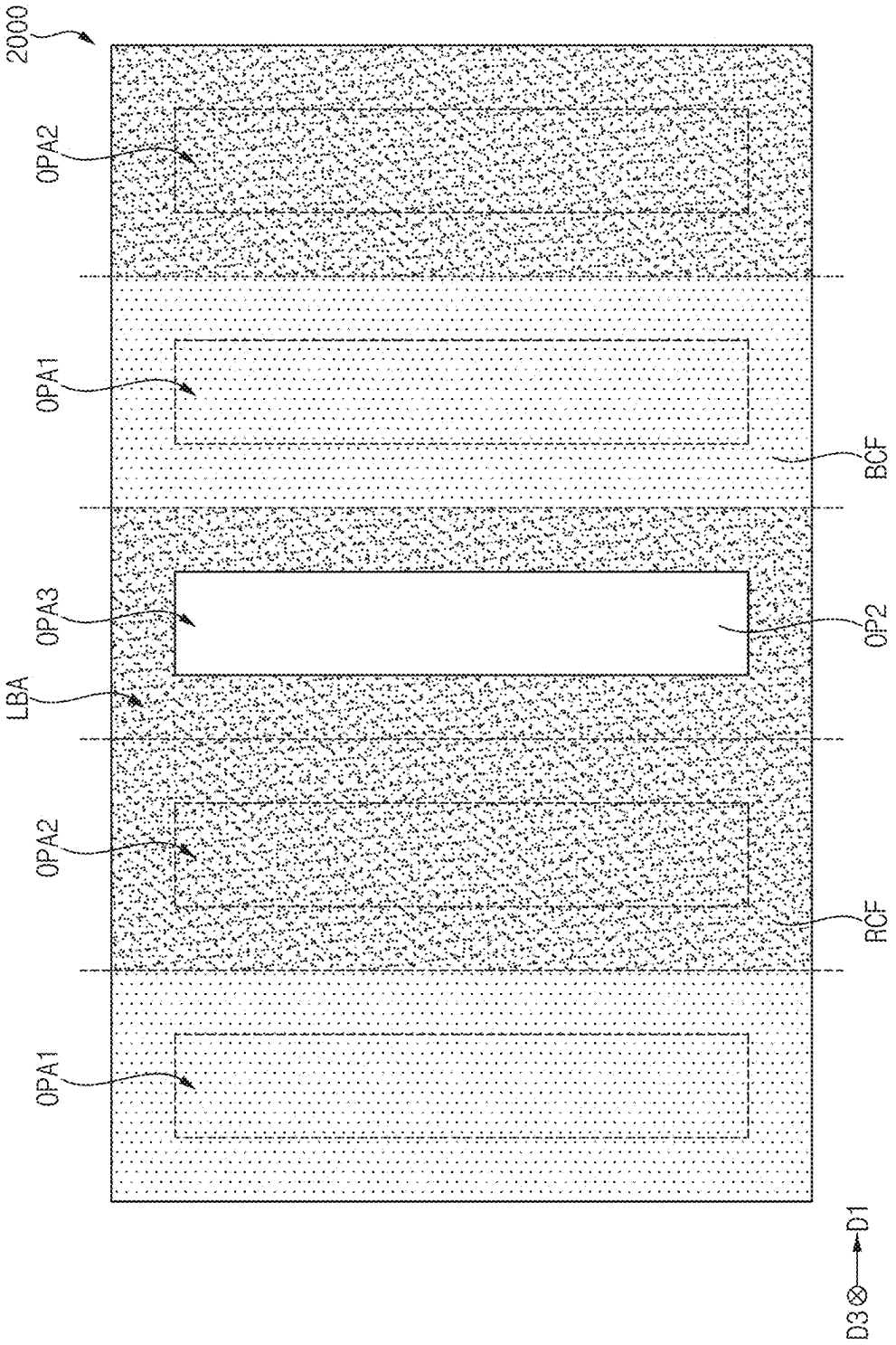

FIG. 15

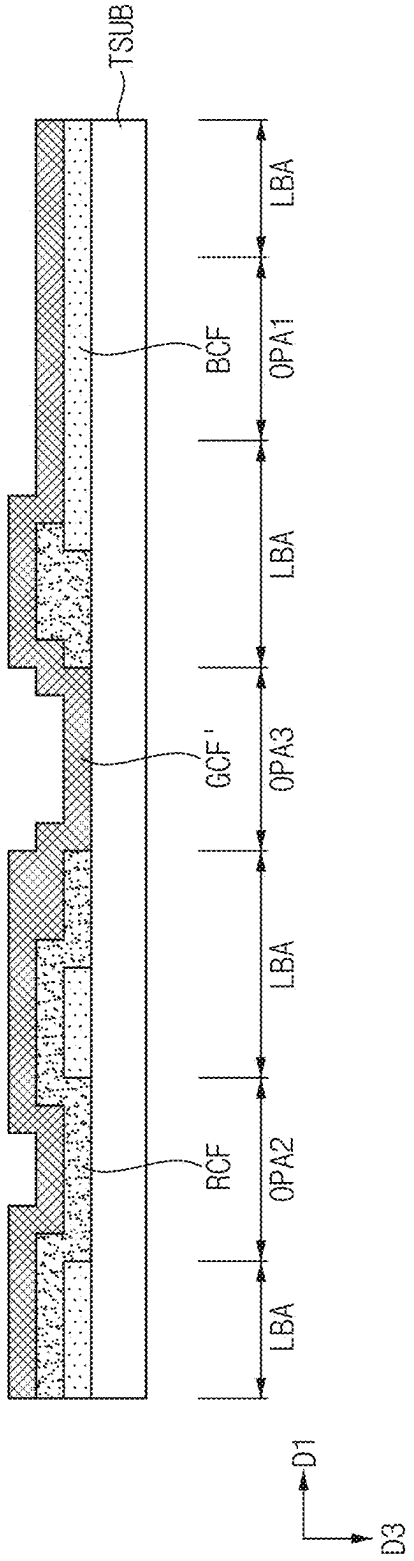

FIG. 16

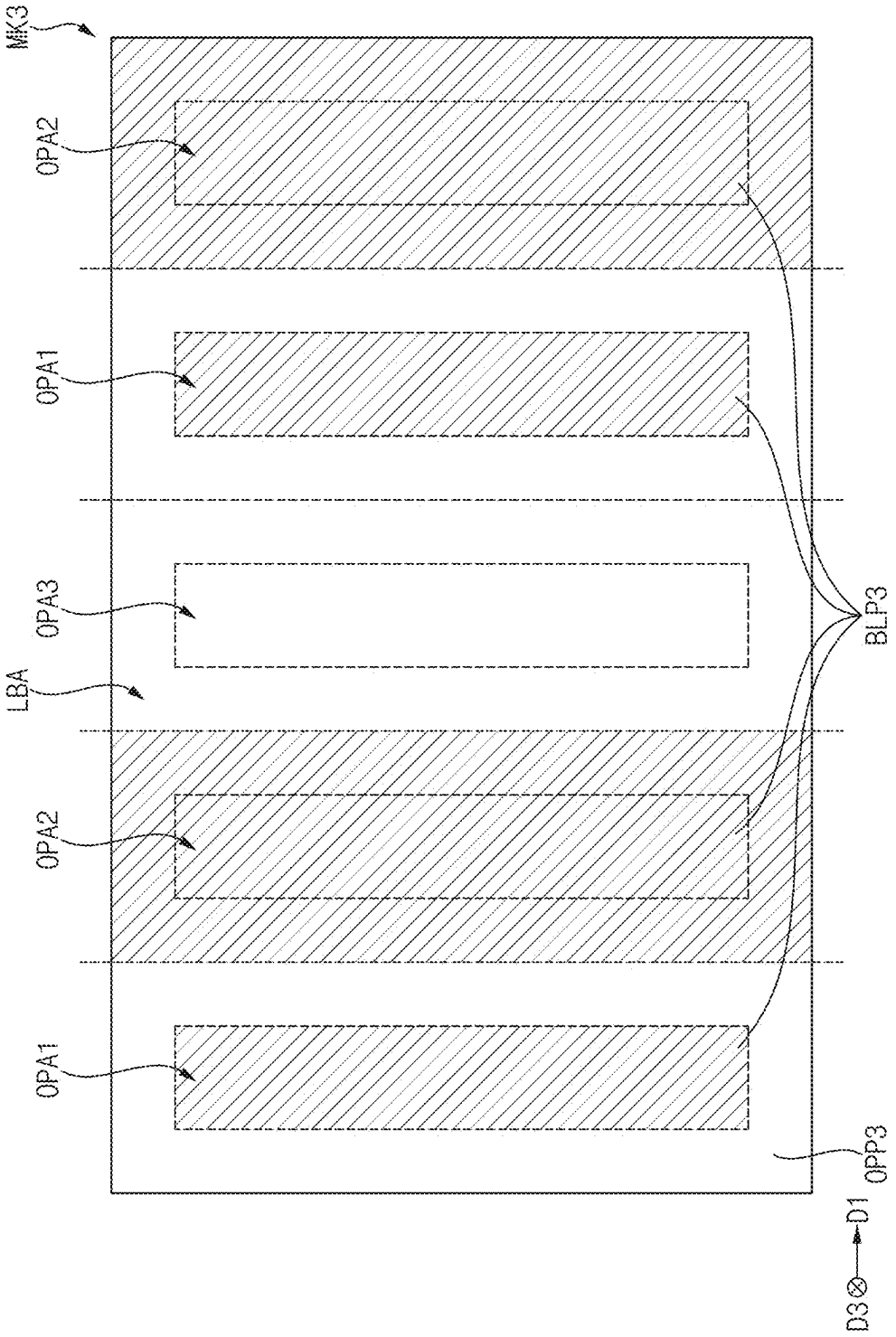

FIG. 17

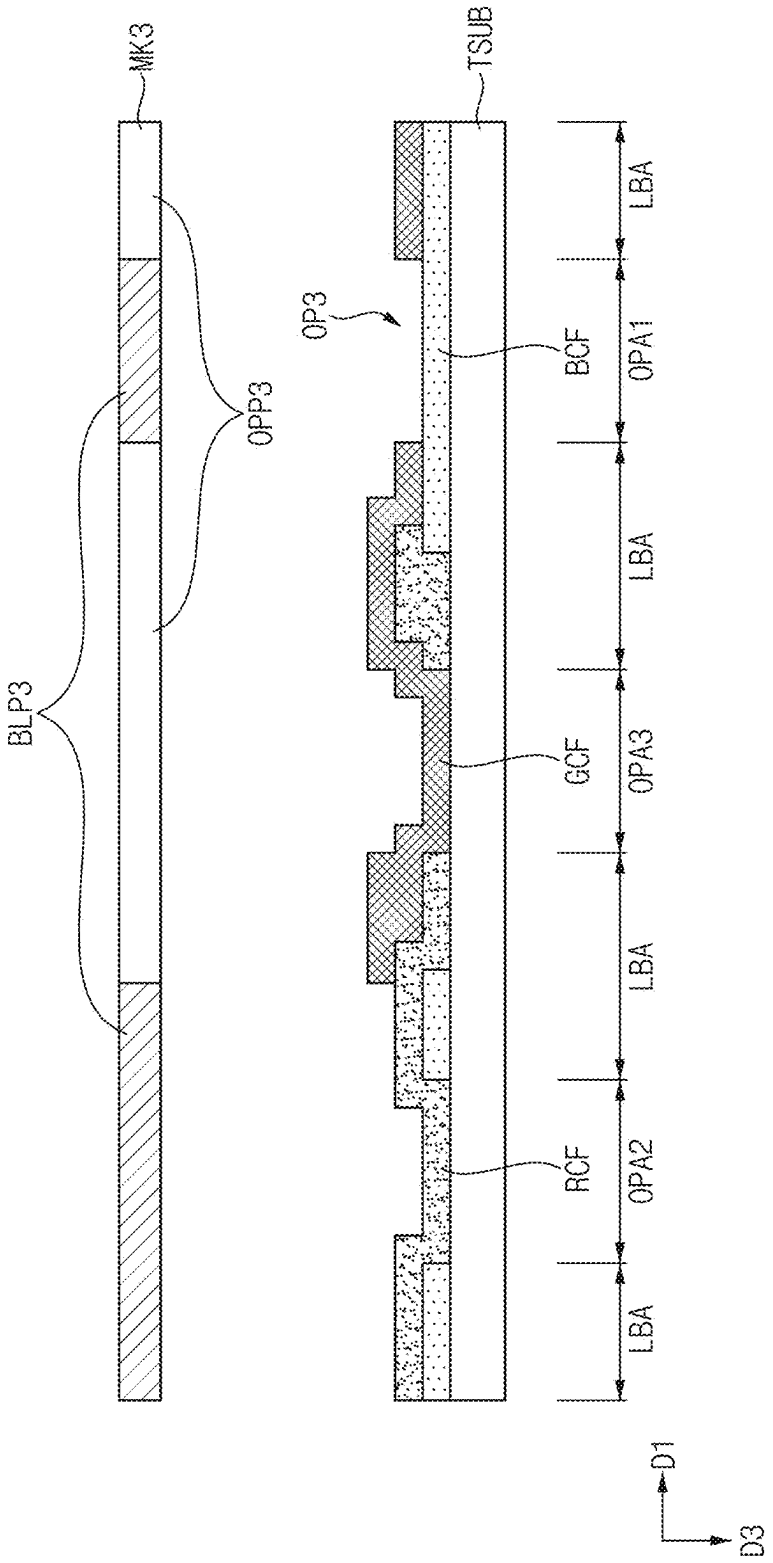
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FIG. 18

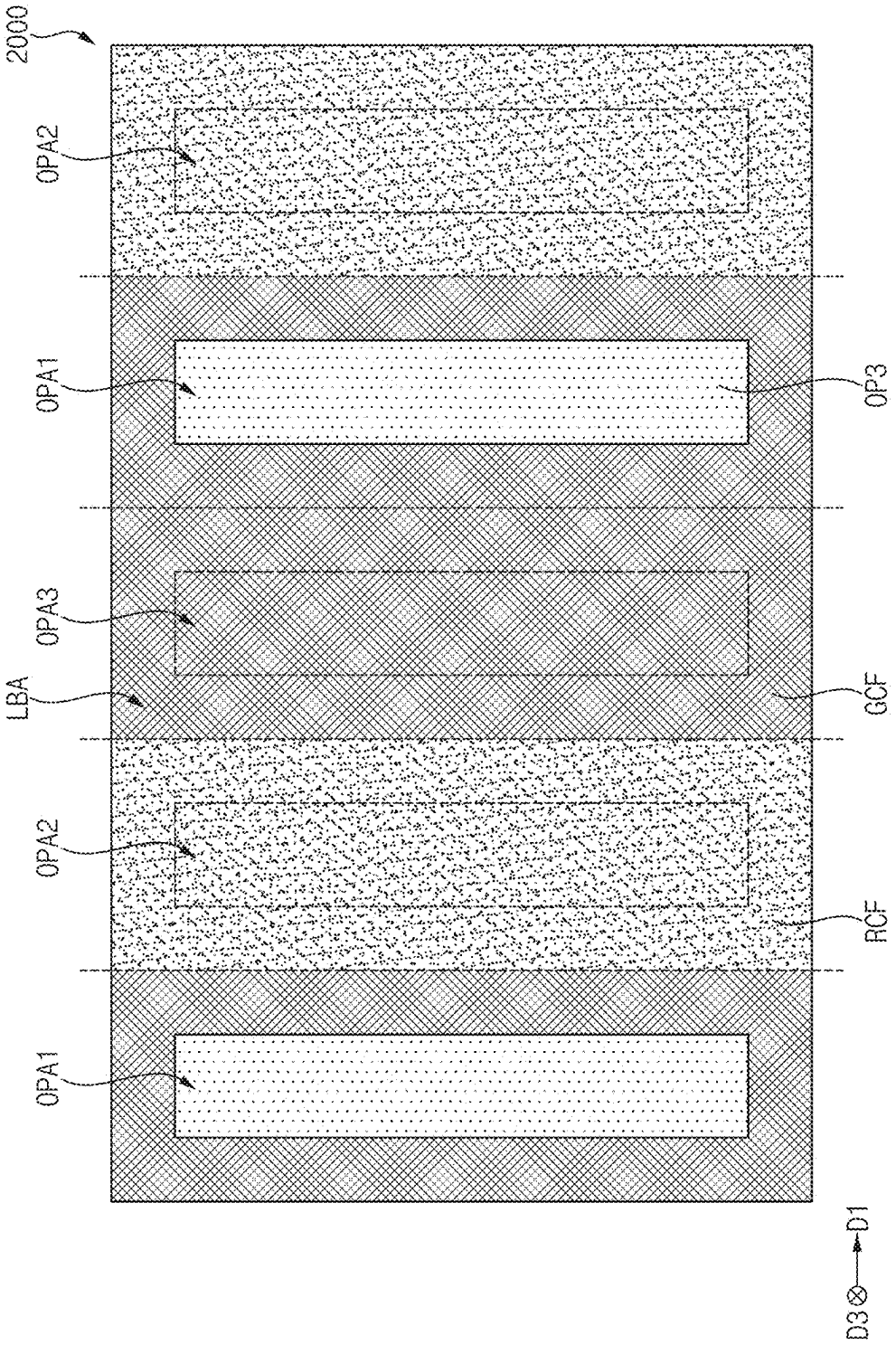

FIG. 19

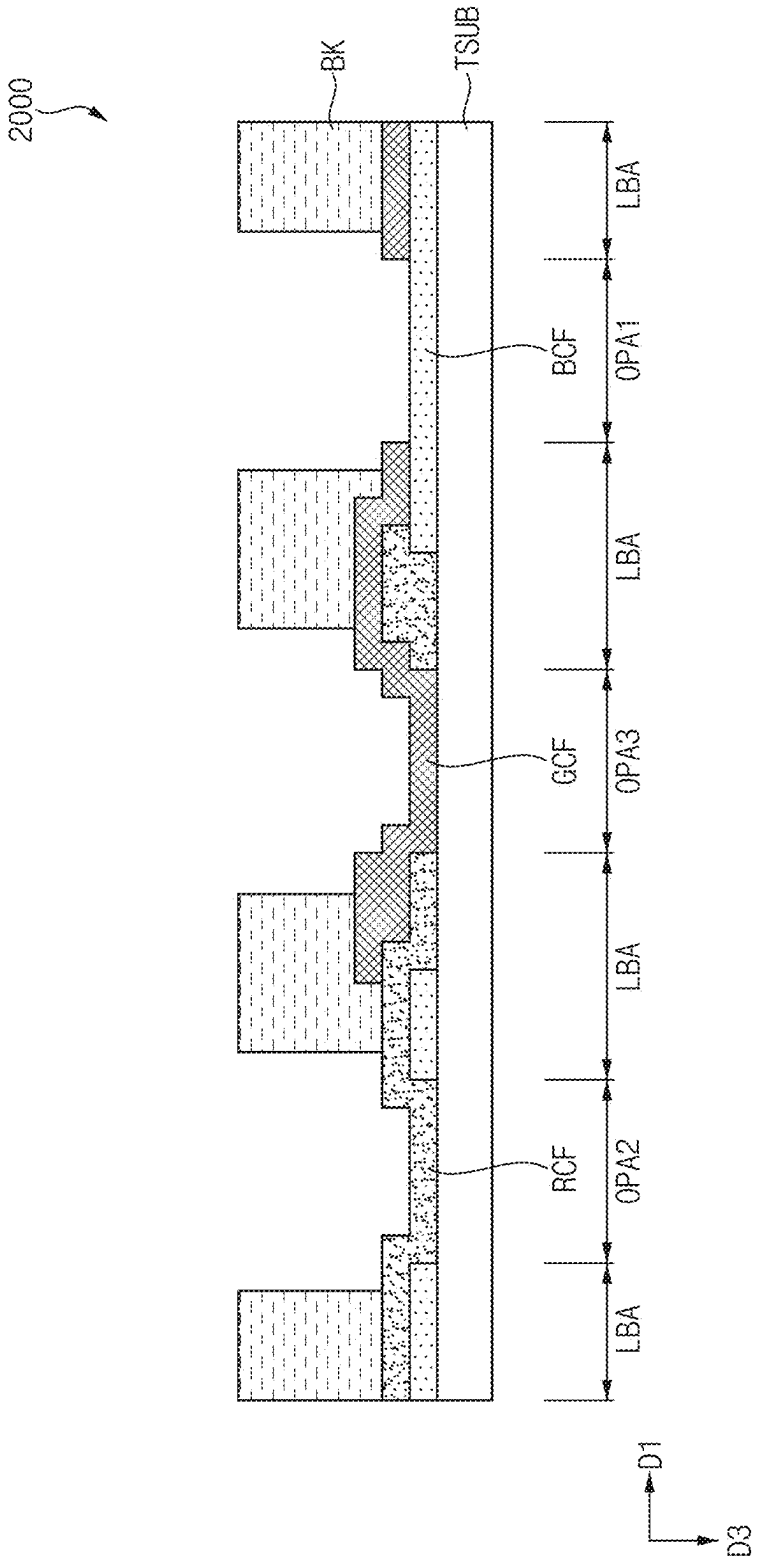

FIG. 20

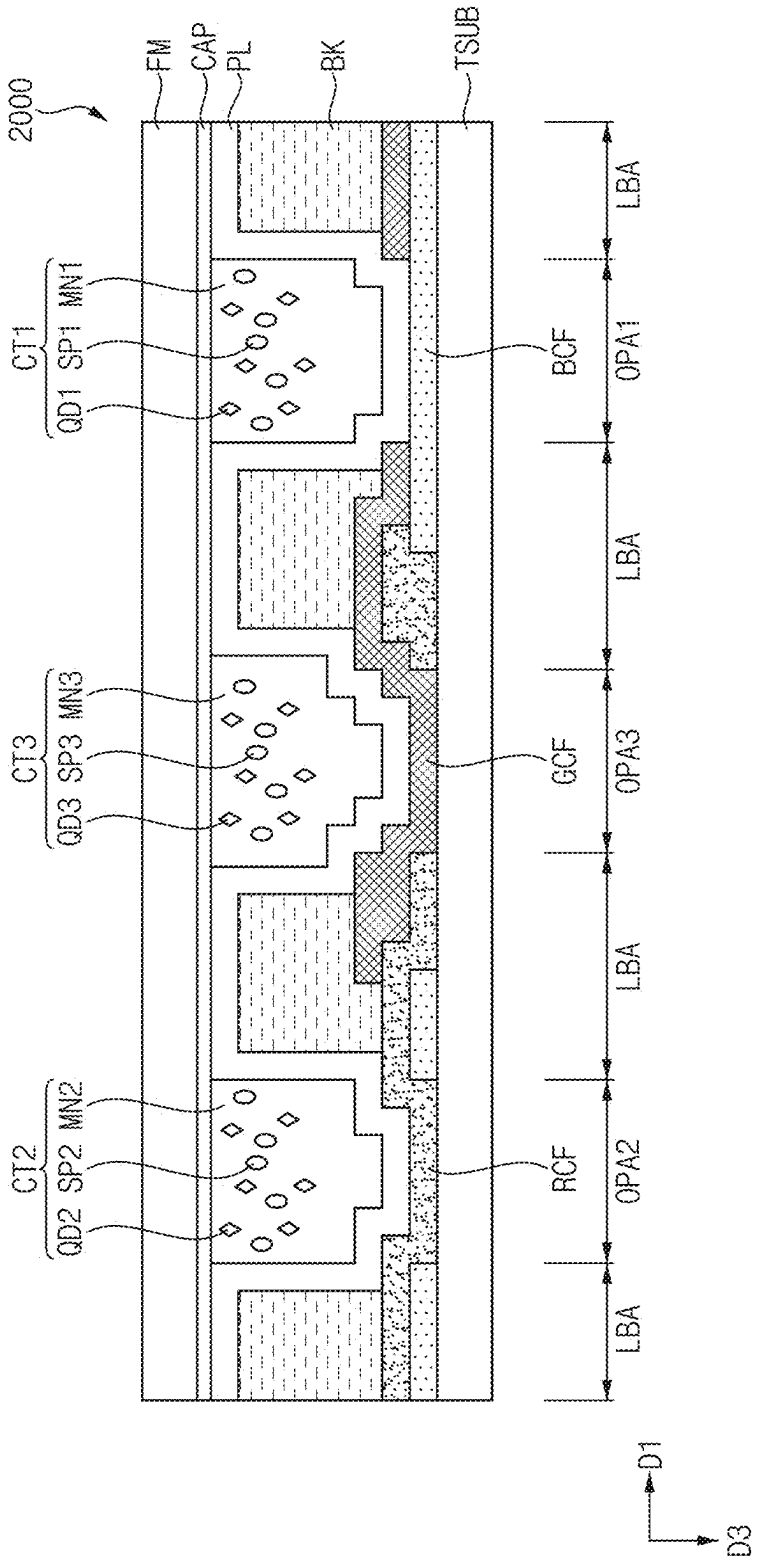
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FIG. 21

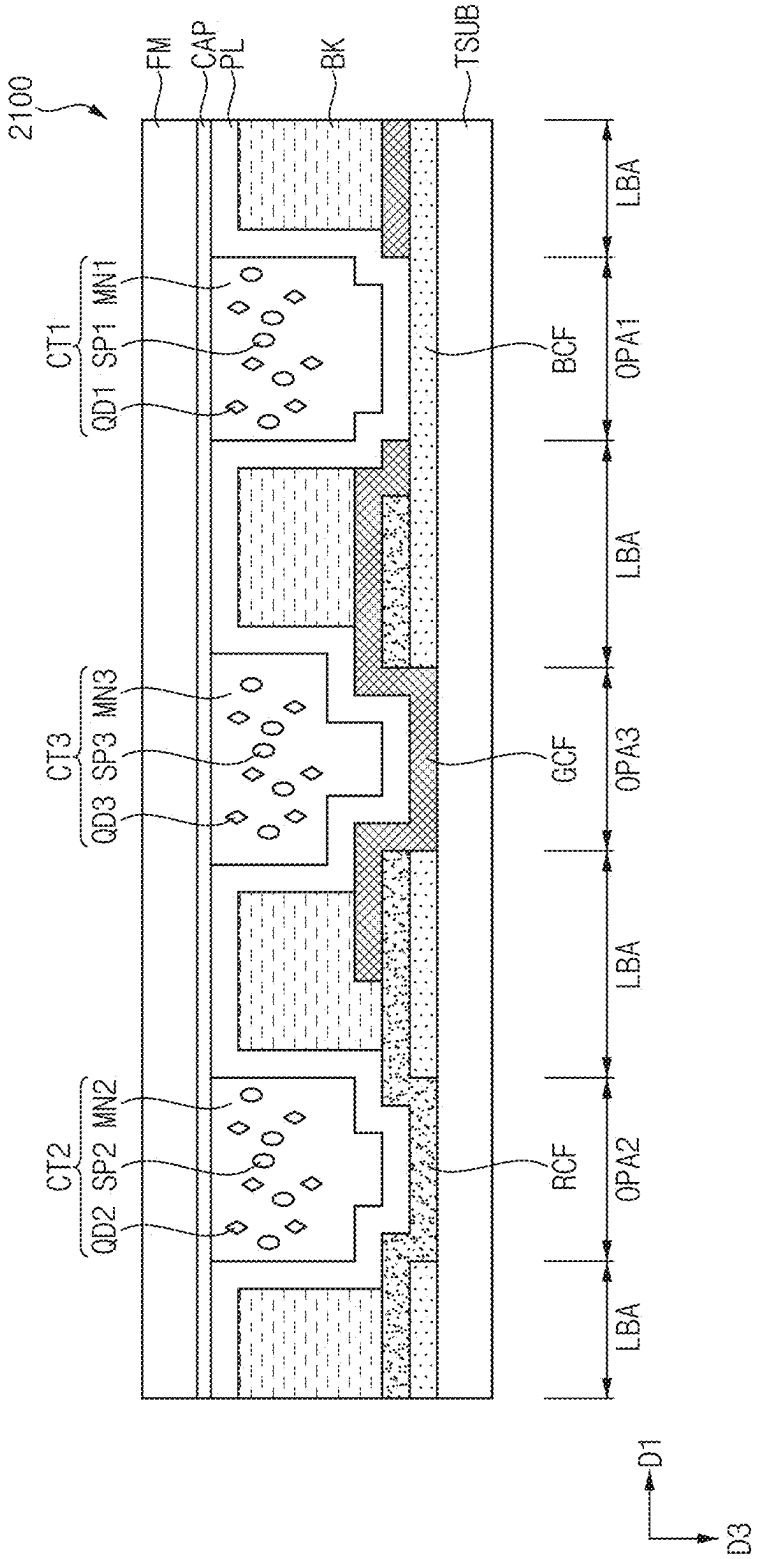
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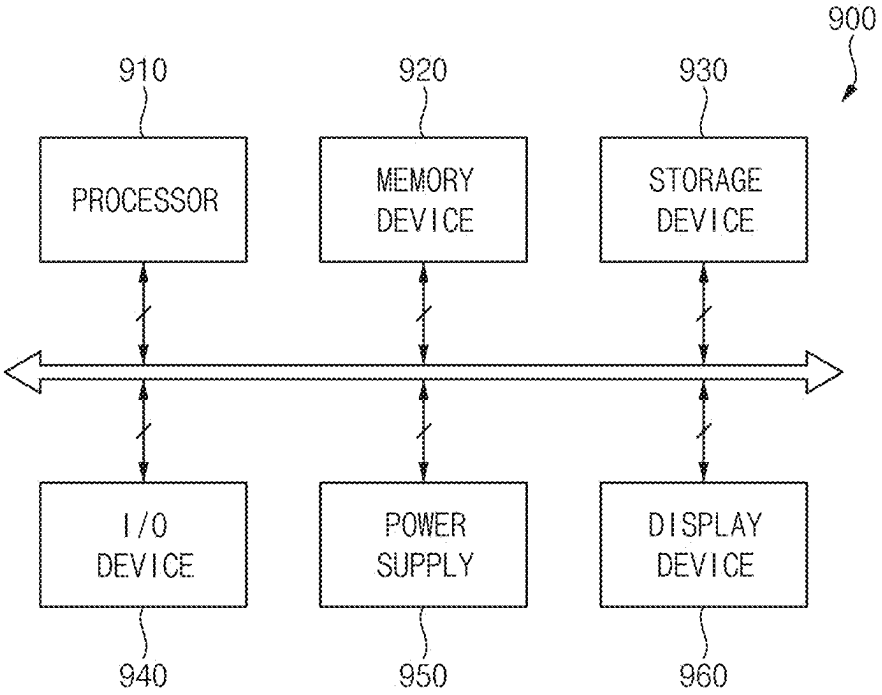
FIG. 22


900
910
920
930
PROCESSOR
MEMORY DEVICE
STORAGE DEVICE
I/O DEVICE
POWER SUPPLY
DISPLAY DEVICE
940
950
960

COLOR CONVERSION SUBSTRATE, DISPLAY DEVICE INCLUDING THE SAME, AND ELECTRONIC DEVICE INCLUDING THE DISPLAY DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority under 35 U.S.C. § 119 from Korean Patent Application No. 10-2024-0022978 filed on Feb. 16, 2024 in the Korean Intellectual Property Office, the entire contents of which are incorporated herein by reference.

BACKGROUND

1. Technical Field

[0002] Implementations of the disclosure relates generally to a color conversion substrate, a display device including the color conversion substrate, and an electronic device including the display device.

2. Description of the Related Art

[0003] Various patterns may be formed in the display device. A photolithography process may be used to form these patterns. In detail, the photolithography process includes depositing a film, coating photoresist on the film, exposing the photoresist using a mask, developing the exposed photoresist to form a photoresist pattern, and checking the degree of alignment of the photoresist pattern, etc.

SUMMARY

[0004] Embodiments provide a color conversion substrate with improved display quality.

[0005] Embodiments provide a display device including the color conversion substrate.

[0006] Embodiments provide an electronic device including the display device.

[0007] A color conversion substrate according to an embodiment may include an upper substrate including a first opening area, a second opening area adjacent to the first opening area, and a third opening area adjacent to the second opening area, a first color filter disposed on the upper substrate and having a first opening which defines the second opening area, a second color filter disposed on the first color filter and having a second opening which defines the third opening area, and a third color filter disposed on the second color filter and having a third opening which defines the first opening area. The first color filter may not overlap a light blocking area surrounding the third opening area.

[0008] In an embodiment, the first color filter may overlap a light blocking area surrounding the second opening area.

[0009] In an embodiment, the first color filter may overlap the first opening area and a light blocking area surrounding the first opening area.

[0010] In an embodiment, the second color filter may not overlap a light blocking area surrounding the first opening area.

[0011] In an embodiment, the second color filter may overlap a light blocking area surrounding the third opening area.

[0012] In an embodiment, the second color filter may overlap the second opening area and a light blocking area surrounding the second opening area.

[0013] In an embodiment, the third color filter may not overlap a light blocking area surrounding the second opening area.

[0014] In an embodiment, the third color filter may overlap a light blocking area surrounding the first opening area.

[0015] In an embodiment, the third color filter may overlap the third opening area and a light blocking area surrounding the third opening area.

[0016] In an embodiment, the first, second, and third opening areas may be arranged side by side.

[0017] In an embodiment, the first color filter may be a blue color filter, the second color filter may be a red color filter, and the third color filter may be a green color filter.

[0018] In an embodiment, the color conversion substrate may further include a bank disposed on the upper substrate and overlapping a light blocking pattern surrounding the first to third opening areas.

[0019] In an embodiment, the color conversion substrate may further include a first color conversion pattern disposed on the first color filter, the first color conversion pattern accommodated by the bank and including first quantum dots, a second color conversion pattern disposed on the second color filter, the second color conversion pattern accommodated by the bank and including second quantum dots, and a third color conversion pattern disposed on the third color filter, the third color conversion pattern accommodated by the bank and including third quantum dots.

[0020] A display device according to an embodiment may include an emission substrate and a color conversion substrate disposed on the emission substrate. The emission substrate may include a lower substrate, a first pixel electrode disposed on the lower substrate, a second pixel electrode disposed on the lower substrate and adjacent to the first pixel electrode, and a third pixel electrode disposed on the lower substrate and adjacent to the second pixel electrode. The color conversion substate may include an upper substrate including a first opening area, a second opening area adjacent to the first opening area, and a third opening area adjacent to the second opening area, a first color filter disposed between the lower substrate and the upper substrate, the first color filter may have a first opening which defines the second opening area, a second color filter disposed between the first color filter and the lower substrate, the second color filter may have a second opening which defines the third opening area, and a third color filter disposed between the second color filter and the lower substrate, the third color filter may have a third opening which defines the first opening area. The first color filter may not overlap a light blocking area surrounding the third opening area.

[0021] In an embodiment, the first color filter may overlap a light blocking area surrounding the second opening area.

[0022] In an embodiment, the first color filter may overlap the first opening area and a light blocking area surrounding the first opening area.

[0023] In an embodiment, the second color filter may not overlap a light blocking area surrounding the first opening area.

[0024] In an embodiment, the first color filter may overlap the first pixel electrode, the second color filter may overlap the second pixel electrode, and the third color filter may overlap the third pixel electrode.

[0025] In an embodiment, the display device may further include an emission layer disposed on the first to third pixel electrodes and a common electrode disposed on the emission layer.

[0026] In an embodiment, the display device may further include an active pattern disposed on the lower substrate, a gate electrode disposed on the active pattern, and a connection electrode disposed on the gate electrode and electrically connected to the active pattern.

[0027] An electronic device according to an embodiment may include a display device and a power supply configured to provide power to the display device. The display device may include an emission substrate and a color conversion substrate disposed on the emission substrate. The emission substrate may include a lower substrate, a first pixel electrode disposed on the lower substrate, a second pixel electrode disposed on the lower substrate and adjacent to the first pixel electrode, and a third pixel electrode disposed on the lower substrate and adjacent to the second pixel electrode. The color conversion substate may include an upper substrate including a first opening area, a second opening area adjacent to the first opening area, and a third opening area adjacent to the second opening area, a first color filter disposed between the lower substrate and the upper substrate, the first color filter may have a first opening which defines the second opening area, a second color filter disposed between the first color filter and the lower substrate, the second color filter may have a second opening which defines the third opening area, and a third color filter disposed between the second color filter and the lower substrate, the third color filter may have a third opening which defines the first opening area. The first color filter may not overlap a light blocking area surrounding the third opening area.

[0028] Therefore, a display device according to embodiments of the disclosure may include a color conversion substrate on which color filters may be formed. Each of the color filters may define only one adjacent opening area and may not define another opening area. For example, a first color filter may define a second opening area and may not define a third opening area. A second color filter may define the third opening area and may not define a first opening area. A third color filter may define the first opening area and may not define the second opening area. Accordingly, a margin for the width of the bank may be secured, and the pitch between the first to third opening areas may be reduced. Accordingly, the resolution of the display device including the color conversion substrate can be improved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0029] The accompanying drawings, which are included to provide a further understanding of the disclosure and are incorporated in and constitute a part of this specification, illustrate embodiments of the disclosure together with the disclosure.

[0030] FIG. **1** is a perspective view illustrating a display device according to an embodiment of the disclosure;

[0031] FIG. **2** is a plan view illustrating an emission substrate included in the display device of FIG. **1**;

[0032] FIG. **3** is a schematic diagram of an equivalent circuit of a pixel included in the emission substrate of FIG. **2**;

[0033] FIG. **4** is a schematic cross-sectional view illustrating the emission substrate of FIG. **2**;

[0034] FIG. **5** is a schematic cross-sectional view illustrating a color conversion substrate included in the display device of FIG. **1**;

[0035] FIG. **6** is a schematic cross-sectional view illustrating the display device of FIG. **1**;

[0036] FIGS. **7** to **20** are schematic diagrams illustrating a method of manufacturing the color conversion substrate of FIG. **5**; and

[0037] FIG. **21** is a schematic cross-sectional view illustrating a color conversion substrate included in a display device according to an embodiment of the disclosure;

[0038] FIG. **22** is a block diagram illustrating an electronic device according to an embodiment of the disclosure.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0039] In the following description, for the purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of various embodiments or implementations of the disclosure. As used herein "embodiments" and "implementations" are interchangeable words that are non-limiting examples of devices or methods disclosed herein. It is apparent, however, that various embodiments may be practiced without these specific details or with one or more equivalent arrangements. Here, various embodiments do not have to be exclusive nor limit the disclosure. For example, specific shapes, configurations, and characteristics of an embodiment may be used or implemented in another embodiment.

[0040] Unless otherwise specified, the illustrated embodiments are to be understood as providing features of the disclosure. Therefore, unless otherwise specified, the features, components, modules, layers, films, panels, regions, and/or aspects, etc. (hereinafter individually or collectively referred to as "elements"), of the various embodiments may be otherwise combined, separated, interchanged, and/or rearranged without departing from the inventive concepts.

[0041] The use of cross-hatching and/or shading in the accompanying drawings is generally provided to clarify boundaries between adjacent elements. As such, neither the presence nor the absence of cross-hatching or shading conveys or indicates any preference or requirement for particular materials, material properties, dimensions, proportions, commonalities between illustrated elements, and/or any other characteristic, attribute, property, etc., of the elements, unless specified. Further, in the accompanying drawings, the size and relative sizes of elements may be exaggerated for clarity and/or descriptive purposes. When an embodiment may be implemented differently, a specific process order may be performed differently from the described order. For example, two consecutively described processes may be performed substantially at the same time or performed in an order opposite to the described order. Also, like reference numerals and/or reference characters denote like elements.

[0042] When an element, such as a layer, is referred to as being "on," "connected to," or "coupled to" another element or layer, it may be directly on, connected to, or coupled to the other element or layer or intervening elements or layers may be present. When, however, an element or layer is referred to as being "directly on," "directly connected to," or "directly coupled to" another element or layer, there are no intervening elements or layers present. To this end, the term "connected" may refer to physical, electrical, and/or fluid

connection, with or without intervening elements. Further, the X-axis, the Y-axis, and the Z-axis are not limited to three axes of a rectangular coordinate system, such as the x, y, and z axes, and may be interpreted in a broader sense. For example, the X-axis, the Y-axis, and the Z-axis may be perpendicular to one another, or may be different directions that are not perpendicular to one another.

[0043] For the purposes of this disclosure, "at least one of A and B" may be construed as A only, B only, or any combination of A and B. Also, "at least one of X, Y, and Z" and "at least one selected from the group consisting of X, Y, and Z" may be construed as X only, Y only, Z only, or any combination of two or more of X, Y, and Z. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0044] Although the terms "first," "second," etc. may be used herein to describe various types of elements, these elements should not be limited by these terms. These terms are used to distinguish one element from another element. Thus, a first element discussed below could be termed a second element without departing from the teachings of the disclosure.

[0045] Spatially relative terms, such as "beneath," "below," "under," "lower," "above," "upper," "over," "higher," "side" (e.g., as in "sidewall"), and the like, may be used herein for descriptive purposes, and, thereby, to describe one elements relationship to another element(s) as illustrated in the drawings. Spatially relative terms are intended to encompass different orientations of an apparatus in use, operation, and/or manufacture in addition to the orientation depicted in the drawings. For example, if the apparatus in the drawings is turned over, elements described as "below" or "beneath" other elements or features would then be oriented "above" the other elements or features. Thus, the term "below" can encompass both an orientation of above and below. Furthermore, the apparatus may be otherwise oriented (e.g., rotated 90 degrees or at other orientations), and, as such, the spatially relative descriptors used herein interpreted accordingly.

[0046] The terminology used herein is for the purpose of describing particular embodiments and is not intended to be limiting. As used herein, the singular forms, "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. Moreover, the terms "comprises," "comprising," "includes," and/or "including," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, components, and/or groups thereof, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof. It is also noted that, as used herein, the terms "substantially," "about," and other similar terms, are used as terms of approximation and not as terms of degree, and, as such, are utilized to account for inherent deviations in measured, calculated, and/or provided values that would be recognized by one of ordinary skill in the art.

[0047] Various embodiments are described herein with reference to sectional and/or exploded illustrations that are schematic illustrations of embodiments and/or intermediate structures. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments disclosed herein should not necessarily be construed as limited to the particular illustrated shapes of regions, but are to include deviations in shapes that result from, for instance, manufacturing. In this manner, regions illustrated in the drawings may be schematic in nature and the shapes of these regions may not reflect actual shapes of regions of a device and, as such, are not necessarily intended to be limiting.

[0048] As customary in the field, some embodiments are described and illustrated in the accompanying drawings in terms of functional blocks, units, and/or modules. Those skilled in the art will appreciate that these blocks, units, and/or modules are physically implemented by electronic (or optical) circuits, such as logic circuits, discrete components, microprocessors, hard-wired circuits, memory elements, wiring connections, and the like, which may be formed using semiconductor-based fabrication techniques or other manufacturing technologies. In the case of the blocks, units, and/or modules being implemented by microprocessors or other similar hardware, they may be programmed and controlled using software (e.g., microcode) to perform various functions discussed herein and may optionally be driven by firmware and/or software. It is also contemplated that each block, unit, and/or module may be implemented by dedicated hardware, or as a combination of dedicated hardware to perform some functions and a processor (e.g., one or more programmed microprocessors and associated circuitry) to perform other functions. Also, each block, unit, and/or module of some embodiments may be physically separated into two or more interacting and discrete blocks, units, and/or modules without departing from the scope of the inventive concepts. Further, the blocks, units, and/or modules of some embodiments may be physically combined into more complex blocks, units, and/or modules without departing from the scope of the inventive concepts.

[0049] Unless otherwise defined or implied herein, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by those skilled in the art to which this disclosure pertains. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and the disclosure, and should not be interpreted in an ideal or excessively formal sense unless clearly so defined herein.

[0050] Illustrative, non-limiting embodiments will be more clearly understood from the following detailed description in conjunction with the accompanying drawings.

[0051] FIG. **1** is a perspective view illustrating a display device according to an embodiment of the disclosure.

[0052] Referring to FIG. **1**, a display device DD according to an embodiment of the disclosure may include an emission substrate **1000** and a color conversion substrate **2000**.

[0053] The emission substrate **1000** may generate and may emit light. In an embodiment, the emission substrate **1000** may include at least one pixel circuit and at least one light emitting diode. The pixel circuit may generate a driving current, and the light emitting diode may emit light corresponding to the driving current.

[0054] The color conversion substrate **2000** may be disposed on the emission substrate **1000**. The color conversion substrate **2000** may convert, transmit, block, and/or absorb the color of light emitted from the emission substrate **1000**. Accordingly, the color conversion substrate **2000** may improve color reproducibility of the display device DD.

[0055] While manufacturing various patterns included in the color conversion substrate **2000**, a photolithography process may be used. For example, the photolithography process may include coating a photoresist, exposing the photoresist using a mask, developing the exposed photoresist to form a photoresist pattern, and checking the degree of alignment of the photoresist pattern.

[0056] FIG. **2** is a plan view illustrating an emission substrate included in the display device of FIG. **1**. FIG. **3** is a schematic diagram of an equivalent circuit of a pixel in the emission substrate of FIG. **2**. FIG. **4** is a schematic cross-sectional view illustrating the emission substrate of FIG. **2**.

[0057] Referring to FIG. **2**, the emission substrate **1000** may be divided into a display area DA and a non-display area NDA. An image may be displayed in the display area DA, and the non-display area NDA may be positioned to surround at least a portion of the display area DA.

[0058] A pixel circuit PC may be disposed in the display area DA. The pixel circuit PC may be electrically connected to a gate line GL extending in a first direction D**1** and a data line DL extending in a second direction D**2** intersecting the first direction D**1**. The pixel circuit PC may generate the driving current.

[0059] A gate driver GDV and a data driver DDV may be disposed in the non-display area NDA.

[0060] The gate driver GDV may generate a gate signal. The gate signal may be transmitted to the pixel circuit PC through the gate line GL.

[0061] The data driver DDV may generate a data voltage. The data voltage may be transmitted to the pixel circuit PC through the data line DL.

[0062] Referring to FIG. **3**, the pixel circuit PC may include a first transistor T**1**, a second transistor T**2**, a third transistor T**3**, and a storage capacitor CST. The pixel circuit PC may be electrically connected to a light emitting diode LED. The pixel circuit PC may generate the driving current, and the light emitting diode LED may emit light in response to the driving current.

[0063] The first transistor T**1** may include a gate terminal, a first terminal, and a second terminal. The gate terminal may be electrically connected to the second transistor T**2**. The first terminal may be provided with a first voltage ELVDD. The second terminal may be electrically connected to the light emitting diode LED. The first transistor T**1** may generate the driving current.

[0064] The second transistor T**2** may include a gate terminal, a first terminal, and a second terminal. The gate terminal may receive a first gate signal SC. The first terminal may be provided with a data voltage DATA. The second terminal may be electrically connected to the first transistor T**1**. The second transistor T**2** may transmit the data voltage DATA in response to the first gate signal SC.

[0065] The third transistor T**3** may include a gate terminal, a first terminal, and a second terminal. The gate terminal may receive a second gate signal SS. The first terminal may be provided with an initialization voltage VINT. The second terminal may be electrically connected to the light emitting diode LED. The third transistor T**3** may transmit the initialization voltage VINT in response to the second gate signal SS.

[0066] The storage capacitor CST may include a first terminal and a second terminal. The first terminal may be electrically connected to the gate terminal of the first transistor T**1**. The second terminal may be electrically connected to the second terminal of the first transistor T**1**.

[0067] The light emitting diode LED may include a first terminal and a second terminal. The first terminal may be electrically connected to the first transistor T**1**. The second terminal may be provided with a second voltage ELVSS.

[0068] Referring to FIG. **4**, the emission substrate **1000** may include a lower substrate BSUB, a lower metal pattern BML, a buffer layer BFR, an active pattern ACT, a gate insulating layer GI, a gate electrode GAT, an interlayer insulating layer ILD, a connection electrode CE, a passivation layer PVX, a via insulating layer VIA, a first pixel electrode ADE**1**, a second pixel electrode ADE**2**, a third pixel electrode ADE**3**, a pixel defining layer PDL, an emission layer EL, a common electrode CTE, a first inorganic layer IL**1**, an organic layer OL, and a second inorganic layer IL**2**.

[0069] The lower metal pattern BML, the active pattern ACT, the gate electrode GAT, and the connection electrode CE may form a transistor TFT.

[0070] The lower metal pattern BML, the buffer layer BFR, the active pattern ACT, the gate insulating layer GI, the gate electrode GAT, the interlayer insulating layer ILD, the connection electrode CE, the passivation layer PVX, and the via insulation layer VIA may be defined as a pixel circuit layer PCL.

[0071] The lower substrate BSUB may include a transparent or opaque material. In an embodiment, examples of materials that can be used as the lower substrate BSUB may include glass, quartz, and plastic. These can be used alone or in combination with each other. The lower substrate BSUB may be composed of a single layer or multiple layers in combination with each other.

[0072] The lower metal pattern BML may be disposed on the lower substrate BSUB. In an embodiment, the lower metal pattern BML may be formed of metal, alloy, conductive metal oxide, transparent conductive material, etc. Examples of materials that can be used as the lower metal pattern BML may include silver (Ag), alloy containing silver, molybdenum (Mo), an alloy containing molybdenum, aluminum (Al), an alloy containing aluminum, aluminum nitride (AlN), tungsten (W), tungsten nitride (WN), copper (Cu), nickel (Ni), chromium (Cr), chromium nitride (CrN), titanium (Ti), tantalum (Ta), platinum (Pt), scandium (Sc), indium tin oxide (ITO), and indium zinc oxide (IZO). These can be used alone or in combination with each other. The lower metal pattern BML may be composed of a single layer or multiple layers by combining them.

[0073] The buffer layer BFR may be disposed on the lower substrate BSUB and may cover the lower metal pattern BML. In an embodiment, the buffer layer BFR may be formed of an inorganic insulating material. Examples of materials that can be used as the inorganic insulating material may include silicon oxide, silicon nitride, silicon oxynitride, and a combination thereof. These can be used alone or in combination with each other. The buffer layer BFR may prevent metal atoms, atoms, or impurities from diffusing from the lower substrate BSUB to the active pattern ACT. The buffer layer BFR may control the rate of heat provision during the crystallization process to form the active pattern ACT.

[0074] The active pattern ACT may be disposed on the buffer layer BFR. In an embodiment, the active pattern ACT may be formed of a silicon semiconductor material or an

oxide semiconductor material. Examples of the silicon semiconductor material that can be used as the active pattern ACT may include amorphous silicon and polycrystalline silicon. Examples of the oxide semiconductor material that can be used as the active pattern ACT may be InGaZnO (IGZO), InSnZnO (ITZO), etc. Examples of the oxide semiconductor material may further include indium (In), gallium (Ga), tin (Sn), zirconium (Zr), vanadium (V), hafnium (Hf), cadmium (Cd), germanium (Ge), and chromium (Cr), titanium (Ti), and zinc (Zn). These can be used alone or in combination with each other.

[0075] The gate insulating layer GI may be disposed on the active pattern ACT. In an embodiment, the gate insulating layer GI may be formed of an insulating material. Examples of insulating materials that can be used as the gate insulating layer GI may include silicon oxide, silicon nitride, and silicon oxynitride. These can be used alone or in combination with each other.

[0076] The gate electrode GAT may be disposed on the gate insulating layer GI. In an embodiment, the gate electrode GAT may be formed of metal, alloy, conductive metal oxide, transparent conductive material, etc. Examples of materials that can be used as the gate electrode GAT may include silver (Ag), an alloy containing silver, molybdenum (Mo), an alloy containing molybdenum, aluminum (Al), an alloy containing aluminum, aluminum nitride (AlN), tungsten (W), tungsten nitride (WN), copper (Cu), nickel (Ni), chromium (Cr), chromium nitride (CrN), titanium (Ti), tantalum (Ta), platinum (Pt), scandium (Sc), indium tin oxide (ITO), indium zinc oxide (IZO), etc. These can be used alone or in combination with each other.

[0077] In an embodiment, the gate electrode GAT may be composed of a single layer or multiple layers in combination with each other. For example, the gate electrode GAT may include a titanium layer and a copper layer disposed on the titanium layer. In other words, the gate electrode GAT may have a Ti/Cu structure.

[0078] The interlayer insulating layer ILD may be disposed on the buffer layer BFR and the gate insulating layer GI. The interlayer insulating layer ILD may cover the gate electrode GAT. In an embodiment, the interlayer insulating layer ILD may be formed of an insulating material. Examples of insulating materials that can be used as the interlayer insulating layer ILD may include silicon oxide, silicon nitride, and silicon oxynitride. These can be used alone or in combination with each other.

[0079] The connection electrode CE may be disposed on the interlayer insulating layer ILD. The connection electrode CE may be in contact with the active pattern ACT. In an embodiment, the connection electrode CE may be formed of metal, alloy, conductive metal oxide, transparent conductive material, etc. Examples of materials that can be used as the connection electrode CE may include silver (Ag), an alloy containing silver, molybdenum (Mo), an alloy containing molybdenum, aluminum (Al), an alloy containing aluminum, aluminum nitride (AlN), tungsten (W), tungsten nitride (WN), copper (Cu), nickel (Ni), chromium (Cr), chromium nitride (CrN), titanium (Ti), tantalum (Ta), platinum (Pt), scandium (Sc), indium tin oxide (ITO), indium zinc oxide (IZO), etc. These can be used alone or in combination with each other.

[0080] In an embodiment, the connection electrode CE may be composed of a single layer or multiple layers in combination with each other. For example, the connection electrode CE may include a titanium layer, a copper layer disposed on the titanium layer, and an indium tin oxide layer disposed on the copper layer. In other words, the connection electrode CE may have a Ti/Cu/ITO structure.

[0081] The passivation layer PVX may be disposed on the interlayer insulating layer ILD. The passivation layer PVX may cover the connection electrode CE.

[0082] In an embodiment, the passivation layer PVX may be formed of an inorganic insulating material. Examples of inorganic insulating materials that can be used as the passivation layer PVX may include silicon oxide, silicon nitride, and silicon oxynitride. These can be used alone or in combination with each other.

[0083] In an embodiment, the passivation layer PVX may be omitted.

[0084] The via insulation layer VIA may be disposed on the passivation layer PVX. In an embodiment, the via insulation layer VIA may be formed of an organic material. Examples of organic materials that can be used as the via insulating layer VIA may include photoresist, polyacrylic resin, polyimide resin, and acrylic resin. These can be used alone or in combination with each other.

[0085] In an embodiment, the passivation layer PVX may be omitted. The via insulation layer VIA may include organic materials and inorganic materials. Examples of materials that can be used as the via insulation layer VIA may include photoresist, polyacrylic resin, polyimide resin, acrylic resin, silicon oxide, silicon nitride, and silicon oxynitride. These can be used alone or in combination with each other.

[0086] The first to third pixel electrodes ADE**1**, ADE**2**, and ADE**3** may be disposed on the via insulating layer VIA. The first to third pixel electrodes ADE**1**, ADE**2**, and ADE**3** may be electrically connected to corresponding transistors, respectively.

[0087] In an embodiment, the first to third pixel electrodes ADE**1**, ADE**2**, and ADE**3** may be arranged side by side in the first direction D**1**. In other words, the second pixel electrode ADE**2** may be adjacent to the first pixel electrode ADE**1** in the first direction D**1**, the third pixel electrode ADE**3** may be adjacent to the first pixel electrode ADE**1** in the first direction D**1**, and the first pixel electrode ADE**1** may be adjacent to the third pixel electrode ADE**3** in the first direction D**1**.

[0088] In an embodiment, the first to third pixel electrodes ADE**1**, ADE**2**, and ADE**3** may be formed of metal, alloy, conductive metal oxide, transparent conductive material, etc. Examples of materials that can be used as the first to third pixel electrodes ADE**1**, ADE**2**, and ADE**3** may include silver (Ag), an alloy containing silver, molybdenum (Mo), an alloy containing molybdenum, aluminum (Al), an alloy containing aluminum, aluminum nitride (AlN), tungsten (W), tungsten nitride (WN), copper (Cu), nickel (Ni), chromium (Cr), chromium nitride (CrN), titanium (Ti), tantalum (Ta), platinum (Pt), scandium (Sc), indium tin oxide (ITO), and indium zinc oxide (IZO). These can be used alone or in combination with each other.

[0089] In an embodiment, each of the first to third pixel electrodes ADE**1**, ADE**2**, and ADE**3** may be configured as a single layer or in combination with each other to form a multi-layer structure. For example, each of the first to third pixel electrodes ADE**1**, ADE**2**, and ADE**3** may have an ITO/Ag/ITO structure.

[0090] The pixel defining layer PDL may be disposed on the via insulating layer VIA. An opening exposing the first to third pixel electrodes ADE**1**, ADE**2**, and ADE**3** may be formed in the pixel defining layer PDL. In an embodiment, the pixel defining layer PDL may be formed of an organic material. Examples of organic materials that can be used as the pixel defining layer PDL may include photoresist, polyacrylic resin, polyimide resin, and acrylic resin. These can be used alone or in combination with each other.

[0091] The emission layer EL may be disposed on the first pixel electrode ADE**1**, the second pixel electrode ADE**2**, the third pixel electrode ADE**3**, and the pixel defining layer PDL. In an embodiment, the emission layer EL may be formed in the entire area including the display area DA and the non-display area NDA. For example, the emission layer EL may have a multilayer structure in which multiple layers may be stacked on each other. The emission layer EL may emit light of different colors. In an embodiment, the emission layer EL may be disposed in the opening.

[0092] The common electrode CTE may be disposed on the emission layer EL. In an embodiment, the common electrode CTE may be formed of metal, alloy, conductive metal oxide, transparent conductive material, etc.

[0093] The first inorganic layer IL**1** may be disposed on the common electrode CTE. In an embodiment, the first inorganic layer IL**1** may be formed of an inorganic material. Examples of inorganic materials that can be used as the first inorganic layer IL**1** may include silicon oxide, silicon nitride, and silicon oxynitride. These can be used alone or in combination with each other.

[0094] The organic layer OL may be disposed on the first inorganic layer IL**1**. In an embodiment, the organic layer OL may be formed of an organic material. Examples of organic materials that can be used as the organic layer OL may include photoresist, polyacrylic resin, polyimide resin, and acrylic resin. These can be used alone or in combination with each other.

[0095] The second inorganic layer IL**2** may be disposed on the organic layer OL. In an embodiment, the second inorganic layer IL**2** may be formed of an inorganic material. Examples of inorganic materials that can be used as the second inorganic layer IL**2** may include silicon oxide, silicon nitride, and silicon oxynitride. These can be used alone or in combination with each other.

[0096] FIG. **5** is a schematic cross-sectional view illustrating a color conversion substrate included in the display device of FIG. **1**.

[0097] Referring to FIG. **5**, the color conversion substrate **2000** may include an upper substrate TSUB, a first color filter BCF, a second color filter RCF, a third color filter GCF, a bank BK, a protective layer PL, a first color conversion pattern CT**1**, a second color conversion pattern CT**2**, a third color conversion pattern CT**3**, a capping layer CAP, and a filler FM.

[0098] The upper substrate TSUB may include a transparent or opaque material. In an embodiment, examples of materials that can be used as the upper substrate TSUB may include glass, quartz, and plastic. These can be used alone or in combination with each other. The upper substrate TSUB may be composed of a single layer or multiple layers in combination with each other.

[0099] In an embodiment, the upper substrate TSUB may include a first opening area OPA**1**, a second opening area OPA**2**, a third opening area OPA**3**, and a light blocking area LBA.

[0100] The first to third opening areas OPA**1**, OPA**2**, and OPA**3** may be arranged side by side in the first direction D**1**. For example, the second opening area OPA**2** may be adjacent to the first opening area OPA**1** in the first direction D**1**, the third opening area OPA**3** may be adjacent to the second opening area OPA**2** in the first direction D**1**, and the first opening area OPA**1** may be adjacent to the third opening area OPA**3** in the first direction D**1**.

[0101] The light blocking area LBA may be defined in an area excluding (or external to) the first to third opening areas OPA**1**, OPA**2**, and OPA**3**, and may surround the first to third opening areas OPA**1**, OPA**2**, and OPA**3** in a plan view.

[0102] The first color filter BCF may be disposed on the upper substrate TSUB. In an embodiment, the first color filter BCF may be a blue color filter and may transmit only light having a wavelength corresponding to blue. For example, the first color filter BCF may include photoresist, acrylic resin, epoxy resin, polyimide resin, or a combination thereof, and may be patterned through the exposure process described above.

[0103] The second color filter RCF may be disposed on the first color filter BCF. In an embodiment, the second color filter RCF may be a red color filter and may transmit only light having a wavelength corresponding to red. For example, the second color filter RCF may include photoresist, acrylic resin, epoxy resin, polyimide resin, or a combination thereof, and may be patterned through the exposure process described above.

[0104] The third color filter GCF may be disposed on the second color filter RCF. In an embodiment, the third color filter GCF may be a green color filter and may transmit only light having a wavelength corresponding to green. For example, the third color filter GCF may include photoresist, acrylic resin, epoxy resin, polyimide resin, or a combination thereof, and may be patterned through the exposure process described above.

[0105] The bank BK may be disposed on the upper substrate TSUB and may overlap the light blocking area LBA. In an embodiment, the bank BK may be disposed on the third color filter GCF, and may overlap at least two color filters among the first to third color filters BCF, RCF, and GCF. In an embodiment, the bank BK may be disposed on the second color filter RCF and may overlap at least one color filter among the first and second color filters BCF and RCF.

[0106] The bank BK may include a light blocking material that blocks or absorbs light. For example, the bank BK may include black pigment, black dye, chromium (Cr), chromium oxide (CrO_x), chromium nitride (CrN_x), graphite, a combination thereof, etc.

[0107] The protective layer PL may be disposed on the bank BK and may entirely cover the first to third color filters BCF, RCF, and GCF. In an embodiment, the protective layer PL may include an inorganic material. For example, the protective layer PL may include silicon oxide (SiO_2), silicon nitride (SiN_x), silicon oxynitride (SiON), aluminum oxide (Al_2O_3), titanium dioxide (TiO_2), tantalum oxide (Ta_2O_5), hafnium dioxide (HfO_2), zinc dioxide (ZnO_2), or a combination thereof.

[0108] The first color conversion pattern CT**1** may be disposed on the first color filter BCF. In an embodiment, the first color conversion pattern CT**1** may be accommodated by the bank BK.

[0109] In an embodiment, the first color conversion pattern CT**1** may include a first monomer MN**1**, a first quantum dot QD**1**, and a first scattering particle SP**1**.

[0110] The first quantum dots QD**1** and the first scattering particle SP**1** may be dispersed in the first monomer MN**1**. In an embodiment, the first monomer MN**1** may include an epoxy-based monomer, an ester-based monomer, etc.

[0111] The first quantum dot QD**1** may convert the color of incident light to blue. For example, the first quantum dot QD**1** may be a quantum dot, and may be selected from the group consisting of group II-VI compounds, group IV-VI compounds, group IV elements, group IV compounds, and combinations thereof. However, the first color conversion pattern CT**1** may not include the first quantum dot QD**1**.

[0112] The first scattering particle SP**1** may scatter light. In an embodiment, the first scattering particle SP**1** may include titanium dioxide (TiO_2) particles, zinc oxide (ZnO) particles, aluminum oxide (Al_2O_3) particles, silicon oxide (SiO_2) particles, hollow silica particles, a combination thereof, etc.

[0113] The second color conversion pattern CT**2** may be disposed on the second color filter RCF. In an embodiment, the second color conversion pattern CT**2** may be accommodated by the bank BK.

[0114] In an embodiment, the second color conversion pattern CT**2** may include a second monomer MN**2**, a second quantum dot QD**2**, and a second scattering particle SP**2**.

[0115] The second quantum dot QD**2** and the second scattering particle SP**2** may be dispersed in the second monomer MN**2**. In an embodiment, the second monomer MN**2** may include an epoxy-based monomer, an ester-based monomer, etc.

[0116] The second quantum dot QD**2** may convert the color of incident light to red. For example, the second quantum dot QD**2** may be a quantum dot, and may be selected from the group consisting of group II-VI compounds, group IV-VI compounds, group IV elements, group IV compounds, and combinations thereof.

[0117] The second scattering particle SP**2** may scatter light. In an embodiment, the second scattering particle SP**2** may include titanium dioxide (TiO_2) particles, zinc oxide (ZnO) particles, aluminum oxide (Al_2O_3) particles, silicon oxide (SiO_2) particles, hollow silica particles, a combination thereof, etc.

[0118] The third color conversion pattern CT**3** may be disposed on the third color filter GCF. In an embodiment, the third color conversion pattern CT**3** may be accommodated by the bank BK.

[0119] In an embodiment, the third color conversion pattern CT**3** may include a third monomer MN**3**, a third quantum dot QD**3**, and a third scattering particle SP**3**.

[0120] The third quantum dot QD**3** and the third scattering particle SP**3** may be dispersed in the third monomer MN**3**. In an embodiment, the third monomer MN**3** may include an epoxy monomer, an ester monomer, etc.

[0121] The third quantum dot QD**3** may convert the color of incident light to green. For example, the third quantum dot QD**3** may be a quantum dot, and may be selected from the group consisting of group II-VI compounds, group IV-VI compounds, group IV elements, group IV compounds, and combinations thereof.

[0122] The third scattering particle SP**3** may scatter light. In an embodiment, the third scattering particle SP**3** may include titanium dioxide (TiO_2) particles, zinc oxide (ZnO) particles, aluminum oxide (Al_2O_3) particles, silicon oxide (SiO_2) particles, hollow silica particles, a combination thereof, etc.

[0123] The capping layer CAP may be disposed on the first to third color conversion patterns CT**1**, CT**2**, and CT**3**. The capping layer CAP may entirely cover the first to third color conversion patterns CT**1**, CT**2**, and CT**3**.

[0124] The filler FM may be disposed on the capping layer CAP. In an embodiment, the filler FM may include an organic material having a relatively high refractive index. For example, the filler FM may include urethane resin, epoxy resin, acrylic resin, a combination thereof, etc.

[0125] FIG. **6** is a schematic cross-sectional view illustrating the display device of FIG. **1**.

[0126] Referring to FIG. **6**, the display device DD may include the emission substrate **1000** described with reference to FIG. **4** and the color conversion substrate **2000** described with reference to FIG. **5**. In an embodiment, the emission substrate **1000** and the color conversion substrate **2000** may be arranged to be aligned with each other. For example, the first color filter BCF may overlap the first pixel electrode ADE**1**, the second color filter RCF may overlap the second pixel electrode ADE**2**, and the third color filter GCF may overlap the third pixel electrode ADE**3**.

[0127] FIGS. **7** to **20** are schematic diagrams illustrating a method of manufacturing the color conversion substrate of FIG. **5**.

[0128] Referring to FIG. **7**, a preliminary first color filter BCF' may be formed on the upper substrate TSUB. In an embodiment, photoresist may be entirely applied on the upper substrate TSUB. In this disclosure, the photoresist may be described as a negative photoresist, but the disclosure is not limited thereto.

[0129] Referring to FIGS. **8**, **9**, and **10**, the first color filter BCF may be formed on the upper substrate TSUB.

[0130] In detail, FIG. **8** may illustrate a first mask MK**1** for exposing the preliminary first color filter BCF'. As shown in FIG. **8**, the first mask MK**1** may include a first blocking part BLP**1** that blocks light and a first open part OPP**1** that allows light to pass. The first blocking part BLP**1** may correspond to the second opening area OPA**2**, the third opening area OPA**3**, and the light blocking area LBA surrounding the third opening area OPA**3** of the upper substrate TSUB. The first open part OPP**1** may correspond to an area excluding (or external to) the first blocking part BLP**1**.

[0131] As shown in FIGS. **9** and **10**, the first color filter BCF patterned according to the pattern of the first blocking part BLP**1** and the first open part OPP**1** may be formed.

[0132] As the first color filter BCF overlaps the first opening area OPA**1**, the light emitted from the first opening area OPA**1** may have a blue color.

[0133] The first color filter BCF may overlap the light blocking area LBA surrounding the second opening area OPA**2** and may not be formed in the second opening area OPA**2**. Accordingly, a first opening OP**1** defining the second opening area OPA**2** may be formed in the first color filter BCF.

[0134] The first color filter BCF may not overlap the light blocking area LBA surrounding the third opening area OPA**3**. In other words, the first color filter BCF may not define the third opening area OPA**3**.

[0135] Referring to FIG. **11**, a preliminary second color filter RCF' may be formed on the first color filter BCF. In an embodiment, photoresist may be entirely applied on the first color filter BCF. In this disclosure, the photoresist may be described as a negative photoresist, but the disclosure is not limited thereto.

[0136] Referring to FIGS. **12**, **13**, and **14**, the second color filter RCF may be formed on the first color filter BCF.

[0137] In detail, FIG. **12** may illustrate a second mask MK**2** for exposing the preliminary second color filter RCF'. As shown in FIG. **12**, the second mask MK**2** may include a second blocking part BLP**2** that blocks light and a second open part OPP**2** that allows light to pass. The second blocking part BLP**2** may correspond to the third opening area OPA**3**, the first opening area OPA**1**, and the light blocking area LBA surrounding the first opening area OPA**1** of the upper substrate TSUB. The second open part OPP**2** may correspond to an area excluding the second blocking part BLP**2**.

[0138] As shown in FIGS. **13** and **14**, the second color filter RCF patterned according to the pattern of the second blocking part BLP**2** and the second open part OPP**2** may be formed.

[0139] As the second color filter RCF overlaps the second opening area OPA**2**, the light emitted from the second opening area OPA**2** may have a red color.

[0140] The second color filter RCF may overlap the light blocking area LBA surrounding the third opening area OPA**3** and may not be formed in the third opening area OPA**3**. Accordingly, a second opening OP**2** defining the third opening area OPA**3** may be formed in the second color filter RCF.

[0141] The second color filter RCF may not overlap the light blocking area LBA surrounding the first opening area OPA**1**. In other words, the second color filter RCF may not define the first opening area OPA**1**.

[0142] Referring to FIG. **15**, a preliminary third color filter GCF' may be formed on the second color filter RCF. In an embodiment, photoresist may be entirely applied on the second color filter RCF. In this disclosure, the photoresist may be described as a negative photoresist, but the disclosure is not limited thereto.

[0143] Referring to FIGS. **16**, **17**, and **18**, the third color filter GCF may be formed on the second color filter RCF.

[0144] In detail, FIG. **16** may illustrate a third mask MK**3** for exposing the preliminary third color filter GCF'. As shown in FIG. **16**, the third mask MK**3** may include a third blocking part BLP**3** that blocks light and a third open part OPP**3** that allows light to pass. The third blocking part BLP**3** may correspond to the first opening area OPA**1**, the second opening area OPA**2**, and the light blocking area LBA surrounding the second opening area OPA**2** of the upper substrate TSUB. The third open part OPP**3** may correspond to an area excluding the third blocking part BLP**3**.

[0145] As shown in FIGS. **17** and **18**, the third color filter GCF patterned according to the pattern of the third blocking part BLP**3** and the third open part OPP**3** may be formed.

[0146] As the third color filter GCF overlaps the third opening area OPA**3**, the light emitted from the third opening area OPA**3** may have a green color.

[0147] The third color filter GCF may overlap the light blocking area LBA surrounding the first opening area OPA**1** and may not be formed in the first opening area OPA**1**. Accordingly, a third opening OP**3** defining the first opening area OPA**1** may be formed in the third color filter GCF.

[0148] The third color filter GCF may not overlap the light blocking area LBA surrounding the second opening area OPA**2**. In other words, the third color filter GCF may not define the second opening area OPA**2**.

[0149] Referring to FIG. **19**, the bank BK may be disposed on the upper substrate TSUB and may overlap the light blocking area LBA. In an embodiment, the bank BK may be disposed on the third color filter GCF, and may overlap at least two color filters among the first to third color filters BCF, RCF, and GCF. In an embodiment, the bank BK may be disposed on the second color filter RCF and may overlap at least one color filter among the first and second color filters BCF and RCF.

[0150] Referring to FIG. **20**, the protective layer PL, the first to third color conversion patterns CT**1**, CT**2**, and CT**3**, the capping layer CAP, and the filler FM may be sequentially formed on the bank BK.

[0151] According to the color conversion substrate **2000** according to an embodiment of the disclosure, the color filter may define only one adjacent opening area and not define another opening area. For example, the first color filter BCF may define the second opening area OPA**2** and may not define the third opening area OPA**3**. The second color filter RCF may define the third opening area OPA**3** and may not define the first opening area OPA**1**. The third color filter GCF may define the first opening area OPA**1** and may not define the second opening area OPA**2**. Accordingly, a margin for the width WBK of the bank BK in the first direction D**1** may be secured, and the pitch between the first to third opening areas OPA**1**, OPA**2**, and OPA**3** may be reduced. Accordingly, the resolution of the display device DD including the color conversion substrate **2000** can be improved.

[0152] FIG. **21** is a schematic cross-sectional view illustrating a color conversion substrate included in a display device according to an embodiment of the disclosure.

[0153] FIG. **21** illustrate that a color conversion substrate **2100** included in a display device according to an embodiment of the disclosure may include first to third color filters BCF, RCF, and GCF.

[0154] The first color filter BCF may be disposed on the upper substrate TSUB, may overlap the first opening area OPA**1**, and may define the second opening area OPA**2** and the third opening area OPA**3**. In other words, the first color filter BCF may define two adjacent opening areas.

[0155] The second color filter RCF may be disposed on the first color filter BCF, may overlap the second opening area OPA**2**, and may define the third opening area OPA**3** and may not define the first opening area OPA**1**. In other words, the second color filter RCF may define only one adjacent opening area and may not define another opening area.

[0156] The third color filter GCF may be disposed on the second color filter RCF, may overlap the third opening area OPA**3**, may define the first opening area OPA**1**, and may not define the second opening area OPA**2**. In other words, the third color filter GCF may define only one adjacent opening area and may not define another opening area.

[0157] According to the color conversion substrate **2100** according to an embodiment of the disclosure, the color filter formed at the bottom may define two adjacent opening areas.

For example, the first color filter BCF may define a second opening area OPA**2** and a third opening area OPA**3**. Each of the different color filters may define only one adjacent opening area and may not define another opening area. For example, the second color filter RCF may define the third opening area OPA**3** and may not define the first opening area OPA**1**. The third color filter GCF may define the first opening area OPA**1** and may not define the second opening area OPA**2**. Accordingly, a margin for the width WBK of the bank BK in the first direction D**1** may be secured, and the pitch between the first to third opening areas OPA**1**, OPA**2**, and OPA**3** may be reduced. Accordingly, the resolution of the display device including the color conversion substrate **2100** can be improved.

[0158] FIG. **22** is a block diagram illustrating an electronic device according to an embodiment of the disclosure.

[0159] Referring to FIG. **22**, in an embodiment, an electronic device **900** may include a processor **910**, a memory device **920**, a storage device **930**, an input/output ("I/O") device **940**, a power supply **950**, and a display device **960**. Here, the display device **960** may correspond to the display device DD of FIG. **1**. The electronic device **900** may further include a plurality of ports for communicating with a video card, a sound card, a memory card, a universal serial bus ("USB") device, or the like. In an embodiment, the electronic device **900** may be implemented as a television. In another embodiment, the electronic device **900** may be implemented as a smart phone. However, embodiments are not limited thereto, in another embodiment, the electronic device **900** may be implemented as a cellular phone, a video phone, a smart pad, a smart watch, a tablet personal computer ("PC"), a car navigation system, a computer monitor, a laptop, a head disposed (e.g., mounted) display ("HMD"), or the like.

[0160] The processor **910** may perform various computing functions. In an embodiment, the processor **910** may be a microprocessor, a central processing unit ("CPU"), an application processor ("AP"), or the like. The processor **910** may be coupled to other components via an address bus, a control bus, a data bus, or the like. In an embodiment, the processor **910** may be coupled to an extended bus such as a peripheral component interconnection ("PCI") bus.

[0161] The memory device **920** may store data for operations of the electronic device **900**. In an embodiment, the memory device **920** may include at least one non-volatile memory device such as an erasable programmable read-only memory ("EPROM") device, an electrically erasable programmable read-only memory ("EEPROM") device, a flash memory device, a phase change random access memory ("PRAM") device, a resistance random access memory ("RRAM") device, a nano floating gate memory ("NFGM") device, a polymer random access memory ("PoRAM") device, a magnetic random access memory ("MRAM") device, a ferroelectric random access memory ("FRAM") device, or the like, and/or at least one volatile memory device such as a dynamic random access memory ("DRAM") device, a static random access memory ("SRAM") device, a mobile DRAM device, or the like.

[0162] In an embodiment, the storage device **930** may include a solid state drive ("SSD") device, a hard disk drive ("HDD") device, a CD-ROM device, or the like. In an embodiment, the I/O device **940** may include an input device such as a keyboard, a keypad, a mouse device, a touchpad, a touch-screen, or the like, and an output device such as a printer, a speaker, or the like.

[0163] The power supply **950** may provide power for operations of the electronic device **900**. The power supply **950** may provide power to the display device **960**. The display device **960** may be coupled to other components via the buses or other communication links. In an embodiment, the display device **960** may be included in the I/O device **940**.

[0164] Although certain embodiments and implementations have been described herein, other embodiments and modifications will be apparent from this disclosure. Accordingly, the disclosure is not limited to such embodiments, but rather to the broader scope of the appended claims and various obvious modifications and equivalent arrangements as would be apparent to a person of ordinary skill in the art.

What is claimed is:

1. A color conversion substrate comprising:

an upper substrate including a first opening area, a second opening area adjacent to the first opening area, and a third opening area adjacent to the second opening area;

a first color filter disposed on the upper substrate and having a first opening which defines the second opening area;

a second color filter disposed on the first color filter and having a second opening which defines the third opening area; and

a third color filter disposed on the second color filter and having a third opening which defines the first opening area,

wherein the first color filter does not overlap a light blocking area surrounding the third opening area.

2. The color conversion substrate of claim **1**, wherein the first color filter overlaps a light blocking area surrounding the second opening area.

3. The color conversion substrate of claim **1**, wherein the first color filter overlaps the first opening area and a light blocking area surrounding the first opening area.

4. The color conversion substrate of claim **1**, wherein the second color filter does not overlap a light blocking area surrounding the first opening area.

5. The color conversion substrate of claim **4**, wherein the second color filter overlaps a light blocking area surrounding the third opening area.

6. The color conversion substrate of claim **4**, wherein the second color filter overlaps the second opening area and a light blocking area surrounding the second opening area.

7. The color conversion substrate of claim **1**, wherein the third color filter does not overlap a light blocking area surrounding the second opening area.

8. The color conversion substrate of claim **7**, wherein the third color filter overlaps a light blocking area surrounding the first opening area.

9. The color conversion substrate of claim **7**, wherein the third color filter overlaps the third opening area and a light blocking area surrounding the third opening area.

10. The color conversion substrate of claim **1**, wherein the first, second, and third opening areas are arranged side by side.

11. The color conversion substrate of claim **1**, wherein

the first color filter is a blue color filter,

the second color filter is a red color filter, and

the third color filter is a green color filter.

12. The color conversion substrate of claim 1, further comprising:

a bank disposed on the upper substrate and overlapping a light blocking pattern surrounding the first to third opening areas.

13. The color conversion substrate of claim 12, further comprising:

a first color conversion pattern disposed on the first color filter, the first color conversion pattern accommodated by the bank and including first quantum dots;

a second color conversion pattern disposed on the second color filter, the second color conversion pattern accommodated by the bank and including second quantum dots; and

a third color conversion pattern disposed on the third color filter, the third color conversion pattern accommodated by the bank and including third quantum dots.

14. A display device comprising:

an emission substrate and a color conversion substrate disposed on the emission substrate, wherein

the emission substrate includes:

a lower substrate;

a first pixel electrode disposed on the lower substrate;

a second pixel electrode disposed on the lower substrate and adjacent to the first pixel electrode; and

a third pixel electrode disposed on the lower substrate and adjacent to the second pixel electrode,

the color conversion substate includes:

an upper substrate including a first opening area, a second opening area adjacent to the first opening area, and a third opening area adjacent to the second opening area;

a first color filter disposed between the lower substrate and the upper substrate, the first color filter having a first opening which defines the second opening area;

a second color filter disposed between the first color filter and the lower substrate, the second color filter having a second opening which defines the third opening area; and

a third color filter disposed between the second color filter and the lower substrate, the third color filter having a third opening which defines the first opening area, and

the first color filter does not overlap a light blocking area surrounding the third opening area.

15. The display device of claim 14, wherein the first color filter overlaps a light blocking area surrounding the second opening area.

16. The display device of claim 14, wherein the first color filter overlaps the first opening area and a light blocking area surrounding the first opening area.

17. The display device of claim 14, wherein the second color filter does not overlap a light blocking area surrounding the first opening area.

18. The display device of claim 14, wherein

the first color filter overlaps the first pixel electrode,

the second color filter overlaps the second pixel electrode, and

the third color filter overlaps the third pixel electrode.

19. The display device of claim 14, further comprising:

an emission layer disposed on the first to third pixel electrodes; and

a common electrode disposed on the emission layer.

20. The display device of claim 14, further comprising:

an active pattern disposed on the lower substrate;

a gate electrode disposed on the active pattern; and

a connection electrode disposed on the gate electrode and electrically connected to the active pattern.

21. An electronic device comprising:

a display device; and

a power supply configured to provide power to the display device,

wherein the display device comprises:

an emission substrate and a color conversion substrate disposed on the emission substrate, wherein

the emission substrate includes:

a lower substrate;

a first pixel electrode disposed on the lower substrate;

a second pixel electrode disposed on the lower substrate and adjacent to the first pixel electrode; and

a third pixel electrode disposed on the lower substrate and adjacent to the second pixel electrode,

the color conversion substate includes:

an upper substrate including a first opening area, a second opening area adjacent to the first opening area, and a third opening area adjacent to the second opening area;

a first color filter disposed between the lower substrate and the upper substrate, the first color filter having a first opening which defines the second opening area;

a second color filter disposed between the first color filter and the lower substrate, the second color filter having a second opening which defines the third opening area; and

a third color filter disposed between the second color filter and the lower substrate, the third color filter having a third opening which defines the first opening area, and

the first color filter does not overlap a light blocking area surrounding the third opening area.

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