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(54) **NEURAL INTERFACE AND METHOD FOR MANUFACTURING SAME**

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(57) **ABSTRACT**

Disclosed herein are a neural interface and a method for fabricating the neural interface. The neural interface comprises: an electrode section for neural stimulation and neural signal recording; a first region defined by a first hole; and a second region defined by a second hole disposed within the first region, wherein the electrode section comprises a first electrode section and a second electrode section, either the first electrode section or the second electrode section being disposed within the second region.

The fabricating method comprises the steps of synthesizing a shape memory polymer; first coating a substrate with the shape memory polymer; forming a photoresist on the shape memory polymer; masking the photoresist; sputtering an electrode material; patterning the electrode material through a photolithography process; second coating the shape memory polymer; and etching the shape memory polymer.

FIG. 1

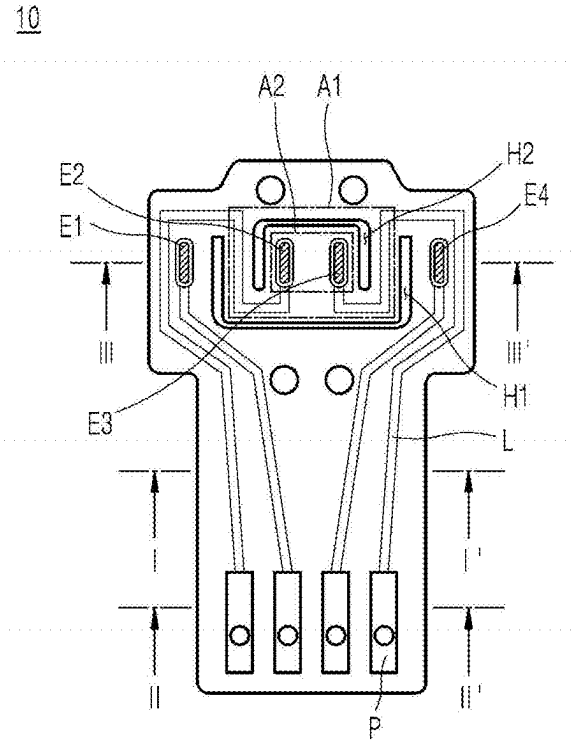

10
A2
A1
H2
E2
E4
E1
III
III'
H1
E3
L
I
I'
II
II'
P

FIG. 2

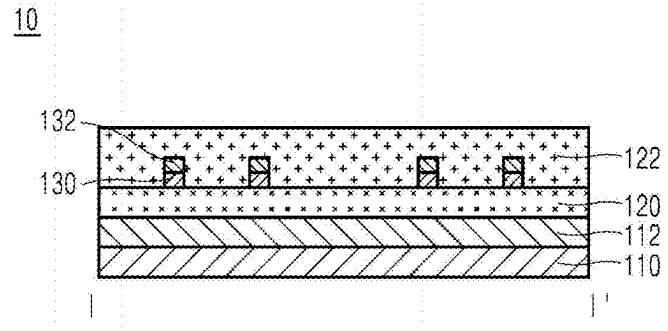

10
132
130
122
120
112
110
I
I'

FIG. 3

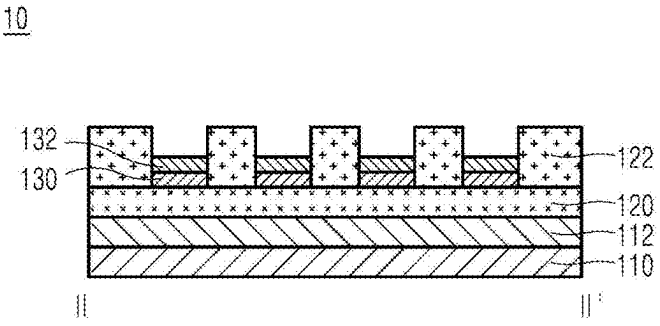

10
132
130
122
120
112
110
II
II'

FIG. 4

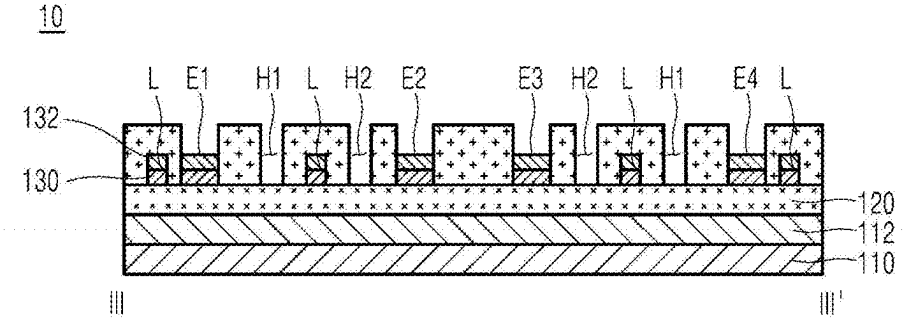

10
L
E1
H1
L
H2
E2
E3
H2
L
H1
E4
L
132
130
120
112
110
III
III'

FIG. 5

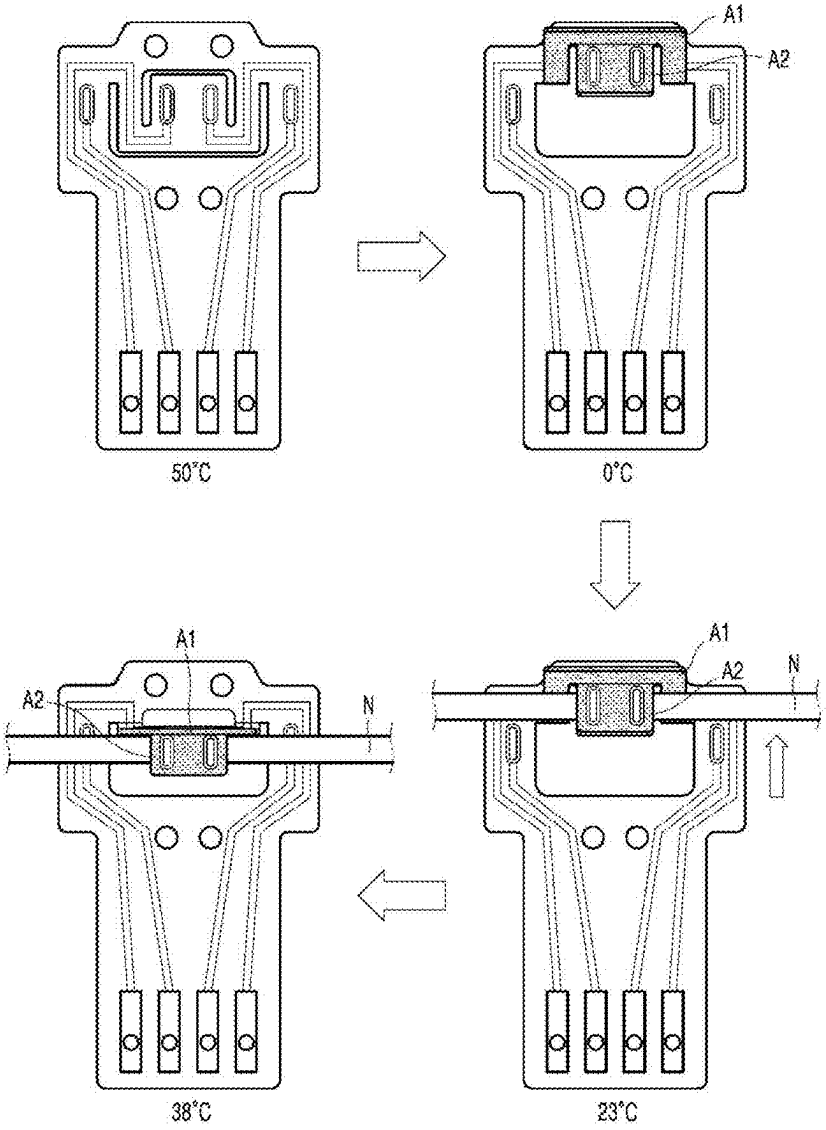


FIG. 6

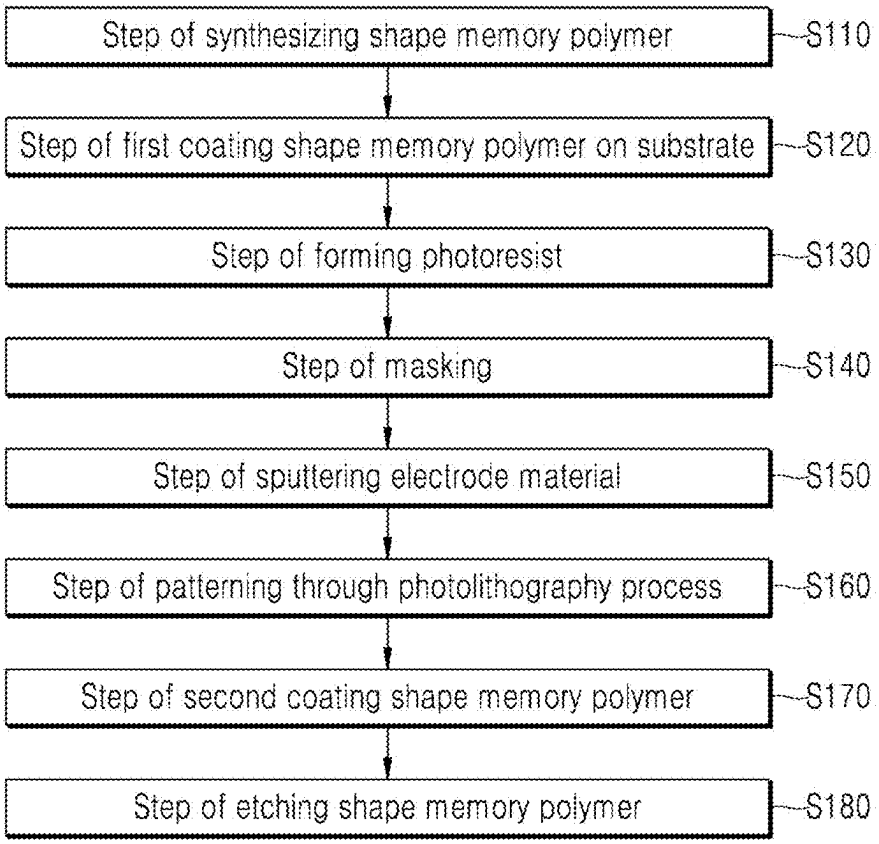

Step of synthesizing shape memory polymer
S110
Step of first coating shape memory polymer on substrate
S120
Step of forming photoresist
S130
Step of masking
S140
Step of sputtering electrode material
S150
Step of patterning through photolithography process
S160
Step of second coating shape memory polymer
S170
Step of etching shape memory polymer
S180

FIG. 7a

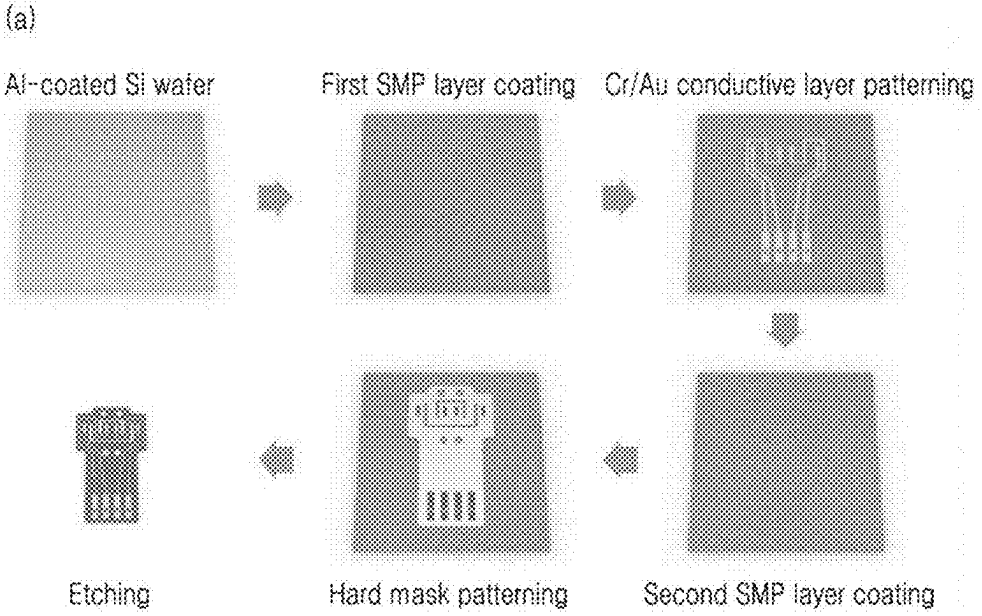

(a)
Al-coated Si wafer
First SMP layer coating
Cr/Au conductive layer patterning
Etching
Hard mask patterning
Second SMP layer coating

FIG. 7b

(b)

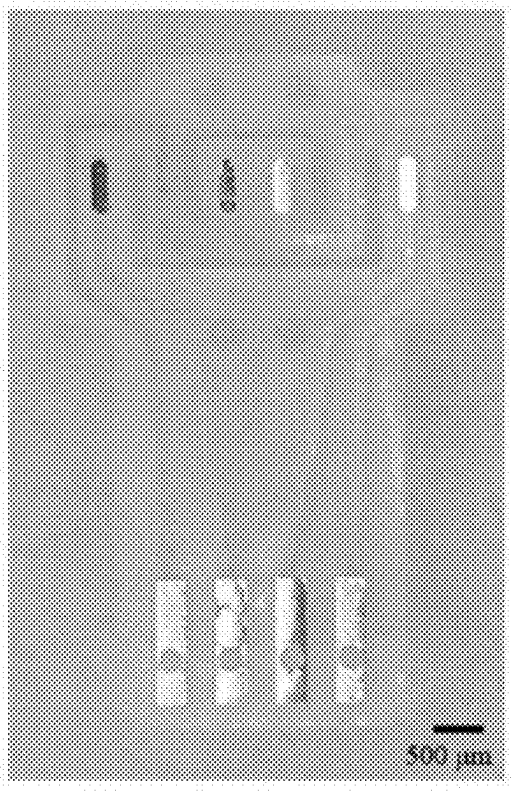


FIG. 8a

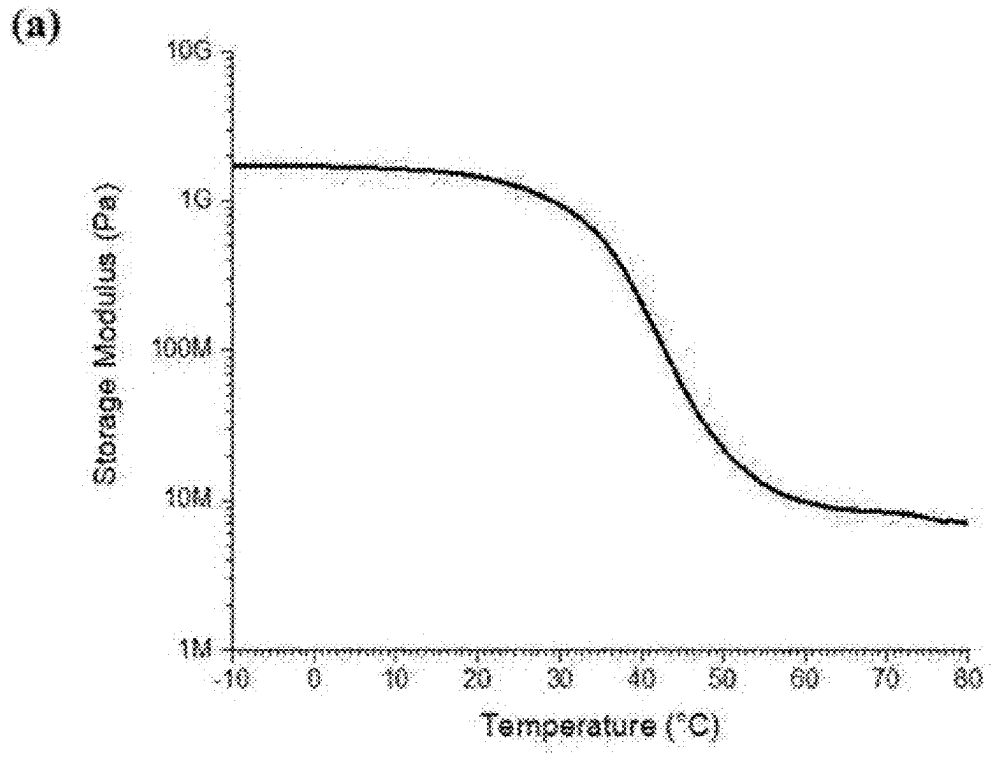

(a)
10G
1G
100M
10M
1M
Storage Modulus (Pa)
-10
0
10
20
30
40
50
60
70
80
Temperature (°C)

FIG. 8b

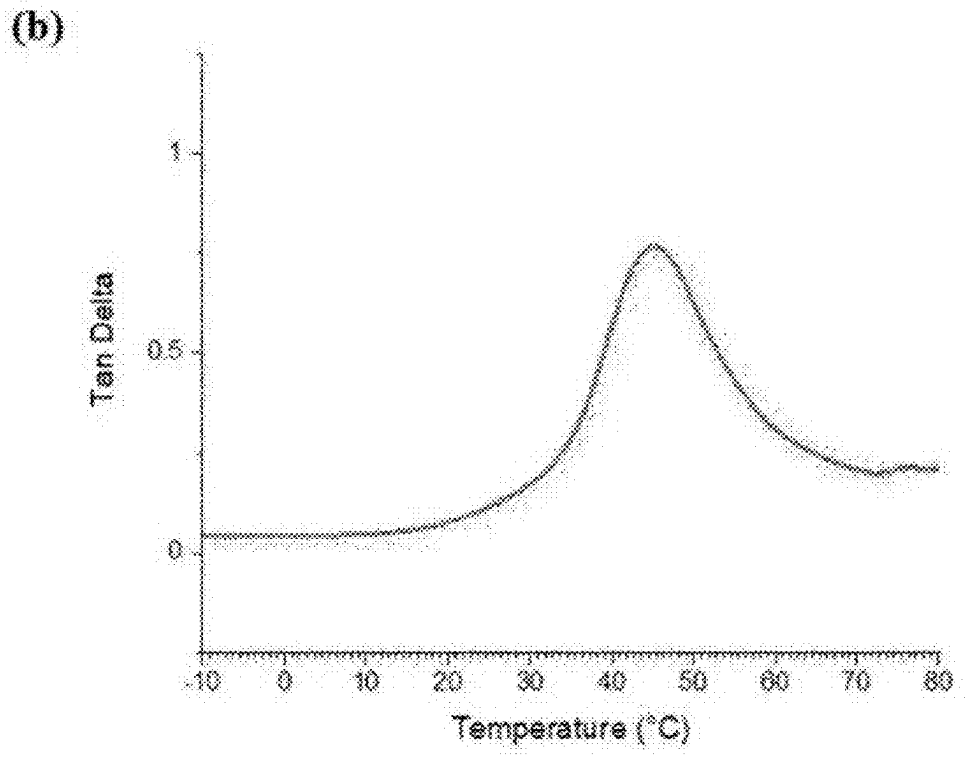


FIG. 9a

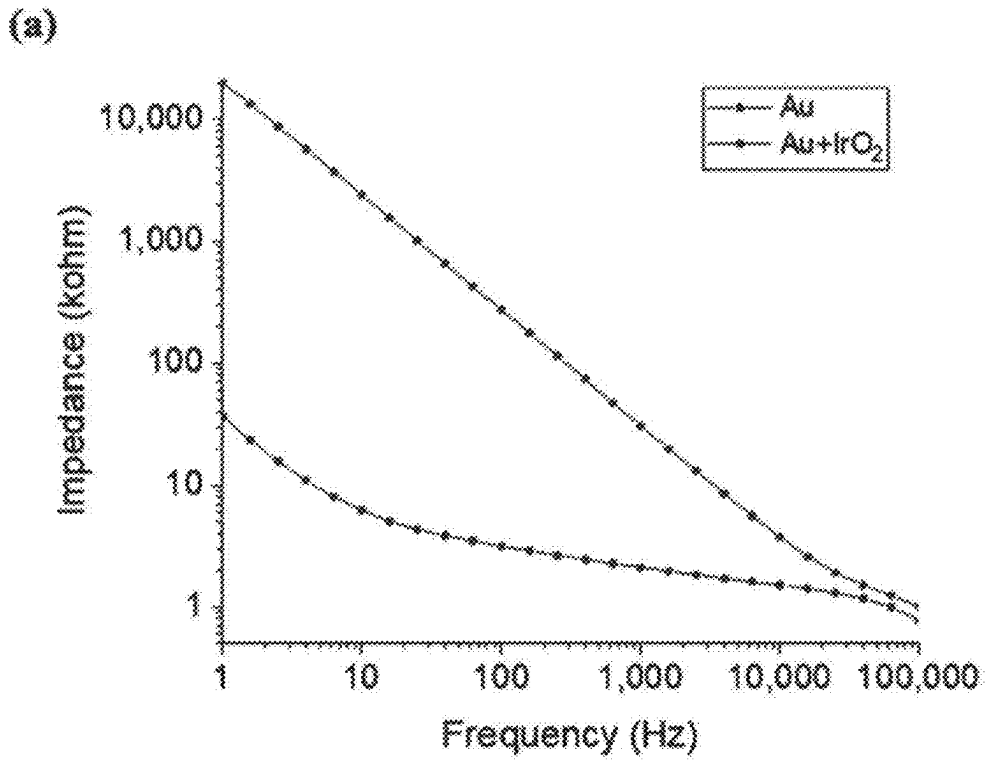

(a)
Au
Au+IrO2
Impedance (kohm)
10,000
1,000
100
10
1
1
10
100
1,000
10,000
100,000
Frequency (Hz)

FIG. 9b

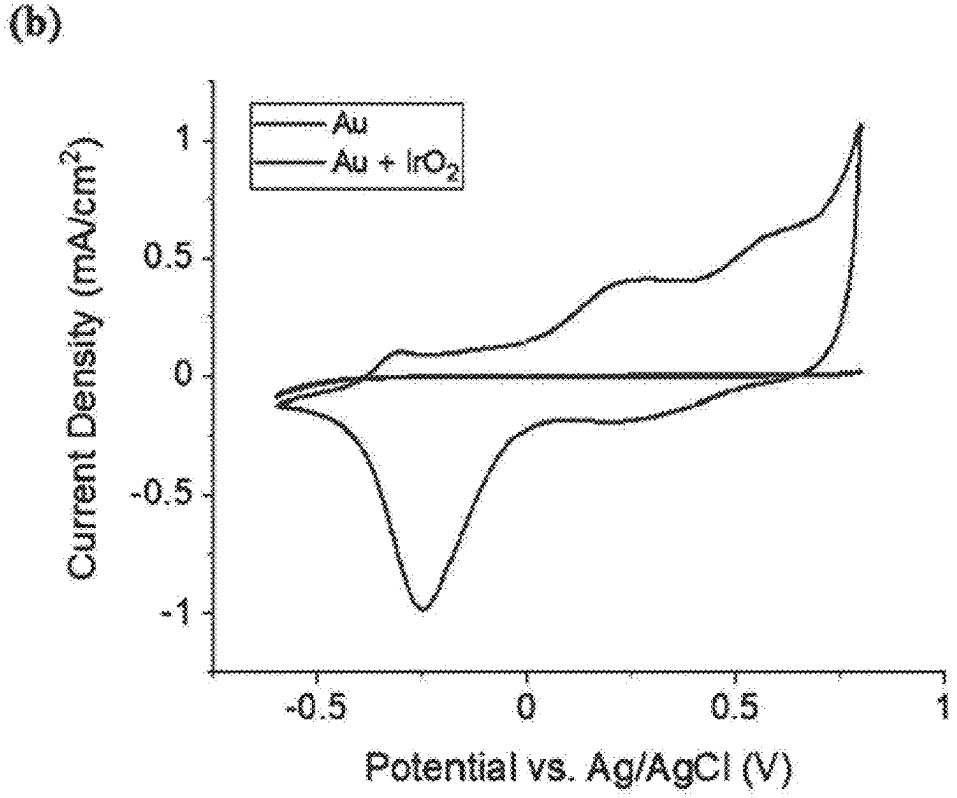

(b)
Au
Au + IrO2
Current Density (mA/cm2)
1
0.5
0
-0.5
-1
-0.5
0
0.5
1
Potential vs. Ag/AgCl (V)

FIG. 10a

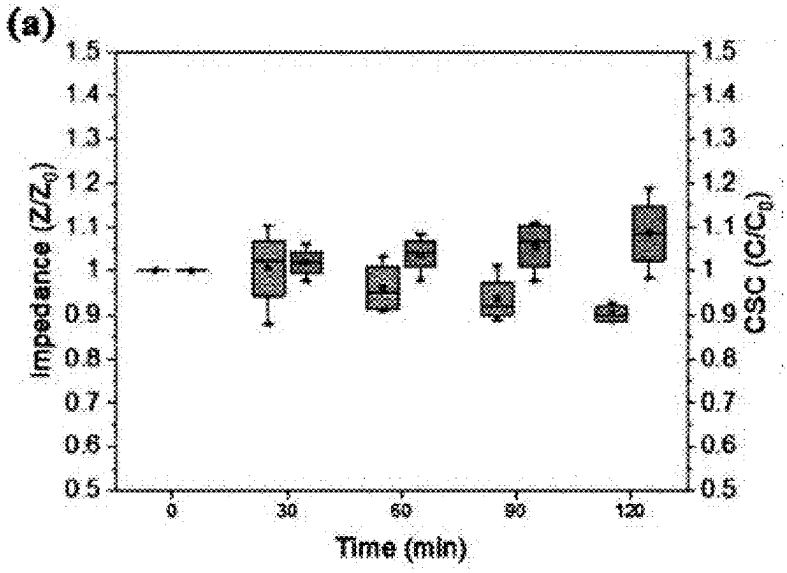


FIG. 10b

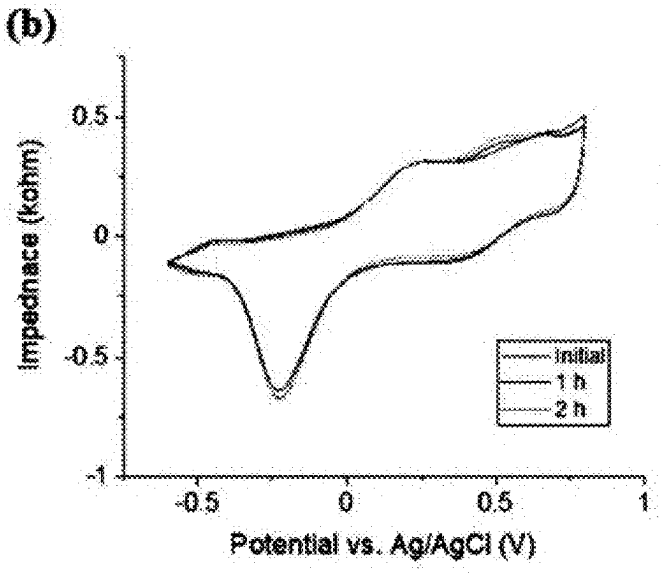


FIG. 10c

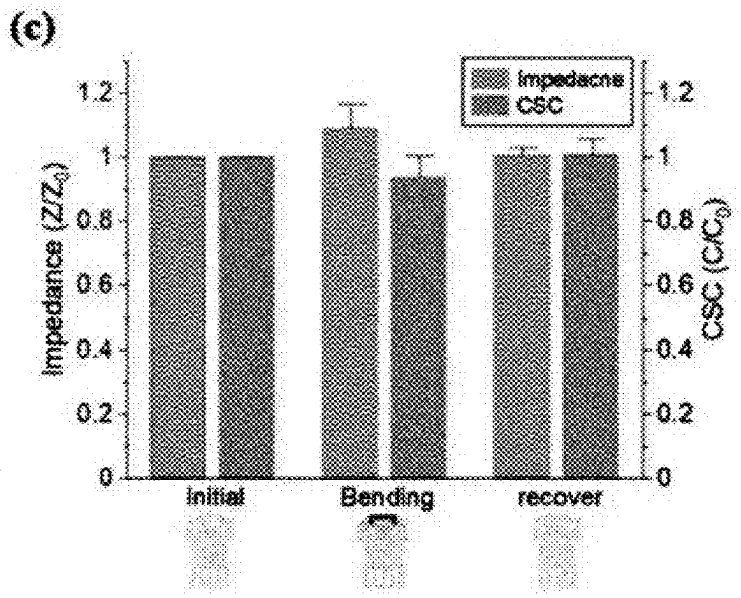

(c)
impedance
CSC
Impedance (Z/Z0)
CSC (C/C0)
1.2
1
0.8
0.6
0.4
0.2
0
Initial
Bending
recover

FIG. 11a

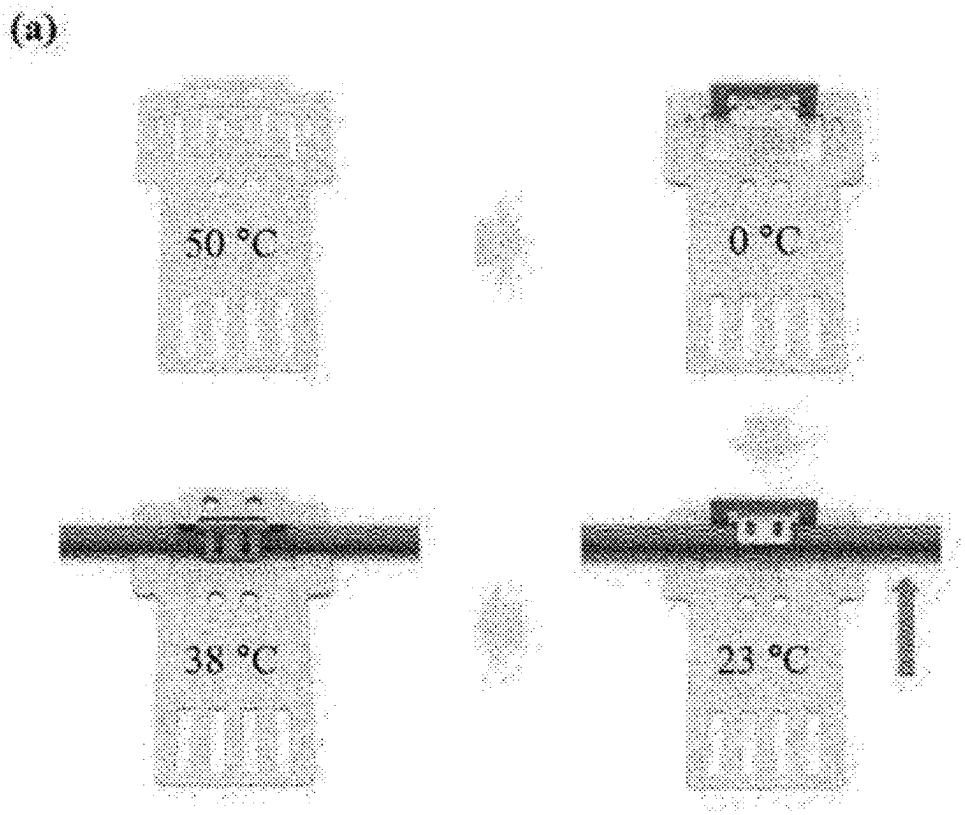


FIG. 11b

FIG. 11c

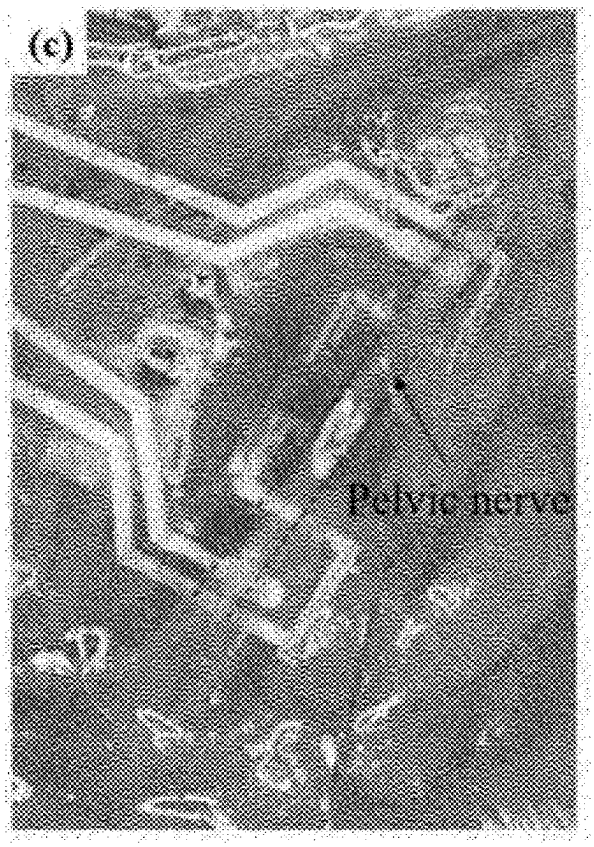


FIG. 12a

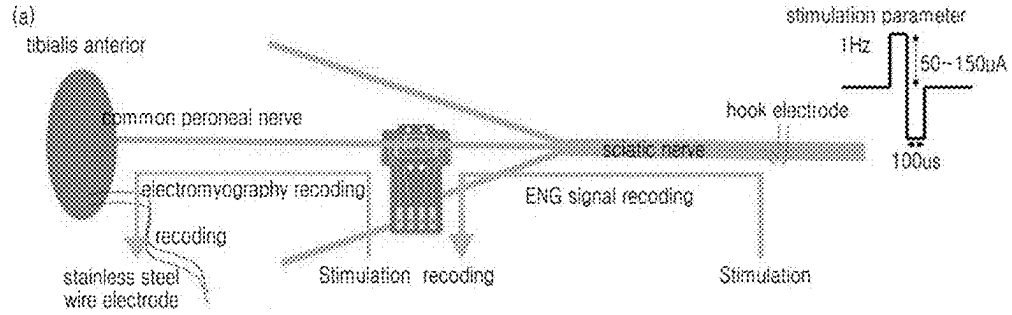
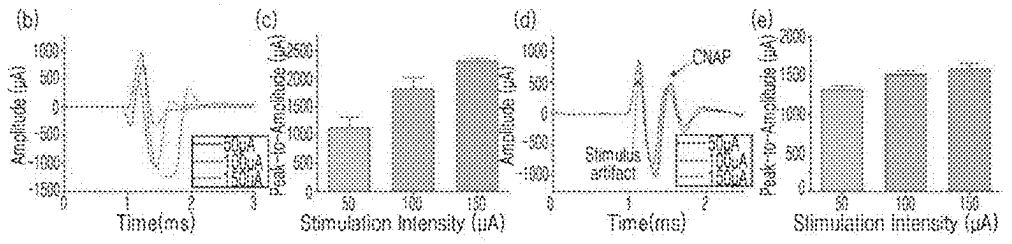


FIG. 12b



NEURAL INTERFACE AND METHOD FOR MANUFACTURING SAME

TECHNICAL FIELD

[0001] Various embodiments of the present disclosure relate to a neural interface and a fabricating method therefor and, more specifically, to a neural interface with a dual clip design utilizing shape memory polymers and a method for fabricating same.

BACKGROUND ART

[0002] For use in implantable neural interfaces for recording and stimulating neural signals of peripheral nerves, it is very important to select materials that have biocompatibility to minimize immune response within the body, as well as softness similar to nerves. Also, the design and shape for maximizing the performance of insertion, recording, and stimulation of the neural interface are crucial as they directly the stability of the neural interface.

[0003] Shape memory polymers are frequently used as biomedical engineering materials due to their biocompatibility and shape memory effects. Previously, neural interfaces utilizing shape memory polymers have been developed, but they were used as additional substrates leveraging only the shape memory effect, separate from neural interfaces including conductive electrodes. Because of the use of relatively thick substrates, the overall neural interface becomes thicker, which reduces its stability for long-term use and makes it unsuitable for insertion into very small peripheral nerves.

[0004] Recently, there have been implementations of neural interfaces using shape memory polymers that are thinner and can be micro-patterned, allowing for the recording of more neural signal channels compared to conventional commercialized silicon cuff electrodes. However, the shape memory polymers used have a high glass transition temperature (66.3° C. in a dry state), resulting in insufficient softness at room or body temperature, and the high glass transition temperature limits the utilization of shape memory effects at physiological temperatures. Additionally, the use of E-Beam for depositing gold conductive layers in the process is costly, making it unsuitable for mass production.

DISCLOSURE OF INVENTION

Technical Problem

[0005] To address the problems encountered in the related art, the present disclosure is to provide a neural interface that includes a shape memory polymer exhibiting shape memory effects at physiological temperatures and a design that allows for dual clipping, and a fabricating method therefor.

Solution to Problem

[0006] A neural interface according to various embodiments of the present disclosure includes: an electrode section for neural stimulation and neural signal recording; a first region defined by a first hole; and a second region defined by a second hole disposed within the first region, wherein the electrode section includes a first electrode section and a second electrode section, either the first electrode section or the second electrode section being disposed within the second region.

[0007] A method for fabricating a neural interface according to various embodiments of the present disclosure may include the steps of: synthesizing a shape memory polymer; first coating a substrate with the shape memory polymer; forming a photoresist on the shape memory polymer; masking the photoresist; sputtering an electrode material; patterning the electrode material through a photolithography process; second coating the shape memory polymer; and etching the shape memory polymer.

Advantageous Effects of Invention

[0008] The neural interface of the present disclosure can be easily inserted into very small nerves due to the shape memory effect of the shape memory polymer. Additionally, the low glass transition temperature (44° C. in a dry state) enables morphological transformation through the shape memory effect without stressing the biological tissues, facilitating easy implantation of the neural interface and minimizing damage to the neural interface and the neural tissue. The neural interface also exhibits a Young's modulus of 400 MPa at 37° C., which is softer than the conventional polyimide (2.5 GPa) used for neural interface substrates.

[0009] The dual clip design of the neural interface allows the electrodes to contact both the upper and lower parts of the nerve, enabling stable fixation by double clipping the nerve.

[0010] In the method for fabricating a neural interface according to the present disclosure, sputtering and photolithography processes are used to directly deposit and pattern the conductive material, eliminating the need for pre-metal layer processes (stamping), which allows for fabrication with a single wafer. Additionally, using sputtering instead of the conventional E-beam process for metal deposition reduces process costs and makes the method more suitable for mass production.

BRIEF DESCRIPTION OF DRAWINGS

[0011] FIG. **1** is a plan view of a neural interface according to an embodiment of the present disclosure.

[0012] FIG. **2** is a cross-sectional view taken along line I-I' of FIG. **1**.

[0013] FIG. **3** is a cross-sectional view taken along line II-II' of FIG. **1**.

[0014] FIG. **4** is a cross-sectional view taken along line III-III' of FIG. **1**.

[0015] FIG. **5** is a schematic diagram of the injection process of the neural interface according to an embodiment of the present disclosure.

[0016] FIG. **6** is a process flowchart of the method for fabricating the neural interface according to an embodiment of the present disclosure.

[0017] FIG. **7** is a schematic diagram of the fabricating process of the neural interface according to an embodiment of the present disclosure.

[0018] FIG. **8** shows (a) a graph of the storage modulus of the shape memory polymer and (b) a graph of the loss factor (tan δ).

[0019] FIG. **9** shows (a) impedance measurement results of the gold (Au) deposited neural interface and IrO_2 coated neural interface, and (b) CV test results.

[0020] FIG. **10** shows (a) a graph of the impedance and charge storage capacity (CSC) changes with applied voltage, (b) a CV curve with applied voltage over time, and (c) the bending process stability.

[0021] FIG. **11** shows (a) a schematic diagram explaining the implantation process of the neural interface, (b) a photograph of the neural interface implanted in the CPN, and (c) a photograph of the neural interface implanted in the PN.

[0022] FIG. **12** shows (a) a schematic diagram of the stimulation and recording process, (b) recorded EMG signals according to neural stimulation through the neural interface, (c) a bar graph of the peak-to-peak amplitude of the EMG signals, (d) recorded EMG signals according to neural stimulation through the hook electrode, and (e) a bar graph of the peak-to-peak amplitude of the CNAP.

BEST MODE FOR CARRYING OUT THE INVENTION

[0023] Hereinafter, various embodiments of the present disclosure are described with reference to the accompanying drawings. The embodiments and the terminology used are not intended to limit the techniques described herein to specific forms of implementation, and it should be understood that various modifications, equivalents, and/or substitutions are included.

[0024] A detailed description will be given of the embodiments of the present disclosure with reference to the accompanying drawings as follows.

[0025] FIG. **1** is a plan view of a neural interface according to an embodiment of the present disclosure. FIG. **2** is a cross-sectional view taken along line I-I' of FIG. **1**. FIG. **3** is a cross-sectional view taken along line II-II' of FIG. **1**. FIG. **4** is a cross-sectional view taken along line III-III' of FIG. **1**.

[0026] Referring to FIGS. **1** to **4**, the neural interface (**10**) according to an embodiment of the present disclosure includes a dual clip design with electrode sections (E**1**, E**2**, E**3**, E**4**), an electrode pad section (P), and wiring (L) disposed on a substrate (**110**).

[0027] The electrode sections (E**1**, E**2**, E**3**, E**4**) may be positioned on the upper part of the neural interface (**10**). The electrode sections (E**1**, E**2**, E**3**, E**4**) can contact nerves for neural signal recording and stimulation. The upper part of the neural interface **10** may have a dual clip design. Specifically, the upper part of the neural interface **10** may include a first hole (H**1**), a first region (A**1**) defined by the first hole (H**1**), a second hole (H**2**) disposed within the first region (A**1**), and a second region (A**2**) defined by the second hole (H**2**).

[0028] The first hole (H**1**) may have a "[" shape, allowing the first region (A**1**) to bend vertically. Similarly, the second region (A**2**) can also bend vertically due to the second hole (H**2**).

[0029] The electrode section (E**1**, E**2**, E**3**, E**4**) may contact both the upper and lower parts of the nerve. Specifically, the electrode section (E**1**, E**2**, E**3**, E**4**) may include a first electrode section (E**1**), a second electrode section (E**2**), a third electrode section (E**3**), and a fourth electrode section (E**4**). The first electrode section (E**1**) and the fourth electrode section (E**4**) may be positioned at the edges of the neural interface (**10**), where the first electrode section (E**1**) and the fourth electrode section (E**4**) can contact the lower part of the nerve.

[0030] The second electrode section (E**2**) and the third electrode section (E**3**) may be positioned at the center of the neural interface **10**, particularly within the second region (A**2**). The second electrode section (E**2**) and the third electrode section (E**3**) positioned at the center of the neural interface **10** can contact the upper part of the nerve through the movement of the first region (A**1**) and the second region (A**2**).

[0031] Thus, the present disclosure can stably fix the nerve by double clipping.

[0032] The electrode pad section (P) may be positioned at the lower part of the neural interface **10** and connected to external electrical signals.

[0033] The wiring (L) may electrically connect the electrode section (E**1**, E**2**, E**3**, E**4**) and the electrode pad section (P).

[0034] With reference to FIGS. **2** to **4**, the layered structure of the neural interface (**10**) is explained. The neural interface (**10**) includes a substrate (**110**) with a coating layer (**112**), a first SMP layer (**120**), an adhesion layer (**130**), a conductive layer (**132**), and a second SMP layer (**122**).

[0035] The substrate (**110**) with the coating layer (**112**) may be, for example, an Si wafer coated with Al.

[0036] The first SMP layer (**120**) may include a shape memory polymer (SMP) with a glass transition temperature (Tg) close to body temperature. The shape memory polymer may be polymerized using different types of multi-thiol monomers. Specifically, the shape memory polymer is polymerized via a thiol-ene reaction, using three monomers: 1,3,5-triallyl-1,3,5-triazine-2,4,6(1H,3H,5H)-trione (TATATO), trimethylolpropanetris(3-mercaptopropionate) (TMTMP), and tricyclodecanedimethanoldiacrylate (TCMDA).

[0037] The adhesion layer (**130**) is an intermediate layer between the first SMP layer (**120**) and the conductive layer (**132**) to enhance the adhesion of the conductive layer (**132**). For example, the adhesion layer (**130**) may include materials like chromium (Cr), titanium (Ti), or titanium/titanium nitride (Ti/TiN). The adhesion layer (**130**) may include various materials that can enhance the adhesion between the first SMP layer (**120**) and the conductive layer (**132**).

[0038] The conductive layer (**132**) is placed on the adhesion layer (**130**) and may transmit electrical signals. For instance, the conductive layer (**132**) may include gold (Au), platinum, titanium nitride (TiN), molybdenum (Mo), carbon nanotubes (CNT), or conductive polymers like PEDOT:PSS. The conductive layer (**132**) includes any biocompatible conductive material suitable for neural stimulation and recording.

[0039] To further enhance the stability and recording performance of the neural interface (**10**), additional conductive material may be electrodeposited on the conductive layer (**132**). Coating with the additional conductive material improves the electrochemical performance of the neural interface (**10**). For instance, the additional conductive material may be IrO2, gold (Au), carbon nanotubes (CNT), platinum black (Pt-black), titanium nitride (TiN), conductive polymers including PEDOT:PSS, molybdenum (Mo), or etc. So long as it is lower in resistance and higher in charge transfer capability than the material constituting the conductive layer (**132**), any conductive material may be used as the additionally improved conductive material.

[0040] The adhesion layer (**130**) and the conductive layer (**132**) may be patterned to form the electrode section (E**1**, E**2**, E**3**, E**4**), the electrode pad section (P), and the wiring (L) as shown in FIG. **1**.

[0041] The second SMP layer (**122**) may include the same material as the first SMP layer (**120**) and be positioned on the topmost surface of the neural interface (**10**). The second SMP layer (**122**) may be patterned to expose the electrode section (E**1**, E**2**, E**3**, E**4**) and the electrode pad section (P). Also, the second SMP layer (**122**) may be patterned to form the first hole (H**1**) and the second hole (H**2**).

[0042] The total thickness of the neural interface of the present disclosure may range from 30 nm to 50 nm. This thin thickness allows the neural interface to be easily implanted.

[0043] Turing to FIG. **5**, an injection process of the neural interface is described.

[0044] For implantation, the neural interface is made soft at a sufficiently high temperature (e.g., above 50° C.). The neural interface is then deformed into a shape that is easy to insert and morphologically fixed at 0° C. Specifically, the first region (A**1**) and the second region (A**2**) may each be moved to create a space for nerve insertion and then fixed. After implanting the neural interface into the nerve (N), the shape is restored by spraying saline of the body temperature or similar temperature. Through this process, the neural interface can be easily inserted and fixed to the peripheral nerve (N). Minimizing contact between the neural interface and the neural tissue during the implantation process is crucial to reduce damage on the neural interface and nerve. The present disclosure utilizes the shape memory effect to minimize contact through a self-implantation method.

[0045] The neural interface (**10**) of the present disclosure can be easily inserted into very small nerves through the shape memory effect of the shape memory polymer. Additionally, the low glass transition temperature (44° C.; dry state) allows shape deformation through the shape memory effect without stressing biological tissues, facilitating easy implantation and minimizing damage to both the neural interface and the neural tissue. Furthermore, the neural interface exhibits a Young's modulus of 400 MPa at 37° C., which is softer than conventional polyimide substrates (2.5 GPa).

[0046] The neural interface of the present disclosure meets various conditions such as biocompatibility, thinness, lower Young's modulus, and simplified fabricating through photolithography processes for micro-patterning. Moreover, utilizing the characteristics of shape memory polymers, the neural interface can be easily implanted into small nerves with a 3D structure. The neural interface of the present disclosure is expected to find applications not only in neural modulation for disease treatment but also in recording neural signals for bionic limb operation and nerve stimulation applied techniques for user's sensory feedback.

[0047] Referring to FIG. **6**, a method is elucidated for fabricating a neural interface according to the present disclosure.

[0048] With reference to FIG. **6**, the method for fabricating a neural interface according to the present disclosure includes the following steps of: synthesizing a shape memory polymer (S**110**); first coating the SMP onto a substrate (S**120**); forming a photoresist layer (S**130**); masking (S**140**); sputtering an electrode material (S**150**); patterning through a photolithography process (S**160**); second coating the shape memory polymer (S**170**); and etching the shape memory polymer (S**180**).

[0049] In step (S**110**) of synthesizing a shape memory polymer, the shape memory polymer can be synthesized by polymerizing 1,3,5-triallyl-1,3,5-triazine-2,4,6(1H, 3H, 5H)-trione (TATATO), trimethylolpropanetris(3-mercaptopropionate) (TMTMP), and tricyclodecanedimethanoldiacrylate (TCMDA). In step (S**110**) of synthesizing a shape memory polymer, these three monomers can be polymerized via a thiol-ene reaction. The polymerization of TATATO, TMTMP, and TCMDA affects the molecular weight and chain formation of the polymer, which can alter the glass transition temperature (Tg).

[0050] In this process, 2,2-dimethoxy-2-phenyl-acetophenone (DMPA) can be used as a photoinitiator. By controlling the ultraviolet (UV) exposure time involved in the polymerization process with the photoinitiator, the chain formation of the polymer can be adjusted to lower the glass transition temperature of the resulting shape memory polymer. For example, in one embodiment of the present disclosure, the UV exposure time may be between 20 and 40 minutes, preferably 30 minutes, which thus results in a softer characteristic at the same temperature and enables the utilization of the shape memory effect at physiological temperatures.

[0051] Next, in step (S**120**) of first coating the shape memory polymer onto a substrate, the shape memory polymer synthesized previously may be coated onto the substrate. The substrate may be, for example, a silicon wafer coated with an aluminum thin film. The shape memory polymer may be spin-coated onto the substrate. The spin-coating process facilitates easy control of the coating thickness and allows for a uniform deposition.

[0052] In step (S**130**) of forming a photoresist layer, a photoresist layer may be deposited on the shape memory polymer.

[0053] In step (S**140**) of masking, the photoresist is patterned using a chrome hard mask and a mask aligner, considering the patterns for the electrode section, electrode pad section, and wiring.

[0054] In step (S**150**) of sputtering an electrode material, the entire surface is sputtered with the electrode material. Both the adhesion material and the conductive material are sputtered. For example, chromium (Cr) may be sputtered as an adhesion material, and gold (Au) may be sputtered as a conductive material. However, the embodiments are not limited to these materials, and various biocompatible conductive materials may be used as adhesion and conductive materials.

[0055] When depositing 200 nm of gold (Au) by sputtering, process conditions may be set to be 3 mTorr to 10 mTorr for the chamber pressure, 150 W to 250 W for the applied power, 2 to 5 minutes for the exposure time, and 10 sccm to 30 sccm for argon gas injection rate. Preferably, for 200 nm gold (Au) deposition, the sputtering may be carried out at a chamber pressure of 5 mTorr, an applied power of 200 W, and an exposure time of 3 minutes and 30 seconds, with argon gas injected at a rate of 20 sccm.

[0056] When depositing 50 nm of chromium (Cr) by sputtering, process conditions may be set to be 10 mTorr to 30 mTorr for the chamber pressure, 150 W to 250 W for the applied power, 1 to 3 minutes for the exposure time, and 30 sccm to 70 sccm for argon gas injection rate. Preferably, for 50 nm gold (Au) deposition, the sputtering may be carried out at a chamber pressure of 20 mTorr, an applied power of

200 W, and an exposure time of 2 minutes and 10 seconds, with argon gas injected at a rate of 50 sccm.

[0057] In step (S**160**) of patterning through photolithograph, the photoresist may be removed to pattern the adhesion layer and the conductive layer. This step involves patterning the adhesion layer and the conductive layer into the electrode section, electrode pad section, and wiring patterns.

[0058] In step S**170** of second coating the shape memory polymer, the shape memory polymer is coated using a method identical or similar to the first coating step (S**120**). Specifically, the shape memory polymer is spin-coated over the adhesion layer and the conductive layer.

[0059] In step (S**180**) of etching the shape memory polymer, the shape memory polymer is etched into the desired shape. That is, the shape memory polymer is etched such that the electrode section and the electrode pad section are exposed. Additionally, the first hole and the second hole may be formed to achieve the dual clip design as described in the foregoing. In this regard, when a chrome hard mask is patterned on the shape memory polymer, followed by reactive ion etching (RIE) with oxygen plasma. Specifically, the patterning conditions may be set to be 110 sccm to 130 sccm for oxygen (O_2) flow rate, 10 mTorr to 30 mTorr for chamber pressure, and 1 minute to 5 minutes for purge time. Preferably, the patterning may be carried out at a chamber pressure of 20 mTorr for an operation time of 20 min×8 times with a purge time of 3 min while oxygen (O_2) was flowed at a rate of 120 sccm. Thereafter, aluminum etchant and chrome etchant may be used to remove the sacrificial aluminum thin film and the chrome hard mask, resulting in the final neural interface

[0060] The present disclosure uses sputtering and photolithography processes to directly deposit and pattern conductive materials. This eliminates the need for pre-metal layer processes (stamping), allowing the neural interface to be fabricated using a single wafer. Furthermore, the use of sputtering instead of the conventional E-beam process for metal deposition reduces the process cost and thus can be more suitable for mass production.

[0061] A better understanding of the present disclosure may be obtained through the following examples, which are set forth illustrate, but are not to be construed to limit, the present disclosure.

Examples

[0062] 1,3,5-Triallyl-1,3,5-triazine-2,4,6(1H,3H,5H)-trione (TATATO) (Sigma-Aldrich, Seoul, Korea), trimethylolpropanetris(3-mercaptopropionate) (TMTMP) (Sigma-Aldrich, Seoul, Korea), tricyclodecanedimethanoldiacrylate (TCMDA) (Sigma-Aldrich, Seoul, Korea), and 2,2-dimethoxy-2-phenyl-acetophenone (DMPA) (Sigma-Aldrich, Seoul, Korea) were used to synthesize the SMP. The synthesis process was conducted in a class 1000 cleanroom. The SMP was synthesized from a mixture of stoichiometric amounts of TATATO and TMTMP, 31 mol % TCMDA, and 0.1 wt % DMPA as a photoinitiator. The solution was mixed using a paste mixer (AR-100, THINKY, Laguna Hills, CA, USA) to obtain a homogeneous solution.

[0063] Using a spin coater (SPIN-1200T, MIDAS, Seongnam, Korea), the solution was first applied to an Al-coated Si wafer at 800 rpm for 25 seconds to achieve a thickness of 20 μm. The Al thin film was used as a sacrificial layer. The coating was then cured under 365 nm UV light for 1 hour and dried in a 120° C. vacuum oven for 24 hours.

[0064] Next, a photoresist (DNR-L300-40, Dongin-Semichem, Seoul, Korea) was formed and patterned using a chrome hard mask and a mask aligner. Chromium (Cr) and gold (Au) thin films, serving as the adhesion and conductive layers respectively, were deposited to thicknesses of 50 nm and 200 nm using sputtering equipment. The photoresist was then removed to pattern the adhesion and conductive layers.

[0065] A second coating and curing of the SMP, with a thickness of 20 μm, was performed in the same manner as the first. A 200 nm chrome hard mask was patterned on the SMP using the same method as in the foregoing adhesive layer and conductive layer. The SMP was etched into the desired shape and micropatterned using reactive ion etching (RIE) with oxygen plasma. The sacrificial aluminum thin film and the chrome hard mask were removed using the aluminum etchant HCl 2M solution and chromium etchant (Sigma-Aldrich, Seoul, Korea), respectively.

[0066] Additionally, to enhance the stability and recording performance of the neural interface, a version of the neural interface with IrO_2 electrodeposition on the conductive layer was also prepared.

Experimental Example 1: Characterization of Mechanical Properties

[0067] The mechanical properties of the SMP substrate were analyzed using dynamic mechanical analysis (DMA). A dynamic mechanical analyzer (DMA Q800, TA Instruments, New Castle, DE, USA) was used to measure the storage modulus (E') and the loss factor (tan δ). Samples were prepared by laser cutting a 20 μm thick SMP film into rectangular shapes of 40 mm×6 mm. Measurements were conducted at 0.2N preload, 0.275% strain, and 1 Hz, with a temperature change rate of 2° C. min^{-1} from −10° C. to 80° C.

[0068] FIG. **8**(*a*) shows the storage modulus of the SMP. At room temperature (22° C.), the storage modulus of the SMP was 1.4 GPa. This level of stiffness allowed for complex micropatterning through photolithography. The SMP began to soften rapidly from 30° C. due to the polymer's properties, with a Young's modulus of 400 MPa at body temperature (37° C.). FIG. **8**(*b*) indicates that the glass transition temperature was 44° C.

Experimental Example 2: Characterization of Electrochemical Properties

[0069] To analyze the performance of the neural interface, electrochemical impedance spectroscopy (EIS) tests were performed using a multichannel potentiostat (Ivium-n-Stat, IVIUM Technology). A three-electrode setup was used with an Ag/AgCl reference electrode and a platinum (Pt) counter electrode. Phosphate buffered saline (PBS) was used as the medium, with a scan rate of 50 mV/s and a frequency range of 1 Hz to 100 kHz.

[0070] The impedance and charge storage capacity (CSC) of the Au-deposited neural interface and the IrO_2-coated neural interface were compared. The impedance of the neural interface was measured over the frequency range of 1 Hz to 100 kHz. FIG. **9**(*a*) shows that the impedance at 1 kHz for the uncoated neural interface and the IrO2-coated neural interface were 30.74 kΩ and 2.114 kΩ, respectively.

[0071] The CSC was measured using cyclic voltammetry (CV) with an applied voltage range of −0.6 V to 0.8 V and a scan rate of 50 mV/s. FIG. **9**(*b*) shows that the CSC for the uncoated neural interface and the IrO_2-coated neural interface were 0.19 mC/cm^2 and 14.59 mC/cm^2, respectively.

[0072] In summary, the IrO_2 coating reduced impedance by a factor of 14.54 and increased CSC by a factor of 76.77.

Experimental Example 3: Stability Confirmation

[0073] To confirm the stable electrodeposition of IrO2 coating, a stability test was conducted. A continuous voltage was applied to the neural interface for 2 hours in PBS. Using the same CV measurement method as in Experimental Example 2 with the potentiostat, a biphasic triangular pulse with a maximum amplitude of 0.8V and a minimum amplitude of −0.6V was applied once per second. Impedance and CSC were measured at 30-minute intervals to monitor the electrode condition, as shown in FIG. **10**(*a*). After 2 hours, the impedance of the neural interface decreased by 9.64%, and the CSC increased by 8.45%.

[0074] As shown in FIG. **10**(*b*), the state of the coated electrode surface was indirectly confirmed by fitting the CV curves over time. There were no significant changes observed in the CV curves or their magnitudes, indicating that the performance of the neural interface did not degrade over prolonged voltage application.

[0075] Another stability test was performed to determine the effect of the bending process during the implantation of the neural interface. Impedance and CSC were measured in three states: the initial state (Initial), the bent state (Bending) after being deformed into a hook shape through the bending process, and the recovered state (Recover) after restoring the shape using the shape memory effect. As shown in FIG. **10**(*c*), bending stress, which is generated in a bent state, caused an 8.84% increase in impedance and a 6.47% decrease in CSC. After recovery at 38° C., impedance increased by 0.39% and CSC increased by 0.65% compared to the initial state. The bending stress impacted the performance of the neural interface during the bending process, but the performance change after recovery was less than 1%, indicating that there was no significant impact on stimulation and recording performance.

Experimental Example 4: Functional Effect after Implantation

[0076] As shown in FIGS. **11**(*b*) and (*c*), the fabricated neural interface was implanted in the common peroneal nerve (CPN) and the pelvic nerve (PN) and analyzed for functional effect. A reshape procedure was conducted to facilitate implantation. As shown in FIG. **11**(*a*), the neural interface was heated on a 50° C. hot plate to minimize damage. The neural interface was then deformed into a hook shape and fixed at 0° C. The hook-shaped neural interface was fixed to the nerve, and 38° C. phosphate buffered saline (PBS) was sprayed on the neural interface. Due to the shape memory effect, the neural interface self-clipped and fixed itself to the nerve.

Experimental Example 5: Stimulation and Recording Test

[0077] Stimulation and recording were performed at the acute level in Sprague Dawley (SD) rats. Stimulation tests were conducted using the neural interface to confirm neural stimulation. An RHD 2216 system (Intan Technologies, LA, USA) was used to acquire electromyography (EMG) signals at a sampling rate of 30 kHz. A 60 Hz notch filter and band-pass filters with cutoff frequencies of 0.1 Hz and 2.5 kHz were applied for signal recording. An RHD 2132 system (Intan Technologies, Los Angeles, CA, USA) was used to collect compound nerve action potentials (CNAPs) at a sampling rate of 30 kHz. The same notch and band-pass filters as those used for the RHD 2216 were applied. The acquired signals were processed using MATLAB 2020a software. EMG signals induced from the tibialis anterior (TA) muscle and CNAPs from the common peroneal nerve (CPN) were recorded and averaged 60 times every second to reduce noise.

[0078] Turning to FIG. **12**(*a*), the nerve was stimulated through the neural interface implanted in the CPN, and muscle signals were recorded using stainless steel wires implanted in the tibialis anterior (TA) muscle. A biphasic waveform of 100 μs pulses was applied at 1 Hz for 1 minute, with current amplitudes varying from 50 μA to 100 μA to 150 μA. Muscle twitches were observed after stimulation. FIG. **12**(*b*) shows the EMG signals processed using the aforementioned signal processing method.

[0079] As shown in FIG. **12**(*c*), the peak-to-peak amplitudes of the acquired EMG signals were 1120.4 μA at 50 μA, 1513.8 μA at 100 μA, and 2221.7 μA at 150 μA, confirming that the magnitude of the EMG signals increased with the stimulation intensity.

[0080] To verify the recording performance of the neural interface, a recording test was conducted. Compound nerve action potentials (CNAPs) were recorded through the neural interface in the CPN by stimulating the sciatic nerve (SN) with a hook electrode. Electrical stimulation was applied through the hook electrode, with stimulation parameters identical to those used in the stimulation test. Leg tremors were observed due to the stimulation.

[0081] Electroneurography (ENG) signals were acquired and processed using the previously mentioned signal processing method. FIG. **12**(*d*) shows the processed ENG signals.

[0082] As shown in FIG. **12**(*e*), the peak-to-peak amplitudes of the acquired ENG signals were 1308.2 μA at 50 μA, 1498.1 μA at 100 μA, and 1544.9 μA at 150 μA. These results indicate that the stimulation parameters exceeded the threshold energy, and the amplitude of the evoked CNAPs saturated as the stimulation amplitude increased.

[0083] Overall, the results demonstrate that the neural interface made of SMP shows excellent implantation performance due to the shape memory effect and is suitable for use in neural recording and stimulation.

[0084] The features, structures, effects and the like described in the above embodiments are included in at least one embodiment of the present invention, and are not necessarily limited to only one embodiment. In addition, the features, structures, effects and the like described in each embodiment may be combined or modified with respect to other embodiments by those skilled in the art. Accordingly, contents related to these combinations and modifications should be construed as being included in the scope of the present invention.

[0085] Although the embodiments of the present invention have been described above in detail with reference to the accompanying drawings, it will be apparent to those skilled in the art that various substitutions, modifications, and

alterations may be devised within the spirit and scope of the present invention. For example, respective constituent elements, which are concretely described in the embodiments, may be altered in various ways. Differences related to these modifications and applications should be construed as included within the scope of the present disclosure as defined by the appended claims.

INDUSTRIAL APPLICABILITY

[0086] The present disclosure is characterized by a dual clip design implemented utilizing shape memory polymers for a bio-implantable neural interface for recording and stimulating neural signals of peripheral nerves. Particularly, using a sputtering method for metal coating on the shape memory polymer coating layer can reduce the process cost and is suitable for mass production, so that the present disclosure is highly industrially applicable.

1. A neural interface, comprising:
an electrode section for neural stimulation and neural signal recording;
a first region defined by a first hole; and
a second region defined by a second hole disposed within the first region,
wherein the electrode section comprises a first electrode section and a second electrode section, either the first electrode section or the second electrode section being disposed within the second region.

2. The neural interface of claim **1**, wherein,
the first electrode section is disposed at an edge of the neural interface, and
the second electrode section is disposed within the second region.

3. The neural interface of claim **1**, wherein the first electrode section and the second electrode section are in contact with the upper and lower parts of the nerve, respectively.

4. The neural interface of claim **1**, wherein the electrode section comprises:
a substrate;
a shape memory polymer (SMP) layer disposed on the substrate;
an adhesion layer disposed on the SMP layer; and
a conductive layer disposed on the adhesion layer.

5. The neural interface of claim **1**, further comprising wiring electrically connected to the electrode section, wherein the wiring comprises:
a substrate;
a first SMP layer disposed on the substrate;
an adhesion layer disposed on the first SMP layer;
a conductive layer disposed on the adhesion layer; and
a second SMP layer disposed on the conductive layer.

6. The neural interface of claim **4**, wherein the shape memory polymer is synthesized by polymerizing 1,3,5-triallyl-1,3,5-triazine-2,4,6(1H,3H,5H)-trione (TATATO), trimethylolpropanetris(3-mercaptopropionate) (TMTMP), and tricyclodecanedimethanoldiacrylate (TCMDA).

7. A method for fabricating a neural interface, the method comprising the steps of:
synthesizing a shape memory polymer;
first coating a substrate with the shape memory polymer;
forming a photoresist on the shape memory polymer;
masking the photoresist;
sputtering an electrode material;
patterning the electrode material through a photolithography process;
second coating the shape memory polymer; and
etching the shape memory polymer.

8. The method of claim **7**, wherein the step of synthesizing a shape memory polymer is carried out by polymerizing 1,3,5-triallyl-1,3,5-triazine-2,4,6(1H,3H,5H)-trione (TATATO), trimethylolpropanetris(3-mercaptopropionate) (TMTMP), and tricyclodecanedimethanoldiacrylate (TCMDA).

9. The method of claim **7**, wherein in the first coating step, the shape memory polymer is spin-coated.

10. The method of claim **7**, wherein in the masking step, the photoresist is patterned using a chrome hard mask and a mask aligner.

11. The method of claim **7**, wherein in the sputtering step, the adhesion material and the conductive material are formed by sputtering.

12. The method of claim **1**, wherein the etching step comprises reactive ion etching using oxygen plasma.

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