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(54) **SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD OF THE SAME**

(71) Applicant: **Kioxia Corporation**, Tokyo (JP)

(72) Inventor: **Shoji AOTA**, Yokkaichi Mie (JP)

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Publication Classification

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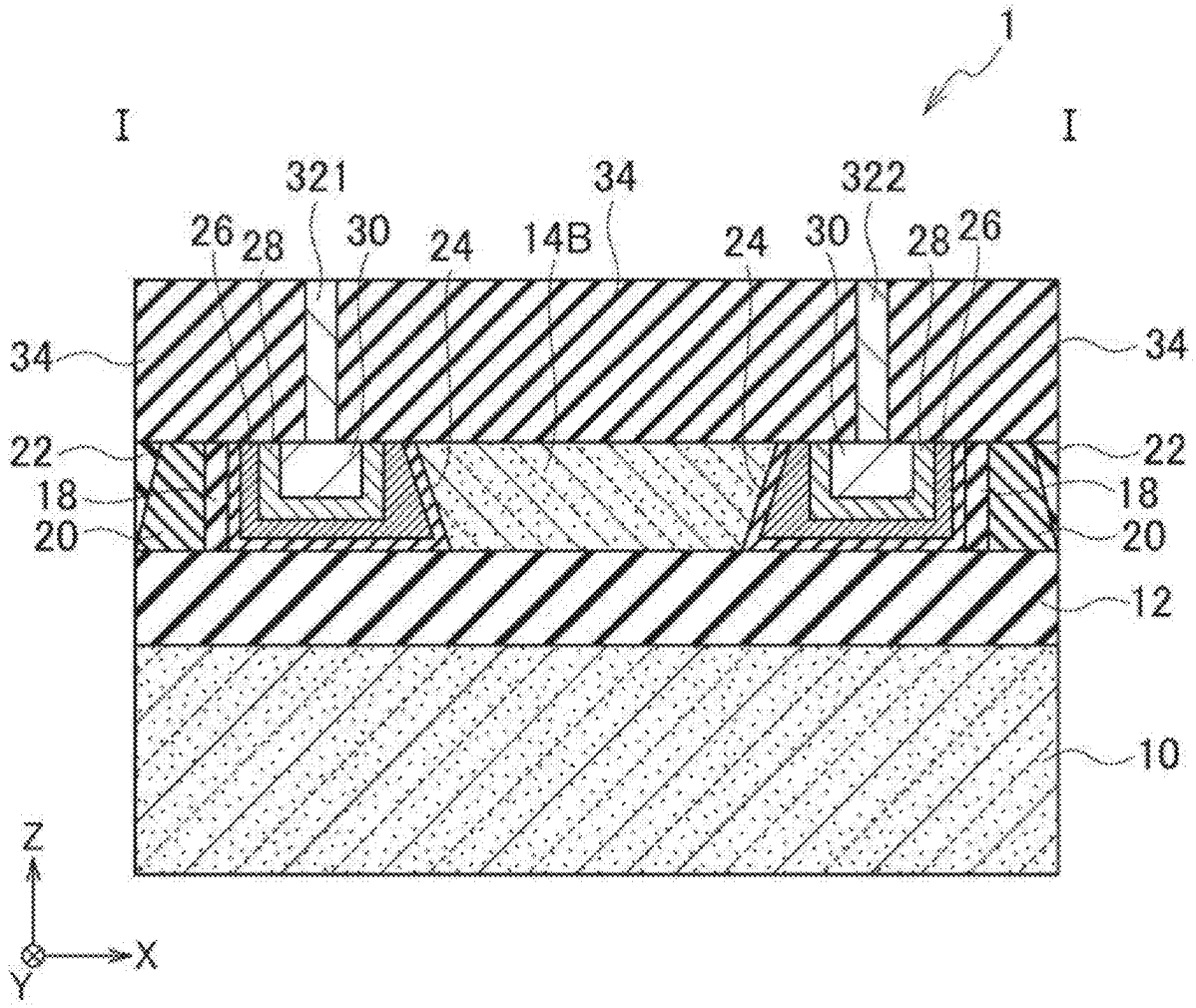
H10D 64/68 (2025.01)

(52) **U.S. Cl.**

CPC ***H10B 20/25*** (2023.02); ***H10D 62/834*** (2025.01); ***H10D 64/666*** (2025.01); ***H10D 64/667*** (2025.01); ***H10D 64/691*** (2025.01)

(57) **ABSTRACT**

A semiconductor device includes a semiconductor substrate including an active region and an isolation region that is electrically isolated from the active region, a fuse disposed on the isolation region and including a polysilicon layer including an impurity, and first and second electrode layers that are electrically connected to the polysilicon layer, and a transistor disposed on the active region and including a metal gate having a stack structure of electrode layers.



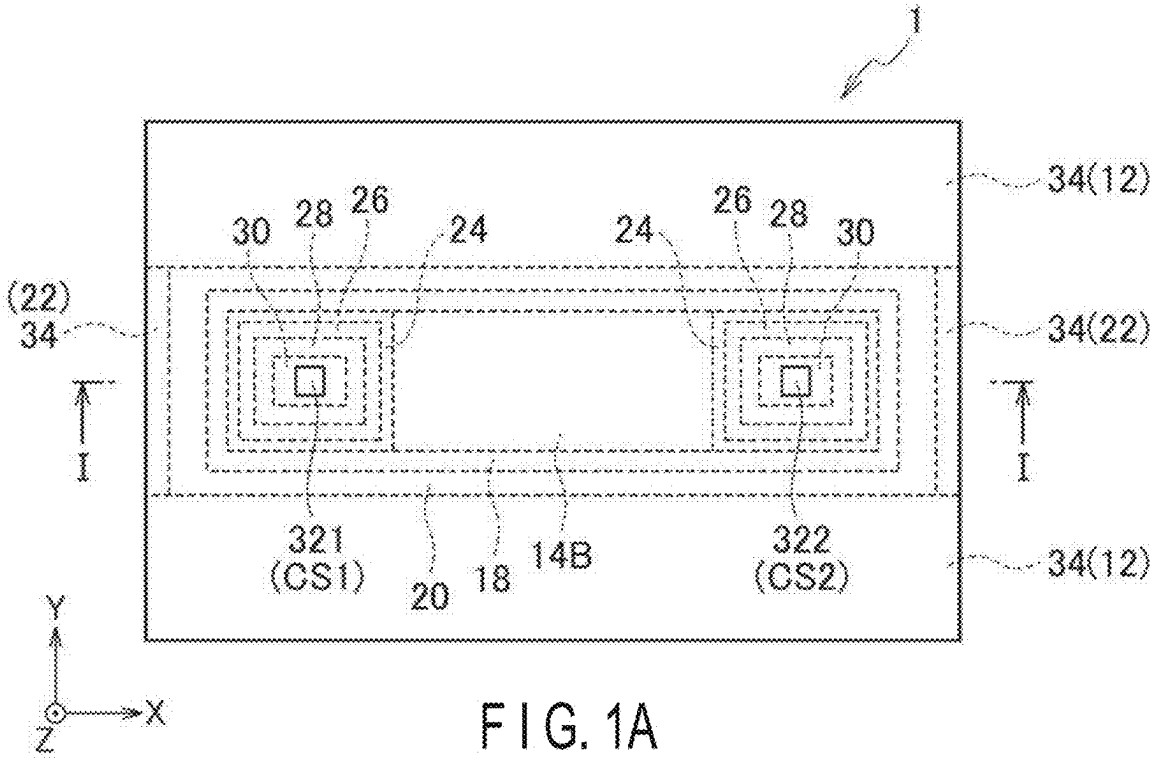

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FIG. 1A

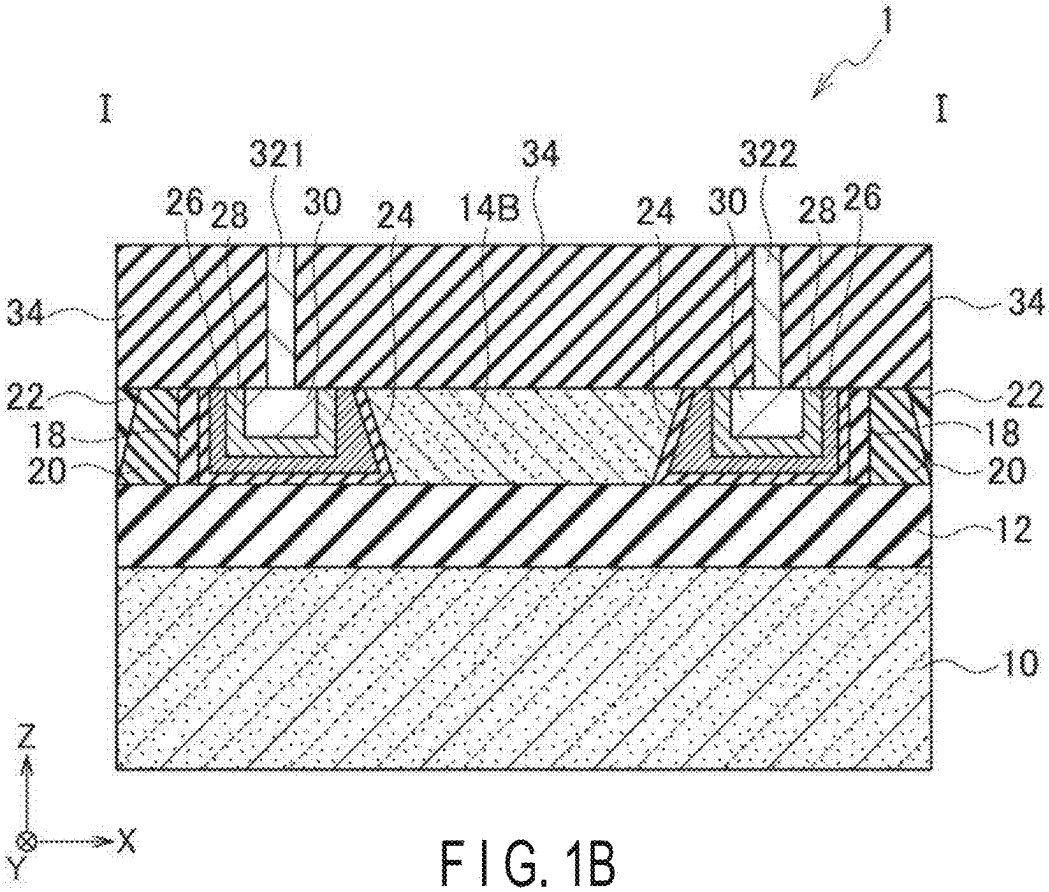
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FIG. 1B

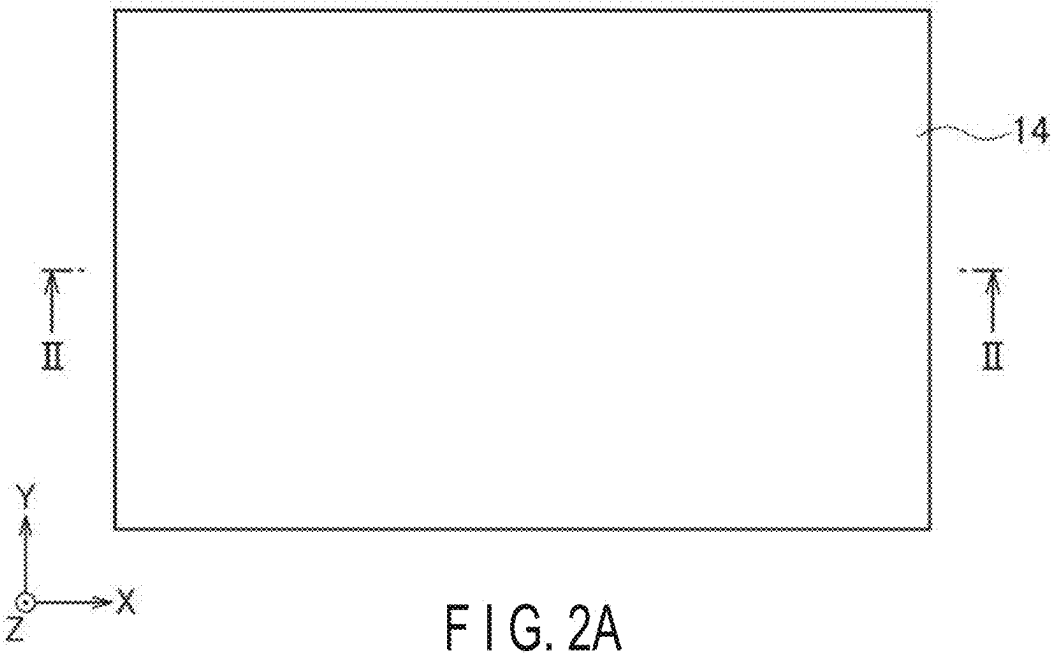

FIG. 2A

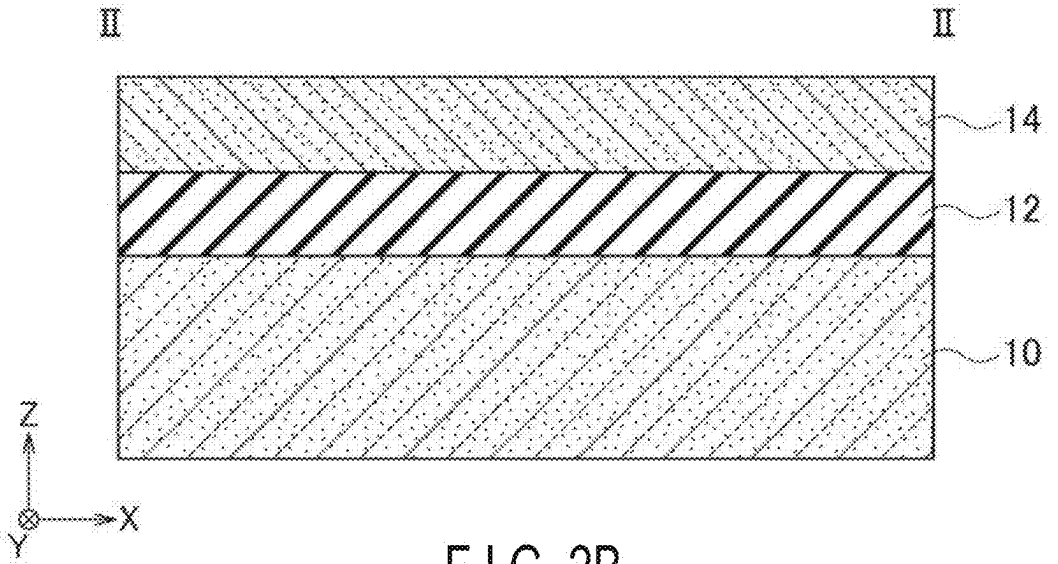

FIG. 2B

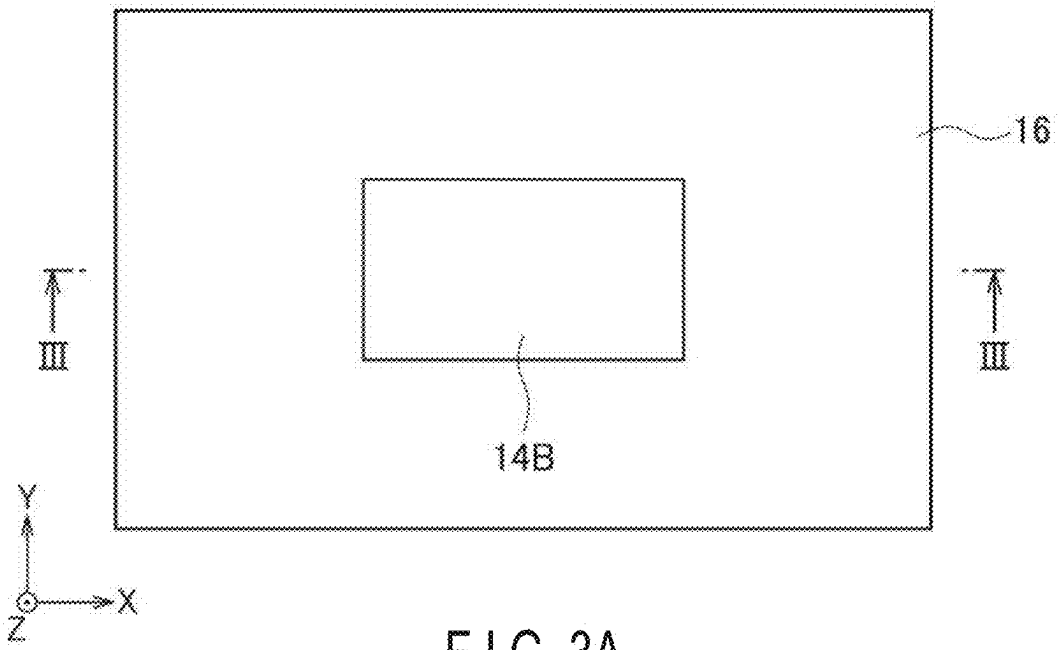

FIG. 3A

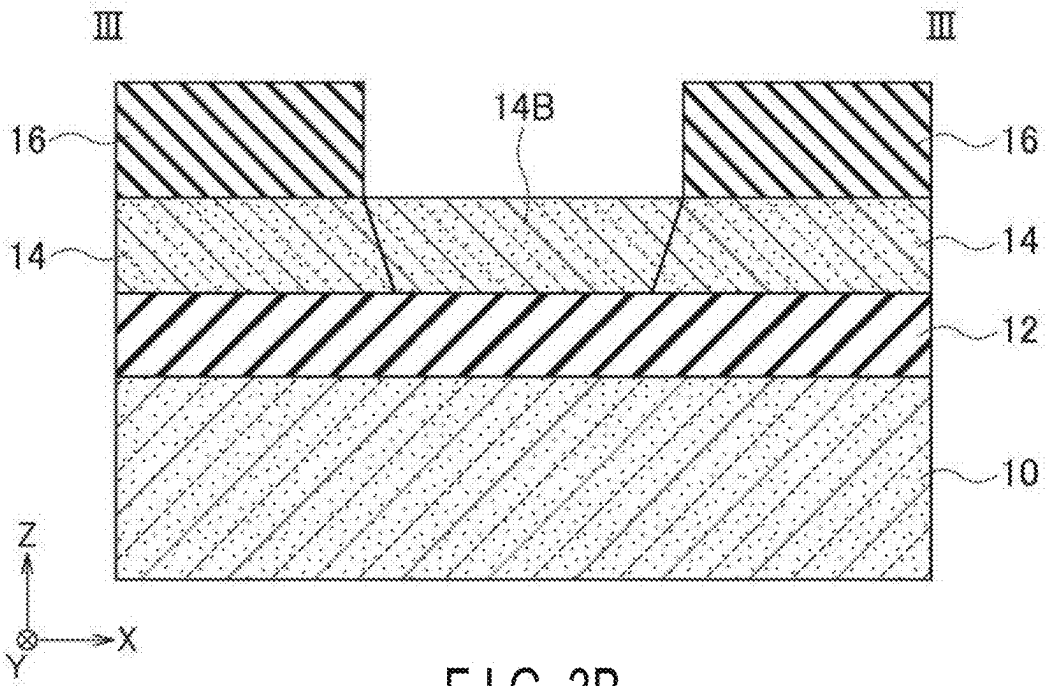

FIG. 3B

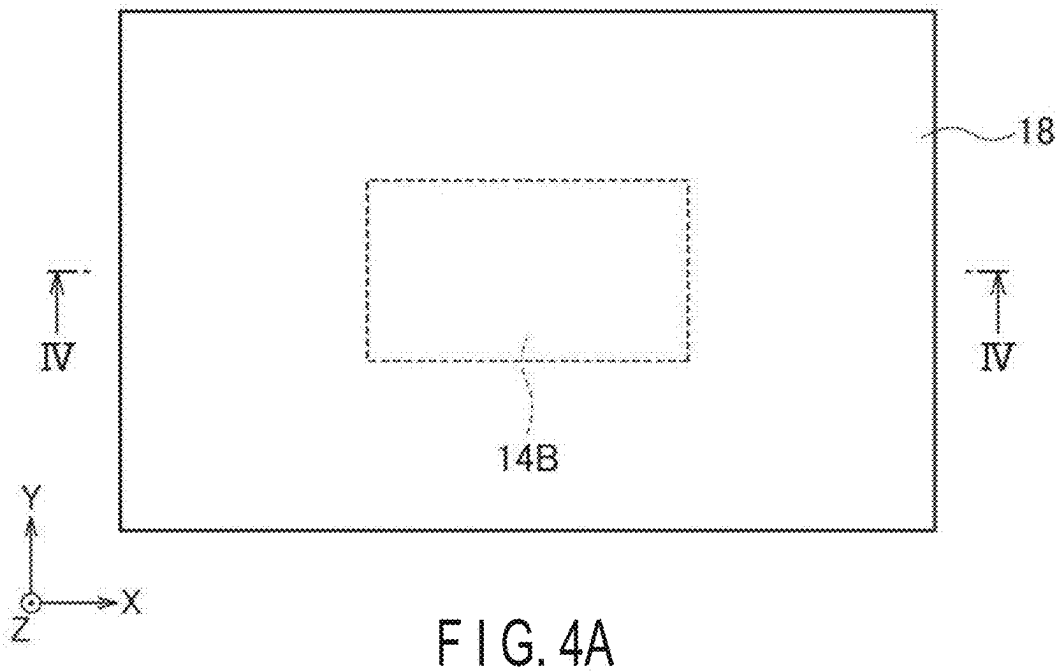

FIG. 4A

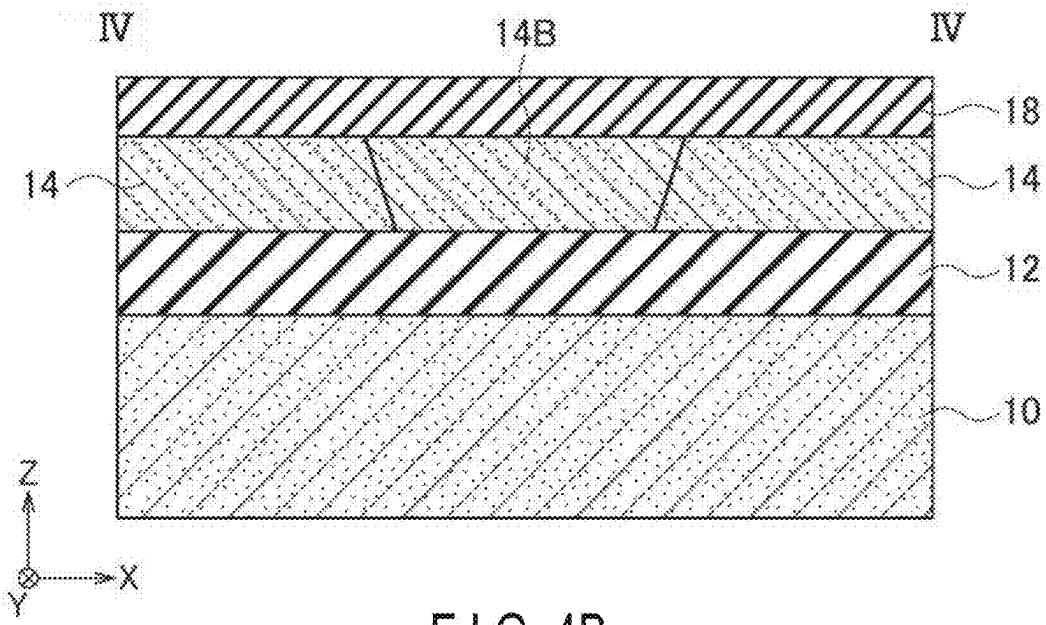

FIG. 4B

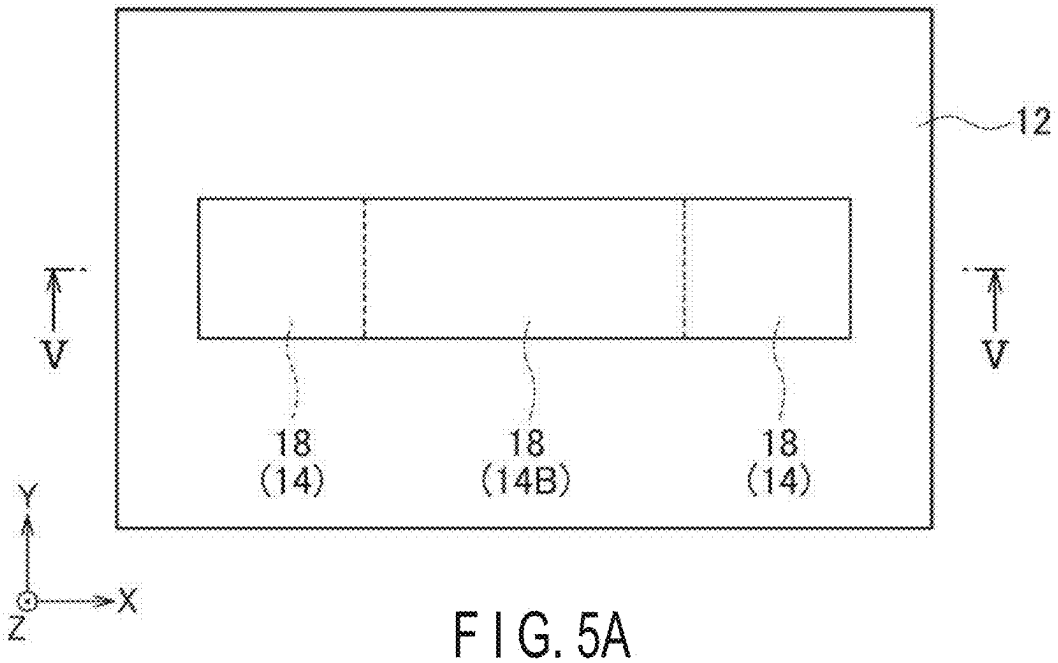

FIG. 5A

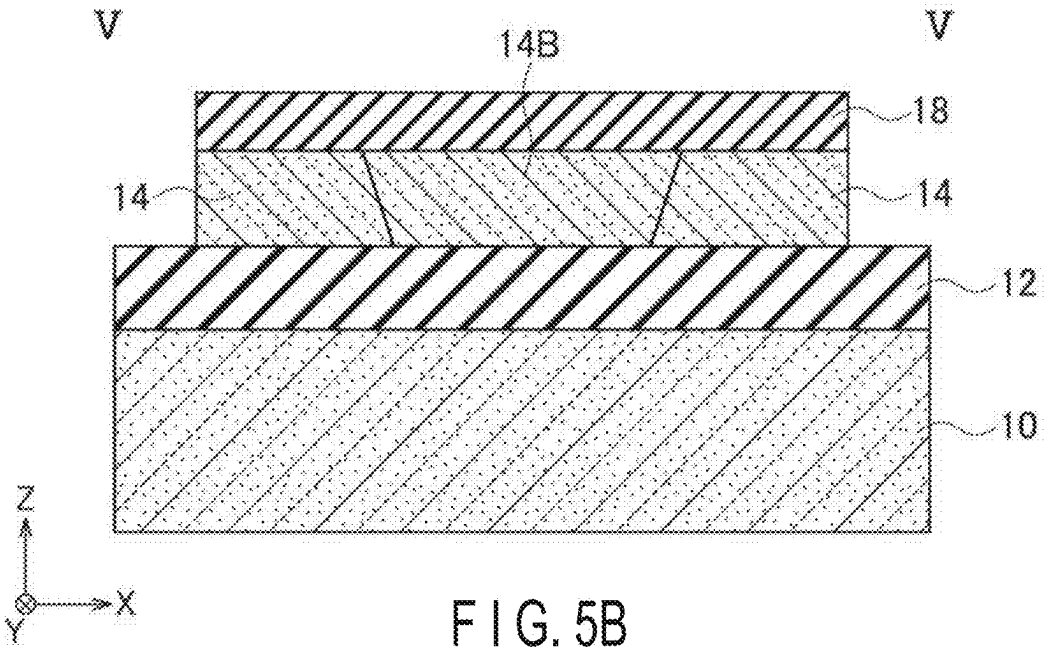

FIG. 5B

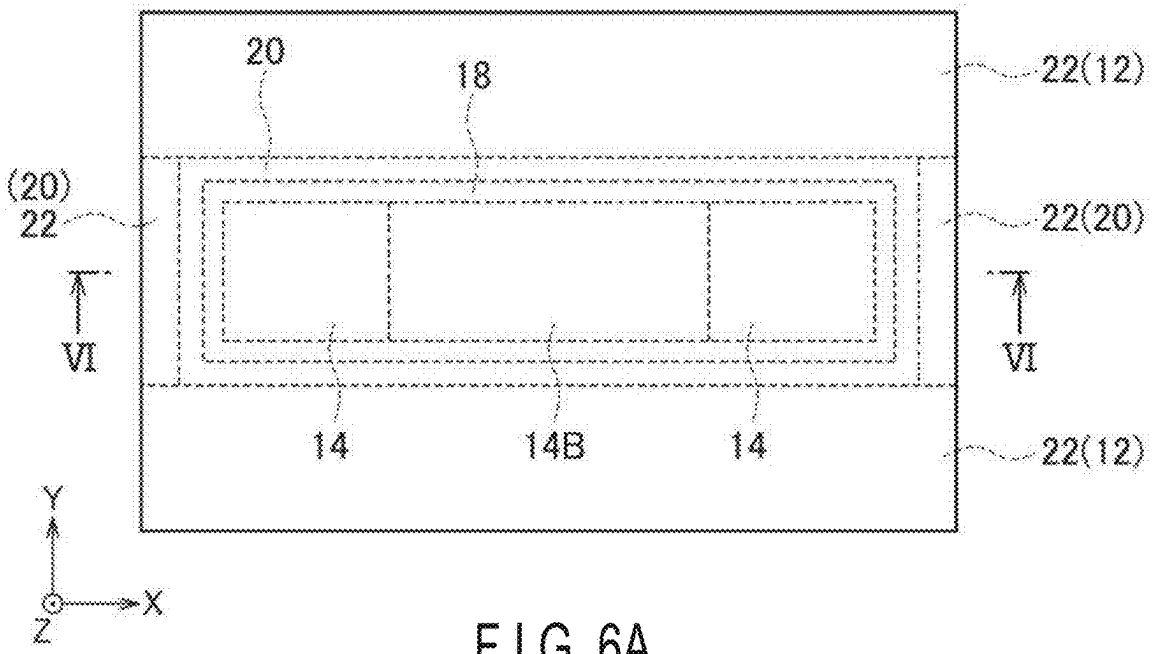
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FIG. 6A

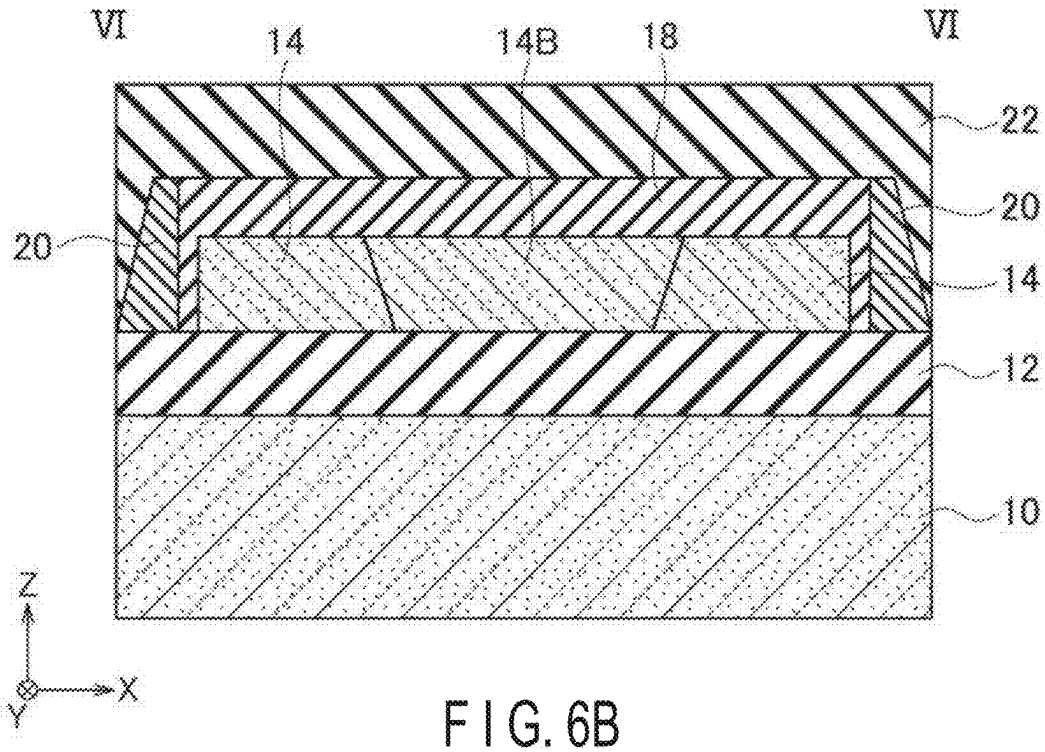
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FIG. 6B

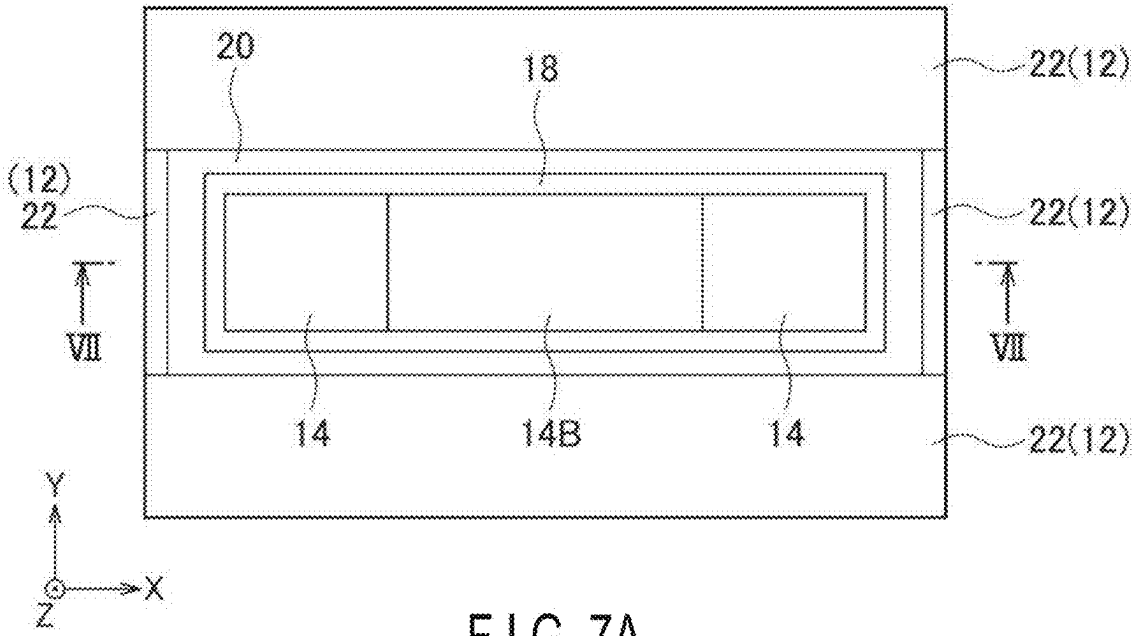
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FIG. 7A

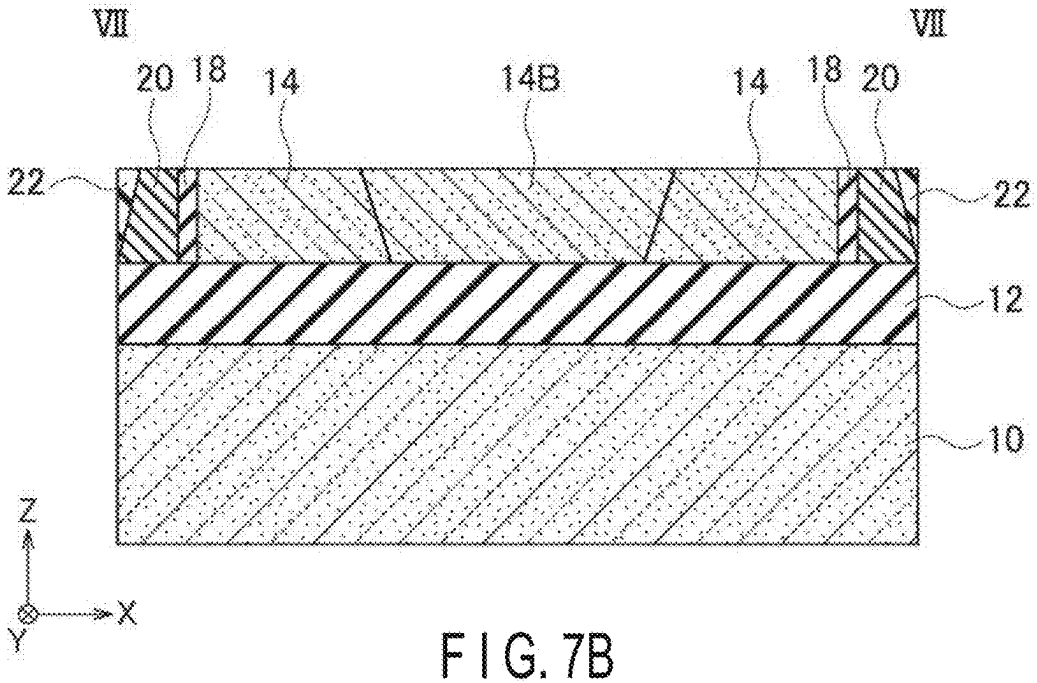
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FIG. 7B

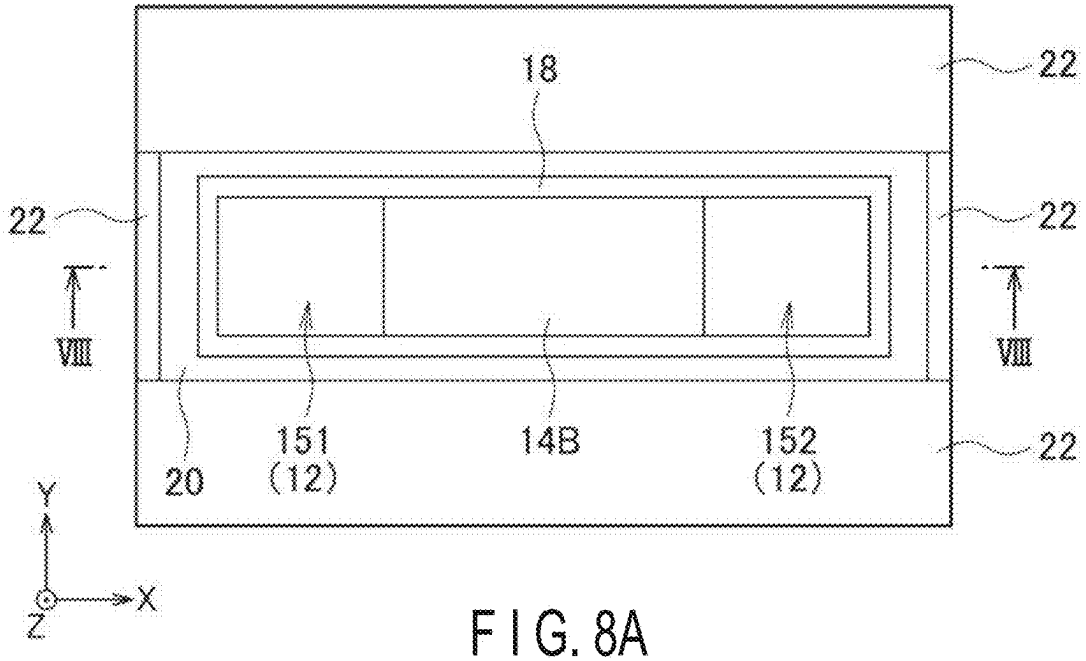
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FIG. 8A

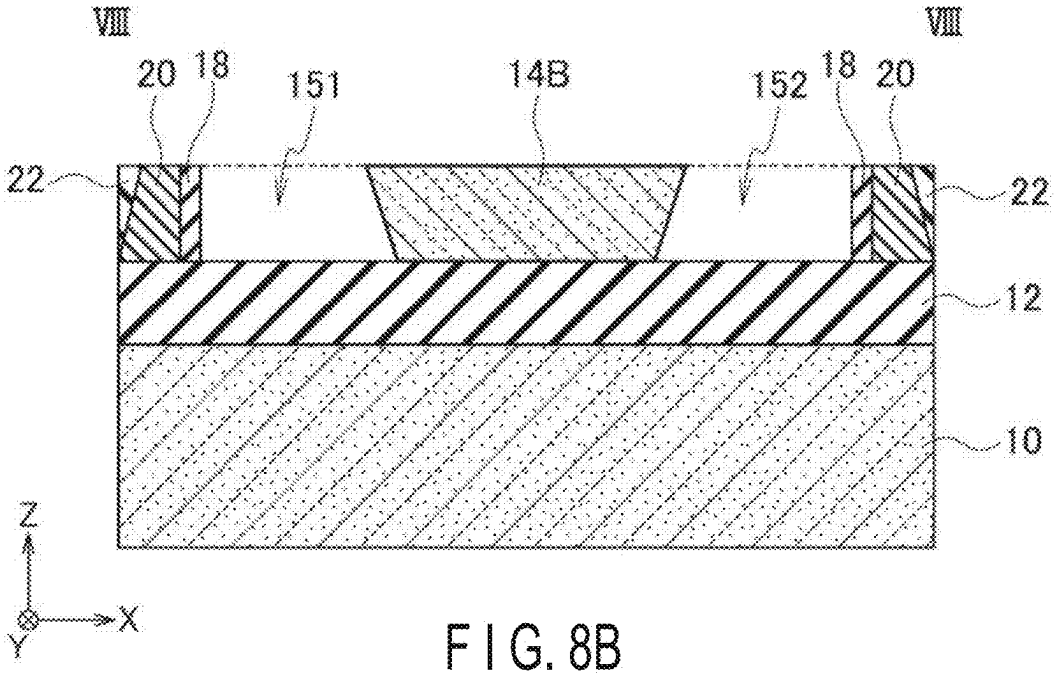
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FIG. 8B

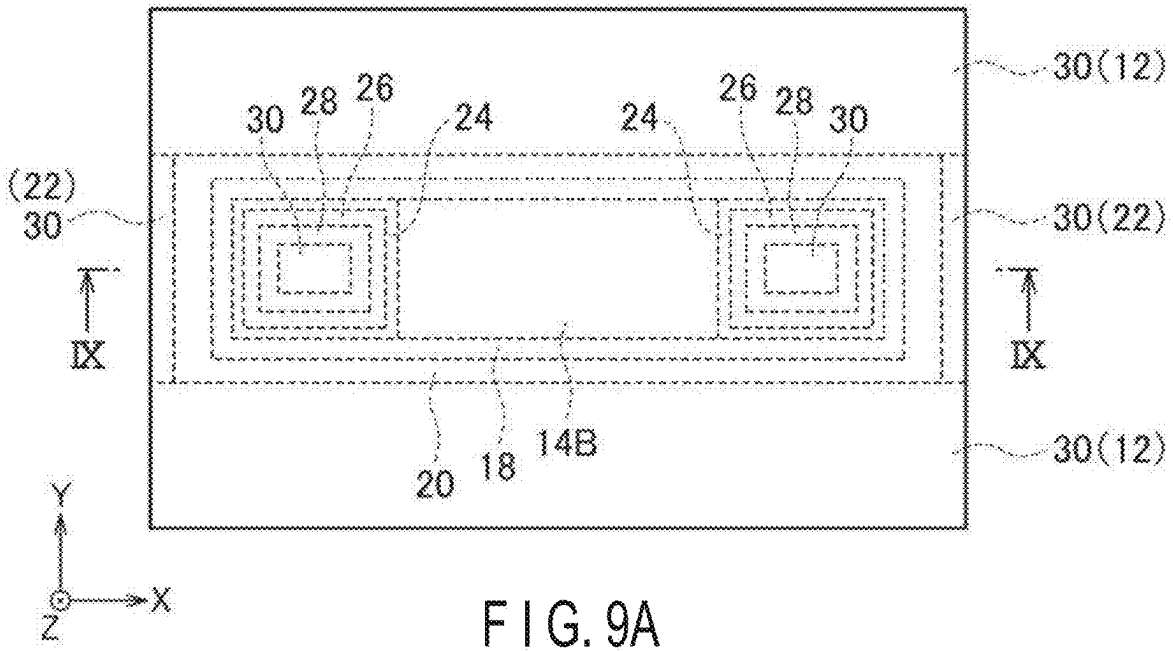
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FIG. 9A

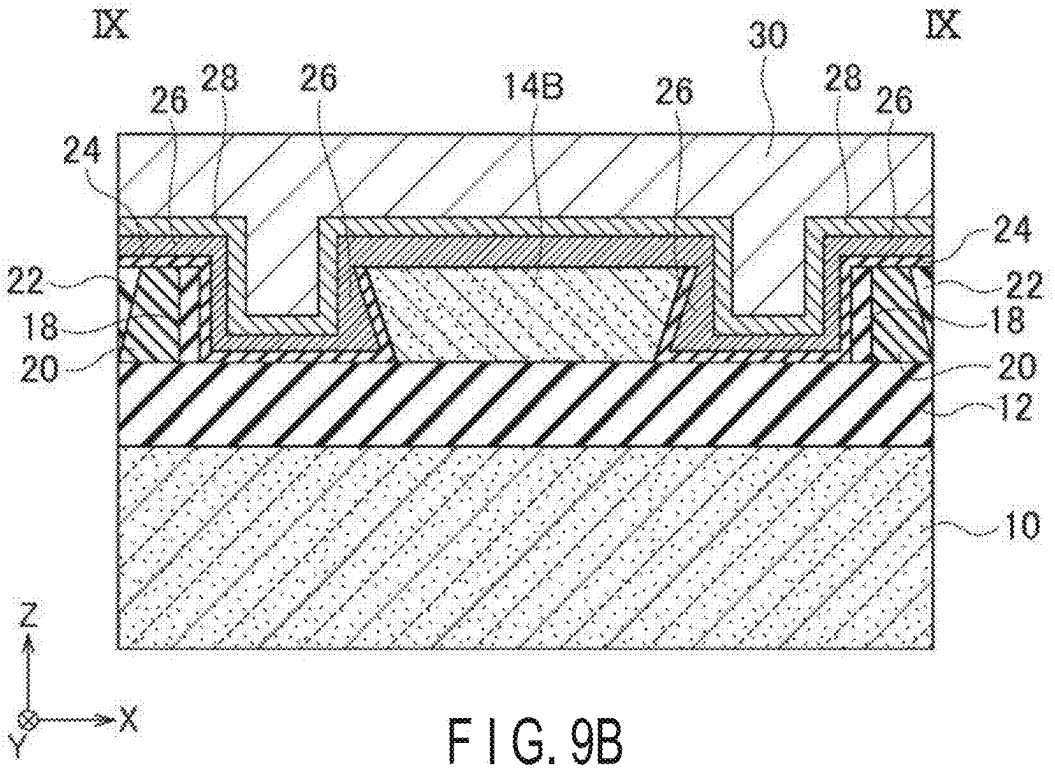
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FIG. 9B

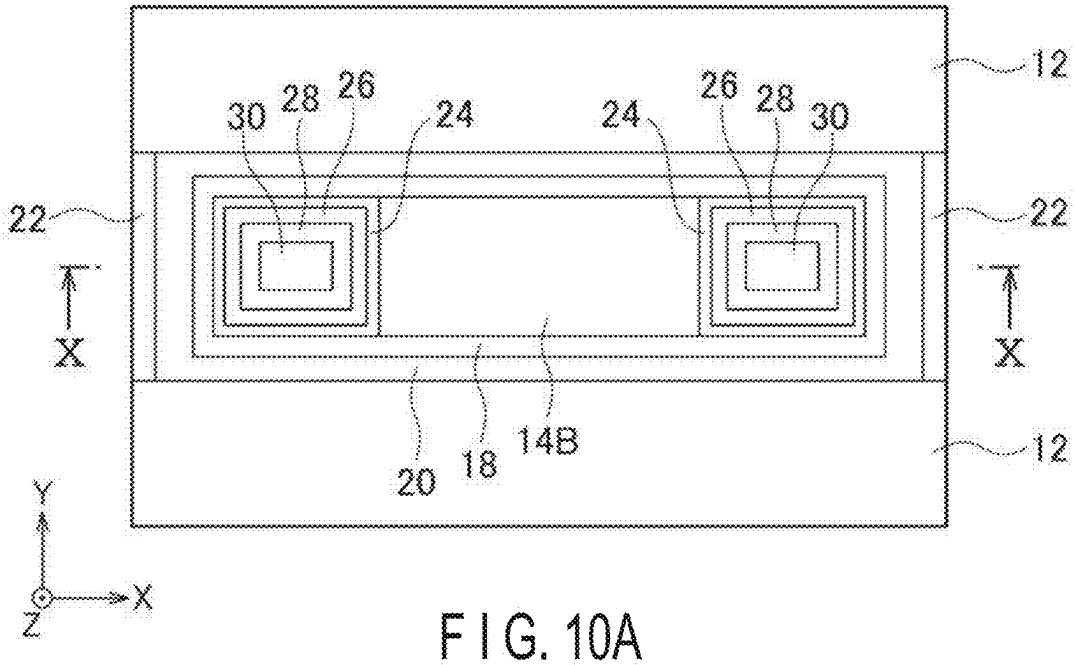

FIG. 10A

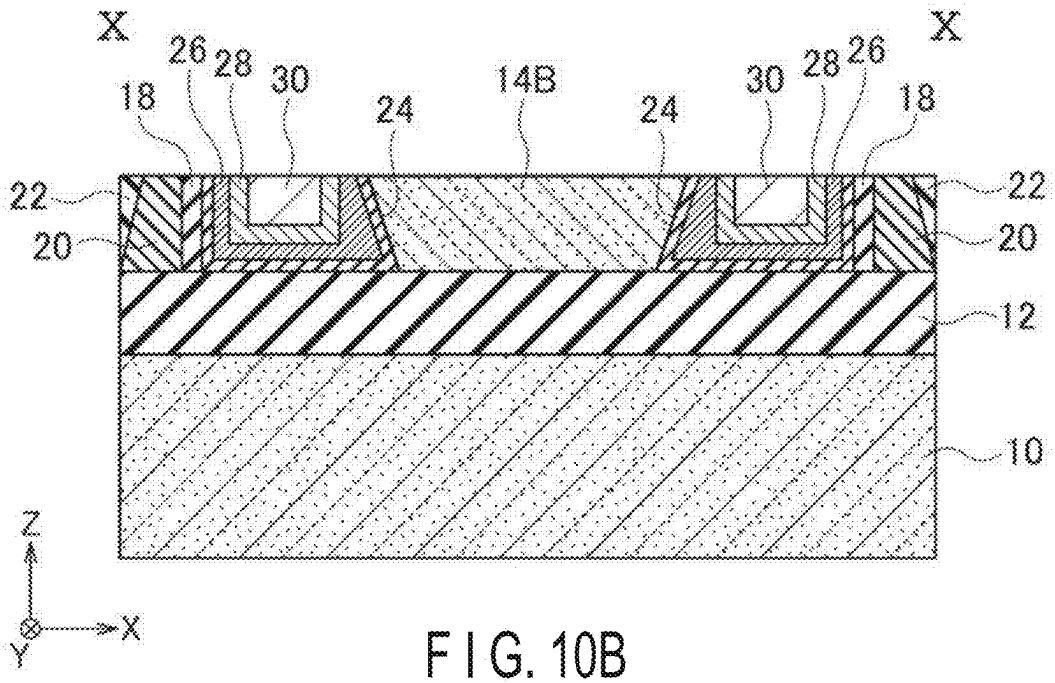

FIG. 10B

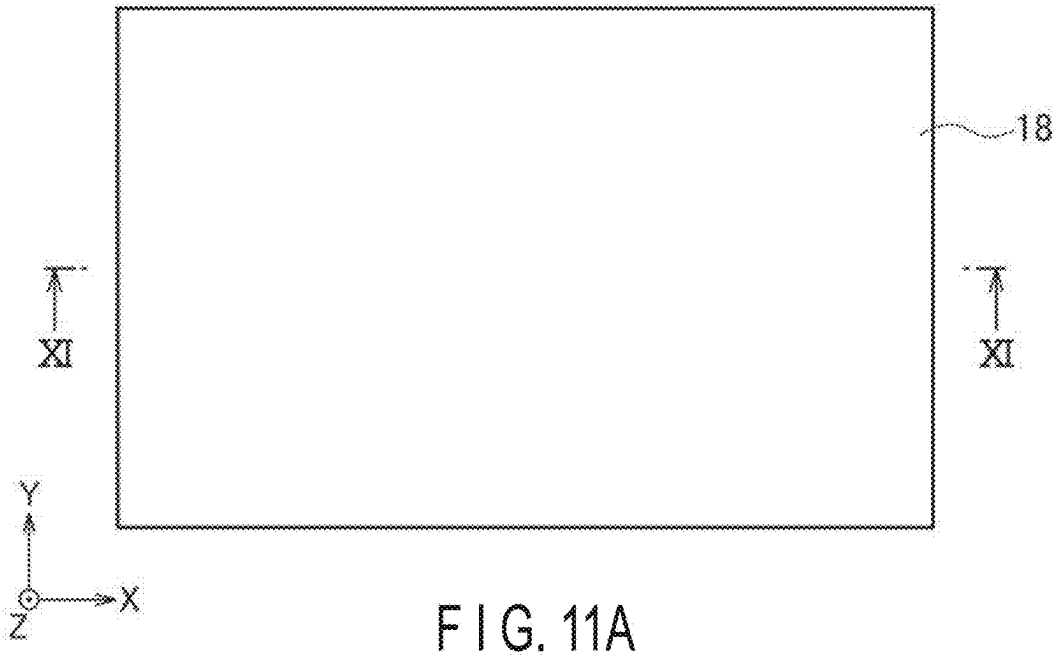

FIG. 11A

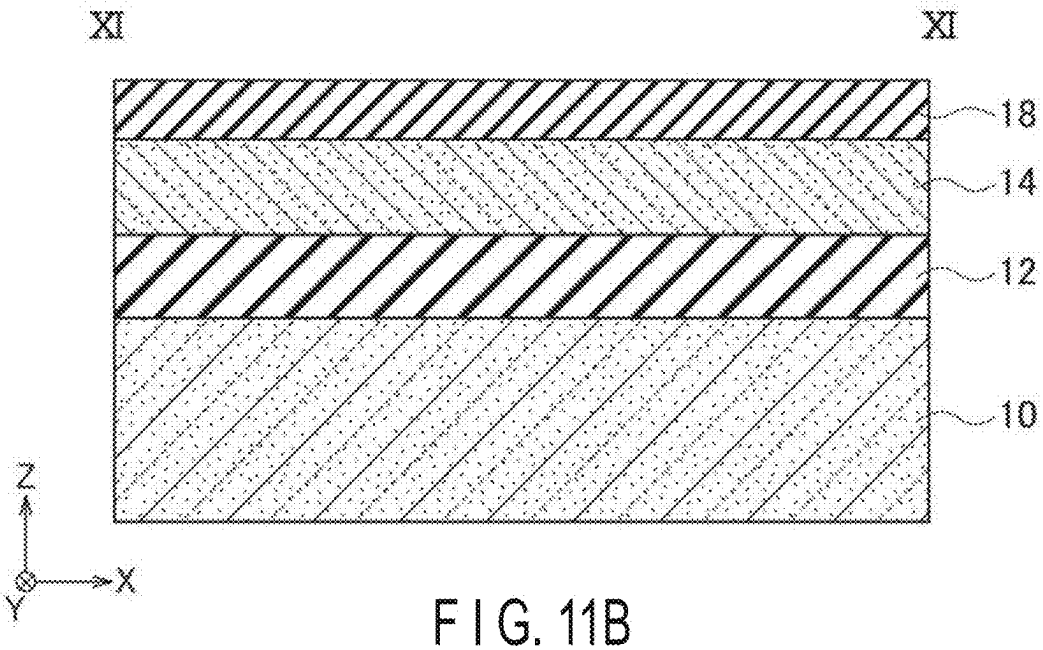

FIG. 11B

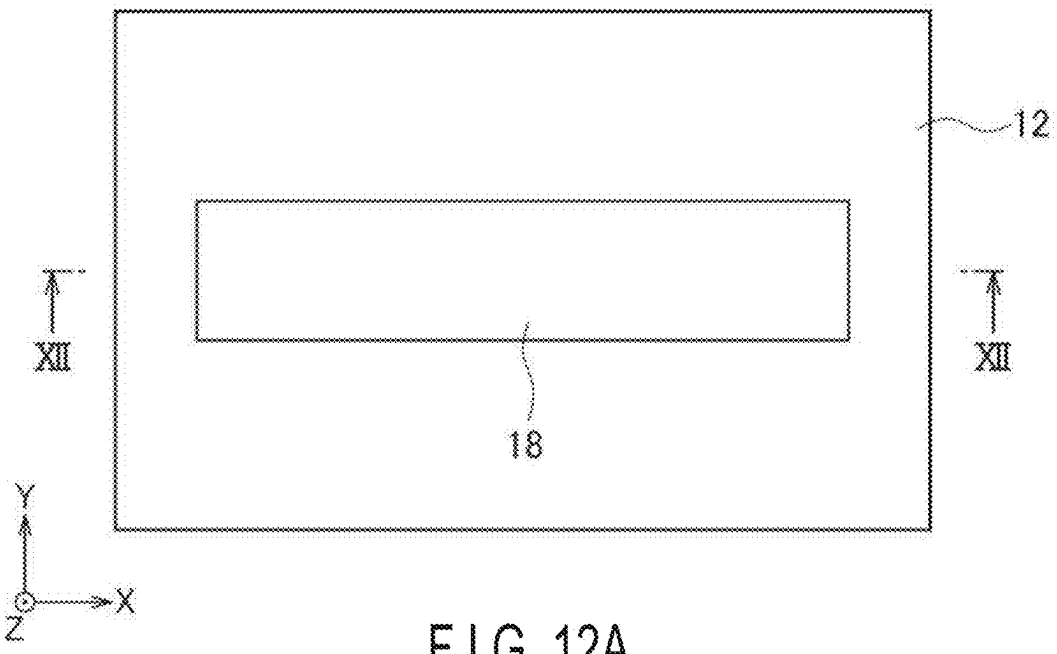

FIG. 12A

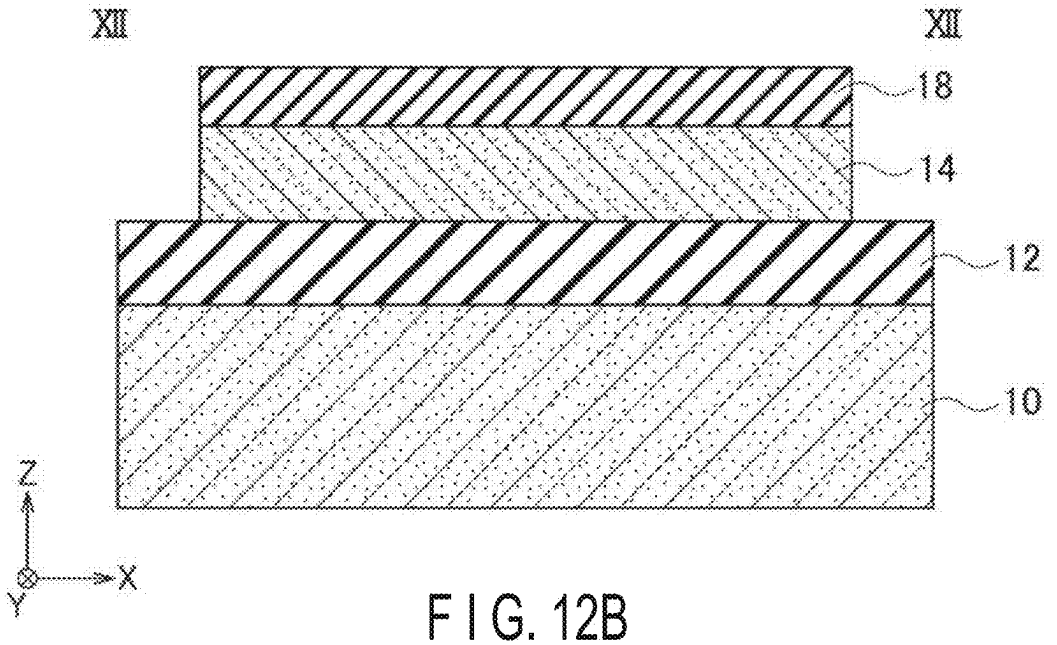

FIG. 12B

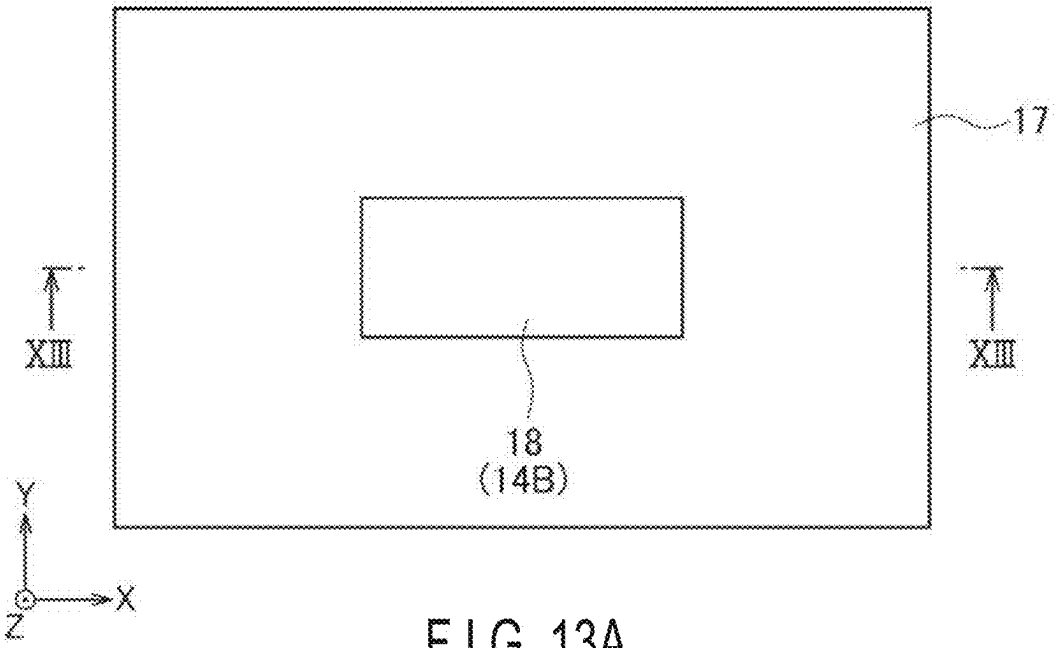

FIG. 13A

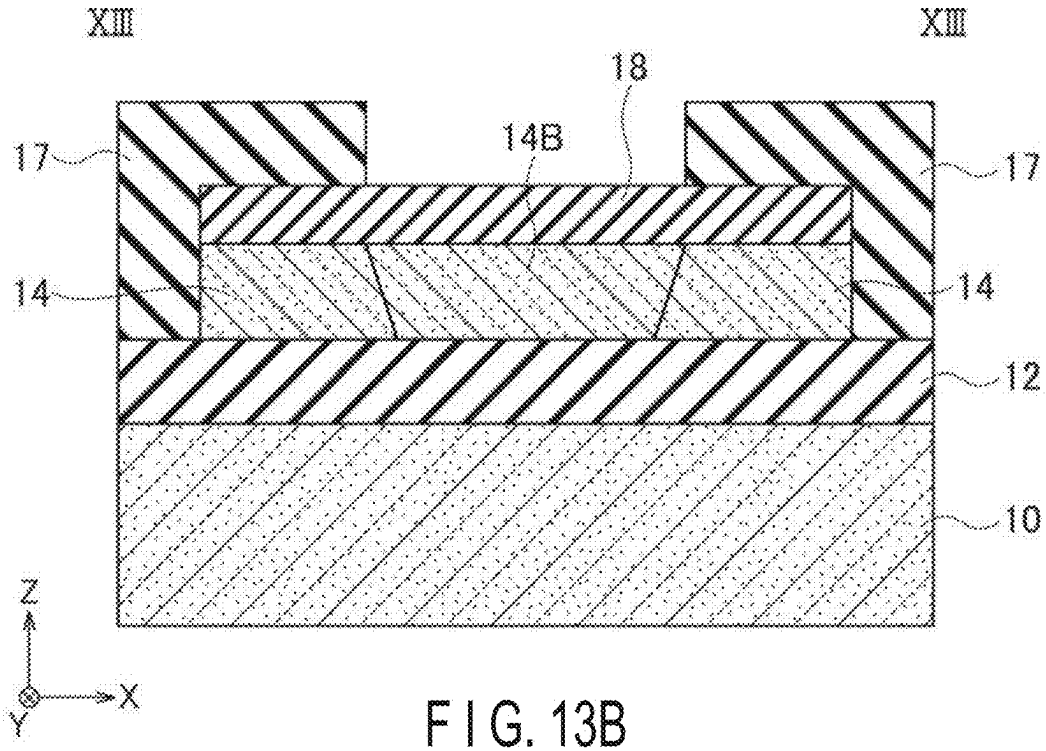

FIG. 13B

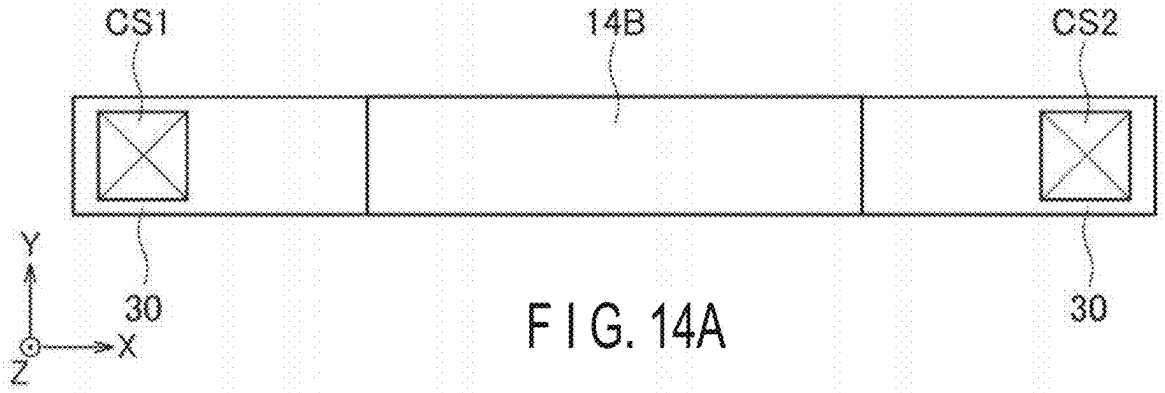

FIG. 14A

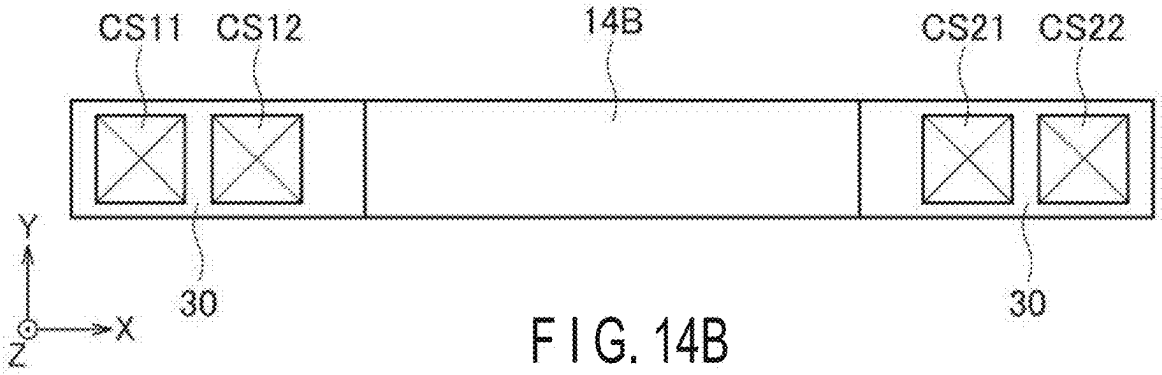

FIG. 14B

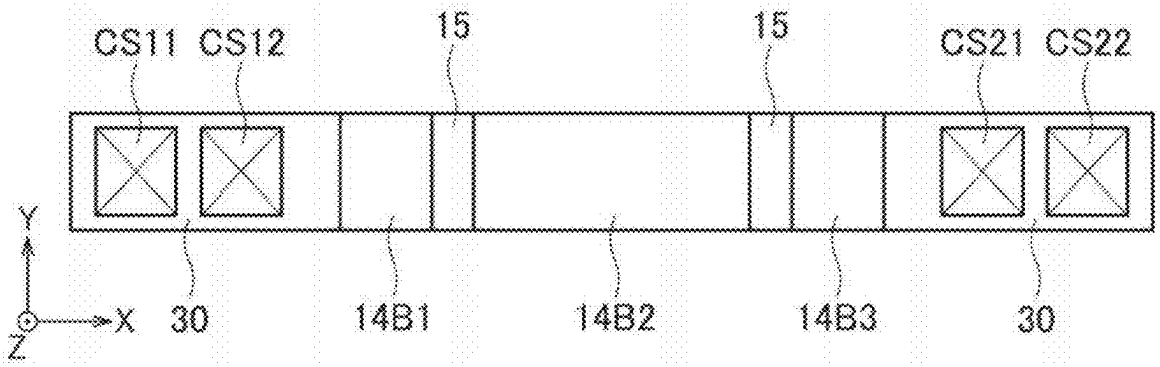

FIG. 14C

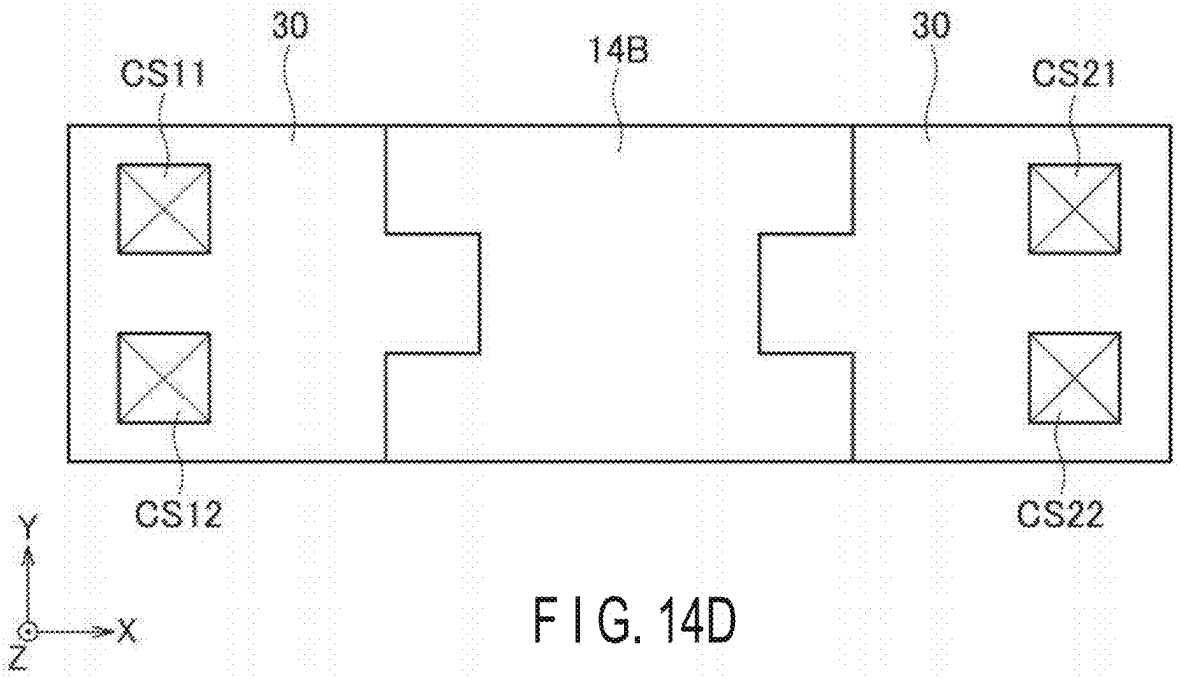

FIG. 14D

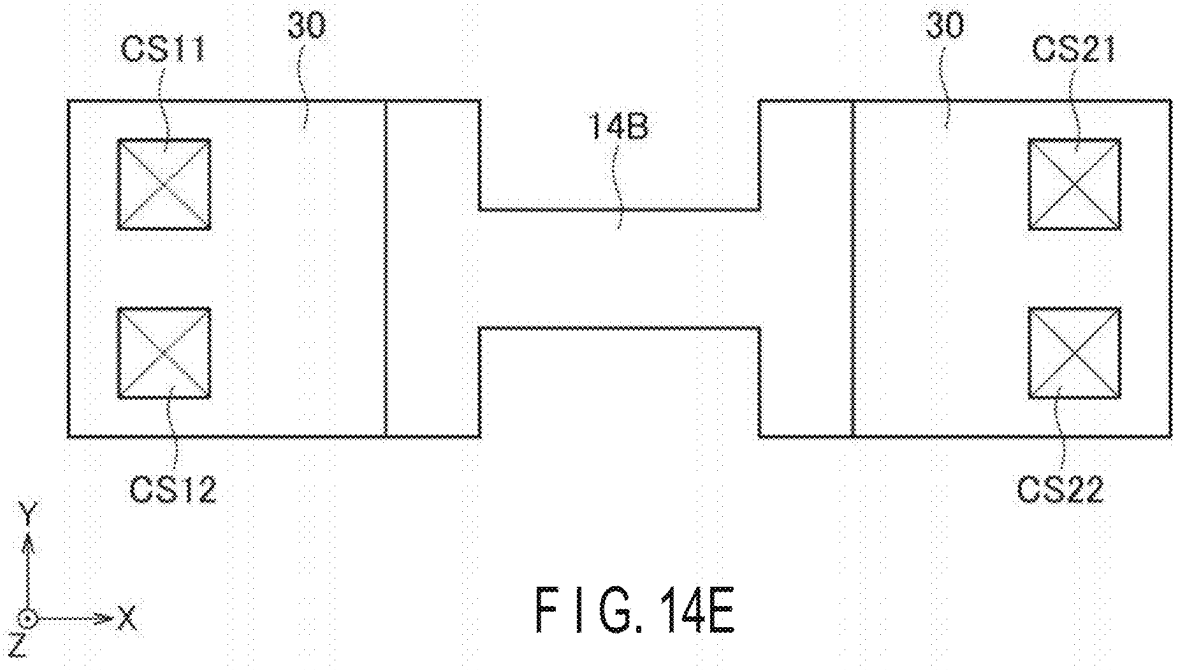

FIG. 14E

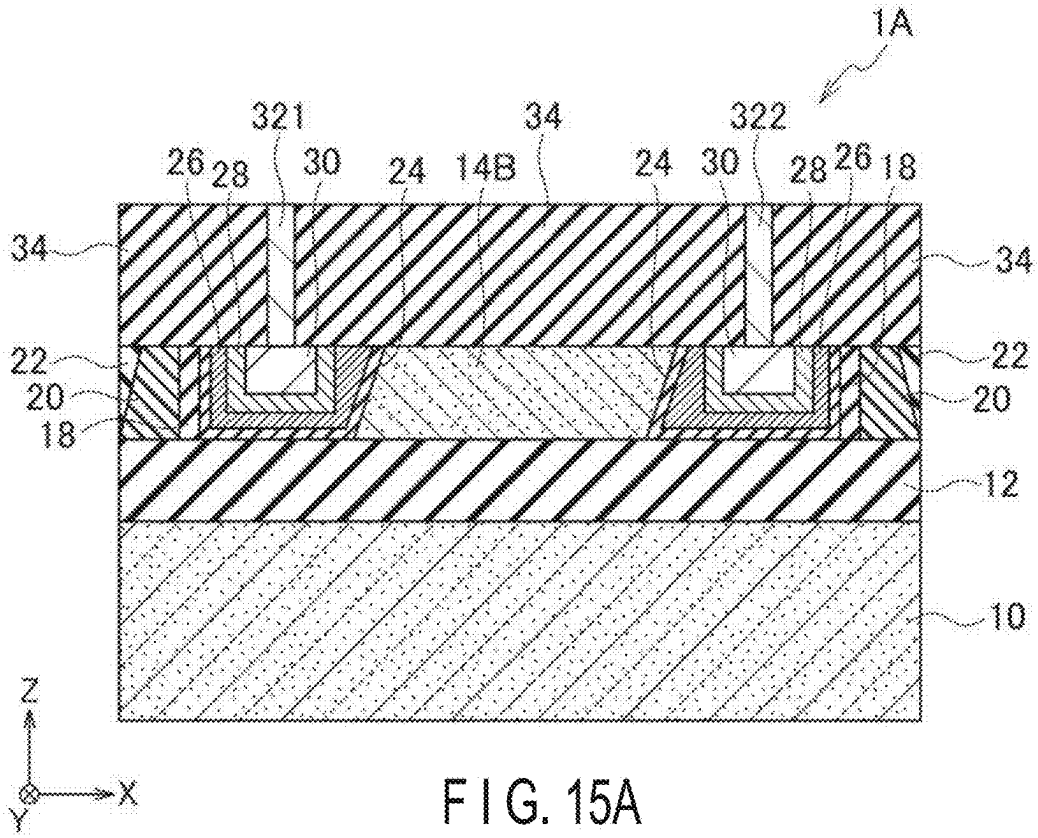

FIG. 15A

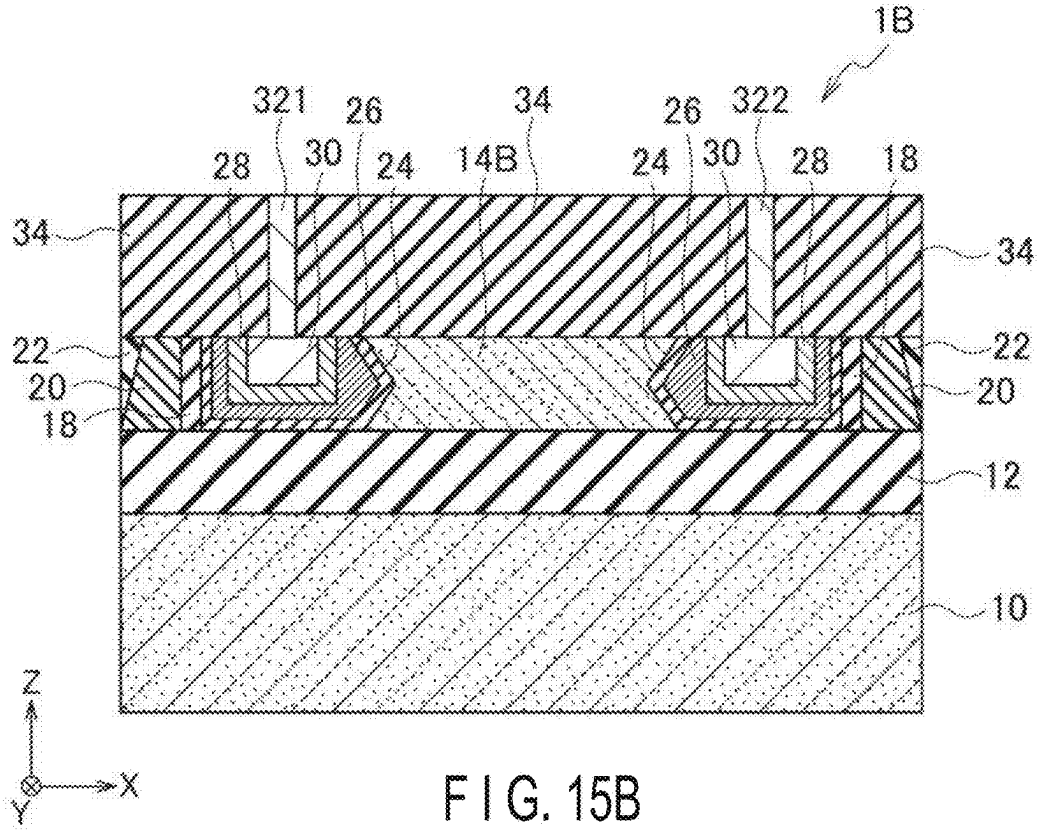

FIG. 15B

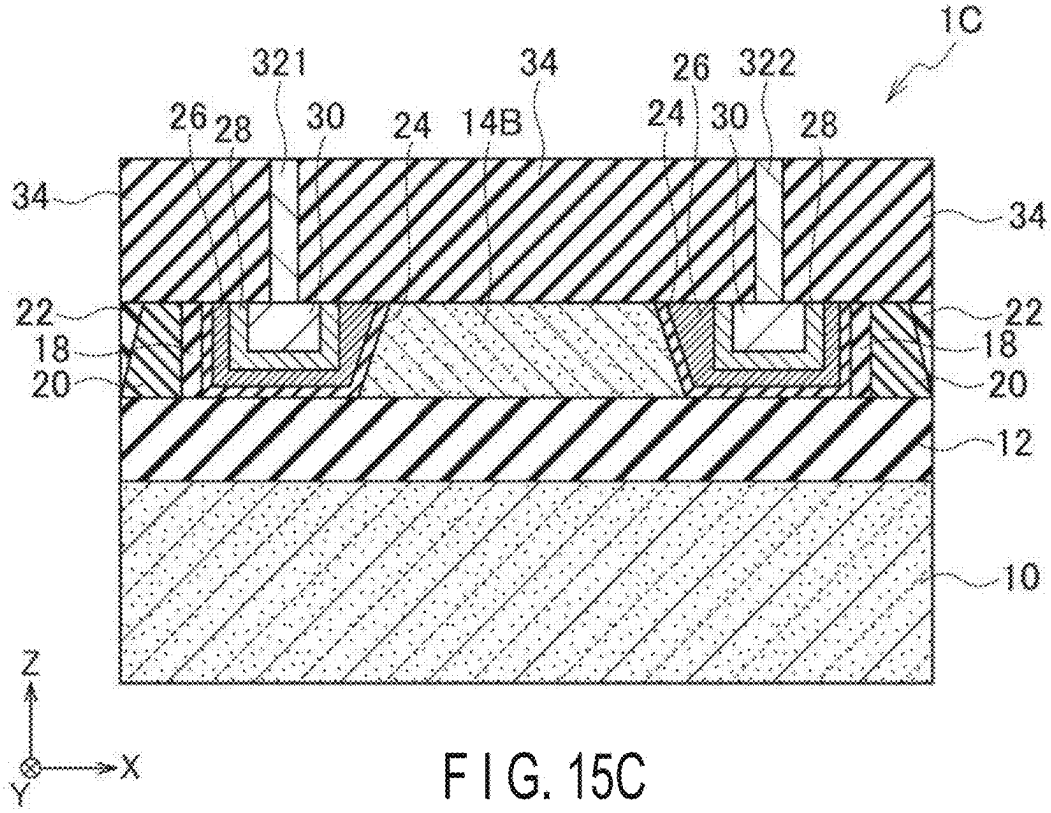

FIG. 15C

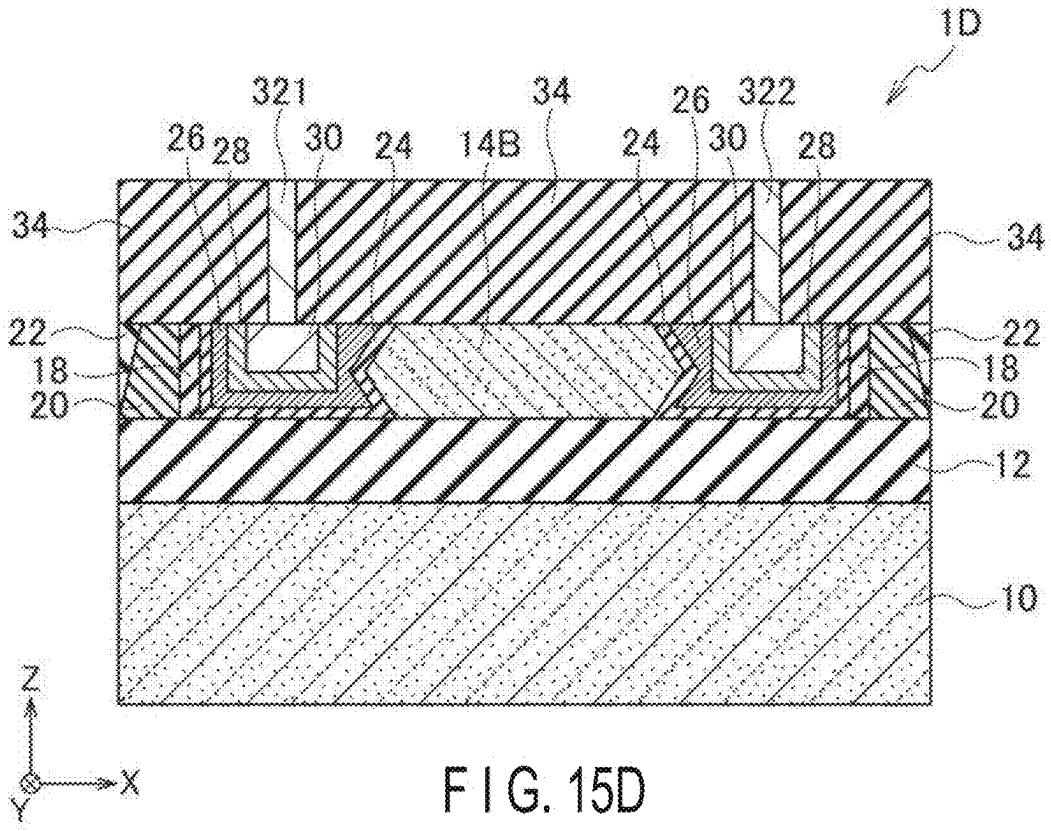

FIG. 15D

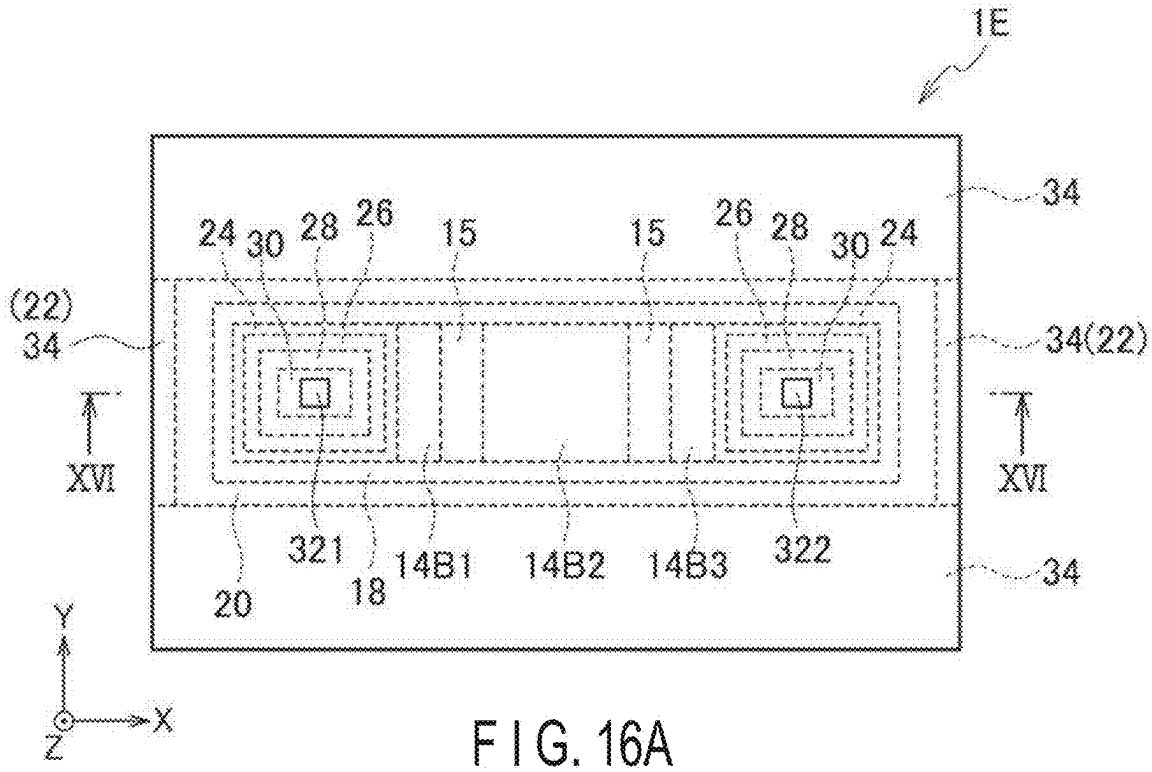

FIG. 16A

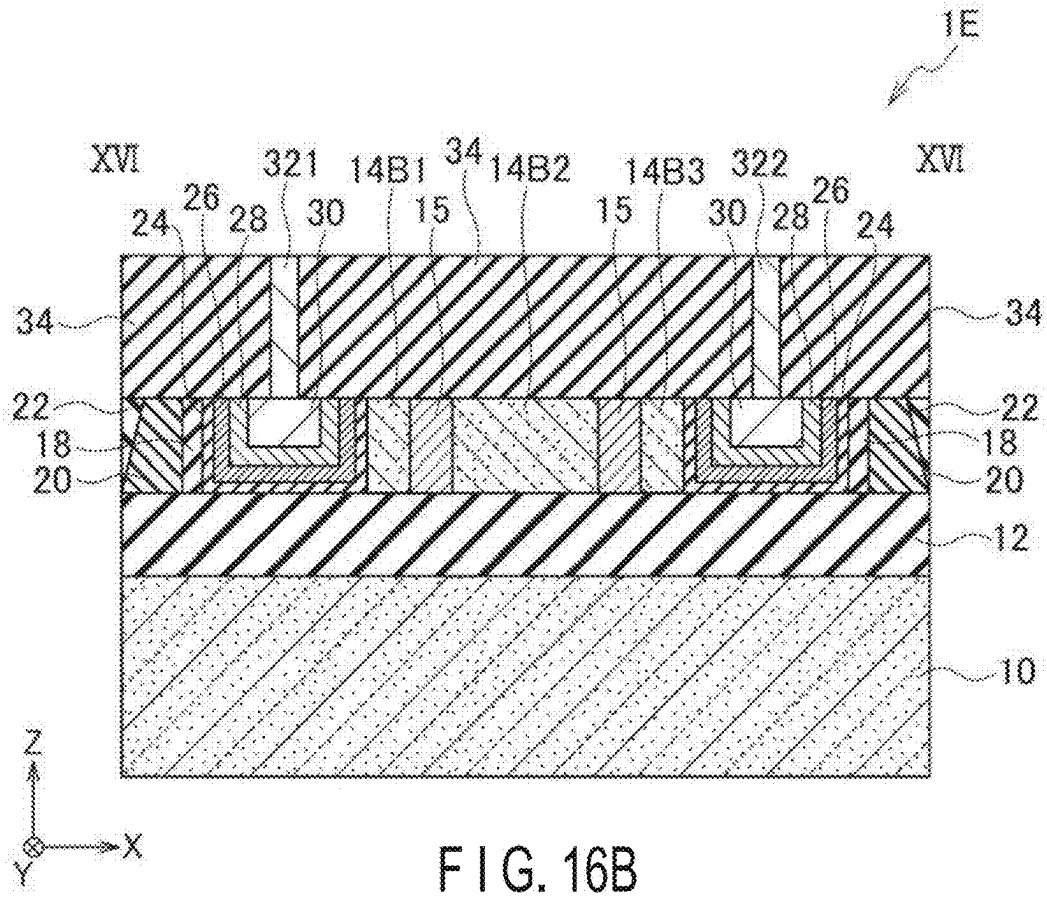

FIG. 16B

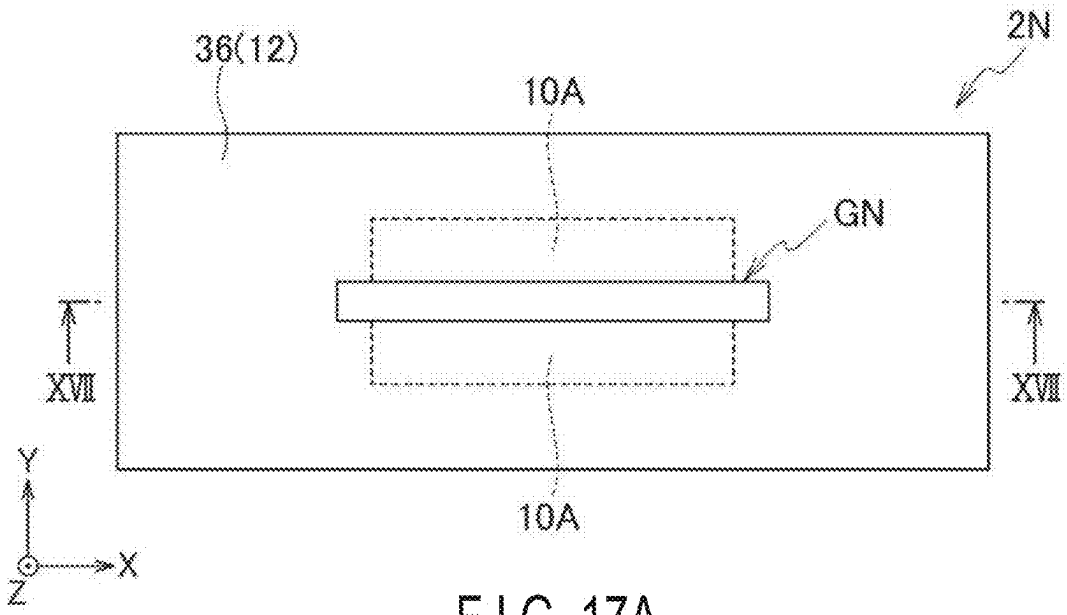

FIG. 17A

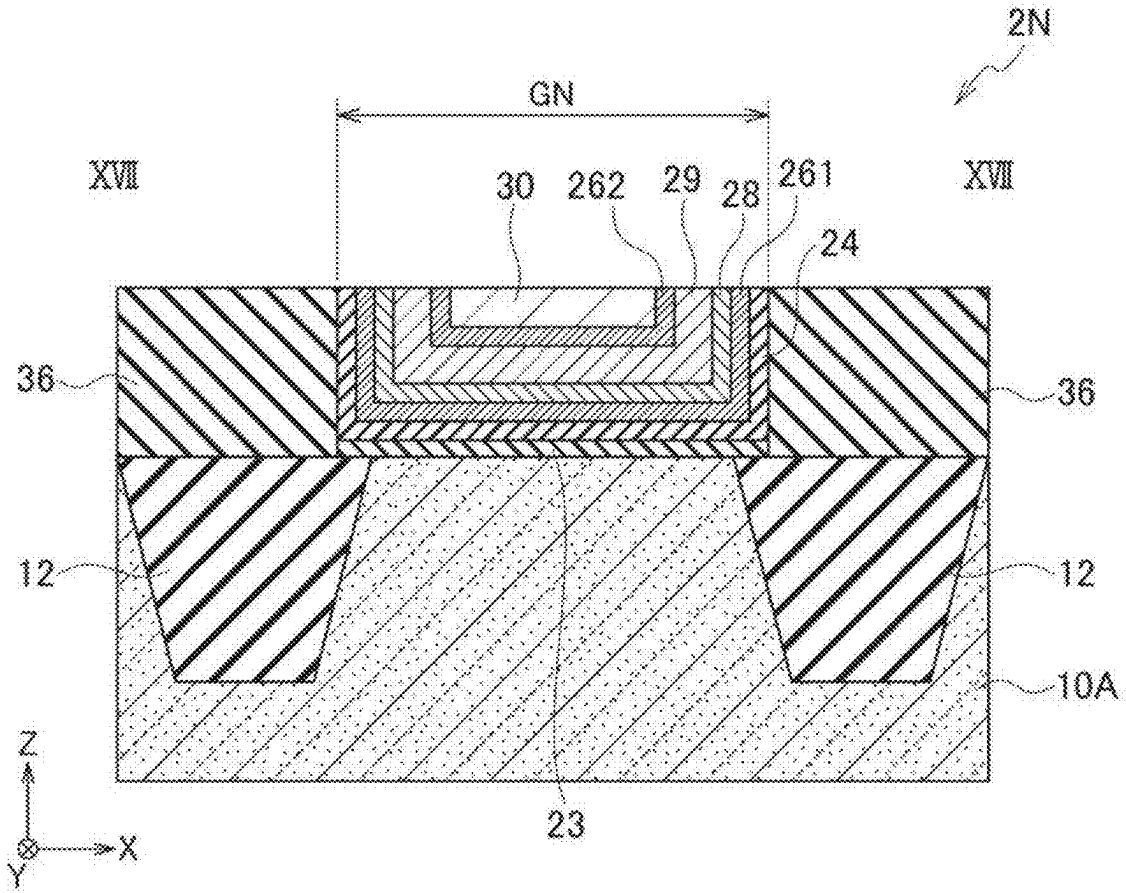

FIG. 17B

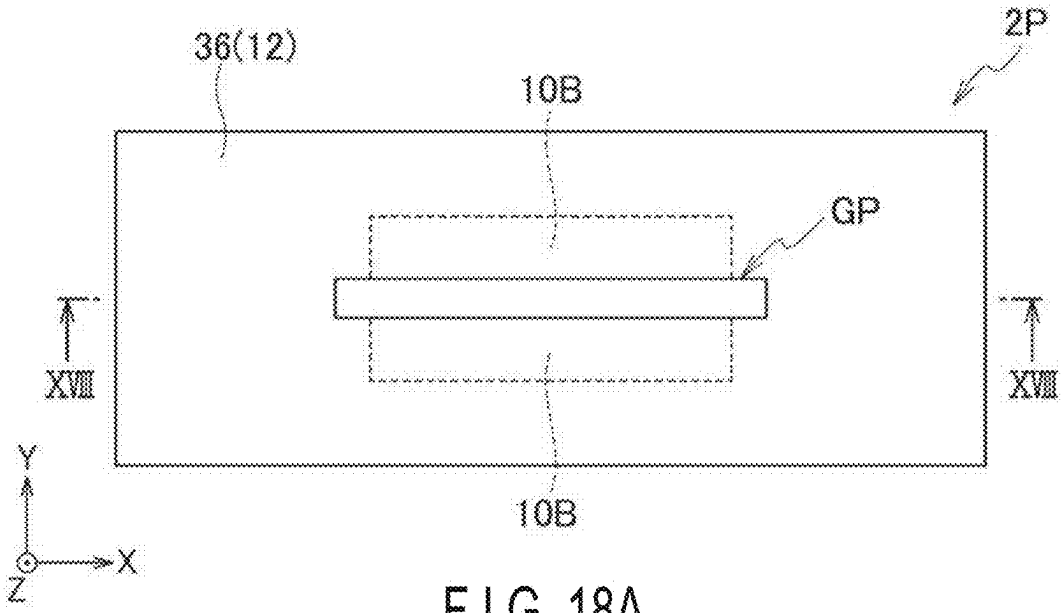

FIG. 18A

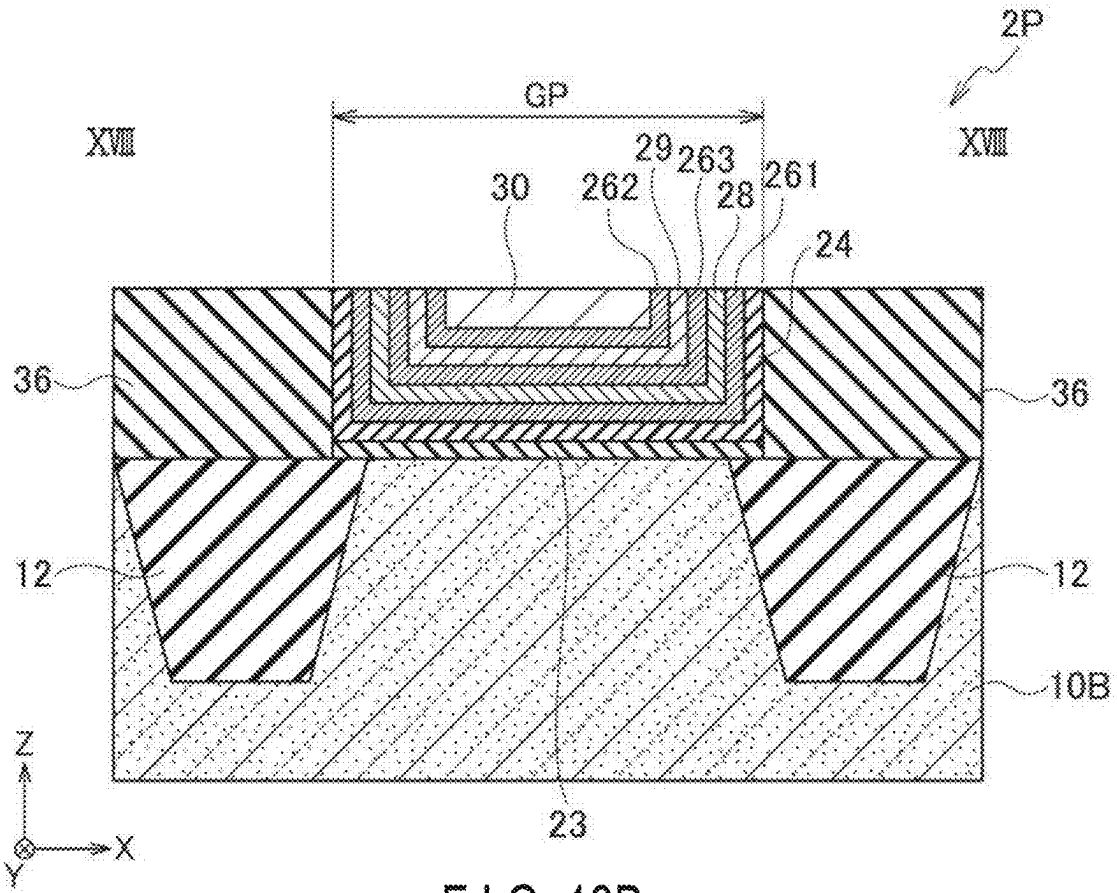

FIG. 18B

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD OF THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2024-022064, filed Feb. 16, 2024, the entire contents of which are incorporated herein by reference.

FIELD

[0002] Embodiments described herein relate generally to a semiconductor device and a manufacturing method of the same.

BACKGROUND

[0003] An electrically programmable fuse (e-Fuse) has a fuse region that can be electrically broken by a write operation or a programming operation, and can reduce an occupancy area on a chip. Therefore, it is used in a central processing unit (CPU), various kinds of memory devices, and large scale integration such as application specific integrated circuits (ASIC).

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. **1**A is a plan view of a fuse of a semiconductor device according to an embodiment.

[0005] FIG. **1**B is a sectional view along I-I line in FIG. **1**A.

[0006] FIG. **2**A is a plan view for illustrating a first manufacturing method of the fuse of the semiconductor device.

[0007] FIG. **2**B is a sectional view along II-II line in FIG. **2**A.

[0008] FIG. **3**A is a plan view for illustrating the first manufacturing method of the fuse of the semiconductor device.

[0009] FIG. **3**B is a sectional view along III-III line in FIG. **3**A.

[0010] FIG. **4**A is a plan view for illustrating the first manufacturing method of the fuse of the semiconductor device.

[0011] FIG. **4**B is a sectional view along IV-IV line in FIG. **4**A.

[0012] FIG. **5**A is a plan view of the first manufacturing method of the fuse of the semiconductor device according to the embodiment.

[0013] FIG. **5**B is a sectional view along a V-V line in FIG. **5**A.

[0014] FIG. **6**A is a plan view for illustrating the first manufacturing method of the fuse of the semiconductor device.

[0015] FIG. **6**B is a sectional view along VI-VI line in FIG. **6**A.

[0016] FIG. **7**A is a plan view for illustrating the first manufacturing method of the fuse of the semiconductor device.

[0017] FIG. **7**B is a sectional view along VII-VII line in FIG. **7**A.

[0018] FIG. **8**A is a plan view for illustrating the first manufacturing method of the fuse of the semiconductor device.

[0019] FIG. **8**B is a sectional view along VIII-VIII line in FIG. **8**A.

[0020] FIG. **9**A is a plan view for illustrating the first manufacturing method of the fuse of the semiconductor device.

[0021] FIG. **9**B is a sectional view along IX-IX line in FIG. **9**A.

[0022] FIG. **10**A is a plan view for illustrating the first manufacturing method of the fuse of the semiconductor device.

[0023] FIG. **10**B is a sectional view along X-X line in FIG. **10**A.

[0024] FIG. **11**A is a plan view for illustrating a second manufacturing method of the fuse of the semiconductor device.

[0025] FIG. **11**B is a sectional view along XI-XI line in FIG. **11**A.

[0026] FIG. **12**A is a plan view for illustrating the second manufacturing method of the fuse of the semiconductor device.

[0027] FIG. **12**B is a sectional view along XII-XII line in FIG. **12**A.

[0028] FIG. **13**A is a plan view for illustrating the second manufacturing method of the fuse of the semiconductor device.

[0029] FIG. **13**B is a sectional view along XIII-XIII line in FIG. **13**A.

[0030] FIG. **14**A illustrates a pattern disposition example 1 of a contact and a polysilicon layer.

[0031] FIG. **14**B illustrates a pattern disposition example 2 of the contact and the polysilicon layer.

[0032] FIG. **14**C illustrates a pattern disposition example 3 of the contact and the polysilicon layer.

[0033] FIG. **14**D illustrates a pattern disposition example 4 of the contact and the polysilicon layer.

[0034] FIG. **14**E illustrates a pattern disposition example 5 of the contact and the polysilicon layer.

[0035] FIG. **15**A is a sectional view of a fuse of a semiconductor device according to a modification 1.

[0036] FIG. **15**B is a sectional view of a fuse of a semiconductor device according to a modification 2.

[0037] FIG. **15**C is a sectional view of a fuse of a semiconductor device according to a modification 3.

[0038] FIG. **15**D is a sectional view of a fuse of a semiconductor device according to a modification 4.

[0039] FIG. **16**A is a plan view of a fuse of a semiconductor device according to a modification 5.

[0040] FIG. **16**B is a sectional view along XVI-XVI line in FIG. **16**A.

[0041] FIG. **17**A is a plan view of an NMOS transistor in a semiconductor device according to an embodiment.

[0042] FIG. **17**B is a sectional view along XVII-XVII line in FIG. **17**A.

[0043] FIG. **18**A is a plan view of a PMOS transistor in a semiconductor device according to an embodiment.

[0044] FIG. **18**B is a sectional view along XVIII-XVIII line in FIG. **18**A.

DETAILED DESCRIPTION

[0045] When replacement metal gate (RMG) technology is applied, since polysilicon serving both as a polysilicon gate electrode and a fuse is replaced with a metal gate material, the polysilicon cannot be used as a fuse.

[0046] Embodiments of this disclosure provide a highly reliable semiconductor device in which polysilicon is applicable to a fuse and a manufacturing method of the same.

[0047] In general, according to one embodiment, a semiconductor device comprises: a semiconductor substrate including an active region and an isolation region that is electrically isolated from the active region; a fuse disposed on the isolation region and including: a polysilicon layer including an impurity, and first and second electrode layers that are electrically connected to the polysilicon layer; and a transistor disposed on the active region and including a metal gate having a stack structure of electrode layers.

[0048] Hereinafter, embodiments will be described with reference to the drawings. Note that, in the following description, same or similar members or the like are denoted by same signs, and the description is appropriately omitted for members described once. In the following description, the direction perpendicular to a semiconductor substrate on XY plane is defined as Z direction, the direction which is orthogonal to Z direction and in which a polysilicon layer to be a fuse stretches is defined as X direction, and the direction perpendicular to Z and X directions is defined as Y direction.

(Configuration of Semiconductor Device)

[0049] FIG. **1**A is a plan view of a fuse **1** of a semiconductor device according to an embodiment. FIG. **1**B is a sectional view along I-I line in FIG. **1**A.

[0050] The semiconductor device according to the present embodiment includes the fuse **1** and a transistor provided on a semiconductor substrate **10**. The semiconductor device realizes a polysilicon fuse (poly fuse) structure by complementary metal oxide semiconductor (CMOS) device technology for which HKMG technology by a high-k dielectric (HK: High-k)/metal gate (MG) and RMG technology are combined.

[0051] As illustrated in FIG. **1**A and FIG. **1**B, the fuse **1** includes an isolation region **12** provided on the semiconductor substrate **10** such as a semiconductor wafer, a polysilicon layer **14**B which is provided on the isolation region **12** and for which a dummy polysilicon layer **14** is doped with an impurity, and electrode layers (**26**, **28**, and **30**) which are provided on the isolation region **12**, replace the dummy polysilicon layer **14**, and electrically connected with the polysilicon layer **14**B. In addition, a first electrode **321** and a second electrode **322** electrically connected with the electrode layers (**26**, **28**, and **30**) are provided. The first electrode **321** and the second electrode **322** configure electrode terminals of the fuse **1**. The first electrode **321** is connected to the metal electrode layer **30** via a contact CS**1**. The second electrode **322** is connected to the metal electrode layer **30** via a contact CS**2**. Note that a plurality of pattern disposition examples of the contact and the polysilicon layer will be described later in the description of FIG. **14**A to FIG. **14**E. The electrode layers (**26**, **28**, and **30**) are provided on both ends of the polysilicon layer **14**B that stretches in X direction on the isolation region **12**. The isolation region **12** is an insulating layer called shallow trench isolation (STI).

[0052] The transistor includes a metal gate which is provided on an active region electrically isolated by the isolation region **12** and includes a stack structure of the electrode layers (**26**, **28**, and **30**). The transistor will be described later in the description of FIG. **17**A, FIG. **17**B, FIG. **18**A, and FIG. **18**B.

[0053] As illustrated in FIG. **1**A and FIG. **1**B, the fuse **1** includes a stack structure of a high-k dielectric layer **24**, a metal-containing layer **26** provided on the high-k dielectric layer **24**, a work function metal (WF) layer **28** provided on the metal-containing layer **26**, and the metal electrode layer **30** provided on the work function metal layer **28**. Though illustration is omitted in FIG. **1**A and FIG. **1**B, an oxide film (IL: Inter Layer; SiO2) is provided between the high-k dielectric layer **24** and the isolation region **12**.

[0054] For the high-k dielectric layer **24**, a dielectric constant k is 10 or larger for example, and hafnium oxide (HfO2), hafnium silicate (HfSiO), tantalum oxide (Ta2O5), strontium titanate (SrTiO3), or zirconium oxide (ZrO2) or the like is applicable.

[0055] For the metal-containing layer **26**, titanium nitride (TiN), tantalum nitride (TaN), tantalum (Ta), or tungsten (W) or the like is applicable. For example, with TiN, an interface with the polysilicon layer **14**B is silicided by TiN. Therefore, a connection part of the polysilicon layer **14**B and the electrode layers (**26**, **28**, and **30**) is made low in resistance. In any case of TaN, Ta, or W, since the interface with the polysilicon layer **14**B is silicided by silicide of TaN, Ta, or W, the connection part is made low in resistance.

[0056] In the HKMG technology, the thin work function metal layer **28** is inserted between the high-k dielectric layer **24** and the metal electrode layer **30**. A threshold voltage can be adjusted by changing a thickness of the work function metal layer **28**. The work function metal layer **28** may contain a metal such as aluminum (Al) or lanthanum (La).

[0057] As the metal electrode layer **30**, for example, W or Al or the like is applicable.

[0058] The fuse **1** is electrically programmable by breaking the polysilicon layer **14**B by a voltage applied between the first electrode **321** and the second electrode **322**.

[0059] In the fuse **1**, by ion-implanting boron (B) for example as an impurity into the dummy polysilicon layer **14**, a B-doped polysilicon layer **14**B can be selectively left at an arbitrary part even after an RMG process, to be utilized as a polysilicon fuse. A heat treatment process may be added after a Bion implantation process.

[0060] In the fuse **1**, the polysilicon layer **14**B can be left at any part just by adding an impurity ion implantation process even in the RMG process which does not leave the dummy polysilicon layer **14**, and the polysilicon fuse can be realized. A bonding surface of the polysilicon layer **14**B and the electrode layers (**26**, **28**, and **30**) can be controlled to be in any shape by adjusting an implantation impurity profile of the polysilicon layer **14**B.

[0061] In the fuse **1**, there is no need to dispose a material having different resistivity in a material of a fuse formation layer. Therefore, the need for a layout of narrowing a line width and concentrating electric power on a breaking part to break the fuse is eliminated, and an occupancy area of the fuse can be reduced.

[0062] In the fuse **1**, since the polysilicon layer is applicable to the fuse, designing can be performed by a layout method finer than a metal fuse using a metal wiring layer, and a fuse area can be reduced. In the metal fuse using the metal wiring layer, there is a reliability defect that a broken part is bonded again due to an electromigration (EM) or stress migration (SM) phenomenon in a long term and fuse information lacks. In the fuse **1**, since the polysilicon layer is applicable to the fuse, a broken part is not bonded again

due to the EM or SM phenomenon, and a fuse structure having higher reliability in information holding than the metal fuse can be realized.

[0063] In the fuse **1**, by selectively implanting the impurity (B) into the dummy polysilicon layer **14** replaced in the RMG process, an etching rate of the polysilicon is lowered, and the polysilicon layer **14**B that functions as the fuse even after the RMG process can be left. Therefore, the fuse structure of the polysilicon can be easily realized even in an RMG process applied device.

[0064] In the fuse **1**, a shape of the connection part with the electrode layers (**26**, **28**, and **30**) can be controlled to be any shape by controlling a profile of impurity implantation of the polysilicon layer **14**B to be left as the fuse, and it is possible to adjust a contact area of the polysilicon layer **14**B and the electrode layers (**26**, **28**, and **30**) and reduce contact resistance.

[0065] For example, while W wiring is generally used for lower layer wiring in a memory device, W has a fusing point as high as 3407° C. and is unsuitable for the metal fuse structure. In this case, the fuse is formed by Cu (fusing point 1084.5° C.) or Al (fusing point 660° C.) wiring or the like of upper layer wiring, however, since a design rule of the upper layer wiring is relatively large, a fuse layout area increases. In the fuse **1**, by the polysilicon (fusing point 1410° C.), the occupancy area of the fuse is reduced and the highly reliable fuse structure can be realized.

[0066] When the direction in which the polysilicon layer **14**B stretches is X direction and the direction perpendicular to the semiconductor substrate **10** is Z direction, in a sectional structure along XZ plane of the polysilicon layer **14**B, a first bonding surface between the polysilicon layer **14**B and the electrode layers (**26**, **28**, and **30**) connected to the first electrode **321** and a second bonding surface between the polysilicon layer **14**B and the electrode layers (**26**, **28**, and **30**) connected to the second electrode **322** can be formed to have various arbitrary shapes.

[0067] As illustrated in FIG. **1**B, the fuse **1** has an inversely tapered shape in Z direction in the sectional structure along XZ plane of the polysilicon layer **14**B. Since this bonding part shape can widen an area as compared to a case of perpendicularly forming the bonding surface, the contact resistance of the bonding surface can be reduced.

(Impurity Ion Implantation)

[0068] By implanting the impurity (B) into the dummy polysilicon layer **14**, the etching rate can be controlled so as not to remove the boron-doped polysilicon layer **14**B even in the RMG process. A timing of impurity ion implantation into the dummy polysilicon layer **14** may be in an arbitrary process before peeling the dummy polysilicon layer **14** by the RMG process. As to be described later in a semiconductor device manufacturing method, it can be realized either before or after processing the fuse structure.

[0069] In addition, a shape of an end part of the polysilicon layer **14**B when etching the dummy polysilicon layer **14** can be controlled by controlling the impurity profile of the polysilicon layer **14**B to be the fuse. As the shape of the end part of the polysilicon layer **14**B, the impurity profile of the polysilicon layer **14**B can be controlled so as to be an inversely tapered, tapered, parallelogram, barrel or hand drum shape, for example. In the ion implantation, oblique ion implantation may be executed, or the ion implantation may be executed in multiple stages in order to adjust the shape. A dose amount and acceleration energy at the time of the ion implantation may be changed. Further, a heat treatment process may be appropriately added.

[0070] A value of etch selectivity is about 15 when a value of boron impurity concentration is 1×10^{20} cm−3, and a value of etch selectivity is about 100 or larger when the value of the boron impurity concentration is 1×10^{21} cm−3. Even when the value of the boron impurity concentration is 1×10^{19} cm−3, allowable etch selectivity is obtained. Thus, the value of the boron impurity concentration is preferably at least about 1×10^{19} cm−3 or larger.

[0071] By forming a bonding area of the polysilicon layer **14**B and the electrode layers (**26**, **28**, and **30**) to be large, a part where the fuse is to be broken is moved to the inside of the polysilicon layer **14**B of higher resistance compared to the electrode layers (**26**, **28**, and **30**), and a breaking region can be limited. In addition, by increasing the bonding area of the polysilicon layer **14**B and the electrode layers (**26**, **28**, and **30**), an area of a contact CS of the first electrode **321** and the second electrode **322**, and the metal electrode layer **30** can be formed to be small.

(Semiconductor Device Manufacturing Method according to Embodiment)

[0072] In a semiconductor device manufacturing method according to an embodiment, the electrically programmable fuse **1** is formed on the isolation region **12** of the semiconductor substrate **10**, and the transistor is formed on the active region of the semiconductor substrate **10**.

[0073] For the fuse **1**, the dummy polysilicon layer **14** is formed on the isolation region **12**, the polysilicon layer **14**B for which the dummy polysilicon layer **14** is doped with the impurity is formed, the dummy polysilicon layer **14** is removed by etching to leave the polysilicon layer **14**B on the isolation region **12**, and the electrode layers (**26**, **28**, and **30**) electrically connected to the polysilicon layer **14**B are formed instead of the dummy polysilicon layer **14**.

[0074] For the transistor, the dummy polysilicon layer is formed above the active region, then the dummy polysilicon layer is removed by etching, and a metal gate is formed instead of the dummy polysilicon layer.

[0075] First Manufacturing Method

[0076] In a first manufacturing method of the fuse **1** of the semiconductor device, the isolation region **12** is formed on the semiconductor substrate **10**, a non-doped dummy polysilicon layer **14** is formed on the isolation region **12**, the polysilicon layer **14**B for which the dummy polysilicon layer **14** is doped with the impurity is formed by lithography and ion implantation technology, an insulating layer **18** is formed on an entire surface, then the dummy polysilicon layer **14** is processed to expose a surface of the isolation region **12**, an interlayer insulating film **22** is formed on the entire surface, flattening is performed by flattening treatment, a surface of the polysilicon layer **14**B is exposed, the polysilicon layer **14**B is left and the dummy polysilicon layer **14** is removed to expose the surface of the isolation region **12** by etching, the electrode layers (**26**, **28**, and **30**) are formed on the entire surface, the surfaces of the electrode layers (**26**, **28**, and **30**) and the polysilicon layer **14**B are exposed flatly by the flattening treatment, an interlayer insulating film **34** is formed on the entire surface, and the first electrode **321** and the second electrode **322** are formed for the electrode layer **30** by patterning.

[0077] In the first manufacturing method of the fuse **1**, in processes, the impurity is ion-implanted into the dummy

polysilicon layer **14** before processing the dummy polysilicon layer **14**. Therefore, dimensional controllability in processes is relatively low and manufacture is easy.

[0078] (A) FIG. **2**A is a plan view for illustrating the first manufacturing method, and FIG. **2**B is a sectional view along II-II line in FIG. **2**A. First, as illustrated in FIG. **2**A and FIG. **2**B, the dummy polysilicon layer **14** is formed on the semiconductor substrate **10**. The dummy polysilicon layer **14** is formed on the isolation region **12** formed on the semiconductor substrate **10**. The dummy polysilicon layer **14** becomes the polysilicon layer **14**B for the fuse after doping, but is called a dummy polysilicon layer since the electrode part is replaced with a metal electrode by the RMG process.

[0079] (B) FIG. **3**A is a plan view for illustrating the first manufacturing method and FIG. **3**B is a sectional view along III-III line in FIG. **3**A. Next, as illustrated in FIG. **3**A and FIG. **3**B, after applying a resist layer **16** on the dummy polysilicon layer **14**, window opening for the dummy polysilicon layer **14** is executed by a lithography process, and ion implantation of impurity ions is performed. Here, as the impurity, boron (B) can be used for example. An ion implantation depth and an impurity concentration distribution of boron for the dummy polysilicon layer **14** can be controlled by the acceleration energy and the dose amount. In addition, an annealing treatment process may be executed after the ion implantation of boron. The ion implantation of boron may be executed in multiple stages. Further, oblique ion implantation technology may be used together. Here, the polysilicon layer **14**B in which boron is ion-implanted is a region to be the polysilicon fuse.

[0080] (C) FIG. **4**A is a plan view for illustrating the first manufacturing method and FIG. **4**B is a sectional view along IV-IV line in FIG. **4**A. Next, as illustrated in FIG. **4**A and FIG. **4**B, after peeling the resist layer **16**, the insulating layer (Cap film) **18** is formed on the polysilicon layer **14**B and the dummy polysilicon layer **14**. Here, as the insulating layer **18**, a silicon nitride film (SiN) can be used for example. The insulating layer **18** can be used as a hard mask.

[0081] (D) FIG. **5**A is a plan view for illustrating the first manufacturing method and FIG. **5**B is a sectional view along V-V line in FIG. **5**A. Next, as illustrated in FIG. **5**A and FIG. **5**B, with the insulating layer **18** as the hard mask, the dummy polysilicon layer **14** is removed by etching technology such as reactive ion etching (RIE), and the surface of the isolation region **12** is exposed. As a result, the processed dummy polysilicon layer **14** and polysilicon layer **14**B are formed on the isolation region **12**.

[0082] (E) FIG. **6**A is a plan view for illustrating the first manufacturing method and FIG. **6**B is a sectional view along VI-VI line in FIG. **6**A. Next, as illustrated in FIG. **6**A and FIG. **6**B, the insulating layer **18** and an oxide film **20** are formed on a side wall of the dummy polysilicon layer **14**. Further, after a flattening process, the surface of the insulating layer **18** is exposed, and the interlayer insulating film **22** is formed on an entire surface including the isolation region **12**. As a result, the dummy polysilicon layer **14** and the polysilicon layer **14**B are embedded and formed inside the interlayer insulating film **22** on the isolation region **12**.

[0083] (F) FIG. **7**A is a plan view for illustrating the first manufacturing method and FIG. **7**B is a sectional view along VII-VII line in FIG. **7**A. Next, as illustrated in FIG. **7**A and FIG. **7**B, by chemical mechanical polishing (CMP) technology, an entire device surface is etched back and the surfaces of the dummy polysilicon layer **14** and the polysilicon layer **14**B are exposed. On a side wall surface of the dummy polysilicon layer **14**, the insulating layer **18**, the oxide film **20**, and the interlayer insulating film **22** are successively stacked.

[0084] (G) FIG. **8**A is a plan view for illustrating the first manufacturing method and FIG. **8**B is a sectional view along VIII-VIII line in FIG. **8**A. Next, as illustrated in FIG. **8**A and FIG. **8**B, by wet etching, the dummy polysilicon layer **14** is peeled and removed. Here, the boron-doped polysilicon layer **14**B is left without being removed due to a difference in the etching rate. The surface of the isolation region **12** is exposed on bottom surfaces of recess regions **151** and **152** where the dummy polysilicon layer **14** is removed, and the insulating layer **18** is exposed on the side wall surfaces.

[0085] (H) FIG. **9**A is a plan view for illustrating the first manufacturing method and FIG. **9**B is a sectional view along IX-IX line in FIG. **9**A. Next, as illustrated in FIG. **9**A and FIG. **9**B, in order to form electrodes in the recess regions **151** and **152** where the dummy polysilicon layer **14** is peeled, the high-k dielectric layer **24**, the metal-containing layer **26**, the work function metal layer **28**, and the metal electrode layer **30** are successively stacked on the entire device surface. The oxide film (IL) is formed for a base of the high-k dielectric layer **24**, but the illustration is omitted.

[0086] (I) FIG. **10**A is a plan view for illustrating the first manufacturing method and FIG. **10**B is a sectional view along X-X line in FIG. **10**A. Next, as illustrated in FIG. **10**A and FIG. **10**B, by the CMP technology, the entire device surface is flattened, and the surface of the polysilicon layer **14**B is exposed. The recess regions **151** and **152** are filled with the high-k dielectric layer **24**, the metal-containing layer **26**, the work function metal layer **28**, and the electrode part of the metal electrode layer **30**.

[0087] (J) Next, as illustrated in FIG. **1**A and FIG. **1**B, after forming the interlayer insulating film **34** on the entire device surface, window opening to the interlayer insulating film **34** is executed by the lithography process, and the first electrode **321** connected to the metal electrode layer **30** via the contact CS**1** and the second electrode **322** connected to the metal electrode layer **30** via the contact CS**2** are formed.

[0088] Second Manufacturing Method

[0089] In a second manufacturing method of the fuse **1**, the isolation region **12** is formed on the semiconductor substrate **10**, the non-doped dummy polysilicon layer **14** is formed on the isolation region **12**, the insulating layer **18** is formed on the dummy polysilicon layer **14**, the dummy polysilicon layer **14** is processed to expose the surface of the isolation region **12**, the polysilicon layer **14**B for which the dummy polysilicon layer **14** is doped with the impurity is formed by the lithography and the ion implantation technology, the interlayer insulating film **22** is formed on the entire surface, flattening is performed by the flattening treatment, the surface of the polysilicon layer **14**B is exposed, the polysilicon layer **14**B is left and the dummy polysilicon layer **14** is removed to expose the surface of the isolation region **12** by etching, the electrode layers (**26**, **28**, and **30**) are formed on the entire surface, the surfaces of the electrode layers (**26**, **28**, and **30**) and the polysilicon layer **14**B are exposed flatly by the flattening treatment, the interlayer insulating film **34** is formed on the entire surface, and the first electrode **321** and the second electrode **322** are formed to the metal electrode layer **30** by patterning.

[0090] In the second manufacturing method of the fuse **1**, after processing the dummy polysilicon layer **14**, the ion implantation is performed and the polysilicon layer **14**B is formed on a process flow. Since the ion implantation is performed on the dummy polysilicon layer **14** after processing the dummy polysilicon layer **14**, high dimensional controllability is required in processes as compared with the first manufacturing method.

[0091] (K) FIG. **11**A is a plan view for illustrating the second manufacturing method and FIG. **11**B is a sectional view along XI-XI line in FIG. **11**A. First, after executing the process illustrated in FIG. **1**A and FIG. **1**B, as illustrated in FIG. **11**A and FIG. **11**B, the insulating layer **18** is formed on the dummy polysilicon layer **14**. Here, as the insulating layer **18**, similarly to the first manufacturing method, the silicon nitride film (SiN) is used for example.

[0092] (L) FIG. **12**A is a plan view for illustrating the second manufacturing method and FIG. **12**B is a sectional view along XII-XII line in FIG. **12**A. Next, as illustrated in FIG. **12**A and FIG. **12**B, with the insulating layer **18** as the hard mask, the dummy polysilicon layer **14** is removed by the etching technology such as the RIE, and the surface of the isolation region **12** is exposed. As a result, the gate-processed dummy polysilicon layer **14** is formed on the isolation region **12**.

[0093] (M) FIG. **13**A is a plan view for illustrating the second manufacturing method and FIG. **13**B is a sectional view along XIII-XIII line in FIG. **13**A. Next, as illustrated in FIG. **13**A and FIG. **13**B, after applying a resist layer **17** on the entire device surface, window opening to the insulating layer **18** and the dummy polysilicon layer **14** is executed by the lithography process. Further, the ion implantation of the impurity ions is performed via the insulating layer **18**. Here, as the impurity, boron (B) can be used for example.

[0094] (N) Next, the resist layer **17** is peeled and the structure illustrated in FIG. **5**A and FIG. **5**B after the processes similar to that in the first manufacturing method is obtained.

[0095] Hereinafter, the structure illustrated in FIG. **1**A and FIG. **1**B is obtained through the processes (FIG. **6**A and FIG. **6**B to FIG. **11**A and FIG. **11**B) similar to that in the first manufacturing method.

(Pattern of Contact and Polysilicon Layer)

[0096] Disposition Example 1

[0097] FIG. **14**A illustrates a pattern disposition example 1 of the contact and the polysilicon layer of the fuse **1**. One each of the contacts CS**1** and CS**2** is disposed in the metal electrode layer **30**, and the polysilicon layer **14**B is disposed in a straight shape in X direction. FIG. **14**A is a simplest pattern disposition example. In the pattern disposition example 1, as illustrated in FIG. **14**A, the polysilicon layer **14**B that stretches in X direction, the metal electrode layers **30** connected to the end parts in positive and negative X directions of the polysilicon layer **14**B, and the contact CS**1** and the contact CS**2** disposed in the metal electrode layers **30** are illustrated. The contact CS**1** is connected to the first electrode **321**, and the contact CS**2** is connected to the second electrode **322**.

[0098] Disposition Example 2

[0099] FIG. **14**B illustrates a pattern disposition example 2 of the contact and the polysilicon layer of the fuse **1**. In the pattern disposition example 2, as illustrated in FIG. **14**B, the polysilicon layer **14**B that stretches in X direction, the metal electrode layers **30** connected to the end parts in the positive and negative X directions of the polysilicon layer **14**B, and contacts CS**11** and CS**12** and contacts CS**21** and CS**22** disposed in the metal electrode layers **30** are illustrated. The contacts CS**11** and CS**12** are connected to the first electrode **321**, and the contacts CS**21** and CS**22** are connected to the second electrode **322**. Two contacts each are disposed for the first electrode **321** and the second electrode **322** and a connection yield of the contact can be improved. By disposing the plurality of contacts for the first electrode **321** and the second electrode **322**, connection resistance to the first electrode **321** and the second electrode **322** can be lowered and a fuse breaking part can be limited to the polysilicon layer **14**B. Note that the number of the contacts is not limited to 2 and may be 3 or more.

[0100] Disposition Example 3

[0101] FIG. **14**C illustrates a pattern disposition example 3 of the contact and the polysilicon layer of the fuse **1**. In the pattern disposition example 3, as illustrated in FIG. **14**C, a plurality of polysilicon layers **14**B**1**, **14**B**2**, and **14**B**3** divided in X direction, the metal electrode layer **30** connected to the polysilicon layer **14**B**1**, the metal electrode layer **30** connected to the polysilicon layer **14**B**3**, and the contacts CS**11** and CS**12** and the contacts CS**21** and CS**22** disposed in the metal electrode layers **30** are illustrated. The contacts CS**11** and CS**12** are connected to the first electrode **321**, and the contacts CS**21** and CS**22** are connected to the second electrode **322**. By providing the plurality of polysilicon layers in a fuse region, a range to be physically destroyed when breaking the fuse is prevented from being widened. In FIG. **14**C, the polysilicon layer **14**B**2** in a range that is long in X direction at a center is a high resistance region where the fuse is to be broken. The polysilicon layers **14**B**1** and **14**B**3** that are short in X direction at both ends are regions that function as a physical barrier to limit fuse breakage. In the example in FIG. **14**C, the plurality of contacts are disposed for the first electrode **321** and the second electrode **322** of the polysilicon layer, and the connection yield of the contact can be improved. Further, by disposing the plurality of contacts for the first electrode **321** and the second electrode **322**, the connection resistance to the first electrode **321** and the second electrode **322** can be lowered and the fuse breaking part can be limited to the polysilicon layer **14**B**2**. Note that metal layers **15** connecting the polysilicon layer **14**B**1** and the polysilicon layer **14**B**2** and the polysilicon layer **14**B**2** and the polysilicon layer **14**B**3** have a laminate structure similar to that of the electrode layers (**26**, **28**, and **30**).

[0102] Disposition Example 4

[0103] FIG. **14**D illustrates a pattern disposition example 4 of the contact and the polysilicon layer of the fuse **1**. In the pattern disposition example 4, the polysilicon layer **14**B, the metal electrode layers **30** connected to the end parts in the positive and negative X directions of the polysilicon layer **14**B, and the contacts CS**11** and CS**12** and the contacts CS**21** and CS**22** disposed in the metal electrode layers **30** are illustrated. The contacts CS**11** and CS**12** are connected to the first electrode **321**, and the contacts CS**21** and CS**22** are connected to the second electrode **322**. Two contacts each are disposed for the first electrode **321** and the second electrode **322** and the connection yield of the contact can be improved. In the example in FIG. **14**D, by turning a bonding surface of the polysilicon layer **14**B and the metal electrode

layer **30** not into a straight shape but into a zigzag shape in a planar view, resistance of the bonding surface of the polysilicon layer **14**B and the metal electrode layer **30** can be reduced by a layout pattern in addition to a sectional shape. Further, by disposing the plurality of contacts for the first electrode **321** and the second electrode **322**, the connection resistance to the first electrode **321** and the second electrode **322** can be lowered and the fuse breaking part can be limited to the polysilicon layer **14**B.

[0104] Disposition Example 5

[0105] FIG. **14**E illustrates a pattern disposition example 5 of the contact and the polysilicon layer of the fuse **1**. In the pattern disposition example 5, the fuse breaking part is formed narrow by the layout pattern to be a shape to limit the breaking part when breaking the fuse to the part of the polysilicon layer **14**B. In the example in FIG. **14**E, the plurality of contacts are disposed for the first electrode **321** and the second electrode **322** of the polysilicon layer, and the connection yield of the contact can be improved. Further, by disposing the plurality of contacts for the first electrode **321** and the second electrode **322**, the connection resistance to the first electrode **321** and the second electrode **322** can be lowered and the fuse breaking part can be limited to the part of the polysilicon layer **14**B formed narrow by the layout pattern.

(Modification 1)

[0106] FIG. **15**A is a sectional view of a fuse **1**A of a semiconductor device according to a modification 1. For the fuse **1**A, as illustrated in FIG. **15**A, in the sectional structure along XZ plane of the polysilicon layer **14**B, the first bonding surface between the polysilicon layer **14**B and the electrode layers (**26**, **28**, and **30**) connected to the first electrode **321** and the second bonding surface between the polysilicon layer **14**B and the electrode layers (**26**, **28**, and **30**) connected to the second electrode **322** have a bilaterally asymmetrical shape in X direction. In addition, the first bonding surface and the second bonding surface extend in Y direction and are parallel to each other. In the ion implantation process, by performing angular implantation of the impurity, both ends of the polysilicon layer **14**B can be turned to an asymmetrical structure. Since this bonding part shape can widen an area as compared with the case of perpendicularly forming the bonding surface, the contact resistance of the bonding surface can be reduced.

(Modification 2)

[0107] FIG. **15**B is a sectional view of a fuse **1**B of a semiconductor device according to a modification 2. For the fuse **1**B, as illustrated in FIG. **15**B, in the sectional structure along XZ plane of the polysilicon layer **14**B, the first bonding surface and the second boning surface have a bilateral hand drum (narrow-in-the-middle) shape in X direction. Since this bonding part shape can widen the area as compared with the case of perpendicularly forming the bonding surface, the contact resistance of the bonding surface can be reduced.

(Modification 3)

[0108] FIG. **15**C is a sectional view of a fuse **1**C of a semiconductor device according to a modification 3. For the fuse **1**C, as illustrated in FIG. **15**C, in the sectional structure along XZ plane of the polysilicon layer **14**B, the first bonding surface and the second boning surface have a tapered shape in Z direction. Since this bonding part shape can widen the area as compared with the case of perpendicularly forming the bonding surface, the contact resistance of the bonding surface can be reduced.

(Modification 4)

[0109] FIG. **15**D is a sectional view of a fuse **1**D of a semiconductor device according to a modification 4. For the fuse **1**D, as illustrated in FIG. **15**D, in the sectional structure along XZ plane of the polysilicon layer **14**B, the first bonding surface and the second boning surface have a bilateral barrel (bowing/thick-in-the-middle) shape in X direction. Since this bonding part shape can widen the area as compared with the case of perpendicularly forming the bonding surface, the contact resistance of the bonding surface can be reduced.

(Modification 5)

[0110] FIG. **16**A is a plan view of a fuse **1**E of a semiconductor device according to a modification 5. FIG. **16**B is a sectional view along XVI-XVI line in FIG. **16**A. The fuse **1**E is provided with the plurality of divided polysilicon layers **14**B**1**, **14**B**2**, and **14**B**3**. By providing the plurality of divided polysilicon layers **14**B**1**, **14**B**2**, and **14**B**3**, a range to be physically destroyed when breaking the fuse is prevented from being widened. In FIG. **16**A and FIG. **16**B, the polysilicon layer **14**B**2** in the range that is long in X direction at the center is the high resistance region where the fuse is to be broken, and the polysilicon layers **14**B**1** and **14**B**3** that are short in X direction at both ends are the regions that function as the physical barrier to limit fuse breakage. Note that the metal layers **15** are formed between the polysilicon layer **14**B**1** and the polysilicon layer **14**B**2** and between the polysilicon layer **14**B**2** and the polysilicon layer **14**B**3**. The metal layers **15** have the structure similar to that of the electrode layers (**26**, **28**, and **30**).

(Transistor Structure)

[0111] FIG. **17**A is a plan view of an NMOS transistor **2**N configuring a CMOS in a semiconductor device according to an embodiment, and FIG. **17**B is a sectional view along XVII-XVII line in FIG. **17**A. FIG. **18**A is a plan view of a PMOS transistor **2**P configuring a CMOS in a semiconductor device according to an embodiment, and FIG. **18**B is a sectional view along XVIII-XVIII line in FIG. **18**A.

[0112] In such semiconductor devices, a metal gate GN of the NMOS transistor **2**N and a metal gate GP of the PMOS transistor **2**P configuring the CMOS can be formed by CMOS device technology for which the HKMG technology and the RMG technology are combined.

[0113] As illustrated in FIG. **17**A and FIG. **17**B, the NMOS transistor **2**N includes the metal gate GN which is provided on an active region **10**A electrically isolated by the isolation region **12** and includes the stack structure of the electrode layers (**26**, **28**, and **30**) illustrated in FIG. **1**A and FIG. **1**B. Here, the active region **10**A can be formed by a P-type semiconductor substrate **10** or a P-well region.

[0114] As illustrated in FIG. **18**A and FIG. **18**B, the PMOS transistor **2**P includes the metal gate GP which is provided on an active region **10**B electrically isolated by the isolation region **12** and includes the stack structure of the electrode layers (**26**, **28**, and **30**) illustrated in FIG. **1**A and FIG. **1**B.

Here, the active region **10**B can be formed by an N-type semiconductor substrate **10** or an N-well region.

[0115] As illustrated in FIG. **17**A and FIG. **17**B, the metal gate GN includes an oxide film (IL) **23** provided on the active region **10**A, the high-k dielectric layer **24** provided on the oxide film **23**, a metal-containing layer **261** provided on the high-k dielectric layer **24**, the work function metal layer **28** provided on the metal-containing layer **261**, and the metal electrode layer **30** provided above the work function metal layer **28**. In the NMOS, between the work function metal layer **28** and the metal electrode layer **30**, a work function metal layer **29** and a metal-containing layer **262** are provided. The metal gate GN is embedded in an interlayer insulating film **36**, as illustrated in FIG. **17**A and FIG. **17**B.

[0116] As illustrated in FIG. **18**A and FIG. **18**B, the metal gate GP includes the oxide film **23** provided on the active region **10**B, the high-k dielectric layer **24** provided on the oxide film **23**, the metal-containing layer **261** provided on the high-k dielectric layer **24**, the work function metal layer **28** provided on the metal-containing layer **261**, and the metal electrode layer **30** provided above the work function metal layer **28**. In the PMOS, between the work function metal layer **28** and the metal electrode layer **30**, a metal-containing layer **263**, the work function metal layer **29** and the metal-containing layer **262** are provided. The metal gate GP is embedded in the interlayer insulating film **36**, as illustrated in FIG. **18**A and FIG. **18**B.

[0117] For the metal-containing layers **261**, **262**, and **263**, similarly to the metal-containing layer **26** used in the fuse **1**, TiN, TaN, Ta or W or the like is applicable. A threshold voltage of the PMOS can be adjusted by changing a thickness of the work function metal layer **29**. The work function metal layer **29** may contain a metal such as aluminum (Al) or lanthanum (La).

[0118] Thicknesses of members configuring the semiconductor devices in the present specification and a distance between the members or the like can be easily measured by physical analysis using a secondary electron microscope (SEM), for example. A position of a fuse part can be specified by planar SEM observation, and a fuse that is not broken or the like can be easily observed from sectional SEM observation.

[0119] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel devices and methods described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modification as would fall within the scope and spirit of the inventions.

What is claimed is:

1. A semiconductor device comprising:
- a semiconductor substrate including an active region and an isolation region that is electrically isolated from the active region;
- a fuse disposed on the isolation region and including:
  - a polysilicon layer including an impurity, and
  - first and second electrode layers that are electrically connected to the polysilicon layer; and
- a transistor disposed on the active region and including a metal gate having a stack structure of electrode layers.

2. The semiconductor device according to claim **1**, wherein the fuse is electrically programmable by a voltage applied between first and second electrode layers to break the polysilicon layer.

3. The semiconductor device according to claim **1**, wherein the first and second electrode layers of the fuse are provided on both ends of the polysilicon layer, and include:
- a first high-k dielectric layer,
- a first metal-containing layer on the first high-k dielectric layer,
- a first work function metal layer on the first metal-containing layer, and
- a first metal electrode layer on the first work function metal layer.

4. The semiconductor device according to claim **3**, wherein the first high-k dielectric layer includes one of: hafnium oxide, hafnium silicate, tantalum oxide, strontium titanate, and zirconium oxide.

5. The semiconductor device according to claim **3**, wherein the first metal-containing layer includes one of: titanium nitride, tantalum nitride, tantalum, and tungsten.

6. The semiconductor device according to claim **3**, wherein the first work function metal layer includes aluminum or lanthanum.

7. The semiconductor device according to claim **3**, wherein the first metal electrode layer includes tungsten (W) or aluminum (Al).

8. The semiconductor device according to claim **3**, wherein the stack structure of the metal gate includes:
- a second high-k dielectric layer,
- a second metal-containing layer on the second high-k dielectric layer,
- a second work function metal layer on the second metal-containing layer, and
- a second metal electrode layer on the second work function metal layer.

9. The semiconductor device according to claim **1**, wherein
- the polysilicon layer extends in a first direction parallel to the semiconductor substrate, and
- in a plane including the first direction and a second direction perpendicular to the semiconductor substrate, the polysilicon layer has a bilaterally symmetrical shape.

10. The semiconductor device according to claim **9**, wherein the polysilicon layer has one of: a tapered shape, an inversely tapered shape, a bilateral barrel shape, and a bilateral hand drum shape.

11. The semiconductor device according to claim **1**, wherein
- in a plane including the first direction and a second direction perpendicular to the semiconductor substrate, the polysilicon layer has a bilaterally asymmetrical shape.

12. The semiconductor device according to claim **1**, wherein the impurity of the polysilicon layer is boron, concentration of which is 1×10^{19} atoms/cm^3 or higher.

13. A semiconductor device manufacturing method comprising:
- forming an electrically programmable fuse on an isolation region of a semiconductor substrate and forming a transistor on an active region of the semiconductor substrate, the isolation region being electrically isolated from the active region, wherein

forming the fuse includes:
forming a first dummy polysilicon layer,
doping an impurity to the first dummy polysilicon layer and forming a first polysilicon layer therein,
removing the first dummy polysilicon layer by etching while leaving the first polysilicon layer, and
forming first and second electrode layers at locations from which the first dummy polysilicon layer was removed, such that the first and second electrode layers are electrically connected to the first polysilicon layer, and
forming the transistor includes:
forming a second dummy polysilicon layer,
removing the second dummy polysilicon layer by etching, and
forming a metal gate at a location from which the second dummy polysilicon layer was removed.

14. The semiconductor device manufacturing method according to claim **13**, wherein the first and second electrode layers are on both ends of the first polysilicon layer on the isolation region.

15. The semiconductor device manufacturing method according to claim **13**, wherein forming the first and second electrode layers includes forming:
a first high-k dielectric layer,
a first metal-containing layer on the first high-k dielectric layer,
a first work function metal layer on the first metal-containing layer, and
a first metal electrode layer on the first work function metal layer.

16. The semiconductor device manufacturing method according to claim **13**, wherein
the metal gate is provided above the active region, and
forming the metal gate includes forming:
a second high-k dielectric layer,
a second metal-containing layer on the second high-k dielectric layer,
a second work function metal layer on the second metal-containing layer, and
a second metal electrode layer on the second work function metal layer.

17. The semiconductor device manufacturing method according to claim **13**, further comprising:
adjusting a concentration distribution of the impurity in the first polysilicon layer to control a shape of bonding surfaces of the first polysilicon layer and the first and second electrode layers.

18. The semiconductor device manufacturing method according to claim **13**, wherein
the first polysilicon layer extends in a first direction parallel to the semiconductor substrate, and
in a plane including the first direction and a second direction perpendicular to the semiconductor substrate, the first polysilicon layer has a symmetrical shape.

19. The semiconductor device manufacturing method according to claim **13**, wherein the impurity is boron, concentration of which is at least 1×10^{19} cm^{-3} or higher.

20. A semiconductor device manufacturing method comprising:
forming an isolation region on a semiconductor substrate;
forming a dummy polysilicon layer on the isolation region;
doping an impurity to the dummy polysilicon layer and forming a first polysilicon layer therein by lithography and ion implantation technology;
applying an insulating layer from above, processing the first polysilicon layer to expose a surface of the isolation region, and applying a first interlayer insulating film from above;
performing flattening treatment and exposing a surface of the first polysilicon layer;
removing the dummy polysilicon layer to expose the surface of the isolation region by etching;
applying an electrode layer from above;
exposing surfaces of the electrode layer and the first polysilicon layer flatly by flattening treatment; and
applying a second interlayer insulating film from above, and forming first and second electrodes electrically connected to the electrode layer by patterning.

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