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(54) **MIM STRUCTURE WITH ROUNDED SIDEWALL AND FABRICATING METHOD OF THE SAME**

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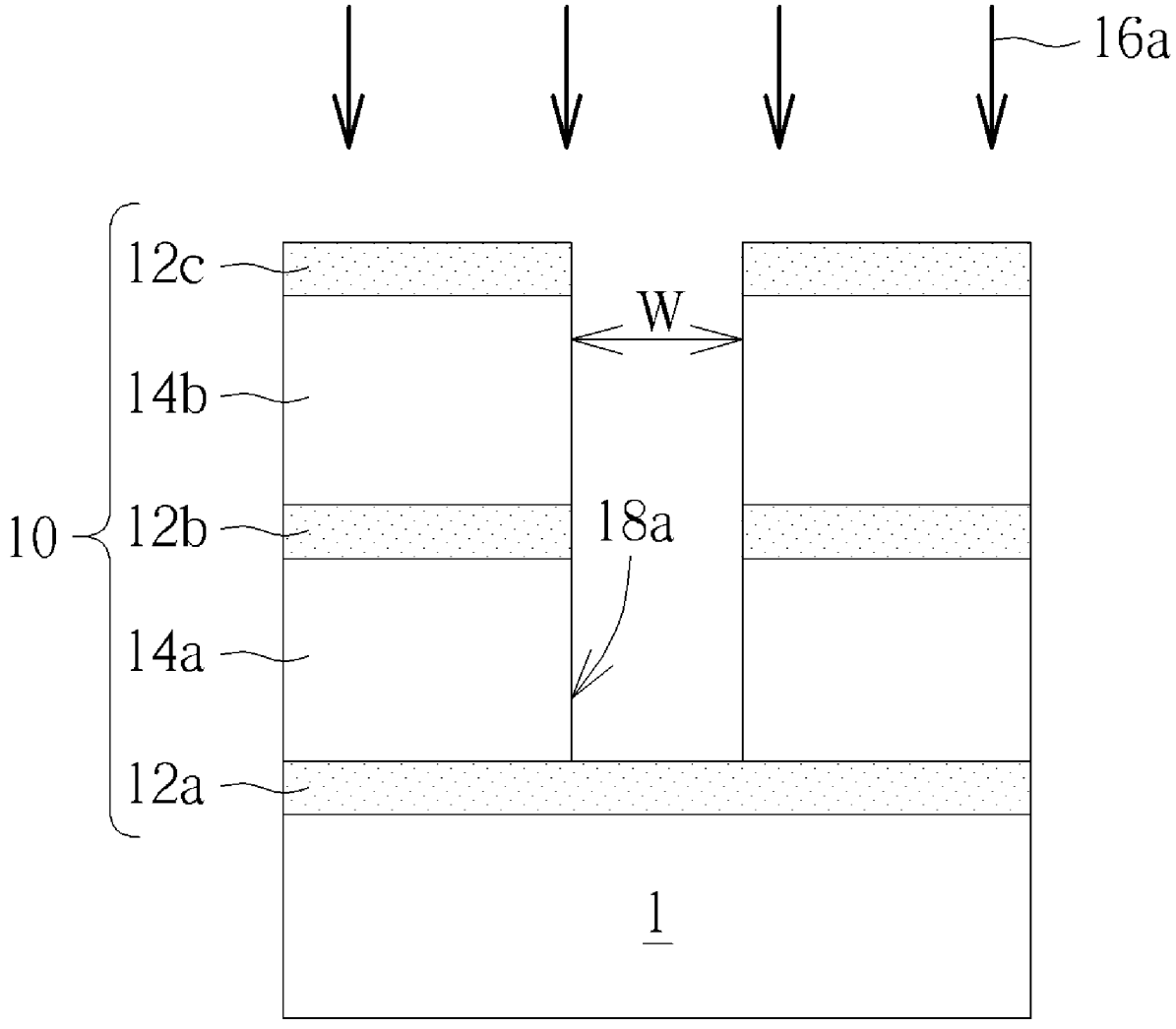
(57) **ABSTRACT**

An MIM capacitor structure with a rounded sidewall includes a stacked layer. The stacked layer includes at least one silicon-containing material layer and at least one oxygen-containing silicon compound layer alternately stacked, and a trench is disposed in the stacked layer. The trench has a rounded sidewall and a vertical sidewall. The vertical sidewall and the rounded sidewall are connected to each other. An MIM capacitor is disposed in the trench and contacts the trench. An insulating layer fills the trench and seals an opening of the trench. An air gap is disposed in the insulating layer.



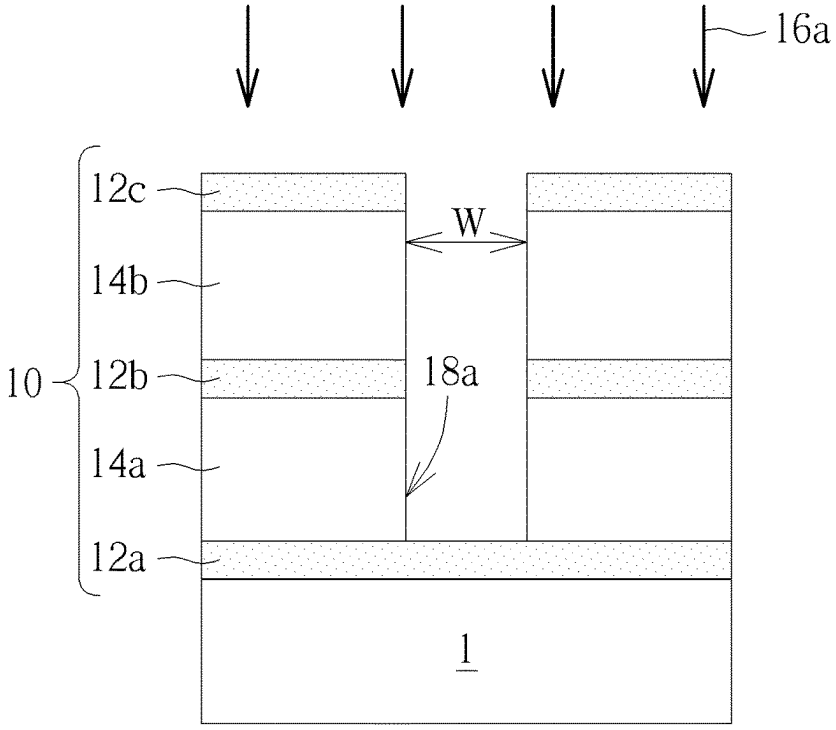

16a
12c
W
14b
10
12b
18a
14a
12a
1

FIG. 1

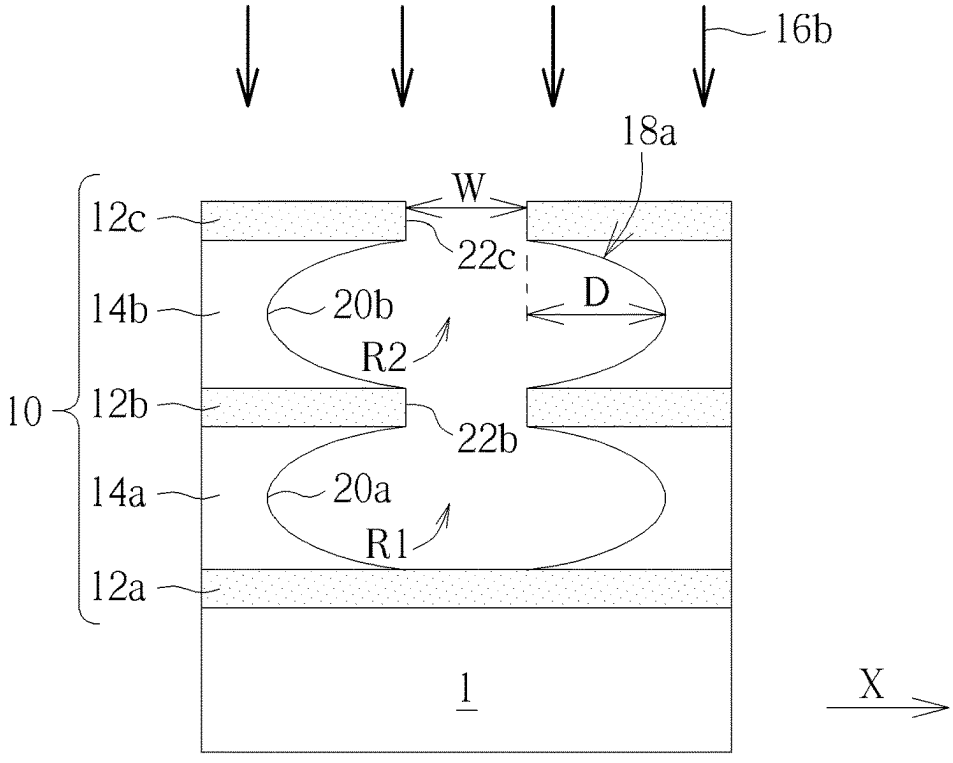

16b
18a
W
12c
22c
14b
20b
D
R2
10
12b
22b
14a
20a
R1
12a
1
X

FIG. 2

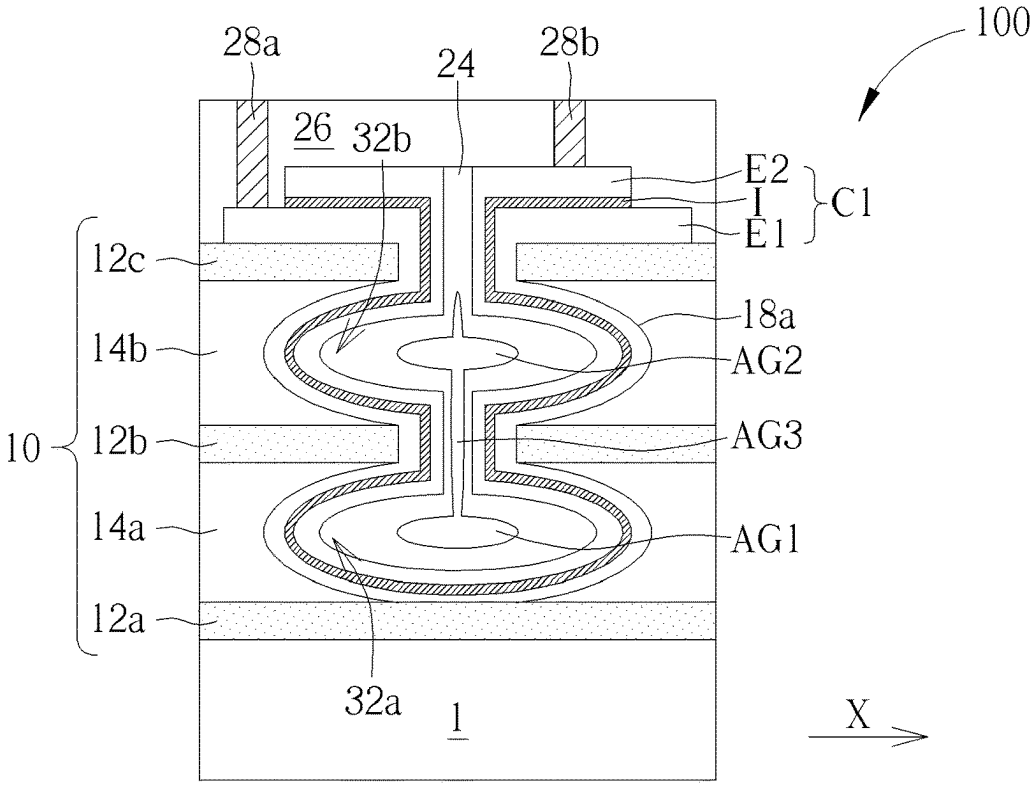

100
28a
24
28b
26
32b
E2
I
E1
C1
12c
14b
18a
AG2
10
12b
AG3
14a
AG1
12a
32a
1
X

FIG. 3

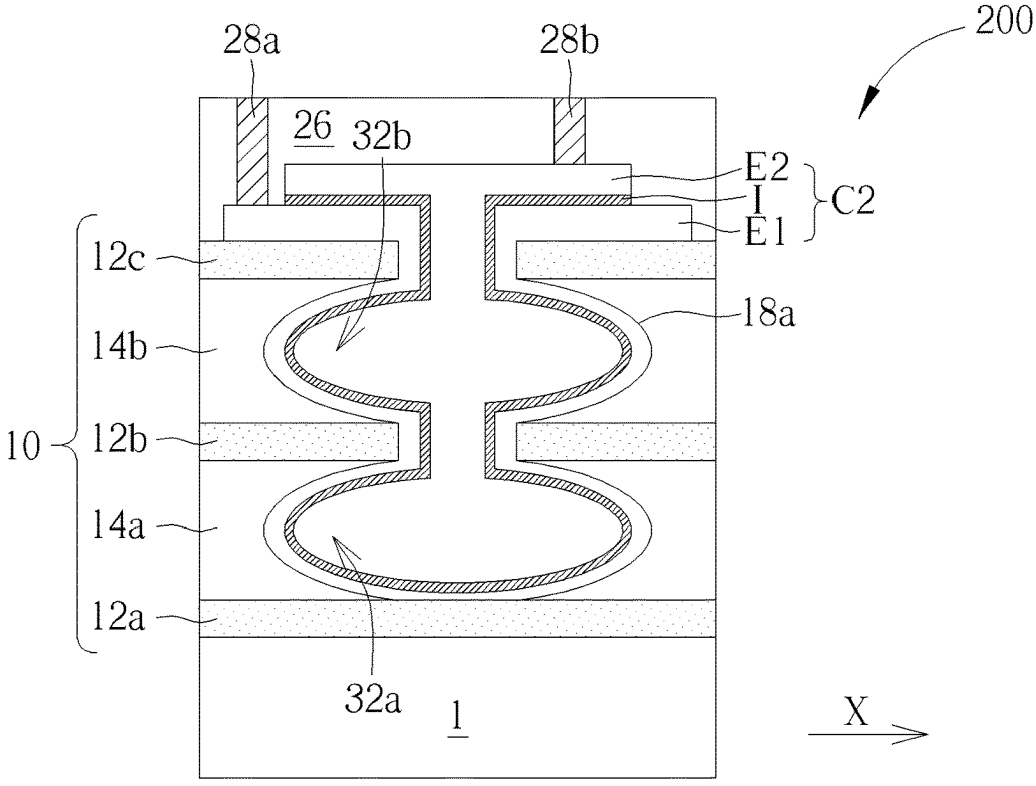

200
28a
28b
26
32b
E2
I
E1
C2
12c
14b
18a
10
12b
14a
12a
32a
1
X

FIG. 4

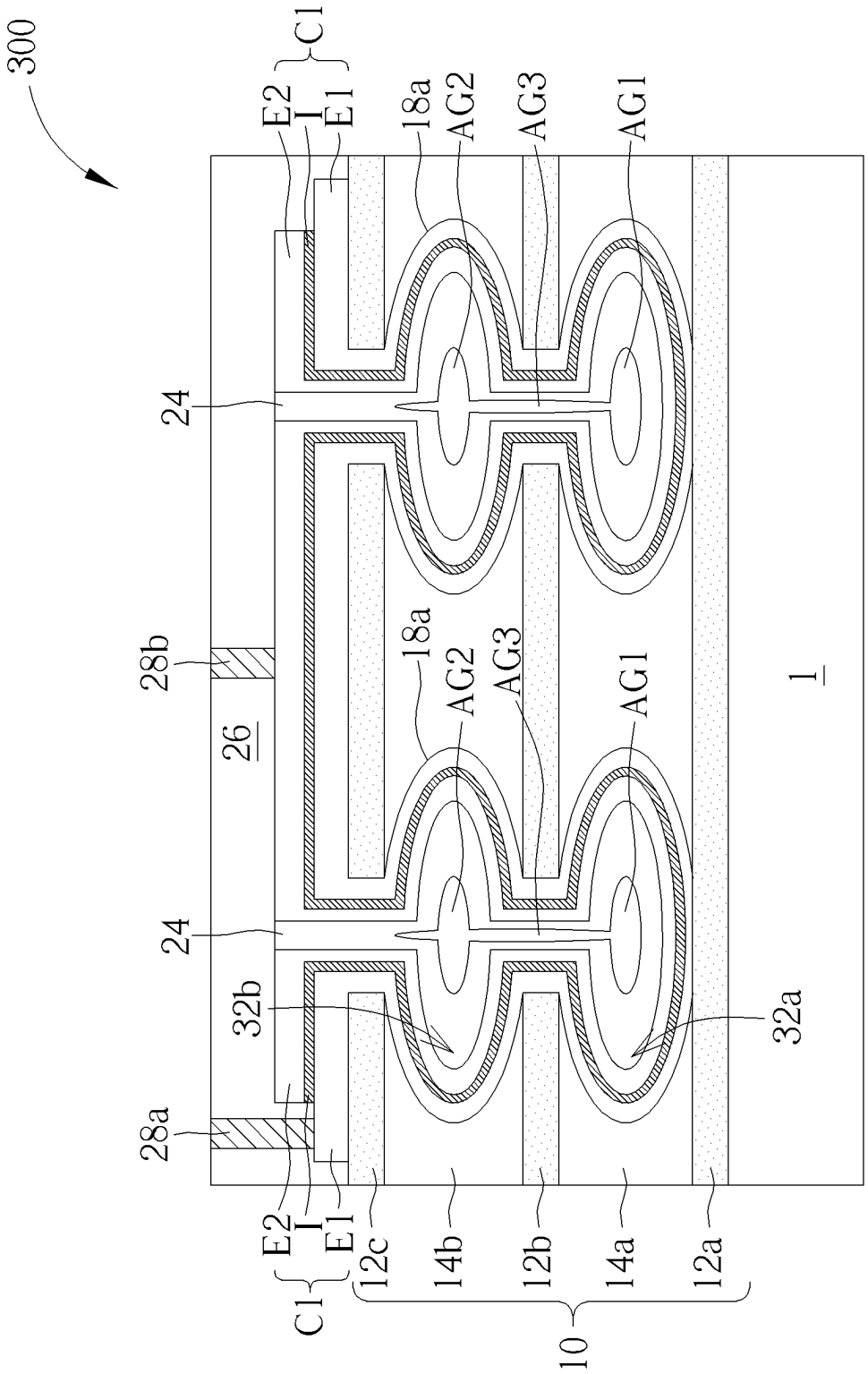

300
C1
E2
I
E1
18a
AG2
AG3
AG1
24
28b
26
18a
AG2
AG3
AG1
1
24
32b
32a
28a
E2
I
E1
C1
12c
14b
12b
14a
12a
10

FIG. 5

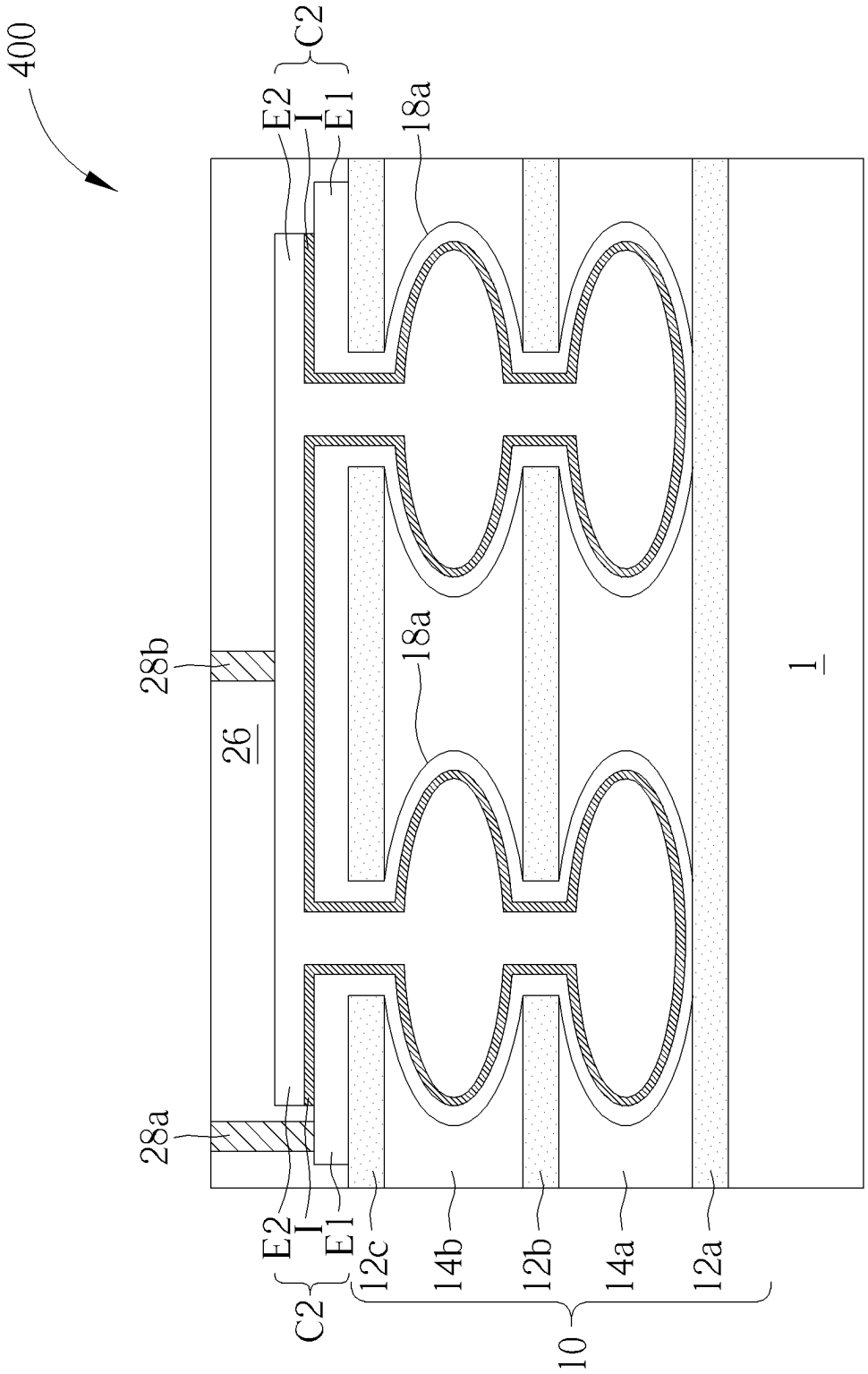


FIG. 6

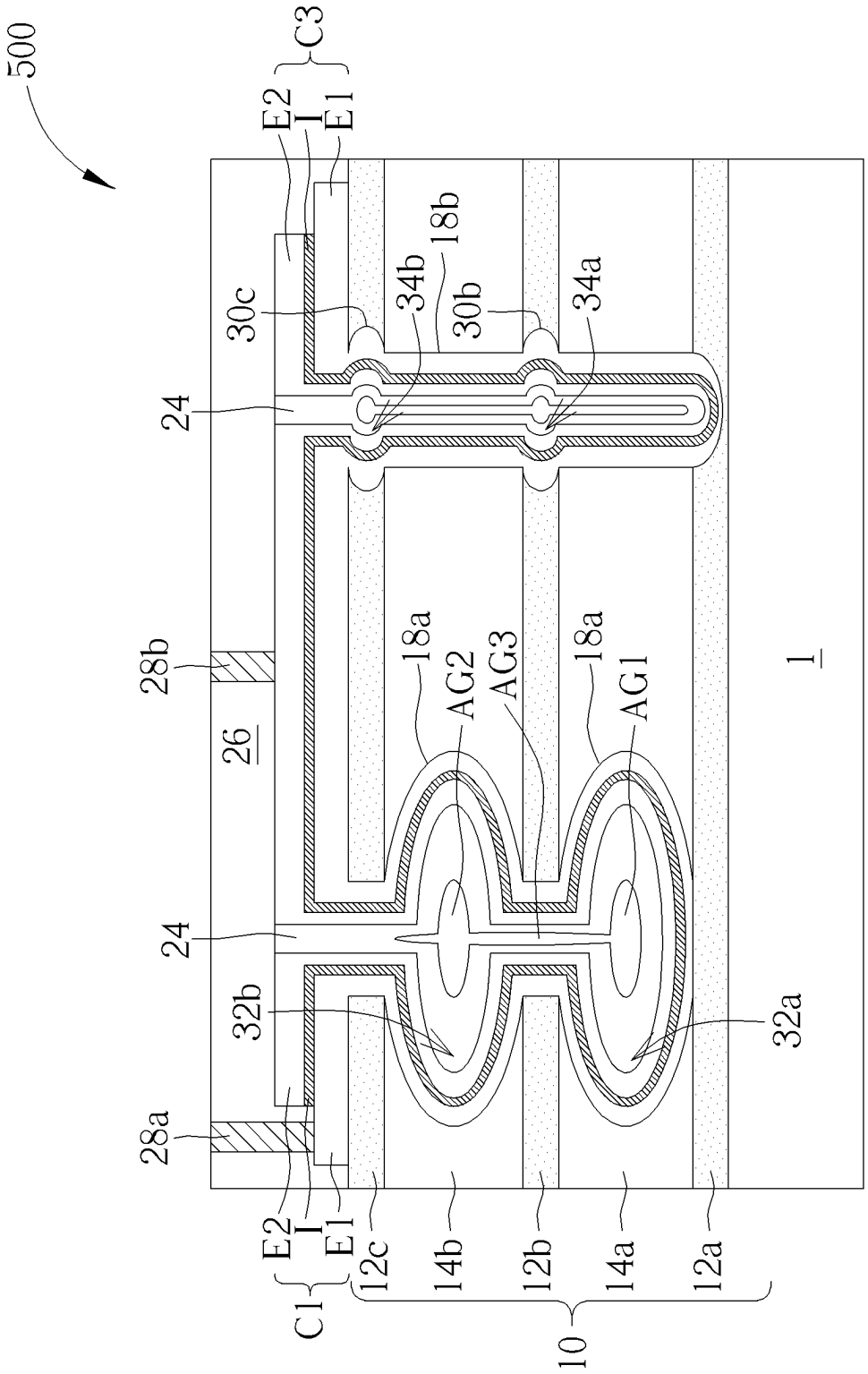

500
C3
E2
I
E1
18b
34b
30b
34a
30c
24
28b
26
18a
AG2
AG3
18a
AG1
1
24
32b
32a
28a
E2
I
E1
12c
14b
12b
14a
12a
C1
10

FIG. 7

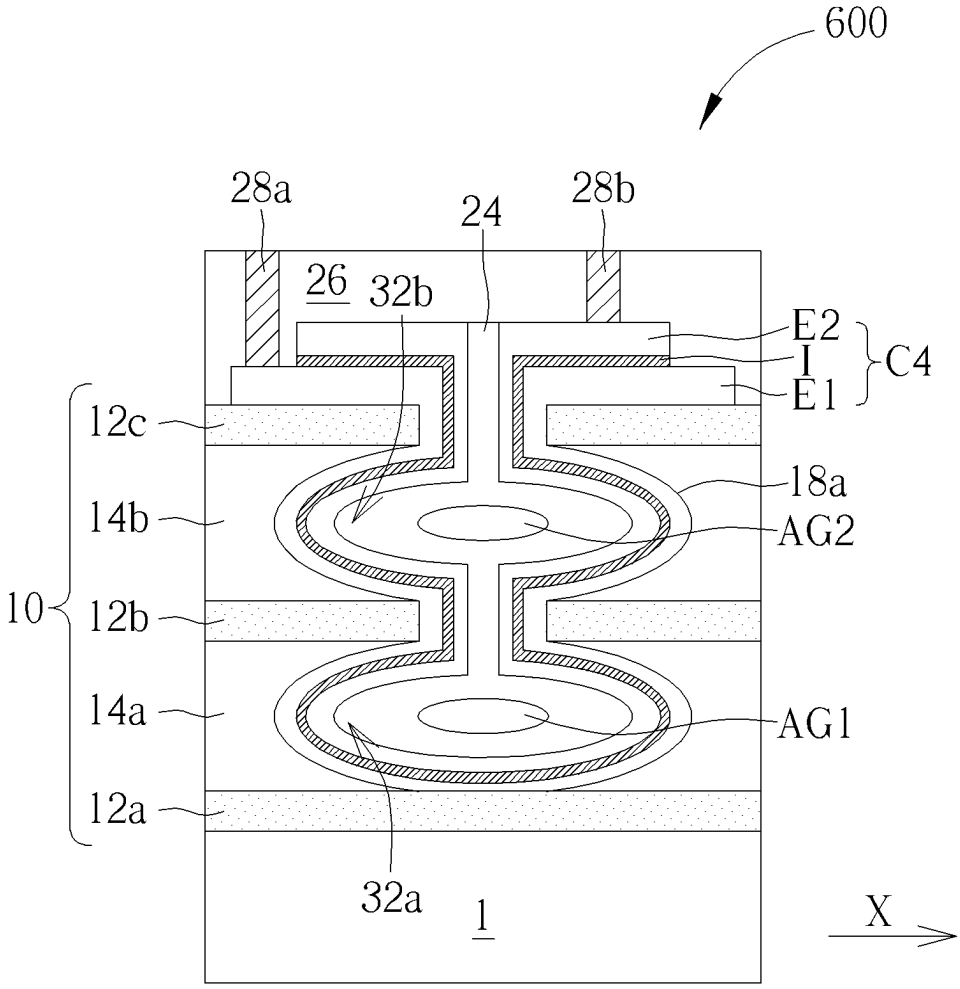

600
28a
24
28b
26
32b
E2
I
E1
C4
12c
14b
18a
AG2
10
12b
14a
AG1
12a
32a
1
X

FIG. 8

MIM STRUCTURE WITH ROUNDED SIDEWALL AND FABRICATING METHOD OF THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a metal-insulator-metal (MIM) capacitor, in particular to an MIM capacitor with a rounded sidewall.

2. Description of the Prior Art

[0002] MIM capacitors are not only used to filter noise in radio frequency circuits, or as load components in digital circuits, it is also widely used in general integrated circuit and circuit board manufacturing processes. In recent years, with the development of semiconductor integrated circuit process technology, the minimum width of devices on semiconductor substrates has gradually become smaller; therefore the density of integrated circuits per unit area is increased.

[0003] Due to the increase in the density of memory cell, the space occupied by a capacitor per unit area for charge storage will become smaller. Therefore, it is necessary to develop capacitors with small size but high capacitance. Currently, how to form MIM capacitors with higher capacitance under high density has become a goal for semiconductor field.

SUMMARY OF THE INVENTION

[0004] In view of this, the present invention provides an MIM capacitor structure with a rounded sidewall and a fabricating method of the same to form an MIM capacitor with high capacitance.

[0005] According to a preferred embodiment of the present invention, an MIM capacitor structure with a rounded sidewall includes a stacked layer, wherein the stacked layer includes at least a silicon-containing material layer and at least one oxygen-containing silicon compound layer stacked alternately. A trench is disposed in the stacked layer, wherein the trench has a rounded sidewall and a vertical sidewall, and the vertical sidewall and the rounded sidewall are connected to each other. An MIM capacitor is disposed in the trench and contacts the trench. An insulating layer fills in the trench and seals up an opening of the trench. An air gap is disposed in the insulating layer.

[0006] According to another preferred embodiment of the present invention, a fabricating method of an MIM capacitor structure with a rounded sidewall includes providing an oxygen-containing silicon compound layer and a silicon-containing material layer. Next, a first etching is performed to etch the oxygen-containing silicon compound layer and the silicon-containing material layer to form a trench. Later, a second etching is performed to etch the oxygen-containing silicon compound layer to laterally expand a portion of a sidewall of the trench to form a rounded sidewall. After forming the rounded sidewall, an MIM capacitor is formed to fill in and contact the trench. Finally, after forming the MIM capacitor, an insulating layer is formed to fill the trench and seal up the opening of the trench, wherein the insulating layer defines an air gap.

[0007] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. **1** to FIG. **3** depict a fabricating method of an MIM capacitor structure with a rounded sidewall according to a first preferred embodiment of the present invention, wherein:

[0009] FIG. **1** depicts a stacked layer;

[0010] FIG. **2** is a fabricating stage in continuous of FIG. **1**; and

[0011] FIG. **3** is a fabricating stage in continuous of FIG. **2**.

[0012] FIG. **4** depicts an MIM capacitor structure with a rounded sidewall according to a second preferred embodiment of the present invention.

[0013] FIG. **5** depicts an MIM capacitor structure with a rounded sidewall according to a third preferred embodiment of the present invention.

[0014] FIG. **6** depicts an MIM capacitor structure with a rounded sidewall according to a fourth preferred embodiment of the present invention.

[0015] FIG. **7** depicts an MIM capacitor structure with a rounded sidewall according to a fifth preferred embodiment of the present invention.

[0016] FIG. **8** depicts an MIM capacitor structure with a rounded sidewall according to a sixth preferred embodiment of the present invention.

DETAILED DESCRIPTION

[0017] FIG. **1** to FIG. **3** depict a fabricating method of an MIM capacitor structure with a rounded sidewall according to a first preferred embodiment of the present invention.

[0018] As shown in FIG. **1**, a substrate **1** is provided. A stacked layer **10** is disposed on the substrate **1**. The substrate **1** includes a silicon substrate, a germanium substrate, a gallium arsenide substrate, a silicon germanium substrate, an indium phosphide substrate, a gallium nitride substrate, a silicon carbide substrate or a silicon on insulator (SOI) substrate. The stacked layer **10** includes at least one silicon-containing material layer and at least one oxygen-containing silicon compound layer alternately stacked on one another. For example, a first silicon-containing material layer **12***a*, a first oxygen-containing silicon compound layer **14***a*, a second silicon-containing material layer **12***b*, a second oxygen-containing silicon compound layer **14***b* and a third silicon-containing material layer **12***c* disposed from bottom to top in sequence. The number of layers in the stacked layer **10** can be adjusted according to different needs, and the material of the silicon-containing material layer and the material of the oxygen-containing silicon compound layer can also be changed according to different requirements. However, the silicon-containing material layer and the oxygen-containing silicon compound layer adjacent to each other need to have different etching selectivity ratios with respective to the same etchant. According to a preferred embodiment of the present invention, the first silicon-containing material layer **12***a*, the second silicon-containing material layer **12***b* and the third silicon-containing material layer **12***c* may be silicon nitride, poly-crystalline silicon, single-crystalline silicon or amorphous silicon. The first oxygen-containing silicon com-

pound layer **14***a* and the second oxygen-containing silicon compound layer **14***b* are preferably silicon oxide.

[0019] Next, a first etching **16***a* is performed to etch the third silicon-containing material layer **12***c*, the second oxygen-containing silicon compound layer **14***b*, the second silicon-containing material layer **12***b* and the first oxygen-containing silicon compound layer **14***a* to form a trench **18***a* in the third silicon-containing material layer **12***c*, the second oxygen-containing silicon compound layer **14***b*, the second silicon-containing material layer **12***b* and the first oxygen-containing silicon compound layer **14***a*. The trench **18***a* uses the first silicon-containing material layer **12***a* as a bottom. The width W of the opening of the trench **18***a* is preferably between 100 and 1000 nanometers. In addition, the sidewall of the trench **18***a* is perpendicular to the top surface of the stacked layer **10**. The sidewall of the trench **18***a* in the third silicon-containing material layer **12***c*, the second oxygen-containing silicon compound layer **14***b*, the second silicon-containing material layer **12***b* and the first oxygen-containing silicon compound layer **14***a* are aligned with each other. The first etching **16***a* is preferably a dry etching.

[0020] As shown in FIG. **2**, a second etching **16***b* is performed to etch the second oxygen-containing silicon compound layer **14***b* and the first oxygen-containing silicon compound layer **14***a* to laterally expand part of the trench **18***a*. The distance D laterally expanded is preferably 0.01 to 1 times of the width W of the opening. The second etching **16***b* includes a wet etching. The second etching **16***b* preferably include only the wet etching. In details, the second etching **16***b* is to selectively etch silicon oxide and not etch silicon nitride or silicon. The wet etching can use dilute hydrofluoric acid as the etchant. According to a preferred embodiment of the present invention, the etching selectivity ratio of silicon oxide to silicon nitride of the etchant is 16.9. Therefore, while the second oxygen-containing silicon compound layer **14***b* and the first oxygen-containing silicon compound layer **14***a* are etched by the etchant, the surfaces of the third silicon-containing material layer **12***c*, the second silicon-containing material layer **12***b* and the first silicon-containing material layer **12***a* can be considered as not etched by the etchant. When the second etching **16***b* is performed, the trench **18***a* in the second oxygen-containing silicon compound layer **14***b* and the first oxygen-containing silicon compound layer **14***a* is etched to be expanded laterally to form a rounded sidewall **20***a* and a rounded sidewall **20***b*. The trench **18***a* in the third silicon-containing material layer **12***c* and the second silicon-containing material layer **12***b* can be regarded as not being etched. Therefore, the sidewall of the trench **18***a* in the third silicon-containing material layer **12***c* and the second silicon-containing material layer **12***b* maintain vertical, and the sidewall of the trench **18***a* in the third silicon-containing material layer **12***c* and the sidewall of the trench **18***a* in the second silicon-containing material layer **12***b* are respectively defined as a vertical sidewall **22***c* and a vertical sidewall **22***b*. The rounded sidewall **20***b* is connected to the vertical sidewall **22***c* and the vertical sidewall **22***b*. The rounded sidewall **20***a* and the vertical sidewall **22***b* are connected. The above-mentioned lateral expansion refers to an expansion along the horizontal direction X parallel to the top surface of the third silicon-containing material layer **12***c*.

[0021] As shown in FIG. **3**, a silicon oxide liner (not shown) may be optionally formed to cover the trench **18***a* and the top surface of the third silicon-containing material layer **12***c*. If the third silicon-containing material layer **12***c*, the second silicon-containing material layer **12***b* and the first silicon-containing material layer **12***a* are made of silicon nitride, the silicon oxide lining layer can be omitted. If the third silicon-containing material layer **12***c*, the second silicon-containing material layer **12***b* and the first silicon-containing material layer **12***a* are poly-crystalline silicon, single-crystalline silicon or amorphous silicon, the silicon oxide lining layer is required. In this embodiment, the third silicon-containing material layer **12***c*, the second silicon-containing material layer **12***b* and the first silicon-containing material layer **12***a* are exemplified as silicon nitride and the silicon oxide liner is omitted. Then, a first electrode E**1**, a capacitor dielectric layer I and a second electrode E**2** are formed in sequence to cover the trench **18***a* and the top surface of the third silicon-containing material layer **12***c*. Later, an insulating layer **24** is formed to fill the trench **18***a*. The insulating layer **24** seals up the opening of the trench **18***a* and forms air gaps AG**1**/AG**2**/AG**3** in the insulating layer **24**.

[0022] After that, the first electrode E**1**, the capacitor dielectric layer I, the second electrode E**2** and the insulating layer **24** are patterned to make the length of the first electrode E**1** on the third silicon-containing material layer **12***c* is greater than the length of the second electrode E**2** on the third silicon-containing material layer **12***c* along the horizontal direction X. Moreover, the first electrode E**1**, the capacitor dielectric layer I, the second electrode E**2** and the insulating layer **24** all protrude above the opening of the trench **18***a*. The first electrode E**1**, the capacitor dielectric layer I, and the second electrode E**2** constitute the MIM capacitor C**1**. Then, a dielectric layer **26** is formed to cover the third silicon-containing material layer **12***c*. Subsequently, contact plugs **28***a*/**28***b* are formed in dielectric layer **26**. The contact plug **28***a* contacts the first electrode E**1**, and the contact plug **28***b* contacts the second electrode E**2**. Now, an MIM capacitor structure **100** with a rounded sidewall of the present invention is completed.

[0023] According to the second preferred embodiment of the present invention, the insulating layer **24** may not be formed, and the remaining space of the trench **18***a* can be filled up with the second electrode E**2**. FIG. **4** shows fabricating steps in continuous of the steps in FIG. **2**. Elements which are substantially the same as those in the embodiment of FIG. **4** are denoted by the same reference numerals in FIG. **3**; an accompanying explanation is therefore omitted. As shown in FIG. **4**, a first electrode E**1** and a capacitor dielectric layer I are sequentially formed to cover the trench **18***a* and the top surface of the third silicon-containing material layer **12***c*. Later, a second electrode E**2** is formed to fill up the remaining space of the trench **18***a*. The following steps are the same as those in FIG. **3**, the steps may include patterning the first electrode E**1**, the capacitor dielectric layer I and the second electrode E**2**. The first electrode E**1**, the capacitor dielectric layer I and the second electrode E**2** form the MIM capacitor C**2**. Next, the dielectric layer **26** and contact plugs **28***a*/**28***b* are formed. Now, an MIM capacitor structure **200** with a rounded sidewall of the present invention is completed.

[0024] When the first etching **16***a* is performed in FIG. **1**, numerous trenches **18***a* may also be formed simultaneously. Subsequently, the second etching **16***b* is performed followed by forming the first electrode E**1**, the second electrode E**2** and the capacitor dielectric layer I. In this way, numerous

MIM capacitors can be formed and connected in series. For example, according to the third preferred embodiment of the present invention, as shown in FIG. **5**, the manufacturing process of the MIM capacitor structure **300** with a rounded sidewall includes using the first etching **16***a* to form two trenches **18***a*. Later, a second etching **16***b* is performed. After that, the steps similar to those in FIG. **3** are performed. That is, the first electrode E**1**, the capacitor dielectric layer I, the second electrode E**2** and the insulating layer **24** are formed to fill in the trenches **18***a*. Then, the dielectric layer **26** and contact plugs **28***a*/**28***b* are then formed. The MIM capacitor structure **300** is exemplified as two capacitor connected in series. Elements in FIG. **5** which are substantially the same as those in the embodiment of FIG. **3** are denoted by the same reference numerals; an accompanying explanation is therefore omitted.

[0025] According to a fourth preferred embodiment of the present invention, as shown in FIG. **6**, the fabricating process of an MIM capacitor structure **400** with a rounded sidewall includes performing the first etching **16***a* to form two trenches **18***a*. Later, the second etching **16***b* is performed followed by using the steps in FIG. **4** such as forming the first electrode E**1**, the capacitor dielectric layer I and the second electrode E**2** to form two MIM capacitors C**2**. Next, the dielectric layer **26** and contact plugs **28***a*/**28***b* are formed. Elements in FIG. **6** which are substantially the same as those in the embodiment of FIG. **4** are denoted by the same reference numerals; an accompanying explanation is therefore omitted.

[0026] According to a fifth preferred embodiment of the present invention, as shown in FIG. **7**, an MIM capacitor structure **500** with rounded a sidewall is formed by using the first etching **16***a* illustrated in FIG. **1** to form two trenches **18***a*/**18***b*. Later, the trench **18***a* in the first oxygen-containing silicon compound layer **14***a* and the second oxygen-containing silicon compound layer **14***b* is laterally enlarged by the second etching **16***b* illustrated in FIG. **2**. The second etching **16***b* only etches the trench **18***a*. Later, an additional third etching is performed. The third etching only etches the trench **18***b* in the silicon nitride, poly-crystalline silicon, single-crystalline silicon or amorphous silicon, and does not etch the silicon oxide nor the entire trench **18***a*. In this way, the trench **18***b* in the third silicon-containing material layer **12***c* and the second silicon-containing material layer **12***b* is laterally widen by the third etching and the bottom of the trench **18***b* is also expand toward the first silicon-containing material layer **12***a*. Therefore, the bottom of the trench **18***b* also becomes rounded. The sidewall of the trench **18***b* in the third silicon-containing material layer **12***c* and the second silicon-containing material layer **12***b* are rounded sidewalls **30***c*/**30***b*. After that, the steps similar to those in FIG. **3** are performed. That is, the first electrode E**1**, the capacitor dielectric layer I, the second electrode E**2** and the insulating layer **24** are formed to fill in the trench **18***a* and the trench **18***b*. Then, the dielectric layer **26** and contact plugs **28***a*/**28***b* are formed. In this way, an MIM capacitor C**1** and an MIM capacitor C**3** can be formed. The MIM capacitor C**1** and the MIM capacitor C**3** are connected to each other in series. Elements in FIG. **7** which are substantially the same as those in the embodiment of FIG. **3** are denoted by the same reference numerals; an accompanying explanation is therefore omitted.

[0027] As shown in FIG. **3**, an MIM capacitor structure **100** with a rounded sidewall includes a stacked layer **10**. The stacked layer **10** preferably has no transistor disposed within, and the substrate **1** preferably has no transistors or active devices disposed on it. The MIM capacitor structure **100** with a rounded sidewall is preferably applied on an interposer. For example, the substrate **1** and the stacked layer **10** constitute an interposer, and the MIM capacitor structure **100** with a rounded sidewall is disposed on the stacked layer **10**. The stacked layer **10** includes at least one silicon-containing material layer and at least one oxygen-containing silicon compound layer stacked alternately. The silicon-containing material layer may include a first silicon-containing material layer **12***a*, a second silicon-containing material layer **12***b* and a third silicon-containing material layer **12***c*. The oxygen-containing silicon compound layer may include a first oxygen-containing silicon compound layer **14***a* and a second oxygen-containing silicon compound layer **14***b*. The first oxygen-containing silicon compound layer **14***a*, the second silicon-containing material layer **12***b*, the second oxygen-containing silicon compound layer **14***b* and the third silicon-containing material layer **12***c* are arranged in sequence from bottom to top. The thickness of each of the silicon-containing material layer is preferably 20 to 50 nanometers. The thickness of each of the oxygen-containing silicon compound layer is 1 to 10 times of each of the silicon-containing material layer. The silicon-containing material layer is preferably poly-crystalline silicon, single-crystalline silicon or amorphous silicon. The oxygen-containing silicon compound layer is preferably silicon oxide.

[0028] Please also refer to FIG. **2**. A trench **18***a* is disposed in the stacked layer **10**. The trench **18***a* has rounded sidewalls **20***a*/**20***b* and vertical sidewalls **22***b*/**22***c*. The vertical sidewalls **20***a*/**20***b* are connected to the rounded sidewalls **22***b*/**22***c*. In details, two sidewalls of the trench **18***a* in the first oxygen-containing silicon compound layer **14***a* and the second oxygen-containing silicon compound layer **14***b* are respectively rounded sidewalls **20***a*/**20***b*. Two sidewalls of the trench **18***a* in the second silicon-containing material layer **12***b* are vertical sidewalls **22***b*. Two sidewalls of the trench **18***a* in the third silicon-containing material layer **12***c* are vertical sidewalls **22***c*. Along a horizontal direction X, the rounded sidewalls **20***a*/**20***b* are respectively concave toward the first oxygen-containing silicon compound layer **14***a* and the second oxygen-containing silicon compound layer **14***b*. Because two sidewalls of the trench **18***a* are rounded sidewalls **20***a*/**20***b*, a widen region R**1** is defined between the rounded sidewalls **20***a* in the first oxygen-containing silicon compound layer **14***a*, and a widen region R**2** is defined between the rounded sidewalls **20***b* in the second oxygen-containing silicon compound layer **14***b*. Moreover, an MIM capacitor C**1** is disposed in the trench **18***a* and contacts the trench **18***a*. The MIM capacitor C**1** includes a first electrode E**1**, a capacitor dielectric layer I and a second electrode E**2**. Since the MIM capacitor C**1** conformally fills the trench **18***a*, the MIM capacitor C**1** also has rounded sidewalls **32***a*/**32***b* respectively in the first oxygen-containing silicon compound layer **14***a* and the second oxygen-containing silicon compound layer **14***b*. An insulating layer **24** fills the trench **18***a* and seals up the opening of the trench **18***a*. The air gaps AG**1**/AG**2**/AG**3** are disposed in the insulating layer **24**. The air gaps AG**1**/AG**2** are respectively located in the insulating layer **24** of the widen region R**1** and widen region R**2**. An air gap AG**3** is also disposed in the insulating layer **24** between the vertical sidewalls **22***b*. The air gaps AG**1**/AG**2** connect to the air gap AG**3**. The

multiple relationship between the width W of the opening of the trench **18***a* and the distance D of the lateral expansion of the trench **18***a* mentioned above is to allow the first electrode E**1**, the capacitor dielectric layer I and the second electrode E**2** to cover the trench **18***a* conformally, and the make sure the trench **18***a* sealed up only after the insulating layer **24** completely cover the surface of the second electrode E**2** in the trench **18***a*. Completely covering the surface of the second electrode E**2** in the trench **18***a* by using the insulating layer **24** can protect the second electrode E**2** from oxidation.

[0029] The first electrode E**1** and the second electrode E**2** respectively include tantalum nitride, titanium nitride, tantalum, titanium, aluminum or polycrystalline silicon. The capacitor dielectric layer I includes aluminum oxide, zirconium oxide, barium strontium titanate (BST), lead zirconate titanate (PZT), zirconium silicate ($ZrSiO_4$), hafnium silicon oxide ($HfSiO_2$), hafnium silicon oxynitride (HfSiON), tantalum oxide or a combination of the above materials. The insulating layer **24** is preferably silicon oxide. The thickness of the first electrode E**1** is preferably between 200 and 300 angstroms. The thickness of the second electrode E**2** is preferably between 200 and 300 angstroms, and the thickness of the capacitor dielectric layer I is preferably between 40 and 80 angstroms.

[0030] FIG. **8** shows an MIM capacitor structure with a rounded sidewall according to the sixth preferred embodiment of the present invention. Elements which are substantially the same as those in the embodiment of FIG. **8** are denoted by the same reference numerals in FIG. **3**; an accompanying explanation is therefore omitted. As shown in FIG. **2** and FIG. **8**, an MIM capacitor structure **600** with a rounded sidewall includes a MIM capacitor C**4**, and the insulating layer **24** between the vertical sidewalls **22***b* is solid; therefore there is no air gap is this part of the insulating layer **24**. In this way, the air gaps AG**1**/AG**2** in the widen region R**1** and R**2** are not connected.

[0031] As shown in FIG. **5**, numerous MIM capacitors C**1** can be disposed in the stacked layer **10** and connected in series with each other. In details, there are two MIM capacitors C**1** disposed in the stack layer **10**. The first electrode E**1**, the capacitor dielectric layer I and the second electrode E**2** of the MIM capacitor C**1** on the left extend to the trench **18***a* on the right to serve as the first electrode E**1**, the capacitor dielectric layer I and the second electrode E**2** of the MIM capacitor C**1** on the right.

[0032] As shown in FIG. **2** and FIG. **4**, the difference between the MIM capacitor C**2** and the MIM capacitor C**1** in FIG. **3** is that the first electrode E**1**, the capacitor dielectric layer I and the second electrode E**2** of MIM capacitor C**2** together fill up the widen region R**1**/R**2**; therefore is no insulation layer and no air gap in the MIM capacitor structure **200** with a rounded sidewall.

[0033] FIG. **6** shows two MIM capacitors C**2** disposed in the stacked layer and connected in series. As shown in FIG. **6**, numerous MIM capacitors C**2** can be disposed in the stacked layer **10** and connected to each other in series. In details, there are two MIM capacitors C**2** disposed in the stacked layer **10**. The first electrode E**1**, the capacitor dielectric layer I and the second electrode E**2** of the MIM capacitor C**2** on the left extend to the trench **18***a* on the right to serve as the first electrode E**1**, the capacitor dielectric layer I and the second electrode E**2** of the MIM capacitor C**2** on the right.

[0034] As shown in FIG. **2** and FIG. **7**, an MIM capacitor C**1** and an MIM capacitor C**3** are respectively disposed in trenches **18***a*/**18***b*. Due to the aforementioned second etching **16***b* and third etching, the rounded sidewalls **20***a*/**20***b* of the trench **18***a* and the rounded sidewalls **30***b*/**30***c* of the trench **18***b* are in different material layers. Moreover, the MIM capacitor C**1** and the MIM capacitor C**3** conformally cover the trenches **18***a*/**18***b* respectively; therefore, the rounded sidewalls **32***a*/**32***b* of the MIM capacitor C**1** are respectively in the first oxygen-containing silicon compound layer **14***a* and the second oxygen-containing silicon compound layer **14***b*, and the rounded sidewalls **34***a*/**34***b* of the MIM capacitor C**3** are respectively in the second silicon-containing material layer **12***b* and the third silicon-containing material layer **12***c*. The MIM capacitor C**1** and The MIM capacitor C**3** are connected in series, that is to say, the first electrode E**1**, the capacitor dielectric layer I and the second electrode E**2** of MIM capacitor C**1** extend to the trench **18***b* on the right to serve as the first electrode E**1**, the capacitor dielectric layer I and the second electrode E**2** of MIM capacitor C**3**.

[0035] The present invention uses the second etching to laterally expand the trench in the stacked layer, thereby forming a MIM capacitor structure with a rounded sidewall, which can increase the surface area of the MIM capacitor and thereby increase the capacitance.

[0036] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

What is claimed is:

1. A metal-insulator-metal (MIM) capacitor structure with a rounded sidewall, comprising:

a stacked layer, wherein the stacked layer comprises at least a silicon-containing material layer and at least one oxygen-containing silicon compound layer stacked alternately;

a trench disposed in the stacked layer, wherein the trench has a rounded sidewall and a vertical sidewall, and the vertical sidewall and the rounded sidewall are connected to each other;

an MIM capacitor disposed in the trench and contacting the trench;

an insulating layer filling in the trench and sealing up an opening of the trench;

and

an air gap disposed in the insulating layer.

2. The MIM capacitor structure with a rounded sidewall of claim **1**, wherein along a horizontal direction parallel to a top surface of the stacked layer, the rounded sidewall is concave toward the stacked layer.

3. The MIM capacitor structure with a rounded sidewall of claim **2**, wherein the vertical sidewall is perpendicular to the horizontal direction.

4. The MIM capacitor structure with a rounded sidewall of claim **1**, wherein the rounded sidewall is disposed in the oxygen-containing silicon compound layer, and the vertical sidewall is disposed in the silicon-containing material layer.

5. The MIM capacitor structure with a rounded sidewall of claim **4**, wherein the oxygen-containing silicon compound layer is silicon oxide, and the silicon-containing material layer is silicon nitride.

6. The MIM capacitor structure with a rounded sidewall of claim **4**, wherein the oxygen-containing silicon compound layer is silicon oxide, and the silicon-containing material layer is poly-crystalline silicon, single-crystalline silicon or amorphous silicon.

7. The MIM capacitor structure with a rounded sidewall of claim **1**, wherein there is no transistor in the stacked layer.

8. The MIM capacitor structure with a rounded sidewall of claim **1**, wherein the rounded sidewall defines a widen region in the trench, and the air gap is disposed in the insulating layer within the widen region.

9. A fabricating method of a metal-insulator-metal (MIM) capacitor structure with a rounded sidewall, comprising:

providing an oxygen-containing silicon compound layer and a silicon-containing material layer;

performing a first etching to etch the oxygen-containing silicon compound layer and the silicon-containing material layer to form a trench;

performing a second etching to etch the oxygen-containing silicon compound layer to laterally expand a portion of a sidewall of the trench to form a rounded sidewall;

after forming the rounded sidewall, forming an MIM capacitor to fill in and contact the trench; and

after forming the MIM capacitor, forming an insulating layer to fill the trench and seal up the opening of the trench, wherein the insulating layer defines an air gap.

10. The fabricating method of an MIM capacitor structure with a rounded sidewall of claim **9**, wherein the second etching selectively etches silicon oxide.

11. The fabricating method of an MIM capacitor structure with a rounded sidewall of claim **9**, wherein the second etching comprises a wet etching.

12. The fabricating method of an MIM capacitor structure with a rounded sidewall of claim **9**, wherein the silicon-containing material layer comprises poly-crystalline silicon, single-crystalline silicon, amorphous silicon or silicon nitride.

13. The fabricating method of an MIM capacitor structure with a rounded sidewall of claim **9**, wherein along a horizontal direction parallel to a top surface of the oxygen-containing silicon compound layer, the rounded sidewall is concave toward the oxygen-containing silicon compound layer.

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