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(54) **SYSTEMS AND METHODS FOR ON-CHIP NOISE MEASUREMENTS**

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None
See application file for complete search history.

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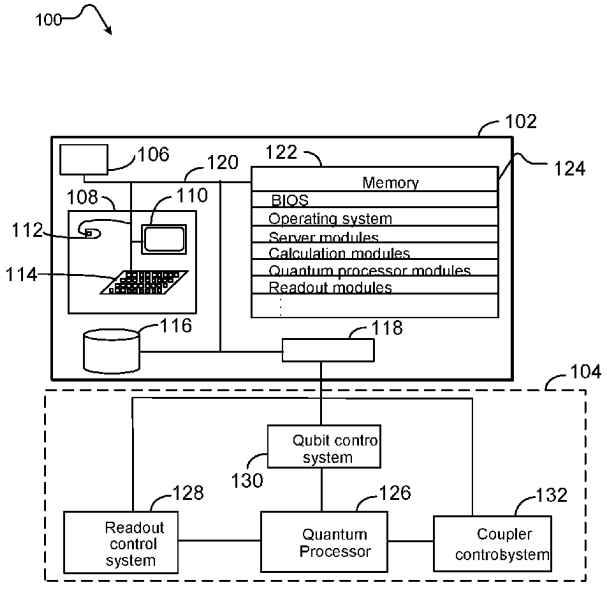
(57) **ABSTRACT**

Systems and methods for measuring noise in discrete regions of multi-layer superconducting fabrication stacks are described. Methods for measuring noise in spatial regions of a superconducting fabrication stacks may include the use of resonators, each having a different geometry. As many resonators as spatial regions are fabricated. Data collected from the resonators may be used to calculate fill fractions and spin densities for different spatial regions of the superconducting fabrication stack. The data may be collected via on-chip electron-spin resonance. The superconducting fabrications may be part of a fabrication stack for a superconducting processor, for example a quantum processor, and the spatial region studied may be proximate to qubit wiring layers.

**18 Claims, 4 Drawing Sheets**



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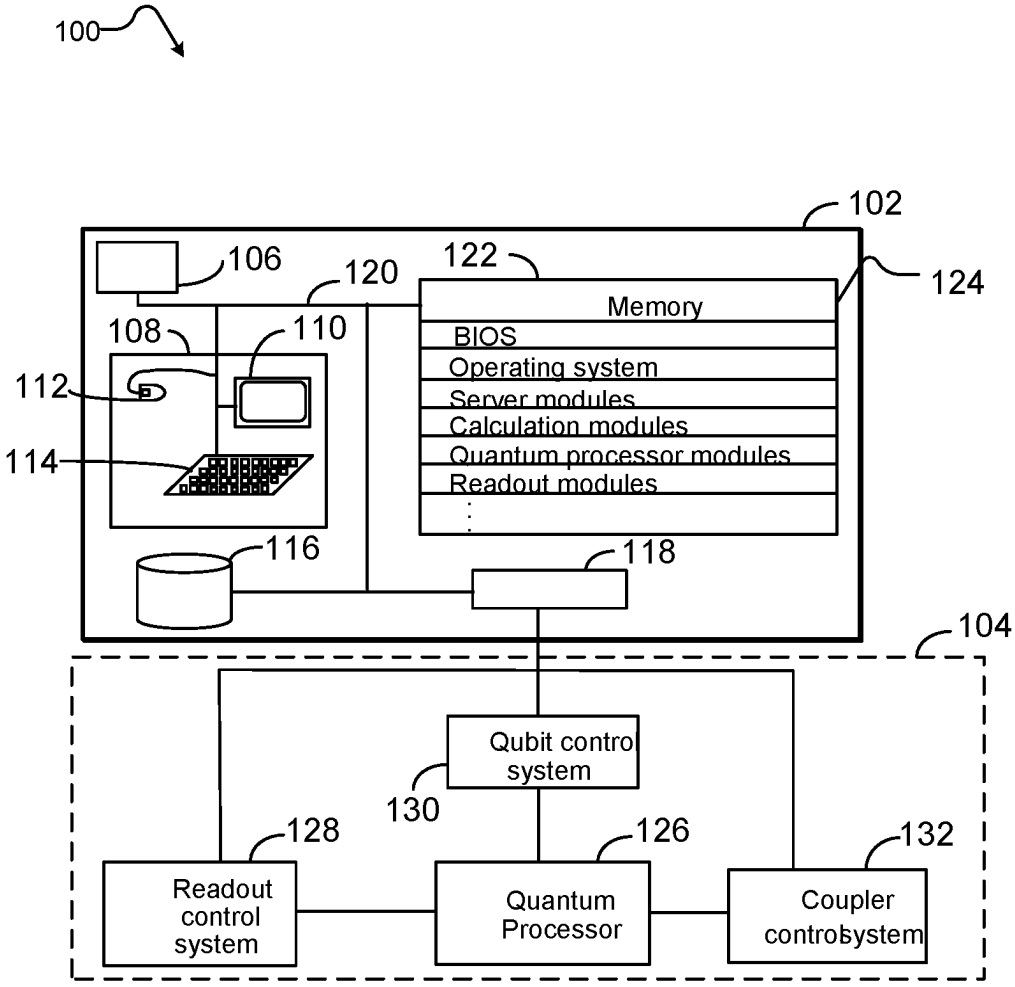
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Coupler control system

FIGURE 1

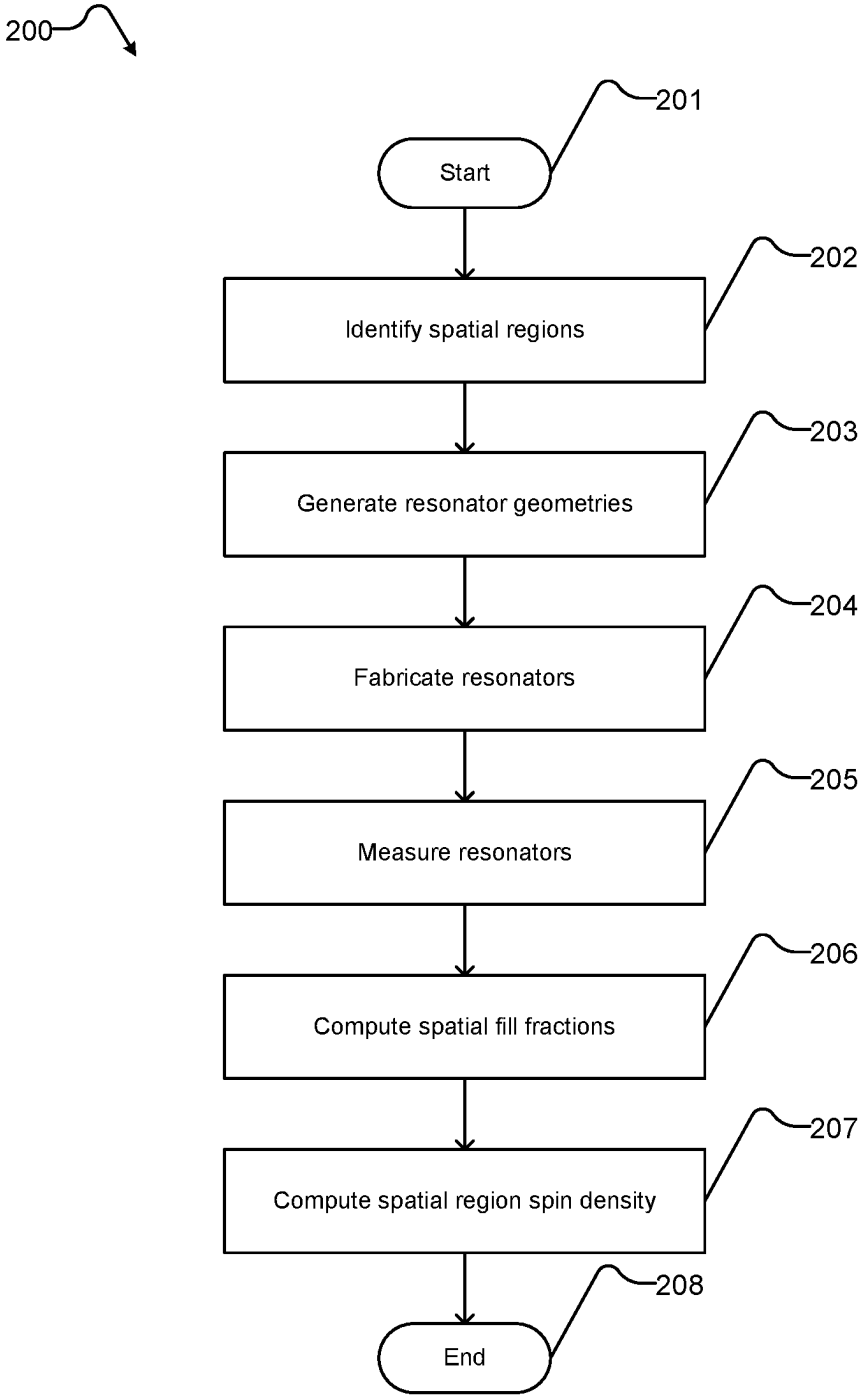
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FIGURE 2

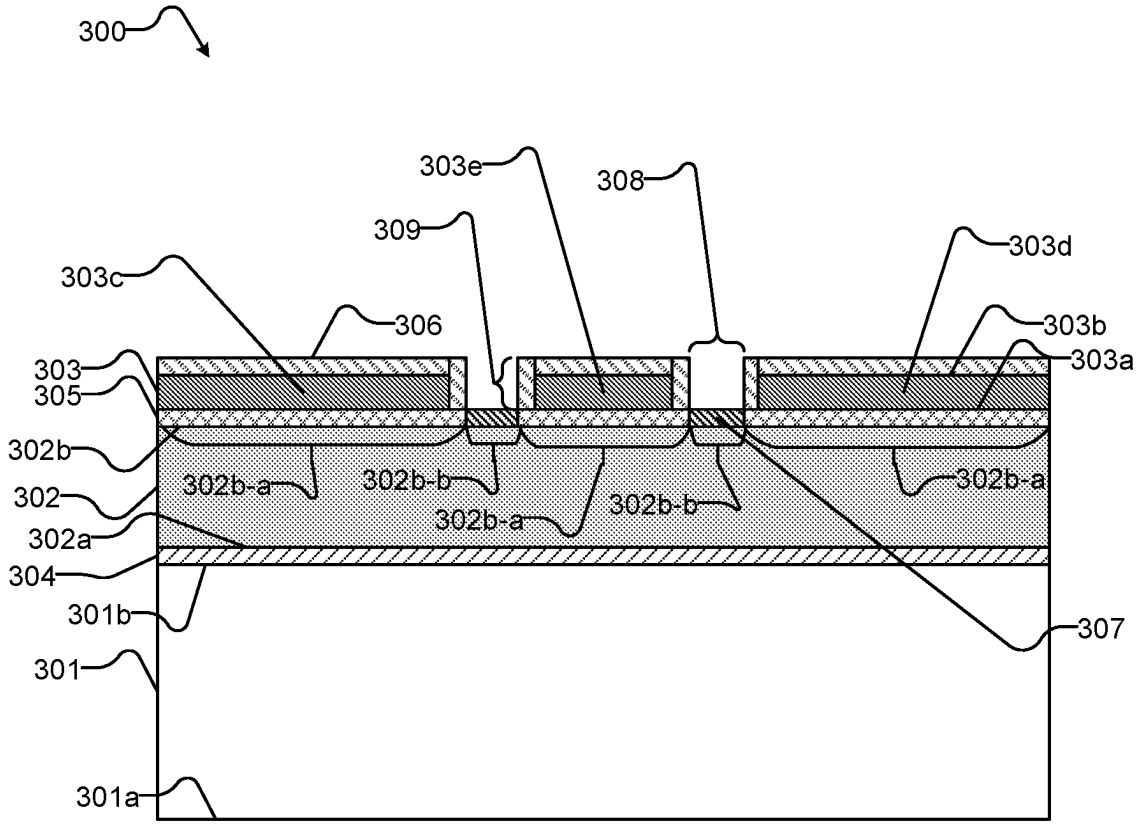
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FIGURE 3

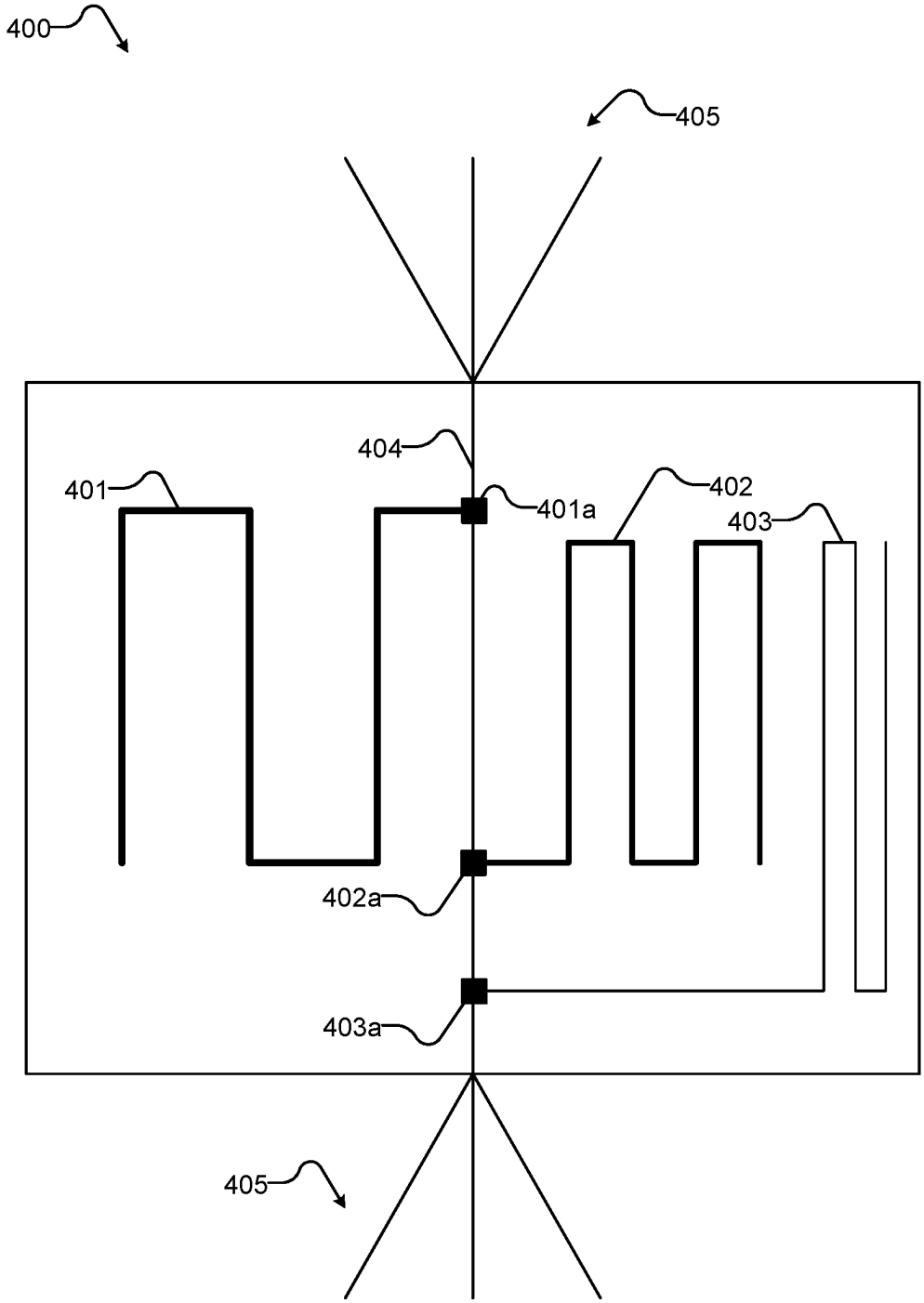


FIGURE 4

# SYSTEMS AND METHODS FOR ON-CHIP NOISE MEASUREMENTS

## FIELD

This disclosure generally relates to systems and methods for measuring noise in discrete regions of multi-layer superconducting integrated circuits.

## BACKGROUND

Superconducting Processor

A quantum processor may take the form of a superconducting processor. However, superconducting processors can include processors that are not intended for quantum computing. For instance, some embodiments of a superconducting processor may not focus on quantum effects such as quantum tunneling, superposition, and entanglement but may rather operate by emphasizing different principles, such as for example the principles that govern the operation of classical computer processors. However, there may still be certain advantages to the implementation of such superconducting "classical" processors. Due to their natural physical properties, superconducting classical processors may be capable of higher switching speeds and shorter computation times than non-superconducting processors, and therefore it may be more practical to solve certain problems on superconducting classical processors. The present articles and methods are particularly well-suited for use in fabricating both superconducting quantum processors and superconducting classical processors.

Superconducting Qubits

Superconducting qubits are a type of superconducting quantum device that can be included in a superconducting integrated circuit. Superconducting qubits can be separated into several categories depending on the physical property used to encode information. For example, superconducting qubits may be separated into charge, flux and phase devices. Charge devices store and manipulate information in the charge states of the device. Flux devices store and manipulate information in a variable related to the magnetic flux through some part of the device. Phase devices store and manipulate information in a variable related to the difference in superconducting phase between two regions of the device. Recently, hybrid devices using two or more of charge, flux and phase degrees of freedom have been developed. Superconducting qubits commonly include at least one Josephson junction. A Josephson junction is a small interruption in an otherwise continuous superconducting current path and is typically realized by a thin insulating barrier sandwiched between two superconducting electrodes. Thus, a Josephson junction may be implemented as a three-layer or "trilayer" structure. Superconducting qubits are further described in, for example, U.S. Pat. Nos. 7,876,248, 8,035,540, and 8,098,179.

Integrated Circuit Fabrication

Superconducting integrated circuits are often fabricated with tools that are traditionally used to fabricate semiconductor chips or integrated circuits. Due to issues unique to superconducting circuits, not all semiconductor processes and techniques are necessarily transferrable to superconductor chip manufacture. Transforming semiconductor processes and techniques for use in superconductor chip and circuit fabrication often requires changes and fine adjustments. Such changes and adjustments typically are not obvious and may require a great deal of experimentation. The semiconductor industry faces problems and issues not necessarily related to the superconducting industry. Likewise, problems and issues that concern the superconducting industry are often of little or no concern in standard semiconductor fabrication.



Any impurities within superconducting chips may result in noise which can compromise or degrade the functionality of the individual devices, such as superconducting qubits, and of the superconducting chip as a whole. Since noise is a serious concern to the operation of quantum computers, measures should be taken to reduce noise wherever possible.

Hamiltonian Description of a Quantum Processor

In accordance with some embodiments of the present articles and methods, a quantum processor may be designed to perform adiabatic quantum computation and/or quantum annealing. A common problem Hamiltonian includes first component proportional to diagonal single qubit terms and a second component proportional to diagonal multi-qubit terms. The problem Hamiltonian, for example, may be of the form:

$$H_P \propto -\frac{\varepsilon}{2}\left[\sum_{i=1}^{N} h_i \sigma_i^z + \sum_{ji}^{N} J_{ij} \sigma_i^z \sigma_j^z\right]$$

where N represents the number of qubits, $\sigma_i^z$ is the Pauli z-matrix for the $i^{th}$ qubit, $h_i$ and are dimensionless local fields for the qubits, and couplings between qubits, and $\varepsilon$ is some characteristic energy scale for Hp. Here, the $\sigma_i^z$ and $\sigma_i^z o_j^z$ terms are examples of "diagonal" terms. The former is a single qubit term and the latter a two qubit term. Hamiltonians may be physically realized in a variety of different ways, for example, by an implementation of superconducting qubits.

Noise in a Quantum Processor

Low-noise is a desirable characteristic of quantum devices. Noise can compromise or degrade the functionality of the individual devices, such as superconducting qubits, and of the superconducting processor as a whole. Noise can negatively affect qubit coherence and reduce the efficacy of qubit tunneling. Since noise is a serious concern to the operation of quantum processors, measures should be taken to reduce noise wherever possible so that a transition from coherent to incoherent tunneling is not induced by the environment.

Impurities may be deposited on the metal surface and/or may arise from an interaction with the etch/photoresist chemistry and the metal. Noise can be caused by impurities on the upper surface of the quantum processor. In some cases, superconducting devices that are susceptible to noise are fabricated in the top wiring layers of a superconducting integrated circuit and are thus sensitive to post-fabrication handling. There is a risk of introducing impurities that cause noise during post-fabrication handling. One approach to reducing noise is using a barrier passivation layer, for example, an insulating layer, to overlie the topmost wiring layer. The use of a barrier passivation layer to minimize noise from impurities on the upper surface of a quantum processor is described in US Patent Application No. Publication 2018/02219150A1.

Noise can also result from an external environment or surrounding circuitry in a superconducting processor. In a quantum processor, flux noise on qubits interferes with properly annealing the quantum processor because of the steep transition between qubit states as the flux bias is swept. Flux noise can be a result of current flowing through wiring of other devices included in the superconducting processor

and can have a particularly negative effect on qubits at their respective degeneracy points. For example, flux noise can introduce errors in calculations carried out by the superconducting processor due to inaccuracies in setting flux bias and coupling strength values. Reducing or even eliminating such inaccuracies may be particularly advantageous in using an integrated circuit as part of a quantum processor. Much of the static control error can be designed out of the processor with careful layout and high-precision flux sources, as well as by adding circuitry, such as an on-chip shield, to tune away any non-ideal flux qubit behavior. However, in many cases, limitations in integrated circuit fabrication capabilities can make it difficult to address noise by changing processor layout and adding circuitry. There is therefore a general desire for articles and methods for fabricating integrated circuits that have reduced flux noise (and thus improved coherence) without having to compromise the quantum processor layout by adding additional layers or circuitry.

The foregoing examples of the related art and limitations related thereto are intended to be illustrative and not exclusive. Other limitations of the related art will become apparent to those of skill in the art upon a reading of the specification and a study of the drawings.

## BRIEF SUMMARY

A method of conducting spatial noise measurements in a superconducting fabrication stack is described. The superconducting fabrication stack comprises one or more material interfaces. The method comprising: identifying one or more spatial regions of the superconducting fabrication stack; generating a plurality of resonator geometries; fabricating a plurality of resonators on the superconducting fabrication stack, each resonator of the plurality of resonators having a respective one of the plurality of resonator geometries; measuring data from the plurality of resonators; calculating fill fractions for the one or more spatial regions of the superconducting fabrication stack based on the data measured from the plurality of resonators; and determining a spin density for each spatial region of the one or more spatial regions of the superconducting fabrication stack based on the data measured from the plurality of resonators and the calculated fill fractions. Measuring data from the plurality of resonators comprises measuring spectra of each resonator in the plurality of resonators using on-chip electron-spin resonance (cESR). The resonators may be coplanar waveguide resonators. Each resonator has a respective resonance frequency. The method may further comprise measuring the resonator geometries via scanning electron microscope (SEM) after fabricating the plurality of resonators. As many resonator geometries are generated as identified spatial regions. The one or more spatial regions comprise at least one of: niobium, aluminum, tantalum, niobium nitride, titanium nitride, or niobium titanium nitride. The one or more spatial regions comprise at least the one or more material interfaces. Resonators are fabricated on a metal layer overlying a dielectric layer in the superconducting fabrication stack. Resonators may be etched on a metal layer overlying a dielectric layer in the superconducting fabrication stack.

## BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S)

In the drawings, identical reference numbers identify similar elements or acts. The sizes and relative positions of elements in the drawings are not necessarily drawn to scale. For example, the shapes of various elements and angles are not necessarily drawn to scale, and some of these elements may be arbitrarily enlarged and positioned to improve drawing legibility. Further, the particular shapes of the elements as drawn, are not necessarily intended to convey any information regarding the actual shape of the particular elements and may have been solely selected for ease of recognition in the drawings.

FIG. **1** is a schematic diagram that illustrates a computing system comprising a digital computer and an analog computer that includes a superconducting integrated circuit, in accordance with the present systems and methods.

FIG. **2** is a flowchart that illustrates an example method of measuring noise in discrete regions of a multi-layer superconducting integrated circuit, in accordance with the present systems and methods.

FIG. **3** is a schematic diagram of a cross section of a superconducting fabrication stack that includes resonators to measure noise in discrete regions of the fabrication stack.

FIG. **4** is a plan view of a superconducting fabrication stack that includes a plurality of resonators, each resonator having a different geometry.

## DETAILED DESCRIPTION

In the following description, certain specific details are set forth in order to provide a thorough understanding of various disclosed implementations. However, one skilled in the relevant art will recognize that implementations may be practiced without one or more of these specific details, or with other methods, components, materials, etc. In other instances, well-known structures associated with computer systems, digital computer systems, analog computer systems, and/or fabrication equipment have not been shown or described in detail to avoid unnecessarily obscuring descriptions of the implementations.

Unless the context requires otherwise, throughout the specification and claims that follow, the word "comprising" is synonymous with "including," and is inclusive or open-ended (i.e., does not exclude additional, unrecited elements or method acts).

Reference throughout this specification to "one implementation" or "an implementation" means that a particular feature, structure or characteristic described in connection with the implementation is included in at least one implementation. Thus, the appearances of the phrases "in one implementation" or "in an implementation" in various places throughout this specification are not necessarily all referring to the same implementation. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more implementations.

As used in this specification and the appended claims, the singular forms "a," "an," and "the" include plural referents unless the context clearly dictates otherwise. It should also be noted that the term "or" is generally employed in its sense including "and/or" unless the context clearly dictates otherwise.

The headings and Abstract of the Disclosure provided herein are for convenience only and do not interpret the scope or meaning of the implementations.

Hybrid Quantum Computing Systems

FIG. **1** illustrates a computing system **100** comprising a digital computer **102**. The example digital computer **102** includes one or more digital processors **106** that may be used to perform classical digital processing tasks. Digital computer **102** may further include at least one system memory

122, and at least one system bus 120 that couples various system components, including system memory 122 to digital processor(s) 106. System memory 122 may store one or more sets of processor-executable instructions, which may be referred to as modules 124.

The digital processor(s) 106 may be any logic processing unit or circuitry (for example, integrated circuits), such as one or more central processing units ("CPUs"), graphics processing units ("GPUs"), digital signal processors ("DSPs"), application-specific integrated circuits ("ASICs"), programmable gate arrays ("FPGAs"), programmable logic controllers ("PLCs"), etc., and/or combinations of the same.

In some implementations, computing system 100 comprises an analog computer 104, which may include one or more quantum processors 126. Quantum processor 126 may include at least one superconducting integrated circuit. Digital computer 102 may communicate with analog computer 104 via, for instance, a controller 118. Certain computations may be performed by analog computer 104 at the instruction of digital computer 102, as described in greater detail herein.

Digital computer 102 may include a user input/output subsystem 108. In some implementations, the user input/output subsystem includes one or more user input/output components such as a display 110, mouse 112, and/or keyboard 114.

System bus 120 may employ any known bus structures or architectures, including a memory bus with a memory controller, a peripheral bus, and a local bus. System memory 122 may include non-volatile memory, such as read-only memory ("ROM"), static random-access memory ("SRAM"), Flash NAND; and volatile memory such as random-access memory ("RAM") (not shown).

Digital computer 102 may also include other non-transitory computer- or processor-readable storage media or non-volatile memory 116. Non-volatile memory 116 may take a variety of forms, including: a hard disk drive for reading from and writing to a hard disk (for example, a magnetic disk), an optical disk drive for reading from and writing to removable optical disks, and/or a solid state drive (SSD) for reading from and writing to solid state media (for example NAND-based Flash memory). Non-volatile memory 116 may communicate with digital processor(s) via system bus 120 and may include appropriate interfaces or controllers 118 coupled to system bus 120. Non-volatile memory 116 may serve as long-term storage for processor- or computer-readable instructions, data structures, or other data (sometimes called program modules or modules 124) for digital computer 102.

Although digital computer 102 has been described as employing hard disks, optical disks and/or solid-state storage media, those skilled in the relevant art will appreciate that other types of non-transitory and non-volatile computer-readable media may be employed. Those skilled in the relevant art will appreciate that some computer architectures employ non-transitory volatile memory and non-transitory non-volatile memory. For example, data in volatile memory may be cached to non-volatile memory or a solid-state disk that employs integrated circuits to provide non-volatile memory.

Various processor- or computer-readable and/or executable instructions, data structures, or other data may be stored in system memory 122. For example, system memory 122 may store instructions for communicating with remote clients and scheduling use of resources including resources on the digital computer 102 and analog computer 104. Also, for example, system memory 122 may store at least one of processor executable instructions or data that, when executed by at least one processor, causes the at least one processor to execute the various algorithms to execute instructions. In some implementations system memory 122 may store processor- or computer-readable calculation instructions and/or data to perform pre-processing, co-processing, and post-processing to analog computer 104. System memory 122 may store a set of analog computer interface instructions to interact with analog computer 104. For example, the system memory 122 may store processor- or computer-readable instructions, data structures, or other data which, when executed by a processor or computer causes the processor(s) or computer(s) to execute one, more or all of the acts of method 200 of FIG. 2.

Analog computer 104 may include at least one analog processor such as quantum processor 126. Analog computer 104 may be provided in an isolated environment, for example, in an isolated environment that shields the internal elements of the quantum computer from heat, magnetic field, and other external noise. The isolated environment may include a refrigerator, for instance a dilution refrigerator, operable to cryogenically cool the analog processor, for example to temperature below approximately 1 K.

Analog computer 104 may include programmable elements such as qubits, couplers, and other devices (also referred to herein as controllable devices). Qubits may be read out via readout system 128. Readout results may be sent to other computer- or processor-readable instructions of digital computer 102. Qubits may be controlled via a qubit control system 130. Qubit control system 130 may include on-chip Digital to Analog Converters (DACs) and analog lines that are operable to apply a bias to a target device. Couplers that couple qubits may be controlled via a coupler control system 132. Coupler control system 132 may include tuning elements such as on-chip DACs and analog lines. Qubit control system 130 and coupler control system 132 may be used to implement a quantum annealing schedule on analog computer 104. Programmable elements may be included in quantum processor 126 in the form of an integrated circuit. Qubits and couplers may be positioned in layers of the integrated circuit that comprise a first material. Other devices, such as readout control system 128, may be positioned in other layers of the integrated circuit that comprise a second material. In accordance with the present disclosure, a quantum processor, such as quantum processor 126, may be designed to perform quantum annealing and/or adiabatic quantum computation. Examples of quantum processors are described in U.S. Pat. No. 7,533,068.

Various respective systems, components, structures and algorithms for implementing such are described herein. Many of the described systems, components, structures and algorithms may be implemented individually, while some may be implemented in combination with one another.

A quantum processor may require a local bias to be applied on a qubit to implement a problem Hamiltonian. The local bias applied on the qubit depends on persistent current $I_P$ and external flux bias $\phi_q$ as described below:

$$\delta h_i = 2|I_P|\delta\phi_q$$

Noise affects the local bias $\delta h_i$ in the same way as the external flux bias $\phi_q$ and thus changes the specification of the qubit terms in the problem Hamiltonian. Noise may introduce errors into the computational result from quantum annealing by altering the problem Hamiltonian.

Throughout the present specification, the phrase 'noise-susceptible device' is used to describe a device for which noise may adversely affect the proper performance in a

quantum processor. Poor performance of a noise-susceptible device may result in the quantum processor producing inaccurate or suboptimal solutions to a problem. For example, a qubit may be considered a noise-susceptible device or device that is susceptible to noise because noise on the qubits may interfere with properly annealing the quantum processor and/or can lead to a different problem being solved. Note that the phrase "noise-susceptible" or "susceptible to noise" does not necessarily suggest that the device itself is physically more or less sensitive to noise compared to other devices that are not described as noise-susceptible. Sensitivities to processor performance is higher in noise-susceptible devices relative to devices that are described as less susceptible to noise.

Noise in a quantum processor may cause qubits to decohere which reduces the efficacy of tunneling. As a result, processor performance may be diminished, and solutions generated from the processor may be suboptimal.

Performance of a superconducting processor can be directly impacted by the performance of certain superconducting devices that are susceptible to noise, for example, qubits and couplers. Since processor performance is particularly sensitive to the outcomes of operation of these devices, it is desirable to reduce noise in these devices as much as possible. For a superconducting processor, one of the dominant sources of environmental noise is flux noise. Flux noise is thought to be a stochastic process generated by magnetic defects, or magnetic spins, in materials. These may also be referred to as "spin defects". Flux noise may cause decoherence which induces a transition from coherent to incoherent tunneling before intrinsic phase transitions can be induced by processor dynamics (e.g., from a programmed problem). Device decoherence during computation may limit accuracy with which the processor evolves and produces solutions. Additionally, flux noise may increase the susceptibility of a processor to spin bath polarization which is a "memory" effect that results in diminished sampling and optimization performance. Systems and methods to reduce spin bath polarization are described in U.S. Pat. No. 11,295,225.

Therefore, in many implementations, it is beneficial to understand the origin of various types of noise in a materials stack. For instance, in a fabrication stack, the dominant noise may be flux noise that originates from one or more of spin defects in the wires, the wire-dielectric interface, or the dielectric material. In order to determine the source of this flux noise, it can be beneficial to spatially identify the layers or interfaces having high-defect densities (e.g., spin defects) before investing significant resources on fabrication development in an effort to reduce noise. In an example implementation of the development of a fabrication stack for a quantum processor, it is advantageous to resolve the source of noise from among noise in a dielectric, noise at the surface of wiring, or noise at the interfaces between wiring and dielectric regions.

A spin density for a system can be determined by forming a single superconducting micro resonator and performing electron spin resonance (ESR) at milli-Kelvin temperatures. Methods, systems, and apparatus discussed herein provide for measuring on-chip electron spin resonance (cESR) spectrum on several resonators with different geometries and analyzing the data to extract the spin density for each region. This can beneficially allow for distinguishing noise parameters of different regions, and in particular noise parameters of different materials and interfaces. In the present disclosure and the appended claims, the terms 'resonator geometry' or 'resonator geometries' are used to define any change in a resonator that will alter a magnetic field distribution in the material system. An example of changing a resonator geometry is altering the cross section (e.g., the width between the ground plates and the center conductor of a resonator, or the width of the center conductor). Another example of a resonator geometry change is etching trenches of different depths between the center conductor and the ground plates. Resonators will operate at a characteristic frequency that is determined by the resonator geometry. By providing a set or plurality of resonators, each having a different resonator geometry, the signals from each resonator can be distinguished. That is, each resonator will provide a distinct signal as it has a different characteristic frequency.

Development of multi-layer fabrication stacks is a complex process having a landscape of variables, the values of which can be adjusted towards the goal of achieving lower noise processors, and thereby more performant processors, and, preferably, more accurate computation performed by quantum processors. Some of these variables include the number of layers within a fabrication stack, the thickness of relative layers, the material of each layer, and the material interfaces between layers. These variables may be interrelated, and a trial and error approach in fabrication can be costly and time consuming. While factors such as paramagnetic defect density in a given dielectric may be thought to be a source of noise, it may be the case that spin defects in the metal layers (e.g., conductive traces or wires) or at material interfaces (e.g., wire-dielectric interfaces) dominate the noise. The methods, systems, and apparatuses described herein can beneficially characterize high defect densities in spatial regions to determine dominate sources of noise, which in turn can provide more efficient fabrication processes. In particular, measuring cESR spectrum on several resonators with different geometries allows for extracting spatially-resolved spin densities. This in turn allows for differentiation in noise between different portions of a fabrication stack.

An example superconducting fabrication stack comprises a substrate, a dielectric, and a superconductor. The superconducting fabrication stack may be used to design a superconducting integrated circuit, for example a superconducting processor (e.g., a superconducting quantum processor comprising qubits and couplers). Examples of superconducting fabrication stacks are discussed in FIGS. **3** and **4**. The systems and methods described in the present disclosure use co-planar waveguide (CPW) resonators of several different geometries measured at milli-kelvin temperature with and without the presence of a large magnetic field.

Charge Noise Measurements with Co-Planar Waveguide (CPW) Resonators

One method that has been used to understand noise in superconducting integrated circuits was first developed at NASA's Jet Propulsion Laboratory; see J. Gao et al., "Experimental evidence for a surface distribution of two-level systems in superconducting lithographed microwave resonators," *Appl. Phys. Lett.*, vol. 92, 2008. The method requires CPW resonators and involves varying the CPW center trace width, $s_r$, and ground plane gap, $g_r$, to extract the amount of loss in the bulk substrate dielectric, the metal-substrate interface, the metal-vacuum interface, and the substrate-vacuum interface. This method was further demonstrated at MIT using Titanium Nitride (TiN) on high-resistivity c-Silicon wafers; see G. Calusine et al., "Analysis and mitigation of interface losses in trenched superconducting coplanar waveguide resonators," *Appl. Phys. Lett.*, vol 112, 2018 and W. Woods et al., "Determining interface dielectric losses in superconducting coplanar waveguide

resonators," *Phys. Rev. Applied,* 12, 2019. In these demonstrations, the $s_r/g_r$ ratio was kept constant, and etched trenches of different depths in the gaps to vary the geometry further. By using electro-magnetic (EM) field analysis they calculated the spatial variation of the electric and magnetic fields. The field distribution can be used to calculate the electric field fill fraction $F_{region}$ for a given region, also called the 'fill factor' or 'filling factor':

$$F_{region} = \frac{U_{region}}{U_{total}} = \frac{\int_{V_{region}} \varepsilon_{region} \vec{E}^2(\vec{r}) d\vec{r}}{\int_{V_{total}} \varepsilon_{effective} \vec{E}^2(\vec{r}) d\vec{r}} \quad (1)$$

where U is the electric field energy, V is the volume, $\epsilon$ is the dielectric constant, E is the electric field and r is the vector in space. As such, the fill fraction can be thought of as the proportion of the electrical energy that is stored in a given region.

By fitting to models of how each region's fill fraction changes with each geometry variation, Woods et al. were able to resolve each of these different interfaces (silicon substrate (Si), metal substrate interface (MS), substrate air (SA), and metal air (MA)) and provide a loss tangent (tan δ) for each. Woods et al. used modeling to calculate the fill fraction Frey ion for each region in each geometry, where Equation 2 is the form of one equation for one geometry in a system of linear equations that can be solved, given enough geometry variations.

$$\tan\delta_{measured} = F_{Si}\tan\delta_{Si} + F_{MS}\tan\delta_{MS} + F_{SA}\tan\delta_{SA} + F_{MA}\tan\delta_{MA} \quad (2)$$

Calusine et al. used seven different trench depths and five different geometries, providing more than enough geometry variation to extract their four unknowns in Equation 2. Calusine et al. measured sixty devices on twelve chips and obtained statistical results via Monte Carlo error analysis.

In contrast with the above, it may be beneficial to measure flux or parametric defect noise for different spatial regions of a fabrication stack in order to better select materials for fabricating superconducting integrated circuits such as quantum processors. The following is a demonstrative example: if one builds four resonators, labeled R1 through R4, with different geometries on the same chip and measures the loss tangent of each resonator $\tan\delta_{measured}^{R}$ (where R is a label for each resonator), then models the fill fractions $F_{region}^{R}$ for each region for each geometry using Equation 2 one will end up with the following set of equations:

$$\tan\delta_{measured}^{R1} = F_{Si}^{R1}\tan\delta_{Si} + F_{MS}^{R1}\tan\delta_{MS} + F_{SA}^{R1}\tan\delta_{SA} + F_{MA}^{R1}\tan\delta_{MA}$$

$$\tan\delta_{measured}^{R2} = F_{Si}^{R2}\tan\delta_{Si} + F_{MS}^{R2}\tan\delta_{MS} + F_{SA}^{R2}\tan\delta_{SA} + F_{MA}^{R2}\tan\delta_{MA}$$

$$\tan\delta_{measured}^{R3} = F_{Si}^{R3}\tan\delta_{Si} + F_{MS}^{R3}\tan\delta_{MS} + F_{SA}^{R3}\tan\delta_{SA} + F_{MA}^{R3}\tan\delta_{MA}$$

$$\tan\delta_{measured}^{R4} = F_{Si}^{R4}\tan\delta_{Si} + F_{MS}^{R4}\tan\delta_{MS} + F_{SA}^{R4}\tan\delta_{SA} + F_{MA}^{R4}\tan\delta_{MA}$$

From measurements one knows all the $\tan\delta_{measured}^{R}$ for each region of the four resonators, so one has four equations and four unknowns that will allow for the four loss tangents $\tan\delta_{region}$ to be solved.

It is advantageous in processor design to ensure the CPW resonator geometries studied have diverse enough fill fractions in each region to ensure that the regions can be clearly separated.

Flux Noise Measurements

The present disclosure applies the fill fraction method outlined above for flux/paramagnetic defect noise measurements instead of charge/Two-Level System (TLS) noise measurements. The present systems and methods employ superconducting CPW resonators of several different geometries measured using on-chip electron spin resonance (cESR).

ESR at room temperature may be used to study paramagnetic defects in deposited dielectric films. In some implementations, such dielectric films may be deposited on high-resistivity crystalline Silicon (c-Si) substrates because, if native Silicon Oxide ($SiO_x$) is removed (e.g., etched off) from the substrate before measurement, such a substrate has very low paramagnetic defect density. In another implementation, sapphire (c-Al2O3) is used as a material for a substrate over which a dielectric is deposited. A material sample to be measured is loaded into a metal cavity of a standard ESR measurement apparatus and then placed in a large, slowly swept magnetic field $B_0$. The sample is placed such that driving the microwave cavity generates a field $B_1$ perpendicular to $B_0$, and when given a paramagnetic defect splitting (a Zeeman splitting due to $B_0$) comes into resonance with the cavity, its quality factor Q changes and can be detected.

The signal expected from an ESR measurement also includes a magnetic field fill fraction η. The ESR signal voltage for a Bruker-type machine is $V_s = \chi'' \eta Q \sqrt{PZ_0}$, where χ" is the magnetic susceptibility of the material under test, Q is the resonator quality factor, P is the microwave drive power, and $Z_0$ is the system impedance (e.g., typically 50Ω). The magnetic field fill fraction η for a given region is the magnetic field energy in that region ($U_{region}$) over the total magnetic field energy in the resonator ($U_{total}$):

$$\eta_{region} = \frac{U_{region}}{U_{total}} = \frac{\int_{V_{region}} \frac{1}{\mu_{region}} \vec{B}^2(\vec{r}) d\vec{r}}{\int_{V_{total}} \frac{1}{\mu_{effective}} \vec{B}^2(\vec{r}) d\vec{r}} \quad (4)$$

where B is the magnetic field, and μ is magnetic permeability and depends on the magnetic susceptibility χ:

$$\mu = \mu_0(1 + \chi_0) = \mu_0\left(1 + \chi''\frac{(\Delta\omega)}{\omega}\right) \quad (5)$$

where ω is the drive frequency.

The magnetic susceptibility χ can further be broken down into an expression that is based on the spin density $N_0$:

$$\chi'' = \frac{\gamma\hbar\mu_0}{4k_B}\frac{N_0}{T}\frac{\omega}{\Delta\omega} = 7.84\times10^{-30}\frac{N_0}{T}\frac{\omega}{\Delta\omega} \quad (6)$$

where T is temperature, γ is the electron gyromagnetic ratio, $\mu_0$ is magnetic permeability of free space, h is the reduced Planck constant and $k_b$ is the Boltzmann constant. Plugging Equation 6 into Equation 5 gives an expression for μ in terms of spin density:

$$\mu = \mu_0\left[1 + 7.84\times10^{-30}\frac{N_0}{T}\right] = \mu_0\left[1 + \alpha\frac{N_0}{T}\right] \quad (7)$$

Where $\alpha$ is a constant. This implies having to know $N_0$ to calculate $\mu$ for fill fraction simulation. Assuming $N_0=1\times10^{15}$ $cm^{-3}=1\times10^{21}$ $m^{-3}$ and T=0.01 K in Equation 8:

$$\mu=\mu_0\left[1+7.84\times10^{-30}\frac{1\times10^{21}}{0.01}\right]=\mu_0\left[1+7.84\times10^{-7}\right]\sim\mu_0 \tag{8}$$

Since many dielectrics seem to have $N_0$ in the range $[1\times10^{15},1\times10^{19}]cm^{-3}$ in all regions, this suggest it is possible to ignore changes in $\mu$ due to parametric defects in the fill fraction calculation and use $\mu_0$ in all regions.

A simplified magnetic field fill fraction expression is shown in Equation 9:

$$\eta_{region}=\frac{U_{region}}{U_{total}}=\frac{\int_{V_{region}}\frac{1}{\mu_0}\vec{B}^2(\vec{r})d\vec{r}}{\int_{V_{total}}\frac{1}{\mu_0}\vec{B}^2(\vec{r})d\vec{r}} \tag{9}$$

The spin density N of each region in the tan $\delta$ measurements from the previous section could be described with the simple expression for a given CPW geometry:

$$N_{total}=\eta_{Si}N_{Si}+\eta_{MS}N_{MS}+\eta_{SA}N_{SA}+\eta_{MA}S_{MA} \tag{10}$$

Measuring ESR data (and subsequent magnetic fill fraction) from all resonators with different geometries produces a linear system of equations that can be solved, given there are enough geometry variations.

Further to what was demonstrated in Calusine et al. with solving for the loss tangent in four different regions of the CPW geometry, the present disclosure proposes to solve for spin density in different regions of CPW used for cESR. In an example implementation, four spatial regions are of interest, and measurements may be introduced into the system of linear equations shown in Equation 11:

$$\begin{aligned}
N_{measured}^{R1}&=\eta_{Si}^{R1}N_{Si}+\eta_{MS}^{R1}N_{MS}+\eta_{SA}^{R1}N_{SA}+\eta_{MA}^{R1}N_{MA}\\
N_{measured}^{R2}&=\eta_{Si}^{R2}N_{Si}+\eta_{MS}^{R2}N_{MS}+\eta_{SA}^{R2}N_{SA}+\eta_{MA}^{R2}N_{MA}\\
N_{measured}^{R3}&=\eta_{Si}^{R3}N_{Si}+\eta_{MS}^{R3}N_{MS}+\eta_{SA}^{R3}N_{SA}+\eta_{MA}^{R3}N_{MA}\\
N_{measured}^{R4}&=\eta_{Si}^{R4}N_{Si}+\eta_{MS}^{R4}N_{MS}+\eta_{SA}^{R4}N_{SA}+\eta_{MA}^{R4}N_{MA}
\end{aligned} \tag{11}$$

In this example embodiment there will be four measurements $N_{measured}^{R}$ (where R is a label for each resonator) and the $B_1$ field fill fraction will be calculated for each region of each unique resonator $\eta_{region}^{R}$, which allows the four equations to be solved for the four unknown spin densities $N_{region}^{R}$.

Note that the fill fraction affects the signal to noise ratio (SNR) for each region according to Equation 12:

$$SNR=\frac{V_S}{V_N}=\frac{\chi''\eta Q\sqrt{PZ_0}}{\sqrt{P_nZ_0}}=\chi''\eta Q\sqrt{\frac{P}{P_n}} \tag{12}$$

where Q is the resonator quality factor, P is the drive power and P n is the noise power at the resonator output, $V_S$ and $V_N$ are the signal voltage and noise voltage at the resonator output, $Z_0$ is charact impedance of transmission line to which the resonator is coupled.

In one implementation, the superconducting material implemented in the present systems may be niobium (Nb). In another implementation, the superconducting material implemented in the present system may include one of: aluminum (Al), tantalum (Ta), niobium nitride (NbN), titanium nitride (TiN), or niobium titanium nitride (NbTiN). As shown in FIGS. **3** and **4**, the superconducting material overlays a dielectric in a fabrication stack.

FIG. **2** is a flowchart that illustrates an example method **200** of measuring noise in discrete regions of a multi-layer superconducting fabrication stack, for example the multi-layer fabrication stack of FIG. **3** or **4**, in accordance with the present systems and methods. In some implementations, the multi-layer superconducting fabrication stack may be a planned multi-layer superconducting processor chip. The processor chip may be used, for example, for quantum computing.

Method **200** comprises acts **201** to **208**; however, a person skilled in the art will understand that the number of acts is an example, and, in some implementations, certain acts may be omitted, further acts may be added, and/or the order of the acts may be changed. Method **200** may be executed by a digital computer, for example digital computer **102** in hybrid computing system **101**.

Method **200** starts at **201**, for example in response to a call from another routine.

At **202**, at least one spatial region of a proposed multi-layer superconducting fabrication stack or integrated circuit is identified. In some implementations, the multi-layer superconducting fabrication stack may be a proposed multi-layer superconducting processor chip that can be used, for example, for quantum computing. It will be understood that the proposed multi-layer superconducting integrated circuit may not have been fabricated, and may instead be a planned layout. For example, spatial regions based on proximity to one or more qubit wiring layers in the multi-layer processor chip may be identified as being of particular interest because of the proximity to noise-sensitive devices. For example, a proposed superconducting processor chip may have a substrate, a dielectric layer proposed to overly the substrate, and a first superconducting metal wiring layer that is proposed to contain all or part of qubit wiring for a processor overlying the dielectric layer. It may be beneficial to determine noise characteristics for some or all of the substrate, the dielectric to substrate interface, the metal to dielectric interface, the metal surface, and the metal to air (or metal to vacuum) interface.

At **203**, a plurality of different resonator geometries is generated. In one implementation, the resonators may be CPW resonators. At least one resonator geometry per spatial region identified at **202** is generated, so that the number of equations in the system of Equations 11 matches the number of variables. For example, if five spatial regions are identified at **202**, at least five different resonator geometries are generated at **203**. As discussed above, varying resonator geometry can, in some implementations, allow for tuning of each resonator frequency. By providing resonators having sufficiently distinct geometries, the signals generated by each resonator can be detected and measured separately.

In an example implementation, the geometries of CPW resonators may be varied by altering the cross section (e.g., the width between the ground plates and the center conductor of a resonator, or the width of the center conductor). Another example of a resonator geometry change is etching trenches of different depths between the center conductor

and the ground plates. Yet another example of geometry variation is altering the length of the resonator.

At **204**, a plurality of resonators is fabricated in and/or on a multi-layer superconducting fabrication stack. In one implementation, the resonators may be CPW resonators. In one example implementation, a multi-layer superconducting integrated circuit that reflects the proposed multi-layer superconducting fabrication stack of act **202** is fabricated. Based on the example given above and further described in FIGS. **3** and **4**, a resonator may be fabricated on a layer overlaying the dielectric layer in the superconducting fabrication stack. Each resonator is fabricated according to a distinct (i.e., different) one of the plurality of resonator geometries generated at **203** and has a unique resonance frequency. The resonance frequency can be chosen after determining the cross-section geometry of the resonator by varying the length of the resonator. The unique resonance frequency is used to uniquely address each resonator. Optionally, digital computer **102** measures the resonator geometries dimensions via scanning electron microscope (SEM).

At **205**, on-chip electron spin resonance (cESR) spectra from each resonator fabricated at **204** is measured.

At **206**, digital computer **102** computes magnetic field fill fractions $\eta$ of each spatial region using electro-magnetic (EM) field modeling together with the respective dimensions of each the resonator geometry from act **204**. The magnetic field fill fraction $\eta$ for a given region is the magnetic field energy in that region over the total magnetic field energy in the resonator. In one implementation, digital computer **102** uses a simplified fill fraction expression, in accordance with Equation 9 above.

At **207**, digital computer **102** computes each spatial region's spin density using the magnetic field fill fractions $\eta$ computed at **206** and the cESR spectra measured at **205**, as described above with reference to system of Equations 11.

At **208**, method **200** ends, until it is for example, invoked again.

FIG. **3** is a schematic diagram of a cross section of an example superconducting fabrication stack **300** that includes resonators to measure noise in discrete regions of the stack.

Superconducting fabrication stack **300** comprises a substrate **301**, having a first surface **301***a* and a second surface **301***b*, opposite the first surface, a dielectric layer **302**, having a first surface **302***a* and a second surface **302***b*, opposite the second surface, and a metal layer **303**, having a first surface **303***a* and a second surface **303***b*, opposite the first surface.

Superconducting fabrication stack **300** further comprises a first interface **304**, a substrate-to-dielectric interface, that in contact with substrate **301** and with dielectric layer **302**, so that first interface **304** is in contact with second surface **301***b* of substrate **301** and with first surface **302***a* of dielectric layer **302**. Superconducting fabrication stack **300** also comprises a second interface **305**, a dielectric-to-metal interface, that is in contact with a portion of dielectric layer **302** and with metal layer **303**, so that second interface **305** is in contact with a portion **302***b-a* of second surface **302***b* of dielectric layer **302** and with first surface **303***a* of metal layer **303**. A third interface **306**, a metal-to-air (or metal-to-vacuum) interface, is in contact with metal layer **303** so that third interface **306** is in contact with second surface **303***b* of metal layer **303**. A fourth interface **307**, a dielectric-to-m air or (dielectric-to-vacuum) interface, is in contact a portion of dielectric layer **302** so that fourth interface **307** is in contact with a portion **302***b-b* of second surface **302***b* of dielectric layer **302**.

Metal layer **303** comprises resonators for measuring noise in superconducting fabrication stack **300**, as discussed in method **200** of FIG. **2**. Metal layer **303** comprises a first ground plate **303***c*, a second ground plate **303***d* and a center conductor **303***e* to form a resonator. Only one resonator in metal layer **303** is shown in superconducting metal stack **300** to reduce visual clutter, but a person skilled in the art will understand that superconducting fabrications stack **300** may comprise a higher number of resonators in metal layer **303**. In particular, superconducting fabrication stack **300** may comprise four resonators to measure noise in the four interfaces **304** through **307**. In an example implementation, four resonators are etched into metal layer **303**. An example of a geometry change, as discussed above is the width **308** between ground plates **303***c*, **303***d* and a center conductor **303***e* of a resonator, or the depth **309** of the trench between ground plates **303***c*, **330***d* and center conductor **303***e*.

According to the embodiment of superconducting fabrication stack **300** of FIG. **3**, spatial regions that may be measured are first, second, third and fourth interfaces **304**, **305**, **306** and **307**.

FIG. **4** is a plan view of an example superconducting fabrication stack **400** that includes three resonators, each resonator having a different geometry.

Superconducting fabrication stack **400** comprises a first resonator **401**, a second resonator **402** and a third resonator **403**. Resonators **401** is coupled to a transmission line **404** via coupling device **401***a*, resonator **402** is coupled to transmission line **404** via coupling device **402***a* and resonator **403** is coupled to transmission line **404** via coupling device **403***a*. Coupling devices **401***a*, **402***a* and **403***a* are capacitive coupling device. In an alternative implementation, coupling devices **401***a*, **402***a* and **403***a* are inductive coupling devices. A person skilled in the art will understand that only three resonators are shown in FIG. **4** but superconducting fabrication stack **400** may comprise a lower or higher number of resonators, in particular superconducting fabrication stack **400** may comprise as many resonators are spatial regions to be measured. In an example implementation, resonators **401**, **402** and **403** are etched on a superconducting metal layer of superconducting fabrication stack **400**, e.g., metal layer **303** of superconducting fabrication stack **300**. Superconducting fabrication stack **400** also comprises wirebonding **405** coupled to transmission line **404**. Transmission line **404** is used to drive frequencies to resonators **401**, **402** and **403**, and to readout measurements from resonators **401**, **402** and **403**. Each resonator **401**, **402** and **403** has a different geometry, for example different width between ground plates and center conductor, represented in FIG. **4** by lines of different thickness, and different length, thereby resulting in a different resonator frequency. In an example embodiment, resonator **401** may have resonant frequency of 9.5 GHz, resonator **402** of 9.75 GHz, and resonator **403** of 10.0 GHz.

The above described method(s), process(es), or technique(s) could be implemented by a series of processor readable instructions stored on one or more nontransitory processor-readable media. Some examples of the above described method(s), process(es), or technique(s) method are performed in part by a specialized device such as an adiabatic quantum computer or a quantum annealer or a system to program or otherwise control operation of an adiabatic quantum computer or a quantum annealer, for instance a computer that includes at least one digital processor. The above described method(s), process(es), or technique(s) may include various acts, though those of skill in the art will appreciate that in alternative examples certain

acts may be omitted and/or additional acts may be added. Those of skill in the art will appreciate that the illustrated order of the acts is shown for example purposes only and may change in alternative examples. Some of the example acts or operations of the above described method(s), process(es), or technique(s) are performed iteratively. Some acts of the above described method(s), process(es), or technique(s) can be performed during each iteration, after a plurality of iterations, or at the end of all the iterations.

The above description of illustrated implementations, including what is described in the Abstract, is not intended to be exhaustive or to limit the implementations to the precise forms disclosed. Although specific implementations of and examples are described herein for illustrative purposes, various equivalent modifications can be made without departing from the spirit and scope of the disclosure, as will be recognized by those skilled in the relevant art. The teachings provided herein of the various implementations can be applied to other methods of quantum computation, not necessarily the example methods for quantum computation generally described above.

The various implementations described above can be combined to provide further implementations. All of the commonly assigned US patent application publications, US patent applications, foreign patents, and foreign patent applications referred to in this specification and/or listed in the Application Data Sheet are incorporated herein by reference, in their entirety, including but not limited to:

U.S. Pat. Nos. 7,533,068, 7,876,248; 8,035,540; 8,098,179; 8,536,566; 11,295,225; US Patent Application No. Publication 2018/02219150A1; and U.S. Provisional Patent Application No. 63/276,113.

These and other changes can be made to the implementations in light of the above-detailed description. In general, in the following claims, the terms used should not be construed to limit the claims to the specific implementations disclosed in the specification and the claims, but should be construed to include all possible implementations along with the full scope of equivalents to which such claims are entitled. Accordingly, the claims are not limited by the disclosure.

The invention claimed is:

**1**. A method of conducting spatial noise measurements in a superconducting fabrication stack, the superconducting fabrication stack comprising one or more material interfaces, the method comprising:

identifying one or more spatial regions of the superconducting fabrication stack;

generating a plurality of resonator geometries;

fabricating a plurality of resonators on the superconducting fabrication stack, each resonator of the plurality of resonators having a respective one of the plurality of resonator geometries;

measuring data from the plurality of resonators;

calculating fill fractions for the one or more spatial regions of the superconducting fabrication stack based on electromagnetic (EM) field modeling and respective dimensions of each resonator geometry; and

determining a spin density for each spatial region of the one or more spatial regions of the superconducting fabrication stack based on the data measured from the plurality of resonators and the calculated fill fractions.

**2**. The method of claim **1**, wherein measuring data from the plurality of resonators comprises measuring spectra of each resonator in the plurality of resonators using on-chip electron-spin resonance (cESR); and determining a spin density for each spatial region of the one or more spatial regions of the superconducting fabrication stack based on the data measured from the plurality of resonators and the calculated fill fractions comprises determining a spin density for each spatial region of the one or more spatial regions of the superconducting fabrication stack based on the cESR spectra measured from the plurality of resonators and the calculated fill fractions.

**3**. The method of claim **1**, wherein fabricating a plurality of resonators comprises fabricating a plurality of coplanar waveguide resonators.

**4**. The method of claim **1**, wherein fabricating a plurality of resonators on the superconducting fabrication stack, each resonator of the plurality of resonators having a respective one of the plurality of resonator geometries comprises fabricating a plurality of resonators on the superconducting fabrication stack, each resonator of the plurality of resonators having a respective resonance frequency.

**5**. The method of claim **1**, further comprising measuring the resonator geometries via scanning electron microscope (SEM) after fabricating the plurality of resonators.

**6**. The method of claim **1**, wherein generating a plurality of resonator geometries comprises generating as many resonator geometries as identified spatial regions.

**7**. The method of claim **1**, wherein identifying one or more spatial regions of the superconducting fabrication stack comprises identifying one or more spatial regions of the superconducting fabrication stack, the one or more spatial regions comprising at least one of: niobium, aluminum, tantalum, niobium nitride, titanium nitride, or niobium titanium nitride.

**8**. The method of claim **1**, wherein identifying one or more spatial regions of the superconducting fabrication stack comprises identifying one or more spatial regions of the superconducting fabrication stack, the one or more spatial regions comprising at least the one or more material interfaces.

**9**. The method of claim **1**, wherein fabricating a plurality of resonators on the superconducting fabrication stack comprises fabricating a plurality of resonators on a metal layer overlying a dielectric layer in the superconducting fabrication stack.

**10**. The method of claim **9** wherein fabricating a plurality of resonators on a metal layer overlying a dielectric layer in the superconducting fabrication stack comprises etching a plurality of resonators on a metal layer overlying a dielectric layer in the superconducting fabrication stack.

**11**. A method of conducting spatial noise measurements in a superconducting fabrication stack, the superconducting fabrication stack comprising a plurality of resonators, each resonator having a different resonator geometry, and the superconducting fabrication stack comprising a plurality of spatial regions, the method executed by a digital processor and comprising:

measuring data from the plurality of resonators;

calculating fill fractions for each spatial region in the plurality of spatial regions of the superconducting fabrication stack based on electromagnetic (EM) field modeling and respective dimensions of each resonator geometry; and

determining a spin density for each spatial region in the plurality of spatial regions of the superconducting fabrication stack based on the data measured from the plurality of resonators and the calculated fill fractions.

**12**. The method of claim **11**, wherein measuring data from the plurality of Resonators comprises measuring spectra of each resonator in the plurality of resonators using on-chip electron-spin resonance (cESR); and determining a spin

density for each spatial region in the plurality of spatial regions of the superconducting fabrication stack based on the data measured from the plurality of resonators and the calculated fill fractions comprises determining a spin density for each spatial region in the plurality of spatial regions of the superconducting fabrication stack based on the cESR spectra measured from the plurality of resonators and the calculated fill fractions.

**13**. The method of claim **12**, wherein measuring spectra of each resonator in the plurality of resonators using on-chip electron-spin resonance (cESR) comprises measuring cESR spectra of each resonator in the plurality of resonators, wherein each resonator has a unique resonance frequency.

**14**. The method of claim **11**, wherein measuring data from the plurality of resonators comprises measuring data from a plurality of coplanar waveguide resonators.

**15**. The method of claim **11** wherein measuring data from the plurality of resonators comprises measuring data from the plurality of resonators, wherein there are as many resonators as spatial regions.

**16**. The method of claim **11**, wherein calculating fill fractions for each spatial region of the plurality of spatial regions of the superconducting fabrication stack comprises calculating fill fractions for each spatial region of the plurality of spatial regions of a superconducting fabrication stack, at least one spatial region of the plurality of spatial regions comprising at least one of: niobium, aluminum, tantalum, niobium nitride, titanium nitride, or niobium titanium nitride.

**17**. The method of claim **11**, wherein collecting data from the plurality of resonators comprises collecting data from the plurality of resonators fabricated on a metal layer overlaying a dielectric layer in the superconducting fabrication stack.

**18**. The method of claim **11**, wherein calculating fill fractions for each spatial region in the plurality of spatial regions comprises calculating fill fractions for each spatial region in the plurality of spatial regions, at least one spatial region of the plurality of spatial regions comprising a material interface.

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