United States Patent Application Publication	20250266305
Kind Code	A1
Publication Date	August 21, 2025
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SEMICONDUCTOR PACKAGE SYSTEM AND RELATED METHODS

Abstract

Implementations of a semiconductor package may include: a substrate, a case coupled to the substrate and a plurality of press-fit pins. The press-fit pins are molded into and fixedly coupled with the case. The pins are also electrically and mechanically coupled to the substrate.

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Appl. No.: **19/186420**

Filed: **April 22, 2025**

Related U.S. Application Data

parent US continuation 17660319 20220422 parent-grant-document US 12308297 child US 19186420
parent US division 15136605 20160422 parent-grant-document US 11342237 child US 17660319
us-provisional-application US 62267349 20151215

Publication Classification

Int. Cl.: **H01L23/053** (20060101); **H01L21/52** (20060101); **H01L23/00** (20060101); **H01L23/498** (20060101); **H01L25/00** (20060101); **H01L25/065** (20230101); **H01L25/07** (20060101); **H01L25/18** (20230101)

U.S. Cl.:

CPC **H01L23/053** (20130101); **H01L21/52** (20130101); **H01L23/49811** (20130101); **H01L24/49** (20130101); **H01L24/85** (20130101); **H01L25/0655** (20130101); **H01L25/072** (20130101); **H01L25/18** (20130101); **H01L25/50** (20130101); H01L24/48 (20130101); H01L2224/48091 (20130101); H01L2224/48227 (20130101); H01L2924/00014 (20130101); H01L2924/01014 (20130101); H01L2924/13055 (20130101); H01L2924/13091 (20130101); H01L2924/15738 (20130101); H01L2924/15747 (20130101)

Background/Summary

CROSS REFERENCE TO RELATED APPLICATIONS [0001] This application is a continuation application of the earlier U.S. Utility Patent Application to Yushuang Yao entitled “Semiconductor Package System and Related Methods,” application Ser. No. 17/660,319, filed Apr. 22, 2022, now pending, which application is a divisional application of the earlier U.S. Utility Patent Application to Yushuang Yao entitled “Semiconductor Package System and Related Methods,” application Ser. No. 15/136,605, filed Apr. 22, 2016, now issued as U.S. Pat. No. 11,342,237, which application claims the benefit of the filing date of U.S. Provisional Patent Application 62/267,349, entitled “Semiconductor Package System and Related Methods” to Yushuang Yao which was filed on Dec. 15, 2015, the disclosures of each of which are hereby incorporated entirely herein by reference.

BACKGROUND
1. Technical Field
[0002] Aspects of this document relate generally to semiconductors, such as power integrated modules. More specific implementations involve press-fit pins for connecting printed circuit board.
2. Background
[0003] Conventionally, to connect a substrate to another circuit board, press-fit pins have been used. Conventional method of manufacture involves using a fixture is used to hold the pins in place on the substrate during the soldering process. Following soldering, the case is conventionally attached separately from the pins.
SUMMARY
[0004] Implementations of a semiconductor package may include: a substrate, a case coupled to the substrate and a plurality of press-fit pins. The press-fit pins may be molded into and fixedly connected with the case. The pins may be electrically and mechanically coupled to the substrate.
[0005] Implementations of a semiconductor package may include one, all, or any of the following:
[0006] The case may have an opening having a strut that extends from a side of the opening to another side of the opening and a first set of a plurality of fingers extending from the strut on one side of the strut and a second set of a plurality of fingers extending from an opposing side of the strut.
[0007] A cover may be coupled to the case, the cover having a plurality of openings therethrough, the plurality of openings configured to receive the plurality of pins.
[0008] The case may have a cover with the plurality of pins molded into and fixedly coupled thereto, the cover having a potting opening therethrough.
[0009] A casing may be configured to be fixedly coupled over one or more edges of the cover and over at least a portion of the substrate.
[0010] The casing may have a plurality of locking projections that engage with the one or more edges of the cover and irreversibly lock the cover to the casing.
[0011] Implementations of a semiconductor package may be manufactured using implementations

of a method of making semiconductor packages. The method may include providing a substrate, coupling one or more die to the substrate, coupling the die to the substrate using one or more connectors and providing a case. The method may also include molding into the case and fixedly coupling thereto a plurality of pins. The method may also include simultaneously electrically and mechanically coupling the plurality of pins and the case with the substrate. The method may also include dispensing a potting compound inside the case over at least a portion of the substrate.
[0012] Implementations of a method of making a semiconductor package may include one, all, or any of the following:
[0013] The case may have an opening having a strut that extends from a side of the opening to another side of the opening. The case may have a first set of a plurality of fingers extending from the strut on one side of the strut. The case may also have a second set of a plurality of fingers extending from an opposing side of the strut.
[0014] A cover may be included that may have a plurality of openings therethrough configured to receive the plurality of pins is coupled to the case.
[0015] The substrate may include at least one of copper, silicon, and any combination thereof.
[0016] The pins may be fixedly coupled to the substrate through soldering.
[0017] The one or more connectors may comprise a wire.
[0018] Semiconductor package implementations disclosed herein may be manufactured using another method of manufacturing a semiconductor package. The method implementations may include providing a substrate, coupling one or more die to the substrate and coupling the die using one of more connectors. The method may also include providing a cover for a case, the cover having a potting opening therein. The method may also include molding into the cover and fixedly coupling thereto a plurality of pins. The method may also include simultaneously electrically and mechanically coupling the plurality of pins and the cover to the substrate. The method may also include coupling a casing over the cover and to the substrate. The method may also include dispensing a potting compound into the case through the potting opening in the cover.
[0019] Implementations of a method of making a semiconductor package may include one, all, or any of the following:
[0020] A temporary fixture may be used to hold the cover and the substrate together while coupling the plurality of pins and the cover to the substrate.
[0021] A plurality of locking projections on the casing may be included to mechanically and irreversibly lock the cover with the casing.
[0022] The substrate may include at least one of copper, silicon or any combination thereof.
[0023] The pins may be fixedly coupled to the substrate through soldering.
[0024] The one or more connectors may be made of a wire.
[0025] The foregoing and other aspects, features, and advantages will be apparent to those artisans of ordinary skill in the art from the DESCRIPTION and DRAWINGS, and from the CLAIMS.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0026] Implementations will hereinafter be described in conjunction with the appended drawings, where like designations denote like elements, and:
[0027] FIG. **1** is a perspective view of a plurality of press-fit pins molded into a case;
[0028] FIG. **2** is a side view of a plurality of press-fit pins molded into a cover;
[0029] FIG. **3**A is a top view of a plurality of press-fit pins molded into the fingers of a case;
[0030] FIG. **3**B is a cross-sectional view of a plurality of press-fit pins molded into the fingers of a case.
[0031] FIGS. **4**A-**4**F shows an implementation of a method of making a semiconductor package

with press-fit pins molded into fingers of a case.
[0032] FIGS. **5**A-**5**F shows an implementation of a method of making a semiconductor package with press-fit pins molded into a cover.

DESCRIPTION

[0033] This disclosure, its aspects and implementations, are not limited to the specific components, assembly procedures or method elements disclosed herein. Many additional components, assembly procedures and/or method elements known in the art consistent with the intended semiconductor packages will become apparent for use with particular implementations from this disclosure. Accordingly, for example, although particular implementations are disclosed, such implementations and implementing components may comprise any shape, size, style, type, model, version, measurement, concentration, material, quantity, method element, step, and/or the like as is known in the art for such semiconductor packages, and implementing components and methods, consistent with the intended operation and methods.
[0034] FIG. **1** illustrates a cross section view of a first implementation semiconductor package **2** where routing lines **4** are electrically and mechanically coupled to a plurality of press-fit pins **8**. As illustrated, the plurality of press-fit pins are molded into a case having fingers **6**. A cover **10** is encloses the package **2** and the plurality of pins fit through a plurality of openings in the cover.
[0035] Referring to FIG. **2**, a second implementation of a semiconductor package **12** is illustrated. Differently oriented press-fit pins **16** and **18** are molded into and fixedly coupled to a cover **14** and enclosed in a case **20**. The case **20** with a plurality of press-fit pins **16** and **18** and cover **14** is fixedly coupled to the substrate **22**. Both first and second implementations of semiconductor packages disclosed herein may help to decrease stress on individual press-fit pins of the plurality of press-fit pins.
[0036] Referring to FIG. **3**A, a top view of the first implementation of a semiconductor package **24** is illustrated. The case **26** has an opening therein where a strut **28** extends from a side of the opening to another side of the opening. A first set of a plurality of fingers **30** extend from the strut **28** on one side of the strut **28** and a second set of a plurality of fingers **30** extend from an opposing side of the strut **28**. The plurality of press-fit pins **32** are molded into the fingers **30** and held by the fingers **30**. Referring to FIG. **3**B, a cross-sectional view of an implementation of a semiconductor package **34** like that of FIG. **3**A is illustrated. The case **36** encloses the fingers **38** which are molded around the plurality of press-fit pins **40**. By non-limiting example a cover **42** may be subsequently added over the press-fit pins **40** embedded in the fingers **38**. As can be seen in FIG. **3**B, all of the press fit pins are oriented the same directly to allow them to be molded in to the fingers **30**. In such implementations, this may allow all of the fingers to have the same size. In other implementations, however, the fingers may vary in width and size relative to each other to allow pins of differing orientations (and/or sizes) to be simultaneously molded into the fingers.
[0037] Referring to FIGS. **4**A-**4**F, a method for manufacturing a semiconductor package is illustrated. FIG. **4**A illustrates a substrate **44**. The substrate **44** may be made of any material including copper, silicon, any combination thereof, or a ceramic or other electrically conductive/insulative material. FIG. **4**B illustrates the addition of die **48** to the substrate **46**. The die **48** can include, by non-limiting example, an insulated gate bipolar junction transistor (IGBT) a rectifier, a metal oxide field effect transistor (MOSFET), or any other semiconductor device. FIG. **4**C illustrates the semiconductor package **50** with addition of connectors **56** to mechanically and electronically connect the die **54** to other die **48** and to the substrate **52**. The connectors **56** may include a wire made of any electrically conductive material. FIG. **4**D illustrates the semiconductor package **58** as case **60** that includes the plurality of pins molded into it is being coupled to the substrate **68**. The case **60** is similar to that illustrated in FIGS. **3**A and **3**B. The case **60** has a strut **62** that extends from one side of an opening in the case to an opposite side of the opening. Extending from either side of the strut **62** are fingers **64**. The fingers **64** extend from the strut **62** to the sides of the case **60**. Embedded in the fingers **64** of the strut is a plurality of press-fit pins **66**.

The press-fit pins **66** are simultaneously electrically and mechanically coupled to the substrate **68** as the case **60** is coupled to the substrate **68** which may decrease the force exerted on the individual press-fit pins. FIG. **4**E illustrates an optional step of coupling a cover **76** to the case **60**. The cover **76** has holes therethrough formed in it that allow the press-fit pins **74** to pass through the cover **76**. The cover **76** is placed over the press-fit pins and rests inside the case **72**. In particular implementations, the cover rests on a flange formed around the opening in the cover. Before the cover **76** is added. a potting compound may be added through the opening within the case **72**. FIG. **4**F is an illustration of the finished semiconductor package **76**. This method may allow for automation of semiconductor package manufacturing when using press-fit pins, as all of the pins may be simultaneously and mechanically coupled to the substrate when the case **60** is coupled to the substrate **68**. This may eliminate the need to use fixtures of any kind to hold the pins individually or collectively to the substrate during manufacturing.

[0038] Referring to FIGS. **5**A-**5**F, another implementation of a method of manufacturing a semiconductor package is illustrated. FIG. **5**A illustrates a substrate **84**. The substrate **84** may be made of any material including copper, silicon, ceramics, electrically conductive/insulative materials and any combination thereof. FIG. **5**B illustrates the substrate following coupling of the die **90** to the substrate **88**. The die **90** can include, by non-limiting example, an insulated gate bipolar junction transistor (IGBT) a rectifier, a metal oxide field effect transistor (MOSFET), or any other semiconductor device. FIG. **5**C illustrates the semiconductor package **92** following coupling wires **98** to mechanically and electronically connect the die **96** to other die and to the substrate **94**. FIG. **5**D illustrates the semiconductor package following coupling of a cover **104** and press-fit pins **108** to the substrate **102**. As can be seen from the figure, the press-fits pins **108** are molded into and fixedly coupled with the cover. When the cover is placed over the substrate the press-fit pins are electrically and mechanically coupled with the substrate **102**. Also, they are automatically aligned to the specific locations on the substrate **102** to which they are to be bonded. The cover **104** includes an opening **106** to allow for the addition of potting compound. FIG. **5**E illustrates the package after the case **112** has been coupled over the cover **104**. The case **112** fits around and over the cover **114** with the embedded press-fit pins **116** and couples the cover **114** with the substrate **118**. As illustrated, a flange extends around the perimeter of the cover **114** which engages with a corresponding flange around the opening of the case **112**. In other implementations, however, the flange may be not be included and the cover **114** may merely be retained within the opening of the case **112**. The case **112** may also include a plurality of locking projections **113** which engage with the one or more edges of the cover **114**. The locking projections **113** may, in various implementations, irreversibly lock the cover **114** to the case **112**. FIG. **5**F illustrates an implementation of the finished semiconductor package **120**. The case **122** is coupled to the cover **124** and the embedded press-fit pins **126** are coupled to the substrate **102**. Potting compound can now optionally be added through the opening **128** in the cover **124**. This method may also allow for automation of semiconductor package manufacturing when using press-fit pins by eliminating the need for a fixture to be used to hold all of the pins during the soldering step. Instead, this method implementation permits a single fixture to be used that holds the cover itself during the soldering/coupling step, which is much simpler mechanically.

[0039] In places where the description above refers to particular implementations of semiconductor packages and implementing components, sub-components, methods and sub-methods, it should be readily apparent that a number of modifications may be made without departing from the spirit thereof and that these implementations, implementing components, sub-components, methods and sub-methods may be applied to other semiconductor packages.

Claims

1. A method for making a semiconductor package, the method comprising: providing a substrate coupled to one or more die; providing a case; molding into the case and fixedly coupling thereto a plurality of pins; simultaneously electrically and mechanically coupling the plurality of pins and the case with the substrate.
2. The method of claim 1, wherein the case comprises an opening comprising a strut that extends from a side of the opening to another side of the opening and a first set of a plurality of fingers extending from the strut on one side of the strut and a second set of a plurality of fingers extending from an opposing side of the strut.
3. The method of claim 1, wherein a cover that has a plurality of openings therethrough configured to receive the plurality of pins is coupled to the case.
4. The method of claim 1, wherein the substrate comprises at least one of copper, silicon, and any combination thereof.
5. The method of claim 1, wherein the plurality of pins are fixedly coupled to the substrate through soldering.
6. The method of claim 1, wherein the semiconductor package is a transfer molded package.
7. A method for making a semiconductor package, the method comprising: providing a substrate coupled to one or more die; and simultaneously coupling one of a plurality of pins and a cover to the substrate or the plurality of pins and a case to the substrate.
8. The method of claim 7, wherein the semiconductor package is a transfer molded package.
9. The method of claim 7, further comprising molding the plurality of pins into one of the cover or the case.
10. The method of claim 7, wherein the plurality of pins extend through a plurality of openings comprised in the cover.
11. The method of claim 7, further comprising mechanically and irreversibly locking the cover with the case through a plurality of locking projections on the case.
12. The method of claim 7, wherein the plurality of pins is fixedly coupled to one of the case or the cover prior to coupling the plurality of pins to the substrate.
13. The method of claim 7, wherein the substrate comprises of at least one of copper, silicon, and any combination thereof.
14. A semiconductor package comprising: a substrate; a case coupled to the substrate; and a plurality of press-fit pins; wherein the plurality of press-fit pins are electrically and mechanically coupled to the substrate; and wherein the plurality of press-fit pins are molded into and fixedly coupled with the case.
15. The semiconductor package of claim 14, wherein the semiconductor package is a transfer molded package.
16. The semiconductor package of claim 14, wherein the substrate is coupled to one or more semiconductor die.
17. The semiconductor package of claim 14, wherein the plurality of press-fit pins comprises at least one locking portion that extends from a side of the plurality of press-fit pins and is molded into the case.
18. The semiconductor package of claim 14, further comprising a plurality of struts within the case.
19. The semiconductor package of claim 14, wherein the substrate comprises at least one of copper, silicon, and any combination thereof.
20. The method of claim 14, wherein the plurality of pins are fixedly coupled to the substrate through soldering.