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### PACKAGE PROCESS AND PACKAGE STRUCTURE

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#### Abstract

A package structure includes: 1) a circuit substrate; 2) a first semiconductor device disposed on the circuit substrate; 3) a first insulation layer covering a sidewall of the first semiconductor device; 4) a second insulation layer covering the first insulation layer; and 5) a third insulation layer disposed on the circuit substrate and in contact with the second insulation layer.

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## Background/Summary

CROSS-REFERENCE TO RELATED PATENT APPLICATIONS [0001] This application is a continuation of U.S. patent application Ser. No. 17/573,593 filed on Jan. 11, 2022, now U.S. Pat. No. 12,266,632 which is a continuation of U.S. patent application Ser. No. 15/620,692 filed on Jun. 12, 2017, now U.S. Pat. No. 11,222,866 which is a continuation of U.S. patent application Ser. No. 14/087,454 filed on Nov. 22, 2013, now U.S. Pat. No. 9,698,120 which is a divisional of U.S. patent application Ser. No. 12/711,870 filed on Feb. 24, 2010, now U.S. Pat. No. 8,618,645, which claims priority to and the benefit of Taiwan application No. 98133269, filed on Sep. 30, 2009. The entirety of each of the above-mentioned patent applications is hereby incorporated by reference herein and made a part of this specification.

### BACKGROUND

#### Field of the Invention

[0002] The present invention relates to a package process and a package structure, and more particularly, to a package process for configuring a relatively large chip onto a relatively small chip and a package structure with a relatively large chip stacked on a relatively small chip.

#### Description of Related Art

[0003] In today's information society, users all seek after electronic products with high speed, high quality and multiple functions. In terms of the product exterior appearance, electronic product designs reveal a trend of light weight, thinness and compactness. Therefore, it is develops various chip package techniques such as stacked-type chip package technique.

[0004] In the stacked-type chip package technique, several chips are perpendicularly stacked together in the same package structure so that the package density is improved and the dimension of the package is decreased. Furthermore, by using 3-dimensional chip stacking method to decrease

the path length of the signal transmission between the chips, rate of the signal transmission is improved and the chips with different functions can be combined in the same package.

[0005] In the conventional stacked-type chip package technique, several chips are flip-chip bonded on a wafer, and then the wafer is cut along the gaps between the chips to form several chip stacked structures. Thereafter, the chip stacked structures are configured on a circuit substrate, and a molding compound is formed on the circuit substrate to protect the chip stacked structures.

[0006] Since, in the conventional stacked-type chip package technique, the chip stacked structures are formed by cutting the wafer, in the chip stacked structures, the chips formed from cutting the wafer are larger than the chips flip-chip bonded onto the wafer. Hence, the conventional stacked-type chip package technique is used to form the package structure with the small chip stacked onto the large chip.

[0007] Furthermore, in the conventional technique, in order to decrease the whole thickness of the stacked-type chip package, the wafer is polished to decrease the thickness of the wafer before the chips are flip-chip bonded on the wafer. However, the process capacitance of the flip-chip bonding technique still has its limit value. When the thickness of the wafer is smaller than the limit value of the process capacitance, fracture often results in the flip-chip bonding technique. Thus, the production yield rate is decreased. Moreover, the fracture of the wafer with a relatively small thickness easily happens during the wafer cutting process. Hence, the production yield rate is decreased.

#### SUMMARY OF THE INVENTION

[0008] The present invention provides a package process capable of producing a package structure having various dimensions of chips stacked one another and having high production yield rate.

[0009] The present invention provides a package structure in which the large chip is configured on the small chip.

[0010] The present invention provides a package process comprising providing a carrier board having an adhesive layer configured thereon. A plurality of first semiconductor devices are configured on the adhesive layer, wherein the first semiconductor devices are separated from each other and fixed on the carrier board through the adhesive layer. Then, a first molding compound is formed on the carrier board to cover the sidewalls of the first semiconductor devices and to fill gaps between the first semiconductor devices so as to form a chip array board comprising the first semiconductor devices and the first molding compound. Thereafter, a plurality of second semiconductor devices is flip-chip bonded to the first semiconductor devices respectively. A second molding compound is formed on the chip array board to at least cover the sidewalls of the second semiconductor devices and to fill gaps between the second semiconductor devices. Then, the chip array board is separated from the adhesive layer. The first molding compound and the second molding compound are cut along the filled gaps between the second semiconductor devices to form a plurality of chip package units.

[0011] In one embodiment of the present invention, each of the first semiconductor devices has a plurality of through-silicon vias and the package process further comprises, after the chip array board is formed, polishing the chip array board to thin the chip array board to expose end surfaces of the through-silicon vias of each of the first semiconductor devices.

[0012] In one embodiment of the present invention, a method of polishing the chip array board comprises: polishing the chip array board until a thickness of the chip array board is substantially smaller than or equal to 4 mil.

[0013] In one embodiment of the present invention, after the second semiconductor devices are flip-chip bonded to the first semiconductor devices respectively, an area of an orthogonal projection of each of the second semiconductor devices on the carrier board is larger than an area of an orthogonal projection of each of the first semiconductor devices on the carrier board.

[0014] In one embodiment of the present invention, after the chip array board is formed, a plurality of first underfills are individually formed on the first semiconductor devices, wherein each of the

first underfills covers the corresponding first semiconductor device and a portion of the first molding compound surrounding the corresponding first semiconductor device, and each of the second semiconductor devices is flip-chip bonded to the corresponding first semiconductor devices by a plurality of conductive bumps of each of the second semiconductor devices passing through the corresponding first underfill on the corresponding first semiconductor device.

[0015] In one embodiment of the present invention, the second molding compound exposes a top surface of each of the second semiconductor devices away from the corresponding first semiconductor device.

[0016] In one embodiment of the present invention, the second molding compound covers a top surface of each of the second semiconductor devices away from the corresponding first semiconductor device.

[0017] In one embodiment of the present invention, for one of the chip package units, the chip package unit is configured on a circuit substrate so that the first semiconductor device is electrically and structurally connected to the circuit substrate.

[0018] In one embodiment of the present invention, for one of the chip package units, a second underfill is formed on the circuit substrate so that the second underfill is configured between the first semiconductor device of the chip package unit and the circuit substrate and covers a plurality of conductive bumps of the first semiconductor device.

[0019] In one embodiment of the present invention, for one of the chip package units, the package process further comprises forming a third molding compound on the circuit substrate, wherein the third molding compound at least covers a sidewall of the chip package unit.

[0020] In one embodiment of the present invention, for one of the chip package units, the second molding compound and the third molding compound expose a top surface of the second semiconductor devices away from the corresponding first semiconductor device.

[0021] In one embodiment of the present invention, for one of the chip package units, the third molding compound covers top surfaces of the second semiconductor devices away from the corresponding first semiconductor device.

[0022] In one embodiment of the present invention, for one of the chip package units, the package process further comprises forming a plurality of solder balls on the surface of the circuit substrate away from the chip package unit, wherein the solder balls are electrically connected to the circuit substrate.

[0023] The present invention further provides a package structure comprising a first semiconductor device, a first molding compound, a second semiconductor devices and a second molding compound. The first molding compound encloses the sidewall of the first semiconductor device. The second semiconductor device is configured on the first semiconductor device and a portion of the first molding compound, wherein a dimension of the second semiconductor device is larger than a dimension of the first semiconductor device. The second molding compound at least covers the sidewall of the second semiconductor device and the first molding compound, wherein the first molding compound and the second molding compound are individually formed.

[0024] In one embodiment of the present invention, the side surface of the first molding compound is aligned with the side surface of the second molding compound.

[0025] In one embodiment of the present invention, a first top surface of the first molding compound facing the second semiconductor device is aligned with a second top surface of the first semiconductor device facing the second semiconductor device.

[0026] In one embodiment of the present invention, a thickness of first molding compound is substantially equal to a thickness of the first semiconductor device.

[0027] In one embodiment of the present invention, the second semiconductor device has a plurality of conductive bumps configured between the second semiconductor device and the first semiconductor device and the package structure further comprises an underfill configured between the second semiconductor device and the first semiconductor device and between the second

semiconductor device and the first molding compound to enclose the conductive bumps of the second semiconductor device.

[0028] In one embodiment of the present invention, a thickness of the first semiconductor device is substantially smaller than or equal to 4 mil.

[0029] In one embodiment of the present invention, a thickness of the first semiconductor device is substantially 2 mil.

[0030] In one embodiment of the present invention, the second molding compound further covers a top surface of the second semiconductor device and the top surface is away from the first semiconductor device.

[0031] In one embodiment of the present invention, the second molding compound exposes a top surface of the second semiconductor device and the top surface is away from the first semiconductor device.

[0032] In one embodiment of the present invention, a bottom surface of the first semiconductor device away from the second semiconductor device has a plurality of conductive bumps configured thereon.

[0033] In one embodiment of the present invention, the package structure further comprises a circuit substrate with the first semiconductor device configured thereon, wherein the conductive bumps are configured between the first semiconductor device and the circuit substrate.

[0034] In one embodiment of the present invention, the chip package structure further includes an underfill configured between the first semiconductor device and the circuit substrate to enclose the conductive bumps.

[0035] In one embodiment of the present invention, the package structure further comprises a third molding compound configured on the circuit substrate to cover at least the sidewall of the first molding compound and the sidewall of the second molding compound.

[0036] In one embodiment of the present invention, the second molding compound and the third molding compound expose a top surface of the second semiconductor device and the top surface is away from the first semiconductor device.

[0037] In one embodiment of the present invention, the third molding compound covers a top surface of the second semiconductor device and the top surface is away from the first semiconductor device.

[0038] In one embodiment of the present invention, the package structure further comprises a plurality of solder balls configured on a bottom surface of the circuit substrate away from the first semiconductor device, wherein the solder balls are electrically connected to the circuit substrate.

[0039] Accordingly, the present invention can produce the package structure in which the chips with various dimensions are stacked on one another. Furthermore, since the second molding compound can strengthen the chip array board with a relatively small thickness so that the second semiconductor devices and the first semiconductor devices are securely connected to one another. Therefore, during the cutting process for forming the chip package units, the chip array board can be prevented from being fractured so that the production yield rate can be improved.

[0040] In order to make the aforementioned and other features and advantages of the invention more comprehensible, embodiments accompanying figures are described in detail below.

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## **Description**

### **BRIEF DESCRIPTION OF THE DRAWINGS**

[0041] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0042] FIGS. 1A through 1I are cross-sectional views illustrating a package process according to one embodiment of the present invention.

[0043] FIGS. 2A through 2D are cross-sectional views illustrating a package process according to one embodiment of the present invention.

#### DETAILED DESCRIPTION

[0044] FIGS. 1A through 1I are cross-sectional views illustrating a package process according to one embodiment of the present invention.

[0045] As shown in FIG. 1A, a carrier board **110** is provided and the shape and the dimension of the carrier board **110** are similar to those of a wafer. The carrier **110** has an adhesive layer **120** configured thereon. Then, a plurality of first semiconductor devices **130** are configured on the adhesive layer **120**, wherein the first semiconductor devices **130** are separated from each other and fixed on the carrier board **110** through the adhesive layer **120**. In the present embodiment, each of the first semiconductor devices **130** has a plurality of conductive bumps **132** buried in the adhesive layer **120**.

[0046] More clearly, in the present embodiment, before the first semiconductor devices **130** are configured on the adhesive layer **120**, a plurality of openings **138** are formed in each of the first semiconductor devices **130** and each of the openings has a relatively high aspect ratio.

Furthermore, an insulating layer I is formed on the inner walls of the openings **138** and then a conductive material D is formed to fill up each of the openings **138** so that the insulating layer I separate the conductive material D from the inner wall of each of the opening **138**. Thereafter, the conductive bumps **132** are formed on the conductive materials D respectively.

[0047] Then, as shown in FIG. 1B, a first molding compound **140** is formed on the carrier board **110** by printing or molding, wherein the first molding compound **140** covers the sidewalls **134** of the first semiconductor devices **130** and fills gaps G1 between the first semiconductor devices **130** so as to form a chip array board A comprising the first semiconductor devices **130** and the first molding compound **140**. Specifically, in the present embodiment, the chip array board A can be a board type structure composed of the first molding compound **140** and the whole first semiconductor devices **130**.

[0048] Then, as shown in FIG. 1C, in the present embodiment, the chip array board A can be polished to thin the chip array board A to expose the conductive material D. In the present embodiment, the chip array board can be polished until a thickness of the chip array board is substantially smaller than or equal to 4 mil. In the present embodiment, the conductive material D, the insulating layer I and the opening **138** together form a through-silicon via (TSV) structure V.

[0049] According to the above description, the TSV technique is applied on each of the first semiconductor devices **130** for being electrically connect to the conductive bumps **132** and to other chips (not shown) later stacked onto the first semiconductor devices. In the TSV technique, for instance, the conductive paths are fabricated within the chip or within the wafer so as to form the TSV structures V perpendicular to the surface of the chip or the wafer. Therefore, the 3-dimensional stacking density of the first semiconductor devices **130** is maximized and the dimension of stacking the first semiconductor devices **130** is minimized. Hence, the signals between the first semiconductor devices **130** and the other chips stacking on the first semiconductor devices **130** can be transmitted through the TSV structures V to decrease the transmission path length between the chips and improve the signal delay phenomenon and decrease power consumption.

[0050] Thereafter, as shown in FIG. 1D, in the present embodiment, a plurality of underfills **150** can be separately formed the chip array board A by dispensing or screen printing. Each of the underfills **150** covers the corresponding first semiconductor device **130** and a portion of the first molding compound **140** enclosing the corresponding first semiconductor device **130**. More clearly, each of the underfills **150** not only entirely covers the corresponding first semiconductor device **130** but also covers a portion of the first molding compound **140** enclosing the corresponding first

semiconductor device **130**. In other words, the dimension of the orthogonal projection of each of the underfills **150** on the carrier board **110** is larger than the dimension of the orthogonal projection of each of the first semiconductor devices **130** on the carrier board **110**. The material of each of the underfills **150** includes non-contact paste (NCP1) or non-contact film (NCF1).

[0051] Then, as shown in FIG. **1E**, a plurality of second semiconductor devices **160** are flip-chip bonded on the first semiconductor devices **130** respectively so that a plurality of the conductive bumps **162** of each of the second semiconductor devices **160** are bonded to the TSV structures **V** of the corresponding first semiconductor device **130** respectively by passing through the corresponding underfill **150**. In the present embodiment, the dimension of the orthogonal projection of each of the second semiconductor devices **160** on the carrier board **110** is larger than the dimension of the orthogonal projection of each of the first semiconductor devices **130** on the carrier board **110**. In other words, the dimension of each of the second semiconductor devices **160** is larger than the dimension of each of the first semiconductor devices **130**.

[0052] Then, as shown in FIG. **1F**, a second molding compound **170** is formed on the chip array board **A** by printing or molding, wherein the second molding compound **170** can selectively cover the sidewalls **164** of the second semiconductor devices **160** and the top surface **166** of the second semiconductor device **160** away from the first semiconductor device **130** to fill up gaps **G2** between the second semiconductor devices **160** to protect the second semiconductor devices **160**. It should be noticed that since the second molding compound **170** fills up the gaps **G2** between the second semiconductor devices **160**, the second molding compound **170** can strengthen the chip array board **A** with a relatively small thickness. Therefore, the whole second semiconductor devices **160** and the whole first semiconductor devices **130** are securely connected to one another.

Moreover, in the other embodiments, the step of forming the underfills **150** can be replaced by the step of filling up a space between the second semiconductor devices **160** and the chip array board **A** with a portion of the second molding compound **170**.

[0053] Then, as shown in FIG. **1G**, the chip array board **A** is separated from the adhesive layer **120**. Thereafter, as shown in FIG. **1G** together with FIG. **1H**, the second molding compound **170** and the first molding compound **140** are cut along the filled gaps **G2** between the second semiconductor devices **160** to form a plurality of chip package units **C1**.

[0054] Accordingly, in the present embodiment, the first semiconductor devices **130** are connected together to form a chip array board **A** by using the first molding compound **140**, and then the second semiconductor devices **160** are configured on the first semiconductor devices **130** of the chip array board **A** respectively and are connected together by the second molding compound **170**. Thereafter, the first molding compound **140** and the second molding compound **170** are cut to form the chip package units **C1**. In other words, in the present embodiment, the first molding compound **140** and the second molding compound **170** are used to secure and connect the first semiconductor devices **130** and the second semiconductor devices **160**, and then the first molding compound **140** and the second molding compound **170** are cut to form the chip package units **C1**.

[0055] Therefore, the present embodiment is not limited to the dimension relationship between the first semiconductor devices **130** and the second semiconductor devices **160**. That is, the chip package unit **C1** in the present embodiment can have the first semiconductor device **130** stacked by the second semiconductor device **160**, in which the dimension of the first semiconductor device **130** can be larger than, equal to or smaller than the dimension of the second semiconductor device **160**. In other words, the present invention can produce the package structure in which the chips with various dimensions are stacked on one another. Furthermore, since the second molding compound **170** can strengthen the chip array board **A** with a relatively small thickness so that, during the cutting process for forming the chip package units, the chip array board **A** can be prevented from being fractured. Thus, the production yield rate can be improved.

[0056] Moreover, as shown in FIG. **1H** together with FIG. **1I**, in the present embodiment, an underfill **190** can be formed on a circuit substrate **180** (such as printed circuit board), and one of the

aforementioned chip package units C1 is configured on the circuit substrate **180** so that the first semiconductor device **130** can electrically and structurally connected to the circuit substrate **180** through the conductive bumps **132** and the underfill **190** is configured between the chip package unit C1 and the circuit board **180** to enclose the conductive bumps **132** of the first semiconductor device **130**.

[0057] As shown in FIG. **1I**, in the present embodiment, a third molding compound M is formed on the circuit substrate **180** by, for example, printing or molding. The third molding compound M can cover the sidewall W of the chip package unit C1 and the top surface **166** of the second semiconductor device **160**. More clearly, a portion of the third molding compound M is configured on a portion of the second molding compound **170** covering the top surface **166**. That is, the third molding compound M indirectly covers the top surface **166** of the second semiconductor device **160**. Among other embodiments not shown in the drawings, the third molding compound M can cover the sidewall W of the chip package unit C1 and exposes the portion of the second molding compound covering the top surface **166**.

[0058] Moreover, in the other embodiments, the step of forming the underfills **190** can be replaced by the step of filling up a space between the first semiconductor device **130** and the circuit substrate **180** with a portion of the third molding compound M. In addition, in order to electrically connect the chip package unit C1 to other electronic devices through the circuit substrate **180**, a plurality of solder balls S can be formed on a bottom surface **182** of the circuit substrate **180** away from the chip package unit C1, and the solder balls S can be electrically connected to the circuit substrate **180**. So far, the package structure **100** of the present embodiment is initially formed.

[0059] The details of package structure **100** shown in FIG. **1I** are provided hereafter.

[0060] As shown in FIG. **1I**, the package structure **100** of the present embodiment includes a first semiconductor device **130**, a first molding compound **140**, a second semiconductor device **160** and a second molding compound **170**. In the present embodiment, the thickness T2 of the first semiconductor device **130** is substantially smaller or equal to 4 mil. For instance, the thickness T2 of the first semiconductor device **130** is substantially 2 mil.

[0061] The first molding compound **140** encloses the sidewall **134** of the first semiconductor device **130**. In the present embodiment, a top surface **144** of the first molding compound **140** facing the second semiconductor device **160** is aligned with a second top surface **136** of the first semiconductor device **130** facing the second semiconductor device **160**, and the thickness T1 of the first molding compound **140** is substantially equal to the thickness T2 of the first semiconductor device **130**.

[0062] The second semiconductor device **160** is configured on the first semiconductor device **130** and a portion of the first molding compound **140**, wherein a dimension of the second semiconductor device **160** is larger than a dimension of the first semiconductor device **130**. In other words, the area of the bottom surface **168** of the second semiconductor device **160** facing the first semiconductor device **130** is larger than the area of the top surface **136** of the first semiconductor device **130**.

[0063] It should be noticed that, in the package structure **100** of the present embodiment, the chip with a relatively large dimension is configured on the chip with a relatively small dimension. Thus, the package structure **100** can be adaptive to the package structure having the memory chip with a relatively large dimension on the operational chip with a relatively small dimension. Moreover, because the thickness T2 of the first semiconductor device **130** of the present embodiment is relatively small (for instance, the thickness T2 is smaller than or equal to 4 mil), the total thickness of the package structure **100** can be decreased.

[0064] The second molding compound **170** covers the sidewall **164** of second semiconductor device **160**, the top surface **166** of the second semiconductor device **160** away from the first semiconductor device **130** and the first molding compound **140**, wherein the first molding compound **140** and the second molding compound **170** are individually formed, and the sidewall



**142** of the first molding compound **140** is aligned with the sidewall **172** of the second molding compound **170**.

[0065] In the present embodiment, the conductive bumps **162** are configured on the bottom surface **168** of the second semiconductor device **160** to be electrically connected to the first semiconductor device **130**. In order to protect the conductive bumps **162**, the underfill **150** can be configured between the second semiconductor device **160** and the first semiconductor device **130** and between the second semiconductor device **160** and the first molding compound **140** to enclose the conductive bumps **162** of the second semiconductor device **160**. In addition, in the other embodiments, the underfill **150** can be replaced by filling the spaces between the second semiconductor device **160** and the first semiconductor device **130** and between the second semiconductor device **160** and the first molding compound **140** with a portion of the second molding compound **170**.

[0066] In the present embodiment, the first semiconductor device **130** can be configured on the circuit substrate **180** so that the conductive bumps **132** of the first semiconductor device **130** can be electrically connected to the circuit substrate **180**. In order to protect the conductive bumps **132**, the underfill **190** can be configured between the first semiconductor device **130** and the circuit substrate **180** to enclose the conductive bumps **132**.

[0067] Furthermore, in the present embodiment, the third molding compound M can be configured on the circuit substrate **180** to cover the sidewall **142** of the first molding compound **140**, the sidewall **172** of the second molding compound **170** and the top surface **166** of the second semiconductor device **160** away from the first semiconductor device **130**. More clearly, a portion of the third molding compound M is configured on a portion of the second molding compound **170** covering the top surface **166**. That is, the third molding compound M indirectly covers the top surface **166** of the second semiconductor device **160**. In other embodiments, the third molding compound M can cover the sidewall **142** of the first molding compound **140** and the sidewall **172** of the second molding compound **170** to expose the portion of the second molding compound **170** covering the top surface **166** of the second semiconductor device **160**. Moreover, in the other embodiments, the underfills **190** can be replaced by the filling up a space between the first semiconductor device **130** and the circuit substrate **180** with a portion of the third molding compound M.

[0068] Further, the solder balls S are configured on the bottom surface **182** of the circuit substrate **180** away from the first semiconductor device **130**. The solder balls S are electrically connected to the circuit substrate **180**, and the circuit substrate **180** can be electrically connected to the other electronic devices (such as circuit substrate) through the solder balls S.

[0069] FIGS. 2A through 2D are cross-sectional views illustrating a package process according to one embodiment of the present invention.

[0070] In the present embodiment, the processes shown in FIGS. 1A through 1E can be performed first, and then, as shown in FIG. 2A, a second molding compound **210** is formed on the chip array board A. The second molding compound **210** can selectively cover the sidewalls **164** of the second semiconductor devices **160** to expose the top surface **166** of the second semiconductor device **160** away from the first semiconductor device **130** and fill up gaps G2 between the second semiconductor devices **160** to protect the second semiconductor devices **160**.

[0071] Then, as shown in FIG. 2B, the chip array board A is separated from the adhesive layer **120**. Thereafter, as shown in FIG. 2B together with FIG. 2C, the second molding compound **170** and the first molding compound **140** are cut along the filled gaps G2 between the second semiconductor devices **160** to form a plurality of chip package units C2. Then, in the present embodiment, the underfill **190** can be formed on the circuit substrate **180**.

[0072] Moreover, as shown in FIG. 2C together with FIG. 2D, in the present embodiment, one of the aforementioned chip package units C2 can be configured on the circuit substrate **180** so that the first semiconductor device **130** can electrically and structurally connected to the circuit substrate

**180** through the conductive bumps **132** and the underfill **190** is configured between the first semiconductor device **130** of the chip package unit **C2** and the circuit board **180** to enclose the conductive bumps **132** of the first semiconductor device **130**.

[0073] As shown in FIG. 2D, in the present embodiment, a third molding compound **220** is formed on the circuit substrate **180**. The third molding compound **220** can cover the sidewall **W1** of the chip package unit **C2** and expose the top surface **166** of the second semiconductor device **160**. So far, the package structure **200** of the present embodiment is initially formed. Among other embodiments not shown in the drawings, the third molding compound **220** can cover the sidewall **W1** of the chip package unit **C2** and the top surface **166**.

[0074] The details of package structure **200** shown in FIG. 2D are provided hereafter.

[0075] As shown in 2D, the package structure **200** of the present embodiment and the package structure **100** shown in FIG. 1I are similar to each other, and the difference between thereto is that the second molding compound **210** and the third molding compound **220** of the package structure **200** together expose the top surface **166** of the second semiconductor device **160**. Therefore, the package structure **200** can transmit the heat generated by the first semiconductor device **130** and the second semiconductor device **160** under operation to the external environment through the top surface **166** of the second semiconductor device **160**. Thus, the dissipation efficiency of the package structure **200** can be improved.

[0076] Altogether, in the present invention, the first molding compound and the second molding compound are used to secure and connect the first semiconductor devices and the second semiconductor devices, and then the first molding compound and the second molding compound are cut to form the chip package units. Accordingly, the present invention can produce the package structure in which the chips with various dimensions are stacked on one another. Furthermore, since the second molding compound can strengthen the chip array board with a relatively small thickness so that the second semiconductor devices and the first semiconductor devices are securely connected to one another. Therefore, during the cutting process for forming the chip package units, the chip array board can be prevented from being fractured so that the production yield rate can be improved.

[0077] Although the invention has been described with reference to the above embodiments, it will be apparent to one of the ordinary skill in the art that modifications to the described embodiment may be made without departing from the spirit of the invention. Accordingly, the scope of the invention will be defined by the attached claims not by the above

## Claims

1. A package structure, comprising: a first semiconductor device; a second semiconductor device disposed over the first semiconductor device; a plurality of conductive bumps connected to the first semiconductor device and the second semiconductor device; and a molding compound covering both of a lateral surface of the second semiconductor device and a lateral surface of the first semiconductor device, wherein the molding compound extends to under the second semiconductor device.
2. The package structure of claim 1, wherein a thickness of the second semiconductor device is greater than a thickness of the first semiconductor device in a cross-sectional view.
3. The package structure of claim 2, wherein the molding compound laterally covers the plurality of conductive bumps.
4. The package structure of claim 2, wherein a top surface of the second semiconductor device is substantially aligned with a top surface of the molding compound.
5. The package structure of claim 1, further comprising a dielectric layer disposed between the second semiconductor device and the molding compound and contacting the second semiconductor device and the molding compound.

6. The package structure of claim 5, wherein the dielectric layer laterally covers the plurality of conductive bumps.
  7. The package structure of claim 1, wherein the lateral surface of the second semiconductor device does not overlap the lateral surface of the first semiconductor device in a direction substantially perpendicular to a top surface of the molding compound in a cross-sectional view.
  8. The package structure of claim 1, wherein the first semiconductor device includes a through-silicon via (TSV) penetrating the first semiconductor device.
  9. The package structure of claim 8, further comprising a second conductive bump disposed under the first semiconductor device, wherein the second conductive bump is electrically connected to one of the plurality of conductive bumps through the TSV.
  10. The package structure of claim 1, further comprising a circuit substrate disposed below and electrically connected to the first semiconductor device, wherein a projection of the first semiconductor device on the circuit substrate is entirely within a projection of the second semiconductor device on the circuit substrate.
  11. A package structure, comprising: a first semiconductor device; a second semiconductor device disposed over the first semiconductor device; a conductive bump connected to the first semiconductor device and the second semiconductor device; a first non-contact film (NCF) disposed between the first semiconductor device and the second semiconductor device; and a molding compound covering a lateral surface of the second semiconductor device and a lateral surface of the first semiconductor device and laterally overlapping the first NCF.
  12. The package structure of claim 11, wherein a lateral surface of the first NCF is beyond the lateral surface of the first semiconductor device.
  13. The package structure of claim 12, wherein a thickness of the second semiconductor device is greater than a thickness of the first semiconductor device.
  14. The package structure of claim 11, further comprising: a substrate below the first semiconductor device; and a second non-contact film (NCF) between the first semiconductor device and the substrate, wherein a width of the second NCF is greater than a width of the first semiconductor device.
  15. The package structure of claim 11, wherein the lateral surface of the first semiconductor device is free of the first NCF, and wherein the first NCF contacts a top surface of the first semiconductor device.
  16. The package structure of claim 11, wherein the first semiconductor device includes a through-silicon via (TSV) penetrating the first semiconductor device.
  17. A package structure, comprising: a first semiconductor device; a second semiconductor device disposed over the first semiconductor device; a conductive bump connected to the first semiconductor device and the second semiconductor device; a first underfill between the first semiconductor device and the second semiconductor device; a second underfill disposed under the first semiconductor device, wherein at least a portion of the second underfill is spaced apart from a lateral surface of the first semiconductor device; and a molding compound covering a lateral surface of the second semiconductor device and the lateral surface of the first semiconductor device and laterally overlapping the second underfill.
  18. The package structure of claim 17, wherein a width of the second underfill is greater than a width of the first semiconductor device.
  19. The package structure of claim 17, wherein a width of the first underfill is greater than a width of the first semiconductor device.
  20. The package structure of claim 19, wherein the first semiconductor device includes a through-silicon via (TSV) extending from a top surface of the first semiconductor device to a bottom surface of the first semiconductor device, wherein the conductive bump is connected to the TSV and covered by and in contact with the first underfill.
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