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(54) **SEMICONDUCTOR MODULE ARRANGEMENT, ELECTRONICS CARRIER FOR A SEMICONDUCTOR MODULE ARRANGEMENT, AND METHOD FOR PRODUCING A SEMICONDUCTOR MODULE ARRANGEMENT**

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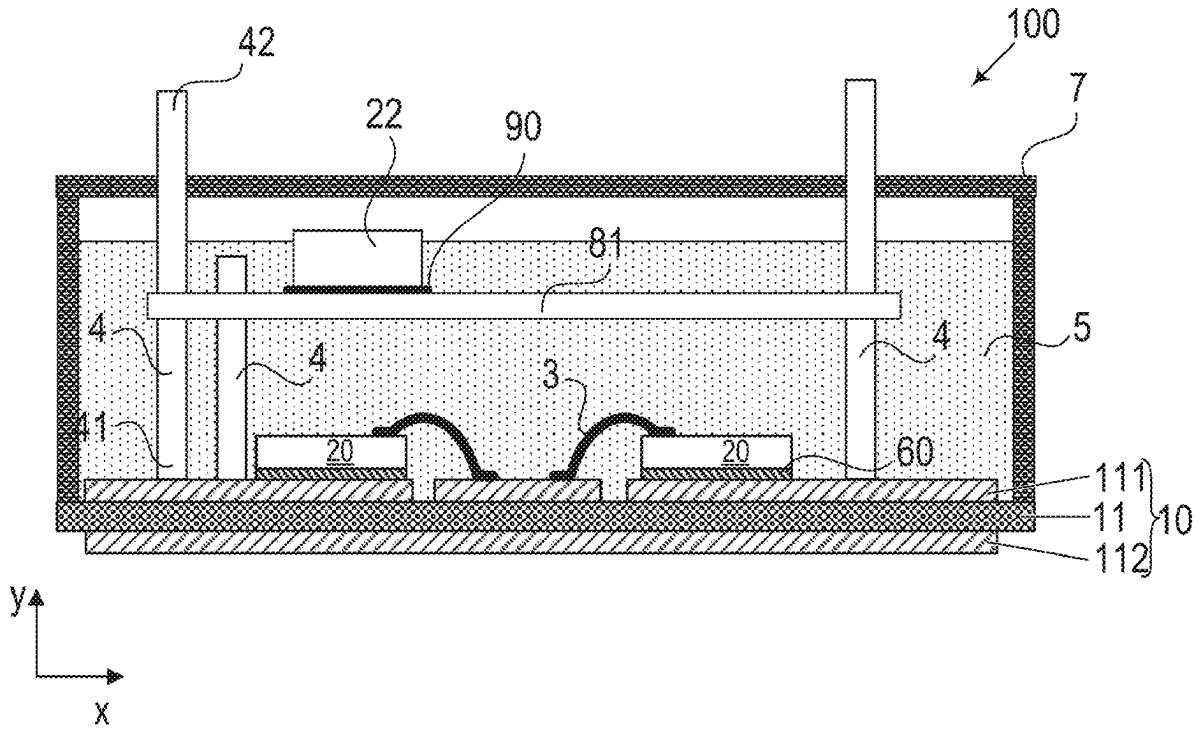
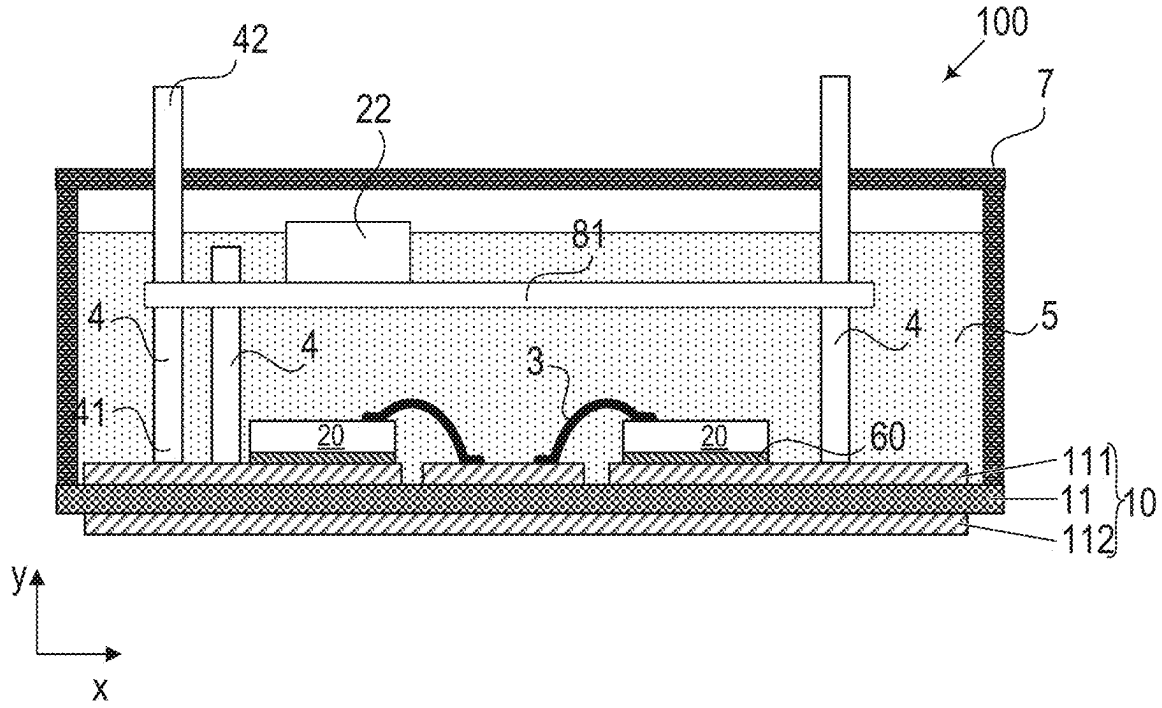
(57) **ABSTRACT**

A semiconductor module arrangement includes a housing, an electronics carrier arranged inside the housing or forming a bottom of the housing, a connector element arranged on and electrically coupled to the electronics carrier, and a sealing gasket surrounding a lower end of the connector element. The lower end is an end of the connector element facing the electronics carrier. The sealing gasket is arranged to seal a gap between the lower end of the connector element and the electronics carrier.




42
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111
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10
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y
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FIG 1

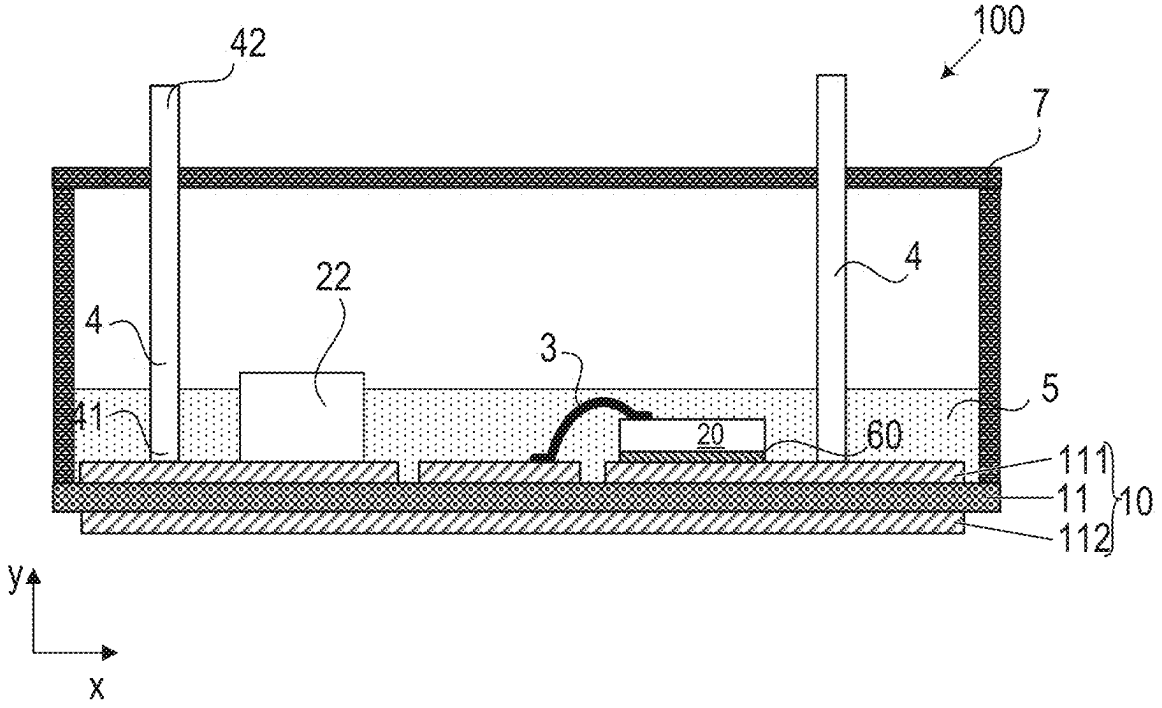
42
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FIG 2

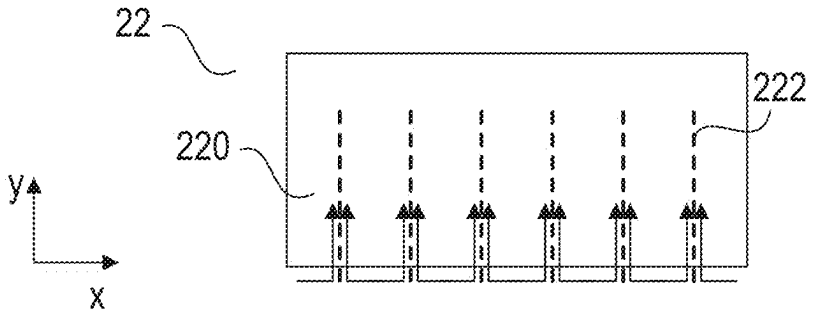


FIG 3

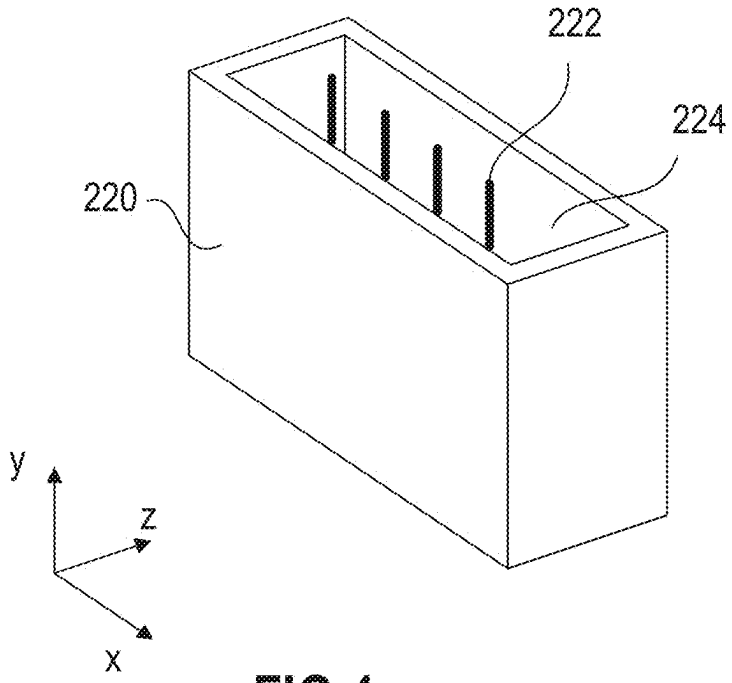


FIG 4

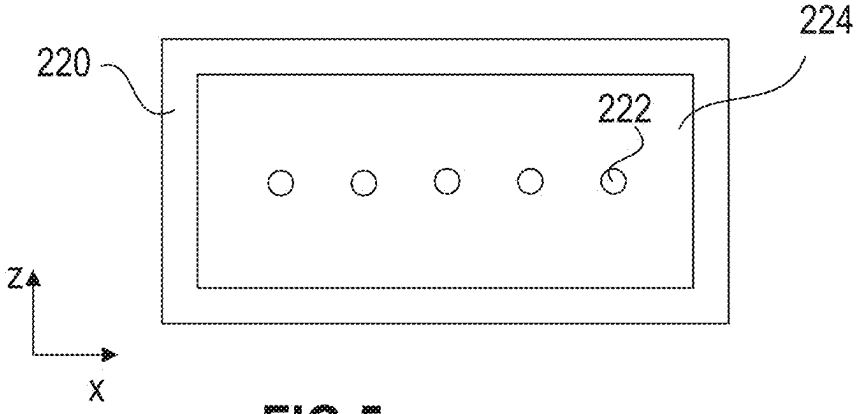


FIG 5

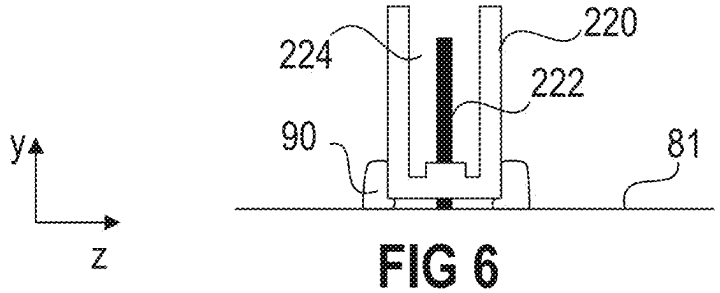


FIG 6

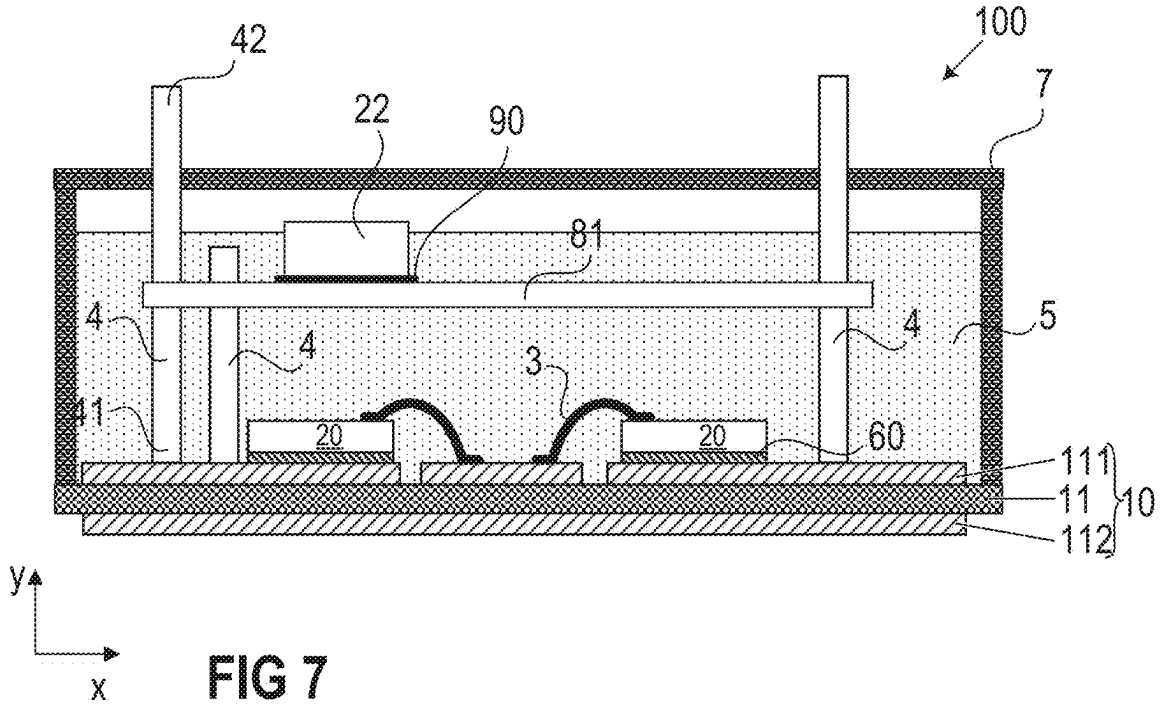


FIG 7

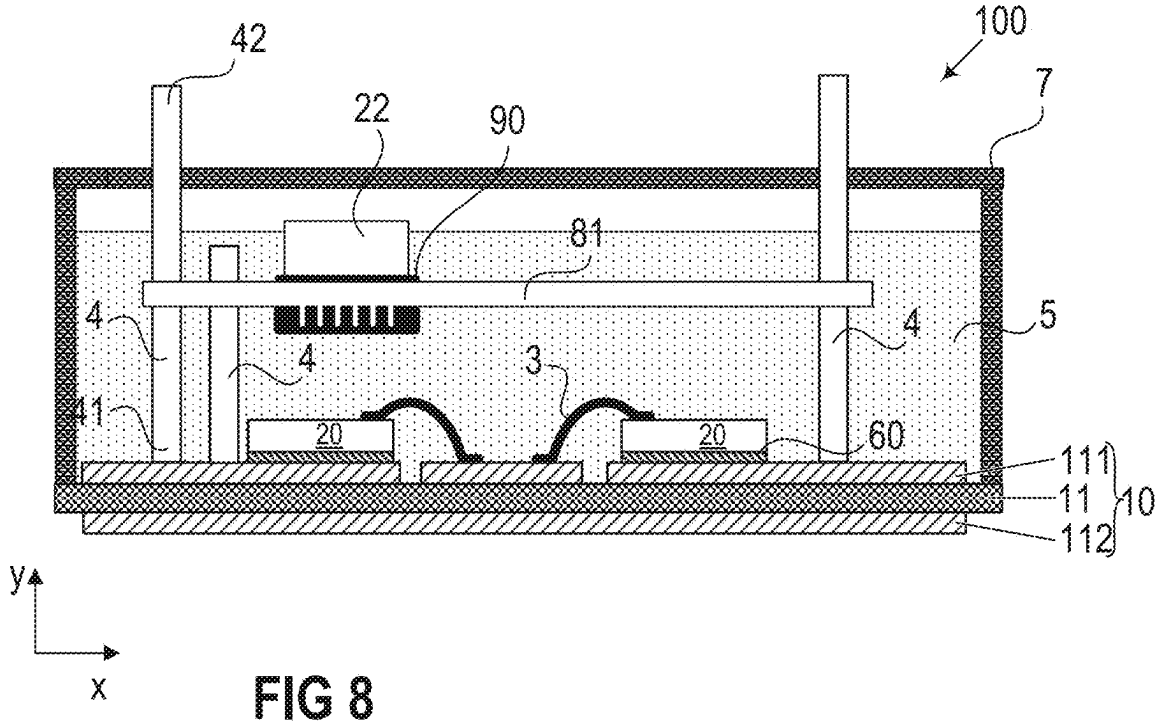


FIG 8

# SEMICONDUCTOR MODULE ARRANGEMENT, ELECTRONICS CARRIER FOR A SEMICONDUCTOR MODULE ARRANGEMENT, AND METHOD FOR PRODUCING A SEMICONDUCTOR MODULE ARRANGEMENT

## TECHNICAL FIELD

**[0001]** The instant disclosure relates to a semiconductor module arrangement, an electronics carrier for a semiconductor module arrangement, and to a method for producing a semiconductor module arrangement.

## BACKGROUND

**[0002]** Semiconductor module arrangements often include at least one semiconductor substrate arranged in a housing. A semiconductor arrangement including a plurality of controllable semiconductor elements (e.g., two IGBTs in a half-bridge configuration) is arranged on each of the at least one substrate. Each substrate usually comprises a substrate layer (e.g., a ceramic layer), a first metallization layer deposited on a first side of the substrate layer and a second metallization layer deposited on a second side of the substrate layer. The controllable semiconductor elements are mounted, for example, on the first metallization layer. The second metallization layer may optionally be attached to a base plate. Some semiconductor module arrangements also include a printed circuit board arranged distant from and in parallel to the substrate. The printed circuit board may also be arranged inside the housing. A plurality of different electrical or electrically conducting components (e.g., semiconductor elements, terminal elements, connection elements, etc.) may be arranged on the substrate and/or on the printed circuit board. One or more connector elements may be arranged on the at least one substrate and/or on the printed circuit board. The one or more connector elements allow to electrically contact the substrate and/or the printed circuit board from the outside of the housing.

**[0003]** Semiconductor module arrangements often also comprise an encapsulant at least partly filling the interior of the housing, thereby covering the substrate and any semiconductor bodies arranged thereon, and also partly covering the one or more connector elements. In order to form the encapsulant, a liquid or viscous encapsulation material is filled into the housing and is subsequently hardened/cured. Before it is sufficiently hardened/cured, the liquid or viscous encapsulation material may penetrate into the one or more connector elements due to capillary effects or adhesion effect. As a result, electrical ports of the one or more connector elements may be at least partly coated by the encapsulation material. When subsequently corresponding counterparts are plugged into the one or more connector elements, any encapsulation material coating the electrical ports may result in a poor electrical connection between the one or more connector elements and their corresponding counterparts, or during the electrical test of the component, the measuring adapter may become contaminated.

**[0004]** There is a need for a semiconductor module arrangement, an electronics carrier for a semiconductor module arrangement, and a method for producing a semiconductor module arrangement which overcome the drawbacks outlined above.

## SUMMARY

**[0005]** A semiconductor module arrangement includes a housing, an electronics carrier arranged inside the housing or forming a bottom of the housing, a connector element arranged on and electrically coupled to the electronics carrier, and a sealing gasket surrounding a lower end of the connector element, wherein the lower end is an end of the connector element facing the electronics carrier, and wherein the sealing gasket is arranged to seal a gap between the lower end of the connector element and the electronics carrier.

**[0006]** An electronics carrier for a semiconductor module arrangement includes a connector element arranged on and electrically coupled to the electronics carrier, and a sealing gasket surrounding a lower end of the connector element, wherein the lower end is an end of the connector element facing the electronics carrier, and wherein the sealing gasket is arranged to seal a gap between the lower end of the connector element and the electronics carrier.

**[0007]** A method includes arranging a connector element on an electronics carrier for a semiconductor module arrangement, forming a sealing gasket such that the sealing gasket surrounds a lower end of the connector element, wherein the lower end is an end of the connector element facing the electronics carrier, and wherein the sealing gasket is arranged to seal a gap between the lower end of the connector element and the electronics carrier.

**[0008]** The invention may be better understood with reference to the following drawings and the description. The components in the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention. Moreover, in the figures, like referenced numerals designate corresponding parts throughout the different views.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0009]** FIG. **1** is a cross-sectional view of a semiconductor module arrangement.

**[0010]** FIG. **2** is a cross-sectional view of another semiconductor module arrangement.

**[0011]** FIG. **3** is a side view of a connector element.

**[0012]** FIG. **4** is a three-dimensional view of a connector element.

**[0013]** FIG. **5** is a top view of a connector element.

**[0014]** FIG. **6** is a cross-sectional view of a connector element and a sealing gasket arranged on a printed circuit board.

**[0015]** FIG. **7** is a cross-sectional view of a semiconductor module arrangement according to embodiments of the disclosure.

**[0016]** FIG. **8** is a cross-sectional view of a semiconductor module arrangement according to further embodiments of the disclosure.

## DETAILED DESCRIPTION

**[0017]** In the following detailed description, reference is made to the accompanying drawings. The drawings show specific examples in which the invention may be practiced. It is to be understood that the features and principles described with respect to the various examples may be combined with each other, unless specifically noted otherwise. In the description, as well as in the claims, designations of certain elements as "first element", "second ele-

ment", "third element" etc. are not to be understood as enumerative. Instead, such designations serve solely to address different "elements". That is, e.g., the existence of a "third element" does not require the existence of a "first element" and a "second element". An electrical line or electrical connection as described herein may be a single electrically conductive element, or include at least two individual electrically conductive elements connected in series and/or parallel. Electrical lines and electrical connections may include metal and/or semiconductor material, and may be permanently electrically conductive (i.e., non-switchable). A semiconductor body as described herein may be made from (doped) semiconductor material and may be a semiconductor chip or be included in a semiconductor chip. A semiconductor body has electrically connecting pads and includes at least one semiconductor element with electrodes.

**[0018]** Referring to FIG. **1**, a cross-sectional view of a semiconductor module arrangement **100** is schematically illustrated. The semiconductor module arrangement **100** includes a housing **7** and an electronics carrier. The electronics carrier is implemented as a substrate **10**. The substrate **10** includes a dielectric insulation layer **11**, a (structured) first metallization layer **111** attached to the dielectric insulation layer **11**, and a (structured) second metallization layer **112** attached to the dielectric insulation layer **11**. The dielectric insulation layer **11** is disposed between the first and second metallization layers **111**, **112**.

**[0019]** Each of the first and second metallization layers **111**, **112** may consist of or include one of the following materials: copper; a copper alloy; aluminum; an aluminum alloy; any other metal or alloy that remains solid during the operation of the semiconductor module arrangement. The substrate **10** may be a ceramic substrate, that is, a substrate in which the dielectric insulation layer **11** is a ceramic, e.g., a thin ceramic layer. The ceramic may consist of or include one of the following materials: aluminum oxide; aluminum nitride; zirconium oxide; silicon nitride; boron nitride; or any other dielectric ceramic. For example, the dielectric insulation layer **11** may consist of or include one of the following materials: $Al_2O_3$, AlN, SiC, BeO or $Si_3N_4$. For instance, the substrate **10** may, e.g., be a Direct Copper Bonding (DCB) substrate, a Direct Aluminum Bonding (DAB) substrate, or an Active Metal Brazing (AMB) substrate. Further, the substrate **10** may be an Insulated Metal Substrate (IMS). An Insulated Metal Substrate generally comprises a dielectric insulation layer **11** comprising (filled) materials such as epoxy resin or polyimide, for example. The material of the dielectric insulation layer **11** may be filled with ceramic particles, for example. Such particles may comprise, e.g., $SiO_2$, $Al_2O_3$, AlN, or BN and may have a diameter of between about 1 μm and about 50 μm. The electronics carrier may also be a conventional printed circuit board (PCB) having a non-ceramic dielectric insulation layer **11**. For instance, a non-ceramic dielectric insulation layer **11** may consist of or include a cured resin.

**[0020]** The substrate **10** is arranged in a housing **7**. In the example illustrated in FIG. **1**, the substrate **10** forms a ground surface of the housing **7**, while the housing **7** itself solely comprises sidewalls and a cover or lid. This is, however, only an example. The cover or lid, for example, may also be omitted. It is also possible that the substrate **10** is arranged on a base plate which forms a ground surface of the housing **7**, or that the housing **7** further comprises a ground surface and the substrate **10** and, optionally, the base plate be arranged inside the housing **7**. In some semiconductor module arrangements **100**, more than one substrate **10** is arranged on a single base plate **12** or on the ground surface of a housing **7**.

**[0021]** One or more semiconductor bodies **20** may be arranged on the at least one substrate **10**. Each of the semiconductor bodies **20** arranged on the at least one substrate **10** may include a diode, an IGBT (Insulated-Gate Bipolar Transistor), a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor), a JFET (Junction Field-Effect Transistor), a HEMT (High-Electron-Mobility Transistor), and/or any other suitable semiconductor element.

**[0022]** The one or more semiconductor bodies **20** may form a semiconductor arrangement on the substrate **10**. In FIG. **1**, only two semiconductor bodies **20** are exemplarily illustrated. The second metallization layer **112** of the substrate **10** in FIG. **1** is a continuous layer. The first metallization layer **111** is a structured layer in the example illustrated in FIG. **1**. "Structured layer" means that the first metallization layer **111** is not a continuous layer, but includes recesses between different sections of the layer. Such recesses are schematically illustrated in FIG. **1**. The first metallization layer **111** in this example includes three different sections. This, however, is only an example. Any other number of sections is possible. Different semiconductor bodies **20** may be mounted to the same or to different sections of the first metallization layer **111**. Different sections of the first metallization layer **111** may have no electrical connection or may be electrically connected to one or more other sections using electrical connections **3** such as, e.g., bonding wires. Electrical connections **3** may also include bonding ribbons, connection plates or conductor rails, for example, to name just a few examples. The one or more semiconductor bodies **20** may be electrically and mechanically connected to the substrate **10** by an electrically conductive connection layer **60**. Such an electrically conductive connection layer **60** may be a solder layer, a layer of an electrically conductive adhesive, or a layer of a sintered metal powder, e.g., a sintered silver powder, for example.

**[0023]** According to other examples, it is also possible that the second metallization layer **112** is a structured layer. It is further possible to omit the second metallization layer **112** altogether. It is generally also possible that the first metallization layer **111** is a continuous layer, for example.

**[0024]** The semiconductor module arrangement **100** illustrated in FIG. **1** further includes terminal elements **4**. A first subset of the terminal elements **4** is electrically connected to the first metallization layer **111** and provides an electrical connection between the inside and the outside of the housing **7**. The terminal elements **4** of the first subset may be electrically connected to the first metallization layer **111** with a first end **41**, while a second end **42** of each of the terminal elements **4** of the first subset protrudes out of the housing **7**. The terminal elements **4** of the first subset may be electrically contacted from the outside of the housing **7** at their respective second ends **42**. A first part of the terminal elements **4** of the first subset may extend through the inside of the housing **7** in a vertical direction y. The vertical direction y is a direction perpendicular to a top surface of the substrate **10**, wherein the top surface of the substrate **10** is a surface on which the at least one semiconductor body **20** is mounted. The terminal elements **4** illustrated in FIG. **1**, however, are only examples. Terminal elements **4** may be implemented in any other way and may be arranged any-

where within the housing **7**. For example, one or more terminal elements **4** may be arranged further away from the sidewalls of the housing **7**. The first end **41** of a terminal element **4** may be electrically and mechanically connected to the substrate **10** by an electrically conductive connection layer, for example (not explicitly illustrated in FIG. **1**). Such an electrically conductive connection layer may be a solder layer, a layer of an electrically conductive adhesive, or a layer of a sintered metal powder, e.g., a sintered silver (Ag) powder, for example. The first end **41** of a terminal element **4** may also be electrically coupled to the substrate **10** via one or more electrical connections **3**, for example.

**[0025]** The semiconductor module arrangement **100** illustrated in FIG. **1** further comprises an additional electronics carrier. The additional electronics carrier in this example is implemented as a printed circuit board **81**. The printed circuit board **81** is arranged inside the housing **7** and may be coupled to the first subset of terminal elements **4** and may be further coupled to a second subset of terminal elements **4**. The second subset of the terminal elements **4** may comprise shorter terminal elements that are arranged entirely inside the housing **7**. The printed circuit board **81** may be electrically and mechanically coupled to the second ends **42** of the terminal elements of the second subset, for example. The first subset of terminal elements **4** may extend from the substrate **10** through a through hole in the printed circuit board **81** to the outside of the housing **7**.

**[0026]** By arranging an additional electronics carrier such as a printed circuit board **81** inside the housing **7**, the semiconductor module arrangement **100** can be implemented in a compact and space saving way, for example. This is, because at least a subset of a plurality of components that is usually arranged on the substrate **10** or on an external printed circuit board (printed circuit board that is arranged outside of the housing **7**) can be arranged on the internal printed circuit board **81** instead of on the substrate **10** or an external printed circuit board. That is, some (or all) components can be arranged on the printed circuit board **81** inside the housing **7**, while others (or none) are arranged on an (optional) external printed circuit board. The size of the substrate **10** and/or an external printed circuit board, therefore, can be reduced as compared to arrangements only comprising a substrate **10**, or a substrate **10** and an external printed circuit board outside the housing **7** but not the printed circuit board **81** inside the housing **7**.

**[0027]** The semiconductor module arrangement **100** further includes an encapsulant **5**. The encapsulant **5** may consist of or include a silicone gel or may be a rigid molding compound, for example. The encapsulant **5** may at least partly fill the interior of the housing **7**, thereby covering the components and electrical connections that are arranged on the substrate **10**. In order to protect the printed circuit board **81** inside the housing **7** and the components arranged on the printed circuit board **81** from certain environmental conditions and mechanical damage, the printed circuit board **81**, optionally, may also be covered by the encapsulant **5**. The terminal elements **4** may be at least partly embedded in the encapsulant **5**. At least the second ends **42** of the first subset, however, are not covered by the encapsulant **5** and protrude from the encapsulant **5** through the housing **7** to the outside of the housing **7**. The encapsulant **5** is configured to protect the components and electrical connections of the semiconductor module **100**, in particular the components arranged on the substrate **10** inside the housing **7**, from certain environmental conditions and mechanical damage.

**[0028]** As has been described above, the substrate **10** and an internal printed circuit board **81** may be electrically coupled to the outside of the housing **7** by means of one or more terminal elements **4**. However, for some applications, one or more connector elements **22** are provided that are configured to form (further) electrical connections to the outside of the housing **7**. In FIG. **1**, one connector element **22** is schematically illustrated, the connector element **22** being arranged on the printed circuit board **81**. Referring to FIG. **2**, a semiconductor module arrangement without a printed circuit board **81** is schematically illustrated. In this case, the connector element **22** is arranged on the substrate **10**. That is, generally speaking, a semiconductor module arrangement according to embodiments of the disclosure comprises a connector element **22** arranged on an electronics carrier (substrate **10** or printed circuit board **81**). In FIGS. **1** and **2**, only one connector element **22** is exemplarily shown. A semiconductor module arrangement, however, may also comprise more than one connector element **22**.

**[0029]** Connector elements **22** often comprise a plurality of electrical ports **222** and an electrically insulating casing **220**, wherein each of the plurality of electrical ports **222** is partly molded into the electrically insulating casing **220**. This is schematically illustrated in FIGS. **3**, **4** and **5**, wherein FIG. **3** shows a side view, FIG. **4** shows a three-dimensional view, and FIG. **5** shows a top view of an exemplary connector element **22**. A connector element **22** may be considered as a kind of socket. A corresponding counterpart may be plugged into the connector element **22** in order to electrically contact the semiconductor module arrangement **100** from outside of the housing **7**. Connector elements **22** are generally comparably simple elements and are often produced by means of injection molding processes. By means of an injection molding process, the electrical ports **222** may be molded into the material forming the casing **220**. The casing **220** may provide a cavity **224** surrounded by sidewalls of the connector element **22**, and the electrical ports **222** may extend into the cavity **224** with a first end. A second end of the electrical ports **222** may extend out of the casing **220** at a lower end (bottom) of the casing **220**, wherein the lower end is an end of the connector element **22** configured to be connected to an electronics carrier **10**, **81**. With the electrical ports **222** extending through the casing **220**, there is a risk that microscopic cavities remain between the electrical ports **222** and the casing **220**. When the encapsulant **5** is formed, a liquid or viscous encapsulation material is filled into the housing **7** and is subsequently hardened to form the encapsulant **5**. Any connector elements **22** arranged on the substrate **10** or the printed circuit board **81** are generally partly covered by encapsulation material. A top side of a connector element **22** generally remains free of encapsulation material such that it may be contacted by a corresponding counterpart. While the encapsulation material is still liquid or viscous, there is a risk that encapsulation material, due to capillary effects, enters the cavity **224** through microscopic cavities between the electrical ports **222** and the casing **220** (indicated by means of arrows in FIG. **3**). Such encapsulation material may at least partly coat the ends of the electrical ports **222** extending into the cavity **224**, which may result in a poor electrical connection between the connector element **22** and a corresponding counterpart.

**[0030]** A semiconductor module arrangement **100** according to embodiments of the disclosure, therefore, comprises a housing **7**, an electronics carrier **10**, **81** arranged inside the housing **7** or forming a bottom of the housing **7**, a connector element **22** arranged on and electrically coupled to the electronics carrier **10**, **81**, and a sealing gasket **90** surrounding a lower end of the connector element **22**, wherein the lower end is an end of the connector element **22** facing the electronics carrier **10**, and wherein the sealing gasket **90** is arranged to seal a gap between the lower end of the connector element **22** and the electronics carrier **10**, **81**. The sealing gasket **90** prevents the encapsulation material, when it is still liquid or viscous, from even reaching any microscopic cavities that may be present in the connector element **22** (e.g., between the electrical ports **222** and the casing **220**). As the electrical ports **222** usually protrude out of the casing **220** on a bottom side of the connector element **22** (the bottom side being the side of the connector element **22** which faces the electronics carrier **10**, **81**), a strand of sealing gasket **90** extending around the entire circumference of the connector element **22** and sealing a gap between the connector element **22** and the electronics carrier **10**, **81** may be sufficient to prevent any encapsulation material from entering into the connector element **22** and contaminating the electrical ports **222**. That is, the sealing gasket **90** may partly cover the sidewalls of the connector element **22** (i.e. of the casing **220**), and may further partly cover the electronics carrier **10**, **81**. This is schematically illustrated in FIG. **6**.

**[0031]** It is also possible that the sealing gasket **90** is partly arranged between the connector element **22** and the electronics carrier **10**, **81**. That is, the material that is used to form the sealing gasket **90** may penetrate into a gap between the lower end of the connector element **22** and the electronics carrier **10**, **81** to a certain degree. This is also schematically illustrated in FIG. **6**.

**[0032]** The material that is used to form the sealing gasket **90**, however, may have different properties as compared to the encapsulation material that is used to form the encapsulant **5**. The sealing gasket **90**, for example, may comprise or consist of one of a silicone glue, an epoxy glue, an acrylic adhesive, a polyimide, and a polyurethane. The material that is used to form the sealing gasket **90**, for example, may be much thicker and much more viscous as compared to the encapsulation material that is used to form the encapsulant **5**. In this way, the material that is used to form the sealing gasket **90** will not penetrate into the connector element **22** (i.e. into the cavity **224**) due to capillary effects.

**[0033]** According to one example, the sealing gasket **90** consists of a first material, the first material having at least one of a dynamic viscosity of between 10 and 100 Pa·s, a tensile shear strength of at least 0.5 MPa, and a hardness of between 30 Shore A and 90 Shore A, or between 9 Shore C and 59 Shore C, or between 6 Shore D and 39 Shore D. A hardness of 30 Shore A defines comparably soft materials such as rubber bands, for example, while 90 Shore A refers to comparably hard materials such as shopping cart wheels, for example. The Shore C scale is usually used for medium hard materials, and the Shore D scale partly covers rubbers and polyurethanes as well as part of known plastics such as, e.g., Teflon, polypropylenes and polystyrenes. The Shore A, Shore C and Shore D scales partly overlap. It would generally also be possible to use the Shore B (e.g., between 15 and 65 Shore B) or Shore 00 scale (e.g., between 65 and 100 Shore 00) in the present case. A hardness of 70 on the Shore A scale, for example, is comparable to a hardness of about 98 on the Shore 00 scale, a hardness of 10 on the Shore B scale, a hardness of 42 on the Shore C scale, or a hardness of 25 on the Shore D scale. Most soft, medium soft and medium hard rubbers have a hardness of between about 20 and about 90 on the Shore A scale.

**[0034]** The first material may be at least one of a thermally cured material, an addition cured material, a condensation cured material, a UV cured material, and a radically cured material, for example. According to one example, the sealing gasket **90** consists of a thixotropic material. Thixotropic materials generally are odd solids and fluids that change their viscosity (that become less viscous) when loaded by stress. The first material may have a saturated connective structure with only few oligomer components included therein such that no or only insignificant amounts of fluids (e.g., water) leak out of the sealing gasket **90**.

**[0035]** The connector element **22** may be attached to, and the sealing gasket **90** may be formed on the electronics carrier **10**, **81** before the electronics carrier **10**, **81** is arranged in a housing **7** of a semiconductor module arrangement **100**. A (pre-produced) electronics carrier **10**, **81** according to embodiments of the disclosure comprises a connector element **22** arranged on and electrically coupled to the electronics carrier **10**, **81**, and a sealing gasket **90** surrounding a lower end of the connector element **22**, wherein the lower end is an end of the connector element **22** facing the electronics carrier **10**, **81**, and wherein the sealing gasket **90** is arranged to seal a gap between the lower end of the connector element **22** and the electronics carrier **10**, **81**. Forming the sealing gasket **90** before arranging the electronics carrier **10**, **81** in a housing **7** generally allows to easily access the electronics carrier **10**, **81**, i.e. the connector element **22** arranged on the electronics carrier **10**, **81**, by means of suitable tools that are required to form the sealing gasket **90**.

**[0036]** A method for producing a semiconductor module arrangement **100** according to embodiments of the disclosure comprises arranging a connector element **22** on an electronics carrier **10**, **81** for a semiconductor module arrangement **100**, and forming a sealing gasket **90** such that the sealing gasket **90** surrounds a lower end of the connector element **22**, wherein the lower end is an end of the connector element **22** facing the electronics carrier **10**, **81**, and wherein the sealing gasket **90** is arranged to seal a gap between the lower end of the connector element **22** and the electronics carrier **10**, **81**.

**[0037]** As has been described above, the connector element **22** may comprise a plurality of electrical ports **222** and an electrically insulating casing **220**, wherein each of the plurality of electrical ports **222** is partly molded into the electrically insulating casing **220**, and arranging the connector element **22** on the electronics carrier **10**, **81** may comprise electrically and mechanically coupling each electrical port **222** of the plurality of electrical ports **222** to the electronics carrier **10**, **81**. For example, the electrical ports **222** may be electrically coupled (e.g., soldered or sintered) to conductive tracks formed on a printed circuit board **81**, or to different sections of a first metallization layer **111** of a substrate **10**.

**[0038]** As mentioned above, the electronics carrier **10**, **81** may be pre-produced. It is, however, also possible that at least the sealing gasket **90** is only formed after the electron-

ics carrier **10**, **81** has been arranged in the housing **7** of the semiconductor module arrangement **100**. A sealing gasket **90** may be formed, for example, by means of a needle valve or a pneumatically or a piezo-controlled jet valve. Such tools are usually able to reach the connector element **22** inside the housing **7**, even if further components are already arranged on the electronics carrier **10**, **81** and space is limited. A curing step may be required in some cases, after forming the sealing gasket **90** on the electronics carrier **10**, **81**.

**[0039]** FIG. **7** schematically illustrates a semiconductor module arrangement **100** according to embodiments of the disclosure. The semiconductor module arrangement **100** comprises a connector element **22** mounted on a first surface of a printed circuit board **81**. Instead of on a printed circuit board **81**, the connector element **22** may also be mounted on another electronics carrier such as a substrate **10**, similar to what has been described with respect to FIG. **2**. Some connector elements **22** comprise electrical ports **222** that extend through corresponding through holes provided in a printed circuit board **81**. That is, the connector element **22** is arranged on a first side of the printed circuit board **81**, and the electrical ports **222** extend from the first side through the printed circuit board **81** to an opposite side of the printed circuit board **81**. This is schematically illustrated in FIG. **8**. In such cases, encapsulation material could also penetrate through the through holes provided in the printed circuit board **81** and from there through microscopic cavities formed between the electrical ports **222** and the casing **220**. In order to prevent this, the sealing gasket **90** may also be applied to a bottom side of the printed circuit board **81**, covering the electrical ports **222** and any gaps formed between the electrical ports **22** and the printed circuit board **81**, as is schematically illustrated in FIG. **8**.

**[0040]** As used herein, the terms "having", "containing", "including", "comprising" and the like are open ended terms that indicate the presence of stated elements or features, but do not preclude additional elements or features. The articles "a", "an" and "the" are intended to include the plural as well as the singular, unless the context clearly indicates otherwise.

**[0041]** The expression "and/or" should be interpreted to include all possible conjunctive and disjunctive combinations, unless expressly noted otherwise. For example, the expression "A and/or B" should be interpreted to mean only A, only B, or both A and B. The expression "at least one of" should be interpreted in the same manner as "and/or", unless expressly noted otherwise. For example, the expression "at least one of A and B" should be interpreted to mean only A, only B, or both A and B.

**[0042]** Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that a variety of alternate and/or equivalent implementations can be substituted for the specific embodiments shown and described without departing from the scope of the present invention. This application is intended to cover any adaptations or variations of the specific embodiments discussed herein. Therefore, it is intended that this invention be limited only by the claims and the equivalents thereof.

What is claimed is:

**1**. A semiconductor module arrangement, comprising:

a housing;

an electronics carrier arranged inside the housing, or forming a bottom of the housing;

a connector element arranged on and electrically coupled to the electronics carrier; and

a sealing gasket surrounding a lower end of the connector element,

wherein the lower end is an end of the connector element facing the electronics carrier,

wherein the sealing gasket is arranged to seal a gap between the lower end of the connector element and the electronics carrier.

**2**. The semiconductor module arrangement of claim **1**, wherein the electronics carrier is a substrate comprising a ceramic substrate layer and a first metallization layer deposited on a first side of the ceramic substrate layer.

**3**. The semiconductor module arrangement of claim **1**, wherein:

the electronics carrier is a printed circuit board;

the semiconductor module arrangement further comprises a substrate arranged inside or forming a bottom of the housing; and

the printed circuit board is arranged inside the housing, vertically above and in parallel to the substrate.

**4**. The semiconductor module arrangement of claim **1**, further comprising:

an encapsulant at least partly filling an interior of the housing, such that the encapsulant covers the electronics carrier and the sealing gasket and partly covers the connector element.

**5**. The semiconductor module arrangement of claim **1**, wherein the connector element comprises a plurality of electrical ports and an electrically insulating casing, and wherein each of the plurality of electrical ports is partly molded into the electrically insulating casing.

**6**. The semiconductor module arrangement of claim **1**, wherein the sealing gasket comprises or consists of one of a silicone glue, an epoxy glue, an acrylic adhesive, a polyimide, and a polyurethane.

**7**. The semiconductor module arrangement of claim **1**, wherein the sealing gasket consists of a first material, the first material having at least one of:

a dynamic viscosity of between 10 and 100 Pa·s;

a tensile shear strength of at least 0.5 MPa; and

a hardness of between 30 Shore A and 90 Shore A, or between 9 Shore C and 59 Shore C, or between 6 Shore D and 39 Shore D.

**8**. The semiconductor module arrangement of claim **7**, wherein the first material is at least one of a thermally cured material, an addition cured material, a condensation cured material, a UV cured material, and a radically cured material.

**9**. The semiconductor module arrangement of claim **1**, wherein the sealing gasket consists of a thixotropic material.

**10**. The semiconductor module arrangement of claim **1**, wherein the sealing gasket is partly arranged between the connector element and the electronics carrier.

**11**. An electronics carrier for a semiconductor module arrangement, the electronics carrier comprising:

a connector element arranged on and electrically coupled to the electronics carrier; and

a sealing gasket surrounding a lower end of the connector element,

wherein the lower end is an end of the connector element facing the electronics carrier,

wherein the sealing gasket is arranged to seal a gap between the lower end of the connector element and the electronics carrier.

**12**. A method, comprising:

arranging a connector element on an electronics carrier for a semiconductor module arrangement;

forming a sealing gasket such that the sealing gasket surrounds a lower end of the connector element, wherein the lower end is an end of the connector element facing the electronics carrier, and wherein the sealing gasket is arranged to seal a gap between the lower end of the connector element and the electronics carrier.

**13**. The method of claim **12**, wherein the sealing gasket is formed by a needle valve or a pneumatically or a piezo-controlled jet valve.

**14**. The method of claim **12**, wherein the connector element comprises a plurality of electrical ports and an electrically insulating casing, wherein each of the plurality of electrical ports is partly molded into the electrically insulating casing, and wherein arranging the connector element on the electronics carrier comprises electrically and mechanically coupling each electrical port of the plurality of electrical ports to the electronics carrier.

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