United States Patent Application Publication	20250266843
Kind Code	A1
Publication Date	August 21, 2025
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ANALOG-TO-DIGITAL CONVERTER AND IMAGE SENSOR INCLUDING THE SAME

Abstract

An image sensor includes a counter circuit that outputs a count value corresponding to a magnitude of a pixel signal. The counter circuit includes a first counter circuit that latches a counting code to generate at least one least significant bit signal of a count value; and a second counter circuit that generates most significant bit signals sequentially toggling in response to one of the at least one least significant bit signal or an inversion signal of the one of the at least one least significant bit signal. The first counter circuit includes a plurality of latch circuits and an addition circuit. The second counter circuit is arranged between the plurality of latch circuits along a first virtual line connecting a comparator and the plurality of latch circuits.

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Family ID: **1000008421739**

Appl. No.: **19/024232**

Filed: **January 16, 2025**

Foreign Application Priority Data

KR	10-2024-0025253	Feb. 21, 2024

Publication Classification

Int. Cl.: **H03M1/34** (20060101); **H04N25/78** (20230101)

U.S. Cl.:

CPC **H03M1/34** (20130101); **H04N25/78** (20230101);

Background/Summary

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0001] This application claims priority under 35 U.S.C. § 119 to Korean Patent Application No. 10-2024-0025253 filed on Feb. 21, 2024, in the Korean Intellectual Property Office, the disclosure of which is incorporated by reference herein in its entirety.

BACKGROUND

[0002] Embodiments of the present disclosure described herein relate to an analog-to-digital converter and a complementary metal oxide semiconductor (CMOS) image sensor, and more particularly, relate to an analog-to-digital converter that converts a pixel signal of an image sensor into a digital signal and an image sensor including the same.

[0003] An image sensor, which is a device that converts an optical signal into an electrical signal, includes a charge coupled device (CCD) image sensor and a complementary metal oxide semiconductor (CMOS) image sensor.

[0004] The analog-to-digital converter (ADC) of an image sensor converts an analog pixel signal into a counting value which is a digital signal. The ADC may be arranged for each column or pixel.

[0005] While power usage increases due to an increase in the number of pixels of an image sensor, the importance of low-power driving capability for a mobile environment has also increased. In other words, it is also important to reduce the power consumed by the ADC.

SUMMARY

[0006] Embodiments of the present disclosure provide an ADC and an image sensor that operate at low power.

[0007] Embodiments of the present disclosure provide an ADC and an image sensor with reduced power consumption and maximum current.

[0008] According to an embodiment, an image sensor includes a pixel array including a plurality of pixels, each pixel configured to output a pixel signal; a comparator that generates a comparison signal based on a ramp signal and the pixel signal; a counter circuit that receives a counting code and the comparison signal and outputs a count value corresponding to a magnitude of the pixel signal based on the comparison signal; and a control circuit that controls the plurality of pixels, the comparator, and the counter circuit, wherein the counter circuit includes a first counter circuit that latches the counting code to generate at least one least significant bit signal of the count value; and a second counter circuit that generates most significant bit signals sequentially toggling in response to one of the at least one least significant bit signal or an inversion signal of the one of the at least one least significant bit signal. The first counter circuit includes a plurality of latch circuits and an addition circuit. The second counter circuit is arranged between the plurality of latch circuits along a first virtual line connecting the comparator and the plurality of latch circuits. The image sensor may be formed on a substrate including a front surface and a back surface opposite to the front surface. The first virtual line may be parallel to the front surface or the back surface of the substrate.

[0009] According to an embodiment, an image sensor includes a pixel array including a plurality of pixels; a plurality of column lines that outputs pixel voltages of the plurality of pixels; a plurality of comparators connected to each of the plurality of column lines, and each configured to generate a comparison signal based on a ramp signal and a pixel voltage; and a plurality of counter circuits that receives the comparison signal from each of the plurality of comparators and outputs a count value corresponding to the pixel voltage based on the comparison signal, wherein each of the plurality of counter circuits includes a first latch circuit that latches a gray code, a second latch circuit that latches a first binary code among outputs of the first latch circuit; a most significant bit counter circuit that receives an output of a most significant bit among the outputs of the first latch

circuit and counts high-order n bits of the count value, n is an integer of 1 or more; and an arithmetic unit that performs an operation on a second binary code among the outputs of the first latch circuit and the first binary code. The gray code corresponds to lower-order m bits of the count value, m is an integer of 1 or more. The most significant bit counter circuit is arranged such that a first distance between the first latch circuit and the most significant bit counter circuit is smaller than a second distance between the first latch circuit and the second latch circuit.

[0010] According to an embodiment, an image sensor includes a pixel array including a plurality of pixels, each pixel configured to output a pixel signal, and an analog-to-digital converter configured to convert the pixel signal into pixel data. The analog-to-digital converter includes a comparator that generates a comparison signal based on a ramp signal and an input signal; and a counter circuit that receives a counting code and the comparison signal and outputs a count value corresponding to a magnitude of the input signal based on the comparison signal. The counter circuit includes a first counter circuit including a plurality of latch circuits and an adder, and configured to latch the counting code, and generate least significant bit signals of the count value; and a second counter circuit that generates most significant bit signals sequentially toggling in response to one of the least significant bit signals or an inversion signal of the one of the least significant bit signals. The plurality of latch circuits, the adder, and the second counter circuit are arranged in series, and the second counter circuit is arranged between the plurality of latch circuits.

[0011] The ADC and image sensor according to the present disclosure may reduce power consumption and maximum current.

Description

BRIEF DESCRIPTION OF THE FIGURES

[0012] The above and other objects and features of the present disclosure will become apparent by describing in detail embodiments thereof with reference to the accompanying drawings.

[0013] FIG. **1** is a block diagram illustrating an image sensor according to an embodiment of the present disclosure.

[0014] FIGS. **2**A and **2**B are diagrams illustrating pixels of an image sensor according to embodiments of the present disclosure.

[0015] FIG. **3**A is a diagram illustrating an ADC of an image sensor according to embodiments of the present disclosure.

[0016] FIG. **3**B illustrates a configurable ADC compared to the ADC of FIG. **3**A according to an embodiment of the present disclosure.

[0017] FIG. **4** is a block diagram illustrating a first counter circuit according to an embodiment of the present disclosure.

[0018] FIG. **5** is a circuit diagram illustrating an example of a first latch circuit according to an embodiment of the present disclosure.

[0019] FIG. **6** is a circuit diagram illustrating an example of a second latch circuit according to an embodiment of the present disclosure.

[0020] FIG. **7** is a circuit diagram illustrating an example of a second counter circuit according to an embodiment of the present disclosure.

[0021] FIG. **8** is a timing diagram illustrating the operation of the second counter circuit of FIG. **7** for correlated double sampling (CDS) according to example embodiments.

[0022] FIG. **9** is a timing diagram illustrating the operation of the ADC of FIG. **3**A for correlated double sampling according to example embodiments.

[0023] FIG. **10** is a diagram illustrating an ADC of an image sensor according to an embodiment.

[0024] FIG. **11** is a block diagram of an image sensor according to an embodiment of the present disclosure.

[0025] FIG. **12** is a block diagram of an image sensor according to an embodiment of the present disclosure.
[0026] FIG. **13** is a block diagram of an electronic device according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0027] Hereinafter, embodiments of the present disclosure will be described clearly and in detail so that those skilled in the art can easily carry out embodiments of the present disclosure.
[0028] FIG. **1** is a block diagram illustrating an image sensor **100** according to an embodiment of the present disclosure.
[0029] The image sensor **100** may be used for an image device. The image device may be an electronic device such as a digital camera, a smartphone, a wearable device, Internet of Things (IoT), a tablet computer, a personal computer (PC), a personal digital assistant (PDA), a portable multimedia player (PMP), a navigation device, or the like. In addition, the image device may be an electronic device provided as accessory equipment included in a vehicle, a manufacturing facility, a door, various measuring devices, or the like.
[0030] The image sensor **100** may generate image data IDT, which is visual information of an object imaged through a lens, and provide the generated image data IDT to an image signal processor (ISP: not shown). The image signal processor may be implemented to process the image data IDT generated from the image sensor **100** and output the processed image data to a display device or store the processed image data in a storage device.
[0031] The image signal processor may demosaic an image signal according to a pixel pattern through interpolation, perform color correction, adjust a dynamic range, or reduce noise through filtering or the like. The image signal processor may additionally perform other schemes of improving image quality. Some logic of the image signal processor may be arranged in the image sensor **100**, and other logic may be arranged in an application processor (AP) outside the image sensor **100**.
[0032] The image sensor **100** may include a pixel array **110**, a row driver **120**, a timing controller **130**, a ramp signal generator **140**, a counting code generator **150**, an ADC **160**, and an output buffer **190**.
[0033] For example, the image sensor **100** may be formed in and on a substrate. The substrate may include a front surface and a back surface opposite to the front surface.
[0034] The pixel array **110** includes a plurality of pixels PXs. For example, the plurality of pixels PXs may be arranged in the pixel array **110** in a matrix form along a plurality of columns and a plurality of rows. The plurality of columns and plurality of rows may be parallel to the front surface and/or back surface of the substrate. Each pixel PX may be electrically connected to one row line and one column line among the plurality of row lines and the plurality of column lines CLI to CLp, p may be a natural number equal to or greater than2.
[0035] In an embodiment, each pixel PX may include a plurality of transistors controlled by the row driver **120**. Alternatively, in another embodiment, two or more pixels PXs adjacent to each other may form one pixel group, and two or more pixels PXs included in the pixel group may share at least some of a transmission transistor, a driving transistor, a selection transistor, and a reset transistor with each other.
[0036] Each of the plurality of pixels PXs may include a photoelectric conversion element that converts an incident optical signal into an electrical signal. Each pixel PX may include at least one photoelectric conversion element.
[0037] The photoelectric conversion element may be a photodiode (PD). The photoelectric conversion element may include at least one of a photodiode (PD), a photocapacitor, photogate, a pinned photodiode (PPD), a partially pinned photodiode, an organic photodiode diode (OPD), a quantum dot (QD), and any combination thereof. Embodiments of the present disclosure are described on the premise that the photoelectric conversion element is a photodiode (PD), but other

photoelectric conversion elements described above may be used and are not limited to the photodiode (PD).
[0038] The pixel array **110** may receive a plurality of pixel driving signals CS**1** to CSq, q may be a natural number equal to or greater than 2, such as a selection signal for controlling a selection transistor, a reset signal for controlling a reset transistor, a transmission transistor control signal for controlling a transmission transistor, and the like. Each of the plurality of pixels of the pixel array **110** operates under control of the received pixel driving signals CS**1** to CSq.
[0039] The row driver **120** may drive the plurality of rows of the pixel array **110** under control of the timing controller **130**. The row driver **120** may generate a selection signal for driving one of the plurality of rows. The row driver **120** may activate pixels corresponding to the selected row. Pixel signals PXS of pixels of the selected row may be transmitted to the ADC **160** through the plurality of column lines CL**1** to CLp. The pixel signals PXS generated from each pixel of the row selected by the selection signal of the row driver **120** may be transmitted to the ADC **160** through the column line corresponding to each pixel.
[0040] The pixel signal PXS may include a reset voltage signal and a pixel voltage signal. The pixel voltage signal may be a voltage of a floating diffusion region corresponding to charges generated from at least one photodiode (PD) included in each of the plurality of pixels. The reset voltage signal may be a voltage of a floating diffusion region that does not reflect charges generated from the photodiode (PD).
[0041] The timing controller **130** may control the pixel array **110**, the row driver **120**, the ramp signal generator **140**, the counting code generator **150**, and the ADC **160**. The timing controller **130** may provide a timing control signal TC to the row driver **120**. The timing controller **130** may control the ramp signal generator **140** through a ramp control signal CS_RP and control the ADC **160** through an ADC control signal CS_ADC. The ramp control signal CS_RP may include a lamp enable signal, and the like.
[0042] The ramp signal generator **140** may generate a ramp signal RAMP in response to the ramp enable signal. The ramp signal generator **140** may generate the ramp signal RAMP having a preset slope. The ramp signal generator **140** may provide the generated ramp signal RAMP to the ADC **160**.
[0043] The ADC **160** may include a comparator **170** and a counter circuit **180**. The ADC **160** may convert each of the reset voltage signal and the pixel voltage signal of the pixel signal PXS into pixel data PXD, which is a digital signal, based on the ramp signal RAMP and output the converted pixel data PXD. For example, the ADC **160** may convert the reset voltage signal and the pixel voltage signal into digital signals based on the ramp signal RAMP in a correlated double sampling (CDS) scheme, respectively and output the difference between the reset voltage signal and the pixel voltage signal as the pixel data PXD, which is a digital signal. The pixel data may be a counting value corresponding to the magnitude of the pixel signal PXS.
[0044] The counter circuit **180** according to an embodiment of the present disclosure may include a plurality of counter circuits. One of the plurality of counter circuits may be arranged between circuits constituting another counter circuit. The plurality of counter circuits may include a first counter circuit and a second counter circuit.
[0045] The first counter circuit may generate the least significant bits (LSBs) among the bits constituting the counting value, and the second counter circuit may generate the most significant bits (MSBs) among the bits constituting the counting value. The least significant bits may be composed of least significant bit signals, which are bit signals generated by the first counter circuit.
[0046] The second counter circuit may include a ripple counter that generates most significant bit signals by sequentially toggling in response to one of the least significant bit signals generated from the first counter circuit. Accordingly, the most significant bit signal corresponding to the least significant bit among the most significant bit signals generated from the second counter circuit may use the most significant bit of the least significant bit signals received from the first counter circuit

as a clock signal. In this case, in order to provide the most significant bit of the least significant bit signals from the first counter circuit to the second counter circuit, the supply current may increase for each period of the provided least significant bit signal.

[0047] In the counter circuit **180** according to an embodiment of the present disclosure, the second counter circuit may be arranged between circuits constituting the first counter circuit. Accordingly, the most significant bit signal of the least significant bit signals generated from the first counter circuit and provided to the second counter circuit may be provided to the second counter circuit through a short path. As a result, the maximum value of the supply current provided to the second counter circuit may be reduced. In addition, the power consumed in the counter circuit **180** may be reduced. In particular, when the number of bits generated from the first counter circuit is smaller than the number of bits generated from the second counter circuit, the logic of the signal provided to the second counter circuit may transition more frequently, thereby increasing the power consumed by the counter circuit. In this case, the counter circuit **180** according to an embodiment of the present disclosure may reduce the power consumption of the counter circuit **180** because the signal provided to the second counter circuit is transmitted through a short path.

[0048] According to an embodiment of the present disclosure, the output buffer **190** may include a memory **191** and a sense amplifier **192**. The memory **191** may include a plurality of static random access memory (SRAM) cells. For example, the pixel data PXD from the counter circuit **180** of the ADC **160** may be stored in the SRAM cells of the memory **191**. The sense amplifier **192** may amplify the pixel data PXD stored in the memory **191** and output the amplified pixel data PXD as the image data IDT.

[0049] FIGS. **2**A and **2**B are diagrams illustrating pixels of an image sensor according to embodiments of the present disclosure. Each pixel PXa and PXb of FIGS. **2**A and **2**B may correspond to the pixel PX of the image sensor **100** of FIG. **1**.

[0050] Referring to FIG. **2**A, the pixel PXa may include a photoelectric conversion element PD, a transmission transistor TX, a floating diffusion node FD, a reset transistor RX, a driving transistor DX, and a selection transistor SX.

[0051] The photoelectric conversion element PD may generate photo charges corresponding to incident light.

[0052] The transmission transistor TX electrically connects the photoelectric conversion element PD to the floating diffusion node FD based on a transmission transistor control signal TG. When the transmission transistor TX is turned on, photo charges of the photoelectric conversion element PD electrically connected to the floating diffusion node FD may move to the floating diffusion node FD.

[0053] The reset transistor RX may electrically connect the floating diffusion node FD and a power supply voltage node VDD. The reset transistor RX may reset the floating diffusion node FD at the voltage level of the power supply voltage node VDD by a reset control signal RS provided from the row driver **120** of FIGS. **1** and **2**. FIG. **2**A illustrates that the reset voltage is provided from the power supply voltage node VDD, but according to an embodiment, the reset voltage may be provided from a voltage node having a voltage level other than the power supply voltage node VDD.

[0054] The driving transistor DX is driven with a driving voltage provided through the power supply voltage node VDD. The driving transistor DX may output an output voltage Vout corresponding to the charges accumulated in the floating diffusion node FD. The driving transistor DX may output the output voltage Vout to the column line CLi through the selection transistor SX.

[0055] The reset voltage signal output after connection of the floating diffusion node FD by the reset transistor RX and the pixel voltage signal output after the photo charges of the photoelectric conversion element PD moves to the floating diffusion node FD may be output to the column line CLi as the output voltage Vout, respectively.

[0056] The ADC **160** in FIG. **1** may generate a counting value corresponding to the magnitude of

each of the reset voltage signal and the pixel voltage signal output to the column line CLi, and may output the difference as pixel data PXD. In this case, among the plurality of counter circuits of the ADC **160** of FIG. **1**, the counter circuit that generates the least significant bits of the counting value may include at least two latch circuits including a latch circuit for storing the reset voltage signal and a latch circuit for storing the pixel voltage signal.

[0057] Referring to FIG. **2**B, unlike the pixel PXa of FIG. **2**A, the pixel PXb may further include a gain control transistor CGX and a capacitor Cp between the reset transistor RX and the floating diffusion node FD. The capacitor Cp may be a parasitic capacitor formed by the source terminal/drain terminal of the gain control transistor CGX. Alternatively, the capacitor Cp may be a passive element having a fixed or variable capacitance. The gain control transistor CGX may be turned on or off in response to a gain control signal CGS to selectively provide the capacitance of the capacitor Cp to the floating diffusion node FD, thereby providing a plurality of gain modes. In this case, according to an embodiment, among the plurality of counter circuits of the ADC **160** in FIG. **1**, the counter circuit that generates the least significant bits of the counting value may include two latch circuits or three or more latch circuits.

[0058] FIGS. **3**A and **3**B are diagrams illustrating ADCs of an image sensor. The ADC in FIG. **3**A illustrates the ADC of an image sensor according to an embodiment of the present disclosure. The ADC in FIG. **3**A may correspond to the ADC **160** of the image sensor **100** in FIG. **1**. FIG. **3**B illustrates a configurable ADC compared to the ADC **160** of FIG. **3**A according to an embodiment of the present disclosure. The ADC **160** according to an embodiment of the present disclosure will be described with reference to FIGS. **1**, **3**A and **3**B.

[0059] The ADC **160** according to an embodiment of the present disclosure may be arranged in plurality to correspond to the plurality of columns of the image sensor **100**, respectively.

[0060] The ADC **160** may include the comparator (COMP) **170**, a plurality of latch circuits **181** and **185**, an addition circuit **183**, and a second counter circuit **187**. The plurality of latch circuits may include the first latch circuit **181** and the second latch circuit **185**.

[0061] The plurality of latch circuits **181** and **185** and the addition circuit **183** may constitute a first counter circuit. The first counter circuit **181**, **183** and **185** may generate least significant bit signals corresponding to the least significant bits of the pixel data PXD, which is a counting value, and the second counter circuit **187** may generate a most significant bit signal corresponding to the most significant bit of the pixel data PXD. The second counter circuit **187** may be called a most significant bit (MSB) counter circuit.

[0062] The pixel signal PXS may be provided to the comparator **170** through one column line CLi of the plurality of column lines CL**1** to CLp of the image sensor **100** in FIG. **1**. The pixel signal PXS may be one of a reset voltage signal or a pixel voltage signal. The ramp signal RAMP generated from the ramp signal generator **140** may be provided to the comparator **170**.

[0063] The comparator **170** may compare the ramp signal RAMP and the pixel signal PXS and provide a comparison signal CDS based on the comparison result of the two signals to the first latch circuit **181** of the first counter circuit. When the level of the ramp signal RAMP is equal to the level of the pixel signal PXS, the comparator **170** may output the comparison signal CDS that transitions from a first level (e.g., logic high) to a second level (e.g., logic low). The time point at which the level of the comparison signal CDS transitions may be determined according to the level of the pixel signal PXS.

[0064] The first latch circuit **181** may additionally receive a counting code generated by the counting code generator **150**. In an embodiment, the counting code may be a gray code. For example, a gray code whose code value changes over time may be provided to the first latch circuit **181** as a counting code CCD. The counting code CCD may include m-bit data CCD[m−**1**:**0**], m is a positive integer of 2 or more.

[0065] The first latch circuit may include a plurality of latches. For example, the first latch circuit may include “m” latches corresponding to m-bit data CCD[m−**1**:**0**]. Each bit of the m-bit data

CCD[m−**1**:**0**] of the counting code CCD may be simultaneously latched in "m" latches of the first latch circuit.

[0066] In an embodiment, after converting m-bit data CCD[m−**1**:**0**] of the latched counting code CCD into an m-bit binary code B[m−**1**:**0**], the first latch circuit **181** may output the converted binary code B[m−**1**:**0**]. The most significant bit B[m−**1**] of the binary code B[m−**1**:**0**] may be the same as the most significant bit signal among the least significant bit signals output from the first counter circuit **181**, **183** and **185**. The most significant bit B[m−**1**] of the binary code B[m−**1**:**0**] may be provided to the second counter circuit **187** through a first line LN**1**. The first line LN**1** may be a line connecting the first latch circuit **181** and the second counter circuit **187**. The binary code B[m−**1**:**0**] may be provided to the addition circuit **183** through a second line LN**2**. The addition circuit **183** may include a plurality of full-adders. The second line LN**2** may be a line connecting the first latch circuit **181** and the addition circuit **183**.

[0067] The second latch circuit **185** may store a first binary code that is a counting value of the pixel signal PXS corresponding to the reset voltage signal among the pixel signals PXS. The first binary code may be provided from the addition circuit **183** to the second latch circuit **185** through a third line LN**3_1**. Alternatively, according to an embodiment, the second latch circuit **185** may store the first binary code, which is a counting value of the pixel signal PXS corresponding to the pixel voltage signal among the pixel signals PXS. In an embodiment, the second latch circuit **185** may store the complement of the first binary code, which is a counting value of the pixel signal PXS corresponding to the reset voltage signal.

[0068] The addition circuit **183** may add the first binary code corresponding to the reset voltage signal stored in the second latch circuit **185** and the second binary code corresponding to the pixel voltage signal stored in the first latch circuit **181**. The second latch circuit **185** may provide the first binary code to the addition circuit **183** through a third line LN**3_2**. The least significant bit signals resulting from the addition may be output as part of the pixel data PXD through a first switch SW**1**.

[0069] The second counter circuit **187** may generate most significant bit signals which sequentially toggle based on the most significant bit B[m−**1**] or the inverted value of the most significant bit B[m−**1**] received from the first latch circuit **181** through the first line LN**1**. In an embodiment, the second counter circuit **187** may include a plurality of flip-flops connected to each other in cascade, and the flip-flop located at the forefront among the plurality of flip-flops may receive the most significant bit B[m−**1**] or the inverted value of the most significant bit B[m−**1**] as a clock signal. After counting is completed, the second counter circuit **187** may output the toggled most significant bit signals through a second switch SW**2** as part of the pixel data PXD.

[0070] Referring to FIG. **3**A, the comparator **170**, the first latch circuit **181**, the second counter circuit **187**, the addition circuit **183**, and the second latch circuit **185** of the ADC **160** may be arranged in a row in the order mentioned. For example, the comparator **170** may be arranged closest to the pixel array **110**, and the second latch circuit **185** may be arranged furthest from the pixel array **110**. When providing a plurality of gain modes and including three or more latch circuits, the remaining latch circuits may be arranged in a row behind the second latch circuit **185**. The comparator **170**, the first latch circuit **181**, the second counter circuit **187**, the addition circuit **183**, and the second latch circuit **185** of the ADC **160** may be arranged in a row in parallel with the column line CLi. When comparing a first distance P**1** which is the distance between the first latch circuit **181** and the second counter circuit **187**, a second distance P**2** which is the distance between the first latch circuit **181** and the second latch circuit **185**, and a third distance P**3** which is the distance between the first latch circuit **181** and the addition circuit **183**, the third distance P**3** may be longer than the first distance P**1**, and the second distance P**2** may be longer than the third distance P**3**.

[0071] In an embodiment, when assuming a first virtual line (not shown) connecting the comparator **170**, the first latch circuit **181**, the second counter circuit **187**, the addition circuit **183**, and the second latch circuit **185** of the ADC **160**, the first virtual line may be parallel to the column

line CLi. The first virtual line may be parallel to the front or back surface of the substrate. The substrate may include the front or back surface with an axis in a first direction D**1** and a second direction D**2**, and the substrate may have a depth toward the inside of the substrate in a third direction D**3** perpendicular to the first direction D**1** and the second direction D**2**. For example, the front or back surface of the substrate may extend in the first direction D**1** or the second direction D**2**.

[0072] Alternatively, when assuming the first virtual line (not shown) connecting the comparator **170**, the first latch circuit **181**, the addition circuit **183**, and the second latch circuit **185** of the ADC **160**, the second counter circuit **187** may be arranged between the first latch circuit **181** and the addition circuit **183** along the first virtual line.

[0073] At least a portion of the first line LN**1**, the second line LN**2**, and the third lines LN**3_1** and LN**3_2** may be formed inside the substrate. The lines in FIGS. **3**A and **3**B conceptually show the connection relationship between components, and the illustrations of the lines in FIGS. **3**A and **3**B may not necessarily be the same as the physical locations of the lines. For example, at least a portion of the second line LN**2** in FIG. **3**A may not be located at the same depth in the substrate as the second counter circuit **187**. Accordingly, in an embodiment, because the second line LN**2** connects the first latch circuit **181** and the addition circuit **183**, and the first latch circuit **181**, the second counter circuit **187** and the addition circuit **183** are arranged in line in the mentioned order, at least a portion PT**1** of the second line LN**2** may be located further inside (e.g., close to the back surface of the substrate) the substrate than the second counter circuit **187**. For example, when assuming a second virtual line (not shown) perpendicular to the front or back surface of the substrate, the second virtual line may pass through at least the portion PT**1** of the second line LN**2** and the second counter circuit **187**. Alternatively, when the substrate is viewed parallel to the second virtual line (when the substrate is viewed perpendicular to the front or back surface of the substrate), at least the portion PT**1** of the second line LN**2** and the second counter circuit **187** may be arranged to overlap.

[0074] Accordingly, the first line LN**1** connecting the first latch circuit **181** and the second counter circuit **187** may be shorter than the second line LN**2** connecting the first latch circuit **181** and the addition circuit **183**. As a result, the most significant bit signal B[m−**1**] provided to the second counter circuit **187** among the binary code B[m−**1**:**0**] may pass through a very short path and be provided to the second counter circuit **187**. For example, the parasitic capacitance of the first line LN**1** may be reduced so that IR drop is reduced, thereby reducing the power consumed for transmission of the most significant bit signal B[m−**1**].

[0075] In contrast to the ADC **160** according to an embodiment of the present disclosure described with reference to FIG. **3**A, the ADC arranged in each column in the image sensor may be exemplarily configured as the ADC in FIG. **3**B.

[0076] The ADC of FIG. **3**B may include a plurality of counter circuits. The plurality of counter circuits may include a first counter circuit LSB_CNT and a second counter circuit R**187**. The first counter circuit LSB_CNT of FIG. **3**B may correspond to the first counter circuits **181**, **183** and **185** of FIG. **3**A, and the second counter circuit R**187** of FIG. **3**B may correspond to the second counter circuit **187** of FIG. **3**A. A first latch circuit R**181**, an addition circuit R**183**, and a second latch circuit R**185** in FIG. **3**B may correspond to the first latch circuit **181**, the addition circuit **183**, and the second latch circuit **185** in FIG. **3**A, respectively. A first line RLN**1**, a second line RLN**2**, and third lines RLN**3_1** and RLN**3_2** in FIG. **3**B may correspond to the first line LN**1**, the second line LN**2**, and the third lines LN**3_1** and LN**3_2** in FIG. **3**A.

[0077] Referring to FIG. **3**B, the exemplary ADC may include the first latch circuit R**181**, the addition circuit R**183**, the second latch circuit R**185**, and the second counter circuit R**187** that are arranged in order of proximity to a comparator R**170** that receives the pixel signal PXS from the column line CLi. That is, according to the ADC of FIG. **3**B, when comparing a first distance RP**1** which is the distance between the first latch circuit R**181** and the second counter circuit **187**, a

second distance RP**2** which is the distance between the first latch circuit R**181** and the second latch circuit R**185**, and a third distance RP**3** which is the distance between the first latch circuit R**181** and the addition circuit R**183**, the second distance RP**2** may be longer than the third distance RP**3**, and the first distance RP**1** may be longer than the second distance RP**2**. As a result, the most significant bit signal B[m−**1**] of the binary code B[m−**1**:**0**] may be provided to the second counter circuit R**187** via a very long path. As a result, the parasitic capacitance of the first line RLN**1** may increase so that IR drop increases, thereby increasing the power consumed for transmission of the most significant bit signal B[m−1].

[0078] FIG. **4** is a block diagram illustrating a first counter circuit according to an embodiment of the present disclosure. The block diagram of FIG. **4** may include a first latch circuit **181**, a second latch circuit **185**, and an addition circuit **183**. The first latch circuit **181**, the second latch circuit **185**, and the addition circuit **183** in FIG. **4** may correspond to the first latch circuit **181**, the second latch circuit **185**, and the addition circuit **183** in FIG. **3**A, respectively.

[0079] The first latch circuit **181** may receive the comparison signal CDS and the counting code CCD. The counting code CCD may be a code whose value increases over time. In an embodiment, the counting code CCD may be a gray code. The counting code CCD may be m-bit. The comparison signal CDS may indicate the result of comparing the pixel signal PXS and the ramp signal RAMP by the comparator **170** in FIG. **3**A. The first latch circuit **181** may latch the counting code CCD at a time point when the comparison signal CDS transitions to a low level. For example, the first latch circuit **181** may latch the counting code CCD based on the comparison signal CDS at a plurality of time points when the pixel signal PXS corresponds to the levels of each of the reset voltage signal and the pixel voltage signal.

[0080] The first latch circuit **181** may convert the latched m-bit counting code CCD into an m-bit binary code B[m−**1**:**0**]. The most significant bit signal B[m−**1**] of the converted binary code B[m−**1**:**0**] may be provided to the second counter circuit **187** in FIG. **3**A. FIG. **4** is a block diagram conceptually explaining the operation of the first counter circuit **181**, **183**, and **185**. The second counter circuit **187**, not shown, may be arranged between the first latch circuit **181** and the addition circuit **183**.

[0081] The first latch circuit **181** may provide the converted binary code B[m−**1**:**0**] as the first binary code to the addition circuit **183**. For example, the first binary code may correspond to the level of the reset voltage signal.

[0082] In a state where the second latch circuit **185** is reset, the addition circuit **183** may complement the first binary code corresponding to the level of the received reset voltage signal and store the complement of the first binary code through a second flip-flop **183_3** in the second latch circuit **185**.

[0083] In an embodiment, the addition circuit **183** may include an adder **183_1**, a first flip-flop **183_2**, and the second flip-flop **183_3**.

[0084] The addition circuit **183** may receive a second binary code corresponding to the level of the pixel voltage signal from the first latch circuit **181**. The addition circuit **183** may add the second binary code and the complement of the first binary code stored in the second latch circuit **185** and output an added result SUM through the second flip-flop **183_3**. The added result SUM may be output through the first switch SW**1**. The added result SUM may constitute a least significant bit PXD[m−**1**:**0**] of the pixel data.

[0085] In an embodiment, the addition circuit **183** may be implemented including the 1-bit adder **183_1**, where the adder **183_1** may receive and add the complement of the first binary code corresponding to the level of the negative reset voltage signal and the second binary code one bit at a time in order from the least significant bit. The carry generated by addition may be stored in the flip-flop **183_2** and provided to the adder **183_1** when adding the next bit. According to an embodiment, the addition circuit **183** may include a plurality of 1-bit adders.

[0086] FIG. **5** is a circuit diagram illustrating an example of a first latch circuit according to an

embodiment of the present disclosure. The circuit diagram of FIG. **5** may include a first latch circuit **181**, an addition circuit **183**, and a second counter circuit **187**. The first latch circuit **181**, the addition circuit **183**, and the second counter circuit **187** in FIG. **5** may correspond to the first latch circuit **181**, the addition circuit **183**, and the second counter circuit **187** in FIG. **3**A, respectively.
[0087] The first latch circuit **181** may include a plurality of latches **181_1** to **181_5** and a gray code-binary code conversion circuit **181_6**.
[0088] The first latch circuit **181** may receive the counting code CCD from the counting code generator **150**. FIG. **5** illustrates, as an example, that the counting code CCD includes a 5-bit counting code CCD[**0**] to CCD[**4**] and the first latch circuit **181** includes five latches **181_1** to **181_5**, but the number of bits of the counting code CCD and the number of latches included in the first latch circuit **181** may vary according to an embodiment.
[0089] Each of the plurality of latches **181_1** to **181_5** may receive a counting code (e.g., a gray code) generated from the counting code generator **150** one bit at a time through an input signal port "D". Each of the plurality of latches **181_1** to **181_5** may latch the gray code received based on the comparison signal CDS applied to an enable port EN, or transmit the gray code to the gray code-binary code conversion circuit **181_6** through an output port "Q".
[0090] The gray code-binary code conversion circuit **181_6** may convert the gray code received from the plurality of latches **181_1** to **181_5** into a binary code B[**4**:**0**], provide the most significant bit signal B[**4**] to the second counter circuit **187**, and provide the converted binary code B[**4**:**0**] to the addition circuit **183**.
[0091] The second counter circuit **187** may sequentially toggle based on the bit signal B[**4**] to output n-bit most significant bit signals PXD[**4**+n−**1**:**4**] of the pixel data through the second switch SW**2**. The addition circuit **183** may output 5-bit least significant bit signals PXD[**4**:**0**] of the pixel data through the first switch SW**1**.
[0092] FIG. **5** illustrates that each of the plurality of latches **181_1** to **181_5** receives a counting code (e.g., a gray code) in parallel one bit at a time, but in another embodiment, each of the plurality of latches **181_1** to **181_5** may be connected in cascade to serially receive a counting code (e.g., a gray code) one bit at a time. In this case, each of the plurality of latches **181_1** to **181_5** may receive the output of the previous latch as an input.
[0093] FIG. **6** is a circuit diagram illustrating an example of a second latch circuit according to an embodiment of the present disclosure. The circuit diagram of FIG. **6** may include an addition circuit **183** and a second latch circuit **185**. Each of the addition circuit **183** and the second latch circuit **185** in FIG. **6** may correspond to the addition circuit **183** and the second latch circuit **185** in FIG. **3**A.
[0094] The second latch circuit **185** may include a plurality of latches **185**_L**1** to **185**_L**5** and a plurality of buffers **185**_B**1** to **185**_B**5**. The plurality of latches **185**_L**1** to **185**_L**5** may receive and latch the first binary code B[m−**1**:**0**] corresponding to the level of the reset voltage signal provided from the first latch circuit **181** through the addition circuit **183**.
[0095] In an embodiment, the plurality of latches **185**_L**1** to **185**_L**5** may be connected to each other in cascade. Among the two interconnected latches, the output port "Q" of the front latch may be connected to the input signal port "D" of the rear latch through a signal line. Accordingly, the value transmitted to each of the plurality of latches **185**_L**1** to **185**_L**5** may be bypassed sequentially through the plurality of latches **185**_L**1** to **185**_L**5** connected in series to each other by control of enable signals EN**1** to EN**5** input to each of the plurality of latches **185**_L**1** to **185**_L**5**. As a result, the least significant bit B[**0**] of the first binary code B[m−**1**:**0**] may be stored in the latch **185**_L**1** among the plurality of latches **185**_L**1** to **185**_L**5**, and the most significant bit signal B[m−**1**] may be stored in the latch **185**_L**5** among the plurality of latches **185**_L**1** to **185**_L**5**.
[0096] Referring to FIG. **6**, the plurality of latches **185**_L**1** to **185**_L**5** are connected to each other in cascade, but according to an embodiment, the plurality of latches may be arranged in parallel.
[0097] Each of the plurality of buffers **185**_B**1** to **185**_B**5** may receive and store values transmitted

from each of the plurality of latches **185**_L**1** to **185**_L**5**. Each of the plurality of buffers **185**_B**1** to **185**_B**5** may include a 3-phase inverter. Each 3-phase inverter may store values received from each of the plurality of buffers **185**_B**1** to **185**_B**5** or output the stored values based on a control signals C**1** to C**5** provided from an outside. The control signals Cl to C**5** may be provided from the timing controller **130** in FIG. **1**.

[0098] The first binary code B[m−**1**:**0**] corresponding to the level of the reset signal stored in each of the plurality of buffers **185**_B**1** to **185**_B**5** may be provided to the addition circuit **183** based on the control signals C**1** to C**5**.

[0099] FIG. **7** is a circuit diagram illustrating an example of a second counter circuit according to an embodiment of the present disclosure. A second counter circuit **187** of FIG. **7** may correspond to the second counter circuit **187** of FIG. **3**A.

[0100] The second counter circuit **187** according to an embodiment of the present disclosure may include a plurality of flip-flops **187**_**1** to **187**_n. The second counter circuit **187** may include an asynchronous ripple counter in which one flip-flop is triggered by an input clock signal. In an embodiment, each of the plurality of flip-flops **187**_**1** to **187**_n may be implemented with a D-flip-flop that is triggered on the falling edge of a clock signal.

[0101] The first flip-flop **187**_**1** may receive the most significant bit signal B[m−**1**] provided from the first latch circuit **181** as a clock signal, and the remaining flip-flops **187**_**2** to **187**_n may be connected to the output port "Q" of the front flip-flop. Toggling of the output ports "Q" and "/Q" of each of the plurality of flip-flops **187**_**1** to **187**_n occurs at the falling edge of the input clock signal. The inverting output port "/Q" is connected to the data input port "D" of each of the plurality of flip-flops **187**_**1** to **187**_n. Therefore, the plurality of flip-flops **187**_**1** to **187**_n are synchronized with the falling edge of the clock signal to output bits PXD[m], PXD[m+1], . . . , and PXD[m+n−1] that repeat toggling. Accordingly, the plurality of flip-flops **187**_**1** to **187**_n may generate n-bit signals PXD[m], PXD[m+**1**], . . . , and PXD[m+n−**1**], n is an integer greater than 1, which are toggled sequentially in response to the most significant bit signal B[m−**1**] among the outputs (e.g., a binary code B[m−**1**:**0**]) of the first latch circuit **181** in FIG. **3**A. For example, the second counter circuit **187** may count the most significant n bits of the plurality of pixel data PXD.

[0102] Basically, each of the plurality of flip-flops **187**_**1** to **187**_n includes a D-flip-flop that is triggered at the falling edge of a signal provided to a clock input terminal CLK.

[0103] The second counter circuit **187** according to an embodiment of the present disclosure may include the plurality of flip-flops **187**_**1** to **187**_n with an inverting function.

[0104] For example, each of the plurality of flip-flops **187**_**1** to **187**_n may receive a clock signal from multiplexers MX_**1** to MX_n. Each of the multiplexers MX_**1** to MX_n may output one of the clock signal and an inversion instruction signal INV**2** received under control of an inversion control signal INV**1**. Each of the multiplexers MX_**1** to MX_n may select the inversion instruction signal INV**2** as an output when the inversion control signal INV**1** transitions to logic high. Each of the plurality of flip-flops **187**_**1** to **187**_n may be triggered at the falling edge of the inversion instruction signal INV**2** to invert the stored value. According to an embodiment, the inversion function of the second counter circuit **187** may be implemented in different manners.

[0105] In an embodiment, the second counter circuit **187** may be toggled by the most significant bit signal B[m−1] of the first binary code B[m−**1**:**0**], and may invert and store the values of the most significant bit signals PXD[m], PXD[m+**1**], . . . , and PXD[m+n−**1**] corresponding to the level of the reset voltage signal for which counting has been completed based on the inversion instruction signal INV**2**. The second counter circuit **187** may toggle sequentially again by the most significant bit signal B[m−**1**] of the second binary code B[m−**1**:**0**] from the most significant bit signals PXD[m], PXD[m+**1**], . . . , and PXD[m+n−**1**] corresponding to the level of the inverted and stored (i.e., negative converted to **1**'s complement) reset signal. As a result, a count-up corresponding to the level of the pixel voltage signal may be performed, and finally, the most significant bit signal of the pixel data corresponding to the difference between the pixel voltage signal and the reset voltage

signal may be output. According to an embodiment, the second counter circuit **187** may be implemented as an up/down counter. In this case, the second counter circuit **187** may perform an up-count of the pixel voltage signal after the down-count of the reset voltage signal is completed.

[0106] FIG. **8** is a timing diagram illustrating the operation of the second counter circuit **187** of FIG. **7** for correlated double sampling (CDS) according to example embodiments. FIG. **8** will be illustrated assuming that the most significant bit signals PXD[m], PXD[m+**1**], . . . , and PXD[m+n−**1**] generated by the second counter circuit **187** are 4-bit signals.

[0107] Referring to FIG. **8**, the second counter circuit **187** may invert the counting value corresponding to the level of the reset voltage signal to take the complement, and performs counting corresponding to the level of the pixel voltage signal, thereby performing correlated double sampling.

[0108] At time point T**0**, the most significant bit signal B[m−**1**] among the outputs of the first latch circuit **181** of FIG. **3**A may be input.

[0109] At time point T**1**, as the level of the bit signal B[m−**1**] transitions to low, among the most significant bit signals PXD[m], PXD[m+**1**], PXD[m+**2**] and PXD[m+**3**], the 0-th bit signal PXD[m] may transition to level high.

[0110] At time point T**2**, as the bit signal B[m−**1**] transitions to level low, the 0-th bit signal PXD[m] may transition to level low, and accordingly, the first bit signal PXD[m+**1**] may transition to level low.

[0111] Similar to the time point T**2**, at time point T**3**, as the first bit signal PXD[m+**1**] transitions to level low, the second bit signal PXD[m+**2**] may transition to level high. In addition, at time point T**4**, as the second bit signal PXD[m+**2**] transitions to level low, the third bit signal PXD[m+**3**] may transition to level high.

[0112] Counting corresponding to the level of the reset voltage signal may end at the time point T**4**, and in this state, when the inversion control signal INV**1** transitions to logic high at time point T**5**, the inversion instruction signal INV**2** may transition to logic low at time point T**6**. Triggered by the inversion instruction signal INV**2** transitioned to logic low, the most significant bit signals PXD[m], PXD[m+**1**], PXD[m+**2**], and PXD[m+**3**] are inverted and stored by the count value corresponding to the level of the reset voltage signal.

[0113] At time point T**7**, the most significant bit signal B[m−**1**] among the outputs of the first latch circuit **181** corresponding to the level of the pixel voltage signal may be received again, and correlated double sampling may be performed by performing counting based on the most significant bit signal B[m−**1**] corresponding to the level of the received pixel voltage signal.

[0114] FIG. **9** is a timing diagram illustrating the operation of the ADC **160** of FIG. **3**A for correlated double sampling according to example embodiments. The operation of the ADC **160** will be described with reference to FIGS. **1**, **3**A, and **9**.

[0115] After one row of the pixel array **110** of FIG. **1** is selected, the ADC **160** may be initialized in response to an auto-zero signal AZS at time point T**0**.

[0116] At time point T**1**, the ramp signal RAMP may rise to a specified level, and at time point T**2**, the ramp signal RAMP may fall at a specified level. The comparison signal CDS may transition to logic high and remain in a logic high state until time point T**3**, when it reaches a first decision point DP**1** where a pixel signal VPixel corresponding to the reset voltage signal is equal to the ramp signal RAMP.

[0117] At the time point T**2**, the counting code CCD may be provided to the ADC **160**, and the first counter circuit (least significant bit counter) may count the counting code CCD while the comparison signal CDS remains logic high. The second counter circuit (most significant bit counter) may sequentially perform toggling based on the most significant bit signal B[m−**1**] provided from the first counter circuit.

[0118] At time point T**3**, the comparison signal CDS may transition to logic low.

[0119] At time point T**4**, the ramp signal RAMP may rise again to a specified level and the first

counter circuit and the second counter circuit may end counting and may temporarily store a counting value RST corresponding to the level of the reset voltage signal.
[0120] At time point T**5**, the inversion instruction signal INV**2** may transition to logic low by the inversion control signal INV**1** of logic high. The second counter circuit may invert the stored value and store it by the inversion instruction signal INV**2**.
[0121] At time point T**6**, the ramp signal RAMP may fall steadily again. The comparison signal CDS may transition back to logic high and remain in a logic high state until at time point T**7** when the pixel signal VPixel corresponding to the pixel voltage signal reaches a second decision point DP**2** where the pixel signal VPixel is equal to the ramp signal RAMP.
[0122] At the time point T**7**, the comparison signal CDS may transition to logic low, and the first counter circuit and the second counter circuit may reflect a counting value SIG corresponding to the level of the pixel voltage signal in the counting value RST corresponding to the level of the reset voltage signal, thereby outputting pixel data.
[0123] FIG. **10** is a diagram illustrating an ADC **160***a* of an image sensor according to an embodiment. The ADC **160***a* of FIG. **10** may correspond to the ADC **160** of the image sensor **100** of FIG. **1**. The ADC **160***a* according to an embodiment of the present disclosure will be described with reference to FIGS. **1**, **3**A, and **10**. Detailed descriptions of parts that overlap or are similar to the ADC **160** previously described with reference to FIG. **3**A will be omitted and the differences will be mainly described.
[0124] Referring to FIG. **10**, unlike the ADC **160** of FIG. **3**A, the ADC **160***a* may include the comparator **170**, the first latch circuit **181**, the addition circuit **183**, the second counter circuit **187**, and the second latch circuit **185** which are arranged in line in order. That is, the comparator **170** may arranged closest to the pixel array **110** and the second latch circuit **185** may be arranged furthest from the pixel array **110**, which is the same as the ADC **160** in FIG. **3**A, but the addition circuit **183** may be arranged adjacent to the first latch circuit **181**.
[0125] The first latch circuit **181**, the addition circuit **183**, the second counter circuit **187**, and the second latch circuit **185** may be arranged in line in the order mentioned along the direction parallel to the column line CLi. When comparing a first distance P**1** which is the distance between the first latch circuit **181** and the second counter circuit **187**, a second distance P**2** which is the distance between the first latch circuit **181** and the second latch circuit **185**, and a third distance P**3** which is the distance between the first latch circuit **181** and the addition circuit **183**, the first distance P**1** may be longer than the third distance P**3**, and the second distance P**2** may be longer than the first distance P**1**. That is, compared to the ADC **160** of FIG. **3**A, the first distance P**1**, which is the distance between the first latch circuit **181** and the second counter circuit **187**, may be longer than that of the ADC **160** of FIG. **3**A, and the third distance P**3**, which is the distance between the first latch circuit **181** and the addition circuit **183**, may decrease. Nevertheless, power consumption may be reduced because the first distance P**1** is shorter than the first distance RP**1** which is the distance between the first latch circuit R**181** and the second counter circuit R**187** in FIG. **3**B.
[0126] In an embodiment, when assuming a first virtual line (not shown) connecting the comparator **170**, the first latch circuit **181**, the addition circuit **183**, the second counter circuit **187**, and the second latch circuit **185** arranged in series in the ADC **160***a*, the first virtual line may be parallel to the column line CLi and the first direction D**1**. The first virtual line may be parallel to the front or back surface of the substrate.
[0127] Alternatively, when assuming a second virtual line (not shown) connecting the comparator **170**, the first latch circuit **181**, the addition circuit **183**, and the second latch circuit **185** of the ADC **160***a*, the second counter circuit **187** may be arranged along the second virtual line and between the addition circuit **183** and the second latch circuit **185**.
[0128] At least a portion of the first line LN**1**, the second line LN**2**, and the third lines LN**3_1** and LN**3_2** may be formed inside the substrate, and at least a portion PT**2** of the third lines LN**3_1** and LN**3_2** connecting the addition circuit **183** and the second latch circuit **185** may be located further

inside the substrate than the second counter circuit **187**. That is, when assuming a third virtual line (not shown) perpendicular to the front or back surface of the substrate, the third virtual line may pass through at least the portion PT**2** of the third lines LN**3_1** and LN**3_2** and the second counter circuit **187**. Alternatively, when the substrate is viewed parallel to the third virtual line (when the substrate is viewed perpendicular to the front or back surface of the substrate), at least the portion PT**2** of the third lines LN**3_1** and LN**3_2** and the second counter circuit **187** may be arranged to overlap.

[0129] FIG. **11** is a block diagram of an image sensor **100***a* according to an embodiment of the present disclosure. Detailed descriptions of parts that overlap with those described previously will be omitted.

[0130] The image sensor **100***a* may include a first chip **10***a* and a second chip **20***a* stacked.

[0131] For example, the first chip **10***a* may be stacked on the second chip **20***a* in a direction D**3** perpendicular to the plane of a substrate. The first chip **10***a* and the second chip **20***a* may be electrically connected to each other. For example, the first chip **10***a* and the second chip **20***a* may transmit a pixel signal or a control signal through a through silicon via TSV between pads located in a peripheral area of the chip. The first chip **10***a* and the second chip **20***a* may also be electrically connected through an in-pixel contact IN_CT inside a pixel PXc. For example, the in-pixel contact may be a Cu-to-Cu (C2C) bonding contact. The pixel signal (or pixel data) of the first chip **10***a* may be transmitted to the read circuit (or image signal processing logic) of the second chip **20***a*.

[0132] There may be a plurality of pixels PXc in the pixel array, which is arranged in the pixel array in a matrix form.

[0133] The second chip **20***a* may include logic such as a read circuit, a timing controller, and image signal processing logic, and the like, and an interface circuit. The read circuit may include an ADC according to an embodiment of the present disclosure.

[0134] The second chip **20***a* according to an embodiment of the present disclosure may include one of the ADCs **160** and **160***a* described above. Alternatively, some circuits of the ADCs **160** and **160***a* may be arranged on the first chip **10***a*, and other circuits of the ADCs **160** and **160***a* may be arranged on the second chip **20***a*.

[0135] FIG. **12** is a block diagram of an image sensor **100***b* according to an embodiment of the present disclosure. Detailed descriptions of parts that overlap with those described previously will be omitted.

[0136] Referring to FIG. **12**, the image sensor **100***b* may further include a third chip **30***b* in addition to a first chip **10***b* and a second chip **20***b*. The third chip **30***b*, the second chip **20***b*, and the first chip **10***b* may be sequentially stacked in the direction D**3** perpendicular to the plane of the substrate. The third chip **30***b* may include a memory device. For example, the third chip **30***b* may include a volatile memory device such as dynamic random access memory (DRAM), synchronous random access memory (SRAM) or the like. The third chip **30***b* may receive signals from the first chip **10***b* and the second chip **20***b* and process the signals through a memory device.

[0137] The second chip **20***b* according to an embodiment of the present disclosure may include one of the ADCs **160** and **160***a* described above. Alternatively, some circuits of the ADCs **160** and **160***a* may be arranged on the first chip **10***b*, and other circuits of the ADCs **160** and **160***a* may be arranged on the second chip **20***b*.

[0138] FIG. **13** is a block diagram of an electronic device according to an embodiment of the present disclosure. Detailed descriptions of parts that overlap with those described previously will be omitted.

[0139] An electronic device **1000** may include an imaging unit **1100**, an image sensor **1200**, and a processor **1300**. The electronic device **1000** may perform autofocusing based on phase data provided from the image sensor **1200** to the processor **1300**.

[0140] The processor **1300** may control overall operations of the electronic device **1000**. The processor **1300** may control the position of a lens **1110** by providing a control signal to a lens

actuator **1120**. As a result, the focal distance may be controlled.
[0141] The imaging unit **1100**, which is a component that receives light, may include the lens **1110** and the lens actuator **1120**. The lens **1110** may include a plurality of lenses.
[0142] The lens actuator **1120** may move the lens **1110** in a direction in which the distance from an object "S" increases or decreases based on a control signal from the processor **1300**.
[0143] The image sensor **1200** may generate image data and phase data based on incident light. The image sensor **1200** may include a pixel array **1210**, a timing controller **1220**, an ADC **1230**, and an image signal processor **1240**.
[0144] Pixels of the pixel array **1210** may include at least one photoelectric conversion element.
[0145] The ADC **1230** according to an embodiment of the present disclosure may include one of the ADCs **160** and **160***a* described above. For example, a most significant bit counter constituting the ADC **1230** may be arranged between a plurality of latches constituting a least significant bit counter.
[0146] The processor **1300** may perform a disparity operation using phase data. The processor **1300** may provide a control signal based on the disparity operation result to the lens actuator **1120** to move the position of the lens **1110**.
[0147] The processor **1300** may provide an operation mode control signal INFO_MD to the timing controller **1220**. The timing controller **1220** may control the operation of the pixel array **1210** based on the operation mode control signal INFO_MD.
[0148] While the inventive concept has been particularly shown and described with reference to embodiments thereof, it will be understood that various changes in form and details may be made therein without departing from the spirit and scope of the present invention as set forth in the following claims.

Claims

1. An image sensor comprising: a pixel array including a plurality of pixels, each pixel configured to output a pixel signal; a comparator configured to generate a comparison signal based on a ramp signal and the pixel signal; a counter circuit configured to receive a counting code and the comparison signal and output a count value corresponding to a magnitude of the pixel signal based on the comparison signal; and a control circuit configured to control the plurality of pixels, the comparator, and the counter circuit, wherein the counter circuit includes: a first counter circuit configured to latch the counting code and generate at least one least significant bit signal of the count value; and a second counter circuit configured to generate most significant bit signals sequentially toggling in response to one of the at least one least significant bit signal or an inversion signal of the one of the at least one least significant bit signal, wherein the first counter circuit includes a plurality of latch circuits and an addition circuit, wherein the second counter circuit is arranged between the plurality of latch circuits along a first virtual line connecting the comparator and the plurality of latch circuits, wherein the image sensor is formed on a substrate including a front surface and a back surface opposite to the front surface, and wherein the first virtual line is parallel to the front surface or the back surface of the substrate.
2. The image sensor of claim 1, wherein the first counter circuit includes: a first latch circuit configured to latch the counting code corresponding to the at least one least significant bit signal, convert the latched counting code into a binary code, and output the binary code; a second latch circuit configured to latch a first binary code among outputs of the first latch circuit; and the addition circuit configured to add a second binary code among the outputs of the first latch circuit and the first binary code latched by the second latch circuit, and wherein the second counter circuit is arranged between the first latch circuit and the second latch circuit along the first virtual line.
3. The image sensor of claim 2, wherein: the addition circuit is configured to receive the second binary code through a first line connected to the first latch circuit and receive the first binary code

through a second line connected to the second latch circuit, the second counter circuit is configured to receive one of the at least one least significant bit signal from the first latch circuit through a third line, and a length of one of the first line and the second line is longer than a length of the third line.

4. The image sensor of claim 2, wherein: the plurality of pixels are arranged in the pixel array along a plurality of columns and a plurality of rows parallel to the front surface or the back surface of the substrate, the addition circuit is configured to receive the second binary code through a first line connected to the first latch circuit and receive the first binary code through a second line connected to the second latch circuit, and a second virtual line perpendicular to the front surface or the back surface of the substrate passes through a portion of one of the first line or the second line and the second counter circuit.

5. The image sensor of claim 2, wherein: the plurality of pixels are arranged in the pixel array along a plurality of columns and a plurality of rows parallel to the front surface or the back surface of the substrate, the addition circuit is configured to receive the second binary code through a first line connected to the first latch circuit and receive the first binary code through a second line connected to the second latch circuit, and at least a portion of the first line and the second line overlaps the second counter circuit when viewed from a direction perpendicular to the front surface or the back surface of the substrate.

6. The image sensor of claim 1, wherein the plurality of pixels are arranged in the pixel array along a plurality of columns and a plurality of rows, and wherein the first virtual line is parallel to one of the plurality of columns.

7. The image sensor of claim 6, wherein the first counter circuit includes: a first latch circuit configured to latch the counting code corresponding to the at least one least significant bit signal, convert the latched counting code into a binary code, and output the binary code; a second latch circuit configured to latch a first binary code among outputs of the first latch circuit; and the addition circuit configured to add a second binary code among the outputs of the first latch circuit and the first binary code latched by the second latch circuit, and wherein the first latch circuit, the second counter circuit, the addition circuit, and the second latch circuit are arranged close to the comparator along the first virtual line in an order of the first latch circuit, the second counter circuit, the addition circuit, and the second latch circuit.

8. The image sensor of claim 6, wherein the first counter circuit includes: a first latch circuit configured to latch the counting code corresponding to the at least one least significant bit signal, convert the latched counting code into a binary code, and output the binary code; a second latch circuit configured to latch a first binary code among outputs of the first latch circuit; and the addition circuit configured to add a second binary code among the outputs of the first latch circuit and the first binary code latched by the second latch circuit, and wherein the first latch circuit, the addition circuit, the second counter circuit, and the second latch circuit are arranged close to the comparator along the first virtual line in an order of the first latch circuit, the addition circuit, the second counter circuit, and the second latch circuit along the first virtual line.

9. The image sensor of claim 1, wherein the count value includes the at least one least significant bit signal and the most significant bit signals, and wherein a number of bits of the at least one least significant bit signal is less than a number of bits of the most significant bit signals.

10. The image sensor of claim 1, wherein the second counter circuit is configured to generate the most significant bit signals sequentially toggling in response to a bit signal corresponding to the most significant bit of the least significant bit signal.

11. The image sensor of claim 1, wherein the counting code includes a gray code, and the second counter circuit includes a ripple counter based on a binary code.

12. An image sensor comprising: a pixel array including a plurality of pixels; a plurality of column lines configured to output pixel voltages of the plurality of pixels; a plurality of comparators connected to each of the plurality of column lines, and each configured to generate a comparison

signal based on a ramp signal and a pixel voltage; and a plurality of counter circuits configured to receive the comparison signal from each of the plurality of comparators and output a count value corresponding to the pixel voltage based on the comparison signal, wherein each of the plurality of counter circuits includes: a first latch circuit configured to latch a gray code; a second latch circuit configured to latch a first binary code among outputs of the first latch circuit; a most significant bit counter circuit configured to receive an output of a most significant bit among the outputs of the first latch circuit and count high-order n bits of the count value, wherein the n is an integer of **1** or more; and an arithmetic unit configured to perform an operation on a second binary code among the outputs of the first latch circuit and the first binary code, wherein the gray code corresponds to lower-order m bits of the count value, wherein the m is an integer of **1** or more, and wherein the most significant bit counter circuit is arranged such that a first distance between the first latch circuit and the most significant bit counter circuit is smaller than a second distance between the first latch circuit and the second latch circuit.

13. The image sensor of claim 12, wherein the most significant bit counter circuit includes a plurality of flip-flops configured to sequentially toggle in response to a most significant bit signal among outputs of the first latch circuit or an inversion signal of the most significant bit signal to count “n” upper bits of the count value.

14. The image sensor of claim 12, wherein the first latch circuit includes: a plurality of latches each configured to latch a bit of the gray code; and a binary conversion unit configured to convert an output of the plurality of latches into a binary code.

15. The image sensor of claim 12, wherein the first latch circuit, the most significant bit counter circuit, the arithmetic unit, and the second latch circuit are arranged adjacent to a corresponding comparator among the plurality of comparators in an order of the first latch circuit, the most significant bit counter circuit, the arithmetic unit, and the second latch circuit.

16. The image sensor of claim 12, wherein the first latch circuit, the arithmetic unit, the most significant bit counter circuit, and the second latch circuit are arranged adjacent to a corresponding comparator among the plurality of comparators in an order of the first latch circuit, the arithmetic unit, the most significant bit counter circuit, and the second latch circuit.

17. An image sensor comprising: a pixel array including a plurality of pixels, each pixel configured to output a pixel signal; and an analog-to-digital converter configured to convert the pixel signal into pixel data, wherein the analog-to-digital converter comprises: a comparator configured to generate a comparison signal based on a ramp signal and an input signal; and a counter circuit configured to receive a counting code and the comparison signal and output a count value corresponding to a magnitude of the input signal based on the comparison signal, wherein the counter circuit includes: a first counter circuit including a plurality of latch circuits and an adder, and the first counter circuit configured to: latch the counting code, and generate least significant bit signals of the count value; and a second counter circuit configured to generate most significant bit signals sequentially toggling in response to one of the least significant bit signals or an inversion signal of the one of the least significant bit signals, and wherein the plurality of latch circuits, the adder, and the second counter circuit are arranged in series, and the second counter circuit is arranged between the plurality of latch circuits.

18. The image sensor of claim 17, wherein: the first counter circuit includes a first latch circuit and a second latch circuit, the adder is configured to generate the least significant bit signal by adding a first bit signal stored in the first latch circuit and a second bit signal stored in the second latch circuit, and the second counter circuit includes a plurality of flip-flops connected to each other in cascade, wherein the flip-flop located at the front most among the plurality of flip-flops is configured to receive the most significant bit signal or an inverted signal of the most significant bit signal as a clock signal.

19. The image sensor of claim 18, further comprising: a first line configured to connect the adder and the first latch circuit; a second line configured to connect the adder and the second latch circuit;

and a third line configured to connect the first latch circuit and the second counter circuit, wherein a length of the third line is shorter than a length of at least one of the first line and the second line.

20. The image sensor of claim 19, wherein the first line transmits the first bit signal, the second line transmits the second bit signal, and the third line transmits the most significant bit signal.