

# US Patent & Trademark Office

## Patent Public Search | Text View

---

United States Patent	12393702
Kind Code	B2
Date of Patent	August 19, 2025
Inventor(s)	Marson; Mark Evan et al.

---

### Protecting cryptographic keys stored in non-volatile memory

---

#### Abstract

Systems and methods for protecting cryptographic keys stored in a non-volatile memory. An example method may comprise: storing a device root key in a non-volatile memory; storing a volatile key in a volatile memory; storing a masked cryptographic key in the non-volatile memory, wherein the masked cryptographic key is produced by combining a cryptographic key and the device root key; storing a masked device root key in the non-volatile memory, wherein the masked root key is produced by combining the device root key and the volatile key; and erasing the device root key from the non-volatile memory.

---

**Inventors:** Marson; Mark Evan (Carlsbad, CA), Hamburg; Michael A. (Laguna Beach, CA)

**Applicant:** CRYPTOGRAPHY RESEARCH, INC. (San Jose, CA)

**Family ID:** 1000008764600

**Assignee:** CRYPTOGRAPHY RESEARCH, INC. (San Jose, CA)

**Appl. No.:** 17/854295

**Filed:** June 30, 2022

#### Prior Publication Data

Document Identifier	Publication Date
US 20220405404 A1	Dec. 22, 2022

#### Related U.S. Application Data

continuation parent-doc US 16963724 US 11416625 WO PCT/US2019/015765 20190130 child-doc US 17854295  
us-provisional-application US 62679317 20180601  
us-provisional-application US 62624694 20180131

---

## Publication Classification

**Int. Cl.:** **G06F21/60** (20130101); **G06F1/24** (20060101); **G06F12/14** (20060101); **G06F21/79** (20130101); **H04L9/08** (20060101)

**U.S. Cl.:**

**CPC** **G06F21/602** (20130101); **G06F1/24** (20130101); **G06F12/1408** (20130101); **G06F21/79** (20130101); **H04L9/0822** (20130101); **H04L9/0894** (20130101);

## Field of Classification Search

**CPC:** G06F (21/602); G06F (1/24); G06F (12/1408); G06F (21/79); H04L (9/0822); H04L (9/0894)

---

## References Cited

### U.S. PATENT DOCUMENTS

Patent No.	Issued Date	Patentee Name	U.S. Cl.	CPC
5363447	12/1993	Rager	380/273	H04L 9/0894
6292899	12/2000	McBride	N/A	N/A
7463739	12/2007	Couillard	N/A	N/A
7596696	12/2008	Perlman	N/A	N/A
8175276	12/2011	Tkacik et al.	N/A	N/A
9659191	12/2016	Cope	N/A	N/A
9674162	12/2016	Miller et al.	N/A	N/A
2006/0200682	12/2005	Hars	713/193	G06F 21/62
2006/0209584	12/2005	Devadas et al.	N/A	N/A
2006/0210082	12/2005	Devadas	380/277	G11C 7/24
2007/0101158	12/2006	Elliott	713/193	G06F 12/1408
2009/0196418	12/2008	Tkacik et al.	N/A	N/A
2010/0005317	12/2009	Pribadi	713/193	G06F 21/79
2012/0011294	12/2011	Shankar et al.	N/A	N/A
2012/0069995	12/2011	Matthews, Jr.	N/A	N/A
2012/0201379	12/2011	Fuchs et al.	N/A	N/A
2013/0166869	12/2012	Wang et al.	N/A	N/A
2018/0165479	12/2017	Chen	N/A	H04L 9/0819

### FOREIGN PATENT DOCUMENTS

Patent No.	Application Date	Country	CPC
103138934	12/2012	CN	N/A
107533623	12/2017	CN	N/A
0671090	12/1994	EP	N/A
2012-0109041	12/2011	KR	N/A
WO-94-13080	12/1993	WO	N/A
WO-2009-098881	12/2008	WO	N/A
WO-2017-048294	12/2016	WO	N/A

### OTHER PUBLICATIONS

EP Extended European Search Report with Mail Date Oct. 15, 2021 re: EP Appln. No. 19746781.4. 10 pages. cited by applicant

Notification Concerning Transmittal of International Preliminary Report on Patentability with Mail Date Aug. 13, 2020 re: Int'l Appln. No. PCT/US2019/015765. 9 pages. cited by applicant

Notification of Transmittal of the International Search Report and the Written Opinion of the International Searching Authority, or the Declaration with Mail Date Apr. 30, 2019 re: Int'l Appln. No. PCT/US2019/015765. 10 Pages. cited by applicant

Schellekens, Dries et al., "Embedded Trusted Computing With Authenticated Non-Volatile Memory", First International Conference on Trusted Computing and Trust in Information Technologies, Trust 2008 Villach, Austria, Mar. 11-12, 2008. Retrieved on Apr. 2, 2019 (Apr. 2, 2019) from <<https://www.esat.kuleuven.be/cosic/publications/article-1013.pdf>> entire document. 18 Pages. cited by applicant

EP Communication Pursuant to Article 94(3) EPC with Mail Date Feb. 22, 2024 re: EP Appln. No. 19746781.4. 7 pages. cited by applicant

CN Office Action with Mail Date Jul. 4, 2024 re: CN Appln. No. 201980005558.X. 11 pages. cited by applicant

EP Response filed Jun. 18, 2024 in Response to the Official Communication Pursuant to Art. 94(3) EPC Dated Feb. 22, 2024 re: Appln. No. 19746781.4. 19 pages. cited by applicant

CN Office Action with Mail Date Dec. 21, 2024 re: CN Appln. No. 201980005558.X. 7 pages. cited by applicant

---

*Primary Examiner:* Alata; Ayoub

*Attorney, Agent or Firm:* Lowenstein Sandler LLP

---

## **Background/Summary**

RELATED APPLICATIONS (1) This application is a continuation of U.S. patent application Ser. No. 16/963,724 filed Jul. 21, 2020, which is the U.S. national stage under 35 U.S.C. § 371 of International Application Number PCT/US2019/015765, filed Jan. 30, 2019, which claims the priority benefit of U.S. Provisional Application No. 62/624,694, filed Jan. 31, 2018 and the priority benefit of U.S. Provisional Application No. 62/679,317, filed Jun. 1, 2018. The entire contents of the above-referenced applications are incorporated by reference herein

### **TECHNICAL FIELD**

(1) The present disclosure is generally related to computer systems, and is more specifically related to cryptographic data processing systems and methods.

### **BACKGROUND**

(2) Since the advent of computers, constantly evolving have been not only various systems and methods for safeguarding cryptographic keys and/or other sensitive data, but also systems and methods for gaining unauthorized access to the protected data, ranging from conceptually unsophisticated brute force password cracking to complex external monitoring attacks.

---

## **Description**

### **BRIEF DESCRIPTION OF THE DRAWINGS**

(1) The present disclosure is illustrated by way of examples, and not by way of limitation, and may be more fully understood with references to the following detailed description when considered in

connection with the figures, in which:

- (2) FIG. 1 schematically illustrates the initialization sequence of an example cryptographic data processing device implementing the methods of the present disclosure for protecting cryptographic keys utilized for performing cryptographic data processing operations;
- (3) FIG. 2 schematically illustrates the key retrieval sequence of the example cryptographic data processing device;
- (4) FIG. 3 schematically illustrates another example of device initialization and key retrieval sequences of the cryptographic data processing device **100** implementing the methods of the present disclosure for protecting cryptographic keys utilized for performing cryptographic data processing operations;
- (5) FIG. 4 depicts a flow diagram of an example method for protecting cryptographic keys utilized for performing cryptographic data processing operations, in accordance with one or more aspects of the present disclosure;
- (6) FIG. 5 depicts a flow diagram of another example method for protecting cryptographic keys utilized for performing cryptographic data processing operations, in accordance with one or more aspects of the present disclosure; and
- (7) FIG. 6 illustrates a diagrammatic representation of an example computing system within which a set of instructions, for causing the computing device to perform the methods described herein, may be executed.

#### DETAILED DESCRIPTION

- (8) Described herein are systems and methods for protecting cryptographic keys utilized for performing cryptographic data processing operations.
- (9) “Cryptographic data processing operation” herein shall refer to a data processing operation involving secret parameters (e.g., encryption/decryption operations using cryptographic keys). “Cryptographic data processing device” herein shall refer to a data processing device (e.g., a general purpose or specialized processor, a system-on-chip, a cryptographic hardware accelerator, or the like) configured or employed for performing cryptographic data processing operations.
- (10) A cryptographic data processing device may securely manage one or more cryptographic keys which may be utilized for performing cryptographic data processing operations. Certain cryptographic applications and standards require that the cryptographic keys be securely destroyed (e.g., overwritten with a specified data pattern, such as all zeroes) upon detecting a tampering attempt with respect to the cryptographic data processing device. However, if one or more cryptographic keys are stored in a non-volatile memory, such as flash memory or one-time programmable (OTP) memory, the cryptographic data processing device cannot be assumed to have sufficient time or power to securely destroy the cryptographic keys.
- (11) This issue can be addressed by storing the cryptographic keys or key splits (i.e., one or more values from which the cryptographic keys may be derived) in a volatile memory such as Static Random Access Memory (SRAM). The volatile memory may be powered by a dedicated power source, such as a battery. Erasing the volatile keys or key splits would only require interrupting power supply to the volatile memory responsive to detecting a tampering attempt. All other cryptographic keys used by the cryptographic data processing device may be derived from the volatile keys or volatile key splits.
- (12) However, this approach would not be suitable if one or more cryptographic keys need to be programmed into the cryptographic data processing device in the absence of a constant power supply, which is necessary to hold the volatile keys. In an illustrative example, a device root key (DRK) may be programmed into the cryptographic data processing device as part of the manufacturing workflow, before a battery is connected to the volatile memory.
- (13) Systems and methods of the present disclosure address the above noted and other deficiencies by providing a method of protecting cryptographic keys which involves storing a device root key in a masked form, such that the masking operation involves combining the device root key with a

volatile key, which may be stored in the volatile memory and thus may be securely destroyed by interrupting the power supply to the volatile memory.

(14) The device root key may be self-generated by the device or loaded from an external source. All other cryptographic keys utilized by the device may be derived from the device root key and may be stored in the non-volatile memory in a masked form, such that the masking operation involves combining a cryptographic key with the device root key (e.g., by a bitwise exclusive disjunction operation, also referred to as “exclusive OR” or XOR).

(15) The result of the single-bit exclusive disjunction is true (binary 1), if and only if one of the two operands is true; otherwise, the result is false (binary 0). Therefore, the result of applying the exclusive disjunction operation to two equal operands is always false. Applying the exclusive disjunction operation to any operand and binary 0 produces the result which is equal to that operand. Therefore, a cryptographic key  $K$  can be masked by the device root key using the exclusive disjunction operation:  $K^*=K\oplus DRK$ ; to remove the mask, the exclusive disjunction is performed on the masked key and the device root key:

$$K=K^*\oplus DRK=(K\oplus DRK)\oplus DRK=K\oplus (DRK\oplus DRK)=K\oplus 0=K.$$

(16) Accordingly, the cryptographic key, which is stored in the volatile memory in the masked form ( $K^*=K\oplus DRK$ ), may be unmasked using the device root key ( $K^*=K\oplus DRK$ ) prior to being utilized in a cryptographic data processing operation.

(17) Since restoring any cryptographic key would require the device root key, securely destroying the device root key if a tampering event is detected would effectively destroy the cryptographic key. In order to achieve secure device root key erasure, the device root key may be stored in the non-volatile memory in a masked form, such that the masking operation involves combining the device root key with a volatile key (e.g., by a bitwise exclusive disjunction operation):

$DRK^*=DRK\oplus VK$ , where  $DRK^*$  is the masked device root key, and  $VK$  is the volatile key (or volatile key split, which is the value utilized for deriving the volatile key).

(18) The volatile key may be self-generated by the device or loaded from an external source, and may be stored in the volatile memory prior to the device becoming operational, at which point the volatile memory is assumed to have a constant power supply.

(19) After storing the masked device root key, the original device root key is erased from non-volatile memory. Restoring a cryptographic key derived from the device root key would thus require restoring the device root key from the masked form by the unmasking operation using the volatile key:  $DRK=DRK^*\oplus VK$ . Accordingly, erasing the volatile key from the volatile memory would effectively erase all cryptographic keys in the system. As noted herein above, erasing the volatile key from the volatile memory would only require interrupting the power supplied to the volatile memory.

(20) Thus, the systems and methods described herein represent improvements to the functionality of general purpose or specialized computing devices, by enabling secure handling of cryptographic keys by such devices.

(21) The systems and methods described herein may be implemented by hardware (e.g., general purpose and/or specialized processing devices, and/or other devices and associated circuitry), software (e.g., instructions executable by a processing device), or a combination thereof. Various aspects of the methods and systems are described herein by way of examples, rather than by way of limitation.

(22) FIG. 1 schematically illustrates the initialization sequence of an example cryptographic data processing device **100** implementing the methods of the present disclosure for protecting cryptographic keys utilized for performing cryptographic data processing operations. As shown in FIG. 1, the example device **100** may include a non-volatile memory (e.g., flash memory) **110**, and a volatile memory **120** (e.g., SRAM). As part of the device manufacturing workflow, the device root key (DRK) **130**, from which all other cryptographic keys would then be derived, may be stored in the non-volatile memory **110**. Alternatively, the device root key may be stored in the non-volatile

memory **110** as part of the device initialization sequence, which may involve generating the device root key or receiving it from an external source.

(23) The device initialization sequence may further involve generating or receiving from an external source one or more cryptographic keys, which may be utilized by the device **100** for performing various cryptographic data processing operations. The cryptographic keys may be stored in the non-volatile memory **110** in the masked form **140**, such that the masking operation involves combining a cryptographic key with the device root key **130** (e.g., by a bitwise exclusive disjunction operation).

(24) The device initialization sequence may further involve generating a volatile key **150** (or one or more volatile key splits, from which the volatile key may then be derived) or receiving the volatile key **150** (or one or more volatile key splits) from an external source. The volatile key **140** may be stored in the volatile memory **120**.

(25) The device initialization sequence may further involve combining the volatile key **150** and the device root key **130** by the masking function **160**, thus producing the masked device root key **170**. In an illustrative example, the masking function **160** may produce the masked device root key  $DRK^*$  by applying the bitwise exclusive disjunction operation to its inputs:  $DRK^* = DRK \oplus VK$ . Alternatively, other masking functions may be used. After storing the masked device root key **170** in the non-volatile memory **110**, the original device root key **130** may be erased from the non-volatile memory **110**.

(26) Accordingly, restoring a cryptographic key derived from the device root key **130** would involve restoring the device root key **130** from the masked form **170** by the unmasking operation using the volatile key **150**:  $DRK = DRK^* \oplus VK$ , and then restoring the cryptographic key from the masked form **140** by applying the unmasking operation using the restored device root key **130**:  $K = (K \oplus DRK) \oplus DRK$ . Thus, erasing the volatile key from the volatile memory would effectively erase all cryptographic keys in the system. In various illustrative examples, erasing the volatile key from the volatile memory **120** may be performed by interrupting the power supply **180** to the volatile memory **120** or asserting the reset signal **190** to the volatile memory **120**.

(27) In operation, one or more cryptographic keys which are stored in the masked form **140** may be unmasked prior to being utilized for performing various cryptographic data processing operations. FIG. 2 schematically illustrates the key retrieval sequence of the example cryptographic data processing device **100**. As shown in FIG. 2, the device root key **130** may be restored from its masked form **170** by applying the masking function **160** to the volatile key **150** and the masked form **170** of the device root key:  $DRK = DRK^* \oplus VK$ . The cryptographic key **210** may then be restored from its masked form **140** by applying the masking function **220** to the device root key **130** and the masked form **140** of the cryptographic key:  $K = (K \oplus DRK) \oplus DRK$ . In an illustrative example, the masking functions **160** and **220** may apply the bitwise exclusive disjunction operation to their respective inputs. Alternatively, other masking functions may be used. As noted herein above, the unmasked cryptographic key **210** may be utilized for performing various cryptographic data processing operations.

(28) FIG. 3 schematically illustrates another example of device initialization and key retrieval sequences of the cryptographic data processing device **300** implementing the methods of the present disclosure for protecting cryptographic keys utilized for performing cryptographic data processing operations. As shown in FIG. 3, as part of the device manufacturing workflow, the device root key (DRK) **130**, from which all other cryptographic keys would then be derived, may be stored in the non-volatile memory **110**. Alternatively, the device root key may be stored in the non-volatile memory **110** as part of the device initialization sequence, which may involve generating the device root key or receiving it from an external source.

(29) The device initialization sequence may further involve generating or receiving from an external source one or more cryptographic keys, which may be utilized by the device **300** for performing various cryptographic data processing operations. The cryptographic keys may be

stored in the non-volatile memory **110** in the masked form **140**, such that the masking operation involves combining a cryptographic key with the device root key **130** (e.g., by a bitwise exclusive disjunction operation). The device initialization sequence may further involve copying the device root key to the volatile memory **120**. After storing the device root key **130** in the volatile memory **120**, the original device root key **130** may be erased from the non-volatile memory **110**.

(30) Accordingly, a cryptographic key derived from the device root key **130** may be restored from its masked form **140** by the unmasking function **310** using the device root key **130**:  $K = (K \oplus DRK) \oplus DRK$ . In an illustrative example, the masking function **310** may apply the bitwise exclusive disjunction operation to their respective inputs. Alternatively, other masking functions may be used. As noted herein above, the unmasked cryptographic key **320** may be utilized for performing various cryptographic data processing operations.

(31) Accordingly, erasing the device root key from the volatile memory would effectively erase all cryptographic keys in the system. In various illustrative examples, erasing the device root key from the volatile memory **120** may be performed by interrupting the power supply **180** to the volatile memory **120** or asserting the reset signal **190** to the volatile memory **120**.

(32) FIG. 4 depicts a flow diagram of an example method **400** for protecting cryptographic keys utilized for performing cryptographic data processing operations, in accordance with one or more aspects of the present disclosure. Method **400** and/or each of its individual functions, routines, subroutines, or operations may be performed by one or more general purpose and/or specialized processing devices. Two or more functions, routines, subroutines, or operations of method **400** may be performed in parallel or in an order that may differ from the order described above. In certain implementations, method **400** may be performed by a single processing thread. Alternatively, method **400** may be performed by two or more processing threads, each thread executing one or more individual functions, routines, subroutines, or operations of the method. In an illustrative example, the processing threads implementing method **400** may be synchronized (e.g., using semaphores, critical sections, and/or other thread synchronization mechanisms). Alternatively, the processing threads implementing method **400** may be executed asynchronously with respect to each other. In an illustrative example, method **400** may be performed by the computing system **1000** described herein below with references to FIG. 6.

(33) Referring to FIG. 4, at block **410**, a cryptographic data processing device implementing the method may receive from an external source or generate a device root key, which may be provided by a bit sequence of an arbitrary length. In an illustrative example, the device root key may be programmed into the cryptographic data processing device as part of the manufacturing workflow. Alternatively, the device root key may be generated by the cryptographic data processing device as part of the device initialization sequence, as described in more detail herein above.

(34) At block **415**, the cryptographic data processing device may store the device root key in a non-volatile memory. In an illustrative example, the non-volatile memory may be provided by flash memory, as described in more detail herein above.

(35) At block **420**, the cryptographic data processing device may receive from an external source or generate a volatile key, which may be provided by a bit sequence of an arbitrary length.

(36) At block **425**, the cryptographic data processing device may store the volatile key in a volatile memory. In an illustrative example, the volatile memory may be provided by SRAM, as described in more detail herein above.

(37) At block **430**, the cryptographic data processing device may receive from an external source or generate a cryptographic key, which may be provided by a bit sequence of an arbitrary length, to be utilized for performing various cryptographic data processing operations.

(38) At block **435**, the cryptographic data processing device may produce a masked cryptographic key by combining the cryptographic key and the device root key. In an illustrative example, the masking operation may involve applying the exclusive disjunction operation to the cryptographic key and the device root key:  $K^* = K \oplus DRK$ , as described in more detail herein above.

(39) At block **440**, the cryptographic data processing device may store the masked cryptographic key in the non-volatile memory.

(40) At block **445**, the cryptographic data processing device may produce a masked device root key by combining the device root key and the volatile key. In an illustrative example, the masking operation may involve applying the exclusive disjunction operation to the device root key and the volatile key:  $DRK^* = DRK \oplus VK$ , as described in more detail herein above.

(41) At block **450**, the cryptographic data processing device may store the masked device root key in the non-volatile memory.

(42) At block **455**, the cryptographic data processing device may erase the device root key from the non-volatile memory.

(43) Responsive to detecting, at block **460**, a tampering event, the cryptographic data processing device may, at block **465**, erase the volatile key from the volatile memory, and the method may terminate, e.g., by throwing an exception at block **470**.

(44) Otherwise, at block **475**, the cryptographic data processing device may, responsive to receiving a request to perform a cryptographic data processing operation, restore the device root key by combining the masked device root key and the volatile key. In an illustrative example, the unmasking operation may involve applying the exclusive disjunction operation to the masked device root key and the volatile key:  $DRK = DRK^* \oplus VK$ , as described in more detail herein above.

(45) At block **480**, the cryptographic data processing device may restore the cryptographic key by combining the masked cryptographic key and the restored device root key. In an illustrative example, the unmasking operation may involve applying the exclusive disjunction operation to the masked cryptographic key and the restored device root key:  $K = K^* \oplus DRK$ , as described in more detail herein above.

(46) At block **485**, the cryptographic data processing device may utilize the cryptographic key for performing a cryptographic data processing operation, and the method may terminate at block **490**.

(47) FIG. 5 depicts a flow diagram of an example method **500** for protecting cryptographic keys utilized for performing cryptographic data processing operations, in accordance with one or more aspects of the present disclosure. Method **500** and/or each of its individual functions, routines, subroutines, or operations may be performed by one or more general purpose and/or specialized processing devices. Two or more functions, routines, subroutines, or operations of method **500** may be performed in parallel or in an order that may differ from the order described above. In certain implementations, method **500** may be performed by a single processing thread. Alternatively, method **500** may be performed by two or more processing threads, each thread executing one or more individual functions, routines, subroutines, or operations of the method. In an illustrative example, the processing threads implementing method **500** may be synchronized (e.g., using semaphores, critical sections, and/or other thread synchronization mechanisms). Alternatively, the processing threads implementing method **500** may be executed asynchronously with respect to each other. In an illustrative example, method **500** may be performed by the computing system **1000** described herein below with references to FIG. 6.

(48) Referring to FIG. 5, at block **510**, a cryptographic data processing device implementing the method may receive from an external source or generate a device root key, which may be provided by a bit sequence of an arbitrary length. In an illustrative example, the device root key may be programmed into the cryptographic data processing device as part of the manufacturing workflow. Alternatively, the device root key may be generated by the cryptographic data processing device as part of the device initialization sequence, as described in more detail herein above.

(49) At block **515**, the cryptographic data processing device may store the device root key in a non-volatile memory. In an illustrative example, the non-volatile memory may be provided by flash memory, as described in more detail herein above.

(50) At block **520**, the cryptographic data processing device may receive from an external source or generate a cryptographic key, which may be provided by a bit sequence of an arbitrary length, to be



utilized for performing various cryptographic data processing operations.

(51) At block **525**, the cryptographic data processing device may produce a masked cryptographic key by combining the cryptographic key and the device root key. In an illustrative example, the masking operation may involve applying the exclusive disjunction operation to the cryptographic key and the device root key:  $K^* = K \oplus DRK$ , as described in more detail herein above.

(52) At block **530**, the cryptographic data processing device may store the masked cryptographic key in the non-volatile memory.

(53) At block **535**, the cryptographic data processing device may store the device root key in the volatile memory.

(54) At block **540**, the cryptographic data processing device may erase the device root key from the non-volatile memory.

(55) Responsive to detecting, at block **545**, a tampering event, the cryptographic data processing device may, at block **550**, erase the device root key from the volatile memory, and the method may terminate, e.g., by throwing an exception at block **555**.

(56) Otherwise, at block **560**, the cryptographic data processing device may, responsive to receiving a request to perform a cryptographic data processing operation, restore the cryptographic key by combining the masked cryptographic root key and the device root key. In an illustrative example, the unmasking operation may involve applying the exclusive disjunction operation to the masked cryptographic root key and the device root key:  $K = K^* \oplus DRK$ , as described in more detail herein above.

(57) At block **565**, the cryptographic data processing device may utilize the cryptographic key for performing a cryptographic data processing operation, and the method may terminate at block **570**.

(58) FIG. **6** illustrates a diagrammatic representation of a computing system **1000** which may incorporate the processing device described herein and within which a set of instructions, for causing the computing device to perform the methods described herein, may be executed.

Computing system **1000** may be connected to other computing devices in a LAN, an intranet, an extranet, and/or the Internet. The computing device may operate in the capacity of a server machine in client-server network environment. The computing device may be provided by a personal computer (PC), a set-top box (STB), a server, a network router, switch or bridge, or any machine capable of executing a set of instructions (sequential or otherwise) that specify actions to be taken by that machine. Further, while only a single computing device is illustrated, the term “computing device” shall also be taken to include any collection of computing devices that individually or jointly execute a set (or multiple sets) of instructions to perform the methods described herein.

(59) The example computing system **1000** may include a processing device **1002**, which in various illustrative examples may be a general purpose or specialized processor comprising one or more processing cores. The example computing system **1000** may further comprise a volatile memory **1004** (e.g., SRAM)), a non-volatile memory **1006** (e.g., flash memory), and a data storage device **1018**, which may communicate with each other via a bus **1030**.

(60) The processing device **1002** may be configured to execute methods **400**, **500** for protecting cryptographic keys utilized for performing cryptographic data processing operations, in accordance with one or more aspects of the present disclosure for performing the operations and steps described herein.

(61) The example computing system **1000** may further include a network interface device **1008** which may communicate with a network **1020**. The example computing system **1000** also may include a video display unit **1010** (e.g., a liquid crystal display (LCD) or a cathode ray tube (CRT)), an alphanumeric input device **1012** (e.g., a keyboard), a cursor control device **1014** (e.g., a mouse) and an acoustic signal generation device **1016** (e.g., a speaker). In one embodiment, the video display unit **1010**, the alphanumeric input device **1012**, and the cursor control device **1014** may be combined into a single component or device (e.g., an LCD touch screen).

(62) The data storage device **1018** may include a computer-readable storage medium **1028** on

which may be stored one or more sets of instructions (e.g., instructions of methods **400**, **500**) implementing any one or more of the methods or functions described herein. Instructions implementing methods **400**, **500** may also reside, completely or at least partially, within the main memory **1004** and/or within the processing device **1002** during execution thereof by the example computing system **1000**, hence the main memory **1004** and the processing device **1002** may also constitute or comprise computer-readable media. The instructions may further be transmitted or received over the network **1020** via the network interface device **1008**.

(63) While the computer-readable storage medium **1028** is shown in an illustrative example to be a single medium, the term “computer-readable storage medium” should be taken to include a single medium or multiple media (e.g., a centralized or distributed database and/or associated caches and servers) that store the one or more sets of instructions. The term “computer-readable storage medium” shall also be taken to include any medium that is capable of storing, encoding or carrying a set of instructions for execution by the machine and that cause the machine to perform the methods described herein. The term “computer-readable storage medium” shall accordingly be taken to include, but not be limited to, solid-state memories, optical media and magnetic media.

(64) Unless specifically stated otherwise, terms such as “updating”, “identifying”, “determining”, “sending”, “assigning”, or the like, refer to actions and processes performed or implemented by computing devices that manipulates and transforms data represented as physical (electronic) quantities within the computing device's registers and memories into other data similarly represented as physical quantities within the computing device memories or registers or other such information storage, transmission or display devices. Also, the terms “first,” “second,” “third,” “fourth,” etc. as used herein are meant as labels to distinguish among different elements and may not necessarily have an ordinal meaning according to their numerical designation.

(65) Examples described herein also relate to an apparatus for performing the methods described herein. This apparatus may be specially constructed for the required purposes, or it may comprise a general purpose computing device selectively programmed by a computer program stored in the computing device. Such a computer program may be stored in a computer-readable non-transitory storage medium.

(66) The methods and illustrative examples described herein are not inherently related to any particular computer or other apparatus. Various general purpose systems may be used in accordance with the teachings described herein, or it may prove convenient to construct more specialized apparatus to perform the required method steps. The required structure for a variety of these systems will appear as set forth in the description above.

(67) The above description is intended to be illustrative, and not restrictive. Although the present disclosure has been described with references to specific illustrative examples, it will be recognized that the present disclosure is not limited to the examples described. The scope of the disclosure should be determined with reference to the following claims, along with the full scope of equivalents to which the claims are entitled.

## Claims

1. A method, comprising: storing a volatile key in a volatile memory; storing a masked cryptographic key in a non-volatile memory, wherein the masked cryptographic key is produced by combining a cryptographic key and a device root key; and storing a masked device root key in the non-volatile memory, wherein the masked device root key is produced by combining the device root key and the volatile key.
2. The method of claim 1, further comprising: responsive to detecting a tampering event, erasing the volatile key from the volatile memory.
3. The method of claim 1, further comprising: restoring the device root key by combining the masked device root key and the volatile key; restoring the cryptographic key by combining the

masked cryptographic key and the device root key; and utilizing the cryptographic key for performing a cryptographic data processing operation.

4. The method of claim 1, wherein combining the cryptographic key and the device root key further comprises: performing an exclusive disjunction operation of the cryptographic key and the device root key.

5. The method of claim 1, wherein combining the device root key and the volatile key further comprises: performing an exclusive disjunction operation of the device root key and the volatile key.

6. The method of claim 1, further comprising: receiving, from an external source, at least one of: the device root key, the volatile key, or the cryptographic key.

7. The method of claim 1, further comprising: generating at least one of: the device root key, the volatile key, or the cryptographic key.

8. A system comprising: a non-volatile memory; a volatile memory; a voltage control circuit configured to interrupt power supply to the volatile memory responsive to receiving a signal indicating a tampering event; and a processor configured to: store a volatile key in the volatile memory; store a masked cryptographic key in the non-volatile memory, wherein the masked cryptographic key is produced by combining a cryptographic key and a device root key; and store a masked device root key in the non-volatile memory, wherein the masked device root key is produced by combining the device root key and the volatile key.

9. The system of claim 8, wherein the processor is further configured to: restore the device root key by combining the masked device root key and the volatile key; restore the cryptographic key by combining the masked cryptographic key and the device root key; and utilize the cryptographic key for performing a cryptographic data processing operation.

10. The system of claim 8, wherein combining the cryptographic key and the device root key further comprises: performing an exclusive disjunction operation of the cryptographic key and the device root key.

11. A method, comprising: storing a masked cryptographic key in a non-volatile memory, wherein the masked cryptographic key is produced by combining a cryptographic key and a device root key; storing the device root key in a volatile memory; and responsive to detecting a tampering event, erasing the device root key from the volatile memory.

12. The method of claim 11, further comprising: restoring the cryptographic key by combining the masked cryptographic key and the device root key; and utilizing the cryptographic key for performing a cryptographic data processing operation.

13. The method of claim 11, wherein combining the cryptographic key and the device root key further comprises: performing an exclusive disjunction operation of the cryptographic key and the device root key.

14. The method of claim 11, further comprising: receiving, from an external source, at least one of: the device root key or the cryptographic key.

15. The method of claim 11, further comprising: generating at least one of: the device root key or the cryptographic key.

16. The method of claim 2, wherein erasing the volatile key from the volatile memory further comprises: sending a reset signal to the volatile memory.

17. The method of claim 2, wherein erasing the volatile key from the volatile memory further comprises: interrupting power supply to the volatile memory.

18. The system of claim 8, wherein combining the device root key and the volatile key further comprises: performing an exclusive disjunction operation of the device root key and the volatile key.

19. The method of claim 11, wherein erasing the device root key from the volatile memory further comprises: sending a reset signal to the volatile memory.

20. The method of claim 11, wherein erasing the device root key from the volatile memory further comprises: interrupting power supply to the volatile memory.

---