



(19) **United States**

(12) **Patent Application Publication**
LIN et al.

(10) **Pub. No.: US 2025/0266104 A1**

(43) **Pub. Date: Aug. 21, 2025**

(54) **MEMORY SEARCHING ENGINE,
REFERENCE ARRAY AND REFERENCE
CALIBRATING METHOD**

(71) Applicant: **MACRONIX INTERNATIONAL
CO., LTD.**, HSINCHU (TW)

(72) Inventors: **Yu-Hsuan LIN**, Taichung City (TW);
Po-Hao TSENG, Taichung City (TW)

(21) Appl. No.: **18/582,708**

(22) Filed: **Feb. 21, 2024**

Publication Classification

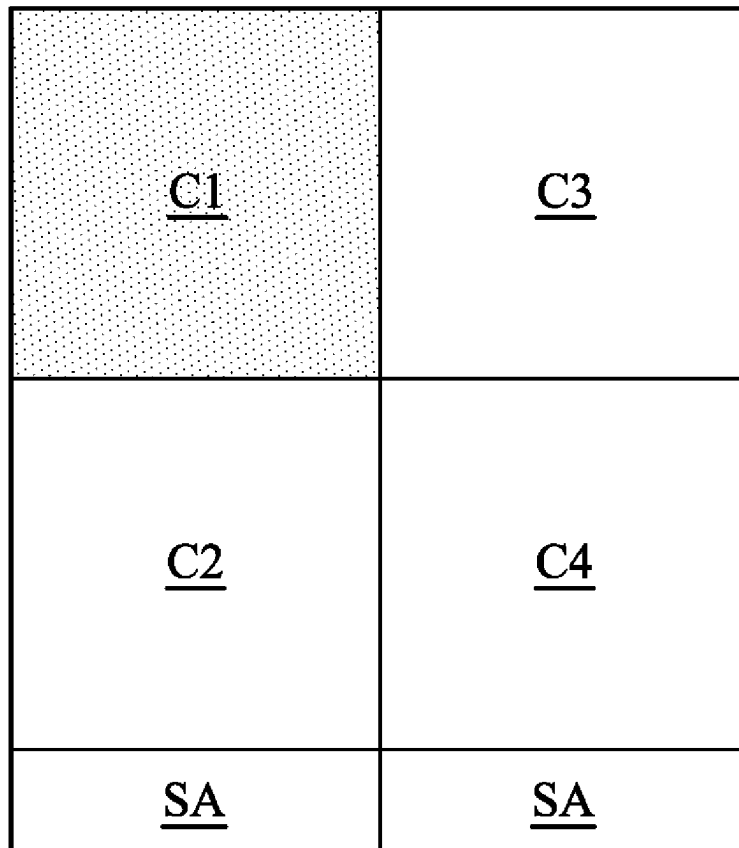
(51) **Int. Cl.**
G11C 16/28 (2006.01)
G11C 16/24 (2006.01)
G11C 29/02 (2006.01)

(52) **U.S. Cl.**
CPC **G11C 16/28** (2013.01); **G11C 16/24**
(2013.01); **G11C 29/028** (2013.01)

(57) **ABSTRACT**

A memory searching engine is provided in present disclosure. The memory searching engine stores at least one reference time and at least one reference voltage corresponding to multiple Hamming distances and comprises a data array and a reference array. The data array stores at least one first pattern data and is configured to perform a data searching according to the difference between at least one input data and the first pattern data. The reference array stores at least one second pattern data and receives the input data. Each of the first and second pattern data comprises m features, wherein m is an integer. The memory searching engine calculates multiple updated reference times and updated reference voltages corresponding to the Hamming distances based on the second pattern data, and update the reference time according to the updated reference times, or update the reference voltage according to the updated reference voltages.

100



100

<u>C1</u>	<u>C3</u>	
<u>C2</u>	<u>C4</u>	<u>SA</u>
		<u>SA</u>

Fig. 1

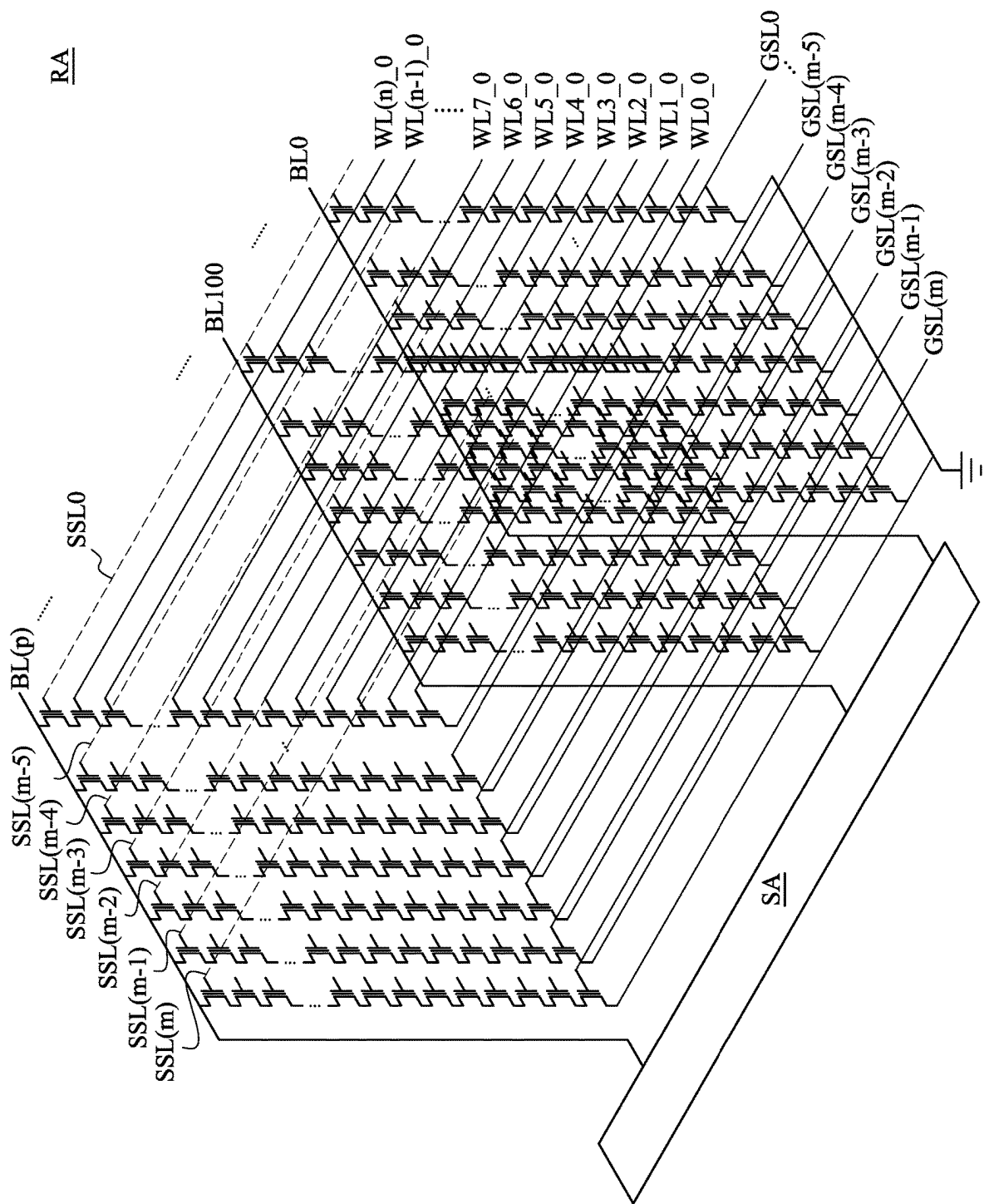


Fig. 2

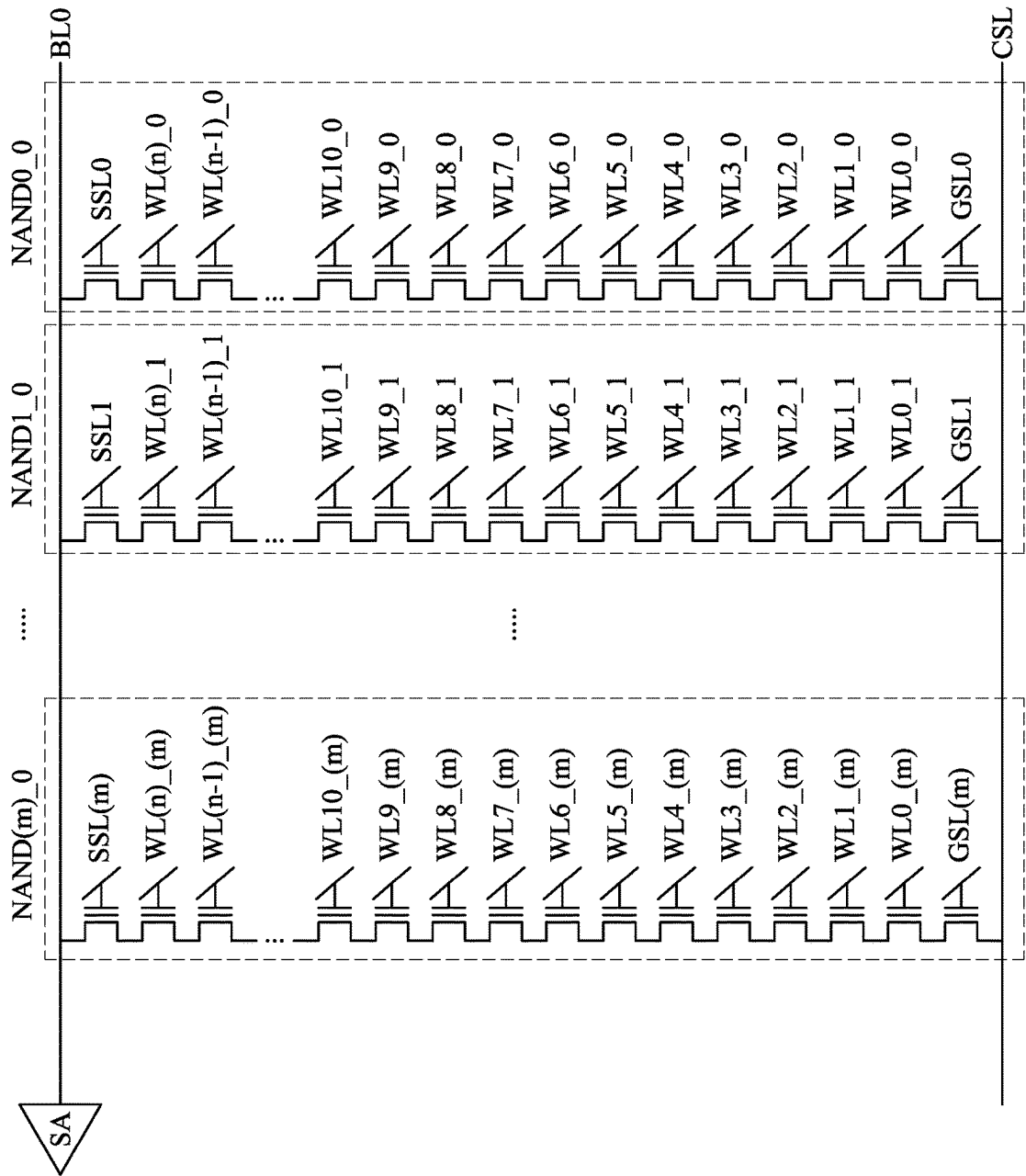


Fig. 3

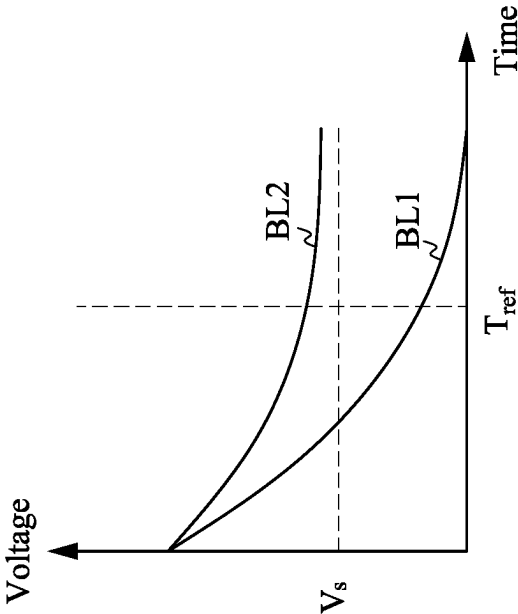


Fig. 4B

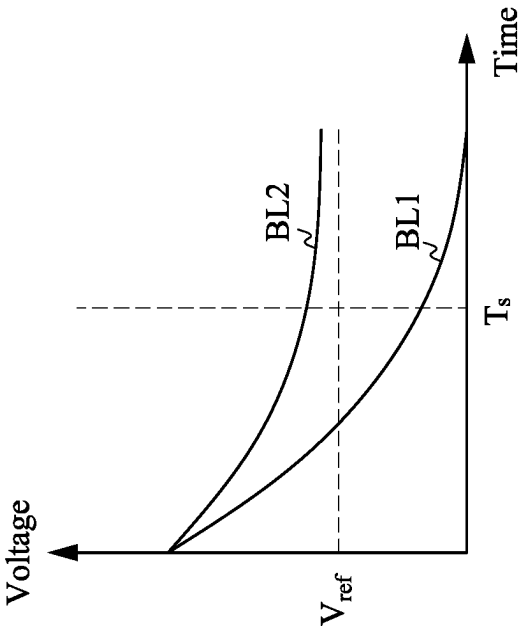


Fig. 4A

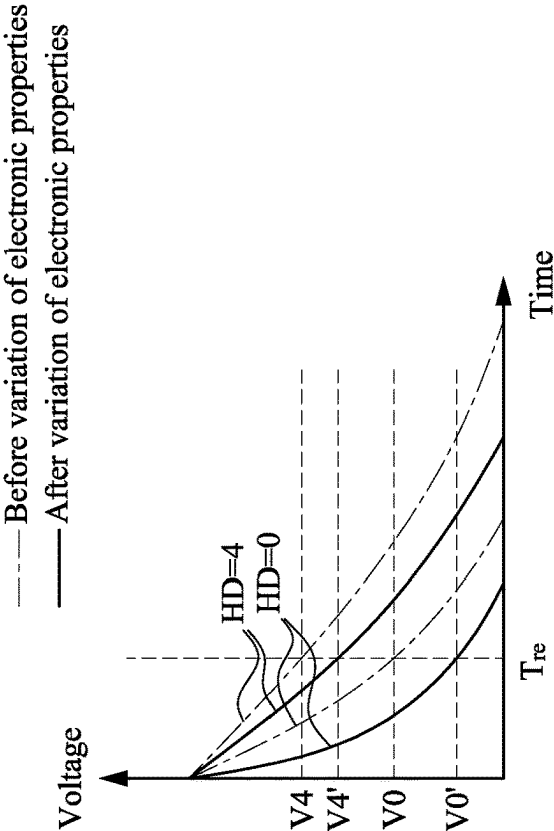


Fig. 5B

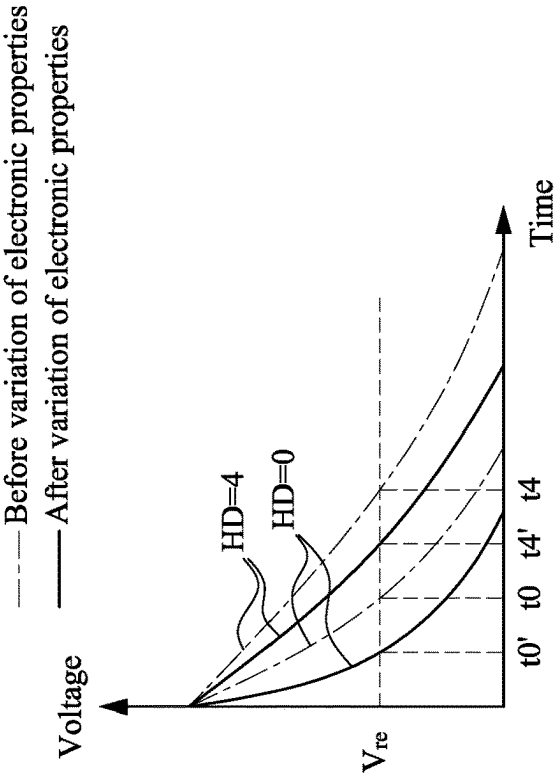


Fig. 5A

600

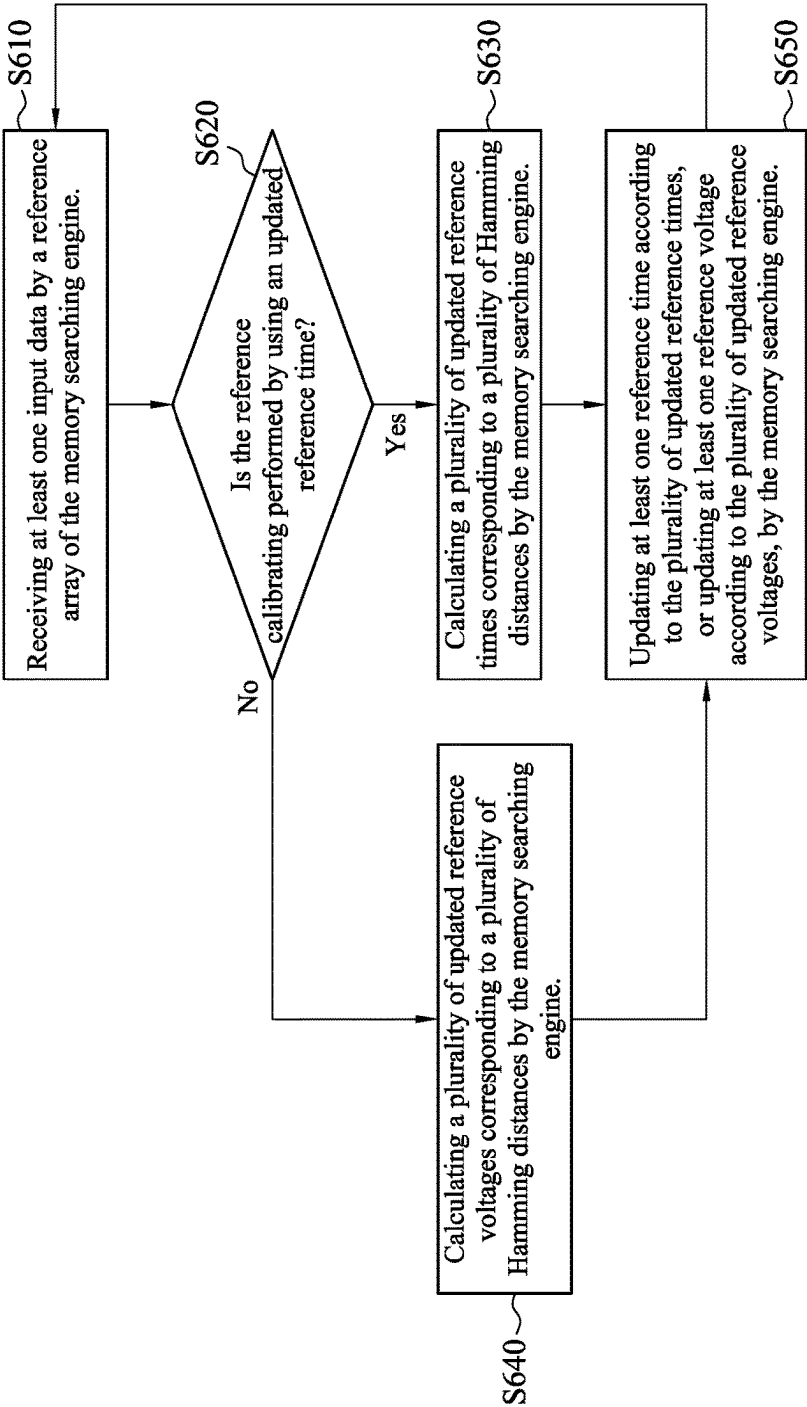


Fig. 6

MEMORY SEARCHING ENGINE, REFERENCE ARRAY AND REFERENCE CALIBRATING METHOD

BACKGROUND

Technical Field

[0001] The present disclosure is related to a memory searching engine, a reference array and a reference calibrating method. More particularly, the present disclosure is related to a memory searching engine, a reference array and a reference calibrating method having a function for calibrating the reference voltage and the reference time used for data searching.

Description of Related Art

[0002] With the development of flash memory technology, three-dimensional (3D) flash memory has gradually replaced traditional planar flash memory due to its lower unit cost. In addition, since big data and artificial intelligence technology require a large amount of calculations, data searching and data comparing functions have become important functions in 3D flash memory.

[0003] However, after long-term storage or internal temperature changes, the electronic properties of the 3D flash memory may shift, which results in changes in the scanned current and further affects the data searching function of the 3D flash memory. Consequently, how to effectively calibrate the search-related parameters as the shift of the electronic properties in 3D flash memory is one of the topics in this field.

SUMMARY

[0004] A memory searching engine is provided in present disclosure. The memory searching engine stores at least one reference time and at least one reference voltage corresponding to a plurality of Hamming distances. The memory searching engine comprises a data array and a reference array. The data array stores at least one first pattern data and is configured to perform a data searching according to the difference between at least one input data and the at least one first pattern data, so as to generate a searching result. Each of the first pattern data comprises m features, wherein m is an integer. The reference array stores at least one second pattern data and is configured to receive the at least one input data. Each of the second pattern data comprises m features. The memory searching engine is further configured to calculate a plurality of updated reference times and a plurality of updated reference voltages corresponding to the plurality of Hamming distances based on the at least one second pattern data and perform a reference calibrating, so as to update the at least one reference time according to the plurality of updated reference times, or update the at least one reference voltage according to the plurality of updated reference voltages.

[0005] In some embodiments of the memory searching engine, the reference array comprises a plurality of bit lines and a plurality of Not-AND (NAND) strings, the plurality of NAND strings are each coupled between one of the plurality of bit lines and a common source line. The plurality of NAND strings are configured to store the at least one second pattern data, and ones of the plurality of NAND strings coupled to the same bit line respectively store a plurality of

portions of the at least one second pattern data, and the plurality of portions are same to each other.

[0006] In some embodiments of the memory searching engine, the at least one input data comprises an input data, the at least one second pattern data comprises a plurality of second pattern data in different types. A plurality of combinations of the input data and the plurality of second pattern data correspond to the plurality of Hamming distances, and one of the at least one reference time corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference times, and one of the at least one reference voltage corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference voltages.

[0007] In some embodiments of the memory searching engine, the at least one input data comprises a plurality of input data in different types, the at least one second pattern data comprises a second pattern data. A plurality of combinations of the plurality of input data and the second pattern data correspond to the plurality of Hamming distances, and one of the at least one reference time corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference times, and one of the at least one reference voltage corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference voltages.

[0008] In some embodiments of the memory searching engine, the at least one input data comprises a plurality of input data in different types, the at least one second pattern data comprises a plurality of second pattern data in different types. A plurality of combinations of the plurality of input data and the plurality of second pattern data correspond to the plurality of Hamming distances, and one of the at least one reference time corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference times, and one of the at least one reference voltage corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference voltages.

[0009] In some embodiments of the memory searching engine, the reference calibrating is performed before the data searching is performed, or the reference calibrating is performed every other a calibration cycle.

[0010] In some embodiments of the memory searching engine, the area of the reference array arranged in the memory searching engine is less than or equal to the area of the data array arranged in the memory search engine.

[0011] A reference array arranged in a memory searching engine is provided in the present disclosure. The memory searching engine stores at least one reference time and at least one reference voltage corresponding to a plurality of Hamming distances, and the memory searching engine comprises a data array storing at least one first pattern data. Each of the first pattern data comprises m features, wherein m is an integer. The reference array is configured to store at least one second pattern data and configured to receive at least one input data, wherein each of the second pattern data comprises m features. The at least one second pattern data is configured to be provided to the memory searching engine, so as to calculate a plurality of updated reference times and a plurality of updated reference voltages corresponding to

the plurality of Hamming distances, and allow the memory searching engine to perform a reference calibrating, so as to update the at least one reference time according to the plurality of updated reference times, or update the at least one reference voltage according to the plurality of updated reference voltages.

[0012] In some embodiments of the reference array, the reference array comprises a plurality of bit lines and a plurality of Not-AND (NAND) strings, the plurality of NAND strings are each coupled between one of the plurality of bit lines and a common source line. The plurality of NAND strings are configured to store the at least one second pattern data, and ones of the plurality of NAND strings coupled to the same bit line respectively store a plurality of portions of the at least one second pattern data, and the plurality of portions are same to each other.

[0013] In some embodiments of the reference array, the at least one input data comprises an input data, the at least one second pattern data comprises a plurality of second pattern data in different types. A plurality of combinations of the input data and the plurality of second pattern data correspond to the plurality of Hamming distances, and one of the at least one reference time corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference times, and one of the at least one reference voltage corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference voltages.

[0014] In some embodiments of the reference array, the at least one input data comprises a plurality of input data in different types, the at least one second pattern data comprises a second pattern data. A plurality of combinations of the plurality of input data and the second pattern data correspond to the plurality of Hamming distances, and one of the at least one reference time corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference times, and one of the at least one reference voltage corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference voltages.

[0015] In some embodiments of the reference array, the at least one input data comprises a plurality of input data in different types, the at least one second pattern data comprises a plurality of second pattern data in different types. A plurality of combinations of the plurality of input data and the plurality of second pattern data correspond to the plurality of Hamming distances, and one of the at least one reference time corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference times, and one of the at least one reference voltage corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference voltages.

[0016] In some embodiments of the reference array, the reference calibrating is performed before a data searching is performed by the memory searching engine, or the reference calibrating is performed every other a calibration cycle.

[0017] In some embodiments of the reference array, the area of the reference array arranged in the memory searching engine is less than or equal to the area of the data array arranged in the memory search engine.

[0018] A reference calibrating method suitable for a memory search engine is provided in the present disclosure. The memory search engine comprises a data array and a reference array, and stores at least one reference time and at least one reference voltage corresponding to a plurality of Hamming distances. The data array stores at least one first pattern data, the reference array stores at least one second pattern data. Each of the first pattern data comprises m features, and each of the second pattern data comprises m features, wherein m is an integer. The reference calibrating method comprises: receiving, by the reference array, at least one input data; calculating, by the memory search engine, a plurality of updated reference times and a plurality of updated reference voltages corresponding to the plurality of Hamming distances, based on the at least one second pattern data; and updating, by the memory search engine, the at least one reference time according to the plurality of updated reference times, or the at least one reference voltage according to the plurality of updated reference voltages.

[0019] In some embodiments of the reference calibrating method, the reference array comprises a plurality of bit lines and a plurality of Not-AND (NAND) strings, the plurality of NAND strings are each coupled between one of the plurality of bit lines and a common source line. The plurality of NAND strings are configured to store the at least one second pattern data, and ones of the plurality of NAND strings coupled to the same bit line respectively store a plurality of portions of the at least one second pattern data, and the plurality of portions are same to each other.

[0020] In some embodiments of the reference calibrating method, the at least one input data comprises an input data, the at least one second pattern data comprises a plurality of second pattern data in different types. A plurality of combinations of the input data and the plurality of second pattern data correspond to the plurality of Hamming distances, and one of the at least one reference time corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference times, and one of the at least one reference voltage corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference voltages.

[0021] In some embodiments of the reference calibrating method, the at least one input data comprises a plurality of input data in different types, the at least one second pattern data comprises a second pattern data. A plurality of combinations of the plurality of input data and the second pattern data correspond to the plurality of Hamming distances, and one of the at least one reference time corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference times, and one of the at least one reference voltage corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference voltages.

[0022] In some embodiments of the reference calibrating method, the at least one input data comprises a plurality of input data in different types, the at least one second pattern data comprises a plurality of second pattern data in different types. A plurality of combinations of the plurality of input data and the plurality of second pattern data correspond to the plurality of Hamming distances, and one of the at least one reference time corresponding to each of the plurality of Hamming distances is configured to be updated according to

at least one of the plurality of updated reference times, and one of the at least one reference voltage corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference voltages.

[0023] In some embodiments of the reference calibrating method, the reference calibrating method is performed before a data searching is performed by the memory searching engine, or the reference calibrating method is performed every other a calibration cycle.

[0024] With the memory searching engine, the reference array and the reference calibrating method disclosed in the present disclosure, the reference time and the reference voltage used in data searching can be updated periodically, so as to prevent the changes in the electronic properties of the memory searching engine from affecting the results of data searching.

[0025] It should be understood that both the foregoing general description and the following detailed description are by examples, and are intended to provide further explanation of the disclosure as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] The present disclosure can be more fully understood by reading the following detailed description of the embodiment, with reference made to the accompanying drawings as follows.

[0027] FIG. 1 is a simplified top view of a memory searching engine in accordance with some embodiments of the present disclosure.

[0028] FIG. 2 is a partial perspective view of a reference array in accordance with some embodiments of the present disclosure.

[0029] FIG. 3 is a schematic diagram of a bit line and Not-AND (NAND) strings in accordance with some embodiments of the present disclosure.

[0030] FIG. 4A is a graph of discharge curves of different bit lines in accordance with some embodiments of the present disclosure.

[0031] FIG. 4B is a graph of discharge curves of different bit lines in accordance with some embodiments of the present disclosure.

[0032] FIG. 5A is a schematic diagram of calibrating the reference time corresponding to changes in the discharge curve in accordance with some embodiments of the present disclosure.

[0033] FIG. 5B is a schematic diagram of calibrating the reference voltage corresponding to changes in the discharge curve in accordance with some embodiments of the present disclosure.

[0034] FIG. 6 is a flowchart of a reference calibrating method in accordance with some embodiments of the present disclosure.

DETAILED DESCRIPTION

[0035] Reference will now be made in detail to the present embodiments of the disclosure, examples of which are illustrated in the accompanying drawings.

[0036] In the present disclosure, when an element is referred to as “connected”, it may mean “electrically connected” or “optical connected”. When an element is referred to as “coupled”, it may mean “electrically coupled” or “optical coupled”. “Connected” or “coupled” can also be

used to indicate that two or more components operate or interact with each other. As used in the present disclosure, the singular forms “a”, “one” and “the” are also intended to include plural forms, unless the context clearly indicates otherwise. It will be further understood that when used in this specification, the terms “comprises (comprising)” and/or “includes (including)” designate the existence of stated features, steps, operations, elements and/or components, but the existence or addition of one or more other features, steps, operations, elements, components, and/or groups thereof are not excluded.

[0037] FIG. 1 is a simplified top view of memory searching engine 100 in accordance with some embodiments of the present disclosure. In some embodiments, the memory searching engine 100 comprises a plurality of half-planes (e.g., the half-planes C1-C4 in FIG. 1) and a plurality of sensing amplifiers SA, wherein each of the plurality of sensing amplifiers SA is adjacent to at least one half-plane (e.g., the two sensing amplifiers SA in FIG. 1 are respectively adjacent to the half-plane C2 and C4), and is configured to connect to a data array or a reference array (described in the following paragraphs) in the corresponding half-plane. In some embodiments, a combination of two half-planes (e.g., the half-planes C1 and C2) is referred to as a plane.

[0038] In some embodiments, the half-planes C1-C4 are configured to set a data array or a reference array, the area of the reference array arranged in the memory searching engine 100 is less than or equal to the area of the data array arranged in the memory search engine 100. For example, as shown in FIG. 1, in the half-planes C1-C4, the area marked with dots is the area for setting the reference array, and the area without dots is the area for setting the data array, thus the area of the half-plane C1 where the reference array is set is less than the area of the half-planes C2-C4 where the data array is set.

[0039] It should be noted that the arrangement of the data array and reference array in FIG. 1 in present disclosure is only an example, and is not intended to limit the present disclosure. In the case that the area of the reference array arranged in the memory searching engine 100 is less than or equal to the area of the data array arranged in the memory search engine 100, other arrangements of the data array and reference array are within the scope of the present disclosure. In some embodiments, the reference array is arranged in the half-planes C1 and C2, and the data array is arranged in the half-planes C3 and C4. In some embodiments, the reference array is arranged in half the area of the half-planes C1, and the data array is arranged in the half-planes C2-C4 and another half the area of the half-planes C1.

[0040] FIG. 2 is a partial perspective view of a reference array RA in accordance with some embodiments of the present disclosure. In some embodiments, the reference array RA comprises bit lines BL0-BL(p) arranged in parallel and a plurality of Not-AND (NAND) strings (not labeled for the sake of brevity in FIG. 2, which will be described in subsequent paragraphs and figures), and the reference array RA is configured to receive at least one input data, wherein p is an integer. The bit lines BL0-BL(p) connect to the sensing amplifiers SA. Each of the NAND strings is connected between one of the bit lines BL0-BL(p) and a common source line CSL, and the number of the NAND strings that each of the bit lines BL0-BL(p) connects to is same to each other. With regard to the structure formed by

the bit lines BL₀-BL_(p) and the NAND strings, please refer to FIG. 2 and FIG. 3 together.

[0041] FIG. 3 is a schematic diagram of the bit line BL₀ and the NAND strings NAND_{0_0}-NAND_{(m)_0} connected to the bit line BL₀ in accordance with some embodiments of the present disclosure. As shown in FIG. 3, in some embodiments, the NAND strings NAND_{0_0}-NAND_{(m)_0} are coupled between the bit line BL₀ and the common source line CSL, wherein m is an integer. The NAND strings NAND_{0_0}-NAND_{(m)_0} each comprises a plurality of serially coupled transistors with the same number, and the control terminals of these transistors are correspondingly coupled to string select lines SSL₀-SSL_(m), ground select lines GSL₀-GSL_(m) or word lines WL_{0_0}-WL_{(n)_0}, wherein n is an integer. Take the instance in FIG. 3 for example, in the NAND string NAND_{0_0}, the control terminal of the transistor closest to the common source line CSL is coupled to the ground select line GSL₀, the control terminal of the transistor closest to the bit line BL₀ is coupled to the string select line SSL₀, and the control terminals of the other transistors are respectively coupled to the word lines WL_{0_0}-WL_{(n)_0}; in the NAND string NAND_{0_1}, the control terminal of the transistor closest to the common source line CSL is coupled to the ground select line GSL₁, the control terminal of the transistor closest to the bit line BL₀ is coupled to the string select line SSL₁, and the control terminals of the other transistors are respectively coupled to the word lines WL_{0_1}-WL_{(n)_1}, and so on.

[0042] The arrangement of each of the bit lines BL₀-BL_(p) and corresponding NAND strings is similar to the arrangement of the bit lines BL₀ and the NAND strings NAND_{0_0}-NAND_{(m)_0}. For example, the bit line BL₁ also connects to m NAND strings, and the connection relationships between these m NAND strings and the common source line CSL, the string select lines SSL₀-SSL_(m), the ground select lines GSL₀-GSL_(m), the word lines WL_{0_0}-WL_{(n)_0} are similar to aforementioned content about the NAND strings NAND_{0_0}-NAND_{(m)_0}. For the sake of brevity, similar content will not be repeated here.

[0043] Through the connection relationships between the plurality of bit lines, the plurality of NAND strings, the plurality of word lines, the plurality of string select lines and the plurality of ground select lines mentioned above, the reference array RA forms a three-dimensional (3D) structure as shown in FIG. 2. In addition, the structure of the data array (not shown) in the memory searching engine 100 is similar to the reference array RA. For the sake of brevity, the details will not be repeated here.

[0044] In some embodiments, in each of the NAND strings, two adjacent transistors coupled to the word lines correspond to one bit of In-Memory-Search (IMS). Take the instance in FIG. 3 for example, in the NAND string NAND_{0_0}, the transistors coupled to the word lines WL_{0_0} and WL_{1_0} correspond to the first bit of IMS, the transistors coupled to the word lines WL_{2_0} and WL_{3_0} correspond to the second bit of IMS, and so on.

[0045] In some embodiments, according to the configuration and conduction status of the plurality of transistors in the NAND string, a pattern data is stored in each NAND string, and all NAND strings connected to the same bit line store the same pattern data. Take the instance in FIG. 3 for example, the NAND strings NAND_{0_0}-NAND_{(m)_0} connected to the bit line BL₀ store the same pattern data.

[0046] In some embodiments, each of the data array (not shown) and the reference array RA in the memory searching engine 100 stores the pattern data, wherein the pattern data stored by the data array and the pattern data stored by the reference array RA have the same number of features. In addition, in some embodiments, the memory searching engine 100 is configured to perform a data searching based on the received input data and the pattern data stored in the data array, and then outputs a corresponding searching result.

[0047] Since the pattern data of the data array and the reference array RA may have different patterns, the logic value output by the bit line depends on the relationship between its discharge curve and the reference time or reference voltage. Please refer to FIG. 4A and FIG. 4B. FIG. 4A and FIG. 4B are graphs of discharge curves of the bit lines BL₁ and BL₂ in accordance with some embodiments of the present disclosure. The discharge curves in FIG. 4A are similar to the discharge curves in FIG. 4B. The difference is that in the embodiment of FIG. 4A, the outputs of the bit lines BL₁ and BL₂ are determined according to a reference voltage V_{ref}, while in the embodiment of FIG. 4B, the outputs of the bit lines BL₁ and BL₂ are determined according to a reference time T_{ref}.

[0048] First, please refer to FIG. 4A. In the embodiments of FIG. 4A, the reference voltage V_{ref} is the reference voltage (e.g., set by a logic unit in the memory searching engine 100) used to determine the logic values of the bit lines BL₁ and BL₂. At sensing time T_s, the voltage of the bit line BL₁ has decreased to the voltage lower than the reference voltage V_{ref}, thus the bit line BL₁ will generate an output corresponding to logic “1”. On the other hand, at sensing time T_s, although the voltage of the bit line BL₂ has decreased, it still remains higher than the reference voltage V_{ref}, thus the bit line BL₂ will generate an output corresponding to logic “0”.

[0049] Next, please refer to FIG. 4B. In the embodiments of FIG. 4B, the reference time T_{ref} is the reference time (e.g., set by a logic unit in the memory searching engine 100) used to determine the logic values of the bit lines BL₁ and BL₂. Since the time required for the voltage of the bit line BL₁ to drop from the start of discharge to the sensing voltage V_s is less than the reference time T_{ref}, the bit line BL₁ will generate an output corresponding to logic “1”. On the other hand, since the time required for the voltage of the bit line BL₂ to drop from the start of discharge to the sensing voltage V_s is more than the reference time T_{ref}, the bit line BL₂ will generate an output corresponding to logic “0”.

[0050] It should be noted that the discharge curves and the output configurations of logic values in FIG. 4A and FIG. 4B in present disclosure is only an example, and is not intended to limit the present disclosure. Other discharge curves and output configurations of logic values are within the scope of the present disclosure.

[0051] As mentioned above, in some embodiments, the memory searching engine 100 stores at least one reference time T_{ref} and at least one reference voltage V_{ref}, and these reference times T_{ref} and reference voltage V_{ref} correspond to a plurality of Hamming distances (HD).

[0052] Specifically, Hamming distance represents the amount of bit difference between input data and stored data. For example, the stored data is a binary string “000000”, when the input data is a binary string “000001”, since there is one bit difference between the input data and the stored

data, the Hamming distance is 1; when the input data is a binary string “011011”, since there are four bit differences between the input data and the stored data, the Hamming distance is 4, and so on. Depending on the difference between the input data and the stored data (i.e., the Hamming distance), the bit lines will have different discharge curves. Therefore, in order to determine the logic values for discharge curves with different Hamming distances, the memory searching engine 100 stores at least one reference time T_{ref} and at least one reference voltage V_{ref} corresponding to the plurality of Hamming distances.

[0053] However, long-term data storage or temperature changes of the memory may cause the electronic properties of the memory searching engine 100 to shift, thereby changing the discharge curves of the bit lines and affecting the outputs of the bit lines. Therefore, the reference time or reference voltage in the memory searching engine 100 may need to be updated. For example, the discharge curve of the bit line BL1 in FIG. 4A may be shifted to the position of the discharge curve of the bit line BL2, resulting in outputting different logic values. Therefore, in some embodiments, the memory searching engine 100 may perform a reference calibrating periodically or before performing specific operations (e.g., data searching) to adjust the stored reference time T_{ref} and reference voltage V_{ref} .

[0054] FIG. 5A is a schematic diagram of calibrating the reference time corresponding to changes in the discharge curve in accordance with some embodiments of the present disclosure. FIG. 5B is a schematic diagram of calibrating the reference voltage corresponding to changes in the discharge curve in accordance with some embodiments of the present disclosure. The discharge curves corresponding to Hamming distance of 0 and Hamming distance of 4 in FIG. 5A and are similar to the discharge curves corresponding to Hamming distance of 0 and Hamming distance of 4 in FIG. 5B. The difference is that FIG. 5A illustrates the time it takes for a bit line to discharge to a specific voltage, and FIG. 5B illustrates the voltage the bit line reaches after a specific time.

[0055] First, please refer to FIG. 5A. In the embodiments of FIG. 5A, the memory searching engine 100 first determines a calibration voltage V_{re} , and calculates the times respectively required for the bit lines with Hamming distances of 0 ($HD=0$) and 4 ($HD=4$) to discharge to the calibration voltage V_{re} . As shown in FIG. 5A, before the electronic properties of the memory searching engine 100 change, the bit lines with Hamming distances of 0 and 4 are discharged to the calibration voltage V_{re} at time t_0 and time t_4 respectively. After the electronic properties of the memory searching engine 100 change, the bit lines with Hamming distances of 0 and 4 are discharged to the calibration voltage V_{re} at time t_0' and time t_4' respectively. Therefore, the memory searching engine 100 determines the time t_0' and time t_4' to be updated reference times to respectively replace the original reference times T_{ref} corresponding to the bit lines with Hamming distances of 0 and 4 (i.e., time t_0 and time t_4) to complete a reference calibration operation.

[0056] Next, please refer to FIG. 5B. In the embodiments of FIG. 5B, the memory searching engine 100 first determines a calibration time T_{re} , and calculates the voltage respectively the bit lines with Hamming distances of 0 ($HD=0$) and 4 ($HD=4$) reach at the calibration times T_{re} . As shown in FIG. 5B, the bit lines with Hamming distances of 0 and 4 are discharged to voltage V_0 and voltage V_4 respectively at the calibration time T_{re} . After the electronic

properties of the memory searching engine 100 change, the bit lines with Hamming distances of 0 and 4 are discharged to voltage V_0' and voltage V_4' respectively at the calibration time T_{re} . Therefore, the memory searching engine 100 determines the voltage V_0' and voltage V_4' to be updated reference voltages to respectively replace the original reference voltages V_{ref} corresponding to the bit lines with Hamming distances of 0 and 4 (i.e., voltage V_0 and voltage V_4) to complete a reference calibration operation.

[0057] In some embodiments, in order to enhance the accuracy of updating the reference time T_{ref} and the reference voltage V_{ref} , in the data array and the reference array RA, the same pattern data will be stored in a plurality of bit lines (for example, 10-100 bit lines). Therefore, the memory searching engine 100 can perform the reference calibration according to the updated reference times and updated reference voltages of the plurality of different bit lines corresponding to the same Hamming distance.

[0058] Continuing from the instances in FIG. 5A and FIG. 5B, the bit lines BL0-BL99 in the reference array RA are configured to store the pattern data corresponding to the Hamming distance of 0, and the bit lines BL100-BL199 are configured to store the pattern data corresponding to the Hamming distance of 4. The memory searching engine 100 can obtain each 100 data of voltage V_0' , voltage V_4' , time t_0' and time t_4' according to the discharge curves of each of the bit lines BL0-BL99, BL100-BL199, and updated the reference voltage V_{ref} and the reference time T_{ref} corresponding to the bit lines with Hamming distances of 0 and 4 based on these each 100 data of voltage V_0' , voltage V_4' , time t_0' and time t_4' .

[0059] In some embodiments, the memory searching engine 100 can calibrate the reference voltage V_{ref} and the reference time T_{ref} based on the average, median, normal distribution or other statistical values of the plurality of updated reference voltages and the plurality of updated reference times respectively.

[0060] The Hamming distances between the input data and the pattern data stored in the data array and reference array RA can have a plurality of different configurations. In some embodiments, the input data input into the reference array RA comprises input data in only one type (e.g., a binary string “0000”), and the pattern data stored by the data array and the reference array RA comprises a plurality of pattern data in different types (e.g., binary strings “0000”, “0001”, “0010”, . . . , “1111”). In this configuration, the memory searching engine 100 can calculate the plurality of updated reference times and the plurality of updated reference voltages corresponding to different Hamming distances based on the input data in one type and the plurality pattern data in different types.

[0061] In some embodiments, the input data input into the reference array RA comprises a plurality of input data in different types (e.g., binary strings “0000”, “0001”, “0010”, . . . , “1111”), and the pattern data stored by the data array and the reference array RA comprises pattern data in only one type (e.g., a binary string “0000”). In this configuration, the memory searching engine 100 can calculate the plurality of updated reference times and the plurality of updated reference voltages corresponding to different Hamming distances based on the plurality of input data in different types and the pattern data in one type. Since the data array and the reference array RA can only store one type of pattern data, storage space can be saved.

[0062] In some embodiments, the configuration of the input data and the pattern data can be determined by combining the two configurations described above. That is, the input data input into the reference array RA comprises a plurality of input data in different types (e.g., binary strings “0000”, “0001”, “0010”, . . . “1111”), and the pattern data stored by the data array and the reference array RA also comprises a plurality of pattern data in different types (e.g., binary strings “0000”, “0001”, “0010”, . . . , “1111”). In this configuration, the memory searching engine 100 can calculate the plurality of updated reference times and the plurality of updated reference voltages corresponding to different Hamming distances based on the plurality of input data in different types and the plurality pattern data in different types. This configuration can reduce the amount and complexity of input data, and also avoid using excessive storage space in the data array and the reference array RA.

[0063] In some embodiments, the reference calibration on the reference voltage V_{ref} and the reference time T_{ref} performed by the memory searching engine 100 can be performed once before each data searching is performed, or be performed every other a calibration cycle, so as to ensure that the reference voltage V_{ref} and the reference time T_{ref} are updated periodically.

[0064] FIG. 6 is a flowchart of a reference calibrating method 600 in accordance with some embodiments of the present disclosure. In some embodiments, the reference calibrating method 600 comprises steps S610, S620, S630, S640 and S650.

[0065] In step S610, the reference array RA of the memory searching engine 100 receives at least one input data. Next, step S620 will be performed.

[0066] In step S620, the memory searching engine 100 determines whether to calibrate the original reference time based on the updated reference time or to calibrate the original reference voltage based on the updated reference voltage. If the memory searching engine 100 determines to calibrate the original reference time based on the updated reference time, step S630 will be performed; if the memory searching engine 100 determines to calibrate the original reference voltage based on the updated reference voltage, step S640 will be performed.

[0067] In step S630, the memory searching engine 100 calculates a plurality of updated reference times corresponding to a plurality of Hamming distances based on the pattern data stored in the reference array RA. Next, step S650 will be performed.

[0068] In step S640, the memory searching engine 100 calculates a plurality of updated reference voltages corresponding to a plurality of Hamming distances based on the pattern data stored in the reference array RA. Next, step S650 will be performed.

[0069] In step S650, the memory searching engine 100 updates the stored original reference times corresponding to the plurality of Hamming distances according to the plurality of updated reference times, or updates the stored original reference voltages corresponding to the plurality of Hamming distances according to the plurality of updated reference voltages.

[0070] It should be noted that the number and order of steps in the reference calibrating method 600 in present disclosure are only examples, and are not intended to limit the present disclosure. The other number and order of steps in the reference calibrating method 600 are within the scope

of the present disclosure. In some embodiments, step S620 can be omitted, steps S630 and S640 can be performed sequentially, and then step S650 is performed.

[0071] Through the memory searching engine, reference array and reference calibrating method in present disclosure, the reference time and reference voltage corresponding to different Hamming distances can be updated regularly to respond to shifts in electronic properties and changes in discharge curves of bit lines due to long-term data storage or temperature changes inside the memory, so as to maintain the normal operation of the data searching function.

[0072] The above are preferred embodiments of the present disclosure. It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present disclosure without departing from the scope or spirit of the present disclosure. In view of the foregoing, it is intended that the present disclosure cover modifications and variations of this disclosure provided they fall within the scope of the following claims and their equivalents.

What is claimed is:

1. A memory searching engine, storing at least one reference time and at least one reference voltage corresponding to a plurality of Hamming distances, wherein the memory searching engine comprises:

a data array, storing at least one first pattern data and configured to perform a data searching according to the difference between at least one input data and the at least one first pattern data, so as to generate a searching result; and

a reference array, storing at least one second pattern data and configured to receive the at least one input data,

wherein the memory searching engine is further configured to calculate a plurality of updated reference times and a plurality of updated reference voltages corresponding to the plurality of Hamming distances based on the at least one second pattern data and perform a reference calibrating, so as to update the at least one reference time according to the plurality of updated reference times, or update the at least one reference voltage according to the plurality of updated reference voltages.

2. The memory searching engine of claim 1, wherein the reference array comprises a plurality of bit lines and a plurality of Not-AND (NAND) strings, the plurality of NAND strings are each coupled between one of the plurality of bit lines and a common source line, and

wherein the plurality of NAND strings are configured to store the at least one second pattern data, and ones of the plurality of NAND strings coupled to the same bit line respectively store a plurality of portions of the at least one second pattern data, and the plurality of portions are same to each other.

3. The memory searching engine of claim 1, wherein the at least one second pattern data comprises a plurality of second pattern data in different types, and

wherein a plurality of combinations of the at least one input data and the plurality of second pattern data correspond to the plurality of Hamming distances, and one of the at least one reference time corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference times, and one of the at least one reference voltage corresponding to each of the

plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference voltages.

4. The memory searching engine of claim 1, wherein the at least one input data comprises a plurality of input data in different types, and

wherein a plurality of combinations of the plurality of input data and the at least one second pattern data correspond to the plurality of Hamming distances, and one of the at least one reference time corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference times, and one of the at least one reference voltage corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference voltages.

5. The memory searching engine of claim 1, wherein the at least one input data comprises a plurality of input data in different types, the at least one second pattern data comprises a plurality of second pattern data in different types, and

wherein a plurality of combinations of the plurality of input data and the plurality of second pattern data correspond to the plurality of Hamming distances, and one of the at least one reference time corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference times, and one of the at least one reference voltage corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference voltages.

6. The memory searching engine of claim 1, wherein the reference calibrating is performed before the data searching is performed, or the reference calibrating is performed every other a calibration cycle.

7. The memory searching engine of claim 1, wherein each of the first pattern data comprises m features, each of the second pattern data comprises m features, wherein m is an integer.

8. A reference array, arranged in a memory searching engine, wherein the memory searching engine stores at least one reference time and at least one reference voltage corresponding to a plurality of Hamming distances, and the memory searching engine comprises a data array storing at least one first pattern data,

wherein the reference array is configured to store at least one second pattern data and configured to receive at least one input data, and

wherein the at least one second pattern data is configured to be provided to the memory searching engine, so as to calculate a plurality of updated reference times and a plurality of updated reference voltages corresponding to the plurality of Hamming distances, and allow the memory searching engine to perform a reference calibrating, so as to update the at least one reference time according to the plurality of updated reference times, or update the at least one reference voltage according to the plurality of updated reference voltages.

9. The reference array of claim 8, wherein the reference array comprises a plurality of bit lines and a plurality of

Not-AND (NAND) strings, the plurality of NAND strings are each coupled between one of the plurality of bit lines and a common source line, and

wherein the plurality of NAND strings are configured to store the at least one second pattern data, and ones of the plurality of NAND strings coupled to the same bit line respectively store a plurality of portions of the at least one second pattern data, and the plurality of portions are same to each other.

10. The reference array of claim 8, wherein the at least one second pattern data comprises a plurality of second pattern data in different types, and

wherein a plurality of combinations of the at least one input data and the plurality of second pattern data correspond to the plurality of Hamming distances, and one of the at least one reference time corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference times, and one of the at least one reference voltage corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference voltages.

11. The reference array of claim 8, wherein the at least one input data comprises a plurality of input data in different types, and

wherein a plurality of combinations of the plurality of input data and the at least one second pattern data correspond to the plurality of Hamming distances, and one of the at least one reference time corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference times, and one of the at least one reference voltage corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference voltages.

12. The reference array of claim 8, wherein the at least one input data comprises a plurality of input data in different types, the at least one second pattern data comprises a plurality of second pattern data in different types, and

wherein a plurality of combinations of the plurality of input data and the plurality of second pattern data correspond to the plurality of Hamming distances, and one of the at least one reference time corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference times, and one of the at least one reference voltage corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference voltages.

13. The reference array of claim 8, wherein the reference calibrating is performed before a data searching is performed by the memory searching engine, or the reference calibrating is performed every other a calibration cycle.

14. The reference array of claim 8, wherein each of the first pattern data comprises m features, each of the second pattern data comprises m features, wherein m is an integer.

15. A reference calibrating method, suitable for a memory search engine comprising a data array and a reference array, wherein the memory searching engine stores at least one reference time and at least one reference voltage corresponding to a plurality of Hamming distances, and the data array

stores at least one first pattern data, the reference array stores at least one second pattern data, wherein the reference calibrating method comprises:

- receiving, by the reference array, at least one input data;
- calculating, by the memory search engine, a plurality of updated reference times and a plurality of updated reference voltages corresponding to the plurality of Hamming distances, based on the at least one second pattern data; and
- updating, by the memory search engine, the at least one reference time according to the plurality of updated reference times, or the at least one reference voltage according to the plurality of updated reference voltages.

16. The reference calibrating method of claim **15**, wherein the reference array comprises a plurality of bit lines and a plurality of Not-AND (NAND) strings, the plurality of NAND strings are each coupled between one of the plurality of bit lines and a common source line, and

wherein the plurality of NAND strings are configured to store the at least one second pattern data, and ones of the plurality of NAND strings coupled to the same bit line respectively store a plurality of portions of the at least one second pattern data, and the plurality of portions are same to each other.

17. The reference calibrating method of claim **15**, wherein the at least one second pattern data comprises a plurality of second pattern data in different types, and

wherein a plurality of combinations of the at least one input data and the plurality of second pattern data correspond to the plurality of Hamming distances, and one of the at least one reference time corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference times, and one of the at least one reference voltage corresponding to each of the plurality of Hamming distances is configured to be

updated according to at least one of the plurality of updated reference voltages.

18. The reference calibrating method of claim **15**, wherein the at least one input data comprises a plurality of input data in different types, and

wherein a plurality of combinations of the plurality of input data and the at least one second pattern data correspond to the plurality of Hamming distances, and one of the at least one reference time corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference times, and one of the at least one reference voltage corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference voltages.

19. The reference calibrating method of claim **15**, wherein the at least one input data comprises a plurality of input data in different types, the at least one second pattern data comprises a plurality of second pattern data in different types, and

wherein a plurality of combinations of the plurality of input data and the plurality of second pattern data correspond to the plurality of Hamming distances, and one of the at least one reference time corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference times, and one of the at least one reference voltage corresponding to each of the plurality of Hamming distances is configured to be updated according to at least one of the plurality of updated reference voltages.

20. The reference calibrating method of claim **15**, wherein the reference calibrating method is performed before a data searching is performed by the memory searching engine, or the reference calibrating method is performed every other a calibration cycle.

* * * * *