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MEMORY DEVICE, MEMORY SYSTEM, MEMORY CONTROLLER, AND OPERATION METHOD

Abstract

Examples of the present application provide a memory device, a memory system, a memory controller, and an operation method. The memory device includes: an array of memory cells comprising multiple memory cells, wherein a preset number of memory cells form one codeword; and a peripheral circuit coupled with the array of memory cells and configured to: obtain a first result corresponding to at least one codeword at a target read voltage; obtain a first threshold according to the corresponding first result at the target read voltage; make at least one adjustment to the target read voltage, and after each adjustment, obtain a corresponding first result at the adjusted target read voltage; and determine a target valley voltage.

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Background/Summary

TECHNICAL FIELD
[0002] Examples of the present application relates to the technical field of semiconductors, and particularly to a memory device, a memory system, a memory controller, and an operation method.

BACKGROUND
[0003] With the development of science and technology, the market scale of the integrated circuit industry becomes increasingly larger, and the process and technology of non-volatile memory devices in the entire integrated circuit industry have been developing rapidly in recent years, with NAND memories being particularly widely used. The NAND memories implement the function of data storage by capturing and storing charges in a gate medium layer of memory cells contained therein. However, as the use time increases, charges stored in memory cells vary due to the increasing use time, repeated read operations, cross temperature, etc., thus affecting the correctness of reading data stored in the memory cells.

SUMMARY
[0004] In view of this, examples of the present application provide a memory device, a memory system, a memory controller, and an operation method.

[0005] In a first aspect, examples of the present application provide a memory device. The memory device comprises: an array of memory cells comprising multiple memory cells, wherein a preset number of memory cells form one codeword; and peripheral circuit coupled with the array of memory cells and configured to: obtain a first result corresponding to at least one codeword at a target read voltage, wherein the first result comprises the number of bits which represents the number of bits in the at least one codeword which are flipped in two read results at a first read voltage and a second read voltage, and a difference between the first read voltage and the second read voltage is less than a preset voltage; obtain a first threshold according to the corresponding first result at the target read voltage, wherein the first threshold is to represent a corresponding first result at a maximum value in an effective range of predicted valley voltages; make at least one adjustment to the target read voltage, and after each adjustment, obtain a corresponding first result at the adjusted target read voltage; and determine a target valley voltage according to a relationship between a corresponding first result at a target read voltage after one adjustment and the first threshold meeting a first preset condition or according to a corresponding first result at the target read voltage after multiple adjustments meeting a second preset condition, wherein the target valley voltage is taken as a read voltage at which a read operation is performed on the at least one codeword.

[0006] In some examples, the peripheral circuit is configured to: obtain the first threshold according to the corresponding first result at the target read voltage and a first mapping function, wherein the first mapping function is to represent a relationship between the corresponding first result at the maximum value in the effective range of predicted valley voltages and the corresponding first result at the target read voltage.

[0007] In some examples, the peripheral circuit is configured to: obtain the corresponding first result at the maximum value in the effective range of predicted valley voltages according to an initial value of the corresponding first result at the maximum value in the effective range of predicted valley voltages, a correction value for the corresponding first result at the target read

voltage, and a correction coefficient, wherein the initial value of the corresponding first result at the maximum value in the effective range of predicted valley voltages and the correction coefficient are both fixed values related to a stage in which a read voltage is, and the larger the corresponding first result at the target read voltage is, the larger the correction value is.

[0008] In some examples, the first preset condition is that a corresponding first result at the target read voltage after one adjustment is less than the first threshold; and the peripheral circuit is configured to: determine the target read voltage after one adjustment as the target valley voltage according to the relationship between the corresponding first result at the target read voltage after one adjustment and the first threshold meeting the first preset condition.

[0009] In some examples, the peripheral circuit is configured to: according to the corresponding first result at the target read voltage being greater than or equal to the first threshold, obtain, with the corresponding first result at the target read voltage, a target adjustment value for adjusting the target read voltage; obtain a corresponding first result at the adjusted target read voltage with the target adjustment value; according to the corresponding first result at the adjusted target read voltage with the target adjustment value being less than the first threshold, determine the adjusted target read voltage with the target adjustment value as the target valley voltage; and according to the corresponding first result at the adjusted target read voltage with the target adjustment value being greater than or equal to the first threshold, make multiple adjustments to the target read voltage, and after each adjustment, obtain the corresponding first result at the adjusted target read voltage, until the corresponding first result at the adjusted target read voltage is less than the first threshold or the corresponding first result at the target read voltage after multiple adjustments meet the second preset condition.

[0010] In some examples, the second preset condition is that taken the minimum first result among multiple corresponding first results at the target read voltages after multiple adjustments as a reference value, the number of first results from remaining first results which differ from the reference value with a difference being less than a second threshold is greater than a preset number; and the peripheral circuit is configured to: according to the corresponding first result at the target read voltage after multiple adjustments meeting the second preset condition, take a target read voltage corresponding to the minimum first result among the multiple first results as the target valley voltage.

[0011] In some examples, the peripheral circuit is configured to: in a process of making multiple adjustments to the target read voltage, make adjustments by employing different adjustment methods, and according to the adjusted target read voltages corresponding to more than a preset number of adjustment methods in the different adjustment methods being same and the corresponding first result at the same target read voltage being the minimum value among all first results, take the same target read voltage as the target valley voltage.

[0012] In some examples, the peripheral circuit is configured to: make multiple first adjustments to the target read voltage with a first step size, and obtain corresponding first results at target read voltages after the multiple first adjustments respectively; determine a value of knee point according to the obtained corresponding first results at the read voltages after the multiple first adjustments, wherein a target read voltage corresponding to the value of knee point is a knee-point voltage; make multiple second adjustments to the knee-point voltage with a second step size, and obtain the corresponding first results at the target read voltages after the multiple second adjustments respectively, wherein the second step size is less than the first step size; and determine the target valley voltage with the obtained corresponding first results at the target read voltages after the multiple second adjustments.

[0013] In some examples, the corresponding first results at the target read voltages after the multiple first adjustments comprise a first adjacent value and a second adjacent value that are adjacent to the value of knee point, and the peripheral circuit is configured to: according to a difference between the first adjacent value and the value of knee point being less than a difference

between the second adjacent value and the value of knee point, narrow a range for the multiple second adjustments to be between a target read voltage corresponding to the first adjacent value and the knee-point voltage; and take an average of the read voltage corresponding to the first adjacent value and the knee-point voltage, and according to a corresponding first result at the average being less than the first threshold, take the average as the target valley voltage; and according to the corresponding first result at the average being greater than or equal to the first threshold, continue to make a second adjustment between the read voltage corresponding to the first adjacent value and the knee-point voltage, until a corresponding first result at the adjusted target read voltage is less than the first threshold.

[0014] In some examples, the peripheral circuit is configured to: obtain the predicted valley voltage according to the corresponding first result at the target read voltage and a second mapping function, wherein the second mapping is to represent a relationship between the corresponding first result at the target read voltage and the predicted valley voltage.

[0015] In some examples, the memory cell comprises multiple memory bits, and the multiple memory bits correspond to multiple pages respectively; and at least part of pages correspond to multiple stages, the multiple stages comprise a first stage and a second stage, and a read voltage in the second stage is less than a read voltage in the first stage; and the peripheral circuit is configured to: obtain at least one of a predicted valley voltage in the second stage from the multiple stages or a target valley voltage in other first stage corresponding to a lower read voltage with the determined target valley voltage according to the stage number corresponding to the determined target valley voltage belonging to the first stage.

[0016] In some examples, the peripheral circuit is configured to: read storage data of the at least one codeword at the first read voltage, to obtain a second result; read storage data of the at least one codeword at the second read voltage, to obtain a third result; perform a logical operation on the second result and the third result, to obtain a fourth result; and count the number of bits in the fourth result which represent flip of bits in the third result relative to the second result, to obtain the first result.

[0017] In some examples, the peripheral circuit comprises: a first latch, a second latch, and a third latch; the first latch is configured to store the second result; the second latch is configured to store the third result; and the third latch is configured to store the fourth result.

[0018] In a second aspect, examples of the present application provide a memory system. The memory system comprises: one or more of any memory devices provided in the first aspect; and a memory controller coupled with the memory device and controlling the memory device.

[0019] In a third aspect, examples of the present application provide a memory controller. The memory controller comprises a control component and is configured to: obtain a first result corresponding to at least one codeword at a target read voltage, wherein the at least one codeword is formed by a preset number of memory cells in an array of memory cells of at least one memory device coupled with the memory controller, wherein the first result comprises the number of bits which represents the number of bits in the at least one codeword which are flipped in two read results at a first read voltage and a second read voltage, and a difference between the first read voltage and the second read voltage is less than a preset voltage; obtain a first threshold according to the corresponding first result at the target read voltage, wherein the first threshold is to represent a corresponding first result at a maximum value in an effective range of predicted valley voltages; make at least one adjustment to the target read voltage, and after each adjustment, obtain a first result corresponding to the at least one codeword at the adjusted target read voltage; and determine a target valley voltage according to a relationship between a corresponding first result at a target read voltage after one adjustment and the first threshold meeting a first preset condition or according to a corresponding first result at the target read voltage after multiple adjustments meeting a second preset condition, wherein the target valley voltage is taken as a read voltage at which a read operation is performed on the at least one codeword.

[0020] In some examples, the control component is configured to: obtain the first threshold according to the corresponding first result at the target read voltage and a first mapping function, wherein the first mapping function is to represent a relationship between the corresponding first result at the maximum value in the effective range of predicted valley voltages and the corresponding first result at the target read voltage.

[0021] In some examples, the control component is configured to: obtain the corresponding first result at the maximum value in the effective range of predicted valley voltages according to an initial value of the corresponding first result at the maximum value in the effective range of predicted valley voltages, a correction value for the corresponding first result at the target read voltage, and a correction coefficient, wherein the initial value of the corresponding first result at the maximum value in the effective range of predicted valley voltages and the correction coefficient are both fixed values related to a stage in which a read voltage is, and the larger the corresponding first result at the target read voltage is, the larger the correction value is.

[0022] In some examples, the first preset condition is that a corresponding first result at the target read voltage after one adjustment is less than the first threshold; and the control component is configured to: determine the target read voltage after one adjustment as the target valley voltage according to the relationship between the corresponding first result at the target read voltage after one adjustment and the first threshold meeting the first preset condition.

[0023] In some examples, the control component is configured to: according to the corresponding first result at the target read voltage being greater than or equal to the first threshold, obtain, with the corresponding first result at the target read voltage, a target adjustment value for adjusting the target read voltage; obtain a corresponding first result at the adjusted target read voltage with the target adjustment value; according to the corresponding first result at the adjusted target read voltage with the target adjustment value being less than the first threshold, determine the adjusted target read voltage with the target adjustment value as the target valley voltage; and according to the corresponding first result at the adjusted target read voltage with the target adjustment value being greater than or equal to the first threshold, make multiple adjustments to the target read voltage, and after each adjustment, obtain the corresponding first result at the adjusted target read voltage, until the corresponding first result at the adjusted target read voltage is less than the first threshold or the corresponding first result at the target read voltage after multiple adjustments meet the second preset condition.

[0024] In some examples, the second preset condition is that taken the minimum first result among multiple corresponding first results at the target read voltages after multiple adjustments as a reference value, the number of first results from remaining first results which differ from the reference value with a difference being less than a second threshold is greater than a preset number; and the control component is configured to: according to the corresponding first result at the target read voltage after multiple adjustments meeting the second preset condition, take a target read voltage corresponding to the minimum first result among the multiple first results as the target valley voltage.

[0025] In some examples, the control component is configured to: in a process of making multiple adjustments to the target read voltage, make adjustments by employing different adjustment methods, and according to the adjusted target read voltages corresponding to more than a preset number of adjustment methods in the different adjustment methods being same and the corresponding first result at the same target read voltage being the minimum value among all first results, take the same target read voltage as the target valley voltage.

[0026] In some examples, the control component is configured to: [0027] make multiple first adjustments to the target read voltage with a first step size, and obtain corresponding first results at target read voltages after the multiple first adjustments respectively; [0028] determine a value of knee point according to the obtained corresponding first results at the read voltages after the multiple first adjustments, wherein a target read voltage corresponding to the value of knee point is

a knee-point voltage; make multiple second adjustments to the knee-point voltage with a second step size, and obtain the corresponding first results at the target read voltages after the multiple second adjustments respectively, wherein the second step size is less than the first step size; and determine the target valley voltage with the obtained corresponding first results at the target read voltages after the multiple second adjustments.

[0029] In some examples, the corresponding first results at the target read voltages after the multiple first adjustments comprise a first adjacent value and a second adjacent value that are adjacent to the value of knee point, and the control component is configured to: according to a difference between the first adjacent value and the value of knee point being less than a difference between the second adjacent value and the value of knee point, narrow a range for the multiple second adjustments to be between a target read voltage corresponding to the first adjacent value and the knee-point voltage; and take an average of the read voltage corresponding to the first adjacent value and the knee-point voltage, and according to a corresponding first result at the average being less than the first threshold, take the average as the target valley voltage; and according to the corresponding first result at the average being greater than or equal to the first threshold, continue to make a second adjustment between the read voltage corresponding to the first adjacent value and the knee-point voltage, until a corresponding first result at the adjusted target read voltage is less than the first threshold.

[0030] In some examples, the control component is configured to: obtain the predicted valley voltage according to the corresponding first result at the target read voltage and a second mapping function, wherein the second mapping is to represent a relationship between the corresponding first result at the target read voltage and the predicted valley voltage, wherein the predicted valley voltage comprises a relationship between adjusted read voltages with the target adjustment value.

[0031] In some examples, the memory cell comprises multiple memory bits, and the multiple memory bits correspond to multiple pages respectively; and at least part of pages comprise multiple stages, the multiple stages comprise a first stage and a second stage, and a read voltage in the second stage is less than a read voltage in the first stage; and the control component is configured to: obtain at least one of a predicted valley voltage in the second stage from the multiple stages or a target valley voltage in other first stage corresponding to a lower read voltage with the determined target valley voltage according to the stage number corresponding to the determined target valley voltage belonging to the first stage.

[0032] In some examples, the memory controller is further configured to: control the memory device to perform a read operation on the at least one codeword with the target read voltage; and in response to an error occurring in reading of data in the at least one codeword at the target read voltage, control the memory device to perform the read operation on the codeword with the target valley voltage.

[0033] In some examples, the memory controller is further configured to: in response to an error occurring in reading of data in the at least one codeword at the target valley voltage, perform an ECC decoding operation on the data of the at least one codeword read at the target valley voltage.

[0034] In a fourth aspect, examples of the present application provide a method of operating a memory device. The operation method comprises: obtaining a first result corresponding to at least one codeword at a target read voltage, the at least one codeword is formed by a preset number of memory cells in an array of memory cells of a memory device, wherein the first result comprises the number of bits in the at least one codeword which are flipped in two read results at a first read voltage and a second read voltage, and a difference between the first read voltage and the second read voltage is less than a preset voltage; obtaining a first threshold according to the corresponding first result at the target read voltage, wherein the first threshold is to represent a corresponding first result at a maximum value in an effective range of predicted valley voltages; making at least one adjustment to the target read voltage, and after each adjustment, obtaining a corresponding first result at the adjusted read voltage; and determining a target valley voltage according to a

relationship between a corresponding first result at a target read voltage after one adjustment and the first threshold meeting a first preset condition or according to a corresponding first result at the target read voltage after multiple adjustments meeting a second preset condition, wherein the target valley voltage is taken as a read voltage at which a read operation is performed on the at least one codeword.

[0035] In a fifth aspect, examples of the present application provide a method of operating a memory system, wherein the memory system comprises a memory device and a memory controller coupled with the memory device and controlling the memory device, and the operation method comprises: performing the operation method of the memory device provided in the fourth aspect.

[0036] In a sixth aspect, examples of the present application provide a method of operating a memory controller. The operation method comprises: obtaining a first result corresponding to at least one codeword at a target read voltage, wherein the at least one codeword is formed by a preset number of memory cells in at least one memory device coupled with the memory controller, wherein the first result comprises the number of bits which represents the number of bits in the at least one codeword which are flipped in two read results at a first read voltage and a second read voltage, and a difference between the first read voltage and the second read voltage is less than a preset voltage; obtaining a first threshold according to the corresponding first result at the target read voltage, wherein the first threshold is to represent a corresponding first result at a maximum value in an effective range of predicted valley voltages; making at least one adjustment to the target read voltage, and after each adjustment, obtaining a corresponding first result at the adjusted target read voltage; and determining a target valley voltage according to a relationship between a corresponding first result at a target read voltage after one adjustment and the first threshold meeting a first preset condition or according to a corresponding first result at the target read voltage after multiple adjustments meeting a second preset condition, wherein the target valley voltage is taken as a read voltage at which a read operation is performed on the at least one codeword.

[0037] In a seventh aspect, examples of the present application provide a storage medium having executable instructions stored thereon, which, when being executed by a processor, implement any operation in any operation method provided in the fourth aspect, the fifth aspect, and the sixth aspect.

[0038] In the memory device and the operation method thereof and the memory system and the operation method thereof provided in the examples of the present application, a first result (a size of the first result may be several bytes) rather than at least one codeword (for example, a size of the codeword may be 4 KB) is transmitted, so that an amount of data transmitted by the memory device is reduced. A first threshold is obtained according to a corresponding first result at a target read voltage. With the dynamic first threshold, the iterative rapidity of convergence of determining a target valley voltage is higher. A process of obtaining the first result converges inside the memory device, does not occupy, for example, a space of the memory controller, and has low dependency on, for example, the memory controller. At least one of a transmission time at an input/output port of the memory device or a time of an error correction decoding operation of the memory controller is reduced, so that an iterative time of an error correction decoding algorithm of the memory controller is saved, and a speed of error correction decoding is higher. The methods are applicable to a memory device/memory system of an MLC, a TLC type or a QLC type.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

[0039] In the accompanying drawings, unless otherwise specified, identical or similar components or elements are represented by a like numeral throughout several figures. These accompanying drawings are not necessarily drawn to scale. It is understood that these accompanying drawings

depict only several implementations disclosed in accordance with the present application and are not to be considered limiting of the scope of the present application.

[0040] FIG. **1** is a schematic diagram of an example system having a memory system according to an example of the present application;

[0041] FIG. **2**A is a schematic diagram of an example memory card having a memory system according to an example of the present application;

[0042] FIG. **2**B is a schematic diagram of an example solid-state drive having a memory system according to an example of the present application;

[0043] FIG. **3** is a schematic diagram of an example memory comprising a peripheral circuit according to an example of the present application;

[0044] FIG. **4** is a schematic cross-sectional view of an array of memory cells comprising a NAND memory string according to an example of the present application;

[0045] FIG. **5** is a schematic diagram of an example memory device comprising an array of memory cells and a peripheral circuit according to an example of the present application;

[0046] FIG. **6** is a schematic diagram of an example flow of a read operation of a memory system provided by the present application;

[0047] FIG. **7** is a schematic diagram of the implementation process of operating a method that peripheral circuit of a memory device provided by an example of the present application is configured to perform;

[0048] FIG. **8**A is a schematic diagram of a threshold voltage distribution corresponding to a memory cell comprising 2 memory bits provided by an example of the present application;

[0049] FIG. **8**B is a schematic diagram of a threshold voltage distribution corresponding to a memory cell comprising 3 memory bits provided by an example of the present application;

[0050] FIG. **8**C is a schematic diagram of a threshold voltage distribution corresponding to a memory cell comprising 4 memory bits provided by an example of the present application;

[0051] FIG. **9**A is a schematic diagram of a method for confirming a predicted valley voltage/target valley voltage in a first stage and a second stage corresponding to a lower page shown in FIG. **8**B provided by an example of the present application;

[0052] FIG. **9**B is a schematic diagram of a method for confirming a predicted valley voltage/target valley voltage in a first stage and a second stage corresponding to a middle page shown in FIG. **8**B provided by an example of the present application;

[0053] FIG. **9**C is a schematic diagram of a method for confirming a predicted valley voltage/target valley voltage in a first stage and a second stage corresponding to a upper page shown in FIG. **8**B provided by an example of the present application;

[0054] FIG. **9**D is an enlarged schematic diagram of a rectangular dash box region in FIG. **9**A;

[0055] FIG. **9**E is an enlarged schematic diagram of a rectangular dash box region in FIG. **9**B;

[0056] FIG. **9**F is an enlarged schematic diagram of a rectangular dash box region in FIG. **9**C;

[0057] FIG. **10**A is a schematic diagram **1** of a method for confirming a fifth-level read voltage corresponding to a lower page shown in FIG. **9**A provided by an example of the present application;

[0058] FIG. **10**B is a schematic diagram **2** of a method for confirming a fifth-level read voltage corresponding to a lower page shown in FIG. **9**A provided by an example of the present application;

[0059] FIG. **10**C is a schematic diagram **3** of a method for confirming a fifth-level read voltage corresponding to a lower page shown in FIG. **9**A provided by an example of the present application;

[0060] FIG. **10**D is a schematic diagram **4** of a method for confirming a fifth-level read voltage corresponding to a lower page shown in FIG. **9**A provided by an example of the present application;

[0061] FIG. **10**E is a schematic diagram **1** of a method for confirming a seventh-level read voltage

corresponding to an upper page shown in FIG. **9**C provided by an example of the present application;

[0062] FIG. **10**F is a schematic diagram **2** of a method for confirming a seventh-level read voltage corresponding to an upper page shown in FIG. **9**C provided by an example of the present application;

[0063] FIG. **10**G is a schematic diagram **3** of a method for confirming a seventh-level read voltage corresponding to an upper page shown in FIG. **9**C provided by an example of the present application;

[0064] FIG. **11** is a schematic diagram of an example structure having a memory system provided by an example of the present application;

[0065] FIG. **12** is a block diagram of a memory system provided by an example of the present application;

[0066] FIGS. **13**A and **13**B (which may be referred to herein collectively as FIG. **13**) are block flowcharts **1** of a method of operating a memory device provided by an example of the present application;

[0067] FIGS. **14**A, **14**B, **14**C, and **14**D (which may be referred to herein collectively as FIG. **14**) are block flowcharts **2** of a method of operating a memory device provided by an example of the present application;

[0068] FIG. **15** is a timing diagram of starting a single-level read mode operation provided in an example of the present application;

[0069] FIG. **16** is a timing diagram of a predicted valley voltage/target valley voltage and performing a read operation provided by an example of the present application; and

[0070] FIG. **17** is a schematic diagram of a structure of a storage medium provided by examples of the present application.

DETAILED DESCRIPTION

[0071] Example implementations disclosed by the present application will be described below in more detail with reference to the drawings. Although example implementations of the present application are shown in the drawings, it is to be understood that, the present application may be implemented in various form without being limited by the specific implementations as set forth herein. Rather, these implementations are provided in order for understanding the present application more thoroughly, and can fully convey the scope disclosed by the present application to those skilled in the art.

[0072] In the description below, many specific details are presented to provide a more thorough understanding of the present application. However, it is apparent to those skilled in the art that the present application may be carried out without one or more of these details. In other examples, in order to avoid confusing with the present application, some technical features well-known in the art are not described; that is, not all features of actual examples are described herein, and well-known functions and structures are not described in detail.

[0073] In addition, the accompanying drawings are only schematic illustration of the present application, and are not necessarily drawn to scale. Same reference numerals in the figures represent same or similar parts. Therefore, repeated description thereof is omitted. Some block diagrams shown in the accompanying drawings are functional entities and do not necessarily have to correspond to physically or logically independent entities. These functional entities can be implemented in software form, or these functional entities can be implemented in one or more hardware modules or integrated circuits, or these functional entities can be implemented in different networks and/or processor apparatuses and/or microcontroller apparatuses.

[0074] A flow chart shown in the accompanying drawings is only an example description, but does not have to comprise all operations. For example, some operations may be further decomposed, and some operations may be combined or partially combined. Therefore, an actual execution sequence may be changed according to an actual case.

[0075] The terms used herein are only intended to describe the examples, and are not used as limitations of the present application. As used herein, unless otherwise indicated expressly in the context, "a", "an" and "the" in a singular form are also intended to comprise a plural form. It is also to be understood that the terms "consist of" and/or "comprise", when used in this specification, determine the presence of the feature, integer, step, operation, element and/or component, but do not preclude the presence of one or more of other features, integers, operations, operations, elements, components, and/or groups. As used herein, the term "and/or" comprises any and all combinations of related items listed.

[0076] The memory device in the examples of the present application comprises, but is not limited to, a three-dimensional NAND memory. In order to facilitate understanding, the illustration is made by taking the three-dimensional NAND memory as an example.

[0077] FIG. **1** shows a block diagram of an example system **100** having a memory device according to some aspects of the present application. The system **100** may be a mobile phone, a desktop computer, a laptop computer, a tablet computer, a vehicle computer, a gaming console, a printer, a positioning apparatus, a wearable electronic apparatus, a smart sensor, a Virtual Reality (VR) apparatus, an Augmented Reality (AR) apparatus, or any other suitable electronic apparatus having a memory. As shown in FIG. **1**, the system **100** may comprise a host **108** and a memory system **102**. The memory system **102** has one or more memory devices **104** and a memory controller **106**. The host **108** may be a processor (e.g., a central processing unit (CPU)) or a system on a chip (SOC) (e.g., an application processor (AP)) of an electronic apparatus. The host **108** may be configured to send or receive data to or from memory devices **104**.

[0078] According to some implementations, the memory controller **106** is coupled to the memory devices **104** and the host **108**, and configured to control the memory devices **104**. The memory controller **106** can manage the data stored in the memory devices **104** and communicate with the host **108**. In some implementations, the memory controller **106** is designed for operating in a low duty-cycle environment, such as secure digital (SD) cards, Compact Flash (CF) Cards, Universal Serial Bus (USB) flash drives, or other media for use in electronic apparatuses, such as personal computers, digital cameras, mobile phones, etc.

[0079] In some implementations, the memory controller **106** is designed for operating in high duty-cycle environment Solid-State Drives (SSDs) or embedded Multi-Media Cards (eMMCs) used as data memories for mobile devices, such as smartphones, tablets, laptop computers, etc., and enterprise memory arrays.

[0080] The memory controller **106** may be configured to control operations of the memory device **104**, such as read, erase, and program operations. The memory controller **106** may further be configured to manage various functions with respect to data stored or to be stored in the memory device **104**, comprising, but not limited to, bad-block management, garbage collection, logical-to-physical address conversion, wear leveling, etc. In some implementations, the memory controller **106** is further configured to process error correction codes (ECCs) with respect to the data read from or written to the memory device **104**.

[0081] The memory controller **106** may further perform any other suitable functions as well, for example, formatting the memory devices **104**. The memory controller **106** may communicate with an external apparatus (e.g., the host **108**) according to a particular communication protocol. For example, the memory controller **106** may communicate with the external apparatus through at least one of various interface protocols, such as a USB protocol, an MMC protocol, a Peripheral Component Interconnect (PCI) protocol, a PCI-Express (PCI-E) protocol, an Advanced Technology Attachment (ATA) protocol, a Serial-ATA protocol, a Parallel-ATA protocol, a Small Computer System Interface (SCSI) protocol, an Enhanced Small Disk Interface (ESDI) protocol, an Integrated Drive Electronics (IDE) protocol, a Firewire protocol, etc.

[0082] The memory controller **106** and the one or more memory devices **104** can be integrated into various types of storage apparatuses, for example, be comprised in the same package, such as a

Universal Flash Storage (UFS) package or an eMMC package. That is, the memory system **102** may be implemented and packaged into different types of end electronic products.

[0083] In an example shown in FIG. **2**A, the memory controller **106** and a single memory device **104** may be integrated into a memory card **202**. The memory card **202** may comprise a PC card (PCMCIA, Personal Computer Memory Card International Association), a CF card, a Smart Media (SM) card, a memory stick, a Multimedia card (MMC, RS-MMC, MMCmicro), an SD card (SD, miniSD, microSD, SDHC), a UFS, etc. The memory card **202** may further comprise a memory card connector **204** coupling the memory card **202** with a host (e.g., the host **108** in FIG. **1**).

[0084] In another example shown in FIG. **2**B, the memory controller **106** and multiple memory devices **104** may be integrated into an SSD **206**. The SSD **206** may further comprise an SSD connector **208** coupling the SSD **206** with a host (e.g., the host **108** in FIG. **1**). In some implementations, at least one of a storage capacity or operation Speed of the SSD **206** is greater than at least one of a storage capacity or operation Speed of the memory card **202**.

[0085] In some examples, each memory block may be coupled to multiple word lines. Multiple memory cells coupled to each word line form a physical page.

[0086] FIG. **3** illustrates a schematic circuit diagram of an example memory device **300** comprising a peripheral circuit according to some aspects of the present application. The memory device **300** may be an example of the memory device **104** in FIG. **1**. The memory device **300** may comprise an array of memory cells **301** and a peripheral circuit **302** coupled to the array of memory cells **301**. For example, the array of memory cells **301** is a three-dimensional NAND memory cell array. A memory cell **306** is a NAND memory cell. The memory cell **306** is provided in the form of an array of memory strings **308**. Each memory string **308** vertically extends above a substrate (not shown). In some implementations, each memory string **308** comprises multiple memory cells **306** coupled in series and stacked vertically. Each memory cell **306** may maintain a continuous analog value, such as voltage or charge, which depends on a number of electrons trapped within a region of the memory cell **306**. Each memory cell **306** may be either a floating gate type memory cell that comprises a floating gate transistor, or a charge trap type memory cell that comprises a charge trap transistor.

[0087] In some implementations, each memory cell **306** is a Single Level Cell (SLC) that has two possible memory states and thus may store one bit of data. For example, a first memory state "0" may correspond to a first voltage range, and a second memory state "1" may correspond to a second voltage range. In some implementations, each memory cell **306** is a Multi-Level Cell (MLC) that can store more than one bit of data in more than four memory states. For example, the MLC can store two bits per cell (which may also be called a double-level cell), three bits per cell (also called a trinary-level cell (TLC)), four bits per cell (also called a quad-level cell (QLC)), five bits per cell (also called a penta-level cell (PLC)), or more than five bits per cell. Each MLC can be programmed to assume a range of possible nominal storage values. In an example, if each MLC stores two bits of data, the MLC can be programmed to employ one of three possible program levels from an erase state by writing one of three possible nominal storage values to the cell, and a fourth nominal storage value may be used to represent the erase state.

[0088] It is to be noted that, the memory state here is a memory state of a memory cell in the present application. Different memory cells have different numbers of memory states. For example, a memory cell of an SLC type has 2 memory states (that is, two memory states). The 2 memory states comprise one programmed state and one erased state. In another example, a memory cell of an MLC type has 4 memory states. The 4 memory states comprise one erased state and three programmed states. In still another example, a memory cell of a TLC type has 8 memory states. The 8 memory states comprise one erased state and seven programmed states. In some implementations, a memory cell of a QLC type has 16 memory states. The 16 memory states comprise one erased state and fifteen programmed states.

[0089] As shown in FIG. **3**b, every memory string **308** may comprise a bottom selective transistor

(BSG) **310** (also referred to as a source side selective transistor) at a source terminal of the memory string and a top selective transistor (TSG) **312** (also referred to as a drain side selective transistor) at a drain terminal of the memory string. The BSG **310** and the TSG **312** may be configured to activate a selected memory string **308** during a read operation and a program operation. In some implementations, sources of memory strings **308** in a same memory block **304** are coupled through a same source line (SL) **314** (for example, a common SL). For example, according to some implementations, all the memory strings **308** in the same memory block **304** have an array common source (ACS). According to some implementations, the TSG **312** of each memory string **308** is coupled to a respective Bit Line (BL) **316**, and data may be read or written from the bit line **316** via an output bus (not shown). In some implementations, each memory string **308** is configured to be selected or unselected by applying a select voltage (e.g., above a threshold voltage of a transistor having the TSG **312**) or an unselect voltage (e.g., 0 V) to the respective TSG **312** via one or more TSG lines **313** and/or by applying a select voltage (e.g., above a threshold voltage of a transistor having the BSG **310**) or an unselect voltage (e.g., 0 V) to the respective BSG **310** via one or more BSG lines **315**.

[0090] As shown in FIG. **3**, the memory strings **308** may be organized into multiple memory blocks **304**, and each of the multiple memory blocks **304** may have a common source line **314** (e.g., coupled to the ground). In some implementations, each memory block **304** is a basic data unit for an erase operation, e.g., all of the memory cells **306** on the same memory block **304** are erased at the same time. In order to erase the cells **306** in a selected memory block **304**, the source lines **314** coupled to the selected memory block **304***a* as well as unselected memory blocks **304** that are in the same plane as the selected memory block **304***a* can be biased with an erase voltage (Vers, such as a high positive voltage (e.g., 20 V or higher)). It is to be understood that in some examples, the erase operation may be performed at a half memory block level, a quarter memory block level, or a level having any suitable number of memory blocks or any suitable fractions of a memory block. The memory cells **306** of adjacent ones of the memory strings **308** may be coupled through word lines **318** that select which row of memory cells **306** is affected by the read and program operations.

[0091] Referring to FIG. **3**, each memory cell **306** of the multiple memory cells is coupled to the respective word line **318**, and each memory string **308** is coupled to the respective bit line **316** through a respective select transistor (such as, the top select transistor (TSG) **312**).

[0092] FIG. **4** shows a schematic cross-sectional view of an example cell array **301** comprising a memory string **308** with NAND as an example according to some aspects of the present application. As shown in FIG. **4**, the NAND cell array **301** may comprise a stack structure **410**. The stack structure **410** comprises multiple gate layers **411** and multiple insulating layers **412** that are sequentially and alternately stacked and a channel structure that penetrates the gate layers **411** and the insulating layers **412** vertically. The channel structure is coupled with each gate layer to form a cell. The channel structure is coupled with the multiple gate layers in the stack structure **410** to form the memory string **308**. The gate layers **411** and the insulating layers **412** may be alternately stacked, and two adjacent gate layers **411** are spaced apart by one insulating layer **412**.

[0093] A constituent material of the gate layers **411** may comprise a conductive material. The conductive material includes, but is not limited to, tungsten (W), cobalt (Co), copper (Cu), aluminum (Al), polysilicon, doped silicon, silicides, or any combination thereof. In some implementations, each gate layer **411** comprises a metal layer, e.g., a tungsten layer. In some implementations, each gate layer **411** comprises a doped polysilicon layer. Each gate layer **411** may comprise a control gate around the cells. The gate layer **411** at the top of the stack structure **410** may extend laterally as an upper select gate line; the gate layer **411** at the bottom of the stack structure **410** may extend laterally as a lower select gate line; and the gate layers **411** that extend laterally between the upper select gate line and the lower select gate line may act as word line layers.

[0094] In some examples, the stack structure **410** may be disposed on a substrate **401**. The substrate **401** may comprise silicon (e.g., single crystalline silicon), silicon germanium (SiGe), gallium arsenide (GaAs), germanium (Ge), silicon on insulator (SOI), germanium on insulator (GOI), or any other suitable materials.

[0095] In some examples, the memory string **308** comprises a channel structure that extends through the stack structure **410** vertically. In some implementations, the channel structure comprises a channel hole filled with (one or more) semiconductor materials (e.g., as a semiconductor channel) and (one or more) dielectric materials (e.g., as a memory film). In some implementations, the semiconductor channel comprises silicon, e.g., polysilicon. In some implementations, the memory film is a composite dielectric layer comprising a tunneling layer, a storage layer (also known as a "charge trap/storage layer"), and a blocking layer. The channel structure may have a cylindrical shape (e.g., a pillar shape). According to some implementations, the semiconductor channel, the tunneling layer, the storage layer, and the blocking layer are arranged radially from the center toward the outer surface of the pillar in this order. The tunneling layer may comprise silicon oxide, silicon oxynitride, or any combination thereof. The storage layer may comprise silicon nitride, silicon oxynitride, or any combination thereof. The blocking layer may comprise silicon oxide, silicon oxynitride, a high dielectric constant (high-k) dielectric, or any combination thereof. In an example, the memory film can include a composite layer of silicon oxide/silicon oxynitride/silicon oxide (ONO).

[0096] Referring back to FIG. **3**, the peripheral circuit **302** may be coupled to the array of memory cells **301** through the bit lines **316**, the word lines **318**, the source lines **314**, the BSG lines **315** and the TSG lines **313**. The peripheral circuit **302** may include any suitable analog, digital, and hybrid signal circuits for facilitating the operations of the memory array **301** by applying and sensing voltage signals and/or current signals to and from each target memory cell **306** with bit lines **316**, the word lines **318**, the source lines **314**, the BSG lines **315**, and the TSG lines **313**. The peripheral circuit **302** may comprise various types of peripheral circuits formed using a metal-oxide-semiconductor (MOS) technology. For example, FIG. **5** illustrates some example peripheral circuits. The peripheral circuit comprises a page buffer/sense amplifier **504**, a column decoder/bit line driver **506**, a row decoder/word line driver **508**, a voltage generator **510**, a control logic **512**, a register **514**, an interface **516**, and a data bus **518**. It is to be understood that in some examples, additional peripheral circuits not shown in FIG. **5** may be comprised as well.

[0097] The page buffer/sense amplifier **504** may be configured to read and program (write) data from and to the cell array **301** according to a control signal from the control logic **512**. In one example, the page buffer/sense amplifier **504** may store program data (write data) to be programmed into the cell array **301**. In another example, the page buffer/sense amplifier **504** may execute a program verification operation to ensure that the data has been properly programmed into the memory cell **306** coupled to the selected word line **318**. In yet another example, the page buffer/sense amplifier **504** may also sense a low power signal from the bit line **316** that represents a data bit stored in the memory cell **306**, and amplifies a small voltage swing to a recognizable logic level in the read operation. The column decoder/bit line driver **506** may be configured to be controlled by the control logic **512** and select one or more memory strings **308** by applying a bit line voltage obtained from the voltage generator **510**.

[0098] The row decoder/word line driver **508** may be configured to be controlled by the control logic **512**, select/unselect the memory blocks **304** of the cell array **301**, and select/unselect the word lines **318** of the memory blocks **304**. The row decoder/word line driver **508** may be further configured to drive the word lines **318** using a word line voltage obtained from the voltage generator **510**. In some implementations, the row decoder/word line driver **508** may also select/unselect and drive the BSG line **315** and the TSG line **313**. As described below in detail, the row decoder/word line driver **508** is configured to execute the program operation on the cells **306** that are coupled to (one or more) selected word line **318**. The voltage generator **510** may be

configured to be controlled by the control logic **512** and obtain a word line voltage (such as, a read voltage, a program voltage, a pass voltage, a channel boost voltage, a verify voltage, etc.), a bit line voltage, and a source line voltage to be supplied to the cell array **301**.

[0099] The control logic **512** can be coupled to every other portion in the peripheral circuit described above and configured to control the operations of every other portion in the peripheral circuit. The register **514** may be coupled to the control logic **512** and comprise a state register, a command register, and an address register for storing state information, a command operation code (OP code), and a command address for controlling the operation of each peripheral circuit. The interface **516** may be coupled to the control logic **512**, and act as a control buffer to buffer and relay control commands received from a host (not shown) to the control logic **512** and state information received from the control logic **512** to the host. The interface **516** may also be coupled to the column decoder/bit line driver **506** with data bus **518** and act as a data I/O interface and a data buffer to buffer and relay the data to and from the cell array **301**.

[0100] A basic principle of a three-dimensional NAND-type memory is a process in which carriers (electrons or holes) cross a charge barrier to inject a certain number of charges into a memory cell (cell) to complete a data write, and then storage data may be read according to a threshold voltage when the memory cell is turned on. Therefore, to read correct data, an ECC error correction algorithm with a strong error correction capability and high efficiency is usually introduced during a data read.

[0101] However, as the use time increases, charges stored in memory cells vary due to the increasing use time, repeated read operations, cross temperature, etc., thus affecting the correctness of reading data. When the threshold voltage deviates up or down obviously, when an original read voltage is used to read the data in the memory cell, a read error is highly probable. When a read error exceeds an ECC error correction capability, the data in the memory cell fails to be read.

[0102] FIG. **6** illustrates a schematic diagram of an example flow of a read operation of a memory system. In conjunction with what is shown in FIG. **6**, when the memory controller controls the memory device to perform a read operation, a default read operation (FW) is first performed on the memory cell at the corresponding physical address; if the default read operation fails, a read retry operation is performed; after the read retry operation fails, a soft decode operation is performed; after the soft decode fails, a Redundant Array of Independent Disk (RAID) operation is performed; and after the RAID operation fails, the read operation stops and the read fails because the error cannot be corrected, then the memory controller sends a read fail signal to the host **108**. Read retry operation and default read operation may be applicable to hard decode.

[0103] In some implementations, a read retry operation may usually be performed by looking up a retry table provided by a manufacturer. The essence of the read retry operation is an error correction mechanism. The retry table may provide a reference voltage used for reading data. A read voltage that deviates from a normal threshold voltage is tried by looking up the retry table to read memory cells again and perform error correction in combination with an ECC error correction algorithm, to try to correctly read data. If data with a read error is corrected, the lookup of the retry table is stopped. If data with a read error fails to be corrected, the lookup of the retry table is continued until the entire retry table is traversed.

[0104] In the foregoing manner of the read retry operation, because the retry table needs to be looked up entry by entry, this inevitably increases a number of trials and errors, consuming a relatively long time. In addition, the retry table provided by the manufacturer is only reference values in some specific environments. Actual use scenarios are high variable, and therefore many scenarios are not covered in the retry table provided by the manufacturer. As a result, data may fail to be corrected by traversing the retry table, and a long time is wasted to process commands. In summary, a manner of performing read retry operations by repeatedly polling a retry table consumes a long time, affects a response time of subsequent commands, and affects the performance of a device.

[0105] Based on one or more of the foregoing problems, in a first aspect, examples of the present application provide a memory device. As shown in FIG. **7**, the memory device comprises: an array of memory cells comprising multiple memory cells, wherein a preset number of memory cells form one codeword; and a peripheral circuit coupled with the array of memory cells and configured to perform the following operations: [0106] Operation S**10**: Obtain a first result corresponding to at least one codeword at a target read voltage, wherein the first result comprises the number of bits which represents the number of bits in the at least one codeword which are flipped in two read results at a first read voltage and a second read voltage, and a difference between the first read voltage and the second read voltage is less than a preset voltage. [0107] Operation S**20**: Obtain a first threshold according to the corresponding first result at the target read voltage, wherein the first threshold is to represent a corresponding first result at a maximum value in an effective range of predicted valley voltages. [0108] Operation S**30**: Make at least one adjustment to the target read voltage, and after each adjustment, obtain a corresponding first result at the adjusted target read voltage. [0109] Operation S**40**: Determine a target valley voltage according to a relationship between a corresponding first result at a target read voltage after one adjustment and the first threshold meeting a first preset condition or according to a corresponding first result at the target read voltage after multiple adjustments meeting a second preset condition, wherein the target valley voltage is taken as a read voltage at which a read operation is performed on the at least one codeword.

[0110] Here, for the structure of the memory device, refer to the foregoing FIG. **3**. Details are not described herein again.

[0111] In some examples, the memory device comprises an array of memory cells. The array of memory cells comprises multiple memory cells. A preset number of memory cells form one codeword (CW).

[0112] In some examples, a number of memory cells comprised in one codeword is the same as a number of memory cells comprised in encoding or decoding once during error correction encoding or decoding. In some examples, the number of memory cells comprised in one codeword may be less than or equal to a number of memory cells coupled with one physical page. For example, the number of memory cells comprised in one codeword is ¼ of the number of memory cells coupled with one physical page. In some examples, the codeword may comprises memory cells with a number ranging from 24 to 212. In an example, the codeword may comprise 24, 28 or 212 memory cells.

[0113] In general, codewords of different sizes may be selected for different memory systems, to meet performance, reliability, and storage requirements of the memory systems.

[0114] Memory cells (for example, an MLC, a TLC or a QLC) in different types of memory devices may store different numbers of bits.

[0115] It is to be noted that, in practice, a codeword has some extra reserved spaces for management and error correction. Therefore, a number of memory cells required in practice may slightly exceed the foregoing calculation result.

[0116] It may be understood that, a codeword may comprise multiple memory cells. A number of the memory cells comprised in the codeword may be adjusted according to an actual case.

[0117] In some examples, in a process of reading the memory device, data of one physical page is read out by one read operation. When the number of memory cells comprised in one codeword may be less than the number of memory cells coupled with one physical page, the codeword is an executable unit in obtaining the first result. However, in practice, multiple codewords are not excluded. That is, a first result corresponding to at least one codeword at a current read voltage may be obtained here. For example, one physical page may comprise 4 codewords. A page buffer hardware operation may calculate respective fail bit counts (FBCs) of the 4 codewords at once, and then the FBCs of the four codewords are added to obtain an FBC of one physical page. A value obtained from the addition is used in subsequent calculation. It may be understood that the first

result here may be data based on one physical page, and one physical page may comprise multiple codewords.

[0118] In some examples, the array of memory cells comprises memory cells with a number of memory bits being P bits. The P memory bits correspond to P pages respectively. The P-bit memory cell reads, through a Q-level read voltage, P-bit storage data of the memory cell. P and Q are both integers greater than 1, and Q=2P−1.

[0119] In an example, when the number of memory bits of the memory cell is 2, a corresponding memory state comprises a 0.sup.th state to a 4.sup.th state. With reference to FIG. **8**A, the 4 states are the 0.sup.th state (also referred to as an erased state) E, the 1.sup.st state (also referred to as a 1.sup.st memory state) P**1**, the 2.sup.nd state (also referred to as a 2.sup.nd memory state) P**2**, and the 3.sup.rd state (also referred to as a 3.sup.rd memory state) P**3** respectively. Binary data corresponding to the 4 states are 11, 10, 00, and 01 respectively. Correspondingly, the memory device comprises two pages, which are a lower page (LP) and an upper page (UP) respectively.

[0120] A memory cell shown in FIG. **8**A is taken as an example. A two-bit memory cell reads, through a 3-level read voltage (a first-level read voltage L**1**, a second-level read voltage L**2**, and a third-level read voltage L**3** shown in FIG. **8**A), two-bit four-state storage data of the two-bit memory cell.

[0121] In an example, one page corresponds to a multi-level read voltage, and the other page corresponds to a one-level read voltage. As shown in FIG. **8**A, binary data corresponding to the lower page is 1001, and a corresponding first-level read voltage L**1** and a corresponding third-level read voltage L**3** are required to read the lower page. Binary data corresponding to the upper page is 1100, and a corresponding second-level read voltage L**2** is required to read the upper page.

[0122] In an example, when the number of memory bits of the memory cell is 3, a corresponding memory state comprises a 0.sup.th state to a 7.sup.th state. With reference to FIG. **8**B, the 8 states are the 0.sup.th state (also referred to as an erased state) E, the 1.sup.st state (also referred to as a 1.sup.st memory state) P**1**, the 2.sup.nd state (also referred to as a 2.sup.nd memory state) P**2**, . . . , and the 7.sup.th state (also referred to as a 7.sup.th memory state) P**7** respectively. Binary data corresponding to the 8 states are 111, 110, 100, 000, 010, 011, 001, and 101 respectively. Correspondingly, the memory device comprises three pages, which are a lower page, a middle page (MP), and an upper page respectively.

[0123] A memory cell shown in FIG. **8**B is taken as an example. A three-bit memory cell reads, through a 7-level read voltage (a first-level read voltage L**1**, a second-level read voltage L**2**, a third-level read voltage L**3**, a fourth-level read voltage L**4**, a fifth-level read voltage L**5**, a sixth-level read voltage L**6**, and a seventh-level read voltage L**7** shown in FIG. **8**B), three-bit and eight-state storage data of the three-bit memory cell.

[0124] In an example, each page corresponds to a multi-level read voltage. As shown in FIG. **8**B, binary data corresponding to the lower page is 10000111, and a corresponding first-level read voltage L**1** and a corresponding fifth-level read voltage L**5** are required to read the lower page. Binary data corresponding to the middle page is 11001100, and a corresponding second-level read voltage L**2**, a corresponding fourth-level read voltage L**4**, and a corresponding sixth-level read voltage L**6** are required to read the middle page. Binary data corresponding to the upper page is 11100001, and a corresponding third-level read voltage L**3** and a corresponding to seventh-level read voltage L**7** are required to read the upper page.

[0125] In an example, when the number of memory bits of the memory cell is 4, a corresponding memory state comprises a 0.sup.th state to a 15.sup.th state. With reference to FIG. **8**C, the 16 states are the 0.sup.th state (also referred to as an erased state) E, the 1.sup.st state (also referred to as a 1.sup.st memory state) P**1**, the 2.sup.nd state (also referred to as a 2.sup.nd memory state) P**2**, . . . , and the 15.sup.th state (also referred to as a 15.sup.th memory state) P**15** respectively. Binary data corresponding to the 16 states are 1111, 0111, 0110, . . . , and 1110 respectively. Correspondingly, the memory device comprises four pages, which are a lower page, a middle page,

an upper page, and an extra page (XP) respectively. Here, the four memory bits corresponding to the 16 states are stored in the lower page, the middle page, the upper page, and the extra page respectively.

[0126] A memory cell shown in FIG. **8**C is taken as an example. A four-bit memory cell reads, through a 15-level read voltage (a first-level read voltage L**1**, a second-level read voltage L**2**, a third-level read voltage L**3**, a fourth-level read voltage L**4**, a fifth-level read voltage L**5**, a sixth-level read voltage L**6**, a seventh-level read voltage L**7**, an eighth-level read voltage L**8**, a ninth-level read voltage L**9**, a tenth-level read voltage L**10**, an eleventh-level read voltage L**11**, a twelfth-level read voltage L**12**, a thirteenth-level read voltage L**13**, a fourteenth-level read voltage L**14**, and a fifteenth-level read voltage L**15** shown in FIG. **8**C), four-bit sixteen-state storage data of the four-bit memory cell.

[0127] In an example, each page corresponds to a multi-level read voltage. As shown in FIG. **8**C, binary data corresponding to the lower page is 1100000011111100, and a corresponding second-level read voltage L**2**, a corresponding eighth-level read voltage L**8**, and a corresponding fourteenth-level read voltage L**14** are required to read the lower page. Binary data corresponding to the middle page is 1110000110000111, and a corresponding third-level read voltage L**3**, a corresponding seventh-level read voltage L**7**, a corresponding ninth-level read voltage L**9**, and a corresponding thirteenth-level read voltage L**13** are required to read the middle page. Binary data corresponding to the upper page is 1111100000110001, and a corresponding fifth-level read voltage L**5**, a corresponding tenth-level read voltage L**10**, a corresponding twelfth-level read voltage L**12**, and a corresponding fifteenth-level read voltage L**15** are required to read the upper page. Binary data corresponding to the extra page is 1000110000011111, and a corresponding first-level read voltage L**1**, a corresponding fourth-level read voltage L**4**, a corresponding sixth-level read voltage L**6**, and a corresponding eleventh-level read voltage L**11** are required to read the extra page.

[0128] The lower page is usually closest to a source/drain. Therefore, each level of read voltage of the corresponding levels of read voltage of the lower page is preferentially determined, an access speed is the highest, and a response time is the shortest, so that a balance between performance and durability in a data access process can be ensured.

[0129] It is to be noted that, the manner of preferentially determining each level of read voltage of the corresponding levels of read voltage of the lower page is only an example, and is not used to limit a sequence of determining each level of read voltage in multi-level read voltages corresponding to at least part of pages in examples of the present application.

[0130] It is to be noted that, the difference between the first read voltage and the second read voltage may be less than the preset voltage. In some examples, the second read voltage is greater than the first read voltage, and a range of the difference between the first read voltage and the second read voltage is set to 5 mV to 20 mV. In an example, the difference may be 5 mV, 10 mV, 15 mV, or 20 mV. In some other examples, the second read voltage is less than the first read voltage, and a range of the difference between the first read voltage and the second read voltage is set to −5 mV to −20 mV. In an example, the difference may be −5 mV, −10 mV, −15 mV, or −20 mV.

[0131] It is to be noted that, the first read voltage and the second read voltage here are sequentially related. That is, the second read voltage is obtained by making a third adjustment according to the first read voltage. Based on this, a voltage difference between the first read voltage and the second read voltage is a step size of the third adjustment. The difference between the first read voltage and the second read voltage being less than the preset voltage may be understood as that the first read voltage and the second read voltage have a small voltage difference. The preset voltage is related to the step size of the third adjustment, and may be a voltage slightly larger than the step size of the third adjustment. In some examples, a range of the preset voltage is set to 6 mV to 21 mV. In an example, the preset voltage may be 6 mV, 11 mV, 16 mV, or 21 mV. In some other examples, a range of the preset voltage is set to −6 mV to −21 mV. In an example, the preset voltage may be −6

mV, −11 mV, −16 mV, or −21 mV.

[0132] It is to be noted that, the first read voltage and the second read voltage are both general concepts. The target read voltage and read voltages obtained by making a first adjustment and a second adjustment to the target read voltage may all referred to as the first read voltage, and a read voltage obtained by making the third adjustment to the first read voltage may be referred to as the second read voltage. That is, the first read voltage is a general concept, and may be understood as the target read voltage or a target adjustment read voltage (a voltage obtained by making an adjustment to the target read voltage with a target step size, a range of the target step size may be set to 20 mV to 40 mV, and in an example, a step size of the second adjustment may be 20 mV, 30 mV, or 40 mV; and the range of the target step size may further be set to 50 mV to 150 mV. In an example, a step size of the first adjustment may be 50 mV, 60 mV, 70 mV, 80 mV, 100 mV, 120 mV, or 150 mV).

[0133] In examples of the present application, a corresponding first result at a voltage may be understood as follows: The third adjustment is made to a voltage, that is, a first voltage difference $\Delta V1$ exists between a voltage and a voltage after the third adjustment. A number of bits in the preset number of memory cells that are flipped in two read results at a voltage and a voltage after the third adjustment may be taken as a corresponding first result at a voltage. The preset number of memory cells may form at least one codeword.

[0134] In an example, the corresponding first result at the first read voltage may be understood as follows: The third adjustment is made to the first read voltage, that is, the first voltage difference $\Delta V1$ exists between the first read voltage and the second read voltage. A number of bits in a preset number of memory cells that are flipped in two read results at the first read voltage and at the second read voltage may be taken as the corresponding first result at the first read voltage. The first read voltage may be a target read voltage in a first stage (V0 shown in FIG. 9D), and the second read voltage may be a read voltage (V1 shown in FIG. 9D) obtained by making the third adjustment to the first read voltage, or, the first read voltage may be a adjusted target read voltage in a first stage (V2 shown in FIG. 9D), and the second read voltage may be a read voltage (V3 shown in FIG. 9D) obtained by making the third adjustment to the adjusted target read voltage.

[0135] In examples of the present application, the obtaining of the target valley voltage may be understood as follows: according to a corresponding first result at a voltage meeting a preset condition, the voltage is determined as the target valley voltage. For example, according to a corresponding first result at a read voltage in a first stage being less than or equal to a second preset value, the read voltage in a first stage is determined as a target valley voltage in a first stage. A range of the second preset value is set to 5 to 30, and in an example, the second preset value may be 5, 10, 15, 20, 25, or 30.

[0136] In examples of the present application, the obtaining of the predicted valley voltage may be understood as follows: The predicted valley voltage is obtained according to a voltage and the first mapping function. For example, according to a predicted valley voltage in a first stage/the target valley voltage in a first stage and the first mapping function, a predicted valley voltage in a second stage is obtained. The first mapping function is to represent a relationship between the predicted valley voltage in a first stage/the target valley voltage in a first stage and the predicted valley voltage in a second stage. The obtaining of the predicted valley voltage may further be understood as follows: according to a corresponding first result at a voltage, the stage number at which the voltage is, and a second mapping function, the predicted valley voltage is obtained. For example, according to a corresponding first result at the target read voltage in a first stage, the stage number at which the first stage is, and the second mapping function, the predicted valley voltage in a first stage is obtained. The second mapping function is to represent a relationship between the corresponding first result at the target read voltage, the stage number at which each stage is and the predicted valley voltage.

[0137] In examples of the present application, the obtaining of the adjusted voltage (for example,

the adjusted read voltage/the adjusted target read voltage) may be understood as a voltage obtained by making an adjustment to a voltage according to the target step size. For example, multiple first adjustments are made to the target read voltage with a first step size, and target read voltages after the multiple first adjustments are obtained respectively, or, multiple the second adjustments are made to the target read voltage with a second step size, and target read voltages after the multiple the second adjustments are obtained respectively.

[0138] In some examples, before a first result corresponding to at least one codeword at the target read voltage in a first stage is obtained, a read mode of the memory device is set to a single-level read (SLR) mode. The single-level read mode comprises reading, through a one-level read voltage, at least one bit of storage data stored in a memory cell. In some examples, the memory device is configured to: enter the single-level read mode in response to a mode setting command, and to obtain the first result corresponding to at least one codeword at the target read voltage in a first stage in the single-level read mode.

[0139] In some examples, the peripheral circuit is configured to: obtain a first result corresponding to at least one codeword at a target read voltage; obtain a first threshold according to the corresponding first result at the target read voltage; make at least one adjustment to the target read voltage, and after each adjustment, obtain a corresponding first result at the adjusted target read voltage; and determine the target valley voltage according to the relationship between the corresponding first result at the target read voltage after one adjustment and the first threshold meeting the first preset condition.

[0140] It is to be noted that, the predicted valley voltage here may be directly used as the target valley voltage as required to perform a read operation on data to be read, or perform further processing to obtain the target valley voltage. A manner of obtaining the predicted valley voltage is further described below.

[0141] Here and below, an example in which the array of memory cells comprises memory cells with a number of memory bits being 3 is taken for detailed description. However, this is not used to limit examples of the present application. In an example, as shown in FIG. **9**A, FIG. **9**B, FIG. **9**C, FIG. **9**D, FIG. **9**E, and FIG. **9**F, a number of memory bits of a memory cell of at least one codeword is 3, which correspond to a lower page, a middle page, and an upper page respectively. Each page corresponds to multiple stages. Multiple stages of the lower page comprise a first level and a fifth level, and a first-level read voltage L**1** is less than a fifth-level read voltage L**5**. Multiple stages of the middle page comprise a second level, a fourth level, and a sixth level, and a second-level read voltage L**2** and a fourth-level read voltage L**4** are both less than a sixth-level read voltage L**6**. Multiple stages of the upper page comprise a third level and a seventh level, and a third-level read voltage L**3** is less than a seventh-level read voltage L**7**. Here, the fifth-level read voltage L**5**, the sixth-level read voltage L**6**, and the seventh-level read voltage L**7** correspond to read voltages in a first stages of the lower page, the middle page, and the upper page respectively. The first-level read voltage L**1**, the second-level read voltage L**2** and the fourth-level read voltage L**4**, and the third-level read voltage L**3** correspond to read voltages in a second stage of the lower page, the middle page, and the upper page respectively.

[0142] In some examples, the peripheral circuit is configured to: obtain the first threshold according to the corresponding first result at the target read voltage and a first mapping function, wherein the first mapping function is to represent a relationship between the corresponding first result at the maximum value in the effective range of predicted valley voltages and the corresponding first result at the target read voltage.

[0143] In some examples, the target read voltage may be an empirical value (for example, a corresponding read voltage at which data is successfully read); or may be a default value configured when the memory device is delivered from a factory, wherein the default value is obtained through a large number of simulated experiments before the memory device is delivered from a factory. A default valley voltage may be a default value configured when the memory device

is delivered from a factory, wherein the default value is obtained through a large number of simulated experiments before the memory device is delivered from a factory.

[0144] In the present application, the term "the corresponding first result at the target read voltage", may be briefly referred to as "a first result for the first time", the term "the corresponding first result at the predicted valley voltage" may be briefly referred to as a "predicted first result", and the term "the corresponding first result at the default valley voltage" may be briefly referred to as "a default first result".

[0145] In some examples, the first threshold is positively correlated to a deviation degree. The deviation degree is an absolute value of a difference between the first result for the first time and the default first result.

[0146] In an example, the larger the absolute value of the difference between the first result for the first time and the default first result is, the larger the first threshold is. A difference between a first result for the first time Y**1** and a default first result Y**3** shown in FIG. **10**B is less than a difference between a first result for the first time Y**1** and a default first result Y**3** shown in FIG. **10**C, and it may be obtained that a first threshold shown in FIG. **10**B is less than a first threshold shown in FIG. **10**C.

[0147] In some examples, the first mapping function is to represent and comprising a relationship between the predicted first result and the first result for the first time. The predicted first result is correlated to at least one of the level number at which the target read voltage is or a use scenario of the memory device.

[0148] In an example, in a data retaining scenario, as shown in FIG. **10**B, when a corresponding first result Y**1** (for example, 500) at a fifth-level target read voltage exceeds a threshold (for example, 400), it may be considered, according to a characteristic of the memory device, that a threshold voltage VT of a memory cell of the memory device is in a strong left deviation state. According to the corresponding first result Y**1** at the fifth-level target read voltage, an adjustment may be made based on the second mapping function to obtain a fifth-level predicted valley voltage. A corresponding first result Y**2** at the fifth-level predicted valley voltage is greater than a corresponding first result Y**3** at the fifth-level default valley voltage.

[0149] In an example, in a read operation interference scenario, as shown in FIG. **10**A, when a corresponding first result Y**1** (for example, 400) at a fifth-level target read voltage exceeds a threshold (for example, 300), it may be considered, according to a characteristic of the memory device, that a threshold voltage VT of a memory cell of the memory device is in a strong left deviation state. According to the corresponding first result Y**1** at the fifth-level target read voltage, an adjustment may be made based on the second mapping function to obtain a fifth-level predicted valley voltage. A corresponding first result Y**2** at the fifth-level predicted valley voltage is greater than a corresponding first result Y**3** at the fifth-level default valley voltage.

[0150] In some examples, the peripheral circuit is configured to: obtain the corresponding first result at the maximum value in the effective range of predicted valley voltages according to an initial value of the corresponding first result at the maximum value in the effective range of predicted valley voltages, a correction value for the corresponding first result at the target read voltage, and a correction coefficient, wherein the initial value of the corresponding first result at the maximum value in the effective range of predicted valley voltages and the correction coefficient are both fixed values related to a stage in which a read voltage is, and the larger the corresponding first result at the target read voltage is, the larger the correction value is.

[0151] In some examples, according to an initial value init_val and a correction value rFBC for the first threshold and a correction coefficient rFactor, the corresponding first result at the maximum value in the effective range of predicted valley voltages is obtained, that is, a first threshold vly_fbc_th obtained for the first time. In an example, the first threshold vly_fbc_th obtained for the first time is: vly_fbc_th[level]=init_val[level]+rFBC/rFactor, and a first threshold vly_fbc_th obtained for the Nth time is: a sum of a first threshold obtained for the (N−1)th time and

(rFBC/rFactor). A formula of the first threshold vly_fbc_th may be represented as: vly_fbc_th[level]=vly_fbc_th[level]+rFBC/rFactor. For details, refer to Formula (1) in Table 1.

[0152] In some examples, according to a first result for the first time fFBC and a reference coefficient ref_fbc**3**, the correction value rFBC is obtained. In an example, a formula of the correction value rFBC is: rFBC=fFBC−fFBC/ref_fbc**3**[level]. For details, refer to Formula (2) in Table 1.

[0153] In an example, a segmentation parameter div_para is 8. In an example the first result for the first time fFBC is 500. In an example, the reference coefficient ref_fbc**3** is {DMY, 1, 1, 1, 6, 5, 5, 4}. According to Formula (2), in an example, it may be obtained that the correction value rFBC is {DMY, 0, 0, 0, 416, 400, 400, 375}.

[0154] In an example, the initial value init_val of the first threshold is {DMY, 90, 90, 90, 90, 95, 90, 90}. In an example, the correction value rFBC is {DMY, 0, 0, 0, 416, 400, 400, 375}. In an example, the correction coefficient rFactor is {DMY, 80, 80, 80, 80, 40, 80, 40}. According to Formula (1), in an example, it may be obtained that the first threshold vly_fbc_th is vly_fbc_th[level]+rFBC/rFactor={DMY, 90, 90, 90, 95, 105, 95, 99}.

[0155] Table 1 below lists the first result for the first time fFBC, the first threshold vly_fbc_th, the correction value rFBC, the reference coefficient ref_fbc**3**, the correction coefficient rFactor, the segmentation parameter div_para, and corresponding descriptions and examples. A value of the segmentation parameter div_para may be understood as that a corresponding memory cell has multiple memory states (one erased state and multiple programmed states). For example, the value of the segmentation parameter div_para being 8 may be understood as that a corresponding memory cell of a TLC type has 8 memory states (one erased state and seven programmed states). The initial value init_val of the first threshold is {DMY, 90, 90, 90, 90, 95, 90, 90}. "DMY", "90", "90", "90", "90", "95", "90", and "90" correspond to the initial values init_val of the first threshold in an erased state, a first programmed state, a second programmed state, a third programmed state, a fourth programmed state, a fifth programmed state, a sixth programmed state, and a seventh programmed state respectively.

TABLE-US-00001 TABLE 1 Parameter code Parameter name, parameter description, and parameter example fFBC The corresponding first result at the target read voltage (referred to as the first result for the first time for short). In an example, the first result for the first time is: 500 vly_fbc_th The first threshold is obtained according to the corresponding first result at the target read voltage. In an example, the first threshold is: vly_fbc_th[level] = vly_fbc_th[level] + rFBC/rFactor (1) In an example, the initial value (init_val) of the first threshold is: {DMY, 90, 90, 90, 90, 95, 90, 90}; rFBC The correction value is a value used for correcting the corresponding first result at the target read voltage. If the corresponding first result at the target read voltage is greater than a threshold (for example, 400), the correction value needs to be adjusted. In an example, the correction value is: rFBC = fFBC − fFBC/ref_fbc3[level] (2) ref_fbc3 Reference coefficient. Refer to the corresponding first result at the target read voltage level by level to calculate the correction value. In an example, the reference coefficient is: {DMY, 1, 1, 1, 6, 5, 5, 4} rFactor Correction coefficient. In an example, the correction coefficient is: {DMY, 80, 80, 80, 80, 40, 80, 40} div_para Segmentation parameter. In an example, the segmentation parameter is: 8

[0156] In some examples, the first preset condition is that a corresponding first result at the target read voltage after one adjustment is less than the first threshold; and the peripheral circuit is configured to: determine the target read voltage after one adjustment as the target valley voltage according to the relationship between the corresponding first result at the target read voltage after one adjustment and the first threshold meeting the first preset condition.

[0157] In an example, as shown in FIG. **10**C, the peripheral circuit is configured to: obtain a corresponding first result Y**1** of a lower page of at least one codeword at a fifth-level target read voltage (V**0** shown in FIG. **10**C); obtain the first threshold according to the corresponding first result Y**1** at the fifth-level target read voltage; make at least one adjustment to the target read

voltage, and after each adjustment, obtain a corresponding first result at the adjusted target read voltage; and determine, according to a corresponding first result Y2 at the target read voltage after one adjustment being less than or equal to the first threshold, that the target read voltage after one adjustment is a fifth-level read voltage L5, wherein the fifth-level read voltage L5 is taken as a read voltage at which a read operation is performed on the at least one codeword.

[0158] The first-level read voltage L1 is determined in a manner similar to that of determining the fifth-level read voltage L5. The fifth-level read voltage L5 and the first-level read voltage L1 may be used for reading data of a lower page of the at least one codeword. In a manner similar to that of determining the fifth-level read voltage L5, the sixth-level read voltage L6, the fourth-level read voltage L4, and the second-level read voltage L2 are determined for reading data of a middle page of the at least one codeword, and the seventh-level read voltage L7 and the third-level read voltage L3 are determined for reading data of an upper page of the at least one codeword.

[0159] In some examples, the peripheral circuit is configured to: according to the corresponding first result at the target read voltage being greater than or equal to the first threshold, obtain, with the corresponding first result at the target read voltage, a target adjustment value for adjusting the target read voltage; obtain a corresponding first result at the adjusted target read voltage with the target adjustment value; according to the corresponding first result at the adjusted target read voltage with the target adjustment value being less than the first threshold, determine the adjusted target read voltage with the target adjustment value as the target valley voltage; and according to the corresponding first result at the adjusted target read voltage with the target adjustment value being greater than or equal to the first threshold, make multiple adjustments to the target read voltage, and after each adjustment, obtain the corresponding first result at the adjusted target read voltage, until the corresponding first result at the adjusted target read voltage is less than the first threshold or the corresponding first result at the target read voltage after multiple adjustments meet the second preset condition.

[0160] Here and below, the target adjustment value/the first step size value/the second step size value is positive (for example, 50 mV), representing adjusting the target read voltage in a first direction (rightward direction), for example, increasing the target read voltage by a voltage value of 50 mV. The target adjustment value/the first step size value/the second step size value here is negative (for example, −50 mV), representing adjusting the target read voltage in a second direction (leftward direction), for example, subtracting a voltage value of 50 mV from the target read voltage.

[0161] In some examples, as shown in FIG. 10D, the peripheral circuit is configured to: according to the corresponding first result Y1 at the fifth-level target read voltage (V0 shown in FIG. 10D) being greater than or equal to the first threshold, make one adjustment to the fifth-level target read voltage with the target adjustment value, obtain the corresponding first result Y2 at the adjusted target read voltage (V2 shown in FIG. 10D), and according to the corresponding first result at the adjusted target read voltage Y2 with the target adjustment value being less than the first threshold, determine the adjusted target read voltage with the target adjustment value as a fifth-level target valley voltage (L5 shown in FIG. 10D).

[0162] In some examples, an absolute value of the target adjustment value is positively correlated to the corresponding first result at the target read voltage. the larger the corresponding first result at the target read voltage is, the larger the target adjustment value is. In an example, when the corresponding first result at the fifth-level target read voltage is 500, the target adjustment value may be 200 mV; when the corresponding first result at the fifth-level target read voltage is 300, the target adjustment value may be 120 mV; and when the corresponding first result at the fifth-level target read voltage is 100, the target adjustment value may be 50 mV.

[0163] In some examples, as shown in FIG. 10D, the peripheral circuit is configured to: according to the corresponding first result Y1 at the fifth-level target read voltage being greater than or equal to the first threshold, make multiple adjustments to the fifth-level target read voltage, and after each

adjustment, obtain the corresponding first result at the adjusted target read voltage, until the corresponding first result at the adjusted target read voltage is less than the first threshold or the corresponding first result at the target read voltage after multiple adjustments meet the second preset condition.

[0164] In some examples, multiple adjustments comprise the first adjustment made with the first step size value and the second adjustment made with the second step size value. The first step size value is greater than the second step size value. The obtaining the adjusted target read voltage with the target adjustment value comprises: making at least one first adjustment with the first step size value to obtain the adjusted target read voltage, and subsequently, making at least one second adjustment with the second step size value to obtain the adjusted target read voltage. In an example, a range of the first step size value is set to 50 mV to 150 mV, and the first step size value may be 50 mV, 60 mV, 70 mV, 80 mV, 100 mV, 120 mV or 150 mV, or, a range of the first step size value is set to −50 mV to −150 mV, and the first step size value may be −50 mV, −60 mV, −70 mV, −80 mV, −100 mV, −120 mV or −150 mV. A range of the second step size value is set to 20 mV to 50 mV, and the second step size value may be 20 mV, 30 mV, 40 mV or 50 mV, or, a range of the second step size value range is set to −20 mV to −50 mV, and the second step size value may be −20 mV, −30 mV, −40 mV or −50 mV.

[0165] In some examples, the second preset condition is that taken the minimum first result among multiple corresponding first results at the target read voltages after multiple adjustments as a reference value, the number of first results from remaining first results which differ from the reference value with a difference being less than a second threshold is greater than a preset number; and the peripheral circuit is configured to: according to the corresponding first result at the target read voltage after multiple adjustments meeting the second preset condition, take a target read voltage corresponding to the minimum first result among the multiple first results as the target valley voltage.

[0166] In an example, as shown in FIG. **10**E, the of 5 first results Y**4**, Y**5**, Y**6**, Y**7**, and Y**8** which differ from the reference value Yr with a difference being less than the second threshold is greater than the preset number (for example, 3), the corresponding first result at the target read voltage after multiple adjustments meet the second preset condition, and a target read voltage (V**2** shown in FIG. **10**E) corresponding to the minimum first result (the reference value Yr) among the multiple first results (comprising the reference value Yr and the 5 first results Y**4**, Y**5**, Y**6**, Y**7**, and Y**8**) is taken as a seventh-level read voltage L**7**.

[0167] In some examples, the second threshold ranges from 2 to 25, and may be 5, 10, 15 or 20. In some examples, the preset number ranges from 1 to 5, and may be 1, 3 or 5.

[0168] In some examples, the peripheral circuit is configured to: in a process of making multiple adjustments to the target read voltage, make adjustments by employing different adjustment methods, and according to the adjusted target read voltages corresponding to more than a preset number of adjustment methods in the different adjustment methods being same and the corresponding first result at the same target read voltage being the minimum value among all first results, take the same target read voltage as the target valley voltage.

[0169] In some examples, as shown in FIG. **10**F, different adjustment methods comprise at least two following methods: making one adjustment to a seventh-level target read voltage with the target adjustment value (DL**1** shown in FIG. **10**F), making at least one first adjustment to a seventh-level target read voltage with the first step size value (DL**2** shown in FIG. **10**F), and making at least one second adjustment to a seventh-level target read voltage with the second step size value (DL**3** shown in FIG. **10**F).

[0170] In an example, as shown in FIG. **10**F, one adjustment is made to the seventh-level target read voltage with the target adjustment value (DL**1** shown in FIG. **10**F), at least one first adjustment is made to the seventh-level target read voltage with the first step size value (DL**2** shown in FIG. **10**F), and at least one second adjustment is made to the seventh-level target read

voltage with the second step size value (DL**3** shown in FIG. **10**F), and the corresponding first results at the target read voltages obtained after the adjustments are all directed to one same first result Ys. The corresponding adjusted target read voltage (V**2** shown in FIG. **10**F) is the seventh-level read voltage L**7**.

[0171] In some examples, the peripheral circuit is configured to: make multiple first adjustments to the target read voltage with a first step size, and obtain corresponding first results at target read voltages after the multiple first adjustments respectively; determine a value of knee point according to the obtained corresponding first results at the read voltages after the multiple first adjustments, wherein a target read voltage corresponding to the value of knee point is a knee-point voltage; make multiple second adjustments to the knee-point voltage with a second step size, and obtain the corresponding first results at the target read voltages after the multiple second adjustments respectively, wherein the second step size is less than the first step size; and determine the target valley voltage with the obtained corresponding first results at the target read voltages after the multiple second adjustments.

[0172] In some examples, as shown in FIG. **10**G, an example in which the seventh-level target read voltage is taken as the target read voltage is used, and the peripheral circuit is configured to obtain a knee-point voltage V**4** through the following operations: [0173] after obtaining a corresponding first result Y**1** at the target read voltage, taking the target read voltage as a reference, making a first adjustment to the target read voltage with the first step size value (positive value) to obtain a first result Y**1-2**, and making a second first adjustment to the target read voltage with the first step size value (negative value) to obtain a first result Y**1-3**; [0174] according to the first result Y**1-2** being greater than the first result Y**1** and the first result Y**1-3** being less than the first result Y**1**, determining to make multiple adjustments to the target read voltage with the first step size value (negative value), to obtain first results (for example, first results Y**1-4**, Y**1-5**, Y**1-6**, and Y**1-7**, or first results Y**1-4** to Y**1-9**, or first results Y**1-4** to Y**1-10**) after multiple adjustments; [0175] according to at least one for upward trend, determining to stop making the first adjustment to the target read voltage, wherein one for upward trend may be understood as that a case that a first result Y**1**-(N+1) obtained by making an Nth first adjustment to the target read voltage with the first step size value (negative value) is less than a first result Y**1**-(N+2) obtained by making an (N+1)th first adjustment to the target read voltage with the first step size value (negative value) is determined as one for upward trend; for example, that the first result Y**7** is greater than the first result Y**1-6**, that the first result Y**1-8** is greater than the first result Y**1-7**, that the first result Y**1-9** is greater than the first result Y**1-8**, or, that the first result Y**1-10** is greater than the first result Y**1-9** may be determined as one for upward trend; and [0176] determining the minimum value among the obtained corresponding first results at the read voltages after the multiple first adjustments as a value of knee point, wherein a target read voltage corresponding to the value of knee point is a knee-point voltage, wherein for example, the minimum value among the multiple first results is the first result Y**1-6**, the first result Y**1-6** is taken as a value of knee point Yt, and a target read voltage corresponding to the value of knee point Yt is a knee-point voltage V**1-4**.

[0177] In some examples, the corresponding first results at the target read voltages after the multiple first adjustments comprise a first adjacent value and a second adjacent value that are adjacent to the value of knee point, and the peripheral circuit is configured to: according to a difference between the first adjacent value and the value of knee point being less than a difference between the second adjacent value and the value of knee point, narrow a range for the multiple second adjustments to be between a target read voltage corresponding to the first adjacent value and the knee-point voltage; and take an average of the read voltage corresponding to the first adjacent value and the knee-point voltage, and according to a corresponding first result at the average being less than the first threshold, take the average as the target valley voltage; and according to the corresponding first result at the average being greater than or equal to the first threshold, continue to make a second adjustment between the read voltage corresponding to the

first adjacent value and the knee-point voltage, until a corresponding first result at the adjusted target read voltage is less than the first threshold.

[0178] In some examples, as shown in FIG. **10**G, an example in which the seventh-level target read voltage is taken as the target read voltage is used, and the peripheral circuit is configured to: after obtaining the value of knee point Yt and the knee-point voltage V**4**, take the knee-point voltage V**4** as a reference, make at least one second adjustment with the second step size value to obtain the adjusted target read voltage. For a detailed process of making at least one second adjustment with the second step size value, refer to a detailed process of making at least one first adjustment with the first step size value in the foregoing example for understanding, wherein the first step size value is greater than the second step size value, or, refer to the adjustment manner in any example shown in FIG. **10**B to **10**F. Details are not described herein again.

[0179] Here, the first step size value is greater than the second step size value. In an example, a range of the first step size value is set to 50 mV to 150 mV, and the first step size value may be 50 mV, 60 mV, 70 mV, 80 mV, 100 mV, 120 mV or 150 mV, or, a range of the first step size value is set to −50 mV to −150 mV, and the first step size value may be −50 mV, 60 mV, −70 mV, −80 mV, −100 mV, −120 mV or −150 mV. A range of the second step size value is set to 20 mV to 50 mV, and the second step size value may be 20 mV, 30 mV, 40 mV or 50 mV, or, a range of the second step size value range is set to −20 mV to −50 mV, and the second step size value may be −20 mV, −30 mV, −40 mV or −50 mV.

[0180] In some examples, as shown in FIG. **10**G, an example in which the seventh-level target read voltage is taken as the target read voltage is used, and the peripheral circuit is configured to: according to the difference between the first adjacent value (the first result Y**1**-**7**) and the value of knee point Yt (the first result Y**1**-**6**) being less than a difference between the second adjacent value the second adjacent value (the first result Y**1**-**5**) and the value of knee point Yt, narrow a range for the multiple second adjustments to be between a target read voltage V**3** corresponding to the first adjacent value (the first result Y**1**-**7**) and the knee-point voltage V**4**; and take an average of the read voltage V**3** corresponding to the first adjacent value and the knee-point voltage V**4**, and according to a corresponding first result Yv at the average being less than the first threshold, take the average as a target valley voltage V**2**, and determine the target valley voltage V**2** as the seventh-level read voltage L**7**.

[0181] In some examples, the peripheral circuit is configured to: obtain the predicted valley voltage according to the corresponding first result at the target read voltage and a second mapping function, wherein the second mapping is to represent a relationship between the corresponding first result at the target read voltage and the predicted valley voltage.

[0182] In some examples, the second mapping function is to represent and comprising a relationship between the predicted valley voltage and the first result for the first time. The predicted valley voltage is correlated to at least one of the level number at which the target read voltage is or a use scenario of the memory device.

[0183] In an example, in a data retaining scenario, as shown in FIG. **10**B, when a corresponding first result Y**1** (for example, 500) at a fifth-level target read voltage exceeds a threshold (for example, 400), it may be considered, according to a characteristic of the memory device, that a threshold voltage VT of a memory cell of the memory device is in a strong left deviation state. According to the corresponding first result Y**1** at the fifth-level target read voltage, an adjustment may be made based on the second mapping function to obtain a fifth-level predicted valley voltage. Compared with the fifth-level target read voltage, the fifth-level predicted valley voltage is in a strong left deviation state.

[0184] In an example, in a read operation interference scenario, as shown in FIG. **10**A, when a corresponding first result Y**1** (for example, 400) at a fifth-level target read voltage exceeds a threshold (for example, 300), it may be considered, according to a characteristic of the memory device, that a threshold voltage VT of a memory cell of the memory device is in a strong left

deviation state. According to the corresponding first result Y**1** at the fifth-level target read voltage, an adjustment may be made based on the second mapping function to obtain a fifth-level predicted valley voltage. Compared with the fifth-level target read voltage, the fifth-level predicted valley voltage is in a strong left deviation state.

[0185] In some examples, as shown in FIG. **10**D, the peripheral circuit is configured to: according to the corresponding first result Y**1** at the fifth-level target read voltage (V**0** shown in FIG. **10**D), obtain the predicted valley voltage, and obtain the corresponding first result Y**2** at the predicted valley voltage (V**2** shown in FIG. **10**D), and according to the corresponding first result Y**2** at the predicted valley voltage being less than the first threshold, determine the predicted valley voltage as the fifth-level target valley voltage (L**5** shown in FIG. **10**D).

[0186] In some examples, the memory cell comprises multiple memory bits, and the multiple memory bits correspond to multiple pages respectively; and at least part of pages correspond to multiple stages, the multiple stages comprise a first stage and a second stage, and a read voltage in the second stage is less than a read voltage in the first stage; and the peripheral circuit is configured to: obtain at least one of a predicted valley voltage in the second stage from the multiple stages or a target valley voltage in other first stage corresponding to a lower read voltage with the determined target valley voltage according to the stage number corresponding to the determined target valley voltage belonging to the first stage.

[0187] In some examples, at least part of pages correspond to read voltages in multiple stages. The read voltages in multiple stages comprise the read voltage in a first stage and the read voltage in a second stage. The read voltage in a second stage is less than the read voltage in a first stage. In an example, the read voltage in a first stage may be understood as the highest read voltage in the read voltages in multiple stages of each page, and the read voltage in a second stage may be understood as another read voltage less than the highest read voltage in the read voltages in multiple stages of each page.

[0188] It is to be noted that, the first stage and the second stage are used for distinguishing between a high-level read voltage and a low-level read voltage in read voltages in multiple stages corresponding to at least part of pages. The low-level read voltage is less than the high-level read voltage. For a memory cell comprising multiple memory bits, one page corresponding to one memory bit may comprise one stage or multiple stages. One stage may comprise one level or multiple levels.

[0189] In an example, with reference to FIG. **8**A, the memory device comprises a lower page and an upper page. The lower page corresponds to multiple stages. The multiple stages of the lower page comprise a first level and a third level. The first-level read voltage L**1** is less than the third-level read voltage L**3**. Here, the third-level read voltage L**3** corresponds to a read voltage in a first stage of the lower page (a high-level read voltage of the lower page), and the first-level read voltage L**1** corresponds to a read voltage in a second stage of the lower page (a low-level read voltage of the lower page).

[0190] In an example, with reference to FIG. **8**B, the memory device comprises a lower page, a middle page, and an upper page. Each page corresponds to multiple stages. Multiple stages of the lower page comprise a first level and a fifth level, and a first-level read voltage L**1** is less than a fifth-level read voltage L**5**. Multiple stages of the middle page comprise a second level, a fourth level, and a sixth level, and a second-level read voltage L**2** and a fourth-level read voltage L**4** are both less than a sixth-level read voltage L**6**. Multiple stages of the upper page comprise a third level and a seventh level, and a third-level read voltage L**3** is less than a seventh-level read voltage L**7**. Here, the fifth-level read voltage L**5**, the sixth-level read voltage L**6**, and the seventh-level read voltage L**7** correspond to read voltages in a first stages of the lower page, the middle page, and the upper page respectively. The first-level read voltage L**1**, the second-level read voltage L**2** and the fourth-level read voltage L**4**, and the third-level read voltage L**3** correspond to read voltages in a second stage of the lower page, the middle page, and the upper page respectively.

[0191] In an example, with reference to FIG. **8**C, the memory device comprise a lower page, a middle page, an upper page, and an extra page. Each page corresponds to multiple stages. Multiple stages of the lower page comprise a second level, an eighth level, and a fourteenth level, and a second-level read voltage L**2** and an eighth-level read voltage L**8** are both less than a fourteenth-level read voltage L**14**. Multiple stages of the middle page comprise a third level, a seventh level, a ninth level, and a thirteenth level, and a third-level read voltage L**3**, a seventh-level read voltage L**7**, and a ninth-level read voltage L**9** are all less than a thirteenth-level read voltage L**13**. Multiple stages of the upper page comprise a fifth level, a tenth level, a twelfth level and a fifteenth level, and a fifth-level read voltage L**5**, a tenth-level read voltage L**10**, and a twelfth-level read voltage L**12** are less than a fifteenth-level read voltage L**15**. Multiple stages of the extra page comprise a first level, a fourth level, a sixth level, and an eleventh level, and a first-level read voltage L**1**, a fourth-level read voltage L**4** and a sixth-level read voltage L**6** are less than the eleventh-level read voltage L**11**. Here, the fourteenth-level read voltage L**14**, the thirteenth-level read voltage L**13**, the fifteenth-level read voltage L**15**, and the eleventh-level read voltage L**11** correspond to read voltage in a first stages of the lower page, the middle page, the upper page, and the extra page respectively. The second-level read voltage L**2** and the eighth-level read voltage L**8** correspond to a read voltage in a second stage of the lower page. The third-level read voltage L**3**, the seventh-level read voltage L**7**, and the ninth-level read voltage L**9** correspond to a read voltage in a second stage of the middle page. The fifth-level read voltage L**5**, the tenth-level read voltage L**10**, and the twelfth-level read voltage L**12** correspond to a read voltage in a second stage of the upper page. The first-level read voltage L**1**, the fourth-level read voltage L**4**, and the sixth-level read voltage L**6** correspond to a read voltage in a second stage of the extra page.

[0192] In some implementations, when a first target stage is the seventh-level read voltage L**7**, predicted valley voltages in all remaining first stages and predicted valley voltage in a second stage may be obtained according to a predicted valley voltage of the seventh-level read voltage L**7**, that is, predicted valley voltages of the first-level read voltage L**1**, the second-level read voltage L**2**, the fourth-level read voltage L**4**, the fifth-level read voltage L**5**, and the sixth-level read voltage L**6** may be directly obtained according to the predicted valley voltage of the seventh-level read voltage L**7**.

[0193] In some examples, with reference to FIG. **8**B, the peripheral circuit is configured to: obtain the predicted valley voltage of the first target stage (the seventh-level read voltage L**7**); and obtain at least one of a predicted valley voltage (the fifth-level read voltage L**5**, the sixth-level read voltage L**6** or the first-level read voltage L**1**, the second-level read voltage L**2** and the fourth-level read voltage L**4**, and the third-level read voltage L**3**) of a second target stage according to the predicted valley voltage of the first target stage (the seventh-level read voltage L**7**).

[0194] In some examples, as shown in FIG. **8**B, the peripheral circuit is configured to: obtain the predicted valley voltage of the second target stage (the sixth-level read voltage L**6**) according to the predicted valley voltage of the first target stage (the seventh-level read voltage L**7**) and the second mapping function, wherein the second mapping function is to represent a relationship between the target valley voltage of the first target stage and the predicted valley voltage of the second target stage.

[0195] In another example, a predicted valley voltage of the sixth-level read voltage L**6** may be obtained according to the seventh-level read voltage L**7**, a target valley voltage of the sixth-level read voltage L**6** may be obtained according to the predicted valley voltage of the sixth-level read voltage L**6**, then a predicted valley voltage of the fifth-level read voltage L**5** may be obtained according to the target valley voltage of the sixth-level read voltage L**6**, and so on, to sequentially obtain target valley voltages of the fifth-level read voltage L**5**, the fourth-level read voltage L**4**, the third-level read voltage L**3**, the second-level read voltage L**2**, and the first-level read voltage L**1** respectively.

[0196] In some examples, the peripheral circuit is configured to: read storage data of the at least

one codeword at the first read voltage, to obtain a second result; read storage data of the at least one codeword at the second read voltage, to obtain a third result; perform a logical operation on the second result and the third result, to obtain a fourth result; and count the number of bits in the fourth result which represent flip of bits in the third result relative to the second result, to obtain the first result.

[0197] In an example, as shown in FIG. **9**D, data stored in a lower page of a memory cell in at least one codeword is read at the first read voltage (V**0** shown in FIG. **9**D). A memory cell with a threshold voltage less than the first read voltage is labeled as a bit **1**, and a memory cell with a threshold voltage greater than the first read voltage is labeled as a bit **0**, to obtain the second result.

[0198] In an example, as shown in FIG. **9**D, data stored in a lower page of a memory cell in at least one codeword is read at the second read voltage (V**1** shown in FIG. **9**D). A memory cell with a threshold voltage less than the second read voltage is labeled as a bit **1**, and a memory cell with a threshold voltage greater than the second read voltage is labeled as a bit **0**, to obtain the third result.

[0199] For example, an XOR operation is performed on the second result and the third result, to obtain the fourth result. It is to be noted that, the XOR operation is one of the basic logical operations. In the binary system, when two binary numbers at a same position are same, a result is "0", and when two binary numbers at a same position are different, a result is "1" (that is, 0 when binary numbers are same, and 1 when binary numbers are different).

[0200] In an example, a bit being 1 in the fourth result represents that different data are read from a memory cell in the at least one codeword at the first read voltage and at the second read voltage, and a bit being 0 in the fourth result represents that same data are read from a memory cell in the at least one codeword at the first read voltage and at the second read voltage. For example, a number of bits being 1 in the fourth result represents a number of bits in the at least one codeword that are flipped in two read results at the first read voltage and the second read voltage, and a number of bits being 0 in the fourth result represents a number of bits in the at least one codeword that are same in two read results at the first read voltage and the second read voltage. Because the single-level read mode is used, that is, the foregoing two read operations both read one bit of data stored in a lower page of a memory cell in at least one codeword, a number of bits being 1 in the fourth result represents a number of memory cells that have flipped in two read results of the at least one codeword at the first read voltage and the second read voltage, and the number of bits is denoted as a first result corresponding to the first read voltage, for example, a corresponding first result Y**1** of the at least one codeword at the target read voltage in a first stage (V**0** shown in FIG. **9**D), a corresponding first result Y**2** of the at least one codeword at the adjusted target read voltage in a first stage (V**2** shown in FIG. **9**D), and a first result Y**3** corresponding to the at least one codeword at an adjusted target read voltage in a first stage (V**22** shown in FIG. **9**D).

[0201] In some examples, the peripheral circuit comprises: a first latch, a second latch, and a third latch; the first latch is configured to store the second result; the second latch is configured to store the third result; and the third latch is configured to store the fourth result.

[0202] In an example, storage data (that is, the second result) of the at least one codeword read at the first read voltage is stored in the first latch, storage data (that is, the third result) of the at least one codeword read at the second read voltage is stored in the second latch, and data (that is, the fourth result) obtained by performing the XOR operation on the second result and the third result is stored in the third latch.

[0203] In the first aspect, in the memory devices provided in the examples of the present application, a first result (a size of the first result may be several bytes) rather than at least one codeword (for example, a size of the codeword may be 4 KB) is transmitted, so that an amount of transmitted data is reduced. A first threshold is obtained according to a corresponding first result at a target read voltage. With the dynamic first threshold, the iterative rapidity of convergence of determining a target valley voltage is higher. A process of obtaining the first result converges inside the memory device, does not occupy, for example, a space of the memory controller, and has low

dependency on, for example, the memory controller. A process of obtaining a predicted valley voltage/the target valley voltage according to the first result is completed in the memory device, so that a transmission time of an output port is reduced. The memory devices are applicable to a memory device of an MLC, a TLC type or a QLC type.

[0204] In a second aspect, examples of the present application provide a memory system. As shown in FIG. **11** and FIG. **12**, the memory system **102** comprises: one or more of the memory devices **104** provided in the first aspect; and a memory controller **106** coupled with the memory device **104** and controlling the memory device **104**.

[0205] As shown in FIG. **11**, in some examples, a memory system **102** is coupled to a host, and performs various feedbacks in response to instructions of the host. The memory system **102** may comprise a memory controller **106** and a memory device **104**. The memory controller **106** is configured to control the memory device **104** to perform operations such as read, write, erase, etc. The memory controller **106** may also be coupled the memory device **104** in any appropriate manner.

[0206] The memory controller **106** may comprise a host interface (I/F) **1061**, a memory interface (I/F) **1062**, a control component **1063**, a read-only memory (ROM) **1069**, a random access memory (RAM) **1070**, an error correction module **1064**, a garbage collection module **1065**, a wear leveling module **1066**, a data buffer **1067**, and a bus **1060**. The host interface **1061** is a connection interface for a connection between a host **108** and the memory controller **106**. The host interface **1061** allows the host and the memory controller to perform communication according to a specific protocol, send a read request and a write request, and perform other operations. The memory interface **1062** is a connection interface between the memory controller **106** and the memory device **104**. The memory interface **1062** is configured to achieve data transmission between the memory controller **106** and the memory device **104**. The control component **1063** is configured to generally control the memory system **106**. The foregoing specific operations performed by the memory controller are mainly performed and completed by the control component **1063** here. In some examples, the control component **1063** is, for example, a central processing unit (CPU), a microcontroller unit (MCU), etc. The ROM **1069** usually comprises firmware or firmware program codes of the memory controller **106**. These codes are used for initializing and operating various members of the memory controller, and the RAM **1070** is usually configured to buffer data. The error correction module **1064** may further comprise a encoding portion and a decoding portion. The encoding portion is configured to encode to-be-storage data to obtain check data, and the decoding portion is configured to decode the check data to detect and correct possible error data in a process of data transmission.

[0207] The garbage collection module **1065** is configured to: after a storage space of the memory device reaches a certain threshold, read out valid data in some memory blocks, perform rewrite, and then label these memory blocks, to obtain new spare memory blocks. A general implementation of garbage collection may comprise three operations: selecting a source memory block with a small amount of valid data; finding the valid data from the source memory block; and writing the valid data to a target memory block. In this case, all data in the source memory block becomes invalid data, and the source memory block is labeled, and may be taken as a new spare memory block. The wear leveling module **1066** is configured to level wear (a number of erase times) of each memory block in the memory system through data statistics and algorithms. A general implementation of wear leveling may comprise two operations: selecting a source memory block in which cold data is located; and reading valid data in the source memory block and writing the valid data in a memory block with a relatively large number of erase times. In this case, the valid data in the source memory block becomes invalid data, and the source memory block is labeled. The buffer **1067** is configured to buffer data.

[0208] In some examples, the memory device **104** comprises an array of memory cells comprising multiple memory cells, wherein a preset number of memory cells form one codeword; and a

peripheral circuit of the memory device **104** coupled with the array of memory cells and configured to perform the following operations: obtaining a first result corresponding to at least one codeword at a target read voltage, wherein the first result comprises the number of bits which represents the number of bits in the at least one codeword which are flipped in two read results at a first read voltage and a second read voltage, and a difference between the first read voltage and the second read voltage is less than a preset voltage; obtaining a first threshold according to the corresponding first result at the target read voltage, wherein the first threshold is to represent a corresponding first result at a maximum value in an effective range of predicted valley voltages; making at least one adjustment to the target read voltage, and after each adjustment, obtaining a corresponding first result at the adjusted target read voltage; and determining a target valley voltage according to a relationship between a corresponding first result at a target read voltage after one adjustment and the first threshold meeting a first preset condition or according to a corresponding first result at the target read voltage after multiple adjustments meeting a second preset condition, wherein the target valley voltage is taken as a read voltage at which a read operation is performed on the at least one codeword. In some examples, the memory controller **106** is configured to: control the memory device **104** to perform a first read operation on the at least one codeword.

[0209] In a second aspect, in the memory system provided in the examples of the present application, a first result (a size of the first result may be several bytes) rather than at least one codeword (for example, a size of the codeword may be 4 KB) is transmitted, so that an amount of data transmitted between the memory device and a memory controller is reduced. A first threshold is obtained according to a corresponding first result at a target read voltage. With the dynamic first threshold, the iterative rapidity of convergence of determining a target valley voltage is higher. A process of obtaining the first result converges inside the memory device, does not occupy a space of the memory controller, and has low dependency on the memory controller. A process of obtaining a predicted valley voltage/the target valley voltage according to the first result is completed in the memory device. At least one of a transmission time at an input/output port of the memory device or a time of an error correction decoding operation of the memory controller is reduced, so that an iterative time of an error correction decoding algorithm of the memory controller is saved, and a speed of error correction decoding is higher. The methods are applicable to a memory system of an MLC, a TLC type or a QLC type.

[0210] In a third aspect, examples of the present application provide a memory controller. The memory controller comprises a control component and is configured to: obtain a first result corresponding to at least one codeword at a target read voltage, wherein the at least one codeword is formed by a preset number of memory cells in an array of memory cells of at least one memory device coupled with the memory controller, wherein the first result comprises the number of bits which represents the number of bits in the at least one codeword which are flipped in two read results at a first read voltage and a second read voltage, and a difference between the first read voltage and the second read voltage is less than a preset voltage; obtain a first threshold according to the corresponding first result at the target read voltage, wherein the first threshold is to represent a corresponding first result at a maximum value in an effective range of predicted valley voltages; make at least one adjustment to the target read voltage, and after each adjustment, obtain a first result corresponding to the at least one codeword at the adjusted target read voltage; and determine a target valley voltage according to a relationship between a corresponding first result at a target read voltage after one adjustment and the first threshold meeting a first preset condition or according to a corresponding first result at the target read voltage after multiple adjustments meeting a second preset condition, wherein the target valley voltage is taken as a read voltage at which a read operation is performed on the at least one codeword.

[0211] In some examples, the control component is configured to: obtain the first threshold according to the corresponding first result at the target read voltage and a first mapping function, wherein the first mapping function is to represent a relationship between the corresponding first

result at the maximum value in the effective range of predicted valley voltages and the corresponding first result at the target read voltage.

[0212] In some examples, the control component is configured to: obtain the corresponding first result at the maximum value in the effective range of predicted valley voltages according to an initial value of the corresponding first result at the maximum value in the effective range of predicted valley voltages, a correction value for the corresponding first result at the target read voltage, and a correction coefficient, wherein the initial value of the corresponding first result at the maximum value in the effective range of predicted valley voltages and the correction coefficient are both fixed values related to a stage in which a read voltage is, and the larger the corresponding first result at the target read voltage is, the larger the correction value is.

[0213] In some examples, the first preset condition is that a corresponding first result at the target read voltage after one adjustment is less than the first threshold; and the control component is configured to: determine the target read voltage after one adjustment as the target valley voltage according to the relationship between the corresponding first result at the target read voltage after one adjustment and the first threshold meeting the first preset condition.

[0214] In some examples, the control component is configured to: according to the corresponding first result at the target read voltage being greater than or equal to the first threshold, obtain, with the corresponding first result at the target read voltage, a target adjustment value for adjusting the target read voltage; obtain a corresponding first result at the adjusted target read voltage with the target adjustment value; according to the corresponding first result at the adjusted target read voltage with the target adjustment value being less than the first threshold, determine the adjusted target read voltage with the target adjustment value as the target valley voltage; and according to the corresponding first result at the adjusted target read voltage with the target adjustment value being greater than or equal to the first threshold, make multiple adjustments to the target read voltage, and after each adjustment, obtain the corresponding first result at the adjusted target read voltage, until the corresponding first result at the adjusted target read voltage is less than the first threshold or the corresponding first result at the target read voltage after multiple adjustments meet the second preset condition.

[0215] In some examples, the second preset condition is that taken the minimum first result among multiple corresponding first results at the target read voltages after multiple adjustments as a reference value, the number of first results from remaining first results which differ from the reference value with a difference being less than a second threshold is greater than a preset number; and the control component is configured to: according to the corresponding first result at the target read voltage after multiple adjustments meeting the second preset condition, take a target read voltage corresponding to the minimum first result among the multiple first results as the target valley voltage.

[0216] In some examples, the control component is configured to: in a process of making multiple adjustments to the target read voltage, make adjustments by employing different adjustment methods, and according to the adjusted target read voltages corresponding to more than a preset number of adjustment methods in the different adjustment methods being same and the corresponding first result at the same target read voltage being the minimum value among all first results, take the same target read voltage as the target valley voltage.

[0217] In some examples, the control component is configured to: [0218] make multiple first adjustments to the target read voltage with a first step size, and obtain corresponding first results at target read voltages after the multiple first adjustments respectively; [0219] determine a value of knee point according to the obtained corresponding first results at the read voltages after the multiple first adjustments, wherein a target read voltage corresponding to the value of knee point is a knee-point voltage; make multiple second adjustments to the knee-point voltage with a second step size, and obtain the corresponding first results at the target read voltages after the multiple second adjustments respectively, wherein the second step size is less than the first step size; and

determine the target valley voltage with the obtained corresponding first results at the target read voltages after the multiple second adjustments.

[0220] In some examples, the corresponding first results at the target read voltages after the multiple first adjustments comprise a first adjacent value and a second adjacent value that are adjacent to the value of knee point, and the control component is configured to: according to a difference between the first adjacent value and the value of knee point being less than a difference between the second adjacent value and the value of knee point, narrow a range for the multiple second adjustments to be between a target read voltage corresponding to the first adjacent value and the knee-point voltage; and take an average of the read voltage corresponding to the first adjacent value and the knee-point voltage, and according to a corresponding first result at the average being less than the first threshold, take the average as the target valley voltage; and according to the corresponding first result at the average being greater than or equal to the first threshold, continue to make a second adjustment between the read voltage corresponding to the first adjacent value and the knee-point voltage, until a corresponding first result at the adjusted target read voltage is less than the first threshold.

[0221] In some examples, the control component is configured to: obtain the predicted valley voltage according to the corresponding first result at the target read voltage and a second mapping function, wherein the second mapping is to represent a relationship between the corresponding first result at the target read voltage and the predicted valley voltage, wherein the predicted valley voltage comprises a relationship between adjusted read voltages with the target adjustment value.

[0222] In some examples, the memory cell comprises multiple memory bits, and the multiple memory bits correspond to multiple pages respectively; and at least part of pages comprise multiple stages, the multiple stages comprise a first stage and a second stage, and a read voltage in the second stage is less than a read voltage in the first stage; and the control component is configured to: according to the stage number corresponding to the determined valley voltage belonging to the first stage, obtain at least one of a predicted valley voltage in the second stage from the multiple stages or a target valley voltage in other first stage corresponding to a lower read voltage with the determined target valley voltage.

[0223] In some examples, the memory controller is further configured to: control the memory device to perform a read operation on the at least one codeword with the target read voltage; and in response to an error occurring in reading of data in the at least one codeword at the target read voltage, control the memory device to perform the read operation on the codeword with the target valley voltage.

[0224] In some examples, the memory controller is further configured to: in response to an error occurring in reading of data in the at least one codeword at the target valley voltage, perform an ECC decoding operation on the data of the at least one codeword read at the target valley voltage.

[0225] In a third aspect, in the memory controller provided in the examples of the present application, a first result (a size of the first result may be several bytes) rather than at least one codeword (for example, a size of the codeword may be 4 KB) is transmitted, so that an amount of data transmitted between the memory device and a memory controller is reduced. A first threshold is obtained according to a corresponding first result at a target read voltage. With the dynamic first threshold, the iterative rapidity of convergence of determining a target valley voltage is higher. A process of obtaining the first result converges inside the memory device, does not occupy a space of the memory controller, and has low dependency on the memory controller. Compared with a memory device, efficiency of completing a process of obtaining a predicted valley voltage/the target valley voltage according to the first result is in the memory controller is higher. At least one of a transmission time at an input/output port of the memory device or a time of an error correction decoding operation of the memory controller is reduced, so that an iterative time of an error correction decoding algorithm of the memory controller is saved, and a speed of error correction decoding is higher. The methods are applicable to a memory system of an MLC, a TLC type or a

QLC type.

[0226] In a fourth aspect, examples of the present application provide a method of operating a memory device. The operation method comprises: obtaining a first result corresponding to at least one codeword at a target read voltage, the at least one codeword is formed by a preset number of memory cells in an array of memory cells of a memory device, wherein the first result comprises the number of bits which represents the number of bits in the at least one codeword which are flipped in two read results at a first read voltage and a second read voltage, and a difference between the first read voltage and the second read voltage is less than a preset voltage; obtaining a first threshold according to the corresponding first result at the target read voltage, wherein the first threshold is to represent a corresponding first result at a maximum value in an effective range of predicted valley voltages; making at least one adjustment to the target read voltage, and after each adjustment, obtaining a corresponding first result at the adjusted read voltage; and determine a target valley voltage according to a relationship between a corresponding first result at a target read voltage after one adjustment and the first threshold meeting a first preset condition or according to a corresponding first result at the target read voltage after multiple adjustments meeting a second preset condition, wherein the target valley voltage is taken as a read voltage at which a read operation is performed on the at least one codeword.

[0227] In some examples, the operation method comprises: obtaining the first threshold according to the corresponding first result at the target read voltage and a first mapping function, wherein the first mapping function is to represent a relationship between the corresponding first result at the maximum value in the effective range of predicted valley voltages and the corresponding first result at the target read voltage.

[0228] In some examples, the operation method comprises: obtaining the corresponding first result at the maximum value in the effective range of predicted valley voltages according to an initial value of the corresponding first result at the maximum value in the effective range of predicted valley voltages, a correction value for the corresponding first result at the target read voltage, and a correction coefficient, wherein the initial value of the corresponding first result at the maximum value in the effective range of predicted valley voltages and the correction coefficient are both fixed values related to a stage in which a read voltage is, and the larger the corresponding first result at the target read voltage is, the larger the correction value is.

[0229] In some examples, the operation method comprises: determining the target read voltage after one adjustment as the target valley voltage according to the relationship between the corresponding first result at the target read voltage after one adjustment and the first threshold meeting the first preset condition, wherein the first preset condition is that a corresponding first result at the target read voltage after one adjustment is less than the first threshold.

[0230] In some examples, the operation method comprises: according to the corresponding first result at the target read voltage being greater than or equal to the first threshold, obtaining, with the corresponding first result at the target read voltage, a target adjustment value for adjusting the target read voltage; obtaining a corresponding first result at the adjusted target read voltage with the target adjustment value; according to the corresponding first result at the adjusted target read voltage with the target adjustment value being less than the first threshold, determining the adjusted target read voltage with the target adjustment value as the target valley voltage; and according to the corresponding first result at the adjusted target read voltage with the target adjustment value being greater than or equal to the first threshold, making multiple adjustments to the target read voltage, and after each adjustment, obtaining the corresponding first result at the adjusted target read voltage, until the corresponding first result at the adjusted target read voltage is less than the first threshold or the corresponding first result at the target read voltage after multiple adjustments meet the second preset condition.

[0231] In some examples, the operation method comprises: according to the corresponding first result at the target read voltage after multiple adjustments meeting the second preset condition,

taking a target read voltage corresponding to the minimum first result among the multiple first results as the target valley voltage, wherein the second preset condition is that taken the minimum first result among multiple corresponding first results at the target read voltages after multiple adjustments as a reference value, the number of first results from remaining first results which differ from the reference value with a difference being less than a second threshold is greater than a preset number.

[0232] In some examples, the operation method comprises: in a process of making multiple adjustments to the target read voltage, making adjustments by employing different adjustment methods, and according to the adjusted target read voltages corresponding to more than a preset number of adjustment methods in the different adjustment methods being same and the corresponding first result at the same target read voltage being the minimum value among all first results, using the same target read voltage as the target valley voltage.

[0233] In some examples, the operation method comprises: making multiple first adjustments to the target read voltage with a first step size, and obtaining corresponding first results at target read voltages after the multiple first adjustments respectively; determining a value of knee point according to the obtained corresponding first results at the read voltages after the multiple first adjustments, wherein a target read voltage corresponding to the value of knee point is a knee-point voltage; making multiple second adjustments to the knee-point voltage with a second step size, and obtaining corresponding first results at target read voltages after the multiple second adjustments respectively, wherein the second step size is less than the first step size; and determining the target valley voltage with the obtained corresponding first results at the target read voltages after the multiple second adjustments.

[0234] In some examples, the operation method comprises: according to a difference between the first adjacent value and the value of knee point being less than a difference between the second adjacent value and the value of knee point, narrowing down a range for the multiple second adjustments between a target read voltage corresponding to the first adjacent value and the knee-point voltage; and taking an average of the read voltage corresponding to the first adjacent value and the knee-point voltage, and according to a corresponding first result at the average being less than the first threshold, using the average as the target valley voltage; and according to the corresponding first result at the average being greater than or equal to the first threshold, continuing to make a second adjustment between the read voltage corresponding to the first adjacent value and the knee-point voltage, until a corresponding first result at the adjusted target read voltage is less than the first threshold, wherein the corresponding first results at the target read voltages after the multiple first adjustments comprise a first adjacent value and a second adjacent value that are adjacent to the value of knee point.

[0235] In some examples, the operation method comprises: obtaining the predicted valley voltage according to the corresponding first result at the target read voltage and a second mapping function, wherein the second mapping is to represent a relationship between the corresponding first result at the target read voltage and the predicted valley voltage.

[0236] In some examples, the operation method comprises: according to the stage number corresponding to the determined target valley voltage belonging to the first stage, obtaining at least one of a predicted valley voltage in the second stage from the multiple stages or a target valley voltage in other first stage corresponding to a lower read voltage with the determined target valley voltage, wherein the memory cell comprises multiple memory bits, and the multiple memory bits correspond to multiple pages respectively; and at least part of pages correspond to multiple stages, the multiple stages comprise a first stage and a second stage, and a read voltage in the second stage is less than a read voltage in the first stage.

[0237] In some examples, the operation method comprises: reading storage data of the at least one codeword at the first read voltage, to obtain a second result; reading storage data of the at least one codeword at the second read voltage, to obtain a third result; performing a logical operation on the

second result and the third result, to obtain a fourth result; and calculating a number of bits that are in the fourth result and represent flips in the third result with respect to the second result, to obtain the first result.

[0238] In a fifth aspect, examples of the present application provide a method of operating a memory system, wherein the memory system comprises a memory device and a memory controller coupled with the memory device and controlling the memory device, and the operation method comprises: performing any operation method of the memory device provided in the fourth aspect.

[0239] In some examples, the operation method of the memory device comprises: obtaining a first result corresponding to at least one codeword at a target read voltage, the at least one codeword is formed by a preset number of memory cells in an array of memory cells of a memory device, wherein the first result comprises the number of bits which represents the number of bits in the at least one codeword which are flipped in two read results at a first read voltage and a second read voltage, and a difference between the first read voltage and the second read voltage is less than a preset voltage; obtaining a first threshold according to the corresponding first result at the target read voltage, wherein the first threshold is to represent a corresponding first result at a maximum value in an effective range of predicted valley voltages; making at least one adjustment to the target read voltage, and after each adjustment, obtaining a corresponding first result at the adjusted read voltage; and determining a target valley voltage according to a relationship between a corresponding first result at a target read voltage after one adjustment and the first threshold meeting a first preset condition or according to a corresponding first result at the target read voltage after multiple adjustments meeting a second preset condition, wherein the target valley voltage is taken as a read voltage at which a read operation is performed on the at least one codeword.

[0240] In a sixth aspect, examples of the present application provide a method of operating a memory controller. The operation method comprises: obtaining a first result corresponding to at least one codeword at a target read voltage, wherein the at least one codeword is formed by a preset number of memory cells in at least one memory device coupled with the memory controller, wherein the first result comprises the number of bits which represents the number of bits in the at least one codeword which are flipped in two read results at a first read voltage and a second read voltage, and a difference between the first read voltage and the second read voltage is less than a preset voltage; obtaining a first threshold according to the corresponding first result at the target read voltage, wherein the first threshold is to represent a corresponding first result at a maximum value in an effective range of predicted valley voltages; making at least one adjustment to the target read voltage, and after each adjustment, obtaining a corresponding first result at the adjusted target read voltage; and determining a target valley voltage according to a relationship between a corresponding first result at a target read voltage after one adjustment and the first threshold meeting a first preset condition or according to a corresponding first result at the target read voltage after multiple adjustments meeting a second preset condition, wherein the target valley voltage is taken as a read voltage at which a read operation is performed on the at least one codeword.

[0241] In some examples, the operation method comprises: obtaining the first threshold according to the corresponding first result at the target read voltage and a first mapping function, wherein the first mapping function is to represent a relationship between the corresponding first result at the maximum value in the effective range of predicted valley voltages and the corresponding first result at the target read voltage.

[0242] In some examples, the operation method comprises: obtaining the corresponding first result at the maximum value in the effective range of predicted valley voltages according to an initial value of the corresponding first result at the maximum value in the effective range of predicted valley voltages, a correction value for the corresponding first result at the target read voltage, and a correction coefficient, wherein the initial value of the corresponding first result at the maximum value in the effective range of predicted valley voltages and the correction coefficient are both fixed values related to a stage in which a read voltage is, and the larger the corresponding first

result at the target read voltage is, the larger the correction value is.

[0243] In some examples, the operation method comprises: determining the target read voltage after one adjustment as the target valley voltage according to the relationship between the corresponding first result at the target read voltage after one adjustment and the first threshold meeting the first preset condition, wherein the first preset condition is that a corresponding first result at the target read voltage after one adjustment is less than the first threshold.

[0244] In some examples, the operation method comprises: according to the corresponding first result at the target read voltage being greater than or equal to the first threshold, obtaining, with the corresponding first result at the target read voltage, a target adjustment value for adjusting the target read voltage; obtaining a corresponding first result at the adjusted target read voltage with the target adjustment value; according to the corresponding first result at the adjusted target read voltage with the target adjustment value being less than the first threshold, determining the adjusted target read voltage with the target adjustment value as the target valley voltage; and according to the corresponding first result at the adjusted target read voltage with the target adjustment value being greater than or equal to the first threshold, making multiple adjustments to the target read voltage, and after each adjustment, obtaining the corresponding first result at the adjusted target read voltage, until the corresponding first result at the adjusted target read voltage is less than the first threshold or the corresponding first result at the target read voltage after multiple adjustments meet the second preset condition.

[0245] In some examples, the operation method comprises: according to the corresponding first result at the target read voltage after multiple adjustments meeting the second preset condition, taking a target read voltage corresponding to the minimum first result among the multiple first results as the target valley voltage, wherein the second preset condition is that taken the minimum first result among multiple corresponding first results at the target read voltages after multiple adjustments as a reference value, the number of first results from remaining first results which differ from the reference value with a difference being less than a second threshold is greater than a preset number.

[0246] In some examples, the operation method comprises: in a process of making multiple adjustments to the target read voltage, making adjustments by employing different adjustment methods, and according to the adjusted target read voltages corresponding to more than a preset number of adjustment methods in the different adjustment methods being same and the corresponding first result at the same target read voltage being the minimum value among all first results, using the same target read voltage as the target valley voltage.

[0247] In some examples, the operation method comprises: making multiple first adjustments to the target read voltage with a first step size, and obtaining corresponding first results at target read voltages after the multiple first adjustments respectively; determining a value of knee point according to the obtained corresponding first results at the read voltages after the multiple first adjustments, wherein a target read voltage corresponding to the value of knee point is a knee-point voltage; making multiple second adjustments to the knee-point voltage with a second step size, and obtaining corresponding first results at target read voltages after the multiple second adjustments respectively, wherein the second step size is less than the first step size; and determining the target valley voltage with the obtained corresponding first results at the target read voltages after the multiple second adjustments.

[0248] In some examples, the operation method comprises: according to a difference between the first adjacent value and the value of knee point being less than a difference between the second adjacent value and the value of knee point, narrowing down a range for the multiple second adjustments between a target read voltage corresponding to the first adjacent value and the knee-point voltage; and taking an average of the read voltage corresponding to the first adjacent value and the knee-point voltage, and according to a corresponding first result at the average being less than the first threshold, using the average as the target valley voltage; and according to the

corresponding first result at the average being greater than or equal to the first threshold, continuing to make a second adjustment between the read voltage corresponding to the first adjacent value and the knee-point voltage, until a corresponding first result at the adjusted target read voltage is less than the first threshold, wherein the corresponding first results at the target read voltages after the multiple first adjustments comprise a first adjacent value and a second adjacent value that are adjacent to the value of knee point.

[0249] In some examples, the operation method comprises: obtaining the predicted valley voltage according to the corresponding first result at the target read voltage and a second mapping function, wherein the second mapping is to represent a relationship between the corresponding first result at the target read voltage and the predicted valley voltage, wherein the predicted valley voltage comprises a relationship between adjusted read voltages with the target adjustment value.

[0250] In some examples, the operation method comprises: according to the stage number corresponding to the determined target valley voltage belonging to the first stage, obtaining at least one of a predicted valley voltage in the second stage from the multiple stages or a target valley voltage in other first stage corresponding to a lower read voltage with the determined target valley voltage, wherein the memory cell comprises multiple memory bits, and the multiple memory bits correspond to multiple pages respectively; and at least part of pages comprise multiple stages, the multiple stages comprise a first stage and a second stage, and a read voltage in the second stage is less than a read voltage in the first stage.

[0251] In some examples, the operation method comprises: controlling the memory device to perform a read operation on the at least one codeword with the target read voltage; and in response to an error occurring in reading of data in the at least one codeword at the target read voltage, controlling the memory device to perform the read operation on the codeword with the target valley voltage.

[0252] In some examples, the operation method comprises: in response to an error occurring in reading of data in the at least one codeword at the target valley voltage, performing an ECC decoding operation on the data of the at least one codeword read at the target valley voltage.

[0253] FIG. **13** is a block flowchart **1** of a method of operating a memory device provided by an example of the present application. A detailed process of determining a target valley voltage is described below in detail with reference to FIG. **13**. It is to be noted that, here and below, the target valley voltage is a voltage used for performing a read operation on data to be read.

[0254] In operation S**101**, the program of obtaining the target valley voltage is triggered, and the process of obtaining the target valley voltage is started. Next, operation S**102** is performed.

[0255] As described above, according to the memory cell comprising multiple memory bits, the multiple memory bits correspond to multiple pages respectively, and at least one page corresponds to multiple stages. During determining of the target valley voltage, the target valley voltage among the read voltages in each of the at least one stage corresponding to each of the multiple pages is determined in sequence. In operation S**103**, one stage is selected from multiple stages corresponding to one page as a target stage, and a target valley voltage corresponding to a read voltage of the target stage is first determined. In an example, a TLC is taken as an example. Target valley voltages of a first-level read voltage L**1** and a fifth-level read voltage L**5** corresponding to a lower page are first determined, and one of L**1** or L**5** may be selected as the target stage. After the target stage is determined, operation S**103** is performed.

[0256] In the operation S**103**, a type of the target stage is mainly determined. Here, the target stage may be classified into two classes: a first stage (or referred to as a high stage) and a second stage (or referred to as a low stage). A read voltage in a first stage is greater than a read voltage in a second stage. In an example, the lower page of the TLC is still used as an example, L**5** is the first stage, and L**1** is the second stage. If L**1** is selected as the target stage in the operation S**103**, the target stage is the second stage, that is, the low stage. If L**5** is selected as the target stage in operation S**104**, the target stage is the first stage, that is, the high stage. According to the target

stage being the low stage, the operation S**104** is performed. According to the target stage being the high stage, operation S**106** is performed.

[0257] In the operation S**104**, a predicted valley voltage is obtained. Here, the predicted valley voltage is a predicted valley voltage corresponding to a low stage obtained according to a target valley voltage corresponding to the high stage and a related mapping function. Here and below, the related mapping function may be obtained by fitting a large number of experimental results before the memory device is delivered from a factory, and is saved in the memory device. Next, operation S**105** is performed.

[0258] In the operation S**105**, it is determined whether prediction by two-step method succeeds. Here, the two-step prediction may comprise first-step prediction and second-step prediction. The first-step prediction is to obtain a predicted valley voltage in the high stage. In an example manner, the predicted valley voltage in the high stage is obtained according to a corresponding first result at a target read voltage (a default read voltage), the stage number in which the high stage is, and a fourth mapping function. The second-step prediction is to obtain the predicted valley voltage in the low stage. In an example manner, the predicted valley voltage in the low stage is obtained according to the foregoing predicted valley voltage in the high stage, the stage number in which the low stage is, and a third mapping function. In addition, confirmation of the predicted valley voltage is not performed after two-step prediction is performed, and hard decoding is directly performed with the predicted valley voltage in the high stage and the predicted valley voltage in the low stage. If the hard decoding succeeds, it represents that the prediction by two-step method succeeds. In this case, a search for a target valley voltage is directly stopped, and operation S**121** is performed. If the hard decoding fails, it represents that the prediction by two-step method fails. In this case, a point corresponding to the predicted valley voltage is taken as a near-valley point of a subsequent iteration, and operation S**107** continues to be performed.

[0259] It is to be noted that, if the hard decoding fails, it represents that the prediction by two-step method does not succeed. In this case, the target valley voltage needs to be determined in a manner of a search or a cycle (or an iteration). Therefore, when the prediction by two-step method does not succeed, a process of the cycle is entered. After the prediction by two-step method does not succeed, a search process may be directly performed from a start of the cycle. That is, the process jumps from the operation S**105** to S**107**.

[0260] If the target stage is a high stage, a target valley voltage in the high stage is to be determined in a manner of a search or a cycle. In the operation S**106**, the default read voltage is taken as the target read voltage. Here, the target read voltage may be taken as an initial value of a subsequent search or cycle. In some examples, the default read voltage may be a read voltage before a threshold voltage of the memory cell deviates, for example, corresponding read voltage upon a write. In this case, a corresponding deviation value is 0 DAC. The operation S**107** is performed after the operation S**106**.

[0261] It is to be noted that, here and below, a conversion relationship between a DAC and the foregoing mv is 1 DAC=10 mv.

[0262] In the operation S**107**, the target valley voltage starts to be determined in a manner of a search or a cycle. The operation S**108** is performed after the operation S**107**.

[0263] For a process of performing a cycle for the first time, in the operation S**108**, the first result at the target read voltage is obtained. It may be understood that for a process of performing a cycle subsequently, in the operation S**108**, a first result at a target read voltage after an adjustment is obtained. Operation S**109** is performed after the operation S**108**.

[0264] In the operation S**109**, a first threshold TH**1** is determined or adjusted according to the first result at the target read voltage. It may be understood that, when a read operation is performed, when the threshold voltage of the memory cell deviates farther compared with a threshold voltage during a write, the first result read with the target read voltage is usually also relatively large. Based on this, the first threshold TH**1** may be confirmed with a specific value of a first result at the default

read voltage. The first threshold TH**1** is to represent a change (rise) in the target valley voltage caused by the deviation of the threshold voltage of the memory cell. The operation S**110** is performed after the operation S**109**.

[0265] It is to be noted that, the operation S**109** is mainly for the process of performing the cycle for the first time. For the process of performing the cycle subsequently, the operation may be skipped.

[0266] In the operation S**110**, the predicted valley voltage is generated, and it is determined whether the predicted valley voltage is less than the aforementioned first threshold TH**1**. Based on the corresponding first result at the target read voltage after the previous adjustment and the associated mapping function (e.g., the aforementioned second mapping function), the predicted read voltage after next adjustment is generated, and the generated predicted valley voltage is compared with the magnitude of the first threshold TH**1**. When the determination result in operation S**110** is no, it indicates that the predicted valley voltage generated at this point is greater than or equal to the first threshold TH**1**, and the operation S**108** of the loop continues where an adjustment is made to the target read voltage and the predicted valley voltage is re-generated, after each re-generation of the predicted valley voltage, a comparison with the first threshold TH**1** is performed until the generated predicted read voltage is less than the first threshold TH**1**. That is to say, the aforementioned prediction formula or related mapping function is used to perform prediction iteration until the generated predicted read voltage is less than the first threshold TH**1**. When the determination result in operation S**110** is yes, it indicates that the predicted valley voltage generated at this point is less than the first threshold TH**1**, and the process proceeds to the next operation S**111**.

[0267] In operation S**111**, search for a knee point. Here, the target read voltage after each adjustment is taken as the abscissa, and the corresponding first result at the corresponding adjusted target read voltage is taken as the ordinate, the abscissa and ordinate will form a point. The knee point may be understood as a point closer to the valley bottom. In some examples, starting from the near-valley point, searching with a coarser step size (a first step size) may be performed to the left boundary and the right boundary respectively until reaching the left boundary and the right boundary, and the point corresponding to the minimum first result during the search process is taken as the knee point. Here, the knee point is a point that is closer to the valley bottom than the near-valley point, and the point less than the first threshold in the preceding operation may be taken as a near-valley point, e.g., the near-valley point may be a point less than the first threshold that first appears in the preceding operation. The first step size may be a larger step size, and in some examples, the first step size may be 5 DAC-15 DAC, in one example, the first step size may be 5 DAC, 10 DAC or 15 DAC. Operation S**112** is performed after operation S**111**.

[0268] In operation S**112**, it is determined whether the knee point has been found. If the knee point is not found, the search continues and operation S**111** is continued until the knee point is found. After the knee point is found, operation S**113** is performed.

[0269] In operations S**113** and S**114**, starting from the near-valley point, searching with a finer step size (a second step size) may be performed to the left boundary and the right boundary respectively until reaching the left boundary and the right boundary or the counted number for upward trend exceeds a preset number. Here when a corresponding first result at the target read voltage after a next adjustment is greater than the corresponding first result at the target read voltage after a previous adjustment, one for upward trend is counted. In some examples, the preset number is 3-7, in one example, the preset number of may be 3, 5, or 7. It should be noted that the locations of operations S**113** and S**114** may be interchanged. The second step size may be a smaller step size, and in some examples, the second step size may be 2 DAC-4 DAC, in one example, the second step size may be 2 DAC, 3 DAC or 4 DAC.

[0270] When the searches in the operation S**113** and the operation S**114** both meet the foregoing conditions (the boundaries are reached or the count of rising trends exceeds the preset number of

times), operation S**115** is performed.

[0271] In the operation S**115**, an adjusted target read voltage corresponding to the minimum first result is taken as the target valley voltage. The operation S**116** is performed after the operation S**115**.

[0272] In operation S**116**, it is determined whether the target valley voltage is valid. Here, the way to determine whether the target valley voltage is valid may be: reading data with the target valley voltage, decoding the read data through the memory controller, and when the decoding is successful, it indicates whether the target valley voltage is valid. When the determination result in operation S**116** is yes, operation S**121** is performed; when the determination result in operation S**116** is no, operation S**117** is performed.

[0273] In the operation S**117**, it is determined whether the cycle ends. When the determination result of the operation S**117** is yes, the operation S**119** is performed. When the determination result of the operation S**117** is no, operation S**118** is performed.

[0274] In operation S**118**, enter the next cycle and searching continues. Operation S**118** jumps to operation S**107**.

[0275] In the operation S**119**, it is determined whether the target stage is a high stage. When a determination result of the operation S**119** is yes, the operation S**120** is performed. When the determination result of the operation S**119** is no, operation S**121** is performed.

[0276] In the operation S**120**, the predicted valley voltage in the low stage is obtained according to the target valley voltage in the high stage. Here, the predicted valley voltage in the low stage may be obtained through the target valley voltage in the high stage, the stage number in which the low stage is, and the related mapping function (for example, the foregoing third mapping function). The operation S**121** is performed after the operation S**120**.

[0277] In operation S**121**, it is determined whether corresponding target valley voltages have been determined for read voltages in all the stages contained on this page. When the determination result in operation S**121** is yes, it indicates that target valley voltages corresponding to read voltages in all the stages contained on this page have been determined, and operation S**123** may be performed at this point; and when the determination result in operation S**121** is no, it indicates that target valley voltages corresponding to read voltages in some of the stages contained on this page have not been determined, and operation S**122** may be performed at this point.

[0278] In operation S**122**, for the stages in which the target valley voltages are not determined, the target valley voltage in each of the stages is determined in sequence. Operation S**122** jumps to operation S**102**.

[0279] In the operation S**123**, the process of obtaining the target valley voltage ends. It should be noted that after operation S**123**, the determination of the target valley voltage corresponding to the read voltages in all stages for the next page may be started.

[0280] FIG. **14** is a block flowchart **2** of a method of operating a memory device provided by an example of the present application. A detailed process of determining a target valley voltage is described below in detail with reference to FIG. **14**.

[0281] In operation S**201**, the program of obtaining the target valley voltage is triggered, and the process of obtaining the target valley voltage is started. Next, operation S**202** is performed.

[0282] In the operation S**202**, in some examples, a read mode of the memory device is set to a single-level read mode. The single-level read mode comprises reading, through a read voltage in one stage, at least one bit of storage data stored in a memory cell. Next, operation S**203** is performed.

[0283] As described above, according to the memory cell comprising multiple memory bits, the multiple memory bits correspond to multiple pages respectively, and at least one page corresponds to multiple stages. During determining of the target valley voltage, the target valley voltage among the read voltages in each of the at least one stage corresponding to each of the multiple pages is determined in sequence. In operation S**203**, one stage is selected from multiple stages

corresponding to one page as a target stage, and a target valley voltage corresponding to a read voltage of the target stage is first determined. In an example, a TLC is taken as an example. Target valley voltages of a first-level read voltage L**1** and a fifth-level read voltage L**5** corresponding to a lower page are first determined, and one of L**1** or L**5** may be selected as the target stage. After the target stage is determined, operation S**204** is performed.

[0284] In the operation S**204**, a type of the target stage is mainly determined. Here, the target stage may be classified into two classes: a first stage (or referred to as a high stage) and a second stage (or referred to as a low stage). A read voltage in a first stage is greater than a read voltage in a second stage. In an example, the lower page of the TLC is still used as an example, L**5** is the first stage, and L**1** is the second stage. If L**1** is selected as the target stage in the operation S**203**, the target stage is the second stage, that is, the low stage. If L**5** is selected as the target stage in operation S**204**, the target stage is the first stage, that is, the high stage. According to the target stage being the low stage, the operation S**205** is performed. According to the target stage being the high stage, operation S**207** is performed.

[0285] In the operation S**205**, a predicted valley voltage is obtained. Here, the predicted valley voltage is a predicted valley voltage corresponding to a low stage obtained according to a target valley voltage corresponding to the high stage and a related mapping function. Here and below, the related mapping function may be obtained by fitting a large number of experimental results before the memory device is delivered from a factory, and is saved in the memory device. Next, operation S**206** is performed.

[0286] In the operation S**206**, it is determined whether prediction by two-step method succeeds. Here, the two-step prediction may comprise first-step prediction and second-step prediction. The first-step prediction is to obtain a predicted valley voltage in the high stage. In an example manner, the predicted valley voltage in the high stage is obtained according to a corresponding first result at a target read voltage (a default read voltage), the stage number in which the high stage is, and a fourth mapping function. The second-step prediction is to obtain the predicted valley voltage in the low stage. In an example manner, the predicted valley voltage in the low stage is obtained according to the foregoing predicted valley voltage in the high stage, the stage number in which the low stage is, and a third mapping function. In addition, confirmation of the predicted valley voltage is not performed after two-step prediction is performed, and hard decoding is directly performed with the predicted valley voltage in the high stage and the predicted valley voltage in the low stage. If the hard decoding succeeds, it represents that the prediction by two-step method succeeds. In this case, a search for a target valley voltage is directly stopped, and operation S**245** is performed. If the hard decoding fails, it represents that the prediction by two-step method fails. In this case, a point corresponding to the predicted valley voltage is taken as a near-valley point of a subsequent iteration, and operation S**220** continues to be performed. The operation S**220** is described in detail in the subsequent description.

[0287] It is to be noted that, if the hard decoding fails, it represents that the prediction by two-step method does not succeed. In this case, the target valley voltage needs to be determined in a manner of a search or a cycle (or an iteration). Therefore, when the prediction by two-step method does not succeed, a process of the cycle is entered. After the prediction by two-step method does not succeed, a search process may be directly performed from a start of the cycle. That is, the process jumps from the operation S**206** to S**208**. Alternatively, the point corresponding to the predicted valley voltage may be directly used as the near-valley point of the subsequent iteration. That is, the process jumps from the operation S**206** (S**219**) to S**220**.

[0288] If the target stage is a high stage, a target valley voltage in the high stage is to be determined in a manner of a search or a cycle. In the operation S**207**, the default read voltage is taken as the target read voltage. Here, the target read voltage may be taken as an initial value of a subsequent search or cycle. In some examples, the default read voltage may be a read voltage before a threshold voltage of the memory cell deviates, for example, corresponding read voltage upon a

write. In this case, a corresponding deviation value is 0 DAC. The operation S**208** is performed after the operation S**207**.

[0289] In the operation S**208**, the target valley voltage starts to be determined in a manner of a search or a cycle. The operation S**209** is performed after the operation S**208**.

[0290] For the first performing of the cycle, in operation S**209**, the first result at the target read voltage is obtained; it may be understood that for the subsequent performing of the cycle, in operation S**209**, the first result at the adjusted target read voltage is obtained. Operation S**210** is performed after operation S**209**.

[0291] In operation S**210**, parameters are determined or adjusted in accordance with the first result at the target read voltage, the parameters here may at least include a first threshold, a first boundary voltage (the location corresponding to the first boundary voltage is also referred to as the left boundary) and a second boundary voltage (the location corresponding to the second boundary voltage is also referred to as the right boundary). It may be understood that when performing a read operation, the further the threshold voltage of the memory cell deviates from the threshold voltage during writing, the first result of reading with the target read voltage will generally be larger, based on this, the value of the first result at the default read voltage may be used to confirm the first threshold, and the first threshold is to present the change (lifting) in the target valley voltage caused by the offset of the threshold voltage of the memory cell. Here, the initial first boundary voltage and the initial second boundary voltage may be set in accordance with empirical values, etc., for example, a relatively large range of the initial first boundary voltage and an initial second boundary voltage are first set, and then the initial first boundary voltage and the initial second boundary voltage are adjusted in accordance with the first result at the target read voltage, e.g., narrowing the range of a boundary voltage and a second boundary voltage, to obtain the first boundary voltage and the second boundary voltage. Operation S**211** is performed after operation S**210**.

[0292] It is to be noted that, the operation S**210** is mainly for the process of performing the cycle for the first time. For the process of performing the cycle subsequently, the operation may be skipped.

[0293] For a process of performing a cycle for the first time, in the operation S**211**, it is determined whether the first result at the target read voltage is less than a first threshold. It may be understood that for a process of performing a cycle subsequently, in the operation S**211**, it is determined whether a first result at a target read voltage after an adjustment is less than the first threshold. When a determination result of the operation S**211** is yes, it may be considered that in this case, the corresponding first result at the adjusted target read voltage may basically meet requirements of decoding read data. Next, the process jumps to S**242**, and the cycle ends, to output a corresponding target valley voltage. When the determination result of the operation S**211** is no, operation S**212** of the cycle is continued.

[0294] In the operation S**212**, it is determined whether a target memory block is a memory block that is not full. Here, the target memory block is a memory block in which at least one codeword on which the read operation is to be performed is located. The memory block that is not full comprises a memory block with two data states being a programmed state and an erased state. When the determination result of the operation S**212** is yes, the operation S**213** is performed. When the determination result of the operation S**212** is no, operation S**214** is performed.

[0295] It is to be noted that, the operation S**212** is mainly for the process of performing the cycle for the first time. For the process of performing the cycle subsequently, the operation may be skipped. After the operation is skipped, the operation S**214** continues to be performed.

[0296] In the operation S**213**, considering that the offset of the threshold voltage of memory cell in a memory block that is not full is more complicated compared to the offset of the threshold voltage of memory cell in a memory block that is full (a memory block that is full may be understood as a memory block whose writing time difference is less than the preset duration in the same application scenario as a memory block that is not full). Compared with the memory block that is full, the

offset of the threshold voltage of memory cell in a memory block that is not full is related to the location of the first blank physical page in the memory block that is not full (the first blank physical page may be understood as the physical page in which the first data state appearing in the memory block that is not full is all erase state in accordance with the program sequence) and the location of the physical page to be read (the physical page where at least one codeword to be read is located). Based on this, the predicted valley voltage may be generated in accordance with the first offset corresponding to the memory block that is full, the second offset corresponding to the location of the first blank physical page in the memory block that is not full, and the third offset corresponding to the location of the physical page to be read, and then proceed to operation S**214**. It is to be understood that the generated predicted valley voltage is more targeted than the blind adjustment of the target read voltage, and can shorten the search time to a certain extent and determine the target valley voltage faster.

[0297] In the operation S**214**, it is determined whether the near-valley point is found. Here, a target read voltage after each adjustment is taken as a horizontal coordinate, and a corresponding first result at the adjusted target read voltage is taken as a vertical coordinate. The horizontal coordinate and the vertical coordinate form one point. In a process of making multiple adjustments to the target read voltage, a point corresponding to a first result less than a near-valley threshold for the first time in multiple corresponding first results at multiple adjusted target read voltages is taken as the near-valley point. The near-valley threshold is to represent the largest value close to a corresponding first result at the target valley voltage. It is to be noted that, the near-valley threshold has a difference from the foregoing first threshold, when the first result is less than the near-valley threshold, it represents that a finer search may be performed next. When the first result is less than the first threshold, it represents that it may be considered to stop the search next. When the determination result of the operation S**214** is yes, the operation S**219** is performed. When the determination result of the operation S**214** is no, operation S**215** is performed.

[0298] In the operation S**215**, when the near-valley point is not found, the operation S**215** is performed. A predicted read voltage after a next adjustment is obtained according to a corresponding first result at a target read voltage after a previous adjustment and the related mapping function (for example, the foregoing second mapping function). That is, predictive iteration is performed with the foregoing prediction formula or the mapping function. The operation S**216** is performed after the operation S**215**.

[0299] In the operation S**216**, it is determined whether the obtained predicted read voltage after the next adjustment hits a boundary. Here, the boundary may be one of the foregoing left the boundary or right the boundary, and the "hits a boundary" may be understood as that the voltage is right at the boundary or has crossed the boundary. When the determination result of the operation S**216** is yes, the operation S**217** is performed. When the determination result of the operation S**216** is no, operation S**218** is performed.

[0300] In the operation S**217**, an adjustment direction is changed. Here, in a process of adjusting the target read voltage, there are two adjustment directions, that is, a positive direction (to the right) and a negative direction (to the left). An adjustment to a deviation direction may be understood as that, an adjustment is made to the right before, and after the right the boundary is hit, an adjustment to the left starts to be made. Alternatively, an adjustment is made to the left before, and after the left the boundary is hit, an adjustment to the right starts to be made. The operation S**218** is performed after the operation S**217**.

[0301] In the operation S**218**, the first result at the adjusted target read voltage is obtained. After the operation S**218**, the operation S**214** is performed. That is, every time after the target read voltage is adjusted and a corresponding first result is obtained, it continues to be determined whether a latest adjustment point is the near-valley point. Here, one or multiple adjustments are made until the near-valley point is found.

[0302] It is to be noted that, if a next cycle is entered because subsequent conditions are not met in

a process of operations after the near-valley point is found, the operations S**215** to S**218** may be skipped.

[0303] In the operation S**219**, refer to the description in the operation S**206**. When the prediction by two-step method does not succeed, the process of the cycle is entered. After the prediction by two-step method does not succeed, the point corresponding to the predicted valley voltage may be directly used as the near-valley point of the subsequent iteration. That is, the process jumps from the operation S**219** to S**220**.

[0304] In the operation S**220**, it is determined whether a predicted valley voltage (a latest target read voltage after an adjustment) of a current point is effective. In some examples, it may be determined that the predicted valley voltage is effective through a corresponding first result at the latest adjusted target read voltage is less than the first threshold. It is to be noted that, in the operation S**211**, S**212** and subsequent operations are performed when the first result at the target read voltage (after the adjustment) is not less than the first threshold. However, before the determination result of the operation S**214** is yes, the target read voltage is adjusted again at least once. Therefore, in this case, a new adjusted target read voltage may be less than the first threshold. When the determination result of the operation S**220** is yes, the operation S**224** is performed. When the determination result of the operation S**220** is no, operation S**221** is performed.

[0305] In the operation S**221**, it is determined whether a first result fbc of the current point is greater than an fbc of a previous point. Here, after the near-valley point is found, in a process of starting to roughly search for a knee point to the left, a value change of the fbc is usually decreasing first and then increasing. When the first result fbc of the current point is greater than the fbc of the previous point, it indicates that in a subsequent process of making an adjustment to the left, the fbc further increases. The previous point is a relatively small point. In this case, the previous point is set as the knee point. In some examples, a step size used in the rough search may be a large step size, for example, may range from 5 DAC to 15 DAC, and in an example, may be 5 DAC, 10 DAC or 15 DAC. Based on this, when a determination result of the operation S**221** is yes, the operation S**223** is performed. When the determination result of the operation S**221** is no, operation S**222** is performed.

[0306] In the operation S**222**, a rough search is made to the left starting from the near-valley point, and after each search, comparison is made with an fbc in a previous search, until a point with an fbc that stops decreasing and starts to increase is found. After the point is found, that is, it indicates that the operation S**222** is completed, and the process jumps to the operation S**223**.

[0307] In the operation S**223**, the previous point (that is, the foregoing point with the fbc that stops decreasing and starts to increase) is set as the knee point, and a fine search is made to the right starting from the knee point. In some examples, a step size used in the fine search may be a small step size, for example, may range from 1 DAC to 4 DAC, and in an example, may be 2 DAC or 3 DAC. The operation S**225** is performed after the operation S**223**.

[0308] In the operation S**224**, the current point is set as the knee point, and a fine search is made to the right starting from the knee point. In some examples, for a step size used in the fine search, refer to the operation S**223**. The operation S**225** is performed after the operation S**224**.

[0309] In the operation S**225**, it is determined whether to adjust the target read voltage to the left. When the determination result of the operation S**225** is yes, the operation S**229** is performed. When the determination result of the operation S**225** is no, operation S**226** is performed.

[0310] In the operation S**226**, the target read voltage is adjusted to the right, and in a process of adjusting the target read voltage to the right, it is determined whether the right boundary is hit or whether a rise count (or referred to as a count of rising trends, wherein when a corresponding first result at a target read voltage after a next adjustment is greater than a corresponding first result at a target read voltage after a previous adjustment, one for upward trend is counted) exceeds a preset number TH**2** of times. In some examples, the preset number of times ranges from 3 to 7. In an example, the preset number of times may be 3, 5 or 7. When the determination result of the

operation S**226** is yes, the operation S**228** is performed. When the determination result of the operation S**226** is no, operation S**227** is performed.

[0311] In the operation S**227**, when the right boundary is not hit or the rise count does not exceed the preset number TH**2** of times, a search to the right boundary continues to be made, and determination is performed after each search, until the right boundary is hit or the rise count exceeds the preset number TH**2** of times. That is, when the operation S**227** is completed, the process jumps to the operation S**228**.

[0312] In the operation S**228**, the target read voltage starts to be adjusted to the left.

[0313] In the operation S**229**, in a process of adjusting the target read voltage to the left, it is determined whether the left the boundary or the rise count is hit. For the rise count here, refer to the foregoing operation S**226** for understanding. Thresholds of rise counts on the left and right are usually set to a same value. When the determination result of the operation S**229** is yes, the operation S**231** is performed. When the determination result of the operation S**229** is no, operation S**230** is performed.

[0314] In the operation S**230**, when the left boundary is not hit or the rise count does not exceed the preset number TH**2** of times, a search to the left boundary continues to be made, and determination is performed after each search, until the left boundary is hit or the rise count exceeds the preset number TH**2** of times. That is, when the operation S**230** is completed, the process jumps to the operation S**231**.

[0315] In the operation S**231**, it is determined whether a latest first result is the minimum. Here, whether the latest first result is the minimum, after the target read voltage is adjusted for the last time, a first result at the adjusted target read voltage is the minimum. In this case, all searched points in this cycle at least need to be traversed, to find a adjusted target read voltage corresponding to the minimum point among the first results. When the determination result of the operation S**231** is yes, the operation S**233** is performed. When the determination result of the operation S**231** is no, operation S**232** is performed.

[0316] In the operation S**232**, the latest first result is updated with the found minimum first result. The operation S**233** is performed after the operation S**232**.

[0317] In the operation S**233**, it is determined whether a near-valley count exceeds a preset number TH**3**. Here, taken the minimum first result among multiple corresponding first results at the target read voltages after multiple adjustments as a reference value, and a number of first results with a difference from the reference value being less than a second threshold (equivalent to the foregoing preset difference) in multiple remaining first results is greater than a preset number. The search is stopped, and a target read voltage corresponding to the minimum first result among the multiple first results is taken as the target valley voltage. In some examples, the second threshold (equivalent to the foregoing preset difference) and the preset number may be set together according to an actual case. When the second threshold (equivalent to the foregoing preset difference) is set slightly large, the preset number is usually also relatively large. When the second threshold (equivalent to the foregoing preset difference) is set slightly small, the preset number is usually also relatively small. When the determination result of the operation S**233** is yes, the search is stopped, and the operation S**237** is performed. When the determination result of the operation S**233** is no, a next determination is performed, and operation S**234** is performed.

[0318] In the operation S**234**, it is determined whether a repetitive valley value count exceeds a preset count TH**4**. Here, in a process of making multiple adjustments to the target read voltage, adjustments may be made by employing different adjustment methods, and according to the adjusted target read voltages corresponding to more than a preset number of adjustment methods in the different adjustment methods being same and the corresponding first result at the same target read voltage being the minimum value among all first results, the same target read voltage is taken as the target valley voltage. In some examples, the preset number of times ranges from 2 to 4. In an example, the preset number of times may be 2, 3 or 4. When the determination result of the

operation S**234** is yes, the search is stopped, and the operation S**237** is performed. When the determination result of the operation S**234** is no, a next determination is performed, and operation S**235** is performed.

[0319] It is to be noted that, the operation S**233** and the operation S**234** belong to different determination manners, and positions of the operations are interchangeable. That is, the repetitive valley value count may be first determined, and when the repetitive valley value count does not meet a condition, the near-valley count is determined. It may be understood that, another determination may be performed here to determine whether the cycle ends.

[0320] In the operation S**235**, it is determined whether the cycle ends. When the determination result of the operation S**235** is yes, the operation S**237** is performed. When the determination result of the operation S**235** is no, operation S**236** is performed.

[0321] In the operation S**236**, the process enters a next cycle, to continue to make searches. The process jumps from the operation S**236** to the operation S**209**.

[0322] In the operation S**237**, a search for the target stage is completed, and an adjusted target read voltage corresponding to the minimum first result is taken as the target valley voltage. The operation S**238** is performed after the operation S**237**.

[0323] In the operation S**238**, it is determined whether the target stage is a high stage. When the determination result of the operation S**238** is yes, the operation S**239** is performed. When the determination result of the operation S**238** is no, operation S**240** is performed.

[0324] In the operation S**239**, the predicted valley voltage in the low stage is obtained according to the target valley voltage in the high stage. Here, the predicted valley voltage in the low stage may be obtained through the target valley voltage in the high stage, the stage number in which the low stage is, and the related mapping function (for example, the foregoing fourth mapping function). The operation S**240** is performed after the operation S**239**.

[0325] In operation S**240**, it is determined whether corresponding target valley voltages have been determined for read voltages in all the stages contained on this page. When the determination result in operation S**240** is yes, it indicates that target valley voltages corresponding to read voltages in all the stages contained on this page have been determined, and operation S**242** may be performed at this point; and when the determination result in operation S**240** is no, it indicates that target valley voltages corresponding to read voltages in some of the stages contained on this page have not been determined, and operation S**241** may be performed at this point.

[0326] In operation S**241**, for the stages in which the target valley voltages are not determined, the target valley voltage in each of the stages is determined in sequence. Operation S**236** jumps to operation S**202**.

[0327] In operation S**242**, the process of obtaining the target valley voltage ends. It should be noted that after operation S**242**, the determination of the target valley voltage corresponding to the read voltages in all stages for the next page may be started.

[0328] It should be noted that the methods disclosed in the examples of the present application are able to solve many problems existing in the re-reading operation, but are not used to limit the application scenarios in the examples of the present application, and the methods disclosed in the examples of the present application are also applicable to conventional read operations.

[0329] FIG. **15** is a timing diagram of starting a single-level read mode operation provided in an example of the present application. DQx may represent a data bus signal, and Cycle Type may further represent a type of the data bus signal.

[0330] As shown in FIG. **15**, it is set that a functional command may comprise, for example, one subcommand (for example, EFh). In an example, a memory device starts a single-level read mode when one subcommand EFh is received. In the single-level read mode, the memory device transmits, between received subcommands 00h and 30h, an address ADDR (for example, two column addresses C**1** and C**2** and three row addresses R**1** to R**3**) of data that needs to be read. Within a read time, corresponding data (for example, Dn) in a page of a received address may be

first buffered in a page buffer, and then the data DATA is read as required. It is to be noted that, in the foregoing example, data (for example, Dn) corresponding to one physical page needs to be frequently transmitted (Din/Dout) between the memory device and a memory controller when a read retry operation is performed, and it takes a long time to transmit the data.

[0331] FIG. **16** is a timing diagram of determining a target valley voltage and performing a read operation provided by an example of the present application. As shown in FIG. **16**, a read command may comprise, for example, two subcommands (for example, 00h and 30h). In an example, a memory device transmits, between received subcommands 00h and 30h, an address ADDR (for example, two column addresses C**1** and C**2** and three row addresses R**1** to R**3**) of data that needs to be read. After the memory device receives the subcommand 30h, within a read time, corresponding data DATA (for example, Dn) in a page of a received address may be first buffered in a page buffer, and then the data DATA is read as required. In an example implementation, a memory device **104** transmits, between the received subcommands 00h and 30h, an address ADDR (for example, two column addresses C**1** and C**2** and three row addresses R**1** to R**3**) of data that needs to be read. After receiving the subcommand 30h, the memory device **104** receives subcommands EFh and xxh of a first instruction/a second instruction. The memory device **104** obtains, under instruction by the first instruction/the second instruction, a first result corresponding to a codeword at a corresponding read voltage, and sends the obtained first result to a memory controller. The memory controller determines target valley voltages according to multiple corresponding first results at multiple different read voltages received from the memory device, and performs read operations on data stored in the memory device according to the target valley voltages.

[0332] As shown in FIG. **16**, in some other examples, the first instruction/the second instruction comprises subcommands 05/06h and E0h. In a process of determining a target valley voltage, there are at most only two times of the timing of two subcommands 05/06h and E0h. In an example implementation, one time of the subcommands 05/06h and E0h means that at least one codeword of the memory device is controlled to perform one read operation, and one error correction decoding operation is performed on a read result of the one read operation. In a process of determining a target valley voltage, there are at most only two read operations, so that at most only two error correction decoding operations, and the decoding of the at least one codeword may be implemented through the smallest number (2 at most) of iterations, thereby greatly improving decoding efficiency.

[0333] In some examples, the memory controller **106** is configured to: send the first instruction, wherein the first instruction comprises the subcommands 05/06h and E0h, to instruct the memory device to perform a first read operation. The memory device **104** is configured to: receive the first instruction, and perform the first read operation according to a predicted valley voltage in information representing multiple stages of predicted valley voltages; and send obtained information representing a first read result of the first read operation to the memory controller. The memory controller **106** is further configured to perform a second error correction decoding operation on the first read result of the first read operation.

[0334] In some examples, the memory controller **106** is configured to: output the first read result according to that first error correction decoding succeeds; or, send the second instruction according to that first error correction decoding fails, wherein the second instruction comprises the subcommands 05/06h and E0h, to instruct the memory device to perform a second read operation. The memory device **104** is configured to: receive the second instruction, and perform the second read operation with a predicted valley voltage in re-obtained information representing multiple stages of predicted valley voltages; and send obtained information representing a second read result of the second read operation to the memory controller. The memory controller **106** is further configured to perform a second error correction decoding operation on the second read result of the second read operation. It is to be noted that, the second instruction provided by examples of the

present application is only an example, and should not excessively limit the protection scope of the present application. In some implementations, a data amount of the first result less than a preset data amount threshold. For example, a size of the data amount of the first result ranges from 1 byte to 4 bytes. Therefore, in a process of determining a target valley voltage, a small amount of data is transmitted between the memory device and the memory controller, and a transmission speed is fast, which helps to improve an overall speed of a read operation.

[0335] It is to be noted that, in the examples mentioned in the first part and the second part of the present application, two times of the timing of the subcommands 05/06h and E0h shown in FIG. **16** are not comprised.

[0336] Referring to FIG. **17**, FIG. **17** is a schematic diagram of a structure of a storage medium provided by examples of the present application. In a seventh aspect, examples of the present application provide a storage medium. As shown in FIG. **17**, the storage medium stores executable instructions which, when being executed by a processor, implement any operation in any operation method provided in the fourth aspect, the fifth aspect, and the sixth aspect.

[0337] In some examples, the storage medium may be a Ferromagnetic Random Access Memory (FRAM), a Read Only Memory (ROM), a Programmable Read-Only Memory (PROM), an Erasable Programmable Read-Only Memory (EPROM), an Electrically Erasable Programmable Read-Only Memory (EEPROM), a Flash Memory, a magnetic surface memory, an optical disc, or a Compact Disc Read-Only Memory (CD-ROM) and other memories, or various apparatuses comprising any one or any combination of the above memory devices.

[0338] In some examples, an executable instruction may be compiled in any form of programming language (comprising a compiling or interpreting language, or a declarative or procedural language) by adopting a form of a program, a software, a software module, a script or a code; and it may be deployed in any form, comprising deployed as an independent program or as a module, a component, a subroutine, or other units suitable for use in a computing environment.

[0339] As an example, the executable instruction may, but do not necessarily, correspond to files in a file system, may be stored in part of a file storing other programs or data, for example, stored in one or more scripts in a Hyper Text Markup Language (HTML) document, stored in single file dedicated for the discussed program, or stored in multiple cooperative files (e.g., the file for storing one or more modules, subprograms or code portions).

[0340] As an example, the executable instruction may be deployed on an electronic apparatus for execution, or on multiple electronic apparatuses at one site for execution, or distributed on multiple electronic apparatuses interconnected through a communication network at multiple sites for execution.

[0341] In some examples, with reference to FIG. **17**, FIG. **17** is a schematic diagram of a structure of a storage medium provided by examples of the present application. The storage medium comprises a first storage medium corresponding to a memory device **104**, a second storage medium corresponding to a memory controller **104**, and a third storage medium corresponding to a memory system **102**. When the executable instructions are executed by the memory device, the first storage medium may be configured to implement the operations of the operation method of the memory device in the foregoing examples of the present application. When the executable instructions are executed by the memory controller, the second storage medium may be configured to implement the operations of the operation method of the memory controller in the foregoing examples of the present application. When the executable instructions are executed by the memory system, the third storage medium may be configured to implement the operations of the operation method of the memory system in the foregoing examples of the present application.

[0342] In the memory device and the operation method thereof and the memory system and the operation method thereof provided in the examples of the present application, a first result (a size of the first result may be several bytes) rather than at least one codeword (for example, a size of the codeword may be 4 KB) is transmitted, so that an amount of data transmitted by the memory

device is reduced. A first threshold is obtained according to a corresponding first result at a target read voltage. With the dynamic first threshold, the iterative rapidity of convergence of determining a target valley voltage is higher. A process of obtaining the first result converges inside the memory device, does not occupy, for example, a space of the memory controller, and has low dependency on, for example, the memory controller. At least one of a transmission time at an input/output port of the memory device or a time of an error correction decoding operation of the memory controller is reduced, so that an iterative time of an error correction decoding algorithm of the memory controller is saved, and a speed of error correction decoding is higher. The methods are applicable to a memory device/memory system of an MLC, a TLC type or a QLC type.

[0343] The memory device and the operation method thereof and the memory system and the operation method thereof provided by the examples in the present application can effectively avoid problems of high time consumption and incomplete scenario coverage caused by use of a retry table, and can save a space occupied by the retry table, find a target valley voltage more quickly and accurately, and effectively reduce a delay in determining a target valley voltage. In addition, a read operation is performed with an obtained target valley voltage, so that a probability of correctly reading storage data is greatly increased, thereby improving the reliability and user experience of a product.

[0344] It is to be understood that, references to "one example" or "an example" throughout this specification mean that particular features, structures, or characteristics related to the example are comprised in at least one example of the present application. Therefore, "in one example" or "in an example" presented everywhere throughout this specification does not necessarily refer to the same example. Furthermore, these particular features, structures, or characteristics may be incorporated in one or more examples in any suitable manner. It is to be understood that, in various examples of the present application, sequence numbers of the above processes do not indicate an execution sequence, and an execution sequence of various processes shall be determined by functionalities and intrinsic logics thereof, and shall constitute no limitation on an implementation process of the examples of the present application. The above sequence numbers of the examples of the present application are only for description, and do not represent goodness and badness of the examples.

[0345] The above descriptions are merely preferred implementations of the present application, and not intended to limit the patent scope of the present application. Equivalent structure transformation made within using the contents of the specification and the drawings of the present application under the inventive concept of the present application, or direct/indirect application to other related technical fields are both encompassed within the patent protection scope of the present application.

Claims

1. A memory device, comprising: an array of memory cells comprising multiple memory cells, wherein a preset number of memory cells form one codeword; and peripheral circuit coupled with the array of memory cells and configured to: obtain a first result corresponding to at least one codeword at a target read voltage, wherein the first result comprises the number of bits which represents the number of bits in the at least one codeword which are flipped in two read results at a first read voltage and a second read voltage, and a difference between the first read voltage and the second read voltage is less than a preset voltage; obtain a first threshold according to the corresponding first result at the target read voltage, wherein the first threshold is to represent a corresponding first result at a maximum value in an effective range of predicted valley voltages; make at least one adjustment to the target read voltage, and after each adjustment, obtain a corresponding first result at the adjusted target read voltage; and determine a target valley voltage according to a relationship between a corresponding first result at a target read voltage after one adjustment and the first threshold meeting a first preset condition or according to a corresponding first result at a target read voltage after multiple adjustments meeting a second preset condition,

wherein the target valley voltage is taken as a read voltage at which a read operation is performed on the at least one codeword.

2. The memory device of claim 1, wherein the peripheral circuit is configured to: obtain the first threshold according to the corresponding first result at the target read voltage and a first mapping function, wherein the first mapping function is to represent a relationship between the corresponding first result at the maximum value in the effective range of predicted valley voltages and the corresponding first result at the target read voltage.

3. The memory device of claim 2, wherein the peripheral circuit is configured to: obtain the corresponding first result at the maximum value in the effective range of predicted valley voltages according to an initial value of the corresponding first result at the maximum value in the effective range of predicted valley voltages, a correction value for the corresponding first result at the target read voltage, and a correction coefficient, wherein the initial value of the corresponding first result at the maximum value in the effective range of predicted valley voltages and the correction coefficient are both fixed values related to a stage in which a read voltage is, and the larger the corresponding first result at the target read voltage is, the larger the correction value is.

4. The memory device of claim 1, wherein the first preset condition is that the corresponding first result at the target read voltage after one adjustment is less than the first threshold; and the peripheral circuit is configured to: determine the target read voltage after one adjustment as the target valley voltage according to the relationship between the corresponding first result at the target read voltage after one adjustment and the first threshold meeting the first preset condition.

5. The memory device of claim 4, wherein the peripheral circuit is configured to: obtain, with the corresponding first result at the target read voltage, a target adjustment value for adjusting the target read voltage, according to the corresponding first result at the target read voltage being greater than or equal to the first threshold; obtain a corresponding first result at the adjusted target read voltage with the target adjustment value; determine the adjusted target read voltage with the target adjustment value as the target valley voltage, according to the corresponding first result at the adjusted target read voltage with the target adjustment value being less than the first threshold; and according to the corresponding first result at the adjusted target read voltage with the target adjustment value being greater than or equal to the first threshold, make multiple adjustments to the target read voltage, and after each adjustment, obtain the corresponding first result at the adjusted target read voltage, until the corresponding first result at the adjusted target read voltage is less than the first threshold or the corresponding first result at the target read voltage after multiple adjustments meet the second preset condition.

6. The memory device of claim 1, wherein the second preset condition is that, taken the minimum first result among multiple corresponding first results at the target read voltages after multiple adjustments as a reference value, the number of first results from remaining first results which differ from the reference value with a difference being less than a second threshold is greater than a preset number; and the peripheral circuit is configured to: take a target read voltage corresponding to the minimum first result among the multiple first results as the target valley voltage, according to the corresponding first result at the target read voltage after multiple adjustments meeting the second preset condition.

7. The memory device of claim 1, wherein the peripheral circuit is configured to: in a process of making multiple adjustments to the target read voltage, make adjustments by employing different adjustment methods; and according to the adjusted target read voltages corresponding to more than a preset number of adjustment methods in the different adjustment methods being same and the corresponding first result at the same target read voltage being the minimum value among all first results, take the same target read voltage as the target valley voltage.

8. The memory device of claim 1, wherein the peripheral circuit is configured to: make multiple first adjustments to the target read voltage with a first step size, and obtain corresponding first results at target read voltages after the multiple first adjustments respectively; determine a value of

knee point according to the obtained corresponding first results at the read voltages after the multiple first adjustments, wherein a target read voltage corresponding to the value of knee point is a knee-point voltage; make multiple second adjustments to the knee-point voltage with a second step size, and obtain the corresponding first results at the target read voltages after the multiple second adjustments respectively, wherein the second step size is less than the first step size; and determine the target valley voltage with the obtained corresponding first results at the target read voltages after the multiple second adjustments.

9. The memory device of claim 8, wherein the corresponding first results at the target read voltages after the multiple first adjustments comprise a first adjacent value and a second adjacent value that are adjacent to the value of knee point, and the peripheral circuit is configured to: narrow a range for the multiple second adjustments to be between a target read voltage corresponding to the first adjacent value and the knee-point voltage, according to a difference between the first adjacent value and the value of knee point being less than a difference between the second adjacent value and the value of knee point; and take an average of the read voltage corresponding to the first adjacent value and the knee-point voltage, and according to a corresponding first result at the average being less than the first threshold, take the average as the target valley voltage; and according to the corresponding first result at the average being greater than or equal to the first threshold, continue to make a second adjustment between the read voltage corresponding to the first adjacent value and the knee-point voltage, until a corresponding first result at the adjusted target read voltage is less than the first threshold.

10. The memory device of claim 5, wherein the peripheral circuit is configured to: obtain the predicted valley voltage according to the corresponding first result at the target read voltage and a second mapping function, wherein the second mapping is to represent a relationship between the corresponding first result at the target read voltage and the predicted valley voltage.

11. The memory device of claim 1, wherein the memory cell comprises multiple memory bits, and the multiple memory bits correspond to multiple pages respectively; and at least part of pages correspond to multiple stages, the multiple stages comprise a first stage and a second stage, and a read voltage in the second stage is less than a read voltage in the first stage; and the peripheral circuit is configured to: obtain at least one of a predicted valley voltage in the second stage from the multiple stages or a target valley voltage in other first stage corresponding to a lower read voltage with the determined target valley voltage according to a stage number corresponding to the determined target valley voltage belonging to the first stage.

12. The memory device of claim 1, wherein the peripheral circuit is configured to: read storage data of the at least one codeword at the first read voltage, to obtain a second result; read storage data of the at least one codeword at the second read voltage, to obtain a third result; perform a logical operation on the second result and the third result, to obtain a fourth result; and count the number of bits in the fourth result which represent flip of bits in the third result relative to the second result, to obtain the first result.

13. The memory device of claim 12, wherein the peripheral circuit comprises: a first latch configured to store the second result; a second latch configured to store the third result; and a third latch configured to store the fourth result.

14. A memory system, comprising: one or more memory devices, the memory device comprising: an array of memory cells comprising multiple memory cells, wherein a preset number of memory cells form one codeword; and peripheral circuit coupled with the array of memory cells and configured to: obtain a first result corresponding to at least one codeword at a target read voltage, wherein the first result comprises the number of bits which represents the number of bits in the at least one codeword which are flipped in two read results at a first read voltage and a second read voltage, and a difference between the first read voltage and the second read voltage is less than a preset voltage; obtain a first threshold according to the corresponding first result at the target read voltage, wherein the first threshold is to represent a corresponding first result at a maximum value

in an effective range of predicted valley voltages; make at least one adjustment to the target read voltage, and after each adjustment, obtain a corresponding first result at the adjusted target read voltage; and determine a target valley voltage according to a relationship between a corresponding first result at a target read voltage after one adjustment and the first threshold meeting a first preset condition or according to a corresponding first result at a target read voltage after multiple adjustments meeting a second preset condition, wherein the target valley voltage is taken as a read voltage at which a read operation is performed on the at least one codeword; and a memory controller coupled with the memory device and controlling the memory device.

15. A memory controller, comprising a control component configured to: obtain a first result corresponding to at least one codeword at a target read voltage, wherein the at least one codeword is formed by a preset number of memory cells in an array of memory cells of at least one memory device coupled with the memory controller, wherein the first result comprises the number of bits which represents the number of bits in the at least one codeword which are flipped in two read results at a first read voltage and a second read voltage, and a difference between the first read voltage and the second read voltage is less than a preset voltage; obtain a first threshold according to the corresponding first result at the target read voltage, wherein the first threshold is to represent a corresponding first result at a maximum value in an effective range of predicted valley voltages; make at least one adjustment to the target read voltage, and after each adjustment, obtain a first result corresponding to the at least one codeword at the adjusted target read voltage; and determine a target valley voltage according to a relationship between a corresponding first result at a target read voltage after one adjustment and the first threshold meeting a first preset condition or according to a corresponding first result at a target read voltage after multiple adjustments meeting a second preset condition, wherein the target valley voltage is taken as a read voltage at which a read operation is performed on the at least one codeword.

16. The memory controller of claim 15, wherein the control component is configured to: obtain the first threshold according to the corresponding first result at the target read voltage and a first mapping function, wherein the first mapping function is to represent a relationship between the corresponding first result at the maximum value in the effective range of predicted valley voltages and the corresponding first result at the target read voltage.

17. The memory controller of claim 16, wherein the control component is configured to: obtain the corresponding first result at the maximum value in the effective range of predicted valley voltages, according to an initial value of the corresponding first result at the maximum value in the effective range of predicted valley voltages, a correction value for the corresponding first result at the target read voltage, and a correction coefficient, wherein the initial value of the corresponding first result at the maximum value in the effective range of predicted valley voltages and the correction coefficient are both fixed values related to a stage in which a read voltage is, and the larger the corresponding first result at the target read voltage is, the larger the correction value is.

18. The memory controller of claim 15, wherein the first preset condition is that the corresponding first result at the target read voltage after one adjustment is less than the first threshold; and the control component is configured to: determine the target read voltage after one adjustment as the target valley voltage according to the relationship between the corresponding first result at the target read voltage after one adjustment and the first threshold meeting the first preset condition.

19. The memory controller of claim 18, wherein the control component is configured to: obtain, with the corresponding first result at the target read voltage, a target adjustment value for adjusting the target read voltage, according to the corresponding first result at the target read voltage being greater than or equal to the first threshold; obtain a corresponding first result at the adjusted target read voltage with the target adjustment value; determine the adjusted target read voltage with the target adjustment value as the target valley voltage, according to the corresponding first result at the adjusted target read voltage with the target adjustment value being less than the first threshold; and according to the corresponding first result at the adjusted target read voltage with the target

adjustment value being greater than or equal to the first threshold, make multiple adjustments to the target read voltage, and after each adjustment, obtain the corresponding first result at the adjusted target read voltage, until the corresponding first result at the adjusted target read voltage is less than the first threshold or the corresponding first result at the target read voltage after multiple adjustments meet the second preset condition.

20. The memory controller of claim 15, wherein the second preset condition is that, taken the minimum first result among multiple corresponding first results at the target read voltages after multiple adjustments as a reference value, the number of first results from remaining first results which differ from the reference value with a difference being less than a second threshold is greater than a preset number; and the control component is configured to: take a target read voltage corresponding to the minimum first result among the multiple first results as the target valley voltage, according to the corresponding first result at the target read voltage after multiple adjustments meeting the second preset condition.