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# BACKSIDE PLACEHOLDER ETCH STOP


## Abstract

A semiconductor structure including a first backside dielectric, a second backside dielectric, and an etch stop liner sandwiched between the first backside dielectric and the second backside dielectric.



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## Background/Summary

BACKGROUND

[0001] The present invention generally relates to semiconductor structures, and more particularly to nanosheet transistor structures having a backside placeholder etch stop.

[0002] Complementary Metal-oxide-semiconductor (CMOS) technology is commonly used for

field effect transistors (hereinafter “FET”) as part of advanced integrated circuits (hereinafter “IC”), such as central processing units (hereinafter “CPUs”), memory, storage devices, and the like. As demands to reduce the dimensions of transistor devices continue, nanosheet FETs help achieve a reduced FET device footprint while maintaining FET device performance. A nanosheet FET includes a plurality of stacked nanosheets extending between a pair of source drain epitaxial regions. The device may be a gate-all-around device or transistor in which the gate surrounds a portion of the nanosheet channel. A nanosheet device contains one or more layers of semiconductor channel material portions having a vertical thickness that is substantially less than its width.

SUMMARY

[0003] According to an embodiment of the present invention, a semiconductor structure is provided. The semiconductor structure may include a first backside dielectric, a second backside dielectric, and an etch stop liner sandwiched between the first backside dielectric and the second backside dielectric.

[0004] According to another embodiment of the present invention, a semiconductor structure is provided. The semiconductor structure may include a first backside dielectric, a second backside dielectric, an etch stop liner sandwiched between the first backside dielectric and the second backside dielectric, and a backside contact structure, where the first dielectric directly contacts a first sidewall and a top surface of the backside contact structure.

[0005] According to another embodiment of the present invention, a semiconductor structure is provided. The semiconductor structure may include a first backside dielectric, a second backside dielectric, an etch stop liner sandwiched between the first backside dielectric and the second backside dielectric, and a backside contact structure, where the first dielectric directly contacts a first sidewall and a top surface of the backside contact structure, and where the second dielectric and the etch stop liner directly contact a second sidewall of the backside contact structure.

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## Description

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The following detailed description, given by way of example and not intended to limit the invention solely thereto, will best be appreciated in conjunction with the accompanying drawings, in which:

[0007] FIG. **1**, a top view of a generic structure is shown to provide spatial context to the different cross-sectional views and structural orientations of the semiconductor structures shown in the subsequent figures;

[0008] FIGS. **2** and **3** are cross-sectional views of the semiconductor structure during an intermediate step of a method of fabricating nanosheet transistor structures according to an exemplary embodiment;

[0009] FIGS. **4** and **5** are cross-sectional views of the semiconductor structure after flipping the assembly and recessing the substrate according to an exemplary embodiment;

[0010] FIGS. **6** and **7** are cross-sectional views of the semiconductor structure after removing and recessing remaining portions of the substrate and trimming the placeholders according to an exemplary embodiment;

[0011] FIGS. **8** and **9** are cross-sectional views of the semiconductor structure after forming a dielectric liner according to an exemplary embodiment;

[0012] FIGS. **10** and **11** are cross-sectional views of the semiconductor structure after forming a first backside dielectric according to an exemplary embodiment;

[0013] FIGS. **12** and **13** are cross-sectional views of the semiconductor structure after recessing the first backside dielectric according to an exemplary embodiment;

[0014] FIGS. **14** and **15** are cross-sectional views of the semiconductor structure after removing

exposed portions of the dielectric liner according to an exemplary embodiment;
[0015] FIGS. **16** and **17** are cross-sectional views of the semiconductor structure after forming an etch stop liner according to an exemplary embodiment;
[0016] FIGS. **18** and **19** are cross-sectional views of the semiconductor structure after forming a second backside dielectric according to an exemplary embodiment;
[0017] FIGS. **20** and **21** are cross-sectional views of the semiconductor structure after forming a mask and removing portions of the second backside dielectric to form contact trenches according to an exemplary embodiment;
[0018] FIGS. **22** and **23** are cross-sectional views of the semiconductor structure after removing portions of the etch stop liner and portions of the placeholders according to an exemplary embodiment;
[0019] FIGS. **24** and **25** are cross-sectional views of the semiconductor structure after forming a backside contact structures and backside wiring layers according to an exemplary embodiment; and
[0020] FIGS. **26** and **27** are cross-sectional views of another semiconductor structure during an intermediate step of a method of fabricating a transistor structure according to an alternative exemplary embodiment.
[0021] The drawings are not necessarily to scale. The drawings are merely schematic representations, not intended to portray specific parameters of the invention. For clarity and ease of illustration, scale of elements may be exaggerated. The drawings are intended to depict only typical embodiments of the invention. In the drawings, like numbering represents like elements.

## DETAILED DESCRIPTION

[0022] Detailed embodiments of the claimed structures and methods are disclosed herein; however, it can be understood that the disclosed embodiments are merely illustrative of the claimed structures and methods that may be embodied in various forms. This invention may, however, be embodied in many different forms and should not be construed as limited to the exemplary embodiments set forth herein. In the description, details of well-known features and techniques may be omitted to avoid unnecessarily obscuring the presented embodiments.
[0023] References in the specification to “one embodiment”, “an embodiment”, “an example embodiment”, etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases are not necessarily referring to the same embodiment. Further, when a particular feature, structure, or characteristic is described in connection with an embodiment, it is submitted that it is within the knowledge of one skilled in the art to affect such feature, structure, or characteristic in connection with other embodiments whether or not explicitly described.
[0024] For purposes of the description hereinafter, the terms “upper”, “lower”, “right”, “left”, “vertical”, “horizontal”, “top”, “bottom”, and derivatives thereof shall relate to the disclosed structures and methods, as oriented in the drawing figures. It will be understood that when an element as a layer, region or substrate is referred to as being “on” or “over” another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being “directly on” or “directly over” another element, there are no intervening elements present. It will also be understood that when an element is referred to as being “connected” or “coupled” to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being “directly connected” or “directly coupled” to another element, there are no intervening elements present. Also, the term “sub-lithographic” may refer to a dimension or size less than current dimensions achievable by photolithographic processes, and the term “lithographic” may refer to a dimension or size equal to or greater than current dimensions achievable by photolithographic processes. The sub-lithographic and lithographic dimensions may be determined by a person of ordinary skill in the art at the time the application is filed.

[0025] The terms substantially, substantially similar, about, or any other term denoting functionally equivalent similarities refer to instances in which the difference in length, height, or orientation convey no practical difference between the definite recitation (e.g. the phrase sans the substantially similar term), and the substantially similar variations. In one embodiment, substantial (and its derivatives) denote a difference by a generally accepted engineering or manufacturing tolerance for similar devices, up to, for example, 10% deviation in value or 10° deviation in angle.
[0026] In the interest of not obscuring the presentation of embodiments of the present invention, in the following detailed description, some processing steps or operations that are known in the art may have been combined together for presentation and for illustration purposes and in some instances may have not been described in detail. In other instances, some processing steps or operations that are known in the art may not be described at all. It should be understood that the following description is rather focused on the distinctive features or elements of various embodiments of the present invention.
[0027] Complementary field effect transistors, including gate-all-around transistor devices and nanosheet transistor devices, have known advantages over conventional transistor structures in terms of density, performance, power consumption, and integration. However, backside fabrication presents unique challenges. More specifically, for example, conventional backside arrangements and fabrication techniques do not use an etch stop. Without an etch stop, various backside etching techniques have the potential to extend deeper than intended and damage exiting front-end-of-line components. Such damage could result in electrical short being formed between backside contact structures and gates in the front-end-of-line.
[0028] The present invention generally relates to semiconductor structures, and more particularly to nanosheet transistor structures having a backside placeholder etch stop. More specifically, the nanosheet transistor structures and associated method disclosed herein enable a novel solution for providing nanosheet transistor structures having a backside etch stop. Exemplary embodiments of nanosheet transistor structures having a backside etch stop are described in detail below by referring to the accompanying drawings in FIGS. **1** to **27**. Those skilled in the art will readily appreciate that the detailed description given herein with respect to these figures is for explanatory purposes as the invention extends beyond these limited embodiments.
[0029] Referring now to FIG. **1**, a top view of a generic structure is shown to provide spatial context to the different cross-sectional views and structural orientations of the semiconductor structures shown in the figures and described below. Additionally, XYZ Cartesian coordinates may be also shown in each of the drawings to provide additional spatial context. The terms “vertical” or “vertical direction” or “vertical height” as used herein denote a Z-direction of the Cartesian coordinates shown in the drawings, and the terms “horizontal,” or “horizontal direction,” or “lateral direction” as used herein denote an X-direction and/or a Y-direction of the Cartesian coordinates shown in the drawings.
[0030] The generic structure illustrated in FIG. **1** shows multiple fins/stacks and multiple gate regions situated perpendicular to one another. FIGS. **1**-**27** represent cross section views oriented as indicated in FIG. **1**
[0031] Referring now to FIGS. **2** and **3**, a structure **100** is shown during an intermediate step of a method of fabricating a nanosheet transistor structure according to an embodiment of the invention. FIG. **2** depicts a cross-sectional view of the structure **100** shown in FIG. **3** taken along line X-X and FIG. **3** depicts a cross-sectional view of the structure **100** shown in FIG. **2** taken along line Y-Y.
[0032] The structure **100** illustrated in FIGS. **2**-**3** includes an array of nanosheet transistors formed on a substrate **102** in accordance with known techniques. As illustrated, the array of nanosheet transistors includes nanosheet stacks **104**. Each nanosheet stack **104** includes a plurality of silicon channels **106** surrounded by a single gate **108**. For purposes of orientation, the substrate **102** is herein referred to as being on a “backside” of the structure **100** and the array of nanosheet transistors are herein referred to as being on a “frontside” of the structure **100**. Further, certain

features may be described herein as having a relative position with respect to the frontside or backside of the structure **100**.

[0033] The substrate **102** may be a layered semiconductor such as a silicon-on-insulator or SiGe-on-insulator, where an etch stop layer **110** separates a base substrate **112** from a top semiconductor layer **114**. Unlike conventional layered semiconductor substrates, the etch stop layer **110** of the substrate **102** may include any material which affects the desired etch selectivity during subsequent processing. For example, the etch stop layer **110** may be a conventional buried oxide layer, or it may be a silicon germanium layer with a specific germanium concentration. In practice, the etch stop layer **110** will function as an etch stop layer and can be composed of any material which supports that function.

[0034] In the present embodiment, both the base substrate **112** and the top semiconductor layer **114** may be any bulk substrate made from any of several known semiconductor materials such as, for example, silicon, germanium, silicon-germanium alloy, and compound (e.g. III-V and II-VI) semiconductor materials. For example, both the base substrate **112** and the top semiconductor layer **114** may be made from silicon.

[0035] The structure **100** further includes placeholders **116**, buffer layers **118**, and source drain regions **120** generally arranged between adjacent nanosheet stacks **104**, as illustrated.

[0036] The placeholders **116** are formed by filling self-aligned openings in the top semiconductor layer **114** between adjacent nanosheet stacks **104** with a sacrificial material according to known techniques. Specifically, after filling, the sacrificial material is recessed to create the placeholders **116** according to known techniques. In an embodiment, the sacrificial material is silicon germanium or amorphous silicon epitaxially grown from the surfaces of the top semiconductor layer **114**. In another embodiment, the sacrificial material is SiC, SiOC deposited using, for example, chemical vapor deposition (CVD) or plasma enhanced CVD (PECVD) and subsequently recessed using, for example, reactive ion etching (RIE). Other suitable deposition and recessing techniques may be used provided they do not induce a physical or chemical change to the silicon channels **106**.

[0037] The buffer layers **118** are formed above the placeholders **116** according to known techniques. Specifically, buffer layers **118** include an etch stop material formed directly above the placeholders **116**. In an embodiment, the etch stop material can be any silicon-based material suitable to provide desired etch stop properties during backside processing. For example, the buffer layers **118** are designed to allow the subsequent removal of the placeholders **116** selective to the source drain regions **120**.

[0038] The source drain regions **120** are formed on top of the buffer layer **118** according to known techniques. Specifically, the source drain regions **120** are disposed between adjacent nanosheet stacks **104** in direct contact with exposed ends of the silicon channels **106**. More specifically, the source drain regions **120** may be epitaxially grown from the exposed ends of the silicon channels **106** according to known techniques.

[0039] The structure **100** further includes shallow trench isolation regions (hereinafter “STI regions”) which extend partially into the substrate **102** below the array of nanosheet transistors. In general, the STI regions may each include an isolation liner **122** and an isolation fill **124**. For example, the isolation liner **122** is SiN, SiON, or SiOCN, and the isolation fill **124** is silicon oxide (SiO) or silicon nitride (SiN).

[0040] The structure **100** further includes stack spacers **126**, inner spacers **128**, and gate spacers **130**.

[0041] The stack spacers **126** are disposed directly beneath the nanosheet stacks **104** separating them from the substrate **102**. Specifically, for example, a relatively thin layer of silicon nitride is conformally deposited prior to forming the nanosheet stacks **104**. In some embodiments, for example, the stack spacers **126** may be composed of SiN, SiBCN, SiOCN, SiOC, or any other combination of low-k materials. Like the buffer layers **118**, the stack spacers **126** can provide

desired etch selectivity during backside processing.
[0042] As used herein, “conformal” it is meant that a material layer has a continuous thickness, or substantially continuous thickness. For example, a continuous thickness generally means a first thickness as measured from a bottom surface to a topmost surface that is the same as a second thickness as measured from an inner sidewall surface to an outer sidewall surface.
[0043] The inner spacers **128** are disposed between alternate channels (**106**), and laterally separate the gates **108** from the source drain regions **120**, as illustrated. The inner spacers **128** provide necessary electrical insulation between the gates **108** and the source drain regions **120**.
[0044] The gate spacers **130** are added to define the channel length and the source drain regions, and ultimately electrically insulate the gates **108** from subsequently formed structures, such as, for example, source drain contact structures. The gate spacers **130** are critical for electrically insulating the gates **108** from the source drain regions **120** or subsequently formed contact structures. In at least one embodiment, the gate spacers **130** include silicon nitride, silicon boron nitride, silicon carbon nitride, silicon boron carbon nitride, or other known equivalents.
[0045] Finally, the structure **100** further includes a dielectric layer **132** directly above and surrounding the source drain regions **120**. The dielectric layer **132** is composed of any suitable interlayer dielectric material, such as, for example, oxides such as silicon oxide (SiO.sub.x), nitrides such as silicon nitride (Si.sub.xN.sub.y), and/or low-K materials such as SiCOH or SiBCN. In another embodiment, is composed of silicon dioxide, undoped silicate glass (USG), fluorosilicate glass (FSG), borophosphosilicate glass (BPSG), a spin-on low-k dielectric layer, a chemical vapor deposition (CVD) low-k dielectric layer or any combination thereof. In yet another embodiment, a self-planarizing material such as a spin-on glass (SOG) or a spin-on low-k dielectric material such as SiLK™ can be used to form the dielectric layer **132**. Using a self-planarizing dielectric material as the dielectric layer **132** can avoid the need to perform a subsequent planarizing step. After formation, top surfaces of the dielectric layer **132** are typically made flush, or substantially flush, with top surfaces of the gates **108** and the gate spacers **130** by chemical mechanical polishing techniques.
[0046] The structure **100** further includes a middle-of-line **134**, a back-end-of-line **136**, a carrier wafer **138**.
[0047] The middle-of-line **134** includes source drain contacts **140** and gate contacts (not shown) which may be generally referred to as middle-of-line contacts. The source drain contacts **140** and the gate contacts are formed according to known techniques. The back-end-of-line **136** may include vias and metal lines which may be generally referred to as back-end-of-line interconnects. The vias and the metal lines are formed according to known techniques. Finally, the carrier wafer **138** is secured to a top of the structure **100** according to an embodiment of the invention. The carrier wafer **138** is attached, or removably secured, to the back-end-of-line **136**. In general, and not depicted, the carrier wafer **138** may be thicker than the other layers. Temporarily bonding the structure **100** to a thicker carrier provides improved handling and additional support for backside processing of thin wafers. After backside processing described below, the structure **100** may be de-bonded, or removed, from the carrier wafer **138** according to known techniques.
[0048] Although only a limited number of components, devices, or structures are shown and described, embodiments of the present invention shall not be limited by any quantity otherwise illustrated or discussed herein.
[0049] Referring now to FIGS. **4** and **5**, the structure **100** is shown after flipping the assembly and recessing the substrate **102** according to an embodiment of the invention. FIG. **4** depicts a cross-sectional view of the structure **100** shown in FIG. **5** taken along line X-X and FIG. **5** depicts a cross-sectional view of the structure **100** shown in FIG. **4** taken along line Y-Y.
[0050] First, the structure **100** is flipped 180 degrees to prepare for backside processing. In general, backside processing includes fabrication or processing of the structure **100** opposite the active device and wiring layers. Next, the substrate **102** is recessed according to known techniques.

Specifically, the base substrate **112** is recessed or completely removed to expose the etch stop layer **110**, as shown. It is noted, the orientation of the cross-sectional views referenced and illustrated hereafter will remain unchanged despite the actualities of flipping of the structure **100** for purposes of fabrication. As such, all references to “upper”, “lower”, “right”, “left”, “vertical”, “horizontal”, “top”, “bottom”, and derivatives thereof shall continue to relate to the disclosed structures and methods, as oriented in the drawing figures.

[0051] Referring now to FIGS. **6** and **7**, the structure **100** is shown after removing and recessing remaining portions of the substrate **102** and trimming the placeholders **116** according to an embodiment of the invention. FIG. **6** depicts a cross-sectional view of the structure **100** shown in FIG. **7** taken along line X-X and FIG. **7** depicts a cross-sectional view of the structure **100** shown in FIG. **6** taken along line Y-Y.

[0052] First, the etch stop layer **110** is selectively removed and the top semiconductor layer **114** is recessed according to known techniques. Specifically, the etch stop layer **110** is removed selective to the top semiconductor layer **114** and the top semiconductor layer **114** is removed selective to the placeholders **116**, the stack spacers **126**, the gates **108**, and the STI regions, as illustrated. As indicated in the figures, some erosion of the placeholders **116** is anticipated to be an unintended consequence resulting from selectively removing the top semiconductor layer **114**. Such erosion would normally lead to smaller backside contacts using conventional fabrication techniques. For example, if the eroded placeholders **116** are removed and replaced with the contact material, the resulting backside contact structure will mimic the eroded shape and size of the placeholders **116** which causes undesirable increases in resistance.

[0053] Referring now to FIGS. **8** and **9**, the structure **100** is shown after forming a dielectric liner **142** according to an embodiment of the invention. FIG. **8** depicts a cross-sectional view of the structure **100** shown in FIG. **9** taken along line X-X and FIG. **9** depicts a cross-sectional view of the structure **100** shown in FIG. **8** taken along line Y-Y.

[0054] First, the dielectric liner **142** is formed across the backside of the structure **100** according to known techniques. Specifically, a liner material is conformally deposited across exposed surfaces on the backside of the structure **100** including directly on the placeholders **116** and the stack spacers **126** (see FIG. **8**) and within the openings between STI regions (see FIG. **9**), as illustrated. In some embodiments, for example, the dielectric liner **142** may be composed of low-k materials, such as, for example, SiN, SiBCN, SiOCN, SiOC, or other combinations thereof. According to embodiments of the present invention, the dielectric liner **142** provides added etch selectivity during backside processing. More specifically, the dielectric liner **142** is made from a material which may be removed selective to the placeholders **116**, as described below.

[0055] Referring now to FIGS. **10** and **11**, the structure **100** is shown after forming a first backside dielectric **144** according to an embodiment of the invention. FIG. **10** depicts a cross-sectional view of the structure **100** shown in FIG. **11** taken along line X-X and FIG. **11** depicts a cross-sectional view of the structure **100** shown in FIG. **10** taken along line Y-Y.

[0056] The first backside dielectric **144** is deposited according to known techniques. Specifically, a first backside dielectric material is blanket deposited across the structure **100**. The first backside dielectric **144** completely covers the dielectric liner **142**. After deposition, known chemical mechanical polishing may be used to remove excess portions of the backside dielectric material from bottom surfaces of the structure **100**.

[0057] Referring now to FIGS. **12** and **13**, the structure **100** is shown after recessing the first backside dielectric **144** according to an embodiment of the invention. FIG. **12** depicts a cross-sectional view of the structure **100** shown in FIG. **13** taken along line X-X and FIG. **13** depicts a cross-sectional view of the structure **100** shown in FIG. **12** taken along line Y-Y.

[0058] First, the first backside dielectric **144** is recessed according to known techniques. Specifically, the first backside dielectric **144** is recessed selective to the dielectric liner **142**. According to embodiments of the present invention, the first backside dielectric **144** is recessed to a

depth sufficient to expose an entirety of the dielectric liner **142** in Section Y-Y without exposing an entirety of the dielectric liner **142** in Section X-X. Controlling, or adjusting, the depth at which the first backside dielectric **144** is recessed directly influences the volume of a subsequently formed backside contact structure, as discussed in greater detail below.

[0059] Referring now to FIGS. **14** and **15**, the structure **100** is shown after removing exposed portions of the dielectric liner **142** according to an embodiment of the invention. FIG. **14** depicts a cross-sectional view of the structure **100** shown in FIG. **15** taken along line X-X and FIG. **15** depicts a cross-sectional view of the structure **100** shown in FIG. **14** taken along line Y-Y.

[0060] Exposed portions of the dielectric liner **142** are selectively removed according to known techniques. Specifically, exposed portions of the dielectric liner **142** are removed using known etching techniques suitable to remove silicon-based materials selective to the first backside dielectric **144** and the placeholders **116**. In an embodiment, the exposed portions of the dielectric liner **142** are removed using an anisotropic etch such as, for example, reactive ion etching. After removing the exposed portions of the dielectric liner **142**, bottom portions of the placeholders **116** are exposed, as illustrated.

[0061] Referring now to FIGS. **16** and **17**, the structure **100** is shown after forming an etch stop liner **146** according to an embodiment of the invention. FIG. **16** depicts a cross-sectional view of the structure **100** shown in FIG. **17** taken along line X-X and FIG. **17** depicts a cross-sectional view of the structure **100** shown in FIG. **16** taken along line Y-Y.

[0062] First, the etch stop liner **146** is formed across the backside of the structure **100** according to known techniques. Specifically, an etch stop material is conformally deposited across exposed surfaces on the backside of the structure **100** including directly on exposed portions of the placeholders **116** and within the openings between STI regions (see FIG. **17**), as illustrated. In some embodiments, for example, the etch stop liner **146** may be composed of known etch stop materials, such as, for example, aluminum nitride, SiCOH, aSi, SiNCH, or other combinations thereof.

[0063] Referring now to FIGS. **18** and **19**, the structure **100** is shown after forming a second backside dielectric **148** according to an embodiment of the invention. FIG. **18** depicts a cross-sectional view of the structure **100** shown in FIG. **19** taken along line X-X and FIG. **19** depicts a cross-sectional view of the structure **100** shown in FIG. **18** taken along line Y-Y.

[0064] The second backside dielectric **148** is deposited according to known techniques. Specifically, a second backside dielectric material is blanket deposited across the structure **100**. The second backside dielectric **148** completely covers the etch stop liner **146**. After deposition, known chemical mechanical polishing may be used to remove excess portions of the second backside dielectric material from bottom surfaces of the structure **100**. According to at least one embodiment, the second backside dielectric material is the same as the first backside dielectric material. According to at least another embodiment, the second backside dielectric material is a different material than the first backside dielectric material.

[0065] Referring now to FIGS. **20** and **21**, the structure **100** is shown after forming a mask **150** and removing portions of the second backside dielectric **148** to form contact trenches **152** according to an embodiment of the invention. FIG. **20** depicts a cross-sectional view of the structure **100** shown in FIG. **21** taken along line X-X and FIG. **21** depicts a cross-sectional view of the structure **100** shown in FIG. **20** taken along line Y-Y.

[0066] First, the mask **150** is deposited and subsequently patterned to expose certain portions of the structure **100** according to known techniques. The mask **150** can be an organic planarization layer (OPL) or a layer of material that is capable of being planarized or etched by known techniques. In an embodiment, for example, the mask **150** can be an amorphous carbon layer able to withstand subsequent processing temperatures. The mask **150** can preferably have a thickness sufficient to cover existing structures. After depositing the mask **150**, a dry etching technique is applied to pattern or recess the mask **150** according to known techniques. The mask **150** is patterned

consistent with a size and a location of subsequently formed backside contact structures. For example, after patterning the mask **150**, portions of the structure **100** in contact regions are exposed, as illustrated. Specific to the embodiments disclosed herein, the mask **150** is patterned selective to the second backside dielectric **148**.

[0067] Exposed portions of the second backside dielectric **148** are then selectively removed to form the contact trenches **152** according to known techniques. Specifically, exposed portions of the second backside dielectric **148** are removed using known etching techniques suitable to remove dielectric materials selective to the mask **150** and the etch stop liner **146**, as illustrated. In an embodiment, the exposed portions of the second backside dielectric **148** are removed using an anisotropic etch such as, for example, reactive ion etching. After removing the exposed portions of the second backside dielectric **148**, portions of the etch stop liner **146** are exposed, as illustrated. Significant to the embodiments disclosed herein, etching stops on the etch stop liner **146**. Over-etching the backside dielectrics is possible without the etch stop liner **146**. Such over-etching increases the risk for shorting between the gate **108** and the source drain regions **120**. Over-etch can also cause subsequently formed backside contact structures to have variable sizes and volumes, when uniform size and volume is more desirable to produce more consistent electrical characteristics.

[0068] Referring now to FIGS. **22** and **23**, the structure **100** is shown after removing portions of the etch stop liner **146** and portions of the placeholders **116** according to an embodiment of the invention. FIG. **22** depicts a cross-sectional view of the structure **100** shown in FIG. **23** taken along line X-X and FIG. **23** depicts a cross-sectional view of the structure **100** shown in FIG. **22** taken along line Y-Y.

[0069] First, the portions of the etch stop liner **146** exposed within the contact trenches **152** are selectively removed according to known techniques. Specifically, the portions of the etch stop liner **146** exposed within the contact trenches **152** are etched or removed selective to the second backside dielectric **148**, the first backside dielectric **144**, the STI regions, and the placeholders **116**. The portions of the etch stop liner **146** exposed within the contact trenches **152** can be removed using compatible selective dry etching techniques. After etching, other portions of the etch stop liner **146** remain sandwiched between the first backside dielectric **144** and the second backside dielectric **148**, as illustrated.

[0070] Next, the placeholders **116** exposed after removing portions of the etch stop liner **146** are selectively removed according to known techniques. Specifically, the placeholders **116** are etched or removed selective to the first backside dielectric **148**, the STI regions, the dielectric liner **142**, and the buffer layer **118**. The placeholders **116** can be removed using compatible selective dry etching techniques.

[0071] In doing so, the backside contact trenches **152** are enlarged directly beneath the source drain regions **120** without exposing the source drain regions **120** due to the existence of the buffer layers **118**. Finally, exposed buffer layers **118** are subsequently removed selective to the surrounding structures according to known techniques. In some cases, some gouging or recessing of the source drain regions **120** may occur, as illustrated.

[0072] In the present embodiment, portions of the dielectric liner **142** are not removed and remain along sidewall portions of the backside contact trenches **152**, as illustrated. As such, according to embodiments, a lateral width of middle portions of the backside contact trenches **152**, measured in the x-direction, will be smaller than lateral widths of corresponding top and bottom portions of the same backside contact trench.

[0073] Referring now to FIGS. **24** and **25**, the structure **100** is shown after forming a backside contact structures **154** and backside wiring layers **156** according to an embodiment of the invention. FIG. **24** depicts a cross-sectional view of the structure **100** shown in FIG. **25** taken along line X-X and FIG. **25** depicts a cross-sectional view of the structure **100** shown in FIG. **24** taken along line Y-Y.

[0074] Next, the backside contact trenches **152** are filled with a conductive material to form the backside contact structures **154** according to known techniques. The backside contact structures **154** may include any suitable conductive material, such as, for example, copper, ruthenium, aluminum, tungsten, cobalt, or alloys thereof. In some embodiments, a metal silicide is formed at the bottom of the backside contact trenches prior to filling them with the conductive material.
[0075] After, excess conductive material can be polished using known techniques until bottommost surfaces of the backside contact structures **154** are flush, or substantially flush, with bottommost surfaces of the second backside dielectric **148**, as illustrated. After polishing, bottommost surfaces of the backside contact structures **154** are substantially flat. It is noted, the backside contact structures **154** may include, for example, backside source drain contacts, as illustrated, as well as backside gate contacts (not shown).
[0076] After forming the backside contact structures **154**, the backside wiring layers **156** are subsequently formed according to known techniques. The backside wiring layers **156** typically include at least backside power rails **158** and a backside power delivery network **160**.
[0077] According to the embodiment illustrated in FIGS. **24** and **25**, the nanosheet transistor structures represented by the structure **100** have some distinctive and notable features. For instance, the structure **100** includes the etch stop liner **146** sandwiched between the first backside dielectric **144** and the second backside dielectric **148**. The etch stop liner **146** enables the formation of constant height backside contact structures (**154**). Without the etch stop liner **146**, a height (H.sub.1) of respective backside contact structures (**154**) will depend on feature size as a result of the wet etching techniques used to create the contact trenches **152** (See FIGS. **22** and **23**). The ability to control depth of the contact trenches **152** and the resulting height (H.sub.1) of the backside contact structures (**154**) using the etch stop liner **146** further limits the risk of over-etching the backside dielectrics, and further limits the risk for shorting between the gate **108** and the source drain regions **120**. As previously indicated, a volume of the bottom portion of the backside contact structures **154** can be controlled by the depth at which the first backside dielectric **144** is recessed (see FIGS. **12** and **13**), which in turn dictates location of the etch stop liner **146**.
[0078] In all cases, a topmost surface of the backside contact structures **154** is above a topmost surface of the placeholders **116**, as illustrated. Further, according to embodiments, a lateral width of middle portions of the backside contact structures **154**, measured in the x-direction, will be smaller than lateral widths of corresponding top and bottom portions of the same backside contact structure. Even further, the backside contact structures **154** have a surface which is substantially parallel with at least one surface of the etch stop liner **146**, as illustrated in FIG. **24**. Said differently, a topmost surface of the bottom portion of the backside contact structures **154** is substantially parallel with at least one surface of the etch stop liner **146**.
[0079] With continued reference to FIGS. **24** and **25**, and according to an embodiment, the structure **100** includes a first backside dielectric, a second backside dielectric, and an etch stop liner sandwiched between the first backside dielectric and the second backside dielectric.
[0080] With continued reference to FIGS. **24** and **25**, and according to an embodiment, the structure further includes a backside contact structure, where a surface of the backside contact structure is substantially parallel with at least one surface of the etch stop liner.
[0081] With continued reference to FIGS. **24** and **25**, and according to an embodiment, the structure further includes a placeholder directly beneath a source drain region, where a lower portion of the placeholder is surrounded by the etch stop liner, and where an upper portion of the placeholder is at least partially surrounded by a dielectric liner.
[0082] With continued reference to FIGS. **24** and **25**, and according to an embodiment, the structure further includes a dielectric liner partially surrounding sidewalls of a top portion of a placeholder.
[0083] With continued reference to FIGS. **24** and **25**, and according to an embodiment, the structure further includes a dielectric liner partially surrounding sidewalls of a middle portion of a

backside contact structure.
[0084] With continued reference to FIGS. **24** and **25**, and according to an embodiment, the etch stop liner is further disposed along sidewalls and bottoms of shallow trench isolation regions.
[0085] With continued reference to FIGS. **24** and **25**, and according to an embodiment, the first backside dielectric is arranged between and physically separates a first portion of the etch stop liner from a first portion of a dielectric liner, and where a second portion of the etch stop liner directly contacts a second portion of a dielectric liner.
[0086] With continued reference to FIGS. **24** and **25**, and according to an embodiment, the structure **100** includes a first backside dielectric, a second backside dielectric, an etch stop liner sandwiched between the first backside dielectric and the second backside dielectric, and a backside contact structure, where the first dielectric directly contacts a first sidewall and a top surface of the backside contact structure.
[0087] With continued reference to FIGS. **24** and **25**, and according to an embodiment, the structure **100** includes a first backside dielectric, a second backside dielectric, an etch stop liner sandwiched between the first backside dielectric and the second backside dielectric, and a backside contact structure, where the first dielectric directly contacts a first sidewall and a top surface of the backside contact structure, and where the second dielectric and the etch stop liner directly contact a second sidewall of the backside contact structure.
[0088] Referring now to FIGS. **26** and **27**, a structure **200** is shown during an intermediate step of a method of fabricating a transistor structure according to an alternative embodiment of the invention. Similar to the views presented and described above with respect to the structure **100**, FIG. **26** depicts a cross-sectional view of the structure **200** shown in FIG. **27** taken along line X-X and FIG. **27** depicts a cross-sectional view of the structure **200** shown in FIG. **24** taken along line Y-Y.
[0089] The structure **200** is substantially similar to the structure **100** described above and is produced by a similar process flow described above with respect to the structure **100** except for the following differences. The structure **200** of FIGS. **26** and **27** represents the resulting structure when an additional etch is used to remove sidewall portions of the dielectric liner **142** following the processing described above and illustrated in FIGS. **22** and **23**.
[0090] Specifically, the sidewall portions of the dielectric liner **142** exposed within the contact trenches **152** are selectively removed according to known techniques. Specifically, the sidewall portions of the dielectric liner **142** exposed within the contact trenches **152** are etched or removed selective to the second backside dielectric **148**, the first backside dielectric **144**, the STI regions, and the placeholders **116**. The sidewall portions of the dielectric liner **142** exposed within the contact trenches **152** can be removed using compatible selective dry etching techniques. After etching other portions of the dielectric liner **142** remain sandwiched between the first backside dielectric **144** and the stack spacers **126**, as illustrated.
[0091] According to the embodiment illustrated in FIGS. **26** and **27**, the nanosheet transistor structures represented by the structure **200** have similar distinctive notable features as those described above with respect to the structure **100**.
[0092] The descriptions of the various embodiments of the present invention have been presented for purposes of illustration, but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope and spirit of the invention. The terminology used herein was chosen to best explain the principles of the embodiment, the practical application or technical improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments disclosed herein.

## Claims

**1**. A semiconductor structure comprising: a first backside dielectric; a second backside dielectric; and an etch stop liner sandwiched between the first backside dielectric and the second backside dielectric.
**2**. The semiconductor structure according to claim 1, further comprising: a backside contact structure, wherein a surface of the backside contact structure is substantially parallel with at least one surface of the etch stop liner.
**3**. The semiconductor structure according to claim 1, further comprising: a placeholder directly beneath a source drain region, wherein a lower portion of the placeholder is surrounded by the etch stop liner, and wherein an upper portion of the placeholder is at least partially surrounded by a dielectric liner.
**4**. The semiconductor structure according to claim 1, further comprising: a dielectric liner partially surrounding sidewalls of a top portion of a placeholder.
**5**. The semiconductor structure according to claim 1, further comprising: a dielectric liner partially surrounding sidewalls of a middle portion of a backside contact structure.
**6**. The semiconductor structure according to claim 1, wherein the etch stop liner is further disposed along sidewalls and bottoms of shallow trench isolation regions.
**7**. The semiconductor structure according to claim 1, wherein the first backside dielectric is arranged between and physically separates a first portion of the etch stop liner from a first portion of a dielectric liner, and wherein a second portion of the etch stop liner directly contacts a second portion of a dielectric liner.
**8**. A semiconductor structure comprising: a first backside dielectric; a second backside dielectric; an etch stop liner sandwiched between the first backside dielectric and the second backside dielectric; and a backside contact structure, wherein the first dielectric directly contacts a first sidewall and a top surface of the backside contact structure.
**9**. The semiconductor structure according to claim 8, wherein a top surface of the backside contact structure is substantially parallel with at least one surface of the etch stop liner.
**10**. The semiconductor structure according to claim 8, further comprising: a placeholder directly beneath a source drain region, wherein a lower portion of the placeholder is surrounded by the etch stop liner, and wherein an upper portion of the placeholder is at least partially surrounded by a dielectric liner.
**11**. The semiconductor structure according to claim 8, further comprising: a dielectric liner partially surrounding sidewalls of a top portion of a placeholder.
**12**. The semiconductor structure according to claim 8, further comprising: a dielectric liner partially surrounding sidewalls of a middle portion of a backside contact structure.
**13**. The semiconductor structure according to claim 8, wherein the etch stop liner is further disposed along sidewalls and bottoms of shallow trench isolation regions.
**14**. The semiconductor structure according to claim 8, wherein the first backside dielectric is arranged between and physically separates a first portion of the etch stop liner from a first portion of a dielectric liner, and wherein a second portion of the etch stop liner directly contacts a second portion of a dielectric liner.
**15**. A semiconductor structure comprising: a first backside dielectric; a second backside dielectric; an etch stop liner sandwiched between the first backside dielectric and the second backside dielectric; and a backside contact structure, wherein the first dielectric directly contacts a first sidewall and a top surface of the backside contact structure, and wherein the second dielectric and the etch stop liner directly contact a second sidewall of the backside contact structure.
**16**. The semiconductor structure according to claim 15, wherein a top surface of the backside contact structure is substantially parallel with at least one surface of the etch stop liner.
**17**. The semiconductor structure according to claim 15, further comprising: a placeholder directly beneath a source drain region, wherein a lower portion of the placeholder is surrounded by the etch

stop liner, and wherein an upper portion of the placeholder is at least partially surrounded by a dielectric liner.

**18**. The semiconductor structure according to claim 15, further comprising: a dielectric liner partially surrounding sidewalls of a middle portion of a backside contact structure.

**19**. The semiconductor structure according to claim 15, wherein the etch stop liner is further disposed along sidewalls and bottoms of shallow trench isolation regions.

**20**. The semiconductor structure according to claim 15, wherein the first backside dielectric is arranged between and physically separates a first portion of the etch stop liner from a first portion of a dielectric liner, and wherein a second portion of the etch stop liner directly contacts a second portion of a dielectric liner.