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Control circuit, control method and electronic device

Abstract

A control circuit including a storage circuit, a voltage detection circuit, a processing circuit, and a wake-up circuit is provided. The storage circuit includes a register and stores a program code. The voltage detection circuit detects an external voltage. The processing circuit accesses the register in response to the external voltage reaching a first predetermined voltage. The processing circuit enters a power-down mode in response to the external voltage reaching a second predetermined voltage. In the power-down mode, the processing circuit stops accessing the register. The wake-up circuit determines whether a wake-up event occurs. In response to the wake-up event, the wake-up circuit directs the processing circuit to exit the power-down mode and enter an operation mode. In response to there being no wake-up event, the processing circuit stays in the power-down mode. In the operation mode, the processing circuit executes the program code.

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References Cited

U.S. PATENT DOCUMENTS

Patent No.	Issued Date	Patentee Name	U.S. Cl.	CPC
6360327	12/2001	Hobson	713/320	G06F 1/3203

FOREIGN PATENT DOCUMENTS

Patent No.	Application Date	Country	CPC
I564703	12/2016	TW	N/A
201942718	12/2018	TW	N/A
202134810	12/2020	TW	N/A
202227835	12/2021	TW	G01R 19/165

OTHER PUBLICATIONS

TW Office Action issued on Jun. 30, 2023, for the corresponding Taiwan Application No. 111132637, 7 pages. cited by applicant

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Background/Summary

CROSS REFERENCE TO RELATED APPLICATIONS
(1) This application claims priority of Taiwan Patent Application No. 111132637, filed on Aug. 30, 2022, the entirety of which is incorporated by reference herein.
BACKGROUND OF THE INVENTION
Field of the Invention
(2) The invention relates to a control circuit, and more particularly to a control circuit that can improve power storage capacity.
Description of the Related Art
(3) A conventional control circuit receives external voltage and operates according to said external voltage. When the control circuit starts to run a program, the external voltage will gradually drop

due to the power consumption caused by the operation of control circuit. When the external voltage is lower than a low-voltage reset (LVR) voltage, the control circuit is reset. After resetting the control circuit, the external voltage is gradually increased. However, when the control circuit runs the program again, the external voltage drops again. When the external voltage is lower than the LVR voltage, the control circuit is reset again. Since the control circuit is repeatedly reset, it cannot complete the booting action quickly.

BRIEF SUMMARY OF THE INVENTION

(4) In accordance with an embodiment of the disclosure, a control circuit comprises a storage circuit, a voltage detection circuit, a processing circuit, and a wake-up circuit. The storage circuit comprises a register and stores a program code. The voltage detection circuit detects an external voltage. The processing circuit accesses the register in response to the external voltage reaching a first predetermined voltage. The processing circuit enters a power-down mode in response to the external voltage reaching a second predetermined voltage. In the power-down mode, the processing circuit stops accessing the register. The wake-up circuit determines whether a wake-up event occurs. In response to the wake-up event, the wake-up circuit directs the processing circuit to exit the power-down mode and enter an operation mode. In response to there being no wake-up event, the processing circuit stays in the power-down mode. In the operation mode, the processing circuit executes the program code.

(5) In accordance with a further embodiment of the disclosure, a control method applied in a micro-controller is described in the following paragraph. An external voltage is detected. In response to the external voltage reaching a first predetermined voltage, a register is accessed. In response to the external voltage reaching a second predetermined voltage, the micro-controller is directed to enter a power-down mode. In the power-down mode, the micro-controller stops accessing the register. A determination is made as to whether a wake-up event occurs. In response to there being no wake-up event, the micro-controller stays in the power-down mode. In response to the wake-up event, the micro-controller is directed to enter an operation mode. In the operation mode, the micro-controller executes a program code.

(6) In accordance with another embodiment of the disclosure, an electronic device receives a power from an external device and comprises an energy storage circuit, a storage circuit, a voltage detection circuit, a processing circuit, and a wake-up circuit. The energy storage circuit stores the power to provide an external voltage. The storage circuit comprises a register and stores a program code. The voltage detection circuit detects the external voltage. In response to the external voltage reaching a first predetermined voltage, the processing circuit accesses the register. In response to the external voltage reaching a second predetermined voltage, the processing circuit enters a power-down mode. The processing circuit stops accessing the register in the power-down mode. The wake-up circuit determines whether a wake-up event occurs. In response to the wake-up event, the wake-up circuit directs the processing circuit to exit the power-down mode and enter an operation mode. In response to there being no wake-up event, the processing circuit operates in the power-down mode. In the operation mode, the processing circuit executes the program code.

(7) Control method of micro-controller may be practiced by the control circuit or the electronic device which have hardware or firmware capable of performing particular functions and may take the form of program code embodied in a tangible media. When the program code is loaded into and executed by an electronic device, a processor, a computer or a machine, the electronic device, the processor, the computer or the machine becomes the control circuit or the electronic device for practicing the disclosed method.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

(1) The present invention can be more fully understood by reading the subsequent detailed description and examples with references made to the accompanying drawings, wherein:

(2) FIG. **1** is a schematic diagram of an exemplary embodiment of an electronic device according to various aspects of the present disclosure.

(3) FIG. **2**A is a schematic diagram of an exemplary embodiment of a control circuit according to various aspects of the present disclosure.

(4) FIG. **2**B is a schematic diagram of an exemplary embodiment of an external voltage according to various aspects of the present disclosure.

(5) FIG. **3**A is a schematic diagram of another exemplary embodiment of the control circuit according to various aspects of the present disclosure.

(6) FIG. **3**B is a schematic diagram of another exemplary embodiment of the external voltage according to various aspects of the present disclosure.

(7) FIG. **4** is a flowchart of an exemplary embodiment of a control method, according to various aspects of the present disclosure.

DETAILED DESCRIPTION OF THE INVENTION

(8) The present invention will be described with respect to particular embodiments and with reference to certain drawings, but the invention is not limited thereto and is only limited by the claims. The drawings described are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated for illustrative purposes and not drawn to scale. The dimensions and the relative dimensions do not correspond to actual dimensions in the practice of the invention.

(9) FIG. **1** is a schematic diagram of an exemplary embodiment of an electronic device according to various aspects of the present disclosure. The electronic device **110** comprises an induction winding **111**, an energy storage circuit **112**, and a control circuit **113**. The induction winding **111** induces a radio wave **130** and generates an induction voltage VR according to the electrical energy component of the radio wave **130**. The induction winding **111** provides the induction voltage VR to the energy storage circuit **112** to charge the energy storage circuit **112**. The energy storage circuit **112** stores the induction voltage VR to provide an external voltage VDD. In this embodiment, since the induction winding **111** charges the energy storage circuit **112** continuously, the external voltage is to increase gradually. In some embodiments, when the external voltage VDD reaches a target value, the induction winding **111** stops charging the energy storage circuit **112**. The control circuit **113** operates according to the external voltage VDD. In one embodiment, the control circuit **113** is a micro-controller unit (MCU).

(10) The kind of electronic device **110** is not limited in the present disclosure. In one embodiment, the electronic device **110** is a smoke detector or a tag of a radio frequency identification (RFID) system. In this case, an external device **120** emits the radio wave **130** to drive the electronic device **110**. The kind of external device **120** is not limited in the present disclosure. In one embodiment, the external device **120** is a reader of the RFID system. In another embodiment, the electronic device **110** is a passive stylus pen. In this case, the external device **120** is a digital pad. In other embodiments, the external device **120** charges the energy storage circuit **112** via a connection line (not shown). In this case, the electronic device **110** does not need the induction winding **111**.

(11) FIG. **2**A is a schematic diagram of an exemplary embodiment of a control circuit according to various aspects of the present disclosure. The control circuit **200** comprises a voltage detection circuit **210**, a wake-up circuit **220**, a processing circuit **230**, and a storage circuit **240**. The voltage detection circuit **210** detects an external voltage VDD. In this embodiment, the external voltage VDD is provided by the energy storage circuit **112**. As shown in FIG. **2**A, the energy storage circuit **112** at least comprises a capacitor C. The voltage stored in the capacitor C is provided as the external voltage VDD.

(12) The voltage detection circuit **210** stores a predetermined voltage V**1**. In one embodiment, the predetermined voltage V**1** is a power-on reset (POR) voltage. When the external voltage VDD is lower than the predetermined voltage V**1**, the voltage detection circuit **210** enables a stop signal STP. When the external voltage VDD reaches the predetermined voltage V**1**, the voltage detection circuit **210** enables an initialization signal RST. The structure of voltage detection circuit **210** is not limited in the present disclosure. Any circuit can serve as the voltage detection circuit **210**, as long as the circuit is capable of detecting voltages.

(13) The processing circuit **230** receives the stop signal STP and the initialization signal RST. When the stop signal STP is enabled, the processing circuit **230** stops operating. When the initialization signal RST is enabled, the processing circuit **230** enters an initialization mode. In the initialization mode, the processing circuit **230** executes an initializing operation. In one embodiment, the processing circuit **230** initials the register **241** in the storage circuit **240**.

(14) The invention does not limit how the processing circuit **230** initializes the register **241**. In one embodiment, the processing circuit **230** writes a set value in the register **241**. In this case, an element (e.g., a comparator **221**) in the control circuit **200** operates according to the value of the register **241**. The number of registers in the storage circuit **240** is not limited in the present disclosure. In other embodiments, the storage circuit **240** comprises more registers. In this case, the processing circuit **230** writes a plurality of set values to the registers. In some embodiments, the storage circuit **240** further comprises a memory **242**. The memory **242** stores a program code. The type of memory **242** is not limited in the present disclosure. In one embodiment, the memory **242** is a flash memory.

(15) In some embodiments, the control circuit **200** further comprises a driving circuit **250**. The driving circuit **250** is configured to drive the processing circuit **230**. When the external voltage VDD arrives the predetermined voltage V**1**, the voltage detection circuit **210** triggers the driving circuit **250**. Therefore, the driving circuit **250** provides at least one driving signal (e.g., at least one of the output voltage VOP and the clock signal CLK) to the processing circuit **230**. In another embodiment, the driving circuit **250** directly receives the external voltage VDD and determines whether the external voltage VDD arrives the predetermined voltage V**1**. When the external voltage VDD arrives the predetermined voltage V**1**, the driving circuit **250** provides the driving signal to the processing circuit **230**.

(16) The structure of driving circuit **250** is not limited in the present disclosure. In one embodiment, the driving circuit **250** comprises a voltage converter circuit **251**. The voltage converter circuit **251** converts the external voltage VDD to generate the output voltage VOP and provides the output voltage VOP to the processing circuit **230**. The invention does not limit how the voltage converter circuit **251** converts the external voltage VDD. In one embodiment, the voltage converter circuit **251** increases or reduces the level of the external voltage VDD. When the processing circuit **230** receives the output voltage VOP, the processing circuit **230** performs an initialization operation, such as to initial the register **241**. The structure of voltage converter circuit **251** is not limited in the present disclosure. The voltage converter circuit **251** is a low-dropout regulator (LDO). In another embodiment, the driving circuit **250** comprises a clock source **252**. The clock source **252** generates a clock signal CLK**1** and provides the clock signal CLK**1** to the processing circuit **230**. The circuit structure of clock source **252** is not limited in the present disclosure. In one embodiment, the clock source **252** comprises an initial RC oscillator (IRC).

(17) In other embodiments, the processing circuit **230** operates in a corresponding mode according to the frequency of the clock signal CLK**1**. For example, when the frequency of the clock signal CLK**1** is equal to a first value, the processing circuit **230** enters a standby mode. When the frequency of the clock signal CLK**1** is equal to a second value, the processing circuit **230** enters an operation mode. The first value is lower than the second value. For example, the first value may be 1 MHz, and the second value may be 4 MHz, 8 MHz, 24 MHz, or 48 MHz.

(18) In some embodiment, the voltage detection circuit **210** further stores a predetermined voltage

V**2**. The predetermined voltage V**2** is higher than the predetermined voltage V**1**. When the external voltage VDD reaches the predetermined voltage V**2**, the processing circuit **230** enters a power-down mode. In the power-down mode, the processing circuit **230** stops performing the initialization operation. In this embodiment, the predetermined voltage V**2** is slightly greater than the a low-voltage reset (LVR) voltage. In some embodiments, when the external voltage VDD drops gradually and is lower than the LVR voltage, the processing circuit **230** re-performs the initialization operation.

(19) The wake-up circuit **220** is coupled to the processing circuit **230** and determines whether a wake-up event occurs. In this embodiment, when the external voltage VDD arrives at the predetermined voltage V**2**, the wake-up circuit **220** determines whether a wake-up event occurs. When there is no wake-up event, the wake-up circuit **220** does not wake-up the processing circuit **230**. Therefore, the processing circuit **230** continues to operate in the power-down mode. However, when an wake-up event occurs, the wake-up circuit **220** wakes-up the processing circuit **230**. Therefore, the processing circuit **230** exits the power-down mode and enters an operation mode. In the operation mode, the processing circuit **230** accesses the memory **242** to execute the program code stored in the memory **242**.

(20) In one embodiment, the wake-up event is the external voltage VDD reaching a predetermined voltage V**3**. The invention does not limit how the wake-up circuit **220** determines whether the external voltage VDD has reached the predetermined voltage V**3**. In one embodiment, the wake-up circuit **220** comprises a comparator **221**. The comparator **221** compares the external voltage VDD and the predetermined voltage V**3**. When the external voltage VDD has not reached the predetermined voltage V**3**, the comparator **221** does not enable a wake-up signal SWU. Therefore, the processing circuit **230** continues to operate in the power-down mode. When the external voltage VDD reaches the predetermined voltage V**3**, the comparator **221** enables the wake-up signal SWU. Therefore, the processing circuit **230** exits the power-down mode and enters the operation mode. In one embodiment, after the processing circuit **230** enters the operation mode, the wake-up circuit **220** stops determining whether the wake-up event occurs. Therefore, the power consumption of the control circuit **200** can be reduced. In some embodiments, after the processing circuit **230** is waked up by the wake-up circuit **220**, the processing circuit **230** ignores the wake-up signal SWU. In this case, the processing circuit **230** may re-enter the power-down mode or exits the power-down mode according to the program code in the memory **242**.

(21) In some embodiments, the wake-up circuit **220** at least comprises a register (not shown). In this case, when the external voltage VDD reaches the predetermined voltage V**1**, the processing circuit **230** performs an initialization operation. The initialization operation is to write at least set value to the register of the wake-up circuit **220** to initial the comparator **221**.

(22) In this embodiment, the predetermined voltage V**3** is higher than the predetermined voltage V**2**, and the predetermined voltage V**2** is higher than the predetermined voltage V**1**. For example, the predetermined voltage V**3** may be 4V, the predetermined voltage V**2** may be 1.8V, and the predetermined voltage V**1** may be 1.2V.

(23) FIG. **2**B is a schematic diagram of an exemplary embodiment of the external voltage according to various aspects of the present disclosure. Before time point T**21**, since the induction winding **111** charges the energy storage circuit **112**, the external voltage VDD generated by the energy storage circuit **112** is increased gradually. Since the external voltage VDD is lower than the predetermined voltage V**1**, the processing circuit **230** does not operate.

(24) At time point T**21**, the external voltage VDD reaches the predetermined voltage V**1**. Therefore, the processing circuit **230** enters an initialization mode, in the initialization mode, the processing circuit **230** performs an initialization operation. When the processing circuit **230** performs the initialization operation, it does not cause too much power consumption, so the external voltage VDD continually to rise.

(25) At time point T**22**, since the external voltage VDD reaches the predetermined voltage V**2**, the

processing circuit **230** enters a power-down mode to temporarily stop performing the initialization operation. Before the processing circuit **230** enters the power-down mode, the external voltage VDD is slightly reduced. Since the external voltage VDD is not lower than the LVR voltage, it will not cause the processing circuit **230** to perform a reset operation, such as to initial the register **241**.

(26) At time point T**23**, since the processing circuit **230** has enter the power-down mode, the external voltage VDD increases gradually. At this time, the wake-up circuit **220** starts operating to determine whether a wake-up event occurs.

(27) At time point T**24**, since the external voltage VDD has reached the predetermined voltage V**3**, the wake-up circuit **220** wakes the processing circuit **230** up. Therefore, the processing circuit **230** exits the power-down mode and enters an operation mode. In the operation mode, the processing circuit **230** performs the program code of the memory **242**. When the processing circuit **230** performs the program code, the processing circuit **230** causes the power consumption so that the external voltage VDD is reduced gradually.

(28) At time point T**25**, the processing circuit **230** enters the power-down mode according to the program code stored in the memory **242**. Since the processing circuit **230** stops operating, the external voltage VDD is gradually increased at time point T**25**.

(29) At time point T**26**, the processing circuit **230** exits the power-down mode and enters the operation mode according to the program code stored in the memory **242**. In the operation mode, the processing circuit **230** performs the program code stored in the memory **242** so that the external voltage VDD is gradually reduced.

(30) At time point T**27**, the processing circuit **230** enters the power-down mode according to the program code of the memory **242**. Since the processing circuit **230** stops operating, the external voltage VDD is gradually increased after time point T**27**.

(31) In this embodiment, when the external voltage VDD reaches the predetermined voltage V**2**, the processing circuit **230** enters the power-down mode to reduce the power consumption. Therefore, the external voltage VDD is stably and gradually increased. When the external voltage VDD reaches the predetermined voltage V**3**, it means that the external voltage VDD is sufficient. At this time, even if the processing circuit **230** performs the program code stored in the memory **242**, the external voltage VDD is not lower than the LVR voltage to avoid the processing circuit **230** from performing a reset operation many times.

(32) FIG. **3**A is a schematic diagram of another exemplary embodiment of the control circuit according to various aspects of the present disclosure. The control circuit **300** of FIG. **3**A is similar to the control circuit **200** of FIG. **2**A with the exception that the wake-up circuit **320** of FIG. **3**A is a timer **321**. Since the characteristics of the voltage detection circuit **310**, the processing circuit **330**, and the storage circuit **340** shown in FIG. **3**A are similar to the characteristics of the voltage detection circuit **210**, the processing circuit **230**, and the storage circuit **240** shown in FIG. **2**A, the related description is omitted here.

(33) When the external voltage VDD reaches the predetermined voltage V**2**, the processing circuit **330** enters the power-down mode. In this case, the wake-up circuit **320** determines whether the duration of the processing circuit **330** being in the power-down mode has reached a predetermined value (e.g., 4 seconds). When the duration of the processing circuit **330** being in the power-down mode has not reached a predetermined value, the wake-up circuit **320** does not wake up the processing circuit **330**. However, when the duration of the processing circuit **330** being in the power-down mode has reached a predetermined value, the wake-up circuit **320** wakes up the processing circuit **330**. Therefore, the processing circuit **330** exits the power-down mode and enters the operation mode. In one embodiment, after the wake-up circuit **320** wakes the processing circuit **330** up, the wake-up circuit **320** stops working. In this case, once the processing circuit **330** is woken up, the processing circuit **330** is no longer controlled by the wake-up circuit **320**.

(34) In this embodiment, the wake-up circuit **320** is a timer **321**. The timer **321** counts the number of pulses of a clock signal CLK**2** and adjusts a counter value according to the number of pulses of

the clock signal CLK**2**. When the counter value has not reached a target value, it means that the duration of the processing circuit **330** being in the power-down mode has not reached a predetermined value. Therefore, the timer **321** does not enable the wake-up signal SWU so that the processing circuit **330** stays in the power-down mode. When the counter value has reached a target value, it means that the duration of the processing circuit **330** being in the power-down mode has reached a predetermined value. Therefore, the timer **321** enables the wake-up signal SWU so that the processing circuit **330** exits the power-down mode and enters the operation mode.

(35) In some embodiments, when the external voltage VDD reaches the predetermined voltage V**1**, the processing circuit **330** writes a set value to the register **341**. In this case, the timer **321** operates according to the value of the register **341**. In another embodiment, the wake-up circuit **320** further comprises a register (not shown). When the external voltage VDD reaches the predetermined voltage V**1**, the processing circuit **330** writes a set value to the register of the wake-up circuit **320**. In this case, the timer **321** operates according to the set value of the register in the wake-up circuit **320**.

(36) The source providing the clock signal CLK**2** is not limited in the present disclosure. In one embodiment, the clock signal CLK**2** is provided by the driving circuit **350**. In this case, the driving circuit **350** may comprise a first clock source (not shown) and a second clock source (not shown). The first clock source is configured to provide the clock signal CLK**2**. The second clock source is configured to provide a driving signal SD to the processing circuit **330**. In this case, the driving signal SD is a clock signal (e.g., the clock signal CLK**1** of FIG. **2**A). In other embodiments, the driving circuit **350** comprises a voltage converter circuit (not shown) to provide power to the processing circuit **330**. In this case, the voltage provided by the driving circuit **350** is served as the driving signal SD.

(37) FIG. **3**B is a schematic diagram of another exemplary embodiment of the external voltage according to various aspects of the present disclosure. FIG. **3**B is similar to FIG. **2**B except that the time point T**34** of FIG. **3**B is different from time point T**24** of FIG. **2**B. In FIG. **2**B, time point T**24** is the time point at which the external voltage VDD reaches the predetermined voltage V**3**. In FIG. **3**B, time point T**34** is the time point at which the duration of the processing circuit **330** being in the power-down mode reaches a predetermined value.

(38) In FIG. **3**B, at time point T**33**, the processing circuit **330** enters the power-down mode and the timer **321** starts to count. At time point T**34**, the duration of the processing circuit **330** entering the power-down mode reaches a predetermined value. Therefore, the timer **321** enables the wake-up signal SWU so that the processing circuit **330** exits the power-down mode and enters the operation mode. Since the characteristics of time points T**31**-T**33** and T**35**-T**37** shown in FIG. **3**B are similar to the characteristics of time points T**21**-T**23** and T**25**-T**27** shown in FIG. **2**B, the related description is omitted here.

(39) FIG. **4** is a flowchart of an exemplary embodiment of a control method, according to various aspects of the present disclosure. The control method is applied in a micro-controller. First, an external voltage is received (step S**411**). In one embodiment, the external voltage is provided by a capacitor. In this case, the capacitor is disposed outside of the micro-controller.

(40) Then, a determination is made as to whether the external voltage has reached a first predetermined voltage (step S**412**). When the external voltage reaches the first predetermined voltage, an initialization operation is performed (step S**413**). In one embodiment, the initialization operation is to write a set parameter to a register. The register may be disposed in the micro-controller. In one embodiment, step S**413** is further to convert the external voltage to generate a driving voltage to the micro-controller. In another embodiment, a clock signal is generated in step S**413** and sent to the micro-controller. In other embodiments, when the external voltage has not reached the first predetermined voltage, the micro-controller is deactivated. Therefore, the micro-controller does not operate.

(41) Then, a determination is made as to whether the external voltage has reached a second

predetermined voltage (step S**414**). When the external voltage reaches the second predetermined voltage, the micro-controller is controlled to enter a power-down mode (step S**415**). In the power-down mode, the micro-controller stops accessing the register.

(42) Next, a determination is made as to whether a wake-up event occurs (step S**416**). When the wake-up event does not occur, the micro-controller is controlled to stay in the power-down mode. When the wake-up event occurs, the micro-controller is controlled to enter an operation mode (step S**417**). In the operation mode, the micro-controller executes a program code. In one embodiment, when the micro-controller enters the operation mode, stop determining whether the wake-up event occurs.

(43) In one embodiment, the wake-up event is the external voltage reaching a third predetermined voltage. In this case, when the external voltage has not reached the third predetermined voltage, the micro-controller is controlled to operate in the power-down mode. When the external voltage reaches the third predetermined voltage, the micro-controller is woken up. The micro-controller exits the power-down mode and enters the operation mode. In this case, the third predetermined voltage is greater than the second predetermined voltage, and the second predetermined voltage is greater than the first predetermined voltage.

(44) In another embodiment, the wake-up event is the duration of the micro-controller operating in the power-down mode reaching a predetermined value. In this case, when the external voltage reaches the second predetermined voltage and the micro-controller enters the power-down mode, a timer is activated. Therefore, the timer adjusts a counter value. Next, a determination is made as to whether the counter value has reached a target value. When the counter value has not reached a target value, it means that the duration for which the micro-controller operates in the power-down mode has not reached a predetermined value. Therefore, the micro-controller is controlled to operate in the power-down mode. When the counter value has reached a target value, it means that the duration for which the micro-controller operates in the power-down mode has reached a predetermined value. Therefore, the micro-controller is woken up. The micro-controller exits the power-down mode and enters the operation mode.

(45) Control methods, or certain aspects or portions thereof, may take the form of a program code (i.e., executable instructions) embodied in tangible media, such as floppy diskettes, CD-ROMS, hard drives, or any other machine-readable storage medium, wherein, when the program code is loaded into and executed by a machine such as a computer, the machine thereby becomes a control circuit or an electronic device for practicing the methods. The methods may also be embodied in the form of a program code transmitted over some transmission medium, such as electrical wiring or cabling, through fiber optics, or via any other form of transmission, wherein, when the program code is received and loaded into and executed by a machine such as a computer, the machine becomes a control circuit or an electronic device for practicing the disclosed methods. When implemented on a general-purpose processor, the program code combines with the processor to provide a unique apparatus that operates analogously to application-specific logic circuits.

(46) Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein. It will be understood that although the terms "first," "second," etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another.

(47) While the invention has been described by way of example and in terms of the preferred embodiments, it should be understood that the invention is not limited to the disclosed embodiments. On the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the

appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

Claims

1. A control circuit comprising: a storage circuit comprising a register and storing a program code; a voltage detection circuit detecting an external voltage; a processing circuit accessing the register in response to the external voltage reaching a first predetermined voltage, and entering a power-down mode in response to the external voltage reaching a second predetermined voltage, wherein in the power-down mode, the processing circuit stops accessing the register; and a wake-up circuit detecting whether a wake-up event occurs, wherein: in response to the wake-up event, the wake-up circuit directs the processing circuit to exit the power-down mode and enter an operation mode, in response to there being no wake-up event, the processing circuit operates in the power-down mode, and in the operation mode, the processing circuit executes the program code.

2. The control circuit as claimed in claim 1, wherein in response to the external voltage not reaching the first predetermined voltage, the voltage detection circuit deactivates the processing circuit, and in response to the external voltage reaching the first predetermined voltage, the voltage detection circuit enables an initialization signal so that the processing circuit starts to access the register.

3. The control circuit as claimed in claim 1, wherein: the wake-up event is the external voltage reaching a third predetermined voltage, the third predetermined voltage is higher than the second predetermined voltage, and the second predetermined voltage is higher than the first predetermined voltage.

4. The control circuit as claimed in claim 3, wherein: the wake-up circuit is a comparator, in response to the external voltage not reaching the third predetermined voltage, the comparator does not enable a wake-up signal so that the processing circuit operates in the power-down mode, and in response to the external voltage reaching the third predetermined voltage, the comparator enables the wake-up signal so that the processing circuit exits the power-down mode and enters the operation mode.

5. The control circuit as claimed in claim 1, wherein the wake-up event is the duration of the processing circuit operating in the power-down mode reaching a predetermined value.

6. The control circuit as claimed in claim 5, wherein: the wake-up circuit is a timer, in response to the counter value of the timer not reaching a target value, the timer does not enable a wake-up signal so that the processing circuit continues to operate in the power-down mode, and in response to the counter value of the timer reaching the target value, the timer enables the wake-up signal so that the power-down mode exits the power-down mode and enters the operation mode.

7. The control circuit as claimed in claim 1, further comprising: a driving circuit generating a driving signal and sending the driving signal to the processing circuit in response to the external voltage reaching the first predetermined voltage.

8. The control circuit as claimed in claim 7, wherein: the driving circuit is a voltage converter circuit, the voltage converter circuit converts the external voltage to generate an output voltage, uses the output voltage as the driving voltage, and provides the driving voltage to the processing circuit.

9. The control circuit as claimed in claim 8, wherein: the driving circuit is a clock source, the clock source generates a clock signal, uses the clock signal as the driving signal, and provides the driving signal to the processing circuit.

10. The control circuit as claimed in claim 1, wherein in response to the processing circuit entering the power-down mode, the wake-up circuit stops detecting the occurrence of the wake-up event.

11. A control method applied in a micro-controller and comprising: detecting an external voltage; accessing a register in response to the external voltage reaching a first predetermined voltage;

directing the micro-controller to enter a power-down mode in response to the external voltage reaching a second predetermined voltage, wherein in the power-down mode, the micro-controller stops accessing the register; determining whether a wake-up event occurs; directing the micro-controller to operate in the power-down mode in response to there being no wake-up event; and directing the micro-controller to enter an operation mode in response to the wake-up event, wherein in the operation mode, the micro-controller executes a program code.

12. The control method as claimed in claim 11, further comprising: deactivating the micro-controller so that the micro-controller stops operating in response to the external voltage not reaching the first external voltage.

13. The control method as claimed in claim 11, further comprising: determining whether the external voltage has reached a third predetermined voltage in response to the external voltage reaching the second predetermined voltage and the micro-controller entering the power-down mode; directing the micro-controller to operate in the power-down mode in response to the external voltage not reaching the third predetermined voltage; and waking-up the micro-controller so that the micro-controller exits the power-down mode and enters the operation mode in response to the external voltage reaching the third predetermined voltage.

14. The control method as claimed in claim 13, wherein the third predetermined voltage is higher than the second predetermined voltage, and the second predetermined voltage is higher than the first predetermined voltage.

15. The control method as claimed in claim 11, wherein the wake-up event is the duration of the micro-controller being in the power-down mode reaching a predetermined value.

16. The control method as claimed in claim 11, further comprising: activating a timer to adjust a counter value in response to the external voltage reaching the second predetermined voltage and the micro-controller operating in the power-down mode; determining whether the counter value has reached a target value; directing the micro-controller to operate in the power-down mode in response to the counter value not reaching the target value; and waking-up the micro-controller so that the micro-controller exits the power-down mode and enters the operation mode in response to the counter value reaching the target value.

17. The control method as claimed in claim 11, further comprising: converting the external voltage to generate a driving voltage in response to the external voltage reaching the first predetermined voltage; and providing the driving voltage to the micro-controller.

18. The control method as claimed in claim 11, further comprising: generating a clock signal in response to the external voltage reaching the first predetermined voltage; and providing the clock signal to the micro-controller.

19. The control method as claimed in claim 11, further comprising: stopping the determination of whether a wake-up event occurs.

20. An electronic device receiving a power from an external device and comprising: an energy storage circuit storing the power to provide an external voltage; a storage circuit comprising a register and storing a program code; a voltage detection circuit detecting the external voltage; a processing circuit accessing the register in response to the external voltage reaching a first predetermined voltage, entering a power-down mode in response to the external voltage reaching a second predetermined voltage, and stopping the access of the register in the power-down mode; and a wake-up circuit determining whether a wake-up event occurs, wherein: in response to the wake-up event, the wake-up circuit directs the processing circuit to exit the power-down mode and enter an operation mode, in response to there being no wake-up event, the processing circuit operates in the power-down mode, and in the operation mode, the processing circuit executes the program code.