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SEMICONDUCTOR PACKAGE DEVICE AND METHOD OF MANUFACTURING THE SAME

Abstract

A semiconductor device package includes a first semiconductor device having a first surface, an interconnection element having a surface substantially coplanar with the first surface of the first semiconductor device, a first encapsulant encapsulating the first semiconductor device and the interconnection element, and a second semiconductor device disposed on and across the first semiconductor device and the interconnection element.

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATION [0001] This application is a continuation of U.S. patent application Ser. No. 17/170,666 filed Feb. 8, 2021, now U.S. Pat. No. 12,266,644, which is a continuation of U.S. patent application Ser. No. 16/236,186 filed Dec. 28, 2018, now U.S. Pat. No. 10,930,627, the contents of which are incorporated herein by reference in their entirety.

BACKGROUND
1. Technical Field
[0002] The subject application relates generally to a semiconductor package device and a method of manufacturing the same.
2. Description of the Related Art
[0003] A semiconductor device package includes one or more semiconductor devices. Some of the semiconductor devices may be stacked in the semiconductor device package. Some of the semiconductor devices may be disposed side-by-side in the semiconductor device package. Signal transmission in the semiconductor device package may use conductive traces that provide for lateral transmission. However, a relatively long conductive trace may result in relatively great transmission loss, and such a phenomenon can be significant (e.g. in high-frequency signal transmission).
SUMMARY
[0004] In one or more embodiments, a semiconductor device package includes a first semiconductor device having a first surface, an interconnection element having a surface substantially coplanar with the first surface of the first semiconductor device, a first encapsulant encapsulating the first semiconductor device and the interconnection element, and a second semiconductor device disposed on and across the first semiconductor device and the interconnection element.
[0005] In one or more embodiments, a method of manufacturing a semiconductor device package includes disposing a first semiconductor device and an interconnection element on a carrier, encapsulating the first semiconductor device and the interconnection element, removing the carrier from the first semiconductor device and the interconnection element, and disposing a second semiconductor device across the first semiconductor device and the interconnection element.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0006] Aspects of the subject application are readily understood from the following detailed description when read with the accompanying drawings. It is noted that various features may not be drawn to scale, and the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.
[0007] FIG. **1** illustrates a cross-sectional view of a semiconductor device package in accordance with some embodiments of the subject application.
[0008] FIG. **2** illustrates a cross-sectional view of a semiconductor device package in accordance with some embodiments of the subject application.

[0009] FIG. **3** illustrates a cross-sectional view of a semiconductor device package in accordance with some embodiments of the subject application.
[0010] FIG. **4**A illustrates a cross-sectional view of a semiconductor device package in accordance with a comparative example.
[0011] FIG. **4**B illustrates an enlarged view of a portion of the semiconductor device package shown in FIG. **4**A.
[0012] FIG. **4**C illustrates an enlarged view of a portion of the semiconductor device package shown in FIG. **4**A.
[0013] FIG. **5**A, FIG. **5**B, FIG. **5**C and FIG. **5**D illustrate a method of manufacturing a semiconductor device package in accordance with some embodiments of the subject application.
[0014] FIG. **6**A, FIG. **6**B, FIG. **6**C and FIG. **6**D illustrate a method of manufacturing a semiconductor device package in accordance with some embodiments of the subject application.
[0015] FIG. **7**A, FIG. **7**B, FIG. **7**C and FIG. **7**D illustrate a method of manufacturing a semiconductor device package in accordance with some embodiments of the subject application.
[0016] FIG. **8**A, FIG. **8**B and FIG. **8**C illustrate a comparative method of manufacturing a semiconductor device package.
[0017] Common reference numerals are used throughout the drawings and the detailed description to indicate the same or similar elements.

DETAILED DESCRIPTION

[0018] A lateral transmission path is reduced or minimized in some embodiments of the subject application. A horizontal transmission path is reduced or minimized in some embodiments of the subject application.
[0019] FIG. **1** illustrates a cross-section view of a semiconductor device package **1** in accordance with some embodiments of the subject application. The semiconductor device package **1** comprises a semiconductor device **11**, an interconnection element **12**, an encapsulant **13**, a semiconductor device **14**, a redistribution layer (RDL) structure **15**, an RDL structure **16**, and connection elements **17**.
[0020] The semiconductor device **11** has a surface **111**. The surface **111** may include or may constitute at least part of an active surface. The surface **111** is adjacent to an active side of the semiconductor device **11**. The surface **111** is opposite a back side or back surface of the semiconductor device **11**.
[0021] The semiconductor device **11** may include, for example, but is not limited to, an optical die (e.g. a photonic die), a radio frequency die, a detector, or other integrated circuit.
[0022] The semiconductor device **11** includes an optical element **112**. The optical element **112** may include a guiding element, such as an optical waveguide. The optical element **112** may include a grating structure **112***g*. The optical element **112** may be embedded in the semiconductor device **11**. The grating structure **112***g* may be exposed from the surface **111** of the semiconductor device **11**. The grating structure **112***g* (e.g. a grating coupler) may receive light beams from an external optical fiber (not illustrated in FIG. **1**), and the received light beams are transmitted via the optical element **112**. The optical element **112** may include an optical waveguide, an acoustic waveguide, an electromagnetic waveguide, or the like. The semiconductor device **11** may include an optoelectronic converter (not illustrated in FIG. **1**).
[0023] The semiconductor device **11** is encapsulated by the encapsulant **13**. The surface **111** of the semiconductor device **11** is exposed by the encapsulant **13**. The encapsulant **13** has a surface **131**. The surface **111** of the semiconductor device **11** is substantially coplanar with the surface **131** of the encapsulant **13**. The semiconductor device **11** is disposed adjacent to the surface **131** of the encapsulant **13**.
[0024] The encapsulant **13** may include an epoxy resin. The encapsulant **13** may include a molding compound (e.g., an epoxy molding compound or other molding compound). The encapsulant **13** may include a polyimide. The encapsulant **13** may include a phenolic compound or material. The

encapsulant **13** may include fillers or particles (e.g. silica particles).
[0025] The RDL structure **15** is disposed on the encapsulant **13**. The RDL structure **15** is disposed on the semiconductor device **11**. The RDL structure **15** is electrically connected to the semiconductor device **11**. The RDL structure **15** includes one or more conductive traces **151**. The RDL structure **15** includes one or more interconnection elements **153**. The interconnection elements **153** may include a conductive via. The RDL structure **15** includes a passivation layer **152**. The RDL structure **15** may include or may be a single layer structure. The RDL structure **15** may include or may be a multilayer structure in accordance with some embodiments of the subject application.
[0026] The interconnection element **12** includes conductive vias **121** and a passivation layer **122**. The interconnection element **12** includes an interposer structure. The interconnection element **12** includes a frameboard structure. The interconnection element **12** is encapsulated by the encapsulant **13**. The interconnection element **12** has a surface **123**. The surface **123** of the interconnection element **12** is exposed by the encapsulant **13**. The surface **123** of the interconnection element **12** is substantially coplanar with the surface **111** of the semiconductor device **11**. The interconnection element **12** is separated from the semiconductor device **11** by the encapsulant **13**. The RDL structure **15** is disposed on the interconnection element **12**. The RDL structure **15** is electrically connected to the interconnection element **12**.
[0027] The semiconductor device **14** is disposed on the RDL structure **15**. The semiconductor device **14** is disposed on the semiconductor device **11**. The semiconductor device **14** is disposed on the interconnection element **12**. The semiconductor device **14** is disposed across the semiconductor device **11** and the interconnection element **12** (e.g. extends at least from a position above the semiconductor device **11** to a position above the interconnection element **12**). A surface of the semiconductor device **14** (e.g. a bottom surface) may face and/or be parallel to the surface **111** of the semiconductor device **11**. A surface of the semiconductor device **14** (e.g. the bottom surface) may face and/or be parallel to the surface **123** of the interconnection element **12**. The semiconductor device **14** may include, for example but is not limited to, a controller die, a processor die, an application specific integrated circuit (ASIC) die, a microcontroller unit (MCU) die, or the like. The semiconductor device **14** is electrically connected to the RDL structure **15**. The semiconductor device **14** is electrically connected to the semiconductor device **11** via the RDL structure **15**. The semiconductor device **14** is electrically connected to the interconnection element **12** via the RDL structure **15**.
[0028] Signal transmission according to some embodiments is indicated by dotted arrows shown in FIG. **1**. A signal in the semiconductor device **11** can be vertically transmitted to the semiconductor device **14** through the conductive via **153**. Thus a lateral or horizontal signal transmission path (e.g. other than the conductive via **153**) can be omitted in signal transmission from the semiconductor device **11** to the semiconductor device **14**, and vice versa.
[0029] A signal in the semiconductor device **14** can be vertically transmitted to the interconnection element **12** through the conductive via **153**. Thus a lateral or horizontal signal transmission path (e.g. other than the conductive via **153**) can be omitted in signal transmission from the semiconductor device **14** to the interconnection element **12**, and vice versa.
[0030] The transmission path of the semiconductor device package **1** may thus be minimized, reduced, or made small to mitigate transmission loss.
[0031] The RDL structure **16** is disposed on the encapsulant **13**. The RDL structure **16** includes an interconnection structure **161** and a passivation layer **162**. The RDL structure **16** is electrically connected to the interconnection element **12**.
[0032] The connection elements **17** are disposed on the RDL structure **16**. The connection element **17** may include a solder ball, solder paste, a presolder or other suitable material(s).
[0033] An encapsulant **18** is disposed between semiconductor device **14** and the encapsulant **13**. An encapsulant **18** is disposed between semiconductor device **14** and the semiconductor device **11**. An

encapsulant **18** is disposed between semiconductor device **14** and the interconnection element **12**. The encapsulant **18** may include a capillary underfill (CUF), a molded underfill (MUF) or a dispensing gel, depending on design specifications.

[0034] FIG. **2** illustrates a cross-section view of a semiconductor device package **2**. The semiconductor device package **2** is similar to the semiconductor device package **1** as described and illustrated with reference to FIG. **1**, except that the semiconductor device **11** is replaced by a semiconductor device **11′** and the encapsulant **13** is replaced by an encapsulant **13′**.

[0035] The semiconductor device **11′** is similar to the semiconductor device **11** except a recess, a groove, or a trench R is defined by the semiconductor device **11′** which can receive an external optical fiber (not illustrated in FIG. **2**). The semiconductor device **11′** may include an optical element **112′**. The optical element **112′** may include a guiding element, such as an optical waveguide. The optical element **112′** may be embedded in the semiconductor device **11**. The optical element **112′** may be exposed by the encapsulant **13′**. The recess, groove, or trench R may expose the optical element **112′**. The optical element **112′** (e.g. an edge coupler) may receive light beams from an external optical fiber (not illustrated in FIG. **2**), and the received light beams are transmitted via the optical element **112′**. The optical element **112′** may include an optical waveguide, an acoustic waveguide, an electromagnetic waveguide, or the like.

[0036] The semiconductor device **11′** is encapsulated by the encapsulant **13′**. The semiconductor device **11′** has a surface **113** adjacent to a surface **111′**. The surface **111′** is substantially coplanar with the surface **123** of the interconnection element **12**. The surface **113** is orthogonal to the surface **111′**. The optical element **112′** is exposed from the surface **113**. The surface **113** is exposed from the encapsulant **13′**.

[0037] The semiconductor device **11′** has a surface **114**. The surface **114** is adjacent to the surface **113**. The surface **114** is exposed by the encapsulant **13′**. The surface **114** may be substantially parallel to the surface **111′**.

[0038] The semiconductor device **11′** has a surface **115** which is exposed by the encapsulant **13′**.

[0039] FIG. **3** illustrates a cross-section view of a semiconductor device package **3**. The semiconductor device package **3** is similar to the semiconductor device package **1** as described and illustrated with reference to FIG. **1**, except that the semiconductor device **11** is replaced by a semiconductor device **11″** and the RDL **16** is replaced by an RDL **16′**, and a light emitting device **19** is included.

[0040] The light emitting device **19** is disposed on the semiconductor device **11″**. The light emitting device **19** may include a laser diode. The optical element **112** of the semiconductor device **11″** receives light emitted from the light emitted device **19**. The optical element **112** may receive optical signals from an external optical fiber (not illustrated in FIG. **3**). The semiconductor device **11″** may include an optoelectronic converter for converting optical signals from the light emitting device **19** and/or from the external optical fiber.

[0041] The RDL **16′** is disposed on the encapsulant **13**. The RDL structure **16′** includes an interconnection structure **161′** and a passivation layer **162′**. The RDL structure **16′** defines an opening **160**. The RDL structure **16′** is electrically connected to the interconnection element **12**. The opening **160** is disposed on a side of the encapsulant **13** opposite to the light emitting device **19**. The area of the opening **160** is greater than the area of the light emitting device **19** occupied on the surface **111** of the semiconductor device **16″**. The area of the opening **160** is greater than the area of a conductive pad **116** (e.g. a bond pad) of the semiconductor device **11″** bonded to the light emitting device **19**. A projection of the light emitting device **19** toward the opening **160** falls within the area of the opening **160**. The projection of the light emitting device **19** on to the RDL structure **16′** falls within (e.g., falls entirely within) the area of the opening **160**. The light emitting device **19** is disposed above and between sides of the opening **160**.

[0042] The RDL **15** is disposed on the surface **111** of the semiconductor device **11″**. The RDL **15** is disposed on the surface **123** of the interconnection element **12**. The semiconductor device **14** is

disposed on the RDL **15**. The bottom surface **141** of the semiconductor device **14** is substantially parallel to the surface **111** of the semiconductor device **11**″. The surface **141** of the semiconductor device **14** is substantially parallel to the surface **123** of the interconnection element **12**.

[0043] An interconnection element **153***a* is disposed between the semiconductor device **11**″ and the semiconductor device **14**. An interconnection element **153***b* is disposed between the interconnection element **12** and the semiconductor device **14**. A height of the interconnection element **153***a* is substantially the same as a height of the interconnection element **153***b*.

[0044] FIG. **4**A illustrates a cross-section view of a semiconductor device package **4** in accordance with a comparative example. The semiconductor device package **4** includes a semiconductor device **41**, a carrier **42**, a semiconductor device **44**, a carrier **45**, an adhesive layer **415** and connection elements **414**, **424** and **425**. The semiconductor device **41** is electrically connected to the semiconductor device **44** via connection elements **414**. The semiconductor device **44** is electrically connected to the carrier **42** via connection elements **424**. The carrier **42** is electrically connected to the carrier **45** via connection elements **425**. The semiconductor device **41** is attached to the carrier **45** by the adhesive layer **415**.

[0045] FIG. **4**B illustrates an enlarged view of a portion of the semiconductor device package **4** in a dotted-circle "A" as shown in FIG. **4**A. Referring to FIG. **4**B, a bond-line thickness (BLT) of the adhesive layer **415**, which is the thickness of the adhesive layer **415** between the bottom surface of the semiconductor device **41** and the top surface of the carrier **45**, may be uneven. The adhesive layer **415** may have a thickness Th**1** at one side and another thickness Th**2**, which is different from the thickness Th**1**, at another side. Such uneven BLT may be caused by characteristics of the adhesive (e.g. a viscosity, a temperature, a volume of the adhesive and the like). A thickness difference may lead to tilting of the semiconductor device **41**.

[0046] FIG. **4**C illustrates an enlarged view of a portion of the semiconductor device package **4** in a dotted-circle "B" as shown in FIG. **4**A. The connection elements **414** may include solder balls. The connection elements **414** may include conductive bumps or posts. The connection elements **424** may include solder balls. The connection elements **424** may include conductive bumps or posts.

[0047] The connection element **424** has a height H**1**. The connection element **414** has a height H**2**. The height H**1** is greater than the height H**2**. There may be a height difference among the connection elements **414** and **424** (e.g. resulting from a manufacturing deviation or tolerance). The height difference between the connection elements **414** and **424** may lead to tilting of the semiconductor device **44**, which can adversely affect a reliability of the connection elements **414** and **424** and may cause damage to the semiconductor device package **4** (e.g. breaking or cracking of the connection elements **414** and **424**).

[0048] It may be challenging to manufacture or make solder balls with an identical diameter. Furthermore, it may be challenging to control a size or a height of the solder balls subsequent to a reflow operation. For example, it may be challenging to manufacture or make conductive posts with an identical height because a deviation or a tolerance is highly likely in certain operations (e.g. plating, etching or other operation(s)).

[0049] FIG. **5**A, FIG. **5**B, FIG. **5**C and FIG. **5**D illustrate a method of manufacturing a semiconductor device package in accordance with some embodiments of the subject application.

[0050] Referring to FIG. **5**A, a carrier **50** is provided. A semiconductor device **11** and an interconnection element **12** are disposed on the carrier **50**. The carrier **50** may include a tape, or other releasable material(s).

[0051] Referring to FIG. **5**B, an encapsulant **53** is formed to encapsulate the semiconductor device **11** and the interconnection element **12**.

[0052] Referring to FIG. **5**C, a thinning or planarization operation is applied to the encapsulant **53** to form an encapsulant **13**. A thinning operation is applied to the encapsulant **53** to expose conductive vias **121** of the interconnection element **12**. The carrier **50** is removed from the semiconductor device **11** and the interconnection element **12**. A surface **111** of the semiconductor

device **11** and a surface **123** of the interconnection element **12**, which are attached to a same surface of the carrier **50** prior to the decarrier operation, are substantially coplanar.

[0053] Referring to FIG. **5**D, an RDL **15** is formed on the surface **111** of the semiconductor device **11** and the surface **123** of the conductive element **12**. The RDL **15** is formed on the encapsulant **13**. The RDL **15** includes one or more conductive traces **151**, a passivation layer **152** and conductive vias **153***a* and **153***b*.

[0054] An RDL **16** is formed on the encapsulant **13** on a side of the encapsulant **13** opposite to the RDL **15**. The RDL **16** includes an interconnection structure **161** and a passivation layer **162**. A semiconductor device **14** is bonded to the conductive vias **153***a* and **153***b* through a bonding technique, and an encapsulant **18** is applied to form the semiconductor device package **1** as shown in FIG. **1**.

[0055] FIG. **6**A, FIG. **6**B, FIG. **6**C and FIG. **6**D illustrate a method of manufacturing a semiconductor device package in accordance with some embodiments of the subject application.

[0056] Referring to FIG. **6**A, a semiconductor device **11**′ and an interconnection element **12** are disposed on a carrier **50**. The semiconductor device **11**′ defines a recess, groove or trench R in the surface **111**′ and adjacent to an edge or a lateral surface of the semiconductor device **11**′.

[0057] Referring to FIG. **6**B, the semiconductor device **11**′ and the interconnection element **12** are encapsulated by an encapsulant **53**′.

[0058] Referring to FIG. **6**C, a trimming or planarization operation is performed to form an encapsulant **13**′. Then, the carrier **50** is removed from the encapsulated semiconductor device **11**′ and interconnection element **12**.

[0059] Referring to FIG. **6**D, an RDL **15** is formed on a surface **111**′ of the semiconductor device **11**′ and a surface **123** of the conductive element **12**. The RDL **15** is formed on the encapsulant **13**′. The RDL **15** includes one or more conductive traces **151**, a passivation layer **152** and conductive vias **153***a* and **153***b*.

[0060] An RDL **16** is formed on the encapsulant **13**′ on a side of the encapsulant **13** opposite to the RDL **15**. The RDL **16** includes an interconnection structure **161** and a passivation layer **162**.

[0061] A semiconductor device **14** is bonded to the conductive vias **153***a* and **153***b* through a bonding technique, and an encapsulant **18** is applied to form the semiconductor device package **2** as shown in FIG. **2**.

[0062] FIG. **7**A, FIG. **7**B, FIG. **7**C and FIG. **7**D illustrate a method of manufacturing a semiconductor device package in accordance with some embodiments of the subject application.

[0063] Referring to FIG. **7**A, a semiconductor device **11**″ and an interconnection element **52** are disposed on a carrier **50**.

[0064] Referring to FIG. **7**B, the semiconductor device **11**″ and the interconnection element **12** are encapsulated by an encapsulant **53**.

[0065] Referring to FIG. **7**C, a thinning or planarization operation is applied to the encapsulant **53** to form an encapsulant **13**. A thinning or planarization operation is applied to the encapsulant **53** to expose conductive vias **121** included in the interconnection element **12**. The carrier **50** is removed from the semiconductor device **11** and the interconnection element **12**. A surface **111** of the semiconductor device **11** and a surface **123** of the interconnection element **12**, which are attached to a same surface of the carrier **50** prior to the decarrier operation, are substantially coplanar.

[0066] Referring to FIG. **7**D, an RDL **15** is formed on the surface **111** of the semiconductor device **11** and the surface **123** of the conductive element **12**. The RDL **15** is formed on the encapsulant **13**. The RDL **15** includes one or more conductive traces **151**, a passivation layer **152** and conductive vias **153***a* and **153***b*.

[0067] An RDL **16**′ is formed on the encapsulant **13** on a side of the encapsulant **13** opposite to the RDL **15**. The RDL **16**′ includes an interconnection structure **161**′ and a passivation layer **162**′. The RDL **16**′ defines an opening **160**.

[0068] A semiconductor device **14** is bonded to the conductive vias **153***a* and **153***b* through a

bonding technique, a light emitting element **19** is bonded to the semiconductor device **11**″ via a laser bonding technique, and an encapsulant **18** is applied to form the semiconductor device package **3** as shown in FIG. **3**.

[0069] The semiconductor device **11**″ includes a conductive pad or a bond pad **116** for bonding with the light emitting element **19**. The area of the pad **116** is smaller than the area of the opening **160**. The pad **116** is exposed by the RDL **15**. A bonding material is, for example but not limited to, a solder material, an adhesive, or the like, and may be disposed on the pad **116** before bonding the semiconductor device **14** to the pad **116**. A laser can pass through the opening **160** and the semiconductor device **11**″ to cure or reflow the bonding material as discussed above. The laser used to cure or reflow the bonding material as discussed above may, in some embodiments, be substantially not absorbed by the semiconductor device **11**″. The semiconductor device **11**″ may be substantially transmissive to the laser (e.g. may be about 80% or more transmissive, about 90% or more transmissive, about 95% or more transmissive, or about 99% or more transmissive).

[0070] FIG. **8**A, FIG. **8**B and FIG. **8**C illustrate a method of manufacturing a semiconductor device package in accordance with a comparative example.

[0071] Referring to FIG. **8**A, a carrier **42** is bonded to a carrier **45**. An adhesive or adhesive material **415**′ is formed on the carrier **45**. The carrier **42** is bonded to the carrier **45** via connection elements **425**. The connection elements **425** may include solder balls.

[0072] There may be a height difference among the connection elements **425** (e.g. resulting from a manufacturing deviation or tolerance). A height difference among the connection elements **425** may lead to tilting of the carrier **42**.

[0073] Referring to FIG. **8**B, a semiconductor device **41** is attached to the carrier **45**. The semiconductor device **41** is attached to the carrier **45** by the adhesive material **415**′. After attaching the semiconductor device **41** onto the adhesive material **415**′, a curing operation may be performed to cure adhesive material **415**′ to form an adhesive layer **415**. The adhesive layer **415** may have an uneven BLT caused by characteristics of the adhesive **415**′ (e.g. a viscosity, a temperature, a volume of the adhesive **415**′ and the like). An unevenness of the thickness of the adhesive layer **415** may lead to tilting of the semiconductor device **41**.

[0074] Referring to FIG. **8**C, connections elements **424** are formed on the carrier **42**. Connections elements **414** are formed on the semiconductor device **41**. The connections elements **424** may be formed by, for example but not limited to, implantation techniques. The connections elements **414** may be formed by, for example but not limited to, implantation techniques.

[0075] The connection elements **414** may include solder balls. The connection elements **414** may include conductive bumps or posts. The connection elements **424** may include solder balls. The connection elements **424** may include conductive bumps or posts.

[0076] There may be a height difference among the connection elements **414** (e.g. resulting from a manufacturing deviation or tolerance). There may be a height difference among the connection elements **414** (e.g. resulting from a manufacturing deviation or tolerance).

[0077] A semiconductor device **44** is bonded to the semiconductor device **41** and the carrier **42**, and a reflow operation is performed to form the semiconductor device package **4** as shown in FIG. **4**, according to the present comparative example.

[0078] It may be challenging to manufacture or make solder balls with an identical diameter. Furthermore, it may be challenging to control a size or a height of the solder balls subsequent to a reflow operation. For example, it may be challenging to manufacture or make conductive posts with an identical height because a deviation or a tolerance is highly likely in certain operations (e.g. plating, etching or other operation(s)).

[0079] As used herein, the terms “approximately,” “substantially,” “substantial” and “about” are used to describe and account for small variations. When used in conjunction with an event or circumstance, the terms can refer to instances in which the event or circumstance occurs precisely as well as instances in which the event or circumstance occurs to a close approximation. For

example, when used in conjunction with a numerical value, the terms can refer to a range of variation less than or equal to ±10% of that numerical value, such as less than or equal to ±5%, less than or equal to ±4%, less than or equal to ±3%, less than or equal to ±2%, less than or equal to ±1%, less than or equal to ±0.5%, less than or equal to ±0.1%, or less than or equal to ±0.05%. For example, two numerical values can be deemed to be "substantially" or "about" the same if a difference between the values is less than or equal to ±10% of an average of the values, such as less than or equal to ±5%, less than or equal to ±4%, less than or equal to ±3%, less than or equal to ±2%, less than or equal to ±1%, less than or equal to ±0.5%, less than or equal to ±0.1%, or less than or equal to ±0.05%. For example, "substantially" parallel can refer to a range of angular variation relative to 0° that is less than or equal to ±10°, such as less than or equal to ±5°, less than or equal to ±4°, less than or equal to ±3°, less than or equal to ±2°, less than or equal to ±1°, less than or equal to ±0.5°, less than or equal to ±0.1°, or less than or equal to ±0.05°. For example, "substantially" perpendicular can refer to a range of angular variation relative to 90° that is less than or equal to ±10°, such as less than or equal to ±5°, less than or equal to ±4°, less than or equal to ±3°, less than or equal to ±2°, less than or equal to ±1°, less than or equal to ±0.5°, less than or equal to ±0.1°, or less than or equal to ±0.05°.

[0080] Two surfaces can be deemed to be coplanar or substantially coplanar if a displacement between the two surfaces is no greater than 5 μm, no greater than 2 μm, no greater than 1 μm, or no greater than 0.5 μm.

[0081] As used herein, the terms "conductive," "electrically conductive" and "electrical conductivity" refer to an ability to transport an electric current. Electrically conductive materials typically indicate those materials that exhibit little or no opposition to the flow of an electric current. One measure of electrical conductivity is Siemens per meter (S/m). Typically, an electrically conductive material is one having conductivity greater than approximately 10.sup.4 S/m, such as at least 10.sup.5 S/m or at least 10.sup.6 S/m. The electrical conductivity of a material can sometimes vary with temperature. Unless otherwise specified, the electrical conductivity of a material is measured at room temperature.

[0082] As used herein, the singular terms "a," "an," and "the" may include plural referents unless the context clearly dictates otherwise. In the description of some embodiments, a component provided "on" or "over" another component can encompass cases where the former component is directly on (e.g., in physical contact with) the latter component, as well as cases where one or more intervening components are located between the former component and the latter component.

[0083] While the subject application has been described and illustrated with reference to specific embodiments thereof, these descriptions and illustrations do not limit the subject application. It can be clearly understood by those skilled in the art that various changes may be made, and equivalent components may be substituted within the embodiments without departing from the true spirit and scope of the subject application as defined by the appended claims. The illustrations may not necessarily be drawn to scale. There may be distinctions between the artistic renditions in the subject application and the actual apparatus, due to variables in manufacturing processes and such. There may be other embodiments of the subject application which are not specifically illustrated. The specification and drawings are to be regarded as illustrative rather than restrictive. Modifications may be made to adapt a particular situation, material, composition of matter, method, or process to the objective, spirit and scope of the subject application. All such modifications are intended to be within the scope of the claims appended hereto. While the methods disclosed herein have been described with reference to particular operations performed in a particular order, it can be understood that these operations may be combined, sub-divided, or re-ordered to form an equivalent method without departing from the teachings of the subject application. Therefore, unless specifically indicated herein, the order and grouping of the operations are not limitations of the subject application.

Claims

1. A semiconductor device package, comprising: a first semiconductor device substantially transmissive to a first light; an optical component disposed over the first semiconductor device; a circuit structure disposed under the first semiconductor device and having an opening, wherein the opening is configured to allow a second light to pass through the first semiconductor device and towards the optical component.
2. The semiconductor device package of claim 1, further comprising: a second semiconductor device on the first semiconductor device, wherein the second semiconductor device is free from vertically overlapping the opening.
3. The semiconductor device package of claim 2, further comprising: an interconnection element electrically connected between the circuit structure and the second semiconductor device.
4. The semiconductor device package of claim 3, wherein the second semiconductor device has a surface facing the circuit structure, and a level of the interconnection element with respect to the surface of the second semiconductor device is less than a level of the opening with respect to the surface of the second semiconductor device.
5. The semiconductor device package of claim 2, wherein a portion of the circuit structure is exposed by the second semiconductor device.
6. The semiconductor device package of claim 1, wherein a width of the optical component is less than a width of the opening in a cross-sectional view.
7. The semiconductor device package of claim 1, further comprising: a material disposed between the opening and the optical component and having a transmittance different from that of the first semiconductor device.
8. A semiconductor device package, comprising: a circuit structure; a photonic component disposed over the circuit structure and including a grating structure configured to receive or transmit a light beam; an encapsulant disposed over the photonic component; and a semiconductor device disposed over the photonic component; and a light emitting device disposed over the circuit structure and configured to optically couple to the photonic component.
9. The semiconductor device package of claim 8, wherein the photonic component includes a waveguide configured to receive the light beam from an optical fiber.
10. The semiconductor device package of claim 8, wherein the grating structure is configured to receive the light beam from the light emitting device.
11. The semiconductor device package of claim 9, wherein the photonic component and the optical fiber are configured to provide an optical path, conducting the light beam, laterally overlapping the encapsulant.
12. The semiconductor device package of claim 8, wherein a vertical distance between the light emitting device and the circuit structure is less than a vertical distance between the semiconductor device and the circuit structure.
13. The semiconductor device package of claim 8, wherein the light emitting device is at least partially free from vertically overlapping the encapsulant.
14. The semiconductor device package of claim 8, further comprising: a conductive via electrically connected between the semiconductor device and the circuit structure, and the conductive via laterally overlaps the grating structure.
15. The semiconductor device package of claim 14, wherein the conductive via is spaced apart from the encapsulant.
16. The semiconductor device package of claim 8, wherein the circuit structure has an exposed surface exposed by the photonic component, and the encapsulant covers the exposed surface of the circuit structure.
17. The semiconductor device package of claim 8, wherein the encapsulant vertically overlaps the

circuit structure and the photonic component.

18. A semiconductor device package, comprising: a first semiconductor device substantially transmissive to a first light; a light emitting device optically coupled to first semiconductor device; a circuit structure disposed under the first semiconductor device and having an opening vertically overlapping the light emitting device, wherein the opening is configured to allow a second light to substantially vertically pass through the first semiconductor device and towards the light emitting device.

19. The semiconductor device package of claim 18, wherein the light emitting device occupies a first area on a first surface of the first semiconductor device, a second surface, opposite to the first surface, of the first semiconductor device has a second area exposed to the opening, and the second area is greater than the first area.

20. The semiconductor device package of claim 18, further comprising: a reflowable material disposed between the opening and the light emitting device, wherein the reflowable material is configured to be cured by the second light.