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Frequency-detecting circuit and electronic device

Abstract

A frequency-detecting circuit and an electronic device are provided. The frequency-detecting circuit includes a pulse-narrowing circuit and a judging-and-sampling circuit coupled to the pulse-narrowing circuit. The pulse-narrowing circuit is configured to receive a to-be-detected clock signal, and perform at least one pulse-narrowing process for the to-be-detected clock signal. The pulse-narrowing circuit has at least one detection-point frequency, and the pulse-narrowing circuit is configured to narrow the to-be-detected clock signal based on the detection-point frequency to obtain a narrowed output clock signal. The judging-and-sampling circuit is configured to sample the narrowed output clock signal by employing the to-be-detected clock signal as a sampling clock signal to obtain a frequency indication signal. The frequency indication signal is configured to indicate whether the to-be-detected clock signal is greater than the detection-point frequency.

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Background/Summary

CROSS REFERENCE

(1) The present application claims priorities and rights to Chinese Patent Application No. 202211176423.X, filed on Sep. 26, 2022, the entire content of which is hereby incorporated by reference in its entirety.

TECHNICAL FIELD

(2) The present disclosure relates to the field of circuit technologies, and in particular to a frequency-detecting circuit and an electronic device.

BACKGROUND

(3) A clock signal is usually used in electronic devices. The clock signal is generally used in synchronization circuits as a timer, ensuring relevant electronic components operate synchronously. In some application scenarios, a frequency of the clock signal is required to be detected. In general, a more complex circuit needs to be designed for a specific value of the frequency of the clock signal being accurately detected.

(4) However, in other application scenarios, it is enough to detect a change of the frequency of the clock signal, and the specific value of the frequency is not required to be detected. A change of the

clock signal is required to be detected in real time, so as to determine a range in which the clock signal is.

SUMMARY OF THE DISCLOSURE

(5) The present disclosure provides a frequency-detecting circuit and an electronic device, which are capable of performing a frequency detection for a clock signal.

(6) A frequency-detecting circuit is provided. The frequency-detecting circuit comprises a pulse-narrowing circuit, configured to receive a to-be-detected clock signal, perform at least one pulse-narrowing process for the to-be-detected clock signal, wherein the pulse-narrowing circuit has at least one detection-point frequency, and the pulse-narrowing circuit is configured to narrow the to-be-detected clock signal based on the detection-point frequency to obtain a narrowed output clock signal; and a judging-and-sampling circuit, coupled to the pulse-narrowing circuit, and configured to sample the narrowed output clock signal by employing the to-be-detected clock signal as a sampling clock signal to obtain a frequency indication signal, wherein the frequency indication signal is configured to indicate whether the to-be-detected clock signal is greater than the detection-point frequency.

(7) An electronic device is provided, and comprises the above frequency-detecting circuit.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

(1) In order to more clearly illustrate the technical solutions in the embodiments of the present disclosure, a brief description of the accompanying drawings to be used in the description of the embodiments will be given below. It will be obvious that the accompanying drawings in the following description are only some embodiments of the present disclosure, and that other accompanying drawings may be obtained on the basis of these drawings without any creative effort for those skilled in the art.

(2) FIG. 1 is a structural schematic view of a frequency-detecting circuit according to a first embodiment of the present disclosure.

(3) FIG. 2 is a structural schematic view of the frequency-detecting circuit according to a second embodiment of the present disclosure.

(4) FIG. 3 is a schematic diagram of signal waveforms of each node in an application scenario according to the second embodiment of the present disclosure.

(5) FIG. 4 is a sampling schematic diagram of a judging-and-sampling circuit according to the second embodiment of the present disclosure.

(6) FIG. 5 is a second sampling schematic diagram of the judging-and-sampling circuit according to the second embodiment of the present disclosure.

(7) FIG. 6 is a schematic diagram of the signal waveforms of each node in another application scenario according to the second embodiment of the present disclosure.

(8) FIG. 7 is a third sampling schematic diagram of the judging-and-sampling circuit according to the second embodiment of the present disclosure.

(9) FIG. 8 is a fourth sampling schematic diagram of the judging-and-sampling circuit according to the second embodiment of the present disclosure.

(10) FIG. 9 is a structural schematic view of a pulse-narrowing unit according to an embodiment of the present disclosure.

(11) FIG. 10 is a structural schematic view of the pulse-narrowing unit according to another embodiment of the present disclosure.

(12) FIG. 11 is a structural schematic view of the pulse-narrowing unit according to another embodiment of the present disclosure.

(13) FIG. 12 is a structural schematic view of the pulse-narrowing unit according to another

embodiment of the present disclosure.

(14) FIG. **13** is a structural schematic view of the pulse-narrowing unit according to another embodiment of the present disclosure.

(15) FIG. **14** is a structural schematic view of the pulse-narrowing unit according to another embodiment of the present disclosure.

(16) FIG. **15** is a structural schematic view of the frequency-detecting circuit according to a third embodiment of the present disclosure.

(17) FIG. **16** is a structural schematic view of the frequency-detecting circuit according to a fourth embodiment of the present disclosure.

(18) FIG. **17** is a schematic diagram of the signal waveforms of each node in an application scenario according to the fourth embodiment of the present disclosure.

(19) FIG. **18** is a sampling schematic diagram of the judging-and-sampling circuit according to the fourth embodiment of the present disclosure.

(20) FIG. **19** is another sampling schematic diagram of the judging-and-sampling circuit according to the fourth embodiment of the present disclosure.

(21) FIG. **20** is a schematic diagram of the signal waveforms of each node in another application scenario according to the fourth embodiment of the present disclosure.

(22) FIG. **21** is another sampling schematic diagram of the judging-and-sampling circuit according to the fourth embodiment of the present disclosure.

(23) FIG. **22** is another sampling schematic diagram of the judging-and-sampling circuit according to the fourth embodiment of the present disclosure.

(24) FIG. **23** is a structural schematic view of the frequency-detecting circuit according to a fifth embodiment of the present disclosure.

(25) FIG. **24** is a structural schematic view of an electronic device according to an embodiment of the present disclosure.

(26) FIG. **25** is a structural schematic view of the electronic device according to another embodiment of the present disclosure.

DETAILED DESCRIPTION

(27) The technical solutions in the embodiments of the present disclosure will be clearly and completely described below with reference to accompanying drawings in the embodiments of the present disclosure. Obviously, the described embodiments are only a part of the embodiments of the present disclosure, but not all of the embodiments. Based on the embodiments in the present disclosure, all other embodiments obtained by those skilled in the art without creative efforts shall fall within the scope of the present disclosure.

(28) FIG. **1** is a structural schematic view of a frequency-detecting circuit **100** according to a first embodiment of the present disclosure. The frequency-detecting circuit **100** includes a pulse-narrowing circuit **10** and a judging-and-sampling circuit **20**.

(29) The pulse-narrowing circuit **10** is configured to receive a to-be-detected clock signal CK and perform at least one pulse-narrowing process for the to-be-detected clock signal CK. In some embodiments, each of the at least one pulse-narrowing process is configured to perform a first inversion for a current-level input clock signal, control a rising speed of a rising edge of a level transition or a falling speed of a falling edge of the level transition in a process of the first inversion to obtain a first inverted clock signal PSRDB (not shown in FIG. **1**, referring to FIG. **3**), and perform a second inversion for the first inverted clock signal PSRDB to obtain a current-level narrowed output clock signal PSRD.

(30) In some embodiments, the pulse-narrowing circuit **10** may narrow a logic low level of the to-be-detected clock signal CK. As shown in FIG. **2**, the pulse-narrowing circuit **10** has a plurality of pulse-narrowing units, e.g., includes a first pulse unit, a second pulse unit, and a nth pulse unit, and n is a natural number greater than 2.

(31) In some embodiments, each of the plurality of pulse-narrowing units may perform the pulse-

narrowing process for the logic low level of a clock signal input by a previous-level pulse unit for one time. The pulse-narrowing circuit **10** has a detection-point frequency. As shown in FIG. **3**, the pulse-narrowing circuit **10** performs the first inversion for an input clock signal CK, controls the rising speed of the rising edge of the level transition in the process of the first inversion to obtain the first inverted clock signal PSRDB, and performs the second inversion for the first inverted clock signal PSRDB to obtain the narrowed output clock signal PSRD. When a level of the input clock signal is changed to the rising edge, a logic high level is formed correspondingly. In this case, the first inversion is performed for the input clock signal, such that a state where the level is changed to the rising edge is inverted to a state where the level is changed to the falling edge, and a corresponding logic low level is obtained. When the level of the input clock signal is changed to the falling edge, the logic low level is formed correspondingly. In this case, when the state where the level is changed to the falling edge is inverted to the state where the level is changed to the rising edge, the rising speed of the rising edge of the level transition is controlled. The logic high level is formed after the transition is successful, while only a sawtooth-shaped level is formed in response to a transition failure. In an embodiment, a voltage value of the sawtooth-shaped level is constantly less than a logic threshold.

(32) The first inverted clock signal PSRDB is obtained through performing the first inversion for the level of the input clock signal according to the above manner. In this case, a duration of the logic high level in the first inverted clock signal PSRDB is less than a duration of the logic low level in the input clock signal.

(33) The second inversion is performed for the first inverted clock signal PSRDB to obtain the narrowed output clock signal PSRD.

(34) In some embodiments, a threshold inversion is performed for the first inverted clock signal PSRDB during the second inversion. When the first inverted clock signal PSRDB meets a threshold at the logic low level, the logic low level is inverted to the logic high level. A ramp-shaped level exists between the logic low level of the first inverted clock signal PSRDB and the logic high level of the first inverted clock signal PSRDB due to controlling the rising speed of the rising edge of the level transition. A part of the ramp-shaped level meets the threshold. The part of the ramp-shaped level meeting the threshold is inverted to the logic high level, and a part of the ramp-shaped level not meeting the threshold is inverted to the logic low level. The first inverted clock signal PSRDB is inverted to the logic low level at the logic high level. In this way, the narrowed output clock signal PSRD is obtained.

(35) A duration of the logic low level in the narrowed output clock signal PSRD is less than the duration of the logic low level in the input clock signal.

(36) The pulse-narrowing circuit **10** acquires the first inverted clock signal PSRDB based on controlling the rising speed of the rising edge of the level transition, and the duration of the logic low level in the outputted narrowed output clock signal PSRD is less than the duration of the logic low level in the input clock signal.

(37) The judging-and-sampling circuit **20** is coupled to the pulse-narrowing circuit **10**, and configured to sample the narrowed output clock signal PSRD by employing the to-be-detected clock signal CK as a sampling clock signal to obtain a frequency indication signal FREDET. The frequency indication signal FREDET is configured to indicate a value range of a frequency of the to-be-detected clock signal CK.

(38) When the frequency of the to-be-detected clock signal CK is less than the detection-point frequency, as a low frequency portion shown in FIG. **3**, an obtained first inverted clock signal PSRDB may be successfully converted to the logic high level, such that the narrowed output clock signal PSRD also has a corresponding logic low level.

(39) When the frequency of the to-be-detected clock signal CK is greater than the detection-point frequency, as a high frequency portion shown in FIG. **3**, the obtained first inverted clock signal PSRDB fails to be converted to the logic high level, and only forms the sawtooth-shaped level,

while a current period of the to-be-detected clock signal CK ends. In this way, the narrowed output clock signal PSRD has no corresponding logic low level, but has all logic high levels instead.

(40) As shown in FIG. 4, when the judging-and-sampling circuit **20** continuously samples the narrowed output clock signal PSRD with a time point corresponding to the rising edge of the to-be-detected clock signal CK as a sampling point and obtained narrowed output clock signals PSRD are all logic low levels, an outputted frequency indication signal FREDET is 0. The frequency indication signal FREDET being 0 indicates the frequency of the to-be-detected clock signal CK is in a first frequency range. The narrowed output clock signal PSRD in FIG. 4 corresponds to the narrowed output clock signal PSRD in the low frequency portion of FIG. 3. In some embodiments, the narrowed output clock signal PSRD itself has a time difference from the to-be-detected clock signal CK for a circuit reason. Thus, the narrowed output clock signal PSRD has a delay relative to the to-be-detected clock signal CK, such that the narrowed output clock signal PSRD sampled with the time point corresponding to the rising edge of the to-be-detected clock signal CK as the sampling point may be the logic low level.

(41) In other embodiments, the pulse-narrowing circuit **10** has a delay module capable of delaying an outputted narrowed output clock signal PSRD, such that the narrowed output clock signal PSRD has the delay relative to the to-be-detected clock signal CK.

(42) In other embodiments, the judging-and-sampling circuit **20** has a delay module capable of delaying an inputted narrowed output clock signal PSRD, such that the narrowed output clock signal PSRD has the delay relative to the to-be-detected clock signal CK.

(43) As shown in FIG. 5, when the judging-and-sampling circuit **20** continuously samples the narrowed output clock signal PSRD with the time point corresponding to the rising edge of the to-be-detected clock signal CK as the sampling point and obtained narrowed output clock signals PSRD are all logic high levels, the outputted frequency indication signal FREDET is 1. The frequency indication signal FREDET being 1 indicates the frequency of the to-be-detected clock signal CK is in a second frequency range. The narrowed output clock signal PSRD in FIG. 5 corresponds to the narrowed output clock signal PSRD in the high frequency portion of FIG. 3.

(44) In some embodiments, the pulse-narrowing circuit **10** may narrow the logic high level of the to-be-detected clock signal CK. The pulse-narrowing circuit **10** may include a plurality of pulse-narrowing units, each of the pulse-narrowing units may perform a pulse narrowing process for the logic low level of the to-be-detected clock signal CK. The pulse-narrowing circuit **10** has the detection-point frequency.

(45) For example, as shown in FIG. 6, the pulse-narrowing circuit **10** performs the first inversion for the input clock signal CK, controls the falling speed of the falling edge of the level transition in the process of the first inversion to obtain the first inverted clock signal PSRDB, and performs the second inversion for the first inverted clock signal PSRDB to obtain the narrowed output clock signal PSRD. When the level of the input clock signal is changed to the falling edge, the logic low level is formed correspondingly. In this case, the first inversion is performed for the input clock signal, such that the state where the level is changed to the falling edge is inverted to the state where the level is changed to the rising edge, and a corresponding logic high level is obtained. When the level of the input clock signal is changed to the rising edge, the logic high level is formed correspondingly. In this case, when the state where the level is changed to the rising edge is inverted to the state where the level is changed to the falling edge, the falling speed of the falling edge of the level transition is controlled. The logic low level is formed after the transition is successful, while only the sawtooth-shaped level is formed in response to the transition failure. In an embodiment, the voltage value of the sawtooth-shaped level is constantly less than the logic threshold.

(46) The first inverted clock signal PSRDB is obtained through performing the first inversion for the level of the input clock signal according to the above manner. In this case, a duration of the logic low level in the first inverted clock signal PSRDB is less than a duration of the logic high

level in the input clock signal.

(47) The second inversion is performed for the first inverted clock signal PSRDB to obtain the narrowed output clock signal PSRD.

(48) In some embodiments, the threshold inversion is performed for the first inverted clock signal PSRDB during the second inversion. When the first inverted clock signal PSRDB meets the threshold at the logic high level, the logic high level is inverted to the logic low level. The ramp-shaped level exists between the logic high level of the first inverted clock signal PSRDB and the logic low level of the first inverted clock signal PSRDB due to controlling the falling speed of the falling edge of the level transition. The part of the ramp-shaped level meets the threshold. The part of the ramp-shaped level meeting the threshold is inverted to the logic low level, and the part of the ramp-shaped level not meeting the threshold is inverted to the logic high level. The first inverted clock signal PSRDB is inverted to the logic high level at the logic low level. In this way, the narrowed output clock signal PSRD is obtained.

(49) A duration of the logic high level in the narrowed output clock signal PSRD is less than the duration of the logic high level in the input clock signal.

(50) The pulse-narrowing circuit **10** acquires the first inverted clock signal PSRDB based on controlling the falling speed of the falling edge of the level transition, and the duration of the logic high level in the outputted narrowed output clock signal PSRD is less than the duration of the logic high level in the input clock signal.

(51) The judging-and-sampling circuit **20** is coupled to the pulse-narrowing circuit **10**, and configured to sample the narrowed output clock signal PSRD by employing the to-be-detected clock signal CK as the sampling clock signal to obtain the frequency indication signal FREDET. The frequency indication signal FREDET is configured to indicate the value range of the frequency of the to-be-detected clock signal CK.

(52) When the frequency of the to-be-detected clock signal CK is less than the detection-point frequency, as a low frequency portion shown in FIG. 6, an obtained first inverted clock signal PSRDB may be successfully converted to the logic low level, such that the narrowed output clock signal PSRD also has a corresponding logic high level.

(53) When the frequency of the to-be-detected clock signal CK is greater than the detection-point frequency, as a high frequency portion shown in FIG. 6, the obtained first inverted clock signal PSRDB fails to be converted to the logic low level, and only forms the sawtooth-shaped level, while the current period of the to-be-detected clock signal CK ends. In this way, the narrowed output clock signal PSRD has no corresponding logic high level, but has all logic low levels instead.

(54) As shown in FIG. 7, when the judging-and-sampling circuit **20** continuously samples the narrowed output clock signal PSRD with a time point corresponding to the falling edge of the to-be-detected clock signal CK as the sampling point and the obtained narrowed output clock signals PSRD are all the logic low levels, the outputted frequency indication signal FREDET is 0. The frequency indication signal FREDET being 0 indicates the frequency of the to-be-detected clock signal CK is in the second frequency range. The narrowed output clock signal PSRD in FIG. 7 corresponds to the narrowed output clock signal PSRD in the low frequency portion of FIG. 6. In some embodiments, the narrowed output clock signal PSRD itself has the time difference from the to-be-detected clock signal CK for the circuit reason. Thus, the narrowed output clock signal PSRD has the delay relative to the to-be-detected clock signal CK, such that the narrowed output clock signal PSRD sampled with the time point corresponding to the falling edge of the to-be-detected clock signal CK as the sampling point may be the logic low level.

(55) In other embodiments, the pulse-narrowing circuit **10** has the delay module capable of delaying the outputted narrowed output clock signal PSRD, such that the narrowed output clock signal PSRD has the delay relative to the to-be-detected clock signal CK.

(56) In other embodiments, the judging-and-sampling circuit **20** has the delay module capable of

delaying the inputted narrowed output clock signal PSRD, such that the narrowed output clock signal PSRD has the delay relative to the to-be-detected clock signal CK.

(57) As shown in FIG. 8, when the judging-and-sampling circuit **20** continuously samples the narrowed output clock signal PSRD with the time point corresponding to the falling edge of the to-be-detected clock signal CK as the sampling point and the obtained narrowed output clock signals PSRD are all the logic high levels, the outputted frequency indication signal FREDET is 1. The frequency indication signal FREDET being 1 indicates the frequency of the to-be-detected clock signal CK is in the first frequency range. The narrowed output clock signal PSRD in FIG. 8 corresponds to the narrowed output clock signal PSRD in the low frequency portion of FIG. 6.

(58) In this embodiment, the pulse-narrowing circuit **10** controls the rising speed of the rising edge of the level transition or the falling speed of the falling edge of the level transition to obtain the first inverted clock signal PSRDB, and perform the second inversion for the first inverted clock signal PSRDB to obtain the narrowed output clock signal PSRD. In addition, the judging-and-sampling circuit **20** samples the narrowed output clock signal PSRD. by employing the to-be-detected clock signal as the sampling clock signal to obtain the frequency indication signal FREDET. The frequency indication signal FREDET is configured to indicate the value range of the frequency of the to-be-detected clock signal CK, so as to achieve a detection of the frequency of the to-be-detected clock signal CK. Further, in some scenarios where an accurate frequency is not required to be acquired, but only a frequency level (i.e., a high frequency or a low frequency) is required to be determined, the frequency range in which the to-be-detected clock signal CK is may be indicated directly by the frequency indication signal FREDET.

(59) In some embodiments, the pulse-narrowing circuit **10** has at least one detection-point frequency. The pulse-narrowing circuit **10** narrows the to-be-detected clock signal CK based on the detection-point frequency to obtain the narrowed output clock signal PSRD. The judging-and-sampling circuit **20** is configured to sample the narrowed output clock signal by employing the to-be-detected clock signal CK as the sampling clock signal to determine whether the to-be-detected clock signal CK is greater than the detection-point frequency. The judging-and-sampling circuit **20** is configured to sample the narrowed output clock signal to obtain the frequency indication signal, and the frequency indication signal is configured to indicate whether the to-be-detected clock signal CK is greater than the detection-point frequency.

(60) The detection-point frequency is determined based on an electronic component in the pulse-narrowing circuit **10**. For example, when the pulse-narrowing circuit **10** includes a capacitor, the detection-point frequency may be determined based on capacitance of the capacitor. When the pulse-narrowing circuit **10** includes a MOS transistor, the detection-point frequency may be determined based on a parameter of the MOS transistor.

(61) When the pulse-narrowing circuit **10** includes a current-limiting element such as a resistor or a current source, the detection-point frequency may be determined based on a resistance value of the resistor or a current value of the current source.

(62) When the pulse-narrowing circuit **10** includes an inverter, the detection-point frequency may be determined based on a flip threshold point of the inverter.

(63) The detection-point frequency is taken as a reference. When the frequency of the to-be-detected clock signal CK is greater than the detection-point frequency, the frequency of the to-be-detected clock signal CK is determined to be the high frequency. When the frequency of the to-be-detected clock signal CK is less than the detection-point frequency, the frequency of the to-be-detected clock signal CK is determined to be the low frequency.

(64) In a scenario to control the rising speed of the rising edge of the level transition, as shown in FIG. 4, the to-be-detected clock signal CK is determined to be less than the detection-point frequency, in response to the whole of the frequency indication signal FREDET being a second logic signal.

(65) It can be understood that the less the frequency of to-be-detected clock signal CK is, the

greater the period is. When the pulse-narrowing circuit **10** narrows a pulse based on the detection-point frequency, the logic low level in a low-frequency to-be-detected clock signal CK is not narrowed to disappear. Thus, the narrowed output clock signal includes the logic low level. When the judging-and-sampling circuit **20** continuously samples the narrowed output clock signal PSRD with the time point corresponding to the rising edge of the to-be-detected clock signal CK as the sampling point and the obtained narrowed output clock signals PSRD are all the logic low levels, the outputted frequency indication signal FREDET is 0. In this case, a frequency indication signal FREDET₀ is the second logic signal, and it is determined that the frequency of the to-be-detected clock signal CK is less than the detection-point frequency.

(66) In a scenario to control the rising speed of the rising edge of the level transition, as shown in FIG. 5, the to-be-detected clock signal CK is determined to be greater than the detection-point frequency, in response to the whole of the frequency indication signal FREDET being a first logic signal.

(67) It can be understood that the greater the frequency of to-be-detected clock signal CK is, the less the period is. When the pulse-narrowing circuit **10** narrows the pulse based on the detection-point frequency, the logic low level in a high-frequency to-be-detected clock signal CK is all narrowed to disappear. Thus, the narrowed output clock signal includes no logic low level. When the judging-and-sampling circuit **20** continuously samples the narrowed output clock signal PSRD with the time point corresponding to the rising edge of the to-be-detected clock signal CK as the sampling point and the obtained narrowed output clock signals PSRD are all the logic high levels, the outputted frequency indication signal FREDET is 1. In this case, a frequency indication signal FREDET₁ is the first logic signal, and it is determined that the frequency of the to-be-detected clock signal CK is greater than the detection-point frequency.

(68) In a scenario to control the falling speed of the falling edge of the level transition, as shown in FIG. 7, the to-be-detected clock signal CK is determined to be greater than the detection-point frequency, in response to the whole of the frequency indication signal FREDET being the first logic signal.

(69) It can be understood that the greater the frequency of to-be-detected clock signal CK is, the less the period is. When the pulse-narrowing circuit **10** narrows the pulse based on the detection-point frequency, the logic high level in the high-frequency to-be-detected clock signal CK is all narrowed to disappear. Thus, the narrowed output clock signal includes no logic high level. When the judging-and-sampling circuit **20** continuously samples the narrowed output clock signal PSRD with the time point corresponding to the falling edge of the to-be-detected clock signal CK as the sampling point and the obtained narrowed output clock signals PSRD are all the logic low levels, the outputted frequency indication signal FREDET is 0. In this case, the frequency indication signal FREDET₀ is the first logic signal, and it is determined that the frequency of the to-be-detected clock signal CK is greater than the detection-point frequency.

(70) In a scenario to control the falling speed of the falling edge of the level transition, as shown in FIG. 8, the to-be-detected clock signal CK is determined to be less than the detection-point frequency, in response to the whole of the frequency indication signal FREDET being the second logic signal.

(71) It can be understood that the less the frequency of to-be-detected clock signal CK is, the greater the period is. When the pulse-narrowing circuit **10** narrows the pulse based on the detection-point frequency, the logic high level in the low-frequency to-be-detected clock signal CK is not narrowed to disappear. Thus, the narrowed output clock signal includes the logic high level. When the judging-and-sampling circuit **20** continuously samples the narrowed output clock signal PSRD with the time point corresponding to the falling edge of the to-be-detected clock signal CK as the sampling point and the obtained narrowed output clock signals PSRD are all the logic high levels, the outputted frequency indication signal FREDET is 1. In this case, the frequency indication signal FREDET₁ is the second logic signal, and it is determined that the frequency of the

to-be-detected clock signal CK is less than the detection-point frequency.

(72) In some embodiments, the pulse-narrowing circuit **10** includes M pulse-narrowing units, each of the pulse-narrowing units is coupled to a previous pulse-narrowing unit, and configured to perform one of the at least one pulse narrowing process by employing a previous-level narrowed output clock signal PSRD of the previous pulse-narrowing unit as a current-level input clock signal thereof, so as to obtain a current-level narrowed output clock signal PSRD. M is a natural number greater than 1. For example, M may be 2, 3, 4, 5, or 6.

(73) The first one of the M pulse-narrowing units is configured to receive the to-be-detected clock signal, and perform the first one of the at least one pulse narrowing process by employing the to-be-detected clock signal as a first-level input clock signal thereof.

(74) In some embodiments, each of the pulse-narrowing units has the same pulse-narrowing capability.

(75) In other embodiments, the pulse-narrowing units have different pulse-narrowing capabilities, respectively. The previous pulse-narrowing unit may have a pulse-narrowing capability higher than a pulse-narrowing capability higher of a current pulse-narrowing unit. In this way, a narrowing level of the narrowed output clock signal PSRD may be increased in the previous pulse-narrowing unit, such that the number of the pulse-narrowing units may be reduced.

(76) In some embodiments, each of the above pulse-narrowing units includes a first inversion circuit and a second inversion circuit. The first inversion circuit is a delayed inversion circuit and configured to perform the first inversion for a received input clock signal, and control the rising speed of the rising edge of the level transition or the falling speed of the falling edge of the level transition by the current-limiting element in a process of the first inversion, to obtain the first inverted clock signal PSRDB. The second inversion circuit is a threshold inversion circuit and configured to perform the second inversion for the first inverted clock signal PSRDB to obtain the narrowed output clock signal. In the following embodiments, the current-limiting element may be a second switching transistor Q2 in FIG. 9, a resistor R1 in FIG. 10, a current source I in FIG. 11, a second switching transistor Q2 in FIG. 12, a resistor R1 in FIG. 13, or a current source I in FIG. 14.

(77) In some embodiments, in the scenario to control the rising speed of the rising edge of the level transition, as shown in FIG. 9, the first inversion circuit includes a first switching transistor Q1, the second switching transistor Q2, a third switching transistor Q3, and a capacitor C, and the second inversion circuit includes the inverter D.

(78) The first switching transistor Q1 has a first terminal configured to receive an operating voltage. The second switching transistor Q2 has a first terminal coupled to a second terminal of the first switching transistor Q1. The third switching transistor Q3 has a first terminal coupled to a second terminal of the second switching transistor Q2, and a second terminal grounded. The capacitor C has a first terminal coupled to the first terminal of the third switching transistor Q1, and a second terminal grounded.

(79) A control terminal of the first switching transistor Q1, a control terminal of the second switching transistor Q2, and a control terminal of the third switching transistor Q3 are configured to receive the to-be-detected clock signal CK. The third switching transistor Q3 is controlled to be turned on to discharge the capacitor C in response to the to-be-detected clock signal CK being the logic high level. The first switching transistor Q1 and the second switching transistor Q2 are controlled to be turned on to charge the capacitor C in response to the to-be-detected clock signal CK being the logic low level, and the second switching transistor Q2 is served as the current-limiting element and configured to control the rising speed of the rising edge of the level transition so as to obtain the first inverted clock signal PSRDB.

(80) During a pulse period having a width in which the to-be-detected clock signal CK is the logic high level, the third switching transistor Q3 is controlled to be turned on, and the first switching transistor Q1 and the second switching transistor Q2 are controlled to be cut off, to discharge the capacitor C. In a process of discharging, the first inverted clock signal PSRDB obtained

correspondingly is the logic low level. During a pulse period having a width in which the to-be-detected clock signal CK is the logic low level, the first switching transistor Q1 and the second switching transistor Q2 are controlled to be turned on, and the third switching transistor Q3 is controlled to be cut off, to charge the capacitor C, and control the rising speed of the rising edge of the level transition. In a process of charging, the first inverted clock signal PSRDB obtained correspondingly is a ramp-shaped logic level in response to a failure control of the rising speed of the rising edge of the level transition, while the first inverted clock signal PSRDB obtained correspondingly is the logic high level in response to a successful control of the rising speed of the rising edge of the level transition.

(81) In subsequence, the second inversion is performed for the first inverted clock signal PSRDB through the inverter D, to obtain the narrowed output clock signal PSRD.

(82) It can be understood that when the third switching transistor Q3 is controlled to be turned on and the first switching transistor Q1 and the second switching transistor Q2 are controlled to be cut off, the capacitor C may be discharged quickly since the first terminal of the capacitor C is coupled to both the first terminal of the third switching transistor Q3 and the second terminal of the second switching transistor Q2. When the first switching transistor Q1 and the second switching transistor Q2 are controlled to be turned on, and the third switching transistor Q3 is controlled to be cut off, a speed of charging the capacitor C is limited since a charging loop includes the first switching transistor Q1 and the second switching transistor Q2.

(83) In an embodiment, the first switching transistor Q1 is a pMOS transistor, the second switching transistor Q2 is the pMOS transistor, and the third switching transistor Q3 is an nMOS transistor.

(84) In some embodiments, in the scenario to control the rising speed of the rising edge of the level transition, as shown in FIG. 10, the first inversion circuit includes the first switching transistor Q1, a resistor R1, the second switching transistor Q2, and the capacitor C, and the second inversion circuit includes the inverter D.

(85) The first switching transistor Q1 has the first terminal configured to receive the operating voltage. The resistor R1 has a first terminal coupled to the second terminal of the first switching transistor Q1. The second switching transistor Q2 has the first terminal coupled to a second terminal of the resistor R1, and the second terminal grounded. The capacitor C has the first terminal coupled to the first terminal of the second switching transistor Q2, and the second terminal grounded.

(86) The control terminal of the first switching transistor Q1 and the control terminal of the second switching transistor Q2 are configured to receive the to-be-detected clock signal CK. The second switching transistor Q2 is controlled to be turned on to discharge the capacitor C in response to the to-be-detected clock signal CK being the logic high level, the first switching transistor Q1 is controlled to be turned on to charge the capacitor C in response to the to-be-detected clock signal CK being the logic low level, and the resistor R1 is served as the current-limiting element and configured to control the rising speed of the rising edge of the level transition so as to obtain the first inverted clock signal PSRDB.

(87) During the pulse period having the width in which the to-be-detected clock signal CK is the logic high level, the second switching transistor Q2 is controlled to be turned on, and the first switching transistor Q1 is controlled to be cut off, to discharge the capacitor C. In the process of discharging, the first inverted clock signal PSRDB obtained correspondingly is the logic low level. During the pulse period having the width in which the to-be-detected clock signal CK is the logic low level, the first switching transistor Q1 and the second switching transistor Q2 are controlled to be cut off, to charge the capacitor C and control the rising speed of the rising edge of the level transition. In the process of charging, the first inverted clock signal PSRDB obtained correspondingly is the ramp-shaped logic level in response to the failure control of the rising speed of the rising edge of the level transition, while the first inverted clock signal PSRDB obtained correspondingly is the logic high level in response to the successful control of the rising speed of

the rising edge of the level transition.

(88) In subsequence, the second inversion is performed for the first inverted clock signal PSRDB through the inverter D, to obtain the narrowed output clock signal PSRD.

(89) It can be understood that when the second switching transistor Q2 is controlled to be turned on and the first switching transistor Q1 is controlled to be cut off, the capacitor C may be discharged quickly since the first terminal of the capacitor C is coupled to both the first terminal of the second switching transistor Q2 and the second terminal of the resistor R1. When the first switching transistor Q1 is controlled to be turned on, and the second switching transistor Q2 is controlled to be cut off, the speed of charging the capacitor C is limited since the charging loop includes the resistor R1.

(90) In an embodiment, the first switching transistor Q1 is the pMOS transistor, the second switching transistor Q2 the nMOS transistor.

(91) In some embodiments, in the scenario to control the rising speed of the rising edge of the level transition, as shown in FIG. 11, the first inversion circuit includes the current source I, the first switching transistor Q1, the second switching transistor Q2, and the capacitor C, and the second inversion circuit includes the inverter D.

(92) The first switching transistor Q1 has the first terminal coupled to the current source I. The second switching transistor Q2 has the first terminal coupled to the second terminal of the first switching transistor Q1, and a second terminal grounded. The capacitor C has the first terminal coupled to the first terminal of the second switching transistor Q2, and the second terminal grounded.

(93) The control terminal of the first switching transistor Q1 and the control terminal of the second switching transistor Q2 are configured to receive the to-be-detected clock signal CK. The second switching transistor Q2 is controlled to be turned on to discharge the capacitor C in response to the to-be-detected clock signal CK being the logic high level. The first switching transistor Q1 is controlled to be turned on to charge the capacitor C in response to the to-be-detected clock signal CK being the logic low level, and the current source I is served as the current-limiting element and configured to control the rising speed of the rising edge of the level transition so as to obtain the first inverted clock signal PSRDB.

(94) During the pulse period having the width in which the to-be-detected clock signal CK is the logic high level, the second switching transistor Q2 is controlled to be turned on, and the first switching transistor Q1 is controlled to be cut off, to discharge the capacitor C. In the process of discharging, the first inverted clock signal PSRDB obtained correspondingly is the logic low level. During the pulse period having the width in which the to-be-detected clock signal CK is the logic low level, the first switching transistor Q1 is controlled to be turned on, and the second switching transistor Q2 is controlled to be cut off, to charge the capacitor C, and control the rising speed of the rising edge of the level transition. In the process of charging, the first inverted clock signal PSRDB obtained correspondingly is the ramp-shaped logic level in response to the failure control of the rising speed of the rising edge of the level transition, while the first inverted clock signal PSRDB obtained correspondingly is the logic high level in response to the successful control of the rising speed of the rising edge of the level transition.

(95) In subsequence, the second inversion is performed for the first inverted clock signal PSRDB through the inverter D, to obtain the narrowed output clock signal PSRD.

(96) It can be understood that when the second switching transistor Q2 is controlled to be turned on and the first switching transistor Q1 is controlled to be cut off, the capacitor C may be discharged quickly since the first terminal of the capacitor C is coupled to both the first terminal of the second switching transistor Q2 and the second terminal of the first switching transistor Q1. When the first switching transistor Q1 is controlled to be turned on, and the second switching transistor Q2 is controlled to be cut off, the speed of charging the capacitor C is limited since the charging loop includes the current source I.

(97) In an embodiment, the first switching transistor Q1 is the pMOS transistor, the second switching transistor Q2 is the nMOS transistor.

(98) In some embodiments, in the scenario to control the falling speed of the falling edge of the level transition, as shown in FIG. 12, the first inversion circuit includes the first switching transistor Q1, the second switching transistor Q2, the third switching transistor Q3, and the capacitor C, and the second inversion circuit includes the inverter D.

(99) The first switching transistor Q1 has the first terminal configured to receive the operating voltage. The second switching transistor Q2 has the first terminal coupled to the second terminal of the first switching transistor Q1. The third switching transistor Q3 has the first terminal coupled to the second terminal of the second switching transistor Q2, and the second terminal grounded. The capacitor C has the first terminal coupled to the first terminal of the second switching transistor Q2, and the second terminal grounded.

(100) The control terminal of the first switching transistor Q1, the control terminal of the second switching transistor Q2, and the control terminal of the third switching transistor Q3 are configured to receive the to-be-detected clock signal CK. The first switching transistor Q1 is controlled to be turned on to charge the capacitor C in response to the to-be-detected clock signal CK being the logic low level. The second switching transistor Q2 and the third switching transistor Q3 are controlled to be turned on to discharge the capacitor C in response to the to-be-detected clock signal CK being the logic high level, and the second switching transistor Q2 is served as the current-limiting element and configured to control the falling speed of the falling edge of the level transition so as to obtain the first inverted clock signal PSRDB.

(101) During the pulse period having the width in which the to-be-detected clock signal CK is the logic low level, the first switching transistor Q1 is controlled to be turned on, and the second switching transistor Q2 and the third switching transistor Q3 are controlled to be cut off, to charge the capacitor C. In the process of charging, the first inverted clock signal PSRDB obtained correspondingly is the logic high level. During the pulse period having the width in which the to-be-detected clock signal CK is the logic high level, the second switching transistor Q2 and the third switching transistor Q3 are controlled to be turned on, and the first switching transistor Q1 is controlled to be cut off, to discharge the capacitor C, and control the falling speed of the falling edge of the level transition. In the process of discharging, the first inverted clock signal PSRDB obtained correspondingly is the ramp-shaped logic level in response to a failure control of the falling speed of the falling edge of the level transition, while the first inverted clock signal PSRDB obtained correspondingly is the logic low level in response to a successful control of the falling speed of the falling edge of the level transition.

(102) In subsequence, the second inversion is performed for the first inverted clock signal PSRDB through the inverter D, to obtain the narrowed output clock signal PSRD.

(103) It can be understood that when the first switching transistor Q1 is controlled to be turned on and the second switching transistor Q2 and the third switching transistor Q3 are controlled to be cut off, the capacitor C may be charged quickly since the first terminal of the capacitor C is coupled to both the first terminal of the second switching transistor Q2 and the second terminal of the first switching transistor Q1. When the second switching transistor Q2 and the third switching transistor Q3 are controlled to be turned on, and the first switching transistor Q1 is controlled to be cut off, a speed of discharging the capacitor C is limited since a discharging loop includes the second switching transistor Q2 and the third switching transistor Q3.

(104) In an embodiment, the first switching transistor Q1 is a pMOS transistor, the second switching transistor Q2 is the nMOS transistor, and the third switching transistor Q3 is the nMOS transistor.

(105) In some embodiments, in the scenario to control the falling speed of the falling edge of the level transition, as shown in FIG. 13, the first inversion circuit includes the first switching transistor Q1, the resistor R1, the second switching transistor Q2, and the capacitor C, and the

second inversion circuit includes the inverter D.

(106) The first switching transistor Q1 has the first terminal configured to receive the operating voltage. The resistor R1 has the first terminal coupled to the second terminal of the first switching transistor Q1. The second switching transistor Q2 has the first terminal coupled to the second terminal of the resistor R1, and the second terminal grounded. The capacitor C has the first terminal coupled to the first terminal of the resistor R1, and the second terminal grounded.

(107) The control terminal of the first switching transistor Q1 and the control terminal of the second switching transistor Q2 are configured to receive the to-be-detected clock signal CK. The first switching transistor Q1 is controlled to be turned on to charge the capacitor C in response to the to-be-detected clock signal CK being the logic low level. The second switching transistor Q2 is controlled to be turned on to discharge the capacitor C in response to the to-be-detected clock signal CK being the logic high level, and the resistor R1 is served as the current-limiting element and configured to control the falling speed of the falling edge of the level transition so as to obtain the first inverted clock signal PSRDB.

(108) During the pulse period having the width in which the to-be-detected clock signal CK is the logic low level, the first switching transistor Q1 is controlled to be turned on, and the second switching transistor Q2 is controlled to be cut off, to charge the capacitor C. In the process of charging, the first inverted clock signal PSRDB obtained correspondingly is the logic high level. During the pulse period having the width in which the to-be-detected clock signal CK is the logic high level, the second switching transistor Q2 is controlled to be turned on, and the first switching transistor Q1 is controlled to be cut off, to discharge the capacitor C and control the falling speed of the falling edge of the level transition. In the process of discharging, the first inverted clock signal PSRDB obtained correspondingly is the ramp-shaped logic level in response to the failure control of the falling speed of the falling edge of the level transition, while the first inverted clock signal PSRDB obtained correspondingly is the logic low level in response to the successful control of the falling speed of the falling edge of the level transition.

(109) In subsequence, the second inversion is performed for the first inverted clock signal PSRDB through the inverter D, to obtain the narrowed output clock signal PSRD.

(110) It can be understood that when the first switching transistor Q1 is controlled to be turned on and the second switching transistor Q2 is controlled to be cut off, the capacitor C may be charged quickly since the first terminal of the capacitor C is coupled to both the first terminal of the second switching transistor Q2 and the second terminal of the first switching transistor Q1. When the second switching transistor Q2 is controlled to be turned on, and the first switching transistor Q1 is controlled to be cut off, the speed of discharging the capacitor C is limited since the discharging loop includes the resistor R1.

(111) In an embodiment, the first switching transistor Q1 is the pMOS transistor, the second switching transistor Q2 the nMOS transistor.

(112) In some embodiments, in the scenario to control the falling speed of the falling edge of the level transition, as shown in FIG. 14, the first inversion circuit includes the current source I, the first switching transistor Q1, the second switching transistor Q2, and the capacitor C, and the second inversion circuit includes the inverter D.

(113) The first switching transistor Q1 has the first terminal configured to receive the operating voltage. The second switching transistor Q2 has the first terminal coupled to the second terminal of the first switching transistor Q1. The capacitor C has the first terminal coupled to the first terminal of the second switching transistor Q2. The current source I has a first terminal coupled to the second terminal of the first switching transistor Q1, and a second terminal grounded.

(114) The control terminal of the first switching transistor Q1 and the control terminal of the second switching transistor Q2 are configured to receive the to-be-detected clock signal CK. The first switching transistor Q1 is controlled to be turned on to charge the capacitor C in response to the to-be-detected clock signal CK being the logic low level. The second switching transistor Q2 is

controlled to be turned on to discharge the capacitor C in response to the to-be-detected clock signal CK being the logic high level, and the current source I is served as the current-limiting element and configured to control the falling speed of the falling edge of the level transition so as to obtain the first inverted clock signal PSRDB.

(115) During the pulse period having the width in which the to-be-detected clock signal CK is the logic low level, the first switching transistor Q1 is controlled to be turned on, and the second switching transistor Q2 is controlled to be cut off, to charge the capacitor C. In the process of charging, the first inverted clock signal PSRDB obtained correspondingly is the logic high level. During the pulse period having the width in which the to-be-detected clock signal CK is the logic high level, the second switching transistor Q2 is controlled to be turned on, and the first switching transistor Q1 is controlled to be cut off, to discharge the capacitor C, and control the falling speed of the falling edge of the level transition. In the process of discharging, the first inverted clock signal PSRDB obtained correspondingly is the ramp-shaped logic level in response to the failure control of the falling speed of the rising edge of the level transition, while the first inverted clock signal PSRDB obtained correspondingly is the logic low level in response to the successful control of the falling speed of the rising edge of the level transition.

(116) In subsequence, the second inversion is performed for the first inverted clock signal PSRDB through the inverter D, to obtain the narrowed output clock signal PSRD.

(117) It can be understood that when the first switching transistor Q1 is controlled to be turned on and the second switching transistor Q2 is controlled to be cut off, the capacitor C may be charged quickly since the first terminal of the capacitor C is coupled to both the first terminal of the second switching transistor Q2 and the second terminal of the first switching transistor Q1. When the second switching transistor Q2 is controlled to be turned on, and the first switching transistor Q1 is controlled to be cut off, the speed of discharging the capacitor C is limited since the discharging loop includes the current source I.

(118) In an embodiment, the first switching transistor Q1 is the pMOS transistor, the second switching transistor Q2 is the nMOS transistor.

(119) In some embodiments, in conjunction with FIG. 15, M being 3 is taken as an example.

(120) The pulse-narrowing circuit 10 includes a first pulse-narrowing unit 11, a second pulse-narrowing unit 12, and a third pulse-narrowing unit 13.

(121) The first-pulse-narrowing unit 11 receives the to-be-detected clock signal CK, and performs one pulse narrowing process by employing the to-be-detected clock signal CK as the current-level input clock signal thereof, so as to obtain the current-level narrowed output clock signal thereof.

(122) The second pulse-narrowing unit 12 is coupled to the first pulse-narrowing unit, and performs one pulse narrowing process by employing the narrowed output clock signal outputted by the first pulse-narrowing unit as the current-level input clock signal thereof, so as to obtain the current-level narrowed output clock signal thereof.

(123) The third pulse-narrowing unit 13 is coupled to the second pulse-narrowing unit, and performs one pulse narrowing process by employing the narrowed output clock signal outputted by the second pulse-narrowing unit as the current-level input clock signal thereof, so as to obtain the current-level narrowed output clock signal thereof.

(124) The first pulse-narrowing unit 11, the second pulse-narrowing unit 12, and the third pulse-narrowing unit 13 may perform a pulse-narrowing process for the logic low level or the logic high level in the input clock signal. It can be understood that the first pulse-narrowing unit 11, the second pulse-narrowing unit 12, and the third pulse-narrowing unit 13 all perform the pulse-narrowing process for the logic low level in the input clock signal; or the first pulse-narrowing unit 11, the second pulse-narrowing unit 12, and the third pulse-narrowing unit 13 all perform the pulse-narrowing process for the logic high level in the input clock signal.

(125) In some embodiments, the pulse-narrowing circuit 10 is configured to provide N detection-point frequencies to obtain N narrowed output clock signals. A coupling point between any of the

pulse-narrowing units and a next-level pulse-narrowing unit, and/or an outputting terminal of the last-level pulse-narrowing unit is able to be an outputting terminal of the pulse-narrowing circuit **10** for outputting a narrowed output clock signal in an individual path. The narrowed output clock signal herein may be the narrowed output clock signal PSRD described above. Each narrowed output clock signal in each individual path corresponds to a corresponding detection-point frequency, which is determined by pulse-narrowing units previous to a corresponding outputting terminal of the pulse-narrowing circuit **10** in each individual path.

(126) The judging-and-sampling circuit **20** includes N judging-and-sampling units. Each of the judging-and-sampling units is coupled to a corresponding one of outputting terminals of the pulse-narrowing circuit **10**, to receive a narrowed output clock signal in a corresponding individual path, and receive the to-be-detected clock signal CK, so as to obtain a corresponding frequency indication signal FREDET in an individual path. N is a natural number less than or equal to M. For example, N may be 2, 3, 4, 5 or 6.

(127) N being 3 is taken as an example.

(128) The pulse-narrowing circuit **10** is configured to provide 3 detection-point frequencies to obtain 3 narrowed output clock signals. The coupling point between any of the pulse-narrowing units and a next-level pulse-narrowing unit, and/or the outputting terminal of the last-level pulse-narrowing unit (e.g., a coupling point A, a coupling point B, and a coupling point C shown in FIG. **15**) is able to be the outputting terminal of the pulse-narrowing circuit **10** for outputting the narrowed output clock signal in the individual path. The narrowed output clock signal herein may be the narrowed output clock signal PSRD described above. Each narrowed output clock signal in each individual path corresponds to the corresponding detection-point frequency, which is determined by pulse-narrowing units previous to the corresponding outputting terminal of the pulse-narrowing circuit **10** in each individual path.

(129) A detection-point frequency of the coupling point A is determined by the first pulse-narrowing unit **11**, a detection-point frequency of the coupling point B is determined by the first pulse-narrowing unit **11** and the second pulse-narrowing unit **12**, and a detection-point frequency of the coupling point C is determined by the first pulse-narrowing unit **11**, the second pulse-narrowing unit **12**, and the third pulse-narrowing unit **13**.

(130) The judging-and-sampling circuit **20** includes 3 judging-and-sampling units, i.e., a first judging-and-sampling unit **21**, a second judging-and-sampling unit **22**, and a third judging-and-sampling unit **23**.

(131) The first judging-and-sampling unit **21** is coupled to the coupling point A to receive the narrowed output clock signal in the corresponding individual path, and receive the to-be-detected clock signal CK, so as to obtain the corresponding frequency indication signal FREDET1 in the individual path.

(132) The second judging-and-sampling unit **22** is coupled to the coupling point B to receive the narrowed output clock signal in the corresponding individual path, and receive the to-be-detected clock signal CK, so as to obtain the corresponding frequency indication signal FREDET2 in the individual path.

(133) The third judging-and-sampling unit **23** is coupled to the coupling point C to receive the narrowed output clock signal in the corresponding individual path, and receive the to-be-detected clock signal CK, so as to obtain the corresponding frequency indication signal FREDET3 in the individual path.

(134) In this way, the value range of the frequency of the to-be-detected clock signal CK may be determined in combination with an obtained frequency indication signal FREDET of each judging-and-sampling unit.

(135) In some embodiments, the frequency indication signal FREDET is indicated 0 or 1. In the scenario to control the rising speed of the rising edge of the level transition, the frequency indication signal FREDET being 0 indicates the frequency of the to-be-detected clock signal CK is

less than the detection-point frequency, while the frequency indication signal FREDET being 1 indicates the frequency of the to-be-detected clock signal CK is greater than the detection-point frequency.

(136) The detection-point frequency of the coupling point A is defined as f_1 , the detection-point frequency of the coupling point B is defined as f_2 , and the detection-point frequency of the coupling point C is defined as f_3 . $f_1 > f_2 > f_3$.

(137) The frequency indication signal obtained by the judging-and-sampling circuit **20** is indicated by XYZ. X indicates the frequency indication signal obtained by the first judging-and-sampling unit, Y indicates the frequency indication signal obtained by the second judging-and-sampling unit, and Z indicates the frequency indication signal obtained by the third judging-and-sampling unit.

(138) When frequency indication signals obtained by the 3 judging-and-sampling units are 111, the frequency of the to-be-detected clock signal CK is greater than f_1 . That is, the frequency of the to-be-detected clock signal CK is greater than the detection-point frequency of the coupling point A.

(139) When the frequency indication signals obtained by the 3 judging-and-sampling units are 011, the frequency of the to-be-detected clock signal CK is greater than f_2 and less than f_1 . That is, the frequency of the to-be-detected clock signal CK is greater than the detection-point frequency of the coupling point B and less than the detection-point frequency of the coupling point A.

(140) When the frequency indication signals obtained by the 3 judging-and-sampling units are 001, the frequency of the to-be-detected clock signal CK is greater than f_3 and less than f_2 . That is, the frequency of the to-be-detected clock signal CK is greater than the detection-point frequency of the coupling point C and less than the detection-point frequency of the coupling point B.

(141) When the frequency indication signals obtained by the 3 judging-and-sampling units are 000, the frequency of the to-be-detected clock signal CK is less than f_3 . That is, the frequency of the to-be-detected clock signal CK is less than the detection-point frequency of the coupling point C.

(142) In the scenario to control the falling speed of the falling edge of the level transition, the frequency indication signal FREDET being 0 indicates the frequency of the to-be-detected clock signal CK is greater than the detection-point frequency, while the frequency indication signal FREDET being 1 indicates the frequency of the to-be-detected clock signal CK is less than the detection-point frequency.

(143) The detection-point frequency of the coupling point A is defined as f_1 , the detection-point frequency of the coupling point B is defined as f_2 , and the detection-point frequency of the coupling point C is defined as f_3 . $f_1 > f_2 > f_3$.

(144) The frequency indication signal obtained by the judging-and-sampling circuit **20** is indicated by XYZ. X indicates the frequency indication signal obtained by the first judging-and-sampling unit, Y indicates the frequency indication signal obtained by the second judging-and-sampling unit, and Z indicates the frequency indication signal obtained by the third judging-and-sampling unit.

(145) When the frequency indication signals obtained by the 3 judging-and-sampling units are 000, the frequency of the to-be-detected clock signal CK is greater than f_1 . That is, the frequency of the to-be-detected clock signal CK is greater than the detection-point frequency of the coupling point A.

(146) When the frequency indication signals obtained by the 3 judging-and-sampling units are 100, the frequency of the to-be-detected clock signal CK is greater than f_2 and less than f_1 . That is, the frequency of the to-be-detected clock signal CK is greater than the detection-point frequency of the coupling point B and less than the detection-point frequency of the coupling point A.

(147) When the frequency indication signals obtained by the 3 judging-and-sampling units are 110, the frequency of the to-be-detected clock signal CK is greater than f_3 and less than f_2 . That is, the frequency of the to-be-detected clock signal CK is greater than the detection-point frequency of the coupling point C and less than the detection-point frequency of the coupling point B.

(148) When the frequency indication signals obtained by the 3 judging-and-sampling units are 111, the frequency of the to-be-detected clock signal CK is less than f_3 . That is, the frequency of the to-

be-detected clock signal CK is less than the detection-point frequency of the coupling point C.

(149) In other embodiments, the frequency indication signal FREDET obtained by the last-level judging-and-sampling unit is taken as a determining basis for frequency detection.

(150) In some embodiments, for protecting a result of the frequency detection from an influence of a duty cycle of the to-be-detected clock signal CK, as shown in FIG. 16, the frequency-detecting circuit 100 includes the pulse-narrowing circuit 10, the judging-and-sampling circuit 20, and a frequency division circuit 30.

(151) The frequency division circuit 30 is configured to receive the to-be-detected clock signal CK, divide the frequency of the to-be-detected clock signal CK, and output a frequency division clock signal CLK.

(152) The pulse-narrowing circuit 10 is coupled to an output terminal of the frequency division circuit 30 and configured to perform the at least one pulse-narrowing process for the frequency division clock signal CLK to obtain the narrowed output clock signal PSRD.

(153) The judging-and-sampling circuit 20 is configured to sample the narrowed output clock signal PSRD by employing the frequency division clock signal CLK as the sampling clock signal, to obtain the frequency indication signal FREDET.

(154) In some embodiments, the frequency division circuit 30 may be a two-frequency division circuit, a four-frequency division circuit, or an eight-frequency division circuit. It can be understood that the frequency division circuit 30 may be a $2n$ -fold frequency division circuit, and n is a natural number greater than 0.

(155) In some embodiments, the frequency division circuit 30 is illustrated as the two-frequency division circuit.

(156) In the scenario to control the rising speed of the rising edge of the level transition, as shown in FIG. 17, the frequency division circuit 30 is configured to receive the to-be-detected clock signal CK, perform a two-frequency division for the to-be-detected clock signal CK, and output a two-frequency division clock signal CKDIV2.

(157) The pulse-narrowing circuit 10 is coupled to the output terminal of the frequency division circuit 30 and configured to perform the at least one pulse-narrowing process for the frequency division clock signal to obtain the narrowed output clock signal PSRD. A level pulse width (e.g., 1 us) of the two-frequency division clock signal CKDIV2 depends on the level number of the pulse-narrowing circuit 10 and a parameter of the current-limiting element of each level (e.g., a transistor size, and a capacitor size; the less the discharging speed is, the less a size of a MOS transistor is, and the less the discharging speed is the greater a resistor value is). A goal of the pulse-narrowing circuit 10 is to narrow all pulses of the two-frequency division clock signal CKDIV2 above the detection-point frequency until these pulses disappear.

(158) As shown in FIG. 17, when the frequency of the to-be-detected clock signal CK is less than the detection-point frequency in the pulse-narrowing circuit 10, the narrowed output clock signal PSRD may show a waveform diagram corresponding to a low-frequency portion as shown in FIG. 17.

(159) When the frequency of the to-be-detected clock signal CK is greater than the detection-point frequency in the pulse-narrowing circuit 10, the narrowed output clock signal PSRD may show a waveform diagram corresponding to a high-frequency portion as shown in FIG. 17.

(160) As shown in FIG. 18, when the judging-and-sampling circuit 20 samples the waveform diagram corresponding to the low-frequency portion in FIG. 17, the judging-and-sampling circuit 20 continuously samples the narrowed output clock signal PSRD by employing a time point corresponding to a rising edge of the two-frequency division clock signal CKDIV2 and the obtained narrowed output clock signals PSRD are all the logic low levels, the outputted frequency indication signal FREDET is 0. When the frequency indication signal FREDET is 0, it is determined that the frequency of the to-be-detected clock signal CK is in the first frequency range.

(161) As shown in FIG. 19, when the judging-and-sampling circuit 20 samples the waveform

diagram corresponding to the high-frequency portion in FIG. 17, the judging-and-sampling circuit **20** continuously samples the narrowed output clock signal PSRD by employing the time point corresponding to the rising edge of the two-frequency division clock signal CKDIV2 and the obtained narrowed output clock signals PSRD are all the logic high levels, the outputted frequency indication signal FREDET is 1. When the frequency indication signal FREDET is 1, it is determined that the frequency of the to-be-detected clock signal CK is in the second frequency range. The first frequency range is less than the second frequency range.

(162) In the scenario to control the falling speed of the falling edge of the level transition, as shown in FIG. 20, the frequency division circuit **30** is configured to receive the to-be-detected clock signal CK, perform the two-frequency division for the to-be-detected clock signal CK, and output the two-frequency division clock signal CKDIV2.

(163) The pulse-narrowing circuit **10** is coupled to the output terminal of the frequency division circuit **30** and configured to perform the at least one pulse-narrowing process for the frequency division clock signal to obtain the narrowed output clock signal PSRD.

(164) As shown in FIG. 20, when the frequency of the to-be-detected clock signal CK is less than the detection-point frequency in the pulse-narrowing circuit **10**, the narrowed output clock signal PSRD may show a waveform diagram corresponding to a low-frequency portion as shown in FIG. 20.

(165) When the frequency of the to-be-detected clock signal CK is greater than the detection-point frequency in the pulse-narrowing circuit **10**, the narrowed output clock signal PSRD may show a waveform diagram corresponding to a high-frequency portion as shown in FIG. 20.

(166) As shown in FIG. 21, when the judging-and-sampling circuit **20** samples the waveform diagram corresponding to the low-frequency portion in FIG. 20, the judging-and-sampling circuit **20** continuously samples the narrowed output clock signal PSRD by employing a time point corresponding to a falling edge of the two-frequency division clock signal CKDIV2 and the obtained narrowed output clock signals PSRD are all the logic high levels, the outputted frequency indication signal FREDET is 1. When the frequency indication signal FREDET is 1, it is determined that the frequency of the to-be-detected clock signal CK is less than the detection-point frequency.

(167) As shown in FIG. 22, when the judging-and-sampling circuit **20** samples the waveform diagram corresponding to the high-frequency portion in FIG. 20, the judging-and-sampling circuit **20** continuously samples the narrowed output clock signal PSRD by employing the time point corresponding to the falling edge of the two-frequency division clock signal CKDIV2 and the obtained narrowed output clock signals PSRD are all the logic low levels, the outputted frequency indication signal FREDET is 0. When the frequency indication signal FREDET is 0, it is determined that the frequency of the to-be-detected clock signal CK is greater than the detection-point frequency.

(168) In this embodiment, the frequency division circuit **30** is configured to divide the frequency of the to-be-detected clock signal CK, such that the logic high level and the logic low level in the to-be-detected clock signal CK of which the frequency is divided have the same duration. Thus, the result of the frequency detection may be not influenced by the duty cycle of the to-be-detected clock signal CK. The frequency division circuit is configured to prevent a mistake caused by a duty cycle deviation in response to the duty cycle of the to-be-detected clock signal CK being other than 50%. For example, a width of the logic high level or a width of the logic low level of the clock signal after two-frequency division from the to-be-detected clock signal CK (i.e., CKDIV2) equals to the period of the to-be-detected clock signal CK, respectively. Thus, the duty cycle is certainly 50%. A frequency division by even number is allowed. In some embodiments, the two-frequency division (i.e., frequency-halving) is adopted.

(169) In some embodiments, in order to ensure that the frequency of the clock signal is smoothly detected, as shown in FIG. 23, the frequency-detecting circuit **100** includes the pulse-narrowing

circuit **10**, the judging-and-sampling circuit **20**, and a delay circuit **40**.

(170) The delay circuit **40** is configured to receive the to-be-detected clock signal CK, delay the to-be-detected clock signal CK, and output a delayed to-be-detected clock signal CK. The pulse-narrowing circuit **10** is coupled to an output terminal of the delay circuit and configured to perform the at least one pulse narrowing process for the delayed to-be-detected clock signal CK to obtain the narrowed output clock signal PSRD.

(171) The judging-and-sampling circuit **20** is configured to sample the narrowed output clock signal PSRD by employing the to-be-detected clock signal CK as the sampling clock signal, to obtain the frequency indication signal FREDET. The frequency indication signal FREDET indicates the value range of the frequency of the to-be-detected clock signal CK.

(172) The pulse-narrowing circuit **10** and the judging-and-sampling circuit **20** in this embodiment may be the same with pulse-narrowing circuit **10** and the judging-and-sampling circuit **20** described in any embodiment described above.

(173) In this embodiment, the delay circuit **40** is configured to delay the to-be-detected clock signal CK, such that the narrowed output clock signal PSRD may have the time difference relative to the to-be-detected clock signal CK, and a successful sample may be achieved.

(174) As shown in FIG. **24**, FIG. **24** is a structural schematic view of an electronic device according to an embodiment of the present disclosure. The electronic device **500** includes the frequency-detecting circuit **100** described in any embodiment above. Of course, the electronic device **500** may be a storage apparatus. The storage apparatus may be a Dynamic Random Access Memory (DRAM), such as a Double Data Rate (DDR) Synchronous Dynamic Random-Access Memory (SDRAM).

(175) As shown in FIG. **25**, FIG. **25** is a structural schematic view of the electronic device according to another embodiment of the present disclosure. The electronic device **500** includes the frequency-detecting circuit **100** and a Delay-locked Loop (DLL) circuit **200**.

(176) The DLL circuit **200** is coupled to the frequency-detecting circuit **100** and configured to adjust a circuit parameter of the DLL circuit **200** based on the frequency indication signal with the to-be-detected clock signal as an input clock. For example, the frequency indication signal FREDET outputted by the frequency-detecting circuit **100** may allow the DLL circuit **200** to adjust the circuit parameter of the DLL circuit **200** in response to the to-be-detected clock signal CK being the low frequency.

(177) For example, since the DLL in the DRAM faces a wide locked frequency range, some characteristic parameters of a DLL system are required to be adjusted according to a variation of an input frequency to improve a performance. For instance, a greater sampling frequency is not suggested to be selected as a loop-locked sampling frequency at the low frequency, otherwise a particularly long DLL locking time may be caused. Thus, the frequency-detecting circuit **100** described above may be selected to generate the frequency indication signal FREDET, to switch the sampling frequency of the DLL.

(178) In some embodiments, the circuit parameter includes the sampling frequency, and the DLL circuit **200** is configured to reduce the sampling frequency in response to the to-be-detected clock signal being less than the detection-point frequency.

(179) In other embodiments, the circuit parameter includes a delay-line delay, and the DLL circuit **200** is configured to increase the delay-line delay in response to the to-be-detected clock signal being less than the detection-point frequency.

(180) For example, the DLL circuit **200** is configured to control an output voltage of a low dropout regulator (LDO) supplying the DLL circuit **200** to be increased or decreased. The delay-line delay varies with the output voltage of the LDO varying. When the frequency of the to-be-detected clock signal CK is the low frequency (e.g. less than the detection-point frequency), the frequency indication signal FREDET controls the output voltage of the LDO to be reduced, and the delay-line delay is in turn increased.

(181) For another example, a MOS capacitor of a delay line node configured to control an on or off of the DLL is controlled. The frequency indication signal FREDET controls a substrate voltage of the MOS capacitor. When the frequency indication signal FREDET is 1, the MOS capacitor is turned off, and the delay-line delay is reduced. When the frequency indication signal FREDET is 0, the MOS capacitor is turned on, and the delay-line delay is increased. In this way, a purpose of changing the delay-line delay is achieved.

(182) When achieved in a form of a soft function unit and is sold or used as a separate product, the embodiments of the present disclosure may be stored in a computer-readable storage medium. Based on such concept, an essential part of the technical solutions of the present disclosure or a part of the technical solutions essentially contributes to the prior art, or a part or a whole of the technical solutions may be embodied in a form of a software product. The computer software product is stored in the storage medium and includes a number of instructions to cause a computer device (e.g., a personal computer, a server, or a network device, etc.) or a processor to perform all or some of the steps of the method described in various embodiments of the present disclosure. The aforementioned storage media include a U disk, a removable hard disk, a ROM, a RAM, a disk, or a CD-ROM, and other media capable of storing program codes.

(183) The scope of the present disclosure is not limited to the above descriptions which are only specific embodiments of the present disclosure. Any equivalent structure or equivalent process transformation using the specification and the accompanying drawings of the present disclosure, or direct or indirect application in other related technical fields, is included in the scope of the present disclosure.

Claims

1. A frequency-detecting circuit, comprising: a pulse-narrowing circuit, configured to receive a to-be-detected clock signal, and perform at least one pulse-narrowing process for the to-be-detected clock signal, wherein the pulse-narrowing circuit has at least one detection-point frequency, and the pulse-narrowing circuit is configured to narrow the to-be-detected clock signal based on the detection-point frequency to obtain a narrowed output clock signal; and a judging-and-sampling circuit, coupled to the pulse-narrowing circuit, and configured to sample the narrowed output clock signal by employing the to-be-detected clock signal as a sampling clock signal to obtain a frequency indication signal, wherein the frequency indication signal is configured to indicate whether the to-be-detected clock signal is greater than the detection-point frequency.
2. The frequency-detecting circuit according to claim 1, wherein each of the at least one pulse-narrowing process is configured to perform a first inversion for a current-level input clock signal, control a rising speed of a rising edge of a level transition or a falling speed of a falling edge of the level transition in a process of the first inversion to obtain a first inverted clock signal, and perform a second inversion for the first inverted clock signal to obtain a current-level narrowed output clock signal.
3. The frequency-detecting circuit according to claim 1, wherein the to-be-detected clock signal is determined to have a frequency higher than the detection-point frequency, in response to the whole of the frequency indication signal being a first logic signal; or the to-be-detected clock signal is determined to have a frequency less than the detection-point frequency, in response to the whole of the frequency indication signal being a second logic signal.
4. The frequency-detecting circuit according to claim 1, wherein the pulse-narrowing circuit comprises M pulse-narrowing units, each of the pulse-narrowing units is coupled to a previous pulse-narrowing unit, and configured to perform one of the at least one pulse narrowing process by employing a previous-level narrowed output clock signal of the previous pulse-narrowing unit as a current-level input clock signal thereof, so as to obtain a current-level narrowed output clock signal; wherein M is a natural number greater than 1; and the first one of the M pulse-narrowing

units is configured to receive the to-be-detected clock signal, and perform the first one of the at least one pulse narrowing process by employing the to-be-detected clock signal as a first-level input clock signal thereof.

5. The frequency-detecting circuit according to claim 4, wherein the pulse-narrowing circuit is configured to provide N detection-point frequencies to obtain N narrowed output clock signals, wherein a coupling point between any of the pulse-narrowing units and a next-level pulse-narrowing unit thereof, and/or an outputting terminal of the last-level pulse-narrowing unit is able to be an outputting terminal of the pulse-narrowing circuit for outputting a narrowed output clock signal in an individual path, and each narrowed output clock signal in each individual path corresponds to a corresponding detection-point frequency, which is determined by pulse-narrowing units previous to a corresponding outputting terminal of the pulse-narrowing circuit in each individual path; wherein the judging-and-sampling circuit comprises N judging-and-sampling units, wherein each of the judging-and-sampling units is coupled to a corresponding one of outputting terminals of the pulse-narrowing circuit, to receive a narrowed output clock signal in a corresponding individual path, and receive the to-be-detected clock signal, so as to obtain a corresponding frequency indication signal in an individual path; wherein N frequency indication signals are configured to indicate a frequency range of the to-be-detected clock signal, and N is a natural number less than or equal to M.

6. The frequency-detecting circuit according to claim 4, wherein each of the pulse-narrowing units comprises: a first inversion circuit, being a delayed inversion circuit, and configured to perform a first inversion for a received input clock signal, and control a rising speed of a rising edge of a level transition or a falling speed of a falling edge of the level transition by a current-limiting element in a process of the first inversion, to obtain a first inverted clock signal; and a second inversion circuit, being a threshold inversion circuit, and configured to perform a second inversion for the first inverted clock signal to obtain a narrowed output clock signal.

7. The frequency-detecting circuit according to claim 6, wherein in response to controlling the rising speed of the rising edge of the level transition, the first inversion circuit comprises: a first switching transistor, having a first terminal configured to receive an operating voltage; a second switching transistor, having a first terminal coupled to a second terminal of the first switching transistor; a third switching transistor, having a first terminal coupled to a second terminal of the second switching transistor, and a second terminal grounded; and a capacitor, having a first terminal coupled to the first terminal of the third switching transistor, and a second terminal grounded; wherein a control terminal of the first switching transistor, a control terminal of the second switching transistor, and a control terminal of the third switching transistor are configured to receive the to-be-detected clock signal; the third switching transistor is controlled to be turned on to discharge the capacitor in response to the to-be-detected clock signal being a logic high level; and the first switching transistor and the second switching transistor are controlled to be turned on to charge the capacitor in response to the to-be-detected clock signal being a logic low level, and the second switching transistor is served as the current-limiting element and configured to control the rising speed of the rising edge of the level transition so as to obtain the first inverted clock signal; or wherein the first inversion circuit comprises: a first switching transistor, having a first terminal configured to receive an operating voltage; a resistor, having a first terminal coupled to a second terminal of the first switching transistor; a second switching transistor, having a first terminal coupled to a second terminal of the resistor, and a second terminal grounded; and a capacitor, having a first terminal coupled to the first terminal of the second switching transistor, and a second terminal grounded; wherein a control terminal of the first switching transistor and a control terminal of the second switching transistor are configured to receive the to-be-detected clock signal; the second switching transistor is controlled to be turned on to discharge the capacitor in response to the to-be-detected clock signal being a logic high level; and the first switching transistor is controlled to be turned on to charge the capacitor in response to the to-be-detected

clock signal being a logic low level, and the resistor is served as the current-limiting element and configured to control the rising speed of the rising edge of the level transition so as to obtain the first inverted clock signal; or wherein the first inversion circuit comprises: a current source; a first switching transistor, having a first terminal coupled to the current source; a second switching transistor, having a first terminal coupled to a second terminal of the first switching transistor, and a second terminal grounded; and a capacitor, having a first terminal coupled to the first terminal of the second switching transistor, and a second terminal grounded; wherein a control terminal of the first switching transistor and a control terminal of the second switching transistor are configured to receive the to-be-detected clock signal; the second switching transistor is controlled to be turned on to discharge the capacitor in response to the to-be-detected clock signal being a logic high level; and the first switching transistor is controlled to be turned on to charge the capacitor in response to the to-be-detected clock signal being a logic low level, and the current source is served as the current-limiting element and configured to control the rising speed of the rising edge of the level transition so as to obtain the first inverted clock signal.

8. The frequency-detecting circuit according to claim 6, wherein in response to controlling the falling speed of the falling edge of the level transition, the first inversion circuit comprises: a first switching transistor, having a first terminal configured to receive an operating voltage; a second switching transistor, having a first terminal coupled to a second terminal of the first switching transistor; a third switching transistor, having a first terminal coupled to a second terminal of the second switching transistor, and a second terminal grounded; and a capacitor, having a first terminal coupled to the first terminal of the second switching transistor, and a second terminal grounded; wherein a control terminal of the first switching transistor, a control terminal of the second switching transistor, and a control terminal of the third switching transistor are configured to receive the to-be-detected clock signal; the first switching transistor is controlled to be turned on to charge the capacitor in response to the to-be-detected clock signal being a logic low level; and the first switching transistor and the second switching transistor are controlled to be turned on to discharge the capacitor in response to the to-be-detected clock signal being a logic high level, and the second switching transistor is served as the current-limiting element and configured to control the falling speed of the falling edge of the level transition so as to obtain the first inverted clock signal; or wherein the first inversion circuit comprises: a first switching transistor, having a first terminal configured to receive an operating voltage; a resistor, having a first terminal coupled to a second terminal of the first switching transistor; a second switching transistor, having a first terminal coupled to a second terminal of the resistor, and a second terminal grounded; and a capacitor, having a first terminal coupled to the first terminal of the resistor, and a second terminal grounded; wherein a control terminal of the first switching transistor and a control terminal of the second switching transistor are configured to receive the to-be-detected clock signal; the first switching transistor is controlled to be turned on to charge the capacitor in response to the to-be-detected clock signal being a logic low level; and the second switching transistor is controlled to be turned on to discharge the capacitor in response to the to-be-detected clock signal being a logic high level, and the resistor is served as the current-limiting element and configured to control the falling speed of the falling edge of the level transition so as to obtain the first inverted clock signal; or wherein the first inversion circuit comprises: a first switching transistor, having a first terminal configured to receive an operating voltage; a second switching transistor, having a first terminal coupled to a second terminal of the first switching transistor; a capacitor, having a first terminal coupled to the first terminal of the second switching transistor; and a current source, having a first terminal coupled to a second terminal of the capacitor, and a second terminal grounded; wherein a control terminal of the first switching transistor and a control terminal of the second switching transistor are configured to receive the to-be-detected clock signal; the first switching transistor is controlled to be turned on to charge the capacitor in response to the to-be-detected clock signal being a logic low level; and the second switching transistor is controlled to be turned on to

discharge the capacitor in response to the to-be-detected clock signal being a logic high level, and the current source is served as the current-limiting element and configured to control the falling speed of the falling edge of the level transition so as to obtain the first inverted clock signal.

9. The frequency-detecting circuit according to claim 1, further comprising: a frequency division circuit, configured to receive the to-be-detected clock signal, divide the frequency of the to-be-detected clock signal, and output a frequency division clock signal; wherein the pulse-narrowing circuit is coupled to an output terminal of the frequency division circuit and configured to perform the at least one pulse-narrowing process for the frequency division clock signal to obtain the narrowed output clock signal.

10. The frequency-detecting circuit according to claim 1, further comprising: a delay circuit, configured to receive the to-be-detected clock signal, delay the to-be-detected clock signal, and output a delayed to-be-detected clock signal; wherein the pulse-narrowing circuit is coupled to an output terminal of the delay circuit and configured to perform the at least one pulse narrowing process for the delayed to-be-detected clock signal to obtain the narrowed output clock signal.

11. An electronic device, wherein the electronic device comprises a frequency-detecting circuit comprising: a pulse-narrowing circuit, configured to receive a to-be-detected clock signal, and perform at least one pulse-narrowing process for the to-be-detected clock signal, wherein the pulse-narrowing circuit has at least one detection-point frequency, and the pulse-narrowing circuit is configured to narrow the to-be-detected clock signal based on the detection-point frequency to obtain a narrowed output clock signal; and a judging-and-sampling circuit, coupled to the pulse-narrowing circuit, and configured to sample the narrowed output clock signal by employing the to-be-detected clock signal as a sampling clock signal to obtain a frequency indication signal, wherein the frequency indication signal is configured to indicate whether the to-be-detected clock signal is greater than the detection-point frequency.

12. The electronic device according to claim 11, further comprising: a Delay-Locked Loop (DLL) circuit, coupled to the frequency-detecting circuit and configured to adjust a circuit parameter of the DLL circuit based on the frequency indication signal with the to-be-detected clock signal as an input clock.

13. The electronic device according to claim 12, wherein the circuit parameter comprises a sampling frequency, and the DLL circuit is configured to reduce the sampling frequency in response to the to-be-detected clock signal being less than the detection-point frequency.

14. The electronic device according to claim 12, wherein the circuit parameter comprises a delay-line delay, and the DLL circuit is configured to increase the delay-line delay in response to the to-be-detected clock signal being less than the detection-point frequency.

15. The electronic device according to claim 11, wherein each of the at least one pulse-narrowing process is configured to perform a first inversion for a current-level input clock signal, control a rising speed of a rising edge of a level transition or a falling speed of a falling edge of the level transition in a process of the first inversion to obtain a first inverted clock signal, and perform a second inversion for the first inverted clock signal to obtain a current-level narrowed output clock signal.

16. The electronic device according to claim 11, wherein the to-be-detected clock signal is determined to have a frequency higher than the detection-point frequency, in response to the whole of the frequency indication signal being a first logic signal; or the to-be-detected clock signal is determined to have a frequency less than the detection-point frequency, in response to the whole of the frequency indication signal being a second logic signal.

17. The electronic device according to claim 11, wherein the pulse-narrowing circuit comprises M pulse-narrowing units, each of the pulse-narrowing units is coupled to a previous pulse-narrowing unit, and configured to perform one of the at least one pulse narrowing process by employing a previous-level narrowed output clock signal of the previous pulse-narrowing unit as a current-level input clock signal thereof, so as to obtain a current-level narrowed output clock signal; wherein M

is a natural number greater than 1; and the first one of the M pulse-narrowing units is configured to receive the to-be-detected clock signal, and perform the first one of the at least one pulse narrowing process by employing the to-be-detected clock signal as a first-level input clock signal thereof.

18. The electronic device according to claim 17, wherein the pulse-narrowing circuit is configured to provide N detection-point frequencies to obtain N narrowed output clock signals, wherein a coupling point between any of the pulse-narrowing units and a next-level pulse-narrowing unit thereof, and/or an outputting terminal of the last-level pulse-narrowing unit is able to be an outputting terminal of the pulse-narrowing circuit for outputting a narrowed output clock signal in an individual path, and each narrowed output clock signal in each individual path corresponds to a corresponding detection-point frequency, which is determined by pulse-narrowing units previous to a corresponding outputting terminal of the pulse-narrowing circuit in each individual path; wherein the judging-and-sampling circuit comprises N judging-and-sampling units, wherein each of the judging-and-sampling units is coupled to a corresponding one of outputting terminals of the pulse-narrowing circuit, to receive a narrowed output clock signal in a corresponding individual path, and receive the to-be-detected clock signal, so as to obtain a corresponding frequency indication signal in an individual path; wherein N frequency indication signals are configured to indicate a frequency range of the to-be-detected clock signal, and N is a natural number less than or equal to M.

19. The electronic device according to claim 17, wherein each of the pulse-narrowing units comprises: a first inversion circuit, being a delayed inversion circuit, and configured to perform a first inversion for a received input clock signal, and control a rising speed of a rising edge of a level transition or a falling speed of a falling edge of the level transition by a current-limiting element in a process of the first inversion, to obtain a first inverted clock signal; and a second inversion circuit, being a threshold inversion circuit, and configured to perform a second inversion for the first inverted clock signal to obtain a narrowed output clock signal.

20. The electronic device according to claim 11, wherein the frequency-detecting circuit further comprises: a frequency division circuit, configured to receive the to-be-detected clock signal, divide the frequency of the to-be-detected clock signal, and output a frequency division clock signal; wherein the pulse-narrowing circuit is coupled to an output terminal of the frequency division circuit and configured to perform the at least one pulse-narrowing process for the frequency division clock signal to obtain the narrowed output clock signal.
