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SEMICONDUCTOR DEVICE PACKAGE AND METHOD OF MANUFACTURING THE SAME

Abstract

A semiconductor device package includes a first substrate, a second substrate, and a first electronic component between the first substrate and the second substrate. The first electronic component has a first surface facing the first substrate and a second surface facing the second substrate. The semiconductor device package also includes a first electrical contact disposed on the first surface of the first electronic component and electrically connecting the first surface of the first electronic component with the first substrate. The semiconductor device package also includes a second electrical contact disposed on the second surface of the first electronic component and electrically connecting the second surface of the first electronic component with the second substrate. A method of manufacturing a semiconductor device package is also disclosed.

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATION 1. Technical Field [0001] This application is a continuation of U.S. patent application Ser. No. 18/440,919, filed Feb. 13, 2024, now U.S. Pat. No. 12,300,560, which is a continuation of U.S. patent application Ser. No. 17/883,550, filed Aug. 8, 2022, now U.S. Pat. No. 11,901,252, which is a continuation of U.S. patent application Ser. No. 16/572,340 filed Sep. 16, 2019, now U.S. Pat. No. 11,410,902, the contents of which are incorporated herein by reference in their entirety.

BACKGROUND
1. Technical Field
[0002] The present disclosure generally relates to a semiconductor device package and a method of manufacturing the same, and to a semiconductor device package including an electronic component and a method of manufacturing the same.
2. Description of the Related Art
[0003] Package on Package (POP) technique can be used to combine discrete packages, and usually composed of two packages, such as a memory device mounted on top of a logic device, connected through an interposer.
SUMMARY
[0004] In one or more embodiments, a semiconductor device package includes a first substrate, a second substrate, and a first electronic component between the first substrate and the second substrate. The first electronic component has a first surface facing the first substrate and a second surface facing the second substrate. The semiconductor device package also includes a first electrical contact disposed on the first surface of the first electronic component and electrically connecting the first surface of the first electronic component with the first substrate. The semiconductor device package also includes a second electrical contact disposed on the second surface of the first electronic component and electrically connecting the second surface of the first electronic component with the second substrate.
[0005] In one or more embodiments, a semiconductor device package includes a first substrate and a first electronic component disposed on the first substrate. The first electronic component has an active surface facing the first substrate and a backside surface opposite to the active surface. The semiconductor device package also includes a first redistribution layer (RDL) disposed on the backside surface of the first electronic component. The semiconductor device package also

includes a conductive via penetrating the first electronic component and electrically connecting the active surface of the first electronic component with the RDL.
[0006] In one or more embodiments, a method of manufacturing a semiconductor device package includes providing an electronic component. The electronic component has a first surface and a second surface opposite to the first surface. The method also includes disposing a first electrical contact on the first surface of the electronic component. The method also includes disposing the electronic component on a first substrate. The first electrical contact is between the electronic component and the first substrate. The method also includes providing an electronic structure on the second surface of the electronic component. The electronic structure includes a second electrical contact electrically connected with the first electrical contact.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0007] Aspects of the present disclosure are readily understood from the following detailed description when read with the accompanying figures. It should be noted that various features may not be drawn to scale. The dimensions of the various features May be arbitrarily increased or reduced for clarity of discussion.
[0008] FIG. **1** illustrates a cross-sectional view of a semiconductor device package in accordance with some embodiments of the present disclosure.
[0009] FIG. **2** illustrates a cross-sectional view of a semiconductor device package in accordance with some embodiments of the present disclosure.
[0010] FIG. **3** illustrates a cross-sectional view of a semiconductor device package in accordance with some embodiments of the present disclosure.
[0011] FIG. **4**A illustrates one or more stages of a method of manufacturing a semiconductor device package in accordance with some embodiments of the present disclosure.
[0012] FIG. **4**B illustrates one or more stages of a method of manufacturing a semiconductor device package in accordance with some embodiments of the present disclosure.
[0013] FIG. **4**C illustrates one or more stages of a method of manufacturing a semiconductor device package in accordance with some embodiments of the present disclosure.
[0014] FIG. **4**D illustrates one or more stages of a method of manufacturing a semiconductor device package in accordance with some embodiments of the present disclosure.
[0015] FIG. **4**E illustrates one or more stages of a method of manufacturing a semiconductor device package in accordance with some embodiments of the present disclosure.
[0016] FIG. **4**F illustrates one or more stages of a method of manufacturing a semiconductor device package in accordance with some embodiments of the present disclosure.
[0017] FIG. **4**G illustrates one or more stages of a method of manufacturing a semiconductor device package in accordance with some embodiments of the present disclosure.
[0018] FIG. **4**H illustrates one or more stages of a method of manufacturing a semiconductor device package in accordance with some embodiments of the present disclosure.
[0019] FIG. **4**I illustrates one or more stages of a method of manufacturing a semiconductor device package in accordance with some embodiments of the present disclosure.
[0020] FIG. **5**A illustrates one or more stages of a method of manufacturing a semiconductor device package in accordance with some embodiments of the present disclosure.
[0021] FIG. **5**B illustrates one or more stages of a method of manufacturing a semiconductor device package in accordance with some embodiments of the present disclosure.
[0022] FIG. **5**C illustrates one or more stages of a method of manufacturing a semiconductor device package in accordance with some embodiments of the present disclosure.
[0023] FIG. **5**D illustrates one or more stages of a method of manufacturing a semiconductor

device package in accordance with some embodiments of the present disclosure.
[0024] Common reference numerals are used throughout the drawings and the detailed description to indicate the same or similar elements. The present disclosure will be more apparent from the following detailed description taken in conjunction with the accompanying drawings.
DETAILED DESCRIPTION
[0025] The following disclosure provides for many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below. These are, of course, merely examples and are not intended to be limiting. In the present disclosure, reference to the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. Besides, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.
[0026] Embodiments of the present disclosure are discussed in detail below. It should be appreciated, however, that the present disclosure provides many applicable concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative and do not limit the scope of the disclosure.
[0027] FIG. **1** illustrates a cross-sectional view of a semiconductor device package **1** in accordance with some embodiments of the present disclosure. The semiconductor device package **1** includes electronic components **10** and **11**, substrates **12** and **14**, an interposer **13**, and encapsulating layers **15** and **16**.
[0028] Each of the substrates **12** and **14** may be, for example, a printed circuit board, such as a paper-based copper foil laminate, a composite copper foil laminate, or a polymer-impregnated glass-fiber-based copper foil laminate. Each of the substrates **12** and **14** may be, or may include, an interconnection structure, such as a redistribution layer (RDL) or a grounding element.
[0029] The substrate **12** has a surface **121** and a surface **122** opposite to the surface **121**. The substrate **12** may include one or more conductive pads **12***p* in proximity to, adjacent to, or embedded in and exposed at the surface **121** of the substrate **12**. The substrate **12** may include a solder resist (not shown) on the surface **12** of the substrate **12** to fully expose or to expose at least a portion of the conductive pads **12***p* for electrical connections. Electrical contact **12***b***1** (e.g. a solder ball) is disposed on the conductive pads **12***p* and can provide electrical connections between the semiconductor package device **1** and external components (e.g. external circuits or circuit boards). In some embodiments, the electrical contact **12***b***1** includes a controlled collapse chip connection (C4) bump, a ball grid array (BGA) or a land grid array (LGA). Opposite to the surface **121** of the substrate **12**, an electrical contact **12***b***2** is provided on the surface **122** of the substrate **12** through a solder paste to provide electrical connections to external components.
[0030] The electronic component **10** is disposed on the surface **122** of the substrate **12**. The electronic component **10** may be a chip, a die including a semiconductor substrate, a central processing unit (CPU), a graphics processing unit (GPU), an accelerated processing unit (APU), or the likes. The electronic component **10** may include one or more integrated circuit devices (such as active devices and/or passive devices) and one or more overlying interconnection structures therein. The electronic component **10** may have high input/output (I/O) connections to meet high bandwidth specifications. As shown in FIG. **1**, the electronic component **10** has an electrical contact **10***b* electrically connected to the substrate **12** and an underfill **10***u* surrounding the electrical contact **10***b*. In some embodiments, the electrical contact **10***b* may include a micro bump, a C4 bump, a BGA or a LGA. In some embodiments, the underfill **10***u* may include an epoxy resin, a molding compound (e.g., an epoxy molding compound or other molding compound), a polyimide

(PI), a phenolic compound or material, a material including a silicone dispersed therein, or a combination thereof.

[0031] The encapsulating layer **15** is disposed on the surface **122** of the substrate **12** to cover and encapsulate the electronic component **10**. In some embodiments, the encapsulating layer **15** may include, for example, one or more organic materials (e.g., a molding compound, bismaleimide triazine (BT), a PI, a polybenzoxazole (PBO), a solder resist, an Ajinomoto build-up film (ABF), a polypropylene (PP), an epoxy-based material, or a combination of two or more thereof), inorganic materials (e.g., silicon, a glass, a ceramic, a quartz, or a combination of two or more thereof), liquid-film material(s) or dry-film material(s), or a combination of two or more thereof.

[0032] Similar to the substrate **12**, the substrate **14** has a surface **141** facing the surface **122** and a surface **142** opposite to the surface **141**. The substrate **14** may include one or more conductive pads **14***p*. Electrical contact **14***b* is disposed on the conductive pads **14***p* to provide electrical connections to external components.

[0033] The electronic component **11** is disposed on the surface **142** of the substrate **14** and electrically connected with the substrate **14** through a flip-chip technique, a wire bonding technique (e.g., through a wire **11***w*), or other suitable technique. The electronic component **11** may be a chip, a die including a semiconductor substrate, a semiconductor memory (e.g., a dynamic random-access memory (DRAM)), or the likes.

[0034] The encapsulating layer **16** is disposed on the surface **142** of the substrate **14** to cover and encapsulate the electronic component **11**. In some embodiments, the encapsulating layer **16** may include a material as noted above for the encapsulating layer **15**.

[0035] The electronic component **10**, encapsulated in the encapsulating layer **15** and disposed on the substrate **12**, is electronically connected to the electronic component **11**, encapsulated in the encapsulating layer **16** and disposed on the substrate **14**, through the interposer **13** and an electrical contact **13***b* provided thereon. The interposer **13** is disposed between the electronic component **10** and the substrate **14**. The interposer **13** may include, for example, a printed circuit board, such as a paper-based copper foil laminate, a composite copper foil laminate, or a polymer-impregnated glass-fiber-based copper foil laminate. The interposer **13** may be, or may include, an interconnection structure, such as a RDL or a grounding element.

[0036] A sum of a thickness of the interposer **13** and a gap between the surface **141** and the interposer **13** is equal to or greater than 200 micrometer (μm), 230 μm, 250 μm, or more. A sum of the thickness of the semiconductor device package **1** is equal to or greater than 1.0 μm, 1.03 μm, 1.06 μm, or more.

[0037] With the interposer **13** in the semiconductor device package **1**, the memory device (such as the electronic component **11**) can be electrically connected to the logic device (such as the electronic component **10**) by vertically stacking to each other through package-on-package (PoP) technique. However, as technology advances, a semiconductor device package having a further reduced thickness is desired. In addition, as shown in the FIG. **1**, the current from the electric component **10** to the electric component **11** flows through the electrical contact **10***b*, the substrate **12**, the electrical contact **12***b***2**, the electrical contact **13***b*, the substrate **13**, the electrical contact **14***b*, the substrate **14**, and the wire **11***w*. As technology advances, chips are provided with relatively more I/O connections in, for examples, High Bandwidth Package on Package (HBPoP). The length of the circuit loop in the semiconductor device package **1** of FIG. **1** is long and may adversely affect the performance thereof.

[0038] FIG. **2** illustrates a cross-sectional view of a semiconductor device package **2** in accordance with some embodiments of the present disclosure. The semiconductor device package **2** includes electronic components **20** and **21**, substrates **22**, and **23**, and encapsulating layers **24** and **25**.

[0039] The substrate **22** may have a material and/or a configuration as noted above for the substrates **12** and **14** in FIG. **1**, and may have a conductive layer **22***r*. As shown in FIG. **2**, the substrate **22** has a surface **221**, a surface **222** opposite to the surface **221**, and a surface **223** (such as

a lateral surface) connected between the surfaces **221** and **222**. Electrical contacts **22***b***1** and **22***b***2** are disposed on the surfaces **221** and **222** of the substrate **22** to provide electrical connections to external components.

[0040] The electronic component **20** may have a material and/or a configuration as noted above for the electronic component **10** in FIG. **1**. The electronic component **20** is disposed on the surface **222** of the substrate **22**. The electronic component **20** has a surface **201** (such as an active surface) facing the substrate **22** and a surface **202** (such as a backside surface) opposite to the surface **201**. The electronic component **20** includes an interconnection structure **20***r***1** (such as a RDL) on the surface **201**. The electronic component **20** includes an interconnection structure **20***r***2** on the surface **202**. The electronic component **20** includes a conductive via **20***t* (such as a through silicon via (TSV)) therewithin and electrically connected the interconnection structure **20***r***1** to the interconnection structure **20***r***2**. An electrical contact **20***b* (surrounded by an underfill **20***u*) is provided on the interconnection structure **20***r***1**.

[0041] The interconnection structure **20***r***1** and the electrical contact **20***b* provide the electrical connection between the electronic component **20** and the substrate **22**. In some embodiments, the electronic component **20** is devoid of the interconnection structure **20***r***1** on the surface **201**, and the electrical contact **20***b* is provided on the surface **201** of the electronic component **20**.

[0042] The interconnection structure **20***r***2** and the electrical contact **23***b* (disposed on a surface **231** of the substrate **23**) provide the electrical connection between the electronic component **20** and the substrate **23**.

[0043] A buffer layer **26** is disposed between the interconnection structure **20***r***2** and the substrate **23**. The buffer layer **26** may include an adhesive, a glue, or other suitable material, such as a material for die-attaching.

[0044] Still referring to FIG. **2**, the substrate **23** may have a material and/or a configuration as noted above for the substrates **12** and **14** in FIG. **1**, and may have a conductive layer **23***r*. As shown in FIG. **2**, the substrate **23** has a surface **231** facing the surface **202**, a surface **232** opposite to the surface **231**, and a surface **233** (such as a lateral surface) connected between the surfaces **231** and **232**. The electrical contact **23***b* is disposed on the surfaces **231** of the substrate **23** to provide the electrical connection to the electronic component **20** and the substrate **22**.

[0045] The electronic component **21** may have a material and/or a configuration as noted above the electronic component **11** in FIG. **1**. The electronic component **21** is disposed on the surface **232** of the substrate **23** and electrically connected with the substrate **23** through a flip-chip technique, a wire bonding technique (e.g., through a wire **21***w*), other suitable techniques.

[0046] The encapsulating layer **25** may have a material and/or a configuration as noted above for the encapsulating layer **16** in FIG. **1**. The encapsulating layer **25** is disposed on the surface **232** of the substrate **23** to cover and encapsulate the electronic component **21**. As shown in FIG. **2**, the encapsulating layer **25** has a surface **251** substantially coplanar with the surface **233** of the substrate **23**. The surface **251** of the encapsulating layer **25** and the surface **233** of the substrate **23** are in contact with the encapsulating layer **24**.

[0047] The encapsulating layer **24** may have the same material as encapsulating layer **25**. In some embodiments, the encapsulating layer **24** and the encapsulating layer **25** may have different materials.

[0048] The encapsulating layer **24** is disposed on the surface **222** of the substrate **22** to cover and encapsulate the electronic component **20**. The encapsulating layer **24** surrounds the electronic component **20**, the substrate **23**, and the encapsulating layer **25**. The encapsulating layer **24** includes a surface **241** substantially coplanar with the surface **223** of the substrate **22**. The surface **241** of the encapsulating layer **24** and the surface **223** of the substrate **22** are spaced apart from the surface **251** of the encapsulating layer **25** and the surface **233** of the substrate **23**. The surface **241** of the encapsulating layer **24** and the surface **223** of the substrate **22** surround the surface **251** of the encapsulating layer **25** and the surface **233** of the substrate **23**. The surface **251** of the encapsulating

layer **25** and the surface **233** of the substrate **23** is recessed from the surface **241** of the encapsulating layer **24** and the surface **223** of the substrate **22**. The surface **251** of the encapsulating layer **25** and the surface **233** of the substrate **23** is surrounded by the surface **241** of the encapsulating layer **24** and the surface **223** of the substrate **22**.

[0049] The electrical contact **23***b* provided on the surface **231** of the substrate **23** may be stacked on the electrical contact **22***b***2** over the surface **222** of the substrate **22**. The electrical contact **23***b* stacked on the electrical contact **22***b***2** is disposed next to the electronic component **20**. In some embodiments, the electrical contact **23***b* stacked on the electrical contact **22***b***2** may be replaced with a solder ball or a cupper (Cu) pillar.

[0050] The current from the electric component **20** may flow to the electric component **21** through the interconnection structure **20***r***1**, the conductive via **20***t*, the interconnection structure **20***r***2**, the electrical contact **23***b*, the conductive layer **23***r* in the substrate **23**, and the wire **21***w*. The circuit loop in the semiconductor device package **2** of FIG. **2** is shorter than the circuit loop in the semiconductor device package **1** of FIG. **1**, which helps to achieve a better performance thereof. The current from the electric component **20** may also flow to the electric component **21** through the electrical contact **20***b*, the substrate **22**, and the electrical contacts **22***b***2** and **23***b* (which is a circuit loop similar to that in the semiconductor device package **1** of FIG. **1**). By this way, the current from the electric component **20** can be distributed, for example, the current directly passing through the conductive via **20***t* may be used for high-bandwidth transmission, and the current passing through the electrical contacts **22***b***2** and **23***b* may be grounded.

[0051] In addition, since the current may flow from the interconnection structure **20***r***1** to the substrate **23** through the interconnection structure **20***r***2** and the electrical contact **23***b*, an interposer may be omitted in the semiconductor device package **2**, which helps to reduce the thickness of the semiconductor device package **2**.

[0052] FIG. **3** illustrates a cross-sectional view of a semiconductor device package **2**′ in accordance with some embodiments of the present disclosure. The semiconductor device package **2**′ of FIG. **3** is similar to the semiconductor device package **2** of FIG. **2**, and the differences therebetween is described below.

[0053] The encapsulating layer **25**′ may have a material and/or a configuration as noted above for the encapsulating layer **25** in FIG. **2**. The encapsulating layer **25**′ is disposed on the surface **232** of the substrate **23**. The encapsulating layer **25**′ is disposed on a portion of the surface **222** of the substrate **22**.

[0054] The encapsulating layer **24**′ may have a material and/or a configuration as noted above for the encapsulating layer **24** in FIG. **2**. The encapsulating layer **24**′ has a surface **241** substantially coplanar with the surface **233** of the substrate **23**. The surface **241** is in contact with the encapsulating layer **25**′. The surface **241** is surrounded by the encapsulating layer **25**′. The encapsulating layer **25**′ has a surface **251** surrounding the surface **241** of the encapsulating layer **24**′ and the surface **233** of the substrate **23**.

[0055] FIG. **4**A, FIG. **4**B, FIG. **4**C, FIG. **4**D, FIG. **4**E, FIG. **4**F, FIG. **4**G, FIG. **4**H, and FIG. **4**I are cross-sectional views of a semiconductor device package at various stages of fabrication, in accordance with some embodiments of the present disclosure. At least some of these figures have been simplified for a better understanding of the aspects of the present disclosure.

[0056] Referring to FIG. **4**A, an electronic component **20** is provided on a carrier **40**, and an opening **20***r* is formed in the electronic component **20** through a laser drill. The electronic component **20** has a surface **201** (such as an active surface) and a surface **202** (such as a backside surface) opposite to the surface **201**. The electronic component **20** includes an interconnection structure **20***r***1** on the surface **201**. A part of the interconnection structure **20***r***1** is exposed through the opening **20***r*.

[0057] Referring to FIG. **4**B, a conductive via **20***t* is formed in the electronic component **20**. In some embodiments, the conductive via **20***t* may be formed by disposing a conductive material in

the opening **20***r* through sputtering, electroless plating, plating, or other suitable processes. The conductive material may include, for example, gold (Au), silver (Ag), copper (Cu), nickel (Ni), palladium (Pd), another metal, a solder alloy, or a combination of two or more thereof.

[0058] Referring to FIG. **4**C, an interconnection structure **20***r***2** is formed on the surface **202** of the substrate **20**. In some embodiments, the process may be conducted by forming a dielectric layer by, for example, coating, lamination or other suitable processes, patterning the dielectric layer through a photoresist film (or a mask) to form a cavity, and disposing a conductive material in the cavity.

[0059] Referring to FIG. **4**D, the carrier **40** is removed to expose the interconnection structure **20***r***1** on the surface **201** of the substrate **20**. An electrical contact **20***b* is provided on the interconnection structure **20***r***1**. Then, in some embodiments, a singulation may be performed to separate out individual devices. That is, the singulation may be performed through the substrate **20** including the interconnection structures **20***r***1** and **20***r***2**. The singulation may be performed, for example, by using a dicing saw, laser or other appropriate cutting technique

[0060] Referring to FIG. **4**E, disposing the structure obtained from the operations in FIG. **4**A to FIG. **4**D on a surface **222** of a substrate **22**. The electronic component **20** and the substrate **22** are electrically connected through the electrical contact **20***b* and the interconnection structure **20***r***1**. Electrical contact **22***b***1** is provided on a surface **221** of the substrate **22** facing away from the electronic component **20**. Electrical contact **22***b***2** is provided on the surface **222** of the substrate **22** and next to the electronic component **20**. In some embodiments, the top surface of the electrical contact **22***b***2** is higher than or equal to the top surface of the interconnection structure **20***r***2**.

[0061] Referring to FIG. **4**F, an underfill **20***u* is disposed between the electronic component **20** and the substrate **22** to surround the electrical contact **20***b*.

[0062] Referring to FIG. **4**G, a buffer layer **26** is disposed on the interconnection structure **20***r***2**.

[0063] Referring to FIG. **4**H, a substrate **23**, an electronic component **21**, an encapsulating layer **25**, and an electrical contact **23***b* is combined and integrated as a unit **41** (such as an electronic structure). The unit **41** is provided on the substrate **22** and the electronic component **20**. The electrical contact **23***b* is disposed on the electrical contact **22***b***2**. The electrical contact **23***b* is disposed on the interconnection structure **20***r***2**. The unit **41** has a surface (composed of a surface **251** of the encapsulating layer **25** and a surface **233** of the substrate **23**) spaced apart from (or recessed from) a surface **223** of the substrate **22**.

[0064] Referring to FIG. **4**I, an encapsulating layer **24** is provided on the substrate **22** to cover and encapsulate the electronic component **20**. The encapsulating layer **24** is also provided to surround the surface **251** and the surface **233**. In some embodiments, although not shown in the figures, the encapsulating layer **24** may be provided on the top surface of the encapsulating layer **25**. The encapsulating layer **24** may be formed by a molding technique. A singulation may be performed to separate out individual semiconductor package devices. That is, the singulation may be performed through the encapsulating layer **24** and a substrate strip including the substrate **22**. The singulation may be performed, for example, by using a dicing saw, laser or other appropriate cutting technique.

[0065] FIG. **5**A, FIG. **5**B, FIG. **5**C, and FIG. **5**D are cross-sectional views of a semiconductor device package at various stages of fabrication, in accordance with some embodiments of the present disclosure. At least some of these figures have been simplified for a better understanding of the aspects of the present disclosure.

[0066] Referring to FIG. **5**A, the operation in FIG. **5**A may be subsequent to the operation in FIG. **4**G, in which the buffer layer **26** is disposed on the interconnection structure **20***r***2**. In FIG. **5**A, the substrate **23** and the electrical contact **23***b* is provided on the substrate **22** and the electronic component **20**.

[0067] Referring to FIG. **5**B, the electronic component **21** is provided on the substrate **22** through a flip-chip technique, a wire bonding technique (e.g., through a wire **21***w*), or other suitable technique.

[0068] Referring to FIG. **5**C, the encapsulating layer **25** is disposed on the substrate **23** to cover and

encapsulate the electronic component **21**. In some embodiments, the encapsulating layer **25** may be formed by a molding technique, such as transfer molding or compression molding.
[0069] Referring to FIG. **5**D, the encapsulating layer **24** is provided on the substrate **22** to cover and encapsulate the electronic component **20**. The product obtained in the operation in FIG. **5**D is the same as the product obtained in FIG. **4**I. In some embodiments, the encapsulating layer **24** is formed before disposing the encapsulating layer **25**, and the encapsulating layer **25** covers and surrounds the encapsulating layer **24** (such as shown in FIG. **3**). In some embodiments, the formations for the encapsulating layer **24** and the encapsulating layer **25** may be conducted in the same operation. For examples, the encapsulating layer **24** and the encapsulating layer **25** may be formed at the same time.
[0070] Spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper,” “left,” “right” and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation, in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly. It should be understood that when an element is referred to as being “connected to” or “coupled to” another element, it may be directly connected to or coupled to the other element, or intervening elements may be present.
[0071] As used herein, the terms “approximately”, “substantially”, “substantial” and “about” are used to describe and account for small variations. When used in connection with an event or circumstance, the terms can refer to instances in which the event or circumstance occurs precisely as well as instances in which the event or circumstance occurs to a close approximation. As used herein with respect to a given value or range, the term “about” generally means within ±10%, ±5%, ±1%, or ±0.5% of the given value or range. Ranges can be expressed herein as from one endpoint to another endpoint or between two endpoints. All ranges disclosed herein are inclusive of the endpoints unless specified otherwise. The term “substantially coplanar” can refer to two surfaces within micrometers (μm) of lying along the same plane, such as within 10 μm, within 5 μm, within 1 μm, or within 0.5 μm of lying along the same plane. When referring to numerical values or characteristics as “substantially” the same, the term can refer to the values lying within ±10%, ±5%, ±1%, or ±0.5% of an average of the values.
[0072] The foregoing outlines features of several embodiments and detailed aspects of the present disclosure. The embodiments described in the present disclosure may be readily used as a basis for designing or modifying other processes and structures for carrying out the same or similar purposes and/or achieving the same or similar advantages of the embodiments introduced herein. Such equivalent constructions do not depart from the spirit and scope of the present disclosure, and various changes, substitutions, and alterations may be made without departing from the spirit and scope of the present disclosure.

Claims

1. A semiconductor device package, comprising: a first redistribution layer (RDL); an electronic component having a through silicon via (TSV) and disposed over the first RDL; a second redistribution layer (RDL) disposed on a bottom surface of the electronic component; and a solder ball disposed between the first RDL and the second RDL; and an encapsulant encapsulating the electronic component, the second RDL, and the solder ball, wherein the encapsulant overlaps the second RDL and the solder ball in a direction substantially parallel to the bottom surface of the electronic component.
2. The semiconductor device package of claim 1, wherein the encapsulant is over the electronic component.

3. The semiconductor device package of claim 2, wherein the encapsulant has a portion lower than the bottom surface of the electronic component.
4. The semiconductor device package of claim 2, further comprising a plurality of first electrical contacts disposed over the electronic component, wherein the encapsulant extends between the plurality of electrical contacts.
5. The semiconductor device package of claim 4, further comprising a third redistribution layer (RDL) disposed over the plurality of first electrical contacts.
6. The semiconductor device package of claim 5, wherein the third RDL includes a dielectric layer and a circuit layer encapsulated by the dielectric layer, wherein a width of the third RDL is less than a width of the encapsulant in a cross-sectional view.
7. The semiconductor device package of claim 4, further comprising a second electrical contact encapsulated by the encapsulant and laterally overlapping the second RDL, wherein a top surface of the second electrical contact is substantially co-level with a top surface of one of the plurality of first electrical contacts.
8. The semiconductor device package of claim 7, wherein the second electrical contact includes a first portion disposed on the first RDL and a second portion disposed on the first portion, wherein a first width of the second electrical contact at an interface between the first portion and the second portion is less than a second width of the second portion of the second electrical contact.
9. A semiconductor device package, comprising: a first electronic component having a through silicon via (TSV); an electrical contact disposed on the first electronic component; a solder ball disposed under the first electronic component; and a second electronic component disposed on the first electronic component, wherein a width of the solder ball is less than a width of the electrical contact.
10. The semiconductor device package of claim 9, further comprising a first redistribution layer (RDL) disposed between the solder ball and the first electronic component.
11. The semiconductor device package of claim 10, further comprising an encapsulant encapsulating the first electronic component, the solder ball, and the first RDL, wherein the encapsulant extends over the first electronic component.
12. The semiconductor device package of claim 11, wherein the first RDL includes a dielectric layer and a circuit layer partially covered by the dielectric layer, wherein the encapsulant contacts a lateral surface of the dielectric layer of the first RDL.
13. The semiconductor device package of claim 10, further comprising a second redistribution layer (RDL) disposed under the first RDL, wherein a width of the second RDL is greater than a width of the first RDL.
14. A semiconductor device package, comprising: a first electronic component having a through silicon via (TSV); a second electronic component stacked on the first electronic component; and an encapsulant encapsulating and laterally covering the first electronic component and the second electronic component, wherein a thickness of the second electronic component is greater than a thickness of the first electronic component.
15. The semiconductor device package of claim 14, wherein the encapsulant does not extend over the second electronic component.
16. The semiconductor device package of claim 14, wherein the encapsulant extends between the first electronic component and the second electronic component.
17. The semiconductor device package of claim 14, further comprising a substrate disposed under the first electrical component, wherein a width of the substrate is greater than a width of the first electronic component.
18. The semiconductor device package of claim 14, further comprising an electrical contact disposed on the first electrical component, wherein the electrical contact vertically overlaps the TSV in a cross-sectional view.
19. The semiconductor device package of claim 18, wherein the electrical contact electrically

connects the first electrical component and the second electronic component, wherein the electrical contact is laterally covered by the encapsulant.

20. The semiconductor device package of claim 19, further comprising a solder ball disposed under the first electrical component, wherein the solder ball vertically overlaps the TSV in the cross-sectional view.