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SEMICONDUCTOR SWITCH

Abstract

A semiconductor switch comprising a first branch comprising a first lateral and/or wide bandgap semiconductor transistor device and a second lateral and/or wide bandgap semiconductor transistor device, the first lateral and/or wide bandgap semiconductor transistor device and the second lateral and/or wide bandgap semiconductor transistor device being connected in series; and a second branch comprising a vertical and/or silicon-based semiconductor transistor device; wherein the first branch and the second branch are connected in parallel; and wherein a maximum voltage rating of the vertical and/or silicon-based semiconductor transistor device is greater than a maximum voltage rating of the first and second lateral and/or wide bandgap semiconductor transistor devices.

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Background/Summary

TECHNICAL FIELD

[0001] The present disclosure relates to a semiconductor switch. Particularly, but not exclusively, the disclosure relates to a parallel switch based on a high-electron-mobility transistor (HEMT) (e.g. a III-nitride HEMT) and optionally a high voltage transistor device such as an insulated-gate bipolar transistor (IGBT), a metal-oxide-semiconductor field-effect transistor (MOSFET), or a superjunction. The high voltage transistor device may be a silicon or silicon carbide device.

BACKGROUND

IGBTs

[0002] Insulated Gate Bipolar transistors (IGBTs) are silicon devices that employ bipolar conduction while maintaining MOS gate control. The bipolar conduction allows for conductivity modulation of the drift region which in turn results in low on-state resistance. The conductivity modulation depends on the current density level. Above a certain current density level (e.g. 0.1 A/cm2), the excess charged (plasma) brought by the bipolar injection of holes and electrons could be larger than the doping charge level of the drift region and therefore resulting an increase in the conductivity of the drift region. The higher the current density, the larger the plasma created in the drift region and therefore the lower the on-state resistance of the drift region. IGBTs are used as switches in high voltage and high power applications. Their typical blocking voltage range is very wide, from 600 V to 6.5 kV, while typical current range is also very wide and varies from a few Amps to thousands of Amps. The on-state voltage drop across the drift region (the region that blocks the voltage during off-state) is directly proportional to the on-state resistance and therefore a smaller on-state resistance results in a lower voltage drop and a more efficient device in the on-state. The simplest equivalent circuit description of an IGBT is that of a metal-oxide-semiconductor field-effect transistor (MOSFET) device driving the base terminal of a bipolar transistor. Most IGBTs are n-channel devices. For these the MOSFET is an n-channel and the transistor is a pnp transistor. The base region of the pnp transistor is the n-type doped drift region of the IGBT. The total on-state voltage drop of the IGBT is approximately given by the sum of the voltage drop across the base-emitter junction of the pnp transistor, the voltage drop across the drift region and the voltage drop across the n-channel of the MOSFET component. The IGBT conducts no current until the base-emitter junction of the pnp transistor is forward-biased. For this, at room temperature, a minimum voltage drop of 0.7 V (at room temperature) is needed between its main terminals. The collector terminal of the IGBT is defined as the high voltage terminal in the forward conduction, while the emitter terminal is defined as the low voltage terminal in the forward conduction. The gate terminal modulates the channel resistance and therefore modulates the electron injection into the base of the pnp transistor.

[0003] Note that the collector terminal of the IGBT is in fact the emitter terminal of the pnp transistor and the emitter terminal of the IGBT is in fact both the collector terminal of the pnp transistor and the source terminal of the MOSFET component. The collector junction of the IGBT is the same as emitter-base junction of the PNP transistor.

[0004] The IGBT has superior on-state characteristics but in general is quite slow due to the need to build and remove the plasma (excess charge of minority carriers, electrons and holes in

equilibrium) during the turn-on and turn-off transients. In particular the removal of the plasma is a slow process dictated by (i) the sweeping action of the depletion region, when the voltage builds up in the depletion region and (ii) by the recombination of carriers.

[0005] The IGBT does not conduct until 0.7 V at room temperature. This voltage level goes down as the temperature is increased. The rate at which it goes down is ˜1.5 to 2 mV/deg C. Nevertheless this is considered a weakness of the IGBT.

[0006] IGBTs are used extensively in motor control applications and they tend to operate at relatively lower frequencies (e.g. 1 to 30 KHz). One of their important applications is that of inverters in electric cars. Here 6 IGBTs (or 6 sets of IGBTs connected in parallel) are used as three half bridges per each of the three phases driving a motor.

[0007] IGBTs have an interesting temperature behavior. At relatively low on-state voltage drops (low currents) the IGBTs have a negative temperature coefficient-meaning that their on-state voltage drop decreases with temperature while at relatively higher on-state voltage drops (higher currents) the IGBTs have a positive temperature coefficient-meaning that their on-state voltage drop increases with temperature. At low currents the bipolar effect is prominent while at higher currents and eventually during the channel saturation, the MOSFET effect becomes prominent. For a nominal current the IGBTs are generally designed to have a mild positive temperature coefficient, meaning that their voltage drop increases slightly with temperature. This is a good compromise between avoiding high on-state losses at high temperatures while allowing for easy-paralleling and avoiding runaway thermal effects.

[0008] The IGBTs have good short-circuit capability and limited avalanche capability. They also have good reliability and most IGBTs are rated for a maximum junction temperature of 175° C.

Silicon Carbide

[0009] Silicon Carbide MOSFETs are unipolar devices (during forward conduction) and are considered good alternatives to the IGBTs. They are faster and they do not have the IGBTs 0.7 V weakness. Unlike silicon MOSFET and silicon Superjunctions, Silicon Carbide MOSFETs and Silicon Carbide superjunctions do not suffer from a very high positive temperature coefficient and in this way they match the high performance of the IGBTs at high temperatures. While the drift mobility decreases with temperature, the channel mobility remains constant or even slightly increases with temperature. Silicon Carbide MOSFETs and Silicon Carbide Superjunctions are among the state-of-the-art devices today. When compared to Power MOSFET superjunctions, they have a lower specific on-state drift resistance due to the presence of n-type and p-type pillars in the drift region to further reduce the resistivity of the drift region. Nevertheless, the process of making n/p pillars within the drift region is complex leading to further increase in the cost.

[0010] In general, silicon carbide wafers and device processing are still significantly more expensive than those of silicon. Moreover, Silicon Carbide MOSFETs have lower short-circuit capability than the IGBTs and are vulnerable to threshold voltage instabilities and reliability effects during the bipolar reverse conduction.

[0011] In applications such as motor control (e.g. inverters in electric cars), the currently preferred devices are vertical switches. Bipolar devices in silicon such as IGBTs or silicon Carbide MOSFETs are the main switches in this market.

[0012] IGBTs are widely available, have relatively low cost, and they are currently manufactured in 12 inch wafers. As mentioned, their on-state performance is very good especially at high currents and/or high temperature. However, they only conduct forward currents above 0.7V (at room temperature) and therefore tend to be less efficient in low to medium load conditions. Silicon Carbide MOSFETs on the other hand are expensive and their availability is scarcer.

[0013] To scale-up in current (up to values of 1000 A), chips of IGBTs or SiC are placed in parallel within a module. In this way, very large area chips are avoided. This has the advantage of higher yield and creating multiple heat sources which results in a lower temperature increase.

[0014] Parallel combinations of Silicon Carbide MOSFETs and IGBTs have also been proposed in

the prior art as shown in FIG. **1**, which shows an IGBT in parallel with Silicon Carbide MOSFET, reproduced from M. Rahimo, IEEE TRANSACTIONS ON POWER

[0015] ELECTRONICS, VOL. 30, NO. 9, September 2015, the contents of which are hereby incorporated by reference.

[0016] The silicon carbide MOSFET can conduct the forward current up to 0.7 V while both the IGBT and SiC can conduct above 0.7 V. However, the IGBTs and the SiC MOSFETs and superjunctions are vertical devices and therefore cannot integrate any smartness. No monolithic integration of sensing and protection features are present in state-of-the-art IGBTs and SiC MOSFETs.

GaN HEMT

[0017] Gallium Nitride (GaN) has been more recently considered as a very promising material for use in the field of power devices. The application areas range from portable consumer electronics, solar power inverters, electric vehicles, and power supplies. The wide band gap of the material (Eg=3.39 eV) results in high critical electric field (Ec=3.3 MV/cm) which can lead to the design of devices with a shorter drift region, and therefore lower on-state resistance if compared to a silicon-based device with the same breakdown voltage.

[0018] The use of an Aluminium Gallium Nitride (AlGaN)/GaN heterostructure also allows the formation of a two-dimensional electron gas (2 DEG) at the hetero-interface where carriers can reach very high mobility [u=2000 cm2/(Vs)] values. In addition, the piezopolarization charge present at the AlGaN/GaN heterostructure, results in a high electron density in the 2 DEG layer (e.g. 1×1013 cm-2). These properties allow the development of High Electron Mobility Transistors (HEMTs) and Schottky barrier diodes with very competitive performance parameters. One common parameter used to compare power semiconductor transistors is Specific ON-state resistance or Specific Rds(ON). The specific Rds(ON) is the product of the resistance of a device times the area of the device on wafer. An extensive amount of research has focused on the development of power devices using AlGaN/GaN heterostructures.

[0019] Layers which constitute the AlGaN/GaN heterojunction transistor are often epitaxially grown on a substrate from a different material for example Silicon, Silicon Carbide or Sapphire. Epitaxial growth of GaN on different substrates has advantages and disadvantages both in terms of the complexity and cost of growing high quality layers and in terms of device performance. A non-exhaustive list of things to consider when choosing a suitable substrate is: substrate lattice constant mismatch with GaN, substrate thermal expansion coefficient mismatch with GaN, substrate cost, substrate thermal conductivity etc. Today, substrates such as silicon (using a transition layer to adapt the mismatch between GaN layers and silicon), semi-insulating silicon carbide, quartz and sapphire are present in the market or in advanced research.

[0020] GaN transistors based on a 2 DEG are mainly available on a lateral configuration. While this is advantageous from a point of view of integrating additional smart circuits around the main power device, it does pose some limitations in terms of scalability at high currents (in excess of 100 A). Moreover, lateral GaN devices tend to be limited today to below 900 V rating, though this limit is expected to grow to 1.2 kV and beyond in the future.

[0021] There are different types of the gate structure available for GaN HEMTs. The p-Gan Gate features a layer of Magnesium doped GaN above the AlGaN layer. It delivers a positive threshold voltage of 1.3 to 1.7 V and results in an enhancement mode (normally-off) transistor. Currently this is the preferred solution in the market. The p-GaN gate technology has also some major disadvantages. If the gate voltage applied to the gate is in excess of 7 V the leakage current becomes very high leading to failure. Moreover, the relatively low threshold voltage does not give sufficient margin for avoiding retriggering on the transistor during the turn-off if the minimum voltage level is zero (ground). For this reason, often such transistors need negative voltage rails which make the driving more cumbersome and could result in some reliability issues such as the dynamic increase in the Rds(ON).

[0022] Other alternative technologies are based on an insulated gate or Schottky gate. The insulated gate is problematic for GaN due to traps in the insulated material and at the interface between the GaN or AlGaN and the insulated material. While this could deliver a higher threshold voltage, the reliability and reproducibility are currently poor and therefore there are no devices of this type in the market. The Schottky gate results in normally-on devices (depletion mode devices), which could only be used in a Cascode configuration or direct drive mode to deliver a normally-off solution. The Cascode relies on placing a silicon MOSFET in series with a depletion mode HEMT (based on Schottky gate technology) with the gate of the HEMT connected to the source of the silicon MOSFET and the drain of the Silicon MOSFET connected to the source of the depletion mode HEMT. The main advantage of this solution is the gate of the Cascode device is the insulated gate of the MOSFET which has a high degree of reliability, ease of use and can be easily tailored for a higher threshold voltage and extended voltage range. No negative voltage rail is needed. However, both the Cascode and direct drive configurations are based on two chip solution. Moreover, adjusting the slew rate in the Cascode configuration is not straightforward, as the gate of the depletion mode HEMT has a fixed potential (connected to the source of the MOSFET and not to the driver). While these solutions (i.e. direct drive and Cascode) are present in the market, they have a strong competition from enhancement gate GaN solutions.

[0023] It would be of interest to parallel GaN HEMTs with vertical devices such as IGBTs or SiC devices such as Power MOSFETs or Superjunctions. A simple, but problematic combination is shown in FIG. **2**. GaN HEMTs are especially efficient at low on-state voltage drops, low on-state currents and lower temperatures, while devices such as IGBTs are inefficient at low currents (due to the forward voltage drop on the base-emitter junction of the pnp transistor) but have superior on-state characteristics at high currents and higher temperatures.

[0024] However, enhancement GaN devices cannot be easily paralleled with vertical devices such as IGBTs and/or SiC MOSFETs and/or SiC superjunctions. The gate voltage range for vertical devices is not aligned to that of the p-GaN HEMTs. P-GaN HEMTs tend to have a threshold voltage of around 1.5 V while IGBTs and SiC power MOSFETs and superjunctions have threshold voltages in excess of 3V (e.g. 4V). The maximum drive voltage for the p-GaN HEMT (to turn-on of the device and maintain it in the on-state) is limited to 7V, before the leakage current through the gate becomes too large. In contrast, IGBTs, SiC MOSFETs and Superjunctions are driven with a maximum voltage in excess of 10 V, and often in excess of 15 V (e.g. 20V). If the HEMT could be done with an insulated gate instead of a p-GaN gate, the threshold could be adjusted and the voltage range could be extended. However, insulated gate HEMTs are not currently available and the technology is not ready for the market as explained above.

[0025] Another approach in paralleling a HEMT with a vertical switch (in this case an IGBT) has been described by L. Molnar, 2018 IEEE 24th International Symposium for Design and Technology in Electronic Packaging (SIITME), 2018, the contents of which is hereby incorporated by reference (FIG. **3**). The circuit implementation provided in FIG. **3** is however very complex with each of the GaN HEMT and the IGBT having a separate gate driver and a common digital control circuit. Furthermore, a monitor feedback circuit is also added for better sharing of current between the two components. The solution is too complex and not cost effective in high power applications.

Three Level Inverter Technology

[0026] The multi-level (e.g. three level) inverter, often referred to as Neutral Point Clamped (NPC) technology, has several advantages over the traditional two level inverter. The more levels present in the technology, the smaller the output voltage steps, resulting in cleaner waveforms, lower output current ripple, higher efficiency and smaller harmonic distortions.

[0027] FIGS. **48** and **49** show the circuit configuration of a two level inverter using IGBTs and the three-level NPC inverter respectively. In the two-level inverter (FIG. **48**) each phase contains a half-bridge with an IGBT in the low-side leg and an IGBT in the high side leg. The output of the two-level inverter can be connected to either the DC+ bus voltage level when the IGBT on the high

side is ON and the IGBT on the low-side is OFF or to the DC− bus voltage level, when the opposite, the IGBT on the high side is OFF and the IGBT on the low-side is ON.
[0028] In the three-level NPC inverter (FIG. **49**), each phase contains a half bridge with each leg of the half bridge having two IGBTs connected in series. In this case, the applied voltage on each of the IGBTs is half of that of the traditional two-level inverter. This allows the use of IGBTs with shorter drift regions to be used. The DC bus voltage is split in two (or more for more than three levels) with a intermediate level (DC MID) which sits at a voltage given by the potential divider of the two capacitors in series. This DC MID voltage level is typically half of that between the DC+ and DC− voltage levels. Depending on the status (ON or OFF) of the four IGBTs and given the action of the additional clamping diodes placed as shown in FIG. **2**, the output voltage can be in steady-state at any of the three level DC voltages (DC+, DC MID, and DC−) and switching between these states when the IGBTs are switched. The clamping diodes are connected between the series devices on each of the high-side and low-side legs to the DC MID (between the series capacitors).
[0029] The IGBTs connected to the output voltage could be in the on-state for a longer period of the cycle, resulting in greater conduction loss. On the opposite, the transistors connected to the DC− and DC+ busses could incur less conduction losses but higher switching losses.
[0030] The IGBTs could handle well the high power and high temperatures, because of their mild positive temperature coefficient. However, IGBTs are particularly inefficient at light loads, when the current is low due to the voltage drop on the collector junction. This voltage drop is around 0.7V at room temperature. IGBTs are also bipolar devices and as a result are slower and have higher switching losses than unipolar devices.
[0031] In both two-level and multi-level topologies the IGBTs could be replaced by unipolar devices such as power MOSFETs, superjunctions or HEMTs and for increased efficiency, power density and higher switching frequency of operation such devices could be made of wide bandgap (WBG) materials such as Silicon Carbide (SiC), Gallium Nitride (GaN) or heterojunctions based on Gallium Nitride and Aluminium GaN Nitride (GaN/AlGaN). Such devices could have a vertical geometry (such as SiC power MOSFETs) or lateral geometry such as GaN/AlGaN HEMTs.
[0032] Nevertheless, such WBG devices are more expensive and some of them have lower ability to handle very high power levels (high currents) or surge current reliably and efficiently.
[0033] A review of modern traction inverter systems is provided in: Sambhavi and Ramachandran, “A technical review of modern traction inverter systems used in electric vehicle application”, Energy Reports 10 (2023), 3882-3907, the contents of which are hereby incorporated by reference.
SUMMARY
[0034] Aspects and preferred features are set out in the accompanying claims.
[0035] The present disclosure provides a semiconductor switch combining a high-electron-mobility transistor (HEMT), and another transistor device that may be, for example, an insulated-gate bipolar transistor (IGBT), a metal-oxide-semiconductor field-effect transistor (MOSFET), or a superjunction. The HEMT may be a lateral device, made in III-nitride material while the transistor device may be a vertical device, preferably made in silicon or silicon-carbide. Alternatively, the vertical device may be made in Vertical GaN, GaN on GaN or ultra wide bandgap materials such as Gallium Oxide (GaO) or Aluminium Nitride (AlN). While the HEMT and the other transistor device can be based on different material systems, the semiconductor switch according to the present disclosure can enable both devices to be driven using a single control terminal, rather than requiring a dedicated driver for each device. Moreover, given the lateral configuration, other devices or circuits can be monolithically integrated with the HEMT, for sensing and protection, for voltage regulation and for enhanced reliability.
[0036] In some examples described herein, the semiconductor switch is referred to as a “combined switch”.
[0037] In some examples, as already mentioned, the HEMT may be a III-nitride based device, and

the high voltage transistor device may be a silicon or silicon carbide based device. The silicon device may be an Insulated Gate Bipolar Transistor (IGBT) while the silicon carbide based device may be a Power MOSFET or a superjunction.

[0038] In some examples, driving voltage compatibility between the HEMT and the transistor device is achieved by having the HEMT form part of an integrated circuit, the integrated circuit further comprising an interface circuit operatively connected to the gate terminal of the HEMT and to the control terminal of the semiconductor switch. In some examples the interface circuit comprises an auxiliary HEMT to achieve driving voltage compatibility between the HEMT and the transistor device.

[0039] It is an aim of this disclosure to create a switch based on a parallel combination between a lateral GaN HEMT and a vertical high voltage device and featuring a single control terminal which could drive directly or indirectly both the GaN HEMT and the vertical device. The switch according to this disclosure needs a single, common drive circuit, placed preferably externally, rather than a dedicated driver for each of the devices. Moreover, such a combined chip could be co-packaged, in a system in package (SIP) technology or packaged within a module or embedded in a PCB, such that from the outside, the switch resembles a single chip. The vertically high voltage device is preferably an IGBT. Alternatively, it could be a Silicon Carbide device such as a Power MOSFET or a Superjunction.

[0040] The module or embedded package or SIP may contain a parallel combination between several HEMT switches and several vertical high voltage devices. This could be seen as a parallel combination of several combined switches according to this disclosure.

[0041] The combined switch according to the present disclosure takes advantage of the superior characteristics of the vertical switch at high currents and high temperature (medium to full load) and the superior performance of the lateral GaN HEMT at low currents and lower temperatures (light load). The lateral GaN HEMT could also provide sensing and protection functions which could benefit both the high voltage GaN HEMT and the overall combined switch. The sensing and protection functions may be monolithically integrated (within the same chip) with the high voltage lateral GaN HEMT.

[0042] The combined switch could be seen as a single high voltage switch with two main terminals, a low voltage terminal (Terminal 1-T1) and a high voltage terminal (Terminal 2-T2) and a control terminal, as well as potentially further terminals such as current sense terminal, DC low voltage rail terminal (VDD), short-circuit protection terminal and Kelvin.

[0043] According to a first aspect of this disclosure, an interface is placed in front of the gate of the high voltage lateral GaN HEMT to adapt the driving voltage of the control terminal to that suitable and allowable for the GaN HEMT. For example, the driving voltage on the gate terminal could be from 0 to 20 V while the driving voltage seen directly by the gate terminal of the lateral high voltage GaN HEMT remains 0 to 7V. The interface may contain other clamping circuits, sensing and protection functions, pull-down devices to ensure a fast and safe turn-off, to enhance immunity against dV/dt and to absorb any transient voltage peaks on the gate. Other sensing and protection functions could also be incorporated.

[0044] In an example according to the present disclosure, the interface is or comprises a low voltage GaN HEMT (Auxiliary HEMT or Aux HEMT) in front of the intrinsic gate of the high voltage GaN HEMT to absorb any differences in the voltage between the voltage applied to the control terminal of the combined switch (which for example could go up to 20 V) and that of the gate of the lateral GaN HEMT (which for the p-GaN gate structure could only go up to ˜7 V). Furthermore, the addition of the low voltage GaN HEMT allows for an increase in the threshold voltage (wherein the threshold voltage in this context may refer to the voltage applied between the control terminal and the GaN HEMT source terminal) at which the high voltage GaN HEMT turns-on and this could be matched or be closer to the threshold voltage of the vertical switch (typically larger than 3 V).

[0045] The combined switch could be driven with voltages between 0V and 20 V (or −5 V to 20 V if desired).
[0046] Additional devices and circuits could be integrated monolithically with the High Voltage GaN HEMT. In other words, the combined switch can be described as a GaN Power Integrated Circuit (GaN Power IC) in parallel with a high voltage device (e.g. IGBT). Besides the Aux HEMT and the high voltage GaN HEMT, the GaN power IC could conveniently incorporate (monolithically integrated) other devices and/or circuits, such as a Miller clamp HEMT (pull-down device), voltage regulators, Current Sources, Current sense HEMTs, Sensing load resistor, Slew rate control circuit, dV/dt control drive circuits, short-circuit detection and protection circuits, over current and over temperature protection circuits, start-up devices/circuits, Electro-static Discharge (ESD) devices or circuits, logic circuits, capacitors, resistors and diodes (e.g. Schottky diodes or diodes made of a HEMT transistor by connecting the gate to one of its other terminals, source or drain). Some of these circuits/devices and their use have been disclosed in detail in, for example, US2020/0168599, US2020/0357909, U.S. Pat. No. 10,818,786, US2021/0335781, and US20230131602, the contents of all of which are hereby incorporated by reference.
[0047] Multiple high voltage GaN HEMTs could be placed in parallel with the IGBT. Similarly, multiple IGBTs could be used in parallel with one or multiple high voltage GaN HEMTs. This could be preferred for higher power applications or for thermal reasons (as multiple heat sources rather than a single cumulative heat source results in lower maximum temperature increase). A single AUX HEMT could be placed in the gate of the multiple GaN devices. Alternatively, individual GaN HEMTs (and possibly individually placed Miller Clamps/pull down devices/circuits) could be connected to each of the high voltage GaN HEMTs. Possibly parallel GaN power ICs further connected in parallel with an IGBT (or other vertical device or multiple parallel vertical devices) could be used in the combined switch.
[0048] The IGBT may be a reverse conducting IGBT (RC-IGBT) and therefore could incorporate a reverse conducting bipolar diode. This diode could become in parallel with the unipolar reverse-biased diode of the GaN HEMT. The reverse-bias diode of the GaN HEMT may not be able to sufficiently carry out the reverse conducting current especially in applications where freewheeling is present. Therefore, the bipolar diode of the RC IGBT could be used for carry out the reverse current or act as a surge protection during reverse conduction or for minimizing the reverse conduction losses.
[0049] Alternatively, an extra external high voltage diode could be placed in parallel with the combined switch for carrying out the current during reversed conduction or for minimizing reverse recovery losses during the reverse recovery transients. The diode could be a silicon bipolar diode such as a high voltage PIN diode or could be a Silicon Carbide Schottky diode, or a Silicon Carbide Junction Barrier Schottky (JBS) diode. Its blocking capability should be similar to that of the vertical power device (IGBT). State-of-the art Silicon Carbide Schottky Schottky or Schottky based (such as JBS) diodes are superior to silicon diodes as they offer zero reverse recovery losses and relatively low voltage drop during reverse conduction, but they are more expensive. A Silicon Carbide Junction Barrier Schottky (JBS) diode may comprise a combination of surface p+ rings and Schottky contact and could be used for a good trade-off between a low leakage current and low on-state losses.
[0050] Described herein is semiconductor switch comprising a first main terminal, a second main terminal, and a control terminal, the semiconductor switch comprising: [0051] a III-nitride integrated circuit, the III-nitride integrated circuit comprising: [0052] a high voltage HEMT, the high voltage HEMT comprising a high voltage HEMT source terminal, a high voltage HEMT drain terminal, and a high voltage HEMT gate terminal; and [0053] at least part of an interface circuit; [0054] wherein the semiconductor switch further comprises a high voltage transistor device, the high voltage transistor device comprising a transistor device first terminal, a transistor device second terminal, and a transistor device gate terminal; [0055] wherein the high voltage HEMT

source terminal and the transistor device first terminal are operatively connected to the first main terminal; [0056] wherein the high voltage HEMT drain terminal and the transistor device second terminal are operatively connected to the second main terminal; and [0057] wherein the high voltage HEMT gate terminal is operatively connected to the control terminal via the interface circuit, wherein the interface circuit is configurable to adjust a voltage applied to the control terminal to be operatively compatible with the high voltage HEMT gate terminal.

[0058] It will be understood that the “vertical device” described herein generally refers to the high voltage transistor device.

[0059] The integrated circuit may comprise the whole III-nitride interface circuit, or the interface circuit may be partly disposed on a separate circuit (from the III-nitride integrated circuit). For example, the interface circuit may be partly disposed on a separate III-nitride or silicon circuit.

[0060] In some examples, the interface circuit comprises: [0061] a low voltage auxiliary HEMT, the low voltage auxiliary HEMT comprising an auxiliary HEMT source terminal, an auxiliary HEMT drain terminal, and an auxiliary HEMT gate terminal; and [0062] a voltage limiter operatively connected to the auxiliary HEMT gate terminal; [0063] wherein the auxiliary HEMT source terminal is operatively connected to the high voltage HEMT gate terminal; [0064] wherein the high voltage HEMT source terminal and the transistor device first terminal are operatively connected to the first main terminal; [0065] wherein the high voltage HEMT drain terminal and the transistor device second terminal are operatively connected to the second main terminal; [0066] wherein the auxiliary HEMT drain terminal is operatively connected to the control terminal; and [0067] wherein the voltage limiter is operatively connected to the high voltage HEMT source terminal and to the auxiliary HEMT gate terminal, further wherein the voltage limiter is configurable to limit a voltage across the high voltage HEMT gate terminal and the high voltage HEMT source terminal.

[0068] The interface circuit may also be configured to perform other functions such as sensing and protection (e.g. current sensing and over-current protection). The interface circuit may comprise “smartness” or intelligence to aid a safe and reliable drive of the high voltage HEMT.

[0069] The interface circuit may for example be configured that higher currents (medium to full load conditions) and/or higher temperatures, the gate voltage of the HEMT could be lowered as to allow more current to flow through the first switch and thus protecting the GaN HEMT from over currents.

[0070] Preferably, the high voltage HEMT source terminal, the high voltage HEMT drain terminal, and the high voltage HEMT gate terminal are all disposed on a same surface of the high voltage HEMT (this may be referred to as a lateral arrangement or a lateral device).

[0071] Preferably, the transistor device first terminal and the transistor device gate terminal are disposed on a first side of the high voltage transistor device, and the transistor device second terminal is disposed on second side of the high voltage transistor device, opposite the first side of the high voltage transistor device (this may be referred to as a vertical arrangement or a vertical device).

[0072] In more detail, the high voltage HEMT is preferably based on a lateral arrangement wherein the main terminals (source, drain and gate terminals) are displaced laterally on the same surface of the device. The lateral HEMT may also contain a substrate terminal on the opposite surface (bottom surface). The substrate terminal may be operatively connected to the source terminal. Alternatively, the substrate may have a different potential to that of the source terminal or may be left floating. In a lateral arrangement, the on-state current flows largely laterally through the GaN HEMT from the drain to the source terminals and is modulated by the gate terminal to source terminal voltage.

[0073] The high voltage transistor device is preferably based on a vertical arrangement wherein the emitter/source and gate terminals are placed on the same surface (top surface) of the device and wherein the collector/drain terminal is placed on the opposite surface. In a vertical arrangement, the

on-state current flows largely vertically through the high voltage transistor device from the collector/drain to the emitter/source terminals and is modulated by the gate terminal to emitter/source terminal voltage.

[0074] Further described herein is a semiconductor switch comprising a first main terminal, a second main terminal, and a control terminal, the semiconductor switch further comprising: [0075] a high voltage high-electron-mobility transistor (HEMT), the high voltage HEMT comprising a high voltage HEMT source terminal, a high voltage HEMT drain terminal, and a high voltage HEMT gate terminal; [0076] a low voltage auxiliary HEMT, the low voltage auxiliary HEMT comprising an auxiliary HEMT source terminal, an auxiliary HEMT drain terminal, and an auxiliary HEMT gate terminal; [0077] a voltage limiter operatively connected to the auxiliary HEMT gate terminal; and [0078] a high voltage transistor device, the high voltage transistor device comprising a transistor device first terminal, a second transistor device second terminal, and a transistor device gate terminal; [0079] wherein the auxiliary HEMT source terminal is operatively connected to the high voltage HEMT gate terminal; [0080] wherein the high voltage HEMT source terminal and the transistor device first terminal are operatively connected to the first main terminal; [0081] wherein the high voltage HEMT drain terminal and the transistor device second terminal are operatively connected to the second main terminal; [0082] wherein the auxiliary HEMT drain terminal and the transistor device gate terminal are operatively connected to the control terminal; and [0083] wherein the voltage limiter is operatively connected to the high voltage HEMT source terminal and to the auxiliary HEMT gate terminal, further wherein the voltage limiter is configured, or configurable, to limit a voltage across the high voltage HEMT gate terminal and the high voltage HEMT source terminal.

[0084] The auxiliary HEMT described above could be part of an interface between the control terminal and the high voltage HEMT gate terminal.

[0085] The high voltage HEMT may be a III-nitride HEMT and preferably an enhancement mode (normally-off) device. The high voltage HEMT may be preferably designed to have a slightly higher breakdown voltage than the high voltage transistor device. Its breakdown may be limited by leakage rather than avalanche. In contrast the high voltage switch may break via avalanche before unacceptable high leakage is present in the high voltage HEMT. The high voltage transistor device can provide avalanche capability to the combined switch and can clamp the breakdown voltage of the combined switch to the avalanche voltage of the high voltage transistor device. As a result of this clamping effect, the high voltage HEMT may not need to be overengineered in terms of its own blocking capability, leading to smaller gate to drain or source to drain dimensions (or smaller GaN epi stack) and as a result lower specific on-state resistance Rds(ON). Note that in general stand-alone HEMTs are overengineered and they are designed to have a large margin between their rated voltage and the voltage at which leakage becomes very high. Here we take advantage of the avalanche provided by the vertical high voltage device, which means that the over engineering and the extra margin is not needed.

[0086] The auxiliary HEMT may be a III-nitride HEMT.

[0087] It will be understood that an operative connection may comprise, or may be, an electrical connection.

[0088] The high voltage transistor device may comprise a material, or materials system, other than a III-nitride material. In some examples, the high voltage transistor device is a silicon and/or silicon carbide transistor.

[0089] The high voltage HEMT and the auxiliary HEMT may be made in lateral configuration (that is to say that the main terminals are placed laterally displaced from each other on the same surface). The high voltage transistor may be made in a vertical configuration (that is to say that the main terminals may be on opposite surfaces and the current conduction is mainly vertical between such terminals).

[0090] It will be understood that the terms “high voltage” and “low voltage” as used herein are

merely relative terms. The high voltage HEMT may equivalently be referred to as a “first HEMT”, and the low voltage auxiliary HEMT may equivalently be referred to as a “second HEMT”, or simply an “auxiliary HEMT”. Similarly, the high voltage transistor device may be referred to as simply a “transistor device”.

[0091] A “III-nitride” transistor, device, or integrated circuit, as used herein, may refer generally to a transistor or device based on the group III-nitride family of materials, including GaN, AlN, InN, and alloys thereof.

[0092] Advantageously, the auxiliary HEMT can absorb any difference in voltage between the voltage applied to the control terminal and the voltage of the gate terminal of the (e.g. lateral) high voltage HEMT. In addition, the auxiliary HEMT enables an increase in the threshold voltage at which the high voltage HEMT turns on, which may therefore be matched (or be made closer to) the threshold voltage of the (e.g. vertical) transistor device.

[0093] The auxiliary HEMT drain terminal may be operatively connected to the control terminal by a first resistance (e.g. a resistor, or a device or circuit providing a resistance).

[0094] Also described herein is a semiconductor switch comprising a first main terminal, a second main terminal, and a control terminal, the semiconductor switch comprising: an integrated circuit, the integrated circuit comprising: [0095] a high voltage HEMT, the high voltage HEMT comprising high voltage HEMT source terminal, a high voltage HEMT drain terminal, and a high voltage HEMT gate terminal; and [0096] an interface circuit; [0097] wherein the semiconductor switch further comprises a high voltage transistor device, the high voltage transistor device comprising a transistor device first terminal, a transistor device second terminal, and a transistor device gate terminal; [0098] wherein the high voltage HEMT source terminal and the transistor device first terminal are operatively connected to the first main terminal; [0099] wherein the high voltage HEMT drain terminal and the transistor device second terminal may be operatively connected to the second main terminal; [0100] wherein the transistor device gate terminal is operatively connected to the control terminal; and [0101] wherein the high voltage HEMT gate terminal is operatively connected to the control terminal via the interface circuit, wherein the interface circuit is configured, or configurable, to adjust a voltage applied to the control terminal to be operatively compatible with the high voltage HEMT gate terminal.

[0102] The integrated circuit may be a III-nitride integrated circuit.

[0103] The high voltage transistor device may comprise a material, or materials system, other than a III-nitride material. For example, preferably the high voltage transistor device is not a III-nitride transistor.

[0104] The voltage limiter could be made of one or several diodes or transistor like diodes put in series. Alternatively, a threshold amplification HEMT could be provided. A description of an example of a voltage limiter is provided in US20230131602. When the voltage limiter is provided with a forward current, the voltage drop across it saturates to a known voltage, the voltage limiter could be supplied with such forward current via a current source connected to the control terminal. A description of an example of a current source is provided in US20230131602.

[0105] The high voltage HEMT could preferably be a normally off HEMT (an enhancement mode HEMT). That means its threshold voltage is positive. The auxiliary HEMT could be either a normally-off (enhancement mode) or normally on (depletion mode) HEMT.

[0106] In some examples, the high voltage transistor device may be a silicon and/or silicon carbide transistor.

[0107] Advantageously, the interface circuit can absorb any difference in voltage between the voltage applied to the control terminal and the voltage of the gate terminal of the (e.g. lateral) high voltage HEMT. In addition, the interface circuit enables an increase in the threshold voltage at which the high voltage HEMT turns on, which may therefore be matched (or be made closer to) the threshold voltage of the (e.g. vertical) transistor device.

[0108] The provision of an integrated circuit may also advantageously enable monolithic

integration of other circuits and devices, as described herein, to provide a compact and robust device package.
[0109] As described herein, the high voltage transistor device may comprise an insulated-gate bipolar transistor (IGBT). The transistor device first terminal may be an IGBT emitter terminal and the transistor device second terminal may be an IGBT collector terminal.
[0110] As described herein, the high voltage transistor device may comprise a metal-oxide-semiconductor field-effect transistor (MOSFET). The transistor device first terminal may be a source terminal (referred to as a MOSFET source terminal) and the transistor device second terminal may be a drain terminal (referred to as a MOSFET drain terminal).
[0111] As described herein, the high voltage transistor device may comprise a superjunction structure. The transistor device first terminal may be a source terminal (referred to as a superjunction source terminal) and the transistor device second terminal may be a drain terminal (referred to as a superjunction drain terminal).
[0112] In some examples, the transistor device gate terminal may be operatively connected to the control terminal via a resistance (which may be referred to as a second resistance) (e.g. a resistor, or a device or circuit providing a resistance and providing for example slew-rate control).
[0113] In some examples, the transistor device gate terminal may be operatively connected to an output of the interface circuit, e.g. such that the interface circuit may be configurable to control the transistor device.
[0114] In some examples, the high voltage HEMT source terminal, the high voltage HEMT drain terminal, and the high voltage HEMT gate terminal are laterally spaced from one another, e.g. the high voltage HEMT may be a lateral device.
[0115] In some examples, the transistor device first terminal and the transistor device second terminal are vertically spaced from one another, e.g. the high voltage transistor device may be a vertical device.
[0116] In some examples, the high voltage HEMT and the high voltage transistor device may be disposed on separate (e.g. different) substrates. For example, the high voltage HEMT may be disposed on a first semiconductor substrate, and the high voltage transistor device may be disposed on a second semiconductor substrate, different from the first semiconductor substrate.
[0117] For example, the semiconductor substrate on which the III-nitride high voltage HEMT is disposed may comprise silicon, silicon carbide, and/or sapphire.
[0118] The semiconductor switch may be configured to turn-on or be in an on-state when the control terminal is driven with a voltage of 10 V or more. The semiconductor switch may be configured to turn-off or be in an off-state when the control terminal is driven with a voltage of 0 V, or approximately 0 V. The semiconductor switch may be configured to turn off when the control terminal is driven with a voltage of less than a lower of: a threshold voltage of the high voltage HEMT; and a threshold voltage of the high voltage transistor device.
[0119] In some examples, the integrated circuit described herein further comprises one or more of:
[0120] A Miller clamp HEMT (or pull-down HEMT); [0121] a pull-down circuit; [0122] a voltage regulator; [0123] a current source; [0124] a sensing load resistor; [0125] a slew rate control circuit; [0126] a short-circuit detection circuit; [0127] a protection circuit; [0128] an over-current protection circuit; [0129] an over-temperature protection circuit; [0130] a dV/dt control circuit; [0131] a drive circuit; [0132] a start-up circuit; [0133] an electrostatic discharge circuit; [0134] a logic circuit; [0135] a capacitor; [0136] a resistor; and/or [0137] a diode.
[0138] In some examples, the semiconductor switch described herein comprises a diode operatively connected between the first main terminal and the second main terminal, the diode comprising one or more of: [0139] part of a reverse conducting IGBT; [0140] part of a reverse conducting MOSFET; [0141] a silicon carbide diode; [0142] a Schottky diode; [0143] a junction barrier Schottky diode; [0144] a silicon diode; and/or [0145] a bipolar diode.
[0146] In some examples, the semiconductor switch described herein comprises an integrated

circuit, which may be referred to as a second integrated circuit, comprising one or more of: [0147] a DC voltage regulator; [0148] a slew rate control circuit; [0149] a short-circuit detection circuit; [0150] an over-current protection circuit; [0151] an over-temperature protection circuit; [0152] a dV/dt control circuit; [0153] a drive circuit; and/or a logic and/or timing circuit.
[0154] The second integrated circuit may be a silicon integrated circuit.
[0155] The range of blocking voltages for the semiconductor switch according to this invention can be from 100 V to 3.5 kV. In particular the range of 600V to 1.7 kV is of interest with various applications including in motor control and traction inverters. For the range of 600 V to around 900 V, the preferred substrate for the high voltage GaN HEMT could be silicon, though sapphire is also possible. Above 900 V (e.g. 1.2 kV), the quartz-based or semi-insulating SiC substrates could be used. Alternatively, a thick epi of GaN on silicon could be used to enhance the breakdown voltage,
[0156] The range of on-state currents for the combined switch can vary from Amps to thousands of Amps. The range of interest could be from 100 Amps to 1000 Amps. Current can be increased by placing multiple switches in parallel. Within the switch it is preferable that the high voltage device (the vertical device) such as the IGBT, to have a higher current capability than the lateral HIGH Voltage HEMT. As an example, at full load the IGBT could carry 60 to 90% of the current while the high voltage HEMT can carry 40% to 10% of the current. This ratio could also be function of the ambient or the self-heating temperature. At higher temperatures it is expected that the ratio of the current in the vertical switch over that in the lateral high voltage HEMT may increase.
[0157] The switch is expected to operate at frequencies similar to those of the vertical device, as the GaN HEMT is expected to be faster than the vertical switch and therefore unlikely to largely limit the frequency of operation of the combined switch. If the vertical device is an IGBT, the frequency range may be below 100 kHz and if the vertical device is a Silicon Carbide MOSFET, the frequency may be below 500 KHz.
[0158] Series multiple GaN HEMTs could also be used in the combined switch. For example, two 650V GaN HEMTs (one on the low-side and one on the high side) could be placed in series with a 1.2 kV IGBT. This could be a favorable option as it is easier to make vertical devices at higher voltages than lateral HEMTs at higher voltages. An interface is still provided between the gate terminal of the low side high voltage HEMT and the control terminal. The high side GaN HEMT could be driven with the signal for the low-voltage GaN HEMT through an additional level shifter. The level shifter could be integrated with any of the high voltage GaN HEMTs.
[0159] According to a third aspect of the disclosure, there is provided a Cascode device in parallel with a high voltage device, wherein the high voltage device can be an IGBT, a silicon carbide MOSFET or superjunction.
[0160] For example, a semiconductor switch may comprise a first main terminal, a second main terminal, and a control terminal, the semiconductor switch comprising: [0161] a Cascode device, the Cascode device comprising: [0162] a MOSFET comprising a MOSFET drain terminal, a MOSFET gate terminal and a MOSFET source terminal; [0163] a high voltage depletion mode III-nitride HEMT comprising a depletion HEMT drain terminal, a depletion HEMT gate terminal and a depletion HEMT source terminal; [0164] wherein the MOSFET drain terminal is operatively connected to the depletion HEMT source terminal; [0165] wherein the semiconductor switch further comprises a high voltage transistor device comprising a transistor device first terminal, a transistor device second terminal, and a transistor device gate terminal; [0166] wherein the MOSFET source terminal and the transistor device first terminal are operatively connected to the first main terminal; [0167] wherein the depletion HEMT drain terminal and the transistor device second terminal are operatively connected to the second main terminal; [0168] wherein the MOSFET gate terminal is operatively connected to the control terminal.
[0169] The high voltage transistor device may comprise an IGBT, a silicon carbide MOSFET or a superjunction; and the MOSFET may comprise an n-channel MOSFET in vertical or quasi-vertical configuration.

[0170] The depletion HEMT gate terminal may be operatively connected to the MOSFET source terminal and the first main terminal; and [0171] the transistor device gate terminal and the MOSFET gate terminal may be operatively connected to the control terminal.
[0172] The high voltage transistor device may comprise a bipolar junction transistor, and the depletion HEMT gate terminal may be operatively connected to the MOSFET source terminal and the first main terminal; and the transistor device gate terminal may be operatively connected to the MOSFET drain terminal and the depletion HEMT source terminal, and the MOSFET gate terminal may be operatively connected to the control terminal.
[0173] The high voltage transistor device may comprise a bipolar junction transistor, and the transistor device gate terminal may be operatively connected to the MOSFET drain terminal and the depletion HEMT source terminal, and the MOSFET gate terminal may be operatively connected to the control terminal, and the depletion HEMT gate terminal may be operatively connected to the control terminal via an interface circuit, and the interface circuit may be configured to adjust a voltage applied to the control terminal to be operatively compatible with the depletion HEMT gate terminal.
[0174] The Cascode device comprises a MOSFET in series with a depletion mode GaN HEMT. The gate of the depletion mode GaN HEMT is connected to the source of the MOSFET. The MOSFET could be preferably an n-channel MOSFET in vertical or quasi-vertical configuration. A blocking voltage of the MOSFET is preferably much smaller than that of the depletion mode HEMT. For example, the MOSFET blocking voltage could be 40 V for a 650V HEMT.
[0175] The gate of the MOSFET could be shorted to the gate of the high voltage switch (e.g. IGBT) and further connected to the control terminal of the combined switch. Alternatively, either of the gates could be connected to the control terminal via slew rate structures (which could be simply resistors or resistors with diodes).
[0176] According to a fourth aspect of this disclosure, an n-channel MOSFET is provided to drive the base of a high voltage PNP transistor (bipolar junction transistor) and concomitantly be connected to the source of a high voltage depletion mode HEMT. In this configuration the combined switch is based on the parallel conduction through a bipolar junction pnp transistor and through the Cascode device. The MOSFET is responsible for both (i) enabling a negative gate-source voltage for the depletion HEMT during the blocking mode and (ii) providing the electron current to the base of the pnp transistor in the on-state. This embodiment can also be described as a split IGBT in parallel with the Cascode device wherein the MOSFET component of the IGBT is one and the same as the MOSFET component of the Cascode device. Preferably the MOSFET is a stand-alone component made in silicon or silicon-carbide technology and the high voltage PNP transistor could be made in silicon or silicon-carbide technology. The high voltage PNP transistor could have a vertical configuration with a wide n base and a relatively narrow p collector or a relatively narrow n base and a relatively wide p collector. The high voltage PNP transistor could have a breakdown voltage similar or slightly smaller than that of the high voltage depletion mode HEMT. The MOSFET could have a voltage blocking much lower than those of the high voltage depletion mode HEMT or the high voltage PNP transistor.
[0177] Alternatively, the MOSFET could also be incorporated in the IGBT itself (using the same layers as the MOSFET component of the IGBT) but this would lead to a more complex design for the IGBT.
[0178] The high voltage depletion mode HEMT may comprise a gate formed of p+ islands.
[0179] According to a fifth aspect of the disclosure, the Cascode is replaced with a high voltage depletion mode HEMT based on p+ islands in series with a MOSFET (as described in U.S. Pat. No. 11,081,578, the contents of which are hereby incorporated by reference). The two series devices are further placed in parallel with the pnp transistor.
[0180] The gate of the MOSFET could be directly connected or indirectly connected (through a slew-rate control structure) to the control terminal.

[0181] The gate of the p+ islands depletion mode HEMT could be connected through an interface to the control terminal. The interface could be the same as the one described in the first aspect in this disclosure. The role of such interface is to adapt the driving voltage of the control terminal to that suitable and allowable for the p+ islands depletion mode GaN HEMT. The interface may contain other clamping circuits, sensing and protection functions, pull-down devices to ensure a fast and safe turn-off, to enhance immunity against dV/dt and to absorb any transient voltage peaks on the gate. Other sensing and protection functions could also be incorporated.
[0182] Alternatively, the high voltage HEMT source terminal and the transistor device first terminal may be operatively connected to the first main terminal through a passive, and/or inductive, component each. This provides a way to modulate the operation of the combined switch as the inductive component would enable to introduce lead/lag in the operation of the two switches so that at times only one switch may be operating within the combined switch. Based on the load conditions, the GaN HEMT may be operated at light load (beneficial low capacitance when the switching loss smaller) through soft switching, and the IGBT or both the IGBT and HEMT may be operated at high load by using hard switching modulation. Current sensing features of GaN HEMT can help to monitor the current and identify the load conditions. These can be communicated to the external driver to enable the appropriate switching between devices based on the load conditions using the energy storing/balancing capabilities of the inductors. The inductors may be coupled inductors or detached inductors.
[0183] For example, the high voltage HEMT source terminal may be operatively connected to the first main terminal via a first inductive component, the first inductive component being operable to produce a first temporal lag between the first main terminal and the high voltage HEMT source terminal. The transistor device first terminal may be operatively connected to the first main terminal via a second inductive component, the second inductive component being operable to produce a second temporal lag between the first main terminal and the transistor device first terminal.
[0184] The combined switch can switch faster than an IGBT or a first transistor device alone.
[0185] The turn-on of the combined switch could be faster than that of an IGBT alone as the internal input capacitance of the high voltage HEMT is very small compared to the input capacitance of the IGBT and therefore it could be charged quickly. During the turn-on the GAN HEMT can take higher current than during the on-state or steady state (as much as the saturation current) until the IGBT turns-on fully and the current is redistributed (part of the current from the GaN HEMT would be redistributed in the IGBT). As a result, the turn-on losses in a combined switch may be smaller than in an IGBT or a first transistor alone.
[0186] The high voltage GaN HEMT (or when taken together the high voltage GaN HEMT and the interface) may have a smaller threshold voltage than that of the first switch (e.g. IGBT), so that the high voltage GaN HEMT turn-on before the first switch (e.g. IGBT) turns on.
[0187] The turn-off the combined switch could be faster than that of an IGBT alone as the GAN HEMT is a unipolar device and there is no excess charge (i.e. plasma) present in the GaN HEMT. Moreover during the turn-off the current may redistribute compared to the on-state or steady-state. Thus a larger proportion of the current may be switched off by the high voltage GaN HEMT, minimizing the tail of the IGBT component in the combined switch. As a result the turn-off tail and turn-off losses can be smaller in a combined switch than an IGBT alone.
[0188] The Combined switch takes advantage of the superior characteristics of the vertical switch (such as IGBTs/or vertical MOSFETs) such as high current capability in medium to full load conditions and good on-state characteristics at high temperature at and superior performance of GaN HEMTs in light load conditions and transient commutation (turn-on and turn-off) to enable the combined device to operate more efficiently in a range of high power applications such as traction inverters and a variety of motor control applications.
[0189] The vertical switch and the lateral GaN HEMT could be co-packaged to form a single

switch from an external view (similar to System in Package-SIP). This would reduce the parasitics between the corresponding terminals of the two components (high voltage HEMT and vertical switch) and provide a more compact and cost-effective solution. Metal packages or plastic or ceramic type packages could be used, A side by side technique could be employed wherein the GaN Chip and the vertical switch are placed next to each other within the same package and separated by a distance (for example by employing split paddles). The package may contain a common lead frame. Moulding compound may be placed above both components and the heatsink or a metal thermal plate can be common to the components with an isolation layer may be provided between the high voltage terminals and the metal thermal plate if required. Specific terminals of the GaN chip could be connected via internal pads and bond wires to specific terminals of the first switch, or indirectly connected via the package pins. Alternatively, a stack-die or 3D packaging technique could be used. The GaN chip could be placed or soldered or attached onto the IGBT die such that the substrate of the GaN chip could be in physical contact (via soldering or die attach) to the source metallization of the first switch. Alternatively, flip chip techniques with solder balls, or embedded PCB solutions could be used to house the combined switch.

[0190] Multiple combined switches could be placed in parallel in modules or within one or multiple embedded PCBs or high conductivity insulating substrates to increase the power (or current) rating.

[0191] For example, a semiconductor switch according to the present disclosure may be disposed in a package to form a singular switch. For example, the package may be such that the singular switch is controllable as a single switch (i.e. the high voltage HEMT and the transistor device may perform together as a single switch).

[0192] In some examples described herein, a semiconductor switch according to the present disclosure comprises a first main terminal, a second main terminal, and a control terminal. The semiconductor switch further comprises: [0193] a high voltage HEMT, the high voltage HEMT comprising a high voltage HEMT source terminal, a high voltage HEMT drain terminal, and a high voltage HEMT gate terminal; and [0194] a high voltage transistor device, the high voltage transistor device comprising a transistor device first terminal, a transistor device second terminal, and a transistor device gate terminal; [0195] wherein the high voltage HEMT source terminal and the transistor device first terminal are operatively connected to the first main terminal; [0196] wherein the high voltage HEMT drain terminal and the transistor device second terminal are operatively connected to the second main terminal; and [0197] wherein the high voltage HEMT gate terminal is operatively connected to the control terminal; [0198] wherein the control terminal is operatively connected to a first driver output of a driver, and wherein the transistor device gate terminal is operatively connected to a second driver output of a driver.

[0199] A method of operating a semiconductor switch as described herein is also described. The method may comprise: driving the control terminal, by a driver via a first driver output, at a first driving voltage, or within a first driving voltage range; and driving the transistor device gate terminal, by a driver via a second driver output, at a second driving voltage, or within a second driving voltage range.

[0200] The second driving voltage, or driving voltage range, may be different from the first driving voltage, or driving voltage range.

[0201] A system is also described herein. The system comprises a semiconductor switch as described herein. The system further comprises a driver, the driver comprising a first driver output and a second driver output; wherein the control terminal is operatively connected to the first driver output, and wherein the transistor device gate terminal is operatively connected to the second driver output.

[0202] In examples, the control terminal of the semiconductor switch, or the system, described herein, may be configured to be driven, by the driver via the first driver output, at a first driving voltage, or within a first driving voltage range. The transistor device gate terminal may be

configured to be driven, by the driver via the second driver output, at a second driving voltage, or within a second driving voltage range. The second driving voltage, or second driving voltage range, is preferably different from the first driving voltage, or first driving voltage range.
[0203] In examples, the first driving voltage, or first driving voltage level, may be within the first driving voltage range. The second driving voltage, or second driving voltage level, may be within the second driving voltage range.
[0204] For example, one or more voltage levels within the first driving voltage range may be different from one or more voltage levels within the second driving voltage range at a given instant in time.
[0205] At least one of the first driving voltage and the second driving voltage, and/or voltage levels within at least one of the first driving voltage range and the second driving voltage range, may be configured to vary selectably, corresponding to the semiconductor switch being selectably in any of: an on-state mode, an off-state mode, a turn-on mode, or a turn-off mode.
[0206] In some examples, a slew rate at the control terminal and/or the transistor device gate terminal is configured to vary selectably, corresponding to the semiconductor switch being selectably in the turn-on mode or the turn-off mode. It will be understood that the slew rates at the control terminal and the transistor device gate terminal, respectively, may be configured to be different at a given instant in time.
[0207] Advantageously, according to some examples described herein, dynamic control of the turn-on and/or turn-off curves, and/or slew rate, and/or timing sequences, for the (high voltage) HEMT can be achieved by driving the terminal(s) of a semiconductor switch as described herein.
[0208] In some examples, the semiconductor switch comprises an interface circuit. The high voltage HEMT gate terminal may be operatively connected to the control terminal via the interface circuit. As described herein, the interface circuit may be configurable to adjust the voltage levels within the first driving voltage range (or to adjust the first driving voltage) to be operatively compatible with the high voltage HEMT gate terminal.
[0209] The semiconductor switch may comprise a feedback circuit (the feedback circuit may form part of the interface circuit). The feedback circuit may comprise at least one output operatively connected to a driver feedback input (e.g. of the driver described herein). The feedback circuit may be configured to provide a feedback signal to the driver feedback input, the feedback signal corresponding to a status of the semiconductor switch. For example, the feedback signal may correspond to the sensed current, sensed voltage, and/or sensed temperature in the semiconductor switch. The driver may be configured to adjust the driving voltage levels, frequencies of the driving voltage levels, slew rates, and/or timing sequences of the driving voltage levels based on the feedback signal.
[0210] In some examples, the high voltage HEMT is part of an integrated circuit. In some examples, the interface circuit is monolithically integrated with the high voltage HEMT (e.g. as part of the integrated circuit).
[0211] The control terminal may be operatively connected to the first driver output via a first resistor, and/or the transistor device gate terminal may be operatively connected to the second driver output via a second resistor. The first and/or the second resistor(s) may be external to the semiconductor switch. In some examples, the first and/or the second resistor(s) are part of the semiconductor switch, e.g. as part of the integrated circuit and/or as part of the interface circuit.
[0212] As described herein, an interface circuit may comprise a low voltage auxiliary HEMT, the low voltage auxiliary HEMT comprising an auxiliary HEMT source terminal, an auxiliary HEMT drain terminal, and an auxiliary HEMT gate terminal; and a voltage limiter operatively connected to the auxiliary HEMT gate terminal; wherein the auxiliary HEMT source terminal is operatively connected to the high voltage HEMT gate terminal; wherein the auxiliary HEMT drain terminal is operatively connected to the control terminal; and wherein the voltage limiter is operatively connected to the high voltage HEMT source terminal and to the auxiliary HEMT gate terminal,

further wherein the voltage limiter is configurable to limit a voltage across the high voltage HEMT gate terminal and the high voltage HEMT source terminal.
[0213] In some examples, the interface circuit comprises a Miller clamp transistor, the Miller clamp transistor comprising a plurality of Miller clamp gates, wherein the interface circuit is configured such that an on-state resistance of the Miller clamp transistor depends on which Miller clamp gate(s) of the plurality of Miller clamp gates is active.
[0214] In some examples, the interface circuit comprises a plurality of Miller clamp transistors having different on-state resistances.
[0215] For example, a single or multiple Miller clamp transistors can provide a variable on-state resistance to control the high voltage HEMT dynamically, e.g. in an on-state mode.
[0216] For example, the interface circuit may further comprise a logic circuit configured to control activation of each Miller clamp transistor of the plurality of Miller clamp transistors. In some examples, the transistor device gate terminal is operatively connected to the second driver output via the interface circuit.
[0217] In some examples, the control terminal is further operatively connected to a third driver output of the driver, wherein: [0218] when the semiconductor switch is in the turn-off mode, the control terminal is configured to selectably receive either: [0219] a regular turn-off signal comprising a first driving voltage level within the first driving voltage range, from the driver via the first driver output; or [0220] a delayed turn-off signal, or a slower turn-off signal, comprising a third driving voltage level within the first driving voltage range, from the driver via the third driver output.
[0221] In some examples, the transistor device gate terminal is operatively connected to a fourth driver output of the driver, wherein: [0222] when the semiconductor switch is in the turn-off mode, the transistor device gate terminal is configured to selectably receive either: [0223] a regular turn-off signal comprising a second driving voltage level within the second driving voltage range, from the driver via the second driver output; or [0224] a delayed turn-off signal, or a slower turn-off signal, comprising a fourth driving voltage level within the second driving voltage range, from the driver via the fourth driver output.
[0225] It will be understood that a slower turn-off signal corresponds to a turn-off signal that is slower than the regular turn-off signal.
[0226] Advantageously, the turn-off speed of the high voltage HEMT and/or the transistor device may be dynamically controlled due to the selectability of the turn-off signals.
[0227] In some examples, the control terminal is operatively connected to the third driver output via a third resistor. A resistance of the third resistor may greater than a resistance of the first resistor to enable the slower turn-off.
[0228] In some examples, the transistor device gate terminal is operatively connected to the fourth driver output via a fourth resistor. A resistance of the fourth resistor may be greater than a resistance of the second resistor to enable the slower turn-off.
[0229] In some examples, the semiconductor switch (e.g. the interface circuit) comprises a first Miller clamp transistor and a second Miller clamp transistor, the first Miller clamp transistor and the second Miller clamp transistor being operatively connected to the High voltage HEMT gate terminal, the second Miller clamp transistor having a higher on-state resistance than the first Miller clamp transistor. The regular turn-off signal may be configured to activate the first Miller clamp transistor. The delayed turn-off signal, or the slower turn-off signal, may be configured to activate the second Miller clamp transistor. For example, the first Miller clamp transistor may be optimized to enable fast turn-off the power HEMT and/or to avoid a false turn-on of the power HEMT during regular operation of the semiconductor switch. The second Miller clamp transistor may be optimized to turn-off the power HEMT when a slow turn-off is selected.
[0230] In some examples, the interface circuit comprises a third Miller clamp transistor, the third Miller clamp transistor comprising a third Miller clamp drain terminal, wherein the third Miller

clamp drain terminal is operatively connected to the high voltage HEMT gate terminal.
[0231] In some examples, the interface circuit further comprises a fourth Miller clamp transistor, the fourth Miller clamp transistor comprising a fourth Miller clamp drain terminal, wherein the fourth Miller clamp drain terminal is operatively connected to the transistor device gate terminal.
[0232] The third and/or fourth Miller clamp transistor(s) may enable regulation or pull-down of the high voltage HEMT, and/or the transistor device, respectively.
[0233] In some examples, a semiconductor switch according to the present disclosure comprises a HEMT (e.g. a high voltage HEMT), without another transistor device in parallel. For example, a semiconductor switch may comprise a HEMT, the HEMT comprising a gate terminal, the gate terminal being operatively connected to a first driver output of a driver and to a second driver output of the driver.
[0234] When the semiconductor switch is in a turn-off mode, the gate terminal is configured to selectably receive either: [0235] a regular turn-off signal from the first driver output; or [0236] a delayed turn-off signal, or a slower turn-off signal, from the second driver output.
[0237] It will be understood that a slower turn-off signal corresponds to a turn-off signal that is slower than the regular turn-off signal.
[0238] In some examples, when the semiconductor switch is in a turn-on mode, the gate terminal is configured to selectably receive either: [0239] a regular turn-on signal from the first driver output; or [0240] a delayed or slower turn-on signal from the second driver output.
[0241] Dynamic adjustment of the turn-off and/or turn-on speeds of the switch comprising the HEMT can therefore be controlled as described herein.
[0242] Also described herein is a semiconductor switch comprising: a first branch comprising a first lateral semiconductor transistor device and a second lateral semiconductor transistor device, the first lateral semiconductor transistor device and the second lateral semiconductor transistor device being connected in series; and a second branch comprising a vertical semiconductor transistor device; wherein the first branch and the second branch are connected in parallel; and wherein a maximum voltage rating of the vertical semiconductor transistor device is greater than a maximum voltage rating of the first and second lateral semiconductor transistor devices.
[0243] In some examples, the voltage rating of the vertical semiconductor transistor device is greater than the maximum voltage rating of the first and second lateral semiconductor transistor devices by a factor of at least 1.5, or at least 2.
[0244] The semiconductor switch may comprise a first control terminal configured to receive the first control signal. The semiconductor switch may comprise a second control terminal configured to receive the second control signal. The semiconductor switch may comprise a third control terminal configured to receive the third control signal. As described herein, the first control terminal may correspond to, or be connected to, a gate terminal of the first lateral semiconductor transistor device. The second control terminal may correspond to, or be connected to, a gate terminal of the second lateral semiconductor transistor device. The third control terminal may correspond to, or be connected to, a gate terminal of the vertical semiconductor transistor device.
[0245] Additionally, the semiconductor switch may also have a mid terminal connected to the mid-point between the first lateral semiconductor transistor device and the second lateral semiconductor transistor device.
[0246] The semiconductor switch may comprise an interface circuit. The interface circuit may be connected between one or both of the first and second control terminals and their respective transistor devices. That is, the interface circuit may be connected between at least one of: the first control terminal and the first lateral semiconductor transistor device; and the second control terminal and the second lateral semiconductor transistor device.
[0247] In an example, the interface circuit may comprise at least one of: a first auxiliary HEMT operatively connected between the first control terminal and the first lateral semiconductor transistor device, and a second auxiliary HEMT operatively connected between the second control

terminal and the second lateral semiconductor transistor device.
[0248] The first and/or second lateral semiconductor transistor device(s) may comprise one or more III-nitride transistors. The first and/or second lateral semiconductor transistor device(s) may comprise one or more HEMTs. The first and/or second lateral semiconductor transistor device(s) may comprise one or more III-nitride HEMTs.
[0249] The vertical semiconductor transistor device may comprise one or more silicon or silicon carbide transistors, one or more IGBTs, one or more MOSFETs, and/or one or more superjunctions.
[0250] The first lateral semiconductor transistor device may be configured to be driven by a first control signal. The second lateral semiconductor transistor device may be configured to be driven by a second control signal. The vertical semiconductor transistor device may be configured to be driven by a third control signal. An apparatus according to the present disclosure may comprise a semiconductor switch as described herein, and a driver. One or more of the transistor devices may be operatively connected to the driver, the driver being configured to provide one or more of the first, second, and third control signals. The first, second, and third control signals may be a same signal, or may be different signals.
[0251] Alternatively, the semiconductor switch may comprise only one control terminal to receive a control signal from a driver/controller. The semiconductor switch may further comprise an interface circuit. The interface circuit may be connected between the control terminal and the three transistor devices-first and second lateral semiconductor transistor devices and the vertical semiconductor transistor device. The interface circuit may be configured to internally generate the first control signal and provide to the gate of the first lateral semiconductor transistor device, generate the second control signal and provide to the gate of the second lateral semiconductor transistor device and generate the third control signal and provide to the gate of the vertical semiconductor transistor device.
[0252] The interface circuit may comprise additional circuits and components such as auxiliary HEMTs, level shifter, slew rate control circuit, logic circuits, voltage regulator to generate the first, second and third control signals.
[0253] Also described herein is a semiconductor switch comprising: a first branch comprising a first wide bandgap semiconductor transistor device, and a second wide bandgap semiconductor transistor device, the first wide bandgap semiconductor transistor device and the second wide bandgap semiconductor transistor device being connected in series; and a second branch comprising a silicon-based semiconductor transistor device; wherein the first branch and the second branch are connected in parallel; and wherein a maximum voltage rating of the silicon semiconductor transistor device is greater than a maximum voltage rating of the first and second wide bandgap semiconductor transistor devices.
[0254] The voltage rating of the silicon-based semiconductor transistor device may be greater than the maximum voltage rating of the first and second wide bandgap semiconductor devices by a factor of at least 1.5, or at least 2.
[0255] The semiconductor switch may comprise a first control terminal configured to receive the first control signal. The semiconductor switch may comprise a second control terminal configured to receive the second control signal. The semiconductor switch may comprise a third control terminal configured to receive the third control signal. As described herein, the first control terminal may correspond to, or be connected to, a gate terminal of the first wide bandgap semiconductor transistor device. The second control terminal may correspond to, or be connected to, a gate terminal of the second wide bandgap semiconductor transistor device. The third control terminal may correspond to, or be connected to, a gate terminal of the silicon-based semiconductor transistor device.
[0256] Additionally, the semiconductor switch may also have a mid terminal connected to the mid-point between the first lateral semiconductor transistor device and the second lateral semiconductor transistor device.

[0257] The semiconductor switch may comprise an interface circuit. The interface circuit may be connected between one or both of the first and second control terminals and their respective transistor devices. That is, the interface circuit may be connected between at least one of: the first control terminal and the first wide bandgap semiconductor transistor device; and the second control terminal and the second wide bandgap semiconductor transistor device.
[0258] At least one of the first and second wide bandgap semiconductor transistor devices may comprise one or more III-nitride transistors, and/or one or more silicon carbide transistors.
[0259] The silicon-based semiconductor transistor device may comprise one or more IGBTs, one or more MOSFETs, and/or one or more superjunctions.
[0260] The first wide bandgap semiconductor transistor device may be configured to be driven by a first control signal. The second wide bandgap semiconductor transistor device may be configured to be driven by a second control signal. The silicon-based semiconductor transistor device may be configured to be driven by a third control signal. An apparatus according to the present disclosure may comprise a semiconductor switch as described herein, and a driver. One or more of the transistor devices may be operatively connected to the driver, the driver being configured to provide one or more of the first, second, and third control signals. The first, second, and third control signals may be a same signal, or may be different signals.
[0261] Alternatively, the semiconductor switch may comprise only one control terminal to receive a control signal from a driver/controller. The semiconductor switch may further comprise an interface circuit. The interface circuit may be connected between the control terminal and the three transistor devices-first and second wide bandgap semiconductor transistor devices and the silicon-based semiconductor transistor device. The interface circuit may be configured to internally generate the first control signal and provide to the gate of the first wide bandgap semiconductor transistor device, generate the second control signal and provide to the gate of the second wide bandgap semiconductor transistor device and generate the third control signal and provide to the gate of the silicon-based semiconductor transistor device.
[0262] The interface circuit may comprise additional circuits and components such as auxiliary HEMTs, level shifter, slew rate control circuit, logic circuits, voltage regulator to generate the first, second and third control signals.
[0263] Also described herein is a half bridge circuit comprising a low-side leg and a high-side leg, each of the low-side leg and the high-side leg comprising a semiconductor switch comprising: a first branch comprising a first wide bandgap semiconductor transistor device, and a second wide bandgap semiconductor transistor device, the first wide bandgap semiconductor transistor device and the second wide bandgap semiconductor transistor device being connected in series; and a second branch comprising a silicon-based semiconductor transistor device; wherein the first branch and the second branch are connected in parallel; and wherein a maximum voltage rating of the silicon semiconductor transistor device is greater than a maximum voltage rating of the first and second wide bandgap semiconductor transistor devices.
[0264] Also described herein is a half bridge circuit comprising a low-side leg and a high-side leg, each of the low-side leg and the high-side leg comprising a semiconductor switch comprising: a first branch comprising a first lateral semiconductor transistor device, and a second lateral semiconductor transistor device, the lateral semiconductor transistor device and the second lateral semiconductor transistor device being connected in series; and a second branch comprising a vertical semiconductor transistor device; wherein the first branch and the second branch are connected in parallel; and wherein a maximum voltage rating of the vertical semiconductor transistor device is greater than a maximum voltage rating of the first and second lateral semiconductor transistor devices.
[0265] Also described herein is an inverter comprising at least one phase, each phase comprising at least one half bridge circuit, each half bridge circuit comprising a low-side leg and a high-side leg, each of the low-side leg and the high-side leg comprising a semiconductor switch comprising: a

first branch comprising a first wide bandgap semiconductor transistor device, and a second wide bandgap semiconductor transistor device, the first wide bandgap semiconductor transistor device and the second wide bandgap semiconductor transistor device being connected in series; and a second branch comprising a silicon-based semiconductor transistor device; wherein the first branch and the second branch are connected in parallel; and wherein a maximum voltage rating of the silicon semiconductor transistor device is greater than a maximum voltage rating of the first and second wide bandgap semiconductor transistor devices.

[0266] Also described herein is an inverter comprising at least one phase, each phase comprising at least one half bridge circuit, each half bridge circuit comprising a low-side leg and a high-side leg, each of the low-side leg and the high-side leg comprising a semiconductor switch comprising: a first branch comprising a first lateral semiconductor transistor device, and a second lateral semiconductor transistor device, the first lateral semiconductor transistor device and the second lateral semiconductor transistor device being connected in series; and a second branch comprising a vertical semiconductor transistor device; wherein the first branch and the second branch are connected in parallel; and wherein a maximum voltage rating of the vertical semiconductor transistor device is greater than a maximum voltage rating of the first and second lateral semiconductor transistor devices.

[0267] Also described herein is a multi-level inverter comprising at least one phase, each phase comprising at least one half-bridge circuit. The half bridge circuit may comprise a low side and a high side. Each side of each half bridge circuit may comprise: a first wide bandgap semiconductor transistor device; and a silicon-based semiconductor transistor device; wherein the wide bandgap semiconductor transistor device and the silicon-based semiconductor transistor device are connected in series.

[0268] The first wide bandgap semiconductor transistor device may comprise one or more III-nitride transistors, and/or one or more silicon carbide transistors.

[0269] The silicon-based semiconductor transistor device may comprise one or more IGBTs, one or more MOSFETs, and/or one or more superjunctions.

[0270] The multi-level inverter may comprise an output terminal. The silicon-based semiconductor transistor device may be arranged closer in proximity to the output terminal than the first wide bandgap semiconductor transistor device. That is, the silicon-based semiconductor transistor device may be connected between the first wide bandgap semiconductor transistor device and the output terminal. In other words, the output terminal may be connected at a mid-point of the high-side and the low-side of the half bridge circuit.

[0271] In some examples of the multi-level inverter according to the present disclosure, each side of each half bridge circuit may further comprise a second wide bandgap semiconductor transistor device connected in parallel with the silicon-based semiconductor transistor device.

[0272] A maximum voltage rating of the silicon-based semiconductor transistor device may be greater than a maximum voltage rating of the first wide bandgap semiconductor transistor device. For example, the maximum voltage rating of the silicon-based semiconductor transistor device may be greater than the maximum voltage rating of the first wide bandgap semiconductor transistor device by a factor of at least 1.5, or at least 2.

[0273] The multi-level inverter may comprise a first control terminal configured to receive a first control signal to drive the first wide bandgap semiconductor device. The multi-level inverter may comprise an interface circuit operatively connected between the first control terminal and the first wide bandgap semiconductor device. The interface circuit may comprise a first auxiliary HEMT operatively connected between the first control terminal and the first wide bandgap semiconductor device.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

[0274] The present invention will now be described by way of example with reference to the following drawings:

[0275] FIG. **1** illustrates a prior art example of an IGBT in parallel with a silicon carbide MOSFET, reproduced from M. Rahimo, IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 30, NO. 9, September 2015;

[0276] FIG. **2** illustrates a parallel combination between a discrete GaN HEMT and an IGBT;

[0277] FIG. **3** illustrates a prior art solution for paralleling IGBTs with a GaN HEMT, reproduced from L. Molnar, 2018 IEEE 24th International Symposium for Design and Technology in Electronic Packaging (SIITME), 2018;

[0278] FIG. **4** illustrates an example of a semiconductor switch according to the present disclosure;

[0279] FIG. **5** illustrates an example of a semiconductor switch according to the present disclosure in which the transistor device gate terminal is operatively connected to an output of the interface circuit;

[0280] FIG. **6** illustrates an example of a semiconductor switch featuring a lateral GaN HEMT, an auxiliary low voltage HEMT and a high voltage IGBT placed in parallel with the lateral high voltage GaN HEMT according to the present disclosure;

[0281] FIG. **7***a* illustrates an example of a semiconductor switch featuring a lateral GaN HEMT, an auxiliary low voltage HEMT, a pull down device and a high voltage IGBT placed in parallel with the lateral high voltage GaN HEMT, according to the present disclosure;

[0282] FIG. **7***b* illustrates an example of a semiconductor switch featuring a lateral high voltage GaN HEMT, an auxiliary low voltage HEMT, a pull down device and a high voltage SiC MOSFET (or superjunction) in parallel with the lateral high voltage GaN HEMT, according to the present disclosure;

[0283] FIG. **8** illustrates an example of a semiconductor switch wherein the interface circuit comprises an auxiliary low voltage HEMT and a pull down device connected to the gate of a GaN HEMT;

[0284] FIG. **9** illustrates the schematic shapes of on-state output I-V characteristics of the high voltage lateral GaN HEMT and the vertical IGBT at room and high temperatures;

[0285] FIG. **10** illustrates the schematic shapes of output on-state I-V characteristics of the combined GaN HEMT and IGBT switch according to the present disclosure;

[0286] FIG. **11** illustrates the schematic shapes of blocking I-V characteristics of the IGBT and high voltage lateral GaN HEMT at room temperature and high temperature;

[0287] FIG. **12** illustrates schematic shapes of blocking I-V characteristics of the semiconductor switch at room temperature and high temperature;

[0288] FIG. **13** illustrates a semiconductor switch according to the present disclosure featuring a lateral GaN HEMT, an auxiliary low voltage HEMT, a pull down device and a high voltage IGBT placed in parallel with the lateral high voltage GaN HEMT;

[0289] FIG. **14** illustrates a semiconductor switch according to the present disclosure featuring a lateral GaN HEMT, an auxiliary low voltage HEMT, a pull down device and a high voltage SiC MOSFET (or superjunction) placed in parallel with the lateral high voltage GaN HEMT;

[0290] FIG. **15** illustrates a semiconductor switch according to the present disclosure featuring a lateral GaN HEMT, an auxiliary low voltage HEMT, a pull down device and a high voltage IGBT placed in parallel with the lateral high voltage GaN HEMT;

[0291] FIG. **16** illustrates a semiconductor switch comprising an additional start-up circuit;

[0292] FIG. **17***a* illustrates a semiconductor switch in which auxiliary HEMT is embedded in a sensing and protection circuit block, which is monolithically integrated with a GaN HEMT;

[0293] FIG. **17***b* illustrates a semiconductor switch in which auxiliary HEMT is embedded in a sensing and protection circuit block, which is monolithically integrated with a GaN HEMT;

[0294] FIG. **18** illustrates an example of a semiconductor switch according to the present disclosure in which a high voltage HEMT is part of a power integrated circuit;
[0295] FIG. **19** illustrates an example of a semiconductor switch comprising slew rate control circuits;
[0296] FIG. **20** illustrates an example of a semiconductor switch comprising multiple high voltage HEMTs in parallel with a high voltage transistor device;
[0297] FIG. **21** illustrates an example of a semiconductor switch comprising two power integrated circuits, each comprising a high voltage HEMT, in parallel with a high voltage transistor device;
[0298] FIG. **22** illustrates an example of a semiconductor switch comprising multiple high voltage HEMTs;
[0299] FIG. **23** illustrates an example of a semiconductor switch comprising a silicon companion chip, or integrated circuit;
[0300] FIG. **24***a* illustrates a schematic cross-section representation and connections between a lateral high voltage HEMT, an auxiliary HEMT, and a trench IGBT;
[0301] FIG. **24***b* illustrates a schematic cross-section representation and connections between a lateral high voltage HEMT, an auxiliary HEMT, and a SiC MOSFET;
[0302] FIG. **25** illustrates a schematic equivalent circuit representation and connections between a lateral high voltage HEMT, an auxiliary HEMT, and an IGBT;
[0303] FIG. **26***a* illustrates a semiconductor switch comprising an IGBT and a GaN Power IC, further comprising a high voltage GaN HEMT and an interface which has at least one connection to the control terminal and at least one connection to the internal gate of the high voltage GaN HEMT and an external diode in parallel;
[0304] FIG. **26***b* illustrates a semiconductor switch comprising an IGBT and a GaN Power IC, further comprising a high voltage GaN HEMT and an interface which has at least one connection to the control terminal and at least one connection to the internal gate of the high voltage GaN HEMT and a series of diodes in parallel to GaN HEMT and IGBT;
[0305] FIG. **26***c* illustrates a semiconductor switch depicting a diode equivalent of a GaN HEMT in a GaN Power IC, and a diode equivalent of a SiC MOSFET;
[0306] FIG. **27** illustrates a semiconductor switch according to the third aspect of this invention and based on a Cascode HEMT in parallel with an IGBT;
[0307] FIG. **28** illustrates a semiconductor switch according to a fourth aspect of this invention, comprising a depletion MODE HEMT, a MOSFET and a PNP transistor;
[0308] FIG. **29** illustrates a semiconductor switch according to a fifth aspect of this invention, comprising a depletion MODE HEMT with p+ islands, an interface between a control terminal and the gate terminal of the depletion mode HEMT with p+ islands, a MOSFET and a PNP transistor;
[0309] FIG. **30** illustrates an example of a voltage limiter;
[0310] FIG. **31** illustrates an additional example of a voltage limiter;
[0311] FIG. **32** illustrates an additional example of a voltage limiter which comprises a current source;
[0312] FIG. **33***a* illustrates an example of a semiconductor switch wherein a control terminal and a transistor device gate terminal are configured to be driven by a driver;
[0313] FIG. **33***b* illustrates an example of a semiconductor switch wherein a control terminal and a transistor device gate terminal are configured to be driven by a driver;
[0314] FIG. **33***c* illustrates an example of a semiconductor switch wherein a control terminal and a transistor device gate terminal are configured to be driven by a driver;
[0315] FIG. **33***d* illustrates an example of a semiconductor switch wherein a control terminal and a transistor device gate terminal are configured to be driven by a driver along with a feedback control circuit;
[0316] FIG. **33***e* illustrates an example of a semiconductor switch wherein a control terminal and a transistor device gate terminal are configured to be driven by a driver along with a feedback control

circuit, wherein a current sensing HEMT acts as a feedback control circuit;
[0317] FIG. **34** illustrates an example of a semiconductor switch wherein the transistor device gate terminal is driven via an interface circuit;
[0318] FIG. **35** illustrates an example of a (combined) semiconductor switch wherein each device forming the semiconductor switch may be driven by respective gate signals where turn-on and turn-off signals are provided separately;
[0319] FIG. **36** illustrates an example of a semiconductor switch wherein the multiple turn-off driving inputs are provided to adjust the turn-off speed of the power integrated circuit;
[0320] FIG. **37** illustrates an example of a semiconductor switch comprising a power HEMT and a high voltage switch each configured to have their own turn-on pins;
[0321] FIG. **38** illustrates an example of a semiconductor switch comprising an example of an interface circuit;
[0322] FIG. **39** illustrates an example of a semiconductor switch wherein all of the gate driving signals pass through an interface circuit;
[0323] FIG. **40***a* illustrates an example of a semiconductor switch wherein different driving voltages can be provided at the gates of the devices forming the switch;
[0324] FIG. **40***b* illustrates an example of a semiconductor switch wherein different driving voltages can be provided at the gates of the devices forming the switch;
[0325] FIG. **41** illustrates an example of a semiconductor switch comprising respective Miller clamp transistors connected to the gates of each transistor device forming the switch;
[0326] FIG. **42** illustrates an example of a semiconductor switch additionally comprising a start-up circuit;
[0327] FIG. **43** illustrates an example of a semiconductor switch comprising a high voltage HEMT configured to enable dynamic adjustment of the turn-on and/or turn-off speeds of the high voltage HEMT;
[0328] FIG. **44** illustrates an example of a semiconductor switch comprising a high voltage HEMT and a Miller clamp transistor comprising multiple gates;
[0329] FIG. **45** illustrates an example of a semiconductor switch comprising a high voltage HEMT without an auxiliary interface circuit;
[0330] FIG. **46** illustrates an example of a semiconductor switch comprising a high voltage HEMT and a start-up circuit;
[0331] FIG. **47** schematically illustrates an example of a method of operating a semiconductor switch according to the present disclosure;
[0332] FIG. **48** illustrates a prior art circuit configuration of a two level inverter using IGBTs;
[0333] FIG. **49** illustrates a prior art circuit configuration of a three level NPC inverter;
[0334] FIG. **50** illustrates an example of a semiconductor switch suitable as part of an inverter according to the present disclosure;
[0335] FIG. **51***a* illustrates an example of a semiconductor switch comprising first and second interface circuits suitable as part of an inverter;
[0336] FIG. **51***b* illustrates an example of a semiconductor switch comprising an interface circuit comprising first and second auxiliary HEMTs suitable as part of an inverter;
[0337] FIG. **52***a* illustrates an example of a semiconductor switch comprising a single, or common, control terminal;
[0338] FIG. **52***b* illustrates an example of an interface circuit that may be used as part of a semiconductor switch;
[0339] FIG. **53** illustrates an example of a half bridge circuit suitable as part of an inverter according to the present disclosure;
[0340] FIG. **54** illustrates an example of a one phase inverter according to the present disclosure;
[0341] FIG. **55** illustrates an example of a three phase inverter according to the present disclosure
[0342] FIG. **56** illustrates an example of a multi-level inverter comprising at least one phase

according to the present disclosure;
[0343] FIG. **57** illustrates another example of a multi-level inverter comprising at least one phase according to the present disclosure;
[0344] FIG. **58** illustrates an example of a semiconductor switch comprising a feedback element according to the present disclosure;
[0345] FIG. **59** illustrates a further example of a semiconductor switch comprising a feedback element according to the present disclosure; and
[0346] FIG. **60** illustrates an example of a semiconductor switch comprising temperature sensors for monitoring the temperatures of the transistor devices.

DETAILED DESCRIPTION

[0347] In the illustrative examples described herein, a semiconductor switch comprises a (high voltage) high-electron-mobility transistor (HEMT), such as a III-nitride HEMT, and optionally a high voltage transistor device such as an insulated-gate bipolar transistor. While the examples of HEMTs described herein are predominantly GaN-based, it will be appreciated that HEMTs based on other III-nitride materials such as InN, AlN, and alloys of InN, AlN, and GaN may also be suitable. Similarly, it will be appreciated that the high voltage transistor device described herein may alternatively comprise a metal-oxide-semiconductor field-effect transistor (MOSFET), and/or a superjunction. The high voltage transistor device may be a silicon or silicon carbide device.
[0348] FIG. **4** illustrates a combined switch according to the first aspect of the present disclosure, featuring a lateral GaN HEMT (**10**), an interface circuit (**207**) and a high voltage transistor (**30**). The interface circuit (**207**) is placed in front of the gate of the lateral GaN HEMT to adapt the driving voltage of the control terminal to that suitable and allowable for the GaN HEMT. This interface could be preferably monolithically integrated with the power HEMT for providing lower parasitics, ease of manufacturing and fast reaction time. Alternatively, this interface could be part of a separate chip (such as a silicon companion chip, or a driver chip). The interface circuit may additionally include clamping circuits, sensing and protection functions, pull-down devices to ensure a fast and safe turn-off, to enhance immunity against dV/dt and to absorb any transient voltage peaks on the gate.
[0349] FIG. **5** illustrates an example of the second aspect of the present disclosure, featuring the high voltage transistor (**30**) to be connected to another output of the interface circuit. The interface circuit can provide functionality of clamping, voltage limiting, sensing and protection and other control functions for the high voltage transistor (**30**).
[0350] As shown in FIG. **6**, the interface circuit may additionally comprise a voltage limiter **201**. The voltage limiter may be a circuit block which can limit (or clamp) the maximum voltage at the gate of the auxiliary low voltage HEMT. Through this manner of operation the voltage limiter may overall act to provide a limit on the maximum voltage on the gate terminal of the GaN HEMT. In operation, the voltage applied to the control terminal may be divided between a voltage drop between the drain and source terminal of the aux HEMT (**20**) and a voltage drop between the gate and source terminal of the GaN HEMT (**10**). The auxiliary HEMT and the voltage limiter may be monolithically integrated with the GaN HEMT.
[0351] FIG. **6** illustrates an example of a combined switch featuring a lateral GaN HEMT (**10**) placed in parallel with a high voltage IGBT (**40**) and an example of the interface circuit comprising, an auxiliary low voltage HEMT (**20**) and a voltage limiter (**201**). The voltage limiter may be a circuit block which can limit (or clamp) the maximum voltage at the gate of the auxiliary low voltage HEMT. Through this manner of operation the voltage limiter may overall act to provide a limit on the maximum voltage on the gate terminal of the GaN HEMT. In operation, the voltage applied to the control terminal may be divided between a voltage drop between the drain and source terminal of the aux HEMT (**20**) and a voltage drop between the gate and source terminal of the GaN HEMT (**10**). The auxiliary HEMT and the voltage limiter may be monolithically integrated with the GaN HEMT.

[0352] FIG. **7***a* illustrates another example of a combined switch according to the present disclosure, featuring a lateral GaN HEMT (**10**), an auxiliary low voltage HEMT (**20**), a pull down device (Miller clamp, **50**) and a high voltage IGBT (**40**) placed in parallel with the lateral high voltage GaN HEMT (**20**). The driving circuit for the Miller Clamp (**50**) is not shown here. For simplicity the Miller clamp may be an active device, for example it may switch according to a signal applied to the control terminal. The signal to the gate of the Miller clamp may be adjusted in relation to the signal at the control terminal for example it may inverted and/or level shifted. The Miller clamp may be monolithically integrated with the GaN HEMT (**10**), aux HEMT (**20**) and Voltage limiter (**201**).

[0353] FIG. **7***b* illustrates a combined switch according to another aspect of the present disclosure, featuring a lateral high voltage GaN HEMT (**10**), an auxiliary low voltage HEMT (**20**), a pull down device (Miller clamp, **50**) and a high voltage SiC MOSFET (or superjunction MOSFET) (**60**) in parallel with the lateral high voltage GaN HEMT (**10**).

[0354] FIG. **8** illustrates an example of the second aspect of the present disclosure. The interface circuit comprises an auxiliary low voltage HEMT (**20***a*) and a pull down device (Miller clamp, **50***a*) connected to the gate of the GaN HEMT (**10**) and an additional auxiliary low voltage HEMT (**20***b*) and an additional pull down device (Miller clamp, **50***b*) connected between the control terminal and the gate of the high voltage IGBT (**40**). The additional low voltage HEMT (**20***b*) and the additional pull down device (Miller clamp, **50***b*) enable on-chip regulation or pull-down of the gate voltage of the IGBT. The driving/control circuits of the auxiliary HEMTs and Miller clamps are not shown here for simplicity. It will be appreciated that the high voltage transistor device described herein as an IGBT may alternatively comprise a metal-oxide-semiconductor field-effect transistor (MOSFET), and/or a superjunction. The high voltage transistor device may be a silicon or silicon carbide device. The silicon carbide device may be preferred in terms of performance and efficiency while the silicon transistor such as a superjunction may be preferred in terms of price. For higher power applications (e.g. more than 10 KW), the high voltage transistor may preferably be an IGBT or a Silicon Carbide power MOSFET or a Silicon Carbide Superjunction device.

[0355] FIG. **9** illustrates the schematic shapes of on-state output I-V characteristics of the high voltage lateral GaN HEMT and the vertical IGBT at room and high temperatures. Note that the HEMT has a linear shape of the characteristics at low currents, while the IGBT does not have any current until 0.7 V and growing super-linearly initially and linearly after 0.7 V (followed by saturation). Note that the HEMT has a severe drop in the current (increased on-state resistance) at high temperatures.

[0356] FIG. **10** illustrates the schematic shapes of output on-state I-V characteristics of the combined GaN HEMT and IGBT switch according to the present disclosure. Note that the HEMT current dominates at lower currents/lower on-state voltage drops (below 0.7V)—low load, while the IGBT currents dominates at higher currents (higher on-state voltage drops). At high temperatures, the IGBT compensates the loss in the current of the HEMT. The two parallel devices offer a complementary behavior with improved performance than either the IGBT or the GaN HEMT.

[0357] FIG. **11** illustrates the schematic shapes of blocking I-V characteristics of the IGBT and high voltage lateral GaN HEMT at room temperature and high temperature. Note that in both the IGBT and the GaN HEMT the higher the temperature the higher the leakage.

[0358] Note that the IGBT breaks via avalanche and typically the avalanche voltage increases with temperature.

[0359] Note that lateral GaN HEMT typically break via an increase in the leakage current (typically between the substrate terminal and the drain terminal).

[0360] FIG. **12** illustrates schematic shapes of blocking I-V characteristics of the combined switch at room temperature and high temperature. Note that the IGBT mainly dictates the blocking characteristics and the IGBT clamps the voltage during its avalanche. The avalanche capability of

the combined switch is provided by the avalanche capability of the IGBT. The avalanche capability of the combined switch may allow the design of a more competitive GaN HEMT. As the maximum voltage across the combined switch can be limited by the avalanche voltage of the IGBT, there may be a reduced need to over-design the breakdown voltage of the GaN HEMT in order to deal with drain-to-source voltage overshoots in operation.

[0361] FIG. **13** illustrates a combined switch according to the present disclosure featuring a lateral GaN HEMT (**10**), an auxiliary low voltage HEMT (**20**), a pull down device (Miller clamp, **50**) and a high voltage IGBT (**40**) placed in parallel with the lateral high voltage GaN HEMT (**10**). A current sense HEMT (**104**) is monolithically integrated within the GaN chip (alongside the other GaN devices). The current sensing load (resistance) (**103**) could also be integrated or provided externally. Other circuit blocks such as logic circuits (**501**) to drive the miller clamp (**50**) (pull-down transistor) or voltage limiter (**201**) placed in the gate of the auxiliary HEMT are also monolithically integrated within the GaN chip.

[0362] The logic circuit can have a connection to the control terminal (external gate) and may comprise an inverter. The voltage limiter can be driven by a current source from the control terminal as shown in FIG. **15**. The circuit blocks (**50**) (**501**) (**20**) (**201**) may be described as being blocks of an overall interface circuit which operates in order to limit the maximum voltage at the gate of the GaN HEMT (for example to 7V) while a higher voltage is applied to the control terminal (for example 20V). The interface circuit is additionally configured to allow a switching signal at the gate of the GaN HEMT when a switching signal is applied to the control terminal. The switching signal may be limited in voltage as described. The interface circuit may also be configured to provide a threshold voltage increase when considering the GaN HEMT and the interface circuit in combination compared to considering the threshold voltage of the GaN HEMT as a discrete device. Through the operation of the interface circuit compatibility between the driving requirements of the GaN HEMT and the IGBT may be ensured such that they may be driven by a control signal from a single gate driver.

[0363] FIG. **14** illustrates another example of the combined switch shown in FIG. **13** wherein the IGBT is replaced by a high voltage SiC MOSFET (**60**).

[0364] In the embodiment of FIG. **15**, the voltage limiter (**201**) is connected between the gate of the auxiliary HEMT (**20**), the HEMT source terminal and the control terminal (via the current source (**204**) and slew rate control circuit (**202**)). This is an additional example of how the voltage limiter may be connected. In this configuration, the voltage limiter can limit (or clamp) the maximum voltage at the gate of the auxiliary low voltage HEMT in relation to the voltage, VDD. FIG. **15** illustrates a combined switch according to the present disclosure featuring a lateral GaN HEMT (**10**), an auxiliary low voltage HEMT (**20**), a pull down device (Miller clamp, **50**) and a high voltage IGBT (**40**) placed in parallel with the lateral high voltage GaN HEMT (**10**). Other circuit blocks such as logic signal (**503**)/logic inverter (**502**) circuits to drive the Miller clamp (**50**) or voltage limiter (**201**) placed in the gate of the auxiliary HEMT (**20**) are also monolithically integrated within the GaN chip. A voltage regulator (**203**), which may regulate an externally applied VDD to a suitable DC voltage to drive the on-chip logic circuits is included. A diode (**205**) (possibly made of a HEMT with the gate shorted to one of the source/drain terminals) could be placed in parallel with the AUX HEMT (**20**) to aid the turn-off of the high voltage GaN HEMT (**10**). The logic circuit (similar to that in FIG. **12**) can have a connection to the control terminal and may comprise a logic signal (**503**) and an inverter (**502**). The voltage limiter (**201**) can be driven by a current source (**204**) from the control terminal. A slew rate control circuit (**202**) is included to adjust the speed of the turn-on and turn-off of the GaN HEMT. This could be monolithically integrated with the high voltage GaN HEMT or provided externally. The symbol for the high voltage switch in FIG. **15** is that of an IGBT, but the high voltage switch could be another type of power semiconductor device, such as a power MOSFET or a superjunction MOSFET preferably comprising a wide band-gap (such as Silicon Carbide) or ultra-wide bandgap (such as Aluminium

Nitride) material, or silicon.
[0365] FIG. **16** is similar to FIG. **14** but with an additional start-up circuit (**206**) which could avoid the need to apply an external VDD voltage for the operation of the combination circuit and the interface circuit blocks. In this embodiment the voltage rail required by the interface circuit blocks may be generated internally through the start-up circuit from either the control terminal or the high voltage terminal (or both). The symbol for the high voltage switch in FIG. **16** is that of an IGBT, but the high voltage switch could be another type of power semiconductor device, such as a power MOSFET or a superjunction MOSFET preferably comprising a wide band-gap (such as Silicon Carbide) or ultra-wide bandgap (such as Aluminium Nitride) material, or silicon.
[0366] FIG. **17***a* illustrates a more generic structure where the Aux HEMT is embedded in the sensing and protection circuit block (**70**) which is monolithically integrated with the GaN HEMT (**10**). The Sensing and protection circuit block could comprise various functions such as voltage clamping circuits and Miller clamp devices.
[0367] FIG. **17***b* illustrates another example of the combined switch shown in FIG. **17***a* wherein the IGBT is replaced by a high voltage SiC MOSFET (**60**).
[0368] FIG. **18** illustrates another aspect of the first aspect of the present disclosure where the High Voltage GaN HEMT (**10**) could be part of a GaN Power IC (**100**). An interface circuit (**207**) has at least one connection to the control terminal and at least one connection to the internal gate of the high voltage GaN HEMT (**10**), wherein the interface allows driving voltage compatibility between the high voltage device (**40**) (e.g. IGBT) and the high voltage GaN HEMT (**10**). The GaN Power IC (**100**) may contain other devices/circuits, such as start-up (**206**) and sensing and protection circuits (**208**). The symbol for the high voltage switch in FIG. **18** is that of an IGBT, but the high voltage switch could be another type of power semiconductor device, such as a power MOSFET or a superjunction MOSFET preferably comprising a wide band-gap (such as Silicon Carbide) or ultra-wide bandgap (such as Aluminium Nitride) material, or silicon.
[0369] FIG. **19** illustrates an example of simple slew rate control circuits that can be provided externally and inserted before the Aux HEMT or in the gate of the IGBT to adjust individually the speed of the two devices. This simple method can also be used for a more balanced (or more desirable) sharing of the current during the transient voltages. Instead of the resistors and resistors with diodes, more complex slew rate circuits can be integrated monolithically alongside the high voltage GaN HEMT. The symbol for the high voltage switch in FIG. **19** is that of an IGBT, but the high voltage switch could be another type of power semiconductor device, such as a power MOSFET or a superjunction MOSFET preferably comprising a wide band-gap (such as Silicon Carbide) or ultra-wide bandgap (such as Aluminium Nitride) material, or silicon.
[0370] FIG. **20** illustrates an example where multiple high voltage GaN HEMTs can be provided in parallel with the high voltage device (IGBT). One (shown) or multiple Aux HEMTs (not shown) can be connected to the internal gate of the high voltage GaN HEMTs. Multiple parallel IGBTs (not shown) can also be connected to scale up the current capability of the combined switch. The symbol for the high voltage switch in FIG. **20** is that of an IGBT, but the high voltage switch could be another type of power semiconductor device, such as a power MOSFET or a superjunction MOSFET preferably comprising a wide band-gap (such as Silicon Carbide) or ultra-wide bandgap (such as Aluminium Nitride) material, or silicon.
[0371] FIG. **21** shows multiple (shown two) Power ICs as were illustrated in FIG. **17**. The two Power ICs are connected in parallel. Additionally, the combination of two Power ICs in parallel, can be provided in parallel with the high voltage device (IGBT). The symbol for the high voltage switch in FIG. **21** is that of an IGBT, but the high voltage switch could be another type of power semiconductor device, such as a power MOSFET or a superjunction MOSFET preferably comprising a wide band-gap (such as Silicon Carbide) or ultra-wide bandgap (such as Aluminium Nitride) material, or silicon.
[0372] FIG. **22** shows series of multiple high voltage HEMTs (here shown only two) can be

provided instead of a single GaN HEMT. This could be a solution if higher blocking voltages (e.g. in excess of 1.2 kV) are needed. A level shifter (**105**) could be used for the upper GaN HEMT (**12**). The level shifter could be monolithically integrated with the lower GaN HEMT (**11**) or provided externally. The symbol for the high voltage switch in FIG. **22** is that of an IGBT, but the high voltage switch could be another type of power semiconductor device, such as a power MOSFET or a superjunction MOSFET preferably comprising a wide band-gap (such as Silicon Carbide) or ultra-wide bandgap (such as Aluminium Nitride) material, or silicon.

[0373] FIG. **23** illustrates another embodiment of the present disclosure where a silicon companion chip (**2000**) can be co-packaged with the Power HEMT (**10**). The Miller clamp (**50**) can be monolithically integrated with the GaN HEMT (**10**). The silicon companion chip can provide an interface allowing a compatible voltage range for driving the GaN HEMT (**10**) and the IGBT (**40**). The companion chip (**2000**) can provide voltage clamping action, slew rate control, high side drive and other sensing and protection features. It can have programmable functions and can be made in mix-signal processes which allow both digital and analogue components to be integrated. A BCD (Bipolar CMOS DMOS) process can be used as an example. The symbol for the high voltage switch in FIG. **23** is that of an IGBT, but the high voltage switch could be another type of power semiconductor device, such as a power MOSFET or a superjunction MOSFET preferably comprising a wide band-gap (such as Silicon Carbide) or ultra-wide bandgap (such as Aluminium Nitride) material, or silicon.

[0374] FIG. **24***a* illustrates a schematic cross-section representation and connections between the lateral high voltage GaN HEMT, the Aux GaN HEMT and a trench IGBT.

[0375] FIG. **24***b* illustrates a schematic cross-section representation and connections between the lateral high voltage GaN HEMT, the Aux GaN HEMT and a SiC MOSFET.

[0376] FIG. **25** illustrates a schematic representation of the equivalent circuit and connections between the lateral high voltage GaN HEMT (**10**), an interface circuit (**207**) comprising the Aux GaN HEMT, and an IGBT. The IGBT is described as a combination between an n-channel MOSFET (**91**) and a bipolar PNP transistor (**92**) with the drain of the n-channel MOSFET being connected to the base of the PNP transistor.

[0377] FIG. **26***a* illustrates a combined switch comprising an IGBT (**40**) and a GaN Power IC (**100**) further comprising a high voltage GaN HEMT (**10**) and an interface (**207**) which has at least one connection to the control terminal and at least one connection to the internal gate of the high voltage GaN HEMT. An extra high voltage anti-parallel diode (**90**) is added to aid the reverse conduction. This diode could become in parallel with the existing intrinsic 2 DEG reverse conducting diode of the high voltage GaN HEMT. The extra diode could be part of a Reverse Conducting IGBT (RC IGBT) or could be an independent bipolar diode such as a high voltage PIN diode, or could be a Schottky or Schottky-based (e.g. Junction Barrier Schottky) diode made in silicon or silicon carbide.

[0378] FIG. **26***b* illustrates another example of the combined switch illustrated in FIG. **26***a*. A series combination of multiple anti-parallel diodes (at least two) is added in parallel to the GaN HEMT. At least one of the diodes may be a high voltage diode. During the steady-state conduction, the on-state voltage drop of these diodes may be higher, however, in light load conditions, when the current are small, the body diode of the GaN HEMT (existing 2 DEG reverse conducting diode) will take most of the current and offer zero reverse recovery switching losses during transient signals. The series diodes are designed to have a cumulative on-state voltage drop larger than that of the body diode of GaN HEMT at low currents and thus will conduct little or virtually no current in light load conditions. The additional series diodes will nevertheless carry current at medium and high loads and in surge conditions. The extra diodes could be independent bipolar diodes made in silicon or silicon carbide. At least one of the diode may preferably be a high voltage PIN diode.

[0379] FIG. **26***c* illustrates an example of a combined switch comprising a SiC MOSFET (**60**) and a GaN Power IC (**100**) further comprising a high voltage GaN HEMT (**10**) and an interface (**207**)

which has at least one connection to the control terminal and at least one connection to the internal gate of the high voltage GaN HEMT. The SiC MOSFET (**60**) and GaN HEMT (**10**) have incorporated within their body diodes, which are active during reverse conduction. The body diode of a SiC MOSFET does not conduct until 2.3 V (across its terminals) while the body diode of a GaN HEMT would conduct from 1.5V, (when a Miller clamp is present) therefore at low currents, in light load conditions, GaN HEMT body diode will conduct most or virtually all the reverse current. As medium loads there will be more natural current sharing between the two diodes, and at high reverse currents or surge conditions the SiC body diode will conduct most of the current.
[0380] Therefore, an external anti-parallel diode may no longer be needed, saving cost. The body diode of the GaN HEMT (through its 2 DEG channel) has zero reverse recovery losses, unlike the bipolar body diode of the SiC IGBT. That is to say that the body diode of the GaN HEMT (with the gate terminal of the HEMT shorted to its source terminal) has significantly better efficiency than the SiC body diode at light loads. At medium and high loads, when the current levels are significantly higher, both diodes may conduct with the SiC body diode taking an increased proportion of the current as the total current becomes larger.
[0381] FIG. **27** illustrates a device according to a third aspect of the present disclosure, comprising a Cascode device in parallel with an IGBT. The Cascode device comprises a MOSFET (**93**) (an n-channel MOSFET made preferably in silicon or silicon carbide technology) in series with a high voltage depletion mode HEMT (**95**) (made in III-Nitride material). The gate of the depletion mode GaN HEMT is connected to the source of the MOSFET. The symbol for the high voltage switch in FIG. **27** is that of an IGBT, but the high voltage switch could be another type of power semiconductor device, such as a power MOSFET or a superjunction MOSFET preferably comprising a wide band-gap (such as Silicon Carbide) or ultra-wide bandgap (such as Aluminium Nitride) material or silicon.
[0382] FIG. **28** illustrates a device according to a fourth aspect of the present disclosure, comprising a MOSFET (**93**) (n-channel MOSFET, preferably in silicon or silicon-carbide technology), a high voltage depletion mode HEMT (**95**) and a PNP transistor (**94**) (bipolar junction transistor). The drain of the n-channel MOSFET is connected to the base of the high voltage PNP transistor and also to the source of the high voltage depletion mode HEMT.
[0383] The n-channel MOSFET is responsible for both (i) enabling a negative gate-source voltage for the depletion HEMT during the blocking mode and (ii) providing the electron current to the base of the pnp transistor in the on-state. Preferably the MOSFET is an n-channel stand-alone component made in silicon or silicon-carbide technology and the high voltage PNP transistor could be made in silicon or silicon-carbide technology. The high voltage PNP transistor could have a vertical configuration with a wide n base and a relatively narrow p collector or a relatively narrow n base and a relatively wide p collector.
[0384] FIG. **29** illustrates a device according to a fifth aspect of the present disclosure. The Cascode device in FIG. **28** is replaced with a high voltage depletion mode HEMT based on p+ islands in series with a MOSFET (as described in U.S. Pat. No. 11,081,578). The two series devices are further placed in parallel with the pnp transistor.
[0385] The gate of the p+ islands depletion mode HEMT could be connected through an interface (**207**) to the control terminal. The interface could be the same as the one described earlier in the first aspect of this disclosure. The role of such interface is to adapt the driving voltage of the control terminal to that suitable and allowable for the p+ islands depletion mode GAN HEMT.
[0386] FIG. **30** illustrates an example of a voltage limiter (**2011**). In this example the voltage limiter comprises an enhancement mode HEMT and two resistors. One terminal of the voltage limiter may be connected to the gate of the auxiliary HEMT and the other terminal may be connected to the source terminal of the GaN HEMT or to a voltage VDD as illustrated in previous examples.
[0387] FIG. **31** illustrates an additional example of a voltage limiter (**2012**). In this example the

voltage limiter comprises two enhancement mode HEMTs in series connected in a diode-like manner. A different number of enhancement mode HEMTs in series may be used in other examples depending on the desirable voltage limit of the circuit.

[0388] FIG. **32** illustrates an additional example of the voltage limiter (**2013**), similar to FIG. **30**, which also comprises a current source. The current source is useful in setting the voltage limit of the voltage limiter while controlling the power dissipation of the circuit in operation.

[0389] Returning to FIG. **4**, a combined switch may comprise, in examples, a lateral GaN Power HEMT (**10**) (i.e. a high voltage HEMT), an interface circuit (**207**) and a high voltage transistor device (**30**) (e.g. an IGBT). The turn-on of the combined switch is faster than that of an IGBT alone as the internal input capacitance of the high voltage HEMT is very small compared to the input capacitance of the IGBT and therefore it could be charged quickly. The turn-off the combined switch is faster than that of an IGBT alone as the GaN HEMT is a unipolar device and there is no excess charge (i.e. plasma) present in the GaN HEMT. Moreover during the turn-off the current may redistribute compared to the on-state or steady-state. Thus a larger proportion of the current may be switched off by the high voltage GaN HEMT, minimizing the tail of the IGBT component in the combined switch. As a result the turn-off tail and turn-off losses can be smaller in a combined switch than an IGBT alone.

[0390] FIG. **33***a* illustrates an example according to the present disclosure, featuring a multiple input III-nitride (e.g. GaN) power HEMT with individual connections for driving the gates of the GaN power HEMT (**10**) and high voltage switch (**40**). In the example illustrated in FIG. **33***a*, the HEMT is part of a GaN power integrated circuit (IC). The symbol for the high voltage switch in FIG. **33***a* is that of an IGBT, but the high voltage switch could be another type of power semiconductor device, such as a power MOSFET or a superjunction MOSFET preferably comprising a wide band-gap (such as Silicon Carbide) or ultra-wide bandgap (such as Aluminium Nitride) material. An optional interface circuit (**207**) may be placed in front of the gate of the lateral GaN power HEMT (**10**) to adapt the driving voltage from the driver to that suitable and allowable for the GaN power HEMT (**10**). This interface could be preferably monolithically integrated with the power HEMT for providing lower parasitics, ease of manufacturing and fast reaction time. Alternatively, this interface could be part of a separate chip (such as a silicon companion chip, or a driver chip). Alternatively, this interface could be integrated within the driver. The interface circuit may additionally include pass transistors (e.g. a low power HEMT), diodes, voltage regulators, voltage limiters, clamping circuits, sensing and protection functions, pull-down devices, such as a Miller clamp, to ensure a fast and safe turn-off, to enhance immunity against dV/dt and to absorb any transient voltage peaks on the gate.

[0391] Multiple inputs of the GaN power IC are configured to have different driving voltage levels and/or slew rates and/or timing sequences when the power IC is in the on-state, off-state, turn-on and turn-off modes. This may enable dynamic control of the IGBT slew rate and turn on and turn off curves while GaN power IC has its own input from the driver. The resistors RG**1**, RG**2**, RG**3** can be provided externally or inserted before the interface circuit for the power HEMT (**10**) and the gate of the IGBT (**40**) to adjust individually the turn-on and turn-off speed of the two devices. The VDD voltage needed as a DC rail for the interface circuit, could be provided internally via a start-up structure (not shown) or could be the same as the VDD supplied to the driver.

[0392] In the example shown in FIG. **33***a*, the turn-on and turn-off of the GaN Power IC are driven by gate G**1** through the same path OUT**1**. Gate G**2** of IGBT may receive driving signal from two outputs of the driver OUT**1** and OUT**2** which can be configured for turn-on and turn-off signals, respectively. This helps in controlling the slew rate of the IGBT by adjusting the resistor values and delaying the gate driving signals. The resistors RG**1**, RG**2** etc. can help dynamically control and modulate the turn-on speeds of the switches. During the turn-on, the GaN power HEMT can take higher current than during the on-state or steady state (as much as the saturation current) until the IGBT turns-on fully and the current is redistributed (part of the current from the GaN power HEMT

would be redistributed in the IGBT). As a result, the turn-on losses in a combined switch may be smaller than in an IGBT or a first transistor alone. Alternatively, the connections between the outputs (e.g. OUT**1**, OUT**2**, OUT**3**) of the driver and the inputs of the interface circuit or the gate of the high voltage switch (e.g. G**1**, G**2**) may contain resistors in parallel with series branches of resistors and diodes to differentiate between turn-on and turn-off speeds. In FIG. **33***a* only one power HEMT **10** and one high voltage switch **40** are shown. It may be understood that multiple HEMT devices in parallel could replace the HEMT **10**, or multiple high voltage switches (e.g. vertical IGBTs or Silicon Carbide MOSFETs) could replace the high voltage switch **40**. It may also be understood that the semiconductor switch may comprise the combination of a cascode device with a high voltage switch or other alternative configurations as illustrated in previous embodiments. For example, a module or a package can house a combined switch which could comprise multiple vertical IGBTs in a combination with a single Power HEMT. A multiple output driver can drive the module as described above.

[0393] FIG. **33***b* illustrates a further example of the aspect depicted in FIG. **33***a* featuring a multiple input semiconductor switch power IC with individual connections for driving the gates of the GaN power HEMT (**10**) and high voltage switch (**40**), wherein the high voltage switch may be a SiC MOSFET (**60**).

[0394] FIG. **33***c* illustrates a further example of the aspect depicted in FIG. **33***a* featuring a multiple input semiconductor switch power IC, wherein the GaN HEMT is replaced by a Cascode device. The Cascode device comprises a MOSFET (**93**) (an n-channel MOSFET made preferably in silicon or silicon carbide technology) in series with a high voltage depletion mode HEMT (**95**) (made in III-Nitride material). The gate of the depletion mode GaN HEMT is connected to the source of the MOSFET. The cascode examples shown in FIG. **28** and FIG. **29** are also applicable. The symbol for the high voltage switch in FIG. **33***c* is that of an IGBT, but the high voltage switch could be another type of power semiconductor device, such as a power MOSFET or a superjunction MOSFET preferably comprising a wide band-gap (such as Silicon Carbide) or ultra-wide bandgap (such as Aluminium Nitride) material, or silicon.

[0395] FIG. **33***d* illustrates a further example according to the present disclosure, featuring a multiple input semiconductor switch power IC with individual connections for driving the gates of the GaN power HEMT (**10**) and high voltage switch (**40**). Compared to FIG. **33***a*, FIG. **33***d* shows an additional feedback control circuit (**301**) preferably integrated within the GaN Power IC. The role of this circuit is to provide a feedback signal to the driver about the state of the combined switch. The feedback control circuit could comprise sensing circuits such as current sensing or short-circuit sensing and provide this information to the driver. The driver could utilize this information to adjust the voltage levels on OUT**1**, OUT**2**, OUT**3**, or the time sequence or the slew-rates to provide (i) increased performance (ii) enhanced reliability. The decision regarding the feedback can come from an additional controller or can be embedded within the driver. As an example, the feedback control may detect the voltage across the combined switch and at higher voltages (e.g. above 5V) it may lower the voltage level applied to the gate of the GaN Power HEMT **10**. The switching frequency or time sequences could also change as a function of the feedback loop control. Another scenario can be when the feedback control circuit detects the current or the temperature in the GaN Power HEMT **10** exceed a certain level, the driver output voltage is configured to take certain actions such as either lower the gate voltage applied to the gate of the Power HEMT **10** or shut off the GaN Power HEMT for a period of time or depending on other threshold levels for current or temperature. In this period, the vertical switch **40** driving signal may not be affected, and the vertical switch may handle the extra load current. The feedback loop circuit can be monolithically integrated with the Power HEMT, **10**. It can also be a part of or regarded as being a part of the interface circuit. The feedback loop circuit can gather certain information regarding the status of the GaN Power IC, such as the current in the Power HEMT **10** or the voltage across the drain-source terminals of Power HEMT **10** or the temperature within the

GaN Power IC, however not limiting to only these conditions. As an additional control, the feedback signal may also be provided to the interface circuit to internally control the GaN power HEMT while the driver controls the device externally. The feedback control circuit may be provided in the subsequent embodiments of the invention, however it is not shown for simplicity. This aspect is also applicable to the examples shown in FIG. **33***b* and FIG. **33***c*. The symbol for the high voltage switch in FIG. **33***d* is that of an IGBT, but the high voltage switch could be another type of power semiconductor device, such as a power MOSFET or a superjunction MOSFET preferably comprising a wide band-gap (such as Silicon Carbide) or ultra-wide bandgap (such as Aluminium Nitride) material, or silicon.

[0396] FIG. **33***e* illustrates a further example of the first aspect of the present disclosure, featuring a multiple input semiconductor switch power IC with individual connections for driving the gates of the GaN power HEMT (**10**) and high voltage switch (**40**). In this embodiment, the feedback control circuit **301** shown in FIG. **33***d* is exemplified by a Sense HEMT **104**. The Sense HEMT **104** is a scaled down, identical version of the Power HEMT (e.g. by an area of 10 to 1000×). The Sense HEMT could be integrated monolithically with the Power HEMT. The Sense HEMT can directly sense the current of the Power HEMT and this information can be communicated directly or indirectly (for example through the voltage signal across a current sensing load as shown in FIG. **14**) to the driver. The driver (or a separate controller—not shown) could decide to change the driving voltages, time sequence, slew rates or frequency of the output pins to the combination switch, function of the feedback provided. As an additional control, the feedback signal may also be provided to the interface circuit to internally control the GaN power HEMT while the driver controls the device externally. The symbol for the high voltage switch in FIG. **33***e* is that of an IGBT, but the high voltage switch could be another type of power semiconductor device, such as a power MOSFET or a superjunction MOSFET preferably comprising a wide band-gap (such as Silicon Carbide) or ultra-wide bandgap (such as Aluminium Nitride) material, or silicon.

[0397] FIG. **34** illustrates another example according to the present disclosure, where the gate of the high voltage switch **40** (e.g. IGBT) is also driven through the interface circuit **207**, preferably incorporated within the GaN Power IC. The interface circuit **207** can internally control the lead/lag and slew rates of the operation of the switches through additional circuits such as logic circuits, signal conditioning circuits, latch circuits, delay circuits, networks of resistors and capacitors etc. Additionally, the interface circuit can provide functionality of clamping, voltage limiting, voltage regulation, sensing and protection and other control functions for the high voltage transistor (**40**), and/or for the GaN Power HEMT (**10**). The symbol for the high voltage switch in FIG. **34** is that of an IGBT, but the high voltage switch could be another type of power semiconductor device, such as a power MOSFET or a superjunction MOSFET preferably comprising a wide band-gap (such as Silicon Carbide) or ultra-wide bandgap (such as Aluminium Nitride) material, or silicon.

[0398] FIG. **35** illustrates a further example according to the present disclosure, where each switch or device (**10**) or (**40**) may be driven by respective gate signals where the turn-on and turn-off signals are provided separately. This may assist in adjusting the speed of the switches by selecting the values of the resistors. This can also be used for a more balanced (or more desirable) sharing of the current during the transient voltages. These resistors may be provided externally or incorporated already in the driver. Monolithically integrated slew rate circuits can also serve this purpose, however, having this external mechanism provides flexibility of dynamically controlling and adjusting the speeds and slew rate resulting in a universal switch that can be adapted for various applications. The symbol for the high voltage switch in FIG. **35** is that of an IGBT, but the high voltage switch could be another type of power semiconductor device, such as a power MOSFET or a superjunction MOSFET preferably comprising a wide band-gap (such as Silicon Carbide) or ultra-wide bandgap (such as Aluminium Nitride) material, or silicon.

[0399] FIG. **36** illustrates an example according to the present disclosure, wherein the power IC is configured to have multiple turn-off gate driving inputs to adjust the turn-off speed. These turn-off

inputs may be independently provided for the GaN power HEMT **10** and the high voltage switch **40** (IGBT). A multi-output driver with independent outputs for High and Low signals would drive this switch. For example, as shown in FIG. **36**, there may be a single turn-on pin G**1** to turn-on the GaN power HEMT **10** through the interface circuit **207** and the high voltage switch **40** (IGBT) directly. There may be multiple turn-off pins such as G**2** and G**3** for GaN power HEMT **10**, and G**4** and G**5** for high voltage switch (IGBT). The symbol for the high voltage switch in FIG. **36** is that of an IGBT, but the high voltage switch could be another type of power semiconductor device, such as a power MOSFET or a superjunction MOSFET preferably comprising a wide band-gap (such as Silicon Carbide) or ultra-wide bandgap (such as Aluminium Nitride) material, or silicon.

[0400] In the example illustrated in FIGS. **36**, G**2** and G**4** may be providing the regular turn-off signal to the GaN Power HEMT **10** (through the interface circuit **207**) and the high voltage switch **40** (IGBT), respectively. Additionally, G**3** and G**5** are configured to provide delayed or slower turn-off signal for slow turn-off of the GaN power HEMT **10** and high voltage switch **40** (IGBT), respectively. Based on the application of the switch, RG**3** and RG**5** would be significantly higher than RG**2** and RG**4** to enable the slower turn-off. As an example, if RG**2** is 5 Ohm then RG**3** may be 10 Ohm.

[0401] FIG. **37** illustrates an example of a semiconductor switch according to the present disclosure where the power HEMT **10** and high voltage switch **40** (IGBT) are configured to have their own turn-on pins (G**1**, G**4**). Although the example shows one turn-on input and two turn-off inputs for each transistor (HEMT and IGBT), it will be understood that there may be additional turn-on/turn-off connections based on the requirement of the application of the power IC. These may provide options for additional slew rate control during turn-on/turn-off. The power IC can be operated through a conventional single output driver, by shorting the gate pins and providing resistances internally. Alternatively, the slow turn-on/turn-off pins may be left unconnected if there is no need to modulate the turn-on/turn-off speed or slew rate. Thus, the proposed power IC is a configurable semiconductor switch power IC where the turn-on/turn-off speeds/slew-rate can be dynamically controlled. The symbol for the high voltage switch in FIG. **37** is that of an IGBT, but the high voltage switch could be another type of power semiconductor device, such as a power MOSFET or a superjunction MOSFET preferably comprising a wide band-gap (such as Silicon Carbide) or ultra-wide bandgap (such as Aluminium Nitride) material or silicon.

[0402] FIG. **38** illustrates a simplified example of the interface circuit **207**. Other examples of interface circuits **207** described herein, such as the example illustrated in FIG. **15**, may also be suitable for use with the examples illustrated in FIGS. **33** to **37** of the present disclosure. As an example, the auxiliary gate interface (**200**) comprises an auxiliary low power HEMT and a voltage limiter. The voltage limiter may be a circuit block which can limit (or clamp) the maximum voltage at the gate of the auxiliary low power HEMT. Through this manner of operation, the voltage limiter may overall act to provide a limit on the maximum voltage on the gate terminal of the GaN power HEMT. The auxiliary low power HEMT and the voltage limiter may be monolithically integrated with the GaN power HEMT. The symbol for the high voltage switch in FIG. **38** is that of an IGBT, but the high voltage switch could be another type of power semiconductor device, such as a power MOSFET or a superjunction MOSFET preferably comprising a wide band-gap (such as Silicon Carbide) or ultra-wide bandgap (such as Aluminium Nitride) material or silicon.

[0403] Additionally, the interface circuit **207** may include a pull down device (Miller clamp MC**1**) and its associated driving circuit. For simplicity, the Miller clamp may be an active device (e.g. a low voltage HEMT), for example it may switch according to a signal applied to its gate terminal.

[0404] It may be desirable to have two pull-down transistors (i.e. two Miller Clamp transistors) connected in the same manner as they may be optimized for different functions. One of the Miller clamp transistors (**50***a*) may be optimized to enable fast turn-off the GaN power HEMT (**10**) and/or to avoid a false turn-on of the GaN power HEMT (**10**) during regular operation of the power electronics circuit. In this case, it may be preferable for the Miller clamp transistor to have a low

on-state resistance, for example <10Ω. The second transistor (**50***b*) may be optimized to turn-off the power HEMT when a slow turn-off is selected based on the input on the slow turn-off pin G**3**, as described in previous examples. In this case, it may be preferable for the transistor **50***b* to have a higher on-state resistance (e.g. >10Ω) than the Miller clamp transistor (**50***a*) intended to operate during regular operation of the device. This may be desirable in order to slow down the turn-off of the power HEMT (or decrease its slew rate during turn-off) and avoid any overvoltage across the power HEMT (for example between its drain and source terminals) due to parasitics in the circuit, for example due to a L*dl/dt voltage being generated across parasitic inductances in the power loop.

[0405] During the slow turn-off, the logic circuit may also activate the Miller Clamp HEMT intended for regular operation (**50***a*) subsequently (e.g. through a delay circuit), enabling slow turn off via the slow miller clamp (MC**2**), but ensuring high dV/dt immunity in steady state from the main miller clamp (MC**1**). As an example, the delay circuit may be triggered through an AND operation of the high signal on G**3** and the gate voltage of power HEMT below a threshold voltage to activate MC**1** to provide additional dV/dt immunity.

[0406] FIG. **39** illustrates an alternative example according to the present disclosure, where all the gate driving signals pass through the interface circuit. In this example, the various output low pins may operate like ‘turn off mode selectors’ and the resultant turn off speed would be set inside the interface circuit, depending on which driver pin was pulled low. The symbol for the high voltage switch in FIG. **39** is that of an IGBT, but the high voltage switch could be another type of power semiconductor device, such as a power MOSFET or a superjunction MOSFET preferably comprising a wide band-gap (such as Silicon Carbide) or ultra-wide bandgap (such as Aluminium Nitride) material or silicon.

[0407] FIG. **40***a* illustrates another example according to the present disclosure, comprising a combined switch with a discrete GaN switch (Power HEMT, **10**) and a vertical high voltage switch **40** (e.g. IGBT). As already mentioned, the vertical high voltage switch **40** can also be a Silicon Carbide vertical power MOSFET or a Silicon Carbide Superjunction. The possibility of having different driving voltages at the independent gates of the GaN power HEMT and the vertical high voltage switch can eliminate the requirement of an interface circuit which is needed to limit the voltage at the gate of the GaN power HEMT. As the voltage is externally controlled, the voltage levels and the turn-on and turn-off speeds and timings can be directly controlled through the external driver, and possibly other external components such as resistors and diodes. The resistors RG**1**, RG**2** and RG**3** can be external (preferably) or integrated in the driver (alternatively) and can set the speed of the turn-off and turn-on of the GaN power HEMT (**10**). To increase the dv/dt immunity and avoid false turn-on events, a Miller clamp may still be connected between the gate and source of the power HEMT. As an example, assuming G**1** is the fastest, G**2** and G**3** the resistors RG**1**, RG**2**, RG**3** may have a ratio of 1:5:10 of the resistance values. As an example, the voltage levels associated with the high voltage switch, **40** (e.g. IGBT) can be from −5V to 15V, while the voltage levels associated with the discrete GaN power HEMT (**10**) could be −3V to 7V.

[0408] FIG. **40***b* illustrates another example according to the present disclosure, comprising a combined switch with a cascode device and a vertical high voltage switch **40** (e.g. IGBT). The Cascode device comprises a MOSFET (**93**) (an n-channel MOSFET made preferably in silicon or silicon carbide technology) in series with a high voltage depletion mode HEMT (**95**) (made in III-Nitride material). The gate of the depletion mode GaN HEMT is connected to the source of the MOSFET. The symbol for the high voltage switch in FIG. **40***b* is that of an IGBT, but the high voltage switch could be another type of power semiconductor device, such as a power MOSFET or a superjunction MOSFET preferably comprising a wide band-gap (such as Silicon Carbide) or ultra-wide bandgap (such as Aluminium Nitride) material, or silicon.

[0409] FIG. **41** illustrates another example similar to the example shown in FIG. **40***a*, the example of FIG. **41** comprising a combined switch with a discrete GaN switch (Power HEMT, **10**) and a

vertical high voltage switch **40** (e.g. IGBT) driven through different voltages at the independent gates of the GaN power HEMT and the vertical high voltage switch (e.g. IGBT). Additionally, one Miller Clamp each (**50***c*, **50***d*) is connected to the gate of the power HEMT and the IGBT, respectively. The additional Miller clamp, **50***d* enables on-chip regulation or pull-down of the gate voltage of the IGBT. Both Miller clamps could be preferably integrated monolithically with the Power HEMT in the GaN Power IC. The symbol for the high voltage switch in FIG. **41** is that of an IGBT, but the high voltage switch could be another type of power semiconductor device, such as a power MOSFET or a superjunction MOSFET preferably comprising a wide band-gap (such as Silicon Carbide) or ultra-wide bandgap (such as Aluminium Nitride) material or silicon.

[0410] FIG. **42** illustrates an example according to the present disclosure comprising the semiconductor switch power IC with an additional start-up circuit (**206***a*) which may avoid the need to apply an external VDD voltage for the operation of the integrated circuit and the interface circuit blocks. In this example the voltage rail required by the interface circuit blocks may be generated internally through the start-up circuit from either the control terminal or the high voltage terminal (or both). The start-up circuit may comprise voltage regulators, voltage limiters, capacitors, depletion mode transistors, pass transistors and/or diodes. The symbol for the high voltage switch in FIG. **42** is that of an IGBT, but the high voltage switch could be another type of power semiconductor device, such as a power MOSFET or a superjunction MOSFET preferably comprising a wide band-gap (such as Silicon Carbide) or ultra-wide bandgap (such as Aluminium Nitride) material or silicon.

[0411] FIG. **43** illustrates another example according to the present disclosure. The dynamic adjustment of turn-off/turn-on speeds of the switch can also be applied to a GaN power IC that may not have an IGBT in parallel. As described above, one of the Miller clamp transistors (MC**1**) may be optimized to enable fast turn-off the power HEMT and/or to avoid a false turn-on of the power HEMT during regular operation of the power electronics circuit through G**2**. In this case, it may be preferable for the Miller clamp transistor to have a low on-state resistance, for example <10Ω. The second transistor (**50***b*) may be optimized to turn-off the power HEMT when a slow turn-off is selected based on the input on the low turn-off pin G**3**, to delay the turn-off of the device as described in previous examples. In this case it may be preferable for the transistor **50***b* to have a higher on-state resistance (e.g. >10Ω) than the Miller clamp transistor (**50***a*) intended to operate during regular operation of the device. This may be desirable in order to slow down the turn-off of the power HEMT and avoid any overvoltage across the power HEMT (for example between its drain and source terminals) due to parasitics in the circuit, for example due to a L*dl/dt voltage being generated across parasitic inductances in the power loop. Therefore, this multi-input configuration is beneficial for modulating even a GaN power IC. The Auxiliary gate interface **200** in FIG. **43** plays the role of a voltage regulator, and may be absent if the driver is capable to drive the GaN HEMT at lower voltages (e.g. −3 V to 7V) than those specific to the high voltage switch (e.g. −5 to 15V).

[0412] FIG. **44** illustrates an alternative example of the example shown in FIG. **44**, wherein a single low voltage HEMT with multiple gates may be used as a Miller Clamp (**50***e*) to pull down the power HEMT during turn-off operations. The multiple gates can provide different on-resistances of the Miller Clamp when active. As described herein, the Auxiliary gate interface in FIG. **44** plays the role of a voltage regulator, and may be absent if the driver is capable to drive the GaN HEMT at lower voltages (e.g. −3V to 7V) than those specific to the high voltage switch (e.g. −5 to 15V).

[0413] FIG. **45** illustrates an alternative example of the power IC comprising a power HEMT switch without an auxiliary interface circuit. This may be possible if the driver is capable to drive the GaN HEMT at lower voltages (e.g. 0V to 7V) through the turn-on gate terminal and therefore, a voltage regulator may not be needed.

[0414] The power IC comprises a pull down device (Miller Clamp MC**1**) and its associated driving

circuit (logic circuit **501**). For simplicity, the Miller clamp may be an active device, for example it may switch according to a signal applied to the turn-off terminals. The Miller clamp transistor is configured to enable fast turn-off the power HEMT and/or to avoid a false turn-on of the power HEMT during regular operation of the power electronics circuit. In this case, it may be preferable for the Miller clamp transistor to have a low on-state resistance, for example <10Ω.
[0415] Additionally, a start-up circuit (**206***a*) is provided which is configured to avoid the need to apply an external VDD voltage for the operation of the integrated circuit and the interface circuit blocks. In this embodiment, the voltage rail required by the interface circuit blocks may be generated internally through the start-up circuit from the high voltage terminal. Alternatively, the voltage rail required by the interface circuit blocks may be generated through the start-up circuit (**206***b*) from the external gate terminal (turn-on gate terminal) as shown in FIG. **46**.
[0416] FIG. **47** illustrates an example of a method **470** of operating a semiconductor switch according to the present disclosure. The semiconductor switch may comprise any of the example semiconductor switches (also referred to as 'combined switches') illustrated in FIGS. **33** to **46**, and described herein, and may comprise a high voltage HEMT (e.g. a GaN HEMT) comprising a high voltage HEMT terminal operatively connected to a control terminal, and a high voltage transistor device (e.g. a vertical device such as an IGBT), the high voltage transistor device comprising a transistor device gate terminal. For example, in a step S**472**, the method **470** comprises driving the control terminal, by a driver via a first driver output, at a first driving voltage. In a step S**474**, the method **470** comprises diving the transistor device gate terminal, by the driver via a second driver output, at a second driving voltage.
[0417] Examples of semiconductor switches that may be suitable for use in phase inverters will now be described.
[0418] For example, described herein is a parallel combination between a 3-level inverter based on a HEMT (e.g. a III-nitride HEMT) and a two-level inverter based on a high voltage transistor device such as an IGBT, a MOSFET, or a superjunction. The high voltage transistor device may be a silicon or silicon carbide device.
[0419] FIG. **50** illustrates a simplified example of a semiconductor switch **101** suitable for use as part of an inverter as described herein. The semiconductor switch **101** comprises a first branch comprising a first lateral semiconductor transistor device **12** (e.g. a GaN HEMT) and a second lateral semiconductor transistor device **11** (e.g. a GaN HEMT) connected in series. A second branch comprises a high voltage vertical semiconductor transistor device **40** (e.g. a Si IGBT). The first branch and the second branch are connected in parallel. A maximum voltage rating of the high voltage vertical semiconductor transistor device **40** is significantly greater (e.g. by a factor of 1.5 or more, or a factor of 2 or more) than the maximum voltage ratings of the lateral semiconductor transistor devices **12**, **11**. Further, it may be understood that the high voltage vertical semiconductor transistor device **40** (e.g. a Si IGBT) may comprise a body diode between its main terminals (emitter, collector). Each of the lateral semiconductor transistor devices **12**, **11**, and the high voltage vertical semiconductor transistor device **40**, may have gates that are each operatively connected to distinct control terminals (first control terminal G**1**, second control terminal G**2**, and third control terminal G**3**) that are operable by a driver or controller. For example, the driver or controller may provide at least one of a first control signal, a second control signal, and a third control signal to at least one of the control terminals G**1**, G**2**, G**3** to drive the transistor devices **12**, **11**, **40**. Additionally, the semiconductor switch may also have a mid terminal M**1** connected to the mid-point between the first lateral semiconductor transistor device **12** and the second lateral semiconductor transistor device **11** to access the DC mid-point between the two lateral semiconductor transistor devices.
[0420] FIG. **51***a* illustrates an additional example of a semiconductor switch **101***a*. The semiconductor switch **101***a* illustrated in FIG. **51** is similar to the semiconductor switch **101** illustrated in FIG. **50**, but additionally comprises a first interface circuit **207_2** operatively

connected between the first control terminal G**1** and the first lateral semiconductor transistor device **12**, and a second interface circuit **207_1** operatively connected between the second control terminal G**2** and the second lateral semiconductor transistor device **11**. In some examples (not shown) an interface circuit (e.g. a third interface circuit) may be connected between the third control terminal G**3** and the vertical semiconductor transistor device **40**. Various examples of interface circuits have been described herein, for example the interface circuit **207** illustrated in FIG. **4** and its variations in FIGS. **5**, **6**, **7**, **8**, **13**, **14**, **15**, **16**, and may be suitable as the first **207_2**, second **207_1**, and/or third interface circuit(s) of the semiconductor switch **101***a*.

[0421] FIG. **51***b* illustrates a further example of a semiconductor switch **101***b*, similar to the semiconductor switch **101** illustrated in FIG. **50**. The semiconductor switch **101***b* illustrated in FIG. **52** includes an example of an interface circuit (e.g. a GaN interface circuit) that may be connected between the first control terminal G**1** and the first lateral semiconductor transistor device **12**, and between the second control terminal G**2** and the second lateral semiconductor transistor device **11**. Similarly to other examples described herein (see e.g. FIG. **22**), the interface circuit may comprise a first auxiliary HEMT **20_1** connected between the first control terminal G**1** and the first lateral semiconductor transistor device **12**, and a second auxiliary HEMT **20_2** connected between the second control terminal G**2** and the second lateral semiconductor transistor device **11**. The connections of the gate terminal for auxiliary HEMTs are not shown for simplicity. The interface circuits may comprise additional circuitry connected to the different terminals of the auxiliary HEMTs and the lateral semiconductor transistor devices. For example, the interface circuits may each additionally comprise a voltage limiter connected between the gate of an auxiliary HEMT and the source of respective lateral semiconductor transistor device with an input from the respective control terminal. The voltage limiter may be a circuit block which can limit (or clamp) the maximum voltage at the gate of respective auxiliary HEMT. Through this manner of operation, the voltage limiter may overall act to provide a limit on the maximum voltage on the gate terminal of the lateral semiconductor transistor device. In operation, the voltage applied to the control terminal may be divided between a voltage drop between the drain and source terminal of the auxiliary HEMT (**20_1**, **20_2**) and a voltage drop between the gate and source terminal of the lateral semiconductor transistor device (**12**, **11**). The auxiliary HEMT and the voltage limiter may be monolithically integrated with the lateral semiconductor transistor device.

[0422] FIG. **52***a* illustrates a further example of a semiconductor switch **101***c*. The semiconductor switch **101***c* may comprise only one control terminal (which may be referred to as a common control terminal) to receive a control signal from a driver/controller. The semiconductor switch may further comprise an interface circuit **207**. The interface circuit **207** may be connected between the control terminal and the three transistor devices **12**, **11** and **40**. The interface circuit **207** may be configured to internally generate the first control signal and provide to the gate G**1** of the first lateral semiconductor transistor device **12**, generate the second control signal and provide to the gate G**2** of the second lateral semiconductor transistor device **11** and generate the third control signal and provide to the gate G**3** of the vertical semiconductor transistor device **40**.

[0423] FIG. **52***b* illustrates an example of the interface circuit that may be used in the semiconductor switch illustrated in FIG. **52***a* and FIG. **5**. The interface circuit may comprise additional circuits and components such as auxiliary HEMTs, level shifter, slew rate control circuit, logic circuits, voltage regulator to generate the first, second and third control signals. Additionally, the interface circuit may comprise sensing and protection circuits for both the lateral and vertical semiconductor devices and may also be configured to receive feedback from the lateral and vertical semiconductor devices. The interface circuit may be implemented on the same substrate as the lateral semiconductor switches such as a GaN chip or it may be implemented on an additional companion chip for example a silicon companion chip.

[0424] FIG. **53** illustrates an example of a half bridge circuit according to the present disclosure. The half bridge circuit comprises at least one switch operated on the low-side leg of the half bridge

and one switch operated on the high-side leg of the half bridge; wherein each of the switches comprises a first branch of two or more lateral semiconductor transistor devices Q**1**, Q**2**, Q**3**, Q**4** (e.g. GaN transistors) and a second branch comprising a high voltage vertical semiconductor transistor device S**1**, S**2** and wherein the first and second branch are in parallel. Each of the semiconductor transistor devices may comprise control terminals which are operated through a driver/controller, as described herein. The rated maximum voltage of the high voltage vertical device is significantly larger (e.g. by a factor or 1.5 or 2) than the rated maximum voltage of the lateral semiconductor transistor device. Additionally, each high voltage vertical semiconductor transistor device S**1**, S**2** (e.g. Si IGBT) may comprise a body diode between its main terminals (emitter, collector).

[0425] FIG. **54** illustrates an example of a one phase inverter according to the present disclosure. In other examples, an inverter may comprise more than one phase. Each phase of the inverter comprises at least one half bridge circuit. Each half bridge circuit may comprise a high side (e.g. a high-side leg) and a low side (e.g. a low-side leg). Each side of the half bridge circuit comprises a first branch of two or more lateral semiconductor transistor devices Q**1**, Q**2**, Q**3**, Q**4** (e.g. GaN transistors) and a second branch comprising a high voltage vertical semiconductor transistor device S**1**, S**2** and wherein the first and second branch are in parallel. Additionally, each high voltage vertical semiconductor transistor device S**1**, S**2** (e.g. Si IGBT) may comprise a body diode between its main terminals (emitter, collector). Each of the semiconductor transistor devices may comprise control terminals which are operated through a driver/controller, as described herein. Alternatively, the control terminals may be operated though an internal interface circuit as illustrated in FIG. **52***a*. The rated maximum voltage of the high voltage vertical device is significantly larger (e.g. by a factor or 1.5 or 2) than the rated maximum voltage of the lateral semiconductor transistor device. The inverter additionally comprises two DC link capacitors connected in series between the high voltage and the low voltage terminals. The mid-point of the DC link capacitors is referred to as a DC Mid point or also referred as neutral point in the literature. Each leg of the half-bridge has a DC point at the mid of the two lateral semiconductor switches denoted as point A in the high-side leg of the half-bridge and point B in the low-side leg of the half-bridge in FIG. **54**. The inverter further comprises two clamping diodes over the neutral point, that is connected between the DC mid-point and the mid point of the first branch of each leg of the half-bridge.

[0426] FIG. **55** illustrates an example of a three phase inverter according to the present disclosure. The three phase inverter comprises a first half bridge circuit comprising a first **101_1** and a second **101_2** semiconductor switch, a second half bridge circuit comprising a third **101_3** and a fourth **101_4** semiconductor switch, and a third half bridge circuit comprising a fifth **101_5** and a sixth **101_6** semiconductor switch as described herein. The DC bus voltage is split in two (or more for more than three levels) with an intermediate level (DC MID) which sits at a voltage given by the potential divider of the two capacitors in series. This DC MID voltage level is typically half of that between the DC+ and DC-voltage levels. Depending on the status (ON or OFF) of low-side and high-side legs of the half-bridge circuits and given the action of the additional clamping diodes placed as shown in FIG. **55**, the output voltage can be in steady-state at any of the three level DC voltages (DC+, DC MID, and DC−) and switching between these states when the switches are switched. The clamping diodes are connected between the series devices on each of the high-side and low-side legs to the DC MID (between the series capacitors).

[0427] It will be understood that a lateral semiconductor transistor device has terminals (e.g. source and drain terminals) on a same surface of the semiconductor. A vertical semiconductor transistor device has terminals (e.g. collector and emitter) on opposite surfaces.

[0428] Each lateral semiconductor transistor device may comprise, e.g. one or multiple III-nitride (e.g. GaN) transistors, such as discrete HEMTs, Cascode HEMTs, smart GaN HEMTs such as those described in U.S. Pat. Nos. 11,217,687 and 11,404,565B2, the contents of which are hereby incorporated by reference. The transistors (e.g. HEMTs) may comprise monolithically integrated

interface circuits, or the lateral semiconductor transistor device may comprise additional companion or interface circuits (e.g. fabricated from silicon). Preferably, where the device comprises multiple transistors, the multiple transistors have similar specifications and are arranged in parallel.

[0429] The high voltage vertical semiconductor transistor device may comprise, e.g., one or more parallel IGBTs, MOSFETs, or superjunctions. The vertical semiconductor transistor device may comprise silicon and/or silicon carbide transistors.

[0430] The maximum voltage rating refers to the maximum voltage supported between the main terminals when the device is in blocking mode. The main terminals are referred to as drain and source terminals for HEMTs, MOSFETs, and superjunctions, and emitter and collector terminals for IGBTs.

[0431] The control terminal(s) described herein correspond to gate terminals of the transistor devices.

[0432] When two branches are in parallel, a first terminal of a first branch is electrically connected to a first terminal of the second branch and a second terminal of the first branch is electrically connected to a second terminal of the second branch.

[0433] Drivers can feature multiple outputs and some outputs of the drivers can be connected to the gate terminals of devices commonly via resistors and diodes to adjust turn-on and turn-off slew rates.

[0434] All half bridges are connected between a DC+ voltage level and a DC− level and feature a mid AC output point (e.g. output terminal). Any low side leg of the half bridge is connected between DC− (or ground) and mid point. Any high side leg of the half bridge is connected between the DC+ and the mid point.

[0435] A three phase or multiple phase inverter could be provided as part of the invention.

[0436] The inverter according to the present disclosure could be viewed as a parallel combination between a two-level component of an inverter comprising high voltage switches such as IGBTs, Power MOSFETs, or superjunctions and multi-level (such as three level) component of an inverter comprising two or more series GaN lateral devices such as HEMTs or MISFETs. The mid points are outputs from the inverter and can be connected to a motor. The inverter described could be used as a traction inverter in automotive or other motor control applications. The inverter according to this aspect of the invention could be referred to as a “combo inverter”.

[0437] Different control schemes could be applied to the combo inverter. The multi-level (such as three level) component (comprising e.g. two or more series GaN lateral devices) could be active or dominant in light load conditions, when the currents are relatively small. The two-level component (comprising e.g. IGBTs, Power MOSFETs, or superjunctions) could be active or dominant in high load conditions surge conditions, when the currents are relatively high or very high. Different control schemes could be applied to the control terminal to optimize the efficiency and robustness of the combo inverter. The drive frequency could also change when driving the two-level component (preferably lower frequency) compared to the multi-level component (preferably higher frequency).

[0438] In another example according to the present disclosure, a semiconductor switch may comprise a first branch comprising a first wide bandgap semiconductor transistor device, and a second wide bandgap semiconductor transistor device, the first wide bandgap semiconductor transistor device and the second wide bandgap semiconductor transistor device being connected in series; and a second branch comprising a high voltage silicon-based semiconductor transistor device; wherein the first branch and the second branch are connected in parallel; and wherein a maximum voltage rating of the silicon semiconductor transistor device is greater than a maximum voltage rating of the first and second wide bandgap semiconductor transistor devices.

[0439] The two or more series wide bandgap semiconductor transistor devices could comprise one or more III-nitride (e.g. GaN) transistors such as discrete HEMTs, Cascode HEMTs, or smart GaN

HEMTs such as those described in U.S. Pat. Nos. 11,217,687 and 11,404,565B2, the contents of which are hereby incorporated by reference. The transistors (e.g. HEMTs) may comprise monolithically integrated interfaces, or HEMTs with additional silicon companion/interface circuits, or could comprise one or multiple silicon carbide transistors such as SiC power MOSFETs or SiC superjunctions. The multiple GaN transistors or the multiple SiC transistors could preferably have similar specifications and placed in parallel.

[0440] The high voltage silicon-based semiconductor transistor device could comprise one or multiple parallel silicon IGBTs, silicon MOSFETs, or silicon superjunctions.

[0441] A half bridge circuit may comprise at least two semiconductor switches as described herein, and an inverter may comprise at least one phase, each phase comprising at least one half bridge, as described herein in relation to other examples.

[0442] FIG. **56** illustrates an example of a multi-level inverter comprising at least one phase according to the present disclosure. Each phase comprises at least one half bridge, each half bridge comprising at least a branch of two or more series devices wherein at least one of the series devices is a wide bandgap device WBG**1**, WBG**2**, and at least one of the other series devices is a (high voltage) silicon-based semiconductor transistor device. Each of the devices may have control terminals which are operated through a driver/controller as described herein.

[0443] The wide bandgap semiconductor transistor device WBG**1**, WBG**2** could comprise one or more III-nitride (e.g. GaN) transistors such as discrete HEMTs, Cascode HEMTs, or smart GaN HEMTs such as those described in U.S. Pat. Nos. 11,217,687 and 11,404,565B2, the contents of which are hereby incorporated by reference. The transistors (e.g. HEMTs) may comprise monolithically integrated interfaces, or HEMTs with additional silicon companion/interface circuits, or could comprise one or multiple silicon carbide transistors such as SiC power MOSFETs or SiC superjunctions. The multiple GaN transistors or the multiple SiC transistors could preferably have similar specifications and placed in parallel.

[0444] The high voltage silicon-based device could be one or multiple parallel silicon IGBTs, silicon MOSFETs, or silicon superjunctions.

[0445] The devices with one terminal connected to the output voltage (i.e. the output terminal OUT) would be mostly in the on-state while the devices with one terminal connected to the DC− or DC+ buses would be switching more. Preferably, the devices with one terminal connected to the output voltage could be a silicon device. Such a device could be in the on-state for a longer period of the cycle, resulting in greater conduction loss. The devices with one terminal connected to the DC− and DC+ buses could be wide bandgap devices and could incur less conduction losses but higher switching losses.

[0446] Alternatively, when one of the devices in series is a GaN transistor then the other transistor device may be a high voltage silicon-carbide based semiconductor transistor device. In this scenario, the SiC device would be connected to the output voltage as it can be in the on-state for longer and incur lower conduction losses relative to the GaN device. The GaN devices could be connected to the DC− and DC+ buses and could incur less conduction losses but higher switching losses. However, switching losses of GaN devices would be lesser than SiC devices.

[0447] As shown in FIG. **56**, the output terminal OUT is operatively connected at a mid-point of the high-side leg and the low-side leg of the half bridge circuit, that is between a transistor device (e.g. silicon-based transistor device) on the high-side leg and a transistor device (e.g. silicon-based transistor device) on the low-side leg.

[0448] This aspect of the invention is advantageous as IGBTs (as the silicon devices) are efficient in steady-state, especially at high temperatures and high power levels, while wide bandgap devices (e.g. GaN or SiC) can switch faster and therefore have lower switching losses.

[0449] Also described herein is a multi-level inverter comprising at least one phase; each phase comprising at least one half bridge, each half bridge comprising at least a branch of two or more series devices wherein at least one of the series devices is a first wide bandgap device and at least

one of the other series devices comprises a parallel combination between a silicon device and a second wide bandgap device wherein each of the devices may have control terminals which are operated through a driver/controller. The parallel combination of the silicon device and the second wide bandgap device may be similar to the combined switch illustrated in FIG. **4** and its various implementations/variations described earlier.

[0450] FIG. **57** illustrates another example of a multi-level inverter comprising at least one phase according to the present disclosure. Each phase comprises at least one half bridge, each half bridge comprising at least a branch of two or more series devices wherein at least one of the series devices is a first wide bandgap semiconductor transistor device WBG**1**, WBG**2** and at least one of the other series devices comprises a parallel combination between a silicon-based semiconductor transistor device and a second wide bandgap semiconductor transistor device WBG**3**, WBG**4**. Each of the devices may have control terminals which are operated through a driver/controller. The parallel combination of the silicon-based semiconductor transistor device and the second wide bandgap semiconductor transistor device may be similar to any of the combined switches described and illustrated herein, such as in FIGS. **4** to **8** and their subsequent variations.

[0451] The example illustrated in FIG. **57** is similar to the example illustrated in FIG. **56**. To address the light load condition in the on-state, preferably, the devices with one terminal connected to the output voltage could comprise a combination between a silicon device and a wide bandgap device. Such devices could be in the on-state for a longer period of the cycle, resulting in greater conduction loss. At light load the wide bandgap device WBG**3**, WBG**4** will take most of the current, reducing the conduction losses while at high load (or high temperature) the silicon device could take most of the current. The devices with one terminal connected to the DC− and DC+ buses WBG**1**, WBG**2** could be wide bandgap devices and could incur less conduction losses but higher switching losses as they would be switching more.

[0452] As shown in FIG. **57**, the output terminal OUT is operatively connected at a mid-point of the high-side leg and the low-side leg of the half bridge circuit, that is between the parallel combination on the high-side leg and the parallel combination on the low-side leg.

[0453] It will be understood that combinations of the examples described and illustrated herein are possible.

[0454] In some examples, feedback control of adjusting the driving scheme of a combined switch comprising at least one GaN transistor and at least a vertical power device (IGBT or SiC power MOSFET) may be enabled. Feedback control may be provided in a similar manner to that illustrated in FIGS. **33***d* and **33***e* and described herein. A semiconductor switch may comprise a parallel combination between a high-electron-mobility transistor (HEMT) (e.g. a III-nitride HEMT) and a high voltage transistor device such as an insulated-gate bipolar transistor (IGBT), a metal-oxide-semiconductor field-effect transistor (MOSFET), or a superjunction. The semiconductor switch may comprise at least one feedback element (e.g. feedback control circuit **301_2** as illustrated in FIG. **58**) based on a current or temperature sensor incorporated alongside the HEMT and/or the high voltage transistor device, wherein the voltage levels provided to the control terminal(s) may be adjusted depending on the output from the at least one feedback element. The high voltage transistor device may be a silicon or silicon carbide device. The temperature feedback may be provided from both the IGBT and the GaN transistor to drive each differently. Examples of temperature sensor include an enhanced 2 DEG with pGaN shielding the edges.

[0455] FIG. **59** illustrates another example of the feedback control for adjusting the driving scheme of a combined switch comprising at least one GaN transistor and at least a vertical power device (IGBT or SiC power MOSFET). Here, the semiconductor switch may comprise a parallel combination between a high-electron-mobility transistor (HEMT) (e.g. a III-nitride HEMT) and a high voltage transistor device such as an insulated-gate bipolar transistor (IGBT), a metal-oxide-semiconductor field-effect transistor (MOSFET), or a superjunction. The semiconductor switch may additionally comprise an interface circuit that would provide control signals to the gates of the

HEMT and the high voltage transistor device. The semiconductor switch may comprise at least one feedback element (e.g. feedback control circuit **301_1**, **301_2** as illustrated in FIG. **59**) based on a current or temperature sensor incorporated alongside the HEMT and/or the high voltage transistor device, wherein the voltage levels provided to the control terminal(s) may be adjusted depending on the output from the at least one feedback element. The high voltage transistor device may be a silicon or silicon carbide device. The temperature feedback may be provided from both the IGBT and the GaN transistor to drive each differently. Examples of temperature sensor include an enhanced 2 DEG with pGaN shielding the edges. The feedback may be provided internal to the semiconductor switch to the interface circuit to adjust the driving signals and/or the feedback may be provided externally to the driver/controller to adjust the control signal from the driver/controller.

[0456] In any of the examples described herein, current or junction temperature feedback from the wide bandgap device (e.g. a GaN transistor or a SiC transistor) and/or the silicon-based device (e.g. IGBT) could be used by a controller or driver or the interface circuit to modify the driving schemes of the switch.

[0457] The temperature sensor for a GaN device (lateral device), could comprise a resistive temperature detector (RTD) in some examples (see FIG. **60**, Sensor1). A RTD is a device that modifies its resistance with the temperature in a known manner. By monitoring the resistance, the temperature could be monitored. The RTD could comprise a 2 DEG resistor, a 2 DEG resistor with edges covered by p-GaN, to give better uniformity, metal resistor or a HEMT used in a resistive mode. Sensing bridges or differential schemes as known in state-of-the art of such RTDs could be used to increase the sensitivity and accuracy of temperature reading. Alternatively, the temperature could be monitored by monitoring the voltage drop on a diode incorporated in GaN or its leakage during reverse blocking. The GaN diode could be made using a similar structure to the pGaN gate diode, or could be done by using Schottky metallization.

[0458] The temperature sensor for the vertical device (e.g. SiC MOSFET or IGBT), could be in the form of a polysilicon diode (see FIG. **60**, Sensor2). The voltage drop on a polysilicon diode at a constant current decreases with temperature linearly. This could be used to monitor the temperature. The diode could be the sensing element in a VPTAT or IPTAT circuit (the rest of the circuit could be external) or could be used as part of differential measurement or in a bridge configuration.

[0459] The feedback in the form of current or junction temperatures could be used to adjust the driving scheme for the combinational switch.

[0460] For example, if either of the GaN lateral device or the IGBT hit a certain temperature level, the devices could be switched off made inactive, or the other device could be actively operated. Continuous adjustment of the driving scheme could be performed as a function of the current/temperature information from the vertical and the lateral device to (i) increase efficiency or (ii) enhance reliability.

[0461] Further examples according to the present disclosure are described in the following non-limiting clauses: [0462] 1. A semiconductor switch comprising a first main terminal, a second main terminal, and a control terminal, the semiconductor switch comprising: [0463] a III-nitride integrated circuit, the III-nitride integrated circuit comprising: [0464] a high voltage HEMT, the high voltage HEMT comprising a high voltage HEMT source terminal, a high voltage HEMT drain terminal, and a high voltage HEMT gate terminal; and [0465] at least part of an interface circuit; [0466] wherein the semiconductor switch further comprises a high voltage transistor device, the high voltage transistor device comprising a transistor device first terminal, a transistor device second terminal, and a transistor device gate terminal; [0467] wherein the high voltage HEMT source terminal and the transistor device first terminal are operatively connected to the first main terminal; [0468] wherein the high voltage HEMT drain terminal and the transistor device second terminal are operatively connected to the second main terminal; and [0469] wherein the high voltage HEMT gate terminal is operatively connected to the control terminal via the interface

circuit, wherein the interface circuit is configurable to adjust a voltage applied to the control terminal to be operatively compatible with the high voltage HEMT gate terminal. [0470] 2. A semiconductor switch according to clause 1, wherein the interface circuit is partly disposed on a silicon circuit separate from the III-nitride integrated circuit. [0471] 3. A semiconductor switch according to clause 1 or clause 2, wherein the interface circuit comprises: [0472] a low voltage auxiliary HEMT, the low voltage auxiliary HEMT comprising an auxiliary HEMT source terminal, an auxiliary HEMT drain terminal, and an auxiliary HEMT gate terminal; and [0473] a voltage limiter operatively connected to the auxiliary HEMT gate terminal; [0474] wherein the auxiliary HEMT source terminal is operatively connected to the high voltage HEMT gate terminal; [0475] wherein the auxiliary HEMT drain terminal is operatively connected to the control terminal; and [0476] wherein the voltage limiter is operatively connected to the high voltage HEMT source terminal and to the auxiliary HEMT gate terminal, further wherein the voltage limiter is configurable to limit a voltage across the high voltage HEMT gate terminal and the high voltage HEMT source terminal. [0477] 4. A semiconductor switch according to any one of the preceding clauses, wherein the transistor device gate terminal is operatively connected to the control terminal, and/or wherein the transistor device gate terminal is connected to the control terminal via the interface circuit. [0478] 5. A semiconductor switch according to any one of the preceding clauses, wherein the auxiliary HEMT drain terminal is operatively connected to the control terminal via a first resistance, and wherein the transistor device gate terminal is operatively connected to the control terminal via a second resistance. [0479] 6. A semiconductor switch according to any one of the preceding clauses, wherein: [0480] the high voltage transistor device comprises a silicon and/or silicon carbide transistor; and/or [0481] wherein the high voltage transistor device comprises an insulated-gate bipolar transistor (IGBT), and wherein the transistor device first terminal is an IGBT emitter terminal and the transistor device second terminal is an IGBT collector terminal; and/or [0482] wherein the high voltage transistor device comprises a metal-oxide-semiconductor field-effect transistor (MOSFET), and wherein the transistor device first terminal is a MOSFET source terminal and the transistor device second terminal is a MOSFET drain terminal; and/or [0483] wherein the high voltage transistor device comprises a superjunction, and wherein the transistor device first terminal is a superjunction source terminal and the transistor device second terminal is a superjunction drain terminal. [0484] 7. A semiconductor switch according to any one of the preceding clauses, wherein the high voltage HEMT source terminal, the high voltage HEMT drain terminal, and the high voltage HEMT gate terminal are laterally spaced from one another; and [0485] wherein the transistor device first terminal and the transistor device second terminal are vertically spaced from one another. [0486] 8. A semiconductor switch according to any one of the preceding clauses, wherein the high voltage HEMT is disposed on a first semiconductor substrate, and wherein the high voltage transistor device is disposed on a second semiconductor substrate, different from the first semiconductor substrate; and/or [0487] wherein the high voltage HEMT and the low voltage auxiliary HEMT are disposed on a same semiconductor substrate. [0488] 9. A semiconductor switch according to any one of the preceding clauses, wherein: [0489] the semiconductor switch is configured to turn-on or be in an on-state when the control terminal is driven with a peak voltage of 10 V or more; and [0490] wherein the semiconductor switch is configured to turn-off or be in an off-state when the control terminal is driven with a minimum voltage of 0 V or negative, or with a voltage of less than a lower of: [0491] a threshold voltage of the high voltage HEMT; and [0492] a threshold voltage of the high voltage transistor device. [0493] 10. A semiconductor switch according to any one of the preceding clauses, wherein the semiconductor switch comprises multiple high voltage HEMTs in parallel with one or more high voltage transistor devices; or multiple III-nitride integrated circuits in parallel with one or more high voltage transistor devices. [0494] 11. A semiconductor switch according to any one of the preceding clauses, wherein the semiconductor switch comprises a series combination of two or more III-nitride high voltage HEMTs in parallel with one or more high voltage transistor devices;

or a series combination of two or more III-nitride integrated circuits connected in parallel with one or more high voltage transistor devices. [0495] 12. A semiconductor switch comprising a first main terminal, a second main terminal, and a control terminal, the semiconductor switch comprising: [0496] a Cascode device, the Cascode device comprising: [0497] a MOSFET comprising a MOSFET drain terminal, a MOSFET gate terminal and a MOSFET source terminal; [0498] a high voltage depletion mode III-nitride HEMT comprising a depletion HEMT drain terminal, a depletion HEMT gate terminal and a depletion HEMT source terminal; [0499] wherein the MOSFET drain terminal is operatively connected to the depletion HEMT source terminal; [0500] wherein the semiconductor switch further comprises a high voltage transistor device comprising a transistor device first terminal, a transistor device second terminal, and a transistor device gate terminal; [0501] wherein the MOSFET source terminal and the transistor device first terminal are operatively connected to the first main terminal; [0502] wherein the depletion HEMT drain terminal and the transistor device second terminal are operatively connected to the second main terminal; [0503] wherein the MOSFET gate terminal is operatively connected to the control terminal. [0504] 13. A semiconductor switch according to clause 12, wherein the high voltage transistor device comprises an IGBT, a silicon carbide MOSFET or a superjunction; and the MOSFET comprises an n-channel MOSFET in vertical or quasi-vertical configuration. [0505] 14. A semiconductor switch according to clause 12 or clause 13, wherein the depletion HEMT gate terminal is operatively connected to the MOSFET source terminal and the first main terminal; and [0506] wherein the transistor device gate terminal and the MOSFET gate terminal are operatively connected to the control terminal. [0507] 15. A semiconductor switch according to any one of clauses 12 to 14, wherein the high voltage transistor device is a bipolar junction transistor, and wherein the depletion HEMT gate terminal is operatively connected to the MOSFET source terminal and the first main terminal; and wherein the transistor device gate terminal is operatively connected to the MOSFET drain terminal and the depletion HEMT source terminal, and wherein the MOSFET gate terminal is operatively connected to the control terminal. [0508] 16. A semiconductor switch according to any one of clauses 12 to 15, wherein the high voltage transistor device is a bipolar junction transistor, and wherein the transistor device gate terminal is operatively connected to the MOSFET drain terminal and the depletion HEMT source terminal, and wherein the MOSFET gate terminal is operatively connected to the control terminal, and wherein the depletion HEMT gate terminal is operatively connected to the control terminal via an interface circuit, and wherein the interface circuit is configured to adjust a voltage applied to the control terminal to be operatively compatible with the depletion HEMT gate terminal. [0509] 17. A semiconductor switch according to any one of clauses 12 to 16, wherein the MOSFET gate terminal is operatively connected to the control terminal through a slew-rate control circuit. [0510] 18. A semiconductor switch according to any one of clauses 1 to 11, wherein the high voltage HEMT source terminal and the transistor device first terminal are electrically connected to the first main terminal via a first passive component; and/or [0511] wherein the high voltage HEMT drain terminal and the transistor device second terminal are electrically connected to the second main terminal via a second passive component. [0512] 19. A semiconductor switch according to any one of clauses 1 to 11, wherein the high voltage HEMT source terminal is operatively connected to the first main terminal via a first inductive component, the first inductive component being operable to produce a first temporal lag between the first main terminal and the high voltage HEMT source terminal; and [0513] wherein the transistor device first terminal is operatively connected to the first main terminal via a second inductive component, the second inductive component being operable to produce a second temporal lag between the first main terminal and the transistor device first terminal. [0514] 20. A semiconductor switch according to any one of clauses 1 to 11, wherein the III-nitride integrated circuit and the high voltage transistor device are disposed in a singular package. [0515] 21. A semiconductor switch comprising a first main terminal, a second main terminal, and a control terminal, the semiconductor switch comprising: [0516] at least one high voltage HEMT, the high voltage HEMT comprising a high

voltage HEMT source terminal, a high voltage HEMT drain terminal, and a high voltage HEMT gate terminal; and [0517] at least one high voltage transistor device, the high voltage transistor device comprising a transistor device first terminal, a transistor device second terminal, and a transistor device gate terminal; [0518] wherein the high voltage HEMT source terminal and the transistor device first terminal are operatively connected to the first main terminal; [0519] wherein the high voltage HEMT drain terminal and the transistor device second terminal are operatively connected to the second main terminal; and [0520] wherein the high voltage HEMT gate terminal is operatively connected to the control terminal; [0521] wherein the control terminal is operatively connected to a first driver output of a driver, and wherein the transistor device gate terminal is operatively connected to a second driver output of a driver; and [0522] wherein the control terminal is configured to be driven, by the driver via the first driver output, within a first driving voltage range; and [0523] wherein the transistor device gate terminal is configured to be driven, by the driver via the second driver output, within a second driving voltage range. [0524] 22. A semiconductor switch according to clause 21, wherein voltage levels within at least one of the first driving voltage range and the second driving voltage range are configured to vary selectably in time, corresponding to the semiconductor switch being selectably in an on-state mode, an off-state mode, a turn-on mode, or a turn-off mode. [0525] 23 A semiconductor switch according to clause 21 or clause 22, wherein a slew rate at the control terminal and/or the transistor device gate terminal are configured to vary selectably, corresponding to the semiconductor switch being selectably in the turn-on mode or the turn-off mode. [0526] 24 A semiconductor switch according to any one of clauses 21 to 23, wherein the control terminal is operatively connected to the first driver output via a first resistor, or via a first resistor in series with a first diode. [0527] 25. A semiconductor switch according to any one of clauses 21 to 24, wherein the transistor device gate terminal is operatively connected to the second driver output via a second resistor, or via a second resistor in series with a second diode. [0528] 26. A semiconductor switch according to any one of clauses 21 to 24, further comprising an interface circuit, wherein the high voltage HEMT gate terminal is operatively connected to the control terminal via the interface circuit, wherein the interface circuit is configurable to adjust voltage levels within the first driving voltage range to be operatively compatible with the high voltage HEMT gate terminal. [0529] 27. A semiconductor switch according to clause 26 as dependent on clause 22, wherein the interface circuit comprises a feedback circuit, the feedback circuit comprising at least one output operatively connected to a driver feedback input; and [0530] wherein the feedback circuit is configured to provide a feedback signal to the driver feedback input, the feedback signal corresponding to a sensed current, a sensed voltage, and/or a sensed temperature in the semiconductor switch. [0531] 28 A semiconductor switch according to clause 26 as dependent on clause 23, wherein the interface circuit comprises a feedback circuit, the feedback circuit comprising at least one output operatively connected to a driver feedback input; and [0532] wherein the feedback circuit is configured to provide a feedback signal to the driver feedback input, the feedback signal corresponding to sensed driving slew rates at the control terminal and/or the transistor device gate terminal. [0533] 29 A semiconductor switch according to any one of clauses 26 to 28, wherein the interface circuit is monolithically integrated with the high voltage HEMT. [0534] 30. A semiconductor switch according to any one of clauses 21 to 29, wherein the high voltage HEMT is a lateral III-nitride HEMT, optionally a GaN HEMT; and [0535] wherein the high voltage transistor device is any of: [0536] a vertical IGBT comprising silicon, [0537] a vertical power MOSFET comprising silicon, silicon carbide, and/or any other wide bandgap material, or [0538] a vertical superjunction device comprising silicon, silicon carbide, and/or any other wide bandgap material. [0539] 31. A semiconductor switch according to clause 26, wherein the interface circuit comprises: [0540] a low voltage auxiliary HEMT, the low voltage auxiliary HEMT comprising an auxiliary HEMT source terminal, an auxiliary HEMT drain terminal, and an auxiliary HEMT gate terminal; and [0541] a voltage limiter operatively connected to the auxiliary HEMT gate terminal; [0542] wherein the auxiliary HEMT source terminal is

operatively connected to the high voltage HEMT gate terminal; [0543] wherein the auxiliary HEMT drain terminal is operatively connected to the control terminal; and [0544] wherein the voltage limiter is operatively connected to the high voltage HEMT source terminal and to the auxiliary HEMT gate terminal, further wherein the voltage limiter is configurable to limit a voltage across the high voltage HEMT gate terminal and the high voltage HEMT source terminal. [0545] 32. A semiconductor switch according to any one of clauses 21 to 31, wherein the interface circuit comprises a Miller clamp transistor, the Miller clamp transistor comprising a plurality of Miller clamp gates, wherein the interface circuit is configured such that an on-state resistance of the Miller clamp transistor depends on which Miller clamp gate(s) of the plurality of Miller clamp gates is active. [0546] 33. A semiconductor switch according to any one of clauses 21 to 32, wherein the interface circuit comprises a plurality of Miller clamp transistors having different on-state resistances. [0547] 34. A semiconductor switch according to clause 33, wherein the interface circuit further comprises a logic circuit configured to control activation of each Miller clamp transistor of the plurality of Miller clamp transistors. [0548] 35. A semiconductor switch according to clause 26, wherein the transistor device gate terminal is operatively connected to the second driver output via the interface circuit. [0549] 36. A semiconductor switch according to any one of clauses 21 to 35, wherein the control terminal is further operatively connected to a third driver output of the driver, wherein: [0550] when the semiconductor switch is in the turn-off mode, the control terminal is configured to selectably receive either: [0551] a regular turn-off signal comprising a first driving voltage level within the first driving voltage range, from the driver via the first driver output; or [0552] a delayed turn-off signal, or a slower turn-off signal, comprising a third driving voltage level within the first driving voltage range, from the driver via the third driver output. [0553] 37. A semiconductor switch according to any one of clauses 21 to 36, wherein the transistor device gate terminal is operatively connected to a fourth driver output of the driver, wherein: [0554] when the semiconductor switch is in the turn-off mode, the transistor device gate terminal is configured to selectably receive either: [0555] a regular turn-off signal comprising a second driving voltage level within the second driving voltage range, from the driver via the second driver output; or [0556] a delayed turn-off signal, or a slower turn-off signal, comprising a fourth driving voltage level within the second driving voltage range, from the driver via the fourth driver output. [0557] 38. A semiconductor switch according to clauses 24 and 36, wherein the control terminal is operatively connected to the third driver output via a third resistor, wherein a resistance of the third resistor is greater than a resistance of the first resistor. [0558] 39. A semiconductor switch according to clauses 25 and 37, wherein the transistor device gate terminal is operatively connected to the fourth driver output via a fourth resistor, wherein a resistance of the fourth resistor is greater than a resistance of the second resistor. [0559] 40. A semiconductor switch according to clause 36, comprising a first Miller clamp transistor and a second Miller clamp transistor, the first Miller clamp transistor and the second Miller clamp transistor being operatively connected to the High voltage HEMT gate terminal, the second Miller clamp transistor having a higher on-state resistance than the first Miller clamp transistor; [0560] wherein the regular turn-off signal is configured to activate the first Miller clamp transistor; [0561] and wherein the delayed turn-off signal, or the slower turn-off signal, is configured to activate the second Miller clamp transistor. [0562] 41. A semiconductor switch according to clause 26, wherein the interface circuit comprises a third Miller clamp transistor, the third Miller clamp transistor comprising a third Miller clamp drain terminal, wherein the third Miller clamp drain terminal is operatively connected to the high voltage HEMT gate terminal. [0563] 42. A semiconductor switch according to clause 41, wherein the interface circuit further comprises a fourth Miller clamp transistor, the fourth Miller clamp transistor comprising a fourth Miller clamp drain terminal, wherein the fourth Miller clamp drain terminal is operatively connected to the transistor device gate terminal. [0564] 43 A semiconductor switch according to any one of the preceding clauses, comprising at least one diode arranged in parallel with the high voltage HEMT and the high voltage transistor device. [0565] 44. A method of

operating a semiconductor switch, the semiconductor switch comprising a first main terminal, a second main terminal, and a control terminal, the semiconductor switch comprising: [0566] a high voltage HEMT, the high voltage HEMT comprising a high voltage HEMT source terminal, a high voltage HEMT drain terminal, and a high voltage HEMT gate terminal; and [0567] a high voltage transistor device, the high voltage transistor device comprising a transistor device first terminal, a transistor device second terminal, and a transistor device gate terminal; [0568] wherein the high voltage HEMT source terminal and the transistor device first terminal are operatively connected to the first main terminal; and [0569] wherein the high voltage HEMT drain terminal and the transistor device second terminal are operatively connected to the second main terminal; [0570] wherein the method comprises: [0571] driving the control terminal, by a driver via a first driver output, within a first driving voltage range; and [0572] driving the transistor device gate terminal, by a driver via a second driver output, within a second driving voltage range. [0573] 45. A system comprising: [0574] a semiconductor switch comprising a first main terminal, a second main terminal, and a control terminal, the semiconductor switch comprising: [0575] a high voltage HEMT, the high voltage HEMT comprising a high voltage HEMT source terminal, a high voltage HEMT drain terminal, and a high voltage HEMT gate terminal; and [0576] a high voltage transistor device, the high voltage transistor device comprising a transistor device first terminal, a transistor device second terminal, and a transistor device gate terminal; [0577] wherein the high voltage HEMT source terminal and the transistor device first terminal are operatively connected to the first main terminal; [0578] wherein the high voltage HEMT drain terminal and the transistor device second terminal are operatively connected to the second main terminal; and [0579] wherein the high voltage HEMT gate terminal is operatively connected to the control terminal; [0580] the system further comprising a driver, the driver comprising a first driver output and a second driver output; [0581] wherein the control terminal is operatively connected to the first driver output, and wherein the transistor device gate terminal is operatively connected to the second driver output; and [0582] wherein the driver is configured to drive the controller, via the first driver output, within a first driving voltage range; and [0583] wherein driver is further configured to drive the transistor device gate terminal, via the second driver output, within a second driving voltage range. [0584] 46. A semiconductor switch comprising a HEMT, the HEMT comprising a gate terminal, the gate terminal being operatively connected to a first driver output of a driver and to a second driver output of the driver; wherein: [0585] when the semiconductor switch is in a turn-off mode, the gate terminal is configured to selectably receive either: [0586] a regular turn-off signal from the first driver output; or [0587] a delayed turn-off signal, or a slower turn-off signal, from the second driver output.

[0588] It will be appreciated that terms such as “top” and “bottom”, “above” and “below”, “lateral” and “vertical”, and “under” and “over”, “front” and “behind”, “underlying”, etc. may be used in this specification by convention and that no particular physical orientation of the device as a whole is implied.

[0589] It will be further appreciated that specific examples described herein may be equivalently applicable to any suitable type of high voltage transistor device, for example IGBTs, MOSFETs (e.g. high voltage Si or SiC MOSFETs), and/or superjunctions.

[0590] Although the disclosure has been described in terms of preferred embodiments as set forth above, it should be understood that these embodiments are illustrative only and that the claims are not limited to those embodiments. Those skilled in the art will be able to make modifications and alternatives in view of the disclosure, which are contemplated as falling within the scope of the appended claims. Each feature disclosed or illustrated in the present specification may be incorporated in the disclosure, whether alone or in any appropriate combination with any other feature disclosed or illustrated herein.

Claims

1. A semiconductor switch comprising: a first branch comprising a first lateral semiconductor transistor device configured to be driven by a first control signal, and a second lateral semiconductor transistor device configured to be driven by a second control signal, the first lateral semiconductor transistor device and the second lateral semiconductor transistor device being connected in series; and a second branch comprising a vertical semiconductor transistor device configured to be driven by a third control signal; wherein the first branch and the second branch are connected in parallel; and wherein a maximum voltage rating of the vertical semiconductor transistor device is greater than a maximum voltage rating of the first and second lateral semiconductor transistor devices.

2. The semiconductor switch according to claim 1, comprising: a first control terminal configured to receive the first control signal; a second control terminal configured to receive the second control signal; and an interface circuit connected between at least one of: the first control terminal and the first lateral semiconductor transistor device; and the second control terminal and the second lateral semiconductor transistor device.

3. The semiconductor switch according to claim 1, comprising: a common control terminal configured to receive a common control signal; and an interface circuit connected between at least one of: the common control terminal and the first lateral semiconductor transistor device; the common control terminal and the second lateral semiconductor transistor device; and the common control terminal and the vertical semiconductor transistor device; wherein the interface circuit is configured to generate at least one of the first control signal, the second control signal, and the third control signal.

4. The semiconductor switch according to claim 1, wherein at least one of the first and second lateral semiconductor transistor devices comprises one or more III-nitride transistors, one or more HEMTs, and/or one or more III-nitride HEMTs; and wherein the vertical semiconductor transistor device comprises one or more silicon or silicon carbide-based IGBTs, MOSFETs, and/or superjunctions.

5. An apparatus comprising: the semiconductor switch according to claim 1; and at least one driver operatively connected to at least one of the first lateral semiconductor transistor device, the second lateral semiconductor transistor device, and the vertical semiconductor transistor device; wherein the at least one driver is configured to output at least one of the first control signal, the second control signal, and the third control signal.

6. A semiconductor switch comprising: a first branch comprising a first wide bandgap semiconductor transistor device configured to be driven by a first control signal, and a second wide bandgap semiconductor transistor device configured to be driven by a second control signal, the first wide bandgap semiconductor transistor device and the second wide bandgap semiconductor transistor device being connected in series; and a second branch comprising a silicon-based semiconductor transistor device configured to be driven by a third control signal; wherein the first branch and the second branch are connected in parallel; and wherein a maximum voltage rating of the silicon semiconductor transistor device is greater than a maximum voltage rating of the first and second wide bandgap semiconductor transistor devices.

7. The semiconductor switch according to claim 6, comprising: a first control terminal configured to receive the first control signal; a second control terminal configured to receive the second control signal; and an interface circuit connected between at least one of: the first control terminal and the first wide bandgap semiconductor transistor device; and the second control terminal and the second wide bandgap semiconductor transistor device.

8. The semiconductor switch according to claim 6, comprising: a common control terminal configured to receive a common control signal; and an interface circuit connected between at least

one of: the common control terminal and the first wide bandgap semiconductor transistor device; the common control terminal and the second wide bandgap semiconductor transistor device; and the common control terminal and the silicon-based semiconductor transistor device; wherein the interface circuit is configured to generate at least one of the first control signal, the second control signal, and the third control signal.

9. The semiconductor switch according to claim 6, wherein at least one of the first and second wide bandgap semiconductor transistor devices comprises one or more III-nitride transistors, and/or one or more silicon carbide transistors; and wherein the silicon-based semiconductor transistor device comprises one or more IGBTs, one or MOSFETs, and/or one or more superjunctions.

10. A half bridge circuit comprising a low-side leg and a high-side leg, each of the low-side leg and the high-side leg comprising a semiconductor switch according to claim 1.

11. An inverter comprising at least one phase, each phase comprising at least one half bridge circuit according to claim 10.

12. A half bridge circuit comprising a low-side leg and a high-side leg, each of the low-side leg and the high-side leg comprising a semiconductor switch according to claim 6.

13. An inverter comprising at least one phase, each phase comprising at least one half bridge circuit according to claim 12.

14. An apparatus comprising: the semiconductor switch according to claim 6; and at least one driver operatively connected to at least one of the first wide bandgap semiconductor transistor device, the second wide bandgap semiconductor transistor device, and the silicon-based semiconductor transistor device; wherein the at least one driver is configured to output at least one of the first control signal, the second control signal, and the third control signal.

15. A multi-level inverter comprising at least one phase, each phase comprising at least one half bridge circuit comprising a high-side and a low-side, wherein each side of each half bridge circuit comprises: a first wide bandgap semiconductor transistor device; and a silicon-based semiconductor transistor device; wherein the wide bandgap semiconductor transistor device and the silicon-based semiconductor transistor device are connected in series.

16. The multi-level inverter according to claim 15, wherein the first wide bandgap semiconductor transistor device comprises one or more III-nitride transistors, and/or one or more silicon carbide transistors; and wherein the silicon-based semiconductor transistor device comprises one or more IGBTs, one or MOSFETs, and/or one or more superjunctions.

17. The multi-level inverter according to claim 15, wherein each phase comprises an output terminal connected at a mid-point of the high-side and the low-side of the half bridge circuit, wherein the silicon-based semiconductor transistor device is connected between the first wide bandgap semiconductor transistor device and the output terminal.

18. The multi-level inverter according to claim 15, wherein each side of each half bridge circuit further comprises: a second wide bandgap semiconductor transistor device connected in parallel with the silicon-based semiconductor transistor device.

19. The inverter according to claim 11, wherein: the first branch of the low-side leg and the first branch of the high-side leg form a first multi-level component; and the second branch of the low-side leg and the second branch of the high-side leg form a second multi-level component; wherein the first multi-level component is configured to be dominant when a current through the inverter is below a threshold level; and wherein the second multi-level component is configured to be dominant when the current through the inverter is above the threshold level.

20. The inverter according to claim 13, wherein: the first branch of the low-side leg and the first branch of the high-side leg form a first multi-level component; and the second branch of the low-side leg and the second branch of the high-side leg form a second multi-level component; wherein the first multi-level component is configured to be dominant when a current through the inverter is below a threshold level; and wherein the second multi-level component is configured to be dominant when the current through the inverter is above the threshold level.