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United States Patent	12395206
Kind Code	B2
Date of Patent	August 19, 2025
Inventor(s)	Bluestone; Aaron James

Parasitic tolerant charge-based coupling measurement

Abstract

A system for measuring parasitic capacitance coupling between adjacent first communication transmission line and second communication transmission line is disclosed. The system including: a parasitic tolerant capacitive based coupling measurement circuit (CBCM), the CBCM including: a capacitive auto-zeroing buffer configured to bias the second communication transmission line and displace coupling charge transferred from the first communication transmission line to a switched capacitor storage element; a capacitive trans-impedance amplifier configured to integrate displaced coupling charge onto an output voltage node; and a comparator configured to switch states once the capacitive trans-impedance amplifier integration has surpassed a reference trippoint.

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Appl. No.:	**18/483344**
Filed:	**October 09, 2023**

Prior Publication Data

Document Identifier	Publication Date
US 20250119178 A1	Apr. 10, 2025

Publication Classification

Int. Cl.: **H04B3/487** (20150101)

U.S. Cl.:

CPC **H04B3/487** (20150115);

Field of Classification Search

CPC: H04B (3/02); H04B (3/46); H04B (3/487); H04B (3/493); H04B (3/32); H04B (3/34)

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Background/Summary

FIELD

(1) This application is directed to systems and method for parasitic tolerant charge-based coupling

measurements.

BACKGROUND

(2) Mutual coupling/cross talk measurements are usually done with expensive test equipment that requires disconnecting signal wires from a system transmitter and receiver and connecting them to test equipment instead, and then reconnecting them back into the system. This approach tends to have many disadvantages including being both inefficient and time consuming.

(3) A major source of crosstalk in high-speed data links comes from the coupling capacitance between parallel interconnect elements. The charge-based capacitance measurement (CBCM) provides a method to precisely characterize the coupling capacitance, and consequently estimate high frequency isolation performance. Conventional CBCM architectures are sensitive to parasitic coupling to ground/power supplies, ultimately limiting measurement resolution for long interconnects with substantial ground shielding.

(4) Accordingly, an improved approach to measure capacitive-coupling between various nodes/wires/interconnect is needed.

SUMMARY

(5) According to examples of the present disclosure, a system for measuring parasitic capacitance coupling between adjacent first communication transmission line and second communication transmission line is disclosed. The system comprises a parasitic tolerant capacitive based coupling measurement circuit (CBCM), the CBCM comprising: a capacitive buffer configured to bias the second communication transmission line and displace coupling charge transferred from the first communication transmission line to a switched capacitor storage element; a capacitive trans-impedance amplifier configured to integrate displaced coupling charge onto an output voltage node; and a comparator configured to switch states once the capacitive trans-impedance amplifier integration has surpassed a reference trippoint.

(6) According to examples of the present disclosure, the system can include one or more of the following features. The system can further comprises a digital signal generator that provides a digital periodic signal to a receive end of the first communication transmission line. The digital periodic signal in the first communication transmission line induces a charge to flow in the second communication transmission line. The second communication transmission line maintains a constant bias and no charge from parasitic capacitances is transferred to the capacitive trans-impedance amplifier. The first communication transmission line is an aggressor line. The second communication transmission line is a victim line. The first communication transmission line and the second communication transmission line are high-speed analog communications channels. The first communication transmission line and the second communication transmission line are digital communications channels. The digital communications channels comprise ASICs or FPGAs. The system can further comprise a processor configured to receive an output from the voltage comparator and determine the capacitive-based coupling measurement. The voltage comparator is a dynamic, clocked voltage comparator.

(7) According to example of the present disclosure, a method to determine a coupling capacitance between a first communication line and a second communication line is disclosed. The method comprises providing a periodic digital signal to a first communication transmission line that induces a charge to flow in a nearby second communication transmission line, wherein the charge flows through a capacitive auto-zeroing buffer; integrating the charge onto a feedback capacitor of a capacitive trans-impedance amplifier when the charge is positive due to a positive change in voltage of the periodic digital signal on the first communication transmission line; disconnecting the capacitive trans-impedance amplifier from a signal path prior to a negative charge flow due to a negative change in voltage in the signal in the first communication transmission line; integrating in one direction until integrated charge formulates a voltage which crosses a known threshold as measured on a voltage comparator circuit; and counting a number of cycles required to cross the known threshold to infer a coupling capacitance between the first communication transmission line

and the second communication transmission line.

(8) According to examples of the present disclosure, the method can include one or more of the following features. Prior to the providing the periodic digital signal, the method comprises resetting a capacitive buffer capacitor of a capacitive auto-zeroing buffer by closing and reopening a switch in parallel with the capacitive buffer capacitor at a first time and resetting the feedback capacitor of the capacitive trans-impedance amplifier by closing and reopening a switch in parallel with the feedback capacitor at a second time. The second communication transmission line maintains a constant bias and no charge from parasitic capacitances is transferred to the capacitive trans-impedance amplifier. The first communication transmission line is an aggressor line. The second communication transmission line is a victim line. The first communication transmission line and the second communication transmission line are high-speed analog communications channels. The first communication transmission line and the second communication transmission line are digital communications channels. The digital communications channels comprise ASICs or FPGAs. The method further comprises receiving, at a processor, an output from the voltage comparator circuit and determining a capacitive-based coupling.

Description

BRIEF DESCRIPTION OF THE FIGURES
(1) The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate embodiments of the present teachings and together with the description, serve to explain the principles of the disclosure.
(2) FIG. **1** shows a simplified conventional overview.
(3) FIG. **2** shows another simplified conventional overview configuration.
(4) FIG. **3** shows a block diagram circuit configuration according to examples of the present disclosure.
(5) FIG. **4** shows an example of FIG. **3** including a parasitic tolerant CBCM with auto-zeroing capacitive buffer according to examples of the present disclosure.
(6) FIG. **5** shows a timing diagram for the configuration of FIG. **4**.
(7) FIG. **6**A and FIG. **6**B show a zoomed-out view of the timing diagram of FIG. **5**.
(8) FIG. **7**A and FIG. **7**B show simulation results for the configuration of FIG. **4**.
(9) FIG. **8** show a flowchart for a method according to examples of the present disclosure.
(10) FIG. **9** shows a computing system according to examples of the present disclosure.
DETAILED DESCRIPTION
(11) Reference will now be made in detail to the present embodiments, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.
(12) Generally speaking, examples according to the present disclose provides for a system or device, such as an integrated circuit (IC), that is configured to measure capacitive coupling between various nodes/wires/interconnect. Additionally, examples according to the present disclose provides for a method for measuring capacitive coupling between various nodes/wires/interconnect using a system or device, such as an IC. Conventional charge-based capacitance measurement (CBCM) architectures are sensitive to parasitic coupling to ground/power supplies, ultimately limiting measurement resolution for long interconnects with substantial ground shielding. In some examples, the present capacitive buffer circuit, combined with auto-zero sequencing, mitigates the aforementioned non-ideality and maintains coupling measurement resolution with parasitic capacitance >100,000× larger than coupling capacitance under test. Examples of the present disclosure allows on-chip capacitive coupling measurements with resolution better than 10 attofarads on circuit nodes with parasitic capacitances greater than 1 nanofarad and allows

characterization of long interconnect (e.g. PCB traces) with capacitive coupling to nearby traces while providing the ability to maintain measurement resolution/accuracy while larger parasitic capacitance are present.

(13) A major source of crosstalk in high-speed data links comes from the coupling capacitance between parallel interconnect elements. Examples of the present disclosure provides for a CBCM that provides a method to precisely characterize the coupling capacitance, and consequently estimate high frequency isolation performance. Examples of the present disclosure exploits the principle $\Delta Q = C\Delta V$ by applying a voltage step on an Aggressor line, and measuring the corresponding change of charge on a Victim line—as required to maintain a constant voltage Vbias. The measurement resolution on C.sub.DUT is significantly improved by repeating the voltage step numerous times and integrating the charge in one direction through a capacitive trans-impedance amplifier (CTIA). A comparator is used to count how many steps are required to integrate above a known trip-point.

(14) Since this measurement is near-DC (no high-frequency content/high-throughput processing), many baseband techniques can be utilized to isolate non-idealities and enhance measurement performance: Digital Correlated Double Sampling, calibration of charge injection, and ramp-up/ramp-down averaging.

(15) In addition to the coupling capacitance, C.sub.DUT, the interconnect elements may exhibit a large parasitic capacitance to the ground plane, C.sub.Para, often many orders of magnitude greater than the coupling capacitance (nanofarads vs. hundreds of attofarads). This is uncommon to typical CBCM implementations and preliminary simulations showed this would corrupt the resolution of the measurement. As the victim line is switched between two versions of V.sub.bias, the parasitic capacitance must charge and discharge small amounts for non-ideal mismatches between the signal paths. For long interconnect DUTs, this delta charge can be orders of magnitude larger than the signal of interest. The capacitive buffer shown in FIG. **4** overcomes the sensitivity to ground plane parasitics. The victim line containing the large parasitic is held a constant voltage, removing the undesired charge and discharge. Furthermore, auto-zeroing operation reduces amplifier non-idealities including systematic voltage offset and flicker noise.

(16) FIG. **1** shows a simplified conventional overview **100**. As shown in FIG. **1**, an aggressor signal **102**, denoted by φ.sub.aggr, is provided to receive end **106** of aggressor line **108**. An example aggressor signal **102** is shown in in FIG. **5** in **508**. Aggressor line **108** is near victim line **110** in a parallel arrangement. Coupling capacitance **112**, denoted by C.sub.DUT, between aggressor line **108** and victim line **110** is measured by using a switched parallel current measurement architecture at transmit end **114** of victim line **110** that includes switch 1 **116**, closed in φ.sub.1, switch 2 **118**, closed in φ.sub.2, and amp meter **120**, and voltage bias, denoted by V.sub.bias **122**.

(17) FIG. **2** shows another simplified conventional overview configuration **200**. As shown in FIG. **2**, an aggressor signal **102**, denoted by φ.sub.aggr, is amplified by amplifier **104** and provided to receive end **106** of aggressor line **108**. Aggressor line **108** is near victim line **110** in a parallel arrangement. Coupling capacitance **112**, denoted by C.sub.DUT, between aggressor line **108** and victim line **110** is measured by using switched parallel current measurement architecture **202** at transit end of victim line **110**. Switched parallel current measurement architecture **202** includes switch 1 **204**, closed in φ.sub.2, which when closed provides voltage bias **206**, denoted V.sub.bias, and switch 2 **208**, closed in φ.sub.3, which when closed provide the signal from victim line **110** to switched capacitance amplifier **210** that includes amplifier **212**, switch **214**, closed in φ.sub.Reset, and capacitor **216**, denoted by C.sub.int. The output of switched capacitance amplifier **212** is provided to integrator and comparator **218**.

(18) On-chip analog-to-digital conversion and calibration are used to eliminate off-chip noise and to extend the measurement accuracy by removing system noise. The test circuit uses switched-capacitor circuits with digital outputs. Coupling noise is sensed by the receiver and passed to the input of the integrator where the sensed noise voltage is amplified and integrated. The integrated

coupling noise is converted to a digital signal by an on-chip ADC consisting of a 1-bit differential comparator and a 10-bit counter. The integrated coupling noise is applied to the inputs of the comparator and compared to the reference voltages at each clock cycle as shown in FIG. **3** and FIG. **4**.

(19) There is noise, however, caused by clock feedthrough from the switches, OPAMP offset, mismatch of the two differential paths, and other forms of random noise. Other noise sources such as noise, thermal noise, and kT/C noise may also exist in the integrator output analog voltage signal. In order to achieve accurate results, these noise sources must be removed from the integrator output. An on-chip calibration process is used in this test circuit to remove the integrator offset voltage and other noise voltages.

(20) The system noise in the measured data is removed by an on-chip calibration process. During the calibration process, the noise generators are maintained inactive such that only the system noise is integrated and compared to the reference voltages. A digital code is generated at the end of the calibration process and used to calibrate the raw test data. Each measurement generates two 10-bit digital codes, the raw data code and the calibration code. The peak-to-peak substrate noise voltage is determined from the integrator gain, reference voltages, and the decimal value of the two digital codes.

(21) FIG. **3** shows a block diagram circuit configuration **300** according to examples of the present disclosure. As shown in FIG. **3**, the circuit comprises timing circuit **302** that has two inputs, namely clock signal input **304** and reset input **306**, both shown in FIG. **5**. Output from timing circuit **302** is provided to coupling generator (aggressor) **308** (amplifier **404** of FIG. **4**). Output from coupling generator (aggressor) **308** is provided to coupling interconnect (DUI) **310** (coupled first communication transmission line **407** and second communication transmission line **409** of FIG. **4**). Output from coupling interconnect (DUI) **310**, which represents the charge transfer to the victim line, is provided to parasitic tolerant capacitive buffer **312** (also shown in **410** of FIG. **4**). Output signal from parasitic tolerant capacitive buffer **312**, denoted by V.sub.COMP, is provided to integrator and comparator **314** (also shown in **426** and **434** of FIG. **4**). Output from integrator and comparator **314** (also shown in **436** of FIG. **4** that goes to **316** of FIG. **3**) is provided to 10-bit counter **316**. Output from 10-bit counter **316** is D.sub.out. Output from timing circuit **302** is also provided to parasitic tolerant capacitive buffer **312**, integrator and comparator **314**, and 10-bit counter **316**.

(22) FIG. **4** shows an example configuration of FIG. **3** that includes a parasitic tolerant CBCM with auto-zeroing capacitive buffer **400** according to examples of the present disclosure. As shown in FIG. **4**, an aggressor signal **402**, denoted by ϕ.sub.aggr, is a periodic digital signal that is amplified by amplifier **404** and provided to receive end **405** of first communication transmission line **407** (e.g., aggressor line, such as aggressor line **108**). For example, aggressor signal **402** is shown FIG. **5** at **508**. First communication transmission line **407** is near second communication transmission line **409** (e.g., victim line, such as victim line **110**) in a parallel arrangement. In some examples, first communication transmission line **407** (e.g., aggressor line, such as aggressor line **108**) and second communication transmission line **409** (e.g., victim line) are separated by a distance that ranges from the scale of microns to the scale of millimeters. In some examples, the digital communications channels comprise application-specific integrated circuits (ASICs) or field programmable gate arrays (FPGAs).

(23) Coupling capacitance **406**, denoted by C.sub.DUT, between first communication transmission line **407** (e.g., such as aggressor line **108** and second communication transmission line **409** (e.g., such as victim line **110**) is measured by using a capacitive trans-impedance amplifier architecture at transmit end **411** of second communication transmission line **409** that includes parasitic capacitor **408**, denoted by C.sub.para, first switched capacitance amplifier, e.g., parasitic-tolerant capacitive auto-zeroing buffer **410**, that comprises amplifier **412**, switch **414**, closed in ϕ.sub.1, and capacitor **416**, denoted by C.sub.s. The output of parasitic-tolerant capacitive auto-zeroing buffer **410** is

provided to capacitor **418** and switch **420**, closed according to timing signal **504**, φ.sub.2, and switch **422**, closed according to timing signal **506**, φ.sub.3, When switch **420** is closed, voltage bias **424**, denoted by V.sub.bias, is provided to the system. When switch **422** is closed, the signal output from capacitor **418** is provided to second switched capacitance amplifier, e.g., capacitive trans-impedance amplifier **426** that comprises amplifier **428**, switch **430** activated by reset signal closed in φ.sub.Reset, and capacitor, e.g., feedback capacitor **432**, denoted by C.sub.int. The output of capacitive trans-impedance amplifier **426** is provided to integrator and comparator, e.g., voltage comparator circuit **434**.

(24) In operation, parasitic-tolerant capacitive auto-zeroing buffer **410** is configured to bias second communication transmission line **409** (e.g., victim line) and displace a coupling charge transferred as a result of coupling from first communication transmission line **407** (e.g., aggressor line) to second communication transmission line **409** (e.g., victim line) to a switched capacitor storage element, such as capacitor **416**, denoted by C.sub.s. Capacitive trans-impedance amplifier (CTIA) **426** is configured to integrate displaced coupling charge onto an output voltage node, denoted V.sub.int. Voltage comparator circuit **434**, such as a dynamic, clocked voltage comparator, is configured to switch states once the CTIA integration has surpassed a reference trippoint, denoted V.sub.COMP. Second communication transmission line **409** (i.e., victim line) maintains a constant bias and no charge from parasitic capacitance C.sub.para **408** is transferred to the CTIA.

(25) FIG. **5** shows a timing diagram **500** for FIG. **3** and FIG. **4**. Timing diagram **500** shows timing signal, φ.sub.1, **502** for switch **414**, timing signal, φ.sub.2, **504** for switch **420**, timing signal **506**, in φ.sub.3, for switch **422**, timing signal **508** for aggressor signal **402**, denoted by φ.sub.aggr, timing signal **510** for reset signal denoted by φ.sub.Reset for switch **430**, and timing signal **512** for V.sub.int. The high signal values represent a signal that closes the respective switch and the low signals values represent a signal that opens the respective switch.

(26) FIG. **6**A and FIG. **6**B show a zoomed-out view of the timing diagram of FIG. **5**, and in particular plots of V.sub.int versus number of cycles. As shown in FIG. **6**A and FIG. **6**B, the voltage, as denoted C.sub.DUT, is shown plotted against V.sub.int versus the number of cycles and when the V.sub.int reaches the known threshold, as denoted V.sub.COMP, capacitive trans-impedance amplifier **426** outputs a signal to voltage comparator circuit **434**.

(27) FIG. **7**A and FIG. **7**B show simulation results for the configuration of FIG. **4**. In particular, FIG. **7**A shows a plot of C.sub.meas[fF] versus C.sub.dut that illustrates simulated measurement (C.sub.meas) for a logarithmic sweep of coupling capacitance (C.sub.DUT) and FIG. **7**B shows a plot of

(28) $\frac{dC_{meas}}{dC_{DUT}}$

versus C.sub.DUT that illustrates derivate of simulation results that shows 99.95% linearity over 5 orders of magnitude. The simulation results are based on transient simulations with foundry-provided transistor models and emulated wiring interconnect in Cadence Virtuoso that validate the improved performance with 10 aF resolution and 1 nF parasitic capacitance.

(29) FIG. **8** shows a method **800** for measuring capacitive-coupling between adjacent communication transmission lines according to examples of the present disclosure. Method **800** comprises providing a periodic digital signal to a first communication line that induces a charge to flow in a nearby second communication line, wherein the charge flows through a capacitive auto-zeroing buffer, as in **802**. Referring to FIG. **4**, aggressor signal **402**, denoted by φ.sub.aggr, is provided to receive end **405** of first communication transmission line **407** (e.g., such as aggressor line **108**) where first communication transmission line **407** is near second communication transmission line **409** (e.g., such as victim line **110**) in a parallel arrangement with coupling capacitance **406**, denoted by C.sub.DUT, between first communication transmission line **407** and second communication transmission line **409**.

(30) Method **800** continues by integrating the charge onto a feedback capacitor of a capacitive trans-impedance amplifier when the charge is positive due to a positive change in voltage of the

periodic digital signal on the first communication line, as in **804**. Returning to FIG. **4**, feedback capacitor **432**, denoted by C.sub.int, (the feedback capacitor) of capacitive trans-impedance amplifier **426** integrates the charge induced on second communication transmission line **409** (e.g., victim line) by first communication transmission line **407** (e.g., aggressor line).

(31) Method **800** continues by disconnecting the capacitive trans-impedance amplifier from a signal path prior to a negative charge flow due to a negative change in voltage in the signal in the first communication line, as in **806**. Returning to FIG. **4**, capacitive trans-impedance amplifier **426** is disconnected from the signal path by first closing switch **422** and then opening switch **420** when aggressor signal **402** induces a negative charge flow in second communication transmission line **409**.

(32) Method **800** continues by integrating in one direction (only positive charge so that voltage only flows in one direction) until integrated charge formulates a voltage which crosses a known threshold as measured on a voltage comparator circuit, as in **808**. Returning to FIG. **4**, capacitive trans-impedance amplifier **426** is reconnected from the signal path by first opening switch **422** and then closing switch **420** when aggressor signal **402** again induces a positive charge flow in second communication transmission line **409**. Also as shown in FIG. **6**A and FIG. **6**B, the voltage, as denoted C.sub.DUT, is shown plotted against V.sub.int versus the number of cycles and when the V.sub.int reaches the known threshold, as denoted V.sub.COMP, the capacitive trans-impedance amplifier **426** outputs a signal to voltage comparator circuit **434**.

(33) Method **800** continues by counting a number of cycles required to cross the known threshold to infer a coupling capacitance between the first and the second communications lines, as in **810**. Returning to FIG. **4**, voltage comparator circuit **434** then counts the number of cycles required to cross the known threshold, as denoted V.sub.COMP in FIG. **6**A and FIG. **6**B, and then outputs a signal representative of completion of the process.

(34) Method **800** can continue by receiving, at a processor, an output from the voltage comparator circuit and determining a capacitive-based coupling, as in **812**. Returning to FIG. **3**, the number of cycles counted prior to crossing the known threshold by 10-bit counter **316** is used to determine a capacitive-based coupling.

(35) Method **800** can continue by prior to the providing the periodic digital signal, the method comprises resetting a capacitive buffer capacitor of capacitive auto-zeroing buffer by closing and reopening a switch in parallel with the capacitive buffer capacitor at a first time and resetting the feedback capacitor of the capacitive trans-impedance amplifier by closing and reopening a switch in parallel with the feedback capacitor at a second time, as in **814**. Returning to FIG. **4**, capacitive trans-impedance amplifier is reset by first opening switch **420** and then opening switch **430**.

(36) In some embodiments, any of the methods of the present disclosure may be executed by a computing system. FIG. **9** illustrates an example of such a computing system **900**, in accordance with some embodiments. The computing system **900** may include a computer or computer system **901**A, which may be an individual computer system **901**A or an arrangement of distributed computer systems. The computer system **901**A includes one or more analysis module(s) **902** configured to perform various tasks according to some embodiments, such as one or more methods disclosed herein. To perform these various tasks, the analysis module **902** executes independently, or in coordination with, one or more hardware processors **904**, which is (or are) connected to one or more non-transitory computer readable medium **906**, such as a computer storage media. The hardware processor(s) **904** is (or are) also connected to a network interface **907** to allow the computer system **901**A to communicate over a data network **909** with one or more additional computer systems and/or computing systems, such as **901**B, **901**C, and/or **901**D (note that computer systems **901**B, **901**C and/or **901**D may or may not share the same architecture as computer system **901**A, and may be located in different physical locations, e.g., computer systems **901**A and **901**B may be located in a processing facility, while in communication with one or more computer systems such as **901**C and/or **901**D that are located in one or more data centers, and/or

located in varying countries on different continents). A processor can include a microprocessor, microcontroller, processor module or subsystem, programmable integrated circuit, programmable gate array, or another control or computing device.

(37) The non-transitory computer readable medium **906** can be implemented as one or more computer-readable or machine-readable storage media. The non-transitory computer readable medium **906** can be connected to or coupled with a machine learning module(s) **908**. Note that while in the example embodiment of FIG. **9** non-transitory computer readable medium **906** is depicted as within computer system **901**A, in some embodiments, non-transitory computer readable medium **906** may be distributed within and/or across multiple internal and/or external enclosures of computing system **901**A and/or additional computing systems. The non-transitory computer readable medium **906** may include one or more different forms of memory including semiconductor memory devices such as dynamic or static random access memories (DRAMs or SRAMs), erasable and programmable read-only memories (EPROMs), electrically erasable and programmable read-only memories (EEPROMs) and flash memories, magnetic disks such as fixed, floppy and removable disks, other magnetic media including tape, optical media such as compact disks (CDs) or digital video disks (DVDs), BLURAY® disks, or other types of optical storage, or other types of storage devices. Note that the instructions discussed above can be provided on one computer-readable or machine-readable storage medium, or alternatively, can be provided on multiple computer-readable or machine-readable storage media distributed in a large system having possibly plural nodes. Such computer-readable or machine-readable storage medium or media is (are) considered to be part of an article (or article of manufacture). An article or article of manufacture can refer to any manufactured single component or multiple components. The storage medium or media can be located either in the machine running the machine-readable instructions or located at a remote site from which machine-readable instructions can be downloaded over a network for execution.

(38) It should be appreciated that computer system **900** (or computing system) is only one example of a computing system, and that computer system **900** may have more or fewer components than shown, may combine additional components not depicted in the example embodiment of FIG. **9**, and/or computer system **900** may have a different configuration or arrangement of the components depicted in FIG. **9**. The various components shown in FIG. **9** may be implemented in hardware, software, or a combination of both hardware and software, including one or more signal processing and/or application specific integrated circuits.

(39) Further, the steps in the processing methods described herein may be implemented by running one or more functional modules in an information processing apparatus such as general-purpose processors or application specific chips, such as ASICs, FPGAs, PLDs, or other appropriate devices. These modules, combinations of these modules, and/or their combination with general hardware are all included within the scope of protection of the invention.

(40) Models and/or other interpretation aids may be refined in an iterative fashion; this concept is applicable to embodiments of the present methods discussed herein. This can include use of feedback loops executed on an algorithmic basis, such as at a computing device (e.g., computing system **900**, FIG. **9**), and/or through manual control by a user who may make determinations regarding whether a given step, action, template, model, or set of curves has become sufficiently accurate for the evaluation of the signal(s) under consideration.

(41) The above-disclosed examples of the present disclosure can include one or more of the following clauses.

(42) Clause 1. A system for measuring parasitic capacitance coupling between a first communication transmission line (**407**) and a second communication transmission line (**409**) that are adjacent, the system comprising: a parasitic tolerant capacitive based coupling measurement circuit (CBCM) (**400**), the CBCM comprising: a capacitive auto-zeroing buffer (**410**) configured to bias the second communication transmission line (**409**) and displace coupling charge transferred

from the first communication transmission line to a switched capacitor storage element; a capacitive trans-impedance amplifier (**426**) configured to integrate displaced coupling charge onto an output voltage node; and a comparator (**434**) configured to switch states once the capacitive trans-impedance amplifier integration has surpassed a reference trippoint.

(43) Clause 2. The system of clause 1, further comprising a digital signal generator (**308**) that provides a digital periodic signal to a receive end (**405**) of the first communication transmission line.

(44) Clause 3. The system of clause 1 or clause 2, wherein the digital periodic signal in the first communication transmission line induces a charge to flow in the second communication transmission line.

(45) Clause 4. The system of any of clauses 1-3, wherein the second communication transmission line maintains a constant bias and no charge from parasitic capacitances is transferred to the capacitive trans-impedance amplifier.

(46) Clause 5. The system of any of clauses 1-4, wherein the first communication transmission line is an aggressor line.

(47) Clause 6. The system of any of clauses 1-5, wherein the second communication transmission line is a victim line.

(48) Clause 7. The system of any of clauses 1-6, wherein the first communication transmission line and the second communication transmission line are high-speed analog communications channels.

(49) Clause 8. The system of any of clauses 1-7, wherein the first communication transmission line and the second communication transmission line are digital communications channels.

(50) Clause 9. The system of any of clauses 1-8, wherein the digital communications channels comprise ASICs or FPGAs.

(51) Clause 10. The system of any of clauses 1-9, further comprising a processor configured to receive an output from the voltage comparator and determine the capacitive-based coupling measurement.

(52) Clause 11. The system of any of clauses 1-10, wherein the voltage comparator is a dynamic, clocked voltage comparator.

(53) Clause 12. A method to determine a coupling capacitance between a first communication line and a second communication line, the method comprising: providing a periodic digital signal to a first communication transmission line that induces a charge to flow in a nearby second communication transmission line, wherein the charge flows through a capacitive auto-zeroing buffer; integrating the charge onto a feedback capacitor of a capacitive trans-impedance amplifier when the charge is positive due to a positive change in voltage of the periodic digital signal on the first communication transmission line; disconnecting the capacitive trans-impedance amplifier from a signal path prior to a negative charge flow due to a negative change in voltage in the signal in the first communication transmission line; integrating in one direction until integrated charge formulates a voltage which crosses a known threshold as measured on a voltage comparator circuit; and counting a number of cycles required to cross the known threshold to infer a coupling capacitance between the first communication transmission line and the second communication transmission line.

(54) Clause 13. The method of clause 12, wherein prior to the providing the periodic digital signal, the method comprises resetting a capacitive buffer capacitor of a capacitive auto-zeroing buffer by closing and reopening a switch in parallel with the capacitive buffer capacitor at a first time and resetting the feedback capacitor of the capacitive trans-impedance amplifier by closing and reopening a switch in parallel with the feedback capacitor at a second time.

(55) Clause 14. The method of any of clauses 12-13, wherein the second communication transmission line maintains a constant bias and no charge from parasitic capacitances is transferred to the capacitive trans-impedance amplifier.

(56) Clause 15. The method of any of clauses 12-14, wherein the first communication transmission

line is an aggressor line.

(57) Clause 16. The method of any of clauses 12-15, wherein the second communication transmission line is a victim line.

(58) Clause 17. The method of any of clauses 12-16, wherein the first communication transmission line and the second communication transmission line are high-speed analog communications channels.

(59) Clause 18. The method of any of clauses 12-17, wherein the first communication transmission line and the second communication transmission line are digital communications channels.

(60) Clause 19. The method of any of clauses 12-18, wherein the digital communications channels comprise ASICs or FPGAs.

(61) Clause 20. The method of any of clauses 12-19, further comprising receiving, at a processor, an output from the voltage comparator circuit and determining a capacitive-based coupling.

(62) The foregoing description, for purpose of explanation, has been described with reference to specific embodiments. However, the illustrative discussions above are not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in view of the above teachings. Moreover, the order in which the elements of the methods are illustrated and described may be re-arranged, and/or two or more elements may occur simultaneously. The embodiments were chosen and described in order to best explain the principles of the invention and its practical applications, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated.

(63) Notwithstanding that the numerical ranges and parameters setting forth the broad scope of the embodiments are approximations, the numerical values set forth in the specific examples are reported as precisely as possible. Any numerical value, however, inherently contains certain errors necessarily resulting from the standard deviation found in their respective testing measurements. Moreover, all ranges disclosed herein are to be understood to encompass any and all sub-ranges subsumed therein. For example, a range of "less than 10" can include any and all sub-ranges between (and including) the minimum value of zero and the maximum value of 10, that is, any and all sub-ranges having a minimum value of equal to or greater than zero and a maximum value of equal to or less than 10, e.g., 1 to 5. In certain cases, the numerical values as stated for the parameter can take on negative values. In this case, the example value of range stated as "less than 10" can assume negative values, e.g. $-1, -2, -3, -10, -20, -30$, etc.

(64) The following embodiments are described for illustrative purposes only with reference to the Figures. Those of skill in the art will appreciate that the following description is exemplary in nature, and that various modifications to the parameters set forth herein could be made without departing from the scope of the present embodiments. It is intended that the specification and examples be considered as examples only. The various embodiments are not necessarily mutually exclusive, as some embodiments can be combined with one or more other embodiments to form new embodiments.

(65) While the embodiments have been illustrated respect to one or more implementations, alterations and/or modifications can be made to the illustrated examples without departing from the spirit and scope of the appended claims. In addition, while a particular feature of the embodiments may have been disclosed with respect to only one of several implementations, such feature may be combined with one or more other features of the other implementations as may be desired and advantageous for any given or particular function.

(66) Furthermore, to the extent that the terms "including", "includes", "having", "has", "with", or variants thereof are used in either the detailed description and the claims, such terms are intended to be inclusive in a manner similar to the term "comprising." As used herein, the phrase "one or more of", for example, A, B, and C means any of the following: either A, B, or C alone; or combinations of two, such as A and B, B and C, and A and C; or combinations of A, B and C.

(67) Other embodiments will be apparent to those skilled in the art from consideration of the specification and practice of the descriptions disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the embodiments being indicated by the following claims.

Claims

1. A system for measuring parasitic capacitance coupling between a first communication transmission line and a second communication transmission line that are adjacent, the system comprising: a parasitic tolerant capacitive based coupling measurement circuit (CBCM), the CBCM comprising: a capacitive auto-zeroing buffer configured to bias the second communication transmission line and displace coupling charge transferred from the first communication transmission line to a switched capacitor storage element; a capacitive trans-impedance amplifier configured to integrate displaced coupling charge onto an output voltage node of the second communication transmission line; and a comparator configured to switch states of the capacitive trans-impedance amplifier once the capacitive trans-impedance amplifier integration has surpassed a reference trippoint.

2. The system of claim 1, further comprising a digital signal generator that provides a digital periodic signal to a receive end of the first communication transmission line.

3. The system of claim 2, wherein the digital periodic signal in the first communication transmission line induces a charge to flow in the second communication transmission line.

4. The system of claim 1, wherein the second communication transmission line maintains a constant bias and no charge from parasitic capacitances is transferred to the capacitive trans-impedance amplifier.

5. The system of claim 1, wherein the first communication transmission line is an aggressor line.

6. The system of claim 1, wherein the second communication transmission line is a victim line.

7. The system of claim 1, wherein the first communication transmission line and the second communication transmission line are high-speed analog communications channels.

8. The system of claim 1, wherein the first communication transmission line and the second communication transmission line are digital communications channels.

9. The system of claim 8, wherein the digital communications channels comprise application-specific integrated circuits (ASICs) or field programmable gate arrays (FPGAs).

10. The system of claim 1, further comprising a processor configured to receive an output from the comparator and determine a capacitive-based coupling measurement.

11. The system of claim 1, wherein the comparator is a dynamic, clocked voltage comparator.

12. A method to determine a coupling capacitance between a first communication transmission line and a second communication transmission line, the method comprising: providing a periodic digital signal to a first communication transmission line that induces a charge to flow in a nearby second communication transmission line, wherein the charge flows through a capacitive auto-zeroing buffer; integrating the charge onto a feedback capacitor of a capacitive trans-impedance amplifier when the charge is positive due to a positive change in voltage of the periodic digital signal on the first communication transmission line; disconnecting the capacitive trans-impedance amplifier from a signal path prior to a negative charge flow due to a negative change in voltage in the periodic digital signal in the first communication transmission line; integrating in one direction until integrated charge formulates a voltage which crosses a known threshold as measured on a voltage comparator circuit; and counting a number of cycles required to cross the known threshold to infer a coupling capacitance between the first communication transmission line and the second communication transmission line.

13. The method of claim 12, wherein prior to the providing the periodic digital signal, the method comprises resetting a capacitive buffer capacitor of a capacitive auto-zeroing buffer by closing and

reopening a switch in parallel with the capacitive buffer capacitor at a first time and resetting the feedback capacitor of the capacitive trans-impedance amplifier by closing and reopening a switch in parallel with the feedback capacitor at a second time.

14. The method of claim 12, wherein the second communication transmission line maintains a constant bias and no charge from parasitic capacitances is transferred to the capacitive trans-impedance amplifier.

15. The method of claim 12, wherein the first communication transmission line is an aggressor line.

16. The method of claim 12, wherein the second communication transmission line is a victim line.

17. The method of claim 12, wherein the first communication transmission line and the second communication transmission line are high-speed analog communications channels.

18. The method of claim 12, wherein the first communication transmission line and the second communication transmission line are digital communications channels.

19. The method of claim 18, wherein the digital communications channels comprise application-specific integrated circuits (ASICs) or field programmable gate arrays (FPGAs).

20. The method of claim 12, further comprising receiving, at a processor, an output from the voltage comparator circuit and determining a capacitive-based coupling.