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(54) CLOCK CONTROL METHOD, DEVICE FOR SWITCH CHIP, AND SWITCH BOARD

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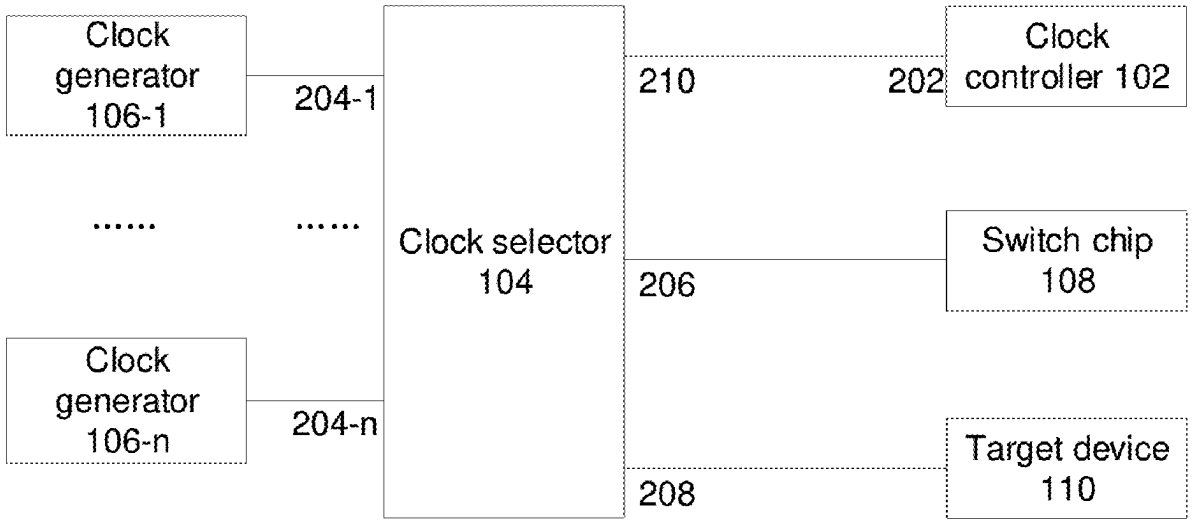
(57) **ABSTRACT**

Provided are a clock control method, device for a switch chip, and a switch board. The method is applied to a clock control device, and includes: receiving clock signals transmitted by clock generators of a plurality of clock types, the clock control device is connected to a switch chip, the switch chip uses clock signals of different clock types in response to controlling target devices of different device types, and the plurality of clock types correspond to a plurality of device types; identifying a target device type of the plurality of device types, to which a target device belongs; and transmitting, to the switch chip and the target device, a target clock signal transmitted by a target clock generator of the clock generators of the plurality of clock types, the target clock generator is a clock generator of a target clock type corresponding to the target device type.



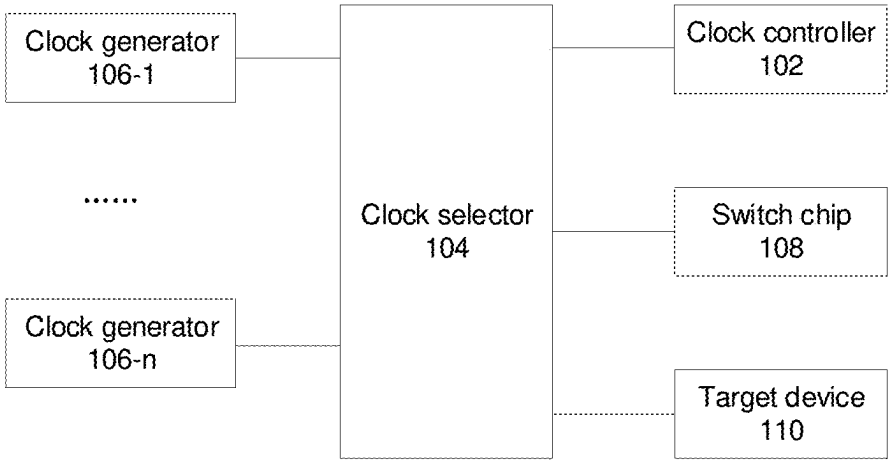

Clock generator 106-1
.....
Clock generator 106-n
Clock selector 104
Clock controller 102
Switch chip 108
Target device 110

FIG. 1

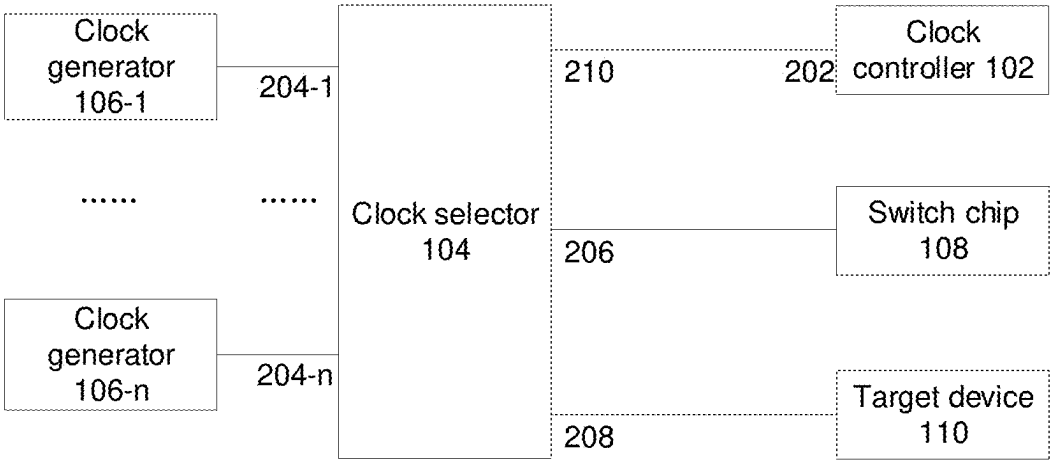

Clock generator 106-1
204-1
.....
.....
Clock generator 106-n
204-n
Clock selector 104
210
202
Clock controller 102
206
Switch chip 108
208
Target device 110

FIG. 2

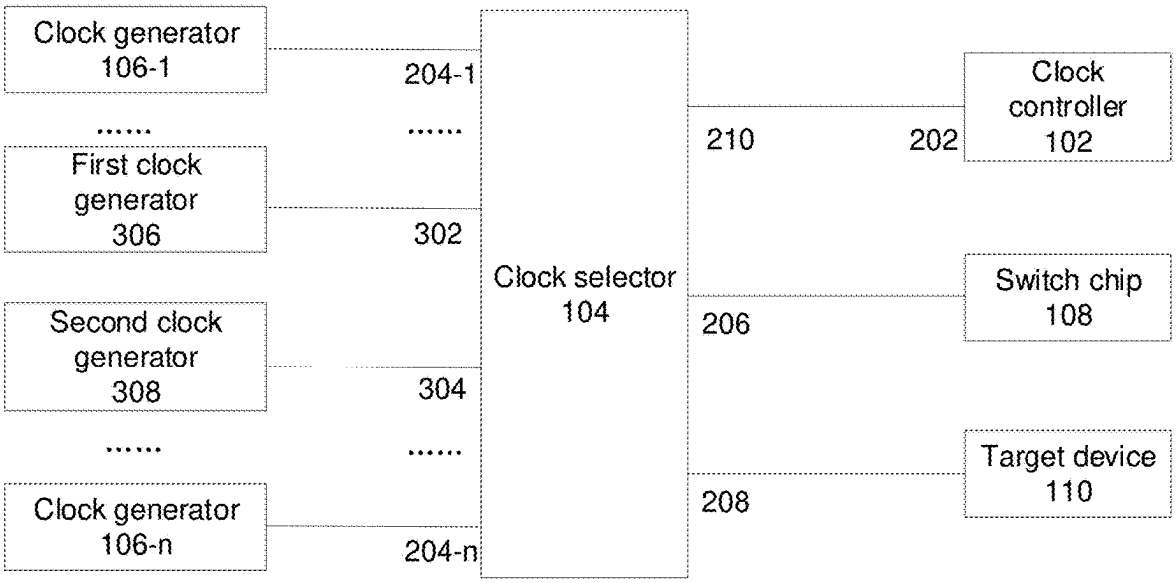

Clock generator 106-1
.....
First clock generator 306
Second clock generator 308
.....
Clock generator 106-n
204-1
.....
302
304
.....
204-n
Clock selector 104
210
202
206
208
Clock controller 102
Switch chip 108
Target device 110

FIG. 3

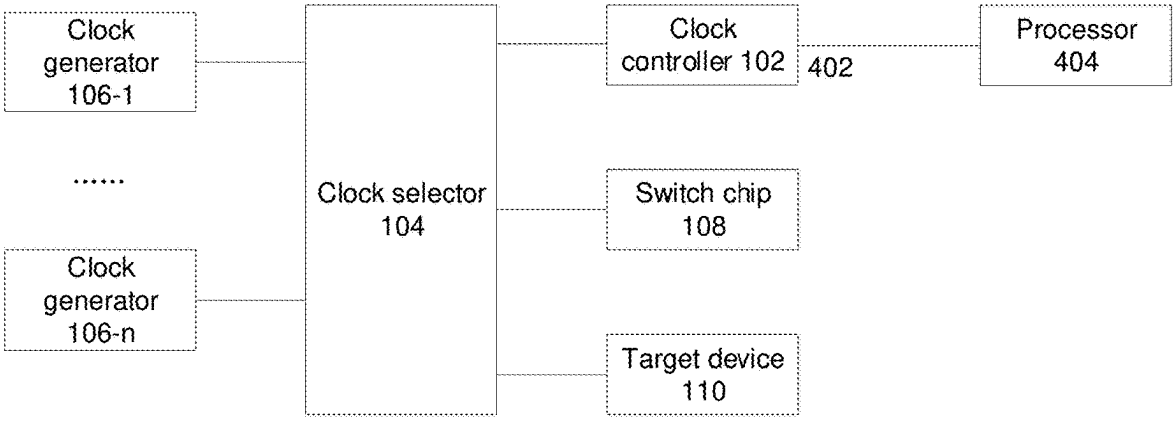

Clock generator 106-1
.....
Clock generator 106-n
Clock selector 104
Clock controller 102
402
Processor 404
Switch chip 108
Target device 110

FIG. 4

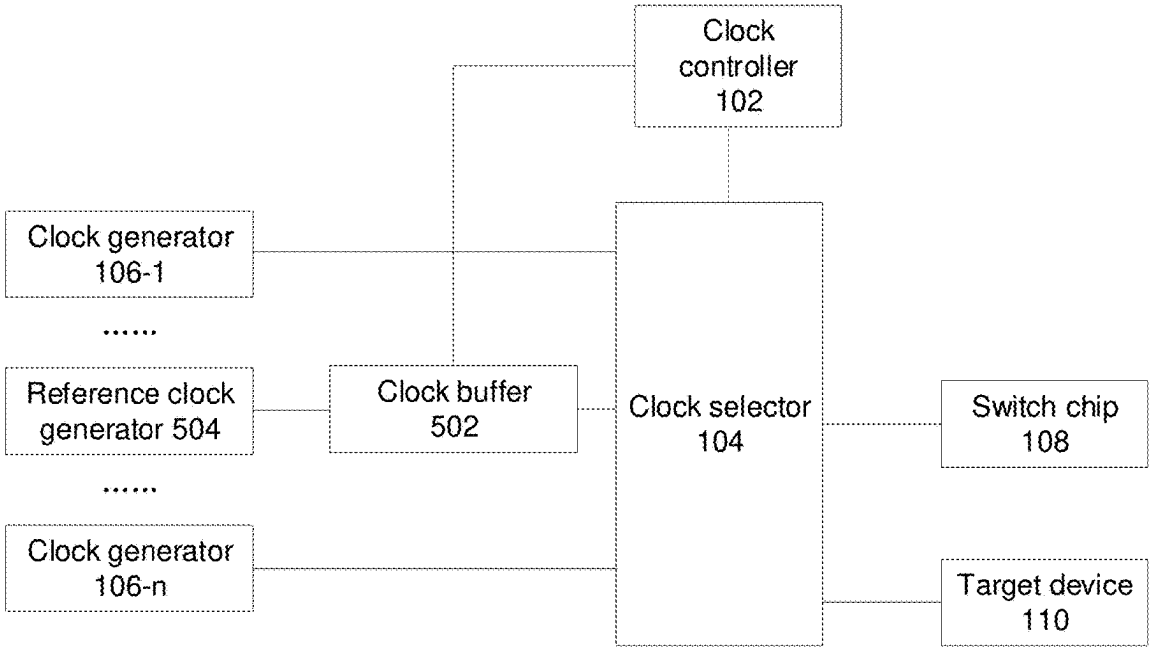

Clock controller 102
Clock generator 106-1
.....
Reference clock generator 504
.....
Clock generator 106-n
Clock buffer 502
Clock selector 104
Switch chip 108
Target device 110

FIG. 5

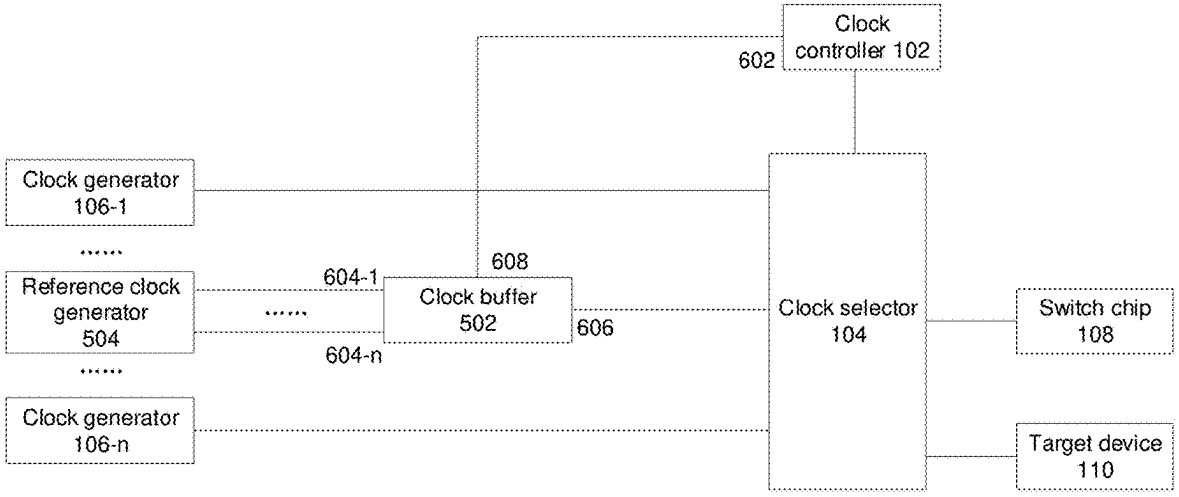

Clock controller 102
602
Clock generator 106-1
.....
Reference clock generator 504
.....
Clock generator 106-n
604-1
.....
604-n
608
Clock buffer 502
606
Clock selector 104
Switch chip 108
Target device 110

FIG. 6

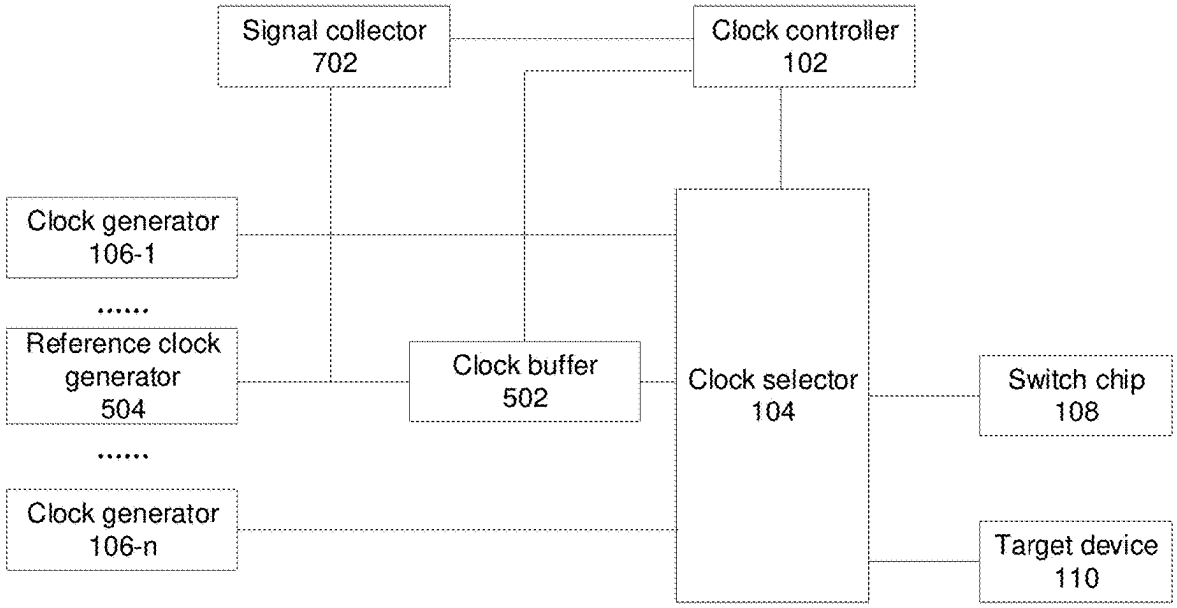

Signal collector
702
Clock controller
102
Clock generator
106-1
.....
Reference clock
generator
504
.....
Clock generator
106-n
Clock buffer
502
Clock selector
104
Switch chip
108
Target device
110

FIG. 7

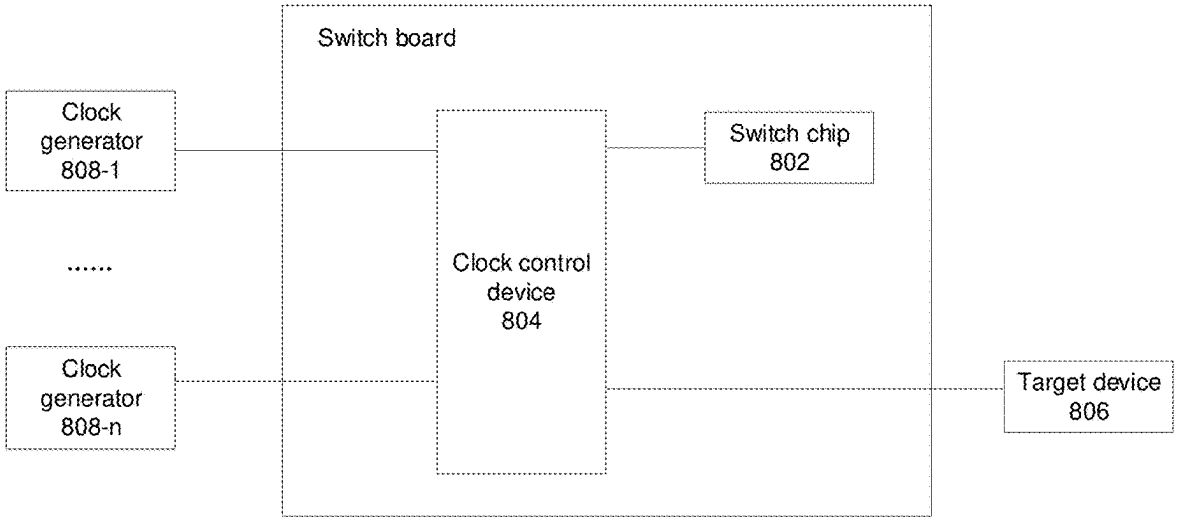

Switch board
Clock
generator
808-1
.....
Clock
generator
808-n
Clock control
device
804
Switch chip
802
Target device
806

FIG. 8

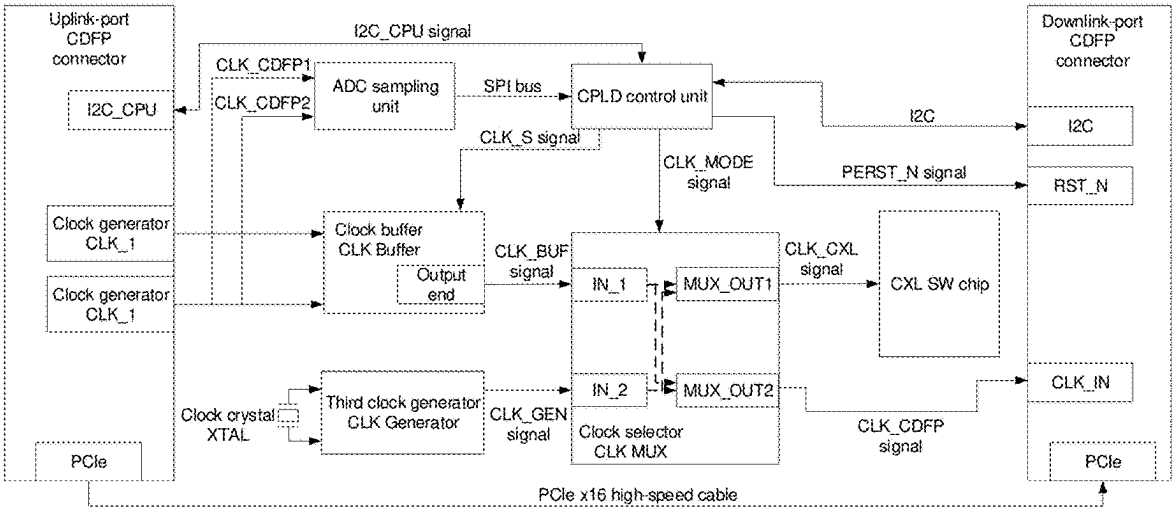

Uplink-port CDFP connector
I2C_CPU signal
Downlink-port CDFP connector
CLK_CDFP1
CLK_CDFP2
ADC sampling unit
SPI bus
CPLD control unit
I2C_CPU
I2C
I2C
CLK_S signal
CLK_MODE signal
PERST_N signal
RST_N
Clock generator CLK_1
Clock buffer CLK Buffer
Output end
CLK_BUF signal
IN_1
MUX_OUT1
CLK_CXL signal
CXL SW chip
Clock generator CLK_1
Third clock generator CLK Generator
IN_2
MUX_OUT2
CLK_IN
Clock crystal XTAL
CLK_GEN signal
Clock selector CLK MUX
CLK_CDFP signal
PCIe
PCIe
PCIe x16 high-speed cable

FIG. 9

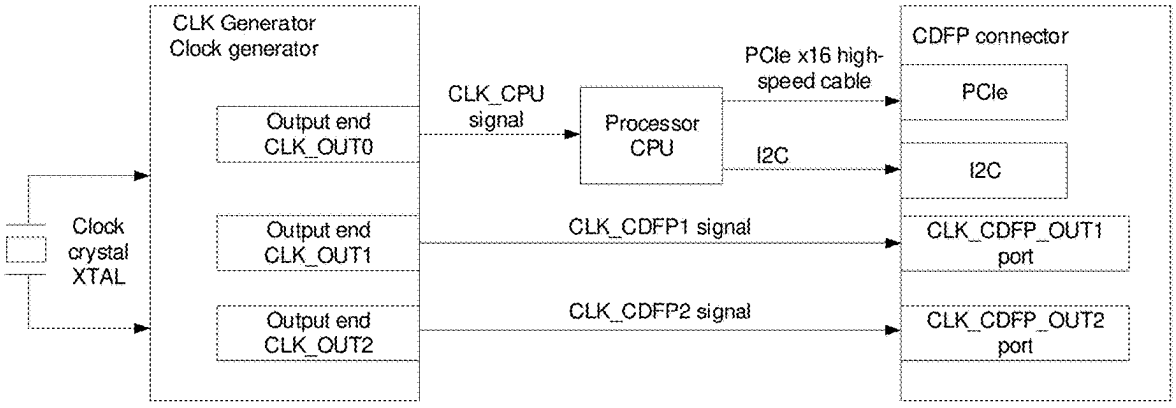

CLK Generator
Clock generator
CDFP connector
PCIe x16 high-speed cable
CLK_CPU signal
Output end CLK_OUT0
Processor CPU
PCIe
I2C
Clock crystal XTAL
Output end CLK_OUT1
CLK_CDFP1 signal
CLK_CDFP_OUT1 port
Output end CLK_OUT2
CLK_CDFP2 signal
CLK_CDFP_OUT2 port

FIG. 10

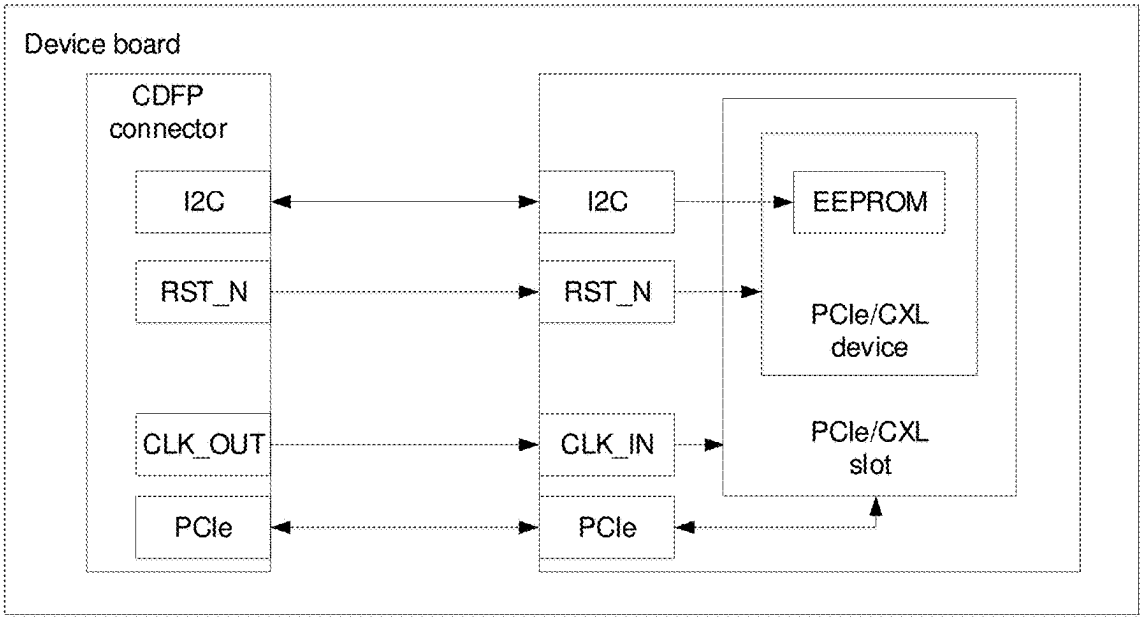

Device board
CDFP connector
I2C
RST_N
CLK_OUT
PCIe
I2C
RST_N
CLK_IN
PCIe
EEPROM
PCIe/CXL device
PCIe/CXL slot

FIG. 11

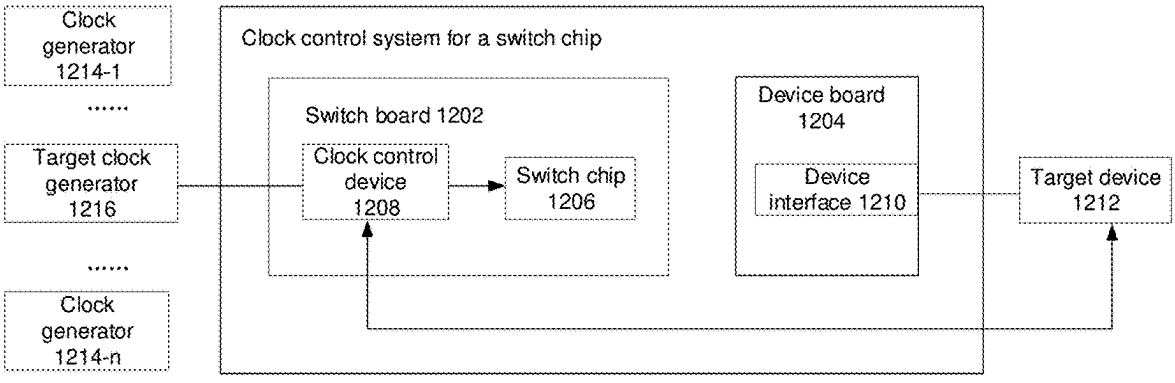

Clock generator 1214-1
.....
Target clock generator 1216
.....
Clock generator 1214-n
Clock control system for a switch chip
Switch board 1202
Clock control device 1208
Switch chip 1206
Device board 1204
Device interface 1210
Target device 1212

FIG. 12

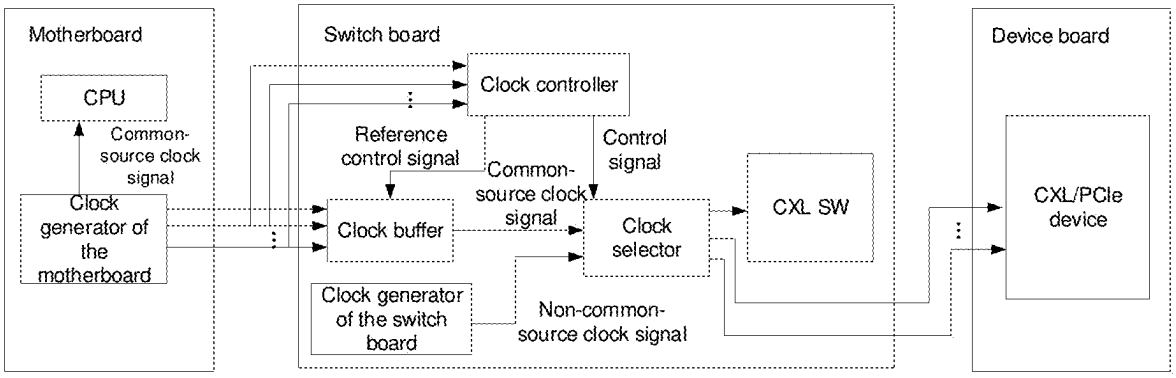

Motherboard
CPU
Common-source clock signal
Clock generator of the motherboard
Switch board
Clock controller
Reference control signal
Control signal
Common-source clock signal
Clock buffer
Clock selector
CXL SW
Clock generator of the switch board
Non-common-source clock signal
Device board
CXL/PCIe device

FIG. 13

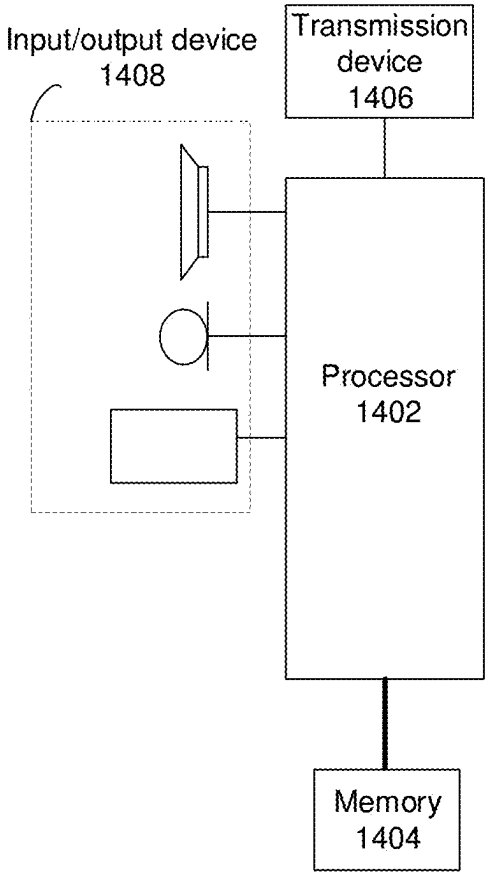

Input/output device 1408
Transmission device 1406
Processor 1402
Memory 1404

FIG. 14

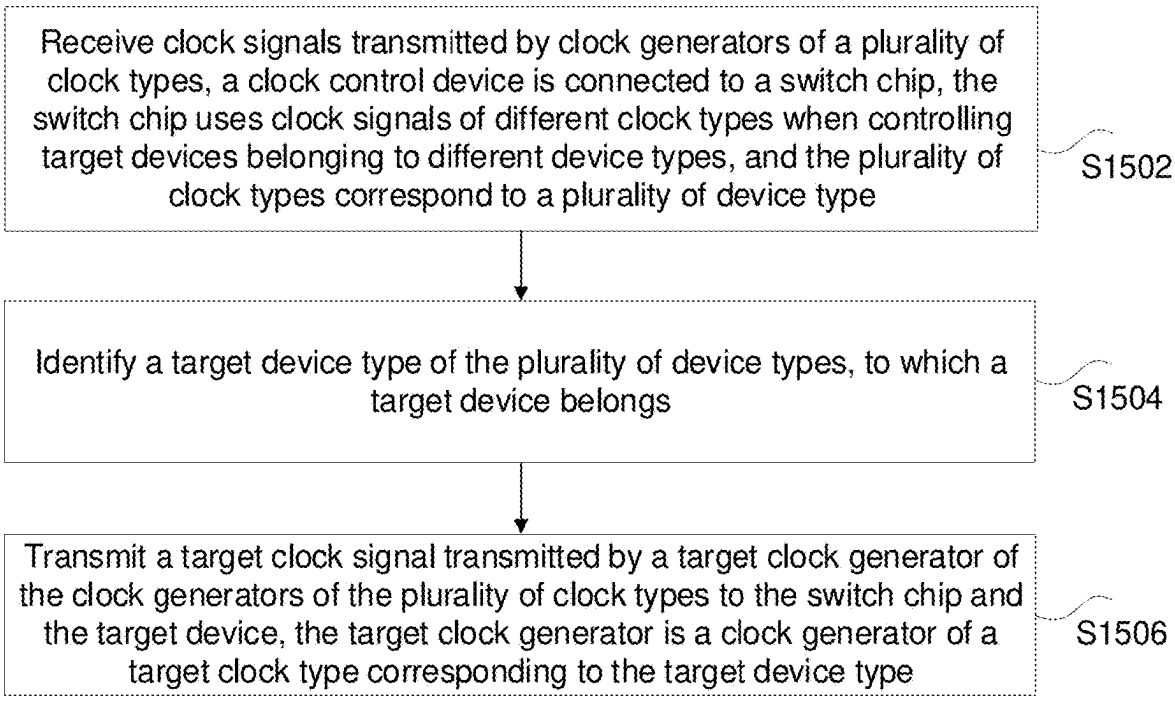

Receive clock signals transmitted by clock generators of a plurality of clock types, a clock control device is connected to a switch chip, the switch chip uses clock signals of different clock types when controlling target devices belonging to different device types, and the plurality of clock types correspond to a plurality of device type
S1502
Identify a target device type of the plurality of device types, to which a target device belongs
S1504
Transmit a target clock signal transmitted by a target clock generator of the clock generators of the plurality of clock types to the switch chip and the target device, the target clock generator is a clock generator of a target clock type corresponding to the target device type
S1506

FIG. 15

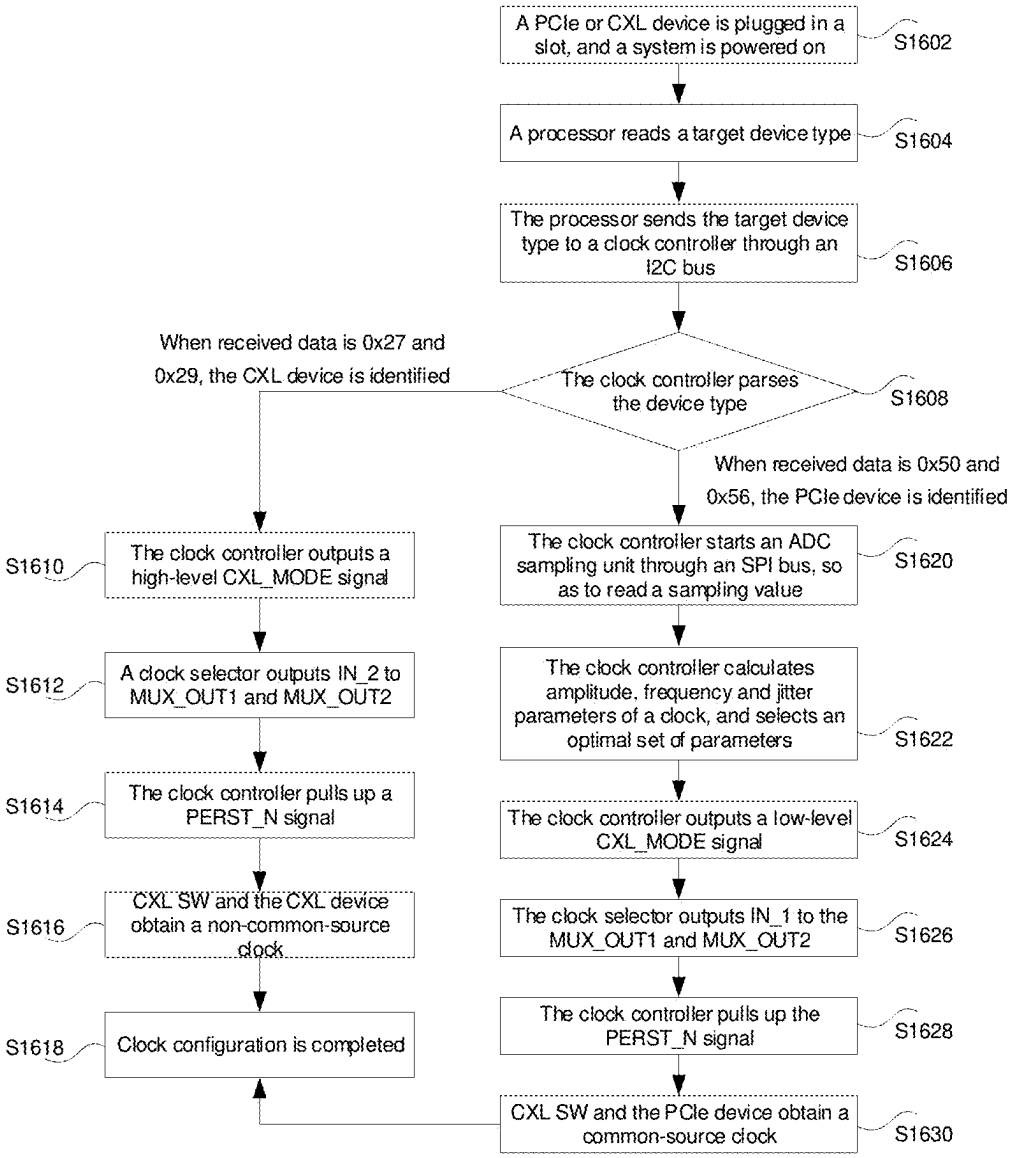

A PCIe or CXL device is plugged in a slot, and a system is powered on
S1602
A processor reads a target device type
S1604
The processor sends the target device type to a clock controller through an I2C bus
S1606
When received data is 0x27 and 0x29, the CXL device is identified
The clock controller parses the device type
S1608
When received data is 0x50 and 0x56, the PCIe device is identified
S1610
The clock controller outputs a high-level CXL_MODE signal
S1612
A clock selector outputs IN_2 to MUX_OUT1 and MUX_OUT2
S1614
The clock controller pulls up a PERST_N signal
S1616
CXL SW and the CXL device obtain a non-common-source clock
S1618
Clock configuration is completed
The clock controller starts an ADC sampling unit through an SPI bus, so as to read a sampling value
S1620
The clock controller calculates amplitude, frequency and jitter parameters of a clock, and selects an optimal set of parameters
S1622
The clock controller outputs a low-level CXL_MODE signal
S1624
The clock selector outputs IN_1 to the MUX_OUT1 and MUX_OUT2
S1626
The clock controller pulls up the PERST_N signal
S1628
CXL SW and the PCIe device obtain a common-source clock
S1630

FIG. 16

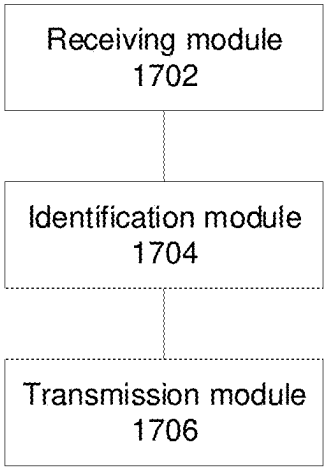

Receiving module
1702
Identification module
1704
Transmission module
1706

FIG. 17

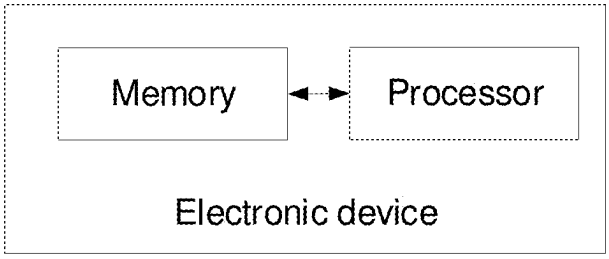

Memory
Processor
Electronic device

FIG. 18

CLOCK CONTROL METHOD, DEVICE FOR SWITCH CHIP, AND SWITCH BOARD

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application claims the priority to the Chinese patent application No.202310743573.2, titled "CLOCK CONTROL METHOD, SYSTEM AND DEVICE FOR SWITCH CHIP, AND SWITCH BOARD", filed to the Patent Office of the People's Republic of China on Jun. 21, 2023, which is incorporated herein in its entirety by reference.

TECHNICAL FIELD

[0002] Embodiments of the present application relate to the field of chips, and particularly to a clock control method, device for a switch chip, and a switch board.

BACKGROUND

[0003] A compute express link (CXL) technique is a cache-coherent interconnect protocol established on a peripheral component interconnect express standard (fifth generation) (PCIe 5.0) physical bus. The CXL technique may be used for a processor, memory expansion, and an accelerator, and allows resource sharing for higher performance. Currently, compute express link 2.0 (CXL 2.0) has been proposed in the industry, introducing a switch (SW) function to support connection with more devices and allowing a server to allocate a corresponding resource according to a workload requirement, so as to improve resource utilization and reduce an overall system cost.

[0004] Compute express link switch (CXL SW) is capable of supporting not only a working mode of a CXL device, but also an application scenario of a peripheral component interconnect express (PCIe) device, thereby causing a problem in choosing a clock mode: a PCIe device is required to work in a mode where a system clock of the SW and a reference clock share a common source, while a CXL device is required to work in a non-homologous clock mode. To enable the CXL SW to be compatible with clocks of two different devices, in related technologies, a clock mode generally is selected manually according to different plugged-in devices. However, such a method is inefficient, and as homologous clocks usually are connected through a cable, resulting in a long link, if a selected homologous clock signal has poor quality, a device is prone to be unrecognized by a central processing unit (CPU).

[0005] With respect to the problem of low clock adaptation efficiency of a switch chip, etc. in the related technologies, no effective solution has been proposed yet.

SUMMARY

[0006] Embodiments of the present application provide a clock control method, device for a switch chip, and a switch board.

[0007] According to an embodiment of the present application, a clock control device for a switch chip is provided. The device includes a clock controller and a clock selector; the clock controller is connected to the clock selector, the clock selector is allowed to be connected to clock generators of a plurality of clock types, a switch chip, and a target device, the switch chip uses clock signals of different clock types in response to controlling target devices belonging to different device types, and the plurality of clock types correspond to a plurality of device types; the clock controller is configured to identify a target device type of the plurality of device types, to which the target device belongs, and control the clock selector to transmit, to the switch chip and the target device, a target clock signal transmitted by a target clock generator of the clock generators of the plurality of clock types. The target clock generator is a clock generator of a target clock type corresponding to the target device type.

[0008] In an exemplary embodiment, a first control port is deployed on the clock controller, and a plurality of clock ports, a first output port, a second output port and a first signal port are deployed on the clock selector. The first control port is connected to the first signal port, the plurality of clock ports are configured to be connected to the clock generators of the plurality of clock types respectively, the first output port is configured to be connected to the switch chip, and the second output port is configured to be connected to the target device; the clock controller is configured to generate a target control signal corresponding to the target device type, and send the target control signal to the clock selector through the first control port; the clock selector is configured to receive the target control signal through the first signal port, and transmit the target clock signal received on a target clock port corresponding to the target control signal to the first output port and the second output port.

[0009] In an exemplary embodiment, the plurality of clock ports include a first clock port and a second clock port. The first clock port is allowed to be connected to a first clock generator of a homologous type, the second clock port is allowed to be connected to a second clock generator of a non-homologous type, the first clock generator is configured to transmit a homologous clock signal, and the second clock generator is configured to transmit a non-homologous clock signal; the clock controller is configured to generate a first control signal in response to the target device type being a first type which is a device type adopting a high-speed serial computer expansion bus standard, generate a second control signal in response to the target device type being a second type which is a device type adopting a compute express link protocol, and send the first control signal or the second control signal to the clock selector through the first control port; the clock selector is configured to transmit the homologous clock signal to the first output port and the second output port in response to receiving the first control signal, and transmit the non-homologous clock signal to the first output port and the second output port in response to receiving the second control signal.

[0010] In an exemplary embodiment, a device type port is deployed on the clock controller. The device type port is allowed to be connected to a processor, and the device type port is configured to receive the target device type sent by the processor.

[0011] In an exemplary embodiment, the clock control device further includes a clock buffer. The clock controller is connected to the clock buffer, and the clock buffer is also connected between the clock selector and a reference clock generator of the clock generators of the plurality of clock types; the reference clock generator is configured to generate a plurality of clock signals; the clock buffer is configured to buffer the plurality of clock signals; the clock controller is configured to collect signal parameters of the plurality of clock signals, determine signal quality of each of the plurality of clock signals based on the signal parameters, and

control the clock buffer to transmit a reference clock signal with the highest signal quality to the clock selector.

[0012] In an exemplary embodiment, a second control port is deployed on the clock controller, and a plurality of reference clock ports, a third output port and a second signal port are deployed on the clock buffer. The second control port is connected to the second signal port, the plurality of reference clock ports are configured to be connected to the reference clock generator, and the third output port is configured to be connected to the clock selector; the clock controller is configured to generate a reference control signal corresponding to the reference clock signal, and send the reference control signal to the clock buffer through the second control port; the clock buffer is configured to receive the reference control signal through the second signal port, and transmit the reference clock signal corresponding to the reference control signal to the third output port.

[0013] In an exemplary embodiment, the clock control device further includes a signal collector. The signal collector is connected between the reference clock generator and the clock controller; the signal collector is configured to sample the plurality of clock signals to obtain a plurality of sampling signals, and transmit the plurality of sampling signals to the clock controller; the clock controller is configured to calculate the signal parameters of the plurality of sampling signals, and convert the signal parameter of each of the sampling signals into the signal quality of each of the sampling signals. The signal parameter of each of the sampling signals including at least one of an amplitude parameter, a frequency parameter, a slope parameter and a jitter parameter.

[0014] According to another embodiment of the present application, a switch board is provided, including a switch chip and a clock control device, the clock control device is connected to the switch chip, and the clock control device is allowed to be connected to a target device and clock generators of a plurality of clock types; the switch chip uses clock signals of different clock types in response to controlling target devices belonging to different device types, and the plurality of clock types correspond to a plurality of device types; the clock control device is configured to identify a target device type of the plurality of device types, to which the target device belongs, and transmit, to the switch chip and the target device, a target clock signal transmitted by a target clock generator of the clock generators of the plurality of clock types. The target clock generator is a clock generator of a target clock type corresponding to the target device type.

[0015] In an exemplary embodiment, the clock control device includes a clock controller and a clock selector. The clock controller is connected to the clock selector, and the clock selector is allowed to be connected to the clock generators of the plurality of clock types, the switch chip and the target device; the clock controller is configured to generate a target control signal corresponding to the target device type, and send the target control signal to the clock selector; the clock selector is configured to receive the target control signal, and transmit the target clock signal corresponding to the target control signal to the switch chip and the target device.

[0016] In an exemplary embodiment, the clock generators of the plurality of clock types include a first clock generator of a homologous type and a second clock generator of a non-homologous type. The clock selector is connected to each of the first clock generator and the second clock generator, the first clock generator is configured to transmit a homologous clock signal, and the second clock generator is configured to transmit a non-homologous clock signal; the clock controller is configured to generate a first control signal in response to the target device type being a first type which is a device type adopting a high-speed serial computer expansion bus standard, generate a second control signal in response to the target device type being a second type which is a device type adopting a compute express link protocol, and send the first control signal or the second control signal to the clock selector; the clock selector is configured to transmit the homologous clock signal to the switch chip and the target device in response to receiving the first control signal, and transmit the non-homologous clock signal to the switch chip and the target device in response to receiving the second control signal.

[0017] In an exemplary embodiment, a reference clock generator of the clock generators of the plurality of clock types is allowed to generate a plurality of clock signals. The clock control device is configured to buffer the plurality of clock signals, collect signal parameters of the plurality of clock signals, determine signal quality of each of the plurality of clock signals based on the signal parameters, and determine a reference clock signal with the highest signal quality as a clock signal corresponding to the reference clock generator.

[0018] In an exemplary embodiment, the clock control device includes a clock controller, a clock selector and a clock buffer. The clock controller is connected to the clock selector, the clock selector is allowed to be connected to the clock generators of the plurality of clock types, the switch chip and the target device, and the clock buffer is connected between the reference clock generator and the clock selector; the clock controller is configured to generate a reference control signal corresponding to the reference clock signal, send the reference control signal to the clock buffer, generate a target control signal corresponding to the target device type, send the target control signal to the clock selector; the clock buffer is configured to receive the reference control signal, and transmit the reference clock signal corresponding to the reference control signal to the clock selector; the clock selector is configured to receive the target control signal, and transmit the target clock signal corresponding to the target control signal to the switch chip and the target device.

[0019] In an exemplary embodiment, the clock control device is further configured to sample the plurality of clock signals to obtain a plurality of sampling signals, calculate the signal parameters of the plurality of sampling signals, and convert the signal parameter of each of the sampling signals into the signal quality of each of the sampling signals. The signal parameter of each of the sampling signals including at least one of an amplitude parameter, a frequency parameter, a slope parameter and a jitter parameter.

[0020] In an exemplary embodiment, the clock control device is allowed to be connected to a processor. The clock control device is configured to receive the target device type sent by the processor.

[0021] In an exemplary embodiment, the switch board further includes an uplink connector, a downlink connector and a third clock generator. The third clock generator is connected to the clock control device, the clock control device is connected to a fourth clock generator of a processor through the uplink connector, and the clock generators of

the plurality of clock types include the third clock generator and the fourth clock generator; the clock control device is connected to the target device through the downlink connector.

[0022] According to still another embodiment of the present application, a clock control system for a switch chip is provided. The system includes a switch board and a device board; a switch chip and a clock control device are deployed on the switch board, and a device interface is deployed on the device board; the device interface is configured to be connected to a target device. The switch chip uses clock signals of different clock types in response to controlling target devices belonging to different device types, and the plurality of clock types correspond to a plurality of device types; the clock control device is configured to identify a target device type of the plurality of device types, to which the target device belongs, and transmit, to the switch chip and the target device, a target clock signal transmitted by a target clock generator of the clock generators of the plurality of clock types. The target clock generator is a clock generator of a target clock type corresponding to the target device type.

[0023] In an exemplary embodiment, the system further includes a motherboard. A third clock generator is deployed on the switch board, a fourth clock generator of a processor is deployed on the motherboard, and the clock control device includes a clock controller and a clock selector; the clock controller is connected to the clock selector, the clock selector is connected to the third clock generator, the fourth clock generator, the switch chip and the target device, the third clock generator is configured to transmit a non-homologous clock signal, and the fourth clock generator is configured to transmit a homologous clock signal; the clock controller is configured to generate a first control signal in response to the target device type is a first type which being a device type adopting a high-speed serial computer expansion bus standard, generate a second control signal in response to the target device type being a second type which is a device type adopting a compute express link protocol, and send the first control signal or the second control signal to the clock selector; the clock selector is configured to transmit the homologous clock signal to the switch chip and the target device in response to receiving the first control signal, and transmit the non-homologous clock signal to the switch chip and the target device in response to receiving the second control signal.

[0024] In an exemplary embodiment, the fourth clock generator is allowed to generate a plurality of clock signals, and the clock control device further includes a clock buffer. The clock buffer is connected between the fourth clock generator and the clock selector; the clock controller is configured to collect signal parameters of the plurality of clock signals, determine signal quality of each of the plurality of clock signals based on the signal parameters, determine a reference clock signal with the highest signal quality as a clock signal corresponding to the fourth clock generator, generate a reference control signal corresponding to the reference clock signal, and send the reference control signal to the clock buffer; the clock buffer is configured to buffer the plurality of clock signals, receive the reference control signal, and transmit the reference clock signal corresponding to the reference control signal to the clock selector.

[0025] In an exemplary embodiment, the processor is deployed on the motherboard, and the clock control device is connected to the processor. The processor is connected to the target device through the switch board and the device board; the processor is configured to output the target device type of the target device during training of the target device, send the target device type to the clock control device; the clock control device is configured to receive the target device type sent by the processor.

[0026] According to still another embodiment of the present application, a clock control method for a switch chip is provided. The method is applied to a clock control device, and the method includes:

[0027] receiving clock signals transmitted by clock generators of a plurality of clock types. The clock control device is connected to a switch chip, the switch chip uses clock signals of different clock types in response to controlling target devices belonging to different device types, and the plurality of clock types correspond to a plurality of device types;

[0028] identifying a target device type of the plurality of device types, to which a target device belongs; and

[0029] transmitting, to the switch chip and the target device, a target clock signal transmitted by a target clock generator of the clock generators of the plurality of clock types. The target clock generator is a clock generator of a target clock type corresponding to the target device type.

[0030] In an exemplary embodiment, the transmitting, to the switch chip and the target device, a target clock signal transmitted by a target clock generator of the clock generators of the plurality of clock types includes:

[0031] generating a target control signal corresponding to the target device type; and

[0032] transmitting the target clock signal corresponding to the target control signal to the switch chip and the target device.

[0033] In an exemplary embodiment, the clock generators of the plurality of clock types include a first clock generator of a homologous type and a second clock generator of a non-homologous type, the first clock generator is configured to transmit a homologous clock signal, and the second clock generator is configured to transmit a non-homologous clock signal;

[0034] the generating a target control signal corresponding to the target device type includes: generating a first control signal in response to the target device type being a first type which is a device type adopting a high-speed serial computer expansion bus standard, and generating a second control signal in response to the target device type being a second type which is a device type adopting a compute express link protocol;

[0035] the transmitting the target clock signal corresponding to the target control signal to the switch chip and the target device includes: transmitting the homologous clock signal to the switch chip and the target device in response to receiving the first control signal, and transmitting the non-homologous clock signal to the switch chip and the target device in response to receiving the second control signal.

[0036] In an exemplary embodiment, a reference clock generator of the clock generators of the plurality of clock types is configured to generate a plurality of clock signals,

and the receiving clock signals transmitted by clock generators of a plurality of clock types includes:

[0037] buffering the plurality of clock signals;

[0038] collecting signal parameters of the plurality of clock signals;

[0039] determining signal quality of each of the plurality of clock signals based on the signal parameters; and

[0040] determining a reference clock signal with the highest signal quality as a clock signal transmitted by the reference clock generator.

[0041] In an exemplary embodiment, the collecting signal parameters of the plurality of clock signals includes:

[0042] sampling the plurality of clock signals to obtain a plurality of sampling signals; and

[0043] calculating the signal parameters of the plurality of sampling signals, the signal parameter of each of the sampling signals including at least one of an amplitude parameter, a frequency parameter, a slope parameter and a jitter parameter.

[0044] In an exemplary embodiment, the identifying a target device type of the plurality of device types, to which a target device belongs includes:

[0045] receiving the target device type sent by a processor connected to the clock control device.

[0046] According to still another embodiment of the present application, a clock control apparatus for a switch chip is provided. The apparatus includes:

[0047] a receiving module configured to receive clock signals transmitted by clock generators of a plurality of clock types. A clock control device is connected to a switch chip, the switch chip uses clock signals of different clock types in response to controlling target devices belonging to different device types, and the plurality of clock types correspond to a plurality of device types;

[0048] an identification module configured to identify a target device type of the plurality of device types, to which the target device belongs; and

[0049] a transmission module configured to transmit, to the switch chip and the target device, a target clock signal transmitted by a target clock generator of the clock generators of the plurality of clock types. The target clock generator is a clock generator of a target clock type corresponding to the target device type.

[0050] According to still another embodiment of the present application, a non-volatile readable storage medium storing a computer program therein is also provided. The computer program is configured to perform the steps in any one of the above method embodiments in response to being executed.

[0051] According to still another embodiment of the present application, an electronic device is also provided, including a memory and a processor. A computer program is stored in the memory, and the processor is configured to run the computer program to perform the steps in any one of the above method embodiments.

[0052] Through the present application, the clock controller controls the clock selector according to the target device type of the target device to transmit, to the switch chip and the target device, the target clock signal transmitted by the target clock generator of the clock generators of the plurality of clock types. That is, since the switch chip is required to correspond to the clock type of the target device, the target device type of the target device is obtained through the clock controller, and then the clock controller controls the clock selector according to the target device type to select and transmit the target clock signal to the switch chip and the target device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0053] FIG. **1** is a schematic diagram I of a clock control device for a switch chip according to an embodiment of the present application;

[0054] FIG. **2** is a schematic diagram Il of a clock control device for a switch chip according to an embodiment of the present application;

[0055] FIG. **3** is a schematic diagram Ill of a clock control device for a switch chip according to an embodiment of the present application;

[0056] FIG. **4** is a schematic diagram IV of a clock control device for a switch chip according to an embodiment of the present application;

[0057] FIG. **5** is a schematic diagram V of a clock control device for a switch chip according to an embodiment of the present application;

[0058] FIG. **6** is a schematic diagram VI of a clock control device for a switch chip according to an embodiment of the present application;

[0059] FIG. **7** is a schematic diagram VII of a clock control device for a switch chip according to an embodiment of the present application;

[0060] FIG. **8** is a schematic diagram of a switch board according to an embodiment of the present application;

[0061] FIG. **9** is a schematic diagram of a working process of a switch board according to an embodiment of the present application;

[0062] FIG. **10** is a schematic diagram of a motherboard on which a clock generator is deployed according to an embodiment of the present application;

[0063] FIG. **11** is a schematic diagram of a device board on which a target device is deployed according to an embodiment of the present application;

[0064] FIG. **12** is a schematic diagram of a clock control system for a switch chip according to an embodiment of the present application;

[0065] FIG. **13** is a schematic diagram of a clock control process in a clock control system for a switch chip according to an embodiment of the present application;

[0066] FIG. **14** is a block diagram of a hardware structure of a mobile terminal of a clock control method for a switch chip according to an embodiment of the present application;

[0067] FIG. **15** is a flow chart of clock control for a switch chip according to an embodiment of the present application;

[0068] FIG. **16** is a schematic diagram of a clock control process in a clock control system for a switch chip according to an embodiment of the present application;

[0069] FIG. **17** is a block diagram of a structure of a clock control apparatus for a switch chip according to an embodiment of the present application; and

[0070] FIG. **18** is a schematic diagram of an electronic device according to an embodiment of the present application.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0071] Embodiments of the present application will be described in detail with reference to the drawings and in combination with the embodiments hereinafter.

[0072] It should be noted that the terms "first", "second", and the like in the description, the claims, and the drawings of the present application and the above drawings are used to distinguish between similar objects, and are not necessarily used to describe a specific sequence or sequential order.

[0073] A clock control device for a switch chip is provided in this embodiment. FIG. **1** is a schematic diagram I of a clock control device for a switch chip according to an embodiment of the present application. As shown in FIG. **1**, the clock control device for a switch chip may include a clock controller **102** and a clock selector **104**. The clock controller **102** is connected to the clock selector **104**, the clock selector **104** is allowed to be connected to clock generators (**106-1** to **106-***n*) of a plurality of clock types, a switch chip **108**, and a target device **110**, the switch chip **108** uses clock signals of different clock types in response to controlling target devices **110** belonging to different device types, and the plurality of clock types correspond to a plurality of device types; the clock controller **102** is configured to identify a target device type of the plurality of device types, to which the target device **110** belongs, and control the clock selector **104** to transmit, to the switch chip **108** and the target device **110**, a target clock signal transmitted by a target clock generator of the clock generators of the plurality of clock types. The target clock generator is a clock generator of a target clock type corresponding to the target device **110** type.

[0074] Through the above device, the clock controller controls the clock selector according to the target device type of the target device to transmit, to the switch chip and the target device, the target clock signal transmitted by the target clock generator of the clock generators of the plurality of clock types, enabling the switch chip to automatically use a corresponding clock type when controlling target devices of different device types. That is, since the switch chip is required to correspond to the clock type of the target device, the target device type of the target device is obtained through the clock controller, and then the clock controller controls the clock selector according to the target device type to select and transmit the target clock signal to the switch chip and the target device, so that the switch chip and the target device may receive the corresponding target clock signal. As such, the problem of low clock adaptation efficiency of the switch chip may be solved, improving the clock adaptation efficiency of the switch chip.

[0075] In one embodiment of this application, in this embodiment, the clock control device is configured to receive the clock signals transmitted by the clock generators of the plurality of clock types, select a clock signal corresponding to the target device from the plurality of clock signals, and transmit the clock signal to the switch chip and the target device, enabling the switch chip to use a corresponding clock type when controlling target devices of different device types.

[0076] In one embodiment of this application, in this embodiment, the clock control device may include the clock controller and the clock selector, but is not limited thereby, and functions of the clock control device may be, but are not limited thereby, implemented through a plurality of devices in the clock control device, such as obtaining the target device type of the plurality of device types, to which the target device belongs through the clock controller, and controlling the clock selector according to the target device type to transmit, to the switch chip and the target device, the target clock signal transmitted by the target clock generator of the clock generators of the plurality of clock types.

[0077] In one embodiment of this application, in this embodiment, the clock controller may, but is not limited thereby, control the clock selector to transmit, to the switch chip and the target device, the target clock signal transmitted by the target clock generator of the clock generators of the plurality of clock types by controlling the magnitude of an output level of the target control signal. For example, when the target control signal outputs a low level, the clock selector is instructed to select a homologous clock. Alternatively, when the target control signal outputs a high level, the clock selector is instructed to select a non-homologous clock.

[0078] In one embodiment of this application, in this embodiment, the clock generator may be, but is not limited to, a device capable of generating and transmitting a clock signal, such as an external crystal oscillator (XTAL), a crystal oscillator, etc. The clock type of the clock generator may include, but is not limited to, a homologous clock and a non-homologous clock.

[0079] In one embodiment of this application, in this embodiment, the clock generator may be, but is not limited to, a device capable of sending a plurality of clock signals at the same time. For example, the clock control device receives a plurality of clock signals sent by the same clock generator and a plurality of clock signals sent by another clock generator of a different clock type. Alternatively, the clock control device receives a plurality of clock signals sent by the same clock generator and a single clock signal sent by another clock generator of a different clock type.

[0080] In one embodiment of this application, in this embodiment, the switch chip may be, but is not limited to, a device with a function of controlling the target device, such as a CXL SW chip. The clock type used by the switch chip may be, but is not limited thereby, determined based on the device type of the target device. For example, when the target device type of the target device is a PCIe device, the clock type used by the switch chip is determined to be a homologous clock. Alternatively, if the target device type of the target device is a CXL device, the clock type used by the switch chip is determined to be a non-homologous clock.

[0081] In an exemplary embodiment, FIG. **2** is a schematic diagram II of a clock control device for a switch chip according to an embodiment of the present application. As shown in FIG. **2**, a first control port **202** is deployed on the clock controller **102**, and a plurality of clock ports (**204-1** to **204-***n*), a first output port **206**, a second output port **208** and a first signal port **210** are deployed on the clock selector **104**. The first control port **202** is connected to the first signal port **210**, the plurality of clock ports (**204-1** to **204-***n*) are configured to be connected to the clock generators (**106-1** to **106-***n*) of the plurality of clock types respectively, the first output port **206** is configured to be connected to the switch chip **108**, and the second output port **208** is configured to be connected to the target device **110**; the clock controller **102** is configured to generate a target control signal corresponding to the target device **110** type, and send the target control

signal to the clock selector **104** through the first control port **202**; the clock selector **104** is configured to receive the target control signal through the first signal port **210**, and transmit the target clock signal received on a target clock port **212** corresponding to the target control signal to the first output port **206** and the second output port **208**.

[0082] In one embodiment of this application, in this embodiment, a plurality of ports may be, but are not limited thereby, deployed on the clock controller. The clock controller may be, but is not limited thereby, connected to the clock selector through the first control port deployed thereon. The clock controller may send a signal to the clock selector through the first control port, the signal being used for controlling the clock selector to transmit, to the switch chip and the target device, the target clock signal transmitted by the target clock generator of the clock generators of the plurality of clock types.

[0083] In one embodiment of this application, in this embodiment, the plurality of ports that may be, but are not limited thereby, deployed on the clock selector include: the plurality of clock ports, the first output port, the second output port, the first signal port, etc.

[0084] In one embodiment of this application, in this embodiment, the plurality of clock ports deployed on the clock selector are connected to the clock generators of the plurality of clock types, and may be, but are not limited thereby, configured to receive clock signals sent by the clock generators of the plurality of clock types.

[0085] In one embodiment of this application, in this embodiment, the first output port deployed on the clock selector is connected to the switch chip, and may be, but is not limited thereby, configured to send the clock signal corresponding to the target device to the switch chip.

[0086] In one embodiment of this application, in this embodiment, the second output port deployed on the clock selector is connected to the target device, and may be, but is not limited thereby, configured to send the clock signal corresponding to the target device to the target device.

[0087] In one embodiment of this application, in this embodiment, the first control port deployed on the clock controller is connected to the clock selector, and may be, but is not limited thereby, configured to send the target control signal to the clock selector. For example, the clock controller generates the corresponding target control signal according to the target device type of the target device, and then transmits the target control signal to the clock selector through the first control port.

[0088] In one embodiment of this application, in this embodiment, the first signal port deployed on the clock selector is connected to the clock controller, and may be, but is not limited thereby, configured to receive the target control signal sent by the clock controller. For example, the clock controller transmits the target control signal through the first control port, and the clock selector receives the target control signal through the first signal port.

[0089] In an exemplary embodiment, FIG. **3** is a schematic diagram III of a clock control device for a switch chip according to an embodiment of the present application. As shown in FIG. **3**, the plurality of clock ports (**204-1** to **204-*n***) include a first clock port **302** and a second clock port **304**. The first clock port **302** is allowed to be connected to a first clock generator **306** of a homologous type, the second clock port **304** is allowed to be connected to a second clock generator **308** of a non-homologous type, the first clock generator **306** is configured to transmit a homologous clock signal, and the second clock generator **308** is configured to transmit a non-homologous clock signal; the clock controller **102** is configured to generate a first control signal when the target device **110** type is a first type which is a device type adopting a high-speed serial computer expansion bus standard, generate a second control signal when the target device **110** type is a second type which is a device type adopting a compute express link protocol, and send the first control signal or the second control signal to the clock selector **104** through the first control port **202**; the clock selector **104** is configured to transmit the homologous clock signal to the first output port **206** and the second output port **208** when receiving the first control signal, and transmit the non-homologous clock signal to the first output port **206** and the second output port **208** when receiving the second control signal.

[0090] In one embodiment of this application, in this embodiment, the plurality of clock ports of the clock controller are configured to be connected to the clock generators of the plurality of clock types. The clock ports may include, but are not limited to, the first clock port and the second clock port. The first clock port and the second clock port are connected to clock generators of different clock types.

[0091] In one embodiment of this application, in this embodiment, the first clock generator is connected to the clock controller through the first clock port, and the first clock port is configured to receive the homologous clock signal sent by the first clock generator.

[0092] In one embodiment of this application, in this embodiment, the second clock generator is connected to the clock controller through the second clock port, and the second clock port is configured to receive the non-homologous clock signal sent by the second clock generator.

[0093] In one embodiment of this application, in this embodiment, the first control signal is used for transmitting the homologous clock signal to the first output port and the second output port, and the second control signal is used for transmitting the non-homologous clock signal to the first output port and the second output port. For example, the target control signal corresponding to the target device type is generated by the clock controller in the clock control device, and the first output port and the second output port are deployed on the clock selector in the clock control device. In this case, the clock selector transmits the homologous clock signal to the first output port and the second output port when receiving the first control signal; and the clock selector transmits the non-homologous clock signal to the first output port and the second output port when receiving the second control signal.

[0094] In an exemplary embodiment, FIG. **4** is a schematic diagram IV of a clock control device for a switch chip according to an embodiment of the present application. As shown in FIG. **4**, a device type port **402** is deployed on the clock controller **102**. The device type port **402** is allowed to be connected to a processor **404**, and the device type port **402** is configured to receive the target device type sent by the processor **404**.

[0095] In one embodiment of this application, in this embodiment, the processor may be, but is not limited thereby, deployed on a motherboard connected to the clock control device. The processor may, but is not limited thereby, read the target device type of the target device through a bus. For example, the processor reads the target device in a PCIe

slot or CXL slot through a PCIe bus, and sends the target device type of the target device to the clock control device.

[0096] In one embodiment of this application, in this embodiment, the device type port is deployed on the clock controller. The device type port may be, but is not limited to, configured to be connected to the processor deployed on the motherboard. The target device type sent by the processor of the motherboard is received through the device type port.

[0097] In one embodiment of this application, in this embodiment, the clock control device may, but is not limited thereby, determine the target device type of the target device based on data received from the processor. For example, 0x50 and 0x56 indicate that the target device type is a PCIe device. In this case, when the clock control device receives 0x50 and 0x56 continuously, it may be determined that the target device type of the plurality of device types, to which the target device belongs is a PCIe device. Alternatively, for example, 0x27 and 0x29 indicate that the target device type is a CXL device. In this case, when the clock control device receives 0x27 and 0x29 continuously, it may be determined that the target device type of the plurality of device types, to which the target device belongs is a CXL device.

[0098] In one embodiment of this application, in this embodiment, the processor on the motherboard may be, but is not limited thereby, configured to obtain the target device type of the target device. For example, the processor on the motherboard is coupled to the target device through a set of PCIe x16 high-speed cables, and identifies the target device type of the target device through the PCIe x16 high-speed cables. The processor then sends the target device type of the target device to the clock controller through an I2C_CPU signal.

[0099] In an exemplary embodiment, FIG. **5** is a schematic diagram V of a clock control device for a switch chip according to an embodiment of the present application. As shown in FIG. **5**, the clock control device further includes a clock buffer **502**. The clock controller **102** is connected to the clock buffer **502**, and the clock buffer **502** is also connected between the clock selector **104** and a reference clock generator **504** of the clock generators (**106-1** to **106-*n***) of the plurality of clock types; the reference clock generator **504** is configured to generate a plurality of clock signals; the clock buffer **502** is configured to buffer the plurality of clock signals; the clock controller **102** is configured to collect signal parameters of the plurality of clock signals, determine signal quality of each of the plurality of clock signals based on the signal parameters, and control the clock buffer **502** to transmit a reference clock signal with the highest signal quality to the clock selector **104**.

[0100] In one embodiment of this application, in this embodiment, the plurality of clock signals may be, but are not limited thereby, buffered by the clock buffer in the clock control device. For example, when the clock controller receives, from the motherboard, the clock signals transmitted by the clock generators of the plurality of clock types, the plurality of clock signals transmitted by the motherboard may be buffered by the clock buffer.

[0101] In one embodiment of this application, in this embodiment, the signal parameters of the plurality of clock signals may be, but are not limited thereby, obtained by the clock controller performing calculation for the plurality of clock signals buffered in the clock buffer. For example, the clock controller first samples the plurality of clock signals buffered in the clock buffer, to obtain sampling signals, and then calculates the signal parameters of the sampling signals.

[0102] In one embodiment of this application, in this embodiment, the signal parameters are used to indicate signal quality of the clock signal, and the signal parameters may include, but are not limited to, amplitude, frequency, slope and jitter parameters of the clock signal, etc.

[0103] In one embodiment of this application, in this embodiment, the clock controller may, but is not limited thereby, select a clock signal with the best signal quality based on the signal parameters and determine the clock signal as the reference clock signal. For example, the clock controller calculates an average of the signal parameters of each clock signal, and determines a clock signal with a maximum average as the clock signal with the best signal quality, i.e., the reference clock signal. Alternatively, the clock controller calculates a weighted average of the signal parameters of each clock signal, and determines a clock signal with a maximum weighted average as the clock signal with the best signal quality, i.e., the reference clock signal.

[0104] In an exemplary embodiment, FIG. **6** is a schematic diagram VI of a clock control device for a switch chip according to an embodiment of the present application. As shown in FIG. **6**, a second control port **602** is deployed on the clock controller **102**, and a plurality of reference clock ports (**604-1** to **604-*n***), a third output port **606** and a second signal port **608** are deployed on the clock buffer **502**. The second control port **602** is connected to the second signal port **608**, the plurality of reference clock ports (**604-1** to **604-*n***) are configured to be connected to the reference clock generator **504**, and the third output port **606** is configured to be connected to the clock selector **104**; the clock controller **102** is configured to generate a reference control signal corresponding to the reference clock signal, and send the reference control signal to the clock buffer **502** through the second control port **602**; the clock buffer **502** is configured to receive the reference control signal through the second signal port **608**, and transmit the reference clock signal corresponding to the reference control signal to the third output port **606**.

[0105] In one embodiment of this application, in this embodiment, the second control port deployed on the clock controller may be, but is not limited thereby, connected to the second signal port of the clock buffer, and the second signal port may be, but is not limited thereby, configured to sample the plurality of clock signals to obtain a plurality of sampling signals.

[0106] In one embodiment of this application, in this embodiment, the reference clock port deployed on the clock buffer may be, but is not limited thereby, connected to the reference clock generator, and the reference clock port may be, but is not limited thereby, configured to receive the clock signal sent by the reference clock generator and perform a buffer operation.

[0107] In one embodiment of this application, in this embodiment, the third output port deployed on the clock buffer may be, but is not limited thereby, connected to the clock selector, the clock signal corresponding to the reference control signal may be, but is not limited thereby, determined based on the reference control signal sent by the clock controller, and the reference control signal is transmitted to the clock selector through the third output port.

[0108] In an exemplary embodiment, FIG. **7** is a schematic diagram VII of a clock control device for a switch chip according to an embodiment of the present application. As shown in FIG. **7**, the clock control device further includes a signal collector **702**. The signal collector **702** is connected between the reference clock generator **504** and the clock controller **102**; the signal collector **702** is configured to sample the plurality of clock signals to obtain a plurality of sampling signals, and transmit the plurality of sampling signals to the clock controller **102**; the clock controller **102** is configured to calculate the signal parameters of the plurality of sampling signals, the signal parameter of each of the sampling signals including at least one of an amplitude parameter, a frequency parameter, a slope parameter and a jitter parameter, and convert the signal parameter of each of the sampling signals into the signal quality of each of the sampling signals.

[0109] In one embodiment of this application, in this embodiment, the signal collector is configured to sample each clock signal during a process of the clock generator sending the clock signal to the clock buffer, so as to obtain the plurality of sampling signals.

[0110] In one embodiment of this application, in this embodiment, the signal collector may, but is not limited thereby, determine signals of the plurality of clock signals in the same time period as the sampling signals. For example, a plurality of clock signals in the same time period are captured and determined to be the sampling signals.

[0111] In one embodiment of this application, in this embodiment, the signal parameters of the sampling signal are used to indicate the signal quality of the sampling signal. For example, the signal quality of the sampling signal may be, but is not limited thereby, determined based on an average of the amplitude parameter, the frequency parameter, the slope parameter and the jitter parameter. Alternatively, the signal quality of the sampling signal may be, but is not limited thereby, determined based on a weighted average of the amplitude parameter, the frequency parameter, the slope parameter and the jitter parameter.

[0112] According to another aspect of the embodiments of the present application, a switch board is also provided. Since the switch board is configured to implement the above embodiment and embodiments, the description is no longer repeated here.

[0113] FIG. **8** is a schematic diagram of a switch board according to an embodiment of the present application. As shown in FIG. **8**, the switch board may include a switch chip **802** and a clock control device **804**. The clock control device **804** is connected to the switch chip **802**, and the clock control device **804** is allowed to be connected to a target device **806** and clock generators (**808-1** to **808-*n***) of a plurality of clock types; the switch chip **802** uses clock signals of different clock types when controlling target devices **806** belonging to different device types, and the plurality of clock types correspond to a plurality of device types; the clock control device **804** is configured to identify a target device type of the plurality of device types, to which the target device **806** belongs, and transmit, to the switch chip **802** and the target device **806**, a target clock signal transmitted by a target clock generator of the clock generators (**808-1** to **808-*n***) of the plurality of clock types. The target clock generator is a clock generator of a target clock type corresponding to the target device type.

[0114] Through the above switch board, the clock controller controls the clock selector according to the target device type of the target device to transmit, to the switch chip and the target device, the target clock signal transmitted by the target clock generator of the clock generators of the plurality of clock types, enabling the switch chip to automatically use a corresponding clock type when controlling target devices of different device types. That is, since the switch chip is required to correspond to the clock type of the target device, the target device type of the target device is obtained through the clock controller, and then the clock controller controls the clock selector according to the target device type to select and transmit the target clock signal to the switch chip and the target device, so that the switch chip and the target device may receive the corresponding target clock signal. As such, the problem of low clock adaptation efficiency of the switch chip may be solved, improving the clock adaptation efficiency of the switch chip.

[0115] In an exemplary embodiment, the clock control device includes a clock controller and a clock selector. The clock controller is connected to the clock selector, and the clock selector is allowed to be connected to the clock generators of the plurality of clock types, the switch chip and the target device; the clock controller is configured to generate a target control signal corresponding to the target device type, and send the target control signal to the clock selector; the clock selector is configured to receive the target control signal, and transmit the target clock signal corresponding to the target control signal to the switch chip and the target device.

[0116] In one embodiment of this application, in this embodiment, the clock generators of the plurality of clock types may be, but are not limited thereby, deployed on the switch board. For example, a plurality of clock generators are deployed on the switch board. Alternatively, the clock generators of the plurality of clock types may be, but are not limited thereby, deployed on a device connected to the switch board. For example, the clock generators of the plurality of clock types are deployed on a motherboard connected to the switch board.

[0117] In one embodiment of this application, in this embodiment, the clock controller and the clock selector may be, but are not limited thereby, deployed on the switch board, and the clock controller may, but is not limited thereby, generate the target control signal based on the target device type and then send the target control signal to the clock selector, to control the clock selector to select and transmit the target clock signal to the switch chip and the target device.

[0118] In an exemplary embodiment, the clock generators of the plurality of clock types include a first clock generator of a homologous type and a second clock generator of a non-homologous type. The clock selector is connected to each of the first clock generator and the second clock generator, the first clock generator is configured to transmit a homologous clock signal, and the second clock generator is configured to transmit a non-homologous clock signal; the clock controller is configured to generate a first control signal when the target device type is a first type which is a device type adopting a high-speed serial computer expansion bus standard, generate a second control signal when the target device type is a second type which is a device type adopting a compute express link protocol, and send the first control signal or the second control signal to the clock

selector; the clock selector is configured to transmit the homologous clock signal to the switch chip and the target device when receiving the first control signal, and transmit the non-homologous clock signal to the switch chip and the target device when receiving the second control signal.

[0119] In an exemplary embodiment, a reference clock generator of the clock generators of the plurality of clock types is allowed to generate a plurality of clock signals. The clock control device is configured to buffer the plurality of clock signals, collect signal parameters of the plurality of clock signals, determine signal quality of each of the plurality of clock signals based on the signal parameters, and determine a reference clock signal with the highest signal quality as a clock signal corresponding to the reference clock generator.

[0120] In one embodiment of this application, in this embodiment, the reference clock generator may generate a plurality of clock signals. For example, the clock control device is connected to the clock generators of the plurality of types, including, but not limited to, a homologous clock generator and a non-homologous clock generator. When the reference clock generator is a homologous clock generator, the homologous clock generator is allowed to generate a plurality of clock signals. Alternatively, when the reference clock generator is a non-homologous clock generator, the non-homologous clock generator is allowed to generate a plurality of clock signals.

[0121] In an exemplary embodiment, the clock control device includes a clock controller, a clock selector and a clock buffer. The clock controller is connected to the clock selector, the clock selector is allowed to be connected to the clock generators of the plurality of clock types, the switch chip and the target device, and the clock buffer is connected between the reference clock generator and the clock selector; the clock controller is configured to generate a reference control signal corresponding to the reference clock signal, send the reference control signal to the clock buffer, generate a target control signal corresponding to the target device type, send the target control signal to the clock selector; the clock buffer is configured to receive the reference control signal, and transmit the reference clock signal corresponding to the reference control signal to the clock selector; the clock selector is configured to receive the target control signal, and transmit the target clock signal corresponding to the target control signal to the switch chip and the target device.

[0122] In one embodiment of this application, in this embodiment, the clock buffer is connected between the reference clock generator and the clock selector, and the clock buffer is configured to buffer the clock signal sent by the reference clock generator to the clock selector. The clock buffer may, but is not limited thereby, determine, based on the reference control signal corresponding to the target device type indicated by the clock controller, the clock signal sent to the clock selector.

[0123] In one embodiment of this application, in this embodiment, the clock controller may be, but is not limited thereby, configured to control the clock buffer to send the reference clock signal to the clock selector. The clock controller is further configured to control the clock selector to send the target clock signal to the switch chip and the target device. For example, the clock controller receives the target device type of the target device and generates the reference control signal and the target control signal based on the target device type. The clock controller sends the reference control signal to the clock buffer, to control the clock buffer to transmit the reference clock signal to the clock selector. The clock controller sends the target control signal to the clock selector, to control the clock selector to transmit the target clock signal to the switch chip and the target device.

[0124] In an exemplary embodiment, the clock control device is further configured to sample the plurality of clock signals to obtain a plurality of sampling signals, calculate the signal parameters of the plurality of sampling signals, the signal parameter of each of the sampling signals including at least one of an amplitude parameter, a frequency parameter, a slope parameter and a jitter parameter, and convert the signal parameter of each of the sampling signals into the signal quality of each of the sampling signals.

[0125] In an exemplary embodiment, the clock control device is allowed to be connected to a processor. The clock control device is configured to receive the target device type sent by the processor.

[0126] In an exemplary embodiment, the switch board further includes an uplink connector, a downlink connector and a third clock generator. The third clock generator is connected to the clock control device, the clock control device is connected to a fourth clock generator of the processor through the uplink connector, and the clock generators of the plurality of clock types include the third clock generator and the fourth clock generator; the clock control device is connected to the target device through the downlink connector.

[0127] In one embodiment of this application, in this embodiment, the clock control device may be, but is not limited thereby, connected to the clock generators including the third clock generator and the fourth clock generator. The third clock generator may be directly connected to the clock control device, and the fourth clock generator of the processor that is not deployed on the switch board may be, but is not limited thereby, connected to the clock control device through the uplink connector of the switch board.

[0128] In one embodiment of this application, in this embodiment, the downlink connector of the switch board is configured to be connected to the target device, and device information of the target device may be, but is not limited thereby, obtained through the downlink connector. For example, information such as the manufacturer, capacity, speed, etc. of the target device may be obtained through the downlink connector.

[0129] In an exemplary embodiment, a switch board is provided, including a switch chip, a clock control device, a third clock generator, an uplink connector and a downlink connector. FIG. **9** is a schematic diagram of a working process of a switch board according to an embodiment of the present application. As shown in FIG. **9**, the switch chip is a CXL SW chip, the clock control device includes a clock controller, a clock selector and a clock buffer. In one embodiment of this application, the clock controller is a complex programmable logic device (CPLD) control unit, and the clock selector is CLK MUX, the clock buffer is CLK Buffer, the third clock generator is CLK Generator, the uplink connector is an uplink-port compact duplex form factor pluggable module (CDFP) connector, and the downlink connector is a downlink-port CDFP connector. For example, a first clock generator configured to transmit a homologous clock signal is deployed on a motherboard, and the third clock generator CLK Generator is configured to

transmit a non-homologous clock signal. In this case, the switch board may work in the following mode:

[0130] For example, the third clock generator CLK Generator includes a 25 MHz clock crystal XTAL. In this case, the XTAL provides an internal phase-locked loop (PLL) for the third clock generator, and accordingly, the third clock generator outputs a 100 MHz CLK_GEN clock signal.

[0131] The CPLD control unit reads information related to a target device of the downlink-port CDFP connector through I2C and PERST_N signals. For example, information such as the manufacturer, capacity, speed, etc. related to the target device is read through the I2C signal, and a reset operation, etc. is performed on the target device through the PERST_N signal.

[0132] The uplink-port CDFP connector is coupled to the downlink-port CDFP connector through a set of PCIe x16 high-speed cables. The uplink-port CDFP connector identifies a target device type of the target device through the PCIe x16 high-speed cables coupled to the downlink-port CDFP connector. A processor CPU of the uplink-port CDFP connector sends the target device type of the target device to the CPLD control unit through an I2C_CPU signal.

[0133] The uplink-port CDFP connector of the switch board is connected to the CDFP connector of the motherboard through a cable, to receive the homologous clock signal from the motherboard. An analog to digital converter (ADC) sampling unit (signal collector) samples a plurality of homologous clock signals from the motherboard, and transmits sampling signals to the CPLD control unit through a serial peripheral interface (SPI) bus. The CPLD control unit calculates signal parameters of the sampling signal: an amplitude parameter, a frequency parameter, a slope parameter, a jitter parameter, etc., and determines the homologous clock signal with the best signal quality based on the signal parameters.

[0134] For example, the homologous clock signals CLK_CDFP**1** and CLK_CDFP**2** sent by a clock generator (CLK_**1**) of the motherboard are received. In this case, the CPLD control unit controls the clock buffer CLK Buffer through a CLK_S signal to select and output the homologous clock signal with the best signal quality. For example, when the CLK_S outputs a low level, it indicates that the CLK_CDFP**1** has the best signal quality, and the clock buffer CLK Buffer outputs the CLK_CDFP**1** to CLK_BUF; and when the CLK_S outputs a high level, it indicates that the CLK_CDFP**2** has the best signal quality, and the CLK Buffer outputs the CLK_CDFP**2** to the CLK_BUF.

[0135] Under the control by a CLK_MODE signal sent by the CPLD control unit, the CLK MUX selects a corresponding clock for the target device interconnected with the downlink-port CDFP connector and the CXL SW in the following manner:

[0136] For example, when the CLK_MODE outputs a low level, the CLK MUX is instructed to select a homologous clock CLK_BUF. In this case, IN_**1** of the CLK MUX outputs the homologous clock CLK_BUF to each of MUX_OUT**1** and MUX_OUT**2**, and then the homologous clock CLK_BUF is input to the CXL SW through CLK_CXL and input to the target device interconnected with the downlink-port CDFP connector through CLK_CDFP, so that clocks of the target device interconnected with the downlink-port CDFP connector and the CXL SW are both homologous clocks.

[0137] For example, when the CLK_MODE outputs a high level, the CLK MUX is instructed to select a non-homologous clock CLK_GEN. In this case, IN_**2** outputs the non-homologous clock CLK_GEN to each of the MUX_OUT**1** and MUX_OUT**2**, and then the non-homologous clock CLK_GEN is input to the CXL SW through CLK_CXL and input to the target device interconnected with the downlink-port CDFP connector through the CLK_CDFP, so that clocks of the target device interconnected with the downlink-port CDFP connector and the CXL SW are both non-homologous clocks. I2C is Inter-Integrated Circuit. I2C_CPU is the specific I2C interface designated for communication with the CPU. CLK stands for clock. CLK_S is the clock select signal. CLK_BUF is the clock buffer circuit. CLK_GEN is the clock generator. IN represents input. CLK_MODE stands for clock mode. MUX_OUT is the multiplexer output. CLK_CXL is the clock for Compute Express Link. RST_N is reset not. PERST_N is power-on reset not. CLK_IN is the clock input.

[0138] In an exemplary embodiment, the clock control device is connected to the motherboard on which the clock generator is deployed. FIG. **10** is a schematic diagram of a motherboard on which a clock generator is deployed according to an embodiment of the present application. As shown in FIG. **10**, the motherboard includes: the XTAL (a 25 MHz clock crystal), the clock generator CLK Generator, the processor CPU, the CDFP connector. The motherboard may send a clock signal to the clock control device through the following method. The clock crystal XTAL provides an internal PLL for the clock generator CLK Generator, thereby outputting a 100 MHz PCIe clock. The CLK Generator outputs a 25 MHz CLK_CPU clock to the CPU through an output end CLK_OUTO. The CPU is connected to the PCIe device of the CDFP connector through a set of PCIe x16 high-speed cables and connected to the I2C device of the CDFP connector through I2C. The CLK Generator outputs the 100 MHz homologous clock signal CLK_CDFP**1** to a CLK_CDFP_OUT**1** port of the CDFP connector through an output end CLK_OUT**1**, and outputs the 100 MHz homologous clock signal CLK_CDFP**2** to a CLK_CDFP_OUT**2** port of the CDFP connector through an output end CLK_OUT**2**. The CDFP connector is configured to be connected to the switch chip deployed on the switch board.

[0139] The motherboard may send the target device type to the clock controller through the following method: the CPU is connected to the clock controller of the switch board through an I2C bus, and sends the target device type (which may include, but is not limited to, a PCIe device and a CXL device) of the target device to the CPLD control unit through the I2C_CPU signal.

[0140] In an exemplary embodiment, a device board on which a target device is deployed is provided. FIG. **11** is a schematic diagram of a device board on which a target device is deployed according to an embodiment of the present application. As shown in FIG. **11**, the device board includes: a CDFP connector, a PCIe slot or CXL slot (PCIe/CXL slot), and a PCIe device or CXL device (PCIe/CXL device). The PCIe device or CXL device is provided with an electrically erasable programmable read-only memory (EEPROM), and the EEPROM is configured to store information such as the manufacturer, capacity, speed, etc. The CDFP connector obtains the information stored in the EEPROM through an I2C port. The CDFP connector performs a reset operation on the PCIe device or CXL device

through RST_N (which may be, but is not limited thereby, configured to indicate a reset signal). The CDFP connector is connected to CLK_IN through CLK_OUT, to transmit a clock signal. The CDFP connector reads the device deployed in the slot through PCIe. The device board may send a target device type to a clock control device of a switch board in the following manner:

[0141] After the device board is powered on, a processor CPU of a motherboard automatically identifies the target device in the PCIe slot or CXL slot through a PCIe bus, and sends the target device type to a clock controller CPLD of the switch board through an I2C_CPU bus. When the clock controller CPLD receives signals such as 0x50, 0x56, etc. continuously, the target device type of the target device may be, but is not limited thereby, considered to be the PCIe device; and when the clock controller CPLD receives signals such as 0x27, 0x29, etc. continuously, the target device type of the target device may be, but is not limited thereby, considered to be the CXL device.

[0142] According to still another aspect of the embodiments of the present application, a clock control system for a switch chip is also provided. Since the switch board is configured to implement the above embodiment and embodiments, the description is no longer repeated here.

[0143] FIG. **12** is a schematic diagram of a clock control system for a switch chip according to an embodiment of the present application. As shown in FIG. **12**, the clock control system for a switch chip may include a switch board **1202** and a device board **1204**. A switch chip **1206** and a clock control device **1208** are deployed on the switch board **1202**, and a device interface **1210** is deployed on the device board **1204**; the device interface **1210** is configured to be connected to a target device **1212**. The switch chip **1206** uses clock signals of different clock types when controlling target devices **1212** belonging to different device types, and the plurality of clock types correspond to a plurality of device types; the clock control device **1208** is configured to identify a target device type of the plurality of device types, to which the target device **1212** belongs, and transmit, to the switch chip **1206** and the target device **1212**, a target clock signal transmitted by a target clock generator **1216** of the clock generators (**1214-1** to **1214-*n***) of the plurality of clock types. The target clock generator is a clock generator of a target clock type corresponding to the target device type.

[0144] Through the above system, the clock controller controls the clock selector according to the target device type of the target device to transmit, to the switch chip and the target device, the target clock signal transmitted by the target clock generator of the clock generators of the plurality of clock types, enabling the switch chip to automatically use a corresponding clock type when controlling target devices of different device types. That is, since the switch chip is required to correspond to the clock type of the target device, the target device type of the target device is obtained through the clock controller, and then the clock controller controls the clock selector according to the target device type to select and transmit the target clock signal to the switch chip and the target device, so that the switch chip and the target device may receive the corresponding target clock signal. As such, the problem of low clock adaptation efficiency of the switch chip may be solved, improving the clock adaptation efficiency of the switch chip.

[0145] In an exemplary embodiment, a first control port is deployed on the clock controller, and a plurality of clock ports, a first output port, a second output port and a first signal port are deployed on the clock selector. The first control port is connected to the first signal port, the plurality of clock ports are configured to be connected to the clock generators of the plurality of clock types respectively, the first output port is configured to be connected to the switch chip, and the second output port is configured to be connected to the target device; the clock controller is configured to generate a target control signal corresponding to the target device type, and send the target control signal to the clock selector through the first control port; the clock selector is configured to receive the target control signal through the first signal port, and transmit the target clock signal received on a target clock port corresponding to the target control signal to the first output port and the second output port.

[0146] In an exemplary embodiment, the system further includes a motherboard. A third clock generator is deployed on the switch board, a fourth clock generator of a processor is deployed on the motherboard, and the clock control device includes a clock controller and a clock selector; the clock controller is connected to the clock selector, the clock selector is connected to the third clock generator, the fourth clock generator, the switch chip and the target device, the third clock generator is configured to transmit a non-homologous clock signal, and the fourth clock generator is configured to transmit a homologous clock signal; the clock controller is configured to generate a first control signal when the target device type is a first type which is a device type adopting a high-speed serial computer expansion bus standard, generate a second control signal when the target device type is a second type which is a device type adopting a compute express link protocol, and send the first control signal or the second control signal to the clock selector; the clock selector is configured to transmit the homologous clock signal to the switch chip and the target device when receiving the first control signal, and transmit the non-homologous clock signal to the switch chip and the target device when receiving the second control signal.

[0147] In one embodiment of this application, in this embodiment, the motherboard may include the clock generator, but is not limited thereby. The clock generator of the motherboard may, but is not limited thereby, provide a clock signal in the following manner: the XTAL provides the internal PLL for the CLK generator, thereby outputting the 100 MHz PCIe clock.

[0148] In one embodiment of this application, in this embodiment, the motherboard may include the clock generator and the processor, but is not limited thereby. The processor of the motherboard may, but is not limited thereby, obtain the target device type of the target device in the following manner: the CPU is connected to the clock controller of the switch board through the I2C bus, and sends the target device type (which may include, but is not limited to, a PCIe device and a CXL device) of the target device to the CPLD control unit through the I2C_CPU signal.

[0149] In an exemplary embodiment, the fourth clock generator is allowed to generate a plurality of clock signals, and the clock control device further includes a clock buffer. The clock buffer is connected between the fourth clock generator and the clock selector; the clock controller is configured to collect signal parameters of the plurality of clock signals, determine signal quality of each of the plurality of clock signals based on the signal parameters, determine a reference clock signal with the highest signal

quality as a clock signal corresponding to the fourth clock generator, generate a reference control signal corresponding to the reference clock signal, and send the reference control signal to the clock buffer; the clock buffer is configured to buffer the plurality of clock signals, receive the reference control signal, and transmit the reference clock signal corresponding to the reference control signal to the clock selector.

[0150] In an exemplary embodiment, a second control port is deployed on the clock controller, and a plurality of reference clock ports, a third output port and a second signal port are deployed on the clock buffer. The second control port is connected to the second signal port, the plurality of reference clock ports are configured to be connected to the reference clock generator, and the third output port is configured to be connected to the clock selector; the clock controller is configured to generate a reference control signal corresponding to the reference clock signal, and send the reference control signal to the clock buffer through the second control port; the clock buffer is configured to receive the reference control signal through the second signal port, and transmit the reference clock signal corresponding to the reference control signal to the third output port.

[0151] In an exemplary embodiment, the clock control device further includes a signal collector. The signal collector is connected between the reference clock generator and the clock controller; the signal collector is configured to sample the plurality of clock signals to obtain a plurality of sampling signals, and transmit the plurality of sampling signals to the clock controller; the clock controller is configured to calculate signal parameters of the plurality of sampling signals, the signal parameter of each of the sampling signals including at least one of an amplitude parameter, a frequency parameter, a slope parameter and a jitter parameter, and convert the signal parameter of each of the sampling signals into the signal quality of each of the sampling signals.

[0152] In an exemplary embodiment, the processor is deployed on the motherboard, and the clock control device is connected to the processor. The processor is connected to the target device through the switch board and the device board; the processor is configured to output the target device type of the target device during training of the target device, send the target device type to the clock control device; the clock control device is configured to receive the target device type sent by the processor.

[0153] In an exemplary embodiment, a clock control system for a switch chip is provided. FIG. **13** is a schematic diagram of a clock control process in a clock control system for a switch chip according to an embodiment of the present application. As shown in FIG. **13**, the clock control system for a switch chip includes a motherboard, a switch board and a device board. The motherboard includes a clock generator and a processor CPU deployed on the motherboard, and the clock generator of the motherboard is configured to provide a clock signal for the CPU and send a first clock signal to the switch board.

[0154] The switch board includes a clock buffer, a clock controller, a clock selector, a clock generator deployed on the switch board, and a switch chip CXL SW. The clock buffer, the clock controller and the clock selector are configured to parse a clock signal with highest quality from the first clock signals sent by the clock generator of the motherboard; the clock controller is further configured to parse a target device (which may be, but is not limited to, a CXL device or PCIe device) deployed on the device board and output a control signal to the clock buffer; the clock generator of the switch board is configured to output a second clock signal to the clock selector. The first clock signal and the second clock signal are of different types; the clock selector outputs a homologous clock or non-homologous clock to the CXL SW and the device board under the control of the control signal sent by the clock controller; the CXL device or PCIe device is deployed on the device board.

[0155] For example, the first clock signal is a homologous clock signal, and the second clock signal is a non-homologous clock signal. In this case, the clock control system for a switch chip may work in the following mode:

[0156] The clock generator of the motherboard sends a plurality of homologous clock signals to the processor of the motherboard and the clock buffer of the switch board, and the clock buffer of the switch board buffers each homologous clock signal.

[0157] In the process of the clock generator of the motherboard sending the homologous clock signals to the clock buffer of the switch board, the clock controller of the switch board samples the homologous clock signals sent by the clock generator of the motherboard, and performs analysis to determine an optimal homologous clock signal in the plurality of homologous clock signals sent by the clock generator of the motherboard. The clock controller sends a reference control signal to the clock buffer, to control the clock buffer to transmit the optimal homologous clock signal to the clock selector.

[0158] The clock generator of the switch board transmits a non-homologous clock signal to the clock selector.

[0159] The clock controller sends a corresponding control signal (first control signal or second control signal) to the clock selector according to a target device type (CXL device or PCIe device) of the target device deployed on the device board, to control the clock selector to select a clock signal corresponding to the target device type from the homologous clock signal and the non-homologous clock signal.

[0160] The clock selector transmits the clock signal corresponding to the target device type to the CXL SW and the target device according to the control signal sent by the clock controller.

[0161] The clock signal of CXL SW and the PCIe device may be, but is not limited thereby, determined to be a homologous clock when sourced from the clock generator of the motherboard; and the clock signal of CXL SW and the CXL device may be, but is not limited thereby, determined to be a non-homologous clock when sourced from the clock generator of the switch board.

[0162] A method embodiment provided in the embodiments of the present application can be executed on a mobile terminal, a computer terminal, or a similar computing apparatus. For example, the method embodiment is executed on a mobile terminal. FIG. **14** is a block diagram of a hardware structure of a mobile terminal of a clock control method for a switch chip according to an embodiment of the present application. As shown in FIG. **14**, the mobile terminal may include one or more (only one is shown in FIG. **14**) processors **1402** (the processor **1402** may include, but is not limited to, a processing apparatus such as a microprocessor MCU or a programmable logic device FPGA) and a memory **1404** configured to store data. The mobile terminal may further include a transmission device **1406** configured for a

communication function and an input/output device **1408**. Those of ordinary skill in the art may understand that the structure shown in FIG. **14** is merely illustrative, and does not limit the structure of the mobile terminal. For example, the mobile terminal may further include more or fewer components than those shown in FIG. **14**, or have a configuration different from that shown in FIG. **14**.

[0163] The memory **1404** may be configured to store computer programs, such as a software program and a module of application software, and a computer program corresponding to the clock control method for a switch chip in this embodiment of the present application. The processor **1402** runs the computer programs stored in the memory **1404**, to execute various functional applications and data processing, i.e., implement the above method. The memory **1404** may include a high-speed random access memory, and may further include a non-volatile memory, such as one or more magnetic storage apparatuses, a flash memory, or other non-volatile solid-state memories. In some examples, the memory **1404** may include a memory configured remotely relative to the processor **1402**, and these remote memories may be connected to the mobile terminal through a network. Examples of the network include, but are not limited to, the Internet, an intranet, a local area network, a mobile communication network and combinations thereof.

[0164] The transmission device **1406** is configured to receive or send data via a network. Examples of the network may include a wireless network provided by a communication provider of the mobile terminal. In an example, the transmission device **1406** includes a network interface controller (NIC), which can be connected to other network devices through a base station so as to communicate with the Internet. In an example, the transmission device **1406** may be a radio frequency (RF) module, which is configured to wirelessly communicate with the Internet.

[0165] In this embodiment, a clock control method for a switch chip to be run on the above mobile terminal is provided. FIG. **15** is a flow chart of clock control for a switch chip according to an embodiment of the present application. As shown in FIG. **15**, the process includes the following steps:

[0166] at step S**1502**, clock signals transmitted by clock generators of a plurality of clock types are received. A clock control device is connected to a switch chip, the switch chip uses clock signals of different clock types when controlling target devices belonging to different device types, and the plurality of clock types correspond to a plurality of device types;

[0167] at step S**1504**, a target device type of the plurality of device types, to which a target device belongs is identified; and

[0168] at step S**1506**, a target clock signal transmitted by a target clock generator of the clock generators of the plurality of clock types is transmitted to the switch chip and the target device. The target clock generator is a clock generator of a target clock type corresponding to the target device type.

[0169] Through the above steps, a clock controller controls a clock selector according to the target device type of the target device to transmit, to the switch chip and the target device, the target clock signal transmitted by the target clock generator of the clock generators of the plurality of clock types, enabling the switch chip to automatically use a corresponding clock type when controlling target devices of different device types. That is, since the switch chip is required to correspond to the clock type of the target device, the target device type of the target device is obtained through the clock controller, and then the clock controller controls the clock selector according to the target device type to select and transmit the target clock signal to the switch chip and the target device, so that the switch chip and the target device may receive the corresponding target clock signal. As such, the problem of low clock adaptation efficiency of the switch chip may be solved, improving the clock adaptation efficiency of the switch chip.

[0170] The execution subject of the above steps may be the clock control device. The clock control device may include the clock controller and the clock selector, but is not limited thereby; may, but is not limited thereby, identify the target device type of the plurality of device types, to which the target device belongs through the clock controller; and may, but is not limited thereby, transmit, to the switch chip and the target device through the clock selector, the target clock signal transmitted by the target clock generator of the target clock type corresponding to the target device type.

[0171] In the technical solution provided by step S**1502**, the clock generator may be, but is not limited to, a device capable of generating and transmitting a clock signal, such as an external crystal oscillator (XTAL), a crystal oscillator, etc. The clock type of the clock generator may include, but is not limited to, a homologous clock and a non-homologous clock.

[0172] In one embodiment of this application, in this embodiment, the clock generator may be, but is not limited to, a device capable of sending a plurality of clock signals at the same time. For example, the clock control device receives a plurality of clock signals sent by the same clock generator and a plurality of clock signals sent by another clock generator of a different clock type. Alternatively, the clock control device receives a plurality of clock signals sent by the same clock generator and a single clock signal sent by another clock generator of a different clock type.

[0173] In one embodiment of this application, in this embodiment, the target device may be, but is not limited to, a device of one of the plurality of device types, such as an RC, a switch, an endpoint, etc. of a device type adopting a high-speed serial computer expansion bus standard. Alternatively, the target device may be a CXL accelerator card, a CXL switch, etc. of a device type adopting a compute express link protocol.

[0174] In one embodiment of this application, in this embodiment, the switch chip may be, but is not limited to, a device with a function of controlling the target device, such as a CXL SW chip. The clock type used by the switch chip may be, but is not limited thereby, determined based on the device type of the target device. For example, when the target device type of the target device is a PCIe device, the clock type used by the switch chip is determined to be a homologous clock. Alternatively, if the target device type of the target device is a CXL device, the clock type used by the switch chip is determined to be a non-homologous clock.

[0175] In the technical solution provided by step S**1504**, the target device type may be, but is not limited thereby, transmitted to the clock control device by a processor on a motherboard. For example, when the clock control device is started, the processor deployed on the motherboard automatically identifies the target device in a PCIe slot or CXL

slot through a PCIe bus, and notifies the clock control device of the identified target device type through an I2C_CPU bus.

[0176] In an embodiment, the target device type of the plurality of device types, to which the target device belongs may be, but is not limited thereby, identified in the following manner of: receiving the target device type sent by the processor connected to the clock control device.

[0177] In one embodiment of this application, in this embodiment, the processor may be, but is not limited thereby, deployed on the motherboard connected to the clock control device. The processor may, but is not limited thereby, read the target device type of the target device through a bus. For example, the processor reads the target device in the PCIe slot or CXL slot through the PCIe bus, and sends the target device type of the target device to the clock control device.

[0178] In one embodiment of this application, in this embodiment, the clock control device may be, but is not limited thereby, configured to receive the target device type, and the clock control device may, but is not limited thereby, select, from the clock signals transmitted by the clock generators of the plurality of clock types, the clock signal corresponding to the target device type according to the target device type.

[0179] In one embodiment of this application, in this embodiment, the clock control device may, but is not limited thereby, determine the target device type of the target device based on data received from the processor. For example, 0x50 and 0x56 indicate that the target device type is a PCIe device. In this case, when the clock control device receives 0x50 and 0x56 continuously, it may be determined that the target device type of the plurality of device types, to which the target device belongs is a PCIe device. Alternatively, for example, 0x27 and 0x29 indicate that the target device type is a CXL device. In this case, when the clock control device receives 0x27 and 0x29 continuously, it may be determined that the target device type of the plurality of device types, to which the target device belongs is a CXL device.

[0180] In the technical solution provided by step **S1506**, the target clock type may be, but is not limited thereby, determined from the plurality of clock types based on the target device type of the target device. For example, the clock type required by the switch chip and the target device is determined to be a homologous clock based on the target device type of the target device. Alternatively, the clock type required by the switch chip and the target device is determined to be a non-homologous clock based on the target device type of the target device.

[0181] In one embodiment of this application, in this embodiment, the clock generator sending the target clock type may be, but is not limited thereby, determined to be the target clock generator. For example, two clock generators of the homologous clock type and two clock generators of the non-homologous clock type send a plurality of clock signals at the same time. In this case, when the clock type required by the switch chip and the target device is determined to be a homologous clock based on the target device type of the target device, the two clock generators of the homologous clock type may be, but are not limited thereby, determined to be the target clock generators. Alternatively, the better of the two clock generators of the homologous clock type is selected and determined to be the target clock generator.

[0182] In an embodiment, the target clock signal transmitted by the target clock generator of the clock generators of the plurality of clock types may be, but is not limited thereby, transmitted to the switch chip and the target device in the following manner: generating a target control signal corresponding to the target device type; and transmitting the target clock signal corresponding to the target control signal to the switch chip and the target device.

[0183] In one embodiment of this application, in this embodiment, the target control signal is used to instruct the clock control device to select the target clock signal transmitted by the target clock generator of the clock generators of the plurality of clock types for transmission. For example, a clock generator A of the homologous clock type sends a clock signal A and a clock signal B, and a clock generator B of the non-homologous clock type sends a clock signal C and a clock signal D. In this case, when the target control signal indicates that the switch chip and the target device require a clock signal of the homologous clock type, the clock generator A sending the clock signal A and the clock signal B may be, but is not limited thereby, determined to be the target clock generator, and a clock signal may be, but is not limited thereby, selected from the clock signal A and the clock signal B and determined to be the target clock signal for transmission.

[0184] In one embodiment of this application, in this embodiment, the clock control device may include the clock controller and the clock selector, but is not limited thereby, the target control signal corresponding to the target device type may be, but is not limited thereby, generated by the clock controller, and the target clock signal corresponding to the target control signal may be, but is not limited thereby, transmitted to the switch chip and the target device by the clock selector. For example, the clock controller generates the target control signal according to the target device type of the target device and transmits the target control signal to the clock selector. The clock selector selects the target clock signal from all the clock signals according to the target control signal for transmission. Alternatively, the clock controller generates the target control signal according to the target device type of the target device and transmits the target control signal to the clock selector. The clock selector screens out first clock signals of a clock type indicated by the target control signal, and then selects the target clock signal from the first clock signals for transmission.

[0185] In one embodiment of this application, in this embodiment, the clock controller may, but is not limited thereby, instruct the clock selector to select the corresponding target clock signal by controlling the magnitude of an output level of the target control signal. For example, when the target control signal outputs a low level, the clock selector is instructed to select a homologous clock. Alternatively, when the target control signal outputs a high level, the clock selector is instructed to select a non-homologous clock.

[0186] In one embodiment of this application, in this embodiment, the target control signal may be, but is not limited thereby, received through a first signal port of the clock selector; and the target clock signal received on a target clock port corresponding to the target control signal is transmitted to a first output port and a second output port.

[0187] In an embodiment, the clock generators of the plurality of clock types include a first clock generator of a homologous type and a second clock generator of a non-homologous type. The first clock generator is configured to transmit a homologous clock signal, and the second clock

generator is configured to transmit a non-homologous clock signal. Generating the target control signal corresponding to the target device type includes: generating a first control signal when the target device type is a first type which is a device type adopting a high-speed serial computer expansion bus standard, and generating a second control signal when the target device type is a second type which is a device type adopting a compute express link protocol. Transmitting the target clock signal corresponding to the target control signal to the switch chip and the target device includes: transmitting the homologous clock signal to the switch chip and the target device when the first control signal is received, and transmitting the non-homologous clock signal to the switch chip and the target device when the second control signal is received.

[0188] In one embodiment of this application, in this embodiment, the first control signal is used for transmitting the homologous clock signal to the first output port and the second output port, and the second control signal is used for transmitting the non-homologous clock signal to the first output port and the second output port. For example, the target control signal corresponding to the target device type is generated by the clock controller in the clock control device, and the first output port and the second output port are deployed on the clock selector in the clock control device. In this case, the clock selector transmits the homologous clock signal to the first output port and the second output port when receiving the first control signal; and the clock selector transmits the non-homologous clock signal to the first output port and the second output port when receiving the second control signal.

[0189] In one embodiment of this application, in this embodiment, the first output port and the second output port may be, but are not limited thereby, configured to transmit a clock signal to the switch chip and the target device. For example, the first output port is connected to the switch chip, and the second output port is connected to the target device. In this case, the clock signal is transmitted to the switch chip and the target device through the first output port and the second output port.

[0190] In one embodiment of this application, in this embodiment, a plurality of clock ports, the first output port, the second output port and the first signal port may be, but are not limited thereby, deployed on the clock selector. The first clock port is allowed to be connected to the first clock generator of the homologous type, the second clock port is allowed to be connected to the second clock generator of the non-homologous type, the first clock generator is configured to transmit the homologous clock signal, and the second clock generator is configured to transmit the non-homologous clock signal.

[0191] In an embodiment, a reference clock generator of the clock generators of the plurality of clock types is configured to generate a plurality of clock signals. Clock signals transmitted by the clock generators of the plurality of clock types may be, but are not limited thereby, received in the following manner: buffering the plurality of clock signals; collecting signal parameters of the plurality of clock signals; determining signal quality of each of the plurality of clock signals based on the signal parameters; and determining a reference clock signal with the highest signal quality as a clock signal transmitted by the reference clock generator.

[0192] In one embodiment of this application, in this embodiment, the plurality of clock signals may be, but are not limited thereby, buffered by the clock buffer in the clock control device. For example, when the clock controller receives, from the motherboard, the clock signals transmitted by the clock generators of the plurality of clock types, the plurality of clock signals transmitted by the motherboard may be buffered by the clock buffer.

[0193] In one embodiment of this application, in this embodiment, the signal parameters of the plurality of clock signals may be, but are not limited thereby, obtained by performing calculation for the plurality of clock signals buffered in the clock buffer. For example, first, the plurality of clock signals buffered in the clock buffer are sampled, to obtain sampling signals, and then signal parameters of the sampling signals are calculated.

[0194] In one embodiment of this application, in this embodiment, the signal parameters are used to indicate signal quality of the clock signal, and the signal parameters may include, but are not limited to, amplitude, frequency, slope and jitter parameters of the clock signal, etc.

[0195] In one embodiment of this application, in this embodiment, the reference clock signal may be, but is not limited thereby, determined by selecting a clock signal with the best signal quality based on the signal parameters. For example, an average of the signal parameters of each clock signal is calculated, and a clock signal with a maximum average is determined to be the clock signal with the best signal quality, i.e., the reference clock signal. Alternatively, a weighted average of the signal parameters of each clock signal is calculated, and a clock signal with a maximum weighted average is determined to be the clock signal with the best signal quality, i.e., the reference clock signal.

[0196] In one embodiment of this application, in this embodiment, a second control port is deployed on the clock controller, and a plurality of reference clock ports, a third output port and a second signal port are deployed on the clock buffer. The second control port is connected to the second signal port, the plurality of reference clock ports are configured to be connected to the reference clock generator, and the third output port is configured to be connected to the clock selector; the clock controller is configured to generate a reference control signal corresponding to the reference clock signal, and send the reference control signal to the clock buffer through the second control port; the clock buffer is configured to receive the reference control signal through the second signal port, and transmit the reference clock signal corresponding to the reference control signal to the third output port.

[0197] In an embodiment, the signal parameters of the plurality of clock signals may be, but are not limited thereby, collected in the following manner: sampling the plurality of clock signals to obtain a plurality of sampling signals; and calculating signal parameters of the plurality of sampling signals. The signal parameter of each of the sampling signals includes at least one of an amplitude parameter, a frequency parameter, a slope parameter and a jitter parameter.

[0198] In one embodiment of this application, in this embodiment, signals of the plurality of clock signals in the same time period may be, but are not limited thereby, determined to be the sampling signals. For example, a plurality of clock signals in the same time period are captured and determined to be the sampling signals.

[0199] In one embodiment of this application, in this embodiment, the signal parameters of the sampling signal are used to indicate the signal quality of the sampling signal. For example, the signal quality of the sampling signal may be, but is not limited thereby, determined based on an average of the amplitude parameter, the frequency parameter, the slope parameter and the jitter parameter. Alternatively, the signal quality of the sampling signal may be, but is not limited thereby, determined based on a weighted average of the amplitude parameter, the frequency parameter, the slope parameter and the jitter parameter.

[0200] In one embodiment of this application, in this embodiment, the clock control device further includes a signal collector. The signal collector is connected between the reference clock generator and the clock controller; the signal collector is configured to sample the plurality of clock signals to obtain a plurality of sampling signals, and transmit the plurality of sampling signals to the clock controller.

[0201] In an exemplary embodiment, a clock control system for a switch chip is provided. FIG. **16** is a schematic diagram of a clock control process in a clock control system for a switch chip according to an embodiment of the present application. As shown in FIG. **16**, the clock control process may, but is not limited thereby, include the following steps:

[0202] at step S**1602**, a user plugs a PCIe device or CXL device into a slot of a device board, and powers on the entire clock control system for the switch chip;

[0203] at step S**1604**, during the process of training a target device by a processor, the processor CPU of a motherboard reads a target device type of the target device in the slot of the device board;

[0204] at step S**1606**, after reading the target device type, the processor sends the target device type to a clock controller CPLD of the switch board through an I2C bus;

[0205] at step S**1608**, the clock controller CPLD parses the target device type;

[0206] and when the target device is the CXL device (when received data is 0x27 and 0x29, the clock controller may, but is not limited thereby, perform parsing to obtain the target device, which is the CXL device), step S**1610** to step S**1618** are performed:

[0207] at step S**1610**, the clock controller CPLD outputs a high-level CXL_MODE signal (i.e., target control signal);

[0208] at step S**1612**, a clock selector CLK_MUX outputs IN_**2** to MUX_OUT**1** and MUX_OUT**2**, the MUX_OUT**1** performs output to the switch chip CXL SW, and the MUX_OUT**2** performs output to the CXL device;

[0209] at step S**1614**, the clock controller CPLD pulls up a PERST_N signal (i.e., reference clock signal);

[0210] at step S**1616**, the switch chip CXL SW and the CXL device obtain a non-homologous clock; and

[0211] at step S**1618**, clock configuration is completed.

[0212] When the target device is the PCIe device (when received data is 0x50 and 0x56, the clock controller may, but is not limited thereby, perform parsing to obtain the target device, which is the PCIe device), step S**1620** to step S**1632** are performed:

[0213] at step S**1620**, the clock controller CPLD starts an ADC sampling unit through an SPI bus, so as to read a sampling signal;

[0214] at step S**1622**, the clock controller CPLD calculates signal parameters of the sampling signal, and selects a reference clock signal with highest signal quality;

[0215] at step S**1624**, the clock controller CPLD outputs a low-level CXL_MODE signal (i.e., target control signal);

[0216] at step S**1626**, the clock selector CLK MUX outputs IN_**1** to the MUX_OUT**1** and MUX_OUT**2**, the MUX_OUT**1** performs output to the switch chip CXL SW, and the MUX_OUT**2** performs output to the PCIe device;

[0217] at step S**1628**, the clock controller CPLD pulls up the PERST_N signal (i.e., reference clock signal);

[0218] at step S**1630**, the switch chip CXL SW and the PCIe device obtain a homologous clock; and

[0219] at step S**1632**, clock configuration is completed.

[0220] Through the above description of the embodiments, those skilled in the art could clearly learn that the method in the above embodiments may be implemented with software and a necessary general-purpose hardware platform or with hardware, while in many cases the former is a preferable implementation. Based on such an understanding, the essence or a portion contributing to the related technologies of the technical solutions of the present application may be embodied in the form of a software products. The computer software product is stored in a storage medium (such as a ROM/RAM, a diskette, or an optical disk), and includes several instructions used to enable a terminal apparatus (which may be a cell phone, a computer, a server, a network device, etc.) to execute the method of each embodiment of the present application.

[0221] This embodiment further provides a clock control apparatus for a switch chip. The apparatus is configured to implement the above embodiments and embodiments, and the description is no longer repeated here. As used hereinafter, the term "module" may be a combination of software and/or hardware that implements a preset function. Although the apparatus described in the following embodiment is implemented in software, an implementation in hardware or a combination of software and hardware is possible and conceivable.

[0222] FIG. **17** is a block diagram of a structure of a clock control apparatus for a switch chip according to an embodiment of the present application. As shown in FIG. **17**, the apparatus includes:

[0223] a receiving module **1702** configured to receive clock signals transmitted by clock generators of a plurality of clock types. A clock control device is connected to the switch chip, the switch chip uses clock signals of different clock types when controlling target devices belonging to different device types, and the plurality of clock types correspond to a plurality of device types;

[0224] an identification module **1704** configured to identify a target device type of the plurality of device types, to which the target device belongs; and

[0225] a transmission module **1706** configured to transmit, to the switch chip and the target device, a target clock signal transmitted by a target clock generator of the clock generators of the plurality of clock types. The target clock generator is a clock generator of a target clock type corresponding to the target device type.

[0226] Through the above apparatus, a clock controller controls a clock selector according to the target device type of the target device to transmit, to the switch chip and the target device, the target clock signal transmitted by the target clock generator of the clock generators of the plurality of clock types, enabling the switch chip to automatically use a corresponding clock type when controlling target devices of different device types. That is, since the switch chip is required to correspond to the clock type of the target device, the target device type of the target device is obtained through the clock controller, and then the clock controller controls the clock selector according to the target device type to select and transmit the target clock signal to the switch chip and the target device, so that the switch chip and the target device may receive the corresponding target clock signal. As such, the problem of low clock adaptation efficiency of the switch chip may be solved, improving the clock adaptation efficiency of the switch chip.

[0227] In an exemplary embodiment, the transmission module is configured to:

[0228] generate a target control signal corresponding to the target device type; and

[0229] transmit the target clock signal corresponding to the target control signal to the switch chip and the target device.

[0230] In an exemplary embodiment, the transmission module is further configured to:

[0231] when generating the target control signal corresponding to the target device type, generate a first control signal when the target device type is a first type which is a device type adopting a high-speed serial computer expansion bus standard, and generate a second control signal when the target device type is a second type which is a device type adopting a compute express link protocol; and

[0232] when transmitting the target clock signal corresponding to the target control signal to the switch chip and the target device, transmit the homologous clock signal to the switch chip and the target device when the first control signal is received, and transmit the non-homologous clock signal to the switch chip and the target device when the second control signal is received.

[0233] In an exemplary embodiment, the transmission module is further configured to:

[0234] buffer the plurality of clock signals;

[0235] collect signal parameters of the plurality of clock signals;

[0236] determine signal quality of each of the plurality of clock signals based on the signal parameters; and

[0237] determine a reference clock signal with the highest signal quality as a clock signal transmitted by the reference clock generator.

[0238] In an exemplary embodiment, the transmission module is further configured to:

[0239] sample the plurality of clock signals to obtain a plurality of sampling signals; and

[0240] calculate the signal parameters of the plurality of sampling signals, the signal parameter of each of the sampling signals including at least one of an amplitude parameter, a frequency parameter, a slope parameter and a jitter parameter.

[0241] In an exemplary embodiment, the identification module is further configured to:

[0242] receive the target device type sent by a processor connected to the clock control device.

[0243] It should be noted that each of the above modules may be realized by software or hardware. In the case of the hardware, the modules may be realized, but is not limited thereby, in the following way: all the modules are in the same processor; or the modules are separately in different processors in the form of any combinations.

[0244] An embodiment of the present application further provides a non-volatile readable storage medium storing a computer program therein. The computer program is configured to perform the steps in any of the above method embodiments when executed.

[0245] In an example embodiment, the non-volatile readable storage medium may include, but is not limited to various media that can store computer programs, such as a USB flash disk, a read-only memory (ROM), a random access memory (RAM), a mobile hard disk, a magnetic disk, or an optical disk.

[0246] An embodiment of the present application further provides an electronic device. FIG. **18** is a schematic diagram of an electronic device according to an embodiment of the present application. As shown in FIG. **18**, the electronic device includes a memory and a processor. The memory stores a computer program, and the processor is configured to run the computer program to perform the steps in any one of the above method embodiments.

[0247] In an exemplary embodiment, the electronic device may further include a transmission device and an input/output device The transmission device is connected to the processor, and the input/output device is connected to the processor.

[0248] Examples in this embodiment may refer to the examples described in the above embodiments and the exemplary embodiments, and are no longer repeated here in this embodiment.

[0249] Obviously, those skilled in the art should understand that the modules or steps of the present application may be implemented with a general-purpose computing device. The modules or steps may be centralized on a single computing device or distributed on a network consisting of a plurality of computing devices, may be implemented with program codes executable by the computing device, and thus may be stored in a storage device and executed by the computing device. Moreover, in some cases, the steps shown or described may be performed in an order different from the order here or may be separately produced as individual integrated circuit modules, or a plurality of the modules or steps may be produced as a single integrated circuit module. As such, the present application is not limited to any particular combination of hardware and software. The above embodiments are just embodiments of the present application and are not used for limiting the present application. For those skilled in the art, the present application may have various modifications and variations. Any modification, equivalent substitution, improvement and the like made within the principle of the present application shall all fall in the protection scope of the present application.

1. A clock control device for a switch chip, wherein the clock control device comprises a clock controller and a clock selector, wherein

the clock controller is connected to the clock selector, the clock selector is allowed to be connected to clock generators of a plurality of clock types, a switch chip, and a target device, the switch chip uses clock signals of different clock types in response to controlling target devices belonging to different device types, and the plurality of clock types correspond to a plurality of device types; and

the clock controller is configured to identify a target device type of the plurality of device types, to which the target device belongs, and control the clock selector to transmit, to the switch chip and the target device, a target clock signal transmitted by a target clock generator of the clock generators of the plurality of clock types, wherein the target clock generator is a clock generator of a target clock type corresponding to the target device type.

2. The device according to claim **1**, wherein a first control port is deployed on the clock controller, and a plurality of clock ports, a first output port, a second output port and a first signal port are deployed on the clock selector, wherein

the first control port is connected to the first signal port, the plurality of clock ports are configured to be connected to the clock generators of the plurality of clock types respectively, the first output port is configured to be connected to the switch chip, and the second output port is configured to be connected to the target device;

the clock controller is configured to generate a target control signal corresponding to the target device type, and send the target control signal to the clock selector through the first control port; and

the clock selector is configured to receive the target control signal through the first signal port, and transmit the target clock signal received on a target clock port corresponding to the target control signal to the first output port and the second output port.

3. The device according to claim **2**, wherein the plurality of clock ports comprise a first clock port and a second clock port, wherein

the first clock port is allowed to be connected to a first clock generator of a homologous type, the second clock port is allowed to be connected to a second clock generator of a non-homologous type, the first clock generator is configured to transmit a homologous clock signal, and the second clock generator is configured to transmit a non-homologous clock signal;

the clock controller is configured to generate a first control signal in response to the target device type being a first type which is a device type adopting a high-speed serial computer expansion bus standard, generate a second control signal in response to the target device type being a second type which is a device type adopting a compute express link protocol, and send the first control signal or the second control signal to the clock selector through the first control port; and

the clock selector is configured to transmit the homologous clock signal to the first output port and the second output port in response to receiving the first control signal, and transmit the non-homologous clock signal to the first output port and the second output port in response to receiving the second control signal.

4. The device according to claim **1**, wherein a device type port is deployed on the clock controller, and the device type port is allowed to be connected to a processor;

the device type port is configured to receive the target device type sent by the processor.

5. The device according to claim **1**, wherein the clock control device further comprises a clock buffer, wherein

the clock controller is connected to the clock buffer, and the clock buffer is also connected between the clock selector and a reference clock generator of the clock generators of the plurality of clock types;

the reference clock generator is configured to generate a plurality of clock signals;

the clock buffer is configured to buffer the plurality of clock signals; and

the clock controller is configured to collect signal parameters of the plurality of clock signals, determine signal quality of each of the plurality of clock signals based on the signal parameters, and control the clock buffer to transmit a reference clock signal with the highest signal quality to the clock selector.

6. The device according to claim **5**, wherein a second control port is deployed on the clock controller, and a plurality of reference clock ports, a third output port and a second signal port are deployed on the clock buffer, wherein

the second control port is connected to the second signal port, the plurality of reference clock ports are configured to be connected to the reference clock generator, and the third output port is configured to be connected to the clock selector;

the clock controller is configured to generate a reference control signal corresponding to the reference clock signal, and send the reference control signal to the clock buffer through the second control port; and

the clock buffer is configured to receive the reference control signal through the second signal port, and transmit the reference clock signal corresponding to the reference control signal to the third output port.

7. The device according to claim **5**, wherein the clock control device further comprises a signal collector, wherein

the signal collector is connected between the reference clock generator and the clock controller;

the signal collector is configured to sample the plurality of clock signals to obtain a plurality of sampling signals, and transmit the plurality of sampling signals to the clock controller; and

the clock controller is configured to calculate the signal parameters of the plurality of sampling signals, and convert the signal parameter of each of the sampling signals into the signal quality of each of the sampling signals, wherein the signal parameter of each of the sampling signals comprising at least one of an amplitude parameter, a frequency parameter, a slope parameter and a jitter parameter.

8. A switch board, comprising a switch chip and a clock control device, wherein

the clock control device is connected to the switch chip, and the clock control device is allowed to be connected to a target device and clock generators of a plurality of clock types;

the switch chip uses clock signals of different clock types in response to controlling target devices belonging to different device types, and the plurality of clock types correspond to a plurality of device types; and

the clock control device is configured to identify a target device type of the plurality of device types, to which the target device belongs, and transmit, to the switch

chip and the target device, a target clock signal transmitted by a target clock generator of the clock generators of the plurality of clock types, wherein the target clock generator is a clock generator of a target clock type corresponding to the target device type.

9. The switch board according to claim **8**, wherein the clock control device comprises a clock controller and a clock selector, wherein

the clock controller is connected to the clock selector, and the clock selector is allowed to be connected to the clock generators of the plurality of clock types, the switch chip and the target device;

the clock controller is configured to generate a target control signal corresponding to the target device type, and send the target control signal to the clock selector; and

the clock selector is configured to receive the target control signal, and transmit the target clock signal corresponding to the target control signal to the switch chip and the target device.

10. The switch board according to claim **9**, wherein the clock generators of the plurality of clock types comprise a first clock generator of a homologous type and a second clock generator of a non-homologous type;

the clock selector is connected to each of the first clock generator and the second clock generator, the first clock generator is configured to transmit a homologous clock signal, and the second clock generator is configured to transmit a non-homologous clock signal;

the clock controller is configured to generate a first control signal in response to the target device type being a first type which is a device type adopting a high-speed serial computer expansion bus standard, generate a second control signal in response to the target device type being a second type which is a device type adopting a compute express link protocol, and send the first control signal or the second control signal to the clock selector; and

the clock selector is configured to transmit the homologous clock signal to the switch chip and the target device in response to receiving the first control signal, and transmit the non-homologous clock signal to the switch chip and the target device in response to receiving the second control signal.

11. The switch board according to claim **8**, wherein a reference clock generator of the clock generators of the plurality of clock types is allowed to generate a plurality of clock signals, wherein

the clock control device is configured to buffer the plurality of clock signals, collect signal parameters of the plurality of clock signals, determine signal quality of each of the plurality of clock signals based on the signal parameters, and determine a reference clock signal with the highest signal quality as a clock signal corresponding to the reference clock generator.

12. The switch board according to claim **11**, wherein the clock control device comprises a clock controller, a clock selector and a clock buffer, wherein

the clock controller is connected to the clock selector, the clock selector is allowed to be connected to the clock generators of the plurality of clock types, the switch chip and the target device, and the clock buffer is connected between the reference clock generator and the clock selector;

the clock controller is configured to generate a reference control signal corresponding to the reference clock signal, send the reference control signal to the clock buffer, generate a target control signal corresponding to the target device type, and send the target control signal to the clock selector;

the clock buffer is configured to receive the reference control signal, and transmit the reference clock signal corresponding to the reference control signal to the clock selector; and

the clock selector is configured to receive the target control signal, and transmit the target clock signal corresponding to the target control signal to the switch chip and the target device.

13. The switch board according to claim **11**, wherein the clock control device is further configured to: sample the plurality of clock signals to obtain a plurality of sampling signals, calculate the signal parameters of the plurality of sampling signals, and convert the signal parameter of each of the sampling signals into the signal quality of each of the sampling signals, wherein the signal parameter of each of the sampling signals comprising at least one of an amplitude parameter, a frequency parameter, a slope parameter and a jitter parameter.

14. The switch board according to claim **8**, wherein the clock control device is allowed to be connected to a processor, wherein

the clock control device is configured to receive the target device type sent by the processor.

15. The switch board according to claim **8**, further comprising an uplink connector, a downlink connector and a third clock generator, wherein

the third clock generator is connected to the clock control device, the clock control device is connected to a fourth clock generator of a processor through the uplink connector, and the clock generators of the plurality of clock types comprise the third clock generator and the fourth clock generator; and

the clock control device is connected to the target device through the downlink connector.

16-19. (canceled)

20. A clock control method for a switch chip, wherein the method is applied to a clock control device, and comprises:

receiving clock signals transmitted by clock generators of a plurality of clock types, wherein the clock control device is connected to a switch chip, the switch chip uses clock signals of different clock types in response to controlling target devices belonging to different device types, and the plurality of clock types correspond to a plurality of device types;

identifying a target device type of the plurality of device types, to which a target device belongs; and

transmitting, to the switch chip and the target device, a target clock signal transmitted by a target clock generator of the clock generators of the plurality of clock types, wherein the target clock generator is a clock generator of a target clock type corresponding to the target device type.

21. The method according to claim **20**, wherein the transmitting, to the switch chip and the target device, a target clock signal transmitted by a target clock generator of the clock generators of the plurality of clock types comprises:

generating a target control signal corresponding to the target device type;

transmitting the target clock signal corresponding to the target control signal to the switch chip and the target device; or

the identifying a target device type of the plurality of device types comprises, to which the target device belongs:

receiving the target device type sent by a processor connected to the clock control device.

22. The method according to claim **21**, wherein the clock generators of the plurality of clock types comprise a first clock generator of a homologous type and a second clock generator of a non-homologous type, the first clock generator is configured to transmit a homologous clock signal, and the second clock generator is configured to transmit a non-homologous clock signal;

the generating a target control signal corresponding to the target device type comprises: generating a first control signal in response to the target device type being a first type which is a device type adopting a high-speed serial computer expansion bus standard, and generating a second control signal in response to the target device type being a second type which is a device type adopting a compute express link protocol;

the transmitting the target clock signal corresponding to the target control signal to the switch chip and the target device comprises: transmitting the homologous clock signal to the switch chip and the target device in response to receiving the first control signal, and transmitting the non-homologous clock signal to the switch chip and the target device in response to receiving the second control signal.

23. The method according to claim **21**, wherein a reference clock generator of the clock generators of the plurality of clock types is configured to generate a plurality of clock signals, wherein the receiving clock signals transmitted by clock generators of a plurality of clock types comprises:

buffering the plurality of clock signals;

collecting signal parameters of the plurality of clock signals;

determining signal quality of each of the plurality of clock signals based on the signal parameters; and

determining a reference clock signal with the highest signal quality as a clock signal transmitted by the reference clock generator.

24. The method according to claim **23**, wherein the collecting signal parameters of the plurality of clock signals comprises:

sampling the plurality of clock signals to obtain a plurality of sampling signals; and

calculating the signal parameters of the plurality of sampling signals, the signal parameter of each of the sampling signals comprising at least one of an amplitude parameter, a frequency parameter, a slope parameter and a jitter parameter.

25-28. (canceled)

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