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(54) **PHOTOELECTRIC CONVERSION APPARATUS**

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(57) **ABSTRACT**

A photoelectric conversion apparatus includes a semiconductor substrate having first and second principal surfaces, a microlens array, pixels each including a corresponding one microlens, photoelectric conversion units in rows and columns that is arranged inside the semiconductor substrate, and arranged in such a manner as to corresponding to the one microlens, and a first trench portion that separates photoelectric conversion units, and a second trench portion provided between neighboring two pixels, wherein, a first region between one first portion and other first portion and a second region between one second portion and other second portion each include a semiconductor region, and wherein, at a depth position between the first principal surface and the second principal surface, in the planar view, a part of the first trench portion is arranged at each of a position overlapping the first region and a position overlapping the second region.

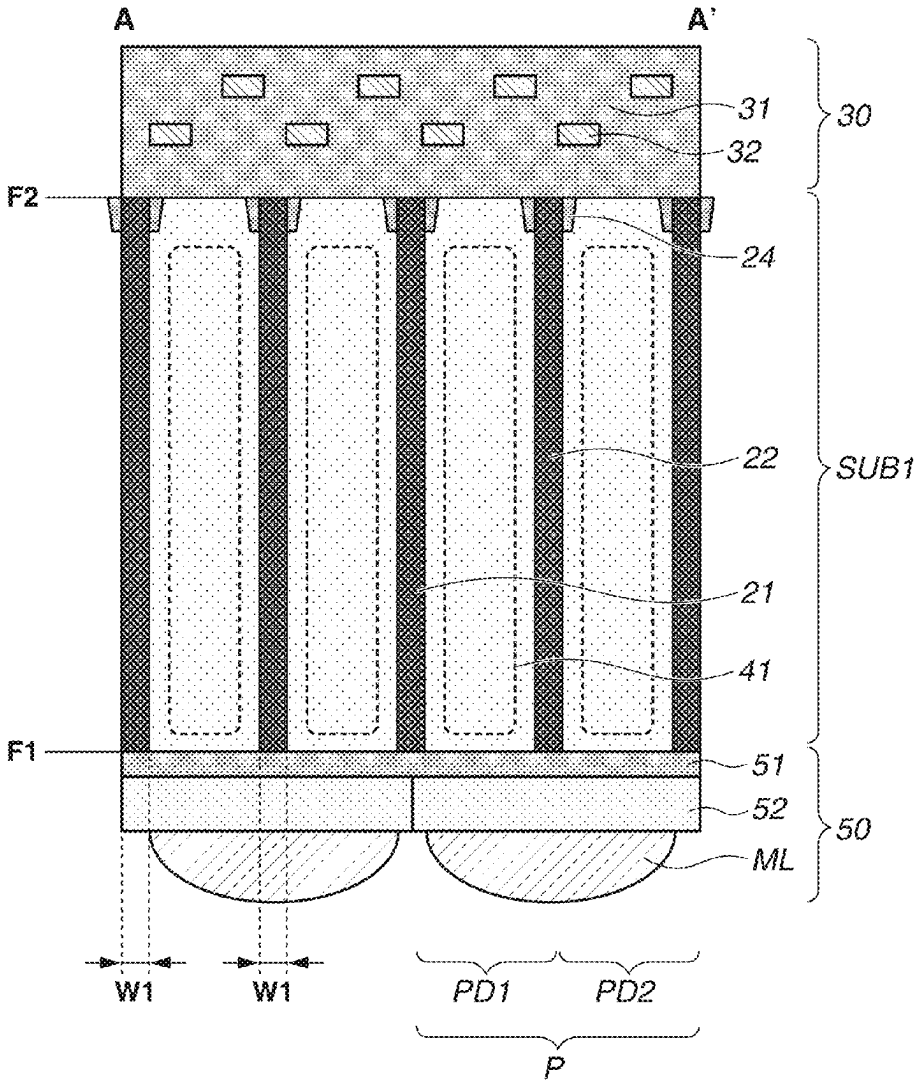


FIG.1

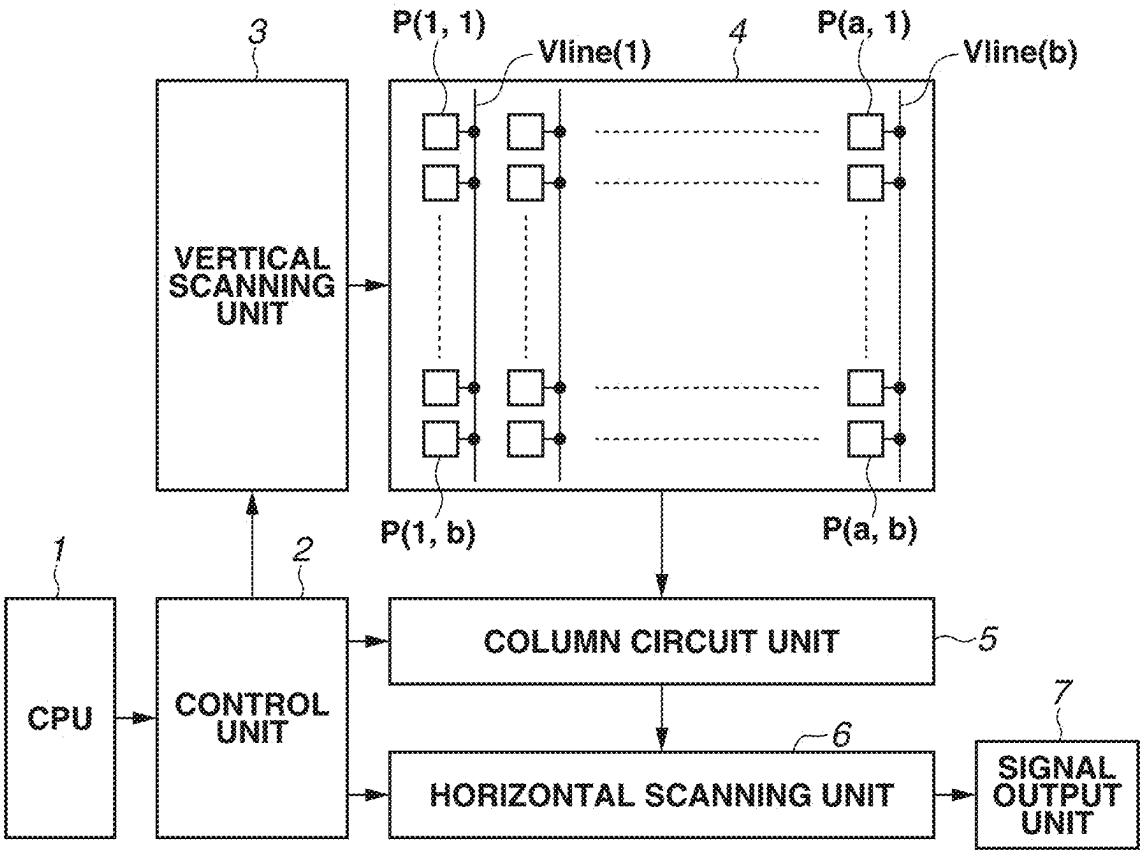

3
P(1, 1)
Vline(1)
4
P(a, 1)
Vline(b)
VERTICAL SCANNING UNIT
P(1, b)
P(a, b)
1
2
CPU
CONTROL UNIT
COLUMN CIRCUIT UNIT
5
6
7
HORIZONTAL SCANNING UNIT
SIGNAL OUTPUT UNIT

FIG.2

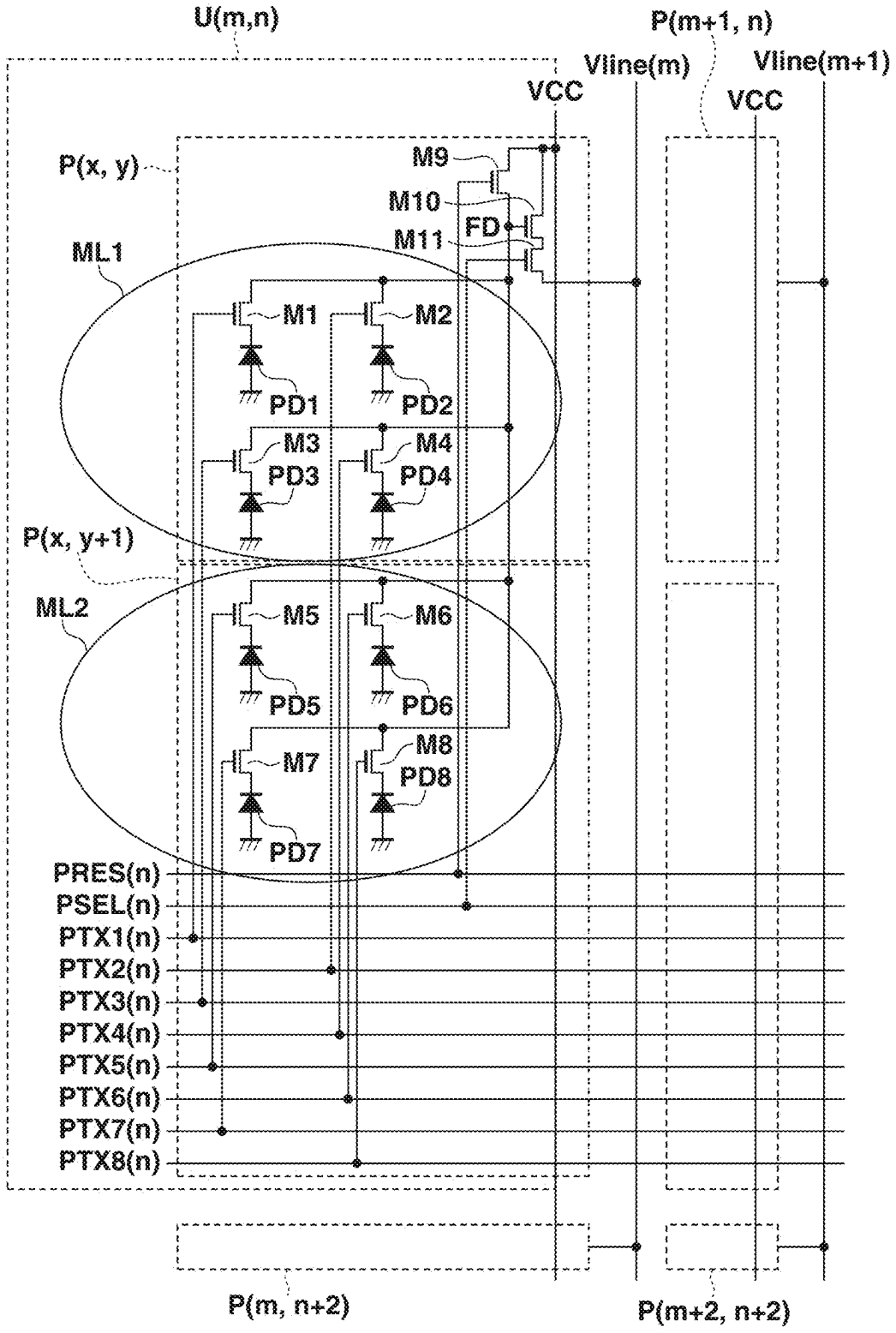

U(m,n)
P(m+1, n)
Vline(m)
Vline(m+1)
VCC
VCC
P(x, y)
M9
M10
M11
FD
ML1
M1
M2
PD1
PD2
M3
M4
PD3
PD4
P(x, y+1)
ML2
M5
M6
PD5
PD6
M7
M8
PD7
PD8
PRES(n)
PSEL(n)
PTX1(n)
PTX2(n)
PTX3(n)
PTX4(n)
PTX5(n)
PTX6(n)
PTX7(n)
PTX8(n)
P(m, n+2)
P(m+2, n+2)

FIG.3

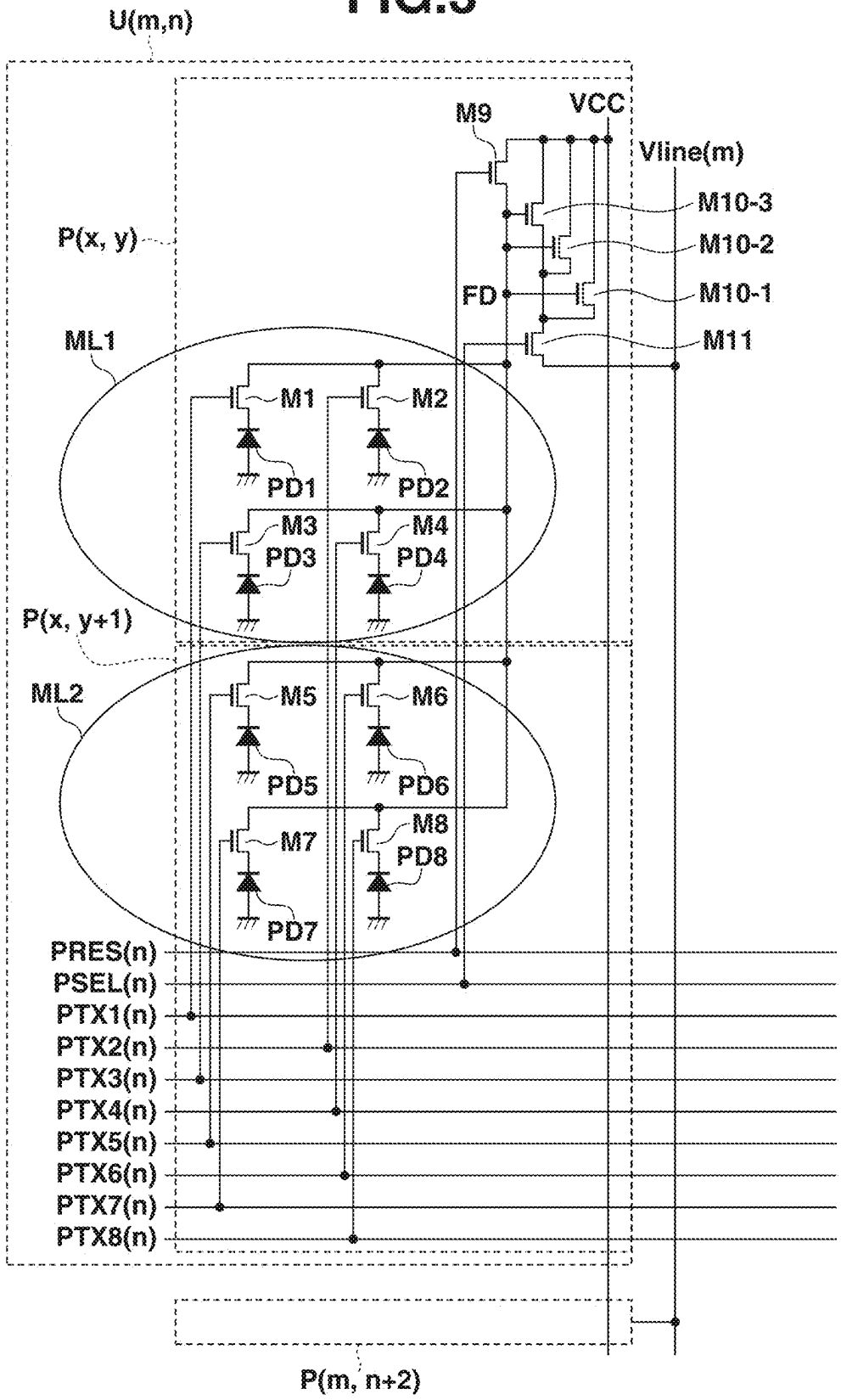

U(m,n)
M9
VCC
Vline(m)
M10-3
M10-2
M10-1
M11
FD
P(x, y)
ML1
M1
M2
PD1
PD2
M3
M4
PD3
PD4
P(x, y+1)
ML2
M5
M6
PD5
PD6
M7
M8
PD7
PD8
PRES(n)
PSEL(n)
PTX1(n)
PTX2(n)
PTX3(n)
PTX4(n)
PTX5(n)
PTX6(n)
PTX7(n)
PTX8(n)
P(m, n+2)

FIG.4

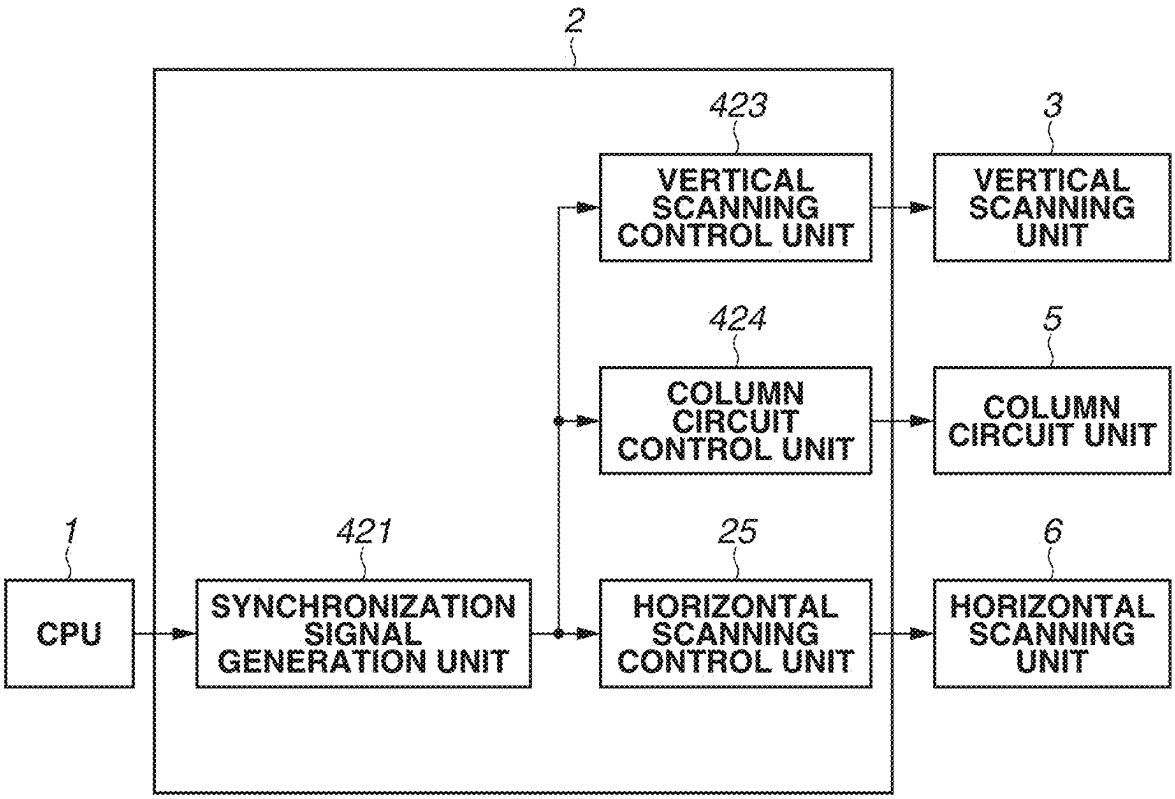

2
423
3
VERTICAL SCANNING CONTROL UNIT
VERTICAL SCANNING UNIT
424
5
COLUMN CIRCUIT CONTROL UNIT
COLUMN CIRCUIT UNIT
1
421
25
6
CPU
SYNCHRONIZATION SIGNAL GENERATION UNIT
HORIZONTAL SCANNING CONTROL UNIT
HORIZONTAL SCANNING UNIT

FIG.5

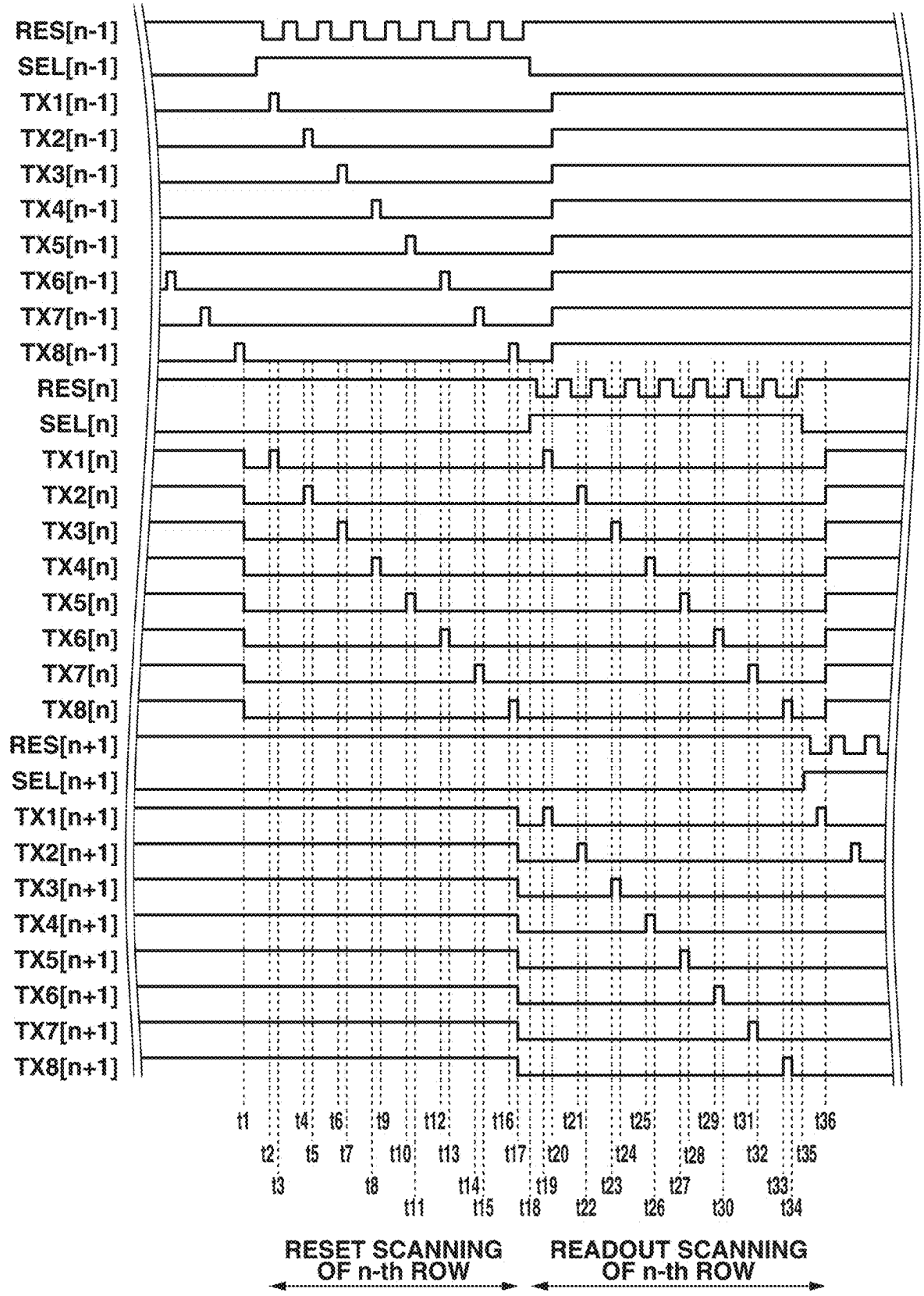

RES[n-1]
SEL[n-1]
TX1[n-1]
TX2[n-1]
TX3[n-1]
TX4[n-1]
TX5[n-1]
TX6[n-1]
TX7[n-1]
TX8[n-1]
RES[n]
SEL[n]
TX1[n]
TX2[n]
TX3[n]
TX4[n]
TX5[n]
TX6[n]
TX7[n]
TX8[n]
RES[n+1]
SEL[n+1]
TX1[n+1]
TX2[n+1]
TX3[n+1]
TX4[n+1]
TX5[n+1]
TX6[n+1]
TX7[n+1]
TX8[n+1]
t1 t2 t3 t4 t5 t6 t7 t8 t9 t10 t11 t12 t13 t14 t15 t16 t17 t18 t19 t20 t21 t22 t23 t24 t25 t26 t27 t28 t29 t30 t31 t32 t33 t34 t35 t36
RESET SCANNING OF n-th ROW
READOUT SCANNING OF n-th ROW

FIG.6

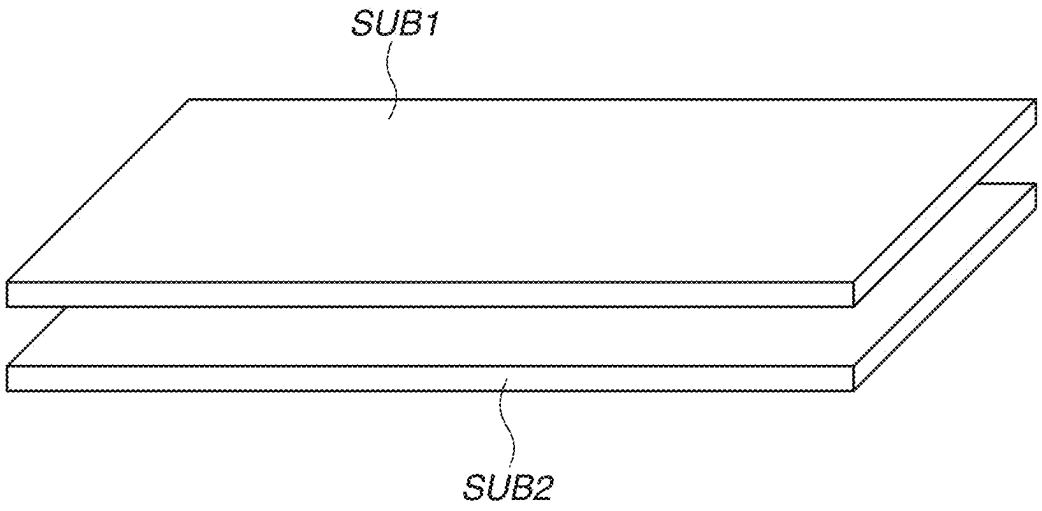


FIG.7

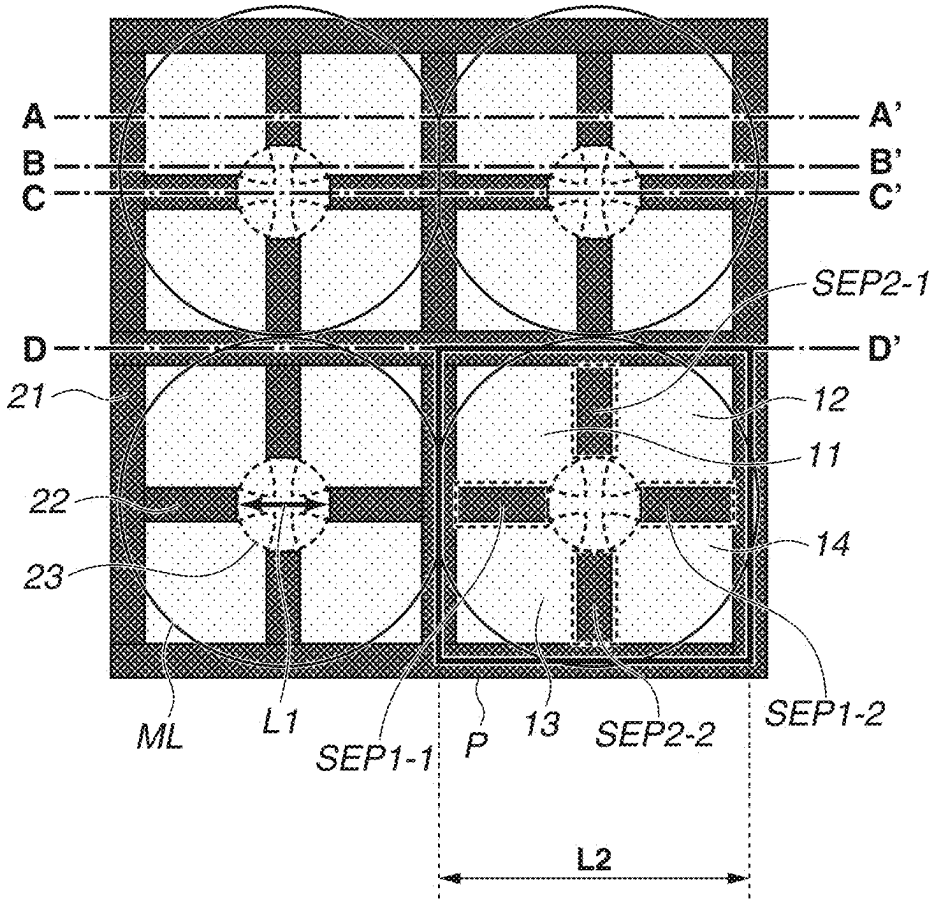


FIG.8

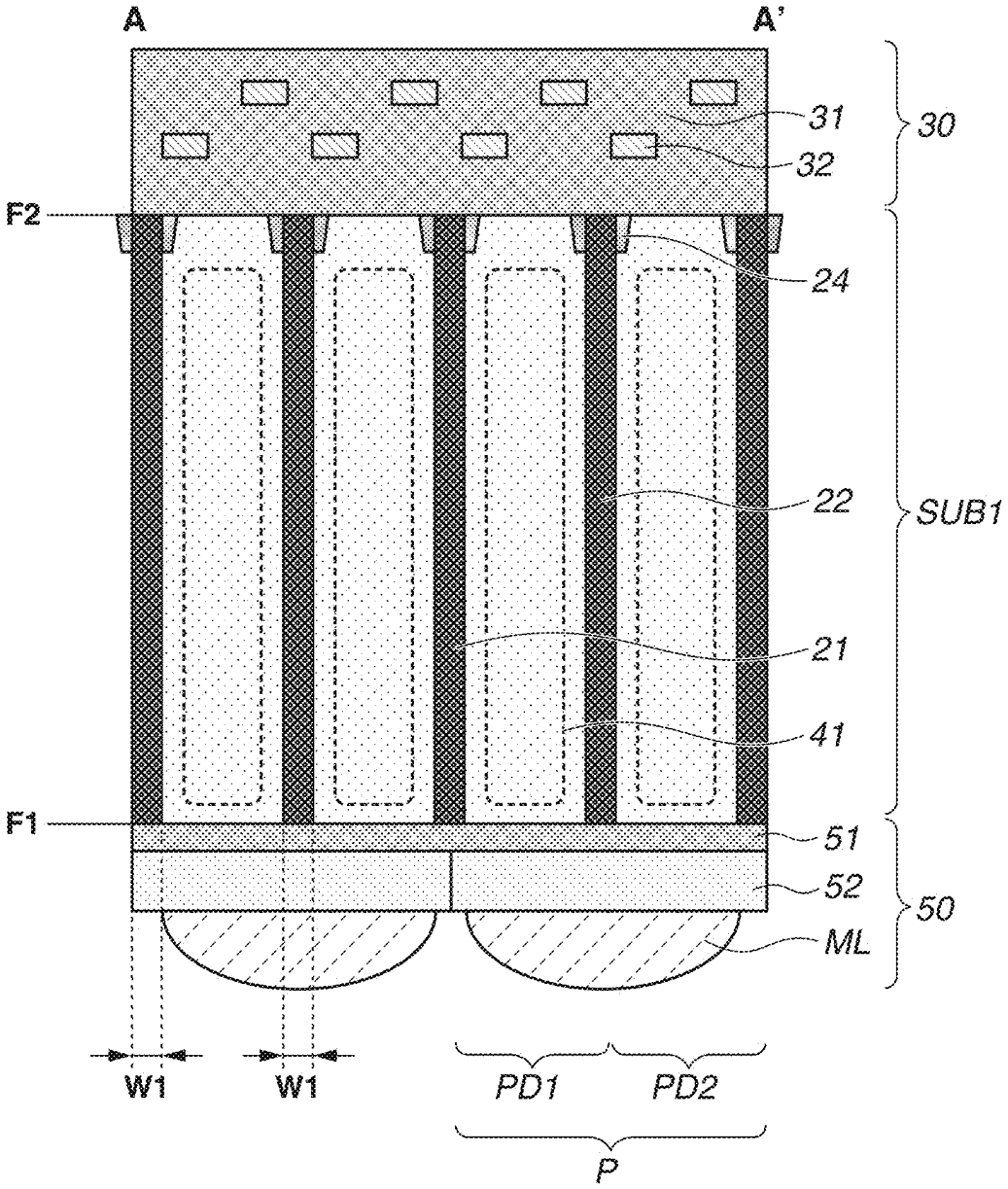


FIG.9

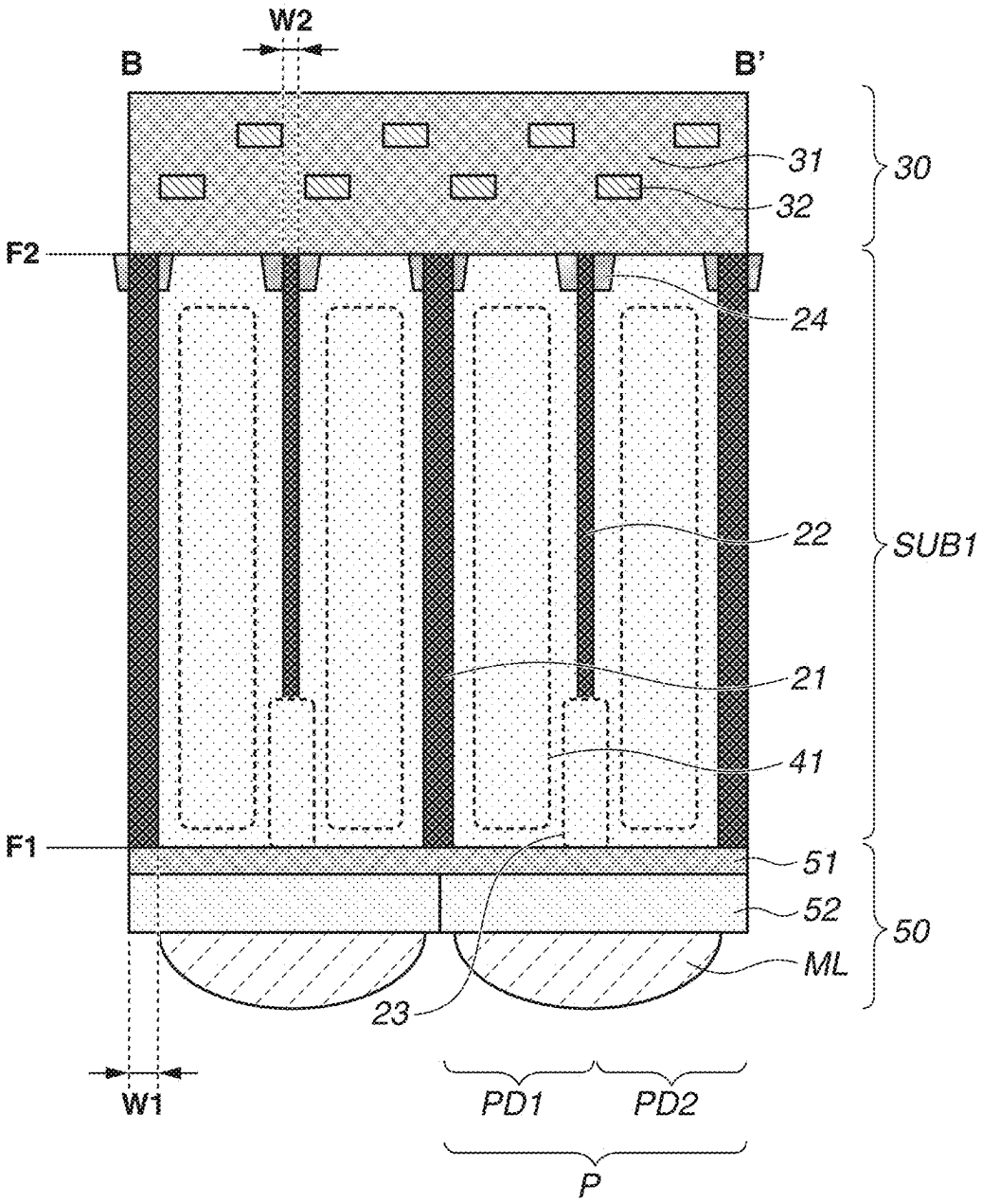


FIG.10

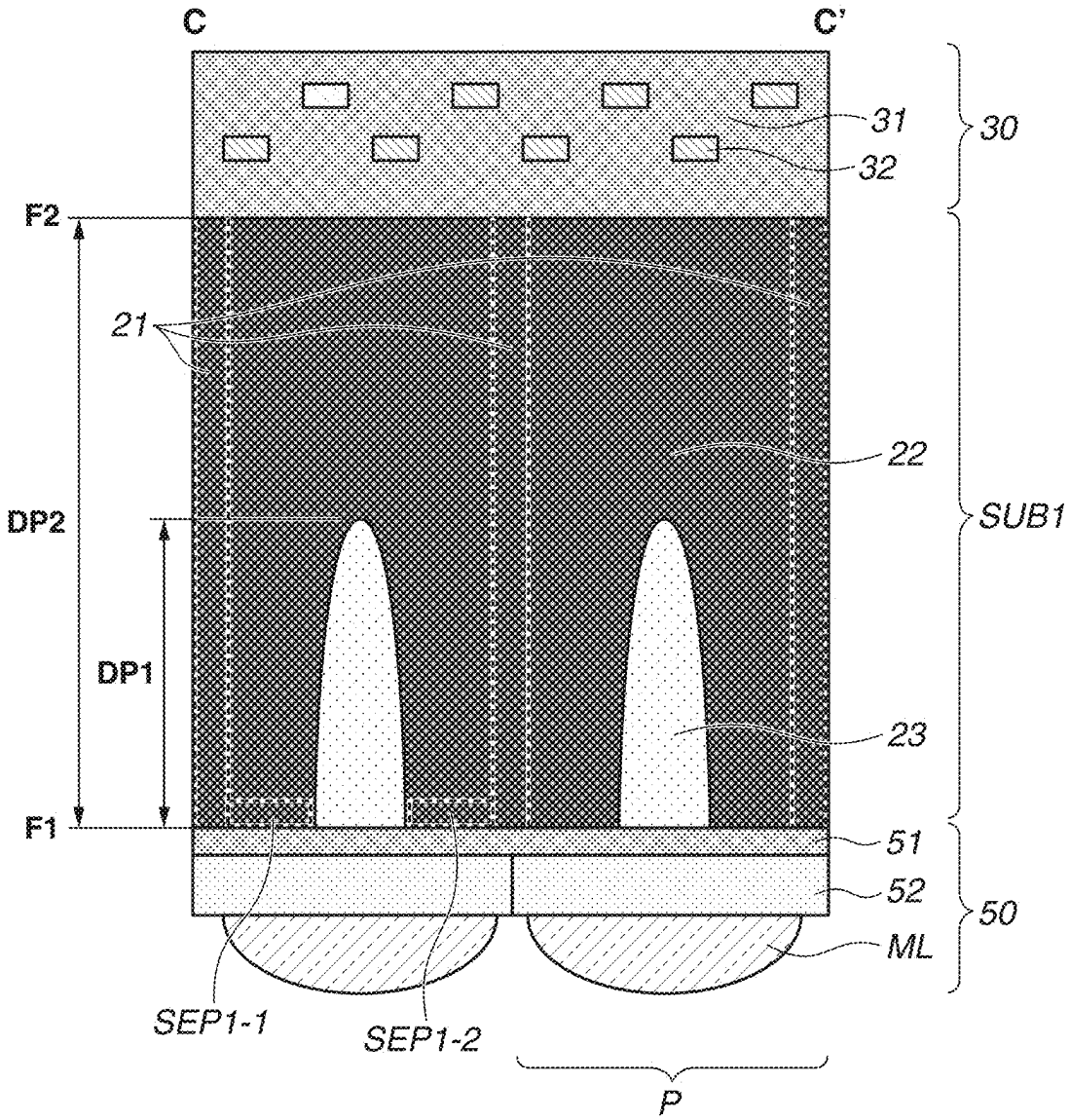


FIG.11

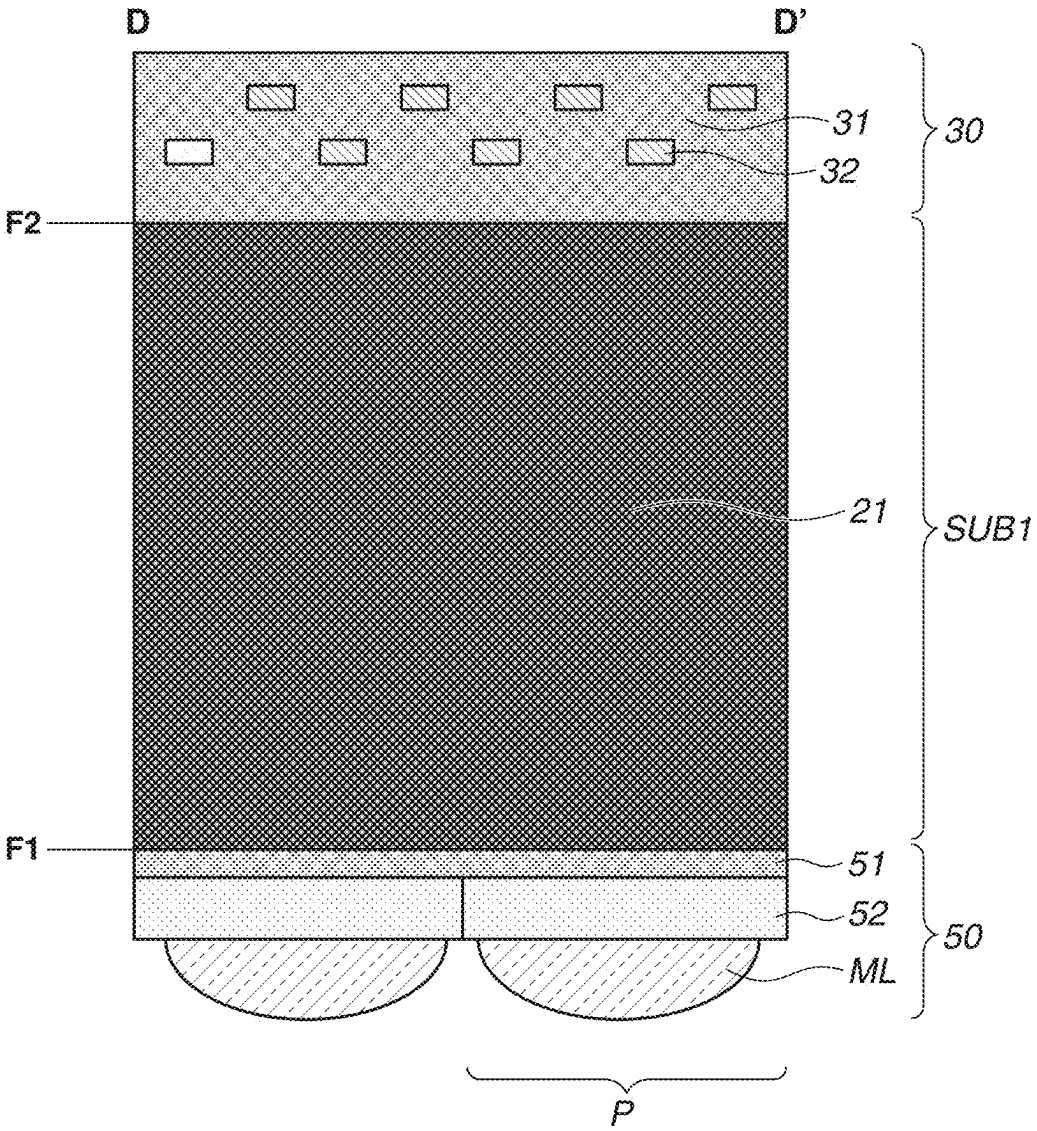


FIG.12

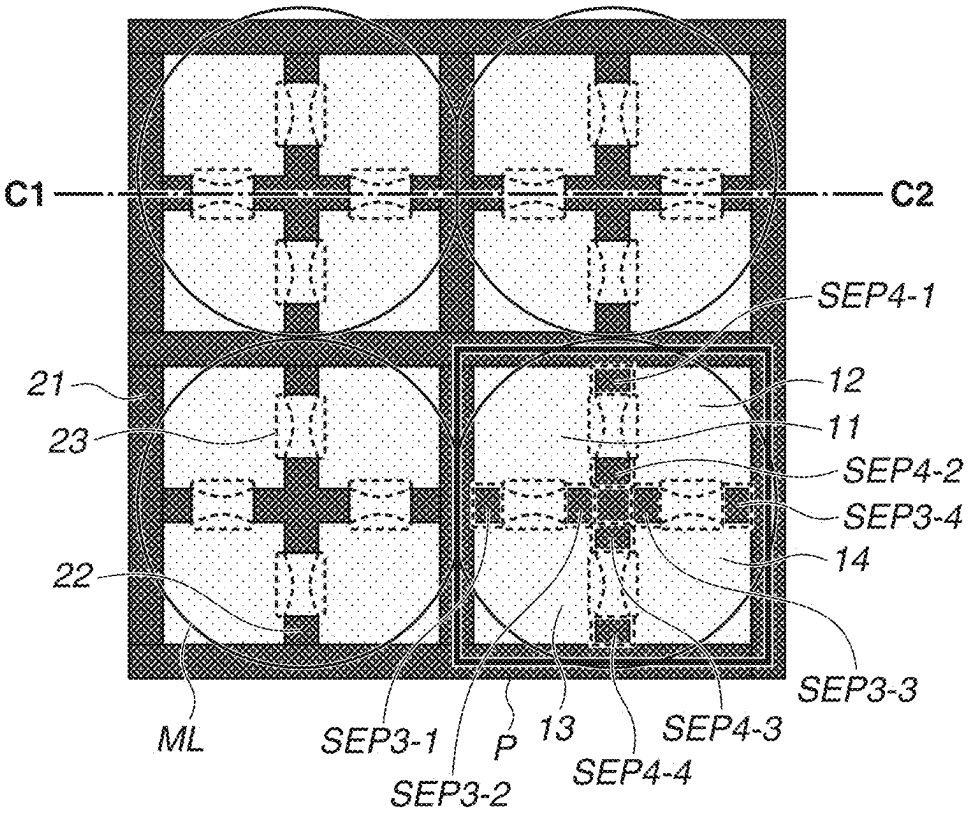

C1
C2
SEP4-1
21
12
23
11
SEP4-2
SEP3-4
22
14
SEP3-3
ML
SEP3-1
P
13
SEP4-3
SEP4-4
SEP3-2

FIG.13

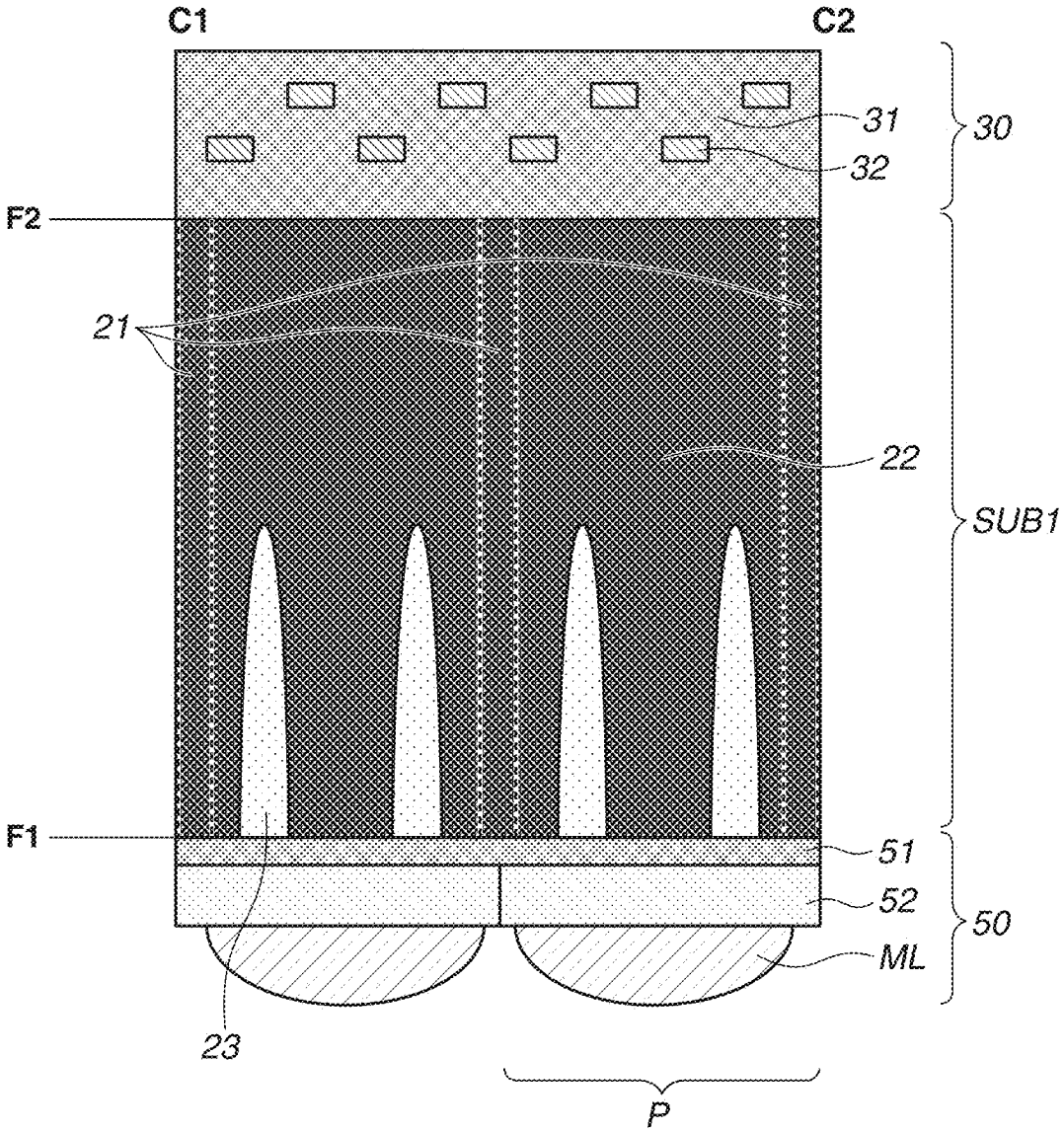


FIG.14

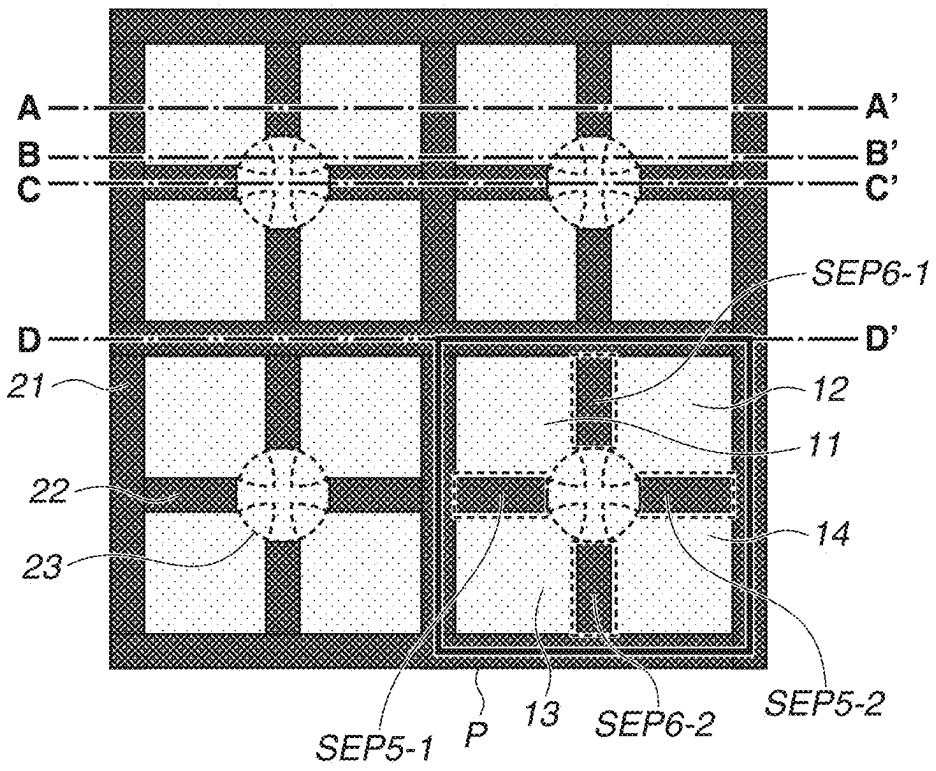


FIG.15

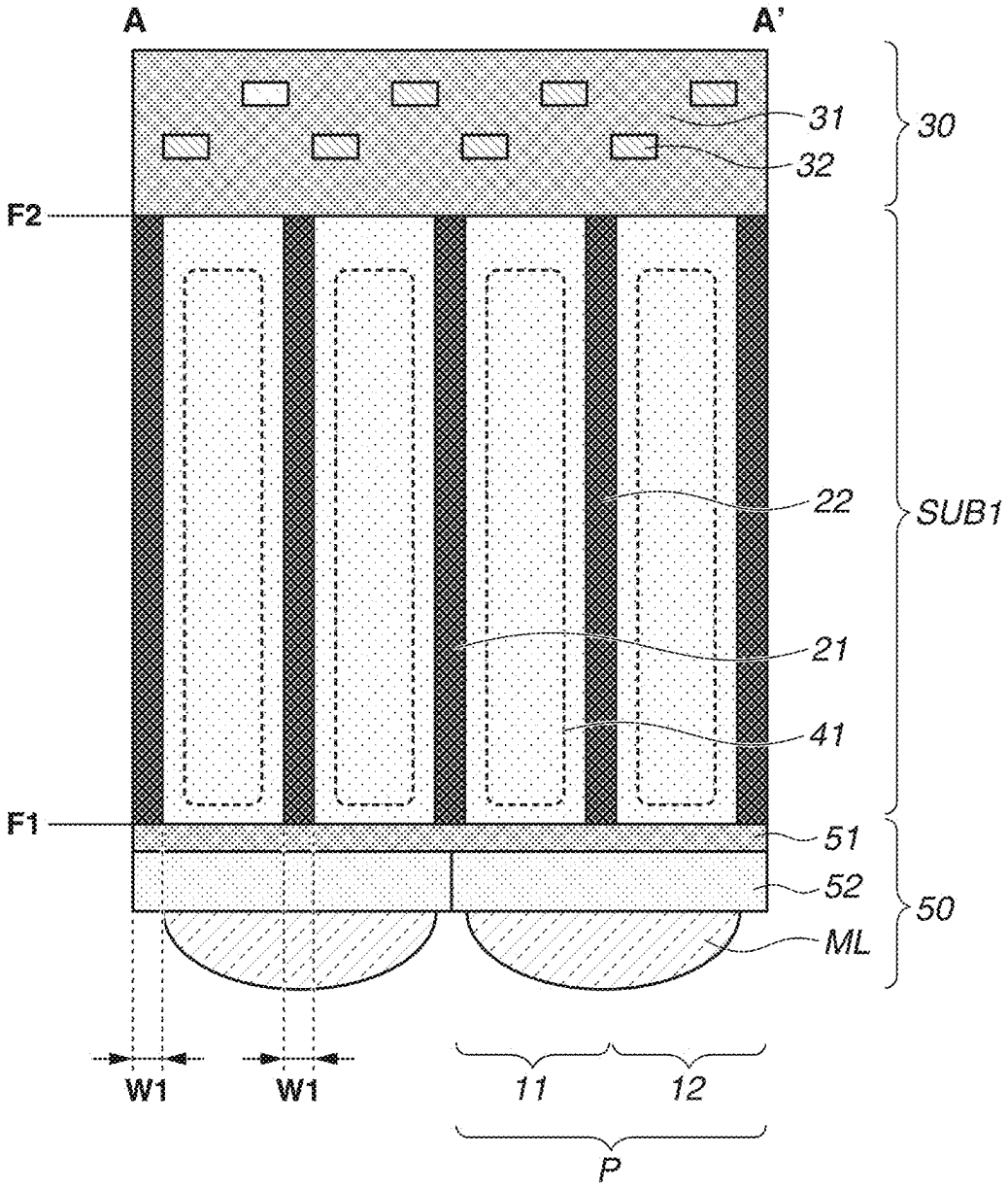


FIG.16

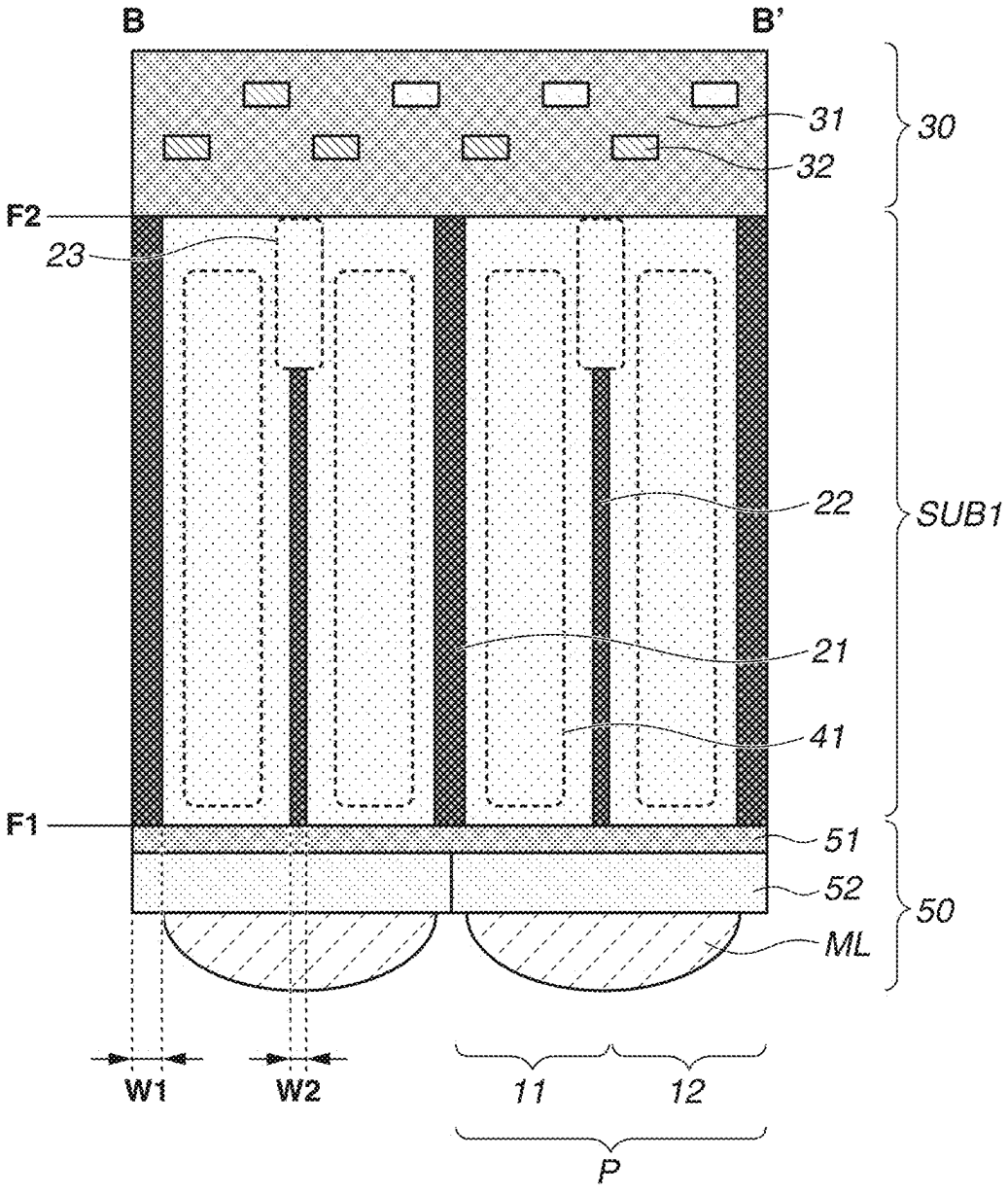


FIG.17

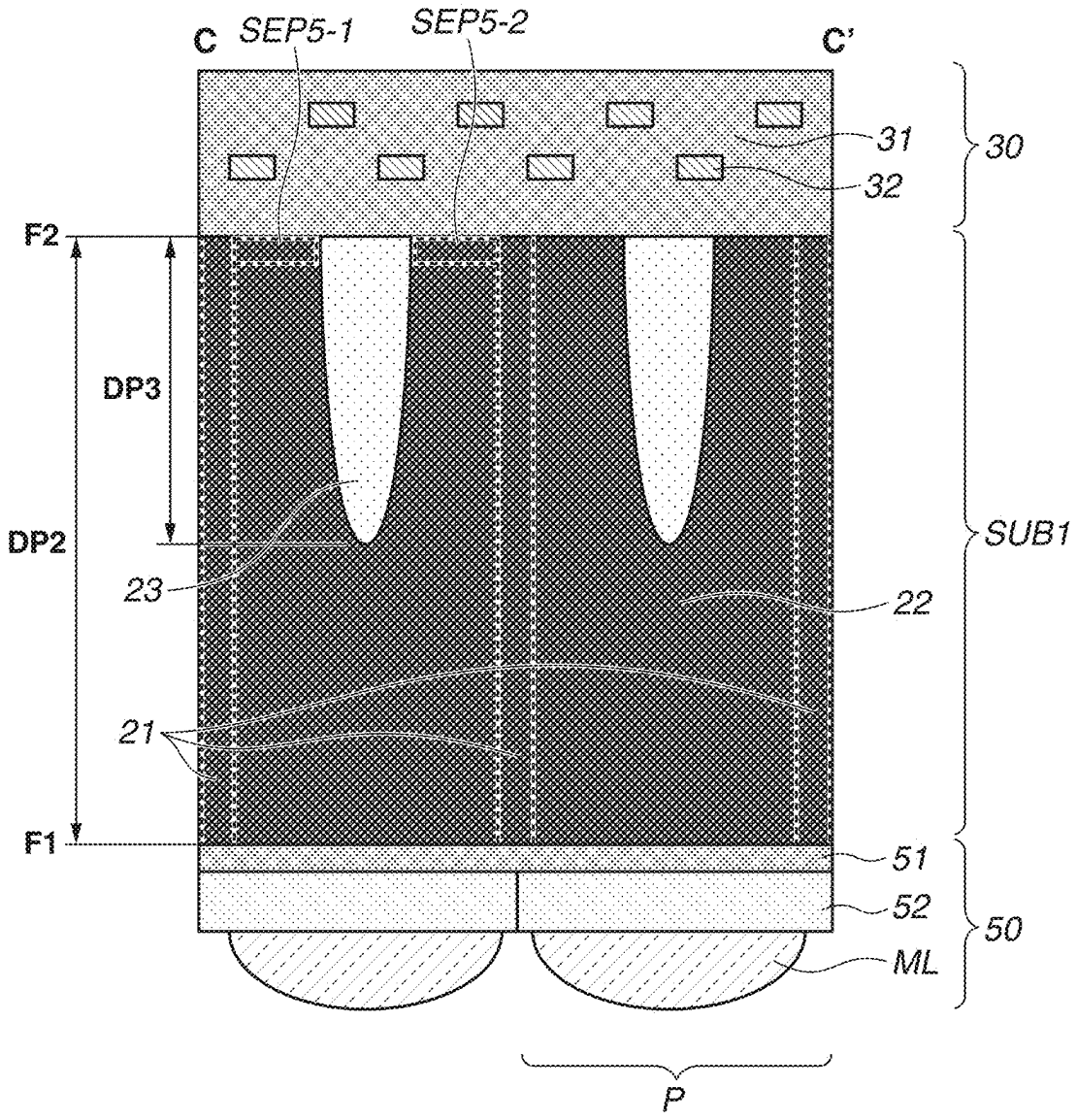


FIG.18

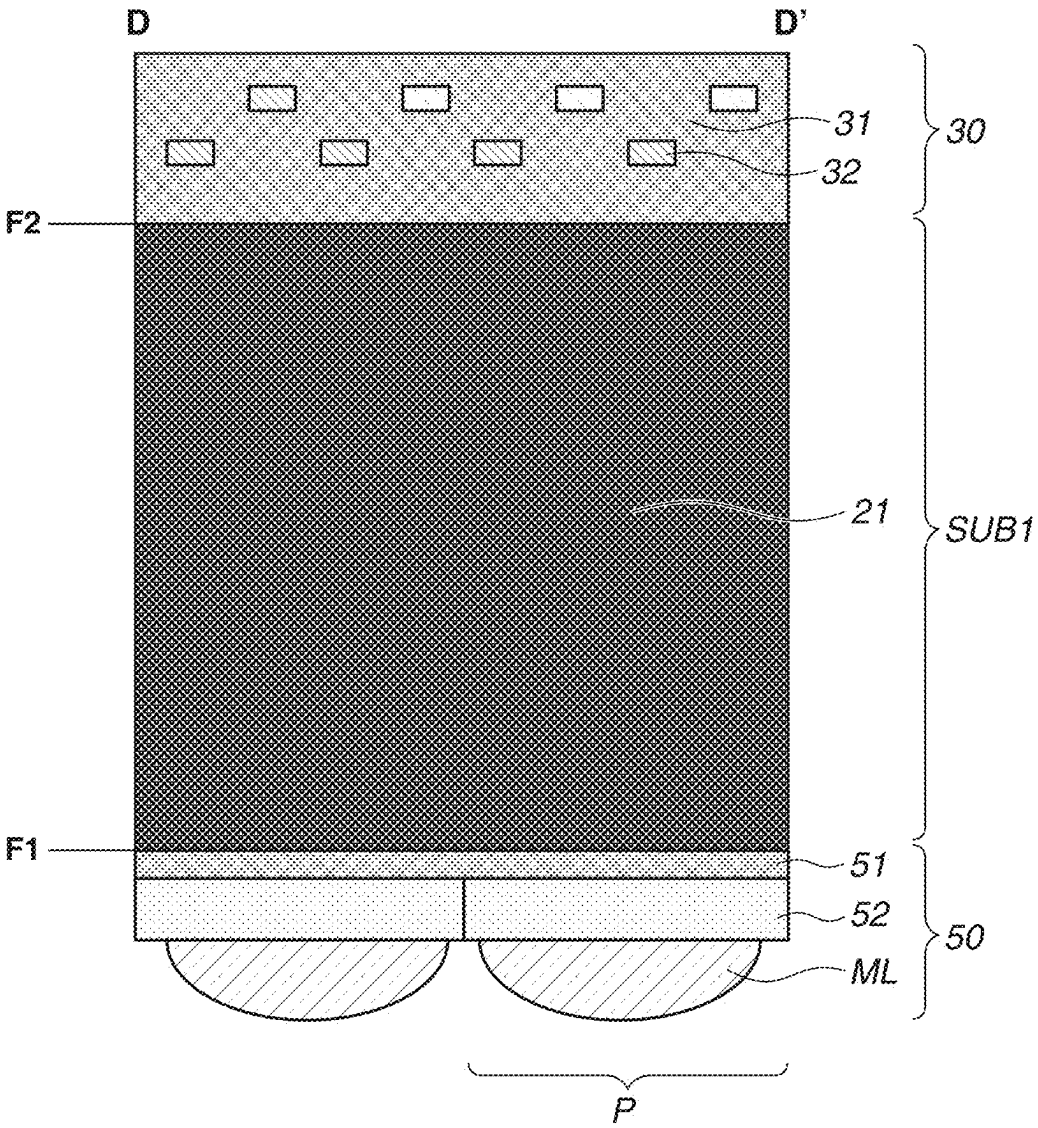


FIG.19

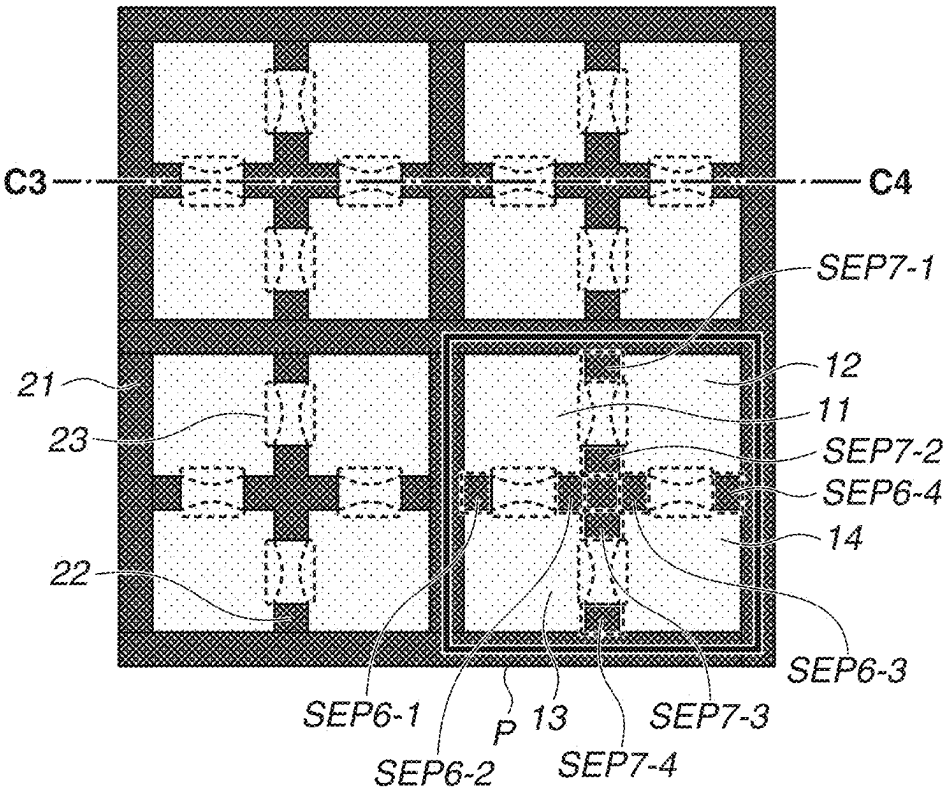

C3
C4
SEP7-1
12
11
SEP7-2
SEP6-4
14
SEP6-3
21
23
22
SEP6-1
SEP6-2
P
13
SEP7-4
SEP7-3

FIG.20

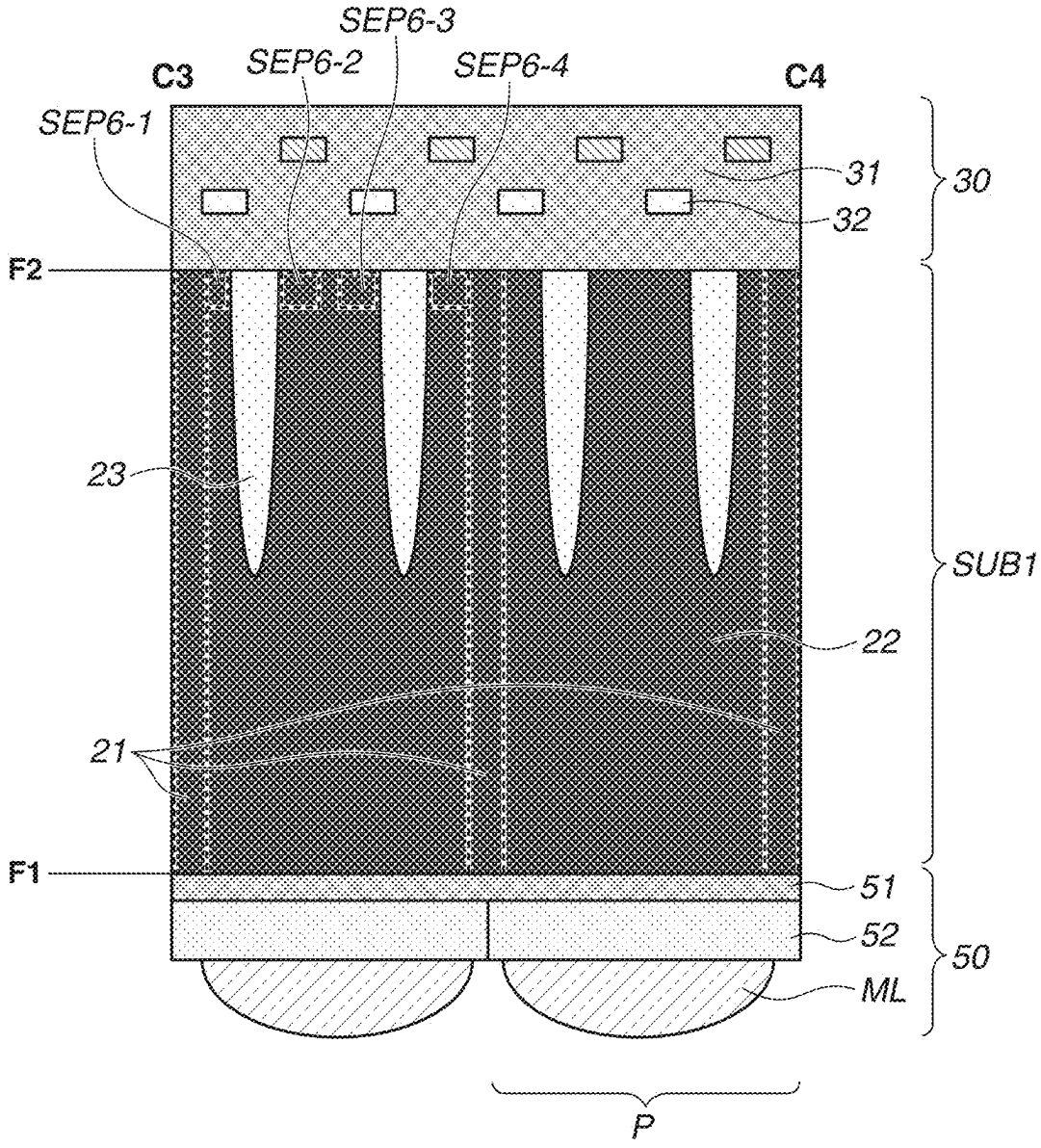

SEP6-3
SEP6-2
SEP6-4
C3
C4
SEP6-1
31
32
30
F2
23
SUB1
22
21
F1
51
52
50
ML
P

FIG.21A

PLANAR VIEW WITH RESPECT TO SECOND PRINCIPAL SURFACE F2

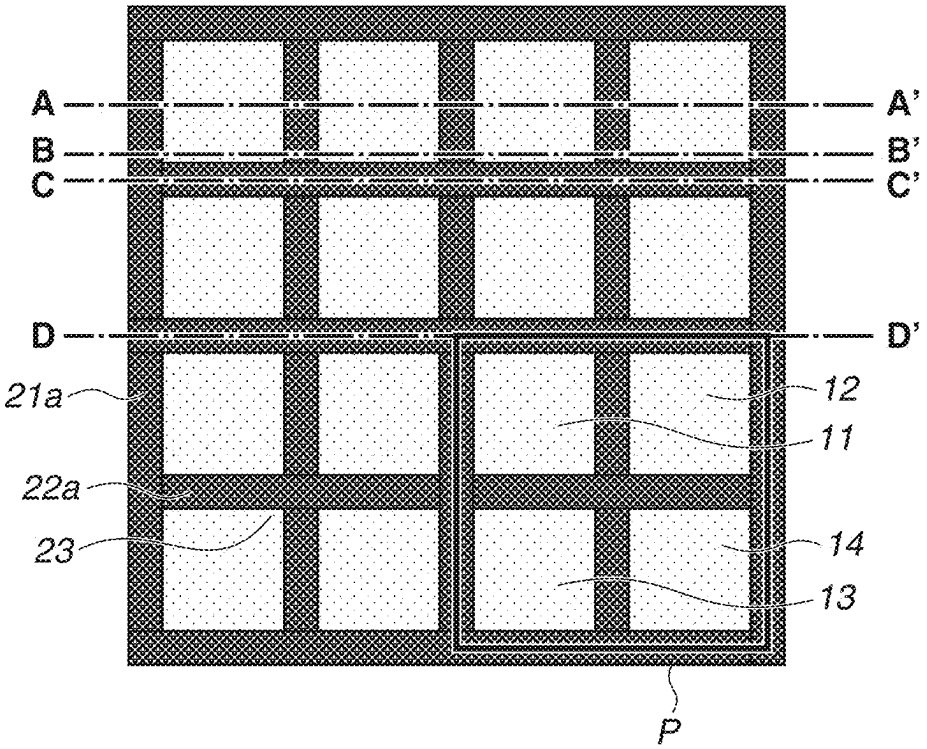


FIG.21B

PLANAR VIEW WITH RESPECT TO FIRST PRINCIPAL SURFACE F1

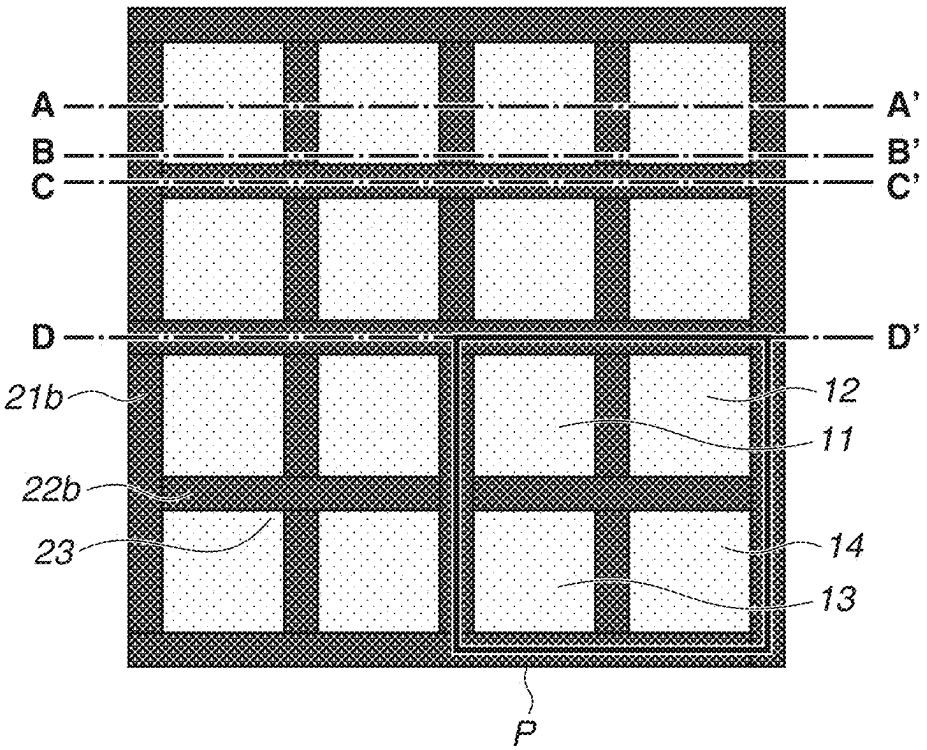


FIG.22

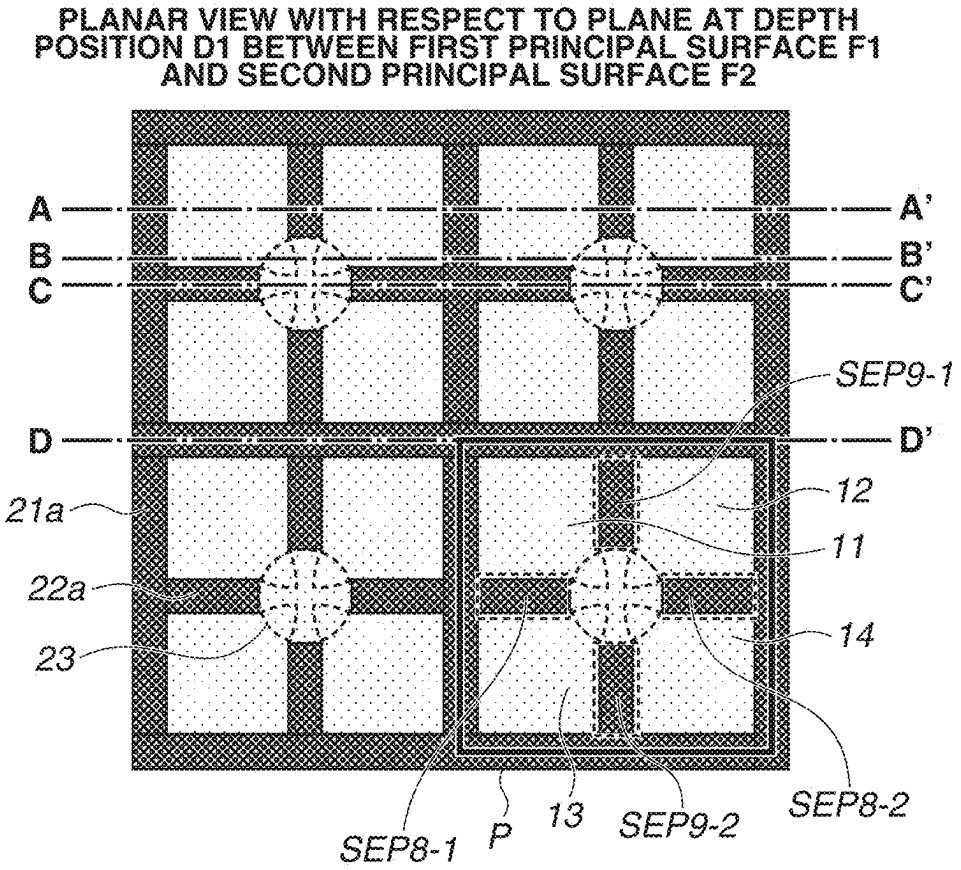

PLANAR VIEW WITH RESPECT TO PLANE AT DEPTH POSITION D1 BETWEEN FIRST PRINCIPAL SURFACE F1 AND SECOND PRINCIPAL SURFACE F2
A
A'
B
B'
C
C'
D
D'
SEP9-1
12
11
14
21a
22a
23
SEP8-1
P
13
SEP9-2
SEP8-2

FIG.23

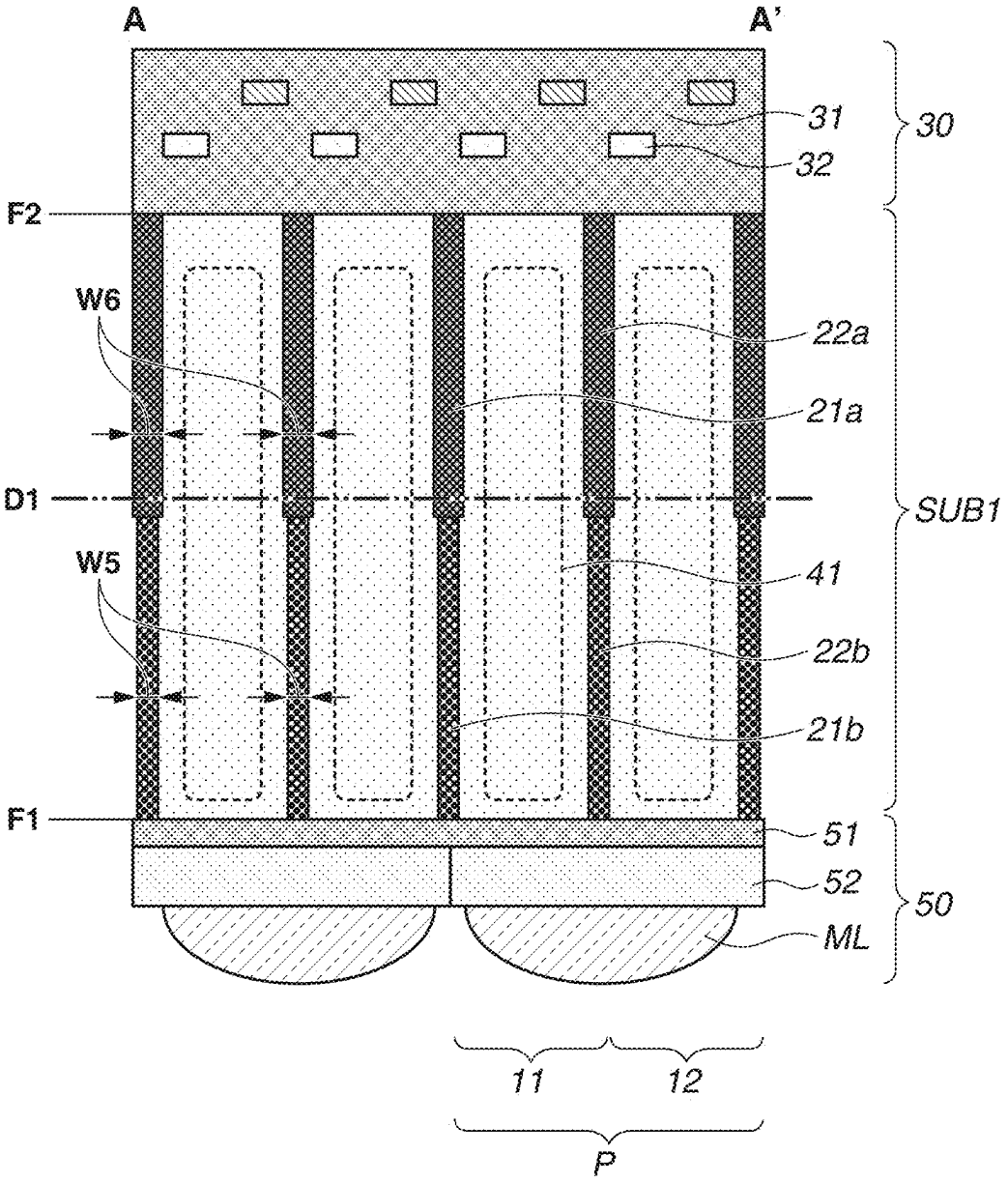


FIG.24

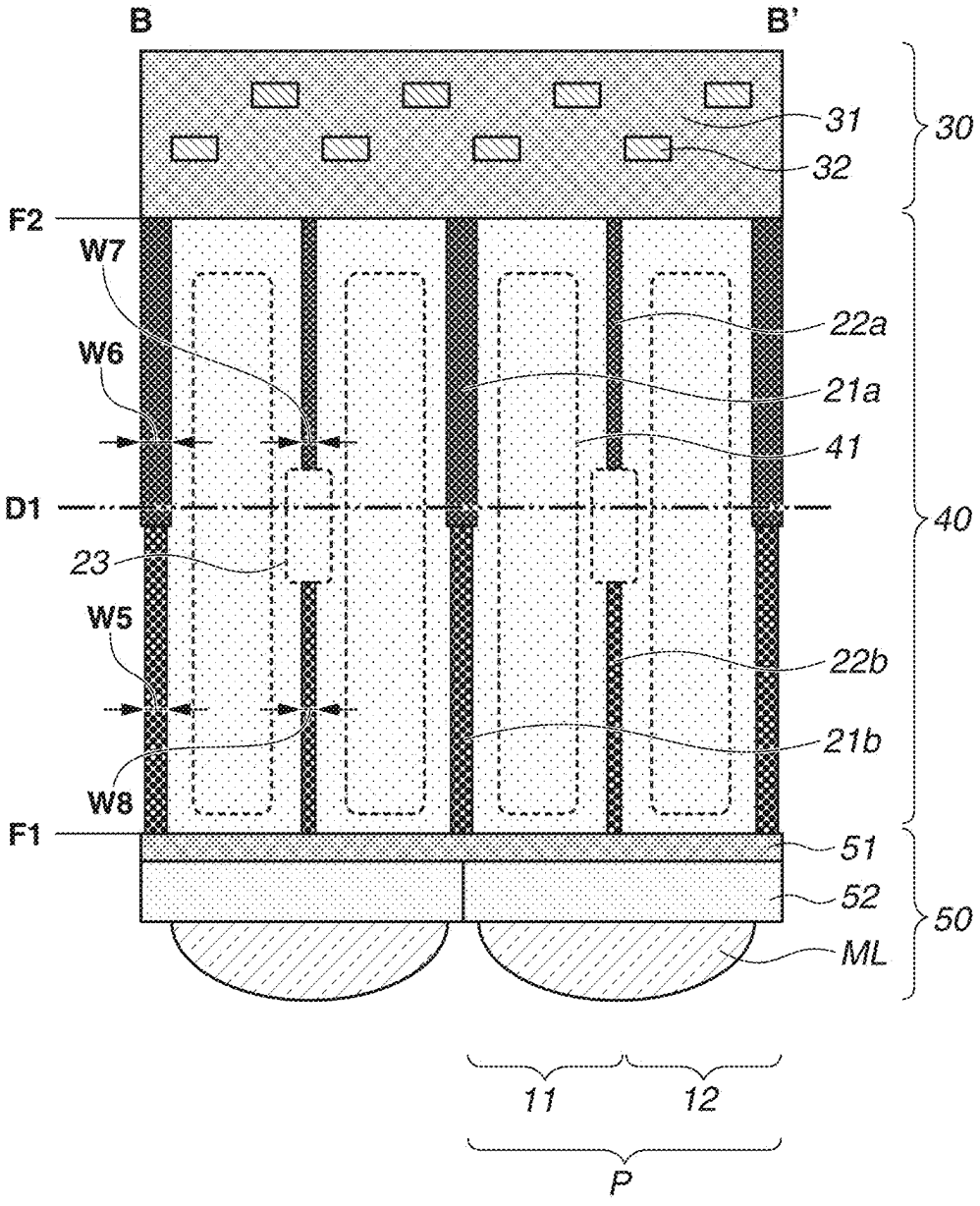

B
B'
31
32
30
F2
W7
22a
W6
21a
41
D1
40
23
W5
22b
21b
W8
F1
51
52
50
ML
11
12
P

FIG.25

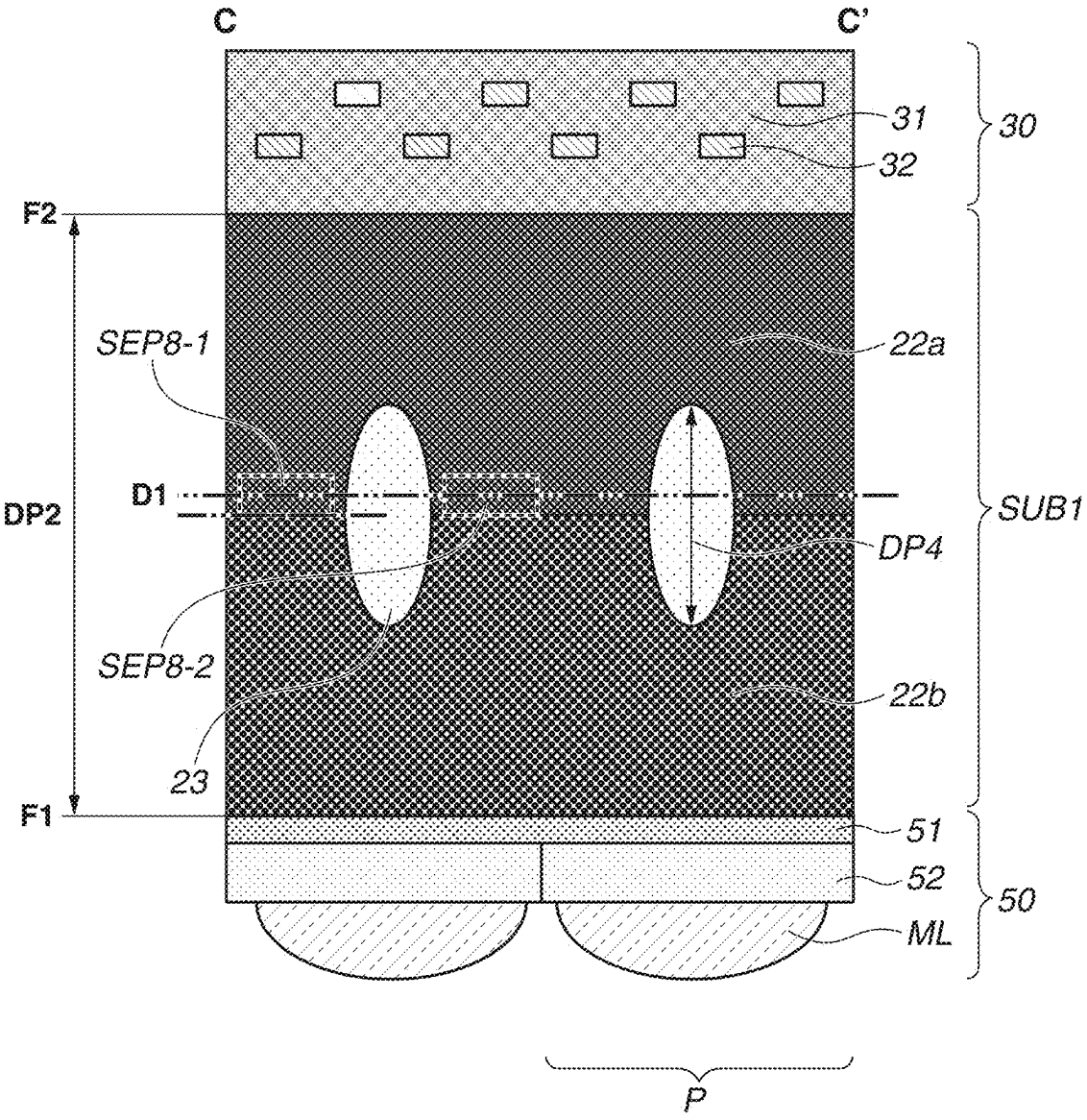

C
C'
31
32
30
F2
SEP8-1
22a
DP2
D1
SUB1
DP4
SEP8-2
22b
23
F1
51
52
50
ML
P

FIG.26

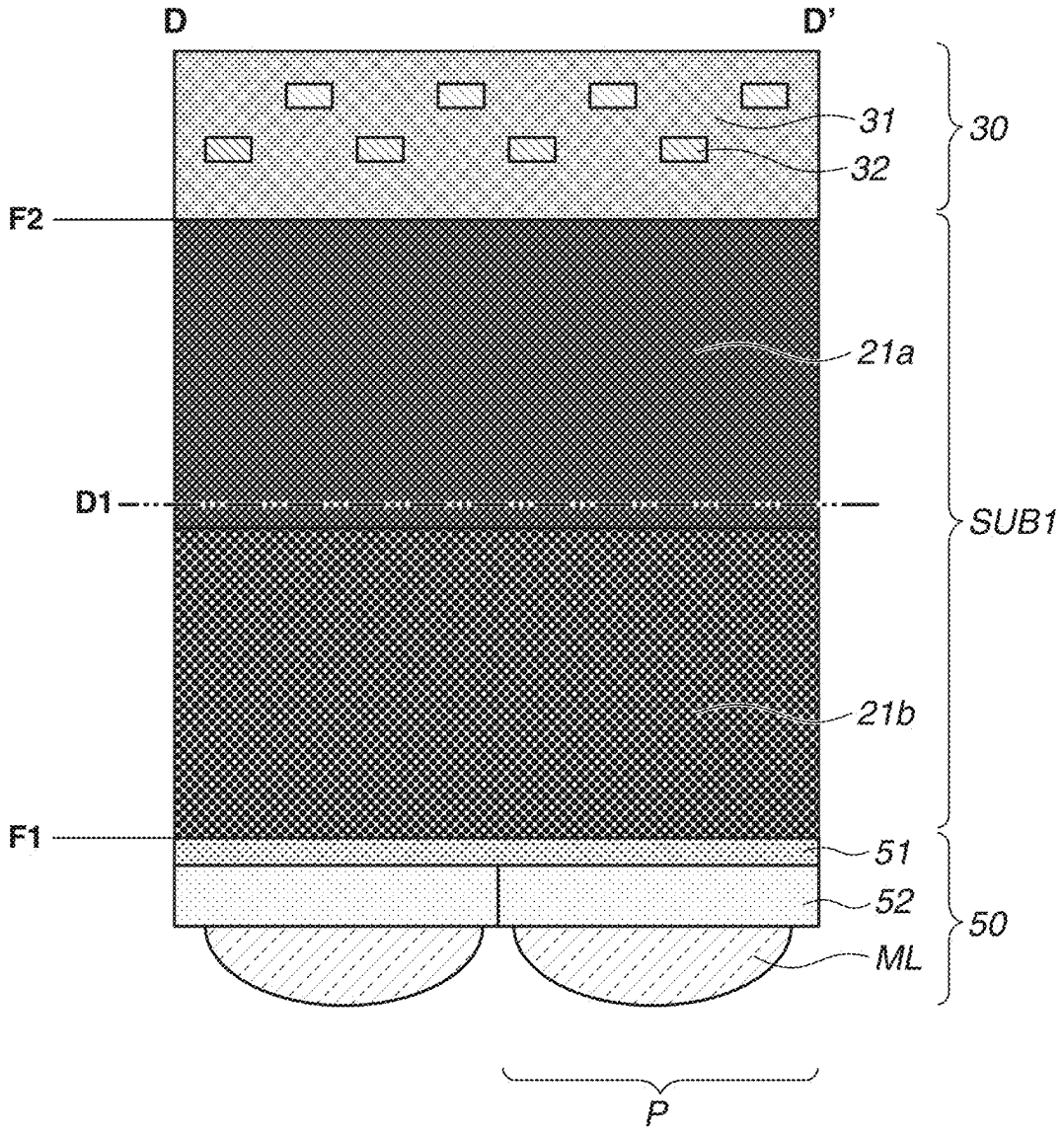


FIG.27

PLANAR VIEW WITH RESPECT TO PLANE AT DEPTH POSITION D1 BETWEEN FIRST PRINCIPAL SURFACE F1 AND SECOND PRINCIPAL SURFACE F2

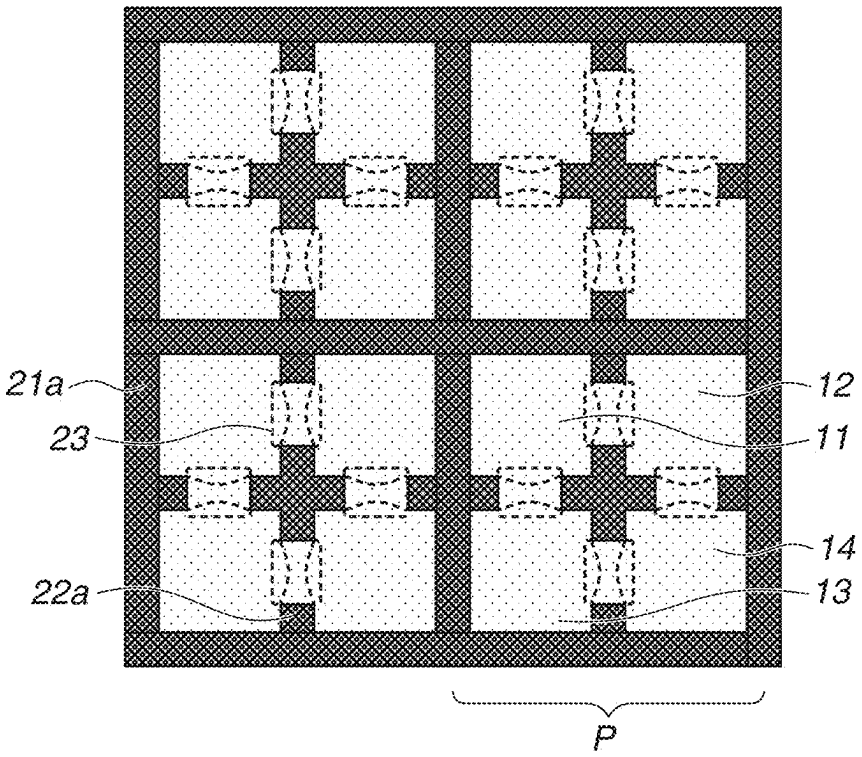


FIG.28A

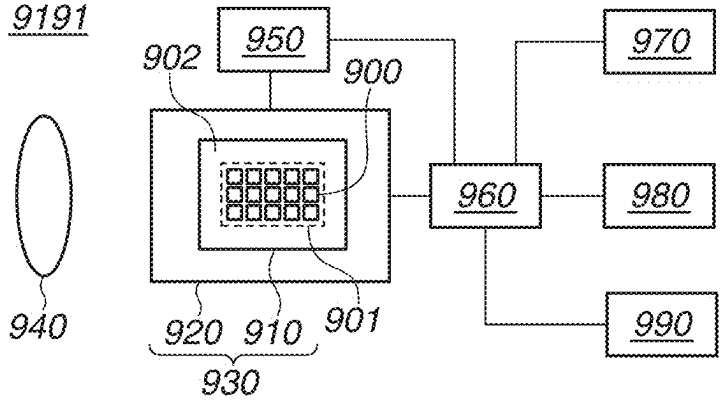


FIG.28B

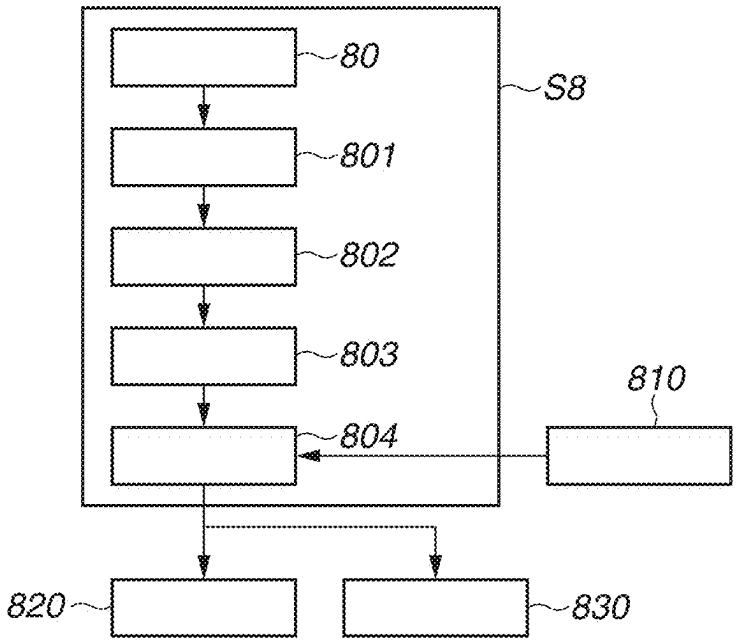
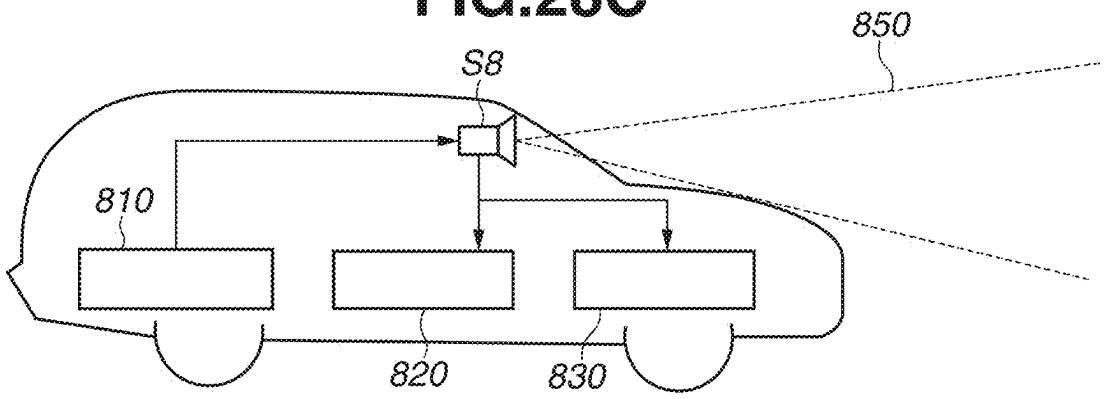


FIG.28C



PHOTOELECTRIC CONVERSION APPARATUS

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present disclosure relates to a photoelectric conversion apparatus that converts light into an electric signal.

Description of the Related Art

[0002] There has been known a photoelectric conversion apparatus that generates a signal charge corresponding to incident light.

[0003] A configuration in which a trench portion is provided between a plurality of photoelectric conversion units as discussed in United States Patent Application Publication No. 2016/0056200 has been known as the photoelectric conversion apparatus. By providing this trench portion, it is possible to desirably electrically separate the plurality of photoelectric conversion units.

SUMMARY OF THE INVENTION

[0004] According to an aspect of the present disclosure, a photoelectric conversion apparatus includes a semiconductor substrate having a first principal surface from which light enters, and a second principal surface facing the first principal surface, a microlens array including a plurality of microlenses, a plurality of pixels each including a corresponding one microlens of the plurality of microlenses, a plurality of photoelectric conversion units in a plurality of rows and a plurality of columns that is arranged inside the semiconductor substrate, and arranged in such a manner as to corresponding to the one microlens, and a first trench portion that separates the plurality of photoelectric conversion units, and a second trench portion provided between a photoelectric conversion unit included in one pixel of neighboring two pixels among the plurality of pixels, and a photoelectric conversion unit included in other one pixel of the neighboring two pixels, wherein, on the first principal surface, in a planar view with respect to the first principal surface, the first trench portion includes a plurality of first portions extending in a first direction, and a plurality of second portions extending in a second direction intersecting with the first direction, wherein a first region between one first portion and other first portion of the plurality of first portions, and a second region between one second portion and other second portion of the plurality of second portions each include a semiconductor region of the semiconductor substrate, and wherein, at a depth position between the first principal surface and the second principal surface, in the planar view, a part of the first trench portion is arranged at each of a position overlapping the first region and a position overlapping the second region.

[0005] According to another aspect, a photoelectric conversion apparatus includes a semiconductor substrate having a first principal surface from which light enters, and a second principal surface facing the first principal surface, a microlens array including a plurality of microlenses, a microlens array including a plurality of microlenses, a plurality of pixels each including a corresponding one microlens of the plurality of microlenses, a plurality of photoelectric conversion units in a plurality of rows and a plurality of columns that is arranged inside the semiconductor substrate, and arranged in such a manner as to corresponding to the one microlens, a first trench portion that separates the plurality of photoelectric conversion units, and a plurality of amplification transistors each having a gate, and a second trench portion provided between a photoelectric conversion unit included in one pixel of neighboring two pixels among the plurality of pixels, and a photoelectric conversion unit included in other one pixel of the neighboring two pixels, wherein the respective gates of the plurality of amplification transistors are connected in common to a node to which signal charges of the plurality of photoelectric conversion units are input, wherein, on the second principal surface, in a planar view with respect to the second principal surface, the first trench portion includes a plurality of first portions extending in a first direction, and a plurality of second portions extending in a second direction intersecting with the first direction, wherein a first region between one first portion and other first portion of the plurality of first portions, and a second region between one second portion and other second portion of the plurality of second portions each include a semiconductor region of the semiconductor substrate, and wherein, at a depth position between the first principal surface and the second principal surface, in the planar view, a part of the first trench portion is arranged at each of a position overlapping the first region and a position overlapping the second region.

[0006] According to still another aspect, a photoelectric conversion apparatus includes a semiconductor substrate having a first principal surface from which light enters, and a second principal surface facing the first principal surface, a microlens array including a plurality of microlenses, a plurality of pixels each including a corresponding one microlens of the plurality of microlenses, a plurality of photoelectric conversion units in a plurality of rows and a plurality of columns that is arranged inside the semiconductor substrate, and arranged in such a manner as to corresponding to the one microlens, and a first trench portion that separates the plurality of photoelectric conversion units, and a second trench portion provided between a photoelectric conversion unit included in one pixel of neighboring two pixels among the plurality of pixels, and a photoelectric conversion unit included in other one pixel of the neighboring two pixels, wherein, on the first principal surface, in a planar view with respect to the first principal surface, the first trench portion includes a first portion extending in a first direction, wherein, on the second principal surface, in a planar view with respect to the second principal surface, the first trench portion includes a third portion extending in the first direction, wherein the first portion and the third portion have portions overlapping in the planar view with respect to the first principal surface, and wherein a semiconductor region of the semiconductor substrate is arranged between the first portion and the third portion.

[0007] Further features of the present invention will become apparent from the following description of exemplary embodiments with reference to the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. **1** is a block diagram illustrating an overall configuration of a photoelectric conversion apparatus.

[0009] FIG. **2** is a diagram illustrating a configuration of a unit.

[0010] FIG. **3** is a diagram illustrating a configuration of a unit.

[0011] FIG. **4** is a block diagram illustrating a partial configuration of a photoelectric conversion apparatus.

[0012] FIG. **5** is a drive timing chart illustrating an operation of a photoelectric conversion apparatus.

[0013] FIG. **6** is a diagram illustrating a configuration of a stack-type photoelectric conversion apparatus.

[0014] FIG. **7** is a plan view of a photoelectric conversion apparatus.

[0015] FIG. **8** is a cross-sectional view of a photoelectric conversion apparatus.

[0016] FIG. **9** is a cross-sectional view of a photoelectric conversion apparatus.

[0017] FIG. **10** is a cross-sectional view of a photoelectric conversion apparatus.

[0018] FIG. **11** is a cross-sectional view of a photoelectric conversion apparatus.

[0019] FIG. **12** is a plan view of a photoelectric conversion apparatus.

[0020] FIG. **13** is a cross-sectional view of a photoelectric conversion apparatus.

[0021] FIG. **14** is a plan view of a photoelectric conversion apparatus.

[0022] FIG. **15** is a cross-sectional view of a photoelectric conversion apparatus.

[0023] FIG. **16** is a cross-sectional view of a photoelectric conversion apparatus.

[0024] FIG. **17** is a cross-sectional view of a photoelectric conversion apparatus.

[0025] FIG. **18** is a cross-sectional view of a photoelectric conversion apparatus.

[0026] FIG. **19** is a plan view of a photoelectric conversion apparatus.

[0027] FIG. **20** is a cross-sectional view of a photoelectric conversion apparatus.

[0028] FIGS. **21**A and **21**B are plan views of a photoelectric conversion apparatus.

[0029] FIG. **22** is a plan view of a photoelectric conversion apparatus.

[0030] FIG. **23** is a cross-sectional view of a photoelectric conversion apparatus.

[0031] FIG. **24** is a cross-sectional view of a photoelectric conversion apparatus.

[0032] FIG. **25** is a cross-sectional view of a photoelectric conversion apparatus.

[0033] FIG. **26** is a cross-sectional view of a photoelectric conversion apparatus.

[0034] FIG. **27** is a plan view of a photoelectric conversion apparatus.

[0035] FIGS. **28**A, **28**B, and **28**C are diagrams illustrating a configuration of a device.

DESCRIPTION OF THE EMBODIMENTS

[0036] In the technique discussed in United States Patent Application Publication No. 2016/0056200, the consideration of a structure of a desirable trench portion in a configuration in which a plurality of photoelectric conversion units is provided for one microlens has been insufficient.

[0037] A technique of the present disclosure provides a structure of a desirable trench portion in a configuration in which a plurality of photoelectric conversion units is provided for one microlens.

[0038] Hereinafter, each exemplary embodiment will be described with reference to the drawings.

[0039] In each exemplary embodiment to be described below, an imaging apparatus will be mainly described as an example of a photoelectric conversion apparatus. Nevertheless, each exemplary embodiment is not limited to the imaging apparatus and can be applied to another example of the photoelectric conversion apparatus. Examples of the photoelectric conversion apparatus include a distance measurement apparatus (apparatus for distance measurement that uses focus detection or time of flight (TOF)), and a photometric apparatus (apparatus for measurement of an incident light amount).

[0040] Conductivity types of semiconductor regions and wells, and dopants to be implanted, which will be described below in the following exemplary embodiments, are mere examples. The conductivity types and the dopants are not limited to those described in the exemplary embodiments. The conductivity types and the dopants can be appropriately changed from those described in the exemplary embodiments, and the potentials of semiconductor regions and wells are appropriately changed in accordance with the change.

[0041] The conductivity type of a transistor to be described in the following exemplary embodiments is a mere example, and the conductivity type is not limited to the conductivity type described in the exemplary embodiments. The conductivity type can be appropriately changed from the conductivity type described in the exemplary embodiments, and potentials of a gate, a source, and a drain of the transistor are appropriately changed in accordance with the change.

[0042] For example, as for a transistor to be operated as a switch, it is sufficient that a low level and a high level of a potential to be supplied to a gate are made reverse to those described in the exemplary embodiments, in accordance with the change of a conductivity type. In addition, the conductivity type of a semiconductor region to be described in the following exemplary embodiments is a mere example, and the conductivity type is not limited to the conductivity type described in the exemplary embodiments. The conductivity type can be appropriately changed from the conductivity type described in the exemplary embodiments, and the potential of the semiconductor region is appropriately changed in accordance with the change.

[0043] In the following exemplary embodiments, the connection between elements of circuits will be sometimes described. In this case, even in a case where another element is interposed between elements to be observed, unless otherwise noted, the elements to be observed are treated as being connected. For example, it is assumed that an element A is connected to one node of a capacitative element C having a plurality of nodes, and an element B is connected to the other node. Even in such a case, unless otherwise noted, the elements A and B are treated as being connected.

[0044] A metal member such as a wire and a pad to be described in this specification may be a metal body of a certain single element, or may be a mixture (alloy). For example, a wire to be described as a copper wire may be a copper single body, or may have a configuration mainly containing copper and further containing other components. In addition, for example, a pad to be connected with an external terminal may be an aluminum single body, or may have a configuration mainly containing aluminum and fur-

ther containing other components. The copper wire and the aluminum pad described here are examples, and can be changed to various types of metal.

[0045] The wire and the pad described here are examples of metal members to be used in a photoelectric conversion apparatus, and can also be applied to other metal members.

[0046] FIG. **1** is a block diagram illustrating a schematic configuration of a photoelectric conversion apparatus according to a first exemplary embodiment. The photoelectric conversion apparatus includes a central processing unit (CPU) **1**, a control unit **2**, a vertical scanning unit **3**, a pixel array **4**, a column circuit unit **5**, a horizontal scanning unit **406**, and a signal output unit **7**.

[0047] Various circuits included in the photoelectric conversion apparatus can be formed on one or a plurality of semiconductor substrates.

[0048] The CPU **1** is a processor that controls the photoelectric conversion apparatus by executing a program. The CPU **1** may be provided within the photoelectric conversion apparatus, or may be provided within a photoelectric conversion system in which the photoelectric conversion apparatus is mounted (i.e., may be provided outside the photoelectric conversion apparatus).

[0049] The control unit **2** is a control circuit that supplies a control signal to the vertical scanning unit **3**, the column circuit unit **5**, and the horizontal scanning unit **406** upon receiving a control signal such as a synchronization signal and a setting signal indicating an operation mode that are output from the CPU **1**.

[0050] The vertical scanning unit **3** is a scanning circuit including a shift register, a gate circuit, and a buffer circuit. The vertical scanning unit **3** performs reset scanning and readout scanning of the pixel array **4** upon receiving control signals such as a vertical synchronization signal, a horizontal synchronization signal, and a clock signal from the control unit **2**. The reset scanning refers to an operation of starting exposure by sequentially cancelling a reset state of the photoelectric conversion units and bringing the photoelectric conversion units into a charge accumulation state for pixels on a part or all of rows of the pixel array **4**. In addition, the readout scanning refers to an operation of sequentially outputting signals that are based on the charges accumulated in the photoelectric conversion units, to pixels on a part or all of rows of the pixel array **4**. The vertical scanning unit **3** corresponds to a drive device that outputs a drive signal for driving the pixel array **4** for each row, to the pixel array **4**.

[0051] The pixel array **4** includes a plurality of pixels P(**1**, **1**) to P(a, b) on N rows and M columns that are arrayed on a plurality of rows and a plurality of columns, and a plurality of vertical output lines Vline(**1**) to Vline(b) on the M columns. Here, a row direction refers to a horizontal direction in the drawings, and a column direction refers to a vertical direction in the drawings. In addition, numbers in the parenthesis of the pixel P(a, b) sequentially indicates a column number and a row number. A row number of the uppermost row in FIG. **1** is 1, and a column number of the leftmost column in FIG. **1** is 1. In a case where there is no need to indicate a column number and a row number, numbers indicating a column number and a row number are sometimes omitted.

[0052] The column circuit unit **5** includes an amplification circuit, an analog-to-digital conversion (hereinafter, will be described as "AD conversion".) circuit, and a column memory. These circuits are arranged corresponding to each of the vertical output lines Vline(**1**) to Vline(b). The column circuit unit **5** amplifies a signal read out from the pixel array **4**, performs AD conversion, and stores the signal into the column memory as a digital signal. The horizontal scanning unit **406** is a scanning circuit including a shift register, a gate circuit, and a buffer circuit. Upon receiving a control signal from the control unit **2**, the horizontal scanning unit **406** sequentially scans signals stored in the memory of the column circuit unit **5**, and outputs the signals to the signal output unit **7**.

[0053] The signal output unit **7** includes a digital processing unit and an output circuit such as a parallel-serial conversion circuit or low voltage differential signaling (LVDS). The signal output unit **7** performs digital processing of a signal output from the horizontal scanning unit **406**, and outputs the processed signal to the outside of the photoelectric conversion apparatus as serial data.

[0054] The column circuit unit **5** needs not always include the function of AD conversion, and a configuration may be modified in such a manner that AD conversion is performed on the outside of the photoelectric conversion apparatus, for example. In this case, the configurations of the horizontal scanning unit **406** and the signal output unit **7** are also appropriately modified in such manner as to be adapted to the processing of an analog signal. FIG. **2** is a circuit diagram of a pixel P included in the pixel array **4** according to the present exemplary embodiment. FIG. **2** illustrates a configuration of a pixel P(x, y) on an x-th column and a y-th row, a pixel P(x, y+1) on the x-th column and a (y+1)th row.

[0055] A unit U (m, n) includes the pixels P in two rows. The unit U (m, n) illustrated in FIG. **2** includes the pixel P(x, y) and the pixel P(x, y+1).

[0056] Each unit U includes photoelectric conversion units PD**1** to PD**8**, a floating diffusion FD, transfer transistors M**1** to M**8**, a reset transistor M**9**, an amplification transistor M**10**, and a selection transistor M**11**. In the unit U, the eight photoelectric conversion units PD**1** to PD**8** share the one floating diffusion FD. FIG. **2** illustrates a configuration in which the one amplification transistor M**10** is provided for one unit U. Alternatively, a configuration in which a plurality of amplification transistors M**10-1**, M**10-2**, and M**10-3** are provided as illustrated in FIG. **3** may be employed, and the number of amplification transistors is not limited.

[0057] Each of the photoelectric conversion units PD**1** to PD**8** is a photoelectric conversion element that generates and accumulates charges corresponding to incident light, by photoelectrically-converting the incident light. Each of the photoelectric conversion units PD**1** to PD**8** is a photodiode, for example. An anode of the photodiode included in each of the photoelectric conversion units PD**1** to PD**8** is connected to a node of a ground potential. Cathodes of photodiodes included in the respective photoelectric conversion units PD**1** to PD**8** are connected to sources of the respective transfer transistors M**1** to M**8**. FIG. **2** illustrates a configuration in which the eight photoelectric conversion units PD**1** to PD**8** share the one floating diffusion FD, but the configuration is not limited to this example. One floating diffusion FD may be arranged in such a manner as to correspond to one photoelectric conversion unit PD**1**, or one floating diffusion FD may be arranged in such a manner as to correspond to the four photoelectric conversion units PD**1** to PD**4**.

[0058] Drains of the transfer transistors M**1** to M**8** are connected to the floating diffusion FD serving as a connection node of a source of the reset transistor M**9** and a gate of the amplification transistor M**10**. A drain of the reset transistor M**9** and a drain of the amplification transistor M**10** are electrically connected to a power line having a pixel power potential VCC. A source of the amplification transistor M**10** is connected to a drain of the selection transistor M**11**. A source of the selection transistor M**11** is electrically connected to a current source (not illustrated) via a vertical output line Vline(m). The amplification transistor M**10** and the current source accordingly operate as a source follower circuit. That is, the amplification transistor M**10** functions as an output unit that can output a signal corresponding to the potential of the floating diffusion FD, to the vertical output line Vline(m). The floating diffusion FD contains a capacitive component (floating diffusion capacitance), and functions as a charge holding unit due to the capacitive component.

[0059] Control signals PTX**1**(*n*) to PTX**8**(*n*) are respectively input to gates of the transfer transistors M**1** to M**8** from the vertical scanning unit **3**. The transfer transistors M**1** to M**8** transfer charges accumulated in the photoelectric conversion units PD**1** to PD**8**, to the floating diffusion FD based on the respective control signals PTX**1**(*n*) to PTX**8**(*n*). That is, each of the transfer transistors M**1** to M**8** functions as a charge transfer unit. The floating diffusion FD holds transferred charges.

[0060] A control signal PRES (n) is input to a gate of the reset transistor M**9** from the vertical scanning unit **3**. The reset transistor M**9** resets the potential of the floating diffusion FD to a predetermined potential based on the control signal PRES (n).

[0061] A control signal PSEL(n) is input to a gate of the selection transistor M**11** from the vertical scanning unit **3**. The control signal PSEL(n) is a signal for selecting a row to which a signal is to be output, and the selection transistor M**11** enters a conductive state or non-conductive state based on the control signal PSEL(n). An additional character "n" of each control signal indicates a row number of a corresponding row.

[0062] A transistor is assumed to enter the conductive state when a control signal input to a gate is at a high level, and enters the non-conductive state when the control signal is at a low level. In addition, the high level corresponds to a logical value "1" and the low level corresponds to a logical value "0".

[0063] When the transfer transistors M**1** to M**8** are in the non-conductive state, the photoelectric conversion units PD**1** to PD**8** enter an accumulation state of accumulating charges generated by photoelectric conversion. When the transfer transistors M**1** to M**8** are in the conductive state and the reset transistor M**9** is in the conductive state, the photoelectric conversion units PD**1** to PD**8** enter a non-accumulation state in which charges are not accumulated (i.e., reset state). When any of the transfer transistors M**1** to M**8** is in the conductive state and the reset transistor M**9** is in the non-conductive state, the pixel P(m, n) enters a readout state in which charges of the photoelectric conversion units PD**1** to PD**8** can be read out by transferring the charges to the floating diffusion FD. The reset of the photoelectric conversion units PD**1** to PD**8** may be controlled by a charge discharge transistor configured to electrically connect cathodes of the photoelectric conversion units PD**1** to PD**8** to a power line having a power potential.

[0064] In the present exemplary embodiment, each transistor is assumed to be an N-channel metal-oxide semiconductor (MOS) transistor, but may be a P-channel MOS transistor. In this case, the level of each control signal can be appropriately changed.

[0065] FIG. **4** is a block diagram illustrating a configuration of the control unit **2** according to the present exemplary embodiment. The control unit **2** includes a synchronization signal generation unit **421**, a vertical scanning control unit **423**, a column circuit control unit **424**, and a horizontal scanning control unit **25**.

[0066] In accordance with the control of the CPU **1**, the synchronization signal generation unit **421** generates a vertical synchronization signal and a horizontal synchronization signal to be used for the control of an operation timing of each component for readout scanning and reset scanning.

[0067] The vertical scanning control unit **423** generates a control signal for controlling the drive of the vertical scanning unit **3**, and outputs the generated control signal to the vertical scanning unit **3**. In accordance with a control signal from the vertical scanning control unit **423**, the vertical scanning unit **3** outputs a control signal RES, a control signal SEL, and control signals TX**1** to TX**8**. In some cases, an additional character indicating a row number is added to the control signals. Hereinafter, control signals to be output from the vertical scanning unit **3** will be collectively referred to as pixel drive pulses.

[0068] The column circuit control unit **424** generates a control signal for controlling the drive of the column circuit unit **5**, and outputs the generated control signal to the column circuit unit **5**. The horizontal scanning control unit **25** generates a control signal for controlling the drive of the horizontal scanning unit **6**, and outputs the generated control signal to the horizontal scanning unit **6**.

[0069] Next, a pixel drive pulse to be output from the vertical scanning unit **3** will be described with reference to FIG. **5**. FIG. **5** is a timing chart of a control signal to be output from the vertical scanning unit **3** according to the present exemplary embodiment. FIG. **5** selectively illustrates timings of pixel drive pulses corresponding to the pixels P of three rows including an (n−1)-th row, an n-th row, and an (n+1)-th row. Because the timings of pixel drive pulses of the (n−1)-th row and the (n+1)-th row are merely shifted in a time direction with respect to the timing of the n-th row, hereinafter, pixel drive pulses of the n-th row will be described, and the description of the other rows will be omitted.

[0070] In a period anterior to a time t**1**, the control signal RES[n] and the control signals TX**1**[*n*] to TX**8**[*n*] are maintained at the high level. The photoelectric conversion units PD**1** to PD**8** are accordingly maintained in the reset state. In addition, the control signal SEL [n] is maintained at the low level and the selection transistor M**11** is in the non-conductive state.

[0071] At the time t**1**, the control signals TX**1**[*n*] to TX**8**[*n*] transition to the low level. The reset state of the photoelectric conversion units PD**1** to PD**8** is thereby cancelled.

[0072] At a time t**2**, the control signal TX**1**[*n*] transitions to the high level, and the photoelectric conversion unit to which the control signal TX**1**[*n*] is input is once reset. After that, at the time t**3**, the control signal TX**1**[*n*] transitions to

the low level. By these operations, charge accumulation is started in the photoelectric conversion unit to which the control signal TX1[*n*] is input.

[0073] At a time t4, the control signal TX2[*n*] transitions to the high level, and the photoelectric conversion unit to which the control signal TX2[*n*] is input is once reset. After that, at the time t5, the control signal TX2[*n*] transitions to the low level. By these operations, charge accumulation is started in the photoelectric conversion unit to which the control signal TX2[*n*] is input.

[0074] During a period from a time t6 to a time t17, pulses of the control signals TX3[*n*] to TX8[*n*] are similarly output, and accumulation in the photoelectric conversion units is sequentially started. A series of operations from the time t2 to a time t17 is called reset scanning of the n-th row.

[0075] The length of a period from a time t17 immediately after the reset scanning of the n-th row, to a time t18 at which the next operation starts can be appropriately set. By adjusting the length of this period, it is possible to control the charge accumulation time of the photoelectric conversion units PD1 to PD8. The setting of the length of the period is made based on a control signal from the CPU 1, for example. FIG. 5 illustrates a case where the length of the period from the time t17 to the time t18 is the shortest.

[0076] At the time t18, the control signal SEL [n] transitions to the high level, and the selection transistor M11 enters the conductive state. The amplification transistor M10 of the pixel P(m, n) and the vertical output line Vline(m) are thereby electrically connected via the selection transistor M11.

[0077] By this operation, a state in which a signal that is based on the potential of the floating diffusion FD can be output to the vertical output line Vline(m) of an m-th column is caused.

[0078] During a time from the time t18 to a time t19, the control signal RES[n] transitions to the low level. The reset state of the floating diffusion FD is accordingly cancelled.

[0079] After the reset of the floating diffusion FD is cancelled, at the time t19, the control signal TX1[*n*] transitions to the high level. By this operation, charges accumulated in the photoelectric conversion unit to which the control signal TX1[*n*] is input are transferred to the floating diffusion FD. Then, a signal corresponding to the potential of the floating diffusion FD is output to the vertical output line Vline(m) on the m-th column. The signal output to the vertical output line Vline(m) is amplified and AD-converted in the column circuit unit 5, and then stored into the column memory as a digital signal.

[0080] After that, at a time t20, the control signal TX1[*n*] transitions to the low level. A transfer operation of charges accumulated in the photoelectric conversion unit is thereby completed. That is, a period from the time t3 to the time t20 corresponds to a charge accumulation period in the photoelectric conversion unit.

[0081] During a time from the time t20 to a time t21, the control signal RES[n] transitions to the high level, and after a predetermined time, transitions again to the low level. By this operation, the potential of the floating diffusion FD is reset.

[0082] At the time t21, the control signal TX2[*n*] transitions to the high level, and a transfer operation similar to that at the time t19 starts. After that, at a time t22, the control signal TX2[*n*] transitions to the low level, and a transfer operation of charges accumulated in the photoelectric conversion unit is completed.

[0083] During a period from a time t23 to a time t34, pulses of the control signals TX3[*n*] to TX8[*n*] are similarly output, and a transfer operation from the photoelectric conversion units to the floating diffusion FD is sequentially performed. A series of operations from the time t19 to a time t34 is called readout scanning of the n-th row.

[0084] At a time t35, the control signal SEL [n] transitions to the low level, and the selection transistor M11 enters the non-conductive state. Accordingly, the amplification transistor M10 of the pixel P and the vertical output line Vline(m) become electrically-disconnected.

[0085] At a time t36, the control signals TX1[*n*] to TX8[*n*] transition to the high level.

[0086] The photoelectric conversion units PD1 to PD8 accordingly enter the reset state. In the above-described manner, a series of operations from a charge accumulation start in the unit U on the n-th row to an end of the readout scanning of the n-th row are completed.

[0087] In this example, an operation of reading out signal charges one by one from the photoelectric conversion units PD1 to PD8 by individually controlling the control signals TX1[*n*] to TX8[*n*] has been described, but the operation is not limited to this operation.

[0088] For example, in the case of performing focus detection focused on a longitudinal direction of a subject, signals may be simultaneously read out from photoelectric conversion units PD neighboring in the row direction. In other words, the control signal TX1[*n*] and the control signal TX3[*n*] may be synchronized, and the control signal TX2[*n*] and the control signal TX4[*n*] may be synchronized. Alternatively, in the case of performing focus detection focused on a traverse direction of a subject, the control signal TX1[*n*] and the control signal TX2[*n*] may be synchronized, and the control signal TX3[*n*] and the control signal TX4[*n*] may be synchronized.

[0089] FIG. 6 is a configuration diagram of a photoelectric conversion apparatus according to the present exemplary embodiment. The photoelectric conversion apparatus according to the present exemplary embodiment has a structure of a stacked sensor in which a first substrate SUB1, which is a semiconductor substrate, and a second substrate SUB2 are stacked. The first substrate SUB1 is typically formed using a silicon single crystal. The second substrate SUB2 may also be formed using a silicon single crystal. Nevertheless, the material is not limited to this example, and the first substrate SUB1 and the second substrate SUB2 may be compound semiconductor substrates obtained by combining a plurality of materials. In other words, the first substrate SUB1 and the second substrate SUB2 can be various semiconductor substrates.

[0090] In addition, the arrangement of the members illustrated in FIG. 1, on the first substrate SUB1 and the second substrate SUB2 can be appropriately changed.

[0091] In addition, the photoelectric conversion apparatus according to the present exemplary embodiment is not limited to the stacked sensor. In other words, the photoelectric conversion apparatus according to the present exemplary embodiment may be a back-illuminated non-stacked sensor in which the second substrate SUB2 is used as a support substrate and all the members illustrated in FIG. 1 are arranged on the first substrate SUB1.

[0092] The pixel array **4** illustrated in FIG. **1** are arranged on the first substrate SUB**1**. On the other hand, among the components illustrated in FIG. **1**, members other than the pixel array **4** are arranged on the second substrate SUB**2**. Electrical connection between the first substrate SUB**1** and the second substrate SUB**2** can be established using a known method. For example, a via structure including a metal portion penetrating through the first substrate SUB**1** may be provided, and the via structure may connect a wire existing between the first substrate SUB**1** and a bonded surface with a wire existing between the second substrate SUB**2** and a bonded surface. This connection method is sometimes called through silicon via (TSV). As another configuration, an exposed metal bonding portion is provided inside an insulating film on the bonded surface on the side of the first substrate SUB**1**. This metal bonding portion is connected to the wire between the first substrate SUB**1** and the bonded surface. In a similar manner, an exposed metal bonding portion is provided inside an insulating film on the bonded surface on the side of the second substrate SUB**2**. This metal bonding portion is connected to the wire between the second substrate SUB**2** and the bonded surface. The metal bonding portions and the insulating films that are respectively provided on the bonded surface on the side of the first substrate SUB**1** and the bonded surface on the side of the second substrate SUB**2** are bonded. This can electrically connect the wire between the first substrate SUB**1** and the bonded surface, and the wire between the second substrate SUB**2** and the bonded surface. This connection method is sometimes called hybrid bonding.

[0093] FIG. **7** is a plan view illustrating a structure of the pixel P according to the present exemplary embodiment. This plan view is a planar view with respect to a first principal surface of the first substrate SUB**1**, which is a principal surface from which light enters.

[0094] The pixel P includes N-type semiconductor regions **11** to **14** that are respectively included in the photoelectric conversion units PD**1** to PD**4**. The photoelectric conversion unit PD**1** illustrated in FIG. **3** includes the semiconductor region **11**. In a similar manner, the photoelectric conversion units PD**2**, PD**3**, and PD**4** respectively include the semiconductor region **12**, the semiconductor region **13**, and the semiconductor region **14** in this order. In addition, the pixel P includes a trench portion **22** as a first trench portion that is an isolation portion in the pixel that electrically separates the N-type semiconductor regions **11** to **14**. In a planar view with respect to the first principal surface, the trench portion **22** includes a plurality of first portions SEP**1**-**1** and SEP**1**-**2** extending in a first direction, which is the row direction, and a plurality of second portions SEP**2**-**1** and SEP**2**-**2** extending in a second direction, which is the column direction.

[0095] The first direction and the second direction are directions intersecting with each other. On the first principal surface, a semiconductor region **23** of the first substrate SUB**1**, which is a semiconductor substrate, is provided in a first region between the first portions SEP**1**-**1** and SEP**1**-**2**, and in a second region between the second portions SEP**2**-**1** and SEP**2**-**2**. In the present exemplary embodiment, the first region and the second region can be considered as the same region. The first region is a region between one and the other of a plurality of first portions SEP**1**-**1** and SEP**1**-**2**. The second region is a region between one and the other of a plurality of second portions SEP**2**-**1** and SEP**2**-**2**.

[0096] In a planar view with respect to the first principal surface, a part of the trench portion **22** provided inside the first substrate SUB**1** is provided at a position overlapping the semiconductor region **23**. The semiconductor region **23** serves as a pathway on which charges move from one N-type semiconductor region to the other N-type semiconductor region of a plurality of N-type semiconductor regions **11** to **14**.

[0097] With this configuration, even in a case where a large amount of charges are generated inside some of the semiconductor regions **11** to **14** to which high-brightness light enters, among the plurality of N-type semiconductor regions **11** to **14**, charges can be moved to the other semiconductor regions **11** to **14**. With this configuration, because charges corresponding to incident light can be accumulated using a plurality of semiconductor regions **11** to **14**, it is possible to expand a dynamic range on a high brightness side. In particular, it is possible to expand a dynamic range on a high brightness side while suppressing a deterioration in linearity of an output signal of the pixel P with respect to an incident light amount.

[0098] Because the semiconductor region **23** is a moving pathway of charges generated by the plurality of semiconductor regions **11** to **14**, the conductivity type of the semiconductor region **23** is desirably set to the same conductivity type as the conductivity type of the plurality of semiconductor regions **11** to **14**.

[0099] A semiconductor region with a conductivity type different from the conductivity type of the semiconductor regions **11** to **14** may be provided between the semiconductor region **23** and the trench portion **22**. In other words, among conductivity types described in the present exemplary embodiment, a P-type semiconductor region may be provided. This P-type semiconductor region has a role of reducing inflow of dark current components generated by the trench portion **22**, into the semiconductor regions **11** to **14**.

[0100] A trench portion **21** is provided between a plurality of pixels P as a second trench portion being an isolation portion between one pixel and the other pixel. The trench portion **21** includes a portion extending in the first direction, which is the row direction, and a portion extending in the second direction, which is the column direction, in a planar view with respect to the first principal surface. The trench portion **21** extends over pixels P of a plurality of rows and a plurality of columns in a planar view with respect to the first principal surface.

[0101] A microlens ML is arranged at a position overlapping the N-type semiconductor regions **11** to **14** arranged in two rows and two columns in one pixel P, in a planar view with respect to the first principal surface. The photoelectric conversion apparatus includes a microlens array in which the microlenses ML are arranged respectively corresponding to a plurality of pixels P. Light having passed through one microlens ML enters the four N-type semiconductor regions **11** to **14**. By having this configuration, it is possible to individually acquire a signal that is based on a light amount of light that has entered each of the photoelectric conversion units PD**1** to PD**4**, by the drive of the timing chart illustrated in FIG. **5**. It is possible to acquire a phase difference component in the row direction and a phase difference component in the column direction. With this configuration, it is possible to perform focus detection focused on the

longitudinal direction of the subject, and focus detection focused on the traverse direction.

[0102] Next, FIG. **8** illustrates a cross-sectional view taken along a line A-A' illustrated in FIG. **7**.

[0103] Among members illustrated in FIG. **8**, the same members as the members illustrated in FIG. **7** are assigned the same reference numerals as those used in FIG. **7**. The first substrate SUB**1** has a first principal surface F**1**, which is a first principal surface from which light enters, and a second principal surface F**2**, which is a principal surface facing the first principal surface F**1**. An insulating film **31** is provided on the second principal surface F**2**. A wiring layer **30** including a wire **32** is provided in the insulating film **31**. The second principal surface F**2** also serves as a surface on which a gate electrode of each transistor illustrated in FIG. **3** is provided, which is not illustrated in FIG. **8**.

[0104] A color filter **52** and an insulating film **51** are provided between the first principal surface F**1** and the microlens ML. An optical layer **50** includes the microlens ML, the color filter **52**, and the insulating film **51**.

[0105] In a cross-sectional view at a position passing through the line A-A' illustrated in FIG. **7**, the trench portion **21** and the trench portion **22** both extend from one surface to the other surface of the first principal surface F**1** and the second principal surface F**2** of the first substrate SUB**1** in a depth direction of the first substrate SUB**1**. The trench portion **21** and the trench portion **22** are both in contact with an element isolation portion **24** on the side of the second principal surface F**2**. The element isolation portion **24** has a structure also called a shallow trench isolation (STI). This STI can be created by a known manufacturing method. Then, by performing etching processing from the formed element isolation portion **24**, a hole portion is formed up to the depth of the first principal surface F**1**. Then, by filling this hole portion with an insulating material, a metal material, or polysilicon, it is possible to form the trench portions **21** and **22**. On a side wall of the trench portion **21** or **22**, a pinning film may be provided as a single-layer aluminum oxide film or tantalum oxide film, or a film stack obtained by combining films. In the present exemplary embodiment, the trench portions **21** and the trench portion **22** have a structure of a deep trench isolation (DTI) formed from the second principal surface F**2** toward the first principal surface F**1**. In the cross section illustrated in FIG. **8**, the trench portions **21** and the trench portion **22** are formed with the same width W**1**. In FIG. **8**, the trench portions **21** and **22** both extend from the second principal surface F**2** to the first principal surface F**1** with the same width, but the configuration is not limited to this configuration. Both the trench portions **21** and **22** can be formed to become thinner toward the first principal surface F**1**.

[0106] A length L**1** in the first direction of the semiconductor region **23** is desirably set to a length equal to or smaller than a half of a length L**2** in the first direction of the pixel P. For example, if the length L**2** of the pixel P is 1 μm, the length L**1** in the first direction of the semiconductor region **23** is set to 0.5 μm or less. With this configuration, it is possible to achieve at least one of electric separation and optical separation of the photoelectric conversion units PD**1** to PD**4**, and the efficiency of charge movement to other photoelectric conversion units PD in a case where a part of photoelectric conversion unit PD of the photoelectric conversion units PD**1** to PD**4** is saturated.

[0107] Next, FIG. **9** illustrates a cross-sectional view taken along a line B-B' illustrated in FIG. **7**. Among members illustrated in FIG. **9**, the same members as the members illustrated in FIGS. **7** and **8** are assigned the same reference numerals as those used in FIGS. **7** and **8**.

[0108] In the cross-sectional view illustrated in FIG. **9**, a bottom portion of the trench portion **22** has contact with the semiconductor region **23**. In other words, the bottom portion of the trench portion **22** exists at a depth position between the second principal surface F**2** and the first principal surface F**1**. A width of the trench portion **22** is a width W**2** smaller than the width W**1** of the trench portion **21**. By making the width of the trench portion **22** smaller, it is possible to reduce an etching rate at the time of etching of a semiconductor substrate in forming the trench portion **22**.

[0109] Next, FIG. **10** illustrates a cross-sectional view taken along a line C-C' illustrated in FIG. **7**. Among members illustrated in FIG. **10**, the same members as the members illustrated in FIGS. **7**, **8**, and **9** are assigned the same reference numerals as those used in FIGS. **7**, **8**, and **9**.

[0110] In FIG. **10**, the semiconductor region **23** is formed at a position between the first portions SEP**1-1** and SEP**1-2** illustrated in FIG. **7**. The trench portion **22** is provided between the semiconductor region **23** and the second principal surface F**2**.

[0111] Next, FIG. **11** illustrates a cross-sectional view taken along a line D-D' illustrated in FIG. **7**. Among members illustrated in FIG. **11**, the same members as the members illustrated in FIGS. **7** to **10** are assigned the same reference numerals as those used in FIGS. **7** to **10**.

[0112] A length DP**1** in the depth direction of the semiconductor region **23** is desirably set to ½ or less of a length DP**2** between the first principal surface F**1** and the second principal surface F**2**. For example, in a case where the length DP**2** is 3 μm, it is desirable to set the length DP**1** to 1.5 μm or less. With this configuration, it is possible to achieve at least one of electric separation and optical separation of the photoelectric conversion units PD**1** to PD**4**, and the efficiency of charge movement to other photoelectric conversion units PD in a case where a part of photoelectric conversion unit PD of the photoelectric conversion units PD**1** to PD**4** is saturated.

[0113] In the cross-sectional view illustrated in FIG. **11**, the trench portion **21** extends over a plurality of pixels P. The trench portion **21** extends from one surface to the other surface of the first principal surface F**1** and the second principal surface F**2** in the depth direction.

[0114] In a planar view with respect to the first principal surface F**1**, the structure described in the present exemplary embodiment forms the semiconductor region **23** in a region that is between the first portions SEP**1-1** and SEP**1-2** and between the first portions SEP**2-1** and SEP**2-2**, the portions being a part of the trench portion **22**. With this configuration, as described above, it is possible to expand a dynamic range on a high brightness side. In particular, it is possible to expand a dynamic range on a high brightness side while suppressing a deterioration in linearity of an output signal of the pixel P with respect to an incident light amount.

[0115] A second exemplary embodiment will be described mainly based on a difference from the first exemplary embodiment.

[0116] FIG. **12** is a plan view with respect to the first principal surface F**1** that illustrates a photoelectric conversion apparatus according to the present exemplary embodi-

ment. In the first exemplary embodiment, the semiconductor region **23** is provided at a position overlapping a central portion of the microlens ML in a planar view. When viewed from another perspective, in the first exemplary embodiment, one semiconductor region **23** is connected with all the semiconductor regions **11** to **14** in two rows and two columns. In the present exemplary embodiment, a plurality of semiconductor regions **23** is provided in one pixel P. In the example illustrated in FIG. **12**, the semiconductor region **23** connecting two semiconductor regions of the N-type semiconductor regions **11** to **14** is provided.

[0117] The trench portion **22** includes portions SEP**3-1**, SEP**3-2**, SEP**3-3**, and SEP**3-4** in the first direction. The trench portion **22** also includes portions SEP**4-1**, SEP**4-2**, SEP**4-3**, and SEP**4-4** in the second direction. The semiconductor regions **23** are provided in a first region between the portions SEP**3-1** and SEP**3-2**, in a second region between the portions SEP**3-3** and SEP**3-4**, in a third region between portions SEP**4-1** and SEP**4-2**, and in a fourth region between he portions SEP**4-3** and SEP**4-4**.

[0118] FIG. **13** illustrates a cross-sectional view taken along a line C**1**-C**2** illustrated in FIG. **12**. Among members illustrated in FIG. **13**, the same members as the members illustrated in FIGS. **7** to **10** are assigned the same reference numerals as those used in FIGS. **7** to **10**. As illustrated in FIG. **13**, by providing a plurality of semiconductor regions **23**, it is possible to improve the directionality of charges generated by a plurality of N-type semiconductor regions **11** to **14**.

[0119] A third exemplary embodiment will be described mainly based on a difference from the first exemplary embodiment. In the first exemplary embodiment, the trench portions **21** and **22** are formed in a direction from the second principal surface F**2** toward the first principal surface F**1**. In the present exemplary embodiment, trench portions **21** and **22** are formed in a direction from the first principal surface F**1** toward the second principal surface F**2**. While the semiconductor region **23** is provided on the first principal surface F**1** in the first exemplary embodiment, the semiconductor region **23** is provided on the second principal surface F**2** in the present exemplary embodiment. Also in the present exemplary embodiment, photoelectric conversion units PD**1** to PD**4** arranged on two rows and two columns are arranged for one microlens.

[0120] FIG. **14** is a plan view illustrating a structure of a photoelectric conversion apparatus according to the present exemplary embodiment in a planar view with respect to the second principal surface F**2**. Among members illustrated in FIG. **14**, the same members as the members illustrated in FIG. **7** are assigned the same reference numerals as those used in FIG. **7**.

[0121] On the second principal surface F**2**, in a planar view with respect to the second principal surface F**2**, the trench portion **22** includes portions SEP**5-1** and SEP**5-2** extending in the first direction, which is the row direction, and portions SEP**6-1** and SEP**6-2** extending in the second direction, which is the column direction. On the second principal surface F**2**, the semiconductor region **23** of the first substrate SUB**1**, which is a semiconductor substrate, is provided in a region that is between the portions SEP**5-1** and SEP**5-2**, and between the second portions SEP**6-1** and SEP**6-2**. In a planar view with respect to the second principal surface F**2**, a part of the trench portion **22** provided inside the first substrate SUB**1** is provided at a position overlapping the semiconductor region **23**. The semiconductor region **23** serves as a pathway on which charges move from one N-type semiconductor region to the other N-type semiconductor region of a plurality of N-type semiconductor regions **11** to **14**. With this configuration, even in a case where a large amount of charges are generated inside a part of semiconductor regions **11** to **14** to which high-brightness light, among the plurality of N-type semiconductor regions **11** to **14**, charges can be moved to the other semiconductor regions **11** to **14**. With this configuration, because charges corresponding to incident light can be accumulated using a plurality of semiconductor regions **11** to **14**, it is possible to expand a dynamic range on a high brightness side. In particular, it is possible to expand a dynamic range on a high brightness side while suppressing a deterioration in linearity of an output signal of the pixel P with respect to an incident light amount.

[0122] Next, FIG. **15** illustrates a cross-sectional view taken along a line A-A' illustrated in FIG. **14**.

[0123] Among members illustrated in FIG. **15**, the same members as the members illustrated in FIG. **14** are assigned the same reference numerals as those used in FIG. **14**.

[0124] In a cross-sectional view at a position passing through the line A-A' illustrated in FIG. **15**, the trench portion **21** and the trench portion **22** both extend from one surface to the other surface of the first principal surface F**1** and the second principal surface F**2** of the first substrate SUB**1** in a depth direction of the first substrate SUB**1**. After the wiring layer **30** is formed, in a process before the optical layer **50** is formed, by performing etching processing from the first principal surface F**1** toward the second principal surface F**2**, a hole portion is formed up to the depth of the second principal surface F**2**. Then, by filling this hole portion with an insulating material or a metal material, it is possible to form the trench portions **21** and **22**. In the present exemplary embodiment, the trench portions **21** and the trench portion **22** have a structure of a DTI formed from the first principal surface F**1** toward the second principal surface F**2**. In the cross section illustrated in FIG. **15**, the trench portions **21** and the trench portion **22** are formed with the same width W**1**. In FIG. **15**, the trench portions **21** and **22** both extend from the second principal surface F**2** to the first principal surface F**1** with the same width, but the configuration is not limited to this configuration. Both the trench portions **21** and **22** can be formed to become thinner toward the second principal surface F**2**.

[0125] Next, FIG. **16** illustrates a cross-sectional view taken along line B-B' illustrated in FIG. **14**. Among members illustrated in FIG. **16**, the same members as the members illustrated in FIGS. **14** and **15** are assigned the same reference numerals as those used in FIGS. **14** and **15**.

[0126] In the cross-sectional view illustrated in FIG. **16**, a bottom portion of the trench portion **22** is in contact with the semiconductor region **23**. In other words, the bottom portion of the trench portion **22** exists at a depth position between the second principal surface F**2** and the first principal surface F**1**. A width of the trench portion **22** is a width W**2** smaller than the width W**1** of the trench portion **21**. In FIG. **16**, the widths W**1** and W**2** are illustrated at different depth positions for the sake of illustration, but it is desirable to compare the widths W**1** and W**2** at the same depth position.

[0127] FIG. **17** illustrates a cross-sectional view taken along line C-C' illustrated in FIG. **14**. Among members illustrated in FIG. **17**, the same members as the members

illustrated in FIGS. **14** to **16** are assigned the same reference numerals as those used in FIGS. **14** to **16**.

[0128] In FIG. **17**, the semiconductor region **23** is formed at a position between the portions SEP**5-1** and SEP**5-2** illustrated in FIG. **14**. The trench portion **22** is provided between the semiconductor region **23** and the first principal surface F**1**.

[0129] It is desirable to set a length DP**3** in the depth direction of the semiconductor region **23** to ½ or less of the length DP**2** between the first principal surface F**1** and the second principal surface F**2**. For example, in a case where the length DP**2** is 3 μm, it is desirable to set the length DP**3** to 1.5 μm or less. With this configuration, it is possible to achieve at least one of electric separation and optical separation of the photoelectric conversion units PD**1** to PD**4**, and the efficiency of charge movement to other photoelectric conversion units PD in a case where a part of photoelectric conversion unit PD of the photoelectric conversion units PD**1** to PD**4** is saturated.

[0130] FIG. **18** illustrates a cross-sectional view taken along line D-D' illustrated in FIG. **14**. Among members illustrated in FIG. **18**, the same members as the members illustrated in FIGS. **14** to **17** are assigned the same reference numerals as those used in FIGS. **14** to **17**.

[0131] In the cross-sectional view illustrated in FIG. **18**, the trench portion **21** extends over a plurality of pixels P. The trench portion **21** extends from one surface to the other surface of the first principal surface F**1** and the second principal surface F**2** in the depth direction.

[0132] In a planar view with respect to the second principal surface F**2**, the structure described in the present exemplary embodiment forms the semiconductor region **23** in a region that is between the portions SEP**5-1** and SEP**5-2** and between the portions SEP**6-1** and SEP**6-2**, the portions being a part of the trench portion **22**. With this configuration, as described above, it is possible to expand a dynamic range on a high brightness side. In particular, it is possible to expand a dynamic range on a high brightness side while suppressing a deterioration in linearity of an output signal of the pixel P with respect to an incident light amount.

[0133] A photoelectric conversion apparatus according to a fourth exemplary embodiment will be described mainly based on a difference from the third exemplary embodiment.

[0134] FIG. **19** is a plan view of a photoelectric conversion apparatus according to the present exemplary embodiment with respect to the second principal surface F**2**. In the third exemplary embodiment, one semiconductor region **23** is connected with all the semiconductor regions **11** to **14** in two rows and two columns. In the present exemplary embodiment, a plurality of semiconductor regions **23** is provided in one pixel P. In the example illustrated in FIG. **19**, the semiconductor region **23** connecting two semiconductor regions of the N-type semiconductor regions **11** to **14** is provided.

[0135] The trench portion **22** includes portions SEP**6-1**, SEP**6-2**, SEP**6-3**, and SEP**6-4** in the first direction. The trench portion **22** also includes portions SEP**7-1**, SEP**7-2**, SEP**7-3**, and SEP**7-4** in the second direction. The semiconductor regions **23** are provided in a region between the portions SEP**6-1** and the SEP**6-2**, in a region between the portions SEP**6-3** and the SEP**6-4**, in a region between the portions SEP**7-1** and the SEP**7-2**, and in region between the portions SEP**7-3** and the SEP**7-4**.

[0136] FIG. **20** illustrates a cross-sectional view taken along a line C**3**-C**4** illustrated in FIG. **19**. Among members illustrated in FIG. **20**, the same members as the members illustrated in FIGS. **16** to **19** are assigned the same reference numerals as those used in FIGS. **16** to **19**. As illustrated in FIG. **20**, by providing a plurality of semiconductor regions **23**, it is possible to improve the directionality of charges generated by a plurality of N-type semiconductor regions **11** to **14**.

[0137] A photoelectric conversion apparatus according to a fifth exemplary embodiment will be described mainly based on a difference from the third exemplary embodiment.

[0138] In the photoelectric conversion apparatus according to the present exemplary embodiment, each of the trench portions **21** and **22** includes a portion extending from the first principal surface F**1**, and a portion extending from the second principal surface F**2**.

[0139] FIGS. **21**A and **21**B illustrate the photoelectric conversion apparatus according to the present exemplary embodiment. FIG. **21**A is a plan view viewed in a planar view with respect to the second principal surface F**2**, and FIG. **21**B is a plan view viewed in a planar view with respect to the first principal surface F**1**. Among members illustrated in FIGS. **21**A and **21**B, members having the same function as the members described in the above-described exemplary embodiments are assigned the same reference numerals as those used in the above-described exemplary embodiments. In the photoelectric conversion apparatus according to the present exemplary embodiment, a trench portion **21***a* is provided on the second principal surface F**2** in a grid shape. A trench portion **21***b* is provided on the first principal surface F**1** in a grid shape.

[0140] FIG. **22** is a plan view of a planar view with respect to a plane at a depth position between the second principal surface F**2** and the first principal surface F**1** (plane parallel to the first principal surface F**1** and the second principal surface F**2**). The depth position is a position at a depth D**1** illustrated in FIGS. **23** to **25** to be described below.

[0141] In a planar view with respect to the first principal surface, the trench portion **22***a* includes portions SEP**8-1** and SEP**8-2** extending in the first direction, which is the row direction, and portions SEP**9-1** and SEP**9-2** extending in the second direction, which is the column direction. On the first principal surface, the semiconductor region **23** of the first substrate SUB**1**, which is a semiconductor substrate, is provided in a region that is between the portions SEP**8-1** and SEP**8-2**, and between the portions SEP**9-1** and SEP**9-2**. In a planar view with respect to the first principal surface, a part of the trench portion **22***a* provided inside the first substrate SUB**1** is provided at a position overlapping the semiconductor region **23**. The semiconductor region **23** serves as a pathway on which charges move from one N-type semiconductor region to the other N-type semiconductor region of a plurality of N-type semiconductor regions **11** to **14**. With this configuration, even in a case where a large amount of charges are generated inside partial semiconductor regions **11** to **14** to which high-brightness light enters, among the plurality of N-type semiconductor regions **11** to **14**, charges can be moved to the other semiconductor regions **11** to **14**. With this configuration, because charges corresponding to incident light can be accumulated using a plurality of semiconductor regions **11** to **14**, it is possible to expand a dynamic range on a high brightness side. In particular, it is possible to expand a dynamic range on a high brightness side

while suppressing a deterioration in linearity of an output signal of the pixel P with respect to an incident light amount.

[0142] FIG. **23** is a cross-sectional view taken along a line A-A' illustrated in FIGS. **21**A, **21**B, and **22**. The trench portion **21** includes the trench portion **21***a* extending from the second principal surface F**2** toward the first principal surface F**1**, and the trench portion **21***b* extending from the first principal surface F**1** toward the second principal surface F**2**, and the trench portion **21***a* and the trench portion **21***b* are in contact with each other inside the first substrate SUB**1**. Lengths by which the trench portion **21***a* and the trench portion **21***b* extend in the depth direction can be appropriately set depending on their process conditions. Typically, it is possible to set the length to a length of M/2 with respect to a length M in the depth direction from the first principal surface F**1** to the second principal surface F**2**. FIG. **23** illustrates the trench portion **21***a* and the trench portion **21***b* in such a manner that their bottom surfaces are in contact with each other, but the configuration is not limited to this example. For example, at the time of formation of the trench portion **21***b*, a structural object (metal, an insulating material, polysilicon, etc.) inside the trench portion **21***a* may be caused to function as an etching stop, and a bottom surface of the trench portion **21***b* may be positioned inside the trench portion **21***a*. In this manner, by the trench portion **21***a* and the trench portion **21***b* being in contact with each other, it is possible to appropriately perform at least one of electric separation and optical separation between a plurality of pixels P.

[0143] The trench portion **22** includes the trench portion **22***a* extending from the second principal surface F**2** toward the first principal surface F**1**, and the trench portion **22***b* extending from the first principal surface F**1** toward the second principal surface F**2**. The trench portion **22***a* and the trench portion **22***b* are in contact with each other inside the first substrate SUB**1**. Lengths by which the trench portion **22***a* and the trench portion **22***b* extend in the depth direction can be appropriately set depending on their process conditions. Typically, it is possible to set the length to a length of M/2 with respect to the length M in the depth direction from the first principal surface F**1** to the second principal surface F**2**. FIG. **23** illustrates the trench portion **22***a* and the trench portion **22***b* in such a manner that their bottom surfaces are in contact with each other, but the configuration is not limited to this example. For example, at the time of formation of the trench portion **22***b*, a structural object (metal, an insulating material, polysilicon, etc.) inside the trench portion **22***a* may be caused to function as an etching stop, and a bottom surface of the trench portion **22***b* may be positioned inside the trench portion **22***a*. In this manner, by the trench portion **22***a* and the trench portion **22***b* being contact with each other, it is possible to appropriately perform at least one of electric separation and optical separation between the photoelectric conversion units PD**1** to PD**4** included in one pixel P.

[0144] A width W**6** of the trench portion **21***a* is wider than a width W**5** of the trench portion **21***b*. The widths of the trench portion **21***a* and **22***a* are assumed to be the same width W**6**, but widths are not limited to the widths in this example, and the widths may be made different. In addition, the widths of the trench portion **21***a* and **22***a* are assumed to be the same width W**5**, but widths are not limited to the widths in this example, and the widths may be made different.

[0145] FIG. **24** is a cross-sectional view taken along a line B-B' illustrated in FIGS. **21**A, **21**B, and **22**. The trench portion **22***a* extends up to a position shallower than the depth position D**1** when viewed from the second principal surface F**2**. The bottom surface of the trench portion **22***a* is in contact with the semiconductor region **23**. The bottom surface of the trench portion **22***b* is in contact with the semiconductor region **23**. In other words, the trench portion **22***a* and the trench portion **22***b* are not in contact with each other. In addition, a width W**7** of the trench portion **22***a* is smaller than the width W**6** of the trench portion **21***a*. In addition, a width W**8** of the trench portion **22***b* is smaller than the width W**5** of the trench portion **21***b*. A relationship between the widths W**5** to W**8** in the present exemplary embodiment is represented by the following formula.

$$W6>W5>W7>W8 \tag{1}$$

[0146] The relationship is not limited to the relationship represented by Formula (1), and the widths W**5** to W**8** are only required to satisfy the relationship of W**6**>W**7** and the relationship of W**5** >W**8**. In other words, the relationship may be a relationship represented by any of the formulae (2) to (4).

$$W6=W5>W7=W8 \tag{2}$$

$$W5>W6>W7=W8 \tag{3}$$

$$W5>W6>W8>W7 \tag{4}$$

[0147] In FIG. **24**, the widths W**6** and W**7** are illustrated at different depth positions for the sake of illustration, but it is desirable to compare the widths W**6** and W**7** at the same depth position. Similarly, the widths W**5** and W**8** are illustrated at different depth positions for the sake of illustration, but it is desirable to compare the widths W**5** and W**8** at the same depth position.

[0148] As seen from the illustration in FIGS. **21**A, **21**B, and **24**, on the first principal surface F**1**, in a planar view with respect to the first principal surface F**1**, a first trench portion **22** includes the trench portion **22***b*, which is a first portion extending in the first direction. In addition, on the second principal surface F**2**, in a planar view with respect to the second principal surface F**2**, the first trench portion **22** includes the trench portion **22***a*, which is a third portion extending in the first direction. The trench portion **22***a* and the trench portion **22***b* include portions overlapping in a planar view with respect to the first principal surface F**1**. The semiconductor region **23** of the first substrate SUB**1** is provided between the trench portion **22***a* and the trench portion **22***b*.

[0149] FIG. **25** is a cross-sectional view taken along a line C-C' illustrated in FIGS. **21**A, **21**B, and **22**. In this cross-sectional view, the semiconductor region **23** is arranged in a region surrounded by the trench portion **22***a* and the trench portion **22***b*. In addition, a portion of the semiconductor region **23** is arranged at a position between the portions SEP**8-1** and SEP**8-2** illustrated in FIG. **22**. With this structure, it is possible to move charges to other photoelectric conversion units PD in a case where a part of photoelectric conversion unit PD of the photoelectric conversion units PD**1** to PD**4** is saturated.

[0150] It is desirable to set a length DP**4** in the depth direction of the semiconductor region **23** to ½ or less of the length DP**2** between the first principal surface F**1** and the second principal surface F**2**. For example, in a case where

the length DP**2** is 3 μm, it is desirable to set the length DP**4** to 1.5 μm or less. With this configuration, it is possible to achieve at least one of electric separation and optical separation of the photoelectric conversion units PD**1** to PD**4**, and the efficiency of charge movement to other photoelectric conversion units PD in a case where a part of photoelectric conversion unit PD of the photoelectric conversion units PD**1** to PD**4** is saturated.

[0151] FIG. **26** is a cross-sectional view taken along a line D-D' illustrated in FIGS. **21**A, **21**B, and **22**. The trench portion **21***a* and the trench portion **21***b* are in contact with each other, and extend over a plurality of pixels P. With this configuration, it is possible to electrically separate photoelectric conversion units of a plurality of pixels P from each other.

[0152] Also in the present exemplary embodiment, it is possible to expand a dynamic range on a high brightness side. In particular, it is possible to expand a dynamic range on a high brightness side while suppressing a deterioration in linearity of an output signal of the pixel P with respect to an incident light amount.

[0153] The structure in the present exemplary embodiment can be modified to the structure illustrated in FIG. **27**. FIG. **27** is a plan view of a planar view with respect to the plane at the depth position D**1** (plane parallel to the first principal surface F**1** and the second principal surface F**2**).

[0154] In this modified example, a configuration is modified to a configuration in which a plurality of semiconductor regions **23** of the present exemplary embodiment is arranged as in the second exemplary embodiment and the fourth exemplary embodiment. With this configuration, it is possible to add the directionality to a moving direction of charges of the semiconductor regions **11** to **14**.

[0155] A sixth exemplary embodiment can be applied to any of the first to fifth exemplary embodiments. FIG. **28**A is a schematic diagram illustrating a device **9191** including a semiconductor apparatus **930** according to the present exemplary embodiment. As the semiconductor apparatus **930**, the photoelectric conversion apparatus (imaging apparatus) according to each of the above-described exemplary embodiments can be used. The device **9191** including the semiconductor apparatus **930** will be described in detail. The semiconductor apparatus **930** can include a semiconductor device **910**. Aside from the semiconductor device **910**, the semiconductor apparatus **930** can include a package **920** storing the semiconductor device **910**. The package **920** can include a base member on which the semiconductor device **910** is fixed, and a lid member such as glass facing the semiconductor device **910**. The package **920** can further include a bonding member such as a bonding wire or a bump that connects a terminal provided in the base member and a terminal provided in the semiconductor device **910**.

[0156] The device **9191** can include at least any of an optical device **940**, a control device **950**, a processing device **960**, a display device **970**, a storage device **980**, and a mechanical device **990**. The optical device **940** corresponds to the semiconductor apparatus **930**. The optical device **940** is a lens, a shutter, or a mirror, for example, and includes an optical system for guiding light to the semiconductor apparatus **930**. The control device **950** controls the semiconductor apparatus **930**. The control device **950** is a semiconductor apparatus such as an application specific integrated circuit (ASIC), for example.

[0157] The processing device **960** processes a signal output from the semiconductor apparatus **930**. The processing device **960** is a semiconductor apparatus such as a CPU or an ASIC for forming an analog front end (AFE) or a digital front end (DFE). The display device **970** is an electroluminescent (EL) display device or a liquid crystal display device that displays information (image) obtained in the semiconductor apparatus **930**. The storage device **980** is a magnetic device or a semiconductor device that stores information (image) obtained in the semiconductor apparatus **930**. The storage device **980** is a volatile memory such as a static random access memory (SRAM) or a dynamic random access memory (DRAM), or a nonvolatile memory such as a flash memory or a hard disk drive.

[0158] The mechanical device **990** includes a moving unit or a propulsion unit such as a motor or an engine. In the device **9191**, a signal output from the semiconductor apparatus **930** is displayed on the display device **970**, and transmitted to the outside by a communication device (not illustrated) included in the device **9191**. For this reason, the device **9191** desirably further includes the storage device **980** and the processing device **960** aside from a storage circuit and a calculation circuit included in the semiconductor apparatus **930**. The mechanical device **990** may be controlled based on a signal output from the semiconductor apparatus **930**.

[0159] The device **9191** is suitable for an electronic device such as an information terminal having an image capturing function (e.g., smartphone or wearable terminal) or a camera (e.g., interchangeable lens camera, compact camera, video camera, monitoring camera). The mechanical device **990** in a camera can drive the component of the optical device **940** for zooming, focusing, or a shutter operation. Alternatively, the mechanical device **990** in a camera can move the semiconductor apparatus **930** for an image stabilization operation.

[0160] The device **9191** can be a transport device such as a vehicle, a ship, or a flight vehicle (drone, airplane, etc.). The mechanical device **990** in a transport device can be used as a moving device. The device **9191** serving as a transport device is suitable for a device that transports the semiconductor apparatus **930**, or a device that aids and/or automates driving (steering) using an image capturing function. The processing device **960** for aiding and/or automating driving (steering) can perform processing for operating the mechanical device **990** serving as a moving device, based on information obtained in the semiconductor apparatus **930**. Alternatively, the device **9191** may be a medical device such as an endoscope, a measuring device such as a distance measuring sensor, an analytical device such as an electronic microscope, an office device such as a copier, or an industrial device such as a robot.

[0161] According to the above-described exemplary embodiment, it becomes possible to obtain good pixel characteristics. Accordingly, it is possible to enhance the value of the semiconductor apparatus. The enhancement of the value corresponds to at least any of the addition of a function, performance improvement, characteristic improvement, reliability improvement, manufacturing yield ratio improvement, environmental burden reduction, cost reduction, downsizing, and weight saving.

[0162] Accordingly, if the semiconductor apparatus **930** according to the present exemplary embodiment is used in the device **9191**, the value of the device **9191** can also be

enhanced. For example, by mounting the semiconductor apparatus **930** on a transport device, it is possible to obtain superior performance when performing the image capturing of the outside of the transport device or the measuring of an external environment. Thus, determining to mount the semiconductor apparatus according to the present exemplary embodiment on a transport device when manufacturing and selling the transport device is advantageous in improving the performance of the transport device itself. The semiconductor apparatus **930** is suitable especially for a transport device that performs drive assist and/or automatic operation of the transport device using information obtained by the semiconductor apparatus.

[0163] A photoelectric conversion system and a movable body according to the present exemplary embodiment will be described with reference to FIGS. **28**B and **28**C.

[0164] FIG. **28**B illustrates an example of a photoelectric conversion system related to an in-vehicle camera. A photoelectric conversion system S**8** includes a photoelectric conversion apparatus **80**. The photoelectric conversion apparatus **80** is the photoelectric conversion apparatus (imaging apparatus) according to any of the above-described exemplary embodiments. The photoelectric conversion system S**8** includes an image processing unit **801** that performs image processing on a plurality of pieces of image data acquired by the photoelectric conversion apparatus **80**, and a parallax acquisition unit **802** that calculates a parallax (phase difference between parallax images) from the plurality of pieces of image data acquired by the photoelectric conversion system S**8**.

[0165] Here, the photoelectric conversion system S**8** may include an optical system (not illustrated) such as a lens, a shutter, or a mirror, for example, that guides light to the photoelectric conversion apparatus **80**. A plurality of photoelectric conversion units approximately conjugate with a pupil of the optical system may be arranged in pixels included in photoelectric conversion apparatus **80**. For example, the plurality of photoelectric conversion units approximately conjugate with the pupil are arranged in such a manner as to correspond to one microlens. By the plurality of photoelectric conversion units receiving light beams having passed through mutually-different position of the pupil of the optical system, the photoelectric conversion apparatus **80** outputs image data corresponding to the light beams having passed through the different positions. Then, the parallax acquisition unit **802** may calculate a parallax using the output image data. The photoelectric conversion system S**8** further includes a distance acquisition unit **803** that calculates a distance to a target object based on the calculated parallax, and a collision determination unit **804** that determines whether collision is likely to occur, based on the calculated distance. In this example, the parallax acquisition unit **802** and the distance acquisition unit **803** serve as an example of a distance information acquisition unit that acquires distance information regarding a distance to a target object. More specifically, the distance information is information regarding a parallax, a defocus amount, and a distance to a target object. The collision determination unit **804** may determine collision likelihood using any of these pieces of distance information. The distance Information may be acquired using a ToF sensor. The distance information acquisition unit may be implemented by dedicatedly-designed hardware, or may be implemented by a software module. Alternatively, the distance information acquisition unit may be implemented by a field programmable gate array (FPGA) or an application specific integrated circuit (ASIC), or may be implemented by the combination of these. The photoelectric conversion system S**8** is connected with a vehicle information acquisition apparatus **810**, and can acquire vehicle information such as a vehicle speed, a yaw rate, or a rudder angle. In addition, an electronic control unit (ECU) **820** is connected to the photoelectric conversion system S**8**. The ECU **820** serves as a control apparatus that outputs a control signal for generating braking force, to a vehicle based on a determination result obtained by the collision determination unit **804**. The photoelectric conversion system S**8** is also connected with an alarm apparatus **830** that raises an alarm to a driver based on a determination result obtained by the collision determination unit **804**. For example, in a case where the determination result obtained by the collision determination unit **804** indicates high collision likelihood, the ECU **820** performs vehicle control for avoiding collision or reducing damages by braking, releasing an accelerator, or suppressing engine output. The alarm apparatus **830** issues an alarm to a user by sounding an alarm, displaying warning information on a screen of a car navigation system, or vibrating a seatbelt or a steering wheel.

[0166] In the present exemplary embodiment, the photoelectric conversion system S**8** captures an image of the periphery of the vehicle such as the front side or the rear side, for example. FIG. **28**C illustrates the photoelectric conversion system S**8** for capturing an image of a vehicle front side (imaging range **850**). The vehicle information acquisition apparatus **810** issues an instruction to the photoelectric conversion system S**8** or the imaging apparatus **80**. With this configuration, the accuracy of distance measurement can be further enhanced.

[0167] The above description has been given of an example in which control is performed in such a manner as not to collide with another vehicle. The photoelectric conversion system can also be applied to the control for performing automatic operation by following another vehicle, or the control for performing automatic operation in such a manner as not to deviate from a lane. Furthermore, the photoelectric conversion system S**8** can be applied to a movable body (moving apparatus) such as a vessel, an aircraft, or an industrial robot, for example, aside from a vehicle such as an automobile. This movable body includes either one or both of a drive force generation unit that generates drive force to be mainly used for the movement of the movable body, and a rotator to be mainly used for the movement of the movable body. The drive force generation unit can be an engine, a motor, or the like. The rotator can be a tire, a wheel, a screw of a ship, a propeller of a flight vehicle, or the like. Moreover, the photoelectric conversion system can be applied to a device that extensively uses object recognition, such as an intelligent transport system (ITS), in addition to a movable body. [Modified Exemplary Embodiment]

[0168] The present invention is not limited to the above-described exemplary embodiments, and various modifications can be made.

[0169] For example, an example in which a partial configuration of a certain exemplary embodiment is added to another exemplary embodiment, and an example in which a partial configuration of a certain exemplary embodiment is replaced with a partial configuration of another exemplary

embodiment are also included in the exemplary embodiments of the present invention.

[0170] The device and the photoelectric conversion systems described in the above-described sixth exemplary embodiment are examples of the photoelectric conversion systems to which the photoelectric conversion apparatus can be applied, and the photoelectric conversion system to which the photoelectric conversion apparatus of the present invention can be applied is not limited to the configuration illustrated in FIGS. **13** and **14**.

[0171] The above-described exemplary embodiments merely indicate examples of substantiation in executing the present invention, and the technical scope of the prevent invention is not to be construed in a limited manner based on these embodiments. That is, the present invention can be executed in various forms without departing from the technical idea or major features thereof.

[0172] In this specification, the wordings such as "A or B", "at least one of A and B", "at least one of A or/and B", and "one or more of A or/and B" can include all possible combinations of listed items, unless otherwise explicitly defined. That is, the above-described wordings are interpreted as disclosing all cases of a case where at least one A is included, a case where at least one B is included, and a case where both of at least one A and at least one B are included. The same applies to the combination of three or more components.

[0173] The exemplary embodiments described above can be appropriately changed without departing from the technical idea. The disclosure in this specification is not limited to matters described in this specification, and includes all matters that can be identified from this specification and the drawings accompanying this specification. The disclosure in this specification includes a complementary set of individual concepts described in this specification. More specifically, if "A is larger than B" is described in this specification, even if the description "B is not larger than A" is omitted, this specification is assumed to disclose that "B is not larger than A". This is because, in a case where "A is larger than B" is described, a case where "B is not larger than A" is assumed to be considered.

[0174] According to the technique of the present disclosure, it is possible to provide a desirable structure of a trench portion in a configuration in which a plurality of photoelectric conversion units is provided for one microlens.

[0175] While the present invention has been described with reference to exemplary embodiments, it is to be understood that the invention is not limited to the disclosed exemplary embodiments. The scope of the following claims is to be accorded the broadest interpretation so as to encompass all such modifications and equivalent structures and functions.

[0176] This application claims the benefit of Japanese Patent Application No. 2024-021764, filed Feb. 16, 2024, which is hereby incorporated by reference herein in its entirety.

What is claimed is:

1. A photoelectric conversion apparatus comprising:

a semiconductor substrate having a first principal surface from which light enters, and a second principal surface facing the first principal surface;

a microlens array including a plurality of microlenses;

a plurality of pixels each including a corresponding one microlens of the plurality of microlenses, a plurality of photoelectric conversion units in a plurality of rows and a plurality of columns that is arranged inside the semiconductor substrate, and arranged in such a manner as to corresponding to the one microlens, and a first trench portion that separates the plurality of photoelectric conversion units; and

a second trench portion provided between a photoelectric conversion unit included in one pixel of neighboring two pixels among the plurality of pixels, and a photoelectric conversion unit included in other one pixel of the neighboring two pixels, wherein, on the first principal surface, in a planar view with respect to the first principal surface, the first trench portion includes a plurality of first portions extending in a first direction, and a plurality of second portions extending in a second direction intersecting with the first direction,

wherein a first region between one first portion and other first portion of the plurality of first portions, and a second region between one second portion and other second portion of the plurality of second portions each include a semiconductor region of the semiconductor substrate, and

wherein, at a depth position between the first principal surface and the second principal surface, in the planar view, a part of the first trench portion is arranged at each of a position overlapping the first region and a position overlapping the second region.

2. A photoelectric conversion apparatus comprising:

a semiconductor substrate having a first principal surface from which light enters, and a second principal surface facing the first principal surface;

a microlens array including a plurality of microlenses;

a plurality of pixels each including a corresponding one microlens of the plurality of microlenses, a plurality of photoelectric conversion units in a plurality of rows and a plurality of columns that is arranged inside the semiconductor substrate, and arranged in such a manner as to corresponding to the one microlens, a first trench portion that separates the plurality of photoelectric conversion units, and a plurality of amplification transistors each having a gate; and

a second trench portion provided between a photoelectric conversion unit included in one pixel of neighboring two pixels among the plurality of pixels, and a photoelectric conversion unit included in other one pixel of the neighboring two pixels,

wherein the respective gates of the plurality of amplification transistors are connected in common to a node to which signal charges of the plurality of photoelectric conversion units are input,

wherein, on the second principal surface, in a planar view with respect to the second principal surface, the first trench portion includes a plurality of first portions extending in a first direction, and a plurality of second portions extending in a second direction intersecting with the first direction,

wherein a first region between one first portion and other first portion of the plurality of first portions, and a second region between one second portion and other second portion of the plurality of second portions each include a semiconductor region of the semiconductor substrate, and

wherein, at a depth position between the first principal surface and the second principal surface, in the planar

view, a part of the first trench portion is arranged at each of a position overlapping the first region and a position overlapping the second region.

3. A photoelectric conversion apparatus comprising:

a semiconductor substrate having a first principal surface from which light enters, and a second principal surface facing the first principal surface;

a microlens array including a plurality of microlenses;

a plurality of pixels each including a corresponding one microlens of the plurality of microlenses, a plurality of photoelectric conversion units in a plurality of rows and a plurality of columns that is arranged inside the semiconductor substrate, and arranged in such a manner as to corresponding to the one microlens, and a first trench portion that separates the plurality of photoelectric conversion units; and

a second trench portion provided between a photoelectric conversion unit included in one pixel of neighboring two pixels among the plurality of pixels, and a photoelectric conversion unit included in other one pixel of the neighboring two pixels,

wherein, on the first principal surface, in a planar view with respect to the first principal surface, the first trench portion includes a first portion extending in a first direction,

wherein, on the second principal surface, in a planar view with respect to the second principal surface, the first trench portion includes a third portion extending in the first direction,

wherein the first portion and the third portion have portions overlapping in the planar view with respect to the first principal surface, and

wherein a semiconductor region of the semiconductor substrate is arranged between the first portion and the third portion.

4. The photoelectric conversion apparatus according to claim **1**,

wherein each of the plurality of pixels includes a plurality of amplification transistors, and

wherein the respective gates of the plurality of amplification transistors are connected in common to a node to which signal charges of the plurality of photoelectric conversion units are input.

5. The photoelectric conversion apparatus according to claim **3**,

wherein each of the plurality of pixels includes a plurality of amplification transistors, and

wherein the respective gates of the plurality of amplification transistors are connected in common to a node to which signal charges of the plurality of photoelectric conversion units are input.

6. The photoelectric conversion apparatus according to claim **1**, wherein the semiconductor region included in each of the first region and the second region extends from the first principal surface up to a predetermined portion positioned at a predetermined depth of the semiconductor substrate, and the first trench portion extends from the predetermined portion up to the second principal surface.

7. The photoelectric conversion apparatus according to claim **2**, wherein the semiconductor region included in each of the first region and the second region extends from the second principal surface up to a predetermined portion positioned at a predetermined depth of the semiconductor substrate, and the first trench portion extends from the predetermined portion up to the first principal surface.

8. The photoelectric conversion apparatus according to claim **3**, wherein the semiconductor region of the semiconductor substrate is positioned on the semiconductor substrate at a predetermined depth from the first principal surface, and the first trench portion is arranged between the semiconductor region and the first principal surface, and between the semiconductor region and the second principal surface.

9. The photoelectric conversion apparatus according to claim **1**,

wherein a part of the first trench portion is arranged between one photoelectric conversion unit of photoelectric conversion units in the plurality of rows, and a different photoelectric conversion unit of photoelectric conversion units in the plurality of rows, and

wherein a part of the first trench portion is arranged between one photoelectric conversion unit of photoelectric conversion units in the plurality of columns and a different photoelectric conversion unit of photoelectric conversion units in the plurality of columns.

10. The photoelectric conversion apparatus according to claim **2**,

wherein a part of the first trench portion is arranged between one photoelectric conversion unit of photoelectric conversion units in the plurality of rows, and a different photoelectric conversion unit of photoelectric conversion units in the plurality of rows, and

wherein a part of the first trench portion is arranged between one photoelectric conversion unit of photoelectric conversion units in the plurality of columns and a different photoelectric conversion unit of photoelectric conversion units in the plurality of columns.

11. The photoelectric conversion apparatus according to claim **3**,

wherein a part of the first trench portion is arranged between one photoelectric conversion unit of photoelectric conversion units in the plurality of rows and a different photoelectric conversion unit of photoelectric conversion units in the plurality of rows, and

wherein a part of the first trench portion is arranged between one photoelectric conversion unit of photoelectric conversion units in the plurality of columns and a different photoelectric conversion unit of photoelectric conversion units in the plurality of columns.

12. The photoelectric conversion apparatus according to claim **3**,

wherein the semiconductor region is arranged between one photoelectric conversion unit of photoelectric conversion units in the plurality of rows and a different photoelectric conversion unit of photoelectric conversion units in the plurality of rows,

wherein, on the first principal surface, in a planar view with respect to the first principal surface, the first trench portion includes a fourth portion extending in a second direction,

wherein, on the second principal surface, in a planar view with respect to the second principal surface, the first trench portion includes a fifth portion extending in the second direction,

wherein the fourth portion and the fifth portion include portions overlapping in the planar view with respect to the first principal surface, and a second semiconductor

region of the semiconductor substrate is arranged between the fourth portion and the fifth portion, and

wherein the second semiconductor region is arranged between one photoelectric conversion unit of photoelectric conversion units in the plurality of columns and a different photoelectric conversion unit of photoelectric conversion units in the plurality of columns.

13. The photoelectric conversion apparatus according to claim **12**,

wherein the semiconductor region is arranged between one photoelectric conversion unit of photoelectric conversion units in the plurality of rows and a different photoelectric conversion unit of photoelectric conversion units in the plurality of rows,

wherein, on the first principal surface, in a planar view with respect to the first principal surface, the first trench portion includes a fourth portion extending in a second direction,

wherein, on the second principal surface, in a planar view with respect to the second principal surface, the first trench portion includes a fifth portion extending in the second direction,

wherein the fourth portion and the fifth portion include portions overlapping in the planar view with respect to the first principal surface, and a second semiconductor region of the semiconductor substrate is arranged between the fourth portion and the fifth portion, and

wherein the second semiconductor region is arranged between one photoelectric conversion unit of photoelectric conversion units in the plurality of columns and a different photoelectric conversion unit of photoelectric conversion units in the plurality of columns.

14. A device comprising:

the semiconductor apparatus according to claim **1**,

wherein the device further includes at least any one of:

an optical device adapted to the semiconductor apparatus,

a control device configured to control the semiconductor apparatus,

a processing device configured to process a signal output from the semiconductor apparatus,

a display device configured to display information obtained by the semiconductor apparatus,

a storage device configured to store information obtained by the semiconductor apparatus, and

a mechanical device configured to operate based on information obtained by the semiconductor apparatus.

15. A device comprising:

the semiconductor apparatus according to claim **2**,

wherein the device further includes at least any one of:

an optical device adapted to the semiconductor apparatus,

a control device configured to control the semiconductor apparatus,

a processing device configured to process a signal output from the semiconductor apparatus,

a display device configured to display information obtained by the semiconductor apparatus,

a storage device configured to store information obtained by the semiconductor apparatus, and

a mechanical device configured to operate based on information obtained by the semiconductor apparatus.

16. A device comprising:

the semiconductor apparatus according to claim **3**,

wherein the device further includes at least any one of:

an optical device adapted to the semiconductor apparatus,

a control device configured to control the semiconductor apparatus,

a processing device configured to process a signal output from the semiconductor apparatus,

a display device configured to display information obtained by the semiconductor apparatus,

a storage device configured to store information obtained by the semiconductor apparatus, and

a mechanical device configured to operate based on information obtained by the semiconductor apparatus.

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