US012394722B2

(12) **United States Patent**
Madhavan et al.

(10) **Patent No.: US 12,394,722 B2**
(45) **Date of Patent: Aug. 19, 2025**

(54) **DIELECTRIC CAPACITANCE RECOVERY OF INTER-LAYER DIELECTRIC LAYERS FOR ADVANCED INTEGRATED CIRCUIT STRUCTURE FABRICATION**

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(72) Inventors: **Atul Madhavan**, Portland, OR (US); **Abhishek Jain**, Portland, OR (US); **Jinhong Shin**, Portland, OR (US); **Anant H. Jahagirdar**, Hillsboro, OR (US)

(73) Assignee: **Intel Corporation**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 767 days.

(21) Appl. No.: **17/131,701**

(22) Filed: **Dec. 22, 2020**

(65) **Prior Publication Data**

US 2022/0102279 A1 Mar. 31, 2022

Related U.S. Application Data

(60) Provisional application No. 63/083,737, filed on Sep. 25, 2020.

(51) **Int. Cl.**
H01L 23/48 (2006.01)
H01L 21/768 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H01L 23/5384*** (2013.01); ***H01L 21/76802*** (2013.01); ***H01L 23/49877*** (2013.01); ***H01L 23/5386*** (2013.01)

(58) **Field of Classification Search**
CPC H01L 23/5384; H01L 21/76802; H01L 23/49877; H01L 23/5386; H01L 2924/00; H01L 21/76835; H01L 21/76877; H01L 21/76224; H01L 21/76837; H01L 23/481; H01L 21/76831; H01L 21/76805; H01L 21/3215; H01L 21/28518;
(Continued)

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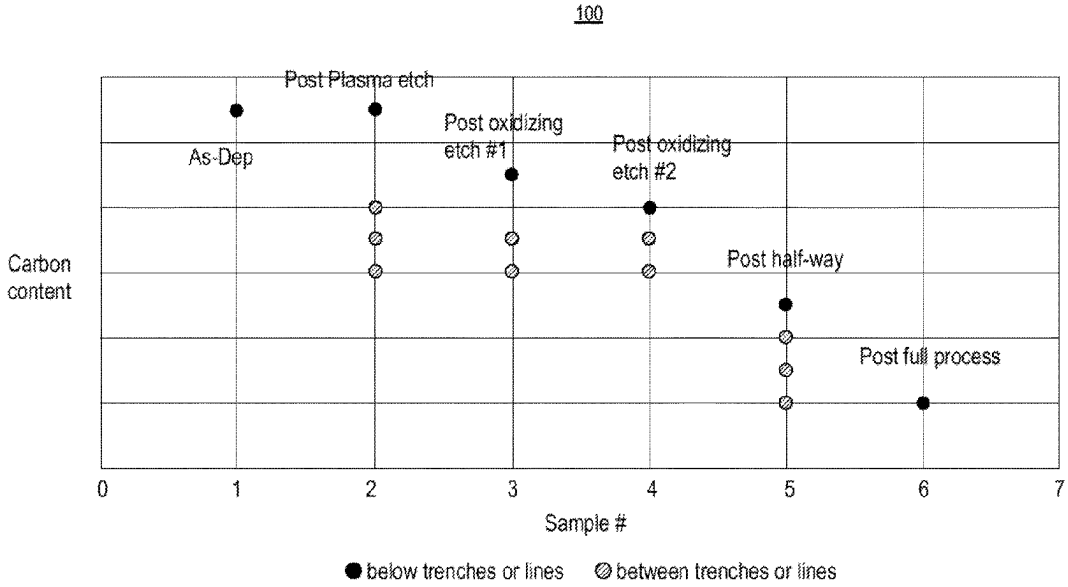
Primary Examiner — Niki H Nguyen
(74) *Attorney, Agent, or Firm* — Schwabe, Williamson & Wyatt P.C.

(57) **ABSTRACT**

Embodiments of the disclosure are in the field of advanced integrated circuit structure fabrication. In an example, an integrated circuit structure includes a single dielectric layer above a substrate. A plurality of conductive lines is in an upper portion of the single dielectric layer above a lower portion of the single dielectric layer. A carbon dopant region is in the upper portion of the single dielectric layer, the carbon dopant region between adjacent ones of the plurality of conductive lines.

20 Claims, 20 Drawing Sheets



(51) **Int. Cl.**

H01L 23/498	(2006.01)
H01L 23/52	(2006.01)
H01L 23/538	(2006.01)
H01L 29/40	(2006.01)

(58) **Field of Classification Search**

CPC H01L 2224/04026; H01L 23/53228; H01L 23/73; H01L 23/5227; H01L 21/28008; H01L 2221/1078; H01L 24/08; H01L 2224/4813; H01L 24/48; H01L 24/49; H01L 21/2007; H01L 2225/0651; H01L 25/0657; H01L 24/73; H01L 23/5329; H01L 23/522–53295; H01L 23/53276; H01L 21/76825; H01L 21/76828; H01L 21/02164; H01L 21/28558; H01L 21/02527; H01L 21/02115; H01L 21/02118–0212; H01L 21/312–3128; H01L 21/768–76898; H01L 21/76807–76813; H01L 2221/1005–1063; C23C 16/26–279; C23C 14/0605; G06F 1/16; C01B 32/30–39; H01B 3/18–56

See application file for complete search history.

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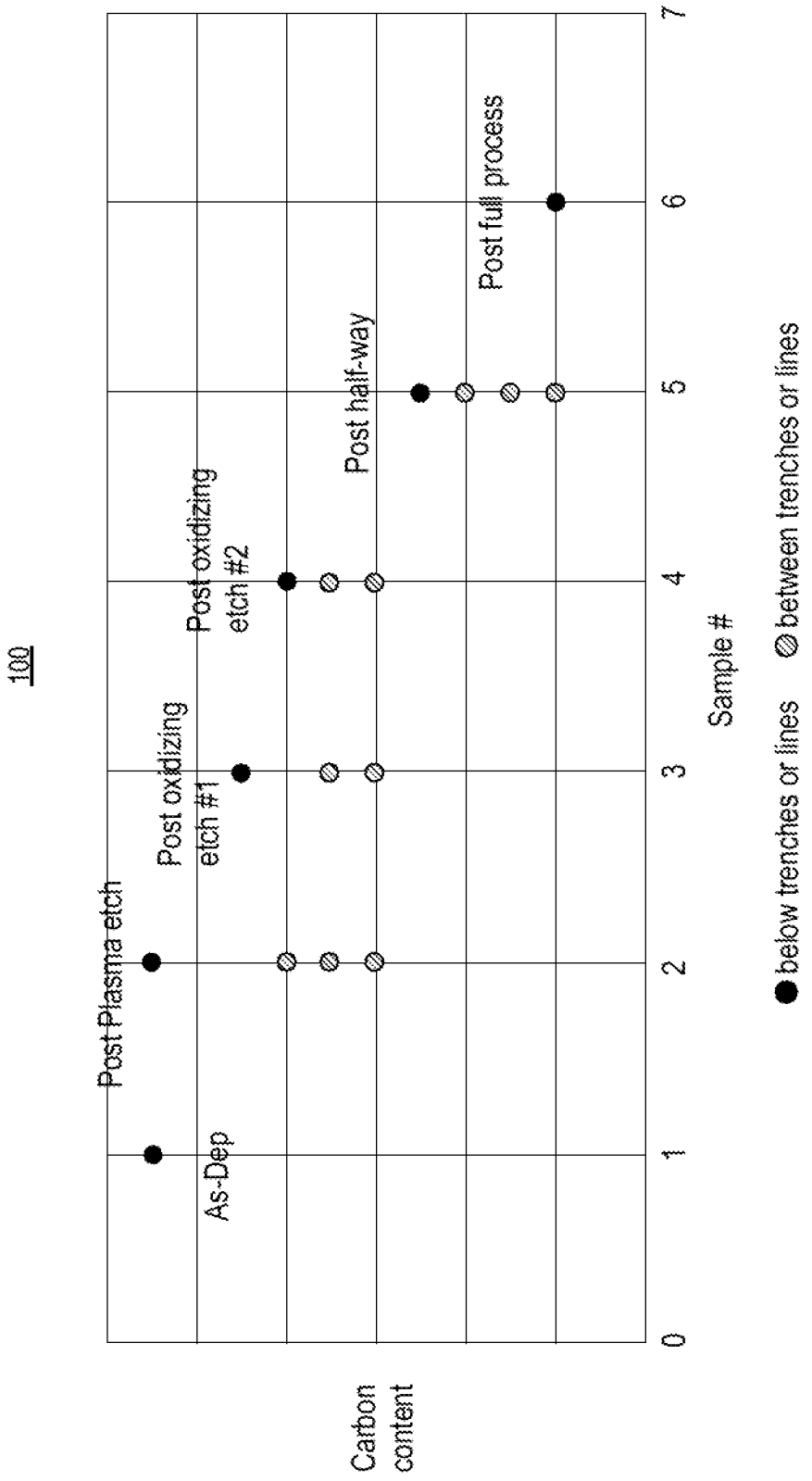

100
Carbon content
0
1
2
3
4
5
6
7
Sample #
As-Dep
Post Plasma etch
Post oxidizing etch #1
Post oxidizing etch #2
Post half-way
Post full process
below trenches or lines
between trenches or lines

FIG. 1

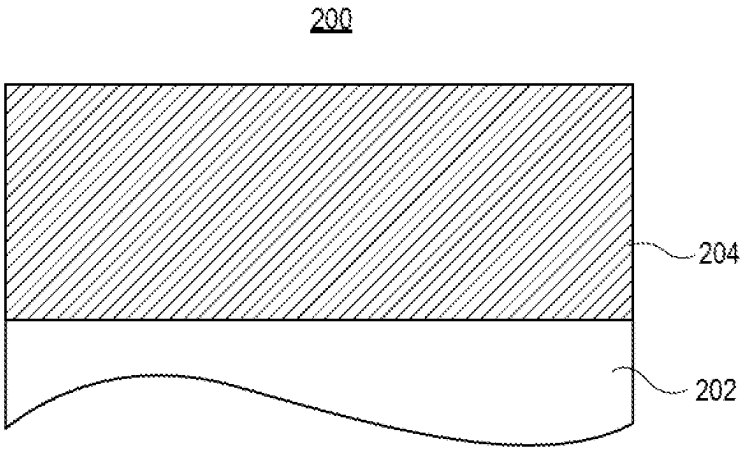


FIG. 2A

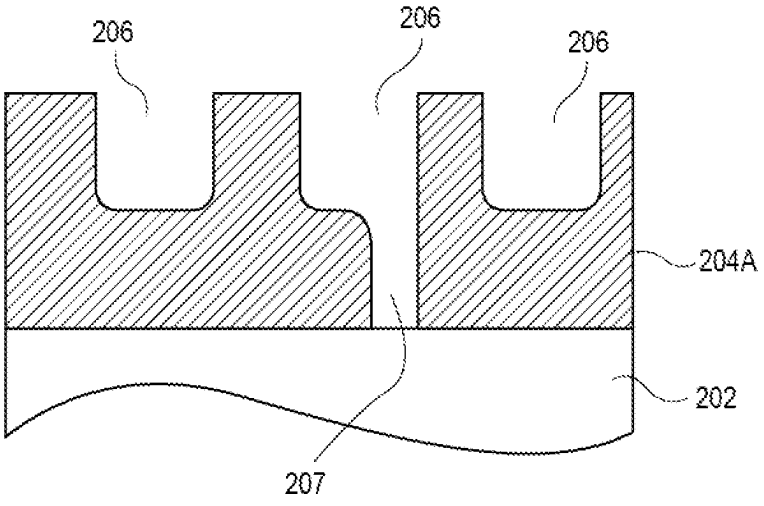


FIG. 2B

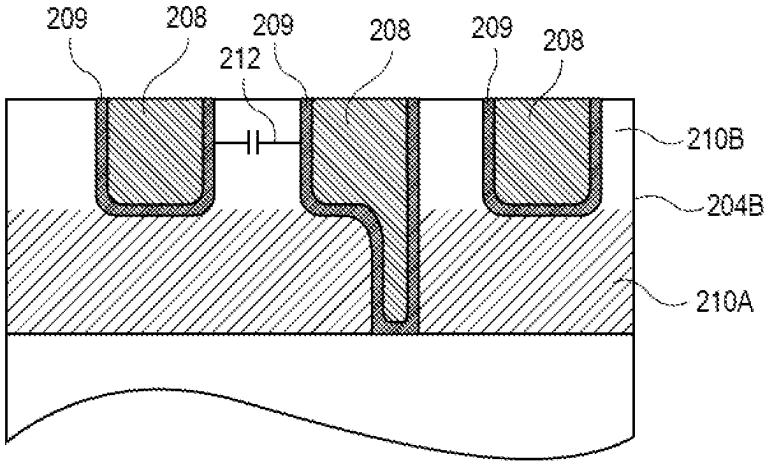

209
208
209
208
209
208
212
210B
204B
210A

FIG. 2C

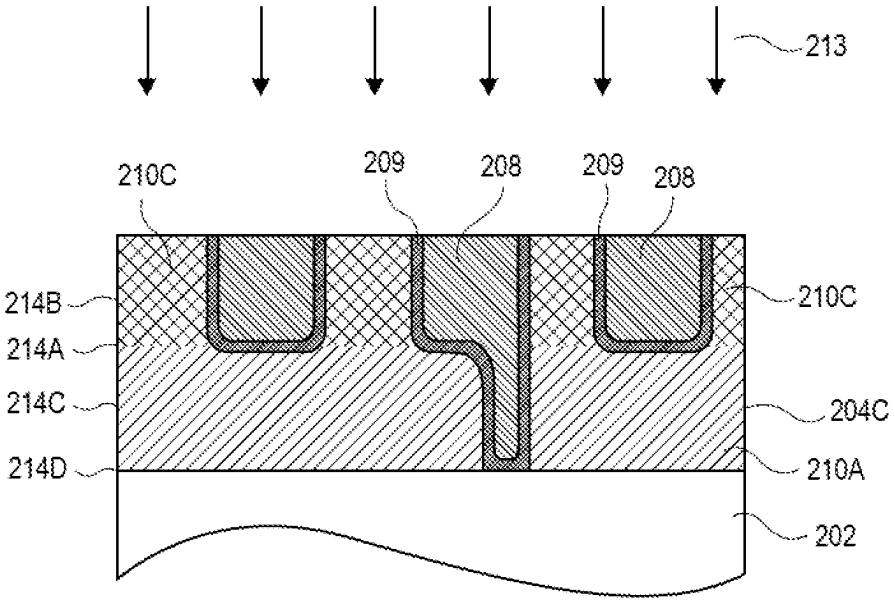

213
210C
209
208
209
208
214B
214A
214C
214D
210C
204C
210A
202

FIG. 2D

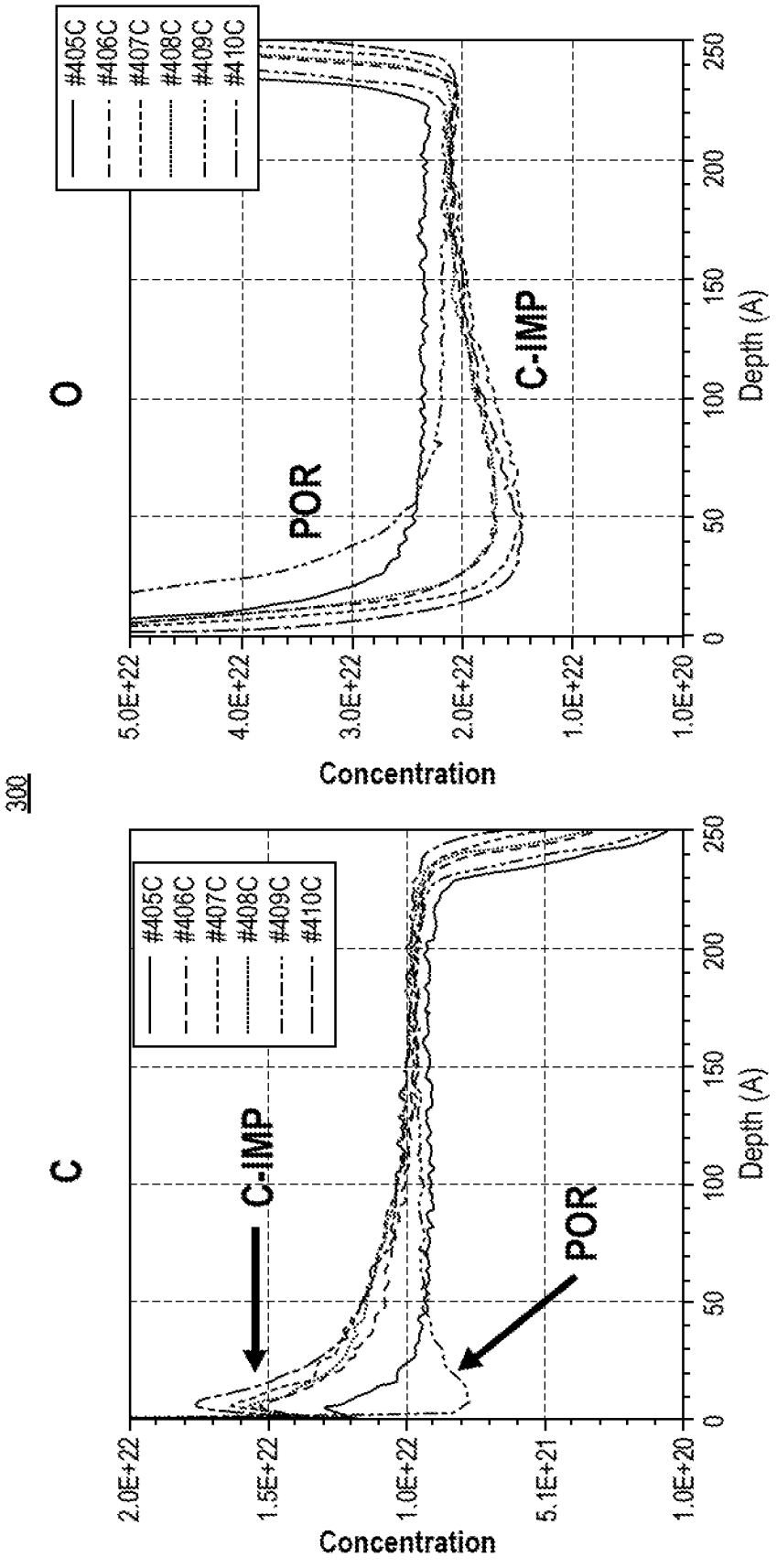

300
O
#405C
#406C
#407C
#408C
#409C
#410C
POR
C-IMP
5.0E+22
4.0E+22
3.0E+22
2.0E+22
1.0E+22
1.0E+20
Concentration
0
50
100
150
200
250
Depth (A)
C
C-IMP
POR
2.0E+22
1.5E+22
1.0E+22
5.1E+21
1.0E+20
Concentration
Depth (A)

FIG. 3

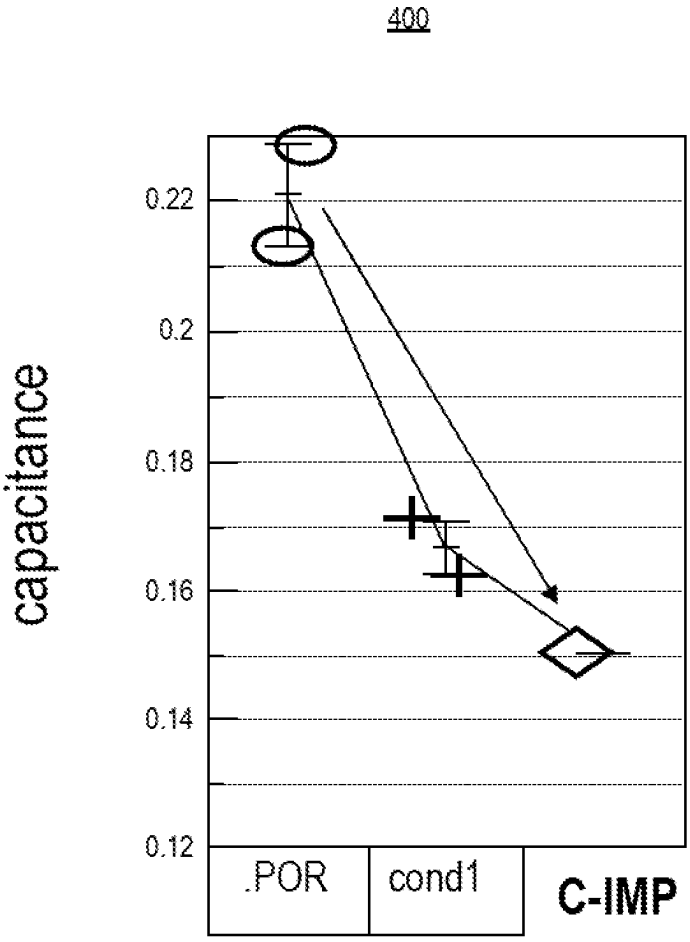


FIG. 4

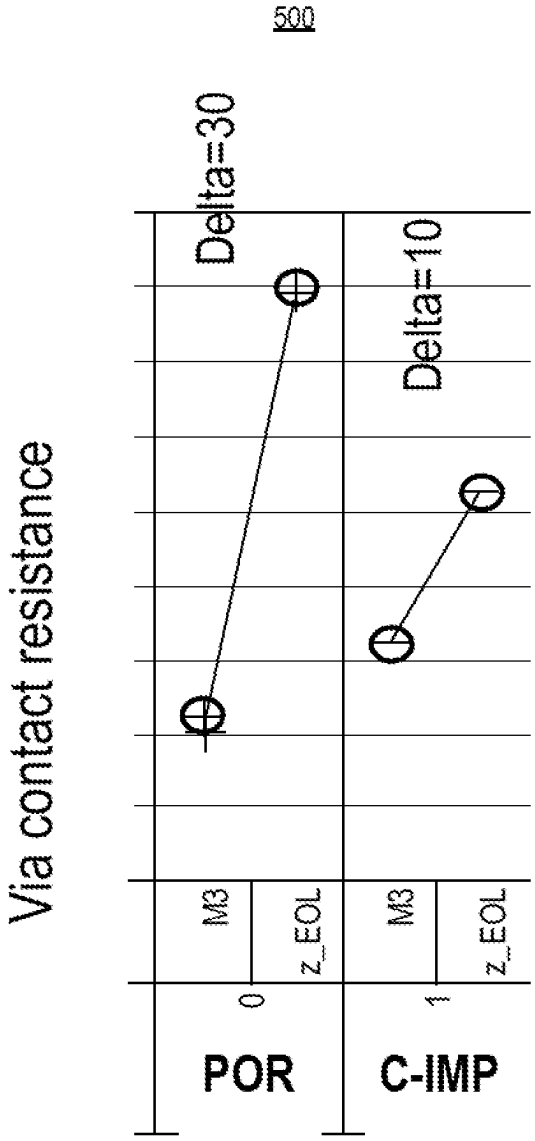

500
Delta=30
Delta=10
Via contact resistance
M3
z_EOL
M3
z_EOL
0
1
POR
C-IMP

FIG. 5

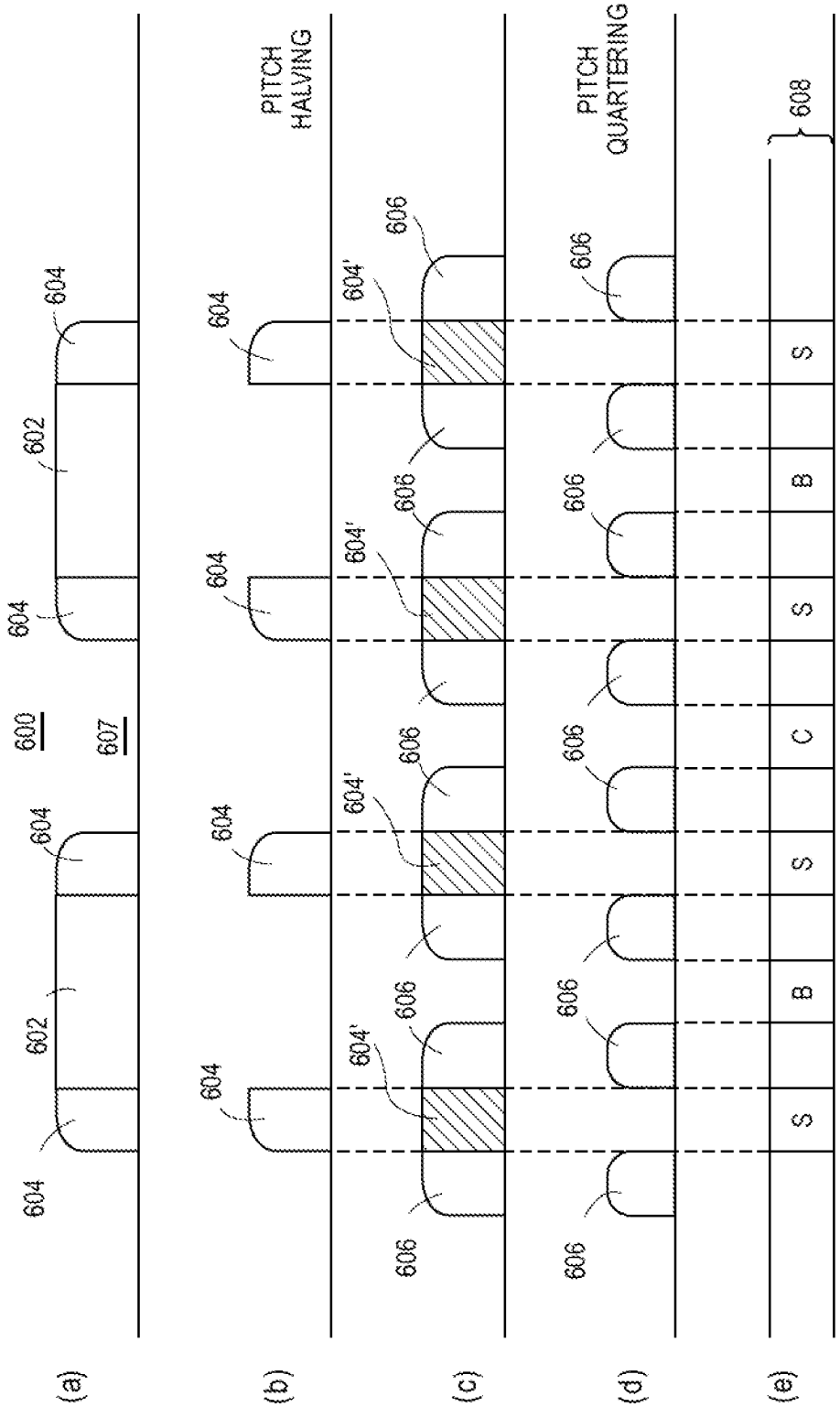

(a)
(b)
(c)
(d)
(e)
600
607
602
604
604'
606
608
PITCH HALVING
PITCH QUARTERING
S
B
S
C
S
B
S

FIG. 6

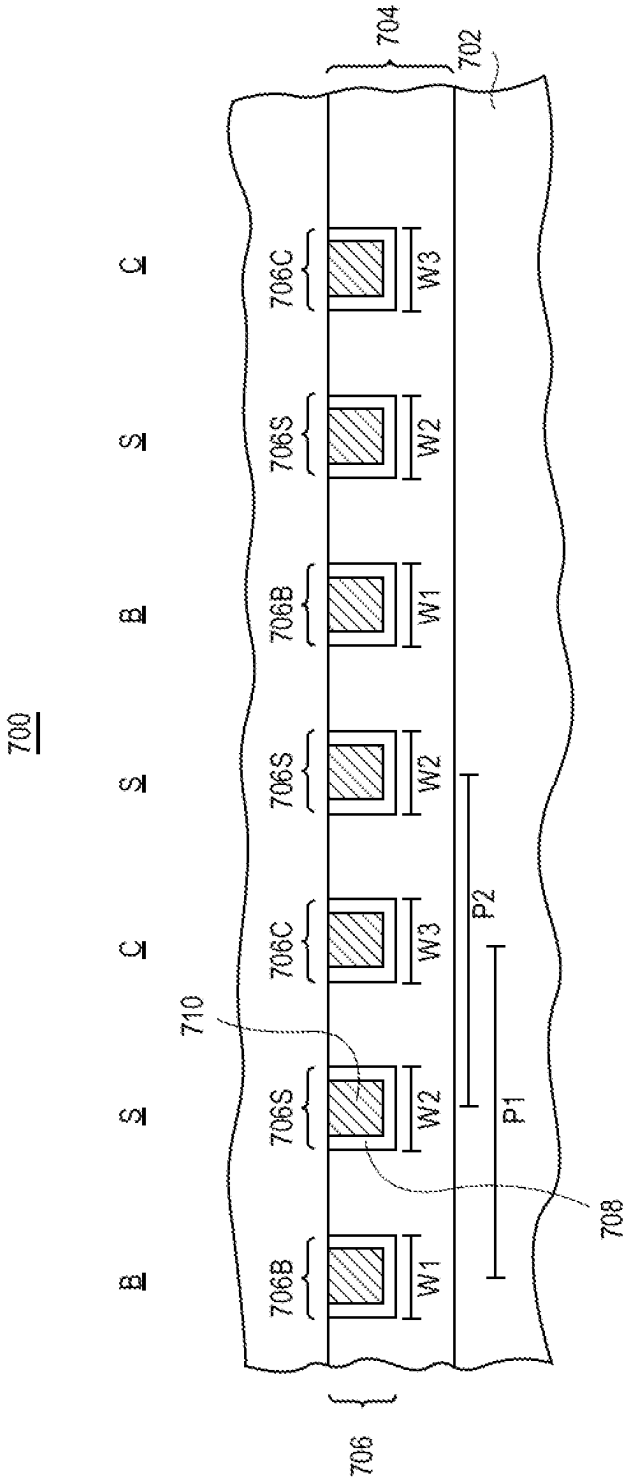

700
704
702
706
B
S
C
S
B
S
C
S
B
706B
706S
706C
706S
706B
706S
706C
706S
706B
W1
W2
W3
W2
W1
W2
W3
W2
W1
P1
P2
708
710

FIG. 7A

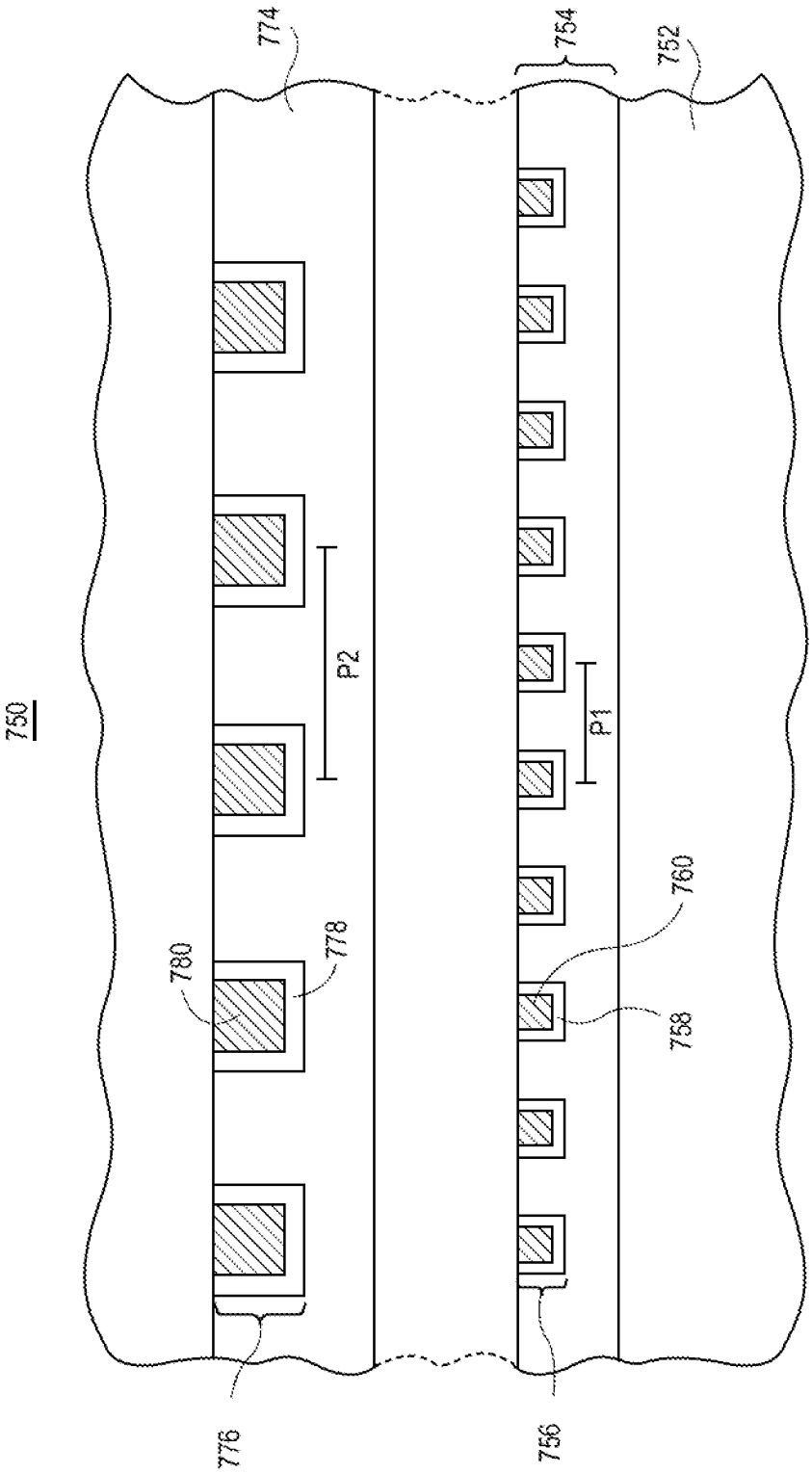


FIG. 7B

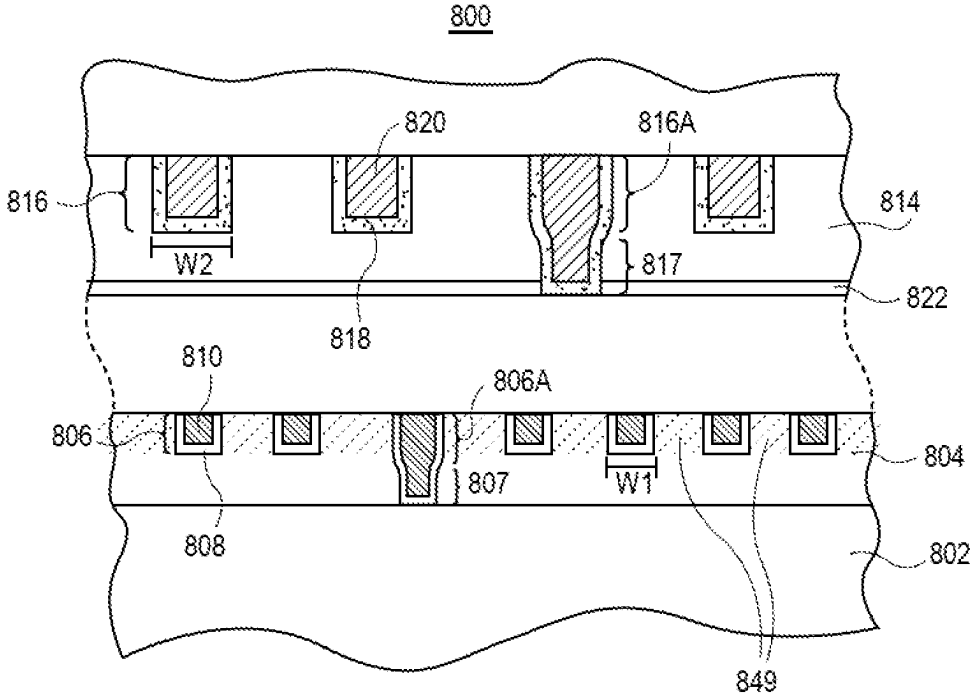

800
820
816A
816
814
W2
817
822
818
810
806A
806
804
807
W1
808
802
849

FIG. 8A

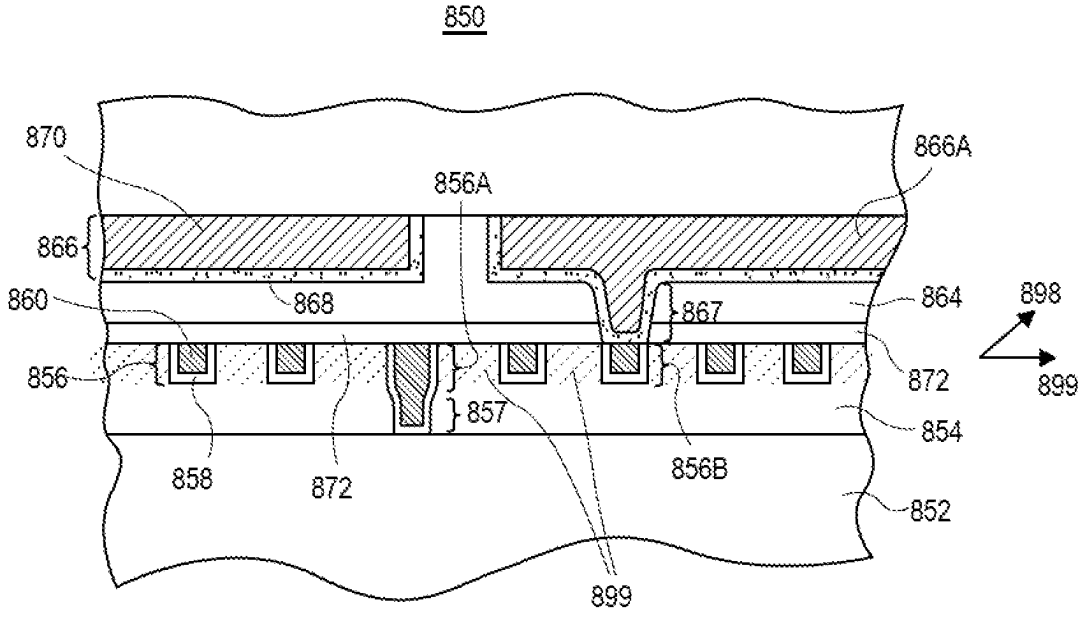

850
870
866A
856A
866
868
867
864
898
860
872
899
856
857
854
858
872
856B
852
899

FIG. 8B

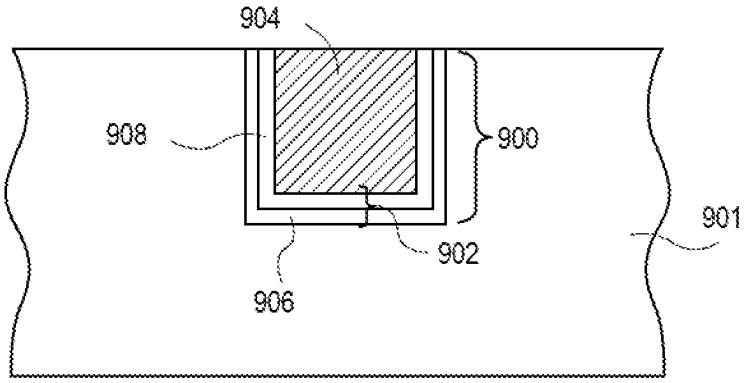


FIG. 9A

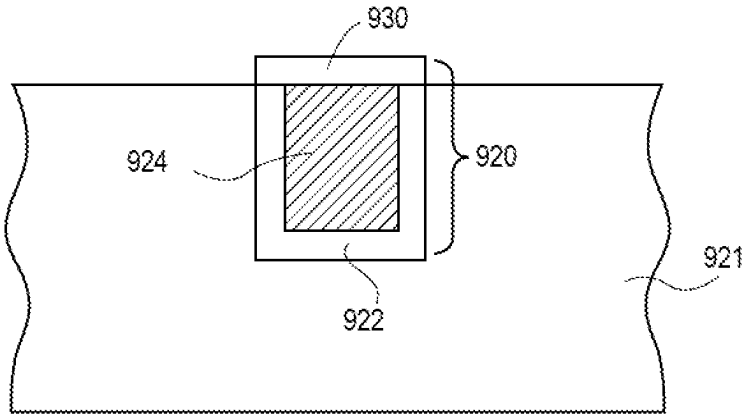


FIG. 9B

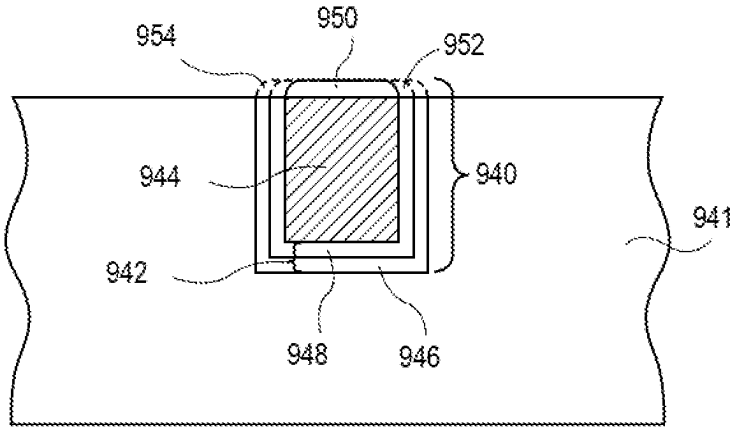


FIG. 9C

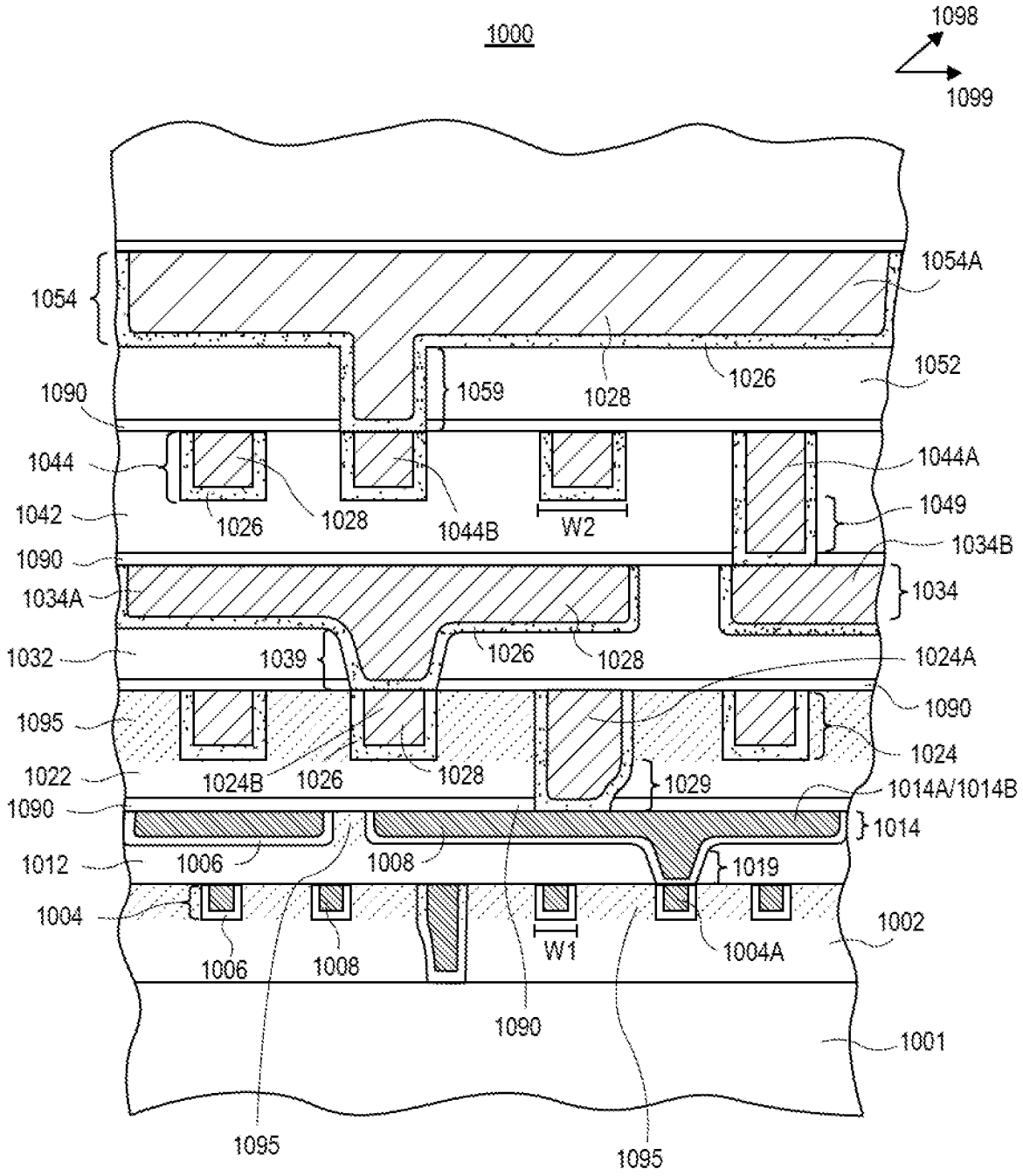

1000
1098
1099
1054
1054A
1052
1090
1059
1028
1026
1044
1044A
1042
1026
1028
1044B
W2
1049
1090
1034B
1034A
1034
1032
1039
1026
1028
1024A
1095
1090
1024
1022
1024B
1026
1028
1029
1014A/1014B
1090
1014
1012
1006
1008
1019
1004
1002
1006
1008
W1
1004A
1090
1001
1095
1095

FIG. 10

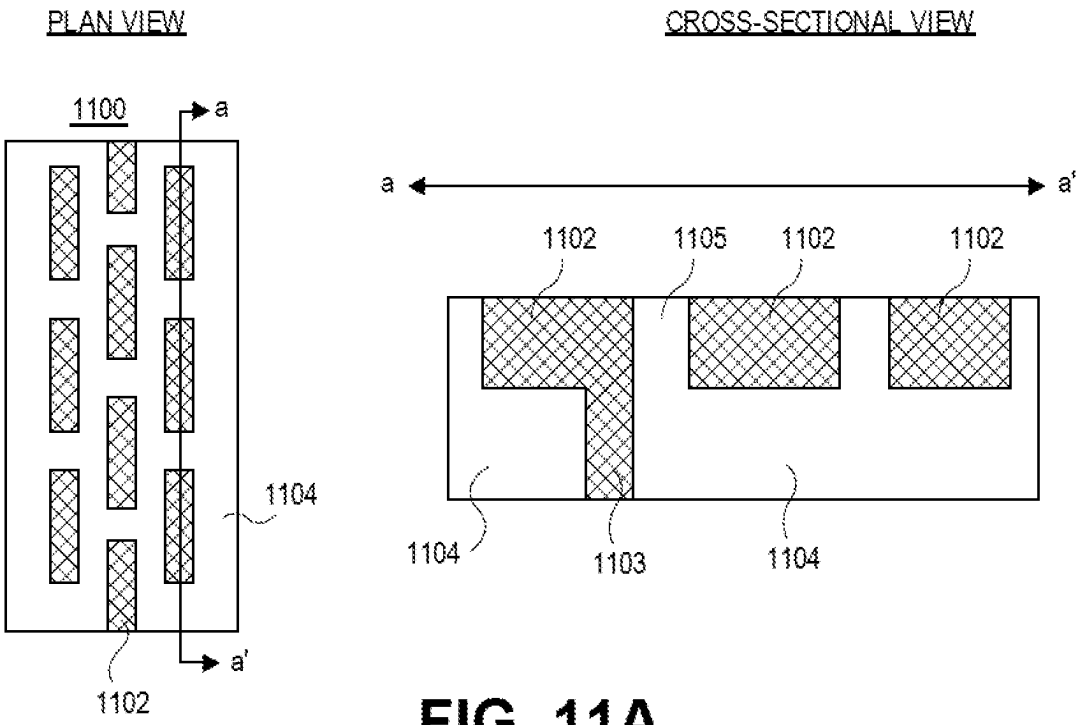


FIG. 11A

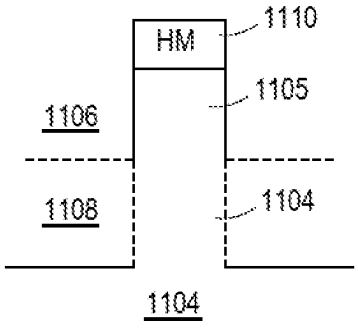
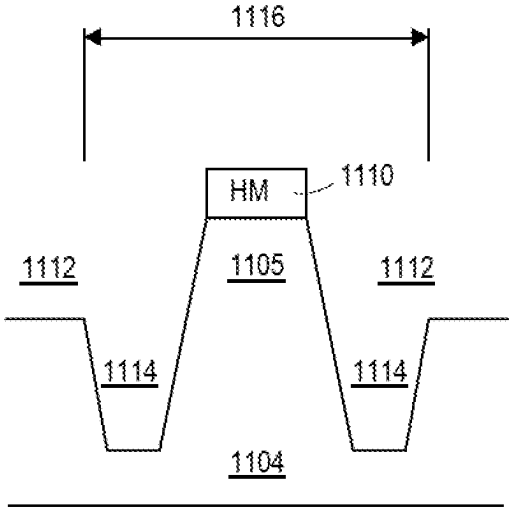


FIG. 11B



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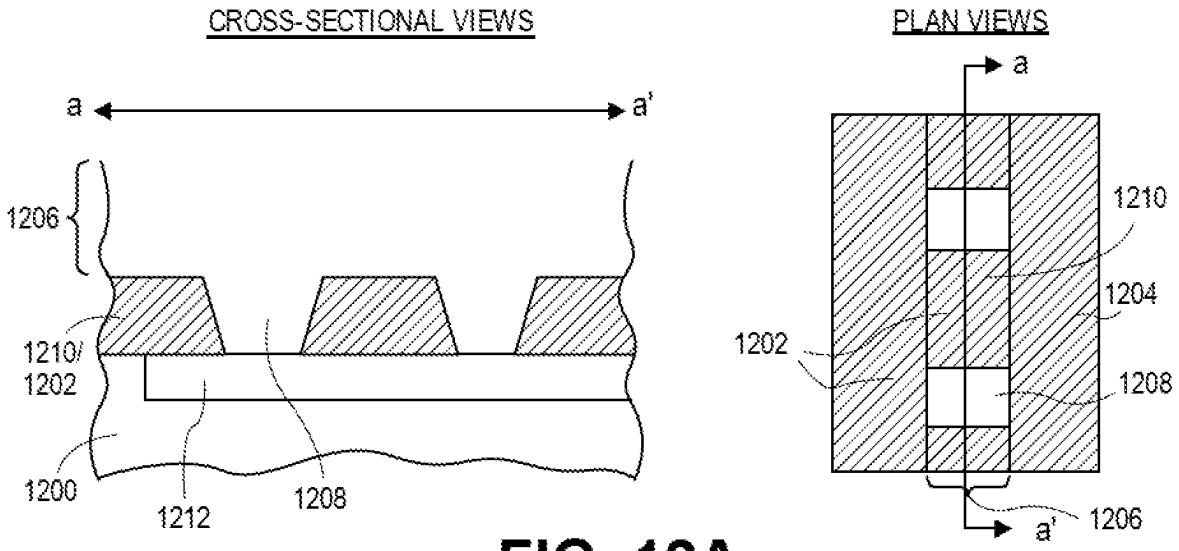
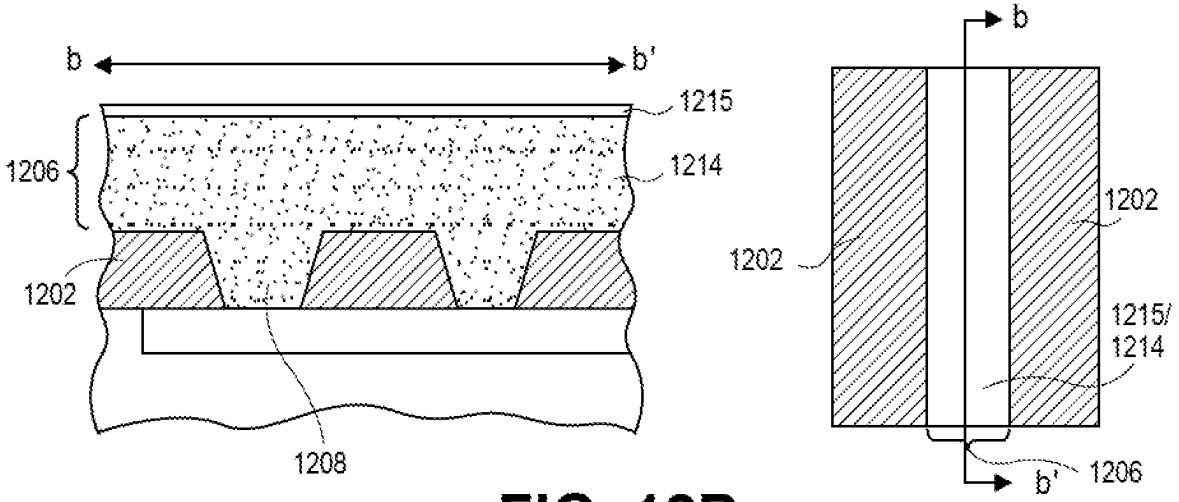


FIG. 12A



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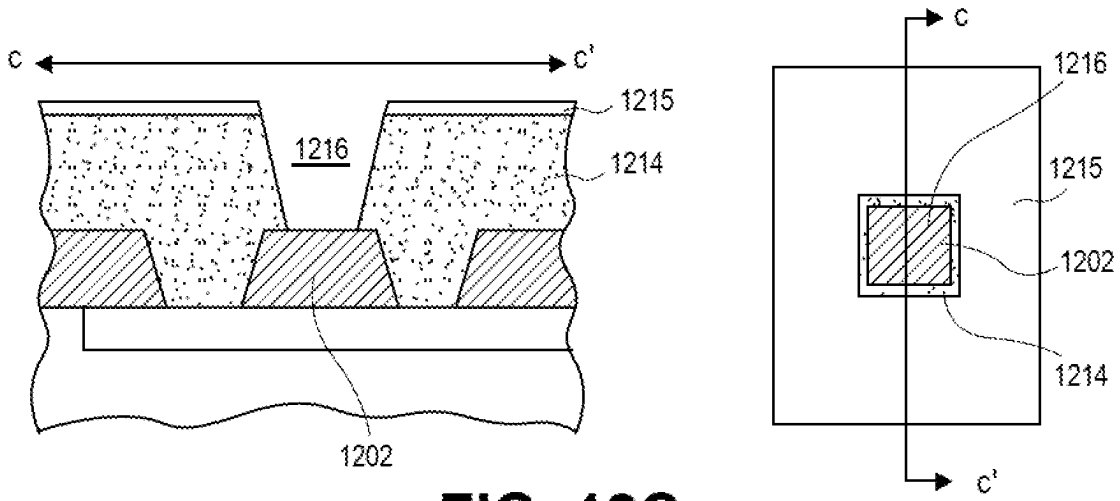

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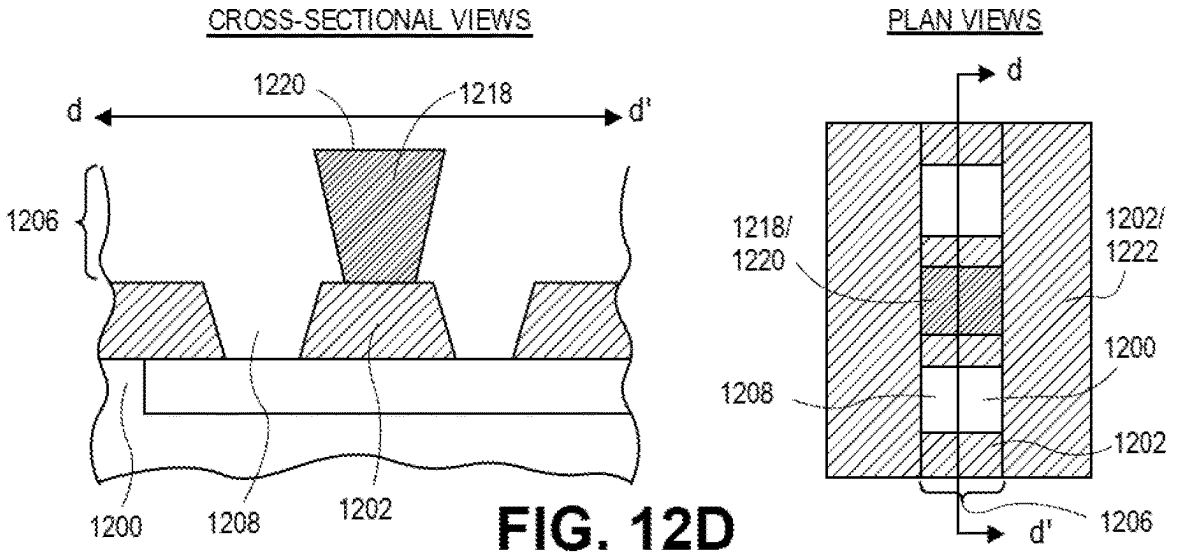

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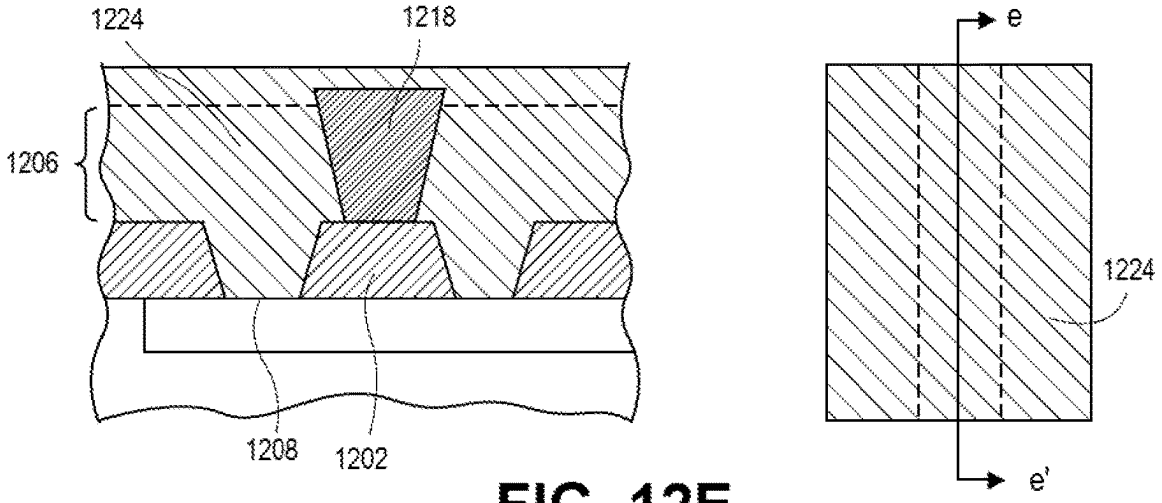
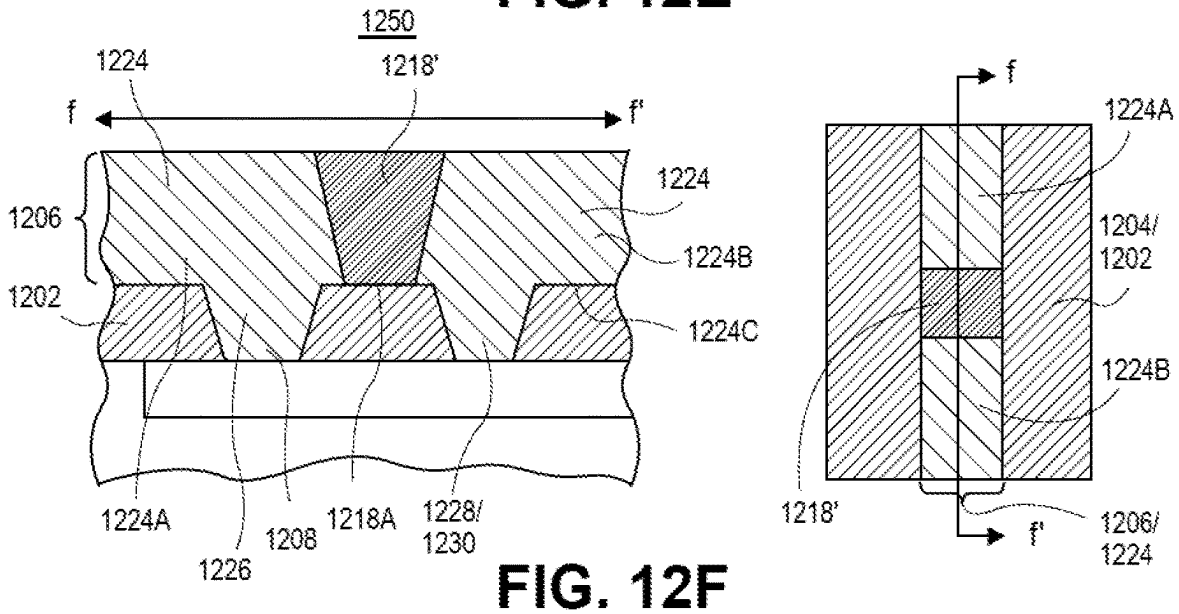


FIG. 12E



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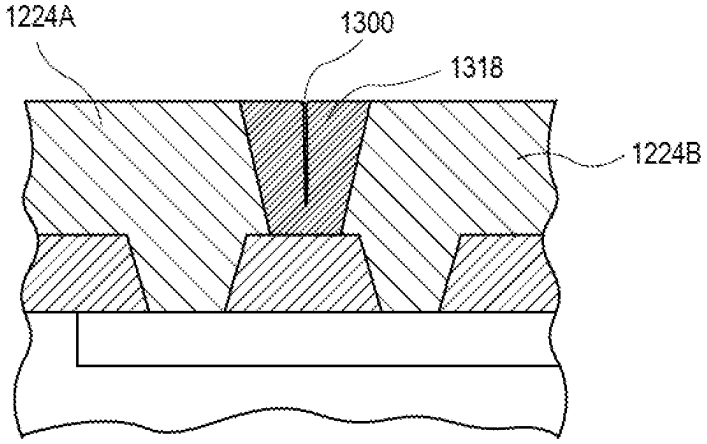

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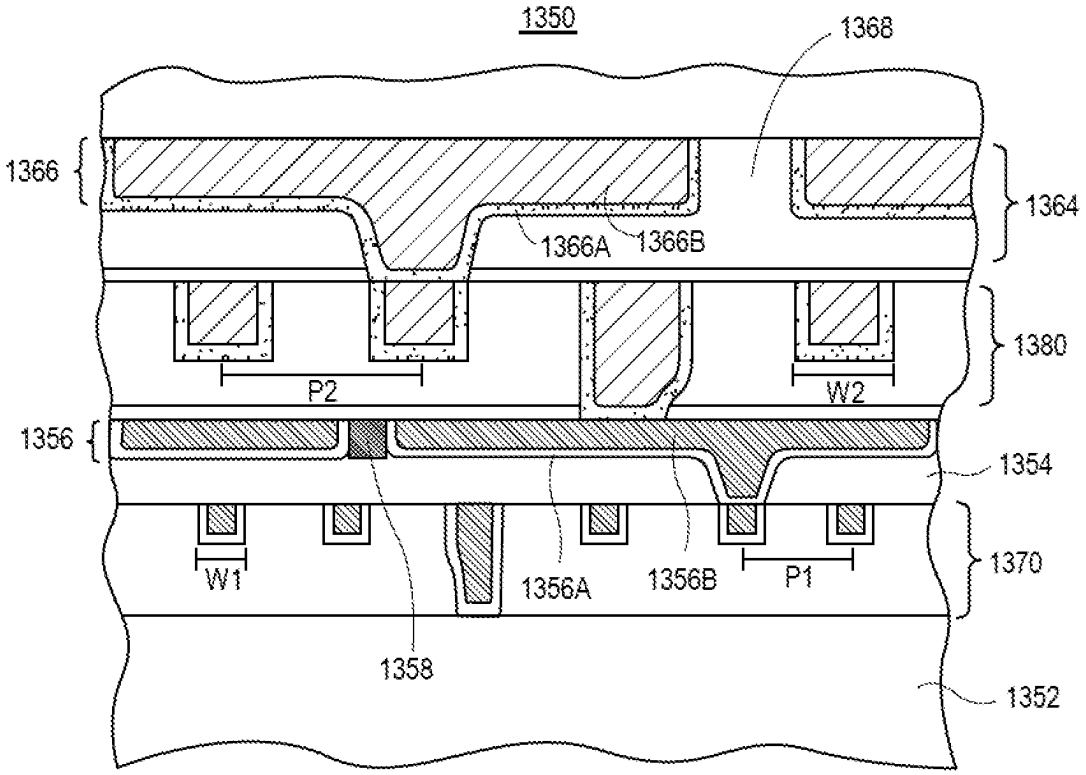

FIG. 13B

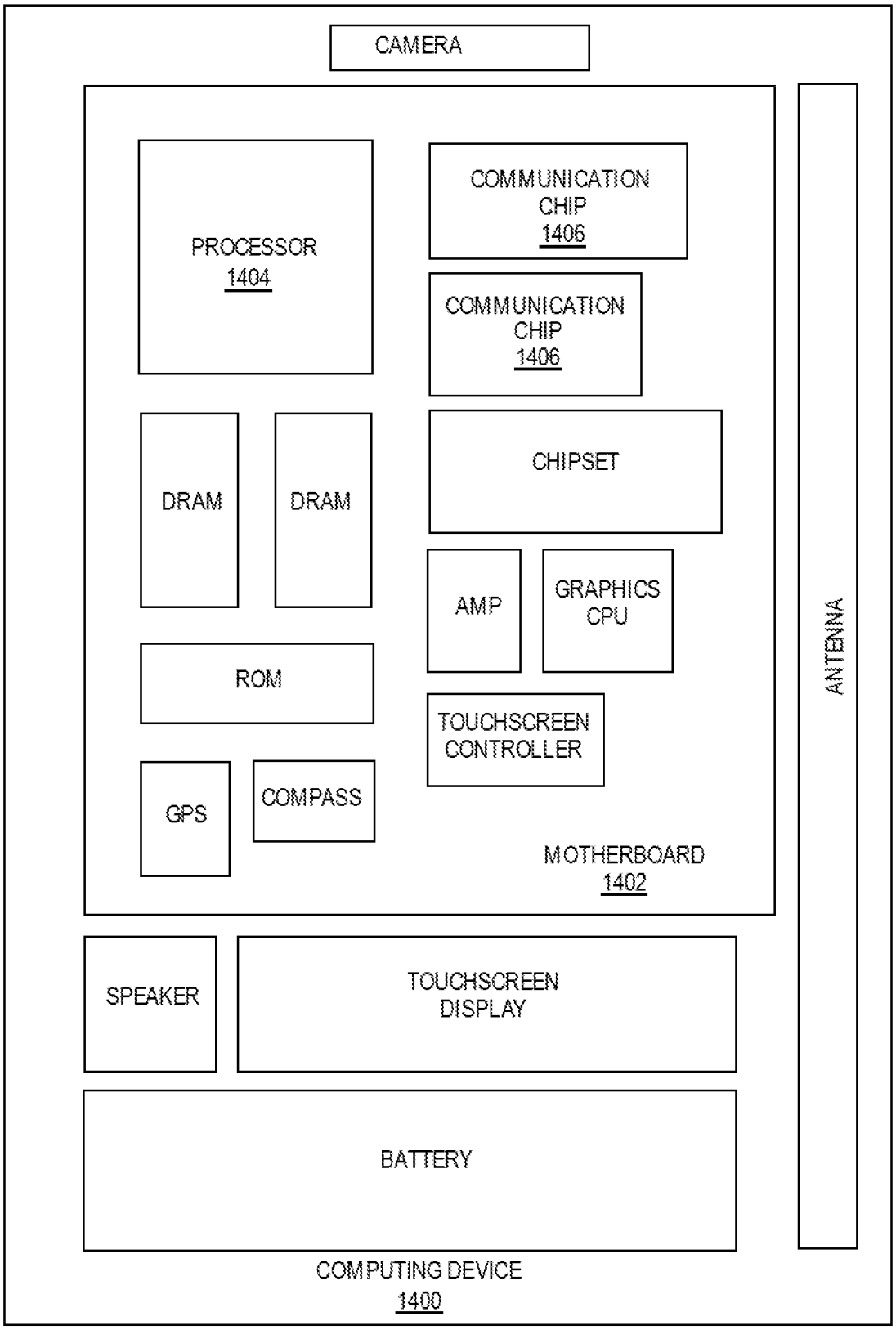
CAMERA
PROCESSOR
1404
COMMUNICATION
CHIP
1406
COMMUNICATION
CHIP
1406
DRAM
DRAM
CHIPSET
AMP
GRAPHICS
CPU
ROM
TOUCHSCREEN
CONTROLLER
GPS
COMPASS
MOTHERBOARD
1402
ANTENNA
SPEAKER
TOUCHSCREEN
DISPLAY
BATTERY
COMPUTING DEVICE
1400

FIG. 14

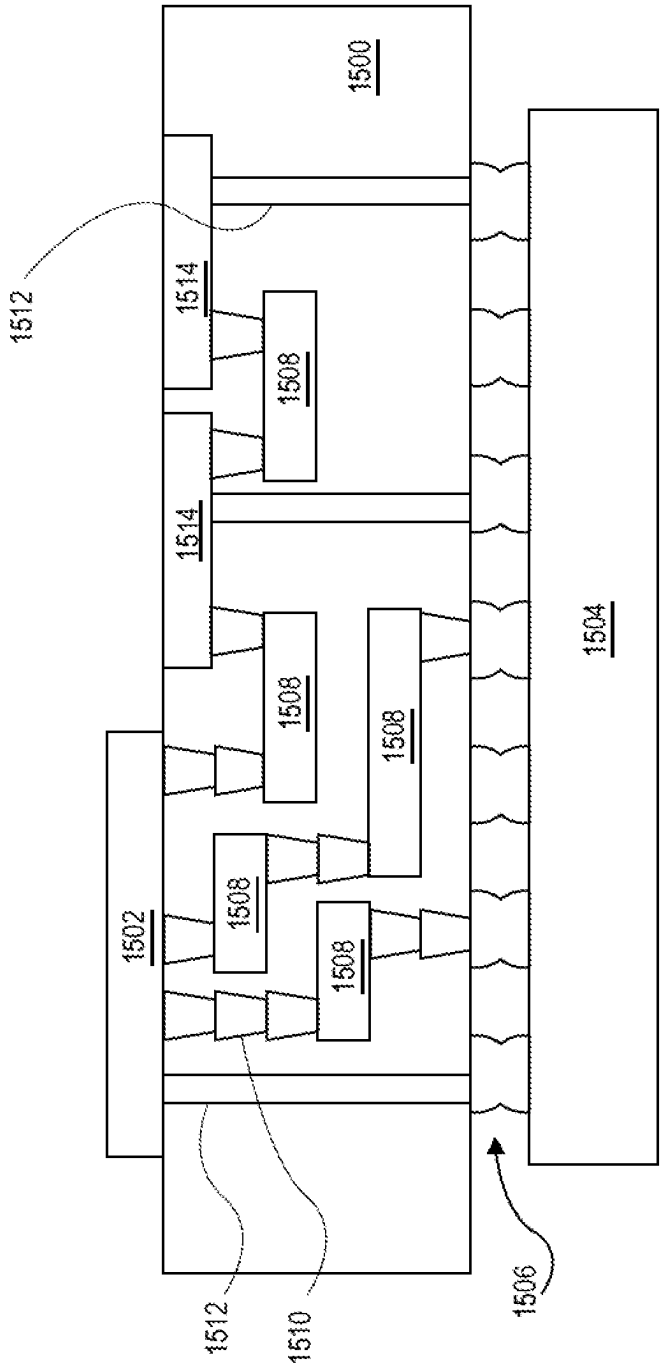
1500
1512
1514
1508
1514
1508
1508
1504
1502
1508
1508
1512
1510
1506

FIG. 15

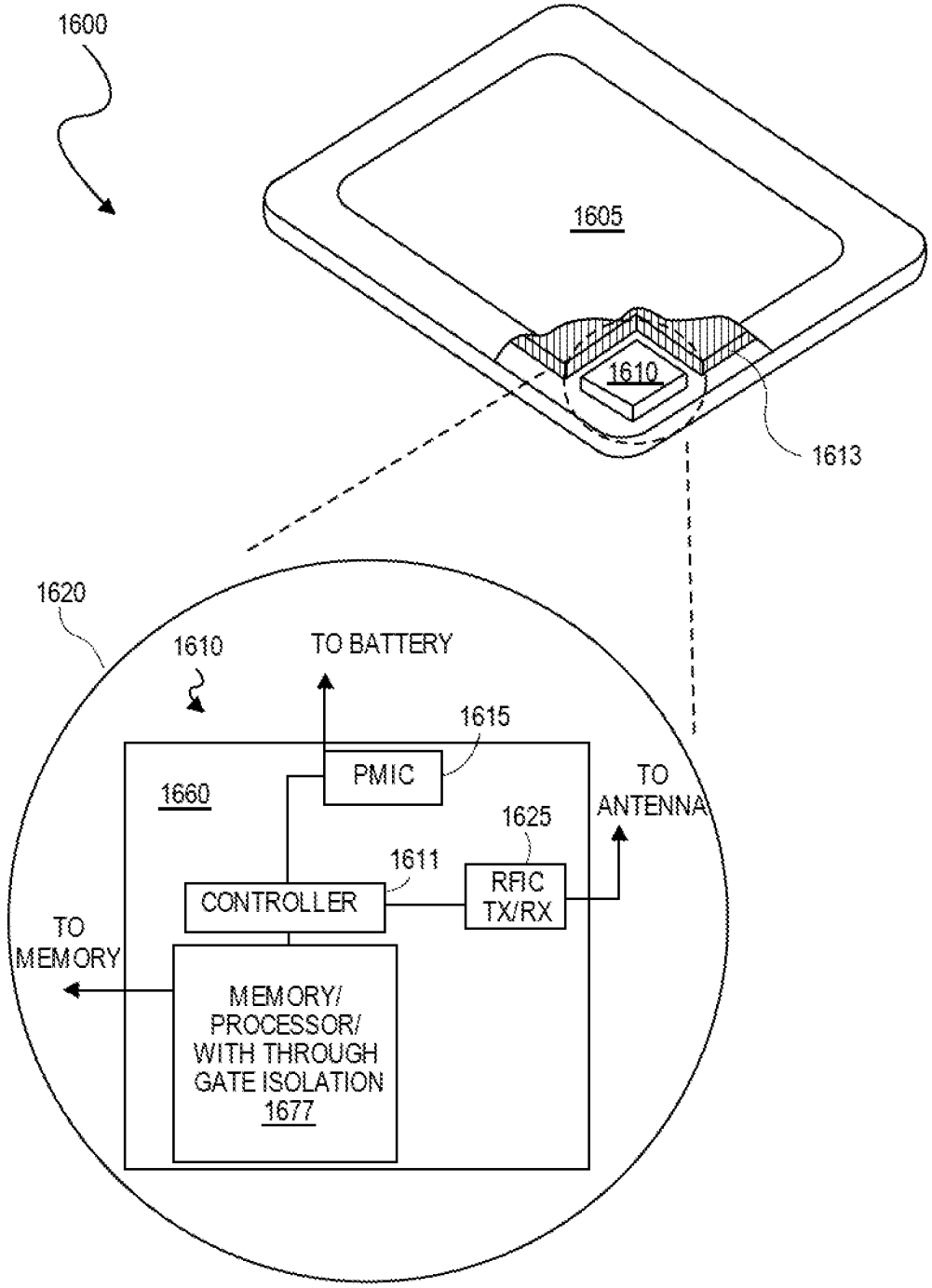
1600
1605
1610
1613
1620
1610
TO BATTERY
1615
PMIC
1660
TO ANTENNA
1625
1611
CONTROLLER
RFIC TX/RX
TO MEMORY
MEMORY/ PROCESSOR/ WITH THROUGH GATE ISOLATION 1677

FIG. 16

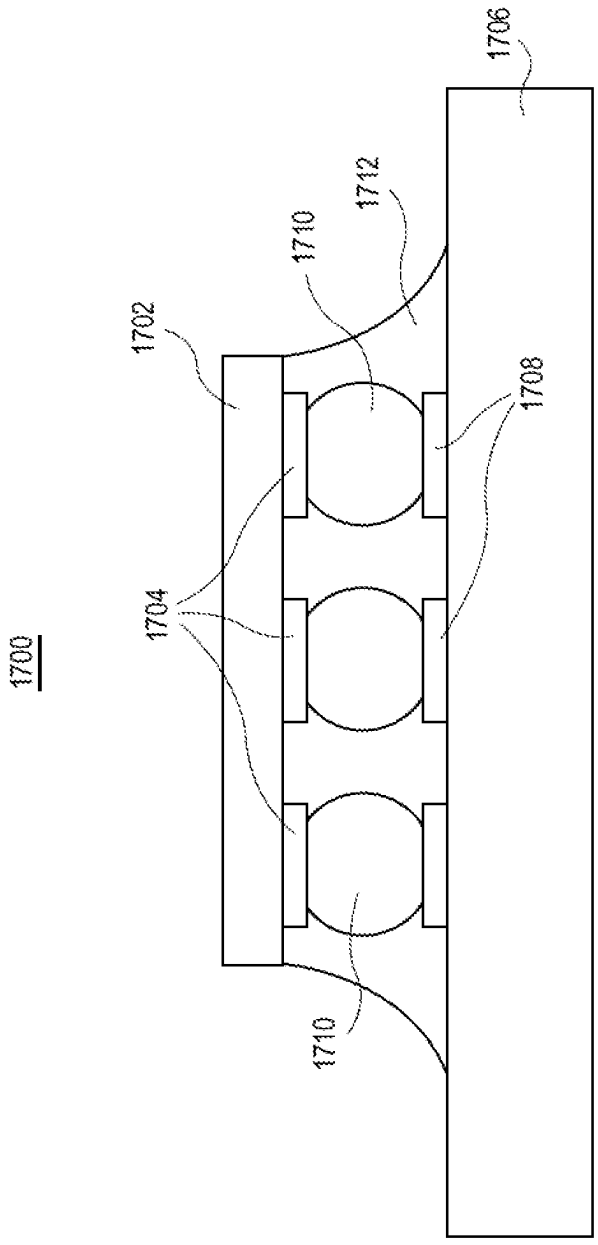

FIG. 17

DIELECTRIC CAPACITANCE RECOVERY OF INTER-LAYER DIELECTRIC LAYERS FOR ADVANCED INTEGRATED CIRCUIT STRUCTURE FABRICATION

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Application No. 63/083,737, entitled "DIELECTRIC CAPACITANCE RECOVERY OF INTER-LAYER DIELECTRIC LAYERS FOR ADVANCED CIRCUIT STRUCTURE FABRICATION," filed on Sep. 25, 2020, the entire contents of which are hereby incorporated by reference herein.

TECHNICAL FIELD

Embodiments of the disclosure are in the field of advanced integrated circuit structure fabrication and, in particular, 10 nanometer node and smaller integrated circuit structure fabrication and the resulting structures.

BACKGROUND

For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips. For example, shrinking transistor size allows for the incorporation of an increased number of memory or logic devices on a chip, lending to the fabrication of products with increased capacity. The drive for ever-more capacity, however, is not without issue. The necessity to optimize the performance of each device becomes increasingly significant.

Variability in conventional and currently known fabrication processes may limit the possibility to further extend them into the 10 nanometer node or sub-10 nanometer node range. Consequently, fabrication of the functional components needed for future technology nodes may require the introduction of new methodologies or the integration of new technologies in current fabrication processes or in place of current fabrication processes.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a plot of carbon content evolution in ILD during interconnect patterning, in accordance with an embodiment of the present disclosure.

FIGS. **2**A-**2**D illustrate cross-sectional views representing various operations in a method involving ILD capacitance recovery, in accordance with an embodiment of the present disclosure.

FIG. **3** includes plots showing carbon and moisture content in ILD for POR (standard flow) and C-IMP (carbon implant flow), in accordance with an embodiment of the present disclosure.

FIG. **4** is a plot showing line-to-line capacitance reduction of 30% with C-IMP, in accordance with an embodiment of the present disclosure.

FIG. **5** is a plot showing via contact resistance increase due to contact oxidation, as compared to C-IMP, in accordance with an embodiment of the present disclosure.

FIG. **6** is a schematic of a pitch quartering approach used to fabricate trenches for interconnect structures, in accordance with an embodiment of the present disclosure.

FIG. **7**A illustrates a cross-sectional view of a metallization layer fabricated using pitch quartering scheme, in accordance with an embodiment of the present disclosure.

FIG. **7**B illustrates a cross-sectional view of a metallization layer fabricated using pitch halving scheme above a metallization layer fabricated using pitch quartering scheme, in accordance with an embodiment of the present disclosure.

FIG. **8**A illustrates a cross-sectional view of an integrated circuit structure having a metallization layer with a metal line composition above a metallization layer with a differing metal line composition, in accordance with an embodiment of the present disclosure.

FIG. **8**B illustrates a cross-sectional view of an integrated circuit structure having a metallization layer with a metal line composition coupled to a metallization layer with a differing metal line composition, in accordance with an embodiment of the present disclosure.

FIGS. **9**A-**9**C illustrate cross-section views of individual interconnect lines having various liner and conductive capping structural arrangements, in accordance with an embodiment of the present disclosure.

FIG. **10** illustrates a cross-sectional view of an integrated circuit structure having four metallization layers with a metal line composition and pitch above two metallization layers with a differing metal line composition and smaller pitch, in accordance with an embodiment of the present disclosure.

FIG. **11**A illustrates a plan view and corresponding cross-sectional view taken along the a-a' axis of the plan view of a metallization layer, in accordance with an embodiment of the present disclosure.

FIG. **11**B illustrates a cross-sectional view of a line end or plug, in accordance with an embodiment of the present disclosure.

FIG. **11**C illustrates another cross-sectional view of a line end or plug, in accordance with an embodiment of the present disclosure.

FIGS. **12**A-**12**F illustrate plan views and corresponding cross-sectional views representing various operations in a plug last processing scheme, in accordance with an embodiment of the present disclosure.

FIG. **13**A illustrates a cross-sectional view of a conductive line plug having a seam therein, in accordance with an embodiment of the present disclosure.

FIG. **13**B illustrates a cross-sectional view of a stack of metallization layers including a conductive line plug at a lower metal line location, in accordance with an embodiment of the present disclosure.

FIG. **14** illustrates a computing device in accordance with one implementation of the disclosure.

FIG. **15** illustrates an interposer that includes one or more embodiments of the disclosure.

FIG. **16** is an isometric view of a mobile computing platform employing an IC fabricated according to one or more processes described herein or including one or more features described herein, in accordance with an embodiment of the present disclosure.

FIG. **17** illustrates a cross-sectional view of a flip-chip mounted die, in accordance with an embodiment of the present disclosure.

DESCRIPTION OF THE EMBODIMENTS

Advanced integrated circuit structure fabrication is described. In the following description, numerous specific

details are set forth, such as specific integration and material regimes, in order to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to one skilled in the art that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known features, such as integrated circuit design layouts, are not described in detail in order to not unnecessarily obscure embodiments of the present disclosure. Furthermore, it is to be appreciated that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

The following detailed description is merely illustrative in nature and is not intended to limit the embodiments of the subject matter or the application and uses of such embodiments. As used herein, the word "exemplary" means "serving as an example, instance, or illustration." Any implementation described herein as exemplary is not necessarily to be construed as preferred or advantageous over other implementations. Furthermore, there is no intention to be bound by any expressed or implied theory presented in the preceding technical field, background, brief summary or the following detailed description.

This specification includes references to "one embodiment" or "an embodiment." The appearances of the phrases "in one embodiment" or "in an embodiment" do not necessarily refer to the same embodiment. Particular features, structures, or characteristics may be combined in any suitable manner consistent with this disclosure.

Terminology. The following paragraphs provide definitions or context for terms found in this disclosure (including the appended claims):

"Comprising." This term is open-ended. As used in the appended claims, this term does not foreclose additional structure or operations.

"Configured To." Various units or components may be described or claimed as "configured to" perform a task or tasks. In such contexts, "configured to" is used to connote structure by indicating that the units or components include structure that performs those task or tasks during operation. As such, the unit or component can be said to be configured to perform the task even when the specified unit or component is not currently operational (e.g., is not on or active). Reciting that a unit or circuit or component is "configured to" perform one or more tasks is expressly intended not to invoke 35 U.S.C. § 112, sixth paragraph, for that unit or component.

"First," "Second," etc. As used herein, these terms are used as labels for nouns that they precede, and do not imply any type of ordering (e.g., spatial, temporal, logical, etc.).

"Coupled"—The following description refers to elements or nodes or features being "coupled" together. As used herein, unless expressly stated otherwise, "coupled" means that one element or node or feature is directly or indirectly joined to (or directly or indirectly communicates with) another element or node or feature, and not necessarily mechanically.

In addition, certain terminology may also be used in the following description for the purpose of reference only, and thus are not intended to be limiting. For example, terms such as "upper", "lower", "above", and "below" refer to directions in the drawings to which reference is made. Terms such as "front", "back", "rear", "side", "outboard", and "inboard" describe the orientation or location or both of portions of the component within a consistent but arbitrary frame of reference which is made clear by reference to the text and the associated drawings describing the component under discussion. Such terminology may include the words specifically mentioned above, derivatives thereof, and words of similar import.

"Inhibit"—As used herein, inhibit is used to describe a reducing or minimizing effect. When a component or feature is described as inhibiting an action, motion, or condition it may completely prevent the result or outcome or future state completely. Additionally, "inhibit" can also refer to a reduction or lessening of the outcome, performance, or effect which might otherwise occur. Accordingly, when a component, element, or feature is referred to as inhibiting a result or state, it need not completely prevent or eliminate the result or state.

Embodiments described herein may be directed to front-end-of-line (FEOL) semiconductor processing and structures. FEOL is the first portion of integrated circuit (IC) fabrication where the individual devices (e.g., transistors, capacitors, resistors, etc.) are patterned in the semiconductor substrate or layer. FEOL generally covers everything up to (but not including) the deposition of metal interconnect layers. Following the last FEOL operation, the result is typically a wafer with isolated transistors (e.g., without any wires).

Embodiments described herein may be directed to back end of line (BEOL) semiconductor processing and structures. BEOL is the second portion of IC fabrication where the individual devices (e.g., transistors, capacitors, resistors, etc.) get interconnected with wiring on the wafer, e.g., the metallization layer or layers. BEOL includes contacts, insulating layers (dielectrics), metal levels, and bonding sites for chip-to-package connections. In the BEOL part of the fabrication stage contacts (pads), interconnect wires, vias and dielectric structures are formed. For modern IC processes, more than 10 metal layers may be added in the BEOL.

Embodiments described below may be applicable to FEOL processing and structures, BEOL processing and structures, or both FEOL and BEOL processing and structures. In particular, although an exemplary processing scheme may be illustrated using a FEOL processing scenario, such approaches may also be applicable to BEOL processing. Likewise, although an exemplary processing scheme may be illustrated using a BEOL processing scenario, such approaches may also be applicable to FEOL processing.

It is to be appreciated that, in an embodiment, FEOL is a technology driver for a given process. In other embodiments, FEOL considerations are driven by BEOL 10 nanometer or sub-10 nanometer processing requirements. For example, material selection and layouts for FEOL layers and devices may need to accommodate BEOL processing. In one such embodiment, material selection and gate stack architectures are selected to accommodate high density metallization of the BEOL layers, e.g., to reduce fringe capacitance in transistor structures formed in the FEOL layers but coupled together by high density metallization of the BEOL layers.

Back end of line (BEOL) layers of integrated circuits commonly include electrically conductive microelectronic structures, which are known in the arts as vias, to electrically connect metal lines or other interconnects above the vias to metal lines or other interconnects below the vias. Vias may be formed by a lithographic process. Representatively, a photoresist layer may be spin coated over a dielectric layer, the photoresist layer may be exposed to patterned actinic radiation through a patterned mask, and then the exposed layer may be developed in order to form an opening in the photoresist layer. Next, an opening for the via may be etched

in the dielectric layer by using the opening in the photoresist layer as an etch mask. This opening is referred to as a via opening. Finally, the via opening may be filled with one or more metals or other conductive materials to form the via.

Sizes and the spacing of vias has progressively decreased, and it is expected that in the future the sizes and the spacing of the vias will continue to progressively decrease, for at least some types of integrated circuits (e.g., advanced microprocessors, chipset components, graphics chips, etc.). When patterning extremely small vias with extremely small pitches by such lithographic processes, several challenges present themselves. One such challenge is that the overlay between the vias and the overlying interconnects, and the overlay between the vias and the underlying landing interconnects, generally need to be controlled to high tolerances on the order of a quarter of the via pitch. As via pitches scale ever smaller over time, the overlay tolerances tend to scale with them at an even greater rate than lithographic equipment is able to keep up.

Another such challenge is that the critical dimensions of the via openings generally tend to scale faster than the resolution capabilities of the lithographic scanners. Shrink technologies exist to shrink the critical dimensions of the via openings. However, the shrink amount tends to be limited by the minimum via pitch, as well as by the ability of the shrink process to be sufficiently optical proximity correction (OPC) neutral, and to not significantly compromise line width roughness (LWR) or critical dimension uniformity (CDU), or both. Yet another such challenge is that the LWR or CDU, or both, characteristics of photoresists generally need to improve as the critical dimensions of the via openings decrease in order to maintain the same overall fraction of the critical dimension budget.

The above factors are also relevant for considering placement and scaling of non-conductive spaces or interruptions between metal lines (referred to as "plugs," "dielectric plugs" or "metal line ends" among the metal lines of back end of line (BEOL) metal interconnect structures. Thus, improvements are needed in the area of back end metallization manufacturing technologies for fabricating inter-layer dielectric layers, metal lines, metal vias, and dielectric plugs.

In accordance with one or more embodiments of the present disclosure, inter-layer dielectric (ILD) capacitance (Cap or CAP) improvement is described.

Embodiments described in the present disclosure can be implemented to provide the capability to recover the capacitance of SiO_XC_Y based interlayer dielectric (ILD) by implanting carbon and removing moisture from ILD. Such approaches can aid with improving the performance and yield of products including integrated circuit structures.

To provide context, ILD used for backend interconnects for transistors are doped with carbon to improve their capacitance. During backend processing, aggressive plasma and oxidizing chemistry drives out most of the carbon from the ILD. It can also render ILD porous leading it to absorb moisture. The moisture can act as a virtual source for oxidation of next layer via contacts during thermal processing downstream resulting in highly resistive contacts and loss of yield.

FIG. **1** is a plot **100** of carbon content evolution in ILD during interconnect patterning, in accordance with an embodiment of the present disclosure. The evolution is poor with respect to carbon retention, particularly between trenches or lines, and there is significant cost associated with developing new processing tools to improve retention of carbon.

Previous attempts have been to increase the carbon content of as-deposited inter-layer dielectric (ILD) materials. Such approaches come with the risk of poor structural quality of ILD against different processing operations. Trying new chemistries which are less impactful on ILD has not been a viable solution as the process margin is associated with high cost and high risk.

Embodiments described herein can be implemented to repair damage to ILD by performing an implant post processing followed by thermal anneal to increase carbon content and drive out any moisture. Such an approach can be implemented to prevent interaction with the patterning process as well as protect upper layer contacts from exposure to moisture embedded in the ILD. Embodiments described herein can be implemented as a lower cost, simpler solution than integrating high carbon content new ILD material. Additionally, the approach offers flexibility to be fine-tuned for future upstream or downstream changes. EDX or SIMS profile can be used to show higher carbon content formed during such an approach.

Embodiments described herein can be implemented to repair an ILD film by implanting carbon therein using a direct beam technique. The implant can be followed by a high temperature anneal to drive out moisture from the ILD. Such a 2-operation approach can be implemented to lower the line-to-line capacitance by about 30%. It can also be implemented to lower the rate of oxidation of upper layer via contacts by about 50%, thus improving the yield.

To provide further context, current processing techniques require aggressive etches for high fidelity patterned structures. Such aggressive etches can drive out a significant amount of carbon from the ILD and at the same time making ILD porous. A relatively low level of carbon in ILD results in a higher dielectric constant which causes capacitance to increase and performance to degrade. Also, during wet cleans, a porous ILD can soak up moisture which acts as a virtual source for oxidizing next layer via contacts. With a carbon-based implant flow (C-IMP), ILD can be repaired in-situ without significant change in process flow. In an embodiment, the carbon level is increased to match the bulk of ILD while moisture level is driven down (e.g., see FIG. **3**, described below). This can help drive down the capacitance in between trenches by 30% (e.g., see FIG. **4**, described below). In an embodiment, next layer via contact resistance can become stable through the rest of downstream processing (e.g., see FIG. **5**, described below) as moisture, the virtual source of oxidation has been eliminated. In an embodiment, implementing such an approach leads to about 1% performance improvement as well as significant yield improvement.

It has be discovered that without C-IMP, post metal trench formation, most of the carbon in upper part of ILD is driven out and moisture is soaked up, while with C-IMP, ILD is repaired post trench formation. As an exemplary processing scheme including a C-IMP process, FIGS. **2**A-**2**D illustrate cross-sectional views representing various operations in a method involving ILD capacitance recovery, in accordance with an embodiment of the present disclosure.

Referring to FIG. **2**A, a starting structure **200** includes an inter-layer dielectric (ILD) layer **204** above a substrate **202**. Substrate **202** can represent an underlying metallization layer ultimately formed above a silicon substrate, or a layer of front end of line (FEOL) devices formed in and/or above a silicon substrate.

Referring to FIG. **2**B, interconnect line openings **206** (and, in some cases, corresponding via openings **207**) are formed in ILD layer **204** to form patterned ILD layer **204**A.

Referring to FIG. **2**C, conductive lines and corresponding vias are formed in the openings **206** and **207**. In a particular embodiment, a conductive fill **208** and barrier layer **209** are formed in openings **206** and **207**. In an embodiment, the processes involved in forming the conductive lines and corresponding vias depletes carbon from at least the upper portion of the patterned ILD layer **204**A to form carbon-depleted patterned ILD layer **204**B, having carbon-depleted region **210**B and, possibly, non-depleted region **210**A. In an embodiment, the formation of carbon-depleted region **210**B leads to a relatively high capacitance **212** between a first conductive interconnect line (e.g., left line) and a second conductive interconnect line (e.g., middle line).

Referring to FIG. **2**D, an implant process **213** is implemented to implant carbon into the carbon-depleted patterned ILD layer **204**B. The implant process **213** forms a restored ILD layer **204**C including a carbon dopant region **210**C. In an embodiment, the formation of carbon dopant region **210**C leads to a reduced capacitance between the first conductive interconnect line (e.g., left line) and the second conductive interconnect line (e.g., middle line) as compared with capacitance **212**. In an embodiment, the implant process is followed by an annealing process.

In an embodiment, the implanting carbon into the ILD layer (**204**) includes implanting using a direct beam technique. In an embodiment, the implanting carbon into the ILD layer (**204**) and annealing the ILD layer reduces a line-to-line capacitance between the first (e.g., left line) and the second conductive interconnect lines (e.g., middle line). In an embodiment, the implanting carbon into the ILD layer (**204**) and annealing the ILD layer reduces a moisture content of the ILD layer. In an embodiment, the implanting carbon into the ILD layer (**204**) and annealing the ILD layer forms a carbon dopant region **210**C having a depth **214**A in the ILD layer approximately the same as a depth of the first and second conductive interconnect lines.

Referring again to FIG. **2**D, in accordance with an embodiment of the present disclosure, an integrated circuit structure includes a single dielectric layer **204**C above a substrate **202**. A plurality of conductive lines **208**/**209** is in an upper portion of the single dielectric layer **204**C above a lower portion **210**A of the single dielectric layer **204**C. A carbon dopant region **210**C is in the upper portion of the single dielectric layer **204**C. The carbon dopant region **210**C between adjacent ones of the plurality of conductive lines **208**/**209**.

In an embodiment, the single dielectric layer **204**C is composed of a carbon-doped silicon oxide (CDO) material. In one such embodiment, the CDO material has a greater carbon concentration in the lower portion of the single dielectric layer than in the upper portion of the single dielectric layer. In a particular such embodiment, a total carbon concentration of the CDO material in the upper portion of the single dielectric layer combined with the carbon dopant region **210**C is about the same as the carbon concentration in the lower portion **210**A of the single dielectric layer **204**C.

In an embodiment, the carbon dopant region **210**C has a depth **214**A in the single dielectric layer **204**C approximately the same as a depth of the plurality of conductive lines, as is depicted. In another embodiment, the carbon dopant region **210**C has a depth **214**B in the single dielectric layer **204**C less than a depth of the plurality of conductive lines. In another embodiment, the carbon dopant region **210**C has a depth **214**C in the single dielectric layer **204**C greater than a depth of the plurality of conductive lines. In another embodiment, the carbon dopant region **210**C has a depth **214**D about the same as the thickness of the single dielectric layer **204**C. In an embodiment, the carbon dopant region **210**C has a depth in the single dielectric layer **204**C in a range of 10-20 nanometers.

In an embodiment, the conductive fill **208** is cobalt, i.e., the plurality of conductive lines **208**/**209** is a plurality of cobalt-based lines. In an embodiment, a copper-based via is ultimately formed on one of the plurality of conductive lines **208**/**209**. In one such embodiment, the implanting carbon into the ILD layer (**204**) reduces the possibility or extend of oxidation of the copper-based via.

FIG. **3** includes plots **300** showing carbon and moisture content in ILD for process of record (POR, standard flow, right-hand-side plot) and carbon-based implant (C-IMP, carbon implant flow, left-hand-side plot), in accordance with an embodiment of the present disclosure. FIG. **4** is a plot **400** showing line-to-line capacitance reduction of 30% with C-IMP, in accordance with an embodiment of the present disclosure. FIG. **5** is a plot **500** showing via contact resistance increase due to contact oxidation, as compared to C-IMP, in accordance with an embodiment of the present disclosure. C-IMP process flow can reduce via contact resistance by greater than 50%.

In another aspect, a pitch quartering approach is implemented for patterning trenches in a dielectric layer for forming BEOL interconnect structures. In accordance with an embodiment of the present disclosure, pitch division is applied for fabricating metal lines in a BEOL fabrication scheme. Embodiments may enable continued scaling of the pitch of metal layers beyond the resolution capability of state-of-the art lithography equipment.

FIG. **6** is a schematic of a pitch quartering approach 600 used to fabricate trenches for interconnect structures, in accordance with an embodiment of the present disclosure.

Referring to FIG. **6**, at operation (a), backbone features **602** are formed using direct lithography. For example, a photoresist layer or stack may be patterned and the pattern transferred into a hardmask material to ultimately form backbone features **602**. The photoresist layer or stack used to form backbone features **602** may be patterned using standard lithographic processing techniques, such as 193 immersion lithography. First spacer features **604** are then formed adjacent the sidewalls of the backbone features **602**.

At operation (b), the backbone features **602** are removed to leave only the first spacer features **604** remaining. At this stage, the first spacer features **604** are effectively a half pitch mask, e.g., representing a pitch halving process. The first spacer features **604** can either be used directly for a pitch quartering process, or the pattern of the first spacer features **604** may first be transferred into a new hardmask material, where the latter approach is depicted.

At operation (c), the pattern of the first spacer features **604** transferred into a new hardmask material to form first spacer features **604'**. Second spacer features **606** are then formed adjacent the sidewalls of the first spacer features **604'**.

At operation (d), the first spacer features **604'** are removed to leave only the second spacer features **606** remaining. At this stage, the second spacer features **606** are effectively a quarter pitch mask, e.g., representing a pitch quartering process.

At operation (e), the second spacer features **606** are used as a mask to pattern a plurality of trenches **608** in a dielectric or hardmask layer. The trenches may ultimately be filled with conductive material to form conductive interconnects in metallization layers of an integrated circuit. Trenches **608** having the label "B" correspond to backbone features **602**. Trenches **608** having the label "S" correspond to first spacer

features **604** or **604'**. Trenches **608** having the label "C" correspond to a complementary region **607** between backbone features **602**.

It is to be appreciated that since individual ones of the trenches **608** of FIG. **6** have a patterning origin that corresponds to one of backbone features **602**, first spacer features **604** or **604'**, or complementary region **607** of FIG. **6**, differences in width and/or pitch of such features may appear as artifacts of a pitch quartering process in ultimately formed conductive interconnects in metallization layers of an integrated circuit. As an example, FIG. **7**A illustrates a cross-sectional view of a metallization layer fabricated using pitch quartering scheme, in accordance with an embodiment of the present disclosure.

Referring to FIG. **7**A, an integrated circuit structure **700** includes an inter-layer dielectric (ILD) layer **704** above a substrate **702**. A plurality of conductive interconnect lines **706** is in the ILD layer **704**, and individual ones of the plurality of conductive interconnect lines **706** are spaced apart from one another by portions of the ILD layer **704**. Individual ones of the plurality of conductive interconnect lines **706** includes a conductive barrier layer **708** and a conductive fill material **710**.

With reference to both FIGS. **6** and **7**A, conductive interconnect lines **706**B are formed in trenches with a pattern originating from backbone features **602**. Conductive interconnect lines **706**S are formed in trenches with a pattern originating from first spacer features **604** or **604'**. Conductive interconnect lines **706**C are formed in trenches with a pattern originating from complementary region **607** between backbone features **602**.

Referring again to FIG. **7**A, in an embodiment, the plurality of conductive interconnect lines **706** includes a first interconnect line **706**B having a width (W**1**). A second interconnect line **706**S is immediately adjacent the first interconnect line **706**B, the second interconnect line **706**S having a width (W**2**) different than the width (W**1**) of the first interconnect line **706**B. A third interconnect line **706**C is immediately adjacent the second interconnect line **706**S, the third interconnect line **706**C having a width (W**3**). A fourth interconnect line (second **706**S) immediately adjacent the third interconnect line **706**C, the fourth interconnect line having a width (W**2**) the same as the width (W**2**) of the second interconnect line **706**S. A fifth interconnect line (second **706**B) is immediately adjacent the fourth interconnect line (second **706**S), the fifth interconnect line (second **706**B) having a width (W**1**) the same as the width (W**1**) of the first interconnect line **706**B.

In an embodiment, the width (W**3**) of the third interconnect line **706**C is different than the width (W**1**) of the first interconnect line **706**B. In one such embodiment, the width (W**3**) of the third interconnect line **706**C is different than the width (W**2**) of the second interconnect line **706**S. In another such embodiment, the width (W**3**) of the third interconnect line **706**C is the same as the width (W**2**) of the second interconnect line **706**S. In another embodiment, the width (W**3**) of the third interconnect line **706**C is the same as the width (W**1**) of the first interconnect line **706**B.

In an embodiment, a pitch (P**1**) between the first interconnect line **706**B and the third interconnect line **706**C is the same as a pitch (P**2**) between the second interconnect **706**S line and the fourth interconnect line (second **706**S). In another embodiment, a pitch (P**1**) between the first interconnect line **706**B and the third interconnect line **706**C is different than a pitch (P**2**) between the second interconnect line **706**S and the fourth interconnect line (second **706**S).

Referring again to FIG. **7**A, in another embodiment, the plurality of conductive interconnect lines **706** includes a first interconnect line **706**B having a width (W**1**). A second interconnect line **706**S is immediately adjacent the first interconnect line **706**B, the second interconnect line **706**S having a width (W**2**). A third interconnect line **706**C is immediately adjacent the second interconnect line **706**S, the third interconnect line **706**S having a width (W**3**) different than the width (W**1**) of the first interconnect line **706**B. A fourth interconnect line (second **706**S) is immediately adjacent the third interconnect line **706**C, the fourth interconnect line having a width (W**2**) the same as the width (W**2**) of the second interconnect line **706**S. A fifth interconnect line (second **706**B) is immediately adjacent the fourth interconnect line (second **706**S), the fifth interconnect line (second **706**B) having a width (W**1**) the same as the width (W**1**) of the first interconnect line **706**B.

In an embodiment, the width (W**2**) of the second interconnect line **706**S is different than the width (W**1**) of the first interconnect line **706**B. In one such embodiment, the width (W**3**) of the third interconnect line **706**C is different than the width (W**2**) of the second interconnect line **706**S. In another such embodiment, the width (W**3**) of the third interconnect line **706**C is the same as the width (W**2**) of the second interconnect line **706**S.

In an embodiment, the width (W**2**) of the second interconnect line **706**S is the same as the width (W**1**) of the first interconnect line **706**B. In an embodiment, a pitch (P**1**) between the first interconnect line **706**B and the third interconnect line **706**C is the same as a pitch (P**2**) between the second interconnect line **706**S and the fourth interconnect line (second **706**S). In an embodiment, a pitch (P**1**) between the first interconnect line **706**B and the third interconnect line **706**C is different than a pitch (P**2**) between the second interconnect line **706**S and the fourth interconnect line (second **706**S).

FIG. **7**B illustrates a cross-sectional view of a metallization layer fabricated using pitch halving scheme above a metallization layer fabricated using pitch quartering scheme, in accordance with an embodiment of the present disclosure.

Referring to FIG. **7**B, an integrated circuit structure **750** includes a first inter-layer dielectric (ILD) layer **754** above a substrate **752**. A first plurality of conductive interconnect lines **756** is in the first ILD layer **754**, and individual ones of the first plurality of conductive interconnect lines **756** are spaced apart from one another by portions of the first ILD layer **754**. Individual ones of the plurality of conductive interconnect lines **756** includes a conductive barrier layer **758** and a conductive fill material **760**. The integrated circuit structure **750** further includes a second inter-layer dielectric (ILD) layer **774** above substrate **752**. A second plurality of conductive interconnect lines **776** is in the second ILD layer **774**, and individual ones of the second plurality of conductive interconnect lines **776** are spaced apart from one another by portions of the second ILD layer **774**. Individual ones of the plurality of conductive interconnect lines **776** includes a conductive barrier layer **778** and a conductive fill material **780**.

In accordance with an embodiment of the present disclosure, with reference again to FIG. **7**B, a method of fabricating an integrated circuit structure includes forming a first plurality of conductive interconnect lines **756** in and spaced apart by a first inter-layer dielectric (ILD) layer **754** above a substrate **752**. The first plurality of conductive interconnect lines **756** is formed using a spacer-based pitch quartering process, e.g., the approach described in association with operations (a)-(e) of FIG. **6**. A second plurality of conductive

interconnect lines **776** is formed in and is spaced apart by a second ILD layer **774** above the first ILD layer **754**. The second plurality of conductive interconnect lines **776** is formed using a spacer-based pitch halving process, e.g., the approach described in association with operations (a) and (b) of FIG. **6**.

In an embodiment, first plurality of conductive interconnect lines **756** has a pitch (P**1**) between immediately adjacent lines of than 40 nanometers. The second plurality of conductive interconnect lines **776** has a pitch (P**2**) between immediately adjacent lines of 44 nanometers or greater. In an embodiment, the spacer-based pitch quartering process and the spacer-based pitch halving process are based on an immersion 193 nm lithography process.

In an embodiment, individual ones of the first plurality of conductive interconnect lines **754** include a first conductive barrier liner **758** and a first conductive fill material **760**. Individual ones of the second plurality of conductive interconnect lines **776** include a second conductive barrier liner **778** and a second conductive fill material **780**. In one such embodiment, the first conductive fill material **760** is different in composition from the second conductive fill material **780**. In another embodiment, the first conductive fill material **760** is the same in composition as the second conductive fill material **780**.

Although not depicted, in an embodiment, the method further includes forming a third plurality of conductive interconnect lines in and spaced apart by a third ILD layer above the second ILD layer **774**. The third plurality of conductive interconnect lines is formed without using pitch division.

Although not depicted, in an embodiment, the method further includes, prior to forming the second plurality of conductive interconnect lines **776**, forming a third plurality of conductive interconnect lines in and spaced apart by a third ILD layer above the first ILD layer **754**. The third plurality of conductive interconnect lines is formed using a spacer-based pitch quartering process. In one such embodiment, subsequent to forming the second plurality of conductive interconnect lines **776**, a fourth plurality of conductive interconnect lines is formed in and is spaced apart by a fourth ILD layer above the second ILD layer **774**. The fourth plurality of conductive interconnect lines is formed using a spacer-based pitch halving process. In an embodiment, such a method further includes forming a fifth plurality of conductive interconnect lines in and spaced apart by a fifth ILD layer above the fourth ILD layer, the fifth plurality of conductive interconnect lines formed using a spacer-based pitch halving process. A sixth plurality of conductive interconnect lines is then formed in and spaced apart by a sixth ILD layer above the fifth ILD layer, the sixth plurality of conductive interconnect lines formed using a spacer-based pitch halving process. A seventh plurality of conductive interconnect lines is then formed in and spaced apart by a seventh ILD layer above the sixth ILD layer. The seventh plurality of conductive interconnect lines is formed without using pitch division.

In another aspect, metal line compositions vary between metallization layers. Such an arrangement may be referred to as heterogeneous metallization layers. In an embodiment, copper is used as a conductive fill material for relatively larger interconnect lines, while cobalt is used as a conductive fill material for relatively smaller interconnect lines. The smaller lines having cobalt as a fill material may provide reduced electromigration while maintaining low resistivity. The use of cobalt in place of copper for smaller interconnect lines may address issues with scaling copper lines, where a conductive barrier layer consumes a greater amount of an interconnect volume and copper is reduced, essentially hindering advantages normally associated with a copper interconnect line.

In a first example, FIG. **8**A illustrates a cross-sectional view of an integrated circuit structure having a metallization layer with a metal line composition above a metallization layer with a differing metal line composition, in accordance with an embodiment of the present disclosure.

Referring to FIG. **8**A, an integrated circuit structure **800** includes a first plurality of conductive interconnect lines **806** in and spaced apart by a first inter-layer dielectric (ILD) layer **804** above a substrate **802**. One of the conductive interconnect lines **806**A is shown as having an underlying via **807**. Individual ones of the first plurality of conductive interconnect lines **806** include a first conductive barrier material **808** along sidewalls and a bottom of a first conductive fill material **810**. In an embodiment, a carbon dopant region **849** is included at least in the first ILD layer **804**, as is depicted.

A second plurality of conductive interconnect lines **816** is in and spaced apart by a second ILD layer **814** above the first ILD layer **804**. One of the conductive interconnect lines **816**A is shown as having an underlying via **817**. Individual ones of the second plurality of conductive interconnect lines **816** include a second conductive barrier material **818** along sidewalls and a bottom of a second conductive fill material **820**. The second conductive fill material **820** is different in composition from the first conductive fill material **810**.

In an embodiment, the second conductive fill material **820** consists essentially of copper, and the first conductive fill material **810** consists essentially of cobalt. In one such embodiment, the first conductive barrier material **808** is different in composition from the second conductive barrier material **818**. In another such embodiment, the first conductive barrier material **808** is the same in composition as the second conductive barrier material **818**.

In an embodiment, the first conductive fill material **810** includes copper having a first concentration of a dopant impurity atom, and the second conductive fill material **820** includes copper having a second concentration of the dopant impurity atom. The second concentration of the dopant impurity atom is less than the first concentration of the dopant impurity atom. In one such embodiment, the dopant impurity atom is selected from the group consisting of aluminum (Al) and manganese (Mn). In an embodiment, the first conductive barrier material **810** and the second conductive barrier material **820** have the same composition. In an embodiment, the first conductive barrier material **810** and the second conductive barrier material **820** have a different composition.

Referring again to FIG. **8**A, the second ILD layer **814** is on an etch-stop layer **822**. The conductive via **817** is in the second ILD layer **814** and in an opening of the etch-stop layer **822**. In an embodiment, the first and second ILD layers **804** and **814** include silicon, carbon and oxygen, and the etch-stop layer **822** includes silicon and nitrogen. In an embodiment, individual ones of the first plurality of conductive interconnect lines **806** have a first width (W**1**), and individual ones of the second plurality of conductive interconnect lines **816** have a second width (W**2**) greater than the first width (W**1**).

In a second example, FIG. **8**B illustrates a cross-sectional view of an integrated circuit structure having a metallization layer with a metal line composition coupled to a metallization layer with a differing metal line composition, in accordance with an embodiment of the present disclosure.

Referring to FIG. **8**B, an integrated circuit structure **850** includes a first plurality of conductive interconnect lines **856** in and spaced apart by a first inter-layer dielectric (ILD) layer **854** above a substrate **852**. One of the conductive interconnect lines **856**A is shown as having an underlying via **857**. Individual ones of the first plurality of conductive interconnect lines **856** include a first conductive barrier material **858** along sidewalls and a bottom of a first conductive fill material **860**. In an embodiment, a carbon dopant region **899** is included at least in the first ILD layer **854**, as is depicted.

A second plurality of conductive interconnect lines **866** is in and spaced apart by a second ILD layer **864** above the first ILD layer **854**. One of the conductive interconnect lines **866**A is shown as having an underlying via **867**. Individual ones of the second plurality of conductive interconnect lines **866** include a second conductive barrier material **868** along sidewalls and a bottom of a second conductive fill material **870**. The second conductive fill material **870** is different in composition from the first conductive fill material **860**.

In an embodiment, the conductive via **867** is on and electrically coupled to an individual one **856**B of the first plurality of conductive interconnect lines **856**, electrically coupling the individual one **866**A of the second plurality of conductive interconnect lines **866** to the individual one **856**B of the first plurality of conductive interconnect lines **856**. In an embodiment, individual ones of the first plurality of conductive interconnect lines **856** are along a first direction **898** (e.g., into and out of the page), and individual ones of the second plurality of conductive interconnect lines **866** are along a second direction **899** orthogonal to the first direction **898**, as is depicted. In an embodiment, the conductive via **867** includes the second conductive barrier material **868** along sidewalls and a bottom of the second conductive fill material **870**, as is depicted.

In an embodiment, the second ILD layer **864** is on an etch-stop layer **872** on the first ILD layer **854**. The conductive via **867** is in the second ILD layer **864** and in an opening of the etch-stop layer **872**. In an embodiment, the first and second ILD layers **854** and **864** include silicon, carbon and oxygen, and the etch-stop layer **872** includes silicon and nitrogen. In an embodiment, individual ones of the first plurality of conductive interconnect lines **856** have a first width, and individual ones of the second plurality of conductive interconnect lines **866** have a second width greater than the first width.

In an embodiment, the second conductive fill material **870** consists essentially of copper, and the first conductive fill material **860** consists essentially of cobalt. In one such embodiment, the first conductive barrier material **858** is different in composition from the second conductive barrier material **868**. In another such embodiment, the first conductive barrier material **858** is the same in composition as the second conductive barrier material **868**.

In an embodiment, the first conductive fill material **860** includes copper having a first concentration of a dopant impurity atom, and the second conductive fill material **870** includes copper having a second concentration of the dopant impurity atom. The second concentration of the dopant impurity atom is less than the first concentration of the dopant impurity atom. In one such embodiment, the dopant impurity atom is selected from the group consisting of aluminum (Al) and manganese (Mn). In an embodiment, the first conductive barrier material **860** and the second conductive barrier material **870** have the same composition. In an embodiment, the first conductive barrier material **860** and the second conductive barrier material **870** have a different composition.

FIGS. **9**A-**9**C illustrate cross-section views of individual interconnect lines having various barrier liner and conductive capping structural arrangements suitable for the structures described in association with FIGS. **8**A and **8**B, in accordance with an embodiment of the present disclosure.

Referring to FIG. **9**A, an interconnect line **900** in a dielectric layer **901** includes a conductive barrier material **902** and a conductive fill material **904**. The conductive barrier material **902** includes an outer layer **906** distal from the conductive fill material **904** and an inner layer **908** proximate to the conductive fill material **904**. In an embodiment, the conductive fill material includes cobalt, the outer layer **906** includes titanium and nitrogen, and the inner layer **908** includes tungsten, nitrogen and carbon. In one such embodiment, the outer layer **906** has a thickness of approximately 2 nanometers, and the inner layer **908** has a thickness of approximately 0.5 nanometers. In another embodiment, the conductive fill material includes cobalt, the outer layer **906** includes tantalum, and the inner layer **908** includes ruthenium. In one such embodiment, the outer layer **906** further includes nitrogen.

Referring to FIG. **9**B, an interconnect line **920** in a dielectric layer **921** includes a conductive barrier material **922** and a conductive fill material **924**. A conductive cap layer **930** is on a top of the conductive fill material **924**. In one such embodiment, the conductive cap layer **930** is further on a top of the conductive barrier material **922**, as is depicted. In another embodiment, the conductive cap layer **930** is not on a top of the conductive barrier material **922**. In an embodiment, the conductive cap layer **930** consists essentially of cobalt, and the conductive fill material **924** consists essentially of copper.

Referring to FIG. **9**C, an interconnect line **940** in a dielectric layer **941** includes a conductive barrier material **942** and a conductive fill material **944**. The conductive barrier material **942** includes an outer layer **946** distal from the conductive fill material **944** and an inner layer **948** proximate to the conductive fill material **944**. A conductive cap layer **950** is on a top of the conductive fill material **944**. In one embodiment, the conductive cap layer **950** is only a top of the conductive fill material **944**. In another embodiment, however, the conductive cap layer **950** is further on a top of the inner layer **948** of the conductive barrier material **942**, i.e., at location **952**. In one such embodiment, the conductive cap layer **950** is further on a top of the outer layer **946** of the conductive barrier material **942**, i.e., at location **954**.

In an embodiment, with reference to FIGS. **9**B and **9**C, a method of fabricating an integrated circuit structure includes forming an inter-layer dielectric (ILD) layer **921** or **941** above a substrate. A plurality of conductive interconnect lines **920** or **940** is formed in trenches in and spaced apart by the ILD layer, individual ones of the plurality of conductive interconnect lines **920** or **940** in a corresponding one of the trenches. The plurality of conductive interconnect lines is formed by first forming a conductive barrier material **922** or **942** on bottoms and sidewalls of the trenches, and then forming a conductive fill material **924** or **944** on the conductive barrier material **922** or **942**, respectively, and filling the trenches, where the conductive barrier material **922** or **942** is along a bottom of and along sidewalls of the conductive fill material **924** or **944**, respectively. The top of the conductive fill material **924** or **944** is then treated with a gas including oxygen and carbon. Subsequent to treating the top

of the conductive fill material **924** or **944** with the gas including oxygen and carbon, a conductive cap layer **930** or **950** is formed on the top of the conductive fill material **924** or **944**, respectively.

In one embodiment, treating the top of the conductive fill material **924** or **944** with the gas including oxygen and carbon includes treating the top of the conductive fill material **924** or **944** with carbon monoxide (CO). In one embodiment, the conductive fill material **924** or **944** includes copper, and forming the conductive cap layer **930** or **950** on the top of the conductive fill material **924** or **944** includes forming a layer including cobalt using chemical vapor deposition (CVD). In one embodiment, the conductive cap layer **930** or **950** is formed on the top of the conductive fill material **924** or **944**, but not on a top of the conductive barrier material **922** or **942**.

In one embodiment, forming the conductive barrier material **922** or **942** includes forming a first conductive layer on the bottoms and sidewalls of the trenches, the first conductive layer including tantalum. A first portion of the first conductive layer is first formed using atomic layer deposition (ALD) and then a second portion of the first conductive layer is then formed using physical vapor deposition (PVD). In one such embodiment, forming the conductive barrier material further includes forming a second conductive layer on the first conductive layer on the bottoms and sidewalls of the trenches, the second conductive layer including ruthenium, and the conductive fill material including copper. In one embodiment, the first conductive layer further includes nitrogen.

FIG. **10** illustrates a cross-sectional view of an integrated circuit structure having four metallization layers with a metal line composition and pitch above two metallization layers with a differing metal line composition and smaller pitch, in accordance with an embodiment of the present disclosure.

Referring to FIG. **10**, an integrated circuit structure **1000** includes a first plurality of conductive interconnect lines **1004** in and spaced apart by a first inter-layer dielectric (ILD) layer **1002** above a substrate **1001**. Individual ones of the first plurality of conductive interconnect lines **1004** include a first conductive barrier material **1006** along sidewalls and a bottom of a first conductive fill material **1008**. Individual ones of the first plurality of conductive interconnect lines **1004** are along a first direction **1098** (e.g., into and out of the page). In an embodiment, a carbon dopant region **1095** is included in the first ILD layer **1002**, as is depicted.

A second plurality of conductive interconnect lines **1014** is in and spaced apart by a second ILD layer **1012** above the first ILD layer **1002**. Individual ones of the second plurality of conductive interconnect lines **1014** include the first conductive barrier material **1006** along sidewalls and a bottom of the first conductive fill material **1008**. Individual ones of the second plurality of conductive interconnect lines **1014** are along a second direction **1099** orthogonal to the first direction **1098**. In an embodiment, a carbon dopant region **1095** is included in the second ILD layer **1012**, as is depicted.

A third plurality of conductive interconnect lines **1024** is in and spaced apart by a third ILD layer **1022** above the second ILD layer **1012**. Individual ones of the third plurality of conductive interconnect lines **1024** include a second conductive barrier material **1026** along sidewalls and a bottom of a second conductive fill material **1028**. The second conductive fill material **1028** is different in composition from the first conductive fill material **1008**. Individual ones of the third plurality of conductive interconnect lines **1024** are along the first direction **1098**. In an embodiment, a carbon dopant region **1095** is included in the third ILD layer **1022**, as is depicted.

A fourth plurality of conductive interconnect lines **1034** is in and spaced apart by a fourth ILD layer **1032** above the third ILD layer **1022**. Individual ones of the fourth plurality of conductive interconnect lines **1034** include the second conductive barrier material **1026** along sidewalls and a bottom of the second conductive fill material **1028**. Individual ones of the fourth plurality of conductive interconnect lines **1034** are along the second direction **1099**. In an embodiment, although not depicted, a carbon dopant region is included in the fourth ILD layer **1032**.

A fifth plurality of conductive interconnect lines **1044** is in and spaced apart by a fifth ILD layer **1042** above the fourth ILD layer **1032**. Individual ones of the fifth plurality of conductive interconnect lines **1044** include the second conductive barrier material **1026** along sidewalls and a bottom of the second conductive fill material **1028**. Individual ones of the fifth plurality of conductive interconnect lines **1044** are along the first direction **1098**. In an embodiment, although not depicted, a carbon dopant region is included in the fifth ILD layer **1042**.

A sixth plurality of conductive interconnect lines **1054** is in and spaced apart by a sixth ILD layer **1052** above the fifth ILD layer **1044**. Individual ones of the sixth plurality of conductive interconnect lines **1054** include the second conductive barrier material **1026** along sidewalls and a bottom of the second conductive fill material **1028**. Individual ones of the sixth plurality of conductive interconnect lines **1054** are along the second direction **1099**. In an embodiment, although not depicted, a carbon dopant region is included in the sixth ILD layer **1052**.

In an embodiment, the second conductive fill material **1028** consists essentially of copper, and the first conductive fill material **1008** consists essentially of cobalt. In an embodiment, the first conductive fill material **1008** includes copper having a first concentration of a dopant impurity atom, and the second conductive fill material **1028** includes copper having a second concentration of the dopant impurity atom, the second concentration of the dopant impurity atom less than the first concentration of the dopant impurity atom.

In an embodiment, the first conductive barrier material **1006** is different in composition from the second conductive barrier material **1026**. In another embodiment, the first conductive barrier material **1006** and the second conductive barrier material **1026** have the same composition.

In an embodiment, a first conductive via **1019** is on and electrically coupled to an individual one **1004**A of the first plurality of conductive interconnect lines **1004**. An individual one **1014**A of the second plurality of conductive interconnect lines **1014** is on and electrically coupled to the first conductive via **1019**.

A second conductive via **1029** is on and electrically coupled to an individual one **1014**B of the second plurality of conductive interconnect lines **1014**. An individual one **1024**A of the third plurality of conductive interconnect lines **1024** is on and electrically coupled to the second conductive via **1029**.

A third conductive via **1039** is on and electrically coupled to an individual one **1024**B of the third plurality of conductive interconnect lines **1024**. An individual one **1034**A of the fourth plurality of conductive interconnect lines **1034** is on and electrically coupled to the third conductive via **1039**.

A fourth conductive via **1049** is on and electrically coupled to an individual one **1034**B of the fourth plurality of conductive interconnect lines **1034**. An individual one

1044A of the fifth plurality of conductive interconnect lines 1044 is on and electrically coupled to the fourth conductive via 1049.

A fifth conductive via 1059 is on and electrically coupled to an individual one 1044B of the fifth plurality of conductive interconnect lines 1044. An individual one 1054A of the sixth plurality of conductive interconnect lines 1054 is on and electrically coupled to the fifth conductive via 1059.

In one embodiment, the first conductive via 1019 includes the first conductive barrier material 1006 along sidewalls and a bottom of the first conductive fill material 1008. The second 1029, third 1039, fourth 1049 and fifth 1059 conductive vias include the second conductive barrier material 1026 along sidewalls and a bottom of the second conductive fill material 1028.

In an embodiment, the second 1012, third 1022, fourth 1032, fifth 1042 and sixth 1052 ILD layers are separated from one another by a corresponding etch-stop layer 1090 between adjacent ILD layers. In an embodiment, the first 1002, second 1012, third 1022, fourth 1032, fifth 1042 and sixth 1052 ILD layers include silicon, carbon and oxygen.

In an embodiment, individual ones of the first 1004 and second 1014 pluralities of conductive interconnect lines have a first width (W1). Individual ones of the third 1024, fourth 1034, fifth 1044 and sixth 1054 pluralities of conductive interconnect lines have a second width (W2) greater than the first width (W1).

In another aspect, techniques for patterning metal line ends are described. To provide context, in the advanced nodes of semiconductor manufacturing, lower level interconnects may be created by separate patterning processes of the line grating, line ends, and vias. However, the fidelity of the composite pattern may tend to degrade as the vias encroach upon the line ends and vice-versa. Embodiments described herein provide for a line end process also known as a plug process that eliminates associated proximity rules. Embodiments may allow for a via to be placed at the line end and a large via to strap across a line end.

To provide further context, FIG. 11A illustrates a plan view and corresponding cross-sectional view taken along the a-a' axis of the plan view of a metallization layer, in accordance with an embodiment of the present disclosure. FIG. 11B illustrates a cross-sectional view of a line end or plug, in accordance with an embodiment of the present disclosure. FIG. 11C illustrates another cross-sectional view of a line end or plug, in accordance with an embodiment of the present disclosure.

Referring to FIG. 11A, a metallization layer 1100 includes metal lines 1102 formed in a dielectric layer 1104. The metal lines 1102 may be coupled to underlying vias 1103. The dielectric layer 1104 may include line end or plug regions 1105. Referring to FIG. 11B, a line end or plug region 1105 of a dielectric layer 1104 may be fabricated by patterning a hardmask layer 1110 on the dielectric layer 1104 and then etching exposed portions of the dielectric layer 1104. The exposed portions of the dielectric layer 1104 may be etched to a depth suitable to form a line trench 1106 or further etched to a depth suitable to form a via trench 1108. Referring to FIG. 11C, two vias adjacent opposing sidewalls of the line end or plug 1105 may be fabricated in a single large exposure 1116 to ultimately form line trenches 1112 and via trenches 1114.

However, referring again to FIGS. 11A-11C, fidelity issues and/or hardmask erosion issues may lead to imperfect patterning regimes. By contrast, one or more embodiments described herein include implementation of a process flow involving construction of a line end dielectric (plug) after a trench and via patterning process.

In an aspect, then, one or more embodiments described herein are directed to approaches for building non-conductive spaces or interruptions between metals lines (referred to as "line ends," "plugs" or "cuts") and, in some embodiments, associated conductive vias. Conductive vias, by definition, are used to land on a previous layer metal pattern. In this vein, embodiments described herein enable a more robust interconnect fabrication scheme since alignment by lithography equipment is relied on to a lesser extent. Such an interconnect fabrication scheme can be used to relax constraints on alignment/exposures, can be used to improve electrical contact (e.g., by reducing via resistance), and can be used to reduce total process operations and processing time otherwise required for patterning such features using conventional approaches.

FIGS. 12A-12F illustrate plan views and corresponding cross-sectional views representing various operations in a plug last processing scheme, in accordance with an embodiment of the present disclosure.

Referring to FIG. 12A, a method of fabricating an integrated circuit structure includes forming a line trench 1206 in an upper portion 1204 of an interlayer dielectric (ILD) material layer 1202 formed above an underlying metallization layer 1200. A via trench 1208 is formed in a lower portion 1210 of the ILD material layer 1202. The via trench 1208 exposes a metal line 1212 of the underlying metallization layer 1200.

Referring to FIG. 12B, a sacrificial material 1214 is formed above the ILD material layer 1202 and in the line trench 1206 and the via trench 1208. The sacrificial material 1214 may have a hardmask 1215 formed thereon, as is depicted in FIG. 12B. In one embodiment, the sacrificial material 1214 includes carbon.

Referring to FIG. 12C, the sacrificial material 1214 is patterned to break a continuity of the sacrificial material 1214 in the line trench 1206, e.g., to provide an opening 1216 in the sacrificial material 1214.

Referring to FIG. 12D, the opening 1216 in the sacrificial material 1214 is filled with a dielectric material to form a dielectric plug 1218. In an embodiment, subsequent to filling the opening 1216 in the sacrificial material 1214 with the dielectric material, the hardmask 1215 is removed to provide the dielectric plug 1218 having an upper surface 1220 above an upper surface 1222 of the ILD material 1202, as is depicted in FIG. 12D. The sacrificial material 1214 is removed to leave the dielectric plug 1218 to remain.

In an embodiment, filling the opening 1216 of the sacrificial material 1214 with the dielectric material includes filling with a metal oxide material. In one such embodiment, the metal oxide material is aluminum oxide. In an embodiment, filling the opening 1216 of the sacrificial material 1214 with the dielectric material includes filling using atomic layer deposition (ALD).

Referring to FIG. 12E, the line trench 1206 and the via trench 1208 are filled with a conductive material 1224. In an embodiment, the conductive material 1224 is formed above and over the dielectric plug 1218 and the ILD layer 1202, as is depicted.

Referring to FIG. 12F, the conductive material 1224 and the dielectric plug 1218 are planarized to provide a planarized dielectric plug 1218' breaking a continuity of the conductive material 1224 in the line trench 1206.

Referring again to FIG. 12F, in an accordance with an embodiment of the present disclosure, an integrated circuit structure 1250 includes an inter-layer dielectric (ILD) layer

1202 above a substrate. A conductive interconnect line 1224 is in a trench 1206 in the ILD layer 1202. The conductive interconnect line 1224 has a first portion 1224A and a second portion 1224B, the first portion 1224A laterally adjacent to the second portion 1224B. A dielectric plug 1218' is between and laterally adjacent to the first 1224A and second 1224B portions of the conductive interconnect line 1224. Although not depicted, in an embodiment, the conductive interconnect line 1224 includes a conductive barrier liner and a conductive fill material, exemplary materials for which are described above. In one such embodiment, the conductive fill material includes cobalt.

In an embodiment, the dielectric plug 1218' includes a metal oxide material. In one such embodiment, the metal oxide material is aluminum oxide. In an embodiment, the dielectric plug 1218' is in direct contact with the first 1224A and second 1224B portions of the conductive interconnect line 1224.

In an embodiment, the dielectric plug 1218' has a bottom 1218A substantially co-planar with a bottom 1224C of the conductive interconnect line 1224. In an embodiment, a first conductive via 1226 is in a trench 1208 in the ILD layer 1202. In one such embodiment, the first conductive via 1226 is below the bottom 1224C of the interconnect line 1224, and the first conductive via 1226 is electrically coupled to the first portion 1224A of the conductive interconnect line 1224.

In an embodiment, a second conductive via 1228 is in a third trench 1230 in the ILD layer 1202. The second conductive via 1228 is below the bottom 1224C of the interconnect line 1224, and the second conductive via 1228 is electrically coupled to the second portion 1224B of the conductive interconnect line 1224.

A dielectric plug may be formed using a fill process such as a chemical vapor deposition process. Artifacts may remain in the fabricated dielectric plug. As an example, FIG. 13A illustrates a cross-sectional view of a conductive line plug having a seam therein, in accordance with an embodiment of the present disclosure.

Referring to FIG. 13A, a dielectric plug 1318 has an approximately vertical seam 1300 spaced approximately equally from the first portion 1224A of the conductive interconnect line 1224 and from the second portion 1224B of the conductive interconnect line 1224.

It is to be appreciated that dielectric plugs differing in composition from an ILD material in which they are housed may be included on only select metallization layers, such as in lower metallization layers. As an example, FIG. 13B illustrates a cross-sectional view of a stack of metallization layers including a conductive line plug at a lower metal line location, in accordance with an embodiment of the present disclosure.

Referring to FIG. 13B, an integrated circuit structure 1350 includes a first plurality of conductive interconnect lines 1356 in and spaced apart by a first inter-layer dielectric (ILD) layer 1354 above a substrate 1352. Individual ones of the first plurality of conductive interconnect lines 1356 have a continuity broken by one or more dielectric plugs 1358. In an embodiment, the one or more dielectric plugs 1358 include a material different than the ILD layer 1352. A second plurality of conductive interconnect lines 1366 is in and spaced apart by a second ILD layer 1364 above the first ILD layer 1354. In an embodiment, individual ones of the second plurality of conductive interconnect lines 1366 have a continuity broken by one or more portions 1368 of the second ILD layer 1364. It is to be appreciated, as depicted, that other metallization layers may be included in the integrated circuit structure 1350.

In one embodiment, the one or more dielectric plugs 1358 include a metal oxide material. In one such embodiment, the metal oxide material is aluminum oxide. In one embodiment, the first ILD layer 1354 and the second ILD layer 1364 (and, hence, the one or more portions 1368 of the second ILD layer 1364) include a carbon-doped silicon oxide material.

In one embodiment, individual ones of the first plurality of conductive interconnect lines 1356 include a first conductive barrier liner 1356A and a first conductive fill material 1356B. Individual ones of the second plurality of conductive interconnect lines 1366 include a second conductive barrier liner 1366A and a second conductive fill material 1366B. In one such embodiment, the first conductive fill material 1356B is different in composition from the second conductive fill material 1366B. In a particular such embodiment, the first conductive fill material 1356B includes cobalt, and the second conductive fill material 1366B includes copper.

In one embodiment, the first plurality of conductive interconnect lines 1356 has a first pitch (P1, as shown in like-layer 1370). The second plurality of conductive interconnect lines 1366 has a second pitch (P2, as shown in like-layer 1380). The second pitch (P2) is greater than the first pitch (P1). In one embodiment, individual ones of the first plurality of conductive interconnect lines 1356 have a first width (W1, as shown in like-layer 1370). Individual ones of the second plurality of conductive interconnect lines 1366 have a second width (W2, as shown in like-layer 1380). The second width (W2) is greater than the first width (W1).

It is to be appreciated that the layers and materials described above in association with back end of line (BEOL) structures and processing may be formed on or above an underlying semiconductor substrate or structure, such as underlying device layer(s) of an integrated circuit. In an embodiment, an underlying semiconductor substrate represents a general workpiece object used to manufacture integrated circuits. The semiconductor substrate often includes a wafer or other piece of silicon or another semiconductor material. Suitable semiconductor substrates include, but are not limited to, single crystal silicon, polycrystalline silicon and silicon on insulator (SOI), as well as similar substrates formed of other semiconductor materials, such as substrates including germanium, carbon, or group materials. The semiconductor substrate, depending on the stage of manufacture, often includes transistors, integrated circuitry, and the like. The substrate may also include semiconductor materials, metals, dielectrics, dopants, and other materials commonly found in semiconductor substrates. Furthermore, the structures depicted may be fabricated on underlying lower level interconnect layers.

Although the preceding methods of fabricating a metallization layer, or portions of a metallization layer, of a BEOL metallization layer are described in detail with respect to select operations, it is to be appreciated that additional or intermediate operations for fabrication may include standard microelectronic fabrication processes such as lithography, etch, thin films deposition, planarization (such as chemical mechanical polishing (CMP)), diffusion, metrology, the use of sacrificial layers, the use of etch stop layers, the use of planarization stop layers, or any other associated action with microelectronic component fabrication. Also, it is to be appreciated that the process operations described for the preceding process flows may be practiced in alternative

sequences, not every operation need be performed or additional process operations may be performed or both.

In an embodiment, as used throughout the present description, interlayer dielectric (ILD) material is composed of or includes a layer of a dielectric or insulating material. Examples of suitable dielectric materials include, but are not limited to, oxides of silicon (e.g., silicon dioxide (SiO_2)), doped oxides of silicon, fluorinated oxides of silicon, carbon doped oxides of silicon, various low-k dielectric materials known in the arts, and combinations thereof. The interlayer dielectric material may be formed by techniques, such as, for example, chemical vapor deposition (CVD), physical vapor deposition (PVD), or by other deposition methods.

In an embodiment, as is also used throughout the present description, metal lines or interconnect line material (and via material) is composed of one or more metal or other conductive structures. A common example is the use of copper lines and structures that may or may not include barrier layers between the copper and surrounding ILD material. As used herein, the term metal includes alloys, stacks, and other combinations of multiple metals. For example, the metal interconnect lines may include barrier layers (e.g., layers including one or more of Ta, TaN, Ti or TiN), stacks of different metals or alloys, etc. Thus, the interconnect lines may be a single material layer, or may be formed from several layers, including conductive liner layers and fill layers. Any suitable deposition process, such as electroplating, chemical vapor deposition or physical vapor deposition, may be used to form interconnect lines. In an embodiment, the interconnect lines are composed of a conductive material such as, but not limited to, Cu, Al, Ti, Zr, Hf, V, Ru, Co, Ni, Pd, Pt, W, Ag, Au or alloys thereof. The interconnect lines are also sometimes referred to in the art as traces, wires, lines, metal, or simply interconnect.

In an embodiment, as is also used throughout the present description, hardmask materials are composed of dielectric materials different from the interlayer dielectric material. In one embodiment, different hardmask materials may be used in different regions so as to provide different growth or etch selectivity to each other and to the underlying dielectric and metal layers. In some embodiments, a hardmask layer includes a layer of a nitride of silicon (e.g., silicon nitride) or a layer of an oxide of silicon, or both, or a combination thereof. Other suitable materials may include carbon-based materials. In another embodiment, a hardmask material includes a metal species. For example, a hardmask or other overlying material may include a layer of a nitride of titanium or another metal (e.g., titanium nitride). Potentially lesser amounts of other materials, such as oxygen, may be included in one or more of these layers. Alternatively, other hardmask layers known in the arts may be used depending upon the particular implementation. The hardmask layers maybe formed by CVD, PVD, or by other deposition methods.

In an embodiment, as is also used throughout the present description, lithographic operations are performed using 193 nm immersion lithography (i193), extreme ultra-violet (EUV) lithography or electron beam direct write (EBDW) lithography, or the like. A positive tone or a negative tone resist may be used. In one embodiment, a lithographic mask is a trilayer mask composed of a topographic masking portion, an anti-reflective coating (ARC) layer, and a photoresist layer. In a particular such embodiment, the topographic masking portion is a carbon hardmask (CHM) layer and the anti-reflective coating layer is a silicon ARC layer.

Embodiments disclosed herein may be used to manufacture a wide variety of different types of integrated circuits or microelectronic devices. Examples of such integrated circuits include, but are not limited to, processors, chipset components, graphics processors, digital signal processors, micro-controllers, and the like. In other embodiments, semiconductor memory may be manufactured. Moreover, the integrated circuits or other microelectronic devices may be used in a wide variety of electronic devices known in the arts. For example, in computer systems (e.g., desktop, laptop, server), cellular phones, personal electronics, etc. The integrated circuits may be coupled with a bus and other components in the systems. For example, a processor may be coupled by one or more buses to a memory, a chipset, etc. Each of the processor, the memory, and the chipset, may potentially be manufactured using the approaches disclosed herein.

FIG. **14** illustrates a computing device **1400** in accordance with one implementation of the disclosure. The computing device **1400** houses a board **1402**. The board **1402** may include a number of components, including but not limited to a processor **1404** and at least one communication chip **1406**. The processor **1404** is physically and electrically coupled to the board **1402**. In some implementations the at least one communication chip **1406** is also physically and electrically coupled to the board **1402**. In further implementations, the communication chip **1406** is part of the processor **1404**.

Depending on its applications, computing device **1400** may include other components that may or may not be physically and electrically coupled to the board **1402**. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communication chip **1406** enables wireless communications for the transfer of data to and from the computing device **1400**. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip **1406** may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device **1400** may include a plurality of communication chips **1406**. For instance, a first communication chip **1406** may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip **1406** may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor **1404** of the computing device **1400** includes an integrated circuit die packaged within the processor **1404**. In some implementations of embodiments of the disclosure, the integrated circuit die of the processor includes one or more structures, such as integrated circuit

structures built in accordance with implementations of the disclosure. The term "processor" may refer to any device or portion of a device that processes electronic data from registers or memory to transform that electronic data, or both, into other electronic data that may be stored in registers or memory, or both.

The communication chip **1406** also includes an integrated circuit die packaged within the communication chip **1406**. In accordance with another implementation of the disclosure, the integrated circuit die of the communication chip is built in accordance with implementations of the disclosure.

In further implementations, another component housed within the computing device **1400** may contain an integrated circuit die built in accordance with implementations of embodiments of the disclosure.

In various embodiments, the computing device **1400** may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultramobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device **1400** may be any other electronic device that processes data.

FIG. **15** illustrates an interposer **1500** that includes one or more embodiments of the disclosure. The interposer **1500** is an intervening substrate used to bridge a first substrate **1502** to a second substrate **1504**. The first substrate **1502** may be, for instance, an integrated circuit die. The second substrate **1504** may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer **1500** is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer **1500** may couple an integrated circuit die to a ball grid array (BGA) **1506** that can subsequently be coupled to the second substrate **1504**. In some embodiments, the first and second substrates **1502**/**1504** are attached to opposing sides of the interposer **1500**. In other embodiments, the first and second substrates **1502**/**1504** are attached to the same side of the interposer **1500**. And in further embodiments, three or more substrates are interconnected by way of the interposer **1500**.

The interposer **1500** may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer **1500** may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

The interposer **1500** may include metal interconnects **1508** and vias **1510**, including but not limited to through-silicon vias (TSVs) **1512**. The interposer **1500** may further include embedded devices **1514**, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer **1500**. In accordance with embodiments of the disclosure, apparatuses or processes disclosed herein may be used in the fabrication of interposer **1500** or in the fabrication of components included in the interposer **1500**.

FIG. **16** is an isometric view of a mobile computing platform **1600** employing an integrated circuit (IC) fabricated according to one or more processes described herein or including one or more features described herein, in accordance with an embodiment of the present disclosure.

The mobile computing platform **1600** may be any portable device configured for each of electronic data display, electronic data processing, and wireless electronic data transmission. For example, mobile computing platform **1600** may be any of a tablet, a smart phone, laptop computer, etc. and includes a display screen **1605** which in the exemplary embodiment is a touchscreen (capacitive, inductive, resistive, etc.), a chip-level (SoC) or package-level integrated system **1610**, and a battery **1613**. As illustrated, the greater the level of integration in the system **1610** enabled by higher transistor packing density, the greater the portion of the mobile computing platform **1600** that may be occupied by the battery **1613** or non-volatile storage, such as a solid state drive, or the greater the transistor gate count for improved platform functionality. Similarly, the greater the carrier mobility of each transistor in the system **1610**, the greater the functionality. As such, techniques described herein may enable performance and form factor improvements in the mobile computing platform **1600**.

The integrated system **1610** is further illustrated in the expanded view **1620**. In the exemplary embodiment, packaged device **1677** includes at least one memory chip (e.g., RAM), or at least one processor chip (e.g., a multi-core microprocessor and/or graphics processor) fabricated according to one or more processes described herein or including one or more features described herein. The packaged device **1677** is further coupled to the board **1660** along with one or more of a power management integrated circuit (PMIC) **1615**, RF (wireless) integrated circuit (RFIC) **1625** including a wideband RF (wireless) transmitter and/or receiver (e.g., including a digital baseband and an analog front end module further includes a power amplifier on a transmit path and a low noise amplifier on a receive path), and a controller thereof **1611**. Functionally, the PMIC **1615** performs battery power regulation, DC-to-DC conversion, etc., and so has an input coupled to the battery **1613** and with an output providing a current supply to all the other functional modules. As further illustrated, in the exemplary embodiment, the RFIC **1625** has an output coupled to an antenna to provide to implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. In alternative implementations, each of these board-level modules may be integrated onto separate ICs coupled to the package substrate of the packaged device **1677** or within a single IC (SoC) coupled to the package substrate of the packaged device **1677**.

In another aspect, semiconductor packages are used for protecting an integrated circuit (IC) chip or die, and also to provide the die with an electrical interface to external circuitry. With the increasing demand for smaller electronic devices, semiconductor packages are designed to be even more compact and must support larger circuit density. Furthermore, the demand for higher performance devices results in a need for an improved semiconductor package that enables a thin packaging profile and low overall warpage compatible with subsequent assembly processing.

In an embodiment, wire bonding to a ceramic or organic package substrate is used. In another embodiment, a C4 process is used to mount a die to a ceramic or organic

package substrate. In particular, C4 solder ball connections can be implemented to provide flip chip interconnections between semiconductor devices and substrates. A flip chip or Controlled Collapse Chip Connection (C4) is a type of mounting used for semiconductor devices, such as integrated circuit (IC) chips, MEMS or components, which utilizes solder bumps instead of wire bonds. The solder bumps are deposited on the C4 pads, located on the top side of the substrate package. In order to mount the semiconductor device to the substrate, it is flipped over with the active side facing down on the mounting area. The solder bumps are used to connect the semiconductor device directly to the substrate.

FIG. **17** illustrates a cross-sectional view of a flip-chip mounted die, in accordance with an embodiment of the present disclosure.

Referring to FIG. **17**, an apparatus **1700** includes a die **1702** such as an integrated circuit (IC) fabricated according to one or more processes described herein or including one or more features described herein, in accordance with an embodiment of the present disclosure. The die **1702** includes metallized pads **1704** thereon. A package substrate **1706**, such as a ceramic or organic substrate, includes connections **1708** thereon. The die **1702** and package substrate **1706** are electrically connected by solder balls **1710** coupled to the metallized pads **1704** and the connections **1708**. An underfill material **1712** surrounds the solder balls **1710**.

Processing a flip chip may be similar to conventional IC fabrication, with a few additional operations. Near the end of the manufacturing process, the attachment pads are metallized to make them more receptive to solder. This typically consists of several treatments. A small dot of solder is then deposited on each metalized pad. The chips are then cut out of the wafer as normal. To attach the flip chip into a circuit, the chip is inverted to bring the solder dots down onto connectors on the underlying electronics or circuit board. The solder is then re-melted to produce an electrical connection, typically using an ultrasonic or alternatively reflow solder process. This also leaves a small space between the chip's circuitry and the underlying mounting. In most cases an electrically-insulating adhesive is then "underfilled" to provide a stronger mechanical connection, provide a heat bridge, and to ensure the solder joints are not stressed due to differential heating of the chip and the rest of the system.

In other embodiments, newer packaging and die-to-die interconnect approaches, such as through silicon via (TSV) and silicon interposer, are implemented to fabricate high performance Multi-Chip Module (MCM) and System in Package (SiP) incorporating an integrated circuit (IC) fabricated according to one or more processes described herein or including one or more features described herein, in accordance with an embodiment of the present disclosure.

Thus, embodiments of the present disclosure include advanced integrated circuit structure fabrication.

Although specific embodiments have been described above, these embodiments are not intended to limit the scope of the present disclosure, even where only a single embodiment is described with respect to a particular feature. Examples of features provided in the disclosure are intended to be illustrative rather than restrictive unless stated otherwise. The above description is intended to cover such alternatives, modifications, and equivalents as would be apparent to a person skilled in the art having the benefit of the present disclosure.

The scope of the present disclosure includes any feature or combination of features disclosed herein (either explicitly or implicitly), or any generalization thereof, whether or not it mitigates any or all of the problems addressed herein. Accordingly, new claims may be formulated during prosecution of the present application (or an application claiming priority thereto) to any such combination of features. In particular, with reference to the appended claims, features from dependent claims may be combined with those of the independent claims and features from respective independent claims may be combined in any appropriate manner and not merely in the specific combinations enumerated in the appended claims.

The following examples pertain to further embodiments. The various features of the different embodiments may be variously combined with some features included and others excluded to suit a variety of different applications.

Example embodiment 1: An integrated circuit structure includes a single dielectric layer above a substrate. A plurality of conductive lines is in an upper portion of the single dielectric layer above a lower portion of the single dielectric layer. A carbon dopant region is in the upper portion of the single dielectric layer, the carbon dopant region between adjacent ones of the plurality of conductive lines.

Example embodiment 2: The integrated circuit structure of example embodiment 1, wherein the single dielectric layer is composed of a carbon-doped silicon oxide (CDO) material.

Example embodiment 3: The integrated circuit structure of example embodiment 2, wherein the CDO material has a greater carbon concentration in the lower portion of the single dielectric layer than in the upper portion of the single dielectric layer.

Example embodiment 4: The integrated circuit structure of example embodiment 3, wherein a total carbon concentration of the CDO material in the upper portion of the single dielectric layer combined with the carbon dopant region is about the same as the carbon concentration in the lower portion of the single dielectric layer.

Example embodiment 5: The integrated circuit structure of example embodiment 1, 2, 3 or 4, wherein the carbon dopant region has a depth in the single dielectric layer approximately the same as a depth of the plurality of conductive lines.

Example embodiment 6: The integrated circuit structure of example embodiment 1, 2, 3 or 4, wherein the carbon dopant region has a depth in the single dielectric layer less than a depth of the plurality of conductive lines.

Example embodiment 7: The integrated circuit structure of example embodiment 1, 2, 3 or 4, wherein the carbon dopant region has a depth in the single dielectric layer greater than a depth of the plurality of conductive lines.

Example embodiment 8: The integrated circuit structure of example embodiment 1, 2, 3, 4, 5, 6 or 7, wherein the carbon dopant region has a depth in the single dielectric layer in a range of 10-20 nanometers.

Example embodiment 9: The integrated circuit structure of example embodiment 1, 2, 3, 4, 5, 6, 7 or 8, wherein the plurality of conductive lines is a plurality of cobalt-based lines.

Example embodiment 10: The integrated circuit structure of example embodiment 1, 2, 3, 4, 5, 6, 7, 8 or 9, further including a copper-based via on one of the plurality of conductive lines.

Example embodiment 11: A method of fabricating an integrated circuit structure includes forming a first conductive interconnect line and a second conductive interconnect line in an inter-layer dielectric (ILD) layer above a substrate, implanting carbon into the ILD layer, and annealing the ILD layer.

Example embodiment 12: The method of example embodiment 11, wherein the implanting carbon into the ILD layer includes implanting using a direct beam technique.

Example embodiment 13: The method of example embodiment 11 or 12, wherein the implanting carbon into the ILD layer and annealing the ILD layer reduces a line-to-line capacitance between the first and the second conductive interconnect lines.

Example embodiment 14: The method of example embodiment 11, 12 or 13, wherein the implanting carbon into the ILD layer and annealing the ILD layer reduces a moisture content of the ILD layer.

Example embodiment 15: The method of example embodiment 11, 12, 13 or 14, wherein the implanting carbon into the ILD layer forms a carbon dopant region having a depth in the ILD layer approximately the same as a depth of the first and second conductive interconnect lines.

Example embodiment 16: A computing device includes a board, and a component coupled to the board. The component includes an integrated circuit structure including a single dielectric layer above a substrate. A plurality of conductive lines is in an upper portion of the single dielectric layer above a lower portion of the single dielectric layer. A carbon dopant region is in the upper portion of the single dielectric layer, the carbon dopant region between adjacent ones of the plurality of conductive lines.

Example embodiment 17: The computing device of example embodiment 16, further including a memory coupled to the board.

Example embodiment 18: The computing device of example embodiment 16 or 17, further including a communication chip coupled to the board.

Example embodiment 19: The computing device of example embodiment 16, 17 or 18, further including a camera coupled to the board.

Example embodiment 20: The computing device of example embodiment 16, 17, 18 or 19, wherein the component is a packaged integrated circuit die.

What is claimed is:

1. An integrated circuit structure, comprising:

a single dielectric layer above a substrate, wherein the single dielectric layer is structurally continuous from a bottommost surface of the single dielectric layer to an uppermost surface of the single dielectric layer;

a plurality of conductive lines in an upper portion of the single dielectric layer above a lower portion of the single dielectric layer; and

a carbon dopant region in the upper portion of the single dielectric layer, the carbon dopant region between adjacent ones of the plurality of conductive lines, and the carbon dopant region having an uppermost surface at a same level as an uppermost surface of the plurality of conductive lines.

2. The integrated circuit structure of claim **1**, wherein the single dielectric layer comprises a carbon-doped silicon oxide (CDO) material.

3. The integrated circuit structure of claim **2**, wherein the CDO material has a greater carbon concentration in the lower portion of the single dielectric layer than in the upper portion of the single dielectric layer.

4. The integrated circuit structure of claim **3**, wherein a total carbon concentration of the CDO material in the upper portion of the single dielectric layer combined with the carbon dopant region is about the same as the carbon concentration in the lower portion of the single dielectric layer.

5. The integrated circuit structure of claim **1**, wherein the carbon dopant region has a depth in the single dielectric layer approximately the same as a depth of the plurality of conductive lines.

6. The integrated circuit structure of claim **1**, wherein the carbon dopant region has a depth in the single dielectric layer less than a depth of the plurality of conductive lines.

7. The integrated circuit structure of claim **1**, wherein the carbon dopant region has a depth in the single dielectric layer greater than a depth of the plurality of conductive lines.

8. The integrated circuit structure of claim **1**, wherein the carbon dopant region has a depth in the single dielectric layer in a range of 10-20 nanometers.

9. The integrated circuit structure of claim **1**, wherein the plurality of conductive lines is a plurality of cobalt-based lines.

10. The integrated circuit structure of claim **9**, further comprising:

a copper-based via on one of the plurality of conductive lines.

11. A method of fabricating an integrated circuit structure, the method comprising:

forming a first conductive interconnect line and a second conductive interconnect line in an inter-layer dielectric (ILD) layer above a substrate;

implanting carbon into the ILD layer; and

annealing the ILD layer to form a carbon dopant region between the first conductive interconnect line and the second conductive interconnect line, the carbon dopant region having an uppermost surface at a same level as an uppermost surface of the first conductive interconnect line and the second conductive interconnect line, wherein the ILD layer is structurally continuous from a bottommost surface of the ILD layer to an uppermost surface of the ILD layer.

12. The method of claim **11**, wherein the implanting carbon into the ILD layer comprises implanting using a direct beam technique.

13. The method of claim **11**, wherein the implanting carbon into the ILD layer and annealing the ILD layer reduces a line-to-line capacitance between the first and the second conductive interconnect lines.

14. The method of claim **11**, wherein the implanting carbon into the ILD layer and annealing the ILD layer reduces a moisture content of the ILD layer.

15. The method of claim **11**, wherein the implanting carbon into the ILD layer forms a carbon dopant region having a depth in the ILD layer approximately the same as a depth of the first and second conductive interconnect lines.

16. A computing device, comprising:

a board; and

a component coupled to the board, the component including an integrated circuit structure, comprising:

a single dielectric layer above a substrate, wherein the single dielectric layer is structurally continuous from a bottommost surface of the single dielectric layer to an uppermost surface of the single dielectric layer;

a plurality of conductive lines in an upper portion of the single dielectric layer above a lower portion of the single dielectric layer; and

a carbon dopant region in the upper portion of the single dielectric layer, the carbon dopant region between adjacent ones of the plurality of conductive lines, and the carbon dopant region having an uppermost surface at a same level as an uppermost surface of the plurality of conductive lines.

17. The computing device of claim 16, further comprising:

a memory chip coupled to the board.

18. The computing device of claim 16, further comprising:

a communication chip coupled to the board.

19. The computing device of claim 16, further comprising:

a camera coupled to the board.

20. The computing device of claim 16, wherein the component is a packaged integrated circuit die.

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