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(54) **SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE**

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(57) **ABSTRACT**

A semiconductor device may include a peripheral circuit comprising a plurality of transistors, a cell array and a contact array positioned adjacent to each other over the peripheral circuit, a bonding pad for electrically connecting the peripheral circuit with the cell array and the contact array, the bonding pad comprising first and second portions, wherein the first portion has a first width and is in electrical connection with at least one transistor of the peripheral circuit, wherein the second portion has a second width that is less than the first width of the first portion, and wherein a bonding via electrically connecting the bonding pad with the contact array or the cell array extends partially inside the first portion of the bonding pad.

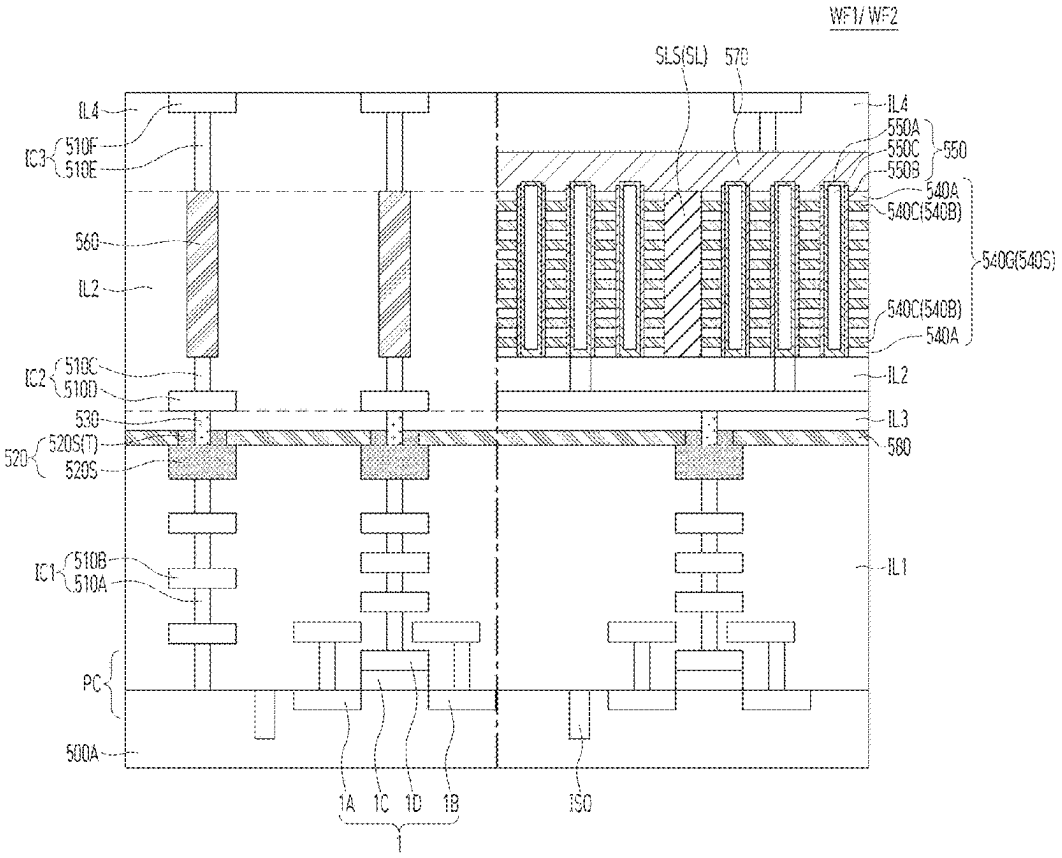
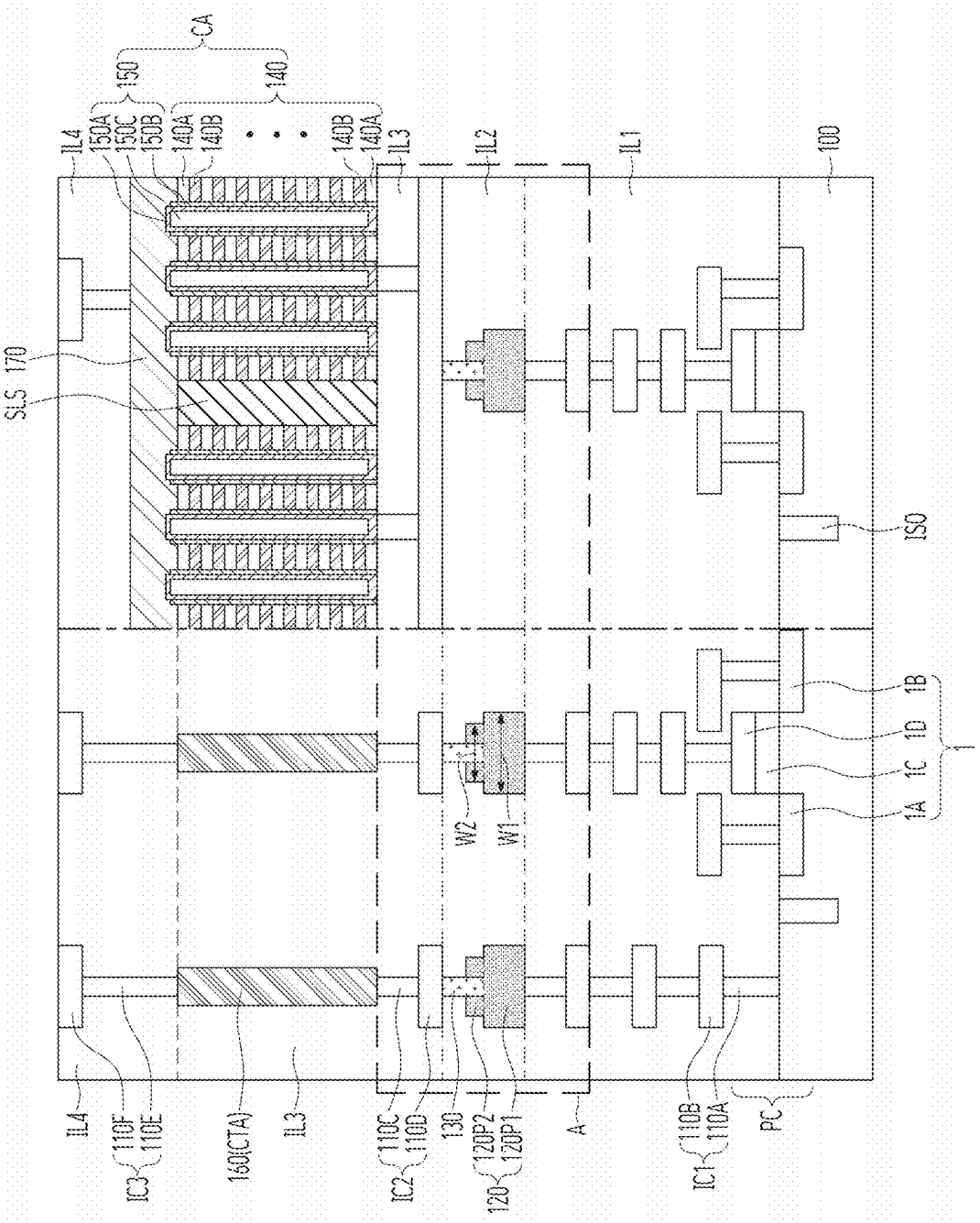


FIG. 1


CA
150
140
IL4
150A
150C
150B
140A
140B
140B
140A
IL3
IL2
IL1
100
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170
ISO
1B
1D
1C
1A
1
W2
W1
IL4
IC3
110F
110E
160(CTA)
IL3
IC2
110C
110D
130
120P2
120P1
120
A
IC1
110B
110A
PC

FIG. 2A

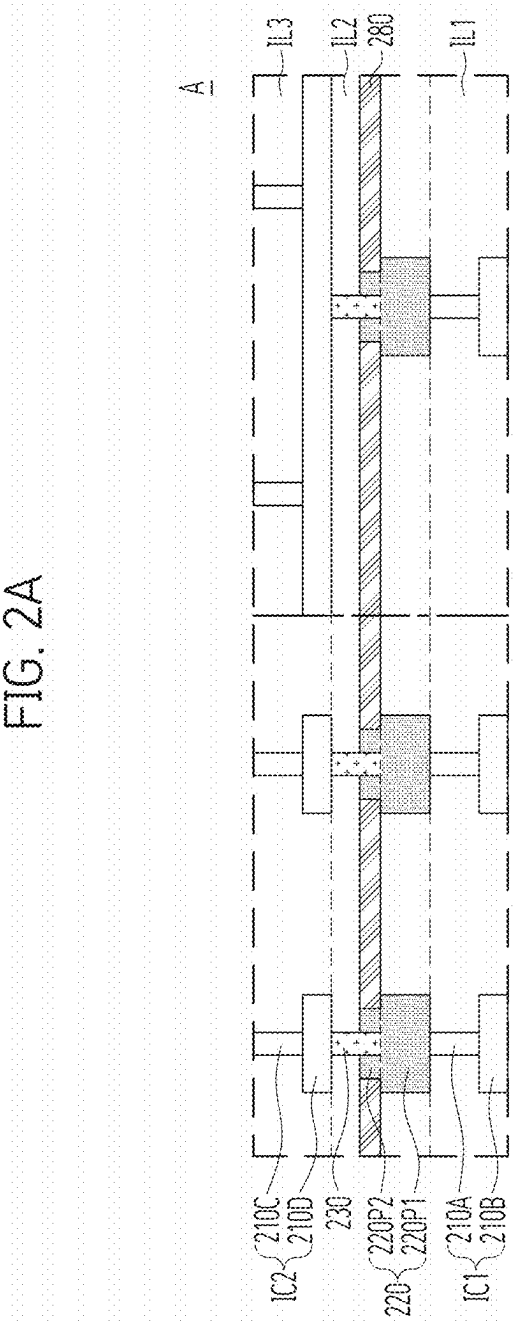

A
IL3
IL2
280
IL1
210C
210D
230
220P2
220P1
210A
210B
IC2
220
IC1

FIG. 2B

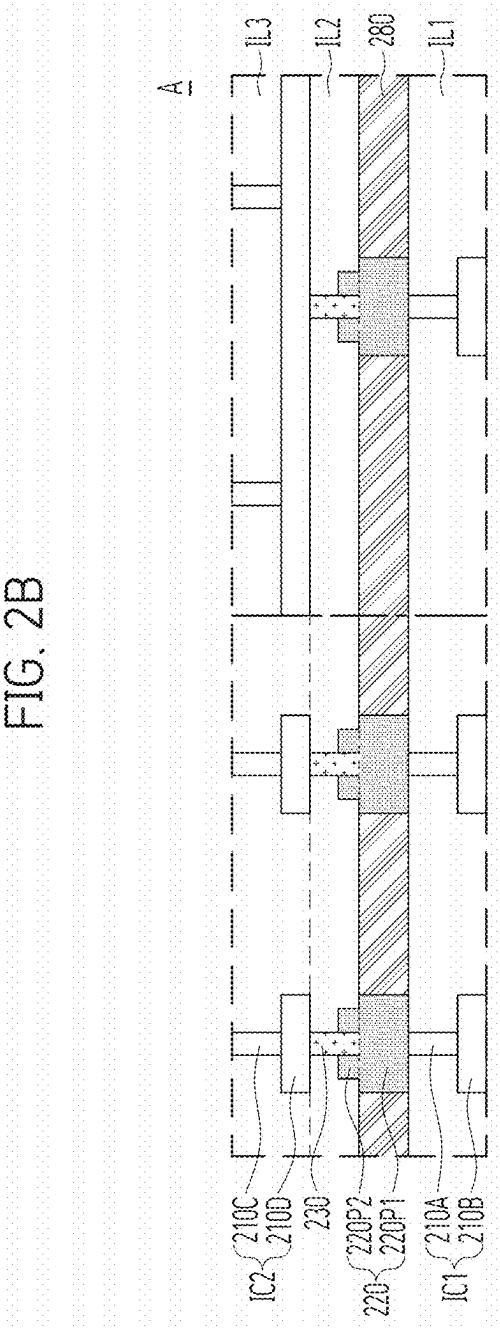

A
IL3
IL2
280
IL1
210C
210D
230
220P2
220P1
210A
210B
IC2
220
IC1

FIG. 3

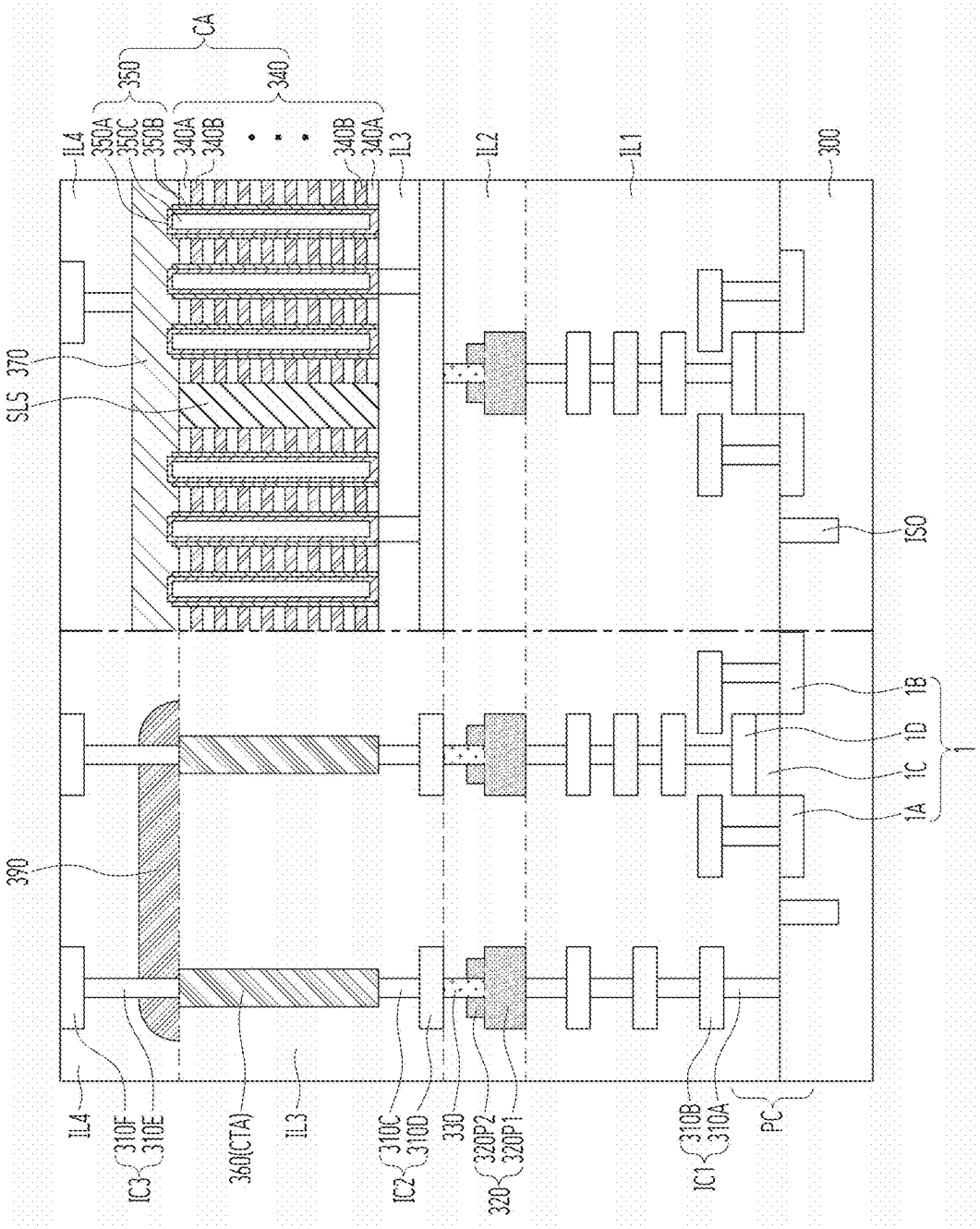

CA
350
340
IL4
350A
350C
350B
340A
340B
340B
340A
IL3
IL2
IL1
300
SLS
370
ISO
1B
1D
1C
1A
1
390
IL4
310F
310E
IC3
360(CTA)
IL3
310C
310D
IC2
330
320P2
320P1
320
310B
310A
IC1
PC

FIG. 4A

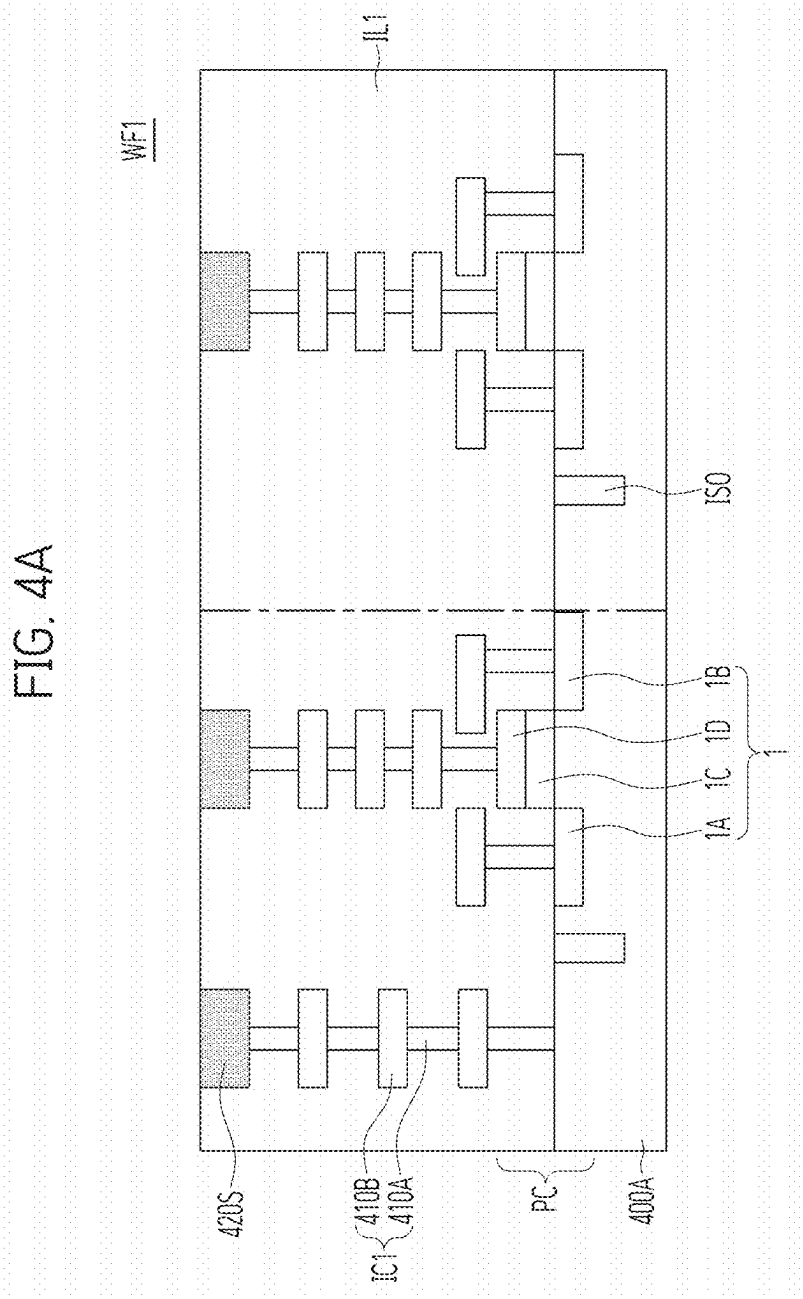


FIG. 4B

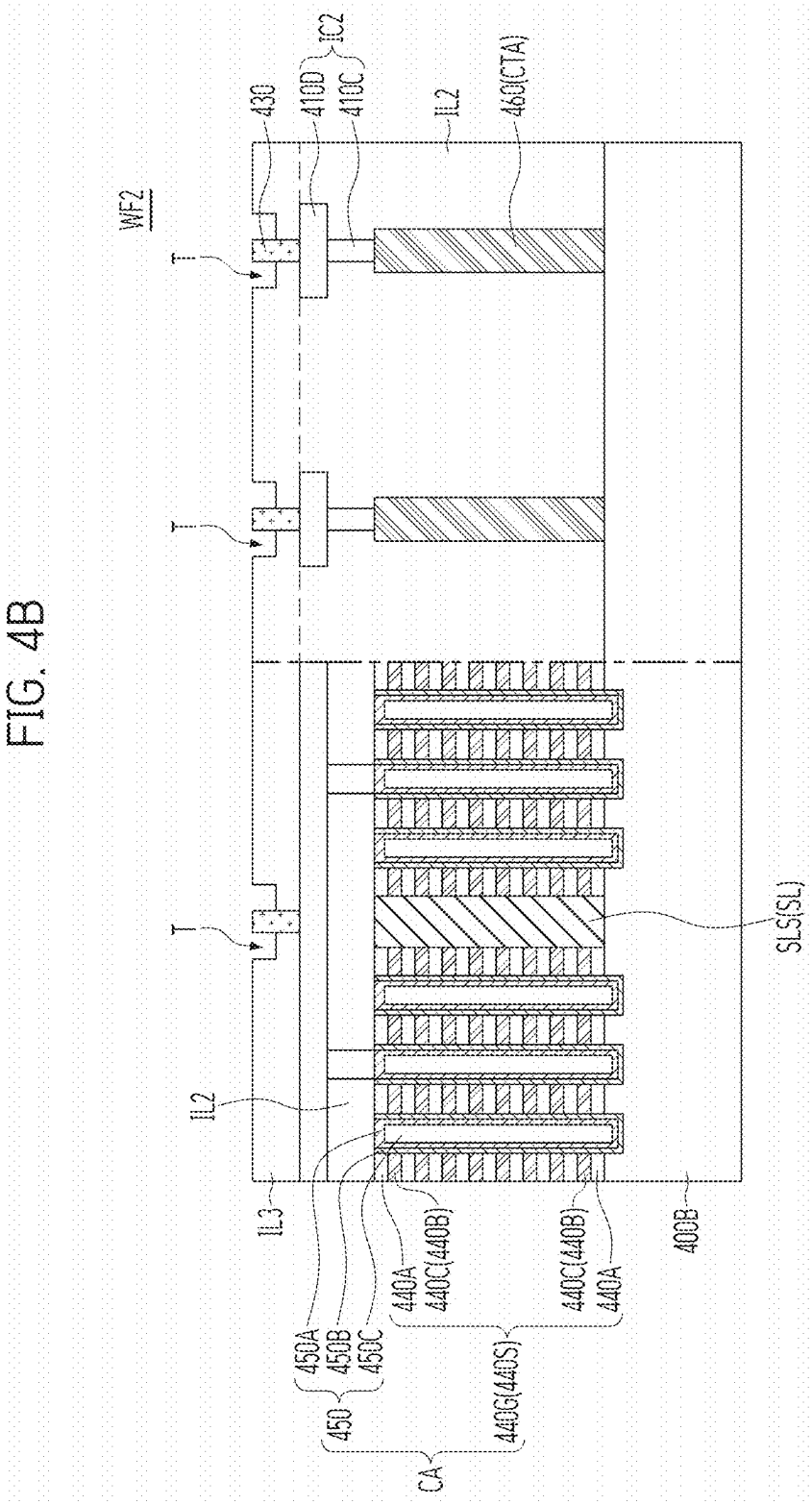

WF2
T
T
T
430
410D
410C
IC2
IL2
460(CTA)
SLS(SL)
IL2
IL3
450A
450B
450C
450
440A
440C(440B)
440G(440S)
440C(440B)
440A
CA
400B

FIG. 5

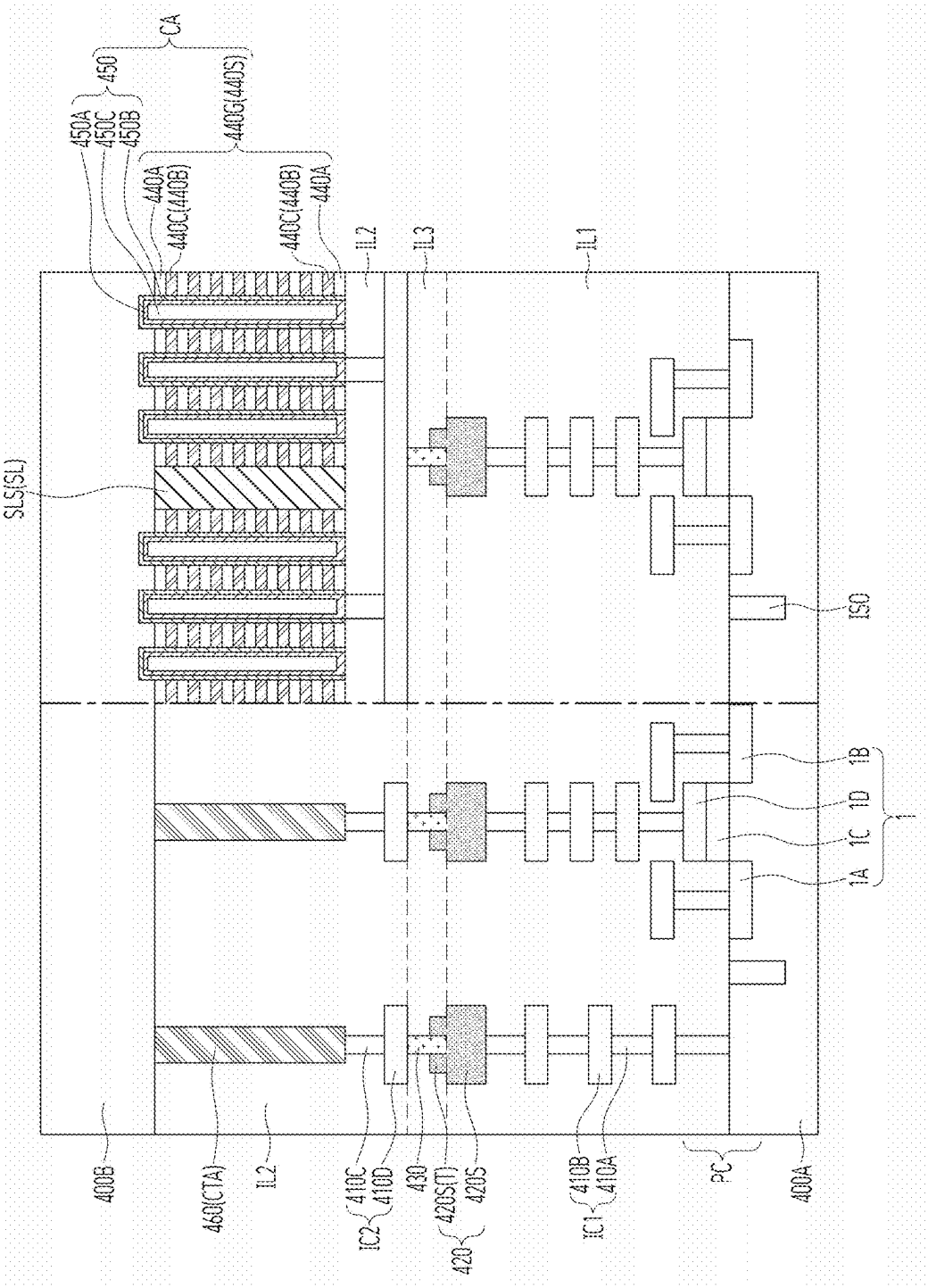

WF1/WF2
CA
450
450A
450C
450B
440G(440S)
440A
440C(440B)
440C(440B)
440A
IL2
IL3
IL1
SLS(SL)
ISO
1B
1D
1C
1A
1
400B
460(CTA)
IL2
410C
410D
IC2
430
420ST)
420S
420
410B
410A
IC1
PC
400A

FIG. 6

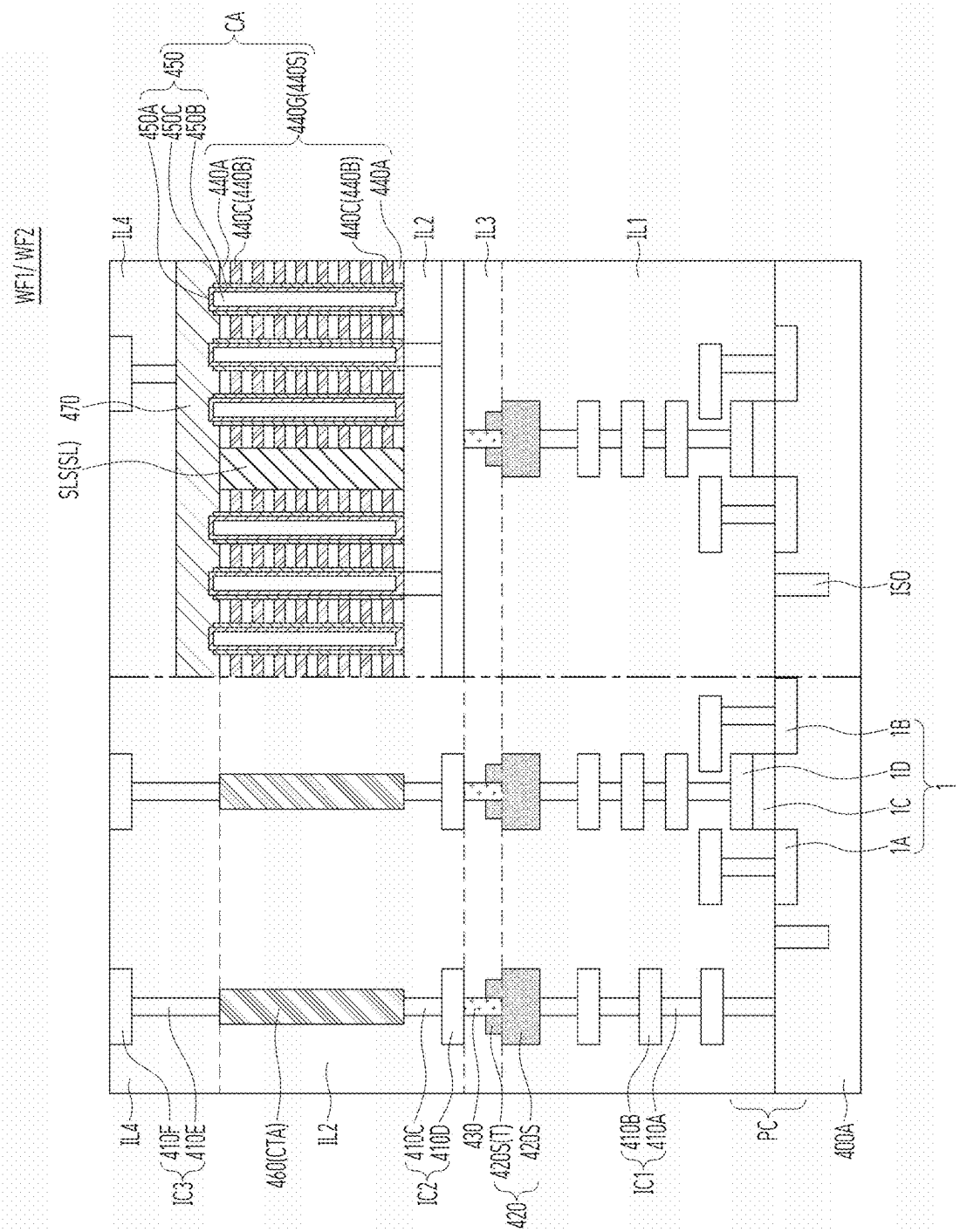

WF1/WF2
CA
450
450A
450C
450B
440G(440S)
440A
440C(440B)
440C(440B)
440A
IL4
IL2
IL3
IL1
470
SLS(SL)
ISO
1B
1D
1C
1A
IL4
410F
410E
IC3
460(CTA)
IL2
410C
410D
IC2
430
420S(T)
420S
420
410B
410A
IC1
PC
400A

FIG. 7

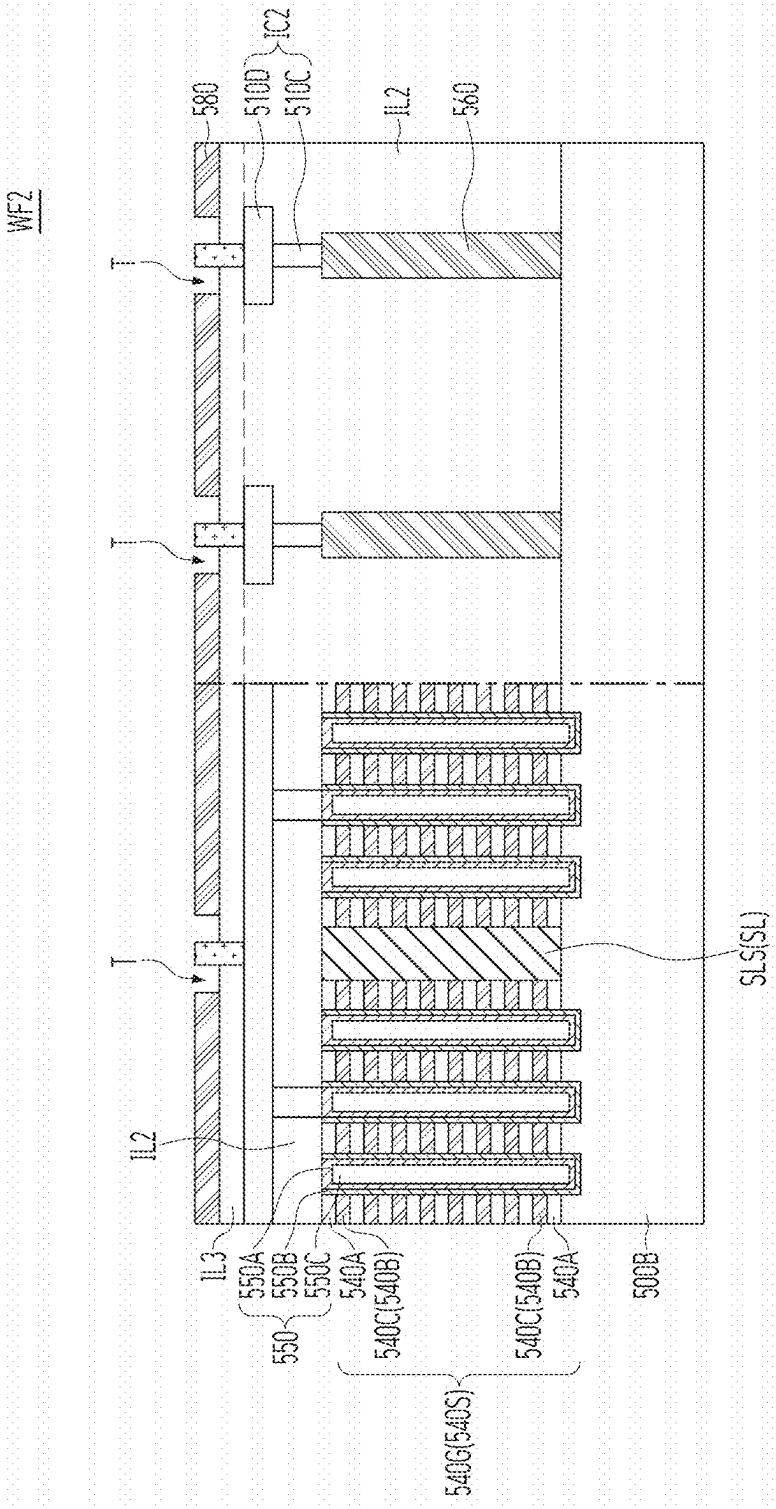

WF2
580
510D
510C
IC2
IL2
560
T
T
T
SLS(SL)
IL2
IL3
550A
550B
550C
550
540A
540C(540B)
540C(540B)
540A
500B
540G(540S)

FIG. 8

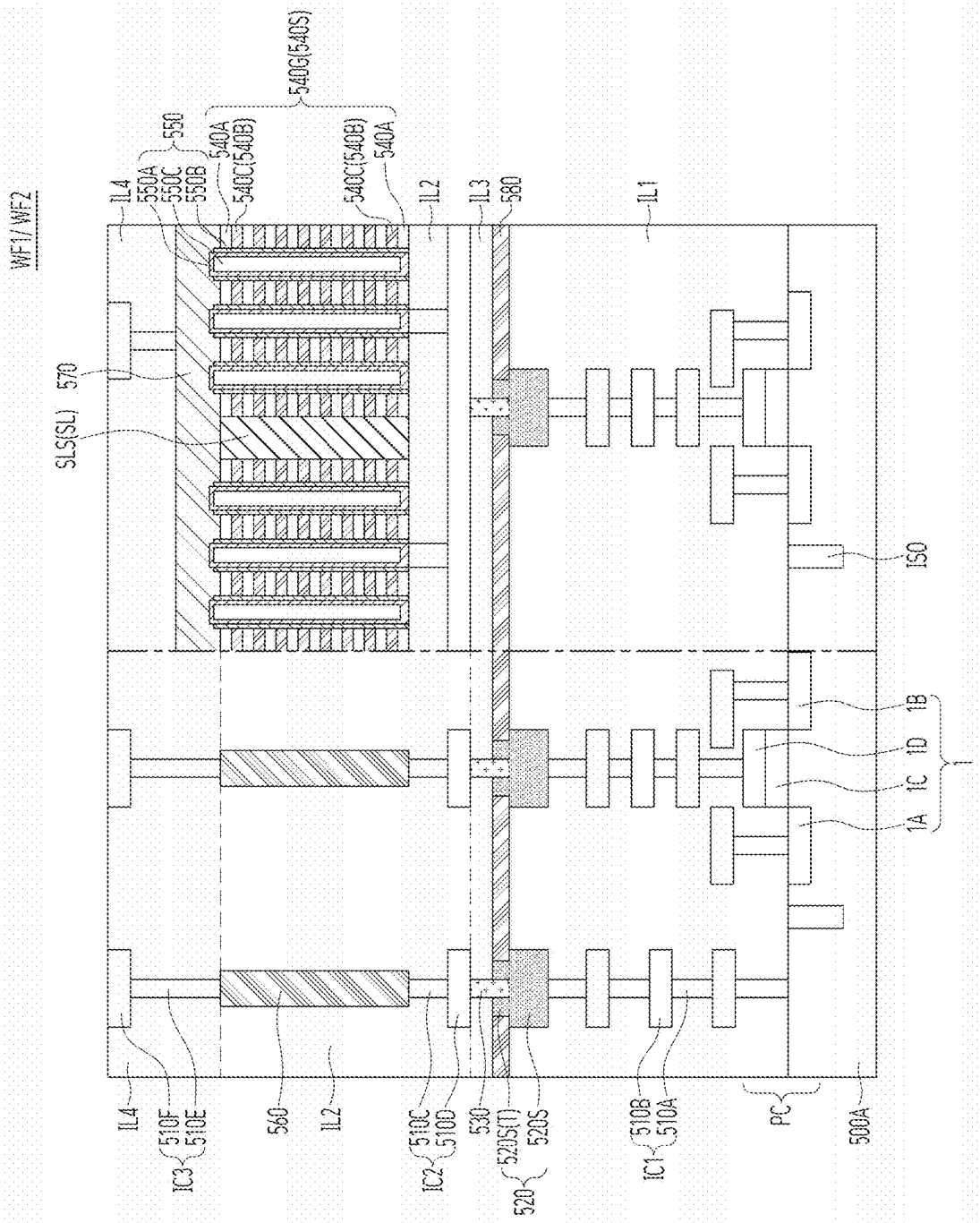

WF1/WF2
540G(540S)
550
540A
540C(540B)
540C(540B)
540A
IL4
550A
550C
550B
IL2
IL3
580
IL1
570
SLS(SL)
ISO
1B
1D
1C
1A
IL4
510F
510E
IC3
560
IL2
510C
510D
IC2
530
520S(T)
520S
520
510B
510A
IC1
PC
500A

FIG. 9

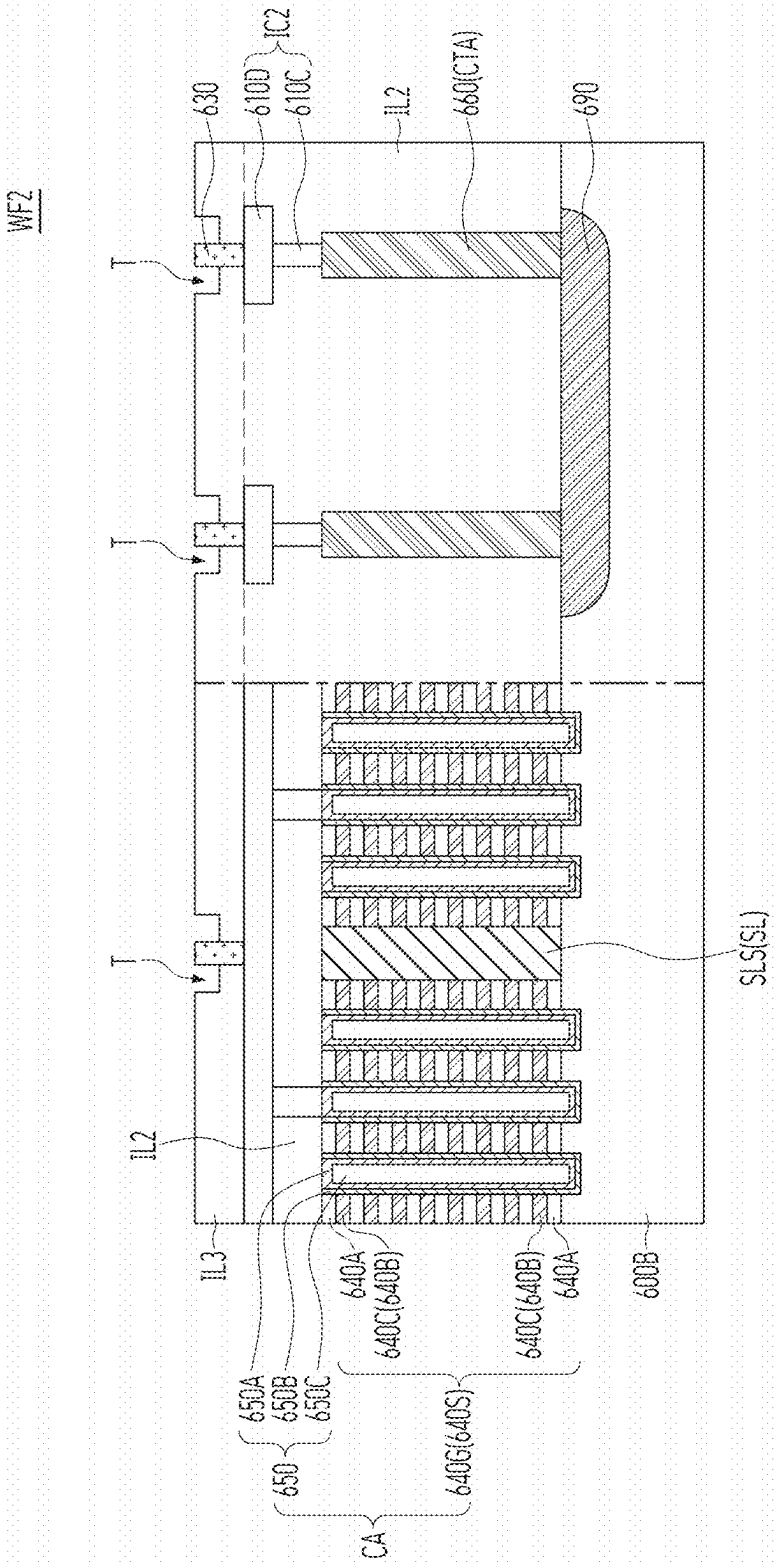
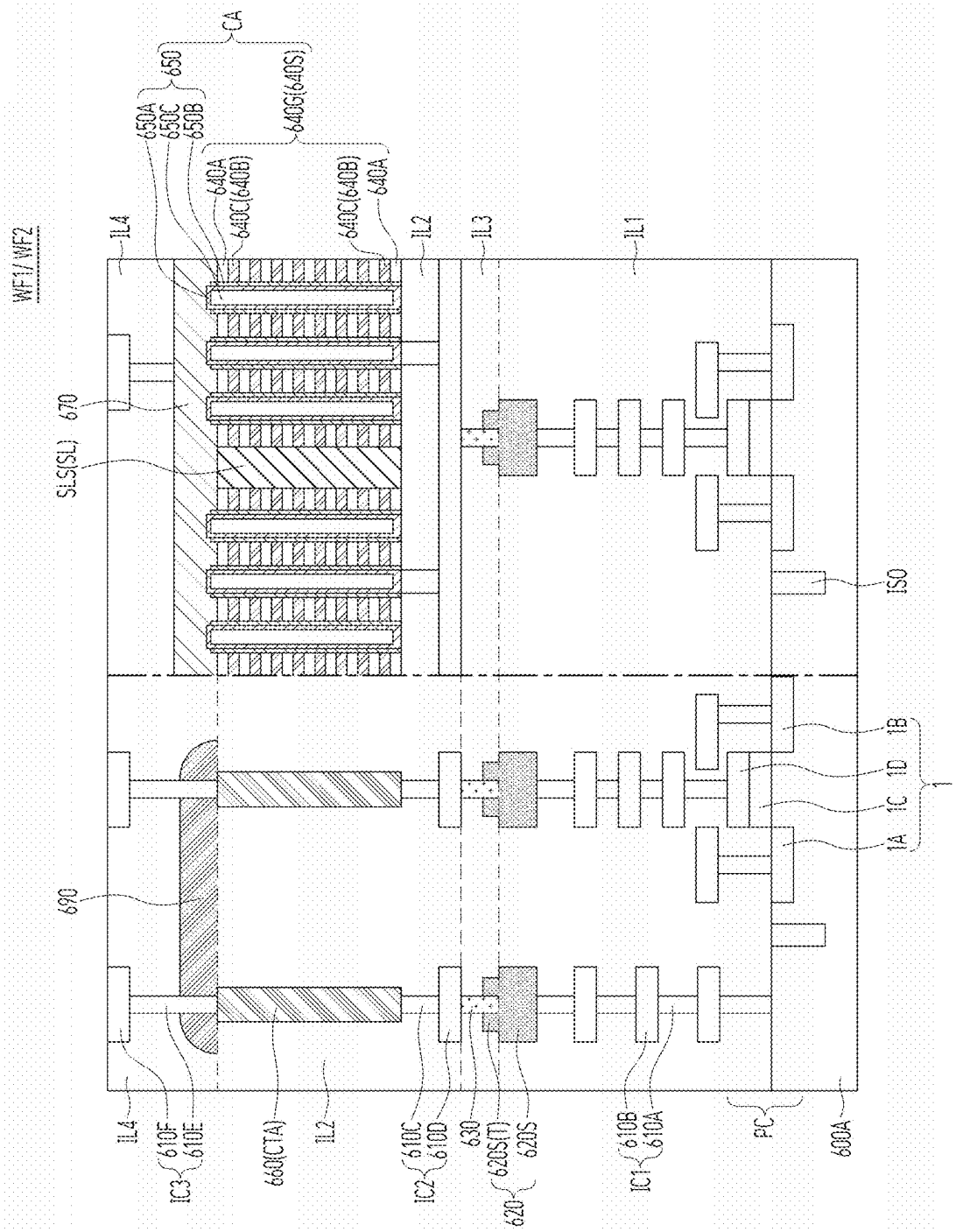

WF2
630
610D
610C
IC2
IL2
660(CTA)
690
T
T
T
SLS(SL)
IL2
IL3
640A
640C(640B)
640C(640B)
640A
600B
650A
650B
650C
650
640G(640S)
CA

FIG. 10


WF1/WF2
CA
650
650A
650C
650B
640G(640S)
640A
640C(640B)
640C(640B)
640A
IL4
IL2
IL3
IL1
670
SLS(SL)
ISO
1B
1D
1C
1A
690
IL4
610F
610E
IC3
660(CTA)
IL2
610C
610D
IC2
630
620(ST)
620S
620
610B
610A
IC1
FC
600A

SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority under 35 U.S.C. § 119 to Korean Patent Application No. 10-2024-0022410 filed on Feb. 16, 2024, which is incorporated herein by reference in its entirety.

BACKGROUND

1. Technical Field

[0002] Embodiments of the present disclosure relate to an electronic device and a method of manufacturing the electronic device, and more particularly, to a semiconductor device and a method of manufacturing the semiconductor device.

2. Related Art

[0003] An integration degree of a semiconductor device is mainly determined by an area occupied by a unit memory cell. Recently, as improvement in an integration degree of a semiconductor device in which a memory cell is formed as a single layer on a substrate reaches a limit, a three-dimensional semiconductor device in which memory cells are stacked on a substrate is being proposed. In addition, various structures and manufacturing methods are being developed to improve operation reliability of the semiconductor device.

SUMMARY

[0004] According to an embodiment of the present disclosure, a three-dimensional semiconductor device (hereinafter referred to simply as semiconductor device) may include a cell array disposed over or on a peripheral circuit, a bonding pad for electrically connecting the peripheral circuit with the cell array, and a bonding via inside the bonding pad.

[0005] According to an embodiment of the present disclosure, a semiconductor device may include a peripheral circuit comprising a plurality of transistors, a cell array and a contact array positioned adjacent to each other over the peripheral circuit, a bonding pad for electrically connecting the peripheral circuit with the cell array and the contact array, the bonding pad comprising first and second portions, wherein the first portion has a first width and is in electrical connection with at least one transistor of the peripheral circuit, wherein the second portion has a second width that is less than the first width of the first portion, and wherein a bonding via electrically connecting the bonding pad with the contact array or the cell array extends partially inside the first portion of the bonding pad.

[0006] According to an embodiment of the present disclosure, a method of manufacturing a semiconductor device may include forming a first wafer including a preliminary bonding pad, forming a second wafer including a substrate, an interlayer insulating layer disposed over or on the substrate, a bonding via positioned in the interlayer insulating layer, and a trench exposing the bonding via, bonding the first wafer and the second wafer so that the preliminary bonding pad and the bonding via contact each other, and forming a bonding pad surrounding the bonding via by expanding the preliminary bonding pad into the trench.

[0007] These and other features and advantages of the embodiments of the present disclosure will become apparent to those skilled in the art from the following detailed description in conjunction with the following drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. **1** is a diagram illustrating a semiconductor device according to an embodiment of the present disclosure.

[0009] FIGS. **2**A and **2**B are diagrams illustrating a semiconductor device according to an embodiment of the present disclosure.

[0010] FIG. **3** is a diagram illustrating a semiconductor device according to an embodiment of the present disclosure.

[0011] FIGS. **4**A to **6** are diagrams illustrating a method of manufacturing a semiconductor device according to an embodiment of the present disclosure.

[0012] FIGS. **7** and **8** are diagrams illustrating a method of manufacturing a semiconductor device according to an embodiment of the present disclosure.

[0013] FIGS. **9** and **10** are diagrams illustrating a method of manufacturing a semiconductor device according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0014] An embodiment of the present disclosure provides a semiconductor device and a method of manufacturing the semiconductor device having a stable structure and an improved characteristic.

[0015] According to embodiments of the present disclosure, a semiconductor device having a stable structure and improved reliability may be provided.

[0016] Hereinafter, embodiments according to the technical concepts of the present disclosure are described with reference to the accompanying drawings.

[0017] FIG. **1** is a diagram illustrating a semiconductor device according to an embodiment of the present disclosure.

[0018] Referring to FIG. **1**, the semiconductor device may include at least one of a substrate **100**, a first interconnection structure IC**1**, a second interconnection structure IC**2**, a third interconnection structure IC**3**, a bonding pad **120**, a bonding via **130**, a gate structure **140**, channel structures **150**, contact plugs **160**, and a source structure **170**. The semiconductor device may further include at least one of a slit structure SLS, an isolation layer ISO, a first interlayer insulating layer IL**1** disposed over the substrate, a second interlayer insulating layer IL**2** disposed over the first interlayer insulating layer IL**1**, a third interlayer insulating layer IL**3** disposed over the second interlayer insulating layer IL**2**, and a fourth interlayer insulating layer IL**4** disposed over the third interlayer insulating layer IL**3**.

[0019] A peripheral circuit PC may be disposed over or on the substrate **100**. The peripheral circuit PC may include at least one transistor **1**, typically a plurality of transistors **1**. Each of the transistors **1** may include junctions **1**A and **1**B, a gate electrode **1**D, and a gate insulating layer **1**C. For example, the gate insulating layer **1**C may be positioned between the gate electrode **1**D and the substrate **100**. The isolation layer ISO may be positioned in the substrate **100**,

and an active region of the transistor **1** may be defined by the isolation layer ISO. The transistors **1** may serve different functions such as amplification, switching, and signal processing, thus supporting the overall operation of the semiconductor device.

[0020] A cell array CA may be disposed over or on the peripheral circuit PC. The cell array CA may include the gate structure **140** and the channel structures **150**. The gate structure **140** may include insulating layers **140**A and conductive layers **140**B that are alternately stacked. The insulating layers **140**A may include an insulating material such as an oxide, and the conductive layers **140**B may include a conductive material such as tungsten, polysilicon, or molybdenum. The channel structures **150** may extend through the gate structure **140**. A source structure **170** may be disposed over or on the cell array CA, and the channel structures **150** may extend into the source structure **170** through the gate structure **140**. Each of the channel structures **150** may include at least one of a channel layer **150**A, a memory layer **150**B surrounding the channel layer **150**A, and an insulating core **150**C in the channel layer **150**A. The slit structure SLS may extend through the gate structure **140**. The slit structure SLS may include an insulating material, a conductive material, a semiconductor material, or the like.

[0021] The conductive layers **140**B may be gate lines such as a source select line, a word line, or a drain select line. A source select transistor, a memory cell, or a drain select transistor may be positioned in a region where the channel structures **150** and the conductive layers **140**B intersect. In an embodiment, at least one source select transistor, a plurality of memory cells, and at least one drain select transistor stacked along the channel structure **150** may configure one memory string.

[0022] A contact array CTA may be disposed over or on the peripheral circuit PC. The contact array CTA may be positioned at a same level as the cell array CA and may include the plurality of contact plugs **160** spaced apart from each other. The contact plugs **160** may be positioned in the third interlayer insulating layer IL**3**. Each of the contact plugs **160** may extend through the entire third interlayer layer IL**3**. The contact plugs **160** may be positioned in the third interlayer insulating layer IL**3**. The contact plugs **160** may include a conductive material such as tungsten.

[0023] The first interconnection structure IC**1** may be disposed over or on the peripheral circuit PC. The first interconnection structure IC**1** may be positioned in the first interlayer insulating layer IL**1**. For example, the first interlayer insulating layer IL**1** may be disposed over or on the substrate **100**. The first interconnection structure IC**1** may include first contact vias **110**A and first contact lines **110**B. At least one of the first contact vias **110**A may be connected to the transistor **1** and may connect the first contact lines **110**B to each other. The first contact vias **110**A may extend in a vertical direction to a top surface of the substrate **100**. The first contact lines **110**B may extend in a direction parallel to the top surface of the substrate **100**. A plurality of parallel first contact lines **110***b* may be arranged at different distances from the substrate **100** inside the first interlayer insulating layer IL**1**. The first interconnection structure IC**1** may include a conductive material such as tungsten. The first interlayer insulating layer IL**1** may include an insulating material such as an oxide or a nitride.

[0024] The second interconnection structure IC**2** may be disposed over or on, for example as illustrated on the first interconnection structure IC**1** and may be positioned under the cell array CA and/or the contact array CTA. The second interconnection structure IC**2** may be positioned in the third interlayer insulating layer IL**3**. For example, the third interlayer insulating layer IL**3** may be disposed over or on second interlayer insulating layer IL**2**. The second interconnection structure IC**2** may include second contact vias **110**C and second contact lines **110**D. At least one of the second contact vias **110**C may be connected to the channel structures **150** and may be connected to at least one of the contact plugs **160**. The second contact lines **110**D may be connected to at least one of the second contact vias **110**C. The second interconnection structure IC**2** may include a conductive material such as tungsten. The third interlayer insulating layer IL**3** may include an insulating material such as an oxide or a nitride.

[0025] The bonding pad **120** may be positioned between the peripheral circuit PC and the cell array CA. Alternatively, the bonding pad **120** may be positioned between the peripheral circuit PC and the contact array CTA. The bonding pad **120** may be positioned in the second interlayer insulating layer IL**2**. For example, the second interlayer insulating layer IL**2** may be positioned between the first interlayer insulating layer IL**1** and the third interlayer insulating layer IL**3**. The bonding pad **120** may include a first portion **120**P**1** having a first width W**1** and a second portion **120**P**2** having a second width W**2**. The first width W**1** may be substantially equal to or different from the second width W**2**. For example, the second width W**2** may be less than the first width W**1**.

[0026] The bonding pad **120** may electrically connect the peripheral circuit PC and the cell array CA. Alternatively, the bonding pad **120** may electrically connect the peripheral circuit PC and the contact array CTA. For example, the bonding pad **120** may electrically connect the peripheral circuit PC and the cell array CA through the first interconnection structure IC**1** and the second interconnection structure IC**2**. Alternatively, the bonding pad **120** may electrically connect the peripheral circuit PC and the contact array CTA through the first interconnection structure IC**1** and the second interconnection structure IC**2**. The bonding pad **120** may include a conductive material such as copper.

[0027] The bonding via **130** may be disposed over or on the bonding pad **120**. The bonding via **130** may extend to the first portion **120**P**1** of the bonding pad **120** by passing through the second portion **120**P**2** of the bonding pad **120**. For example, the second portion **120**P**2** of the bonding pad **120** may surround a portion of a sidewall of the bonding via **130**. In this case, a lower surface of the bonding via **130** may contact the first portion **120**P**1** of the bonding pad **120**, and a side wall of the bonding via **130** may contact the second portion **120**P**2** of the bonding pad **120**. A contact area between the bonding via **130** and the bonding pad **120** may be increased. Therefore, electrical connectivity between the bonding via **130** and the bonding pad **120** may be improved.

[0028] The bonding via **130** may include a material substantially equal to or different from that of the bonding pad **120**. As an example, the bonding via **130** may include copper as the material substantially equal to that of the bonding pad **120**. In this case, an interface between the bonding pad **120** and the bonding via **130** might not exist. As another example, the bonding via **130** may include tungsten as the

material different from that of the bonding pad **120**. In this case, the interface between the bonding pad **120** and the bonding via **130** may exist.

[0029] The third interconnection structure IC**3** may be disposed over or on the cell array CA or the contact array CTA, and may be electrically connected to the cell array CA or the contact array CTA. For example, the third interconnection structure IC**3** may be disposed over or on the source structure **170** and may be electrically connected to the source structure **170**. The third interconnection structure IC**3** may be disposed over or on the contact plugs **160** and may be electrically connected to the contact plugs **160**. The third interconnection structure IC**3** may be positioned in the fourth interlayer insulating layer IL**4**. For example, the fourth interlayer insulating layer IL**4** may be disposed over or on the third interlayer insulating layer IL**3**. Alternatively, the fourth interlayer insulating layer IL**4** may be disposed over or on the source structure **170**.

[0030] The third interconnection structure IC**3** may include third contact vias **110**E and third contact lines **110**F. At least one of the third contact vias **110**E may be connected to the contact plug **160**. At least one of the third contact vias **110**E may be connected to the source structure **170**. At least one of the third contact lines **110**F may be connected to the third contact via **110**E. The third interconnection structure IC**3** may include a conductive material such as tungsten. The fourth interlayer insulating layer IL**4** may include an insulating material such as an oxide or a nitride. The first, second, and third contact vias, **110**A, **110**C, and **110**E may be in the form of vertical lines, i.e., they may be perpendicular to the top surface of the substrate **100**. The first, second, and third contact lines **110**B, **110**D, and **110**F may be in the form of horizontal lines, i.e., they may be extending in parallel to the top surface of the substrate **100**.

[0031] According to the structure described above, the bonding pad **120** may include the second portion **120**P**2** having the second width W**2** less than the first width W**1** of the first portion **120**P**1**. The bonding via **130** may extend to the first portion **120**P**1** by passing through the second portion **120**P**2**. In this case, the contact area between the bonding via **130** and the bonding pad **120** may be increased, and thus electrical connectivity between the bonding via **130** and the bonding pad **120** may be improved.

[0032] FIGS. **2**A and **2**B are diagrams illustrating a semiconductor device according to an embodiment of the present disclosure. FIGS. **2**A and **2**B may be enlarged views of A of FIG. **1**. Hereinafter, any content that overlaps with the content described above may be omitted.

[0033] Referring to FIGS. **2**A and **2**B, the semiconductor device may include at least one of a first interconnection structure IC**1**, a second interconnection structure IC**2**, a bonding pad **220**, a bonding via **230**, and a bonding layer **280**. The semiconductor device may further include at least one of a first interlayer insulating layer IL**1**, a second interlayer insulating layer IL**2**, and a third interlayer insulating layer IL**3**.

[0034] The first interconnection structure IC**1** may be positioned in the first interlayer insulating layer IL**1**. The first interconnection structure IC**1** may include first contact vias **210**A and first contact lines **210**B.

[0035] The bonding pad **220** may be disposed over or on the first interconnection structure IC**1**. The bonding pad **220** may be positioned in the first interlayer insulating layer IL**1** and the bonding layer **280** or in the second interlayer insulating layer IL**2**, and the bonding layer **280**. In an embodiment, the bonding pad **220** may be positioned in the first interlayer insulating layer IL**1**, the second interlayer insulating layer IL**2**, and the bonding layer **280**. The bonding pad **220** may include a first portion **220**P**1** having a first width W**1** and a second portion **220**P**2** having a second width W**2** which may be less than the first width W**1**. Referring to FIG. **2**A, the second portion **220**P**2** of the bonding pad **220** may be positioned in the bonding layer **280**, and the first portion **220**P**1** of the bonding pad **220** may be positioned in the first interlayer insulating layer IL**1**. Referring to FIG. **2**B, the first portion **220**P**1** of the bonding pad **220** may be positioned in the bonding layer **280**, and the second portion **220**P**2** may be positioned in the second interlayer insulating layer IL**2**. For example, the bonding layer **280** may be positioned between the first interlayer insulating layer IL**1** and the second interlayer insulating layer IL**2**. The second interlayer insulating layer IL**2** may be disposed over or on the first interlayer insulating layer IL**1**. The bonding pad **220** may include a conductive material such as copper. In an embodiment, the first portion **220**P**1** and the second portion **220**P**2** of the bonding pad **220** may be positioned in the bonding layer **280**.

[0036] The bonding layer **280** may include a material substantially equal to or different from that of the first interlayer insulating layer IL**1** or the second interlayer insulating layer IL**2**. For example, the bonding layer **280** may include a nitride, and the first interlayer insulating layer IL**1** and the second interlayer insulating layer IL**2** may include an oxide. Using nitride for the bonding layer **280** is advantageous because it may increase the bonding force at an interface between the bonding layer **280** and each of the interlayer insulating layers IL**1** and IL**2**. For example, referring to FIG. **2**A, the bonding force between the bonding layer **280** and the first interlayer insulating layer IL**1** may increase. Referring to FIG. **2**B, the bonding force between the bonding layer **280** and the second interlayer insulating layer IL**2** may increase.

[0037] The bonding via **230** may be positioned on the bonding pad **220**. The bonding via **230** may be positioned in the second interlayer insulating layer IL**2**. The bonding via **230** may extend to the first portion **220**P**1** of the bonding pad **220** by passing through the second portion **220**P**2** of the bonding pad **220**. Therefore, the second portion **220**P**2** of the bonding pad **220** may surround a portion of a sidewall of the bonding via **230**. In this case, electrical connectivity between the bonding via **230** and the bonding pad **220** may be improved.

[0038] The bonding via **230** may include a material substantially equal to or different from that of the bonding pad **220**. For example, the bonding via **230** may include tungsten as the material different from that of the bonding pad **220**. In this case, an interface between the bonding pad **220** and the bonding via **230** may exist.

[0039] The second interconnection structure IC**2** may be disposed over or on the bonding via **230**. The second interconnection structure IC**2** may be positioned in the third interlayer insulating layer IL**3**. The third interlayer insulating layer IL**3** may be disposed over or on the second interlayer insulating layer IL**2**. The second interconnection structure IC**2** may include second contact vias **210**C and second contact lines **210**D.

[0040] According to the structure described above, the bonding layer **280** may be positioned between the first

interlayer insulating layer IL**1** and the second interlayer insulating layer IL**2**. In this case, bonding force may increase at the interface between the bonding layer **280** and the interlayer insulating layers IL**1** and IL**2**.

[0041] FIG. **3** is a diagram illustrating a semiconductor device according to an embodiment of the present disclosure. Hereinafter, any content that overlaps with the content described above may be omitted.

[0042] Referring to FIG. **3**, the semiconductor device may include at least one of a substrate **300**, a first interconnection structure IC**1**, a second interconnection structure IC**2**, a third interconnection structure IC**3**, a bonding pad **320**, a bonding via **330**, a gate structure **340**, channel structures **350**, contact plugs **360**, a source structure **370**, and a protective layer **390**. The semiconductor device may further include at least one of a slit structure SLS, an isolation layer ISO, a first interlayer insulating layer IL**1**, a second interlayer insulating layer IL**2**, a third interlayer insulating layer IL**3**, and a fourth interlayer insulating layer IL**4**.

[0043] A peripheral circuit PC may be disposed over or on the substrate **300**. A cell array CA and a contact array CTA may be disposed over or on the peripheral circuit PC. The cell array CA and the contact array CTA may be positioned at a same level from the substrate **300**. The cell array CA may include the gate structure **340** and the channel structures **350** arranged spaced part from each other inside the gate structure **340**. The contact array CTA may include the contact plugs **360**. For reference, the cell array CA may be positioned in a chip region of the semiconductor device, and the contact array CTA may be positioned in a sealing region of the semiconductor device. For example, the sealing region may be a region surrounding the chip region to protect the chip region in a process of manufacturing the semiconductor device.

[0044] The gate structure **340** may include insulating layers **340**A and conductive layers **340**B that are alternately stacked. The channel structures **350** may extend through the gate structure **340**. The source structure **370** may be disposed over, or as illustrated, on the cell array CA, and the channel structures **350** may extend into the source structure **370** through the gate structure **340**. Each of the channel structures **350** may include at least one of a channel layer **350**A, a memory layer **350**B surrounding the channel layer **350**A, and an insulating core **350**C in the channel layer **350**A.

[0045] The first interconnection structure IC**1** may be disposed over, or as illustrated, on the peripheral circuit PC. The first interconnection structure IC**1** may be positioned in the first interlayer insulating layer IL**1**. For example, the first interlayer insulating layer IL**1** may be disposed over, or as illustrated, on the substrate **300**. The first interconnection structure IC**1** may include first contact vias **310**A and first contact lines **310**B.

[0046] The second interconnection structure IC**2** may be disposed over, or as illustrated, on the first interconnection structure IC**1** and may be positioned under the cell array CA and the contact array CTA. The second interconnection structure IC**2** may be positioned in the third interlayer insulating layer IL**3**. The third interlayer insulating layer IL**3** may be disposed over, or as illustrated, on the first interlayer insulating layer IL**1**. The second interconnection structure IC**2** may include second contact vias **310**C and second contact lines **310**D.

[0047] The bonding pad **320** may be positioned between the peripheral circuit PC and the cell array CA. Alternatively, the bonding pad **320** may be positioned between the peripheral circuit PC and the contact array CTA. The bonding pad **320** may be positioned in the second interlayer insulating layer IL**2**. For example, the second interlayer insulating layer IL**2** may be positioned between the first interlayer insulating layer IL**1** and the third interlayer insulating layer IL**3**. The bonding pad **320** may include a first portion **320**P**1** having a first width W**1** and a second portion **320**P**2** having a second width W**2** less than the first width W**1**.

[0048] The bonding pad **320** may electrically connect the peripheral circuit PC and the cell array CA, and may electrically connect the peripheral circuit PC and the contact array CTA. For example, the bonding pad **320** may electrically connect the peripheral circuit PC and the cell array CA through the first interconnection structure IC**1** and the second interconnection structure IC**2**, and may electrically connect the peripheral circuit PC and the contact array CTA through the interconnection structure IC**1** and the second interconnection structure IC**2**. The bonding pad **320** may include a conductive material such as copper.

[0049] The bonding via **330** may be disposed over, or as illustrated, on the bonding pad **320**. The bonding via **330** may extend to the first portion **320**P**1** of the bonding pad **320** by passing through the second portion **320**P**2** of the bonding pad **320**. Therefore, the second portion **320**P**2** of the bonding pad **320** may surround a portion of a sidewall of the bonding via **330**.

[0050] The bonding via **330** may include a material substantially equal to or different from that of the bonding pad **320**. For example, the bonding via **330** may include tungsten as the material different from that of the bonding pad **320**. For example, an interface between the bonding pad **320** and the bonding via **330** may exist.

[0051] The protective layer **390** may be disposed over, or as illustrated, on the contact array CTA. For example, the protective layer **390** may be disposed over, or as illustrated, on the contact plugs **360**. The protective layer **390** may be positioned in the sealing region of the semiconductor device. For example, the protective layer **390** may be positioned in the fourth interlayer insulating layer IL**4**. The fourth interlayer insulating layer IL**4** may be disposed over, or as illustrated, on the third interlayer insulating layer IL**3** and may be disposed over, or as illustrated, on the source structure **370**. The protective layer **390** may prevent or reduce damage to the substrate on which the protective layer **390** is formed in a process of forming the contact plugs **360**. The protective layer **390** may include an insulating material such as an oxide.

[0052] The third interconnection structure IC**3** may be disposed over, or as illustrated, on the cell array CA or the contact array CTA, and may be electrically connected to the cell array CA or the contact array CTA. For example, the third interconnection structure IC**3** may be disposed over, or as illustrated, on the source structure **370** and may be electrically connected to the source structure **370**. The third interconnection structure IC**3** may be disposed over, or as illustrated, on the contact plugs **360** and may be electrically connected to the contact plugs **360**. The third interconnection structure IC**3** may be connected to the contact array CTA through the protective layer **390**. The third interconnection structure IC**3** may be positioned in the fourth

interlayer insulating layer IL**4**. The third interconnection structure IC**3** may include third contact vias **310**E and third contact lines **310**F.

[0053] For reference, although not shown in this drawing, a bonding layer may be positioned between the first interlayer insulating layer IL**1** and the second interlayer insulating layer IL**2**. For example, the bonding layer **280** of FIGS. **2**A and **2**B may be positioned between the first interlayer insulating layer IL**1** and the second interlayer insulating layer IL**2**. For example, the bonding layer may increase bonding force at an interface with the interlayer insulating layers IL**1** and IL**2**.

[0054] According to the structure described above, the protective layer **390** may be disposed over, or as illustrated, on the contact array CTA. The protective layer **390** may be positioned in the sealing region surrounding the chip region where the cell array CA of the semiconductor device is positioned. The protective layer **390** may prevent or reduce damage to the substrate on which the protective layer **390** is formed in a process of forming the contact plugs **360** of the contact array CTA.

[0055] FIGS. **4**A to **6** are diagrams illustrating a method of manufacturing a semiconductor device according to an embodiment of the present disclosure. Hereinafter, any content that overlaps with the content described above may be omitted.

[0056] Referring to FIG. **4**A, a first wafer WF**1** may be formed. A peripheral circuit PC may be formed over or on a first substrate **400**A. The peripheral circuit PC may include at least one transistor **1**. An isolation layer ISO may be formed in the first substrate **400**A and may define an active region of the transistor **1**.

[0057] A first interconnection structure IC**1** may be formed on the first substrate **400**A. The first interconnection structure IC**1** may be formed in a first interlayer insulating layer IL**1**. For example, the first interlayer insulating layer IL**1** may be formed on the first substrate **400**A. The first interconnection structure IC**1** may include a first contact via **410**A and a first contact line **410**B. The first contact via **410**A may be connected to the peripheral circuit PC. Alternatively, the first contact via **410**A may connect the first contact lines **410**B. The first interconnection structure IC**1** may include a conductive material such as tungsten. The first interlayer insulating layer IL**1** may include an insulating material such as an oxide.

[0058] A preliminary bonding pad **420**S may be formed on the first interconnection structure IC**1**. The preliminary bonding pad **420**S may be formed in the first interlayer insulating layer IL**1**. The preliminary bonding pad **420**S may be connected to the peripheral circuit PC through the first interconnection structure IC**1**. The preliminary bonding pad **420**S may include a conductive material such as copper.

[0059] Referring to FIG. **4**B, a second wafer WF**2** may be formed. A stack **440**S may be formed by alternately stacking first material layers **440**A and second material layers **440**B over or on a second substrate **400**B. For example, the first material layers **440**A may include an insulating material such as an oxide, and the second material layers **440**B may include a sacrificial material such as a nitride.

[0060] Channel structures **450** extending into the second substrate **400**B through the stack **440**S may be formed. Each of the channel structures **450** may include a channel layer **450**A, a memory layer **450**B surrounding the channel layer **450**A, and an insulating core **450**C in the channel layer **450**A.

[0061] A slit SL extending through the stack **440**S may be formed and the second material layers **440**B of the stack **440**S may be replaced with third material layers **440**C through the slit SL. Accordingly, a gate structure **440**G including the first material layers **440**A and the third material layers **440**C alternately stacked may be defined. For example, the third material layers **440**C may include a conductive material such as tungsten. For reference, when the second material layers **440**B include a conductive material, a process of replacing the second material layers **440**B with the third material layers **440**C may be omitted. Accordingly, a cell array CA including the gate structure **440**G and the channel structures **450** may be defined.

[0062] Subsequently, a slit structure SLS may be formed in the slit SL. The slit structure SLS may include an insulating material, a conductive material, a semiconductor material, or the like.

[0063] A second interlayer insulating layer IL**2** may be formed on the second substrate **400**B. The second interlayer insulating layer IL**2** may be formed also on the gate structure **440**G. A contact array CTA including contact plugs **460** may be formed over or on the second substrate **400**B. The contact plugs **460** may be formed in the second interlayer insulating layer IL**2**. The second interlayer insulating layer IL**2** may include an insulating material such as an oxide.

[0064] A second interconnection structure IC**2** may be formed on the contact plugs **460**. The second interconnection structure IC**2** may be formed over or on the gate structure **440**G. The second interconnection structure IC**2** may be formed in a second interlayer insulating layer IL**2**. The second interconnection structure IC**2** may include a second contact via **410**C and a second contact line **410**D. The second interconnection structure IC**2** may include a conductive material such as tungsten.

[0065] A third interlayer insulating layer IL**3** may be formed on the second interconnection structure IC**2**. The third interlayer insulating layer IL**3** may include an insulating material such as an oxide. A bonding via **430** may be formed in the third interlayer insulating layer IL**3**. The bonding via **430** may be connected to the second interconnection structure IC**2**. The bonding via **430** may include a conductive material such as tungsten.

[0066] A trench T exposing the bonding via **430** may be formed. For example, the third interlayer insulating layer IL**3** may be etched to form the trench T exposing a sidewall of the bonding via **430**. A depth of the trench T may be determined by controlling a time for etching the third interlayer insulating layer IL**3**. Therefore, the trench T exposing the sidewall of the bonding via **430** may be formed by controlling the time for etching the third interlayer insulating layer IL**3**.

[0067] Referring to FIG. **5**, the first wafer WF**1** and the second wafer WF**2** may be bonded. For example, the first wafer WF**1** and the second wafer WF**2** may be bonded so that a preliminary bonding pad **420**S of the first wafer WF**1** and the bonding via **430** of the second wafer WF**2** are in contact with each other. In a process of bonding the first wafer WF**1** and the second wafer WF**2**, the preliminary bonding pad **420**S of the first wafer WF**1** may be expanded.

In this case, a delamination phenomenon may occur at an interface between the first wafer WF**1** and the second wafer WF**2**.

[0068] According to an embodiment of the present disclosure, the preliminary bonding pad **420**S of the first wafer WF**1** may be expanded into the trench T of the second wafer WF**2**. Therefore, even though the preliminary bonding pad **420**S of the first wafer WF**1** is expanded, a delamination phenomenon might not occur at the interface between the first wafer WF**1** and the second wafer WF**2**. As the preliminary bonding pad **420** is expanded into the trench T, the bonding pad **420** surrounding the bonding via **430** of the second wafer WF**2** may be formed.

[0069] Referring to FIG. **6**, the second substrate **400**B may be removed to expose the channel structures **450**. Subsequently, the memory layer **450**B of the channel structures **450** may be partially removed to expose the channel layer **450**A. Subsequently, a source structure **470** connected to the channel structures **450** may be formed. For example, the source structure **470** may be connected to the channel layer **450**A of the channel structures **450**.

[0070] Subsequently, a fourth interlayer insulating layer IL**4** may be formed on the source structure **470**. The fourth interlayer insulating layer IL**4** may also be formed on the contact plugs **460**. The fourth interlayer insulating layer IL**4** may include an insulating material such as an oxide. Subsequently, a third interconnection structure IC**3** may be formed in the fourth interlayer insulating layer IL**4**. The third interconnection structure IC**3** may include a third contact via **410**E and a third contact line **410**F. The third contact via **410***e* may be connected to the contact plug **460**. Alternatively, the third contact via **410**E may be connected to the source structure **470**. The third interconnection structure IC**3** may include a conductive material such as tungsten.

[0071] According to the manufacturing method described above, in the process of bonding the first wafer WF**1** and the second wafer WF**2**, the preliminary bonding pad **420**S of the first wafer WF**1** may be expanded into the trench of the second wafer WF**2**. Therefore, even though the preliminary bonding pad **420**S is expanded, a delamination phenomenon might not occur at the interface between the first and second wafers WF**1** and WF**2**.

[0072] FIGS. **7** and **8** are diagrams illustrating a method of manufacturing a semiconductor device according to an embodiment of the present disclosure. Hereinafter, any content that overlaps with the content described above may be omitted.

[0073] Referring to FIG. **7**, a second wafer WF**2** including a second substrate **500**B, a gate structure **540**G over or on the second substrate **500**B, channel structures **550** extending into the second substrate **500**B through the gate structure **540**G, a slit structure SLS extending through the gate structure **540**G, contact plugs **560** over or on the second substrate **500**B, a second interconnection structure IC**2** over or on the gate structure **540**G and the contact plugs **560**, and a bonding via **530** on the second interconnection structure IC**2** may be formed.

[0074] The contact plugs **560** and the second interconnection structure IC**2** may be formed in a second interlayer insulating layer IL**2**. For example, the second interlayer insulating layer IL**2** may be formed on the second substrate **500**B. The bonding via **530** may be formed in a third interlayer insulating layer IL**3** and a bonding layer **580**. For example, the third interlayer insulating layer IL**3** may be formed on the second interlayer insulating layer IL**2**. The bonding layer **580** may be formed on the third interlayer insulating layer IL**3**. The second interlayer insulating layer IL**2** and the third interlayer insulating layer IL**3** may include an insulating material such as an oxide, and the bonding layer **580** may include an insulating material such as a nitride.

[0075] Subsequently, a trench T exposing the bonding via **530** may be formed. For example, the bonding layer **580** may be etched to form the trench T exposing a sidewall of the bonding via **530**.

[0076] Referring to FIG. **8**, the first wafer WF**1** and the second wafer WF**2** may be bonded. For example, the first wafer WF**1** may include a first substrate **500**A, a peripheral circuit PC over or on the first substrate **500**A, a first interlayer insulating layer IL**1** on the first substrate **500**A, a first interconnection structure IC**1** in the first interlayer insulating layer IL**1**, and a preliminary bonding pad **520**S in the first interlayer insulating layer IL**1**.

[0077] In a process of bonding the first and second wafers WF**1** and WF**2**, the preliminary bonding pad **520**S of the first wafer WF**1** may be expanded into the trench T of the second wafer WF**2**. Therefore, even though the preliminary bonding pad **520**S is expanded, a delamination phenomenon might not occur at an interface between the first and second wafers WF**1** and WF**2**.

[0078] In addition, because the bonding layer **580** of the second wafer WF**2** includes a nitride, the bonding force at an interface between the bonding layer **580** and the first interlayer insulating layer IL**1** may be increased. The bonding force between the first and second wafers WF**1** and WF**2** may increase.

[0079] Subsequently, the second substrate **500**B may be removed to expose the channel structures **550** and a source structure **570** connected to the channel structures **550** may be formed over or on the channel structure **550**. Subsequently, a fourth interlayer insulating layer IL**4** may be formed on the source structure **570** and the contact plugs **560**. Subsequently, third interconnection structures IC**3** may be formed in the fourth interlayer insulating layer IL**4**. Each of the third interconnection structures IC**3** may be connected to the contact plug **560** or the source structure **570**.

[0080] For reference, although not shown in this drawing, the bonding layer **580** may be formed in a process of forming the first wafer WF**1**. For example, the preliminary bonding pad **520**S may be formed in the bonding layer **580**. In this case, bonding force may increase at an interface between the bonding layer **580** and the third interlayer insulating layer IL**3** of the second wafer WF**2**.

[0081] Alternatively, the bonding layer **580** may also be formed over or on the first wafer WF**1** and the second wafer WF**2**, respectively. For example, the preliminary bonding pad **520**S of the first wafer WF**1** may be formed in the bonding layer **580** of the first wafer WF**1**, and the bonding via **530** of the second wafer WF**2** may be formed in the bonding layer **580** of the second wafer WF**2**. In this case, the bonding layer **580** of the first wafer WF**1** and the bonding layer **580** of the second wafer WF**2** may be bonded.

[0082] According to the manufacturing method described above, the bonding layer **580** may be formed in a process of forming the first wafer WF**1**. Alternatively, the bonding layer **580** may be formed in a process of forming the second wafer WF**2**. The bonding layer **580** may include a nitride. Because the bonding layer **580** includes a nitride, the bond-

ing force at an interface between the bonding layer **580** and the interlayer insulating layers IL**1** and IL**3** may increase. Therefore, the bonding force between the first wafer WF**1** and the second wafer WF**2** may increase.

[0083] FIGS. **9** and **10** are diagrams illustrating a method of manufacturing a semiconductor device according to an embodiment of the present disclosure. Hereinafter, any content that overlaps with the content described above may be omitted.

[0084] Referring to FIG. **9**, a second wafer WF**2** may be formed. First, a protective layer **690** may be formed in a second substrate **600**B. The protective layer **690** may be formed in a sealing region of the substrate. For example, the sealing region may be a region surrounding a chip region to protect the chip region in a process of manufacturing the semiconductor device. For example, the sealing region may be a region surrounding the entire sidewall of the chip region. The protective layer **690** may include an insulating material such as an oxide. Subsequently, the second wafer WF**2** including a gate structure **640**G over or on the second substrate **600**B, channel structures **650** extending into the second substrate **600**B through the gate structure **640**G, a slit structure SLS extending through the gate structure **640**G, contact plugs **660** over or on the second substrate **600**B, a second interconnection structure IC**2** over or on the gate structure **640**G and the contact plugs **660**, and a bonding via **630** over or on the second interconnection structure IC**2** may be formed.

[0085] For example, a cell array CA including the gate structure **640**G and the channel structures **650** may be formed in the chip region. A contact array CTA including the contact plugs **660** may be formed in the sealing region. For example, the contact plugs **660** may be formed over or on the protective layer **690**. The second substrate **600**B may be damaged in a process of forming the contact plugs **660**. For example, the second substrate **600**B may be exposed in a process of forming contact holes for forming the contact plugs **660**. In this case, a portion of the second substrate **600**B may be etched and damaged. However, according to an embodiment of the present disclosure, the protective layer **690** may be formed in the second substrate **600**B, thereby preventing or minimizing damage to the second substrate **600**B in the process of forming the contact holes. The contact plugs **660** and the second interconnection structure IC**2** may be formed in a second interlayer insulating layer IL**2**. For example, the second interlayer insulating layer IL**2** may be formed over or on the second substrate **600**B. The bonding via **630** may be formed in a third interlayer insulating layer IL**3**.

[0086] Subsequently, a trench T exposing the bonding via **630** may be formed. For example, the third interlayer insulating layer IL**3** may be etched to form the trench T exposing a sidewall of the bonding via **630**.

[0087] Referring to FIG. **10**, a first wafer WF**1** and the second wafer WF**2** may be bonded. For example, the first wafer WF**1** may include a first substrate **600**A, a peripheral circuit PC over or on the first substrate **600**A, a first interlayer insulating layer IL**1** over or on the first substrate **600**A, a first interconnection structure IC**1** in the first interlayer insulating layer IL**1**, and a preliminary bonding pad **620**S in the first interlayer insulating layer IL**1**.

[0088] In a process of bonding the first wafer WF**1** and the second wafer WF**2**, the preliminary bonding pad **620**S of the first wafer WF**1** may be expanded into the trench T of the second wafer WF**2**. Therefore, even though the preliminary bonding pad **620**S is expanded, a delamination phenomenon might not occur at an interface between the first and second wafers WF**1** and WF**2**.

[0089] Subsequently, the second substrate **600**B may be removed to expose the channel structures **650**. The second substrate **600**B may be removed to expose the protective layer **690**. Subsequently, a source structure **670** connected to the channel structures **650** may be formed. Subsequently, a fourth interlayer insulating layer IL**4** may be formed on the source structure **670** and the protective layer **690**. Subsequently, a third interconnection structure IC**3** may be formed in the fourth interlayer insulating layer IL**4**. The third interconnection structure IC**3** may be connected to the contact plug **660** or the source structure **670**. For example, the third interconnection structure IC**3** may be connected to the contact plug **660** through the protective layer **690**.

[0090] For reference, after removing the second substrate **600**B, the protective layer **690** may also be removed, and in this case, the third interconnection structure IC**3** may be connected to the contact plug **660** through the fourth interlayer insulating layer IL**4**.

[0091] In addition, in an embodiment a bonding layer may be formed in the process of forming the first wafer WF**1** or the second wafer WF**2**. For example, referring to FIGS. **7** and **8**, the bonding layer **580** may be formed over or on the first wafer WF**1** or the second wafer WF**2**. For example, the bonding layer may include nitride. Therefore, the bonding force between the first wafer WF**1** and the second wafer WF**2** may increase.

[0092] According to the manufacturing method described above, the protective layer **690** may be formed in the second substrate **600**B. The protective layer **690** may be formed in the sealing region surrounding the chip region. The protective layer **690** may prevent or minimize damage to the second substrate **600**B in the process of forming the contact plugs **660** of the contact array CTA.

[0093] Although embodiments according to the technical concepts of the present disclosure have been described with reference to the accompanying drawings, the embodiments of the present disclosure are not limited to the above-described embodiments. Within the scope of the technical concepts of the present disclosure described in the claims, various forms of substitution, modification, and change of the embodiments will be possible by those skilled in the art to which the present disclosure belongs.

What is claimed is:

1. A semiconductor device comprising:
a cell array disposed over or on a peripheral circuit;
a bonding pad for electrically connecting the peripheral circuit with the cell array; and
a bonding via extending inside the bonding pad.

2. The semiconductor device of claim **1**, further comprising:
an interlayer insulating layer surrounding a first portion; and
a bonding layer surrounding a second portion.

3. The semiconductor device of claim **1**, further comprising:
a bonding layer surrounding a first portion; and
an interlayer insulating layer surrounding a first portion.

4. The semiconductor device of claim **3**, wherein the interlayer insulating layer includes a material different from the bonding layer.

5. The semiconductor device of claim 4, wherein the interlayer insulating layer includes oxide and the bonding layer includes nitride, and

wherein the bonding pad includes a two-part shape including the first portion and the second portion having different widths.

6. The semiconductor device of claim 1, further comprising:

a contact array disposed over or on the peripheral circuit and positioned at a level corresponding to the cell array.

7. The semiconductor device of claim 6, further comprising:

a protective layer disposed over or on the contact array.

8. The semiconductor device of claim 7, further comprising:

an interconnection structure electrically connected to the contact array through the protective layer.

9. The semiconductor device of claim 7, wherein the protective layer includes oxide.

10. The semiconductor device of claim 1, further comprising:

a source structure disposed over or on the cell array.

11. The semiconductor device of claim 10, further comprising:

an interconnection structure disposed over or on the source structure and electrically connected to the source structure.

12. A semiconductor device comprising:

a peripheral circuit comprising a plurality of transistors;

a cell array and a contact array positioned adjacent to each other over the peripheral circuit;

bonding pads for electrically connecting the peripheral circuit with the cell array and for electrically connecting the peripheral circuit with the contact array,

each of the bonding pads comprising first portion and second portion;

wherein the first portion has a first width and is in electrical connection with at least one transistor of the peripheral circuit,

wherein the second portion has a second width that is less than the first width of the first portion, and

wherein a bonding via electrically connecting the bonding pad with the contact array or the cell array extends partially inside the first portion of the bonding pad.

13. The semiconductor device of claim 12, further comprising:

an interlayer insulating layer surrounding the first portion; and

a bonding layer surrounding the second portion.

14. The semiconductor device of claim 12, further comprising:

a bonding layer surrounding the first portion; and

an interlayer insulating layer surrounding the first portion.

15. The semiconductor device of claim 14, wherein the interlayer insulating layer includes a material different from the bonding layer.

16. The semiconductor device of claim 15, wherein the interlayer insulating layer includes oxide and the bonding layer includes nitride.

17. The semiconductor device of claim 12, further comprising:

a protective layer disposed over or on the contact array.

18. The semiconductor device of claim 17, further comprising:

an interconnection structure electrically connected to the contact array through the protective layer.

19. The semiconductor device of claim 17, wherein the protective layer includes oxide.

20. The semiconductor device of claim 12, further comprising:

a source structure disposed over or on the cell array.

21. The semiconductor device of claim 20, further comprising:

an interconnection structure disposed over or on the source structure and electrically connected to the source structure.

22. A method of manufacturing a semiconductor device, the method comprising:

forming a first wafer including a preliminary bonding pad;

forming a second wafer including a substrate, an interlayer insulating layer disposed over or on the substrate, a bonding via positioned in the interlayer insulating layer, and a trench exposing the bonding via;

bonding the first wafer and the second wafer so that the preliminary bonding pad and the bonding via contact each other; and

forming a bonding pad surrounding the bonding via by expanding the preliminary bonding pad into the trench.

23. The method of claim 22, wherein forming the second wafer comprises:

forming the interlayer insulating layer on the substrate;

forming the bonding via in the interlayer insulating layer; and

forming the trench exposing a sidewall of the bonding via, in the interlayer insulating layer.

24. The method of claim 22, wherein forming the second wafer comprises:

forming the interlayer insulating layer on the substrate;

forming a bonding layer on the interlayer insulating layer;

forming the bonding via in the interlayer insulating layer and the bonding layer; and

forming the trench in the bonding layer.

25. The method of claim 22, wherein forming the second wafer comprises:

forming a protective layer in the substrate; and

forming a contact array including a contact plug disposed over or on the protective layer.

26. The method of claim 25, further comprising:

exposing the protective layer by removing the substrate; and

forming an interconnection structure connected to the contact plug through the protective layer.

27. The method of claim 25, further comprising:

exposing the contact plug by removing the substrate and the protective layer; and

forming an interconnection structure connected to the contact plug.

28. The method of claim 22, wherein forming the second wafer comprises forming a cell array including channel structures disposed over or on the substrate.

29. The method of claim 28, further comprising:

removing the substrate; and

forming a source structure connected to the channel structures.

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