US Patent & Trademark Office
Patent Public Search | Text View

United States Patent	12393214
Kind Code	B2
Date of Patent	August 19, 2025
Inventor(s)	Richmond; James et al.

Device design for short-circuit protection of transistors

Abstract

A transistor semiconductor die includes a first current terminal, a second current terminal, and a control terminal. A semiconductor structure is between the first current terminal, the second current terminal, and the control terminal and configured such that a resistance between the first current terminal and the second current terminal is based on a control signal provided at the control terminal. Short circuit protection circuitry is coupled between the control terminal and the second current terminal. In a normal mode of operation, the short circuit protection circuitry is configured to provide a voltage drop that is greater than a voltage of the control signal. In a short circuit protection mode of operation, the short circuit protection circuitry is configured to provide a voltage drop that is less than a voltage of the control signal.

Inventors: **Richmond; James (Hillsborough, NC), Van Brunt; Edward Robert (Raleigh, NC), Steinmann; Philipp (Durham, NC)**

Applicant: **Wolfspeed, Inc.** (Durham, NC)

Family ID: **1000008766382**

Assignee: **Wolfspeed, Inc. (Durham, NC)**

Appl. No.: **18/093838**

Filed: **January 06, 2023**

Prior Publication Data

Document Identifier	Publication Date
US 20230152830 A1	May. 18, 2023

Related U.S. Application Data

continuation parent-doc US 16448538 20190621 US 11579645 child-doc US 18093838

Publication Classification

Int. Cl.: **G05F1/569** (20060101); **G01R31/50** (20200101); **G05F3/20** (20060101); **H10D62/832** (20250101)

U.S. Cl.:

CPC **G05F1/569** (20130101); **G01R31/50** (20200101); **G05F3/20** (20130101); **H10D62/8325** (20250101);

Field of Classification Search

CPC: H02H (9/04-046)

References Cited

U.S. PATENT DOCUMENTS

Patent No.	Issued Date	Patentee Name	U.S. Cl.	CPC
4142115	12/1978	Nakata et al.	N/A	N/A
4760434	12/1987	Tsuzuki et al.	N/A	N/A
4893159	12/1989	Suzuki et al.	N/A	N/A
5119162	12/1991	Todd et al.	N/A	N/A
5311391	12/1993	Dungan et al.	N/A	N/A
5631494	12/1996	Sakurai	257/E29.198	H01L 27/0251
5691557	12/1996	Watanabe	N/A	N/A
5754074	12/1997	Kelly	N/A	N/A
5812006	12/1997	Teggatz	327/309	H03K 17/0822
5825603	12/1997	Parat et al.	N/A	N/A
5886543	12/1998	Moody	N/A	N/A
5894200	12/1998	Goodale, Jr.	315/307	H05B 39/047
5978192	12/1998	Young et al.	N/A	N/A
6541826	12/2002	Iwagami	438/210	H01L 27/0248
6906386	12/2004	Williams	257/E23.044	H01L 23/62
7511357	12/2008	Hshieh	257/481	H01L 27/0255
8022505	12/2010	Renaud	257/355	H01L 27/0259
8437109	12/2012	Wu	N/A	N/A
8743518	12/2013	Ozard	N/A	N/A
9136381	12/2014	Kocon et al.	N/A	N/A
9349721	12/2015	Saito et al.	N/A	N/A
9379181	12/2015	Sugimoto	N/A	N/A
9786778	12/2016	Morizuka	N/A	N/A
9998109	12/2017	Das et al.	N/A	N/A
10026728	12/2017	Agam et al.	N/A	N/A
10529812	12/2019	Edwards	N/A	N/A

10879692	12/2019	Kubo et al.	N/A	N/A
10950596	12/2020	Zeng et al.	N/A	N/A
11322610	12/2021	Kim et al.	N/A	N/A
2002/0018330	12/2001	Bremond et al.	N/A	N/A
2003/0141918	12/2002	Uno	N/A	N/A
2004/0084753	12/2003	Fruth et al.	N/A	N/A
2004/0113172	12/2003	Yasuda	257/197	H03K 17/08128
2005/0122748	12/2004	Tadokoro et al.	N/A	N/A
2005/0167742	12/2004	Challa et al.	N/A	N/A
2006/0113593	12/2005	Sankin et al.	N/A	N/A
2006/0203400	12/2005	Bodano	257/E23.044	H01L 27/0658
2006/0284276	12/2005	Yilmaz	N/A	N/A
2007/0168638	12/2006	Hepkin et al.	N/A	N/A
2007/0258176	12/2006	Ball	361/56	H05B 45/44
2007/0290738	12/2006	Wendt	327/427	H03K 17/0822
2008/0258224	12/2007	Hshieh	N/A	N/A
2008/0272828	12/2007	Min	327/512	G01K 7/01
2009/0195947	12/2008	Ootsuka et al.	N/A	N/A
2010/0001783	12/2009	Ronsisvalle et al.	N/A	N/A
2011/0049564	12/2010	Guan et al.	N/A	N/A
2011/0073906	12/2010	Bobde et al.	N/A	N/A
2011/0127586	12/2010	Bobde et al.	N/A	N/A
2011/0227095	12/2010	Treu	257/77	H03K 17/567
2012/0007138	12/2011	Nguyen	N/A	N/A
2012/0037955	12/2011	Hirler	257/140	H01L 29/7397
2012/0120531	12/2011	Abou-Khalil et al.	N/A	N/A
2012/0193676	12/2011	Bobde et al.	N/A	N/A
2012/0236456	12/2011	Yu	361/91.1	H05B 47/25
2012/0292636	12/2011	Zhang et al.	N/A	N/A
2013/0026493	12/2012	Cheng et al.	N/A	N/A
2013/0063846	12/2012	Pierco et al.	N/A	N/A
2013/0140616	12/2012	Schulze	257/296	H01L 27/0251
2013/0146971	12/2012	Hirler et al.	N/A	N/A
2013/0193454	12/2012	Bergenek	257/536	H01C 7/112
2013/0314833	12/2012	Smith et al.	N/A	N/A
2014/0111893	12/2013	Kato et al.	N/A	N/A
2014/0138737	12/2013	Bobde et al.	N/A	N/A
2014/0177113	12/2013	Gueorguiev et al.	N/A	N/A
2014/0268443	12/2013	Nassar et al.	N/A	N/A
2014/0332877	12/2013	Noebauer et al.	N/A	N/A
2014/0334522	12/2013	Meiser	374/178	H10N 19/00
2015/0021659	12/2014	Rountree	N/A	N/A
2015/0028351	12/2014	Van Brunt et al.	N/A	N/A

2015/0076521	12/2014	Tanaka et al.	N/A	N/A
2015/0084118	12/2014	Van Brunt et al.	N/A	N/A
2015/0084125	12/2014	Pala et al.	N/A	N/A
2015/0138678	12/2014	Parthasarathy et al.	N/A	N/A
2015/0162321	12/2014	Briere	N/A	N/A
2015/0364468	12/2014	Kiep	257/329	H01C 7/04
2016/0013639	12/2015	Willkofer	361/56	H03K 17/0828
2016/0043169	12/2015	Guan et al.	N/A	N/A
2016/0148925	12/2015	Tonazzo	257/361	H01L 27/0266
2016/0163689	12/2015	Laven et al.	N/A	N/A
2016/0181391	12/2015	Bobde et al.	N/A	N/A
2016/0247799	12/2015	Stafanov et al.	N/A	N/A
2016/0285255	12/2015	O'Donnell et al.	N/A	N/A
2017/0054360	12/2016	Uemura	N/A	N/A
2017/0149430	12/2016	Dupuy et al.	N/A	N/A
2017/0194438	12/2016	Kumagai et al.	N/A	N/A
2017/0200785	12/2016	Janssens	N/A	N/A
2017/0248646	12/2016	Mauder	N/A	G01R 31/3277
2017/0256938	12/2016	Fukuhara	N/A	N/A
2017/0338809	12/2016	Stefanov et al.	N/A	N/A
2017/0345891	12/2016	Van et al.	N/A	N/A
2017/0373491	12/2016	Schork et al.	N/A	N/A
2018/0114788	12/2017	Ahlers et al.	N/A	N/A
2018/0166994	12/2017	Dorn et al.	N/A	N/A
2018/0166999	12/2017	Pidutti	N/A	H01L 27/0676
2018/0269313	12/2017	Bina et al.	N/A	N/A
2018/0301553	12/2017	Weyers et al.	N/A	N/A
2018/0350797	12/2017	Lee et al.	N/A	N/A
2018/0366569	12/2017	Zeng et al.	N/A	N/A
2019/0067174	12/2018	Seok	N/A	N/A
2019/0067493	12/2018	Seok	N/A	N/A
2019/0131964	12/2018	Bryant	N/A	N/A
2019/0198666	12/2018	Kim et al.	N/A	N/A
2019/0287959	12/2018	Hua et al.	N/A	N/A
2019/0393334	12/2018	Weyers et al.	N/A	N/A
2020/0035669	12/2019	Tamaru et al.	N/A	N/A
2020/0169079	12/2019	Smith	N/A	N/A
2020/0212664	12/2019	Takuma et al.	N/A	N/A
2020/0335493	12/2019	Arnold et al.	N/A	N/A
2020/0343721	12/2019	Parthasarathy et al.	N/A	N/A
2020/0403397	12/2019	Nakagawa	N/A	H02H 5/041
2021/0193646	12/2020	Zeng et al.	N/A	N/A
2022/0044982	12/2021	Mongin	N/A	H01L 23/66
2022/0102487	12/2021	Siemieniec et al.	N/A	N/A

2022/0271156	12/2021	Peters	N/A	G01K 7/16

FOREIGN PATENT DOCUMENTS

Patent No.	Application Date	Country	CPC
0224274	12/1986	EP	N/A
0437939	12/1990	EP	N/A
0702455	12/1995	EP	N/A
1041634	12/1999	EP	H01L 27/0255
1063757	12/1999	EP	N/A
3419170	12/2017	EP	N/A
62229866	12/1986	JP	N/A
H11251594	12/1998	JP	N/A
2005175054	12/2004	JP	N/A
2006041441	12/2005	JP	N/A
2008172411	12/2007	JP	N/A
5272183	12/2012	JP	N/A
2014216465	12/2013	JP	N/A
2015103605	12/2014	JP	N/A
2015115608	12/2014	JP	N/A
2013161420	12/2012	WO	N/A

OTHER PUBLICATIONS

International Search Report and Written Opinion for International Patent Application No. PCT/US2020/036251, mailed Sep. 1, 2020, 14 pages. cited by applicant
“Japanese Office Action in Corresponding Patent Application No. 2021-576295, dated Mar. 10, 2023, 15 pages”. cited by applicant
“Translation of Japanese Office Action in Corresponding Patent Application No. 2023-172691, mailed Mar. 11, 25, 4 pages”. cited by applicant

---

Primary Examiner: Kayes; Sean

Assistant Examiner: Quddus; Nusrat

Attorney, Agent or Firm: Myers Bigel, P.A.

Background/Summary

CROSS-REFERENCE TO RELATED APPLICATION (1) The present application claims priority under 35 U.S.C. § 120 as a continuation of U.S. patent application Ser. No. 16/448,538, filed Jun. 21, 2019, the entire content of which is incorporated herein by reference as if set forth fully herein.

FIELD
(1) The present disclosure is related to transistor semiconductor die, and in particular to transistor semiconductor die with improved protection against short circuit events.
BACKGROUND
(2) Transistor devices such as metal-oxide semiconductor field-effect transistors (MOSFETs), insulated gate bipolar transistors (IGBTs), junction field-effect transistors (JFETs), and bipolar junction transistors (BJTs) are often used in power electronics, in which they may be used to selectively deliver current to and from a load. In certain situations, a load may provide a short

circuit across a transistor device. Such a short circuit event may cause the transistor device to fail.
(3) In recent years, there has been a push towards using wide bandgap semiconductor material systems for devices used in power electronics. For example, silicon carbide transistors are now in widespread use in power electronics. Compared to their silicon counterparts, silicon carbide transistors provide better performance, for example, by providing higher blocking voltage, lower on-state resistance, and lower switching loss. Silicon carbide transistors are also much smaller in size, and thus have higher current density. Accordingly, the short circuit withstand time, or the amount of time that a device can survive without failure during a short circuit event, of a silicon carbide transistor is much lower than that of a similar silicon device.
(4) In light of the above, there is a present need for silicon carbide transistor devices with improved short circuit protection.

SUMMARY

(5) In one embodiment, a transistor semiconductor die includes a first current terminal, a second current terminal, and a control terminal. A semiconductor structure is between the first current terminal, the second current terminal, and the control terminal and configured such that a resistance between the first current terminal and the second current terminal is based on a control signal provided at the control terminal. Short circuit protection circuitry is coupled between the control terminal and the second current terminal. In a normal mode of operation, the short circuit protection circuitry is configured to provide a voltage drop between the control terminal and the second current terminal that is greater than a voltage of the control signal. In a short circuit protection mode of operation, the short circuit protection circuitry is configured to provide a voltage drop between the control terminal and the second current terminal that is less than a voltage of the control signal. Accordingly, the short circuit protection circuit is configured to protect the transistor semiconductor die from failure due to a short circuit condition while not interfering with the operation of the transistor semiconductor die in a normal mode of operation.
(6) Those skilled in the art will appreciate the scope of the present disclosure and realize additional aspects thereof after reading the following detailed description of the preferred embodiments in association with the accompanying drawing figures.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

(1) The accompanying drawing figures incorporated in and forming a part of this specification illustrate several aspects of the disclosure, and together with the description serve to explain the principles of the disclosure.
(2) FIG. **1** is a schematic representation of a transistor semiconductor die according to one embodiment of the present disclosure.
(3) FIG. **2** is a schematic representation of a transistor semiconductor die according to one embodiment of the present disclosure.
(4) FIG. **3** is a graph illustrating a relationship between drain-source voltage, drain-source current, and gate-source voltage for a metal-oxide semiconductor field-effect transistor (MOSFET) according to one embodiment of the present disclosure.
(5) FIG. **4** is a cross-sectional view of a portion of a transistor semiconductor die according to one embodiment of the present disclosure.
(6) FIG. **5** is a cross-sectional view of a portion of a transistor semiconductor die according to one embodiment of the present disclosure.
(7) FIG. **6** is a schematic representation of a transistor semiconductor die according to one embodiment of the present disclosure.
(8) FIG. **7** is a cross-sectional view of a transistor semiconductor die according to one embodiment

of the present disclosure.
(9) FIG. **8** is a schematic representation of a transistor semiconductor die according to one embodiment of the present disclosure.
(10) FIG. **9** is a schematic representation of a transistor semiconductor die according to one embodiment of the present disclosure.
(11) FIG. **10** is a schematic representation of a transistor semiconductor die according to one embodiment of the present disclosure.
(12) FIG. **11** is a schematic representation of a transistor semiconductor die according to one embodiment of the present disclosure.

DETAILED DESCRIPTION

(13) The embodiments set forth below represent the necessary information to enable those skilled in the art to practice the embodiments and illustrate the best mode of practicing the embodiments. Upon reading the following description in light of the accompanying drawing figures, those skilled in the art will understand the concepts of the disclosure and will recognize applications of these concepts not particularly addressed herein. It should be understood that these concepts and applications fall within the scope of the disclosure and the accompanying claims.
(14) It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present disclosure. As used herein, the term “and/or” includes any and all combinations of one or more of the associated listed items.
(15) It will be understood that when an element such as a layer, region, or substrate is referred to as being “on” or extending “onto” another element, it can be directly on or extend directly onto the other element or intervening elements may also be present. In contrast, when an element is referred to as being “directly on” or extending “directly onto” another element, there are no intervening elements present. Likewise, it will be understood that when an element such as a layer, region, or substrate is referred to as being “over” or extending “over” another element, it can be directly over or extend directly over the other element or intervening elements may also be present. In contrast, when an element is referred to as being “directly over” or extending “directly over” another element, there are no intervening elements present. It will also be understood that when an element is referred to as being “connected” or “coupled” to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being “directly connected” or “directly coupled” to another element, there are no intervening elements present.
(16) Relative terms such as “below” or “above” or “upper” or “lower” or “horizontal” or “vertical” may be used herein to describe a relationship of one element, layer, or region to another element, layer, or region as illustrated in the Figures. It will be understood that these terms and those discussed above are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures.
(17) The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the disclosure. As used herein, the singular forms “a,” “an,” and “the” are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms “comprises,” “comprising,” “includes,” and/or “including” when used herein specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.
(18) Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further understood that terms used herein should be interpreted as

having a meaning that is consistent with their meaning in the context of this specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

(19) FIG. **1** shows a schematic representation of a transistor semiconductor die **10** according to one embodiment of the present disclosure. The transistor semiconductor die **10** includes a first current terminal **12**, a second current terminal **14**, and a control terminal **16**. A semiconductor structure between the first current terminal **12**, the second current terminal **14**, and the control terminal **16** forms a transistor device Q.sub.ig such that a resistance between the first current terminal **12** and the second current terminal **14** is based on a control signal CNT provided at the control terminal **16**. As shown in FIG. **1**, the transistor device Q.sub.ig is a metal-oxide semiconductor field-effect transistor (MOSFET). Accordingly, the first current terminal **12** is a drain terminal, the second current terminal **14** is a source terminal, and the control terminal **16** is a gate terminal. However, the principles of the present disclosure apply equally to any transistor device such as an insulated gate bipolar transistor (IGBT). In the case of an IGBT, the first current terminal **12** is a collector terminal, the second current terminal **14** is an emitter terminal, and the control terminal **16** is a gate terminal. Since the transistor device Q.sub.ig may be used for power electronics, a freewheeling anti-parallel diode D.sub.fw may be coupled in anti-parallel with the transistor device Q.sub.ig so that current can be conducted bidirectionally between the first current terminal **12** and the second current terminal **14**. In various embodiments, the freewheeling diode D.sub.fw may be external from the transistor device Q.sub.ig, or may be internal to the transistor device Q.sub.ig, e.g., a body diode.

(20) While the transistor device Q.sub.ig is shown herein as an insulated gate device, the principles of the present disclosure apply equally to any transistor device such as bipolar junction transistors (BJTs), and junction field-effect transistors (JFETs). In the case of a BJT, the first current terminal **12** is a collector terminal, the second current terminal **14** is an emitter terminal, and the control terminal **16** is a base terminal. In the case of a JFET, the first current terminal **12** is a drain terminal, the second current terminal **14** is a source terminal, and the control terminal **16** is a gate terminal. Further, the transistor device Q.sub.ig may be a thyristor. In the case of a thyristor, the first current terminal **12** is an anode, the second current terminal **14** is a cathode, and the control terminal **16** is a gate terminal.

(21) The transistor semiconductor die **10** may utilize a wide bandgap material system such as silicon carbide. As discussed above, the silicon carbide transistor semiconductor die **10** may be more sensitive to short circuit events than their silicon counterparts due to the smaller size and higher current density thereof. Accordingly, short circuit protection circuitry **18** is coupled between the control terminal **16** and the second current terminal **14**. The short circuit protection circuitry **18** is configured to operate in a normal mode of operation and a short circuit protection mode of operation. In the normal mode of operation, the short circuit protection circuitry **18** is configured to provide a voltage drop between the control terminal **16** and the second current terminal **14** that is greater than a voltage of the control signal CNT. In the short circuit protection mode of operation, the short circuit protection circuitry **18** is configured to provide a voltage drop between the control terminal **16** and the second current terminal **14** that is less than a voltage of the control signal CNT. In the normal mode of operation when a voltage drop across the short circuit protection circuitry **18** is greater than a voltage of the control signal CNT, the operation of the transistor device Q.sub.ig is relatively unaffected. In the short circuit protection mode of operation when a voltage drop across the short circuit protection circuitry **18** is less than a voltage of the control signal CNT, a voltage at the control terminal **16** is lowered such that voltage between the control terminal **16** and the second current terminal **14** (i.e., the gate-to-source voltage of the transistor device Q.sub.ig) is reduced, which in turn partially or completely shuts off the device. Shutting off the transistor device Q.sub.ig protects the device during a short circuit event in order to prevent a failure.

(22) One way in which the above-mentioned functionality may be accomplished is by providing the

short circuit protection circuitry **18** such that it has a negative temperature coefficient with respect to a voltage drop across the short circuit protection circuitry **18**. In other words, the short circuit protection circuitry **18** may be provided such that a voltage drop across the short circuit protection circuitry **18** decreases as temperature increases. Since during a short circuit event a temperature of the transistor semiconductor die **10** will rapidly increase far above normal operating temperatures thereof, the short circuit protection circuitry **18** may significantly reduce a voltage drop between the control terminal **16** and the second current terminal **14** only when a short circuit event occurs. Note that this functionality requires adequate thermal coupling between the short circuit protection circuitry **18** and the current carrying portion of the transistor semiconductor die **10**.

(23) Notably, the short circuit protection circuitry **18** is located on the transistor semiconductor die **10**. As discussed in detail below, the short circuit protection circuitry **18** takes up minimal area on the transistor semiconductor die **10** and may be capable of extending a short circuit withstand time of the transistor semiconductor die **10** significantly, and in some cases indefinitely.

(24) FIG. **2** is a schematic representation of the transistor semiconductor die **10** showing details of the short circuit protection circuitry **18** according to one embodiment of the present disclosure. As shown in FIG. **2**, the short circuit protection circuitry **18** may include a number of short circuit protection diodes D.sub.sc coupled in series between the control terminal **16** and the second current terminal **14**. In particular, the short circuit protection diodes D.sub.sc are coupled anode-to-cathode between the control terminal **16** and the second current terminal **14** such that an anode of a first one of the short circuit protection diodes D.sub.sc is coupled to the control terminal **16** and a cathode of a last one of the short circuit protection diodes D.sub.sc is coupled to the second current terminal **14**. As discussed above, the short circuit protection diodes D.sub.sc may be provided with a negative temperature coefficient (e.g., an exponential negative temperature coefficient) with respect to a forward voltage drop thereof. In other words, the short circuit protection diodes D.sub.sc may be provided such that a forward voltage drop across the diodes decreases as temperature increases. Such a negative temperature coefficient is naturally present in silicon carbide diodes. The negative temperature coefficient enables a voltage drop across the short circuit protection diodes D.sub.sc to be greater than a voltage of the control signal CNT in the normal mode of operation (and thus not interfere with the operation of the transistor device Q.sub.ig) and be less than a voltage of the control signal CNT in the short circuit protection mode of operation (thus partially or completely turning off the transistor device Q.sub.ig). Note that this functionality requires adequate thermal coupling between the short circuit protection circuitry **18** and the current carrying portion of the transistor semiconductor die **10**. The number of short circuit protection diodes D.sub.sc may be chosen such that when a temperature of the transistor semiconductor die **10** is below a short circuit threshold temperature a voltage drop across the short circuit protection diodes D.sub.sc is greater than or equal to a voltage of the control signal CNT and when a temperature of the transistor semiconductor die **10** is above the short circuit threshold temperature a voltage drop across the short circuit protection diodes D.sub.sc is significantly less than the voltage of the control signal CNT such that a voltage at the control terminal **16** is lowered enough to partially or completely turn off the transistor device Q.sub.ig.

(25) In addition to protecting the transistor device Q.sub.ig against short circuit events, the short circuit protection circuitry **18** also clamps the maximum voltage of the gate to the combined forward voltage drop of the short circuit protection diodes D.sub.sc. This has the additional benefits of protecting the transistor device Q.sub.ig against electrostatic discharge (ESD) and provides voltage overshoot protection for the gate of the transistor device Q.sub.ig.

(26) The short circuit protection circuitry **18** may enable significant improvements in the short circuit withstand time of the transistor semiconductor die **10**. As discussed herein, the short circuit protection circuitry **18** may require minimal active area on the transistor semiconductor die **10**. In various embodiments, an on-state resistance of the transistor semiconductor die **10** may be between 0.1 mΩ/cm.sup.2 and 3.0 mΩ/cm.sup.2, a blocking voltage of the transistor semiconductor die **10**

may be between 600V and 10 kV, and a short circuit withstand time of the transistor semiconductor die **10** may be greater than 3 μs. Notably, the on-state resistance of the transistor semiconductor die **10** may fall anywhere in the above range, such as between 0.5 mΩ/cm.sup.2 and 3.0 mΩ/cm.sup.2, between 1.0 mΩ/cm.sup.2 and 3.0 mΩ/cm.sup.2, between 1.5 mΩ/cm.sup.2 and 3.0 mΩ/cm.sup.2, between 2.0 mΩ/cm.sup.2 and 3.0 mΩ/cm.sup.2, between 2.5 mΩ/cm.sup.2 and 3.0 mΩ/cm.sup.2, and the like. The blocking voltage of the transistor semiconductor die **10** may similarly fall anywhere inside the above range, such as between 600V and 1 kV, between 600V and 2 kV, between 600V and 5 kV, between 1 kV and 5 kV, between 5 kV and 10 kV, and the like. A relationship between the on-state resistance and the blocking voltage of the transistor semiconductor die **10** may be expressed according to Equation (1):

$$R_{on} = 0.8 \times (3 \times 10^{-8}) \times V_{block}^{2.4} \quad (1)$$

where R.sub.on is the on-state resistance of the transistor semiconductor die and V.sub.block is the blocking voltage of the transistor semiconductor die **10**.

(27) The short circuit withstand time of the transistor semiconductor die **10** may be less than 10 s in some embodiments, but the principles of the present disclosure may also enable the transistor semiconductor die **10** to indefinitely withstand a short circuit event in some circumstances. The short circuit withstand time of the transistor semiconductor die **10** may fall anywhere in the above ranges such that the short circuit withstand time is between 4 μs and 10 s, between 5 μs and 10 s, between 10 μs and 10 s, between 50 μs and 10 s, between 5 ms and 10 s, between 10 ms and 10 s, between 50 ms and 10 s, between is and 10 s, and the like.

(28) FIG. **3** is a graph illustrating a relationship between drain-source voltage, drain-source current, and gate-source voltage in a MOSFET. As shown, a relationship between drain-source voltage and drain-source current is dependent on gate-source voltage such that as the gate-source voltage increases, a steepness of the curve between drain-source voltage and drain-source current increases. Accordingly, higher gate-source voltages will lead to higher drain-source currents during a short circuit event. When a drain-source current becomes high enough, the device will fail. By reducing the gate-source voltage during a short circuit event, the drain-source current is significantly reduced such that a failure of the device can be prevented.

(29) FIG. **4** is a cross-sectional view of a portion of the transistor semiconductor die **10** according to one embodiment of the present disclosure. The transistor semiconductor die **10** includes a substrate **20**, a drift layer **22** on the substrate **20**, a number of implants **24** in the drift layer **22**, a top metallization layer **26**, and a bottom metallization layer **28**. In particular, on the right side of the transistor semiconductor die **10** the transistor device Q.sub.ig is provided as a vertical MOSFET including a pair of junction implants **30** in the drift layer **22** such that the junction implants **30** are separated by a JFET gap **32**. A gate contact **34** on top of a gate oxide layer **36** runs between the junction implants **30** on a surface of the drift layer **22** opposite the substrate **20**. A source contact **38** (which may also be the second current terminal **14**) also contacts each one of the junction implants **30** on the surface of the drift layer **22** opposite the substrate. A drain contact **40** (which may also be the first current terminal **12**) is on the substrate **20** opposite the drift layer **22**. The source contact **38** is provided by a portion of the top metallization layer **26**. The drain contact **40** is provided by the bottom metallization layer **28**.

(30) On the left side of the transistor semiconductor die **10**, the control terminal **16** is provided by a portion of the top metallization layer **26**. While not shown, the control terminal **16** is coupled to the gate contact **34** of the transistor device Q.sub.ig on a plane not shown in the cross-section (e.g., via a gate runner **42** provided on a field oxide layer **44** below the top metallization layer **26**). The control terminal **16** is also coupled to the source contact **38** of the transistor device Q.sub.ig through a number of P-N junctions **46** formed in the drift layer **22**. Each one of these P-N junctions **46** forms one of the short circuit protection diodes D.sub.sc discussed above with respect to FIG. **2**. The top metallization layer **26** is appropriately patterned to form connections between the control terminal **16** and the source contact **38** through the P-N junctions **46** as shown. An intermetal

dielectric layer **48** may insulate different portions of the top metallization layer **26** to form the desired connection pattern.

(31) While only one unit cell of the transistor device Q.sub.ig is shown in FIG. **4**, the transistor device Q.sub.ig may comprise any number of cells coupled together to provide a desired forward current rating of the transistor semiconductor die **10**. Further, while the short circuit protection diodes D.sub.sc are shown one next to another in the drift layer **22** in FIG. **4**, the short circuit protection diodes D.sub.sc may be distributed in any suitable manner in the transistor semiconductor die **10**. For example, the short circuit protection diodes D.sub.sc may be distributed between different cells of the transistor device Q.sub.ig in a pattern in order to reduce the total active area devoted to the short circuit protection diodes D.sub.sc. In general, the short circuit protection diodes D.sub.sc will consume very little area when compared to the transistor device Q.sub.ig and thus will have a minimal impact on the total active area of the transistor semiconductor die **10**.

(32) FIG. **5** shows the transistor semiconductor die **10** according to an additional embodiment of the present disclosure. The transistor semiconductor die **10** shown in FIG. **5** is substantially similar to that shown in FIG. **4**, except that the short circuit protection diodes D.sub.sc are provided as a number of P-N junctions **50** formed in an additional semiconductor layer **52** (e.g., a polysilicon layer) that is provided on the drift layer **22** (with the field oxide layer **44** between the additional semiconductor layer **52** and the drift layer **22** to avoid interaction between the layers). A number of metal jumpers **53** may be provided between each adjacent P-N junction **50**. In the embodiment shown in FIG. **5** the short circuit protection diodes D.sub.sc may be Zener diodes. In such an embodiment, the short circuit protection diodes D.sub.sc are coupled in series cathode-to-anode between the insulted gate terminal **16** and the second current terminal **14** such that a cathode of a first one of the short circuit protection diodes D.sub.sc is coupled to the control terminal **16** and an anode of a last one of the short circuit protection diodes D.sub.sc is coupled to the second current terminal **14**. However, the P-N junctions **50** in FIG. **5** may be reversed such that they are coupled anode-to-cathode between the insulated gate terminal **16** and the second current terminal **14** as shown. Providing the short circuit protection diodes D.sub.sc in the additional semiconductor layer **52** that is provided on the drift layer **22** may allow a reduction or elimination of the active area devoted to the short circuit protection circuitry **18**, since the short circuit protection diodes D.sub.sc can be moved over the transistor device Q.sub.ig in some embodiments.

(33) FIG. **6** is a schematic representation of the transistor semiconductor die **10** according to an additional embodiment of the present disclosure. The transistor semiconductor die **10** shown in FIG. **6** is substantially similar to that shown in FIG. **2**, except that the short circuit protection circuitry **18** further includes a short circuit protection resistive element R.sub.sc coupled in series with the short circuit protection diodes D.sub.sc. The short circuit protection resistive element R.sub.sc may be used to achieve a precise voltage drop across the short circuit protection circuitry **18** that may be difficult to achieve using diodes alone. Since using only diodes in the short circuit protection circuitry **18** effectively limits the total voltage drop across the short circuit protection circuitry **18** to integer multiples of the forward voltage drop of the diodes, providing the short circuit protection resistive element R.sub.sc allows for more precise tuning of the voltage drop across the short circuit protection circuitry **18**. The short circuit protection circuitry **18** may be provided with a negative temperature coefficient with respect to the resistance thereof, such that as the temperature of the transistor semiconductor die **10** increases, the resistance of the short circuit protection resistive element R.sub.sc decreases.

(34) FIG. **7** is a cross-sectional view of a portion of the transistor semiconductor die **10** according to an additional embodiment of the present disclosure. The transistor semiconductor die **10** shown in FIG. **7** is substantially similar to that shown in FIG. **4**, except that the transistor semiconductor die **10** further includes the short circuit protection resistive element R.sub.sc coupled between the control terminal **16** and the second current terminal **14**. The short circuit protection resistive

element R.sub.sc may be implemented using a deep N-doped well **54**. Providing the short circuit protection resistive element R.sub.sc in this manner may ensure a negative temperature coefficient with respect to resistance. While not shown, in other embodiments, the short circuit protection resistive element R.sub.sc may be implemented using a highly doped polysilicon resistor, a metal resistor with sufficiently high positive temperature coefficient with respect to resistance, or any other suitable type of resistive element.

(35) FIG. **8** is a schematic representation of the transistor semiconductor die **10** according to an additional embodiment of the present disclosure. The transistor semiconductor die **10** shown in FIG. **8** is substantially similar to that shown in FIG. **1**, except that the transistor semiconductor die **10** further includes a gate resistive element R.sub.g coupled between the control terminal **16** and a gate of the transistor device Q.sub.ig. The gate resistive element R.sub.g is provided with a positive temperature coefficient with respect to a resistance thereof In other words, a resistance of the gate resistive element R.sub.g increases as a temperature of the transistor semiconductor die **10** increases. Note that this functionality requires adequate thermal coupling between the short circuit protection circuitry **18** and the current carrying portion of the transistor semiconductor die **10**. This may reduce a gate drive current in the event of a short circuit event, thereby enhancing the action of the short circuit protection circuitry **18**.

(36) As discussed above, while the foregoing examples of transistor semiconductor die **10** are primarily shown depicting the transistor device Q.sub.ig as a MOSFET, the principles of the present disclosure apply equally to any type of transistor devices including IGBTs, BJTs, JFETs, and the like. Accordingly, for the sake of completeness FIG. **9** shows a schematic view of the transistor semiconductor die **10** wherein the transistor device Q.sub.ig is an IGBT instead of a MOSFET. In this case, the first current terminal **12** is a collector terminal and the second current terminal **14** is an emitter terminal. Those skilled in the art will readily appreciate that the MOSFET depicted in the cross-sectional views of the transistor semiconductor die **10** shown above can be readily replaced with an IGBT, for example, by adding an injector layer between the substrate **20** and the drift layer **22**. FIG. **10** shows a schematic view of the transistor semiconductor die **10** wherein the transistor device Q.sub.ig is a BJT instead of a MOSFET. In this case, the first current terminal **12** is a collector terminal, the second current terminal **14** is an emitter terminal, and the control terminal **14** is a base terminal. Those skilled in the art will readily appreciate that the MOSFET depicted in the cross-sectional views of the transistor semiconductor die **10** shown above can be readily replaced with a BJT. FIG. **11** shows a schematic view the transistor semiconductor die **10** wherein the transistor device Q.sub.ig is a JFET instead of a MOSFET. In this case, the first current terminal **12** is a drain terminal, the second current terminal **14** is a source terminal, and the control terminal **16** is a gate terminal. Those skilled in the art will readily appreciate that the MOSFET depicted in the cross-sectional views of the transistor semiconductor die **10** shown above can be readily replaced with a JFET.

(37) Those skilled in the art will recognize improvements and modifications to the preferred embodiments of the present disclosure. All such improvements and modifications are considered within the scope of the concepts disclosed herein and the claims that follow.

Claims

1. A transistor semiconductor die comprising: a first current terminal and a second current terminal; a control terminal; a semiconductor structure between the first current terminal and the second current terminal; and short circuit protection circuitry comprising at least a first diode coupled in series between the control terminal and the second current terminal, wherein the first diode has a negative temperature coefficient with respect to a voltage drop across the first diode so that the first diode turns on in a short circuit protection mode of operation, wherein the short circuit protection circuitry is configured to operate in the short circuit protection mode of operation in response to a

temperature of the transistor semiconductor die exceeding a short circuit threshold temperature.
2. The transistor semiconductor die of claim 1, wherein the short circuit protection circuitry is configured to: in a normal mode of operation, provide a voltage drop between the control terminal and the second current terminal that is greater than a voltage of a control signal provided at the control terminal; and in the short circuit protection mode of operation, provide a voltage drop between the control terminal and the second current terminal that is less than a voltage of the control signal.
3. The transistor semiconductor die of claim 2, further comprising a resistive element coupled between the control terminal and a gate of a semiconductor device implemented in the transistor semiconductor die, wherein the resistive element has a negative temperature coefficient with respect to a resistance thereof.
4. The transistor semiconductor die of claim 2, wherein the semiconductor structure comprises a drift layer, and wherein the first diode resides within the drift layer.
5. The transistor semiconductor die of claim 2, wherein the first diode is provided in an additional semiconductor layer on the semiconductor structure.
6. The transistor semiconductor die of claim 1, wherein the short circuit protection circuitry further comprises a second diode, wherein the first and second diodes are coupled in series, and wherein an anode of the first diode is coupled to the control terminal and a cathode of the second diode is coupled to the second current terminal.
7. The transistor semiconductor die of claim 1, wherein the short circuit protection circuitry is configured to reduce a voltage drop between the control terminal and the second current terminal in response to the first diode turning on.
8. The transistor semiconductor die of claim 2, wherein: the short circuit protection circuitry is configured to operate in the normal mode of operation when the temperature of the transistor semiconductor die is below the short circuit threshold temperature.
9. The transistor semiconductor die of claim 1, wherein the semiconductor structure comprises silicon carbide.
10. A transistor semiconductor die comprising: a first current terminal and a second current terminal; a control terminal; a semiconductor structure between the first current terminal and the second current terminal; a gate resistive element coupled between the control terminal and a gate of the transistor semiconductor die, wherein the gate resistive element has a positive temperature coefficient with respect to a resistance thereof; and short circuit protection circuitry comprising a plurality of diodes coupled in series between the control terminal and the second current terminal.
11. The transistor semiconductor die of claim 10, wherein at least one of the plurality of diodes has a negative temperature coefficient with respect to a voltage drop across the at least one of the plurality of diodes.
12. The transistor semiconductor die of claim 10, wherein the gate resistive element is thermally coupled to a current carrying portion of the transistor semiconductor die.
13. A transistor semiconductor die comprising: a first current terminal and a second current terminal; a control terminal; a semiconductor structure between the first current terminal and the second current terminal, the semiconductor structure comprising a first conductivity type well region; and short circuit protection circuitry comprising one or more diodes and a resistive element coupled in series between the control terminal and the second current terminal, wherein the resistive element comprises a second conductivity type semiconductor region in the first conductivity type well region.
14. The transistor semiconductor die of claim 13, wherein at least one of the one or more diodes has a negative temperature coefficient with respect to a voltage drop across the one or more diodes.
15. The transistor semiconductor die of claim 14, wherein: the transistor semiconductor die is configured to operate in a normal mode of operation when a temperature of the semiconductor structure is below a short circuit threshold temperature; and the transistor semiconductor die is

configured to operate in a short circuit protection mode of operation when a temperature of the semiconductor structure is above the short circuit threshold temperature.
16. The transistor semiconductor die of claim 13, wherein the resistive element has a negative temperature coefficient with respect to a resistance thereof.
17. The transistor semiconductor die of claim 1, wherein an on-state resistance of the transistor semiconductor die is less than 3.0 mΩ/cm.sup.2, a blocking voltage of the transistor semiconductor die is greater than 600V, and a short circuit withstand time of the transistor semiconductor die is greater than 3 μs.
18. The transistor semiconductor die of claim 17, wherein the on-state resistance of the transistor semiconductor die is greater than 0.1 mΩ/cm.sup.2, the blocking voltage of the transistor semiconductor die is less than 10 kV, and a short circuit withstand time of the transistor semiconductor die is less than 10 s.
19. The transistor semiconductor die of claim 13, wherein the semiconductor structure comprises a drift layer, and wherein the one or more diodes reside within the drift layer.
20. The transistor semiconductor die of claim 13, wherein the semiconductor structure comprises silicon carbide.
21. A transistor semiconductor die comprising: a first current terminal and a second current terminal; a control terminal; a semiconductor structure between the first current terminal and the second current terminal; and protection circuitry comprising a plurality of protection elements that comprise at least a first diode coupled between the control terminal and the second current terminal, wherein the first diode has a negative temperature coefficient with respect to a voltage drop across the first diode so that the protection circuitry at least partially shuts off the semiconductor structure in a protection event, wherein, in the protection event, the protection circuitry is configured to clamp a voltage provided at a gate of a semiconductor device implemented in the transistor semiconductor die to a combined forward voltage drop of the plurality of protection elements.
22. The transistor semiconductor die of claim 1, wherein the transistor semiconductor die is configured to at least partially turn off in response to the first diode turning on.
23. The transistor semiconductor die of claim 21, wherein the first diode is configured to turn on in the protection event.
24. The transistor semiconductor die of claim 21, wherein the protection circuitry is configured to reduce a voltage drop between the control terminal and the second current terminal in the protection event.
25. The transistor semiconductor die of claim 21, wherein the protection event is a short circuit condition between the first current terminal and the second current terminal.
26. The transistor semiconductor die of claim 21, wherein the protection circuitry is configured to at least partially shut off the semiconductor structure in the protection event in response to a temperature of the transistor semiconductor die exceeding a threshold value.