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SEMICONDUCTOR DEVICE

Abstract

A semiconductor device includes a substrate including a fin-type active area and a device separation layer configured to cover both sidewalls of the fin-type active area, a pair of nanosheet stacks each including a lower nanosheet stack arranged on the fin-type active area and an upper nanosheet stack arranged on the lower nanosheet stack, an intermediate insulating layer arranged between the lower nanosheet stack and the upper nanosheet stack, a nanosheet separation wall arranged between each of the pair of nanosheet stacks and extending in a first horizontal direction, and a pair of gate lines extending on the pair of nanosheet stacks in a second horizontal direction, wherein the nanosheet separation wall separates respective lower nanosheet stacks in the pair of nanosheet stacks from each other in the second horizontal direction.

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority under 35 U.S.C. § 119 to Korean Patent Application No. 10-2024-0019835, filed on Feb. 8, 2024, in the Korean Intellectual Property office, the entirety of which is incorporated by reference herein.

BACKGROUND

[0002] Due to the development of electronic technology, the demand for high integration of semiconductor devices is increasing and downscaling of the semiconductor devices is proceeding. Down-scaling of the semiconductor devices may cause a short channel effect of transistors, which reduces the reliability of integrated circuit devices. To reduce the short channel effect, a semiconductor device of a multi-gate structure such as a nanosheet-type transistor has been proposed.

SUMMARY

[0003] Some aspects of this disclosure provide semiconductor devices with improved operation characteristics.

[0004] According to some implementations of the present disclosure, there is provided a semiconductor device including a substrate including a fin-type active area and a device separation layer configured to cover both sidewalls of the fin-type active area, a pair of nanosheet stacks each including a lower nanosheet stack arranged on the fin-type active area and an upper nanosheet stack arranged on the lower nanosheet stack, an intermediate insulating layer arranged between the lower nanosheet stack and the upper nanosheet stack, a nanosheet separation wall arranged between each of the pair of nanosheet stacks and extending in a first horizontal direction, and a pair of gate lines extending on the pair of nanosheet stacks in a second horizontal direction, wherein the nanosheet separation wall separates respective lower nanosheet stacks in the pair of nanosheet stacks from each other in the second horizontal direction.

[0005] According to some implementations of the present disclosure, there is provided a semiconductor device including a substrate including a fin-type active area and a device separation layer configured to cover both sidewalls of the fin-type active area, a pair of nanosheet stacks each including a lower nanosheet stack arranged on the fin-type active area and an upper nanosheet stack arranged on the lower nanosheet stack, an intermediate insulating layer arranged between the lower nanosheet stack and the upper nanosheet stack, a nanosheet separation wall arranged between the pair of nanosheet stacks and extending in a first horizontal direction, a gate separation spacer arranged on one sidewall relatively distant in a second horizontal direction from the nanosheet separation wall, among both sidewalls of each of the upper nanosheet stacks respectively included in the pair of nanosheet stacks, and a pair of gate lines extending on the pair of nanosheet stacks in the second horizontal direction, wherein the nanosheet separation wall separates lower nanosheet stacks each included in the pair of nanosheet stacks from each other in the second horizontal direction.

[0006] According to some implementations of the present disclosure, there is provided a semiconductor device including a substrate including a fin-type active area and a device separation layer configured to cover both sidewalls of the fin-type active area and arranged in a device separation trench, a pair of nanosheet stacks each including a lower nanosheet stack arranged on the fin-type active area and an upper nanosheet stack arranged on the lower nanosheet stack, an

intermediate insulating layer arranged between the lower nanosheet stack and the upper nanosheet stack, a nanosheet separation wall arranged between the one pair of nanosheet stacks and extending in a first horizontal direction, a residual insulating material arranged on lower end edges of both sidewalls of the device separation trench adjacent to the pair of nanosheet stacks in a second horizontal direction, a gate separation spacer arranged on one sidewall relatively distant in the second horizontal direction from the nanosheet separation wall, among both sidewalls of each of the upper nanosheet stacks respectively included in the pair of nanosheet stacks, a pair of gate lines extending on the pair of nanosheet stacks in the second horizontal direction, and including a first metal layer, a second metal layer, and a third metal layer, and a gate cut structure including a first gate cut structure configured to separate the upper nanosheet stacks each included in the pair of nano sheet stacks from each other in the second horizontal direction, and a second gate cut structure configured to separate another pair of nanosheet stacks adjacent to the pair of nanosheet stacks from the pair of nanosheet stacks in the second horizontal direction, wherein the nanosheet separation wall separates the lower nanosheet stacks respectively included in the pair of nanosheet stacks from each other in the second horizontal direction, and the third metal layer includes a lower gate metal layer and an upper gate metal layer, which are apart from each other by the gate separation spacer.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The foregoing and other implementations will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[0008] FIG. **1** is a schematic top view of an example of a semiconductor device according to some implementations;

[0009] FIG. **2**A is a cross-sectional view of the semiconductor device taken along line X**1**-X**1**′ in FIG. **1**;

[0010] FIG. **2**B is a cross-sectional view of the semiconductor device taken along line Y**1**-Y**1**′ in FIG. **1**;

[0011] FIG. **3** is a cross-sectional view of an example of a semiconductor device according to some implementations;

[0012] FIG. **4** is a cross-sectional view of an example of a semiconductor device according to some implementations; and

[0013] FIGS. **5**A-**26**D are cross-sectional views illustrating an example of a manufacturing method of a semiconductor device, according to some implementations.

DETAILED DESCRIPTION

[0014] Hereinafter, examples are described in detail with reference to the accompanying drawings. Identical reference numerals are used for the same constituent elements in the drawings, and duplicate descriptions thereof are omitted.

[0015] FIG. **1** is a schematic top view of a semiconductor device **100** according to some implementations. FIG. **2**A is a cross-sectional view of the semiconductor device **100** taken along line X**1**-X**1**′ in FIG. **1**. FIG. **2**B is a cross-sectional view of the semiconductor device **100** taken along line Y**1**-Y**1**′ in FIG. **1**.

[0016] Referring to FIGS. **1**, **2**A, and **2**B, the semiconductor device **100** may include a substrate **102** having a fin-type active area FA, a plurality of gate lines GL, a plurality of nanosheet stacks NSS, and a plurality of nanosheet separation walls **122**.

[0017] The semiconductor device **100** may include a plurality of logic cells. The plurality of logic cells may each include a plurality of circuit elements, such as a transistor and a register, and may be variously configured. The logic cell may constitute, for example, an AND gate, a NAND gate, an

OR gate, a NOR gate, an exclusive OR (XOR) gate, an exclusive NOR (XNOR) gate, an inverter (INV), an adder (ADD), a buffer (BUF), a delay (DLY), a filter (FIL), a multiplexer (MXT/MXIT), an OR/AND INV (OAI), an AND/OR (AO) INV (AOI), a D flip-flop, a reset flip-flop, a master-slave flip-flop, a latch, and/or the like, and may constitute a standard cell performing a logic function.

[0018] The substrate **102** may include a Group IV semiconductor, such as silicon (Si) and germanium (Ge), a Group IV-IV compound semiconductor, such as silicon-germanium (SiGe) and silicon carbide (SiC), or a Group III-V semiconductor, such as gallium arsenide (GaAs), indium arsenide (InAs), and indium phosphide (InP). The terms “SiGe”, “SiC”, “GaAs”, “InAs”, and “InP” and the like used herein refer to materials including the elements included in each term, but do not represent a stoichiometric relationship. The substrate **102** may include a conductive area, for example, a well doped with impurities, or a structure doped with impurities.

[0019] A device separation layer **112** may be formed in a device separation layer trench **112**T formed in the substrate **102**. The device separation layer **112** may cover both sidewalls of the fin-type active area FA. The device separation layer **112** may include, for example, an oxide layer, a nitride layer, or a combination thereof. A residual insulating material **124** may be arranged at a lower edge of both sidewalls of the device separation layer trench **112**T adjacent to the nanosheet stack NSS in a second horizontal direction (Y direction). The residual insulating material **124** may include a material which has not been removed and remains during a forming process of the nanosheet separation wall **122** to be described below with reference to FIGS. **5**A, **5**B, **6**A, and **6**B. Accordingly, the residual insulating material **124** may substantially include the same material as the nanosheet separation wall **122**.

[0020] The fin-type active area FA may protrude from an upper surface of the substrate **102** in a vertical direction (Z direction). The fin-type active areas FA may extend in parallel with each other in a first horizontal direction (X direction).

[0021] The plurality of gate lines GL may extend in parallel with each other on the fin-type active area FA in the second horizontal direction (Y direction). The plurality of nanosheet stacks NSS may be arranged in areas, where the fin-type active area FA and the plurality of gate lines GL cross each other, on the fin-type active area FA. The plurality of nanosheet stacks NSS may be arranged to form rows and columns in the first horizontal direction (X direction) and the second horizontal direction (Y direction).

[0022] Each of the plurality of nanosheet stacks NSS may include a lower nanosheet stack NSSb arranged on the fin-type active area FA, and an upper nanosheet stack NSSt arranged on the lower nanosheet stack NSSb. The lower nanosheet stack NSSb may include a first nanosheet Nb**1** and a second nanosheet Nb**2**, which are sequentially stacked on the fin-type active area FA, and the upper nanosheet stack NSSt may include a third nanosheet Nt**1** and a fourth nanosheet Nt**2**, which are sequentially stacked on the lower nanosheet stack NSSb. The first nanosheet Nb**1**, the second nanosheet Nb**2**, the third nanosheet Nt**1**, and the fourth nanosheet Nt**2** may each include a Group IV semiconductor, such as Si and Ge, a Group IV-IV compound semiconductor, such as SiGe and SiC, or a Group III-V compound semiconductor, such as GaAs, InAs, and InP. Each of the first nanosheet Nb**1**, the second nanosheet Nb**2**, the third nanosheet Nt**1**, and the fourth nanosheet Nt**2** may have a channel area (not illustrated). In some implementations, the first nanosheet Nb**1**, the second nanosheet Nb**2**, the third nanosheet Nt**1**, and the fourth nanosheet Nt**2** have substantially the same thickness in the vertical direction (Z direction). In some implementations, at least some of the first nanosheet Nb**1**, the second nanosheet Nb**2**, the third nanosheet Nt**1**, and the fourth nanosheet Nt**2** have different thicknesses in the vertical direction (Z direction).

[0023] In FIGS. **2**A and **2**B, each of the lower nanosheet stack NSSb and the upper nanosheet stack NSSt is illustrated to include two nanosheets, but the number of nanosheets is not limited thereto. For example, each of the lower nanosheet stack NSSb and the upper nanosheet stack NSSt may include one, three, or more than three nanosheets.

[0024] In some implementations, each of the first nanosheet Nb**1**, the second nanosheet Nb**2**, the third nanosheet Nt**1**, and the fourth nanosheet Nt**2**, which are included in each of the lower nanosheet stack NSSb and the upper nanosheet stack NSSt, have the same size in the first horizontal direction (X direction). In some implementations, at least some of the first nanosheet Nb**1**, the second nanosheet Nb**2**, the third nanosheet Nt**1**, and the fourth nanosheet Nt**2**, which are included in each of the lower nanosheet stack NSSb and the upper nanosheet stack NSSt, have different sizes from each other in the first horizontal direction (X direction). For example, in the first horizontal direction (X direction), a length of each of the first nanosheet Nb**1** and the second nanosheet Nb**2**, which are relatively close to an upper surface of the fin-type active area FA, among the first nanosheet Nb**1**, the second nanosheet Nb**2**, the third nanosheet Nt**1**, and the fourth nanosheet Nt**2** may be less than a length of the third nanosheet Nt**1** and the fourth nanosheet Nt**2**, which are relatively far from the upper surface of the fin-type active area FA.
[0025] An intermediate insulating layer MDI may be arranged between the lower nanosheet stack NSSb and the upper nanosheet stack NSSt. The intermediate insulating layer MDI may include an insulating material.
[0026] The plurality of nanosheet separation walls **122** may extend in parallel with each other in the first horizontal direction (X direction). Each of a plurality of nanosheet separation walls **122** may protrude from the upper surface of the substrate **102** in the vertical direction (Z direction). Both sidewalls of the nanosheet separation wall **122** may be in contact with the fin-type active area FA, the lower nanosheet stack NSS, and the intermediate insulating layer MDI. A pair of nanosheet stacks NSS facing each other in the second horizontal direction (Y direction) may be arranged spaced apart from each other with one nanosheet separation wall **122** therebetween in the second horizontal direction (Y direction). In some implementations, a lower surface of the nanosheet separation wall **122** is at the same vertical level as the upper surface of the substrate **102**. In some implementations, the upper surface of the nanosheet separation wall **122** is at a higher vertical level than the lower surface of the intermediate insulating layer MDI, and is at a lower vertical level than the upper surface of the intermediate insulating layer MDI. In some implementations, the nanosheet separation wall **122** includes an insulating material. For example, the insulating material may include SiCN, SiBCN, or a combination thereof.
[0027] A gate separation spacer **126** may be arranged on one sidewall relatively distant from one nanosheet separation wall **122** in the second horizontal direction (Y direction), among both sidewalls of each of a pair of upper nanosheet stacks NSSt, each of which is arranged on a pair of lower nanosheet stacks NSSb which include the one nanosheet separation wall **122** therebetween and are apart from each other in the second horizontal direction (Y direction). The gate separation spacer **126** may extend in parallel with each other in the second horizontal direction (Y direction). In some implementations, the lower surface of the gate separation spacer **126** is at a higher vertical level than a lower surface of the intermediate insulating layer MDI, and is at a lower vertical level than the upper surface of the intermediate insulating layer MDI. In some implementations, the gate separation spacer **126** is at a higher vertical level than each of an upper surface of an upper gate metal layer GMt and an upper surface of a lower gate metal layer GMb. The upper gate metal layer GMt and the lower gate metal layer GMb may be insulated from each other by the gate separation spacer **126**. In some implementations, the gate separation spacer **126** includes an insulating material. The insulating material may include, for example, SiCN, SiBCN, or a combination thereof. In some implementations, the gate separation spacer **126** includes substantially the same material as the nanosheet separation wall **122**. For example, the gate separation spacer **126** and the nanosheet separation wall **122** may include SiCN.
[0028] The plurality of gate lines GL may include a first gate metal layer **140***b*, a second gate metal layer **140***t*, and a third gate metal layer GM. The first gate metal layer **140***b* (sometimes referred to as a “first metal layer **140***b*”) may be arranged between the fin-type active area FA and the first nanosheet Nb**1**, between the first nanosheet Nb**1** and the second nanosheet Nb**2**, and between the

second nanosheet Nb**2** and the intermediate insulating layer MDI. The second gate metal layer **140***t* (sometimes referred to as a "second metal layer **140***t*") may be arranged between the intermediate insulating layer MDI and the third nanosheet Nt**1** and between the third nanosheet Nt**1** and the fourth nanosheet Nt**2**. The third gate metal layer GM (sometimes referred to as a "third metal layer GM") may include the lower gate metal layer GMb and the upper gate metal layer GMt. The lower gate metal layer GMb may cover one relatively distant sidewall on the one nanosheet separation wall **122** in the second horizontal direction (Y direction), among both sidewalls of each of a pair of lower nanosheet stacks NSSb which include one nanosheet separation wall **122** therebetween and are apart from each other in the second horizontal direction (Y direction). The upper gate metal layer GMt may cover one sidewall relatively close to the one nanosheet separation wall **122** in the second horizontal direction (Y direction), among both sidewalls of each of the pair of upper nanosheet stacks NSSt respectively arranged on the pair of lower nanosheet stacks NSSb, and may cover an upper surface of the fourth nanosheet Nt**2**. The lower gate metal layer GMb and the upper gate metal layer GMt may be spaced apart from each other with the gate separation spacer **126** therebetween in the second horizontal direction (Y direction).

[0029] The third metal layer GM may include, for example, a metal, conductive metal nitride, conductive metal carbide, conductive metal silicide, or a combination thereof. For example, the third gate metal layer GM may include Al, Cu, Ti, Ta, W, Mo, TaN, NiSi, CoSi, TiN, WN, TiAl, TiAlN, TaCN, TaC, TaSiN, or a combination thereof, but is not limited thereto.

[0030] The first metal layer **140***b* may include a metal, conductive metal nitride, conductive metal carbide, conductive metal silicide, that are doped with a p-type dopant, or a combination thereof. For example, the first metal layer **140***b* may include Al, Cu, Ti, Ta, W, Mo, TaN, NiSi, CoSi, TiN, WN, TiAl, TiAlN, TaCN, TaC, TaSiN, that are doped with a p-type dopant, or a combination thereof. The p-type dopant may include, for example, boron (B).

[0031] The second metal layer **140***t* may include a metal, conductive metal nitride, conductive metal carbide, conductive metal silicide, that are doped with an n-type dopant, or a combination thereof. For example, the first metal layer **140***b* may include Al, Cu, Ti, Ta, W, Mo, TaN, NiSi, CoSi, TiN, WN, TiAl, TiAlN, TaCN, TaC, TaSiN, that are doped with an n-type dopant, or a combination thereof. The p-type dopant may include, for example, arsenide (As) or phosphorus (P).

[0032] The first metal layer **140***b* and the lower gate metal layer GMb may constitute one gate connected to one lower nanosheet stack NSSb, and the second metal layer **140***t* and the upper gate metal layer GMt may constitute another gate connected to one upper nanosheet stack NSSt arranged on the one lower nanosheet stack NSSb. Accordingly, the lower gate metal layer GMb and the upper gate metal layer GMt may be insulated from each other by the gate separation spacer **126**, and the lower gate metal layer GMb and the upper gate metal layer GMt, which are insulated from each other, may constitute separate gates.

[0033] A first spacer **142***b* may be arranged on both sidewalls of the first metal layer **140***b*, and a second spacer **142***t* may be arranged on both sidewalls of the second metal layer **140***t*. Each of the first spacer **142***b* and the second spacer **142***t* may extend in parallel with each other in the second horizontal direction (Y direction). Each of the first spacer **142***b* and the second spacer **142***t* may include, for example, a nitride (e.g., silicon nitride).

[0034] A gate insulating layer **130** may be arranged between the fin-type active area FA and the first nanosheet Nb**1**, each of the first nanosheet Nb**1** and the second nanosheet Nb**2** and the first metal layer **140***b*, each of the first nanosheet Nb**1** and the second nanosheet Nb**2** and the lower gate metal layer GMb, between the first metal layer **140***b* and the intermediate insulating layer MDI, between each of the third nanosheet Nt**1** and the fourth nanosheet Nt**2** and the second metal layer **140***t*, between each of the third nanosheet Nt**1** and the fourth nanosheet Nt**2** and the upper gate metal layer GMt. In addition, the gate insulating layer **130** may cover at least a portion of the upper surface of the nanosheet separation wall **122**, and may cover at least a portion of the surface of the gate separation spacer **126**.

[0035] In some implementations, the gate insulating layer **130** includes a silicon oxide layer, a silicon oxynitride layer, a high-k dielectric layer having a dielectric constant higher than that of the silicon oxide layer, or a combination thereof. The high-k dielectric layer may include a metal oxide or a metal oxynitride. For example, the high-k layer may include HfO.sub.2, HfSiO, HfSiON, HfTaO, HfTiO, HfZrO, ZrO.sub.2, Al.sub.2O.sub.3, or a combination thereof, but is not limited thereto.

[0036] A gate capping layer **150** may be arranged on the third metal layer GM of the gate line GL. The gate capping layer **150** may cover an upper surface of the third metal layer GM. The gate capping layer **150** may extend on the third metal layer GM in the second horizontal direction (Y direction). In some implementations, the gate capping layer **150** includes silicon nitride or silicon oxynitride.

[0037] A first gate spacer CLD**1** and a second gate spacer CLD**2** may be sequentially arranged on both sidewalls of the third metal layer GM and the gate capping layer **150**. The first gate spacer CLD**1** and the second gate spacer CLD**2** may cover both sidewalls of the third metal layer GM and the gate capping layer **150**. The first gate spacer CLD**1** and the second gate spacer CLD**2** may extend on the substrate **102** in the second horizontal direction (Y direction).

[0038] In some implementations, each of the first gate spacer CLD**1** and the second gate spacer CLD**2** includes silicon oxide, silicon nitride, silicon oxynitride, silicon carbide, silicon oxide nitride, or a combination thereof.

[0039] A gate cut structure CT may extend in the first horizontal direction (X direction). The gate cut structure CT may cut (e.g., extend between) at least a portion of the gate lines GL adjacent to each other. The gate cut structure CT may include a first gate cut structure CTn and a second gate cut structure CTw. The first gate cut structure CTn may penetrate the gate capping layer **150** and the upper gate metal layer GMt to extend in the vertical direction (Z direction). The first gate cut structure CTn may be in contact with the upper surface of the nanosheet separation wall **122** on a bottom surface thereof. The first gate cut structure CTn may cut the upper gate metal layer GMt between a pair of upper nanosheet stacks NSSt respectively arranged on a pair of lower nanosheet stacks NSSb which include one nanosheet separation wall **122** therebetween and are apart from each other in the second horizontal direction (Y direction). The second gate cut structure CTw may penetrate the gate capping layer **150** and the lower gate metal layer GMb to extend in the vertical direction (Z direction). The second gate cut structure CTw may be in contact with the upper surface of the device separation layer **112** on a bottom surface thereof. The second gate cut structure CTw may cut the upper gate metal layer GMt between a pair of nanosheet stacks NSS (e.g., including NSSt and NSSb) including one nanosheet separation wall **122** and spaced apart from each other in the second horizontal direction (Y direction) and another pair of nanosheet stacks NSS adjacent to the pair of the nanosheet stacks NSS. The first gate cut structure CTn and the second gate cut structure CTw may include, for example, silicon nitride.

[0040] In some implementations, a second horizontal direction length of the first gate cut structure CTn is less than a second horizontal direction length of the second gate cut structure CTw. For example, the second horizontal direction length of the first gate cut structure CTn may be about 5 nm to about 10 nm, and the second horizontal direction length of the second gate cut structure CTw may be about 15 nm to about 35 nm.

[0041] A lower source/drain area SDb may be arranged between the lower nanosheet stacks NSSb apart from each other in the first horizontal direction (X direction), and an upper source/drain area SDt may be arranged between the upper nanosheet stacks NSSt arranged on the lower nanosheet stack NSSb. The lower source/drain area SDb may extend into the fin-type active area FA. The lower source/drain area SDb may be connected to both ends of the lower nanosheet stack NSSb, and the upper source/drain area SDt may be connected to both ends of the upper nanosheet stack NSSt. In some implementations, the lower source/drain area SDb and the upper source/drain area SDt include a doped Si layer, a doped SiGe layer, a doped Ge layer, a doped SiC layer, or a doped

InGaAs layer, but are not limited thereto. In some implementations, the lower source/drain area SDb and the upper source/drain area SDt include dopants of different conductivity types. For example, the lower source/drain area SDb may include an n-type dopant, and the upper source/drain area SDt may include a p-type dopant. The lower source/drain area SDb may form an n-type metal oxide semiconductor (NMOS) transistor together with the lower nanosheet stack NSSb, and the upper source/drain area SDt may form a p-type metal oxide semiconductor (PMOS) transistor together with the upper nanosheet stack NSSt.

[0042] A first etching stop layer CESL**1** may cover a surface of the lower source/drain area SDb. A second etching stop layer CESL**2** (refer to FIG. **26**D) may cover a surface of the upper source/drain area SDt. Each of the first etching stop layer CESL**1** and the second etching stop layer CESL**2** may include, for example, a nitride layer. A first interlayer insulating layer FO**1** may be arranged on the first etching stop layer CESL**1**, and may cover the first etching stop layer CESL**1**. A second interlayer insulating layer FO**2** (refer to FIG. **26**D) may be arranged on the second etching stop layer CESL**2**, and may cover the second etching stop layer CESL**2**. Each of the first interlayer insulating layer FO**1** and the second interlayer insulating layer FO**2** may include, for example, silicon oxide or an insulating material having a lower dielectric constant than silicon oxide. In some implementations, each of the first interlayer insulating layer FO**1** and the second interlayer insulating layer FO**2** includes a tetraethyl orthosilicate (TEOS) layer or an ultra-low dielectric constant (ULK) layer having an ultra-low dielectric constant K of about 2.2 to about 2.4. The ULK layer may include an SiOC layer or an SiCOH layer.

[0043] A plurality of gate contacts CB may penetrate the gate capping layer **150** to be in contact with the third metal layer GM of the gate line GL. Each of the plurality of gate contacts CB may include a first gate contact CBb and a second gate contact CBt. The first gate contact CBb may be in contact with the lower gate metal layer GMb, and the second gate contact CBt may be in contact with the upper gate metal layer GMt. The first gate contact CBb may be connected to a gate including the lower gate metal layer GMb and the first metal layer **140***b*, and the second gate contact CBt may be connected to a gate including the upper gate metal layer GMt and the second metal layer **140***t*.

[0044] A plurality of source/drain contacts CA may penetrate the second interlayer insulating layer FO**2** (refer to FIG. **26**D) and/or the first interlayer insulating layer FO**1** to be in contact with the upper source/drain area SDt or the lower source/drain area SDb. Each of the plurality of source/drain contacts CA may include a first source/drain contact CAb and a second source/drain contact CAt. The first source/drain contact CAb may penetrate the first interlayer insulating layer FO**1** and the second interlayer insulating layer FO**2** to be in contact with the lower source/drain area SDb. The second source/drain contact CAt may penetrate the second interlayer insulating layer FO**2** to be in contact with the upper source/drain area SDt.

[0045] In some implementations, each of the plurality of gate contacts CB and the plurality of source/drain contacts CA includes a metal, conductive metal nitride, or a combination thereof. For example, each of the plurality of gate contacts CB and the plurality of source/drain contacts CA may include a metal material, such as W, Al, Cu, Ti, Ta, Ru, Mn, and Co, metal nitride, such as TiN, TaN, CoN, and WN, or an alloy (e.g., a conductive alloy), such as cobalt tungsten phosphide (CoWP), cobalt tungsten boron (CoWB), and cobalt tungsten boron phosphide (CoWBP).

[0046] A contact cut structure CX (refer to FIG. **26**D) may penetrate the second interlayer insulating layer FO**2** and may be in contact with the upper surface of the first interlayer insulating layer FO**1**. The second source/drain contact CAt may be horizontally apart from each other with the contact cut structure CX therebetween. The contact cut structure CX may include, for example, silicon nitride.

[0047] The semiconductor device **100** may include the nanosheet separation wall **122** arranged between a pair of nanosheet stacks NSS and the gate separation spacer **126** arranged on both sidewalls of the pair of nanosheet stacks NSS. A pair of nanosheet stacks NSS may be apart from

each other by the nanosheet separation wall **122** to improve parasitic capacitance of the semiconductor device **100**. In addition, because the upper gate metal layer GMt is separated by the gate separation spacer **126**, each of the lower nanosheet stack NSSb and the upper nanosheet stack NSSt, which are included in the nanosheet stack NSS, may be connected to a separate gate. Accordingly, in some implementations, operating characteristics of the semiconductor device **100** may be improved.

[0048] FIG. **3** is a cross-sectional view of a semiconductor device **100***a*. Because components of the semiconductor device **100***a* illustrated in FIG. **3** are similar to components of the semiconductor device **100** illustrated in FIGS. **1**, **2**A, and **2**B, differences thereof are mainly described below; the characteristics of the semiconductor device **100***a* are the same as those described for the semiconductor device **100**, except where noted otherwise or suggested otherwise by context.

[0049] Referring to FIG. **3**, the semiconductor device **100***a* may have a configuration substantially similar to the configuration of the semiconductor device **100** illustrated in FIGS. **1**, **2**A, and **2**B, except that the semiconductor device **100***a* includes a gate cut structure CT**1** including the first gate cut structure CTn and a second gate cut structure CTw**1** and includes a vertical via VV penetrating the second gate cut structure CTw**1**.

[0050] The semiconductor device **100***a* may include the vertical via VV which penetrates the second gate cut structure CTw**1** and extends in the vertical direction (Z direction). The second gate cut structure CTw**1** and the vertical via VV may extend into the device separation layer **112**. The vertical via VV may include, for example, a conductive metal. For example, the vertical via VV may include W. In some implementations, the second horizontal direction length of the vertical via VV ia about 10 nm. The vertical via VV may provide an electrical connection path between transistors included in the semiconductor device **100***a*.

[0051] FIG. **4** is a cross-sectional view of a semiconductor device **100***b*. Because components of the semiconductor device **100***b* illustrated in FIG. **4** are similar to components of the semiconductor device **100** illustrated in FIGS. **1**, **2**A, and **2**B, differences thereof are mainly described below; the characteristics of the semiconductor device **100***b* are the same as those described for the semiconductor device **100**, except where noted otherwise or suggested otherwise by context.

[0052] Referring to FIG. **4**, the semiconductor device **100***b* may have a configuration substantially similar to the configuration of the semiconductor device **100** illustrated in FIGS. **1**, **2**A, and **2**B except that the gate separation spacer **126** (refer to FIG. **2**B) is not included.

[0053] The semiconductor device **100***b* may not include the gate separation spacer **126**. Accordingly, a third metal layer GM**1** may not be separated by the gate separation spacer **126**. Because the third metal layer GM**1** is not separated, the first metal layer **140***b*, the second metal layer **140***t*, and the third metal layer GM**1** may form one gate together. One lower nanosheet stack NSSb and one upper nanosheet stack NSSt arranged on the one lower nanosheet stack NSSb may share one gate including the first metal layer **140***b*, the second metal layer **140***t*, and the third metal layer GM**1**. The one gate including the first metal layer **140***b*, the second metal layer **140***t*, and the third metal layer GM**1** may be connected to a gate contact CB**1**.

[0054] FIGS. **5**A, **5**B, **6**A, **6**B, **7**A, **7**B, **8**A, **8**B, **9**A, **9**B, **9**C, **9**D, **10**A, **10**B, **10**C, **10**D, **11**A, **11**B, **12**A, **12**B, **12**C, **13**A, **13**B, **14**A, **14**B, **14**C, **15**A, **15**B, **15**C, **16**A, **16**B, **16**C, **17**A, **17**B, **17**C, **18**A, **18**B, **18**C, **19**A, **19**B, **20**A, **20**B, **21**A, **21**B, **22**A, **22**B, **23**A, **23**B, **23**C, **24**A, **24**B, **24**C, **25**A, **25**B, **25**C, **25**D, **26**A, **26**B, **26**C, and **26**D are cross-sectional views of a manufacturing method of a semiconductor device, e.g., the semiconductor device **100**. FIGS. **5**A, **6**A, **7**A, **8**A, **9**A, **10**A, **11**A, **12**A, **13**A, **14**A, **15**A, **16**A, **17**A, **18**A, **19**A, **20**A, **21**A, **22**A, **23**A, **24**A, **25**A, and **26**A are cross-sectional views taken along line X**1**-X**1**′ in FIG. **1**; FIGS. **9**B, **10**B, **12**B, **14**B, **15**B, **16**B, **17**B, **18**B, **23**B, **24**B, **25**B, and **26**B are cross-sectional views taken along line X**2**-X**2**′ in FIG. **1**; FIGS. **5**B, **6**B, **7**B, **8**B, **9**C, **10**C, **18**C, **19**B, **21**B, **22**B, **23**C, **24**C, **24**C, **25**C, and **26**C are cross-sectional views taken along line Y**1**-Y**1**′ in FIG. **1**; and FIGS. **9**D, **10**D, **11**D, **12**C, **13**B, **14**C, **15**C, **16**D, **17**C, **25**D, and **26**D are cross-sectional views taken along line Y**2**-Y**2**′ in FIG. **1**.

[0055] Referring to FIGS. **5**A and **5**B, firstly, a plurality of sacrificial layers **104** and a plurality of lower nanosheet semiconductor layers NSb may be alternately stacked on the substrate **102**, and after an intermediate sacrificial layer MDS is formed, the plurality of sacrificial layers **104** and a plurality of upper nanosheet semiconductor layers NSt may be alternately stacked on the intermediate sacrificial layer MDS. Each of the plurality of sacrificial layers **104**, the plurality of lower nanosheet semiconductor layers NSb, the plurality of upper nanosheet semiconductor layers NSt, and the intermediate sacrificial layer MDS may extend in parallel with the upper surface of the substrate **102**.

[0056] Next, after a plurality of hard mask patterns are formed on a stacked structure of the plurality of sacrificial layers **104**, the plurality of lower nanosheet semiconductor layers NSb, the plurality of upper nanosheet semiconductor layers NSt, and the intermediate sacrificial layer MDS, the plurality of sacrificial layers **104**, the plurality of lower nanosheet semiconductor layers NSb, the plurality of upper nanosheet semiconductor layers NSt, and the intermediate sacrificial layer MDS may be patterned by using the plurality of hard mask patterns as an etching mask, and by removing a portion of the semiconductor substrate **102** exposed between the patterned resultant product together, a plurality of device separation layer trenches **112**T and a plurality of separation recesses **122**T may be formed. Each of the plurality of hard mask patterns may include nitride. For example, each of the plurality of hard mask patterns may include silicon nitride. After the plurality of device separation layer trenches **112**T and the plurality of separation recesses **122**T are formed, the plurality of hard mask patterns may be removed.

[0057] Each of the plurality of device separation layer trenches **112**T and the plurality of separation recesses **122**T may extend in the first horizontal direction (X direction). In some implementations, the plurality of device separation layer trenches **112**T and the plurality of separation recesses **122**T are formed to be alternately arranged in the second horizontal direction (Y direction).

[0058] Next, an insulating material layer **120**M may be formed, which fills the plurality of separation recesses **122**T and covers surfaces of the substrate **102**, the plurality of sacrificial layers **104**, the plurality of lower nanosheet semiconductor layers NSb, the plurality of upper nanosheet semiconductor layers NSt, and the intermediate sacrificial layer MDS. The insulating material layer **120**M may include, for example, SiCN, SiBCN, or a combination thereof.

[0059] Referring to FIGS. **6**A and **6**B, from the resultant product of FIGS. **5**A and **5**B, a portion of the insulating material layer **120**M (refer to FIG. **5**A) may be removed to form the nanosheet separation wall **122** filling each of the plurality of separation recesses **122**T. The nanosheet separation wall **122** may be formed by removing a portion of the insulating material layer **120**M by using, for example, an etch-back process. A portion of the insulating material layer **120**M which has not been removed by using the etch-back process may remain at a lower edge of each of the plurality of device separation layer trenches **112**T. The insulating material remaining at the lower edge of each of the plurality of device separation layer trenches **112**T may be referred to as the residual insulating material **124**. The upper surface of the nanosheet separation wall **122** formed by using the etch-back process may be at a lower vertical level than the upper surface of the intermediate sacrificial layer MDS, and may be at a higher vertical level than the lower surface of the intermediate sacrificial layer MDS.

[0060] Referring to FIGS. **7**A and **7**B, in the resultant product of FIGS. **6**A and **6**B, the plurality of device separation layer trenches **112**T may be filled with an insulating material to form the device separation layer **112**. In this case, the upper surface of the formed device separation layer **112** may be at a lower vertical level than the upper surface of the intermediate sacrificial layer MDS, and may be at a higher vertical level than the lower surface of the intermediate sacrificial layer MDS.

[0061] Next, an insulating material layer **126**M covering a surface of each of the device separation layer **112**, the plurality of sacrificial layers **104**, the plurality of upper nanosheet semiconductor layers NSt, and the intermediate sacrificial layer MDS may be formed. The insulating material layer **126**M may include, for example, SiCN, SiBCN, or a combination thereof.

[0062] Referring to FIGS. **8**A and **8**B, from the resultant product of FIGS. **7**A and **7**B, a portion of the insulating material layer **126**M may be removed to form the gate separation spacer **126**. Next, a portion of the device separation layer **112** may be removed so that the upper surface of the device separation layer **112** is positioned at the same vertical level as the upper surface of the fin-type active area FA.

[0063] In some implementations, the process described with reference to FIGS. **7**A and **7**B and the process described with reference to FIGS. **8**A and **8**B may be omitted. In this case, the gate separation spacer **126** may not be formed, and after the process described with reference to FIGS. **6**A and **6**B is performed, and then the process to be described below with reference to FIGS. **9**A through **26**D is performed, the semiconductor device **100***b* illustrated in FIG. **4** may be formed.

[0064] Referring to FIGS. **9**A, **9**B, **9**C, and **9**D, after a dummy gate electrode DPCP and a plurality of hard mask patterns HM are sequentially formed from the resultant product of FIGS. **8**A and **8**B, the dummy gate electrode DPCP may be patterned by using the plurality of hard mask patterns HM as an etching mask. An upper surface of the sacrificial layer **104** at the uppermost end and the upper surface of the device separation layer **112** may be exposed by the patterned dummy gate electrode DPCP.

[0065] The plurality of hard mask patterns HM may extend in the second horizontal direction (Y direction), and may be formed apart from each other in the first horizontal direction (X direction). Each of the plurality of hard mask patterns HM may include nitride. For example, each of the plurality of hard mask patterns HM may include silicon nitride. The plurality of dummy gate electrodes DPCP respectively patterned by the plurality of hard mask patterns HM may each extend in the second horizontal direction (Y direction), and may be formed apart from each other in the first horizontal direction (X direction). The dummy gate electrode DPCP may include, for example, polysilicon, but is not limited thereto.

[0066] Referring to FIGS. **10**A, **10**B, **10**C, and **10**D, from the resultant product of FIGS. **9**A, **9**B, **9**C, and **9**D, the first gate spacer CLD**1** covering the side surfaces of the plurality of dummy gate electrodes DPCP and the side surfaces of the plurality of hard mask patterns HM may be formed. Next, an anisotropic etching process may be performed to remove a portion of a stacked structure of the plurality of sacrificial layers **104**, the plurality of lower nanosheet semiconductor layers NSb, the plurality of upper nanosheet semiconductor layers NSt, and the intermediate sacrificial layer MDS, thereby forming a first nanosheet Nb**1**, which are under a space between a stacked structure of the plurality of dummy gate electrodes DPCP and a plurality of hard mask patterns HM, and form the first nanosheet Nb**1**, the second nanosheet Nb**2**, a third nanosheet Nb**3**, and a fourth nanosheet Nb**4**. A plurality of source/drain trenches SDT may be defined in spaces between the first nanosheet Nb**1**, the second nanosheet Nb**2**, the third nanosheet Nb**3**, and the fourth nanosheet Nb**4**. In the process of forming the first nanosheet Nb**1**, the second nanosheet Nb**2**, the third nanosheet Nb**3**, and the fourth nanosheet Nb**4**, a portion of the fin-type active area FA may be removed to form a first recess RS**1**, and a portion of the nanosheet separation wall **122** may be removed to form a second recess RS**2**.

[0067] Next, the intermediate sacrificial layer MDS may be removed, and an intermediate insulating layer MDI may be formed by filling the space, where the intermediate sacrificial layer MDS has been removed, with an insulating material.

[0068] Referring to FIGS. **11**A and **11**B, from the resultant product of FIGS. **10**A, **10**B, **10**C, and **10**D, a spin-on hard mask SOH may be formed to fill the first recess RS**1** formed by removing a portion of the plurality of source/drain trenches SDT and a portion of the fin-type active area FA, and the second recess RS**2** formed by removing a portion of the nanosheet separation wall **122**, and a portion of the spin-on hard mask SOH may be removed so that the upper surface of the spin-on hard mask SOH is at a lower vertical level than the upper surface of the intermediate insulating layer MDI while the upper surface of the spin-on hard mask SOH is at a higher vertical level than the lower surface of the intermediate insulating layer MDI.

[0069] Next, portions of the sidewalls of each of the plurality of sacrificial layers **104** formed on the intermediate insulating layer MDI may be recessed, and the second spacer **142***t* filling recessed spaces may be formed.
[0070] Referring to FIGS. **12**A, **12**B, and **12**C, from the resultant product of FIGS. **11**A and **11**B, the spin-on hard mask SOH may be removed, portions of sidewalls of each of the plurality of sacrificial layers **104** formed under the intermediate insulating layer MDI may be recessed, and an insulating material layer **142***b*M filling recessed spaces may be formed. The insulating material layer **142***b*M may include, for example, silicon nitride.
[0071] Referring to FIGS. **13**A and **13**B, from the resultant product of FIGS. **12**A, **12**B, and **12**C, the lower source/drain area SDb may be formed by using an epitaxial growth from both side surfaces of each of the first nanosheet Nb**1** and the second nanosheet Nb**2**. The lower source/drain area SDb may include, for example, an embedded SiGe structure including a plurality of epitaxially grown SiGe layers, an epitaxially grown Si layer, or an epitaxially grown SiC layer.
[0072] Referring to FIGS. **14**A, **14**B, and **14**C, from the resultant product of FIGS. **13**A and **13**B, the first etching stop layer CESL**1** covering at least a portion of the surface of the lower source/drain area SDb and the upper surface of the device separation layer **112** may be formed. The first etching stop layer CESL**1** may cover the second recess RS**2** formed in the nanosheet separation wall **122**. The first etching stop layer CESL**1** may include, for example, a silicon nitride layer.
[0073] Referring to FIGS. **15**A, **15**B, and **15**C, from the results of FIGS. **14**A, **14**B, and **14**C, a first interlayer insulating layer FO**1** covering the first etching stop layer CESL**1** may be formed. Next, after a portion of the first interlayer insulating layer FO**1** is removed, the upper surface of the first interlayer insulating layer FO**1** may be at substantially the same vertical level as the upper surface of the intermediate insulating layer MDI. The first interlayer insulating layer FO**1** may include, for example, silicon oxide.
[0074] Referring to FIGS. **16**A, **16**B, and **16**C, from the resultant product of FIGS. **15**A, **15**B, and **15**C, an upper source/drain area SDt may be formed by using an epitaxial growth from both side surfaces of each of the third nanosheet Nt**1** and the fourth nanosheet Nt**2**. The upper source/drain area SDt may include, for example, an embedded SiGe structure including a plurality of epitaxially grown SiGe layers, an epitaxially grown Si layer, or an epitaxially grown SiC layer. Next, a second etching stop layer CESL**2** covering the surface of the upper source/drain area SDt may be formed. The second etching stop layer CESL**2** may include, for example, a silicon nitride layer. Next, the second interlayer insulating layer FO**2** may be formed on the second etching stop layer CESL**2**. The second interlayer insulating layer FO**2** may include, for example, silicon oxide.
[0075] Referring to FIGS. **17**A, **17**B, and **17**C, from the resultant product of FIGS. **16**A, **16**B, and **16**C, a portion of the second interlayer insulating layer FO**2** may be removed, and an upper insulating layer ILD filling a space, in which the portion of the second interlayer insulating layer FO**2** has been removed, may be formed. The upper insulating layer ILD may cover an upper surface of the second interlayer insulating layer FO**2**. The upper insulating layer ILD may include, for example, silicon nitride.
[0076] Referring to FIGS. **18**A, **18**B, and **18**C, in the resultant product of FIGS. **17**A, **17**B, and **17**C, a portion of the upper insulating layer ILD may be removed, and a patterned dummy gate electrode DPCP (refer to FIG. **17**A) and the plurality of hard mask patterns HM (refer to FIG. **17**A) may be removed to form a first gate space GS**1**. A portion of the upper insulating layer ILD may be removed by using, for example, a chemical mechanical polishing (CMP) process. The first gate space GS**1** may expose at least a portion of an upper surface of the sacrificial layer **104** at the uppermost end among the plurality of sacrificial layers **104** and an upper surface of the device separation layer **112**.
[0077] Referring to FIGS. **19**A and **19**B, from the resultant product of FIGS. **18**A, **18**B, and **18**C, by removing the plurality of sacrificial layers **104** (refer to FIG. **18**A) through the first gate space

GS**1**, the second gate space GS**2** and a third gate space GS**3**, the first gate space GS**1**, the second gate space GS**2**, and the third gate space GS**3** may interconnected with each other. In some implementations, to selectively remove the plurality of sacrificial layers **104** (refer to FIG. **18**A), an etching selectivity difference between the first nanosheet Nb**1**, the second nanosheet Nb**2**, the third nanosheet Nt**1**, and the fourth nanosheet Nt**2**, and the plurality of sacrificial layers **104** (refer to FIG. **18**A) may be used. For example, a liquid or gaseous etchant may be used to selectively remove the plurality of sacrificial layers **104**. In some implementations, to selectively remove the plurality of sacrificial layers **104**, a CH.sub.3COOH-based etchant, such as an etchant solution containing a mixture of CH.sub.3COOH, HNO.sub.3, and HF, or an etchant solution containing a mixture of CH.sub.3COOH, H.sub.2O.sub.2, and HF, may be used, but is not limited thereto.

[0078] Next, the gate insulating layer **130** covering a surface of each of the first nanosheet Nb**1**, the second nanosheet Nb**2**, the third nanosheet Nt**1**, and the fourth nanosheet Nt**2**, which are exposed by the first gate space GS**1**, the second gate space GS**2**, and the third gate space GS**3**, may be formed.

[0079] In some implementations, after the process described with reference to FIGS. **19**A and **19**B is performed, a process of forming a dipole material layer covering at least a portion of the gate insulating layer **130** exposed by the second gate space GS**2** and the third gate space GS**3** is performed. For example, the dipole material layer may be formed on the gate insulating layer **130** covering at least one of a pair of lower nanosheet stacks NSSb or at least one of a pair of upper nanosheet stacks NSSt, which are spaced apart from each other with the nanosheet separation wall **122** therebetween.

[0080] Referring to FIGS. **20**A and **20**B, from the resultant product of FIGS. **19**A and **19**B, a metal oxide layer **140***t*M filling the second gate space GS**2** may be formed. The metal oxide layer **140***t*M may be formed by using, for example, a deposition process. The metal oxide layer **140***t*M may include, for example, aluminum oxide.

[0081] Referring to FIGS. **21**A and **21**B, from the resultant product of FIGS. **20**A and **20**B, the first metal layer **140***b* filling the third gate space GS**3** (refer to FIG. **20**A) may be formed. The first metal layer **140***b* may include, for example, a deposition process. A portion of the first metal layer **140***b* formed by using the deposition process beyond the third gate space GS**3** may be removed by using the etch-back process, and only the first metal layer **140***b* filling the third gate space GS**3** may remain. The first metal layer **140***b* may include, for example, a metal doped with a p-type dopant.

[0082] Referring to FIGS. **22**A and **22**B, from the resultant product of FIGS. **21**A and **21**B, the metal oxide layer **140***t*M (refer to FIG. **21**A) filling the second gate space GS**2** (refer to FIG. **19**A) may be removed, and the second metal layer **140***t* filling the second gate space GS**2** (refer to FIG. **21**A), from which the metal oxide layer **140***t*M (refer to FIG. **21**A) is removed, may be formed. The metal oxide layer **140***t*M (refer to FIG. **21**A) may be removed by using, for example, a wet etching process. The second metal layer **140***t* may include, for example, a deposition process. A portion formed beyond the second gate space GS**2** of the second metal layer **140***t*, which is formed by the deposition process, may be removed by using the etch-back process, and only the second metal layer **140***t* filling the second gate space GS**2** may remain. The second metal layer **140***t* may include, for example, a metal doped with an n-type dopant.

[0083] Referring to FIGS. **23**A, **23**B, and **23**C, from the resultant product of FIGS. **22**A and **22**B, the third metal layer GM filling the first gate space GS**1** (refer to FIG. **22**A) may be formed. The third metal layer GM may be formed by using, for example, a deposition process. A third metal layer GM may include, for example, a metal, conductive metal nitride, conductive metal carbide, conductive metal silicide, or a combination thereof. The third metal layer GM formed as described above may include the upper gate metal layer GMt and the lower gate metal layer GMb, which are apart from each other by the gate separation spacer **126**.

[0084] Referring to FIGS. **24**A, **24**B, and **24**C, from the resultant product of FIGS. **23**A, **23**B, and

23C, a portion of the third metal layer GM may be removed, and then the gate capping layer **150** filling a space, from which the portion of the third metal layer GM has been removed, may be formed. The gate capping layer **150** may cover the upper surface of the third metal layer GM. The gate capping layer **150** may include, for example, silicon nitride.

[0085] Referring to FIGS. **25**A, **25**B, **25**C, and **25**D, from the resultant product of FIGS. **24**A, **24**B, and **24**C, the upper insulating layer ILD (refer to FIG. **24**A), a portion of the gate capping layer **150**, a portion of the first gate spacer CLD**1**, and a portion of the second gate spacer CLD**2** may be removed. The upper insulating layer ILD (refer to FIG. **24**A), a portion of the gate capping layer **150**, a portion of the first gate spacer CLD**1**, and a portion of the second gate spacer CLD**2** may be removed by using, for example, a chemical mechanical polishing (CMP) process. The upper insulating layer ILD (refer to FIG. **24**A) may be completely removed by using the CMP process.

[0086] Next, the first gate cut structure CTn penetrating the gate capping layer **150** and the upper gate metal layer GMt and extending in the vertical direction (Z direction), and the second gate cut structure CTw penetrating the gate capping layer **150** and the lower gate metal layer GMb and extending in the vertical direction (Z direction) may be formed. The first gate cut structure CTn may be in contact with the upper surface of the nanosheet separation wall **122** on a bottom surface thereof, and the second gate cut structure CTw may be in contact with the upper surface of the device separation layer **112** on the bottom surface thereof.

[0087] In some implementations, after the processes described above with reference to FIGS. **25**A, **25**B, **25**C, and **25**D are performed, a process of forming the vertical via VV (refer to FIG. **3**), which penetrates the second gate cut structure CTw and extends in the vertical direction (Z direction), is performed. In this case, processes described below with reference to FIGS. **26**A, **26**B, **26**C, and **26**D may be performed to manufacture the semiconductor device **100***a* illustrated in FIG. **3**.

[0088] Referring to FIGS. **26**A, **26**B, **26**C, and **26**D, from the resultant product of FIGS. **25**A, **25**B, **25**C, and **25**D, a contact cut structure CX penetrating the second interlayer insulating layer FO**2** and extending in the vertical direction (Z direction) may be formed. The contact cut structure CX may be in contact with the first interlayer insulating layer FO**1** on a bottom surface thereof. Next, the first source/drain contact CAB penetrating the first interlayer insulating layer FO**1** and the second interlayer insulating layer FO**2** and extending in the vertical direction (Z direction), and the second source/drain contact CAt penetrating the second interlayer insulating layer FO**2** and extending in the vertical direction (Z direction) may be formed. The first source/drain contact CAb may be in contact with the lower source/drain area SDb on a bottom surface thereof, and the second source/drain contact CAt may be in contact with the upper source/drain area SDt on the bottom surface thereof.

[0089] Next, from the resultant product of FIGS. **26**A, **26**B, **26**C, and **26**D, by forming the first gate contact CBb and the second gate contact CBt, which penetrate the gate capping layer **150** and extend in the vertical direction (Z direction), the semiconductor device **100** illustrated in FIGS. **1**, **2***a*, and **2***b* may be manufactured.

[0090] While this disclosure contains many specific implementation details, these should not be construed as limitations on the scope of what may be claimed. Certain features that are described in this disclosure in the context of separate implementations can also be implemented in combination in a single implementation. Conversely, various features that are described in the context of a single implementation can also be implemented in multiple implementations separately or in any suitable subcombination. Moreover, although features may be described above as acting in certain combinations, one or more features from a combination can in some cases be excised from the combination, and the combination may be directed to a subcombination or variation of a subcombination.

[0091] While various examples have been particularly shown and described, it will be understood that various change in form and details may be made therein without departing from the spirit and scope of the following claims.

Claims

1. A semiconductor device comprising: a substrate including a pair of fin-type active areas and a device separation layer covering a sidewall of the pair of fin-type active areas; a pair of nanosheet stacks arranged on the pair of fin-type active areas, respectively, wherein each nanosheet stack of the pair of nanosheet stacks includes a lower nanosheet stack arranged on a corresponding fin-type active area of the pair of fin-type active areas, and an upper nanosheet stack arranged on the lower nanosheet stack; an intermediate insulating layer arranged between the lower nanosheet stack and the upper nanosheet stack of each of the pair of nanosheet stacks; a nanosheet separation wall arranged between the pair of nanosheet stacks and extending in a first horizontal direction; and a pair of gate lines on the pair of nanosheet stacks, wherein the nanosheet separation wall separates the lower nanosheet stacks in the pair of nanosheet stacks from one another in a second horizontal direction.

2. The semiconductor device of claim 1, wherein an upper surface of the nanosheet separation wall is at a lower vertical level than an upper surface of the intermediate insulating layer and at a higher vertical level than a lower surface of the intermediate insulating layer.

3. The semiconductor device of claim 1, wherein the device separation layer is arranged in a device separation trench formed in the substrate, and wherein a residual insulating material is arranged on a lower end edge of a sidewall of the device separation trench adjacent to the pair of nanosheet stacks in the second horizontal direction.

4. The semiconductor device of claim 3, wherein the nanosheet separation wall and the residual insulating material comprise a same material.

5. The semiconductor device of claim 1, further comprising: a first gate cut structure separating the upper nanosheet stacks in the pair of nano sheet stacks from one another in the second horizontal direction; and a second gate cut structure separating another pair of nanosheet stacks, adjacent to the pair of nanosheet stacks, from the pair of nanosheet stacks in the second horizontal direction, wherein a length of the first gate cut structure in the second horizontal direction is less than a length of the second gate cut structure in the second horizontal direction.

6. The semiconductor device of claim 5, wherein: a bottom surface of the first gate cut structure is in contact with an upper surface of the nanosheet separation wall, and a bottom surface of the second gate cut structure is in contact with the device separation layer.

7. The semiconductor device of claim 5, further comprising a vertical via extending vertically into the second gate cut structure.

8. The semiconductor device of claim 1, wherein the lower nanosheet stack and the upper nanosheet stack included in a first nanosheet stack of the pair of nanosheet stacks are connected to a gate contact.

9. A semiconductor device comprising: a substrate including a pair of fin-type active areas and a device separation layer covering a sidewall of the pair of fin-type active areas; a pair of nanosheet stacks arranged on the pair of fin-type active areas, respectively, wherein each nanosheet stack of the pair of nanosheet stacks includes a lower nanosheet stack arranged on a corresponding fin-type active area of the pair of fin-type active areas, and an upper nanosheet stack arranged on the lower nanosheet stack; an intermediate insulating layer arranged between the lower nanosheet stack and the upper nanosheet stack of each of the pair of nanosheet stacks; a nanosheet separation wall arranged between the pair of nanosheet stacks and extending in a first horizontal direction; a gate separation spacer arranged on a first sidewall of a first nanosheet stack of the pair of nanosheet stacks, wherein the first sidewall is opposite a second sidewall of the first nanosheet stack, and wherein the second sidewall is closer to a second nanosheet stack of the pair of nanosheet stacks than is the first sidewall; and a pair of gate lines on the pair of nanosheet stacks, wherein the nanosheet separation wall separates the lower nanosheet stacks of the pair of nanosheet stacks from

one another in a second horizontal direction.

10. The semiconductor device of claim 9, wherein an upper surface of the gate separation spacer is at a higher vertical level than an upper surface of the first nanosheet stack.

11. The semiconductor device of claim 9, wherein a lower surface of the gate separation spacer is at a lower vertical level than an upper surface of the intermediate insulating layer and at a higher vertical level than a lower surface of the intermediate insulating layer.

12. The semiconductor device of claim 9, wherein the gate separation spacer and the nanosheet separation wall comprise a same material.

13. The semiconductor device of claim 9, wherein the lower nanosheet stack of the first nanosheet stack comprises a first nanosheet and a second nanosheet, wherein the upper nanosheet stack of the first nanosheet stack comprises a third nanosheet and a fourth nanosheet, wherein the pair of gate lines comprise: a first metal layer arranged between the fin-type active area corresponding to the first nanosheet stack and the first nanosheet, between the first nanosheet and the second nanosheet, and between the second nanosheet and the intermediate insulating layer, and a second metal layer and a third metal layer respectively arranged between the intermediate insulating layer and the third nanosheet and between the third nanosheet and the fourth nanosheet, and wherein the third metal layer comprises a lower gate metal layer and an upper gate metal layer spaced apart from one another by the gate separation spacer.

14. The semiconductor device of claim 13, wherein the lower nanosheet stack of the first nanosheet stack is electrically connected to a first gate contact in contact with the lower gate metal layer, and the upper nanosheet stack of the first nanosheet stack is electrically connected to a second gate contact in contact with the upper gate metal layer.

15. The semiconductor device of claim 9, wherein an upper surface of the nanosheet separation wall is at a lower vertical level than an upper surface of the intermediate insulating layer and at a higher vertical level than a lower surface of the intermediate insulating layer.

16. The semiconductor device of claim 9, wherein: the device separation layer is arranged in a device separation trench formed in the substrate, a residual insulating material is arranged on a lower end edge of a sidewalls of the device separation trench adjacent to the pair of nanosheet stacks in the second horizontal direction, and the residual insulating material comprises a same material to that of the nanosheet separation wall.

17. The semiconductor device of claim 9, further comprising: a first gate cut structure separating the upper nanosheet stacks of the pair of nano sheet stacks from one another in the second horizontal direction; and a second gate cut structure separating another pair of nanosheet stacks, adjacent to the pair of nanosheet stacks, from the pair of nanosheet stacks in the second horizontal direction, wherein a bottom surface of the first gate cut structure is in contact with an upper surface of the nanosheet separation wall, wherein the second gate cut structure is in contact with the device separation layer, and wherein a length of the first gate cut structure in the second horizontal direction is less than a length of the second gate cut structure in the second horizontal direction.

18. The semiconductor device of claim 17, comprising a vertical via configured to extending into the second gate cut structure and the device separation layer.

19. A semiconductor device comprising: a substrate including a pair of fin-type active areas and a device separation layer covering a sidewall of the pair of fin-type active areas, wherein the device separation layer is arranged in a device separation trench; a pair of nanosheet stacks arranged on the pair of fin-type active areas, respectively, wherein each nanosheet stack of the pair of nanosheet stacks includes a lower nanosheet stack arranged on a corresponding fin-type active area of the pair of fin-type active areas, and an upper nanosheet stack arranged on the lower nanosheet stack; an intermediate insulating layer arranged between the lower nanosheet stack and the upper nanosheet stack of each of the pair of nanosheet stacks; a nanosheet separation wall arranged between the pair of nanosheet stacks and extending in a first horizontal direction; a residual insulating material arranged on a lower end edge of a sidewall of the device separation trench adjacent to the pair of

nanosheet stacks in a second horizontal direction; a gate separation spacer arranged on a first sidewall of a first nanosheet stack of the pair of nanosheet stacks, wherein the first sidewall is opposite a second sidewall of the first nanosheet stack, and wherein the second sidewall is closer to a second nanosheet stack of the pair of nanosheet stacks than is the first sidewall; a pair of gate lines on the pair of nanosheet stacks, the pair of gate lines including a first metal layer, a second metal layer, and a third metal layer; and a gate cut structure including: a first gate cut structure separating the upper nanosheet stacks of the pair of nano sheet stacks from one another in the second horizontal direction, and a second gate cut structure separating another pair of nanosheet stacks, adjacent to the pair of nanosheet stacks, from the pair of nanosheet stacks in the second horizontal direction, wherein the nanosheet separation wall separates the lower nanosheet stacks of the pair of nanosheet stacks from one another in the second horizontal direction, and wherein the third metal layer comprises a lower gate metal layer and an upper gate metal layer spaced apart from one another by the gate separation spacer.

20. The semiconductor device of claim 19, wherein the nanosheet separation wall, the gate separation spacer, and the residual insulating material comprise a same material comprising SiCN, SiBCN, or a combination thereof.