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(54) **SOLID-STATE IMAGING DEVICE**

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H10F 39/18	(2025.01)

(52) **U.S. Cl.**

CPC ***H10F 39/811*** (2025.01); ***H01L 23/5223*** (2013.01); ***H04N 25/79*** (2023.01); ***H10F 39/182*** (2025.01); ***H10F 39/8063*** (2025.01); ***H10F 39/809*** (2025.01)

(57) **ABSTRACT**

Provided is a solid-state imaging device capable of reducing cost related to a capacitor. A solid-state imaging device of the present disclosure includes: a first substrate; a photoelectric conversion unit provided in the first substrate; a floating diffusion unit provided in the first substrate; a pixel transistor electrically connected to the floating diffusion unit; and a capacitor including a first electrode electrically connected or connectable to the pixel transistor, a second electrode different from the first electrode, and a first ferroelectric film or a first antiferroelectric film provided between the first electrode and the second electrode.

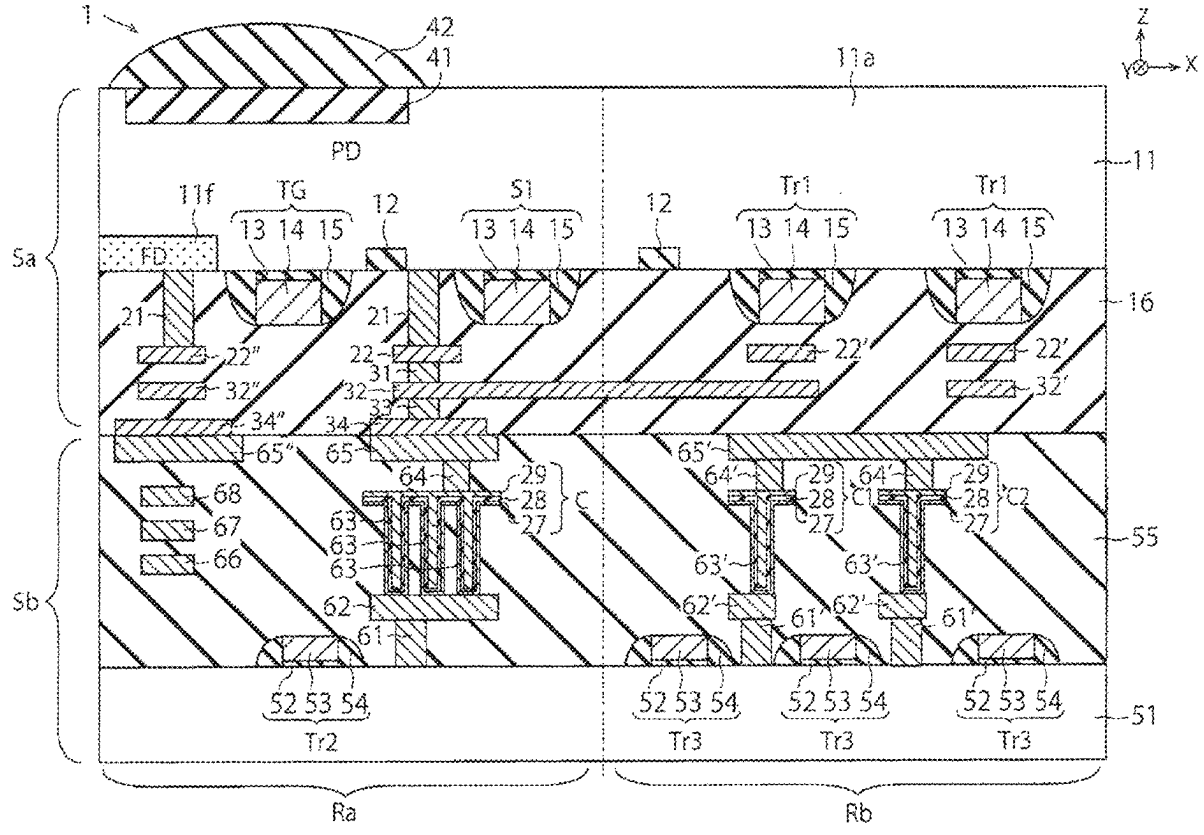


FIG. 1

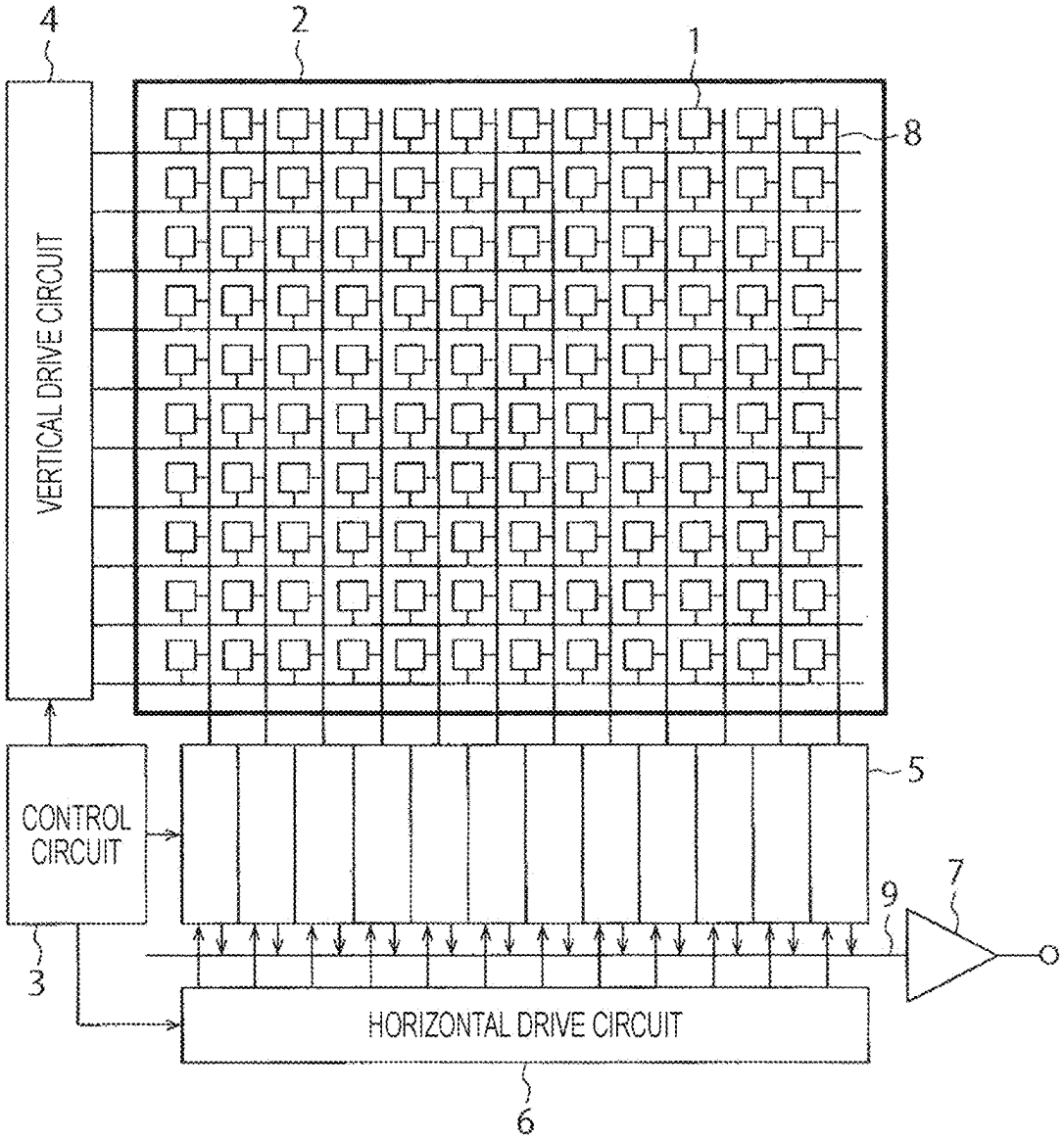

4
2
1
8
VERTICAL DRIVE CIRCUIT
CONTROL CIRCUIT
5
9
7
3
HORIZONTAL DRIVE CIRCUIT
6

FIG. 2

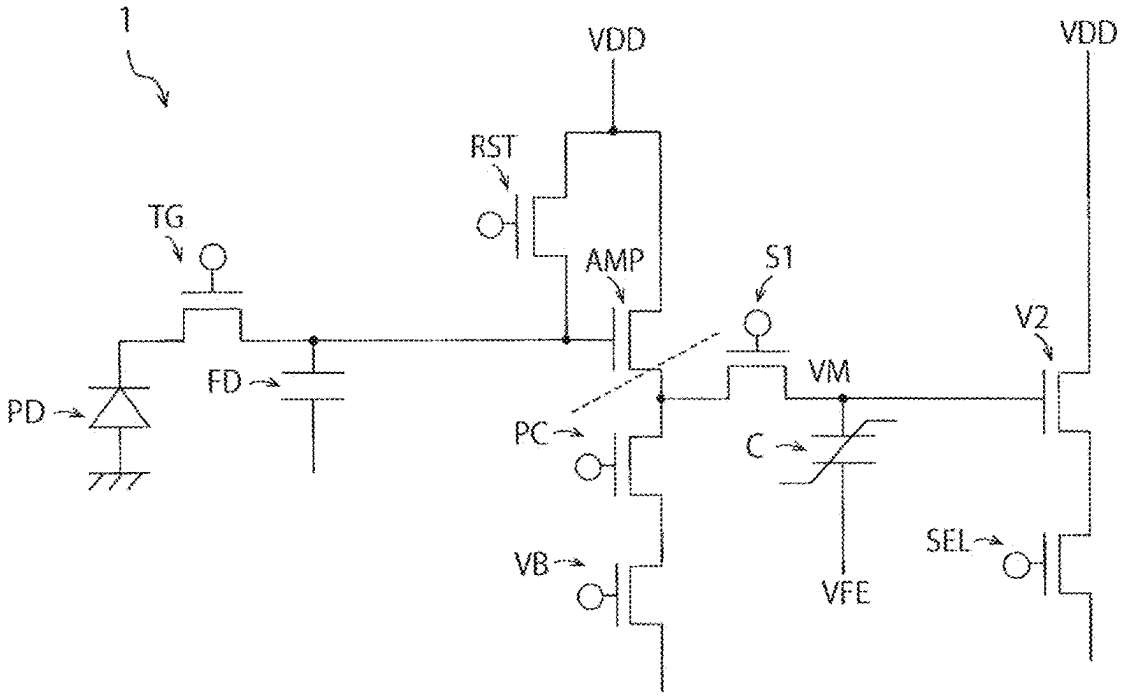


FIG. 3

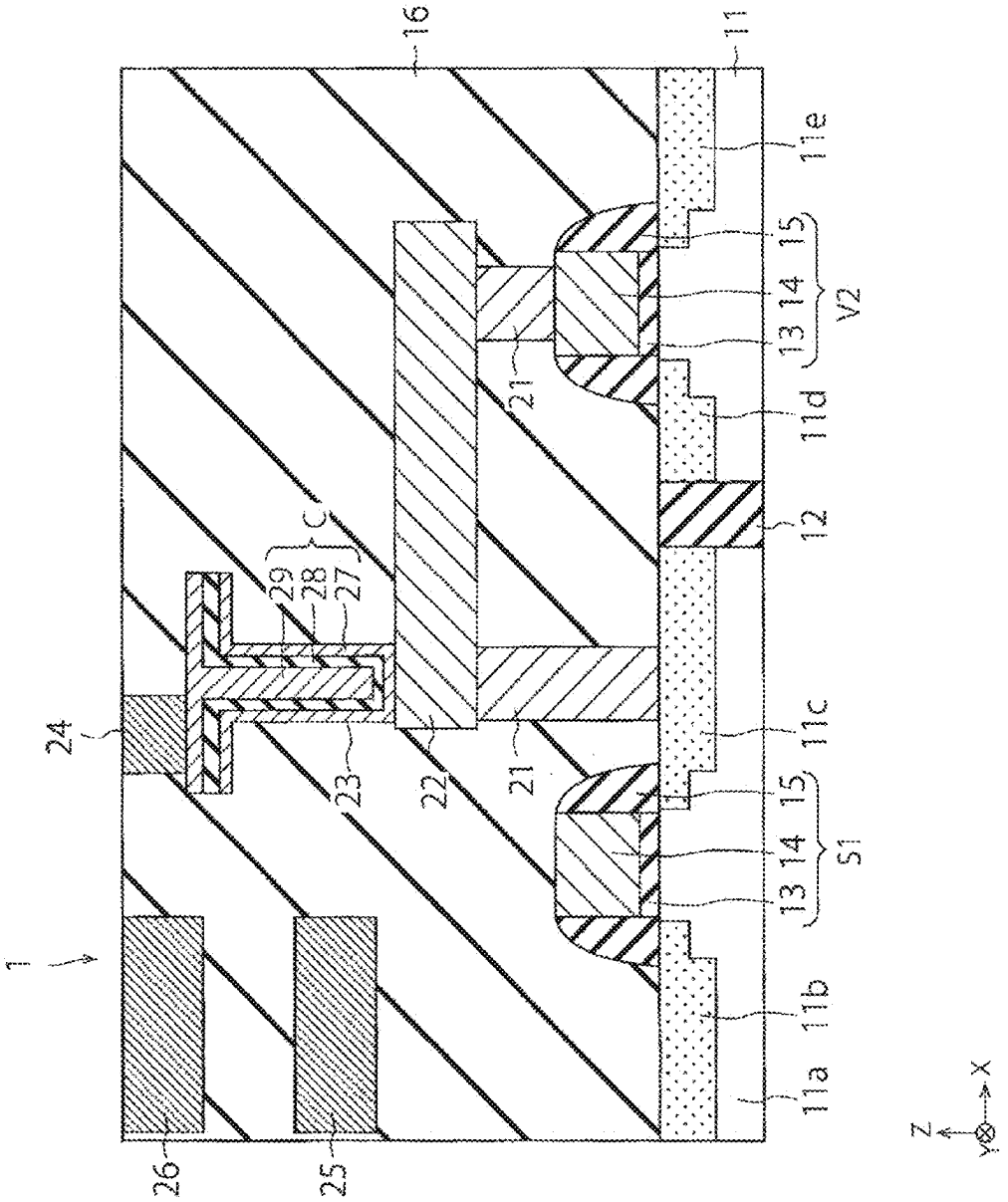

16
11
11e
15
14
13
V2
21
11d
12
C
29
28
27
24
23
22
21
11c
15
14
13
51
1
11b
11a
26
25
Z
X
Y

FIG. 4

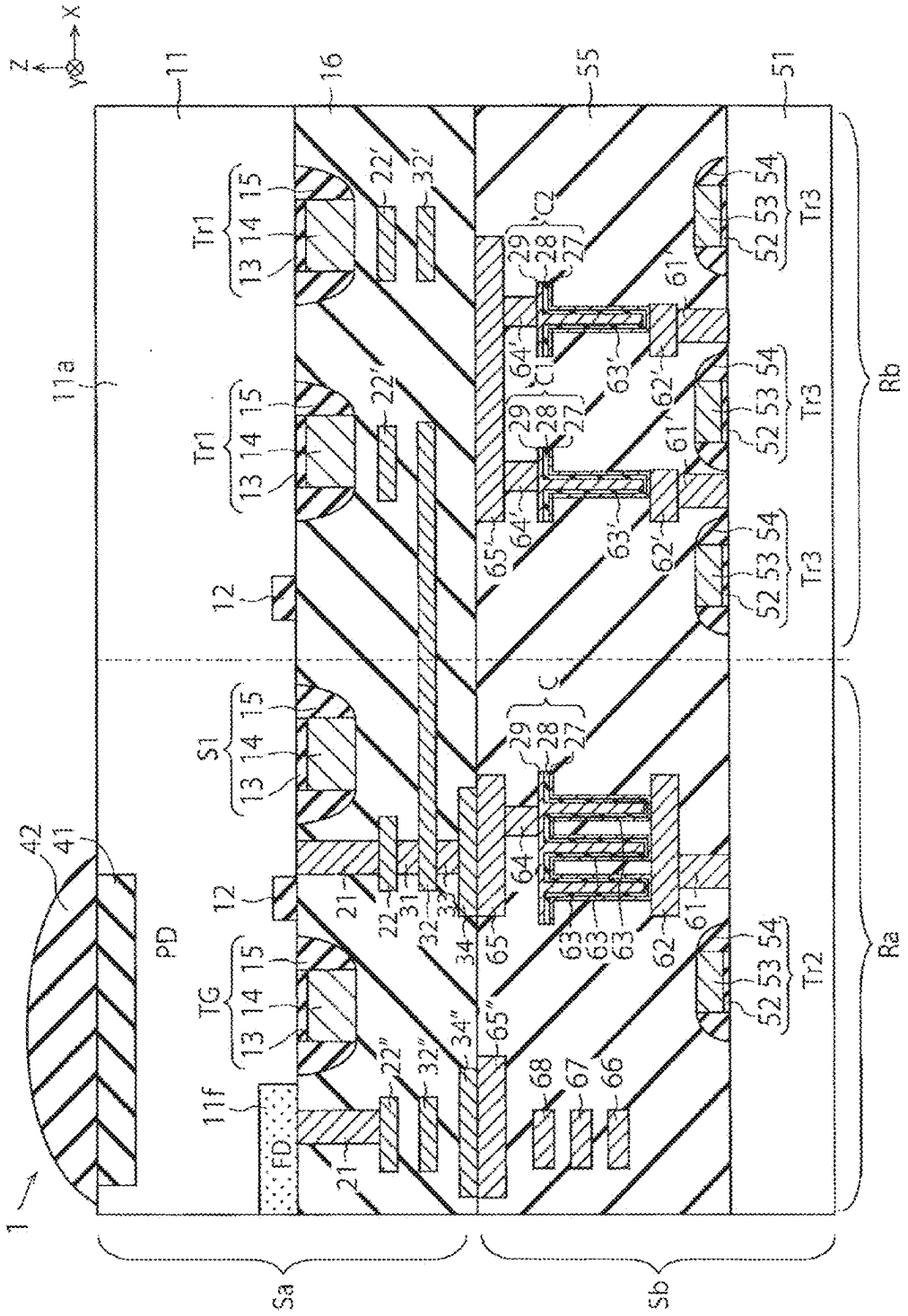

Z
X
Y
11
16
55
51
11a
Tr1
13 14 15
22'
32'
C2
29
28
27
61
64'
C1
63'
62'
52 53 54
Tr3
Rb
65
12
S1
C
21
22
31
33
32
34
64
63
62
61
PD
42
41
TG
22"
32"
34"
65"
11f
FD
68
67
66
Tr2
Ra
1
Sa
Sb

FIG. 5

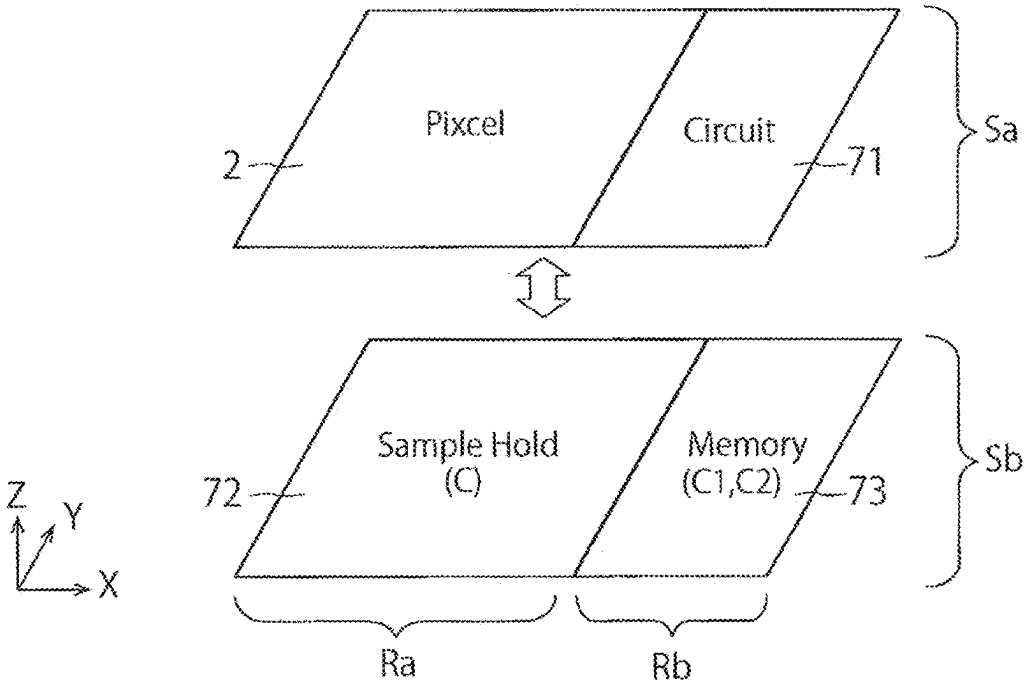

Pixcel
Circuit
2
71
Sa
Sample Hold
(C)
Memory
(C1,C2)
72
73
Sb
Z
Y
X
Ra
Rb

FIG. 6

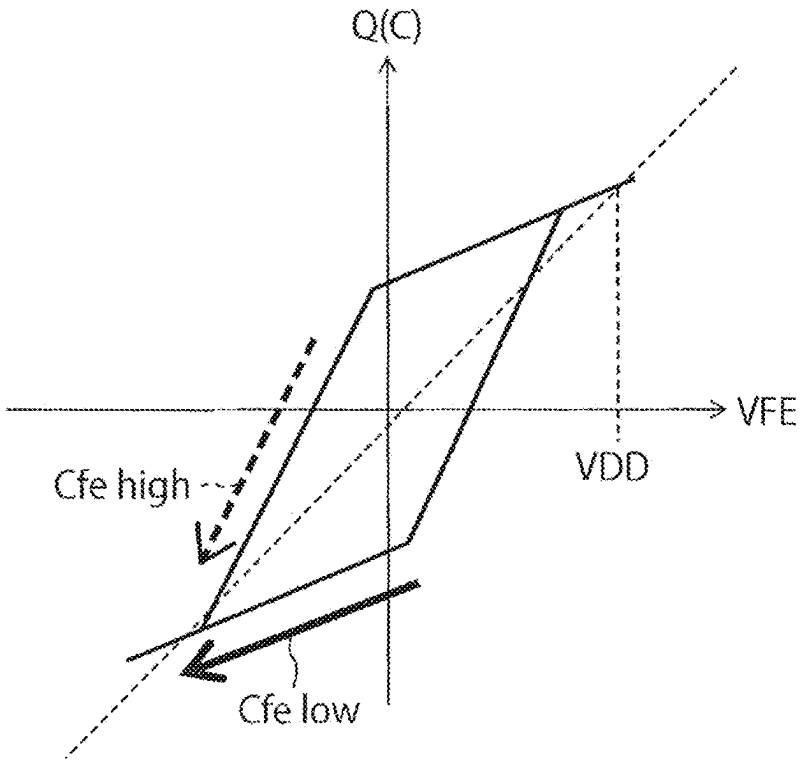


FIG. 7

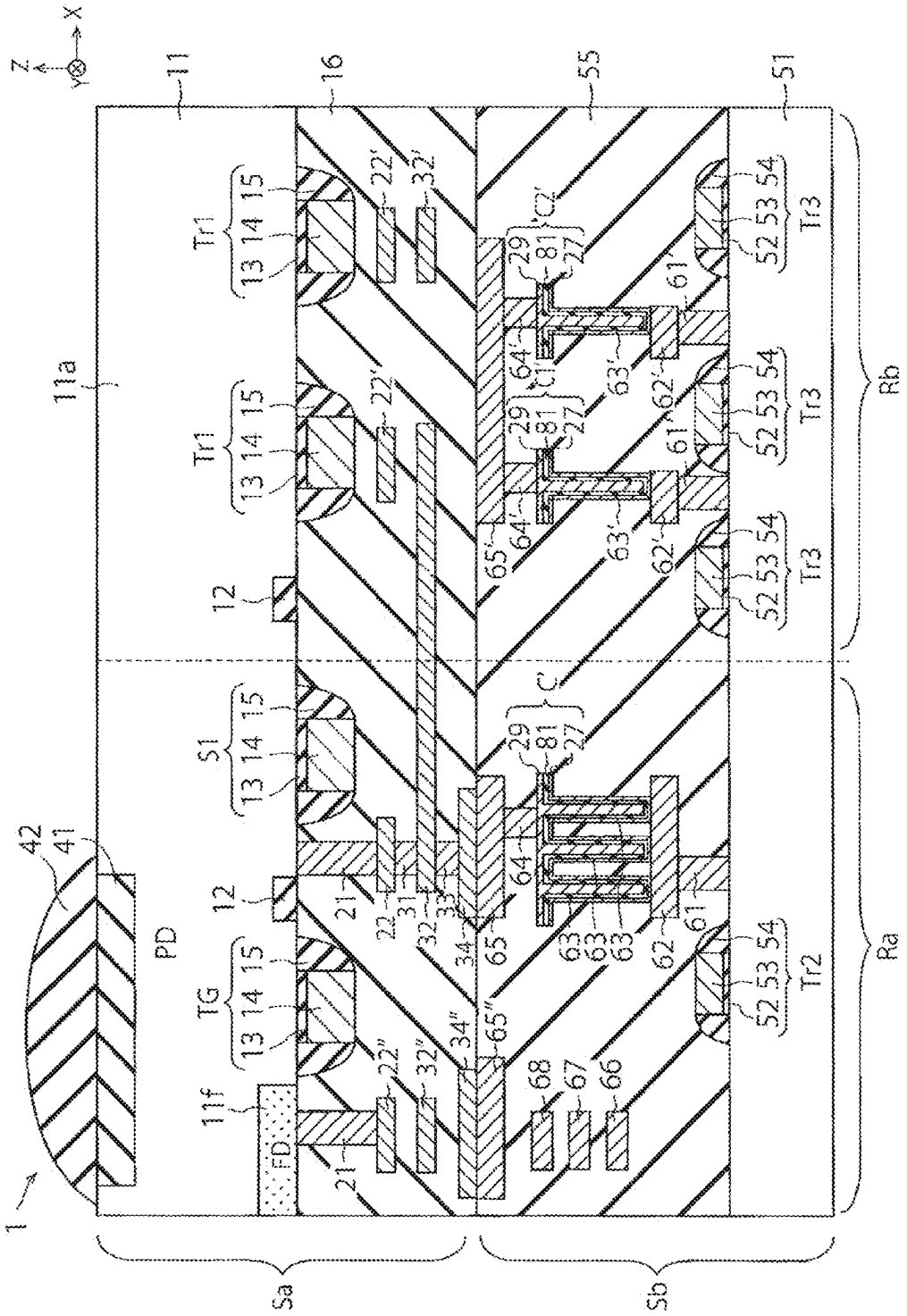

Z
X
Y
11
16
55
51
11a
Tr1
13 14 15
22'
32'
27'
29
81
27
C'
61
64'
63'
62'
52 53 54
Tr3
Rb
12
65'
S1
C
21
22
31
32
33
34
64
63
62
65
PD
42
41
TG
22"
32"
34"
65"
11f
FD
68
67
66
Tr2
Ra
1
Sa
Sb

FIG. 8

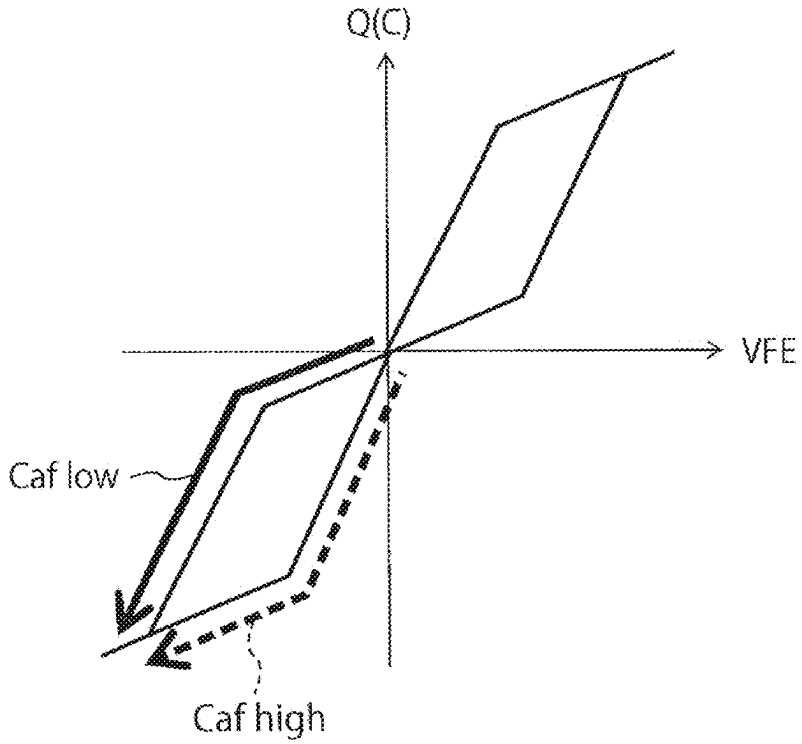


FIG. 9

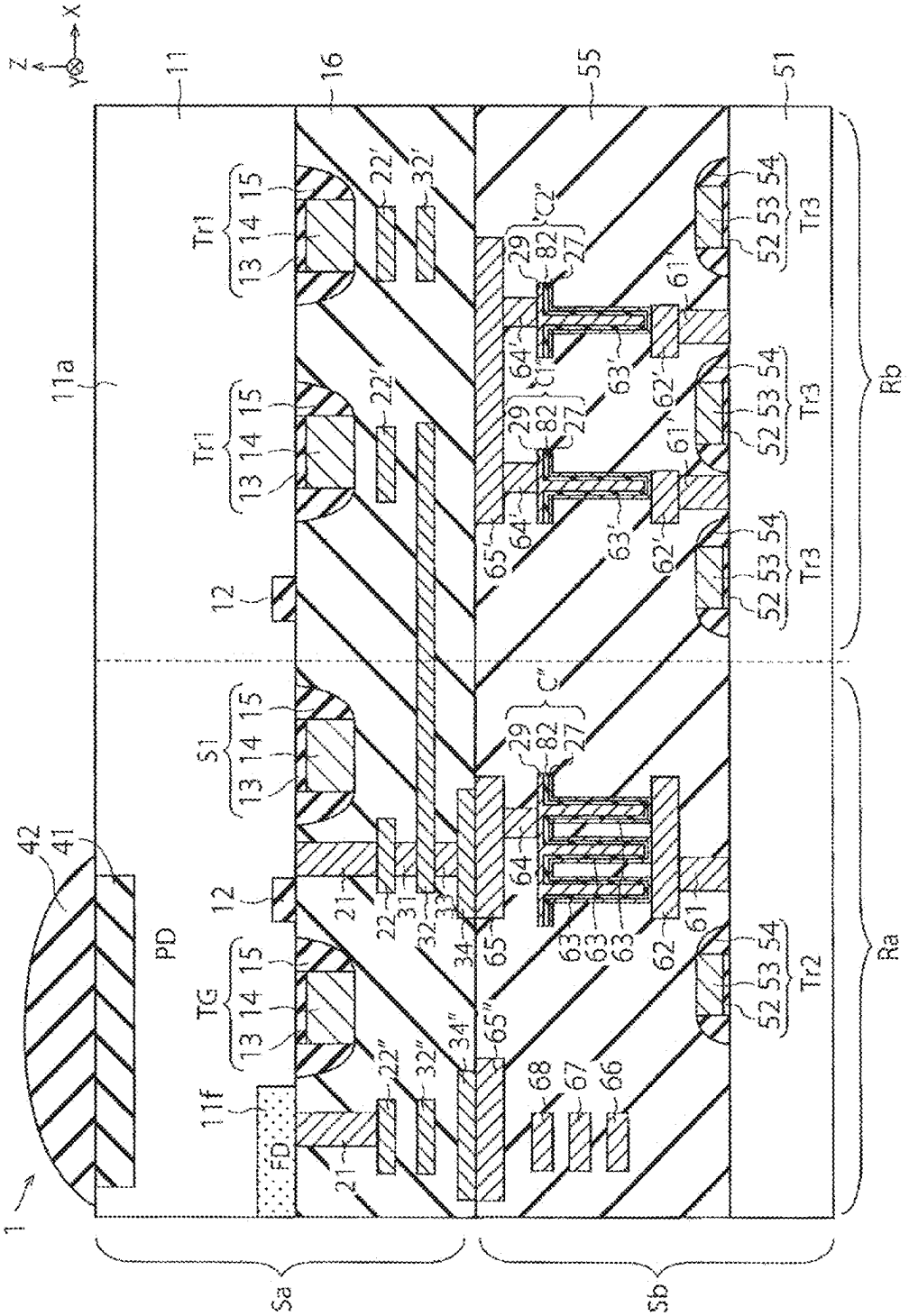

Z
X
Y
11
16
55
51
11a
Tr1
13 14 15
22'
32'
29
82
27
C'
C''
61'
64'
63'
62'
52 53 54
Tr3
Rb
65'
12
51
C''
42
41
PD
21
22
31
32
33
34
64
63
62
61
TG
22''
32''
34''
65''
11f
FD
68
67
66
Tr2
Ra
1
Sa
Sb

FIG. 10

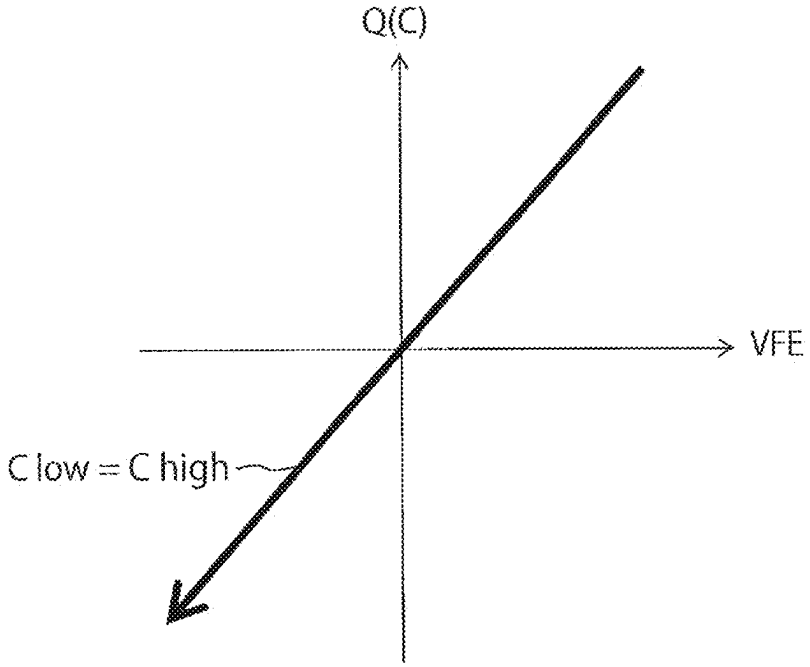


FIG. 11

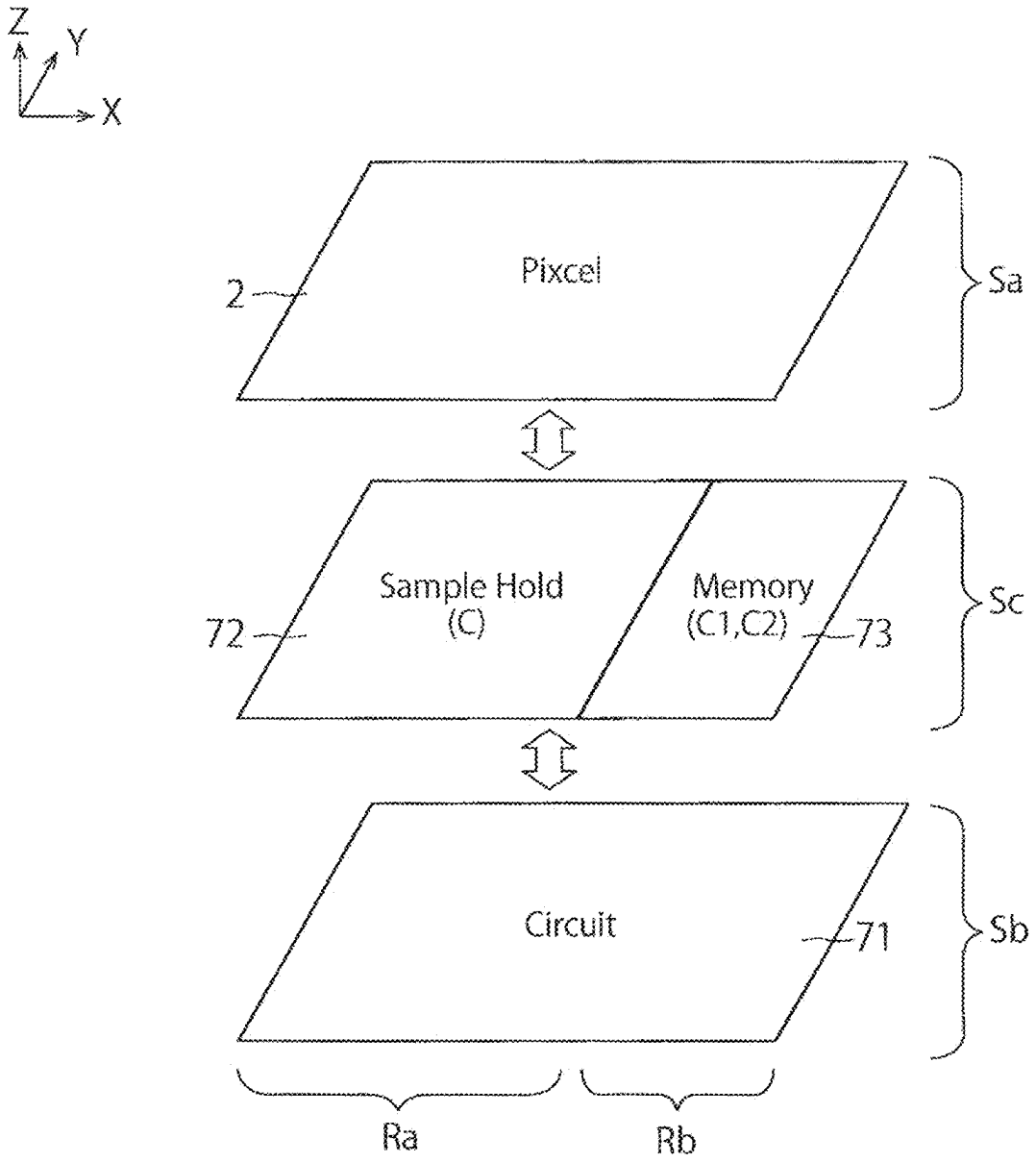

Z
Y
X
Pixcel
2
Sa
Sample Hold
(C)
Memory
(C1,C2)
72
73
Sc
Circuit
71
Sb
Ra
Rb

FIG. 12

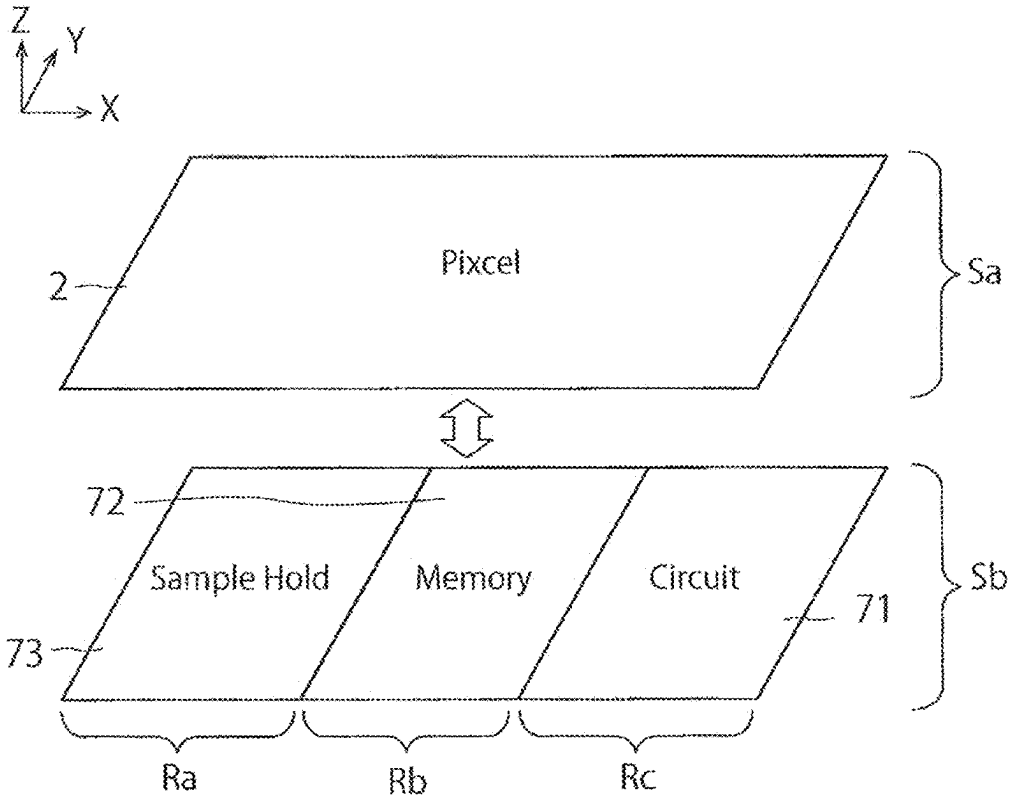


FIG. 13A

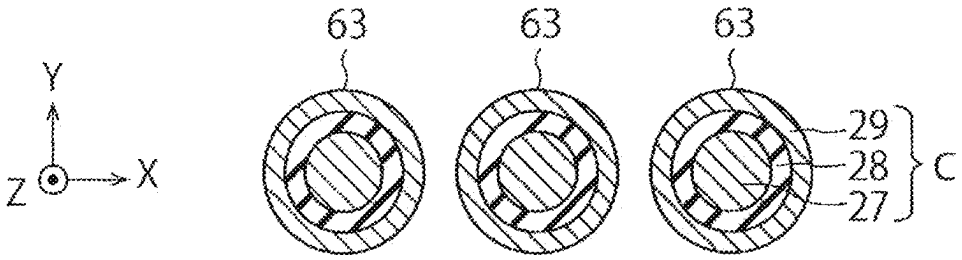


FIG. 13B

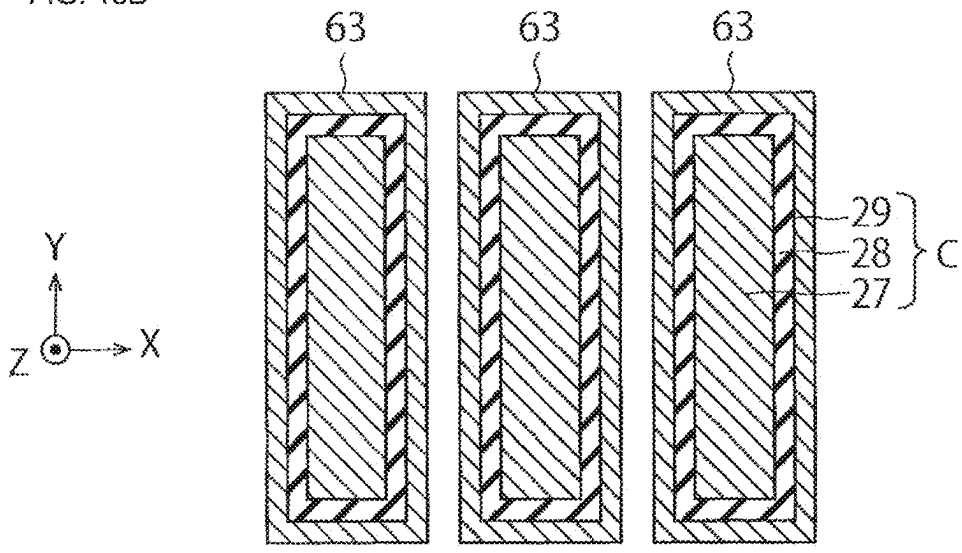


FIG. 14

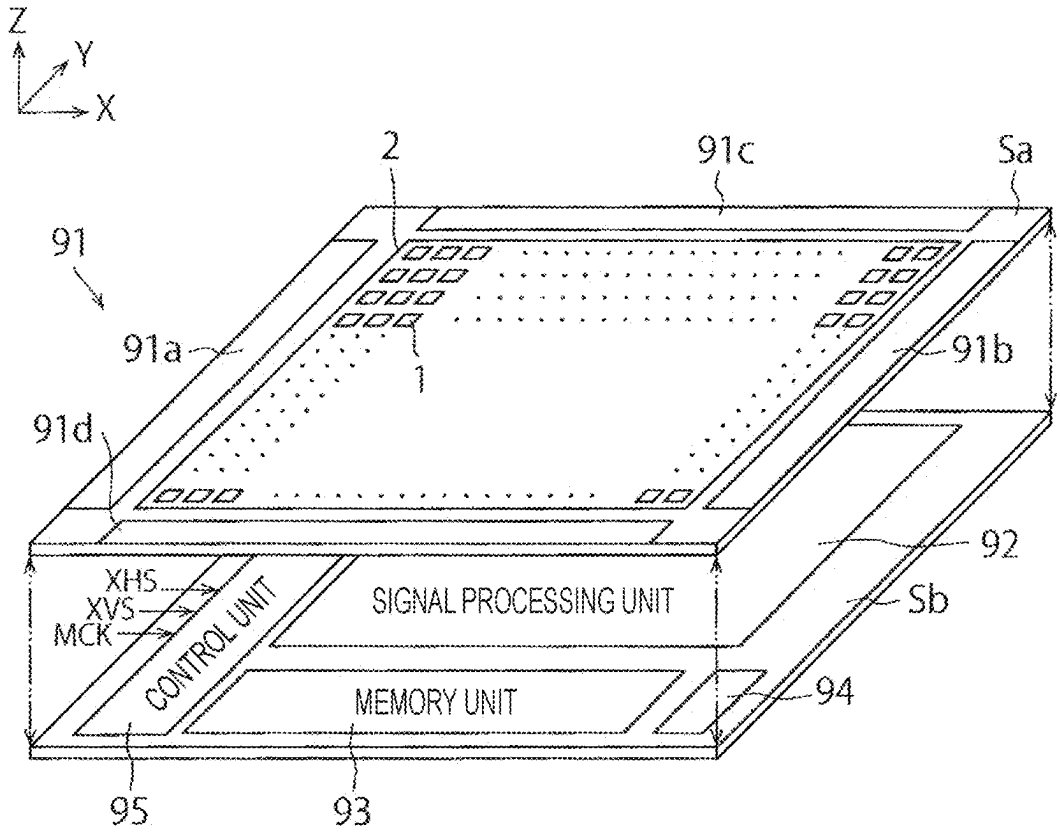

Z
Y
X
2
91c
Sa
91
91a
1
91b
91d
92
XHS
XVS
MCK
CONTROL UNIT
SIGNAL PROCESSING UNIT
Sb
MEMORY UNIT
94
95
93

FIG. 15

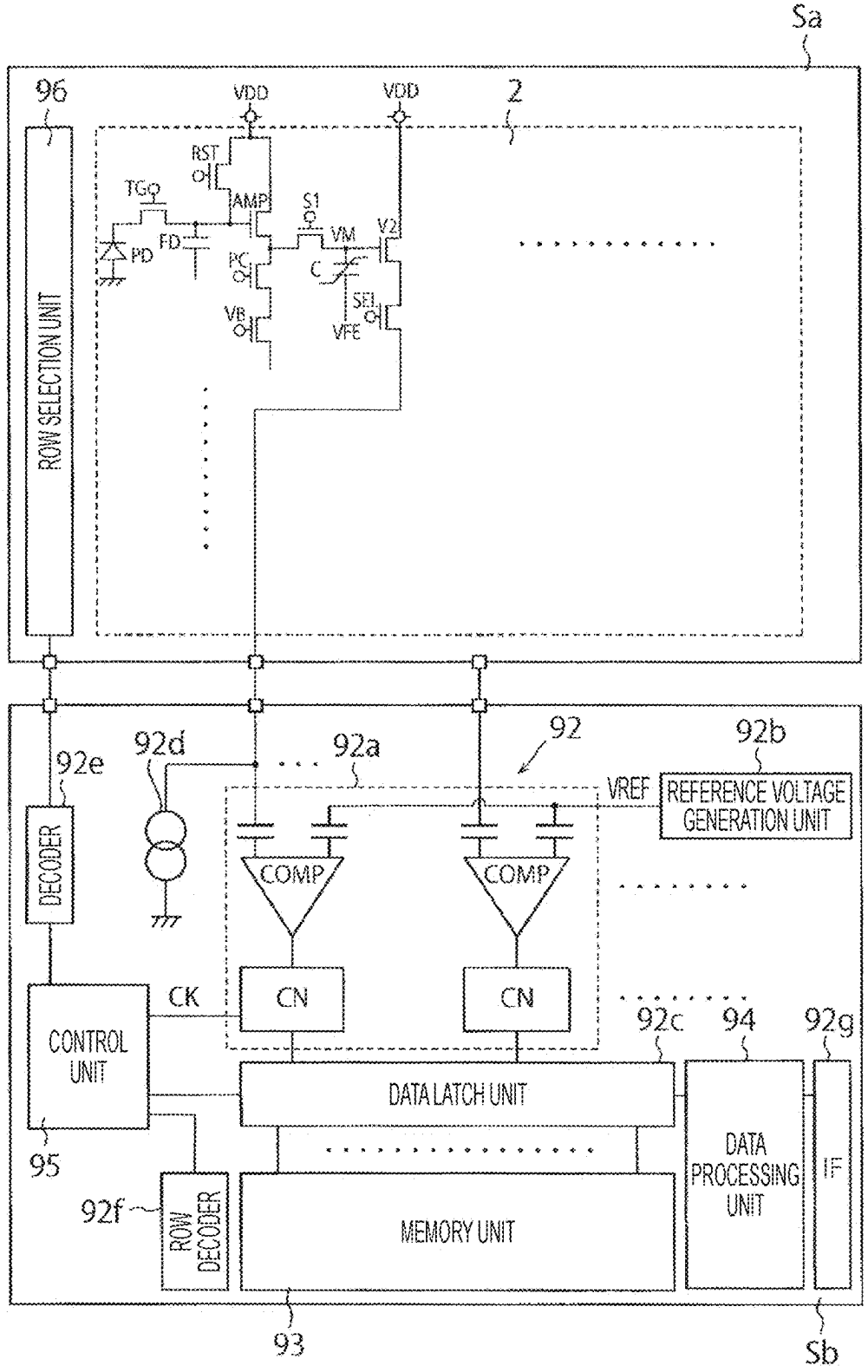

Sa
96
VDD
VDD
2
RST
TGp
AMP
S1
PD
FD
PC
VM
V2
C
SEL
VB
VFE
ROW SELECTION UNIT
92
92b
92d
92a
92e
VREF
REFERENCE VOLTAGE GENERATION UNIT
DECODER
COMP
COMP
CK
CN
CN
CONTROL UNIT
92c
94
92g
DATA LATCH UNIT
95
DATA PROCESSING UNIT
IF
92f
ROW DECODER
MEMORY UNIT
93
Sb

FIG. 16

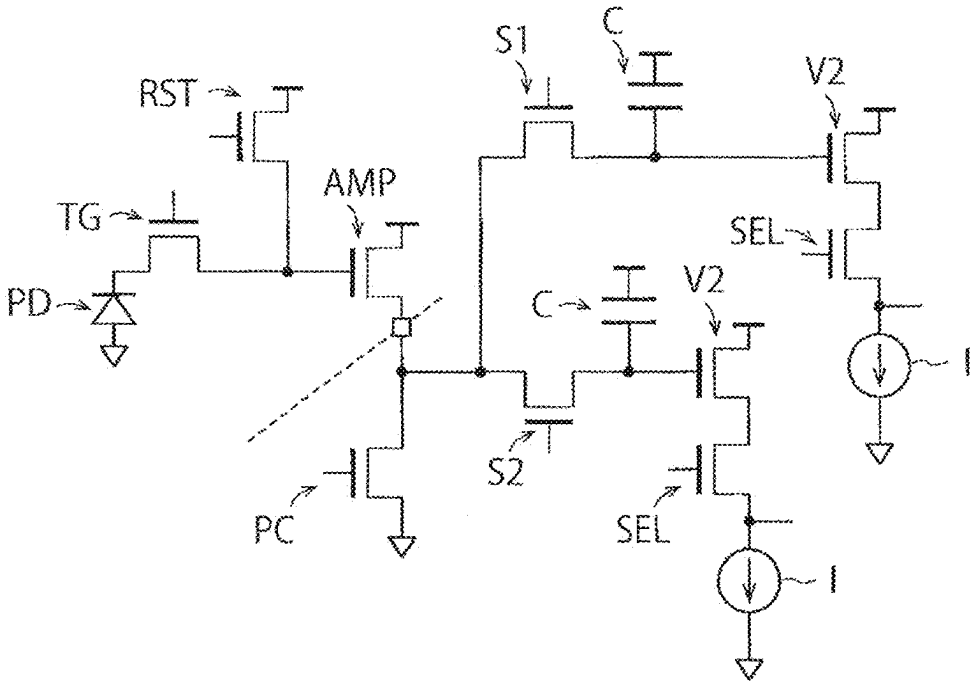


FIG. 17

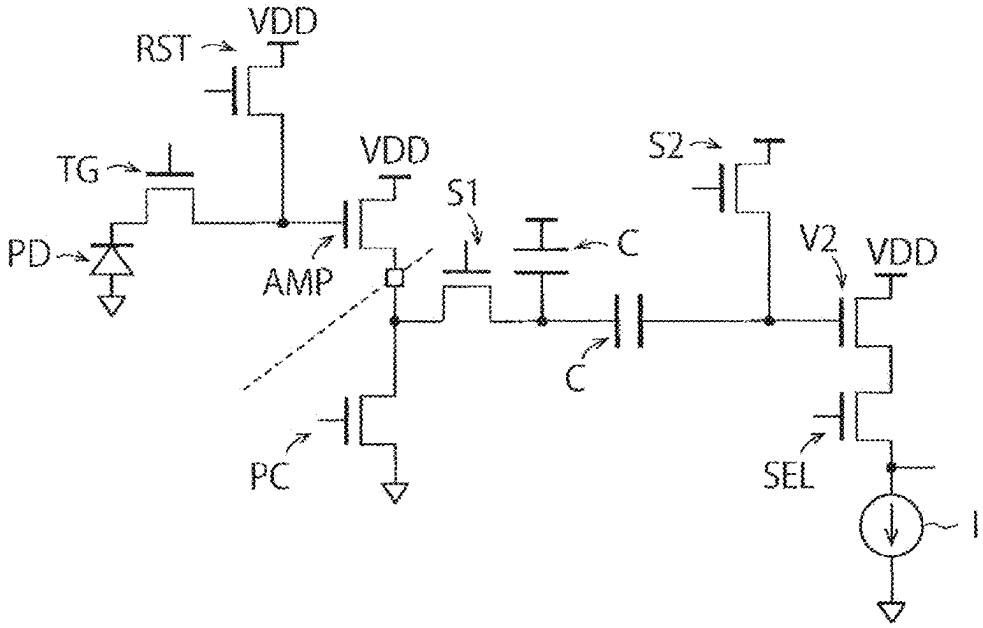


FIG. 18

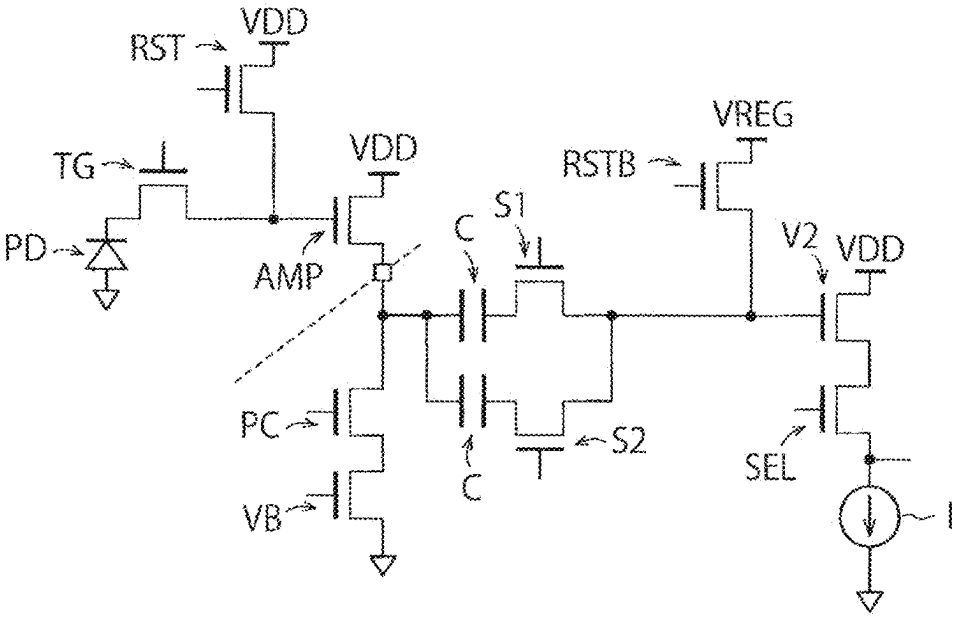


FIG. 19

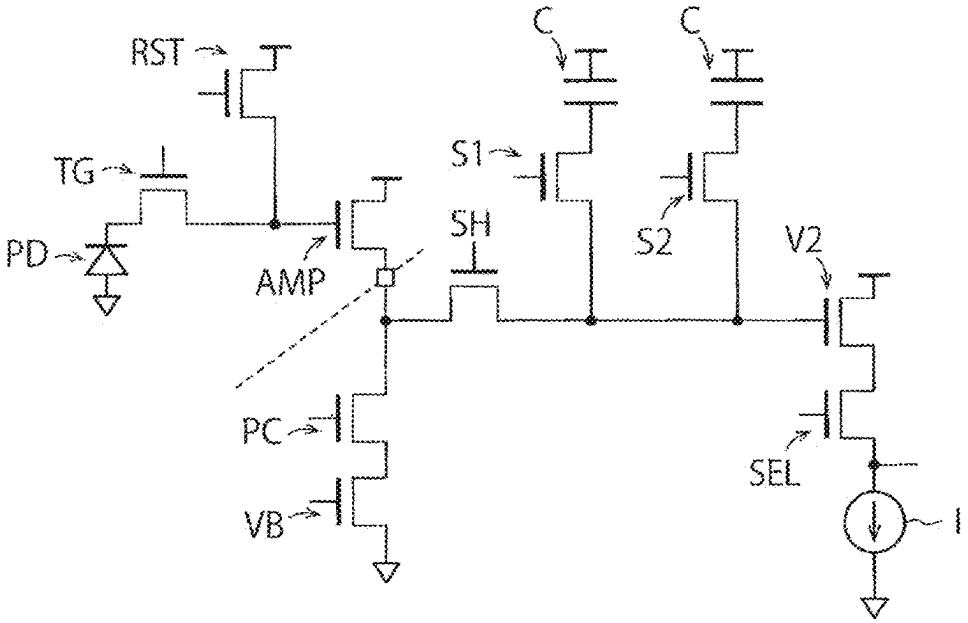


FIG. 20

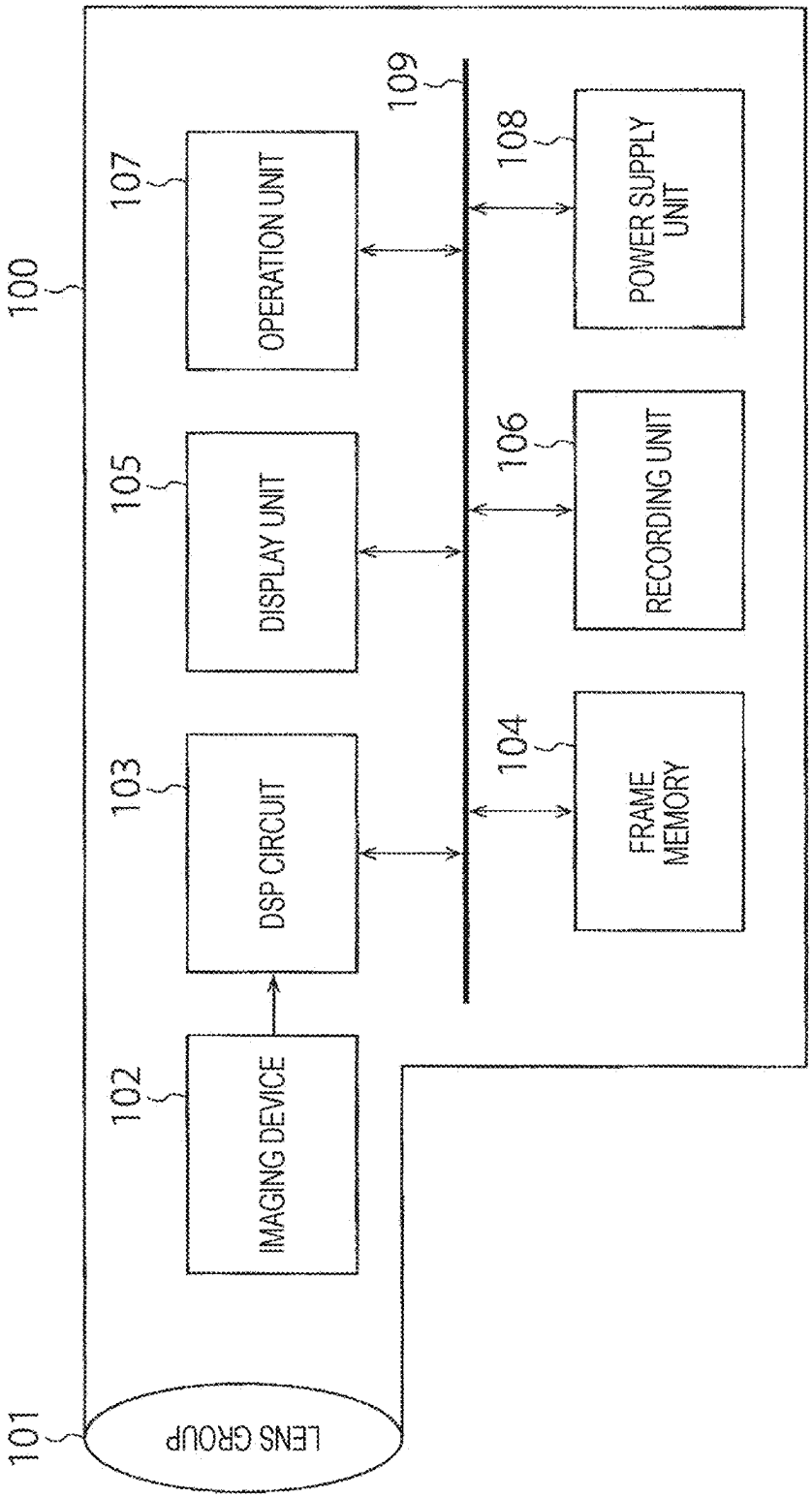

100
101
LENS GROUP
102
IMAGING DEVICE
103
DSP CIRCUIT
104
FRAME MEMORY
105
DISPLAY UNIT
106
RECORDING UNIT
107
OPERATION UNIT
108
POWER SUPPLY UNIT
109

FIG. 21

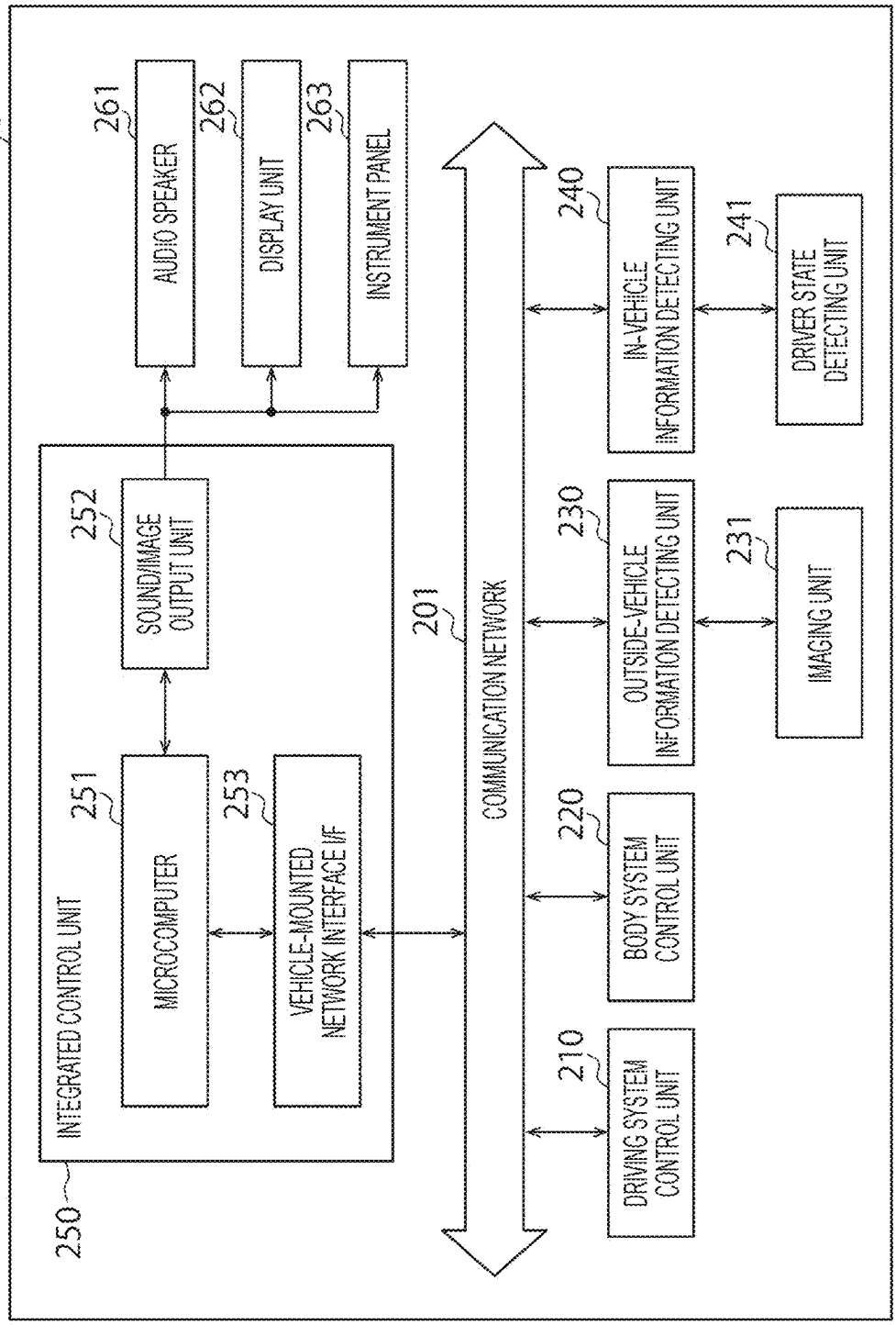

200
261
AUDIO SPEAKER
262
DISPLAY UNIT
263
INSTRUMENT PANEL
252
SOUND/IMAGE OUTPUT UNIT
251
MICROCOMPUTER
253
VEHICLE-MOUNTED NETWORK INTERFACE I/F
INTEGRATED CONTROL UNIT
250
201
COMMUNICATION NETWORK
210
DRIVING SYSTEM CONTROL UNIT
220
BODY SYSTEM CONTROL UNIT
230
OUTSIDE-VEHICLE INFORMATION DETECTING UNIT
231
IMAGING UNIT
240
IN-VEHICLE INFORMATION DETECTING UNIT
241
DRIVER STATE DETECTING UNIT

FIG. 22

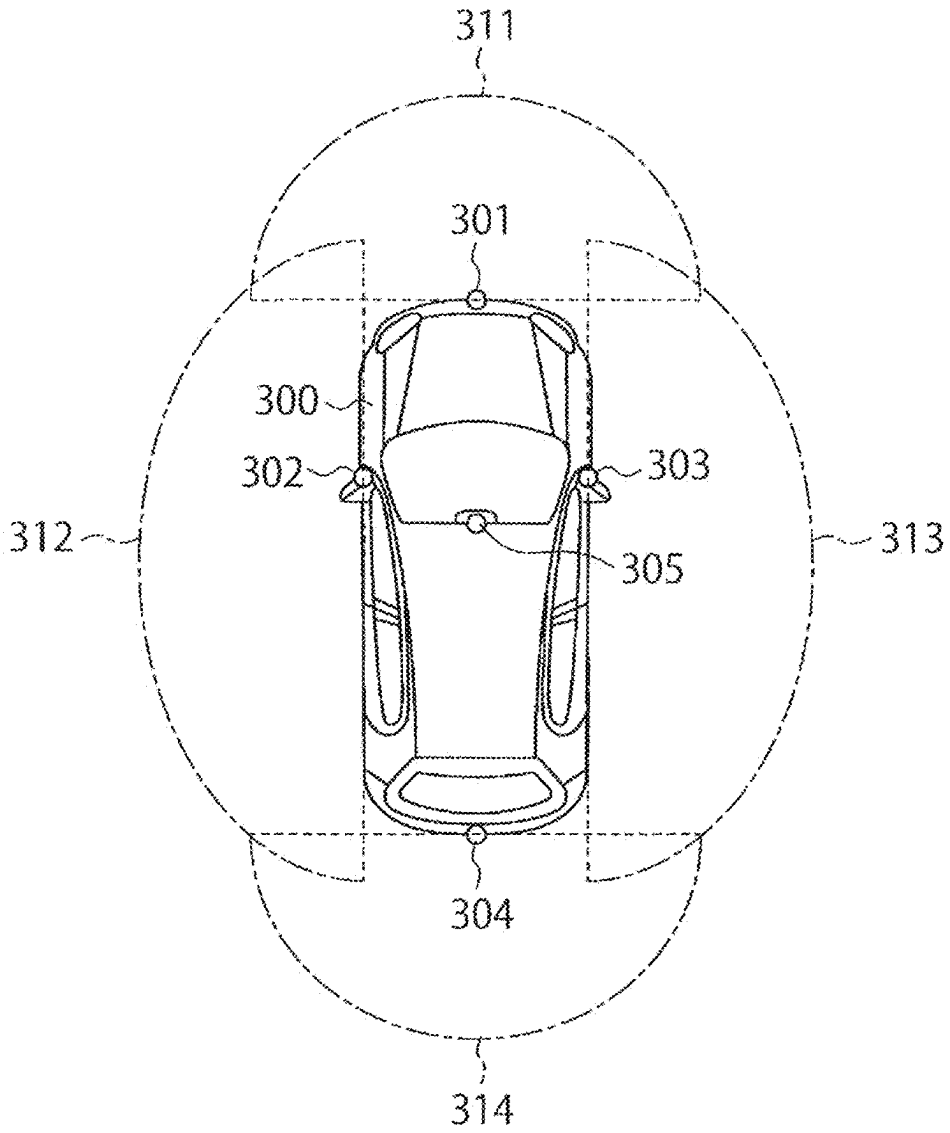


FIG. 23

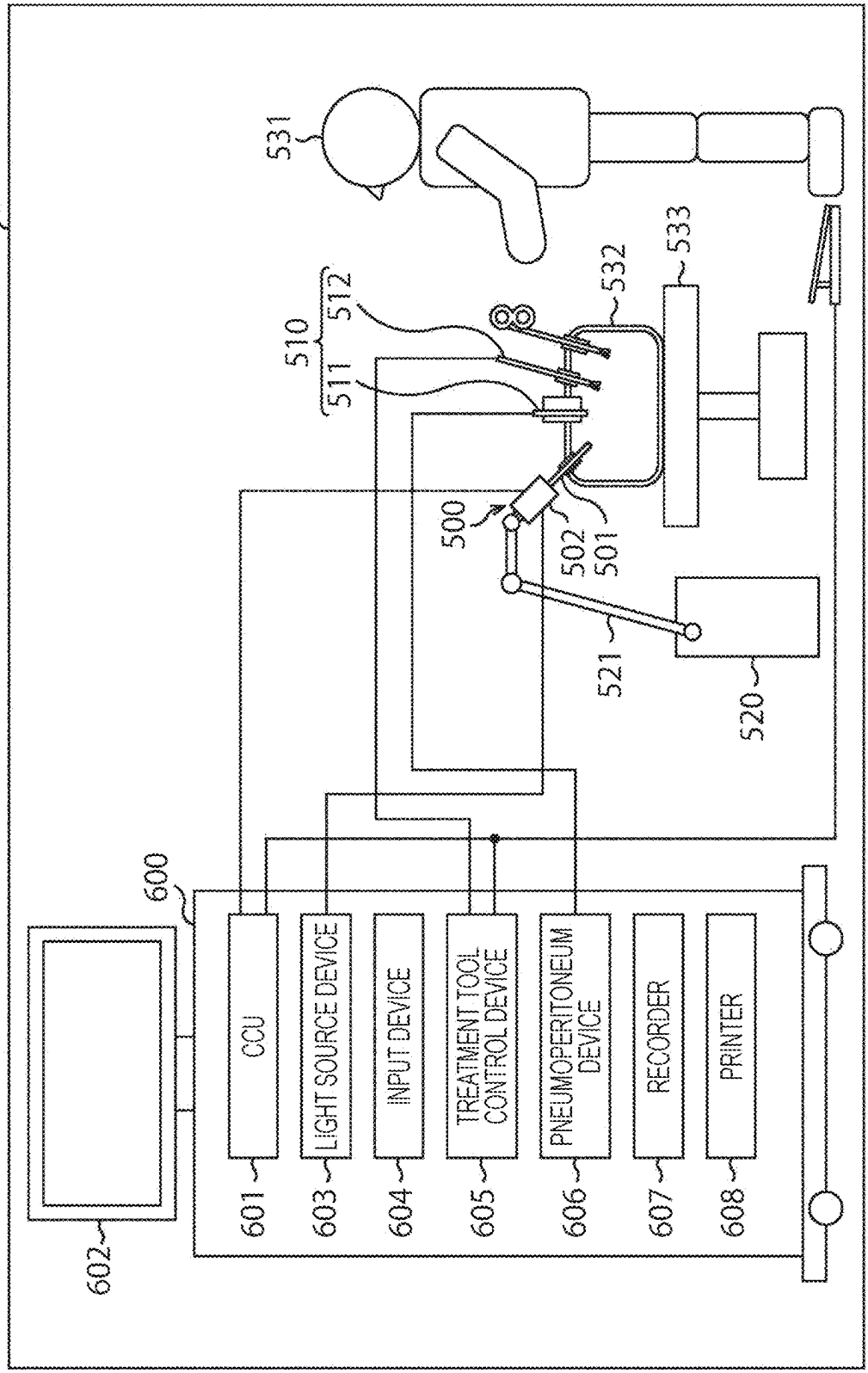
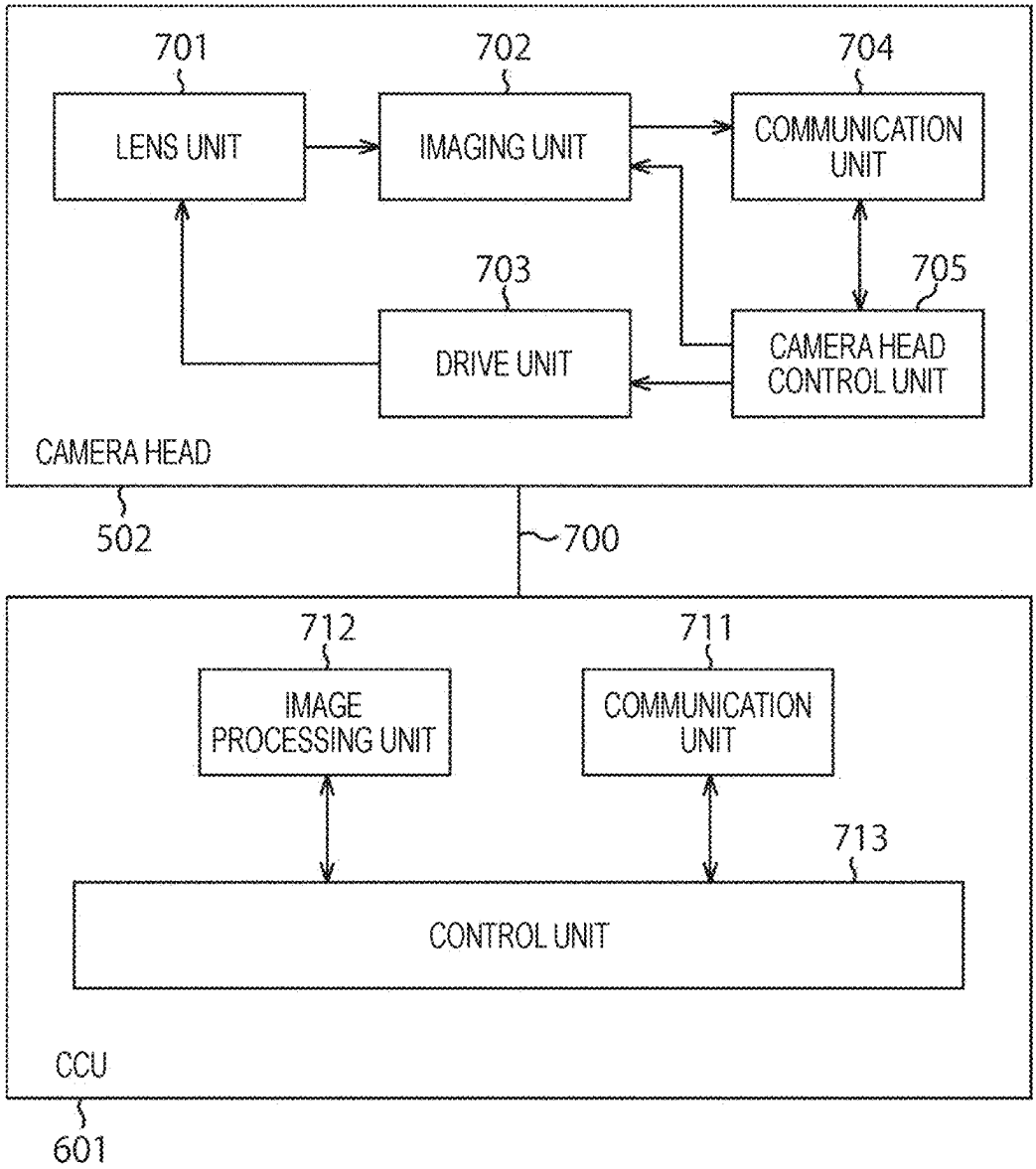

400
531
533
532
512
510
511
500
502
501
521
520
600
602
601
CCU
603
LIGHT SOURCE DEVICE
604
INPUT DEVICE
605
TREATMENT TOOL CONTROL DEVICE
606
PNEUMOPERITONEUM DEVICE
607
RECORDER
608
PRINTER

FIG. 24


701
LENS UNIT
702
IMAGING UNIT
704
COMMUNICATION UNIT
703
DRIVE UNIT
705
CAMERA HEAD CONTROL UNIT
CAMERA HEAD
502
700
712
IMAGE PROCESSING UNIT
711
COMMUNICATION UNIT
713
CONTROL UNIT
CCU
601

SOLID-STATE IMAGING DEVICE

TECHNICAL FIELD

[0001] The present disclosure relates to a solid-state imaging device.

BACKGROUND ART

[0002] A voltage domain type solid-state imaging device realizes a global shutter function by simultaneously converting charges generated in a photodiode into voltages in all pixels and holding the voltages until reading is completed. In this case, charges are simultaneously transferred from the photodiode to a floating diffusion unit in all the pixels, and a current flows through an amplifying transistor simultaneously in all the pixels. The above voltage is held in a capacitor at a post stage of the amplifying transistor. Thereafter, signals are sequentially read from the capacitors of these pixels. Although this capacitor desirably has a large capacity, an increase in the capacity of the capacitor may increase the cost of the solid-state imaging device.

[0003] Furthermore, in order to realize a moving image capturing at a high frame rate and a pseudo global shutter function, a frame memory including a capacitor as a storage element may be provided in the solid-state imaging device. However, when it is attempted to provide a frame memory in a voltage domain type solid-state imaging device, forming both a capacitor and a memory may increase the cost of the solid-state imaging device.

CITATION LIST

Patent Document

[0004] Patent Document 1: U.S. Patent Application Publication No. 2020/0279876

Non-Patent Document

[0005] Non-Patent Document 1: H. Tsugawa et al., IEDM Dig. Tech. Papers, December 2017.

SUMMARY OF THE INVENTION

Problems to be Solved by the Invention

[0006] The present disclosure provides a solid-state imaging device capable of reducing the cost related to a capacitor.

Solutions to Problems

[0007] A solid-state imaging device of a first aspect of the present disclosure includes: a first substrate; a photoelectric conversion unit provided in the first substrate; a floating diffusion unit provided in the first substrate; a pixel transistor electrically connected to the floating diffusion unit; and a capacitor including a first electrode electrically connected or connectable to the pixel transistor, a second electrode different from the first electrode, and a first ferroelectric film or a first antiferroelectric film provided between the first electrode and the second electrode. As a result, for example, it is possible to reduce the cost related to the capacitor, for example, it is possible to form a large-capacity capacitor or a high-performance capacitor at low cost.

[0008] Furthermore, in the first aspect, the pixel transistor may be an amplifying transistor having a gate electrically connected to the floating diffusion unit and a source or a drain electrically connected to or connectable to the first electrode. As a result, for example, the cost related to the capacitor of the voltage domain type solid-state imaging device can be reduced.

[0009] Furthermore, in the first aspect, the first electrode may be electrically connectable to the pixel transistor via a switch transistor. As a result, for example, the cost related to the capacitor of the voltage domain type solid-state imaging device can be reduced.

[0010] Furthermore, in the first aspect, the first ferroelectric film or the first antiferroelectric film may contain hafnium (Hf), zirconium (Zr), niobium (Nb), scandium (Sc), yttrium (Y), lanthanum (La), germanium (Ge), or silicon (Si). Thus, for example, a suitable ferroelectric film or antiferroelectric film can be formed.

[0011] Furthermore, in the first aspect, the capacitor may be provided on a first surface side of the first substrate, and the solid-state imaging device may further include a lens provided on a second surface side of the first substrate. As a result, for example, the capacitor can be applied to a back-illuminated type solid-state imaging device.

[0012] Furthermore, the solid-state imaging device of the first aspect may further include a second substrate bonded to the first substrate, and the pixel transistor and the capacitor may be provided between the first substrate and the second substrate. As a result, for example, the capacitor can be applied to a solid-state imaging device configured using two substrates.

[0013] Furthermore, in the first aspect, the pixel transistor may be provided in a first insulating film provided on the first substrate, and the capacitor may be provided in a second insulating film provided on the second substrate and located between the second substrate and the first insulating film. As a result, for example, the capacitor can be applied to a solid-state imaging device configured using two substrates.

[0014] Furthermore, the solid-state imaging device of the first aspect may further include a third substrate provided between the first substrate and the second substrate, and the capacitor may be provided between the second substrate and the third substrate. As a result, for example, the capacitor can be applied to a solid-state imaging device configured using three substrates.

[0015] Furthermore, in the first aspect, a capacity of the capacitor is controlled to be set to only one of a plurality of types of values. As a result, for example, a capacitor other than the paraelectric capacitor can be used like a paraelectric capacitor.

[0016] Furthermore, the solid-state imaging device of the first aspect may further include a memory including a third electrode and a fourth electrode different from the third electrode, and the memory may include a second ferroelectric film between the third electrode and the fourth electrode in a case where the capacitor includes the first ferroelectric film, and includes a second antiferroelectric film between the third electrode and the fourth electrode in a case where the capacitor includes the first antiferroelectric film. As a result, for example, the total cost of the capacitor and the memory can be reduced by simultaneously forming the capacitor and the memory.

[0017] Furthermore, in the first aspect, the third electrode may be formed of the same material as the first electrode, the fourth electrode may be formed of the same material as the second electrode, and the second ferroelectric film or the second antiferroelectric film may be formed of the same

material as the first ferroelectric film or the first antiferroelectric film. As a result, for example, the total cost of the capacitor and the memory can be reduced by forming the capacitor and the memory with the same material.

[0018] A solid-state imaging device of a second aspect of the present disclosure includes: a first substrate; a photoelectric conversion unit provided in the first substrate; a floating diffusion unit provided in the first substrate; a capacitor including a first electrode provided on a first surface side or a second surface side of the first substrate, a second electrode different from the first electrode, and a first ferroelectric film, a first antiferroelectric film, or a first paraelectric film provided between the first electrode and the second electrode; and a memory including a third electrode and a fourth electrode different from the third electrode, in which the memory includes a second ferroelectric film between the third electrode and the fourth electrode in a case where the capacitor includes the first ferroelectric film, includes a second antiferroelectric film between the third electrode and the fourth electrode in a case where the capacitor includes the first antiferroelectric film, and includes a second paraelectric film between the third electrode and the fourth electrode in a case where the capacitor includes the first paraelectric film. As a result, for example, the total cost of the capacitor and the memory can be reduced by simultaneously forming the capacitor and the memory, and the cost related to the capacitor can be reduced.

[0019] Furthermore, in the second aspect, the third electrode may be formed of the same material as the first electrode, the fourth electrode may be formed of the same material as the second electrode, and the second ferroelectric film, the second antiferroelectric film, or the second paraelectric film may be formed of the same material as the first ferroelectric film, the first antiferroelectric film, or the second paraelectric film. As a result, for example, the total cost of the capacitor and the memory can be reduced by forming the capacitor and the memory with the same material.

[0020] Furthermore, in the second aspect, the first and second ferroelectric films, the first and second antiferroelectric films, or the first and second paraelectric films may contain hafnium (Hf), zirconium (Zr), niobium (Nb), scandium (Sc), yttrium (Y), lanthanum (La), germanium (Ge), or silicon (Si). Thus, for example, a suitable ferroelectric film, antiferroelectric film, or paraelectric film can be formed.

[0021] Furthermore, in the second aspect, the capacitor and the memory may be provided on the first surface side of the first substrate, and the solid-state imaging device may further include a lens provided on the second surface side of the first substrate. As a result, for example, the capacitor and the memory can be applied to a back-illuminated type solid-state imaging device.

[0022] Furthermore, the solid-state imaging device of the second aspect may further include a pixel transistor electrically connected to the floating diffusion unit, and the first electrode may be electrically connected or connectable to the pixel transistor. As a result, for example, the cost related to the capacitor of the solid-state imaging device including such a pixel transistor can be reduced.

[0023] Furthermore, the solid-state imaging device of the second aspect may further include a second substrate bonded to the first substrate, and the pixel transistor, the capacitor, and the memory may be provided between the first substrate and the second substrate. As a result, for example, the capacitor and the memory can be applied to a solid-state imaging device configured using two substrates.

[0024] Furthermore, in the second aspect, the pixel transistor may be provided in a first insulating film provided on the first substrate, and the capacitor and the memory may be provided in a second insulating film provided on the second substrate and located between the second substrate and the first insulating film. As a result, for example, the capacitor and the memory can be applied to a solid-state imaging device configured using two substrates.

[0025] Furthermore, the solid-state imaging device of the second aspect may further include a third substrate provided between the first substrate and the second substrate, and the capacitor and the memory may be provided between the second substrate and the third substrate. As a result, for example, the capacitor and the memory can be applied to a solid-state imaging device configured using three substrates.

[0026] Furthermore, in the second aspect, the capacitor and the memory may have a portion provided in the same cross section. As a result, for example, the capacitor and the memory can be formed at substantially the same height at the same time.

BRIEF DESCRIPTION OF DRAWINGS

[0027] FIG. **1** is a block diagram illustrating a configuration of a solid-state imaging device of a first embodiment.

[0028] FIG. **2** is a circuit diagram showing a configuration of the solid-state imaging device of the first embodiment.

[0029] FIG. **3** is a cross-sectional view illustrating a first example of a structure of the solid-state imaging device of the first embodiment.

[0030] FIG. **4** is a cross-sectional view illustrating a second example of the structure of the solid-state imaging device of the first embodiment.

[0031] FIG. **5** is a perspective view illustrating the structure of the solid-state imaging device illustrated in FIG. **4**.

[0032] FIG. **6** is a graph for explaining the operation of the solid-state imaging device of the first embodiment.

[0033] FIG. **7** is a cross-sectional view illustrating a structure of a solid-state imaging device of a second embodiment.

[0034] FIG. **8** is a graph for explaining the operation of the solid-state imaging device of the second embodiment.

[0035] FIG. **9** is a cross-sectional view illustrating a structure of a solid-state imaging device of a third embodiment.

[0036] FIG. **10** is a graph for explaining the operation of the solid-state imaging device of the third embodiment.

[0037] FIG. **11** is a perspective view illustrating a structure of a solid-state imaging device of a fourth embodiment.

[0038] FIG. **12** is a perspective view illustrating a structure of a solid-state imaging device of a fifth embodiment.

[0039] FIG. **13** is a transverse cross-sectional view illustrating two examples of a structure of a solid-state imaging device of a sixth embodiment.

[0040] FIG. **14** is a perspective view illustrating a structure of a solid-state imaging device of a seventh embodiment.

[0041] FIG. **15** is a block diagram illustrating a configuration of the solid-state imaging device of the seventh embodiment.

[0042] FIG. **16** is a circuit diagram showing a configuration of a solid-state imaging device of an eighth embodiment.

[0043] FIG. **17** is a circuit diagram showing a configuration of a solid-state imaging device of a ninth embodiment.

[0044] FIG. **18** is a circuit diagram showing a configuration of a solid-state imaging device of a tenth embodiment.

[0045] FIG. **19** is a circuit diagram showing a configuration of a solid-state imaging device of an eleventh embodiment.

[0046] FIG. **20** is a block diagram illustrating a configuration example of an electronic device.

[0047] FIG. **21** is a block diagram illustrating a configuration example of a moving body control system.

[0048] FIG. **22** is a plan view illustrating a specific example of a setting position of an imaging unit in FIG. **21**.

[0049] FIG. **23** is a view illustrating an example of a schematic configuration of an endoscopic surgery system.

[0050] FIG. **24** is a block diagram illustrating an example of a functional configuration of a camera head and a camera control unit (CCU).

MODE FOR CARRYING OUT THE INVENTION

[0051] Hereinafter, embodiments of the present disclosure are described below with reference to the drawings.

First Embodiment

[0052] FIG. **1** is a block diagram illustrating a configuration of a solid-state imaging device of a first embodiment.

[0053] The solid-state imaging device in FIG. **1** is a complementary metal oxide semiconductor (CMOS) type image sensor (CIS), and includes a pixel array region **2** having a plurality of pixels **1**, a control circuit **3**, a vertical drive circuit **4**, a plurality of column signal processing circuits **5**, a horizontal drive circuit **6**, an output circuit **7**, a plurality of vertical signal lines (VSL) **8**, and a horizontal signal line (HSL) **9**.

[0054] Each of the pixels **1** includes a photodiode functioning as a photoelectric conversion unit and a MOS transistor functioning as a pixel transistor. Examples of the pixel transistor include a transfer transistor, a reset transistor, an amplifying transistor, a selection transistor, and a switch transistor. These pixel transistors may be shared by several pixels **1**.

[0055] The pixel array region **2** includes a plurality of pixels **1** arranged in a two-dimensional array. The pixel array region **2** includes an effective pixel region that receives light, performs photoelectric conversion, and outputs a signal charge generated by the photoelectric conversion, and a black reference pixel region that outputs optical black serving as a reference of a black level. In general, the black reference pixel region is arranged on an outer peripheral portion of the effective pixel region.

[0056] The control circuit **3** generates various signals serving as references of operations of the vertical drive circuit **4**, the column signal processing circuit **5**, the horizontal drive circuit **6**, and the like on the basis of a vertical synchronization signal, a horizontal synchronization signal, a master clock, and the like. The signals generated by the control circuit **3** are, for example, a clock signal and a control signal, and are input to the vertical drive circuit **4**, the column signal processing circuit **5**, the horizontal drive circuit **6**, and the like.

[0057] The vertical drive circuit **4** includes, for example, a shift register, and scans each of the pixels **1** in the pixel array region **2** in the vertical direction row by row. The vertical drive circuit **4** further supplies a pixel signal based on the signal charge generated by each pixel **1** to the column signal processing circuit **5** through the vertical signal line **8**.

[0058] The column signal processing circuit **5** is arranged, for example, for every column of the pixels **1** in the pixel array region **2**, and performs signal processing of the signals output from the pixels **1** of one row for every column on the basis of a signal from the black reference pixel region. Examples of this signal processing are noise removal and signal amplification.

[0059] The horizontal drive circuit **6** includes, for example, a shift register, and supplies the pixel signal from each of the column signal processing circuits **5** to the horizontal signal line **9**.

[0060] The output circuit **7** performs signal processing on the signal supplied from each of the column signal processing circuits **5** through the horizontal signal line **9**, and outputs the signal subjected to the signal processing.

[0061] Note that the pixel array region **2** of the present embodiment may include only one of the pixel **1** that detects visible light and the pixel **1** that detects light other than visible light, or may include both the pixel **1** that detects visible light and the pixel **1** that detects light other than visible light. The light other than the visible light is, for example, infrared light.

[0062] FIG. **2** is a circuit diagram illustrating a configuration of the solid-state imaging device of the first embodiment.

[0063] As illustrated in FIG. **2**, each pixel **1** includes a photodiode PD, a floating diffusion unit FD, a ferroelectric capacitor C, a transfer transistor TG, a reset transistor RST, an amplifying transistor AMP, a selection transistor SEL, a switch transistor S**1**, a post-amplifying transistor V**2**, a current source transistor PC, and a post-current source transistor VB. The solid-state imaging device of the present embodiment is a voltage domain type CIS (VD-GS) that realizes a global shutter function by simultaneously converting charges generated in the photodiodes PD into voltages in all the pixels **1** and holding the voltages until reading is completed.

[0064] The photodiode PD performs photoelectric conversion of incident light. The anode of the photodiode PD is electrically connected to the ground potential, and the cathode of the photodiode PD is electrically connected to the transfer transistor TG. Incident light into the photodiode PD is referred to as exposure of the photodiode PD.

[0065] The transfer transistor TG transfers the charge generated by the photoelectric conversion to the floating diffusion unit FD. One of the source and the drain of the transfer transistor TG is electrically connected to the photodiode PD, and the other of the source and the drain of the transfer transistor TG is electrically connected to the floating diffusion unit FD, the reset transistor RST, and the amplifying transistor AMP.

[0066] The floating diffusion unit FD accumulates the charge transferred by the transfer transistor TG. As illustrated in FIG. **2**, the floating diffusion unit FD functions as a capacitor. The floating diffusion unit FD is electrically connected to the transfer transistor TG, the reset transistor RST, and the amplifying transistor AMP.

[0067] The reset transistor RST discharges charges from the floating diffusion unit FD and resets the potential of the floating diffusion unit FD to the power supply voltage (VDD) before the exposure of the photodiode PD is started. One of the source and the drain of the reset transistor RST

is electrically connected to the power supply voltage, and the other of the source and the drain of the reset transistor RST is electrically connected to the transfer transistor TG, the floating diffusion unit FD, and the amplifying transistor AMP.

[0068] The amplifying transistor AMP receives the charge transferred to the floating diffusion unit FD at the gate, and outputs the charge to the switch transistor **S1** by the source follower. The gate of the amplifying transistor AMP is electrically connected to the transfer transistor TG, the floating diffusion unit FD, and the reset transistor RST. One of the source and the drain of the amplifying transistor AMP is electrically connected to the power supply voltage, and the other of the source and the drain of the amplifying transistor AMP is electrically connected to the switch transistor **S1** and the current source transistor PC.

[0069] The switch transistor **S1** can electrically connect the amplifying transistor AMP and the post-amplifying transistor **V2**. When the switch transistor **S1** is turned on, the amplifying transistor AMP and the post-amplifying transistor **V2** are electrically connected, and when the switch transistor **S1** is turned off, the amplifying transistor AMP and the post-amplifying transistor **V2** are electrically insulated. One of the source and the drain of the switch transistor **S1** is electrically connected to the amplifying transistor AMP and the current source transistor PC, and the other of the source and the drain of the switch transistor **S1** is electrically connected to the ferroelectric capacitor C and the post-amplifying transistor **V2**.

[0070] The post-amplifying transistor **V2** receives the charge output from the amplifying transistor AMP at the gate, and outputs the charge to the vertical signal line **8** by the source follower. The gate of the post-amplifying transistor **V2** is electrically connected to the switch transistor **S1** and the ferroelectric capacitor C. One of the source and the drain of the post-amplifying transistor **V2** is electrically connected to the power supply voltage, and the other of the source and the drain of the post-amplifying transistor **V2** is electrically connected to the selection transistor SEL.

[0071] The selection transistor SEL can electrically connect the post-amplifying transistor **V2** and the vertical signal line **8**. When the selection transistor SEL is turned on, the post-amplifying transistor **V2** and the vertical signal line **8** are electrically connected, and when the selection transistor SEL is turned off, the post-amplifying transistor **V2** and the vertical signal line **8** are electrically insulated. One of the source and the drain of the selection transistor SEL is electrically connected to the post-amplifying transistor **V2**, and the other of the source and the drain of the selection transistor SEL is electrically connected to or connectable to the vertical signal line **8**.

[0072] FIG. **2** illustrates a node VM between the switch transistor **S1**, the ferroelectric capacitor C, and the selection transistor SEL. The gate of the post-amplifying transistor **V2** is electrically connected to the node VM, and the operation of the post-amplifying transistor **V2** is controlled by the voltage of the node VM.

[0073] The current source transistor PC and the post-current source transistor VB function as current sources. One of the source and the drain of the current source transistor PC is electrically connected to the amplifying transistor AMP, and the other of the source and the drain of the current source transistor PC is electrically connected to the post-current source transistor VB. One of the source and the drain of the post-current source transistor VB is electrically connected to the current source transistor PC.

[0074] The ferroelectric capacitor C is electrically connected to the node VM. Specifically, one electrode of the ferroelectric capacitor C is electrically connected to the switch transistor **S1** and the post-amplifying transistor **V2**, and electrically connectable to the amplifying transistor AMP and the current source transistor PC via the switch transistor **S1**, and corresponds to an example of the first electrode of the present disclosure. The other electrode of the ferroelectric capacitor C is electrically connected to the wiring that supplies a voltage VFE, and corresponds to an example of a second electrode of the present disclosure. The ferroelectric capacitor C includes a ferroelectric film between these electrodes. This ferroelectric film is an example of the first ferroelectric film of the present disclosure. The ferroelectric capacitor C illustrated in FIG. **2** is used to hold a signal of the pixel **1** illustrated in FIG. **2**.

[0075] The solid-state imaging device of the present embodiment has, for example, a structure as illustrated in FIG. **3** or a structure as illustrated in FIG. **4**. Hereinafter, two examples of the structure of the solid-state imaging device of the present embodiment will be described with reference to FIGS. **3** and **4** in order.

[0076] FIG. **3** is a cross-sectional view illustrating a first example of the structure of the solid-state imaging device of the first embodiment. Similarly to FIG. **2**, FIG. **3** illustrates one pixel **1** in the solid-state imaging device of the present embodiment.

[0077] FIG. **3** illustrates an X axis, a Y axis, and a Z axis perpendicular to each other. An X direction and a Y direction correspond to a lateral direction (horizontal direction), and a Z direction corresponds to a longitudinal direction (vertical direction). Furthermore, a +Z direction corresponds to an upward direction, and a −Z direction corresponds to a downward direction. Note that the −Z direction may strictly match the gravity direction, or does not necessarily strictly match the gravity direction.

[0078] The solid-state imaging device illustrated in FIG. **3** includes a substrate **11**, an element isolation insulating film **12**, a gate insulating film **13**, a gate electrode **14**, and a sidewall insulating film **15** included in the switch transistor **S1** and the post-amplifying transistor **V2**, and an interlayer insulating film **16**. The substrate **11** is an example of a first substrate of the present disclosure, and the interlayer insulating film **16** is an example of a first insulating film of the present disclosure.

[0079] The solid-state imaging device illustrated in FIG. **3** further includes a plurality of contact plugs **21**, a wiring **22**, a contact hole **23**, a wiring **24**, a wiring **25**, a wiring **26**, and an electrode **27**, a ferroelectric film **28**, and an electrode **29** included in the ferroelectric capacitor C. The electrode **27**, the ferroelectric film **28**, and the electrode **29** are examples of the first electrode, the first ferroelectric film, and the second electrode of the present disclosure, respectively.

[0080] The substrate **11** is, for example, a semiconductor substrate such as a silicon substrate. In FIG. **3**, the X direction and the Y direction are parallel to the upper surface of the substrate **11**, and the Z direction is perpendicular to the upper surface of the substrate **11**. The substrate **11** includes a well region **11***a* and diffusion regions **11***b*, **11***c*, **11***d*, and **11***e*. The diffusion regions **11***b* and **11***c* function as source and drain regions of the switch transistor **S1**, and the diffusion regions **11***d* and **11***e* function as source and drain

regions of the post-amplifying transistor V2. The substrate **11** further includes the photodiode PD and the floating diffusion unit FD described with reference to FIG. **2** (not illustrated). The photodiode PD is formed by a pn junction in the substrate **11**, and the floating diffusion unit FD is formed by a diffusion region in the substrate **11**.

[0081] The element isolation insulating film **12** is formed in the substrate **11**. The element isolation insulating film **12** is, for example, a silicon oxide film. The element isolation insulating film **12** illustrated in FIG. **3** is interposed between the switch transistor S1 and the post-amplifying transistor V2.

[0082] In each of the switch transistor S1 and the post-amplifying transistor V2, the gate insulating film **13** is formed on the substrate **11**, the gate electrode **14** is formed on the gate insulating film **13**, and the sidewall insulating film **15** is formed on the side surface of the gate electrode **14**. In the example illustrated in FIG. **3**, each of the transfer transistor TG, the reset transistor RST, the amplifying transistor AMP, the selection transistor SEL, the current source transistor PC, and the post-current source transistor VB also includes a gate insulating film **13**, a gate electrode **14**, and a sidewall insulating film **15**.

[0083] The interlayer insulating film **16** is formed on the substrate **11** so as to cover the switch transistor S1 and the post-amplifying transistor V2. In the example illustrated in FIG. **3**, the transfer transistor TG, the reset transistor RST, the amplifying transistor AMP, the selection transistor SEL, the current source transistor PC, the post-current source transistor VB, and the like are also covered with the interlayer insulating film **26**.

[0084] The contact plug **21**, the wiring **22**, the contact hole **23**, and the wiring **24** are formed in the interlayer insulating film **16** on the substrate **11**. FIG. **3** illustrates the contact plug **21** provided on the diffusion region **11***c* of the switch transistor S1 and the contact plug **21** provided on the gate electrode **14** of the post-amplifying transistor V2. The wiring **22** is provided on these contact plugs **21**, and electrically connects the switch transistor S1 and the post-amplifying transistor V2. Note that the above-described node VM is located, for example, in the wiring **22**.

[0085] The contact hole **23** is provided on the wiring **22**. A part of the ferroelectric capacitor C is embedded in the contact hole **23** and is electrically connected to the wiring **22** in the contact hole **23**. The wiring **24** is provided on the ferroelectric capacitor C and is electrically connected to the ferroelectric capacitor C. Note that the wiring **24** is electrically connected to the wiring that supplies the above-described voltage VFE.

[0086] The wirings **25** and **26** are also formed in the interlayer insulating film **16** on the substrate **11**. The wiring **25** is provided at the same height as a part of the contact hole **23**. The wiring **26** is provided at the same height as the wiring **24**.

[0087] The ferroelectric capacitor C includes an electrode **27**, a ferroelectric film **28**, and an electrode **29** which are sequentially formed inside and outside the contact hole **23**. Inside the contact hole **23**, the electrode **27**, the ferroelectric film **28**, and the electrode **29** are sequentially formed on the upper surface of the wiring **22** and the side surface of the interlayer insulating film **16**. Outside the contact hole **23**, the electrode **27**, the ferroelectric film **28**, and the electrode **29** are sequentially formed on the upper surface of the interlayer insulating film **16**. The electrode **27** is in contact with the upper surface of the wiring **22** and is electrically connected to the wiring **22**. The electrode **29** is in contact with the lower surface of the wiring **24** and is electrically connected to the wiring **24**. As described above, the ferroelectric capacitor C in FIG. **3** has a three-dimensional structure spreading in the X direction, the Y direction, and the Z direction.

[0088] The ferroelectric film **28** desirably contains, for example, hafnium (Hf), zirconium (Zr), niobium (Nb), scandium (Sc), yttrium (Y), lanthanum (La), germanium (Ge), or silicon (Si). Examples of the ferroelectric film **28** in FIG. **3** include a hafnium oxide (HfO_2) film, a lead zirconate titanate (PZT) film, a strontium bismuth tantalate (SBT) film, and a lanthanum bismuth titanate (BLT) film. On the other hand, each of the electrodes **27** and **29** is desirably formed of a metal having high reducibility, such as a laminated film including a TiN film and a TiAl film, or a laminated film including a TiN film, a TaN film, and a TiAl film (Ti, N, Al, and Ta represent titanium, nitrogen, aluminum, and tantalum, respectively.).

[0089] Note that the wiring **12** is located in the first (lowermost) wiring layer on the substrate **11**. The ferroelectric capacitor C may be formed on the wiring in any one of the second or more wiring layers instead of being formed on the wiring **12** in the first wiring layer.

[0090] The solid-state imaging device of the present embodiment may have the structure illustrated in FIG. **4** instead of having the structure illustrated in FIG. **3**. FIG. **3** illustrates a structure of a front-illuminated type solid-state imaging device, and FIG. **4** illustrates a structure of a back-illuminated type solid-state imaging device. When the back surface irradiation type structure is adopted, the area of the photodiode (PD) region can be effectively used, and the region where the ferroelectric capacitor C can be formed can be increased.

[0091] FIG. **4** is a cross-sectional view illustrating a second example of the structure of the solid-state imaging device of the first embodiment. Similarly to FIGS. **2** and **3**, FIG. **4** illustrates one pixel **1** and the like in the solid-state imaging device of the present embodiment. The structure illustrated in FIG. **4** will be described focusing on differences from the structure illustrated in FIG. **3**.

[0092] In FIG. **4**, the lower surface of the substrate **11** is the front surface of the substrate **11**, and the upper surface of the substrate **11** is the back surface of the substrate **11**. The solid-state imaging device illustrated in FIG. **4** is a back-illuminated type, and an upper surface (back surface) of the substrate **11** is a light incident surface (light-receiving surface) of the substrate **11**. In FIG. **4**, the lower surface of the substrate **11** is an example of a first surface of the present disclosure, and the upper surface of the substrate **11** is an example of a second surface of the present disclosure.

[0093] The solid-state imaging device illustrated in FIG. **4** includes a region Ra including the above-described pixel array region **2** and the like and a region Rb including a logic circuit and the like as regions existing in the substrate **11**, on the substrate **11**, and under the substrate **11**. In addition, the solid-state imaging device illustrated in FIG. **4** has a two-layer structure including an upper layer Sa and a lower layer Sb.

[0094] The upper layer Sa includes the substrate **11**, the element isolation insulating film **12**, the gate insulating film **13**, the gate electrode **14**, and the sidewall insulating film **15** included in the transfer transistor TG, the switch transistor

S1, a transistor Tr1, and the like, the interlayer insulating film **16**, the plurality of contact plugs **21**, the wiring **22**, a plurality of wirings **22'**, and a wiring **22'**. The upper layer Sa further includes a via plug **31**, a wiring **32**, a wiring **32'**, a wiring **32"**, a via plug **33**, a wiring **34**, and a wiring **34"**, an on-chip filter **41**, and an on-chip lens **42**.

[0095] The lower layer Sb includes a substrate **51**, a gate insulating film **52**, a gate electrode **53**, and a sidewall insulating film **54** included in a transistor Tr2, a transistor Tr3, and the like, and an interlayer insulating film **55**. The lower layer Sb further includes a contact plug **61**, a plurality of contact plugs **61'**, a wiring **62**, a plurality of wirings **62'**, a plurality of contact holes **63**, a plurality of contact holes **63'**, a wiring **64**, a plurality of wirings **64'**, a wiring **65**, a wiring **65'**, a wiring **65"**, a wiring **66**, a wiring **67**, and a wiring **68**. The lower layer Sb further includes an electrode **27**, a ferroelectric film **28**, and an electrode **29** included in a ferroelectric capacitor C and memory capacitors C1 and C2. The substrate **51** is an example of a second substrate of the present disclosure, and the interlayer insulating film **55** is an example of a second insulating film of the present disclosure.

[Upper Layer Sa]

[0096] The substrate **11** illustrated in FIG. **4** includes the photodiode PD and the floating diffusion unit FD in the region Ra. The photodiode PD is formed by a pn junction in the substrate **11**, and the floating diffusion unit FD is formed by a diffusion region **11***f* in the substrate **11**.

[0097] The on-chip filter **41** and the on-chip lens **42** are arranged on the upper surface side of the substrate **11** in the region Ra. Specifically, the on-chip filter **41** is formed on the upper surface of the substrate **11**, and the on-chip lens **42** is formed on the on-chip filter **41**.

[0098] The on-chip filter **41** has a function of transmitting light having a predetermined wavelength, and is formed on the upper surface of the substrate **11** for each pixel **1**. For example, the on-chip filters **41** for red (R), green (G), and blue (B) are arranged above the photodiodes PD of the red, green, and blue pixels **1**, respectively. Furthermore, the on-chip filter **41** for infrared light may be arranged above the photodiode PD of the pixel **1** of infrared light.

[0099] The on-chip lens **42** has a function of condensing incident light, and is formed on the on-chip filter **41** for each pixel **1**. In the present embodiment, light incident on the on-chip lens **42** is condensed by the on-chip lens **42**, transmitted through the on-chip filter **41**, and incident on the photodiode PD. The photodiode PD converts the light into a charge by photoelectric conversion to generate a signal charge.

[0100] On the other hand, the other components in the upper layer Sa are disposed on the lower surface side of the substrate **11**. The transfer transistor TG, the switch transistor S1, and other pixel transistors are provided on the lower surface of the substrate **11** in the region Ra, and the transistor Tr1 is provided on the lower surface of the substrate **11** in the region Rb. These transistors are covered with the interlayer insulating film **16**. The transistor Tr1 constitutes, for example, a logic circuit in the region Rb. Note that the ferroelectric capacitor C and the memory capacitors C1 and C2 are disposed on the lower surface side of the substrate **11**, but are disposed not in the upper layer Sa but in the lower layer Sb. Furthermore, some pixel transistors may be arranged not in the region Ra of the upper layer Sa but in the region Ra of the lower layer Sb.

[0101] In the region Ra, the contact plug **21**, the wiring **22**, the via plug **31**, the wiring **32**, the via plug **33**, and the wiring **34** are sequentially provided on the lower surface of the substrate **11**. Further, in the region Ra, the contact plug **21**, the wiring **22"**, the wiring **32"**, and the wiring **34"** are sequentially provided on the lower surface of the substrate **11**. On the other hand, in the region Rb, a part of the wiring **32** and the wiring **32'** are provided below the substrate **11** via the wiring **22'**.

[Lower Layer Sb]

[0102] The substrate **51** is, for example, a semiconductor substrate such as a silicon substrate. The transistor Tr2 is provided on the substrate **51** in the region Ra, and the transistor Tr3 is provided on the substrate **51** in the region Rb. The transistor Tr2 constitutes a sample hold circuit together with the ferroelectric capacitor C in the region Ra, for example. The transistor Tr3 constitutes a frame memory together with the memory capacitors C1 and C2 in the region Rb, for example. These transistors are covered with an interlayer insulating film **55** formed on the substrate **51**. The interlayer insulating film **55** has a lower surface in contact with the substrate **51** and an upper surface in contact with the interlayer insulating film **16**, and is located between the substrate **51** and the interlayer insulating film **16**. In FIG. **4**, the substrate **51** is bonded to the substrate **11** via the interlayer insulating films **55** and **16**. Note that the shape and arrangement of the gate insulating film **52**, the gate electrode **53**, and the sidewall insulating film **54** are similar to the shape and arrangement of the gate insulating film **13**, the gate electrode **14**, and the sidewall insulating film **15**, respectively.

[0103] The contact plug **61**, the wiring **62**, the contact hole **63**, the wiring **64**, and the wiring **65** are formed in the interlayer insulating film **55** on the substrate **51** in the region Ra. The contact plug **61** is provided on the substrate **51**. The wiring **62** is provided on the contact plug **61**. The contact hole **63** is provided on the wiring **62**. A part of the ferroelectric capacitor C is embedded in the contact hole **63** and is electrically connected to the wiring **62** in the contact hole **63**. The wiring **64** is provided on the ferroelectric capacitor C and is electrically connected to the ferroelectric capacitor C. The wiring **65** is provided on the wiring **64** and is in contact with the wiring **34**. The wiring **65"** is provided at the same height as the wiring **65** and is in contact with the wiring **34"**. The wirings **66**, **67**, and **68** are provided at the same height as a part of the contact hole **63**.

[0104] The ferroelectric capacitor C illustrated in FIG. **4** includes the electrode **27**, the ferroelectric film **28**, and the electrode **29** which are sequentially formed inside and outside the contact hole **63**. Inside the contact hole **63**, the electrode **27**, the ferroelectric film **28**, and the electrode **29** are sequentially formed on the upper surface of the wiring **62** and the side surface of the interlayer insulating film **55**. Outside the contact hole **63**, the electrode **27**, the ferroelectric film **28**, and the electrode **29** are sequentially formed on the upper surface of the interlayer insulating film **55**. The electrode **27** is in contact with the upper surface of the wiring **62** and is electrically connected to the wiring **62**. Similarly, the electrode **29** is in contact with the lower surface of the wiring **64** and is electrically connected to the wiring **64**. As described above, the ferroelectric capacitor C

illustrated in FIG. **4** has a three-dimensional structure spreading in the X direction, the Y direction, and the Z direction.

[0105] The ferroelectric capacitor C illustrated in FIG. **4** includes a plurality of partial capacitors formed in the plurality of contact holes **63**, and these partial capacitors are connected in parallel. Note that the contact area between these partial capacitors and the wiring **62** is desirably as wide as possible.

[0106] The contact plug **61'**, the wiring **62'**, the contact hole **63'**, the wiring **64'**, and the wiring **65'** are formed in the interlayer insulating film **55** on the substrate **51** in the region Rb. The contact plug **61'** is provided on the substrate **51**. The wiring **62'** is provided on the contact plug **61'**. The contact hole **63'** is provided on the wiring **62'**. A part of the memory capacitors C**1** and C**2** is embedded in the contact hole **63'** and is electrically connected to the wiring **62'** in the contact hole **63'**. The wiring **64'** is provided on the memory capacitors C**1** and C**2**, and is electrically connected to the memory capacitors C**1** and C**2**. The wiring **65'** is provided on the wiring **64'**.

[0107] Each of the memory capacitors C**1** and C**2** includes the electrode **27**, the ferroelectric film **28**, and the electrode **29** which are sequentially formed inside and outside the contact hole **63'**. Inside the contact hole **63'**, the electrode **27**, the ferroelectric film **28**, and the electrode **29** are sequentially formed on the upper surface of the wiring **62'** and the side surface of the interlayer insulating film **55**. Outside the contact hole **63'**, the electrode **27**, the ferroelectric film **28**, and the electrode **29** are sequentially formed on the upper surface of the interlayer insulating film **55**. The electrode **27** is in contact with the upper surface of the wiring **62'** and is electrically connected to the wiring **62'**. Similarly, the electrode **29** is in contact with the lower surface of the wiring **64'** and is electrically connected to the wiring **64'**. As described above, the memory capacitors C**1** and C**2** have a three-dimensional structure spreading in the X direction, the Y direction, and the Z direction. The electrode **27**, the ferroelectric film **28**, and the electrode **29** of the memory capacitors C**1** and C**2** are examples of a third electrode, a second ferroelectric film, and a fourth electrode of the present disclosure, respectively.

[0108] In FIG. **4**, a plurality of memory capacitors C**1** and C**2** are formed in the plurality of contact holes **63'**. These memory capacitors C**1** and C**2** are disposed on different wirings **62'** and under different wirings **64'**, but are electrically connected to the same wiring **65'**.

[0109] Next, further details of the ferroelectric capacitor C and the memory capacitors C**1** and C**2** of the present embodiment will be described.

[0110] In the solid-state imaging device of the present embodiment, the electrodes **27** of the memory capacitors C**1** and C**2** are formed of the same material as the electrode **27** of the ferroelectric capacitor C, the ferroelectric films **28** of the memory capacitors C**1** and C**2** are formed of the same material as the ferroelectric film **28** of the ferroelectric capacitor C, and the electrodes **29** of the memory capacitors C**1** and C**2** are formed of the same material as the electrode **29** of the ferroelectric capacitor C.

[0111] Therefore, the electrodes **27**, the ferroelectric films **28**, and the electrodes **29** of the memory capacitors C**1** and C**2** have the same composition as the electrodes **27**, the ferroelectric films **28**, and the electrodes **29** of the ferroelectric capacitors C, respectively. For example, in a case where the ferroelectric film **28** of the ferroelectric capacitor C is a PZT film, the ferroelectric films **28** of the memory capacitors C**1** and C**2** are also PZT films. However, in a case where the composition of at least one of these ferroelectric films **28** is changed after formation of these ferroelectric films **28**, these ferroelectric films **28** may not have the same composition.

[0112] Further, the electrodes **27**, the ferroelectric films **28**, and the electrodes **29** of the memory capacitors C**1** and C**2** have the same film thicknesses as the electrodes **27**, the ferroelectric films **28**, and the electrodes **29** of the ferroelectric capacitors C, respectively. For example, in a case where the film thickness of the ferroelectric film **28** of the ferroelectric capacitor C is X nm, the ferroelectric films **28** of the memory capacitors C**1** and C**2** are also X nm (X is an arbitrary real number). However, in a case where the film thickness of at least one of these ferroelectric films **28** is changed after formation of these ferroelectric films **28**, these ferroelectric films **28** may not have the same film thickness.

[0113] In the solid-state imaging device of the present embodiment, since the memory capacitors C**1** and C**2** and the ferroelectric capacitor C are formed of the same material, not only the ferroelectric capacitor C but also the memory capacitors C**1** and C**2** are ferroelectric capacitors. Note that at least one of the electrode **27** and the electrode **29** may be made of a material different between the memory capacitors C**1** and C**2** and the ferroelectric capacitor C.

[0114] The ferroelectric capacitor C and the memory capacitors C**1** and C**2** of the present embodiment are formed, for example, as follows. First, the contact holes **63** and **63'** are simultaneously formed in the interlayer insulating film **55**. Next, a lower electrode material, a ferroelectric material, and an upper electrode material are sequentially formed inside and outside the contact holes **63** and **63'**. Next, the lower electrode material, the ferroelectric material, and the upper electrode material are processed by etching. As a result, the electrodes **27**, the ferroelectric films **28**, and the electrodes **29** of the ferroelectric capacitor C and the memory capacitors C**1** and C**2** are formed from the lower electrode material, the ferroelectric material, and the upper electrode material, respectively.

[0115] In FIG. **4**, the height (Z coordinate) of the lower end of the contact hole **63'** is substantially the same as the height of the lower end of the contact hole **63**, and the height of the upper end of the contact hole **63'** is also substantially the same as the height of the upper end of the contact hole **63**. Therefore, the ferroelectric capacitor C and the memory capacitors C**1** and C**2** can be cut at the same XY cross section (cross section). That is, in the solid-state imaging device illustrated in FIG. **4**, an XY plane passing through both the ferroelectric capacitor C and the memory capacitors C**1** and C**2** can be set. This can be expressed that the ferroelectric capacitor C and the memory capacitors C**1** and C**2** are located at the same height. Note that the heights of the lower ends of the contact holes **63** and **63'** may not coincide with each other, and the heights of the upper ends of the contact holes **63** and **63'** may not coincide with each other. However, it is desirable to form the contact holes **63** and **63'** simultaneously in order to simplify the semiconductor manufacturing process, and in this case, the heights of the lower ends coincide with each other and the heights of the upper ends coincide with each other in many cases.

[0116] As described above, the solid-state imaging device of the present embodiment includes the ferroelectric capacitor C as a capacitor. As a result, it is possible to reduce the

cost related to the capacitor, for example, it is possible to form a large-capacity capacitor or a high-performance capacitor at low cost.

[0117] Furthermore, the solid-state imaging device of the present embodiment includes the ferroelectric capacitor C as a capacitor, and includes the memory capacitors C**1** and C**2** as ferroelectric capacitors. As a result, the ferroelectric capacitor C and the memory capacitors C**1** and C**2** can be formed at the same time, the ferroelectric capacitor C and the memory capacitors C**1** and C**2** can be formed of the same material, and the total cost of the ferroelectric capacitor C and the memory capacitors C**1** and C**2** can be reduced. Furthermore, in the present embodiment, since the frame memory is an FeRAM, the capacity and performance of the frame memory can be improved.

[0118] FIG. **5** is a perspective view illustrating a structure of the solid-state imaging device illustrated in FIG. **4**.

[0119] FIG. **5** schematically illustrates a relationship between the upper layer Sa and the lower layer Sb. In FIG. **5**, the upper layer Sa includes the pixel array region **2** provided in the region Ra and the circuit region **71** provided in the region Rb, and the lower layer Sb includes the sample hold region **72** provided in the region Ra and the memory region **73** provided in the region Rb.

[0120] The pixel array region **2** includes the plurality of pixels **1** (see FIG. **1**). The circuit region **71** includes a logic circuit including the transistor Tr**1** and the like. The sample hold region **72** includes a sample hold circuit including the transistor Tr**2**, the ferroelectric capacitor C, and the like. The memory region **73** includes a frame memory including the transistor Tr**3**, the memory capacitors C**1** and C**2**, and the like.

[0121] In FIG. **5**, since the upper layer Sa of the solid-state imaging device and the lower layer Sb of the solid-state imaging device are manufactured by different processes, the ferroelectric capacitors C and the memory capacitors C**1** and C**2** can be formed without being limited to the process generation of the upper layer Sa. For example, by manufacturing the ferroelectric capacitor C and the memory capacitors C**1** and C**2** by a finer technology, the capacity of the ferroelectric capacitor C and the memory capacitors C**1** and C**2** can be increased.

[0122] FIG. **6** is a graph for explaining the operation of the solid-state imaging device of the first embodiment.

[0123] FIG. **6** shows a Q-V curve for explaining the operation of the ferroelectric capacitor C of the present embodiment. The horizontal axis in FIG. **6** represents the potential (voltage VFE) applied to the ferroelectric capacitor C. The vertical axis in FIG. **6** represents the polarization amount generated in the ferroelectric capacitor C. When the direction of the write voltage applied to the ferroelectric capacitor C changes, residual polarization occurs in the ferroelectric capacitor C. Therefore, the Q-V curve of the ferroelectric capacitor C draws hysteresis as illustrated in FIG. **6**. In addition, the capacity Cfe of the ferroelectric capacitor C represented by the slope of the Q-V curve can take two types of values of Cfe low and Cfe high as illustrated in FIG. **6**. The Q-V curve shown in FIG. **6** has a shape close to a parallelogram. Cfe low corresponds to the inclination of the lower side of the parallelogram, and Cfe high corresponds to the inclination of the left side of the parallelogram.

[0124] In the solid-state imaging device of the present embodiment, before reading from the floating diffusion unit FD, the state of the ferroelectric capacitor C is set in advance to the "Cfe low state" instead of the "Cfe high state". That is, before reading from the floating diffusion unit FD, the capacity Cfe of the ferroelectric capacitor C is not Cfe high but Cfe low. The state of the ferroelectric capacitor C is controlled by, for example, the control circuit **3**.

[0125] The solid-state imaging device of the present embodiment is the VD-GS as described above. In this case, if the state of the ferroelectric capacitor C is set to the "Cfe high state" in advance before reading from the floating diffusion unit FD, the Cfe high state is destroyed at the time of reading. Therefore, in the present embodiment, only the Cfe low state is used. This corresponds to using the ferroelectric capacitor C like a paraelectric capacitor. The Cfe low state can be realized, for example, by setting the voltage VFE to 0 V and setting the voltage of the node VM to VDD.

[0126] As described above, the solid-state imaging device of the present embodiment includes the ferroelectric capacitor C as a capacitor, and includes the memory capacitors C**1** and C**2** as ferroelectric capacitors. Therefore, according to the present embodiment, the cost of the former capacitor (ferroelectric capacitor C) can be reduced, and the total cost of the ferroelectric capacitor C and the memory capacitors C**1** and C**2** can be reduced.

Second Embodiment

[0127] FIG. **7** is a cross-sectional view illustrating a structure of a solid-state imaging device of a second embodiment. Similarly to FIG. **4**, FIG. **7** illustrates one pixel **1** and the like in the solid-state imaging device of the present embodiment. The structure illustrated in FIG. **7** will be described focusing on differences from the structure illustrated in FIG. **4**.

[0128] The solid-state imaging device of the present embodiment has a structure in which the ferroelectric capacitor C is replaced with an antiferroelectric capacitor C', and the memory capacitors C**1** and C**2** are replaced with memory capacitors C**1'** and C**2'**. The antiferroelectric capacitor C' includes an antiferroelectric film **81** instead of the ferroelectric film **28**. The antiferroelectric film **81** is an example of a first antiferroelectric film of the present disclosure. Similarly, the memory capacitors C**1'** and C**2'** include the antiferroelectric film **81** instead of the ferroelectric film **28**. The antiferroelectric film **81** is an example of a second antiferroelectric film of the present disclosure. In the present embodiment, not only the antiferroelectric capacitor C' but also the memory capacitors C**1'** and C**2'** are antiferroelectric capacitors.

[0129] In the solid-state imaging device of the present embodiment, the electrodes **27** of the memory capacitors C**1'** and C**2'** are formed of the same material as the electrode **27** of the antiferroelectric capacitor C', the antiferroelectric films **81** of the memory capacitors C**1'** and C**2'** are formed of the same material as the antiferroelectric film **81** of the antiferroelectric capacitor C', and the electrodes **29** of the memory capacitors C**1'** and C**2'** are formed of the same material as the electrode **29** of the antiferroelectric capacitor C'. These antiferroelectric films **81** desirably contain, for example, hafnium (Hf), zirconium (Zr), niobium (Nb), scandium (Sc), yttrium (Y), lanthanum (La), germanium (Ge), or silicon (Si).

[0130] FIG. **8** is a graph for explaining the operation of the solid-state imaging device of the second embodiment.

[0131] FIG. **8** shows a Q-V curve for explaining the operation of the antiferroelectric capacitor C' of the present

embodiment. The Q-V curve of the antiferroelectric capacitor C' draws hysteresis as illustrated in FIG. **8**. FIG. **8** further shows Cfe low and Cfe high as values of the capacity Cfe of the antiferroelectric capacitor C'. In the solid-state imaging device of the present embodiment, before reading from the floating diffusion unit FD, the state of the antiferroelectric capacitor C' is set in advance not to the "Caf high state" but to the "Caf low state". The state of the antiferroelectric capacitor C' is controlled by, for example, the control circuit **3**.

[0132] As described above, the solid-state imaging device of the present embodiment includes the antiferroelectric capacitor C' as a capacitor, and includes the memory capacitors C**1**' and C**2**' as antiferroelectric capacitors. Therefore, according to the present embodiment, the cost of the former capacitor (antiferroelectric capacitor C') can be reduced, and the total cost of the antiferroelectric capacitor C' and the memory capacitors C**1**' and C**2**' can be reduced. The frame memory of the present embodiment is an FeRAM because the memory capacitors C**1**' and C**2**' are antiferroelectric capacitors.

Third Embodiment

[0133] FIG. **9** is a cross-sectional view illustrating a structure of a solid-state imaging device of a third embodiment. Similarly to FIG. **4**, FIG. **9** illustrates one pixel **1** and the like in the solid-state imaging device of the present embodiment. The structure illustrated in FIG. **9** will be described focusing on differences from the structure illustrated in FIG. **4**.

[0134] The solid-state imaging device of the present embodiment has a structure in which the ferroelectric capacitor C is replaced with a paraelectric capacitor C", and the memory capacitors C**1** and C**2** are replaced with memory capacitors C**1**" and C**2**". The paraelectric capacitor C" includes a paraelectric film **82** instead of the ferroelectric film **28**. The paraelectric film **82** is an example of a first paraelectric film of the present disclosure. Similarly, the memory capacitors C**1**" and C**2**" include the paraelectric film **82** instead of the ferroelectric film **28**. The paraelectric film **82** is an example of a second paraelectric film of the present disclosure. In the present embodiment, not only the paraelectric capacitor C" but also the memory capacitors C**1**" and C**2**" are antiferroelectric capacitors.

[0135] In the solid-state imaging device of the present embodiment, the electrodes **27** of the memory capacitors C**1**" and C**2**" are formed of the same material as the electrode **27** of the paraelectric capacitor C", the paraelectric films **82** of the memory capacitors C**1**" and C**2**" are formed of the same material as the paraelectric film **82** of the paraelectric capacitor C", and the electrodes **29** of the memory capacitors C**1**" and C**2**" are formed of the same material as the electrode **29** of the paraelectric capacitor C". These paraelectric films **82** desirably contain, for example, hafnium (Hf), zirconium (Zr), niobium (Nb), scandium (Sc), yttrium (Y), lanthanum (La), germanium (Ge), or silicon (Si).

[0136] FIG. **10** is a graph for explaining the operation of the solid-state imaging device of the third embodiment.

[0137] FIG. **10** shows a Q-V curve for explaining the operation of the paraelectric capacitor C" of the present embodiment. As shown in FIG. **10**, the Q-V curve of the paraelectric capacitor C" does not draw hysteresis. Therefore, the paraelectric capacitor C" of the present embodiment does not have a plurality of values as the value of the capacity C, unlike the ferroelectric capacitor C of the first embodiment and the antiferroelectric capacitor C' of the second embodiment. Before reading in the present embodiment, it is desirable to set the state of the paraelectric capacitor C" to the "Clow state" in advance. This state may be the "C high state" or the "C low state".

[0138] As described above, the solid-state imaging device of the present embodiment includes the paraelectric capacitor C" as a capacitor, and includes the memory capacitors C**1**" and C**2**" as paraelectric capacitors. Therefore, according to the present embodiment, the total cost of the paraelectric capacitor C" and the memory capacitors C**1**" and C**2**" can be reduced. The frame memory of the present embodiment is a DRAM since the memory capacitors C**1**" and C**2**" are paraelectric capacitors.

Fourth Embodiment

[0139] FIG. **11** is a perspective view illustrating a structure of a solid-state imaging device of a fourth embodiment.

[0140] The solid-state imaging device of the present embodiment has a structure illustrated in FIG. **11** instead of the structure illustrated in FIG. **5**. The solid-state imaging device of the present embodiment has a three-layer structure including an upper layer Sa, a lower layer Sb, and an intermediate layer Sc. In the present embodiment, the upper layer Sa includes the pixel array region **2** provided in the regions Ra and Rb, the lower layer Sb includes the circuit region **71** provided in the regions Ra and Rb, and the intermediate layer Sc includes the sample hold region **72** provided in the region Ra and the memory region **73** provided in the region Rb.

[0141] The intermediate layer Sc includes, for example, a substrate similar to the substrates **11** and **51** (hereinafter referred to as "intermediate substrate"). In this case, the intermediate layer Sc includes, for example, the ferroelectric capacitor C, the memory capacitors C**1** and C**2**, and the transistors Tr**2** and Tr**3** provided on the lower surface of the intermediate substrate, and an interlayer insulating film provided on the lower surface of the intermediate substrate so as to cover these transistors. The intermediate substrate is, for example, a semiconductor substrate such as a silicon substrate. The intermediate substrate is an example of a third substrate of the present disclosure.

[0142] In the present embodiment, since the upper layer Sa, the lower layer Sb, and the intermediate layer Sc of the solid-state imaging device are manufactured by different processes, it is possible to form the ferroelectric capacitor C and the memory capacitors C**1** and C**2** without being limited to the process generation of the upper layer Sa. For example, by manufacturing the ferroelectric capacitor C and the memory capacitors C**1** and C**2** by a finer technology, the capacity of the ferroelectric capacitor C and the memory capacitors C**1** and C**2** can be increased.

[0143] Note that the solid-state imaging device of the present embodiment may include the antiferroelectric capacitor C' or the paraelectric capacitor C" instead of the ferroelectric capacitor C, and may include the memory capacitors C**1**' and C**2**' or the memory capacitors C**1**" and C**2**" instead of the memory capacitors C**1** and C**2**.

Fifth Embodiment

[0144] FIG. **12** is a perspective view illustrating a structure of a solid-state imaging device of a fifth embodiment.

[0145] The solid-state imaging device of the present embodiment has a structure illustrated in FIG. **12** instead of the structure illustrated in FIG. **5**. The solid-state imaging device of the present embodiment includes a region Rc in addition to the regions Ra and Rb. The solid-state imaging device of the present embodiment further has a two-layer structure including the upper layer Sa and the lower layer Sb. In the present embodiment, the upper layer Sa includes the pixel array region **2** provided in the regions Ra, Rb, and Rc, and the lower layer Sb includes the circuit region **71** provided in the region Rc, the sample hold region **72** provided in the region Ra, and the memory region **73** provided in the region Rb.

[0146] In the present embodiment, since the upper layer Sa and the lower layer Sb of the solid-state imaging device are manufactured by different processes, the ferroelectric capacitor C and the memory capacitors C**1** and C**2** can be formed without being limited to the process generation of the upper layer Sa. For example, by manufacturing the ferroelectric capacitor C and the memory capacitors C**1** and C**2** by a finer technology, the capacity of the ferroelectric capacitor C and the memory capacitors C**1** and C**2** can be increased.

[0147] Note that the solid-state imaging device of the present embodiment may include the antiferroelectric capacitor C' or the paraelectric capacitor C" instead of the ferroelectric capacitor C, and may include the memory capacitors C**1**' and C**2**' or the memory capacitors C**1**" and C**2**" instead of the memory capacitors C**1** and C**2**.

Sixth Embodiment

[0148] FIG. **13** is a transverse cross-sectional view illustrating two examples of the structure of the solid-state imaging device of the sixth embodiment.

[0149] A of FIG. **13** illustrates a first example of an XY cross section (cross section) of the ferroelectric capacitor C illustrated in FIG. **4**. In A of FIG. **13**, each contact hole **63** has a circular XY cross section, and thus has a columnar shape extending in the Z direction.

[0150] B of FIG. **13** illustrates a second example of the XY cross section (cross section) of the ferroelectric capacitor C illustrated in FIG. **4**. In B of FIG. **13**, each contact hole **63** has a linear XY cross section extending in the Y direction, and thus has a planar shape extending in the Y direction and the Z direction.

[0151] As described above, the ferroelectric capacitor C of the present embodiment may have any shape. For example, the XY cross section of each contact hole **63** may be an elliptical shape or a quadrangular shape instead of a circular shape, or may be a curved shape instead of a linear shape. Note that the structure of the present embodiment is also applicable to the antiferroelectric capacitor C' and the paraelectric capacitor C".

Seventh Embodiment

[0152] FIG. **14** is a perspective view illustrating a structure of a solid-state imaging device of a seventh embodiment.

[0153] The solid-state imaging device of the present embodiment has a two-layer structure including the upper layer Sa and the lower layer Sb. The upper layer Sa includes the pixel array region **2** including the plurality of pixels **1** and a plurality of connecting portions **91**. These connecting portions **91** include a pad portion **91***a*, a pad portion **91***b*, a via portion **91***c*, and a via portion **91***d*. The lower layer Sb includes a signal processing unit **92**, a memory unit **93**, a data processing unit **94**, and a control unit **95**. The configuration of the solid-state imaging device illustrated in FIG. **1** can be realized by, for example, the structure illustrated in FIG. **14**.

[0154] The pad portion **91***a*, the pad portion **91***b*, the via portion **91***c*, and the via portion **91***d* are arranged around the pixel array region **2**. The pad portions **91***a* and **91***b* are provided to electrically connect the solid-state imaging device of the present embodiment to another device. The via portions **91***c* and **91***d* are provided to electrically connect the upper layer Sa of the present embodiment to the lower layer Sb.

[0155] The signal processing unit **92** performs various processes on the signal from the pixel array region **2**. The memory unit **93** stores the image data processed by the signal processing unit **92**. The data processing unit **94** performs various processes on the image data stored in the memory unit **93**, and outputs the processed image data to another device. The control unit **95** controls various operations of the solid-state imaging device of the present embodiment, and functions as, for example, the control circuit **3** illustrated in FIG. **1**.

[0156] FIG. **15** is a block diagram illustrating a configuration of a solid-state imaging device of a seventh embodiment.

[0157] FIG. **15** illustrates the pixel array region **2** and the row selection unit **96** in the upper layer Sa, and the signal processing unit **92**, the memory unit **93**, the data processing unit **94**, and the control unit **95** in the lower layer Sb. The pixel **1** in the pixel array region **2** in FIG. **15** has the configuration illustrated in FIG. **2**. Furthermore, the signal processing unit **92** includes an analog to digital (A/D) converter **92***a*, a reference voltage generation unit **92***b*, a data latch unit **92***c*, a current source **92***d*, a decoder **92***e*, a row decoder **92***f*, and an interface (I/F) unit **92***g*.

[0158] The A/D converter **92***a* includes two comparators CMP and two counters CN, and converts a signal from the pixel array region **2** from an analog signal to a digital signal. The reference voltage generation unit **92***b* generates a reference signal VREF for the A/D converter **92***a*. The data latch unit **92***c* latches the digital signal from the A/D converter **92***a*. The current source **92***d* supplies a constant current to the A/D converter **92***a*. Under the control of the control unit **95**, the decoder **92***e* and the row decoder **92***f* specify a row address and provide an address signal for specifying a selected row to the row selection unit **96**. The I/F unit **92***g* functions as an interface for outputting processed image data to another device.

[0159] Note that the configuration of the solid-state imaging device illustrated in FIG. **1** may be implemented by the structure illustrated in FIG. **14** or may be implemented by another structure.

Eighth to Eleventh Embodiments

[0160] The circuit configuration illustrated in FIG. **2** may be replaced with the circuit configurations illustrated in FIGS. **16** to **19**. Hereinafter, the circuit configuration illustrated in FIGS. **16** to **19** will be described.

[0161] FIG. **16** is a circuit diagram showing a configuration of a solid-state imaging device of an eighth embodiment.

[0162] The pixel **1** illustrated in FIG. **16** includes a switch transistor S**2**, a ferroelectric capacitor C provided at a post stage of the switch transistor S**2**, a post-amplifying transistor V**2**, and a selection transistor SEL, in addition to the components illustrated in FIG. **2**. In FIG. **16**, the configurations of the switch transistor S**2**, the ferroelectric capacitor C provided at the post stage of the switch transistor S**2**, the post-amplifying transistor V**2**, and the selection transistor SEL are the same as the configurations of the switch transistor S**1**, the ferroelectric capacitor C provided at the post stage of the switch transistor S**1**, the post-amplifying transistor V**2**, and the selection transistor SEL, respectively. The pixel **1** illustrated in FIG. **16** further includes two current sources I provided at the post stage of the switch transistors S**1** and S**2**.

[0163] FIG. **17** is a circuit diagram illustrating a configuration of a solid-state imaging device of a ninth embodiment.

[0164] The pixel **1** illustrated in FIG. **17** includes, in addition to the components illustrated in FIG. **2**, the ferroelectric capacitor C provided between the switch transistor S**1** and the post-amplifying transistor V**2**, and the switch transistor S**2** electrically connected to the ferroelectric capacitor C and the post-amplifying transistor V**2**. The pixel **1** illustrated in FIG. **17** further includes a current source I provided at a post stage of the selection transistor SEL.

[0165] FIG. **18** is a circuit diagram illustrating a configuration of a solid-state imaging device of a tenth embodiment.

[0166] The pixel **1** illustrated in FIG. **18** includes, in addition to the components illustrated in FIG. **2**, the switch transistor S**2** connected in parallel with the switch transistor S**1**, and a transistor RSTB electrically connected to the switch transistors S**1** and S**2** and the post-amplifying transistor V**2**. The pixel **1** illustrated in FIG. **18** further includes the current source I provided at the post stage of the selection transistor SEL.

[0167] The pixel **1** illustrated in FIG. **18** further includes two ferroelectric capacitors C. However, one of these ferroelectric capacitors C is disposed between the amplifying transistor AMP and the switch transistor S**1**, and the other of these ferroelectric capacitors C is disposed between the amplifying transistor AMP and the switch transistor S**2**. One electrode of the ferroelectric capacitors C is electrically connected to the source or the drain of the amplifying transistor AMP.

[0168] FIG. **19** is a circuit diagram illustrating a configuration of a solid-state imaging device of an eleventh embodiment.

[0169] The pixel **1** shown in FIG. **19** includes the switch transistor S**2**, the ferroelectric capacitor C provided at a post stage of the switch transistor S**2**, and a switch transistor SH, in addition to the components shown in FIG. **2**.

[0170] The switch transistor SH is provided between the amplifying transistor AMP and the post-amplifying transistor V**2**. The switch transistor S**1** is electrically connected to the switch transistor SH and the post-amplifying transistor V**2**, and the switch transistor S**2** is also electrically connected to the switch transistor SH and the post-amplifying transistor V**2**. The ferroelectric capacitor C at the post stage of the switch transistor S**1** is electrically connectable to the amplifying transistor AMP via the switch transistors SH and S**1**. Similarly, the ferroelectric capacitor C at the post stage of the switch transistor S**2** is electrically connectable to the amplifying transistor AMP via the switch transistors SH and S**2**.

[0171] Note that the configurations of the eighth to eleventh embodiments can be applied not only to the ferroelectric capacitor C but also to the antiferroelectric capacitor C' and the paraelectric capacitor C".

Application Example

[0172] FIG. **20** is a block diagram illustrating a configuration example of an electronic device. The electric device illustrated in FIG. **20** is a camera **100**.

[0173] The camera **100** includes an optical unit **101** including a lens group and the like, an imaging device **102** that is the solid-state imaging device of any of the first to eleventh embodiments, a digital signal processor (DSP) circuit **103** that is a camera signal processing circuit, a frame memory **104**, a display unit **105**, a recording unit **106**, an operation unit **107**, and a power supply unit **108**. Furthermore, the DSP circuit **103**, the frame memory **104**, the display unit **105**, the recording unit **106**, the operation unit **107**, and the power supply unit **108** are connected to each other via a bus line **109**.

[0174] The optical unit **101** captures incident light (image light) from a subject and forms an image on an imaging surface of the imaging device **102**. The imaging device **102** converts an amount of incident light formed into an image on the imaging surface by the optical unit **101** into an electric signal on a pixel-by-pixel basis and outputs the electric signal as a pixel signal.

[0175] The DSP circuit **103** performs signal processing on the pixel signal output from the imaging device **102**. The frame memory **104** is a memory for storing one screen of a moving image or a still image captured by the imaging device **102**.

[0176] The display unit **105** includes, for example, a panel type display device such as a liquid crystal panel or an organic EL panel, and displays a moving image or a still image captured by the imaging device **102**. The recording unit **106** records a moving image or a still image captured by the imaging device **102** on a recording medium such as a hard disk or a semiconductor memory.

[0177] The operation unit **107** issues operation commands for various functions of the camera **100** in response to an operation performed by a user. The power supply unit **108** appropriately supplies various power supplies, which are operation power supplies for the DSP circuit **103**, the frame memory **104**, the display unit **105**, the recording unit **106**, and the operation unit **107**, to these power supply targets.

[0178] It can be expected to acquire a satisfactory image by using the solid-state imaging device of any of the first to eleventh embodiments as the imaging device **102**.

[0179] The solid-state imaging device can be applied to various other products. For example, the solid-state imaging device may be mounted on any type of moving bodies such as vehicles, electric vehicles, hybrid electric vehicles, motorcycles, bicycles, personal mobility, airplanes, drones, ships, and robots.

[0180] FIG. **21** is a block diagram illustrating a configuration example of a moving body control system. The moving body control system illustrated in FIG. **21** is a vehicle control system **200**.

[0181] The vehicle control system **200** includes a plurality of electronic control units connected to each other via a communication network **201**. In the example illustrated in FIG. **21**, the vehicle control system **200** includes a driving system control unit **210**, a body system control unit **220**, an

outside-vehicle information detecting unit **230**, an in-vehicle information detecting unit **240**, and an integrated control unit **250**. Moreover, FIG. **21** illustrates a microcomputer **251**, a sound/image output unit **252**, and a vehicle-mounted network interface (I/F) **253** as components of the integrated control unit **250**.

[0182] The driving system control unit **210** controls the operation of devices related to a driving system of a vehicle in accordance with various types of programs. For example, the driving system control unit **210** functions as a control device for a driving force generating device for generating a driving force of a vehicle, such as an internal combustion engine, a driving motor, or the like, a driving force transmitting mechanism for transmitting the driving force to wheels, a steering mechanism for adjusting a steering angle of the vehicle, a braking device for generating a braking force of the vehicle, and the like.

[0183] The body system control unit **220** controls the operation of various types of devices provided to a vehicle body in accordance with various types of programs. For example, the body system control unit **220** functions as a control device for a smart key system, a keyless entry system, a power window device, or various types of lamps (for example, a head lamp, a backup lamp, a brake lamp, a turn signal, a fog lamp, or the like). In this case, radio waves transmitted from a mobile device as an alternative to a key or signals of various types of switches can be input to the body system control unit **220**. The body system control unit **220** receives inputs of such radio waves or signals, and controls a door lock device, the power window device, the lamps, or the like of the vehicle.

[0184] The outside-vehicle information detecting unit **230** detects information on the outside of the vehicle including the vehicle control system **200**. The outside-vehicle information detecting unit **230** is connected with, for example, an imaging unit **231**. The outside-vehicle information detecting unit **230** makes the imaging unit **231** capture an image of the outside of the vehicle, and receives the captured image from the imaging unit **231**. On the basis of the received image, the outside-vehicle information detecting unit **230** may perform processing of detecting an object such as a human, an automobile, an obstacle, a sign, a character on a road surface, or the like, or processing of detecting a distance thereto.

[0185] The imaging unit **231** is an optical sensor that receives light and that outputs an electric signal corresponding to the amount of received light. The imaging unit **231** can output the electric signal as an image, or can output the electric signal as information on a measured distance. The light received by the imaging unit **231** may be visible light, or may be invisible light such as infrared light. The imaging unit **231** includes the solid-state imaging device of any of the first to eleventh embodiments.

[0186] The in-vehicle information detecting unit **240** detects information on the inside of the vehicle equipped with the vehicle control system **200**. The in-vehicle information detecting unit **240** is, for example, connected with a driver state detecting unit **241** that detects a state of a driver. For example, the driver state detecting unit **241** includes a camera that captures an image of the driver, and on the basis of detection information input from the driver state detecting unit **241**, the in-vehicle information detecting unit **240** may calculate a degree of fatigue of the driver or a degree of concentration of the driver, or may determine whether or not the driver is dozing off. The camera may include the solid-state imaging device of any of the first to eleventh embodiments, and may be, for example, the camera **100** illustrated in FIG. **20**.

[0187] The microcomputer **251** can calculate a control target value for the driving force generating device, the steering mechanism, or the braking device on the basis of the information on the inside or outside of the vehicle obtained by the outside-vehicle information detecting unit **230** or the in-vehicle information detecting unit **240**, and output a control command to the driving system control unit **210**. For example, the microcomputer **251** can perform cooperative control intended to implement functions of an advanced driver assistance system (ADAS), the functions including collision avoidance or shock mitigation for the vehicle, following traveling based on a following distance, vehicle speed maintaining traveling, a warning of collision of the vehicle, a warning of deviation of the vehicle from a lane, and the like.

[0188] Furthermore, the microcomputer **251** can perform cooperative control intended for automated driving, which makes the vehicle travel autonomously without depending on the operation of the driver, or the like, by controlling the driving force generating device, the steering mechanism, the braking device, or the like on the basis of the information around the vehicle obtained by the outside-vehicle information detecting unit **230** or the in-vehicle information detecting unit **240**.

[0189] Furthermore, the microcomputer **251** can output a control command to the body system control unit **220** on the basis of the information on the outside of the vehicle obtained by the outside-vehicle information detecting unit **230**. For example, the microcomputer **251** can perform cooperative control for the purpose of preventing glare, such as switching from a high beam to a low beam, by controlling the headlamp according to the position of a preceding vehicle or an oncoming vehicle detected by the outside-vehicle information detecting unit **230**.

[0190] The sound/image output unit **252** transmits an output signal of at least one of a sound or an image to an output device that can visually or auditorily provide information to an occupant of the vehicle or the outside of the vehicle. In the example of FIG. **21**, an audio speaker **261**, a display unit **262**, and an instrument panel **263** are illustrated as such an output device. The display unit **262** may, for example, include an on-board display or a head-up display.

[0191] FIG. **22** is a plan view illustrating a specific example of a setting position of the imaging unit **231** in FIG. **21**.

[0192] A vehicle **300** illustrated in FIG. **22** includes imaging units **301**, **302**, **303**, **304**, and **305** as the imaging unit **231**. The imaging units **301**, **302**, **303**, **304**, and **305** are, for example, provided at positions on a front nose, side mirrors, a rear bumper, and a back door of the vehicle **300**, and on an upper portion of a windshield in the interior of the vehicle.

[0193] The imaging unit **301** provided on the front nose mainly acquires an image of the front of the vehicle **300**. The imaging unit **302** provided on the left side mirror and the imaging unit **303** provided on the right side mirror mainly acquire images of the sides of the vehicle **300**. The imaging unit **304** provided to the rear bumper or the back door mainly acquires an image of the rear of the vehicle **300**. The imaging unit **305** provided to the upper portion of the windshield in the interior of the vehicle mainly acquires an

image of the front of the vehicle **300**. The imaging unit **305** is used to detect, for example, a preceding vehicle, a pedestrian, an obstacle, a traffic light, a traffic sign, a lane, and the like.

[0194] FIG. **22** illustrates an example of imaging ranges of the imaging units **301**, **302**, **303**, and **304** (hereinafter referred to as "imaging units **301** to **304**"). An imaging range **311** represents the imaging range of the imaging unit **301** provided to the front nose. An imaging range **312** represents the imaging range of the imaging unit **302** provided to the left side mirror. An imaging range **313** represents the imaging range of the imaging unit **303** provided to the right side mirror. An imaging range **314** represents the imaging range of the imaging unit **304** provided to the rear bumper or the back door. For example, an overhead view of the vehicle **300** as viewed from above is obtained by superimposing image data captured by the imaging units **301** to **304**. Hereinafter, the imaging ranges **311**, **312**, **313**, and **314** are referred to as the "imaging ranges **311** to **314**".

[0195] At least one of the imaging units **301** to **304** may have a function of acquiring distance information. For example, at least one of the imaging units **301** to **304** may be a stereo camera including a plurality of imaging devices or an imaging device including pixels for phase difference detection.

[0196] For example, the microcomputer **251** (FIG. **21**) calculates a distance to each three-dimensional object within the imaging ranges **311** to **314** and a temporal change in the distance (relative speed with respect to the vehicle **300**) on the basis of the distance information obtained from the imaging units **301** to **304**. On the basis of the calculation results, the microcomputer **251** can extract, as a preceding vehicle, a nearest three-dimensional object that is present on a traveling path of the vehicle **300** and travels in substantially the same direction as the vehicle **300** at a predetermined speed (for example, equal to or more than 0 km/h). Moreover, the microcomputer **251** can set a following distance to be maintained in front of a preceding vehicle in advance, and perform automatic brake control (including following stop control), automatic acceleration control (including following start control), or the like. According to this example, the cooperative control intended for automated driving that makes the vehicle travel autonomously and the like can be performed without depending on the operation of the driver.

[0197] For example, the microcomputer **251** can classify three-dimensional object data related to three-dimensional objects into a two-wheeled vehicle, a standard-sized vehicle, a large-sized vehicle, a pedestrian, a utility pole, and other three-dimensional objects on the basis of the distance information obtained from the imaging units **301** to **304**, extract the classified three-dimensional object data, and use the extracted three-dimensional object data for automatic avoidance of an obstacle. For example, the microcomputer **251** identifies obstacles around the vehicle **300** as obstacles that the driver of the vehicle **300** can recognize visually and obstacles that are difficult for the driver of the vehicle **300** to recognize visually. Then, the microcomputer **251** determines a collision risk indicating a risk of collision with each obstacle, and in a situation in which the collision risk is equal to or higher than a set value and there is thus a possibility of collision, the microcomputer **251** outputs a warning to the driver via the audio speaker **261** or the display unit **262**, and performs forced deceleration or avoidance steering via the driving system control unit **210** to assist in driving to avoid collision.

[0198] At least one of the imaging units **301** to **304** may be an infrared camera that detects infrared light. The microcomputer **251** can, for example, recognize a pedestrian by determining whether or not there is a pedestrian in images captured by the imaging units **301** to **304**. Such recognition of a pedestrian is, for example, performed by a procedure of extracting characteristic points in the images captured by the imaging units **301** to **304** as infrared cameras and a procedure of determining whether or not an object is a pedestrian by performing pattern matching processing on a series of characteristic points representing the contour of the object. In a case where the microcomputer **251** determines that there is a pedestrian in the captured images captured by the imaging units **301** to **304** and recognizes the pedestrian, the sound/image output unit **252** controls the display unit **262** so that a square contour line for emphasis is displayed in a superimposed manner on the recognized pedestrian. Furthermore, the sound/image output unit **252** may also control the display unit **262** so that an icon or the like representing the pedestrian is displayed at a desired position.

[0199] FIG. **23** is a diagram illustrating an example of a schematic configuration of an endoscopic surgery system to which the technology according to the present disclosure (the present technology) can be applied.

[0200] In FIG. **23**, a state is illustrated in which a surgeon (medical doctor) **531** is using an endoscopic surgery system **400** to perform surgery for a patient **532** on a patient bed **533**. As illustrated, the endoscopic surgery system **400** includes an endoscope **500**, other surgical tools **510** such as a pneumoperitoneum tube **511** and an energy treatment tool **512**, a supporting arm device **520** for supporting the endoscope **500**, and a cart **600** on which various devices for endoscopic surgery are mounted.

[0201] The endoscope **500** includes a lens barrel **501** having a region of a predetermined length from a distal end thereof to be inserted into a body cavity of the patient **532**, and a camera head **502** connected to a proximal end of the lens barrel **501**. Although the illustrated example illustrates the endoscope **500** configured as a so-called rigid endoscope having a rigid lens barrel **501**, the endoscope **500** may be a so-called flexible endoscope having a flexible lens barrel.

[0202] An opening in which an objective lens is fitted is provided at the distal end of the lens barrel **501**. A light source device **603** is connected to the endoscope **500**, and light generated by the light source device **603** is guided to the distal end of the lens barrel by a light guide extending in the lens barrel **501** and is emitted to an observation target in the body cavity of the patient **532** through the objective lens. Note that the endoscope **500** may be a forward-viewing endoscope, an oblique-viewing endoscope, or a side-viewing endoscope.

[0203] An optical system and an imaging element are provided in the camera head **502**, and light reflected by the observation target (observation light) is collected on the imaging element by the optical system. The imaging element photoelectrically converts the observation light and generates an electric signal corresponding to the observation light, that is, an image signal corresponding to an observation image. The image signal is transmitted to a camera control unit (CCU) **601** as RAW data.

[0204] The CCU **601** includes a central processing unit (CPU), a graphics processing unit (GPU), and the like, and integrally controls the operations of the endoscope **500** and a display device **602**. Moreover, the CCU **601** receives the image signal from the camera head **502** and applies, on the image signal, various types of image processing, for example, development processing (demosaicing processing) or the like for displaying an image based on the image signal.

[0205] The display device **602** displays the image based on the image signal which has been subjected to the image processing by the CCU **601** under the control of the CCU **601**.

[0206] The light source device **603** includes, for example, a light source such as a light emitting diode (LED), and supplies irradiation light for imaging a surgical site or the like to the endoscope **500**.

[0207] An input device **604** is an input interface for the endoscopic surgery system **11000**. A user may input various types of information and instructions to the endoscopic surgery system **400** via the input device **604**. For example, the user inputs an instruction and the like to change an imaging condition (type of irradiation light, magnification, focal length and the like) by the endoscope **500**.

[0208] A treatment tool control device **605** controls driving of the energy treatment tool **512** for tissue cauterization, incision, blood vessel sealing, and the like. A pneumoperitoneum device **606** sends gas into the body cavity of the patient **532** via the pneumoperitoneum tube **511** in order to inflate the body cavity for a purpose of securing a field of view by the endoscope **500** and securing work space for the surgeon. A recorder **607** is a device that can record various types of information regarding surgery. A printer **608** is a device that can print various types of information regarding surgery in various formats such as a text, an image, or a graph.

[0209] Note that, the light source device **603** which supplies the irradiation light for imaging the surgical site to the endoscope **500** may include, for example, an LED, a laser light source, or a white light source obtained by combining these. In a case where the white light source includes a combination of RGB laser light sources, because an output intensity and an output timing of each color (each wavelength) can be controlled with high accuracy, the light source device **603** can adjust white balance of a captured image. Furthermore, in this case, by irradiating the observation target with the laser light from each of the R, G, and B laser light sources in time division and controlling driving of the imaging element of the camera head **502** in synchronism with the irradiation timing, images corresponding to R, G, and B can be captured in time division. According to this method, a color image can be obtained even if color filters are not provided for the imaging element.

[0210] Furthermore, the driving of the light source device **603** may be controlled such that the intensity of light to be output is changed every predetermined time. The driving of the imaging element of the camera head **502** is controlled in synchronization with a timing of changing the light intensity to obtain the images in time division, and the obtained images are synthesized to enable generation of an image with a high dynamic range that does not have so-called black defect and halation.

[0211] Furthermore, the light source device **603** may be able to supply light in a predetermined wavelength band adapted to special light observation. In special light observation, for example, by utilizing the wavelength dependency of absorption of light in a body tissue to irradiate light of a narrow band in comparison with irradiation light upon ordinary observation (namely, white light), narrow band observation (narrow band imaging) of imaging a predetermined tissue such as a blood vessel of a superficial portion of the mucous membrane or the like in a high contrast is performed. Alternatively, in special light observation, fluorescent observation for obtaining an image from fluorescent light generated by irradiation of excitation light may be performed. In fluorescent observation, it is possible to perform observation of fluorescent light from a body tissue by irradiating excitation light on the body tissue (autofluorescence observation) or to obtain a fluorescent light image by locally injecting a reagent such as indocyanine green (ICG) into a body tissue and irradiating excitation light corresponding to a fluorescent light wavelength of the reagent upon the body tissue. The light source device **603** can be configured to supply narrow band light and/or excitation light adapted to such special light observation.

[0212] FIG. **24** is a block diagram illustrating an example of functional configurations of the camera head **502** and the CCU **601** illustrated in FIG. **23**.

[0213] The camera head **502** includes a lens unit **701**, an imaging unit **702**, a drive unit **703**, a communication unit **704**, and a camera head control unit **705**. The CCU **601** includes a communication unit **711**, an image processing unit **712**, and a control unit **713**. The camera head **502** and the CCU **601** are connected to each other communicably by a transmission cable **700**.

[0214] The lens unit **701** is an optical system provided at a connecting portion with the lens barrel **501**. The observation light captured from the distal end of the lens barrel **501** is guided to the camera head **502** and enters the lens unit **701**. The lens unit **701** is configured by combining a plurality of lenses including a zoom lens and a focus lens.

[0215] The imaging unit **702** includes an imaging element. The number of imaging elements included in the imaging unit **702** may be one (so-called single plate type) or two or more (so-called multiple plate type). In a case where the imaging unit **702** is configured as the multiple plate type, for example, image signals corresponding to R, G, and B may be generated by the respective imaging elements, and a color image may be obtained by combining the generated image signals. Alternatively, the imaging unit **702** may include a pair of imaging elements for obtaining right-eye and left-eye image signals corresponding to three-dimensional (3D) display. By performing the 3D display, the surgeon **531** can grasp a depth of a living body tissue in a surgical site more accurately. Note that, in a case where the imaging unit **702** is configured as the multiple plate type, a plurality of systems of lens units **701** may be provided so as to correspond to the respective imaging elements. The imaging unit **702** is, for example, the solid-state imaging device of any of the first to eleventh embodiments.

[0216] Furthermore, the imaging unit **702** is not necessarily provided in the camera head **502**. For example, the imaging unit **702** may be provided inside the lens barrel **501** immediately behind the objective lens.

[0217] The drive unit **703** includes an actuator and moves the zoom lens and the focusing lens of the lens unit **701** by a predetermined distance along an optical axis under the control of the camera head control unit **705**. With this

arrangement, the magnification and focal point of the image captured by the imaging unit **702** may be appropriately adjusted.

[0218] The communication unit **704** includes a communication device for transmitting and receiving various types of information to and from the CCU **601**. The communication unit **704** transmits the image signal obtained from the imaging unit **702** as RAW data to the CCU **601** via the transmission cable **700**.

[0219] Furthermore, the communication unit **704** receives a control signal for controlling driving of the camera head **502** from the CCU **601** and supplies the control signal to the camera head control unit **705**. The control signal includes information relating to image pickup conditions such as, for example, information that a frame rate of a picked up image is designated, information that an exposure value upon image picking up is designated and/or information that a magnification and a focal point of a picked up image are designated.

[0220] Note that the imaging conditions such as the frame rate, exposure value, magnification, and focus described above may be appropriately specified by the user, or may be automatically set by the control unit **713** of the CCU **601** on the basis of the acquired image signal. In the latter case, the endoscope **500** is equipped with a so-called auto exposure (AE) function, an auto focus (AF) function, and an auto white balance (AWB) function.

[0221] The camera head control unit **705** controls the driving of the camera head **502** on the basis of the control signal from the CCU **601** received via the communication unit **704**.

[0222] The communication unit **711** includes a communication device for transmitting and receiving various types of information to and from the camera head **502**. The communication unit **711** receives the image signal transmitted from the camera head **502** via the transmission cable **700**.

[0223] Furthermore, the communication unit **711** transmits the control signal for controlling the driving of the camera head **502** to the camera head **502**. The image signal and the control signal can be transmitted by electrical communication, optical communication or the like.

[0224] The image processing unit **712** performs various types of image processing on the image signal which is the RAW data transmitted from the camera head **502**.

[0225] The control unit **713** performs various types of control regarding imaging of the surgical site and the like by the endoscope **500** and display of the captured image obtained by the imaging of the surgical site and the like. For example, the control unit **713** generates the control signal for controlling the driving of the camera head **502**.

[0226] Furthermore, the control unit **713** allows the display device **602** to display the captured image including the surgical site and the like on the basis of the image signal subjected to the image processing by the image processing unit **712**. At this time, the control unit **713** may recognize various objects in the captured image using various image recognition technologies. For example, the control unit **713** may detect edge shapes, colors, and the like of the objects included in the captured image, to recognize the surgical tool such as forceps, a specific living body site, bleeding, mist when the energy treatment tool **512** is used, and the like. At the time of causing the display device **602** to display the captured image, the control unit **713** may superimpose various types of surgery assistance information on the image of the surgical site using the recognition result. The surgery assistance information is displayed to be superimposed and presented to the surgeon **531**, which can reduce the burden on the surgeon **531** and enable the surgeon **531** to reliably proceed with surgery.

[0227] The transmission cable **700** connecting the camera head **502** and the CCU **601** is an electric signal cable compatible with communication of electric signals, an optical fiber compatible with optical communication, or a composite cable thereof.

[0228] Here, in the illustrated example, the communication is performed wired using the transmission cable **700**, but the communication between the camera head **502** and the CCU **601** may be performed wirelessly.

[0229] Although the embodiments of the present disclosure have been described above, these embodiments may be implemented with various modifications within a scope not departing from the gist of the present disclosure. For example, two or more embodiments may be implemented in combination.

[0230] Note that the present disclosure can also have the following configurations.

(1)

[0231] A solid-state imaging device including:

[0232] a first substrate;

[0233] a photoelectric conversion unit provided in the first substrate;

[0234] a floating diffusion unit provided in the first substrate;

[0235] a pixel transistor electrically connected to the floating diffusion unit; and

[0236] a capacitor including a first electrode electrically connected or connectable to the pixel transistor, a second electrode different from the first electrode, and a first ferroelectric film or a first antiferroelectric film provided between the first electrode and the second electrode.

(2)

[0237] The solid-state imaging device according to (1), in which the pixel transistor is an amplifying transistor having a gate electrically connected to the floating diffusion unit and a source or a drain electrically connected to or connectable to the first electrode.

(3)

[0238] The solid-state imaging device according to (1), in which the first electrode is electrically connectable to the pixel transistor via a switch transistor.

(4)

[0239] The solid-state imaging device according to (1), in which the first ferroelectric film or the first antiferroelectric film contains hafnium (Hf), zirconium (Zr), niobium (Nb), scandium (Sc), yttrium (Y), lanthanum (La), germanium (Ge), or silicon (Si).

(5)

[0240] The solid-state imaging device according to (1),

[0241] in which the capacitor is provided on a first surface side of the first substrate, and

[0242] the solid-state imaging device further includes a lens provided on a second surface side of the first substrate.

(6)

[0243] The solid-state imaging device according to (1), further including a second substrate bonded to the first substrate,

[0244] in which the pixel transistor and the capacitor are provided between the first substrate and the second substrate.

(7)

[0245] The solid-state imaging device according to (6),

[0246] in which the pixel transistor is provided in a first insulating film provided on the first substrate, and

[0247] the capacitor is provided in a second insulating film provided on the second substrate and located between the second substrate and the first insulating film.

(8)

[0248] The solid-state imaging device according to (6), further including a third substrate provided between the first substrate and the second substrate,

[0249] in which the capacitor is provided between the second substrate and the third substrate.

(9)

[0250] The solid-state imaging device according to (1), in which a capacity of the capacitor is controlled to be set to only one of a plurality of types of values.

(10)

[0251] The solid-state imaging device according to (1), further including a memory including a third electrode and a fourth electrode different from the third electrode,

[0252] in which the memory

[0253] includes a second ferroelectric film between the third electrode and the fourth electrode in a case where the capacitor includes the first ferroelectric film, and

[0254] includes a second antiferroelectric film between the third electrode and the fourth electrode in a case where the capacitor includes the first antiferroelectric film.

(11)

[0255] The solid-state imaging device according to (10),

[0256] in which the third electrode is formed of the same material as the first electrode,

[0257] the fourth electrode is formed of the same material as the second electrode, and

[0258] the second ferroelectric film or the second antiferroelectric film is formed of the same material as the first ferroelectric film or the first antiferroelectric film.

(12)

[0259] A solid-state imaging device including:

[0260] a first substrate;

[0261] a photoelectric conversion unit provided in the first substrate;

[0262] a floating diffusion unit provided in the first substrate;

[0263] a capacitor including a first electrode provided on a first surface side or a second surface side of the first substrate, a second electrode different from the first electrode, and a first ferroelectric film, a first antiferroelectric film, or a first paraelectric film provided between the first electrode and the second electrode; and

[0264] a memory including a third electrode and a fourth electrode different from the third electrode,

[0265] in which the memory

[0266] includes a second ferroelectric film between the third electrode and the fourth electrode in a case where the capacitor includes the first ferroelectric film,

[0267] includes a second antiferroelectric film between the third electrode and the fourth electrode in a case where the capacitor includes the first antiferroelectric film, and

[0268] includes a second paraelectric film between the third electrode and the fourth electrode in a case where the capacitor includes the first paraelectric film.

(13)

[0269] The solid-state imaging device according to (12),

[0270] in which the third electrode is formed of the same material as the first electrode,

[0271] the fourth electrode is formed of the same material as the second electrode, and

[0272] the second ferroelectric film, the second antiferroelectric film, or the second paraelectric film is formed of the same material as the first ferroelectric film, the first antiferroelectric film, or the second paraelectric film.

(14)

[0273] The solid-state imaging device according to (12), in which the first and second ferroelectric films, the first and second antiferroelectric films, or the first and second paraelectric films contain hafnium (Hf), zirconium (Zr), niobium (Nb), scandium (Sc), yttrium (Y), lanthanum (La), germanium (Ge), or silicon (Si).

(15)

[0274] The solid-state imaging device according to (12),

[0275] in which the capacitor and the memory are provided on the first surface side of the first substrate, and

[0276] the solid-state imaging device further includes a lens provided on the second surface side of the first substrate.

(16)

[0277] The solid-state imaging device according to (12), further including a pixel transistor electrically connected to the floating diffusion unit,

[0278] in which the first electrode is electrically connected or connectable to the pixel transistor.

(17)

[0279] The solid-state imaging device according to (16), further including a second substrate bonded to the first substrate,

[0280] in which the pixel transistor, the capacitor, and the memory are provided between the first substrate and the second substrate.

(18)

[0281] The solid-state imaging device according to (17),

[0282] in which the pixel transistor is provided in a first insulating film provided on the first substrate, and

[0283] the capacitor and the memory are provided in a second insulating film provided on the second substrate and located between the second substrate and the first insulating film.

(19)

[0284] The solid-state imaging device according to (17), further including a third substrate provided between the first substrate and the second substrate,

[0285] in which the capacitor and the memory are provided between the second substrate and the third substrate.

(20)

[0286] The solid-state imaging device according to (12), in which the capacitor and the memory have portions provided in the same transverse plane.

REFERENCE SIGNS LIST

[0287] **1** Pixel
[0288] **2** Pixel array region
[0289] **3** Control circuit
[0290] **4** Vertical drive circuit
[0291] **5** Column signal processing circuit
[0292] **6** Horizontal drive circuit
[0293] **7** Output circuit
[0294] **8** Vertical signal line
[0295] **9** Horizontal signal line
[0296] **11** Substrate
[0297] **11***a* Well region
[0298] **11***b* Diffusion region
[0299] **11***c* Diffusion region
[0300] **11***d* Diffusion region
[0301] **11***e* Diffusion region
[0302] **11***f* Diffusion region
[0303] **12** Element isolation insulating film
[0304] **13** Gate insulating film
[0305] **14** Gate electrode
[0306] **15** Sidewall insulating film
[0307] **16** Interlayer insulating film
[0308] **21** Contact plug
[0309] **22** Wiring
[0310] **22'** Wiring
[0311] **22"** Wiring
[0312] **23** Contact hole
[0313] **24** Wiring
[0314] **25** Wiring
[0315] **26** Wiring
[0316] **27** Electrode
[0317] **28** Ferroelectric film
[0318] **29** Electrode
[0319] **31** Via plug
[0320] **32** Wiring
[0321] **32'** Wiring
[0322] **32"** Wiring
[0323] **33** Via plug
[0324] **34** Wiring
[0325] **34"** Wiring
[0326] **41** On-chip filter
[0327] **42** On-chip lens
[0328] **51** Substrate
[0329] **52** Gate insulating film
[0330] **53** Gate electrode
[0331] **54** Sidewall insulating film
[0332] **55** Interlayer insulating film
[0333] **61** Contact plug
[0334] **61'** Contact plug
[0335] **62** Wiring
[0336] **62'** Wiring
[0337] **63** Contact hole
[0338] **63'** Contact hole
[0339] **64** Wiring
[0340] **64'** Wiring
[0341] **65** Wiring
[0342] **65'** Wiring
[0343] **65"** Wiring
[0344] **66** Wiring
[0345] **67** Wiring
[0346] **68** Wiring
[0347] **71** Circuit region
[0348] **72** Sample hold region
[0349] **73** Memory region
[0350] **81** Ferroelectric film
[0351] **82** Paraelectric film
[0352] **91** Connecting portion
[0353] **91***a* Pad portion
[0354] **91***b* Pad portion
[0355] **91***c* Via portion
[0356] **91***d* Via portion
[0357] **92** Signal processing unit
[0358] **92***a* A/D converter
[0359] **92***b* Reference voltage generation unit
[0360] **92***c* Data latch unit
[0361] **92***d* Current source
[0362] **92***e* Decoder
[0363] **92***f* Row decoder
[0364] **92***g* I/F unit
[0365] **93** Memory unit
[0366] **94** Data processing unit
[0367] **95** Control unit
[0368] **96** Row selection unit

1. A solid-state imaging device comprising:
a first substrate;
a photoelectric conversion unit provided in the first substrate;
a floating diffusion unit provided in the first substrate;
a pixel transistor electrically connected to the floating diffusion unit; and
a capacitor including a first electrode electrically connected or connectable to the pixel transistor, a second electrode different from the first electrode, and a first ferroelectric film or a first antiferroelectric film provided between the first electrode and the second electrode.

2. The solid-state imaging device according to claim **1**, wherein the pixel transistor is an amplifying transistor having a gate electrically connected to the floating diffusion unit and a source or a drain electrically connected to or connectable to the first electrode.

3. The solid-state imaging device according to claim **1**, wherein the first electrode is electrically connectable to the pixel transistor via a switch transistor.

4. The solid-state imaging device according to claim **1**, wherein the first ferroelectric film or the first antiferroelectric film contains hafnium (Hf), zirconium (Zr), niobium (Nb), scandium (Sc), yttrium (Y), lanthanum (La), germanium (Ge), or silicon (Si).

5. The solid-state imaging device according to claim **1**,
wherein the capacitor is provided on a first surface side of the first substrate, and
the solid-state imaging device further includes a lens provided on a second surface side of the first substrate.

6. The solid-state imaging device according to claim **1**, further comprising a second substrate bonded to the first substrate,
wherein the pixel transistor and the capacitor are provided between the first substrate and the second substrate.

7. The solid-state imaging device according to claim **6**,
wherein the pixel transistor is provided in a first insulating film provided on the first substrate, and

the capacitor is provided in a second insulating film provided on the second substrate and located between the second substrate and the first insulating film.

8. The solid-state imaging device according to claim **6**, further comprising a third substrate provided between the first substrate and the second substrate,

wherein the capacitor is provided between the second substrate and the third substrate.

9. The solid-state imaging device according to claim **1**, wherein a capacity of the capacitor is controlled to be set to only one of a plurality of types of values.

10. The solid-state imaging device according to claim **1**, further comprising a memory including a third electrode and a fourth electrode different from the third electrode,

wherein the memory

includes a second ferroelectric film between the third electrode and the fourth electrode in a case where the capacitor includes the first ferroelectric film, and

includes a second antiferroelectric film between the third electrode and the fourth electrode in a case where the capacitor includes the first antiferroelectric film.

11. The solid-state imaging device according to claim **10**,

wherein the third electrode is formed of the same material as the first electrode,

the fourth electrode is formed of the same material as the second electrode, and

the second ferroelectric film or the second antiferroelectric film is formed of the same material as the first ferroelectric film or the first antiferroelectric film.

12. A solid-state imaging device comprising:

a first substrate;

a photoelectric conversion unit provided in the first substrate;

a floating diffusion unit provided in the first substrate;

a capacitor including a first electrode provided on a first surface side or a second surface side of the first substrate, a second electrode different from the first electrode, and a first ferroelectric film, a first antiferroelectric film, or a first paraelectric film provided between the first electrode and the second electrode; and

a memory including a third electrode and a fourth electrode different from the third electrode,

wherein the memory

includes a second ferroelectric film between the third electrode and the fourth electrode in a case where the capacitor includes the first ferroelectric film,

includes a second antiferroelectric film between the third electrode and the fourth electrode in a case where the capacitor includes the first antiferroelectric film, and

includes a second paraelectric film between the third electrode and the fourth electrode in a case where the capacitor includes the first paraelectric film.

13. The solid-state imaging device according to claim **12**,

wherein the third electrode is formed of the same material as the first electrode,

the fourth electrode is formed of the same material as the second electrode, and

the second ferroelectric film, the second antiferroelectric film, or the second paraelectric film is formed of the same material as the first ferroelectric film, the first antiferroelectric film, or the second paraelectric film.

14. The solid-state imaging device according to claim **12**, wherein the first and second ferroelectric films, the first and second antiferroelectric films, or the first and second paraelectric films contain hafnium (Hf), zirconium (Zr), niobium (Nb), scandium (Sc), yttrium (Y), lanthanum (La), germanium (Ge), or silicon (Si).

15. The solid-state imaging device according to claim **12**,

wherein the capacitor and the memory are provided on the first surface side of the first substrate, and

the solid-state imaging device further includes a lens provided on the second surface side of the first substrate.

16. The solid-state imaging device according to claim **12**, further comprising a pixel transistor electrically connected to the floating diffusion unit,

wherein the first electrode is electrically connected or connectable to the pixel transistor.

17. The solid-state imaging device according to claim **16**, further comprising a second substrate bonded to the first substrate,

wherein the pixel transistor, the capacitor, and the memory are provided between the first substrate and the second substrate.

18. The solid-state imaging device according to claim **17**,

wherein the pixel transistor is provided in a first insulating film provided on the first substrate, and

the capacitor and the memory are provided in a second insulating film provided on the second substrate and located between the second substrate and the first insulating film.

19. The solid-state imaging device according to claim **17**, further comprising a third substrate provided between the first substrate and the second substrate,

wherein the capacitor and the memory are provided between the second substrate and the third substrate.

20. The solid-state imaging device according to claim **12**, wherein the capacitor and the memory have portions provided in the same transverse plane.

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