| | |
|---|---|
| United States Patent Application Publication | 20250266401 |
| Kind Code | A1 |
| Publication Date | August 21, 2025 |
| Inventor(s) | Uzoh; Cyprian Emeka et al. |

## DIRECT BONDED STACK STRUCTURES FOR INCREASED RELIABILITY AND IMPROVED YIELD IN MICROELECTRONICS

### Abstract

Direct bonded stack structures for increased reliability and improved yields in microelectronics are provided. Structural features and stack configurations are provided for memory modules and 3DICs to reduce defects in vertically stacked dies. Example processes alleviate warpage stresses between a thicker top die and direct bonded dies beneath it, for example. An etched surface on the top die may relieve warpage stresses. An example stack may include a compliant layer between dies. Another stack configuration replaces the top die with a layer of molding material to circumvent warpage stresses. An array of cavities on a bonding surface can alleviate stress forces. One or more stress balancing layers may also be created on a side of the top die or between other dies to alleviate or counter warpage. Rounding of edges can prevent stresses and pressure forces from being destructively transmitted through die and substrate layers. These measures may be applied together or in combinations in a single package.

**Inventors:** **Uzoh; Cyprian Emeka (San Jose, CA), Katkar; Rajesh (Milpitas, CA), Workman; Thomas (San Jose, CA), Gao; Guilian (Campbell, CA), Fountain, JR.; Gaius Gillman (Youngsville, NC), Mirkarimi; Laura Wills (Sunol, CA), Haba; Belgacem (Saratoga, CA), Guevara; Gabriel Z. (Gilroy, CA), Watanabe; Joy (Campbell, CA)**

**Applicant:** **ADEIA SEMICONDUCTOR BONDING TECHNOLOGIES INC.** (San Jose, CA)

**Family ID:** **1000008578028**

**Appl. No.:** **19/169894**

**Filed:** **April 03, 2025**

### Related U.S. Application Data

parent US continuation 18589231 20240227 parent-grant-document US 12272677 child US 19169894
parent US continuation 17681563 20220225 parent-grant-document US 11955463 child US 18589231
parent US continuation 16911360 20200624 parent-grant-document US 11296053 child US 17681563
us-provisional-application US 62866965 20190626

---

## Publication Classification

**Int. Cl.:** **H01L25/065** (20230101); **H01L21/56** (20060101); **H01L23/00** (20060101); **H01L23/31** (20060101)

**U.S. Cl.:**

CPC **H01L25/0657** (20130101); **H01L21/561** (20130101); **H01L23/3121** (20130101); **H01L24/97** (20130101); H01L2224/0401 (20130101); H01L2924/3511 (20130101); H01L2924/35121 (20130101)

---

## Background/Summary

INCORPORATION BY REFERENCE TO ANY PRIORITY APPLICATIONS [0001] Any and all applications for which a foreign or domestic priority claim is identified in the Application Data Sheet as filed with the present application are hereby incorporated by reference under 37 CFR 1.57.

BACKGROUND
[0002] Stacks of integrated circuit microchips ("dies") bonded together during fabrication of conventional 3DIC microelectronic packages, such as high bandwidth memory modules (HBM, HBM2, HBM3), are vulnerable to certain types of defects by virtue of the vertical stacking, and these defects affect the overall production yield. In the case of the HBM2 modules, for example, memory specifications may dictate some physical dimensions of the modules to be constructed, such as a 700 μm height requirement.
[0003] As shown in FIG. **1**, the high bandwidth of an example conventional HBM2 memory module **100** is achieved by bonding multiple memory dies **102** together in a vertical stack **103** on a substrate **104**. Each individual die **102** may have a certain vertical thickness, such as 55 μm. At the top of the vertical stack, a top die **106** to be added is often made thicker than the other dies **102** in order to reach the 700 μm (or other) specification for height. For example, the top die **106** may be 90-400 μm in thickness, compared to 55 μm in thickness for each of the dies **102** below the top die **106**. In some cases, this top die **106** may be a dummy or spacer die. The module **100** may be filled out and completed with a side filler **108**, underfill, or molding material.
[0004] The thicker top die **106** may cause structural problems for the dies **102** stacked beneath it during fabrication, decreasing the average reliability and overall production yield. For various reasons, the multiple thin dies **102** forming the vertical memory stack **103** under the top die **106** may assume a negative warpage, with the warp facing concave side down **110**. The thicker top die **106** often ends up with a positive warpage, facing concave-up **112**. When the concave-up top die **106** is pressed into the concave-down stack of dies **102** beneath it during bonding to the vertical stack **103**, destructive defects such as cracking **114** of the direct bonded dies **102**, delamination **116** of the bond between dies, or cracking and chipping **118** of the substrate **104** underlying the vertical stack at points of increased pressure may occur in a certain number of instances, decreasing overall

yield. The cracking **114** of thin dies **102** may occur near the edges of the dies **102**, when there is a slight difference in footprint sizes between the dies **102**, creating small overhangs where pressure forces can concentrate.

SUMMARY

[0005] Direct bonded stack structures for increased reliability and improved yields in microelectronics are provided. Structural features and stack configurations are provided for memory modules and 3DICs to reduce both severe and minor defects in vertically stacked dies. Example processes alleviate warpage stresses between a thicker top die and direct bonded dies beneath it, for example. In one technique, an etched surface on the top die may relieve warpage stresses. In another technique, an example stack may include a compliant layer between the top die and dies beneath it. Another example stack configuration replaces the top die with a layer of molding material to circumvent warpage stresses. An array of cavities on the bonding surface of the top die can also alleviate stress forces. One or more stress balancing layers may also be created on the topside or backside of the top die, or between thin dies as another way to relieve stack stresses and warpage. Rounding of edges can prevent stresses and pressure forces from being destructively transmitted through die and substrate layers. These various techniques and structures are not mutually exclusive, but may be used together or in various combinations in the package.

[0006] This summary is not intended to identify key or essential features of the claimed subject matter, nor is it intended to be used as an aid in limiting the scope of the claimed subject matter.

---

## Description

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. **1** is a diagram of a conventional prior art vertical die stack with structural problems introduced by various stresses and die warpage, including delamination of bonds, cracking, and chipping resulting in unreliability and decreased production yield.

[0008] FIG. **2** is a diagram of an example module with a grind/etch feature for alleviating a warpage stresses in a vertical stack of dies.

[0009] FIG. **3** is a flow diagram of an example process for making the structure of FIG. **2**.

[0010] FIG. **4** is a diagram of an example module with a vertical die stack that includes a compliant layer feature for alleviating a warpage stress in the vertical stack.

[0011] FIG. **5** is a flow diagram of an example process for fabricating the example module FIG. **4**.

[0012] FIG. **6** is a diagram of an example module with a die stack that includes a molding feature for alleviating a warpage stress in the vertical stack.

[0013] FIG. **7** is a flow diagram of an example process for fabricating the example module of FIG. **6**.

[0014] FIG. **8** is a diagram of an example module with a vertical die stack, including a relief cavity feature for alleviating a warpage stress in the vertical stack.

[0015] FIG. **9** is a flow diagram of an example process for fabricating the example module of FIG. **8**.

[0016] FIG. **10** is a diagram of an example module with a die stack that includes a stress balancing layer feature for alleviating a warpage stress in the vertical stack.

[0017] FIG. **11** is a flow diagram of an example process for fabricating the example module of FIG. **10**.

[0018] FIG. **12** is a diagram of an example module of vertically stacked dies with at least some rounded corners or edges to prevent stress concentration at corners.

[0019] FIG. **13** is a flow diagram of an example process for preventing concentration of damaging forces in fabrication of a vertical stack of dies.

[0020] FIG. **14** is a diagram of an example module with multiple thin dies substituting for a large die to reduce stress warpage in a die stack.

[0021] FIG. **15** is a diagram of an example structure including a lateral support for eliminating warpage problems and increasing yield in fabrication of modules with vertical die stacks.

[0022] FIG. **16** is a diagram of an example structure with no top die spacer, and with lateral support structures and molding, for reducing interior stresses.

[0023] FIG. **17** is a diagram of example structures formed in a process that uses temperature differentials to reduce warpage stresses during fabrication of vertical stacks of dies.

[0024] FIG. **18** is a diagram of example structures and associated processes for making an example module of stacked dies by uniting multiple pre-made stacks of dies, while reducing interior stress warpage.

[0025] FIG. **19** is a diagram of an example structure with features for alleviating warpage stresses in stacks of dies, including rounded die corners supported by an encapsulant fillet or wedge.

[0026] FIG. **20** is a diagram of example structures for constructing larger modules that have numerous stacked dies, without introducing problems caused by stress warpage.

[0027] FIG. **21** is a diagram of example structures including thin layers of dielectric material and features for reducing interior stresses.

[0028] FIG. **22** is another diagram of example structures possible that include features for reducing interior stresses.

[0029] FIG. **23** is a diagram of an example structure with one or more direct bonded die stacks incorporating stress-relief measures, a processor, and optional heat sink.

## DETAILED DESCRIPTION

### Overview

[0030] This disclosure describes direct bonded stack structures for increased reliability and improved yields in microelectronics. Structural features and stack configurations are provided for memory modules, stacked passive elements, interposers, and 3DICs to reduce both severe and minor defects in vertically stacked dies. Example processes and structures alleviate stresses, such as warpage stresses, between a thicker top die and direct bonded dies beneath it or a thinner top die directly bonded to a thicker die beneath, for example.

[0031] In an implementation, a surface that has been ground and etched on the top die may relieve stresses, such as warpage stresses, of the stack of dies. In the same or another implementation, the example stack may include a compliant layer between the top die and dies beneath it to relieve warpage stresses. In an implementation, another stack configuration replaces the top die with a layer of molding material to circumvent warpage stresses. In another implementation, an array of cavities on the bonding surface of the top die or elsewhere can alleviate stress forces. Yet again, a stress balancing layer may also be created on the topside or backside of the top die to relieve warpage stresses of the stack, or one or more stress balancing layers can intervene between other dies in a stack of dies. In another example technique and related structure, right-angle corners of some dies in a stack are rounded to prevent concentration of pressing forces at square corners of dies during stack fabrication, and to prevent transmission of those concentrated forces to relatively fragile dies or substrate layer below or above, cracking and chipping them.

### Example Processes and Systems

[0032] Example processes fabricate stack structures with structural features and configurations to reduce severe and minor defects that can occur in vertical stacks of direct bonded dies. Memory modules include, but are not limited to, 3DS®, HMC hybrid memory cube, HBM, HBM2 and HBM3, which are described below as representative examples, but the described technology can be applied to any microelectronics package with vertically stacked dies, especially dies that are direct bonded together, and the structures and techniques described herein are not limited to memory modules.

[0033] It should be noted that the embodiments described below can in some cases be combined together in a single embodiment that includes the features of each embodiment described below.

The embodiments described below are not intended to be mutually exclusive, but may be combined together, when possible.

[0034] FIG. **2** shows an example memory module **200** with a die stack **202** that includes a feature for alleviating a warpage stress in the vertical stack **202**. The top die **106** of the stack **202** has a surface that is treated by grinding **204** and then either wet etching **206** or dry etching **206** to relieve a warpage **112** or an internal stress of the top die **106**, thus decreasing or eliminating its concavity **112** in some cases. The etching **206** relieves pent up stress from the grinding operation **204**. This in turn helps to relieve defects resulting from stress forces that can occur between the top die **106** and the dies **102** beneath it. As above, substrate **104** may be an organic or inorganic structure, such as a circuit board, package substrate, die, wafer, carrier etc, which may be electrically coupled to the stack **202**, including coupling at least in part through direct and/or hybrid bonding, eutectic bonding, etc.

[0035] FIG. **3** shows an example process **300** for making the structure **200** of FIG. **2**. In FIG. **3**, operations of the example process are shown in individual blocks.

[0036] At block **302**, the example process includes direct bonding dies **102** together to make part of the vertical stack **202**.

[0037] At block **304**, the top die **106** is prepared for bonding to the top of the other dies **102** to form vertical stack **202**.

[0038] At block **306**, the backside of the top die **106** is ground.

[0039] At block **308**, the backside of the top die **106** is then wet etched **206** or dry etched for stress relief.

[0040] At block **310**, the top die **106** is then bonded to the dies below **102**, to produce a microelectronics package **200** of vertically stacked dies **102** & **106** with reduced internal stress and increased reliability, thereby alleviating a warpage stress between the top die **106** and the dies **102** in the vertical stack beneath the top die **106**.

[0041] FIG. **4** shows an example memory module **400** with a die stack **402** that includes a feature for alleviating a warpage stress in the vertical stack **402**. The vertical stack **402** is fabricated with a compliant layer **404** intervening in between the top die **106** and the dies **102** direct bonded to each other beneath the top die **106**. The top die may have different vertical and/or horizontal dimensions than at least one other die in the direct bonded die stack **400**.

[0042] The compliant layer **404** is intended to cushion uneven forces during bonding of the top die **106** to the vertical stack **402**, and to counteract or dissipate ongoing unevenness of stresses and warpage forces between the top die **106** and the dies **102** beneath. The thickness of the compliant material or compliant layer **404** may range between 0.5-55.0 microns and preferably between 3.0-30.0 microns. The compliant layer **404** may be adhered or bonded between the dies, and can provide a single solution to warpage when the top die **106** is a dummy die for filling the top space of the package **400**. The compliant layer **404** may be adhered or bonded between the dies, and can provide a single solution to warpage when the top die **106** is a dummy die for filling the top space of the package **400**. The Young's modulus of compliant layer **404** is preferably less than 4 GPa.

[0043] In some embodiments, as in stack **400**, the width of the top die **106** is similar to the width of one of the dies below **102**. In other embodiments, as in stack **400′**, the width of the top die **106′** is different from a width of other dies in the vertical stack **400′**, and may be wider than the dies **102** below, for example.

[0044] FIG. **5** shows an example process **500** for fabricating the example module **400** of FIG. **4**. Operations of the example process **500** are shown in individual blocks.

[0045] At block **502**, the example process **500** includes direct bonding dies **102** together to make part of a vertical stack **402**.

[0046] At block **504**, a top die **106** is prepared for bonding to the top of the direct bonded dies **102**.

[0047] At block **506**, a compliant layer **404** is applied to interpose between the top die **106** and other dies **102** of the vertical stack **402**, for example.

[0048] At block **508**, the top die **106** is then bonded to the compliant layer **404**. The compliant layer may be an adhesive or another compliant material bonded by thin film die attach, printed or stenciled die attach material, or other adhesives, for example. The microelectronics package **400** with vertically stacked dies **102** & **106** and compliant layer **404** provides reduced internal stress and increased reliability, alleviating a warpage stress between the top die **106** and the dies **102** of the vertical stack **402**. A flowable material that sets may be used for the compliant layer **404**. The dispensed material flows and will accommodate the warpage very well. In the thin film die attach embodiment, flow is achieved at elevated temperatures and the flowed material also accommodates the height differences across warped dies to alleviate the warpage. The width of the top die **106** may be similar or different than the width of the dies below **102**, as in FIG. **4**.

[0049] FIG. **6** shows as example module, a microelectronics package **600** with a die stack **602** that includes a fill feature for alleviating a warpage stress in the vertical stack **602**. In this example microelectronics package **600**, a volume of molding material **604**, filler, underfill material, etc., substitutes for a top die **106**, which is eliminated in this embodiment. Since there is no conflict of warpage stresses between the positive warpage of a top die that is not present, and the dies **102** of the stack **602** that may have a negative warpage, the actual dies **102** in the vertical stack **602** remain with a slight but acceptable negative warpage, and the microelectronics package **600** is filled out with the molding compound **604** to complete the microelectronics package **600**. The residual negative warpage of the direct bonded dies **102** may also be addressed and alleviated with a stress balancing layer as described with respect to FIGS. **10-11**. One or more stress balancing layers (not shown in FIG. **6**) can be applied on or within the stack **602** to counterbalance and cancel out the net warpage of the entire stack **602**. Or, such stress balancing layers can be matched with each individual die **102** to be bonded into the stack **602**.

[0050] Each stress balancing layer is designed to counteract a camber of a warped die or stack, with an opposite camber of its own, before the stress balancing layer and the warped die or stack are mated together, at which point the cambers cancel each other out resulting in a flat stack **602** with a net overall warp of zero. Also, in the microelectronics package **600**, the lateral width of the molding material **604** on the either side of the stacked dies **602** is smaller than a width of the dies **102** and preferably less than 10% of the width of the dies **102**. In some embodiments, the vertical thickness of the molding material abutting the top **102** die is less than the thickness of the die stack **602** and preferably less than 50% of the vertical thickness of the die stack **602**.

[0051] FIG. **7** shows an example process **700** for fabricating the example module **600** of FIG. **6**. Operations of the example process **700** are shown in individual blocks.

[0052] At block **702**, the example process **700** includes direct bonding dies **102** together to make a vertical stack **602**.

[0053] At block **704**, molding material **604** is at least partly filled around the vertical stack **602** to substitute for the volume of the missing top die **106** and to complete the outer physical dimensions of the memory module **600** to specification. The thickness of the molding material **604** on top of the vertical stack **602** may be multiples of the thickness of an individual die **102** in the vertical stack **602**. For example, the thickness of the molding material **604** may be 3 times the thickness of a die **102** in the vertical stack **602**. One or more stress balancing layers may be added anywhere in or around the stack **602**.

[0054] FIG. **8** shows as example module **800** with a die stack **802** that includes a relief cavity feature for alleviating a warpage stress in the vertical stack **802**. In this example module **800**, relief cavities **804** (not to scale) are made in the bonding surface of the top die **106** to relieve coupling forces between the top die **106** and at least the next die **102'''** beneath the top die **106**. An array of the relief cavities **804** may be placed where coupling forces are known or determined to be detrimental to the stability of the microelectronics package **800**. If the top die **106** is an active die and part of the electronics of the memory module **800** (and not just a dummy die), then there may be metal interconnects, such as direct bonded interconnects, between the top die **106** and the next die **102‴** beneath. Even though the metal interconnects may be rigid, the array of relief cavities **804** may still reduce and relieve coupling forces between the top die **106** and the vertical stack **802** to decrease the effect of warpage forces in the microelectronics package **800**.

[0055] The example relief cavities **804** are typically formed in some portions of the dielectric regions between adjacent interconnects. In other applications, the relief cavities **804** may be formed between the interconnect portion and the edges on the die or singulation lanes. Also, the relief cavities **804** may be continuous or discontinuous and the geometrical profile of a relief cavity **804** may be triangular, rectangular or curvilinear. The depth of the relief cavities **804** may range between a few nanometers to a few microns. In an implementation, it is important that in the immediate region of the relief cavities **804**, the bonding surface of the top die **106** is discontinuous from the surface of the die **102** beneath.

[0056] FIG. **9** shows an example process **900** for fabricating the example module **800** of FIG. **8**. Operations of the example process **900** are shown in individual blocks.

[0057] At block **902**, the example process **900** includes direct bonding dies **102** together to make a vertical stack **802**.

[0058] At block **904**, the top die **106** is prepared for direct bonding to the vertical stack **802**.

[0059] At block **906**, relief cavities **804** are created in the top die **106**.

[0060] At block **908**, the top die **106** is bonded or direct bonded to the vertical stack **802** to create a microelectronics package **800** with warpage stresses alleviated between the top die **106** and the dies **102** of the vertical stack **802** to provide a more reliable package with reduced possibility of severe defects.

[0061] FIG. **10** shows as example memory module **1000** with a die stack **1002** that includes a feature for alleviating a warpage stress in the vertical stack **1002**. In one example embodiment, a stress balancing layer **1004** is created on a backside of the top die **106** (topside of the vertical stack **1002** when the vertical stack **1002** includes the top die **106**). The stress balancing layer **1004** may be made of a hard or firm material applied by physical vapor deposition (PVD) methods, for example, or by other application techniques to prevent warpage from occurring in the first place. The stress balancing layer **1004** may also be one or more firm materials to suppress or counteract the warpage of a die or stack, resulting from construction of the package **1000** or resulting from subsequent thermal changes during operation. The stress balancing layer **1004** may also be a layer that has a warp or camber of its own, designed to counter and cancel out the warpage or stress of a die or stack to which it will be adhered or bonded. The stress balancing layer **1004**, in some configurations, can also redistribute stresses, balancing local stresses by horizontal redistribution of local warps and stress points with other local areas that have the opposite warp or stress, for a net zero overall warpage.

[0062] In some applications and structures **1000′** the stress balancing layer **1004** may be coated on the lower side of the top die **106**. In this arrangement, the stress balancing layer **1004** is disposed between the top die **106** and the bonded die immediately beneath the top die **106** in the stack **1002′**, such as die 4 **102‴** in structure **1000′** of FIG. **10**, for example.

[0063] In structure **1000″**, one or more stress balancing layers **1004** may be placed between the thin dies **102** in a die stack **1002″**, or anywhere in the stack **1002″**.

[0064] Such stress balancing layers **1004** can also be matched with each individual die **102** to be bonded into the stack **1002″**. Each stress balancing layer **1004** is designed to counteract a camber of a warped die **102** or stack **1002**, with an opposite camber of its own. Thus, the stress balancing layer **1004** may apply a slight leaf spring action to the die or stack being unwarped. The opposing cambers cancel each other out when each stress balancing layer **1004** is mated to its warped die or stack, resulting in a flat stack **1002**, or flatter stack **1002**, ideally with a net overall warpage of zero.

[0065] In other embodiments, a stress balancing structure may comprise the stress balancing layer **1004** and a bonding layer, such as a distinct dielectric layer (not shown) and this bonding layer is disposed between the stress balancing layer **1004** and the bonded die immediately beneath, such as die 4 **102**″ in FIG. **10**, for example. In some applications, the dielectric bonding layer may be a thin adhesive layer and the thickness of the adhesive layer is substantially thinner than one of the bonded dies **102**.

[0066] In an implementation, an example stress balancing layer **1004** can be made of one or more conductive layers, for example, an example stress balancing layer **1004** may be made of titanium nitride and/or tantalum (TiN/Ta), or Ta and Al as co-evaporated or co-sputtered layers, or these metals may be deposited sequentially over each other. But the example stress balancing layer **1004** is not limited to these compounds and elements. Multiple stress balancing layers **1004** may be applied and may have different coefficients of thermal expansion (CTEs) to provide different balancing force differentials at different temperatures. Moreover, a bonding layer, such as an oxide, nitride, or similar material may be formed on the stress balancing layer to enable direct or hybrid bonding to another surface. When the stress balancing layer **1004** is a nonconductor, the stress balancing layer **1004** may be able to accommodate vertical conductors, such as TSVs and/or metal interconnects transiting through a thickness of the stress balancing layer **1004**.

[0067] In an implementation, the stress balancing layer **1004** can be made of a photopatterned polymer, which assembles or has a tendency to assemble into a curved geometry. A differentially photo-crosslinked SU-8 photoresist film, for example, may curve upon photolithographic patterning. In another implementation, a polymeric thin film with heterogeneous mechanical properties makes a curved or leaf spring stress balancing layer **1004** to be bonded to a warped die.

[0068] FIG. **11** shows an example process **1100** for fabricating the example module **1000** of FIG. **10** including one or more stress balancing layers **1004**. Operations of the example process **1100** are shown in individual blocks.

[0069] At block **1102**, the example process **1100** includes direct bonding dies **102** together to make a vertical stack **1002** of the dies **102**.

[0070] At block **1104**, a top die **106** is prepared for direct bonding with the vertical stack **1002**.

[0071] At block **1106**, the top die **106** is associated with a stress balancing layer **1004**. In one example process, the top die **106** is pre-coated with the stress balancing layer **1004** prior to its attachment to the vertical stack **1002**. After the attachment step, the new stack may be processed further, for example, undergoing thermal annealing or molding operations.

[0072] At block **1108**, the top die **106** and stress balancing layer **1004** are bonded to the dies **102** in the vertical stack **1002**.

[0073] In a variation of the example process **1100**, one or more stress balancing layers **1004** are placed anywhere in a stack of dies to balance stresses or cancel warpages of a die, a group of dies, or an entire stack of dies.

[0074] FIG. **12** shows a memory module **1200** of vertically stacked dies **102** direct bonded together. Right-angle corners **1204** of some dies **102** in the stack **1202** can be rounded in the x-, y-, and/or z-directions to prevent stress concentration: a concentration of pressing forces **1205** at the conventionally squared corners **1204** of the dies **102** during stack fabrication. The pressing forces **1205** can conventionally crack and chip the fragile dies, or the substrate **104**, below the 90 degree corners. Rounding, chamfering, or otherwise easing the typically sharp 90 degree corners or the edges between the z-plane and the x/y-planes can prevent or disperse transmission of the concentrated pressing forces **1205** to the relatively fragile and brittle dies, or the substrate **104**, beneath. In one embodiment, the edges of the bonded dies **102** of stack **1202** are rounded to prevent point stresses at corners **1204**. In other applications, the edges of the top die **106** may also be rounded.

[0075] FIG. **13** shows an example process **1300** for preventing concentration of damaging forces in fabrication of a vertical stack of dies **1202**. Operations of the example process **1300** are shown in individual blocks.

[0076] At block **1302**, the example process **1300** includes rounding right-angle corners of selected dies to be made into the vertical stack of dies **1202**. The corner-rounding can be achieved, for example, by applying a high pressure dielectric etch during a plasma etching operation. The etching operation may comprise etching the substrate **104** and coated dielectric layers. In other cases, the edges of the dielectric of the bonding surface need to be rounded prior to the bonding operation. In some applications, the boding surface may be shielded with a protectant and the selected edges may be rounded by wet etching methods or by mild abrasive powder blasting operations, or by laser jet methods or combinations thereof. The dies **102** to be used in the stack **1202** are then lined up according to a vertical plane. The dies **102** with at least some rounded corners **1204** are direct bonded together into a stack **1202**, with the rounded corners **1204** preventing pressing forces from concentration at the corners **1204** and also preventing these forces from being transmitted to break, crack, or chip the next die or substrate **104** below.

[0077] FIG. **14** shows another example module **1400**, memory module, or other stacked device, constructed according to one or more techniques for reducing stress warpage in the die stack **1402** making up the module **1400**. In this implementation, instead of using a large monolithic die on top of the die stack **1402**, two or more thinner dies **1404** are bonded on top of the stack **1402** of smaller dies **102**. These thinner dies **1404** on top either conform to the stack below **1402** or can impose a counter-warpage to that of the warpage of the stack **1402** underneath. In some arrangements, a molding material **1406** laterally surrounds the bonded die stack **1402**.

[0078] FIG. **15** shows another example structure **1500** for eliminating warpage problems and reduced yield in fabrication of modules, such as memory modules and other devices with stacked dies.

[0079] A stack of the dies **102** are provided with a lateral support **1502**, such as side buttresses made of underfill material or another firm solid or particulate composite layer. Since the individual dies **102** can be very thin, such as 55 μm in thickness or even thinner, they may be prone to warping. Before a thick top die **1504** is bonded to the stack, the lateral supports **1502** are built against the sides of the stack. These one or more lateral die support structures **1502** may be formed by various dispensing methods including printing or molding methods. During direct bonding of a top dummy die **1504** (or active die) to the stack of dies **102**, for example, the lateral supports **1502** hold the edges of the dies and also stabilize the stack of dies **102** as a whole. A lateral support structure **1502** also reduces incidences of damage to the bonded dies from routine handling operations. This results in a finished module, in which the various dies **102** and **1504** are less prone to chipping or cracking on account of the solid stabilization of the lateral supports **1502**. Side molding **1506** may also be added to further stabilize the stack **102** & **1504** and complete the package. It is of note that the lateral support structure **1502** abuts the periphery of the bonded dies **102** and not that of the top die **1504**. Also, the side molding **1506** is disposed around the bonded dies **102** and the top die **1504**, but the side molding **1506** is not in direct contact with the lower dies **102** of the stacked bonded dies, such as die “1” **102** and die “2” **102′**, for example. Thus, the side molding **1506** directly abuts only some portions of the bonded dies in the bonded dies stack.

[0080] FIG. **16** shows an implementation of a structure **1600** similar to the structure **1500** of FIG. **15**, but the example module **1600** does not use a top extra die **1504**. In this case, side molding **1602** may be used after the lateral supports **1502** are placed, in order to complete a shorter package **1600**. As described earlier, the side molding **1602** directly abuts some portions of the topmost die or dies, and not the other bonded dies in the bonded dies stack. In one embodiment, the side molding **1602** does not directly contact the stacked bonded dies.

[0081] FIG. **17** shows additional example structures **1700** & **1702** for creating modules with stacked dies **102** while reducing stress warpage when the dies **102** are direct bonded in a stack. The example technique also applies when an extra dummy die **1704** is direct bonded on top of the respective stacks with a concavity of warpage that may be different from that of the stack of dies **102** beneath it.

[0082] First, in an example process, multiple thin dies **102** are direct bonded together at a first temperature, for example in the approximate range of 140-350° C. The top die, the extra dummy die **1704**, is then bonded to the stack of dies **102** at a second temperature preferably lower than the first temperature. In one embodiment, for example, the multiple thin dies **102** may be bonded at a temperature sufficiently high for a metallic bond to form between mating metallic electric contacts between intimately mated dies. For example, the mating temperature for the opposing electrical and non-electrical contacts may range between 150-300° C., and preferably between 180-250° C. for a time duration ranging from 45 minutes to 2-4 hours or even longer. The bonding temperature depends on the nature of the mating metal layer. In practice, the higher the bonding temperature, the shorter the bonding times and vice versa.

[0083] The stack of dies **102** is allowed to cool to the lower bonding temperature for additional processing if needed before attaching the top extra dummy die **1704** to the upper surface of the last die in the stack of dies **102**. The attached dummy die **1704** is then bonded at a temperature preferably lower than the metallic mating temperature of the bonded stacked dies. In one embodiment, the dummy die **1704** is bonded at temperatures ranging from below room temperature to below 130° C., and preferably below 100° C. Reducing the bonding temperature of the top die **1704** reduces the stress transmitted from the die **1704** to bonded dies beneath, such as in example stacks **602** (FIG. **6**), stack **1402** (FIG. **14**), and stack **1801** (FIG. **18**).

[0084] In one implementation, the warpage state of the stack of dies **102** direct bonded at the higher temperature and then cooler to the lower temperature is memorialized and “fixed” by adding a lateral support **1502** of underfill or other solid material to stabilize the stack. In another implementation, the package is stabilized and/or completed with molding material **1706** on sides as needed.

[0085] FIG. **18** shows example structures and associated processes for making an example module **1800** of stacked dies that has reduced interior stress warpage and/or a higher manufacturing yield due to less failure from warpage during fabrication. A first stack of dies **1801** is assembled by direct bonding thin dies **102** to each other, or by other bonding means. Underfill or other solid material is used to make lateral supports **1502** for the stack of dies **102**, thereby stabilizing the stack of dies **102** in a non-warped state.

[0086] Another stack **1810** of dies **1802** & **1804** & **1806** & **1808** are made separately, applying one or more of the anti-warping measures as described herein. This pre-made stack **1810** of additional dies is then bonded or direct bonded to the initial stack of dies **102**, rather than just continuing the initial single stack **102** by adding the individual additional dies **1802** & **1804** & **1806** & **1808** one-by-one, which would propagate and further exaggerate the negative warpage of the initial stack of dies **102**.

[0087] In an implementation, a layer **1812** topping the initial stack of dies **102**, which would be an extra dummy die in conventional modules to fill out the package, is made of active dies **1802** & **1804** in this implementation of the microelectronic device or module **1800** being assembled, these dies **1802** & **1804** are not dummy dies. The module **1800**, now containing two stacks of dies **102** & **1810** direct bonded together, can be filled out and completed with a molding material **1814**.

[0088] It should be noted that in one implementation, the lateral supports **1502** made of underfill material, for example, represent a first encapsulation that touches, supports and stabilizes only the dies **102** of the first stack of dies **102**, while the molding material **1814** added later represents a second encapsulation that touches, supports, and stabilizes only the dies of the second stack **1810**. Thus all dies in the two stacks **102** and **1810** get stabilized in a non-warped configuration by encapsulants, but in a different manner for each of the stacks as the module **1800** is assembled. The first stack of dies **102** receives lateral supports **1502** from a buttressing underfill material, while the next stack of dies **1810** receives non-warp stabilization from side molding **1814** that completes the package.

[0089] FIG. **19** shows another example structure **1900** and method for alleviating warpage stresses in stacks of dies and microchips, especially when the dies are very thin. An example module **1900** with a stack **1902** of dies **102** is built on a substrate **104**, such as a semiconductor wafer, carrier, panel, or interposer, etc.

[0090] In an implementation, a top die **1904** is added to the stack of dies **102** to bring the package to a height specification. The top die **1904** may be a dummy die, but can also be one or more active dies. In an implementation, the top die **1904** is thicker than the individual dies **102** making up the stack **1902** beneath it, and so is subject to warping in its own right. The bonding surface of the top die **1904** may be formed by photolithographic and selective material methods. In one example, the bonding surface of die **1904** may be selectively protected with an organic or inorganic resist protective layer for example. The unprotected portion of the bond surface may be etched by a dry or a wet method to remove sufficient materials to prevent the etched regions from contacting the top bonding surface of the die **102** immediately beneath during and after the bonding operation.

[0091] After the material removal step on die **1904**, the protective layer is stripped, the bottom bonding surface of the top dies is cleaned, prepared and bonded to the top surface of die **102**. The top die **1904** may be imparted with rounded edges on its bonding side proactively. The top die **1904** is direct bonded to the stack of dies beneath it at its middle region forming a peripheral gap beyond the bonded region. In this configuration, the prepared bonding surface of the top die **1904** is smaller than the bonding surface of die **102** beneath. Reducing the bonded area between top die **1904** and the die beneath, for example die “4” **102‴**, reduces the force transmitted to the bonded dies beneath. In one embodiment, an encapsulant wedge or fillet **1906** may be applied to fill the peripheral gap beyond the bonded region of die **1904**. The encapsulant fillet **1906** may comprise or incorporate a particulate material to reduce the thermal expansion of the encapsulant material. In other embodiments, underfill material or a molding material **1908** may be applied to encapsulate the bonded dies, such as dies **102** and die **1904**, and to fill the fillet **1906** between the top die **1904** and the die **102‴** beneath.

[0092] The encapsulating material **1908** firmly couples the bonded dies stack **102** and the top die **1904** to form an integrated solid structure and also acts as a protective layer thereby preventing stress cracking and delamination between the stack of dies **102** and the top die **1904**. The fillet **1906** of compliant material may also be the same material as the molding **1908** around the sides of the stack **102** & **1904**, which completes the package **1900**.

[0093] FIG. **20** shows another example scheme for constructing larger modules **2000** that have numerous stacked dies, without introducing problems caused by stress warpage, which decrease yield during fabrication. In this embodiment, a compliant layer **2001** is added at intervals, between groups of dies, such as between a first group of dies **102**, a second group **2010** of dies **2002** & **2004** & **2006** & **2008**, and a third group **2012** of active or dummy dies. In one embodiment, the compliant layer **2001** comprises one or more conductive vias for electrically connecting conductive features on the backside of die “4” **102‴** to the conductive features of die “5” **2002**. In some applications, the layer **2001** may comprise one or more low melting point conductive materials (for example solder) for connecting desirable portions of die “4” **102‴** to similar portions in die “5” **2002**.

[0094] In an implementation the dies **102** and compliant layers **2001** are stacked up individually, one die **102** or layer **2001** at a time, by direct bonding or direct hybrid bonding, for example. In another implementation, the groups of dies **102** & **2010** & **2012** are constructed separately, and groups of dies are added to the overall stack as grouped units.

[0095] When the overall stack of dies **102** & **2010** & **2012** is completed, the stack may be encapsulated with molding **2014** or the same compliant material as used in the compliant layers **2001**.

[0096] FIG. **21** shows thin dies **2102** direct hybrid-bonded together into stacks **2104**. Each stack **2104** is built on a common wafer substrate **2106**, for example, or carrier, panel, etc. Thin layers of dielectric and metal **2108** (direct hybrid bonding layers **2108**) on the dies **2102** and substrate **2106** enable the direct hybrid bonding. That is, the bonding layer **2108** may consist of multiple layers, and/or may consist of a combination of dielectric material(s) and metal(s). The dielectric may consist of multilayer dielectrics including but not limited to diffusion barrier layers and dielectric layers for bonding which consist of Si, O, N, and C. Additionally, layer **2108** may also contain metal materials as conductive pads, wherein the direct bonding occurs at the dielectric surfaces followed by direct bonding between metal bonding pads, vias, and interconnects of the dies **2102** in an annealing step of the same overall direct bonding operation. One or more extra dummy dies on top of each stack **2104** may be direct bonded to each respective stack **2104** with oxide-oxide direct bonding.

[0097] A singulation operation **2110** dices individual stacks **2104** into individual module units **2112**, such as individual high bandwidth memory modules.

[0098] FIG. **22** shows thin dies **2202** direct hybrid bonded together into stacks **2204** and encapsulated with a molding material **2205**. Each stack **2204** is built on a common wafer substrate **2206**, carrier, panel, etc. Direct hybrid bonding layer **2208** consists of extremely thin layers of dielectric **2208** on the dies **2202** and substrate **2206** to enable the direct hybrid bonding. Thin layers **2208** of dielectric and metal (direct hybrid bonding layer **2108**) on the dies **2202** and substrate **2206** enable the direct hybrid bonding. The bonding layer **2208** may consist of multiple layers, and/or may consist of a combination of dielectric material(s) and metal(s). The dielectric may consist of multilayer dielectrics including but not limited to diffusion barrier layers and dielectric layers for bonding which consist of Si, O, N, and C. Additionally, layer **2208** may also contain metal materials as conductive pads, wherein the direct bonding occurs at the dielectric surfaces followed by direct bonding between metal bonding pads, vias, and interconnects of the dies **2202** in an annealing step of the same overall direct bonding operation. One or more extra dummy dies on top of each stack **2204** may be direct bonded to each respective stack **2204** with oxide-oxide direct bonding, for example.

[0099] A singulation operation **2210** dices individual stacks **2204** into individual module units **2212** that are pre-encapsulated **2205**.

[0100] FIG. **23** shows an example module **2300** with one or more direct bonded die stacks **2302** on a substrate **2304** or board, and a microprocessor **2306** and/or graphics processor, or microcontroller, mounted on the same substrate **2304** or board. Each of the one or more direct bonded die stacks **2302** incorporates one of the described stress or warpage-relief measures or stress-warpage prevention devices of FIGS. **2-22**. The microprocessor **2306** or other logic unit or processor is communicatively coupled with the one or more direct bonded die stacks **2302**. Thin layers **2303** of dielectric and metal (direct hybrid bonding layer **2303**) on the dies **2305** and substrate **2304** enable the direct hybrid bonding. The bonding layer **2303** may consist of multiple layers, and/or may consist of a combination of dielectric material(s) and metal(s). The dielectric may consist of multilayer dielectrics including but not limited to diffusion barrier layers and dielectric layers for bonding which consist of Si, O, N, and C. Additionally, layer **2303** may also contain metal materials as conductive pads, wherein the direct bonding occurs at the dielectric surfaces followed by direct bonding between metal bonding pads, vias, and interconnects of the dies **2305** in an annealing step of the same overall direct bonding operation.

[0101] In an implementation, the module **2300** includes at least one heat sink **2308**, and in an implementation, the one or more die stacks **2302** and the microprocessor **2306** are in contact with a common heat sink **2308**.

[0102] In the foregoing description and in the accompanying drawings, specific terminology and drawing symbols have been set forth to provide a thorough understanding of the disclosed embodiments. In some instances, the terminology and symbols may imply specific details that are not required to practice those embodiments. For example, any of the specific dimensions, quantities, material types, fabrication steps and the like can be different from those described above in alternative embodiments. The term “coupled” is used herein to express a direct connection as well as a connection through one or more intervening circuits or structures. The terms “example,” “embodiment,” and “implementation” are used to express an example, not a preference or

requirement. Also, the terms “may” and “can” are used interchangeably to denote optional (permissible) subject matter. The absence of either term should not be construed as meaning that a given feature or technique is required.
[0103] Various modifications and changes can be made to the embodiments presented herein without departing from the broader spirit and scope of the disclosure. For example, features or aspects of any of the embodiments can be applied in combination with any other of the embodiments or in place of counterpart features or aspects thereof. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense.
[0104] While the present disclosure has been disclosed with respect to a limited number of embodiments, those skilled in the art, having the benefit of this disclosure, will appreciate numerous modifications and variations possible given the description. It is intended that the appended claims cover such modifications and variations as fall within the true spirit and scope of the disclosure.

## Claims

**1**. (canceled)
**2**. A singulated die comprising: a hybrid bonding surface; an upper surface opposite the hybrid bonding surface; a first side die surface extending from the hybrid bonding surface to the upper surface; a second side die surface extending from the hybrid bonding surface to the upper surface, the second side die surface transverse to the first side die surface; and a corner region between the first and second side die surfaces, wherein the corner region provides a transition between the first and second side dies that is non-perpendicular.
**3**. The singulated die of claim 2, wherein the non-perpendicular transition is chamfered.
**4**. The singulated die of claim 2, wherein the non-perpendicular transition is rounded.
**5**. The singulated die of claim 2, wherein the non-perpendicular transition is angled relative to the first and second side die surfaces.
**6**. The singulated die of claim 2, wherein the non-perpendicular transition reduces stress concentration as compared to a perpendicular transition.
**7**. The singulated die of claim 2, wherein multiple corner regions of the singulated die include transitions between adjacent transverse side die surfaces that are non-perpendicular.
**8**. A bonded structure comprising: the singulated die of claim 2; and a substrate directly bonded to the hybrid bonding surface of the singulated die.
**9**. The bonded structure of claim 8, wherein the non-perpendicular transition of the singulated die is chamfered.
**10**. The bonded structure of claim 8, wherein the non-perpendicular transition of the singulated die is rounded.
**11**. The bonded structure of claim 8, wherein the non-perpendicular transition of the singulated die is angled relative to the first and second die edges.
**12**. The bonded structure of claim 8, wherein the non-perpendicular transition of the singulated die reduces stress concentration as compared to a perpendicular transition.
**13**. The bonded structure of claim 8, wherein the singulated die is hybrid bonded to the substrate.
**14**. The bonded structure of claim 8, wherein the substrate comprises a second die.
**15**. The singulated die of claim 8, wherein the first and second side die surfaces are covered by an encapsulant.
**16**. The bonded structure of claim 14, wherein the second die comprises a third side die surface, a fourth side die surface transverse to the third side die surface, and a second corner region having a transition between the third and fourth side die surfaces that is non-perpendicular.
**17**. A bonded structure comprising: a substrate; and a singulated die disposed above the substrate along a vertical direction, the singulated die having a bonding surface transverse to the vertical

direction and an upper surface opposite the bonding surface, the bonding surface hybrid bonded to the substrate without an intervening adhesive, wherein the singulated die comprises a first side die surface extending from the bonding surface to the upper surface, a second side die surface extending from the bonding surface to the upper surface and transverse to the first side die surface, and a corner region between the first and second side die surfaces, and wherein the corner region is chamfered.

**18**. The bonded structure of claim 17, wherein multiple corner regions of the singulated die include chamfered transitions between adjacent transverse side die surfaces.

**19**. The bonded structure of claim 17, wherein the substrate comprises a second die.

**20**. The singulated die of claim 19, wherein the first and second side die surfaces are covered by an encapsulant.

**21**. The bonded structure of claim 19, wherein the second die comprises a third side die surface, a fourth side die surface transverse to the third side die surface, and a second corner region having a transition between the third and fourth side die surfaces that is chamfered.