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Semiconductor device and electronic device

Abstract

A neuron circuit can switch between two functions: as an input neuron circuit, and as a hidden neuron circuit. An error circuit can switch between two functions: as a hidden error circuit, and as an output neuron circuit. A switching circuit is configured to be capable of changing the connections between the neuron circuit, a synapse circuit, and the error circuit. The synapse circuit includes an analog memory that stores data that corresponds to the connection strength between the input neuron circuit and the hidden neuron circuit or between the hidden neuron circuit and the output neuron circuit, a writing circuit that changes the data in the analog memory, and a weighting circuit that weights an input signal in reaction to the data of the analog memory and outputs the weighted output signal. The analog memory includes a transistor comprising an oxide semiconductor with extremely low off-state current.

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Background/Summary

TECHNICAL FIELD

(1) One embodiment of the present invention relates to an electronic device which includes a semiconductor device or the semiconductor device.

(2) Note that one embodiment of the present invention is not limited to the above technical field. The technical field of the invention disclosed in this specification and the like relates to an object, a method, or a manufacturing method. Furthermore, one embodiment of the present invention relates to a process, a machine, manufacture, or a composition of matter. Specifically, examples of the technical field of one embodiment of the present invention disclosed in this specification include a semiconductor device, a display device, a light-emitting device, a power storage device, a memory device, a method for driving any of them, and a method for manufacturing any of them.

(3) In this specification and the like, a semiconductor device refers to an element, a circuit, a device, or the like that can function by utilizing semiconductor characteristics. An example of the semiconductor device is a semiconductor element such as a transistor or a diode. Another example of the semiconductor device is a circuit including the semiconductor element. Another example of the semiconductor device is a device provided with a circuit including a semiconductor element.

BACKGROUND ART

(4) A neural network, which is a model simulating a network of neural circuits and implemented by computers or the like, is expected to enable a fabrication of computers with higher performance than von Neumann type computers. The research and development in this field is active, example of which can be seen in Non-Patent Document 1.

(5) In the neural network, units which simulate neurons are connected to each other through units which simulate synapses. The neural network can change the connection strengths by learning, which enables high-speed pattern recognition and associative memory for various input patterns.

(6) In an effective pattern recognition method, a unit simulating a neural network with a hierarchical perceptron architecture learns patterns of a target moving object as instructor data, then is given image data as an input data to determine the degree of matching between the instructor data and the input data, thereby extracting whether the moving object is included in the image or not. The neural network with the hierarchical perceptron architecture is configured with a neuron circuit, which is a unit simulating neurons, and a synapse circuit, which is a unit simulating a synapse.

(7) The synapse circuit needs to have the functions of storing the connection strength between the neuron circuits, of multiplying the connection strength to an output of the neuron circuit, and of adding the results of each multiplication. The synapse circuit thus needs a memory to store the connection strength, a multiplier circuit for implementing a function of multiplication, and an adder circuit for implementing a function of addition.

(8) As a screen of a television (TV) becomes larger, a demand for the option to watch high-definition images has been created. For this reason, ultra-high definition TV (UHDTV) broadcast has been increasingly put into practical use. Japan, which has promoted UHDTV broadcast, started 4K broadcast services utilizing a communication satellite (CS) and an optical line in 2015. The test broadcast of UHDTV (4K and 8K) by a broadcast satellite (BS) will start in the future. Therefore, various electronic devices which are compatible with 8K broadcast have been developed (see Non-Patent Document 2). In practical 8K broadcasts, 4K broadcasts and 2K broadcasts (full-high vision broadcast) will be also employed.

(9) In addition, imaging elements are provided in a wide variety of electronic devices such as digital cameras or mobile phones. As described above, UHDTV broadcast has been increasingly put into practical use; in recent years, the number of pixels in imaging elements has been increased accordingly. As the number of pixels in imaging elements increases, the amount of data obtained by imaging inevitably increases. Thus, faster data reading and transfer are demanded. A compression of the image data is a known technique to react to the image data size increase caused by the increase in the number of pixels in the imaging element. Patent Document 1 discloses an imaging element module that compresses data by calculating differential data between a current imaging data and a past imaging data, during video recording or continuous shooting.

REFERENCE

Patent Document

(10) [Patent Document 1] Japanese Published Patent Application No. 2009-296353

Non-Patent Document

(11) [Non-Patent Document 1] Yutaka Arima et al., "A Self-Learning Neural Network Chip with 125 Neurons and 10K Self-Organization Synapses," *IEEE Journal of Solid-State Circuits*, Vol. 26, No. 4, April 1991, pp. 607-611 [Non-Patent Document 2] S. Kawashima et al., "13.3-In. 8K×4K 664-ppi OLED Display Using CAAC-OS FETs," *SID* 2014 *DIGEST*, pp. 627-630

DISCLOSURE OF INVENTION

(12) However, in the case where the memory, the multiplier circuit, and the adder circuit are configured with digital circuits, the memory to store multiple bits and the adder and multiplier circuits capable of processing multiple bits are needed. This makes the circuit configuration large and

reliant upon minute patterning.

(13) Furthermore, in the case where the memory, the multiplier circuit, and the adder circuit are configured with analog circuits, the number of circuit elements can be reduced. However, configuring an analog memory that is ideal for the above memory, that is, an analog memory capable of storing analog values, is highly difficult. In the case where the analog memory cell with a dynamic random access memory (DRAM) type cell structure is used, the data retention time is extremely short. As measures against this issue, configurations such as where a large capacitor for memory storage is implemented in the analog memory, or where an analog data is recovered by periodic refresh operations, have been proposed. The configurations, however, increases in a chip area, and power consumption.

(14) In addition, a configuration in which the hierarchical structure (e.g., the number of neural layers and the number of neurons in a given layer) can be freely changed according to the data input is preferred.

(15) In light of the above, an object of one embodiment of the present invention is to provide a novel semiconductor device or the like that has a configuration which is different from that of existing semiconductor devices or the like.

(16) Alternatively, an object of one embodiment of the present invention is to provide a semiconductor device or the like with a novel configuration and a reduced chip area. Another object of one embodiment of the present invention is to provide a semiconductor device or the like with a novel configuration, in which power consumption is reduced. Another object of one embodiment of the present invention is to provide a semiconductor device or the like with a novel configuration, in which the hierarchical structure constituting of circuits such as the neuron circuit or the synapse circuit can be freely changed.

(17) Note that the objects of one embodiment of the present invention are not limited to the above objects. The objects described above do not disturb the existence of other objects. The other objects are the ones that are not described above and will be described below. The other objects will be apparent from and can be derived from the description of the specification, the drawings, and the like by those skilled in the art. One embodiment of the present invention is to solve at least one of the aforementioned objects and the other objects.

(18) One embodiment of the present invention is a semiconductor device that includes a first circuit, a second circuit, and a third circuit. The first circuit includes a first function of amplifying a first signal and output the first signal to the second circuit, and a second function of converting the first signal from current to voltage and output the first signal converted from current to voltage to the third circuit. The second circuit includes a first multiplier circuit that changes data corresponding to a connection strength, an analog memory that stores the data, and a second multiplier circuit that outputs a second signal that is obtained by weighting of the first signal. The third circuit includes a first function of converting the second signal from current to voltage and output the second signal converted from current to voltage to the outside, and a second function of generating a fourth signal from a difference between the first signal converted from current into voltage and a third signal that is input from the outside. The analog memory includes a transistor that includes an oxide semiconductor in a channel formation region.

(19) In one embodiment of the present invention, the first multiplier circuit of the semiconductor device preferably includes a function of changing the data in reaction to the first signal converted from current into voltage and the fourth signal.

(20) One embodiment of the present invention is an electronic device including an encoder for encoding video data, which utilizes the above semiconductor device. The video data includes first video data and second video data. The semiconductor device compares the first video data and the second video data when the first video data and the second video data are input to the semiconductor device, and obtains a motion vector from the first video data to the second video data when the first video data and the second video data match.

(21) Note that other embodiments of the present invention will be described in the following embodiments with reference to the drawings.

(22) One embodiment of the present invention can provide a novel semiconductor device, a novel display device, a novel electronic device, or the like.

(23) One embodiment of the present invention can provide a semiconductor device or the like with a novel configuration and a reduced chip area. Another embodiment of the present invention can provide a semiconductor device or the like with a novel configuration, in which power consumption is reduced. Another embodiment of the present invention can provide a semiconductor device or the like with a novel configuration, in which the hierarchical structure constituting of circuits such as the neuron circuit or the synapse circuit can be freely changed.

(24) Note that the effects of one embodiment of the present invention are not limited to the above effects. The effects described above do not disturb the existence of other effects. The other effects are the ones that are not described above and will be described below. The other effects will be apparent from and can be derived from the description of the specification, the drawings, and the like by those skilled in the art. One embodiment of the present invention is to have at least one of the aforementioned effects and the other effects. Accordingly, one embodiment of the present invention does not have the aforementioned effects in some cases.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

(1) In the accompanying drawings:

(2) FIG. **1** illustrates an example of a block diagram;

(3) FIGS. **2**A, **2**B, **2**C, and **2**D each illustrate an example of a circuit diagram;

(4) FIG. **3** illustrates an example of a block diagram;

(5) FIG. **4** illustrate an example of a block diagram;

(6) FIG. **5** illustrates an example of a circuit diagram;

(7) FIG. **6** illustrates an example of a circuit diagram;

(8) FIG. **7** illustrates an example of a circuit diagram;

(9) FIG. **8** illustrates an example of a circuit diagram;

(10) FIG. **9** illustrates an example of a circuit diagram;

(11) FIG. **10** illustrates an example of a flow chart;

(12) FIG. **11** illustrates an example of a flow chart;

(13) FIGS. **12**A to **12**F each illustrate an operation example;

(14) FIG. **13** illustrates an example of a flow chart;

(15) FIG. **14** illustrates an example of a block diagram;

(16) FIG. **15** illustrates an example of a schematic diagram;

(17) FIG. **16** illustrates an example of a video distribution system;

(18) FIGS. **17**A to **17**D each illustrate an example of a receiver device;

(19) FIG. **18** illustrates an example of a block diagram;

(20) FIG. **19**A illustrates an example of a top view, and FIGS. **19**B and **19**C each illustrate an example of a cross-sectional diagram;

(21) FIG. **20**A illustrates an example of a cross-sectional diagram, and FIG. **20**B illustrates an example of an energy band diagram;

(22) FIGS. **21**A and **21**B are cross-sectional diagrams illustrating oxygen diffusion paths;

(23) FIG. **22**A illustrates an example of a top view, and FIGS. **22**B and **22**C each illustrate an example of a cross-sectional diagram;

(24) FIG. **23**A illustrates an example of a top view, and FIGS. **23**B and **23**C each illustrate an example of a cross-sectional diagram;

(25) FIG. **24**A illustrates an example of a top view, and FIGS. **24**B and **24**C each illustrate an example of a cross-sectional diagram;

(26) FIG. **25**A illustrates an example of a top view, and FIGS. **25**B and **25**C each illustrate an example of a cross-sectional diagram;

(27) FIG. **26**A illustrates an example of a top view, and FIGS. **26**B, **26**C and **26**D each illustrate an example of a cross-sectional diagram;

(28) FIG. **27**A illustrates an example of a top view, and FIG. **27**B illustrates an example of a cross-sectional diagram;

(29) FIGS. **28**A to **28**E show structural analysis of a CAAC-OS and a single crystal oxide semiconductor by XRD and selected-area electron diffraction patterns of a CAAC-OS;

(30) FIGS. **29**A to **29**E show a cross-sectional TEM image and plan-view TEM images of a CAAC-OS and images obtained through analysis thereof;

(31) FIGS. **30**A to **30**D show electron diffraction patterns and a cross-sectional TEM image of an nc-OS;

(32) FIGS. **31**A and **31**B show cross-sectional TEM images of an a-like OS;

(33) FIG. **32** shows a change of crystal parts of an In—Ga—Zn oxide owing to electron irradiation; and

(34) FIG. **33** illustrates an example of a block diagram.

BEST MODE FOR CARRYING OUT THE INVENTION

(35) Hereinafter, embodiments will be described with reference to drawings. However, the embodiments can be implemented with various modes. It will be readily appreciated by those skilled in the art that modes and details can be changed in various ways without departing from the spirit and scope of the present invention. Thus, the present invention should not be interpreted as being limited to the following description of the embodiments.

(36) In this specification and the like, ordinal numbers such as "first", "second", and "third" are used in order to avoid confusion among components. Thus, the terms do not limit the number or order of components. In the present specification and the like, a "first" component in one embodiment can be referred to as a "second" component in other embodiments or claims. Furthermore, in the present specification and the like, a "first" component in one embodiment can be omitted in other embodiments or claims.

(37) The same elements or elements having similar functions, elements formed using the same material, elements formed at the same time, or the like in the drawings are denoted by the same reference numerals in some cases, and the description thereof is not repeated in some cases.

EMBODIMENT 1

(38) The embodiment of the present invention is explained with reference to FIG. **1**, FIGS. **2**A to **2**D, FIG. **3**, FIG. **4**, FIG. **5**, FIG. **6**, FIG. **7**, FIG. **8**, and FIG. **9**.

(39) <Module Configuration>

(40) FIG. **1** shows circuit blocks of module **100** that make up the semiconductor device. Module **100** is made up of n (n is a natural number) neuron circuits NU, m×n (m is a natural number) synapse circuits SU, and m error circuits EU.

(41) Each of the circuit blocks that make up the module **100** illustrated in FIG. **1** is explained below.

(42) FIG. **2**A illustrates a configuration of the neuron circuit NU. The neuron circuit NU can function as an input neuron circuit or as a hidden neuron circuit. The neuron circuit NU includes an amplifier **101**, a selector circuit **102**, a differential amplifier **103**, a switch **104** and a resistor **105**.

(43) When the neuron circuit NU is to function as the input neuron circuit, the signal to be output is changed to the side of "1" by a switching signal (IN? in FIGS. **2**A to **2**D) of the selector circuit **102**. The neuron circuit NU that functions as the input neuron circuit is a circuit which receives an input signal i from the outside of the semiconductor device, and generates an output signal x to the synapse circuit SU within the same module through the selector circuit **102** and the amplifier **101**.

(44) The selector circuit **102** preferably inputs and outputs analog signals. The selector circuit **102** can be configured with a pass transistor and an analog switch, for example.

(45) A unity gain buffer **106**, which is illustrated in FIG. **2**B, may be used as the amplifier **101**, which is illustrated in FIG. **2**A. The amplifier **101** may have a function of changing the standard signal level of the output signal x using an amplifier circuit **107**, as illustrated in FIG. **2**C. In addition, as illustrated in FIG. **2**D, the amplifier **101** may have a function of generating a pair of differential signals (x and xb) as output signals by using a buffer **108**, which generates differential signals. Furthermore, when the input signal i has an adequate driving power, the amplifier **101** is not necessarily implemented.

(46) On the other hand, when the neuron circuit NU is to function as the hidden neuron circuit, the signal to be output is changed to the side of "0" by a switching signal (IN? in FIGS. **2**A to **2**D) of the selector circuit **102**. The neuron circuit NU that functions as the hidden neuron circuit receives the input signal i that is output from the synapse circuit SU of the module in the previous stage, from which the neuron circuit NU generates the output signal x output to the synapse circuit SU in a different module, through the differential amplifier **103**, the selector circuit **102**, and the amplifier **101**.

(47) When the input signal i is the output signal of the synapse circuit SU, the input signal i corresponds to the sum (expressed as $\Sigma w[i, j]x[j]$) of the current of each of the synapse circuits SU. The sum of the current is converted into voltage with the resistor **105**, and the differential voltage between this voltage and a threshold voltage θ_N is generated with the differential amplifier **103**.

(48) The signal (Ri? in FIGS. **2**A to **2**D) that controls the on/off state of the switch **104** may be set so that the signal Ri? turns on the switch **104** when the neuron circuit NU is to function as a hidden neuron circuit, and that the switch **104** is turned off in other periods.

(49) The differential amplifier **103** is configured so that its output signal is equal to $f_H(X)$ in Formula (1) or can be approximated to $f_H(X)$ in Formula (1), when the input signal X is given as a variable.

[Formula(1)]

(50) $$f_H(x) = \frac{1}{(1 + e^{-\alpha_H(X - \theta_N)})} \quad (1)$$

(51) α_H in Formula (1) is a given constant, and corresponds to the rate of change of the output signal, when $X=\theta_N$ is given. When the sum of the current of each of the synapse circuits, which is $\Sigma w[i,j]x[j]$, becomes higher than the threshold voltage ON, the output signal $f_H(X)=1$; that is, the output signal reaches H level (expressed as "H" or "high level"). This is described as the "firing" of the neuron circuit NU. In other words, the threshold voltage θ_N corresponds to a threshold at which the neuron circuit NU fires.

(52) Furthermore, when not all of the n neuron circuits NU are needed in the module, the potential of the input signal i of the unnecessary neuron circuit NU can be set at "0." In this case, the potential of the output signal x of the neuron circuit NU becomes "0," and the succeeding synapse circuit SU effectively does not function.

(53) FIG. **3** illustrates a configuration of the synapse circuit SU. The synapse circuit SU is made up of an analog memory AM, and multiplier circuits MUL**1** to MUL**3**.

(54) The analog memory AM has a function of storing data that corresponds to a connection strength (weight coefficient) w between the neuron circuit NU in the same module and the neuron circuit NU in the module in the succeeding stage. The analog memory AM also has a function of outputting a voltage that corresponds to the stored data.

(55) The multiplier circuit MUL**1** multiplies the output signal x from the C neuron circuit NU of the same module by the weight coefficient w of the analog memory AM, thereby generating an output signal wx. A current that corresponds to the multiplication result is supplied as the output signal wx. That is, the multiplier circuit MUL**1** outputs an output signal wx, which is obtained by weighting the output signal x from the neuron circuit NU in the same module according to the data in the analog memory AM, to the neuron circuit NU in the module of the succeeding stage, and to the error circuit EU in the same module.

(56) The multiplier circuit MUL**2** multiplies the output signal x from the neuron circuit NU of the same module by an output signal d from the error circuit EU in the same module, thereby generating an output signal dw. A current that corresponds to the multiplication result is supplied as the output signal dw. The output signal dw is supplied as a current that corresponds to the amount of the change of the weight coefficient w, which is

stored in the analog memory AM. In other words, the multiplier circuit MUL**2** updates the data in the analog memory AM according to the error signal d, which is output from the error circuit EU in the same module.

(57) The multiplier circuit MUL**3** multiplies the output signal d from the error circuit EU of the same module by the weight coefficient w of the analog memory AM, thereby generating an output signal wd. A current that corresponds to the multiplication result is supplied as the output signal wd. That is, the multiplier circuit MUL**3** outputs an error signal wd, which is obtained by weighting the error signal d from the error circuit EU of the same module according to the data in the analog memory AM, to the error circuit EU in the module of the previous stage.

(58) FIG. **4** illustrates a configuration of the error circuit EU. The error circuit EU can function as the output neuron circuit or as a hidden error circuit. The error circuit EU includes a differential amplifier **111**, a switch **112**, a resistor **113**, a differentiator circuit DV, a multiplier circuit MUL**4**, a selector circuit **114**, a differential amplifier **115**, a switch **116** and a resistor **117**.

(59) When the error circuit EU is to function as the output neuron circuit, the signal to be output is changed to the side of "1" by a switching signal (ON? in FIG. **4**) of the selector circuit **114**. The error circuit EU that functions as the output neuron circuit generates the signal o, which is output to the outside of the semiconductor device, from a signal Σwx, which correspond to a sum of current from the output signals wx that are output from the synapse circuits SU in the same stage with the differential amplifier **111**. When the error circuit EU functions as an output neuron circuit, the difference signal (e−o) between the instructor signal e that is supplied from the outside of the semiconductor device and the signal o is generated with a differential amplifier **115**. In addition, when the error circuit EU functions as the output neuron circuit, the differentiator circuit DV generates a derivative f′ of the signal o. Furthermore, the multiplier circuit MUL**4** generates an error signal d by multiplying the difference signal (e−o) by the derivative f′. The error signal d is output to the synapse circuit SU of the same module. Note that when the instructor signal e is given as a voltage, a signal that controls the on/off state of the switch **116** (Re? in FIG. **4**) is set to turn off the switch **116**.

(60) In addition, the differential amplifier **111** converts the output signal Σwx, which corresponds to the sum of current output from the synapse circuits SU in the same stage, to voltage with the resistor **113**, then generates a difference voltage between the voltage output by the differential amplifier **111** and the threshold voltage θ.sub.O.

(61) The differential amplifier **111** is configured so that the signal o is equal to f.sub.O(X) in Formula (2) or can be approximated to f.sub.O(X) in Formula (2), when the input signal X is given as a variable.

[Formula(2)]

(62)
$$f_O(x) = \frac{1}{(1+e^{-\alpha_O(X-\theta_O)})} \quad (2)$$

(63) In Formula (2), α.sub.O is a given constant, and corresponds to the rate of change when X=θ.sub.O is valid. When the potential of output signal Σwx becomes greater than the threshold voltage θ.sub.O, the equation f.sub.O(X)=1 is valid; that is, the potential of the output signal becomes H level. This is described as the "firing" of the output neuron circuit EU. In other words, the threshold voltage θ.sub.O corresponds to a threshold at which the neuron circuit EU fires.

(64) On the other hand, when the error circuit EU is to function as the hidden error circuit, the signal to be output is changed to the side of "0" by the switching signal (ON? in FIG. **4**) of the selector circuit **114**. The error circuit EU that functions as the hidden error circuit generates the signal o in a similar manner as when the error circuit EU functions as an output neuron circuit; specifically, the error circuit EU generates the signal o from the signal Σwx, which corresponds to the sum of current from the output signals wx that are output from the synapse circuits SU in the same stage, with the differential amplifier **111**. Furthermore, when the error circuit EU functions as a hidden error circuit, the sum of current from the error signals wd that are output from the synapse circuits SU of the modules in the succeeding stages is supplied as the instructor signal e; the error circuit EU then generates a difference signal with the differential amplifier **115**.

(65) The instructor signal e in this case is a signal Σw[i,j]d[i], which corresponds to the sum of current w[i,j]d[i]. This signal is converted to voltage with the resistor **117**, and the difference signal is generated as the difference voltage between the instructor signal e converted into voltage and the reference voltage θ.sub.E. In addition, the differentiator circuit DV generates the derivative f′ of the signal o. Furthermore, the multiplier circuit MUL**4** generates the error signal d by multiplying the difference signal by the derivative f′. The error signal d is output to the synapse circuit SU of the same module.

(66) When one stage is configured with a plurality of modules, the signal Σwx from the synapse circuits SU in the previous stage serves as an input signal of the neuron circuits NU that function as a plurality of hidden neuron circuits in a plurality of modules, and as an input signal of the error circuits EU that function as a plurality of error circuits in the plurality of modules in the previous stage. In this case, any one of the plurality of hidden neuron circuits may convert the input signal i to a voltage with the resistor **105**, or any one of the plurality of error circuits may convert the input signal Σwx to a voltage with the resistor **113**. A signal (RΣwx? in FIG. **4**) that controls the on/off state of the switch **112** may be set so that the signal RΣwx? turns on the switch **112** when the error circuit EU is to function as a hidden error circuit, and that the switch **112** is turned off in other periods.

(67) When one stage is configured with a plurality of modules, the error signal wd from the synapse circuits SU in the module of the succeeding stage serves as the instructor signal e of the error circuits EU that function as a plurality of hidden error circuits in the plurality of modules. In this case, the instructor signal e may be converted into voltage with a resistor **117** in any one of the plurality of error circuits EU. In other words, the signal (Re? in FIG. **4**) that controls the on/off state of the switch **116** may be set so that the signal Re? turns on the switch **116** when the error circuit EU is to function as a hidden error circuit, and that the switch **116** is turned off in other periods.

(68) <Configuration of Each Constituting Circuit of the Module>

(69) FIG. **5** illustrates a configuration of the multiplier circuit MULapplicable to the multiplier circuits MUL**1** to MUL**4** in the synapse circuit SU and the error circuit EU. The multiplier circuit MUL is made up of a first transistor Tr**01** to a fourteenth transistor Tr**14**, and capacitors C**0** and C**1**. This multiplier circuit adopts a configuration which is based on a Chible multiplier circuit; a current that is proportional to the product of the input signals A and B is obtained as the output signal Y. In addition, when it is assumed that the capacitance of the capacitors C**0** and C**1** are adequately larger than gate capacitances of the eighth transistor Tr**08** and the eleventh transistor Tr**11**, the potential change of the input signal B is multiplied by C**1**/(C**0**+C**1**), then is input to the gates of the eighth transistor Tr**08** and the eleventh transistor Tr**11**. Thus, the input range of the input signal B can be made wide, which secures the linearity of the multiplier circuit MUL in a wide input range. Similarly, providing a capacitor to the input signal A secures the linearity of the multiplier circuit MUL in a wide input range.

(70) FIG. **6** illustrates a configuration of the differentiator circuit DV in the error circuit EU. The differentiator circuit DV is made up of operational amplifiers **121** and **122**, and the multiplier circuit MUL. Here, the operational amplifier **121** is configured so that when the difference between the non-inverted input signal A and the inverted input signal V.sub.ref is given as X=A−V.sub.ref, its output signal Y.sub.1 follows or approximates the following equation: Y.sub.1=f(X)=1/1+e.sup.−aX). In addition, the operational amplifier **122** is configured so that when the difference between the non-inverted input signal V.sub.ref and the inverted input signal A is given as X.sub.2=V.sub.ref−A=−X, its output signal Y.sub.2 follows or approximates the following equation: Y.sub.2=f(X.sub.2)=1/(1+e.sup.−aX2). Here, Y.sub.2 can be expressed as Y.sub.2=f(−X)=1/(1+e.sup.+aX)=e.sup.−aX/(e.sup.−aX+1)=1−1/(1+e.sup.−aX)=1−f(X). Therefore, the output of the multiplier circuit MUL can be expressed as Y=Y.sub.1×Y.sub.2=f(X)[1−f(X)]=f(X)(=df(X)/dX). That is, the differentiator circuit DV has a function of differentiating f(X).

(71) FIG. **7** illustrates the configuration of the analog memory AM in the synapse circuit SU. The analog memory AM is made up of a transistor Tr**15** and a capacitor C. Implementing a transistor with an extremely low off-state current using an oxide semiconductor as the transistor Tr**15** enables the fabrication of an ideal analog memory. Thus, implementation of large capacitors for memory retention or the recovery of analog data through periodic refresh operations are unnecessary. This enables the shrinking of chip area and the reduction of power consumption. Because the analog

memory AM is configured so that a current corresponding to the amount of change is supplied during the update of data, the amount of data change can be changed by adjusting the period in which the potential of the signal line WL is set at "H".

(72) <Three-Layer Neural Network>

(73) A three-layer neural network that uses two of the module **100** illustrated in FIG. **1**, that is, a neural network that includes an input stage, a hidden stage, and an output stage is described as a semiconductor device; in addition, learning in the neural network is described. A three-layer neural network that includes a first module **100_1** and a second module **100_2** is illustrated in FIG. **33**. In the first module **100_1**, the neuron circuit NU and the error circuit EU serve as the input neuron circuit and the hidden error circuit, respectively; in the second module **100_2**, the neuron circuit NU and the error circuit EU serve as the hidden neuron circuit and the output neuron circuit, respectively. The output signal of the synapse circuit SU of the first module **100_1** serves as the input signal of the neuron circuit NU of the second module **100_2**, and the error signal from the synapse circuit SU of the second module **100_2** serves as the input signal of the error circuit EU of the first module **100_1**.

(74) In the three-layer neural network, learning amounts to storing data corresponding to a weight coefficient w1[j,i] (j and i are natural numbers) of the synapse circuit SU of the first module **100_1** and a weight coefficient w2[k,j] (k is a natural number) of the synapse circuit SU of the second module **100_2** to each analog memory AM, in response to input signals I[1] to I[n], so that desired signals O[1] to O[n] can be obtained. Specifically, learning amounts to: providing a given value as an initial value to the weight coefficients w1[j,i] and w2[k,j]; providing input data used for learning to the input signals I[1] to I[n] of the input neuron circuits; providing an instructor signal as an expected value to the input signals E[1] to E[n] of the output neuron circuits; and converging the weight coefficients w1[j,i] and w2[k,j] so that a sum of squared errors of the signals O[1] to O[n] and the input signals E[1] to E[n] of the output neuron circuits is the smallest.

(75) The sum of squared errors between the signals O[1] to O[n] and the input signals E[1] to E[n] of the output neuron circuits can be expressed as in Formula (3).

[Formula(3)]

(76)
$$E = \tfrac{1}{2} \text{.Math. } (E[k] - O[k])^2 \quad (3)$$

When e2[k]=E[k]−O[k] is assumed, Formula (3) can be expressed as in Formula (4).

[Formula(4)]

(77)
$$E = \tfrac{1}{2} \text{.Math. } (e2[k])^2 \quad (4)$$

(78) Finding the minimum value of the sum of squared errors amounts to finding a local minimum of the weight coefficients w1[j,i] and w2[k,j], i.e., finding w1[j,i] and w2[k,j] that satisfy Formula (5) and Formula (6).

[Formula(5)]　　　　[Formula(6)]

(79)
$$\frac{\partial E}{\partial w1[j,i]} = 0 \quad (5) \qquad \frac{\partial E}{\partial w2[k,j]} = 0 \quad (6)$$

(80) In other words, finding the minimum value of the sum of squared errors amounts to updating the weight coefficients w1[j,i] and w2[k,j] in accordance with the values in the left sides of Formula (5) and Formula (6).

(81) The weight coefficient w2[k,j] follows the relationship expressed in Formula (7).

[Formula(7)]

(82)
$$\frac{\partial E}{\partial w2[k,j]} = \frac{\partial E}{\partial e2[k]} \text{.Math. } \frac{\partial e2[k]}{\partial O[k]} \text{.Math. } \frac{\partial O[k]}{\partial Y} \text{.Math. } \frac{\partial Y}{\partial w2[k,j]} = e2[k] \text{ .Math. } (-1) \text{ .Math. } f^{\,i}(Y) \text{ .Math. } {}_0 x2(j) \quad (7)$$

(83) Note that in Formula (7), Y is expressed as Y=a.sub.0(Σw2[k,j]x2[j]−θ.sub.0). Thus, the value of the weight coefficient w2[k,j] may be changed by an amount that corresponds to η.sub.w2×e2[k]×f(Y)×x2[j]. Note that η.sub.w2 is a constant.

(84) In addition, the weight coefficient w1[j,i] follows a relationship expressed in Formula (8)

(85)

[Formula(8)]

$$\frac{\partial E}{\partial w1[j,i]} = \frac{\text{.Math. } \partial E}{\partial e2[k]} \text{ .Math. } \frac{\partial e2[k]}{\partial O[k]} \text{ .Math. } \frac{\partial O[k]}{\partial Y} \text{ .Math. } \frac{\partial Y}{\partial x2[j]} \text{ .Math. } \frac{\partial x2[j]}{\partial X} \text{ .Math. } \frac{\partial X}{\partial w1[j,i]} = \text{ .Math. } e2[k] \text{ .Math. } (-1) \text{ .Math. } f^{\,i}(Y) \text{ .Math. } {}_0 w2[k,j[\text{ .Math. } f^{\,i}(X$$

(86) Note that in Formula (8), X and Y are expressed as X=a.sub.H(Σw1[j,i]x1[i]−θ.sub.H), Y=a.sub.0(Σw2[k,j]x2[j]−θ.sub.0). The value of the weight coefficient w1[j,i] may be changed by an amount that corresponds to η.sub.w1×(Σe2[k]×f′(Y)×w2[k,j])×f′(X)×x1[i].

(87) In the error circuit EU (output neuron circuit) of the second module **100_2**, the differential amplifier **115** obtains the difference signal e2[k] between the instructor signal e[k] and the signal o[k], the differentiator circuit DV obtains the differential signal f′(Y) of the signal Y, and the multiplier circuit MUL**4** obtains the result of multiplication of f(Y) by the difference signal e2[k], which is expressed as d2[k]=e2[k]×f′(Y). Here, Y is expressed as Y=a.sub.0(Σw2[k,j]x2[j]−θ.sub.0). Signal d2[k] is a signal that is output to the synapse circuit SU[k,j] of the second module **100_2**.

(88) In reaction to the input signal d2[k] from the error circuit EU[k] of the second module **100_2**, the synapse circuit SU[k,j] of the second module **100_2** changes the data (weight coefficient w2[k,j]) of the analog memory AM by an amount that corresponds to dw2=d2[k]×x2[j]=e2[k]×f′(Y)×x2[j]; the result of the change can be expressed as η.sub.w2×dw2=η.sub.w2×e2[k]×f′(Y)×x2[j]. An output signal w2[k,j]d2[k] that is output from the synapse circuit SU[k,j] of the second module **100_2** and is input to the error circuit EU[j] of the first module **100_1** is expressed as w2[k,j]d2[k]=e2[k]×f′(Y)×w2[k,j]. Note that the output signal w2[k, j]d2[k] corresponds to the output signal w2d2 in some cases.

(89) The error circuit EU[j] (hidden error circuit) of the first module **100_1** takes the following signals as input signals: a signal Σw1[j,i]x1[i] which is the sum of the output signals w1[j,i]x1[i] (current) of the synapse circuit SU[j,i] of the first module **100_1**, and a signal Σw2[k,j]d2[k]=Σe2[k]×f′(Y)×w2[k,j]=e1[j] which corresponds to a sum of currents expressed as w2[k,j]d2[k]=e2[k]×f′(Y)×w2[k, j], which is an output signal of the synapse circuit SU[k,j] of the second module **100_2**. The error circuit EU[j] of the first module **100_1** then obtains the following signals: signal X from Σw1[j,i]x1[i] through a differential amplifier, a difference signal EX from e1[j] through the differential amplifier **103**, an output signal f(X) from signal X through the differentiator circuit DV, and a multiplication result of f(X) and signal EX, which is expressed as d1[j]=e1[j]×f′(X)=Σe2[k]×f(Y)×w2[k,j]×f(X), through the multiplier circuit MUL. Here, X is expressed as X=a.sub.H(Σw1[j,i]x1[i]−Θ.sub.H). Signal d1[j] is a signal that is output to the synapse circuit SU[j,i] of the first module **100_1**.

(90) In reaction to the input signal d1[k] from the error circuit EU[j] of the first module **100_1**, the synapse circuit SU[j,i] of the first module **100_1** changes the data (weight coefficient w1[j,i]) of the analog memory AM by an amount that corresponds to dw1=d1[j]×x1[i]=Σe2[k]×f′(Y)×w2[k,j]×f(X)×x1[i]; the amount of the change can also be expressed as η.sub.w1×dw1=η.sub.w1×Σe2[k]×f′(Y)×w2[k,j]×f(X)×f′(X)×x1[i]. Note that the output signal w1[j,i]d1[j] (=wd1) of the synapse circuit SU[j,i] of the first module **100_1** is not output to other modules.

(91) As described above, in the semiconductor device, the weight coefficients w1[j,i] and w2[k,j] can be updated. In the semiconductor device, data corresponding to the weight coefficients w1[j,i] and w2[k,j] that enables the semiconductor device to obtain a desired output signal from an input signal can be stored in each analog memory AM. That is, the semiconductor device can learn.

(92) <Four-Layer Neural Network>

(93) FIG. **8** illustrates an example of the semiconductor device which is a four-layer neural network composed of the module **100** described above. Here, the neuron circuits NU of modules U[1, 1], U[1, 2], and U[1, 3] are the input neuron circuits, the neuron circuits NU of modules U[2, 1], U[2, 2], U[3, 1], U[3, 2], U[4, 1], and U[4, 2] are first hidden neuron circuits; the neuron circuits NU and the error circuits EU of modules U[2, 3] and U[3, 3] are second hidden neuron circuits and the output neuron circuits, respectively. The output signal wx of the synapse circuit SU of the module

U[1, 1] is the input signal i of the neuron circuits NU of the modules U[2, 1] and U[2, 2]; the output signal wx of the synapse circuit SU of the module U[1, 2] is the input signal i of the neuron circuits NU in modules U[3, 1] and U[3, 2]; the output signal wx of the synapse circuit SU of the module U[1, 3] is the input signal i of the neuron circuits NU of the modules U[4, 1] and U[4, 2]; the error signal WD of the synapse circuit SU of the module U[2, 3] is the input signal E of the error circuits EU of the modules U[2, 1], U[3, 1], and U[4, 1]; and the error signal WD of the synapse circuit SU of the module U[3, 3] is the input signal E of the error circuits EU of the modules U[2, 2], U[3, 2], and U[4, 2].

(94) Wiring groups H[1, 1] to H[4, 6] and V[1, 1] to V[3, 6], each of which are made up of a plurality of signal lines, are arranged among the modules. Programmable switches are provided at each of their intersections. The circuit configuration of a programmable switch PS is shown in FIG. **9**. Note that in FIG. **8**, the intersections where the programmable switches are placed have black dots placed thereupon, to denote the case in which the wiring groups are electrically connected to each other.

(95) The programmable switch PS illustrated in FIG. **9** is made up of transistors Tr**16** and Tr**17**; when the transistor Tr**16**, which includes the oxide semiconductor, is on (at which point the potential of a signal line WW is at "H"), data is stored from the signal line BL as the gate potential of the transistor Tr**17**, and the conduction of transistor Tr**17** is controlled in accordance with the data. In other words, the programmable switch PS can be programmed to control the electrical connection between the wirings V and H.

(96) In FIG. **8**, the input signal of the semiconductor device is input to the input neuron circuits of the modules U[1, 1], U[1, 2], and U[1, 3] through the wiring group H[1, 3]. The output of the output neuron circuit of the module U[3, 3] is output through the wiring group H[3, 6] as the output signal of the semiconductor device. The instructor signal of the semiconductor device is input to the output neuron circuits of the modules U[2, 3] and U[3, 3] through the wiring groups H[4, 4] and V[3, 3].

(97) The output signal of the synapse circuit SU of the module U[1, 1] is input to the neuron circuits NU of the modules U[2, 1] and U[2, 2] through the wiring groups V[1, 4] and H[2, 3].

(98) The output signal of the synapse circuit SU of the module U[1, 2] is input to the neuron circuits NU of the modules U[3, 1] and U[3, 2] through the wiring groups V[2, 4] and H[3, 3].

(99) The output signal of the synapse circuit SU of the module U[1, 3] is input to the neuron circuits NU of the modules U[4, 1] and U[4, 2] through the wiring groups V[3, 4] and H[4, 3].

(100) The output signals of the synapse circuits SU of the modules U[2, 1], U[3, 1], and U[4, 1] are input to the neuron circuit NU of the module U[2, 3] through the wiring groups V[1, 5] and H[2, 2].

(101) The output signals of the synapse circuits SU of the modules U[2, 2], U[3, 2] and U[4, 2] are input to the neuron circuit NU of the module U[2, 3] through the wiring groups V[2, 5] and H[3, 2].

(102) The output signals of the synapse circuits SU of the modules U[2, 3] and U[3, 3] are shared within the wiring group V[3, 5].

(103) The error signal of the synapse circuit SU of the module U[2, 3] is input to the error circuits EU of the modules U[2, 1], U[3, 1], and U[4, 1], through the wiring groups H[2, 4] and V[1, 3].

(104) The error signal of the synapse circuit SU of the module U[3, 3] is input to the error circuits EU of the modules U[2, 2], U[3, 2], and U[4, 2] through the wiring groups H[3, 4], and V[2, 3].

(105) The error signals of the synapse circuits SU of the modules U[2, 1] and U[2, 2] are input to the error circuit EU of the module U[1, 1] through the wiring groups H[2, 5] and V[1, 2].

(106) The error signals of the synapse circuits SU of the modules U[3, 1] and U[3, 2] are input to the error circuit EU of the module U[1, 2] through the wiring groups H[3, 5], and V[2, 2].

(107) The error signals of the synapse circuits SU of the modules U[4, 1] and U[4, 2] are input to the error circuit EU of the module U[1, 3] through the wiring groups H[4, 5] and V[3, 2].

(108) The semiconductor device described above learns by providing the learning data as the input signal of the input neuron circuit, providing the instructor signal that corresponds to the learning data to the output neuron circuit as the input signal, and updating the data in the analog memory in accordance with the error signal. By learning, the semiconductor device becomes able to determine whether the subject data and the learning data are matching or similar when the subject data is supplied as the input signal of the input neuron circuit. Here, by using data of an object (moving object) as a subject in the image data as the learning data, the semiconductor device becomes able to detect the object in the image data. In other words, efficient pattern extraction of the moving object from the image data becomes possible, and motion-compensated prediction can be performed efficiently.

(109) With such a structure, a semiconductor device including a hierarchical neural network architecture can be provided. The semiconductor device is configured with an analog circuit and capable of reducing the circuit size and retaining data without a refresh operation. Furthermore, in this device, the hierarchical structure such as the layer number of neurons and number of neurons within a layer can be freely changed.

EMBODIMENT 2

(110) In this embodiment, an operation example of the semiconductor device illustrated in FIG. **1** is described. Here, an operation of a three-layer neural network with modules **100_1** and **100_2** illustrated in FIG. **33** is described as an operation of the semiconductor device. The selector circuit is set so that the neuron circuit NU of the first module **100_1** is the input neuron circuit, the error circuit EU of the first module **100_1** is the hidden error circuit, the neuron circuit NU of the second module **100_2** is the hidden neuron circuit, and the error circuit EU of the second module **100_2** is the output neuron circuit. The output signal of the synapse circuit SU of the first module **100_1** serves as the input signal of the neuron circuit NU of the second module **100_2**, and the error signal from the synapse circuit SU of the second module **100_2** serves as the input signal of the error circuit EU of the first module **100_1**.

Operation Example

(111) The operation of the semiconductor device refers to an operation where the learning data is input to the semiconductor device illustrated in FIG. **1** of the embodiment above, the semiconductor device learns the learning data, the subject data is input to the semiconductor device, and the learning data and the subject data are determined to be matching, similar, or not matching. FIG. **10** and FIG. **11** are flowcharts of the operation of the semiconductor device.

(112) <<Learning>>

(113) First, operation where the semiconductor device illustrated in FIG. **1** learns data is described with reference to FIGS. **1** and **10**.

(114) [Step S**1-1**]

(115) In Step S**1-1**, a learning data is input from the outside to the input neuron circuit, that is, the neuron circuit NU of the first module **100_1**. Learning data corresponds to input signals I[1] to I[n] in FIG. **33**. Note that learning data is represented in binary here, and the number of neuron circuits NU to which learning data is input is determined in accordance with the number of bits of the learning data. The semiconductor device preferably is configured to input data that results in a fixed value of the output signal x from the neuron circuit NU that is not needed for the input of learning data. Furthermore, the semiconductor device is preferably configured, for example, to block the power supply to the neuron circuit NU. Here, the amount of learning data is given as n bits. Learning data I[1] to I[n] are input to the neuron circuits NU[1] to NU[n], respectively.

(116) [Step S**1-2**]

(117) In Step S**1-2**, the output signal x from the input neuron circuit, i.e., the neuron circuit NU of the first module **100_1**, is input to the synapse circuit SU of the first module **100_1**. The synapse circuit SU of the first module **100_1** outputs an output signal w1x, which is a signal obtained by multiplying the output signal x with the weight coefficient w1 that is contained in the analog memory AM, to the hidden error circuit, i.e., the error circuit EU of the first module **100_1**, and the hidden neuron circuit, i.e., the neuron circuit NU of the second module **100_2**.

(118) [Step S**1**-**3**]

(119) In Step S**1**-**3**, Σw1x, which is a sum of the output signals of the synapse circuits SU of the first module **100_1**, is input to the hidden neuron circuit, i.e., the neuron circuit NU of the second module **100_2**.

(120) Note that the number of hidden neuron circuits, i.e., the neuron circuits NU of the second module **100_2**, may be changed in accordance with the learning data. The semiconductor device preferably is configured to input data to the neuron circuit NU that is not needed, which results in the output signal x with a fixed value. Furthermore, the semiconductor device is preferably configured to block the power supply to the neuron circuit NU described in the previous line. Here, the number of neuron circuits NU of the second module **100_2** is m; the input of the neuron circuit NU is given as the sum of w1x[1] to w1x[m].

(121) [Step S**1**-**4**]

(122) In Step S**1**-**4**, an output signal x2 from the hidden neuron circuit, i.e., the neuron circuit NU of the second module **100_2**, is input to the synapse circuit SU of the second module **100_2**. The output signal x2 corresponds to the output signal x in FIG. **1**. The synapse circuit SU of the second module **100_2** outputs an output signal w2x2, which is a signal obtained by multiplying the output signal x2 by the weight coefficient w2 stored in the analog memory AM, to the output neuron circuit, i.e., the error circuit EU of the second module **100_2**. The weight coefficient w2 is a weight coefficient that is stored in the analog memory AM of the synapse circuit SU of the second module **100_2**.

(123) [Step S**1**-**5**]

(124) In Step S**1**-**5**, Σw2x2 is input to the output neuron circuit, i.e., the error circuit EU of the second module **100_2**. Σw2x2 corresponds to Σwx in FIG. **1**.

(125) [Step S**1**-**6**]

(126) The error circuits EU[1] to EU[m] performs multiplication according to Σw2x2 and the instructor signal e that is input from the outside; the error circuits EU[1] to EU[m] then output a difference signal d d2 to the neuron circuit NU of the second module **100_2**. The difference signal d2 corresponds to d[1] to d[m] in FIG. **1**. The instructor signal e corresponds to the input signals E[1] to E[n] that are input to the error circuits EU[1] to EU[n] of the second module.

(127) [Step S**1**-**7**]

(128) In Step S**1**-**7**, the weight coefficient w2 stored in the analog memory AM of the synapse circuit SU of the second module **100_2** is updated in accordance with the difference signal d2. In addition, in Step S**1**-**7**, the weight coefficient w2, which is updated in the synapse circuit SU of the second module **100_2**, is multiplied by the difference signal d2; subsequently, the output signal w2d2 is output. The output signals w2d2 are output to the hidden error circuits, i.e., the error circuits EU of the first module **100_1**, as the input signals E[1] to E[n].

(129) [Step S**1**-**8**]

(130) In Step S**1**-**8**, multiplication is performed with Σw1x, which is a sum of output signals, and the output signal w2d2, then a difference signal d1 is output to the neuron circuit NU of the first module **100_1**. The difference signal d1 corresponds to d[1] to d[m] in FIG. **1**.

(131) [Step S**1**-**9**]

(132) In Step S**1**-**9**, the weight coefficient w stored in the analog memory AM of the synapse circuit SU of the first module **100_1** is updated in accordance with the difference signal d1. After Step S**1**-**9** is complete, Step S**1**-**2** to Step S**1**-**9** are repeated for a predetermined number of times in accordance with the updated weight coefficients w1 and w2.

(133) In Step S**1**-**10**, it is determined whether Step S**1**-**2** to Step S**1**-**9** have been repeated for the predetermined number of times. When the number of repetitions reaches a predetermined number, the learning of the learning data is terminated.

(134) Note that the predetermined number here is ideally set so that Step S**1**-**2** to Step S**1**-**9** are repeated as many times until the error between the output signal o of the error circuit EU of the second module and the instructor signal e are contained within a specified value; however, the number of repetition may be set as a given number determined by experience.

(135) [Step S**1**-**11**]

(136) In Step S**1**-**11**, it is determined whether learning is complete for all the learning data. When there are learning data for which learning is not complete, Step S**1**-**1** to S**1**-**10** are repeated; when learning is complete for all data, the operation is terminated. Note that the semiconductor device may be configured to perform learning on the learning data that has already been learned by the semiconductor device, after all the sequences of learning all the learning data have been completed.

(137) In the neural network with hierarchical perceptron architecture, multiple hidden layers are preferably provided. When hidden neuron circuits and synapse circuits equivalent to hidden layers are provided in multiple layers, the weight coefficient can be updated repeatedly; the learning efficiency can thus be increased.

(138) <<Comparison>>

(139) Next, an operation in which the subject data is input to the semiconductor device illustrated in FIG. **33** that has learned the data beforehand and a result is output is described with reference to FIG. **11**. Among a plurality of data learned here, data that are associated to be the most similar to the subject data are output as a result.

(140) [Step S**2**-**1**]

(141) In Step S**2**-**1**, a subject data is input from the outside to the input neuron circuit, i.e., the neuron circuit NU of the first module **100_1**.

(142) [Step S**2**-**2**]

(143) In Step S**2**-**2**, the output signal x that corresponds to the subject data is output from the neuron circuit NU of the first module **100_1** and input to the synapse circuit SU of the first module **100_1**. The synapse circuit SU of the first module **100_1** outputs the output signal w1x, which is a signal obtained by multiplying the output signal x by the weight coefficient w1 retained in the Step S**1**-**9** of learning, to the hidden neuron circuit, i.e., the neuron circuit NU of the second module **100_2**.

(144) [Step S**2**-**3**]

(145) In Step S**2**-**3**, Σw1x, which is a sum of the output signals of the synapse circuits of the first module **100_1**, is input to the hidden neuron circuit, i.e., the neuron circuit NU of the second module **100_2**.

(146) In Step S**2**-**4**, the output signal x2 from the hidden neuron circuit, i.e., the neuron circuit NU of the second module **100_2**, is input to the synapse circuit SU of the second module **100_2**. The synapse circuit SU of the second module **100_2** outputs an output signal w2x2, which is a signal obtained by multiplying the output signal x2 by the weight coefficient w2 stored in the analog memory AM, to the output neuron circuit, i.e., the error circuit EU of the second module **100_2**.

(147) In Step S**2**-**5**, Σw2x2, which is a sum of output signals from the synapse circuit SU of the second module **100_2**, is input to the output neuron circuit, i.e., error circuit EU of the second module **100_2**. The output neuron circuit, i.e., the error circuit EU of the second module **100_2** outputs the output signal o.

(148) When the learned plurality of data includes data which matches, or is very similar to the data contained in the output signal o, the data in the output signal o is the data that was supplied as the instructor signal when the learning data was learned. In other words, judgement whether learning data and subject data match, are similar, or do not match can be made.

(149) By performing Step S**1**-**1** to Step S**1**-**10**, and Step S**2**-**1** to Step S**2**-**5**, the semiconductor device illustrated in FIG. **1** can learn the learning data, then output a signal that signifies whether the learning data and the subject data match or do not match. Thus, the semiconductor device illustrated in can perform processing such as pattern recognition or associative storage.

EMBODIMENT 3

(150) In this embodiment, an operation example where the semiconductor device described in Embodiment 1 and illustrated in FIG. **1** is used as an encoder is described.

Example of Motion Detection of an Object

(151) Firstly, an example of detecting a motion of an object is described. FIGS. **12**A to **12**F illustrate an algorithm performed by the encoder on image data for detection of the motion of the object.

(152) FIG. **12**A shows image data **10** that has a triangle **11** and a circle **12**. FIG. **12**B shows image data **20** where the triangle **11** and the circle **12** of the image data **10** are moved to the upper right.

(153) Image data **30** in FIG. **12**C shows an operation by which a region **31** including the triangle **11** and the circle **12** is extracted from the image data **10**. In the image data **30**, a cell at the upper left corner of the extracted region **31** is regarded as a reference point (0, 0), and numbers indicating positions in the right/left and upper/lower directions are added to the image data **10**. The extracted region **31** of FIG. **12**C is shown in FIG. **12**E.

(154) Image data **40** in FIG. **12**D shows an operation by which a plurality of regions **41** are extracted from the image data **20** by cutting out regions from the image data **20**. The image data **40** is image data with the numbers indicating the positions in left/right and upper/lower directions, which are added to the image data **30**, are also added to the image data **20**. In other words, from the image data **30** and the image data **40**, the position to which the region **31** moves can be expressed with a displacement (motion vector). FIG. **12**F shows some of the plurality of extracted regions **41**.

(155) After the extraction operation of the plurality of regions **41**, an operation in which the plurality of regions **41** are sequentially compared with the region **31** is performed, to detect a motion of the objects. This comparison operation detects that the region **31** and the region **41** with a motion vector (1, −1) match, and the region **31** and the regions **41** with motion vectors other than the motion vector (1, −1) do not match. Accordingly, the motion vector (1, −1) from the region **31** to the region **41** can be obtained.

(156) Note that in this specification, the data of the region **31** described above is expressed as learning data in some cases, and the data of the one of the plurality of regions **41** described above is expressed as subject data in some cases.

(157) Although the extraction, comparison, and detection operations are performed based on the regions each formed of 4×4 cells in FIGS. **12**A to **12**F, the size of the regions is not limited thereto in this operation example. The size of the regions may be changed as appropriate in accordance with the size of image data to be extracted. For example, the extraction, comparison, and detection operations may be performed based on the regions each formed of 3×5 cells. Additionally, there is no limitation on the number of pixels forming a cell; for example, one cell used for forming a region may be formed of 10×10 pixels, or be one pixel. Alternatively, one cell used for forming a region may be formed of 5×10 pixels, for example.

(158) Depending on the video content, image data contained in the region **31** may be changed. For example, the triangle **11** or the circle **12** in the region **31** may be scaled in the image data **40**. Alternatively, the triangle **11** or the circle **12** in the region **31** may be rotated in the image data **40**. To achieve this, it is preferable that whether or not the region **31** and any of the plurality of regions **41** are identical be determined by characteristics extraction or the like. Motion-compensated prediction becomes possible when image data where the region **31** moves in the motion vector direction is generated from the image data of the region **31** and a difference between the generated data and the plurality of regions **41** is obtained. Furthermore, when the amount of motion of the image data in the region **31** does not coincide with an integral multiple of a pixel pitch, the semiconductor device may be configured so that signals output to the outside are calculated through the comparison of the region **31** and the plurality of regions **41**, the displacement that allows for the smallest amount of difference between those output signals is inferred, and the smallest amount of difference is detected as an object's displacement (motion vector).

(159) <Judgement Whether Image Data Match, are Similar, or do not Match>

(160) Next, a motion-compensated prediction method using the encoder is described with reference to FIG. **13**.

(161) [Step S**3-1**]

(162) In Step S**3-1**, the data of the region **31** is input as the learning data to the neuron circuit NU of the first module.

(163) [Step S**3-2**]

(164) In Step S**3-2**, operations equivalent to Step S**1-2** to Step S**1-10** are performed on the input data of the region **31**. That is, the update of the weight coefficients of each of the synapse circuits SU is repeated, and the weight coefficient of the synapse circuit SU that corresponds to the data of the region **31** is updated.

(165) [Step S**3-3**]

(166) In Step S**3-3**, data of one of the plurality of regions **41** is input as the subject data to the semiconductor device illustrated in FIG. **1**; this semiconductor device contains the weight coefficient that is updated in Step S**3-2**.

(167) [Step S**3-4**]

(168) In Step S**3-4**, input of the data of one of the plurality of regions **41** is performed in an operation similar to Step S**2-2** to Step S**2-5**. In other words, by inputting data of one of the plurality of regions **41**, the semiconductor device which has learned data of the region **31** outputs data that are associated therefrom.

(169) Here, the semiconductor device determines whether or not the data of the region **31** and the data of the plurality of regions **41** match.

(170) [Step S**3-5**]

(171) In Step S**3-5**, the step to which the sequence will proceed is decided in reaction to the determination above.

(172) When the data of region **31** and the data of one of the plurality of regions **41** do not match according to the determination above, Step S**3-3** and Step S**3-4** will be performed again taking a region **41** that is different from the one of the plurality of region **41** as the subject data.

(173) In addition, when the data of the region **31** and the data of the one of the plurality of regions **41** match according to the determination above, the operation terminates after obtaining the motion vector of the one of the plurality of the regions **41** that uses the region **31** as a standard. By obtaining the motion vector, motion-compensated prediction using the motion vector as a difference can be performed. By performing the motion-compensated prediction, video data can be efficiently compressed.

(174) Furthermore, the semiconductor device determines the data of the region **31** and the data of the one of the plurality of regions **41** match even when the two data are similar. When the data of the one of the plurality of regions **41** is similar to the data of the plurality of regions **41**, the data of the one of the plurality of the regions **41** is determined to match with the data of the plurality of regions **41**. In this case, by determining the matching degree of the data of the one of the plurality of regions **41** to the data of each of the plurality of regions **41**, the change in position of the object is inferred; this position is obtained as the motion vector of the object. Then, the operation is terminated.

(175) In addition, when all of the data of the regions **41** are compared as the subject data and there are no match or similarity between the learning data and all of the subject data in the determination, the semiconductor device assesses that the motion vector for motion-compensated prediction cannot be obtained from the data of the region **31** and the data of the plurality of regions **41**; thus, the operation is terminated.

(176) By performing the operations above, a neural network with the hierarchical perceptron architecture can be used as an encoder that compresses video data. This makes possible to achieve a highly efficient encoder that can compress a large volume of image data.

EMBODIMENT MODE 3

(177) In this embodiment, a broadcast system according to the disclosed invention will be described.

(178) <Broadcasting System>

(179) FIG. **14** is a block diagram that schematically illustrates a configuration example of the broadcasting system. A broadcasting system **500** includes a camera **510**, a transceiver **511**, a receiver **512**, and a display device **513**. The camera **510** includes an image sensor **520** and an image processor **521**. The transceiver **511** includes an encoder **522** and a modulator **523**. The receiver **512** includes a demodulator **525** and a decoder **526**. The display device **513** includes an image processor **527** and a display portion **528**.

(180) When the camera **510** is capable of capturing 8K video, the image sensor **520** has an adequate number of pixels for capturing a color image in 8K resolution. For example, when one pixel is made up of one red (R) subpixel, two green (G) subpixels, and one blue (B) subpixel, the image sensor **520** needs at least 7680×4320×4 [R, G+G, B] pixels; when the camera **510** is a camera for capturing 4K images, the image sensor **520** needs at least 3840×2160×4 pixels; when the camera **510** is a camera for capturing 2K images, the image sensor **520** needs at least 1920×1080×4 pixels.

(181) The image sensor **520** generates a Raw data **540** which is unprocessed. The image processor **521** performs image processing (such as noise removal or interpolation processing) on the Raw data **540** and generates video data **541**. The video data **541** is output to the transceiver **511**.

(182) The transceiver **511** processes the video data **541**, and generates a broadcasting signal **543** that is compliant with a broadcasting bandwidth (the broadcasting signal may be referred to as a carrier wave in some cases). The encoder **522** processes the video data **541** and generates encoding data **542**. The encoder **522** performs operations such as encoding of the video data **541**, addition of data for broadcasting control (e.g. authentication data) to the video data **541**, encryption, and scrambling (data rearrangement for spread spectrum).

(183) The modulator **523** generates and outputs the broadcasting signal **543** by performing IQ modulation on the encoding data **542**. The broadcasting signal **543** is a composite signal that has an I (identical phase) component and a Q (quadrature phase) component. A TV broadcasting station is tasked with obtaining the video data **541**, and supplying the broadcasting signal **543**.

(184) The receiver **512** receives the broadcast signal **543**. The receiver **512** has a function of converting the broadcasting signal **543** to video data **544** that can be displayed on the display device **513**. The demodulator **525** demodulates the broadcasting signal **543**, and decomposes the broadcasting signal **543** to two analog signals, i.e., an I signal and a Q signal.

(185) The decoder **526** has a function of converting the I signal and the Q signal into digital signals. Moreover, the decoder **526** processes the digital signal through various methods and generates a data stream. The methods of processing performed on the digital signal include frame separation, decoding of a low density parity check (LDPC) code, separation of data for broadcasting control, descrambling, and the like. The decoder **526** decodes the data stream and generates the video data **544**. Processing methods for decoding include orthogonal conversion such as discrete cosine transform (DCT) and discrete sine transform (DST), intra-frame prediction, motion-compensated prediction, and the like.

(186) The video data **544** is input to the image processor **527** of the display device **513**. The image processor **527** processes the video data **544** and generates a data signal **545** that can be input to the display portion **528**. The processing performed by the image processor **527** include image processing (e.g., gamma processing), digital-analog conversion, and the like. The display portion **528** displays an image after input of the data signal **545**.

(187) A schematic representation of the data transfer within a broadcasting system is shown in FIG. **15**. FIG. **15** illustrates paths that radio waves (broadcasting signals) transmitted from a broadcasting station **561** take to television receivers (TV) **560** in each household. The TV **560** is equipped with the receiver **512** and the display device **513**. Examples of an artificial satellite **562** include a communication satellite (CS) and a broadcasting satellite (BS). Examples of an antenna **564** include a BS/110° CS antenna and a CS antenna. Examples of an antenna **565** include an ultra-high frequency (UHF) antenna.

(188) Radio waves **566**A and **566**B are broadcasting signals for satellite broadcasting. When the artificial satellite **562** receives the radio wave **566**A, the artificial satellite **562** transmits the radio wave **566**B to the ground. The radio wave **566**B is received by the antenna **564** in each household, which enables the viewing of satellite TV broadcasting on the TV **560**. Alternatively, the radio wave **566**B is received by an antenna of another broadcasting station, where a receiver processes the radio wave **566**B into a signal that can be transmitted to an optical cable. The broadcasting station then sends the broadcasting signal to the TV **560** in each household using an optical cable network. Radio waves **567**A and **567**B are broadcasting signals for terrestrial broadcasting. A radio tower **563** amplifies the received radio wave **567**A, and transmits the radio wave **567**B. Each household can view terrestrial TV broadcasting on the TV **560** by receiving the radio wave **567**B with the antenna **565**.

(189) Furthermore, the video distribution system according to this embodiment is not limited to a system for TV broadcasting. In addition, the image data to be distributed may be either video data or still image data.

(190) For example, the video data **541** of the camera **510** may be distributed through a high-speed IP network. For example, a system for distributing the video data **541** can be used in the medical field for giving out medical care and diagnoses remotely. Images with higher resolution are demanded for accurate image diagnoses and medical care; images with high resolution, such as 8K, 4K, and 2K images, are thus demanded for images for medical use. FIG. **16** schematically illustrates an emergency medical system that utilizes the video data distribution system.

(191) The communication between an ambulance **600** and a medical institution **601** and between the medical institution **601** and a medical institution **602** are performed using a high-speed network **605**. The ambulance **600** is equipped with a camera **610**, an encoder **611**, and a communication device **612**.

(192) The camera **610** is used to capture images of a patient being transported to the medical institution **601**. Video data **615** obtained by the camera **610** may be transmitted without compression by the communication device **612**. This enables the transmission of the high-resolution video data **615** to the medical institution **601** with little delay. When the high-speed network **605** cannot be used for the communication between the ambulance **600** and the medical institution **601**, the video data can be encoded with the encoder **611**, and encoded video data **616** can be transmitted.

(193) In the medical institution **601**, the video data transmitted from the ambulance **600** is received by a communication device **620**. When the received video data is uncompressed data, the video data is transmitted through the communication device **620** to the display device **623**, where the video data is displayed. When the video data is compressed data, the data is decompressed in a decoder **621**, and then is transmitted to the display device **623**, where the video data is displayed. Medical practitioners give instructions to a crew of the ambulance **600**, or to staff members in the medical institution **601** who treat the patient, based on the image on the display device **623**. The distribution system illustrated in FIG. **16** can transmit high-resolution images; this allows the medical practitioners in the medical institution **601** to inspect the patient being transported in detail. This allows the medical practitioners to give instructions that are more precise to the crew of the ambulance **600** and the staff members of the medical institution **601**; this allows the improvement of the survival rate of the patients.

(194) The communication of video data between the medical instiuitions **601** and **602** is similar to that described above. The medical images obtained with an image diagnosis tool such as CT, and MRI in the medical institution **601** can be transmitted to the medical institution **602**. Here, the ambulance **600** is used as an example. However, the methods for transporting the patient may be aircrafts such as helicopters, or ships.

(195) FIG. **15** illustrates an example in which a receiver is included in the TV **560**. A configuration in which a stand-alone receiver is used to receive signals to display images on the TV **560** is also possible. An example of such a case is shown in FIGS. **17**A to **17**D. As illustrated in FIG. **17**A, a receiver **571** may be provided on the outside of the TV **560**. As illustrated in FIG. **17**B, the antennae **564** and **565** and the TV **560** may transmit data to, and receive data from each other through wireless transmitters **572** and **573**. In this case, the wireless transmitters **572** and **573** also serve as receivers. As illustrated in FIG. **17**C, the wireless transmitter **573** may be incorporated in the TV **560**.

(196) The receiver can be of a portable size. A receiver **574** illustrated in FIG. **17**D includes a connector portion **575**. If an electronic device such as a display device or an information terminal (e.g., a personal computer, a smartphone, a cellular phone, and a tablet-type terminal) is equipped with a terminal that is capable of connecting with the connector portion **575**, they can be used to watch satellite and terrestrial broadcasting.

(197) The semiconductor device described in Embodiment 1 may be applied to the encoder **522** in the broadcasting system **500** illustrated in FIG. **14**. In addition, the encoder **522** may have a configuration including a combination of the semiconductor device and a dedicated IC, a processor such as a graphical processing unit (GPU) or a central processing unit (CPU). Furthermore, the encoder **522** may be integrated into one dedicated IC chip.

(198) <Encoder>

(199) FIG. **18** is a block diagram that illustrates an example of the encoder **522**. The encoder **522** includes circuits **591** to **594**.

(200) The circuit **591** performs source encoding, and includes an inter-frame prediction circuit **591***a*, a motion-compensated prediction circuit **591***b*,

and a DCT circuit **591***c*. The circuit **592** includes a circuit for video encoding by multiplexing. The circuit **593** includes a low density parity check (LDPC) encoding circuit **593***a*, an authentication processing circuit **593***b*, and a scrambler **593***c*. The circuit **594** is a digital-analog conversion (DAC) portion.

(201) The circuit **591** performs source encoding on the video data **541** that has been transmitted. Source encoding refers to a process in which a redundant component included in image information is removed. Note that original video data cannot be completely restored from the data output from the circuit **591**; it can thus be said that source encoding is an irreversible process.

(202) The inter-frame prediction circuit **591***a* creates a prediction frame from a frame before the frame subject to encoding, or a frame after the frame subject to encoding, or both, thereby encoding the prediction frame. The motion-compensated prediction circuit **591***b* detects the motion and deformation of the subject within the video data **541**, calculates the displacement and the amount of rotation and expansion and contraction, and creates a prediction frame of the frame that includes the subject, thereby encoding the prediction frame. The DCT circuit **591***c* uses discrete cosine transform to convert information obtained in the pixel region that corresponds to the video data to information in a frequency region.

(203) The circuit **591** has a function of quantization of the source-encoded video data **541** through the inter-frame prediction circuit **591***a*, the motion-compensated prediction circuit **591***b*, and the DCT circuit **591***c*. Here, quantization means an operation in which frequency components obtained with the DCT circuit **591***c* are each coordinated with a discrete value. This operation can reduce large data included in the video data **541**. Furthermore, the circuit **591** sends a data stream **551**, which includes video data that has been source-encoded and quantized, and information that is obtained by motion-compensated prediction, to the circuit **592**.

(204) The circuit **592** is a circuit in which the information included in the data stream **551** is compressed by variable-length coding, then is multiplexed. Here, multiplexing refers to a process in which a plurality of pieces of information are aligned so that they can be transmitted as one bit string or one byte string. The information subjected to video encoding for multiplexing is transmitted to the circuit **593** as a data stream **552**.

(205) The circuit **593** mainly performs error-correction encoding, authentication processing, and encryption on the data stream **552** which is transmitted from the circuit **592**. The LDPC encoding circuit **593***a* transmits data through noisy communication channels by performing error correction encoding. The authentication processing circuit **593***b* adds a code for identification (ID), a password, or the like to the data to be transmitted so that the data cannot be recovered by unintended receivers. The scrambler **593***c* is equipment that converts the transmission data column of data to be transmitted to a random column that is not related to a signal data column. The converted data can be recovered to the original data by descrambling at a receiver side. The circuit **593** performs error correction encoding, authentication processing, and encryption on the data stream **552**; the resulting data is transmitted to the circuit **594** as the data stream **553**.

(206) The circuit **594** is a circuit for digital-analog conversion of the data stream **553**, to transmit the data stream **553** to the receiver **512**. The data stream **553** after digital-to-analog conversion is transmitted to the modulator **523** as the encoded data **542**.

EMBODIMENT 5

(207) Described in this embodiment are transistors of one embodiment of the disclosed invention.

(208) Transistors according to one embodiment of the present invention each preferably include an nc-OS or a CAAC-OS, which are described in Embodiment 5.

Structure Example 1 of Transistor

(209) FIGS. **19**A to **19**C are a top view and cross-sectional diagrams of a transistor **1400***a*. FIG. **19**A is a top view. FIG. **19**B is a cross-sectional diagram taken along dashed-dotted line A**1**-A**2** in FIG. **19**A, and FIG. **19**C is a cross-sectional diagram taken along dashed-dotted line A**3**-A**4** in FIG. **19**A. Note that for simplification of the drawing, some components in the top view in FIG. **19**A are not illustrated. Note that the dashed-dotted line A**1**-A**2** and the dashed-dotted line A**3**-A**4** are sometimes referred to as a channel length direction of the transistor **1400***a* and a channel width direction of the transistor **1400***a*, respectively.

(210) The transistor **1400***a* includes a substrate **1450**, an insulating film **1401** over the substrate **1450**, a conductive film **1414** over the insulating film **1401**, an insulating film **1402** covering the conductive film **1414**, an insulating film **1403** over the insulating film **1402**, an insulating film **1404** over the insulating film **1403**, a metal oxide **1431** and a metal oxide **1432** which are stacked in this order over the insulating film **1404**, a conductive film **1421** touching top and side surfaces of the metal oxide **1432**, a conductive film **1423** also touching top and side surfaces of the metal oxide **1432**, a conductive film **1422** over the conductive film **1421**, a conductive film **1424** over the conductive film **1423**, an insulating film **1405** over the conductive films **1422** and **1424**, a metal oxide **1433** touching the metal oxides **1431** and **1432**, the conductive films **1421** to **1424**, and the insulating film **1405**, an insulating film **1406** over the metal oxide **1433**, a conductive film **1411** over the insulating film **1406**, a conductive film **1412** over the conductive film **1411**, a conductive film **1413** over the conductive film **1412**, an insulating film **1407** covering the conductive film **1413**, and an insulating film **1408** over the insulating film **1407**. Note that the metal oxides **1431** to **1433** are collectively referred to as a metal oxide **1430**.

(211) The metal oxide **1432** is a semiconductor and serves as a channel of the transistor **1400***a*.

(212) Furthermore, the metal oxides **1431** and **1432** include a region **1441** and a region **1442**. The region **1441** is formed in the vicinity of a region where the conductive film **1421** is in contact with the metal oxides **1431** and **1432**. The region **1442** is formed in the vicinity of a region where the conductive film **1423** is in contact with the metal oxides **1431** and **1432**.

(213) The regions **1441** and **1442** serve as low-resistance regions. The region **1441** contributes to a decrease in the contact resistance between the conductive film **1421** and the metal oxides **1431** and **1432**. Similarly, the region **1442** contributes to a decrease in the contact resistance between the conductive film **1423** and the metal oxides **1431** and **1432**.

(214) The conductive films **1421** and **1422** serve as one of source and drain electrodes of the transistor **1400***a*. The conductive films **1423** and **1424** serve as the other of the source and drain electrodes of the transistor **1400***a*.

(215) The conductive film **1422** is configured to allow less oxygen to pass therethrough than the conductive film **1421**. It is thus possible to prevent a decrease in the conductivity of the conductive film **1421** due to oxidation.

(216) Similarly, the conductive film **1424** is configured to allow less oxygen to pass therethrough than the conductive film **1423**. It is thus possible to prevent a decrease in the conductivity of the conductive film **1423** due to oxidation.

(217) The conductive films **1411** to **1413** serve as a first gate electrode of the transistor **1400***a*.

(218) The conductive films **1411** and **1413** are configured to allow less oxygen to pass therethrough than the conductive film **1412**. It is thus possible to prevent a decrease in the conductivity of the conductive film **1412** due to oxidation.

(219) The insulating film **1406** serves as a first gate insulating film of the transistor **1400***a*.

(220) The conductive film **1414** serves as a second gate electrode of the transistor **1400***a*.

(221) The potential applied to the conductive films **1411** to **1413** may be the same as or different from that applied to the conductive film **1414**. The conductive film **1414** may be omitted in some cases.

(222) The insulating films **1401** to **1404** serve as a base insulating film of the transistor **1400***a*. The insulating films **1402** to **1404** also serve as a second gate insulating film of the transistor **1400***a*.

(223) The insulating films **1405** to **1408** serve as a protective insulating film or an interlayer insulating film of the transistor **1400***a*.

(224) As shown in FIG. **19**C, the side surface of the metal oxide **1432** is surrounded by the conductive film **1411**. With this structure, the metal oxide **1432** can be electrically surrounded by an electric field of the conductive film **1411**. A structure in which a semiconductor is electrically surrounded by an electric field of a gate electrode is referred to as a surrounded channel (s-channel) structure. Therefore, a channel is formed in the entire metal oxide **1432** (bulk). In an s-channel structure, a large amount of current can flow between a source and a drain of a transistor, so that the transistor can have a high on-state current.

(225) The s-channel structure, because of its high on-state current, is suitable for a semiconductor device such as large-scale integration (LSI) which requires a miniaturized transistor. A semiconductor device including the miniaturized transistor can have a high integration degree and high density.

(226) In the transistor **1400**a, a region serving as a gate electrode is formed so as to fill an opening formed in the insulating film **1405** or the like, that is, in a self-aligned manner.

(227) As shown in FIG. **19**B, the conductive films **1411** and **1422** have a region where they overlap with each other with the insulating film positioned therebetween. Similarly, the conductive films **1411** and **1423** have a region where they overlap with each other with the insulating film positioned therebetween. These regions serve as the parasitic capacitance caused between the gate electrode and the source or drain electrode and might decrease the operation speed of the transistor **1400**a. This parasitic capacitance can be reduced by providing the insulating film **1405** in the transistor **1400**a. The insulating film **1405** preferably contains a material with a low relative dielectric constant.

(228) FIG. **20**A is an enlarged view of the center of the transistor **1400**a. A width L_G denotes the length of the region in the bottom surface of the conductive film **1411**, which faces parallel to the top surface of the metal oxide **1432** with the insulating film **1406** and the metal oxide **1433** positioned therebetween. The width L_G is the line width of the gate electrode. In FIG. **20**A, a width L_{SD} indicates the length between the conductive films **1421** and **1423**. The width L_{SD} is the length between the source electrode and the drain electrode.

(229) In general, the width L_{SD} is determined by the minimum feature size. As shown in FIG. **20**A, the width L_G is narrower than the width L_{SD}. This signifies that in the transistor **1400**a, the line width of the gate electrode can be made smaller than the minimum feature size. Specifically, the width L_G can be greater than or equal to 5 nm and less than or equal to 60 nm, preferably greater than or equal to 5 nm and less than or equal to 30 nm.

(230) In FIG. **20**A, a height H_{SD} is the total thickness of the conductive films **1421** and **1422**, or the total thickness of the conductive films **1423** and **1424**.

(231) The thickness of the insulating film **1406** is preferably less than or equal to the height H_{SD}, in which case the electric field of the gate electrode can be applied to the entire channel formation region. The thickness of the insulating film **1406** is less than or equal to 30 nm, preferably less than or equal to 10 nm.

(232) The parasitic capacitance between the conductive films **1422** and **1411** and the parasitic capacitance between the conductive films **1424** and **1411** are inversely proportional to the thickness of the insulating film **1405**. For example, the thickness of the insulating film **1405** is preferably larger than or equal to three times, and further preferably larger than or equal to five times the thickness of the insulating film **1406**, in which case the parasitic capacitance is negligibly small. As a result, the transistor **1400**a can operate at high frequencies.

(233) Components of the transistor **1400**a will be described below.

(234) <<Metal Oxide Layer>>

(235) First, a metal oxide that can be used as the metal oxides **1431** to **1433** will be described.

(236) The transistor **1400**a preferably has a low current (off-state current) flowing between a source and a drain when the transistor **1400**a is in an off state. Examples of the transistor with a low off-state current include a transistor including an oxide semiconductor in a channel formation region.

(237) The metal oxide **1432** is an oxide semiconductor containing indium (In), for example. The metal oxide **1432** can have high carrier mobility (electron mobility) by containing indium, for example. The metal oxide **1432** preferably contains an element M. The element M is preferably aluminum (Al), gallium (Ga), yttrium (Y), tin (Sn), or the like. Other elements that can be used as the element M are boron (B), silicon (Si), titanium (Ti), iron (Fe), nickel (Ni), germanium (Ge), zirconium (Zr), molybdenum (Mo), lanthanum (La), cerium (Ce), neodymium (Nd), hafnium (Hf), tantalum (Ta), tungsten (W), and the like. Note that two or more of the above elements may be used in combination as the element M. The element M is an element having high bonding energy with oxygen, for example. The element M is an element whose bonding energy with oxygen is higher than that of indium, for example. The element M is an element that can increase the energy gap of the metal oxide, for example. Furthermore, the metal oxide **1432** preferably contains zinc (Zn). When containing zinc, the metal oxide is easily crystallized in some cases.

(238) Note that the metal oxide **1432** is not limited to the oxide semiconductor containing indium. The metal oxide **1432** may be an oxide semiconductor that does not contain indium and contains at least one of zinc, gallium, and tin (e.g., a zinc tin oxide or a gallium tin oxide).

(239) For the metal oxide **1432**, an oxide semiconductor with a wide energy gap is used, for example. The energy gap of the metal oxide **1432** is, for example, greater than or equal to 2.5 eV and less than or equal to 4.2 eV, preferably greater than or equal to 2.8 eV and less than or equal to 3.8 eV, more preferably greater than or equal to 3 eV and less than or equal to 3.5 eV.

(240) The metal oxide **1432** is preferably a CAAC-OS film which is described later in Embodiment 6.

(241) The metal oxides **1431** and **1433** include, for example, one or more elements other than oxygen included in the metal oxide **1432**. Since the metal oxides **1431** and **1433** include one or more elements other than oxygen included in the metal oxide **1432**, an interface state is less likely to be formed at an interface between the metal oxides **1431** and **1432** and an interface between the metal oxides **1432** and **1433**.

(242) In the case of using an In-M-Zn oxide as the metal oxide **1431**, when the total proportion of In and M is assumed to be 100 atomic %, the proportions of In and M are preferably set to be lower than 50 atomic % and higher than 50 atomic %, respectively, and more preferably lower than 25 atomic % and higher than 75 atomic %, respectively. When the metal oxide **1431** is formed by a sputtering method, a sputtering target with the above composition is preferably used. For example, the atomic ratio of In to M to Zn in the metal oxide **1431** is preferably 1:3:2 or in the neighborhood of 1:3:2, or 1:3:4 or in the neighborhood of 1:3:4.

(243) In the case of using an In-M-Zn oxide as the metal oxide **1432**, when the total proportion of In and M is assumed to be 100 atomic %, the proportions of In and M are preferably set to be higher than 25 atomic % and lower than 75 atomic %, respectively, more preferably higher than 34 atomic % and lower than 66 atomic %, respectively. When the metal oxide **1432** is formed by a sputtering method, a sputtering target with the above composition is preferably used. For example, the atomic ratio of In to M to Zn in the metal oxide **1432** is preferably one of the following ratios: 1:1:1 or in the neighborhood of 1:1:1, 1:1:1.2 or in the neighborhood of 1:1:1.2, 2:1:3 or in the neighborhood of 2:1:3, 3:1:2 or in the neighborhood of 3:1:2, and 4:2:4.1 or in the neighborhood of 4:2:4.1. In particular, when a sputtering target with an atomic ratio of In to Ga to Zn of 4:2:4.1 is used, the atomic ratio of In to Ga to Zn in the metal oxide **1432** may be in the neighborhood of 4:2:3.

(244) In the case of using an In-M-Zn oxide as the metal oxide **1433**, when the total proportion of In and M is assumed to be 100 atomic %, the proportions of In and M are preferably set to be lower than 50 atomic % and higher than 50 atomic %, respectively, more preferably lower than 25 atomic % and higher than 75 atomic %, respectively. For example, the atomic ratio of In to M to Zn in the metal oxide **1433** preferably is 1:3:2 or in the neighborhood of 1:3:2, or 1:3:4 or in the neighborhood of 1:3:4. The metal oxide **1433** may be a metal oxide that is of the same type as the metal oxide **1431**.

(245) The metal oxide **1431** or the metal oxide **1433** does not need to contain indium in some cases. For example, the metal oxide **1431** or the metal oxide **1433** may be gallium oxide.

(246) Next, the function and effect of the metal oxide **1430**, which includes a stack of the metal oxides **1431** to **1433**, are described with reference to the energy band diagram of FIG. **20**B. FIG. **20**B illustrates the energy band structure of a section signified by the dashed-dotted line Y_1-Y_2 in FIG. **20**A. Furthermore, FIG. **20**B illustrates the energy band structure of the channel formation region and the vicinities thereof in the transistor **1400**a.

(247) In FIG. **20**B, Ec**1404**, Ec**1431**, Ec**1432**, Ec**1433**, and Ec**1406** indicate the energy at the bottom of the conduction band of the insulating film **1404**, the metal oxide **1431**, the metal oxide **1432**, the metal oxide **1433**, and the insulating film **1406**, respectively.

(248) Here, a difference in energy between the vacuum level and the bottom of the conduction band (the difference is also referred to as electron affinity) corresponds to a value obtained by subtracting an energy gap from a difference in energy between the vacuum level and the top of the

valence band (the difference is also referred to as an ionization potential). The energy gap can be measured using a spectroscopic ellipsometer. The energy difference between the vacuum level and the top of the valence band can be measured using an ultraviolet photoelectron spectroscopy (UPS) device.

(249) Since the insulating films **1404** and **1406** are insulators, Ec**1406** and Ec**1404** are closer to the vacuum level (i.e., have a lower electron affinity) than Ec**1431**, Ec**1432**, and Ec**1433**.

(250) The metal oxide **1432** is a metal oxide having higher electron affinity than those of the metal oxides **1431** and **1433**. For example, as the metal oxide **1432**, a metal oxide having an electron affinity greater than or equal to 0.07 eV and less than or equal to 1.3 eV, preferably greater than or equal to 0.1 eV and less than or equal to 0.7 eV, more preferably greater than or equal to 0.15 eV and less than or equal to 0.4 eV is used.

(251) An indium gallium oxide has a small electron affinity and an excellent oxygen-blocking property. Therefore, the metal oxide **1433** preferably includes an indium gallium oxide. The gallium atomic ratio [Ga/(In+Ga)] is, for example, higher than or equal to 70%, preferably higher than or equal to 80%, more preferably higher than or equal to 90%.

(252) At this time, when a gate voltage is applied, a channel is formed in the metal oxide **1432** having the highest electron affinity among the metal oxides **1431** to **1433**.

(253) Thus, electrons move mainly in the metal oxide **1432**, not in the metal oxides **1431** and **1433**. Hence, the on-state current of the transistor hardly varies even when the density of interface states, which inhibit electron movement, is high at the interface between the metal oxide **1431** and the insulating film **1404** or at the interface between the metal oxide **1433** and the insulating film **1406**. The metal oxides **1431** and **1433** function as an insulating film.

(254) In some cases, there is a mixed region of the metal oxides **1431** and **1432** between the metal oxides **1431** and **1432**. Furthermore, in some cases, there is a mixed region of the metal oxides **1432** and **1433** between the metal oxides **1432** and **1433**. The mixed region has a low interface state density. Because the mixed region has a low interface state density, a stack of the metal oxides **1431** to **1433** has a band structure where energy at each interface and in the vicinity of the interface is changed continuously (continuous junction).

(255) As described above, the interface between the metal oxides **1431** and **1432** or the interface between the metal oxides **1432** and **1433** has a low interface state density. Hence, electron movement in the metal oxide **1432** is less likely to be inhibited and the on-state current of the transistor can be increased.

(256) Electron movement in the transistor is inhibited, for example, in the case where physical unevenness in a channel formation region is large. To increase the on-state current of the transistor, for example, root mean square (RMS) roughness with a measurement area of 1 μm×1 μm of a top surface or a bottom surface of the metal oxide **1432** (a formation surface; here, the top surface of the metal oxide **1431**) is less than 1 nm, preferably less than 0.6 nm, more preferably less than 0.5 nm, still more preferably less than 0.4 nm. The average surface roughness (also referred to as Ra) with the measurement area of 1 μm×1 μm is less than 1 nm, preferably less than 0.6 nm, more preferably less than 0.5 nm, still more preferably less than 0.4 nm. The maximum difference (P−V) with the measurement area of 1 μm×1 μm is less than 10 nm, preferably less than 9 nm, more preferably less than 8 nm, still more preferably less than 7 nm. The RMS roughness, Ra, and P−V can be measured with, for example, a scanning probe microscope SPA-500 manufactured by SII Nano Technology Inc.

(257) The electron movement is also inhibited, for example, in the case where the density of defect states is high in a region where a channel is formed. For example, in the case where the metal oxide **1432** contains oxygen vacancies (V_O), donor levels are formed by entry of hydrogen into sites of oxygen vacancies in some cases. A state in which hydrogen enters sites of oxygen vacancies is denoted by V_{OH} in the following description in some cases. V_{OH} is a factor of decreasing the on-state current of the transistor because V_{OH} scatters electrons. Note that sites of oxygen vacancies become more stable by entry of oxygen than by entry of hydrogen. Thus, by decreasing oxygen vacancies in the metal oxide **1432**, the on-state current of the transistor can be increased in some cases.

(258) For example, at a certain depth in the metal oxide **1432** or in a certain region of the metal oxide **1432**, the concentration of hydrogen measured by secondary ion mass spectrometry (SIMS) is set to be higher than or equal to $1×10^{16}$ atoms/cm^3 and lower than or equal to $2×10^{20}$ atoms/cm^3, preferably higher than or equal to $1×10^{16}$ atoms/cm^3 and lower than or equal to $5×10^{19}$ atoms/cm^3, more preferably higher than or equal to $1×10^{16}$ atoms/cm^3 and lower than or equal to $1×10^{19}$ atoms/cm^3, still more preferably higher than or equal to $1×10^{16}$ atoms/cm^3 and lower than or equal to $5×10^{18}$ atoms/cm^3.

(259) To decrease oxygen vacancies in the metal oxide **1432**, for example, there is a method in which excess oxygen contained in the insulating film **1404** is moved to the metal oxide **1432** through the metal oxide **1431**. In that case, the metal oxide **1431** is preferably a layer having an oxygen-transmitting property (a layer through which oxygen passes or is transmitted).

(260) Note that in the case where the transistor has an s-channel structure, a channel is formed in the entire metal oxide **1432**. Therefore, as the metal oxide **1432** has larger thickness, a channel region becomes larger. In other words, the thicker the metal oxide **1432** is, the larger the on-state current of the transistor is.

(261) Moreover, the thickness of the metal oxide **1433** is preferably as small as possible to increase the on-state current of the transistor. For example, the metal oxide **1433** may have a region with a thickness of less than 10 nm, preferably less than or equal to 5 nm, or more preferably less than or equal to 3 nm. Meanwhile, the metal oxide **1433** has a function of blocking entry of elements other than oxygen (such as hydrogen and silicon) included in the adjacent insulator into the metal oxide **1432** where a channel is formed. Thus, the metal oxide **1433** preferably has a certain thickness. For example, the metal oxide **1433** may have a region with a thickness of greater than or equal to 0.3 nm, preferably greater than or equal to 1 nm, more preferably greater than or equal to 2 nm. The metal oxide **1433** preferably has an oxygen blocking property to inhibit outward diffusion of oxygen released from the insulating film **1404** and the like.

(262) To improve reliability, the metal oxide **1431** is preferably thick and the metal oxide **1433** is preferably thin. For example, the metal oxide **1431** has a region with a thickness of greater than or equal to 10 nm, preferably greater than or equal to 20 nm, more preferably greater than or equal to 40 nm, still more preferably greater than or equal to 60 nm. An increase in the thickness of the metal oxide **1431** can increase the distance from the interface between the metal oxide **1431** and the adjacent insulator to the metal oxide **1432** where a channel is formed. Note that the metal oxide **1431** has a region with a thickness of, for example, less than or equal to 200 nm, preferably less than or equal to 120 nm, more preferably less than or equal to 80 nm, otherwise the productivity of the semiconductor device might be decreased.

(263) For example, a region in which the concentration of silicon is higher than or equal to $1×10^{16}$ atoms/cm^3 and lower than $1×10^{19}$ atoms/cm^3 is provided between the metal oxides **1432** and **1431**. The concentration of silicon is preferably higher than or equal to $1×10^{16}$ atoms/cm^3 and lower than $5×10^{18}$ atoms/cm^3, more preferably higher than or equal to $1×10^{16}$ atoms/cm^3 and lower than $2×10^{18}$ atoms/cm^3. A region in which the concentration of silicon is higher than or equal to $1×10^{16}$ atoms/cm^3 and lower than $1×10^{19}$ atoms/cm^3 is provided between the metal oxides **1432** and **1433**. The concentration of silicon is preferably higher than or equal to $1×10^{16}$ atoms/cm^3 and lower than $5×10^{18}$ atoms/cm^3, more preferably higher than or equal to $1×10^{16}$ atoms/cm^3 and lower than $2×10^{18}$ atoms/cm^3. The concentration of silicon can be measured by SIMS.

(264) It is preferable to reduce the concentration of hydrogen in the metal oxides **1431** and **1433** in order to reduce the concentration of hydrogen in the metal oxide **1432**. The metal oxides **1431** and **1433** each have a region in which the concentration of hydrogen is higher than or equal to $1×10^{16}$ atoms/cm^3 and lower than or equal to $2×10^{20}$ atoms/cm^3. The concentration of hydrogen is preferably higher than or equal to $1×10^{16}$ atoms/cm^3 and lower than or equal to $5×10^{19}$ atoms/cm^3, more preferably higher than or equal to $1×10^{16}$ atoms/cm^3 and lower than or equal to $1×10^{19}$ atoms/cm^3, still more preferably higher than or equal to $1×10^{16}$ atoms/cm^3 and lower than or equal to $5×10^{18}$ atoms/cm^3. The concentration of silicon can be measured by SIMS. It is also preferable to reduce the

concentration of nitrogen in the metal oxides **1431** and **1433** in order to reduce the concentration of nitrogen in the metal oxide **1432**. The metal oxides **1431** and **1433** each have a region in which the concentration of nitrogen is higher than or equal to 1×10^{16} atoms/cm^3 and lower than 5×10^{19} atoms/cm^3. The concentration of nitrogen is preferably higher than or equal to 1×10^{16} atoms/cm^3 and lower than or equal to 5×10^{18} atoms/cm^3, more preferably higher than or equal to 1×10^{16} atoms/cm^3 and lower than or equal to 1×10^{18} atoms/cm^3, still more preferably higher than or equal to 1×10^{16} atoms/cm^3 and lower than or equal to 5×10^{17} atoms/cm^3. The concentration of nitrogen can be measured by SIMS.

(265) The metal oxides **1431** to **1433** may be formed by a sputtering method, a chemical vapor deposition (CVD) method, a molecular beam epitaxy (MBE) method, a pulsed laser deposition (PLD) method, an atomic layer deposition (ALD) method, or the like.

(266) After the metal oxides **1431** and **1432** are formed, first heat treatment is preferably performed. The first heat treatment can be performed at a temperature higher than or equal to 250° C. and lower than or equal to 650° C., preferably higher than or equal to 450° C. and lower than or equal to 600° C., further preferably higher than or equal to 520° C. and lower than or equal to 570° C. The first heat treatment is performed in an inert gas atmosphere or an atmosphere containing an oxidizing gas at more than or equal to 10 ppm, more than or equal to 1%, or more than or equal to 10%. The first heat treatment may be performed under a reduced pressure. Alternatively, the first heat treatment may be performed in such a manner that heat treatment is performed in an inert gas atmosphere, and then another heat treatment is performed in an atmosphere containing an oxidizing gas at more than or equal to 10 ppm, more than or equal to 1%, or more than or equal to 10% in order to compensate for the desorbed oxygen. The crystallinity of the metal oxides **1431** and **1432** can be increased by the first heat treatment. Furthermore, impurities such as hydrogen and water can be removed by the first heat treatment.

(267) The above three-layer structure is an example. For example, a two-layer structure without the metal oxide **1431** or **1433** may be employed. Alternatively, any one of the semiconductors shown as examples of the metal oxides **1431** to **1433** may be provided over or under the metal oxide **1431** or over or under the metal oxide **1433**, i.e., a four-layer structure may be employed. Further alternatively, an n-layer structure (n is an integer of greater than or equal to 5) in which any one of the semiconductors shown as examples of the metal oxides **1431** to **1433** is provided at two or more of the following positions may be employed: over the metal oxide **1431**, under the metal oxide **1431**, over the metal oxide **1433**, and under the metal oxide **1433**.

(268) <Substrate>

(269) As the substrate **1450**, for example, an insulator substrate, a semiconductor substrate, or a conductor substrate may be used. As the insulator substrate, a glass substrate, a quartz substrate, a sapphire substrate, a stabilized zirconia substrate (e.g., an yttria-stabilized zirconia substrate), or a resin substrate is used, for example. Examples of the semiconductor substrate include a semiconductor substrate of silicon, germanium, or the like, and a compound semiconductor substrate of silicon carbide, silicon germanium, gallium arsenide, indium phosphide, zinc oxide, or gallium oxide. Another example of the semiconductor substrate is a silicon-on-insulator (SOI) substrate, where an insulator region is provided in the above semiconductor substrate. Examples of the conductor substrate include a graphite substrate, a metal substrate, an alloy substrate, and a conductive resin substrate. Other examples of the conductor substrate include a substrate including a metal nitride and a substrate including a metal oxide. Furthermore, an insulator substrate provided with a conductor or a semiconductor, a semiconductor substrate provided with a conductor or an insulator, a conductor substrate provided with a semiconductor or an insulator, or the like may be used. Alternatively, any of these substrates over which an element is provided may be used. As the element provided over the substrate, a capacitor, a resistor, a switching element, a light-emitting element, a memory element, or the like is used.

(270) A flexible substrate may be used as the substrate **1450**. Examples of a method for providing a transistor over a flexible substrate include fabricating the transistor over a non-flexible substrate, separating the transistor, and transferring the transistor to the substrate **1450** that is a flexible substrate. In that case, a separation layer is preferably provided between the non-flexible substrate and the transistor. As the substrate **1450**, a sheet, a film, or foil containing a fiber may be used. The substrate **1450** may have elasticity. The substrate **1450** may have a property of returning to its original shape when bending or pulling is stopped. Alternatively, the substrate **400** may have a property of not returning to its original shape. The thickness of the substrate **1450** is, for example, greater than or equal to 5 μm and less than or equal to 700 μm, preferably greater than or equal to 10 μm and less than or equal to 500 μm, more preferably greater than or equal to 15 μm and less than or equal to 300 μm. When the substrate **1450** is thin, the semiconductor device can be made lightweight. By making the substrate **1450** thin, the substrate **1450** may have elasticity or the property of returning to its original shape when bending or pulling is stopped, even when glass or the like is used as the substrate **1450**. This can alleviate an impact applied to the semiconductor device over the substrate **1450** which is caused by dropping or the like. That is, a durable semiconductor device can be provided.

(271) For the flexible substrate **1450**, metal, an alloy, a resin, glass, or fiber thereof can be used, for example. The flexible substrate **1450** preferably has a lower coefficient of linear expansion because deformation due to an environment is suppressed. The flexible substrate **1450** is preferably formed using, for example, a material whose coefficient of linear expansion is lower than or equal to 1×10^{-3}/K, lower than or equal to 5×10^{-5}/K, or lower than or equal to 1×10^{-5}/K. Examples of the resin include polyester, polyolefin, polyamide (e.g., nylon or aramid), polyimide, polycarbonate, acrylic, and polytetrafluoroethylene (PTFE). In particular, aramid is preferably used as the material of the flexible substrate **1450** because of its low coefficient of linear expansion.

Base Insulating Film

(272) The insulating film **1401** has a function of electrically isolating the substrate **1450** from the conductive film **1414**.

(273) The insulating film **1401** or **1402** is formed using an insulating film having a single-layer structure or a layered structure. Examples of the material of the insulating film include aluminum oxide, magnesium oxide, silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, and tantalum oxide.

(274) The insulating film **1402** may be formed using silicon oxide with high step coverage which is formed by reacting tetraethyl orthosilicate (TEOS), silane, or the like with oxygen, nitrous oxide, or the like.

(275) After the insulating film **1402** is formed, the insulating film **1402** may be subjected to planarization treatment using a CMP method or the like to improve the planarity of the top surface thereof.

(276) The insulating film **1404** preferably contains an oxide. In particular, the insulating film **1404** preferably contains an oxide material that releases some of its oxygen by heating. The insulating film **1404** preferably contains an oxide containing oxygen more than that in the stoichiometric composition. An oxide film containing more oxygen than that in the stoichiometric composition releases some of its oxygen by heating. Oxygen released from the insulating film **1404** is supplied to the metal oxide **1430**, so that oxygen vacancies in the metal oxide **1430** can be reduced. Consequently, changes in the electrical characteristics of the transistor can be reduced and the reliability of the transistor can be improved.

(277) The oxide film containing more oxygen than that in the stoichiometric composition is an oxide film in which the amount of released oxygen converted into oxygen atoms is greater than or equal to 1.0×10^{18} atoms/cm^3, preferably greater than or equal to 3.0×10^{20} atoms/cm^3 in thermal desorption spectroscopy (TDS) analysis, for example. Note that the temperature of the film surface in the TDS analysis is preferably higher than or equal to 100° C. and lower than or equal to 700° C., or higher than or equal to 100° C. and lower than or equal to 500° C.

(278) The insulating film **1404** preferably contains an oxide that can supply oxygen to the metal oxide **1430**. For example, a material containing silicon oxide or silicon oxynitride is preferably used.

(279) Alternatively, a metal oxide such as aluminum oxide, aluminum oxynitride, gallium oxide, gallium oxynitride, yttrium oxide, yttrium oxynitride, hafnium oxide, or hafnium oxynitride may be used for the insulating film **1404**.

(280) To make the insulating film **1404** contain excess oxygen, the insulating film **1404** may be formed in an oxygen atmosphere, for example.

Alternatively, a region containing excess oxygen may be formed by introducing oxygen into the insulating film **1404** that has been formed. These two methods may be combined.

(281) For example, oxygen (at least including any of oxygen radicals, oxygen atoms, and oxygen ions) may be introduced into the insulating film **1404** that has been formed, so that a region containing excess oxygen is formed. Oxygen can be introduced by an ion implantation method, an ion doping method, a plasma immersion ion implantation method, plasma treatment, or the like.

(282) A gas containing oxygen can be used for oxygen introducing treatment. As the gas containing oxygen, oxygen, nitrous oxide, nitrogen dioxide, carbon dioxide, carbon monoxide, and the like can be used. Further, a rare gas may be included in the gas containing oxygen for the oxygen introduction treatment. Moreover, hydrogen or the like may be included. For example, a mixed gas of carbon dioxide, hydrogen, and argon may be used.

(283) After the insulating film **1404** is formed, the insulating film **1404** may be subjected to planarization treatment using a CMP method or the like to improve the planarity of the top surface thereof.

(284) The insulating film **1403** has a passivation function of preventing oxygen contained in the insulating film **1404** from decreasing by bonding to metal contained in the conductive film **1414**.

(285) The insulating film **1403** has a function of blocking oxygen, hydrogen, water, alkali metal, alkaline earth metal, and the like. Providing the insulating film **1403** can prevent outward diffusion of oxygen from the metal oxide **1430** and entry of hydrogen, water, or the like into the metal oxide **1430** from the outside.

(286) The insulating film **1403** can be, for example, a nitride insulating film. The nitride insulating film is formed using silicon nitride, silicon nitride oxide, aluminum nitride, aluminum nitride oxide, or the like. Note that instead of the nitride insulating film, an oxide insulating film having a blocking effect against oxygen, hydrogen, water, and the like, may be provided. The oxide insulating film is formed using aluminum oxide, aluminum oxynitride, gallium oxide, gallium oxynitride, yttrium oxide, yttrium oxynitride, hafnium oxide, and hafnium oxynitride.

(287) The threshold voltage of the transistor **1400***a* can be controlled by injecting electrons into a charge trap layer. The charge trap layer is preferably provided in the insulating film **1402** or the insulating film **1403**. For example, when the insulating film **1403** is formed using hafnium oxide, aluminum oxide, tantalum oxide, aluminum silicate, or the like, the insulating film **1403** can function as a charge trap layer.

(288) <<Gate Electrode>>

(289) The conductive films **1411** to **1414** each preferably have a single-layer structure or a layered structure of a conductive film containing a low-resistance material selected from copper (Cu), tungsten (W), molybdenum (Mo), gold (Au), aluminum (Al), manganese (Mn), titanium (Ti), tantalum (Ta), nickel (Ni), chromium (Cr), lead (Pb), tin (Sn), iron (Fe), cobalt (Co), ruthenium (Ru), platinum (Pt), iridium (Ir), or strontium (Sr), an alloy of such a low-resistance material, or a compound containing such a material as its main component. It is particularly preferable to use a high-melting-point material that has both heat resistance and conductivity, such as tungsten or molybdenum. In addition, the conductive layers are preferably formed using a low-resistance conductive material such as aluminum or copper. The conductive layers are preferably formed using a Cu—Mn alloy, since in that case, manganese oxide formed at the interface with an insulator containing oxygen has a function of preventing Cu diffusion.

(290) <<Source Electrode and Drain Electrode>>

(291) The conductive films **1421** to **1424** each preferably have a single-layer structure or a layered structure of a conductive film containing a low-resistance material selected from copper (Cu), tungsten (W), molybdenum (Mo), gold (Au), aluminum (Al), manganese (Mn), titanium (Ti), tantalum (Ta), nickel (Ni), chromium (Cr), lead (Pb), tin (Sn), iron (Fe), cobalt (Co), ruthenium (Ru), platinum (Pt), iridium (Ir), and strontium (Sr), an alloy of such a low-resistance material, or a compound containing such a material as its main component. It is particularly preferable to use a high-melting-point material that has both heat resistance and conductivity, such as tungsten or molybdenum. In addition, the conductive layers are preferably formed using a low-resistance conductive material such as aluminum or copper. The conductive layers are preferably formed using a Cu—Mn alloy, since in that case, manganese oxide formed at the interface with an insulator containing oxygen has a function of preventing Cu diffusion.

(292) The conductive films **1421** to **1424** are preferably formed using a conductive oxide including noble metal, such as iridium oxide, ruthenium oxide, or strontium ruthenate. Such a conductive oxide hardly takes oxygen from an oxide semiconductor even when it is in contact with the oxide semiconductor and hardly generates oxygen vacancies in the oxide semiconductor.

(293) <Low-Resistance Region>

(294) The regions **1441** and **1442** are formed when, for example, the conductive films **1421** and **1423** take oxygen from the metal oxides **1431** and **1432**. Oxygen is more likely to be extracted at a higher temperature. Oxygen vacancies are formed in the regions **1441** and **1442** through several heating steps in the manufacturing process of the transistor. In addition, hydrogen enters sites of the oxygen vacancies by heating, increasing the carrier concentration in the regions **1441** and **1442**. As a result, the resistance of the regions **1441** and **1442** is reduced.

(295) <<Gate Insulating Film>>

(296) The insulating film **1406** preferably contains an insulator with a high relative dielectric constant. For example, the insulating film **1406** preferably contains gallium oxide, hafnium oxide, an oxide containing aluminum and hafnium, an oxynitride containing aluminum and hafnium, an oxide containing silicon and hafnium, or an oxynitride containing silicon and hafnium.

(297) The insulating film **1406** preferably has a layered structure containing silicon oxide or silicon oxynitride and an insulator with a high relative dielectric constant. Because silicon oxide and silicon oxynitride have thermal stability, combination of silicon oxide or silicon oxynitride with an insulator with a high relative dielectric constant allows the layered structure to be thermally stable and have a high relative dielectric constant. For example, when aluminum oxide, gallium oxide, or hafnium oxide is closer to the metal oxide **1433**, entry of silicon from silicon oxide or silicon oxynitride into the metal oxide **1432** can be suppressed.

(298) When silicon oxide or silicon oxynitride is closer to the metal oxide **1433**, for example, trap centers might be formed at the interface between aluminum oxide, gallium oxide, or hafnium oxide and silicon oxide or silicon oxynitride. The trap centers can shift the threshold voltage of the transistor in the positive direction by trapping electrons in some cases.

(299) <<Interlayer Insulating Film and Protective Insulating Film>>

(300) The insulating film **1405** preferably contains an insulator with a low relative dielectric constant. For example, the insulating film **1405** preferably contains silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, or a resin. Alternatively, the insulating film **1405** preferably has a layered structure containing silicon oxide or silicon oxynitride and a resin. Because silicon oxide and silicon oxynitride have thermal stability, combination of silicon oxide or silicon oxynitride with a resin allows the layered structure to be thermally stable and have a low relative dielectric constant. Examples of the resin include polyester, polyolefin, polyamide (e.g., nylon or aramid), polyimide, polycarbonate, and acrylic.

(301) The insulating film **1407** has a function of blocking oxygen, hydrogen, water, alkali metal, alkaline earth metal, and the like. Providing the insulating film **1407** can prevent outward diffusion of oxygen from the metal oxide **1430** and entry of hydrogen, water, or the like into the metal oxide **1430** from the outside.

(302) The insulating film **1407** can be, for example, a nitride insulating film. The nitride insulating film is formed using silicon nitride, silicon nitride oxide, aluminum nitride, aluminum nitride oxide, or the like. Note that instead of the nitride insulating film, an oxide insulating film having a blocking effect against oxygen, hydrogen, water, and the like, may be provided. The oxide insulating film is formed using aluminum oxide, aluminum oxynitride, gallium oxide, gallium oxynitride, yttrium oxide, yttrium oxynitride, hafnium oxide, and hafnium oxynitride.

(303) An aluminum oxide film is preferably used as the insulating film **1407** because it is highly effective in preventing transmission of both oxygen and impurities such as hydrogen and moisture.

(304) When the insulating film **1407** is formed by a method using plasma containing oxygen, e.g., by a sputtering method or a CVD method, oxygen

can be added to side and top surfaces of the insulating films **1405** and **1406**. It is preferable to perform second heat treatment at any time after the formation of the insulating film **1407**. Through the second heat treatment, oxygen added to the insulating films **1405** and **1406** is diffused in the insulating films to reach the metal oxide **1430**, whereby oxygen vacancies in the metal oxide **1430** can be reduced.

(305) In schematic views of FIGS. **21**A and **21**B, oxygen added to the insulating films **1405** and **1406** during the formation of the insulating film **1407** is diffused in the insulating films through the second heat treatment and reaches the metal oxide **1430**. In FIG. **21**A, oxygen diffused in the cross-sectional diagram of FIG. **19**B is indicated by arrows. Similarly, in FIG. **21**B, oxygen diffused in the cross-sectional diagram of FIG. **19**C is indicated by arrows.

(306) As shown in FIGS. **21**A and **21**B, oxygen added to the side surface of the insulating film **1406** is diffused in the insulating film **1406** and reaches the metal oxide **1430**. In addition, a region **1461**, a region **1462**, and a region **1463** each containing excess oxygen may be formed in the vicinity of the interface between the insulating films **1407** and **1405**. Oxygen contained in the regions **1461** to **1463** reaches the metal oxide **1430** through the insulating films **1405** and **1404**. In the case where the insulating film **1405** includes silicon oxide and the insulating film **1407** includes aluminum oxide, a mixed layer of silicon, aluminum, and oxygen is formed in the regions **1461** to **1463** in some cases.

(307) The insulating film **1407** has a function of blocking oxygen and prevents oxygen from being diffused upward across the insulating film **1407**. The insulating film **1403** also has a function of blocking oxygen and prevents oxygen from being diffused downward across the insulating film **1403**.

(308) Note that the second heat treatment may be performed at a temperature that allows oxygen added to the insulating films **1405** and **1406** to be diffused to the metal oxide **1430**. For example, the description of the first heat treatment may be referred to for the second heat treatment. Alternatively, the temperature of the second heat treatment is preferably lower than that of the first heat treatment. The second heat treatment is performed at a temperature lower than that of the first heat treatment by higher than or equal to 20° C. and lower than or equal to 150° C., preferably higher than or equal to 40° C. and lower than or equal to 100° C. Accordingly, superfluous release of oxygen from the insulating film **1404** can be inhibited. Note that the second heat treatment is not necessarily performed when heating during formation of the films can work as heat treatment comparable to the second heat treatment.

(309) As described above, oxygen can be supplied to the metal oxide **1430** from above and below through the formation of the insulating film **1407** and the second heat treatment.

(310) Alternatively, oxygen may be added to the insulating films **1405** and **1406** by forming a film containing indium oxide, e.g., an In-M-Zn oxide, as the insulating film **1407**.

(311) The insulating film **1408** can be formed using an insulator including one or more kinds of materials selected from aluminum oxide, aluminum nitride oxide, magnesium oxide, silicon oxide, silicon oxynitride, silicon nitride oxide, silicon nitride, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, tantalum oxide, and the like. Alternatively, for the insulating film **1408**, a resin such as a polyimide resin, a polyamide resin, an acrylic resin, a siloxane resin, an epoxy resin, or a phenol resin can be used. The insulating film **1408** may be a stack including any of the above materials.

Structure Example 2 of Transistor

(312) The conductive film **1414** and the insulating films **1402** and **1403** can be omitted in the transistor **1400***a* shown in FIGS. **19**A to **19**C. An example of such a structure is shown in FIGS. **22**A to **22**C.

(313) FIGS. **22**A to **22**C are a top view and cross-sectional diagrams of a transistor **1400***b*. FIG. **22**A is a top view. FIG. **22**B is a cross-sectional diagram taken along dashed-dotted line A**1**-A**2** in FIG. **22**A and FIG. **22**C is a cross-sectional diagram taken along dashed-dotted line A**3**-A**4** in FIG. **22**A. Note that for simplification of the drawing, some components are not illustrated in the top view in FIG. **22**A. Note that the dashed-dotted line A**1**-A**2** and the dashed-dotted line A**3**-A**4** are sometimes referred to as a channel length direction of the transistor **1400***b* and a channel width direction of the transistor **1400***b*, respectively.

(314) In the transistor **1400***a* shown in FIGS. **19**A to **19**C, parts of the conductive films **1421** and **1423** that overlap with the gate electrode (the conductive films **1411** to **1413**) can be reduced in thickness. An example of such a structure is shown in FIGS. **23**A to **23**C.

(315) FIGS. **23**A to **23**C are a top view and cross-sectional diagrams of a transistor **1400***c*. FIG. **23**A is a top view. FIG. **23**B is a cross-sectional diagram taken along dashed-dotted line A**1**-A**2** in FIG. **23**A and FIG. **23**C is a cross-sectional diagram taken along dashed-dotted line A**3**-A**4** in FIG. **23**A. Note that for simplification of the drawing, some components are not illustrated in the top view in FIG. **23**A. Note that the dashed-dotted line A**1**-A**2** and the dashed-dotted line A**3**-A**4** are sometimes referred to as a channel length direction of the transistor **1400***c* and a channel width direction of the transistor **1400***c*, respectively.

(316) In the transistor **1400***c* shown in FIG. **23**B, part of the conductive film **1421** that overlaps with the gate electrode is reduced in thickness, and the conductive film **1422** covers the conductive film **1421**. Part of the conductive film **1423** that overlaps with the gate electrode is also reduced in thickness, and the conductive film **1424** covers the conductive film **1423**.

(317) The transistor **1400***c*, which has the structure shown in FIG. **23**B, can have an increased distance between the gate and source electrodes or between the gate and drain electrodes. This results in a reduction in the parasitic capacitance formed between the gate electrode and the source and drain electrodes. As a result, a transistor capable of high-speed operation can be obtained.

Structure Example 3 of Transistor

(318) In the transistor **1400***c* shown in FIGS. **23**A to **23**C, the width of the metal oxides **1431** and **1432** can be increased in the A**3**-A**4** direction. An example of such a structure is illustrated in FIGS. **24**A to **24**C.

(319) FIGS. **24**A to **24**C are a top view and cross-sectional diagrams of a transistor **1400***d*. FIG. **24**A is the top view. FIG. **24**B is a cross-sectional diagram taken along dashed-dotted line A**1**-A**2** in FIG. **24**A, and FIG. **24**C is a cross-sectional diagram taken along dashed-dotted line A**3**-A**4** in FIG. **24**A. Note that for simplification of the drawing, some components in the top view in FIG. **24**A are not illustrated. Note that the dashed-dotted line A**1**-A**2** and the dashed-dotted line A**3**-A**4** are sometimes referred to as a channel length direction of the transistor **1400***d* and a channel width direction of the transistor **1400***d*, respectively.

(320) The transistor **1400***d*, which has the structure shown in FIGS. **24**A to **24**C, can have an increased on-state current.

Structure Example 4 of Transistor

(321) In the transistor **1400***c* shown in FIGS. **23**A to **23**C, a plurality of regions (fins) consisting of the metal oxides **1431** and **1432** may be provided in the A**3**-A**4** direction. An example of such a structure is illustrated in FIGS. **25**A to **25**C.

(322) FIGS. **25**A to **25**C are a top view and cross-sectional diagrams of a transistor **1400***e*. FIG. **25**A is the top view. FIG. **25**B is a cross-sectional diagram taken along dashed-dotted line A**1**-A**2** in FIG. **25**A, and FIG. **25**C is a cross-sectional diagram taken along dashed-dotted line A**3**-A**4** in FIG. **25**A. Note that for simplification of the drawing, some components in the top view in FIG. **25**A are not illustrated. Note that the dashed-dotted line A**1**-A**2** and the dashed-dotted line A**3**-A**4** are sometimes referred to as a channel length direction of the transistor **1400***e* and a channel width direction of the transistor **1400***e*, respectively.

(323) The transistor **1400***e* includes a first fin consisting of metal oxides **1431***a* and **1432***a*, a second fin consisting of metal oxides **1431***b* and **1432***b*, and a third fin consisting of metal oxides **1431***c* and **1432***c*.

(324) In the transistor **1400***e*, the metal oxides **1432***a* to **1432***c* where a channel is formed are surrounded by the gate electrode. Hence, the gate electric field can be applied to the entire channel, so that a transistor with a high on-state current can be obtained.

Structure Example 5 of Transistor

(325) FIGS. **26**A to **26**D are a top view and cross-sectional diagrams of a transistor **1400***f*. FIG. **26**A is a top view of the transistor **1400***f*. FIG. **26**B is a cross-sectional diagram taken along dashed-dotted line A**1**-A**2** in FIG. **26**A and FIG. **26**C is a cross-sectional diagram taken along dashed-dotted

line A**3**-A**4** in FIG. **26**A. Note that the dashed-dotted line A**1**-A**2** and the dashed-dotted line A**3**-A**4** are sometimes referred to as a channel length direction and a channel width direction, respectively. The transistor **1400***f* has the s-channel structure like the transistor **1400***a* and the like. In the transistor **1400***f*, an insulating film **1409** is provided in contact with the side surface of the conductive film **1412** used as a gate electrode. The insulating film **1409** and the conductive film **1412** are covered with the insulating film **1408**. The insulating film **1409** serves as a sidewall insulating film of the transistor **1400***f*. As in the transistor **1400***a*, the gate electrode may be a stack of the conductive films **1411** to **1413**.

(326) The insulating film **1406** and the conductive film **1412** overlap with the conductive film **1414** and the metal oxide **1432** at least partly. The side edge of the conductive film **1412** in the channel length direction is preferably approximately aligned with the side edge of the insulating film **1406** in the channel length direction. Here, the insulating film **1406** serves as a gate insulating film of the transistor **1400***f*, the conductive film **1412** serves as a gate electrode of the transistor **1400***f*, and the insulating film **1409** serves as a sidewall insulating film of the transistor **1400***f*.

(327) The metal oxide **1432** has a region that overlaps with the conductive film **1412** with the metal oxide **1433** and the insulating film **1406** positioned therebetween. Preferably, the outer edge of the metal oxide **1431** is approximately aligned with the outer edge of the metal oxide **1432**, and the outer edge of the metal oxide **1433** is positioned outward from the outer edges of the metal oxides **1431** and **1432**. However, the shape of the transistor in this embodiment is not limited to that where the outer edge of the metal oxide **1433** is positioned outward from the outer edge of the metal oxide **1431**. For example, the outer edge of the metal oxide **1431** may be positioned outward from the outer edge of the metal oxide **1433**, or the side edge of the metal oxide **1431** may be approximately aligned with the side edge of the metal oxide **1433**.

(328) FIG. **26**D is an enlarged view of part of FIG. **26**B. As shown in FIG. **26**D, regions **1461***a* to **1461***e* are formed in the metal oxide **1430**. The regions **1461***b* to **1461***e* have a higher dopant concentration and therefore have a lower resistance than the region **1461***a*. Furthermore, the regions **1461***b* and **1461***c* have a higher concentration of hydrogen and therefore have a much lower resistance than the regions **1461***d* and **1461***e*. The concentration of a dopant in the region **1461***a* is, for example, less than or equal to 5%, less than or equal to 2%, or less than or equal to 1% of the maximum concentration of a dopant in the region **1461***b* or **1461***c*. Note that the dopant may be rephrased as a donor, an acceptor, an impurity, or an element.

(329) As shown in FIG. **26**D, in the metal oxide **1430**, the region **1461***a* substantially overlaps with the conductive film **1412**, and the regions **1461***b* to **1461***e* are the regions other than the region **1461***a*. In the regions **1461***b* and **1461***c*, the top surface of metal oxide **1433** is in contact with the insulating film **1407**. In the regions **1461***d* and **1461***e*, the top surface of the metal oxide **1433** is in contact with the insulating film **1409** or **1406**. That is, as shown in FIG. **26**D, the border between the regions **1461***b* and **1461***d* overlaps with the border between the side edges of the insulating films **1407** and **1409**. The same applies to the border between the regions **1461***c* and **1461***e*. Here, part of the regions **1461***d* and **1461***e* preferably overlaps with part of a region (a channel formation region) where the metal oxide **1432** and the conductive film **1412** overlap with each other. For example, the side edges of the regions **1461***d* and **1461***e* in the channel length direction are preferably positioned inward from the side edge of the conductive film **1412** by a distance d. In that case, the thickness **1406** of the insulating film **1406** and the distanced preferably satisfy 0.25t.sub.406<d<t.sub.406.

(330) In the above manner, the regions **1461***d* and **1461***e* are formed in part of the region where the metal oxide **1430** and the conductive film **1412** overlap with each other. Accordingly, the channel formation region of the transistor **1400***f* is in contact with the low-resistance regions **1461***d* and **1461***e* and a high-resistance offset region is not formed between the region **1461***a* and each of the regions **1461***d* and **1461***e*, so that the on-state current of the transistor **1400***f* can be increased. Furthermore, since the side edges of the regions **1461***d* and **1461***e* in the channel length direction are formed so as to satisfy the above range, the regions **1461***d* and **1461***e* can be prevented from spreading inward too much in the channel formation region and thus the transistor **1400***f* can be prevented from being constantly in an on state.

(331) The regions **1461***b* to **1461***e* are formed by ion doping treatment such as an ion implantation method. Therefore, as shown in FIG. **26**D, the positions of the side edges of the regions **1461***d* and **1461***e* in the channel length direction are sometimes shifted closer to the side edge of the metal oxide **1430** in a channel length direction, in areas where the regions **1461***d* and **1461***e* are farther from the top surface of the metal oxide **1433**. The distanced in this case is the distance between the side edge of the conductive film **1412** in the channel length direction and each of the side edges of the regions **1461***d* and **1461***e* that are closest to the inner part of the conductive film **1412**.

(332) In this case, for example, the regions **1461***d* and **1461***e* in the metal oxide **1431** do not not overlap with the conductive film **1412** in some cases. In that case, at least part of the regions **1461***d* and **1461***e* in the metal oxide **1431** or **1432** is preferably formed in a region overlapping with the conductive film **1412**.

(333) In addition, low-resistance regions **1451** and **1452** are preferably formed in the metal oxide **1431**, the metal oxide **1432**, and the metal oxide **1433** in the vicinity of the interface with the insulating film **1407**. The low-resistance regions **1451** and **1452** contain at least one of elements included in the insulating film **1407**. Preferably, part of the low-resistance regions **1451** and **1452** is substantially in contact with or overlaps partly with the region (the channel formation region) where the metal oxide **1432** and the conductive film **1412** overlap with each other.

(334) Since a large part of the metal oxide **1433** is in contact with the insulating film **1407**, the low-resistance regions **1451** and **1452** are likely to be formed in the metal oxide **1433**. The low-resistance regions **1451** and **1452** in the metal oxide **1433** contain a higher concentration of elements included in the insulating film **1407** than the other regions of the metal oxide **1433** (e.g., the region of the metal oxide **1433** that overlaps with the conductive film **1412**).

(335) The low-resistance regions **1451** and **1452** are formed in the regions **1461***b* and **1461***c*, respectively. Ideally, the metal oxide **1430** has a structure in which the concentration of added elements is the highest in the low-resistance regions **1451** and **1452**, the second highest in the regions **1461***b* and **1461***c* to **1461***e* other than the low-resistance regions **1451** and **1452**, and the lowest in the region **1461***a*. The added elements refer to a dopant for forming the regions **1461***b* and **1461***c* and an element added from the insulating film **1407** to the low-resistance regions **1451** and **1452**.

(336) Although the low-resistance regions **1451** and **1452** are formed in the transistor **1400***f*, the semiconductor device shown in this embodiment is not limited to this structure. For example, the low-resistance regions **1451** and **1452** need not be formed in the case where the regions **1461***b* and **1461***c* have a sufficiently low resistance.

Structure Example 6 of Transistor

(337) FIGS. **27**A and **27**B are a top view and a cross-sectional diagrams of a transistor **1680**. FIG. **27**A is a top view, and FIG. **27**B is a cross-sectional diagram taken along dashed-dotted line A-B in FIG. **27**A. Note that for simplification of the drawing, some components are increased or reduced in size, or omitted in FIGS. **27**A and **27**B. The direction of the dashed-dotted line A-B may be referred to as a channel length direction.

(338) The transistor **1680** shown in FIG. **27**B includes a conductive film **1689** serving as a first gate, a conductive film **1688** serving as a second gate, a semiconductor **1682**, a conductive film **1683** and a conductive film **1684** serving as a source and a drain, an insulating film **1681**, an insulating film **1685**, an insulating film **1686**, and an insulating film **1687**.

(339) The conductive film **1689** is on an insulating surface. The conductive film **1689** overlaps with the semiconductor **1682** with the insulating film **1681** provided therebetween. The conductive film **1688** overlaps with the semiconductor **1682** with the insulating films **1685**, **1686**, and **1687** provided therebetween. The conductive films **1683** and **1684** are connected to the semiconductor **1682**.

(340) The description of the conductive films **1411** to **1414** in FIGS. **19**A to **19**C can be referred to for the details of the conductive films **1689** and **1688**.

(341) The conductive films **1689** and **1688** may be supplied with different potentials, or may be supplied with the same potential at the same time. The conductive film **1688** serving as a second gate electrode in the transistor **1680** leads to stabilization of the threshold voltage. Note that the conductive film **1688** may be omitted in some cases.

(342) The description of the metal oxide **1432** in FIGS. **19**A to **19**C can be referred to for the details of the semiconductor **1682**. The semiconductor

1682 may be a single layer or a stack including a plurality of semiconductor layers.

(343) The description of the conductive films **1421** to **1424** in FIGS. **19**A to **19**C can be referred to for the details of the conductive films **1683** and **1684**.

(344) The description of the insulating film **1406** in FIGS. **19**A to **19**C can be referred to for the details of the insulating film **1681**.

(345) The insulating films **1685** to **1687** are sequentially stacked over the semiconductor **1682** and the conductive films **1683** and **1684** in FIG. **27**B; however, an insulating film provided over the semiconductor **1682** and the conductive films **1683** and **1684** may be a single layer or a stack including a plurality of insulating films.

(346) In the case of using an oxide semiconductor as the semiconductor **1682**, the insulating film **1686** preferably contains oxygen at a proportion higher than or equal to that in the stoichiometric composition and preferably has a function of supplying part of oxygen to the semiconductor **1682** by heating. Note that in the case where the provision of the insulating film **1686** directly on the semiconductor **1682** causes damage to the semiconductor **1682** at the time of formation of the insulating film **1686**, the insulating film **1685** is preferably provided between the semiconductor **1682** and the insulating film **1686**, as shown in FIG. **27**B. The insulating film **1685** preferably allows oxygen to pass therethrough, and preferably causes little damage to the semiconductor **1682** when the insulating film **1685** is formed compared with the case of the insulating film **1686**. If the insulating film **1686** can be formed directly on the semiconductor **1682** while keeping the damage to the semiconductor **1682** small, the insulating film **1685** is not necessarily provided.

(347) For the insulating films **1685** and **1686**, a material containing silicon oxide or silicon oxynitride is preferably used, for example. Alternatively, a metal oxide such as aluminum oxide, aluminum oxynitride, gallium oxide, gallium oxynitride, yttrium oxide, yttrium oxynitride, hafnium oxide, or hafnium oxynitride can be used.

(348) The insulating film **1687** preferably has an effect of blocking diffusion of oxygen, hydrogen, and water. Alternatively, the insulating film **1687** preferably has an effect of blocking diffusion of hydrogen and water.

(349) An insulating film that has a higher density or that has fewer dangling bonds and is more chemically stable exhibits superior blocking effect. An insulating film that has an effect of blocking diffusion of oxygen, hydrogen, and water can be formed using, for example, aluminum oxide, aluminum oxynitride, gallium oxide, gallium oxynitride, yttrium oxide, yttrium oxynitride, hafnium oxide, or hafnium oxynitride. An insulating film that has an effect of blocking diffusion of hydrogen and water can be formed using, for example, silicon nitride or silicon nitride oxide.

(350) In the case where the insulating film **1687** has an effect of blocking diffusion of water, hydrogen, and the like, impurities such as water and hydrogen that exist in a resin in a panel or exist outside the panel can be prevented from entering the semiconductor **1682**. In the case where an oxide semiconductor is used as the semiconductor **1682**, part of water or hydrogen that enters the oxide semiconductor serves as an electron donor (donor). Thus, the use of the insulating film **1687** having the blocking effect can prevent a shift in the threshold voltage of the transistor **1680** due to the generation of donors.

(351) In addition, in the case where an oxide semiconductor is used as the semiconductor **1682**, the effect of insulating film **1687** to block the diffusion of oxygen prevents oxygen from the oxide semiconductor to diffuse to the outside. Accordingly, oxygen vacancies in the oxide semiconductor that serve as donors are reduced, so that a shift in the threshold voltage of the transistor **1680** due to generation of donors can be prevented.

(352) Note that this embodiment can be combined with any of the other embodiments in this specification as appropriate.

EMBODIMENT 5

(353) Described in this embodiment are structures of an oxide semiconductor film capable of being used for the OS transistors described in the above embodiments.

(354) <Structure of Oxide Semiconductor>

(355) An oxide semiconductor is classified into a single crystal oxide semiconductor and a non-single-crystal oxide semiconductor. Examples of a non-single-crystal oxide semiconductor include a c-axis-aligned and a-b-plane anchored crystalline oxide semiconductor (CAAC-OS), a polycrystalline oxide semiconductor, a nanocrystalline oxide semiconductor (nc-OS), an amorphous-like oxide semiconductor (a-like OS), and an amorphous oxide semiconductor.

(356) From another perspective, an oxide semiconductor is classified into an amorphous oxide semiconductor and a crystalline oxide semiconductor. Examples of a crystalline oxide semiconductor include a single crystal oxide semiconductor, a CAAC-OS, a polycrystalline oxide semiconductor, and an nc-OS.

(357) An amorphous structure is generally thought to be isotropic and have no non-uniform structure, to be metastable and not to have fixed positions of atoms, to have a flexible bond angle, and to have a short-range order but have no long-range order, for example.

(358) This means that a stable oxide semiconductor cannot be regarded as a completely amorphous oxide semiconductor. Moreover, an oxide semiconductor that is not isotropic (e.g., an oxide semiconductor that has a periodic structure in a microscopic region) cannot be regarded as a completely amorphous oxide semiconductor. In contrast, an a-like OS, which is not isotropic, has an unstable structure that contains a void. Because of its instability, an a-like OS is close to an amorphous oxide semiconductor in terms of physical properties.

(359) <CAAC-OS>

(360) First, a CAAC-OS will be described.

(361) A CAAC-OS is one of oxide semiconductors having a plurality of c-axis aligned crystal parts (also referred to as pellets).

(362) Analysis of a CAAC-OS by X-ray diffraction (XRD) is described. For example, when the structure of a CAAC-OS including an InGaZnO.sub.4 crystal that is classified into the space group R-**3***m* is analyzed by an out-of-plane method, a peak appears at a diffraction angle (2θ) of around 31° as shown in FIG. **28**A. This peak is derived from the (009) plane of the InGaZnO.sub.4 crystal, which indicates that crystals in the CAAC-OS have c-axis alignment, and that the c-axes are aligned in a direction substantially perpendicular to a surface over which the CAAC-OS film is formed (also referred to as a formation surface) or the top surface of the CAAC-OS film. Note that a peak sometimes appears at a 2θ of around 36° in addition to the peak at a 2θ of around 31°. The peak at a 2θ of around 36° is derived from a crystal structure classified into the space group Fd-3m. Therefore, it is preferred that the CAAC-OS do not show the peak at a 2θ of around 36°.

(363) On the other hand, in structural analysis of the CAAC-OS by an in-plane method in which an X-ray is incident on the CAAC-OS in a direction parallel to the formation surface, a peak appears at a 2θ of around 56°. This peak is attributed to the (110) plane of the InGaZnO.sub.4 crystal. When analysis (φ scan) is performed with 2θ fixed at around 56° and with the sample rotated using a normal vector to the sample surface as an axis (φ axis), as shown in FIG. **28**B, a peak is not clearly observed. In contrast, in the case where single crystal InGaZnO.sub.4 is subjected to φ scan with 2θ fixed at around 56°, as shown in FIG. **28**C, six peaks which are derived from crystal planes equivalent to the (110) plane are observed. Accordingly, the structural analysis using XRD shows that the directions of a-axes and b-axes are irregularly oriented in the CAAC-OS.

(364) Next, a CAAC-OS analyzed by electron diffraction will be described. For example, when an electron beam with a probe diameter of 300 nm is incident on a CAAC-OS including an InGaZnO.sub.4 crystal in a direction parallel to the formation surface of the CAAC-OS, a diffraction pattern (also referred to as a selected-area electron diffraction pattern) shown in FIG. **28**D can be obtained. In this diffraction pattern, spots derived from the (009) plane of an InGaZnO.sub.4 crystal are included. Thus, the electron diffraction also indicates that pellets included in the CAAC-OS have c-axis alignment and that the c-axes are aligned in a direction substantially perpendicular to the formation surface or the top surface of the CAAC-OS. Meanwhile, FIG. **28**E shows a diffraction pattern obtained in such a manner that an electron beam with a probe diameter of 300 nm is incident on the same sample in a direction perpendicular to the sample surface. As shown in FIG. **28**E, a ring-like diffraction pattern is observed. Thus, the electron diffraction using an electron beam with a probe diameter of 300 nm also indicates that the a-axes and b-axes of the pellets included in the CAAC-OS

do not have regular orientation. The first ring in FIG. **28**E is considered to be derived from the (010) plane, the (100) plane, and the like of the InGaZnO.sub.4 crystal. The second ring in FIG. **28**E is considered to be derived from the (110) plane and the like.

(365) In a combined analysis image (also referred to as a high-resolution TEM image) of a bright-field image and a diffraction pattern of a CAAC-OS, which is obtained using a transmission electron microscope (TEM), a plurality of pellets can be observed. However, even in the high-resolution TEM image, a boundary between pellets, that is, a crystal grain boundary is not clearly observed in some cases. Thus, in the CAAC-OS, a reduction in electron mobility due to the grain boundary is less likely to occur.

(366) FIG. **29**A shows a high-resolution TEM image of a cross section of the CAAC-OS which is observed from a direction substantially parallel to the sample surface. The high-resolution TEM image is obtained with a spherical aberration corrector function. The high-resolution TEM image obtained with a spherical aberration corrector function is particularly referred to as a Cs-corrected high-resolution TEM image. The Cs-corrected high-resolution TEM image can be observed with, for example, an atomic resolution analytical electron microscope JEM-ARM 200F manufactured by JEOL Ltd.

(367) FIG. **29**A shows pellets in which metal atoms are arranged in a layered manner. FIG. **47**A proves that the size of a pellet is greater than or equal to 1 nm or greater than or equal to 3 nm. Therefore, the pellet can also be referred to as a nanocrystal (nc). Furthermore, the CAAC-OS can also be referred to as an oxide semiconductor including c-axis aligned nanocrystals (CANC). A pellet reflects unevenness of a formation surface or a top surface of the CAAC-OS film, and is parallel to the formation surface or the top surface of the CAAC-OS.

(368) FIGS. **29**B and **29**C show Cs-corrected high-resolution TEM images of a plane of the CAAC-OS observed from a direction substantially perpendicular to the sample surface. FIGS. **29**D and **29**E are images obtained through image processing of FIGS. **29**B and **29**C. The method of image processing is as follows. The image in FIG. **29**B is subjected to fast Fourier transform (FFT), so that an FFT image is obtained. Then, mask processing is performed such that a range of from 2.8 nm.sup.−1 to 5.0 nm.sup.−1 from the origin in the obtained FFT image remains. After the mask processing, the FFT image is processed by inverse fast Fourier transform (IFFT) to obtain a processed image. The image obtained in this manner is called an FFT filtering image. The FFT filtering image is a Cs-corrected high-resolution TEM image from which a periodic component is extracted, and shows a lattice arrangement.

(369) In FIG. **29**D, a portion where a lattice arrangement is broken is denoted with a dashed line. A region surrounded by a dashed line is one pellet. The portion denoted with the dashed line is a junction of pellets. The dashed line draws a hexagon, which means that the pellet has a hexagonal shape. Note that the shape of the pellet is not always a regular hexagon but is a non-regular hexagon in many cases.

(370) In FIG. **29**E, a dotted line denotes a portion where the direction of a lattice arrangement changes between a region with a regular lattice arrangement and another region with a regular lattice arrangement, and a dashed line denotes the change in the direction of the lattice arrangement. A clear crystal grain boundary cannot be observed even in the vicinity of the dotted line. When a lattice point in the vicinity of the dotted line is regarded as a center and surrounding lattice points are joined, a distorted hexagon, pentagon, and/or heptagon can be formed, for example. That is, a lattice arrangement is distorted so that formation of a crystal grain boundary is inhibited. This is probably because the CAAC-OS can tolerate distortion owing to a low density of the atomic arrangement in an a-b plane direction, the change of interatomic bond distance caused by substitution of a metal element, and the like.

(371) As described above, the CAAC-OS has c-axis alignment, its pellets (nanocrystals) are connected in an a-b plane direction, and the crystal structure has distortion. For this reason, the CAAC-OS can also be referred to as an oxide semiconductor including a c-axis-aligned a-b-plane-anchored (CAA) crystal.

(372) The CAAC-OS is an oxide semiconductor with high crystallinity. Entry of impurities, formation of defects, or the like might decrease the crystallinity of an oxide semiconductor. This means that the CAAC-OS has small amounts of impurities and defects (e.g., oxygen vacancies).

(373) Note that the impurity means an element other than the main components of the oxide semiconductor, such as hydrogen, carbon, silicon, or a transition metal element. For example, an element (specifically, silicon or the like) having higher strength of bonding to oxygen than a metal element included in an oxide semiconductor extracts oxygen from the oxide semiconductor, which results in disorder of the atomic arrangement and reduced crystallinity of the oxide semiconductor. A heavy metal such as iron or nickel, argon, carbon dioxide, or the like has a large atomic radius (or molecular radius), and thus disturbs the atomic arrangement of the oxide semiconductor and decreases crystallinity.

(374) The characteristics of an oxide semiconductor having impurities or defects might be changed by light, heat, or the like. For example, impurities contained in the oxide semiconductor might serve as carrier traps or carrier generation sources. For example, oxygen vacancy in the oxide semiconductor might serve as a carrier trap or serve as a carrier generation source when hydrogen is captured therein.

(375) The CAAC-OS having small amounts of impurities and oxygen vacancies is an oxide semiconductor with low carrier density (specifically, lower than 8×10.sup.11/cm.sup.3, preferably lower than 1×10.sup.11/cm.sup.3, further preferably lower than 1×10.sup.10/cm.sup.3 and higher than or equal to 1×10.sup.−9/cm.sup.3). Such an oxide semiconductor is referred to as a highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor. A CAAC-OS has a low impurity concentration and a low density of defect states. Thus, the CAAC-OS can be referred to as an oxide semiconductor having stable characteristics.

(376) <nc-OS>

(377) Next, an nc-OS is described.

(378) Analysis of an nc-OS by XRD is described. For example, when the structure of an nc-OS is analyzed by an out-of-plane method, a peak indicating orientation does not appear. That is, a crystal of an nc-OS does not have orientation.

(379) In addition, for example, when an electron beam with a probe diameter of 50 nm is incident on a 34-nm-thick region of thinned nc-OS including an InGaZnO 4 crystal in a direction parallel to the formation surface, a ring-shaped diffraction pattern (a nanobeam electron diffraction pattern) shown in FIG. **30**A is observed. FIG. **30**B shows a diffraction pattern obtained when an electron beam with a probe diameter of 1 nm is incident on the same sample. As shown in FIG. **30**B, a plurality of spots are observed in a ring-like region. In other words, ordering in an nc-OS is not observed with an electron beam with a probe diameter of 50 nm but is observed with an electron beam with a probe diameter of 1 nm.

(380) Furthermore, an electron diffraction pattern in which spots are arranged in an approximately regular hexagonal shape is observed in some cases as shown in FIG. **30**C when an electron beam having a probe diameter of 1 nm is incident on a region with a thickness of less than 10 nm. This means that an nc-OS has a well-ordered region, i.e., a crystal, in the range of less than 10 nm in thickness. Note that an electron diffraction pattern having regularity is not observed in some regions because crystals are aligned in various directions.

(381) FIG. **30**D shows a Cs-corrected high-resolution TEM image of a cross section of an nc-OS observed from the direction substantially parallel to the formation surface. In a high-resolution TEM image, an nc-OS has a region in which a crystal part is observed, such as the part indicated by additional lines in FIG. **30**D, and a region in which a crystal part is not clearly observed. In most cases, the size of a crystal part included in the nc-OS is greater than or equal to 1 nm and less than or equal to 10 nm, or specifically, greater than or equal to 1 nm and less than or equal to 3 nm. Note that an oxide semiconductor including a crystal part whose size is greater than 10 nm and less than or equal to 100 nm is sometimes referred to as a microcrystalline oxide semiconductor. In a high-resolution TEM image of the nc-OS, for example, a grain boundary is not clearly observed in some cases. Note that there is a possibility that the origin of the nanocrystal is the same as that of a pellet in a CAAC-OS. Therefore, a crystal part of the nc-OS may be referred to as a pellet in the following description.

(382) As described above, in the nc-OS, a microscopic region (for example, a region with a size greater than or equal to 1 nm and less than or equal to 10 nm, in particular, a region with a size greater than or equal to 1 nm and less than or equal to 3 nm) has a periodic atomic arrangement. There is no regularity of crystal orientation between different pellets in the nc-OS. Thus, the orientation of the whole film is not observed. Accordingly, the nc-OS cannot be distinguished from an a-like OS or an amorphous oxide semiconductor, depending on an analysis method.

(383) Since there is no regularity of crystal orientation between the pellets (nanocrystals) as mentioned above, the nc-OS can also be referred to as an oxide semiconductor including random aligned nanocrystals (RANC) or an oxide semiconductor including non-aligned nanocrystals (NANC).

(384) The nc-OS is an oxide semiconductor that has high regularity as compared with an amorphous oxide semiconductor. Therefore, the nc-OS is likely to have a lower density of defect states than an a-like OS and an amorphous oxide semiconductor. Note that there is no regularity of crystal orientation between different pellets in the nc-OS. Therefore, the nc-OS has a higher density of defect states than the CAAC-OS.

(385) <a-like OS>

(386) An a-like OS has a structure intermediate between those of the nc-OS and the amorphous oxide semiconductor.

(387) FIGS. **31**A and **31**B are high-resolution cross-sectional TEM images of an a-like OS. FIG. **31**A is the high-resolution cross-sectional TEM image of the a-like OS at the start of the electron irradiation. FIG. **31**B is the high-resolution cross-sectional TEM image of a-like OS after the electron (e^{-}) irradiation at $4.3 \times 10^{8} e^{-}/nm^{2}$. FIGS. **31**A and **31**B show that stripe-like bright regions extending vertically are observed in the a-like OS from the start of the electron irradiation. It can also be found that the shape of the bright region changes after the electron irradiation. Note that the bright region is presumably a void or a low-density region.

(388) The a-like OS has an unstable structure because it contains a void. To verify that an a-like OS has an unstable structure as compared with a CAAC-OS and an nc-OS, a change in structure caused by electron irradiation is described below.

(389) An a-like OS, an nc-OS, and a CAAC-OS are prepared as samples. Each of the samples is an In—Ga—Zn oxide.

(390) First, a high-resolution cross-sectional TEM image of each sample is obtained. The high-resolution cross-sectional TEM images show that all the samples have crystal parts.

(391) It is known that a unit cell of an InGaZnO$_4$ crystal has a structure in which nine layers including three In—O layers and six Ga—Zn—O layers are stacked in the c-axis direction. The distance between the adjacent layers is equivalent to the lattice spacing on the (009) plane (also referred to asd value). The value is calculated to be 0.29 nm from crystal structural analysis. Accordingly, a portion where the spacing between lattice fringes is greater than or equal to 0.28 nm and less than or equal to 0.30 nm is regarded as a crystal part of InGaZnO 4 in the following description. Each of lattice fringes corresponds to the a-b plane of the InGaZnO 4 crystal.

(392) FIG. **32** shows change in the average size of crystal parts (at 22 points to 30 points) in each sample. Note that the crystal part size corresponds to the length of the lattice fringe. FIG. **32** indicates that the crystal part size in the a-like OS increases with an increase in the cumulative electron dose in obtaining TEM images, for example. As shown in FIG. **32**, a crystal part of approximately 1.2 nm (also referred to as an initial nucleus) at the start of TEM observation grows to a size of approximately 1.9 nm at a cumulative electron (e^{-}) dose of $4.2 \times 10^{8} e^{-}/nm^{2}$. In contrast, the crystal part size in the nc-OS and the CAAC-OS shows little change from the start of electron irradiation to a cumulative electron dose of $4.2 \times 10^{8} e^{-}/nm^{2}$. As shown in FIG. **32**, the crystal part sizes in an nc-OS and a CAAC-OS are approximately 1.3 nm and approximately 1.8 nm, respectively, regardless of the cumulative electron dose. For the electron beam irradiation and TEM observation, a Hitachi H-9000 NAR transmission electron microscope was used. The conditions of electron beam irradiation were as follows: the accelerating voltage was 300 kV; the current density was $6.7 \times 10^{5} e^{-}/(nm^{2} \cdot s)$; and the diameter of the irradiation region was 230 nm.

(393) In this manner, growth of the crystal part in the a-like OS is induced by electron irradiation in some cases. In contrast, in the nc-OS and the CAAC-OS, growth of the crystal part is hardly induced by electron irradiation. Therefore, the a-like OS has an unstable structure as compared with the nc-OS and the CAAC-OS.

(394) The a-like OS has a lower density than the nc-OS and the CAAC-OS because it contains a void. Specifically, the density of the a-like OS is higher than or equal to 78.6% and lower than 92.3% of the density of the single crystal oxide semiconductor having the same composition. The density of each of the nc-OS and the CAAC-OS is higher than or equal to 92.3% and lower than 100% of the density of the single crystal oxide semiconductor having the same composition. Note that it is difficult to deposit an oxide semiconductor having a density of lower than 78% of the density of the single crystal oxide semiconductor.

(395) For example, in the case of an oxide semiconductor having an atomic ratio of In:Ga:Zn=1:1:1, the density of single crystal InGaZnO$_4$ with a rhombohedral crystal structure is 6.357 g/cm^3. Accordingly, in the case of the oxide semiconductor having an atomic ratio of In:Ga:Zn=1:1:1, the density of the a-like OS is higher than or equal to 5.0 g/cm^3 and lower than 5.9 g/cm^3. For example, in the case of the oxide semiconductor having an atomic ratio of In:Ga:Zn=1:1:1, the density of each of the nc-OS and the CAAC-OS is higher than or equal to 5.9 g/cm^3 and lower than 6.3 g/cm^3.

(396) Note that in the case where an oxide semiconductor having a certain composition does not exist in a single crystal structure, single crystal oxide semiconductors with different compositions are combined at an adequate ratio, which makes it possible to calculate density equivalent to that of a single crystal oxide semiconductor with the desired composition. The density of a single crystal oxide semiconductor having the desired composition can be estimated using a weighted average according to the combination ratio of the single crystal oxide semiconductors with different compositions. Note that it is preferable to use as few kinds of single crystal oxide semiconductors as possible to estimate the density.

(397) As described above, oxide semiconductors have various structures and various properties. Note that an oxide semiconductor may be a stacked layer including two or more films of an amorphous oxide semiconductor, an a-like OS, an nc-OS, and a CAAC-OS, for example.

(398) (Supplementary Notes on the Description in this Specification and the Like)

(399) The following are notes on the description of the above embodiments and structures in the embodiments.

Notes on One Embodiment of the Present Invention Described in Embodiments

(400) One embodiment of the present invention can be constituted by appropriately combining the structure described in an embodiment with any of the structures described in the other embodiments. In addition, in the case where a plurality of structure examples are described in one embodiment, some of the structure examples can be combined as appropriate.

(401) Note that what is described (or part thereof) in an embodiment can be applied to, combined with, or replaced with another content in the same embodiment and/or what is described (or part thereof) in another embodiment or other embodiments.

(402) Note that in each embodiment, a content described in the embodiment is a content described with reference to a variety of diagrams or a content described with text disclosed in this specification.

(403) Note that by combining a diagram (or may be part of the diagram) described in one embodiment with another part of the diagram, a different diagram (or may be part of the different diagram) described in the embodiment, and/or a diagram (or may be part of the diagram) described in one or a plurality of different embodiments, much more diagrams can be formed.

Notes on the Description for Drawings

(404) In this specification and the like, terms for explaining arrangement, such as "over" and "under", are used for convenience to describe the positional relation between components with reference to drawings. Furthermore, the positional relation between components is changed as appropriate in accordance with a direction in which the components are described. Therefore, the terms for explaining arrangement are not limited to those used in this specification and may be changed to other terms as appropriate depending on the situation.

(405) The term "over" or "below" does not necessarily mean that a component is placed directly on or directly below and directly in contact with another component. For example, the expression "electrode B over insulating layer A" does not necessarily mean that the electrode B is on and in direct contact with the insulating layer A and can mean the case where another component is provided between the insulating layer A and the electrode B.

(406) Furthermore, in a block diagram in this specification and the like, components are functionally classified and shown by blocks that are independent from each other. However, in an actual circuit and the like, such components are sometimes hard to classify functionally, and there is a

case in which one circuit is concerned with a plurality of functions or a case in which a plurality of circuits are concerned with one function. Therefore, blocks in a block diagram do not necessarily show components described in the specification, which can be explained with another term as appropriate depending on the situation.

(407) In drawings, the size, the layer thickness, or the region is determined arbitrarily for description convenience. Therefore, the size, the layer thickness, or the region is not limited to the illustrated scale. Note that the drawings are schematically shown for clarity, and embodiments of the present invention are not limited to shapes or values shown in the drawings. For example, the following can be included: variation in signal, voltage, or current due to noise or difference in timing.

Notes on Expressions that can be Rephrased

(408) In this specification or the like, the terms "one of a source and a drain" (or a first electrode or a first terminal) and "the other of the source and the drain" (or a second electrode or a second terminal) are used to describe the connection relation of a transistor. This is because a source and a drain of a transistor are interchangeable depending on the structure, operation conditions, or the like of the transistor. Note that the source or the drain of the transistor can also be referred to as a source (or drain) terminal, a source (or drain) electrode, or the like as appropriate depending on the situation.

(409) In addition, in this specification and the like, the term such as an "electrode" or a "wiring" does not limit a function of the component. For example, an "electrode" is used as part of a "wiring" in some cases, and vice versa. Further, the term "electrode" or "wiring" can also mean a combination of a plurality of "electrodes" and "wirings" formed in an integrated manner.

(410) In this specification and the like, "voltage" and "potential" can be replaced with each other. The term "voltage" refers to a potential difference from a reference potential. When the reference potential is a ground potential, for example, "voltage" can be replaced with "potential." The ground potential does not necessarily mean 0 V. Potentials are relative values, and the potential applied to a wiring or the like is changed depending on the reference potential, in some cases.

(411) In this specification and the like, the terms "film" and "layer" can be used interchangeably depending on the case or circumstances. For example, the term "conductive layer" can be changed into the term "conductive film" in some cases. Also, the term "insulating film" can be changed into the term "insulating layer" in some cases.

Notes on Definitions of Terms

(412) The following are definitions of the terms that are not mentioned in the above embodiments.

(413) <<Switch>>

(414) In this specification and the like, a switch is conducting (on state) or not conducting (off state) to determine whether current flows therethrough or not. Alternatively, a switch has a function of selecting and changing a current path.

(415) Examples of a switch are an electrical switch, a mechanical switch, and the like. That is, any element can be used as a switch as long as it can control current, without limitation to a certain element.

(416) Examples of the electrical switch are a transistor (e.g., a bipolar transistor or a MOS transistor), a diode (e.g., a PN diode, a PIN diode, a Schottky diode, a metal-insulator-metal (MIM) diode, a metal-insulator-semiconductor (MIS) diode, or a diode-connected transistor), and a logic circuit in which such elements are combined.

(417) In the case of using a transistor as a switch, an "on state" of the transistor refers to a state in which a source and a drain of the transistor are electrically short-circuited. Furthermore, an "off state" of the transistor refers to a state in which the source and the drain of the transistor are electrically disconnected. In the case where a transistor operates just as a switch, the polarity (conductivity type) of the transistor is not particularly limited to a certain type.

(418) An example of a mechanical switch is a switch formed using a micro electro mechanical system (MEMS) technology, such as a digital micromirror device (DMD). Such a switch includes an electrode which can be moved mechanically, and operates by controlling conduction and non-conduction in accordance with movement of the electrode.

(419) <<Channel Length>>

(420) In this specification and the like, the channel length refers to, for example, a distance between a source and a drain in a region where a semiconductor (or a portion where a current flows in a semiconductor when a transistor is on) and a gate overlap with each other or a region where a channel is formed in a top view of the transistor.

(421) In one transistor, channel lengths in all regions are not necessarily the same. In other words, the channel length of one transistor is not fixed to one value in some cases. Therefore, in this specification, the channel length is any one of values, the maximum value, the minimum value, or the average value in a region where a channel is formed.

(422) <<Channel Width>>

(423) In this specification and the like, the channel width refers to, for example, the length of a portion where a source and a drain face each other in a region where a semiconductor (or a portion where current flows in a semiconductor when a transistor is on) and a gate electrode overlap with each other, or a region where a channel is formed in a top view of the transistor.

(424) In one transistor, channel widths in all regions are not necessarily the same. In other words, the channel width of one transistor is not fixed to one value in some cases. Therefore, in this specification, the channel width is any one of values, the maximum value, the minimum value, or the average value in a region where a channel is formed.

(425) Note that depending on transistor structures, a channel width in a region where a channel is formed actually (hereinafter referred to as an effective channel width) is different from a channel width shown in a top view of the transistor (hereinafter referred to as an apparent channel width) in some cases. For example, in a transistor having a three-dimensional structure, an effective channel width is greater than an apparent channel width shown in a top view of the transistor, and its influence cannot be ignored in some cases. For example, in a miniaturized transistor having a three-dimensional structure, the proportion of a channel region formed in a side surface of a semiconductor is high in some cases. In that case, an effective channel width obtained when a channel is actually formed is greater than an apparent channel width shown in the top view.

(426) In a transistor having a three-dimensional structure, an effective channel width is difficult to measure in some cases. For example, to estimate an effective channel width from design parameters, the shape of the semiconductor need to be known beforehand. Therefore, when accurate shape information of the semiconductor is not available, accurate measurement of an effective channel width is difficult.

(427) Thus, in this specification, in a top view of a transistor, an apparent channel width that is a length of a portion where a source and a drain face each other in a region where a semiconductor and a gate electrode overlap with each other is referred to as a surrounded channel width (SCW) in some cases. Further, in this specification, in the case where the term "channel width" is simply used, it may represent a surrounded channel width or an apparent channel width. Alternatively, in this specification, in the case where the term "channel width" is simply used, it may represent an effective channel width in some cases. Note that the values of a channel length, a channel width, an effective channel width, an apparent channel width, a surrounded channel width, and the like can be determined by obtaining and analyzing a cross-sectional TEM image and the like.

(428) Note that in the case where field-effect mobility, a current value per channel width, and the like of a transistor are obtained by calculation, a surrounded channel width may be used for the calculation. In that case, a value different from one in the case where an effective channel width is used for the calculation is obtained in some cases.

(429) <<Connection>>

(430) In this specification and the like, when it is described that "A and B are connected to each other", the case where A and B are electrically connected to each other is included in addition to the case where A and B are directly connected to each other. Here, the expression "A and B are electrically connected" means the case where electric signals can be transmitted and received between A and B when an object having any electric

action exists between A and B.

REFERENCE NUMERALS

(431) A**1**-A**2**: dashed-dotted line, A**3**-A**4**: dashed-dotted line, C**0**: capacitor, C**1**: capacitor, MUL**1**: multiplier circuit, MUL**2**: multiplier circuit, MUL**3**: multiplier circuit, MUL**4**: multiplier circuit, Tr**01**: transistor, Tr**08**: transistor, Tr**11**: transistor, Tr**14**: transistor, Tr**15**: transistor, Tr**16**: transistor, Tr**17**: transistor, **10**: image data, **11**: triangle, **12**: circle, **20**: image data, **30**: image data, **31**: region, **40**: image data, **41**: region, **100**: module, **101**: amplifier, **102**: selector circuit, **103**: differential amplifier, **104**: switch, **105**: resistor, **106**: unity gain buffer, **107**: amplifier circuit, **108**: buffer, **111**: differential amplifier, **112**: switch, **113**: resistor, **114**: selector circuit, **115**: differential amplifier, **116**: switch, **117**: resistor, **121**: operational amplifier, **122**: operational amplifier, **500**: broadcasting system, **510**: camera, **511**: transceiver, **512**: receiver, **513**: display device, **520**: image sensor, **521**: image processor, **522**: encoder, **523**: modulator, **525**: demodulator, **526**: decoder, **527**: image processor, **528**: display portion, **540**: Raw data, **541**: video data, **542**: encoding data, **543**: broadcasting signal, **544**: video data, **545**: data signal, **551**: data stream, **552**: data stream, **553**: data stream, **560**: TV, **561**: broadcasting station, **562**: artificial satellite, **563**: radio tower, **564**: antenna, **565**: antenna, **566**A: radio wave, **566**B: radio wave, **567**A: radio wave, **567**B: radio wave, **571**: receiver, **572**: wireless transmitter, **573**: wireless transmitter, **574**: receiver, **575**: connector portion, **591**: circuit, **591***a*: inter-frame prediction circuit, **591***b*: motion-compensated prediction circuit, **591***c*: DCT circuit, **592**: circuit, **593**: circuit, **593***a*: LDPC encoding circuit, **593***b*: authentication processing circuit, **593***c*: scrambler, **594**: circuit, **600**: ambulance, **601**: medical institution, **602**: medical institution, **605**: high-speed network, **610**: camera, **611**: encoder, **612**: communication device, **615**: video data, **616**: video data, **620**: communication device, **621**: decoder, **623**: display device, **1400***a*: transistor, **1400***b*: transistor, **1400***c*: transistor, **1400***d*: transistor, **1400***e*: transistor, **1400***f*: transistor, **1401**: insulating film, **1402**: insulating film, **1403**: insulating film, **1404**: insulating film, **1405**: insulating film, **1406**: insulating film, **1407**: insulating film, **1408**: insulating film, **1409**: insulating film, **1411**: conductive film, **1412**: conductive film, **1413**: conductive film, **1414**: conductive film, **1421**: conductive film, **1422**: conductive film, **1423**: conductive film, **1424**: conductive film, **1430**: metal oxide, **1431**: metal oxide, **1431***a*: metal oxide, **1431***b*: metal oxide, **1431***c*: metal oxide, **1432**: metal oxide, **1432***a*: metal oxide, **1432***b*: metal oxide, **1432***c*: metal oxide, **1433**: metal oxide, **1441**: region, **1442**: region, **1450**: substrate, **1451**: low-resistance region, **1452**: low-resistance region, **1461**: region, **1461***a*: region, **1461***b*: region, **1461***c*: region, **1461***d*: region, **1461***e*: region, **1462**: region, **1463**: region, **1680**: transistor, **1681**: insulating film, **1682**: semiconductor, **1683**: conductive film, **1684**: conductive film, **1685**: insulating film, **1686**: insulating film, **1687**: insulating film, **1688**: conductive film, and **1689**: conductive film.

(432) This application is based on Japanese Patent Application serial no. 2015-208505 filed with Japan Patent Office on Oct. 23, 2015 and Japanese Patent Application serial no. 2015-228425 filed with Japan Patent Office on Nov. 24, 2015, the entire contents of which are hereby incorporated by reference.

Claims

1. A module comprising: a first circuit; a second circuit; and a third circuit, wherein the first circuit is configured: to amplify a first signal and to output the amplified first signal to the second circuit; and to convert the first signal from current to voltage, to amplify the converted first signal, and to output the amplified converted first signal to another module, wherein the second circuit comprises: a first multiplier circuit multiplying the amplified first signal and a third signal from the third circuit, for changing data corresponding to a connection strength; an analog memory configured to store the changed data; and a second multiplier circuit configured to output a second signal corresponding to the amplified first signal, that the amplified first signal has been weighted in accordance with the changed data, wherein the third circuit is configured: to convert the second signal from current to voltage; to output the converted second signal to an outside; and to output the third signal to the second circuit, and wherein the analog memory comprises: a transistor comprising an oxide semiconductor in a channel formation region; and a capacitor.

2. The module according to claim 1, wherein the first circuit is a neuron circuit.

3. The module according to claim 1, wherein the second circuit is a synapse circuit.

4. The module according to claim 1, wherein the third circuit is an error circuit.

5. An electronic device comprising the module according to claim 1, further comprising: an encoder configured to encode video data, wherein the video data comprises first video data and second video data, and wherein the module is configured: to compare the first video data and the second video data when the first video data and the second video data are input to the module; and to obtain a motion vector from position of a part of the first video data to position of a part of the second video data when the part of the first video data and the part of the second video data match.

6. A module comprising: a neuron circuit; a synapse circuit; and an error circuit, wherein the synapse circuit comprises: a first multiplier circuit multiplying an output signal from the neuron circuit and an output signal from the error circuit, for changing data corresponding to a connection strength; an analog memory configured to store the changed data; and a second multiplier circuit configured to output a signal that the output signal from the neuron circuit is weighted in accordance with the changed data, and wherein the analog memory comprises: a transistor comprising an oxide semiconductor in a channel formation region; and a capacitor.

7. The module according to claim 6, wherein the neuron circuit comprises a first selector circuit configured to select whether the neuron circuit is configured as an input neuron circuit or as a hidden neuron circuit, wherein the neuron circuit is configured to amplify an input signal and output the amplified input signal to the synapse circuit when the neuron circuit functions as the input neuron circuit, and wherein the neuron circuit is configured: to convert the input signal from current to voltage; to amplify the converted input signal; and to output the amplified converted input signal to another synapse circuit when the neuron circuit is the hidden neuron circuit.

8. The module according to claim 6, wherein the error circuit comprises a second selector circuit configured to select whether the error circuit is configured as an output neuron circuit or as a hidden error circuit, wherein the error circuit is configured to convert a current output from the synapse circuit to voltage and output the converted voltage to another module when the error circuit is the output neuron circuit, and wherein the error circuit is configured to multiply a derivative of the converted voltage and a difference signal between an instructor signal based on an error signal outputted from a synapse circuit of a module in a succeeding stage and a reference signal when the error circuit is the hidden error circuit.