

(56)

References Cited

U.S. PATENT DOCUMENTS

- | | | | | | | | |
|--------------|-----|---------|-----------------------------|--------------|-----|---------|-------------------------------|
| 2002/0009851 | A1 | 1/2002 | Shukuri et al. | 2011/0114996 | A1 | 5/2011 | Fiorenza et al. |
| 2003/0232285 | A1 | 12/2003 | Hao et al. | 2011/0117738 | A1 | 5/2011 | Russell et al. |
| 2004/0209432 | A1 | 10/2004 | Ku et al. | 2011/0169105 | A1 | 7/2011 | Okubo |
| 2004/0251479 | A1 | 12/2004 | Tsutsui et al. | 2011/0220964 | A1* | 9/2011 | Shin H01L 29/66628 |
| 2005/0032359 | A1* | 2/2005 | Hao H01L 29/66553 | | | | 257/E29.005 |
| | | | 257/E21.434 | 2011/0241071 | A1* | 10/2011 | Shin H01L 29/66636 |
| 2005/0127468 | A1* | 6/2005 | Ito H01L 21/823481 | | | | 257/190 |
| | | | 257/E21.546 | 2012/0001198 | A1* | 1/2012 | Yin H01L 29/78 |
| 2005/0285137 | A1 | 12/2005 | Satoh | | | | 257/E21.409 |
| 2006/0003527 | A1* | 1/2006 | Mitros H10B 20/00 | 2012/0001271 | A1* | 1/2012 | Chae H01L 23/535 |
| | | | 438/257 | | | | 257/E27.06 |
| 2007/0063349 | A1 | 3/2007 | Kao et al. | 2012/0108032 | A1* | 5/2012 | Yin H01L 29/045 |
| 2007/0221962 | A1 | 9/2007 | Ishizu | | | | 257/E21.54 |
| 2007/0267707 | A1 | 11/2007 | Tsutsui | 2012/0132987 | A1 | 5/2012 | Chuang et al. |
| 2007/0287240 | A1 | 12/2007 | Chen | 2012/0302018 | A1* | 11/2012 | Shin H01L 29/66636 |
| 2008/0036013 | A1 | 2/2008 | Kotani | | | | 257/E21.409 |
| 2008/0054250 | A1* | 3/2008 | Chuang H01L 21/823425 | 2013/0011983 | A1 | 1/2013 | Tsai et al. |
| | | | 257/19 | 2013/0069136 | A1* | 3/2013 | Mao H10D 30/0411 |
| 2008/0083949 | A1 | 4/2008 | Zhu et al. | | | | 438/257 |
| 2008/0093673 | A1* | 4/2008 | Tamura H01L 29/7843 | 2013/0113047 | A1* | 5/2013 | Dhanyakumar H01L 29/167 |
| | | | 257/E29.345 | | | | 257/E21.409 |
| 2008/0128825 | A1 | 6/2008 | Sato et al. | 2013/0115743 | A1* | 5/2013 | Yin H01L 21/8238 |
| 2008/0217665 | A1 | 9/2008 | Chen | | | | 438/199 |
| 2008/0246057 | A1 | 10/2008 | Lin | 2013/0217194 | A1 | 8/2013 | Pidin |
| 2009/0001566 | A1 | 1/2009 | Tigelaar | 2013/0244435 | A1 | 9/2013 | Tanabe |
| 2009/0194817 | A1 | 8/2009 | Lee | 2013/0277719 | A1* | 10/2013 | Kao H01L 27/14609 |
| 2009/0230439 | A1 | 9/2009 | Wang et al. | | | | 257/E21.409 |
| 2009/0236633 | A1 | 9/2009 | Chuang et al. | 2014/0004695 | A1 | 1/2014 | Ando et al. |
| 2009/0283836 | A1* | 11/2009 | Zhu H10D 84/0188 | 2014/0110798 | A1 | 4/2014 | Cai et al. |
| | | | 257/369 | 2014/0231924 | A1 | 8/2014 | Kuo |
| | | | | 2014/0242763 | A1 | 8/2014 | Chen et al. |

* cited by examiner

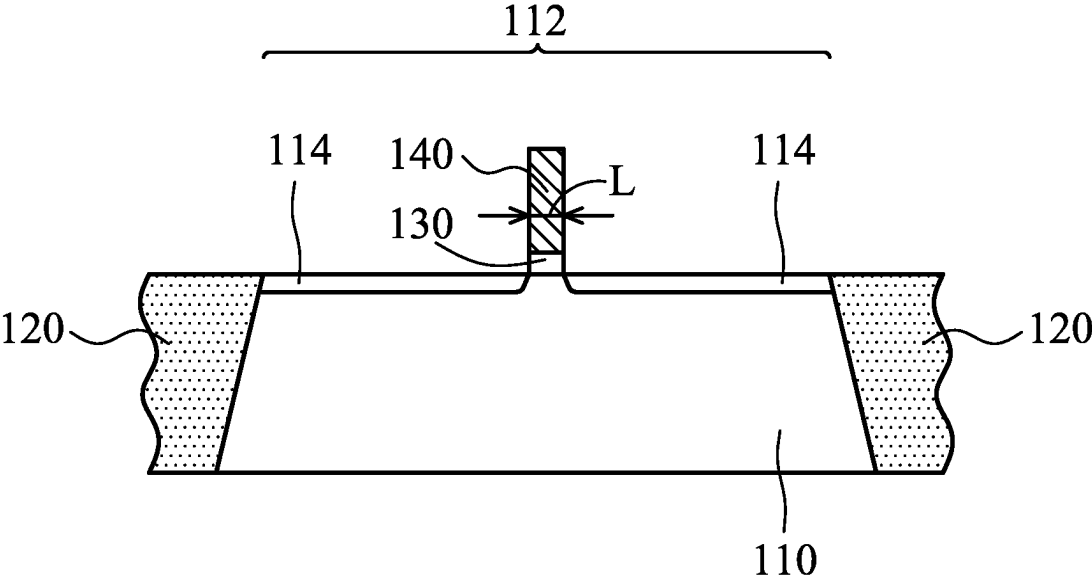


FIG. 1A

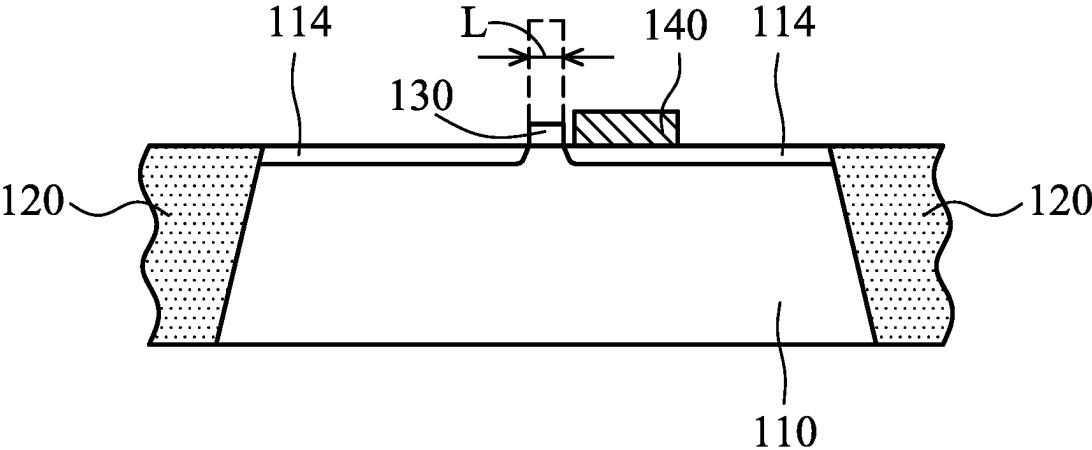


FIG. 1B

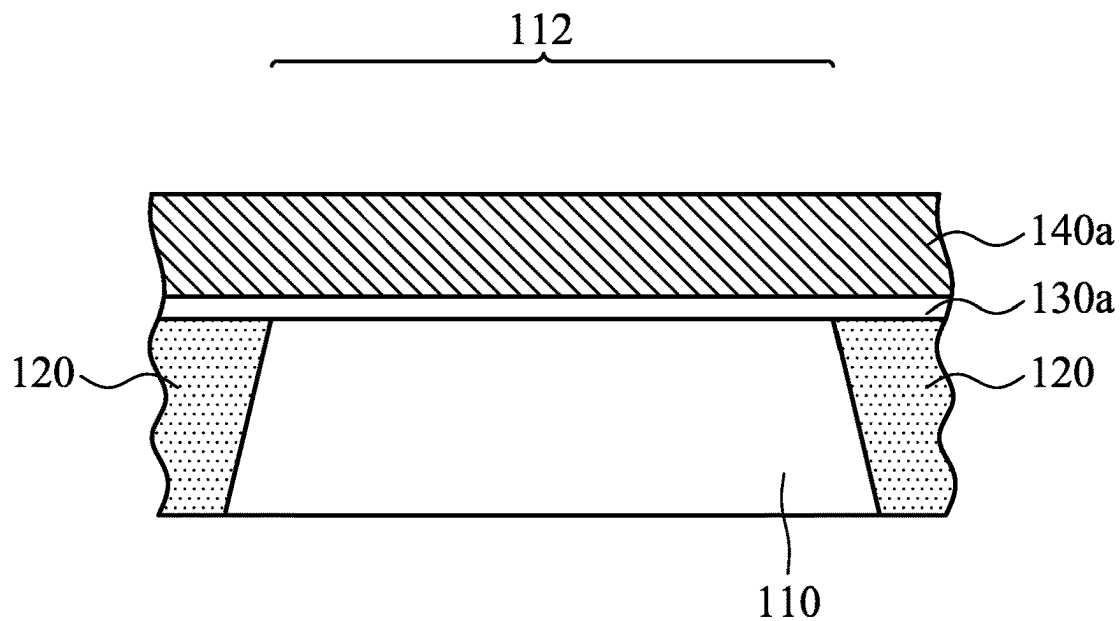


FIG. 2A

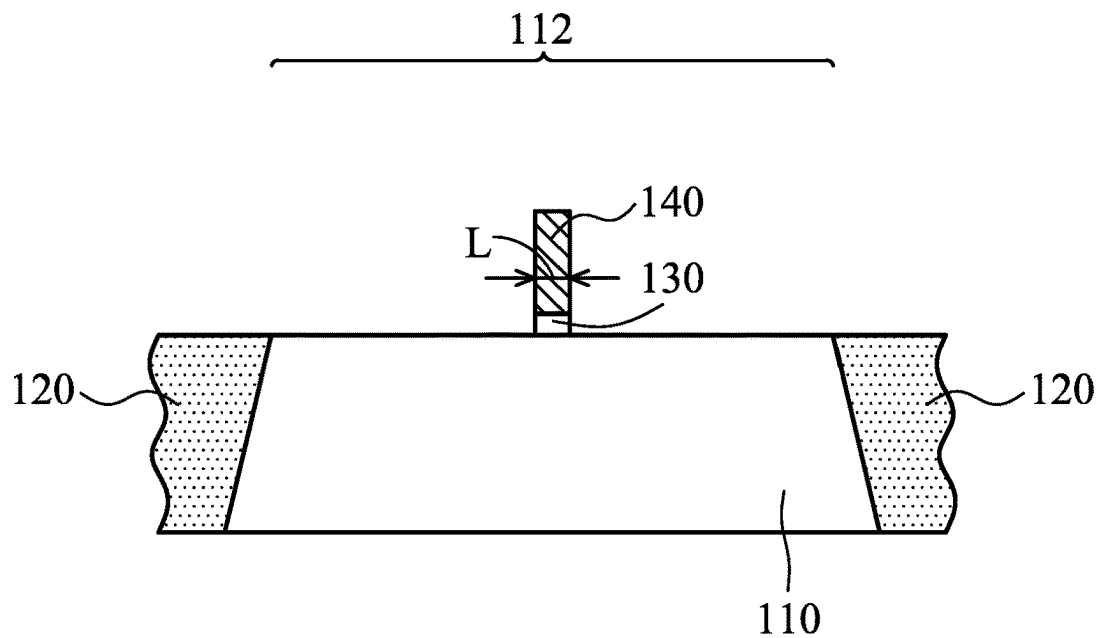


FIG. 2B

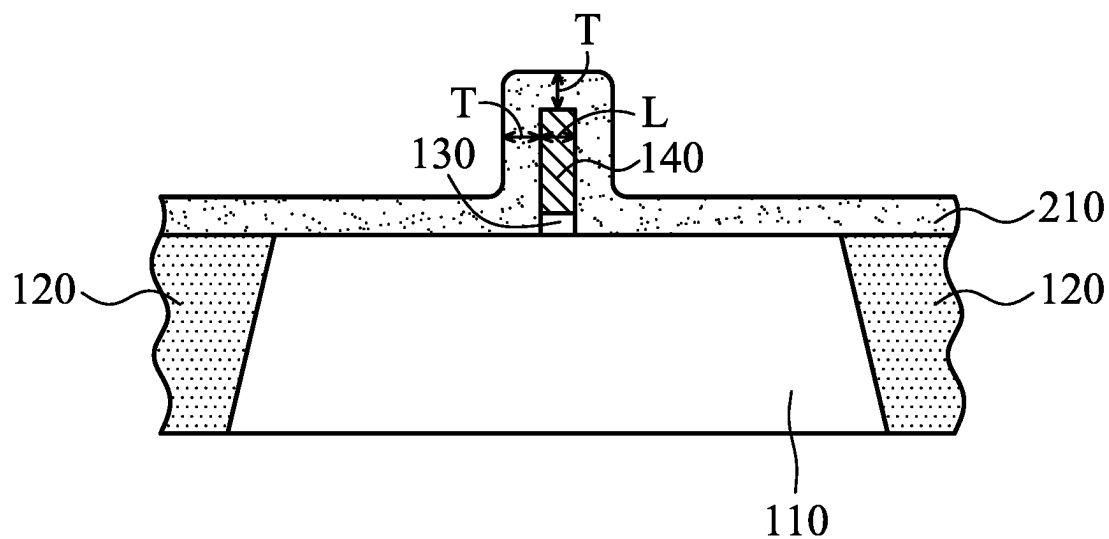


FIG. 2C

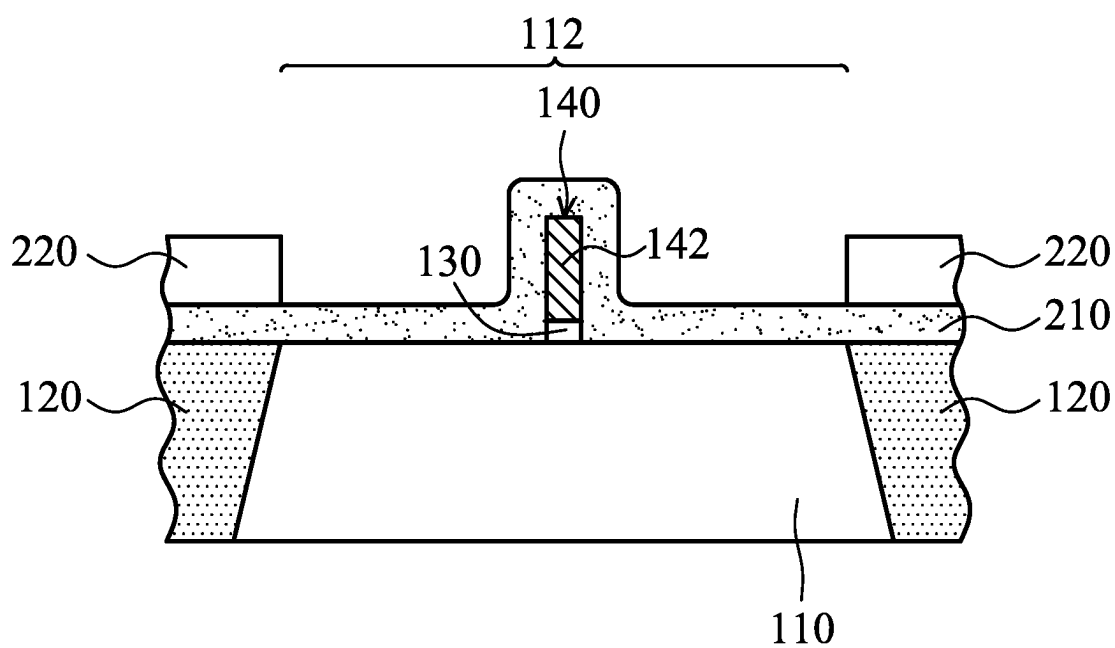


FIG. 2D

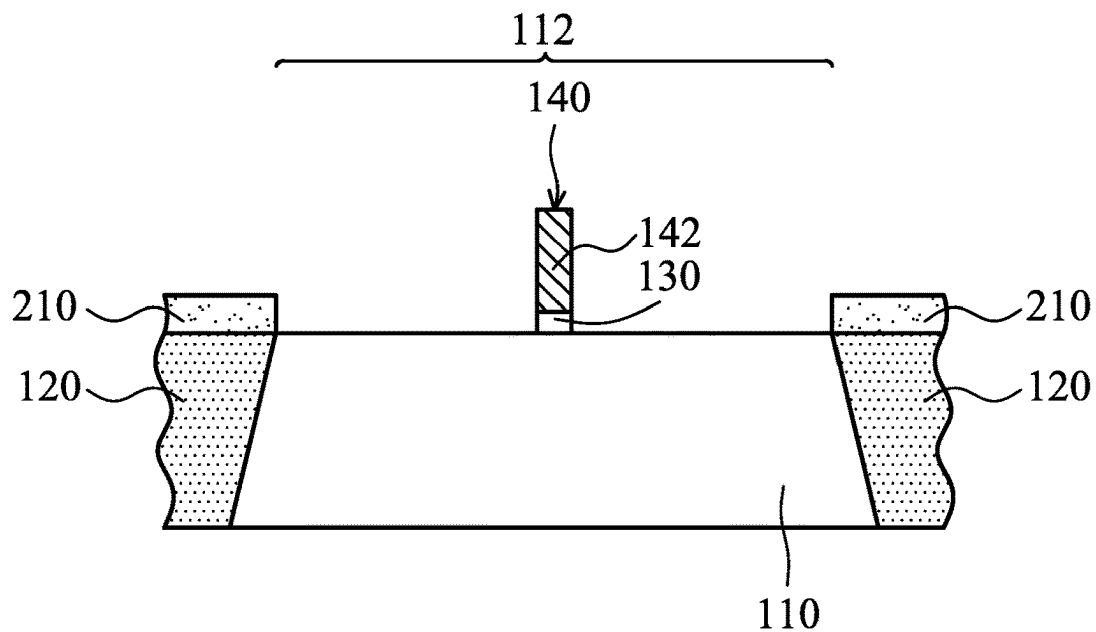


FIG. 2E

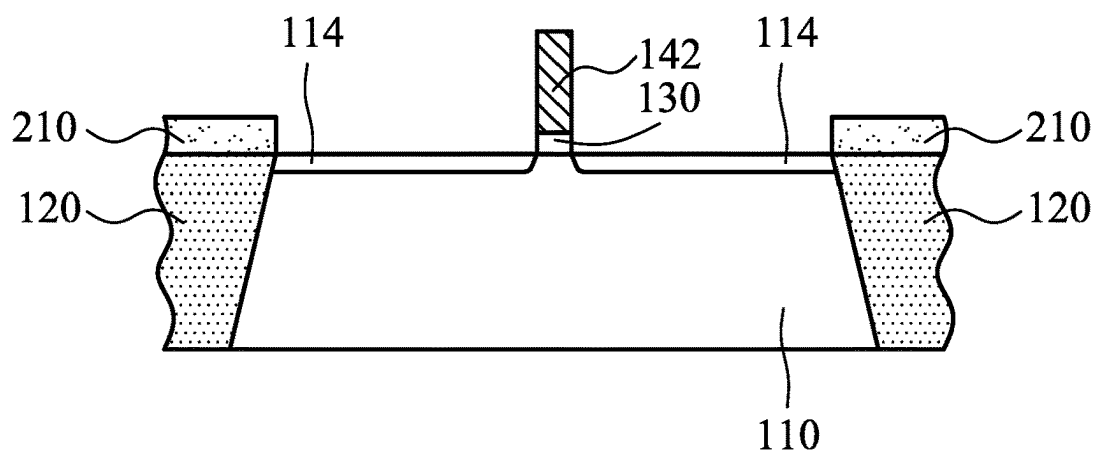


FIG. 2F

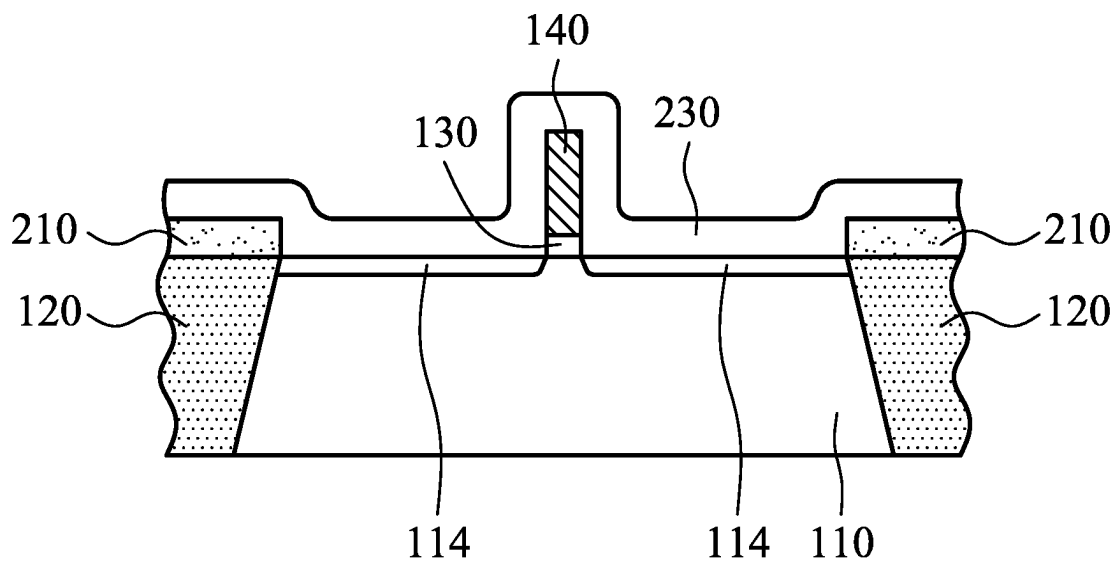


FIG. 2G

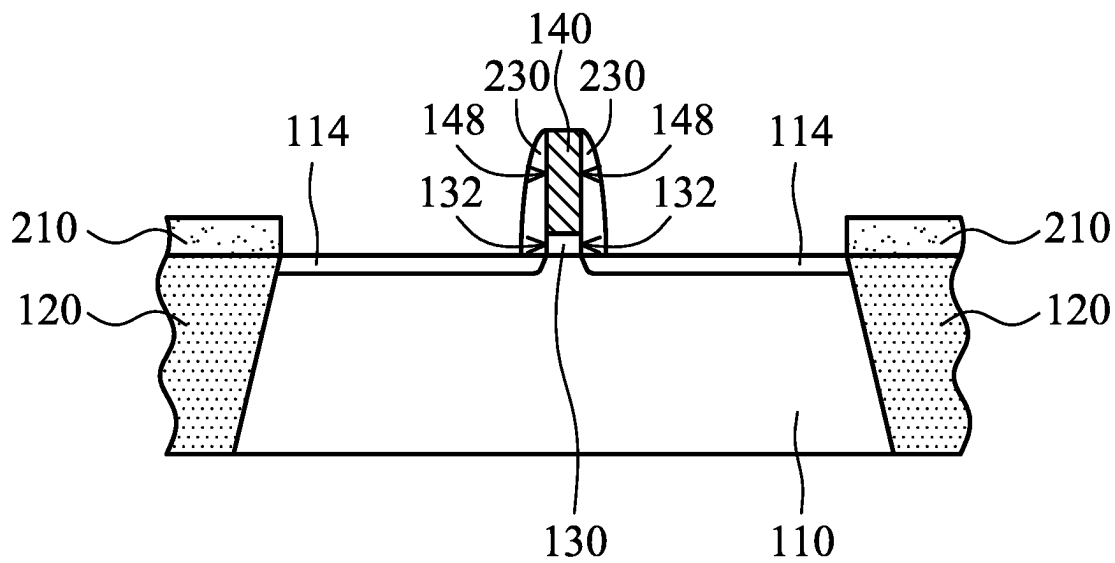


FIG. 2H

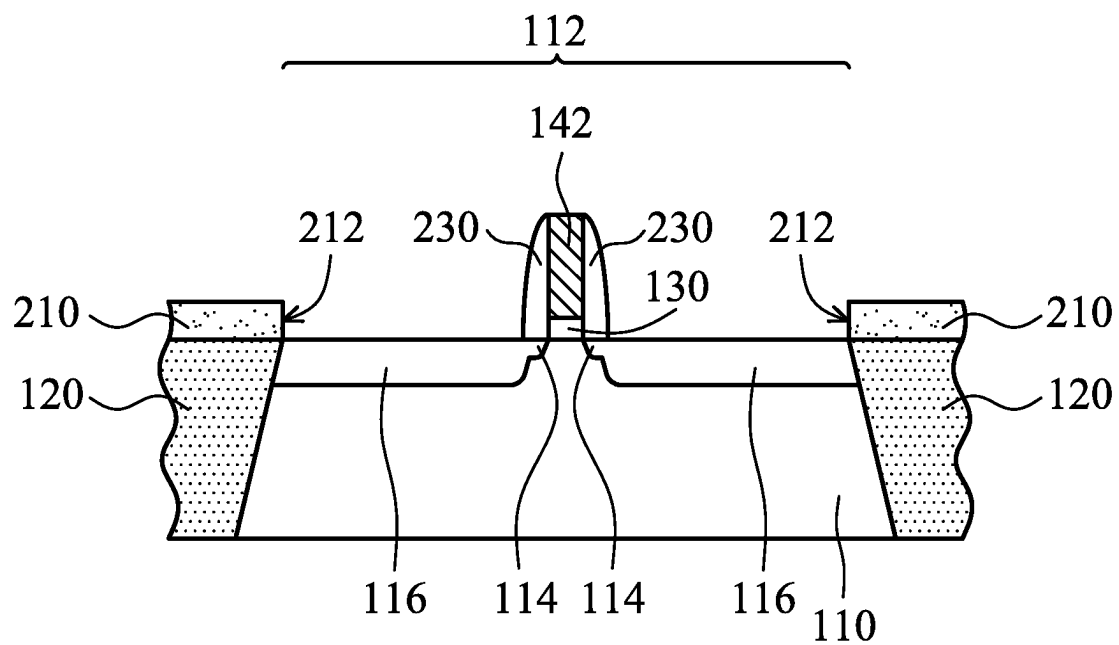


FIG. 2I

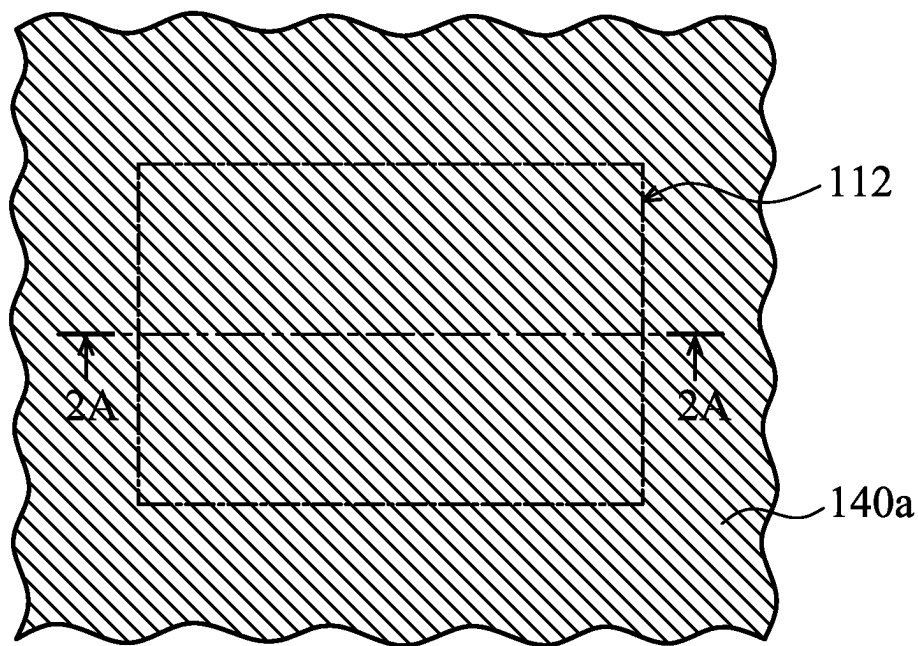


FIG. 3A

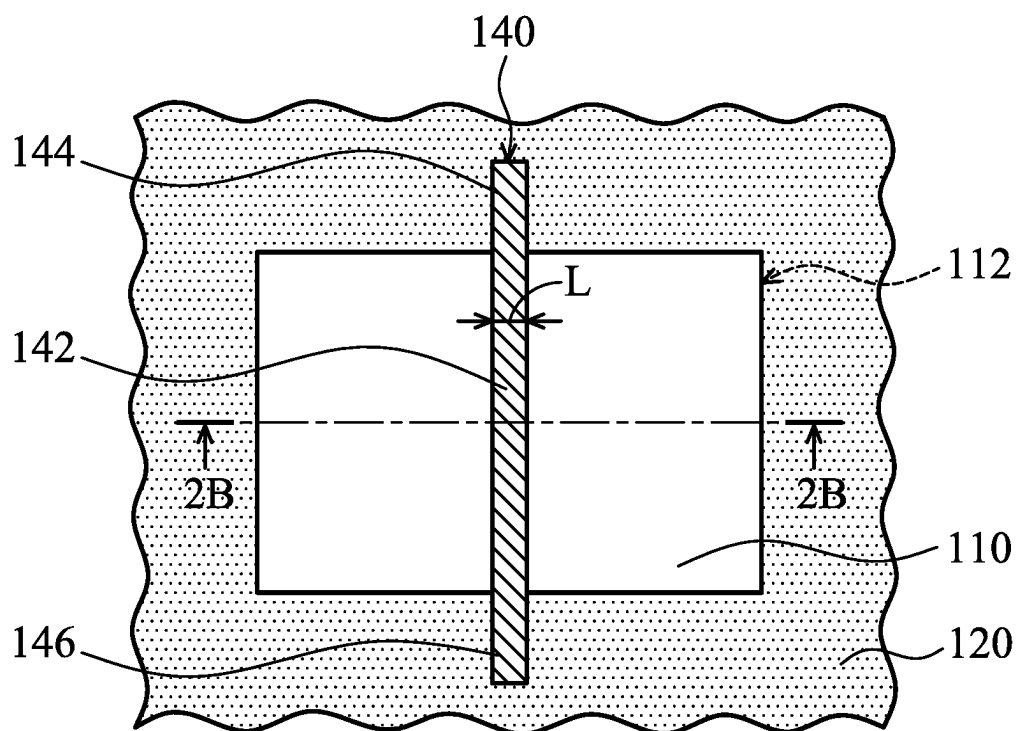


FIG. 3B

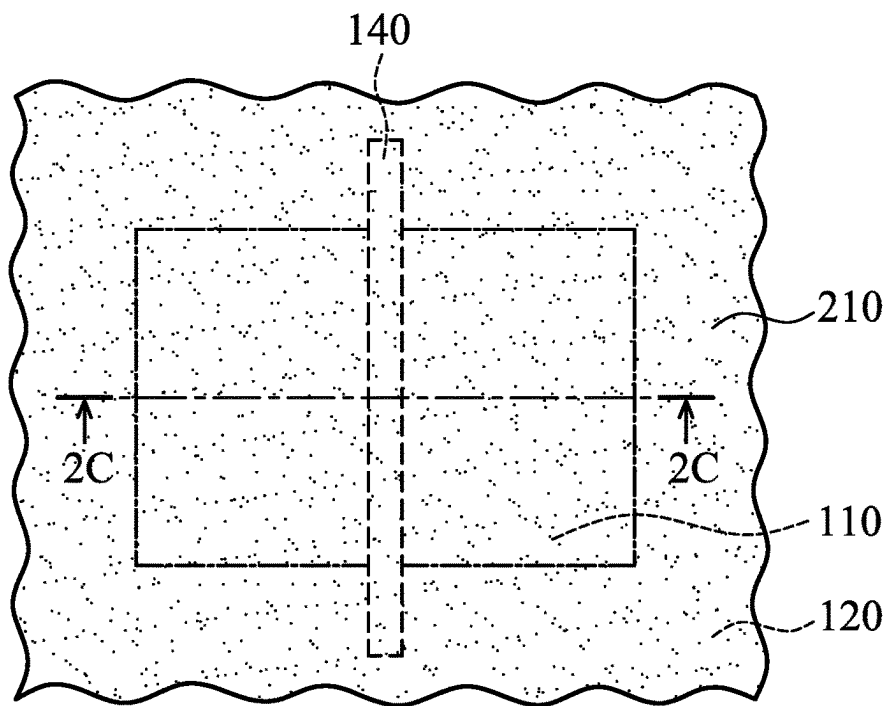


FIG. 3C

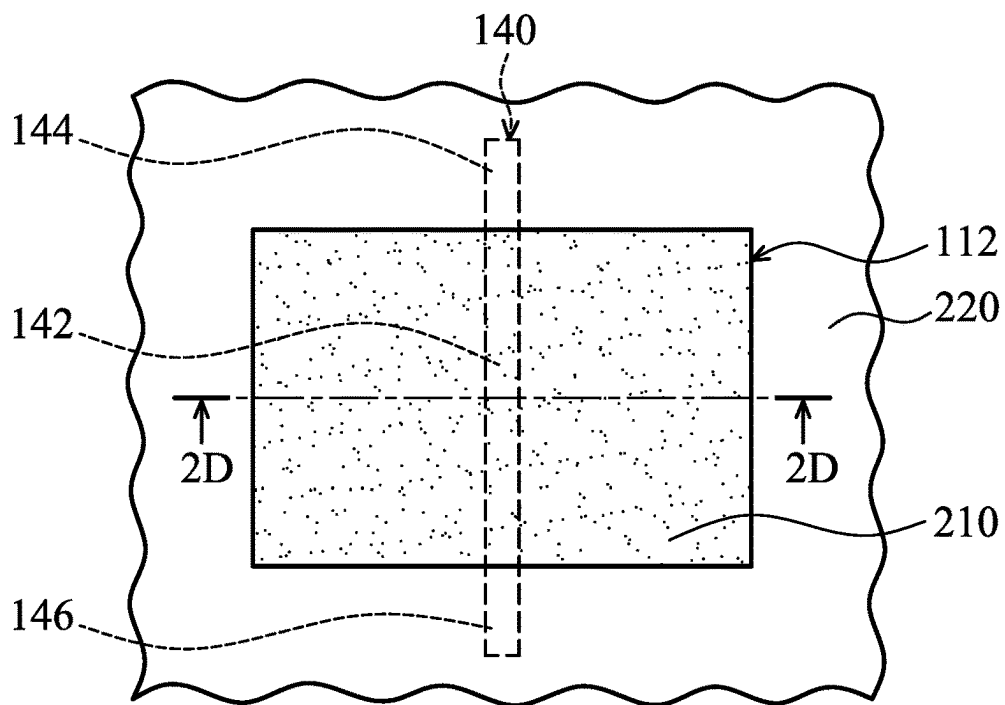


FIG. 3D

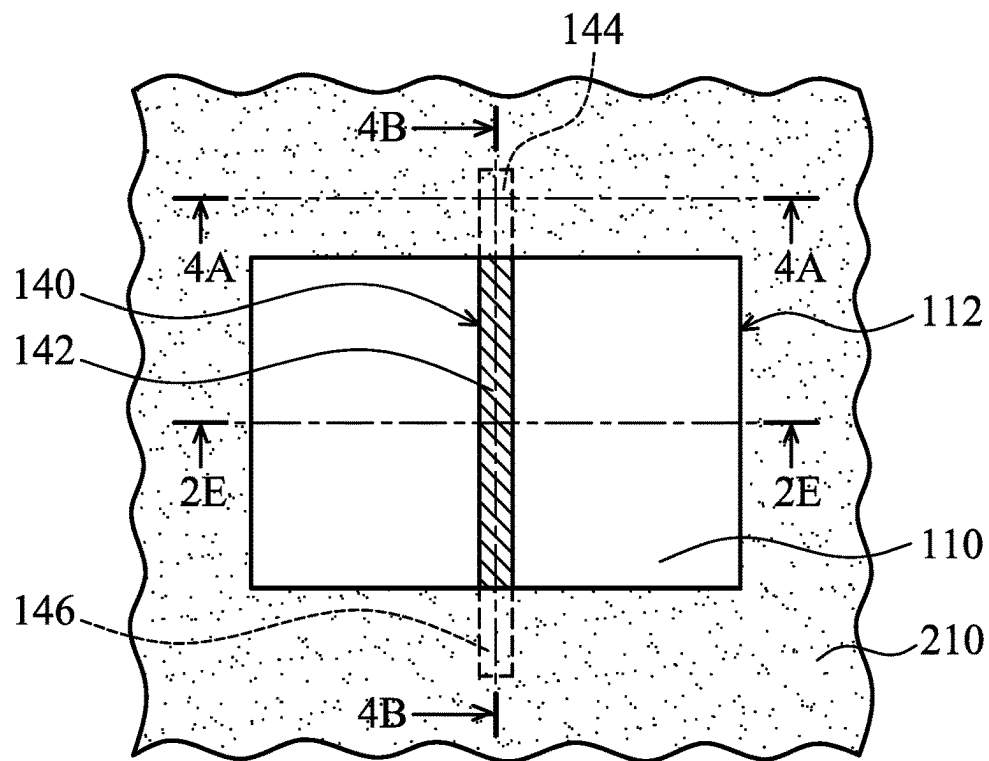


FIG. 3E

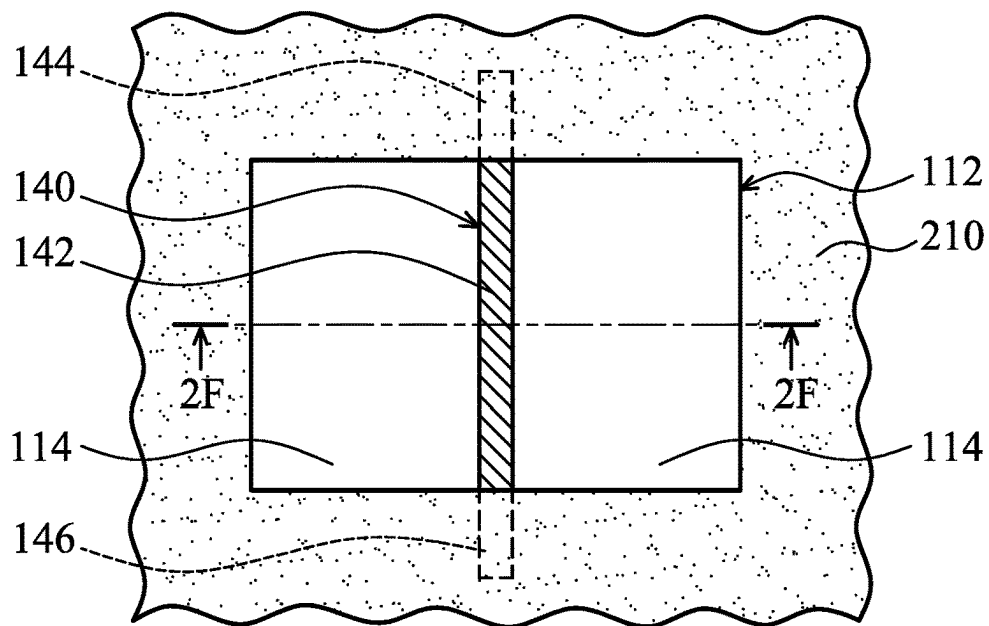


FIG. 3F

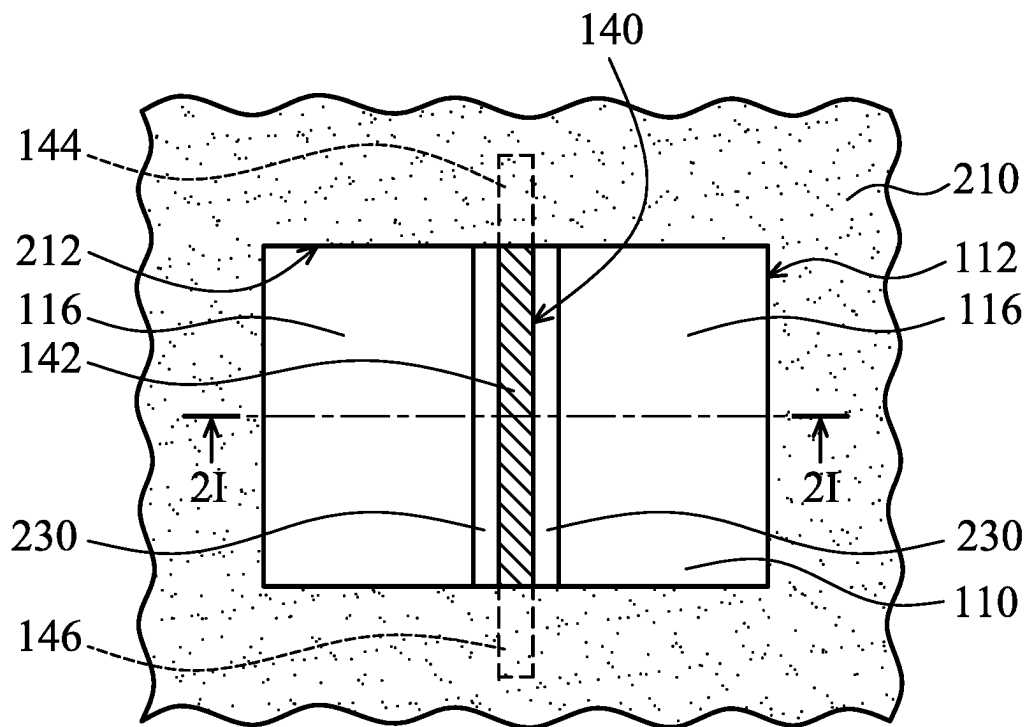


FIG. 3G

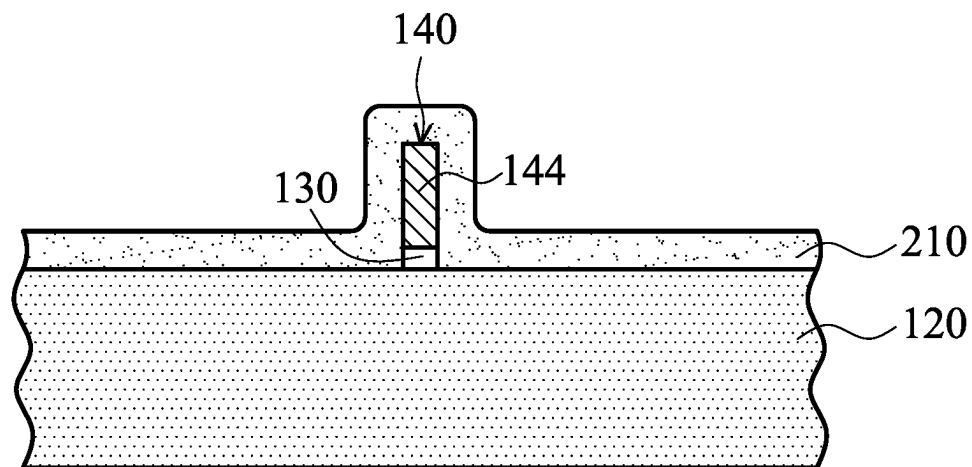


FIG. 4A

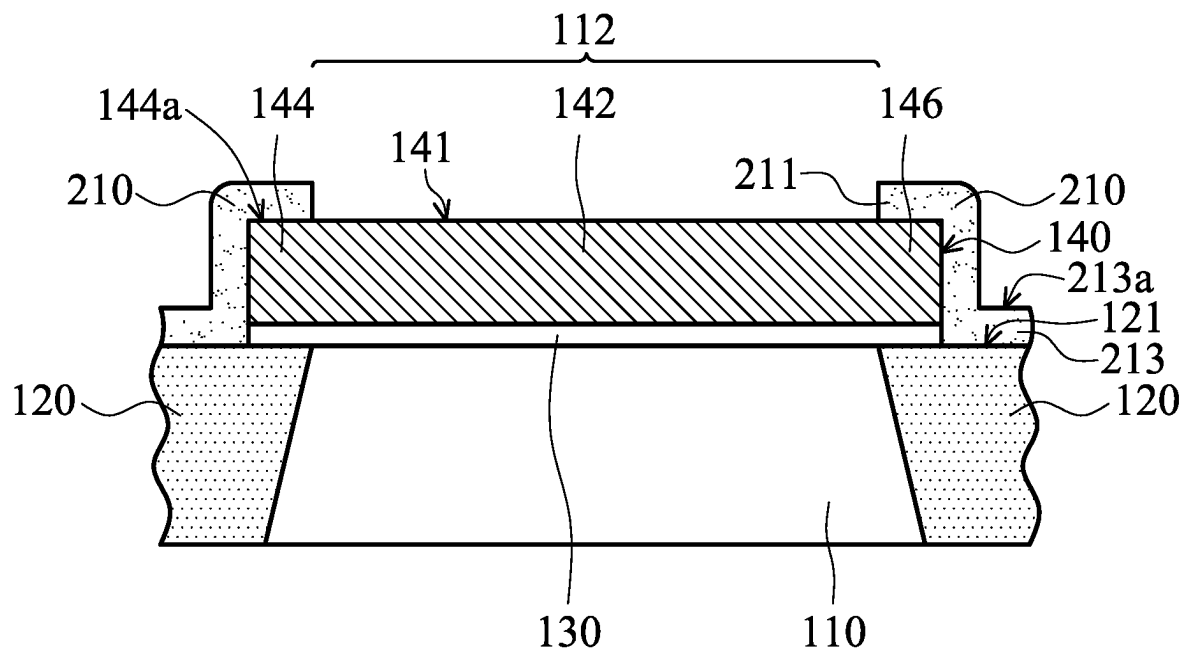


FIG. 4B

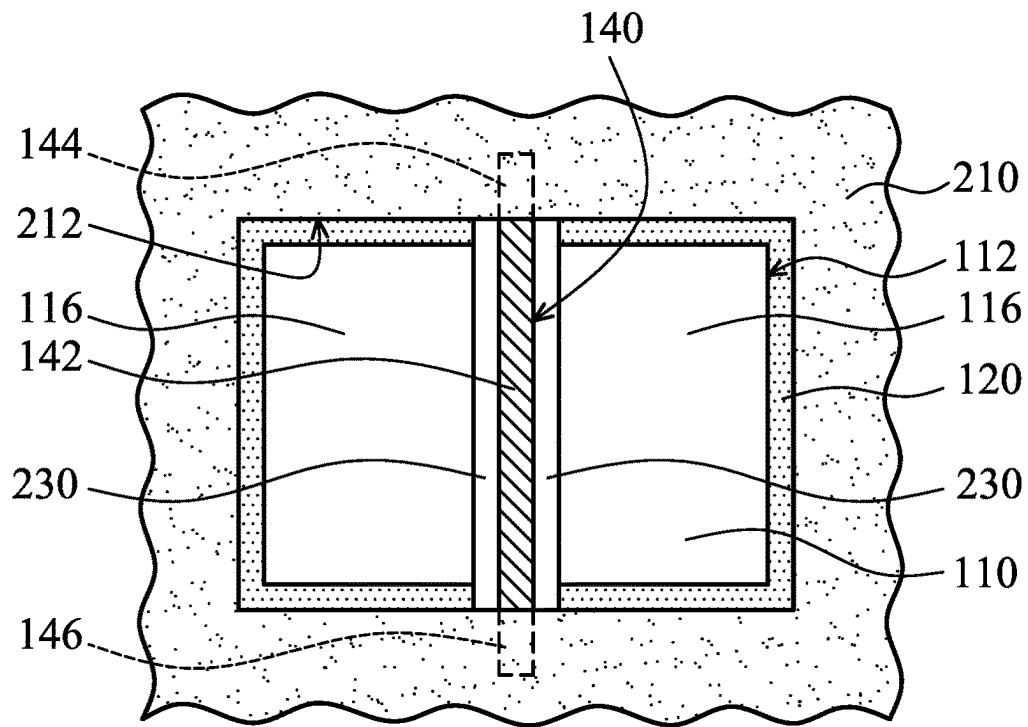


FIG. 5

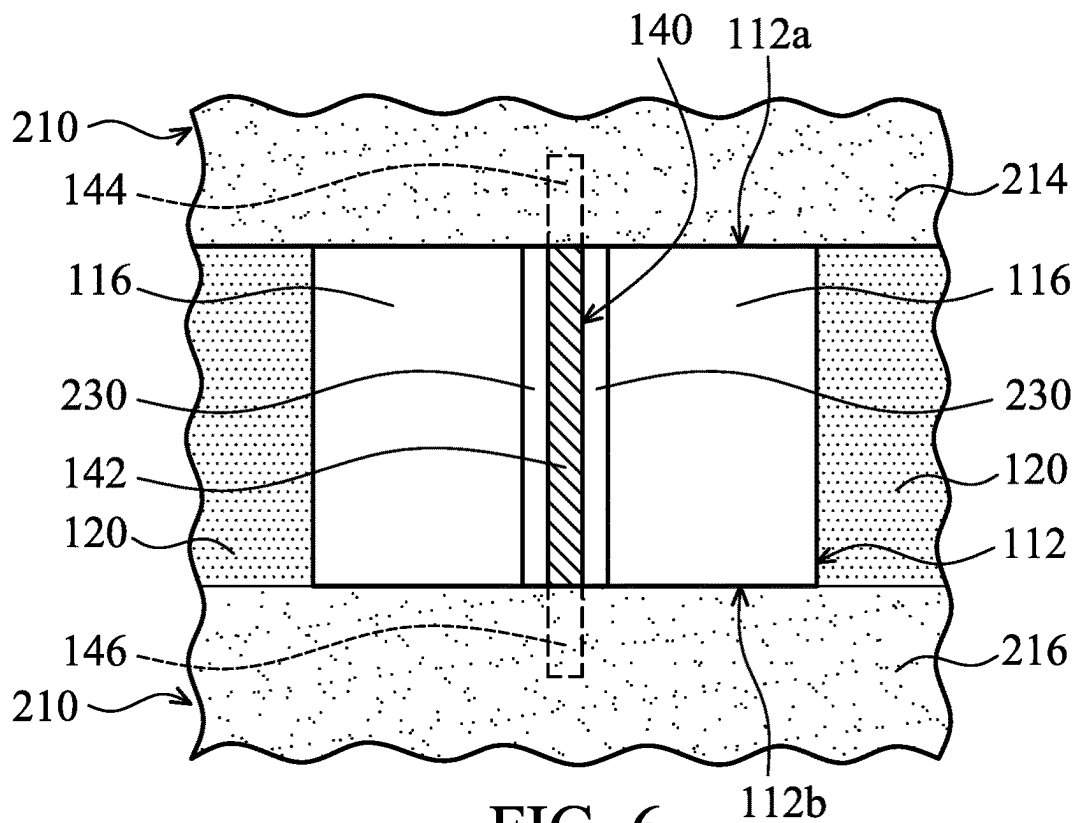


FIG. 6

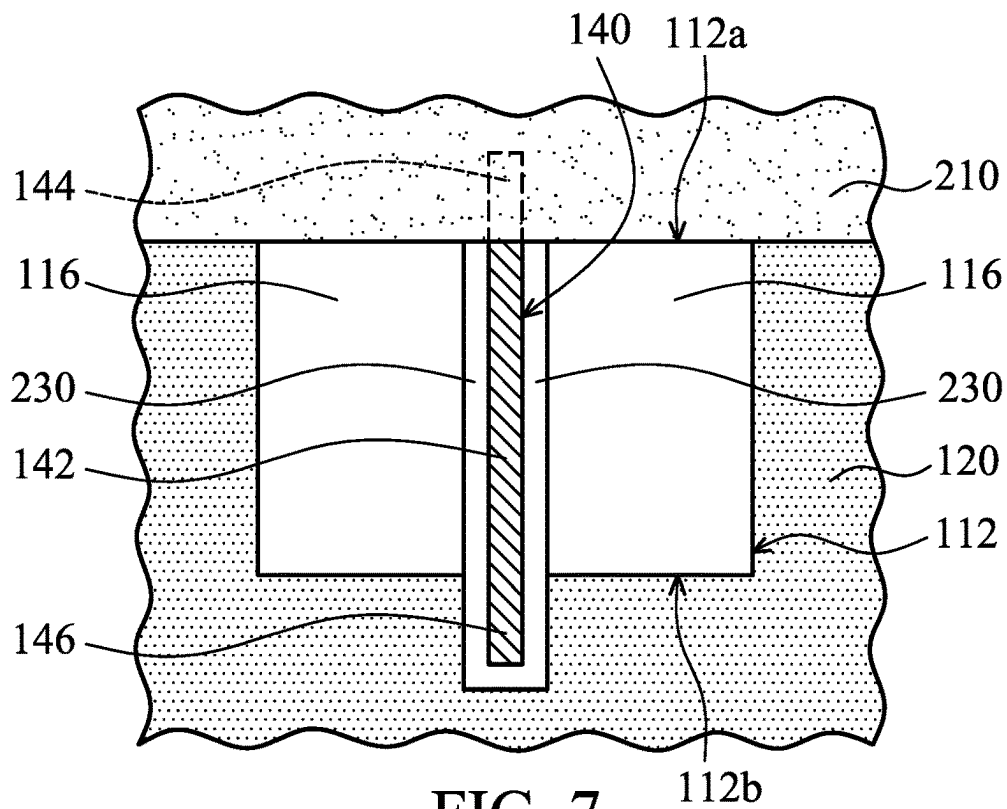


FIG. 7

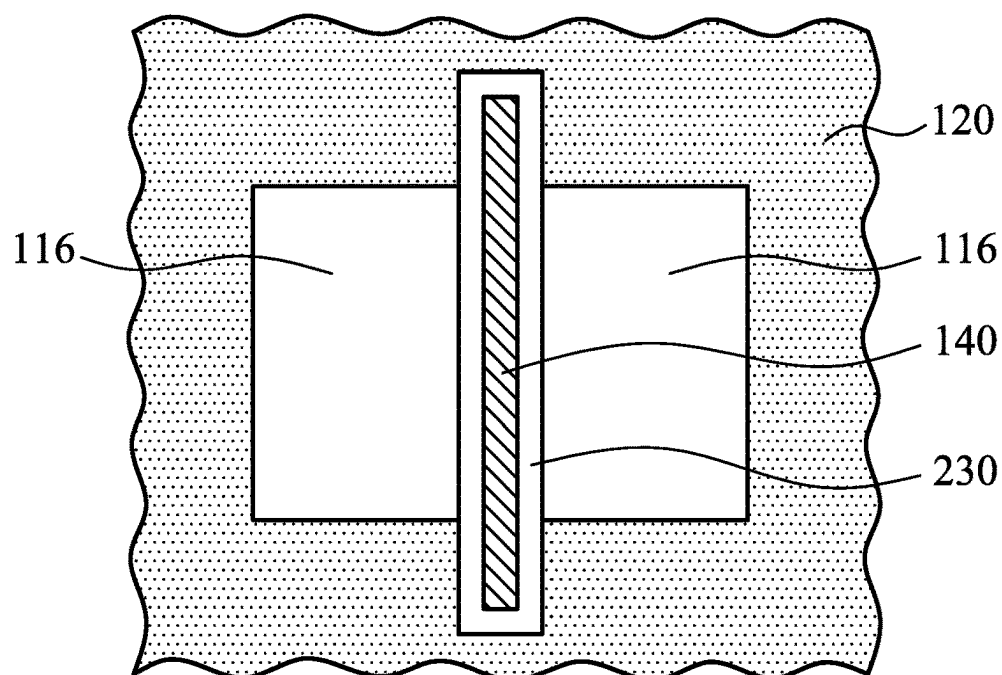


FIG. 8

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SEMICONDUCTOR DEVICE WITH GATE

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a Divisional application of U.S. patent application Ser. No. 16/892,458, filed on Jun. 4, 2020, which is a Divisional application of U.S. patent application Ser. No. 15/670,978, filed on Aug. 7, 2017, which is a Divisional application of U.S. patent application Ser. No. 14/080,313, filed on Nov. 14, 2013, the entire of which is incorporated by reference herein.

BACKGROUND

The semiconductor integrated circuit (IC) industry has experienced rapid growth. Technological advances in IC materials and design have produced generations of ICs. Each generation has smaller and more complex circuits than the previous generation. However, these advances have increased the complexity of processing and manufacturing ICs.

In the course of IC evolution, functional density (i.e., the number of interconnected devices per chip area) has generally increased while geometric size (i.e., the smallest component (or line) that can be created using a fabrication process) has decreased. This scaling-down process generally provides benefits by increasing production efficiency and lowering associated costs.

However, since the feature sizes continue to decrease, fabrication processes continue to become more difficult to perform. Therefore, it is a challenge to form reliable semiconductor devices with smaller and smaller sizes.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the embodiments, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings.

FIGS. 1A-1B are cross-sectional views of various stages of a process for forming a semiconductor device, in accordance with some embodiments.

FIGS. 2A-2I are cross-sectional views of various stages of a process for forming a semiconductor device, in accordance with some embodiments.

FIGS. 3A-3G are top views of the structures shown in FIGS. 2A-2F and 2I, respectively.

FIGS. 4A-4B are cross-sectional views of the structures along sectional lines 4A-4A and 4B-4B shown in FIG. 3E, respectively.

FIG. 5 is a top view of a semiconductor device, in accordance with some embodiments.

FIG. 6 is a top view of a semiconductor device, in accordance with some embodiments.

FIG. 7 is a top view of a semiconductor device, in accordance with some embodiments.

FIG. 8 is a top view of a semiconductor device, in accordance with some embodiments.

DETAILED DESCRIPTION OF THE ILLUSTRATIVE EMBODIMENTS

The making and using of the embodiments of the disclosure are discussed in detail below. It should be appreciated, however, that the embodiments can be embodied in a wide

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variety of specific contexts. The specific embodiments discussed are merely illustrative, and do not limit the scope of the disclosure.

It is to be understood that the following disclosure provides many different embodiments, or examples, for implementing different features of the disclosure. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. Moreover, the performance of a first process before a second process in the description that follows may include embodiments in which the second process is performed immediately after the first process, and may also include embodiments in which additional processes may be performed between the first and second processes. Various features may be arbitrarily drawn in different scales for the sake of simplicity and clarity. Furthermore, the formation of a first feature over or on a second feature in the description that follows include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact.

Some variations of the embodiments are described. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements. It is understood that additional operations can be provided before, during, and after the method, and some of the operations described can be replaced or eliminated for other embodiments of the method.

FIGS. 1A-1B are cross-sectional views of various stages of a process for forming a semiconductor device, in accordance with some embodiments. As shown in FIG. 1A, a semiconductor substrate 110 is provided. The semiconductor substrate 110 may be a semiconductor wafer (such as a silicon wafer) or a portion of a semiconductor wafer.

In some embodiments, the semiconductor substrate 110 is made of an elementary semiconductor material including silicon or germanium in a single crystal, polycrystal, or amorphous structure. In some other embodiments, the semiconductor substrate 110 is made of a compound semiconductor such as silicon carbide, gallium arsenide, gallium phosphide, indium phosphide, indium arsenide, an alloy semiconductor such as SiGe, or GaAsP, or a combination thereof. The semiconductor substrate 110 may also include multi-layer semiconductors, semiconductor on insulator (SOI) (such as silicon on insulator or germanium on insulator), or a combination thereof.

An isolation structure 120 is formed in the semiconductor substrate 110 to define various active regions 112 of the semiconductor substrate 110, and to electrically isolate neighboring devices (e.g. transistors) from one another. The isolation structure 120 surrounds the active regions 112. The isolation structure 120 may be made of a dielectric material, such as silicon oxide, silicon nitride, silicon oxynitride, fluoride-doped silicate glass (FSG), a low-K dielectric material, other suitable materials, or combinations thereof. The isolation structure 120 may be formed by using an isolation technology, such as local oxidation of semiconductor (LOCOS), shallow trench isolation (STI), or the like.

In some embodiments, the formation of the isolation structure 120 includes patterning the semiconductor substrate 110 by a photolithography process, etching a trench in the semiconductor substrate 110 (for example, by using a dry etching, wet etching, or plasma etching process, or a combination thereof), and filling the trench (for example, by using a chemical vapor deposition process) with the dielec-

tric material. In some embodiments, the filled trench may have a multi-layer structure, such as a thermal oxide liner layer filled with silicon nitride or silicon oxide.

As shown in FIG. 1A, a gate dielectric layer 130 and a gate 140 are formed over the active regions 112 of the semiconductor substrate 110. The gate dielectric layer 130 may be made of silicon oxide, silicon oxynitride, a high dielectric constant material (high-k material), or a combination thereof. The gate 140 may be made of polysilicon or other suitable materials.

Thereafter, lightly doped regions 114 are formed in the semiconductor substrate 110 by using a suitable process, such as an ion implantation process. The ion implantation process may use the gate 140 as a mask, and the lightly doped regions 114 are at two opposite sides of the gate 140. The lightly doped regions 114 may be a lightly doped source region and a lightly doped drain (LDD) region. The dopants used in the ion implantation process may include boron or phosphorus. Afterwards, a cleaning process is performed to clean away the residues formed in the ion implantation process. The cleaning process includes soaking the semiconductor substrate 110 and the gate 140 in a cleaning solution (e.g. an acid solution).

As shown in FIG. 1B, since the gate length L of the gate 140 is very short (e.g. shorter than 100 nm), the gate 140 tends to collapse in the ion implantation process if the ion implantation process is not properly performed. Besides, the gate 140 tends to collapse in the cleaning process due to the surface tension of the cleaning solution. Therefore, it is desirable to find alternative mechanisms for solving the problem mentioned above.

FIGS. 2A-2I are cross-sectional views of various stages of a process for forming a semiconductor device, in accordance with some embodiments. FIGS. 3A-3G are top views of the structures shown in FIGS. 2A-2F and 2I, respectively. FIGS. 2A-2F and 2I are cross-sectional views of the structures along sectional lines 2A-2A, 2B-2B, 2C-2C, 2D-2D, 2E-2E, 2F-2F and 2I-2I shown in FIGS. 3A-3G, respectively.

As shown in FIGS. 2A and 3A, a semiconductor substrate 110 is provided. An isolation structure 120 is formed in the semiconductor substrate 110 to define various active regions 112 of the semiconductor substrate 110, and to electrically isolate neighboring devices (e.g. transistors) from one another. A gate dielectric material layer 130a is deposited over the semiconductor substrate 110 by, for example, a chemical vapor deposition process (CVD process). Thereafter, a gate material layer 140a is deposited over the gate dielectric material layer 130a by, for example, a CVD process.

As shown in FIGS. 2B and 3B, a patterning process is performed to pattern the gate material layer 140a and the gate dielectric material layer 130a so as to form a gate 140 and a gate dielectric layer 130 under the gate 140. The gate 140 may extend across the active region 112 onto the isolation structure 120 surrounding the active region 112.

The gate 140 has an intermediate portion 142 over the active region 112 and two opposite end portions 144 and 146 over the isolation structure 120. The intermediate portion 142 is connected between the end portions 144 and 146. In some embodiments, the intermediate portion 142 and the end portions 144 and 146 have substantially the same gate length L. In some embodiments, the gate length L is shorter than or equal to about 100 nm (e.g., shorter than 60 nm, 50 nm, 40 nm, 30 nm or 20 nm). In some other embodiments, the gate length L is longer than about 100 nm. In some embodiments, the gate 140 is in a straight-line shape.

Thereafter, as shown in FIGS. 2C and 3C, a support film 210 may be deposited on the semiconductor substrate 110 to continuously cover the gate 140 and the isolation structure 120. In some embodiments, the support film 210 conformally covers the gate 140 and the isolation structure 120. The support film 210 includes silicon oxides (SiO₂), silicon oxynitrides (SiON), silicon nitrides (SiN), silicon carbonitrides (SiCN), or other suitable insulating materials. The deposition of the support film 210 includes, for example, a CVD process or a physical vapor deposition process (PVD process).

In some embodiments, the thickness T of the support film 210 ranges from about 5 Å to about 5000 Å. In some embodiments, the thickness T of the support film 210 ranges from about 5 Å to about 1000 Å. In some embodiments, the thickness T of the support film 210 ranges from about 5 Å to about 500 Å. In some embodiments, the thickness T of the support film 210 is substantially the same as the gate length L of the gate 140.

Afterwards, as shown in FIGS. 2D and 3D, a photoresist layer 220 may be formed over a portion of the support film 210 over the isolation structure 120. The photoresist layer 220 exposes another portion of the support film 210 over the active region 112. Afterwards, as shown in FIGS. 2E and 3E, an etching process is performed to remove the exposed portion of the support film 210 over the active region 112 by using the photoresist layer 220 as an etching mask. The etching process includes, for example, a dry etching process or a wet etching process. Thereafter, the photoresist layer 220 is removed.

FIGS. 4A-4B are cross-sectional views of the structures along sectional lines 4A-4A and 4B-4B of FIG. 3E, respectively. As shown in FIGS. 3E, 4A and 4B, the support film 210 may continuously cover the isolation structure 120 and the end portions 144 and 146 of the gate 140 over the isolation structure 120. The support film 210 exposes the active region 112 and the intermediate portion 142 of the gate 140 over the active region 112.

The support film 210 continuously covering the end portions 144 and 146 and the isolation structure 120 may support the gate 140 to prevent the gate 140 from collapsing in the subsequent processes (such as ion implantation processes and/or cleaning processes). The support film 210 has a first part 211 and a second part 213, and the second part 213 has a fourth top surface 213a. The gate 140 has a first top surface 141. The isolation structure 120 has a second top surface 121. The end portion 144 of the gate 140 has a fifth top surface 144a.

Thereafter, as shown in FIGS. 2F and 3F, lightly doped regions 114 are formed in the semiconductor substrate 110 by using a suitable process, such as an ion implantation process. The ion implantation process may be performed to introduce p-type impurities (e.g., boron) or n-type impurities (e.g., phosphorus) into the semiconductor substrate 110. The lightly doped regions 114 may be a lightly doped source region and a lightly doped drain (LDD) region. The lightly doped regions 114 may be located at two opposite sides of the intermediate portion 142. Afterwards, a cleaning process is performed to clean away the residues formed in the ion implantation process.

Afterwards, as shown in FIG. 2G, a spacer layer 230 may be deposited on the semiconductor substrate 110 by using, for example, a CVD process. The spacer layer 230 includes insulating materials, such as silicon oxides or silicon nitrides.

Thereafter, as shown in FIG. 2H, an anisotropic etching process (e.g. a dry etching process) is performed to remove

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a portion of the spacer layer **230**. The remaining spacer layer **230** is over the sidewalls **148** and **132** of the gate **140** and the gate dielectric layer **130**. The remaining spacer layer **230** over the sidewalls **148** and **132** may be configured to electrically isolate the gate **140** from other devices and to act as a mask layer in a subsequent ion implantation process.

Thereafter, as shown in FIGS. **2I** and **3G**, heavily doped regions **116** are formed in the semiconductor substrate **110** by using a suitable process, such as an ion implantation process. The ion implantation process may be performed to introduce p-type impurities (e.g., boron) or n-type impurities (e.g., phosphorus) into the semiconductor substrate **110**.

The heavily doped regions **116** may be a heavily doped source region and a heavily doped drain region. The heavily doped regions **116** may be located at the two opposite sides of the intermediate portion **142**. The gate **140**, the gate dielectric layer **130**, the spacer layer **230**, the lightly doped regions **114** and the heavily doped regions **116** may constitute a transistor device.

In some embodiments, the support film **210** surrounds the active region **112**. In some embodiments, the support film **210** is a continuous film and continuously surrounds the active region **112**. In some embodiments, the edge **212** of the support film **210** is aligned with the edge of the active region **112**. In some embodiments, the edge **212** of the support film **210** is spaced from the edge of the active region **112** (as shown in FIG. **5**). The support film **210** exposes the active region **112** and the intermediate portion **142** of the gate **140** to prevent the support film **210** from retarding the formation of the lightly doped regions **114** and the heavily doped regions **116**.

In some embodiments, the support film **210** covers the whole isolation structure **120** (as shown in FIG. **3G**). In some other embodiments, the support film **210** merely covers a portion of the isolation structure **120** (as shown in FIGS. **6** and **7**). The support film **210** may be, for example, in a bar shape (as shown in FIGS. **6** and **7**).

As shown in FIG. **6**, the support film **210** has two portions **214** and **216** separated from each other and located at two opposite sides **112a** and **112b** of the active region **112**. The portion **214** continuously covers the isolation structure **120** and the end portion **144**. The portion **216** continuously covers the isolation structure **120** and the end portion **146**. As shown in FIG. **7**, the support film **210** is located at only one side **112a** of the active region **112** and continuously covers the isolation structure **120** and the end portion **144**.

FIG. **8** is a top view of a semiconductor device, in accordance with some embodiments. As shown in FIG. **8**, after the formation of the lightly doped regions **114** and the cleaning process (as shown in FIGS. **2F** and **3F**), the support film **210** may be removed, and then the steps of FIGS. **2G-2I** are subsequently performed.

Embodiments of mechanisms for forming a semiconductor device as described above include forming a support film over an isolation structure in a semiconductor substrate to cover the isolation structure and at least one end portion of a gate over the isolation structure. Therefore, the support film may support the gate to prevent the gate from collapsing in the subsequent processes.

In accordance with some embodiments, a semiconductor device is provided. The semiconductor device includes a semiconductor substrate. The semiconductor device includes an isolation structure in the semiconductor substrate. The isolation structure surrounds an active region of the semiconductor substrate. The semiconductor device includes a gate over the semiconductor substrate. The gate is across the active region and extends onto the isolation

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structure. The semiconductor device includes a support film over the isolation structure. The support film is a continuous film which continuously covers the isolation structure and the gate over the isolation structure, the support film conformally covers a first portion of a first top surface and a second portion of a first sidewall of the gate and a second top surface of the isolation structure, the first top surface and the second top surface face away from the semiconductor substrate, the entire support film and an entire topmost surface of the active region do not overlap with each other, the topmost surface of the active region faces the gate, the support film has a first part and a second part, the first part is over the first top surface, the second part is over the second top surface, a first distance between a third top surface of the first part and the second top surface is greater than a second distance between a fourth top surface of the second part and the second top surface, and the first distance and the second distance are measured along an axis perpendicular to the second top surface.

In accordance with some embodiments, a semiconductor device is provided. The semiconductor device includes. The semiconductor device includes a semiconductor substrate. The semiconductor device includes an isolation structure in the semiconductor substrate. The isolation structure surrounds an active region of the semiconductor substrate. The semiconductor device includes a gate over the semiconductor substrate. The gate is across the active region and extends onto the isolation structure. The semiconductor device includes a patterned insulating layer over the semiconductor substrate, the gate, and the isolation structure and exposing an intermediate portion of the gate and the active region. The patterned insulating layer is over a first top surface and a sidewall of the gate and a second top surface of the isolation structure, the first top surface and the second top surface face away from the semiconductor substrate, the entire patterned insulating layer and an entire topmost surface of the active region do not overlap with each other, the topmost surface of the active region faces the gate, the patterned insulating layer has a first part and a second part, the first part is over the first top surface, the second part is over the second top surface, and the second part is between the first part and the isolation structure along an axis perpendicular to the second top surface.

In accordance with some embodiments, a semiconductor device is provided. The semiconductor device includes a semiconductor substrate. The semiconductor device includes an isolation structure in the semiconductor substrate. The isolation structure surrounds an active region of the semiconductor substrate. The semiconductor device includes a gate over the semiconductor substrate. The gate is across the active region and extends onto the isolation structure, the gate has an intermediate portion and a first end portion, the intermediate portion is over the active region, and the first end portion is over the isolation structure. The semiconductor device includes a support film over the isolation structure and the first end portion. The support film continuously covers a first top surface and a first sidewall of the first end portion and a second top surface of the isolation structure, the first top surface and the second top surface face away from the semiconductor substrate, the support film is spaced apart from the active region, a portion of the support film covering the gate has an inverted U shape in a cross-sectional view of the support film and the gate, the support film has a first part and a second part, and the first part is higher than the second part in a direction perpendicular to the second top surface.

Although the embodiments and their advantages have been described in detail, it should be understood that various changes, substitutions, and alterations can be made herein without departing from the spirit and scope of the embodiments as defined by the appended claims. Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods, and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the disclosure. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps. In addition, each claim constitutes a separate embodiment, and the combination of various claims and embodiments are within the scope of the disclosure.

What is claimed is:

1. A semiconductor device, comprising:

a semiconductor substrate;

an isolation structure in the semiconductor substrate, wherein the isolation structure surrounds an active region of the semiconductor substrate;

a gate over the semiconductor substrate, wherein the gate is across the active region and extends onto the isolation structure, and the gate has a first sidewall across the active region and extending onto the isolation structure;

a spacer layer covering a middle portion of the first sidewall and across a boundary between the active region and the isolation structure; and

a support film over the isolation structure, wherein the support film is a continuous film which continuously covers the isolation structure and the gate over the isolation structure, the support film conformally covers a first portion of a first top surface and a second portion of a second sidewall of the gate and a second top surface of the isolation structure, the first top surface and the second top surface face away from the semiconductor substrate, the entire support film and an entire topmost surface of the active region do not overlap with each other, the topmost surface of the active region faces the gate,

the support film has a third top surface, a first inner wall, and a second inner wall, the first inner wall and the second inner wall face each other and are connected to the third top surface, the entire topmost surface of the active region and the entire spacer layer are between the first inner wall and the second inner wall in a top view of the active region, the spacer layer, and the support film, a first distance between the first inner wall and the second inner wall is substantially equal to a first length of the spacer layer, the first length is measured in a direction from the first inner wall toward the second inner wall,

the gate has a corner between the first top surface and the second sidewall, the support film has a corner part wrapped around the corner, the corner part is connected to the first part, and the corner part has a convex curved surface facing away from the corner.

2. The semiconductor device as claimed in claim 1, wherein the support film has an opening, and the opening exposes an intermediate portion of the gate and the active region.

3. The semiconductor device as claimed in claim 2, wherein the opening further exposes a third portion of the isolation structure adjacent to the active region.

4. The semiconductor device as claimed in claim 3, wherein the third portion surrounds the active region.

5. The semiconductor device as claimed in claim 3, wherein the opening further exposes a fourth portion of the isolation structure, and the active region is between the third portion and the fourth portion.

6. The semiconductor device as claimed in claim 1, wherein the spacer layer is in direct contact with the support film.

7. The semiconductor device as claimed in claim 6, wherein the spacer layer is in direct contact with the isolation structure.

8. The semiconductor device as claimed in claim 1, wherein a portion of the support film covering the gate has an inverted U shape in a cross-sectional view of the support film and the gate.

9. The semiconductor device as claimed in claim 1, wherein the support film has an opening exposing a portion of the isolation structure, and the portion of the isolation structure has a U shape in a top view of the support film and the isolation structure.

10. The semiconductor device as claimed in claim 1, wherein a third portion of the third top surface of the support film is higher than the first top surface of the gate relative to the second top surface of the isolation structure.

11. The semiconductor device as claimed in claim 1, wherein the spacer layer overlaps a topmost portion of the isolation structure in a top view of the spacer layer and the isolation structure.

12. A semiconductor device, comprising:

a semiconductor substrate;

an isolation structure in the semiconductor substrate, wherein the isolation structure surrounds an active region of the semiconductor substrate;

a gate over the semiconductor substrate, wherein the gate is across the active region and extends onto the isolation structure, and the gate has a first sidewall across the active region and extending onto the isolation structure;

a spacer layer covering a middle portion of the first sidewall and across a boundary between the active region and the isolation structure; and

a patterned insulating layer over the semiconductor substrate, the gate, and the isolation structure and exposing an intermediate portion of the gate and the active region, wherein the patterned insulating layer is over a first top surface and a second sidewall of the gate and a second top surface of the isolation structure, the first top surface and the second top surface face away from the semiconductor substrate, the entire patterned insulating layer and an entire topmost surface of the active region do not overlap with each other, the topmost surface of the active region faces the gate,

the patterned insulating layer has a third top surface, a first inner wall, and a second inner wall, the first inner wall and the second inner wall face each other and are connected to the third top surface, the entire topmost surface of the active region and the entire spacer layer are between the first inner wall and the second inner wall in a top view of the active region, the spacer layer,

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and the patterned insulating layer, the spacer layer has a first end surface and a second end surface, the first end surface is substantially level with the first inner wall and faces away from the second inner wall, and the second end surface is substantially level with the second inner wall and faces away from the first inner wall.

13. The semiconductor device as claimed in claim 12, wherein the patterned insulating layer is a continuous film which continuously covers the second top surface of the isolation structure and the first top surface and the second sidewall of the gate over the isolation structure.

14. The semiconductor device as claimed in claim 13, wherein the patterned insulating layer conformally covers the isolation structure and the first top surface and the second sidewall of the gate over the isolation structure.

15. The semiconductor device as claimed in claim 12, wherein the patterned insulating layer has an opening, and the opening is wider than the active region as measured along an axis perpendicular to a longitudinal axis of the gate.

16. The semiconductor device as claimed in claim 15, wherein the opening exposes the intermediate portion, the active region and a portion of the isolation structure.

17. The semiconductor device as claimed in claim 16, wherein the portion of the isolation structure continuously surrounds the active region.

18. A semiconductor device, comprising:

a semiconductor substrate;

an isolation structure in the semiconductor substrate, wherein the isolation structure surrounds an active region of the semiconductor substrate;

a gate over the semiconductor substrate, wherein the gate is across the active region and extends onto the isolation structure, the gate has an intermediate portion and a first end portion, the intermediate portion is over the active region, the first end portion is over the isolation

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structure, and the gate has a first sidewall across the active region and extending onto the isolation structure;

a spacer layer covering a middle portion of the first sidewall and across a boundary between the active region and the isolation structure; and

a support film over the isolation structure and the first end portion, wherein the support film continuously covers a first top surface and a second sidewall of the first end portion and a second top surface of the isolation structure, the first top surface and the second top surface face away from the semiconductor substrate, the support film is spaced apart from the active region, the support film has a third top surface, a first inner wall, and a second inner wall, the first inner wall and the second inner wall face each other and are connected to the third top surface, an entire topmost surface of the active region and the entire spacer layer are between the first inner wall and the second inner wall in a top view of the active region, the spacer layer, and the support film, the spacer layer extends from the first inner wall to the second inner wall, the spacer layer has a third sidewall, the second sidewall and the third sidewall face away from the second inner wall, and the third sidewall is closer to the second inner wall than the second sidewall.

19. The semiconductor device as claimed in claim 18, wherein the gate further has a second end portion over the isolation structure, the support film further continuously covers a fourth top surface and a fourth sidewall of the second end portion, and the fourth top surface faces away from the semiconductor substrate.

20. The semiconductor device as claimed in claim 18, wherein the support film conformally covers the isolation structure and the first top surface and the second sidewall of the first end portion.

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