

US Patent & Trademark Office

Patent Public Search | Text View

United States Patent Application Publication

20250268027

Kind Code

A1

Publication Date

August 21, 2025

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DISPLAY DEVICE

Abstract

According to one embodiment, a display device includes an organic insulating layer disposed on a first inorganic insulating layer, a second inorganic insulating layer disposed on the organic insulating layer and overlapping a circumferential edge portion of a lower electrode, an organic layer disposed on the lower electrode, metal layers disposed on the first inorganic insulating layer, and second metal layers disposed on the second inorganic insulating layer. The organic insulating layer includes first slits in which the second inorganic insulating layer and the first inorganic insulating layer are in contact with each other.

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Appl. No.: 19/050147

Filed: February 11, 2025

Foreign Application Priority Data

JP 2024-022858

Feb. 19, 2024

Publication Classification

Int. Cl.: H10K59/122 (20230101); H10K59/131 (20230101)

U.S. Cl.:

CPC H10K59/122 (20230201); H10K59/131 (20230201);

Background/Summary

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2024-022858, filed Feb. 19, 2024, the entire contents of which are incorporated herein by reference.

FIELD

[0002] Embodiments described herein relate generally to a display device.

BACKGROUND

[0003] In recent years, display devices in which organic light emitting diodes (OLEDs) are applied as display elements have been put to practical use. These display elements comprise a pixel circuit that contains a thin-film transistor, a lower electrode connected to the pixel circuit, an organic layer that covers the lower electrode, and an upper electrode that covers the organic layer. The organic layer includes a light emitting layer and, in addition, functional layers such as a hole transport layer and an electron transport layer. In such display devices, there is a need for technology to suppress a decrease in reliability.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1 is a diagram showing a configuration example of a display device according to the first embodiment.

[0005] FIG. 2 is a diagram showing an example of layout of subpixels.

[0006] FIG. 3 is a cross-sectional view schematically showing the display device taken along the line III-III in FIG. 2.

[0007] FIG. 4 is a plan view showing a configuration example of a region including a plurality of pads in the display device shown in FIG. 1.

[0008] FIG. 5 is a plan view showing a configuration example of a region including a plurality of pads in the display device shown in FIG. 1.

[0009] FIG. 6 is a plan view showing a metal layer shown in FIG. 5.

[0010] FIG. 7 is a cross-sectional view showing the display device taken along the line VII-VII in FIG. 5.

[0011] FIG. 8 is a cross-sectional view showing the display device taken along the line VIII-VIII in FIG. 5.

[0012] FIG. 9 is a plan view showing a configuration example of a region including a plurality of pads in a display device according to a comparative example.

[0013] FIG. 10 is a cross-sectional view showing the display device taken along the line X-X in FIG. 9.

[0014] FIG. 11 is a cross-sectional view showing the display device taken along the line XI-XI in FIG. 9.

[0015] FIG. 12 is a plan view showing a configuration example of a region including a plurality of pads in a display device according to the second embodiment.

[0016] FIG. 13 is a cross-sectional view showing the display device taken along the line XIII-XIII in FIG. 12.

[0017] FIG. 14 is a cross-sectional view showing the display device taken along the line XIV-XIV in FIG. 12.

[0018] FIG. 15 is a plan view showing a configuration example of a region including a plurality of pads in a display device according to the third embodiment.

[0019] FIG. **16** is a plan view showing a configuration example of a region including a plurality of pads in a display device according to the third embodiment.

[0020] FIG. **17** is a cross-sectional view showing the display device taken along the line XVII-XVII in FIG. **16**.

[0021] FIG. **18** is a cross-sectional view showing the display device taken along the line XVIII-XVIII in FIG. **16**.

[0022] FIG. **19** is a plan view showing a configuration example of a region including a plurality of pads in a display device according to the fourth embodiment.

[0023] FIG. **20** is a cross-sectional view showing the display device taken along the line XX-XX in FIG. **19**.

[0024] FIG. **21** is a cross-sectional view showing the display device taken along the line XXI-XXI in FIG. **19**.

DETAILED DESCRIPTION

[0025] In general, according to one embodiment, a display device comprises a substrate, a first inorganic insulating layer disposed above the substrate and over a display area which displays images and a peripheral area which surrounds the display area, an organic insulating layer disposed on the first inorganic insulating layer, a lower electrode disposed on the organic insulating layer in the display area, a second inorganic insulating layer disposed on the organic insulating layer and overlapping a circumferential edge portion of the lower electrode, an organic layer disposed on the lower electrode, an upper electrode disposed on the organic layer, a plurality of first metal layers disposed on the first inorganic insulating layer and aligned in a first direction along an end of the substrate, in the peripheral area, and a plurality of second metal layers disposed on the second inorganic insulating layer and electrically connected to the first metal layers.

[0026] The second inorganic insulating layer comprises a plurality of first apertures overlapping the second metal layers, respectively, and the organic insulating layer comprises a plurality of second apertures overlapping the plurality of first apertures, respectively, via which the first metal layers and the second metal layers are in contact respectively with each other, and a plurality of first slits each formed between a respective adjacent pair of the plurality of second apertures, via which the second inorganic insulating layer and the first inorganic insulating layer are in contact with each other.

[0027] According to another embodiment, a display device comprises a substrate, a first inorganic insulating layer disposed above the substrate and over a display area which displays images and a peripheral area which surrounds the display area, an organic insulating layer disposed on the first inorganic insulating layer, a lower electrode disposed on the organic insulating layer in the display area, a second inorganic insulating layer disposed on the organic insulating layer and overlapping a circumferential edge portion of the lower electrode, an organic layer disposed on the lower electrode, an upper electrode disposed on the organic layer, a plurality of first metal layers disposed on the first inorganic insulating layer and aligned in a first direction along an end of the substrate, in the peripheral area, and a plurality of second metal layers disposed on the second inorganic insulating layer and electrically connected to the first metal layers.

[0028] The second inorganic insulating layer comprises a third aperture, and the third aperture overlaps the plurality of first metal layers.

[0029] According to still another embodiment, a display device comprises a substrate, a first inorganic insulating layer disposed above the substrate and over a display area which displays images and a peripheral area which surrounds the display area, an organic insulating layer disposed on the first inorganic insulating layer, a lower electrode disposed on the organic insulating layer in the display area, a second inorganic insulating layer disposed on the organic insulating layer and overlapping a circumferential edge portion of the lower electrode, an organic layer disposed on the lower electrode, an upper electrode disposed on the organic layer, and a plurality of first metal layers disposed on the first inorganic insulating layer and aligned in a first direction along an end of

the substrate, in the peripheral area. The organic insulating layer includes a slit formed along the first direction and disposed between the lower electrode and the plurality of first metal layers, in the peripheral area.

[0030] With configurations such as described above, it is possible to provide a display device which can suppress the increase in reliability.

[0031] Embodiments will be described hereinafter with reference to the accompanying drawings. Note that the disclosure is merely an example, and proper changes within the spirit of the invention, which are easily conceivable by a skilled person, are included in the scope of the invention as a matter of course.

[0032] In addition, in some cases, in order to make the description clearer, the widths, thicknesses, shapes, etc., of the respective parts are schematically illustrated in the drawings, compared to the actual modes. However, the schematic illustration is merely an example, and adds no restrictions to the interpretation of the invention. Besides, in the specification and drawings, the same or similar elements as or to those described in connection with preceding drawings or those exhibiting similar functions are denoted by like reference numerals, and a detailed description thereof is omitted unless otherwise necessary.

[0033] Note that, in order to make the descriptions more easily understandable, some of the drawings illustrate an X axis, a Y axis and a Z axis orthogonal to each other. A direction along the X axis is referred to as a first direction X, a direction along the Y axis is referred to as a second direction Y and a direction along the Z axis is referred to as a third direction Z. Further, viewing the constitutional elements parallel to the Z direction is referred to as plan view.

[0034] In the following explanations, the expression “overlapping” refers not only to cases where other elements overlap the target element from the third direction Z, but also to cases where other elements overlap the target element from a direction opposite to the third direction Z. Further, the expression “overlapping” refers not only to cases where the target elements are directly in contact with each other, but also to cases where the target elements are spaced apart from each other or where some other element is located between the target elements.

[0035] The display device of each of the embodiments is an organic electroluminescent display device equipped with an organic light emitting diode (OLED) as a display element, and can be mounted in various electronic devices such as TVs, personal computers, in-vehicle equipment, tablet terminals, smartphones, cell phone terminals, wearable terminals and the like.

First Embodiment

[0036] FIG. 1 is a diagram showing a configuration example of a display device DSP according to this embodiment. The display device DSP comprises a display panel PNL. The display panel PNL includes an insulating substrate 10. The substrate 10 may be glass or a flexible resin film.

[0037] In this embodiment, the shape of the substrate 10 is rectangular that is elongated along the second direction Y when viewed in plan view. Note here that the shape of the substrate 10 in plan view is not limited to rectangular, and may as well be some other shape such as square, circle or oval.

[0038] The display panel PNL includes a display area DA that displays images and a peripheral area SA around the display area DA on the substrate 10. The display area DA comprises a plurality of pixels PX arranged along a matrix along the first direction X and the second direction Y.

[0039] The pixels PX each include a plurality of subpixels SP. For example, each of the pixels PX contains a subpixel SP1 of a first color, a subpixel SP2 of a second color, and a subpixel SP3 of a third color. The first color, the second color, and the third color are different from each other. Note that each of the pixels PX may as well contain a subpixel SP of another color such as white, together with the subpixels SP1, SP2, and SP3, or in place of any of the subpixels SP1, SP2, and SP3.

[0040] The subpixel SP comprises a pixel circuit 1 and a display element 20 driven by the pixel circuit 1. The pixel circuit 1 comprises a pixel switch 2, a drive transistor 3, and a capacitor 4. The

pixel switch **2** and the drive transistor **3** are switching elements, for example, constituted by thin film transistors.

[0041] A gate electrode of the pixel switch **2** is connected to a respective scanning line GL. One of a source electrode and a drain electrode of the pixel switch **2** is connected to a respective signal line SL, and the other is connected to the gate electrode of the drive transistor **3** and the capacitor **4**. In the drive transistor **3**, one of the source electrode and the drain electrode is connected to a power supply line PL and the capacitor **4**, and the other is connected to an anode of the display element **20**.

[0042] Note that the configuration of the pixel circuit **1** is not limited to that of the example illustrated in the figure. For example, the pixel circuit **1** may as well contain more thin film transistors and capacitors. The display element **20** is an organic light emitting diode (OLED) as a light emitting element, and may as well be referred to as an organic EL element.

[0043] The display device DSP has a plurality of pads PD in the peripheral area SA. The plurality of pads PD constitute, for example, a pad for the touch panel. The plurality of pads PD are arranged in one direction along a panel edge PNLE. Here, the edge includes the end and the region in the vicinity thereof. The panel edge PNLE includes an edge of the substrate **10**. In this embodiment, the direction along the edge of the substrate **10** corresponds to the first direction X.

[0044] Each of the pads PD extends along the second direction Y, but configuration is not limited to this. For example, some of the plurality of pads PD may as well extend in a diagonal direction. The pads PD are, for example, constituted by a plurality of metal layers, which will be described later. These pads PD are electrically connected to, for example, a flexible printed circuit board FPC shown by dotted lines.

[0045] FIG. **2** shows an example of the layout of subpixels SP**1**, SP**2**, and SP**3**. In the example illustrated in FIG. **2**, the subpixel SP**2** and the subpixel SP**3** are aligned along the second direction Y. The subpixel SP**1** and the subpixel SP**2** are aligned along the first direction X, and the subpixel SP**1** and the subpixel SP**3** are aligned along the first direction X.

[0046] When the subpixels SP**1**, SP**2**, and SP**3** are arranged in such a layout as described above in the display area DA, rows in which subpixels SP**2** and subpixels SP**3** are arranged alternately along the second direction Y, and rows in which a plurality of subpixels SP**1** are arranged along the second direction Y are formed. These rows are arranged alternately along the first direction X.

[0047] Note here that the layout of the subpixels SP**1**, SP**2**, and SP**3** is not limited to that of the example illustrated in FIG. **2**. As another example, the subpixels SP**1**, SP**2**, and SP**3** in each pixel PX may as well be disposed in order along the first direction X.

[0048] In the display area DA, an insulating layer **5** and a partition **6** are provided. The insulating layer **5** has apertures AP**1**, AP**2**, and AP**3** in the subpixels SP**1**, SP**2**, and SP**3**, respectively. The insulating layer **5** with these apertures AP**1**, AP**2**, and AP**3** may as well be referred to as a rib in some cases.

[0049] The partition **6** overlaps the insulating layer **5** in plan view. The partition **6** is formed into a grid pattern surrounding the apertures AP**1**, AP**2**, and AP**3**. It may as well be said that the partition **6** have apertures in the subpixels SP**1**, SP**2**, and SP**3** as in the case of the insulating layer **5**.

[0050] The subpixels SP**1**, SP**2**, and SP**3** comprise display elements **201**, **202**, and **203**, respectively, as the display elements **20**. The display element **201** of the subpixel SP**1** has a lower electrode LE**1**, an upper electrode UE**1**, and an organic layer OR**1** each overlapping the respective aperture AP**1**. Circumferential edge portions of the lower electrode LE**1**, the organic layer OR**1**, and the upper electrode UE**1** overlap the insulating layer **5** in plan view. Note here that the circumferential edge portions include the edges and the regions in the vicinity thereof.

[0051] The display element **202** of the subpixel SP**2** comprises a lower electrode LE**2**, an upper electrode UE**2**, and an organic layer OR**2** each overlapping the respective aperture AP**2**. The circumferential edge portions of the lower electrode LE**2**, the organic layer OR**2**, and the upper electrode UE**2** overlap the insulating layer **5** in plan view.

[0052] The display element **203** of the subpixel **SP3** comprises a lower electrode **LE3**, an upper electrode **UE3**, and an organic layer **OR3** each overlapping the respective aperture **AP3**. The circumferential edge portions of the lower electrode **LE3**, the organic layer **OR3**, and the upper electrode **UE3** overlap the insulating layer **5** in plan view.

[0053] In the example illustrated in FIG. **2**, the outlines of the lower electrodes **LE1**, **LE2**, and **LE3** are indicated as dotted lines, and the outlines of the organic layers **OR1**, **OR2**, and **OR3** and the upper electrodes **UE1**, **UE2**, and **UE3** are indicated as alternate long and short dash lines. Note that the outlines of the lower electrodes, the organic layers, and the upper electrodes shown in the figure may not necessarily be those reflected by the actual shapes.

[0054] The lower electrodes **LE1**, **LE2**, and **LE3** correspond to the anodes of the display elements, for example. The upper electrodes **UE1**, **UE2**, and **UE3** correspond to the cathodes or common electrodes of the display elements, respectively.

[0055] The lower electrode **LE1** is connected to the pixel circuit **1** of the subpixel **SP1** (as shown in FIG. **1**) via a contact hole **CH1**. The lower electrode **LE2** is connected to the pixel circuit **1** of the subpixel **SP2** via a contact hole **CH2**. The lower electrode **LE3** is connected to the pixel circuit **1** of the subpixel **SP3** via a contact hole **CH3**.

[0056] In the example illustrated in FIG. **2**, the areas of the apertures **AP1**, **AP2**, and **AP3** are different from each other. The area of the aperture **AP1** is larger than the area of the aperture **AP2**, and the area of the aperture **AP2** is larger than the area of the aperture **AP3**. In other words, the area of the lower electrode **LE1** exposed through the aperture **AP1** is larger than the area of the lower electrode **LE2** exposed through the aperture **AP2**, and the area of the lower electrode **LE2** exposed through the aperture **AP2** is larger than the area of the lower electrode **LE3** exposed through the aperture **AP3**.

[0057] FIG. **3** is a cross-sectional view schematically showing the display device **DSP** taken along the line III-III in FIG. **2**. The circuit layer **11** is disposed on the substrate **10**. The circuit layer **11** includes various circuits such as the pixel circuit **1** and the like and various wiring such as the scanning line **GL**, the signal line **SL**, and the power line **PL**, shown in FIG. **1**.

[0058] The circuit layer **11** is covered by the insulating layer **12**. The insulating layer **12** is disposed on the circuit layer **11**. The insulating layer **12** has a function of planarizing the projections and recesses caused by the circuit layer **11**. The insulating layer **12** is an organic insulating layer.

[0059] The lower electrodes **LE1**, **LE2**, and **LE3** are disposed on the insulating layer **12** and are separated from each other. The insulating layer **5** is disposed on the insulating layer **12** and the lower electrodes **LE1**, **LE2**, and **LE3**. The insulating layer **5** is an inorganic insulating layer. In this embodiment, the insulating layer **5** corresponds to the second inorganic insulating layer.

[0060] The aperture **AP1** of the insulating layer **5** overlaps the lower electrode **LE1**, the aperture **AP2** overlaps the lower electrode **LE2**, and the aperture **AP3** overlaps the lower electrode **LE3**. The circumferential edge portions of the lower electrodes **LE1**, **LE2**, and **LE3** are covered by the insulating layer **5**.

[0061] The lower electrodes **LE1**, **LE2**, and **LE3** are connected to the respective pixel circuits **1** of the subpixels **SP1**, **SP2**, and **SP3** via respective contact holes formed in the insulating layer **12**. The contact holes in the insulating layer **12** are omitted from the illustration in FIG. **3**, but correspond to the contact holes **CH1**, **CH2**, and **CH3** in FIG. **2**, respectively.

[0062] The partition **6** includes an electrically conductive lower portion **61** disposed on the insulating layer **5** and an upper portion **62** disposed on the lower portion **61**. The lower portion **61** of the partition **6** shown on the right side of the figure is located between the aperture **AP1** and the aperture **AP2**. The lower portion **61** of the partition **6** shown on the left side of the figure is located between the aperture **AP2** and the aperture **AP3**.

[0063] The lower portion **61** may be a single layer or a multi-layered body. The upper portion **62** has a width larger than that of the lower portion **61**. Both end portions of the upper portion **62** protrude beyond the respective side surfaces of the lower portion **61**. Such a shape of the partition **6**

is referred to as an overhang shape.

[0064] In the example illustrated in FIG. 3, the lower portion **61** has a bottom layer **63** disposed on the insulating layer **5** and an axial layer **64** disposed on the bottom layer **63**. For example, the bottom layer **63** is formed thinner than the axial layer **64**. Further, in the example illustrated in FIG. 3, both end portions of the bottom layer **63** protrude from the respective side surfaces of the axial layer **64**.

[0065] The organic layer **OR1** is brought into contact with the lower electrode **LE1** via the aperture **AP1** so as to cover the lower electrode **LE1**, which is exposed through the aperture **AP1**, and the circumferential edge portion is located on the insulating layer **5**. The upper electrode **UE1** covers the organic layer **OR1** and is brought into contact with the lower portion **61**.

[0066] The organic layer **OR2** is brought into contact with the lower electrode **LE2** via the aperture **AP2** so as to cover the lower electrode **LE2** which is exposed through the aperture **AP2**, and the circumferential edge portion is located on the insulating layer **5**. The upper electrode **UE2** covers the organic layer **OR2**, and is in contact with the lower electrode **LE2**.

[0067] The organic layer **OR3** is brought into contact with the lower electrode **LE3** via the aperture **AP3** so as to cover the lower electrode **LE3** which is exposed through the aperture **AP3**, and the circumferential edge portion is located on the insulating layer **5**. The upper electrode **UE3** covers the organic layer **OR3**, and is in contact with the lower **61**.

[0068] In the example illustrated in FIG. 3, the subpixel **SP1** includes a cap layer **CP1** and a sealing layer **SE1**, the subpixel **SP2** includes a cap layer **CP2** and a sealing layer **SE2**, and the subpixel **SP3** includes a cap layer **CP3** and a sealing layer **SE3**. The cap layers **CP1**, **CP2**, and **CP3** each serve as an optical adjustment layer that improve the light extraction efficiency of the light emitted from the respective one of the organic layers **OR1**, **OR2**, and **OR3**.

[0069] The cap layer **CP1** is disposed on the upper electrode **UE1**. The cap layer **CP2** is disposed on the upper electrode **UE2**. The cap layer **CP3** is disposed on the upper electrode **UE3**.

[0070] The sealing layer **SE1** is disposed on the cap layer **CP1**, is brought into contact with the partition **6**, and continuously covers the elements of the subpixel **SP1**. The sealing layer **SE2** is disposed on the cap layer **CP2**, is brought into contact with the partition **6**, and continuously covers the elements of the subpixel **SP2**. The sealing layer **SE3** is disposed on the cap layer **CP3**, is brought into contact with the partition **6**, and continuously covers the elements of the subpixel **SP3**.

[0071] In the example illustrated in FIG. 3, respective parts of the organic layer **OR1**, the upper electrode **UE1**, and the cap layer **CP1** are located on the partition **6** which surrounds the subpixel **SP1**. These parts are separated from the portions of the organic layer **OR1**, the upper electrode **UE1**, and the cap layer **CP1**, which are located in the aperture **AP1** (that is, the portions that constitute the display element **201**).

[0072] Similarly, parts of the organic layer **OR2**, the upper electrode **UE2** and the cap layer **CP2** are located on the partition **6** surrounding the subpixel **SP2**, and these parts are separated from the portions of the organic layer **OR2**, the upper electrode **UE2** and the cap layer **CP2** which are located in the aperture **AP2** (that is, the portions that constitute the display element **202**).

[0073] Similarly, parts of the organic layer **OR3**, the upper electrode **UE3** and the cap layer **CP3** are located on the partition **6** surrounding the subpixel **SP3**, and these parts are separated from the portions of the organic layer **OR3**, the upper electrode **UE3** and the cap layer **CP3** which are located in the aperture **AP3** (portions that constitute the display element **203**).

[0074] The end portions of the sealing layers **SE1**, **SE2**, and **SE3** are located on the partition **6**. In the example illustrated in FIG. 3, the end portions of the sealing layers **SE1** and **SE2**, which are located on the partition **6** between the subpixels **SP1** and **SP2**, are separated from each other, and the end portions of the sealing layers **SE2** and **SE3**, which are located on the partition **6** between the subpixels **SP2** and **SP3**, are separated from each other.

[0075] The sealing layers **SE1**, **SE2**, and **SE3** are covered by the resin layer **13**. The resin layer **13** is covered by the sealing layer **14**. The sealing layer **14** is covered by the resin layer **15**.

[0076] The insulating layer **5**, the sealing layers **SE1**, **SE2**, and **SE3**, and the sealing layer **14** are each formed, for example, of any one of inorganic insulating materials such as silicon nitride (SiN.sub.x), silicon oxide (SiO.sub.x), silicon oxynitride (SiON), and aluminum oxide (Al.sub.2O.sub.3).

[0077] The bottom layer **63** and the axial layer **64** of the partition **6** are formed of a metal material. As the metal material for the bottom layer **63**, for example, molybdenum, titanium, titanium nitride (TiN), molybdenum-tungsten alloy (MoW) or molybdenum-niobium alloy (MoNb) can be used.

[0078] As the metal material of the axial layer **64**, for example, aluminum, aluminum-neodymium alloy (AlNd), aluminum-yttrium alloy (AlY), or aluminum-silicon alloy (AlSi) can be used. Note that the axial layer **64** may as well be formed of an insulating material.

[0079] For example, the upper portion **62** of the partition **6** has a stacked layer structure constituted by a lower layer formed of a metal material and an upper layer formed of a conductive oxide. As the metal material for forming the lower layer, for example, titanium, titanium nitride, molybdenum, tungsten, molybdenum-tungsten alloy or molybdenum-niobium alloy can be used.

[0080] As the conductive oxide for forming the upper layer, for example, indium tin oxide (ITO) or indium zinc oxide (IZO) can be used. Note here that the upper portion **62** may as well have a single-layer structure of a metal material. Further, the upper portion **62** may include a layer formed of an insulating material.

[0081] The lower electrodes **LE1**, **LE2**, and **LE3** are stacked-layered body that includes a transparent electrode formed of an oxide conductive material such as ITO and a metal electrode formed of a metal material such as silver.

[0082] The organic layer **OR1** includes a light emitting layer **EM1**. The organic layer **OR2** includes a light emitting layer **EM2**. The organic layer **OR3** includes a light emitting layer **EM3**. The light emitting layer **EM1**, light emitting layer **EM2**, and light emitting layer **EM3** are formed from materials different from each other.

[0083] In one example, the light emitting layer **EM1** is formed of a material that emits light in a blue wavelength range, the light emitting layer **EM2** is formed of a material that emits light in a green wavelength range, and the light emitting layer **EM3** is formed of a material that emits light in a red wavelength range. Further, each of the organic layers **OR1**, **OR2**, and **OR3** includes a plurality of functional layers such as a hole injection layer, a hole transport layer, an electron blocking layer, a hole blocking layer, an electron transport layer, an electron injection layer and the like.

[0084] The upper electrodes **UE1**, **UE2**, and **UE3** are formed, for example, of a metal material such as an alloy of magnesium and silver (MgAg). The cap layers **CP1**, **CP2**, and **CP3** are each a stacked-layered body of a plurality of thin films. All of the plurality of thin films are transparent and have refractive indices different from each other.

[0085] The circuit layer **11**, the insulating layer **12**, and the insulating layer **5** shown in FIG. 3 are disposed on the display area **DA** and over to the peripheral area **SA**.

[0086] FIGS. 4 and 5 are each a plan view showing a configuration example of a region including a plurality of pads **PD** of the display device **DSP** shown in FIG. 1. FIG. 6 is a plan view showing the metal layers **M1**, **M2**, **M3**, and **M4** shown in FIG. 5.

[0087] FIGS. 4 and 5 show the vicinity of the panel edge **PNLE** in the peripheral area **SA**. In FIGS. 4 and 5, the display area **DA** is formed in the upper part of the figure. In FIG. 4, the flexible printed circuit board **FPC** shown in FIG. 1 is indicated by dotted lines. In FIG. 5, the insulating layer **5** is omitted from the configuration example illustrated in FIG. 4.

[0088] As shown in FIGS. 4 and 5, the plurality of pads **PD** are aligned along the first direction **X** and extend along the second direction **Y**. As described above, the insulating layer **5** and the insulating layer **12** are formed over to the region (the peripheral area **SA**) including the pads **PD**.

[0089] As shown in FIG. 4, the insulating layer **5** is formed to extend to the panel edge **PNLE**. In contrast, the insulating layer **12** is not formed to extend to the panel edge **PNLE**, as shown in FIG.

5. In other words, the peripheral area SA includes an area A11 where the insulating layer 12 is not formed, in the panel edge PNLE.

[0090] The insulating layer 5 has apertures 51 each overlapping the respective one of the pads PD, as shown in FIG. 4. The insulating layer 12 has apertures 121 each overlapping the respective one of the pads PD, as shown in FIG. 5. In this embodiment, the apertures 51 correspond to the first apertures, and the apertures 121 correspond to the second apertures.

[0091] The apertures 51 of the insulating layer 5 overlap the apertures 121 of the insulating layer 12, respectively. In the example illustrated in FIGS. 4 and 5, each aperture 51 and each respective aperture 121 overlap one pad PD.

[0092] The apertures 51 in the insulating layer 5 and the apertures 121 in the insulating layer 12 each extend along a direction different from the direction in which the pads PD are aligned. The apertures 51 and apertures 121 extend along the second direction Y, for example. Specifically, the apertures 51 and apertures 121 each have a rectangular shape elongated along the second direction Y.

[0093] In the example illustrated in FIG. 4, the area of each aperture 51 of the insulating layer 5 is larger than the area of the respective aperture 121 of the insulating layer 12 in plan view. The edge of each aperture 51 is located on an outer side the respective edge of the respective aperture 121. The insulating layer 12 is exposed from the apertures 51.

[0094] The insulating layer 12 further has slits 123, as shown in FIG. 5. In this embodiment, the slits 123 corresponds to the first slits. The slits 123 are each located between a respective adjacent pair of pads PD. In other words, the slits 123 are each located between a respective adjacent pair of apertures 121 of the insulating layer 12. Further, the slits 123 are each formed a respective adjacent pair of apertures 51 of the insulating layer 5.

[0095] The slits 123 extend along the second direction Y. The plurality of slits 123 are aligned along the first direction X. In the example illustrated in FIG. 5, the slits 123 are each opened toward the panel edge PNLE. The length of the slits 123 along the second direction Y is greater than the length of the apertures 121 of the insulating layer 12 along the second direction Y. The slits 123 are connected to the area A11 of the panel edge PNLE.

[0096] As shown in FIG. 5, the insulating layer 12 further has a slit 125, slits 127 and 129 in the peripheral area SA. In this embodiment, the slit 125 corresponds to a second slit, and the slits 127 and 129 correspond to third slits.

[0097] The slit 125 is located between the display area DA, which includes the lower electrodes LE1, LE2, and LE3, and the pads PD. The slit 125 is formed along the first direction X. The width of the slit 125 along the first direction X is greater than the distance between pads PD located at both ends along the first direction X.

[0098] The slits 127 and 129 are respectively connected to both ends of the slit 125 along the first direction X. The slits 127 and 129 are formed from the slit 125 toward the panel edge PNLE along the second direction Y.

[0099] The slits 127 and 129 are connected to the area A11 of the panel edge PNLE. In plan view, the insulating layer 5 overlaps the slits 123, 125, 127, 129 and the area A11.

[0100] In plan view, the plurality of pads PD are surrounded by the slit 125 and the slits 127 and 129. In another point of view, the plurality of pads PD are separated from the insulating layer 12 formed therearound by the slit 125 and the slits 127 and 129. Note here that the insulating layer 12 formed therearound includes the insulating layer 12 formed on the display area DA side.

[0101] The display device DSP further comprises a plurality of metal layers M1, M2, M3, and M4, as shown in FIG. 6. In this embodiment, the metal layer M1 corresponds to a fourth metal layer, the metal layer M2 corresponds to a third metal layer, the metal layer M3 corresponds to a first metal layer, and the metal layer M4 corresponds to a second metal layer.

[0102] Each of the metal layers M1, M2, M3, and M4 extends along the second direction Y. The metal layers M1, M2, M3, and M4, respectively adjacent to each other, are arranged along the first

direction X at intervals therebetween. The pad PD is constituted by the metal layers M3 and M4. [0103] FIG. 7 is a cross-sectional view of the display device DSP taken along the line VII-VII in FIG. 5. FIG. 8 is a cross-sectional view of the display device DSP taken along the line VIII-VIII in FIG. 5. The circuit layer 11 includes insulating layers 111, 112, and 113. The metal layers M1 and M2 described above, together with the insulating layers 111, 112, and 113, constitute the circuit layer 11.

[0104] The insulating layer 111 is an inorganic insulating layer and is disposed on the substrate 10. The metal layer M1 is disposed on the insulating layer 111. The metal layer M1 is formed in the same layer as that of the scanning lines GL, for example.

[0105] The insulating layer 112 is an inorganic insulating layer and is disposed on the insulating layer 111 and the metal layer M1. The insulating layer 112 has contact holes CH4 and CH5.

[0106] The metal layer M2 is disposed on the insulating layer 112. In another point of view, the metal layer M1 is disposed between the substrate 10 and the metal layer M2. The metal layer M2 is formed in the same layer as that of the signal lines SL, for example.

[0107] When focusing on the slit 125, the metal layer M2 does not overlap the slit 125, as shown in FIG. 8. The metal layer M2 is electrically connected to the metal layer M1 via the contact holes CH4 and CH5.

[0108] More specifically, the metal layer M2 includes a first portion P1 connected to the metal layer M1 via the contact hole CH4 and a second portion P2 connected to the metal layer M1 via the contact hole CH5. The second portion P2 extends toward the display area DA.

[0109] The first portion P1 is aligned with the second portion P2 along the second direction Y with an interval therebetween. In other words, a gap G1 is formed between the first portion P1 and the second portion P2 in the metal layer M2.

[0110] The gap G1 overlaps the slit 125. In the example illustrated in FIG. 8, the length of the slit 125 along the second direction Y is less than the length of the gap G1 along the second direction Y. A part of the metal layer M1 overlaps the slit 125 while the gap G1 interposed therebetween.

[0111] The insulating layer 113 is an inorganic insulating layer, and is disposed on the insulating layer 112 and the metal layer M2. In this embodiment, the insulating layer 113 corresponds to a first inorganic insulating layer. The metal layer M2 is disposed between the substrate 10 and the insulating layer 113. The insulating layer 113 has a contact hole CH6.

[0112] The metal layer M3 is located directly above the metal layer M1 and is disposed on the insulating layer 113. The metal layer M3 is electrically connected to the metal layer M2. More specifically, the metal layer M3 is in contact with the first portion P1 of the metal layer M2 via the contact hole CH6.

[0113] The insulating layer 12 is disposed on the insulating layer 113 and the metal layer M3. The metal layer M3 is exposed through the aperture 121 in the insulating layer 12. The insulating layer 12 covers the entire circumferential edge portion of the metal layer M3, as shown in FIGS. 7 and 8.

[0114] The insulating layer 113 is exposed from the insulating layer 12 in the slit 123, as shown in FIG. 7. The insulating layer 5 is disposed on the insulating layer 12. The insulating layer 5 is in contact with the insulating layer 113 at the slit 123. In other words, the insulating layer 113 is covered by the insulating layer 5 in the slit 123.

[0115] As shown in FIG. 8, the insulating layer 113 is exposed from the insulating layer 12 in the slit 125. The insulating layer 5 is in contact with the insulating layer 113 in the slit 125. In other words, the insulating layer 113 is covered by the insulating layer 5 in the slit 125. Although not shown in FIGS. 7 and 8, the insulating layer 5 is in contact with the insulating layer 113 in the slits 127 and 129 as well.

[0116] The metal layer M4 is located directly above the metal layer M3 and is disposed on the insulating layer 5. The metal layer M4 is in contact with the metal layer M3, which is exposed from the aperture 121 of the insulating layer 12, via the aperture 51 of the insulating layer 5. In other words, the metal layer M4 is electrically connected to the metal layer M3 via the apertures 51 and

121. The metal layer **M4** overlaps a circumferential edge portion **121E** of the aperture **121**.

[0117] The insulating layers **111**, **112**, and **113** are formed of one of silicon oxide, silicon nitride, and silicon oxynitride. The insulating layer **5** is formed of silicon oxynitride, for example.

[0118] The metal layers **M2**, **M3**, and **M4** are each formed from a plurality of layers, for example. In one example, each includes two titanium layers formed from titanium-based materials and an aluminum layer formed from an aluminum-based material located between the two titanium layers. Note that at least one of the metal layers **M2**, **M3**, and **M4** may be formed by placing an aluminum layer between layers formed from molybdenum-based materials.

[0119] FIG. **9** is a plan view showing a configuration example of an area including a plurality of pads **PD** in a display device **DSP10** according to a comparative example. FIG. **10** is a cross-sectional view of the display device **DSP10** taken along the line X-X in FIG. **9**. FIG. **11** is a cross-sectional view of the display device **DSP10** taken along the line XI-XI in FIG. **9**. In FIG. **9**, only the aperture **51** of the insulating layers **5** is shown.

[0120] The display device **DSP10** of the comparative example is different from the display device **DSP** of the present embodiment in that the insulating layer **12** does not have slits **123**, **125**, **127**, and **129**.

[0121] In the display device **DSP10**, as shown in FIG. **10**, the insulating layer **12** is located between each adjacent pair of apertures **121**, and with this configuration, the insulating layer **5** is in contact with the insulating layer **12** between each adjacent pair of apertures **121**.

[0122] In other words, the insulating layer **5** is not brought into contact with the insulating layer **113** between each adjacent pair of apertures **121**. Further, as shown in FIG. **11**, also in the area where the slit **125** is formed in this embodiment, the insulating layer **5** is brought into contact with the insulating layer **12**.

[0123] The adhesion strength between the insulating layer **5**, which is an inorganic insulating layer, and the organic insulating layer **12**, which is an organic insulating layer, is weaker than the adhesion strength between the insulating layer **5** and the insulating layer **113**, which are inorganic insulating layers. With this configuration, in the display device **DSP10**, the insulating layer **5** can be easily peeled off from the insulating layer **12**. Such peeling off lowers the reliability of the display device.

[0124] By contrast, in the display device **DSP** of this embodiment, the insulating layer **5** and the insulating layer **113** are in contact with each other and adhered together firmly. Therefore, compared to the case where the insulating layer **5** is in contact with the insulating layer **12**, the adhesion between the insulating layer **5** and the underlying layer is improved, and peeling off of the insulating layer **5** can be suppressed. As a result, in this embodiment, it is possible to suppress a decrease in reliability.

[0125] In the display device **DSP10** of the comparative example, the pads **PD** are connected to the insulating layer **12** formed therearound, as shown in FIGS. **9** and **11**. With this configuration, moisture can easily penetrate to the pads **PD** from the surrounding area via the insulating layer **12**.

[0126] The term “moisture” used here means, for example, moisture in the air (outside air). In FIG. **9**, a path of moisture intrusion is indicated by an arrow **W**. The moisture penetrated may corrode the metal layers **M3** and **M4** that constitute the pad **PD**. Such corrosion may cause the insulation layer **5** and the metal layers **M3** and **M4** to peel off.

[0127] In this embodiment, the pads **PD** are each separated from the insulating layer **12** formed to surround them, by the slits **125**, **127**, and **129**. With this configuration, moisture cannot easily penetrate to the pads **PD** from the outside over the slits **125**, **127**, and **129**, as indicated by the arrow **W** in FIG. **5**. As a result, corrosion that can cause peeling of the metal layers **M3** and **M4** is less likely to occur. In this way, according to this embodiment, it is possible to suppress a decrease in reliability.

[0128] In this embodiment, the insulating layer **12** covers the entire circumference of the circumferential edge portion of the metal layer **M3**, as shown in FIGS. **7** and **8**. In other words, the

circumferential edge portion of the metal layer M3 is not exposed. With this configuration, it is possible to prevent undesirable erosion of the aluminum layer, which may be caused by the etching solution used in the process of forming the lower electrode on the insulating layer 12.

[0129] In this embodiment, the metal layer M2 does not overlap the slit 125, as shown in FIG. 8. With this configuration, it is possible to prevent undesirable etching of the metal layer M2 (disconnection of the metal layer M2), which may be caused by the etching solution used in the area overlapping the slit 125 during the process of forming the slit 125 in the manufacturing process.

[0130] As explained above, according to the configuration of this embodiment, it is possible to provide a display device DSP that can suppress a decrease in reliability. In addition, various other advantageous effects can be obtained from this embodiment.

[0131] Next, other embodiments will be explained. In the configurations of the following embodiments, similar parts and structure to those of the first embodiment can be applied to parts that are not specifically mentioned.

Second Embodiment

[0132] FIG. 12 is a plan view showing a configuration example of an area including a plurality of pads PD in the display device DSP of this embodiment. FIG. 13 is a cross-sectional view of the display device DSP taken along the line XIII-XIII in FIG. 12. FIG. 14 is a cross-sectional view of the display device DSP taken along the line XIV-XIV in FIG. 12. In FIG. 12, the vicinity around two pads PD is shown enlarged.

[0133] This embodiment is different from the first embodiment in that the insulating layer 5 covers the circumferential edge portion 121E of each aperture 121 in the insulating layer 12.

[0134] In the example illustrated in FIG. 12, the area of the aperture 121 of the insulating layer 12 is larger than the area of the aperture 51 of the insulating layer 5 in plan view. Note that the edge of the aperture 121 is located on an outer side of the respective edge of the respective aperture 51. The insulating layer 12 is not exposed from the aperture 51.

[0135] As shown in FIGS. 13 and 14, the insulating layer 5 covers the circumferential edge portion 121E of the aperture 121 in the insulating layer 12. In other words, the insulating layer 12 is not exposed from the insulating layer 5. From another point of view, the metal layer M4 is not brought into contact with the insulating layer 12.

[0136] According to the configuration of this embodiment as well, advantageous effects similar to those of the first embodiment can be obtained. In this embodiment, the insulating layer 5 covers the circumferential edge portion 121E of each aperture 121 of the insulating layer 12. With this configuration, it is possible to prevent the undesirable erosion (dissipation) of the insulating layer 12 during the process of forming the apertures 51 of the insulating layer 5 in the manufacturing process. This embodiment can further suppress the decrease in reliability.

Third Embodiment

[0137] FIG. 15 is a plan view showing a configuration example of an area including a plurality of pads PD in the display device DSP of this embodiment. FIG. 16 a plan view showing a configuration example of an area including a plurality of pads PD in the display device DSP of this embodiment. FIG. 17 is a cross-sectional view of the display device DSP taken along the line XVII-XVII in FIG. 16. FIG. 18 is a cross-sectional view of the display device DSP taken along the line XVIII-XVIII in FIG. 16. In FIG. 16, the vicinity of two pads PD is shown enlarged.

[0138] This embodiment is different from each of the above-provided embodiments in that the insulating layer 5 has apertures of a shape different from those of the apertures 51 in the above-provided embodiments.

[0139] The insulating layer 5 has aperture 53, as shown in FIG. 15. In this embodiment, the aperture 53 correspond to third apertures. The aperture 53 overlap a plurality of pads PD. In other words, the aperture 53 overlap a plurality of metal layers M3, as shown in FIG. 16. The aperture 53 are formed along the first direction X. The slits 123 of the insulating layer 12 overlap the aperture

53 of the insulating layer **5**, respectively. The insulating layer **12** is exposed from the aperture **53**, as shown in FIGS. **15** and **18**.

[0140] The aperture **53** have edges **531** and **533**. In this embodiment, the edge **531** corresponds to a first edge, and the edge **533** corresponds to a second edge. The edges **531** and **533** each extend along the first direction X. The edge **531** opposes the edge **533** along the second direction Y. The edges **531** and **533** are located on an outer side of the respective edges of the respective aperture **121** of the insulating layer **12**.

[0141] The edges **531** and **533** each includes a plurality of protrusions **531P** and **533P**, as shown in FIG. **16**. In this embodiment, the protrusion **531P** corresponds to a first protrusion, and the protrusion **533P** corresponds to a second protrusion.

[0142] The protrusion **531P** protrudes in the second direction Y, and the protrusion **533P** protrudes in a direction opposite to the second direction Y. From another point of view, the protrusions **531P** and **533P** protrude in the respective directions toward each other.

[0143] The protrusion **531P** is disposed at a distance from the protrusion **533P** along the second direction Y. The protrusions **531P** and **533P** each have a tapered shape narrowing down toward the distal end. The distal ends of the protrusions **531P** and **533P** overlap the respective slit **123**.

[0144] As shown in FIG. **17**, the insulating layer **5** is not formed between each adjacent pair of pads PD (the metal layers **M3** and **M4**). In other words, the peripheral area SA includes an area **A13** where the insulating layer **5** is not formed between each adjacent pair of pads PD.

[0145] According to the configuration of this embodiment as well, advantageous effects similar to those of the first embodiment can be obtained. In the etching step of the manufacturing process, there may be such a case sometimes that residues from the member that constitutes the pads PD (for example, the metal layer **M4**) may be created between adjacent pads PD. The residues may occur along stepped portions of the insulating layer **5**. Such residues may cause short-circuiting between adjacent pads PD, resulting in a defect.

[0146] In this embodiment, the edges **531** and **533** of each aperture **53** in the insulating layer **5** includes protrusions **531P** and **533P**, respectively. With this configuration, the member that constituting the metal layer **M4** can be removed in the distal ends of the protrusions **531P** and **533P** during the etching step of the manufacturing process, thereby suppressing the generation of residues. In this manner, short-circuiting between adjacent pads PD are not easily allowed to occur.

[0147] Thus, according to this embodiment, it is possible to further suppress the decrease in reliability.

Fourth Embodiment

[0148] FIG. **19** is a plan view showing a configuration example of an area including a plurality of pads PD in the display device DSP of this embodiment. FIG. **20** is a cross-sectional view of the display device DSP taken along the line XX-XX in FIG. **19**. FIG. **21** is a cross-sectional view of the display device DSP taken along the line XXI-XXI in FIG. **19**. In FIG. **19**, the vicinity of two pads PD is shown enlarged.

[0149] This embodiment is different from the third embodiment in that the insulating layer **12** is removed in the area overlapping the aperture **53** when the aperture **53** are formed in the manufacturing process.

[0150] As shown in FIGS. **19** to **21**, the insulating layer **12** is not disposed in the area overlapping the aperture **53**. As shown in FIG. **20**, the insulating layers **5** and **12** are not formed between each adjacent pair of pads PD (the metal layers **M3** and **M4**). In other words, the peripheral area SA has an area **A15** where the insulating layers **5** and **12** are not formed between each adjacent pair of pads PD.

[0151] According to the configuration of this embodiment as well, advantageous effects similar to those of the first embodiment can be obtained. In this embodiment, the circumferential edge portion of the metal layer **M3** is not covered by the insulating layer **12**. In the case where there is no such processing step that the aluminum layer that makes up the metal layer **M3** may be eroded by an

etching solution after the processing step of forming the aperture 53, in the manufacturing process, it can be said that there is no problem with the configuration of this embodiment.

[0152] Based on the display devices described above as embodiments of the invention, a person having ordinary skill in the art may achieve display devices with arbitral design changes; however, as long as they fall within the scope and spirit of the present invention, all of such display devices are encompassed by the scope of the present invention. A skilled person would conceive various changes and modifications of the present invention within the scope of the technical concept of the invention, and naturally, such changes and modifications are encompassed by the scope of the present invention. For example, if a skilled person adds/deletes/alters a structural element or design to/from/in the above-described embodiments, or adds/deletes/alters a step or a condition to/from/in the above-described embodiment, as long as they fall within the scope and spirit of the present invention, such addition, deletion, and alteration are encompassed by the scope of the present invention.

[0153] Furthermore, regarding the present embodiments, any advantage and effect those will be obvious from the description of the specification or arbitrarily conceived by a skilled person are naturally considered achievable by the present invention.

Claims

1. A display device comprising: a substrate; a first inorganic insulating layer disposed above the substrate and over a display area which displays images and a peripheral area which surrounds the display area; an organic insulating layer disposed on the first inorganic insulating layer; a lower electrode disposed on the organic insulating layer in the display area; a second inorganic insulating layer disposed on the organic insulating layer and overlapping a circumferential edge portion of the lower electrode; an organic layer disposed on the lower electrode; an upper electrode disposed on the organic layer; a plurality of first metal layers disposed on the first inorganic insulating layer and aligned in a first direction along an end of the substrate, in the peripheral area; and a plurality of second metal layers disposed on the second inorganic insulating layer and electrically connected to the first metal layers, wherein the second inorganic insulating layer comprises a plurality of first apertures overlapping the second metal layers, respectively, and the organic insulating layer comprises a plurality of second apertures overlapping the plurality of first apertures, respectively, via which the first metal layers and the second metal layers are in contact respectively with each other, and a plurality of first slits each formed between a respective adjacent pair of the plurality of second apertures, via which the second inorganic insulating layer and the first inorganic insulating layer are in contact with each other.
2. The display device of claim 1, wherein each of the plurality of first slits is opened toward an end of the substrate.
3. The display device of claim 2, wherein the plurality of second metal layers each overlap a circumferential edge portion of a respective one of the plurality of second apertures of the organic insulating layer.
4. The display device of claim 1, wherein the second inorganic insulating layer covers the circumferential edge portions of the plurality of second apertures of the organic insulating layer.
5. A display device comprising: a substrate; a first inorganic insulating layer disposed above the substrate and over a display area which displays images and a peripheral area which surrounds the display area; an organic insulating layer disposed on the first inorganic insulating layer; a lower electrode disposed on the organic insulating layer in the display area; a second inorganic insulating layer disposed on the organic insulating layer and overlapping a circumferential edge portion of the lower electrode; an organic layer disposed on the lower electrode; an upper electrode disposed on the organic layer; a plurality of first metal layers disposed on the first inorganic insulating layer and aligned in a first direction along an end of the substrate, in the peripheral area; and a plurality of

second metal layers disposed on the second inorganic insulating layer and electrically connected to the first metal layers, wherein the second inorganic insulating layer comprises a third aperture, and the third aperture overlaps the plurality of first metal layers.

6. The display device of claim 1, wherein the third aperture comprises a first edge and a second edge opposing each other along a second direction that intersects the first direction, the first edge comprises a plurality of first protrusions each located between a respective adjacent pair of the second metal layers and protruding toward the second edge, and the second edge comprises a plurality of second protrusions each located between a respective adjacent pair of the plurality of second metal layers and each protruding toward the first edge.

7. The display device of claim 6, wherein the organic insulating layer comprises a plurality of first slits each overlapping a respective one of the plurality of first protrusions and a respective one of the plurality of second protrusions and formed between a respective adjacent pair of the plurality of first metal layers.

8. The display device of claim 6, wherein the peripheral area includes an area where the second inorganic insulating layer is not formed between adjacent ones of the plurality of first metal layers.

9. The display device of claim 6, wherein the organic insulating layer is not disposed in an area overlapping the third aperture.

10. The display device of claim 1, wherein the organic insulating layer further comprises a second slit formed along the first direction and located between the lower electrode and the plurality of first metal layers in the peripheral area.

11. The display device of claim 10, further comprising: a third metal layer located between the first inorganic insulating layer and the substrate, electrically connected to the plurality of first metal layers, and not overlapping the second slit.

12. The display device of claim 11, further comprising: a fourth metal layer located between the third metal layer and the substrate, electrically connected to the third metal layer, and overlapping the second slit.

13. The display device of claim 11, wherein the organic insulating layer further comprises a third slit connected to the second slit and formed toward an end of the substrate.

14. A display device comprising: a substrate; a first inorganic insulating layer disposed above the substrate and over a display area which displays images and a peripheral area which surrounds the display area; an organic insulating layer disposed on the first inorganic insulating layer; a lower electrode disposed on the organic insulating layer in the display area; a second inorganic insulating layer disposed on the organic insulating layer and overlapping a circumferential edge portion of the lower electrode; an organic layer disposed on the lower electrode; an upper electrode disposed on the organic layer; and a plurality of first metal layers disposed on the first inorganic insulating layer and aligned in a first direction along an end of the substrate, in the peripheral area, wherein the organic insulating layer comprises a slit formed along the first direction and disposed between the lower electrode and the plurality of first metal layers, in the peripheral area.

15. The display device of claim 14, further comprising: a plurality of second metal layers disposed on the second inorganic insulating layer and electrically connected to the plurality of first metal layers, respectively, in the peripheral area.

16. The display device of claim 15, further comprising: a third metal layer disposed between the first inorganic insulating layer and the substrate, electrically connected to the plurality of first metal layers, and not overlapping the slit.

17. The display device of claim 16, further comprising: a fourth metal layer disposed between the third metal layer and the substrate, electrically connected to the third metal layer, and overlapping the slit.

18. The display device of claim 14, wherein the third metal layer includes a first portion connected to the plurality of first metal layers and the fourth metal layer, and a second portion connected to the fourth metal layer.

19. The display device of claim 14, wherein the fourth metal layer overlaps the slit while interposing a gap formed between the first portion and the second portion.

20. The display device of claim 14, wherein the second inorganic insulating layer is in contact with the first inorganic insulating layer in the slit.
