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Insulated gate bipolar transistor device

Abstract

An IGBT device includes a p-type collector region, an n-type semiconductor layer located above the p-type collector region, a plurality of gate trenches, shielded gates, gates, and a p-type body region located in the n-type semiconductor layer and between adjacent gate trenches. The gate trenches are located in the n-type semiconductor layer. A shielded gate is located in a lower part of a gate trench. A gate is located in an upper part of the gate trench. The gate, the shielded gate, and the n-type semiconductor layer are insulated and isolated from each other.

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATION(S)

(1) This is a national stage application filed under 37 U.S.C. 371 based on International Patent Application No. PCT/CN2022/101534, filed Jun. 27, 2022, which claims priority to Chinese Patent Application No. 202111561080.4 filed with the China National Intellectual Property Administration (CNIPA) on Dec. 15, 2021, the disclosure of which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

(2) The present application relates to the technical field of semiconductor power devices, for example, an insulated gate bipolar transistor (IGBT) device.

BACKGROUND

(3) An IGBT device is a device compounded by a metal oxide semiconductor (MOS) transistor and a bipolar transistor. An input pole of the IGBT device is the MOS transistor. An output pole of the IGBT device is a PNP transistor. Combining features of the two transistor devices, the IGBT device is equipped with both features (that is, a low driving power and a high on-off speed) of the MOS transistor, and features (that is, a low saturation voltage drop and a large capacity) of the bipolar transistor. For the IGBT device, due to a relatively low hole injection efficiency at a boundary between a p-type body region and an n-type drift region, a carrier concentration distribution is low, causing the saturation voltage drop to rise. When the IGBT device turns off, a large number of minority carriers are stored in the n-type drift region, resulting in a serious phenomenon of a tailing turning-off current of the IGBT device and leading to a large turning-off loss.

SUMMARY

(4) The present application provides an IGBT device to reduce the turning-off loss of the IGBT device.

(5) The present application provides an IGBT device. The IGBT device includes a p-type collector region, an n-type semiconductor layer located above the p-type collector region, a plurality of gate trenches, shielded gates, gates, and a p-type body region located in the n-type semiconductor layer and between adjacent gate trenches.

(6) The gate trenches are located in the n-type semiconductor layer. A shielded gate is located in a lower part of a gate trench. A gate is located in an upper part of the gate trench. The gate, the shielded gate, and the n-type semiconductor layer are insulated and isolated from each other.

(7) Each of partial shielded gates located in the gate trenches is externally connected to a gate voltage. The partial shielded gates are each defined as a first shielded gate. Each of shielded gates other than the partial shielded gates and located in the gate trenches is externally connected to an emitter electrode voltage. The shielded gates other than the partial shielded gates are each defined as a second shielded gate. The first shielded gate and the second shielded gate are disposed alternately.

(8) The p-type body region includes a first p-type body region and a second p-type body region. The first p-type body region is located on a side of the p-type body region close to a first shielded gate adjacent to the p-type body region. The second p-type body region is located on a side of the

p-type body region close to a second shielded gate adjacent to the p-type body region. An n-type emitter electrode region is disposed in each of the first p-type body region and the second p-type body region. The doping concentration of the first p-type body region is smaller than the doping concentration of the second p-type body region.

Description

BRIEF DESCRIPTION OF DRAWINGS

(1) FIG. **1** is a section view of an IGBT device according to embodiments of the present application.

(2) FIG. **2** is a section view of another IGBT device according to embodiments of the present application.

DETAILED DESCRIPTION

(3) The solution of the present application is described hereinafter through specific implementations in conjunction with drawings in embodiments of the present application. The described embodiments are part of embodiments of the present application. To illustrate embodiments of the present application, in the schematic views illustrated in BRIEF DESCRIPTION OF DRAWINGS, thicknesses of layers and regions described in the present application are enlarged, and dimensions illustrated in the views do not represent the actual dimensions.

(4) FIG. **1** is a section view of an IGBT device according to embodiments of the present application. As shown in FIG. **1**, the IGBT device in the present application includes a p-type collector region **20** and an n-type semiconductor layer **21** located above the p-type collector region **20**.

(5) The IGBT device also includes a plurality of gate trenches, gates **25**, and shielded gates **27**. The gate trenches are located in the n-type semiconductor layer **21**. A gate **25** is located in an upper part of a gate trench. A shielded gate **27** is located in a lower part of the gate trench. The shielded gate **27** may be merely located in the lower part of the gate trench so that the gate **25** and the shielded gate **27** are an upper and lower structure. Optionally, the shielded gate **27** may also be located in the lower part of the gate trench and extend upward into the upper part of the gate trench. FIG. **1** illustrates an example in which the shielded gate **27** is located in the lower part of the gate trench and extends upward into the upper part of the gate trench. Moreover, the width of the upper part of the gate trench may be greater than, equal to, or smaller than the width of the lower part of the gate trench. FIG. **1** illustrates that the width of the upper part of the gate trench is greater than the width of the lower part of the gate trench.

(6) The gate **25**, the shielded gate **27**, and the n-type semiconductor layer **21** are insulated and isolated from each other. In FIG. **1**, the gate **25** is insulated and isolated from the n-type semiconductor layer **21** through a gate dielectric layer **24**, and the shielded gate **27** is isolated from the gate **25** and the n-type semiconductor layer **21** through a field oxide layer **26**. In general, the thickness of the field oxide layer **26** is greater than the thickness of the gate dielectric layer **24**.

(7) For the IGBT device in the present application, each of partial shielded gates **27** located in the gate trenches is externally connected to a gate voltage G. The partial shielded gates **27** are each defined as a first shielded gate **27***a*. Each of shielded gates **27** other than the partial shielded gates **27** and located in the gate trenches is externally connected to an emitter electrode voltage (not shown). The shielded gates **27** other than the partial shielded gates **27** are each defined as a second shielded gate **27***b*. The first shielded gate **27***a* and the second shielded gate **27***b* are disposed alternately.

(8) The IGBT device in the present application further includes a p-type body region **22** located in the n-type semiconductor layer **21** and between adjacent gate trenches. The p-type body region **22**

includes a first p-type body region **22***a* and a second p-type body region **22***b*. The first p-type body region **22***a* is located on a side close to an adjacent first shielded gate **27***a*. The second p-type body region **22***b* is located on a side close to an adjacent second shielded gate **27***b*. An n-type emitter electrode region **23** is disposed in each of the first p-type body region **22***a* and the second p-type body region **22***b*. The doping concentration of the first p-type body region **22***a* is smaller than the doping concentration of the second p-type body region **22***b*.

(9) Exemplarily, FIG. **1** merely illustrates **4***p*-type body regions **22**. Moreover, only for each of two p-type body regions **22** in the middle, a first p-type body region **22***a* and a second p-type body region **22***b* are illustrated. For each of two p-type body regions **22** on two sides, only a second p-type body region **22***b* is illustrated.

(10) For the IGBT device in the present application, a threshold voltage Vth1 of a current channel in the first p-type body region **22***a* is smaller than a threshold voltage Vth2 of a current channel in the second p-type body region **22***b*. When a shielded gate **27** is externally connected to the gate voltage G, a gate **25** in the gate trench has a greater gate charge Qg1. When a shielded gate **27** is externally connected to the emitter electrode voltage, a gate **25** in the gate trench has a smaller gate charge Qg2. The arrangement in which the first p-type body region **22***a* is adjacent to the first shielded gate **27***a* and the second p-type body region **22***b* is adjacent to the second shielded gate **27***b* enables the small Vth1 to be combined with the great Qg1 and enables the great Vth2 to be combined with the small Qg2. Accordingly, in a process in which the IGBT device turns off from turning on, a current channel in a region where the great Vth2 is combined with the small Qg2 may turn off rapidly, while a current channel in a region where the small Vth1 is combined with the great Qg1 may turn off later. In this case, when the current channel in the region where the great Vth2 is combined with the small Qg2 just turns off, the current channel in the region where the small Vth1 is combined with the great Qg1 is still in the on state. With the reduction of the gate voltage Vg, the current channel in the region where the small Vth1 is combined with the great Qg1 turns off. Therefore, as an external manifestation of the IGBT device, a turning-off loss of the region where the small Vth1 is combined with the great Qg1 reduces a turning-off loss of the region where the great Vth2 is combined with the small Qg2, thereby reducing a turning-off loss of the IGBT device entirely.

(11) FIG. **2** is a section view of another IGBT device according to embodiments of the present application. As shown in FIG. **2**, on the basis of the structure of the IGBT device shown in FIG. **1**, the IGBT device in the present application may further include an n-type charge storage region **32** located in the n-type semiconductor layer **21**. The n-type charge storage region **32** is located below the gates **25**. In an embodiment, the IGBT device in the present application may further include n-type collector regions **30**. The n-type collector regions **30** are located below the n-type semiconductor layer **21**. Moreover, the n-type collector regions **30** and the p-type collector regions **20** are disposed alternately. Optionally, the IGBT device in the present application may further include an n-type field cutoff region **31**. The n-type field cutoff region **31** is located between the p-type collector region **20** and the n-type semiconductor layer **21**. The n-type charge storage region **32**, the n-type field cutoff region **31**, and the n-type collector region **30** are all known technology and are not described in detail in embodiments of the present application.

Claims

1. An insulated gate bipolar transistor (IGBT) device, comprising: a p-type collector region; an n-type semiconductor layer located above the p-type collector region; a plurality of gate trenches, shielded gates, and gates, wherein the plurality of gate trenches are located in the n-type semiconductor layer; each of the shielded gates is located in a lower part of one of the plurality of gate trenches; each of the gates is located in an upper part of one of the plurality of the gate trenches; and each of the gates, each of the shielded gates, and the n-type semiconductor layer are

insulated and isolated from each other, wherein each of partial shielded gates among the shielded gates located in the plurality of gate trenches is externally connected to a gate voltage, the partial shielded gates are each defined as a first shielded gate, each of shielded gates other than the partial shielded gates and among the shielded gates located in the plurality of gate trenches is externally connected to an emitter electrode voltage, the shielded gates other than the partial shielded gates are each defined as a second shielded gate, and the first shielded gate and the second shielded gate are disposed alternately; and a p-type body region located in the n-type semiconductor layer and between adjacent gate trenches among the plurality of gate trenches, wherein the p-type body region comprises a first p-type body region and a second p-type body region, the first p-type body region is located on a side of the p-type body region close to a first shielded gate adjacent to the p-type body region, the second p-type body region is located on a side of the p-type body region close to a second shielded gate adjacent to the p-type body region, an n-type emitter electrode region is disposed in each of the first p-type body region and the second p-type body region, and a doping concentration of the first p-type body region is smaller than a doping concentration of the second p-type body region.

2. The IGBT device according to claim 1, wherein each of the shielded gates extends from the lower part of one of the gate trenches upward into the upper part of one of the gate trenches.

3. The IGBT device according to claim 2, wherein a width of the upper part of each of the gate trench is greater than a width of the lower part of the each of the gate trenches.

4. The IGBT device according to claim 3, further comprising n-type charge storage regions located in the n-type semiconductor layer, wherein each of the n-type charge storage regions is located below a respective one of the gates.

5. The IGBT device according to claim 1, further comprising n-type collector regions, wherein the IGBT device comprises a plurality of p-type collector regions, the n-type collector regions are located below the n-type semiconductor layer, and the n-type collector regions and the plurality of p-type collector regions are disposed alternately.

6. The IGBT device according to claim 1, further comprising an n-type field cutoff region, wherein the n-type field cutoff region is located between the p-type collector region and the n-type semiconductor layer.