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### CURRENT CONTROL DEVICE, MOTOR CONTROL DEVICE AND ELECTRIC POWER STEERING DEVICE

#### Abstract

To improve the estimation accuracy for component temperatures of electronic components included in a current control circuit in terms of an overheat protection of current control circuits that control drive current to drive loads. A component temperature estimating unit (**61e2, 61g**) estimates a first component temperature (Teg), which is a component temperature of a first electronic component (La) based on a current value (I1ad to I1cd) detected or estimated by a current detecting unit, a detected temperature (SdA1) detected by a temperature detection circuit **45**, and estimates a second component temperature (Tee2), which is a component temperature of a second electronic component (QC2) based on the current value (I1ad to I1cd), the detected temperature (SdA1), and the first component temperature (Teg).

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## Background/Summary

### TECHNICAL FIELD

[0001] The present invention relates to a current control device, a motor control device and an electric power steering device.

### BACKGROUND ART

[0002] The following patent literature 1 describes a technology that detects the temperature of a motor drive circuit for driving a motor that generates a steering assist force in an electric power steering apparatus and, when a detected temperature is equal to or above a threshold value, limits drive current of the motor. The following patent literature 2 describes a technology for estimating the temperature of a power supply coil used in the electronic control unit of an electric power steering apparatus from the power supply current and thermistor temperature.

### CITATION LIST

#### Patent Literature

[0003] Patent Literature 1: JP 2006-341795 A [0004] Patent Literature 2: WO 2019/189648 A

### SUMMARY OF INVENTION

#### Technical Problem

[0005] However, when estimating the component temperature of electronic components included in the current control circuit, the estimation accuracy may be lowered by being affected by heat generated by other electronic components that exist around the electronic component to be estimated.

[0006] In view of such a problem described above, it is an object of the present invention to improve the estimation accuracy for component temperatures of electronic components included in a current control circuit in terms of overheat protection of the current control circuit that controls drive current to drive a load.

#### Solution to Problem

[0007] In order to achieve the above-described object, according to an aspect of the present invention, there is provided a current control apparatus including: a current control circuit including a plurality of electronic components; a temperature detection circuit having a temperature detecting element disposed in the vicinity of the current control circuit; a current detecting unit configured to detect or estimate a current value flowing to each of the plurality of electronic components; a component temperature estimating unit configured to estimate a component temperature, which is the temperature of the electronic component, for each of the plurality of electronic components based on the current value detected or estimated by the current detecting unit and the detected temperature detected by the temperature detection circuit; a reduction coefficient setting unit configured to set a plurality of different reduction coefficients for a plurality of different component temperatures included in the component temperature estimated for each of the plurality of electronic components; a selecting unit configured to select any one of the plurality of reduction

coefficients; and a current limiting unit configured to limit output current outputted from the current control circuit to a load based on the selected reduction coefficient, wherein the plurality of electronic components include at least a first electronic component and a second electronic component, the component temperature estimating unit estimates a first component temperature, which is the component temperature of the first electronic component based on the current value detected or estimated by the current detecting unit and the detected temperature detected by the temperature detection circuit, and estimates a second component temperature, which is the component temperature of the second electronic component based on the current value detected or estimated by the current detecting unit, the detected temperature detected by the temperature detection circuit, and the first component temperature.

[0008] According to another aspect of the present invention, there is provided a motor control apparatus characterized in that current supplied to an electric motor as the load is controlled by the current control apparatus described above.

[0009] According to still another aspect of the present invention, there is provided an electric power steering apparatus including: the motor control apparatus described above, and an electric motor configured to be controlled by the motor control apparatus, characterized in that the electric motor provides a steering assist force to a steering system of a vehicle.

#### Advantageous Effects of Invention

[0010] According to the present invention, it is possible to improve the estimation accuracy for component temperatures of electronic components included in a current control circuit in terms of overheat protection of the current control circuit that controls drive current to drive a load.

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## Description

### BRIEF DESCRIPTION OF DRAWINGS

[0011] FIG. 1 is a configuration diagram illustrating an overview of an example of an electric power steering apparatus of the embodiment.

[0012] FIG. 2 is a configuration diagram illustrating an overview of an example of an electronic control unit (ECU) of the embodiment.

[0013] FIG. 3 is a circuit diagram of an example of the temperature detection circuit.

[0014] FIG. 4 is a schematic illustration of a heat dissipation structure that dissipates heat generated by a power conversion circuit.

[0015] FIG. 5 is a block diagram illustrating an example of a functional configuration of the control calculating apparatus.

[0016] FIG. 6 is a block diagram of an example of the functional configuration of the first reduction coefficient setting unit according to the first embodiment.

[0017] FIG. 7 is a block diagram of an example of the functional configuration of the high-side FET temperature estimating unit.

[0018] FIG. 8 is a schematic illustration of an example of a characteristic map of high-side FET reduction coefficients.

[0019] FIGS. 9(a) to (c) are schematic illustration of an example of a setting operation of the component reduction coefficient.

[0020] FIG. 10 is a schematic illustration of an example of a characteristic map of battery reduction coefficients.

[0021] FIG. 11 is an example flowchart of a process in the control calculating apparatus.

[0022] FIG. 12 is a schematic illustration to describe effects of a second low-pass filter.

[0023] FIG. 13 is a block diagram of an example of the functional configuration of a first reduction coefficient setting unit according to a second embodiment.

[0024] FIG. 14 is a graph illustrating temperatures when a specific magnitude of current is applied

in order to investigate trends in component temperatures and temperatures of the temperature sensor in each of the dual-system drive mode and the single-system drive mode.

[0025] FIG. **15** is a graph illustrating temperatures difference when a specific magnitude of current is applied in order to investigate trends in difference between component temperatures and temperatures of the temperature sensor in each of the dual-system drive mode and the single-system drive mode.

[0026] FIG. **16(a)** is a drawing illustrating an example of conversion gain setting, and **(b)** is a drawing illustrating an example of first cutoff frequency setting.

[0027] FIGS. **17(a)** to **(c)** are schematic illustrations illustrating the relationship between a distribution ratio of output current between a first current control circuit and a second current control circuit, a conversion gain and a first cutoff frequency.

[0028] FIG. **18** is a block diagram of a first example of the functional configuration of the high-side FET temperature estimating unit according to a fourth embodiment.

[0029] FIGS. **19(a)** and **(b)** are schematic illustrations of temperature estimation results in the first embodiment and the fourth embodiment, respectively, and **(c)** and **(d)** are schematic illustrations of estimation errors in the first embodiment and the fourth embodiment, respectively.

[0030] FIGS. **20(a)** and **(b)** are schematic illustrations of heat dissipation paths from electronic components to a heat sink, and **(c)** is an equivalent circuit diagram that schematically represents the heat dissipation paths in **(a)** and **(b)**.

[0031] FIG. **21** is a block diagram of a second example of the functional configuration of the high-side FET temperature estimating unit according to the fourth embodiment.

[0032] FIG. **22** is a block diagram of a first example of the functional configuration of a capacitor temperature estimating unit according to a fifth embodiment.

[0033] FIGS. **23(a)** and **(b)** are schematic illustrations of temperature estimation results in the first embodiment and the fifth embodiment, respectively, and **(c)** and **(d)** are schematic illustrations of estimation errors in the first embodiment and the fifth embodiments, respectively.

[0034] FIGS. **24(a)** to **(i)** are image diagrams illustrating the trend of component temperature estimation results when the three-phase FETs are each driven at a specific duty ratio.

[0035] FIG. **25(a)** is a schematic illustration of the heat dissipation paths from electronic components to the heat sink, **(b)** is an equivalent circuit diagram schematically representing the heat dissipation paths in **(a)**, and **(c)** is a block diagram of a second example of the functional configuration of the capacitor temperature estimating unit according to the fifth embodiment.

[0036] FIGS. **26(a)** and **(b)** are block diagrams illustrating a first modification and a second modification of the component temperature estimating unit configured to estimate the component temperatures of electronic components included in the current control circuit.

[0037] FIG. **27** is a configuration diagram illustrating an overview of an example of an electronic control unit according to a sixth embodiment.

[0038] FIG. **28** is a block diagram illustrating an example of the functional configuration of the high-side FET temperature estimating unit according to the sixth embodiment.

[0039] FIGS. **29(a)** to **(d)** are schematic illustrations for explaining an error that occurs in an estimated component temperature based on a first estimated gain  $Ge1$  when a delayed response of the component temperature to be estimated is slower than a delayed response of a second detected temperature.

[0040] FIG. **30(a)** is a schematic illustration of an example of a second estimated gain  $Ge2$ , and **(b)** is a schematic illustration of the estimated component temperature based on the second estimated gain  $Ge2$ .

[0041] FIGS. **31(a)** to **(c)** are schematic illustrations for explaining an error that occurs in the estimated component temperature based on the first estimated gain  $Ge1$  when the delayed response of the component temperature to be estimated is faster than the delayed response of the second detected temperature, **(d)** is a schematic illustration of an example of the second estimated gain

Ge2, and (e) is a schematic illustration of the estimated component temperature based on the second estimated gain Ge2.

[0042] FIG. 32(a) illustrates an example of the change in assumed component temperature of a choke coil La, (b) illustrates an example of the change in assumed component temperature of power cutoff FET QC2, (c) illustrates an example of the change in assumed component temperature of power cutoff FET QD2, (d) illustrates an example of the change in assumed component temperature of power cutoff FET QC1, and (e) illustrates an example of the change in assumed component temperature of power cutoff FET QD1.

[0043] FIGS. 33(a) to (c) are schematic illustrations of a first example to a third example of heat dissipation paths from the choke coil.

[0044] FIGS. 34(a) and (b) are block diagrams of a first example and a second example of the functional configuration of the power cutoff FET temperature estimating unit of a seventh embodiment, respectively.

[0045] FIG. 35 is a configuration diagram illustrating an overview of a first modification of the electronic control unit.

[0046] FIG. 36 is a configuration diagram illustrating an overview of a second modification of the electronic control unit.

[0047] FIG. 37 is a configuration diagram illustrating an overview of the first modification of the electric power steering apparatus.

[0048] FIG. 38 is a configuration diagram illustrating an overview of a second modification of the electric power steering apparatus.

[0049] FIG. 39 is a configuration diagram illustrating an overview of a third modification of the electric power steering apparatus.

#### DESCRIPTION OF EMBODIMENTS

[0050] The embodiments of the present invention will be described in detail with reference to the drawings. Note that the embodiments of the present invention given below are examples of apparatuses and methods to embody the technical concept of the invention, and the technical concept of the present invention does not specify the configuration, arrangement, and the like of the components to those given below. The technical concept of the present invention may be modified in various ways within the technical scope defined by the claims.

[0051] In addition, in the following description, a case in which the present invention is applied to a current control apparatus configured to supply drive current to an electric motor that generates steering assist force for electric power steering will be described, but the present invention is not limited to application to electric power steering apparatuses or motors and can be widely applied to various applications. For example, the present invention may be applied to a current control apparatus configured to apply drive current for an actuator that drives robot's joints, or the present invention may be applied to a current control apparatus configured to supply drive current for an electrical device other than the motor (such as a light emitting diode, or IC such as a pre-driver or microcontroller).

#### First Embodiment

##### Configuration

[0052] FIG. 1 is a configuration diagram illustrating an overview of an example of an EPS (electric power steering) according to an embodiment. A steering shaft (handle shaft) 2 of a steering wheel (steering handle) 1 is connected to steered wheels 8L and 8R via a reduction gear (worm gear) 3, which constitute a reduction mechanism, universal joints 4a and 4b, a pinion rack mechanism 5 and tie rods 6a and 6b and then via hub units 7a and 7b.

[0053] The pinion rack mechanism 5 includes a pinion 5a coupled to a pinion shaft to which a steering force is transferred from the universal joint 4b, and a rack 5b engaged with the pinion 5a, and configured to convert a rotational motion transferred to the pinion 5a into a linear motion in the vehicle's width direction by the rack 5b.

[0054] The steering shaft **2** is provided with a torque sensor **10** configured to detect a steering torque  $T_h$ . In addition, the steering shaft **2** is provided with a steering angle sensor **14** configured to detect a steering angle  $\theta_h$  of the steering wheel **1**.

[0055] A motor **20** configured to assist the steering force of the steering wheel **1** is connected to the steering shaft **2** via the reduction gear **3**. The motor **20** may be, for example, a multiphase motor. In the following description, an example of a three-phase motor having a double winding configuration configured to rotate a common rotor by two system coils including a first system coil and a second system coil wound in a common motor housing will be described. However, the motor **20** may be a motor other than the double winding motor, and the motor **20** does not necessarily have to be of 3-phases. A plurality of the motors **20** configured to assist the steering force of the steering wheel **1** may be connected to the same steering shaft **2**.

[0056] An ECU (electronic control unit) **30** configured to control an electric power steering apparatus receives a supply of power from a battery **13** and an input of an ignition key signal via an ignition switch **11**.

[0057] The ECU **30** controls current to be supplied to the motor **20** (a phase A current  $I_{1a}$ , a phase B current  $I_{1b}$ , and a phase C current  $I_{1c}$  of the first system coil, and a phase A current  $I_{2a}$ , a phase B current  $I_{2b}$ , and a phase C current  $I_{2c}$  of the second system coil) by the voltage control command value obtained by calculating the current command value of the assist control command based on the steering torque  $T_h$  detected by the torque sensor **10**, a vehicle speed  $V_h$  detected by a vehicle speed sensor **12**, and steering angle  $\theta_h$  detected by the steering angle sensor **14** and applying compensation or the like to the current command value. The ECU **30** is an example of a “current control apparatus” and a “motor control apparatus” described in claims.

[0058] The steering angle sensor **14** is not mandatory and may be substituted by calculation of the steering angle  $\theta_h$  by adding a torsion angle of a torsion bar of the torque sensor **10** to a product of a motor rotational angle  $\theta_m$  obtained from a rotational angle sensor **23a** that detects a rotational angle of a rotating shaft of the motor **20** and a gear ratio of the reduction gear **3**. For example, a resolver configured to detect a rotational position of the motor, or a magnetic sensor configured to detect a magnetic field of a magnet attached to the rotating shaft of the motor **20** may be employed as the rotational angle sensor **23a**. Alternatively, a turning angle of steered wheels **8L** and **8R** may be used instead of the steering angle  $\theta_h$ . For example, the turning angle may be detected by detecting the amount of displacement of the rack **5b**.

[0059] The ECU **30** includes, for example, a computer that includes a processor and peripheral components such as storage devices. The processor may be, for example, CPU (Central Processing Unit) or MPU (Micro-Processing Unit).

[0060] The storage device may include any one of a semiconductor storage device, a magnetic storage device, and an optical storage device. The storage device may include memories such as a register, a cache memory, an ROM (Read Only Memory), and an RAM (Random Access Memory).

[0061] Functions of the ECU **30** described below are implemented, for example, by the processor of the ECU **30** executing a computer program stored in the storage device.

[0062] Note that the ECU **30** may be formed by dedicated hardware for executing each data processing described below.

[0063] For example, the ECU **30** may include a functional logic circuit set in a general-purpose semiconductor integrated circuit. For example, the ECU **30** may have a Programmable Logic Device (PLD) such as a Field-Programmable Gate Array (FPGA).

[0064] FIG. **2** is a configuration diagram illustrating an overview of an example of the ECU **30** of the embodiment. The ECU **30** includes a motor rotational angle detection circuit **23**, control calculating apparatuses **31a** and **31b**, a first motor current cutoff circuit **33A** and a second motor current cutoff circuit **33B**, a first gate drive circuit **41A** and a second gate drive circuit **41B**, a first power conversion circuit **42A** and a second power conversion circuit **42B**, a first power cutoff circuit **44A** and a second power cutoff circuit **44B**, and temperature detection circuits **45A** and **45B**.

[0065] A power line PWa configured to transmit power from the battery **13** is connected to the ECU **30** via a connector CNT. A positive-side power line Lpa of the power line PWa branches at a branch point Pb after passing through a noise filter circuit such as EMC (Electromagnetic Compatibility) filter formed of a choke coil La and ceramic capacitors Ca1 and Ca2. One of the branches of the positive-side power line Lpa branched at the branch point Pb is connected to the control calculating apparatus **31a** and the first power cutoff circuit **44A**, and the other branch is connected to the control calculating apparatus **31b** and the second power cutoff circuit **44B**.

[0066] One end of the choke coil La is connected to the positive-side power line Lpa and one end of the ceramic capacitor Ca1 and the other end of the choke coil La is connected to one end of the ceramic capacitor Ca2 and the branch point Pb, and the other ends of the ceramic capacitors Ca1 and Ca2 are grounded. On the other hand, a negative-side line of the power line PWa is connected to a ground line of the ECU **30**.

[0067] A voltage detection circuit **34A** detects supply voltage VRA supplied from the first power cutoff circuit **44A** to the first power conversion circuit **42A**, and outputs the detected supply voltage VRA to the control calculating apparatus **31a**. A voltage detection circuit **34B** detects supply voltage VRB supplied from the second power cutoff circuit **44B** to the second power conversion circuit **42B**, and outputs the detected supply voltage VRB to the control calculating apparatus **31b**.

[0068] The steering torque Th detected by the torque sensor **10**, the vehicle speed Vh detected by the vehicle speed sensor **12**, and a signal of the steering angle  $\theta h$  detected by the steering angle sensor **14** are transferred to the control calculating apparatuses **31a** and **31b** via the connector CNT.

[0069] The control calculating apparatus **31a** calculates the current command value, which is a target value of control of the drive current of the motor **20** based at least on the steering torque Th, and outputs voltage control command values V1a, V1b, and V1c obtained by applying compensation or the like on the current command value to the first gate drive circuit **41A**. The voltage control command values V1a, V1b, and V1c are a phase A voltage control command value, a phase B voltage control command value, and a phase C voltage control command value of the first system coil, respectively.

[0070] The control calculating apparatus **31b** calculates the current command value, which is a target value of control of the drive current of the motor **20** based at least on the steering torque Th, and outputs voltage control command values V2a, V2b, and V2c obtained by applying compensation or the like on the current command value to the second gate drive circuit **41B**. The voltage control command values V2a, V2b, and V2c are a phase A voltage control command value, a phase B voltage control command value, and a phase C voltage control command value of the second system coil, respectively.

[0071] Note that the control calculating apparatus **31a** and the control calculating apparatus **31b** may be integrated into a single control calculating apparatus.

[0072] The first power cutoff circuit **44A** includes a series circuit configuration with two power cutoff field effect transistors (FET) QC1 and QC2 connected source to source, ensuring that parasitic diodes are oriented opposite directions to connect or disconnect the positive-side power line Lpa and the first power conversion circuit **42A**. The drain of the power cutoff FET QC1 is connected to a positive-side power line Lpa, and the drain of the power cutoff FET QC2 is connected to drains of high-side FETs Q1, Q3, and Q5 of the first power conversion circuit **42A**. The control calculating apparatus **31a** outputs control signals SsA and SpA configured to control energization and cutting-off of the power cutoff FETs QC1 and QC2, respectively, to the first gate drive circuit **41A**. The first gate drive circuit **41A** outputs gate signals of the power cutoff FETs QC1 and QC2 according to the control signals SsA and SpA, respectively, to control power on and off of the power cutoff FETs QC1 and QC2. Note that the power cutoff FET QC2 functions as a reverse connection protection field-effect transistor that is connected between DC power source and an inverter to prevent current from flowing from an inverter-side to a DC power source-side in order to prevent failures that may occur when the battery **13**, which is the DC power source, is

connected incorrectly to the wrong polarity by mistake.

[0073] Likewise, the second power cutoff circuit **44B** includes a series circuit configuration with two power cutoff FET QD1 and QD2 connected source to source, ensuring that parasitic diodes are oriented opposite directions to connect or disconnect the positive-side power line Lpa and the second power conversion circuit **42B**. The power cutoff FET QD2 also functions as the reverse connection protection field-effect transistor. The drain of the power cutoff FET QD1 is connected to a positive-side power line Lpa, and the drain of the power cutoff FET QD2 is connected to drains of high-side FETs Q1, Q3 and 05 of the second power conversion circuit **42B**. The control calculating apparatus **31b** outputs control signals SsB and SpB configured to control energization and cutting-off of the power cutoff FETs QD1 and QD2, respectively, to the second gate drive circuit **41B**. The second gate drive circuit **41B** outputs gate signals of the power cutoff FETs QD1 and QD2 according to the control signals SsB and SpB, respectively, to control power on and off of the power cutoff FETs QD1 and QD2.

[0074] When voltage control command values V1a, V1b, and V1c are input from the control calculating apparatus **31a**, the first gate drive circuit **41A** forms six gate signals which are pulse-width-modulated (PWM) based on these voltage control command values V1a, V1b, and V1c and a triangle carrier signal. These gate signals are then outputted to the first power conversion circuit **42A**.

[0075] When voltage control command values V2a, V2b, and V2c are input from the control calculating apparatus **31b**, the second gate drive circuit **41B** forms six gate signals which are pulse-width-modulated based on these voltage control command values V2a, V2b, and V2c and a triangle carrier signal. These gate signals are then outputted to the second power conversion circuit **42B**.

[0076] The first power conversion circuit **42A** includes an inverter having three switching arms SWAa, SWAb, and SWAc composed of FETs as switching devices, and electrolytic capacitors CA1 and CA2.

[0077] The switching arms SWAa, SWAb, and SWAc are connected in parallel to each other. The phase A switching arm SWAa includes the high-side FET Q1 and the low-side FET Q2 connected in series, the phase B switching arm SWAb includes a high-side FET Q3 and a low-side FET Q4 connected in series, and the phase C switching arm SWAc includes a high-side FET Q5 and a low-side FET Q6 connected in series.

[0078] Gate signals outputted from the first gate drive circuit **41A** are inputted to the gates of each of the FETs Q1 to Q6, and by means of these gate signals, the phase A current I1a, the phase B current I1b, and the phase C current I1c from connecting points between the FETs of each of the switching arms SWAa, SWAb, and SWAc are supplied to a phase A winding, a phase B winding, and a phase C winding of the first system coil of the motor **20** via the first motor current cutoff circuit **33A**.

[0079] The electrolytic capacitors CA1 and CA2 include a noise cancellation function and a power supply assistance function with respect to the first power conversion circuit **42A**. The electrolytic capacitors CA1 and CA2 may be, for example, hybrid capacitors using electrolyte combining conductive polymer and electrolyte solution.

[0080] The second power conversion circuit **42B** includes an inverter having three switching arms SWBa, SWBb, and SWBc composed of FETs as switching devices, and electrolytic capacitors CB1 and CB2.

[0081] The switching arms SWBa, SWBb, and SWBc are connected in parallel to each other. The phase A switching arm SWBa includes the high-side FET Q1 and the low-side FET Q2 connected in series, the phase B switching arm SWBb includes a high-side FET Q3 and a low-side FET Q4 connected in series, and the phase C switching arm SWBc includes a high-side FET Q5 and a low-side FET Q6 connected in series.

[0082] Gate signals outputted from the second gate drive circuit **41B** are inputted to the gates of each of the FETs Q1 to 06, and by means of these gate signals, the phase A current I2a, the phase B



current **I2b**, and the phase C current **I2c** from connecting points between the FETs of each of the switching arms **SWBa**, **SWBb**, and **SWBc** are supplied to the phase A winding, the phase B winding, and the phase C winding of the second system coil of the motor **20** via the second motor current cutoff circuit **33B**.

[0083] The electrolytic capacitors **CB1** and **CB2** include a noise cancellation function and a power supply assistance function with respect to the second power conversion circuit **42B**. The electrolytic capacitors **CB1** and **CB2** may be, for example, hybrid capacitors.

[0084] Note that the first power conversion circuit **42A** and the second power conversion circuit **42B** may be power conversion circuits supplying three-phase current to two different motors each providing a steering assist force that assists steering of the steering wheel **1**. For example, these two different motors may be connected to the same steering shaft **2** via reduction gears.

[0085] Current detection circuits **39A1**, **39B1**, and **39C1** are provided on the respective source sides of the low-side FETs **Q2**, **Q4**, and **Q6** that form the lower arm of the switching arms **SWAa**, **SWAb**, and **SWAc** of the first power conversion circuit **42A**. The current detection circuits **39A1**, **39B1**, and **39C1** include shunt resistors through which downstream currents of the switching arms **SWAa**, **SWAb**, and **SWAc** flow, respectively, current detection circuits **39A1**, **39B1**, and **39C1** detects a phase A current, a phase B current, and a phase C current of the first system coil based on the voltage drop across the shunt resistor, and outputs detected values **I1ad**, **I1bd**, and **I1cd**.

[0086] Current detection circuits **39A2**, **39B2**, and **39C2** are provided on the respective source sides of the low-side FETs **Q2**, **Q4**, and **Q6** that form the lower arm of the switching arms **SWBa**, **SWBb**, and **SWBc** of the second power conversion circuit **42B**. The current detection circuits **39A2**, **39B2**, and **39C2** include shunt resistors through which downstream currents of the switching arms **SWBa**, **SWBb**, and **SWBc** flow, respectively, current detection circuits **39A2**, **39B2**, and **39C2** detects a phase A current, a phase B current, and a phase C current of the second system coil based on the voltage drop across the shunt resistor, and outputs detected values **I2ad**, **I2bd**, and **I2cd**.

[0087] The first motor current cutoff circuit **33A** includes three phase cutoff FETs **QA1**, **QA2**, and **QA3** for cutting off the phase current of the motor. The source of the phase cutoff FET **QA1** is connected to the connecting points of the FETs **Q1** and **Q2** of the switching arm **SWAa** of the first power conversion circuit **42A**, and the drain is connected to the phase A winding of the first system coil of the motor **20**. The source of the phase cutoff FET **QA2** is connected to the connecting point of the FETs **Q3** and **Q4** of the switching arm **SWAb**, and the drain is connected to the phase B winding of the first system coil. The source of the phase cutoff FET **QA3** is connected to the connecting point of the FETs **Q5** and **Q6** of the switching arm **SWAc**, and the drain is connected to the phase C winding of the first system coil.

[0088] The control calculating apparatus **31a** outputs a control signal **SmA** configured to control energization and cutting-off of the first motor current cutoff circuit **33A** to the first gate drive circuit **41A**. The first gate drive circuit **41A** outputs gate signals of the phase cutoff FETs **QA1** to **QA3** according to the control signals **SmA** to power the phase A current **I1a** the phase B current **I1b**, and the phase C current **I1c** from the first power conversion circuit **42A** to the motor **20** on or off.

[0089] The second motor current cutoff circuit **33B** includes three phase cutoff FETs **QB1**, **QB2**, and **QB3** for cutting off the phase current of the motor. The source of the phase cutoff FET **QB1** is connected to the connecting points of the FETs **Q1** and **Q2** of the switching arm **SWBa** of the second power conversion circuit **42B**, and the drain is connected to the phase A winding of the second system coil of the motor **20**. The source of the phase cutoff FET **QB2** is connected to the connecting point of the FETs **Q3** and **Q4** of the switching arm **SWBb**, and the drain is connected to the phase B winding of the second system coil. The source of the phase cutoff FET **QB3** is connected to the connecting point of the FETs **Q5** and **Q6** of the switching arm **SWBc**, and the drain is connected to the phase C winding of the second system coil.

[0090] The control calculating apparatus **31b** outputs a control signal **SmB** configured to control energization and cutting-off of the second motor current cutoff circuit **33B** to the second gate drive circuit **41B**. The second gate drive circuit **41B** outputs gate signals of the phase cutoff FETs **QB1** to **QB3** according to the control signals **SmB** to energize or cutoff the phase A current **I2a**, the phase B current **I2b**, and the phase C current **I2c** from the second power conversion circuit **42B** to the motor **20**.

[0091] For example, silicon devices may be used or silicon carbide devices may be used as the high-side FETs **Q1**, **Q3**, and **Q5**, the low-side FET **Q2**, **Q4**, and **Q6**, the phase cutoff FETs **QA1** to **QA3** and **QB1** to **QB3**, and the power cutoff FETs **QC1**, **QC2**, **QD1**, and **QD2**.

[0092] The motor rotational angle detection circuit **23** acquires detected values from the rotational angle sensor **23a**, and detects the motor rotational angle  $\theta_m$ , which is the rotational angle of the rotating shaft of the motor **20**. The motor rotational angle detection circuit **23** outputs the motor rotational angle  $\theta_m$  to the control calculating apparatuses **31a** and **31b**.

[0093] The temperature detection circuit **45A** includes two temperature sensors disposed in close proximity to each other in the vicinity of the first power conversion circuit **42A**. The temperature detection circuit **45B** includes two temperature sensors disposed in close proximity to each other in the vicinity of the second power conversion circuit **42B**. These temperature sensors are examples of “temperature detecting element” described in claims. Note that the temperature sensors do not have to be arranged at the positions in the vicinity of the first power conversion circuit **42A** and the second power conversion circuit **42B**. The temperature sensors need only to be disposed at any locations susceptible to heat generation in the ECU **30**.

[0094] The temperature detection circuit **45A** outputs a detection signal **SdA1** of the temperature of the ECU **30** based on the outputted from one of the two temperature sensors and a detection signal **SdA2** of the temperature of the ECU **30** based on the outputted from the other sensor to the control calculating apparatus **31a**. The temperature detection circuit **45B** outputs a detection signal **SdB1** of the temperature of the ECU **30** based on the outputted from one of the two temperature sensors and a detection signal **SdB2** of the temperature of the ECU **30** based on the outputted from the other sensor to the control calculating apparatus **31b**.

[0095] These temperature sensors may be, for example, a thermistor. The temperature detection circuits **45A** and **45B** may include a thermistor processing circuit configured to detect the temperature of the ECU **30** according to the resistance value of the thermistor.

[0096] FIG. **3** illustrates a circuit diagram of an example of the temperature detection circuit **45A**. The temperature detection circuit **45A** includes a voltage-dividing circuit to which thermistors such as the temperature sensor **45A1** and the thermistor **45A2** and fixed resistors **R1** and **R2** are connected in series respectively, and capacitors **Ct1** and **Ct2**. The temperature detection circuit **45B** includes the same configuration.

[0097] The voltage-dividing circuit composed of the thermistor **45A1** and the fixed resistor **R1** divides a predetermined voltage **Vcc** at a ratio of the resistance value of the thermistor **45A1** to the resistance value of the fixed resistor **R1**, and outputs the value obtained by voltage division to the control calculating apparatus **31a** as the detection signal **SdA1**. The voltage-dividing circuit composed of the thermistor **45A2** and the fixed resistor **R2** divides a predetermined voltage **Vcc** at a ratio of the resistance value of the thermistor **45A2** to the resistance value of the fixed resistor **R2**, and outputs the value obtained by voltage division to the control calculating apparatus **31a** as the detection signal **SdA2**.

[0098] FIG. **4** is a schematic illustration illustrating a heat dissipation structure that dissipates heat generated by the first power conversion circuit **42A** and the second power conversion circuit **42B**. Reference numeral **36** denotes a circuit board, and electronic components of the first power conversion circuit **42A** and the second power conversion circuit **42B** are mounted on a front surface **ff** and a back surface **fr** of the circuit board **36**. Reference numeral **37** denotes a heat-dissipating member **37** configured to dissipate heat generated by the first power conversion circuit **42A** and the

second power conversion circuit **42B**. The heat-dissipating member **37** may be a heat sink formed of heat-conductive metal such as aluminum alloy.

[0099] Electronic components included in each of the first power conversion circuit **42A** and the second power conversion circuit **42B** dissipate heat through the heat sink **37**. A surface **f1** of the electronic component mounted on the front surface **ff** of the circuit board **36** on the opposite side from the circuit board **36** and surfaces **f2** of the temperature sensors **45A1** and **45A2** of the temperature detection circuit **45A** on the opposite side from the circuit board **36** are thermally connected to the same heat sink **37**. An electronic component mounted on the back surface **fr** of the circuit board **36** is thermally connected to the same heat sink **37** through a via penetrating through the circuit board **36**.

[0100] For example, the surfaces **f1** and **f2** are brought into contact with the heat sink **37** via thermal interface materials (TIM) **38a** and **38b** such as conductive paste (for example, heat dissipating grease), respectively, and the electronic component mounted on the back surface **fr** is brought into contact with the heat sink **37** through the thermal interface material **38c** and the via.

[0101] The temperature sensor of the temperature detection circuit **45B** is also thermally connected to the heat sink **37** in the same configuration as the temperature sensors **45A1** and **45A2**.

[0102] Refer to FIG. 2. The control calculating apparatus **31a** acquires detected values **I1ad**, **I1bd**, and **I1cd** of the phase A current, the phase B current, and the phase C current of the first system coil and detection signals **SdA1** and **SdA2** of the temperature of the ECU **30** via an A/D converting unit, not illustrated. The control calculating apparatus **31b** acquires detected values **I2ad**, **I2bd**, and **I2cd** of the phase A current, the phase B current, and the phase C current of the second system coil and detection signals **SdB1** and **SdB2** of the temperature of the ECU **30** via an A/D converting unit, not illustrated. In the following description, the detection signals **SdA1** and **SdA2** may be collectively expressed as “**SdA**”, and the detection signals **SdB1** and **SdB2** may be collectively referred to as “**SdB**”.

[0103] The control calculating apparatus **31a** and the control calculating apparatus **31b** are connected via a communication line **35** such as CAN (Controller Area Network), thereby transmitting data with each other.

[0104] For example, the control calculating apparatus **31a** may calculate battery current **Ibat1** flowing from the battery **13** to the first system coil based on the detected values **I1ad**, **I1bd**, and **I1cd** of the phase A current, the phase B current, and the phase C current of the first system coil and transmit the calculated battery current **Ibat1** to the control calculating apparatus **31b**. Likewise, the control calculating apparatus **31b** may calculate battery current **Ibat2** flowing from the battery **13** to the second system coil based on the detected values **I2ad**, **I2bd**, and **I2cd** of the phase A current, the phase B current, and the phase C current of the second system coil and transmit the calculated battery current **Ibat2** to the control calculating apparatus **31a**.

[0105] Based on the detected values **I1ad**, **I1bd**, and **I1cd** of the phase A current, the phase B current, and the phase C current of the first system coil of the motor **20**, the battery currents **Ibat1** and **Ibat2**, the supply voltage **VRA**, and detection signal **SdA** outputted by the temperature detection circuit **45A**, the control calculating apparatus **31a** estimates component temperatures, which are the temperatures of a plurality of electronic components that constitutes the first current control circuit **40A** configured to control current that drives the first system coil.

[0106] As the electronic components that constitutes the first current control circuit **40A**, the control calculating apparatus **31a** may estimate the component temperatures of, for example, the high-side FETs **Q1**, **Q3**, and **Q5**, the low-side FETs **Q2**, **Q4**, and **Q6** of the first power conversion circuit **42A**, the electrolytic capacitors **CA1** and **CA2**, the shunt resistors of the current detection circuits **39A1**, **39B1**, and **39C1**, the phase cutoff FETs **QA1**, **QA2**, and **QA3**, and the power cutoff FETs **QC1** and **QC2**.

[0107] Likewise, based on the detected values **I2ad**, **I2bd**, and **I2cd** of the phase A current, the phase B current, and the phase C current of the second system coil of the motor **20**, the battery

currents **Ibat1** and **Ibat2**, the supply voltage **VRB**, and detection signal **SdB** outputted by the temperature detection circuit **45B**, the control calculating apparatus **31b** estimates component temperatures, which are the temperatures of a plurality of electronic components that constitutes the second current control circuit **40B** configured to control current that drives the second system coil.

[0108] As the electronic components that constitutes the second current control circuit **40B**, the control calculating apparatus **31b** may estimate the component temperatures of, for example, the high-side FETs **Q1**, **Q3**, and **Q5**, the low-side FETs **Q2**, **Q4**, and **Q6** of the second power conversion circuit **42B**, the electrolytic capacitors **CB1** and **CB2**, the shunt resistors of the current detection circuits **39A2**, **39B2**, and **39C2**, the phase cutoff FETs **QB1**, **QB2**, and **QB3**, and the power cutoff FETs **QD1** and **QD2**.

[0109] The control calculating apparatuses **31a** and **31b** may estimate the component temperature of a choke coil **La** of the noise filter circuit as a common electronic component of the first current control circuit **40A** and the second current control circuit **40B**.

[0110] The control calculating apparatus **31a** estimates the temperature of the ECU **30** based on the detection signal **SdA** outputted by the temperature detection circuit **45A**. The control calculating apparatus **31b** estimates the temperature of the ECU **30** based on the detection signal **SdB** outputted by the temperature detection circuit **45B**. In the following description, the temperature of the ECU **30** is referred to as “ECU temperature”.

[0111] The control calculating apparatus **31a** also estimate the temperature of the motor **20** (for example, the temperature of the winding coil of the first system coil) based on the detected values **I1ad**, **I1bd**, and **I1cd** of the phase A current, the phase B current, and the phase C current of the first system coil and the ECU temperature. The control calculating apparatus **31b** estimates the temperature of the motor **20** (for example, the temperature of the winding coil of the second system coil) based on the detected values **I2ad**, **I2bd**, and **I2cd** of the phase A current, the phase B current, and the phase C current of the second system coil and the ECU temperature. In the following description, the temperature of the motor **20** may be referred to as “motor temperature”.

[0112] The control calculating apparatus **31a** limits the current that drives the first system coil based on the estimated component temperature, the ECU temperature, and the motor temperature, and the battery voltage **Vbat1**, which is a voltage between output terminals of the battery **13**. Likewise, the control calculating apparatus **31b** limits the current that drives the second system coil based on the estimated component temperature, the ECU temperature, and the motor temperature, and the battery voltage **Vbat1**.

[0113] The control calculating apparatuses **31a** and **31b** will be described. FIG. 5 is a block diagram of an example of a functional configuration of the control calculating apparatus **31a**. The control calculating apparatus **31b** has the similar configuration.

[0114] The control calculating apparatus **31a** includes a current command value calculating unit **50**, a current limiting unit **51**, subtractors **52** and **53**, a proportional-Integral (PI) control unit **54**, a 2-phase/3-phase converting unit **55**, a three phase/two phase converting unit **56**, an angular speed converting unit **57**, a first reduction coefficient setting unit **60**, a second reduction coefficient setting unit **70**, and a third reduction coefficient setting unit **71**, and the motor **20** is driven by a vector control.

[0115] The current command value calculating unit **50** calculates a q-axis current command value **Iq0** and a d-axis current command value **Id0** to be flowed to the motor **20** based on the steering torque **Th**, the vehicle speed **Vh**, the motor rotational angle  $\theta_m$  of the motor **20**, and the rotational angular speed  $\omega$  of the motor **20**.

[0116] The current limiting unit **51** limits the q-axis current command value **Iq0** and d-axis current command value **Id0** based on the component reduction coefficient **K1** set by the first reduction coefficient setting unit **60**, the ECU reduction coefficient **K2** and motor reduction coefficient **K3** set by the second reduction coefficient setting unit **70** and the battery reduction coefficient **K4** set by

the third reduction coefficient setting unit **71**. The limited q-axis current command value **Iq1** and limited d-axis current command value **Id1** are outputted. The component reduction coefficient **K1**, ECU reduction coefficient **K2**, motor reduction coefficient **K3** and battery reduction coefficient **K4** will be discussed below.

[0117] The detected values **I1ad**, **I1bd** and **I1cd** of the phase A current, the phase B current and the phase C current of the first system coil of motor **20** detected by the current detection circuits **39A1**, **39B1** and **39C1** are converted to d-q2 axis currents **id** and **iq** in the 3-phase/2-phase converting unit **56**.

[0118] The subtractors **52** and **53** calculate the q-axis deviation current  $\Delta q$  and d-axis deviation current  $\Delta d$  by subtracting the fed back currents **iq** and **id** from the q-axis current command value **Iq1** and d-axis current command value **Id1**, respectively.

[0119] The PI control unit **54** calculates the voltage command values **vq** and **vd** such that the q-axis deviation current  $\Delta q$  and d-axis deviation current  $\Delta d$  each becomes zero. The 2-phase/3-phase converting unit **55** converts the voltage commands **vd** and **vq** into a phase A voltage control command value **V1a**, a phase B voltage control command value **V1b** and a phase C voltage control command value **V1c** of the first system of motor **20**, respectively, and outputs the converted values to the first gate drive circuit **41A**.

[0120] The angular speed converting unit **57** calculates the rotational angular speed **w** of the motor **20** based on the temporal variation of the motor rotational angle  $\theta_m$ . These motor rotational angles  $\theta_m$  and rotational angular speed  $\omega$  are input to the current command value calculating unit **50** for vector control.

[0121] FIG. **6** is a block diagram of an example of the functional configuration of the first reduction coefficient setting unit **60** according to the first embodiment. The first reduction coefficient setting unit **60** estimates the component temperature of each of the plurality of electronic components which constitute the first current control circuit **40A**. The first reduction coefficient setting unit **60** sets a plurality of reduction coefficients for limiting the current that drives the first system coil based on the component temperature estimated for each of the plurality of electronic components. For example, a plurality of different reduction coefficients are set for a plurality of different component temperatures included in the component temperature estimated for each of the plurality of electronic components.

[0122] For example, the first reduction coefficient setting unit **60** may sort the plurality of electronic components into a plurality of groups based on the type of the electronic components and the connection relation or the like in the first current control circuit **40A** and set the reduction coefficient for each group. The first reduction coefficient setting unit **60** selects one of the plurality of limiting coefficients as a component reduction coefficient **K1** and outputs the selected one.

[0123] The first reduction coefficient setting unit **60** includes high-side FET temperature estimating units **61a1** to **61a3**, low-side FET temperature estimating units **61b1** to **61b3**, shunt resistance temperature estimating units **61c1** to **61c3**, phase cutoff FET temperature estimating units **61d1** to **61d3**, power cutoff FET temperature estimating units **61e1** and **61e2**, capacitor temperature estimating units **61f1** and **61f2**, coil temperature estimating unit **61g**, selectors **62a**, **62b**, **62c**, **62d**, **62e**, **62f** and **64**, high-side FET reduction coefficient setting unit **63a**, low-side FET reduction coefficient setting unit **63b**, shunt resistance reduction coefficient setting unit **63c**, phase cutoff FET reduction coefficient setting unit **63d**, power cutoff FET reduction coefficient setting unit **63e**, capacitor reduction coefficient setting unit **63f** and coil reduction coefficient setting unit **63g**.

[0124] The high-side FET temperature estimating units **61a1** to **61a3** estimate the component temperatures **Tea1** to **Tea3** of the high-side FETs **Q1**, **Q3** and **Q5** of the first power conversion circuit **42A**, respectively. The low-side FET temperature estimating units **61b1** to **61b3** estimate the component temperatures **Teb1** to **Teb3** of the low-side FETs **Q2**, **Q4** and **Q6** of the first power conversion circuit **42A**, respectively. The shunt resistance temperature estimating units **61c1** to **61c3** estimate the component temperatures **Tec1** to **Tec3** of the shunt resistors of the current

detection circuits **39A1**, **39B1** and **39C1**, respectively.

[0125] The phase cutoff FET temperature estimating units **61d1** to **61d3** estimate the component temperatures **Ted1** to **Ted3** of the phase cutoff FETs **QA1**, **QA2**, and **QA3**, respectively. The power cutoff FET temperature estimating units **61e1** and **61e2** estimate the component temperatures **Tee1** and **Tee2** of the power cutoff FETs **QC1** and **QC2**. The capacitor temperature estimating units **61f1** and **61f2** estimate the component temperatures **Tef1** and **Tef2** of the electrolytic capacitors **CA1** and **CA2** of the first power conversion circuit **42A**, respectively. The coil temperature estimating unit **61g** estimates the component temperature **Teg** of the choke coil **La** in the noise filter circuit.

[0126] In the following description, the component temperature **Teg** of the choke coil **La** may be referred to as “coil temperature **Teg**”.

[0127] FIG. 7 is a block diagram of an example of the functional configuration of the high-side FET temperature estimating unit **61a1**.

[0128] The high-side FET temperature estimating unit **61a1** has a power loss calculating unit **72**, a gain multiplying unit **73**, a first low-pass filter **74**, a second low-pass filter **75** and an adder **76**.

[0129] The power loss calculating unit **72** calculates the power loss **W** in the high-side FET **Q1** of the first power conversion circuit **42A**.

[0130] For example, the power loss calculating unit **72** estimates the ON-resistance **Rf** of the FET based on the previous value of the component temperature **Tea1** of the high-side FET **Q1** calculated in the previous control cycle. Then, the power loss calculating unit **72** calculates a power loss **W** in the high-side FET **Q1** based on the ON-resistance **Rf**, the duty ratio **Da** of the phase A voltage control command value, the phase A current **I1ad**, the supply voltage **VRA**, the switching loss generation time **Tsw** of the FET, the body diode forward voltage **Vdsf**, the body diode current generation time **Td** and the motor drive PWM frequency **fpwm**.

[0131] The power loss calculating unit **72** of the control calculating apparatus **31b** estimates the power loss **W** using the supply voltage **VRB** instead of the supply voltage **VRA**. The same applies in the following description.

[0132] The switching loss generation time **Tsw** is the sum of the FET turn-on and turn-off times, while the body diode current generation time **Td** is the time for regenerative current to flow in the body diode (parasitic diode) after the FET is switched off.

[0133] For example, the power loss calculating unit **72** may calculate the power loss **W** based on the following calculation formula.

$$W = Rf \times Da \times I1ad \cdot \sup{.2} + (1/6) \times VRA \times I1ad \times Tsw \times fpwm \quad (\text{where, } I1ad \geq 0)$$

$$W = Rf \times Da \times I1ad \cdot \sup{.2} - Vdsf \times I1ad \times Td \times fpwm \quad (\text{where } I1ad < 0)$$

[0134] The gain multiplying unit **73** calculates a product of the power loss **W** and a predetermined conversion gain **G1** (**G1**×**W**) and output the result to the first low-pass filter **74**. The first low-pass filter **74** outputs a signal obtained by applying a low-pass filtering to the product (**G1**×**W**) to the adder **76**. The second low-pass filter **75** outputs a signal obtained by applying the low-pass filtering to a detection signal **SdA** of the temperature of the ECU **30** outputted by the temperature detection circuit **45A** to the adder **76** as a base temperature **Tth**. The adder **76** calculates the sum of the output of the first low-pass filter **74** and the base temperature **Tth** as the component temperature **Tea1** of the high-side FET **Q1**.

[0135] Note that the conversion gain **G1** as well as the first cutoff frequency **fc1** of the first low-pass filter **74** and a second cutoff frequency **fc2** of the second low-pass filter **75** may be set as needed by simulation or the like in advance.

[0136] The high-side FET temperature estimating units **61a2** and **61a3**, the low-side FET temperature estimating units **61b1** to **61b3**, the shunt resistance temperature estimating units **61c1** to **61c3**, the phase cutoff FET temperature estimating units **61d1** to **61d3**, the power cutoff FET temperature estimating units **61e1** and **61e2**, the capacitor temperature estimating units **61f1** and

**61/2**, and the coil temperature estimating unit **61g** may be considered to have the similar configuration as the high-side FET temperature estimating unit **61a1**.

[0137] However, these temperature estimating units and the high-side FET temperature estimating unit **61a1** are different from each other in the conversion gain **G1** of the gain multiplying unit **73**, the first cutoff frequency **fc1** of the first low-pass filter **74** and the second cutoff frequency **fc2** of the second low-pass filter **75**, and a way of calculating the power loss **W** in the power loss calculating unit **72**.

[0138] For example, the conversion gain **G1** of the gain multiplying unit **73** and the first cutoff frequency **fc1** of the first low-pass filter **74** and the second cutoff frequency **fc2** of the second low-pass filter **75** may be set to different values among the electronic components disposed at different locations. These conversion gains **G1**, these first cutoff frequencies **fc1**, and these second cutoff frequencies **fc2** may be set as needed by simulation or the like in advance.

[0139] Also, the method of calculating the power loss **W** in the power loss calculating unit **72** may differ for each of the electronic components having different heat generation modes.

[0140] For example, the power loss calculating unit **72** of the high-side FET temperature estimating unit **61a2** estimates the ON-resistance **Rf** of the FETs based on the previous value of the component temperature **Tea2** of the high-side FET **Q3** calculated in the previous control cycle. Then, the power loss calculating unit **72** calculates a power loss **W** in the high-side FET **Q3** based on the ON-resistance **Rf**, the duty ratio **Db** of the phase B voltage control command value, the phase B current **I1bd**, the supply voltage **VRA**, the switching loss generation time **Tsw**, the body diode forward voltage **Vdsf**, the body diode current generation time **Td** and the motor drive PWM frequency **fpwm**.

[0141] For example, the power loss calculating unit **72** of the high-side FET temperature estimating unit **61a2** may calculate the power loss **W** based on the following calculation formulas.

$$[00001] W = Rf \times Db \times I1bd^2 + (1 / 6) \times VRA \times I1bd \times Tsw \times fpwm (\text{where } I1bd \geq 0) \\ W = Rf \times Db \times I1bd^2 - Vdsf \times I1bd \times Td \times fpwm (\text{where } I1bd < 0)$$

[0142] In addition, for example, the power loss calculating unit **72** of the high-side FET temperature estimating unit **61a3** estimates the ON-resistance **Rf** of the FETs based on the previous value of the component temperature **Tea3** of the high-side FET **Q5** calculated in the previous control cycle. Then, the power loss calculating unit **72** calculates a power loss **W** in the high-side FET **Q5** based on the ON-resistance **Rf**, the duty ratio **Dc** of the phase C voltage control command value, the phase C current **I1cd**, the supply voltage **VRA**, the switching loss generation time **Tsw**, the body diode forward voltage **Vdsf**, the body diode current generation time **Td** and the motor drive PWM frequency **fpwm**.

[0143] For example, the power loss calculating unit **72** of the high-side FET temperature estimating units **61a3** may calculate the power loss **W** based on the following calculation formulas.

$$[00002] W = Rf \times Dc \times I1cd^2 + (1 / 6) \times VRA \times I1cd \times Tsw \times fpwm (\text{where } I1cd \geq 0) \\ W = Rf \times Dc \times I1cd^2 - Vdsf \times I1cd \times Td \times fpwm (\text{where } I1cd < 0)$$

[0144] In addition, for example, the power loss calculating unit **72** of the low-side FET temperature estimating unit **61b1** estimates the ON-resistance **Rf** of the FETs based on the previous value of the component temperature **Teb1** of the low-side FET **Q2** calculated in the previous control cycle. Then, the power loss calculating unit **72** calculates a power loss **W** in the low-side FET **Q2** based on the ON-resistance **Rf**, the duty ratio **Da** of the phase A, the phase A current **I1ad**, the supply voltage **VRA**, the switching loss generation time **Tsw**, the body diode forward voltage **Vdsf**, the body diode current generation time **Td** and the motor drive PWM frequency **fpwm**.

[0145] For example, the power loss calculating unit **72** of the low-side FET temperature estimating unit **61b1** may calculate the power loss **W** based on the following calculation formulas.

$$[00003] W = Rf \times (1 - Da) \times I1ad^2 - (1 / 6) \times VRA \times I1ad \times Tsw \times fpwm (\text{where } I1ad > 0) \\ W = Rf \times (1 - Da) \times I1ad^2 + Vdsf \times I1ad \times Td \times fpwm (\text{where } I1ad < 0)$$

[0146] In addition, for example, the power loss calculating unit 72 of the low-side FET temperature estimating unit 61b2 estimates the ON-resistance  $R_f$  of the FETs based on the previous value of the component temperature  $T_{eb2}$  of the low-side FET Q4 calculated in the previous control cycle. Then, the power loss calculating unit 72 calculates a power loss  $W$  in the low-side FET Q4 based on the ON-resistance  $R_f$ , the duty ratio  $D_b$  of the phase B, the phase B current  $I_{1bd}$ , the supply voltage  $V_{RA}$ , the switching loss generation time  $T_{sw}$ , the body diode forward voltage  $V_{dsf}$ , the body diode current generation time  $T_d$  and the motor drive PWM frequency  $f_{pwm}$ .

[0147] For example, the power loss calculating unit 72 of the low-side FET temperature estimating units 61b2 may calculate the power loss  $W$  based on the following calculation formulas.

$$[00004] W = R_f \times (1 - D_b) \times I_{1bd}^2 - (1 / 6) \times V_{RA} \times I_{1bd} \times T_{sw} \times f_{pwm} (\text{where } I_{1bd} < 0)$$

$$W = R_f \times (1 - D_b) \times I_{1bd}^2 + V_{dsf} \times I_{1bd} \times T_d \times f_{pwm} (\text{where } I_{1bd} > 0)$$

[0148] In addition, for example, the power loss calculating unit 72 of the low-side FET temperature estimating unit 61b3 estimates the ON-resistance  $R_f$  of the FETs based on the previous value of the component temperature  $T_{eb3}$  of the low-side FET Q6 calculated in the previous control cycle.

Then, the power loss calculating unit 72 calculates a power loss  $W$  in the low-side FET Q6 based on the ON-resistance  $R_f$ , the duty ratio  $D_c$  of the phase C, the phase C current  $I_{1cd}$ , the supply voltage  $V_{RA}$ , the switching loss generation time  $T_{sw}$ , the body diode forward voltage  $V_{dsf}$ , the body diode current generation time  $T_d$  and the motor drive PWM frequency  $f_{pwm}$ .

[0149] For example, the power loss calculating unit 72 of the low-side FET temperature estimating units 61b3 may calculate the power loss  $W$  based on the following calculation formulas.

$$[00005] W = R_f \times (1 - D_c) \times I_{1cd}^2 - (1 / 6) \times V_{RA} \times I_{1cd} \times T_{sw} \times f_{pwm} (\text{where } I_{1cd} < 0)$$

$$W = R_f \times (1 - D_c) \times I_{1cd}^2 + V_{dsf} \times I_{1cd} \times T_d \times f_{pwm} (\text{where } I_{1cd} > 0)$$

[0150] Also, the power loss calculating unit 72 of the shunt resistance temperature estimating unit 61c1 estimates the resistance value  $R_s$  of the shunt resistor based on the previous value of the component temperature  $T_{ec1}$  of the shunt resistor of the current detection circuit 39A1 calculated in the previous control cycle. Based on the shunt resistor  $R_s$  and the phase A duty ratio  $D_a$ , and the phase A current  $I_{1ad}$ , the power loss calculating unit 72 calculates the power loss  $W$  in the shunt resistor of the current detection circuit 39A1.

[0151] For example, the power loss calculating unit 72 of the shunt resistance temperature estimating unit 61c1 may calculate the power loss  $W$  based on the following calculation formula.

$$[00006] W = R_s \times (1 - D_a) \times I_{1ad}^2$$

[0152] Also, the power loss calculating unit 72 of the shunt resistance temperature estimating unit 61c2 estimates the resistance value  $R_s$  of the shunt resistor based on the previous value of the component temperature  $T_{ec2}$  of the shunt resistor of the current detection circuit 39B1 calculated in the previous control cycle. Based on the shunt resistor  $R_s$  and the phase B duty ratio  $D_b$ , and the phase B current  $I_{1bd}$ , the power loss calculating unit 72 calculates the power loss  $W$  in the shunt resistor of the current detection circuit 39B1.

[0153] For example, the power loss calculating unit 72 of the shunt resistance temperature estimating unit 61c2 may calculate the power loss  $W$  based on the following calculation formula.

$$[00007] W = R_s \times (1 - D_b) \times I_{1bd}^2$$

[0154] Also, the power loss calculating unit 72 of the shunt resistance temperature estimating unit 61c3 estimates the resistance value  $R_s$  of the shunt resistor based on the previous value of the component temperature  $T_{ec3}$  of the shunt resistor of the current detection circuit 39C1 calculated in the previous control cycle. Based on the shunt resistor  $R_s$  and the phase C duty ratio  $D_c$ , and the phase C current  $I_{1cd}$ , the power loss calculating unit 72 calculates the power loss  $W$  in the shunt resistor of the current detection circuit 39C1.

[0155] For example, the power loss calculating unit 72 of the shunt resistance temperature estimating unit 61c3 may calculate the power loss  $W$  based on the following calculation formula.

$$[00008] W = R_s \times (1 - D_c) \times I_{1cd}^2$$



[0156] In addition, for example, the power loss calculating unit **72** of the phase cutoff FET temperature estimating units **61d1** estimates the ON-resistance  $R_f$  of the FETs based on the previous value of the component temperature  $T_{ed1}$  of the phase cutoff FET **QA1** calculated in the previous control cycle. Then, based on the On-resistance  $R_f$  and the phase A current  $I_{1ad}$ , the power loss  $W$  in the phase cutoff FET **QA1** is calculated.

[0157] For example, the power loss calculating unit **72** of the phase cutoff FET temperature estimating unit **61d1** may calculate the power loss  $W$  based on the following calculation formula.

$$[00009] W = R_f \times I_{1ad}^2$$

[0158] In addition, for example, the power loss calculating unit **72** of the phase cutoff FET temperature estimating units **61d2** estimates the ON-resistance  $R_f$  of the FETs based on the previous value of the component temperature  $T_{ed2}$  of the phase cutoff FET **QA2** calculated in the previous control cycle. Then, based on the On-resistance  $R_f$  and the phase B current  $I_{1bd}$ , the power loss  $W$  in the phase cutoff FET **QA2** is calculated.

[0159] For example, the power loss calculating unit **72** of the phase cutoff FET temperature estimating unit **61d2** may calculate the power loss  $W$  based on the following calculation formula.

$$[00010] W = R_f \times I_{1bd}^2$$

[0160] In addition, for example, the power loss calculating unit **72** of the phase cutoff FET temperature estimating units **61d3** estimates the ON-resistance  $R_f$  of the FETs based on the previous value of the component temperature  $T_{ed3}$  of the phase cutoff FET **QA3** calculated in the previous control cycle. Then, based on the On-resistance  $R_f$  and the phase C current  $I_{1cd}$ , the power loss  $W$  in the phase cutoff FET **QA3** is calculated.

[0161] For example, the power loss calculating unit **72** of the phase cutoff FET temperature estimating unit **61d3** may calculate the power loss  $W$  based on the following calculation formula.

$$[00011] W = R_f \times I_{1cd}^2$$

[0162] For example, the power loss calculating unit **72** of the power cutoff FET temperature estimating units **61e1** and **61e2** estimate the ON-resistance  $R_f$  of the power cutoff FETs **QC1** and **QC2** based on the previous values of the component temperatures  $T_{ee1}$  and  $T_{ee2}$  of the power cutoff FETs **QC1** and **QC2** calculated in the previous control cycle. Then, the power loss  $W$  of each of the power cutoff FETs **QC1** and **QC2** is calculated based on the ON-resistance  $R_f$  and the Battery current  $I_{bat1}$ .

[0163] For example, the power loss calculating unit **72** of the power cutoff FET temperature estimating units **61e1** and **61e2** may calculate the power loss  $W$  based on the following calculation formula.

$$[00012] W = R_f \times I_{bat1}^2$$

[0164] For example, the capacitor temperature estimating units **61f1** and **61f2** estimate Equivalent Series Resistances (ESR)  $R_{esr}$  of the electrolytic capacitors **CA1** and **CA2** respectively based on the previous values of the component temperatures  $T_{ef1}$ ,  $T_{ef2}$  of the electrolytic capacitors **CA1** and **CA2** of the first power conversion circuit **42A** calculated in the previous control cycle. The power loss calculating unit **72** of the capacitor temperature estimating units **61f1** and **61f2** then calculate the power loss  $W$  of each of the electrolytic capacitors **CA1** and **CA2** based on the equivalent series resistance  $R_{esr}$  and the d-axis current  $i_d$  and the q-axis current  $i_q$  calculated by the 3-phase/2-phase converting unit **56**.

[0165] For example, the power loss calculating unit **72** of the capacitor temperature estimating units **61f1** and **61f2** may calculate the power loss  $W$  based on the following calculation formulas.

$$[00013] W = R_f \times (I_d^2 + I_q^2)$$

[0166] The coil temperature estimating unit **61g** estimates a series resistance  $R_{dc}$  of the choke coil  $L_a$  of the noise filter circuit based on the previous value of the coil temperature  $T_{eg}$  calculated in the previous control cycle. The power loss calculating unit **72** of the coil temperature estimating unit **61g** then calculates the power loss  $W$  in the choke coil  $L_a$  based on the series resistance  $R_{dc}$  and the battery current  $I_{bat1}$  and  $I_{bat2}$ .

[0167] For example, the power loss calculating unit **72** of the coil temperature estimating unit **61g** may calculate the power loss  $W$  based on the following calculation formulas.

$$[00014] W = R_{dc} \times (I_{bat1} + I_{bat2})^2$$

[0168] Note that if the driving of the second system coil is prohibited, the power loss  $W$  can be calculated by substituting the battery current  $I_{bat2}$  with  $0[A]$ . When the data of the battery current  $I_{bat2}$  cannot be acquired from the control calculating apparatus **31b** due to the reason such as abnormality or the like of the communication line **35**, the value of the battery current  $I_{bat2}$  can be substituted with the value of the battery current  $I_{bat1}$ .

[0169] Refer to FIG. **6**. The selector **62a** selects any one of the component temperatures  $Tea1$  to  $Tea3$  of the high-side FETs **Q1**, **Q3** and **05** estimated by the high-side FET temperature estimating units **61a1** to **61a3** as a high-side FET temperature  $Tea$ . For example, the selector **62a** may select the highest temperature out of the component temperatures  $Tea1$  to  $Tea3$  as the high-side FET temperature  $Tea$ .

[0170] The selector **62b** selects any one of the component temperatures  $Teb1$  to  $Teb3$  of the low-side FET **Q2**, **Q4**, and **Q6** estimated by the low-side FET temperature estimating units **61b1** to **61b3** as a low-side FET temperature  $Teb$ . For example, the selector **62b** may select the highest temperature among the component temperatures  $Teb1$  to  $Teb3$  as the low-side FET temperature  $Teb$ .

[0171] The selector **62c** selects any one of the component temperatures  $Tec1$  to  $Tec3$  of the shunt resistor estimated by the shunt resistance temperature estimating units **61c1** to **61c3** as the shunt resistance temperature  $Tec$ . For example, the selector **62c** may select the highest temperature among the component temperatures  $Tec1$  to  $Tec3$  as the shunt resistance temperature  $Tec$ .

[0172] The selector **62d** selects any one of the component temperatures  $Ted1$  to  $Ted3$  of the phase cutoff FETs **QA1**, **QA2**, and **QA3** estimated by the phase cutoff FET temperature estimating units **61d1** to **61d3** as the phase cutoff FET temperature  $Ted$ . For example, the selector **62d** may select the highest temperature among the component temperatures  $Ted1$  to  $Ted3$  as the phase cutoff FET temperature  $Ted$ .

[0173] The selector **62e** selects any one of the component temperatures  $Tee1$  and  $Tee2$  of the power cutoff FETs **QC1** and **QC2** estimated by the power cutoff FET temperature estimating units **61e1** and **61e2** as the power cutoff FET temperature  $Tee$ . The selector **62e** may select a temperature higher than either one of the component temperatures  $Tee1$  and  $Tee2$  as the power cutoff FET temperature  $Tee$ .

[0174] The selector **62f** selects either one of the component temperatures  $Tef1$  and  $Tef2$  of the electrolytic capacitors **CA1** and **CA2** estimated by the capacitor temperature estimating units **61f1** and **61f2** as the capacitor temperature  $Tef$ . For example, the selector **62f** may select a temperature higher than either one of the component temperatures  $Tef1$  and  $Tef2$  as the capacitor temperature  $Tef$ .

[0175] The high-side FET reduction coefficient setting unit **63a** sets a high-side FET reduction coefficient  $Ka$ , which is a reduction coefficient for limiting the current that drives the first system coil based on the high-side FET temperature  $Tea$ .

[0176] FIG. **8** is a schematic illustration illustrating an example of a characteristic map illustrating the characteristics of the high-side FET reduction coefficient  $Ka$  set by the high-side FET reduction coefficient setting unit **63a**. The high-side FET reduction coefficient setting unit **63a** sets the high-side FET reduction coefficient  $Ka$  to a maximum value  $K_{max}$  when the high-side FET temperature  $Tea$  is lower than the first temperature  $T1$ . The maximum value  $K_{max}$  may be, for example, greater than  $0 [\%]$  and less than or equal to  $100 [\%]$ .

[0177] The high-side FET reduction coefficient setting unit **63a** sets the high-side FET reduction coefficient  $Ka$  to the maximum value  $K_{max}$  in order to impart hysteresis characteristics to the high-side FET reduction coefficient  $Ka$  in a state in which the high-side FET reduction coefficient  $Ka$  is at its maximum value  $K_{max}$ , as long as the high-side FET temperature  $Tea$  is lower than the second

temperature T2, which is higher than the first temperature T1.

[0178] When the high-side FET temperature  $T_{ea}$  exceeds the second temperature T2 in a state in which the high-side FET reduction coefficient  $K_a$  is at its maximum value  $K_{max}$ , the high-side FET reduction coefficient setting unit **63a** reduces the high-side FET reduction coefficient  $K_a$  from the maximum value  $K_{max}$  to a minimum value  $K_{min}$  until the high-side FET temperature  $T_{ea}$  reaches a third temperature T3, which is higher than the second temperature T2. The minimum value  $K_{min}$  may be, for example, less than 100 [%] and greater than or equal to 0 [%]. The high-side FET reduction coefficient setting unit **63a** sets the high-side FET reduction coefficient  $K_a$  to a minimum value  $K_{min}$  when the high-side FET temperature  $T_{ea}$  is higher than the third temperature T3.

[0179] In a state in which the high-side FET reduction coefficient  $K_a$  is at its minimum value  $K_{min}$ , the high-side FET reduction coefficient setting unit **63a** sets the high-side FET reduction coefficient  $K_a$  to the minimum value  $K_{min}$  as long as the high-side FET temperature  $T_{ea}$  is lower than a fourth temperature T4, which is lower than the third temperature T3. When the high-side FET temperature  $T_{ea}$  becomes smaller than the fourth temperature T4 in a state in which the high-side FET reduction coefficient  $K_a$  is at its minimum value  $K_{min}$ , the high-side FET reduction coefficient setting unit **63a** increases the high-side FET reduction coefficient  $K_a$  from the minimum value  $K_{min}$  to a maximum value  $K_{max}$  until the high-side FET temperature  $T_{ea}$  reaches the first temperature T1.

[0180] A margin width  $\Delta T3$ , which is a difference between a rated temperature  $T_n$  as the electronic component of the high-side FET Q1 to the third temperature T3, a reduction width  $\Delta T4$ , which is a difference between the first temperature T1 and the fourth temperature T4, a reduction width  $\Delta T2$ , which is a difference between the second temperature T2 and the third temperature T3, and a hysteresis width  $\Delta T1$ , which is a difference between the first temperature T1 and the second temperature T2 may be set in advance as needed by simulation or the like. The rated temperature  $T_n$  may be set as needed according to the high-side FET Q1 used. Note that the reduction width  $\Delta T2$  and the reduction width  $\Delta T4$  may be set to the same value, and the reduction width  $\Delta T2$  and the reduction width  $\Delta T4$  may be set to different values. For example, the hysteresis width on the high-temperature side may be increased by setting the reduction width  $\Delta T4$  to a width smaller than the reduction width  $\Delta T2$ .

[0181] Refer to FIG. 6. The low-side FET reduction coefficient setting unit **63b** sets a low-side FET reduction coefficient  $K_b$  for limiting the current that drives the first system coil based on the low-side FET temperature  $T_{eb}$ . The shunt resistance reduction coefficient setting unit **63c** sets a shunt reduction coefficient  $K_c$  for limiting the current that drives the first system coil based on the shunt resistance temperature  $T_{ec}$ . The phase cutoff FET reduction coefficient setting unit **63d** sets a phase cutoff FET reduction coefficient  $K_d$  for limiting the current that drives the first system coil based on the phase cutoff FET temperature  $T_{ed}$ .

[0182] The power cutoff FET reduction coefficient setting unit **63e** sets a power cutoff FET reduction coefficient  $K_e$  for limiting the current that drives the first system coil based on the power cutoff FET temperature  $T_{ee}$ . The capacitor reduction coefficient setting unit **63f** sets a capacitor reduction coefficient  $k_f$  for limiting the current that drives the first system coil based on the capacitor temperature  $T_{ef}$ . The coil reduction coefficient setting unit **63g** sets a coil reduction coefficient  $K_g$  for limiting the current that drives the first system coil based on the coil temperature  $T_{eg}$ .

[0183] The low-side FET reduction coefficient setting unit **63b**, the shunt resistance reduction coefficient setting unit **63c**, the phase cutoff FET reduction coefficient setting unit **63d**, the power cutoff FET reduction coefficient setting unit **63e**, the capacitor reduction coefficient setting unit **63f**, and the coil reduction coefficient setting unit **63g** may set the low-side FET reduction coefficient  $K_b$ , the shunt reduction coefficient  $K_c$ , the phase cutoff FET reduction coefficient  $K_d$ , the power cutoff FET reduction coefficient  $K_e$ , the capacitor reduction coefficient  $K_f$ , and the coil

reduction coefficient Kg having the same characteristics as the characteristic map in FIG. 8.

[0184] It is also applicable to set at least one of the rated temperature  $T_n$ , the hysteresis width  $\Delta T1$ , the reduction widths  $\Delta T2$  and  $\Delta T4$ , and the margin width  $\Delta T3$  in the characteristic map in FIG. 8 to a different value among different types of electronic components. In other words, at least one of the first temperature  $T1$  to the fourth temperature  $T4$  may be set to a different value among different types of electronic components.

[0185] For example, at least one of the rated temperature  $T_n$ , the hysteresis width  $\Delta T1$ , the reduction widths  $\Delta T2$  and  $\Delta T4$ , and the margin width  $\Delta T3$  may be set to a different value among the FETs (the high-side FETs Q1, Q3, and Q5, the low-side FETs Q2, Q4, and Q6, the phase cutoff FETs QA1 to QA3, the power cutoff FETs QC1 and QC2), the resistance (shunt resistor), the capacitors (electrolytic capacitors CA1 and CA2), and coil (choke coil Lp). These hysteresis width  $\Delta T1$ , the reduction widths  $\Delta T2$  and  $\Delta T4$ , and the margin width  $\Delta T3$  may be set as needed in advance, for example, by simulation. The rated temperature  $T_n$  may be set as needed according to the electronic component used.

[0186] The selector 64 selects any one of the high-side FET reduction coefficient Ka, the low-side FET reduction coefficient Kb, the shunt reduction coefficient Kc, the phase cutoff FET reduction coefficient Kd, the power cutoff FET reduction coefficient Ke, the capacitor reduction coefficient Kf, and the coil reduction coefficient Kg as the component reduction coefficient K1. For example, the selector 64 may select the smallest coefficient among the above-described reduction coefficients Ka to Kg as the component reduction coefficient K1.

[0187] FIGS. 9(a) to 9(c) are schematic illustration of an example of a setting operation of the component reduction coefficient K1. For the sake of simplify the description, it is here assumed that the low-side FET reduction coefficient Kb, the shunt reduction coefficient Kc, the phase cutoff FET reduction coefficient Kd, the power cutoff FET reduction coefficient Ke, and the capacitor reduction coefficient Kf are fixed to the maximum value Kmax. It is also assumed that the selector 64 selects the smallest coefficient among the reduction coefficients Ka to Kg as the component reduction coefficient K1.

[0188] As illustrated in FIG. 9(a), the high-side FET reduction coefficient Ka is set to the maximum value Kmax from the time  $t0$  to the time  $t3$ , then starts to reduce at the time  $t3$ , then is reduced to values K11, K13, and K15 at the time  $t4$ , the time  $t5$ , and the time  $t6$ , respectively.

[0189] In contrast, as illustrated in FIG. 9(b), the coil reduction coefficient Kg is set to the maximum value Kmax from the time  $t0$  to the time  $t1$ , then starts to reduce at the time  $t1$ , and is reduced to the value K12 at the time  $t2$ , which is earlier than the time  $t3$ . The value K12 is smaller than the value K11 and is greater than the value K13. Subsequently, the coil reduction coefficient Kg is set to the value K12 during the period from the time  $t2$  to the time  $t4$ , and then is reduced to K13 and K14 at the time  $t5$  and  $t6$ , respectively. The value K14 is smaller than the value K13 and is greater than the value K15.

[0190] When the selector 64 selects the smaller one of the high-side FET reduction coefficient Ka and the coil reduction coefficient Kg as the component reduction coefficient K1, the selector 64 sets the component reduction coefficient K1 to the maximum value Kmax from the time  $t0$  to the time  $t1$ , selects the coil reduction coefficient Kg as the component reduction coefficient K1 from the time  $t1$  to the time  $t5$ , and selects the high-side FET reduction coefficient Ka as the component reduction coefficient K1 from the time  $t5$  onward.

[0191] Consequently, the component reduction coefficient K1 is set to the maximum value Kmax from the period from the time  $t0$  to the time  $t1$ , starts to reduce at the time  $t1$ , and reduces to the value K12 at the time  $t2$ . During the period from the time  $t2$  to the time  $t4$ , the component reduction coefficient K1 is set to K12, and then is reduced to K13 and K15 at the time  $t5$  and the time  $t6$ , respectively.

[0192] Refer to FIG. 5. The second reduction coefficient setting unit 70 estimates the ECU temperature based on the detection signal SdA outputted by the temperature detection circuit 45A.

Based on the detected values  $I1ad$ ,  $I1bd$ , and  $I1cd$  of the phase A current, the phase B current and the phase C current, the rising value of the temperature in the motor **20** due to the motor current (for example, the temperature of the winding coil of the first system coil) is estimated, and the sum of the ECU temperature and the raised value is estimated as the motor temperature.

[0193] The second reduction coefficient setting unit **70** sets the ECU reduction coefficient  $K2$  based on the ECU temperature. For example, the second reduction coefficient setting unit **70** may set the ECU reduction coefficient  $K2$  having the characteristics similar to that in the characteristic map in FIG. **8** for variation of ECU temperature.

[0194] The second reduction coefficient setting unit **70** sets the motor reduction coefficient  $K3$  based on the motor temperature. For example, the second reduction coefficient setting unit **70** may set the motor reduction coefficient  $K3$  having the characteristics similar to that in the characteristic map in FIG. **8** for variation of motor temperature.

[0195] The third reduction coefficient setting unit **71** sets the battery reduction coefficient  $K4$  based on the battery voltage  $Vbat1$ , which is a voltage between output terminals of the battery **13**. FIG. **10** is a schematic illustration of an example of the characteristic map of the battery reduction coefficient  $K4$  set by the third reduction coefficient setting unit **71**. The third reduction coefficient setting unit **71** sets the battery reduction coefficient  $K4$  to the minimum value  $K4_{min}$  when the battery voltage  $Vbat1$  is lower than the first voltage  $V1$ . The minimum value  $K4_{min}$  may be, for example, less than 100 [%] and greater than or equal to 0 [%].

[0196] When the battery voltage  $Vbat1$  is in the range from the first voltage  $V1$  to the second voltage  $V2$ , the higher the battery voltage  $Vbat1$  is, the greater battery reduction coefficient  $K4$  the third reduction coefficient setting unit **71** sets, and when the battery voltage  $Vbat1$  reaches the second voltage  $V2$ , sets the battery reduction coefficient  $K4$  to the maximum value  $K4_{max}$ . The maximum value  $K4_{max}$  may be, for example, a value greater than 0 [%] and equal to or smaller than 100 [%].

[0197] When the battery voltage  $Vbat1$  is in the range from the second voltage  $V2$  to the third voltage  $V3$ , the third reduction coefficient setting unit **71** sets the battery reduction coefficient  $K4$  to the maximum value  $K4_{max}$ .

[0198] When the battery voltage  $Vbat1$  is in the range from the third voltage  $V3$  to the fourth voltage  $V4$ , the higher the battery voltage  $Vbat1$  is, the smaller battery reduction coefficient  $K4$  the third reduction coefficient setting unit **71** sets, and when the battery voltage  $Vbat1$  reaches the fourth voltage  $V4$ , sets the battery reduction coefficient  $K4$  to the minimum value  $K4_{min}$ .

[0199] The third reduction coefficient setting unit **71** sets the battery reduction coefficient  $K4$  to the minimum value  $K4_{min}$  when the battery voltage  $Vbat1$  is higher than the fourth voltage  $V4$ .

[0200] Refer to FIG. **5**. The current limiting unit **51** limits the q-axis current command value  $Iq0$  and d-axis current command value  $Id0$  based on the component reduction coefficient  $K1$ , the ECU reduction coefficient  $K2$ , the motor reduction coefficient  $K3$ , and the battery reduction coefficient  $K4$ , and outputs the limited q-axis current command value  $Iq1$  and the limited d-axis current command value  $Id1$ .

[0201] For example, the current limiting unit **51** may select the minimum coefficient out of the component reduction coefficient  $K1$ , the ECU reduction coefficient  $K2$ , and motor reduction coefficient  $K3$ , and the battery reduction coefficient  $K4$  as the reduction coefficient  $K$ , and limit the q-axis current command value  $Iq0$  and the d-axis current command value  $Id0$  based on the reduction coefficient  $K$ . For example, the q-axis current command value  $Iq0$  and the d-axis current command value  $Id0$  may be limited so that the smaller the reduction coefficient  $K$ , the smaller the limited q-axis current command value  $Iq1$  and the limited d-axis current command value  $Id1$  will be.

[0202] For example, the product of each of the q-axis current command value  $Iq0$  and the d-axis current command value  $Id0$  multiplied by the reduction coefficient  $K$  may be calculated as limited q-axis current command value  $Iq1=K \times Iq0$  and limited d-axis current command value  $Id1=K \times Id0$ .

## Operation

[0203] FIG. 11 is an example flowchart of a process in the control calculating apparatus 31a.

[0204] In Step S1, the first reduction coefficient setting unit 60 and the second reduction coefficient setting unit 70 acquires a detection signal SdA of the temperature detection circuit 45A.

[0205] In Step S2, the current detection circuits 39A1, 39B1, and 39C1 detect the phase A current I1ad, the phase B current I1bd, and the phase C current I1cd of the first system coil.

[0206] Step S3, the voltage detection circuit 34A detects the supply voltage VRA of the first power conversion circuit 42A.

[0207] In Step S4, the control calculating apparatus 31a calculates the battery current Ibat1 flowing from the battery 13 to the first system coil based on the phase A current I1ad, the phase B current I1bd, and the phase C current I1cd. The control calculating apparatus 31a also receives the battery current Ibat2 flowing from the battery 13 to the second system coil from the control calculating apparatus 31b.

[0208] In Step S5, the first reduction coefficient setting unit 60 estimates the power loss W in each of the plurality of electronic components which constitute the first current control circuit 40A based on the phase A current I1ad, the phase B current I1bd, the phase C current I1cd, the battery currents Ibat1 and Ibat2, and the supply voltage VRA.

[0209] In Step S6, the first reduction coefficient setting unit 60 estimates the component temperature of each of the plurality of electronic components which constitute the first current control circuit 40A based on the power loss W and the detection signal SdA.

[0210] In Step S7, the second reduction coefficient setting unit 70 estimates the ECU temperature based on the detection signal SdA. The second reduction coefficient setting unit 70 also estimates the motor temperature based on the phase A current I1ad, the phase B current I1bd, and the phase C current I1cd based on the ECU temperature.

[0211] In Step S8, the first reduction coefficient setting unit 60 sets the component reduction coefficient K1 based on the estimated component temperature of each of the plurality of electronic components.

[0212] In Step S9, the second reduction coefficient setting unit 70 sets the ECU reduction coefficient K2 based on the estimated ECU temperature.

[0213] In Step S10, the second reduction coefficient setting unit 70 sets the motor reduction coefficient K3 based on the estimated motor temperature.

[0214] In Step S11, the third reduction coefficient setting unit 71 sets the battery reduction coefficient K4 based on the battery voltage Vbat1, which is a voltage between output terminals of the battery 13.

[0215] In Step S12, the current limiting unit 51 limits the drive current of the first system coil based on the component reduction coefficient K1, the ECU reduction coefficient K2, the motor reduction coefficient K3, and the battery reduction coefficient K4. The process is then ended.

[0216] Note that the configuration and the process of the control calculating apparatus 31b is the same as the configuration and the process of the control calculating apparatus 31a described above. Therefore, in reading the above-described description, “temperature detection circuit 45A” is replaced with “temperature detection circuit 45B”, “detection signal SdA, SdA1, SdA2” is replaced with “detection signal SdB, SdB1, SdB2”, “first system coil” is replaced with “second system coil”, “phase A current I1ad, phase B current I1bd, phase C current I1cd” is replaced with “phase A current I2ad, phase B current I2bd, phase C current I2cd”, “control calculating apparatus 31a” is replaced with “control calculating apparatus 31b”, “battery current Ibat1” is replaced with “battery current Ibat2”, “control calculating apparatus 31b” is replaced with “control calculating apparatus 31a”, “voltage detection circuit 34A” is replaced with “voltage detection circuit 34B”, “first power conversion circuit 42A” is replaced with “second power conversion circuit 42B”, and “supply voltage VRA” is replaced with “supply voltage VRB”.

Effect of the First Embodiment

[0217] (1) The current control apparatus according to the first embodiment includes: a current control circuit including a plurality of electronic components; a temperature detection circuit having a temperature detecting element disposed in the vicinity of the current control circuit; a current detecting unit configured to detect or estimate current values flowing to each of the plurality of electronic components; a component temperature estimating unit configured to estimate a component temperature, which is the temperature of the electronic component, for each of the plurality of electronic components based on the current value detected or estimated by the current detecting unit and the detected temperature detected by the temperature detection circuit; a reduction coefficient setting unit configured to set a plurality of different reduction coefficients for a plurality of different component temperatures included in the component temperature estimated for each of the plurality of electronic components; a selecting unit configured to select any one of the plurality of reduction coefficients; and a current limiting unit configured to limit output current outputted from the current control circuit to a load based on the selected reduction coefficient.

[0218] This can suppress overheating of the plurality of electronic components included in the current control circuit that are susceptible to thermal damage. For example, even when the components with a large heat generation rate change due to the changes in the energizing pattern in the current control circuit, the reduction coefficient can be set according to the components that are more susceptible to thermal damage due to the increase in heat generation rate. The reduction coefficient can be set according to the characteristics of each component (for example, rated voltage) and the component temperature, depending on the component susceptible to thermal damage. By setting the reduction coefficient according to the needs of individual components, excessive limitation of drive current can be suppressed.

[0219] (2) The plurality of electronic components may include electronic components with different heat generation modes. The component temperature estimating unit estimates the component temperature of each of the electronic components with different heat generation modes based on the resistance value of the electronic component, the current value, and the energization time of the current flowing to the electronic component (for example, energization duty ratio), and the detected temperature detected by the temperature detection circuit.

[0220] This allows individual component temperatures to be estimated according to the heat generation modes of each electronic component.

[0221] (3) A plurality of electronic components may include a plurality of different types of electronic components. The reduction coefficient setting unit may set one reduction coefficient for each type of electronic component.

[0222] By setting reduction coefficients for a plurality of electronic components of the same type together, the calculation load required for the process of setting reduction coefficients when estimating component temperatures for each of the plurality of electronic components can be reduced.

[0223] (4) At least one of the plurality of different types of electronic components may include a plurality of electronic components disposed at different locations in the current control circuit. The current control apparatus may include a second selecting unit configured to select any one of the component temperatures estimated for each of the plurality of electronic components disposed at different locations. The reduction coefficient setting unit may set the reduction coefficient for at least one type of electronic component based on the component temperature selected by the second selecting unit.

[0224] By grouping electronic components based on component types and locations and setting a reduction coefficient for each group, the calculation load required for the process of setting reduction coefficients when estimating component temperatures for each of the plurality of electronic components can be reduced.

[0225] (5) The component temperature estimating unit may estimate the power loss generated in electronic component for each of the plurality of electronic components. The component

temperature estimating unit may estimate the component temperature for each of the plurality of electronic components based on the sum of the value obtained by first low-pass filtering the product of the power loss and the predetermined gain and the value obtained by second low-pass filtering the detected temperature detected by the temperature detection circuit.

[0226] By estimating the component temperature based on the value obtained by the first low-pass filtering of the power loss, the component temperature can be estimated with high accuracy. By the second low-pass filtering the detected temperature detected by the temperature detection circuit, an estimated value of the ambient temperature in the proximity of individual electronic components can be obtained. If the electronic component is thermally connected to a heat sink, the heat sink temperature in the proximity of the electronic component can be obtained.

[0227] FIG. 12 is a schematic illustration of the effect of the second low-pass filtering. Reference numerals **100**, **101**, and **102** schematically illustrate electronic components provided on the circuit board **36**. The component temperature estimating unit estimates the individual temperatures of the electronic components **100** to **102** by adding the temperature change due to power loss of each of the electronic components **100** to **102** to the ambient temperature. Therefore, if the detected value of the temperature detection circuit is used as it is as the ambient temperature when estimating the component temperature of the electronic components **100** and **101**, it is affected by the heat generated by the other electronic components **102** disposed near the temperature sensors **45A1** and **45A2** of the temperature detection circuit and thus the component temperature around the electronic components **100** and **101** cannot be properly estimated. Therefore, by the second low-pass filtering the detected temperature detected by the temperature detection circuit, the ambient temperature in the vicinity of individual electronic components can be estimated with high accuracy by suppressing the effect of heat generated by the **102** electronic components in the proximity of the temperature sensors **45A1** and **45A2**.

[0228] (6) The plurality of electronic components may include electronic components disposed at different locations in the current control circuit. At least one of the above-described predetermined gains, the cutoff frequency of the first low-pass filtering, and the cutoff frequency of the second low-pass filtering may be set to a different value among electronic components disposed at different locations.

[0229] This allows the component temperatures to be estimated individually based on locations where electronic components are disposed. For example, as illustrated in FIG. 12, the distance between temperature sensors **45A1** and **45A2** and individual electronic components **100** to **102** differs depending on the electronic components **100** to **102**. Therefore, by setting the cutoff frequency of the second low-pass filtering to different values among the electronic components the effect of the difference in distance between the temperature sensor and electronic components can be suppressed.

[0230] (7) The current limiting unit may limit the output current so that the smaller the reduction coefficient, the smaller the output current outputted from the current control circuit to the load. The reduction coefficient setting unit may set the reduction coefficient to the maximum value when the component temperature is lower than a first temperature, and reduce the reduction coefficient from the maximum value to a minimum value until the component temperature reaches a third temperature, which is higher than the second temperature when the component temperature exceeds a second temperature which is higher than the first temperature in a state in which the reduction coefficient is at its maximum value, set the reduction coefficient to the minimum value when the component temperature is higher than the third temperature, and increase the reduction coefficient from the minimum value to the maximum value until the component temperature reaches the first temperature when the component temperature reaches a fourth temperature which is lower than the third temperature in a state in which the reduction coefficient is at its minimum value. The plurality of electronic components may include electronic components with different heat generation modes, and at least one of the first temperature, the second temperature, the third



temperature, and the fourth temperature may be set to a different value among electronic components with different heat generation modes.

[0231] This allows the reduction coefficient to be set individually according to the heat generation modes of electronic components.

[0232] (8) The current control apparatus may include a heat sink to dissipate heat generated from the current control circuit. The temperature detecting element may be thermally coupled to the heat sink.

[0233] This makes it easier to detect the overall temperature of the electronic components of the current control circuit with the temperature detecting element.

#### Second Embodiment

[0234] In the first embodiment, one of the component temperatures estimated for each of a plurality of electronic components of the same type disposed at different locations respectively is selected, and the reduction coefficients for these electronic components are set based on the selected component temperature. For example, one of the component temperatures  $Tea1$  to  $Tea3$  of the high-side FETs  $Q1$ ,  $Q3$ , and  $Q5$  estimated by the high-side FET temperature estimating units  $61a1$  to  $61a3$  is selected as the high-side FET temperature  $Tea$ , and the high-side FET reduction coefficient  $Ka$  is set based on the high-side FET temperature  $Tea$ .

[0235] In the second embodiment, a plurality of different reduction coefficients are set for a plurality of electronic components of the same type, each disposed at different locations. For example, a plurality of high-side FET reduction coefficients  $Ka1$  to  $Ka3$  may be set based on each of the component temperatures  $Tea1$  to  $Tea3$  of high-side FETs  $Q1$ ,  $Q3$  and  $Q5$ . Similarly, for the low-side FETs  $Q2$ ,  $Q4$ , and  $Q6$ , the shunt resistors, the phase cutoff FETs  $QA1$  to  $QA3$ , the power cutoff FETs  $QC1$  and  $QC2$ , and the electrolytic capacitors  $CA1$  and  $CA2$ , a plurality of low-side FET reduction coefficients  $Kb1$  to  $Kb3$ , shunt reduction coefficients  $Kc1$  to  $Kc3$ , phase cutoff FET reduction coefficients  $Kd1$  to  $Kd3$ , power cutoff FET reduction coefficients  $Ke1$  and  $Ke2$ , and capacitor reduction coefficients  $Kf1$  and  $Kf2$ , respectively, may be set.

[0236] Then, any one of the high-side FET reduction coefficients  $Ka1$  to  $Ka3$ , the low-side FET reduction coefficients  $Kb1$  to  $Kb3$ , the shunt reduction coefficients  $Kc1$  to  $Kc3$ , the phase cutoff FET reduction coefficients  $Kd1$  to  $Kd3$ , the power cutoff FET reduction coefficients  $Ke1$  and  $Ke2$ , the capacitor reduction coefficients  $Kf1$  and  $Kf2$ , and the coil reduction coefficient  $Kg$  is selected as the component reduction coefficient  $K1$ .

[0237] In this manner, by selecting one of the reduction coefficients set for each of the plurality of electronic components of the same type disposed at different locations as the component reduction coefficient  $K1$ , it is possible to limit the output current more finely based on the electronic components.

[0238] FIG. 13 is a block diagram of an example of the functional configuration of the first reduction coefficient setting unit  $60$  according to the second embodiment. The first reduction coefficient setting unit  $60$  of the second embodiment has a similar configuration to the first reduction coefficient setting unit  $60$  of the first embodiment described with reference to FIG. 6, and the same or similar components are indicated by the same reference numerals and duplicate descriptions are omitted. The first reduction coefficient setting unit  $60$  of the second embodiment has high-side FET reduction coefficient setting units  $63a1$  to  $63a3$ , low-side FET reduction coefficient setting units  $63b1$  to  $63b3$ , shunt resistance reduction coefficient setting units  $63c1$  to  $63c3$ , phase cutoff FET reduction coefficient setting units  $63d1$  to  $63d3$ , power cutoff FET reduction coefficient setting units  $63e1$  and  $63e2$ , and capacitor reduction coefficient setting units  $63f1$  and  $63f2$ , and coil reduction coefficient setting unit  $63g$ .

[0239] The high-side FET reduction coefficient setting units  $63a1$  to  $63a3$  set a plurality of high-side FET reduction coefficients  $Ka1$  to  $Ka3$  based on each of the component temperatures  $Tea1$  to  $Tea3$  of high-side FETs  $Q1$ ,  $Q3$  and  $Q5$ . The low-side FET reduction coefficient setting units  $63b1$  to  $63b3$  set a plurality of low-side FET reduction coefficients  $Kb1$  to  $Kb3$  based on each of the

component temperatures  $T_{eb1}$  to  $T_{eb3}$  of low-side FETs Q2, Q4 and Q6. The shunt resistance reduction coefficient setting units **63c1** to **63c3** set a plurality of shunt reduction coefficients  $K_{c1}$  to  $K_{c3}$  based on each of the component temperatures  $T_{ec1}$  to  $T_{ec3}$  of the shunt resistors of the current detection circuits **39A1**, **39B1** and **39C1**. The phase cutoff FET reduction coefficient setting units **63d1** to **63d3** set a plurality of phase cutoff FET reduction coefficients  $K_{d1}$  to  $K_{d3}$  based on each of the component temperatures  $T_{ed1}$  to  $T_{ed3}$  of the phase cutoff FETs QA1, QA2, and QA3. The power cutoff FET reduction coefficient setting units **63e1** and **63e2** set a plurality of power cutoff FET reduction coefficients  $K_{e1}$  and  $K_{e2}$  based on each of the component temperatures  $T_{ee1}$  and  $T_{ee2}$  of the power cutoff FETs QC1 and QC2. The capacitor reduction coefficient setting units **63f1** and **63f2** set a plurality of capacitor reduction coefficients  $K_{f1}$  and  $K_{f2}$  based on each of the component temperatures  $T_{ef1}$  and  $T_{ef2}$  of the electrolytic capacitors CA1 and CA2 of the first power conversion circuit **42A**. The coil reduction coefficient setting unit **63g** sets the coil reduction coefficient  $K_g$  based on the coil temperature  $T_{eg}$ .

[0240] The high-side FET reduction coefficient setting units **63a1** to **63a3**, the low-side FET reduction coefficient setting units **63b1** to **63b3**, the shunt resistance reduction coefficient setting units **63c1** to **63c3**, the phase cutoff FET reduction coefficient setting units **63d1** to **63d3**, the power cutoff FET reduction coefficient setting units **63e1** and **63e2**, the capacitor reduction coefficient setting units **63f1** and **63f2**, and the coil reduction coefficient setting unit **63g** may set the high-side FET reduction coefficients  $K_{a1}$  to  $K_{a3}$ , the low-side FET reduction coefficients  $K_{b1}$  to  $K_{b3}$ , the shunt reduction coefficients  $K_{c1}$  to  $K_{c3}$ , the phase cutoff FET reduction coefficients  $K_{d1}$  to  $K_{d3}$ , the power cutoff FET reduction coefficients  $K_{e1}$  and  $K_{e2}$ , the capacitor reduction coefficients  $K_{f1}$  and  $K_{f2}$ , and coil reduction coefficient  $K_g$  having the same characteristics as the characteristic map illustrated in FIG. 8.

[0241] It is also applicable to set at least one of the rated temperature  $T_n$ , the hysteresis width  $\Delta T1$ , the reduction widths  $\Delta T2$  and  $\Delta T4$ , and the margin width  $\Delta T3$  in the characteristic map in FIG. 8 to a different value among different types of electronic components.

[0242] In particular, at least one of the rated temperature  $T_n$ , the hysteresis width  $\Delta T1$ , the reduction widths  $\Delta T2$  and  $\Delta T4$ , and the margin width  $\Delta T3$  may be set to a different value among a plurality of electronic components of the same type disposed at different locations, respectively. For example, at least one of the rated temperature  $T_n$ , the hysteresis width  $\Delta T1$ , the reduction widths  $\Delta T2$  and  $\Delta T4$ , and the margin width  $\Delta T3$  may be set to a different value among the plurality of shunt reduction coefficients  $K_{c1}$  to  $K_{c3}$ . The same is true for the low-side FET reduction coefficients  $K_{b1}$  to  $K_{b3}$ , the shunt reduction coefficients  $K_{c1}$  to  $K_{c3}$ , the phase cutoff FET reduction coefficients  $K_{d1}$  to  $K_{d3}$ , the power cutoff FET reduction coefficients  $K_{e1}$  and  $K_{e2}$ , and the capacitor reduction coefficients  $K_{f1}$  and  $K_{f2}$ .

[0243] The selector **64** selects any one of the high-side FET reduction coefficients  $K_{a1}$  to  $K_{a3}$ , the low-side FET reduction coefficients  $K_{b1}$  to  $K_{b3}$ , the shunt reduction coefficients  $K_{c1}$  to  $K_{c3}$ , the phase cutoff FET reduction coefficients  $K_{d1}$  to  $K_{d3}$ , the power cutoff FET reduction coefficients  $K_{e1}$  and  $K_{e2}$ , the capacitor reduction coefficients  $K_{f1}$  and  $K_{f2}$ , and the coil reduction coefficient  $K_g$  as the component reduction coefficient  $K1$ . For example, the selector **64** may select the smallest coefficient out of the above reduction coefficients  $K_{a1}$  to  $K_{a3}$ ,  $K_{b1}$  to  $K_{b3}$ ,  $K_{c1}$  to  $K_{c3}$ ,  $K_{d1}$  to  $K_{d3}$ ,  $K_{e1}$  and  $K_{e2}$ ,  $K_{f1}$  and  $K_{f2}$  and  $K_g$  as the component reduction coefficient  $K1$ .

#### Effect of Second Embodiment

[0244] The current control apparatus according to the second embodiment includes: a current control circuit including a plurality of electronic components; a temperature detection circuit having a temperature detecting element disposed in the vicinity of the current control circuit; a current detecting unit configured to detect or estimate current values flowing to each of the plurality of electronic components; a component temperature estimating unit configured to estimate a component temperature, which is the temperature of the electronic component, for each of the plurality of electronic components based on the current value detected or estimated by the current

detecting unit and the detected temperature detected by the temperature detection circuit; a reduction coefficient setting unit configured to set a plurality of different reduction coefficients for a plurality of different component temperatures included in the component temperature estimated for each of the plurality of electronic components; a selecting unit configured to select any one of the plurality of reduction coefficients; and a current limiting unit configured to limit output current outputted from the current control circuit to a load based on the selected reduction coefficient. The plurality of electronic components includes a plurality of different types of electronic components, and at least one type of electronic component among the plurality of different types of electronic components includes a plurality of electronic components disposed at different locations in the current control circuit. The reduction coefficient setting unit sets a plurality of different reduction coefficients each for a plurality of electronic components disposed at different locations in the current control circuit included in the at least one type of electronic component.

[0245] This can suppress overheating of the plurality of electronic components included in the current control circuit that are susceptible to thermal damage. For example, even when the components with a large heat generation rate change due to the changes in the energizing pattern in the current control circuit, the reduction coefficient can be set according to the components that are more susceptible to thermal damage due to the increase in heat generation rate. The reduction coefficient can be set according to the characteristics of each component (for example, rated voltage) and the component temperature, depending on the component susceptible to thermal damage. By setting the reduction coefficient according to the needs of individual components, excessive limitation of drive current can be suppressed.

### Third Embodiment

[0246] Next, the third embodiment of the present invention will be described. There are two operating modes in which the current control apparatus drives the electric motor. One is a dual-system drive mode in which both the first system coil and the second system coil are driven, and another is a single-system drive mode in which only one of the first system coil and the second system coil is driven. In the dual-system drive mode, drive current is output to motor **20** from both the first current control circuit **40A** and the second current control circuit **40B**, while in the single-system drive mode, drive current is output to motor **20** from only one of them. For example, the current control apparatus operates in dual-system drive mode during normal operation and in single-system drive mode during abnormal conditions.

[0247] In the case of the dual-system drive mode, unlike the case of the single-system drive mode, the component temperature of the electronic components of the first current control circuit **40A** is affected by the heat generated by the electronic components of the second current control circuit **40B**, and conversely, the component temperature of the electronic components of the second current control circuit **40B** is affected by the heat generated by the electronic components of the first current control circuit **40A**. For example, the temperature of the heat-dissipating member **37** is higher in the dual-system drive mode than in the single-system drive mode, resulting in higher component temperatures and temperature sensor temperatures.

[0248] FIG. **14** is a graph illustrating temperatures when a specific magnitude of current is applied in order to investigate trends in component temperatures and temperatures of the temperature sensor during energization in each of the dual-system drive mode and the single-system drive mode. The solid line illustrates the trend of the component temperature of the high-side FET in single-system drive mode, the dashed line illustrates the trend of the component temperature of the high-side FET in dual-system drive mode, the single-dotted chain line illustrates the trend of the temperature of the temperature sensor in single-system drive mode, and the double-dotted chain line illustrates the trend of the temperature of the temperature sensor in the dual-system drive mode.

[0249] As illustrated in FIG. **14**, the component temperatures of the components during energization are higher in the case of the dual-system drive mode than the case of the single-system

drive mode. The temperature of the temperature sensor is also higher in the dual-system drive mode than in the single-system drive mode.

[0250] Furthermore, the difference  $\Delta 1$  in component temperatures between the dual-system drive mode and the single-system drive mode is smaller than the difference  $\Delta 2$  in temperature of the temperature sensor between the dual-system drive mode and the single-system drive mode. It is because the components during energization generate heat by themselves, the temperature rise due to the influence of the ambient high temperature (for example, high temperature of the heat-dissipating member 37) is suppressed.

[0251] As a result, the difference obtained by subtracting the temperature of the temperature sensor from the component temperature is larger in the single-system drive mode than in the dual-system drive mode. FIG. 15 is a graph illustrating temperatures difference (the component temperature minus temperature sensor temperature) when a specific magnitude of current is applied in order to investigate trends in difference between component temperatures and temperatures of the temperature sensor in each of the dual-system drive mode and the single-system drive mode. The solid line illustrates the trend of the difference between the component temperature and the temperature of the temperature sensor in the single-system drive mode, and the dashed line illustrates the trend of the difference between the component temperature and the temperature of the temperature sensor in the dual-system drive mode. As illustrated in FIG. 15, the difference between the component temperature and the temperature of the temperature sensor in the single-system drive mode (solid line) is larger than the difference in the dual-system drive mode (dashed line).

[0252] Now, refer to the high-side FET temperature estimating unit 61a1 in FIG. 7. The gain multiplying unit 73 calculates a product ( $G1 \times W$ ) of the power loss  $W$  and a predetermined conversion gain  $G1$  and output the result to the first low-pass filter 74. The first low-pass filter 74 outputs a signal obtained by applying a low-pass filtering to the product ( $G1 \times W$ ). The output of the first low-pass filter 74 may hereinafter be denoted as LPF ( $G1 \times W$ ).

[0253] The second low-pass filter 75 outputs a signal obtained by applying the low-pass filtering to a detection signal of the temperature sensor (that is, the temperature of the temperature sensor) of the temperature detection circuit 45A to the adder 76 as a base temperature  $T_{th}$ . The output of the second low-pass filter 75 (base temperature  $T_{th}$ ) may hereinafter be denoted as LPF (SdA). The high-side FET temperature estimating unit 61a1 estimates the sum of the output of the first low-pass filter 74 and the output of the second low-pass filter 75 (LPF ( $G1 \times W$ )+LPF (SdA)) as the component temperature of high-side FET Q1.

[0254] The FET component temperature in the graph in FIG. 14 corresponds to the sum (LPF ( $G1 \times W$ )+LPF (SdA)), which is an estimation result of the high-side FET temperature estimating unit 61a1, and the temperature of the temperature sensor in the graph in FIG. 14 corresponds to the output LPF (SdA) of the second low-pass filter 75. Therefore, the difference between the component temperature and the temperature of the temperature sensor in the graph in FIG. 15 corresponds to LPF ( $G1 \times W$ ), the difference obtained by subtracting LPF (SdA) from the sum (LPF ( $G1 \times W$ )+LPF (SdA)), that is, the output of the first low-pass filter 74.

[0255] Therefore, adjusting the output LPF ( $G1 \times W$ ) of the first low-pass filter 74 so that the value for single-system drive mode is larger than the value for dual-system drive mode, as illustrated in FIG. 15 makes it possible to estimate the component temperatures according to the difference in drive modes, and achieve more accurate estimation of the component temperatures.

[0256] In dual-system drive mode, the distribution ratio of the drive current outputted from the first current control circuit 40A and the second current control circuit 40B to the motor 20 can be made different by varying the magnitude of the current command value calculated by the current command value calculating unit 50 of each of the control calculating apparatuses 31a and 31b. When the distribution ratio of these output currents is changed, the magnitude of the difference between the component temperatures and the temperature of the temperature sensor changes for the

same reason as when switching between the dual-system drive mode and the single-system drive mode described above.

[0257] Therefore, the high-side FET temperature estimating unit **61A1** of the third embodiment sets the conversion gain **G1** according to the distribution ratio between the output current of the first current control circuit **40A** and the output current of the second current control circuit **40B**. The same applies to the high-side FET temperature estimating units **61a2** and **61a3**, the low-side FET temperature estimating units **61b1** to **61b3**, the shunt resistance temperature estimating units **61c1** to **61c3**, the phase cutoff FET temperature estimating units **61d1** to **61d3**, the power cutoff FET temperature estimating units **61e1** and **61e2**, the capacitor temperature estimating units **61f1** and **61f2**, and the coil temperature estimating unit **61g**.

[0258] In the following description, the high-side FET temperature estimating units **61a1** to **61a3**, the low-side FET temperature estimating units **61b1** to **61b3**, the shunt resistance temperature estimating units **61c1** to **61c3**, the phase cutoff FET temperature estimating units **61d1** to **61d3**, the power cutoff FET temperature estimating units **61e1** and **61e2**, the capacitor temperature estimating units **61f1** and **61f2**, and the coil temperature estimating unit **61g** may be collectively referred to as “temperature estimating unit **61**”.

[0259] FIG. **16(a)** illustrates an example of setting the conversion gain **G1**. The component temperature estimating unit **61** of the control calculating apparatus **31A** of the first current control circuit **40A** may set a larger conversion gain **G1** for a higher distribution ratio of the first current control circuit **40A**. Similarly, the component temperature estimating unit **61** of the control calculating apparatus **31b** of the second current control circuit **40B** may set a larger conversion gain **G1** for a higher distribution ratio of the second current control circuit **40B**.

[0260] For example, if the distribution ratio is 50%, the conversion gain **G1** is set to the value “**g0**”; if the distribution ratio is 100%, the conversion gain **G1** is set to a value “**g1**” larger than the value “**g0**”; and if the distribution ratio is 0%, the conversion gain **G1** is set to a value “**g2**” smaller than the value “**g0**”.

[0261] In the range of 0% to 50% of the distribution ratio, the conversion gain **G1** is increased from “**g2**” to “**g0**” as the distribution ratio increases, and in the range of 50% to 100% of the distribution ratio, the conversion gain **G1** is increased from “**g0**” to “**g1**” as the distribution ratio increases. For example, the value “**g1**” may be set to a value of about  $(1.1 \times g_0)$  and the value “**g2**” may be set to a value of about  $(0.9 \times g_0)$ .

[0262] As a result, a larger conversion gain **G1** is set in the single-system drive mode than in the dual-system drive mode.

[0263] Refer to FIG. **15**. Focusing on the waveform in the part indicated by an arrow **77**, the waveform of the difference between the component temperature and the temperature of the temperature sensor in the single-system drive mode has a slower response than the waveform of the difference in the dual-system drive mode.

[0264] Therefore, the component temperature estimating unit **61** of the third embodiment sets the first cutoff frequency **fc1** of the first low-pass filter **74** according to the distribution ratio between the output current of the first current control circuit **40A** and the output current of the second current control circuit **40B**.

[0265] FIG. **16(b)** illustrates an example of setting the first cutoff frequency **fc1**. The component temperature estimating unit **61** of the control calculating apparatus **31a** of the first current control circuit **40A** may set a lower first cutoff frequency **fc1** as the distribution ratio of the first current control circuit **40A** increases. Similarly, the component temperature estimating unit **61** of the control calculating apparatus **31b** of the second current control circuit **40B** may set a lower first cutoff frequency **fc1** for a higher distribution ratio of the second current control circuit **40B**.

[0266] For example, if the distribution ratio is 50%, the first cutoff frequency **fc1** is set to the value “**f0**”, if the distribution ratio is 100%, the first cutoff frequency **fc1** is set to the value “**f1**”, which is lower than the value “**f0**”, and if the distribution ratio is 0%, the first cutoff frequency **fc1** is set to

the value “f2”, which is higher than the value “f0.

[0267] In the range of 0% to 50% of the distribution ratio, the first cutoff frequency  $fc1$  is decreased from “f2” to “f0” as the distribution ratio increases, and in the range of 50% to 100% of the distribution ratio, the conversion gain  $G1$  is decreased from “f0” to “f1” as the distribution ratio increases.

[0268] This sets a lower first cutoff frequency  $fc1$  in the single-system drive mode than in the dual-system drive mode.

[0269] FIGS. 17(a) to 17(c) are schematic illustrations illustrating the relationship between the output current distribution ratio between the first current control circuit 40A and the second current control circuit 40B and the conversion gain  $G1$  and the first cutoff frequency  $fc1$ .

[0270] The solid line in FIG. 17(a) illustrates the distribution ratio of the output current of the first current control circuit 40A, and the single-dotted chain line illustrates the distribution ratio of the output current of the second current control circuit 40B.

[0271] FIG. 17(a) illustrates an example where the first current control circuit 40A and the second current control circuit 40B operate in dual-system drive mode during the period before time  $t1$ , and the first current control circuit 40A and the second current control circuit 40B operate in single-system drive mode during time  $t2$  and later.

[0272] In the period before time  $t1$ , the distribution ratio of the output current of the first current control circuit 40A and the second current control circuit 40B is 50%, and between time  $t1$  and time  $t2$ , the distribution ratio of the output current of the first current control circuit 40A increases to 100% and the distribution ratio of the output current of the second current control circuit 40B decreases to 0%. In the period after time  $t2$ , the distribution ratios of the output currents of the first current control circuit 40A and the second current control circuit 40B are 100% and 0%, respectively.

[0273] In this case, the value of the conversion gain  $G1$  of the component temperature estimating unit 61 of the control calculating apparatus 31a of the first current control circuit 40A, illustrated in the solid line in FIG. 17(b), is set to the value “g0” in the period before time  $t1$ , increases to the value “g1” between time  $t1$  and  $t2$ , and is set to the value “g1” after time  $t2$ .

[0274] The value of conversion gain  $G1$  of the component temperature estimating unit 61 of the control calculating apparatus 31b of the second current control circuit 40B, illustrated in the dashed line in FIG. 17(b), is set to the value “g0” in the period before time  $t1$ , decreases to the value “g2” between time  $t1$  and  $t2$ , and is set to the value “g2” after time  $t2$ .

[0275] The value of the first cutoff frequency  $fc1$  of the component temperature estimating unit 61 of the control calculating apparatus 31a of the first current control circuit 40A illustrated in the solid line in FIG. 17(c) is set to the value “f0” in the period before time  $t1$ , decreases to the value “f1” between time  $t1$  and time  $t2$ , and is set to the value “f1” after time  $t2$ .

[0276] The value of the first cutoff frequency  $fc1$  of the component temperature estimating unit 61 of the control calculating apparatus 31b of the second current control circuit 40B illustrated in the dashed line in FIG. 17(c) is set to the value “f0” in the period before time  $t1$ , increases to the value “f2” between time  $t1$  and time  $t2$ , and is set to the value “f2” after time  $t2$ .

### Effect of Third Embodiment

[0277] (1) The component temperature estimating unit may set a predetermined gain according to the distribution ratio between the output currents of a pair of current control circuits, estimate the power loss generated in the electronic components for each of the plurality of electronic components, and estimate the component temperature for each of the plurality of electronic components based on the sum of a value according to the product of the power loss and the predetermined gain and a value according to the detected temperature detected by the temperature detection circuit.

[0278] For example, the component temperature estimating unit may estimate the component temperature of one of the current control circuits based on a predetermined gain that is larger the

higher the distribution ratio of one of the pair of current control circuits.

[0279] The difference between the detected temperature detected by the temperature detection circuit and the actual component temperature varies according to the distribution ratio between the output currents of the pair of current control circuits. Estimating component temperatures based on predetermined gains set according to the distribution ratio makes it possible to estimate component temperatures in accordance with the distribution ratio and to estimate component temperatures more accurately.

[0280] (2) For example, the component temperature estimating unit may set a larger predetermined gain when only one of the pair of current control circuits is driven than when both are driven.

[0281] This enables more estimation of the component temperature according to the difference of the driving mode, and thus enables more accurate estimation of component temperatures.

[0282] (3) The component temperature estimating unit may obtain a value obtained by passing the product of the power loss and the predetermined gain through a first low-pass filter as a value according to the product of the power loss and the predetermined gain and set the cutoff frequency of the first low-pass filter according to the distribution ratio.

[0283] For example, the component temperature estimating unit may estimate the component temperature of one of the pair of current control circuits using the first low-pass filter with a lower cutoff frequency the higher the distribution ratio of one of the current control circuits.

[0284] The component temperature varies according to the distribution ratio between the output currents of a pair of current control circuits. Estimating component temperatures based on predetermined gains set according to the distribution ratio makes it possible to estimate component temperatures in accordance with the distribution ratio and to estimate component temperatures more accurately.

[0285] When the output current of the current control circuit changes, the heat generation rate of the electronic components changes, and the component temperature and the detected temperature detected by the temperature detection circuit also change accordingly. The waveform of the difference between the detected temperature detected by the temperature detection circuit and the actual component temperature has different responses according to the distribution ratio.

[0286] Estimating component temperatures using a first low-pass filter with a cutoff frequency set according to the distribution ratio makes it possible to estimate component temperatures according to the distribution ratio and to estimate component temperatures with higher accuracy.

[0287] (4) The component temperature estimating unit may set the cutoff frequency of the first low-pass filter lower when only one of the pair of current control circuits is driven than when both are driven.

[0288] This enables more estimation of the component temperature according to the difference of the driving mode, and thus enables more accurate estimation of component temperatures.

#### Fourth Embodiment

[0289] FIG. **18** is a block diagram of a first example of the functional configuration of the high-side FET temperature estimating unit **61a1** according to the fourth embodiment.

[0290] In the first embodiment and the second embodiment, the component temperature is estimated based on the sum of a first value obtained by filtering the power loss generated in the electronic component by the first low-pass filter **74** and a second value obtained by filtering the detected temperature detected by the temperature detection circuit **45A** and the temperature detection circuit **45B** by the second low-pass filter **75**.

[0291] In contrast, in the fourth embodiment, the component temperature is estimated for each of the plurality of electronic components based on the sum of the first value obtained by filtering the power loss by a plurality of first low-pass filters **74a** and **74b** connected in parallel and the second value obtained by filtering the detected temperature detected by the temperature detection circuit **45A** and temperature detection circuit **45B** by the second low-pass filter **75**.

[0292] The plurality of first low-pass filters **74a** and **74b** connected in parallel input the signals

obtained by low-pass filtering the multiplication result ( $G1 \times W$ ) of the power loss  $W$  at the high-side FET  $Q1$  of the first power conversion circuit **42A** and the predetermined gain  $G1$  to the adder **76**, respectively. The adder **76** calculates the sum of the output of the first low-pass filter **74a**, the output of the first low-pass filter **74b**, and the output of the second low-pass filter **75** as the component temperature  $Tea1$  of the high-side FET  $Q1$ .

[0293] Thus, calculating as the component temperature  $Tea1$  of the high-side FET  $Q1$  based on the first value obtained by filtering the power loss  $W$  in the high-side FET  $Q1$  of the first power conversion circuit **42A** by a plurality of first low-pass filters **74a** and **74b** connected in parallel makes it possible to improve the estimation accuracy of the component temperature  $Tea1$  of the high-side FET  $Q1$ .

[0294] FIGS. **19(a)** and **19(b)** are schematic illustrations of the temperature estimation results in the first embodiment and the fourth embodiment, respectively, with the solid line illustrating the assumed actual component temperature of the high-side FET  $Q1$  and the dashed line illustrating the estimated component temperature by the high-side FET temperature estimating unit **61a1**. FIGS. **19(c)** and **19(d)** are schematic illustrations of the estimation error between the estimated value (dashed line) and the assumed value (solid line) in FIGS. **19(a)** and **19(b)**, respectively. As used herein the phrase “assumed value” of component temperature is used to mean the value of component temperature assumed based on past performance and experience.

[0295] As can be seen from FIGS. **19(a)** to **19(d)**, filtering through a plurality of first low-pass filters **74a** and **74b** connected in parallel improves the accuracy of estimation of component temperature.

[0296] FIG. **20(a)** is a schematic illustration of an example of the heat dissipation paths from an electronic component to a heat sink. As described above, the electronic components in each of the first power conversion circuits **42A** and the second power conversion circuit **42B**, and the temperature sensors **45A1** and **45A2** in the temperature detection circuit **45A** are mounted on the same circuit board **36**. A surface  $f1$  of the electronic component mounted on the front surface  $ff$  of the circuit board **36** on the opposite side from the circuit board **36** and surfaces  $f2$  of the temperature sensors **45A1** and **45A2** of the temperature detection circuit **45A** on the opposite side from the circuit board **36** are thermally connected to the same heat sink **37**. For example, surfaces  $f1$  and  $f2$  are brought into contact with heat sink **37** via the thermal interface materials **38a** and **38b**, respectively. The temperature sensor of the temperature detection circuit **45B** is also thermally connected to the heat sink **37** in the same configuration as the temperature sensors **45A1** and **45A2**.

[0297] Therefore, the heat generated by the electronic components is transferred in parallel via a first heat dissipation path  $Pth1$ , in which the heat is directly transferred to the heat sink **37** via the thermal interface material **38a**, and a second heat dissipation path  $Pth2$ , in which the heat is transferred to the heat sink **37** via the circuit board **36**. The second heat dissipation path  $Pth2$  has different thermal characteristics (for example, thermal conductivity and heat capacity) from the first heat dissipation path  $Pth1$  because it is a path through the circuit board **36**.

[0298] FIG. **20(b)** is a schematic illustration of another example of the heat dissipation paths from the electronic components to the heat sink. The first electronic component and the second electronic component in each of the first power conversion circuit **42A** and the second power conversion circuit **42B** are mounted on the same circuit board **36**. The sides  $f1a$  and  $f1b$  of these electronic components mounted on the front surface  $ff$  of the circuit board **36**, which are opposite from the circuit board **36**, are thermally connected to the same heat sink **37**. In this structure as well, the heat generated in the first electronic component is transferred in parallel via the first heat dissipation path  $Pth1$  that transfers the heat directly to the heat sink **37** via the thermal interface material **38a** and via the second heat dissipation path  $Pth2$  that transfers the heat to the heat sink **37** via the circuit board **36** having different thermal characteristics from the first heat dissipation path  $Pth1$ .

[0299] FIG. **20(c)** is an equivalent circuit diagram that schematically represents the delayed



response of component temperature when there are a plurality of heat dissipation paths Pth1 and Pth2 that transfer heat generated by electronic components in parallel.

[0300] The first heat dissipation path Pth1 and the second heat dissipation path Pth2 have different heat transfer characteristics. Therefore, it is difficult for a single first low-pass filter 74 to reproduce the delayed response of the temperature change of the electronic components that are dissipated by these heat dissipation paths Pth1 and Pth2.

[0301] Therefore, in the fourth embodiment, the respective delayed responses of the temperature change of the electronic component caused by the heat generated in the electronic component and transferred through the plurality of heat dissipation paths Pth1 and Pth2 are reproduced by the plurality of first low-pass filters 74a and 74b connected in parallel to each other, respectively.

[0302] This enables accurate estimation of the temperature of the electronic component by reproducing the delayed response of the temperature change of the electronic component when the heat generated by the electronic component is dissipated through the plurality of heat dissipation paths Pth1 and Pth2 to the heat sink 37 by the plurality of first low-pass filters 74a and 74b, respectively.

[0303] FIG. 21 is a block diagram of a second example of the functional configuration of the high-side FET temperature estimating unit 61a1 according to the fourth embodiment. In this example, the sum of the values obtained by filtering a plurality of multiplication results obtained by multiplying the power loss  $W$  by a plurality of different predetermined gains, respectively, through a plurality of first low-pass filters is calculated as the first value. In the example in FIG. 21, when values obtained by filtering the a plurality of multiplication results  $G1a \times W$  and  $G1b \times W$ , obtained by multiplying the power loss  $W$  by different predetermined gains  $G1a$  and  $G1b$ , respectively, through the plurality of first low-pass filters 74a and 74b, respectively, are represented as LPF1a ( $G1a \times W$ ) and LPF1b ( $G1b \times W$ ), respectively, the sum of these values, LPF1a ( $G1a \times W$ ) + LPF1b ( $G1b \times W$ ), is calculated as the first value.

[0304] In this manner, by setting different values of gains  $G1a$  and  $G1b$  for the first low-pass filters 74a and 74b, respectively, it is possible to reflect differences in the thermal characteristics of heat dissipation paths Pth1 and Pth2 on the estimated values. As a result, the accuracy of component temperature estimation can be improved.

[0305] Of the first heat dissipation path Pth1 and the second heat dissipation path Pth2 schematically illustrated in FIGS. 20(a) and 20(b), the second heat dissipation path Pth2 dissipates heat generated by the electronic components through both a plurality of materials (circuit board 36 and heat sink 37) that are made of materials with significantly different thermal characteristics. Therefore, the delayed response of the temperature change of the electronic component when dissipating heat through the second heat dissipation path Pth2 may be reproduced by a second-order or higher low-pass filter equivalent to a series connection of a plurality of first-order low-pass filters.

[0306] For this reason, any of the plurality of first low-pass filters 74a and 74b connected in parallel may be a second-order or higher low-pass filter.

[0307] Other component temperature estimating units such as the high-side FET temperature estimating units 61a2 and 61a3, the low-side FET temperature estimating units 61b1 to 61b3, the shunt resistance temperature estimating units 61c1 to 61c3, the phase cutoff FET temperature estimating units 61d1 to 61d3, the power cutoff FET temperature estimating units 61e1 and 61e2, and the coil temperature estimating unit 61g may have the same configuration as the high-side FET temperature estimating unit 61a1 illustrated in FIG. 18 or FIG. 21.

[0308] For electronic components mounted on the back surface fr of the circuit board 36, the first heat dissipation path Pth1 where heat generated by the electronic components is directly transferred to the heat sink 37 via the thermal interface material does not exist. Therefore, the temperature estimating unit that estimates the component temperature of electronic components mounted on the back surface fr of the circuit board 36 does not have to employ the configuration illustrated in FIG.

**18** or FIG. **21**. For example, if the electrolytic capacitors **CA1** and **CA2** are mounted on the back surface of the circuit board **36**, the capacitor temperature estimating units **61f1** and **61f2** do not have to employ the configuration illustrated in FIG. **18** or FIG. **21**.

#### Effect of Fourth Embodiment

[0309] (1) The current control apparatus according to the fourth embodiment includes: a current control circuit including a plurality of electronic components; a temperature detection circuit having a temperature detecting element disposed in the vicinity of the current control circuit; a current detecting unit configured to detect or estimate current values flowing to each of the plurality of electronic components; a component temperature estimating unit configured to estimate a component temperature, which is the temperature of the electronic component, for each of the plurality of electronic components based on the current value detected or estimated by the current detecting unit and the detected temperature detected by the temperature detection circuit; a reduction coefficient setting unit configured to set a plurality of different reduction coefficients for a plurality of different component temperatures included in the component temperature estimated for each of the plurality of electronic components; a selecting unit configured to select any one of the plurality of reduction coefficients; and a current limiting unit configured to limit output current outputted from the current control circuit to a load based on the selected reduction coefficient.

[0310] The component temperature estimating unit estimates the power loss generated in each electronic component for each of the plurality of electronic components, and estimates the component temperature for each of the plurality of electronic components based on the sum of the first value obtained by filtering the power loss through a plurality of first low-pass filters connected in parallel with each other and a second value obtained by filtering the detected temperature detected by a temperature detection circuit through a second low-pass filter. For example, the first value may be obtained by filtering the result of multiplying the power loss by a predetermined gain through a plurality of first low-pass filters.

[0311] This allows accurate estimation of component temperatures in cases where heat generated in one electronic component is dissipated by transferring heat through a plurality of heat dissipation paths that exist in parallel.

[0312] (2) The plurality of electronic components and the temperature detecting element may be mounted on the same circuit board, and the surface opposite from the circuit board side of a first component, which is one of the plurality of electronic components, and a surface opposite from the circuit board side of the temperature detecting element or a second component other than the first component of the plurality of electronic components may be thermally coupled to the same heat sink.

[0313] This allows each delayed response of temperature change of electronic components that are dissipated by a heat dissipation path that dissipates heat at the heat sink without passing through the circuit board and a heat dissipation path that dissipates heat while passing through the circuit board, respectively, to be reproduced by a plurality of first low-pass filters that are connected in parallel to each other.

[0314] (3) The component temperature estimating unit may acquire the sum of the values obtained by filtering a plurality of multiplication results obtained by multiplying the power loss  $W$  by a plurality of different predetermined gains, respectively, through a plurality of first low-pass filters as the first value.

[0315] In this manner, setting different values of the predetermined gain for the different first low-pass filters enables reflection of differences in the thermal characteristics of the heat dissipation paths in the estimated values. As a result, the accuracy of component temperature estimation can be improved.

[0316] (4) At least one of the plurality of first low-pass filters may be a second-order or higher low-pass filter.

[0317] This allows accurate estimation of the delayed response of temperature change of electronic

components that are dissipated through a plurality of members made of materials with significantly different thermal characteristics.

#### Fifth Embodiment

[0318] For example, the high-side FET temperature estimating unit **61a1** of the fourth embodiment estimates the component temperatures of the electronic components included in the current control apparatus and are mounted on the front surface ff of the circuit board **36**, as illustrated in FIGS. **20(a)** and **20(b)**. The electronic component is disposed between the circuit board **36** and the heat sink **37**, and the side f1 facing away from the circuit board **36** is thermally connected to the heat sink **37**. The heat generated by the electronic component is dissipated to the heat sink **37** directly or through the thermal interface material **38a**.

[0319] On the other hand, some of the electronic components included in the current control apparatus are mounted on the back surface fr on the opposite the front surface ff facing the heat sink **37** out of the front surface ff and the back surface fr of the circuit board **36**.

[0320] In the following description, for example, a case where the electrolytic capacitors CA1 and CA2, which connect a positive pole wire and a negative pole wire of the inverter, are mounted on the back surface fr will be exemplified. However, the present invention is not intended to limit the electronic components mounted on the back surface fr of the circuit board **36** to electrolytic capacitors CA1 and CA2. Which of the electronic components included in the current control apparatus will be mounted on the face fr of the circuit board **36** facing away from the heat sink **37** depends on the individual product.

[0321] In the case of electronic components mounted on the back surface fr of the circuit board **36**, the heat generated by the electronic components is dissipated to the heat sink **37** through the circuit board **36** and also through the components interposed between the circuit board **36** and the heat sink **37** (such as other electronic components and temperature sensors mounted on the front surface ff) and interposers (such as a thermal interface material applied on the front surface ff, etc.). This complicates the heat transfer paths and may make it difficult for a first-order low-pass filter alone to accurately estimate the amount of rise in component temperature of electronic components from the power loss of the electronic components.

[0322] Therefore, in the fifth embodiment, the amount of rise in component temperature due to heat generation of electronic components is estimated by filtering the power loss by a plurality of first low-pass filters connected in series.

[0323] FIG. **22** is a block diagram of a first example of the functional configuration of a capacitor temperature estimating unit **61f1** according to a fifth embodiment. The capacitor temperature estimating unit **61f1** estimates the component temperature of the electrolytic capacitor CA1 of the first power conversion circuit **42A** mounted on the back surface fr of the circuit board **36**. The capacitor temperature estimating unit **61f2**, which estimates the component temperature of the electrolytic capacitor CA2 mounted on the back surface fr of the circuit board **36**, may also have the same functional configuration as illustrated in FIG. **22**.

[0324] The capacitor temperature estimating unit **61f1** of the fifth embodiment estimates the component temperature for each of the plurality of electronic components based on the sum of the first value obtained by filtering the power loss W calculated by the power loss calculating unit **72** through the plurality of first low-pass filters **74a** and **74c** connected in series, and the second value obtained by filtering the detected temperature detected by the temperature detection circuits **45A** and **45B** through the second low-pass filter **75**.

[0325] The power loss calculating unit **72** of the capacitor temperature estimating unit **61f1** of the fifth embodiment calculates the power loss W of the electrolytic capacitor CA1 based on the phase A current I1ad, the phase B current I1bd and the phase C current I1cd according to the following calculation formula.

$$[00015] W = G_a \times I_{1ad}^2 + G_b \times I_{1bd}^2 + G_c \times I_{1cd}^2$$

[0326] In other words, the capacitor temperature estimating unit **61f1** of the fifth embodiment

calculates the power loss  $W$  based on the weighted sum of the squared values of each of the phase A current  $I1ad$ , the phase B current  $I1bd$ , and the phase C current  $I1cd$ .

[0327] Note that in the capacitor temperature estimating unit **61f1** of the fifth embodiment, the power loss  $W$  of the electrolytic capacitor **CA1** may be calculated based on the following calculation formula as in the capacitor temperature estimating unit **61f1** of the first embodiment to the fourth embodiment.

$$[00016] W = Rf \times (Id^2 + Iq^2)$$

[0328] Among a plurality of first low-pass filters **74a** and **74c** connected in series, the first low-pass filter **74a** in the first stage performs low-pass filtering on the multiplication results ( $G1 \times W$ ) of the power loss  $W$  in the electrolytic capacitor **CA** and the predetermined gain **G1**. The first low-pass filter **74c** in the second stage inputs the signals obtained by low-pass filtering the output of the first low-pass filter **74a** in the first stage to the adder **76**, respectively. The adder **76** calculates the sum of the output of the first low-pass filter **74c** and the output of the second low-pass filter **75** as the component temperature  $Tef1$  of the electrolytic capacitor **CA**.

[0329] In this manner, the estimation accuracy of the component temperature  $Tef1$  of the electrolytic capacitor **CA** mounted on the back surface **fr** of the circuit board **36** can be improved by calculating the power loss  $W$  of the electrolytic capacitor **CA1** based on the phase A current  $I1ad$ , the phase B current  $I1bd$ , and the phase C current  $I1cd$ , and calculating the component temperature  $Tef1$  of the electrolytic capacitor **CA** based on the first value obtained by filtering the calculated power loss  $W$  through the plurality of first low-pass filters **74a** and **74c** connected in series.

[0330] FIGS. **23(a)** and **23(b)** are schematic illustrations of the temperature estimation results in the first embodiment and the fifth embodiment, respectively, with the solid line illustrating the assumed value of the actual component temperature of the electrolytic capacitor **CA** and the dashed line illustrating the estimated value of the component temperature by the capacitor temperature estimating unit **61f1**. FIGS. **23(c)** and **23(d)** are schematic illustrations of the estimation error between the estimated value (dashed line) and the assumed value (solid line) in FIGS. **23(a)** and **23(b)**, respectively.

[0331] As can be seen from FIGS. **23(a)** to **23(d)**, it is understood that the accuracy of estimation of component temperature is found to be improved by calculating the power loss  $W$  of the electrolytic capacitor **CA1** based on the phase A current  $I1ad$ , the phase B current  $I1bd$ , and the phase C current  $I1cd$ , and by filtering the power loss  $W$  through the a plurality of first low-pass filters **74a** and **74c** connected in series.

[0332] Next, referring to FIGS. **24(a)** to **24(f)**, the reason the accuracy of estimation of component temperature is improved by calculating the power loss  $W$  of electrolytic capacitor **CA1** based on the phase A current  $I1ad$ , the phase B current  $I1bd$ , and the phase C current  $I1cd$  will be described.

[0333] FIGS. **24(a)** to **24(c)** are image diagrams of the waveforms of the estimated value of the component temperature by the capacitor temperature estimating unit **61f1** (dashed line) and the waveforms of the assumed value of the actual component temperature of the electrolytic capacitor **CA** (solid line) when the power loss  $W$  of the electrolytic capacitor **CA1** is calculated based on d-axis current  $id$  and q-axis current  $iq$ .

[0334] FIGS. **24(d)** to **24(f)** are image diagrams of the waveforms of the estimated value of the component temperature by the capacitor temperature estimating unit **61f1** (dashed line) and the waveforms of the assumed value of the actual component temperature of the electrolytic capacitor **CA** (solid line) when the power loss  $W$  of the electrolytic capacitor **CA1** is calculated based on the phase A current  $I1ad$ , the phase B current  $I1bd$ , and the phase C current  $I1cd$ .

[0335] The waveforms in FIGS. **24(a)** and **24(d)** are obtained when the duty ratio  $Da$  of the phase A is set to the maximum among the duty ratios  $Da$  to  $Dc$  of the phase A to the phase C. The waveforms in FIG. **24(g)** below are similar. Periods of rising and falling component temperatures indicate periods when the component is energized and de-energized, respectively. Such a waveform

can be reproduced, for example, by controlling the rotational angle of the rotating shaft of the motor **20** to be fixed at a specific angle.

[0336] The waveforms in FIGS. **24(b)**, **24(e)** and **24(h)** are obtained when the duty ratio  $D_b$  of the phase B is set to maximum, and the waveforms in FIGS. **24(c)**, **24(f)** and **24(i)** are obtained when the duty ratio  $D_c$  of the phase C is set to maximum.

[0337] Referring to FIGS. **24(a)** to **24(c)**, the assumed value of the actual component temperatures (solid lines) of the electrolytic capacitors CA are lower when the phase B duty ratio  $D_b$  is maximum (FIG. **24(b)**) than when the phase A duty ratio  $D_a$  is maximum (FIG. **24(a)**), and it is higher when the phase C duty ratio  $D_c$  is maximum (FIG. **24(c)**) than when the phase A duty ratio  $D_a$  is maximum (FIG. **24(a)**).

[0338] This is considered to be because the components that generate heat when the phase A current  $I_{1ad}$ , the phase B current  $I_{1bd}$ , and the phase C current  $I_{1cd}$  flow (electronic components and power line wiring) differ in their respective distances to the electrolytic capacitor CA and the heat generated by these components has a different effect on the electrolytic capacitor CA.

[0339] Therefore, when calculating the power loss  $W$  of the electrolytic capacitor CA1, the power loss  $W$  is calculated based on the phase A current  $I_{1ad}$ , the phase B current  $I_{1bd}$  and the phase C current  $I_{1cd}$ , and the weighting coefficients  $G_a$ ,  $G_b$  and  $G_c$  are adjusted to compensate differences in the respective distances from each of the high-side FETs Q1, Q3, and Q5 to the electrolytic capacitor CA, so that the magnitude of the waveform of the estimated value of the component temperature by the capacitor temperature estimating unit **61f1** (dashed line) can be brought closer to the magnitude of the waveform of the assumed value of the actual component temperature of the electrolytic capacitor CA (solid line) as illustrated in the dashed lines in FIG. **24(d)** through FIG. **24(f)**.

[0340] However, simply by adjusting the weighting coefficients  $G_a$ ,  $G_b$  and  $G_c$ , the maximum value of the waveform of the estimated value (dashed line) can be matched to the maximum value of the waveform of the assumed value (solid line) of the actual component temperature of electrolytic capacitor CA, but the shape deviation between the shape of the waveform of the estimated value (dashed line) and the shape of the waveform of the assumed value (solid line) cannot be adjusted.

[0341] Therefore, the reproducibility of the waveform of the estimated value by the capacitor temperature estimating unit **61f1** can be improved by filtering the power loss  $W$  through a plurality of first low-pass filters **74a** and **74c** connected in series. Here, for example, the characteristics of the first low-pass filters **74a** and **74c** are adjusted so that the estimation error of the shape of the waveform of the estimated value (dashed line) relative to the shape of the waveform of the assumed value (solid line) is minimized.

[0342] FIGS. **24(g)** to **24(i)** are image diagrams of the waveform of the estimated value of the component temperature by the capacitor temperature estimating unit **61f1** (dashed line) and the waveform of the assumed value of the actual component temperature of the electrolytic capacitor CA (solid line) when the power loss  $W$  is filtered by the plurality of first low-pass filters **74a** and **74c** connected in series. As illustrated in FIGS. **24(g)** to **24(i)**, the waveform of the estimated value of the component temperature by the capacitor temperature estimating unit **61f1** (dashed line) is closer to the waveform of the assumed value (solid line), that is, reproducibility is improved.

[0343] Next, the reason the use of the plurality of first low-pass filters **74a** and **74c** connected in series improves the reproducibility of the waveform of the estimated value by the capacitor temperature estimating unit **61f1** will be discussed. FIG. **25(a)** is a schematic illustration of an example of the heat dissipation path from the electronic component ecr mounted on the back surface fr of the circuit board **36** to the heat sink.

[0344] The electronic components ecr are mounted on the back surface fr of the circuit board **36**, and the electronic components ecf and temperature sensors **45A1** and **45A2** are mounted on the front surface ff on the opposite side of the circuit board **36** from the back surface fr and are

thermally coupled to the heat sink **37** via the thermal interface materials **38a** and **38b**.  
[0345] For example, the surface **f1** of the electronic component **ecf** on the opposite side from the circuit board **36** is thermally coupled to the heat sink **37** via the thermal interface material **38a**, so that the front surface **ff** of the circuit board **36** is thermally coupled to the heat sink **37** via the electronic component **ecf**. The surface **f2** of the temperature sensors **45A1** and **45A2** opposite from the circuit board **36** side is thermally coupled to the heat sink **37** via the thermal interface material **38b**, so that the front surface **ff** of the circuit board **36** is thermally coupled to the heat sink **37** via the temperature sensors **45A1** and **45A2**. The front surface **ff** of the circuit board **36** is thermally coupled to the heat sink **37** via a thermal interface material **38a** interposed between the circuit board **36** and the heat sink **37**.

[0346] Therefore, the heat generated by the electronic component **ecr** mounted on the back surface **fr** of the circuit board **36** is dissipated from the electronic component **ecr** to the circuit board **36** via the heat dissipation path **Pth3**, and then pass from the circuit board **36** to the heat sink **37** through the heat dissipation path **Pth1** passing through the electronic component **ecf** and the thermal interface material **38a** interposed therebetween and is dissipated to the heat sink **37**. The heat dissipation path **Pth3** and the heat dissipation path **Pth1** have different thermal characteristics (for example, thermal conductivity and heat capacity), which complicates the path of heat transfer from the electronic component **ecr** to the heat sink **37**.

[0347] FIG. **25(b)** is an equivalent circuit diagram that schematically represents the delayed response of component temperature when the heat generated in the electronic component **ecr** is transferred in series through the heat dissipation paths **Pth3** and **Pth1**.

[0348] Heat transfer characteristics are different between heat dissipation path **Pth3** and heat dissipation path **Pth1**. Therefore, it is difficult for a single first low-pass filter **74** to reproduce the delayed response of the temperature change of the electronic components that are dissipated by these heat dissipation paths **Pth3** and **Pth1**.

[0349] Therefore, in the fifth embodiment, the respective delayed responses of the temperature change of the electronic component caused by the heat generated in the electronic component **ecr** and transferred through the heat dissipation paths **Pth3** and **Pth1** are reproduced by the plurality of first low-pass filters **74a** and **74c** connected in series to each other, respectively.

[0350] This reproduces the delayed response of the temperature change of the electronic component **ecr** when the heat generated in the electronic component **ecr** is transferred in series through the heat dissipation paths **Pth3** and **Pth1** to the heat sink **37** by the plurality of first low-pass filters **74a** and **74c**, respectively, so that the temperature of the electronic component **ecr** on the back surface **fr** of the circuit board **36** can be estimated with high accuracy.

[0351] Heat dissipation paths through which heat generated in the electronic component **ecr** is transferred from the circuit board **36** to the heat sink **37** also include a heat dissipation path **Pth4** through which the heat is transferred through, other than the electronic component **ecf**, other electronic components mounted on the front surface **ff** of the circuit board **36**, the temperature sensors **45A1** and **45A2**, the thermal interface material **38a**, **38b** in parallel with the heat dissipation path **Pth1**.

[0352] For this purpose, a first low-pass filter **74d** may be connected in parallel to the first low-pass filter **74c** to reproduce the delayed response of the temperature change of the electronic component **ecr** due to heat dissipation via the heat dissipation path **Pth4** as illustrated in FIG. **25(c)**.

[0353] However, in the example in FIG. **25(a)**, from the perspective of the electronic component **ecf**, both heat dissipation paths **Pth1** and **Pth4** dissipate heat via circuit board **36**. Therefore, the characteristics of the first low-pass filter **74c** and the first low-pass filter **74d** are considered to be closer, and the first low-pass filter **74c** and the first low-pass filter **74d** may be realized with a single first low-pass filter **74c**.

[0354] If the effect of the first low-pass filter **74c** is dominant, the first low-pass filter **74d** may be omitted because the effect of connecting the first low-pass filter **74d** in parallel to the first low-pass

filter **74c** is reduced.

[0355] Furthermore, the arrangement of electronic components in current control apparatuses can take various forms depending on the actual product, and the heat dissipation paths for the heat generated by these electronic components can also take various forms. Therefore, a plurality of first low-pass filters **74** connected in various connection configurations may be used as the first low-pass filter **74** that filters the power loss **W** calculated by the power loss calculating unit **72**, depending on the arrangement configuration of the electronic components.

[0356] Now, for the sake of convenience of explanation, the high-side FET temperature estimating units **61a1** to **61a3**, the low-side FET temperature estimating units **61b1** to **61b3**, the shunt resistance temperature estimating units **61c1** to **61c3**, the phase cutoff FET temperature estimating units **61d1** to **61d3**, the power cutoff FET temperature estimating units **61e1** and **61e2**, the capacitor temperature estimating units **61f1** and **61f2**, and the coil temperature estimating unit **61g** may be collectively referred to as “component temperature estimating unit **61**”.

[0357] For example, the first reduction coefficient setting unit **60** of the fifth embodiment may have both the component temperature estimating unit **61** configured similar to the high-side FET temperature estimating unit **61a1** illustrated in FIG. **18** or FIG. **21** and a component temperature estimating unit **61** configured similarly to the capacitor temperature estimating unit **61f1** illustrated in FIG. **22** or FIG. **25(c)**.

[0358] For example, the component temperature estimating unit **61**, configured similarly to the high-side FET temperature estimating unit **61a1** illustrated in FIG. **18** or FIG. **21**, may estimate the electronic components mounted on the front surface **ff** of the circuit board **36**, and the component temperature estimating unit **61**, configured similarly to the capacitor temperature estimating unit **61f1**, illustrated in FIG. **22** or FIG. **25(c)** may estimate the electronic components mounted on the back surface **fr** of the circuit board **36**.

[0359] FIGS. **26(a)** and **26(b)** illustrate block diagrams of the first modification and the second modification of the component temperature estimating unit **61**.

[0360] In FIGS. **26(a)** and **26(b)**, illustration of the input signals to the power loss calculating unit **72** is omitted. This is because the calculation formula of the power loss **W** in the power loss calculating unit **72** differs depending on the high-side FET temperature estimating units **61a1** to **61a3**, the low-side FET temperature estimating units **61b1** to **61b3**, the shunt resistance temperature estimating units **61c1** to **61c3**, the phase cutoff FET temperature estimating units **61d1** to **61d3**, the power cutoff FET temperature estimating units **61e1**, **61e2**, the capacitor temperature estimating units **61f1** and **61f2**, and the coil temperature estimating unit **61g**.

[0361] For example, the component temperature estimating unit **61** may include a parallel-series connection of first low-pass filters **74**, consisting of a plurality of first low-pass filters **74** connected in parallel, with other first low-pass filters **74** connected in series. For example, the component temperature estimating unit **61** illustrated in FIG. **26(a)** may filter the power loss **W** computed by the power loss calculating unit **72** by a parallel-series connection of the first low-pass filters **74a** to **74d** formed by connecting in series the first low-pass filters **74a** and **74b** connected in parallel with the first low-pass filters **74c** and **74d** connected in parallel.

[0362] Alternatively, for example, the component temperature estimating unit **61** may include a series-parallel connection of first low-pass filters **74**, consisting of a plurality of first low-pass filters **74** connected in series, with other first low-pass filters **74** connected in parallel. For example, the component temperature estimating unit **61** illustrated in FIG. **26(b)** may filter the power loss **W** calculated by the power loss calculating unit **72** by a series-parallel connection of the first low-pass filters **74a** to **74d** formed by connecting in parallel the first low-pass filters **74a** and **74c** connected in series with the first low-pass filters **74b** and **74d** in series.

#### Effect of Fifth Embodiment

[0363] (1) The current control apparatus according to the embodiment includes: a current control circuit including a plurality of electronic components; a temperature detection circuit having a

temperature detecting element disposed in the vicinity of the current control circuit; a current detecting unit configured to detect or estimate current values flowing to each of the plurality of electronic components; a component temperature estimating unit configured to estimate a component temperature, which is the temperature of the electronic component, for each of the plurality of electronic components based on the current value detected or estimated by the current detecting unit and the detected temperature detected by the temperature detection circuit; a reduction coefficient setting unit configured to set a plurality of different reduction coefficients for a plurality of different component temperatures included in the component temperature estimated for each of the plurality of electronic components; a selecting unit configured to select any one of the plurality of reduction coefficients; and a current limiting unit configured to limit output current outputted from the current control circuit to a load based on the selected reduction coefficient.

[0364] The component temperature estimating unit estimates the power loss generated in each electronic component for each of the plurality of electronic components, and estimates the component temperature for any one of the plurality of electronic components based on the sum of the first value obtained by filtering the power loss through a plurality of first low-pass filters connected in series with each other and a second value obtained by filtering the detected temperature detected by a temperature detection circuit through a second low-pass filter. For example, the first value may be obtained by filtering the result of multiplying the power loss by a predetermined gain through a plurality of first low-pass filters. This allows accurate estimation of component temperatures when heat generated in electronic components is dissipated via various members and interposers between the electronic component and the heat-dissipating member.

[0365] (2) Either electronic component may be mounted on a first side of the circuit board, and a second side of the circuit board opposite the first side may be thermally coupled to a heat sink. This allows accurate estimation of component temperatures of electronic components mounted on the first side of the circuit board facing away from the heat sink.

[0366] (3) At least one of the plurality of first low-pass filters may be a second-order or higher low-pass filter. This allows accurate estimation of the delayed response of temperature change of electronic components that are dissipated through a plurality of members made of materials with significantly different thermal characteristics.

[0367] (4) The component temperature estimating unit may estimate the component temperature of other electronic components other than any of the electronic components based on the sum of a third value obtained by filtering the power loss through a plurality of second low-pass filters connected in parallel with each other and a second value obtained by filtering the detected temperature detected by the temperature detection circuit through the second low-pass filter. This allows accurate estimation of component temperatures in cases where heat generated in other electronic components is dissipated by transferring heat through a plurality of heat dissipation paths that exist in parallel.

[0368] (5) Either electronic component may be mounted on the first side of the circuit board, the other electronic components may be mounted on the second side of the circuit board opposite the first side, the side opposite from the circuit board of the other electronic components may be thermally coupled to the heat sink, and the second side of the circuit board may be thermally coupled to the heat sink via other electronic components, a temperature detecting element mounted on the second side, or a thermal interface material. This allows accurate estimation of the component temperatures of the respective electronic components mounted on the first and second sides of the circuit board.

[0369] (6) The component temperature estimating unit may estimate the component temperature of each of the plurality of electronic components based on the sum of a first value obtained by filtering the power loss through the plurality of first low-pass filter connected in parallel-series or connected in series-parallel and a second value obtained by filtering the detected temperature detected by the temperature detection circuit through the second low-pass filter for each of a



plurality of electronic components. This allows the selection of a first low-pass filter **74** with various delay characteristics according to the arrangement configuration of electronic components included in the current control apparatus.

[0370] (7) The current control circuit is an inverter circuit, and any of the electronic components may be a smoothing capacitor connecting the positive pole wire and the negative pole wire of the inverter circuit. This allows accurate estimation of the component temperature of the smoothing capacitor when the heat generated by the smoothing capacitor is dissipated through various members and interposers between the smoothing capacitor and the heat-dissipating member.

[0371] (8) The current control circuit is an inverter circuit, the plurality of electronic components includes a smoothing capacitor connecting the positive pole wire and the negative pole wire of the inverter circuit, and the component temperature estimating unit may estimate the power loss generated in the smoothing capacitor based on the magnitude of the phase current of the inverter circuit. This reduces the variation in the estimated values of the component temperatures that occurs as a result of differences in the distance between the switching and smoothing capacitors in the inverter circuit.

#### Sixth Embodiment

[0372] The high-side FET temperature estimating unit **61a1** illustrated in FIG. 7 has a first low-pass filter **74** for estimating the component temperature  $T_{ea1}$  of the high-side FET **Q1**. The first low-pass filter **74** is composed of an integrating circuit, and when the ECU **30** stops operation (that is, when the first current control circuit **40A** and the second current control circuit **40B** stop), the delay element of the integrating circuit is reset. In the following description, the first current control circuit **40A** and the second current control circuit **40B** may be collectively referred to as the current control circuit **40**.

[0373] The resetting of the delay element of the integrating circuit is caused, for example, by momentary fluctuations in the battery voltage of the battery **13**, a failure of the connector of the battery **13**, a forced resetting of the control calculating apparatuses **31a** and **31b** by the system check function of the ECU **30**, or the ignition switch **11** being turned off, which causes the first reduction coefficient setting unit **60** stops functioning and the temperature estimation of the component temperature  $T_{ea1}$  of the high-side FET **Q1** cannot be continued.

[0374] When the delay element of the integrating circuit are reset, the high-side FET temperature estimating unit **61a1** cannot estimate the proper component temperature  $T_{ea}$  unless the integrating circuit is operated after setting an appropriate initial value for the delay element of the first low-pass filter **74**.

[0375] Therefore, the high-side FET temperature estimating unit **61a1** of the sixth embodiment sets the initial value of the component temperature estimated by the high-side FET temperature estimating unit **61a1** based on the first detected temperature  $T_{d1}$  and the second detected temperature  $T_{d2}$  detected at two locations in the vicinity of the current control circuit **40** when resuming operation after the stop of the ECU **30**.

[0376] In the following description, the high-side FET temperature estimating unit **61a1** is exemplified, but the high-side FET temperature estimating units **61a2** and **61a3**, the low-side FET temperature estimating units **61b1** to **61b3**, the shunt resistance temperature estimating units **61c1** to **61c3**, the phase cutoff FET temperature estimating units **61d1** to **61d3**, the power cutoff FET temperature estimating units **61e1** and **61e2**, the capacitor temperature estimating units **61f1** and **61f2**, and the coil temperature estimating unit **61g** may be considered to have the similar configuration as the high-side FET temperature estimating unit **61a1**.

[0377] The temperature detecting elements for detecting the first detected temperature  $T_{d1}$  and the second detected temperature  $T_{d2}$  should be installed at a sufficient distance from each other so that a temperature difference occurs between the first detected temperature  $T_{d1}$  and the second detected temperature  $T_{d2}$ , and the installation position is not particularly limited.

[0378] Refer to FIG. 27. For example, temperature detectors **46A** and **46B** in the IC packages of

control calculating apparatuses **31a** and **31b** may be used as temperature detecting elements for detecting one of the first detected temperature **Td1** and the second detected temperature **Td2**.  
[0379] The temperature detection circuit **45A** or **45B** may be used as a temperature detecting element for the other one of the first detected temperature **Td1** or the second detected temperature **Td2**

[0380] In this manner, the temperature detecting elements for detecting the first detected temperature **Td1** and the second detected temperature **Td2** may be provided in the IC package of any of the ICs constituting the ECU **30** or may be provided in the vicinity of the current control circuit **40** separately from the IC package.

[0381] FIG. **28** is a block diagram of an example of the functional configuration of the high-side FET temperature estimating unit **61a1** according to the sixth embodiment. The high-side FET temperature estimating unit **61a1** of the sixth embodiment has an initial value setting unit **78** and a subtractor **79**.

[0382] The initial value setting unit **78** calculates the initial value  $T_{ini}$  of the estimated value of the component temperature **Tea1** at the time when the ECU **30** resumes operation based on the first detected temperature **Td1** and the second detected temperature **Td2** at the time when the ECU **30** stops operation, the estimated value of the component temperature **Tea1** outputted by the high-side FET temperature estimating unit **61a1** at the time when the ECU **30** stops operation, the first detected temperature **Td1** and the second detected temperature **Td2** at the time when the ECU **30** resumes operation.

[0383] Hereinafter, the first detected temperature **Td1** and the second detected temperature **Td2** at the time when ECU **30** stopped operation are referred to as “first detected temperature **Td1e** and second detected temperature **Td2e** at the time of stop,” the estimated value of the component temperature **Tea1** outputted by the high-side FET temperature estimating unit **61a1** at the time when ECU **30** stopped operation is referred to as “estimated value **Teale** of the component temperature **Tea1** at the time of stop” and the first detected temperature **Td1** and the second detected temperature **Td2** at the time when ECU **30** resumes operation may be referred to as “first detected temperature **Td1r** and second detected temperature **Td2r** at the time of resumption”.

[0384] In the following explanation, the case in which the detection signal **SdA** of the temperature of ECU **30** outputted by temperature detection circuit **45A** is used as the first detected temperature **Td1** is exemplified, but the detection signal **SdA** of the temperature of ECU **30** outputted by temperature detection circuit **45A** may be used as the second detected temperature **Td2**.

[0385] When the ECU **30** stops operation, the initial value setting unit **78** stores the first detected temperature **Td1** and the second detected temperature **Td2**, which were last inputted when the ECU **30** stopped operation, as the first detected temperature **Td1e** and the second detected temperature **Td2e** at the time of stop. The estimated value of the component temperature **Tea1** last outputted by the high-side FET temperature estimating unit **61a1** when the ECU **30** operation is stopped is stored as the estimated value **Teale** of the component temperature **Tea1** at the time of stop.

[0386] When the ECU **30** resumes operation, the initial value setting unit **78** acquires the first detected temperature **Td1r** and the second detected temperature **Td2r** at the time of resumption.

[0387] The initial value setting unit **78** calculates the ratio of the temperature difference between the first detected temperature **Td1e** and the second detected temperature **Td2e** at the time of stop ( $Td2e - Td1e$ ) to the temperature difference between the first detected temperature **Td1r** and the second detected temperature **Td2r** at the time of resumption ( $Td2r - Td1r$ ) as the first estimated gain  $Ge1 = (Td2r - Td1r) / (Td2e - Td1e)$ .

[0388] FIG. **29(a)** is a schematic illustration of the first detected temperature **Td1** (solid line) and the second detected temperature **Td2** (dashed line) and the assumed value of the component temperature **Tea1** of the high-side FET **Q1** to be estimated (single-dotted chain line) after ECU **30** stops operation at time  $t=0$ . FIG. **29(b)** is a schematic illustration of the first estimated gain **Ge1** calculated based on the first detected temperature **Td1** and the second detected temperature **Td2** in

FIG. 29(a). FIG. 29(a) illustrates an example where the delayed response of the temperature drop of the component temperature Tea1 to be estimated after ECU 30 stops operation is slower than the delayed response of the temperature drop of the second detected temperature Td2.

[0389] For example, U.S. Pat. No. 6,569,447 describes a temperature estimation method for calculating the estimated value of the component temperature Tea1 at the time of resumption ( $Ge1 \times (Tea1e - Td1e)$ ) by multiplying the temperature difference between the first detected temperature Td1e at the time of stop, which is susceptible to the first component temperature of the first electronic component and the estimated component temperature Teale of the component temperature Tea1 at the time of stop ( $Teale - Td1e$ ) by the first estimated gain Ge1.

[0390] However, if the delayed response of the temperature drop of the component temperature Tea1 to be estimated is different from the delayed response of the temperature drop of the second detected temperature Td2, estimating the component temperature Tea1 using the first estimated gain Ge1 as it will produce an error in the estimated value of the component temperature Tea1.

[0391] The dashed line in FIG. 29(c) indicates the estimated value of component temperature Tea1 based on the first estimated gain Ge1 ( $Ge1 \times (Tea1e - Td1e)$ ), and the single-dotted chain line in FIG. 29(c) indicates the assumed value of component temperature Tea1. FIG. 29(d) is a schematic illustration illustrating an error between the estimated value and the assumed value.

[0392] When the delayed response of the temperature drop of the component temperature Tea1 is slower than the delayed response of the temperature drop of the second detected temperature Td2, as illustrated in FIGS. 29(c) and 29(d), the estimated value based on the first estimated gain Ge1 (dashed line) is estimated to be lower than the assumed value (single-dotted chain line) and the error is largest at time t10. If the component temperature Tea1 is underestimated, limitation of the current command value will be insufficient, and thus the estimation errors in FIGS. 29(c) and 29(d) are errors that have occurred on the dangerous side.

[0393] If the delayed response of the temperature drop of the component temperature Tea1 to be estimated is different from the delayed response of the temperature drop of the first detected temperature Td1 as well, estimating the component temperature Tea1 using the first estimated gain Ge1 as it will produce an error in the estimated value.

[0394] Therefore, in the sixth embodiment, the temporal variation of the component temperature Tea1 that occurs when the ECU 30 stops operation (that is, when the current control circuit 40 stops) is actually measured in advance. The initial value setting unit 78 then sets the second estimated gain Ge2 by calibrating the first estimated gain Ge1 based on the temperature data of the temporal variation of the component temperature Tea1 obtained from the measurement results. Hereafter, the temperature data of the temporal variation of component temperature Tea1 obtained by actually measuring in advance the temporal variation of the component temperature Tea1 when ECU 30 stops operation may be referred to as “actual measured temperature data”.

[0395] For example, a function to convert from the first estimated gain Ge1 to the second estimated gain Ge2 may be set in advance based on the actual measured temperature data. The initial value setting unit 78 may set the second estimated gain Ge2 by assigning the first estimated gain Ge1 into a preset function.

[0396] For example, the initial value setting unit 78 may set the second estimated gain  $Ge2 = Ge1 \cdot \sup \cdot x$  using an x power exponent set based on the actual measured temperature data and the power function with the first estimated gain Ge1 at the base. This is because the error in the estimated value based on the first estimated gain Ge1 described above is considered to be caused by the difference in time constant between the time constant of the delayed response of the temperature drop of the component temperature Tea1 and the time constant of the delayed response of the temperature drop of the second detected temperature Td2.

[0397] FIG. 30(a) is a schematic illustration of an example of the second estimated gain Ge. For example, if the delayed response of the temperature drop of the component temperature Tea1 to be estimated is slower than the delayed response of the temperature drop of the second detected

temperature Td2, a power exponent  $x$  of a value smaller than 1 may be set.

[0398] The initial value setting unit **78** calculates the initial value  $Tini = (Ge2 \times (Tea1e - Td1e))$  of the estimated value of the component temperature Tea1 at the time of resumption by multiplying the temperature difference  $(Tea1e - Td1e)$  between the first detected temperature Td1e at the time of stop and the estimated value Teale of the component temperature Tea1 at the time of stop by the second estimated gain Ge2.

[0399] FIG. 30(b) is a schematic illustration of the estimated component temperature based on the second estimated gain Ge2. The estimated value can be brought closer to the assumed value by using the second estimated gain Ge2 to estimate the component temperature Tea1. This avoids insufficient limitation of the current command value caused by an underestimate of the component temperature Tea1.

[0400] The initial value setting unit **78** may convert from the first estimated gain Ge1 to the second estimated gain Ge2 based on a look-up table set in advance based on actual measured temperature data.

[0401] Refer to FIG. 28. The subtractor **79** sets the difference  $(Tini - Tth)$ , which is the result of subtracting the base temperature Tth from the initial value Tini to the first low-pass filter **74** as an initial value of the output of the first low-pass filter **74** when the ECU **30** resumes operation. For example, subtractor **79** may assign the difference  $(Tini - Tth)$  to the delay element of the first low-pass filter **74**.

[0402] As a result, the difference  $(Tini - Tth)$  is outputted from the first low-pass filter **74** when the ECU **30** resumes operation. Adder **76** adds the base temperature Tth to the difference  $(Tini - Tth)$ . As a result, the initial value Tini is outputted from the high-side FET temperature estimating unit **61a1**.

[0403] FIG. 31(a) is a schematic illustration illustrating the first detected temperature Td1 (solid line) and the second detected temperature Td2 (dashed line) when the delayed response of the temperature drop of the component temperature Tea1 to be estimated after ECU **30** stops operation is faster than the delayed response of the temperature drop of the second detected temperature Td2 and an assumed value (single-dotted chain line) of the component temperature Tea1 of high-side FET Q1 to be estimated.

[0404] The dashed line in FIG. 31(b) indicates the estimated value of component temperature Tea1 calculated based on the first estimated gain Ge1 obtained from the first detected temperature Td1 and the second detected temperature Td2 in FIG. 31(a), and the single-dotted chain line in FIG. 31(b) indicates the assumed value of component temperature Tea1. FIG. 31(c) is a schematic illustration illustrating an error between the estimated value and the assumed value.

[0405] If the delayed response of the component temperature Tea1 is faster than the delayed response of the second detected temperature Td2, the estimated value based on the first estimated gain Ge1 (dashed line) is estimated higher than the assumed value (single-dotted chain line) as illustrated in FIGS. 31(b) and 31(c). As a result, the current command value may be unnecessarily limited.

[0406] Therefore, if the delayed response of the component temperature Tea1 is faster than the delayed response of the second detected temperature Td2, the power exponent  $x$  of the power function to convert from the first estimated gain Ge1 to the second estimated gain Ge2 may be set to a value greater than 1.

[0407] FIG. 31(d) is a schematic illustration of an example of the first estimated gain Ge1 and the second estimated gain Ge, respectively, and FIG. 31(e) is a schematic illustration of the estimated value of the component temperature based on the second estimated gain Ge2. The estimated value can be brought closer to the assumed value by using the second estimated gain Ge2 to estimate the component temperature Tea1. This avoids unnecessary limitation of the current command value caused by an overestimation of the component temperature Tea1.

Effect of Sixth Embodiment

[0408] (1) The current control apparatus includes a current control circuit including an electronic component; a temperature detection circuit having a temperature detecting element disposed in the vicinity of the current control circuit; a current detecting unit configured to detect or estimate a current value flowing to the electronic components, a component temperature estimating unit configured to estimate a component temperature, which is the temperature of an electronic component based on the current value detected or estimated by the current detecting unit and the detected temperature detected by the temperature detection circuit, and a current limiting unit configured to limit output current outputted from the current control circuit to a load based on the component temperature.

[0409] The component temperature estimating unit includes an initial value setting unit configured to set the initial value of the estimated value of the component temperature when the current control circuit resumes operation after the current control circuit stops the operation.

[0410] The initial value setting unit acquires the first detected temperature and the second detected temperature detected at two locations at a distance from each other in the vicinity of the current control circuit, stores the estimated temperature, the first detected temperature, and the second detected temperature of the component temperature when the current control circuit is stopped, calculates the ratio of the temperature difference between the first detected temperature and the second detected temperature at the time of stop and the temperature difference between the first detected temperature and the second detected temperature when the current control circuit resumes operation as the first estimated gain, sets the second estimated gain by calibrating the first estimated gain based on temperature data obtained by actually measuring in advance the temporal variation of the component temperature when the current control circuit stops, and sets the initial value based on the temperature difference obtained by multiplying the temperature difference between the first detected temperature and the estimated component temperature at the time of stop by the second estimated gain.

[0411] This improves the estimation accuracy of the electronic components when the current control circuit resumes operation, even if the time constant of the delayed response of the drop in the second detected temperature after the stop of the current control circuit differs from the time constant of the delayed response of the drop in the component temperature of the electronic component to be estimated. As a result, when the current control circuit stops and then resumes operation, the accuracy of component temperature estimation at the time of resumption can be improved.

[0412] (2) The initial value setting unit may convert the first estimated gain to the second estimated gain by a function of the first estimated gain set based on temperature data. The above function may be a power function with a constant set based on temperature data as the power exponent and the first estimated gain as the base or may be a look-up table set based on the temperature data. This allows the second estimated gain to be set appropriately based on the temperature data obtained by actually measuring the temporal variation of the component temperature in advance and the first estimated gain.

[0413] (3) A power exponent smaller than 1 may be set when the delayed response of the component temperature obtained based on the temperature data is slower than the delayed response of the second detected temperature when the current control circuit is stopped, and a power exponent greater than 1 may be set when the delayed response of the component temperature obtained based on the temperature data is faster than the delayed response of the second detected temperature when the current control circuit is stopped. This allows the power function to convert the first estimated gain to the second estimated gain to be set appropriately according to the delayed response characteristics of the temperature drop of the component temperature when the current control circuit is stopped.

[0414] (4) The component temperature estimating unit may obtain a value obtained by passing the detected temperature detected by the temperature detection circuit through the second low-pass

filter 75 as a value corresponding to the detected temperature detected by the temperature detection circuit. In this manner, by applying low-pass filtering to the detected temperature detected by the temperature detection circuit, an estimated value of the ambient temperature in the proximity of individual electronic components can be obtained. For example, by suppressing the effect of heat generated by electronic components in the vicinity of the temperature detection circuit, the ambient temperature in the proximity of other electronic components can be estimated with high accuracy. If the electronic component is thermally connected to a heat sink, the heat sink temperature in the proximity of the electronic component can be obtained.

#### Seventh Embodiment

[0415] FIGS. 32(a) to 32(e) illustrate an example of the change in the assumed values of the component temperature of the choke coil La, power cutoff FETs QC2, QD2, QC1, and QD1 when the ECU 30 operates in the dual-system drive mode in which both the first system coil and the second system coil of motor 20 are driven, and the distribution ratio of the drive current outputted from the first current control circuit 40A and the second current control circuit 40B to the motor 20 is substantially equal.

[0416] In dual-system drive mode, both battery currents Ibat1 and Ibat2 flowing from battery 13 to the first system coil and the second system coil, respectively, flow in the choke coil La. Therefore, the choke coil La easily becomes hot, and the component temperature of the choke coil La is high at time t1, as illustrated in FIG. 32(a).

[0417] In contrast, the component temperatures of power cutoff FETs QC1 and QC2 through which only battery current Ibat1 (FIGS. 32(d) and 32(b)) flows and the heat generation rate of power cutoff FETs QD1 and QD2 through which only battery current Ibat2 (FIGS. 32(e) and 32(c)) flow are less than the heat generation rate of the choke coil La.

[0418] Furthermore, if the distribution ratios of the drive currents outputted from the first current control circuit 40A and the second current control circuit 40B to the motor 20 are substantially equal, the magnitudes of the battery currents Ibat1 and Ibat2 are substantially equal. Therefore, the difference in component temperatures near time t1 between the power cutoff FET QC1 (FIG. 32(d)), through which the battery current Ibat1 flows, and the power cutoff FET QD1 (FIG. 32(e)), through which the battery current Ibat2 flows, is small.

[0419] On the other hand, the difference in component temperatures between the power cutoff FET QC2 (FIG. 32(b)), through which the battery current Ibat1 flows, and the power cutoff FET QD2 (FIG. 32(c)), through which the battery current Ibat2 flows, is expected to be small. However, comparing FIGS. 32(b) and 32(c), the component temperature of power cutoff FET QD2 is significantly higher than the component temperature of power cutoff FET QC2 at around time t1.

[0420] This is thought to be because the power cutoff FET QD2 is placed closer to the choke coil La than the power cutoff FETs QC1, QC2, and QD1, so the amount of heat propagated from the hot choke coil La affects the component temperature of power cutoff FET QD2.

[0421] FIG. 33(a) is a schematic illustration of the first example of a heat dissipation path from the choke coil La. In the example in FIG. 33(a), the power cutoff FET QD2, temperature sensors 45B1 and 45B2, and the choke coil La are mounted on the front surface ff of the circuit board 36 and are in contact with the heat sink 37 via the thermal interface materials 38a to 38c, respectively.

[0422] In this case, the heat dissipation path Pth5, where the heat from the choke coil La is dissipated through the thermal interface material 38c to the heat sink 37, and a heat dissipation path Pth6, where the heat from the choke coil La is dissipated through the circuit board 36, the power cutoff FET QD2 and the thermal interface material 38a to the heat sink 37 are assumed. Therefore, the heat propagating from the choke coil La through the heat dissipation path Pth6 is expected to cause a rise in the component temperature of the power cutoff FET QD2.

[0423] FIG. 33(b) is a schematic illustration of the second example of the heat dissipation path from the choke coil La. In the example in FIG. 33(b), the power cutoff FET QD2 and the temperature sensors 45B1 and 45B2 are mounted on the front surface ff of the circuit board 36 and

are in contact with the heat sink **37** via the thermal interface materials **38a** and **38b**, respectively. The choke coil **La**, on the other hand, is electrically connected to the circuit board **36** with connection wiring **W** and is in contact with the heat sink **37** via the thermal interface material **38c**. [0424] In this case, the heat dissipation path **Pth5**, where the heat from choke coil **La** is dissipated through the thermal interface material **38c** to the heat sink **37**, and a heat dissipation path **Pth7**, where heat from the choke coil **La** is dissipated through the connection wiring **W**, the circuit board **36**, the power cutoff FET **QD2**, and the thermal interface material **38a** to the heat sink **37**, are assumed. Therefore, the heat propagating from the choke coil **La** through the heat dissipation path **Pth7** is expected to cause a rise in the component temperature of the power cutoff FET **QD2**. [0425] FIG. **33(c)** is a schematic illustration of a third example of a heat dissipation path from the choke coil **La**. In the example in FIG. **33(c)**, the power cutoff FET **QD2** and the temperature sensors **45B1** and **45B2** are mounted on the front surface **ff** of the circuit board **36** and are in contact with the heat sink **37** via the thermal interface materials **38a** and **38b**, respectively. The choke coil **La**, on the other hand, is mounted on the back surface **fr** of the circuit board **36** and is thermally connected to the heat sink **37** via a via through the circuit board **36** and a thermal interface material **38c**.

[0426] In this case, a heat dissipation path **Pth8**, where the heat from the choke coil **La** is dissipated through the via and the thermal interface material **38c** to the heat sink **37**, and a heat dissipation path **Pth9**, where the heat from the choke coil **La** is dissipated through the circuit board **36**, the power cutoff FET **QD2** and the thermal interface material **38a** to the heat sink **37** are assumed. Therefore, heat propagating from the choke coil **La** through the heat dissipation path **Pth9** is expected to cause a rise in the component temperature of the power cutoff FET **QD2**.

[0427] Thus, if the power cutoff FET **QD2** is disposed in proximity to the choke coil **La**, which is susceptible to high temperature, the power cutoff FET **QD2** may be affected by the high temperature of the choke coil **La**. As a result, the actual component temperature of the power cutoff FET **QD2** may be higher than the value estimated by the power cutoff FET temperature estimating units **61e2**, which may reduce the accuracy of the component temperature estimation. In the following description, electronic components that are susceptible to high temperatures are sometimes referred to as the “first electronic components” and electronic components that are easily affected by the component temperature of the first electronic component are sometimes referred to as the “second electronic components. The choke coil **La** is an example of the “first electronic component” and the power cutoff FET **QD2** is an example of the “second electronic component.

[0428] For convenience of explanation, in the following description, for the component temperatures of the high-side FETs **Q1**, **Q3** and **Q5**, the low-side FETs **Q2**, **Q4** and **Q6**, and the shunt resistors of the current detection circuits **39A2**, **39B2** and **39C2** of the second power conversion circuit **42B**, the phase cutoff FETs **QB1**, **QB2** and **QB3**, the power cutoff FETs **QD1** and **QD2**, and electrolytic capacitors **CB1** and **CB2**, which constitute the current control circuit that controls current driving the second system coil, the same signs as the component temperatures of the electronic components constituting the current control circuit that controls the current driving the first system coil (that is, **Tea1** to **Tea3**, **Teb1** to **Teb3**, **Tec1** to **Tec3**, **Ted1** to **Ted3**, **Tee1** and **Tee2**, and **Tef1** and **Tef2**) are used.

[0429] In the seventh embodiment, in addition to the power loss **W** of the second electronic component and the detection signal **SdB** of the ECU **30** temperature outputted by the temperature detection circuit **45B**, the second component temperature of the second electronic component is estimated based on the first component temperature of the first electronic component. For example, the component temperature **Tee2** of the power cutoff FET **QD2** is estimated based on the power loss **W** of the power cutoff FET **QD2**, the detection signal **SdB**, and the component temperature **Teg** of the choke coil **La**.

[0430] This makes it possible to correct the estimated temperature of the second component based

on the estimated temperature of the first component in a configuration where the second component temperature of the second electronic component is easily affected by the first component temperature of the first electronic component, thereby improving the estimation accuracy of the second component temperature.

[0431] FIG. 34(a) is a block diagram of a first example of the functional configuration of the power cutoff FET temperature estimating unit **61e2** in the first reduction coefficient setting unit **60** of the control calculating apparatus **31b** in the seventh embodiment. The power off FET temperature estimating unit **61e2** receives the detected values  $I_{2ad}$ ,  $I_{2bd}$ , and  $I_{2cd}$  of the phase A current, the phase B current, and the phase C current detected by the current detection circuits **39A2**, **39B2**, and **39C2**, respectively, the detection signal  $S_{dB}$  of the temperature of the ECU **30** detected by the temperature detection circuit **45B**, and the estimated value of the component temperature  $T_{eg}$  of the choke coil  $L_a$  estimated by the coil temperature estimating unit **61g**.

[0432] The power loss calculating unit **72** estimates the on-resistance  $R_f$  of the power cutoff FET **QD2** based on the previous value of the component temperature  $T_{ee2}$  of the power cutoff FET **QD2** calculated in the previous control cycle. The battery current  $I_{bat2}$  flowing from the battery **13** to the second system coil is then calculated based on the on-resistance  $R_f$  and the detected values  $I_{2ad}$ ,  $I_{2bd}$ , and  $I_{2cd}$  of the phase A current, the phase B current, and the phase C current. Then, the power loss  $W$  of the power cutoff FET **QD2** is calculated based on the following calculation formula.

$$W = R_f \times I_{bat2}.sup.2$$

[0433] The gain multiplying unit **73** calculates a product of the power loss  $W$  and a predetermined gain  $G_1$  ( $G_1 \times W$ ) and outputs the result to the first low-pass filter **74**.

[0434] The first low-pass filter **74** outputs a signal obtained by applying a low-pass filtering to the product ( $G_1 \times W$ ) to the adder **76**. The second low-pass filter **75** outputs a signal obtained by applying the low-pass filtering to a detection signal  $S_{dB}$  of the temperature of the ECU **30** outputted by the temperature detection circuit **45B** to the adder **76**.

[0435] The gain multiplying unit **81** calculates the product ( $G_2 \times T_{eg}$ ) of a predetermined gain  $G_2$ , which is different from the above gain  $G_1$ , and the component temperature  $T_{eg}$  of the choke coil  $L_a$ , and outputs it to the third low-pass filter **82**. The third low-pass filter **82** outputs a signal obtained by applying a low-pass filtering to the product ( $G_2 \times T_{eg}$ ) to the adder **76**.

[0436] The adder **76** calculates the sum of the output of the first low-pass filter **74**, the output of the second low-pass filter **75**, and the output of the third low-pass filter **82** as the component temperature  $T_{ee2}$  of the power cutoff FET **QD2**.

[0437] In this specification, the choke coil  $L_a$  is exemplified as the “first electronic component” and the power cutoff FET **QD2** is exemplified as the “second electronic component,” but this embodiment is not limited to these specific examples. This embodiment is widely applicable to a combination of a plurality of electronic components in a current control circuit that are susceptible to heat generation and other components disposed in close proximity to this electronic component.

[0438] FIG. 34(b) is a block diagram of a second example of the functional configuration of the power cutoff FET temperature estimating unit **61e2** in the first reduction coefficient setting unit **60** of the control calculating apparatus **31b** in the seventh embodiment.

[0439] The operating state (operating mode) of a current control circuit includes an operating state in which the electronic components in the current control circuit are susceptible to heat generation (that is, easily become hot) and an operating state in which the heat generation is moderate. In the following description, the operating state in which electronic components generate heat relatively easily (that is, easily become hot) is denoted as “first state,” while the operating state in which heat generation is relatively moderate is denoted as “second state”.

[0440] For example, the first state may be a state in which the time average of the heat generation rate of the electronic component or the time average of the current flowing to the electronic



component is equal to or above the threshold value, and the second state may be a state in which the time average of the heat generation rate of the electronic component or the time average of the current flowing to the electronic component is below the threshold value. For example, the first state may be a state in which the battery current  $I_{bat} = (I_{bat1} + I_{bat2})$  flowing from battery **13** or its time average is equal to or above the threshold value, and the second state may be a state in which the battery current  $I_{bat}$  or its time average is below the threshold value.

[0441] A switch **83** determines whether the current control circuit is in the first state or the second state of operation.

[0442] For example, when the battery current  $I_{bat}$  or its time average is equal to or above the threshold value, the switch **83** may determine that the operating state of the current control circuit is in the first state and when the battery current  $I_{bat}$  or its time average is below the threshold value, the switch **83** may determine that the operating state of the current control circuit is in the second state.

[0443] For example, when the present invention is applied to a current control apparatus that supplies drive current to a motor **20**, it is determined to be in the first state when the rotation speed of the motor rotating shaft of the motor **20** is equal to or above a threshold value, and to be in the second state when the rotation speed is below the threshold value. The state in which the current of any one particular phase of a multiphase motor continues to be higher than the currents of the other phases and the rotation of the motor rotating shaft has stopped may be determined to be the second state, and the state in which the motor rotating shaft is rotating may be determined to be the first state.

[0444] The switch **83** outputs the output of the third low-pass filter **82** to the adder **76** when the operating state of the current control circuit is in the first state. The adder **76** calculates the sum of the output of the first low-pass filter **74**, the output of the second low-pass filter **75**, and the output of the third low-pass filter **82** as the component temperature  $T_{ee2}$  of the power cutoff FET QD2.

[0445] On the other hand, when the operating state of the current control circuit is the second state, switch **83** outputs the value "0" to adder **76**. The adder **76** calculates the sum of the output of the first low-pass filter **74** and the output of the second low-pass filter **75** as the component temperature  $T_{ee2}$  of the power cutoff FET QD2. In other words, the component temperature  $T_{ee2}$  of the power cutoff FET Q2 is estimated without being based on the component temperature  $T_{eg}$  of the choke coil  $L_a$ .

#### Effect of Seventh Embodiment

[0446] (1) The current control apparatus includes: a current control circuit including a plurality of electronic components; a temperature detection circuit having a temperature detecting element disposed in the vicinity of the current control circuit; a current detecting unit configured to detect or estimate current values flowing to each of the plurality of electronic components; a component temperature estimating unit configured to estimate a component temperature, which is the temperature of an electronic component, for each of the plurality of electronic components based on the current value detected or estimated by the current detecting unit and the detected temperature detected by the temperature detection circuit; a reduction coefficient setting unit configured to set a plurality of different reduction coefficients for a plurality of different component temperatures included in the component temperature estimated for each of the plurality of electronic components; a selecting unit configured to select any one of the plurality of reduction coefficients; and a current limiting unit configured to limit output current outputted from the current control circuit to a load based on the selected reduction coefficient.

[0447] The plurality of electronic components includes at least the first electronic component and the second electronic component, and the component temperature estimating unit estimates the first component temperature, which is the component temperature of the first electronic component, based on the current value detected or estimated by the current detecting unit and the detected temperature detected by the temperature detection circuit, and estimates the second component

temperature, which is the component temperature of the second electronic component, based on the current value detected or estimated by the current detecting unit, the detected temperature detected by the temperature detection circuit, and the first component temperature. For example, the first electronic component and the second electronic component may be components disposed in close proximity to each other.

[0448] This makes it possible to correct the estimated temperature of the second component based on the estimated temperature of the first component in a configuration where the second component temperature of the second electronic component is easily affected by the first component temperature of the first electronic component, thereby improving the estimation accuracy of the second component temperature.

[0449] (2) The component temperature estimating unit may estimate a first power loss, which is a power loss generated in the first electronic component, and a second power loss, which is a power loss generated in the second electronic component, and may estimate the first component temperature based on the sum of the value obtained by low-pass filtering the product of the first power loss and the predetermined gain and the value obtained by low-pass filtering the detected temperature detected by the temperature detection circuit, and estimate the second component temperature based on the sum of the value obtained by low-pass filtering the product of the second power loss and the predetermined gain and the value obtained by low-pass filtering the detected temperature detected by the temperature detection circuit, and the value obtained by low-pass filtering the product of the first component temperature and the predetermined gain.

[0450] The component temperature can be estimated with high accuracy by estimating the component temperature based on the value obtained by low-pass filtering of the power loss. An estimated value of the ambient temperature in the proximity of individual electronic components can be obtained by applying a low-pass filtering to the detected temperature detected by the temperature detection circuit. If the electronic component is thermally connected to a heat sink, the heat sink temperature in the proximity of the electronic component can be obtained. The effect of the propagation of heat generated by the first electronic component on the second component temperature can be estimated with high accuracy by estimating the component temperature based on the value obtained by low-pass filtering the first component temperature.

[0451] (3) The component temperature estimating unit may estimate the second component temperature based on the first component temperature when the current control apparatus is in the first state and may estimate the second component temperature without being based on the first component temperature when the current control apparatus is in the second state.

[0452] This allows switching whether or not the first component temperature is reflected in the estimation of the second component temperature, depending on the operating state of the current control apparatus.

[0453] (4) For example, the first state may be a state in which the heat generation rate of the first electronic component is equal to or above the threshold value, and the second state may be a state in which the heat generation rate of the first electronic component is below the threshold value. For example, the first state may be a state in which the supply current flowing from the DC power source supplying DC power to the current control circuit is equal to or above the threshold value, and the second state may be a state in which the supply current is below the threshold value.

[0454] This allows switching whether or not the first component temperature is reflected in the estimation of the second component temperature, depending on whether or not the first electronic component is susceptible to high temperature.

#### Modifications

[0455] (1) FIG. 35 is a configuration diagram illustrating an overview of the first modification of ECU 30. The electric power steering apparatus may separately include, as the battery 13, a first battery that supplies power to the first power conversion circuit 42A via the first power line PWa and a second battery that supplies power to the second power conversion circuit 42B via the second

power line PWb.

[0456] The positive-side power line Lpa of the first power line PWa is connected to the control calculating apparatus **31a** via a noise filter circuit formed by the choke coil La and ceramic capacitors Ca1 and Ca2, and to the first power cutoff circuit **44A**.

[0457] One end of the choke coil La is connected to the positive-side power line Lpa and one end of the ceramic capacitor Ca1, the other end of the choke coil La is connected to one end of the ceramic capacitor Ca2 and the control calculating apparatus **31a**, and the other ends of the ceramic capacitors Ca1 and Ca2 are grounded. On the other hand, a negative-side line of the first power line PWa is connected to a ground line of the ECU **30**.

[0458] The positive-side power line Lpb of the second power line PWb is connected to the control calculating apparatus **31b** via a noise filter circuit formed by the choke coil Lb and ceramic capacitors Cb1 and Cb2, and to the second power cutoff circuit **44B**.

[0459] One end of the choke coil Lb is connected to the positive-side power line Lpb and one end of the ceramic capacitor Cb1 and the other end of the choke coil Lb is connected to one end of the ceramic capacitor Cb2 and the control calculating apparatus **31b**, and the other ends of the ceramic capacitors Cb1 and Cb2 are grounded. On the other hand, a negative-side line of the second power line PWb is connected to a ground line of the ECU **30**.

[0460] In the first modification of the control calculating apparatus **31b**, the coil reduction coefficient Kg is set by estimating the coil temperature Teg of the choke coil Lb instead of the choke coil La.

[0461] The third reduction coefficient setting unit **71** also sets the battery reduction coefficient K4 based on the battery voltage Vbat2, which is a voltage between output terminals of the second battery.

[0462] When the initial value setting unit **78** is provided as in the sixth embodiment, the temperature detectors **46A** and **46B** may be provided in the control calculating apparatuses **31a** and **31b**. Alternatively, temperature detectors other than temperature detection circuits **45A** and **45B** may be provided elsewhere in the ECU **30**. The same is true for the second modification of ECU **30** in FIG. **36**.

[0463] (2) FIG. **36** is a configuration diagram illustrating an overview of the second modification of ECU **30**. The second modification of ECU **30** uses a single inverter to drive motor **20**. Therefore, of the first motor current cutoff circuit **33A** and the second motor current cutoff circuit **33B**, the first gate drive circuit **41A** and the second gate drive circuit **41B**, the first power conversion circuit **42A** and the second power conversion circuit **42B**, the first power cutoff circuit **44A** and the second power cutoff circuit **44B**, and the temperature detection circuits **45A** and **45B** included in the configuration illustrated in FIG. **2**, only the first motor current cutoff circuit **33A**, the first gate drive circuit **41A**, the first power conversion circuit **42A**, the first power cutoff circuit **44A**, and the temperature detection circuit **45A** are provided.

[0464] (3) The above description describes an example of applying the current control apparatus of the present invention to a column assist electric power steering apparatuses of a so-called upstream assist system. However, the current control apparatus of the present invention may be applied to a so-called downstream assist electric power steering apparatus. The following is a configuration example of the application of the electric power steering apparatus of the present invention to the single-pinion assist, rack assist, and dual-pinion assist current control apparatus of the present invention as examples of the downstream assist electric power steering apparatus.

[0465] In the case of the downstream assist system, the motor **20**, the rotational angle sensor **23a**, and the ECU **30** may be integrated into an MCU (Motor Control Unit) with an integrated structure as illustrated by the dashed lines in FIGS. **37** to **39**, instead of being separate units for waterproofing.

[0466] FIG. **37** illustrates an example of a configuration in which the current control apparatus of the present invention is applied to an electric power steering apparatus of a single-pinion assist

system. The steering wheel **1** is connected to the universal joint **4a** on one of intermediate shafts via the steering shaft **2**. The input-side shaft **4c** of the torsion bar (not illustrated) is connected to the other universal joint **4b**.

[0467] The pinion rack mechanism **5** has a pinion gear (pinion) **5a**, a rack bar (rack) **5b**, and a pinion shaft **5c**. The input-side shaft **4c** and the pinion rack mechanism **5** are connected by a torsion bar (not illustrated) that twists due to the rotational angle shift between the input-side shaft **4c** and the pinion rack mechanism **5**. The torque sensor **10** electromagnetically measures the torsion angle of the torsion bar as steering torque  $T_h$  of the steering wheel **1**.

[0468] Motor **20**, which assists the steering force of steering wheel **1**, is connected to pinion shaft **5c** via reduction gear **3**, and rotational angle sensor **23a** calculates the rotational angle information of the motor rotating shaft of motor **20**.

[0469] (4) FIG. **38** illustrates a configuration example of applying the current control apparatus of the present invention to an electric power steering apparatus of a rack-assist system. A helical groove (not illustrated) is formed on the outer surface of a rack bar **5b**, and a similar lead helical groove (not illustrated) is formed on the inner surface of nut **91**. A ball screw is formed by being disposed a plurality of rolling elements in the rolling paths formed by these helical grooves.

[0470] A belt **94** is wound around a drive pulley **92** connected to the rotating shaft **20a** of the motor **20** that assists the steering force of the steering wheel **1** and a driven pulley **93** connected to a nut **91**, thereby converting the rotational motion of the rotating shaft **20a** into a linear motion of the rack bar **5b**. The rotational angle sensor **23a** calculates the rotational angle information of the motor rotating shaft of the motor **20**.

[0471] (5) FIG. **39** illustrates a configuration example in which the current control apparatus of the present invention is applied to an electric power steering apparatus of a dual-pinion assist system. In addition to the pinion shaft **5c** and pinion gear **5a**, the dual-pinion assist electric power steering apparatus has a second pinion shaft **95** and a second pinion gear **96**, and the rack bar **5b** has first rack teeth (not illustrated) that mesh with the pinion gear **5a** and the second rack teeth (not illustrated) that mesh with the second pinion gear **96**.

[0472] The motor **20**, which assists the steering force of steering wheel **1**, is connected to the second pinion shaft **95** via reduction gear **3** and the rotational angle sensor **23a** calculates the rotational angle information of the motor rotating shaft of motor **20**.

[0473] (6) Each of the first low-pass filter **74** and the second low-pass filter **75** may be replaced by a second-order delay filter.

#### REFERENCE SIGNS LIST

[0474] **1** . . . Steering wheel [0475] **2** . . . Steering shaft [0476] **3** . . . Reduction gear [0477] **4a, 4b** . . . Universal joint [0478] **4c** . . . Input-side shaft [0479] **5** . . . Pinion rack mechanism [0480] **5a** . . . Pinion gear (pinion) [0481] **5b** . . . Rack bar (rack) [0482] **5c** . . . Pinion shaft [0483] **6a, 6b** . . . Tie rod [0484] **7a, 7b** . . . Hub unit [0485] **8L, 8R** . . . Steered wheel [0486] **10** . . . Torque sensor [0487] **11** . . . Ignition switch [0488] **12** . . . Vehicle speed sensor [0489] **13** . . . Battery [0490] **14** . . . Steering angle sensor [0491] **20** . . . Motor [0492] **20a** . . . Rotating shaft [0493] **23** . . . Motor rotational angle detection circuit [0494] **23a** . . . Rotational angle sensor [0495] **30** . . . Electronic control unit (ECU) [0496] **31a, 31b** . . . Control calculating apparatus [0497] **33A** . . . First motor current cutoff circuit [0498] **33B** . . . Second motor current cutoff circuit [0499] **34A, 34B** . . . Voltage detection circuit [0500] **35** . . . Communication line [0501] **36** . . . Circuit board [0502] **37** . . . Heat-dissipating member (heat sink) [0503] **38a to 38c** . . . Thermal interface material [0504] **39A1, 39A2, 39B1, 39B2, 39C1, 39C2** . . . Current detection circuit [0505] **41A** . . . First gate drive circuit [0506] **41B** . . . Second gate drive circuit [0507] **42A** . . . First power conversion circuit [0508] **42B** . . . Second power conversion circuit [0509] **44A** . . . First power cutoff circuit [0510] **44B** . . . Second power cutoff circuit [0511] **45A, 45B** . . . Temperature detection circuit [0512] **46A, 46B** . . . Temperature detector [0513] **50** . . . Current command value calculating unit [0514] **51** . . . Current limiting unit [0515] **52, 53** . . . Subtractor [0516] **54** . . . Proportional integral (PI)

control unit [0517] **55** . . . 2-phase/3-phase converting unit [0518] **56** . . . 3-phase/2-phase converting unit [0519] **57** . . . Angular speed converting unit [0520] **60** . . . First reduction coefficient setting unit [0521] **61a1, 61a2, 61a3** . . . High-side FET temperature estimating unit **61b1, 61b2, 61b3** . . . Low-side FET temperature [0522] estimating unit [0523] **61c1, 61c2, 61c3** . . . Shunt resistance temperature estimating unit [0524] **61d1, 61d2, 61d3** . . . Phase cutoff FET temperature estimating unit [0525] **61e1, 61e2** . . . Power cutoff FET temperature estimating unit [0526] **61f1, 61f2** . . . Capacitor temperature estimating unit [0527] **61g** . . . Coil temperature estimating unit [0528] **62a, 62b, 62c, 62d, 62e, 62f, 64** . . . Selector [0529] **63a, 63a1, 63a2, 63a3** . . . High-side FET temperature estimating unit [0530] **63b, 63b1, 63b2, 63b3** . . . Low-side FET reduction coefficient setting unit [0531] **63c, 63c1, 63c2, 63c3** . . . Shunt resistance reduction coefficient setting unit [0532] **63d, 63d1, 63d2, 63d3** . . . Phase cutoff FET reduction coefficient setting unit [0533] **63e, 63e1, 63e2** . . . Power cutoff FET reduction coefficient setting unit [0534] **63f, 63f1, 63f2** . . . Capacitor reduction coefficient setting unit [0535] **63g** . . . Coil reduction coefficient setting unit [0536] **70** . . . Second reduction coefficient setting unit [0537] **71** . . . Third reduction coefficient setting unit [0538] **72** . . . Power loss calculating unit [0539] **73, 73a, 73b** . . . Gain multiplying unit [0540] **74, 74a, 74b, 74c, 74d** . . . First low-pass filter [0541] **75** . . . Second low-pass filter [0542] **76** . . . Adder [0543] **78** . . . Initial value setting unit [0544] **79** . . . Subtractor [0545] **81** . . . Gain multiplying unit [0546] **82** . . . Third low-pass filter [0547] **83** . . . Switch [0548] **91** . . . Nut [0549] **92** . . . Drive pulley [0550] **93** . . . Driven pulley [0551] **94** . . . Belt [0552] **95** . . . Second pinion shaft [0553] **96** . . . Second pinion gear [0554] **Ca1, Ca2, Cb1, Cb2** . . . Ceramic capacitor [0555] **CA1, CA2, CB1, CB2** . . . Electrolytic capacitor [0556] **CNT** . . . Connector [0557] **Ct1, Ct2** . . . Capacitor [0558] **Q1, Q3, Q5** . . . High-side FET [0559] **Q2, Q4, Q6** . . . Low-side FET [0560] **QA1, QA2, QA3, QB1, QB2, QB3** . . . Phase cutoff FET [0561] **QC1, QC2, QD1, QD2** . . . Power cutoff FET [0562] **La, Lb** . . . Choke coil [0563] **Lpa, Lpb** . . . Positive-side power line [0564] **PWa** . . . First power line [0565] **PWb** . . . Second power line [0566] **SWAa, SWAb, SWAc, SWBa, SWBb, SWBc** . . . Switching arm

## Claims

**1.** A current control apparatus comprising: a current control circuit including a plurality of electronic components; a temperature detection circuit having a temperature detecting element disposed in the vicinity of the current control circuit; a current detecting unit configured to detect or estimate a current value flowing to each of the plurality of electronic components; a component temperature estimating unit configured to estimate a component temperature, which is the temperature of the electronic component, for each of the plurality of electronic components based on the current value detected or estimated by the current detecting unit and the detected temperature detected by the temperature detection circuit; a reduction coefficient setting unit configured to set a plurality of different reduction coefficients for a plurality of different component temperatures included in the component temperature estimated for each of the plurality of electronic components; a selecting unit configured to select any one of the plurality of reduction coefficients; and a current limiting unit configured to limit output current outputted from the current control circuit to a load based on the selected reduction coefficient, wherein the plurality of electronic components include at least a first electronic component and a second electronic component, the component temperature estimating unit estimates a first component temperature, which is the component temperature of the first electronic component based on the current value detected or estimated by the current detecting unit and the detected temperature detected by the temperature detection circuit, and estimates a second component temperature, which is the component temperature of the second electronic component based on the current value detected or estimated by the current detecting unit, the detected temperature detected by the temperature detection circuit, and the first component temperature.

2. The current control apparatus according to claim 1, characterized in that the component temperature estimating unit estimates a first power loss, which is a power loss generated in the first electronic component, and a second power loss, which is a power loss generated in the second electronic component, estimates the first component temperature based on a sum of the value obtained by low-pass filtering a product of the first power loss and a predetermined gain and the value obtained by low-pass filtering the detected temperature detected by the temperature detection circuit, and estimates the second component temperature based on a sum of a value obtained by low-pass filtering a product of the second power loss and the predetermined gain, a value obtained by low-pass filtering the detected temperature detected by the temperature detection circuit, and a value obtained by low-pass filtering the product of the first component temperature and the predetermined gain.
3. A current control apparatus according to claim 1 or 2, characterized in that the first electronic component and the second electronic component are disposed in close proximity.
4. The current control apparatus according to any one of claims 1 to 3, characterized in that the component temperature estimating unit estimates the second component temperature based on the first component temperature when the current control apparatus is in a first state and estimates the second component temperature not based on the first component temperature when the current control apparatus is in a second state.
5. The current control apparatus according to claim 4, characterized in that the first state is a state in which a heat generation rate of the first electronic component is equal to or above a threshold value and the second state is a state in which the heat generation rate of the first electronic component is below the threshold value.
6. The current control apparatus according to claim 4, characterized in that the first state is a state in which a power supply current flowing from a DC power source configured to supply DC power to the current control circuit is equal to or above a threshold value, and the second state is a state in which the power supply current is below the threshold value.
7. The current control apparatus according to any one of claims 1 to 6, characterized in that the plurality of electronic components include a plurality of different types of electronic components, and the reduction coefficient setting unit sets one of the reduction coefficients for each type of the electronic components.
8. The current control apparatus according to any one of claims 1 to 6, characterized in that the plurality of electronic components include a plurality of different types of electronic components, and at least one type of electronic component of the plurality of different types of electronic components includes a plurality of electronic components disposed at different locations in the current control circuit, the reduction coefficient setting unit sets a plurality of different reduction coefficients for a plurality of electronic components disposed at different locations in the current control circuit included in at least one type of electronic component, respectively.
9. The current control apparatus according to any one of claims 1 to 8, characterized in that the current control apparatus includes a pair of the current control circuits, the component temperature estimating unit sets a predetermined gain according to a distribution ratio between output currents of the pair of current control circuits, estimates a power loss generated in the electronic component for each of the plurality of electronic components, and estimates the component temperature for each of the plurality of electronic components based on a sum of a value according to a product of the power loss and the predetermined gain and a value according to the detected temperature detected by the temperature detection circuit.
10. The current control apparatus according to any one of claims 1 to 9, characterized in that the component temperature estimating unit estimates a power loss generated in the electronic component for each of the plurality of electronic components, and estimates the second component temperature based on a sum obtained by adding a first value obtained by filtering the power loss through a plurality of first low-pass filters connected in parallel with each other and a second value

obtained by filtering the detected temperature detected by the temperature detection circuit through a second low-pass filter, and the first component temperature.

**11.** The current control apparatus according to any one of claims 1 to 9, characterized in that the component temperature estimating unit estimates a power loss generated in the electronic component for each of the plurality of electronic components, and estimates the second component temperature based on a sum obtained by adding a first value obtained by filtering the power loss through a plurality of first low-pass filters connected in series with each other and a second value obtained by filtering the detected temperature detected by the temperature detection circuit through a second low-pass filter, and the first component temperature.

**12.** The current control apparatus according to any one of claims 1 to 11, characterized in that the component temperature estimating unit comprises an initial value setting unit configured to set an initial value of an estimated value of the component temperature when the current control circuit resumes operation after the current control circuit is stopped, and the initial value setting unit acquires a first detected temperature and a second detected temperature detected at two locations at a distance from each other in the vicinity of the current control circuit, stores an estimated temperature of the component temperature and the first detected temperature and the second detected temperature when the current control circuit is stopped, calculates a ratio of a temperature difference between the first detected temperature and the second detected temperature at the time of the stop and the temperature difference between the first detected temperature and the second detected temperature when the current control circuit resumes operation as a first estimated gain, sets a second estimated gain by calibrating the first estimated gain based on temperature data obtained by actually measuring in advance a temporal variation of the component temperature when the current control circuit is stopped, and sets the initial value based on a temperature difference obtained by multiplying a temperature difference between the first detected temperature and an estimated temperature of the component temperature at the time of stop by the second estimated gain.

**13.** A motor control apparatus characterized in that current supplied to an electric motor as a load is controlled by the current control apparatus according to any one of claims 1 to 12.

**14.** An electric power steering apparatus comprising: the motor control apparatus according to claim 13, and an electric motor controlled by the motor control apparatus, characterized in that a steering assist force is applied to a steering system of a vehicle by the electric motor.

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