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Multi-active area semiconductor structure and method for manufacturing same

Abstract

A multi-active area semiconductor structure and a method for manufacturing same. The multi-active area semiconductor structure includes: a (2k−1).sup.th common confining layer arranged between a k.sup.th active layer and a k.sup.th tunnel junction and in contact with the k.sup.th tunnel junction; and a 2k.sup.th common confining layer arranged between the k.sup.th active layer and a (k+1).sup.th tunnel junction and in contact with the k.sup.th tunnel junction, where a forbidden band width of a k.sup.th quantum well layer is less than both a forbidden band width of a k.sup.th first-semiconductor layer and a forbidden band width of a k.sup.th second-semiconductor layer; a total thickness of the (2k−1).sup.th common confining layer and the 2k.sup.th common confining layer is greater than a critical optical field coupling thickness and less than or equal to twice the critical optical field coupling thickness; and a thickness of the k.sup.th quantum well layer is less than or equal to 1/10 of a thickness of the (2k−1).sup.th common confining layer, and the thickness of the k.sup.th quantum well layer is less than or equal to 1/10 of a thickness of the 2k.sup.th common confining layer. The multi-active area semiconductor structure has effectively improved light-emission efficiency and reduced optical field crosstalk.

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Background/Summary

(1) This application claims priority to Chinese patent application No. 202210000451.X, entitled "MULTI-ACTIVE AREA SEMICONDUCTOR STRUCTURE AND METHOD FOR MANUFACTURING SAME", filed with the China National Intellectual Property Administration on Jan. 4, 2022, the disclosure of which is hereby incorporated by reference in its entirety.

TECHNICAL FIELD

(2) The present application relates to the field of semiconductor technologies, and specifically to a multi-active area semiconductor structure and a method for manufacturing same.

BACKGROUND

(3) A light-emitting semiconductor device is a device that produces excited emission by using a certain semiconductor material as a working material. The working principle of the device is implementing particle number inversion of non-equilibrium carriers between energy bands (conduction bands and valence bands) of a semiconductor material or between an energy band of a semiconductor material and an energy level of an impurity (an acceptor or a donor) through certain excitation. Excited emission is produced when a large number of electrons and holes in a particle number inversion state recombine. Light-emitting semiconductor devices are widely used because of small sizes and high electro-optical conversion efficiency.

(4) At present, existing technologies cannot simultaneously improve light-emission efficiency effectively and reduce optical field crosstalk.

SUMMARY OF THE INVENTION

(5) Therefore, a technical problem to be resolved by the present application is to overcome the problem that existing technologies cannot simultaneously improve light-emission efficiency effectively and reduce optical field crosstalk, and a multi-active area semiconductor structure and a method for manufacturing same are provided.

(6) The present application provides a multi-active area semiconductor structure, including: a semiconductor substrate layer; a first active layer to an N.sup.th active layer arranged on the semiconductor substrate layer, where N is an integer greater than or equal to 2; a k.sup.th tunnel junction arranged between a k.sup.th active layer and a (k+1).sup.th active layer, where k is greater than or equal to 1 and less than or equal to N−1; and the k.sup.th tunnel junction includes a k.sup.th first-semiconductor layer and a k.sup.th second-semiconductor layer that are of opposite conductivity types and a k.sup.th quantum well layer, the k.sup.th second-semiconductor layer is arranged on a side of the k.sup.th first-semiconductor layer away from the k.sup.th active layer, the k.sup.th quantum well layer is arranged between the k.sup.th second-semiconductor layer and the k.sup.th first-semiconductor layer, and a forbidden band width of the k.sup.th quantum well layer is less than both a forbidden band width of the k.sup.th first-semiconductor layer and a forbidden band width of the k.sup.th second-semiconductor layer; a (2k−1).sup.th common confining layer arranged between the k.sup.th active layer and the k.sup.th tunnel junction, where the (2k−1).sup.th common confining layer is in contact with the k.sup.th tunnel junction; and a 2k.sup.th common

confining layer arranged between the (k+1).sup.th active layer and the k.sup.th tunnel junction, where the 2k.sup.th common confining layer is in contact with the k.sup.th tunnel junction, and a conductivity type of the 2k.sup.th common confining layer is opposite to a conductivity type of the (2k−1).sup.th common confining layer and the same as the conductivity type of the k.sup.th second-semiconductor layer, where a total thickness of the (2k−1).sup.th common confining layer and the 2k.sup.th common confining layer is greater than a critical optical field coupling thickness and less than or equal to twice the critical optical field coupling thickness; and a thickness of the k.sup.th quantum well layer is less than or equal to 1/10 of a thickness of the (2k−1).sup.th common confining layer, and the thickness of the k.sup.th quantum well layer is less than or equal to 1/10 of a thickness of the 2k.sup.th common confining layer.

(7) Optionally, the (2k−1).sup.th common confining layer is used for confining optical fields in the k.sup.th active layer and the (k+1).sup.th active layer, and the 2k.sup.th common confining layer is used for confining the optical fields in the (k+1).sup.th active layer and the k.sup.th active layer.

(8) Optionally, the critical optical field coupling thickness ranges from 0.3 micrometers to 5 micrometers.

(9) Optionally, the total thickness of the (2k−1).sup.th common confining layer and the 2k.sup.th common confining layer ranges from 0.4 micrometers to 6 micrometers.

(10) Optionally, the thickness of the k.sup.th quantum well layer is less than or equal to 10 nanometers.

(11) Optionally, a doping concentration in the k.sup.th quantum well layer is greater than a doping concentration in the (2k−1).sup.th common confining layer and greater than a doping concentration in the 2k.sup.th common confining layer.

(12) Optionally, the doping concentration in the k.sup.th quantum well layer ranges from 5 E18 atom/cm.sup.3 to 1 E20 atom/cm.sup.3.

(13) Optionally, a material of the k.sup.th first-semiconductor layer is the same as a material of the (2k−1).sup.th common confining layer; and a material of the k.sup.th second-semiconductor layer is the same as a material of the 2k.sup.th common confining layer.

(14) Optionally, when the semiconductor substrate layer is a GaAs substrate, the material of the k.sup.th first-semiconductor layer and the (2k−1).sup.th common confining layer is Al.sub.x1Ga.sub.1-x1As, (Al.sub.x2Ga.sub.1-x2).sub.0.51In.sub.0.49P or In.sub.1-x3Ga.sub.x3As.sub.y1P.sub.1-y1 doped with P-type conductive ions, and the material of the k.sup.th second-semiconductor layer and the 2k.sup.th common confining layer is Al.sub.x1Ga.sub.1-x1As, (Al.sub.x2Ga.sub.1-x2).sub.0.51In.sub.0.49P or In.sub.1-x3Ga.sub.x3As.sub.y1P.sub.1-y1 doped with N-type conductive ions; and when the semiconductor substrate layer is an InP substrate, the material of the k.sup.th first-semiconductor layer and the (2k−1).sup.th common confining layer is InP, In.sub.0.53(Al.sub.x4Ga.sub.1-x4).sub.0.47As or In.sub.1-x5Ga.sub.x5As.sub.y2P.sub.1-y2 doped with P-type conductive ions, and the material of the k.sup.th second-semiconductor layer and the 2k.sup.th common confining layer is InP, In.sub.0.53(Al.sub.x4Ga.sub.1-x4).sub.0.47As or In.sub.1-x5Ga.sub.x5As.sub.y2P.sub.1-y2 doped with N-type conductive ions.

(15) Optionally, a conductivity type of the k.sup.th quantum well layer is an N type, and doped ions in the k.sup.th quantum well layer are Te ions or Si ions.

(16) Optionally, a material of the k.sup.th quantum well layer is In.sub.yGa.sub.1-yAs doped with Te ions or Si ions.

(17) Optionally, the semiconductor structure further includes: a lower confining layer arranged between the semiconductor substrate layer and the first active layer; an upper confining layer arranged on a side of the N.sup.th active layer away from the semiconductor substrate layer; a first waveguide layer arranged between the first active layer and the lower confining layer; a 2k.sup.th waveguide layer arranged between the k.sup.th active layer and the (2k−1).sup.th common confining layer; and a (2k+1).sup.th waveguide layer arranged between the (k+1).sup.th active

layer and the 2k.sup.th common confining layer.
(18) The present application further provides a method for manufacturing a multi-active area semiconductor structure, including: providing a semiconductor substrate layer; sequentially forming a first active layer to an N.sup.th active layer on the semiconductor substrate layer, where N is an integer greater than or equal to 2; forming a k.sup.th tunnel junction before a (k+1).sup.th active layer is formed, where k is greater than or equal to 1 and less than or equal to N−1; and the step of forming a k.sup.th tunnel junction includes: sequentially forming a k.sup.th first-semiconductor layer, a k.sup.th quantum well layer, and a k.sup.th second-semiconductor layer on a side of a k.sup.th active layer away from the semiconductor substrate layer, the k.sup.th first-semiconductor layer and the k.sup.th second-semiconductor layer are of opposite conductivity types, and a forbidden band width of the k.sup.th quantum well layer is less than both a forbidden band width of the k.sup.th first-semiconductor layer and a forbidden band width of the k.sup.th second-semiconductor layer; forming a (2k−1).sup.th common confining layer on the side of the k.sup.th active layer away from the semiconductor substrate layer before the k.sup.th tunnel junction is formed, where, after the k.sup.th tunnel junction is formed, the (2k−1).sup.th common confining layer is in contact with the k.sup.th tunnel junction; and forming a 2k.sup.th common confining layer on a side of the k.sup.th tunnel junction away from the semiconductor substrate layer before the (k+1).sup.th active layer is formed, where the 2k.sup.th common confining layer is in contact with the k.sup.th tunnel junction, and a conductivity type of the 2k.sup.th common confining layer is opposite to a conductivity type of the (2k−1).sup.th common confining layer and the same as the conductivity type of the k.sup.th second-semiconductor layer, where a total thickness of the (2k−1).sup.th common confining layer and the 2k.sup.th common confining layer is greater than a critical optical field coupling thickness and less than or equal to twice the critical optical field coupling thickness; and a thickness of the k.sup.th quantum well layer is less than or equal to 1/10 of a thickness of the (2k−1).sup.th common confining layer, and the thickness of the k.sup.th quantum well layer is less than or equal to 1/10 of a thickness of the 2k.sup.th common confining layer.
(19) Optionally, the (2k−1).sup.th common confining layer is used for confining optical fields in the k.sup.th active layer and the (k+1).sup.th active layer, and the 2k.sup.th common confining layer is used for confining the optical fields in the (k+1).sup.th active layer and the k.sup.th active layer.
(20) Optionally, doped ions in the k.sup.th quantum well layer are Te ions; the step of forming a k.sup.th quantum well layer includes: sequentially and consecutively performing a first stage and a second stage, where a temperature in the first stage is constant, a temperature in the second stage increases as a growth time increases, and a temperature at a starting moment of the second stage is the same as the temperature in the first stage; and a flow rate of a Te doping gas source in a chamber in the first stage is constant, a flow rate of the Te doping gas source in the chamber in the second stage decreases as the growth time increases, and a flow rate of the Te doping gas source at the starting moment of the second stage is the same as the flow rate of the Te doping gas source in the first stage; and the method for manufacturing the multi-active area semiconductor structure further includes: introducing the Te doping gas source into the chamber in an end stage of forming the k.sup.th first-semiconductor layer, where a flow rate of the Te doping gas source introduced into the chamber increases as the growth time increases, and a flow rate of the Te doping gas source corresponding to an end moment of the end stage of forming the k.sup.th first-semiconductor layer is the same as the flow rate of the Te doping gas source in the first stage.
(21) Optionally, a duration of the end stage of forming the k.sup.th first-semiconductor layer ranges from 1 second to 30 seconds; and a duration of the second stage ranges from 30 seconds to 1 minute.
(22) Optionally, a temperature at a termination moment of the second stage is increased by 10% to 30% with respect to the temperature at the starting moment of the second stage.

(23) Optionally, a flow rate of the Te doping gas source corresponding to a termination moment of the second stage is zero; and the flow rate of the Te doping gas source introduced in the end stage of forming the k.sup.th first-semiconductor layer increases from zero until becoming the same as the flow rate of the Te doping gas source in the first stage.
(24) Optionally, the flow rate of the Te doping gas source in the first stage ranges from 10 sccm to 20 sccm.
(25) Optionally, doped ions in the k.sup.th quantum well layer are Te ions, and Te ions are doped in the k.sup.th second-semiconductor layer; in a process of forming the k.sup.th quantum well layer, a temperature is constant and a flow rate of a Te doping gas source is constant; the step of forming a k.sup.th second-semiconductor layer includes: sequentially and consecutively performing a third stage and a fourth stage, where a temperature in the third stage is constant, a temperature in the fourth stage increases as a growth time increases, and a temperature at a starting moment of the fourth stage is the same as the temperature in the third stage; and a flow rate of the Te doping gas source in a chamber in the third stage is constant, a flow rate of the Te doping gas source in the chamber in the fourth stage decreases as the growth time increases, and a flow rate of the Te doping gas source at the starting moment of the fourth stage is the same as the flow rate of the Te doping gas source in the third stage; and the method for manufacturing the multi-active area semiconductor structure further includes: introducing the Te doping gas source into the chamber in an end stage of forming the k.sup.th first-semiconductor layer, where a flow rate of the Te doping gas source introduced into the chamber increases as the growth time increases, and a flow rate of the Te doping gas source corresponding to an end moment of the end stage of forming the k.sup.th first-semiconductor layer is the same as the flow rate of the Te doping gas source used in the process of forming the k.sup.th quantum well layer.
(26) Optionally, the method further includes: forming a lower confining layer on the semiconductor substrate layer before the first active layer is formed; forming a first waveguide layer on a side of the lower confining layer away from the semiconductor substrate layer; forming a 2k.sup.th waveguide layer on the side of the k.sup.th active layer away from the semiconductor substrate layer before the (2k−1).sup.th common confining layer is formed; forming a (2k+1).sup.th waveguide layer on a side of the 2k.sup.th common confining layer away from the semiconductor substrate layer before the (k+1).sup.th active layer is formed; and forming an upper confining layer on a side of the N.sup.th active layer away from the semiconductor substrate layer.
(27) The technical solutions of the present application have the following beneficial effects.
(28) In the multi-active area semiconductor structure provided in the technical solution of the present application, a forbidden band width of a k.sup.th quantum well layer is less than both a forbidden band width of a k.sup.th first-semiconductor layer and a forbidden band width of a k.sup.th second-semiconductor layer in a k.sup.th tunnel junction, so that a tunneling probability of the k.sup.th tunnel junction can be increased, thereby reducing a junction resistance. A (2k−1).sup.th common confining layer is provided between a k.sup.th active layer and the k.sup.th tunnel junction, and a 2k.sup.th common confining layer is provided between a (k+1).sup.th active layer and the k.sup.th tunnel junction. Because both the (2k−1).sup.th common confining layer and the 2k.sup.th common confining layer are in contact with the k.sup.th tunnel junction, some ohmic contact layers and some buffer layers disposed between the first active layer and an N.sup.th active layer are omitted. Because some ohmic contact layers and some buffer layers disposed between the first active layer and the N.sup.th active layer are omitted, a total thickness of the (2k−1).sup.th common confining layer and the 2k.sup.th common confining layer is greater than a critical optical field coupling thickness and less than or equal to twice the critical optical field coupling thickness. In this way, the thickness of the multi-active area semiconductor structure is effectively reduced. As the thickness of the multi-active area semiconductor structure is reduced, the resistance of the multi-active area semiconductor structure is effectively reduced, and a spacing between spots emitted by adjacent active layers is reduced, thereby improving the optical performance. Next, the

forbidden band width of the k.sup.th quantum well layer is less than both the forbidden band width of the k.sup.th first-semiconductor layer and the forbidden band width of the k.sup.th second-semiconductor layer in the k.sup.th tunnel junction. Therefore, a refractive index of the k.sup.th quantum well layer is greater than a refractive index of the k.sup.th first-semiconductor layer and a refractive index of the k.sup.th second-semiconductor layer. The refractive index of the k.sup.th quantum well layer is relatively large. The thickness of the k.sup.th quantum well layer is less than or equal to 1/10 of the thickness of the (2k−1).sup.th common confining layer, and the thickness of the k.sup.th quantum well layer is less than or equal to 1/10 of the thickness of the 2k.sup.th common confining layer. In this way, the thickness of the k.sup.th quantum well layer is extremely small. The k.sup.th quantum well layer with an extremely small thickness can avoid crosstalk in optical fields on two sides of the k.sup.th tunnel junction, thereby avoiding a decrease in laser power and a change in a divergence angle. In summary, the light-emission efficiency is effectively improved, and the optical field crosstalk is effectively reduced.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

(1) To describe the technical solutions in specific embodiments of the present application or the prior art more clearly, the following briefly introduces the accompanying drawings required for describing the specific embodiments or the prior art. Apparently, the accompanying drawings in the following description show some embodiments of the present application, and a person of ordinary skill in the art may still derive other drawings from these accompanying drawings without creative efforts.

(2) FIG. **1** is a schematic diagram of a multi-active area semiconductor structure according to an embodiment of the present application;

(3) FIG. **2** is a diagram of optical field distribution a multi-active area semiconductor structure according to an embodiment of the present application;

(4) FIG. **3** is a schematic diagram of the temperature and the flow rate of a Te doping gas source in a growth process of a k.sup.th quantum well layer in a multi-active area semiconductor structure according to an embodiment of the present application; and

(5) FIG. **4** is a schematic diagram of the temperature and the flow rate of a Te doping gas source in a growth process of a k.sup.th quantum well layer and a k.sup.th second-semiconductor layer in a multi-active area semiconductor structure according to another embodiment of the present application.

DETAILED DESCRIPTION

(6) The output power of a semiconductor laser is generally increased by increasing an injection current. The internal quantum efficiency of a conventional quantum well type semiconductor laser with a single active area remains less than 1. However, as the current increases, the thickness of a power supply transmission lead required for the semiconductor laser needs to be increased to reduce the resistance to maintain the reliability of power supply. A nearly double power output can be reached at a single injection current by using a double active area semiconductor laser, thereby reducing an operating current. In the epitaxial structure of the double active area semiconductor laser, two active areas are vertically stacked through one single epitaxial growth. An upper active area and a lower active area are connected in series by an inversely highly doped PN tunnel junction. After one carrier has passed through the first active area to participate in recombination and light emission, the inversion is completed at the tunnel junction and can also participate in recombination and light emission in the second active area. A tunnel structure in the double active area semiconductor laser includes a first doped semiconductor layer and a second doped semiconductor layer that are of opposite conductivity types.

(7) The requirements for a good tunnel junction in the double active area semiconductor laser are as follows: forbidden band widths of the first doped semiconductor layer and the second doped semiconductor layer need to be small. If the forbidden band widths of the first doped semiconductor layer and the second doped semiconductor layer are large, the tunnel junction has a low tunneling probability, that is, the tunnel junction resistance is large. The first doped semiconductor layer and the second doped semiconductor layer need to be heavily doped into a degenerate semiconductor. An interface between the first doped semiconductor layer and the second doped semiconductor layer needs to be steep, with low impurity diffusion and a thin depletion layer. It is only in this way that a tunnel junction with a low series resistance can be formed, or otherwise, a tunnel junction with a high resistance is formed, which in one aspect directly causes an increase in the operating voltage of the double active area semiconductor laser, resulting in reduced electro-optical efficiency, and in another aspect increases the waste heat at the tunnel junction, resulting in deteriorated performance of the double active area semiconductor laser.
(8) In the epitaxial structure of a multi-active area semiconductor laser, multiple (Q) complete single active area structures are generally connected by a tunnel junction. In this way, a total epitaxial thickness of a multi-active area structure is Q times the thickness of a single active area and Q times the thickness of the tunnel junction. The total thickness is relatively large. The series resistance of the multi-active area semiconductor laser is equal to the resistance of Q complete single active area semiconductor lasers plus the resistance of the tunnel junction. Such a design is a simple structural stack and has both a thickness and a resistance Q times the original.
(9) In addition, in terms of optics, a total epitaxial thickness of a relatively thick multi-active area structure represents a larger distance between corresponding light emission fields of active areas. During optical shaping, the dispersion angle in a vertical direction is relatively large, which affects the optical performance. Especially, a LIDAR chip requires relatively large optical indicators.
(10) To reduce the total thickness of the epitaxial structure of a multi-active area semiconductor laser with a particular quantity of active areas, in one method, a confining layer is placed in direct contact with a tunnel junction, some ohmic contact layers and buffer layers are omitted, and the thickness of the confining layer is reduced.
(11) However, the foregoing structure causes crosstalk in optical fields on two sides of a tunnel junction, to cause changes in a laser mode and a divergence angle.
(12) Based on this, the present application provides a multi-active area semiconductor structure, including: a (2k−1).sup.th common confining layer arranged between the k.sup.th active layer and the k.sup.th tunnel junction, where the (2k−1).sup.th common confining layer is in contact with the k.sup.th tunnel junction; and a 2k.sup.th common confining layer arranged between the (k+1).sup.th active layer and the k.sup.th tunnel junction, where the 2k.sup.th common confining layer is in contact with the k.sup.th tunnel junction, and where a forbidden band width of a k.sup.th quantum well layer is less than both a forbidden band width of a k.sup.th first-semiconductor layer and a forbidden band width of a k.sup.th second-semiconductor layer; a total thickness of the (2k−1).sup.th common confining layer and the 2k.sup.th common confining layer is greater than a critical optical field coupling thickness and less than or equal to twice the critical optical field coupling thickness; and a thickness of the k.sup.th quantum well layer is less than or equal to 1/10 of a thickness of the (2k−1).sup.th common confining layer, and the thickness of the k.sup.th quantum well layer is less than or equal to 1/10 of a thickness of the 2k.sup.th common confining layer. The multi-active area semiconductor structure has effectively improved light-emission efficiency and reduced optical field crosstalk.
(13) The following clearly and completely describes the technical solutions in the present application with reference to the accompanying drawings. Apparently, the described embodiments are some rather than all of the embodiments of the present application. All other embodiments obtained by persons of ordinary skill in the art based on the embodiments of the present application without creative efforts shall fall within the protection scope of the present application.

(14) In the description of the present application, it needs to be understood that orientation or location relationships indicated by terms “center”, “up”, “down”, “left”, “right”, “vertical”, “horizontal”, “inside”, and “outside” are based on orientation or location relationships shown in the accompanying drawings, and are only used to facilitate description of the present application and simplify description, but are not used to indicate or imply that the apparatuses or elements must have specific orientations or are constructed and operated by using specific orientations, and therefore, cannot be understood as a limit to the present application. In addition, the terms “first”, “second”, and “third” are used only for description, but are not intended to indicate or imply relative importance.

(15) In addition, the technical features involved in different embodiments of the present application described below can be combined with each other as long as they do not constitute a conflict between them.

(16) An embodiment of the present application provides a multi-active area semiconductor structure, referring to FIG. **1**, including: a semiconductor substrate layer **100**; a first active layer **140** to an N.sup.th active layer arranged on the semiconductor substrate layer **100**, where N is an integer greater than or equal to 2; a k.sup.th tunnel junction arranged between a k.sup.th active layer and a (k+1).sup.th active layer, where k is greater than or equal to 1 and less than or equal to N−1; and the k.sup.th tunnel junction includes a k.sup.th first-semiconductor layer and a k.sup.th second-semiconductor layer that are of opposite conductivity types and a k.sup.th quantum well layer, the k.sup.th second-semiconductor layer is arranged on a side of the k.sup.th first-semiconductor layer away from the k.sup.th active layer, the k.sup.th quantum well layer is arranged between the k.sup.th second-semiconductor layer and the k.sup.th first-semiconductor layer, and a forbidden band width of the k.sup.th quantum well layer is less than both a forbidden band width of the k.sup.th first-semiconductor layer and a forbidden band width of the k.sup.th second-semiconductor layer; a (2k−1).sup.th common confining layer arranged between the k.sup.th active layer and the k.sup.th tunnel junction, where the (2k−1).sup.th common confining layer is in contact with the k.sup.th tunnel junction; and a 2k.sup.th common confining layer arranged between the (k+1).sup.th active layer and the k.sup.th tunnel junction, where the 2k.sup.th common confining layer is in contact with the k.sup.th tunnel junction, and a conductivity type of the 2k.sup.th common confining layer is opposite to a conductivity type of the (2k−1).sup.th common confining layer and the same as the conductivity type of the k.sup.th second-semiconductor layer, where a total thickness of the (2k−1).sup.th common confining layer and the 2k.sup.th common confining layer is greater than a critical optical field coupling thickness and less than or equal to twice the critical optical field coupling thickness; and a thickness of the k.sup.th quantum well layer is less than or equal to 1/10 of a thickness of the (2k−1).sup.th common confining layer, and the thickness of the k.sup.th quantum well layer is less than or equal to 1/10 of a thickness of the 2k.sup.th common confining layer.

(17) In this embodiment, because both the (2k−1).sup.th common confining layer and the 2k.sup.th common confining layer are in contact with the k.sup.th tunnel junction, some ohmic contact layers and some buffer layers disposed between the first active layer and an N.sup.th active layer are omitted. Because some ohmic contact layers and some buffer layers disposed between the first active layer and the N.sup.th active layer are omitted, a total thickness of the (2k−1).sup.th common confining layer and the 2k.sup.th common confining layer is greater than a critical optical field coupling thickness and less than or equal to twice the critical optical field coupling thickness. In this way, the thickness of the multi-active area semiconductor structure is effectively reduced. As the thickness of the multi-active area semiconductor structure is reduced, the resistance of the multi-active area semiconductor structure is effectively reduced, and a spacing between spots emitted by adjacent active layers is reduced, thereby improving the optical performance. Next, the forbidden band width of the k.sup.th quantum well layer is less than both the forbidden band width of the k.sup.th first-semiconductor layer and the forbidden band width of the k.sup.th second-

semiconductor layer in the k.sup.th tunnel junction. Therefore, a refractive index of the k.sup.th quantum well layer is greater than a refractive index of the k.sup.th first-semiconductor layer and a refractive index of the k.sup.th second-semiconductor layer. The refractive index of the k.sup.th quantum well layer is relatively large. The thickness of the k.sup.th quantum well layer is less than or equal to 1/10 of the thickness of the (2k−1).sup.th common confining layer, and the thickness of the k.sup.th quantum well layer is less than or equal to 1/10 of the thickness of the 2k.sup.th common confining layer. In this way, the thickness of the k.sup.th quantum well layer is extremely small. The k.sup.th quantum well layer with an extremely small thickness can avoid crosstalk in optical fields on two sides of the k.sup.th tunnel junction, thereby avoiding changes in a laser mode and a divergence angle.

(18) In this embodiment, an example in which the multi-active area semiconductor structure is an edge-emitting multi-active area semiconductor laser is used for description.

(19) In this embodiment, the semiconductor substrate layer is a gallium arsenide substrate layer. It needs to be noted that in other embodiments, the semiconductor substrate layer may be a substrate layer made of another material.

(20) The multi-active area semiconductor structure further includes: a lower confining layer **120** arranged between the semiconductor substrate layer **100** and the first active layer **140**; an upper confining layer **190** arranged on a side of the N.sup.th active layer away from the semiconductor substrate layer **100**; a first waveguide layer **131** arranged between the first active layer **140** and the lower confining layer **120**; a 2k.sup.th waveguide layer arranged between the k.sup.th active layer and the (2k−1).sup.th common confining layer; and a (2k+1).sup.th waveguide layer arranged between the (k+1).sup.th active layer and the 2k.sup.th common confining layer.

(21) The multi-active area semiconductor structure further includes: a buffer layer **101** arranged between the lower confining layer **120** and the semiconductor substrate layer **100**; and an ohmic contact semiconductor layer **200** arranged on a surface of a side of the upper confining layer **190** away from the semiconductor substrate layer **100**.

(22) In this embodiment, the semiconductor substrate layer is a GaAs substrate layer, and the buffer layer is a GaAs buffer layer. In other embodiments, the semiconductor substrate layer is an InP substrate layer, and the buffer layer is an InP buffer layer.

(23) The (2k−1).sup.th common confining layer and the 2k.sup.th common confining layer between the k.sup.th active layer and the (k+1).sup.th active layer are used as one complete common confining layer. The (2k−1).sup.th common confining layer confines both an optical field in the k.sup.th active layer and an optical field in the (k+1).sup.th active layer. The 2k.sup.th common confining layer confines both the optical field in the (k+1).sup.th active layer and the optical field in the k.sup.th active layer. In this way, it can be set that both the (2k−1).sup.th common confining layer and the 2k.sup.th common confining layer have relatively small thicknesses, so that the resistance can be reduced.

(24) The total thickness of the (2k−1).sup.th common confining layer and the 2k.sup.th common confining layer is greater than the critical optical field coupling thickness and less than or equal to twice the critical optical field coupling thickness. The physical meaning of the critical optical field coupling thickness is that in a case that no tunnel junction is disposed in the multi-active area semiconductor structure, when the total thickness of the (2k−1).sup.th common confining layer and the 2k.sup.th common confining layer is equal to the critical optical field coupling thickness, the optical field in the k.sup.th active layer and the optical field in the (k+1).sup.th active layer are in a coupled critical state.

(25) It needs to be noted that in the prior art, the thickness of a single-layer N-type confining layer is greater than the critical optical field coupling thickness, the thickness of a single-layer P-type confining layer is greater than the critical optical field coupling thickness, and a total thickness of the single-layer N-type confining layer and the single-layer P-type confining layer is greater than twice the critical optical field coupling thickness.

(26) In this embodiment, the critical optical field coupling thickness ranges from 0.3 micrometers to 5 micrometers, and is, for example, 0.3 micrometers, 1 micrometer, 2 micrometers, 3 micrometers, 4 micrometers or 5 micrometers. It needs to be noted that the critical optical field coupling thickness may vary in different multi-active area semiconductor structures.
(27) In an embodiment, the total thickness of the (2k−1).sup.th common confining layer and the 2k.sup.th common confining layer ranges from 0.4 micrometers to 6 micrometers. The thickness of the (2k−1).sup.th common confining layer ranges from 0.2 micrometers to 3 micrometers, and is, for example, 0.2 micrometers, 0.5 micrometers, 0.8 micrometers, 1 micrometer, 1.5 micrometers, 2 micrometers, 2.5 micrometers or 3 micrometers. The thickness of the 2k.sup.th common confining layer ranges from 0.2 micrometers to 3 micrometers, and is, for example, 0.2 micrometers, 0.5 micrometers, 0.8 micrometers, 1 micrometer, 1.5 micrometers, 2 micrometers, 2.5 micrometers or 3 micrometers.
(28) In this embodiment, the thickness of the (2k−1).sup.th common confining layer is equal to the thickness of the 2k.sup.th common confining layer. In other embodiments, the thickness of the (2k−1).sup.th common confining layer is not equal to the thickness of the 2k.sup.th common confining layer.
(29) In this embodiment, when the semiconductor substrate layer **100** is a GaAs substrate, the material of the (2k−1).sup.th common confining layer is Al.sub.x1Ga.sub.1-x1As, (Al.sub.x2Ga.sub.1-x2).sub.0.51In.sub.0.49P or In.sub.1-x3Ga.sub.x3As.sub.y1P.sub.1-y1 doped with P-type conductive ions. When the semiconductor substrate layer **100** is a GaAs substrate, the material of the 2k.sup.th common confining layer is Al.sub.x1Ga.sub.1-x1As, (Al.sub.x2Ga.sub.1-x2).sub.0.51In.sub.0.49P or In.sub.1-x3Ga.sub.x3As.sub.y1P.sub.1-y1 doped with N-type conductive ions. x1 ranges from 0.2 to 0.9, x2 ranges from 0 to 1, x3 ranges from 0.52 to 1, and y1 ranges from 0 to 1.
(30) In other embodiments, when the semiconductor substrate layer **100** is an InP substrate, the material of the (2k−1).sup.th common confining layer is InP, In.sub.0.53(Al.sub.x4Ga.sub.1-x4).sub.0.47As or In.sub.1-x5Ga.sub.x5As.sub.y2P.sub.1-y2 doped with P-type conductive ions. When the semiconductor substrate layer **100** is an InP substrate, the material of the 2k.sup.th common confining layer is InP, In.sub.0.53(Al.sub.x4Ga.sub.1-x4).sub.0.47As or In.sub.1-x5Ga.sub.x5As.sub.y2P.sub.1-y2 doped with N-type conductive ions. X4 ranges from 0 to 1, x5 ranges from 0 to 0.47, and y2 ranges from 0 to 1.
(31) A forbidden band width of the (2k−1).sup.th common confining layer is greater than a forbidden band width of the buffer layer **101** and is greater than a forbidden band width of the ohmic contact semiconductor layer **200**. A forbidden band width of the 2k.sup.th common confining layer is greater than the forbidden band width of the buffer layer **101** and is greater than the forbidden band width of the ohmic contact semiconductor layer **200**. That is, the forbidden band width of the (2k−1).sup.th common confining layer and the forbidden band width of the 2k.sup.th common confining layer are both relatively large. Correspondingly, a refractive index of the (2k−1).sup.th common confining layer and a refractive index of the 2k.sup.th common confining layer are both relatively small.
(32) In this embodiment, it is set that the material of the k.sup.th first-semiconductor layer is the same as the material of the (2k−1).sup.th common confining layer; and it is set that the material of the k.sup.th second-semiconductor layer is the same as a material of the 2k.sup.th common confining layer. In this way, the refractive index of the k.sup.th first-semiconductor layer in the k.sup.th tunnel junction is relatively small, the refractive index of the k.sup.th second-semiconductor layer in the k.sup.th tunnel junction is relatively small, and the k.sup.th first-semiconductor layer and the k.sup.th second-semiconductor layer have relatively low impact on the optical field in the k.sup.th active layer and the optical field in the (k+1).sup.th active layer.
(33) In this embodiment, when the semiconductor substrate layer is a GaAs substrate, the material of the k.sup.th first-semiconductor layer and the (2k−1).sup.th common confining layer is

Al.sub.x1Ga.sub.1-x1As, (Al.sub.x2Ga.sub.1-x2).sub.0.51In.sub.0.49P or In.sub.1-x3Ga.sub.x3As.sub.y1P.sub.1-y1 doped with P-type conductive ions, and the material of the k.sup.th second-semiconductor layer and the 2k.sup.th common confining layer is Al.sub.x1Ga.sub.1-x1As, (Al.sub.x2Ga.sub.1-x2).sub.0.51In.sub.0.49P or In.sub.1-x3Ga.sub.x3As.sub.y1P.sub.1-y1 doped with N-type conductive ions; and when the semiconductor substrate layer is an InP substrate, the material of the k.sup.th first-semiconductor layer and the (2k−1).sup.th common confining layer is InP, In.sub.0.53(Al.sub.x4Ga.sub.1-x4).sub.0.47As or In.sub.1-x5Ga.sub.x5As.sub.y2P.sub.1-y2 doped with P-type conductive ions, and the material of the k.sup.th second-semiconductor layer and the 2k.sup.th common confining layer is InP, In.sub.0.53(Al.sub.x4Ga.sub.1-x4).sub.0.47As or In.sub.1-x5Ga.sub.x5As.sub.y2P.sub.1-y2 doped with N-type conductive ions.

(34) In this embodiment, the forbidden band width of the (2k−1).sup.th common confining layer and the forbidden band width of the 2k.sup.th common confining layer are both relatively large. Therefore, the k.sup.th quantum well layer is inserted between the (2k−1).sup.th common confining layer and the 2k.sup.th common confining layer. The forbidden band width of the k.sup.th quantum well layer is less than both the forbidden band width of the (2k−1).sup.th common confining layer and the forbidden band width of the 2k.sup.th common confining layer. Therefore, the forbidden band width of the k.sup.th quantum well layer is relatively small. In this way, a tunneling probability of the k.sup.th tunnel junction is greatly increased, thereby reducing the resistance of the k.sup.th tunnel junction.

(35) In an embodiment, the material of the k.sup.th quantum well layer is In.sub.yGa.sub.1-yAs doped with conductive ions, where y ranges from 0 to 0.2, and is, for example, 0.05, 0.1, 0.15 or 0.2. A forbidden band width of In.sub.yGa.sub.1-yAs is less than a forbidden band width of Al.sub.x1Ga.sub.1-x1As, the forbidden band width of In.sub.yGa.sub.1-yAs is less than a forbidden band width of (Al.sub.x2Ga.sub.1-x2).sub.0.51In.sub.0.49, the forbidden band width of In.sub.yGa.sub.1-yAs is less than a forbidden band width of In.sub.1-x3Ga.sub.x3As.sub.y1P.sub.1-y1, the forbidden band width of In.sub.yGa.sub.1-yAs is less than a forbidden band width of InP, the forbidden band width of In.sub.yGa.sub.1-yAs is less than a forbidden band width of In.sub.0.53(Al.sub.x4Ga.sub.1-x4).sub.0.47As, and the forbidden band width of In.sub.yGa.sub.1-yAs is less than a forbidden band width of In.sub.1-x5Ga.sub.x5As.sub.y2P.sub.1-y2.

(36) In this embodiment, the benefit of the conductivity type of the k.sup.th quantum well layer being the conductivity type of the k.sup.th second-semiconductor layer lies in that through the doping of Te ions in the N-type k.sup.th quantum well layer, it is easily implemented that an interface between the k.sup.th quantum well layer and the k.sup.th second-semiconductor layer is steep, and the k.sup.th quantum well layer and the k.sup.th second-semiconductor layer are uniformly doped.

(37) In this embodiment, the conductivity type of the k.sup.th quantum well layer and the conductivity type of the k.sup.th second-semiconductor layer are N types, and a conductivity type of the k.sup.th first-semiconductor layer is a P type. It needs to be noted that in other embodiments, the conductivity type of the k.sup.th quantum well layer may be consistent with the conductivity type of the k.sup.th first-semiconductor layer, and the conductivity type of the k.sup.th quantum well layer and the conductivity type of the k.sup.th first-semiconductor layer are P types.

(38) In an embodiment, a conductivity type of the k.sup.th quantum well layer is an N type, and doped ions in the k.sup.th quantum well layer are Te ions. In another embodiment, a conductivity type of the k.sup.th quantum well layer is an N type, and doped ions in the k.sup.th quantum well layer are Si ions.

(39) The thickness of the k.sup.th quantum well layer is extremely small. The k.sup.th quantum well layer with an extremely small thickness can compensate for the impact of a high refractive index of the k.sup.th quantum well layer on crosstalk in optical fields on two sides of the k.sup.th

tunnel junction, to prevent the k.sup.th quantum well layer with a high refractive index from causing crosstalk impact on the optical fields on the two sides of the k.sup.th tunnel junction.
(40) In a specific embodiment, the thickness of the k.sup.th quantum well layer is less than or equal to 10 nanometers, specifically ranges from 1 nanometer to 10 nanometers, and is, for example, 1 nanometer, 2 nanometers, 3 nanometers, 4 nanometers, 5 nanometers, 6 nanometers, 7 nanometers, 8 nanometers, 9 nanometers or 10 nanometers.
(41) In this embodiment, after the thickness of the k.sup.th quantum well layer decreases, to keep the effect of increasing the tunneling probability of the k.sup.th tunnel junction by the k.sup.th quantum well layer, a doping concentration in the k.sup.th quantum well layer needs to be increased, the steepness between the k.sup.th quantum well layer and the k.sup.th second-semiconductor layer is relatively large, and the steepness between the k.sup.th quantum well layer and the k.sup.th first-semiconductor layer is relatively large.
(42) In this embodiment, the doping concentration in the k.sup.th quantum well layer is greater than a doping concentration in the (2k−1).sup.th common confining layer and greater than a doping concentration in the 2k.sup.th common confining layer.
(43) In an embodiment, the doping concentration in the k.sup.th quantum well layer ranges from 5 E18 atom/cm.sup.3 to 1 E20 atom/cm.sup.3, and is, for example, 5 E18 atom/cm.sup.3, 1 E19 atom/cm.sup.3 or 1 E20 atom/cm.sup.3.
(44) The doped ions in the k.sup.th quantum well layer are Te ions, and the Te ions have a relatively large radius. Therefore, while the doping concentration in the k.sup.th quantum well layer is relatively high, low diffusibility is provided. The saturated doping concentration of Te ions is relatively high. It needs to be noted that in this embodiment the doped ions in the k.sup.th quantum well layer only includes Te ions.
(45) In this embodiment, in a thickness direction of the k.sup.th quantum well layer, and the doping concentration of the Te ions in the k.sup.th quantum well layer is uniform. In this way, it can be ensured that the k.sup.th quantum well layer and the k.sup.th first-semiconductor layer have a steep doping interface, and a junction resistance is relatively small.
(46) It needs to be noted that in other embodiments, the doped ions in the k.sup.th quantum well layer are Te ions, and Te ions are doped in the k.sup.th second-semiconductor layer.
(47) In this embodiment, an example in which N is equal to 2 is used for description.
(48) When N is equal to 2, the multi-active area semiconductor structure includes: a semiconductor substrate layer **100**; a buffer layer **101** arranged on the semiconductor substrate layer **100**; a lower confining layer **120** arranged on a side of the buffer layer **101** away from the semiconductor substrate layer **100**; a first waveguide layer **131** arranged on a side of the lower confining layer **120** away from the semiconductor substrate layer **100**; a first active layer **140** arranged on a side of the first waveguide layer **131** away from the semiconductor substrate layer **100**; a second waveguide layer **132** arranged on a side of the first active layer **140** away from the semiconductor substrate layer **100**; a first common confining layer **151** arranged on a side of the second waveguide layer **132** away from the semiconductor substrate layer **100**; and a first tunnel junction **160** arranged on a side of the first common confining layer **151** away from the first active layer **140** and in contact with the first common confining layer **151**, where the first tunnel junction **160** includes: a first first-semiconductor layer and a first second-semiconductor layer that are of opposite conductivity types and a first quantum well layer, a forbidden band width of the first quantum well layer is less than both a forbidden band width of the first first-semiconductor layer and a forbidden band width of the first second-semiconductor layer, the first second-semiconductor layer is arranged on a side of the first first-semiconductor layer away from the first active layer **140**, the first quantum well layer is arranged between the first second-semiconductor layer and the first first-semiconductor layer, and the first first-semiconductor layer is in contact with the first common confining layer **151**; a second common confining layer **152** arranged on a side of the first tunnel junction **160** away from the first active layer **140** and in contact with the first tunnel junction **160**, where the second common

confining layer **152** is in contact with the first second-semiconductor layer; a third waveguide layer **171** arranged on a side of the second common confining layer **152** away from the first tunnel junction **160**; a second active layer **180** arranged on a side of the third waveguide layer **171** away from the second common confining layer **152**; a fourth waveguide layer **172** arranged on a side of the second active layer **180** away from the third waveguide layer **171**; an upper confining layer **190** arranged on a side of the fourth waveguide layer **172** away from the second active layer **180**; and an ohmic contact semiconductor layer **200** arranged on a side of the upper confining layer **190** away from the second active layer **180**.

(49) A total thickness of the first common confining layer **151** and the second common confining layer **152** is less than the critical optical field coupling thickness. A conductivity type of the first common confining layer **151** is opposite to a conductivity type of the second common confining layer **152**. The first common confining layer **151** and the first first-semiconductor layer have the same conductivity type, and the second common confining layer **152** and the first second-semiconductor layer have the same conductivity type.

(50) The thickness of the first quantum well layer is less than or equal to 1/10 of the thickness of the first common confining layer **151**, and the thickness of the first quantum well layer is less than or equal to 1/10 of the thickness of the second common confining layer **152**.

(51) In other embodiments, N may be another integer greater than or equal to 3.

(52) FIG. **2** is a diagram of optical field distribution a multi-active area semiconductor structure according to an embodiment of the present application. Corresponding N in FIG. **2** is 2. A horizontal axis in FIG. **2** is a position of the multi-active area semiconductor structure in an epitaxial thickness direction. The unit of the horizontal axis in FIG. **2** is μm. There are sequentially from left to the right on the horizontal axis the buffer layer **101**, the lower confining layer **120**, the first waveguide layer **131**, the first active layer **140**, the second waveguide layer **132**, the first common confining layer **151**, the first tunnel junction **160**, the second common confining layer **152**, the third waveguide layer **171**, the second active layer **180**, the fourth waveguide layer **172**, the upper confining layer **190**, and the ohmic contact semiconductor layer **200**. A first vertical axis and a second vertical axis are provided in FIG. **2**. The first vertical axis is located on the left side in FIG. **2**, the second vertical axis is located on the right side in FIG. **2**, the first vertical axis represents a refractive index, and the second vertical axis represents an optical field. The thickness of the first quantum well layer ranges from 1 micrometer to 10 micrometers. The extremely narrow first quantum well layer does not have crosstalk impact on an optical field in the first active layer **140** and an optical field in the second active layer **180**.

(53) Correspondingly, this embodiment further provides a method for manufacturing a multi-active area semiconductor structure, including: providing a semiconductor substrate layer **100**; sequentially forming the first active layer **140** to an N.sup.th active layer on the semiconductor substrate layer **100**, where N is an integer greater than or equal to 2; forming a k.sup.th tunnel junction before a (k+1).sup.th active layer is formed, where k is greater than or equal to 1 and less than or equal to N−1; and the step of forming a k.sup.th tunnel junction includes: sequentially forming a k.sup.th first-semiconductor layer, a k.sup.th quantum well layer, and a k.sup.th second-semiconductor layer on a side of a k.sup.th active layer away from the semiconductor substrate layer **100**, the k.sup.th first-semiconductor layer and the k.sup.th second-semiconductor layer are of opposite conductivity types, and a forbidden band width of the k.sup.th quantum well layer is less than both a forbidden band width of the k.sup.th first-semiconductor layer and a forbidden band width of the k.sup.th second-semiconductor layer; forming a (2k−1).sup.th common confining layer on the side of the k.sup.th active layer away from the semiconductor substrate layer **100** before the k.sup.th tunnel junction is formed, where, after the k.sup.th tunnel junction is formed, the (2k−1).sup.th common confining layer is in contact with the k.sup.th tunnel junction; and forming a 2k.sup.th common confining layer on a side of the k.sup.th tunnel junction away from the semiconductor substrate layer **100** before the (k+1).sup.th active layer is formed, where the

2k.sup.th common confining layer is in contact with the k.sup.th tunnel junction, and a conductivity type of the 2k.sup.th common confining layer is opposite to a conductivity type of the (2k−1).sup.th common confining layer and the same as the conductivity type of the k.sup.th second-semiconductor layer, where a total thickness of the (2k−1).sup.th common confining layer and the 2k.sup.th common confining layer is greater than a critical optical field coupling thickness and less than or equal to twice the critical optical field coupling thickness; and a thickness of the k.sup.th quantum well layer is less than or equal to 1/10 of a thickness of the (2k−1).sup.th common confining layer, and the thickness of the k.sup.th quantum well layer is less than or equal to 1/10 of a thickness of the 2k.sup.th common confining layer.

(54) The method for manufacturing a multi-active area semiconductor structure further includes: forming a lower confining layer **120** on the semiconductor substrate layer **100** before the first active layer **140** is formed; forming a first waveguide layer **131** on a side of the lower confining layer **120** away from the semiconductor substrate layer **100** before the first active layer **140** is formed; forming a 2k.sup.th waveguide layer on the side of the k.sup.th active layer away from the semiconductor substrate layer **100** before the (2k−1).sup.th common confining layer is formed; forming a (2k+1).sup.th waveguide layer on a side of the 2k.sup.th common confining layer away from the semiconductor substrate layer **100** before the (k+1).sup.th active layer is formed; and forming an upper confining layer **190** on a side of the N.sup.th active layer away from the semiconductor substrate layer **100**. forming an ohmic contact semiconductor layer **200** on a side of the upper confining layer **190** away from the semiconductor substrate layer **100**.

(55) In this embodiment, an example in which N is equal to 2 is used for description.

(56) When N is equal to 2, a method for forming the multi-active area semiconductor structure includes: providing a semiconductor substrate layer **100**; forming a buffer layer **101** on the semiconductor substrate layer **100**; forming a lower confining layer **120** on a side of the buffer layer **101** away from the semiconductor substrate layer **100**; forming a first waveguide layer **131** on a side of the lower confining layer **120** away from the semiconductor substrate layer **100**; forming a first active layer **140** on a side of the first waveguide layer **131** away from the semiconductor substrate layer **100**; forming a second waveguide layer **132** on a side of the first active layer **140** away from the semiconductor substrate layer **100**; forming a first common confining layer **151** on a side of the second waveguide layer **132** away from the semiconductor substrate layer **100**; and forming a first tunnel junction **160** on a side of the first common confining layer **151** away from the first active layer **140** and in contact with the first common confining layer **151**, where a method for forming the first tunnel junction **160** includes: sequentially forming a first first-semiconductor layer, a first quantum well layer, and a first second-semiconductor layer, the first first-semiconductor layer and the first second-semiconductor layer have opposite conductivity types, a forbidden band width of the first quantum well layer is less than both a forbidden band width of the first first-semiconductor layer and a forbidden band width of the first second-semiconductor layer, and the first first-semiconductor layer is in contact with the first common confining layer **151**; forming a second common confining layer **152** on a side of the first tunnel junction **160** away from the first active layer **140** and in contact with the first tunnel junction **160**, where the second common confining layer **152** is in contact with the first second-semiconductor layer; forming a third waveguide layer **171** on a side of the second common confining layer **152** away from the first tunnel junction **160**; forming a second active layer **180** on a side of the third waveguide layer **171** away from the second common confining layer **152**; forming a fourth waveguide layer **172** on a side of the second active layer **180** away from the third waveguide layer **171**; forming an upper confining layer **190** on a side of the fourth waveguide layer **172** away from the second active layer **180**; and forming an ohmic contact semiconductor layer **200** on a side of the upper confining layer **190** away from the second active layer **180**.

(57) In other embodiments, N may be another integer greater than or equal to 3.

(58) In an embodiment, doped ions in the formed k.sup.th quantum well layer are Te ions.

Correspondingly, referring to FIG. **3**, the step of forming a k.sup.th quantum well layer includes: sequentially and consecutively performing a first stage and a second stage, where a temperature in the first stage is constant, a temperature in the second stage increases as a growth time increases, and a temperature at a starting moment of the second stage is the same as the temperature in the first stage; and a flow rate of a Te doping gas source in a chamber in the first stage is constant, a flow rate of the Te doping gas source in the chamber in the second stage decreases as the growth time increases, and a flow rate of the Te doping gas source at the starting moment of the second stage is the same as the flow rate of the Te doping gas source in the first stage; and the method for manufacturing the multi-active area semiconductor structure further includes: introducing the Te doping gas source into the chamber in an end stage of forming the k.sup.th first-semiconductor layer, where a flow rate of the Te doping gas source introduced into the chamber increases as the growth time increases, and a flow rate of the Te doping gas source corresponding to an end moment of the end stage of forming the k.sup.th first-semiconductor layer is the same as the flow rate of the Te doping gas source in the first stage.

(59) In a specific embodiment, the temperature in the second stage linearly increases as the growth time increases, and the flow rate of the Te doping gas source in the chamber in the second stage linearly decreases as the growth time increases. In the end stage of forming the k.sup.th first-semiconductor layer, the flow rate of the Te doping gas source introduced in the chamber linearly increases as the growth time increases.

(60) In the end stage of forming the k.sup.th first-semiconductor layer, the Te doping gas source is introduced in the chamber. A relaxation process of the Te doping gas source occurs before the first stage instead of in the first stage. Therefore, even if the Te doping gas source has a memory effect, that is, the Te doping gas source has a relaxation effect, the uniformity of the doping concentration in the k.sup.th quantum well layer can still be ensured in a process of performing the first stage, thereby avoiding the trend that the doping concentrations in film layers grown in the first stage increase. That is, it can be ensured that the doping concentrations in the film layers grown in the first stage are uniform in this embodiment. Especially the doping concentration in the first quantum well layer at the interface in contact with the k.sup.th first-semiconductor layer is relatively high, and the doping is steep between the k.sup.th first-semiconductor layer and the first quantum well layer. In the second stage, as the time increases, the temperature in the chamber keeps being increased, and the flow rate of the Te doping gas source is gradually decreased until a valve is closed. In the second stage, as the time increases, the temperature in the chamber keeps being increased, to enable the Te doping gas source attached on a chamber wall of the chamber to be desorbed and leave the chamber wall of the chamber, so that in a process of forming the 2k.sup.th common confining layer, an extra Te doping gas source is prevented from being doped and entering the 2k.sup.th common confining layer, to avoid that the concentration of N-type doped ions in the 2k.sup.th common confining layer is uncontrollable.

(61) Referring to FIG. **3**, a growth temperature of the k.sup.th first-semiconductor layer is equal to a temperature in the first stage.

(62) N-type conductive ions doped in the k.sup.th second-semiconductor layer include Si ions, Te ions or a combination thereof.

(63) It needs to be noted that in the end stage of forming the k.sup.th first-semiconductor layer, the Te doping gas source has a relaxation effect. Therefore, the Te doping gas source is not doped in the k.sup.th first-semiconductor layer in the end stage of forming the k.sup.th first-semiconductor layer.

(64) In an embodiment, a duration of the end stage of forming the k.sup.th first-semiconductor layer ranges from 1 second to 30 seconds, for example, 1 second, 5 seconds, 10 seconds, 20 seconds or 30 seconds.

(65) In an embodiment, a duration of the first stage is 30 seconds to 1 minute, and the duration of the first stage changes according to the thickness of the k.sup.th quantum well layer.

(66) In an embodiment, a duration of the second stage ranges from 30 seconds to 1 minute.
(67) In an embodiment, a temperature at a termination moment of the second stage is increased by 10% to 30% with respect to the temperature at the starting moment of the second stage, for example, by 10%, 15%, 20%, 25% or 30%.
(68) In an embodiment, the temperature in the second stage ranges from 550 degrees Celsius to 650 degrees Celsius, and the temperature in the first stage ranges from 550 degrees Celsius to 610 degrees Celsius.
(69) In an embodiment, a flow rate of the Te doping gas source corresponding to a termination moment of the second stage is zero; and the flow rate of the Te doping gas source introduced in the end stage of forming the k.sup.th first-semiconductor layer increases from zero until becoming the same as the flow rate of the Te doping gas source in the first stage.
(70) In an embodiment, the flow rate of the Te doping gas source in the first stage ranges from 10 sccm to 20 sccm.
(71) In another embodiment, doped ions in the k.sup.th quantum well layer are Te ions, and Te ions are doped in the k.sup.th second-semiconductor layer. Correspondingly, referring to FIG. **4**, in a process of forming the k.sup.th quantum well layer, a temperature is constant and a flow rate of a Te doping gas source is constant; the step of forming a k.sup.th second-semiconductor layer includes: sequentially and consecutively performing a third stage and a fourth stage, where a temperature in the third stage is constant, a temperature in the fourth stage increases as a growth time increases, and a temperature at a starting moment of the fourth stage is the same as the temperature in the third stage; and a flow rate of the Te doping gas source in a chamber in the third stage is constant, a flow rate of the Te doping gas source in the chamber in the fourth stage decreases as the growth time increases, and a flow rate of the Te doping gas source at the starting moment of the fourth stage is the same as the flow rate of the Te doping gas source in the third stage; and the method for manufacturing the multi-active area semiconductor structure further includes: introducing the Te doping gas source into the chamber in an end stage of forming the k.sup.th first-semiconductor layer, where a flow rate of the Te doping gas source introduced into the chamber increases as the growth time increases, and a flow rate of the Te doping gas source corresponding to an end moment of the end stage of forming the k.sup.th first-semiconductor layer is the same as the flow rate of the Te doping gas source used in the process of forming the k.sup.th quantum well layer. In a specific embodiment, the temperature in the fourth stage linearly increases as the growth time increases, and the flow rate of the Te doping gas source in the chamber in the fourth stage linearly decreases as the growth time increases. In the end stage of forming the k.sup.th first-semiconductor layer, the flow rate of the Te doping gas source introduced in the chamber linearly increases as the growth time increases.
(72) Referring to FIG. **4**, the growth temperature of the k.sup.th first-semiconductor layer, the growth temperature of the k.sup.th quantum well layer, and the temperature in the third stage are consistent. In an embodiment, a temperature at a termination moment of the fourth stage is increased by 10% to 30% with respect to the temperature at the starting moment of the third stage, for example, by 10%, 15%, 20%, 25% or 30%. The temperature in the fourth stage ranges from 550 degrees Celsius to 650 degrees Celsius, and the temperature in the third stage ranges from 550 degrees Celsius to 610 degrees Celsius. A flow rate of the Te doping gas source corresponding to a termination moment of the fourth stage is zero; and the flow rate of the Te doping gas source introduced in the end stage of forming the k.sup.th first-semiconductor layer increases from zero until becoming the same as the flow rate of the Te doping gas source used for forming the k.sup.th quantum well layer. The flow rate of the Te doping gas source in the third stage ranges from 10 sccm to 20 sccm. A duration of the fourth stage ranges from 30 seconds to 1 minute. The duration of the end stage of forming the k.sup.th first-semiconductor layer ranges from 1 second to 30 seconds, for example, 1 second, 5 seconds, 10 seconds, 20 seconds or 30 seconds.
(73) Obviously, the foregoing embodiments are merely examples for clear description, rather than a

limitation to implementations. For a person of ordinary skill in the art, other changes or variations in different forms may also be made based on the foregoing description. All implementations cannot and do not need to be exhaustively listed herein. Obvious changes or variations that are derived there from still fall within the protection scope of present application.

Claims

1. A multi-active area semiconductor structure, comprising: a semiconductor substrate layer; a first active layer to an N.sup.th active layer arranged on the semiconductor substrate layer, wherein N is an integer greater than or equal to 2; a k.sup.th tunnel junction arranged between a k.sup.th active layer and a (k+1).sup.th active layer, wherein k is greater than or equal to 1 and less than or equal to N−1; and the k.sup.th tunnel junction comprises a k.sup.th first-semiconductor layer and a k.sup.th second-semiconductor layer that are of opposite conductivity types and a k.sup.th quantum well layer, the k.sup.th second-semiconductor layer is arranged on a side of the k.sup.th first-semiconductor layer away from the k.sup.th active layer, the k.sup.th quantum well layer is arranged between the k.sup.th second-semiconductor layer and the k.sup.th first-semiconductor layer, and a forbidden band width of the k.sup.th quantum well layer is less than both a forbidden band width of the k.sup.th first-semiconductor layer and a forbidden band width of the k.sup.th second-semiconductor layer; a (2k−1).sup.th common confining layer arranged between the k.sup.th active layer and the k.sup.th tunnel junction, wherein the (2k−1).sup.th common confining layer is in contact with the k.sup.th tunnel junction; and a 2k.sup.th common confining layer arranged between the (k+1).sup.th active layer and the k.sup.th tunnel junction, wherein the 2k.sup.th common confining layer is in contact with the k.sup.th tunnel junction, and a conductivity type of the 2k.sup.th common confining layer is opposite to a conductivity type of the (2k−1).sup.th common confining layer and the same as the conductivity type of the k.sup.th second-semiconductor layer, wherein a total thickness of the (2k−1).sup.th common confining layer and the 2k.sup.th common confining layer is greater than a critical optical field coupling thickness and less than or equal to twice the critical optical field coupling thickness; and a thickness of the k.sup.th quantum well layer is less than or equal to 1/10 of a thickness of the (2k−1).sup.th common confining layer, and the thickness of the k.sup.th quantum well layer is less than or equal to 1/10 of a thickness of the 2k.sup.th common confining layer.
2. The multi-active area semiconductor structure according to claim 1, wherein the (2k−1).sup.th common confining layer is used for confining optical fields in the k.sup.th active layer and the (k+1).sup.th active layer, and the 2k.sup.th common confining layer is used for confining the optical fields in the (k+1).sup.th active layer and the k.sup.th active layer.
3. The multi-active area semiconductor structure according to claim 1, wherein the critical optical field coupling thickness ranges from 0.3 micrometers to 5 micrometers.
4. The multi-active area semiconductor structure according to claim 1, wherein the total thickness of the (2k−1).sup.th common confining layer and the 2k.sup.th common confining layer ranges from 0.4 micrometers to 6 micrometers.
5. The multi-active area semiconductor structure according to claim 1, wherein the thickness of the k.sup.th quantum well layer is less than or equal to 10 nanometers.
6. The multi-active area semiconductor structure according to claim 1, wherein a doping concentration in the k.sup.th quantum well layer is greater than a doping concentration in the (2k−1).sup.th common confining layer and greater than a doping concentration in the 2k.sup.th common confining layer.
7. The multi-active area semiconductor structure according to claim 6, wherein the doping concentration in the k.sup.th quantum well layer ranges from 5 E18 atom/cm.sup.3 to 1 E20 atom/cm.sup.3.
8. The multi-active area semiconductor structure according to claim 1, wherein a material of the

k.sup.th first-semiconductor layer is the same as a material of the (2k−1).sup.th common confining layer; and a material of the k.sup.th second-semiconductor layer is the same as a material of the 2k.sup.th common confining layer.

9. The multi-active area semiconductor structure according to claim 8, wherein when the semiconductor substrate layer is a GaAs substrate, the material of the k.sup.th first-semiconductor layer and the (2k−1).sup.th common confining layer is Al.sub.x1Ga.sub.1-x1As, (Al.sub.x2Ga.sub.1-x2).sub.0.51In.sub.0.49P or In.sub.1-x3Ga.sub.x3AS.sub.y1P.sub.1-y1 doped with P-type conductive ions, and the material of the k.sup.th second-semiconductor layer and the 2k.sup.th common confining layer is Al.sub.x1Ga.sub.1-x1As, (Al.sub.x2Ga.sub.1-x2).sub.0.51In.sub.0.49P or In.sub.1-x3Ga.sub.x3AS.sub.y1P.sub.1-y1 doped with N-type conductive ions; and when the semiconductor substrate layer is an InP substrate, the material of the k.sup.th first-semiconductor layer and the (2k−1).sup.th common confining layer is InP, In.sub.0.53(Al.sub.x4Ga.sub.1-x4).sub.0.47As or In.sub.1-x5Ga.sub.x5As.sub.y2P.sub.1-y2 doped with P-type conductive ions, and the material of the k.sup.th second-semiconductor layer and the 2k.sup.th common confining layer is InP, In.sub.0.53(Al.sub.x4Ga.sub.1-x4).sub.0.47As or In.sub.1-x5Ga.sub.x5As.sub.y2P.sub.1-y2 doped with N-type conductive ions.

10. The multi-active area semiconductor structure according to claim 1, wherein a conductivity type of the k.sup.th quantum well layer is an N type, and doped ions in the k.sup.th quantum well layer are Te ions or Si ions.

11. The multi-active area semiconductor structure according to claim 10, wherein a material of the k.sup.th quantum well layer is In.sub.yGa.sub.1-yAs doped with Te ions or Si ions.

12. The multi-active area semiconductor structure according to claim 1, further comprising: a lower confining layer arranged between the semiconductor substrate layer and the first active layer; an upper confining layer arranged on a side of the N.sup.th active layer away from the semiconductor substrate layer; a first waveguide layer arranged between the first active layer and the lower confining layer; a 2k.sup.th waveguide layer arranged between the k.sup.th active layer and the (2k−1).sup.th common confining layer; and a (2k+1).sup.th waveguide layer arranged between the (k+1).sup.th active layer and the 2k.sup.th common confining layer.

13. A method for manufacturing the multi-active area semiconductor structure according to claim 1, comprising: providing a semiconductor substrate layer; sequentially forming a first active layer to an N.sup.th active layer on the semiconductor substrate layer, wherein N is an integer greater than or equal to 2; forming a k.sup.th tunnel junction before a (k+1).sup.th active layer is formed, wherein k is greater than or equal to 1 and less than or equal to N−1; and the step of forming a k.sup.th tunnel junction comprises: sequentially forming a k.sup.th first-semiconductor layer, a k.sup.th quantum well layer, and a k.sup.th second-semiconductor layer on a side of a k.sup.th active layer away from the semiconductor substrate layer, the k.sup.th first-semiconductor layer and the k.sup.th second-semiconductor layer are of opposite conductivity types, and a forbidden band width of the k.sup.th quantum well layer is less than both a forbidden band width of the k.sup.th first-semiconductor layer and a forbidden band width of the k.sup.th second-semiconductor layer; forming a (2k−1).sup.th common confining layer on the side of the k.sup.th active layer away from the semiconductor substrate layer before the k.sup.th tunnel junction is formed, wherein, after the k.sup.th tunnel junction is formed, the (2k−1).sup.th common confining layer is in contact with the k.sup.th tunnel junction; and forming a 2k.sup.th common confining layer on a side of the k.sup.th tunnel junction away from the semiconductor substrate layer before the (k+1).sup.th active layer is formed, wherein the 2k.sup.th common confining layer is in contact with the k.sup.th tunnel junction, and a conductivity type of the 2k.sup.th common confining layer is opposite to a conductivity type of the (2k−1).sup.th common confining layer and the same as the conductivity type of the k.sup.th second-semiconductor layer, wherein a total thickness of the (2k−1).sup.th common confining layer and the 2k.sup.th common confining layer is greater than a critical optical field coupling thickness and less than or equal to twice the critical optical field

coupling thickness; and a thickness of the k.sup.th quantum well layer is less than or equal to 1/10 of a thickness of the (2k−1).sup.th common confining layer, and the thickness of the k.sup.th quantum well layer is less than or equal to 1/10 of a thickness of the 2k.sup.th common confining layer.

14. The method for manufacturing the multi-active area semiconductor structure according to claim 13, wherein the (2k−1).sup.th common confining layer is used for confining optical fields in the k.sup.th active layer and the (k+1).sup.th active layer, and the 2k.sup.th common confining layer is used for confining the optical fields in the (k+1).sup.th active layer and the k.sup.th active layer.

15. The method for manufacturing the multi-active area semiconductor structure according to claim 13, wherein doped ions in the k.sup.th quantum well layer are Te ions; the step of forming a k.sup.th quantum well layer comprises: sequentially and consecutively performing a first stage and a second stage, wherein a temperature in the first stage is constant, a temperature in the second stage increases as a growth time increases, and a temperature at a starting moment of the second stage is the same as the temperature in the first stage; and a flow rate of a Te doping gas source in a chamber in the first stage is constant, a flow rate of the Te doping gas source in the chamber in the second stage decreases as the growth time increases, and a flow rate of the Te doping gas source at the starting moment of the second stage is the same as the flow rate of the Te doping gas source in the first stage; and the method for manufacturing the multi-active area semiconductor structure further comprises: introducing the Te doping gas source into the chamber in an end stage of forming the k.sup.th first-semiconductor layer, wherein a flow rate of the Te doping gas source introduced into the chamber increases as the growth time increases, and a flow rate of the Te doping gas source corresponding to an end moment of the end stage of forming the k.sup.th first-semiconductor layer is the same as the flow rate of the Te doping gas source in the first stage.

16. The method for manufacturing the multi-active area semiconductor structure according to claim 15, wherein a duration of the end stage of forming the k.sup.th first-semiconductor layer ranges from 1 second to 30 seconds; and a duration of the second stage ranges from 30 seconds to 1 minute.

17. The method for manufacturing the multi-active area semiconductor structure according to claim 15, wherein a temperature at a termination moment of the second stage is increased by 10% to 30% with respect to the temperature at the starting moment of the second stage.

18. The method for manufacturing the multi-active area semiconductor structure according to claim 15, wherein a flow rate of the Te doping gas source corresponding to a termination moment of the second stage is zero; and the flow rate of the Te doping gas source introduced in the end stage of forming the k.sup.th first-semiconductor layer increases from zero until becoming the same as the flow rate of the Te doping gas source in the first stage.

19. The method for manufacturing the multi-active area semiconductor structure according to claim 13, wherein doped ions in the k.sup.th quantum well layer are Te ions, and Te ions are doped in the k.sup.th second-semiconductor layer; in a process of forming the k.sup.th quantum well layer, a temperature is constant and a flow rate of a Te doping gas source is constant; the step of forming a k.sup.th second-semiconductor layer comprises: sequentially and consecutively performing a third stage and a fourth stage, wherein a temperature in the third stage is constant, a temperature in the fourth stage increases as a growth time increases, and a temperature at a starting moment of the fourth stage is the same as the temperature in the third stage; and a flow rate of the Te doping gas source in a chamber in the third stage is constant, a flow rate of the Te doping gas source in the chamber in the fourth stage decreases as the growth time increases, and a flow rate of the Te doping gas source at the starting moment of the fourth stage is the same as the flow rate of the Te doping gas source in the third stage; and the method for manufacturing the multi-active area semiconductor structure further comprises: introducing the Te doping gas source into the chamber in an end stage of forming the k.sup.th first-semiconductor layer, wherein a flow rate of the Te doping gas source introduced into the chamber increases as the growth time increases, and a flow rate of the Te

doping gas source corresponding to an end moment of the end stage of forming the k.sup.th first-semiconductor layer is the same as the flow rate of the Te doping gas source used in the process of forming the k.sup.th quantum well layer.

20. The method for manufacturing the multi-active area semiconductor structure according to claim 13, further comprising: forming a lower confining layer on the semiconductor substrate layer before the first active layer is formed; forming a first waveguide layer on a side of the lower confining layer away from the semiconductor substrate layer; forming a 2k.sup.th waveguide layer on the side of the k.sup.th active layer away from the semiconductor substrate layer before the (2k−1).sup.th common confining layer is formed; forming a (2k+1).sup.th waveguide layer on a side of the 2k.sup.th common confining layer away from the semiconductor substrate layer before the (k+1).sup.th active layer is formed; and forming an upper confining layer on a side of the N.sup.th active layer away from the semiconductor substrate layer.