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Woo et al.

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(45) **Date of Patent: Aug. 19, 2025**

(54) **QUAD-CHANNEL DRAM**

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(73) Assignee: **Rambus Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **18/231,108**

(22) Filed: **Aug. 7, 2023**

(65) **Prior Publication Data**

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Related U.S. Application Data

(63) Continuation of application No. 17/433,071, filed as application No. PCT/US2020/018634 on Feb. 18, 2020, now Pat. No. 11,762,787.

(60) Provisional application No. 62/811,903, filed on Feb. 28, 2019.

(51) **Int. Cl.**
G06F 13/16 (2006.01)

(52) **U.S. Cl.**
CPC *G06F 13/1668* (2013.01)

(58) **Field of Classification Search**
None
See application file for complete search history.

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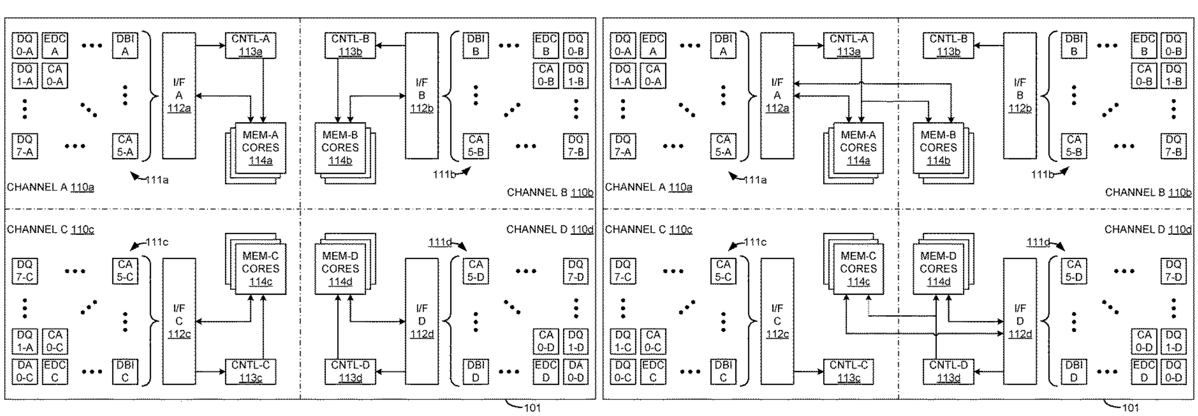
Primary Examiner — Michael Sun
(74) *Attorney, Agent, or Firm* — The Neudeck Law Firm, LLC

(57) **ABSTRACT**

A DRAM includes at least four groups of memory cores and at least four memory access channel interfaces that, in a first mode, each respectively are to receive memory access commands, directed to a corresponding one of the groups of memory cores. One-half of the memory access channel interfaces are to, in a second mode, each respectively receive memory access commands, directed to a corresponding two of four of the groups of memory cores. The memory access channel interfaces to have electrical connection conductors that lie on opposing sides of at least one line of reflectional symmetry from a second one-half of the one-half of the at least four memory access channel interfaces.

20 Claims, 22 Drawing Sheets



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Notification of Transmittal of the International Search Report and the Written Opinion of the International Searching Authority, or the Declaration with Mail Date Jun. 12, 2020 re: Int'l Appln. No. PCT/US2020/018634. 15 pages.

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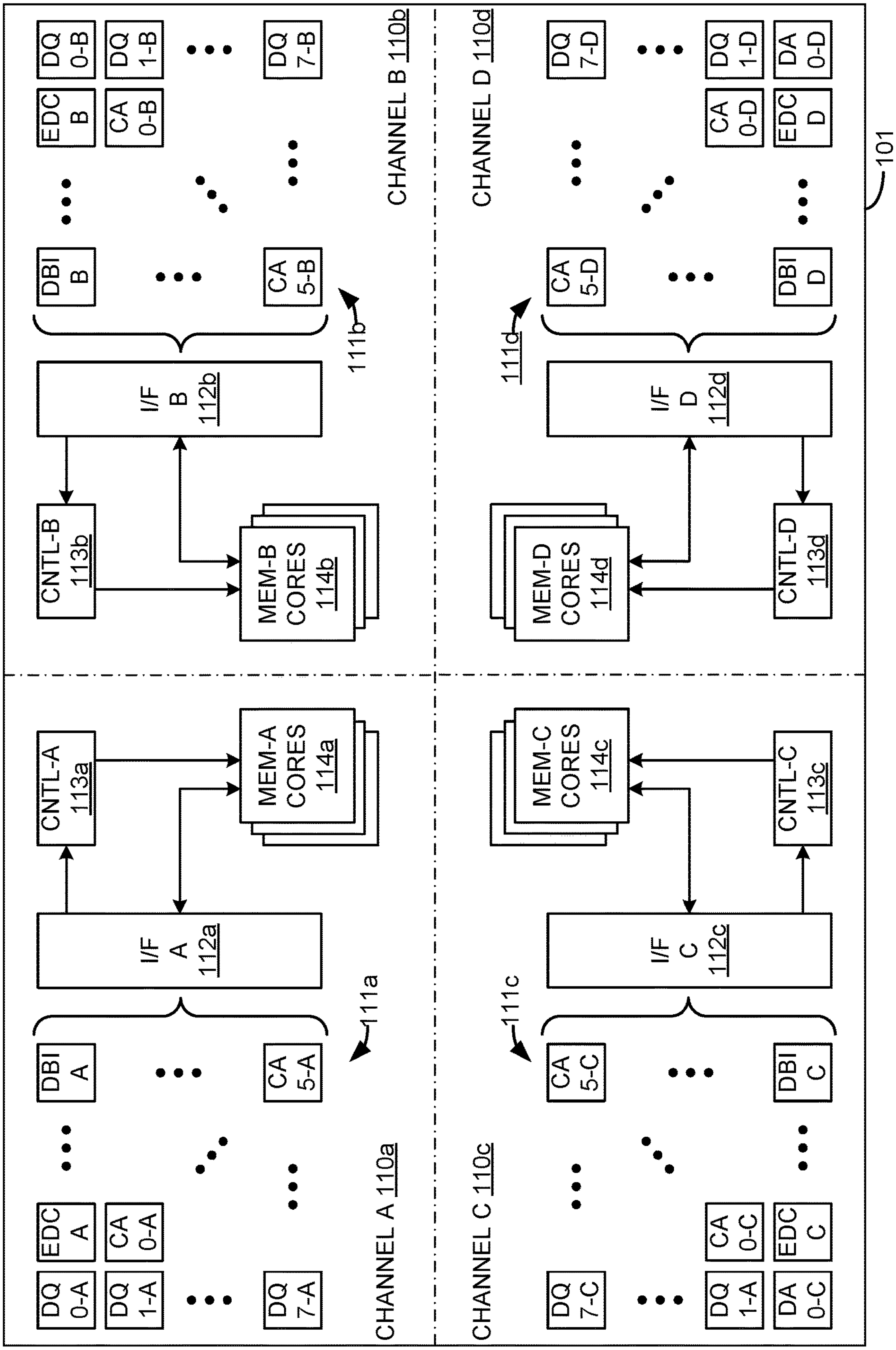
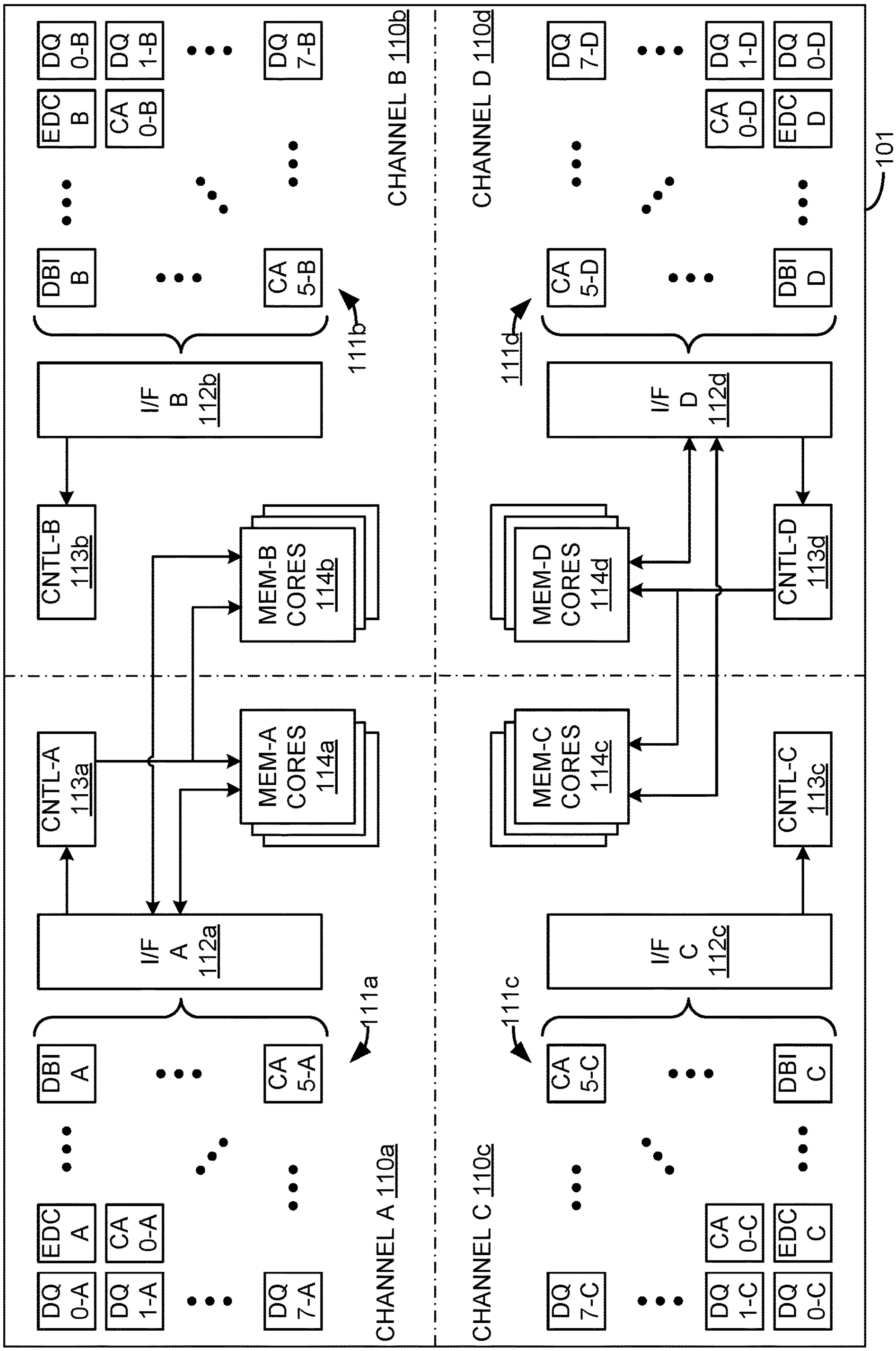


CHANNEL A 110a
CHANNEL B 110b
CHANNEL C 110c
CHANNEL D 110d
DQ 0-A
DQ 1-A
DQ 7-A
EDC A
CA 0-A
DBI A
CA 5-A
111a
I/F A 112a
CNTL-A 113a
MEM-A CORES 114a
DQ 0-B
DQ 1-B
DQ 7-B
EDC B
CA 0-B
DBI B
CA 5-B
111b
I/F B 112b
CNTL-B 113b
MEM-B CORES 114b
DQ 7-C
DQ 1-A
DA 0-C
CA 0-C
EDC C
CA 5-C
DBI C
111c
I/F C 112c
CNTL-C 113c
MEM-C CORES 114c
DQ 7-D
DQ 1-D
DA 0-D
CA 0-D
EDC D
CA 5-D
DBI D
111d
I/F D 112d
CNTL-D 113d
MEM-D CORES 114d
101

FIG. 1A



DQ 0-A
DQ 1-A
DQ 7-A
EDC A
CA 0-A
DBI A
CA 5-A
111a
I/F A 112a
CNTL-A 113a
MEM-A CORES 114a
CHANNEL A 110a
DQ 0-B
DQ 1-B
DQ 7-B
EDC B
CA 0-B
DBI B
CA 5-B
111b
I/F B 112b
CNTL-B 113b
MEM-B CORES 114b
CHANNEL B 110b
DQ 7-C
DQ 1-C
DQ 0-C
CA 0-C
EDC C
CA 5-C
DBI C
111c
I/F C 112c
CNTL-C 113c
MEM-C CORES 114c
CHANNEL C 110c
DQ 7-D
DQ 1-D
DQ 0-D
CA 0-D
EDC D
CA 5-D
DBI D
111d
I/F D 112d
CNTL-D 113d
MEM-D CORES 114d
CHANNEL D 110d
101

FIG. 1B

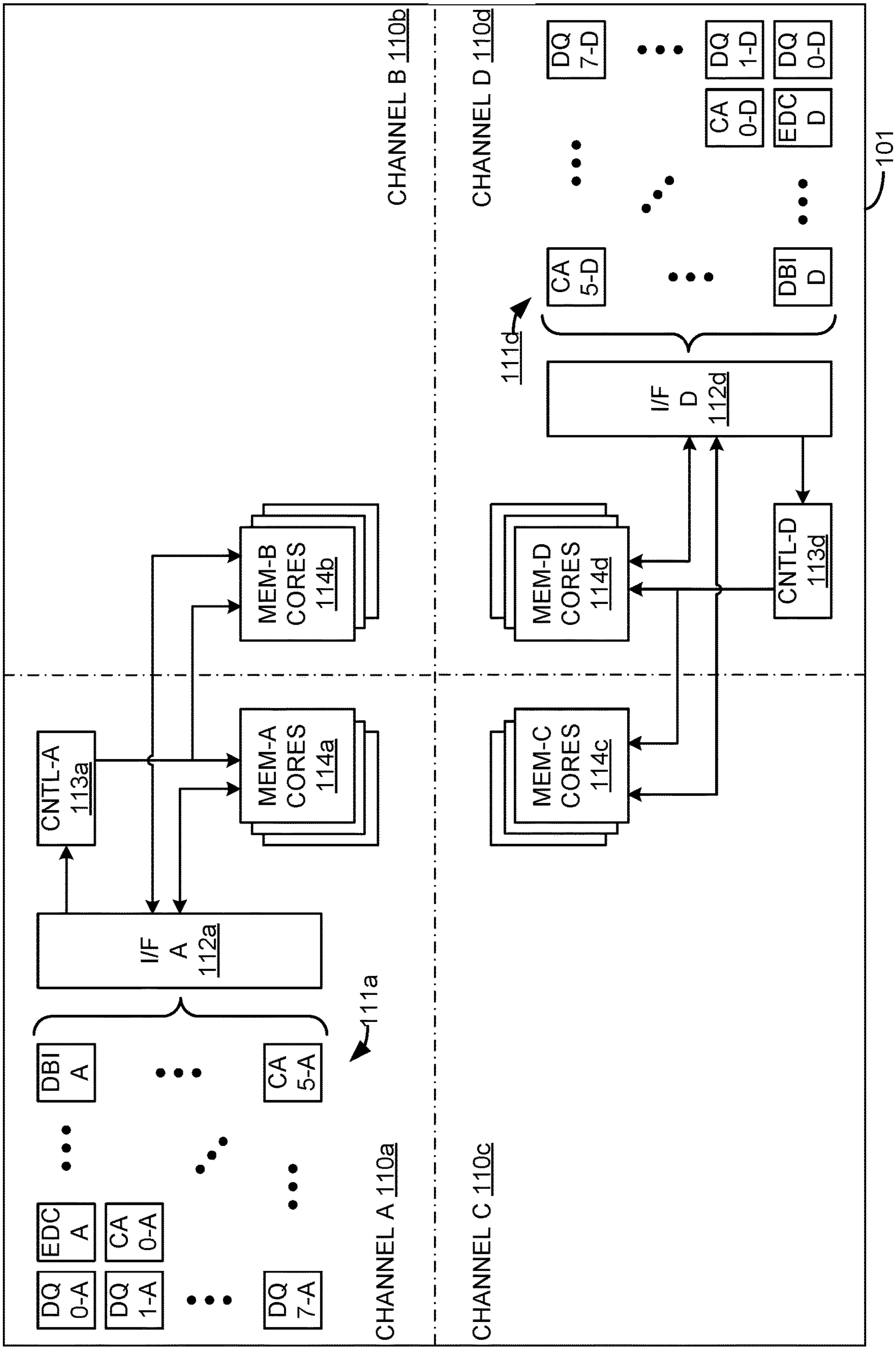

CHANNEL A 110a
CHANNEL B 110b
CHANNEL C 110c
CHANNEL D 110d
DQ 0-A
DQ 1-A
DQ 7-A
EDC A
CA 0-A
DBI A
CA 5-A
111a
I/F A 112a
CNTL-A 113a
MEM-A CORES 114a
MEM-B CORES 114b
MEM-C CORES 114c
MEM-D CORES 114d
CNTL-D 113d
I/F D 112d
111d
CA 5-D
DBI D
CA 0-D
EDC D
DQ 7-D
DQ 1-D
DQ 0-D
101

FIG. 1C

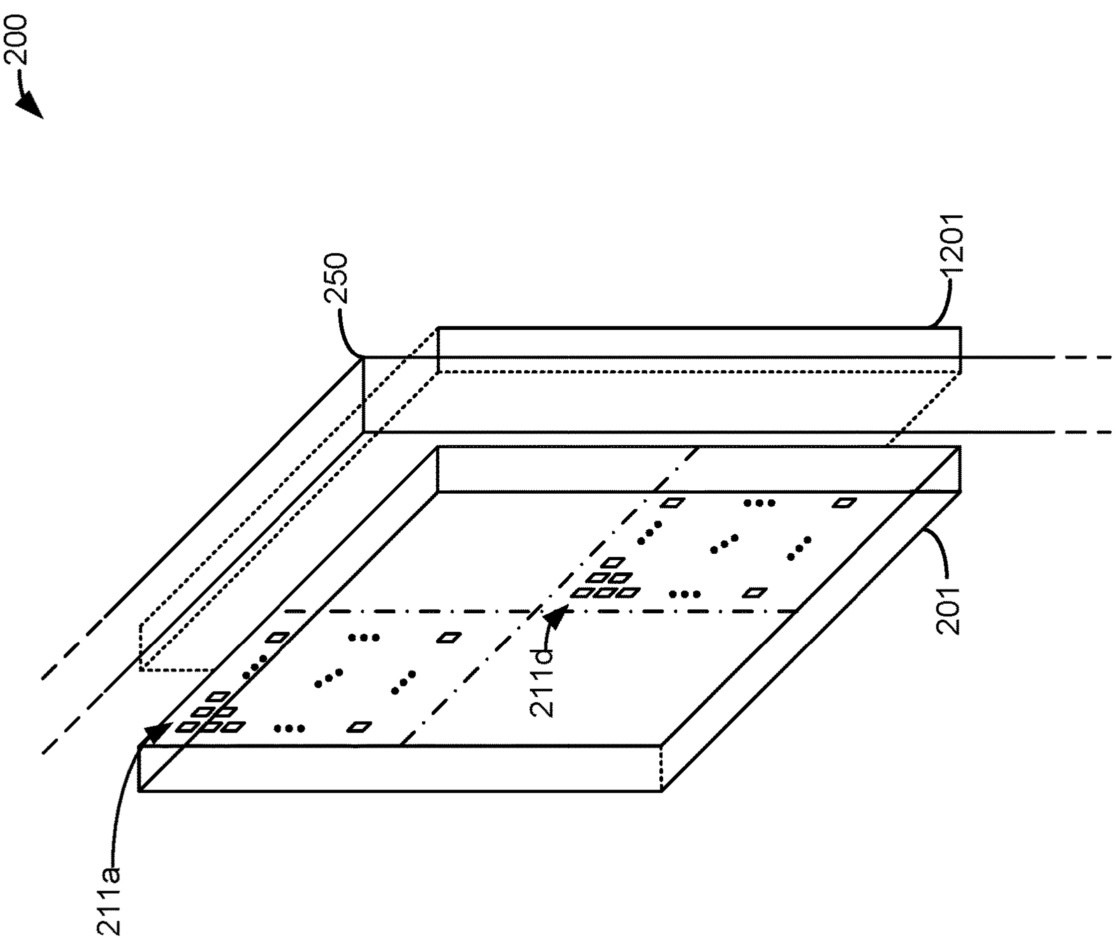


FIG. 2A

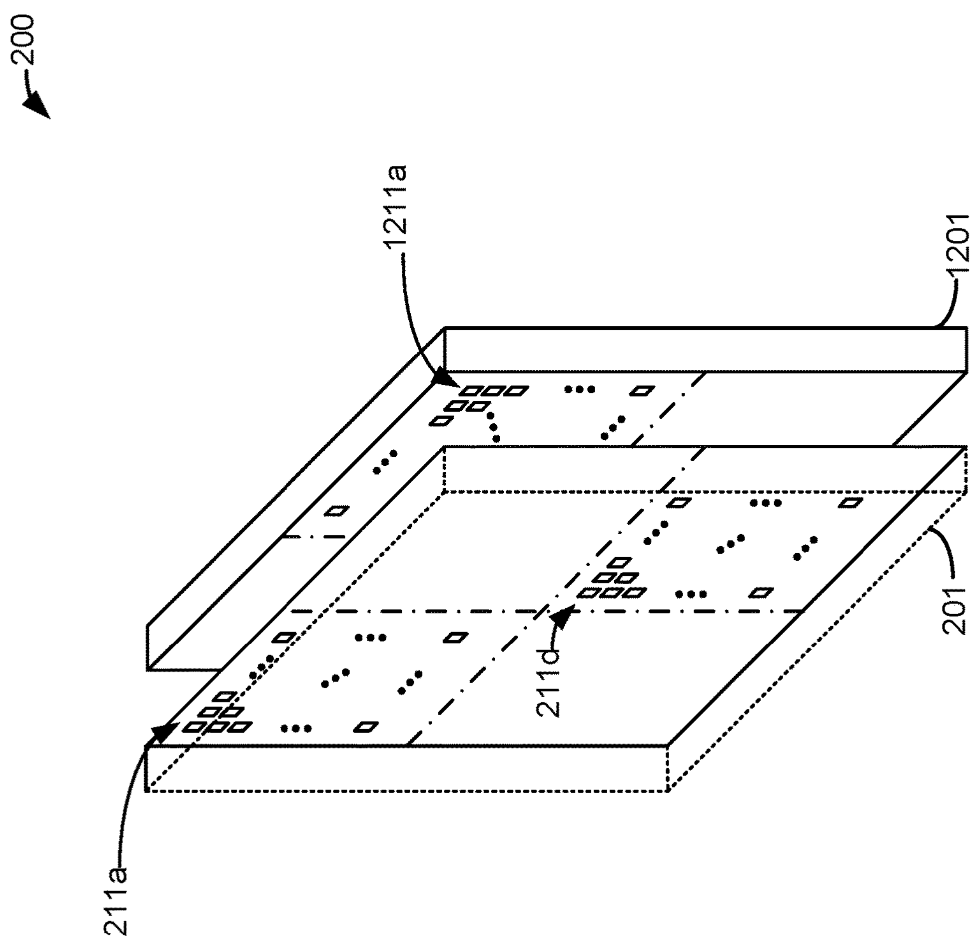


FIG. 2B

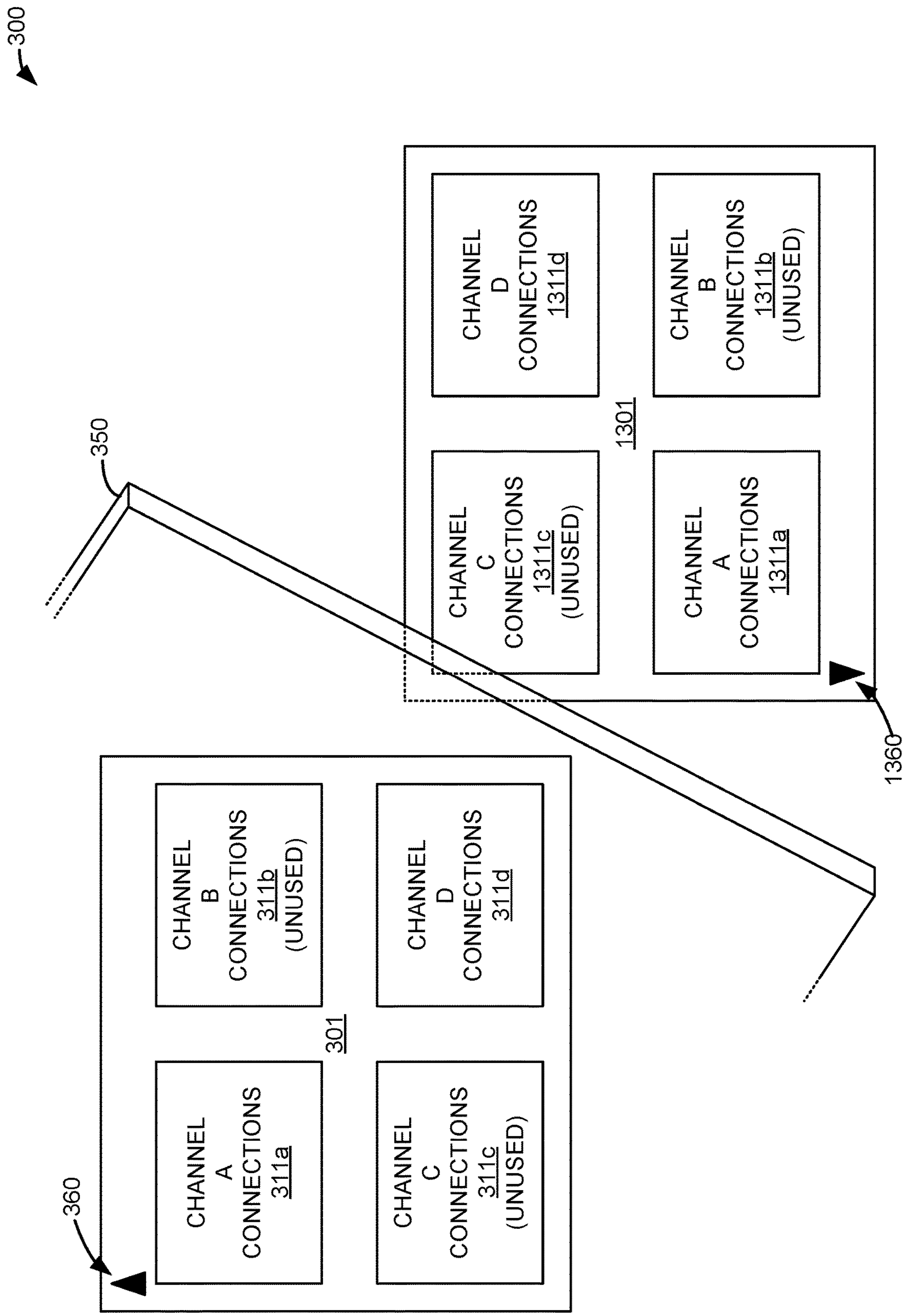

300
350
CHANNEL D CONNECTIONS 1311d
CHANNEL B CONNECTIONS 1311b (UNUSED)
1301
CHANNEL C CONNECTIONS 1311c (UNUSED)
CHANNEL A CONNECTIONS 1311a
1360
CHANNEL B CONNECTIONS 311b (UNUSED)
CHANNEL D CONNECTIONS 311d
301
CHANNEL A CONNECTIONS 311a
CHANNEL C CONNECTIONS 311c (UNUSED)
360

FIG. 3A

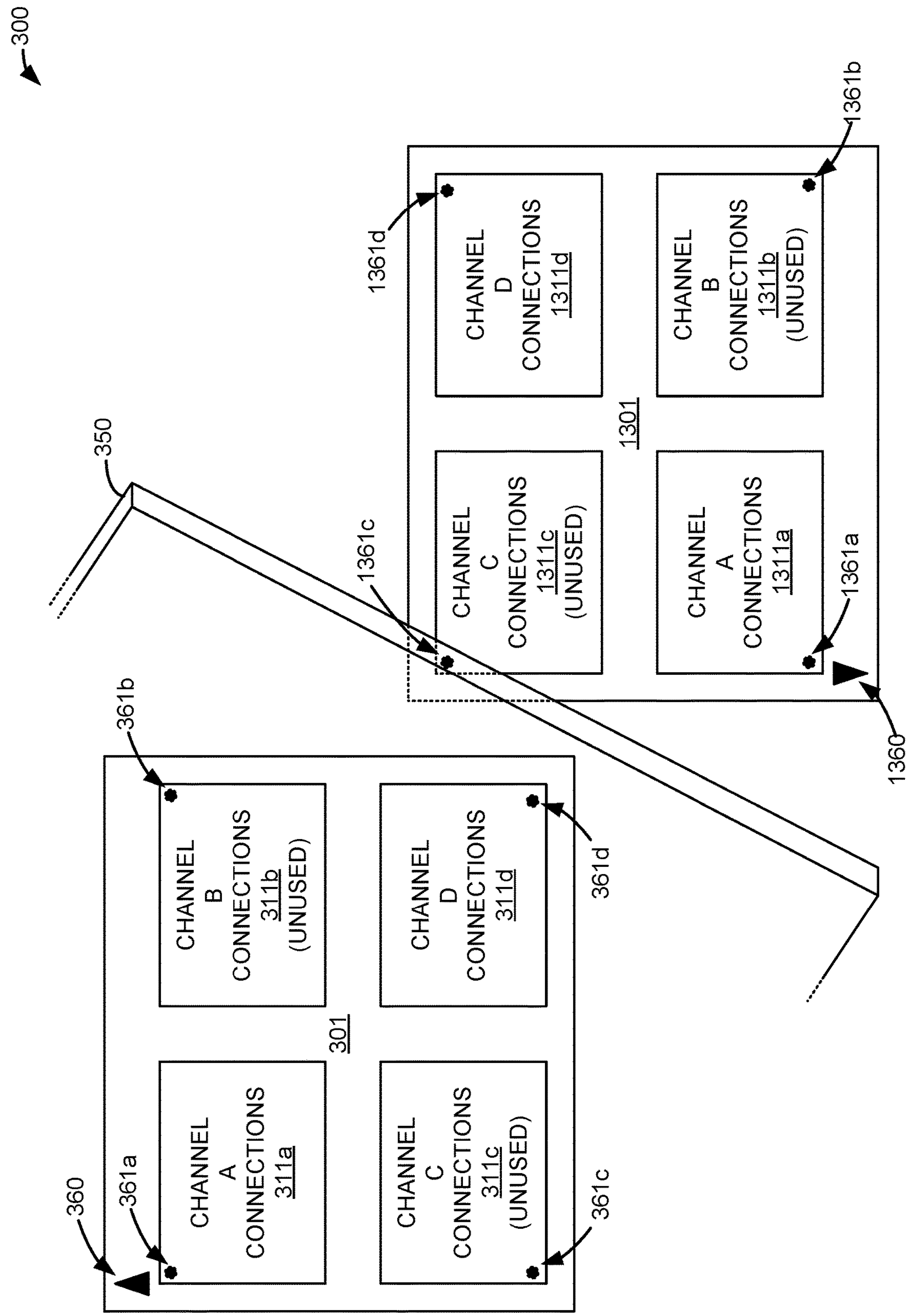

300
350
1301
CHANNEL D CONNECTIONS 1311d
CHANNEL B CONNECTIONS 1311b (UNUSED)
CHANNEL C CONNECTIONS 1311c (UNUSED)
CHANNEL A CONNECTIONS 1311a
1361a
1361b
1361c
1361d
1360
301
CHANNEL B CONNECTIONS 311b (UNUSED)
CHANNEL D CONNECTIONS 311d
CHANNEL A CONNECTIONS 311a
CHANNEL C CONNECTIONS 311c (UNUSED)
361a
361b
361c
361d
360

FIG. 3B

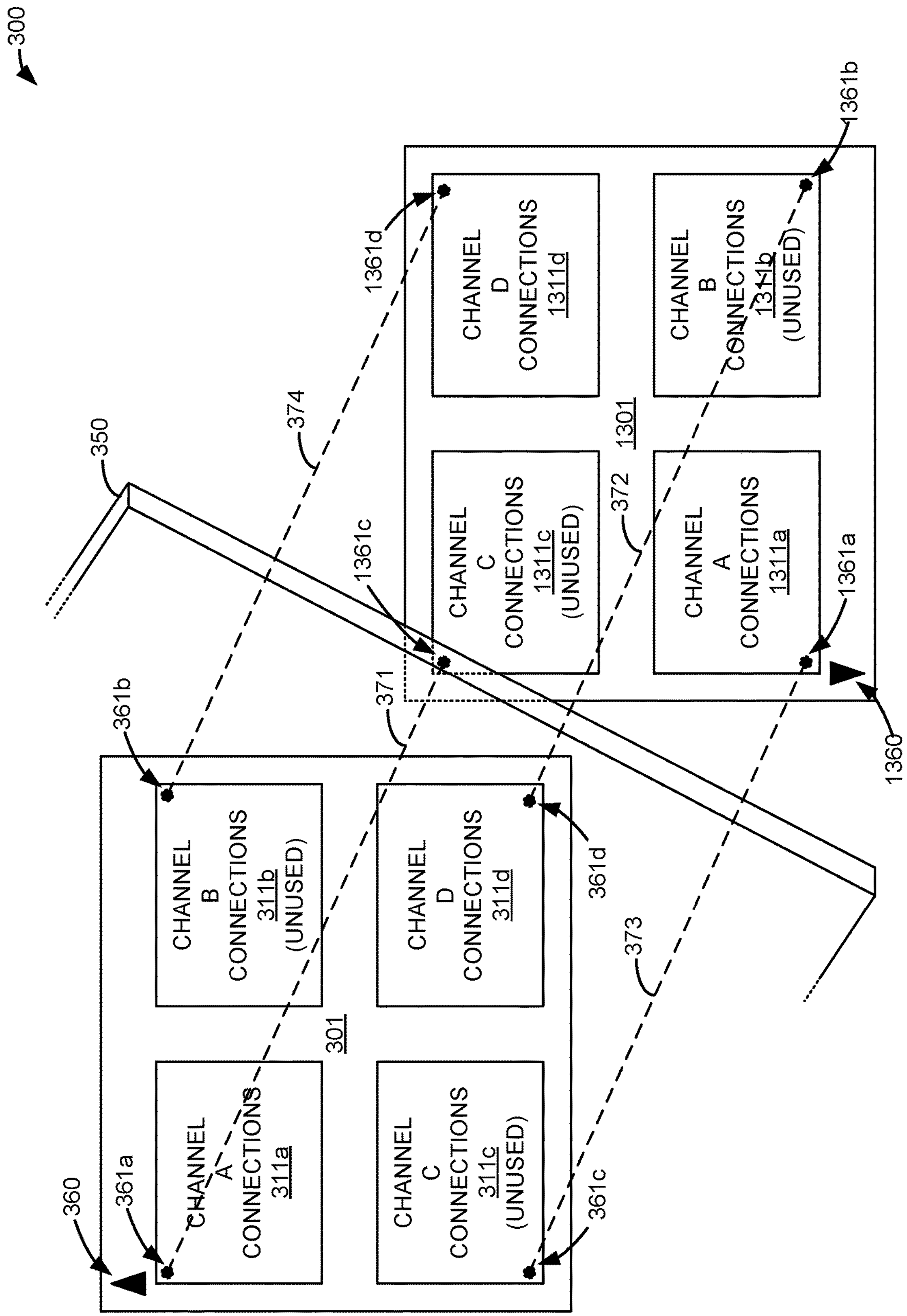

300
350
374
372
371
373
1301
301
1360
360
1361a
1361b
1361c
1361d
361a
361b
361c
361d
CHANNEL D CONNECTIONS 1311d
CHANNEL B CONNECTIONS 1311b (UNUSED)
CHANNEL C CONNECTIONS 1311c (UNUSED)
CHANNEL A CONNECTIONS 1311a
CHANNEL B CONNECTIONS 311b (UNUSED)
CHANNEL D CONNECTIONS 311d
CHANNEL A CONNECTIONS 311a
CHANNEL C CONNECTIONS 311c (UNUSED)

FIG. 3C

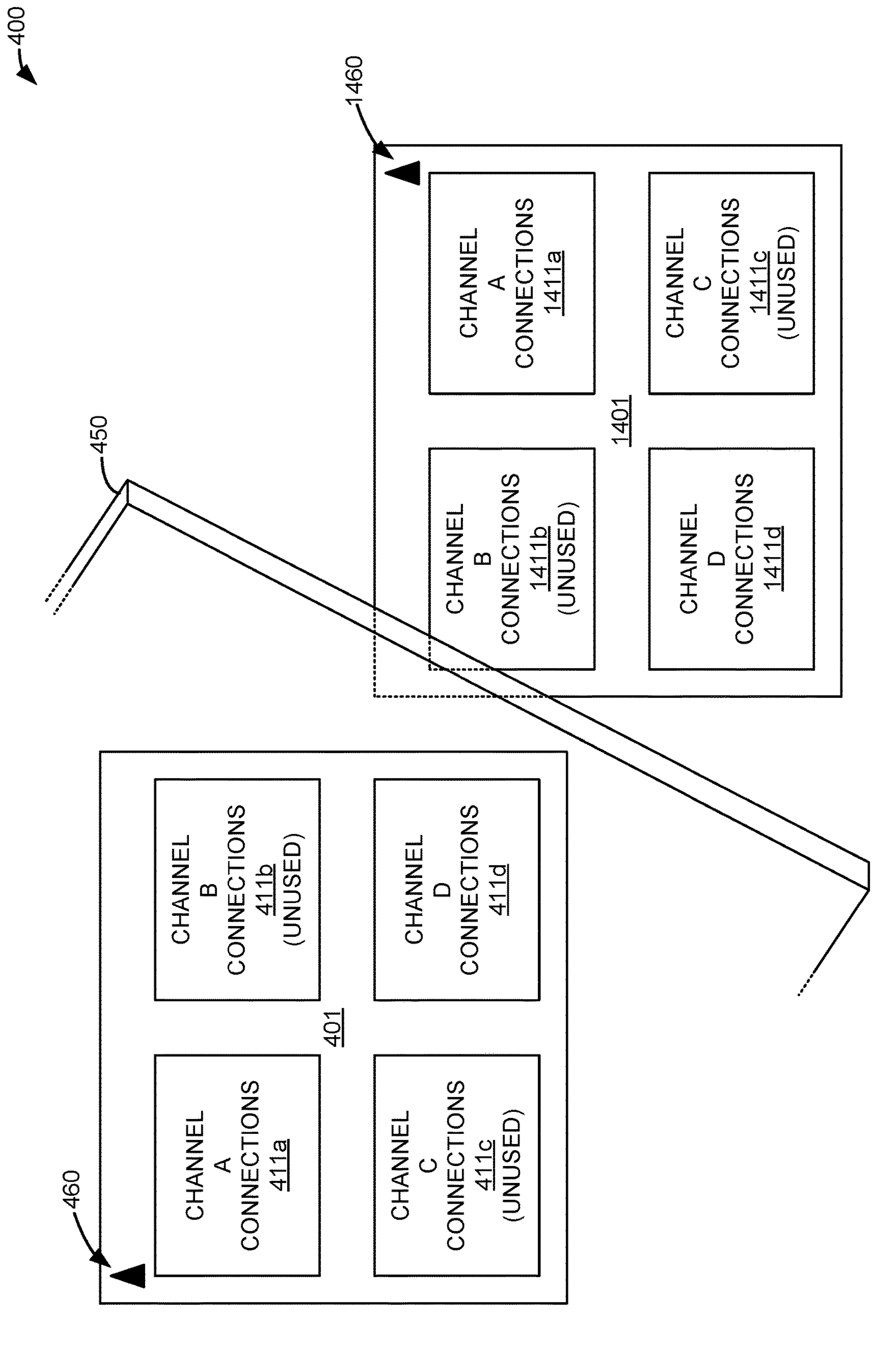

400
1460
450
1401
CHANNEL A CONNECTIONS 1411a
CHANNEL B CONNECTIONS 1411b (UNUSED)
CHANNEL C CONNECTIONS 1411c (UNUSED)
CHANNEL D CONNECTIONS 1411d
460
401
CHANNEL A CONNECTIONS 411a
CHANNEL B CONNECTIONS 411b (UNUSED)
CHANNEL C CONNECTIONS 411c (UNUSED)
CHANNEL D CONNECTIONS 411d

FIG. 4A

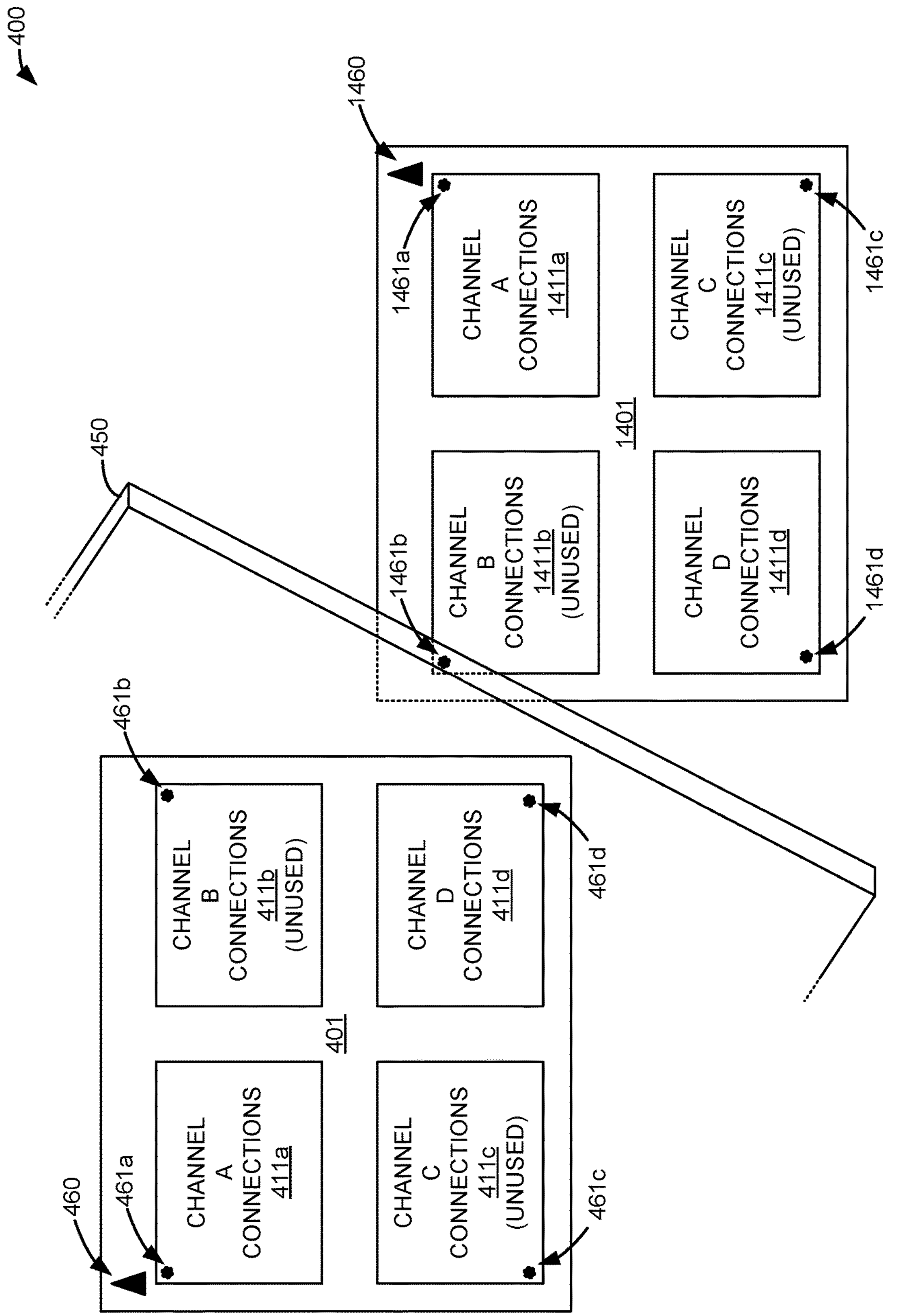

400
1460
1461a
CHANNEL A CONNECTIONS 1411a
CHANNEL C CONNECTIONS 1411c (UNUSED)
1461c
1401
450
1461b
CHANNEL B CONNECTIONS 1411b (UNUSED)
CHANNEL D CONNECTIONS 1411d
1461d
461b
CHANNEL B CONNECTIONS 411b (UNUSED)
CHANNEL D CONNECTIONS 411d
461d
401
460
461a
CHANNEL A CONNECTIONS 411a
CHANNEL C CONNECTIONS 411c (UNUSED)
461c

FIG. 4B

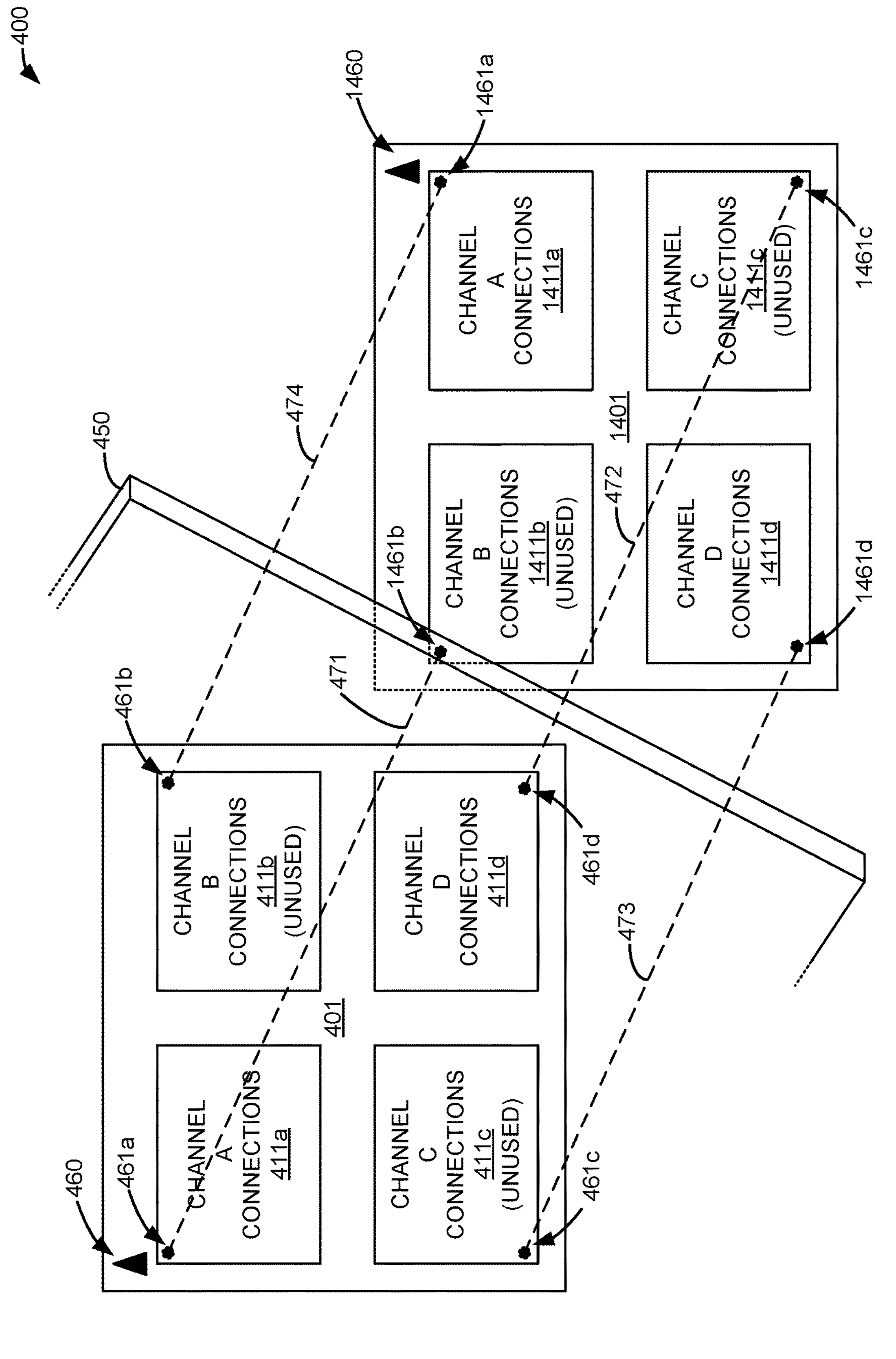

400
1460
1461a
CHANNEL A CONNECTIONS 1411a
CHANNEL C CONNECTIONS 1411c (UNUSED)
1461c
1401
CHANNEL B CONNECTIONS 1411b (UNUSED)
CHANNEL D CONNECTIONS 1411d
1461b
1461d
474
472
450
471
461b
CHANNEL B CONNECTIONS 411b (UNUSED)
CHANNEL D CONNECTIONS 411d
461d
473
401
460
461a
CHANNEL A CONNECTIONS 411a
CHANNEL C CONNECTIONS 411c (UNUSED)
461c

FIG. 4C

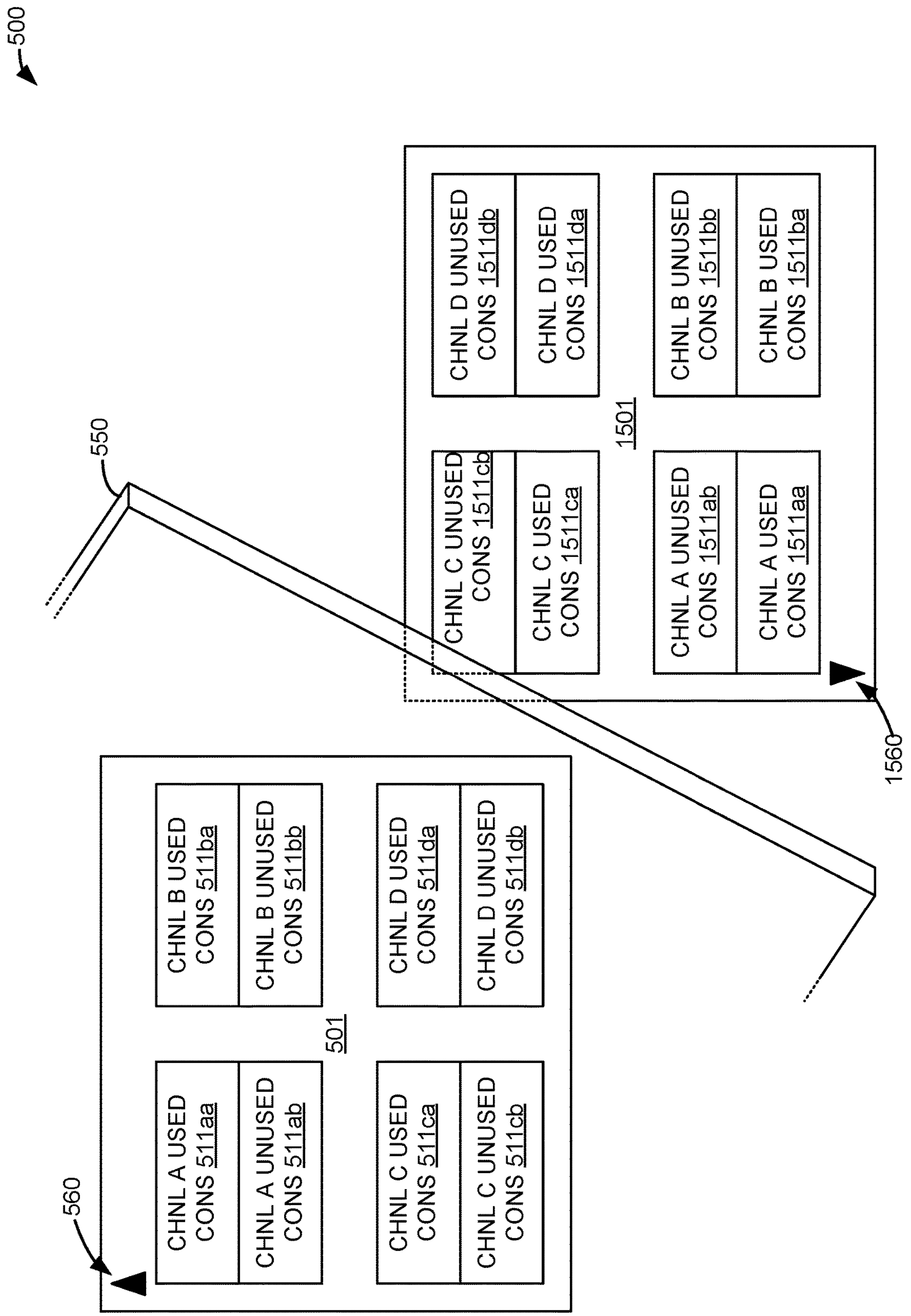

500
550
560
1560
501
1501
CHNL A USED CONS 511aa
CHNL A UNUSED CONS 511ab
CHNL B USED CONS 511ba
CHNL B UNUSED CONS 511bb
CHNL C USED CONS 511ca
CHNL C UNUSED CONS 511cb
CHNL D USED CONS 511da
CHNL D UNUSED CONS 511db
CHNL A USED CONS 1511aa
CHNL A UNUSED CONS 1511ab
CHNL B USED CONS 1511ba
CHNL B UNUSED CONS 1511bb
CHNL C USED CONS 1511ca
CHNL C UNUSED CONS 1511cb
CHNL D USED CONS 1511da
CHNL D UNUSED CONS 1511db

FIG. 5A

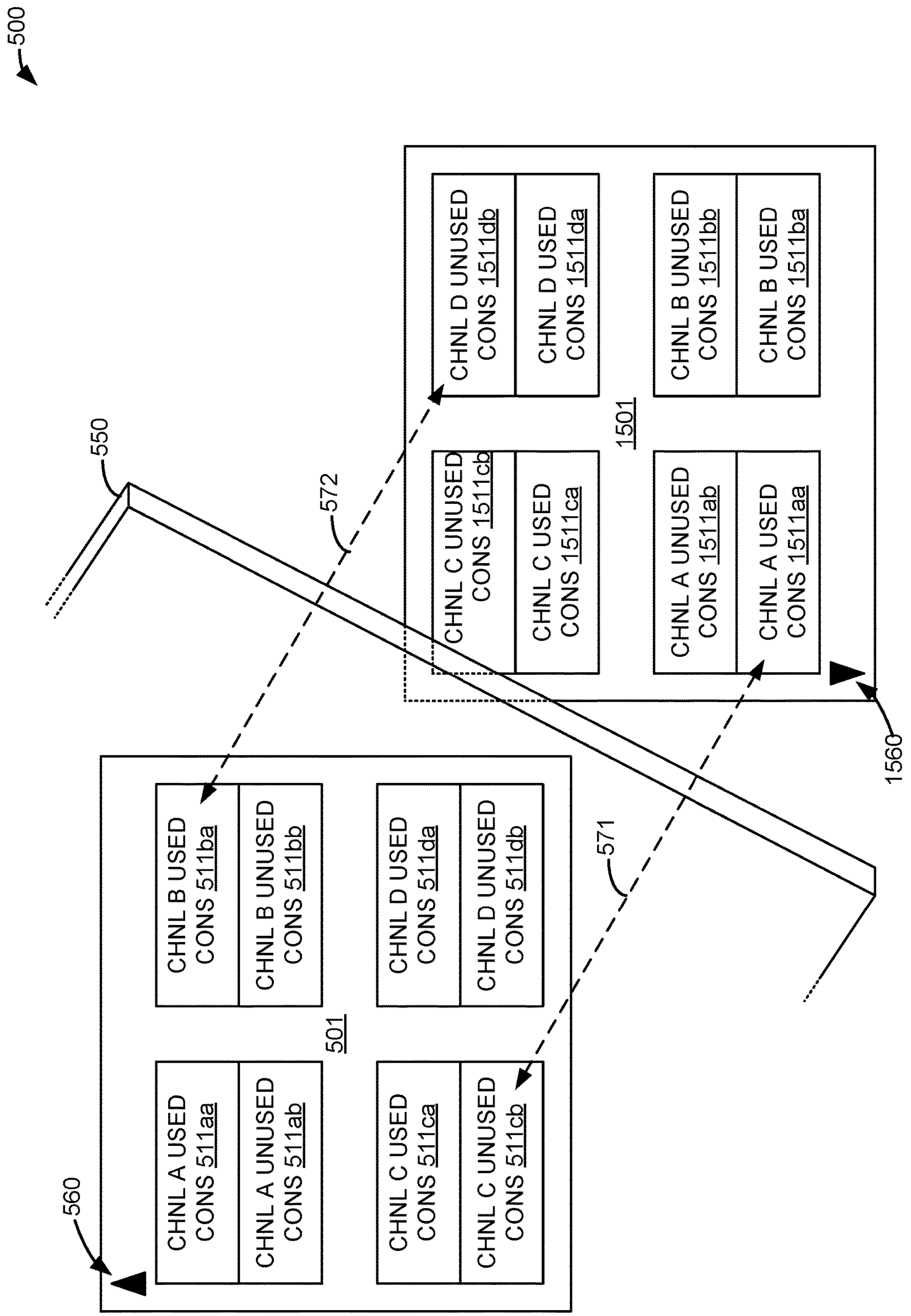

500
550
572
571
560
1560
501
1501
CHNL A USED CONS 511aa
CHNL A UNUSED CONS 511ab
CHNL B USED CONS 511ba
CHNL B UNUSED CONS 511bb
CHNL C USED CONS 511ca
CHNL C UNUSED CONS 511cb
CHNL D USED CONS 511da
CHNL D UNUSED CONS 511db
CHNL A USED CONS 1511aa
CHNL A UNUSED CONS 1511ab
CHNL B USED CONS 1511ba
CHNL B UNUSED CONS 1511bb
CHNL C USED CONS 1511ca
CHNL C UNUSED CONS 1511cb
CHNL D USED CONS 1511da
CHNL D UNUSED CONS 1511db

FIG. 5B

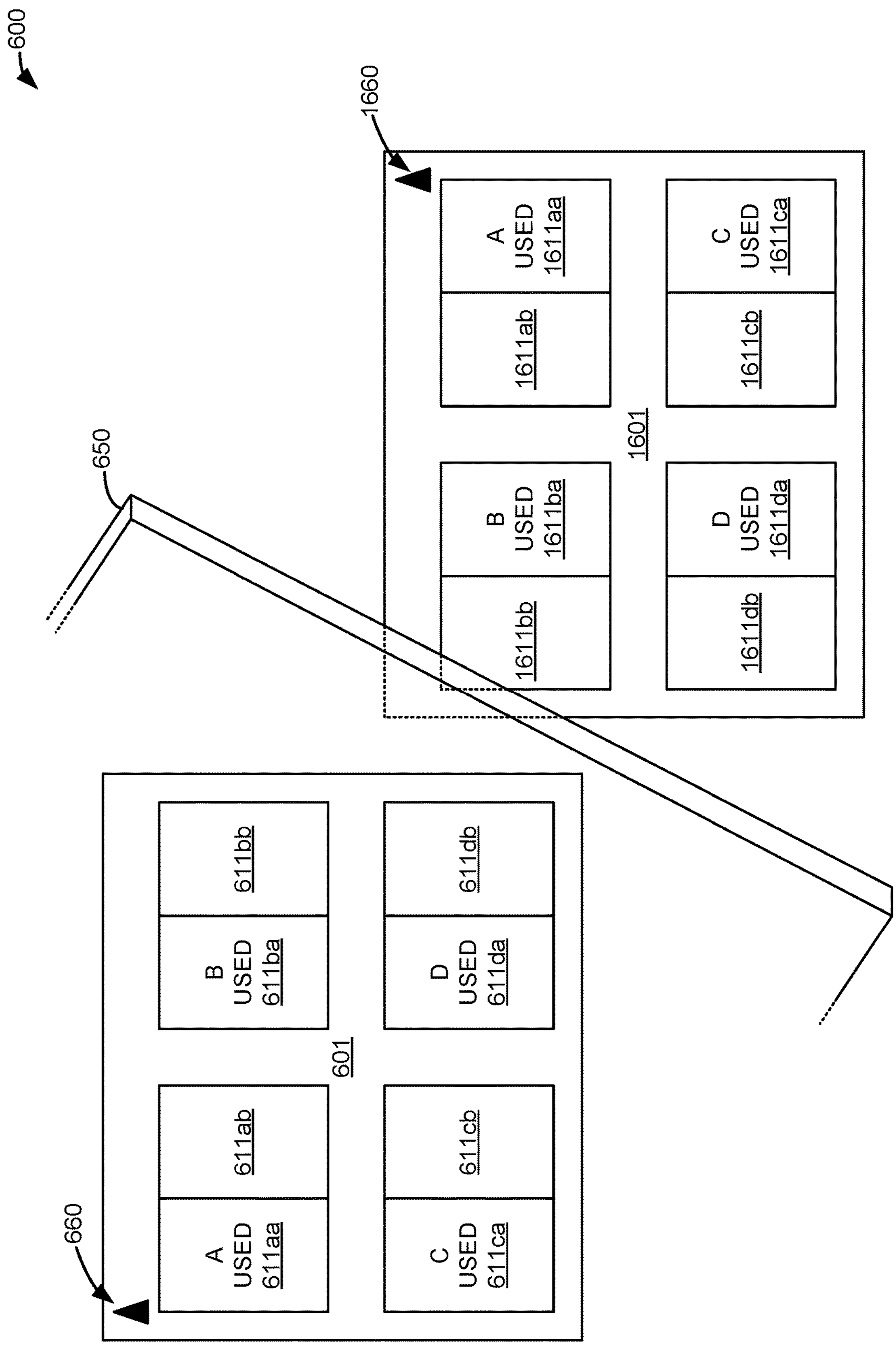

600
1660
A
USED
1611aa
1611ab
C
USED
1611ca
1611cb
1601
B
USED
1611ba
1611bb
D
USED
1611da
1611db
650
611bb
B
USED
611ba
611db
D
USED
611da
601
611ab
A
USED
611aa
611cb
C
USED
611ca
660

FIG. 6A

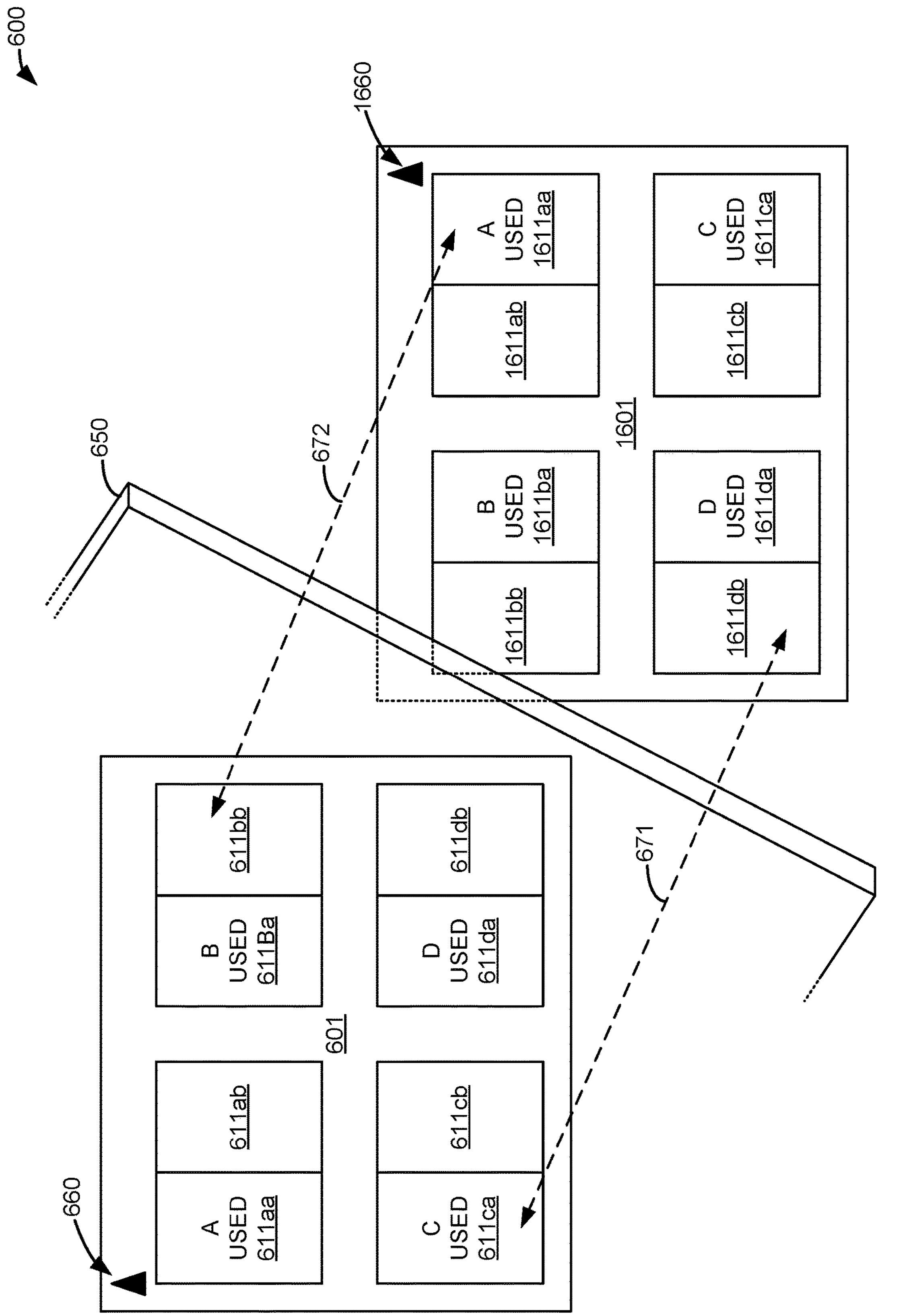

600
1660
650
672
1601
A USED 1611aa
1611ab
C USED 1611ca
1611cb
B USED 1611ba
1611bb
D USED 1611da
1611db
671
601
B USED 611Ba
611bb
D USED 611da
611db
A USED 611aa
611ab
C USED 611ca
611cb
660

FIG. 6B

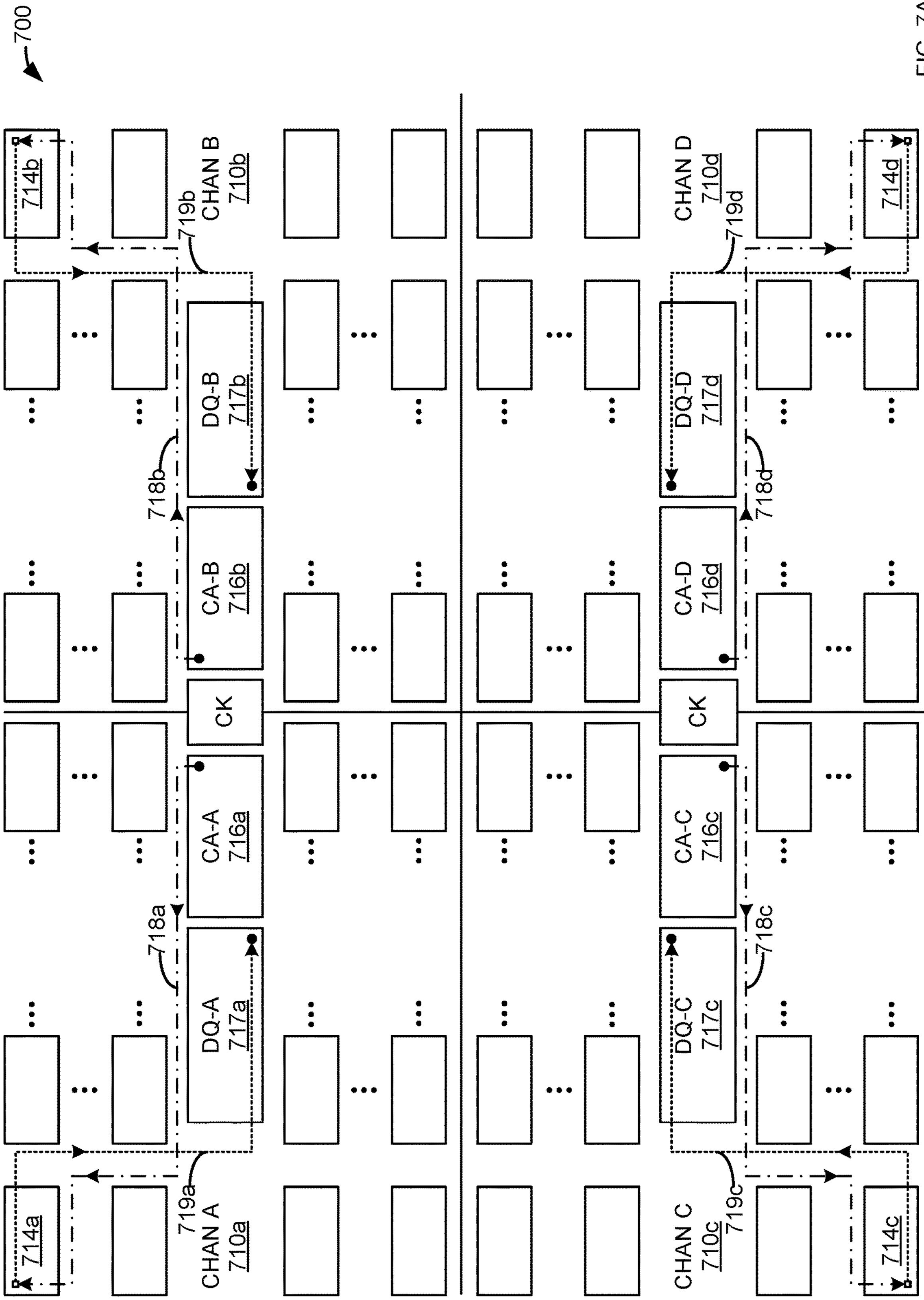

700
CHAN A 710a
CHAN B 710b
CHAN C 710c
CHAN D 710d
714a
714b
714c
714d
719a
719b
719c
719d
718a
718b
718c
718d
DQ-A 717a
DQ-B 717b
DQ-C 717c
DQ-D 717d
CA-A 716a
CA-B 716b
CA-C 716c
CA-D 716d
CK
CK

FIG. 7A

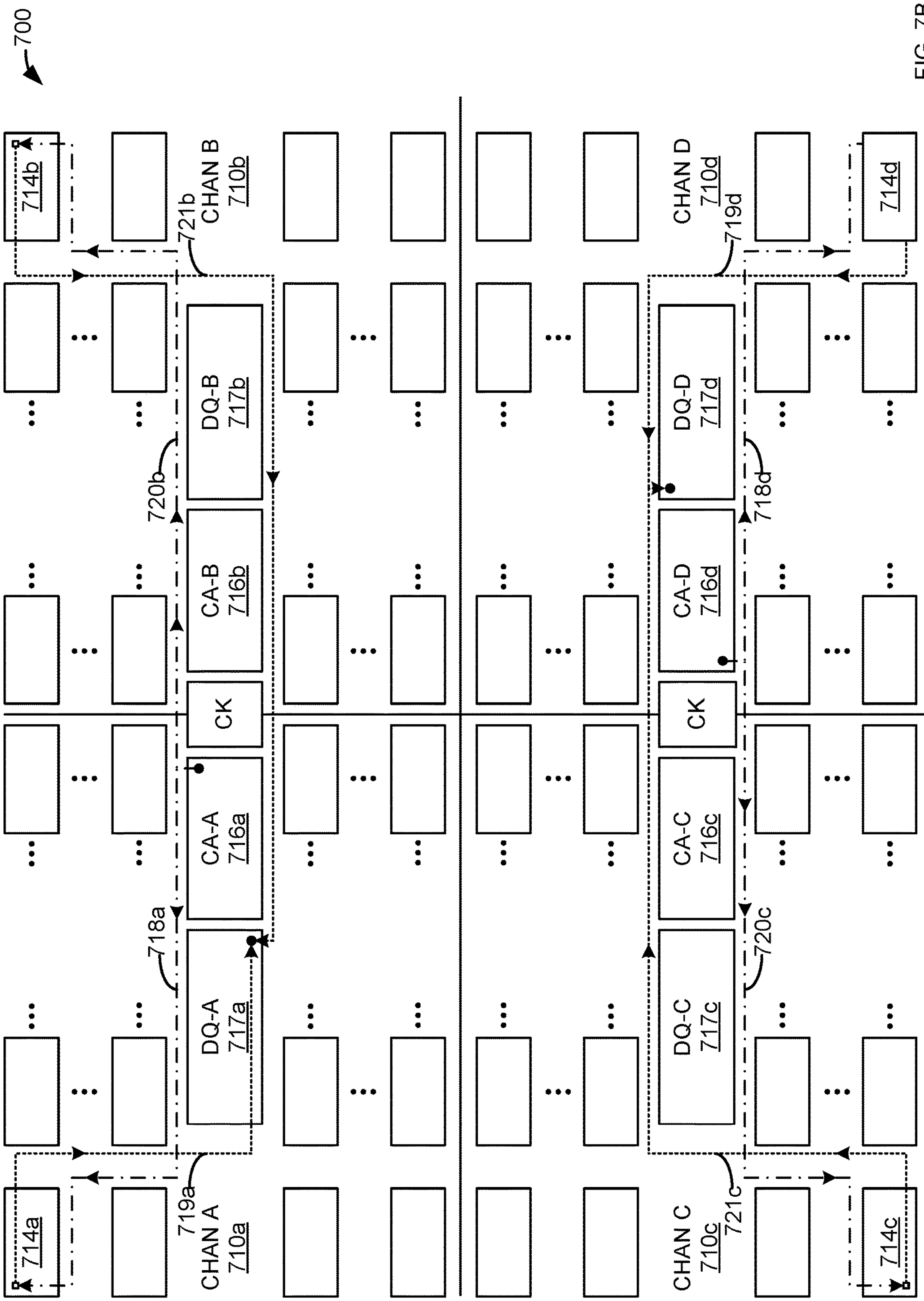

700
714b
CHAN B
710b
721b
DQ-B
717b
720b
CA-B
716b
CK
CA-A
716a
718a
DQ-A
717a
719a
CHAN A
710a
714a
CHAN D
710d
719d
714d
DQ-D
717d
718d
CA-D
716d
CK
CA-C
716c
720c
DQ-C
717c
721c
CHAN C
710c
714c

FIG. 7B

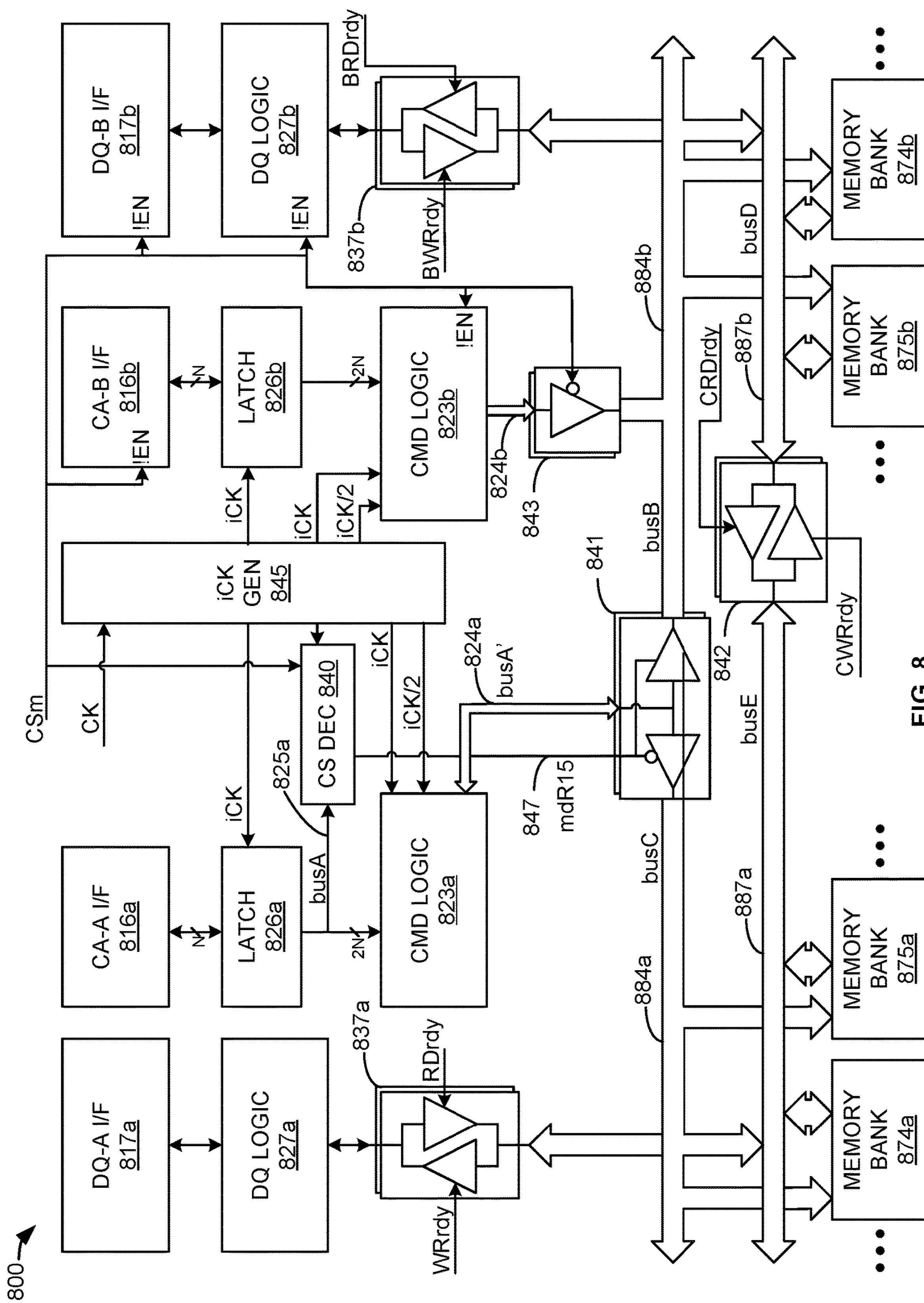
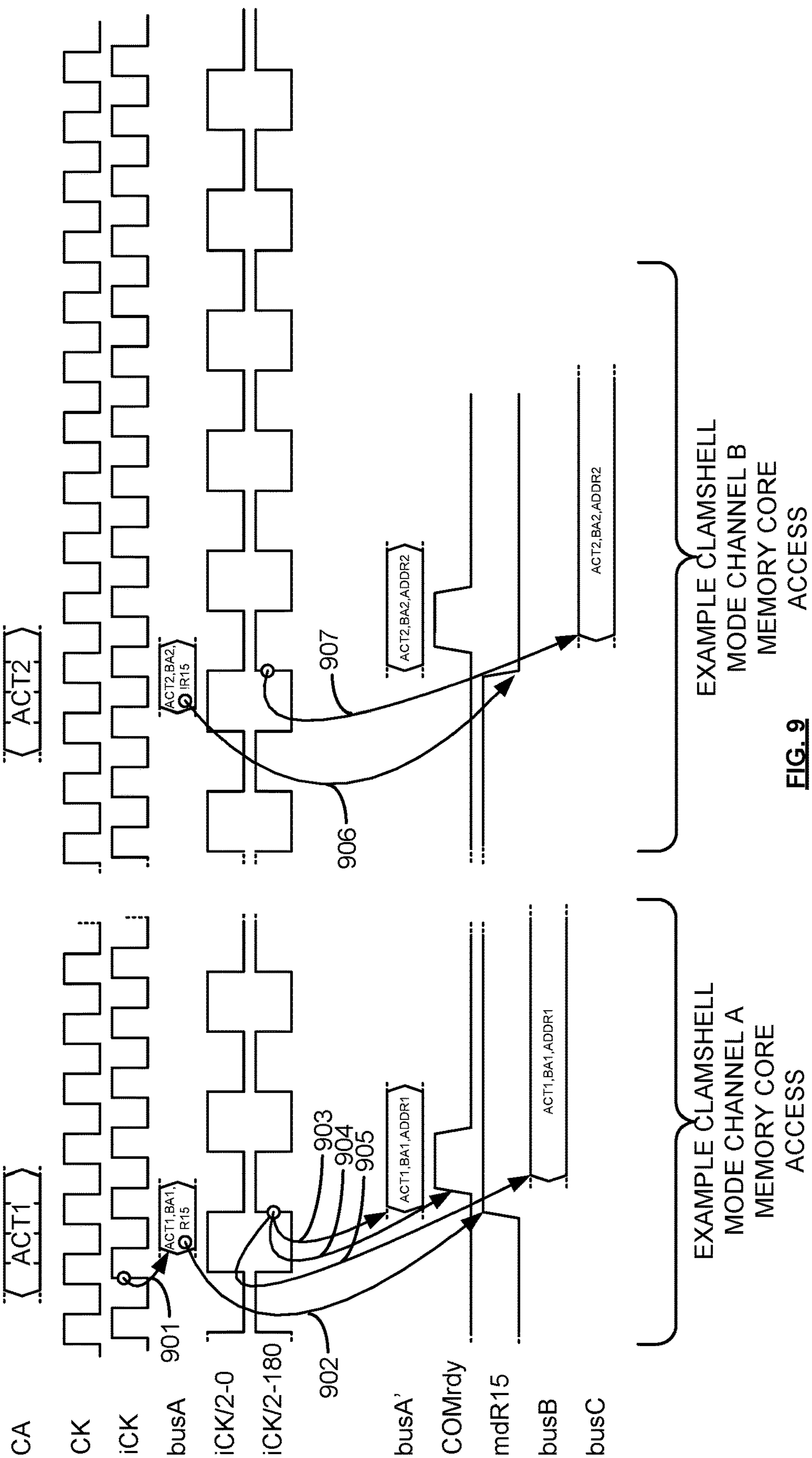

800
DQ-A I/F 817a
DQ LOGIC 827a
CA-A I/F 816a
LATCH 826a
CMD LOGIC 823a
CS DEC 840
iCK GEN 845
CA-B I/F 816b
!EN
LATCH 826b
CMD LOGIC 823b
!EN
DQ-B I/F 817b
!EN
DQ LOGIC 827b
!EN
CSm
CK
iCK
iCK/2
N
2N
busA
busA'
825a
824a
824b
837a
837b
RDrdy
WRrdy
BRDrdy
BWRrdy
841
842
843
847
mdR15
busB
busC
busD
busE
884a
884b
887a
887b
CRDrdy
CWRrdy
MEMORY BANK 874a
MEMORY BANK 875a
MEMORY BANK 875b
MEMORY BANK 874b

FIG. 8



CA
CK
iCK
busA
iCK/2-0
iCK/2-180
busA'
COMrdy
mdR15
busB
busC
ACT1
ACT1,BA1, R15
901
902
903
904
905
ACT1,BA1,ADDR1
ACT1,BA1,ADDR1
ACT2
ACT2,BA2, !R15
906
907
ACT2,BA2,ADDR2
ACT2,BA2,ADDR2
EXAMPLE CLAMSHELL MODE CHANNEL A MEMORY CORE ACCESS
EXAMPLE CLAMSHELL MODE CHANNEL B MEMORY CORE ACCESS

FIG. 9

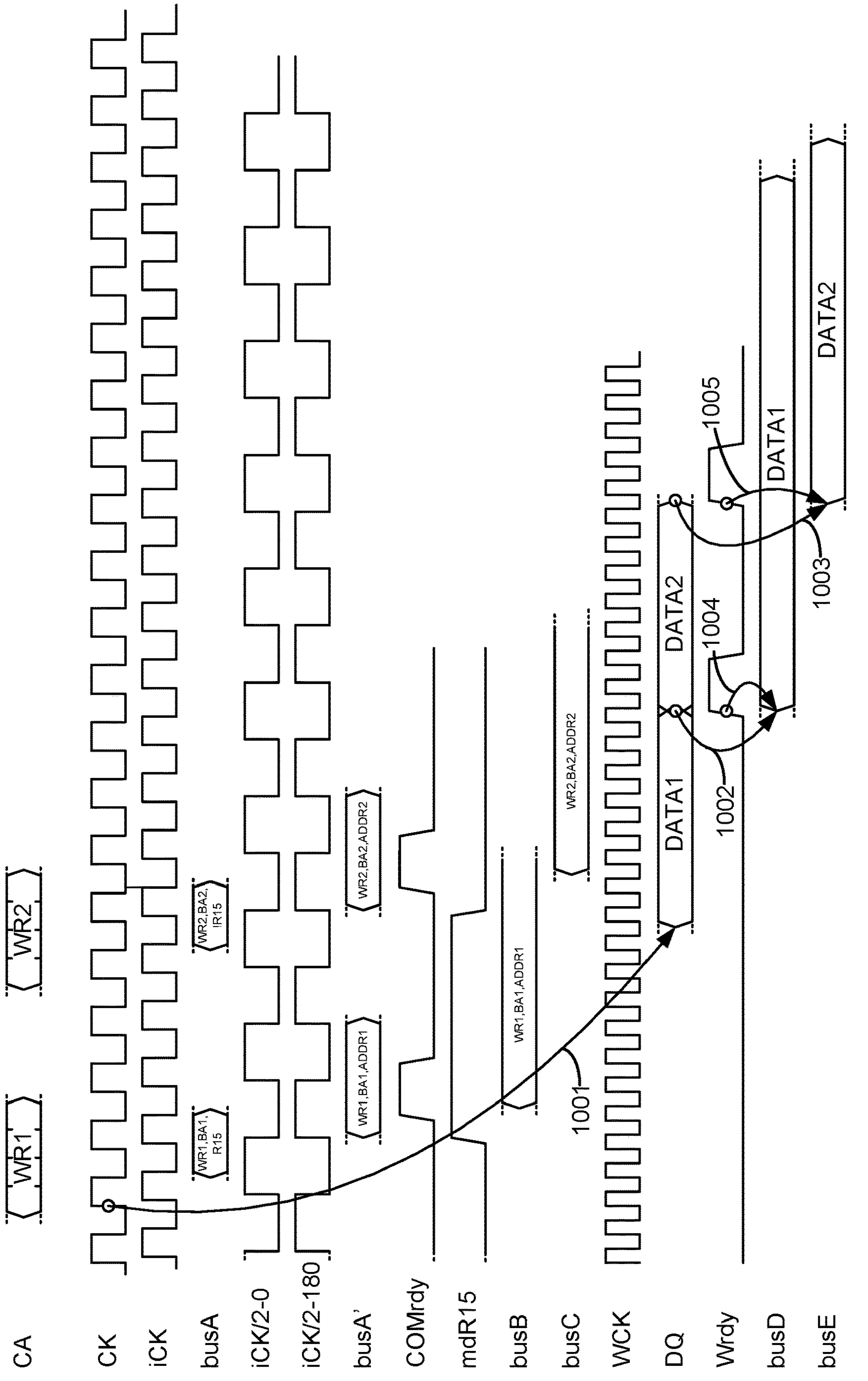

CA
CK
iCK
busA
iCK/2-0
iCK/2-180
busA'
COMrdy
mdR15
busB
busC
WCK
DQ
Wrdy
busD
busE
WR1
WR2
WR1,BA1,
R15
WR2,BA2,
!R15
WR1,BA1,ADDR1
WR2,BA2,ADDR2
WR1,BA1,ADDR1
WR2,BA2,ADDR2
DATA1
DATA2
DATA1
DATA2
1001
1002
1003
1004
1005

FIG. 10

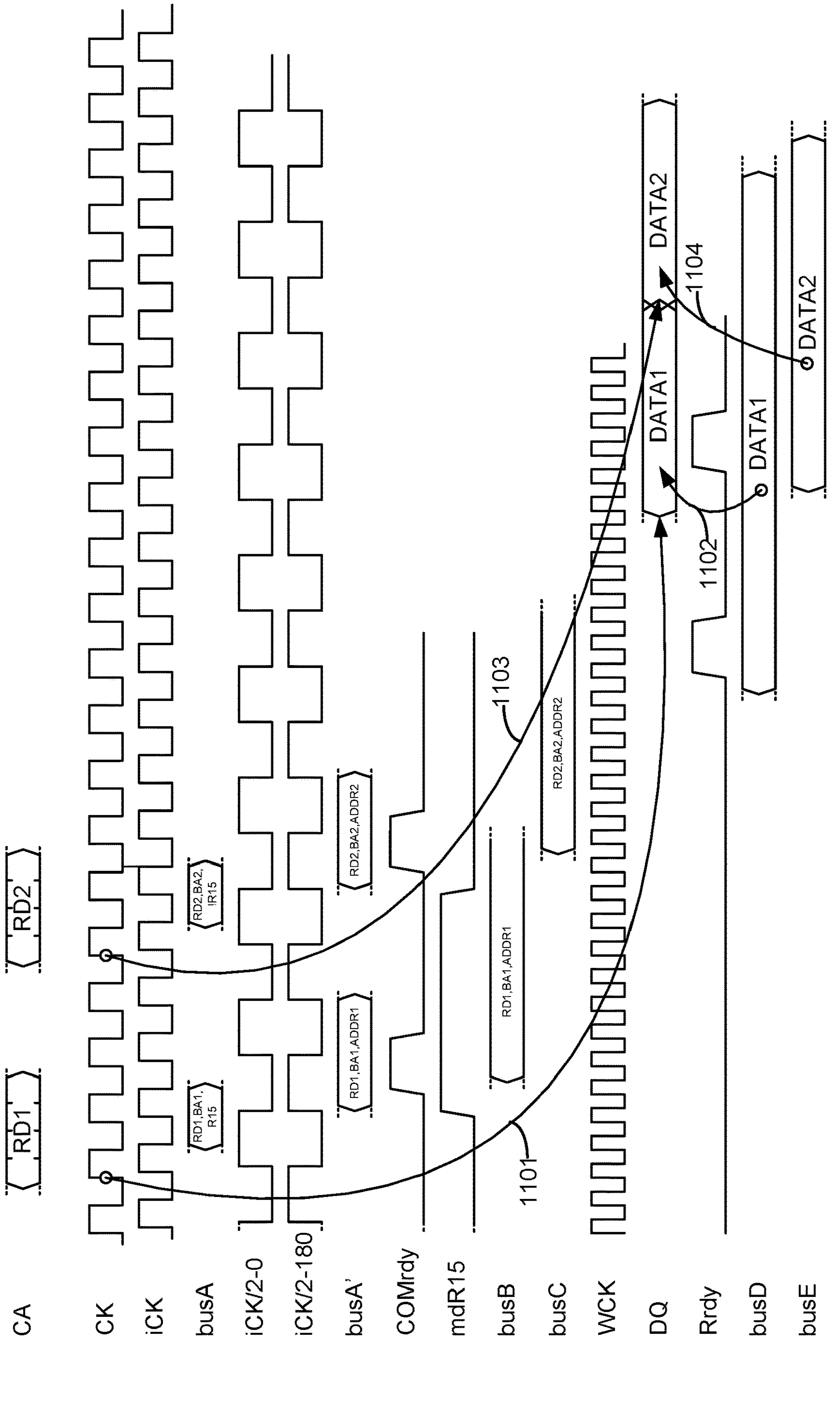

CA
CK
iCK
busA
iCK/2-0
iCK/2-180
busA'
COMrdy
mdR15
busB
busC
WCK
DQ
Rrdy
busD
busE
RD1
RD2
RD1,BA1,R15
RD2,BA2,!R15
RD1,BA1,ADDR1
RD2,BA2,ADDR2
RD1,BA1,ADDR1
RD2,BA2,ADDR2
1101
1102
1103
1104
DATA1
DATA2
DATA1
DATA2

FIG. 11

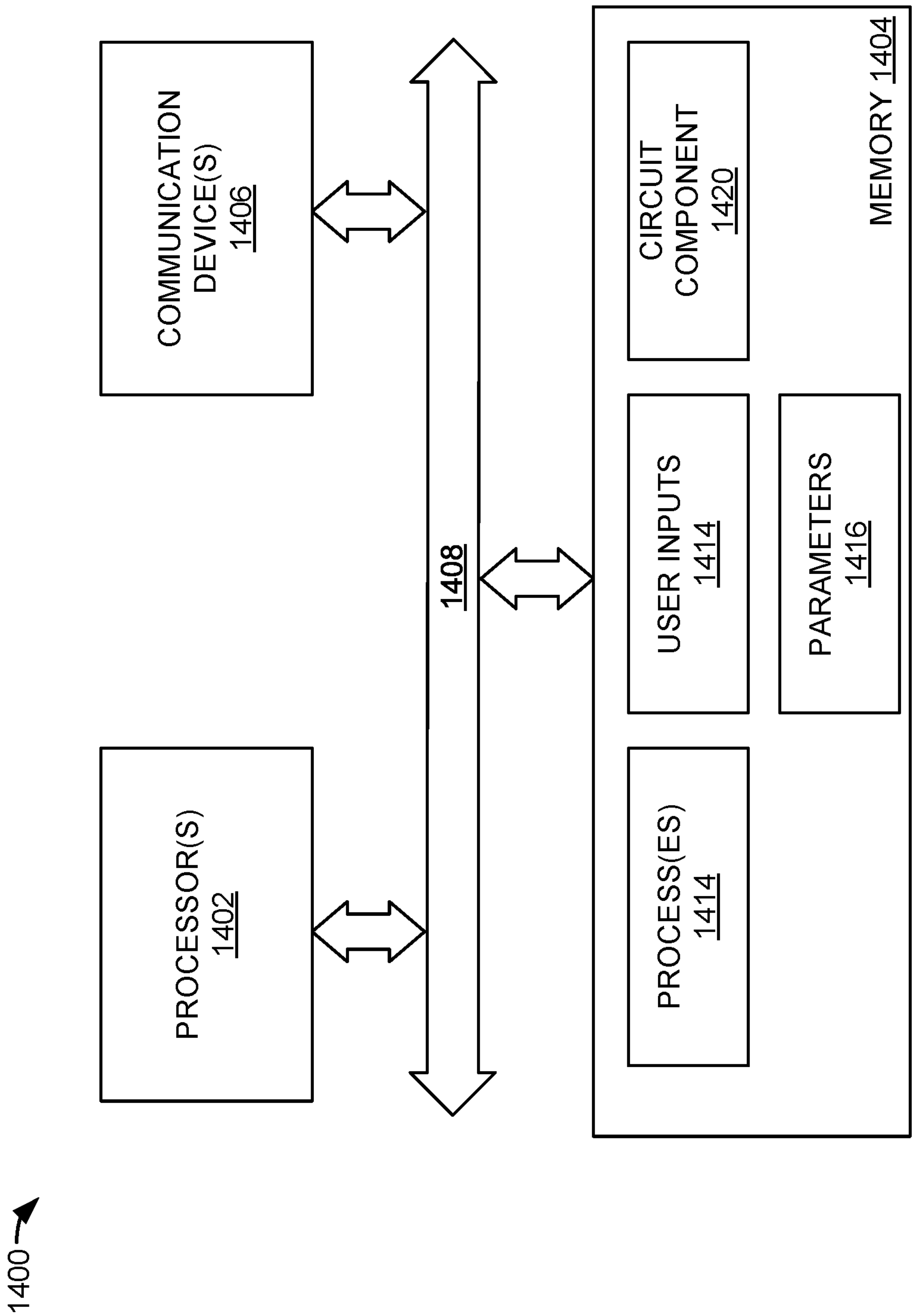

1400
PROCESSOR(S) 1402
COMMUNICATION DEVICE(S) 1406
1408
PROCESS(ES) 1414
USER INPUTS 1414
PARAMETERS 1416
CIRCUIT COMPONENT 1420
MEMORY 1404

FIG. 12

QUAD-CHANNEL DRAM

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a block diagram illustrating a first mode of a quad-channel DRAM.

FIG. 1B is a block diagram illustrating a second mode of a quad-channel DRAM.

FIG. 1C is a block diagram illustrating example active circuitry when the quad-channel DRAM is in the second mode.

FIG. 2A illustrates a first and second quad-channel DRAMs oppositely mounted to utilize dual-channel mode.

FIG. 2B illustrates, with the substrate removed for clarity, the first and second quad-channel DRAMs oppositely mounted to utilize dual-channel mode.

FIG. 3A illustrates a first example device orientation and active channel connections for a pair of oppositely mounted quad-channel DRAMs.

FIG. 3B illustrates a first example device orientation and active channel connection symmetry for a pair of oppositely mounted quad-channel DRAMs.

FIG. 3C illustrates a first example active to inactive channel connection correspondence for a pair of oppositely mounted quad-channel DRAMs.

FIG. 4A illustrates a second example device orientation and active channel connections for a pair of oppositely mounted quad-channel DRAMs.

FIG. 4B illustrates a second example device orientation and active channel connection symmetry for a pair of oppositely mounted quad-channel DRAMs.

FIG. 4C illustrates a second example active to inactive channel connection correspondence for a pair of oppositely mounted quad-channel DRAMs.

FIG. 5A illustrates a first example device orientation using partial per-channel connections for a pair of oppositely mounted quad-channel DRAMs.

FIG. 5B illustrates a first example active to inactive partial per-channel connection correspondence for a pair of oppositely mounted quad-channel DRAMs.

FIG. 6A illustrates a second example device orientation using partial per-channel connections for a pair of oppositely mounted quad-channel DRAMs.

FIG. 6B illustrates a second example active to inactive partial per-channel connection correspondence for a pair of oppositely mounted quad-channel DRAMs.

FIG. 7A illustrates an example floorplan for a quad-channel DRAM and example worst-case latency paths in quad-channel mode.

FIG. 7B illustrates an example floorplan for a quad-channel DRAM and example worst-case latency paths in clamshell (dual-channel) mode.

FIG. 8 illustrates an example block diagram for two channels of a quad-channel DRAM.

FIG. 9 is a timing diagram illustrating example row accesses for a quad-channel DRAM in clamshell (dual-channel) mode.

FIG. 10 is a timing diagram illustrating example write accesses for a quad-channel DRAM in clamshell (dual-channel) mode.

FIG. 11 is a timing diagram illustrating example read accesses for a quad-channel DRAM in clamshell (dual-channel) mode.

FIG. 12 is a block diagram of a processing system.

DETAILED DESCRIPTION OF THE EMBODIMENTS

In an embodiment, a dynamic random access memory (DRAM) device may have four channels (i.e., a quad-

channel device.) In a first mode (i.e., quad-channel mode), these channels may all be operated independently of each other and each access (i.e., read and write) different internal memory cores. In another mode, two of the four channels may be inactivated (i.e., dual-channel mode.) The remaining active channels respectively access the internal memory cores that otherwise would have been accessed by the inactivated channels. In an embodiment, the data width of the active channels is the same as the data width used in the quad-channel mode. The arrangement of the DRAM package balls is such that when two DRAM devices being operated in dual-channel mode, and are aligned on opposite sides of a substrate, they appear, to a memory controller, electrically and logically as a single quad-channel device being operated in four-channel mode. This type of arrangement allows each of the command/address (C/A) and data (DQ) buses, to be routed point-to-point. Since all of the signal routing is point-to-point, branches to reach multiple devices on the same signal line are not required.

Mounting two DRAM devices that are aligned on opposite sides of a substrate, and operating them as a single channel having twice the memory capacity can be referred to as clamshell mode. At high data rates, this type of arrangement requires short signal branches (a.k.a., stubs) off of the main signal traces of the command/address (C/A) bus in order to reach the two devices (rather than no stubs required to reach only one device.) Because these branches are relatively short (e.g., the thickness of the substrate) it is an efficient way of doubling the capacity of a memory channel without excessively loading the C/A signals while also keeping the data bus signals (DQs) point-to-point.

FIG. 1A is a block diagram illustrating a first mode of a quad-channel DRAM. In FIG. 1A, DRAM device **101** is configured with four active channels: channel A **110***a*, channel B **110***b*, channel C **110***c*, and channel d **110***d*. The active circuitry/logic for channel A **110***a* when DRAM device **101** is configured in the four active channel (a.k.a., quad-channel) mode comprises a set of memory cores **114***a* that are accessed via channel A, channel A control circuitry **113***a*, channel A interface (I/F) circuitry **112***a*, and channel A electrical connection points **111***a*. The active circuitry/logic for channel B **110***b* when DRAM device **101** is configured in quad-channel mode comprises a set of memory cores **114***b* that are accessed via channel B, channel B control circuitry **113***b*, channel B interface (I/F) circuitry **112***b*, and channel B electrical connection points **111***b*. The active circuitry/logic for channel C **110***c* when DRAM device **101** is configured in quad-channel mode comprises a set of memory cores **114***c* that are accessed via channel C, channel C control circuitry **113***c*, channel C interface (I/F) circuitry **112***c*, and channel C electrical connection points **111***c*. The active circuitry/logic for channel D **110***d* when DRAM device **101** is configured in quad-channel mode comprises a set of memory cores **114***d* that are accessed via channel D, channel D control circuitry **113***d*, channel D interface (I/F) circuitry **112***d*, and channel D electrical connection points **111***d*.

Channel A electrical connection points **111***a* are operatively coupled to interface circuitry **112***a*. Interface circuitry **112***a* is operatively coupled to control circuitry **113***a* and memory cores **114***a*. Control circuitry **113***a* is operatively coupled to interface **112***a*. Control circuitry **113***a* receives commands and addressed from interface circuitry **112***a*. These commands include commands to access (i.e., read, write, activate, precharge, etc.) one or more of memory cores **114***a*. In the case of a write command, data received at interface **112***a* via electrical connection points **111***a* is coupled to one or more of memory cores **114***a* to be stored. In the case of a read command, the addressed one or more of memory cores **114***a* couples retrieved data to interface **112***a* to be transmitted via electrical connection points **111***a*.

Channel B electrical connection points **111***b* are operatively coupled to interface circuitry **112***b*. Interface circuitry **112***b* is operatively coupled to control circuitry **113***b* and memory cores **114***b*. Control circuitry **113***b* is operatively coupled to interface **112***b*. Control circuitry **113***b* receives commands and addressed from interface circuitry **112***b*. These commands include commands to access one or more of memory cores **114***b*. In the case of a write command, data received at interface **112***b* via electrical connection points **111***b* is coupled to one or more of memory cores **114***b* to be stored. In the case of a read command, the addressed one or more of memory cores **114***b* couples retrieved data to interface **112***b* to be transmitted via electrical connection points **111***b*.

Channel C electrical connection points **111***c* are operatively coupled to interface circuitry **112***c*. Interface circuitry **112***c* is operatively coupled to control circuitry **113***c* and memory cores **114***c*. Control circuitry **113***c* is operatively coupled to interface **112***c*. Control circuitry **113***c* receives commands and addressed from interface circuitry **112***c*. These commands include commands to access one or more of memory cores **114***c*. In the case of a write command, data received at interface **112***c* via electrical connection points **111***c* is coupled to one or more of memory cores **114***c* to be stored. In the case of a read command, the addressed one or more of memory cores **114***c* couples retrieved data to interface **112***c* to be transmitted via electrical connection points **111***c*.

Channel D electrical connection points **111***d* are operatively coupled to interface circuitry **112***d*. Interface circuitry **112***d* is operatively coupled to control circuitry **113***d* and memory cores **114***d*. Control circuitry **113***d* is operatively coupled to interface **112***d*. Control circuitry **113***d* receives commands and addressed from interface circuitry **112***d*. These commands include commands to access one or more of memory cores **114***d*. In the case of a write command, data received at interface **112***d* via electrical connection points **111***d* is coupled to one or more of memory cores **114***d* to be stored. In the case of a read command, the addressed one or more of memory cores **114***d* couples retrieved data to interface **112***d* to be transmitted via electrical connection points **111***d*.

Channel A-D electrical connection points **111***a*-**111***d* may correspond to pads, package pins, solder balls, or other means of electrically connecting a DRAM integrated circuit to a substrate, such as a printed circuit board. Memory cores **114***a*-**114***d* may comprise dynamic random access memory (DRAM) array or other type of memory arrays, for example, static random access memory (SRAM) array, or non-volatile memory arrays such as flash.

It should be understood from the foregoing that, in quad-channel mode, each of channels A-D **110***a*-**110***d* comprise enough active circuitry and electrical connection points **111***a*-**111***d* to each operate independently of each other channel A-D **110***a*-**110***d*. Each of channels A-D **110***a*-**110***d* in quad-channel mode operate the command, address, and data transfer functions of their respective channel A-D **110***a*-**110***d* independently of the other channels A-D **110***a*-**110***d*.

In an embodiment, each of channels A-D **110***a*-**110***d* includes nine (9) bidirectional data (DQ) lines (eight data lines and one for error-detection, correction, and/or parity.) In another embodiment, each of channels A-D **110***a*-**110***d* includes eight (8) bidirectional data (DQ) lines. Each of channels A-D **110***a*-**110***d* includes a C/A bus. Each of the channel A-D **110***a*-**110***d* C/A busses include separate and independent, from the other C/A busses, data bus inversion (DBI), error detection (EDC), and timing signals (e.g., write strobes).

In an embodiment, each channel A-D **110***a*-**110***d* may each receive one or more independent clocking signal(s) (not shown in FIGS. 1A-1B) that drive the operations of that respective channel A-D **110***a*-**110***d*. In another embodiment, channels A-D **110***a*-**110***d* may all share the one or more clock signal(s). Even though channels A-D **110***a*-**110***d* function independently, their operations are driven by, and aligned to, the common clocking signal(s). In another embodiment, two channels A-D **110***a*-**110***d* may share common clocking signal(s). For example, channel A **110***a* and channel B **110***b* may share a clocking signal while channel C **110***c* and channel D **110***d* share another clocking signal.

FIG. **1**B is a block diagram illustrating a second mode of a quad-channel DRAM. In FIG. **1**B, DRAM device **101** is configured with two active channels: channel A **110***a*, and channel D **110***d*. Thus, in this dual-channel mode, channel B electrical connection points **111***b*, channel B interface circuitry **112***b*, and channel B control circuitry **113***b* are inactivated, unused, and/or powered off. Likewise, in this dual-channel mode, channel C electrical connection points **111***c*, channel C interface circuitry **112***c*, and channel B control circuitry **113***c* are inactivated, unused, and/or powered off.

However, in the dual-channel modes, memory cores **114***b* and memory cores **114***c* are configured to be accessed via the remaining two active channels. For example, memory cores **114***b* may be accessed via channel A **110***a*, and memory cores **114***c* may be accessed via channel D **110***d*. Memory cores **114***b* being able to be accessed via channel A **110***a* in the dual-channel mode is illustrated in FIG. **1**B by the arrows from channel A interface **112***a* and channel A control circuitry **113***a* to and from memory cores **114***b* (which in quad channel mode are accessed via channel B **110***b*.) Memory cores **114***c* being able to be accessed via channel D **110***d* in the dual-channel mode is illustrated in FIG. **1**B by the arrows from channel D interface **112***d* and channel D control circuitry **113***d* to and from memory cores **114***c* (which in quad channel mode would be accessed via channel C **110***c*.) Thus, in an embodiment, the amount of memory accessible via channel A **110***a* is increased in the dual-channel mode (e.g., doubled if memory cores **114***a* and **114***b* each have the same capacity.) Likewise, the amount of memory accessible via channel D **110***d* is increased in the dual-channel mode (e.g., doubled if memory cores **114***c* and **114***d* each have the same capacity.)

As described herein, in an embodiment, sets of two channels A-D **110***a*-**110***d* may share common clocking signal(s). In an embodiment, the pairs of channels that share common clocking signals include one channel (e.g., channel A) that is active in the second mode and one channel that is inactive in the second mode (e.g., channel B).

FIG. **1**C is a block diagram illustrating example active circuitry when the quad-channel DRAM is in the second mode. In FIG. **3**, the inactive, unused, and/or powered down circuitry is not shown. The circuitry that is active in the dual-channel mode is shown. Thus, in FIG. **1**C, channel A electrical connection points **111***a*, channel A interface circuitry **112***a*, control circuitry **113***a*, memory cores **114***a*, memory cores **114***b* are shown. FIG. **1**C also illustrates the active couplings in dual-channel mode between: interface circuitry **112***a* and control circuitry **113***a*; control circuitry **113***a* and memory cores **114***a*; control circuitry **113***a* and memory cores **114***b*; memory cores **114***a* and interface circuitry **112***a*; and memory cores **114***b* and interface circuitry **112***a*. Likewise, in FIG. **1**C, channel D electrical connection points **111***d*, channel D interface circuitry **112***d*, control circuitry **113***d*, memory cores **114***d*, memory cores **114***c* are shown. FIG. **1**C also illustrates the active couplings in dual-channel mode between: interface circuitry **112***d* and control circuitry **113***d*; control circuitry **113***d* and memory cores **114***d*; control circuitry **113***d* and memory cores **114***c*; memory cores **114***d* and interface circuitry **112***d*; and memory cores **114***c* and interface circuitry **112***d*.

FIG. **2**A illustrates a first and second quad-channel DRAM oppositely mounted to utilize dual-channel mode. In FIGS. **2**A-**2**B, memory system **200** comprises a first quad-channel device **201**, a second quad-channel device **1201**, and a substrate **250**. The first quad-channel device **201** is disposed on a first side of substrate **250**. The second quad-channel device **1201** is disposed on a second and opposite side of substrate **250**. In FIG. **2**, the active electrical connection points **211***a* and **211***d* of the first quad-channel device **201** are illustrated. Active electrical connection points **211***a* (e.g., channel A electrical connection points **111***a*) are illustrated in the upper left quadrant of quad-channel device **201** (as viewed through the top of the package, where the electrical connection points are on the bottom of the package.) Active electrical connection points **211***d* (e.g., channel D electrical connection points **111***d*) are illustrated in the lower right quadrant of quad-channel device **201**. The upper right and lower left quadrants of quad-channel device **201** are illustrated as blank in FIG. **2**A to represent electrical connection points (e.g., electrical connection points **111***b* and **111***c*, respectively) that are inactive, unused, and/or unconnected to substrate **250**.

FIG. **2**B illustrates, with the substrate removed for clarity, the first and second quad-channel DRAMs oppositely mounted to utilize dual-channel mode. In FIG. **2**B, as in FIG. **2**A, active electrical connection points **211***a* are illustrated in the upper left quadrant of quad-channel device **201** (as viewed through the top of the package, where the electrical connection points are on the bottom of the package.) Active electrical connection points **211***d* are illustrated in the lower right quadrant of quad-channel device **201** when viewed from the same perspective. The upper right and lower left quadrants of quad-channel device **201** are illustrated as blank in FIG. **2**B.

In addition, in FIG. **2**B, active electrical connection points **1211***a* are illustrated in the upper right quadrant of quad-channel device **1201** (when viewed from the bottom of the package, where the electrical connection points are on the bottom of the package.) When viewed from the perspective of the top of quad-channel device **1211***a*, electrical connection points **1211***a* would be in the upper left quadrant of quad-channel device **1201**. Note that when viewed from the respective tops of their packages, active electrical connections points **211***a* and **1211***a* occupy the same quadrant (i.e., upper left.) Thus, when in dual-channel mode, electrical connection points **211***a* and **1211***a* correspond to the same channel (e.g., channel A **111***a* in FIGS. **1**A-**1**C.) Likewise, but not shown in FIG. **2**B, electrical connection points in the lower right quadrant of quad-channel device **1201** (when viewed from top of **1201**) correspond to the same channel as electrical connection points **211***d* of quad-channel device **201** (e.g., channel D **111***d* in FIG. **1**A-**1**C.)

It should be noted that the inactive upper right quadrant of quad-channel device **201** is aligned with and positioned opposite of active electrical connection points **1211***a* of quad-channel device **1201**. Likewise, but not shown in FIG. **2**B, the inactive lower left quadrant of quad-channel device **201** is aligned with and positioned opposite of active electrical connection points in the lower right quadrant (viewed from the top) of quad-channel device **1201**.

FIG. **3**A illustrates a first example device orientation and active channel connections for a pair of oppositely mounted quad-channel DRAMs. In FIGS. **3**A-**3**C, memory system **300** comprises a first quad-channel device **301**, a second quad-channel device **1301**, and a substrate **350**. Quad-channel device **301** is disposed on a first side of substrate **350** with its bottom (i.e., side with electrical connections/solder balls/pins) towards substrate **350** (and away from the viewer of FIGS. **3**A-**3**C.) When viewed from the perspective of FIGS. **3**A-**3**C: device orientation marker **360** and channel A electrical connections **311***a* of quad-channel device **301** are in the upper left quadrant; channel B electrical connections **311***b* are in the upper right quadrant; channel C connections **311***c* are in the lower left quadrant; and channel D connections **311***d* are in the lower right.

Quad channel device **1301** is disposed on the opposite side of substrate **350** with its bottom towards substrate **350** (thus, towards the viewer of FIGS. **3**A-**3**C.) When viewed from the perspective of FIGS. **3**A-**3**C, device orientation marker **1360** and channel A electrical connections **1311***a* of quad-channel device **1301** are in the lower left quadrant; channel B electrical connections **1311***b* are in the lower right quadrant; channel C connections **1311***c* are in the upper left quadrant; and channel D connections **1311***d* are in the upper right.

As can be observed from FIGS. **3**A-**3**C, when devices **301** and **1301** are in dual-channel mode, active channel A connections **311***a* of device **301** are disposed opposite of and aligned with the inactive channel C connections **1311***c* of device **1301**; inactive channel B connections **311***b* of device **301** are disposed opposite of and aligned with active channel D connections **1311***d* of device **1301**; inactive channel C connections **311***c* of device **301** are disposed opposite of and aligned with active channel A connections **1311***a* of device **1301**; and, active channel D connections **311***d* of device **301** are disposed opposite of and aligned with the inactive channel B connections **1311***b* of device **1301**.

FIG. **3**B illustrates a first example device orientation and active channel connection symmetry for a pair of oppositely mounted quad-channel DRAMs. In FIG. **3**B, channel connections **311***a*-**311***d* and **1311***a*-**1311***d*, and device orientation markers **360** and **1360** are disposed in the same positions as illustrated in FIG. **3**A. A channel connection orientation marker **361***a* is shown in the upper left corner of channel A connections **311***a*. Channel connection orientation marker **361***b* is shown in the upper right corner of channel B connections **311***b*. Channel connection orientation marker **361***c* is shown in the lower left corner of channel C connections **311***c*. Channel connection orientation marker **361***d* is shown in the lower right corner of channel D connections **311***d*.

In an embodiment, channel connections **311***a*-**311***d* have the same signal to physical position (e.g., grid location) layout except are mirrored from each other along one or more reflective symmetry lines. This is illustrated by the locations of connection orientations markers **361***a*-**361***c* (which, for example, could correspond to a particular physical connection location—e.g., pad, ball, pin, etc.) Thus, for example, channel B connections **311***b* have the same layout as the channel A connections **311***a* except that, as illustrated by the locations of orientation markers **361***a* and **361***b*, the channel B connections **311***b* are mirrored from the channel A connection positions along a line that lies between them. When mirrored along a vertical line (in FIG. **3**B) between channel A connections **311**a and channel B connections **311**b, orientation marker **361**b (and corresponding other connection points etc.) moves to the righthand side of channel B connections **311**b as compared to the left-hand side of channel A connections **311**a.

Channel C connections **311**c have the same layout as the channel A connections **311**a except that, as illustrated by the locations of orientation markers **361**a and **361**c, the channel C connections **311**c are mirrored from the channel A connection positions along a line that lies between them. When mirrored along a horizontal line (in FIG. **3**B) between channel A connections **311**a and channel C connections **311**c, orientation marker **361**c (and corresponding other connection points etc.) moves to the bottom of channel C connections **311**c as compared to the top of channel A connections **311**a.

Channel D connections **311**d have the same layout as the channel A connections **311**a except that, as illustrated by the locations of orientation markers **361**a and **361**d, the channel D connections **311**d are mirrored from the channel A connection positions along two lines: a first symmetry line that lies between channel A connections **311**a and channel B connections **311**b (and also lies between channel C connections **311**c and channel D connections **311**d), and a second symmetry line that lies between channel A connections **311**a and channel C connections **311**c (and also lies between channel B connections **311**b and channel D connections **311**d). When mirrored along these lines (one horizontal line and one vertical in FIG. **3**B), orientation marker **361**d (and corresponding other connection points etc.) move to the bottom right hand corner of channel D connections **311**d as compared to the top left-hand corner of channel A connections **311**a.

Since quad-channel device **301** and quad-channel device **1301** have the same layout of channel connections **311**a-**311**d, **1301**a-**1301**d, the physical connection positions of **1301**a-**1301**d have the same mirroring. This is illustrated by the locations of orientation markers **1361**a-**1361**d in FIGS. **3**B-**3**C.

It should be understood that, in an embodiment, there may be one or more individual signals (e.g., low-speed signals such as a reset signal and/or reference voltages) that don't physically mirror perfectly. For example, a given data signal (e.g., DQ**0**) may mirror with another data signal (e.g., DQ**4**) that performs the same function and/or has the same meaning. In another embodiment, a majority or substantially all of the individual signals of a channel are mirrored with another channel and those that are not perfectly mirrored are close to the mirrored location so that a small amount of routing is used on the substrate between the DRAMs to connect them.

In an embodiment, the DRAM includes one or more registers to store a register value that determines top-side/bottom side modes such that the package balls are coupled to the internal circuits in a manner that the signals are mirrored between the two modes. For example, this register value (i.e., mode) may be set by a memory controller via one or more of the channels. The memory controller includes an interface that issues a mode register set (MRS) command, along with the register value to the memory device. The DRAM receives the MRS command and stores the register value in the register to set the top-side/bottom side (or other variants) mode. In another example, the register value may also be set using serial presence detect circuitry where parameter information pertaining to the DRAM, stored in a memory device (such as a serial presence detect (SPD) device) or the DRAM itself is read by the memory controller or other interface. The memory controller then, based on the parameter information, sets the top-side/bottom side mode using one of the methods described herein. In another example, the register value (or the top-side/bottom side mode) may be set by a signal (i.e., voltage) asserted on a pin during power-up, reset, and/or normal operating state The memory controller may assert the voltage on the pin which is included on the DRAM. In another embodiment, two different package designs can be used for when the device is placed on top of the substrate or the bottom so that the signals are mirrored. These different package designs may also be configured set the signal (i.e., voltage) on a pin of the DRAM that determines the mode.

FIG. **3**C illustrates a first example active to inactive channel connection correspondence for a pair of oppositely mounted quad-channel DRAMs. As is illustrated in FIG. **3**C, the physical location of orientation marker **361**a corresponds to the physical location of orientation marker **1361**c (but on the other side of substrate **350**). Thus, the physical location of a pad/ball/etc. connection corresponding to a given signal in channel A **311**a corresponds to and is opposite of the physical location of a pad/ball/etc. of the same signal in channel C **1311**c. This is illustrated in FIG. **3**C by arrow **371** running between orientation marker **361**a to orientation marker **1361**c. The same relationship holds for the physical connection locations of the individual signals of channel D connections **311**d and channel B connections **1311**b (illustrated by arrow **372** running between orientation marker **361**d and orientation marker **1361**b); the physical connection locations of the individual signals of channel C connections **311**c and channel A connections **1311**a (illustrated by arrow **373** running between orientation marker **361**c and orientation marker **1361**a); and, the physical connection locations of the individual signals of channel B connections **311**b and channel D connections **1311**d (illustrated by arrow **374** running between orientation marker **361**b and orientation marker **1361**d).

FIG. **4**A illustrates a second example device orientation and active channel connections for a pair of oppositely mounted quad-channel DRAMs. In FIGS. **4**A-**4**C, memory system **400** comprises a first quad-channel device **401**, a second quad-channel device **1401**, and a substrate **450**. Quad-channel device **401** is disposed on a first side of substrate **450** with its bottom (i.e., side with electrical connections/solder balls/pins) towards substrate **450** (and away from the viewer of FIGS. **4**A-**4**C.) When viewed from the perspective of FIGS. **4**A-**4**C: device orientation marker **460** and channel A electrical connections **411**a of quad-channel device **401** are in the upper left quadrant; channel B electrical connections **411**b are in the upper right quadrant; channel C connections **411**c are in the lower left quadrant; and channel D connections **411**d are in the lower right.

Quad channel device **1401** is disposed on the opposite side of substrate **450** with its bottom towards substrate **450** (towards the viewer of FIGS. **4**A-**4**C.) When viewed from the perspective of FIGS. **4**A-**4**C, device orientation marker **1460** and channel A electrical connections **1411**a of quad-channel device **1401** are in the upper right; channel B electrical connections **411**b are in the upper left; channel C connections **1 411**c are in the lower right quadrant; and channel D connections **1411**d are in the lower left quadrant.

As can be observed from FIGS. **4**A-**4**C, when devices **401** and **1401** are in dual-channel mode, active channel A connections **411**a of device **401** are disposed opposite of and aligned with the inactive channel B connections **1411**b of device **1401**; inactive channel B connections **411**b are disposed opposite of and aligned with active channel A connections **1411**a of device **1401**; inactive channel C connections **411**c are disposed opposite of and aligned with active channel D connections **1411**d of device **1401**; and, active channel D connections **411**d of device **401** are disposed opposite of and aligned with the inactive channel C connections **1411**c of device **1401**.

In an embodiment, channel connections **411**a-**411**d and **1411**a-**1411**d have the same signal to physical position (e.g., grid location) layout except are mirrored from each other along one or more reflective symmetry lines. This is illustrated by the locations of connection orientations markers **461**a-**461**d and **1461**a-**1461**d (which, for example, could correspond to a particular signal physical connection location.) The mirroring of physical connections to signal assignments along symmetry lines between channel connections **411**a-**411**d and **1411**a-**1411**d was discussed previously with reference to FIGS. **3**A-3C (**311**a-**311**d and **1311**a-**1311**d) and thus, for the sake of brevity, will not be repeated here.

FIG. **4**C illustrates a second example active to inactive channel connection correspondence for a pair of oppositely mounted quad-channel DRAMs. As is illustrated in FIG. **4**C, the physical location of orientation marker **461**a corresponds to the physical location of orientation marker **1461**b (but on the other side of substrate **450**). Thus, the physical location of a pad/ball/etc. connection corresponding to a given signal in channel A **411**a corresponds to and is opposite of the physical location of a pad/ball/etc. of the same signal in channel B **1411**b. This is illustrated in FIG. **4**C by arrow **471** running between orientation marker **461**a to orientation marker **1461**b. The same relationship holds for the physical connection locations of the individual signals of channel D connections **411**d and channel C connections **1411**c (illustrated by arrow **472** running between orientation marker **461**d and orientation marker **1461**c); the physical connection locations of the individual signals of channel C connections **411**c and channel D connections **1411**d (illustrated by arrow **473** running between orientation marker **461**c and orientation marker **1461**d); and, the physical connection locations of the individual signals of channel B connections **411**b and channel A connections **1411**a (illustrated by arrow **474** running between orientation marker **461**b and orientation marker **1461**a).

FIG. **5**A illustrates a first example device orientation using partial per-channel connections for a pair of oppositely mounted quad-channel DRAMs. In FIGS. **5**A-**5**B, memory system **500** comprises a first quad-channel device **501**, a second quad-channel device **1501**, and a substrate **550**. Quad-channel device **501** is disposed on a first side of substrate **550** with its bottom (i.e., side with electrical connections/solder balls/pins) towards substrate **550** (and away from the viewer of FIGS. **5**A-**5**B.) When viewed from the perspective of FIGS. **5**A-**5**B: device orientation marker **560** and channel A electrical connections **511**aa-**511**ab, of quad-channel device **501** are in the upper left quadrant; channel B electrical connections **511**ba-**511**bb are in the upper right quadrant; channel C connections **511**ca-**511**cb are in the lower left quadrant; and channel D connections **511**da-**511**db are in the lower right.

Quad channel device **1501** is disposed on the opposite side of substrate **550** with its bottom towards substrate **550** (i.e., towards the viewer of FIGS. **5**A-**5**B.) When viewed from the perspective of FIGS. **5**A-**5**B, device orientation marker **1560** and channel A electrical connections **1511**aa-**1511**ab of quad-channel device **1501** are in the lower left quadrant; channel B electrical connections **1511**ba-**1511**bb are in the lower right quadrant; channel C connections **1511**ca-**1511**cb are in the upper left quadrant; and channel D connections **1511**da-**1511**db are in the upper right.

In FIGS. **5**A-**5**B, channel connections **511**aa, **511**ba, **511**ca, **511**da, **1511**aa, **1511**ba, **1511**ca, and **1511**da are active in the dual-channel mode. Channel connections **511**ab, **511**bb, **511**cb, **511**db, **1511**ab, **1511**bb, **1511**cb, and **1511**db are inactive in the dual-channel mode. Thus, for any given group of channel A, B, C, or D connections, a portion of the connections are active and a portion of the connections are inactive.

As can be observed from FIGS. **5**A-**5**B, when devices **501** and **1501** are in dual-channel mode, the active portion of channel A connections **511**aa of device **501** are disposed opposite of and aligned with the inactive portion of channel C connections **1511**cb of device **1301**; the inactive portion of channel B connections **511**bb are disposed opposite of and aligned with the active portion of channel D connections **1511**da of device **1501**; the inactive portion of channel C connections **511**cb are disposed opposite of and aligned with the active portion of channel A connections **1511**aa of device **1501**; the active portion of channel D connections **511**da of device **501** are disposed opposite of and aligned with the inactive portion of channel B connections **1511**bb of device **1501**; the inactive portion of channel A connections **511**ab are disposed opposite of and aligned with the active portion of channel C connections **1511**ca; the active portion of channel B connections **511**ba are disposed opposite of and aligned with the inactive portion of channel D connections **1511**db of device **1501**; the active portion of channel C connections **511**ca are disposed opposite of and aligned with the inactive portion of channel A connections **1511**ab of device **1501**; and, the inactive portion of channel D connections **511**db of device **501** are disposed opposite of and aligned with the active portion of channel B connections **1511**ba of device **1501**.

FIG. **5**B illustrates a first example active to inactive partial per-channel connection correspondence for a pair of oppositely mounted quad-channel DRAMs. In particular, the physical location correspondence between signals in the inactive portion of channel C connections **511**cb and the physical location of signals in the active portion of channel A connections **1511**aa is illustrated by arrow **571**. The physical location correspondence between signals in the active portion of channel B connections **511**ba and the physical location of signals in the inactive portion of channel D connections **1511**db is illustrated by arrow **572**. Further discussion of the other physical location correspondences present between the active/inactive signals of devices **501** and **1501** are omitted herein for the sake of brevity.

FIG. **6**A illustrates a second example device orientation using partial per-channel connections for a pair of oppositely mounted quad-channel DRAMs. In FIGS. **6**A-**6**B, memory system **600** comprises a first quad-channel device **601**, a second quad-channel device **1601**, and a substrate **650**. Quad-channel device **601** is disposed on a first side of substrate **650** with its bottom (i.e., side with electrical connections/solder balls/pins) towards substrate **650** (and away from the viewer of FIGS. **6**A-**6**B.) When viewed from the perspective of FIGS. **6**A-**6**B: device orientation marker **660** and channel A electrical connections **611**aa-**611**ab, of quad-channel device **601** are in the upper left quadrant; channel B electrical connections **611**ba-**611**bb are in the upper right quadrant; channel C connections **611**ca-**611**cb are in the lower left quadrant; and channel D connections **611**da-**611**db are in the lower right.

Quad channel device **1601** is disposed on the opposite side of substrate **650** with its bottom towards substrate **650** (i.e., towards the viewer of FIGS. **6**A-**6**B.) When viewed from the perspective of FIGS. **6**A-**6**B, device orientation marker **1660** and channel A electrical connections **1611***aa*-**1611***ab* of quad-channel device **1601** are in the upper right quadrant; channel B electrical connections **1611***ba*-**1611***bb* are in the upper left quadrant; channel C connections **1611***ca*-**1611***cb* are in the lower right quadrant; and channel D connections **1611***da*-**1611***db* are in the lower left.

In FIGS. **6**A-**6**B, channel connections **611***aa*, **611***ba*, **611***ca*, **611***da*, **1611***aa*, **1611***ba*, **1611***ca*, and **1611***da* are active in the dual-channel mode. Channel connections **611***ab*, **611***bb*, **611***cb*, **611***db*, **1611***ab*, **1611***bb*, **1611***cb*, and **1611***db* are inactive in the dual-channel mode. Thus, for any given group of channel A, B, C, or D connections, a portion of the connections are active and a portion of the connections are inactive.

As can be observed from FIGS. **6**A-**6**B, when devices **601** and **1601** are in dual-channel mode, the active portion of channel A connections **611***aa* of device **601** are disposed opposite of and aligned with the inactive portion of channel B connections **1611***bb* of device **1601**; the inactive portion of channel B connections **611***bb* are disposed opposite of and aligned with the active portion of channel A connections **1611***aa* of device **1601**; the inactive portion of channel C connections **611***cb* are disposed opposite of and aligned with the active portion of channel D connections **1611***da* of device **1601**; the active portion of channel D connections **611***da* of device **601** are disposed opposite of and aligned with the inactive portion of channel C connections **1611***cb* of device **1601**, the inactive portion of channel A connections **611***ab* of device **601** are disposed opposite of and aligned with the active portion of channel B connections **1611***ba* of device **1601**; the active portion of channel B connections **611***ba* are disposed opposite of and aligned with the inactive portion of channel A connections **1611***ab* of device **1601**; the active portion of channel C connections **611***ca* are disposed opposite of and aligned with the inactive portion of channel D connections **1611***db* of device **1601**; and, the inactive portion of channel D connections **611***db* of device **601** are disposed opposite of and aligned with the active portion of channel C connections **1611***ca* of device **1601**.

FIG. **6**B illustrates a first example active to inactive partial per-channel connection correspondence for a pair of oppositely mounted quad-channel DRAMs. In particular, the physical location correspondence between signals in the active portion of channel C connections **611***ca* and the physical location of signals in the inactive portion of channel D connections **1611***db* is illustrated by arrow **671**. The physical location correspondence between signals in the inactive portion of channel B connections **611***bb* and the physical location of signals in the active portion of channel A connections **1611***aa* is illustrated by arrow **672**. Further discussion of the other physical location correspondences present between the active/inactive signals of devices **601** and **1601** are omitted herein for the sake of brevity.

FIG. **7**A illustrates an example floorplan for a quad-channel DRAM and example worst-case latency paths in quad-channel mode. In FIG. **7**A, memory device **700** is configured with four active channels: channel A **710***a*, channel B **710***b*, channel C **710***c*, and channel D **710***d*. The active circuitry/logic for channel A **710***a* when DRAM device **700** is configured in the four active channel (a.k.a., quad-channel) mode comprises a set of memory cores **714***a* that are accessed using channel A data (DQ) circuitry **717***a*, and channel A command/address (CA) circuitry **716***a*. The active circuitry/logic for channel B **710***b* when DRAM device **700** is configured in quad-channel mode comprises a set of memory cores **714***b* that are accessed using channel B data (DQ) circuitry **717***b*, and channel B command/address (CA) circuitry **716***b*. The active circuitry/logic for channel C **710***c* when DRAM device **700** is configured in quad-channel mode comprises a set of memory cores **714***c* that are accessed using channel C data (DQ) circuitry **717***c*, and channel C command/address (CA) circuitry **716***c*. The active circuitry/logic for channel D **710***d* when DRAM device **700** is configured in quad-channel mode comprises a set of memory cores **714***d* that are accessed using channel D data (DQ) circuitry **717***d*, and channel D command/address (CA) circuitry **716***d*.

Also illustrated in FIG. **7**A are example worst case access paths for each of the channels **710***a*-**710***d*. An example worst case access path for CA distribution by channel A **710***a* is illustrated by arrow **718***a*. Arrow **718***a* runs from channel A CA interface circuitry **716***a* to the memory core **714***a* in the upper-left corner of channel A circuitry **710***a*. An example worst case data path returning from the memory core **714***a* in the upper-left corner of channel A circuitry **710***a* to channel A DQ interface circuitry **717***a* is illustrated by arrow **719***a*. Similar example worst case CA distribution access paths and DQ return paths are illustrated for channels B-D by arrows **718***b*-**718***d*, and **719***b*-**719***d*, respectively.

FIG. **7**B illustrates an example floorplan for a quad-channel DRAM and example worst-case latency paths in clamshell (dual-channel) mode. In FIG. **7**B, memory device **700** is configured with two active channels: channel A **710***a* and channel D **710***d*. The memory cores **714***b* and **714***c* accessed by channel B **710***b* and channel C **710***c*, respectively, in the quad channel mode are accessed by the circuitry (and interfaces) of channel A **710***a* and channel D **710***d*, respectively, when memory device **700** is in dual channel mode.

Also illustrated in FIG. **7**B are example worst case access paths for each of the channels **710***a* and **710***d*. An example worst case access path for CA distribution for memory cores **714***a* is illustrated by arrow **718***a*. Arrow **718***a* runs from channel A CA interface circuitry **716***a* to the memory core **714***a* in the upper-left corner of channel A circuitry **710***a*. An example worst case data path returning from the memory core **714***a* in the upper-left corner of channel A circuitry **710***a* to channel A DQ interface circuitry **717***a* is illustrated by arrow **719***a*.

In dual-channel mode, the memory cores **714***b* associated with channel B **710***b* in the quad channel mode are now accessed via the channel A **710***a* circuitry. An example worst case access path for CA distribution to memory cores **714***b* is illustrated by arrow **720***b*. Arrow **720***b* runs from channel A CA interface circuitry **716***a* to the memory core **714***b* in the upper-right corner of channel B circuitry **710***b*. An example worst case data path returning from memory core **714***b* in the upper-right corner of channel B circuitry **710***b* to channel A DQ interface circuitry **717***a* is illustrated by arrow **721***b*. Example worst case CA distribution access path and DQ return path are illustrated for channel C **710***c* memory cores **714***c* by arrows **720***c* and **721***c*, respectively. Example worst case CA distribution access path and DQ return path are illustrated for channel D **710***d* memory cores **714***d* by arrows **718***d* and **719***d*, respectively.

In an embodiment, the extra length of access paths **720***b* and **721***b*, as compared to access paths **719***a* and **719***b*, may result in additional access latency. For example, 2 additional clock cycle/phases may be used—1 to account for increased CA distribution path delay (path **720***b*) and 1 for increased DQ return path delay (path **721***b*). In an embodiment, memory device **700** may be configured to also increase access latencies for channel A **710***a* memory cores **714***a* such that the all accesses via channel A **710***a*, whether to memory cores **714***a* or **714***b* have the same access latency. In another embodiment, the access latencies to memory cores **714***a* may be shorter than the access latencies to memory cores **714***b*. In an embodiment, the most-significant bit (MSB) of the row address may determine whether the access latency is the shorter (i.e., to memory cores **714***a*) or the longer (i.e., to memory cores **714***b*) access latency. To allow for additional processing time in order to determine whether an access is to memory cores **714***a* versus **714***b*, memory device **700** may be configured to receive the MSB of the row access and the bank address early (or at the start of) the command sequence (e.g., received in the first and/or second cycles of the command/address information packet.) Receiving the MSB of the row access and the bank address (or whatever signals determine the quadrant of the access) early in the command sequence allows the decoding of the quadrant before the entire command/address is decoded. This reduces the path delay impact that would otherwise occur if the quadrant information was received later in the command sequence. In another embodiment, a bit of the column address may determine whether the access time is the shorter (i.e., to memory cores **714***a*) or the longer (i.e., to memory cores **714***b*) access time.

FIG. **8** illustrates an example block diagram for two channels of a quad-channel DRAM. In FIG. **8**, memory device **800** comprises channel A DQ interface circuitry **817***a*, channel B DQ interface circuitry **817***b*, channel A CA interface circuitry **816***a*, channel B CA interface circuitry **816***b*, channel A DQ logic **827***a*, channel B DQ logic **827***b*, channel A CA latch **826***a*, channel B CA latch **826***b*, clamshell mode decoder **840**, internal clock (iCK) generation circuitry **845**, channel A command logic **823***a*, channel B command logic **823***b*, channel A bi-directional tri-state buffers **837***a*, channel B bi-directional tri-state buffers **837***b*, internal CA steering tri-state buffers **841**, internal DQ bus isolation/steering tri-state buffers **842**, channel A associated memory banks **874***a*-**875***a*, and channel B associated memory banks **874***b*-**875***b*.

In an embodiment, DQ interface circuitry **817***a*-**817***b* includes circuitry for nine (or alternately eight) bidirectional data signals (e.g., DQ[0:8] or DQ[0:7]), receiving a write clock signal (WCK), and a bidirectional data bus inversion (DBI) signal. Command address interface circuitry **816***a*-**816***b* include circuitry for seven command/address signals (e.g., CA[0:6].) Internal clock generation circuitry **845** receives an external clock signal CK. Clock generation circuitry **845** generates and distributes internal clock signals iCK, iCK/2. iCK2 is a ½ frequency version of iCK and includes two phases separated by 180° (e.g., inversions of each other.)

Channel A associated memory banks **874***a*-**875***a* are operatively coupled to internal command bus C (busC) **884***a* and internal data bus E (busE) **887***a*. Internal busC **884***a* may include signals corresponding to a row address strobe (RAS), read column address strove (RCAS), write column address strobe (WCAS), and address signals (ADDR). Internal command busA'**824***a* is generated by command logic **823***a* from signals received via the output of latch **826***a* (i.e., busA **825***a*). Internal busA **825***a* (or a subset thereof—e.g., MSB of row address) is also provided to clamshell decoder logic **840**. Internal busA'**824***a* may include signals corresponding to, for channel A associated memory banks **874***a*-**875***a* and/or for channel B associated memory banks **874***b*-**875***b*, RAS, RCAS, WCAS, and address signals (ADDR).

Channel B associated memory banks **874***b*-**875***b* are operatively coupled to internal command bus B (busB) **884***b* and internal data bus D (busD) **887***b*. Internal busB **884***b* may include signals corresponding to, for channel B associated memory banks **874***b*-**875***b*, RAS, RCAS, WCAS, and address signals (ADDR).

Tri-state buffers **837***a* selectively couple and uncouple DQ logic **827***a* with internal data bus E (busE) **887***a* under the control of write ready (WRrdy) and read ready (RDrdy) signals. Internal busE **887***a* may include 256 data lines and the RDrdy signal. The RDrdy signal may be generated along with the data being read from a memory bank **874***a*-**875***a* (and banks **874***b*-**875***b* when memory device **800** is in clamshell mode) and acts as a handshake signal.

When not in clamshell mode, tri-state buffers **837***b* selectively couple and uncouple DQ logic **827***b* with internal data bus D (busD) under the control of B-channel write ready (BWRrdy) and B-channel read ready (BRDrdy) signals. Internal busD may include 256 data lines and the RDrdy signal. The RDrdy signal may be generated along with the data being read from a memory bank **874***b*-**875***b* and acts as a handshake signal. Tri-state buffers **837***b* do not couple DQ logic **827***b* with busD **887***b* when memory device **800** is in clamshell mode. Thus, in an embodiment, the signal BWRdy may be generated, at least in part, according to the following logical equation: BWRrdy=!CSm AND WRrdy, where CSm is a logical '1' when memory device **800** is in clamshell mode, and the exclamation point represents a logical NOT (i.e., inversion) operation. The signal BRDrdy may be generated, at least in part, according to the following logical equation: BRDrdy=!CSm AND RDrdy.

Tri-state buffers **841** selectively drive internal command bus A' (busA') to either busB **884***b* or busC **884***a*. When memory device **800** is not in clamshell mode, clamshell decode **840** sets mdR15 signal **847** such that busA' is driven to busC **884***a*. When memory device **800** is in clamshell mode, clamshell decode **840** sets mdR15 signal **847** such that busA' is driven to busC **884***a* if the MSB of the row address (e.g., R15) is logical zero (0) and to busB **884***b* if it is a logical one (1). Thus, in an embodiment, the signal mdR15 may be generated, at least in part, according to the following logical equation: mdR15=CSm AND R15.

Tri-state buffers **842** selectively couple busD **887***b* to busE **887***a* and vice versa under the control of the signals CWRrdy and CRDrdy. In non-clamshell mode, busD **887***b* to busE **887***a* are not coupled to each other. In clamshell mode, busD **887***b* may be coupled to busE **887***a* depending upon the value of the MSB of the row address (e.g., R15). The direction that signals are propagated between busD **887***b* and busE **887***a* depends upon whether the operation is a read or a write. Thus, in an embodiment, the signal CWRrdy may be generated, at least in part, according to the following logical equation: CWRrdy=CSm AND R15 AND WRrdy. The signal CRDrdy may be generated, at least in part, according to the following logical equation: CRDrdy=CSm AND R15 AND RDrdy.

Tri-state buffers **843** selectively couple outputs **824***b* of command logic **823***b* to busB **884***b*. When in clamshell mode, the CSm signal tri-states the outputs of buffers **843** so that tri-state buffers **841** may drive busB **884***b*. In an embodiment, the CSm mode signal can also disable channel B DQ interface circuitry **817***b*, channel B CA interface circuitry **816***b*, channel B DQ logic **827***b*, and channel A command logic **823***a*.

FIG. **9** is a timing diagram illustrating example row accesses for a quad-channel DRAM in clamshell (dual-channel) mode. The timings, signals, and functions illustrated in FIG. **9** may be used by one or more of memory device **101**, memory system **200**, memory system **300**, memory system **400**, memory system **500**, memory system **600**, memory device **700**, memory device **800**, and/or their components.

In FIG. **9**, an edge of internal clock, iCK, latches a first activate command (ACT**1**) on the CA interface and drives (at least) the activate command (ACT**1**), a first bank address (BA**1**), and the most significant bit of the row address (R15) onto busA (e.g., busA **825***a*). This is illustrated in FIG. **9** by arrow **901**. The value of R15 and the mode (i.e., clamshell mode) are logically combined to set mdR15 to a logical '1' (e.g., mdR15=CSm AND R15=1.) This is illustrated in FIG. **9** by arrow **902**. In other embodiments, different bits may be used to distinguish which memory bank(s) an access is directed to. For example, the most significant bit of the column address, or a bit in the command itself (rather than an address bit) may be used.

An edge of a half-frequency internal clock (e.g., iCK/2-180) times the driving of the activate command, the bank address, and the row address bits (except for the MSB—R15) onto busA' and from busA' to busB. This is illustrated by arrows **903** and **905**, respectively. An edge of the half-frequency internal clock also times the assertion of a 'command ready' signal to the memory bank addressed by the bank address (e.g., memory banks **874***b*-**875***b*.) This is illustrated by arrow **904**.

Another edge of internal clock, iCK, latches a second activate command (ACT**2**) on the CA interface and drives (at least) the second activate command (ACT**2**), a second bank address (BA**1**), and the most significant bit of the row address onto busA (e.g., busA **825***a*). The most significant bit of the row address is the opposite value as for the first activate command. This is illustrated in FIG. **9** using the notation !R15. The value of !R15 and the mode (i.e., clamshell mode) are logically combined to set mdR15 to a logical '0' (e.g., mdR15=CSm AND !R15=0.) This is illustrated in FIG. **9** by arrow **906**.

An edge of a half-frequency internal clock (e.g., iCK/2-180) times the driving of the second activate command, the second bank address, and the second row address bits (except for the MSB—!R15) onto busA' and from busA' to busC. This is illustrated by arrow **907**. An edge of the half-frequency internal clock also times the assertion of a 'command ready' signal to the memory bank addressed by the bank address (e.g., memory banks **874***a*-**875***a*.)

FIG. **10** is a timing diagram illustrating example write accesses for a quad-channel DRAM in clamshell (dual-channel) mode. The timings, signals, and functions illustrated in FIG. **10** may be used by one or more of memory device **101**, memory system **200**, memory system **300**, memory system **400**, memory system **500**, memory system **600**, memory device **700**, memory device **800**, and/or their components.

An edge on the external clock CK initiates the processing of a first write command (WR**1**). A number of clock CK cycles later, first set of data bits (DATA**1**) on the external DQ signals is latched into the device by a write clock (WCK) over a number of cycles of WCK. This is illustrated by arrow **1001**. This first set of data bits is addressed to a channel B memory bank **874***b*-**875***b* (note value of mdR15). Thus, the first set of data bits (DATA**1**) is accompanied by Wrdy and steered to busD. This is illustrated by arrows **1002** and **1004**.

Another edge on the external clock CK initiates the processing of a second write command (WR**2**). A number of clock CK cycles later, second set of data bits (DATA**2**) on the external DQ signals is latched into the device by a write clock (WCK) over a number of cycles of WCK. This second set of data bits is addressed to a channel A memory bank **874***a*-**875***a* (note value of mdR15). Thus, the second set of data bits (DATA**2**) is accompanied by Wrdy and is steered to busE. This is illustrated by arrows **1003** and **1005**.

FIG. **11** is a timing diagram illustrating example read accesses for a quad-channel DRAM in clamshell (dual-channel) mode. The timings, signals, and functions illustrated in FIG. **11** may be used by one or more of memory device **101**, memory system **200**, memory system **300**, memory system **400**, memory system **500**, memory system **600**, memory device **700**, memory device **800**, and/or their components.

An edge on the external clock CK initiates the processing of a first read command (RD**1**). A number of clock CK cycles later, first set of data bits (DATA**1**) are output on the external DQ signals. This is illustrated by arrow **1101**. This first set of data bits comes from a channel B memory bank **874***b*-**875***b* (note value of mdR15). Thus, the first set of data bits (DATA**1**) comes from busD and is latched using the Drdy signal. This is illustrated by arrow **1102**.

Another edge on the external clock CK initiates the processing of a second read command (RD**2**). A number of clock CK cycles later, second set of data bits (DATA**2**) are output on the external DQ signals. This is illustrated by arrow **1103**. This second set of data bits comes from a channel A memory bank **874***a*-**875***a* (note value of mdR15). Thus, the second set of data bits (DATA**2**) is comes from busE and is latched using the Drdy signal. This is illustrated by arrow **1104**.

The methods, systems and devices described above may be implemented in computer systems, or stored by computer systems. The methods described above may also be stored on a non-transitory computer readable medium. Devices, circuits, and systems described herein may be implemented using computer-aided design tools available in the art, and embodied by computer-readable files containing software descriptions of such circuits. This includes, but is not limited to one or more elements of memory device **101**, memory system **200**, memory system **300**, memory system **400**, memory system **500**, memory system **600**, memory device **700**, memory device **800**, and their components.

These software descriptions may be: behavioral, register transfer, logic component, transistor, and layout geometry-level descriptions. Moreover, the software descriptions may be stored on storage media or communicated by carrier waves.

Data formats in which such descriptions may be implemented include, but are not limited to: formats supporting behavioral languages like C, formats supporting register transfer level (RTL) languages like Verilog and VHDL, formats supporting geometry description languages (such as GDSII, GDSIII, GDSIV, CIF, and MEBES), and other suitable formats and languages. Moreover, data transfers of such files on machine-readable media may be done electronically over the diverse media on the Internet or, for example, via email. Note that physical files may be implemented on machine-readable media such as: 4 mm magnetic tape, 8 mm magnetic tape, 3½ inch floppy media, CDs, DVDs, and so on.

FIG. **12** is a block diagram illustrating one embodiment of a processing system **1400** for including, processing, or generating, a representation of a circuit component **1420**. Processing system **1400** includes one or more processors **1402**, a memory **1404**, and one or more communications devices **1406**. Processors **1402**, memory **1404**, and communications devices **1406** communicate using any suitable type, number, and/or configuration of wired and/or wireless connections **1408**.

Processors **1402** execute instructions of one or more processes **1412** stored in a memory **1404** to process and/or generate circuit component **1420** responsive to user inputs **1414** and parameters **1416**. Processes **1412** may be any suitable electronic design automation (EDA) tool or portion thereof used to design, simulate, analyze, and/or verify electronic circuitry and/or generate photomasks for electronic circuitry. Representation **1420** includes data that describes all or portions of memory device **101**, memory system **200**, memory system **300**, memory system **400**, memory system **500**, memory system **600**, memory device **700**, memory device **800**, and their components as shown in the Figures.

Representation **1420** may include one or more of behavioral, register transfer, logic component, transistor, and layout geometry-level descriptions. Moreover, representation **1420** may be stored on storage media or communicated by carrier waves.

Data formats in which representation **1420** may be implemented include, but are not limited to: formats supporting behavioral languages like C, formats supporting register transfer level (RTL) languages like Verilog and VHDL, formats supporting geometry description languages (such as GDSII, GDSIII, GDSIV, CIF, and MEBES), and other suitable formats and languages. Moreover, data transfers of such files on machine-readable media may be done electronically over the diverse media on the Internet or, for example, via email

User inputs **1414** may comprise input parameters from a keyboard, mouse, voice recognition interface, microphone and speakers, graphical display, touch screen, or other type of user interface device. This user interface may be distributed among multiple interface devices. Parameters **1416** may include specifications and/or characteristics that are input to help define representation **1420**. For example, parameters **1416** may include information that defines device types (e.g., NFET, PFET, etc.), topology (e.g., block diagrams, circuit descriptions, schematics, etc.), and/or device descriptions (e.g., device properties, device dimensions, power supply voltages, simulation temperatures, simulation models, etc.).

Memory **1404** includes any suitable type, number, and/or configuration of non-transitory computer-readable storage media that stores processes **1412**, user inputs **1414**, parameters **1416**, and circuit component **1420**.

Communications devices **1406** include any suitable type, number, and/or configuration of wired and/or wireless devices that transmit information from processing system **1400** to another processing or storage system (not shown) and/or receive information from another processing or storage system (not shown). For example, communications devices **1406** may transmit circuit component **1420** to another system. Communications devices **1406** may receive processes **1412**, user inputs **1414**, parameters **1416**, and/or circuit component **1420** and cause processes **1412**, user inputs **1414**, parameters **1416**, and/or circuit component **1420** to be stored in memory **1404**.

The foregoing description of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and other modifications and variations may be possible in light of the above teachings. The embodiment was chosen and described in order to best explain the principles of the invention and its practical application to thereby enable others skilled in the art to best utilize the invention in various embodiments and various modifications as are suited to the particular use contemplated. It is intended that the appended claims be construed to include other alternative embodiments of the invention except insofar as limited by the prior art.

What is claimed is:

1. A packaged dynamic random access memory (DRAM), comprising:

a rectangular array of electrical connection conductors, the electrical connection conductors grouped into first, second, third, and fourth quadrants to serve as external, to the packaged DRAM, electrical connection points for a first memory channel, a second memory channel, a third memory channel, and a fourth memory channel, respectively; and

mode indicator circuitry to specify at least first and second modes wherein, in the first mode, each of the first, second, third and fourth memory channels are are to each concurrently operate memory channel command, address, and data transfer functions independent of the other concurrently operating first, second, third, and fourth memory channels, and in the second mode, the first and third memory channels are to each concurrently operate memory channel command, address, and data transfer functions independent of the other concurrently operating first and third memory channels, and also in the second mode, the second and fourth memory channels are disabled.

2. The packaged DRAM of claim **1**, wherein the mode indicator circuit is settable to the first mode and the second mode via at least one of the first memory channel, the second memory channel, the third memory channel, and the fourth memory channel.

3. The packaged DRAM of claim **2**, wherein the mode indicator circuit is settable to the first mode and the second mode using a mode register set command received via the at least one of the first memory channel, the second memory channel, the third memory channel, and the fourth memory channel.

4. The packaged DRAM of claim **1**, wherein the mode indicator circuit is settable to the first mode and the second mode via serial presence detect circuitry.

5. The packaged DRAM of claim **1**, wherein the mode indicator circuit is settable to the first mode and the second mode via a signal asserted on a pin of the packaged DRAM.

6. The packaged DRAM of claim **5**, wherein the signal asserted on the pin is to be asserted during a reset of the packaged DRAM.

7. The packaged DRAM of claim **5**, wherein the signal asserted on the pin is to be asserted during a normal operating state of the packaged DRAM.

8. A packaged dynamic random access memory (DRAM), comprising:

a mode register circuit to indicate at least a first mode and a second mode;

a rectangular array of electrical connection conductors, the electrical connection conductors grouped into first, second, third, and fourth quadrants to serve as external, to the packaged DRAM, electrical connection points for a first memory channel, a second memory channel, a third memory channel, and a fourth memory channel, respectively; and

in the first mode, each of the first, second, third and fourth memory channels are to each concurrently operate memory channel command, address, and data transfer functions independent of the other concurrently operating first, second, third and fourth memory channels, and in the second mode, the first and third memory channels are to each concurrently operate memory channel command, address, and data transfer functions independent of the other concurrently operating first and third memory channels, and also in the second mode, the second and fourth memory channels are disabled.

9. The packaged DRAM of claim **8**, wherein the mode register circuit is settable to indicate the first mode and the second mode via at least one of the first memory channel, the second memory channel, the third memory channel, and the fourth memory channel.

10. The packaged DRAM of claim **9**, wherein the mode register circuit is settable to indicate the first mode and the second mode using a mode register set command received via the at least one of the first memory channel, the second memory channel, the third memory channel, and the fourth memory channel.

11. The packaged DRAM of claim **8**, wherein the mode register circuit is settable to indicate the first mode and the second mode via serial presence detect circuitry.

12. The packaged DRAM of claim **8**, wherein the mode register circuit is settable to indicate the first mode and the second mode via a signal asserted on a pin of the packaged DRAM.

13. The packaged DRAM of claim **12**, wherein the signal asserted on the pin is to be asserted during a reset of the packaged DRAM.

14. The packaged DRAM of claim **12**, wherein the signal asserted on the pin is to be asserted during a normal operating state of the packaged DRAM.

15. A packaged dynamic random access memory (DRAM), comprising:

mode indicator circuitry to indicate at least first and second modes;

four groups of external, to the packaged DRAM, electrical connection conductors corresponding to, in the first mode, four memory channel interfaces that each concurrently operate, in the first mode, memory channel command, address, and data transfer functions independent of each other of the concurrently operating four memory channel interfaces; and

a first two of the four groups of external, to the packaged DRAM, electrical connection conductors corresponding to, in the second mode, two memory channel interfaces that each concurrently operate, in the second mode, memory channel command, address, and data transfer functions independent of the other of the concurrently operating first two memory channel interfaces, a second two of the four groups of external, to the packaged DRAM, electrical connection conductor corresponding to, in the second mode, disabled memory channel interfaces.

16. The packaged DRAM of claim **15**, wherein the mode indicator circuitry is settable to indicate the first mode and the second mode via at least one of the four memory channel interfaces.

17. The packaged DRAM of claim **16**, wherein the mode indicator circuitry is settable to the first mode and the second mode using a mode register set command received via the at least one of the four memory channel interfaces.

18. The packaged DRAM of claim **15**, wherein the mode indicator circuitry is settable to indicate the first mode and the second mode via serial presence detect circuitry.

19. The packaged DRAM of claim **15**, wherein the mode indicator circuitry is settable to indicate the first mode and the second mode via a signal asserted on a pin of the packaged DRAM.

20. The packaged DRAM of claim **19**, wherein the signal asserted on the pin is to be asserted during a reset of the packaged DRAM.

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