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Xiao et al.

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(54) **PIXEL CIRCUIT AND DRIVING METHOD THEREOF, AND DISPLAY PANEL AND DRIVING METHOD THEREOF**

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(73) Assignee: **BOE Technology Group Co., Ltd.**, Beijing (CN)

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(21) Appl. No.: **18/533,211**

(22) Filed: **Dec. 8, 2023**

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Related U.S. Application Data

(63) Continuation of application No. 17/636,897, filed as application No. PCT/CN2021/088615 on Apr. 21, 2021, now Pat. No. 11,875,734.

(51) **Int. Cl.**

G09G 3/32 (2016.01)
G09G 3/20 (2006.01)
(Continued)

(52) **U.S. Cl.**

CPC ***G09G 3/32*** (2013.01); ***G09G 3/2007*** (2013.01); *G09G 3/3208* (2013.01);
(Continued)

(58) **Field of Classification Search**

CPC G09G 3/32; G09G 3/2007; G09G 3/3208; G09G 3/3233; G09G 3/3258;
(Continued)

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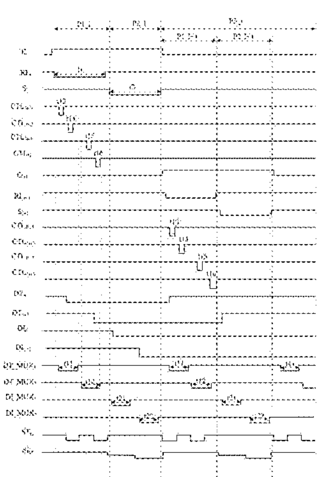
Primary Examiner — Tom V Sheng
(74) *Attorney, Agent, or Firm* — Ling Wu; Stephen Yang; Ling and Yang Intellectual Property

(57) **ABSTRACT**

A drive method for a display panel, wherein the display panel includes a plurality of current data lines, a plurality of time-length data lines, a first current selection signal line, a second current selection signal line, a first time-length selection signal line and a second time-length selection signal line, at least one current data line is connected with the first current selection signal line or the second current selection signal line, and at least one time-length data line is connected with the first time-length selection signal line or the second time-length selection signal line; the method includes: providing a valid level signal to the first time-length selection signal line, the second time-length selection signal line, the first current selection signal line and the second current selection signal line.

18 Claims, 18 Drawing Sheets



(51) **Int. Cl.**
G09G 3/3208 (2016.01)
G09G 3/3233 (2016.01)
G09G 3/3258 (2016.01)

(52) **U.S. Cl.**
CPC *G09G 3/3233* (2013.01); *G09G 3/3258* (2013.01); *G09G 2300/0819* (2013.01); *G09G 2300/0852* (2013.01); *G09G 2300/0861* (2013.01); *G09G 2310/0251* (2013.01); *G09G 2310/08* (2013.01); *G09G 2320/0233* (2013.01); *G09G 2320/0247* (2013.01); *G09G 2320/043* (2013.01); *G09G 2320/045* (2013.01)

(58) **Field of Classification Search**
CPC ... G09G 2300/0819; G09G 2300/0852; G09G 2300/0861; G09G 2310/08; G09G 2310/0251; G09G 2320/0233; G09G 2320/0247; G09G 2320/043; G09G 2320/045
USPC 345/204
See application file for complete search history.

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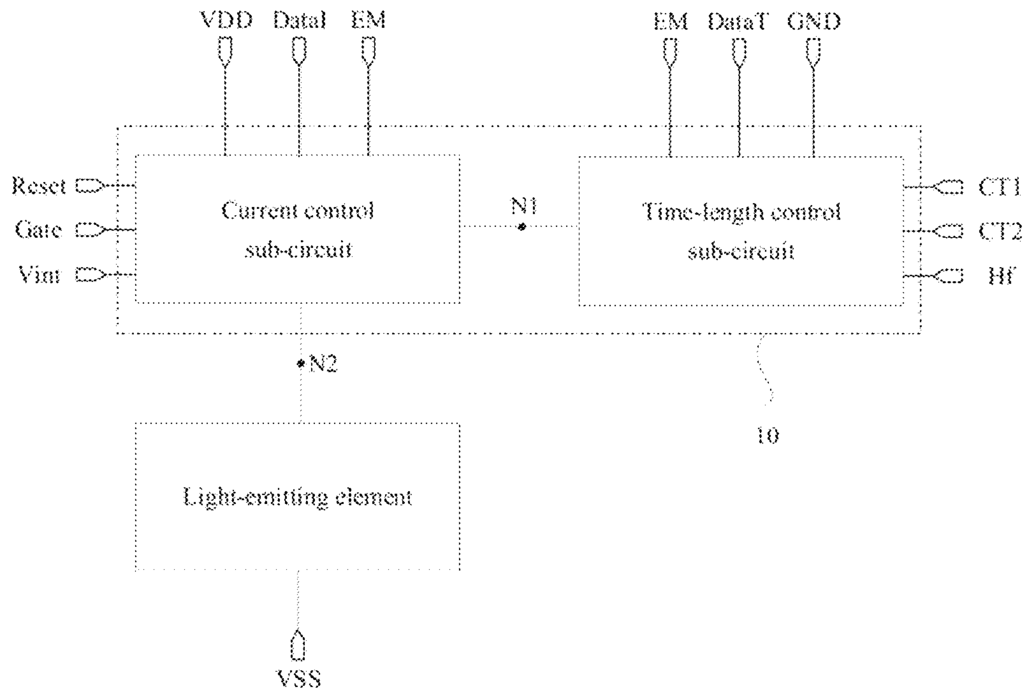
VDD
DataI
EM
EM
DataT
GND
Reset
Gate
Vint
Current control sub-circuit
N1
Time-length control sub-circuit
CT1
CT2
Hf
N2
10
Light-emitting element
VSS

FIG. 1

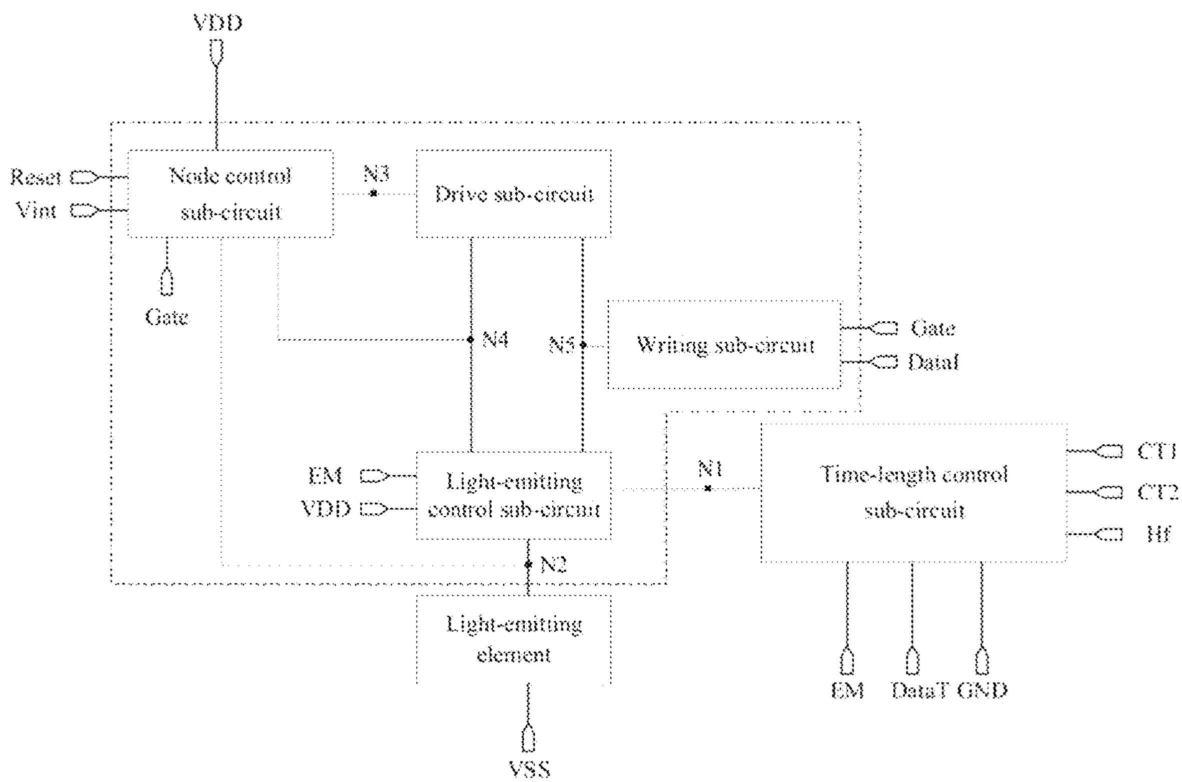
VDD
Reset
Vint
Node control sub-circuit
N3
Drive sub-circuit
Gate
N4
N5
Writing sub-circuit
Gate
DataI
EM
VDD
Light-emitting control sub-circuit
N1
Time-length control sub-circuit
CT1
CT2
Hf
N2
Light-emitting element
EM
DataT
GND
VSS

FIG. 2

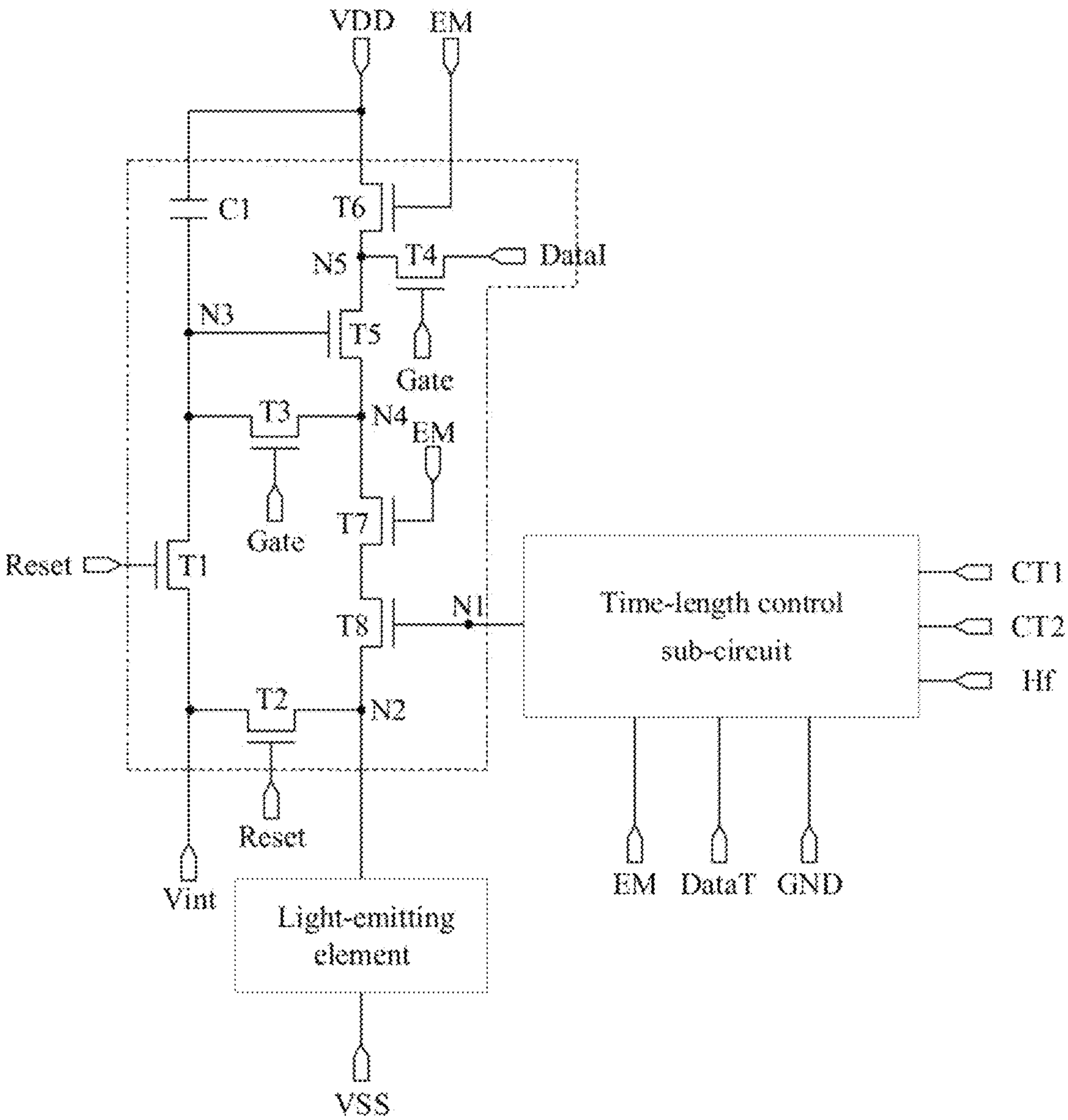
VDD
EM
C1
T6
N5
T4
DataI
N3
T5
Gate
T3
N4
EM
Gate
T7
Reset
T1
T8
N1
Time-length control sub-circuit
CT1
CT2
Hf
T2
N2
Reset
EM
DataT
GND
Vint
Light-emitting element
VSS

FIG. 3

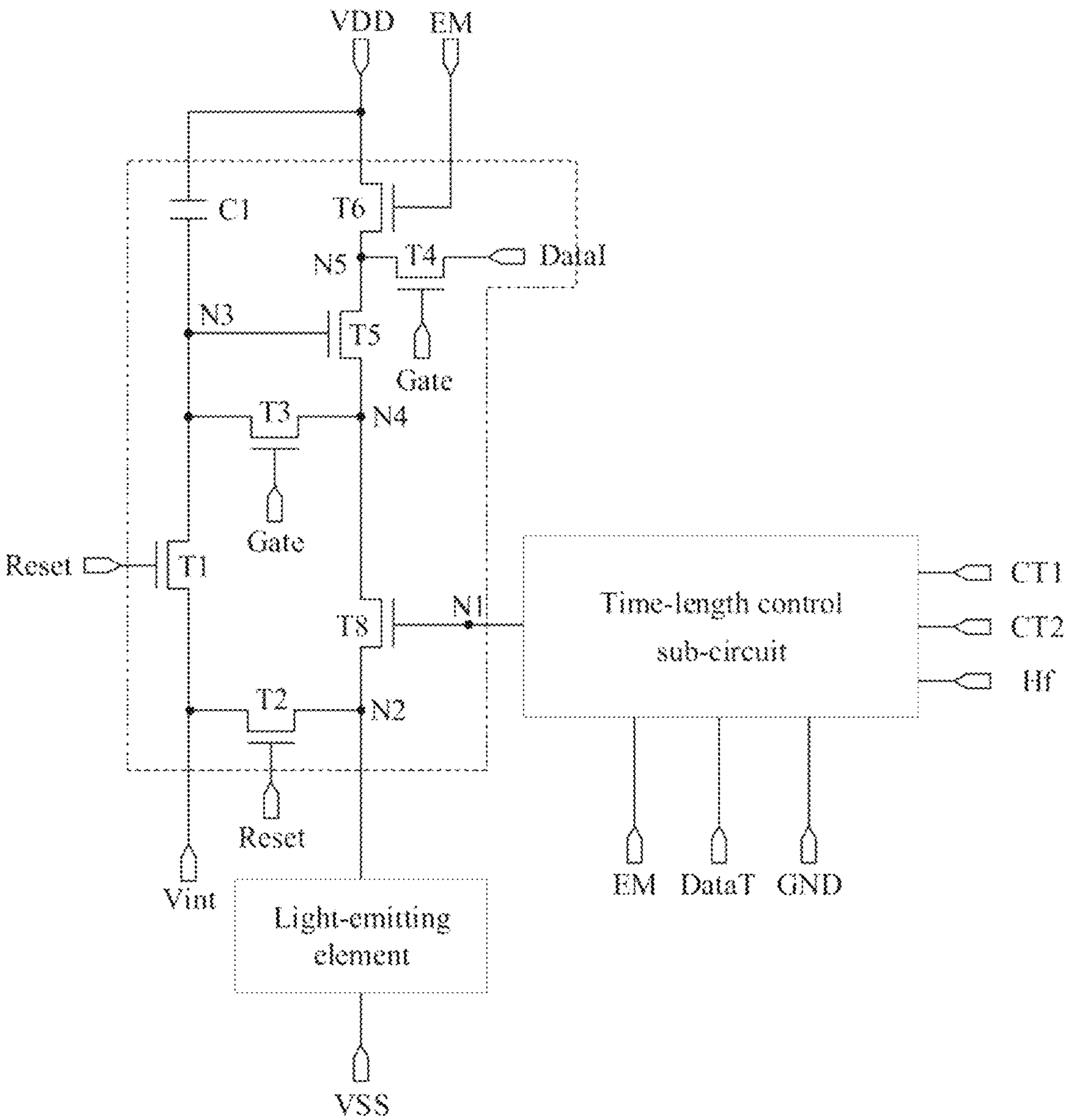
VDD
EM
C1
T6
N5
T4
DataI
N3
T5
Gate
T3
N4
Gate
Reset
T1
T8
N1
Time-length control sub-circuit
CT1
CT2
Hf
T2
N2
Reset
Vint
EM
DataT
GND
Light-emitting element
VSS

FIG. 4

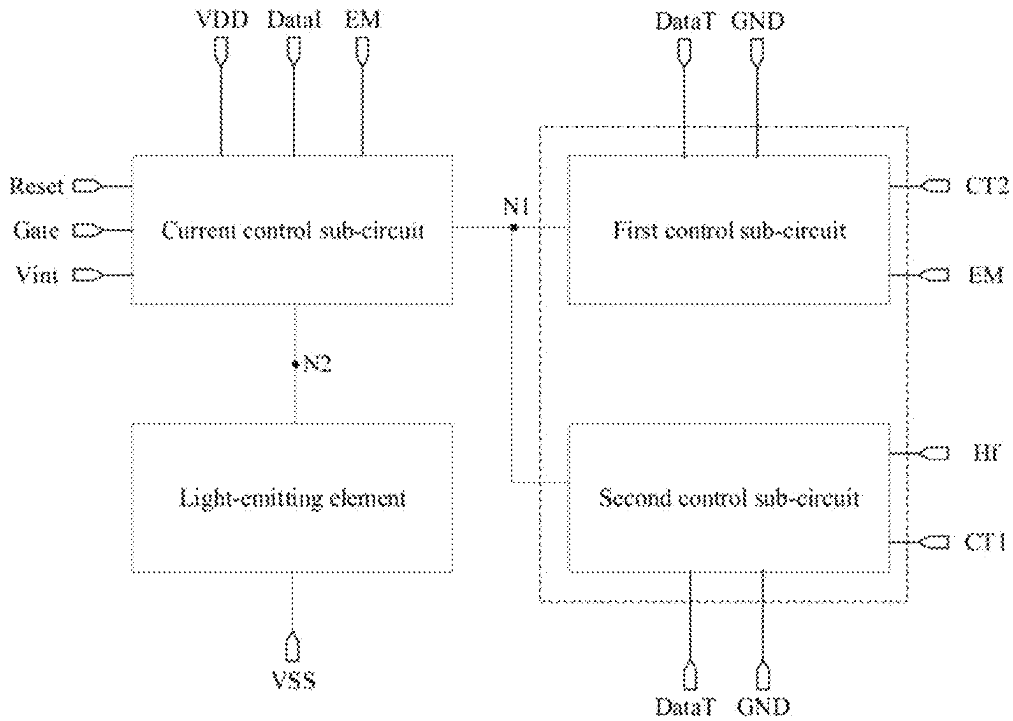
VDD
DataI
EM
DataT
GND
Reset
Gate
Vini
Current control sub-circuit
N1
First control sub-circuit
CT2
EM
N2
Light-emitting element
Second control sub-circuit
Hf
CT1
VSS
DataT
GND

FIG. 5

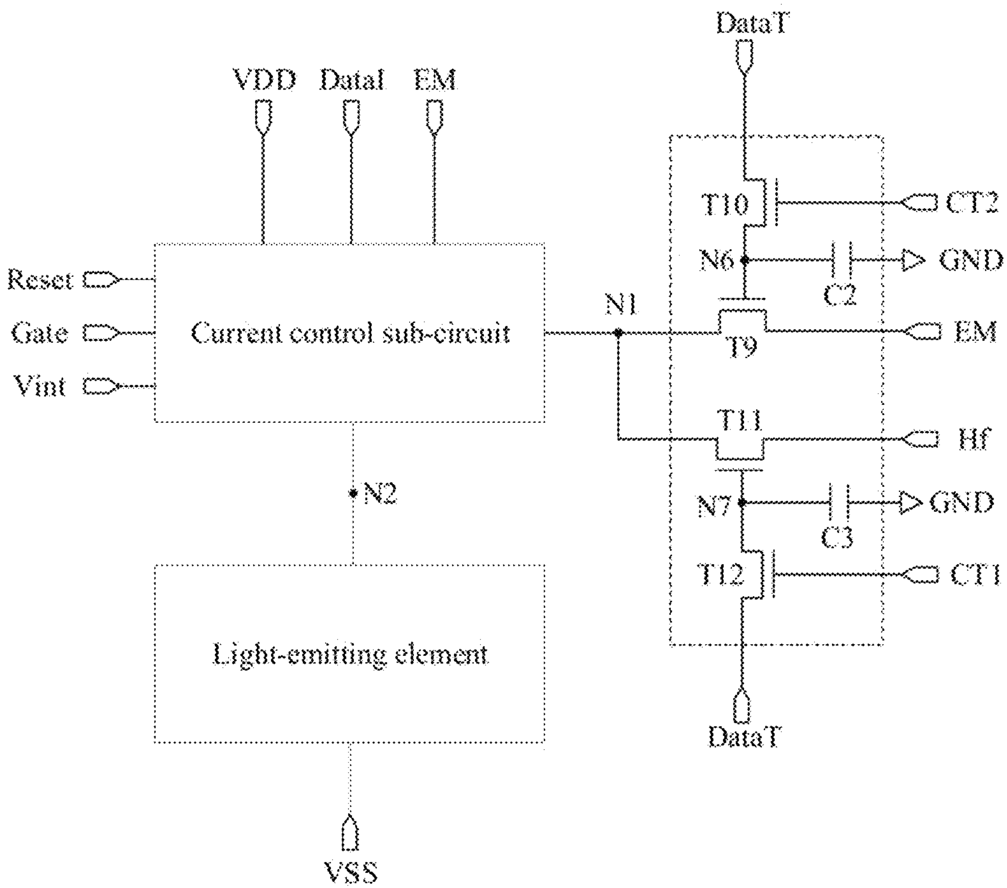
DataT
VDD
DataI
EM
T10
CT2
N6
GND
C2
Reset
Current control sub-circuit
N1
EM
Gate
T9
Vint
T11
Hf
N2
N7
GND
C3
T12
CT1
Light-emitting element
DataT
VSS

FIG. 6

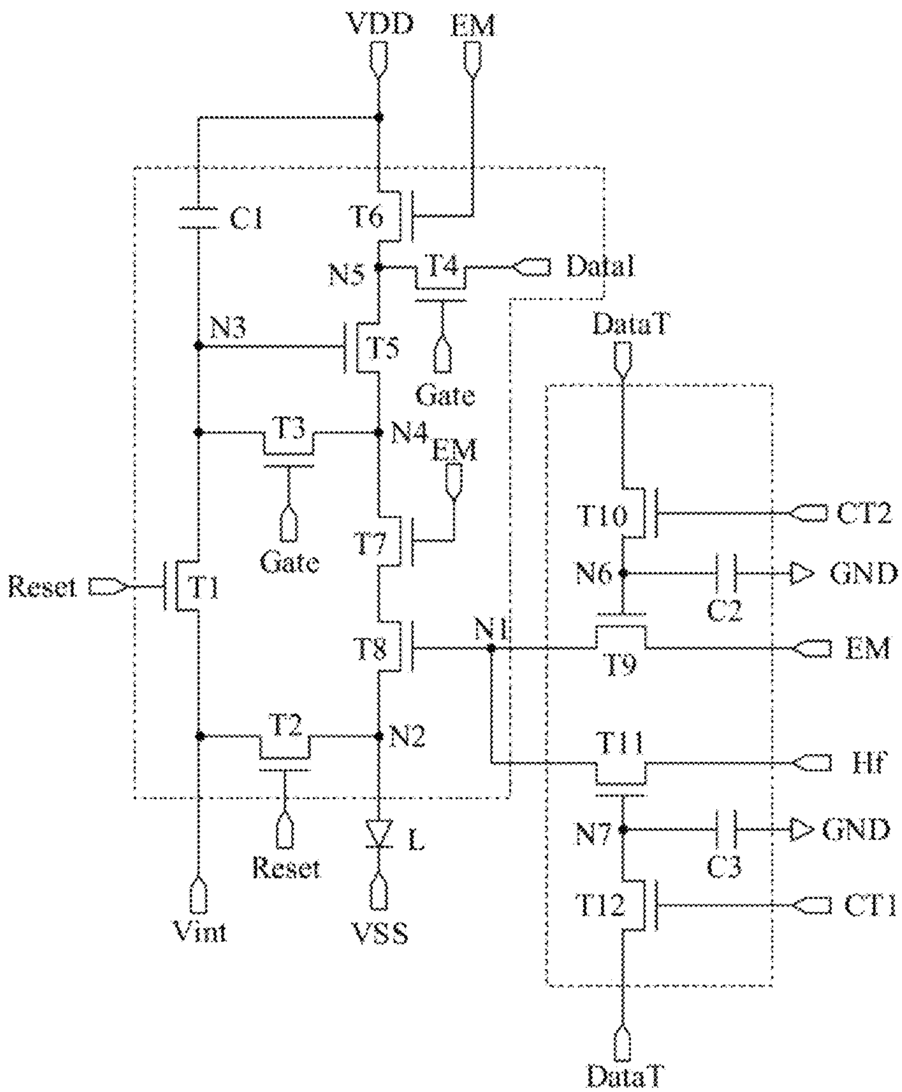
VDD
EM
C1
T6
N5
T4
DataI
N3
T5
Gate
DataT
T3
N4
EM
T10
CT2
T7
Gate
N6
GND
Reset
T1
C2
T8
N1
T9
EM
T2
N2
T11
Hf
N7
GND
L
Reset
C3
T12
CT1
Vint
VSS
DataT

FIG. 7

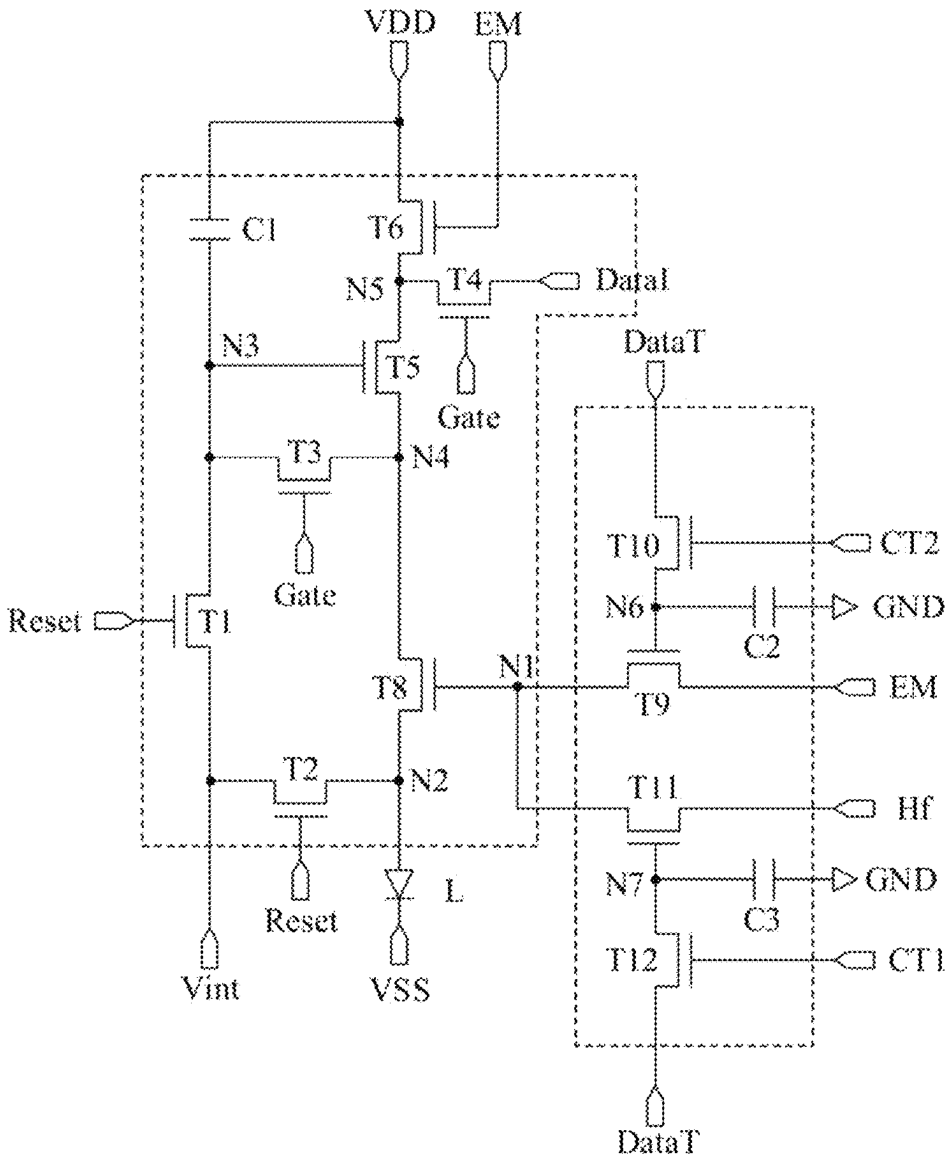
VDD
EM
C1
T6
N5
T4
DataI
N3
T5
Gate
DataT
T3
N4
Gate
T10
CT2
N6
C2
GND
Reset
T1
T8
N1
T9
EM
T2
N2
T11
Hf
N7
C3
GND
Reset
L
T12
CT1
Vint
VSS
DataT

FIG. 8

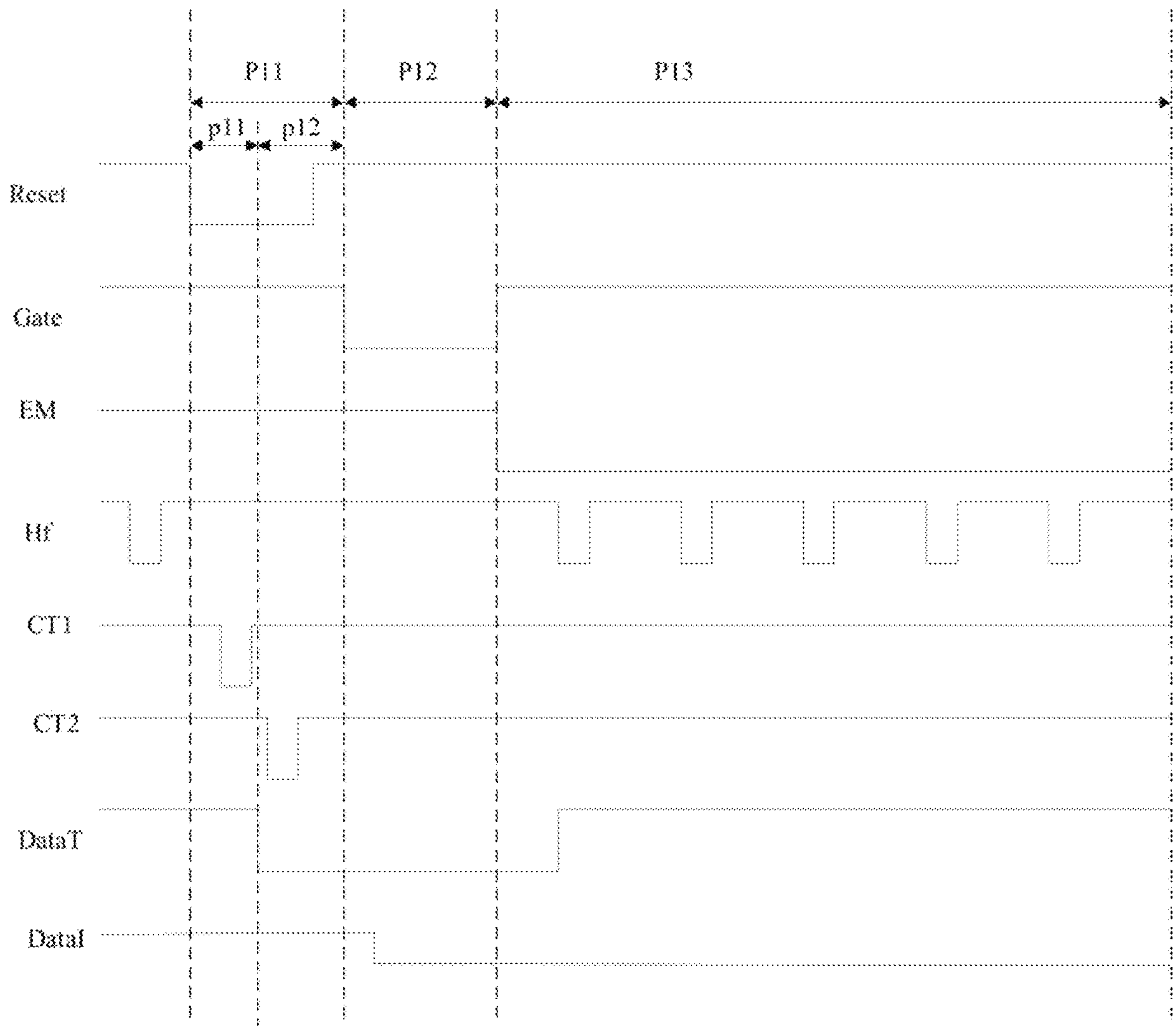

FIG. 9

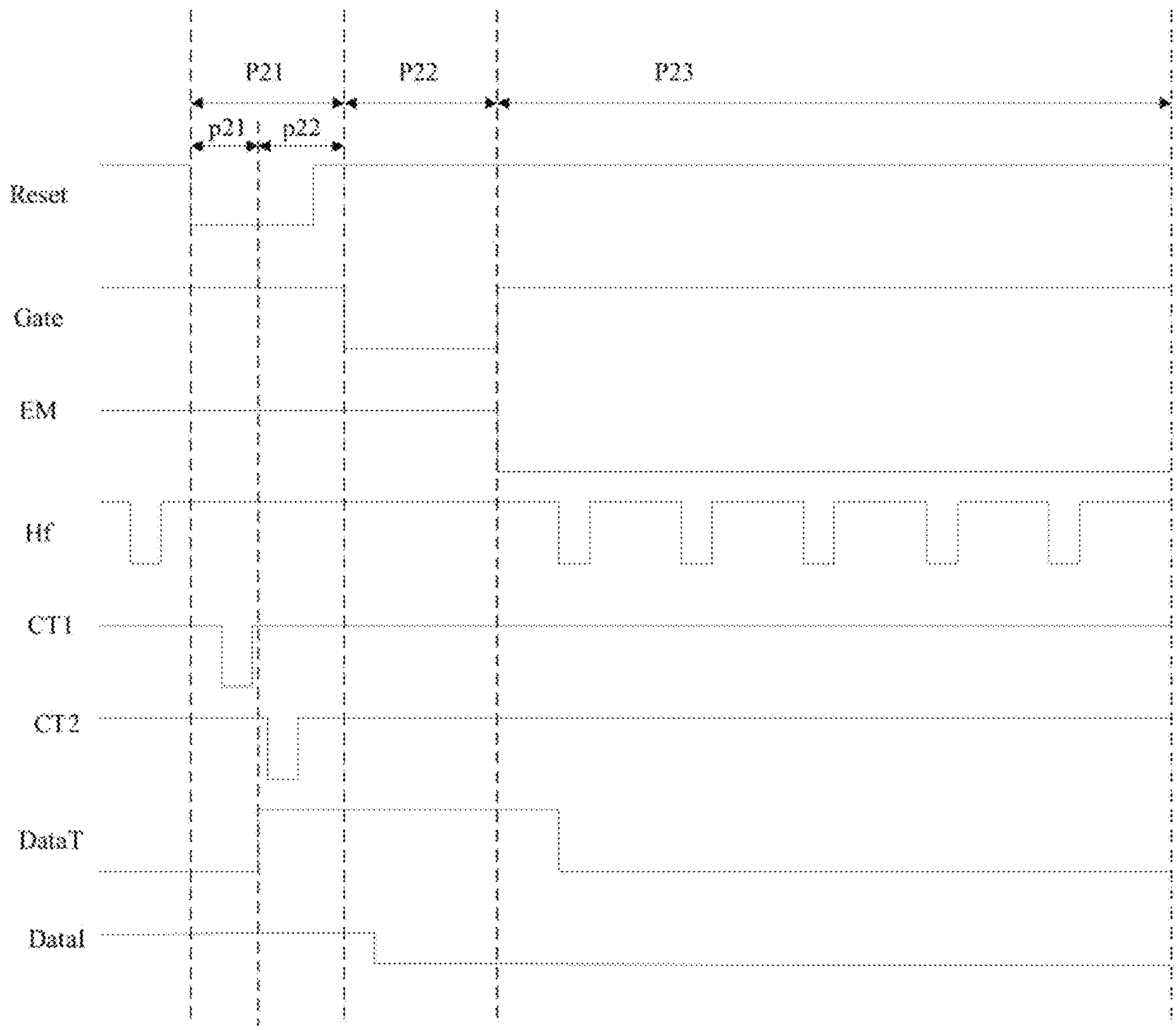

FIG. 10

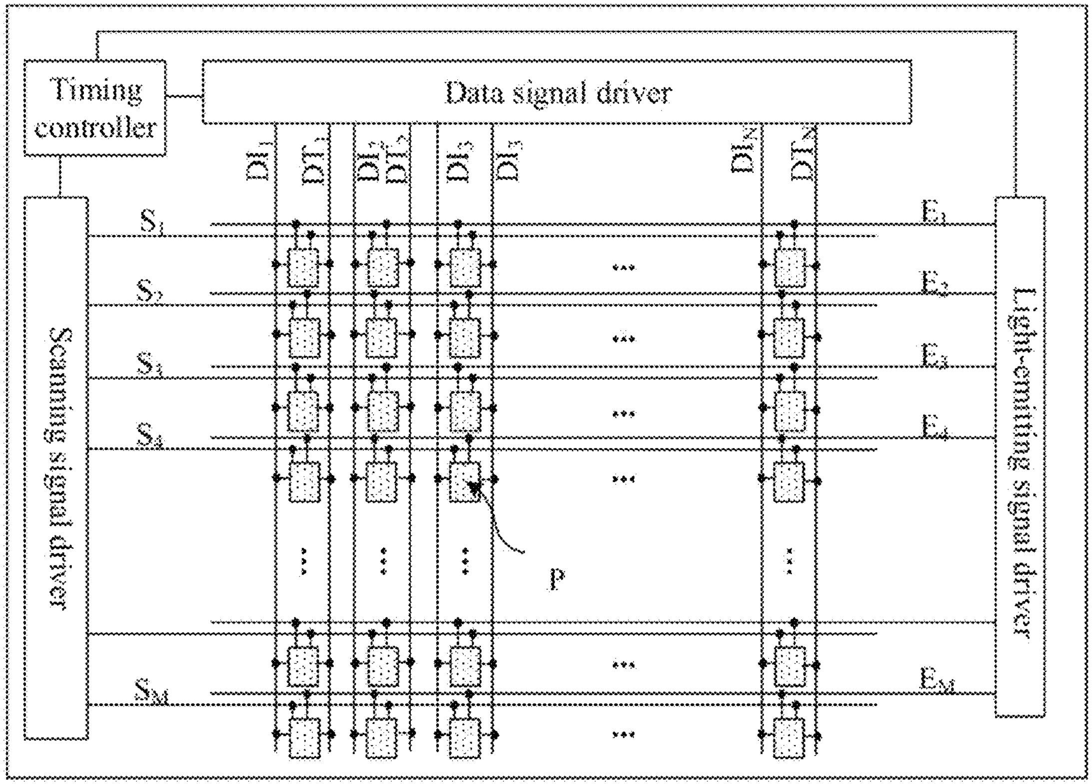
Timing controller
Data signal driver
Scanning signal driver
Light-emitting signal driver
DI1
DT1
DI2
DT2
DI3
DT3
DIN
DTN
S1
S2
S3
S4
SM
E1
E2
E3
E4
EM
P

FIG. 11

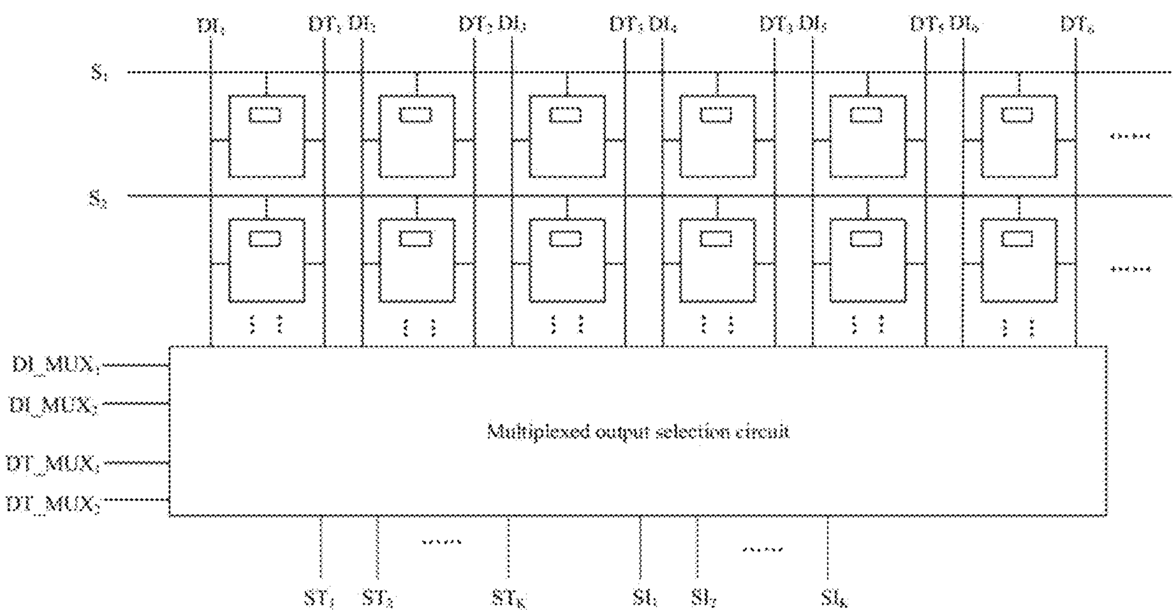
DI1
DT1 DI2
DT2 DI3
DT3 DI4
DT4 DI5
DT5 DI6
DT6
S1
S2
DI_MUX1
DI_MUX2
DT_MUX1
DT_MUX2
Multiplexed output selection circuit
ST1
ST2
STK
SI1
SI2
SIK

FIG. 12

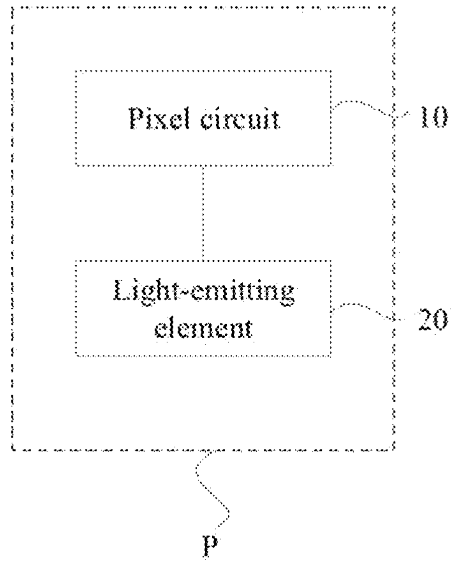
Pixel circuit
10
Light-emitting element
20
P

FIG. 13

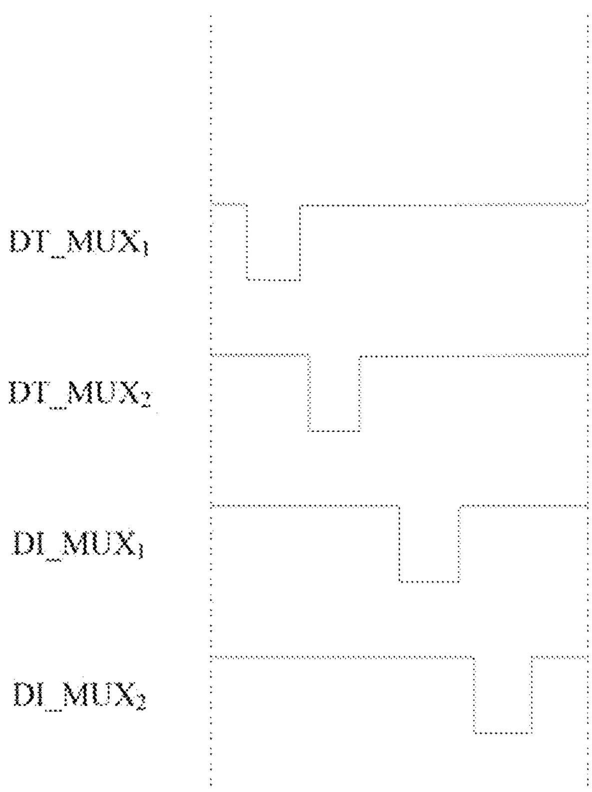
DT_MUX1
DT_MUX2
DI_MUX1
DI_MUX2

FIG. 14

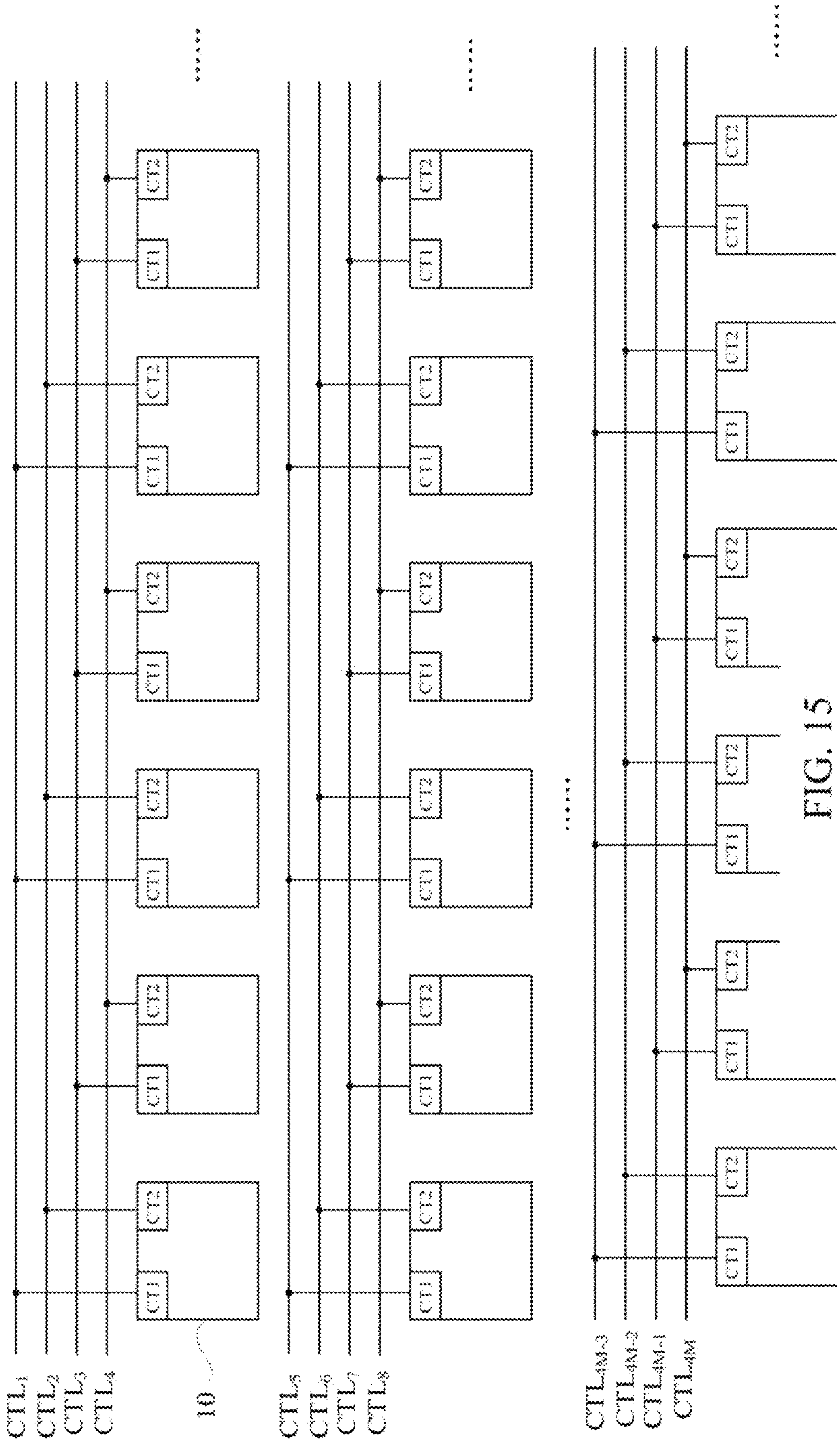
CTL1
CTL2
CTL3
CTL4
10
CTL5
CTL6
CTL7
CTL8
CTL4M-3
CTL4M-2
CTL4M-1
CTL4M
CT1
CT2

FIG. 15

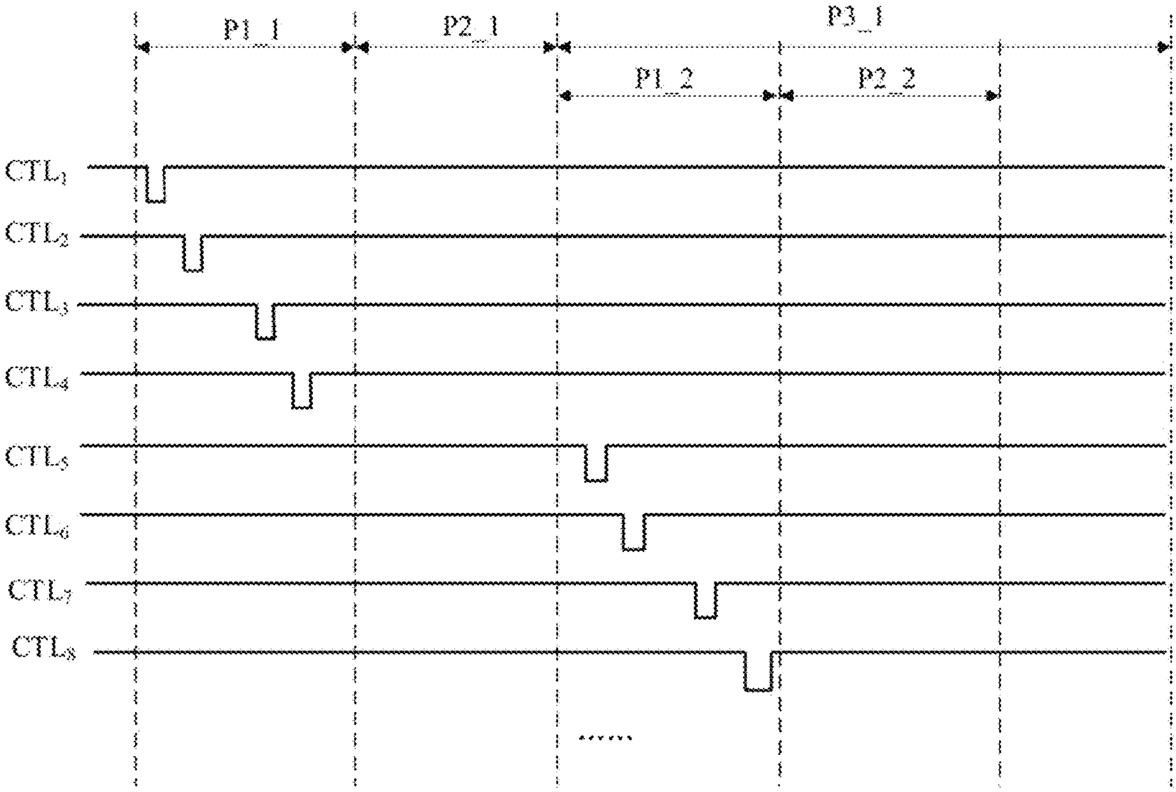

FIG. 16

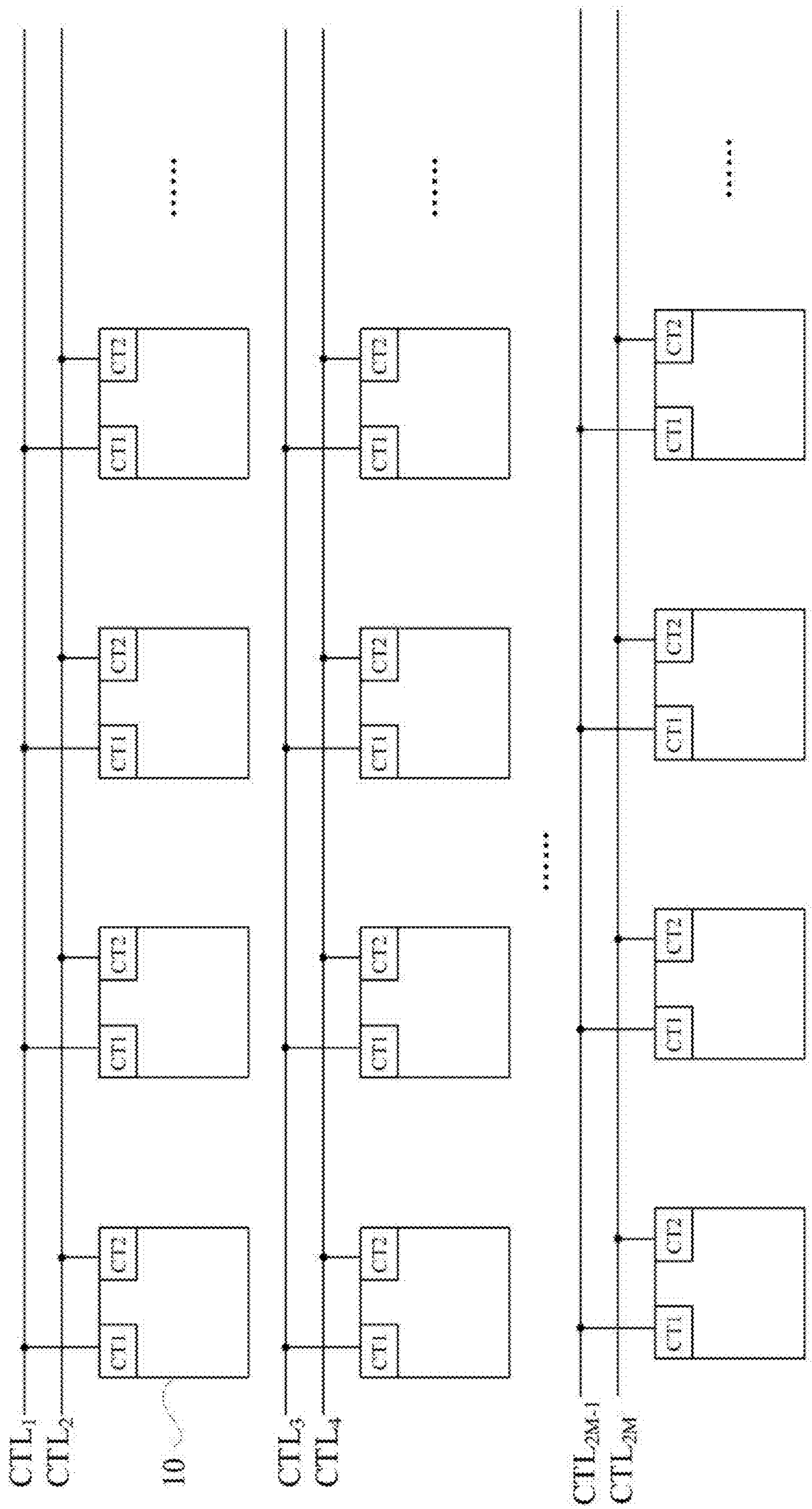

FIG. 17

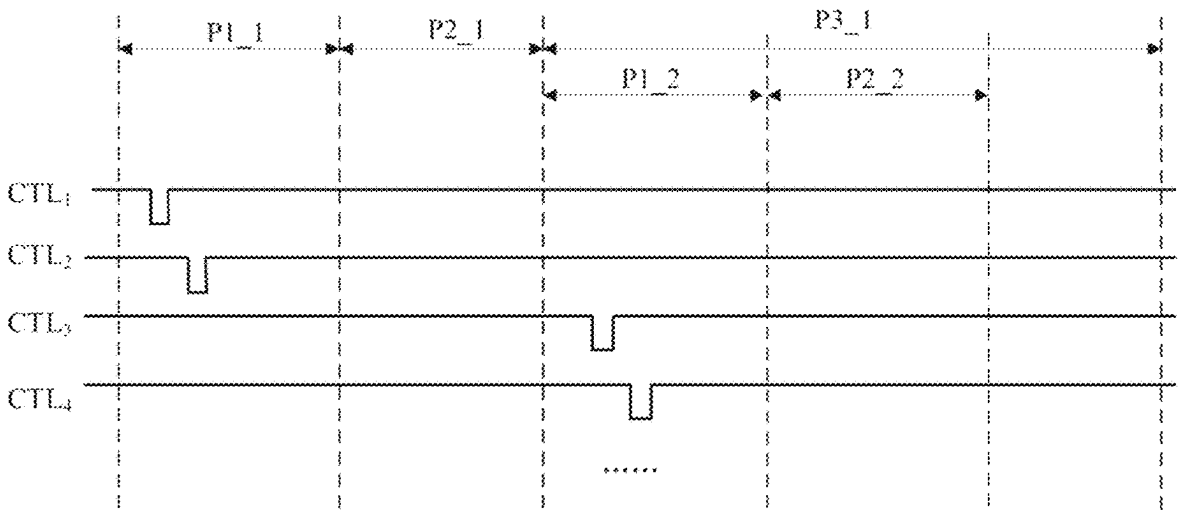

FIG. 18

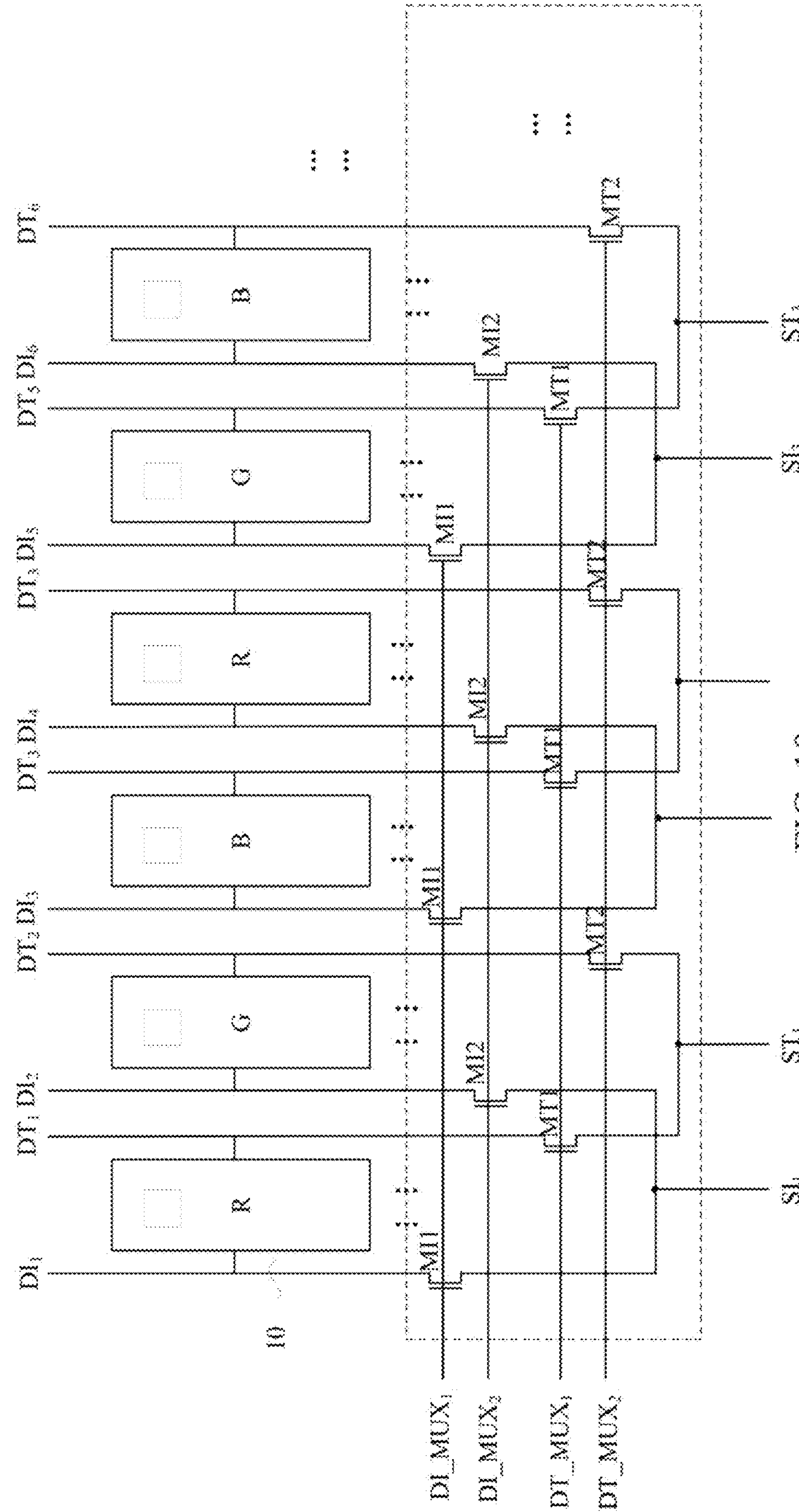
DI1
DT1 DI2
DT2 DI3
DT3 DI4
DT3 DI5
DT5 DI6
DT6
R
G
B
R
G
B
MI1
MI2
MT1
MT2
SI1
ST1
SI3
ST3
10
DI_MUX1
DI_MUX2
DT_MUX1
DT_MUX2

FIG. 19

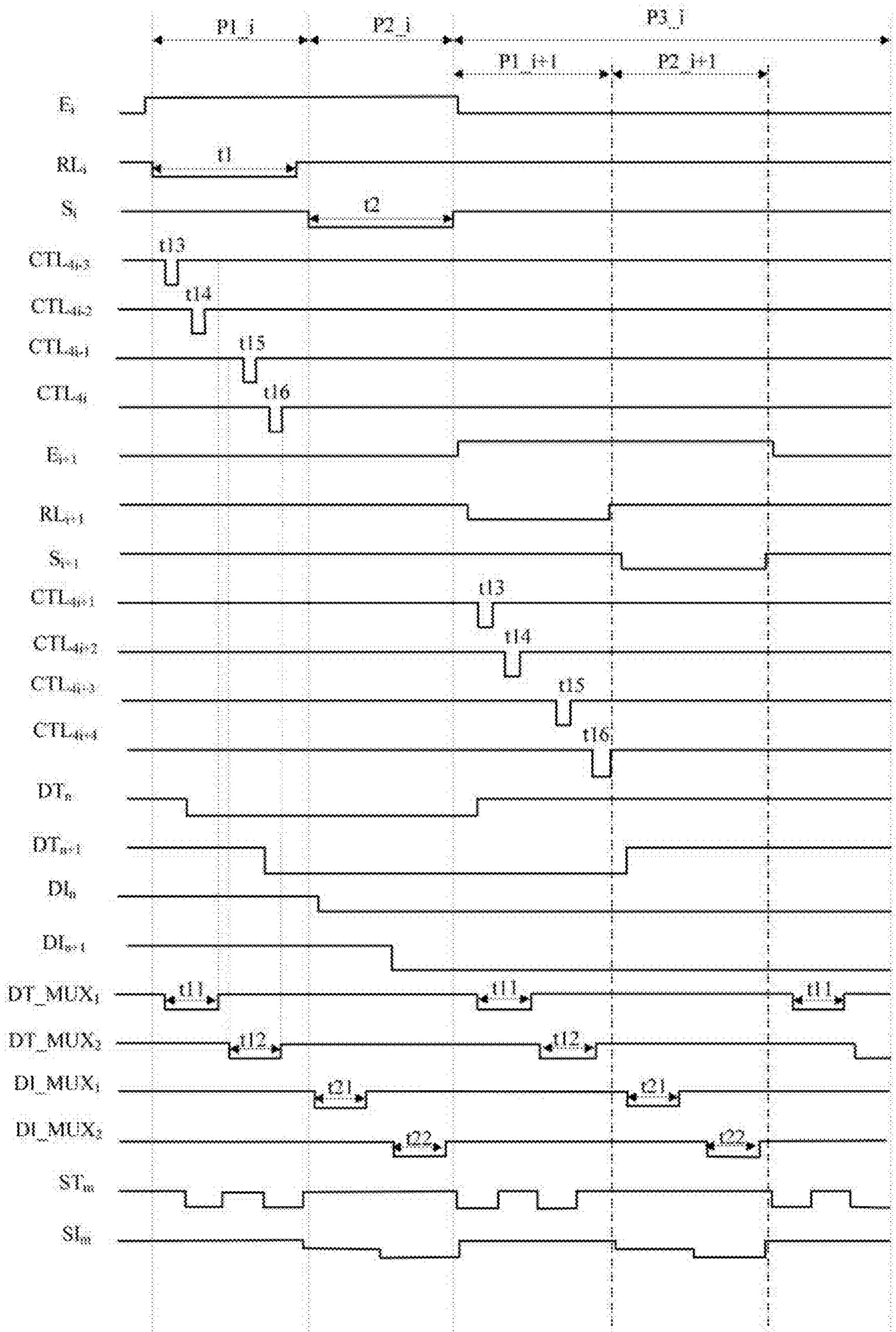
P1_i
P2_i
P3_i
P1_i+1
P2_i+1
Ei
RLi
t1
Si
t2
CTL4i-3
t13
CTL4i-2
t14
CTL4i-1
t15
CTL4i
t16
Ei+1
RLi+1
Si+1
CTL4i+1
t13
CTL4i+2
t14
CTL4i+3
t15
CTL4i+4
t16
DTn
DTn+1
DIn
DIn+1
DT_MUX1
t11
t11
t11
DT_MUX2
t12
t12
DI_MUX1
t21
t21
DI_MUX2
t22
t22
STm
SIm

FIG. 20

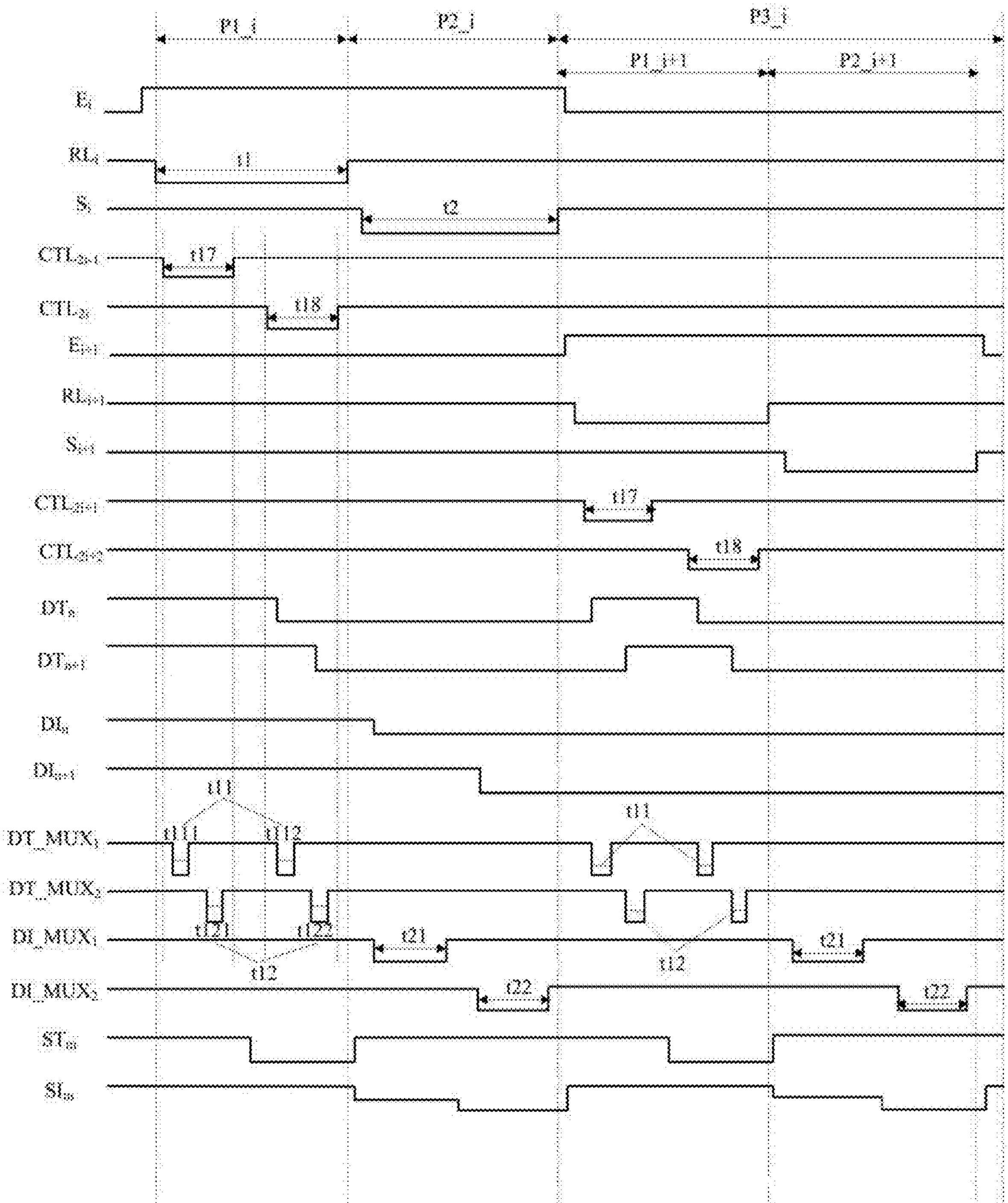
P1_i
P2_i
P3_i
P1_i+1
P2_i+1
E_i
RL_i
t1
S_i
t2
CTL_{2i-1}
t17
CTL_{2i}
t18
E_{i+1}
RL_{i+1}
S_{i+1}
CTL_{2i+1}
t17
CTL_{2i+2}
t18
DT_n
DT_{n+1}
DI_n
DI_{n+1}
t11
t111
t112
DT_MUX_1
DT_MUX_2
t121
t122
DI_MUX_1
t12
t21
DI_MUX_2
t22
ST_m
SI_m

FIG. 21

PIXEL CIRCUIT AND DRIVING METHOD THEREOF, AND DISPLAY PANEL AND DRIVING METHOD THEREOF

CROSS-REFERENCE TO RELATED APPLICATION(S)

This application is a continuation of U.S. application Ser. No. 17/636,897 filed on Feb. 21, 2022, which is a national stage application of PCT Application No. PCT/CN2021/088615, filed on Apr. 21, 2021, the above identified applications are hereby incorporated by reference in their entireties.

TECHNICAL FIELD

Embodiments of the present disclosure relate to, but are not limited to, the technical field of display, and more particularly to a pixel circuit and a drive method for the same, and a display panel and a drive method for the same.

BACKGROUND

At present, the display market is booming. As consumer demand for various display products such as laptops, smart phones, TVs, tablets, smart watches and fitness wristbands continues to increase, more new display products will emerge in the future.

SUMMARY

The below is a summary about the subject matter described in the present disclosure in detail. The summary is not intended to limit the scope of protection of the claims.

According to a first aspect, the present disclosure provides a drive method for a display panel, wherein the display panel includes: pixel circuits arranged in array, a plurality of current data lines, a plurality of time-length data lines, a first current selection signal line, a second current selection signal line, a first time-length selection signal line and a second time-length selection signal line, the pixel circuits are respectively connected with the current data lines and the time-length data lines, at least one current data line is connected with the first current selection signal line or the second current selection signal line, two adjacent current data lines are connected with different current selection signal lines, at least one time-length data line is connected with the first time-length selection signal line or the second time-length selection signal line, and two adjacent time-length data lines are connected with different time-length selection signal lines; the method includes: providing a valid level signal to the first time-length selection signal line, the second time-length selection signal line, the first current selection signal line and the second current selection signal line; wherein, the time for at least two signal lines of the first time-length selection signal line, the second time-length selection signal line, the first current selection signal line and the second current selection signal line to receive the valid level signal do not overlap.

In some possible implementations, the display panel further includes: a reset signal line, a scanning signal line, and a light-emitting signal line; the pixel circuits are respectively connected with the reset signal line, the scanning signal line and the light-emitting signal line; the method further includes: providing a valid level signal to the reset signal line, the scanning signal line and the light-emitting signal line; wherein, the time for at least two signal lines of the reset signal line, the scanning signal line and the light-emitting signal line connected to the same pixel circuit to receive the valid level signal do not overlap.

In some possible implementations, the time for the reset signal line connected to the $(m+1)^{th}$ row of pixel circuits to receive the valid level signal is within the time for the light-emitting signal line connected to the m^{th} row of pixel circuits to receive the valid level signal, herein $1 \leq m \leq M$ and M is the total number of rows of the pixel circuits.

In some possible implementations, the time for the first time-length selection signal line to receive the valid level signal is within the time for the reset signal line connected to at least one row of pixel circuits to receive the valid level signal.

In some possible implementations, the time for the second time-length selection signal line to receive the valid level signal is within the time for the reset signal line connected to at least one row of pixel circuits to receive the valid level signal.

In some possible implementations, the time for the first time-length selection signal line to receive the valid level signal and the time for the second time-length selection signal line to receive the valid level signal do not overlap, and the sum of the time length for the first time-length selection signal line to receive the valid level signal and the time length for the second time-length selection signal line to receive the valid level signal is less than the time length for the reset signal line connected to at least one row of pixel circuits to receive the valid level signal.

In some possible implementations, the time for the first current selection signal line to receive the valid level signal is within the time for the scanning signal line connected to at least one row of pixel circuits to receive the valid level signal.

In some possible implementations, the time for the second current selection signal line to receive the valid level signal is within the time for the scanning signal line connected to at least one row of pixel circuits to receive the valid level signal.

In some possible implementations, the time for the first current selection signal line to receive the valid level signal and the time for the second current selection signal line to receive the valid level signal do not overlap, and the sum of the time length for the first current selection signal line to receive the valid level signal and the time length for the second current selection signal line to receive the valid level signal is less than the time length for the scanning signal line connected to at least one row of pixel circuits to receive the valid level signal.

In some possible implementations, the display panel further includes: 4M control signal lines, the m^{th} row of pixel circuits are connected with the $(4m-3)^{th}$ control signal line, the $(4m-2)^{th}$ control signal line, the $(4m-1)^{th}$ control signal line and $(4m)^{th}$ control signal line, respectively; the method further includes: providing a valid level signal to the control signal lines; when the m^{th} row of pixel units display, the time for the $(4m-3)^{th}$ control signal line to receive the valid level signal, the time for the $(4m-2)^{th}$ control signal line to receive the valid level signal, the time for the $(4m-1)^{th}$ control signal line to receive the valid level signal and the time for the $(4m)^{th}$ control signal line to receive the valid level signal are within the time for the reset signal line connected to the m^{th} row of pixel circuits to receive the valid level signal, and the time for the $(4m-3)^{th}$ control signal line to receive the valid level signal, the time for the $(4m-2)^{th}$ control signal line to receive the valid level signal, the time for the $(4m-1)^{th}$ control signal line to receive the valid level signal and the time for the $(4m)^{th}$ control signal line to receive the valid level signal do not overlap.

In some possible implementations, the pixel circuits in odd columns of the m^{th} row are electrically connected to the $(4m-3)^{t}$ control signal line and the $(4m-2)^{th}$ control signal line respectively, the pixel circuits in even columns of the m^{th} row are electrically connected to the $(4m-1)^{th}$ control signal line and the $(4m)^{th}$ control signal line respectively, the time-length data lines connected to the pixel circuits in odd columns are connected to the first time-length selection signal line, and when the time-length data lines connected to the pixel circuits in even columns are connected to the second time-length selection signal line, the time for the $(4m-3)^{th}$ control signal line to receive the valid level signal and the time for the $(4m-2)^{th}$ control signal line to receive the valid level signal are within the time for the first time-length selection signal line to receive the valid level signal, and the time for the $(4m-1)^{th}$ control signal line to receive the valid level signal and the time for the $(4m)^{th}$ control signal line to receive the valid level signal are within the time for the second time-length selection signal line to receive the valid level signal.

In some possible implementations, the sum of the time length for the $(4m-3)^{th}$ control signal line to receive the valid level signal and the time length for the $(4m-2)^{th}$ control signal line to receive the valid level signal is less than the time length for the first time selection signal line to receive the valid level signal; the sum of the time length for the $(4m-1)^{th}$ control signal line to receive the valid level signal and the time length for the $(4m)^{th}$ control signal line to receive the valid level signal is less than the time length for the second time-length selection signal line to receive the valid level signal.

In some possible implementations, the display panel further includes: 2M control signal lines, the m^{th} row of pixel circuits are connected to the $(2m-1)^{th}$ control signal line and the $(2m)^{th}$ control signal line respectively, and M is the total number of rows of the pixel circuits; the method further includes: providing a valid level signal to the control signal lines; when the m^{th} row of pixel units display, the time for the $(2m-1)^{th}$ control signal line to receive the valid level signal and the time for the $(2m)^{th}$ control signal line to receive the valid level signal are within the time for the reset signal line connected to the m^{th} row of pixel circuits to receive the valid level signal, and the time for the $(2m-1)^{th}$ control signal line to receive the valid level signal and the time for the $(2m)^{th}$ control signal line to receive the valid level signal do not overlap.

In some possible implementations, within the time for the reset signal line connected to at least one row of pixel circuits to receive the valid level signal, the valid level signal received by the first time-length control signal line includes two first pulse signals and the valid level signal received by the second time-length control signal line includes two second pulse signals, the first pulse signals and the second pulse signals are alternately generated; the time for the first time-length control signal line to receive one of the first pulse signals is within the time for one of the control signal lines connected to at least one row of pixel circuits to receive the valid level signal when the at least one row of pixel circuits display, and the time for the first time-length control signal line to receive another first pulse signal is within the time for another control signal line connected to at least one row of pixel circuits to receive the valid level signal when the at least one row of pixel circuits display; the time for the second time-length control signal line to receive one of the second pulse signals is within the time for one of the control signal lines connected to at least one row of pixel circuits to receive the valid level signal when the at least one row of pixel circuits display, and the time for the second time-length control signal line to receive another second pulse signal is within the time for another control signal line connected to at least one row of pixel circuits to receive the valid level signal when the at least one row of pixel circuits display.

In some possible implementations, the sum of the time length for the first pulse signal and the time length for the second pulse signal within the time for one of the control signal lines connected to at least one row of pixel circuits to receive the valid level signal when the at least one row of pixel circuits display is less than the time length for one of the control signal lines connected to at least one row of pixel circuits to receive the valid level signal when the at least one row of pixel circuits display; the sum of the time length for the first pulse signal and the time length for the second pulse signal within the time for another control signal line connected to at least one row of pixel circuits to receive the valid level signal when the at least one row of pixel circuits display is less than the time length for another control signal line connected to at least one row of pixel circuits to receive the valid level signal when the at least one row of pixel circuits display.

After the drawings and the detailed descriptions are read and understood, the other aspects may be comprehended.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompany drawings are used to provide further understanding of the technical solution of the present disclosure, and form a part of the description. The accompany drawings and embodiments of the present disclosure are adopted to explain the technical solution of the present disclosure, and do not form limits to the technical solution of the present disclosure.

FIG. **1** is a schematic structural diagram of a pixel circuit according to an embodiment of the present disclosure.

FIG. **2** is a schematic structural diagram of a current control sub-circuit according to an exemplary embodiment.

FIG. **3** is an equivalent circuit diagram of a current control sub-circuit according to an exemplary embodiment.

FIG. **4** is an equivalent circuit diagram of a current control sub-circuit according to another exemplary embodiment.

FIG. **5** is a schematic structural diagram of a time-length control sub-circuit according to an exemplary embodiment.

FIG. **6** is an equivalent circuit diagram of a time-length control sub-circuit according to an exemplary embodiment.

FIG. **7** is an equivalent circuit diagram of a pixel circuit according to an exemplary embodiment.

FIG. **8** is an equivalent circuit diagram of a pixel circuit according to another exemplary embodiment.

FIG. **9** is a working sequence diagram of the pixel circuit provided in FIG. **7**.

FIG. **10** is another working sequence diagram of the pixel circuit provided in FIG. **7**.

FIG. **11** is a schematic structural diagram of a display panel according to an embodiment of the present disclosure.

FIG. **12** is another schematic structural diagram of a display panel according to an embodiment of the present disclosure.

FIG. **13** is a schematic structural diagram of a pixel unit according to an exemplary embodiment.

FIG. **14** is a sequence diagram of multiple selection signal lines according to an exemplary embodiment.

FIG. **15** is a schematic structural diagram of a display panel according to an exemplary embodiment.

FIG. **16** is a sequence diagram of control signal lines in the display panel provided in FIG. **15**.

FIG. **17** is another schematic structural diagram of a display panel according to an exemplary embodiment.

FIG. **18** is a sequence diagram of control signal lines in the display panel provided in FIG. **17**.

FIG. **19** is an equivalent circuit diagram of a multiplexed output selection circuit according to an exemplary embodiment.

FIG. **20** is a sequence diagram of a display panel according to an exemplary embodiment.

FIG. **21** is another sequence diagram of a display panel according to an exemplary embodiment.

DETAILED DESCRIPTION

To make the objectives, technical solutions, and advantages of the present disclosure clearer, the embodiments of the present disclosure will be described in detail below in combination with the accompany drawings. It is to be noted that the implementations may be implemented in various forms. Those of ordinary skill in the art can easily understand such a fact that modes and contents may be transformed into various forms without departing from the purpose and scope of the present disclosure. Therefore, the present disclosure should not be explained as being limited to the contents recorded in the following implementations only. The embodiments and features in the embodiments of the present disclosure may be randomly combined with each other in case of no conflicts.

In the accompanying drawings, the size of each composition element, the thicknesses of layers, or regions may be exaggerated sometimes for clarity. Therefore, a mode of the present disclosure is not always limited to the size, and the shape and size of each component in the drawings do not reflect the true scale. In addition, the accompanying drawings schematically illustrate ideal examples, and a mode of the present disclosure is not limited to the shapes, numerical values, or the like shown in the drawings.

Ordinal numerals "first", "second", "third", etc., in the specification are set not to form limits in number but only to avoid the confusion of composition elements.

In the specification, for convenience, expressions "central", "above", "below", "front", "back", "vertical", "horizontal", "top", "bottom", "inside", "outside", etc., indicating directional or positional relationships are used to illustrate positional relationships between the composition elements, not to indicate or imply that involved devices or elements are required to have specific orientations and be structured and operated with the specific orientations but only to easily and simply describe the present specification, and thus should not be understood as limits to the present disclosure. The positional relationships between the composition elements may be changed as appropriate according to the direction where each composition element is described. Therefore, appropriate replacements based on situations are allowed, not limited to the expressions in the specification.

In the specification, unless otherwise specified and defined, terms "mounting", "mutual connection", and "connection" should be generally understood. For example, the term may be fixed connection, or detachable connection, or integral connection. The term may be mechanical connection or electric connection. The term may be direct connection, or indirect connection through an intermediate, or communication inside two elements. Those of ordinary skill in the art can understand specific meanings of the above terms in the present disclosure according to specific situations.

In the specification, a transistor refers to an element that at least includes three terminals, i.e., a gate electrode, a drain electrode, and a source electrode. The transistor has a channel region between the drain electrode (drain electrode terminal, drain region, or drain electrode) and the source electrode (source electrode terminal, source region, or source electrode), and a current may flow through the drain electrode, the channel region, and the source region. It is to be noted that in the specification, the channel region refers to a main region that a current flows through.

In the specification, a first electrode may be the drain electrode, and a second electrode may be the source electrode. Alternatively, the first electrode may be a source electrode, and the second electrode may be a drain electrode. In cases that transistors with opposite polarities are used, or a current direction changes during work of a circuit, or the like, functions of the "source electrode" and the "drain electrode" may sometimes be exchanged. Therefore, the "source electrode" and the "drain electrode" may be exchanged in the specification.

In the specification, "electric connection" includes connection of the composition elements through an element with a certain electric action. "An element with a certain electric action" is not particularly limited as long as electric signals between the connected composition elements may be sent and received. Examples of "an element with a certain electric action" not only include an electrode and a line, but also include a switch element such as a transistor, a resistor, an inductor, a capacitor, another element with various functions, etc.

For a high-resolution display product, among multiple pixels arranged in an array, pixels in the same column share one signal line, thereby saving a wiring space and reducing the difficulty in process implementation.

In the case that the pixel of the high-resolution display product includes a micro-inorganic light-emitting diode, the micro-inorganic light-emitting diode is a current-type drive element; under the driving of a lower current density, color coordinate drift and low external quantum efficiency will occur, resulting in poor uniformity of brightness. Thus, it is difficult to accurately represent a low gray tone only by controlling current amplitude. Therefore, it is required to control a time length of a current provided to the micro-inorganic light-emitting diode on the basis of controlling the amplitude of the current provided to the micro-inorganic light-emitting diode so as to achieve accurate gray tone display. It can be understood that, in some embodiments, a pixel circuit used to provide a drive signal (a current signal) to the micro-inorganic light-emitting diode includes at least two types of data terminals, namely a current data terminal and a time-length data terminal. The current data terminal is configured to provide the current signal of different amplitudes to the micro-inorganic light-emitting diode, and the time-length data terminal is configured to control the time length for providing the above-mentioned current signal to the micro-inorganic light-emitting diode. The inventor found that in low-gray tone display, the micro-inorganic light-emitting diode may enter a black state after emitting light for a short period of time in one frame, such that the human eyes can clearly capture flickering, which results in a reduction of a display effect of the display product.

FIG. **1** is a schematic structural diagram of a pixel circuit according to an embodiment of the present disclosure. As shown in FIG. **1**, a pixel circuit **10** according to the embodiment of the present disclosure is configured to drive a light-emitting element. The pixel circuit includes: a current control sub-circuit and a time-length control sub-circuit.

The current control sub-circuit is electrically connected to a current data terminal DataI, a scanning signal terminal Gate, a reset signal terminal Reset, an initial signal terminal Vint, a light-emitting signal terminal EM, a first power terminal VDD, a first node **N1**, and a second node **N2**, respectively, and is configured to provide a drive current to the second node **N2** under the control of the current data terminal DataI, the scanning signal terminal Gate, the reset signal terminal Reset, the initial signal terminal Vint, the light-emitting signal terminal EM, the first power terminal VDD, and the first node **N1**. The time-length control sub-circuit is electrically connected to a first control terminal CT**1**, a second control terminal CT**2**, a time-length data terminal DataT, a ground terminal GND, a light-emitting signal terminal EM, a high-frequency input terminal Hf, and the first node **N1**, respectively, and is configured to provide a signal of the light-emitting signal terminal EM or a signal of the high-frequency input terminal Hf to the first node **N1** under the control of the first control terminal CT**1**, the second control terminal CT**2**, the time-length data terminal DataT, and the ground terminal GND. The light-emitting element is electrically connected to the second node **N2** and a second power terminal VSS, respectively.

The time for the first control terminal CT**1** to receive a valid level signal is within the time for the reset signal terminal Reset to receive a valid level signal. The time for the second control terminal CT**2** to receive a valid level signal is within the time for the reset signal terminal Reset to receive the valid level signal, and the time for the first control terminal CT**1** to receive the valid level signal and the time for the second control terminal CT**2** to receive the valid level signal do not coincide. Exemplarily, when the signal of the reset signal terminal Reset is a valid level signal, the signal of the first control terminal CT**1** is a valid level signal, the signal of the second control terminal CT**2** is a valid level signal, and the signal of the first control terminal CT**1** and the signal of the second control terminal CT**2** are valid level signals at different times.

In an exemplary embodiment, the signal of the time-length data terminal DataT is written when the signal of the reset signal terminal Reset is the valid level signal.

In an exemplary embodiment, the first power terminal VDD is configured to transmit a direct-current voltage signal and continuously provide a high-level signal, such as a direct-current high voltage. The second power terminal VSS is configured to transmit a direct-current voltage signal and continuously provide a low-level signal, for example, a direct-current low voltage.

In an exemplary embodiment, the signal of the high-frequency input terminal Hf is a pulse signal. For example, in an image frame, the signal of the high-frequency input terminal Hf is of multiple pulses. Exemplarily, a frequency of the signal of the high-frequency input terminal Hf is greater than a frequency of the signal of the light-emitting signal terminal EM. For example, in a unit time, the number of times the signal of the high-frequency input terminal has a valid level time period is greater than the number of times the signal of the light-emitting signal terminal has a valid level time period.

In an exemplary embodiment, the signal of the high-frequency input terminal Hf is a high-frequency pulse signal. For example, the frequency of the signal of the high-frequency input terminal Hf ranges from 3000 Hz to 60000 Hz, for example, it may be 3000 Hz or 60000 Hz. For example, the frequency of the light-emitting signal terminal EM ranges from 60 Hz to 120 Hz, for example, it may be 60 Hz or 120 Hz. For example, the frame frequency of the display panel is 60 Hz, that is, within 1s, the display panel can display 60 frames of images, and the display time length of each frame of image is equal. In this way, when a signal frequency of the high-frequency input terminal Hf is 3000 Hz and a signal frequency of the light-emitting signal terminal EM is 60 Hz, in an image frame, if one light-emitting element is required to emit low-gray tone light, the light-emitting element can receive about 50 valid time periods of the high-frequency signal in a light emitting phase (i.e., within a time period during which the light-emitting signal terminal EM provides a valid signal).

In an exemplary embodiment, the signal of the light-emitting signal terminal or high-frequency input terminal is transmitted to the current control sub-circuit by controlling the time-length control sub-circuit, to control an ON (Start) frequency of the current control sub-circuit, and to control a frequency of forming a conductive path by the pixel circuit and the light-emitting element, so that a frequency of transmitting the drive current to the light-emitting element can be controlled. The sum of time lengths for forming the conductive path is a total time length of the light-emitting element. The total time length of the light-emitting element is a superposition of sub-time lengths of the light-emitting element when forming the conductive path multiple times. Thus, a luminous intensity of the light-emitting element can be controlled by controlling amplitude of the drive current, thereby realizing gray tone display of the pixel unit.

In an exemplary embodiment, a value range of the amplitude of the drive current may be within a range where the light-emitting element works with high and stable luminous efficiency, the uniformity of color coordinates is good, and a dominant wavelength of emission is stable, for example, a range where the drive current amplitude is large. Therefore, the signal provided by the current data terminal when a gray tone displayed by the light-emitting element connected to the pixel circuit is greater than a threshold gray tone may have the same value range as the signal provided by the current data terminal when the gray tone displayed by the light-emitting element connected to the pixel unit is smaller than the threshold gray tone.

In an exemplary embodiment, when the gray tone displayed by the light-emitting element connected to the pixel unit is greater than the threshold gray tone, the time-length control sub-circuit transmits the signal of the light-emitting signal terminal to the current control sub-circuit. The current control sub-circuit is always in an ON state under the control of the light-emitting signal terminal, the pixel circuit and the light-emitting element always form the conductive path, and the drive current is continuously transmitted to the light-emitting element. Because the gray tone displayed by the light-emitting element connected to the pixel unit is greater than the threshold gray tone, the amplitude of the drive current corresponding thereto is relatively high, the light-emitting elements works under the driving of the drive signal with the higher amplitude, and the working efficiency of the light-emitting element is ensured.

In an exemplary embodiment, when the gray tone displayed by the light-emitting element connected to the pixel unit is less than the threshold gray tone, the time-length control sub-circuit transmits the signal of the high-frequency input terminal to the current control sub-circuit. The current control sub-circuit is an ON or OFF state alternatively under the control of the high-frequency pulse signal of the high-frequency input terminal, so that the drive current is intermittently transmitted to the light-emitting element, and the light-emitting element periodically receives the drive current. For example, the light-emitting element stops for a period of time after receiving the drive current for a period of time, and then stops again for a period of time after receiving the drive current for a period of time. Thus, the time for forming the conductive path by the pixel circuit and the light-emitting element is shortened, and the time for transmitting the drive circuit to the light-emitting element is shortened. Therefore, when the gray tone displayed by the pixel unit where the pixel circuit is located is less than the threshold gray tone, the amplitude of the drive current can be maintained in a higher value range or kept at a larger fixed amplitude value; by changing the working time length of the light-emitting element, the pixel unit is allowed to realize the corresponding low-gray tone display, thereby improving the working efficiency of the light-emitting element, avoiding the problem of low working efficiency and high power consumption of the light-emitting element when the low-gray tone display is implemented with small current amplitude, avoiding reduction of the gray tone display uniformity, avoiding color shift in display, and improving the display effect of the display panel.

Exemplarily, the amplitude of the drive current is related to a current data signal received at the current data terminal. The current data signal may be a signal that enables the light-emitting element to have a higher working efficiency. For example, the current data signal may be a signal that changes within a higher amplitude range or a signal with a higher fixed amplitude. In this case, the pixel circuit controls, by the current control sub-circuit and the time-length control sub-circuit, the time and frequency of transmitting the drive current to the light-emitting element, to control the corresponding gray tone display of the pixel unit.

In an image frame, in the case where the gray tone displayed by the light-emitting element connected to the pixel unit is less than the threshold gray tone, compared with the circumstance that flickering to the human eyes will be obvious when the light-emitting element works for a short time and then being idle for a long time, the light-emitting element in the embodiment of the present disclosure is intermittently in a working state, that is, the light-emitting element is in a working state and an idle state alternatively with a high alternating frequency, that is, the light-emitting element has a high light-dark alternating frequency, and flickering is not easy to be observed by the human eyes, thereby improving the display effect.

The pixel circuit according to the embodiment of the present disclosure is configured to drive the light-emitting element to emit light, including: a current control sub-circuit and a time-length control sub-circuit. The current control sub-circuit is electrically connected to a current data terminal, a scanning signal terminal, a reset signal terminal, an initial signal terminal, a light-emitting signal terminal, a first power terminal, a first node, and a second node, respectively, and is configured to provide a drive current to the second node under the control of the current data terminal, the scanning signal terminal, the reset signal terminal, the initial signal terminal, the light-emitting signal terminal, the first power terminal, and the first node. The time-length control sub-circuit is electrically connected to a first control terminal, a second control terminal, a time-length data terminal, a ground terminal, a light-emitting signal terminal, a high-frequency input terminal, and the first node, respectively, and is configured to provide the signal of the light-emitting signal terminal or the signal of the high-frequency input terminal to the first node under the control of the first control terminal, the second control terminal, the time-length data terminal, and the ground terminal. The light-emitting element is electrically connected to the second node and the second power terminal, respectively. The time for the first control terminal to receive a valid level signal is within the time for the reset signal terminal to receive a valid level signal, the time for the second control terminal to receive a valid level signal is within the time for the reset signal terminal to receive the valid level signal, and the time for the first control terminal to receive the valid level signal and the time for the second control terminal to receive the valid level signal do not coincide. In the present disclosure, through the cooperation of the current control sub-circuit and the time-length control sub-circuit, when the light-emitting element connected to the pixel circuit displays a low gray tone, the light-emitting element has a higher alternating frequency of light and dark, the flickering is not easy to be observed by the human eyes, and accordingly the display effect of the display product is improved.

In an exemplary embodiment, a first electrode of the light-emitting element is electrically connected to the second node **N2**. A second electrode of the light-emitting element is electrically connected to the second power terminal VSS. The first electrode of the light-emitting element is an anode thereof, and the second electrode of the light-emitting element is a cathode thereof.

FIG. **2** is a schematic structural diagram of a current control sub-circuit according to an exemplary embodiment. As shown in FIG. **2**, in an exemplary embodiment, the current control sub-circuit may include: a node control sub-circuit, a writing sub-circuit, a drive sub-circuit, and a light-emitting control sub-circuit. The node control sub-circuit is electrically connected to the scanning signal terminal Gate, the reset signal terminal Reset, the initial signal terminal Vint, the second node N**2**, a third node N**3**, a fourth node N**4**, and the first power terminal VDD, respectively, and is configured to provide a signal of the initial signal terminal Vint to the second node N**2** and the third node N**3** and provide a signal of the third node N**3** to the fourth node N**4** under the control of the reset signal terminal Reset and the scanning signal terminal Gate. The writing sub-circuit is electrically connected to the scanning signal terminal Gate, the current data terminal DataI, and a fifth node N**5**, respectively, and is configured to provide a signal of the current data terminal DataI to the fifth node N**5** under the control of the scanning signal terminal Gate. The drive sub-circuit is electrically connected to the third node N**3**, the fourth node N**4**, and the fifth node N**5**, respectively, and is configured to provide the drive current to the fourth node N**4** under the control of the third node N**3** and the fifth node N**5**. The light-emitting control sub-circuit is electrically connected to the light-emitting signal terminal EM, the first node N**1**, the second node N**2**, the fourth node N**4**, the fifth node N**5**, and the first power terminal VDD, respectively, and is configured to provide a signal of the first power terminal VDD to the fifth node N**5** and provide a signal of the fourth node N**4** to the second node N**2** under the control of the first node N**1** and the light-emitting signal terminal EM.

FIG. **3** is an equivalent circuit diagram of a current control sub-circuit according to an exemplary embodiment. As shown in FIG. **3**, in the current control sub-circuit according to the exemplary embodiment, the node control sub-circuit may include: a first transistor T**1**, a second transistor T**2**, a third transistor T**3**, and a first capacitor C**1**; the writing sub-circuit may include: a fourth transistor T**4**; the drive sub-circuit may include: a fifth transistor T**5**; and the light-emitting control sub-circuit may include: a sixth transistor T6, a seventh transistor T7, and an eighth transistor T8.

A control electrode of the first transistor T1 is electrically connected to the reset signal terminal Reset, a first electrode of the first transistor T1 is electrically connected to the initial signal terminal Vint, and a second electrode of the first transistor T1 is electrically connected to a third node N3. A control electrode of the second transistor T2 is electrically connected to the reset signal terminal Reset, a first electrode of the second transistor T2 is electrically connected to the initial signal terminal Vint, and a second electrode of the second transistor T2 is electrically connected to the second node N2. A control electrode of the third transistor T3 is electrically connected to the scanning signal terminal Gate, a first electrode of the third transistor T3 is electrically connected to the third node N3, and a second electrode of the third transistor T3 is electrically connected to a fourth node N4. A first terminal of the first capacitor C1 is electrically connected to the third node N3, and a second terminal of the first capacitor C1 is electrically connected to the first power terminal VDD. A control electrode of the fourth transistor T4 is electrically connected to the scanning signal terminal Gate, a first electrode of the fourth transistor T4 is electrically connected to a fifth node N5, and a second electrode of the fourth transistor T4 is electrically connected to the current data terminal DataI. A control terminal of the fifth transistor T5 is electrically connected to the third node N3, a first electrode of the fifth transistor T5 is electrically connected to the fifth node N5, and a second electrode of the fifth transistor T5 is electrically connected to the fourth node N4. A control terminal of the sixth transistor T6 is electrically connected to the light-emitting signal terminal EM, a first electrode of the sixth transistor T6 is electrically connected to the first power terminal VDD, and a second electrode of the sixth transistor T6 is electrically connected to the fifth node N5. A control electrode of the seventh transistor T7 is electrically connected to the light-emitting signal terminal EM, a first electrode of the seventh transistor T7 is electrically connected to the fourth node N4, and a second electrode of the seventh transistor T7 is electrically connected to a first electrode of the eighth transistor T8. A control electrode of the eighth transistor T8 is electrically connected to the first node N1, and a second electrode of the eighth transistor T8 is electrically connected to the second node N2.

In an exemplary embodiment, the first transistor T1, the second transistor T2, the third transistor T3, the fourth transistor T4, the sixth transistor T6, the seventh transistor T7, and the eighth transistor T8 may be switch transistors.

In an exemplary embodiment, the fifth transistor T5 may be a drive transistor.

FIG. 4 is an equivalent circuit diagram of a current control sub-circuit according to another exemplary embodiment. As shown in FIG. 4, in the current control sub-circuit according to the exemplary embodiment, the node control sub-circuit may include: a first transistor T1, a second transistor T2, a third transistor T3, and a first capacitor C1; the writing sub-circuit may include: a fourth transistor T4; the drive sub-circuit may include: a fifth transistor T5; and the light-emitting control sub-circuit may include: a sixth transistor T6, and an eighth transistor T8. A control electrode of the first transistor T1 is electrically connected to the reset signal terminal Reset, a first electrode of the first transistor T1 is electrically connected to the initial signal terminal Vint, and a second electrode of the first transistor T1 is electrically connected to a third node N3. A control electrode of the second transistor T2 is electrically connected to the reset signal terminal Reset, a first electrode of the second transistor T2 is electrically connected to the initial signal terminal Vint, and a second electrode of the second transistor T2 is electrically connected to the second node N2. A control electrode of the third transistor T3 is electrically connected to the scanning signal terminal Gate, a first electrode of the third transistor T3 is electrically connected to the third node N3, and a second electrode of the third transistor T3 is electrically connected to a fourth node N4. A first terminal of the first capacitor C1 is electrically connected to the third node N3, and a second terminal of the first capacitor C1 is electrically connected to the first power terminal VDD. A control electrode of the fourth transistor T4 is electrically connected to the scanning signal terminal Gate, a first electrode of the fourth transistor T4 is electrically connected to a fifth node N5, and a second electrode of the fourth transistor T4 is electrically connected to the current data terminal DataI. A control terminal of the fifth transistor T5 is electrically connected to the third node N3, a first electrode of the fifth transistor T5 is electrically connected to the fifth node N5, and a second electrode of the fifth transistor T5 is electrically connected to the fourth node N4. A control terminal of the sixth transistor T6 is electrically connected to the light-emitting signal terminal EM, a first electrode of the sixth transistor T6 is electrically connected to the first power terminal VDD, and a second electrode of the sixth transistor T6 is electrically connected to the fifth node N5. A control electrode of the eighth transistor T8 is electrically connected to the first node N1, a first electrode of the eighth transistor T8 is electrically connected to the fourth node, and a second electrode of the eighth transistor T8 is electrically connected to the second node N2.

In an exemplary embodiment, the first transistor T1, the second transistor T2, the third transistor T3, the fourth transistor T4, the sixth transistor T6, and the eighth transistor T8 may be switch transistors.

In an exemplary embodiment, the fifth transistor T5 may be a drive transistor.

FIG. 3 and FIG. 4 illustrate exemplary structures of the current control sub-circuit. The implementation of the current control sub-circuit is not limited to this.

FIG. 5 is a schematic structural diagram of a time-length control sub-circuit according to an exemplary embodiment. As shown in FIG. 5, the time-length control sub-circuit according to an exemplary embodiment includes: a first control sub-circuit and a second control sub-circuit. The first control sub-circuit is electrically connected to the time-length data terminal DataT, the second control terminal CT2, the ground terminal GND, the light-emitting signal terminal EM, and the first node N1, respectively, and is configured to provide the signal of the light-emitting signal terminal EM to the first node N1 under the control of the time-length data terminal DataT, the second control terminal CT2, and the ground terminal GND. The second control sub-circuit is electrically connected to the time-length data terminal DataT, the first control terminal CT1, the ground terminal GND, the high-frequency input terminal Hf, and the first node N1, respectively, and is configured to provide the signal of the high-frequency input terminal Hf to the first node N1 under the control of the time-length data terminal DataT, the first control terminal CT1, and the ground terminal GND.

FIG. 6 is an equivalent circuit diagram of a time-length control sub-circuit according to an exemplary embodiment. As shown in FIG. 6, in the time-length control sub-circuit according to an exemplary embodiment, the first control sub-circuit may include: a ninth transistor T9, a tenth transistor T10, and a second capacitor C2; and the second control sub-circuit may include: an eleventh transistor T11, a twelfth transistor T12, and a third capacitor C3.

A control electrode of the ninth transistor T9 is electrically connected to a sixth node N6, a first electrode of the ninth transistor T9 is electrically connected to the light-emitting signal terminal EM, and a second electrode of the ninth transistor T9 is electrically connected to the first node N1. A control electrode of the tenth transistor T10 is electrically connected to the second control terminal CT2, a first electrode of the tenth transistor T10 is electrically connected to the time-length data terminal DataT, and a second electrode of the tenth transistor T10 is electrically connected to the sixth node N6. A first terminal of the second capacitor C2 is electrically connected to the sixth node N6, and a second terminal of the second capacitor C2 is electrically connected to the ground terminal GND. A control electrode of the eleventh transistor T11 is electrically connected to a seventh node N7, a first electrode of the eleventh transistor T11 is electrically connected to the high-frequency input terminal Hf, and a second electrode of the eleventh transistor T11 is electrically connected to the first node N1. A control electrode of the twelfth transistor T12 is electrically connected to the first control terminal CT1, a first electrode of the twelfth transistor T12 is electrically connected to the time-length data terminal DataT, and a second electrode of the twelfth transistor T12 is electrically connected to the seventh node N7. A first terminal of the third capacitor C3 is electrically connected to the seventh node N7, and a second terminal of the third capacitor C3 is electrically connected to the ground terminal GND.

In an exemplary embodiment, the ninth transistor T9, the tenth transistor T10, the eleventh transistor T11, and the twelfth transistor T12 may be switch transistors.

FIG. 6 illustrates an exemplary structure of the time-length control sub-circuit. The implementation of the time-length control sub-circuit is not limited to this.

In an exemplary embodiment, the light-emitting element includes a current-driven device which may use a current-type light-emitting diode, for example, a Micro light-emitting Diode (Micro LED for short), or a Mini light-emitting Diode (Mini LED for short), or an Organic light-emitting Diode (OLED for short), or a Quantum light-emitting Diode (QLED for short).

FIG. 7 is an equivalent circuit diagram of a pixel circuit according to an exemplary embodiment. As shown in FIG. 7, in the pixel circuit according to an exemplary embodiment, the current control sub-circuit may include: a first transistor T1, a second transistor T2, a third transistor T3, a first capacitor C1, a fourth transistor T4, a fifth transistor T5, a sixth transistor T6, a seventh transistor T7, and an eighth transistor T8; and the time-length control sub-circuit may include: a ninth transistor T9, a tenth transistor T10, a second capacitor C2, an eleventh transistor T11, a twelfth transistor T12, and a third capacitor C3.

A control electrode of the first transistor T1 is electrically connected to the reset signal terminal Reset, a first electrode of the first transistor T1 is electrically connected to the initial signal terminal Vint, and a second electrode of the first transistor T1 is electrically connected to the third node N3. A control electrode of the second transistor T2 is electrically connected to the reset signal terminal Reset, a first electrode of the second transistor T2 is electrically connected to the initial signal terminal Vint, and a second electrode of the second transistor T2 is electrically connected to the second node N2. A control electrode of the third transistor T3 is electrically connected to the scanning signal terminal Gate, a first electrode of the third transistor T3 is electrically connected to the third node N3, and a second electrode of the third transistor T3 is electrically connected to the fourth node N4. A first terminal of the first capacitor C1 is electrically connected to the third node N3, and a second terminal of the first capacitor C1 is electrically connected to the first power terminal VDD. A control electrode of the fourth transistor T4 is electrically connected to the scanning signal terminal Gate, a first electrode of the fourth transistor T4 is electrically connected to the fifth node N5, and a second electrode of the fourth transistor T4 is electrically connected to the current data terminal DataI. A control terminal of the fifth transistor T5 is electrically connected to the third node N3, a first electrode of the fifth transistor T5 is electrically connected to the fifth node N5, and a second electrode of the fifth transistor T5 is electrically connected to the fourth node N4. A control terminal of the sixth transistor T6 is electrically connected to the light-emitting signal terminal EM, a first electrode of the sixth transistor T6 is electrically connected to the first power terminal VDD, and a second electrode of the sixth transistor T6 is electrically connected to the fifth node N5. A control electrode of the seventh transistor T7 is electrically connected to the light-emitting signal terminal EM, a first electrode of the seventh transistor T7 is electrically connected to the fourth node N4, and a second electrode of the seventh transistor T7 is electrically connected to a first electrode of the eighth transistor T8. A control electrode of the eighth transistor T8 is electrically connected to the first node N1, and a second electrode of the eighth transistor T8 is electrically connected to the second node N2. A control electrode of the ninth transistor T9 is electrically connected to the sixth node N6, a first electrode of the ninth transistor T9 is electrically connected to the light-emitting signal terminal EM, and a second electrode of the ninth transistor T9 is electrically connected to the first node N1. A control electrode of the tenth transistor T10 is electrically connected to the second control terminal CT2, a first electrode of the tenth transistor T10 is electrically connected to the time-length data terminal DataT, and a second electrode of the tenth transistor T10 is electrically connected to the sixth node N6. A first terminal of the second capacitor C2 is electrically connected to the sixth node N6, and a second terminal of the second capacitor C2 is electrically connected to the ground terminal GND. A control electrode of the eleventh transistor T11 is electrically connected to the seventh node N7, a first electrode of the eleventh transistor T11 is electrically connected to the high-frequency input terminal Hf, and a second electrode of the eleventh transistor T11 is electrically connected to the first node N1. A control electrode of the twelfth transistor T12 is electrically connected to the first control terminal CT1, a first electrode of the twelfth transistor T12 is electrically connected to the time-length data terminal DataT, and a second electrode of the twelfth transistor T12 is electrically connected to the seventh node N7. A first terminal of the third capacitor C3 is electrically connected to the seventh node N7, and a second terminal of the third capacitor C3 is electrically connected to the ground terminal GND.

In an exemplary embodiment, the first transistor T1 to the twelfth transistor T12 may be P-type transistors, or may be N-type transistors. Adopting the same type of transistors in the pixel circuit may simplify the process flow, reduce the process difficulties of the display panel, and improve the yield of the product.

In some possible implementations, the first transistor T1 to the twelfth transistor T12 may include P-type transistors and N-type transistors.

FIG. 8 is an equivalent circuit diagram of a pixel circuit according to another exemplary embodiment. As shown in FIG. 8, in the pixel circuit according to an exemplary embodiment, the current control sub-circuit may include: a first transistor T1, a second transistor T2, a third transistor T3, a first capacitor C1, a fourth transistor T4, a fifth transistor T5, a sixth transistor T6, and an eighth transistor T8. The time-length control sub-circuit may include: a ninth transistor T9, a tenth transistor T10, a second capacitor C2, an eleventh transistor T11, a twelfth transistor T12, and a third capacitor C3.

A control electrode of the first transistor T1 is electrically connected to the reset signal terminal Reset, a first electrode of the first transistor T1 is electrically connected to the initial signal terminal Vint, and a second electrode of the first transistor T1 is electrically connected to the third node N3. A control electrode of the second transistor T2 is electrically connected to the reset signal terminal Reset, a first electrode of the second transistor T2 is electrically connected to the initial signal terminal Vint, and a second electrode of the second transistor T2 is electrically connected to the second node N2. A control electrode of the third transistor T3 is electrically connected to the scanning signal terminal Gate, a first electrode of the third transistor T3 is electrically connected to the third node N3, and a second electrode of the third transistor T3 is electrically connected to the fourth node N4. A first terminal of the first capacitor C1 is electrically connected to the third node N3, and a second terminal of the first capacitor C1 is electrically connected to the first power terminal VDD. A control electrode of the fourth transistor T4 is electrically connected to the scanning signal terminal Gate, a first electrode of the fourth transistor T4 is electrically connected to the fifth node N5, and a second electrode of the fourth transistor T4 is electrically connected to the current data terminal DataI. A control terminal of the fifth transistor T5 is electrically connected to the third node N3, a first electrode of the fifth transistor T5 is electrically connected to the fifth node N5, and a second electrode of the fifth transistor T5 is electrically connected to the fourth node N4. A control terminal of the sixth transistor T6 is electrically connected to the light-emitting signal terminal EM, a first electrode of the sixth transistor T6 is electrically connected to the first power terminal VDD, and a second electrode of the sixth transistor T6 is electrically connected to the fifth node N5. A control electrode of the eighth transistor T8 is electrically connected to the first node N1, a first electrode of the eighth transistor T8 is electrically connected to the fourth node N4, and a second electrode of the eighth transistor T8 is electrically connected to the second node N2. A control electrode of the ninth transistor T9 is electrically connected to the sixth node N6, a first electrode of the ninth transistor T9 is electrically connected to the light-emitting signal terminal EM, and a second electrode of the ninth transistor T9 is electrically connected to the first node N1. A control electrode of the tenth transistor T10 is electrically connected to the second control terminal CT2, a first electrode of the tenth transistor T10 is electrically connected to the time-length data terminal DataT, and a second electrode of the tenth transistor T10 is electrically connected to the sixth node N6. A first terminal of the second capacitor C2 is electrically connected to the sixth node N6, and a second terminal of the second capacitor C2 is electrically connected to the ground terminal GND. A control electrode of the eleventh transistor T11 is electrically connected to the seventh node N7, a first electrode of the eleventh transistor T11 is electrically connected to the high-frequency input terminal Hf, and a second electrode of the eleventh transistor T11 is electrically connected to the first node N1. A control electrode of the twelfth transistor T12 is electrically connected to the first control terminal CT1, a first electrode of the twelfth transistor T12 is electrically connected to the time-length data terminal DataT, and a second electrode of the twelfth transistor T12 is electrically connected to the seventh node N7. A first terminal of the third capacitor C3 is electrically connected to the seventh node N7, and a second terminal of the third capacitor C3 is electrically connected to the ground terminal GND.

In an exemplary embodiment, the first transistor T1 to the sixth transistor T6, and the eighth transistor T8 to the twelfth transistor T12 may be P-type transistors or may be N-type transistors. Adopting the same type of transistors in the pixel circuit may simplify the process flow, reduce the process difficulties of the display panel, and improve the yield of the product.

In an exemplary embodiment, the first transistor T1 to the sixth transistor T6, and the eighth transistor T8 to the twelfth transistor T12 may include P-type transistors and N-type transistors.

In an exemplary embodiment, the time-length data terminal DataT receives a valid level signal at the time when the first control terminal CT1 receives the valid level signal or when the second control terminal CT2 receives the valid level signal. The signal of the time-length data terminal DataT is a valid level signal when the time for the first control terminal CT1 to receive the valid level signal and the time for the second control terminal CT2 to receive the valid level signal are different.

In an exemplary embodiment, when a gray tone displayed by the light-emitting element connected to the pixel circuit is greater than a threshold gray tone, the time for the time-length data terminal to receive the valid level signal is within the time for the second control terminal to receive the valid level signal. Exemplarily, in a case where the light-emitting element connected to the pixel circuit displays a medium and high gray tone, when the signal of the second control terminal is a valid level signal, the signal of the time-length data terminal is a valid level signal.

In an exemplary embodiment, when a gray tone displayed by the light-emitting element connected to the pixel circuit is less than a threshold gray tone, the time for the time-length data terminal to receive the valid level signal is within the time for the first control terminal to receive the valid level signal. Exemplarily, in a case where the light-emitting element connected to the pixel circuit displays a low gray tone, when the signal of the first control terminal is a valid level signal, the signal of the time-length data terminal is a valid level signal, and a control signal can be provided to the first node through the high-frequency input terminal; the high-frequency pulse signal of the high-frequency input terminal controls the light-emitting time length, and a short light-emitting time length is dispersed to one frame of time, so that the flickering caused when the gray tone of the displayed content of the pixel unit is less than the threshold gray tone is reduced.

A pixel circuit according to an exemplary embodiment will be described below through a working process of the pixel circuit.

Taking an example that the first transistor T1 to the twelfth transistor T12 are all P-type transistors in the pixel circuit provided in the FIG. 7, FIG. 9 is a working sequence diagram of the pixel circuit provided in FIG. 7, and FIG. 10 is another working sequence diagram of the pixel circuit provided in FIG. 7. FIG. 9 is a working sequence diagram of the pixel circuit in a case where a gray tone displayed by a light-emitting element connected to the pixel circuit is greater than a threshold gray tone. FIG. **10** is a working sequence diagram of the pixel circuit in a case where a gray tone displayed by a light-emitting element connected to the pixel unit is less than a threshold gray tone. As shown in FIG. **7**, FIG. **9** and FIG. **10**, the pixel circuit involved in an exemplary embodiment includes: 11 switch transistors (T**1** to T**4**, and T**6** to T**12**), 1 driving transistor (T**5**), 3 capacitor units (C**1** to C**3**), 9 input terminals (Gate, DataT, DataI, Reset, Vint, EM, Hf, CT**1** and CT**2**) and **3** power terminals (GND, VDD and VSS).

When the gray tone displayed by the light-emitting element connected to the pixel unit is greater than the threshold gray tone, as shown in FIG. **7** and FIG. **9**, the working process of the pixel circuit includes: an initialization phase, a writing phase, and a light-emitting phase.

A first phase P**11**, i.e., the initialization phase, includes a first sub-phase p**11** and a second sub-phase p**12**.

In the first sub-phase p**11**, the signal of the reset signal terminal Reset is a low-level signal, the first transistor T**1** is switched on, so that the signal of the initial signal terminal Vint is written into the third node N**3** to reset the third node N**3** and charge the first capacitor C**1**; the second transistor T**2** is switched on, so that the signal of the initial signal terminal Vint is written into the second node N**2**, the second node N**2** is electrically connected to an anode of a light-emitting element L, to reset the anode of the light-emitting element L so as to eliminate residual charge of the anode of the light-emitting element L. The signal of the first control terminal CT**1** is a low-level signal, the twelfth transistor T**12** is switched on, so that a signal of the time-length data terminal DataT is written into the seventh node N**7** and the third capacitor C**3** is charged. Because the signal of the time-length data terminal DataT is a high-level signal, the eleventh transistor T**11** is cut off, and the signal of the high-frequency input terminal Hf cannot be written into the first node N**1**. In this phase, the signal of the second control terminal CT**2** is a high-level signal such that the tenth transistor T**10** is cut off.

In the second sub-phase p**12**, the signal of the reset signal terminal Reset is a low-level signal, the first transistor T**1** is switched on, so that the signal of the initial signal terminal Vint is written into the third node N**3** to reset the third node N**3** and charge the first capacitor C**1**; the second transistor T**2** is switched on, so that the signal of the initial signal terminal Vint is written into the second node N**2**, the second node N**2** is electrically connected to an anode of a light-emitting element L, to reset the anode of the light-emitting element L so as to eliminate residual charge of the anode of the light-emitting element L. The signal of the second control terminal CT**2** is a low-level signal, the tenth transistor T**10** is switched on, so that the signal of the time-length data terminal DataT is written into the sixth node N**6** and the second capacitor C**2** is charged. Because the signal of the time-length data terminal DataT is a low-level signal, the ninth transistor T**9** is cut off, and the signal of the light-emitting signal terminal EM is written into the first node N**1**.

In a second phase P**12**, i.e., the writing phase, the signal of the scanning signal terminal Gate is a low-level signal, the fourth transistor T**4** is switched on, the signal of the current data terminal DataI is written into the fifth node N**5**, and the third transistor T**3** is switched on, then a level V**5** of the fifth node N**5**=Vd, where Vd is a voltage value of the signal of the current data terminal DataI, the first capacitor C**1** starts to discharge to charge the third node N**3** until a level V**3** of the third node N**3**=Vd+Vth, where Vth is a threshold voltage of the fifth transistor T**5**, and at this point, the fifth transistor T**5** is cut off. The second capacitor C**2** keeps a potential of the signal of the sixth node N**6** unchanged, and the ninth transistor T**9** remains on. The signal of the light-emitting signal terminal EM is written into the first node N**1**.

In a third phase P**13**, i.e., the light-emitting phase, the signal of the light-emitting signal terminal EM is a low-level signal, the sixth transistor T**6** is switched on, and at this point, the level of the fifth node N**5** is V**5**=Vdd, where Vdd is a voltage value of the signal at the first power supply terminal VDD; the seventh transistor T**7** is switched on, the second capacitor C**2** keeps the potential of the signal of the sixth node N**6** unchanged, the ninth transistor T**9** remains ON, the signal of the light-emitting signal terminal EM is written into the first node N**1**, and the eighth transistor T**8** is switched on. Since a voltage value of the third node N**3** is V**3**=Vd+Vth, the fifth transistor T**5** is switched on, and the drive current flows into the light-emitting element L.

According to a current formula when the drive transistor is saturated, it can be obtained that the drive current IDLED flowing through the light-emitting element L satisfies the following equations.

$$
\begin{aligned}
I_{OLED} &= (1/2)K(V_{GS} - Vth)^2 \\
&= (1/2)K(V3 - V5 - Vth)^2 \\
&= (1/2)K(Vd + Vth - Vdd - Vth)^2 \\
&= (1/2)K(Vd - Vdd)^2
\end{aligned}
$$

K is a fixed constant related to process parameters and geometric dimensions of the drive transistor, and VGS is a gate-source voltage difference of the drive transistor.

It can be seen from the derivation of the above current formula that in the light-emitting phase, the drive current output by the fifth transistor T**5** is not affected by the threshold voltage of the fifth transistor T**5**, and is only related to the signal of the current data terminal and the signal of the first power terminal. Therefore, the impact of the threshold voltage of the drive transistor on the drive current is eliminated, uniformity of the display brightness of the display product is ensured, and the display effect is improved.

The working process of the pixel circuit as shown in the pixel circuit in FIG. **7** is substantially the same as that of the pixel circuit in FIG. **8**, which will not be repeated here.

When the gray tone displayed by the light-emitting element connected to the pixel unit is less than the threshold gray tone, as shown in FIG. **7** and FIG. **10**, the working process of the pixel circuit includes: an initialization phase, a writing phase, and a light-emitting phase.

A first phase P**21**, i.e., the initialization phase, includes a first sub-phase p**21** and a second sub-phase p**22**.

In the first sub-phase p**21**, the signal of the reset signal terminal Reset is a low-level signal, the first transistor T**1** is switched on, so that the signal of the initial signal terminal Vint is written into the third node N**3** to reset the third node N**3** and charge the first capacitor C**1**; the second transistor T**2** is switched on, so that the signal of the initial signal terminal Vint is written into the second node N**2**, the second node N**2** is electrically connected to an anode of a light-emitting element L, to reset the anode of the light-emitting element L so as to eliminate residual charge of the anode of the light-emitting element L. The signal of the first control terminal CT**1** is a low-level signal, the twelfth transistor T**12** is switched on, so that a signal of the time-length data terminal DataT is written into the seventh node **N7** and the third capacitor C**3** is charged. Because the signal of the time-length data terminal DataT is a low-level signal, the eleventh transistor T**11** is switched on, and the signal of the high-frequency input terminal Hf is written into the first node N**1**. In this phase, the signal of the second control terminal CT**2** is a high-level signal such that the tenth transistor T**10** is cut off.

In the second sub-phase p**22**, the signal of the reset signal terminal Reset is a low-level signal, the first transistor T**1** is switched on, so that a signal of the initial signal terminal Vint is written into the third node N**3** to reset the third node N**3** and charge the first capacitor C**1**; the second transistor T**2** is switched on, so that the signal of the initial signal terminal Vint is written into the second node N**2**, the second node N**2** is electrically connected to an anode of a light-emitting element L, to reset the anode of the light-emitting element L so as to eliminate residual charge of the anode of the light-emitting element L. The signal of the second control terminal CT**2** is a low-level signal, the tenth transistor T**10** is switched on, so that a signal of the time-length data terminal DataT is written into the sixth node **N6** and the second capacitor C**2** is charged. Because the signal of the time-length data terminal DataT is a high-level signal, the ninth transistor T**9** is switched on, and the signal of the light-emitting signal terminal EM cannot be written into the first node N**1**.

In a second phase P**22**, i.e., the writing phase, the signal of the scanning signal terminal Gate is a low-level signal, the fourth transistor T**4** is switched on, the signal of the current data terminal DataI is written into the fifth node N**5**; the third transistor T3 is switched on, at this point, a level of the fifth node N**5** is V**5**=Vd, where Vd is a voltage value of the signal of the current data terminal DataI, the first capacitor C**1** starts to discharge to charge the third node N3 until a level of the third node N**3** is V3=Vd+Vth, where Vth is a threshold voltage of the fifth transistor T**5**, and at this point, the fifth transistor T**5** is cut off. The third capacitor C**3** keeps a potential of the signal of the seventh node N**7** unchanged such that the eleventh transistor T**11** is always switched on, and the signal of the high-frequency input terminal Hf is written into the first node N**1**.

In a third phase P**23**, i.e., the light-emitting phase, the signal of the light-emitting signal terminal EM is a low-level signal, the sixth transistor T**6** is switched on, and the level of the fifth node N**5** is V**5**=Vdd, where Vdd is a voltage value of the signal at the first power supply terminal VDD; the seventh transistor T7 is switched on, the third capacitor C**3** keeps the potential of the signal of the seventh node N**7** unchanged, the eleventh transistor T**11** is aways switched on, the signal of the light-emitting signal terminal EM is written into the first node N**1**, and the eighth transistor T**8** is switched on. Since a voltage value of the third node N**3** is V3=Vd+Vth, the fifth transistor T5 is switched on, and the drive current flows into the light-emitting element L.

According to a current formula when the drive transistor is saturated, it can be obtained that the drive current I_L flowing through the light-emitting element L satisfies the following equations.

$$
\begin{aligned}
I_L &= (1/2)K(V_{GS} - Vth)^2 \\
&= (1/2)K(V3 - V5 - Vth)^2
\end{aligned}
$$

-continued

$$
\begin{aligned}
&= (1/2)K(Vd + Vth - Vdd - Vth)^2 \\
&= (1/2)K(Vd - Vdd)^2
\end{aligned}
$$

K is a fixed constant related to process parameters and geometric dimensions of the drive transistor, and VGs is a gate-source voltage difference of the drive transistor.

It can be seen from the derivation of the above current formula that in the light-emitting phase, the drive current output by the fifth transistor T**5** is not affected by the threshold voltage of the fifth transistor T**5**, and is only related to the signal of the current data terminal and the signal of the first power terminal. Therefore, the impact of the threshold voltage of the drive transistor on the drive current is eliminated, uniformity of the display brightness of the display product is ensured, and the display effect is improved.

In an exemplary embodiment, in the writing phase, the longer writing time of the signal of the current data terminal may cause prolonging of the threshold compensation time of the pixel circuit. The writing time of the signal of the current data terminal depends on the time that the current selection signal line of the current data line connected to the current data terminal has the valid level signal. The longer the time that the current selection signal line has the valid level signal is, the longer the writing time of the signal of the current data terminal is.

In an exemplary embodiment, when the gray tone displayed by the light-emitting element connected to the pixel unit is greater than the threshold gray tone, a control signal is provided to the first node through the light-emitting signal terminal, and at this point, the gray tone of the light-emitting element is controlled through the drive current. When the gray tone displayed by the light-emitting element connected to the pixel unit is less than the threshold gray tone, a control signal is provided to the first node through the high-frequency input terminal, and at this point, the gray tone of the light-emitting element is controlled through the drive current and the light-emitting time length. In an exemplary embodiment, the high-frequency pulse signal at the high-frequency input terminal controls the light-emitting time length, and a short light-emitting time length is dispersed to a frame of time, so that the flickering caused when the gray tone displayed by the light-emitting element connected to the pixel unit is less than the threshold gray tone is reduced, and the display effect of the display product is improved.

An embodiment of the present disclosure further provides a display panel. FIG. **11** is a schematic structural diagram of a display panel according to an embodiment of the present disclosure; FIG. **12** is another schematic structural diagram of a display panel according to an embodiment of the present disclosure; and FIG. **13** is a schematic structural diagram of a pixel unit according to an exemplary embodiment. As shown in FIG. **11** to FIG. **13**, the display panel according to the embodiment of the present disclosure includes: M rows and N columns of pixel units P, N current data lines DI_1 to DI_N sequentially arranged along a row direction, and N time-length data lines DT_1 to DT_N sequentially arranged along the row direction. Each pixel unit P includes a pixel circuit **10** and a light-emitting element **20**.

An i^{th} column of current data line DI_i and an i^{th} column of time-length data line DT_i are respectively located on two sides of an i^{th} column of pixel units, the current data terminals of the pixel circuits of the i^{th} column of pixel units are electrically connected to the i^{th} column of current data line DI_i, and the time-length data terminals of the pixel circuits of the i^{th} column of pixel units are electrically connected to the i^{th} column of time-length data line DT_i, where $1 \leq i \leq N$. The time for two current data lines between two adjacent columns of pixel units, and/or the time for two time-length data lines between two adjacent columns of pixel units, and/or the time for a time-length data line and a current data line between two adjacent columns of pixel units to receive a valid level signal do not coincide.

The pixel circuit is the pixel circuit according to any one of the foregoing embodiments, and the implementation principle and implementation effects are similar, which will not be repeated here.

As shown in FIG. **11**, in an exemplary embodiment, the display panel may further include a timing controller, a data signal driver, a scanning signal driver, a light-emitting signal driver, multiple scanning signal lines (S_1 to S_M) and multiple light-emitting signals line (E_1 to E_M).

In an exemplary embodiment, the timing controller may provide a gray-scale value and control signal suitable for a specification of the data signal driver to the data signal driver, may provide a clock signal, a scan starting signal, etc., suitable for a specification of the scanning signal driver to the scanning signal driver, and may provide a clock signal, an emission stopping signal, etc., suitable for a specification of the light-emitting signal driver to the light-emitting signal driver.

In an exemplary embodiment, the data signal driver may use a gray value and control signal received from the timing controller to generate a data voltage that is to be provided to the current data lines $DI_1, DI_2, \ldots, DI_N$ and a data voltage that is to be provided to the multiple time-length data lines $DT_1, DT_2, \ldots, DT_N$, where N may be a natural number.

In an exemplary embodiment, the scanning signal driver may receive a clock signal, a scan starting signal, etc., from the timing controller to generate a scanning signal that is to be provided to the scanning lines $S_1, S_2, S_3, \ldots$, and S_M. For example, the scanning signal driver may sequentially provide the scanning signal to the scanning signal lines S_1 to S_M. For example, the scanning signal driver may be composed of multiple cascaded shift registers, and may drive each shift register to sequentially generate the scanning signal under the control of the clock signal, where M may be a natural number.

In an exemplary embodiment, the light-emitting signal driver may receive the clock signal, the emission stopping signal, etc., from the timing controller to generate a light-emitting signal that is to be provided to the light-emitting signal lines $E_1, E_2, E_3, \ldots$, and E_M. For example, the light-emitting signal driver may sequentially provide the light-emitting signal to the light-emitting signal lines E_1 to E_M. For example, the light-emitting signal driver may be composed of multiple cascaded shift registers, and may drive each shift register to sequentially generate the light-emitting signal under the control of the clock signal, where M may be a natural number.

In an exemplary embodiment, the display panel may further include a substrate. The pixel circuits and the light-emitting elements are both located on the substrate.

In an exemplary embodiment, the substrate may be a rigid substrate or a flexible substrate. The rigid substrate may be, but not limited to, one or more of glass and metal foil. The flexible substrate may be, but not limited to, one or more of polyethylene terephthalate, ethylene terephthalate, polyether ether ketone, polystyrene, polycarbonate, PAT, PAR, polyimide, polyvinyl chloride, polyethylene, and textile fibers.

In an exemplary embodiment, the pixel unit may be any one of a red (R) pixel unit, a green (G) pixel unit, a blue (B) pixel unit, and a white pixel unit, which is not limited in the present disclosure. When the display panel includes the red (R) pixel unit, the green (G) pixel unit and the blue (B) pixel unit, the three pixel units can be arranged in parallel in a horizontal direction, in parallel in a vertical direction, or in a Delta shape. When the display panel includes the red (R) pixel unit, the green (G) pixel unit, the blue (B) pixel unit, and the white pixel unit, the four pixel units can be arranged in parallel in a horizontal direction, in parallel in a vertical direction, or in an array. No limits are made thereto in the present disclosure.

In an exemplary embodiment, a pixel circuit and a light-emitting element, in the same pixel unit, are electrically connected, and the pixel circuit is configured to provide a drive signal to the light-emitting element so as to drive the light-emitting element to work.

When the light-emitting element emits light, since a brightness of the light-emitting element when it emits light is related to its light-emitting time length and drive current, the brightness of the light-emitting element can be controlled by adjusting its light-emitting time length and drive current. Exemplarily, if two light-emitting elements have the same drive current and different light-emitting time lengths, the two light-emitting elements have different display brightness; if two light-emitting elements have different drive currents and the same light-emitting time lengths, the two light-emitting elements also have different display brightness; if two light-emitting elements have different drive currents and different light-emitting time lengths, whether the two light-emitting elements have the same display brightness needs to be analyzed.

In an exemplary embodiment, the light-emitting element in the red pixel unit is a red light-emitting diode, the light-emitting element in the blue pixel unit is a blue light-emitting diode, and the light-emitting element in the green pixel unit is a green light-emitting diode, or the light-emitting elements in the red pixel unit, the blue pixel unit, the green pixel unit and the white pixel unit are all blue light-emitting diodes. With color reversal materials (such as quantum dots, and phosphors), light emission of corresponding colors such as red, blue, green and white is implemented.

In an exemplary embodiment, that an i^{th} column of current data line DI_i and an i^{th} column of time-length data line DT_i are respectively located on two sides of an i^{th} column of pixel units may include: the i^{th} column of time-length data line DT^i and an $(i+1)^{th}$ column of current data line DI_{i+1}, or the i^{th} column of current data line DI_i and an $(i+1)^{th}$ column of data current line DI_{i+1}, or the i^{th} column of time-length data line DI_i and an $(i+1)^{th}$ column of time-length data line DT_{i+1}, or the i^{th} column of current data line DL and an $(i+1)^{th}$ column of time-length data line DT_{i+1} are arranged between the i^{th} column of pixel units and an $(i+1)^{th}$ column of pixel units. FIG. **2** is illustrated by taking an example that the i^{th} column of time-length data line DT^i and an $(i+1)^{th}$ column of current data line DI_{i+1} are arranged between the i^{th} column of pixel units and an $(i+1)^{th}$ column of pixel units.

In the present disclosure, since the time for two current data lines between two adjacent columns of pixel units, and/or the time for two time-length data lines between two adjacent columns of pixel units, and/or the time for a time-length data line and a current data line between two adjacent columns of pixel units to receive a valid level signal do not coincide, the cross talk of signal lines between adjacent pixel units may be reduced, the poor column brightness contrast is avoided, and the display effect of the display product is improved.

FIG. **14** is a sequence diagram of multiple selection signal lines according to an exemplary embodiment. As shown in FIG. **12** and FIG. **14**, in an exemplary embodiment, the display panel may further include: a first current selection signal line DI_MUX_1, a second current selection signal line DI_MUX_2, a first time-length selection signal line DT_MUX_1, and a second time-length selection signal line DT_MUX_2. Two adjacent columns of current data lines are respectively electrically connected to the first current selection signal line DI_MUX_1 and the second current selection signal line DI_MUX_2, and two adjacent columns of time-length data lines are respectively electrically connected to the first time-length selection signal line DT_MUX_1 and the second time-length selection signal line DT_MUX_2.

In an exemplary embodiment, the time for the first time-length selection signal line DT_MUX_1 to receive a valid level signal is within the time for a reset signal terminal in a pixel circuit connected to a time-length data line that is connected to the first time-length selection signal line DT_MUX_1 to receive a valid level signal. When one row of pixels display, the signal of the first time-length selection signal line DT_MUX_1 in the initialization phase is a valid level signal.

In an exemplary embodiment, the time for the second time-length selection signal line DT_MUX_2 to receive a valid level signal is within the time for a reset signal terminal in a pixel circuit connected to a time-length data line that is connected to the second time-length selection signal line DT_MUX_2 to receive a valid level signal. When one row of pixels display, the signal of the second time-length selection signal line DT_MUX_2 in the initialization phase is a valid level signal.

In an exemplary embodiment, the time for the first current selection signal line DI_MUX_1 to receive a valid level signal is within the time for a scanning signal terminal in a pixel circuit connected to a current data line that is connected to the first current selection signal line DI_MUX_1 to receive a valid level signal. When one row of pixels display, the signal of the first current selection signal line DI_MUX_1 in the initialization phase is a valid level signal.

In an exemplary embodiment, the time for the second current selection signal line DI_MUX_2 to receive a valid level signal is within the time for a scanning signal terminal in a pixel circuit connected to a current data line that is connected to the second current selection signal line DI_MUX_2 to receive a valid level signal. When one row of pixels display, the signal of the second current selection signal line DI_MUX_2 in the initialization phase is a valid level signal.

The time for the first time-length selection signal line DT_MUX_1 to receive the valid level signal and the time for the second time-length selection signal line DT_MUX_2 to receive the valid level signal do not coincide, and the time for the first current selection signal line DI_MUX_1 to receive the valid level signal and the time for the second current selection signal line DI_MUX_2 to receive the valid signal do not coincide.

In an exemplary embodiment, a current data line coupled to an odd column of pixel circuits is electrically connected to the first current selection signal line, and a time-length data line coupled to the odd column of pixel circuits is electrically connected to the first time-length selection signal line. A current data line coupled to an even column of pixel circuits is electrically connected to the second current selection signal line, and a time-length data line coupled to the even column of pixel circuits is electrically connected to the second time-length selection signal line. FIG. **2** is illustrated by an example in which the current data line coupled to an odd column of pixel circuits is electrically connected to the first current selection signal line, the time-length data line coupled to the odd column of pixel circuits is electrically connected to the first time-length selection signal line, the current data line coupled to an even column of pixel circuits is electrically connected to the second current selection signal line, and the time-length data line coupled to the even column of pixel circuits is electrically connected to the second time-length selection signal line.

In an exemplary embodiment, a current data line coupled to an even column of pixel circuits is electrically connected to the first current selection signal line, a time-length data line coupled to the even column of pixel circuits is electrically connected to the first time-length selection signal line, a current data line coupled to an odd column of pixel circuits is electrically connected to the second current selection signal line, and a time-length data line coupled to the odd column of pixel circuits is electrically connected to the second time-length selection signal line.

Since two adjacent columns of current data lines are electrically connected to different current selection signal lines, and two adjacent columns of time-length data lines are electrically connected to different time-length selection signals, the time for the first time-length selection signal line DT_MUX_1 to receive the valid level signal and the time for the second time-length selection signal line DT_MUX_2 to receive the valid level signal do not coincide, and the time for the first current selection signal line DI_MUX_1 to receive the valid level signal and the time for the second current selection signal line DI_MUX_2 to receive the valid signal do not coincide. Therefore, during the writing phase of one row of pixel circuits, when one signal line between an i^{th} column of pixel circuits and an $(i+1)^{th}$ column of pixel units is in a floating state, high-and-low level switching of a voltage of the other signal line has already been completed, that is, level fluctuation is avoided during the writing phase and interference between the adjacent signal lines is avoided.

In an exemplary embodiment, as shown in FIG. **12** and FIG. **13**, the display panel may further include: M reset signal lines (not shown in the figure) sequentially arranged along the column direction.

For each pixel circuit in an m^{th} row of pixel units, a scanning signal terminal of the pixel circuit is electrically connected to an m^{th} row of scanning signal line S_m, a reset signal terminal of the pixel circuit is electrically connected to an m^{th} row of reset signal line, and a light-emitting signal terminal of the pixel circuit is electrically connected to an m^{th} row of light-emitting signal line E_m, where $1 \leq m \leq M$.

The scanning signal terminals in the same row of pixel circuits are connected to the same scanning signal line, the reset signal terminals in the same row of pixel circuits are connected to the same reset signal line, the light-emitting signal terminals in the same row of pixel circuits are connected to the same signal line, and the initialization phase, writing phase, and light-emitting phase occur at the same time for all the pixel circuits in the same row of pixel circuits.

In an exemplary embodiment, FIG. **15** is a schematic structural diagram of a display panel according to an exemplary embodiment, and FIG. **16** is a sequence diagram of control signal lines in the display panel provided in FIG. **15**. As shown in FIG. **15** and FIG. **16**, the display panel according to an exemplary embodiment further includes: 4M control signal lines CTL_1 to CTL_{4M} sequentially arranged in a column direction. The pixel circuits **10** in the m^{th} row of pixel units are respectively connected to a $(4m-3)^{th}$ control signal line CTL_{4m-3}, a $(4m-2)^{th}$ control signal line CTL_{4m-2}, a $(4m-1)^{th}$ control signal line CTL_{4m-1}, and a $(4m)^{th}$ control signal line CTL_{4m}, respectively, where $1 \leq m \leq M$.

When the m^{th} row of pixel units display, the time for the $(4m-3)^{th}$ control signal line CTL_{4m-3} as well as the time for the $(4m-2)^{th}$ control signal line CTL_{4m-2}, the $(4m-1)^{th}$ control signal line CTL_{4m-1}, and the $(4m)^{th}$ control signal line CTL_{4m} to receive a valid level signal is within the time for the reset signal terminal in the pixel circuit in each pixel unit. The $(4m-3)^{th}$ control signal line CTL_{4m-3}, the $(4m-2)^{th}$ control signal line CTL_{4m-2}, the $(4m-1)^{th}$ control signal line CTL_{4m-1}, and the $(4m)^{th}$ control signal line CTL_{4m} that are connected to the same row of pixel circuits respectively at least receive the valid level signal once in the initialization phase of the pixel circuits.

The time for the $(4m-3)^{th}$ control signal line CTL_{4m-3} to receive the valid level signal, the time for the $(4m-2)^{th}$ control signal line to receive the valid level signal, the time for the $(4m-1)^{th}$ control signal line to receive the valid level signal, and the time for the $(4m)^{th}$ control signal line to receive the valid level signal do not coincide.

In an exemplary embodiment, a first control terminal CT**1** of each pixel circuit in a pixel unit in an odd column of the m^{th} row is electrically connected to the $(4m-3)^{th}$ control signal line CTL_{4m-3}, and a second control terminal CT**2** of the pixel circuit in the pixel unit in the odd column of the m^{th} row is electrically connected to the $(4m-2)^{th}$ control signal line CTL_{4m-2}. A first control terminal CT**1** of each pixel circuit in a pixel unit in an even column of the m^{th} row is electrically connected to the $(4m-1)^{th}$ control signal line CTL_{4m-1}, and a second control terminal CT**2** of the pixel circuit in the pixel unit in the even column of the m^{th} row is electrically connected to the $(4m)^{th}$ control signal line CTL_{4m}.

As shown in FIG. **15**, the working process of each pixel circuit in an i^{th} row of pixel units includes: an initialization phase P**1**_*i*, a writing phase P**2**_*i*, and a light-emitting phase P**3**_*i*. The initialization phase P**1**_*i*+1 and the writing phase P**2**_*i*+1 of each pixel circuit in an $(i+1)^{th}$ row of pixel units occur in the time period where the light-emitting phase P**3**_*i* of each pixel circuit in the i^{th} row of pixel units is located.

In the initialization phase P**1**_**1** of a first row of pixel circuits, a first control signal line CTL_1 as well as a second control signal line CTL_2, a third control signal line CTL_3, and a fourth row control signal line CTL_4 is of a valid level signal. In the initialization phase P**1**_**2** of a second row of pixel circuits, a fifth control signal line CTL_5 as well as a sixth control signal line CTL_6, a seventh control signal line CTL_7, and an eighth row control signal line CTL_8 is of a valid level signal, and so on.

In an exemplary embodiment, FIG. **17** is another schematic structural diagram of a display panel according to an exemplary embodiment, and FIG. **18** is a sequence diagram of control signal lines in the display panel provided in FIG. **17**. As shown in FIG. **17** and FIG. **18**, the display panel according to an exemplary embodiment further includes: 2M control signal lines CTL_1 to CTL_{2M} sequentially arranged in a column direction. A first control terminal of each pixel circuit **10** in an m^{th} row of pixel units is electrically connected to a $(2m-1)^{th}$ control signal line CTL_{2m-1}, and a second control terminal of the pixel circuit in the m^{th} row of pixel units is electrically connected to a $(2m)^{th}$ control signal line CTL_{2m}, where $1 \leq m \leq M$.

When the m^{th} row of pixel units display, the time for the $(2m-1)^{th}$ control signal line CTL_{2m-1} to receive a valid level signal and the time for the $2m^{th}$ control signal line CTL_{2m} to receive a valid level signal are both within the time for a reset signal terminal in a pixel circuit in each pixel unit to receive a valid level signal. The $(2m-1)^{th}$ control signal line CTL_{2m-1} and the $(2m)^{th}$ control signal line CTL_{2m} that are connected to the same row of pixel circuits respectively at least receive the valid level signal once in the initialization phase of the pixel circuits.

The time for the $(2m-1)^{th}$ control signal line to receive the valid level signal and the time for the $(2m)^{th}$ control signal line to receive the valid level signal do not coincide.

As shown in FIG. **18**, the working process of each pixel circuit in an i^{th} pixel unit includes: an initialization phase P**1**_*i*, a writing phase P**2**_*i*, and a light-emitting phase P**3**_*i*. The initialization phase P**1**_*i*+1 and the writing phase P**2**_*i*+1 of each pixel circuit in an $(i+1)^{th}$ rows of pixel units occur in the time period where the light-emitting phase P**3**_*i* of each pixel circuit in the i^{th} row of pixel units is located.

In the initialization phase P**1**_**1** of a first row of pixel circuits, a first control signal line CTL_1 as well as a second control signal line CTL_2 is of a valid level signal; in the initialization phase P**1**_**2** of a second row of pixel circuits, a third control signal line CTL_3 as well as a fourth control signal line CTL_4 is of a valid level signal, and so on.

In an exemplary embodiment, as shown in FIG. **12**, the display panel may further include: a multiplexed output selection circuit **20**, K current data output lines SI_1 to SI_K sequentially arranged in a column direction, and K time-length data output lines ST_1 to ST_K sequentially arranged in the column direction, where K=N/2.

The multiplexed output selection circuit **20** is electrically connected to N current data lines DI_1 to DI_N, N time-length data lines DT_1 to DT_N, a first current selection signal line DI_MUX_1, a second current selection signal line DI_MUX_2, a first time-length selection signal line DT_MUX_1, a second time-length selection signal line DT_MUX_2, K current data output lines, and K time-length data output lines, respectively, and is configured to output data signals of the K current data lines to the N current data lines in a time-sharing manner and output data signals of the K time-length data output lines to the N time-length data lines in a time-sharing manner under the control of the first current selection signal line DI_MUX_1, the second current selection signal line DI_MUX_2, the first time-length selection signal line DT_MUX_1, and the second time-length selection signal line DT_MUX_2.

FIG. **19** is an equivalent circuit diagram of a multiplexed output selection circuit according to an exemplary embodiment. As shown in FIG. **19**, in an exemplary embodiment, the multiple output selection circuit includes: K first current selection transistors MI**1**, K second current selection transistors MI**2**, K first time-length selection transistors MT**1**, and K second time-length selection transistors MT**2**.

A control electrode of a k^{th} first current selection transistor MI**1** is electrically connected to the first current selection signal line DI_MUX_1, a first electrode of the k^{th} first current selection transistor MI**1** is electrically connected to a $(2k-1)^{th}$ column of current data line DI_{2k-1}, and a second electrode of the k^{th} first current selection transistor MI**1** is electrically connected to a k^{th} column of current data output line SI_k, where $1 \leq k \leq N/2$. A control electrode of a first first current selection transistor MI**1** is electrically connected to the first current selection signal line DI_MUX_1, a first electrode of the first first current selection transistor MI**1** is electrically connected to a first column of current data line

DI_1, a second electrode of the first first current selection transistor MI1 is electrically connected to a first column of current data output line SI_1, a control electrode of a second first current selection transistor MI1 is electrically connected to the first current selection signal line DI_MUX_1, a first electrode of the second first current selection transistor MI1 is electrically connected to a third column of current data line DI_3, a second electrode of the second first current selection transistor MI1 is electrically connected to a first column of current data output line SI_2, and so on.

A control electrode of a k^{th} second current selection transistor MI2 is electrically connected to the second current selection signal line DI_MUX_2, a first electrode of the k^{th} second current selection transistor MI2 is electrically connected to a $(2k)^{th}$ column of current data line DI_{2k}, and a second electrode of the k^{th} second current selection transistor MI2 is electrically connected to the k^{th} column of current data output line SI_k. A control electrode of a first second current selection transistor MI2 is electrically connected to the second current selection signal line DI_MUX_2, a first electrode of the first second current selection transistor MI2 is electrically connected to a second column of current data line DI_2, and a second electrode of the first second current selection transistor MI2 is electrically connected to the first column of current data output line SI_1. A control electrode of a second second current selection transistor MI2 is electrically connected to the second current selection signal line DI_MUX_2, a first electrode of the second second current selection transistor MI2 is electrically connected to a fourth column of current data line DI_4, and a second electrode of the second second current selection transistor MI2 is electrically connected to the second column of current data output line SI_2, and so on.

A control electrode of a k^{th} first time-length selection transistor MT1 is electrically connected to the first time-length selection signal line DT_MUX_1, a first electrode of the k^{th} first time-length selection transistor MT_1 is electrically connected to a $(2k-1)^{th}$ column of time-length data line DT_{2k-1}, and a second electrode of the k^{th} first time-length selection transistor MT1 is electrically connected to a k^{th} column of time-length data output line ST_k. A control electrode of a first first time-length selection transistor MT1 is electrically connected to the first time-length selection signal line DT_MUX_1, a first electrode of the first first time-length selection transistor MT1 is electrically connected to a first column of time-length data line DT_1, and a second electrode of the first first time-length selection transistor MT1 is electrically connected to a first column of time-length data output line ST_1. A control electrode of a second first time-length selection transistor MT1 is electrically connected to the first time-length selection signal line DT_MUX_1, a first electrode of the second first time-length selection transistor MT1 is electrically connected to a third column of time-length data line DT_3, and a second electrode of the second first time-length selection transistor MT1 is electrically connected to a third column of time-length data output line ST_3, and so on.

A control electrode of a k^{th} second time-length selection transistor MT2 is electrically connected to the second time-length selection signal line DT_MUX_2, a first electrode of the k^{th} second time-length selection transistor MT2 is electrically connected to a $(2k)^{th}$ column of time-length data line DT_{2k}, and a second electrode of the k^{th} second time-length selection transistor MT2 is electrically connected to the k^{th} column of time-length data output line ST_k. A control electrode of a first second time-length selection transistor MT2 is electrically connected to the second time-length selection signal line DT_MUX_2, a first electrode of the first second time-length selection transistor MT2 is electrically connected to a second column of time-length data line DT_2, and a second electrode of the first second time-length selection transistor MT2 is electrically connected to the first column of time-length data output line ST_1. A control electrode of a second second time-length selection transistor MT2 is electrically connected to the second time-length selection signal line DT_MUX_2, a first electrode of the second second time-length selection transistor MT2 is electrically connected to a fourth column of time-length data line DT_4, and a second electrode of the second second time-length selection transistor MT2 is electrically connected to the second column of time-length data output line ST_2.

In an exemplary embodiment, a time-length data output line ST_i provides a data signal to a $(2i-1)^{th}$ column of time-length data line DT_{2i-1} and a $2i^{th}$ column of time-length data line DT_{2i} in a time sharing manner. A current data output line SI_i provides a data signal to a $(2i-1)^{th}$ column of current data line DI_{2i-1} and a $2i^{th}$ column of current data line DI_{2i} in a time-sharing manner.

In an exemplary embodiment, the first current selection transistor MI1, the second current selection transistor MI2, the first time-length selection transistor MT1, and the second time-length selection transistor MT2 may be switch transistors.

The first current selection transistor MI1, the second current selection transistor MI2, the first time-length selection transistor MT1, and the second time-length selection transistor MT2 may be all P-type transistors, or may be all N-type transistors.

Taking an example that the first current selection transistor Mul, the second current selection transistor MI2, the first time length selection transistor MT1, and the second time length selection transistor MT2 as P-type transistors, FIG. **20** is a sequence diagram of a display panel according to an exemplary embodiment. A display panel provided in FIG. **20** corresponds to the display panel in FIG. **15**. As shown in FIG. **20**, E_i is a light-emitting signal line connected to a light-emitting signal terminal of each pixel circuit in the i^{th} row of pixel units; RL_i is a reset signal line connected to a reset signal terminal of each pixel circuit in the i^{th} row of pixel units; S_i is a scanning signal line connected to a scanning signal terminal of each pixel circuit in the i^{th} row of pixel units; CTL_{4i-3} is a control signal line connected to a first control terminal of a pixel circuit in a pixel unit in the i^{th} row and n^{th} column; CTL_{4i-2} is a control signal line connected to a second control terminal of the pixel circuit in the pixel unit in the i^{th} row and n^{th} column; CTL_{4i-1} is a control signal line connected to a first control terminal of a pixel circuit in the i^{th} row and $(n+1)^{th}$ column; and CTL_{4i} is a control signal line connected to a second control terminal of the pixel circuit in the pixel unit in the i^{th} row and the $(n+1)^{th}$ column. The working process of each pixel circuit in the i^{th} row of pixel units includes: an initialization phase P1_*i*, a writing phase P2_*i*, and a light-emitting phase P3_*i*. RL_i is of a valid level signal in the initialization phase P1_*i*, S_i is of a valid level signal in the writing phase P2_*i*, and E_i is of a valid level signal in the light-emitting phase P3_*i*. The CTL_{4i-3}, CTL_{4i-2}, CTL_{4i-1}, and CTL_{4i} are of valid level signals when the i^{th} row of pixel units are in the initialization phase P1_*i*, and the CTL_{4i-3}, CTL_{4i-2}, CTL_{4i_1}, and CTL_{4i} are of valid level signals at different time.

As shown in FIG. **20**, E_{i+1} is a light-emitting signal line connected to a light-emitting signal terminal of each pixel circuit in an $(i+1)^{th}$ row of pixel units; RL_{i+1} is a reset signal line connected to a reset signal terminal of each pixel circuit in the (i+1)th row of pixel units; S_{i+1} is a scanning signal line connected to a scanning signal terminal of each pixel circuit in the (i+1)th row of pixel units; CTL_{4i+1} is a control signal line connected to a first control terminal of a pixel circuit in a pixel unit in the (i+1)th row and nth column; CTL_{4i+2} is a control signal line connected to a second control terminal of the pixel circuit in the pixel unit in the (i+1)th row and nth column; CTL_{4i+3} is a control signal line connected to a first control terminal of a pixel circuit in the (i+1)th row and (n+1)th column; and CTL_{4i+4} is a control signal line connected to a second control terminal of the pixel circuit in the pixel unit in the (i+1)th row and the (n+1)th column. The working process of each pixel circuit in the (i+1)th row of pixel units includes: an initialization phase P**1**_*i*+1, a writing phase P**2**_*i*+2, and a light-emitting phase. RL_{i+1} is of a valid level signal in the initialization phase P**1**_*i*+1, S_{i+1} is of a valid level signal in the writing phase P**2**_*i*+1, and E_{i+1} is of a valid level signal in the light-emitting phase P**3**_*i*+1. The CTL_{4i+3}, CTL_{4i+2}, CTL_{4i+1}, and CTL_{4i+4} are of valid level signals when the (i+1)th row of pixel units are in the initialization phase P**1**_*i*+1, and the CTL_{4i+3}, CTL_{4i+2}, CTL_{4i+1}, and CTL_{4i+4} are of valid level signals at different time.

As shown in FIG. **20**, the initialization phase P**1**_*i*+1 of each pixel circuit in the (i+1)th row of pixel units occurs in the time period where the light-emitting phase P**3**_*i* of each pixel circuit in the ith row of pixel units is located.

As shown in FIG. **20**, DI_n is a current data line connected to the current data terminal in the pixel circuit in the pixel unit in the ith row and nth column; DT_n is a time-length data line connected to the time-length data terminal in the pixel circuit in the pixel unit in the ith row and nth column; DI_{n+1} is a current data line connected to the current data terminal in the pixel circuit in the pixel unit in the ith row and (n+1)th column, DT_{n+1} is a time-length data line connected to the time-length data terminal in the pixel circuit in the pixel unit in the ith row and (n+1)th column; ST_m is a time-length data output line connected to the DT_n and DT_{n+1}; and SI_m is a current data output line connected to the DI_n and DI_{n+1}, where m=(n+1)/2, and n is an odd number.

For the pixel unit in the ith row and nth column and the pixel unit in the ith row and (n+1)th column, an example is taken that the DT_n is electrically connected to the first time-length selection signal line DT_MUX_1, the DT_{n+1} is electrically connected to the second time-length selection signal line DT_MUX_2, the DI_n is electrically connected to the first time-length selection signal line DT_MUX_1, the DI_{n+1} is electrically connected to the second time-length selection signal line DT_MUX_2, and the DI_n and DT_{n+1} are located between the pixel unit in the ith row and nth column and the pixel unit in the ith row and (n+1)th column, as shown in FIG. **20**, the light-emitting signal line E_i, reset signal line RL_i and scanning signal line G_i that are connected to the pixel circuit in the pixel unit in the ith row and nth column and the pixel circuit in the ith row and (n+1)th column are the same signal line. That is, the pixel circuit in the pixel unit in the ith row and nth column and the pixel circuit in the pixel unit in the ith row and (n+1)th column sequentially simultaneously undergo the initialization phase, the writing phase, and the light-emitting phase. Since the first time-length selection signal line DT_MUX_1 and the second time-length selection signal line DT_MUX_2 are of valid level signals in the initialization phase P**1**_*i* of each pixel circuit in the ith row of pixel units, and the first current selection signal line DI_MUX_1 and the second time-length selection signal line DI_MUX_2 are both of the valid level signal in the writing stage P**2**_*i* of each pixel circuit in the ith row of pixel units, when the DI_{n+1} is in a floating state during the writing phase (that is, a time period when the DI_MUX_2 is at an invalid level), no voltage fluctuations will be caused in the signal of the DT_n or the DT_{n+1}, that is, the signal of the DT_n or DT_{n+1} has completed a change of the corresponding voltage signal, so that the signal of the DI_{n+1} can be prevented from being disturbed by the level change of the signal of the DT_{n+1}, the poor column brightness contrast can be avoided, and the display effect of the display product is improved. Correspondingly, when the DI_n is in a floating state during the writing phase (that is, a time period when the DI_MUX_1 is at an invalid level), no voltage fluctuations will be caused in the signal of the DT_{n-1} or DT_n, that is, the signal of the DT_n or DT_{n-1} has completed a change of the corresponding voltage signal, so that the signal of the DI_n is prevented from being disturbed by the level change of the signal of the DT_{n-1}, the poor column brightness contrast can be avoided, and the display effect of the display product is improved.

In an exemplary embodiment, as shown in FIG. **20**, for the ith row of pixel circuits, the time for the first time-length selection signal line DT_MUX_1 and the second time-length selection signal line DT_MUX_2 to receive the valid level signal is within the initialization phase P**1**_*i* of the ith row of pixel circuits. The time for the CTL_{4i-3} and CTL_{4i-2} to receive the valid level signal is within the time for the first time-length selection signal line DT_MUX_1 to receive the valid level signal. The time for the CTL_{4i-1} and CTL_{4i} to receive the valid level signal is within the time for the second time-length selection signal line DT_MUX_2 to receive the valid level signal. A voltage value of the time-length data line DT_n connected to the pixel circuit in the ith row and nth column when the CTL_{4i-3} receives the valid level signal is different from a voltage value of the time-length data line connected to the pixel circuit in the ith row and nth column when the CTL_{4i-2} receives the valid level signal. A voltage value of the time-length data line DT_{n+1} connected to the pixel circuit in the ith row and (n+1)th column when the CTL_{4i-1} receives the valid level signal is different from a voltage value of the time-length data line connected to the pixel circuit in the ith row and (n+1)th column when the CTL_{4i} receives the valid level signal.

Taking an example that the first current selection transistor MI**1**, the second current selection transistor MI**2**, the first time length selection transistor MT**1**, and the second time length selection transistor MT**2** as P-type transistors, FIG. **21** is another sequence diagram of a display panel according to an exemplary embodiment. A display panel provided in FIG. **21** corresponds to the display panel in FIG. **17**. As shown in FIG. **21**, E_i is a light-emitting signal line connected to a light-emitting signal terminal of each pixel circuit in an ith row of pixel units; RL_i is a reset signal line connected to a reset signal terminal of each pixel circuit in the ith row of pixel units; S_i is a scanning signal line connected to a scanning signal terminal of each pixel circuit in the ith row of pixel units; CTL_{2i-1} is a control signal line connected to a first control terminal of each pixel circuit in the ith row of pixel units; CTL_{2i} is a control signal line connected to a second control terminal of each pixel circuit in the ith row of pixel circuits. The working process of each pixel circuit in the ith row of pixel units includes: an initialization phase P**1**_*i*, a writing phase P**2**_*i*, and a light-emitting phase P**3**_*i*. RL_i is of a valid level signal in the initialization phase P**1**_*i*, S_i is of a valid level signal in the writing phase P**2**_*i*, and E_i is of a valid level signal in the light-emitting phase P**3**_*i*. The CTL_{2i-1} and CTL_{2i} are of valid level signals when the ith row of pixel units are in the initialization phase **P1**_*i*, and the CTL_{2i-1} and CTL_{2i} are of valid level signals at different time.

As shown in FIG. **21**, E_{i+1} is a light-emitting signal line connected to a light-emitting signal terminal of each pixel circuit in an $(i+1)^{th}$ row of pixel units; RL_{i+1} is a reset signal line connected to a reset signal terminal of each pixel circuit in the $(i+1)^{th}$ row of pixel units; S_{i+1} is a scanning signal line connected to a scanning signal terminal of each pixel circuit in the $(i+1)^{th}$ row of pixel units; CTL_{2i+1} is a control signal line connected to a first control terminal of each pixel circuit in the $(i+1)^{th}$ row of pixel units; CTL_{2i+2} is a control signal line connected to a second control terminal of each pixel circuit in the $(i+1)^{th}$ row of pixel circuits. The working process of each pixel circuit in the $(i+1)^{th}$ row of pixel units includes: an initialization phase **P1**_*i*+1, a writing phase **P2**_*i*+1, and a light-emitting phase **P3**_*i*+1. RL_{i+1} is of a valid level signal in the initialization phase **P1**_*i*+1, S_{i+1} is of a valid level signal in the writing phase **P2**_*i*+1, and E_{i+1} is of a valid level signal in the light-emitting phase **P3**_*i*+1. The CTL_{2i+1} and CTL_{2i+2} are of valid level signals when the $(i+1)^{th}$ row of pixel units are in the initialization phase **P1**_*i*+1, and the CTL_{2i+1} and CTL_{2i+2} are of valid level signals at different time.

As shown in FIG. **21**, the initialization phase **P1**_*i*+1 of each pixel circuit in the $(i+1)^{th}$ row of pixel units occur in the time for the light-emitting phase P**3**_*i* of each pixel circuit in the i^{th} row of pixel units.

As shown in FIG. **21**, DI_n is a current data line connected to a current data terminal in a pixel circuit in a pixel unit in the i^{th} row and n^{th} column; DT_n is a time-length data line connected to a time-length data terminal in the pixel circuit in the pixel unit in the i^{th} row and n^{th} column; DI_{n+1} is a current data line connected to a current data terminal in a pixel circuit in a pixel unit in the i^{th} row and $(n+1)^{th}$ column, DT_{n+1} is a time-length data line connected to a time-length data terminal in the pixel circuit in the pixel unit in the i^{th} row and $(n+1)^{th}$ column; ST_m is a time-length data output line connected to the DT_n and DT_{n+1}; and SI_m is a current data output line connected to the DI_n and DI_{n+1}, where m=(n+1)/2, and n is an odd number.

For the pixel unit in i^{th} row and n^{th} column and the pixel unit in i^{th} row and (n+1)th column, an example is taken that DT_n is electrically connected to the first time-length selection signal line DT_MUX_1, DT_{n+1} is electrically connected to the second time-length selection signal line DT_MUX_2, DI_n is electrically connected to the first time-length selection signal line DT_MUX_1, DI_{n+1} is electrically connected to the second time-length selection signal line DT_MUX_2, and DI_n and DT_{n+1} are located between the pixel unit in the i^{th} row and n^{th} column and the pixel unit in the i^{th} row and $(n+1)^{th}$ column, as shown in FIG. **21**, the light-emitting signal line E_i, reset signal line RL_i and scanning signal line G_i that are connected to the pixel circuit in the pixel unit in the i^{th} row and n^{th} column and the pixel circuit in the i^{th} row and $(n+1)^{th}$ column are the same signal line. That is, the pixel circuit in the pixel unit in the i^{th} row and n^{th} column and the pixel circuit in the pixel unit in the i^{th} row and $(n+1)^{th}$ column sequentially simultaneously undergo the initialization phase, the writing phase, and the light-emitting phase. Since the first time-length selection signal line DT_MUX_1 and the second time-length selection signal line DT_MUX_2 are of valid level signals in the initialization stage P**1**_*i* of each pixel circuit in the i^{th} row of pixel units, and the first current selection signal line DI_MUX_1 and the second time-length selection signal line DT_MUX_2 are both of the valid level signal in the writing stage P**2**_*i* of each pixel circuit in the i^{th} row of pixel units, when the DI_{n+1} is in a floating state during the writing phase (that is, a time period when DI_MUX_2 is at an invalid level), no voltage fluctuations will be caused in the signal of the DT_n or the DT_{n+1}, that is, the signal of the DT_n or DT_{n+1} has completed a change of the corresponding voltage signal, so that the signal of the DI_{n+1} can be prevented from being disturbed by the level change of the signal of the DT_{n+1}, the poor column brightness contrast can be avoided, and the display effect of the display product is improved. Correspondingly, when the DI_n is in a floating state during the writing phase (that is, a time period when DI_MUX_1 is at an invalid level), no voltage fluctuations will be caused in the signal of the DT_{n-1} or DT_n, that is, the signal of the DT_n or DT_{n-1} has completed a change of the corresponding voltage signal, so that the signal of the DI_n is prevented from being disturbed by the level change of the signal of the DT_{n-1}, the poor column brightness contrast can be avoided, and the display effect of the display product is improved.

In an exemplary embodiment, as shown in FIG. **21**, for the i^{th} row of pixel circuits, the time for the first time-length selection signal line DT_MUX_1 and the second time-length selection signal line DT_MUX_2 to receive the valid level signal is within the initialization phase **P1**_*i* of the i^{th} row of pixel circuits. The time for the first time-length selection signal line DT_MUX_1 to receive the valid level signal is within the time for the CTL_{2i-1} or CTL_{2i} to receive the valid level signal. The time for the second time-length selection signal line DT_MUX_2 to receive the valid level signal is within the time for the CTL_{2i-1} or CTL_{2i} to receive the valid level signal. The time for the first time-length selection signal line DT_MUX_1 to receive the valid level signal and the time for the second time-length selection signal line DT_MUX_2 to receive the valid signal do not coincide. A voltage value of the time-length data line DT_n connected to the pixel circuit in the i^{th} row and n^{th} column when the CTL_{2i-1} receives the valid level signal is different from a voltage value of the time-length data line connected to the pixel circuit in the i^{th} row and n^{th} column when the CTL_{2i} receives the valid level signal.

An embodiment of the present disclosure further provides a display device, including a display panel.

The display panel is the display panel according to any one of the foregoing embodiments, and the implementation principle and implementation effects are similar, which will not be repeated here.

In an exemplary embodiment, the display device may be any device that displays whether it is moving (for example, a video) or fixed (for example, a still image), and whether it is text or image. More specifically, the display device can be one of various electronic devices, can be implemented in or associated with various electronic devices. The various electronic devices include, for example, (but not limited to), a mobile phone, a wireless device, a Personal Data Assistant (PS1), a handheld or portable computer, a GPS receiver/navigator, a camera, an MP4 video player, a camcorder, a game console, a watch, a clock, a calculator, a TV monitor, a flat panel display, a computer monitor, a car monitor (e.g., an odometer display), a navigator, a cockpit controller and/or display, a camera view display (e.g., a display of a rear-view camera in a car), an electronic photo, an electronic billboards or sign, a projector, building structure, a package, and an aesthetic structure (e.g., an image display for a piece of jewelry). The embodiment of the present disclosure does not limit the specific form of the above-mentioned display device.

An embodiment of the present disclosure further provides a drive method for a pixel circuit. The drive method for a pixel circuit is configured to drive the pixel circuit. The drive method for a pixel circuit according to the embodiment of the present disclosure includes the following operations.

A node control sub-circuit provides a signal of an initial signal terminal to a second node and a third node under the control of a reset signal terminal.

The node control sub-circuit provides a signal of the third node to the fourth node under the control of a scanning signal terminal; a writing sub-circuit provides a signal of a current data terminal to a fifth node under the control of the scanning signal terminal; and a drive sub-circuit provides a drive current to a fourth node under the control of the third node and the fifth node.

A light-emitting control sub-circuit provides a signal of a first power terminal to the fifth node and provides a signal of the fourth node to the second node under the control of a first node and a light-emitting signal line.

The pixel circuit is the pixel circuit according to any one of the foregoing embodiments, and the implementation principle and implementation effects are similar, which will not be repeated here.

In a case where a gray tone displayed by a light-emitting element connected to the pixel unit is greater than a threshold gray tone, the drive method for a pixel circuit according to an exemplary embodiment may further include: a first control sub-circuit provides a signal of a light-emitting signal terminal to the first node under the control of a current data terminal, a second control terminal, and a ground terminal.

In a case where a gray tone displayed by a light-emitting element connected to the pixel unit is less than a threshold gray tone, the drive method for a pixel circuit according to an exemplary embodiment may further include: a second control sub-circuit provides a signal of a high-frequency input terminal to the first node under the control of a time-length data terminal, a first control terminal, and a ground terminal.

An embodiment of the present disclosure further provides a drive method for a display panel. The drive method for a display panel is configured to drive the display panel. The drive method for the display panel according to the embodiment of the present disclosure may include the following operations.

A signal is provided to N current data lines and along N time-length data lines so that the time for two current data lines between two adjacent columns of pixel units, and/or the time for two time-length data lines between two adjacent columns of pixel units, and/or the time for a time-length data line and a current data line between two adjacent columns of pixel units to receive a valid level signal do not coincide.

An embodiment of the present disclosure further provides a drive method for a display panel, wherein the display panel comprises: pixel circuits arranged in array, a plurality of current data lines, a plurality of time-length data lines, a first current selection signal line DI_MUX_1, a second current selection signal line DI_MUX_2, a first time-length selection signal line DT_MUX_1 and a second time-length selection signal line DT_MUX_2, the pixel circuits are respectively connected with the current data lines and the time-length data lines, at least one current data line is connected with the first current selection signal line DI_MUX_1 or the second current selection signal line DI_MUX**2**, two adjacent current data lines are connected with different current selection signal lines, at least one time-length data line is connected with the first time-length selection signal line DT_MUX_1 or the second time-length selection signal line DT_MUX_2, and two adjacent time-length data lines are connected with different time-length selection signal lines.

The pixel circuit is the pixel circuit according to any one of the foregoing embodiments, which is not limited in present disclosure.

The drive method for a display panel according to the embodiment of the present disclosure includes providing a valid level signal to a first time-length selection signal line DT_MUX_1, a second time-length selection signal line DT_MUX_2, a first current selection signal line DI_MUX_1 and a second current selection signal line DI_MUX_2. FIGS. **20** and **21** are illustrated by taking a case in which the transistors in the pixel circuit are P-type transistor as an example, so the valid level signal refers to a low-level signal. When the transistors in the pixel circuit are N-type transistors, the valid level signal refers to a high-level signal.

As shown in FIGS. **20** and **21**, the time for at least two signal lines of the first time-length selection signal line DT_MUX_1, the second time-length selection signal line DT_MUX_2, the first current selection signal line DI_MUX_1, and the second current selection signal line DI_MUX_2 to receive the valid level signal do not overlap. Exemplarily, the time for all of the first time-length selection signal line DT_MUX_1, the second time-length selection signal line DT_MUX_2, the first current selection signal line DI_MUX_1, and the second current selection signal line DI_MUX_2 to receive the valid level signal does not overlap.

In some possible implementations, the display panel further includes: a reset signal line, a scanning signal line, and a light-emitting signal line; the pixel circuit is connected to the reset signal line, the scanning signal line and the light-emitting signal line, respectively. As shown in FIGS. **20** and **21**, an i^{th} row of pixel circuits are connected to the reset signal line RL_i, the scanning signal line S_i, and the light-emitting signal line and an $(i+1)^{th}$ row of pixel circuits are connected to the reset signal line RL_{i+1}, the scanning signal line S_{i+1}, and the light-emitting signal line E_{i+1}, and so on.

In some possible implementations, the drive method for the display panel may further include: providing a valid level signal to the reset signal line, the scanning signal line, and the light-emitting signal line; the time for at least two signal lines of the reset signal line, the scanning signal line and the light-emitting signal line connected to the same pixel circuit to receive the valid level signal do not overlap. Exemplarily, as shown in FIGS. **20** and **21**, the time for the reset signal line RL_i, the scanning signal line S_i, and the light-emitting signal line E_i connected to the i^{th} row of pixel circuits to receive the valid level signal do not overlap, and the time for the reset signal line RL_{i+1}, the scanning signal line S_{i+1}, and the light-emitting signal line E_{i+1} connected to the $(i+1)^{th}$ row of pixel circuits to receive the valid level signal do not overlap.

In some possible implementations, the time for the reset signal line connected to a $(m+1)^{th}$ row of pixel circuits to receive the valid level signal is within the time for the light-emitting signal line connected to a m^{th} row of pixel units to receive the valid level signal, herein $1 \leq m \leq M$, and M is the total number of rows of the pixel circuits. Exemplarily, as shown in FIGS. **20** and **21**, the time for the reset signal line RL_{i+1} connected to the $(i+1)^{th}$ row of pixel circuits to receive the valid level signal is within the time for the light-emitting signal line E_i connected to the i^{th} row of pixel circuits to receive the valid level signal.

In some possible implementations, as shown in FIGS. **20** and **21**, the time for the first time-length selection signal line

DT_MUX_1 to receive the valid level signal is within the time for the reset signal line connected to at least one row of pixel circuits to receive the valid level signal. Exemplarily, the time for the first time-length selection signal line DT_MUX_1 to receive the valid level signal is within the time for the reset signal line RL_i connected to the i^{th} row of pixel circuits to receive the valid level signal, and the time for the first time-length selection signal line DT_MUX_1 to receive the valid level signal is within the time for the reset signal line RL_{i+1} connected to the $(i+1)^{th}$ row of pixel circuits to receive the valid level signal.

In some possible implementations, as shown in FIGS. **20** and **21**, the time for the second time-length selection signal line DT_MUX_2 to receive the valid level signal is within the time for the reset signal line connected to at least one row of pixel circuits to receive the valid level signal. Exemplarily, the time for the second time-length selection signal line DT_MUX_2 to receive the valid level signal is within the time for the reset signal line RL_i connected to the i^{th} row of pixel circuits to receive the valid level signal, and the time for the second time-length selection signal line DT_MUX_2 to receive the valid level signal is within the time for the reset signal line RL_{i+1} connected to the $(i+1)^{th}$ row of pixel circuits to receive the valid level signal.

In some possible implementations, as shown in FIGS. **20** and **21**, the time for the first time-length selection signal line DT_MUX_1 to receive the valid level signal and the time for the second time-length selection signal line DT_MUX_2 to receive the valid level signal do not overlap, and the sum of the time length t**11** for the first time-length selection signal line DT_MUX_1 to receive the valid level signal and the time length t**12** for the second time-length selection signal line DT_MUX_2 to receive the valid level signal is less than the time length t**1** for the reset signal line connected to at least one row of pixel circuits to receive the valid level signal.

In some possible implementations, within the time for the reset signal line connected to at least one row of pixel circuits to receive the valid level signal, the valid level signal received by the first time-length selection signal line DT_MUX_1 may be a single pulse signal or a multiple pulse signal, and the valid level signal received by the second time-length selection signal line DT_MUX_2 may be a single pulse signal or a multiple pulse signal. When the valid level signal received by the first time-length selection signal line DT_MUX_1 is a single pulse signal, the valid level signal received by the second time-length selection signal line DT_MUX_2 is a single pulse signal, alternatively, when the valid level signal received by the first time-length selection signal line DT_MUX_1 is a multiple pulse signal, the valid level signal received by the second time-length selection signal line DT_MUX_2 is a multiple pulse signal. FIG. **20** is illustrated by taking a case in which the valid level signal received by the first time-length selection signal line DT_MUX_1 is a single pulse signal and the valid level signal received by the second time-length selection signal line DT_MUX_2 is a single pulse signal as an example. FIG. **21** is illustrated by taking a case that the valid level signal received by the second time-length selection signal line DT_MUX_2 is a multiple pulse signal when the valid level signal received by the first time-length selection signal line DT_MUX_1 is a multiple pulse signal as an example. When the valid level signal received by the first time-length selection signal line DT_MUX_1 is a multiple pulse signal and the valid level signal received by the second time-length selection signal line DT_MUX_2 is a multiple pulse signal, the time length of the valid level signal received by the first time-length selection signal line DT_MUX_1 is equal to the sum of the time lengths of the multiple pulse signals, and the time length of the valid level signal received by the second time-length selection signal line DT_MUX_2 is equal to the sum of the time lengths of the multiple pulse signals. FIG. **21** is illustrated by taking a case that the valid level signal received by the first time-length selection signal line DT_MUX_1 and the valid level signal received by the second time-length selection signal line DT_MUX_2 include two pulse signals as an example.

In some possible implementations, the time for the first current selection signal line DI_MUX_1 to receive the valid level signal is within the time for the scanning signal line connected to at least one row of pixel circuits to receive the valid level signal. Exemplarily, as shown in FIGS. **20** and **21**, the time for the first current selection signal line DI_MUX_1 to receive the valid level signal is within the time for the scanning signal line S_i connected to the i^{th} row of pixel circuits to receive the valid level signal, and the time for the first current selection signal line DI_MUX_1 to receive the valid level signal is within the time for the scanning signal line S_{i+1} connected to the $(i+1)^{th}$ row of pixel circuits to receive the valid level signal.

In some possible implementations, the time for the second current selection signal line DI_MUX_2 to receive the valid level signal is within the time for the scanning signal line connected to at least one row of pixel circuits to receive the valid level signal. Exemplarily, as shown in FIGS. **20** and **21**, the time for the second current selection signal line DI_MUX_2 to receive the valid level signal is within the time for the scanning signal line S_i connected to the i^{th} row of pixel circuits to receive the valid level signal, and the time for the second current selection signal line DI_MUX_2 to receive the valid level signal is within the time for the scanning signal line S_{i+1} connected to the $(i+1)^{th}$ row of pixel circuits to receive the valid level signal.

In an exemplary embodiment, as shown in FIGS. **20** and **21**, within the time for the scanning signal line connected to at least one row of pixel circuits to receive the valid level signal, the valid level signal received by the first current selection signal line DI_MUX_1 is a single pulse signal, and the valid level signal received by the second current selection signal line DI_MUX_2 is a single pulse signal.

In some possible implementations, as shown in FIGS. **20** and **21**, the time for the first current selection signal line DI_MUX_1 to receive the valid level signal and the time for the second current selection signal line DI_MUX_2 to receive the valid level signal do not overlap, and the sum of the time length t**21** for the first current selection signal line DI_MUX_1 to receive the valid level signal and the time length t**22** for the second current selection signal line DI_MUX_2 to receive the valid level signal is less than the time length t**2** for the scanning signal line connected to at least one row of pixel circuits to receive the valid level signal.

In some possible implementations, as shown in FIG. **20**, the display panel further includes 4M control signal lines, and a m^{th} row of pixel circuits are connected to a $(4m-3)^{th}$ control signal line, a $(4m-2)^{th}$ control signal line, a $(4m-1)^{th}$ control signal line, and a $(4m)^{th}$ control signal line, respectively. An i^{th} row of pixel circuits are connected to a $(4i-3)^{th}$ control signal line CTL_{4i-3}, a $(4i-2)^{th}$ control signal line CTL_{4i-2}, a $(4i-1)^{th}$ control signal line CTL_{4i-1}, and a $(4i)^{th}$ control signal line CTL_{4i}. An $(i+1)^{th}$ row of pixel circuits are connected to a $(4i+1)^{th}$ control signal line CTL_{4i+1}, the $(4i+2)^{th}$ control signal line CTL_{4i+2}, a $(4i+3)^{th}$ control signal line CTL_{4i-1}, and a $(4i+4)^{th}$ control signal line CTL_{4i}.

In some possible implementations, the drive method for the display panel may further include providing a valid level signal to the control signal lines. When the m^{th} row of pixel units display, the time for the $(4m-3)^{th}$ control signal line to receive the valid level signal, the time for the $(4m-2)^{th}$ control signal line to receive the valid level signal, the time for the $(4m-1)^{th}$ control signal line to receive the valid level signal and the time for the $(4m)^{th}$ control signal line to receive the valid level signal are within the time for the reset signal line connected to the m^{th} row of pixel circuits to receive the valid level signal, and the time for the $(4m-3)^{th}$ control signal line to receive the valid level signal, the time for the $(4m-2)^{th}$ control signal line to receive the valid level signal, the time for the $(4m-1)^{th}$ control signal line to receive the valid level signal and the time for the $(4m)^{th}$ control signal line to receive the valid level signal do not overlap. Exemplarily, as shown in FIGS. **20** and **21**, when the i^{th} row of pixel units display, the time for the $(4i-3)^{th}$ control signal line CTL_{4i-3} to receive the valid level signal, the time for the $(4i-2)^{th}$ control signal line CTL_{4i-2} to receive the valid level signal, the time for the $(4i-1)^{th}$ control signal line CTL_{4i-1} to receive the valid level signal and the time for the $(4i)^{th}$ control signal line CTL_{4i} to receive the valid level signal are within the time for the reset signal line RL_i connected to the i^{th} row of pixel units to receive the valid level signal, and the time for the $(4i-3)^{th}$ control signal line CTL_{4i-3} to receive the valid level signal, the time for the $(4i-2)^{th}$ control signal line CTL_{4i-2} to receive the valid level signal, the time for the $(4i-1)^{th}$ control signal line CTL_{4i-1} to receive the valid level signal and the time for the $(4i)^{th}$ control signal line CTL_{4i} to receive the valid level signal do not overlap. When the $(i+1)^{th}$ row of pixel units display, the time for the $(4i+1)^{th}$ control signal line CTL_{4i+1} to receive the valid level signal, the $(4i+2)^{th}$ control signal line CTL_{4i+2} to receive the valid level signal, the $(4i+3)^{th}$ control signal line CTL_{4i+3} to receive the valid level signal and the $(4i+4)^{th}$ control signal line CTL_{4i+4} to receive the valid level signal within the time for the reset signal line RL_{i+1} connected to the $(i+1)^{th}$ row of pixel circuits to receive the valid level signal, and the time for the $(4i+1)^{th}$ control signal line CTL_{4i+1} to receive the valid level signal, the $(4i+2)^{th}$ control signal line CTL_{4i+2} to receive the valid level signal, the $(4i+3)^{th}$ control signal line CTL_{4i+3} to receive the valid level signal and the $(4i+4)^{th}$ control signal line CTL_{4i+4} to receive the valid level signal do not overlap.

In some possible implementations, as shown in FIG. **20**, the pixel circuits in odd columns of the m^{th} row are electrically connected to the $(4m-3)^{th}$ control signal line and the $(4m-2)^{th}$ control signal line respectively, the pixel circuits in even columns of the m^{th} row are electrically connected to the $(4m-1)^{th}$ control signal line and the $(4m)^{th}$ control signal line respectively, the time-length data lines connected to the pixel circuits in odd columns are connected to the first time-length selection signal line DT_MUX_1, and when the time-length data lines connected to the pixel circuits in even columns are connected to the second time-length selection signal line DT_MUX_2, the time for the $(4m-3)^{th}$ control signal line to receive the valid level signal and the time for the $(4m-2)^{th}$ control signal line to receive the valid level signal are within the time for the first time-length selection signal line DT_MUX_1 to receive the valid level signal, and the time for the $(4m-1)^{th}$ control signal line to receive the valid level signal and the time for the $(4m)^{th}$ control signal line CTL_{4i-3} to receive the valid level signal are within the time for the second time-length selection signal line DT_MUX_2 to receive the valid level signal. Exemplarily, the time for the $(4i-3)^{th}$ control signal line CTL_{4i-3} to receive the valid level signal and the time for the $(4i-2)^{th}$ control signal line CTL_{4i-2} to receive the valid level signal are within the time for the first time-length selection signal line DT_MUX_1 to receive the valid level signal, and the time for the $(4i-1)^{th}$ control signal line CTL_{4i-1} to receive the valid level signal and the time for the $(4i)^{th}$ control signal line CTL_{4i} to receive the valid level signal are within the time for the second time-length selection signal line DT_MUX_2 to receive the valid level signal. The time for the $(4i+1)^{th}$ control signal line CTL_{4i+1} to receive the valid level signal and the time for the $(4i+2)^{th}$ control signal line CTL_{4i+2} to receive the valid level signal are within the time for the first time-length selection signal line DT_MUX_1 to receive the valid level signal. The time for the $(4i+3)^{th}$ control signal line CTL_{4i+3} to receive the valid level signal and the time for the $(4i+4)^{th}$ control signal line CTL_{4i+4} to receive the valid level signal are within the time for the second time-length selection signal line DT_MUX_2 to receive the valid level signal.

In some possible implementations, as shown in FIG. **20**, the sum of the time length t**13** for the $(4m-3)^{th}$ control signal line to receive the valid level signal and the time length t**14** for the $(4m-2)^{th}$ control signal line to receive the valid level signal is less than the time length t**11** for the first time-length selection signal line to receive the valid level signal.

In some possible implementations, as shown in FIG. **20**, the sum of the time length t**15** for the $(4m-1)^{th}$ control signal line to receive the valid level signal and the time length t**16** for the $(4m)^{th}$ control signal line to receive the valid level signal is less than the time length t**12** for the second time-length selection signal line to receive the valid level signal.

In some possible implementations, the display panel further includes 2M control signal lines, the m^{th} row of pixel circuits are connected to a $(2m-1)^{th}$ control signal line and a $(2m)^{th}$ control signal line respectively, and M is the total number of rows of the pixel circuits.

Exemplarily, the i^{th} row of pixel circuits are connected to a $(2i-1)^{th}$ control signal line CTL_{2i-1} and the $(2i)^{th}$ control signal line CTL_{2i}, respectively, and the $(i+1)^{th}$ row of pixel circuits are connected to a $(2i+1)^{th}$ control signal line CTL_{2i+1} and a $(2i+2)^{th}$ control signal line CTL_{2i+2}, respectively.

In some possible implementations, the drive method for a display panel may further include providing a valid level signal to the control signal lines. When the m^{th} row of pixel units display, the time for the $(2m-1)^{th}$ control signal line to receive the valid level signal and the time for the $(2m)^{th}$ control signal line to receive the valid level signal are within the time for the reset signal line connected to the m^{th} row of pixel circuits to receive the valid level signal, and the time for the $(2m-1)^{th}$ control signal line to receive the valid level signal and the time for the $(2m)^{th}$ control signal line to receive the valid level signal do not overlap. Exemplarily, as shown in FIG. **21**, when the i^{th} row of pixel units display, the time for the $(2i-1)^{th}$ control signal line CTL_{2i-1} to receive the valid level signal and the time for the $(2i)^{th}$ control signal line CTL_{2i} to receive the valid level signal are within the time for the reset signal line RL_i connected to the i^{th} row of pixel units to receive the valid level signal, and the time for the $(2i-1)^{th}$ control signal line CTL_{2i-1} to receive the valid level signal and the time for the $(2i)^{th}$ control signal line CTL_{2i} to receive the valid level signal do not overlap. When the $(i+1)^{th}$ row of pixel units display, the time for the $(2i+1)^{th}$ control signal line CTL_{2i+1} to receive the valid level signal and the time for the $(2i+2)^{th}$ control signal line CTL_{2i+1} to receive the valid level signal are within the time for the reset signal line RL_{i+1} connected to the $(i+1)^{th}$ row of pixel circuits to receive the valid level signal, and the time for the $(2i+1)^{th}$ control signal line CTL_{2i+1} to receive the valid level signal and the time for the $(2i+2)^{th}$ control signal line CTL_{2i+2} to receive the valid level signal do not overlap.

In some possible implementations, as shown in FIG. **21**, within the time for the reset signal line connected to at least one row of pixel circuits to receive the valid level signal, the valid level signal received by the first time-length control signal line DT_MUX_1 includes two first pulse signals and the valid level signal received by the second time-length control signal line DT_MUX_2 includes two second pulse signals, the first pulse signals and the second pulse signals are alternately produced. The time for the first time-length control signal line DT_MUX_1 to receive one of the first pulse signals is within the time for one of the control signal lines connected to at least one row of pixel circuits to receive the valid level signal when the at least one row of pixel circuits display, and the time for the first time-length control signal line DT_MUX_1 to receive another first pulse signal is within the time for another control signal line connected to at least one row of pixel circuits to receive the valid level signal when the at least one row of pixel circuits display; the time for the second time-length control signal line DT_MUX_2 to receive one of the second pulse signals is within the time for one of the control signal lines connected to at least one row of pixel circuits to receive the valid level signal when the at least one row of pixel circuits display, and the time for the second time-length control signal line DT_MUX_2 to receive another second pulse signal is within the time for another control signal line connected to at least one row of pixel circuits to receive the valid level signal when the at least one row of pixel circuits display.

In some possible implementations, the sum of the time length for the first pulse signal and the time length for the second pulse signal within the time for one of the control signal lines connected to at least one row of pixel circuits to receive the valid level signal when the at least one row of pixel circuits display is less than the time length for one of the control signal lines connected to at least one row of pixel circuits to receive the valid level signal when the at least one row of pixel circuits display. The sum of the time length for the first pulse signal and the time length for the second pulse signal within the time for another control signal line connected to at least one row of pixel circuits to receive the valid level signal when the at least one row of pixel circuits display is less than the time length for another control signal line connected to at least one row of pixel circuits to receive the valid level signal when the at least one row of pixel circuits display. Exemplarily, the sum of the time length t**111** of the first pulse signal and the time length t**121** of the second pulse signal within the time for the $(2i-1)^{th}$ control signal line CTL_{2i-1} connected to the i^{th} row of pixel circuits to receive the valid level signal when the i^{th} row of pixel circuits display is less than the time length t**17** for the $(2i-1)^{th}$ control signal line CTL_{2i-1} connected to the i^{th} row of pixel circuits to receive the valid level signal when the i^{th} row of pixel circuits display, and the sum of the time length t**112** of the first pulse signal and the time length t**122** of the second pulse signal within the time for the $(2i)^{th}$ control signal line CTL_{2i} connected to the i^{th} row of pixel circuits to receive the valid level signal when the i^{th} row of pixel circuits display is less than the time length t**18** for the $(2i)^{th}$ control signal line CTL_{2i} connected to the i^{th} row of pixel circuits to receive the valid level signal when the i^{th} row of pixel circuits display, and the sum of the time length t**111** of the first pulse signal and the time length t**121** of the second pulse signal within the time for the $(2i+1)^{th}$ control signal line CTL_{2i+1} connected to the $(i+1)^{th}$ row of pixel circuits to receive the valid level signal when the $(i+1)^{th}$ row of pixel circuits display is less than the time length t**17** for the $(2i+1)^{th}$ control signal line CTL_{2i+1} connected to the $(i+1)^{th}$ row of pixel circuits to receive the valid level signal when the $(i+1)^{th}$ row of pixel circuits display. The sum of the time length t**112** of the first pulse signal and the time length t**122** of the second pulse signal within the time for the $(2i+2)^{th}$ control signal line CTL_{2i+2} connected to the $(i+1)^{th}$ row of pixel circuits to receive the valid level signal when the $(i+1)^{th}$ row of pixel circuits display is less than the time length t**18** for the $(2i+2)^{th}$ control signal line CTL_{2i+2} connected to the $(i+1)^{th}$ row of pixel circuits to receive the valid level signal when the $(i+1)^{th}$ row of pixel circuits display.

The display panel is the display panel according to any one of the foregoing embodiments, and the implementation principle and implementation effects are similar, which will not be repeated here.

The accompanying drawings of the present disclosure only involve the structures involved in the embodiments of the present disclosure, and the other structures may refer to conventional designs.

Although the implementations of the present disclosure are disclosed above, the contents are only implementations adopted to easily understand the present disclosure and not intended to limit the present disclosure. Any of those skilled in the art of the present disclosure can make any modifications and variations in the implementation manner and details without departing from the spirit and scope of the present disclosure. However, the protection scope of the present disclosure should be subject to the scope defined by the appended claims.

The invention claimed is:

1. A drive method for a display panel, wherein:

the display panel comprises: pixel circuits arranged in array, a plurality of current data lines, a plurality of time-length data lines, a first current selection signal line, a second current selection signal line, a first time-length selection signal line and a second time-length selection signal line;

the pixel circuits are respectively connected with the current data lines and the time-length data lines, at least one current data line is connected with the first current selection signal line or the second current selection signal line, two adjacent current data lines are connected with different current selection signal lines, at least one time-length data line is connected with the first time-length selection signal line or the second time-length selection signal line, and two adjacent time-length data lines are connected with different time-length selection signal lines;

the method comprises: providing a valid level signal to the first time-length selection signal line, the second time-length selection signal line, the first current selection signal line and the second current selection signal line; and

time for at least two signal lines of the first time-length selection signal line, the second time-length selection signal line, the first current selection signal line and the second current selection signal line to receive the valid level signal is not overlapped;

wherein:

the display panel further comprises: a reset signal line, a scanning signal line, and a light-emitting signal line, the pixel circuits are respectively connected with the reset signal line, the scanning signal line and the light-emitting signal line;

the method further comprises: providing a valid level signal to the reset signal line, the scanning signal line and the light-emitting signal line; and

time for at least two signal lines of the reset signal line, the scanning signal line and the light-emitting signal line connected to a same pixel circuit to receive the valid level signal is not overlapped;

wherein: the time for the reset signal line connected to a $(m+1)^{th}$ row of pixel circuits to receive the valid level signal is within the time for the light-emitting signal line connected to a m^{th} row of pixel circuits to receive the valid level signal, and $1 \leq m \leq M$ and M is a total number of rows of the pixel circuits.

2. The method according to claim **1**, wherein the time for the first time-length selection signal line to receive the valid level signal is within the time for the reset signal line connected to at least one row of pixel circuits to receive the valid level signal.

3. The method according to claim **2**, wherein the time for the first time-length selection signal line to receive the valid level signal and the time for the second time-length selection signal line to receive the valid level signal are not overlapped, and a sum of a time length for the first time-length selection signal line to receive the valid level signal and a time length for the second time-length selection signal line to receive the valid level signal is less than a time length for the reset signal line connected to at least one row of pixel circuits to receive the valid level signal.

4. The method according to claim **1**, wherein the time for the second time-length selection signal line to receive the valid level signal is within the time for the reset signal line connected to at least one row of pixel circuits to receive the valid level signal.

5. The method according to claim **4**, wherein the time for the first time-length selection signal line to receive the valid level signal and the time for the second time-length selection signal line to receive the valid level signal are not overlapped, and a sum of a time length for the first time-length selection signal line to receive the valid level signal and a time length for the second time-length selection signal line to receive the valid level signal is less than a time length for the reset signal line connected to at least one row of pixel circuits to receive the valid level signal.

6. The method according to claim **1**, wherein the time for the first current selection signal line to receive the valid level signal is within the time for the scanning signal line connected to at least one row of pixel circuits to receive the valid level signal.

7. The method according to claim **6**, wherein the time for the first current selection signal line to receive the valid level signal and the time for the second current selection signal line to receive the valid level signal are not overlapped, and a sum of a time length for the first current selection signal line to receive the valid level signal and a time length for the second current selection signal line to receive the valid level signal is less than a time length for the scanning signal line connected to at least one row of pixel circuits to receive the valid level signal.

8. The method according to claim **1**, wherein the time for the second current selection signal line to receive the valid level signal is within the time for the scanning signal line connected to at least one row of pixel circuits to receive the valid level signal.

9. The method according to claim **8**, wherein the time for the first current selection signal line to receive the valid level signal and the time for the second current selection signal line to receive the valid level signal are not overlapped, and a sum of a time length for the first current selection signal line to receive the valid level signal and a time length for the second current selection signal line to receive the valid level signal is less than a time length for the scanning signal line connected to at least one row of pixel circuits to receive the valid level signal.

10. The method according to claim **1**, wherein:

the display panel further comprises: 4M control signal lines, wherein the m^{th} row of pixel circuits are connected with a $(4m-3)^{th}$ control signal line, a $(4m-2)^{th}$ control signal line, a $(4m-1)^{th}$ control signal line and a $(4m)^{th}$ control signal line, respectively; and

the method further comprises: providing a valid level signal to the control signal lines; and

in a case that the m^{th} row of pixel units are used for display, time for the $(4m-3)^{th}$ control signal line to receive the valid level signal, time for the $(4m-2)^{th}$ control signal line to receive the valid level signal, time for the $(4m-1)^{th}$ control signal line to receive the valid level signal and time for the $(4m)^{th}$ control signal line to receive the valid level signal are within the time for the reset signal line connected to the m^{th} row of pixel circuits to receive the valid level signal, and the time for the $(4m-3)^{th}$ control signal line to receive the valid level signal, the time for the $(4m-2)^{th}$ control signal line to receive the valid level signal, the time for the $(4m-1)^{th}$ control signal line to receive the valid level signal and the time for the $(4m)^{th}$ control signal line to receive the valid level signal are not overlapped.

11. The method according to claim **10**, wherein the pixel circuits in odd columns of the m^{th} row are electrically connected to the $(4m-3)^{th}$ control signal line and the $(4m-2)^{th}$ control signal line respectively, the pixel circuits in even columns of the m^{th} row are electrically connected to the $(4m-1)^{th}$ control signal line and the $(4m)^{th}$ control signal line respectively, the time-length data lines connected to the pixel circuits in odd columns are connected to the first time-length selection signal line, and in a case that the time-length data lines connected to the pixel circuits in even columns are connected to the second time-length selection signal line, the time for the $(4m-3)^{th}$ control signal line to receive the valid level signal and the time for the $(4m-2)^{th}$ control signal line to receive the valid level signal are within the time for the first time-length selection signal line to receive the valid level signal, and the time for the $(4m-1)^{th}$ control signal line to receive the valid level signal and the time for the $(4m)^{th}$ control signal line to receive the valid level signal are within the time for the second time-length selection signal line to receive the valid level signal.

12. The method according to claim **11**, wherein:

a sum of a time length for the $(4m-3)^{th}$ control signal line to receive the valid level signal and a time length for the $(4m-2)^{th}$ control signal line to receive the valid level signal is less than a time length for the first time selection signal line to receive the valid level signal; and

a sum of a time length for the $(4m-1)^{th}$ control signal line to receive the valid level signal and a time length for the $(4m)^{th}$ control signal line to receive the valid level signal is less than a time length for the second time-length selection signal line to receive the valid level signal.

13. The method according to claim 1, wherein:
the display panel further comprises: 2M control signal lines, the m^{th} row of pixel circuits are connected to a $(2m-1)^{th}$ control signal line and a $(2m)^{th}$ control signal line respectively, and M is a total number of rows of the pixel circuits;
the method further comprises: providing a valid level signal to the control signal lines; and
in a case that the m^{th} row of pixel units are used for display, time for the $(2m-1)^{th}$ control signal line to receive the valid level signal and time for the $(2m)^{th}$ control signal line to receive the valid level signal are within the time for the reset signal line connected to the m^{th} row of pixel circuits to receive the valid level signal, and the time for the $(2m-1)^{th}$ control signal line to receive the valid level signal and the time for the $(2m)^{th}$ control signal line to receive the valid level signal are not overlapped.

14. The method according to claim 13, wherein:
within the time for the reset signal line connected to at least one row of pixel circuits to receive the valid level signal, the valid level signal received by the first time-length control signal line comprises two first pulse signals, and the valid level signal received by the second time-length control signal line comprises two second pulse signals, the first pulse signals and the second pulse signals are alternately produced.

15. The method according to claim 14, wherein:
time for the first time-length control signal line to receive one of the first pulse signals is within time for one of the control signal lines connected to at least one row of pixel circuits to receive the valid level signal in a case that the at least one row of pixel circuits are used for display, and time for the first time-length control signal line to receive another first pulse signal is within time for another control signal line connected to at least one row of pixel circuits to receive the valid level signal in a case that the at least one row of pixel circuits are used for display.

16. The method according to claim 15, wherein:
time for the second time-length control signal line to receive one of the second pulse signals is within the time for one of the control signal lines connected to at least one row of pixel circuits to receive the valid level signal in a case that the at least one row of pixel circuits are used for display, and time for the second time-length control signal line to receive another second pulse signal is within the time for another control signal line connected to at least one row of pixel circuits to receive the valid level signal in a case that the at least one row of pixel circuits are used for display.

17. The method according to claim 14, wherein:
a sum of a time length for the first pulse signal and a time length for the second pulse signal within the time for one of the control signal lines connected to at least one row of pixel circuits to receive the valid level signal in a case that the at least one row of pixel circuits are used for display is less than a time length for one of the control signal lines connected to at least one row of pixel circuits to receive the valid level signal in a case that the at least one row of pixel circuits are used for display.

18. The method according to claim 17, wherein:
a sum of the time length for the first pulse signal and the time length for the second pulse signal within the time for another control signal line connected to at least one row of pixel circuits to receive the valid level signal in a case that the at least one row of pixel circuits are used for display is less than a time length for another control signal line connected to at least one row of pixel circuits to receive the valid level signal in a case that the at least one row of pixel circuits are used for display.

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