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(54) **DRIVING CIRCUIT, DRIVING METHOD, AND DISPLAY DEVICE**

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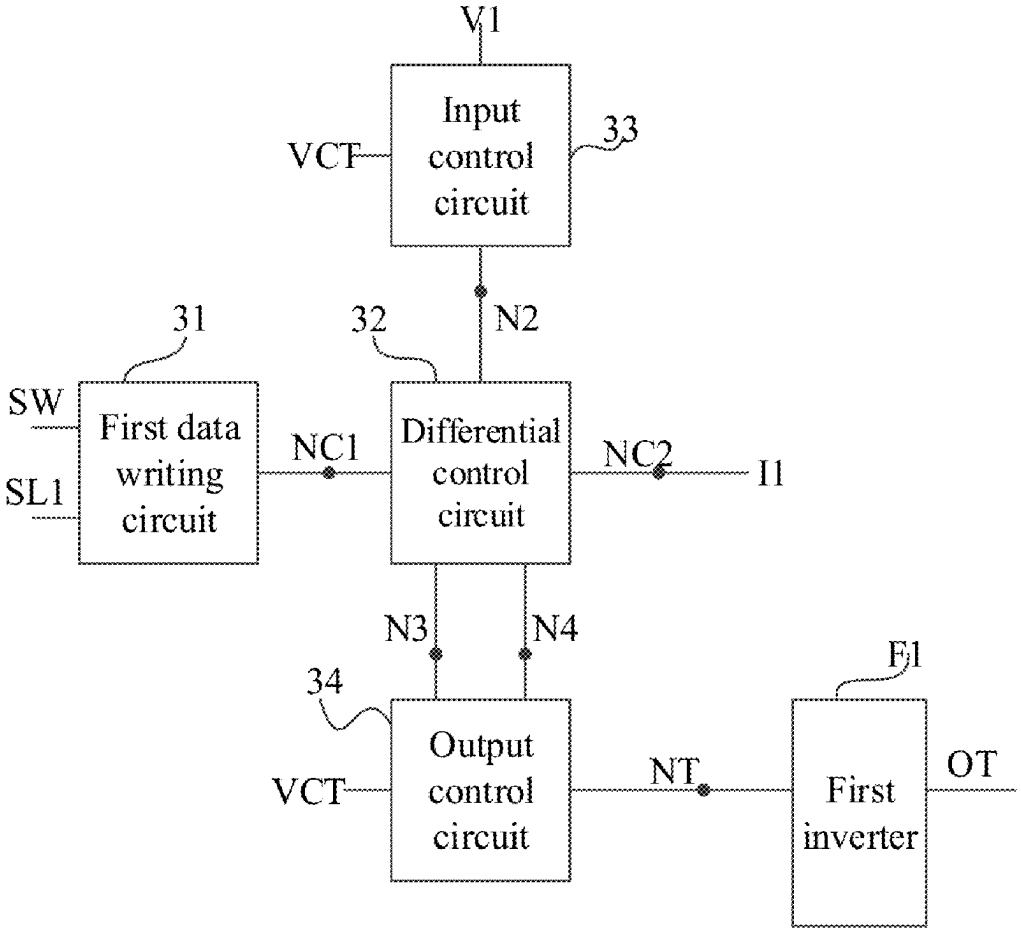
(52) **U.S. Cl.**
CPC ***G09G 3/3225*** (2013.01); *G09G 2310/061* (2013.01); *G09G 2310/08* (2013.01)

(57) **ABSTRACT**

A driving circuit, driving method, and display device are provided. The drive circuit includes output circuit and inverting circuit; the output circuit provides driving output signal via the driving output terminal based on data voltage under control of switch control signal and output control signal; the inverting circuit includes N stages of inverters, N is positive integer; input terminal of first inverter is electrically connected to the driving output terminal, and output terminal of N-th inverter is electrically connected to driving signal output terminal; if N is greater than 1, output terminal of m-th inverter is electrically connected to input terminal of (m+1)-th inverter, m is positive integer less than N; the inverter inverts signal received by its input terminal to obtain inverted signal and output it via its output terminal. The drive circuit has high output stability.



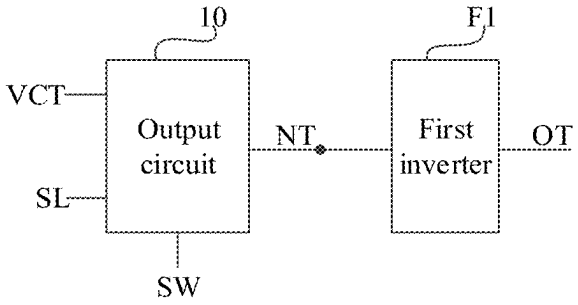


FIG. 1

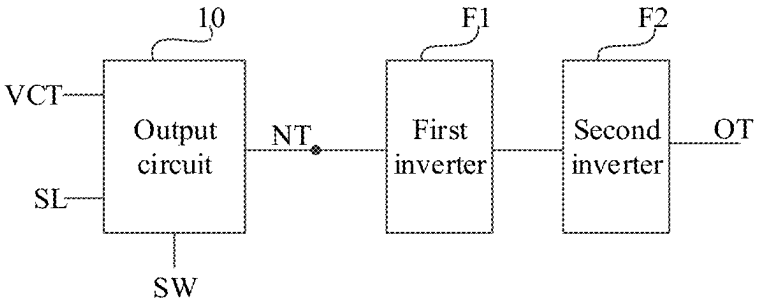


FIG. 2

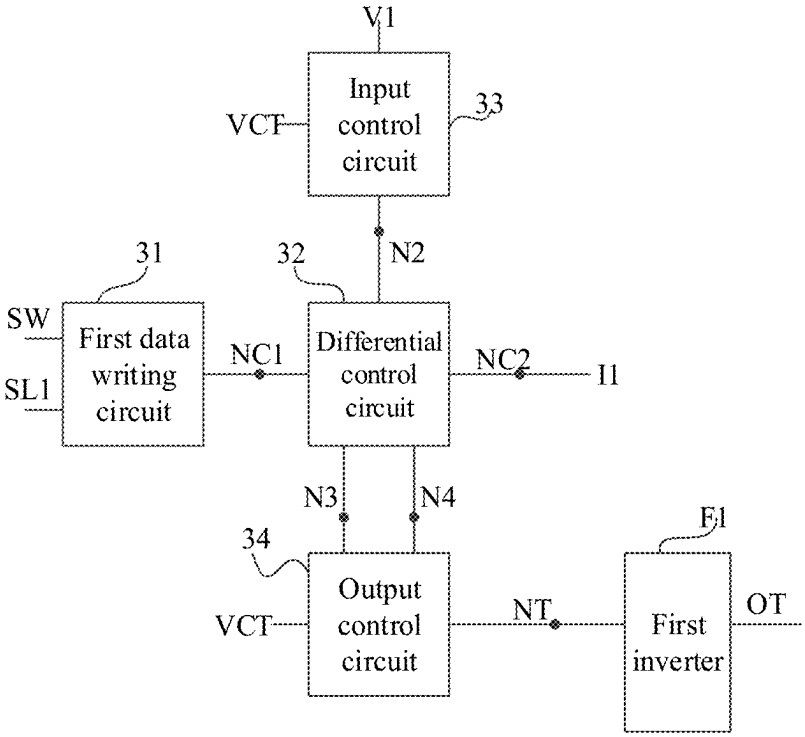


FIG. 3

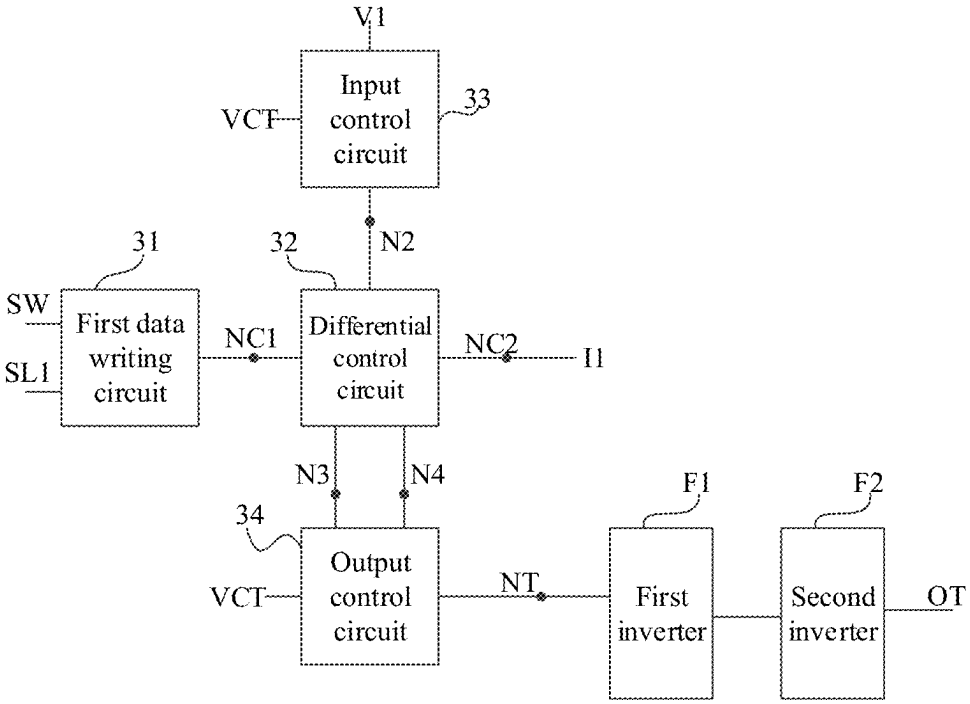

V1
Input control circuit
33
VCT
31
32
N2
SW
First data writing circuit
SL1
NC1
Differential control circuit
NC2
I1
N3
N4
34
F1
F2
Output control circuit
VCT
NT
First inverter
Second inverter
OT

FIG. 4

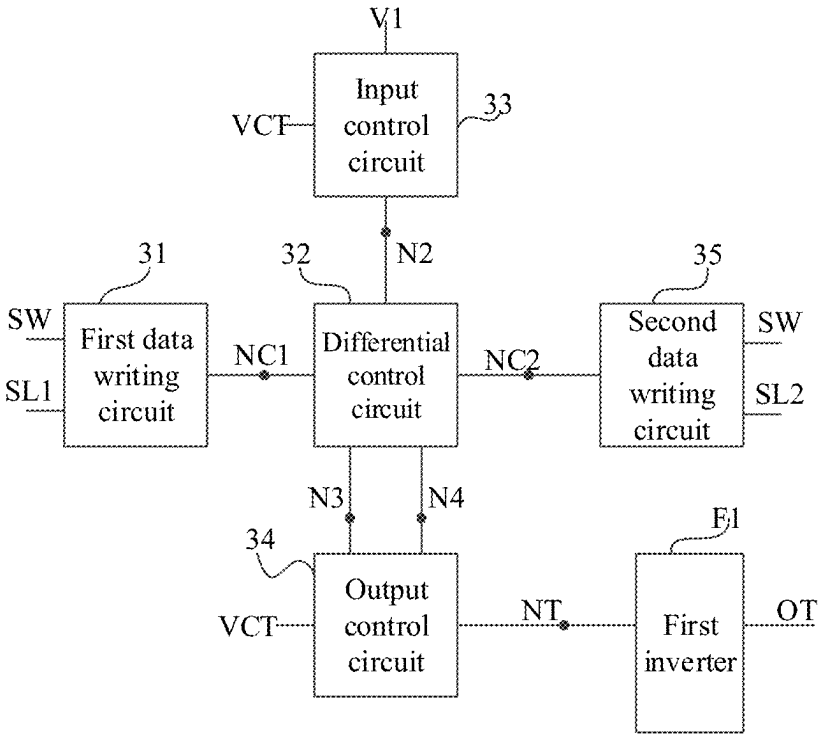

V1
Input control circuit
33
VCT
31
32
N2
35
SW
First data writing circuit
SL1
NC1
Differential control circuit
NC2
Second data writing circuit
SW
SL2
N3
N4
34
F1
Output control circuit
VCT
NT
First inverter
OT

FIG. 5

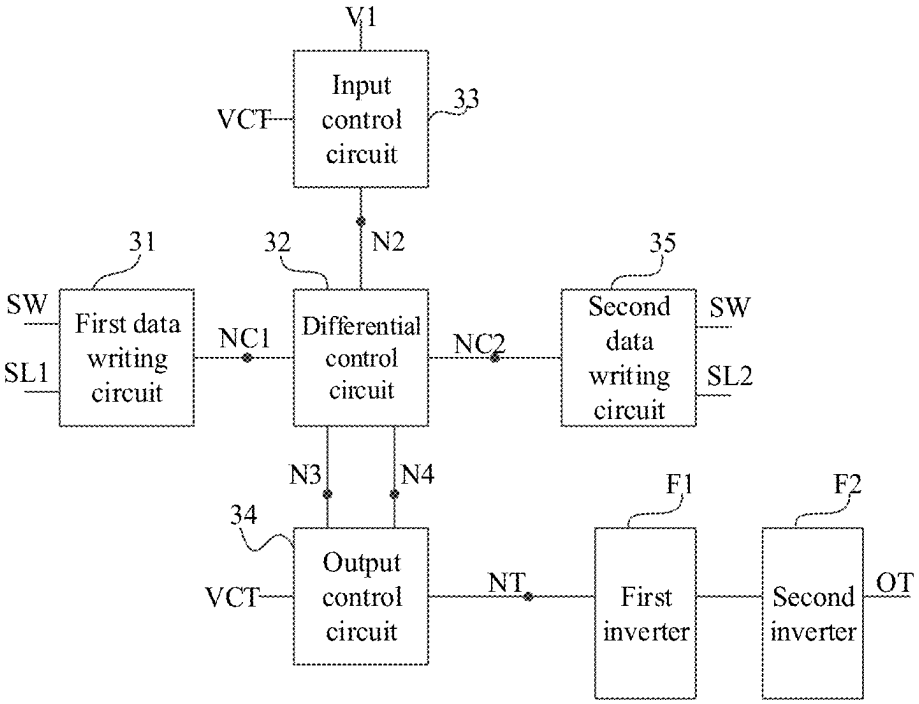

V1
Input control circuit
VCT
33
31
32
N2
35
SW
First data writing circuit
SL1
NC1
Differential control circuit
NC2
Second data writing circuit
SW
SL2
N3
N4
F1
F2
34
Output control circuit
VCT
NT
First inverter
Second inverter
OT

FIG. 6

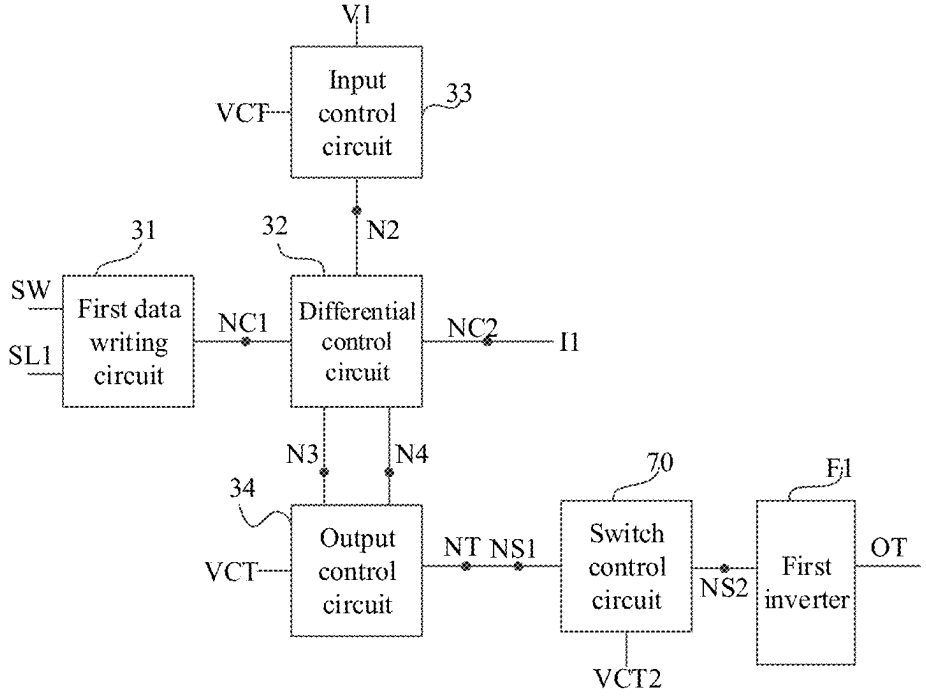

V1
Input control circuit
VCT
33
31
32
N2
SW
First data writing circuit
SL1
NC1
Differential control circuit
NC2
I1
N3
N4
70
F1
34
Output control circuit
VCT
NT NS1
Switch control circuit
NS2
First inverter
OT
VCT2

FIG. 7A

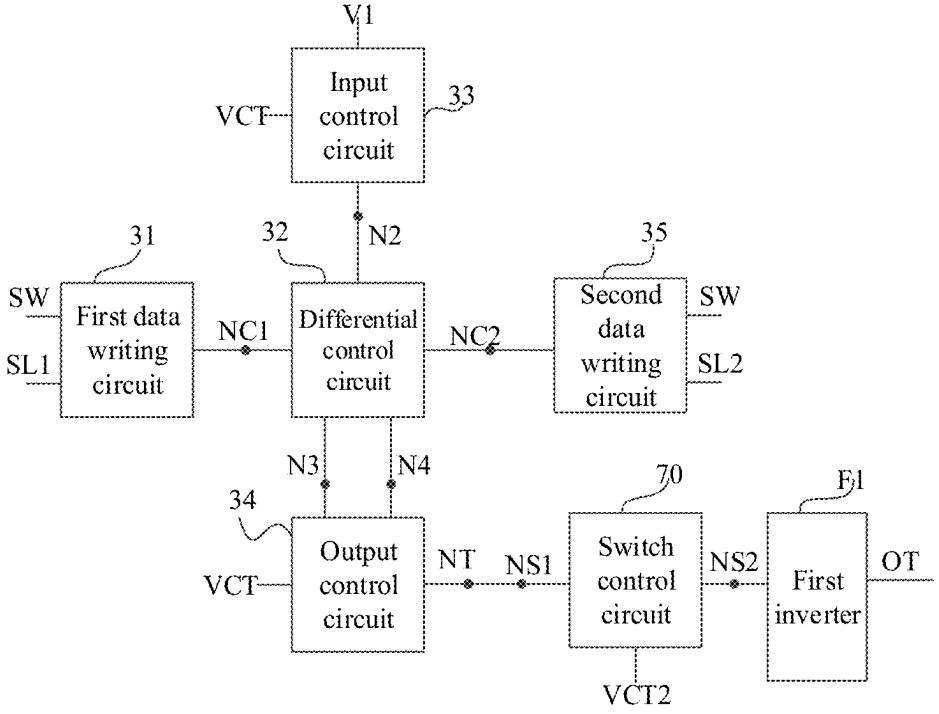

V1
Input control circuit
33
VCT
N2
31
32
35
SW
First data writing circuit
NC1
Differential control circuit
NC2
Second data writing circuit
SW
SL1
SL2
N3
N4
70
F1
34
Output control circuit
NT
NS1
Switch control circuit
NS2
First inverter
OT
VCT
VCT2

FIG. 7B

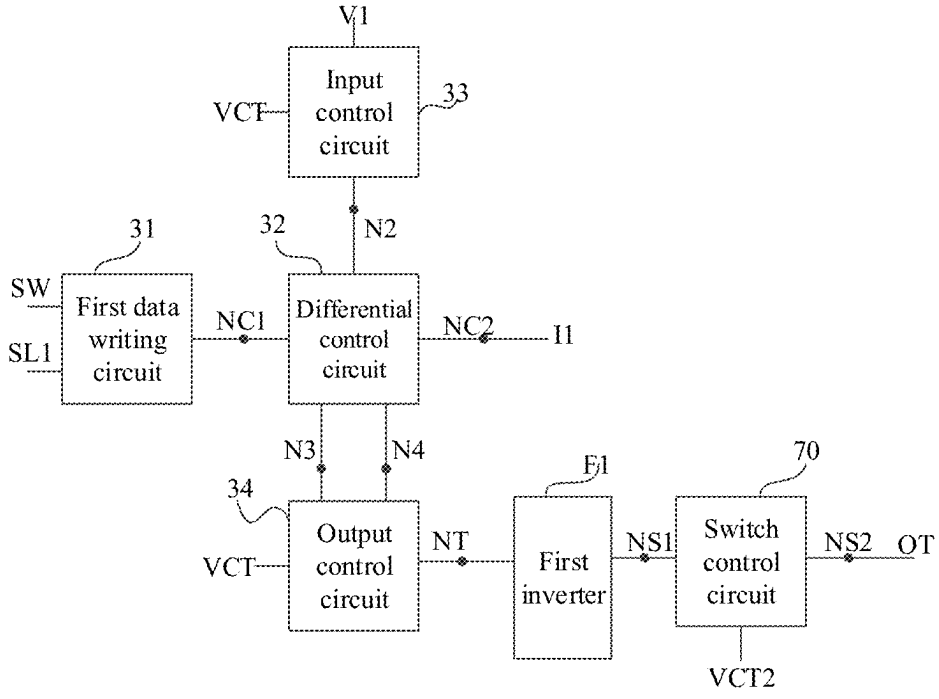

V1
Input control circuit
33
VCT
N2
31
32
SW
First data writing circuit
NC1
Differential control circuit
NC2
I1
SL1
N3
N4
F1
70
34
Output control circuit
NT
First inverter
NS1
Switch control circuit
NS2
OT
VCT
VCT2

FIG. 8A

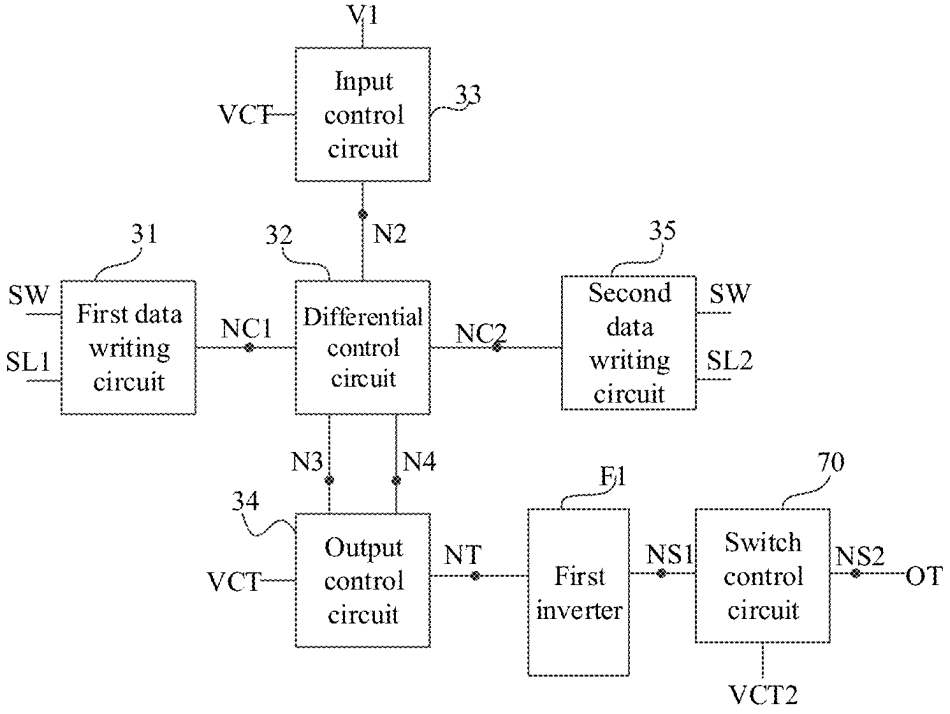

V1
Input control circuit
33
VCT
N2
31
32
35
SW
First data writing circuit
SL1
NC1
Differential control circuit
NC2
Second data writing circuit
SW
SL2
N3
N4
34
F1
70
Output control circuit
VCT
NT
First inverter
NS1
Switch control circuit
NS2
OT
VCT2

FIG. 8B

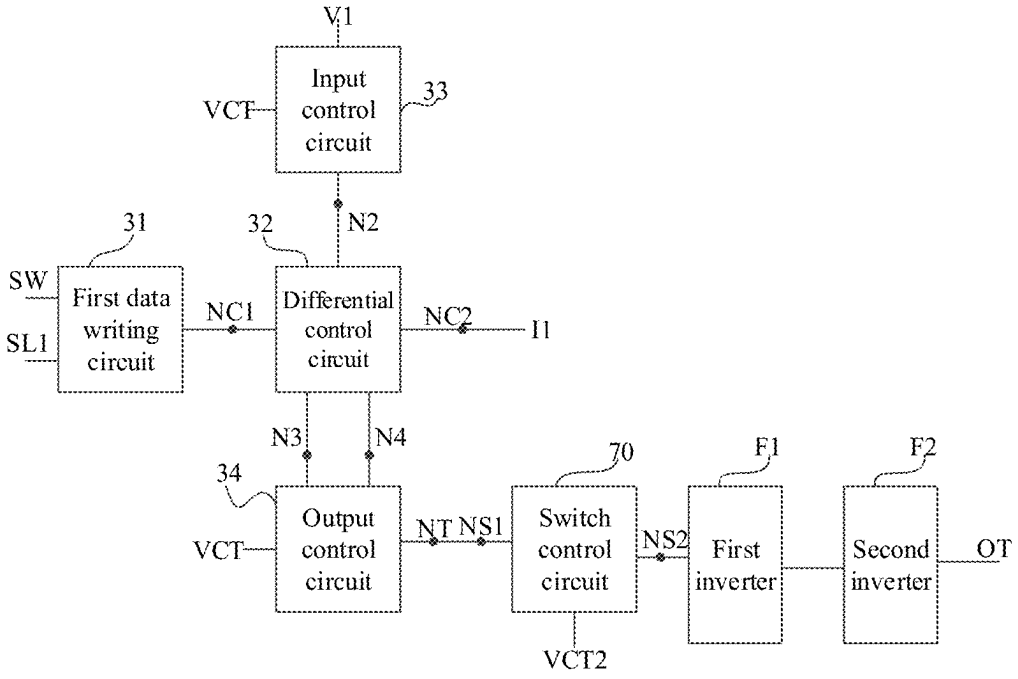

V1
Input control circuit
33
VCT
N2
31
32
SW
First data writing circuit
SL1
NC1
Differential control circuit
NC2
I1
N3
N4
34
70
F1
F2
Output control circuit
VCT
NT
NS1
Switch control circuit
NS2
First inverter
Second inverter
OT
VCT2

FIG. 9A

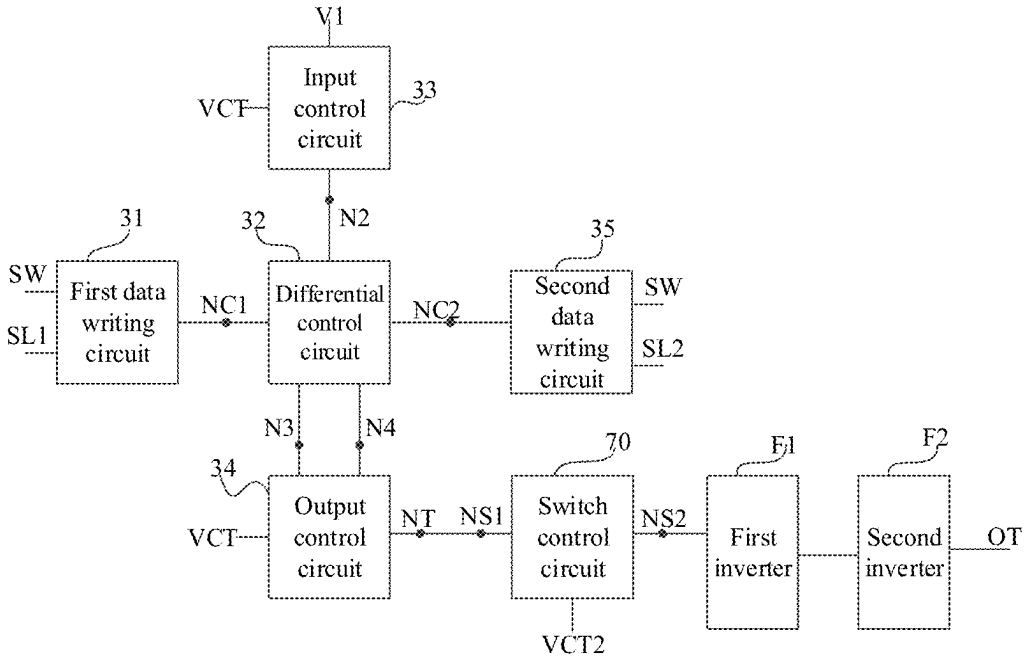


FIG. 9B

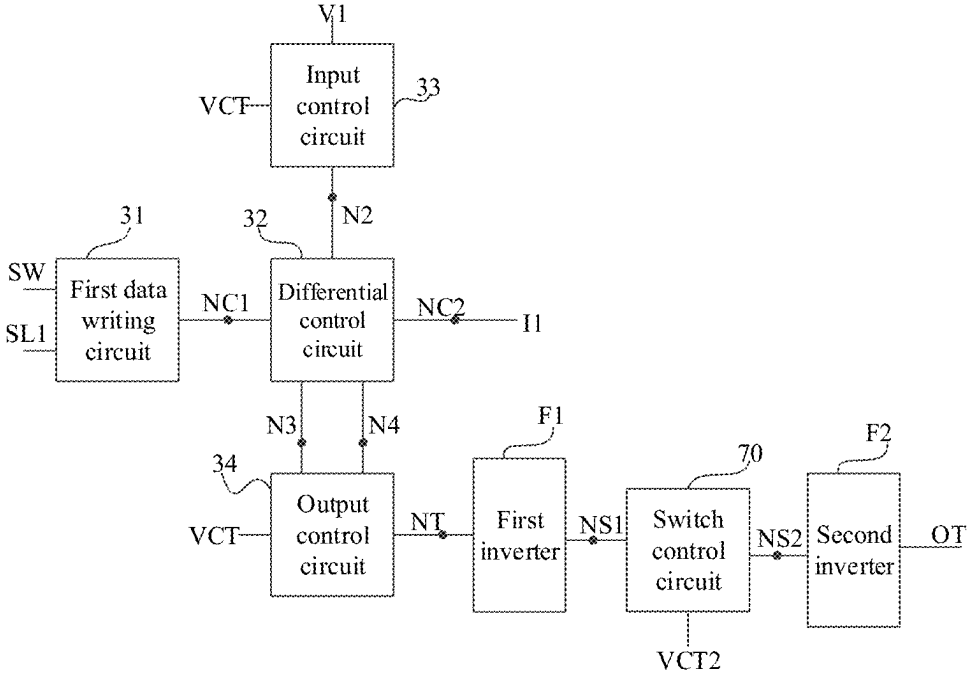


FIG. 10A

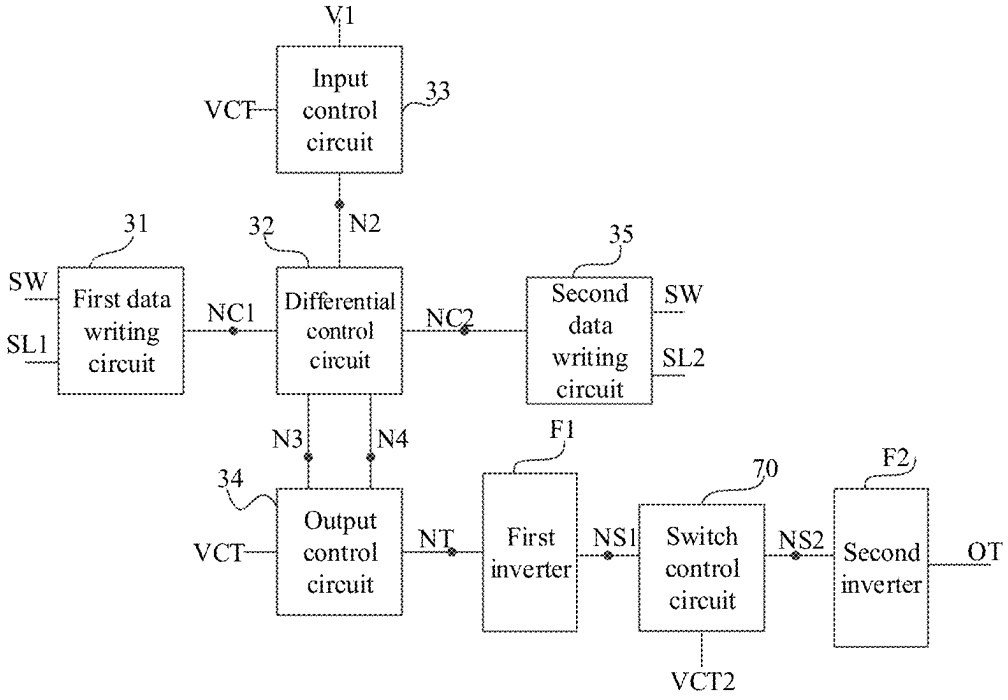


FIG. 10B

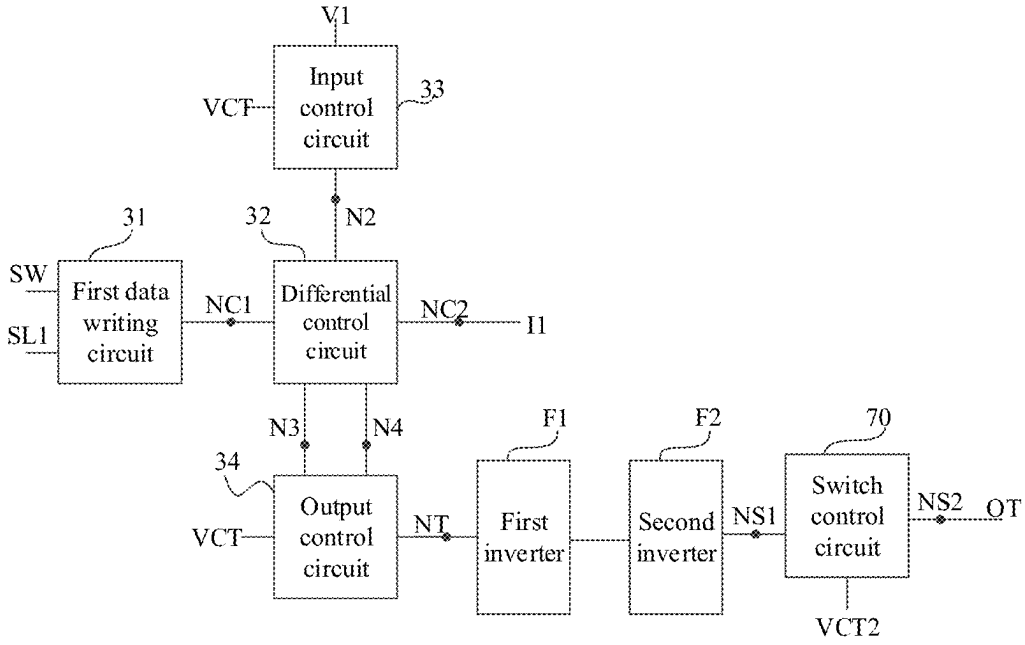


FIG. 11A

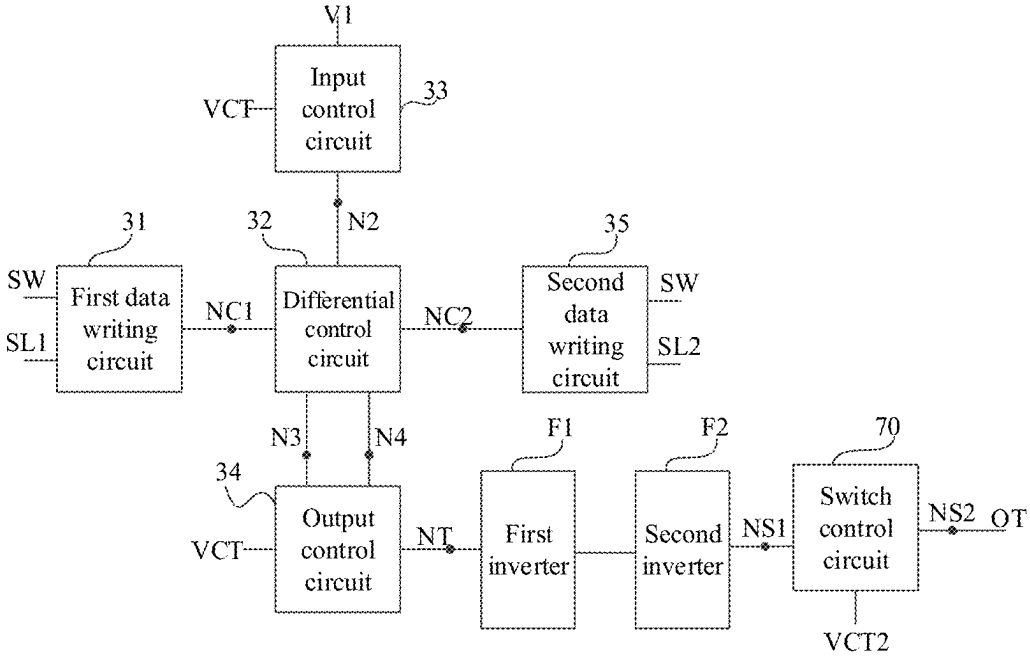


FIG. 11B

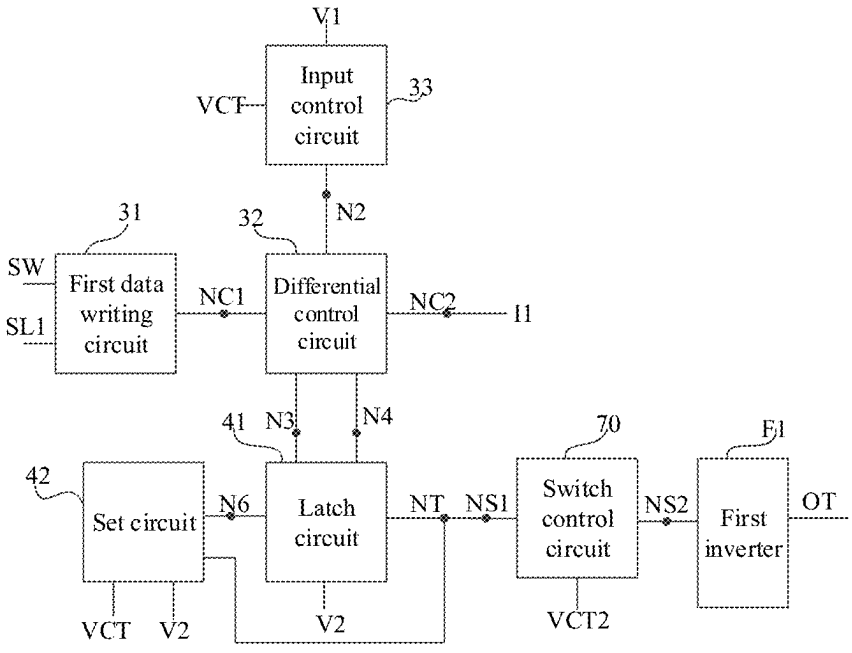


FIG. 12A

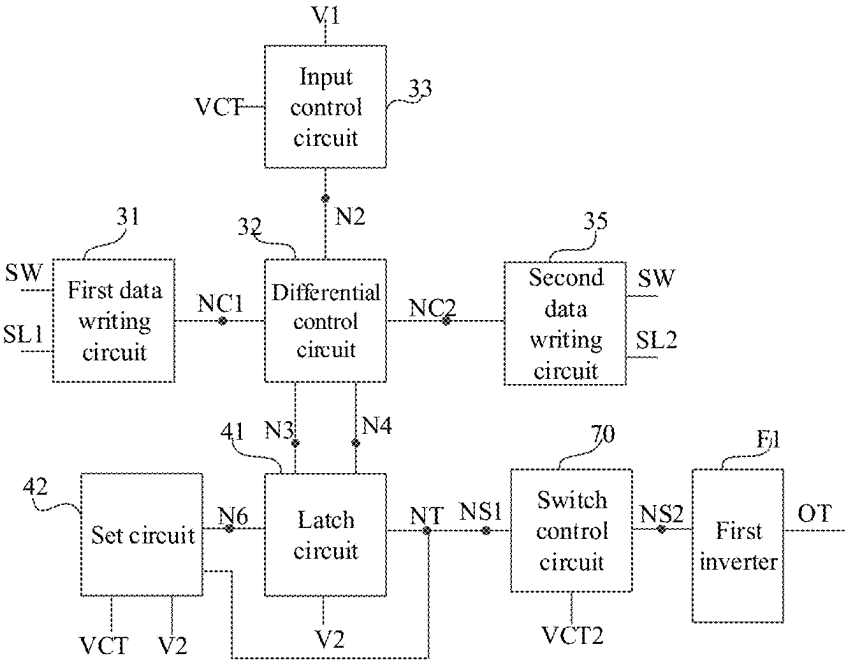


FIG. 12B

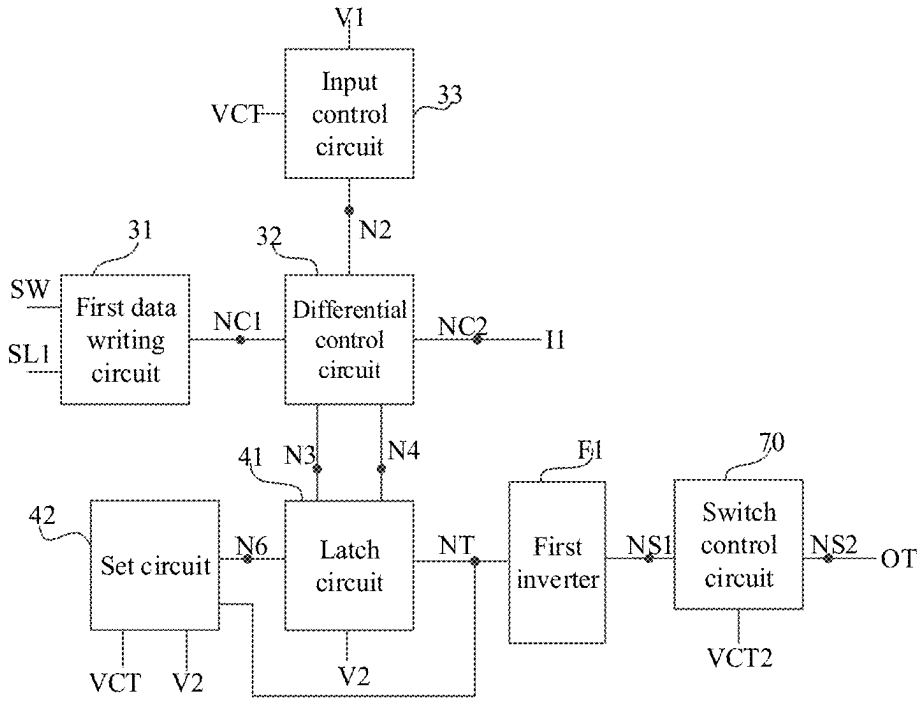


FIG. 13A

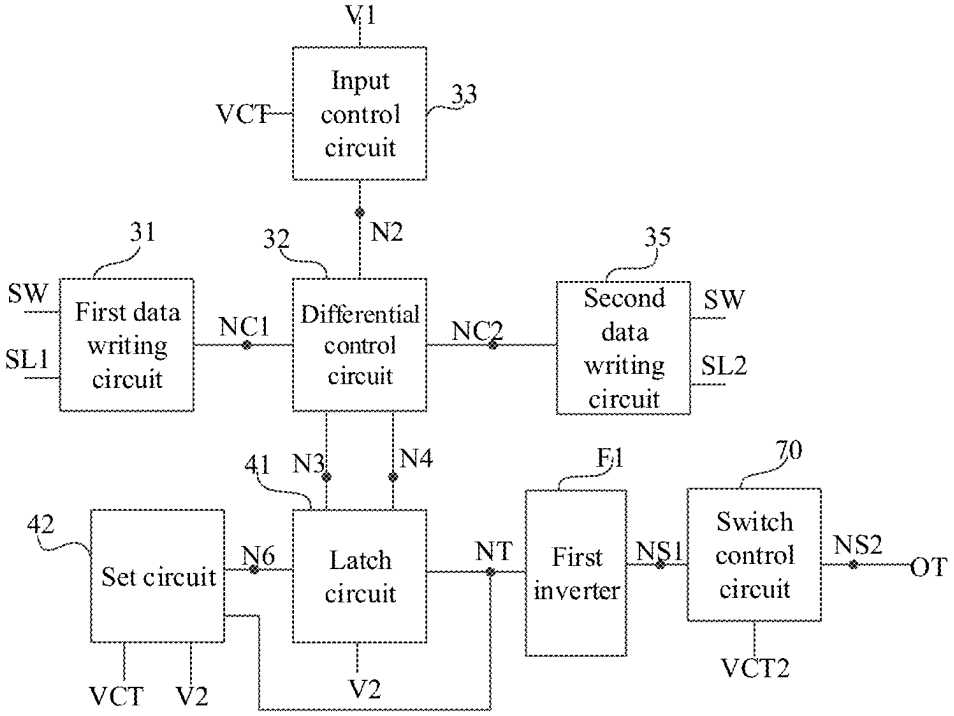


FIG. 13B

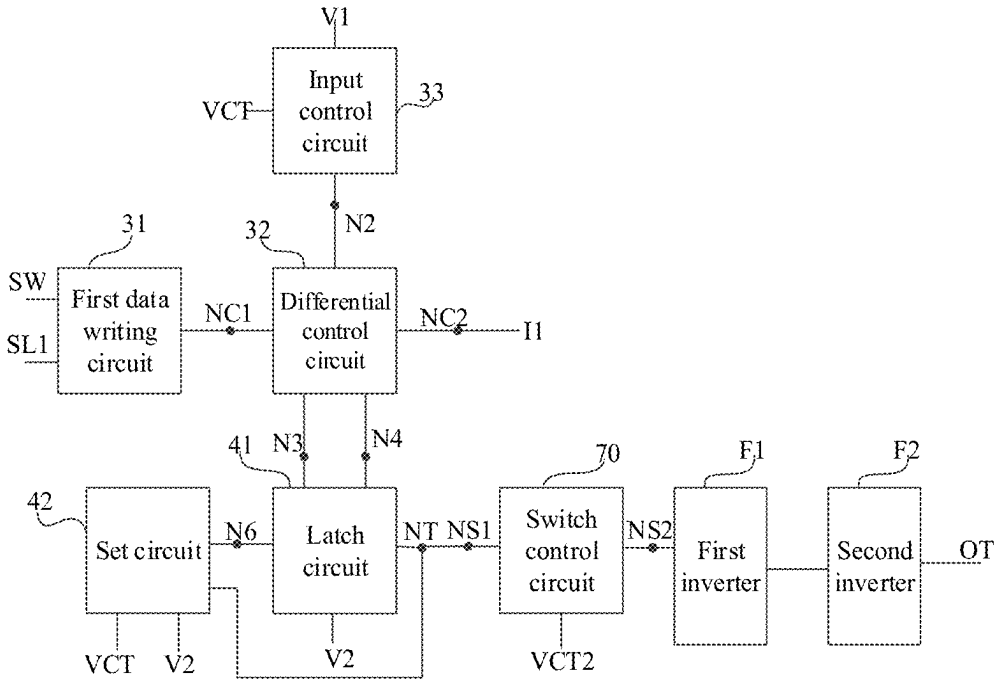


FIG. 14A

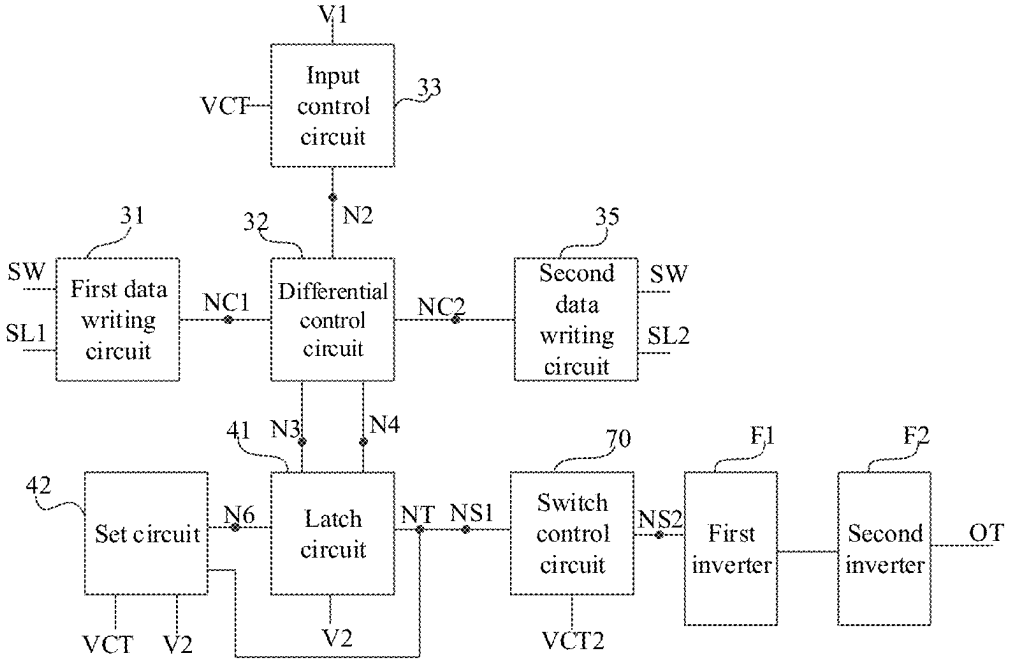


FIG. 14B

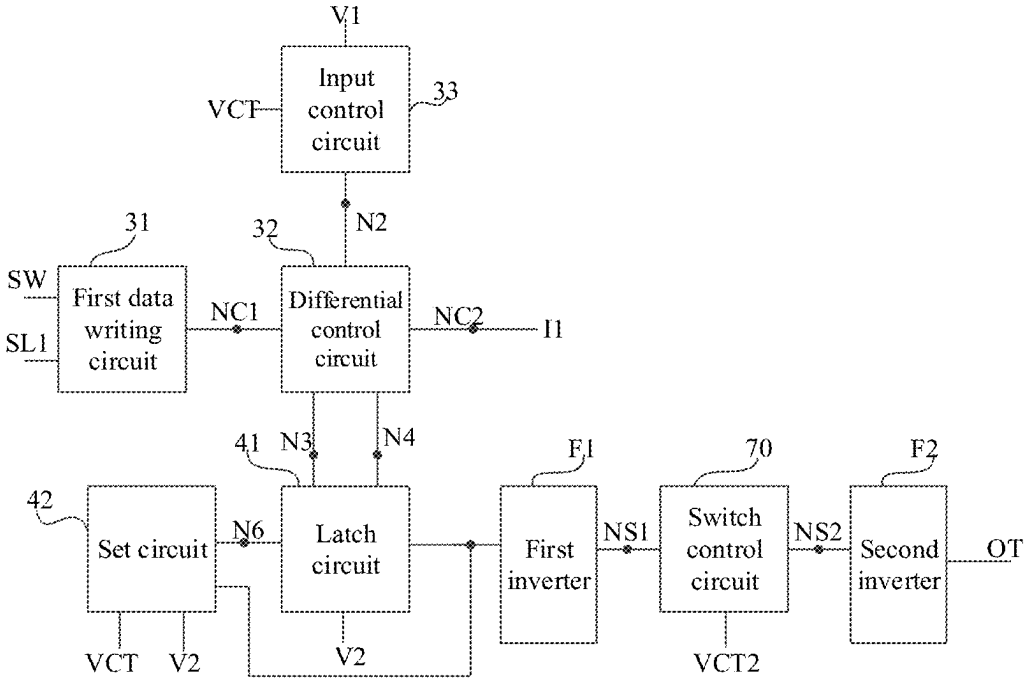


FIG. 15A

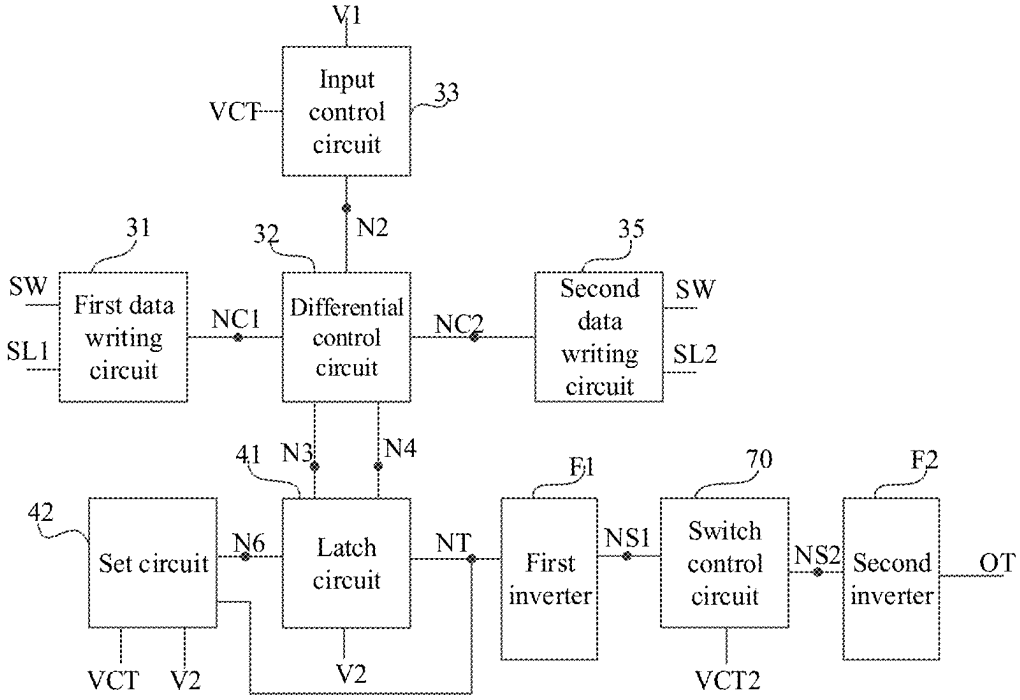


FIG. 15B

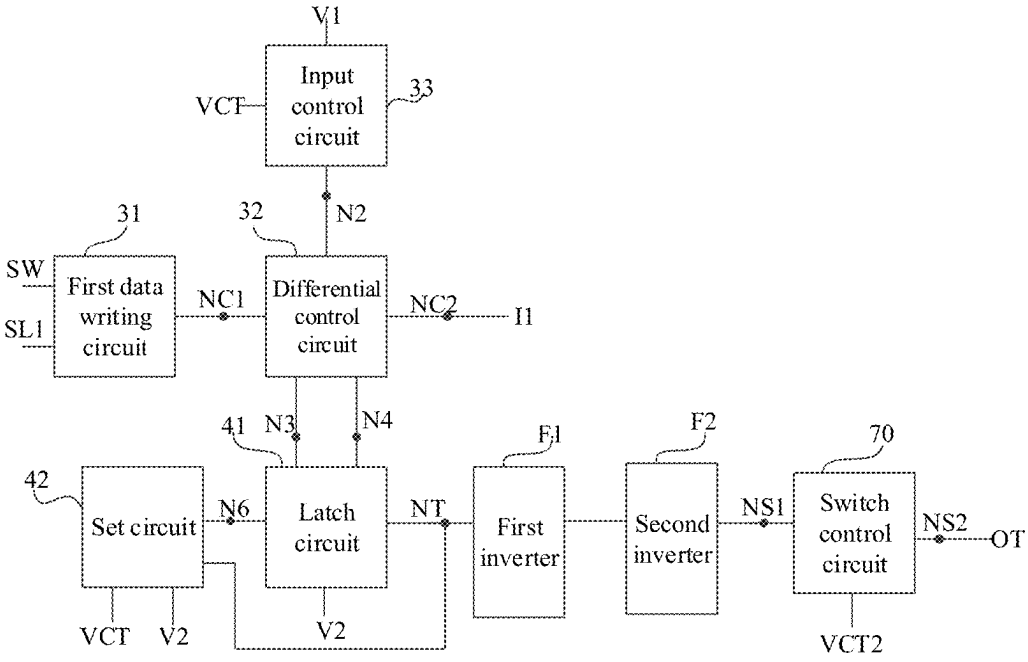


FIG. 16A

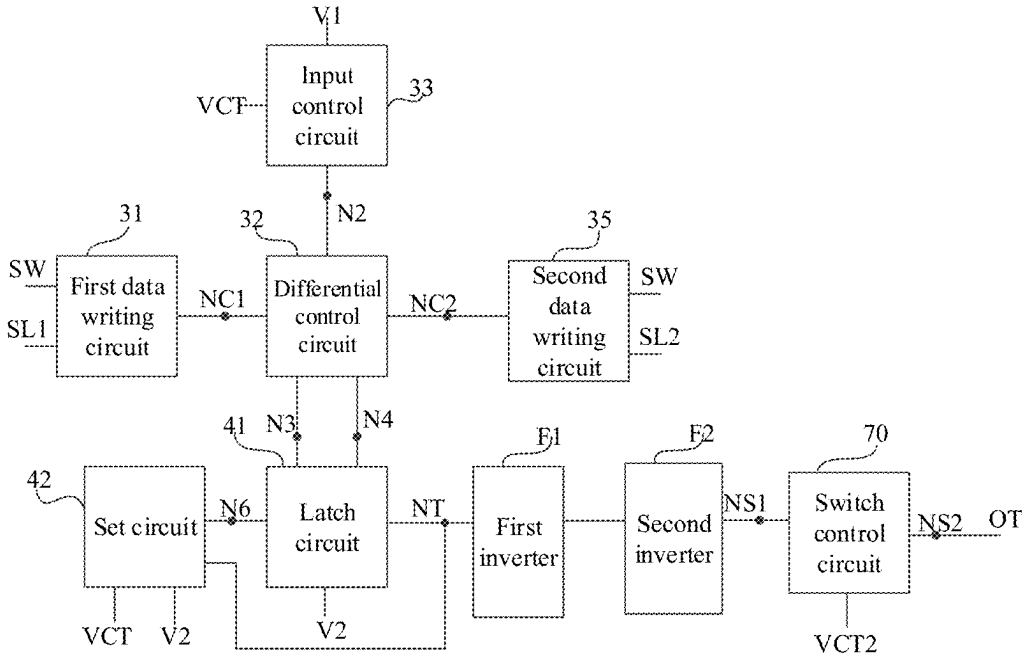


FIG. 16B

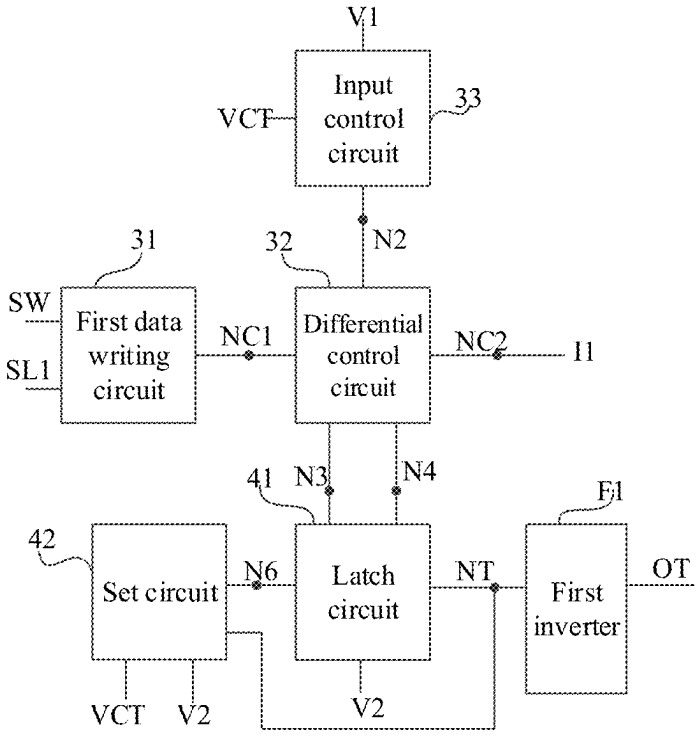


FIG. 17

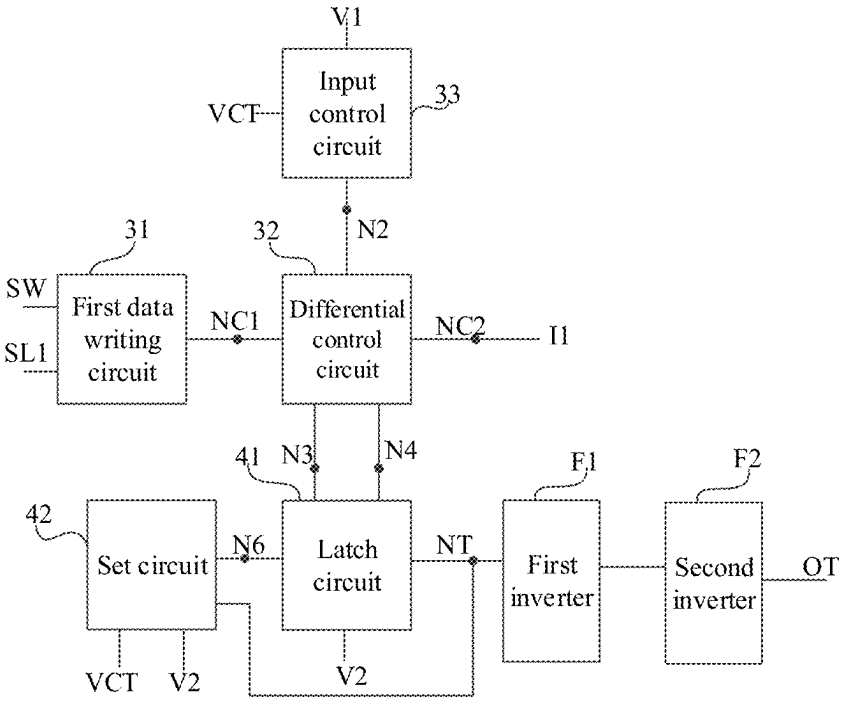

V1
Input control circuit
VCT
33
31
32
N2
SW
First data writing circuit
SL1
NC1
Differential control circuit
NC2
I1
41
N3
N4
F1
F2
42
Set circuit
N6
Latch circuit
NT
First inverter
Second inverter
OT
VCT
V2
V2

FIG. 18

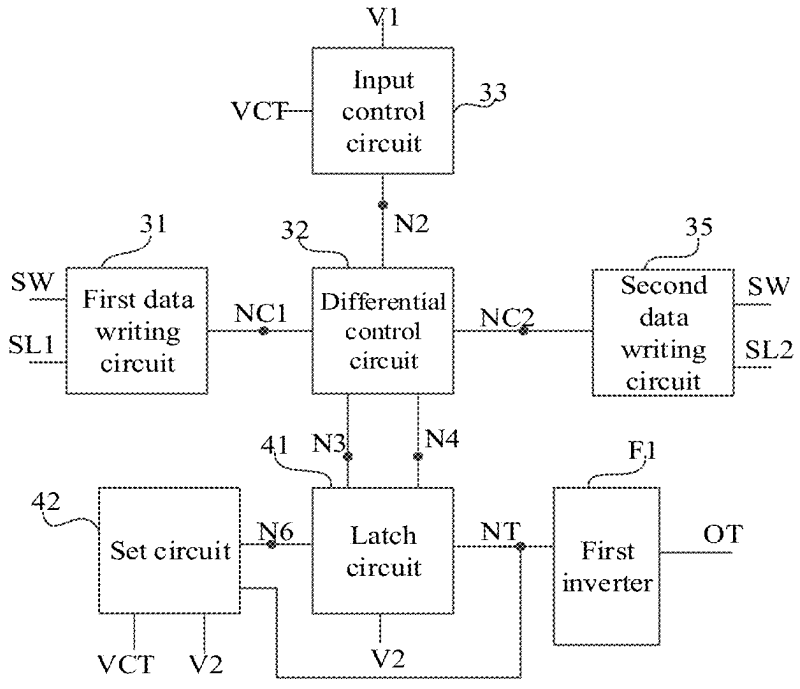

V1
Input control circuit
VCT
33
31
32
N2
35
SW
First data writing circuit
SL1
NC1
Differential control circuit
NC2
Second data writing circuit
SW
SL2
41
N3
N4
F1
42
Set circuit
N6
Latch circuit
NT
First inverter
OT
VCT
V2
V2

FIG. 19

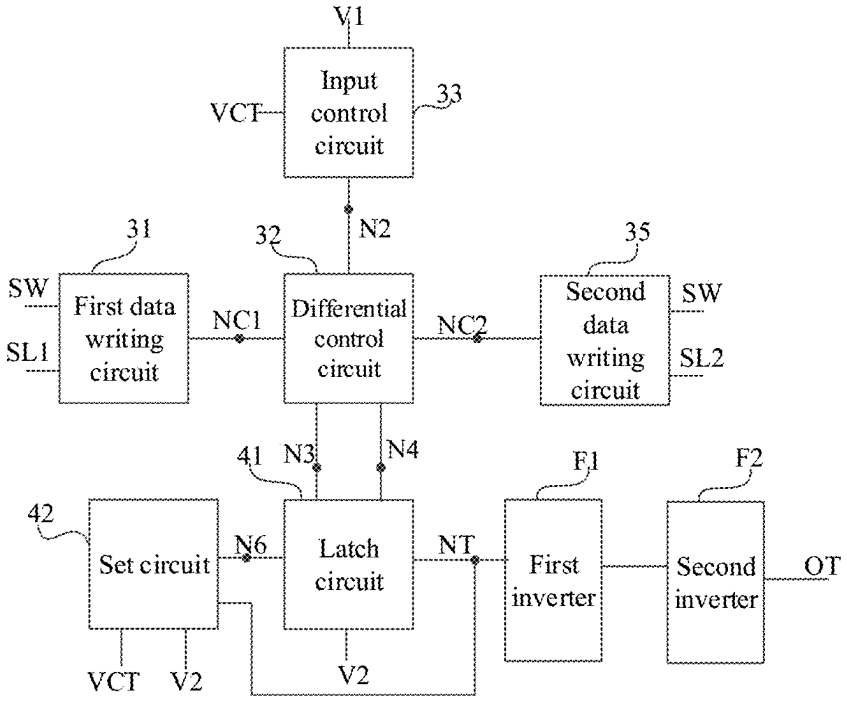


FIG. 20

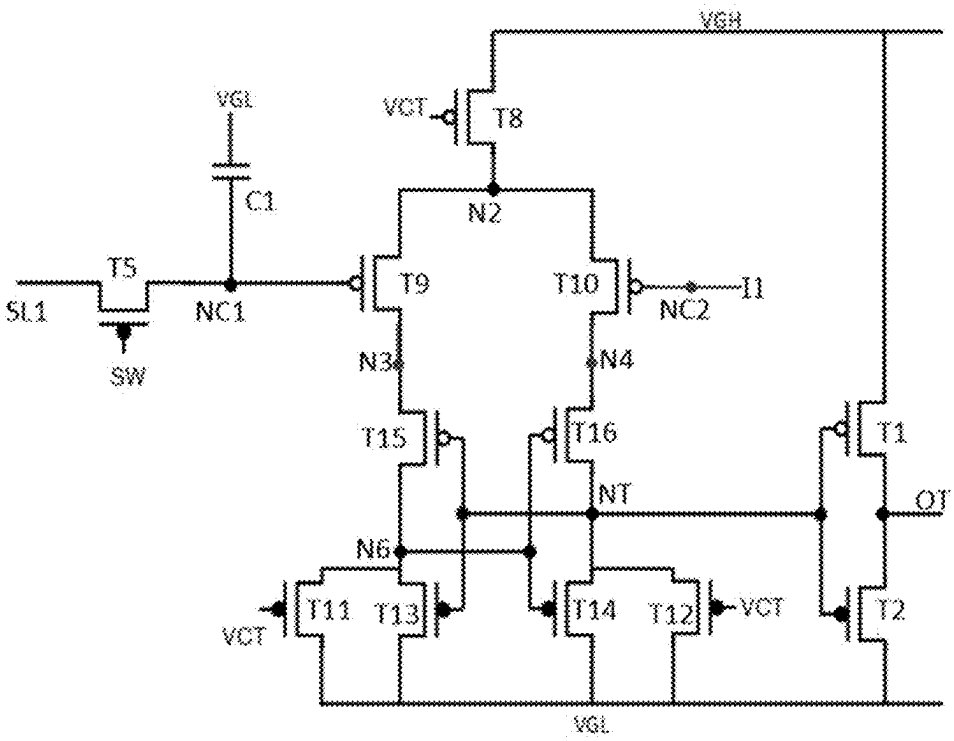


FIG. 21A

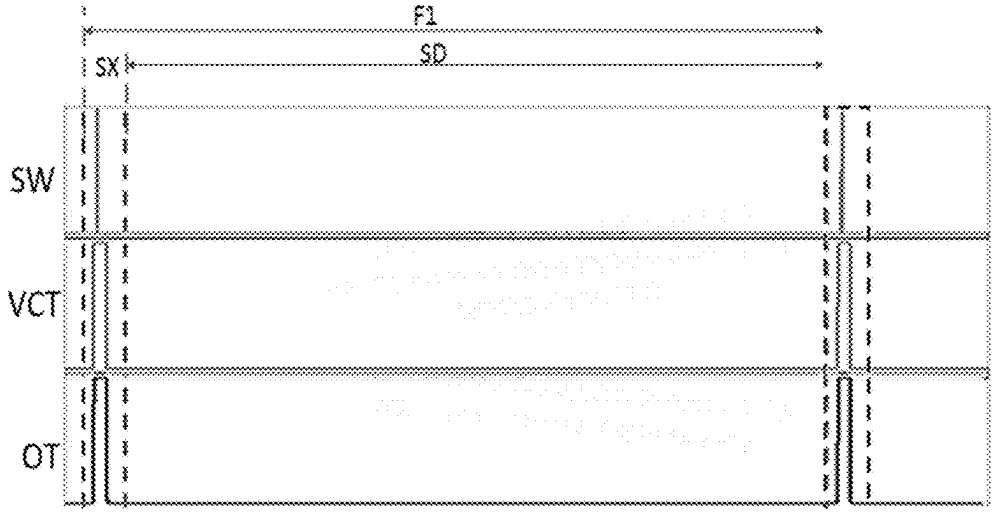


FIG. 21B

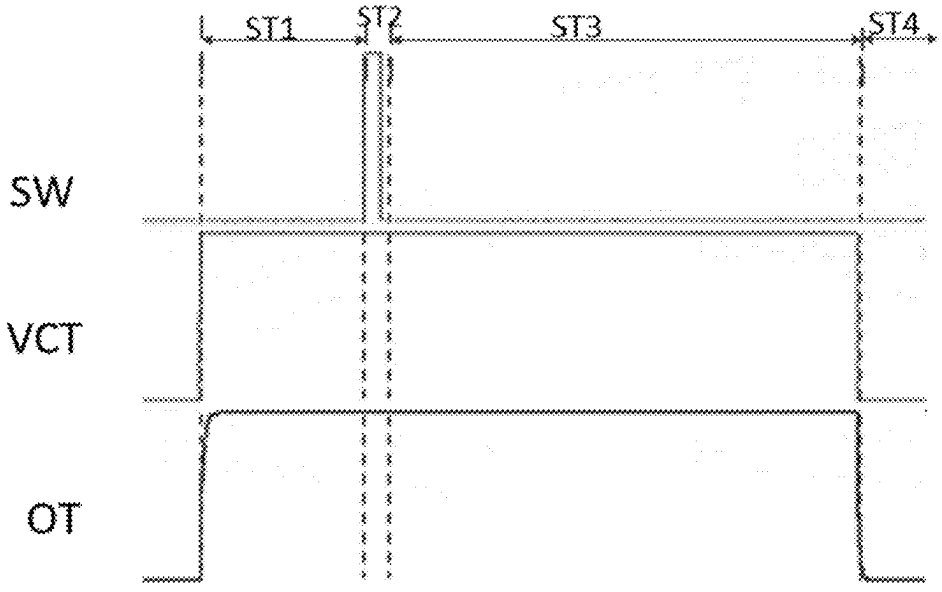


FIG. 21C

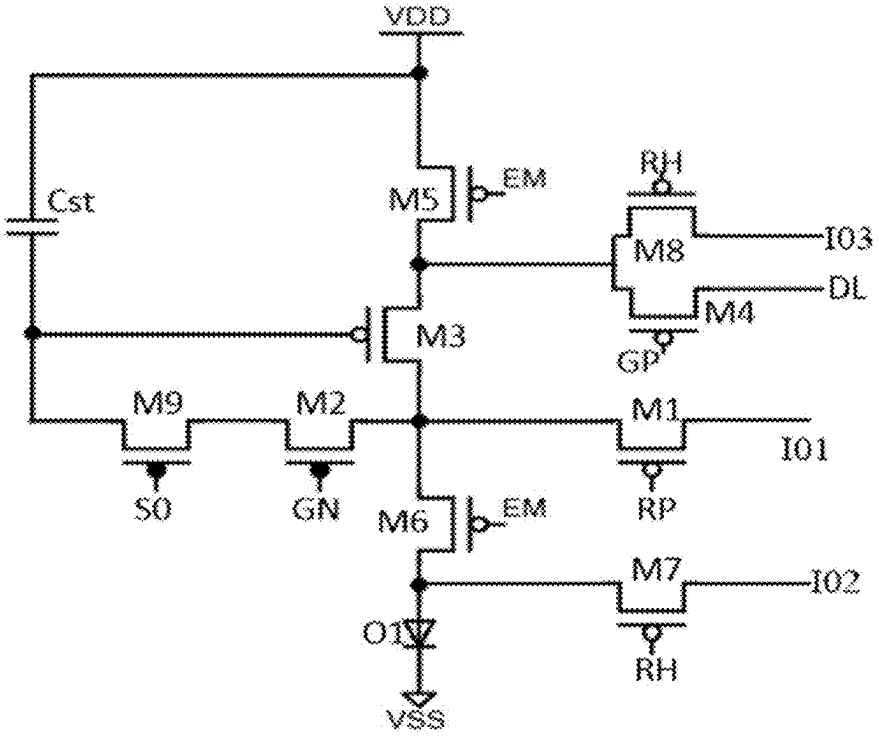


FIG. 21D

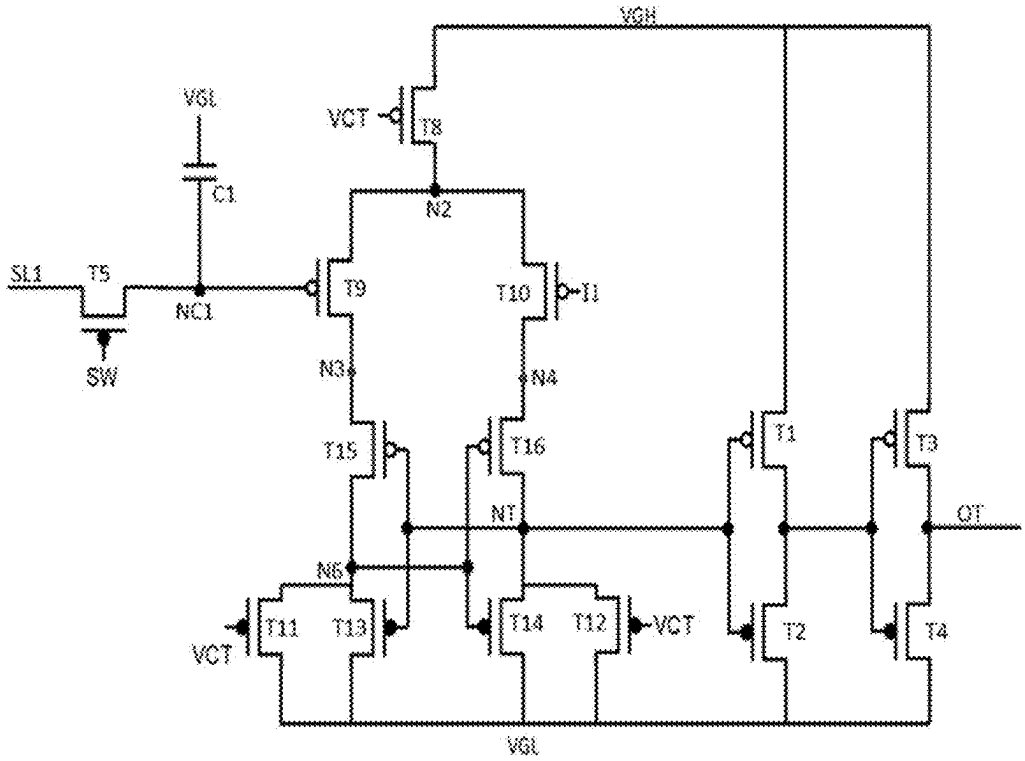


FIG. 22A

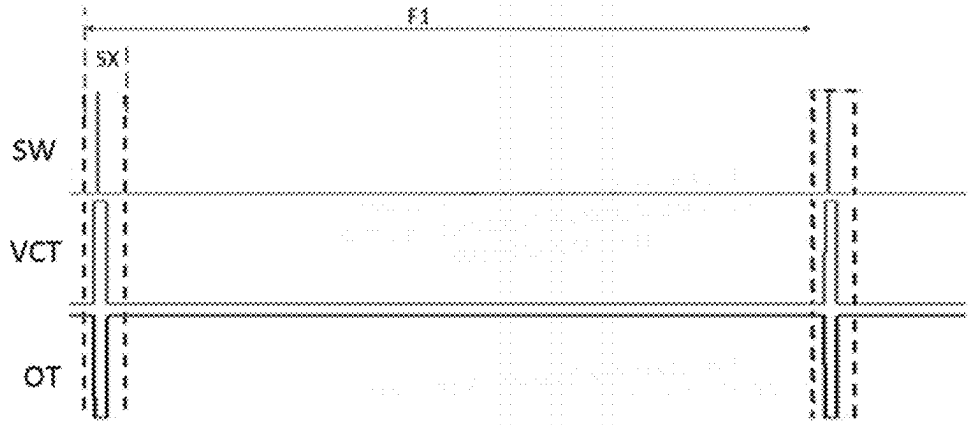


FIG. 22B

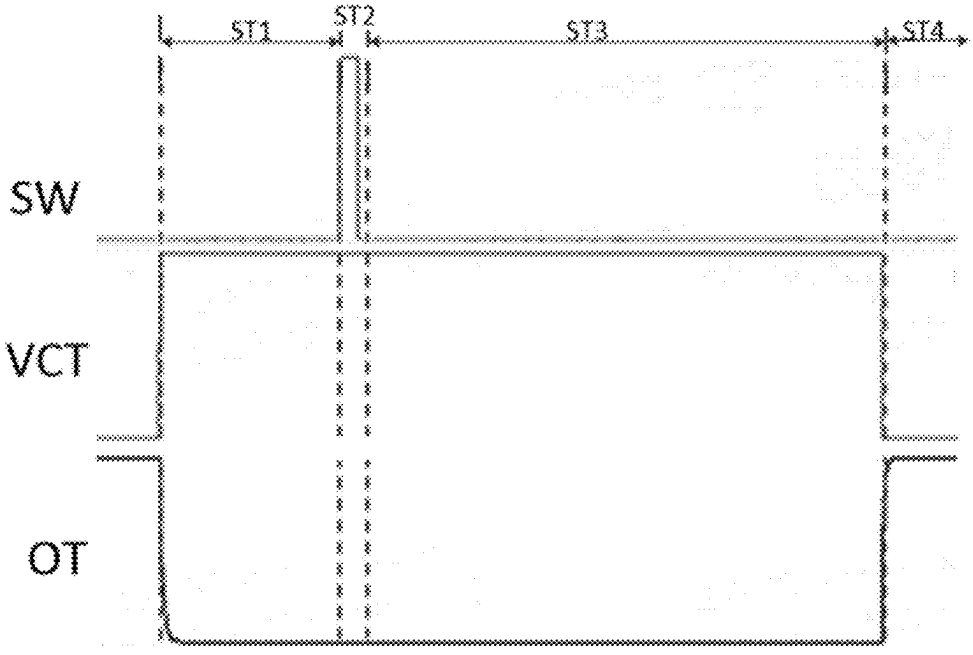


FIG. 22C

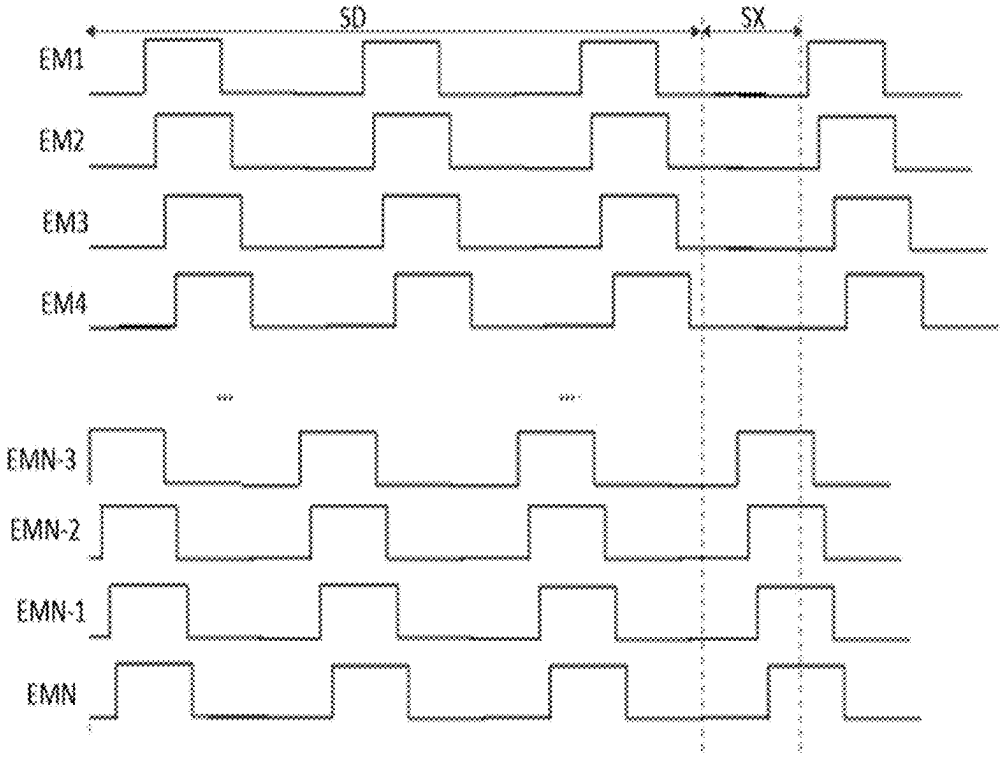


FIG. 22D

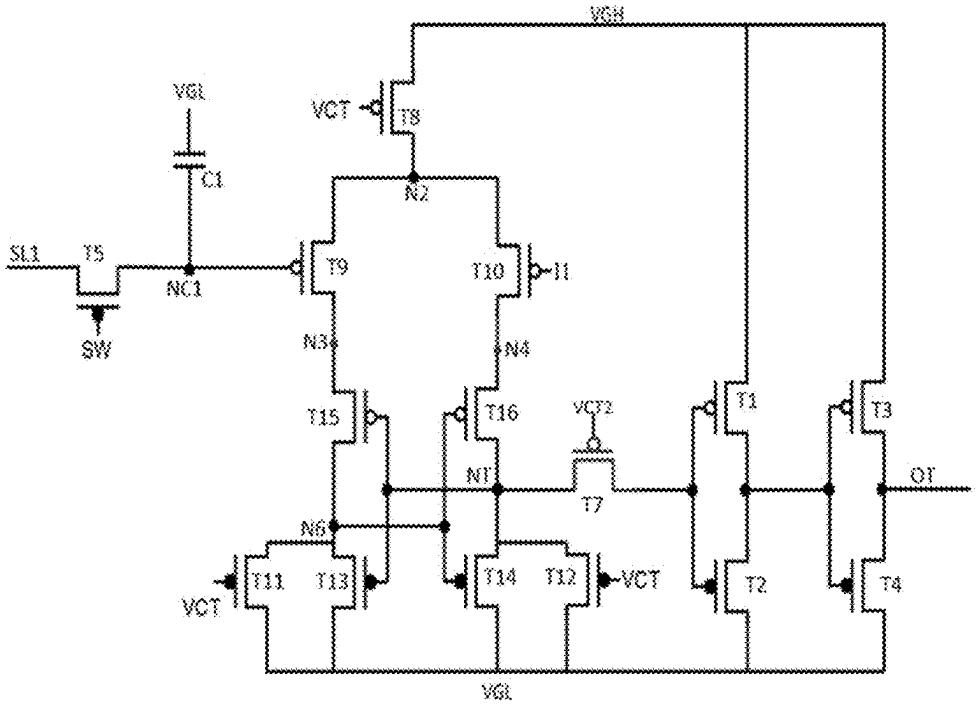


FIG. 23A

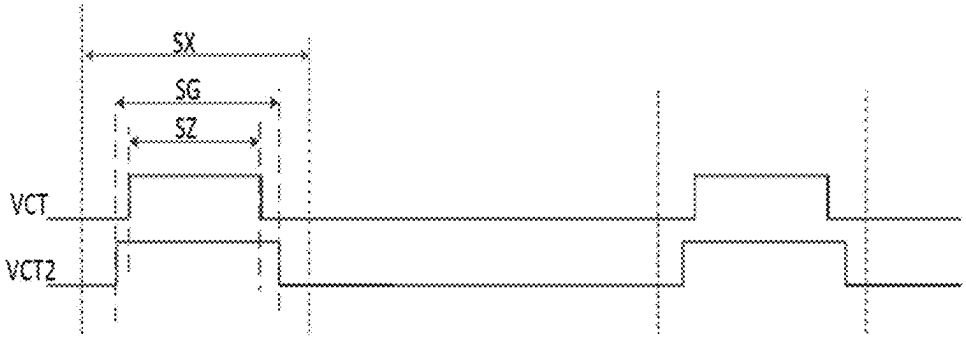


FIG. 23B

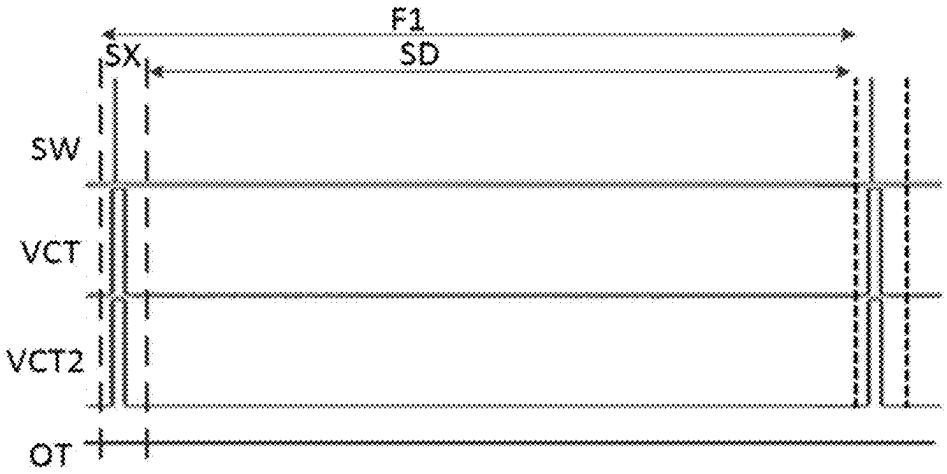


FIG. 23C

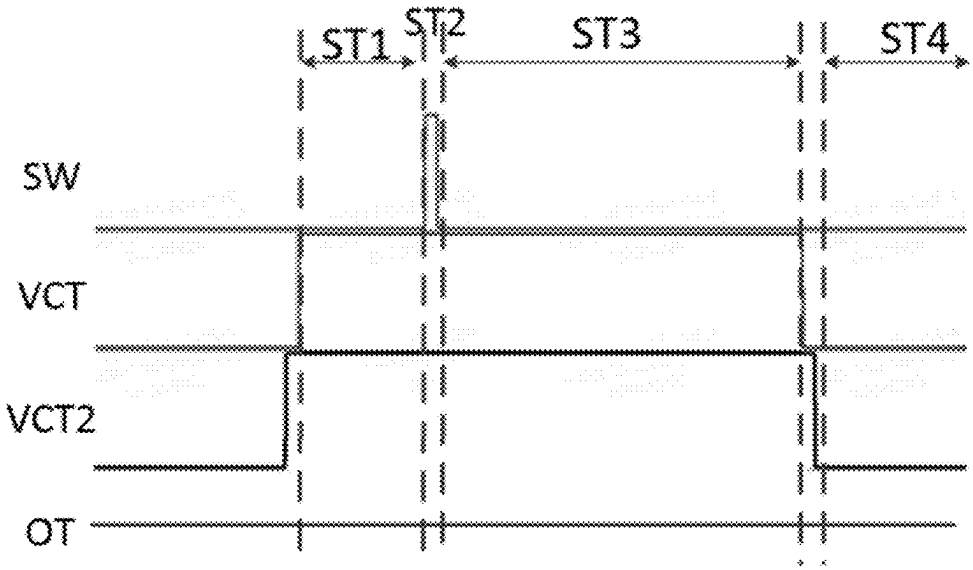
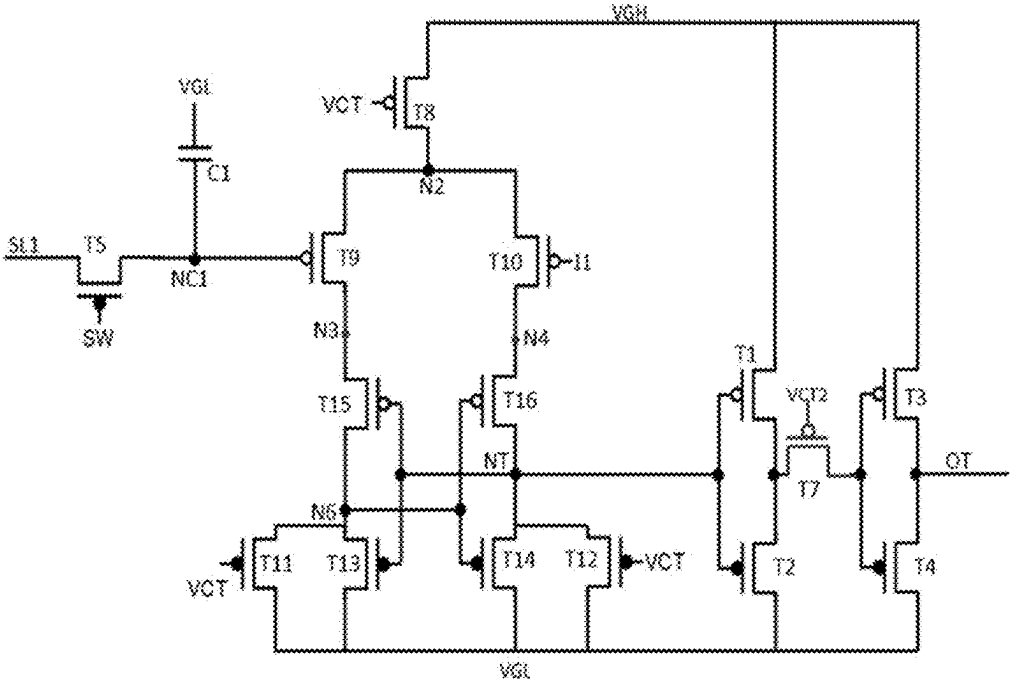


FIG. 23D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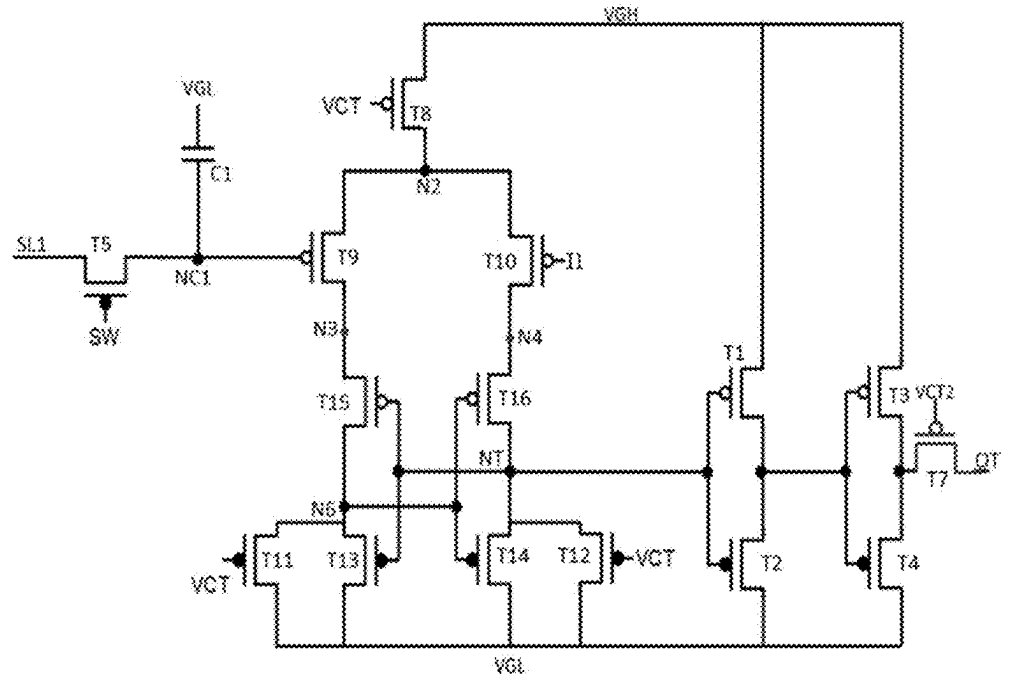
VGL
C1
VCT
T8
N2
SL1
T5
NC1
SW
T9
T10
I1
N3
N4
T15
T16
T1
VCT2
T3
NT
OT
T7
N6
T11
T13
T14
T12
VCT
T2
T4
VGL

FIG. 24


VGH
VGL
C1
VCT
T8
N2
SL1
T5
NC1
SW
T9
T10
I1
N3
N4
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T16
T1
T3
VCT2
NT
T7
OT
N6
T11
T13
T14
T12
VCT
T2
T4
VGL

FIG. 25

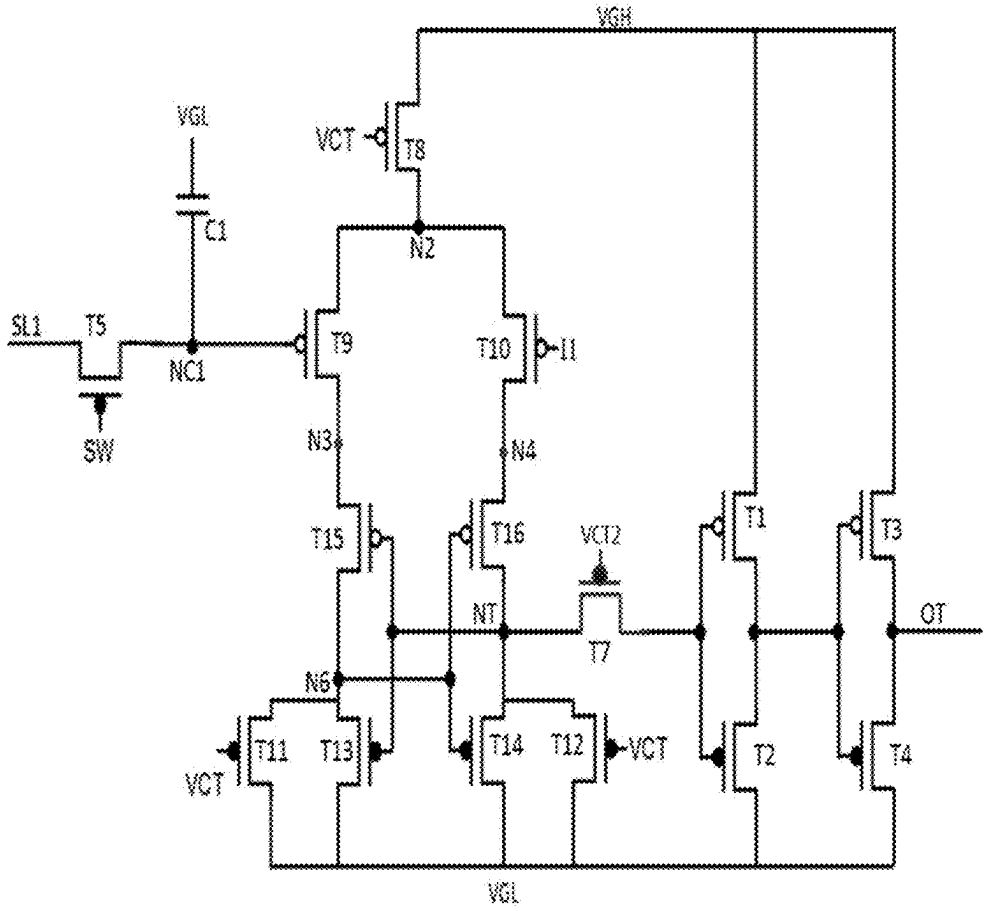


FIG. 26A

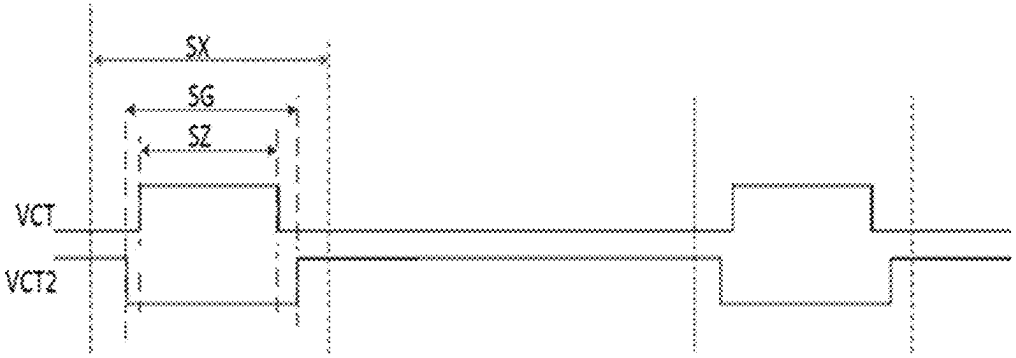
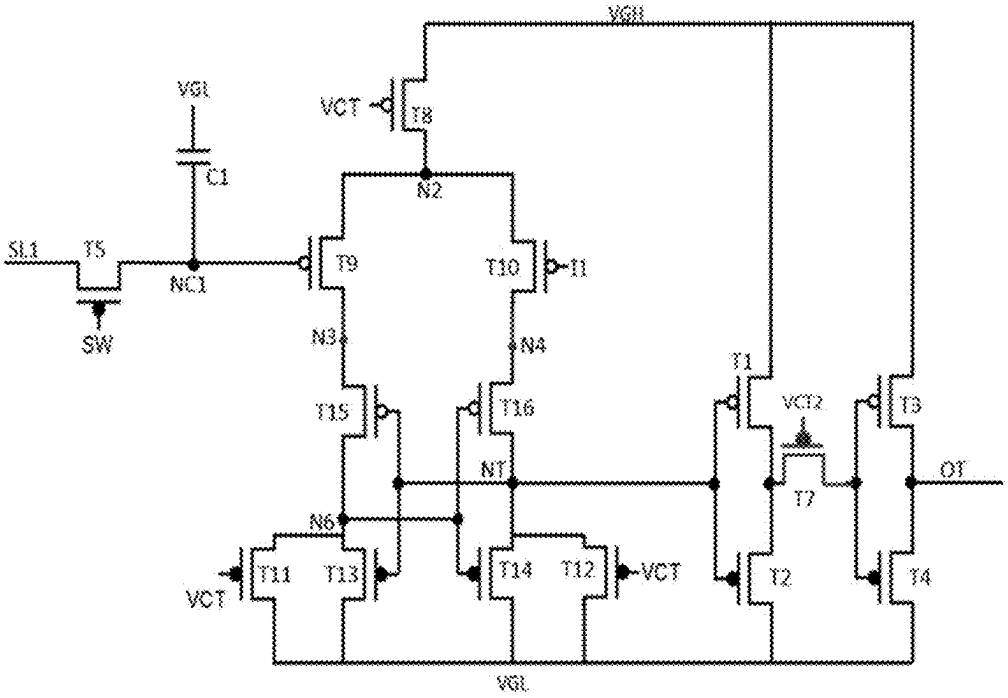


FIG. 26B


VGH
VGL
C1
VCT
T8
N2
SL1
T5
NC1
T9
T10
T11
SW
N3
N4
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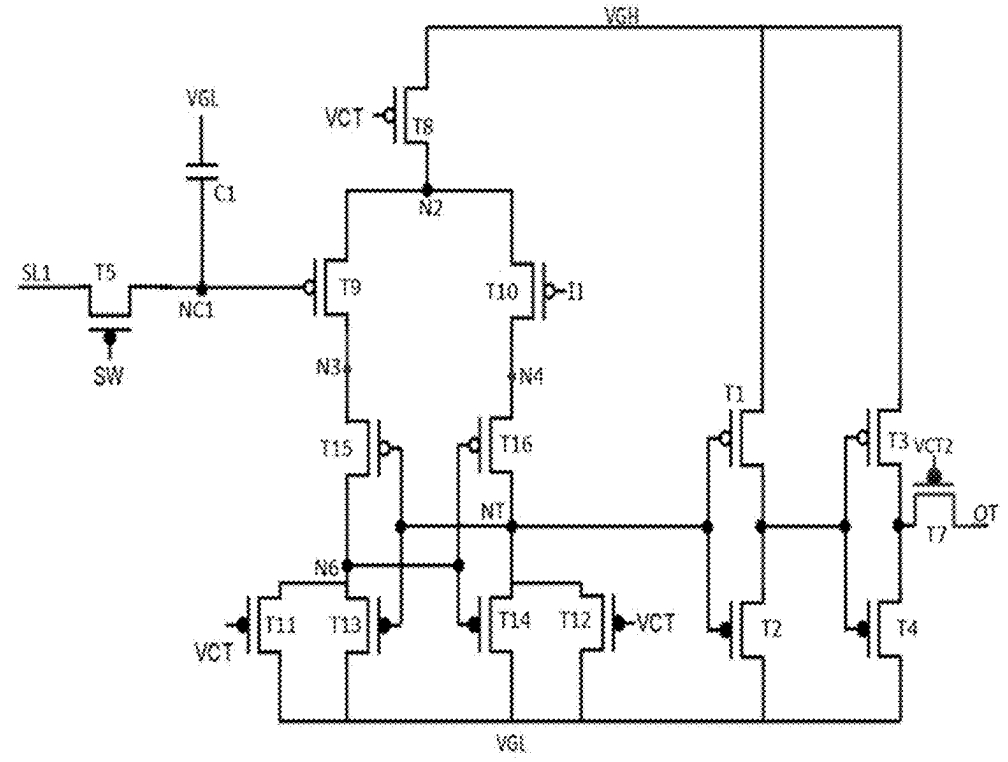
T16
T1
VCT2
T3
NT
OT
T7
N6
T11
T13
T14
T12
VCT
T2
T4
VGL

FIG. 27


VGH
VGL
C1
VCT
T8
N2
SL1
T5
NC1
T9
T10
T11
SW
N3
N4
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T15
T16
T3
VCT2
NT
OT
T7
N6
T11
T13
T14
T12
VCT
T2
T4
VGL

FIG. 28

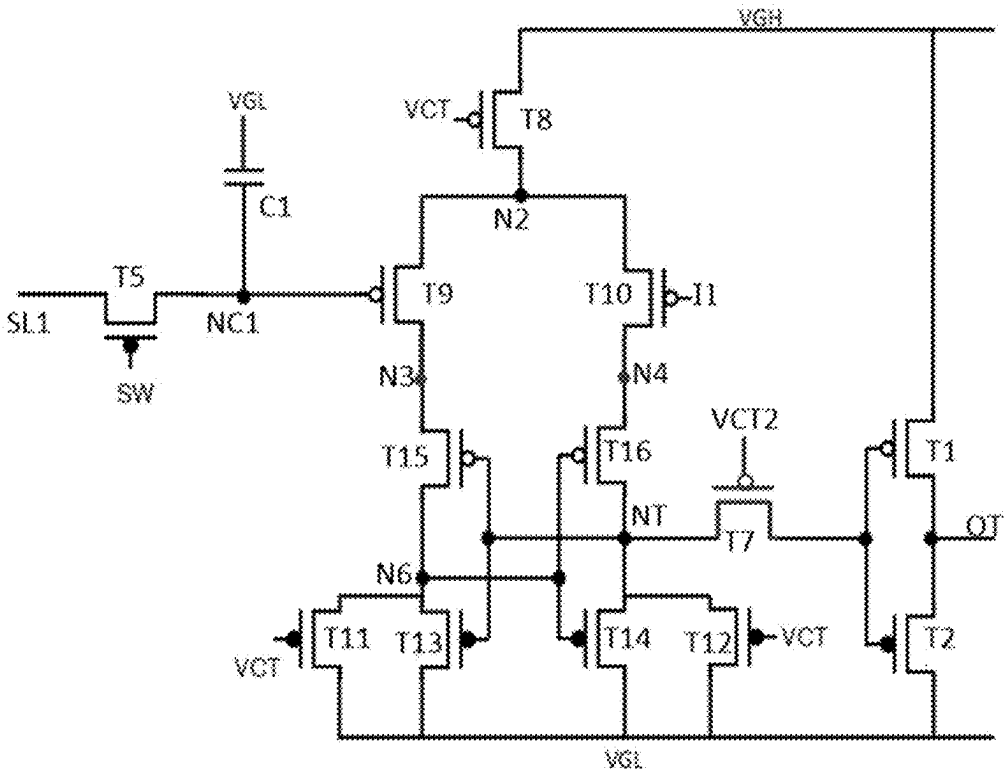


FIG. 29A

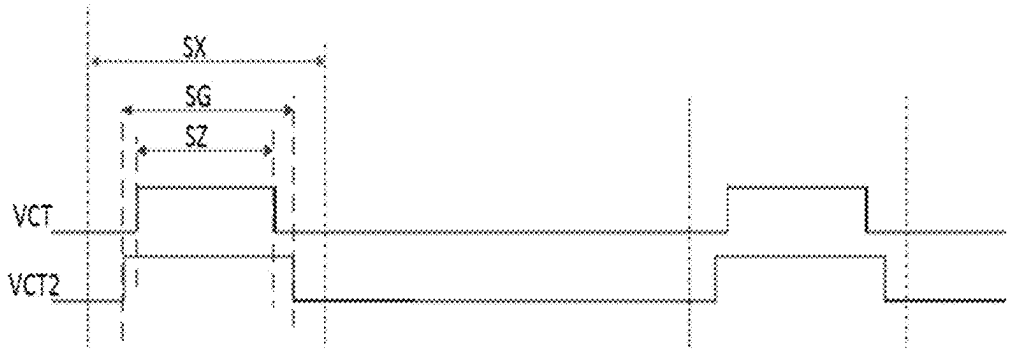


FIG. 29B

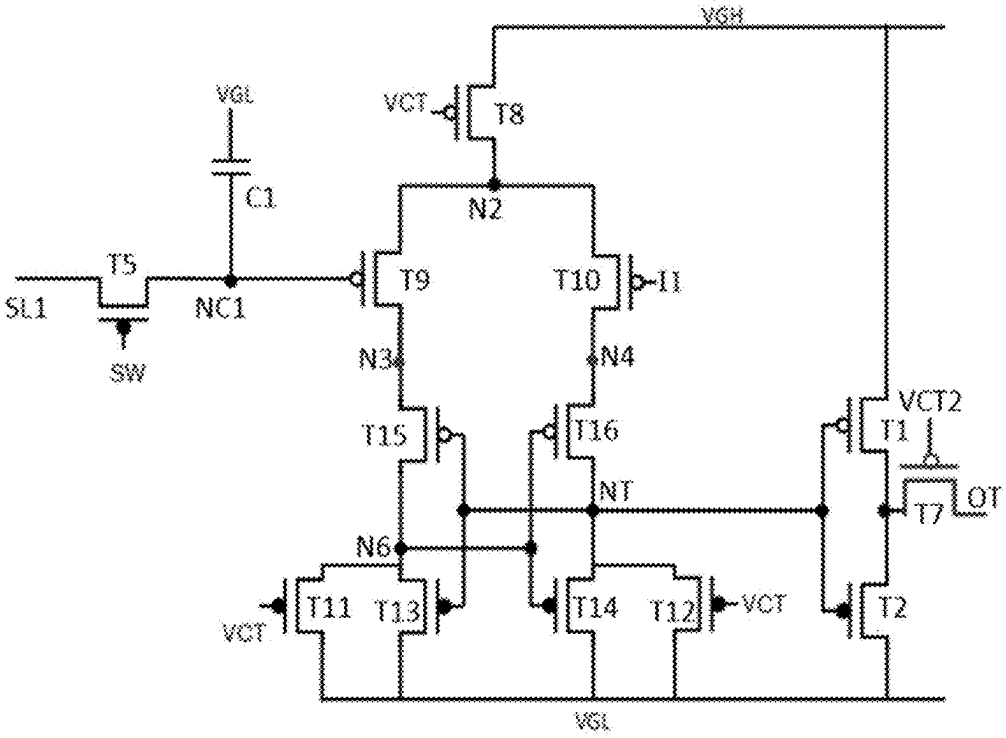


FIG. 30

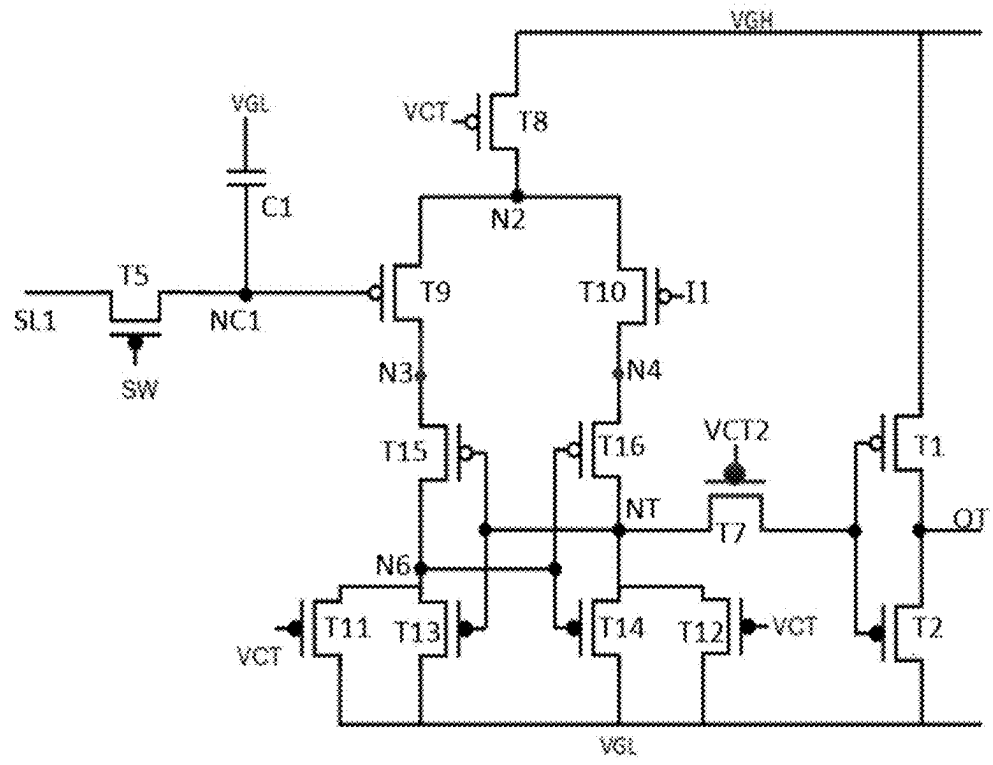


FIG. 31A

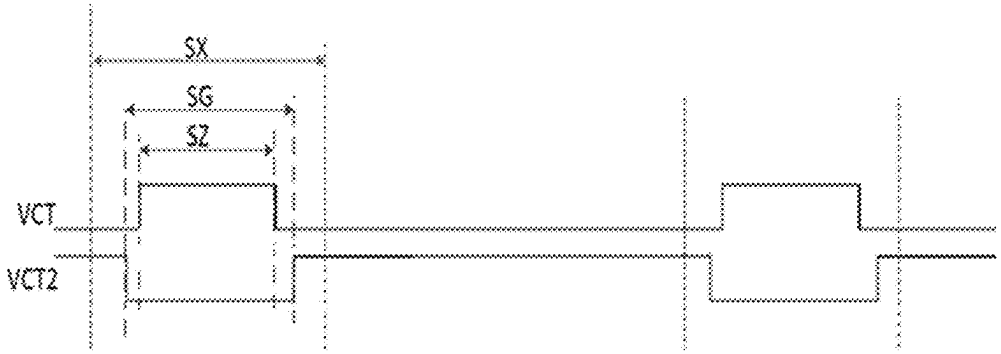


FIG. 31B

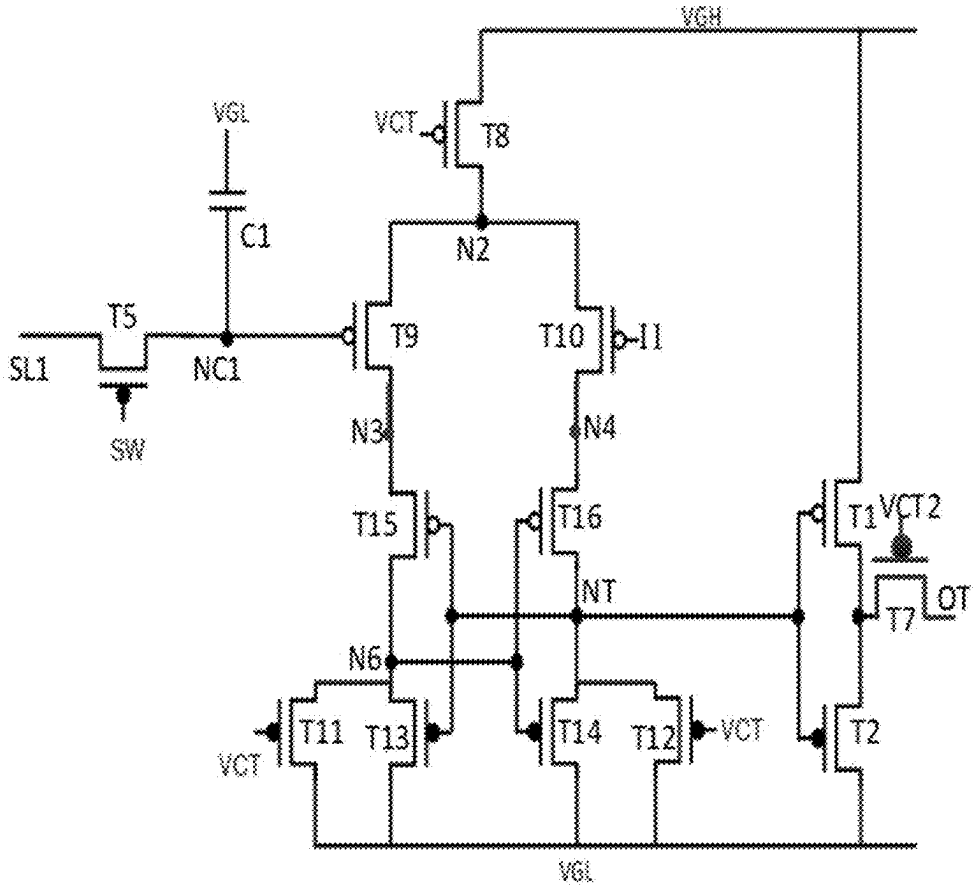
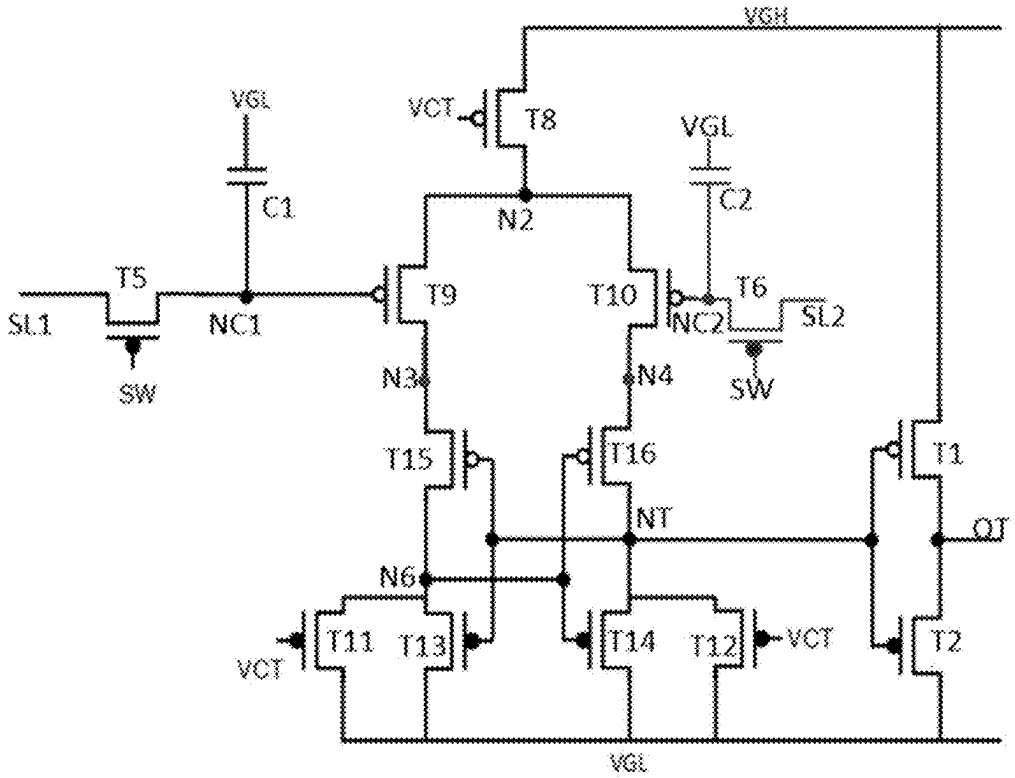


FIG. 32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VGL
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VGL
C2
N2
T5
SL1
NC1
T9
T10
T6
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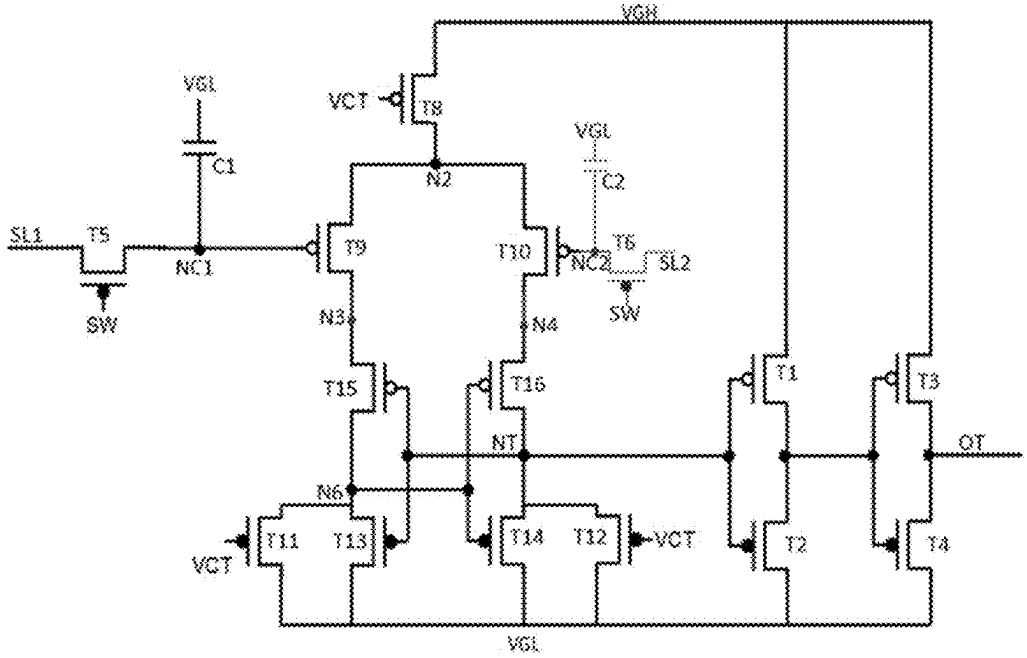
SL2
SW
SW
N3
N4
T15
T16
T1
NT
OT
N6
T11
T13
T14
T12
VCT
VCT
T2
VGL

FIG. 33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VCT
T8
VGL
C2
N2
SL1
T5
NC1
T9
T10
T6
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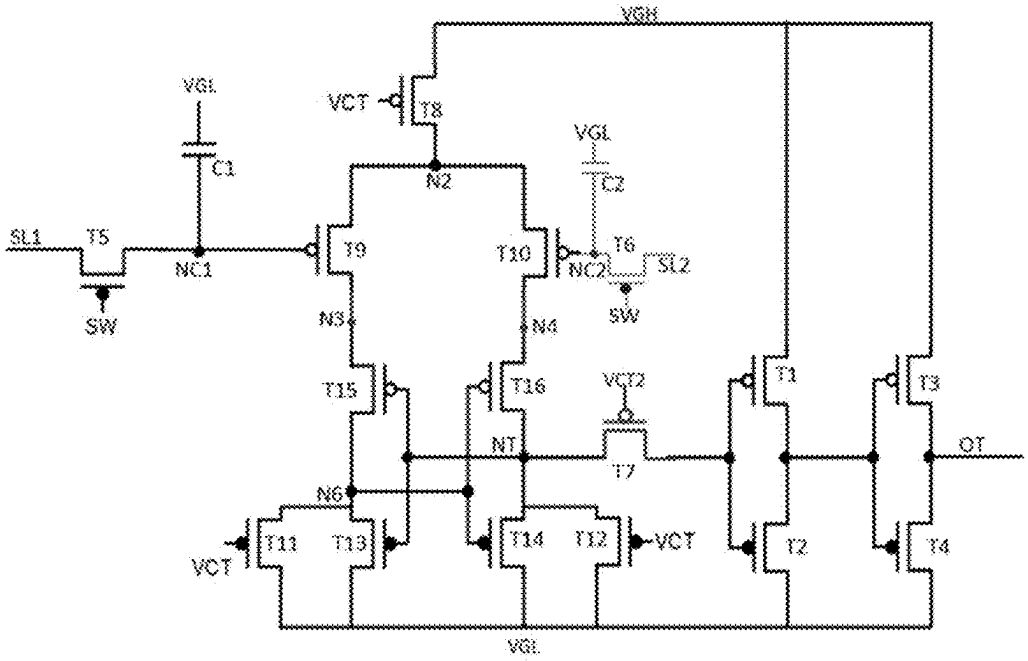
SL2
SW
SW
N3
N4
T15
T16
T1
T3
NT
OT
N6
T11
T13
T14
T12
VCT
VCT
T2
T4
VGL

FIG. 34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VCT
T8
N2
VGL
C2
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T5
NC1
T9
T10
NC2
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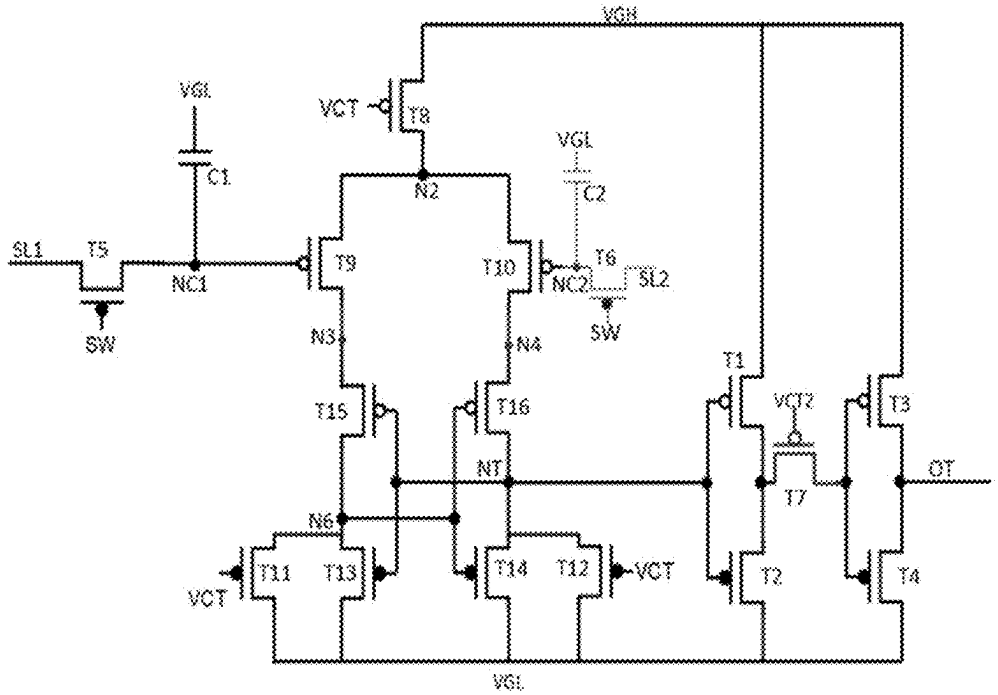
SL2
SW
SW
N3
N4
T15
T16
VCT2
T1
T3
NT
T7
OT
N6
T11
T13
T14
T12
VCT
VCT
T2
T4
VGL

FIG. 35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VGL
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T5
NC1
T9
T10
NC2
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SL2
SW
SW
N3
N4
T1
T15
T16
VCT2
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T7
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T11
T13
T14
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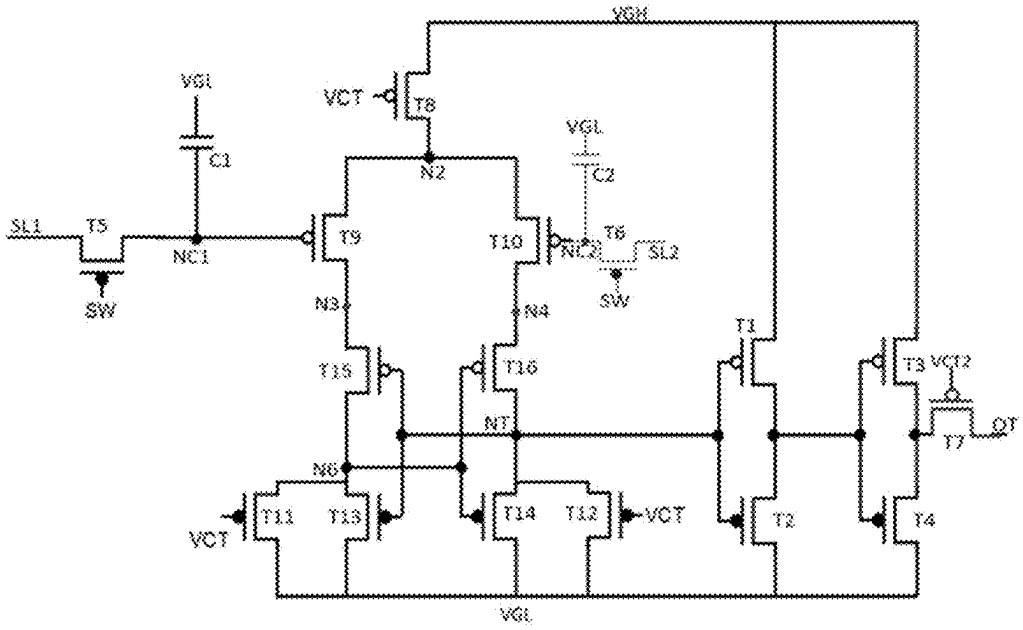
VCT
VCT
T2
T4
VGL

FIG. 36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N2
VGL
C2
SL1
T5
NC1
T9
T10
NC2
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N3
N4
T15
T16
T1
T3
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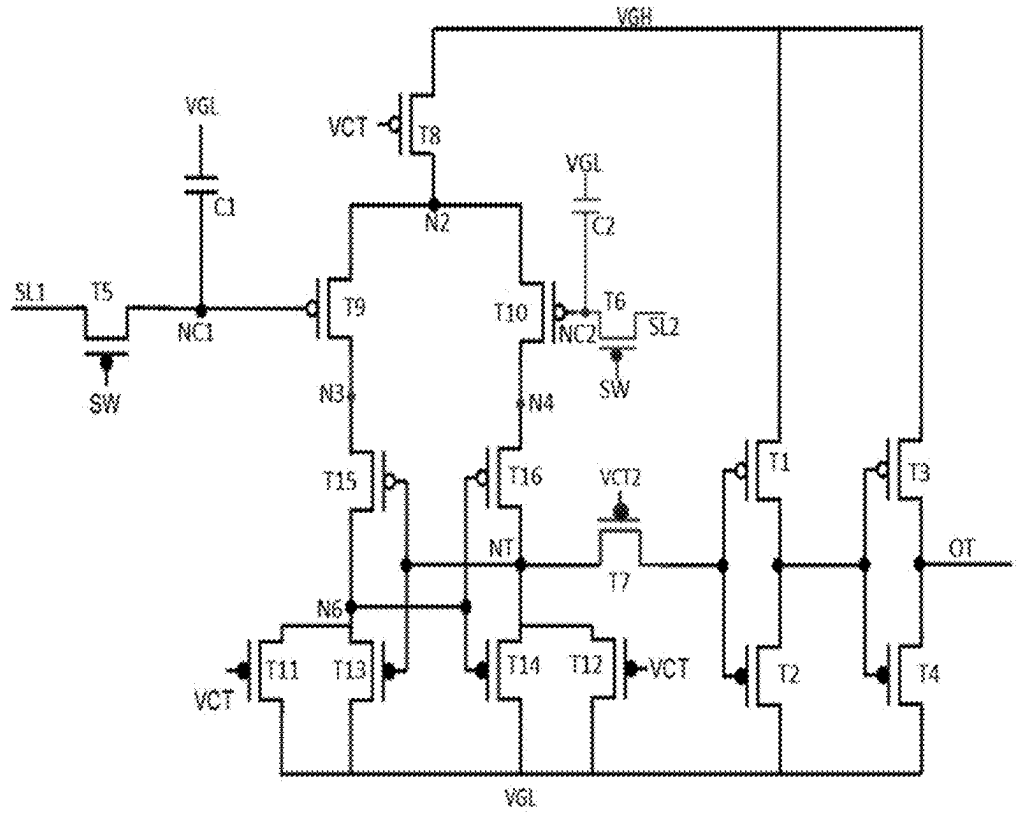
T7
OT
N6
T11
T13
T14
T12
VCT
VCT
T2
T4
VGL

FIG. 37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N2
VGL
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T5
NC1
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N4
T15
T16
VCT2
T1
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T7
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N6
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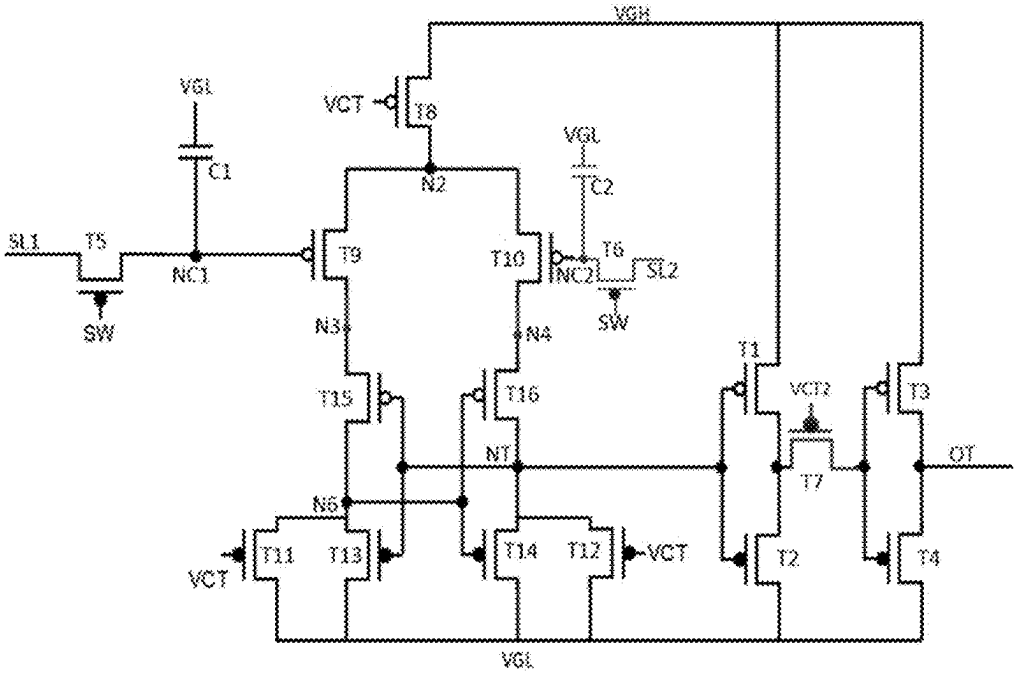
T13
T14
T12
VCT
VCT
T2
T4
VGL

FIG. 38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VCT
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VGL
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T5
NC1
T9
T10
NC2
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N4
T1
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T16
VCT2
T3
NT
OT
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N6
T11
T13
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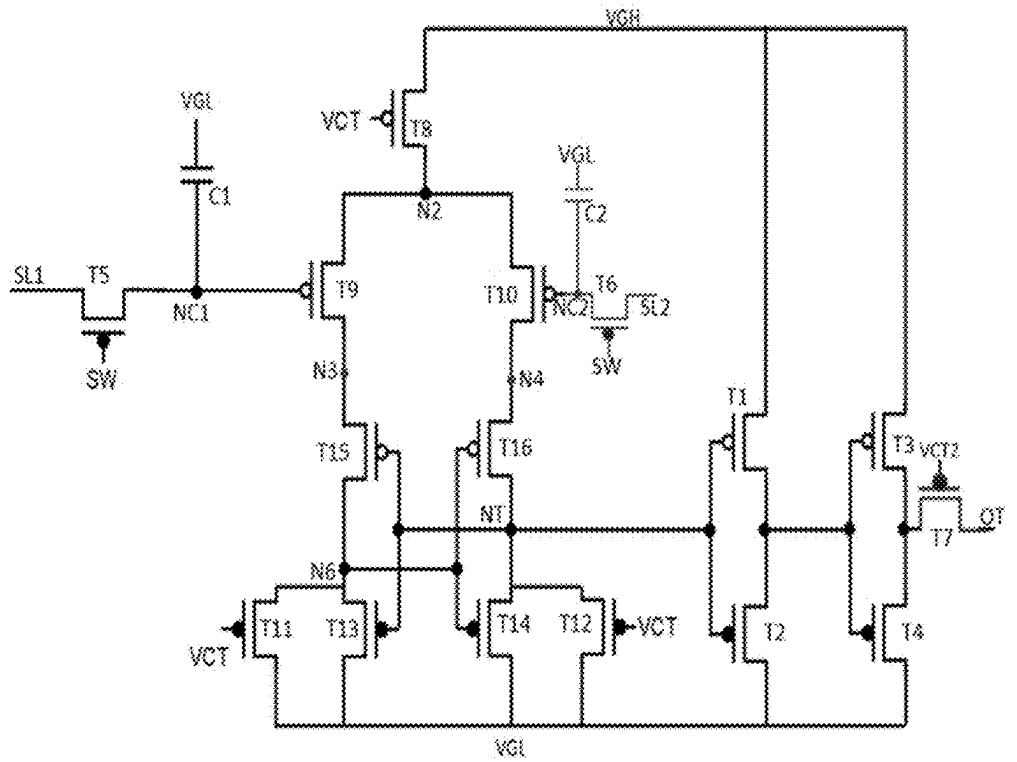
T12
VCT
VCT
T2
T4
VGL

FIG. 39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VCT
T8
VGL
C2
N2
SL1
T5
NC1
T9
T10
NC2
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SW
N3
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T1
T15
T16
T3
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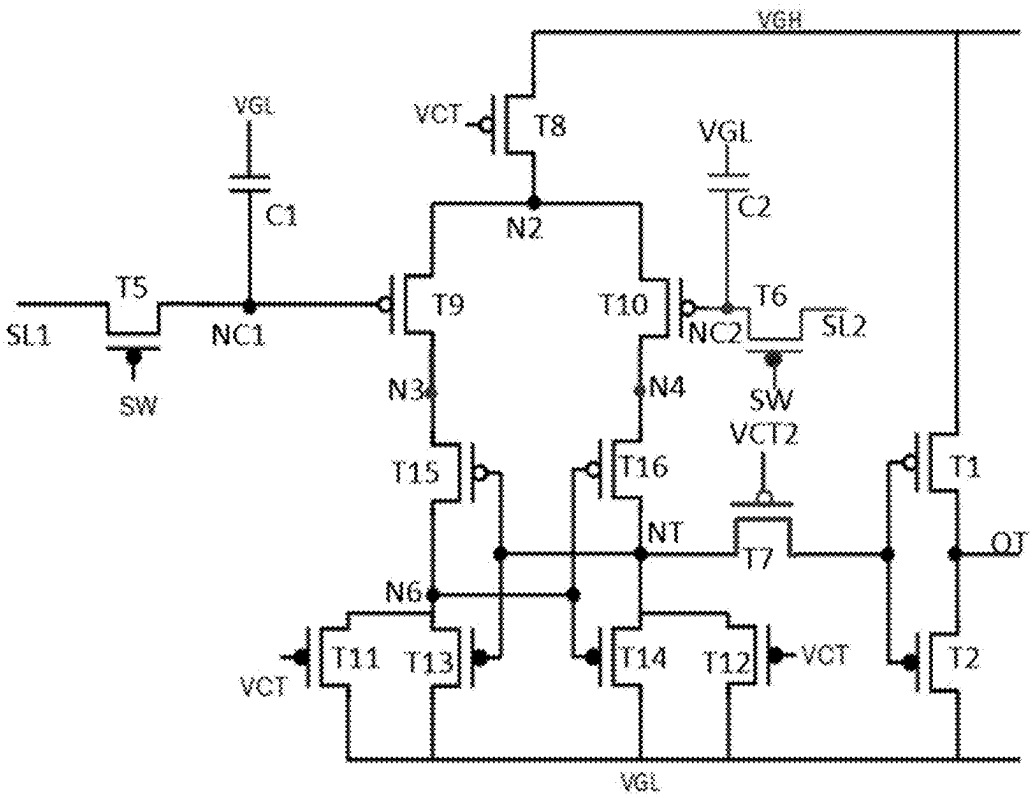
NT
OT
T7
N6
T11
T13
T14
T12
VCT
VCT
T2
T4
VGL

FIG. 40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N2
C2
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T9
T10
T6
SL1
NC1
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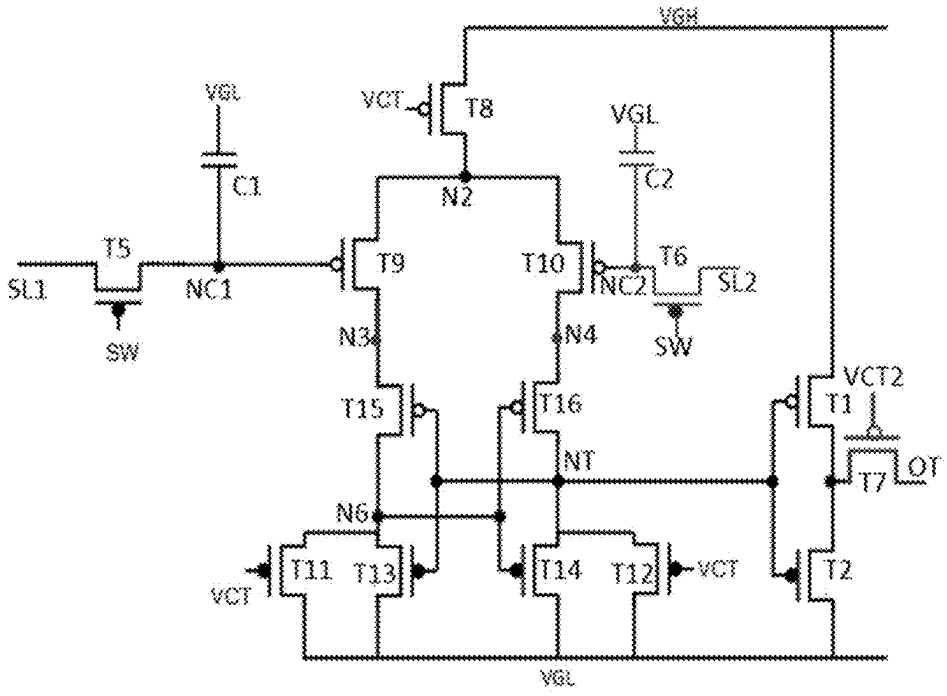
SW
N3
N4
SW
VCT2
T15
T16
T1
NT
T7
OT
N6
T11
T13
T14
T12
VCT
VCT
T2
VGL

FIG. 41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VGL
VCT
T8
VGL
C1
N2
C2
T5
T9
T10
T6
SL1
NC1
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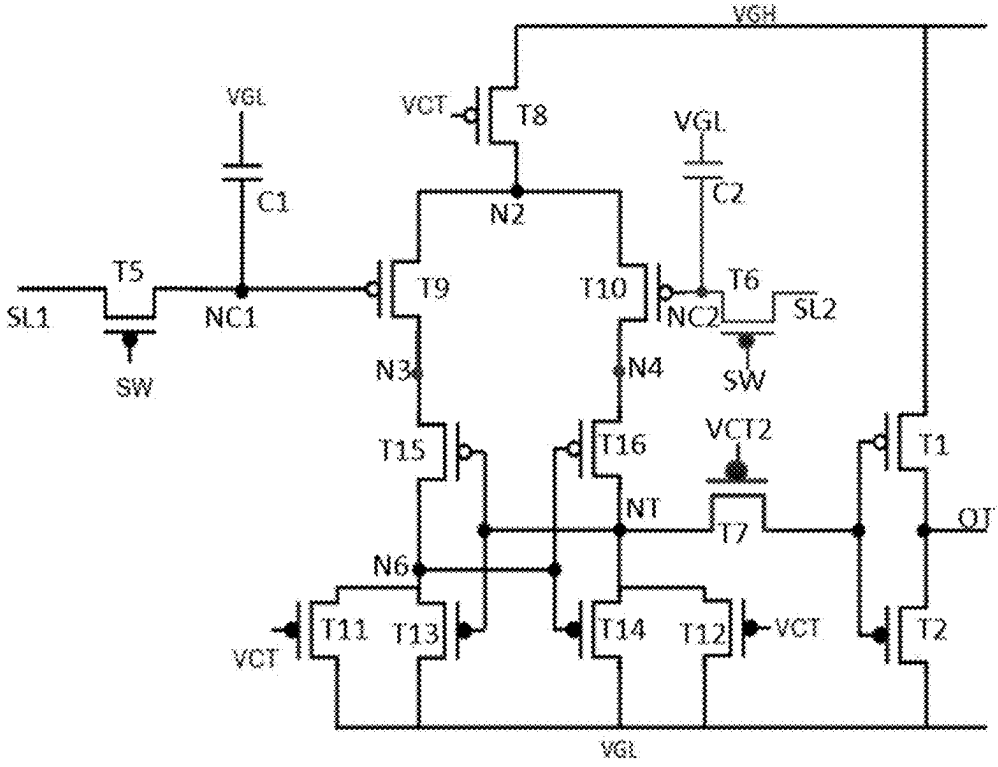
SL2
SW
N3
N4
SW
VCT2
T15
T16
T1
NT
T7
OT
N6
T11
T13
T14
T12
VCT
VCT
T2
VGL

FIG. 42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VCT
T8
VGL
C2
N2
T5
SL1
NC1
T9
T10
T6
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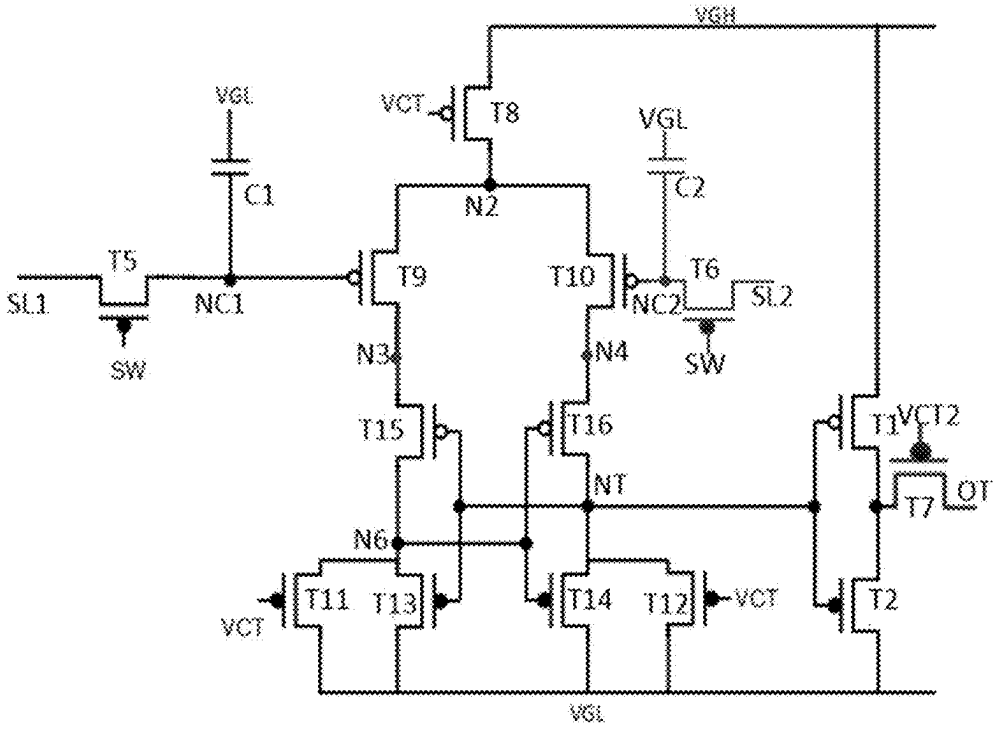
SL2
SW
N3
N4
SW
T15
T16
VCT2
T1
NT
T7
OT
N6
T11
T13
T14
T12
VCT
T2
VCT
VGL

FIG. 43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VGL
C1
VCT
T8
VGL
C2
N2
T5
SL1
NC1
T9
T10
T6
NC2
SL2
SW
N3
N4
SW
T15
T16
T1
VCT2
NT
T7
OT
N6
T11
T13
T14
T12
VCT
T2
VCT
VGL

FIG. 44

DRIVING CIRCUIT, DRIVING METHOD, AND DISPLAY DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application is the U.S. national phase of PCT Application No. PCT/CN2024/094704 filed on May 22, 2024, which claims a priority to PCT Application No. PCT/CN2023/084683 filed on Mar. 29, 2023, which is incorporated in its entirety by reference herein.

TECHNICAL FIELD

[0002] The present disclosure relates to the field of display technologies, and in particular to a driving circuit, a driving method and a display device.

BACKGROUND

[0003] In most cases, a conventional OLED (organic light emitting diode) pixel driving method includes that: reset, data writing and light emission phase are completed once in each frame, with the entire screen maintaining a consistent refresh rate. However, with advancements in time and technology, it has become possible to use different driving frequencies for the same display. In the low-frequency regions, during frame maintaining, some signals do not need to be reset repeatedly, nor do they require the writing of data voltage signals. Therefore, by controlling source control circuits of these signals and turning off certain TFTs (thin film transistor) in the circuit, power consumption can be reduced. The above technology is known as partial refresh. In the related technologies, output stability of the driving circuit that provides a driving signal is low.

SUMMARY

[0004] In an aspect, embodiments of the present disclosure provide a driving circuit, including an output circuit and an inverting circuit;

[0005] the output circuit is electrically connected to an output control terminal, a switch control terminal, a data line and a driving output terminal, and is configured to provide a driving output signal via the driving output terminal based on a data voltage provided by the data line under control of a switch control signal provided by the switch control terminal and an output control signal provided by the output control terminal;

[0006] the inverting circuit includes N stages of inverters, N is a positive integer;

[0007] an input terminal of a first inverter is electrically connected to the driving output terminal, and an output terminal of an N-th inverter is electrically connected to a driving signal output terminal;

[0008] in a case that N is greater than 1, an output terminal of an m-th inverter is electrically connected to an input terminal of an (m+1)-th inverter, and m is a positive integer less than N; and

[0009] the inverter is configured to invert a signal received by the input terminal of the inverter to obtain an inverted signal, and output the inverted signal via the output terminal of the inverter.

[0010] Optionally, the output circuit includes a first data writing circuit, a differential control circuit, an input control circuit and an output control circuit;

[0011] the first data writing circuit is electrically connected to the switch control terminal, a first data line and a first differential control node, and is configured to write a first data voltage provided by the first data line into the first differential control node and maintain a potential of the first differential control node under control of the switch control signal provided by the switch control terminal;

[0012] the differential control circuit is electrically connected to the first differential control node, a second differential control node, an input node, a first output node, and a second output node, and is configured to control a potential of the first output node and a potential of the second output node based on a potential of the input node under control of the potential of the first differential control node and a potential of the second differential control node;

[0013] the input control circuit is electrically connected to the output control terminal, the input node and a first voltage terminal, and is configured to control connection or disconnection between the input node and the first voltage terminal under control of the output control signal provided by the output control terminal; and

[0014] the output control circuit is electrically connected to the output control terminal, the first output node, the second output node and the driving output terminal, and is configured to generate the driving output signal and provide the driving output signal via the driving output terminal based on the potential of the first output node and the potential of the second output node under control of the output control signal.

[0015] Optionally, the output control circuit includes a latch circuit and a set circuit;

[0016] the set circuit is electrically connected to the output control terminal, an intermediate node, the driving output terminal and a second voltage terminal, and is configured to control connection or disconnection between the intermediate node and the second voltage terminal and control connection or disconnection between the driving output terminal and the second voltage terminal under control of the output control signal; and

[0017] the latch circuit is electrically connected to the first output node, the second output node, the intermediate node, the driving output terminal and the second voltage terminal, and is configured to control a potential of the driving output terminal based on the potential of the first output node and the potential of the second output node under control of a potential of the intermediate node.

[0018] Optionally, the output circuit further includes a second data writing circuit;

[0019] the second data writing circuit is electrically connected to the switch control terminal, a second data line and the second differential control node, and is configured to write a second data voltage provided by the second data line into the second differential control node and maintain the potential of the second differential control node under control of the switch control signal provided by the switch control terminal.

[0020] Optionally, the driving circuit in at least one embodiment of the present disclosure further includes a switch control circuit;

[0021] the switch control circuit is electrically connected to an on-off control terminal, a first output control node and a second output control node, and is configured to control connection or disconnection between the first output control node and the second output control node under control of an on-off control signal provided by the on-off control terminal;

[0022] the first output control node is electrically connected to the driving output terminal, and the second output control node is electrically connected to the input terminal of the first inverter; or,

[0023] the first output control node is electrically connected to the output terminal of the N-th inverter, and the second output control node is electrically connected to the driving signal output terminal; or,

[0024] N is greater than 1, the first output control node is electrically connected to the output terminal of the m-th inverter, and the second output control node is electrically connected to the input terminal of the (m+1)-th inverter.

[0025] Optionally, the latch circuit is configured to control connection or disconnection between the second output node and the driving output terminal and connection or disconnection between the driving output terminal and the second voltage terminal under control of the potential of the intermediate node, and to control connection or disconnection between the first output node and the intermediate node and connection or disconnection between the intermediate node and the second voltage terminal under control of the potential of the driving output terminal.

[0026] Optionally, a frame time includes a blanking period, the blanking period includes an off phase, and the off phase includes a setting period;

[0027] the set circuit is configured to control connection between the intermediate node and the second voltage terminal and control connection between the driving output terminal and the second voltage terminal under control of the output control signal during the setting period; and

[0028] the switch control circuit is configured to control disconnection between the first output control node and the second output control node under control of the on-off control signal during the off phase.

[0029] Optionally, N is equal to 1, the inverting circuit includes the first inverter, and the first inverter includes a first transistor and a second transistor

[0030] a gate electrode of the first transistor is electrically connected to the input terminal of the first inverter, a first electrode of the first transistor is electrically connected to a first voltage terminal, and a second electrode of the first transistor and a first electrode of the second transistor are both electrically connected to the driving signal output terminal;

[0031] a gate electrode of the second transistor is electrically connected to the input terminal of the first inverter, and a second electrode of the second transistor is electrically connected to a second voltage terminal; and

[0032] the first transistor is a p-type transistor, and the second transistor is an n-type transistor.

[0033] Optionally, N is equal to 2, the inverting circuit includes the first inverter and a second inverter, the first inverter includes a first transistor and a second transistor, and the second inverter includes a third transistor and a fourth transistor;

[0034] a gate electrode of the first transistor is electrically connected to the input terminal of the first inverter, a first electrode of the first transistor is electrically connected to a first voltage terminal, and a second electrode of the first transistor and a first electrode of the second transistor are both electrically connected to an input terminal of the second inverter;

[0035] a gate electrode of the second transistor is electrically connected to the input terminal of the first inverter, and a second electrode of the second transistor is electrically connected to a second voltage terminal;

[0036] a gate electrode of the third transistor and a gate electrode of the fourth transistor are both electrically connected to the input terminal of the second inverter, a first electrode of the third transistor is electrically connected to the first voltage terminal, and a second electrode of the third transistor and a first electrode of the fourth transistor are both electrically connected to the driving signal output terminal;

[0037] a second electrode of the fourth transistor is electrically connected to the second voltage terminal; and

[0038] the first transistor is a p-type transistor, the second transistor is an n-type transistor; the third transistor is a p-type transistor, and the fourth transistor is an n-type transistor.

[0039] Optionally, the first data writing circuit includes a fifth transistor and a first capacitor;

[0040] a gate electrode of the fifth transistor is electrically connected to the switch control terminal, a first electrode of the fifth transistor is electrically connected to the first data line, and a second electrode of the fifth transistor is electrically connected to the first differential control node; and

[0041] a first terminal of the first capacitor is electrically connected to the first differential control node, and a second terminal of the first capacitor is electrically connected to a second voltage terminal.

[0042] Optionally, the second data writing circuit includes a sixth transistor and a second capacitor, a gate electrode of the sixth transistor is electrically connected to the switch control terminal, a first electrode of the sixth transistor is electrically connected to the second data line, and a second electrode of the sixth transistor is electrically connected to the second differential control node; and

[0043] a first terminal of the second capacitor is electrically connected to the second differential control node, and a second terminal of the second capacitor is electrically connected to the second voltage terminal.

[0044] Optionally, the switch control circuit includes a seventh transistor;

[0045] a gate electrode of the seventh transistor is electrically connected to the on-off control terminal, a first electrode of the seventh transistor is electrically connected to the first output control node, and a second electrode of the seventh transistor is electrically connected to the second output control node.

[0046] Optionally, the input control circuit includes an eighth transistor, and the differential control circuit includes a ninth transistor and a tenth transistor;

[0047] a gate electrode of the eighth transistor is electrically connected to the output control terminal, a first electrode of the eighth transistor is electrically connected to the first voltage terminal, and a second electrode of the eighth transistor is electrically connected to the input node;

[0048] a gate electrode of the ninth transistor is electrically connected to the first differential control node, a first electrode of the ninth transistor is electrically connected to the input node, and a second electrode of the ninth transistor is electrically connected to the first output node; and

[0049] a gate electrode of the tenth transistor is electrically connected to the second differential control node, a first electrode of the tenth transistor is electrically connected to the input node, and a second electrode of the tenth transistor is electrically connected to the second output node.

[0050] Optionally, the set circuit includes an eleventh transistor and a twelfth transistor;

[0051] a gate electrode of the eleventh transistor is electrically connected to the output control terminal, a first electrode of the eleventh transistor is electrically connected to the intermediate node, and a second electrode of the eleventh transistor is electrically connected to the second voltage terminal; and

[0052] a gate electrode of the twelfth transistor is electrically connected to the output control terminal, a first electrode of the twelfth transistor is electrically connected to the driving output terminal, and a second electrode of the twelfth transistor is electrically connected to the second voltage terminal.

[0053] Optionally, the eighth transistor is a p-type transistor, and the eleventh transistor and the twelfth transistor are n-type transistors; or, the eighth transistor is an n-type transistor, and the eleventh transistor and the twelfth transistor are p-type transistors.

[0054] Optionally, the latch circuit includes a thirteenth transistor, a fourteenth transistor, a fifteenth transistor, and a sixteenth transistor;

[0055] a gate electrode of the thirteenth transistor is electrically connected to the driving output terminal, a first electrode of the thirteenth transistor is electrically connected to the intermediate node, and a second electrode of the thirteenth transistor is electrically connected to the second voltage terminal;

[0056] a gate electrode of the fourteenth transistor is electrically connected to the intermediate node, a first electrode of the fourteenth transistor is electrically connected to the driving output terminal, and a second electrode of the fourteenth transistor is electrically connected to the second voltage terminal;

[0057] a gate electrode of the fifteenth transistor is electrically connected to the driving output terminal, a first electrode of the fifteenth transistor is electrically connected to the first output node, and a second electrode of the fifteenth transistor is electrically connected to the intermediate node; and

[0058] a gate electrode of the sixteenth transistor is electrically connected to the intermediate node, a first electrode of the sixteenth transistor is electrically connected to the second output node, and a second electrode of the sixteenth transistor is electrically connected to the driving output terminal.

[0059] Optionally, the thirteenth transistor and the fourteenth transistor are n-type transistors, and the fifteenth transistor and the sixteenth transistor are p-type transistors.

[0060] In a second aspect, embodiments of the present disclosure provide a driving method, applied to the above driving circuit, and the driving method includes:

[0061] providing, by the output circuit, the driving output signal via the driving output terminal based on the data voltage under control of the switch control signal and the output control signal; and

[0062] inverting, by the inverter included in the inverting circuit, the signal received by the input terminal of the inverter, to obtain the inverted signal, and outputting the inverted signal via the output terminal of the inverter.

[0063] Optionally, the output circuit includes a first data writing circuit, a differential control circuit, an input control circuit and an output control circuit, the output control circuit includes a latch circuit and a set circuit, a frame time includes a blanking period, the blanking period includes a setting period and an output phase, the setting period includes a reset phase, a data writing phase and a potential maintaining phase, and the driving method includes:

[0064] in the reset phase, controlling, by the set circuit, connection between an intermediate node and a second voltage terminal and connection between the driving output terminal and the second voltage terminal under control of the output control signal;

[0065] in the data writing phase, writing, by the first data writing circuit, a first data voltage provided by a first data line into a first differential control node under control of the switch control signal;

[0066] in the potential maintaining phase, maintaining, by the first data writing circuit, a potential of the first differential control node; and

[0067] in the output phase, controlling, by the input control circuit, connection between an input node and a first voltage terminal under control of the output control signal; controlling, by the differential control circuit, a potential of a first output node and a potential of a second output node based on a potential of the input node under control of the potential of the first differential control node and a potential of the second differential control node; controlling, by the latch circuit, the potential of the driving output terminal based on the potential of the first output node and the potential of the second output node under control of a potential of the intermediate node.

[0068] Optionally, the output circuit further includes a second data writing circuit, and the driving method further includes:

[0069] in the data writing phase, writing, by the second data writing circuit, a second data voltage provided by a second data line into the second differential control node under control of the switch control signal; and

[0070] in the potential maintaining phase, maintaining, by the second data writing circuit, the potential of the second differential control node.

[0071] Optionally, the driving circuit further includes a switch control circuit, the blanking period includes an off phase, the off phase includes the setting period, and the driving method further includes:

[0072] in the off phase, controlling, by the switch control circuit, disconnection between the first output

control node and the second output control node under control of an on-off control signal.

[0073] In a third aspect, embodiments of the present disclosure provide a display device, including the above driving circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0074] FIG. **1** is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0075] FIG. **2** is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0076] FIG. **3** is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0077] FIG. **4** is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0078] FIG. **5** is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0079] FIG. **6** is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0080] FIG. **7**A is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0081] FIG. **7**B is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0082] FIG. **8**A is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0083] FIG. **8**B is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0084] FIG. **9**A is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0085] FIG. **9**B is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0086] FIG. **10**A is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0087] FIG. **10**B is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0088] FIG. **11**A is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0089] FIG. **11**B is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0090] FIG. **12**A is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0091] FIG. **12**B is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0092] FIG. **13**A is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0093] FIG. **13**B is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0094] FIG. **14**A is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0095] FIG. **14**B is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0096] FIG. **15**A is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0097] FIG. **15**B is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0098] FIG. **16**A is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0099] FIG. **16**B is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0100] FIG. **17** is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0101] FIG. **18** is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0102] FIG. **19** is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0103] FIG. **20** is a structural diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0104] FIG. **21**A is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0105] FIG. **21**B is an operation timing diagram of at least one embodiment of the driving circuit shown in FIG. **21**A;

[0106] FIG. **21**C is an operation timing diagram of at least one embodiment of the driving circuit shown in FIG. **21**A;

[0107] FIG. **21**D is a circuit diagram of at least one embodiment of a pixel circuit;

[0108] FIG. **22**A is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0109] FIG. **22**B is an operation timing diagram of at least one embodiment of the driving circuit shown in FIG. **22**A;

[0110] FIG. **22**C is an operation timing diagram of at least one embodiment of the driving circuit shown in FIG. **22**A;

[0111] FIG. **22**D is a waveform diagram of a light emitting control signal provided by each row light emitting control line;

[0112] FIG. **23**A is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0113] FIG. **23**B is an operation timing diagram of at least one embodiment of the driving circuit shown in FIG. **23**A;

[0114] FIG. **23**C is an operation timing diagram of at least one embodiment of the driving circuit shown in FIG. **23**A;

[0115] FIG. **23**D is an operation timing diagram of at least one embodiment of the driving circuit shown in FIG. **23**A;

[0116] FIG. **24** is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0117] FIG. **25** is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0118] FIG. **26**A is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0119] FIG. **26**B is an operation timing diagram of at least one embodiment of the driving circuit shown in FIG. **26**A;

[0120] FIG. **27** is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0121] FIG. **28** is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0122] FIG. **29**A is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0123] FIG. **29**B is an operation timing diagram of at least one embodiment of the driving circuit shown in FIG. **29**A;

[0124] FIG. **30** is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0125] FIG. **31**A is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0126] FIG. **31**B is an operation timing diagram of at least one embodiment of the driving circuit shown in FIG. **31**A;

[0127] FIG. **32** is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0128] FIG. **33** is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0129] FIG. **34** is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0130] FIG. **35** is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0131] FIG. **36** is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0132] FIG. **37** is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0133] FIG. **38** is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0134] FIG. **39** is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0135] FIG. **40** is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0136] FIG. **41** is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0137] FIG. **42** is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure;

[0138] FIG. **43** is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure; and

[0139] FIG. **44** is a circuit diagram of a driving circuit according to at least one embodiment of the present disclosure.

DETAILED DESCRIPTION

[0140] The technical solutions in embodiments of the present disclosure are described clearly and completely in conjunction with drawings in the embodiments of the present disclosure. Apparently, the described embodiments are merely a part of rather than all the embodiments of the present disclosure. All other embodiments obtained by a person ordinary skilled in the art based on the embodiments of the present disclosure without any creative efforts fall within the protection scope of the present disclosure.

[0141] The transistors used in all embodiments of the present disclosure may be thin film transistors, field effect transistors, or other devices having the same characteristics. In the embodiments of the present disclosure, in order to distinguish two terminals of a transistor other than a gate electrode, one of the terminals is referred to as a first terminal, and the other is referred to as a second terminal.

[0142] In practical operation, when the transistor is a thin film transistor or a field effect transistor, the first electrode may be a drain electrode, and the second electrode may be a source electrode; or the first electrode may be a source electrode, and the second electrode may be a drain electrode.

[0143] The driving circuit in the embodiments of the present disclosure includes an output circuit and an inverting circuit;

[0144] the output circuit is electrically connected to an output control terminal, a switch control terminal, a data line and a driving output terminal, and is configured to provide a driving output signal via the driving output terminal based on a data voltage provided by the data line under control of a switch control signal provided by the switch control terminal and an output control signal provided by the output control terminal;

[0145] the inverting circuit includes N stages of inverters, N is a positive integer;

[0146] an input terminal of a first inverter is electrically connected to the driving output terminal, and an output terminal of an N-th inverter is electrically connected to a driving signal output terminal;

[0147] in a case that N is greater than 1, an output terminal of an m-th inverter is electrically connected to an input terminal of an (m+1)-th inverter, and m is a positive integer less than N; and

[0148] the inverter is configured to invert a signal received by the input terminal of the inverter to obtain an inverted signal, and output the inverted signal via the output terminal of the inverter.

[0149] The driving circuit in the embodiments of the present disclosure adopts the inverting circuit. In a case that the inverting circuit includes one stage of inverter, partial low refresh can be achieved. In a case that the inverting circuit includes two stages of inverters, the driving signal provided by the driving signal output terminal can be stabilized.

[0150] As shown in FIG. **1**, the driving circuit in the embodiments of the present disclosure includes an output circuit **10** and an inverting circuit **11**.

[0151] The output circuit **10** is electrically connected to an output control terminal VCT, a switch control terminal SW, a data line SL and a driving output terminal NT, and is

configured to provide a driving output signal via the driving output terminal NT based on a data voltage provided by the data line SL under control of a switch control signal provided by the switch control terminal SW and an output control signal provided by the output control terminal VCT.

[0152] The inverting circuit includes a first inverter F**1**.

[0153] An input terminal of the first inverter F**1** is electrically connected to the driving output terminal NT, and an output terminal of the first inverter F**1** is electrically connected to a driving signal output terminal OT.

[0154] The first inverter F**1** is configured to invert a signal received by its input terminal to obtain an inverted signal, and output the inverted signal via the output terminal of the first inverter F**1**.

[0155] In at least one embodiment of the driving circuit shown in FIG. **1**, N is equal to 1.

[0156] As shown in FIG. **2**, the driving circuit in the embodiments of the present disclosure includes an output circuit **10** and an inverting circuit **11**.

[0157] The output circuit **10** is electrically connected to an output control terminal VCT, a switch control terminal SW, a data line SL and a driving output terminal NT, and is configured to provide a driving output signal via the driving output terminal NT based on a data voltage provided by the data line SL under control of a switch control signal provided by the switch control terminal SW and an output control signal provided by the output control terminal VCT.

[0158] The inverting circuit includes a first inverter F**1** and a second inverter F**2**.

[0159] An input terminal of the first inverter F**1** is electrically connected to the driving output terminal NT, and an output terminal of the first inverter F**1** is electrically connected to an input terminal of the second inverter F**2**.

[0160] An output terminal of the second inverter F**2** is electrically connected to a driving signal output terminal OT.

[0161] The first inverter F**1** is configured to invert a signal received by its input terminal to obtain a first inverted signal, and output the first inverted signal via the output terminal of the first inverter F**1**.

[0162] The second inverter F**2** is configured to invert a signal received by its input terminal to obtain a second inverted signal, and output the second inverted signal via the output terminal of the second inverter F**2**.

[0163] In at least one embodiment shown in FIG. **2**, N is equal to 2.

[0164] In at least one embodiment of the present disclosure, the output circuit includes a first data writing circuit, a differential control circuit, an input control circuit and an output control circuit

[0165] the first data writing circuit is electrically connected to the switch control terminal, a first data line and a first differential control node, and is configured to write a first data voltage provided by the first data line into the first differential control node and maintain a potential of the first differential control node under control of the switch control signal provided by the switch control terminal;

[0166] the differential control circuit is electrically connected to the first differential control node, a second differential control node, an input node, a first output node, and a second output node, and is configured to control a potential of the first output node and a potential of the second output node based on a potential of the input node under control of the potential of the first differential control node and a potential of the second differential control node;

[0167] the input control circuit is electrically connected to the output control terminal, the input node and a first voltage terminal, and is configured to control connection or disconnection between the input node and the first voltage terminal under control of the output control signal provided by the output control terminal; and

[0168] the output control circuit is electrically connected to the output control terminal, the first output node, the second output node and the driving output terminal, and is configured to generate the driving output signal and provide the driving output signal via the driving output terminal based on the potential of the first output node and the potential of the second output node under control of the output control signal.

[0169] Optionally, the first voltage terminal may be a high voltage terminal.

[0170] As shown in FIG. **3**, based on at least one embodiment of the driving circuit shown in FIG. **1**, the output circuit includes a first data writing circuit **31**, a differential control circuit **32**, an input control circuit **33** and an output control circuit **34**.

[0171] The first data writing circuit **31** is electrically connected to the switch control terminal SW, a first data line SL**1** and a first differential control node NC**1**, and is configured to write a first data voltage provided by the first data line SL**1** into the first differential control node NC**1** and maintain a potential of the first differential control node NC**1** under control of the switch control signal provided by the switch control terminal SW.

[0172] The second differential control node NC**2** is electrically connected to an initial voltage terminal I**1**, and the initial voltage terminal I**1** is configured to provide an initial voltage Vinit.

[0173] The differential control circuit **32** is electrically connected to the first differential control node NC**1**, a second differential control node NC**2**, an input node N**2**, a first output node N**3** and a second output node N**4**, and is configured to control a potential of the first output node N**3** and a potential of the second output node N**4** based on a potential of the input node N**2** under control of the potential of the first differential control node NC**1** and a potential of the second differential control node NC**2**.

[0174] The input control circuit **33** is electrically connected to the output control terminal VCT, the input node N**2** and a first voltage terminal V**1**, and is configured to control connection or disconnection between the input node N**2** and the first voltage terminal V**1** under control of the output control signal provided by the output control terminal VCT.

[0175] The output control circuit **34** is electrically connected to the output control terminal VCT, the first output node N**3**, the second output node N**4** and the driving output terminal NT, and is configured to generate the driving output signal and provide the driving output signal via the driving output terminal NT based on the potential of the first output node N**3** and the potential of the second output node N**4** under control of the output control signal.

[0176] As shown in FIG. **4**, based on at least one embodiment of the driving circuit shown in FIG. **2**, the output circuit includes a first data writing circuit **31**, a differential control circuit **32**, an input control circuit **33** and an output control circuit **34**.

[0177] The first data writing circuit **31** is electrically connected to the switch control terminal SW, a first data line SL**1** and a first differential control node NC**1**, and is configured to write a first data voltage provided by the first data line SL**1** into the first differential control node NC**1** and maintain a potential of the first differential control node NC**1** under control of the switch control signal provided by the switch control terminal SW.

[0178] The second differential control node NC is electrically connected to an initial voltage terminal I**1**, and the initial voltage terminal I**1** is configured to provide an initial voltage Vinit.

[0179] The differential control circuit **32** is electrically connected to the first differential control node NC**1**, a second differential control node NC**2**, an input node N**2**, a first output node N**3** and a second output node N**4**, and is configured to control a potential of the first output node N**3** and a potential of the second output node N**4** based on a potential of the input node N**2** under control of the potential of the first differential control node NC**1** and a potential of the second differential control node NC**2**.

[0180] The input control circuit **33** is electrically connected to the output control terminal VCT, the input node N**2** and a first voltage terminal V**1**, and is configured to control connection or disconnection between the input node N**2** and the first voltage terminal V**1** under control of the output control signal provided by the output control terminal VCT.

[0181] The output control circuit **34** is electrically connected to the output control terminal VCT, the first output node N**3**, the second output node N**4** and the driving output terminal NT, and is configured to generate the driving output signal and provide the driving output signal via the driving output terminal NT based on the potential of the first output node N**3** and the potential of the second output node N**4** under control of the output control signal.

[0182] In at least one embodiment of the present disclosure, the output circuit further includes a second data writing circuit;

[0183] the second data writing circuit is electrically connected to the switch control terminal, a second data line and the second differential control node, and is configured to write a second data voltage provided by the second data line into the second differential control node and maintain the potential of the second differential control node under control of the switch control signal provided by the switch control terminal.

[0184] In a specific implementation, the output circuit may further include the second data writing circuit, and the second data writing circuit writes the second data voltage into the second differential control node and maintain the potential of the second differential control node under control of the switch control signal.

[0185] As shown in FIG. **5**, based on at least one embodiment of the driving circuit shown in FIG. **1**, the output circuit includes a first data writing circuit **31**, a differential control circuit **32**, an input control circuit **33**, an output control circuit **34** and a second data writing circuit **35**.

[0186] The first data writing circuit **31** is electrically connected to the switch control terminal SW, a first data line SL**1** and a first differential control node NC**1**, and is configured to write a first data voltage provided by the first data line SL**1** into the first differential control node NC**1** and maintain a potential of the first differential control node NC**1** under control of the switch control signal provided by the switch control terminal SW.

[0187] The second data writing circuit **35** is electrically connected to the switch control terminal SW, a second data line SL**2** and the second differential control node NC**2**, and is configured to write a second data voltage provided by the second data line SL**2** into the second differential control node NC**2** and maintain the potential of the second differential control node NC**2** under control of the switch control signal provided by the switch control terminal SW.

[0188] The differential control circuit **32** is electrically connected to the first differential control node NC**1**, a second differential control node NC**2**, an input node N**2**, a first output node N**3** and a second output node N**4**, and is configured to control a potential of the first output node N**3** and a potential of the second output node N**4** based on a potential of the input node N**2** under control of the potential of the first differential control node NC**1** and a potential of the second differential control node NC**2**.

[0189] The input control circuit **33** is electrically connected to the output control terminal VCT, the input node N**2** and a first voltage terminal V**1**, and is configured to control connection or disconnection between the input node N**2** and the first voltage terminal V**1** under control of the output control signal provided by the output control terminal VCT.

[0190] The output control circuit **34** is electrically connected to the output control terminal VCT, the first output node N**3**, the second output node N**4** and the driving output terminal NT, and is configured to generate the driving output signal and provide the driving output signal via the driving output terminal NT based on the potential of the first output node N**3** and the potential of the second output node N**4** under control of the output control signal.

[0191] As shown in FIG. **6**, based on at least one embodiment of the driving circuit shown in FIG. **2**, the output circuit includes a first data writing circuit **31**, a differential control circuit **32**, an input control circuit **33**, an output control circuit **34** and a second data writing circuit **35**.

[0192] The first data writing circuit **31** is electrically connected to the switch control terminal SW, a first data line SL**1** and a first differential control node NC**1**, and is configured to write a first data voltage provided by the first data line SL**1** into the first differential control node NC**1** and maintain a potential of the first differential control node NC**1** under control of the switch control signal provided by the switch control terminal SW.

[0193] The second data writing circuit **35** is electrically connected to the switch control terminal SW, a second data line SL**2** and the second differential control node NC**2**, and is configured to write a second data voltage provided by the second data line SL**2** into the second differential control node NC**2** and maintain the potential of the second differential control node NC**2** under control of the switch control signal provided by the switch control terminal SW.

[0194] The differential control circuit **32** is electrically connected to the first differential control node NC**1**, a second differential control node NC**2**, an input node N**2**, a first output node N**3** and a second output node N**4**, and is configured to control a potential of the first output node N**3** and a potential of the second output node N**4** based on a potential of the input node N**2** under control of the potential of the first differential control node NC**1** and a potential of the second differential control node NC**2**.

[0195] The input control circuit **33** is electrically connected to the output control terminal VCT, the input node N**2** and a first voltage terminal V**1**, and is configured to control connection or disconnection between the input node N**2** and the first voltage terminal V**1** under control of the output control signal provided by the output control terminal VCT.

[0196] The output control circuit **34** is electrically connected to the output control terminal VCT, the first output node N**3**, the second output node N**4** and the driving output terminal NT, and is configured to generate the driving output signal and provide the driving output signal via the driving output terminal NT based on the potential of the first output node N**3** and the potential of the second output node N**4** under control of the output control signal.

[0197] The driving circuit in at least one embodiment of the present disclosure further includes a switch control circuit;

[0198] the switch control circuit is electrically connected to an on-off control terminal, a first output control node and a second output control node, and is configured to control connection or disconnection between the first output control node and the second output control node under control of an on-off control signal provided by the on-off control terminal;

[0199] the first output control node is electrically connected to the driving output terminal, and the second output control node is electrically connected to the input terminal of the first inverter; or,

[0200] the first output control node is electrically connected to the output terminal of the N-th inverter, and the second output control node is electrically connected to the driving signal output terminal; or,

[0201] N is greater than 1, the first output control node is electrically connected to the output terminal of the m-th inverter, and the second output control node is electrically connected to the input terminal of the (m+1)-th inverter.

[0202] In a specific implementation, the driving circuit may further include the switch control circuit, and the switch control circuit controls connection or disconnection between the first output control node and the second output control node under control of the on-off control signal.

[0203] As shown in FIG. **7**A, based on at least one embodiment of the driving circuit shown in FIG. **3**, the driving circuit according to at least one embodiment of the present disclosure further includes a switch control circuit **70**.

[0204] The switch control circuit **70** is electrically connected to an on-off control terminal VCT**2**, the driving output terminal NT and the input terminal of the first inverter F**1**, and is configured to control connection or disconnection between the driving output terminal NT and the input terminal of the first inverter F**1** under control of an on-off control signal provided by the on-off control terminal VCT**2**.

[0205] In at least one embodiment of the driving circuit shown in FIG. **7**A, reference sign NS**1** denotes the first output control node, and reference sign NS**2** denotes the second output control node.

[0206] NS**1** is electrically connected to NT, and NS**2** is electrically connected to the input terminal of the first inverter F**1**.

[0207] As shown in FIG. **7**B, based on at least one embodiment of the driving circuit shown in FIG. **5**, the driving circuit according to at least one embodiment of the present disclosure further includes a switch control circuit **70**.

[0208] The switch control circuit **70** is electrically connected to an on-off control terminal VCT**2**, the driving output terminal NT and the input terminal of the first inverter F**1**, and is configured to control connection or disconnection between the driving output terminal NT and the input terminal of the first inverter F**1** under control of an on-off control signal provided by the on-off control terminal VCT**2**.

[0209] In at least one embodiment of the driving circuit shown in FIG. **7**B, reference sign NS**1** denotes the first output control node, and reference sign NS**2** denotes the second output control node.

[0210] NS**1** is electrically connected to NT, and NS**2** is electrically connected to the input terminal of the first inverter F**1**.

[0211] As shown in FIG. **8**A, based on at least one embodiment of the driving circuit shown in FIG. **3**, the driving circuit according to at least one embodiment of the present disclosure further includes a switch control circuit **70**.

[0212] The switch control circuit **70** is electrically connected to an on-off control terminal VCT**2**, the output terminal of the first inverter F**1** and the driving signal output terminal OT, and is configured to control connection or disconnection between the output terminal of the first inverter F**1** and the driving signal output terminal OT under control of an on-off control signal provided by the on-off control terminal VCT**2**.

[0213] In at least one embodiment of the driving circuit shown in FIG. **8**A, reference sign NS**1** denotes the first output control node, and reference sign NS**2** denotes the second output control node.

[0214] NS**1** is electrically connected to the output terminal of the first inverter F**1**, and NS**2** is electrically connected to the driving signal output terminal OT.

[0215] As shown in FIG. **8**B, based on at least one embodiment of the driving circuit shown in FIG. **5**, the driving circuit according to at least one embodiment of the present disclosure further includes a switch control circuit **70**.

[0216] The switch control circuit **70** is electrically connected to an on-off control terminal VCT**2**, the output terminal of the first inverter F**1** and the driving signal output terminal OT, and is configured to control connection or disconnection between the output terminal of the first inverter F**1** and the driving signal output terminal OT under control of an on-off control signal provided by the on-off control terminal VCT**2**.

[0217] In at least one embodiment of the driving circuit shown in FIG. **8**B, reference sign NS**1** denotes the first output control node, and reference sign NS**2** denotes the second output control node.

[0218] NS**1** is electrically connected to the output terminal of the first inverter F**1**, and NS**2** is electrically connected to the driving signal output terminal OT.

[0219] As shown in FIG. **9**A, based on at least one embodiment of the driving circuit shown in FIG. **4**, the driving circuit according to at least one embodiment of the present disclosure further includes a switch control circuit **70**.

[0220] The switch control circuit **70** is electrically connected to an on-off control terminal VCT**2**, the driving

output terminal NT and the input terminal of the first inverter F1, and is configured to control connection or disconnection between the driving output terminal NT and the input terminal of the first inverter F1 under control of an on-off control signal provided by the on-off control terminal VCT2.

[0221] In at least one embodiment of the driving circuit shown in FIG. 9A, reference sign NS1 denotes the first output control node, and reference sign NS2 denotes the second output control node.

[0222] NS1 is electrically connected to the driving output terminal NT, and NS2 is electrically connected to the input terminal of the first inverter F1.

[0223] As shown in FIG. 9B, based on at least one embodiment of the driving circuit shown in FIG. 6, the driving circuit according to at least one embodiment of the present disclosure further includes a switch control circuit 70.

[0224] The switch control circuit 70 is electrically connected to an on-off control terminal VCT2, the driving output terminal NT and the input terminal of the first inverter F1, and is configured to control connection or disconnection between the driving output terminal NT and the input terminal of the first inverter F1 under control of an on-off control signal provided by the on-off control terminal VCT2.

[0225] In at least one embodiment of the driving circuit shown in FIG. 9B, reference sign NS1 denotes the first output control node, and reference sign NS2 denotes the second output control node.

[0226] NS1 is electrically connected to the driving output terminal NT, and NS2 is electrically connected to the input terminal of the first inverter F1.

[0227] As shown in FIG. 10A, based on at least one embodiment of the driving circuit shown in FIG. 4, the driving circuit according to at least one embodiment of the present disclosure further includes a switch control circuit 70.

[0228] The switch control circuit 70 is electrically connected to an on-off control terminal VCT2, the output terminal of the first inverter F1 and the input terminal of the second inverter F2, and is configured to control connection or disconnection between the output terminal of the first inverter F1 and the input terminal of the second inverter F2 under control of an on-off control signal provided by the on-off control terminal VCT2.

[0229] In at least one embodiment of the driving circuit shown in FIG. 10A, reference sign NS1 denotes the first output control node, and reference sign NS2 denotes the second output control node.

[0230] NS1 is electrically connected to the output terminal of the first inverter F1, and NS2 is electrically connected to the input terminal of the second inverter F2.

[0231] As shown in FIG. 10B, based on at least one embodiment of the driving circuit shown in FIG. 6, the driving circuit according to at least one embodiment of the present disclosure further includes a switch control circuit 70.

[0232] The switch control circuit 70 is electrically connected to an on-off control terminal VCT2, the output terminal of the first inverter F1 and the input terminal of the second inverter F2, and is configured to control connection or disconnection between the output terminal of the first inverter F1 and the input terminal of the second inverter F2 under control of an on-off control signal provided by the on-off control terminal VCT2.

[0233] In at least one embodiment of the driving circuit shown in FIG. 10B, reference sign NS1 denotes the first output control node, and reference sign NS2 denotes the second output control node.

[0234] NS1 is electrically connected to the output terminal of the first inverter F1, and NS2 is electrically connected to the input terminal of the second inverter F2.

[0235] As shown in FIG. 11A, based on at least one embodiment of the driving circuit shown in FIG. 4, the driving circuit according to at least one embodiment of the present disclosure further includes a switch control circuit 70.

[0236] The switch control circuit 70 is electrically connected to an on-off control terminal VCT2, the output terminal of the second inverter F2 and the driving signal output terminal OT, and is configured to control connection or disconnection between the output terminal of the second inverter F2 and the driving signal output terminal OT under control of an on-off control signal provided by the on-off control terminal VCT2.

[0237] In at least one embodiment of the driving circuit shown in FIG. 11A, reference sign NS1 denotes the first output control node, and reference sign NS2 denotes the second output control node.

[0238] NS1 is electrically connected to the output terminal of the second inverter F2, and NS2 is electrically connected to the driving signal output terminal OT.

[0239] As shown in FIG. 11B, based on at least one embodiment of the driving circuit shown in FIG. 6, the driving circuit according to at least one embodiment of the present disclosure further includes a switch control circuit 70.

[0240] The switch control circuit 70 is electrically connected to an on-off control terminal VCT2, the output terminal of the second inverter F2 and the driving signal output terminal OT, and is configured to control connection or disconnection between the output terminal of the second inverter F2 and the driving signal output terminal OT under control of an on-off control signal provided by the on-off control terminal VCT2.

[0241] In at least one embodiment of the driving circuit shown in FIG. 11B, reference sign NS1 denotes the first output control node, and reference sign NS2 denotes the second output control node.

[0242] NS1 is electrically connected to the output terminal of the second inverter F2, and NS2 is electrically connected to the driving signal output terminal OT.

[0243] In at least one embodiment of the present disclosure, the output control circuit includes a latch circuit and a set circuit;

[0244] the set circuit is electrically connected to the output control terminal, an intermediate node, the driving output terminal and a second voltage terminal, and is configured to control connection or disconnection between the intermediate node and the second voltage terminal and control connection or disconnection between the driving output terminal and the second voltage terminal under control of the output control signal; and

[0245] the latch circuit is electrically connected to the first output node, the second output node, the intermediate node, the driving output terminal and the second voltage terminal, and is configured to control a potential of the driving output terminal based on the potential

of the first output node and the potential of the second output node under control of a potential of the intermediate node.

[0246] In a specific implementation, the output control circuit may include the latch circuit and the set circuit. The set circuit controls connection or disconnection between the intermediate node and the second voltage terminal and controls connection or disconnection between the driving output terminal and the second voltage terminal under control of the output control signal; the latch circuit controls the potential of the driving output terminal based on the potential of the first output node and the potential of the second output node under control of the potential of the intermediate node.

[0247] In at least one embodiment of the present disclosure, the latch circuit is configured to control connection or disconnection between the second output node and the driving output terminal and connection or disconnection between the driving output terminal and the second voltage terminal under control of the potential of the intermediate node, and to control connection or disconnection between the first output node and the intermediate node and connection or disconnection between the intermediate node and the second voltage terminal under control of the potential of the driving output terminal.

[0248] Optionally, the second voltage terminal may be a low voltage terminal.

[0249] As shown in FIG. **12**A, based on at least one embodiment of the driving circuit shown in FIG. **7**A, in at least one embodiment of the present disclosure, the output control circuit includes a latch circuit **41** and a set circuit **42**.

[0250] The set circuit **42** is electrically connected to the output control terminal VCT, the intermediate node N**6**, the driving output terminal NT and the second voltage terminal V**2**, and is configured to control connection or disconnection between the intermediate node N**6** and the second voltage terminal V**2** and control connection or disconnection between the driving output terminal NT and the second voltage terminal V**2** under control of the output control signal.

[0251] The latch circuit **41** is electrically connected to the first output node N**3**, the second output node N**4**, the intermediate node N**6**, the driving output terminal NT and the second voltage terminal V**2**, and is configured to control a potential of the driving output terminal NT based on the potential of the first output node N**3** and the potential of the second output node N**4** under control of a potential of the intermediate node N**6**.

[0252] In at least one embodiment of the driving circuit shown in FIG. **12**A, reference sign NS**1** denotes the first output control node, and reference sign NS**2** denotes the second output control node.

[0253] NS**1** is electrically connected to the driving output terminal NT, and NS**2** is electrically connected to the input terminal of the first inverter F**1**.

[0254] As shown in FIG. **12**B, based on at least one embodiment of the driving circuit shown in FIG. **7**B, in at least one embodiment of the present disclosure, the output control circuit includes a latch circuit **41** and a set circuit **42**.

[0255] The set circuit **42** is electrically connected to the output control terminal VCT, the intermediate node N**6**, the driving output terminal NT and the second voltage terminal V**2**, and is configured to control connection or disconnection between the intermediate node N**6** and the second voltage terminal V**2** and control connection or disconnection between the driving output terminal NT and the second voltage terminal V**2** under control of the output control signal.

[0256] The latch circuit **41** is electrically connected to the first output node N**3**, the second output node N**4**, the intermediate node N**6**, the driving output terminal NT and the second voltage terminal V**2**, and is configured to control a potential of the driving output terminal NT based on the potential of the first output node N**3** and the potential of the second output node N**4** under control of a potential of the intermediate node N**6**.

[0257] In at least one embodiment of the driving circuit shown in FIG. **12**B, reference sign NS**1** denotes the first output control node, and reference sign NS**2** denotes the second output control node.

[0258] NST is electrically connected to the driving output terminal NT, and NS**2** is electrically connected to the input terminal of the first inverter F**1**.

[0259] As shown in FIG. **13**A, based on at least one embodiment of the driving circuit shown in FIG. **8**A, in at least one embodiment of the present disclosure, the output control circuit includes a latch circuit **41** and a set circuit **42**.

[0260] The set circuit **42** is electrically connected to the output control terminal VCT, the intermediate node N**6**, the driving output terminal NT and the second voltage terminal V**2**, and is configured to control connection or disconnection between the intermediate node N**6** and the second voltage terminal V**2** and control connection or disconnection between the driving output terminal NT and the second voltage terminal V**2** under control of the output control signal.

[0261] The latch circuit **41** is electrically connected to the first output node N**3**, the second output node N**4**, the intermediate node N**6**, the driving output terminal NT and the second voltage terminal V**2**, and is configured to control a potential of the driving output terminal NT based on the potential of the first output node N**3** and the potential of the second output node N**4** under control of a potential of the intermediate node N**6**.

[0262] In at least one embodiment of the driving circuit shown in FIG. **13**A, reference sign NS**1** denotes the first output control node, and reference sign NS**2** denotes the second output control node.

[0263] NS**1** is electrically connected to the output terminal of the first inverter F**1**, and NS**2** is electrically connected to the driving signal output terminal OT.

[0264] As shown in FIG. **13**B, based on at least one embodiment of the driving circuit shown in FIG. **8**B, in at least one embodiment of the present disclosure, the output control circuit includes a latch circuit **41** and a set circuit **42**.

[0265] The set circuit **42** is electrically connected to the output control terminal VCT, the intermediate node N**6**, the driving output terminal NT and the second voltage terminal V**2**, and is configured to control connection or disconnection between the intermediate node N**6** and the second voltage terminal V**2** and control connection or disconnection between the driving output terminal NT and the second voltage terminal V**2** under control of the output control signal.

[0266] The latch circuit **41** is electrically connected to the first output node N**3**, the second output node N**4**, the intermediate node N**6**, the driving output terminal NT and the second voltage terminal V**2**, and is configured to control

a potential of the driving output terminal NT based on the potential of the first output node N3 and the potential of the second output node N4 under control of a potential of the intermediate node N6.

[0267] In at least one embodiment of the driving circuit shown in FIG. 13B, reference sign NS1 denotes the first output control node, and reference sign NS2 denotes the second output control node.

[0268] NS1 is electrically connected to the output terminal of the first inverter F1, and NS2 is electrically connected to the driving signal output terminal OT.

[0269] As shown in FIG. 14A, based on at least one embodiment of the driving circuit shown in FIG. 9A, in at least one embodiment of the present disclosure, the output control circuit includes a latch circuit 41 and a set circuit 42.

[0270] The set circuit 42 is electrically connected to the output control terminal VCT, the intermediate node N6, the driving output terminal NT and the second voltage terminal V2, and is configured to control connection or disconnection between the intermediate node N6 and the second voltage terminal V2 and control connection or disconnection between the driving output terminal NT and the second voltage terminal V2 under control of the output control signal.

[0271] The latch circuit 41 is electrically connected to the first output node N3, the second output node N4, the intermediate node N6, the driving output terminal NT and the second voltage terminal V2, and is configured to control a potential of the driving output terminal NT based on the potential of the first output node N3 and the potential of the second output node N4 under control of a potential of the intermediate node N6.

[0272] In at least one embodiment of the driving circuit shown in FIG. 14A, reference sign NST denotes the first output control node, and reference sign NS2 denotes the second output control node.

[0273] NS1 is electrically connected to the driving output terminal NT, and NS2 is electrically connected to the input terminal of the first inverter F1.

[0274] As shown in FIG. 14B, based on at least one embodiment of the driving circuit shown in FIG. 9B, in at least one embodiment of the present disclosure, the output control circuit includes a latch circuit 41 and a set circuit 42.

[0275] The set circuit 42 is electrically connected to the output control terminal VCT, the intermediate node N6, the driving output terminal NT and the second voltage terminal V2, and is configured to control connection or disconnection between the intermediate node N6 and the second voltage terminal V2 and control connection or disconnection between the driving output terminal NT and the second voltage terminal V2 under control of the output control signal.

[0276] The latch circuit 41 is electrically connected to the first output node N3, the second output node N4, the intermediate node N6, the driving output terminal NT and the second voltage terminal V2, and is configured to control a potential of the driving output terminal NT based on the potential of the first output node N3 and the potential of the second output node N4 under control of a potential of the intermediate node N6.

[0277] In at least one embodiment of the driving circuit shown in FIG. 14B, reference sign NS1 denotes the first output control node, and reference sign NS2 denotes the second output control node.

[0278] NS1 is electrically connected to the driving output terminal NT, and NS2 is electrically connected to the input terminal of the first inverter F1.

[0279] As shown in FIG. 15A, based on at least one embodiment of the driving circuit shown in FIG. 10A, in at least one embodiment of the present disclosure, the output control circuit includes a latch circuit 41 and a set circuit 42.

[0280] The set circuit 42 is electrically connected to the output control terminal VCT, the intermediate node N6, the driving output terminal NT and the second voltage terminal V2, and is configured to control connection or disconnection between the intermediate node N6 and the second voltage terminal V2 and control connection or disconnection between the driving output terminal NT and the second voltage terminal V2 under control of the output control signal.

[0281] The latch circuit 41 is electrically connected to the first output node N3, the second output node N4, the intermediate node N6, the driving output terminal NT and the second voltage terminal V2, and is configured to control a potential of the driving output terminal NT based on the potential of the first output node N3 and the potential of the second output node N4 under control of a potential of the intermediate node N6.

[0282] In at least one embodiment of the driving circuit shown in FIG. 15A, reference sign NS1 denotes the first output control node, and reference sign NS2 denotes the second output control node.

[0283] NS1 is electrically connected to the output terminal of the first inverter F1, and NS2 is electrically connected to the input terminal of the second inverter F2.

[0284] As shown in FIG. 15B, based on at least one embodiment of the driving circuit shown in FIG. 10B, in at least one embodiment of the present disclosure, the output control circuit includes a latch circuit 41 and a set circuit 42.

[0285] The set circuit 42 is electrically connected to the output control terminal VCT, the intermediate node N6, the driving output terminal NT and the second voltage terminal V2, and is configured to control connection or disconnection between the intermediate node N6 and the second voltage terminal V2 and control connection or disconnection between the driving output terminal NT and the second voltage terminal V2 under control of the output control signal.

[0286] The latch circuit 41 is electrically connected to the first output node N3, the second output node N4, the intermediate node N6, the driving output terminal NT and the second voltage terminal V2, and is configured to control a potential of the driving output terminal NT based on the potential of the first output node N3 and the potential of the second output node N4 under control of a potential of the intermediate node N6.

[0287] In at least one embodiment of the driving circuit shown in FIG. 15B, reference sign NS1 denotes the first output control node, and reference sign NS2 denotes the second output control node.

[0288] NS1 is electrically connected to the output terminal of the first inverter F1, and NS2 is electrically connected to the input terminal of the second inverter F2.

[0289] As shown in FIG. 16A, based on at least one embodiment of the driving circuit shown in FIG. 11A, in at least one embodiment of the present disclosure, the output control circuit includes a latch circuit 41 and a set circuit 42.

[0290] The set circuit **42** is electrically connected to the output control terminal VCT, the intermediate node N**6**, the driving output terminal NT and the second voltage terminal V**2**, and is configured to control connection or disconnection between the intermediate node N**6** and the second voltage terminal V**2** and control connection or disconnection between the driving output terminal NT and the second voltage terminal V**2** under control of the output control signal.

[0291] The latch circuit **41** is electrically connected to the first output node N**3**, the second output node N**4**, the intermediate node N**6**, the driving output terminal NT and the second voltage terminal V**2**, and is configured to control a potential of the driving output terminal NT based on the potential of the first output node N**3** and the potential of the second output node N**4** under control of a potential of the intermediate node N**6**.

[0292] In at least one embodiment of the driving circuit shown in FIG. **16**A, reference sign NS**1** denotes the first output control node, and reference sign NS**2** denotes the second output control node.

[0293] NS**1** is electrically connected to the output terminal of the second inverter F**2**, and NS**2** is electrically connected to the driving signal output terminal OT.

[0294] As shown in FIG. **16**B, based on at least one embodiment of the driving circuit shown in FIG. **11**B, in at least one embodiment of the present disclosure, the output control circuit includes a latch circuit **41** and a set circuit **42**.

[0295] The set circuit **42** is electrically connected to the output control terminal VCT, the intermediate node N**6**, the driving output terminal NT and the second voltage terminal V**2**, and is configured to control connection or disconnection between the intermediate node N**6** and the second voltage terminal V**2** and control connection or disconnection between the driving output terminal NT and the second voltage terminal V**2** under control of the output control signal.

[0296] The latch circuit **41** is electrically connected to the first output node N**3**, the second output node N**4**, the intermediate node N**6**, the driving output terminal NT and the second voltage terminal V**2**, and is configured to control a potential of the driving output terminal NT based on the potential of the first output node N**3** and the potential of the second output node N**4** under control of a potential of the intermediate node N**6**.

[0297] In at least one embodiment of the driving circuit shown in FIG. **16**B, reference sign NS**1** denotes the first output control node, and reference sign NS**2** denotes the second output control node.

[0298] NS**1** is electrically connected to the output terminal of the second inverter F**2**, and NS**2** is electrically connected to the driving signal output terminal OT.

[0299] In at least one embodiment of the present disclosure, a frame time includes a blanking period, the blanking period includes an off phase, and the off phase includes a setting period;

[0300] the set circuit is configured to control connection between the intermediate node and the second voltage terminal and control connection between the driving output terminal and the second voltage terminal under control of the output control signal during the setting period; and

[0301] the switch control circuit is configured to control disconnection between the first output control node and the second output control node under control of the on-off control signal during the off phase.

[0302] In a specific implementation, the frame time includes the blanking period, the blanking period includes the off phase, the off phase includes the setting period; in the setting period, the set circuit controls connection between the intermediate node and the second voltage terminal and controls connection between the driving output terminal and the second voltage terminal under control of the output control signal; and in the off phase, the switch control circuit controls disconnection between the first output control node and the second output control node under control of the on-off control signal. In this way, in the blanking period, the driving signal provided by the driving signal output terminal is not affected by the rising edge and the falling edge of the driving output signal provided by the driving output terminal.

[0303] As shown in FIG. **17**, based on at least one embodiment of the driving circuit shown in FIG. **3**, in at least one embodiment of the present disclosure, the output control circuit includes a latch circuit **41** and a set circuit **42**.

[0304] The set circuit **42** is electrically connected to the output control terminal VCT, the intermediate node N**6**, the driving output terminal NT and the second voltage terminal V**2**, and is configured to control connection or disconnection between the intermediate node N**6** and the second voltage terminal V**2** and control connection or disconnection between the driving output terminal NT and the second voltage terminal V**2** under control of the output control signal.

[0305] The latch circuit **41** is electrically connected to the first output node N**3**, the second output node N**4**, the intermediate node N**6**, the driving output terminal NT and the second voltage terminal V**2**, and is configured to control a potential of the driving output terminal NT based on the potential of the first output node N**3** and the potential of the second output node N**4** under control of a potential of the intermediate node N**6**.

[0306] As shown in FIG. **18**, based on at least one embodiment of the driving circuit shown in FIG. **4**, in at least one embodiment of the present disclosure, the output control circuit includes a latch circuit **41** and a set circuit **42**.

[0307] The set circuit **42** is electrically connected to the output control terminal VCT, the intermediate node N**6**, the driving output terminal NT and the second voltage terminal V**2**, and is configured to control connection or disconnection between the intermediate node N**6** and the second voltage terminal V**2** and control connection or disconnection between the driving output terminal NT and the second voltage terminal V**2** under control of the output control signal.

[0308] The latch circuit **41** is electrically connected to the first output node N**3**, the second output node N**4**, the intermediate node N**6**, the driving output terminal NT and the second voltage terminal V**2**, and is configured to control a potential of the driving output terminal NT based on the potential of the first output node N**3** and the potential of the second output node N**4** under control of a potential of the intermediate node N**6**.

[0309] As shown in FIG. **19**, based on at least one embodiment of the driving circuit shown in FIG. **5**, in at least one embodiment of the present disclosure, the output control circuit includes a latch circuit **41** and a set circuit **42**.

[0310] The set circuit **42** is electrically connected to the output control terminal VCT, the intermediate node N**6**, the driving output terminal NT and the second voltage terminal V**2**, and is configured to control connection or disconnection between the intermediate node N**6** and the second voltage terminal V**2** and control connection or disconnection between the driving output terminal NT and the second voltage terminal V**2** under control of the output control signal.

[0311] The latch circuit **41** is electrically connected to the first output node N**3**, the second output node N**4**, the intermediate node N**6**, the driving output terminal NT and the second voltage terminal V**2**, and is configured to control a potential of the driving output terminal NT based on the potential of the first output node N**3** and the potential of the second output node N**4** under control of a potential of the intermediate node N**6**.

[0312] As shown in FIG. **20**, based on at least one embodiment of the driving circuit shown in FIG. **6**, in at least one embodiment of the present disclosure, the output control circuit includes a latch circuit **41** and a set circuit **42**.

[0313] The set circuit **42** is electrically connected to the output control terminal VCT, the intermediate node N**6**, the driving output terminal NT and the second voltage terminal V**2**, and is configured to control connection or disconnection between the intermediate node N**6** and the second voltage terminal V**2** and control connection or disconnection between the driving output terminal NT and the second voltage terminal V**2** under control of the output control signal.

[0314] The latch circuit **41** is electrically connected to the first output node N**3**, the second output node N**4**, the intermediate node N**6**, the driving output terminal NT and the second voltage terminal V**2**, and is configured to control a potential of the driving output terminal NT based on the potential of the first output node N**3** and the potential of the second output node N**4** under control of a potential of the intermediate node N**6**.

[0315] Optionally, N is equal to 1, the inverting circuit includes the first inverter, and the first inverter includes a first transistor and a second transistor;

[0316] a gate electrode of the first transistor is electrically connected to the input terminal of the first inverter, a first electrode of the first transistor is electrically connected to a first voltage terminal, and a second electrode of the first transistor and a first electrode of the second transistor are both electrically connected to the driving signal output terminal;

[0317] a gate electrode of the second transistor is electrically connected to the input terminal of the first inverter, and a second electrode of the second transistor is electrically connected to a second voltage terminal; and

[0318] the first transistor is a p-type transistor, and the second transistor is an n-type transistor.

[0319] Optionally, N is equal to 2, the inverting circuit includes the first inverter and a second inverter, the first inverter includes a first transistor and a second transistor, and the second inverter includes a third transistor and a fourth transistor;

[0320] a gate electrode of the first transistor is electrically connected to the input terminal of the first inverter, a first electrode of the first transistor is electrically connected to a first voltage terminal, and a second electrode of the first transistor and a first electrode of the second transistor are both electrically connected to an input terminal of the second inverter;

[0321] a gate electrode of the second transistor is electrically connected to the input terminal of the first inverter, and a second electrode of the second transistor is electrically connected to a second voltage terminal;

[0322] a gate electrode of the third transistor and a gate electrode of the fourth transistor are both electrically connected to the input terminal of the second inverter, a first electrode of the third transistor is electrically connected to the first voltage terminal, and a second electrode of the third transistor and a first electrode of the fourth transistor are both electrically connected to the driving signal output terminal;

[0323] a second electrode of the fourth transistor is electrically connected to the second voltage terminal; and

[0324] the first transistor is a p-type transistor, the second transistor is an n-type transistor; the third transistor is a p-type transistor, and the fourth transistor is an n-type transistor.

[0325] the first data writing circuit includes a fifth transistor and a first capacitor;

[0326] a gate electrode of the fifth transistor is electrically connected to the switch control terminal, a first electrode of the fifth transistor is electrically connected to the first data line, and a second electrode of the fifth transistor is electrically connected to the first differential control node; and

[0327] a first terminal of the first capacitor is electrically connected to the first differential control node, and a second terminal of the first capacitor is electrically connected to a second voltage terminal.

[0328] Optionally, the second data writing circuit includes a sixth transistor and a second capacitor, a gate electrode of the sixth transistor is electrically connected to the switch control terminal, a first electrode of the sixth transistor is electrically connected to the second data line, and a second electrode of the sixth transistor is electrically connected to the second differential control node; and

[0329] a first terminal of the second capacitor is electrically connected to the second differential control node, and a second terminal of the second capacitor is electrically connected to the second voltage terminal.

[0330] Optionally, the switch control circuit includes a seventh transistor;

[0331] a gate electrode of the seventh transistor is electrically connected to the on-off control terminal, a first electrode of the seventh transistor is electrically connected to the first output control node, and a second electrode of the seventh transistor is electrically connected to the second output control node.

[0332] In at least one embodiment of the present disclosure, the first output control node is electrically connected to the driving output terminal, and the second output control node is electrically connected to the input terminal of the first inverter; or,

[0333] the first output control node is electrically connected to the output terminal of the N-th inverter, and the second output control node is electrically connected to the driving signal output terminal; or,

[0334] N is greater than 1, the first output control node is electrically connected to the output terminal of the

m-th inverter, and the second output control node is electrically connected to the input terminal of the (m+1)-th inverter.

[0335] Optionally, the input control circuit includes an eighth transistor, and the differential control circuit includes a ninth transistor and a tenth transistor;

[0336] a gate electrode of the eighth transistor is electrically connected to the output control terminal, a first electrode of the eighth transistor is electrically connected to the first voltage terminal, and a second electrode of the eighth transistor is electrically connected to the input node;

[0337] a gate electrode of the ninth transistor is electrically connected to the first differential control node, a first electrode of the ninth transistor is electrically connected to the input node, and a second electrode of the ninth transistor is electrically connected to the first output node; and

[0338] a gate electrode of the tenth transistor is electrically connected to the second differential control node, a first electrode of the tenth transistor is electrically connected to the input node, and a second electrode of the tenth transistor is electrically connected to the second output node.

[0339] Optionally, the set circuit includes an eleventh transistor and a twelfth transistor;

[0340] a gate electrode of the eleventh transistor is electrically connected to the output control terminal, a first electrode of the eleventh transistor is electrically connected to the intermediate node, and a second electrode of the eleventh transistor is electrically connected to the second voltage terminal; and

[0341] a gate electrode of the twelfth transistor is electrically connected to the output control terminal, a first electrode of the twelfth transistor is electrically connected to the driving output terminal, and a second electrode of the twelfth transistor is electrically connected to the second voltage terminal.

[0342] Optionally, the eighth transistor is a p-type transistor, and the eleventh transistor and the twelfth transistor are n-type transistors; or, the eighth transistor is an n-type transistor, and the eleventh transistor and the twelfth transistor are p-type transistors.

[0343] Optionally the latch circuit includes a thirteenth transistor, a fourteenth transistor, a fifteenth transistor, and a sixteenth transistor;

[0344] a gate electrode of the thirteenth transistor is electrically connected to the driving output terminal, a first electrode of the thirteenth transistor is electrically connected to the intermediate node, and a second electrode of the thirteenth transistor is electrically connected to the second voltage terminal;

[0345] a gate electrode of the fourteenth transistor is electrically connected to the intermediate node, a first electrode of the fourteenth transistor is electrically connected to the driving output terminal, and a second electrode of the fourteenth transistor is electrically connected to the second voltage terminal;

[0346] a gate electrode of the fifteenth transistor is electrically connected to the driving output terminal, a first electrode of the fifteenth transistor is electrically connected to the first output node, and a second electrode of the fifteenth transistor is electrically connected to the intermediate node; and

[0347] a gate electrode of the sixteenth transistor is electrically connected to the intermediate node, a first electrode of the sixteenth transistor is electrically connected to the second output node, and a second electrode of the sixteenth transistor is electrically connected to the driving output terminal.

[0348] Optionally, the thirteenth transistor and the fourteenth transistor are n-type transistors, and the fifteenth transistor and the sixteenth transistor are p-type transistors.

[0349] As shown in FIG. **21**A, based on at least one embodiment of the pixel circuit shown in FIG. **17**:

[0350] The first inverter includes a first transistor T**1** and a second transistor T**2**.

[0351] A gate electrode of the first transistor T**1** is electrically connected to the input terminal of the first inverter, a source electrode of the first transistor T**1** is electrically connected to a high voltage terminal VGH, and a drain electrode of the first transistor T**1** and a source electrode of the second transistor T**2** are both electrically connected to the driving signal output terminal OT.

[0352] A gate electrode of the second transistor T**2** is electrically connected to the input terminal of the first inverter, and a drain electrode of the second transistor T**2** is electrically connected to the low voltage terminal VGL.

[0353] The input terminal of the first inverter is electrically connected to the driving output terminal NT.

[0354] The first transistor T**1** is a p-type transistor, and the second transistor T**2** is an n-type transistor.

[0355] The first data writing circuit includes a fifth transistor T**5** and a first capacitor C**1**.

[0356] A gate electrode of the fifth transistor T**5** is electrically connected to the switch control terminal SW, a source electrode of the fifth transistor T**5** is electrically connected to the first data line SL**1**, and a drain electrode of the fifth transistor T**5** is electrically connected to the first differential control node NC**1**.

[0357] A first terminal of the first capacitor C**1** is electrically connected to the first differential control node NC**1**, and a second terminal of the first capacitor C**1** is electrically connected to the low voltage terminal VGL.

[0358] The input control circuit includes an eighth transistor T**8**, and the differential control circuit includes a ninth transistor T**9** and a tenth transistor T**10**.

[0359] A gate electrode of the eighth transistor T**8** is electrically connected to the output control terminal VCT, a source electrode of the eighth transistor T**8** is electrically connected to the high voltage terminal VGH, and a drain electrode of the eighth transistor T**8** is electrically connected to the input node N**2**.

[0360] A gate electrode of the ninth transistor T**9** is electrically connected to the first differential control node NCT, a source electrode of the ninth transistor T**9** is electrically connected to the input node N**2**, and a drain electrode of the ninth transistor T**9** is electrically connected to the first output node N**3**.

[0361] A gate electrode of the tenth transistor T**10** is electrically connected to the second differential control node NC**2**, a source electrode of the tenth transistor T**10** is electrically connected to the input node N**2**, and a drain electrode of the tenth transistor T**10** is electrically connected to the second output node N**4**; the second differential control node NC**2** is electrically connected to an initial voltage terminal I**1**.

[0362] The set circuit includes an eleventh transistor T**11** and a twelfth transistor T**12**.

[0363] A gate electrode of the eleventh transistor T**11** is electrically connected to the output control terminal VCT, a source electrode of the eleventh transistor T**11** is electrically connected to the intermediate node N**6**, and a source electrode of the eleventh transistor T**11** is electrically connected to the low voltage terminal VGL.

[0364] A gate electrode of the twelfth transistor T**12** is electrically connected to the output control terminal VCT, a source electrode of the twelfth transistor T**12** is electrically connected to the driving output terminal NT, and a drain electrode of the twelfth transistor T**12** is electrically connected to the low voltage terminal VGL.

[0365] The eighth transistor T**8** is a p-type transistor, and the eleventh transistor T**11** and the twelfth transistor T**12** are n-type transistors.

[0366] The latch circuit includes a thirteenth transistor T**13**, a fourteenth transistor T**14**, a fifteenth transistor T**15** and a sixteenth transistor T**16**.

[0367] A gate electrode of the thirteenth transistor T**13** is electrically connected to the driving output terminal NT, a source electrode of the thirteenth transistor T**13** is electrically connected to the intermediate node N**6**, and a drain electrode of the thirteenth transistor T**13** is electrically connected to the low voltage terminal VGL.

[0368] Agate electrode of the fourteenth transistor T**14** is electrically connected to the intermediate node N**6**, a source electrode of the fourteenth transistor T**14** is electrically connected to the driving output terminal NT, and a drain electrode of the fourteenth transistor T**14** is electrically connected to the low voltage terminal VGL.

[0369] A gate electrode of the fifteenth transistor T**15** is electrically connected to the driving output terminal NT, a source electrode of the fifteenth transistor T**15** is electrically connected to the first output node N**3**, and a drain electrode of the fifteenth transistor T**15** is electrically connected to the intermediate node N**6**.

[0370] A gate electrode of the sixteenth transistor T**16** is electrically connected to the intermediate node N**6**, a source electrode of the sixteenth transistor T**16** is electrically connected to the second output node N**4**, and a drain electrode of the sixteenth transistor T**16** is electrically connected to the driving output terminal NT.

[0371] The thirteenth transistor T**13** and the fourteenth transistor T**14** are n-type transistors, and the fifteenth transistor T**15** and the sixteenth transistor T**16** are p-type transistors.

[0372] In at least one embodiment of the present disclosure, the second voltage terminal may be a low voltage terminal, which is not limited thereto.

[0373] In at least one embodiment of the driving circuit shown in FIG. **21**A, T**1**, T**8**, T**9**, T**10**, T**15**, and T**16** are all p-type transistors, and T**2**, T**5**, T**11**, T**12**, T**13**, and T**14** are all n-type transistors.

[0374] FIG. **21**B is an operation timing diagram of at least one embodiment of the driving circuit shown in FIG. **21**A.

[0375] In FIG. **21**B, reference sign F**1** denotes a frame time, reference sign SX denotes a blanking period, and the blanking period is set at the very beginning of the frame time F**1**, and reference sign SD denotes a display period included in the frame time FT.

[0376] FIG. **21**C is an enlarged timing diagram of the blanking period SX in FIG. **21**B.

[0377] As shown in FIG. **21**C, when the driving circuit of at least one embodiment of FIG. **21**A of the present disclosure is in operation, the blanking period includes a first period ST**1**, a second period ST**2**, a third period ST**3** and a fourth period ST**4** which are set successively.

[0378] In the first period ST**1**, the second period ST**2** and the third period ST**3**, VCT provides a high voltage signal, T**11** and T**12** are turned on, the potential of N**6** is a low voltage, NT is connected to VGL, T**15** and T**16** are both turned on, N**3** and N**4** are both connected to VGL, the first inverter formed by T**1** and T**2** inverts the driving output signal provided by NT, and OT outputs a high voltage signal.

[0379] In the first period ST**1**, SW provides a low voltage signal and T**5** is turned off.

[0380] In the second period ST**2**, SW provides a high voltage signal, VCT provides a high voltage signal, T**5** is turned on, and the first data voltage provided by SL**1** is written into NC**1**. Since T**5** is an IGZO (indium gallium zinc oxide) TFT (thin film transistor), it takes a certain time to write the first data voltage into NC**1**.

[0381] In the third period ST**3**, SW provides a low voltage signal, VCT provides a high voltage signal, T**5** is turned off, the time for writing the first data voltage into NC**1** is up, NC**1** is no longer charged, and the potential ofNCl is maintained via C**1**.

[0382] In the fourth period ST**4**, VCT provides a low voltage signal, T**11** and T**12** are turned off, T**8** is turned on, VGH is continuously written into N**2** via T**8**, and I**1** provides an initial voltage Vinit. Since there is a voltage difference between the potential of NC**1** and the voltage value of Vinit, the potential of N**3** is different from the potential of N**4**.

[0383] In the fourth period ST**4**, the potential of NC**1** is greater than the voltage value of Vinit, and the potential of N**3** is less than the potential of N**4**; at the beginning of the fourth period ST**4**, T**15** and T**16** are turned on, the potential of N**6** is less than the potential of NT, T**16** is turned on, NT outputs a high voltage signal, and OT outputs a low voltage signal.

[0384] When the driving circuit of at least one embodiment of FIG. **21**A of the present disclosure is in operation, in the fourth period ST**4**, in a case that the potential of NC**1** is less than the voltage value of Vinit, the potential of N**3** is greater than the potential of N**4**, and at the beginning of the fourth period ST**4**, T**15** and T**16** are turned on, the potential of N**6** is greater than the potential of NT, T**14** is turned on, NT outputs a low voltage signal, and OT outputs a high voltage signal.

[0385] When the driving circuit of at least one embodiment of FIG. **21**A of the present disclosure is in operation, the driving signal output by OT in the display period is the same as the driving signal output by OT in the fourth period ST**4**; OT outputs a low voltage signal in both the fourth period ST**4** and the display period SD; or, OT outputs a high voltage signal in both the fourth period ST**4** and the display period SD.

[0386] In at least one embodiment of the driving circuit shown in FIG. **21**A, T**13**, T**14**, T**15**, and T**16** form a latch, and T**9** and T**10** constitute a differential part.

[0387] The driving circuit in at least one embodiment of the present disclosure can provide a driving signal to a gate electrode of a first control transistor M**9** in a pixel circuit shown in FIG. **21**D via the driving signal output terminal OT.

[0388] As shown in FIG. **21**D, the pixel circuit of at least one embodiment may include a driving transistor M**3**, a first initialization transistor M**1**, a compensation control transistor M**2**, a data writing transistor M**4**, a first light emitting control transistor M**5**, a second light emitting control transistor M**6**, a second initialization transistor M**7**, a third initialization transistor M**8**, a first control transistor M**9**, a storage capacitor Cst, and an organic light emitting diode O**1**.

[0389] Agate electrode of M**5** is electrically connected to a light emitting control line EM, a source electrode of M**5** is electrically connected to a power supply voltage terminal VDD, and a drain electrode of M**5** is electrically connected to a source electrode of M**3**.

[0390] Agate electrode of M**9** is electrically connected to a first control terminal S**0**, a drain electrode of M**9** is electrically connected to a gate electrode of M**3**, a source electrode of M**9** is electrically connected to a drain electrode of M**2**, and a source electrode of M**2** is electrically connected to a drain electrode of M**3**.

[0391] A gate electrode of M**1** is electrically connected to a first reset control terminal RP, a source electrode of M**1** is electrically connected to a first initial voltage terminal I**01**, and a drain electrode of M**1** is electrically connected to the drain electrode of M**3**.

[0392] A gate electrode of M**2** is electrically connected to a compensation control terminal GN.

[0393] A gate electrode of M**4** is electrically connected to a scanning terminal GP, a source electrode of M**4** is electrically connected to a data line DL, and a drain electrode of M**4** is electrically connected to the source electrode of M**3**.

[0394] A gate electrode of M**6** is electrically connected to the light emitting control line EM, a source electrode of M**6** is electrically connected to the drain electrode of M**3**, a drain electrode of M**6** is electrically connected to an anode of **01**; a cathode of O**1** is electrically connected to a low level terminal VSS.

[0395] Agate electrode of M**7** is electrically connected to a second reset control terminal RH, a source electrode of M**7** is electrically connected to a second initial voltage terminal **102**, and a drain electrode of M**7** is electrically connected to the anode of O**1**.

[0396] A gate electrode of M**8** is electrically connected to the second reset control terminal RH, a source electrode of M**8** is electrically connected to a third initial voltage terminal **103**, and a drain electrode of M**8** is electrically connected to the source electrode of M**3**.

[0397] A first terminal of Cst is electrically connected to the gate electrode of M**3**, and a second terminal of Cst is electrically connected to the power supply voltage terminal VDD.

[0398] In at least one embodiment of the pixel circuit shown in FIG. **21**D, M**2** and M**9** are oxide transistors, M**2** and M**9** are n-type transistors, and the other transistors are p-type transistors.

[0399] When the pixel circuit of at least one embodiment of FIG. **21**D is in operation, in a display period included in a frame time, in a case that OT outputs a high voltage signal, M**9** is turned on, and the pixel circuit is refreshed normally; in the display period, in a case that OT outputs a low voltage signal, M**9** is turned off, and the pixel circuit is not refreshed.

[0400] As shown in FIG. **22**A, based on at least one embodiment of the pixel circuit shown in FIG. **18**:

[0401] The inverting circuit includes a first inverter and a second inverter; the first inverter includes a first transistor T**1** and a second transistor T**2**; the second inverter includes a third transistor T**3** and a fourth transistor T**4**.

[0402] A gate electrode of the first transistor T**1** is electrically connected to the input terminal of the first inverter, a source electrode of the first transistor T**1** is electrically connected to the high voltage terminal VGH, and a drain electrode of the first transistor T**1** and a source electrode of the second transistor T**2** are both electrically connected to the input terminal of the second inverter.

[0403] A gate electrode of the second transistor T**2** is electrically connected to the input terminal of the first inverter, and a drain electrode of the second transistor T**2** is electrically connected to the low voltage terminal.

[0404] A gate electrode of the third transistor T**3** and a gate electrode of the fourth transistor T**4** are both electrically connected to the input terminal of the second inverter, a source electrode of the third transistor T**3** is electrically connected to the high voltage terminal VGH, and a drain electrode of the third transistor T**3** and a source electrode of the fourth transistor T**4** are both electrically connected to the driving signal output terminal OT.

[0405] A drain electrode of the fourth transistor T**4** is electrically connected to the low voltage terminal VGL.

[0406] The first transistor T**1** is a p-type transistor, the second transistor T**2** is an n-type transistor; the third transistor T**3** is a p-type transistor, and the fourth transistor T**4** is an n-type transistor.

[0407] The input terminal of the first inverter is electrically connected to the driving output terminal NT.

[0408] The first data writing circuit includes a fifth transistor T**5** and a first capacitor C**1**.

[0409] A gate electrode of the fifth transistor T**5** is electrically connected to the switch control terminal SW, a source electrode of the fifth transistor T**5** is electrically connected to the first data line SL**1**, and a drain electrode of the fifth transistor T**5** is electrically connected to the first differential control node NC**1**.

[0410] A first terminal of the first capacitor C**1** is electrically connected to the first differential control node NC**1**, and a second terminal of the first capacitor C**1** is electrically connected to the low voltage terminal VGL.

[0411] The input control circuit includes an eighth transistor T**8**, and the differential control circuit includes a ninth transistor T**9** and a tenth transistor T**10**.

[0412] A gate electrode of the eighth transistor T**8** is electrically connected to the output control terminal VCT, a source electrode of the eighth transistor T**8** is electrically connected to the high voltage terminal VGH, and a drain electrode of the eighth transistor T**8** is electrically connected to the input node N**2**.

[0413] A gate electrode of the ninth transistor T**9** is electrically connected to the first differential control node NC**1**, a source electrode of the ninth transistor T**9** is electrically connected to the input node N**2**, and a drain electrode of the ninth transistor T**9** is electrically connected to the first output node N**3**.

[0414] A gate electrode of the tenth transistor T**10** is electrically connected to the second differential control node NC**2**, a source electrode of the tenth transistor T**10** is electrically connected to the input node N**2**, and a drain

electrode of the tenth transistor T10 is electrically connected to the second output node N4; the second differential control node NC2 is electrically connected to the initial voltage terminal I1.

[0415] The set circuit includes an eleventh transistor TI1 and a twelfth transistor T12.

[0416] A gate electrode of the eleventh transistor T11 is electrically connected to the output control terminal VCT, a source electrode of the eleventh transistor T11 is electrically connected to the low voltage terminal VGL.

[0417] A gate electrode of the twelfth transistor T12 is electrically connected to the output control terminal VCT, a source electrode of the twelfth transistor T12 is electrically connected to the driving output terminal NT, and a drain electrode of the twelfth transistor T12 is electrically connected to the low voltage terminal VGL.

[0418] The eighth transistor T8 is a p-type transistor, and the eleventh transistor T11 and the twelfth transistor T12 are n-type transistors.

[0419] The latch circuit includes a thirteenth transistor T13, a fourteenth transistor T14, a fifteenth transistor T15 and a sixteenth transistor T16.

[0420] A gate electrode of the thirteenth transistor T13 is electrically connected to the driving output terminal NT, a source electrode of the thirteenth transistor T13 is electrically connected to the intermediate node N6, and a drain electrode of the thirteenth transistor T13 is electrically connected to the low voltage terminal VGL.

[0421] Agate electrode of the fourteenth transistor T14 is electrically connected to the intermediate node N6, a source electrode of the fourteenth transistor T14 is electrically connected to the driving output terminal NT, and a drain electrode of the fourteenth transistor T14 is electrically connected to the low voltage terminal VGL.

[0422] A gate electrode of the fifteenth transistor T15 is electrically connected to the driving output terminal NT, a source electrode of the fifteenth transistor T15 is electrically connected to the first output node N3, and a drain electrode of the fifteenth transistor T15 is electrically connected to the intermediate node N6.

[0423] A gate electrode of the sixteenth transistor T16 is electrically connected to the intermediate node N6, a source electrode of the sixteenth transistor T16 is electrically connected to the second output node N4, and a drain electrode of the sixteenth transistor T16 is electrically connected to the driving output terminal OT.

[0424] The thirteenth transistor T13 and the fourteenth transistor T14 are n-type transistors, and the fifteenth transistor T15 and the sixteenth transistor T16 are p-type transistors.

[0425] In at least one embodiment shown in FIG. 22A, T1, T3, T8, T9, T10, T15, and T16 are all p-type transistors, and T2, T4, T5, T11, T12, T13, and T14 are all n-type transistors.

[0426] In at least one embodiment of the driving circuit shown in FIG. 22A, T1 and T2 form the first inverter, T3 and T4 form the second inverter, and T1, T2, T3, and T4 may be configured to amplify and stabilize the driving output signal, and output the driving signal.

[0427] FIG. 22B is an operation timing diagram of at least one embodiment of the driving circuit shown in FIG. 22A.

[0428] In FIG. 22B, reference sign F1 denotes a frame time, reference sign SX denotes a blanking period, the blanking period SX is set at the very beginning of the frame time F1, and reference sign SD denotes a display period included in the frame time FT.

[0429] As shown in FIG. 22C, when the driving circuit of at least one embodiment of FIG. 22A of the present disclosure is in operation, the blanking period includes a first period ST1, a second period ST2, a third period ST3 and a fourth period ST4 which are set successively.

[0430] In the first period ST1, the second period ST2 and the third period ST3, VCT provides a high voltage signal, T11 and T12 are turned on, NT outputs a low voltage signal, and after passing through two phases of inverters, OT outputs a low voltage signal.

[0431] In the first period ST1, SW provides a low voltage signal, and T5 is turned off.

[0432] In the second period ST2, SW provides a high voltage signal, VCT provides a high voltage signal, T5 is turned on, and the first data voltage provided by SL1 is written into NC1. Since T5 is an IGZO TFT (thin film transistor), it takes a certain time to write the first data voltage into NC1.

[0433] In the third period ST3, SW provides a low voltage signal, VCT provides a high voltage signal, T5 is turned off, the time for writing the first data voltage into NC1 is up, NC1 is no longer charged, and the potential of NC1 is maintained via C1.

[0434] In the fourth period ST4, VCT provides a low voltage signal, T11 and T12 are turned off, T8 is turned on, VGH is continuously written into N2 via T8, I1 provides an initial voltage Vinit. Since there is a voltage difference between the potential of NC1 and the voltage value of Vinit, there is a difference between the potential of the gate electrode of T9 and the potential of the gate electrode of T10, resulting in a difference in voltage writing speeds or voltage values of the first output node N3 and the second output node N4.

[0435] In the fourth period ST4, the potential of NC1 is greater than the voltage value of Vinit, and the potential of N3 is less than the potential of N4; at the beginning of the fourth period ST4, T15 and T16 are turned on, the potential of N6 is less than the potential of NT, T16 is turned on, NT outputs a high voltage signal, and OT outputs a high voltage signal.

[0436] When the driving circuit of at least one embodiment of FIG. 22A of the present disclosure is in operation, in the fourth period ST4, in a case that the potential of NC1 is less than the voltage value of Vinit, the potential of N3 is greater than the potential of N4, and at the beginning of the fourth period ST4, T15 and T16 are turned on, the potential of N6 is greater than the potential of NT, T14 is turned on, NT outputs a low voltage signal, and OT outputs a low voltage signal.

[0437] When the driving circuit of at least one embodiment of FIG. 22A of the present disclosure is in operation, the driving signal output by OT in the display period is the same as the driving signal output by OT in the fourth period ST4; OT outputs a low voltage signal in both the fourth period ST4 and the display period SD; or, OT outputs a high voltage signal in both the fourth period ST4 and the display period SD.

[0438] In at least one embodiment of the driving circuit shown in FIG. 22A, T13, T14, T15, and T16 form a latch, and T9 and T10 form a differential part.

[0439] When the driving circuit of at least one embodiment of FIGS. 21A and 22A of the present disclosure is in

operation, in the blanking period in each frame time, in a case that the output control signal provided by VCT is being set high, it causes the driving output signal output by NT to have either a pull-down signal or a pull-up signal with the same pulse width as the output control signal provided by VCT, and the driving signal output by OT will also be disturbed.

[0440] When the pixel circuit of at least one embodiment of FIG. **21**D is in operation, in a case that OT outputs a high voltage signal, M**9** is in an on state, and in a case that OT outputs a low voltage signal, M**9** is in an off state. There is capacitance between the gate electrode and drain electrode of M**9**, the capacitance mainly includes: the parasitic capacitance of M**9** itself; and the capacitance between nodes other than those of the TFTs in the Layout design; where the capacitance between nodes other than those of the TFTs can be optimized in the design to minimize it as much as possible, but the capacitance of M**9** itself is inevitable in the TFT itself and can not be completely eliminated, with a capacitance value in the order of fF, which is considered a large capacitance among capacitances between nodes at the pixel level.

[0441] In a case that the light emitting control signal provided by the light emitting control line EM adopts multiple pulses in the display period, as shown in FIG. **22**D, the display panel including the pixel circuit of at least one embodiment of FIG. **21**D includes multiple row light emitting control lines, and in the display period SD, each row light emitting control line outputs a corresponding light emitting control signal, and each light emitting control signal has three upward pulses.

[0442] In the blanking period SX, the light emitting control signals provided by some of the light emitting control lines have rising edges.

[0443] In FIG. **22**D, reference sign EM**1** denotes a first row light emitting control line, reference sign EM**2** denotes a second row light emitting control line, reference sign EM**3** denotes a third row light emitting control line, reference sign EM**4** denotes a fourth row light emitting control line, reference sign EMN-**3** denotes an (N-3)-th row light emitting control line, reference sign EMN-**2** denotes an (N-2)-th row light emitting control line, reference sign EMN-**1** denotes an (N-1)-th row light emitting control line, and reference sign EMN denotes an N-th row light emitting control line; N is an integer greater than 7.

[0444] As shown in FIG. **22**D, in the blanking period SX, the (N-3)-th row light control signal provided by EMN-**3**, the (N-2)-th row light control signal provided by EMN-**2**, the (N-1)-th row light control signal provided by EMN-**1**, and the N-th row light control signal provided by EMN-**1** have rising edges.

[0445] In the blanking period, there is a pull-down signal in the driving signal output by OT. In the pixel circuit, there is a capacitance between the gate electrode of M**9** and the gate electrode of the driving transistor M**3**. The pull-down signal of the driving signal has a coupling effect on the potential of the gate electrode of M**3**, thereby lowering the potential of the gate electrode of M**3**. When the light emitting control line outputs multiple pulses, some row light emitting control signals are in the off state in the blanking period, most of the light emitting control signals remain in the on state in the blanking period, and the organic light emitting diodes in the pixel circuits are in the light emitting stage. In this case, the change in the potential of the gate electrode of the driving transistor M**3** has different effects on the light emitting of the pixel circuits corresponding to these two types of rows, causing brightness differences in different regions, which results in a multi-screen artifacts.

[0446] In view of the above problems, optimization solutions can be divided into two categories: one is to reduce the capacitance between the gate electrode of M**9** and the gate electrode of the driving transistor M**3**, and reduce the coupling effect of the disturbance of the driving signal on the gate electrode of M**3**; the other is to start from the driving circuit that generates the driving signal, which stabilize the driving signal output by the driving circuit. At least one embodiment of the present disclosure provides a driving circuit adopting a switch control circuit. The switch control circuit controls connection or disconnection between a first output control node and a second output control node under control of an on-off control signal provided by an on-off control terminal VCT**2**, so that a driving signal output by a driving signal output terminal OT is not affected by an output control signal provided by VCT.

[0447] In a specific implementation, in the blanking period, a pulse width of the on-off control signal provided by VCT**2** is greater than a pulse width of the output control signal provided by VCT, a start time of an effective period of the on-off control signal is earlier than a start time of an effective period of the output control signal, and an end time of the effective period of the on-off control signal is later than an end time of the effective period of the output control signal.

[0448] In at least one embodiment of the present disclosure, the effective period of the on-off control signal refers to: a period during which the on-off control signal is an active voltage signal.

[0449] The effective period of the output control signal refers to: a period during which the output control signal is an active voltage signal.

[0450] When the transistor controlled by the on-off control signal is an n-type transistor, the active voltage signal is a high voltage signal, and when the transistor controlled by the on-off control signal is a p-type transistor, the active voltage signal is a low voltage signal.

[0451] When the transistor controlled by the output control signal is an n-type transistor, the active voltage signal is a high voltage signal, and when the transistor controlled by the output control signal is a p-type transistor, the active voltage signal is a low voltage signal.

[0452] The difference between the driving circuit of at least one embodiment of FIG. **23**A and the driving circuit of at least one embodiment of FIG. **22**A is as follows:

[0453] a switch control circuit is further included;

[0454] the switch control circuit includes a seventh transistor T**7**;

[0455] a gate electrode of the seventh transistor T**7** is electrically connected to the on-off control terminal VCT**2**, a source electrode of the seventh transistor T**7** is electrically connected to the driving output terminal NT, and a drain electrode of the seventh transistor T**7** is electrically connected to the gate electrode of T**1**.

[0456] In at least one embodiment of the driving circuit shown in FIG. **23**A, T**7** is a p-type transistor, and T**7** is an LTPS (low-temperature polysilicon) transistor.

[0457] As shown in FIG. **23**B, when the driving circuit of at least one embodiment of FIG. **23**A of the present disclosure is in operation, a frame time includes a blanking period

SX, the blanking period includes an off phase SG, and the off phase SG includes a setting period SZ.

[0458] In the setting period SZ, VCT provides a high voltage signal, T11 and T12 are turned on, N6 is connected to VGL, and NT is connected to VGL.

[0459] In the off phase SG, VCT2 provides a high voltage signal, and T7 is turned off, so that the driving signal provided by OT is not affected by the output control signal provided by VCT.

[0460] In at least one embodiment of the present disclosure, the switch control circuit is additionally provided, the switch control circuit includes the seventh transistor, and the seventh transistor is an isolation TFT (thin film transistor) for isolating changes in the driving output signal caused by signal jumps in each frame in the driving circuit, thereby improving stability of the driving signal and improving display effect of the OLED (organic light emitting diode) display product.

[0461] FIG. **23**C is an operation timing diagram of at least one embodiment of the driving circuit shown in FIG. **23**B.

[0462] In FIG. **23**C, reference sign F1 denotes a frame time, reference sign SX denotes a blanking period, the blanking period SX is set at the very beginning of the frame time F1, and reference sign SD denotes a display period included in the frame time F1.

[0463] As shown in FIG. **23**D, when the driving circuit of at least one embodiment of FIG. **23**A of the present disclosure is in operation, the blanking period includes a first period ST1, a second period ST2, a third period ST3 and a fourth period ST4 which are set successively.

[0464] In the first period ST1, the second period ST2 and the third period ST3, VCT provides a high voltage signal, T11 and T12 are turned on, N6 and NT are connected to VGL, T15 and T16 are turned on, NT outputs a low voltage signal, T7 is turned off, and OT maintains outputting a high voltage signal.

[0465] In the first period ST1, SW provides a low voltage signal and T5 is turned off.

[0466] In the second period ST2, SW provides a high voltage signal, VCT provides a high voltage signal, T5 is turned on, and the first data voltage provided by SL1 is written into NC1. Since T5 is an IGZO TFT (thin film transistor), it takes a certain time to write the first data voltage into NC1.

[0467] In the third period ST3, SW provides a low voltage signal, VCT provides a high voltage signal, T5 is turned off, the time for writing the first data voltage into NC1 is up, NC1 is no longer charged, and the potential of NC1 is maintained via C1.

[0468] In the fourth period ST4, VCT provides a low voltage signal, T11 and T12 are turned off, T8 is turned on, VGH is continuously written into N2 via T8, and I1 provides an initial voltage Vinit. Since there is a voltage difference between the potential of NC1 and the voltage value of Vinit, the potential of N3 is different from the potential of N4.

[0469] In the fourth period ST4, VCT2 provides a low voltage signal and T7 is turned on.

[0470] In the fourth period ST4, the potential of NC1 is greater than the voltage value of Vinit, and the potential of N3 is less than the potential of N4; at the beginning of the fourth period ST4, T15 and T16 are turned on, the potential of N6 is less than the potential of NT, T16 is turned on, NT outputs a high voltage signal, and OT outputs a high voltage signal.

[0471] When the driving circuit of at least one embodiment of FIG. **23**A of the present disclosure is in operation, in the fourth period ST4, in a case that the potential of NC1 is less than the voltage value of Vinit, the potential of N3 is greater than the potential of N4, and at the beginning of the fourth period ST4, T15 and T16 are turned on, the potential of N6 is greater than the potential of NT, T14 is turned on, NT outputs a low voltage signal, and OT outputs a low voltage signal.

[0472] The difference between the driving circuit of at least one embodiment of FIG. **24** and the driving circuit of at least one embodiment of FIG. **22**A is as follows:

[0473] a switch control circuit is included;

[0474] the switch control circuit includes a seventh transistor T7;

[0475] a gate electrode of the seventh transistor T7 is electrically connected to the on-off control terminal VCT2, a source electrode of the seventh transistor T7 is electrically connected to the drain electrode of T1, and a drain electrode of the seventh transistor T7 is electrically connected to the gate electrode of T3.

[0476] In at least one embodiment of the driving circuit shown in FIG. **24**, T7 is a p-type transistor, and T7 is an LTPS (low-temperature polysilicon) transistor.

[0477] As shown in FIG. **23**B, when the driving circuit of at least one embodiment of FIG. **24** of the present disclosure is in operation, a frame time includes a blanking period SX, the blanking period includes an off phase SG, and the off phase SG includes a setting period SZ.

[0478] In the setting period SZ, VCT provides a high voltage signal, T11 and T12 are turned on, N6 is connected to VGL, and NT is connected to VGL.

[0479] In the off phase SG, VCT2 provides a high voltage signal, and T7 is turned off, so that the driving signal provided by OT is not affected by the output control signal provided by VCT.

[0480] The difference between the driving circuit of at least one embodiment of FIG. **25** and the driving circuit of at least one embodiment of FIG. **22**A is as follows:

[0481] a switch control circuit is further included;

[0482] the switch control circuit includes a seventh transistor T7;

[0483] a gate electrode of the seventh transistor T7 is electrically connected to the on-off control terminal VCT2, a source electrode of the seventh transistor T7 is electrically connected to a drain electrode of T3, and a drain electrode of the seventh transistor T7 is electrically connected to the driving signal output terminal OT.

[0484] In at least one embodiment of the driving circuit shown in FIG. **25**, T7 is a p-type transistor, and T7 is an LTPS (low-temperature polysilicon) transistor.

[0485] As shown in FIG. **23**B, when the driving circuit of at least one embodiment of FIG. **25** of the present disclosure is in operation, a frame time includes a blanking period SX, the blanking period includes an off phase SG, and the off phase SG includes a setting period SZ.

[0486] In the setting period SZ, VCT provides a high voltage signal, T11 and T12 are turned on, N6 is connected to VGL, and NT is connected to VGL.

[0487] In the off phase SG, VCT2 provides a high voltage signal, and T7 is turned off, so that the driving signal provided by OT is not affected by the output control signal provided by VCT.

[0488] The difference between the driving circuit of at least one embodiment of FIG. **26**A and the driving circuit of at least one embodiment of FIG. **22**A is as follows:

[0489] a switch control circuit is further included;

[0490] the switch control circuit includes a seventh transistor T**7**;

[0491] a gate electrode of the seventh transistor T**7** is electrically connected to the on-off control terminal VCT**2**, a source electrode of the seventh transistor T**7** is electrically connected to the driving output terminal NT, and a drain electrode of the seventh transistor T**7** is electrically connected to the gate electrode of T**1**.

[0492] In the driving circuit of at least one embodiment of FIG. **26**A, T**7** is an n-type transistor, and T**7** is an IGZO (indium gallium zinc oxide) transistor.

[0493] As shown in FIG. **26**B, when the driving circuit of at least one embodiment of FIG. **26**A of the present disclosure is in operation, a frame time includes a blanking period SX, the blanking period includes an off phase SG, and the off phase SG includes a setting period SZ.

[0494] In the setting period SZ, VCT provides a high voltage signal, T**11** and T**12** are turned on, N**6** is connected to VGL, and NT is connected to VGL.

[0495] In the off phase SG, VCT**2** provides a low voltage signal, and T**7** is turned off, so that the driving signal provided by OT is not affected by the output control signal provided by VCT.

[0496] The difference between the driving circuit of at least one embodiment of FIG. **27** and the driving circuit of at least one embodiment of FIG. **22**A is as follows:

[0497] a switch control circuit is further included;

[0498] the switch control circuit includes a seventh transistor T**7**;

[0499] a gate electrode of the seventh transistor T**7** is electrically connected to the on-off control terminal VCT**2**, a source electrode of the seventh transistor T**7** is electrically connected to the drain electrode of T**1**, and a drain electrode of the seventh transistor T**7** is electrically connected to the gate electrode of T**3**.

[0500] In at least one embodiment of the driving circuit shown in FIG. **27**, T**7** is an n-type transistor, and T**7** is an IGZO (indium gallium zinc oxide) transistor.

[0501] As shown in FIG. **26**B, when the driving circuit of at least one embodiment of FIG. **27** of the present disclosure is in operation, a frame time includes a blanking period SX, the blanking period includes an off phase SG, and the off phase SG includes a setting period SZ.

[0502] In the setting period SZ, VCT provides a high voltage signal, T**11** and T**12** are turned on, N**6** is connected to VGL, and NT is connected to VGL.

[0503] In the off phase SG, VCT**2** provides a low voltage signal, and T**7** is turned off, so that the driving signal provided by OT is not affected by the output control signal provided by VCT.

[0504] The difference between the driving circuit of at least one embodiment of FIG. **28** and the driving circuit of at least one embodiment of FIG. **22**A is as follows:

[0505] a switch control circuit is further included;

[0506] the switch control circuit includes a seventh transistor T**7**;

[0507] a gate electrode of the seventh transistor T**7** is electrically connected to the on-off control terminal VCT**2**, a source electrode of the seventh transistor T**7** is electrically connected to the drain electrode of T**3**, and a drain electrode of the seventh transistor T**7** is electrically connected to the driving signal output terminal OT.

[0508] In at least one embodiment of the driving circuit shown in FIG. **28**, T**7** is an n-type transistor, and T**7** is an IGZO (indium gallium zinc oxide) transistor.

[0509] As shown in FIG. **26**B, when the driving circuit of at least one embodiment of FIG. **28** of the present disclosure is in operation, a frame time includes a blanking period SX, the blanking period includes an off phase SG, and the off phase SG includes a setting period SZ.

[0510] In the setting period SZ, VCT provides a high voltage signal, T**11** and T**12** are turned on, N**6** is connected to VGL, and NT is connected to VGL.

[0511] In the off phase SG, VCT**2** provides a low voltage signal, and T**7** is turned off, so that the driving signal provided by OT is not affected by the output control signal provided by VCT.

[0512] The difference between the driving circuit of at least one embodiment of FIG. **29**A and the driving circuit of at least one embodiment of FIG. **21**A is as follows:

[0513] a switch control circuit is further included;

[0514] the switch control circuit includes a seventh transistor T**7**;

[0515] a gate electrode of the seventh transistor T**7** is electrically connected to the on-off control terminal VCT**2**, a source electrode of the seventh transistor T**7** is electrically connected to the driving output terminal NT, and a drain electrode of the seventh transistor T**7** is electrically connected to the gate electrode of T**1**.

[0516] In at least one embodiment of the driving circuit shown in FIG. **29**A, T**7** is a p-type transistor, and T**7** is an LTPS (low-temperature polysilicon) transistor.

[0517] As shown in FIG. **29**B, when the driving circuit of at least one embodiment of FIG. **29**A of the present disclosure is in operation, a frame time includes a blanking period SX, the blanking period includes an off phase SG, and the off phase SG includes a setting period SZ.

[0518] In the setting period SZ, VCT provides a high voltage signal, T**11** and T**12** are turned on, N**6** is connected to VGL, and NT is connected to VGL.

[0519] In the off phase SG, VCT**2** provides a high voltage signal, and T**7** is turned off, so that the driving signal provided by OT is not affected by the output control signal provided by VCT.

[0520] The difference between the driving circuit of at least one embodiment of FIG. **30** and the driving circuit of at least one embodiment of FIG. **21**A is as follows:

[0521] a switch control circuit is further included;

[0522] the switch control circuit includes a seventh transistor T**7**;

[0523] a gate electrode of the seventh transistor T**7** is electrically connected to the on-off control terminal VCT**2**, a source electrode of the seventh transistor T**7** is electrically connected to the drain electrode of T**1**, and a drain electrode of the seventh transistor T**7** is electrically connected to the driving signal output terminal OT.

[0524] In at least one embodiment of the driving circuit shown in FIG. **30**, T**7** is a p-type transistor, and T**7** is an LTPS (low-temperature polysilicon) transistor.

[0525] As shown in FIG. **29**B, when the driving circuit of at least one embodiment of FIG. **30** of the present disclosure is in operation, a frame time includes a blanking period SX,

the blanking period includes an off phase SG, and the off phase SG includes a setting period SZ.

[0526] In the setting period SZ, VCT provides a high voltage signal, T**11** and T**12** are turned on, N**6** is connected to VGL, and NT is connected to VGL.

[0527] In the off phase SG, VCT**2** provides a high voltage signal, and T**7** is turned off, so that the driving signal provided by OT is not affected by the output control signal provided by VCT.

[0528] The difference between the driving circuit of at least one embodiment of FIG. **31**A and the driving circuit of at least one embodiment of FIG. **21**A is as follows:

[0529] a switch control circuit is further included;

[0530] the switch control circuit includes a seventh transistor T**7**;

[0531] a gate electrode of the seventh transistor T**7** is electrically connected to the on-off control terminal VCT**2**, a source electrode of the seventh transistor T**7** is electrically connected to the driving output terminal NT, and a drain electrode of the seventh transistor T**7** is electrically connected to the gate electrode of T**1**.

[0532] In at least one embodiment of the driving circuit shown in FIG. **31**A, T**7** is an n-type transistor, and T**7** is an IGZO (indium gallium zinc oxide) transistor.

[0533] As shown in FIG. **31**B, when the driving circuit of at least one embodiment of FIG. **31**A of the present disclosure is in operation, a frame time includes a blanking period SX, the blanking period includes an off phase SG, and the off phase SG includes a setting period SZ.

[0534] In the setting period SZ, VCT provides a high voltage signal, T**11** and T**12** are turned on, N**6** is connected to VGL, and NT is connected to VGL.

[0535] In the off phase SG, VCT**2** provides a low voltage signal, and T**7** is turned off, so that the driving signal provided by OT is not affected by the output control signal provided by VCT.

[0536] The difference between the driving circuit of at least one embodiment of FIG. **32** and the driving circuit of at least one embodiment of FIG. **21**A is as follows:

[0537] a switch control circuit is further included;

[0538] the switch control circuit includes a seventh transistor T**7**;

[0539] a gate electrode of the seventh transistor T**7** is electrically connected to the on-off control terminal VCT**2**, a source electrode of the seventh transistor T**7** is electrically connected to the drain electrode of T**1**, and a drain electrode of the seventh transistor T**7** is electrically connected to the driving signal output terminal OT.

[0540] In at least one embodiment of the driving circuit shown in FIG. **32**, T**7** is an n-type transistor, and T**7** is an IGZO (indium gallium zinc oxide) transistor.

[0541] As shown in FIG. **31**B, when the driving circuit of at least one embodiment of FIG. **32** of the present disclosure is in operation, a frame time includes a blanking period SX, the blanking period includes an off phase SG, and the off phase SG includes a setting period SZ.

[0542] In the setting period SZ, VCT provides a high voltage signal, T**11** and T**12** are turned on, N**6** is connected to VGL, and NT is connected to VGL.

[0543] In the off phase SG, VCT**2** provides a low voltage signal, and T**7** is turned off, so that the driving signal provided by OT is not affected by the output control signal provided by VCT.

[0544] The difference between the driving circuit of at least one embodiment of FIG. **33** and the driving circuit of at least one embodiment of FIG. **21**A is as follows: a second data writing circuit is further included;

[0545] the second data writing circuit includes a sixth transistor T**6** and a second capacitor C**2**;

[0546] a gate electrode of the sixth transistor T**6** is electrically connected to the switch control terminal SW, a source electrode of the sixth transistor T**6** is electrically connected to the second data line SL**2**, and a drain electrode of the sixth transistor T**6** is electrically connected to the second differential control node NC**2**;

[0547] a first terminal of the second capacitor C**2** is electrically connected to the second differential control node NC**2**, and a second terminal of the second capacitor C**2** is electrically connected to the low voltage terminal VGL.

[0548] In at least one embodiment of the driving circuit shown in FIGS. **33** to **44**, T**6** is an n-type transistor.

[0549] In at least one embodiment of the driving circuit shown in FIGS. **33** to **44** of the present disclosure, in a case that SW provides a high voltage signal, the first data voltage provided by SL**1** is written into NC**1**, the second data voltage provided by SL**2** is written into NC**2**, the potential of NC**1** and the potential of NC**2** are differentiated, the first data voltage provided by SL**1** is a low voltage signal, and the second data voltage provided by SL**2** is a high voltage signal; or, the first data voltage provided by SL**1** is a high voltage signal, and the second data voltage provided by SL**2** is a low voltage signal. For example, the first data voltage is a 7V voltage signal, and the second data voltage is a OV voltage signal; or, the first data voltage is a OV voltage signal, and the second data voltage is a 7V voltage signal. When one of the first data voltage and the second data voltage is high and the other is low, T**15** and T**16** can achieve better differential functionality. There is a relatively large difference between the potential of the first differential control node NC**1** and the potential of the second differential control node NC**2**, therefore, for the driving circuit of at least one embodiment of FIGS. **21**A and **22**A, the differential effect of T**15** and T**16** is more significant, and the margin of the driving circuit is larger.

[0550] In at least one embodiment of the driving circuit shown in FIGS. **33** to **44**, since the driving circuit requires the simultaneous use of data voltages from two adjacent data lines, the partial refresh control resolution in the column direction is relatively high; a single stage of driving circuit can drive two adjacent rows of pixel circuits.

[0551] The difference between the driving circuit of at least one embodiment of FIG. **34** and the driving circuit of at least one embodiment of FIG. **22**A is as follows: a second data writing circuit is further included;

[0552] the second data writing circuit includes a sixth transistor T**6** and a second capacitor C**2**;

[0553] a gate electrode of the sixth transistor T**6** is electrically connected to the switch control terminal SW, a source electrode of the sixth transistor T**6** is electrically connected to the second data line SL**2**, and a drain electrode of the sixth transistor T**6** is electrically connected to the second differential control node NC**2**;

[0554] a first terminal of the second capacitor C**2** is electrically connected to the second differential control

node NC2, and a second terminal of the second capacitor C2 is electrically connected to the low voltage terminal VGL.

[0555] Optionally, the second voltage terminal may be a low voltage terminal.

[0556] The difference between the driving circuit of at least one embodiment of FIG. 35 and the driving circuit of at least one embodiment of FIG. 23A is as follows: a second data writing circuit is further included;

[0557] the second data writing circuit includes a sixth transistor T6 and a second capacitor C2;

[0558] a gate electrode of the sixth transistor T6 is electrically connected to the switch control terminal SW, a source electrode of the sixth transistor T6 is electrically connected to the second data line SL2, and a drain electrode of the sixth transistor T6 is electrically connected to the second differential control node NC2;

[0559] a first terminal of the second capacitor C2 is electrically connected to the second differential control node NC2, and a second terminal of the second capacitor C2 is electrically connected to the low voltage terminal VGL.

[0560] The difference between the driving circuit of at least one embodiment of FIG. 36 and the driving circuit of at least one embodiment of FIG. 24 is as follows: a second data writing circuit is further included;

[0561] the second data writing circuit includes a sixth transistor T6 and a second capacitor C2;

[0562] a gate electrode of the sixth transistor T6 is electrically connected to the switch control terminal SW, a source electrode of the sixth transistor T6 is electrically connected to the second data line SL2, and a drain electrode of the sixth transistor T6 is electrically connected to the second differential control node NC2;

[0563] a first terminal of the second capacitor C2 is electrically connected to the second differential control node NC2, and a second terminal of the second capacitor C2 is electrically connected to the low voltage terminal VGL.

[0564] The difference between the driving circuit of at least one embodiment of FIG. 37 and the driving circuit of at least one embodiment of FIG. 25 is as follows: a second data writing circuit is further included;

[0565] the second data writing circuit includes a sixth transistor T6 and a second capacitor C2;

[0566] a gate electrode of the sixth transistor T6 is electrically connected to the switch control terminal SW, a source electrode of the sixth transistor T6 is electrically connected to the second data line SL2, and a drain electrode of the sixth transistor T6 is electrically connected to the second differential control node NC2;

[0567] a first terminal of the second capacitor C2 is electrically connected to the second differential control node NC2, and a second terminal of the second capacitor C2 is electrically connected to the low voltage terminal VGL.

[0568] The difference between the driving circuit of at least one embodiment of FIG. 38 and the driving circuit of at least one embodiment of FIG. 26A is as follows: a second data writing circuit is further included;

[0569] the second data writing circuit includes a sixth transistor T6 and a second capacitor C2;

[0570] a gate electrode of the sixth transistor T6 is electrically connected to the switch control terminal SW, a source electrode of the sixth transistor T6 is electrically connected to the second data line SL2, and a drain electrode of the sixth transistor T6 is electrically connected to the second differential control node NC2;

[0571] a first terminal of the second capacitor C2 is electrically connected to the second differential control node NC2, and a second terminal of the second capacitor C2 is electrically connected to the low voltage terminal VGL.

[0572] The difference between the driving circuit of at least one embodiment of FIG. 39 and the driving circuit of at least one embodiment of FIG. 27 is as follows: a second data writing circuit is further included;

[0573] the second data writing circuit includes a sixth transistor T6 and a second capacitor C2;

[0574] a gate electrode of the sixth transistor T6 is electrically connected to the switch control terminal SW, a source electrode of the sixth transistor T6 is electrically connected to the second data line SL2, and a drain electrode of the sixth transistor T6 is electrically connected to the second differential control node NC2;

[0575] a first terminal of the second capacitor C2 is electrically connected to the second differential control node NC2, and a second terminal of the second capacitor C2 is electrically connected to the low voltage terminal VGL.

[0576] The difference between the driving circuit of at least one embodiment of FIG. 40 and the driving circuit of at least one embodiment of FIG. 28 is as follows: a second data writing circuit is further included;

[0577] the second data writing circuit includes a sixth transistor T6 and a second capacitor C2;

[0578] a gate electrode of the sixth transistor T6 is electrically connected to the switch control terminal SW, a source electrode of the sixth transistor T6 is electrically connected to the second data line SL2, and a drain electrode of the sixth transistor T6 is electrically connected to the second differential control node NC2;

[0579] a first terminal of the second capacitor C2 is electrically connected to the second differential control node NC2, and a second terminal of the second capacitor C2 is electrically connected to the low voltage terminal VGL.

[0580] The difference between the driving circuit of at least one embodiment of FIG. 41 and the driving circuit of at least one embodiment of FIG. 29A is as follows: a second data writing circuit is further included;

[0581] the second data writing circuit includes a sixth transistor T6 and a second capacitor C2;

[0582] a gate electrode of the sixth transistor T6 is electrically connected to the switch control terminal SW, a source electrode of the sixth transistor T6 is electrically connected to the second data line SL2, and a drain electrode of the sixth transistor T6 is electrically connected to the second differential control node NC2;

[0583] a first terminal of the second capacitor C2 is electrically connected to the second differential control node NC2, and a second terminal of the second capacitor C2 is electrically connected to the low voltage terminal VGL.

[0584] The difference between the driving circuit of at least one embodiment of FIG. 42 and the driving circuit of at least one embodiment of FIG. 30 is as follows: a second data writing circuit is further included;

[0585] the second data writing circuit includes a sixth transistor T6 and a second capacitor C2;

[0586] a gate electrode of the sixth transistor T6 is electrically connected to the switch control terminal SW, a source electrode of the sixth transistor T6 is electrically connected to the second data line SL2, and a drain electrode of the sixth transistor T6 is electrically connected to the second differential control node NC2;

[0587] a first terminal of the second capacitor C2 is electrically connected to the second differential control node NC2, and a second terminal of the second capacitor C2 is electrically connected to the low voltage terminal VGL.

[0588] The difference between the driving circuit of at least one embodiment of FIG. 43 and the driving circuit of at least one embodiment of FIG. 31A is as follows: a second data writing circuit is further included;

[0589] the second data writing circuit includes a sixth transistor T6 and a second capacitor C2;

[0590] a gate electrode of the sixth transistor T6 is electrically connected to the switch control terminal SW, a source electrode of the sixth transistor T6 is electrically connected to the second data line SL2, and a drain electrode of the sixth transistor T6 is electrically connected to the second differential control node NC2;

[0591] a first terminal of the second capacitor C2 is electrically connected to the second differential control node NC2, and a second terminal of the second capacitor C2 is electrically connected to the low voltage terminal VGL.

[0592] The difference between the driving circuit of at least one embodiment of FIG. 44 and the driving circuit of at least one embodiment of FIG. 32 is as follows: a second data writing circuit is further included;

[0593] the second data writing circuit includes a sixth transistor T6 and a second capacitor C2;

[0594] a gate electrode of the sixth transistor T6 is electrically connected to the switch control terminal SW, a source electrode of the sixth transistor T6 is electrically connected to the second data line SL2, and a drain electrode of the sixth transistor T6 is electrically connected to the second differential control node NC2;

[0595] a first terminal of the second capacitor C2 is electrically connected to the second differential control node NC2, and a second terminal of the second capacitor C2 is electrically connected to the low voltage terminal VGL.

[0596] A driving method according to the embodiments of the present disclosure, applied to the above driving circuit, including:

[0597] providing, by output circuit, the driving output signal via the driving output terminal based on the data voltage under control of the switch control signal and the output control signal; and

[0598] inverting, by the inverter included in the inverting circuit, the signal received by the input terminal of the inverter, to obtain the inverted signal, and outputting the inverted signal via the output terminal of the inverter.

[0599] In at least one embodiment of the present disclosure, the output circuit includes a first data writing circuit, a differential control circuit, an input control circuit and an output control circuit, the output control circuit includes a latch circuit and a set circuit, a frame time includes a blanking period, the blanking period includes a setting period and an output phase, the setting period includes a reset phase, a data writing phase and a potential maintaining phase, and the driving method includes:

[0600] in the reset phase, controlling, by the set circuit, connection between an intermediate node and a second voltage terminal and connection between the driving output terminal and the second voltage terminal under control of the output control signal;

[0601] in the data writing phase, writing, by the first data writing circuit, a first data voltage provided by a first data line into a first differential control node under control of the switch control signal;

[0602] in the potential maintaining phase, maintaining, by the first data writing circuit, a potential of the first differential control node; and

[0603] in the output phase, controlling, by the input control circuit, connection between an input node and a first voltage terminal under control of the output control signal; controlling, by the differential control circuit, a potential of a first output node and a potential of a second output node based on a potential of the input node under control of the potential of the first differential control node and a potential of the second differential control node; controlling, by the latch circuit, the potential of the driving output terminal based on the potential of the first output node and the potential of the second output node under control of a potential of the intermediate node.

[0604] In at least one embodiment of the present disclosure, the output circuit further includes a second data writing circuit, and the driving method further includes:

[0605] in the data writing phase, writing, by the second data writing circuit, a second data voltage provided by a second data line into the second differential control node under control of the switch control signal; and

[0606] in the potential maintaining phase, maintaining, by the second data writing circuit, the potential of the second differential control node.

[0607] Optionally, the driving circuit further includes a switch control circuit, the blanking period includes an off phase, the off phase includes the setting period, and the driving method further includes:

[0608] in the off phase, controlling, by the switch control circuit, disconnection between the first output control node and the second output control node under control of an on-off control signal.

[0609] A display device according to the embodiments of the present disclosure includes the above driving circuit.

[0610] The above descriptions are preferred embodiments of the present disclosure. It should be noted that those skilled in the art that can make various improvements and modifications without departing from the principle of the present disclosure, and the improvements and the modifications shall fall within the scope of protection of the present disclosure.

1. A driving circuit, comprising: an output circuit and an inverting circuit;

wherein the output circuit is electrically connected to an output control terminal, a switch control terminal, a data line and a driving output terminal, and is configured to provide a driving output signal via the driving output terminal based on a data voltage provided by the data line under control of a switch control signal

provided by the switch control terminal and an output control signal provided by the output control terminal;

wherein the inverting circuit comprises N stages of inverters, N is a positive integer;

wherein an input terminal of a first inverter is electrically connected to the driving output terminal, and an output terminal of an N-th inverter is electrically connected to a driving signal output terminal;

wherein in a case that N is greater than 1, an output terminal of an m-th inverter is electrically connected to an input terminal of an (m+1)-th inverter, and m is a positive integer less than N; and

wherein the inverter is configured to invert a signal received by received by the input terminal of the inverter to obtain an inverted signal, and output the inverted signal via the output terminal of the inverter.

2. The driving circuit according to claim **1**, wherein the output circuit comprises a first data writing circuit, a differential control circuit, an input control circuit and an output control circuit;

wherein the first data writing circuit is electrically connected to the switch control terminal, a first data line and a first differential control node, and is configured to write a first data voltage provided by the first data line into the first differential control node and maintain a potential of the first differential control node under control of the switch control signal provided by the switch control terminal;

wherein the differential control circuit is electrically connected to the first differential control node, a second differential control node, an input node, a first output node, and a second output node, and is configured to control a potential of the first output node and a potential of the second output node based on a potential of the input node under control of the potential of the first differential control node and a potential of the second differential control node;

wherein the input control circuit is electrically connected to the output control terminal, the input node and a first voltage terminal, and is configured to control connection or disconnection between the input node and the first voltage terminal under control of the output control signal provided by the output control terminal; and

wherein the output control circuit is electrically connected to the output control terminal, the first output node, the second output node and the driving output terminal, and is configured to generate the driving output signal and provide the driving output signal via the driving output terminal based on the potential of the first output node and the potential of the second output node under control of the output control signal.

3. The driving circuit according to claim **2**, wherein the output control circuit comprises a latch circuit and a set circuit;

wherein the set circuit is electrically connected to the output control terminal, an intermediate node, the driving output terminal and a second voltage terminal, and is configured to control connection or disconnection between the intermediate node and the second voltage terminal and control connection or disconnection between the driving output terminal and the second voltage terminal under control of the output control signal; and

wherein the latch circuit is electrically connected to the first output node, the second output node, the intermediate node, the driving output terminal and the second voltage terminal, and is configured to control a potential of the driving output terminal based on the potential of the first output node and the potential of the second output node under control of a potential of the intermediate node.

4. The driving circuit according to claim **3**, wherein the output circuit further comprises a second data writing circuit;

wherein the second data writing circuit is electrically connected to the switch control terminal, a second data line and the second differential control node, and is configured to write a second data voltage provided by the second data line into the second differential control node and maintain the potential of the second differential control node under control of the switch control signal provided by the switch control terminal;

or,

wherein the driving circuit further comprises a switch control circuit;

wherein the switch control circuit is electrically connected to an on-off control terminal, a first output control node and a second output control node, and is configured to control connection or disconnection between the first output control node and the second output control node under control of an on-off control signal provided by the on-off control terminal;

wherein the first output control node is electrically connected to the driving output terminal, and the second output control node is electrically connected to the input terminal of the first inverter; or,

the first output control node is electrically connected to the output terminal of the N-th inverter, and the second output control node is electrically connected to the driving signal output terminal; or,

N is greater than 1, the first output control node is electrically connected to the output terminal of the m-th inverter, and the second output control node is electrically connected to the input terminal of the (m+1)-th inverter.

5. (canceled)

6. The driving circuit according to claim **4**, wherein the latch circuit is configured to control connection or disconnection between the second output node and the driving output terminal and connection or disconnection between the driving output terminal and the second voltage terminal under control of the potential of the intermediate node, and to control connection or disconnection between the first output node and the intermediate node and connection or disconnection between the intermediate node and the second voltage terminal under control of the potential of the driving output terminal.

7. The driving circuit according to claim **6**, wherein a frame time comprises a blanking period, the blanking period comprises an off phase, and the off phase comprises a setting period;

wherein the set circuit is configured to control connection between the intermediate node and the second voltage terminal and control connection between the driving output terminal and the second voltage terminal under control of the output control signal during the setting period; and

wherein the switch control circuit is configured to control disconnection between the first output control node and the second output control node under control of the on-off control signal during the off phase.

8. The driving circuit according to claim **1**, wherein N is equal to 1, the inverting circuit comprises the first inverter, and the first inverter comprises a first transistor and a second transistor;

wherein a gate electrode of the first transistor is electrically connected to the input terminal of the first inverter, a first electrode of the first transistor is electrically connected to a first voltage terminal, and a second electrode of the first transistor and a first electrode of the second transistor are both electrically connected to the driving signal output terminal;

wherein a gate electrode of the second transistor is electrically connected to the input terminal of the first inverter, and a second electrode of the second transistor is electrically connected to a second voltage terminal; and

wherein the first transistor is a p-type transistor, and the second transistor is an n-type transistor.

9. The driving circuit according to claim **1**, wherein N is equal to 2, the inverting circuit comprises the first inverter and a second inverter, the first inverter comprises a first transistor and a second transistor, and the second inverter comprises a third transistor and a fourth transistor;

wherein a gate electrode of the first transistor is electrically connected to the input terminal of the first inverter, a first electrode of the first transistor is electrically connected to a first voltage terminal, and a second electrode of the first transistor and a first electrode of the second transistor are both electrically connected to an input terminal of the second inverter;

wherein a gate electrode of the second transistor is electrically connected to the input terminal of the first inverter, and a second electrode of the second transistor is electrically connected to a second voltage terminal;

wherein a gate electrode of the third transistor and a gate electrode of the fourth transistor are both electrically connected to the input terminal of the second inverter, a first electrode of the third transistor is electrically connected to the first voltage terminal, and a second electrode of the third transistor and a first electrode of the fourth transistor are both electrically connected to the driving signal output terminal;

wherein a second electrode of the fourth transistor is electrically connected to the second voltage terminal; and

wherein the first transistor is a p-type transistor, the second transistor is an n-type transistor; the third transistor is a p-type transistor, and the fourth transistor is an n-type transistor.

10. The driving circuit according to claim **2**, wherein the first data writing circuit comprises a fifth transistor and a first capacitor;

wherein a gate electrode of the fifth transistor is electrically connected to the switch control terminal, a first electrode of the fifth transistor is electrically connected to the first data line, and a second electrode of the fifth transistor is electrically connected to the first differential control node; and

wherein a first terminal of the first capacitor is electrically connected to the first differential control node, and a second terminal of the first capacitor is electrically connected to a second voltage terminal.

11. The driving circuit according to claim **4**, wherein the second data writing circuit comprises a sixth transistor and a second capacitor, a gate electrode of the sixth transistor is electrically connected to the switch control terminal, a first electrode of the sixth transistor is electrically connected to the second data line, and a second electrode of the sixth transistor is electrically connected to the second differential control node; and

wherein a first terminal of the second capacitor is electrically connected to the second differential control node, and a second terminal of the second capacitor is electrically connected to the second voltage terminal.

12. The driving circuit according to claim **4**, wherein the switch control circuit comprises a seventh transistor;

wherein a gate electrode of the seventh transistor is electrically connected to the on-off control terminal, a first electrode of the seventh transistor is electrically connected to the first output control node, and a second electrode of the seventh transistor is electrically connected to the second output control node.

13. The driving circuit according to claim **3**, wherein the input control circuit comprises an eighth transistor, and the differential control circuit comprises a ninth transistor and a tenth transistor;

wherein a gate electrode of the eighth transistor is electrically connected to the output control terminal, a first electrode of the eighth transistor is electrically connected to the first voltage terminal, and a second electrode of the eighth transistor is electrically connected to the input node;

wherein a gate electrode of the ninth transistor is electrically connected to the first differential control node, a first electrode of the ninth transistor is electrically connected to the input node, and a second electrode of the ninth transistor is electrically connected to the first output node; and

wherein a gate electrode of the tenth transistor is electrically connected to the second differential control node, a first electrode of the tenth transistor is electrically connected to the input node, and a second electrode of the tenth transistor is electrically connected to the second output node.

14. The driving circuit according to claim **13**, wherein the set circuit comprises an eleventh transistor and a twelfth transistor;

wherein a gate electrode of the eleventh transistor is electrically connected to the output control terminal, a first electrode of the eleventh transistor is electrically connected to the intermediate node, and a second electrode of the eleventh transistor is electrically connected to the second voltage terminal; and

wherein a gate electrode of the twelfth transistor is electrically connected to the output control terminal, a first electrode of the twelfth transistor is electrically connected to the driving output terminal, and a second electrode of the twelfth transistor is electrically connected to the second voltage terminal.

15. The driving circuit according to claim **14**, wherein the eighth transistor is a p-type transistor, and the eleventh transistor and the twelfth transistor are n-type transistors; or, the eighth transistor is an n-type transistor, and the eleventh transistor and the twelfth transistor are p-type transistors.

16. The driving circuit according to claim 6, wherein the latch circuit comprises a thirteenth transistor, a fourteenth transistor, a fifteenth transistor, and a sixteenth transistor;

wherein a gate electrode of the thirteenth transistor is electrically connected to the driving output terminal, a first electrode of the thirteenth transistor is electrically connected to the intermediate node, and a second electrode of the thirteenth transistor is electrically connected to the second voltage terminal;

wherein a gate electrode of the fourteenth transistor is electrically connected to the intermediate node, a first electrode of the fourteenth transistor is electrically connected to the driving output terminal, and a second electrode of the fourteenth transistor is electrically connected to the second voltage terminal;

wherein a gate electrode of the fifteenth transistor is electrically connected to the driving output terminal, a first electrode of the fifteenth transistor is electrically connected to the first output node, and a second electrode of the fifteenth transistor is electrically connected to the intermediate node; and

wherein a gate electrode of the sixteenth transistor is electrically connected to the intermediate node, a first electrode of the sixteenth transistor is electrically connected to the second output node, and a second electrode of the sixteenth transistor is electrically connected to the driving output terminal.

17. The driving circuit according to claim 16, wherein the thirteenth transistor and the fourteenth transistor are n-type transistors, and the fifteenth transistor and the sixteenth transistor are p-type transistors.

18. A driving method, applied to the driving circuit according to claim 1, comprising:

providing, by the output circuit, the driving output signal via the driving output terminal based on the data voltage under control of the switch control signal and the output control signal; and

inverting, by the inverter comprised in the inverting circuit, the signal received by the input terminal of the inverter, to obtain the inverted signal, and outputting the inverted signal via the output terminal of the inverter.

19. The driving method according to claim 18, wherein the output circuit comprises a first data writing circuit, a differential control circuit, an input control circuit and an output control circuit, the output control circuit comprises a latch circuit and a set circuit, a frame time comprises a blanking period, the blanking period comprises a setting period and an output phase, the setting period comprises a reset phase, a data writing phase and a potential maintaining phase, and the driving method comprises:

in the reset phase, controlling, by the set circuit, connection between an intermediate node and a second voltage terminal and connection between the driving output terminal and the second voltage terminal under control of the output control signal;

in the data writing phase, writing, by the first data writing circuit, a first data voltage provided by a first data line into a first differential control node under control of the switch control signal;

in the potential maintaining phase, maintaining, by the first data writing circuit, a potential of the first differential control node; and

in the output phase, controlling, by the input control circuit, connection between an input node and a first voltage terminal under control of the output control signal; controlling, by the differential control circuit, a potential of a first output node and a potential of a second output node based on a potential of the input node under control of the potential of the first differential control node and a potential of the second differential control node; controlling, by the latch circuit, the potential of the driving output terminal based on the potential of the first output node and the potential of the second output node under control of a potential of the intermediate node.

20. The driving method according to claim 19, wherein the output circuit further comprises a second data writing circuit, and the driving method further comprises:

in the data writing phase, writing, by the second data writing circuit, a second data voltage provided by a second data line into the second differential control node under control of the switch control signal; and

in the potential maintaining phase, maintaining, by the second data writing circuit, the potential of the second differential control node;

and/or,

wherein the driving circuit further comprises a switch control circuit, the blanking period comprises an off phase, the off phase comprises the setting period, and the driving method further comprises:

in the off phase, controlling, by the switch control circuit, disconnection between the first output control node and the second output control node under control of an on-off control signal.

21. (canceled)

22. A display device, comprising a driving circuit; wherein the driving circuit comprises: an output circuit and an inverting circuit:

wherein the output circuit is electrically connected to an output control terminal, a switch control terminal, a data line and a driving output terminal, and is configured to provide a driving output signal via the driving output terminal based on a data voltage provided by the data line under control of a switch control signal provided by the switch control terminal and an output control signal provided by the output control terminal;

wherein the inverting circuit comprises N stages of inverters, N is a positive integer;

wherein an input terminal of a first inverter is electrically connected to the driving output terminal, and an output terminal of an N-th inverter is electrically connected to a driving signal output terminal;

wherein in a case that N is greater than 1, an output terminal of an m-th inverter is electrically connected to an input terminal of an (m+1)-th inverter, and m is a positive integer less than N; and

wherein the inverter is configured to invert a signal received by received by the input terminal of the inverter to obtain an inverted signal, and output the inverted signal via the output terminal of the inverter.

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