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Inventor(s)	Lim; Dongkyun

SEMICONDUCTOR DEVICE

Abstract

A semiconductor device includes active patterns stacked and spaced apart from each other in a vertical direction; and a capacitor connected to the active patterns. The capacitor includes first electrodes respectively connected to the active patterns and stacked and spaced apart from each other in the vertical direction; a second electrode penetrating through the first electrodes and extending in the vertical direction; a third electrode penetrating through the first electrodes and extending in the vertical direction, and spaced apart from the second electrode; first dielectric layers, each first dielectric layer being between a respective first electrode and the second electrode; and second dielectric layers, each second dielectric layer being between a respective first electrode and the third electrode.

Inventors: **Lim; Dongkyun (Suwon-si, KR)**

Applicant: **Samsung Electronics Co., Ltd.** (Suwon-si, KR)

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims benefit of priority to Korean Patent Application No. 10-2024-0021559 filed on Feb. 15, 2024, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein by reference in its entirety.

BACKGROUND

[0002] The present disclosure relates to a semiconductor device including a data storage structure having three electrodes and a method of forming the same.

[0003] Research is being conducted to reduce the size of elements included in a semiconductor device and improve performance thereof. For example, in a DRAM, research is being conducted to reliably and stably form reduced-sized elements, but with the reduction in the size of the elements, dispersion characteristics of semiconductor devices are deteriorating.

SUMMARY

[0004] An aspect of the present disclosure is to provide a semiconductor device that may increase a degree of integration and improve performance.

[0005] An aspect of the present disclosure is to provide a method of forming a semiconductor device.

[0006] A semiconductor device according to an example embodiment includes: active patterns stacked and spaced apart from each other in a vertical direction; and a capacitor connected to the active patterns, wherein the capacitor includes: first electrodes respectively connected to the active patterns and stacked and spaced apart from each other in the vertical direction; a second electrode penetrating through the first electrodes and extending in the vertical direction; a third electrode penetrating through the first electrodes and extending in the vertical direction, and spaced apart from the second electrode; first dielectric layers, each first dielectric layer being between a respective first electrode and the second electrode; and second dielectric layers, each second dielectric layer being between a respective first electrode and the third electrode.

[0007] A semiconductor device according to an example embodiment includes: a peripheral circuit region including a peripheral circuit; and a memory region on the peripheral circuit region and including cell blocks, wherein each of the cell blocks includes cell transistors and a data storage structure connected to first source/drain regions of the cell transistors, wherein the data storage structure of each of the cell blocks includes: first electrodes respectively connected to the first source/drain regions of the cell transistors, the first electrodes being stacked and spaced apart from each other in a vertical direction; a second electrode having a side surface facing the first electrodes; and a third electrode having a side surface facing the first electrodes and spaced apart from the second electrode, and wherein the peripheral circuit includes: a fixed voltage supply circuit configured to apply a fixed voltage to the second electrode; a write circuit configured to perform a write operation for storing “1” or “0” data in a unit memory cell of the cell blocks; and a variable voltage supply circuit configured to, during the write operation for storing data “1” in the unit memory cell, apply a positive voltage to the third electrode, and to, during the write operation for storing “0” data in the unit memory cell, apply a negative voltage to the third electrode.

[0008] A semiconductor device according to an example embodiment includes: active patterns stacked and spaced apart from each other in a vertical direction; and a data storage structure connected to the active patterns, wherein the data storage structure includes: first electrodes respectively connected to the active patterns, the first electrodes being stacked and spaced apart from each other in the vertical direction; a second electrode having a side surface facing the first electrodes; a third electrode having a side surface facing the first electrodes and spaced apart from the second electrode; first dielectric layers between respective first electrodes and the second

electrode; and second dielectric layers between respective first electrodes and the third electrode.
[0009] According to example embodiments, a capacitor structure including three electrodes and capable of storing information may be provided. Among the three electrodes, first electrodes may be respectively connected to first source/drain regions of cell transistors and may be stacked in a vertical direction, a second electrode may penetrate through the first electrodes and may be electrically connected to a fixed voltage circuit, and the third electrode may penetrate through the first electrodes and may be electrically connected to a variable voltage circuit.
[0010] The semiconductor device may include the capacitor structure including the three electrodes, thereby increasing the integration degree of semiconductor devices, and increasing a sensing margin for sensing information.
[0011] Additionally, because the second and third electrodes penetrating through the first electrodes may serve as supports, deformation such as warpage of cell transistors and capacitor structures may be prevented.
[0012] Advantages and effects of the present application are not limited to the foregoing content and may be more easily understood in the process of describing a specific example embodiment of the present disclosure.

Description

BRIEF DESCRIPTION OF DRAWINGS
[0013] The above and other aspects, features, and advantages of the present disclosure will be more clearly understood from the following detailed description, taken in conjunction with the accompanying drawings, in which:
[0014] FIGS. **1**, **2**A, and **2**B are views conceptually illustrating an example of a semiconductor device according to an example embodiment of the present disclosure;
[0015] FIGS. **3** and **4** are views conceptually illustrating a modified example of a semiconductor device according to an example embodiment of the present disclosure;
[0016] FIG. **5**A is a conceptual circuit diagram illustrating an example of a semiconductor device according to an example embodiment of the present disclosure;
[0017] FIG. **5**B is a conceptual circuit diagram illustrating a modified example of a semiconductor device according to an example embodiment of the present disclosure;
[0018] FIG. **5**C is a conceptual circuit diagram illustrating a modified example of a semiconductor device according to an example embodiment of the present disclosure;
[0019] FIG. **5**D is a conceptual circuit diagram illustrating a modified example of a semiconductor device according to an example embodiment of the present disclosure;
[0020] FIG. **6**A is a conceptual diagram illustrating an example of a semiconductor device according to an example embodiment of the present disclosure;
[0021] FIG. **6**B is a conceptual diagram illustrating a modified example of a semiconductor device according to an example embodiment of the present disclosure;
[0022] FIG. **6**C is a conceptual diagram illustrating a modified example of a semiconductor device according to an example embodiment of the present disclosure;
[0023] FIG. **6**D is a conceptual diagram illustrating a modified example of a semiconductor device according to an example embodiment of the present disclosure;
[0024] FIG. **7**A is a block diagram illustrating an example of a semiconductor device according to an example embodiment of the present disclosure;
[0025] FIG. **7**B is a circuit diagram illustrating an example of a semiconductor device according to an example embodiment of the present disclosure;
[0026] FIG. **8**A is a block diagram illustrating an example of a semiconductor device according to an example embodiment of the present disclosure;

[0027] FIGS. **8**B to **8**D are circuit diagrams illustrating an example of a semiconductor device according to an example embodiment of the present disclosure;
[0028] FIGS. **8**E to **8**G are circuit diagrams illustrating an example of a semiconductor device according to an example embodiment of the present disclosure;
[0029] FIG. **9**A is a conceptual perspective view illustrating an example of a semiconductor device according to an example embodiment of the present disclosure;
[0030] FIG. **9**B is a conceptual perspective view illustrating a modified example of a semiconductor device according to an example embodiment of the present disclosure;
[0031] FIG. **9**C is a conceptual perspective view illustrating a modified example of a semiconductor device according to an example embodiment of the present disclosure;
[0032] FIG. **9**D is a conceptual perspective view illustrating a modified example of a semiconductor device according to an example embodiment of the present disclosure;
[0033] FIG. **10**A is a plan view illustrating an example of a semiconductor device according to an example embodiment of the present disclosure;
[0034] FIG. **10**B is a plan view illustrating a modified example of a semiconductor device according to an example embodiment of the present disclosure;
[0035] FIG. **10**C is a plan view illustrating a modified example of a semiconductor device according to an example embodiment of the present disclosure;
[0036] FIG. **10**D is a plan view illustrating a modified example of a semiconductor device according to an example embodiment of the present disclosure;
[0037] FIG. **10**E is a plan view illustrating a modified example of a semiconductor device according to an example embodiment of the present disclosure;
[0038] FIG. **10**F is a plan view illustrating a modified example of a semiconductor device according to an example embodiment of the present disclosure;
[0039] FIG. **10**G is a plan view illustrating a modified example of a semiconductor device according to an example embodiment of the present disclosure;
[0040] FIG. **10**H is a plan view illustrating a modified example of a semiconductor device according to an example embodiment of the present disclosure;
[0041] FIG. **10**I is a plan view illustrating a modified example of a semiconductor device according to an example embodiment of the present disclosure;
[0042] FIGS. **11**A to **11**D are perspective views illustrating an example of a method of forming a semiconductor device according to an example embodiment of the present disclosure; and
[0043] FIGS. **12**A to **12**G are views illustrating an example of a method of forming a semiconductor device according to an example embodiment of the present disclosure.

DETAILED DESCRIPTION

[0044] Hereinafter, the terms such as “upper,” “intermediate,” and “lower” may be replaced with other terms such as “first,” “second,” and “third” and may be used to describe elements of the specification. The terms such as “first,” “second,” and “third” may be used to describe various elements, but the elements are not limited thereto, and the “first element” could be termed “second element.”
[0045] In the specification, it may be understood that the expressions such as “below”, “beneath,” “on,” “above,” “upper,” and “lower” may be described based on drawings.
[0046] First, an example of a semiconductor device according to an example embodiment of the present disclosure will be described with reference to FIG. **1**. FIG. **1** is a circuit diagram schematically illustrating a semiconductor device according to an example embodiment of the present disclosure.
[0047] Throughout the specification, when a component is described as “including” a particular element or group of elements, it is to be understood that the component is formed of only the element or the group of elements, or the element or group of elements may be combined with additional elements to form the component, unless the context indicates otherwise. The term

"consisting of," on the other hand, indicates that a component is formed only of the element(s) listed.

[0048] Terms such as "same," "equal," etc. as used herein when referring to features such as orientation, layout, location, shapes, sizes, compositions, amounts, or other measures do not necessarily mean an exactly identical feature but is intended to encompass nearly identical features including typical variations that may occur resulting from conventional manufacturing processes. The term "substantially" may be used herein to emphasize this meaning.

[0049] Referring to FIG. **1**, a semiconductor device **1** according to an example embodiment may include a plurality of cell blocks CB. Each of the plurality of cell blocks CB may include cell transistors cTR. Each of the cell transistors cTR may include a first source/drain region SD**1**, a second source/drain region SD**2**, and a channel region between the first source/drain region SD**1** and the second source/drain region SD**2**, and a word line WL that may be a gate electrode.

[0050] Hereinafter, the description will focus on one cell block CB among the plurality of cell blocks CB.

[0051] The cell block CB may further include a bit line BL electrically connected to the second source/drain regions SD**2** of the cell transistors cTR.

[0052] The cell block CB may further include a data storage structure C**1** electrically connected to the first source/drain regions SD**1** of the cell transistors cTR.

[0053] In an example embodiment, the data storage structure C**1** may be a capacitor structure capable of storing information. Hereinafter, the data storage structure C**1** will be described and referred to as a capacitor structure.

[0054] The data storage structure C**1** may include first electrodes E**1** respectively connected to the first source/drain regions SD**1**, second electrodes E**2** facing the first electrodes E**1**, and third electrodes E**3** facing the first electrodes E**1** and spaced apart from the first electrodes E**1**.

[0055] Referring to FIG. **1**, when describing one first electrode E**1** of the first electrodes E**1** as a reference, the first electrode E**1**, the corresponding second electrode E**2**, and the corresponding third electrode E**3** may be included in a first capacitor C**1***a*. Another first electrode E**1**, the corresponding second electrode E**2**, and the corresponding third electrode E**3** may be included in a second capacitor C**1***b*. Accordingly, the capacitor structure C**1** may include the first capacitor C**1***a* and the second capacitor C**1***b*. Next, together with FIG. **1** described above, an example of a semiconductor

[0056] device according to an example embodiment of the present disclosure will be described with reference to FIGS. **2**A and **2**B. FIG. **2**A is a conceptual perspective view illustrating a semiconductor device according to an example embodiment of the present disclosure, and FIG. **2**B is a perspective view illustrating an active pattern ACT of FIG. **2**A.

[0057] Referring to FIGS. **2**A and **2**B along with FIG. **1**, the semiconductor device **1** may include active patterns ACT stacked and spaced apart from each other in a vertical direction (Z-direction).

[0058] Each of the activation patterns ACT may include the first source/drain region SD**1**, the second source/drain region SD**2**, and the channel region CH between the first source/drain region SD**1** and the second source/drain region SD**2** described in FIG. **1**. The second source/drain region SD**2**, the channel region CH, and the first source/drain region SD**1** may be sequentially arranged in a first horizontal direction (X-direction). Each of the active patterns ACT may have a bar shape extending in the first horizontal direction (X-direction). The first horizontal direction (X-direction) may be a first horizontal direction, perpendicular to the vertical direction (Z-direction).

[0059] An item, layer, or portion of an item or layer described as "extending" or as extending "lengthwise" in a particular direction has a length in the particular direction and a width perpendicular to that direction, where the length is greater than the width.

[0060] Two active patterns ACT stacked in the vertical direction (Z-direction) are illustrated in FIG. **2**A, but the inventive concept is not limited thereto. The number of active patterns ACT stacked in the vertical direction (Z-direction) may be more than two.

[0061] The active patterns ACT may be semiconductor patterns formed of a semiconductor material. For example, each of the active patterns ACT may be formed of a silicon layer, but the inventive concept is not limited thereto, and each of the active patterns ACT may also be formed of other semiconductor materials.
[0062] The first and second source/drain regions SD**1** and SD**2** may have an N-type conductivity. The first source/drain regions SD**1** may be stacked and spaced apart from each other in the vertical direction (Z-direction), and may overlap each other vertically. The second source/drain regions SD**1** may be stacked and spaced apart from each other in the vertical direction (Z-direction), and may overlap each other vertically. The channel regions CH may be stacked and spaced apart from each other in the vertical direction (Z-direction), and may overlap each other vertically.
[0063] As described in FIG. **1**, the capacitor structure C**1** may be electrically connected to the first source/drain regions SD**1**. Accordingly, the capacitor structure C**1** may be connected to the active patterns ACT.
[0064] The capacitor structure C**1** may be a data storage structure capable of storing information in a semiconductor device including a memory such as DRAM.
[0065] The capacitor structure C**1** may further include first dielectric layers Dia**1** between the first electrodes E**1** and the second electrode E**2**, and second dielectric layers Dia**2** between the first electrodes E**1** and the third electrode E**3**.
[0066] The first electrodes E**1** that may be electrically connected to the corresponding first source/drain regions SD**1** may be stacked and spaced apart from each other in the vertical direction (Z-direction), and may overlap each other vertically.
[0067] The second electrode E**2** may have a side surface facing the first electrodes E**1**. For example, each of the side surfaces of the second electrode E**2** may face the first electrodes E**1**. The second electrode E**2** may extend in the vertical direction (Z-direction) and may penetrate through the first electrodes E**1**. The second electrode E**2** may be a conductive pillar extending in the vertical direction (Z-direction).
[0068] The third electrode E**3** may have a side surface facing the first electrodes E**1**. For example, each of the side surfaces of the third electrode E**3** may face the first electrodes E**1**. The third electrode E**3** may extend in the vertical direction (Z-direction) and may penetrate through the first electrodes E**1**. The third electrode E**3** may be a conductive pillar extending in the vertical direction (Z-direction). The second electrode E**2** may be spaced apart from the third electrode E**3**. Each of the first electrodes E**1** may surround a side surface (e.g., side surfaces) of the second electrode E**2** and a side surface (e.g., side surfaces) of the third electrode E**3**. Accordingly, each of the first electrodes E**1** may have a ring shape surrounding the side surfaces of the second and third electrodes E**2** and E**3**. The ring shape of each of the first electrodes E**1** may have two holes through which the second electrode E**2** and the third electrode E**3** pass.
[0069] The second and third electrodes E**2** and E**3** may be formed simultaneously and may include the same conductive material.
[0070] Since the second and third electrodes E**2** and E**3** penetrating through the first electrodes E**1** may serve as supports, deformation such as warpage of the cell transistors cTR and the capacitor structure C**1** may be prevented.
[0071] Each of the second and third electrodes E**2** and E**3** may include a lower surface disposed at a lower level than a lowermost active pattern, among the active patterns ACT, and an upper surface disposed at a higher level than an uppermost active pattern, among the active patterns.
[0072] In example embodiments, one of the second electrode E**2** and the third electrode E**3** may be an electrode to which a fixed voltage is applied, and the other thereof may be an electrode to which a variable voltage is applied.
[0073] The bit line BL electrically connected to the second source/drain regions SD**2** described in FIG. **1** may extend in the vertical direction (Z-direction). The bit line BL may be connected to the active patterns ACT.

[0074] The word lines WL described in FIG. **1** may be stacked and spaced apart from each other in the vertical direction (Z-direction). The word lines WL may vertically overlap the channel regions CH.
[0075] The semiconductor device **1** may further include gate dielectric layers Gox disposed between the word lines WL and the active patterns ACT.
[0076] Each of the cell transistors (cTR) described in FIG. **1** may include the first source/drain region SD**1**, the second source/drain region SD**2**, the channel region CH, the gate dielectric layer Gox, and the word line WL. The cell transistors cTR may be stacked in the vertical direction (Z-direction). The word lines WL may be gate electrodes.
[0077] In one channel region CH and one word line WL that are adjacent to each other, among the channel regions CH and the word lines WL, the word line WL may face at least one of a lower surface and an upper surface of the channel region CH. For example, the word line WL may include a first portion WL_**1** disposed below the lower surface of the channel region CH, and a second portion WL_**2** disposed on the upper surface of the channel region CH.
[0078] The semiconductor device **1** may further include gate connection patterns WLc connected to the word lines WL. For example, in one word line WL and one gate connection pattern WLc connected to each other, among the word lines WL and the gate connection patterns WLc, the gate connection pattern WLc may be connected to the first and second portions WLa_**1** and WLa_**2** of the word line WL.
[0079] Next, a modified example of a semiconductor device according to an example embodiment of the present disclosure will be described with reference to FIG. **3**. FIG. **3** is a circuit diagram illustrating a modified example of the word line WL and the bit line BL described in FIG. **1**.
[0080] Referring to FIG. **3**, the cell transistors cTR (see FIG. **1**) including the word line WL (see FIG. **1**) described above may be modified into cell transistors cTRa including a word line WLa as illustrated in FIG. **3**. Each of the cell transistors cTRa may include the first source/drain region SD**1**, the channel region CH, and the second source/drain region SD**2**, as described in FIG. **1**. The cell transistors cTRa may share the word line WLa.
[0081] The bit line BL (see FIG. **1**) described above may be modified into separate bit lines BLa electrically connected to the second source/drain regions SD**2**, respectively, and spaced apart from each other, as illustrated in FIG. **3**.
[0082] Next, a modified example of a semiconductor device according to an example embodiment of the present disclosure will be described with reference to FIG. **4** along with FIG. **3**. FIG. **4** further illustrates that the active patterns ACT stacked in the vertical direction (Z-direction) in FIG. **2**A are arranged in the second horizontal direction (Y-direction), and is a conceptual perspective view illustrating a modified example of the word lines WL (see FIG. **2**A) and the bit lines BL (FIG. **2**A) described in FIG. **2**A.
[0083] Referring to FIG. **4** along with FIG. **3**, the word line WL (see FIG. **2**A) described above may be modified into word lines WLa as illustrated in FIG. **4**.
[0084] Each of the word lines WLa may include a vertical portion WLaa extending in the vertical direction (Z-direction) and a protruding portion WLab extending in a horizontal direction from the vertical portion WLaa to vertically overlap the channel regions CH. The gate dielectric layers Gox described above may be disposed between each word line WLa and the corresponding active pattern ACT.
[0085] The bit line BL (see FIGS. **1** and **2**A) described above may be modified into bit lines BLa as illustrated in FIGS. **3** and **4**. The bit lines BLa may be respectively connected to the second source/drain regions SD**2** sequentially arranged in the vertical direction (Z-direction). Each of the bit lines BLa may be connected to the second source/drain regions SD**2** sequentially arranged in the second horizontal direction (Y-direction). Each of the bit lines BLa may include a line portion BLaa extending in the second horizontal direction (Y-direction) and electrically connected to the second source/drain regions SD**2** disposed at the same level, and a pad portion BLab extending from the

line portion BLaa in a direction away from the active patterns ACT.
[0086] The cell transistors cTR (see FIGS. **1** and **2**) illustrated in FIGS. **1** and **2** may be modified into cell transistors cTRa as illustrated in FIGS. **3** and **4**.
[0087] Each of the cell transistors cTRa includes the first source/drain region SD**1**, the second source/drain region SD**2**, the channel region CH, the gate dielectric layer Gox, and the word line WLa.
[0088] Next, referring to FIG. **5**A, an example in which voltage is applied to the second electrode E**2** (FIGS. **1**, **2**A, **3** and **4**) and the third electrode E**3** (FIGS. **1**, **2**A, **3** and **4**) described above will be described. FIG. **5**A is a circuit diagram illustrating a first routing interconnection structure R**2***a* for applying voltage to the second electrode E**2** and a second routing interconnection structure R**3***a* for applying voltage to the third electrode E**3** in the circuit of FIG. **1**. In an example embodiment, first and second routing interconnection structures R**2***a* and R**3***a* that apply voltage in the circuit of FIG. **1** are illustrated, but the first and second routing interconnection structures R**2***a* and R**3***a* may be equally applied to FIGS. **2**, **3** and **4**.
[0089] In FIG. **5**A, the vertical direction (Z-direction) may be described to be divided into a +Z direction directed from a lower surface to an upper surface of each of the second and third electrodes E**2** and E**3** and a −Z direction directed from the upper surface to the lower surface of each of the second and third electrodes E**2** and E**3**. Here, the +Z direction may be a direction directed from a lowermost active pattern to an uppermost active pattern, among the active patterns ACT (see FIG. **3**), and the −Z direction may be a direction directed from the uppermost active pattern to the lowermost active pattern, among the active patterns ACT (see FIG. **3**).
[0090] Referring to FIG. **5**A, the semiconductor device **1** may further include a first routing interconnection structure R**2***a* electrically connected to the second electrode E**2** to apply fixed voltage, and a second routing interconnection structure R**3***a* electrically connected to the third electrode E**3** to apply variable voltage.
[0091] The first routing interconnection structure R**2***a* may be connected to a lower end of the second electrode E**2**. Accordingly, the first routing interconnection structure R**2***a* may be connected to a lower end of the second electrode E**2** to apply voltage to the second electrode E**2** in the +Z direction. The second routing interconnection structure R**3***a* may be connected to an upper end of the third electrode E**3**. Accordingly, the second routing interconnection structure R**3***a* may be connected to the upper end of the third electrode E**3** to apply voltage to the third electrode E**3** in the −Z direction.
[0092] Accordingly, the second and third electrodes E**2** and E**3** of the cell block CB may be electrically connected to the first and second routing interconnection structures R**2***a* and R**3***a*, respectively.
[0093] Next, referring to FIGS. **5**B, **5**C and **5**D, respectively, various modified examples of the first routing interconnection structure R**2***a* (see FIG. **5**A) and the second routing interconnection structure R**3***a* (see FIG. **5**A) described in FIG. **5**A will be described. FIGS. **5**B, **5**C and **5**D are circuit diagrams illustrating various modified examples of the first routing interconnection structure R**2***a* (FIG. **5**A) and the second routing interconnection structure R**3***a* (FIG. **5**A) described in FIG. **5**A.
[0094] In a modified example, referring to FIG. **5**B, the first routing interconnection structure R**2***a* (see FIG. **5**A) shown in FIG. **5**A may be modified into a first routing interconnection structure R**2***b* connected to an upper end of the second electrode E**2**, and the second routing interconnection structure R**3***a* (FIG. **5**A) shown in FIG. **5**A may be modified into a second routing interconnection structure R**3***b* connected to a lower end of the third electrode E**3**. The first routing interconnection structure R**2***b* may be connected to the upper end of the second electrode E**2** to apply voltage to the second electrode E**2** in the −Z direction. The second routing interconnection structure R**3***b* may be connected to the lower end of the third electrode E**3** to apply voltage to the third electrode E**3** in the +Z direction.

[0095] In a modified example, referring to FIG. **5**C, as shown in FIG. **5**A, the first routing interconnection structure R**2***a* may be connected to the lower end of the second electrode E**2** to apply voltage to the second electrode E**2** in the +Z direction, and as shown in FIG. **5**B, the second routing interconnection structure R**3***b* may be connected to the lower end of the third electrode E**3** to apply voltage to the third electrode E**3** in the +Z direction.
[0096] In a modified example, referring to FIG. **5**D, as shown in FIG. **5**B, the first routing interconnection structure R**2***b* may be connected to the upper end of the second electrode E**2** to apply voltage to the second electrode E**2** in the −Z direction, and as shown in FIG. **5**A, the second routing interconnection structure R**3***a* may be connected to the upper end of the third electrode E**3** to apply voltage to the third electrode E**3** in the −Z direction.
[0097] In the above-described example embodiments, one of the second electrode E**2** and the third electrode E**3** may be an electrode to which fixed voltage is applied, and the other thereof may be an electrode to which variable voltage is applied. Hereinafter, the second electrode E**2** will be described as an electrode to which fixed voltage is applied, and the third electrode E**3** will be described as an electrode to which variable voltage is applied.
[0098] Next, referring to FIG. **6**A along with FIG. **5**A, an example of a semiconductor device according to an example embodiment of the present disclosure will be described.
[0099] FIG. **6**A is a conceptual diagram illustrating an example of a semiconductor device according to an example embodiment of the present disclosure.
[0100] Referring to FIG. **6**A together with FIG. **5**A, the semiconductor device **1** may include a memory region MR including the cell block CB and the first and second routing interconnection structures R**2***a* and R**3***a*, and a peripheral circuit region PR vertically overlapping the memory region MR. The memory region MR may be disposed on the peripheral circuit region PR.
[0101] The peripheral circuit region PR may include a fixed voltage supply circuit VP**1** for applying the fixed voltage to the second electrode E**2** in the memory region MR, and a variable voltage supply circuit VP**2** for applying the variable voltage to the third electrode E**3** in the memory region MR.
[0102] The first routing interconnection structure R**2***a* may extend into the peripheral circuit region PR and may be electrically connected to the fixed voltage supply circuit VP**1**. The second routing interconnection structure R**3***a* may extend into the peripheral circuit region PR and may be electrically connected to the variable voltage supply circuit VP**2**. Each of the first and second routing interconnection structures R**2***a* and R**3***a* may be formed using a conductive pad, a conductive via, and a conductive interconnection.
[0103] The first routing interconnection structure R**2***a* may electrically connect the lower end of the second electrode E**2** to the fixed voltage supply circuit VP**1**, and the second routing interconnection structure R**3***a* may electrically connect the upper end of the third electrode E**3** to the variable voltage supply circuit VP**2**.
[0104] Next, referring to FIG. **6**B, an electrical connection relationship between the first and second routing interconnection structures R**2***b* and R**3***b* shown in FIG. **5**B and the variable voltage supply circuit VP**2** and the fixed voltage supply circuit VP**1** shown in FIG. **6**A is described.
[0105] Referring to FIG. **6**B together with FIG. **5**B, the first routing interconnection structure R**2***b* may electrically connect the upper end of the second electrode E**2** to the fixed voltage supply circuit VP**1**, and the second routing interconnection structure R**3***b* may electrically connect the lower end of the third electrode E**3** to the variable voltage supply circuit VP**2**.
[0106] Next, referring to FIG. **6**C, an electrical connection relationship between the first and second routing interconnection structures R**2***a* and R**3***b* shown in FIG. **5**C and the variable voltage supply circuit VP**2** and the fixed voltage supply circuit VP**1** shown in FIG. **6**A is described.
[0107] Referring to FIG. **6**C together with FIG. **5**C, the first routing interconnection structure R**2***a* may electrically connect the lower end of the second electrode E**2** to the fixed voltage supply circuit VP**1**, and the second routing interconnection structure R**3***b* may electrically connect the

lower end of the third electrode E**3** to the variable voltage supply circuit VP**2**.
[0108] Next, referring to FIG. **6**D, an electrical connection relationship between the first and second routing interconnection structures R**2***b* and R**3***a* shown in FIG. **5**D and the variable voltage supply circuit VP**2** and the fixed voltage supply circuit VP**1** shown in FIG. **6**A is described.
[0109] Referring to FIG. **6**D together with FIG. **5**D, the first routing interconnection structure R**2***b* may electrically connect the upper end of the second electrode E**2** to the fixed voltage supply circuit VP**1**, and the second routing interconnection structure R**3***a* may electrically connect the upper end of the third electrode E**3** to the variable voltage supply circuit VP**2**.
[0110] Next, referring to FIGS. **7**A and **7**B, an example of a semiconductor device according to an example embodiment of the present disclosure will be described. FIG. **7**A is a block diagram illustrating an example of a semiconductor device according to an example embodiment of the present disclosure, and FIG. **7**B is a circuit diagram illustrating an example of the variable voltage supply circuit VP**2**.
[0111] Referring to FIGS. **7**A and **7**B, the memory region MR of any of the example embodiments of FIGS. **6**A to **6**D may include a memory cell array region MCA including the plurality of cell blocks CB, and the peripheral circuit region PR of any of the example embodiments of FIGS. **6**A to **6**D may include a peripheral circuit PC.
[0112] The variable voltage supply circuit VP**2** may include a first voltage supply circuit VP**2***a* and a second voltage supply circuit VP**2***b*.
[0113] The peripheral circuit PC may include a write circuit WC for performing a write operation, and the first voltage supply circuit VP**2***a* of the variable voltage supply circuit VP**2** electrically may be connected to the writing circuit WC.
[0114] The writing circuit WC and the first voltage supply circuit VP**2***a* of the variable voltage supply circuit VP**2** may be circuits for storing data in the capacitor structures C**1** of the plurality of cell blocks CB.
[0115] In an example embodiment, a unit memory cell cTR, C**1** (see FIG. **1**) of the cell block CB may be comprised of one cell transistor cTR (see FIG. **1**) and one capacitor structure C**1** connected to the one cell transistor cTR.
[0116] Storing “1” data in the unit memory cell cTR, C**1** (see FIG. **1**) in the write circuit WC may be performed in a manner in which, in a state in which Vp voltage, that is, fixed voltage, is applied to the second electrode E**2**, the cell transistor cTR (see FIG. **1**) is turned on, and then, in order to charge the capacitor structure C**1** with electric charges, Vdd voltage is applied to the bit line BL (see FIG. **1**) to save “1” data, and when the cell transistor cTR (see FIG. **1**) is turned off, the saved “1” data is stored.
[0117] Storing “0” data in the unit memory cell cTR, C**1** (see FIG. **1**) in the write circuit WC may be performed in a manner in which, in a state in which the fixed voltage is applied to the second electrode E**2**, the cell transistor cTR (see FIG. **1**) is turned on, and in order to discharge the electric charges of the capacitor structure C**1**, voltage, for example, 0V, is applied to the bit line BL (see FIG. **1**) to save “0” data, and when the cell transistor cTR (see FIG. **1**) is turned off, the saved “0” data may be stored.
[0118] The first voltage supply circuit VP**2***a* of the variable voltage supply circuit VP**2** may be a circuit for providing variable voltage to the third electrode E**3** during the write operation. For example, the first voltage supply circuit VP**2***a* of the variable voltage supply circuit VP**2** may be electrically connected to the writing circuit WC and the second routing interconnection structure R**3***a*, and may provide the variable voltage to the third electrode E**3**, between the writing circuit WC of the peripheral circuit PC and the second routing interconnection structure R**3***a*. The second routing interconnection structure R**3***a* may be the same as that described in FIGS. **6**A and **6**D, but the inventive concept is not limited thereto. For example, the second routing interconnection structure R**3***a* may be replaced with the second routing interconnection structure R**3***b* described in FIGS. **6**B and **6**C.

[0119] The first voltage supply circuit VP**2***a* of the variable voltage supply circuit VP**2** may include a PMOS transistor TR**1** and a first NMOS transistor TR**2** in which sources are connected to each other and gates are connected to each other. The sources connected to each other of the PMOS transistor TR**1** and the first NMOS transistor TR**2** may be electrically connected to the second routing interconnection structure R**3***a*. A drain of the PMOS transistor TR**1** may be connected to V.sub.H voltage, and a drain of the first NMOS transistor TR**2** may be connected to V.sub.L voltage. The first voltage supply circuit VP**2***a* of the variable voltage supply circuit VP**2** may further include a second NMOS transistor TR**3** between the writing circuit WC and gates connected to each other of the PMOS transistor TR**1** and the first NMOS transistor TR**2**.
[0120] The fixed voltage applied to the second electrode E**2** may be a first positive voltage, the V.sub.H voltage may be a second positive voltage different from the first positive voltage, and the V.sub.L voltage may be a negative voltage. The first positive voltage may be higher than the second positive voltage.
TABLE-US-00001 TABLE 1 Applying V.sub.H voltage to the Applying V.sub.L voltage to the third electrode third electrode D0 G W D1 W G
[0121] Table 1 above may show that in a cell block CB in the memory cell array region MCA, during the write operation, when data is "0" or data is "1," operation characteristics may be displayed according to the voltage applied to the third electrode E**3** (see FIG. **1**). Here, among "W" and "G," "G" may mean better operating characteristics than "W." The operating characteristic may be a sensing margin. Thus, as shown in Table 1, when writing "0" to the cell block CB, the sensing margin when applying voltage V.sub.H to the third electrode is better than the sensing margin when applying voltage V.sub.L to the third electrode. Further, when writing "1" to the cell block CB, the sensing margin when applying voltage V.sub.L to the third electrode is better than the sensing margin when applying voltage V.sub.H to the third electrode.
[0122] During the write operation, when "0" data is being stored in the capacitor structure C**1** of the unit memory cell cTR, C**1** (see FIG. **1**), the operating characteristics may be improved when the V.sub.H voltage is applied to the third electrode E**3**, as compared to when the V.sub.L voltage is applied to the third electrode E**3**. Accordingly, during the write operation, in the case of storing information "0" in the capacitor structure C**1** of a unit memory cell, in order to improve the operating characteristics, the variable voltage supply circuit VP**2** may apply the V.sub.H voltage to the third electrode E**3** through the second routing interconnection structure R**3***a*.
[0123] During the write operation, when "1" data is being stored in the capacitor structure C**1** of the unit memory cell cTR, C**1** (see FIG. **1**), the operating characteristics may be improved when the V.sub.L voltage is applied to the third electrode E**3**, as compared to when the V.sub.H voltage is applied to the third electrode E**3**. Accordingly, during the write operation, when "1" data is stored in the capacitor structure C**1** of the unit memory cell cTR, C**1** (see FIG. **1**), in order to improve the operating characteristics, the variable voltage supply circuit VP**2** may apply the V.sub.L voltage to the third electrode E**3** through the second routing interconnection structure R**3***a*.
[0124] In example embodiments, during the write operation, when storing "0" data in the capacitor structure C**1** of the unit memory cell cTR, C**1** (see FIG. **1**), the V.sub.H voltage applied to the third electrode E**3** may be about +0.1V to about +0.3V.
[0125] In example embodiments, during the write operation, when storing "1" data in the capacitor structure C**1** of the unit memory cell cTR, C**1** (see FIG. **1**), the V.sub.L voltage applied to the third electrode E**3** may be about-0.1V to about-0.3V.
[0126] In example embodiments, during read and write operations, the fixed voltage applied to the second electrode E**2** may be about +0.5V to about +0.6V.
[0127] The peripheral circuit PC may further include a read circuit RC for performing a read operation. When the cell blocks CB (see FIGS. **1** and **2**A) are in an off state, the peripheral circuit PC may further include voltage control circuits FC for supplying an optimized voltage to each of the turned-off cell blocks CB, and/or supplying an optimized offset voltage to the third electrode

E**3** during the read operation using the read circuit RC. Accordingly, the voltage control circuits FC may be used when the cell blocks CB (see FIGS. **1** and **2**A) are in an off state or may be used during the read operation.

[0128] In one example, in order to read data stored in the unit memory cell cTR, C**1** (see FIG. **1**) using the read circuit RC, in a state in which the fixed voltage is applied to the second electrode E**2**, when the cell transistor cTR (see FIG. **1**) is turned on and ½ Vdd voltage is applied to the bit line BL (see FIG. **1**), the bit line BL (see FIG. **1**) may be connected to the capacitor C**1** (see FIG. **1**), and when the capacitor structure C**1** is charged with electric charges, the ½ Vdd voltage of the bit line BL may slightly increase, and when the capacitor structure C**1** is discharged, the ½ Vdd voltage of the bit line BL may slightly decrease. The slight voltage change, that is, a potential difference, of the bit line BL may be amplified by a sense amplifier of the peripheral circuit PC, and thus, when the potential difference of the bit line BL increases, "1" data may be read as being stored, and when the potential difference of the bit line BL decreases, "0" data may be read as being stored.

[0129] During the write and read operations as described above, the Vp voltage, that is, fixed voltage, may be applied to the second electrode E**2** by the fixed voltage supply circuit VP**1** (FIG. **6**A) in the peripheral circuit PC.

[0130] During the read operation, in order to increase the sensing margin, an optimal offset voltage may be applied to the third electrode E**3** using the voltage control circuits FC. In this manner, examples of applying an optimal voltage to the third electrode E**3** using the voltage control circuits FC when the cell blocks (CB in FIGS. **1** and **2**A) are in an off state or during the read operation will be described referring to FIGS. **8**A, **8**B, **8**C, **8**D and **8**E. FIG. **8**A is a block diagram illustrating an example of a semiconductor device according to an example embodiment of the present disclosure, FIG. **8**B is a circuit diagram illustrating an example of a first voltage control circuit F**1** of FIG. **8**A, FIG. **8**C is a circuit diagram illustrating an example of a second voltage control circuit F**2** of FIG. **8**A, FIG. **8**D is a circuit diagram illustrating an example of a third voltage control circuit F**3** of FIG. **8**A, FIG. **8**E is a circuit diagram illustrating a modified example of the first voltage control circuit F**1** of FIG. **8**B, FIG. **8**F is a circuit diagram illustrating a modified example of the second voltage control circuit F**2** of FIG. **8**C, and FIG. **8**G is a circuit diagram illustrating a modified example of the third voltage control circuit F**3** of FIG. **8**D.

[0131] First, referring to FIGS. **8**A, **8**B, **8**C and **8**D along with FIG. **7**A, the memory cell array region MCA in FIG. **7**A may include a plurality of cell blocks CB. For example, the memory cell array region MCA may include a first cell block CB**1**, a second cell block CB**2**, and a third cell block CB**3**.

[0132] In one example, the voltage control circuits FC may be provided to apply an optimal offset voltage to the third electrodes E**3** connected to the first, second, and third cell blocks CB**1**, CB**2**, and CB**3** during the read operation.

[0133] Each of the voltage control circuits FC may include one or more unit voltage control cells F_ON**1**, F_ON**2**, F_ON**3**, F_OFF**1** and F_OFF**2** connected in parallel. Each of the unit voltage control cells F_ON**1**, F_ON**2**, F_ON**3**, F_OFF**1** and F_OFF**2** may include a capacitor Cf, a fuse Rf or Sf, and a transistor TRf connected in series.

[0134] In one example, the transistor TRf may be turned on during the read operation and may be turned off during the write operation.

[0135] In one example, the transistor TRf may be turned on when the cell blocks CB are turned off.

[0136] Terminals of the voltage control circuits FC adjacent to the capacitor Cf may be electrically connected to the third electrode E**3**, and terminals of the voltage control circuits FC adjacent to the transistor TRf may be electrically connected to the second voltage supply circuit VP**2***b* of the variable voltage supply circuit VP**2**.

[0137] Depending on the state of the fuse Rf or Sf, the unit voltage control cells F_ON**1**, F_ON**2**, F_ON**3**, F_OFF**1** and F_OFF**2** may include first unit voltage control cells F_ON**1**, F_ON**2** and F_ON**3** in an on state and second unit voltage control cells F_OFF**1** and F_OFF**2** in an off state.

[0138] The unit voltage control cells F_ON**1**, F_ON**2**, F_ON**3**, F_OFF**1** and F_OFF**2** may use a MOSFET fuse. For example, the second unit voltage control cells F_OFF**1** and F_OFF**2** may include a fuse Sf in which the MOSFET fuse is cut off, that is, in an off state, and the first unit voltage control cells F_ON**1**, F_ON**2** and F_ON**3** may include a fuse Rf in which the MOSFET fuse is in an on state. The voltage control circuits FC may include the same number of unit voltage control cells as each other, and at least some of the voltage control circuits FC may include both a unit voltage control cell in an on state and a unit voltage control cell in an off state.
[0139] The voltage control circuits FC may include a first voltage control circuit F**1** electrically connected to the third electrode E**3** of the first cell block CB**1**, a second voltage control circuit F**2** electrically connected to the third electrode E**3** of the second cell block CB**2**, and a third voltage control circuit F**3** electrically connected to the third electrode E**3** of the third cell block CB**3**.
[0140] The first voltage control circuit F**1** may include the first unit voltage control cells F_ON**1**, F_ON**2** and F_ON**3** in an on state. The first voltage control circuit F**1** may apply a first voltage V**1** to the third electrodes E**3** of the first cell block CB**1**.
[0141] The second voltage control circuit F**2** may include the first unit voltage control cells F_ON**1** and F_ON**2** and the second unit voltage control cell F_OFF**1**. The second voltage control circuit F**2** may apply a second voltage V**2** different from the first voltage V**1** to the third electrodes E**3** of the second cell block CB**2**.
[0142] The third voltage control circuit F**3** may include the first unit voltage control cell F_ON**1** and the second unit voltage control cells F_OFF**1** and F_OFF**2**. The third voltage control circuit F**3** may apply a third voltage V**3** different from the first and second voltages V**1** and V**2** to the third electrodes E**3** of the third cell block CB**3**.
[0143] Depending on the distribution of the semiconductor process, optimal voltages required for the cell blocks CB may vary. Accordingly, the number of the second unit voltage control cells F_OFF**1** and F_OFF**2** in an off state, among the unit voltage control cells F_ON**1**, F_ON**2**, F_ON**3**, F_OFF**1** and F_OFF**2** of the voltage control circuits FC may vary, depending on the optimal voltages required for the cell blocks CB. For example, the first voltage control circuit F**1** may not have a unit cell in an off state, the second voltage control circuit F**2** may include ‘m’ number of second unit voltage control cells F_OFF**1**, and the third voltage control circuit F**3** may include ‘n’ number of second unit voltage control cells F_OFF**1** and F_OFF**2**. The ‘n’ and ‘m’ may be different natural numbers. The ‘n’ may be larger than ‘m.’
[0144] During the read operation described above, an optimal offset voltage may be provided to the third electrode E**3** using the voltage control circuits FC in which the number of the second unit voltage control cells F_OFF**1** and F_OFF**2** in the off state as described above is controlled. For example, during the read operation, the first voltage V**1**, the second voltage V**2** or the third voltage V**3** may be applied to the third electrodes E**3** of the cell blocks CB using the voltage control circuits FC.
[0145] When the cell blocks CB described above are turned off, in order to provide optimal fixed voltages required for the cell blocks CB generated according to the distribution of the semiconductor process, a first fixed voltage may be applied to the second electrodes E**2** of the cell blocks CB using the fixed voltage supply circuit VP**1**, the second voltage supply circuit VP**2***b* of the variable voltage supply circuit VP**2** may provide a second fixed voltage, and the second fixed voltage provided from the second voltage supply circuit VP**2***b* may be provided as an optimal fixed voltage to the third electrodes E**3** of each of the cell blocks CB, using the voltage control circuits FC in which the number of second unit voltage control cells F_OFF**1** and F_OFF**2** is adjusted. For example, when the cell blocks CB are turned off, the first voltage V**1** may be applied to the third electrodes E**3** of the first cell block CB**1** using the voltage control circuits FC, the second voltage V**2** may be applied to the third electrodes E**3** of the second cell block CB**2**, and the third voltage V**3** may be applied to the third electrodes E**3** of the third cell block CB**3**.
[0146] In a modified example, referring to FIGS. **8**E, **8**F and **8**G along with FIGS. **7**A and **8**A, in

the voltage control circuits FC described above, each of the unit voltage control cells may further include a charge pump CP for stable pumping. For example, each of the voltage control circuits FC may include one or more unit voltage control cells F_ON**1***a*, F_ON**2***a*, F_ON**3***a*, F_OFF**1***a* and F_OFF**2***a* connected in parallel, and each of the unit voltage control cells F_ON**1***a*, F_ON**2***a*, F_ON**3***a*, F_OFF**1***a* and F_OFF**2***a* may include the capacitor Cf, the charge pump CP, the fuse Rf or Sf, and the transistor TRf connected in series.

[0147] The first voltage control circuit F**1** may include the first unit voltage control cells F_ON**1***a*, F_ON**2***a* and F_ON**3***a* in an on state. The first voltage control circuit F**1** may apply a first voltage V**1***a* to the third electrodes E**3** of the first cell block CB**1**.

[0148] The second voltage control circuit F**2** may include the first unit voltage control cells F_ON**1***a* and F_ON**2***a* in an on state and the second unit voltage control cell F_OFF**1***a* in an off state. The second voltage control circuit F**2** may apply a second voltage V**2***a* different from the first voltage V**1***a* to the third electrodes E**3** of the second cell block CB**2**.

[0149] The third voltage control circuit F**3** may include the first unit voltage control cell F_ON**1***a* in an on state and the second unit voltage control cells F_OFF**1***a* and F_OFF**2***a* in an off state. The third voltage control circuit F**3** may apply a third voltage V**3***a* different from the first and second voltages V**1***a* and V**2***a* to the third electrodes E**3** of the third cell block CB**3**.

[0150] Next, referring to FIG. **9**A along with FIGS. **1** to **5**A, examples of routing interconnection structures of a first cell block CB**1***a* and a second cell block CB**2***a* disposed adjacently to each other will now be described. FIG. **9**A is a conceptual perspective view illustrating routing interconnection structures of the first cell block CB**1***a* and the second cell block CB**2***a* disposed adjacently to each other.

[0151] In one example, referring to FIG. **9**A, along with FIGS. **2**A and **5**A, a semiconductor device **1** according to an example embodiment may include a first cell block CB**1***a* having the same structure as the cell block CB described in FIG. **2**A or the same structure as the cell block CB′ described in FIG. **4**, and a second cell block CB**2***a* having a mirror symmetrical structure to the first cell block CB**1***a*. The first electrodes E**1** of the first cell block CB**1***a* and the first electrodes E**1** of the second cell block CB**2***a* may face each other. The second electrode E**2** may be an electrode to which a fixed voltage is applied, and the third electrode E**3** may be an electrode to which a variable voltage is applied.

[0152] The first routing interconnection structure R**2***a* described in FIG. **5**A may be connected to a lower surface of the second electrode E**2** of the first cell block CB**1***a* and the lower surface of the second electrode E**2** of the second cell block CB**2***a*. The second routing interconnection structure R**3***a* described in FIG. **5**A may include a second routing interconnection structure R**3***a* connected to an upper surface of the third electrode E**3** of the first cell block CB**1***a*, and a second routing interconnection structure R**3***a* connected to the upper surface of the third electrode E**3** of the second cell block CB**2***a*. The second routing interconnection structure R**3***a* connected to the upper surface of the third electrode E**3** of the first cell block CB**1***a* and the second routing interconnection structure R**3***a* connected to the upper surface of the third electrode E**3** of the second cell block CB**2***a* may be separated from each other.

[0153] Next, referring to FIGS. **9**B, **9**C and **9**D, along with FIGS. **1** to **5**D, various modified examples of the first and second routing interconnection structures R**2***a* and R**3***a* described in FIG. **9**A will now be described. FIGS. **9**B, **9**C, and **9**D are conceptual perspective views illustrating routing interconnection structures of the first cell block CB**1***a* and the second cell block CB**2***a* disposed adjacently to each other.

[0154] In a modified example, referring to FIG. **9**B along with FIGS. **2**A and **5**B, the first routing interconnection structure R**2***a* (see FIG. **9**A) described in FIG. **9**A may be modified into a first routing interconnection structure R**2***b* connected to an upper surface of the second electrode E**2** of the first cell block CB**1***a* and an upper surface of the second electrode E**2** of the second cell block CB**2***a*. The second routing interconnection structures R**3***a* described in FIG. **9**A may be modified

into a second routing interconnection structure R**3***b* connected to a lower surface of the third electrode E**3** of the first cell block CB**1***a* and a second routing interconnection structure R**3***b* connected to a lower surface of the third electrode E**3** of the second cell block CB**2***a*.

[0155] In a modified example, referring to FIG. **9**C along with FIGS. **2**A and **5**C, as described in FIG. **9**A, the first routing interconnection structure R**2***a* may be connected to the lower surface of the second electrode E**2** of the first cell block CB**1***a* and the lower surface of the second electrode E**2** of the second cell block CB**2**, and the second routing interconnection structures R**3***a* (see FIG. **9**A) described in FIG. **9**A may be modified into a second routing interconnection structure R**3***b* connected to the lower surface of the third electrode E**3** of the first cell block CB**1***a*, and a second routing interconnection structure R**3***b* connected to the lower surface of the third electrode E**3** of the second cell block CB**2***a*.

[0156] In a modified example, referring to FIG. **9**D along with FIGS. **2**A and **5**D, the first routing interconnection structure R**2***a* (see FIG. **9**A) described in FIG. **9**A may be modified into a first routing interconnection structure R**2***b* connected to the upper surface of the second electrode E**2** of the first cell block CB**1***a* and the upper surface of the second electrode E**2** of the second cell block CB**2***a*, and as described in FIG. **9**A, the second routing interconnection structures R**3***a* may include a second routing interconnection structure R**3***a* connected to the upper surface of the third electrode E**3** of the first cell block CB**1***a*, and a second routing interconnection structure R**3***a* connected to an upper surface of the third electrode E**3** of the second cell block CB**2***a*.

[0157] In the capacitor structure C**1** (see FIG. **2**A) described above, the third electrode E**3** and the second electrode E**2** may be sequentially arranged in a direction away from the active pattern ACT, and each of the third electrodes E**3** and the second electrode E**2** may be square or substantially square, or have a shape similar to a square. For example, each of the third electrodes E**3** may have a square shape when viewed in plan view. For example, the distance from the active pattern ACT to the corresponding third electrode E**3** may be smaller than the distance from the active pattern ACT to the corresponding second electrode E**2**.

[0158] FIGS. **10**A to **10**I are plan views illustrating various examples of a planar shape of the capacitor structure C**1** (see FIG. **2**A) described above. Hereinafter, elements referred to by symbols different from symbols described above, but referred to by the same term, may differ only in planar shape, and may play the same role as each other. In a modified example, referring to FIG. **10**A, the capacitor structure C**1** (see FIG. **2**A) may be modified into a capacitor structure CAPa as in FIG. **10**A. For example, the first electrode E**1** (see FIG. **2**A) in FIG. **2**A may be modified into a first electrode E**1***a* having a width larger than the first source/drain region SD**1**, and the second electrode E**2** (see FIG. **2**A) in FIG. **2**A may be modified into a second electrode E**2***a* disposed adjacently to the first source/drain region SD**1**, the third electrode E**3** (see FIG. **2**A) in FIG. **2**A may be modified into a third electrode E**3***a* disposed in a position farther away from the first source/drain region SD**1** than the second electrode E**2***a*, the first dielectric layer Dia**1** in FIG. **2**A may be modified into a first dielectric layer Dia**1***a* disposed between the first electrode E**1***a* and the second electrode E**2***a*, and the second dielectric layer Dia**2** in FIG. **2**A may be modified into a second dielectric layer Dia**2***a* disposed between the first electrode E**1***a* and the third electrode E**3***a*. Each of the second electrode E**2***a* and the third electrode E**3***a* may be circular or substantially circular, or have a shape similar to a circle.

[0159] Each of the active patterns ACT (see FIGS. **2**A and **2**B) including the first source/drain region SD**1** may have a bar shape extending in the first horizontal direction (X-direction), and each of the active patterns ACT (see FIGS. **2**A and **2**B) may have a first width in the second horizontal direction (Y-direction), and the first electrode E**1***a* may have a second width larger than the first width in the second horizontal direction (Y-direction). The second electrode E**2***a* and the third electrode E**3***a* may be sequentially arranged in the first horizontal direction (X-direction).

[0160] In a modified example, referring to FIG. **10**B, the capacitor structure C**1** (see FIG. **2**A) may be modified into a capacitor structure CAPb as in FIG. **10**B. For example, the first electrode E**1**

(see FIG. **2**A) in FIG. **2**A may be modified into a first electrode E**1***b* having a width larger than the first source/drain region SD**1**, the second electrode E**2** (see FIG. **2**A) in FIG. **2**A may be modified into a second electrode E**2***b* with an increased planar area, the third electrode E**3** (see FIG. **2**A) in FIG. **2**A may be modified into a third electrode E**3***b* with a reduced planar area, the first dielectric layer Dia**1** in FIG. **2**A may be modified into a first dielectric layer Dia**1***b* disposed between the first electrode E**1***b* and the second electrode E**2***b*, and the second dielectric layer Dia**2** in FIG. **2**A may be modified into a second dielectric layer Dia**2***b* disposed between the first electrode E**1***b* and the third electrode E**3***b*.

[0161] At the same level as the active pattern ACT (see FIGS. **2**A and **2**B), when viewed from top view (e.g., plan view), a planar area of the second electrode E**2***b* may be different from a planar area of the third electrode E**3***b*. For example, at the same level as the active pattern ACT (see FIGS. **2**A and **2**B), when viewed from top view, the planar area of the second electrode E**2***b* may be larger than the planar area of the third electrode E**3***b*. For example, the planar area of the third electrode E**3***b* may be about 0.1 to 0.8 times the planar area of the second electrode E**2***b*. The planar area of the third electrode E**3***b* may be about 0.3 to 0.6 times the planar area of the second electrode E**2***b*.

[0162] The second electrode E**2***b* may be disposed between the third electrode E**3***b* and the first source/drain region SD**1**, but the inventive concept is not limited thereto. For example, the third electrode E**3***b* may be modified to be disposed between the second electrode E**2***b* and the first source/drain region SD**1**.

[0163] In a modified example, referring to FIG. **10**C, the capacitor structure CAPb (see FIG. **10**B) in FIG. **10**B may be modified into a capacitor structure CAPc as in FIG. **10**C. For example, the first electrode E**1** (see FIG. **2**A) in FIG. **2**A may be modified into a first electrode E**1***c* having a width larger than the first source/drain region SD**1**, and the second electrode E**2***b* (see FIG. **10**B) in FIG. **10**B may be modified into a second electrode E**2***c* including a plurality of second electrode patterns E**2***c***1**, E**2***c***2** and E**2***c***3** spaced apart from each other. The third electrode E**3***b* (see FIG. **10**B) in FIG. **10**C may be modified into a third electrode E**3***c* including a plurality of third electrode patterns E**3***cl* and E**3***c***2** spaced apart from each other. The first dielectric layer Dia**1***b* in FIG. **10**B may be modified into a first dielectric layer Dia**1***c* disposed between the first electrode E**1***c* and the plurality of second electrode patterns E**2***c***1**, E**2***c***2** and E**2***c***3**, and the second dielectric layer Dia**2***b* in FIG. **10**B may be modified into a second dielectric layer Dia**2***c* disposed between the first electrode E**1***c* and the plurality of third electrode patterns E**3***cl* and E**3***c***2**.

[0164] Each of the plurality of second electrode patterns E**2***c***1**, E**2***c***2** and E**2***c***3** and the plurality of third electrode patterns E**3***cl* and E**3***c***2** may be a bar shape extending in the second horizontal direction (Y-direction).

[0165] The plurality of second electrode patterns E**2***c***1**, E**2***c***2** and E**2***c***3** and the plurality of third electrode patterns E**3***cl* and E**3***c***2** may have the same size as each other.

[0166] The number of the plurality of second electrode patterns E**2***c***1**, E**2***c***2** and E**2***c***3** may be greater than the number of the plurality of third electrode patterns E**3***cl* and E**3***c***2**.

[0167] In a modified example, referring to FIG. **10**D, the capacitor structure CAPb (see FIG. **10**B) in FIG. **10**B may be modified into a capacitor structure CAPd as in FIG. **10**D. For example, the first electrode E**1** (see FIG. **2**A) in FIG. **2**A may be modified into a first electrode E**1***d* having a width larger than the first source/drain region SD**1**. The second electrode E**2***b* (FIG. **10**B) in FIG. **10**B may be modified into a second electrode E**2***d* including a plurality of second electrode patterns spaced apart from each other. The third electrode E**3***b* (see FIG. **10**B) in FIG. **10**C may be modified into a third electrode E**3***d* including a plurality of third electrode patterns spaced apart from each other. The first dielectric layer Dia**1***b* in FIG. **10**B may be modified into a first dielectric layer Dia**1***d* disposed between the first electrode E**1***d* and a plurality of second electrode patterns of the second electrode E**2***d*, and the second dielectric layer Dia**2***b* in FIG. **10**B may be modified into a second dielectric layer Dia**2***d* disposed between the first electrode E**1***d* and the plurality of third electrode patterns of the third electrode E**3***d*.

[0168] The plurality of second electrode patterns of the second electrode E**2***d* and the plurality of third electrode patterns of the third electrode E**3***d* may be the same size as each other.
[0169] Each of the plurality of second electrode patterns of the second electrode E**2***d* and the plurality of third electrode patterns of the third electrode E**3***d* may be substantially circular or substantially square in shape.
[0170] The electrode patterns of the second and third electrodes E**2***d* and E**3***d* may be arranged in the first horizontal direction (X-direction) while crossing in the second horizontal direction (Y-direction).
[0171] The number of second electrode patterns of the second electrode E**2***d* may be greater than the number of third electrode patterns of the third electrode E**3***d*.
[0172] In a modified example, referring to FIG. **10**E, the capacitor structure C**1** (see FIG. **2**A) may be modified into a capacitor structure CAPe as in FIG. **10**E. For example, the first electrode E**1** (see FIG. **2**A) in FIG. **2**A may be modified into a first electrode E**1***e* having a width larger than the first source/drain region SD**1**, the second electrode E**2** (see FIG. **2**A) in FIG. **2**A may be modified into a bar-shaped second electrode E**2***e* extending in the first horizontal direction (X-direction), the third electrode E**3** (see FIG. **2**A) in FIG. **2**A may be modified into a bar-shaped third electrode E**3***e* extending in the first horizontal direction (X-direction), the first dielectric layer Dia**1** in FIG. **2**A may be modified into a first dielectric layer Dia**1***e* disposed between the first electrode E**1***e* and the second electrode E**2***e*, and the second dielectric layer Dia**2** in FIG. **2**A may be modified into a second dielectric layer Dia**2***e* disposed between the first electrode E**1***e* and the third electrode E**3***e*.
[0173] The second electrode E**2***e* and the third electrode E**3***e* may be sequentially arranged in the second horizontal direction (Y-direction).
[0174] In a modified example, referring to FIG. **10**F, the capacitor structure CAPb (see FIG. **10**B) may be modified into a capacitor structure CAPf as in FIG. **10**F. For example, the first electrode E**1** (see FIG. **2**A) in FIG. **2**A may be modified into a first electrode E**1***f* having a width larger than the first source/drain region SD**1**, the second electrode E**2***b* (see FIG. **10**B) in FIG. **10**B may be modified into a bar-shaped second electrode E**2***f* extending in the first horizontal direction (X-direction), and the third electrode E**3***b* (see FIG. **10**B) in FIG. **10**B may be modified into a bar-shaped third electrode E**3***f* extending in the first horizontal direction (X-direction). The first dielectric layer Dia**1***b* in FIG. **10**B may be modified into a first dielectric layer Dia**1***f* disposed between the first electrode E**1***f* and the second electrode E**2***f*, and the second dielectric layer Dia**2***b* in FIG. **10**B may be modified into a second dielectric layer Dia**2***f* disposed between the first electrode E**1***f* and the third electrode E**3***f*.
[0175] The third electrode E**2***f* and the second electrode E**2***f* may be sequentially arranged in the second horizontal direction (Y-direction). As described in FIG. **10**B, a planar area of the third electrode E**2***f* may be larger than a planar area of the second electrode E**2***f*.
[0176] In a modified example, referring to FIG. **10**G, the capacitor structure CAPe (see FIG. **10**E) may be modified into a capacitor structure CAPg as in FIG. **10**G. The first electrode E**1** (see FIG. **2**A) in FIG. **2**A may be modified into a first electrode E**1***g* having a width larger than the first source/drain region SD**1**. The second electrode E**2***e* (see FIG. **10**E) in FIG. **10**E may be modified into a second electrode E**2***g* including a plurality of second electrode patterns spaced apart from each other. A third electrode E**3***g* having a similar shape as the third electrode E**3***e* (see FIG. **10**E) in FIG. **10**E may be provided. The first dielectric layer Dia**1***e* in FIG. **10**E may be modified into a first dielectric layer Dia**1***g* disposed between the first electrode E**1***g* and a plurality of second electrode patterns of the second electrode E**2***g*, and the second dielectric layer Dia**2***e* in FIG. **10**E may be modified into a second dielectric layer Dia**2***g* disposed between the first electrode E**1***g* and the third electrode E**3***g*.
[0177] The electrode patterns of the second electrode E**2***g* may be sequentially arranged in the second horizontal direction (Y-direction). The third electrode E**3***g* and the second electrode E**2***g* may be sequentially arranged in the second horizontal direction (Y-direction). Each of the electrode

patterns of the second electrode E**2***g* and the third electrode E**3***g* may be in a shape of a line extending in the first horizontal direction (X-direction). The electrode patterns of the second electrode E**2***g* and the third electrode E**3***g* may have substantially the same size.

[0178] In a modified example, referring to FIG. **10**H, the capacitor structure C**1** (See FIG. **2**A) may be modified into a capacitor structure CAPh as in FIG. **10**H. For example, the first electrode E**1** (see FIG. **2**A) in FIG. **2**A may be modified into a first electrode E**1***h* having a width larger than the first source/drain region SD**1**, the second electrode E**2** (see FIG. **2**A) in FIG. **2**A may be modified into a bar-shaped second electrode E**2***h* extending in the first horizontal direction (X-direction), the third electrode E**3** (see FIG. **2**A) in FIG. **2**A may be modified into a bar-shaped third electrode E**3***h* extending in the first horizontal direction (X-direction), the first dielectric layer Dia**1** in FIG. **2**A may be modified into a first dielectric layer Dia**1***h* disposed between the first electrode E**1***h* and the second electrode E**2***h*, and the second dielectric layer Dia**2** in FIG. **2**A may be modified into a second dielectric layer Dia**2***h* disposed between the first electrode E**1***h* and the third electrode E**3***h*. The first dielectric layer Dia**1***h* and the second dielectric layer Dia**2***h* may contact each other or may be continuously formed of a single material.

[0179] The capacitor structure CAPh may further include an insulating separation pattern SP disposed between the second electrode E**2***h* and the third electrode E**3***h* separating the second electrode E**2***h* and the third electrode E**3***h* from each other. The insulating separation pattern SP may be in contact with the second electrode E**2***h* and the third electrode E**3***h* between the second electrode E**2***h* and the third electrode E**3***h*.

[0180] In a modified example, referring to FIG. **10**I, the first source/drain region described in the example embodiments described in FIGS. **1** to **10**H may be modified into a first source/drain region SD**1***a* extending to surround a side surface of the first electrode described in the example embodiments described in FIGS. **1** to **10**H. For example, the first source/drain region SD**1** in FIG. **10**H may be modified into the first source/drain region SD**1***a* extending to surround a side surface of the first electrode E**1***h* of the capacitor structure CAPh (see FIG. **10***h*) described in FIG. **10**H. An entire side surface of the first electrode E**1***h* may be surrounded by the first source/drain region SD**1***a*.

[0181] Next, an example of a method of forming a semiconductor device according to an example embodiment of the present disclosure will be described with reference to FIGS. **11**A to **11**D. FIGS. **11**A to **11**D are perspective views illustrating a portion of a region in which the capacitor structure is to be formed, to describe a method of forming the capacitor structure in the previously described example embodiments.

[0182] Referring to FIG. **11**A, a stack structure **115** may be formed on a first region A**1** and a second region A**2**. A semiconductor process may be performed on the stack structure **115** on the first region A**1**, thus forming a structure ST including the active patterns ACT, the word lines WL, the gate dielectric layers Gox, and the bit lines BL described in the example embodiments of FIGS. **1** to **10**I.

[0183] The stack structure **115** may include first layers **105** and second layers **110** that are alternately stacked. The first layers **105** may be interlayer insulating layers. The second layers **110** may be formed of the same material as the active patterns ACT. For example, the second layers **110** may be silicon layers. In another example, the second layers **110** of the stack structure **115** on the first region A**1** and the second layers **110** of the stack structure **115** on the second region A**2** may be formed from layers of different materials. For example, by an ion implantation process, the second layers **110** of the stack structure **115** on the first region A**1** may be formed of a semiconductor layer such as a silicon layer, and the second layers **110** of the stack structure **115** on the second region A**2** may be formed of an insulating layer such as silicon nitride.

[0184] Referring to FIG. **11**B, a semiconductor process may be performed on the stack structure **115** on the second region A**2**, thus forming first insulating patterns **120** defining side surfaces opposite to each other in the second horizontal direction (Y-direction) and a second insulating

pattern **125** defining a side surface spaced apart from the first region A**1** in the first horizontal direction (X-direction).
[0185] In one example, the first insulating patterns **120** and the second insulating pattern **125** may be formed in the same process.
[0186] In another example, the first insulating patterns **120** and the second insulating pattern **125** may be formed in different processes.
[0187] Referring to FIG. **11**C, a plurality of openings **130***a* and **130***b* spaced apart from each other may be formed by penetrating through the stack structure **115** on the second region A**2**. The plurality of openings **130***a* and **130***b* may include a first opening **130***a* and a second opening **130***b*.
[0188] The planar shapes of the plurality of openings **130***a* and **130***b* may be substantially the same as the planar shapes of the elements referred to as the "second electrode" and "third electrode" described above. According to an example embodiment, the first opening **130***a* may have a larger planar area than the second opening **130***b*. Referring to FIG. **11**D, the second layers **110** (see FIG. **11**A) exposed by the first and second openings **130***a* and **130***b* may be selectively removed to expose the active patterns ACT (see FIGS. **2**A and **2**B) of the structure ST. Next, impurities may be injected into the active patterns ACT (see FIGS. **2**A and **2**B) of the structure ST, thus forming first source/drain regions SD**1** as described above. Then, first electrodes E**1***i* may be formed in spaces from which the second layers **110** (see FIG. **11**A) are removed. dielectric layers Dia**1***i* and Dia**2***i* may be formed on sidewalls of the first and second openings **130***a* and **130***b*, and conductive material layers D**2***i* and D**3***i* filling the first and second openings **130***a* and **130***b* may be formed.
[0189] The dielectric layers Dia**1***i* and Dia**2***i* may cover side surfaces of the first electrodes E**1***i* exposed by the first and second openings **130***a* and **130***b*. The dielectric layers Dia**1***i* and Dia**2***i* may include a first dielectric layer Dia**1***i* in the first opening **130***a* and a second dielectric layer Dia**2***i* in the second opening **130***b*. The conductive material layers D**2***i* and D**3***i* may include a second electrode D**2***i* in the first opening **130***a* and a third electrode D**3***i* in the second opening **130***b*. Accordingly, a capacitor structure CAPi including the first to third electrodes E**1***i*, E**2***i* and E**3***i* and the first and second dielectric layers Dia**1***i* and Dia**2***i* may be formed.
[0190] Next, an example of a method of forming a semiconductor device according to an example embodiment of the present disclosure will be described with reference to FIGS. **12**A to **12**G. FIGS. **12**A to **12**G are views illustrating a portion of a region in which the capacitor structure is to be formed, to describe the method of forming the capacitor structure in the previously described example embodiments. FIG. **12**A is a perspective view illustrating a partial region in which the capacitor structure is to be formed, and FIGS. **12**B to **12**G are cross-sectional views illustrating a region taken along line I-I′ of FIG. **12**A.
[0191] Referring to FIGS. **12**A and **12**B, as described in FIG. **11**A, the stack structure **115** may be formed on the first region A**1** and the second region A**2**, and a semiconductor process may be performed on the stack structure **115** on the first region A**1**, thus forming the structure ST. As described in FIG. **11**B, a semiconductor process may be performed on the stack structure **115** on the second region A**2**, thus forming the first insulating patterns **120** and the second insulating pattern **125**. An opening **230** penetrating through the stack structure **115** may be formed on the second region A**2**. Side surfaces of the first layers **105** and the second layers **110** of the stack structure **115** may be exposed through the opening **230**.
[0192] Referring to FIGS. **12**C and **12**D, the first layers **105** exposed by the opening **230** may be isotropically etched to form first recessed regions **105***s* recessed at a first depth. The second layers **110** exposed by the opening **230** may be isotropically etched so that second recessed regions **110***s* recessed at a second depth deeper than the first depth may be formed.
[0193] In an example embodiment, when the second layers **110** are formed of a semiconductor material, the second recessed regions **110***s* may be formed, and then, the second layers **110** may remain. By injecting impurities into the second layers **110** and the active patterns ACT (see FIGS. **2**A and **2**B) of the structure ST, a first source/drain region SD**1***a* (see FIG. **10**I) may be formed as

described in FIG. **10**I.
[0194] In another example embodiment, when the second layers **110** are formed of an insulating material such as silicon nitride, the second layers **110** may be removed to expose the first and second insulating patterns **120** and **125** and the active patterns ACT (see FIGS. **2**A and **2**B) of the structure ST, thus forming the second recessed regions **110***s*. Next, impurities may be injected into the active patterns ACT (see FIGS. **2**A and **2**B) of the structure ST, thus forming the first source/drain region SD**1** (see FIG. **10***h*) as illustrated in FIG. **10**H.
[0195] Hereinafter, a case in which the second layers **110** remain will be described, but the inventive concept is not limited thereto. For example, even when the second layers **110** are removed, the same process may be performed later.
[0196] Referring to FIG. **12**E, conductive patterns **240** and **245** may be formed on side surfaces of the first recessed regions **105***s* and side surfaces of the second recessed regions **110***s*. Because the side surfaces of the first recessed regions **105***s* and the side surfaces of the second recessed regions **110***s* have curved surfaces, when a conductive material layer may be deposited thereon and the conductive material layer may then be etch-backed, the conductive material layer remains on the side surfaces of the first recessed regions **105***s* and the side surfaces of the second recessed regions **110***s*, thereby forming the conductive patterns **240** and **245**.
[0197] The conductive patterns **240** and **245** may include dummy conductive patterns **240** formed on side surfaces of the first recessed regions **105***s*, and first electrodes **245** formed on side surfaces of the second recessed regions **110***s*. The first electrodes **245** may be the first electrodes E**1***h* described in FIGS. **10**H and **10**I.
[0198] Referring to FIG. **12**F, a dielectric layer **250** covering the conductive patterns **240** and **245** may be formed, and a conductive material layer **260** filling the first and second recessed regions **105***s* and **110***s* and filling the opening **230** (see FIG. **12**E) may be formed on the dielectric layer **250**.
[0199] Referring to FIG. **12**G, an insulating separation pattern **270** penetrating through the conductive material layer **260** may be formed. The conductive material layer **260** may be formed of a second electrode **260***a* and a third electrode **260***b* spaced apart from each other by the insulating separation pattern **270**. The dielectric layer **250** may include a first dielectric layer **250***a* remaining between the second electrode **260***a* and the first electrodes **245** and between the second electrode **260***a* and the dummy conductive patterns **240**, and a second dielectric layer **250***b* remaining between the third electrode **260***b* and the first electrodes **245**, and between the third electrode **260***b* and the dummy conductive patterns **240**.
[0200] The second electrode **260***a* may be the second electrode E**2***h* described in FIGS. **10**H and **10**I, the third electrode **260***b* may be the third electrode E**3***h* described in FIGS. **10**H and **10**I, and the insulating separation pattern **270** may be the insulating separation pattern SP described in FIGS. **10**H and **10**I. A semiconductor device including the capacitor structure CAPh described in FIGS. **10**H and **10**I may include the first layers **105** as in FIG. **12**G, and the dummy conductive patterns **240**.
[0201] Although example embodiments of the present disclosure have been described with reference to the accompanying drawings, it will be understood by those skilled in the art that the present disclosure may be implemented in other specific forms without changing its technical concepts or essential features. Therefore, it should be understood that the example embodiments described above are exemplary and not limited in all respects.

Claims

1. A semiconductor device comprising: active patterns stacked and spaced apart from each other in a vertical direction; and a capacitor connected to the active patterns, wherein the capacitor includes: first electrodes respectively connected to the active patterns and stacked and spaced apart from

each other in the vertical direction; a second electrode penetrating through the first electrodes and extending in the vertical direction; a third electrode penetrating through the first electrodes and extending in the vertical direction, and spaced apart from the second electrode; first dielectric layers, each first dielectric layer being between a respective first electrode and the second electrode; and second dielectric layers, each second dielectric layer being between a respective first electrode and the third electrode.

2. The semiconductor device of claim 1, wherein each of the second electrode and the third electrode has a lower surface at a lower level than a lowermost active pattern among the active patterns, and an upper surface at a higher level than an uppermost active pattern among the active patterns.

3. The semiconductor device of claim 1, wherein at the same height level as one first electrode of the first electrodes, a planar area in plan view of the second electrode is different from a planar area in plan view of the third electrode.

4. The semiconductor device of claim 1, wherein the second electrode includes a plurality of second electrode patterns penetrating through the first electrodes in the vertical direction and spaced apart from each other.

5. The semiconductor device of claim 4, wherein the third electrode includes a plurality of third electrode patterns penetrating through the first electrodes in the vertical direction and spaced apart from each other.

6. The semiconductor device of claim 5, wherein the number of the plurality of second electrode patterns is greater than the number of the plurality of third electrode patterns.

7. The semiconductor device of claim 1, wherein each of the second electrode and the third electrode has a bar shape extending in a horizontal direction perpendicular to the vertical direction.

8. The semiconductor device of claim 1, wherein each of the active patterns has a bar shape extending in a first horizontal direction, wherein each of the active patterns has a first width in a second horizontal direction perpendicular to the first horizontal direction, and wherein each of the first electrodes has a second width greater than the first width in the second horizontal direction.

9. The semiconductor device of claim 1, wherein each of the active patterns has a bar shape extending in a first horizontal direction, and wherein the second electrode and the third electrode are sequentially arranged in the first horizontal direction.

10. The semiconductor device of claim 1, wherein each of the active patterns has a bar shape extending in a first horizontal direction, and wherein the second electrode and the third electrode are sequentially arranged in a second horizontal direction perpendicular to the first horizontal direction.

11. The semiconductor device of claim 1, wherein each of the active patterns has a bar shape extending in a first horizontal direction, wherein each of the active patterns includes a first source/drain region, a second source/drain region, and a channel region between the first source/drain region and the second source/drain region, and wherein the first electrodes are connected to the first source/drain regions of the active patterns.

12. The semiconductor device of claim 11, further comprising: a bit line connected to the second source/drain region of each of the active patterns, the bit line extending in the vertical direction; and a word line vertically overlapping the channel region of each of the active patterns, the word line extending in a second horizontal direction perpendicular to the first horizontal direction.

13. The semiconductor device of claim 11, further comprising: bit lines, each bit line being connected to the second source/drain region of a corresponding active pattern, and each bit line extending in a second horizontal direction perpendicular to the first horizontal direction; and a word line including a vertical portion extending in the vertical direction, and protruding portions extending from the vertical portion, wherein each protruding portion vertically overlaps the channel region of a corresponding active pattern.

14. A semiconductor device comprising: a peripheral circuit region including a peripheral circuit;

and a memory region on the peripheral circuit region and including cell blocks, wherein each of the cell blocks includes cell transistors and a data storage structure connected to first source/drain regions of the cell transistors, wherein the data storage structure of each of the cell blocks includes: first electrodes respectively connected to the first source/drain regions of the cell transistors, the first electrodes being stacked and spaced apart from each other in a vertical direction; a second electrode having a side surface facing the first electrodes; and a third electrode having a side surface facing the first electrodes and spaced apart from the second electrode, and wherein the peripheral circuit includes: a fixed voltage supply circuit configured to apply a fixed voltage to the second electrode; a write circuit configured to perform a write operation for storing “1” or “0” data in a unit memory cell of the cell blocks; and a variable voltage supply circuit configured to, during the write operation for storing data “1” in the unit memory cell, apply a positive voltage to the third electrode, and to, during the write operation for storing “0” data in the unit memory cell, apply a negative voltage to the third electrode.

15. The semiconductor device of claim 14, further comprising: a first routing interconnection structure electrically connecting the second electrode to the fixed voltage supply circuit; and a second routing interconnection structure electrically connecting the third electrode to the variable voltage supply circuit.

16. The semiconductor device of claim 15, wherein the first routing interconnection structure is connected to a lower surface of the second electrode, and wherein the second routing interconnection structure is connected to an upper surface of the third electrode.

17. The semiconductor device of claim 15, wherein the first routing interconnection structure is connected to an upper surface of the second electrode, and wherein the second routing interconnection structure is connected to a lower surface of the third electrode.

18. The semiconductor device of claim 15, wherein the peripheral circuit further includes a read circuit and voltage control circuits, the read circuit being configured to read data stored in the unit memory cell, wherein the cell blocks include a first cell block and a second cell block, wherein the voltage control circuits include a first voltage control circuit configured to apply a first voltage to the third electrode of the first cell block and a second voltage control circuit configured to apply a second voltage to the third electrode of the second cell block, wherein each of the first voltage control circuit and the second voltage control circuit includes unit voltage control cells connected in parallel, wherein each of the unit voltage control cells includes a capacitor, a fuse, and a transistor connected in series, wherein the unit voltage control cells of the first voltage control circuit include ‘m’ unit voltage control cells in an off state, wherein the unit voltage control cells of the second voltage control circuit include ‘n’ unit voltage control cells in an off state, and wherein ‘n’ and ‘m’ are different natural numbers.

19. A semiconductor device comprising: active patterns stacked and spaced apart from each other in a vertical direction; and a data storage structure connected to the active patterns, wherein the data storage structure includes: first electrodes respectively connected to the active patterns, the first electrodes being stacked and spaced apart from each other in the vertical direction; a second electrode having a side surface facing the first electrodes; a third electrode having a side surface facing the first electrodes and spaced apart from the second electrode; first dielectric layers between respective first electrodes and the second electrode; and second dielectric layers between respective first electrodes and the third electrode.

20. The semiconductor device of claim 19, further comprising: a first routing interconnection structure connected to an upper surface of the second electrode; and a second routing interconnection structure connected to a lower surface of the third electrode.