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RESISTIVE RANDOM ACCESS MEMORY

Abstract

A resistive random access memory is provided. The resistive random access memory includes a conductive line structure and a memory unit. The conductive line structure is disposed in an array area and a periphery circuit area. The memory unit is disposed on the conductive line structure in the array area. The memory unit includes a lower electrode, a resistive switching layer, and an upper electrode. The lower electrode is disposed on the conductive line structure. The resistive switching layer is disposed on the lower electrode. The upper electrode is disposed on the resistive switching layer. The upper surface of the conductive line structure is in direct contact with the lower electrode.

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Background/Summary

CROSS REFERENCE TO RELATED APPLICATIONS [0001] This application is a Divisional of pending U.S. patent application Ser. No. 17/571,149, filed on Jan. 7, 2022, the entirety of which is incorporated by reference herein.

BACKGROUND
Technical Field
[0002] The present disclosure relates to semiconductor manufacturing techniques, and in particular it relates to a resistive random access memory.
Description of the Related Art
[0003] Resistive random access memory (RRAM) has the advantages of fast computing speeds, low power consumption, and the like, and is an ideal choice as the non-volatile memory for the next generation. RRAM is configured with a transition metal oxide (TMO) layer between two metal electrodes, and the RRAM undergoes electrical switching between a high resistance state (HRS) and a low resistance state (LRS) by changing the state of conductive filaments in the transition metal oxide layer.
[0004] However, the forming operation of RRAM depends on the series resistance in the device, and the magnitude of the external resistance can affect how much potential is distributed to the memory unit when a bias is applied to the entire RRAM. The conductive line structure and the memory unit of the conventional RRAM are not in direct contact with each other, and there are other conductive structures (such as vias) between the conductive line structure and the memory unit that provide higher contact resistance in the entire RRAM. This configuration makes the RRAM unable to perform the forming operation well (for example, the current difference between the high resistance state and the low resistance state during the forming operation of is too small), which may cause the RRAM to fail to switch properly.
BRIEF SUMMARY
[0005] The present disclosure provides a resistive random access memory which includes a conductive line structure and a memory unit. The conductive line structure is disposed in an array area and a periphery circuit area, respectively. The memory unit is disposed on the conductive line structure in the array area. The memory unit includes a lower electrode, a resistive switching layer, and an upper electrode. The lower electrode is disposed on the conductive line structure. The resistive switching layer is disposed on the lower electrode. The upper electrode is disposed on the resistive switching layer. An upper surface of the conductive line structure is in direct contact with the lower electrode.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0006] FIGS. **1**A˜**1**H illustrate cross-sectional views of a resistive random access memory in a manufacturing process, in accordance with some embodiments of the present disclosure.
[0007] FIGS. **2**A and **2**B illustrate cross-sectional views of the resistive random access memory in a manufacturing process following FIG. **1**H, in accordance with a first implementation of the present disclosure.
[0008] FIGS. **3**A and **3**B illustrate cross-sectional views of the resistive random access memory in a manufacturing process following FIG. **1**H, in accordance with a second implementation of the present disclosure.

DETAILED DESCRIPTION

[0009] The present disclosure provides a resistive random access memory, wherein a conductive line structure is in contact with a memory unit directly without going through a via, thereby this can reduce the series resistance within the resistive random access memory. As a result, since a forming operation may be performed well on the resulted resistive random access memory, it can be ensured that the resulted resistive random access memory has improved yield and performance. Moreover, since the formation of other conductive structures (such as vias) is omitted between the conductive line structure and the memory unit, while reducing the contact resistance within the resistive random access memory, it also simplifies the manufacturing process and reduces the cost. It is understood that the term "conductive line structure" in the text refers to one or more layers of conductive lines extending horizontally, but does not include vias or plugs extending vertically.

[0010] As shown in FIG. **1**A, a semiconductor structure **100** includes an array area **100**A and a periphery circuit area **100**B divided by a divider **101**, and a dielectric layer **102** is formed in both the array area **100**A and the periphery circuit area **100**B.

[0011] The material of the dielectric layer **102** includes an oxide, an nitride, a low-k dielectric material with a dielectric constant lower than about 3.9 or an extreme low-k (ELK) dielectric material with a dielectric constant lower than about 2, or a combination thereof. Specifically, the material of the dielectric layer **102** is, for example, silicon oxide, silicon oxynitride, phosphosilicate glass (PSG), borosilicate glass (BSG), borophosphosilicate glass (BPSG), undoped silicate glass (USG), fluorinated silicate glass (FSG), other suitable materials, or a combination thereof.

[0012] Then, a contact plug **104** may be formed in the dielectric layer **102** in the array area **100**A and/or the periphery circuit area **100**B, wherein the contact plug **104** in the array area **100**A may electrically connect a subsequently formed resistive random access memory (such as resistive random access memory **200** or **300**) to an underlying control element (not shown) for applying a bias. For example, the control element may be a transistor, and the contact plug **104** in the array area **100**A may be electrically connected to a drain of the transistor. The contact plug **104** may include, for example, copper, tungsten, titanium, titanium nitride, aluminum, ruthenium, molybdenum, cobalt, other suitable conductive materials, or a combination thereof.

[0013] A masking layer (not shown) is disposed on the dielectric layer **102** and used as an etching mask to perform an etching process, thereby etching a contact opening in the dielectric layer **102**. Then, the material of the contact plug **104** is filled into the opening, and a planarization process is performed to form the contact plug **104**. For example, the masking layer may include a photoresist, such as a positive photoresist or a negative photoresist. The masking layer may include a hard mask, and may be formed of silicon oxide, silicon nitride, silicon oxynitride, silicon carbide, silicon carbonitride, similar materials or a combination thereof. The masking layer may be a single-layered or a multi-layered structure. The method for forming the masking layer may include a deposition process, a photolithography process, or the like. The aforementioned etching process may include a dry etching process, a wet etching process or a combination thereof. The method of filling the material of the contact plug **104** into the opening may include a physical vapor deposition (PVD) process, a chemical vapor deposition (CVD) process, an atomic layer deposition (ALD) process, evaporation or any suitable deposition processes. The material of the contact plug **104** may include copper, aluminum, tungsten or any suitable conductive materials.

[0014] Then, a lower conductive material layer **106** and an adhesion material layer **108** may be formed sequentially over the dielectric layer **102**. By forming the adhesion material layer **108** on the lower conductive material layer **106**, the adhesion or work function properties between the lower conductive material layer **106** and overlying conductive materials may be adjusted. The material of the lower conductive material layer **106** may include, for example, aluminum or other suitable conductive materials, and the material of the adhesion material layer **108** may include, for example, titanium, titanium nitride, other suitable materials, or a combination thereof. The method for forming the lower conductive material layer **106** and the adhesion material layer **108** may

include PVD, CVD, ALD, e-beam evaporation, plating, or other suitable methods, or a combination thereof.

[0015] In some embodiments, the adhesion material layer **108** is a multi-layered structure. For example, the formation of the adhesion material layer **108** may include forming a titanium layer on the lower conductive material layer **106** and forming a titanium nitride layer on the titanium layer. It should be noted that although not illustrated, an adhesion material layer may also be formed between the contact plug **104** and the lower conductive material layer **106**, thereby adjusting the adhesion or work function properties between the contact plug **104** and the lower conductive material layer **106**.

[0016] Then, a masking material layer **110** may be formed over the lower conductive layer **106** and the adhesion material layer **108**. The masking material layer **110** may include a material similar to the aforementioned masking layer. The method for forming the masking material layer **110** may include a CVD process, an ALD process, or any suitable deposition processes. In some embodiments, the masking material layer **110** may be formed using a nitride including silicon nitride, silicon oxynitride, silicon carbonitride, or a combination thereof. As a result, a mask formed with the above nitride (such as a patterned mask **112** in FIG. **1**C) may be removed by wet etching in a following process.

[0017] Referring to FIG. **1**B, after forming the masking material layer **110**, a portion of the masking material layer **110** may be removed by performing an etching process to form a patterned mask **112**, wherein the etching process may include a dry etching process, a wet etching process or a combination thereof. In some embodiments, the formed patterned mask **112** corresponds to the position of the underlying contact plug **104**.

[0018] Referring to FIG. **1**C, the patterned mask **112** is used as an etching mask, and the underlying adhesion material layer **108** and lower conductive material layer **106** are etched sequentially to form an adhesion layer **116** and a lower conductive layer **114**, respectively. The etching process may include a dry etching process, a wet etching process or a combination thereof. Depending on the conditions of the etching process, in some embodiments, the formed lower conductive layer **114** and the adhesion layer **116** have inclined sidewalls, and the lower conductive layer **114** has an average width wider than the adhesion layer **116**. As shown in FIG. **1**C, the lower conductive layer **114** and the adhesion layer **116** have cross-sections that taper upward. In some embodiments, the lower conductive layer **114** and the adhesion layer **116** are a portion of the conductive line structure of the subsequently formed resistive random access memory.

[0019] Referring to FIG. **1**D, after forming the lower conductive layer **114** and the adhesion layer **116**, another dielectric layer **102′** may be deposited on the semiconductor structure **100**. The dielectric layer **102′** forms a dielectric layer **103** together with the underlying dielectric layer **102**, wherein the dielectric layer **103** includes the material of the previously formed dielectric layer **102** and the material of the dielectric layer **102′** deposited on the dielectric layer **102**. Since the material and the forming method of the dielectric layer **102′** may be similar to that of the dielectric layer **102**, the detailed description is omitted herein for the sake of brevity. As shown in FIG. **1**D, the dielectric layer **103** may fill the spaces surrounding the lower conductive layers **114** and cover the lower conductive layer **114**, the adhesion layer **116**, and the patterned mask **112**. In some embodiments, if the desired conductive line structure has a shorter pitch, high density plasma chemical vapor deposition (HDP-CVD) may be performed to fill the dielectric layer **103**, which prevents voids from being generated in the spaces between the lower conductive layers **114**.

[0020] Referring to FIG. **1**E, after forming the dielectric layer **103**, to remove excess dielectric layer **103** and expose a top surface of the patterned mask **112**, a planarization process such as a chemical mechanical polishing (CMP) process may be performed, such that the top surfaces of the patterned mask **112** and the dielectric layer **103** are substantially leveled. In other embodiments, an etch back process may be performed to substantially level the top surfaces of the patterned mask **112** and the dielectric layer **103**.

[0021] Referring to FIG. **1**F, the patterned mask **112** is removed to form a trench **118** which exposes the adhesion layer **116**. The removal may be performed by a wet etching process, and the utilized etchant includes hydrofluoric acid (HF), nitric acid (HNO.sub.3), sulfuric acid (H.sub.2SO.sub.4), phosphoric acid (H.sub.3PO.sub.4), hydrochloric acid (HCl), ammonia (NH.sub.3), other suitable etchants, or a combination thereof. In the embodiments where the material of the patterned mask **112** includes a nitride, a wet etching process utilizing, for example, hot phosphoric acid may be used to remove the patterned mask **112**.
[0022] Referring to FIG. **1**G, an upper conductive material layer **120** is formed in the trench **118** and over the dielectric layer **103**. The upper conductive material layer **120** may include, for example, copper, tungsten, titanium, titanium nitride, aluminum, ruthenium, molybdenum, cobalt, other suitable conductive material, or a combination thereof. The method for forming the upper conductive material layer **120** may include PVD, CVD, ALD, e-beam evaporation, plating, or other suitable methods, or a combination thereof.
[0023] Referring to FIG. **1**H, after forming the upper conductive material layer **120**, a suitable etch back process or a planarization process may be performed to remove excess upper conductive material layer **120**, thereby forming an upper conductive layer **122**. As shown in FIG. **1**H, the formed upper conductive layer **122** may have a width that substantially corresponds to the widths of the underlying lower conductive layer **114** and adhesion layer **116**. The adhesion layer **116** is disposed between the upper conductive layer **122** and the lower conductive layer **114**. It should be noted that the upper conductive layer **122** is used as a topmost layer of the conductive line structure in a first implementation of the subsequently formed resistive random access memory (such as the resistive random access memory **200**), and the upper conductive layer **122** is used as a lower electrode of the memory unit in a second implementation of the subsequently formed resistive random access memory (such as the resistive random access memory **300**).
[0024] FIGS. **2**A and **2**B illustrate cross-sectional views of the resistive random access memory in a manufacturing process following FIG. **1**H, in accordance with the first implementation of the present disclosure. Referring to FIG. **2**A, after forming the upper conductive layer **122**, a lower electrode layer **124**, a metal oxide layer **126**, and an upper electrode **128** are sequentially formed over the upper conductive layer **122** and the dielectric layer **103**, and the lower electrode layer **124** is formed directly on an upper surface of the upper conductive layer **122**. The material of the lower electrode layer **124** and the upper electrode layer **128** may include platinum, titanium nitride, gold, titanium, tantalum, tantalum nitride, tungsten, tungsten nitride, copper, other suitable materials, or a combination thereof, and the lower electrode layer **124** and the upper electrode layer **128** may each include a single-layered structure or a multi-layered structure. The material of the metal oxide layer **126** may include a transition metal oxide, such as nickel oxide, titanium oxide, hafnium oxide, zirconium oxide, zinc oxide, tungsten oxide, aluminum oxide, tantalum oxide, molybdenum oxide, copper oxide, other suitable materials, or a combination thereof.
[0025] Referring to FIG. **2**B, after the lower electrode layer **124**, the metal oxide layer **126**, and the upper electrode layer **128** are sequentially formed, a patterning process is performed to remove the lower electrode layer **124**, the metal oxide layer **126**, and the upper electrode layer **128** in a periphery circuit area **200**B, thereby forming a lower electrode **224**, a resistive switching layer **226**, and an upper electrode **228** in an array area **200**A, respectively.
[0026] As shown in FIG. **2**B, the resulted resistive random access memory **200** includes a conductive line structure **210** and a memory unit **220**, wherein the upper surface of the conductive line structure **210** is in direct contact with the lower electrode **224** of the memory unit **220**. In some embodiments, via is not formed between the conductive line structure **210** and the memory unit **220**. It is understood that in this implementation, the conductive line structure **210** includes the lower conductive layer **114**, the adhesion layer **116**, and the upper conductive layer **122**, and the memory unit **220** includes the lower electrode **224**, the resistive switching layer **226**, and the upper electrode **228** in the array area **200**A.

[0027] In this implementation, since the memory unit **220** may be formed in a single patterning process, the lower electrode **224**, the resistive switching layer **226**, and the upper electrode **228** may have sidewalls that are substantially coplanar. In addition, since the formation of other conductive structures (such as vias) is omitted between the conductive line structure **210** and the memory unit **220**, while reducing the contact resistance within the resistive random access memory **200**, it also simplifies the manufacturing process and reduces the cost.

[0028] FIGS. **3**A and **3**B illustrate cross-sectional views of the resistive random access memory in a manufacturing process following FIG. **1**H, in accordance with the second implementation of the present disclosure. Referring to FIG. **3**A, after forming the upper conductive layer **122**, a metal oxide layer **126** and an upper electrode **128** are sequentially formed over the upper conductive layer **122** and the dielectric layer **103**, and the metal oxide layer **126** is formed directly on an upper surface of the upper conductive layer **122**. The material of the upper electrode layer **128** may include platinum, titanium nitride, gold, titanium, tantalum, tantalum nitride, tungsten, tungsten nitride, copper, other suitable materials, or a combination thereof, and the upper electrode layer **128** may include a single-layered structure or a multi-layered structure. The material of the metal oxide layer **126** may include a transition metal oxide, such as nickel oxide, titanium oxide, hafnium oxide, zirconium oxide, zinc oxide, tungsten oxide, aluminum oxide, tantalum oxide, molybdenum oxide, copper oxide, other suitable materials, or a combination thereof. In some embodiments, a nitridation or oxidation treatment may be performed on the upper conductive layer **122** before forming the metal oxide layer **126** and the upper electrode layer. Therefore, the redox reaction to the metal oxide layer **126** (and the subsequently formed resistive switching layer **326**) can be reduced to prevent the device from failing to undergo transition.

[0029] Referring to FIG. **3**B, after the metal oxide layer **126** and the upper electrode layer **128** are sequentially formed, a patterning process is performed to remove the metal oxide layer **126** and the upper electrode layer **128** in a periphery circuit area **300**B, thereby forming a resistive switching layer **326**, and an upper electrode **328** in an array area **300**A, respectively. In addition, in some embodiments, sidewalls of the upper electrode **328** and the resistive switching layer **326** are substantially coplanar, and the widths of the upper electrode **328** and the resistive switching layer **326** are wider than the width of the upper conductive layer **122**.

[0030] As shown in FIG. **3**B, the resulted resistive random access memory **300** includes a conductive line structure **310** and a memory unit **320**, wherein the upper surface of the conductive line structure **310** is in direct contact with the upper conductive layer **122** of the memory unit **320**. The upper conductive layer **122** functions as a lower electrode of the memory unit **320**. In some embodiments, via is not formed between the conductive line structure **310** and the memory unit **320**. It is understood that in this implementation, the conductive line structure **310** of the array area **300**A includes the lower conductive layer **114** and the adhesion layer **116**, but does not include the upper conductive layer **122**, and the conductive line structure **310** of the periphery circuit area **300**B includes the lower conductive layer **114**, the adhesion layer **116**, and the upper conductive layer **122**. In addition, the memory unit **320** includes the upper conductive layer **122**, the resistive switching layer **326**, and the upper electrode **328** in the array area **300**A, wherein the upper conductive layer **122** is used as a lower electrode of the memory unit **320**. As shown in FIGS. **3**A and **3**B, in some embodiments, a sidewall of the upper conductive layer **122** used as the lower electrode corresponds the sidewall of the conductive line structure **310**.

[0031] In this implementation, the upper conductive layer **122** is buried in a trench in the dielectric layer **103** corresponding to the conductive line structure **310**, and the upper conductive layer **122** as the lower electrode may be formed directly on the upper surface of the adhesion layer **116**, so that the upper surface of the adhesion layer **116** is in direct contact with the upper conductive layer **122**. Since the upper conductive layer **122** is used as the lower electrode of the memory unit **320** directly, and the formation of other layers is omitted between the upper conductive layer **122** and the resistive switching layer **326**, while further reducing the contact resistance within the resistive

random access memory **300**, it also simplifies the manufacturing process and reduces the cost.
[0032] Specifically, when a forward voltage is applied to the resistive random access memories **200** and **300**, the oxygen ions in the resistive switching layers **226** and **326** migrate to the electrode above, and oxygen vacancy conductive filaments are formed in the resistive switching layers **226** and **326**, so that the resistive switching layers **226** and **326** are converted to the low resistance state. Conversely, when a reverse voltage is applied to the resistive random access memories **200** and **300**, the oxygen ions return to the resistive switching layers **226** and **326** and combine with the oxygen-vacancies in the resistive switching layers **226** and **326**, resulting in the disappearance of the oxygen vacancy conductive filaments, so that the resistive switching layers **226** and **326** are converted to the high resistance state. The resistive random access memories **200** and **300** convert their resistance value in the aforementioned manner to store or read data to achieve the memory function.
[0033] In summary, the present disclosure provides a resistive random access memory an a method for manufacturing the same, wherein a conductive line structure is in contact with a memory unit directly, thereby reducing the series resistance within the resistive random access memory. As a result, since a forming operation may be performed well on the resulted resistive random access memory, it can be ensured that the resulted resistive random access memory has improved yield and performance. Moreover, since the formation of other conductive structures (such as vias) is omitted between the conductive line structure and the memory unit, while reducing the contact resistance within the RRAM, it also simplifies the manufacturing process and reduces the cost.
[0034] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

Claims

1. A resistive random access memory, comprising: a conductive line structure disposed in an array area and a periphery circuit area; and a memory unit disposed on the conductive line structure in the array area, wherein the memory unit comprises: a lower electrode disposed on the conductive line structure; a resistive switching layer disposed on the lower electrode; and an upper electrode disposed on the resistive switching layer, wherein an upper surface of the conductive line structure is in direct contact with the lower electrode.
2. The resistive random access memory as claimed in claim 1, wherein there is no via between the conductive line structure and the memory unit.
3. The resistive random access memory as claimed in claim 1, wherein each of the lower electrode layer and the upper electrode layer comprises platinum, titanium nitride, gold, titanium, tantalum, tantalum nitride, tungsten, tungsten nitride, copper, or a combination thereof.
4. The resistive random access memory as claimed in claim 1, wherein the resistive switching layer comprises a transition metal oxide.
5. The resistive random access memory as claimed in claim 4, wherein the transition metal oxide comprises nickel oxide, titanium oxide, hafnium oxide, zirconium oxide, zinc oxide, tungsten oxide, aluminum oxide, tantalum oxide, molybdenum oxide, copper oxide, or a combination thereof.
6. The resistive random access memory as claimed in claim 1, wherein sidewalls of the lower electrode, the resistive switching layer, and the upper electrode are coplanar.

7. The resistive random access memory as claimed in claim 1, further comprising: a dielectric layer in which a trench is disposed, and the conductive line structure comprises: an upper conductive layer disposed in the trench, and the upper conductive layer is in direct contact with a lower surface of the lower electrode; and a lower conductive layer disposed below the upper conductive layer.
8. The resistive random access memory as claimed in claim 7, wherein top surfaces of the upper conductive layer and the dielectric layer are leveled.
9. The resistive random access memory as claimed in claim 7, wherein the upper conductive layer comprises copper, tungsten, titanium, titanium nitride, aluminum, ruthenium, molybdenum, cobalt, or a combination thereof.
10. The resistive random access memory as claimed in claim 7, wherein the lower conductive layer comprises aluminum.
11. The resistive random access memory as claimed in claim 7, wherein the conductive line structure further comprises: an adhesion layer disposed between the upper conductive layer and the lower conductive layer.
12. The resistive random access memory as claimed in claim 11, wherein both the lower conductive layer and the adhesion layer have inclined sidewalls.
13. The resistive random access memory as claimed in claim 12, wherein the lower conductive layer has an average width wider than an average width of the adhesion layer.
14. The resistive random access memory as claimed in claim 11, wherein the adhesion layer comprises titanium, titanium nitride, or a combination thereof.
15. The resistive random access memory as claimed in claim 1, further comprising: a dielectric layer in which a trench corresponding to the conductive line structure is disposed, and the lower electrode is buried in the trench.
16. The resistive random access memory as claimed in claim 15, wherein the conductive line structure further comprises: an adhesion layer, and an upper surface of the adhesion layer is in direct contact with the lower electrode.
17. The resistive random access memory as claimed in claim 15, wherein the sidewalls of the upper electrode and the resistive switching layer are coplanar, and widths of the upper electrode and the resistive switching layer are larger than a width of the lower electrode.
18. The resistive random access memory as claimed in claim 15, wherein a sidewall of the lower electrode is aligned with a sidewall of the conductive line structure.
19. The resistive random access memory as claimed in claim 15, wherein the dielectric layer comprises silicon oxide, silicon oxynitride, phosphosilicate glass (PSG), borosilicate glass (BSG), borophosphosilicate glass (BPSG), undoped silicate glass (USG), fluorinated silicate glass (FSG), or a combination thereof.
20. The resistive random access memory as claimed in claim 1, further comprising: a contact plug disposed under the conductive line structure in the array area, wherein the contact plug is electrically connected to a control element.