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MAGNETORESISTIVE MEMORY DEVICE AND MANUFACTURING METHOD THEREOF

Abstract

A method includes forming bottom conductive lines extending along a first direction; forming a first memory cell over one of the bottom conductive lines and a second memory cell over another one of the bottom conductive lines; forming a third memory cell over the one of the bottom conductive lines and a fourth memory cell over the another one of the bottom conductive lines, wherein the third memory cell and the fourth memory cell are at a higher level than the first memory cell and the second memory cell; and forming top conductive lines above the bottom conductive lines, wherein one of the top conductive line vertically overlaps the first and third memory cells, and another one of the top conductive line vertically overlaps the second and fourth memory cells.

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATION [0001] The present application is a Continuation application of U.S. application Ser. No. 18/352,872, filed on Jul. 14, 2023, which is Continuation application of U.S. application Ser. No. 17/871,983, filed on Jul. 25, 2022, now U.S. Pat. No. 11,749,328, issued on Sep. 5, 2023, which is a Divisional application of U.S. application Ser. No. 16/572,329, filed on Sep. 16, 2019, now U.S. Pat. No. 11,410,714, issued on Aug. 9, 2022, which are herein incorporated by references.

BACKGROUND
[0002] In the semiconductor integrated circuit (IC) industry, technological advances in IC materials and design have produced generations of ICs where each generation has smaller and more complex circuits than the previous generation. In the course of IC evolution, functional density (i.e., the number of interconnected devices per chip area) has generally increased as a result of decreasing minimum feature size or geometry sizes (i.e., the smallest component (or line) that can be created using a fabrication process). Such scaling down has also increased the complexity of IC processing and manufacturing.
[0003] One type of feature that may be part of an integrated circuit is a Magnetic Tunnel Junction (MTJ). An MTJ is a device that changes its resistive state based on the state of magnetic materials within the device. The MTJ involves spin electronics, which combines semiconductor technology and magnetic materials and devices. The spin polarization of electrons, rather than the charge of the electrons, is used to indicate the state of “1” or “0.”

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0004] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.
[0005] FIGS. **1**A and **1**B are a flowchart of a method for manufacturing a memory device according to aspects of the present disclosure in various embodiments.
[0006] FIGS. **2**A, **3**A, **4**A, **5**A, **6**A, **7**A, **8**A, **9**A, **10**A, **11**A, **12**A, **13**A, and **14**A respectively illustrate top views of the semiconductor device at various stages in accordance with some embodiments of the present disclosure.
[0007] FIGS. **2**B, **3**B, **4**B, **5**B, **6**B, **7**B, **8**B, **9**B, **10**B, **11**B, **12**B, **13**B, and **14**B illustrate cross-

sectional views of lines B-B respectively illustrated in FIGS. **2**A, **3**A, **4**A, **5**A, **6**A, **7**A, **8**A, **9**A, **10**A, **11**A, **12**A, **13**A, and **14**A.
[0008] FIG. **15**A is an enlarged cross-sectional view of the first MTJ structure in FIG. **3**B.
[0009] FIG. **15**B is an enlarged cross-sectional view of the first MTJ stacks in FIG. **4**B.
[0010] FIG. **16** is a perspective view of the memory device in FIGS. **14**A and **14**B in accordance with various embodiments of the present disclosure.
[0011] FIGS. **17**A and **17**B are a flowchart of a method for manufacturing a memory device according to aspects of the present disclosure in various embodiments.
[0012] FIGS. **18**A, **19**A, **20**A, **21**A, **22**A, **23**A, **24**A, **25**A, **26**A, **27**A, **28**A, **29**A, **30**A, and **31**A respectively illustrate top views of the semiconductor device at various stages in accordance with some embodiments of the present disclosure.
[0013] FIGS. **18**B, **19**B, **20**B, **21**B, **22**B, **23**B, **24**B, **25**B, **26**B, **27**B, **28**B, **29**B, **30**B, and **31**B illustrate cross-sectional views of lines B-B respectively illustrated in FIGS. **18**A, **19**A, **20**A, **21**A, **22**A, **23**A, **24**A, **25**A, **26**A, **27**A, **28**A, **29**A, **30**A, and **31**A.
[0014] FIG. **32** is a perspective view of the memory device in FIGS. **31**A and **31**B in accordance with various embodiments of the present disclosure.
[0015] FIG. **33** is a top view of the memory device in accordance with various embodiments of the present disclosure.
[0016] FIG. **34** is a perspective view of an area P of FIG. **33** in accordance with various embodiments of the present disclosure.
[0017] FIG. **35** is a top view of a memory device in accordance with various embodiments of the present disclosure.
[0018] FIG. **36** is a top view of a memory device in accordance with various embodiments of the present disclosure.

DETAILED DESCRIPTION

[0019] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.
[0020] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper” and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.
[0021] As used herein, “around”, “about”, “approximately”, or “substantially” shall generally mean within 20 percent, or within 10 percent, or within 5 percent of a given value or range. Numerical quantities given herein are approximate, meaning that the term “around”, “about”, “approximately”, or “substantially” can be inferred if not expressly stated.
[0022] The embodiments of this disclosure relate to integrated memory fabrications and more specifically to magnetoresistive memory formations by forming a memory array with different leveled magnetic tunnel junctions (MTJs). Because of the different leveled magnetic tunnel

junctions, an integrated memory device with high density can be formed. Further, the area of back-end-of-line (BEOL) may be saved. The memory device may be used in spin-transfer torque (STT) MRAM or other suitable memories.

[0023] FIGS. **1**A and **1**B are a flowchart of a method M**10** for manufacturing a memory device according to aspects of the present disclosure in various embodiments. Various operations of the method M**10** are discussed in association with diagrams FIGS. **2**A-**14**B, where FIGS. **2**A, **3**A, **4**A, **5**A, **6**A, **7**A, **8**A, **9**A, **10**A, **11**A, **12**A, **13**A, and **14**A respectively illustrate top views of the semiconductor device at various stages in accordance with some embodiments of the present disclosure, and FIGS. **2**B, **3**B, **4**B, **5**B, **6**B, **7**B, **8**B, **9**B, **10**B, **11**B, **12**B, **13**B, and **14**B illustrate cross-sectional views of lines B-B respectively illustrated in FIGS. **2**A, **3**A, **4**A, **5**A, **6**A, **7**A, **8**A, **9**A, **10**A, **11**A, **12**A, **13**A, and **14**A. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements.

[0024] In operation S**12** of method M**10** in FIG. **1**A, a wafer **110** is provided, as shown in FIGS. **2**A and **2**B. In some embodiments, the wafer **110** is a substrate. In some other embodiments, the wafer **110** includes a substrate and a logic circuit over the substrate. The substrate may be a silicon substrate. Alternatively, the substrate may include another elementary semiconductor, such as germanium; a compound semiconductor including silicon carbide; an alloy semiconductor including silicon germanium; or combinations thereof. In some embodiments, the substrate is a semiconductor on insulator (SOI) substrate. The substrate may include doped regions, such as p-wells and n-wells. In some embodiments, the wafer **110** is a workpiece that includes the substrate and various features formed in and over and attached to the substrate. In some embodiments, the logic circuit includes transistors formed by transistor fabrication processes and may be a planar transistor, such as polysilicon gate transistors or high-k metal gate transistors, or a multi-gate transistor, such as fin field effect transistors.

[0025] In operation S**14** of method M**10** in FIG. **1**A, a plurality of bottom conductive lines **120** are formed over the wafer **110**, as shown in FIGS. **2**A and **2**B. In some embodiments, the bottom conductive lines **120** are formed of copper or copper alloys. In some other embodiments, the bottom conductive lines **120** may be formed of conductive materials such as cobalt, aluminum, tungsten, carbon, Ru, Ra, TaN, or other suitable materials. In still some other embodiments, the bottom conductive lines **120** may be a bilayer structure (e.g., a TaN layer and a TiN layer formed on the TaN layer). In some embodiments, a blanket conductive layer may be formed on the wafer **110** in advance, and then the blanket conductive layer is patterned to be a plurality of the bottom conductive lines **120**. In FIG. **2**A, the bottom conductive lines **120** extend in the X direction. In some embodiments, the bottom conductive lines **120** has a thickness in a range from about 0.1 nm to about 1000 nm, and may have a width in a range of about 0.1 nm to about 1000 nm, e.g., about 30 nm.

[0026] In operation S**16** of method M**10** in FIG. **1**A, a plurality of first MTJ stacks **130** are formed over the bottom conductive lines **120**, as shown in FIGS. **3**A, **3**B, **4**A, and **4**B. Reference is made to FIGS. **3**A, **3**B, and **15**A, where FIG. **15**A is an enlarged cross-sectional view of the first MTJ structure **130**′ in FIG. **3**B. A seed layer **132**′ is formed on the bottom conductive lines **120** and the wafer **110**. The seed layer **132**′ may be made of a variety of conductive materials such as metal or metal alloy materials. For example, the seed layer **132**′ may be made of platinum (Pt), ruthenium (Ru), copper (Cu), tungsten (W), aluminum (Al), titanium (Ti), tantalum (Ta), or other suitable conductive material(s) or layered combination thereof. The seed layer **132**′ may be deposited by a suitable technique, such as physical vapor deposition (PVD), plating, or other suitable processes. In some embodiments, the seed layer **132**′ has a thickness in a range from about 0.1 nm to about 1000 nm.

[0027] A pinned layer **134**′ is then formed on the seed layer **132**′. A purpose of the pinned layer **134**′ (also called as a synthetic anti-ferromagnetic (SAF) layer) is to fix, or pin, the magnetization direction of the reference layer **138**′ through anti-ferromagnetic coupling. In some embodiments,

the pinned layer **134** includes a ferromagnetic material layer, therefore also referred to as pinned ferromagnetic layer. The ferromagnetic material may form permanent magnets and/or exhibit strong interactions with magnets. In some embodiments, the pinned layer **134** includes a cobalt-based film, e.g., a cobalt-iron-boron (CoFeB) film. The pinned layer **134** may alternatively include other materials, such as CoFeTa, NiFe, Co, CoFe, CoPt, CoPd, FePt, or the alloy of Ni, Co and Fe. As one example, the CoFeB film may be formed by PVD, or alternatively other suitable process.

[0028] The pinned layer **134**′ may alternatively include an SAF layer having a three-layer structure. In some embodiments, the pinned layer **134**′ includes a first pinned layer (or bottom pinned layer) and a second pinned layer (or top pinned layer) interposed by a spacer layer. The first and second pinned layers may include a ferromagnetic material. In one example, the ferromagnetic material in the first and/or second pinned layer(s) includes a CoFeB film. The ferromagnetic material layer may alternatively include other materials, such as CoFeTa, NiFe, Co, CoFe, CoPt, CoPd, FePt, or the alloy of Ni, Co and Fe.

[0029] The pinned layer **134**′ may alternatively include a buffer layer, a ferromagnetic layer, a bottom pinned layer, a top pinned layer, and a spacer film between the bottom ferromagnetic layer and the top ferromagnetic layer. The buffer layer may include Ta, Ru, or other suitable materials, and the ferromagnetic layer may include Co. The bottom pinned layer and the top pinned layer are both multilayers. Specifically, the bottom pinned layer includes two or more ferromagnetic films. Particularly, the bottom pinned layer includes a first film of a first ferromagnetic material and a second film of a second ferromagnetic material alternatively arranged. In some embodiments, there are N layers of first film and N layers of second film, and N is 1 to about 100. In some examples, the first and second ferromagnetic materials in the bottom pinned layer F**1**′ include Co, Pt, Ni, Fe, or other suitable materials. For example, the first ferromagnetic material may be Co and the second ferromagnetic material may be Pt.

[0030] Further, the top pinned layer includes two or more ferromagnetic films. Particularly, the top pinned layer includes a third film of a third ferromagnetic material and a fourth film of a fourth ferromagnetic material alternatively arranged. In some embodiments, there are M layers of third film and M layers of second film, and M is 1 to about 100. In some embodiments, N is greater than M. In some examples, the third and fourth ferromagnetic materials in the top pinned layer include Co, Pt, Ni, Fe, or other suitable materials. For example, the third ferromagnetic material may be Co and the fourth ferromagnetic material may be Pt.

[0031] The spacer film is disposed between the bottom pinned layer and the top pinned layer. In some embodiments, the spacer film includes ruthenium (Ru). Alternatively, the spacer film may include other suitable material, such as Ir, Ti, Ta, Cu, or Ag. The spacer film may be formed by a PVD process, or another suitable process.

[0032] A spacer layer **136**′ is then formed on the pinned layer **134**′. The spacer layer **136**′ may be made of a variety of conductive materials such as metal or metal alloy materials. For example, the spacer layer **136**′ may be made of tantalum (Ta), Molybdenum (Mo), tungsten (W), or other suitable conductive material(s) or layered combination thereof. The spacer layer **136**′ may be deposited by a suitable technique, such as physical vapor deposition (PVD), plating, or other suitable processes. In some embodiments, the spacer layer **136**′ has a thickness in a range from about 0.1 nm to about 1000 nm.

[0033] A reference layer **138**′ is formed on the spacer layer **136**′. The reference layer **138**′ is a (single) ferromagnetic layer. The reference layer **138**′ may include Co, Fe, Ni, Mn, B, and/or their alloys, including for example, NiFe, NiFe, CoFe, Y.sub.3Fe.sub.5O.sub.12, CoFeB, or compounds thereof, including other ferromagnetic materials. The reference layer **138**′ may be formed by processes such as, chemical vapor deposition (CVD), physical vapor deposition (PVD), electro-chemical deposition, molecular manipulation, and/or other processes. The reference layer **138**′ is illustrated in FIG. **15**A as a single layer; however, the reference layer **138**′ may be synthetic. In some embodiments, the reference layer **138**′ has a thickness in a range from about 0.1 nm to about

1000 nm.
[0034] A tunnel barrier layer **142**′ is formed on the reference layer **138**′. The tunnel barrier layer **142**′ is thin enough to allow the tunneling of electrons through it. The tunnel barrier layer **142**′ has a nonmagnetic composition and can be formed from any suitable material that may function as an electrical insulator. In some embodiments, the tunnel barrier layer **142**′ includes MgO. In some alternative embodiments, the tunnel barrier layer **142**′ includes aluminum. Examples of other dielectric materials that may be included in the tunnel barrier layer **142**′ include oxides or nitrides of Al, Mg, Si, Hf, Sr, or Ti such as, SiOx, SiNx, SiOxNy, AlOx, TOx, TiOx, AlNx, and/or combinations thereof. The tunnel barrier layer **142**′ may be formed by processes such as, chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), physical vapor deposition (PVD), electro-chemical deposition, molecular manipulation, oxidation, and/or other suitable processes. In some embodiments, the tunnel barrier layer **142**′ has a thickness in a range from about 0.1 nm to about 1000 nm. The tunnel barrier layer **142**′ may electrically insulate the reference layer **138**′ from the free layer **144**′ independently, or in conjunction with other layers interposing the reference layer **138**′ and the free layer **144**′.
[0035] Then, a free layer **144**′ is formed on the tunnel barrier layer **142**′. The free layer **144**′ includes a bottom free layer F**1**′, a top free layer F**2**′, and a spacer film S′ between the bottom free layer F**1**′ and the top free layer F**2**′. In some examples, the bottom free layer F**1**′ includes Co, Pt, Ni, Fe, or other suitable materials. For example, the bottom free layer F**1**′ may be CoFeB. The bottom free layer F**1**′ may have a thickness in a range from about 0.1 nm to about 1000 nm. Further, the top free layer F**2**′ includes Co, Pt, Ni, Fe, or other suitable materials. For example, the top free layer F**2**′ may be CoFeB. The top free layer F**2**′ may have a thickness in a range from about 0.1 nm to about 1000 nm.
[0036] The spacer film S′ is disposed between the bottom free layer F**1**′ and the top free layer F**2**′. In some embodiments, the spacer film S′ includes tantalum (Ta). Alternatively, the spacer film S′ may include other suitable material, such as Ir, Ti, Ru, Cu, or Ag. In some examples, the spacer film S′ may have a thickness in a range from about 0.1 nm to about 1000 nm. The spacer film S′ may be formed by a PVD process, or another suitable process.
[0037] Then, a patterned mask layer M**1** is formed over the first MTJ structure **130**′. In some embodiments, a mask material may be formed over the first MTJ structure **130**′ by using spin-coating or other suitable techniques, and the mask material is patterned to be the patterned mask layer M**1**. In some embodiments, the patterned mask layer M**1** may be a photoresist, a hard mask layer, a SiNx layer, or combinations thereof. The patterned mask layer M**1** may have a thickness in a range from about 0.1 nm to about 1000 nm.
[0038] Reference is made to FIGS. **4**A, **4**B, and **15**B, where FIG. **15**B is an enlarged cross-sectional view of the first MTJ stacks **130** in FIG. **4**B. The first MTJ structure **130**′ of FIGS. **3**A and **3**B are patterned to form the first MTJ stacks **130** using the patterned mask layer M**1** (see FIGS. **3**A and **3**B) as a mask. Each of the first MTJ stacks **130** includes a seed layer **132**, a pinned layer **134**, a spacer layer **136**, a reference layer **138**, a tunnel barrier layer **142**, and a free layer **144**, and the free layer **144** includes a bottom free layer F**1**, a top free layer F**2**, and a spacer film S between the bottom layer F**1** and the top free layer F**2**. The memory information is stored in a magnetization state of the free layer **144**. The relative magnetization direction between the free layer **144** and the reference layer **138** determines the resistance of the first MTJ stack **130**. In some embodiments, the reference layer **138** and the free layer **144** may have a magnetization orientation that can be both in-plane or out-of plane with respect to the top surface of the first MTJ stack **130**. The patterning process in FIGS. **4**A and **4**B may be performed by using an etching process, such as reactive ion etching (RIE), ion beam etching (IBE), wet etching, or combinations thereof. After the patterning process, the patterned mask layer M**1** is removed by using stripping, ashing, or etching process (such as reactive ion etching (RIE), ion beam etching (IBE), wet etching, or combinations thereof).
[0039] In FIG. **4**A, the first MTJ stacks **130** are respectively formed on the bottom conductive lines

120. The (adjacent) first MTJ stacks **130** are neither aligned in the X direction nor in the Y direction. For example, the (adjacent) first MTJ stacks **170** are arranged in diagonal. In some embodiments, a connection line L**1** of the (adjacent) first MTJ stacks **130** and an extension direction E**1** of the bottom conductive line **120** form an angle θ**1** greater than about 0 degree and less than about 90 degree (i.e., an acute angle). That is, the connection line L**1** and the extension direction E**1** are neither parallel nor perpendicular to each other. In some embodiments, the angle θ**1** is about 40 degrees to about 50 degrees, e.g., about 45 degrees, and the present disclosure is not limited in this respect. Further, a distance D**1** is formed between the adjacent first MTJ stacks **130**. In some embodiments, the distance D**1** depends on the lithography limitation, which may be greater than about 10 nm in some embodiments. In some embodiments, the first MTJ stack **130** may has a radius in a range of about 0.1 nm to about 1000 nm, e.g., about 25 nm. A top view of the first MTJ stack **130** may be circular, elliptical, rectangular, square or other suitable shapes with or without rounded corners.

[0040] In operation S**18** of method M**10** in FIG. **1**A, a first dielectric structure **150** is formed over the first MTJ stacks **130**, as shown in FIGS. **5**A, **5**B, **6**A, and **6**B. Reference is made to FIGS. **5**A and **5**B. A first encapsulation layer **152** is formed over the first MTJ stacks **130** and the bottom conductive lines **120**, lining the upper surface and sidewalls of the first MTJ stacks **130**. In some embodiments, the first encapsulation layer **152** may be formed by suitable deposition technique and may be formed conformally. Further, the first encapsulation layer **152** may be formed of, for example, silicon nitride, silicon carbide, or combinations thereof. The first encapsulation layer **152** may have a thickness in a range from about 0.1 nm to about 1000 nm.

[0041] Then, a first dielectric layer **154** is formed over the first encapsulation layer **152** and covers the first MTJ stacks **130**. The first dielectric layer **154** may include, for example, silicon oxide, silicon nitride, low-k silicon oxide such as a porous silicon oxide layer, other suitable dielectric material, combinations thereof, or the like. The first dielectric layer **154** may have a thickness in a range from about 0.1 nm to about 1000 nm.

[0042] Reference is made to FIGS. **6**A and **6**B. A planarization process is performed to the first dielectric layer **154** and the first encapsulation layer **152** until top surfaces of the first MTJ stacks **130** are exposed. For example, the planarization process is a CMP process.

[0043] Then, a second dielectric layer **156** is formed over the first encapsulation layer **152**, the first dielectric layer **154**, and covers the first MTJ stacks **130**. The second dielectric layer **156** may include, for example, silicon oxide, silicon nitride, low-k silicon oxide such as a porous silicon oxide layer, other suitable dielectric material, combinations thereof, or the like. The second dielectric layer **156** may have a thickness in a range from about 0.1 nm to about 1000 nm. The second dielectric layer **156**, the first dielectric layer **154**, and the first encapsulation layer **152** are together referred to as the first dielectric structure **150**.

[0044] In operation S**20** of method M**10** in FIG. **1**A, a plurality of first vias **160** are formed in the first dielectric structure **150**, as shown in FIGS. **7**A, **7**B, **8**A, and **8**B. Reference is made to FIGS. **7**A and **7**B. More specific, another patterned mask layer M**2** is formed over the first dielectric structure **150**, and the patterned mask layer M**2** exposes portions of the first dielectric structure **150**. In some embodiments, a mask material may be formed over the first dielectric structure **150** by using spin-coating or other suitable techniques, and the mask material is patterned to be the patterned mask layer M**2**. In some embodiments, the patterned mask layer M**2** may be a photoresist, a hard mask layer, a SiN.sub.x layer, or combinations thereof. The patterned mask layer M**2** may have a thickness in a range from about 0.1 nm to about 1000 nm.

[0045] Then, a plurality of first openings **151** are formed in the first dielectric structure **150**. The second dielectric layer **156**, the first dielectric layer **154**, and the first encapsulation layer **152** of the first dielectric structure **150** are patterned (etched) using the patterned mask layer M**2** as a mask to form the first openings **151** in the second dielectric layer **156**, the first dielectric layer **154**, and the first encapsulation layer **152**. The first openings **151** respectively expose portions of the bottom

conductive lines **120**.

[0046] Reference is made to FIGS. **8**A and **8**B. The patterned mask layer M**2** (see FIGS. **7**A and **7**B) is removed by using stripping, ashing, or etching process (such as reactive ion etching (RIE), ion beam etching (IBE), wet etching, or combinations thereof). Then, barrier layers **162** are conformally formed in the first openings **151**. The barrier layers **162** can improve the adhesion between the bottom conductive lines **120** and a material formed thereon (such as the filling materials **164**), or prevent a diffusion of a metal from diffusing from the via into the first dielectric structure **150**. The barrier layers **162** may include metal nitride materials. For example, the barrier layers **162** include Ta, TaN, or other suitable materials. In some embodiments, the barrier layers **162** include a single layer or multiple layers. For a multiple-layer configuration, the layers include different compositions of metal nitride from each other. The barrier layers **162** may have a thickness in a range from about 0.1 nm to about 1000 nm.

[0047] Filling materials **164** are respectively formed in the first openings **151** and over the barrier layers **162**. The filling materials **164** are electrically connected to the bottom conductive lines **120**. In some embodiments, a blanket barrier layer and a filling layer are sequentially formed on the first dielectric structure **150** and in the first openings **151**, and excessive portions of the filling layer and the blanket barrier layer are removed by performing a CMP process to form the filling materials **164** and the barrier layers **162**. The filling materials **164** can be made of Ti, TiN, or other suitable materials. The filling material **164** and the barrier layer **162** are referred to as the first via **160**.

[0048] In operation S**22** of method M**10** in FIG. **1**A, a plurality of second MTJ stacks **170** are formed on the first dielectric structure **150** and respectively on the first vias **160**, as shown in FIGS. **9**A, **9**B, **10**A, and **10**B. Reference is made to FIGS. **9**A and **9**B. A second MTJ structure **170**′ is formed over the first dielectric structure **150**, such that the second MTJ structure **170**′ covers the first vias **160**. The second MTJ structure **170**′ may have the same or similar structure to the first MTJ structure **130**′ in FIGS. **3**A and **3**B. In some embodiments, the second MTJ structure **170**′ has the structure shown in FIG. **15**A. That is, the second MTJ structure **170**′ includes a seed layer, a pinned layer, a spacer layer, a reference layer, a tunnel barrier layer, and a free layer, and the free layer includes a bottom free layer, a top free layer, and a spacer film between the bottom layer and the top free layer.

[0049] Then, another patterned mask layer M**3** is formed over the second MTJ structure **170**′. In some embodiments, a mask material may be formed over the second MTJ structure **170**′ by using spin-coating or other suitable techniques, and the mask material is patterned to be the patterned mask layer M**3**. In some embodiments, the patterned mask layer M**3** may be a photoresist, a hard mask layer, a SiN.sub.x layer, or combinations thereof. The patterned mask layer M**3** may have a thickness in a range from about 0.1 nm to about 1000 nm.

[0050] Reference is made to FIGS. **10**A and **10**B. The second MTJ structure **170**′ of FIGS. **9**A and **9**B are patterned to form the second MTJ stacks **170** using the patterned mask layer M**3** (see FIGS. **9**A and **9**B) as a mask. Each of the second MTJ stacks **170** may have the structure shown in FIG. **15**B, i.e., the second MTJ stack **170** includes a seed layer, a pinned layer, a spacer layer, a reference layer, a tunnel barrier layer, and a free layer, and the free layer includes a bottom free layer, a top free layer, and a spacer film between the bottom layer and the top free layer. The patterning process in FIGS. **10**A and **10**B may be performed by using an etching process, such as reactive ion etching (RIE), ion beam etching (IBE), wet etching, or combinations thereof. After the patterning process, the patterned mask layer M**3** is removed by using stripping, ashing, or etching process (such as reactive ion etching (RIE), ion beam etching (IBE), wet etching, or combinations thereof).

[0051] In FIG. **10**A, the second MTJ stacks **170** are respectively formed on the first vias **160**. In some embodiments, the first via **160** has a radius less than a radius of the second MTJ stack **170**. For example, the radius of the first via **160** may be in a range of about 0.1 nm to about 1000 nm, e.g., about 12.5 nm. The (adjacent) second MTJ stacks **170** are neither aligned in the X direction nor in the Y direction. For example, the (adjacent) second MTJ stacks **170** are arranged in diagonal.

In some embodiments, a connection line L**2** of the (adjacent) second MTJ stacks **170** and the extension direction E**1** of the bottom conductive line **120** form an angle θ**2** greater than about 0 degree and less than about 90 degree (i.e., an acute angle). That is, the connection line L**2** and the extension direction E**1** are neither parallel nor perpendicular to each other. In some embodiments, the angle θ**2** is about 40 degrees to about 50 degrees, e.g., about 45 degrees, and the present disclosure is not limited in this respect. Further, a distance D**2** is formed between the adjacent second MTJ stacks **170**. In some embodiments, the distance D**2** depends on the lithography limitation, which may be greater than about 10 nm in some embodiments. A top view of the second MTJ stack **170** may be circular, elliptical, rectangular, square or other suitable shapes with or without rounded corners.

[0052] In FIG. **10**A, one of the first MTJ stacks **130** and one of the second MTJ stacks **170** are electrically connected to the same bottom conductive line **120**, and this first MTJ stack **130** and second MTJ stack **170** are at different levels. In FIG. **10**B, the second MTJ stack **170** is higher than the first MTJ stack **130**. Since the first MTJ stack **130** and the second MTJ stack **170** are at different levels, the lateral spacing S**1** between these two MTJ stacks **130** and **170** can be reduced while the first and second MTJ stacks **130** and **170** are well isolated from each other. Similarly, another one of the first MTJ stacks **130** and another one of the second MTJ stacks **170** are electrically connected to another one of the bottom conductive line **120**, and these two MTJ stacks **130** and **170** have reduced lateral spacing S**2**. Also, the lateral spacings S**3** and S**4** shown in FIG. **10**A can be reduced with this configuration. That is, the distance between two adjacent MTJ stacks does not depend on the lateral spacing S**1**, S**2**, S**3**, and/or S**4**. Rather, the distance between two adjacent MTJ stacks depends on the distances D**1** (see FIG. **4**A) and/or D**2** (see FIG. **10**A). In some embodiments, the lateral spacing S**1**, S**2**, S**3**, and/or S**4** is shorter than the distance D**1** and/or D**2**. The first and second MTJ stacks **130** and **170** may overlap with each other in the top view (i.e., the spacing S**1**, S**2**, S**3**, and/or S**4** may be negative) as long as the distances D**1** and/or D**2** are positive (or greater than the lithography limitation).

[0053] In operation S**24** of method M**10** in FIG. **1**A, a second dielectric structure **180** is formed over the second MTJ stacks **170** and the first dielectric structure **150**, as shown in FIGS. **11**A and **11**B. A second encapsulation layer **182** is formed over the second MTJ stacks **170** and the first dielectric structure **150**, lining the upper surface and sidewalls of the second MTJ stacks **170**. In some embodiments, the second encapsulation layer **182** may be formed by suitable deposition technique and may be formed conformally. Further, the second encapsulation layer **182** may be formed of, for example, silicon nitride, silicon carbide, or combinations thereof. The second encapsulation layer **182** may have a thickness in a range from about 0.1 nm to about 1000 nm.

[0054] Then, a third dielectric layer **184** is formed over the second encapsulation layer **182**. The third dielectric layer **184** may include, for example, silicon oxide, silicon nitride, low-k silicon oxide such as a porous silicon oxide layer, other suitable dielectric material, combinations thereof, or the like. The third dielectric layer **184** may have a thickness in a range from about 0.1 nm to about 1000 nm. The second encapsulation layer **182** and the third dielectric layer **184** are together referred to as the second dielectric structure **180**.

[0055] In operation S**26** of method M**10** in FIG. **1**B, a plurality of second openings **181** are formed in the second dielectric structure **180** and the first dielectric structure **150**, as shown in FIGS. **12**A and **12**B. More specific, another patterned mask layer M**4** is formed over the second dielectric structure **180**. In some embodiments, a mask material may be formed over the second dielectric structure **180** by using spin-coating or other suitable techniques, and the mask material is patterned to be the patterned mask layer M**4**. In some embodiments, the patterned mask layer M**4** may be a photoresist, a hard mask layer, a SiNx layer, or combinations thereof. The patterned mask layer M**4** may have a thickness in a range from about 0.1 nm to about 1000 nm.

[0056] Then, a plurality of second openings **181** are formed in the second dielectric structure **180** and the first dielectric structure **150**. The second dielectric structure **180** and the first dielectric

structure **150** are patterned (etched) using the patterned mask layer M**4** as a mask to form the second openings **181** in the second dielectric structure **180** and the first dielectric structure **150**. The second openings **181** respectively expose portions of the first MTJ stacks **130**.

[0057] In operation S**28** of method M**10** in FIG. **1**B, a plurality of trenches **183** are formed in the second dielectric structure **180**, as shown in FIGS. **13**A and **13**B. More specific, the patterned mask layer M**4** (see FIGS. **12**A and **12**B) is removed by using stripping, ashing, or etching process (such as reactive ion etching (RIE), ion beam etching (IBE), wet etching, or combinations thereof). Then, another patterned mask layer M**5** is formed over the second dielectric structure **180**. In some embodiments, a mask material may be formed over the second dielectric structure **180** by using spin-coating or other suitable techniques, and the mask material is patterned to be the patterned mask layer M**5**. In some embodiments, the patterned mask layer M**5** may be a photoresist, a hard mask layer, a SiNx layer, or combinations thereof. The patterned mask layer M**5** may have a thickness in a range from about 0.1 nm to about 1000 nm.

[0058] Then, a plurality of trenches **183** are formed in the second dielectric structure **180**. The second dielectric structure **180** is patterned (etched) using the patterned mask layer M**5** as a mask to form the trenches **183** in the second dielectric structure **180**. The trenches **183** expose the second MTJ stacks **170** and the first MTJ stacks **130**.

[0059] In operation S**30** of method M**10** in FIG. **1**B, a plurality of second vias **190** are formed in the second openings **181** and a plurality of top conductive lines **195** are formed in the trenches **183**, as shown in FIGS. **14**A and **14**B. The patterned mask layer M**5** (see FIGS. **13**A and **13**B) is removed by using stripping, ashing, or etching process (such as reactive ion etching (RIE), ion beam etching (IBE), wet etching, or combinations thereof). Then, barrier layers **192** and **197** are conformally formed in the second openings **181** and the trenches **183**. The barrier layers **192** and **197** can improve the adhesion between the MTJ stacks (i.e., the first MTJ stacks **130** and/or the second MTJ stacks **170**) and a material formed thereon (such as the filling materials **194** and **199**), or prevent a diffusion of a metal from diffusing from the via/line into the first dielectric structure **150** and the second dielectric structure **180**. The barrier layers **192** and **197** may include metal nitride materials. For example, the barrier layers **192** and **197** include Ta, TaN, or other suitable materials. In some embodiments, the barrier layers **192** and **197** include a single layer or multiple layers. For a multiple-layer configuration, the layers include different compositions of metal nitride from each other. The barrier layers **192** and **197** may have a thickness in a range from about 0.1 nm to about 1000 nm.

[0060] Filling materials **194** and **199** are respectively formed in the second openings **181** and the trenches **183**. The filling materials **194** and **199** are electrically connected to the first MTJ stacks **130** and the second MTJ stacks **170**. In some embodiments, a blanket barrier layer and a filling layer are sequentially formed on the second dielectric structure **180** and in the second openings **181** and the trenches **183**, and excessive portions of the filling layer and the blanket barrier layer are removed by performing a CMP process to form the filling materials **194** and **199** and the barrier layer **192** and **197**. The filling materials **194** and **199** can be made of Ti, TiN, or other suitable materials. The filling material **194** and the barrier layer **192** are referred to as the second via **190**, and the filling material **199** and the barrier layer **197** are referred to as the top conductive lines **195**. In some embodiments, the second via **190** has a radius less than a radius of the first MTJ stack **130**. For example, the radius of the second via **190** may be in a range of about 0.1 nm to about 1000 nm, e.g., about 12.5 nm.

[0061] In FIG. **14**A, the top conductive lines **195** extend in the Y direction, and one of the top conductive lines **195** is electrically connected to one first MTJ stack **130** and one second MTJ stack **170**, where these first MTJ stack **130** and second MTJ stack **170** are arranged along the Y direction.

[0062] FIG. **16** is a perspective view of the memory device in FIGS. **14**A and **14**B in accordance with various embodiments of the present disclosure. The dielectric materials (such as the first dielectric structure **150** and the second dielectric structure **180** in FIG. **14**B) are omitted in FIG. **16**

for clarity. Also, the barrier layers in the vias and or conductive lines are not shown in FIG. **16** for clarity. The memory device includes a plurality of bottom conductive lines **120**, a plurality of first MTJ stacks **130**, a plurality of second MTJ stacks **170**, and a plurality of top conductive lines **195**. The bottom conductive lines **120** are disposed over a wafer **110**. The first MTJ stacks **130** are respectively disposed over the bottom conductive lines **120**. In some embodiments, the first MTJ stacks **130** are respectively in contact with the bottom conductive lines **120**. The second MTJ stacks **170** are at a different level from the first MTJ stacks **130** and electrically connected to the bottom conductive lines **120** respectively through first vias **160**. For example, a top surface **170***t* of the second MTJ stack **170** is higher than a top surface **130***b* of the first MTJ stack **130** (see FIG. **14**B). The top conductive lines **195** are disposed over the first MTJ stacks **130** and the second MTJ stacks **170**. In some embodiments, the second MTJ stacks **170** are respectively in contact with the top conductive lines **195**. The first MTJ stacks **130** are electrically connected to the top conductive lines **195** respectively through second vias **190**.

[0063] The first MTJ stack **130** and the second via **190** form a memory cell C**1**, and the second MTJ stack **170** and the first via **160** form another memory cell C**2**. The memory cells C**1** and C**2** are alternately arranged. For example, the bottom conductive lines **120** extend in the X direction, and two of the memory cells C**1** and C**2**, which are connected to the same bottom conductive line **120**, are arranged in the X direction. Further, the top conductive lines **195** extend in the Y direction, and two of the memory cells C**1** and C**2**, which are connected to the same top conductive line **195**, are arranged in the X direction. The two memory cells C**1** and C**2** are adjacent to each other but the MTJ stacks thereof are at different levels. For example, in FIG. **16**, the second MTJ stack **170** is at a level higher than the first MTJ stack **130**. The top surface **170***t* of the second MTJ stack **170** is higher than the top surface **130***b* of the first MTJ stack **130** (see FIG. **14**B). With this configuration, the memory cell C**1** may be close to the memory cell C**2** (e.g., the first MTJ stack **130** and the second MTJ stack **170** may overlap with each other in a top view), and the layout area of the memory device can be reduced.

[0064] In FIGS. **14**B and **16**, the first MTJ stacks **130** and the second MTJ stacks **170** are both disposed between adjacent conductive lines (i.e., the bottom conductive lines **120** and the top conductive lines **195**). The memory cells C**1** and C**2** have substantially the same height. That is, a total height of the first MTJ stack **130** and the second via **190** may be substantially the same as a total height of the second MTJ stack **170** and the first via **160**.

[0065] FIGS. **17**A and **17**B are a flowchart of a method M**40** for manufacturing a memory device according to aspects of the present disclosure in various embodiments. Various operations of the method M**40** are discussed in association with diagrams FIGS. **18**A-**31**B, where FIGS. **18**A, **19**A, **20**A, **21**A, **22**A, **23**A, **24**A, **25**A, **26**A, **27**A, **28**A, **29**A, **30**A, and **31**A respectively illustrate top views of the semiconductor device at various stages in accordance with some embodiments of the present disclosure, and FIGS. **18**B, **19**B, **20**B, **21**B, **22**B, **23**B, **24**B, **25**B, **26**B, **27**B, **28**B, **29**B, **30**B, and **31**B illustrate cross-sectional views of lines B-B respectively illustrated in FIGS. **18**A, **19**A, **20**A, **21**A, **22**A, **23**A, **24**A, **25**A, **26**A, **27**A, **28**A, **29**A, **30**A, and **31**A. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements. The present embodiment may repeat reference numerals and/or letters used in FIGS. **2**A-**14**B. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed. In the following embodiments, the structural and material details described before are not repeated hereinafter, and only further information is supplied to perform the semiconductor devices of FIGS. **18**A-**31**B.

[0066] In operation S**42** of method M**40** in FIG. **17**A, a wafer **110** is provided, as shown in FIGS. **18**A and **18**B. In operation S**44** of method M**40** in FIG. **17**A, a plurality of bottom conductive lines **120** are formed over the wafer **110**, as shown in FIGS. **18**A and **18**B.

[0067] In operation S**46** of method M**40** in FIG. **17**A, a plurality of first vias **210** are formed over the bottom conductive lines **120**, as shown in FIGS. **19**A and **19**B. More specific, a first dielectric

layer **205** is formed over the wafer **110** and covers the bottom conductive lines **120**. The first dielectric layer **205** may have the same or similar materials to the first dielectric layer **154** of FIG. **5**B. Then, a plurality of first openings **207** are formed in the first dielectric layer **205**. The first openings **207** respectively expose the bottom conductive lines **120**. Since the formation of the first openings **207** is similar to the formation of the first openings **151** in FIGS. **7**A and **7**B, a detailed description thereof is not repeated herein.

[0068] Subsequently, first vias **210** are respectively formed in the first opening **207**. In some embodiments, each of the first vias **210** includes a barrier layer **212** and a filling material **214** over the barrier layer **212**. Since the formation of the first vias **210** and the material thereof are similar to the first vias **160** in FIGS. **8**A and **8**B, a detailed description thereof is not repeated herein.

[0069] In operation S**48** of method M**40** in FIG. **17**A, a plurality of first MTJ stacks **130** are formed over the first vias **210**, as shown in FIGS. **20**A and **20**B. For example, a MTJ structure (e.g., the MTJ structure in FIG. **15**A) may be formed over the first dielectric layer **205** and cover the first vias **210**. A patterned mask layer is then formed over the MTJ structure and exposes portions of the MTJ structure. The MTJ structure is subsequently patterned using the patterned mask layer as a mask to form the first MTJ stacks **130**, and the patterned mask layer is removed. The first MTJ stacks **130** are respectively formed over the first vias **210**. In other words, the first MTJ stacks **130** are electrically connected to the bottom conductive lines **120** respectively through the first vias **210**.

[0070] In operation S**50** of method M**40** in FIG. **17**A, a first dielectric structure **220** is formed over the first MTJ stacks **130**, as shown in FIGS. **21**A and **21**B. A first encapsulation layer **222** is formed over the first MTJ stacks **130** and the first dielectric layer **205**, lining the upper surface and sidewalls of the first MTJ stacks **130**. In some embodiments, the first encapsulation layer **222** may be formed by suitable deposition technique and may be formed conformally. Further, the first encapsulation layer **222** may have the same or similar materials to the first encapsulation layer **152** of FIG. **5**B. The first encapsulation layer **222** may have a thickness in a range from about 0.1 nm to about 1000 nm.

[0071] Then, a second dielectric layer **224** is formed over the first encapsulation layer **222**. The second dielectric layer **224** may have the same or similar materials to the first dielectric layer **154** of FIG. **5**B. The second dielectric layer **224** may have a thickness in a range from about 0.1 nm to about 1000 nm. The first encapsulation layer **222** and the second dielectric layer **224** are together referred to as the first dielectric structure **220**.

[0072] In operation S**52** of method M**40** in FIG. **17**A, a plurality of second vias **230** and a plurality of middle conductive lines **240** are formed in the first dielectric structure **220**, as shown in FIGS. **22**A, **22**B, **23**A, **23**B, **24**A, and **24**B. Reference is made to FIGS. **22**A and **22**B. Another patterned mask layer M**6** is formed over the first dielectric structure **220**. The patterned mask layer M**6** may have the same or similar materials to the patterned mask layer M**1** of FIGS. **3**A and **3**B. The patterned mask layer M**6** may have a thickness in a range from about 0.1 nm to about 1000 nm.

[0073] Then, a plurality of second openings **221** are formed in the first dielectric structure **220** and the first dielectric layer **205**. The first dielectric structure **220** and the first dielectric layer **205** are patterned (etched) using the patterned mask layer M**6** as a mask to form the second openings **221** in the first dielectric structure **220** and the first dielectric layer **205**. The second openings **221** respectively expose portions of the bottom conductive lines **120**.

[0074] Reference is made to FIGS. **23**A and **23**B. The patterned mask layer M**6** (see FIGS. **22**A and **22**B) is removed by using stripping, ashing, or etching process (such as reactive ion etching (RIE), ion beam etching (IBE), wet etching, or combinations thereof). Then, another patterned mask layer M**7** is formed over the first dielectric structure **220**. The patterned mask layer M**7** may have the same or similar materials to the patterned mask layer M**1** of FIGS. **3**A and **3**B. The patterned mask layer M**7** may have a thickness in a range from about 0.1 nm to about 1000 nm.

[0075] Then, a plurality of trenches **223** are formed in the first dielectric structure **220**. The first

dielectric structure **220** is patterned (etched) using the patterned mask layer M**7** as a mask to form the trenches **223** in the first dielectric structure **220**. The trenches **223** expose the first MTJ stacks **130**.

[0076] Reference is made to FIGS. **24**A and **24**B. The patterned mask layer M**7** (see FIGS. **23**A and **23**B) is removed by using stripping, ashing, or etching process (such as reactive ion etching (RIE), ion beam etching (IBE), wet etching, or combinations thereof). Then, barrier layers **232** and **242** are conformally formed in the second openings **221** and the trenches **223**. The barrier layers **232** and **242** can improve the adhesion between the first MTJ stacks **130** or the bottom conductive lines **120** and a material formed thereon (such as the filling materials **234** and **244**), or prevent a diffusion of a metal from diffusing from the via/line into the first dielectric structure **220** and the first dielectric layer **205**. The barrier layers **232** and **242** may have the same or similar materials to the barrier layers **162** of FIG. **8**B. The barrier layers **232** and **242** may have a thickness in a range from about 0.1 nm to about 1000 nm.

[0077] Filling materials **234** and **244** are respectively formed in the second openings **221** and the trenches **223** (see FIG. **23**B). The filling materials **234** and **244** are electrically connected to the first MTJ stacks **130** and the bottom conductive lines **120**. The formations of the barrier layers **232** and **242** and the filling materials **234** and **244** are similar to or the same as the formations of the barrier layers **192** and **197** and the filling materials **194** and **199** of FIG. **14**B. The filling materials **234** and **244** may have the same or similar materials to the filling material **194** and **199** of FIG. **14**B. The filling material **234** and the barrier layer **232** are referred to as the second via **230**, and the filling material **244** and the barrier layer **242** are referred to as the middle conductive lines **240**.

[0078] In FIG. **24**A, the bottom conductive lines **120** and the middle conductive lines **240** extend in different directions. For example, the bottom conductive lines **120** extend in the X direction, and the second conductive lines extend in the Y direction. The first MTJ stacks **130** may have similar arrangement to the first MTJ stacks **130** in FIG. **4**A. Thus, the description thereof is not repeated herein.

[0079] In operation S**54** of method M**40** in FIG. **17**A, a plurality of third vias **260** are formed over the middle conductive lines **240**, as shown in FIGS. **25**A and **25**B. More specific, a third dielectric layer **250** is formed over the first dielectric structure **220** and covers the middle conductive lines **240**. The third dielectric layer **250** may have the same or similar materials to the first dielectric layer **154** of FIG. **5**B. Then, a plurality of third openings **251** are formed in the first dielectric layer **205**. The third openings **251** respectively expose the middle conductive lines **240**. Since the formation of the third openings **251** is similar to the formation of the first openings **151** in FIGS. **7**A and **7**B, a detailed description thereof is not repeated herein.

[0080] Subsequently, third vias **260** are respectively formed in the third opening **251**. In some embodiments, each of the third vias **260** includes a barrier layer **262** and a filling material **264** over the barrier layer **262**. Since the formation of the third vias **260** and the material thereof are similar to the first vias **160** in FIGS. **8**A and **8**B, a detailed description thereof is not repeated herein.

[0081] In operation S**56** of method M**40** in FIG. **17**B, a plurality of second MTJ stacks **170** are formed over the third vias **260**, as shown in FIGS. **26**A and **26**B. For example, a MTJ structure (e.g., the MTJ structure in FIG. **15**A) may be formed over the third dielectric layer **250** and covers the third vias **260**. A patterned mask layer is then formed over the MTJ structure and exposes portions of the MTJ structure. The MTJ structure is subsequently patterned using the patterned mask layer as a mask to form the second MTJ stacks **170**, and the patterned mask layer is removed. The second MTJ stacks **170** are respectively formed over the third vias **260**. In other words, the second MTJ stacks **170** are electrically connected to the middle conductive lines **240** respectively through the third vias **260**. In FIG. **26**A, the first MTJ stacks **130** and the second MTJ stacks **170** may have similar arrangement to the first MTJ stacks **130** and the second MTJ stacks **170** in FIG. **10**A. Thus, the description thereof is not repeated herein.

[0082] In operation S**58** of method M**40** in FIG. **17**B, a second dielectric structure **270** is formed

over the second MTJ stacks **170**, as shown in FIGS. **27**A, **27**B, **28**A, and **28**B. Reference is made to FIGS. **27**A and **27**B. A second encapsulation layer **272** is formed over the second MTJ stacks **170** and the middle conductive lines **240**, lining the upper surface and sidewalls of the second MTJ stacks **170**. In some embodiments, the second encapsulation layer **272** may be formed by suitable deposition technique and may be formed conformally. Further, the second encapsulation layer **272** may have the same or similar materials to the first encapsulation layer **152** of FIG. **5**B. The second encapsulation layer **272** may have a thickness in a range from about 0.1 nm to about 1000 nm.
[0083] Then, a fourth dielectric layer **274** is formed over the second encapsulation layer **272** and covers the second MTJ stacks **170**. The fourth dielectric layer **274** may have the same or similar materials to the first dielectric layer **154** of FIG. **5**B. The fourth dielectric layer **274** may have a thickness in a range from about 0.1 nm to about 1000 nm.
[0084] Reference is made to FIG. **28**A and **28**B. A planarization process is performed to the fourth dielectric layer **274** and the second encapsulation layer **272** until top surfaces of the second MTJ stacks **170** are exposed. For example, the planarization process is a CMP process.
[0085] Then, a fifth dielectric layer **276** is formed over the second encapsulation layer **272** and the fourth dielectric layer **274**, and covers the second MTJ stacks **170**. The fifth dielectric layer **276** may have the same or similar materials to the first dielectric layer **154** of FIG. **5**B. The fifth dielectric layer **276** may have a thickness in a range from about 0.1 nm to about 1000 nm. The fifth dielectric layer **276**, the fourth dielectric layer **274**, and the second encapsulation layer **272** are together referred to as the second dielectric structure **270**.
[0086] In operation S**60** of method M**40** in FIG. **17**B, a plurality of fourth vias **280** and a plurality of top conductive lines **290** are formed in the second dielectric structure **270**, as shown in FIGS. **29**A, **29**B, **30**A, **30**B, **31**A, and **31**B. Reference is made to FIGS. **29**A and **29**B. Another patterned mask layer M**8** is formed over the second dielectric structure **270**. The patterned mask layer M**8** may have the same or similar materials to the patterned mask layer M**1** of FIGS. **3**A and **3**B. The patterned mask layer M**8** may have a thickness in a range from about 0.1 nm to about 1000 nm.
[0087] Then, a plurality of fourth openings **271** are formed in the second dielectric structure **270**. The second dielectric structure **270** is patterned (etched) using the patterned mask layer M**8** as a mask to form the fourth openings **271** in the second dielectric structure **270**. The fourth openings **271** respectively expose portions of the middle conductive lines **240**.
[0088] Reference is made to FIGS. **30**A and **30**B. The patterned mask layer M**8** (see FIGS. **29**A and **29**B) is removed by using stripping, ashing, or etching process (such as reactive ion etching (RIE), ion beam etching (IBE), wet etching, or combinations thereof). Then, another patterned mask layer M**9** is formed over the second dielectric structure **270**. The patterned mask layer M**9** may have the same or similar materials to the patterned mask layer M**1** of FIGS. **3**A and **3**B. The patterned mask layer M**9** may have a thickness in a range from about 0.1 nm to about 1000 nm.
[0089] Then, a plurality of trenches **273** are formed in the second dielectric structure **270**. The second dielectric structure **270** is patterned (etched) using the patterned mask layer M**9** as a mask to form the trenches **273** in the second dielectric structure **270**. The trenches **273** expose the second MTJ stacks **170**.
[0090] Reference is made to FIGS. **31**A and **31**B. The patterned mask layer M**9** (see FIG. **31**A) is removed by using stripping, ashing, or etching process (such as reactive ion etching (RIE), ion beam etching (IBE), wet etching, or combinations thereof). Then, barrier layers **282** and **292** are conformally formed in the fourth openings **271** and the trenches **273**. The barrier layers **282** and **292** can improve the adhesion between the second MTJ stacks **170** or the middle conductive lines **240** and a material formed thereon (such as the filling materials **284** and **294**), or prevent a diffusion of a metal from diffusing from the via/line into the second dielectric structure **270**. The barrier layers **282** and **292** may have the same or similar materials to the barrier layers **162** of FIG. **8**B. The barrier layers **282** and **292** may have a thickness in a range from about 0.1 nm to about 1000 nm.

[0091] Filling materials **284** and **294** are respectively formed in the fourth openings **271** and the trenches **273** (see FIGS. **30**A and **30**B). The filling materials **284** and **294** are electrically connected to the second MTJ stacks **170** and the middle conductive lines **240**. The formations of the barrier layers **282** and **292** and the filling materials **284** and **294** are similar to or the same as the formations of the barrier layers **192** and **197** and the filling materials **194** and **199** of FIG. **14**B. The filling materials **284** and **294** may have the same or similar materials to the filling material **194** and **199** of FIG. **14**B. The filling material **284** and the barrier layer **282** are referred to as the fourth via **280**, and the filling material **294** and the barrier layer **292** are referred to as the top conductive lines **290**.

[0092] In FIG. **31**A, the top conductive lines **290** and the middle conductive lines **240** extend in different directions. For example, the top conductive lines **290** extend in the X direction, and the middle conductive lines **240** extend in the Y direction. In some embodiments, the top conductive lines **290** and the bottom conductive lines **120** extend in the same direction (e.g., the X direction in this case). Further, one of the top conductive lines **290** is electrically connected to one first MTJ stack **130** and one second MTJ stack **170**, where these first MTJ stack **130** and second MTJ stack **170** are arranged along the Y direction.

[0093] FIG. **32** is a perspective view of the memory device in FIGS. **31**A and **31**B in accordance with various embodiments of the present disclosure. The dielectric materials (such as the first dielectric layer **205**, the first dielectric structure **220**, the third dielectric layer **250**, and the second dielectric structure **270** in FIG. **31**B) are omitted in FIG. **32** for clarity. Also, the barrier layers in the vias and or conductive lines are not shown in FIG. **32** for clarity. The memory device includes a plurality of bottom conductive lines **120**, a plurality of first MTJ stacks **130**, a plurality of middle conductive lines **240**, a plurality of second MTJ stacks **170**, and a plurality of top conductive lines **290**. The bottom conductive lines **120** are disposed over a wafer **110**. The first MTJ stacks **130** are respectively disposed over the bottom conductive lines **120**. In some embodiments, the first MTJ stacks **130** are electrically connected to the bottom conductive lines **120** respectively through first vias **210**. The middle conductive lines **240** are disposed over the first MTJ stacks **130**. In some embodiments, the first MTJ stacks **130** are respectively in contact with the middle conductive lines **240**. The second MTJ stacks **170** are at a different level from the first MTJ stacks **130** and disposed over the middle conductive lines **240**. The top surface **170***t* of the second MTJ stack **170** is higher than the top surface **130***b* of the first MTJ stack **130** (see FIG. **31**B). The second MTJ stacks **170** are electrically connected to the middle conductive lines **240** respectively through third vias **260**. The top conductive lines **290** are disposed over the first MTJ stacks **130** and the second MTJ stacks **170**. In some embodiments, the second MTJ stacks **170** are respectively in contact with the top conductive lines **290**. In some embodiments, second vias **230** are formed between the bottom conductive lines **120** and the middle conductive lines **240** to interconnect the second MTJ stack **170** and the bottom conductive line **120**. In some embodiments, fourth vias **280** are formed between the top conductive lines **290** and the middle conductive lines **240** to interconnect the first MTJ stack **130** and the top conductive line **290**.

[0094] The first MTJ stack **130**, the first via **210**, and the fourth via **280** form a memory cell C**3**, and the second MTJ stack **170**, the second via **230**, and the third via **260** form another memory cell C**4**. The memory cells C**3** and C**4** are alternately arranged. The two memory cells C**3** and C**4** are adjacent to each other but the MTJ stacks thereof are at different levels. For example, in FIG. **32**, the second MTJ stack **170** is at a level higher than the first MTJ stack **130**. More specific, the first MTJ stacks **130** are between the bottom conductive lines **120** and the middle conductive lines **240**, and the second MTJ stacks **170** are between the middle conductive lines **240** and the top conductive lines **290**. With this configuration, the memory cell C**3** may be close to the memory cell C**4** (e.g., the first MTJ stack **130** and the second MTJ stack **170** may overlap with each other in a top view), and the layout area of the memory device can be reduced.

[0095] FIG. **33** is a top view of the memory device in accordance with various embodiments of the

present disclosure, and FIG. **34** is a perspective view of an area P of FIG. **33** in accordance with various embodiments of the present disclosure. For clarity, top conductive lines **360** FIG. **34** are not shown in FIG. **33**. The memory device includes a plurality of bottom conductive lines **320**, a plurality of first MTJ stacks **330**, a plurality of second MTJ stacks **340**, a plurality of third MTJ stacks **350**, and a plurality of top conductive lines **360**.

[0096] The bottom conductive lines **320** are disposed over a wafer **310** which may have the same or similar to the wafer **110** of FIGS. **2**A and **2**B. The first MTJ stacks **330**, the second MTJ stacks **340**, and the third MTJ stacks **350** are disposed over the bottom conductive lines **320**. The first MTJ stacks **330**, the second MTJ stacks **340**, and the third MTJ stacks **350** are at different levels. For example, a top surface **350***t* of the third MTJ stack **350** is higher than a top surface **340***t* of the second MTJ stack **340**, and the top surface **340***t* of the second MTJ stack **340** is higher than a top surface **330***t* of the first MTJ stack **330**. In some embodiments, the first MTJ stacks **330** may be in contact with the bottom conductive lines **320** as shown in FIG. **34**. In some other embodiments, the first MTJ stacks **330** are electrically connected to the bottom conductive lines **320** through via(s). The first MTJ stacks **330** may be electrically connected to the top conductive lines **360** through vias **334**. The second MTJ stacks **340** are higher than the first MTJ stacks **330**. In some embodiments, the second MTJ stacks **340** are electrically connected to the bottom conductive lines **320** through vias **342** and to the top conductive lines **360** through vias **344**. The third MTJ stacks **350** are higher than the first MTJ stacks **330** and the second MTJ stacks **340**. In some embodiments, the third MTJ stacks **350** are electrically connected to the bottom conductive lines **320** through vias **352** and to the top conductive lines **360** through vias **354**. In some embodiments, the bottom conductive lines **320** and the top conductive lines **360** are not parallel. The bottom conductive lines **320** and the top conductive lines **360** extend in different directions. An angle may be formed between extension directions of the bottom conductive lines **320** and the top conductive lines **360**, and the angle may be in a range of about 50 degrees to about 70 degrees, e.g., about 60 degrees.

[0097] The first MTJ stack **330** and the via **334** form a memory cell C**1**′, the second MTJ stack **340** and the vias **342** and **344** form a memory cell C**2**′, and the third MTJ stack **350** and the vias **352** and **354** form a memory cell C**3**′. The memory cells C**1**′, C**2**′, and C**3**′ are alternately arranged and form a honeycomb shape in a top view (see FIG. **33**). The density of the memory cells depends on the distance between two MTJ stacks at the same level. For example, in FIG. **33**, a distance dl is between the first MTJ stacks **330**, a distance d**2** is between the second MTJ stacks **340**, and a distance d**3** is between the third MTJ stacks **350**. Since the distances d**1**, d**2**, and d**3** can be small (as long as greater than the lithography limitation), the first MTJ stacks **330**, the second MTJ stacks **340**, and the third MTJ stacks **350** may overlap with each other in the top view. Moreover, the memory cells C**1**′, C**2**′, and C**3**′ have substantially the same height. That is, a total height of the first MTJ stack **330** and the via **334**, a total height of the second MTJ stack **340** and the vias **342** and **344**, and a total height of the third MTJ stack **350** and the vias **352** and **354** may be substantially the same.

[0098] The bottom conductive lines **320** may have the same or similar materials to the bottom conductive lines **120** in FIG. **14**B. The top conductive lines **360** may have the same or similar materials to the top conductive lines **195** in FIG. **14**B. The first MTJ stacks **330**, the second MTJ stacks **340**, and the third MTJ stacks **350** may have the same or similar materials to the first MTJ stacks **130** and/or the second MTJ stacks **170** in FIG. **14**B.

[0099] The MTJ stacks in FIGS. **16** and **32** are at two levels, and the MTJ stacks in FIG. **34** are at three levels. In some other embodiments, however, the MTJ stacks may be distributed in N levels, where N is greater than 3. Furthermore, some of the MTJ stacks may be between n and n+1 conductive lines, and some other of the MTJ stacks may be between m and m+1 conductive lines, where n is equal to m or not equal to m.

[0100] FIG. **35** is a top view of a memory device in accordance with various embodiments of the

present disclosure. The memory device includes a wafer **410**, a memory structure **420**, and a logic device **430**. The wafer **410** may be a substrate, and the memory structure **420** and the logic device **430** are disposed over the wafer **410**. The memory structure **420** includes a plurality of memory cells C**1**, C**2** (see FIG. **16**), C**3**, C**4** (see FIG. **32**), C**1**′, C**2**′, C**3**′ (see FIG. **34**), or combinations thereof. The logic device **430** is electrically connected to the memory structure **420** to operate the memory cells in the memory structure **420**. Various logic circuitry, such as row and column decoders and/or sense amplifiers, can be included in the logic device **430**. The logic device **430** may further include other logic such as counters, clock circuits, processing circuits, and or input/output circuitry such as buffers and drivers. In this case, the memory cells of the memory structure **420** are stand-alone memories.

[0101] FIG. **36** is a top view of a memory device in accordance with various embodiments of the present disclosure. The memory device includes a wafer **510** and a memory structure **520** over the wafer **510**. The wafer **510** includes a plurality of (access) transistors and an inter-metal dielectric (IMD) layer over the transistors. In some embodiments, the transistor may be planar MOSFET, BJT, FinFET, or gate-all-around FET (GAAFET). The IMD layer interconnects the transistors and the memory cells in the memory structure **520**. As such, the memory cell is referred to as an embedded memory and memory device has one-transistor-one-MTJ memory configuration. In some other embodiments, the memory structure **520** is in the IMD layer. Some levels of the IMD layer are configured to interconnect the memory cells and the transistors, and some other levels of the IMD layer are configured to form the memory cells. The memory cells may be formed in arbitrary levels of the IMD layer. The memory structure **420** includes a plurality of memory cells C**1**, C**2** (see FIG. **16**), C**3**, C**4** (see FIG. **32**), C**1**′, C**2**′, C**3**′ (see FIG. **34**), or combinations thereof. Therefore, the memory structure **420** may have a smaller layout area than the layout area **515** of the transistors. As such, a portion of the area M above the transistors may be available for other circuits or devices to be formed.

[0102] Based on the above discussions, it can be seen that the present disclosure offers advantages. It is understood, however, that other embodiments may offer additional advantages, and not all advantages are necessarily disclosed herein, and that no particular advantage is required for all embodiments. One advantage is that the MTJ stacks of adjacent memory cells are at different levels (or vertically staggered), such that the memory cells can be close to each other, and the layout area of the memory cells can be reduced. Another advantage is that the MTJ stacks may be formed in different levels of the IMD layer. As such, it is more flexible to design the position of the memories.

[0103] According to some embodiments, a method includes forming bottom conductive lines over a wafer. A first magnetic tunnel junction (MTJ) stack is formed over the bottom conductive lines. Middle conductive lines are formed over the first MTJ stack. A second MTJ stack is formed over the middle conductive lines. Top conductive lines are formed over the second MTJ stack.

[0104] According to some embodiments, a method includes forming bottom conductive lines over a substrate; forming a first magnetic tunnel junction (MTJ) stack over the bottom conductive lines and electrically connected to one of the bottom conductive lines; forming a first dielectric structure over the bottom conductive lines and covering the first MTJ stack; forming a first via in the first dielectric structure and in contact with the one of the bottom conductive lines; forming a second magnetic tunnel junction (MTJ) stack over the first dielectric structure and electrically connected to the first via; forming a second dielectric structure over the first dielectric structure and covering the second MTJ stack; and forming a second via in the first and second dielectric structures and in contact with the first MTJ stack.

[0105] According to some embodiments, a method includes forming first and second bottom conductive lines over a substrate and extending along a first direction; forming a first MTJ stack over the first bottom conductive line; forming a first via over the first bottom conductive line after forming the first MTJ stack, wherein the first MTJ stack and the first via are arranged along the

first direction; forming a second MTJ stack over the second bottom conductive line after forming the first via, wherein the second MTJ stack and the first MTJ stack are arranged along a second direction perpendicular to the first direction; and forming a second via over the second bottom conductive line after forming the second MTJ stack, wherein the second via and the second MTJ stack are arranged along the first direction.

[0106] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

Claims

1. A method, comprising: forming bottom conductive lines extending along a first direction; forming a first memory cell over one of the bottom conductive lines and a second memory cell over another one of the bottom conductive lines; forming a third memory cell over the one of the bottom conductive lines and a fourth memory cell over the another one of the bottom conductive lines, wherein the third memory cell and the fourth memory cell are at a higher level than the first memory cell and the second memory cell; and forming top conductive lines above the bottom conductive lines, wherein one of the top conductive line vertically overlaps the first and third memory cells, and another one of the top conductive line vertically overlaps the second and fourth memory cells.

2. The method of claim 1, wherein the first memory cell is in direct contact with the one of the bottom conductive lines and the second memory cell is in direct contact with the another one of the bottom conductive lines.

3. The method of claim 1, wherein the third memory cell is in direct contact with the one of the top conductive lines and the fourth memory cell is in direct contact with the another one of the top conductive lines.

4. The method of claim 1, further comprising, after forming the first memory cell and the second memory cell, forming a first via and a second via over the one of the bottom conductive lines and the another one of the bottom conductive lines, respectively, wherein the first via electrically connects the third memory cell and the one of the bottom conductive lines, and the second via electrically connects the fourth memory cell and the another one of the bottom conductive lines.

5. The method of claim 4, wherein the first via is in direct contact with the one of the bottom conductive lines and the second via is in direct contact with the another one of the bottom conductive lines.

6. The method of claim 1, further comprising: forming a first encapsulation layer lining the first memory cell; forming a first dielectric layer over the first encapsulation layer; and performing a planarization process to the first encapsulation layer and the first dielectric layer until the first memory cell is exposed.

7. The method of claim 6, further comprising forming a second dielectric layer over the first encapsulation layer, the first dielectric layer, and the first memory cell, wherein the third memory cell and the fourth memory cell are formed over the second dielectric layer.

8. A method, comprising: forming a bottom conductive line; forming a first memory cell over and electrically connected to the bottom conductive line; forming a first encapsulation layer lining a sidewall of the first memory cell; forming a first dielectric layer over the first encapsulation layer; forming a second dielectric layer covering the first memory cell, the first encapsulation layer, and

the first dielectric layer; forming a first via extending through the first encapsulation layer, the first dielectric layer, and the second dielectric layer and electrically connected to the bottom conductive line; and forming a second memory cell over the second dielectric layer and electrically connected to the first via.

9. The method of claim 8, further comprising, prior to forming the second dielectric layer, performing a planarization process to the first encapsulation layer and the first dielectric layer until the first memory cell is exposed.

10. The method of claim 8, wherein the first via comprises a barrier layer and a filling material over the barrier layer.

11. The method of claim 8, wherein the first memory cell and the first via are in direct contact with the bottom conductive line.

12. The method of claim 8, further comprising: forming a second encapsulation layer lining the second memory cell; and forming a third dielectric layer over the second encapsulation layer.

13. The method of claim 12, further comprising forming a second via extending through the third dielectric layer, the second encapsulation layer, and the first dielectric layer, to the first memory cell.

14. The method of claim 13, further comprising forming a top conductive line in the third dielectric layer and over the second via.

15. The method of claim 14, wherein the second via and the top conductive line are formed by: forming an opening extending through the third dielectric layer, the second encapsulation layer, and the first dielectric layer; forming a trench in the third dielectric layer and spatially communicated with the opening; and filling the trench and the opening with metal.

16. A method, comprising: a bottom conductive line extending along a first direction; forming a first via vertically above and electrically connected to the bottom conductive line; forming a first memory cell vertically above and electrically connected to the first via; forming a middle conductive line above the bottom conductive line and extending along a second direction perpendicular to the first direction, the middle conductive line being vertically above and electrically connected to the first memory cell; forming a second memory cell vertically above and electrically connected to the middle conductive line; and forming a top conductive line above the middle conductive line and extending along the first direction, the top conductive line being vertically above and electrically connected to the second memory cell.

17. The method of claim 16, wherein the first via is in direct contact with the bottom conductive line.

18. The method of claim 16, further comprising forming a second via over the middle conductive line, wherein the second memory cell is formed over the second via.

19. The method of claim 16, wherein the first memory cell is in direct contact with the middle conductive line.

20. The method of claim 16, wherein the first memory cell and the second memory cell are arranged along the second direction.