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(54) **INTEGRATED CIRCUIT STRUCTURES  
HAVING PRE-SPACER DEPOSITION CUT  
GATES AND ASSOCIATED DEFECT TEST  
STRUCTURES**

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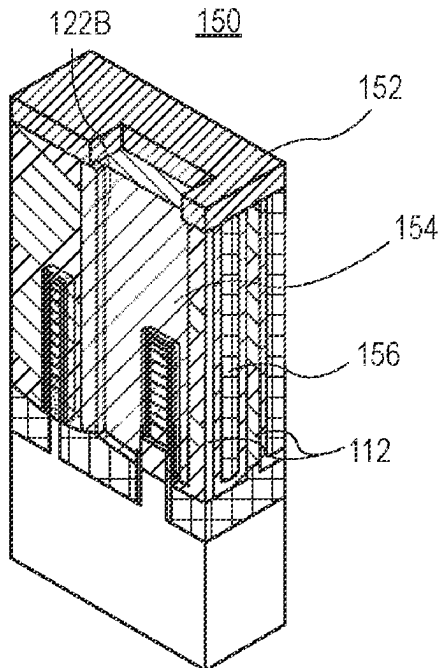
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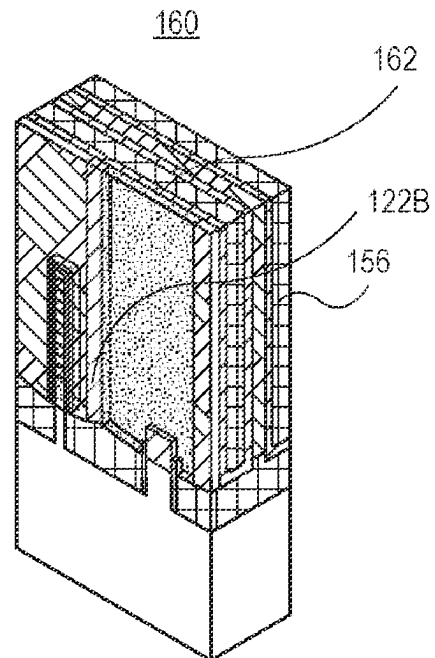
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**H10D 84/83** (2025.01)

(57) **ABSTRACT**

Integrated circuit structures having pre-spacer-deposition cut gates and associated defect test structures are described. For example, an integrated circuit structure includes a first and second fin or vertical arrangement of horizontal nanowires. First and second gate stacks are over the first and second fin or vertical arrangement of horizontal nanowires, respectively. An end of the second gate stack is spaced apart from an end of the first gate stack by a gap. A dielectric structure has first and second portions forming a gate spacer along sidewalls of the first and second gate stacks, respectively, and a third portion completely filling the gap, the third portion continuous with the first and second portions. The integrated circuit structure also includes an array having a periodic arrangement of alternating floating and grounded conductive trench contacts along a direction parallel with the first gate stack and the second gate stack.



(i)



(ii)

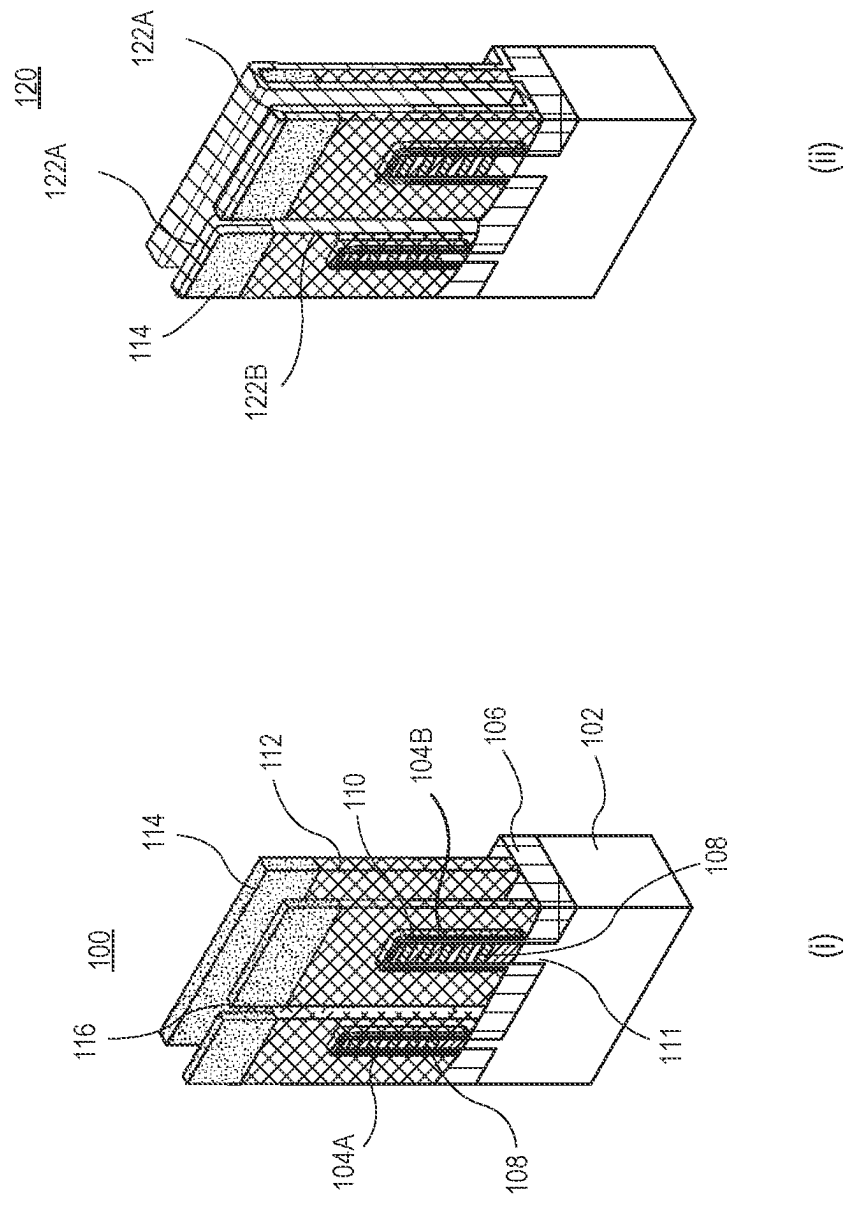


FIG. 1A

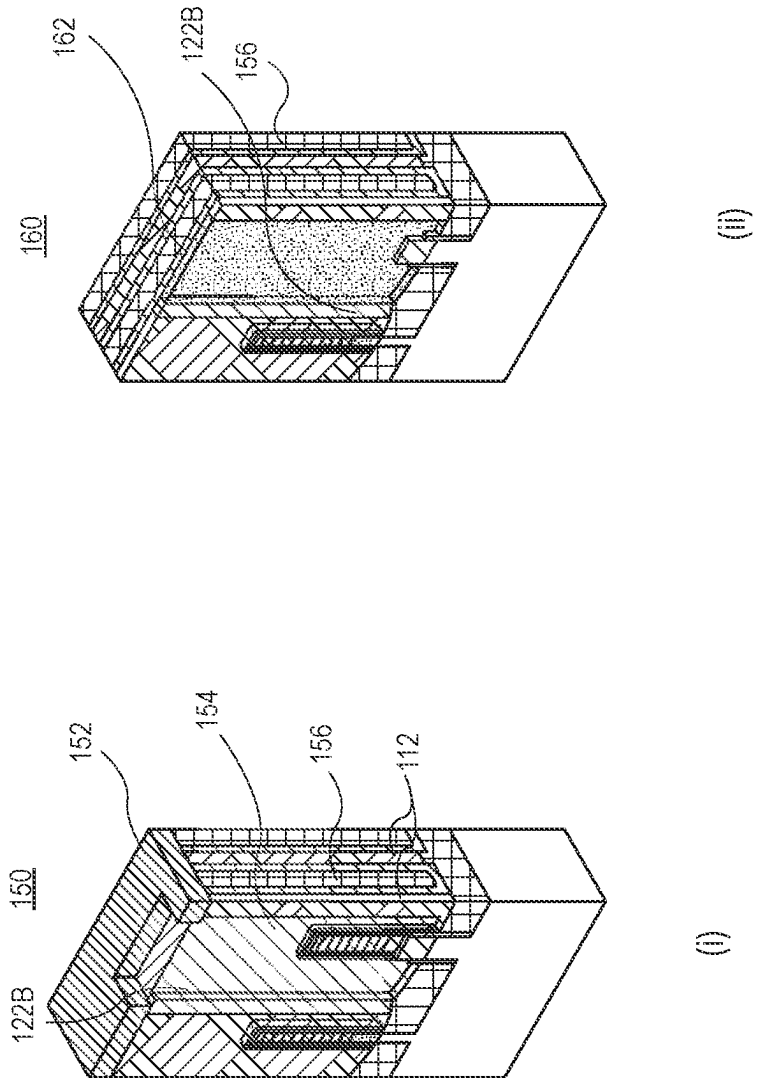
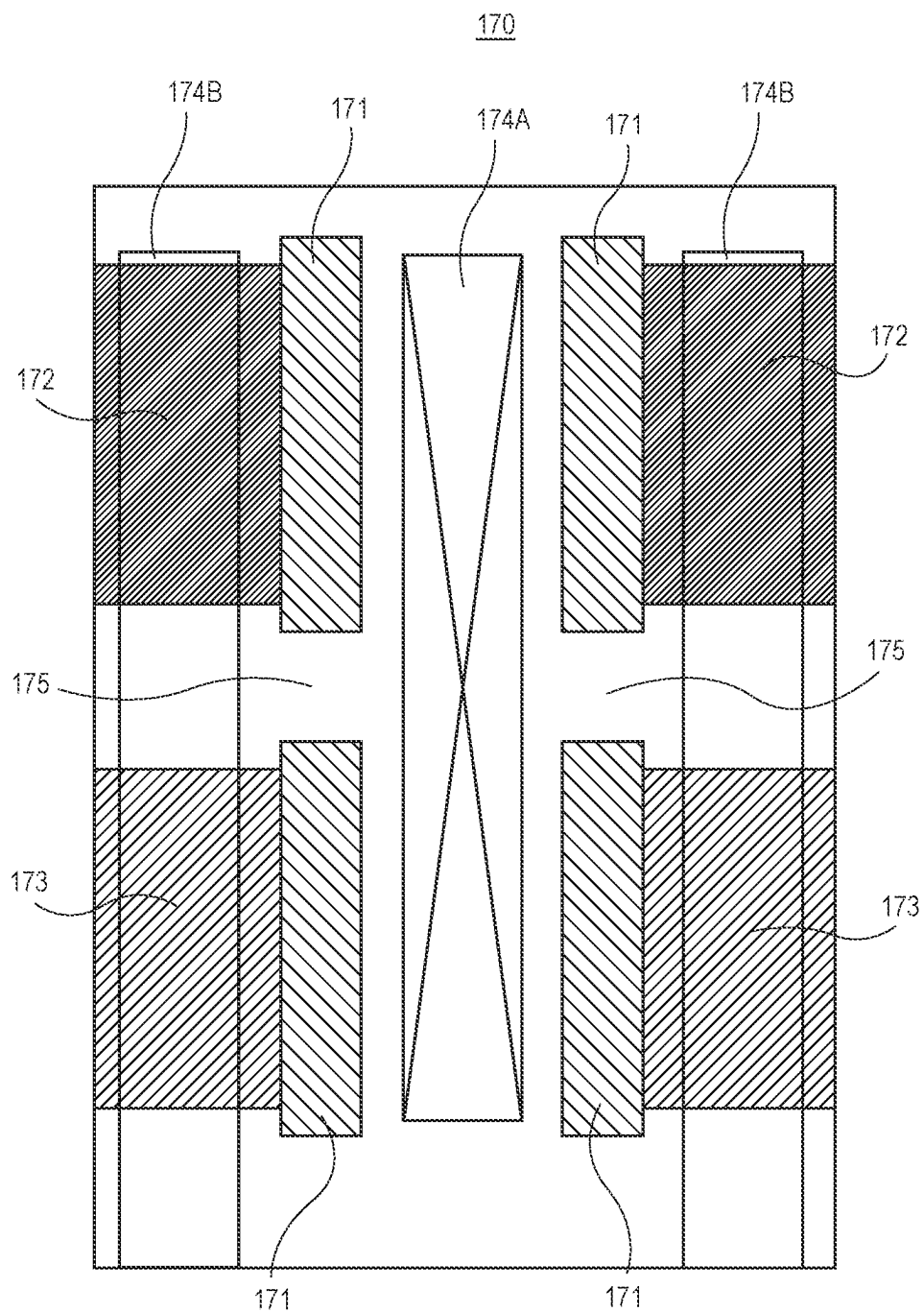


FIG. 1B



**FIG. 1C**

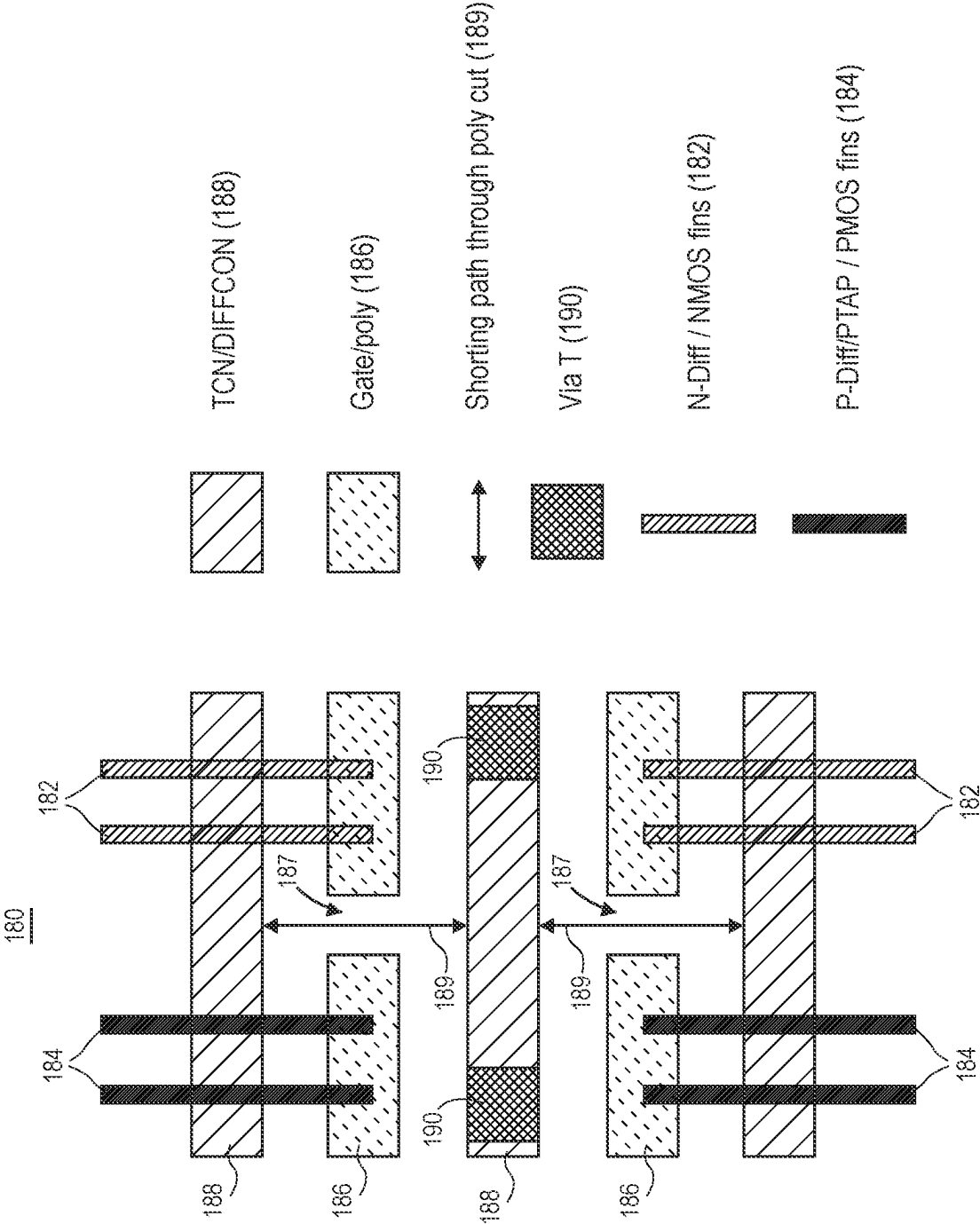


FIG. 1D

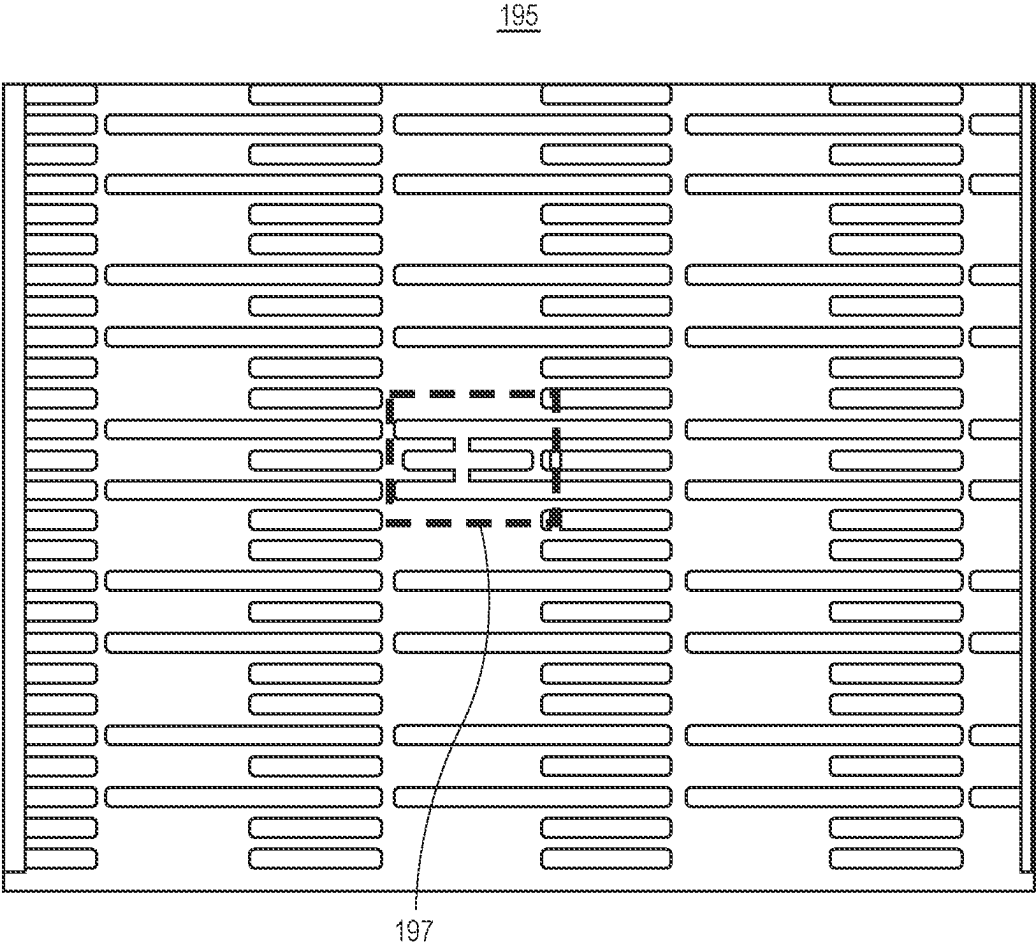


FIG. 1E

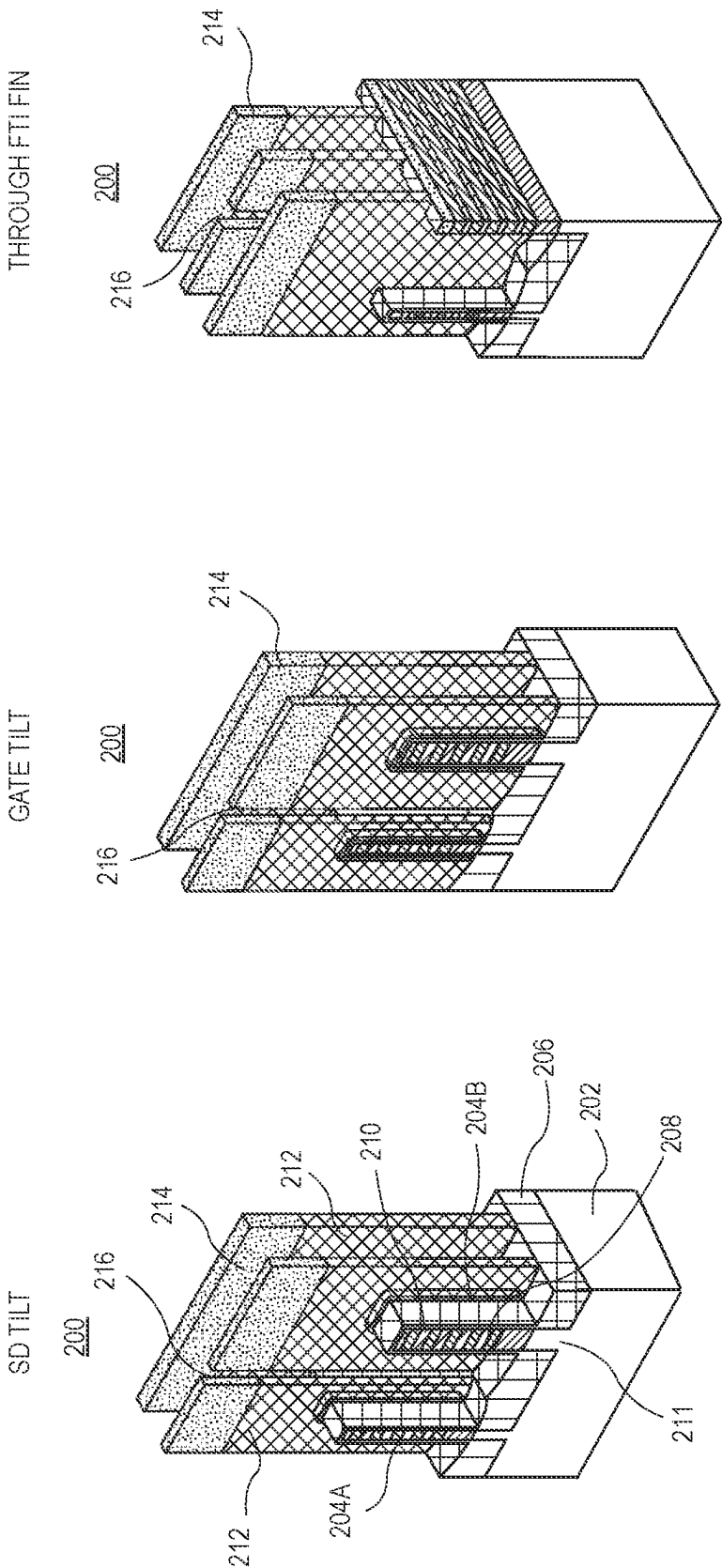


FIG. 2A

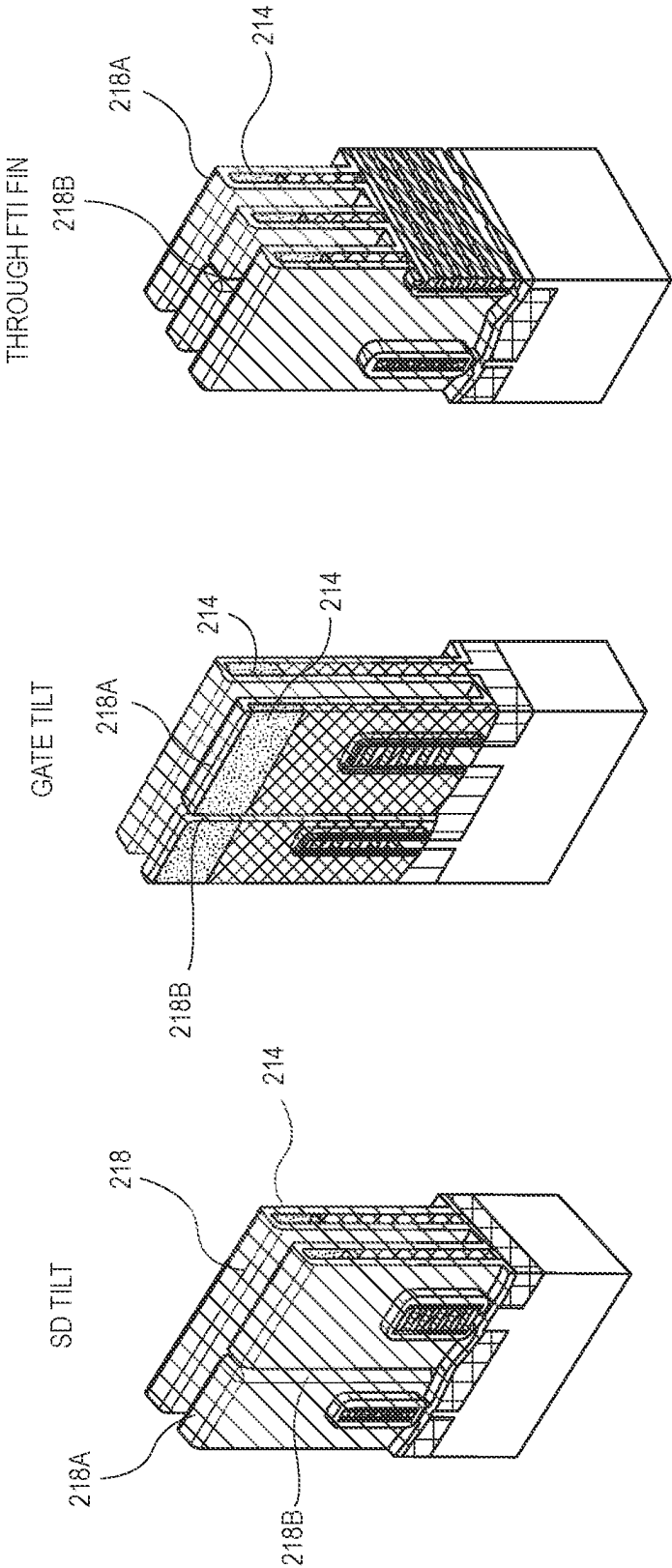


FIG. 2B



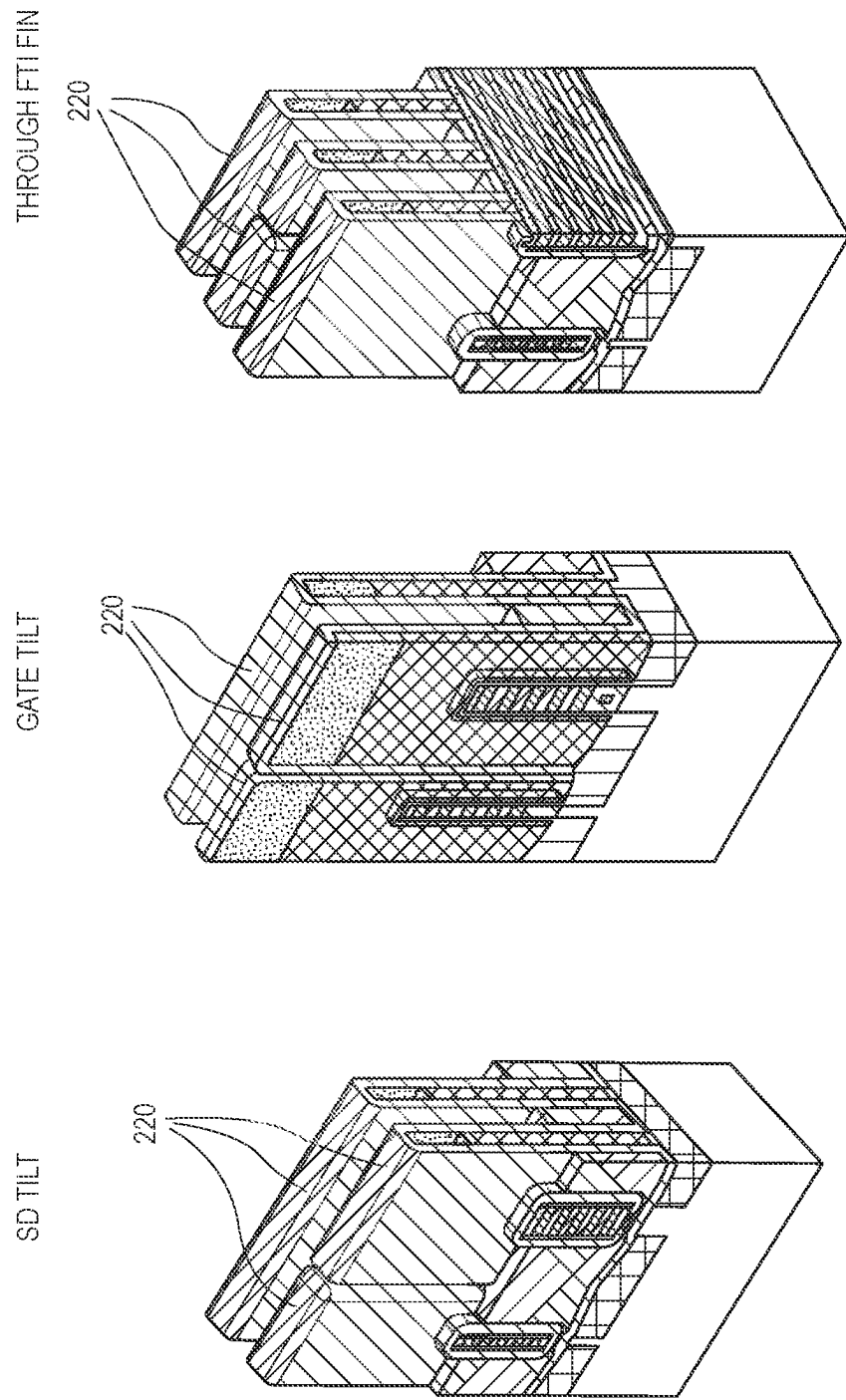


FIG. 2C

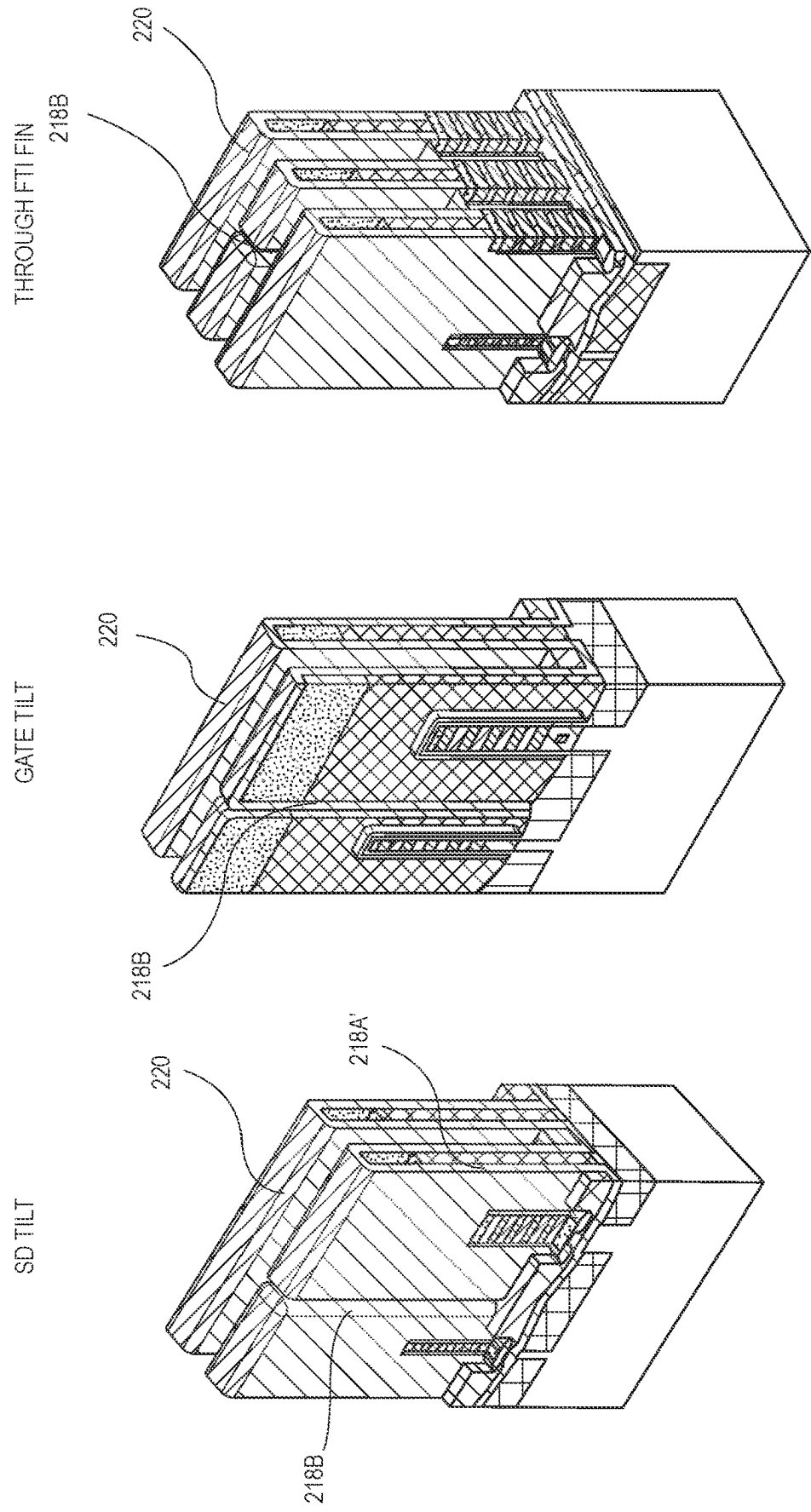


FIG. 2D

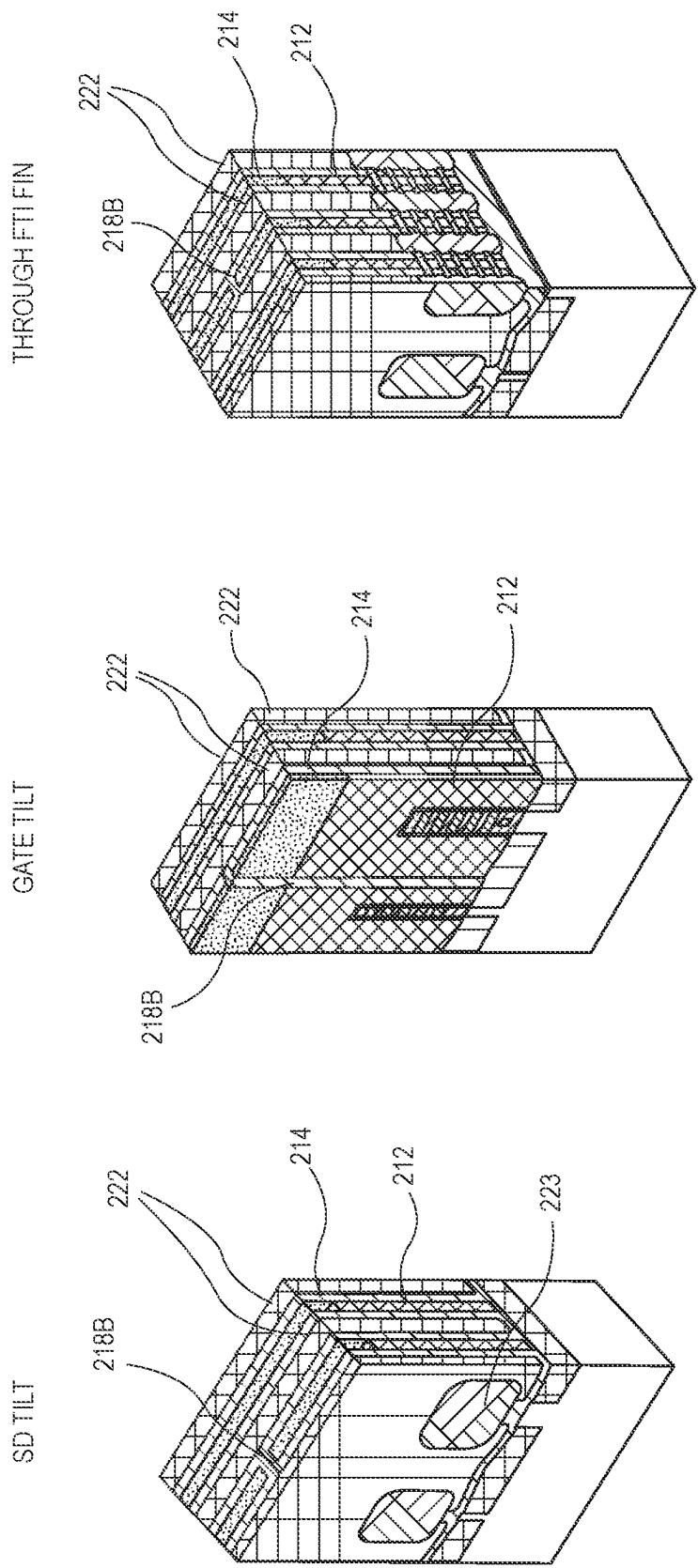


FIG. 2E

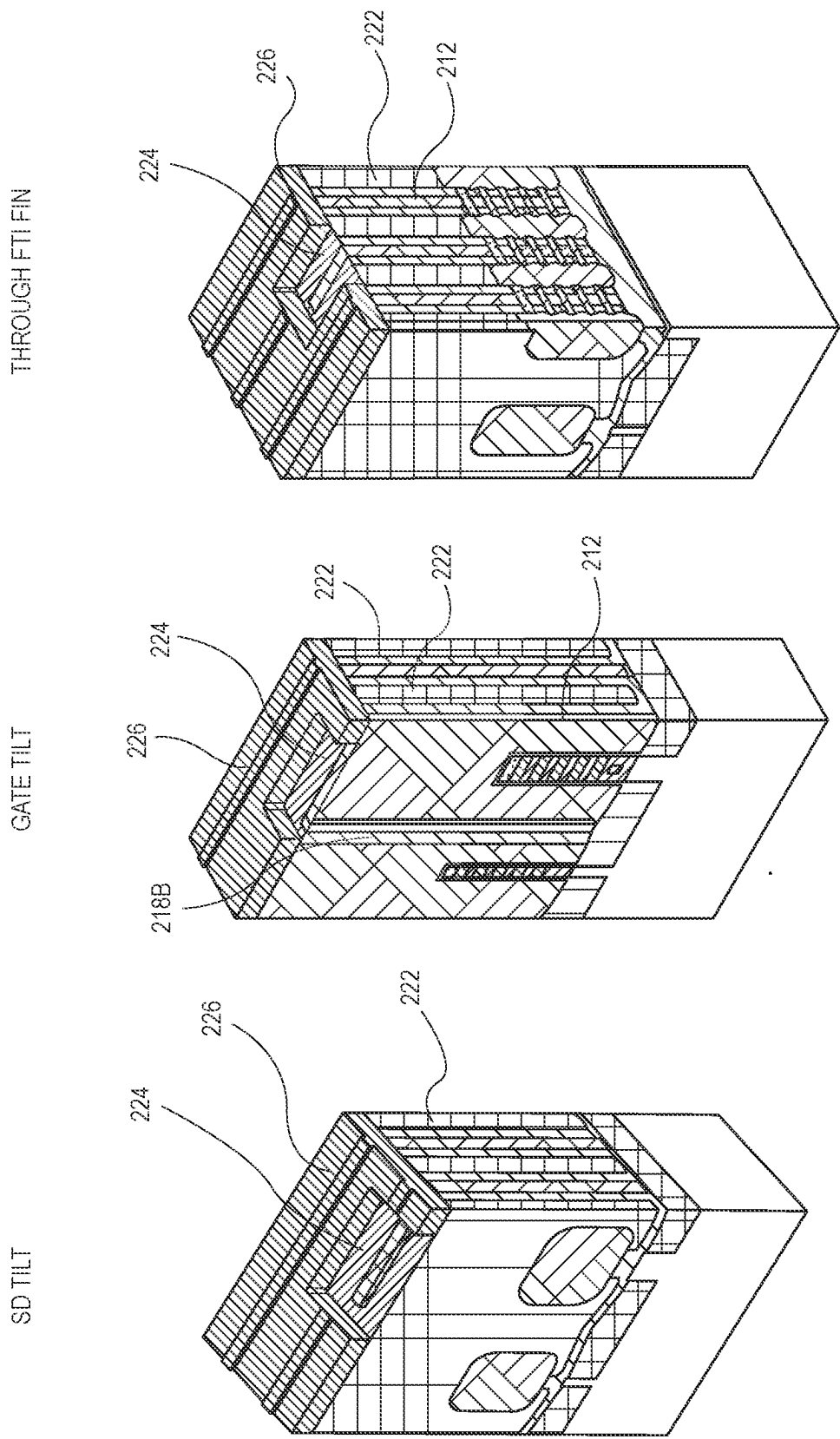


FIG. 2F

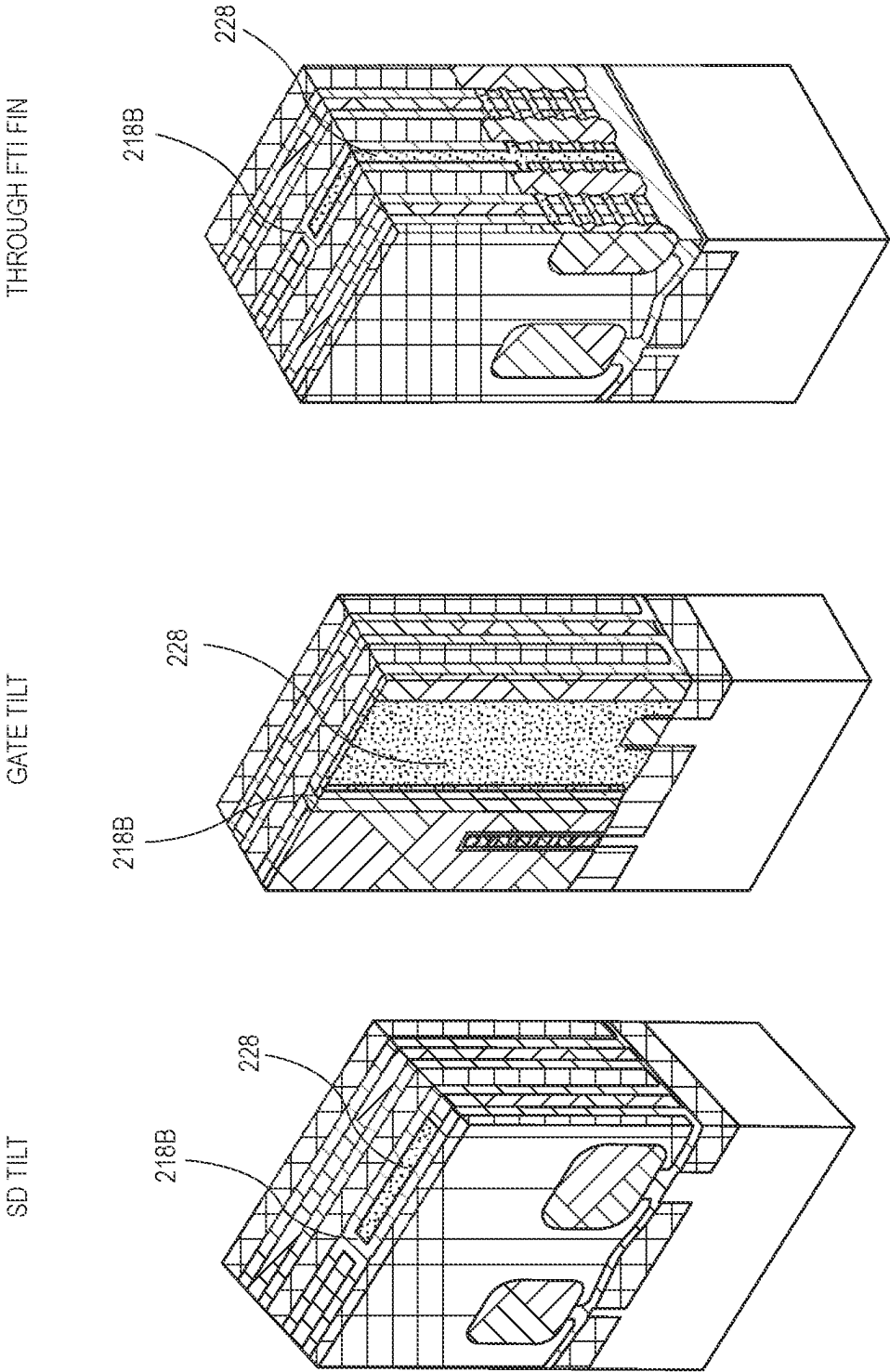


FIG. 2G

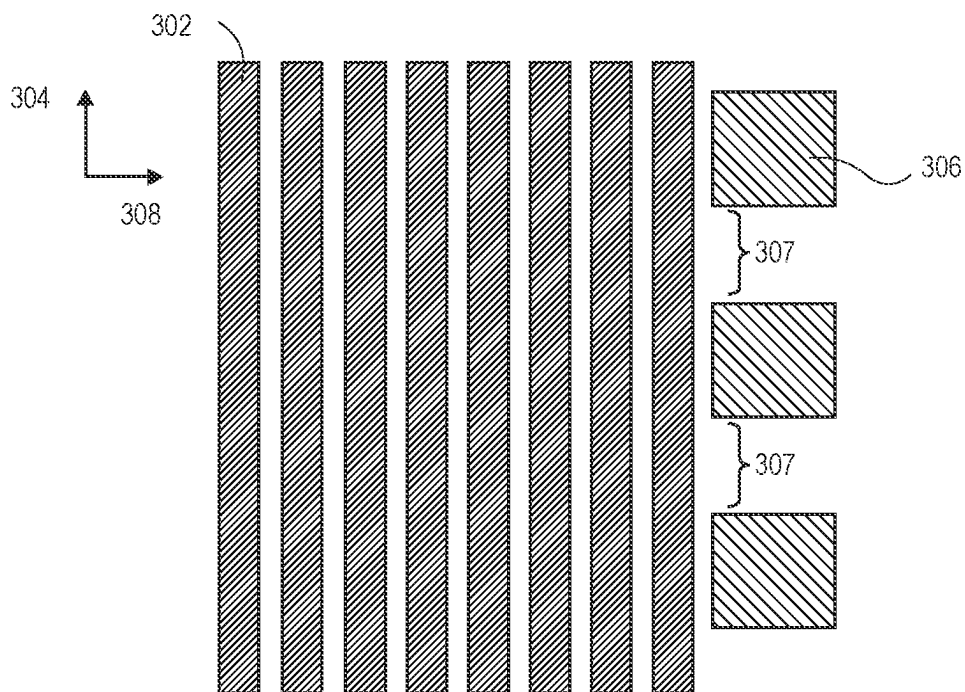


FIG. 3A

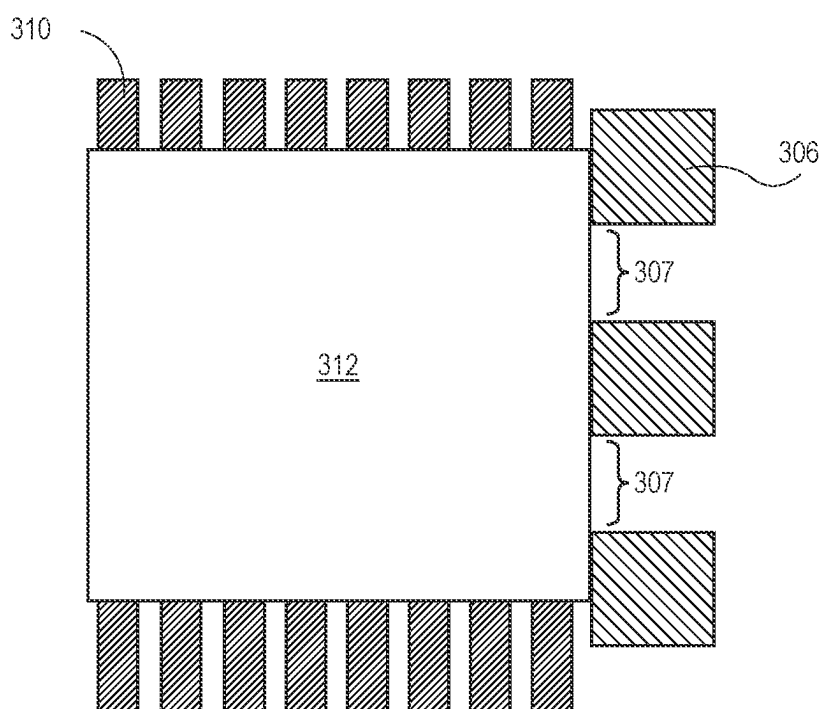


FIG. 3B

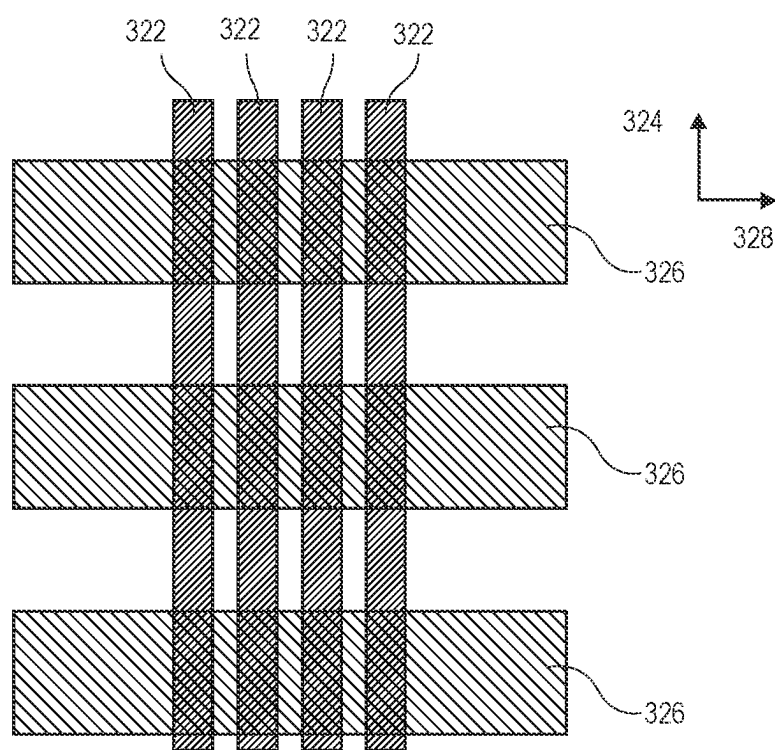


FIG. 3C

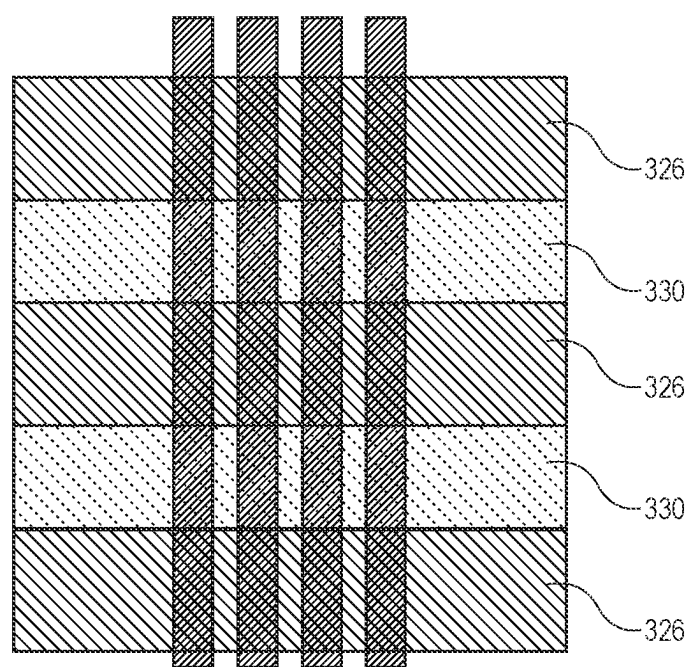


FIG. 3D

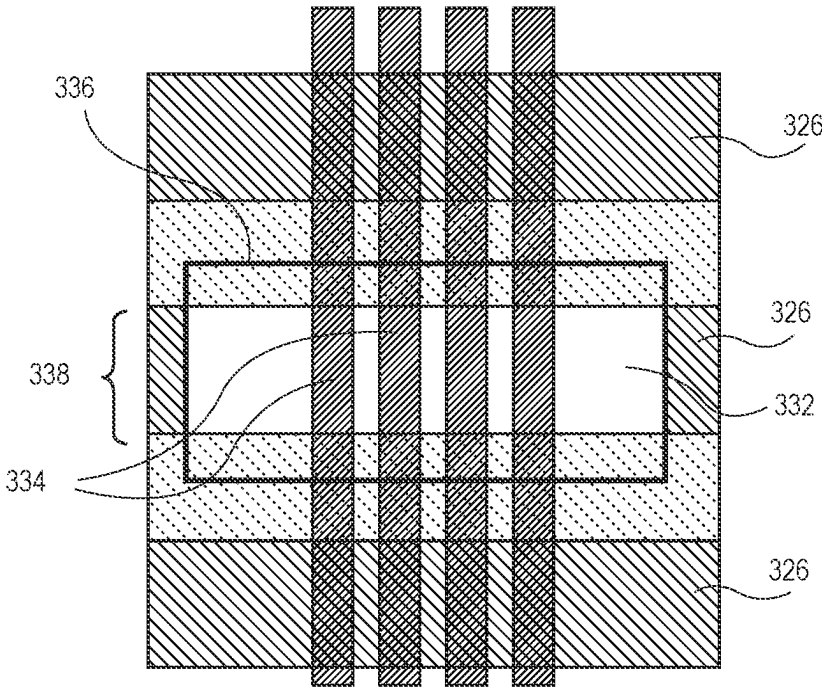


FIG. 3E

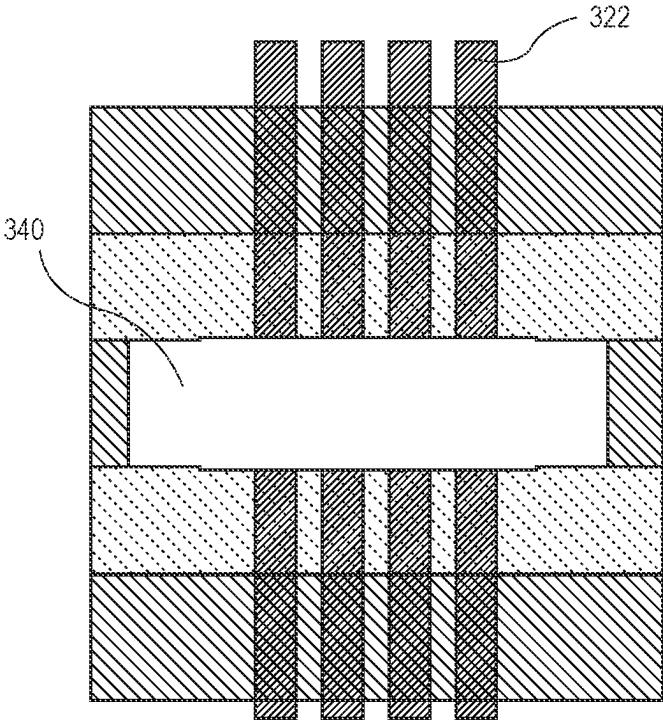


FIG. 3F



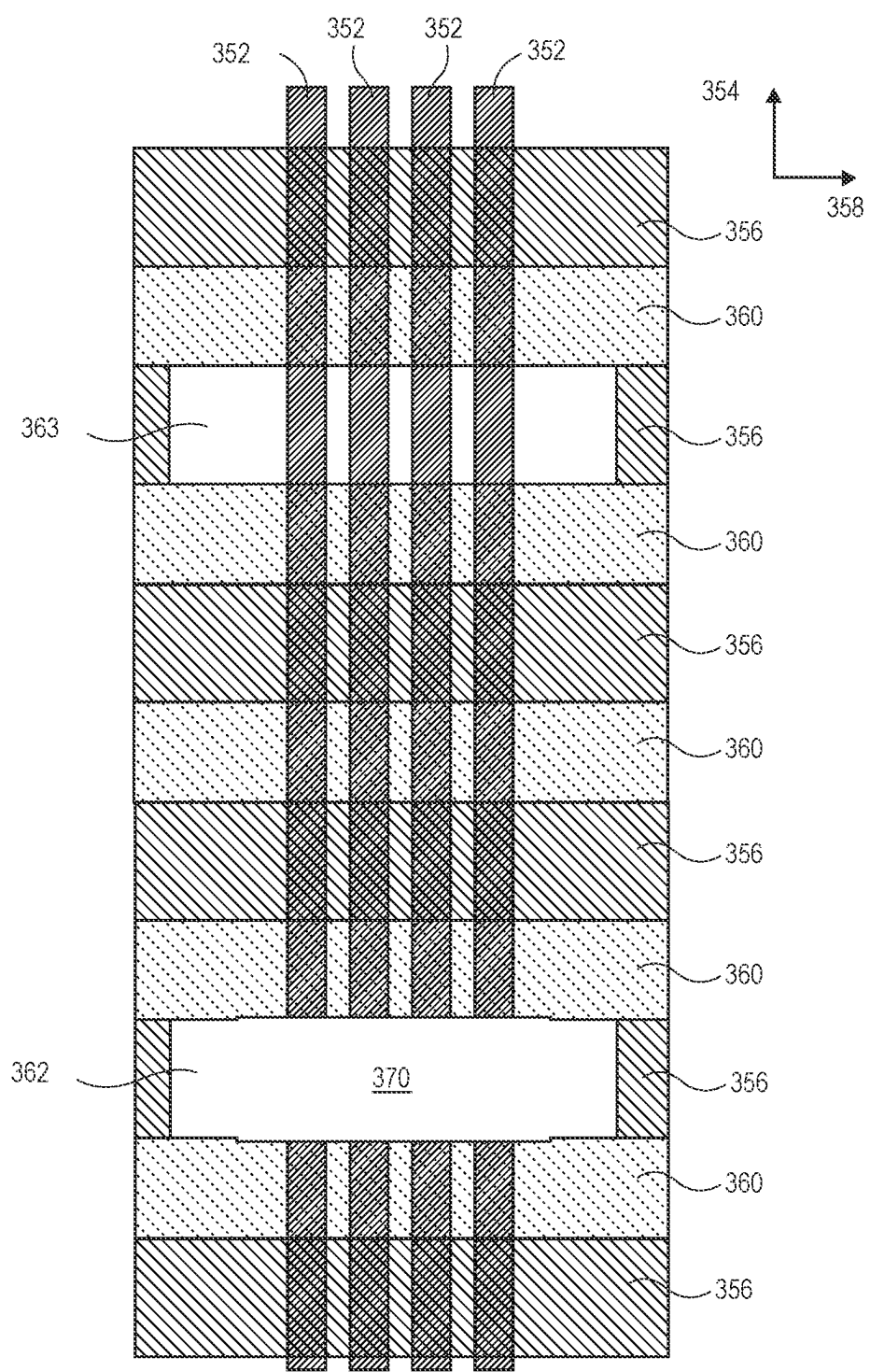


FIG. 3G

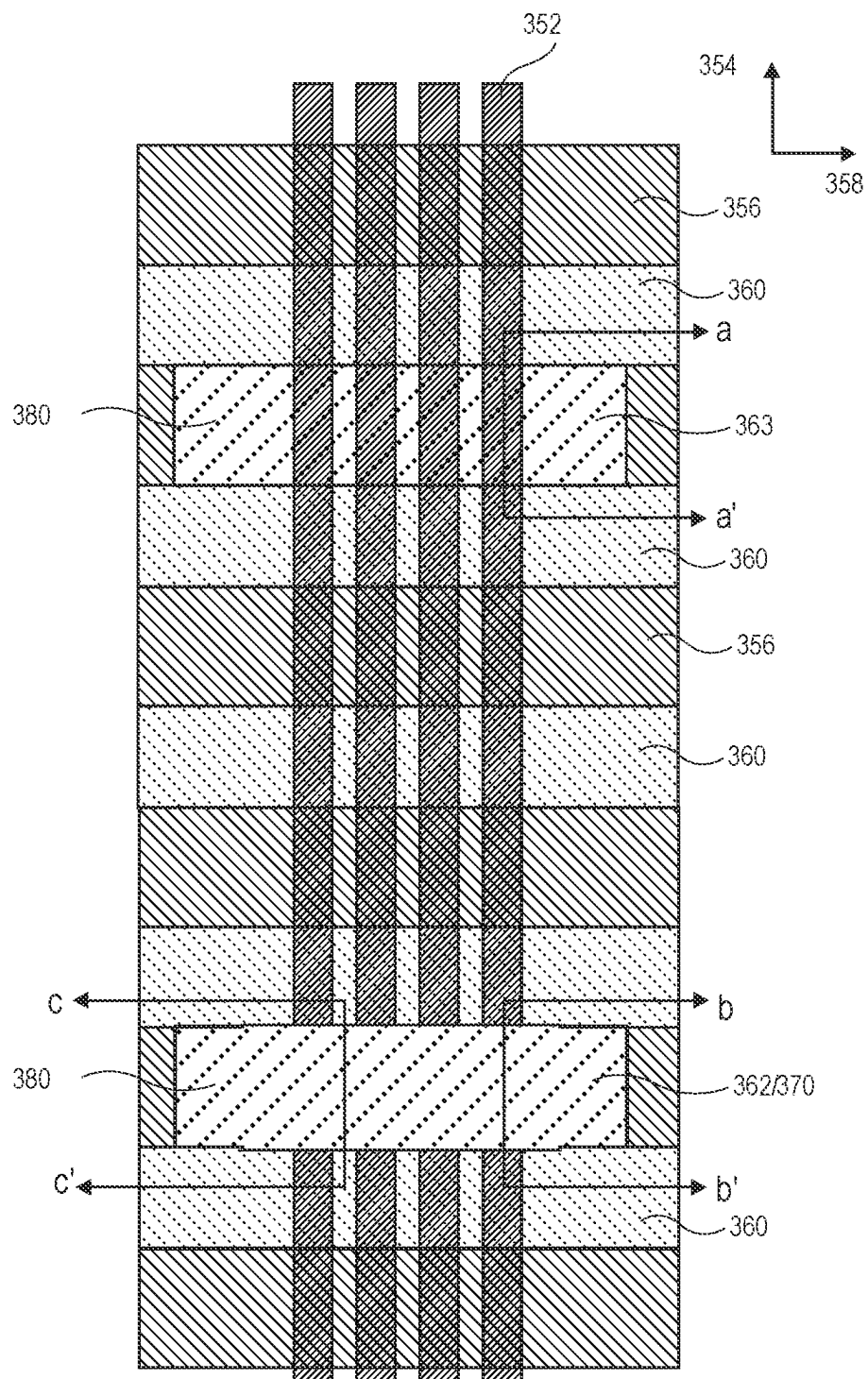


FIG. 3H

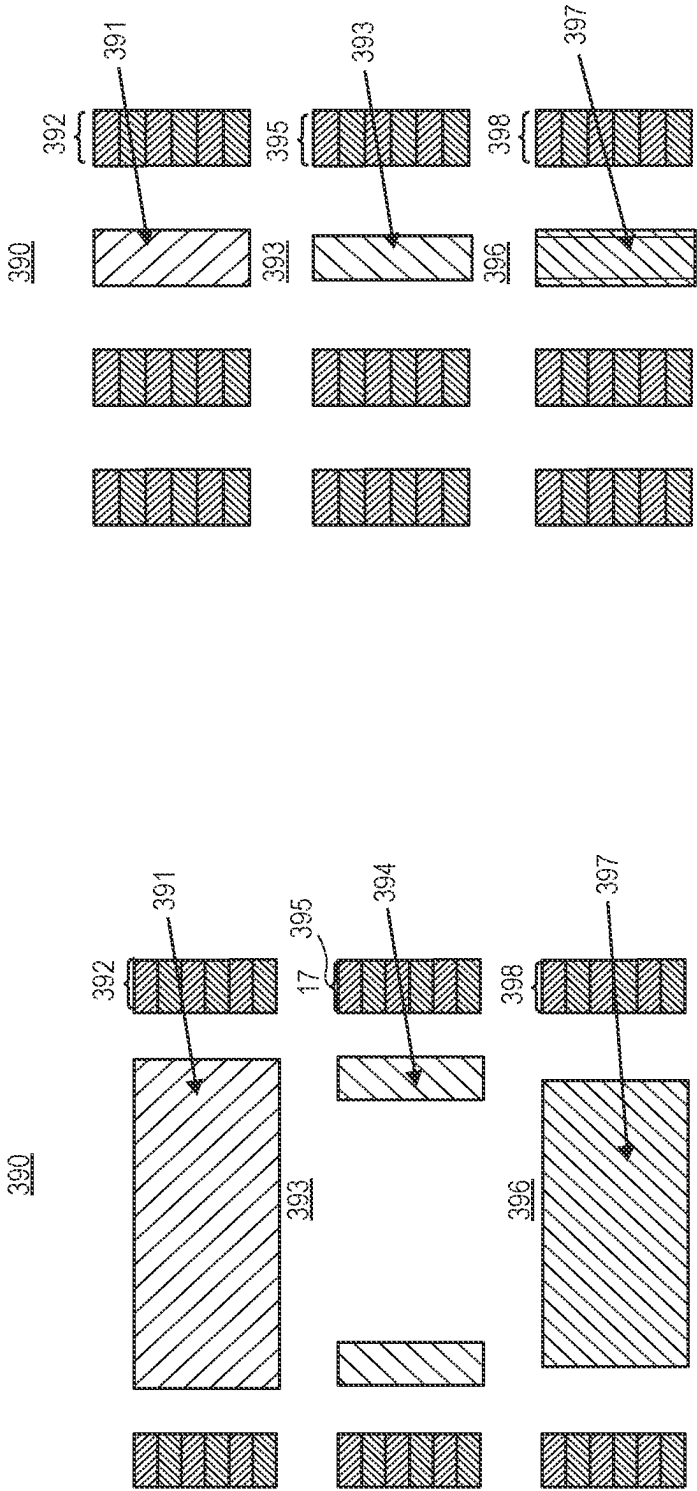


FIG. 31

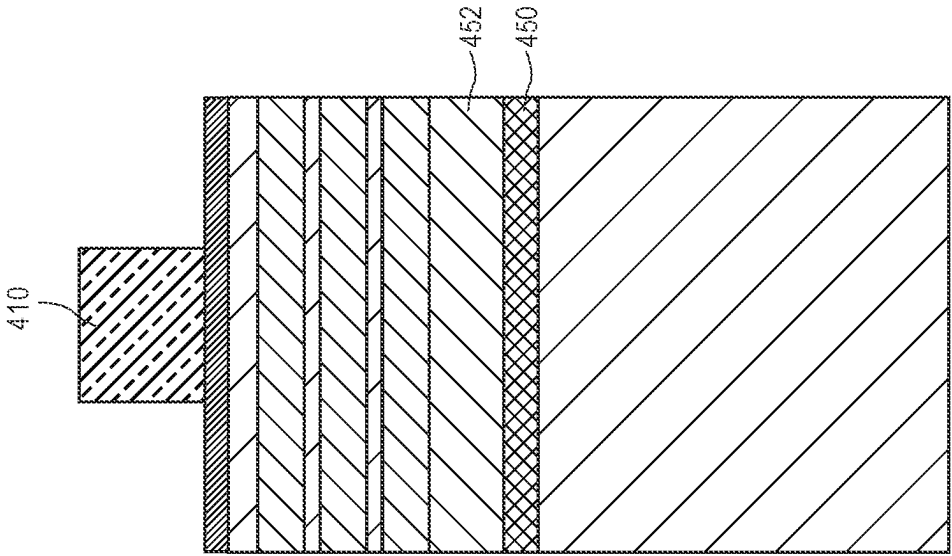


FIG. 4B

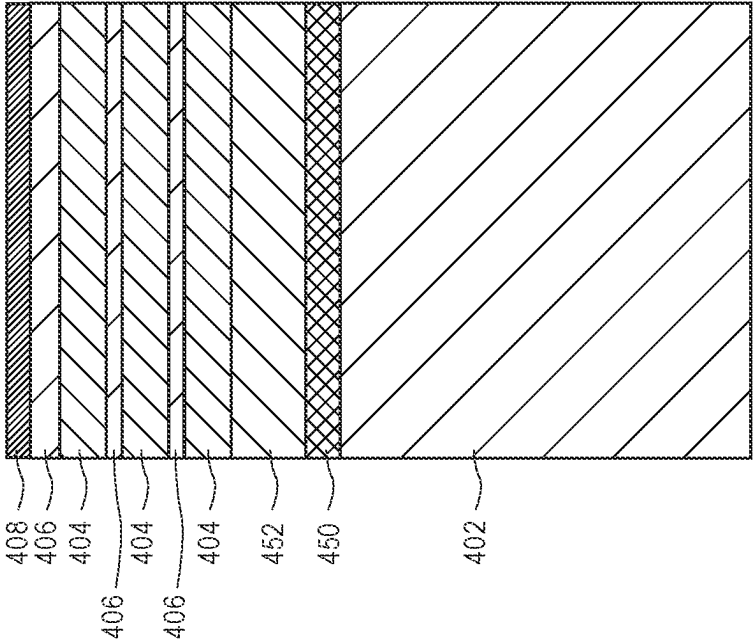
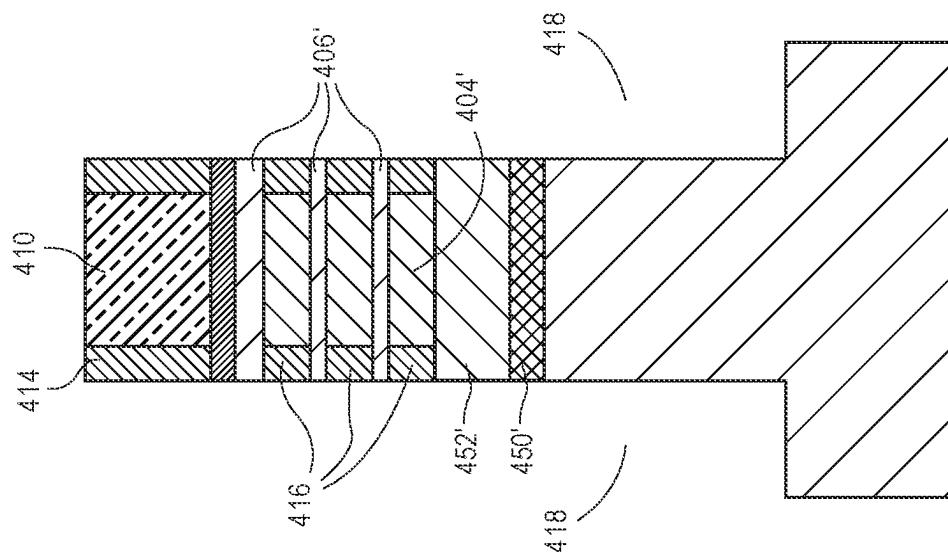


FIG. 4A



4. **Geometric**

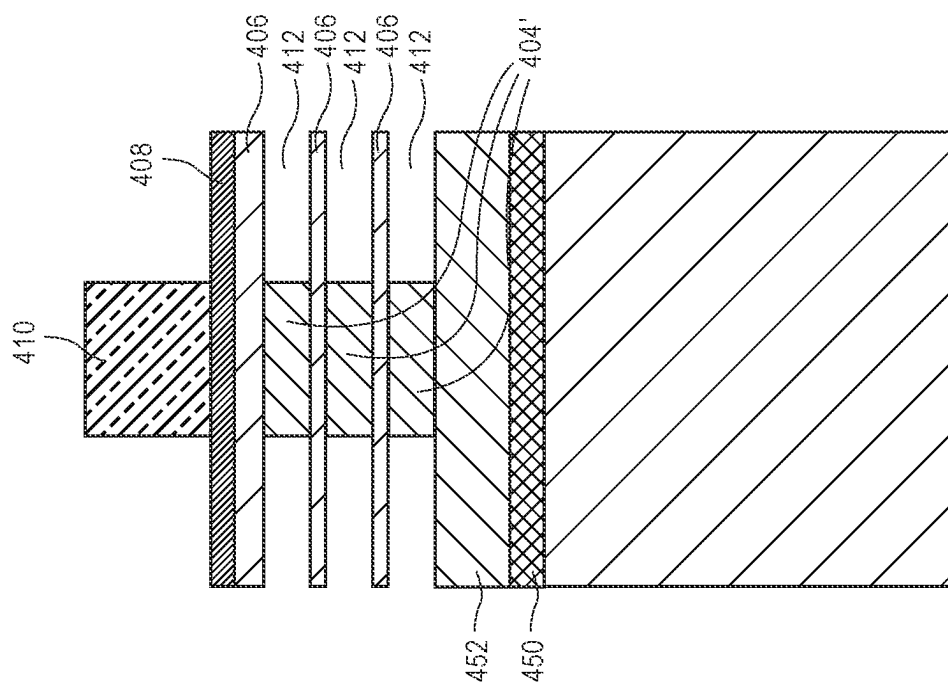


FIG. 4C

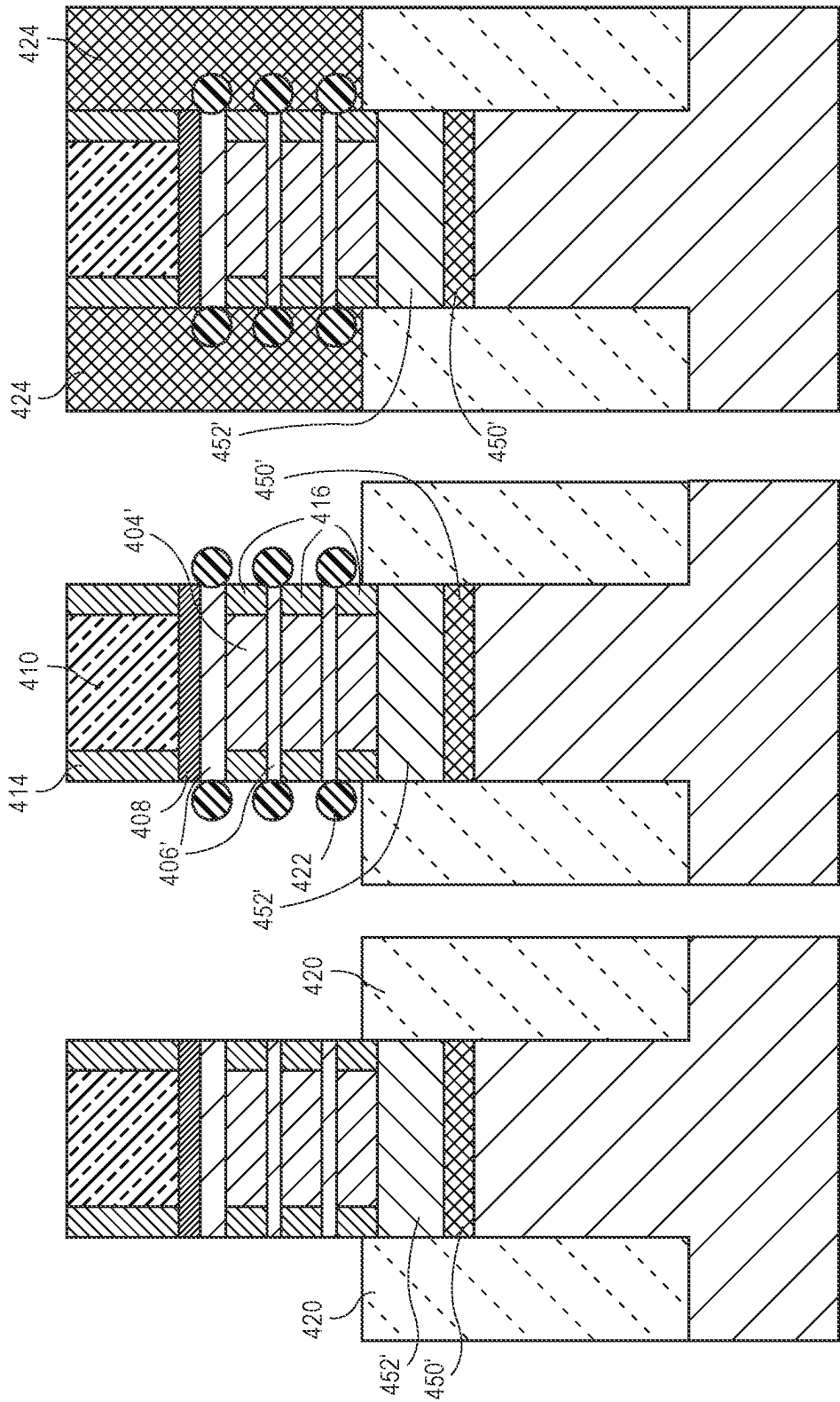


FIG. 4E

FIG. 4F

FIG. 4G

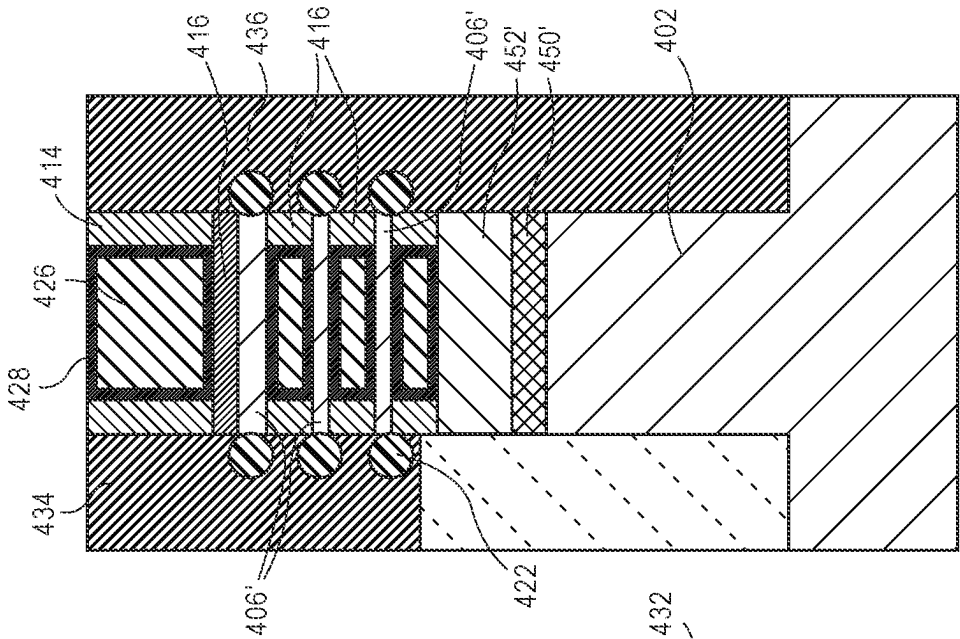


FIG. 4J

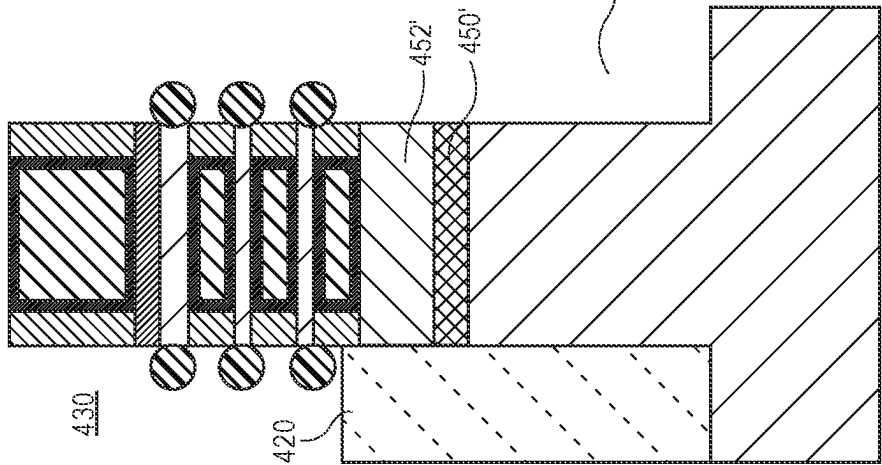


FIG. 4I

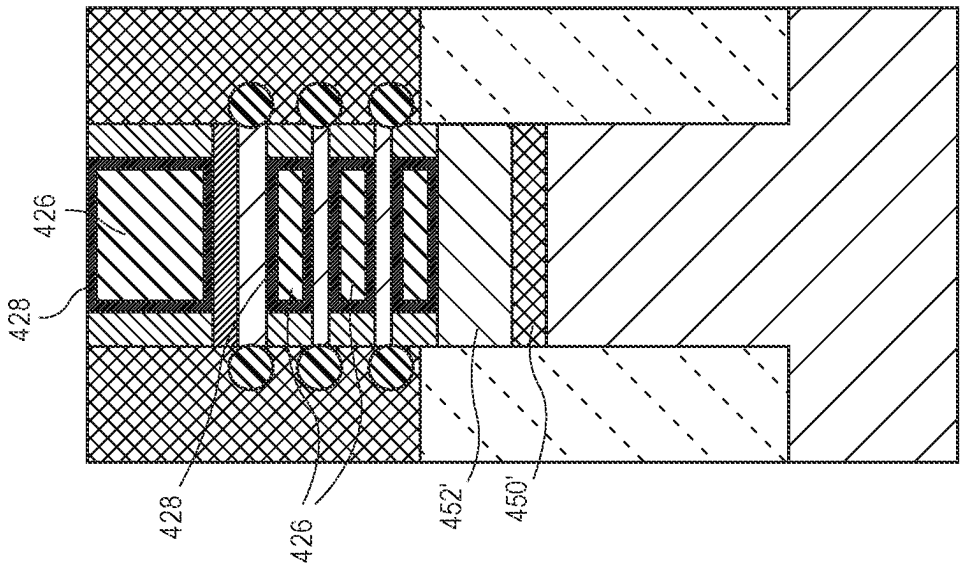


FIG. 4H

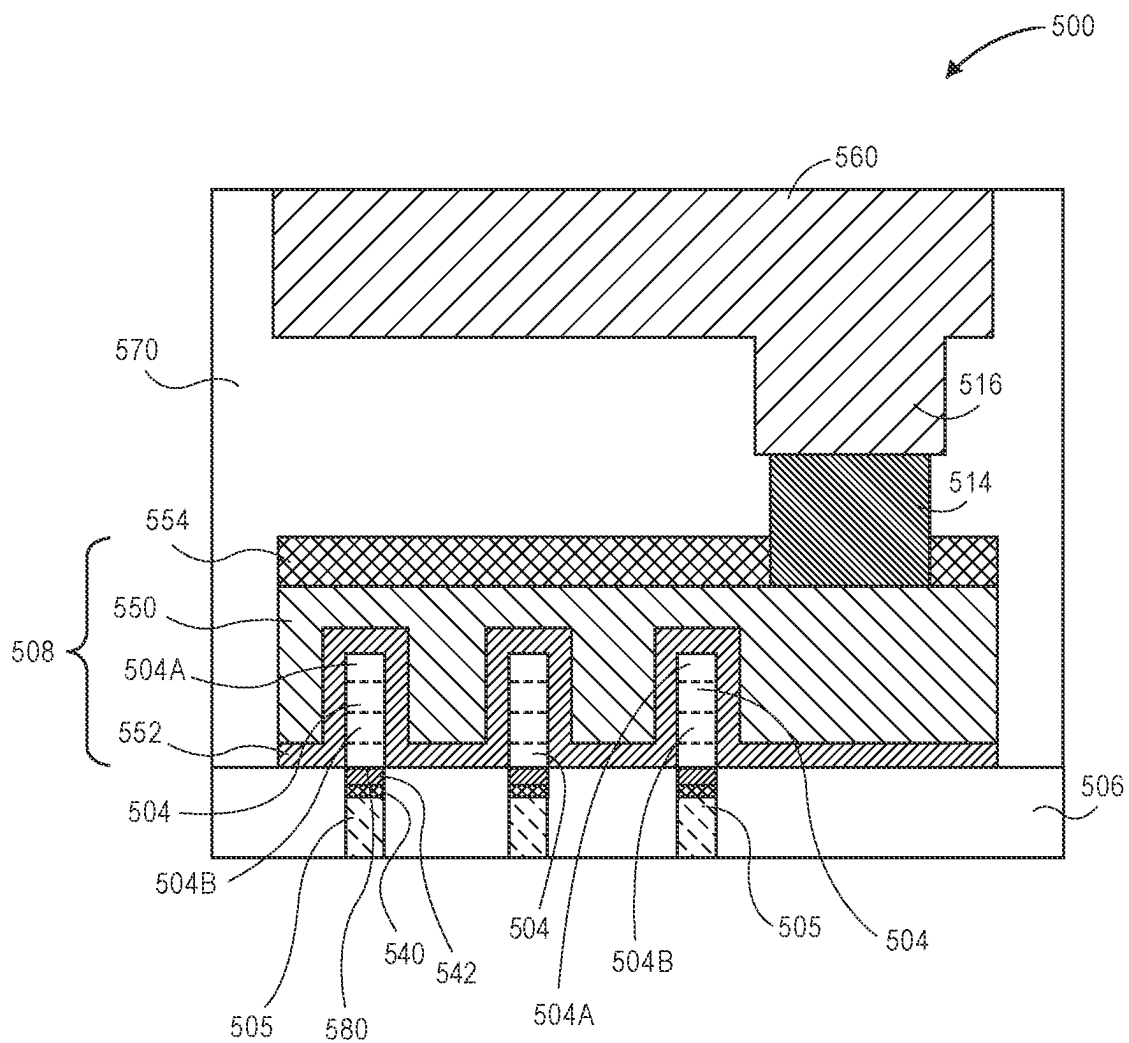


FIG. 5



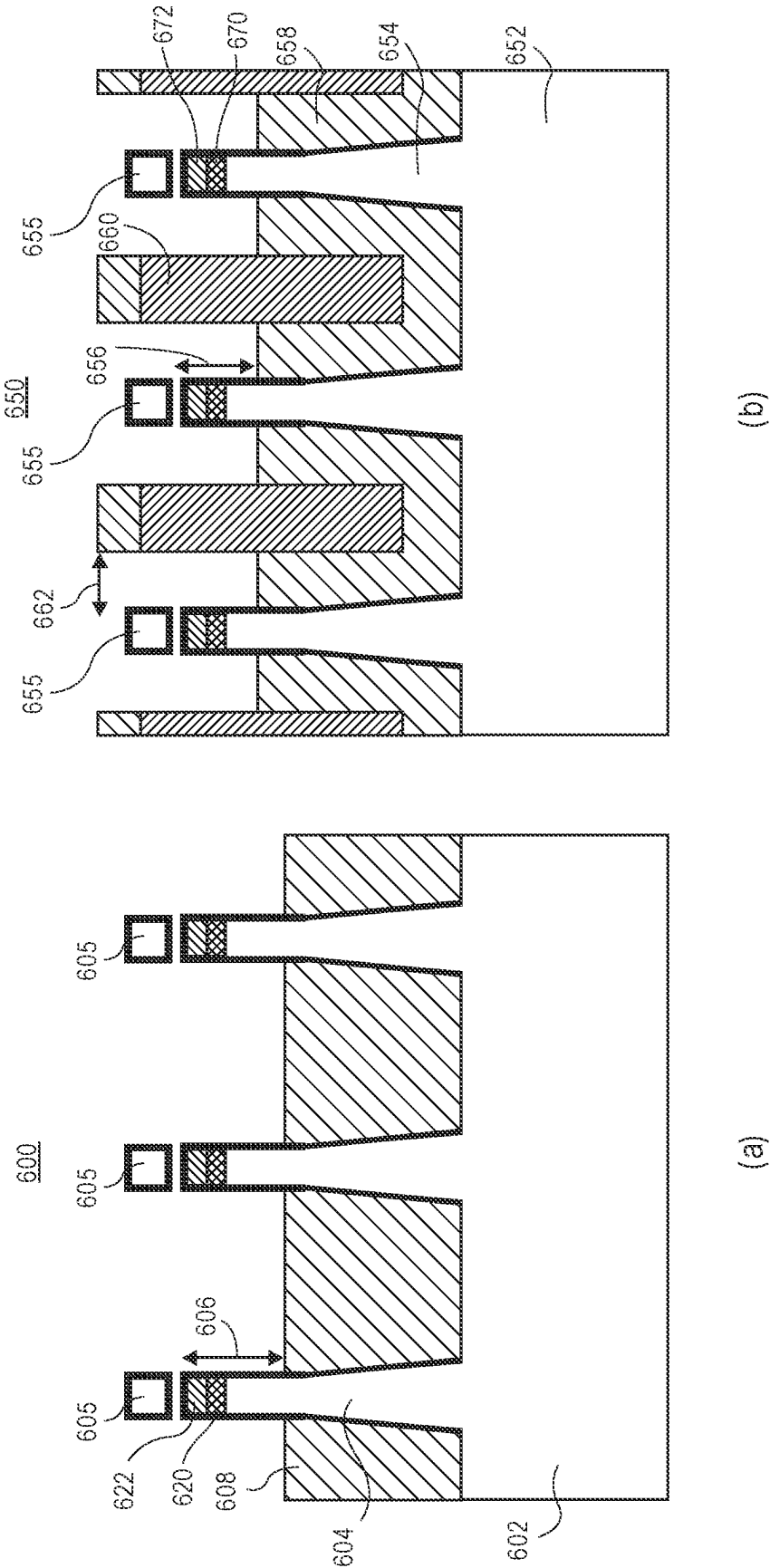
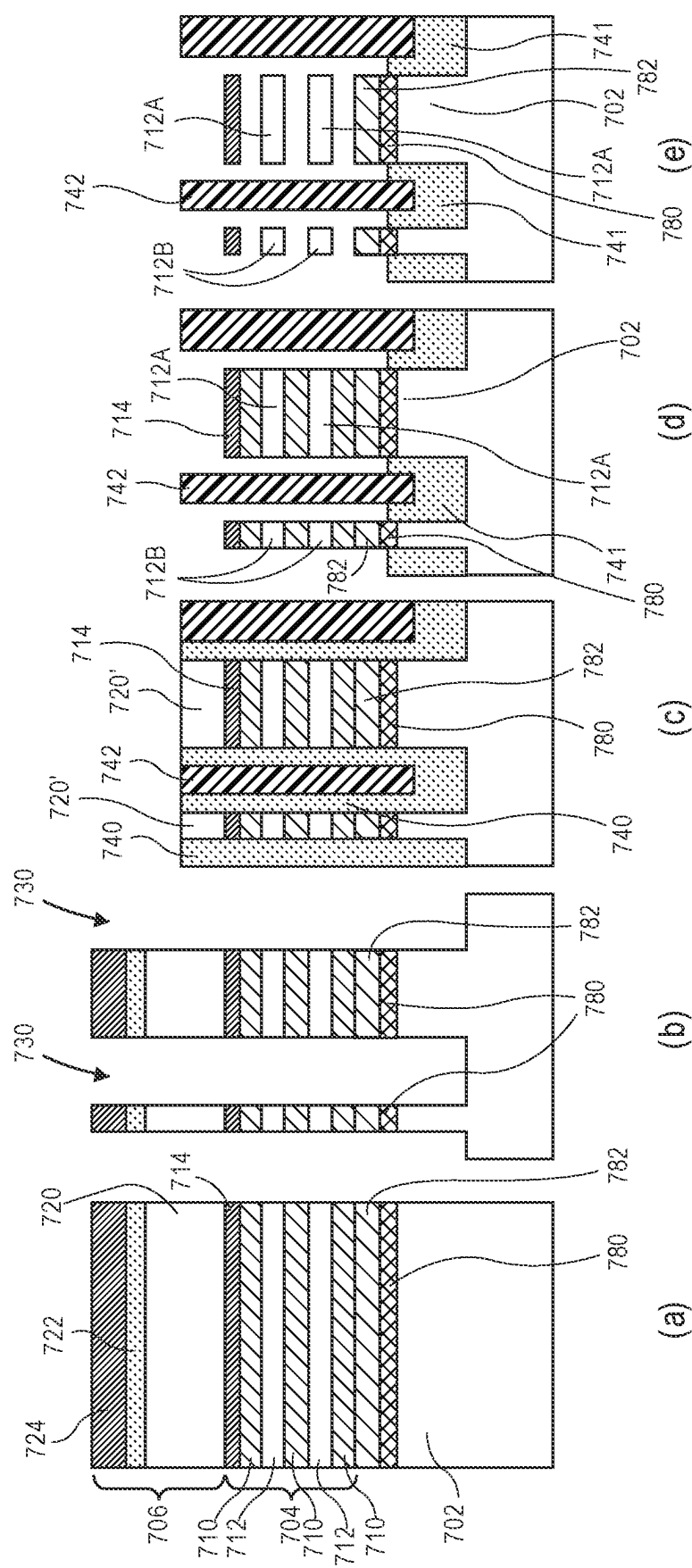


FIG. 6



100

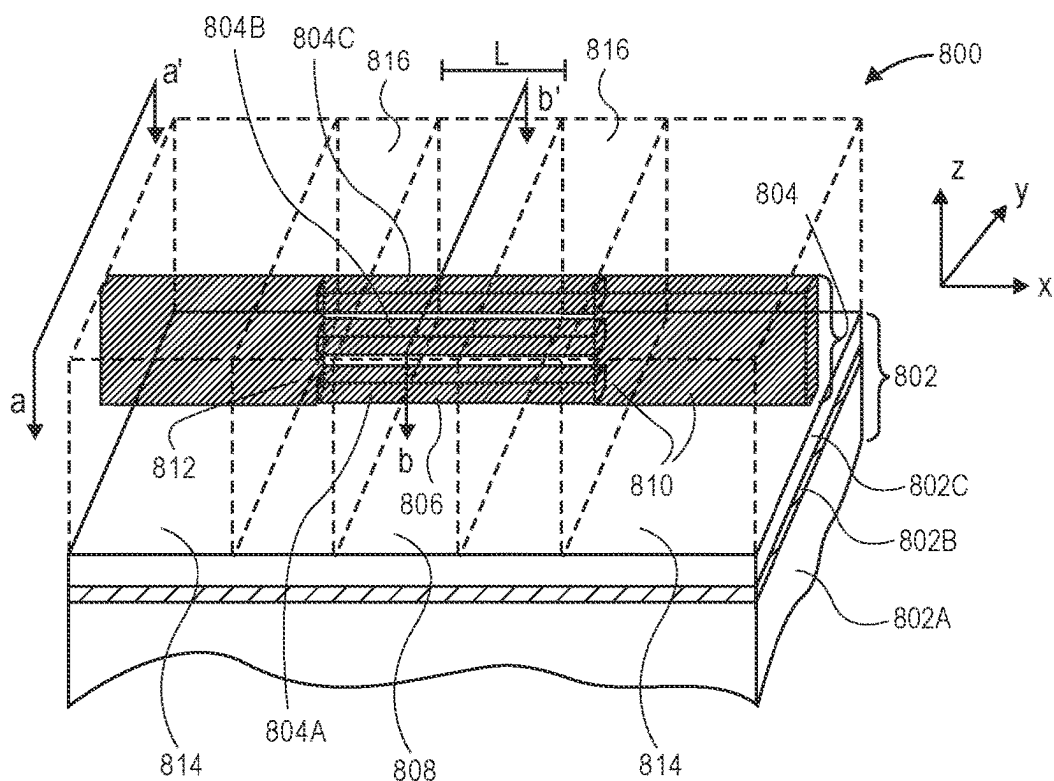


FIG. 8A

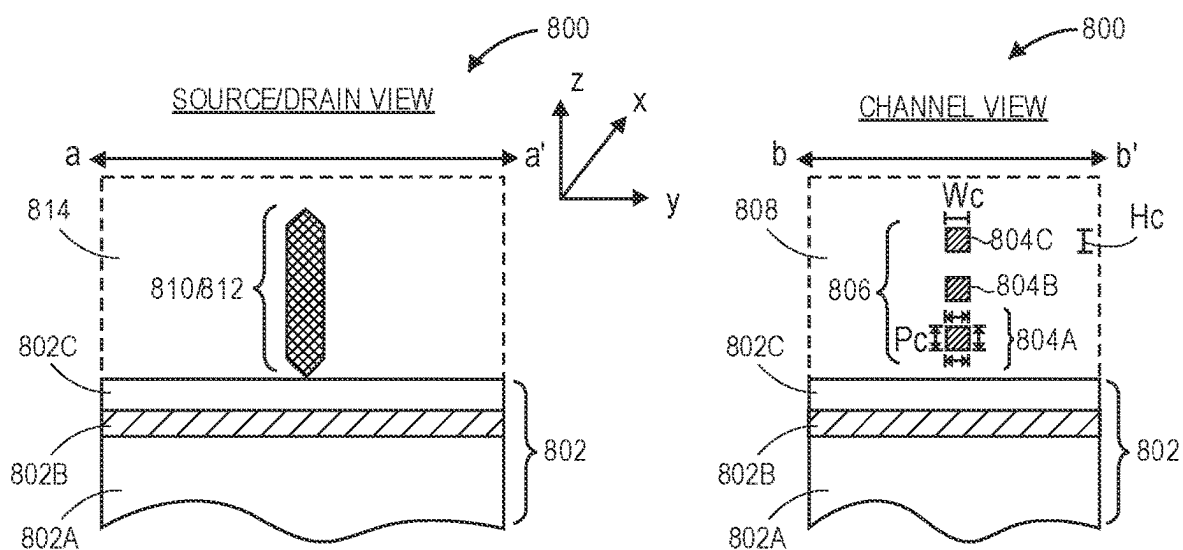
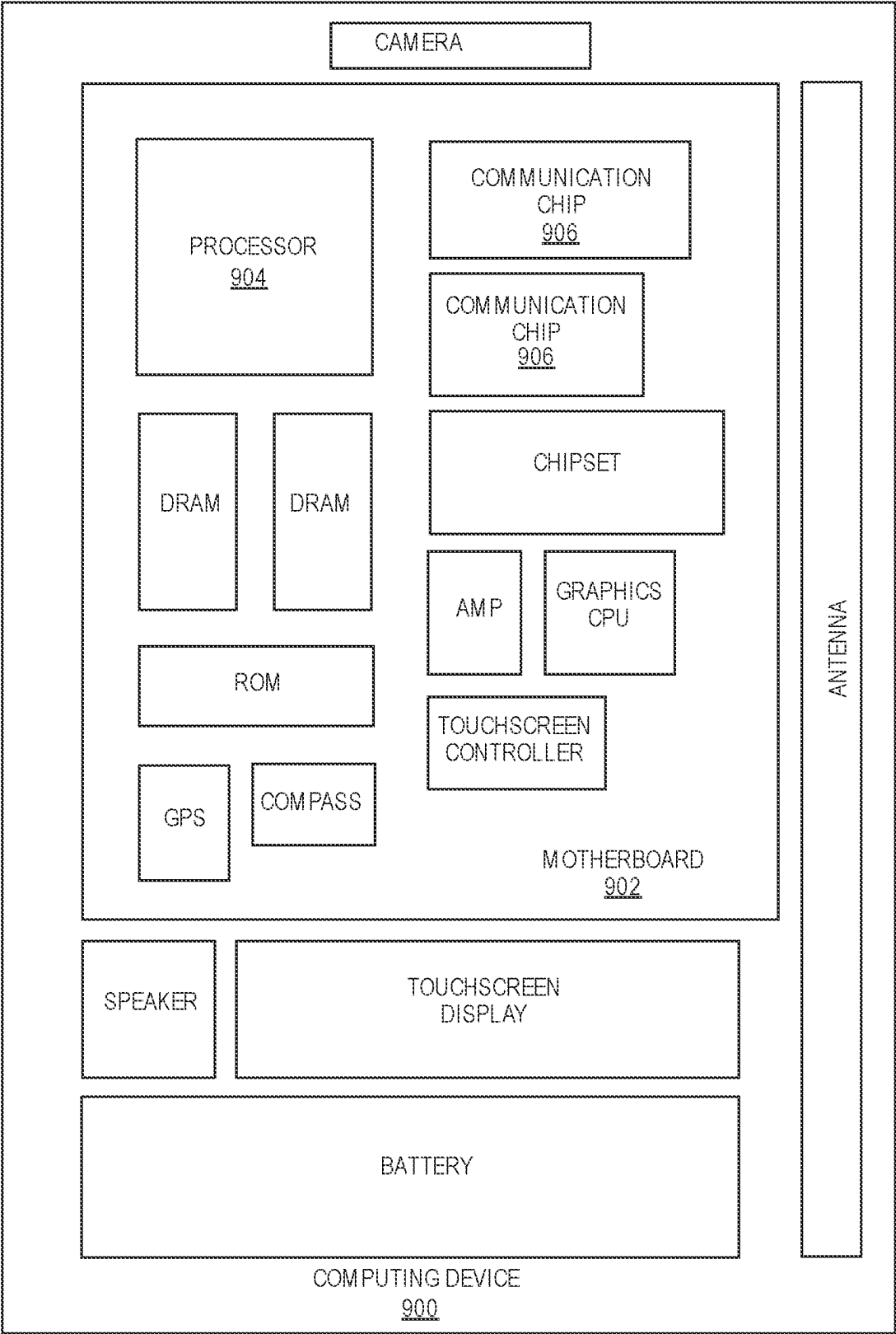


FIG. 8B

FIG. 8C



**FIG. 9**

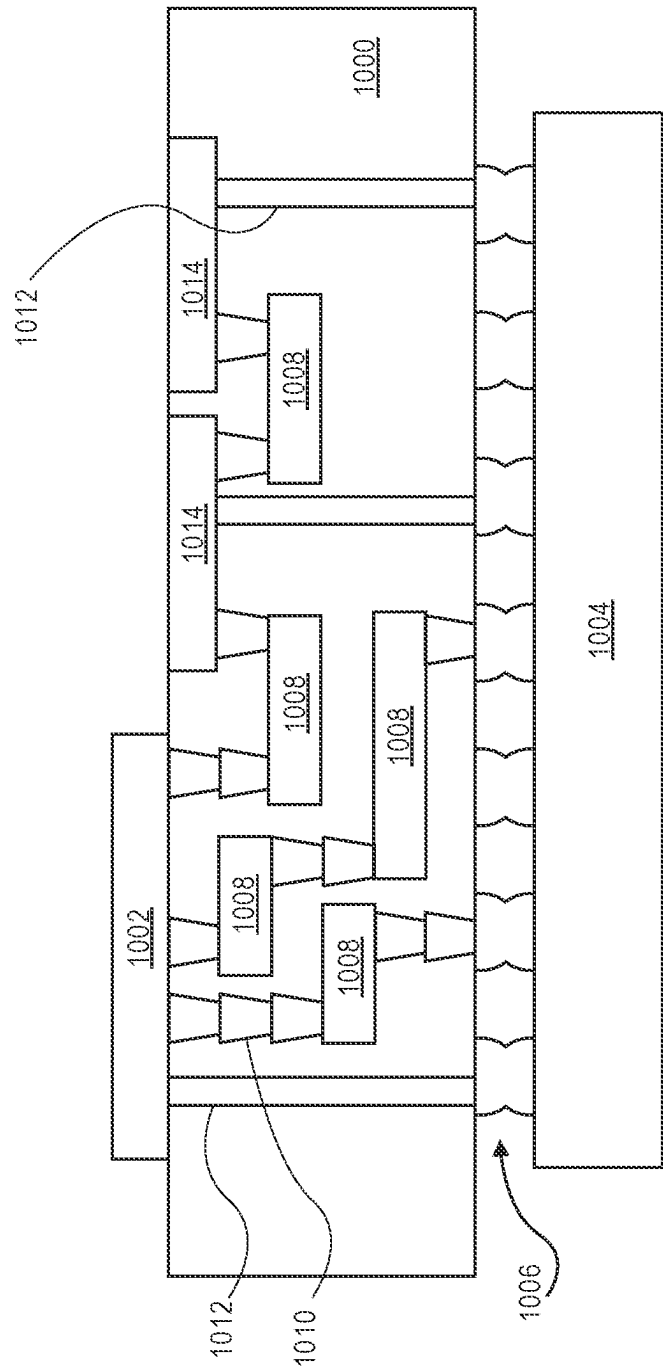


FIG. 10

# **INTEGRATED CIRCUIT STRUCTURES HAVING PRE-SPACER DEPOSITION CUT GATES AND ASSOCIATED DEFECT TEST STRUCTURES**

## **BACKGROUND**

[0001] For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips. For example, shrinking transistor size allows for the incorporation of an increased number of memory or logic devices on a chip, lending to the fabrication of products with increased capacity. The drive for ever-more capacity, however, is not without issue. The necessity to optimize the performance of each device becomes increasingly significant.

[0002] In the manufacture of integrated circuit devices, multi-gate transistors, such as tri-gate transistors, have become more prevalent as device dimensions continue to scale down. In conventional processes, tri-gate transistors are generally fabricated on either bulk silicon substrates or silicon-on-insulator substrates. In some instances, bulk silicon substrates are preferred due to their lower cost and because they enable a less complicated tri-gate fabrication process. In another aspect, maintaining mobility improvement and short channel control as microelectronic device dimensions scale below the 10 nanometer (nm) node provides a challenge in device fabrication. Nanowires used to fabricate devices provide improved short channel control.

[0003] Scaling multi-gate and nanowire transistors has not been without consequence, however. As the dimensions of these fundamental building blocks of microelectronic circuitry are reduced and as the sheer number of fundamental building blocks fabricated in a given region is increased, the constraints on the lithographic processes used to pattern these building blocks have become overwhelming. In particular, there may be a trade-off between the smallest dimension of a feature patterned in a semiconductor stack (the critical dimension) and the spacing between such features.

## **BRIEF DESCRIPTION OF THE DRAWINGS**

[0004] FIG. 1A illustrates cross-sectional views of various operations in a method of fabricating a gate-all-around integrated circuit structure using a pre-spacer-deposition cut gate approach, in accordance with an embodiment of the present disclosure.

[0005] FIG. 1B illustrates cross-sectional views of various operations in a method of fabricating a gate-all-around integrated circuit structure using a pre-spacer-deposition cut gate approach, in accordance with an embodiment of the present disclosure.

[0006] FIG. 1C is a schematic of a layout for detection of trench contact opens, in accordance with an embodiment of the present disclosure.

[0007] FIG. 1D is a schematic of a layout for detection of trench contact shorts, in accordance with an embodiment of the present disclosure.

[0008] FIG. 1E illustrates bright portions of a structure under voltage contrast testing, in accordance with an embodiment of the present disclosure.

[0009] FIGS. 2A-2G illustrate cross-sectional views of various operations in a method of fabricating a gate-all-around integrated circuit structure using a pre-spacer-deposition cut gate approach, in accordance with an embodiment of the present disclosure.

[0010] FIGS. 3A and 3B illustrate plan views representing various operations in a method of patterning of fins with multi-gate spacing for forming a local isolation structure.

[0011] FIGS. 3C-3F illustrate plan views representing various operations in a method of patterning of fins with single gate spacing for forming a local isolation structure, in accordance with another embodiment of the present disclosure.

[0012] FIGS. 3G and 3H illustrate plan views representing various operations in a method of patterning of fins with single gate spacing for forming a local isolation structure in select gate line cut locations, in accordance with an embodiment of the present disclosure.

[0013] FIG. 3I illustrates exemplary mask splitting schematics for a method of fabricating a gate-all-around integrated circuit structure using a pre-spacer-deposition cut gate approach, in accordance with an embodiment of the present disclosure.

[0014] FIGS. 4A-4J illustrates cross-sectional views of various operations in a method of fabricating a gate-all-around integrated circuit structure, in accordance with an embodiment of the present disclosure.

[0015] FIG. 5 illustrates a cross-sectional view of a non-planar integrated circuit structure as taken along a gate line, in accordance with an embodiment of the present disclosure.

[0016] FIG. 6 illustrates cross-sectional views taken through nanowires and fins for a non-endcap architecture (left-hand side (a)) versus a self-aligned gate endcap (SAGE) architecture (right-hand side (b)), in accordance with an embodiment of the present disclosure.

[0017] FIG. 7 illustrates cross-sectional views representing various operations in a method of fabricating a self-aligned gate endcap (SAGE) structure with gate-all-around devices, in accordance with an embodiment of the present disclosure.

[0018] FIG. 8A illustrates a three-dimensional cross-sectional view of a nanowire-based integrated circuit structure, in accordance with an embodiment of the present disclosure.

[0019] FIG. 8B illustrates a cross-sectional source or drain view of the nanowire-based integrated circuit structure of FIG. 8A, as taken along the a-a' axis, in accordance with an embodiment of the present disclosure.

[0020] FIG. 8C illustrates a cross-sectional channel view of the nanowire-based integrated circuit structure of FIG. 8A, as taken along the b-b' axis, in accordance with an embodiment of the present disclosure.

[0021] FIG. 9 illustrates a computing device in accordance with one implementation of an embodiment of the disclosure.

[0022] FIG. 10 illustrates an interposer that includes one or more embodiments of the disclosure.

## **DESCRIPTION OF THE EMBODIMENTS**

[0023] Integrated circuit structures having pre-spacer-deposition cut gates and associated defect test structures are described. In the following description, numerous specific details are set forth, such as specific integration and material regimes, in order to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to

one skilled in the art that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known features, such as integrated circuit design layouts, are not described in detail in order to not unnecessarily obscure embodiments of the present disclosure. Furthermore, it is to be appreciated that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

**[0024]** Certain terminology may also be used in the following description for the purpose of reference only, and thus are not intended to be limiting. For example, terms such as “upper”, “lower”, “above”, and “below” refer to directions in the drawings to which reference is made. Terms such as “front”, “back”, “rear”, and “side” describe the orientation and/or location of portions of the component within a consistent but arbitrary frame of reference which is made clear by reference to the text and the associated drawings describing the component under discussion. Such terminology may include the words specifically mentioned above, derivatives thereof, and words of similar import.

**[0025]** Embodiments described herein may be directed to front-end-of-line (FEOL) semiconductor processing and structures. FEOL is the first portion of integrated circuit (IC) fabrication where the individual devices (e.g., transistors, capacitors, resistors, etc.) are patterned in the semiconductor substrate or layer. FEOL generally covers everything up to (but not including) the deposition of metal interconnect layers. Following the last FEOL operation, the result is typically a wafer with isolated transistors (e.g., without any wires).

**[0026]** Embodiments described herein may be directed to back-end-of-line (BEOL) semiconductor processing and structures. BEOL is the second portion of IC fabrication where the individual devices (e.g., transistors, capacitors, resistors, etc.) are interconnected with wiring on the wafer, e.g., the metallization layer or layers. BEOL includes contacts, insulating layers (dielectrics), metal levels, and bonding sites for chip-to-package connections. In the BEOL part of the fabrication stage contacts (pads), interconnect wires, vias and dielectric structures are formed. For modern IC processes, more than 10 metal layers may be added in the BEOL.

**[0027]** Embodiments described below may be applicable to FEOL processing and structures, BEOL processing and structures, or both FEOL and BEOL processing and structures. In particular, although an exemplary processing scheme may be illustrated using a FEOL processing scenario, such approaches may also be applicable to BEOL processing. Likewise, although an exemplary processing scheme may be illustrated using a BEOL processing scenario, such approaches may also be applicable to FEOL processing.

**[0028]** One or more embodiments described herein are directed to gate-all-around devices fabricated using a poly (gate) cut implemented prior to gate spacer deposition, e.g., for gates overlying stacks of nanowires. It is to be appreciated that, unless indicated otherwise, reference to nanowires can indicate nanowires or nanoribbons or nanosheets. One or more embodiments described herein are directed to FinFET devices fabricated using a poly (gate) cut implemented prior to gate spacer deposition, e.g., for gates overlying fins. One or more embodiments are directed to the design of voltage contrast (VC) structures and a methodology to detect trench contact (TCN) STS shorts.

**[0029]** To provide context, it can be difficult to create a very narrow poly (gate) cut (PCT) at a later stage of a process flow, e.g., a stage subsequent to gate spacer deposition. Narrow and wide PCTs may need to be split and performed at separate operations in a process flow. Also, it is proving much easier to disconnect two gates with a narrow poly cut (PCT) than other approaches explored.

**[0030]** In accordance with one or more embodiments of the present disclosure, addressing issues outlined above, approaches are described for implementing a narrow PCT cut that takes place after hardmask (HM) patterning or immediately after poly (PLY) etch, e.g., immediately after the etch used to pattern gate lines such as dummy polysilicon gate lines ultimately used in a replacement gate process. In one embodiment, after spacer deposition a PCT end-to-end (ETE) is bridged using a spacer deposition operation, e.g., a gate spacer deposition. The approach may simplify the process flow and enable PCT for very small PCT cuts. In an embodiment, a narrow PCT is patterned during PLY etch, allowing for large scaling where very small PCT critical dimension (CD) can be achieved; wide PCT plugs can still be patterned at the same time as a subsequent fin trim isolation (FTI) or through fin isolation approach.

**[0031]** Advantages for implementing approaches described herein include that it may be more cost effective to add PCT pre-spacer etch and then run a standard process flow. Isotropic Si removal can be used such that there is no remaining Si in the gates since the process is independent of the PLY profile. Also, there may be no gate height loss through the narrow poly cut process.

**[0032]** In accordance with one or more embodiments of the present disclosure, a PCT mask split is into all narrow cuts, and then all wider PCT cuts go to the FTI mask. As an example, FIG. 1A illustrates cross-sectional views of various operations in a method of fabricating a gate-all-around integrated circuit structure using a pre-spacer-deposition cut gate approach, in accordance with an embodiment of the present disclosure. FIG. 1B illustrates cross-sectional views of various operations in a method of fabricating a gate-all-around integrated circuit structure using a pre-spacer-deposition cut gate approach, in accordance with an embodiment of the present disclosure. It is to be appreciated that although described in association with stacks of nanowires (or nanoribbons or nanosheets), semiconductor fins can also be covered by the embodiments, e.g., where a semiconductor fin would replace a stack of nanowires. It is also to be appreciated that the resulting structures can be fabricated together with associated defect test structures such as described below in association with FIGS. 1C-1E.

**[0033]** Referring to part (i) of FIG. 1A, a starting structure **100** includes a first fin **104A** including a plurality of horizontal nanowires **108** (which can be nanoribbons) and a second fin **104B** including a plurality of horizontal nanowires **108** (which can be nanoribbons) above a substrate **102**. The first fin **104A** and the second fin **104B** may be over respective cavities **111** over respective sub-fin portions of the substrate **102**, where the sub-fin portions are separated by shallow trench isolation (STI) structures. The first fin **104A** and the second fin **104B** may each include intervening sacrificial material **110** between the plurality of horizontal nanowires **108**. Gate lines **112**, such as sacrificial polysilicon gate lines, are over the first fin **104A** and the second fin **104B**. The gate lines **112** may include a hardmask **114** thereon, as is depicted. A narrow poly cut **116** is formed as

a trench in one of the gate lines **112** between the first fin **104A** and the second fin **104B**. Referring to part (ii) of FIG. **1A**, a structure **120** includes a spacer material formed over the starting structure **100**. The spacer material includes first and second portions **122A** over and along sidewalls of the gate lines **112**, and a third portion **122B** in the narrow poly cut **116**, the third portion continuous with the first and second portions. It is to be appreciated that subsequent spacer material etching can be implemented to leave the portion **122A** remaining only along the sidewalls of the gate lines **112**, while retaining the second portion **122B** in the narrow poly cut **116**. The second portion **122B** in the narrow poly cut **116** may be referred to as a narrow gate plug or a narrow poly cut plug.

**[0034]** Referring to part (i) of FIG. **1B**, a structure **150** shows the structure **120** of FIG. **1A** following processing that provided trench contacts or dummy trench contact structures **156** between gate lines **112**. A patterned mask **152** is formed over the structure and a wide poly cut **154** is formed as a trench in one of the gate lines **112**. In one embodiment, the wide poly cut **154** is formed in the same gate line **112** and is adjacent to the narrow gate plug or narrow poly cut plug **122B**. Referring to part (ii) of FIG. **1B**, a structure **160** is formed by depositing a dielectric material over the structure **150** to form a wide gate plug or wide poly cut plug **162**. In one embodiment, the wide gate plug or wide poly cut plug **162** is in contact with the narrow gate plug or narrow poly cut plug **122B**, as is depicted.

**[0035]** In another aspect, the design of voltage contrast (VC) structures and a methodology to detect trench contact (TCN) STS shorts is described.

**[0036]** To provide context, the self-sealing poly cut (PCT) architecture where PCT (poly cut or gate plug) is patterned before poly etch and plugged naturally by the gate dielectric spacer deposition leaves itself open to trench contact (TCN) STS short defects (through the seam in the orthogonal gate direction (OGD) where the spacer merges). Detection of these shorts inline can be extremely difficult from traditional means and hence process development can be slowed and gated by data turns.

**[0037]** In previous approaches, successful inline detection of such fails which are buried or thin defects post contact metallization has been poor. Processes have had to rely on end of line signals for such buried defects. Some destructive Quick turn monitors (QTMs) have been developed that try to etch the plug through post contact metallization to determine if there is a metal layer that prevents the etch. However, such QTMs can be unreliable as they are hard to engineer and are destructive and hence need duplicate wafer silicon funding and no correlations can be established to sort.

**[0038]** In accordance with an embodiment of the present disclosure, voltage contrast (VC) is used to determine if the contact metal from one TCN is shorting to another TCN in the OGD direction through a gate plug (PCT) which in turn is grounded to the substrate. Under the right electrical field, a grounded contact (e.g., a conductive trench contact coupled to ground) will appear bright under VC post metallization. A contact that is floating or on isolation (e.g., an electrically isolated conductive trench contact) will appear dark/gray. Dense arrays of floating TCNs (TCNs on isolation) that are next to TCNs that land on diffusion (grounded TCNs) and have a shorting that with a PCT between them allows isolation and test of massive areas to identify this fail.

**[0039]** Advantages for implementing embodiments described herein can include inline detection to a difficult problem reduce time to yield learning time by not having to run potential skews for solutions to end of line. The VC test is also non-destructive and can be run on production wafers that can go to end of line, thereby minimizing cost and also by establishing correlations to known yield signals at end of line.

**[0040]** Detectability of embodiments described herein can include the observation of VC structures that are large arrays spanning several 10s/100s of microns with a periodic arrangement of alternating floating (dummy TCNs on isolation) and grounded (TCNs on p-diff/pTAP) TCNs in parallel gate direction (PGD) with one or more PCT plugs between them. In one embodiment, the gates and TCNs are dummy and do not connect up to routing metal layers or power rails. In one embodiment, a contact via lands on each floating TCN segment to enable detection post via formation. In one embodiment, such structures can be detected by reverse engineering by polishing down to the via and front end stack and observing a planar TEM image.

**[0041]** To provide further context, in voltage contrast mode, E-Beam tools can distinguish between grounded and floating features. Grounded features appear bright whereas floated appear darker under the right polarity. This helps design custom structures which can be used to detect electrical opens/shorts. This technique can be especially useful in detecting defects that are buried or hidden and are not otherwise accessible for detection through optical metrology. Specifically for TCN STS shorts, a dense array of structures is designed to have a floating TCN immediately adjacent to a grounded TCN in PGD and separated by a PCT (gate plug) between them. The process corners are stressed by using the max CD of the PCT plug. In one embodiment, only one PCT is used for each floating TCN/grounded TCN pair. This can allow quicker fault isolation as the exact PCT plug fail location leading to the TCN STS defect is isolated. The scheme can be replicated over large arrays. The gates can be floating and not connected up to ViaG. In one embodiment, there is a ViaT that lands on each individual floating/dummy TCN segment that allows detection of these shorts at either contact layers or via layers.

**[0042]** As an example, FIG. **1C** is a schematic of a layout for detection of trench contact opens, in accordance with an embodiment of the present disclosure.

**[0043]** Referring to FIG. **1C**, a layout **170** includes gate lines **171**, P-diffusion **172**, N-diffusion **173**, an isolated trench contact **174A**, trench contacts **174B**, and poly cut locations **175** (which can also be fin trim isolation locations). In one embodiment, the center trench contact (TCN) **174A** is on isolation flanked by poly cut (PCT) plugs on either side and is the TCN under test.

**[0044]** As an example, FIG. **1D** is a schematic of a layout for detection of trench contact shorts, in accordance with an embodiment of the present disclosure.

**[0045]** Referring to FIG. **1D**, a layout **180** includes N-diffusion structures **182** (such as NMOS fins or stacks of nanowires), P-diffusion/P-tap structures **184** (such as PMOS fins or stacks of nanowires), gate/poly lines **186** with poly cut (PCT) locations **187** there between, trench contact **188**, and trench contact vias **190**. A shorting path **189** is shown in locations through the PCT locations **187** which, in an embodiment, is a defect.



[0046] As an example, FIG. 1E illustrates bright portions of a structure under voltage contrast testing, in accordance with an embodiment of the present disclosure.

[0047] Referring to FIG. 1E, a structure 195 shows portions of an array of alternating trench contact structures and gate lines that are made to appear “bright” using a voltage contrast measurement. The section 197 highlights a location where trench contacts are shorted through a poly cut (PCT) location. Open locations in FIG. 1E are regions of the array that remain “dark” during the voltage contrast measurement. In one embodiment, the bright locations are portions of the array that are electrically “floating.”

[0048] In another aspect, as an exemplary process flow, FIGS. 2A-2G illustrate cross-sectional views of various operations in a method of fabricating a gate-all-around integrated circuit structure using a pre-spacer-deposition cut gate approach, in accordance with an embodiment of the present disclosure. At each operation, a source/drain tilt (S/D tilt) view, a gate tilt view, and a through fin trim isolation fin (thru FTI fin) view is provided. It is to be appreciated that although described in association with stacks of nanowires (or nanoribbons or nanosheets), semiconductor fins can also be covered by the embodiments, e.g., where a semiconductor fin would replace a stack of nanowires. It is also to be appreciated that the resulting structures can be fabricated together with associated defect test structures such as described above in association with FIGS. 1C-1E.

[0049] Referring to FIG. 2A, a starting structure 200 includes a first fin 204A including a plurality of horizontal nanowires 208 (which can be nanoribbons) and a second fin 204B including a plurality of horizontal nanowires 208 (which can be nanoribbons) above a substrate 202. The first fin 204A and the second fin 204B may be over respective cavities 211 over respective sub-fin portions of the substrate 202, where the sub-fin portions are separated by shallow trench isolation (STI) structures. The first fin 204A and the second fin 204B may each include intervening sacrificial material 210 between the plurality of horizontal nanowires 208. Gate lines 212, such as sacrificial polysilicon gate lines, are over the first fin 204A and the second fin 204B. The gate lines 212 may include a hardmask 214 thereon, as is depicted. A narrow poly cut 216 is formed as a trench in one of the gate lines 212 between the first fin 204A and the second fin 204B.

[0050] Referring to FIG. 2B, a spacer material is formed over the starting structure 200. The spacer material 218 includes a portion 218A over and along sidewalls of the gate lines 212, and a second portion 218B in the narrow poly cut 216.

[0051] Referring to FIG. 2C, a helmet layer 220 is formed over the structure of FIG. 2B. Spacer material etching is then implemented to leave a portion 218A' of portion 218A remaining only along the sidewalls of the gate lines 212, while retaining the second portion 218B in the narrow poly cut 216. The second portion 218B in the narrow poly cut 216 may be referred to as a narrow gate plug or a narrow poly cut plug, as depicted in FIG. 2D.

[0052] Referring FIG. 2E, epitaxial source or drain structure 223 are formed, trench contacts or dummy trench contact structures 222 are formed between gate lines 212, and a planarization operation is performed to expose the hardmask 214 and the narrow gate plug or narrow poly cut plug 218B. It is to be appreciated that poly cut processing may be complete at this stage. In such a case, subsequent

processing can next involve replacement gate and nanowire release processing. Alternatively, later, wider cuts may be formed. In such an example, a first patterned mask 224 and a second patterned mask 226 are then formed over the structure of FIG. 2E, as is depicted in FIG. 2F.

[0053] Referring to FIG. 2G, a wide poly cut is formed as a trench in one of the gate lines 212 (e.g., as described above in association with FIG. 1B), and a dielectric material is deposited to form a wide gate plug or wide poly cut plug 228, and then planarization and mask removal is performed. In one embodiment, the wide gate plug or wide poly cut plug 228 is in contact with the narrow gate plug or narrow poly cut plug 218B, as is depicted. It is to be appreciated that subsequent processing can next involve replacement gate and nanowire release processing.

[0054] With reference again to FIG. 2E, in accordance with an embodiment of the present disclosure, an integrated circuit structure includes a first vertical arrangement of horizontal nanowires and a second vertical arrangement of horizontal nanowires. A first gate stack is over the first vertical arrangement of horizontal nanowires, and a second gate stack is over the second vertical arrangement of horizontal nanowires. An end of the second gate stack is spaced apart from an end of the first gate stack by a gap. The integrated circuit structure also includes a dielectric structure having a first portion forming a gate spacer along sidewalls of the first gate stack, a second portion forming a gate spacer along sidewalls of the second gate stack, and a third portion completely filling the gap, the third portion continuous with the first and second portions.

[0055] With reference again to FIG. 2G, in accordance with an embodiment of the present disclosure, an integrated circuit structure includes a first vertical arrangement of horizontal nanowires and a second vertical arrangement of horizontal nanowires. A gate stack is over the first vertical arrangement of horizontal nanowires, and a gate plug is over the second vertical arrangement of horizontal nanowires. An end of the gate plug is spaced apart from an end of the gate stack by a gap. The integrated circuit structure also includes a dielectric structure having a first portion forming a gate spacer along sidewalls of the gate stack, a second portion forming a spacer along sidewalls of the gate plug, and a third portion completely filling the gap, the third portion continuous with the first and second portions. In one embodiment, a seam is between the third portion of the dielectric structure and the gate plug.

[0056] In another aspect, fin-trim isolation (FTI) and single gate spacing for isolated fins is described. Non-planar transistors which utilize a fin of semiconductor material protruding from a substrate surface employ a gate electrode that wraps around two, three, or even all sides of the fin (i.e., dual-gate, tri-gate, nanowire transistors). Source and drain regions are typically then formed in the fin, or as re-grown portions of the fin, on either side of the gate electrode. To isolate a source or drain region of a first non-planar transistor from a source or drain region of an adjacent second non-planar transistor, a gap or space may be formed between two adjacent fins. Such an isolation gap generally requires a masked etch of some sort. Once isolated, a gate stack is then patterned over the individual fins, again typically with a masked etch of some sort (e.g., a line etch or an opening etch depending on the specific implementation).

[0057] One potential issue with the fin isolation techniques described above is that the gates are not self-aligned

with the ends of the fins, and alignment of the gate stack pattern with the semiconductor fin pattern relies on overlay of these two patterns. As such, lithographic overlay tolerances are added into the dimensioning of the semiconductor fin and the isolation gap with fins needing to be of greater length and isolation gaps larger than they would be otherwise for a given level of transistor functionality. Device architectures and fabrication techniques that reduce such over-dimensioning therefore offer highly advantageous improvements in transistor density.

**[0058]** Another potential issue with the fin isolation techniques described in the above is that stress in the semiconductor fin desirable for improving carrier mobility may be lost from the channel region of the transistor where too many fin surfaces are left free during fabrication, allowing fin strain to relax. Device architectures and fabrication techniques that maintain higher levels of desirable fin stress therefore offer advantageous improvements in non-planar transistor performance.

**[0059]** In accordance with an embodiment of the present disclosure, through-gate fin isolation architectures and techniques are described herein. In the exemplary embodiments illustrated, non-planar transistors in a microelectronic device, such as an integrated circuit (IC) are isolated from one another in a manner that is self-aligned to gate electrodes of the transistors. Although embodiments of the present disclosure are applicable to virtually any IC employing non-planar transistors, exemplary ICs include, but are not limited to, microprocessor cores including logic and memory (SRAM) portions, RFICs (e.g., wireless ICs including digital baseband and analog front end modules), and power ICs.

**[0060]** In embodiments, two ends of adjacent semiconductor fins are electrically isolated from each other with an isolation region that is positioned relative to gate electrodes with the use of only one patterning mask level. In an embodiment, a single mask is employed to form a plurality of sacrificial placeholder stripes of a fixed pitch, a first subset of the placeholder stripes define a location or dimension of isolation regions while a second subset of the placeholder stripes defines a location or dimension of a gate electrode. In certain embodiments, the first subset of placeholder stripes is removed and isolation cuts made into the semiconductor fins in the openings resulting from the first subset removal while the second subset of the placeholder stripes is ultimately replaced with non-sacrificial gate electrode stacks. Since a subset of placeholders utilized for gate electrode replacement are employed to form the isolation regions, the method and resulting architecture is referred to herein as “through-gate” isolation. One or more through-gate isolation embodiments described herein, may, for example, enable higher transistor densities and higher levels of advantageous transistor channel stress.

**[0061]** With isolation defined after placement or definition of the gate electrode, a greater transistor density can be achieved because fin isolation dimensioning and placement can be made perfectly on-pitch with the gate electrodes so that both gate electrodes and isolation regions are integer multiples of a minimum feature pitch of a single masking level. In further embodiments where the semiconductor fin has a lattice mismatch with a substrate on which the fin is disposed, greater degrees of strain are maintained by defining the isolation after placement or definition of the gate electrode. For such embodiments, other features of the

transistor (such as the gate electrode and added source or drain materials) that are formed before ends of the fin are defined help to mechanically maintain fin strain after an isolation cut is made into the fin.

**[0062]** To provide further context, transistor scaling can benefit from a denser packing of cells within the chip. Currently, most cells are separated from their neighbors by two or more dummy gates, which have buried fins. The cells are isolated by etching the fins beneath these two or more dummy gates, which connect one cell to the other. Scaling can benefit significantly if the number of dummy gates that separate neighboring cells can be reduced from two or more down to one. As explained above, one solution requires two or more dummy gates. The fins under the two or more dummy gates are etched during fin patterning. A potential issue with such an approach is that dummy gates consume space on the chip which can be used for cells. In an embodiment, approaches described herein enable the use of only a single dummy gate to separate neighboring cells.

**[0063]** In an embodiment, a fin trim isolation approach is implemented as a self-aligned patterning scheme. Here, the fins beneath a single gate are etched out. Thus, neighboring cells can be separated by a single dummy gate. Advantages to such an approach may include saving space on the chip and allowing for more computational power for a given area. The approach may also allow for fin trim to be performed at a sub-fin pitch distance.

**[0064]** For comparative purposes, FIGS. 3A and 3B illustrate plan views representing various operations in a method of patterning of fins with multi-gate spacing for forming a local isolation structure.

**[0065]** Referring to FIG. 3A, a plurality of fins 302 is shown having a length along a first direction 304. A grid 306, having spacings 307 there between, defining locations for ultimately forming a plurality of gate lines is shown along a second direction 308 orthogonal to the first direction 304.

**[0066]** Referring to FIG. 3B, a portion of the plurality of fins 302 is cut (e.g., removed by an etch process) to leave fins 310 having a cut 312 therein. An isolation structure ultimately formed in the cut 312 therefore has a dimension of more than a single gate line, e.g., a dimension of three gate lines 306. Accordingly, gate structures ultimately formed along the locations of the gate lines 306 will be formed at least partially over an isolation structure formed in cut 312. Thus, cut 312 is a relatively wide fin cut.

**[0067]** FIGS. 3C-3F illustrate plan views representing various operations in a method of patterning of fins with single gate spacing for forming a local isolation structure, in accordance with another embodiment of the present disclosure.

**[0068]** Referring to FIG. 3C, a method of fabricating an integrated circuit structure includes forming a plurality of fins 322, individual ones of the plurality of fins 322 having a longest dimension along a first direction 324. A plurality of gate structures 326 is over the plurality of fins 322, individual ones of the gate structures 326 having a longest dimension along a second direction 328 orthogonal to the first direction 324. In an embodiment, the gate structures 326 are sacrificial or dummy gate lines, e.g., fabricated from polycrystalline silicon. In one embodiment, the plurality of fins 322 are silicon fins and are continuous with a portion of an underlying silicon substrate.

[0069] Referring to FIG. 3D, a dielectric material structure 330 is formed between adjacent ones of the plurality of gate structures 326.

[0070] Referring to FIG. 3E, a portion 332 of one of the plurality of gate structures 326 is removed to expose a portion 334 of each of the plurality of fins 322. In an embodiment, removing the portion 332 of the one of the plurality of gate structures 326 involves using a lithographic window 336 wider than a width 338 of the portion 332 of the one of the plurality of gate structures 326.

[0071] Referring to FIG. 3F, the exposed portion 334 of each of the plurality of fins 322 is removed to form a cut region 340. In an embodiment, the exposed portion 334 of each of the plurality of fins 322 is removed using a dry or plasma etch process. In an embodiment, removing the exposed portion 334 of each of the plurality of fins 322 involves etching to a depth less than a height of the plurality of fins 322. In one such embodiment, the depth is greater than a depth of source or drain regions in the plurality of fins 322. In an embodiment, the depth is deeper than a depth of an active portion of the plurality of fins 322 to provide isolation margin. In an embodiment, the exposed portion 334 of each of the plurality of fins 322 is removed without etching or without substantially etching source or drain regions (such as epitaxial source or drain regions) of the plurality of fins 322. In one such embodiment, the exposed portion 334 of each of the plurality of fins 322 is removed without laterally etching or without substantially laterally etching source or drain regions (such as epitaxial source or drain regions) of the plurality of fins 322. In an embodiment, the cut region 340 is ultimately filled with an insulating layer, e.g., in locations of the removed portion 334 of each of the plurality of fins 322 to form a “poly cut” or “plug” structure.

[0072] In an embodiment, the process of FIGS. 3C-3F are used in or together with a pre-spacer-deposition cut gate approach, such as described in association with FIGS. 1A, 1B and 2A-2G, and can be fabricated together with associated defect test structures such as described in association with FIGS. 1C-1E.

[0073] In another aspect, there may be a relationship between locations where gate line cuts (poly cuts) are made and fin-trim isolation (FTI) local fin cuts are made. In an embodiment, FTI local fin cuts are made only in locations where poly cuts are made. In one such embodiment, however, an FTI cut is not necessarily made at every location where a poly cut is made.

[0074] FIGS. 3G and 3H illustrate plan views representing various operations in a method of patterning of fins with single gate spacing for forming a local isolation structure in select gate line cut locations, in accordance with an embodiment of the present disclosure.

[0075] Referring to FIG. 3G, a method of fabricating an integrated circuit structure includes forming a plurality of fins 352, individual ones of the plurality of fins 352 having a longest dimension along a first direction 354. A plurality of gate structures 356 is over the plurality of fins 352, individual ones of the gate structures 356 having a longest dimension along a second direction 358 orthogonal to the first direction 354. In an embodiment, the gate structures 356 are sacrificial or dummy gate lines, e.g., fabricated from polycrystalline silicon. In one embodiment, the plurality of fins 352 are silicon fins and are continuous with a portion of an underlying silicon substrate.

[0076] Referring again to FIG. 3G, a dielectric material structure 360 is formed between adjacent ones of the plurality of gate structures 356. Portions 362 and 363 of two of the plurality of gate structures 356 are removed to expose portions of each of the plurality of fins 352. In an embodiment, removing the portions 362 and 363 of the two gate structures 356 involves using a lithographic window wider than a width of each of the portions 362 and 363 of the gate structures 356. The exposed portion of each of the plurality of fins 352 at location 362 is removed to form a cut region 370. In an embodiment, the exposed portion of each of the plurality of fins 352 is removed using a dry or plasma etch process. However, the exposed portion of each of the plurality of fins 352 at location 363 is masked from removal. In an embodiment, the region 362/370 represents both a poly cut and an FTI local fin cut. However, the location 363 represents a poly cut only. Referring to FIG. 3H, the location 362/370 of the poly cut and FTI local fin cut and the location 363 of the poly cut are filled with insulating structures 380 such as a dielectric plugs or “poly cut” or “plug” structures. [0077] In an embodiment, the process of FIGS. 3G-3H are used in or together with a pre-spacer-deposition cut gate approach, such as described in association with FIGS. 1A, 1B and 2A-2G, and can be fabricated together with associated defect test structures such as described in association with FIGS. 1C-1E.

[0078] FIG. 3I illustrates exemplary mask splitting schematics for a method of fabricating a gate-all-around integrated circuit structure using a pre-spacer-deposition cut gate approach, in accordance with an embodiment of the present disclosure.

[0079] Referring to FIG. 3I, a mask 390 includes a wide PCT feature 391 between structures 392. A mask 393 includes narrow PCT features 394 (e.g., a pre-spacer feature) between structures 395. A mask 396 includes a PCT/FTI feature 397 between structures 398. In an embodiment, masks of FIG. 3I are used in a pre-spacer-deposition cut gate approach, such as described in association with FIGS. 1A, 1B and 2A-2G.

[0080] It is to be appreciated that the embodiments described herein can also include other implementations such as nanowires and/or nanoribbons with various widths, thicknesses and/or materials including but not limited to Si and SiGe. For example, group III-V materials may be used.

[0081] It is to be appreciated that, in a particular embodiment, nanowires or nanoribbons, or sacrificial intervening layers, may be composed of silicon. As used throughout, a silicon layer may be used to describe a silicon material composed of a very substantial amount of, if not all, silicon. However, it is to be appreciated that, practically, 100% pure Si may be difficult to form and, hence, could include a tiny percentage of carbon, germanium or tin. Such impurities may be included as an unavoidable impurity or component during deposition of Si or may “contaminate” the Si upon diffusion during post deposition processing. As such, embodiments described herein directed to a silicon layer may include a silicon layer that contains a relatively small amount, e.g., “impurity” level, non-Si atoms or species, such as Ge, C or Sn. It is to be appreciated that a silicon layer as described herein may be undoped or may be doped with dopant atoms such as boron, phosphorous or arsenic.

[0082] It is to be appreciated that, in a particular embodiment, nanowires or nanoribbons, or sacrificial intervening layers, may be composed of silicon germanium. As used

throughout, a silicon germanium layer may be used to describe a silicon germanium material composed of substantial portions of both silicon and germanium, such as at least 5% of both. In some embodiments, the amount of germanium is greater than the amount of silicon. In particular embodiments, a silicon germanium layer includes approximately 60% germanium and approximately 40% silicon ( $\text{Si}_{40}\text{Ge}_{60}$ ). In other embodiments, the amount of silicon is greater than the amount of germanium. In particular embodiments, a silicon germanium layer includes approximately 30% germanium and approximately 70% silicon ( $\text{Si}_{70}\text{Ge}_{30}$ ). It is to be appreciated that, practically, 100% pure silicon germanium (referred to generally as SiGe) may be difficult to form and, hence, could include a tiny percentage of carbon or tin. Such impurities may be included as an unavoidable impurity or component during deposition of SiGe or may “contaminate” the SiGe upon diffusion during post deposition processing. As such, embodiments described herein directed to a silicon germanium layer may include a silicon germanium layer that contains a relatively small amount, e.g., “impurity” level, non-Ge and non-Si atoms or species, such as carbon or tin. It is to be appreciated that a silicon germanium layer as described herein may be undoped or may be doped with dopant atoms such as boron, phosphorous or arsenic.

**[0083]** Described below are various devices and processing schemes that may be used to fabricate a device that can be integrated with a pre-spacer-deposition cut gate, and can be fabricated together with associated defect test structures such as described in association with FIGS. 1C-1E. It is to be appreciated that the exemplary embodiments need not necessarily require all features described, or may include more features than are described. For example, nanowire release processing may be performed through a replacement gate trench. Examples of such release processes are described below. Additionally, in yet another aspect, back-end (BE) interconnect scaling can result in lower performance and higher manufacturing cost due to patterning complexity. Embodiments described herein may be implemented to enable front side and backside interconnect integration for nanowire transistors. Embodiments described herein may provide an approach to achieve a relatively wider interconnect pitch. The result may be improved product performance and lower patterning costs. Embodiments may be implemented to enable robust functionality of scaled nanowire or nanoribbon transistors with low power and high performance.

**[0084]** One or more embodiments described herein are directed dual epitaxial (EPI) connections for nanowire or nanoribbon transistors using partial source or drain (SD) and asymmetric trench contact (TCN) depth. In an embodiment, an integrated circuit structure is fabricated by forming source-drain openings of nanowire/nanoribbon transistors which are partially filled with SD epitaxy. A remainder of the opening is filled with a conductive material. Deep trench formation on one of the source or drain side enables direct contact to a backside interconnect level.

**[0085]** As an exemplary process flow for fabricating a gate-all-around device of a gate-all-around integrated circuit structure, FIGS. 4A-4J illustrates cross-sectional views of various operations in a method of fabricating a gate-all-around integrated circuit structure, in accordance with an embodiment of the present disclosure.

**[0086]** Referring to FIG. 4A, a method of fabricating an integrated circuit structure includes forming a starting stack which includes alternating sacrificial layers **404** and nanowires **406** above a fin **402**, such as a silicon fin. The nanowires **406** may be referred to as a vertical arrangement of nanowires. A protective cap **408** may be formed above the alternating sacrificial layers **404** and nanowires **406**, as is depicted. A relaxed buffer layer **452** and a defect modification layer **450** may be formed beneath the alternating sacrificial layers **404** and nanowires **406**, as is also depicted.

**[0087]** Referring to FIG. 4B, a gate stack **410** is formed over the vertical arrangement of horizontal nanowires **406**. Portions of the vertical arrangement of horizontal nanowires **406** are then released by removing portions of the sacrificial layers **404** to provide recessed sacrificial layers **404'** and cavities **412**, as is depicted in FIG. 4C.

**[0088]** It is to be appreciated that the structure of FIG. 4C may be fabricated to completion without first performing the deep etch and asymmetric contact processing described below. In either case (e.g., with or without asymmetric contact processing), in an embodiment, a fabrication process involves use of a process scheme that provides a gate-all-around integrated circuit structure having epitaxial nubs, which may be vertically discrete source or drain structures.

**[0089]** Referring to FIG. 4D, upper gate spacers **414** are formed at sidewalls of the gate structure **410**. Cavity spacers **416** are formed in the cavities **412** beneath the upper gate spacers **414**. A deep trench contact etch is then optionally performed to form trenches **418** and to form recessed nanowires **406'**. A patterned relaxed buffer layer **452'** and a patterned defect modification layer **450'** may also be present, as is depicted.

**[0090]** A sacrificial material **420** is then formed in the trenches **418**, as is depicted in FIG. 4E. In other process schemes, an isolated trench bottom or silicon trench bottom may be used.

**[0091]** Referring to FIG. 4F, a first epitaxial source or drain structure (e.g., left-hand features **422**) is formed at a first end of the vertical arrangement of horizontal nanowires **406'**. A second epitaxial source or drain structure (e.g., right-hand features **422**) is formed at a second end of the vertical arrangement of horizontal nanowires **406'**. In an embodiment, as depicted, the epitaxial source or drain structures **422** are vertically discrete source or drain structures and may be referred to as epitaxial nubs.

**[0092]** An inter-layer dielectric (ILD) material **424** is then formed at the sides of the gate electrode **410** and adjacent the source or drain structures **422**, as is depicted in FIG. 4G. Referring to FIG. 4H, a replacement gate process is used to form a permanent gate dielectric **428** and a permanent gate electrode **426**. The ILD material **424** is then removed, as is depicted in FIG. 4I. The sacrificial material **420** is then removed from one of the source drain locations (e.g., right-hand side) to form trench **432**, but is not removed from the other of the source drain locations to form trench **430**.

**[0093]** Referring to FIG. 4J, a first conductive contact structure **434** is formed coupled to the first epitaxial source or drain structure (e.g., left-hand features **422**). A second conductive contact structure **436** is formed coupled to the second epitaxial source or drain structure (e.g., right-hand features **422**). The second conductive contact structure **436** is formed deeper along the fin **402** than the first conductive contact structure **434**. In an embodiment, although not depicted in FIG. 4J, the method further includes forming an

exposed surface of the second conductive contact structure **436** at a bottom of the fin **402**. Conductive contacts may include a contact resistance reducing layer and a primary contact electrode layer, where examples can include Ti, Ni, Co (for the former and W, Ru, Co for the latter.)

**[0094]** In an embodiment, the second conductive contact structure **436** is deeper along the fin **402** than the first conductive contact structure **434**, as is depicted. In one such embodiment, the first conductive contact structure **434** is not along the fin **402**, as is depicted. In another such embodiment, not depicted, the first conductive contact structure **434** is partially along the fin **402**.

**[0095]** In an embodiment, the second conductive contact structure **436** is along an entirety of the fin **402**. In an embodiment, although not depicted, in the case that the bottom of the fin **402** is exposed by a backside substrate removal process, the second conductive contact structure **436** has an exposed surface at a bottom of the fin **402**.

**[0096]** In an embodiment, the structure of FIG. **4J**, or related structures of FIGS. **4A-4J**, is formed using a pre-spacer-deposition cut gate approach, such as described in association with FIGS. **1A**, **1B**, **2A-2G** and **3I**, and can be fabricated together with associated defect test structures such as described in association with FIGS. **1C-1E**.

**[0097]** In another aspect, in order to enable access to both conductive contact structures of a pair of asymmetric source and drain contact structures, integrated circuit structures described herein may be fabricated using a backside reveal of front side structures fabrication approach. In some exemplary embodiments, reveal of the backside of a transistor or other device structure entails wafer-level backside processing. In contrast to a conventional TSV-type technology, a reveal of the back-side of a transistor as described herein may be performed at the density of the device cells, and even within sub-regions of a device. Furthermore, such a reveal of the backside of a transistor may be performed to remove substantially all of a donor substrate upon which a device layer was disposed during front side device processing. As such, a microns-deep TSV becomes unnecessary with the thickness of semiconductor in the device cells following a reveal of the backside of a transistor potentially being only tens or hundreds of nanometers.

**[0098]** Reveal techniques described herein may enable a paradigm shift from “bottom-up” device fabrication to “center-out” fabrication, where the “center” is any layer that is employed in front side fabrication, revealed from the backside, and again employed in backside fabrication. Processing of both a front side and revealed backside of a device structure may address many of the challenges associated with fabricating 3D ICs when primarily relying on front side processing.

**[0099]** A reveal of the backside of a transistor approach may be employed for example to remove at least a portion of a carrier layer and intervening layer of a donor-host substrate assembly. The process flow begins with an input of a donor-host substrate assembly. A thickness of a carrier layer in the donor-host substrate is polished (e.g., CMP) and/or etched with a wet or dry (e.g., plasma) etch process. Any grind, polish, and/or wet/dry etch process known to be suitable for the composition of the carrier layer may be employed. For example, where the carrier layer is a group IV semiconductor (e.g., silicon) a CMP slurry known to be suitable for thinning the semiconductor may be employed.

Likewise, any wet etchant or plasma etch process known to be suitable for thinning the group IV semiconductor may also be employed.

**[0100]** In some embodiments, the above is preceded by cleaving the carrier layer along a fracture plane substantially parallel to the intervening layer. The cleaving or fracture process may be utilized to remove a substantial portion of the carrier layer as a bulk mass, reducing the polish or etch time needed to remove the carrier layer. For example, where a carrier layer is 400-900  $\mu\text{m}$  in thickness, 100-700  $\mu\text{m}$  may be cleaved off by practicing any blanket implant known to promote a wafer-level fracture. In some exemplary embodiments, a light element (e.g., H, He, or Li) is implanted to a uniform target depth within the carrier layer where the fracture plane is desired. Following such a cleaving process, the thickness of the carrier layer remaining in the donor-host substrate assembly may then be polished or etched to complete removal. Alternatively, where the carrier layer is not fractured, the grind, polish and/or etch operation may be employed to remove a greater thickness of the carrier layer.

**[0101]** Next, exposure of an intervening layer is detected. Detection is used to identify a point when the backside surface of the donor substrate has advanced to nearly the device layer. Any endpoint detection technique known to be suitable for detecting a transition between the materials employed for the carrier layer and the intervening layer may be practiced. In some embodiments, one or more endpoint criteria are based on detecting a change in optical absorbance or emission of the backside surface of the donor substrate during the polishing or etching performance. In some other embodiments, the endpoint criteria are associated with a change in optical absorbance or emission of byproducts during the polishing or etching of the donor substrate backside surface. For example, absorbance or emission wavelengths associated with the carrier layer etch byproducts may change as a function of the different compositions of the carrier layer and intervening layer. In other embodiments, the endpoint criteria are associated with a change in mass of species in byproducts of polishing or etching the backside surface of the donor substrate. For example, the byproducts of processing may be sampled through a quadrupole mass analyzer and a change in the species mass may be correlated to the different compositions of the carrier layer and intervening layer. In another exemplary embodiment, the endpoint criteria is associated with a change in friction between a backside surface of the donor substrate and a polishing surface in contact with the backside surface of the donor substrate.

**[0102]** Detection of the intervening layer may be enhanced where the removal process is selective to the carrier layer relative to the intervening layer as non-uniformity in the carrier removal process may be mitigated by an etch rate delta between the carrier layer and intervening layer. Detection may even be skipped if the grind, polish and/or etch operation removes the intervening layer at a rate sufficiently below the rate at which the carrier layer is removed. If an endpoint criteria is not employed, a grind, polish and/or etch operation of a predetermined fixed duration may stop on the intervening layer material if the thickness of the intervening layer is sufficient for the selectivity of the etch. In some examples, the carrier etch rate: intervening layer etch rate is 3:1-10:1, or more.

**[0103]** Upon exposing the intervening layer, at least a portion of the intervening layer may be removed. For

example, one or more component layers of the intervening layer may be removed. A thickness of the intervening layer may be removed uniformly by a polish, for example. Alternatively, a thickness of the intervening layer may be removed with a masked or blanket etch process. The process may employ the same polish or etch process as that employed to thin the carrier, or may be a distinct process with distinct process parameters. For example, where the intervening layer provides an etch stop for the carrier removal process, the latter operation may employ a different polish or etch process that favors removal of the intervening layer over removal of the device layer. Where less than a few hundred nanometers of intervening layer thickness is to be removed, the removal process may be relatively slow, optimized for across-wafer uniformity, and more precisely controlled than that employed for removal of the carrier layer. A CMP process employed may, for example employ a slurry that offers very high selectivity (e.g., 100:1-300:1, or more) between semiconductor (e.g., silicon) and dielectric material (e.g., SiO) surrounding the device layer and embedded within the intervening layer, for example, as electrical isolation between adjacent device regions.

[0104] For embodiments where the device layer is revealed through complete removal of the intervening layer, backside processing may commence on an exposed backside of the device layer or specific device regions there in. In some embodiments, the backside device layer processing includes a further polish or wet/dry etch through a thickness of the device layer disposed between the intervening layer and a device region previously fabricated in the device layer, such as a source or drain region.

[0105] In some embodiments where the carrier layer, intervening layer, or device layer backside is recessed with a wet and/or plasma etch, such an etch may be a patterned etch or a materially selective etch that imparts significant non-planarity or topography into the device layer backside surface. As described further below, the patterning may be within a device cell (i.e., “intra-cell” patterning) or may be across device cells (i.e., “inter-cell” patterning). In some patterned etch embodiments, at least a partial thickness of the intervening layer is employed as a hard mask for backside device layer patterning. Hence, a masked etch process may preface a correspondingly masked device layer etch.

[0106] The above described processing scheme may result in a donor-host substrate assembly that includes IC devices that have a back-side of an intervening layer, a backside of the device layer, and/or backside of one or more semiconductor regions within the device layer, and/or front side metallization revealed. Additional backside processing of any of these revealed regions may then be performed during downstream processing.

[0107] It is to be appreciated that the structures resulting from the above exemplary processing schemes may be used in a same or similar form for subsequent processing operations to complete device fabrication, such as PMOS and/or NMOS device fabrication. As an example of a completed device, FIG. 5 illustrates a cross-sectional view of a non-planar integrated circuit structure as taken along a gate line, in accordance with an embodiment of the present disclosure.

[0108] Referring to FIG. 5, a semiconductor structure or device 500 includes a non-planar active region (e.g., a fin structure including protruding fin portion 504 and sub-fin region 505) within a trench isolation region 506. In an

embodiment, instead of a solid fin, the non-planar active region is separated into nanowires (such as nanowires 504A and 504B) above sub-fin region 505, as is represented by the dashed lines. In either case, for ease of description for non-planar integrated circuit structure 500, a non-planar active region 504 is referenced below as a protruding fin portion. In an embodiment, the sub-fin region 505 also includes a relaxed buffer layer 542 and a defect modification layer 540, as is depicted.

[0109] A gate line 508 is disposed over the protruding portions 504 of the non-planar active region (including, if applicable, surrounding nanowires 504A and 504B), as well as over a portion of the trench isolation region 506. As shown, gate line 508 includes a gate electrode 550 and a gate dielectric layer 552. In one embodiment, gate line 508 may also include a dielectric cap layer 554. A gate contact 514, and overlying gate contact via 516 are also seen from this perspective, along with an overlying metal interconnect 560, all of which are disposed in inter-layer dielectric stacks or layers 570. Also seen from the perspective of FIG. 5, the gate contact 514 is, in one embodiment, disposed over trench isolation region 506, but not over the non-planar active regions. In another embodiment, the gate contact 514 is over the non-planar active regions.

[0110] In an embodiment, the semiconductor structure or device 500 is a non-planar device such as, but not limited to, a fin-FET device, a tri-gate device, a nanoribbon device, or a nanowire device. In such an embodiment, a corresponding semiconducting channel region is composed of or is formed in a three-dimensional body. In one such embodiment, the gate electrode stacks of gate lines 508 surround at least a top surface and a pair of sidewalls of the three-dimensional body.

[0111] As is also depicted in FIG. 5, in an embodiment, an interface 580 exists between a protruding fin portion 504 and sub-fin region 505. The interface 580 can be a transition region between a doped sub-fin region 505 and a lightly or undoped upper fin portion 504. In one such embodiment, each fin is approximately 10 nanometers wide or less, and sub-fin dopants are optionally supplied from an adjacent solid state doping layer at the sub-fin location. In a particular such embodiment, each fin is less than 10 nanometers wide.

[0112] Although not depicted in FIG. 5, it is to be appreciated that source or drain regions of or adjacent to the protruding fin portions 504 are on either side of the gate line 508, i.e., into and out of the page. In one embodiment, the material of the protruding fin portions 504 in the source or drain locations is removed and replaced with another semiconductor material, e.g., by epitaxial deposition to form epitaxial source or drain structures. The source or drain regions may extend below the height of dielectric layer of trench isolation region 506, i.e., into the sub-fin region 505. In accordance with an embodiment of the present disclosure, the more heavily doped sub-fin regions, i.e., the doped portions of the fins below interface 580, inhibits source to drain leakage through this portion of the bulk semiconductor fins. In an embodiment, the source and drain regions have associated asymmetric source and drain contact structures, as described above in association with FIG. 4J.

[0113] With reference again to FIG. 5, in an embodiment, fins 504/505 (and, possibly nanowires 504A and 504B) are composed of a crystalline silicon germanium layer which

may be doped with a charge carrier, such as but not limited to phosphorus, arsenic, boron, gallium or a combination thereof.

**[0114]** In an embodiment, trench isolation region **506**, and trench isolation regions (trench isolations structures or trench isolation layers) described throughout, may be composed of a material suitable to ultimately electrically isolate, or contribute to the isolation of, portions of a permanent gate structure from an underlying bulk substrate or isolate active regions formed within an underlying bulk substrate, such as isolating fin active regions. For example, in one embodiment, trench isolation region **506** is composed of a dielectric material such as, but not limited to, silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride.

**[0115]** Gate line **508** may be composed of a gate electrode stack which includes a gate dielectric layer **552** and a gate electrode layer **550**. In an embodiment, the gate electrode of the gate electrode stack is composed of a metal gate and the gate dielectric layer is composed of a high-k material. For example, in one embodiment, the gate dielectric layer **552** is composed of a material such as, but not limited to, hafnium oxide, hafnium oxy-nitride, hafnium silicate, lanthanum oxide, zirconium oxide, zirconium silicate, tantalum oxide, barium strontium titanate, barium titanate, strontium titanate, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, lead zinc niobate, or a combination thereof. Furthermore, a portion of gate dielectric layer **552** may include a layer of native oxide formed from the top few layers of the substrate fin **504**. In an embodiment, the gate dielectric layer **552** is composed of a top high-k portion and a lower portion composed of an oxide of a semiconductor material. In one embodiment, the gate dielectric layer **552** is composed of a top portion of hafnium oxide and a bottom portion of silicon dioxide or silicon oxy-nitride. In some implementations, a portion of the gate dielectric is a “U”-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate.

**[0116]** In one embodiment, the gate electrode layer **550** is composed of a metal layer such as, but not limited to, metal nitrides, metal carbides, metal silicides, metal aluminides, hafnium, zirconium, titanium, tantalum, aluminum, ruthenium, palladium, platinum, cobalt, nickel or conductive metal oxides. In a specific embodiment, the gate electrode layer **550** is composed of a non-workfunction-setting fill material formed above a metal workfunction-setting layer. The gate electrode layer **550** may consist of a P-type workfunction metal or an N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer **550** may consist of a stack of two or more metal layers, where one or more metal layers are workfunction metal layers and at least one metal layer is a conductive fill layer. For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, tungsten and conductive metal oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium car-

bide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV. In some implementations, the gate electrode may consist of a “U”-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further implementations of the disclosure, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

**[0117]** Spacers associated with the gate electrode stacks may be composed of a material suitable to ultimately electrically isolate, or contribute to the isolation of, a permanent gate structure from adjacent conductive contacts, such as self-aligned contacts. For example, in one embodiment, the spacers are composed of a dielectric material such as, but not limited to, silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride.

**[0118]** Gate contact **514** and overlying gate contact via **516** may be composed of a conductive material. In an embodiment, one or more of the contacts or vias are composed of a metal species. The metal species may be a pure metal, such as tungsten, nickel, or cobalt, or may be an alloy such as a metal-metal alloy or a metal-semiconductor alloy (e.g., such as a silicide material).

**[0119]** In an embodiment (although not shown), a contact pattern which is essentially perfectly aligned to an existing gate pattern **508** is formed while eliminating the use of a lithographic step with exceedingly tight registration budget. In an embodiment, the contact pattern is a vertically symmetric contact pattern, or an asymmetric contact pattern such as described in association with FIG. 4J. In other embodiments, all contacts are front-side connected and are not asymmetric. In one such embodiment, the self-aligned approach enables the use of intrinsically highly selective wet etching (e.g., versus conventionally implemented dry or plasma etching) to generate contact openings. In an embodiment, a contact pattern is formed by utilizing an existing gate pattern in combination with a contact plug lithography operation. In one such embodiment, the approach enables elimination of the need for an otherwise critical lithography operation to generate a contact pattern, as used in conventional approaches. In an embodiment, a trench contact grid is not separately patterned, but is rather formed between poly (gate) lines. For example, in one such embodiment, a trench contact grid is formed subsequent to gate grating patterning but prior to gate grating cuts.

**[0120]** In an embodiment, providing structure **500** involves fabrication of the gate stack structure **508** by a replacement gate process. In such a scheme, dummy gate material such as polysilicon or silicon nitride pillar material, may be removed and replaced with permanent gate electrode material. In one such embodiment, a permanent gate dielectric layer is also formed in this process, as opposed to being carried through from earlier processing. In an embodiment,

dummy gates are removed by a dry etch or wet etch process. In one embodiment, dummy gates are composed of polycrystalline silicon or amorphous silicon and are removed with a dry etch process including use of  $\text{SF}_6$ . In another embodiment, dummy gates are composed of polycrystalline silicon or amorphous silicon and are removed with a wet etch process including use of aqueous  $\text{NH}_4\text{OH}$  or tetramethylammonium hydroxide. In one embodiment, dummy gates are composed of silicon nitride and are removed with a wet etch including aqueous phosphoric acid.

**[0121]** Referring again to FIG. 5, the arrangement of semiconductor structure or device 500 places the gate contact over isolation regions. Such an arrangement may be viewed as inefficient use of layout space. In another embodiment, however, a semiconductor device has contact structures that contact portions of a gate electrode formed over an active region, e.g., over a fin 505, and in a same layer as a trench contact via.

**[0122]** In an embodiment, the structure of FIG. 5 is formed using a pre-spacer-deposition cut gate approach, such as described in association with FIGS. 1A, 1B, 2A-2G and 3I, and can be fabricated together with associated defect test structures such as described in association with FIGS. 1C-1E.

**[0123]** It is to be appreciated that not all aspects of the processes described above need be practiced to fall within the spirit and scope of embodiments of the present disclosure. Also, the processes described herein may be used to fabricate one or a plurality of semiconductor devices. The semiconductor devices may be transistors or like devices. For example, in an embodiment, the semiconductor devices are a metal-oxide semiconductor (MOS) transistors for logic or memory, or are bipolar transistors. Also, in an embodiment, the semiconductor devices have a three-dimensional architecture, such as a nanowire device, a nanoribbon device, a tri-gate device, an independently accessed double gate device, or a FIN-FET. One or more embodiments may be particularly useful for fabricating semiconductor devices at a sub-10 nanometer (10 nm) technology node.

**[0124]** In an embodiment, as used throughout the present description, interlayer dielectric (ILD) material is composed of or includes a layer of a dielectric or insulating material. Examples of suitable dielectric materials include, but are not limited to, oxides of silicon (e.g., silicon dioxide ( $\text{SiO}_2$ )), doped oxides of silicon, fluorinated oxides of silicon, carbon doped oxides of silicon, various low-k dielectric materials known in the arts, and combinations thereof. The interlayer dielectric material may be formed by conventional techniques, such as, for example, chemical vapor deposition (CVD), physical vapor deposition (PVD), or by other deposition methods.

**[0125]** In an embodiment, as is also used throughout the present description, metal lines or interconnect line material (and via material) is composed of one or more metal or other conductive structures. A common example is the use of copper lines and structures that may or may not include barrier layers between the copper and surrounding ILD material. As used herein, the term metal includes alloys, stacks, and other combinations of multiple metals. For example, the metal interconnect lines may include barrier layers (e.g., layers including one or more of Ta, TaN, Ti or TiN), stacks of different metals or alloys, etc. Thus, the interconnect lines may be a single material layer, or may be

formed from several layers, including conductive liner layers and fill layers. Any suitable deposition process, such as electroplating, chemical vapor deposition or physical vapor deposition, may be used to form interconnect lines. In an embodiment, the interconnect lines are composed of a conductive material such as, but not limited to, Cu, Al, Ti, Zr, Hf, V, Ru, Co, Ni, Pd, Pt, W, Ag, Au or alloys thereof. The interconnect lines are also sometimes referred to in the art as traces, wires, lines, metal, or simply interconnect.

**[0126]** In an embodiment, as is also used throughout the present description, hardmask materials, capping layers, or plugs are composed of dielectric materials different from the interlayer dielectric material. In one embodiment, different hardmask, capping or plug materials may be used in different regions so as to provide different growth or etch selectivity to each other and to the underlying dielectric and metal layers. In some embodiments, a hardmask layer, capping or plug layer includes a layer of a nitride of silicon (e.g., silicon nitride) or a layer of an oxide of silicon, or both, or a combination thereof. Other suitable materials may include carbon-based materials. Other hardmask, capping or plug layers known in the arts may be used depending upon the particular implementation. The hardmask, capping or plug layers may be formed by CVD, PVD, or by other deposition methods.

**[0127]** In an embodiment, as is also used throughout the present description, lithographic operations are performed using 193 nm immersion lithography (i193), EUV and/or EBDW lithography, or the like. A positive tone or a negative tone resist may be used. In one embodiment, a lithographic mask is a tri-layer mask composed of a topographic masking portion, an anti-reflective coating (ARC) layer, and a photoresist layer. In a particular such embodiment, the topographic masking portion is a carbon hardmask (CHM) layer and the anti-reflective coating layer is a silicon ARC layer.

**[0128]** In another aspect, one or more embodiments are directed to neighboring semiconductor structures or devices separated by self-aligned gate endcap (SAGE) structures. Particular embodiments may be directed to integration of multiple width (multi-Wsi) nanowires and nanoribbons in a SAGE architecture and separated by a SAGE wall. In an embodiment, nanowires/nanoribbons are integrated with multiple Wsi in a SAGE architecture portion of a front-end process flow. Such a process flow may involve integration of nanowires and nanoribbons of different Wsi to provide robust functionality of next generation transistors with low power and high performance. Associated epitaxial source or drain regions may be embedded (e.g., portions of nanowires removed and then source or drain (S/D) growth is performed).

**[0129]** To provide further context, advantages of a self-aligned gate endcap (SAGE) architecture may include the enabling of higher layout density and, in particular, scaling of diffusion-to-diffusion spacing. To provide illustrative comparison, FIG. 6 illustrates cross-sectional views taken through nanowires and fins for a non-endcap architecture (left-hand side (a)) versus a self-aligned gate endcap (SAGE) architecture (right-hand side (b)), in accordance with an embodiment of the present disclosure.

**[0130]** Referring to the left-hand side (a) of FIG. 6, an integrated circuit structure 600 includes a substrate 602 having fins 604 protruding there from by an amount 606 above an isolation structure 608 laterally surrounding lower portions of the fins 604. Upper portions of the fins may



include a relaxed buffer layer **622** and a defect modification layer **620**, as is depicted. Corresponding nanowires **605** are over the fins **604**. A gate structure may be formed over the integrated circuit structure **600** to fabricate a device. However, breaks in such a gate structure may be accommodated for by increasing the spacing between fin **604**/nanowire **605** pairs.

[0131] By contrast, referring to the right-hand side (b) of FIG. 6, an integrated circuit structure **650** includes a substrate **652** having fins **654** protruding therefrom by an amount **656** above an isolation structure **658** laterally surrounding lower portions of the fins **654**. Upper portions of the fins may include a relaxed buffer layer **672** and a defect modification layer **670**, as is depicted. Corresponding nanowires **655** are over the fins **654**. Isolating SAGE walls **660** (which may include a hardmask thereon, as depicted) are included within the isolation structure **652** and between adjacent fin **654**/nanowire **655** pairs. The distance between an isolating SAGE wall **660** and a nearest fin **654**/nanowire **655** pair defines the gate endcap spacing **662**. A gate structure may be formed over the integrated circuit structure **600**, between insulating SAGE walls to fabricate a device. Breaks in such a gate structure are imposed by the isolating SAGE walls. Since the isolating SAGE walls **660** are self-aligned, restrictions from conventional approaches can be minimized to enable more aggressive diffusion-to-diffusion spacing. Furthermore, since gate structures include breaks at all locations, individual gate structure portions may be layer connected by local interconnects formed over the isolating SAGE walls **660**. In an embodiment, as depicted, the SAGE walls **660** each include a lower dielectric portion and a dielectric cap on the lower dielectric portion. In accordance with an embodiment of the present disclosure, a fabrication process for structures associated with FIG. 6 involves use of a process scheme that provides a gate-all-around integrated circuit structure having epitaxial source or drain structures.

[0132] In an embodiment, the structure of part (b) of FIG. 6 is formed using a pre-spacer-deposition cut gate approach, such as described in association with FIGS. 1A, 1B, 2A-2G and 3I, and can be fabricated together with associated defect test structures such as described in association with FIGS. 1C-1E.

[0133] A self-aligned gate endcap (SAGE) processing scheme involves the formation of gate/trench contact endcaps self-aligned to fins without requiring an extra length to account for mask mis-registration. Thus, embodiments may be implemented to enable shrinking of transistor layout area. Embodiments described herein may involve the fabrication of gate endcap isolation structures, which may also be referred to as gate walls, isolation gate walls or self-aligned gate endcap (SAGE) walls.

[0134] In an exemplary processing scheme for structures having SAGE walls separating neighboring devices, FIG. 7 illustrate cross-sectional views representing various operations in a method of fabricating a self-aligned gate endcap (SAGE) structure with gate-all-around devices, in accordance with an embodiment of the present disclosure.

[0135] Referring to part (a) of FIG. 7, a starting structure includes a nanowire patterning stack **704** above a substrate **702**. A lithographic patterning stack **706** is formed above the nanowire patterning stack **704**. The nanowire patterning stack **704** includes alternating sacrificial layers **710** and nanowire layers **712**, which may be above a relaxed buffer

layer **782** and a defect modification layer **780**, as is depicted. A protective mask **714** is between the nanowire patterning stack **704** and the lithographic patterning stack **706**. In one embodiment, the lithographic patterning stack **706** is tri-layer mask composed of a topographic masking portion **720**, an anti-reflective coating (ARC) layer **722**, and a photoresist layer **724**. In a particular such embodiment, the topographic masking portion **720** is a carbon hardmask (CHM) layer and the anti-reflective coating layer **722** is a silicon ARC layer. [0136] Referring to part (b) of FIG. 7, the stack of part (a) is lithographically patterned and then etched to provide an etched structure including a patterned substrate **702** and trenches **730**.

[0137] Referring to part (c) of FIG. 7, the structure of part (b) has an isolation layer **740** and a SAGE material **742** formed in trenches **730**. The structure is then planarized to leave patterned topographic masking layer **720'** as an exposed upper layer.

[0138] Referring to part (d) of FIG. 7, the isolation layer **740** is recessed below an upper surface of the patterned substrate **702**, e.g., to define a protruding fin portion and to provide a trench isolation structure **741** beneath SAGE walls **742**.

[0139] Referring to part (e) of FIG. 7, the sacrificial layers **710** are removed at least in the channel region to release nanowires **712A** and **712B**. Subsequent to the formation of the structure of part (e) of FIG. 7, a gate stacks may be formed around nanowires **712B** or **712A**, over protruding fins of substrate **702**, and between SAGE walls **742**. In one embodiment, prior to formation of the gate stacks, the remaining portion of protective mask **714** is removed. In another embodiment, the remaining portion of protective mask **714** is retained as an insulating fin hat as an artifact of the processing scheme.

[0140] Referring again to part (e) of FIG. 7, it is to be appreciated that a channel view is depicted, with source or drain regions being locating into and out of the page. In an embodiment, the channel region including nanowires **712B** has a width less than the channel region including nanowires **712A**. Thus, in an embodiment, an integrated circuit structure includes multiple width (multi-Wsi) nanowires. Although structures of **712B** and **712A** may be differentiated as nanowires and nanoribbons, respectively, both such structures are typically referred to herein as nanowires. It is also to be appreciated that reference to or depiction of a fin/nanowire pair throughout may refer to a structure including a fin and one or more overlying nanowires (e.g., two overlying nanowires are shown in FIG. 7). In accordance with an embodiment of the present disclosure, a fabrication process for structures associated with FIG. 7 involves use of a process scheme that provides a gate-all-around integrated circuit structure having epitaxial source or drain structures.

[0141] In an embodiment, the structure of part (e) FIG. 7 is formed using a pre-spacer-deposition cut gate approach, such as described in association with FIGS. 1A, 1B, 2A-2G and 3I, and can be fabricated together with associated defect test structures such as described in association with FIGS. 1C-1E.

[0142] In an embodiment, as described throughout, self-aligned gate endcap (SAGE) isolation structures may be composed of a material or materials suitable to ultimately electrically isolate, or contribute to the isolation of, portions of permanent gate structures from one another. Exemplary materials or material combinations include a single material

structure such as silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride. Other exemplary materials or material combinations include a multi-layer stack having lower portion silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride and an upper portion higher dielectric constant material such as hafnium oxide.

[0143] To highlight an exemplary integrated circuit structure having three vertically arranged nanowires, FIG. 8A illustrates a three-dimensional cross-sectional view of a nanowire-based integrated circuit structure, in accordance with an embodiment of the present disclosure. FIG. 8B illustrates a cross-sectional source or drain view of the nanowire-based integrated circuit structure of FIG. 8A, as taken along the a-a' axis. FIG. 8C illustrates a cross-sectional channel view of the nanowire-based integrated circuit structure of FIG. 8A, as taken along the b-b' axis.

[0144] Referring to FIG. 8A, an integrated circuit structure 800 includes one or more vertically stacked nanowires (804 set) above a substrate 802. In an embodiment, as depicted, a relaxed buffer layer 802C, a defect modification layer 802B, and a lower substrate portion 802A are included in substrate 802, as is depicted. An optional fin below the bottommost nanowire and formed from the substrate 802 is not depicted for the sake of emphasizing the nanowire portion for illustrative purposes. Embodiments herein are targeted at both single wire devices and multiple wire devices. As an example, a three nanowire-based devices having nanowires 804A, 804B and 804C is shown for illustrative purposes. For convenience of description, nanowire 804A is used as an example where description is focused on one of the nanowires. It is to be appreciated that where attributes of one nanowire are described, embodiments based on a plurality of nanowires may have the same or essentially the same attributes for each of the nanowires.

[0145] Each of the nanowires 804 includes a channel region 806 in the nanowire. The channel region 806 has a length (L). Referring to FIG. 8C, the channel region also has a perimeter (Pc) orthogonal to the length (L). Referring to both FIGS. 8A and 8C, a gate electrode stack 808 surrounds the entire perimeter (Pc) of each of the channel regions 806. The gate electrode stack 808 includes a gate electrode along with a gate dielectric layer between the channel region 806 and the gate electrode (not shown). In an embodiment, the channel region is discrete in that it is completely surrounded by the gate electrode stack 808 without any intervening material such as underlying substrate material or overlying channel fabrication materials. Accordingly, in embodiments having a plurality of nanowires 804, the channel regions 806 of the nanowires are also discrete relative to one another.

[0146] Referring to both FIGS. 8A and 8B, integrated circuit structure 800 includes a pair of non-discrete source or drain regions 810/812. The pair of non-discrete source or drain regions 810/812 is on either side of the channel regions 806 of the plurality of vertically stacked nanowires 804. Furthermore, the pair of non-discrete source or drain regions 810/812 is adjoining for the channel regions 806 of the plurality of vertically stacked nanowires 804. In one such embodiment, not depicted, the pair of non-discrete source or drain regions 810/812 is directly vertically adjoining for the channel regions 806 in that epitaxial growth is on and between nanowire portions extending beyond the channel regions 806, where nanowire ends are shown within the source or drain structures. In another embodiment, as

depicted in FIG. 8A, the pair of non-discrete source or drain regions 810/812 is indirectly vertically adjoining for the channel regions 806 in that they are formed at the ends of the nanowires and not between the nanowires.

[0147] In an embodiment, as depicted, the source or drain regions 810/812 are non-discrete in that there are not individual and discrete source or drain regions for each channel region 806 of a nanowire 804. Accordingly, in embodiments having a plurality of nanowires 804, the source or drain regions 810/812 of the nanowires are global or unified source or drain regions as opposed to discrete for each nanowire. That is, the non-discrete source or drain regions 810/812 are global in the sense that a single unified feature is used as a source or drain region for a plurality (in this case, 3) of nanowires 804 and, more particularly, for more than one discrete channel region 806. In one embodiment, from a cross-sectional perspective orthogonal to the length of the discrete channel regions 806, each of the pair of non-discrete source or drain regions 810/812 is approximately rectangular in shape with a bottom tapered portion and a top vertex portion, as depicted in FIG. 8B. In other embodiments, however, the source or drain regions 810/812 of the nanowires are relatively larger yet discrete non-vertically merged epitaxial structures such as nubs described in association with FIGS. 4A-4J.

[0148] In accordance with an embodiment of the present disclosure, and as depicted in FIGS. 8A and 8B, integrated circuit structure 800 further includes a pair of contacts 814, each contact 814 on one of the pair of non-discrete source or drain regions 810/812. In one such embodiment, in a vertical sense, each contact 814 completely surrounds the respective non-discrete source or drain region 810/812. In another aspect, the entire perimeter of the non-discrete source or drain regions 810/812 may not be accessible for contact with contacts 814, and the contact 814 thus only partially surrounds the non-discrete source or drain regions 810/812, as depicted in FIG. 8B. In a contrasting embodiment, not depicted, the entire perimeter of the non-discrete source or drain regions 810/812, as taken along the a-a' axis, is surrounded by the contacts 814.

[0149] Referring again to FIG. 8A, in an embodiment, integrated circuit structure 800 further includes a pair of spacers 816. As is depicted, outer portions of the pair of spacers 816 may overlap portions of the non-discrete source or drain regions 810/812, providing for "embedded" portions of the non-discrete source or drain regions 810/812 beneath the pair of spacers 816. As is also depicted, the embedded portions of the non-discrete source or drain regions 810/812 may not extend beneath the entirety of the pair of spacers 816.

[0150] Substrate 802 may be composed of a material suitable for integrated circuit structure fabrication. In one embodiment, substrate 802 includes a lower bulk substrate composed of a single crystal of a material which may include, but is not limited to, silicon, germanium, silicon-germanium, germanium-tin, silicon-germanium-tin, or a group III-V compound semiconductor material. An upper insulator layer composed of a material which may include, but is not limited to, silicon dioxide, silicon nitride or silicon oxy-nitride is on the lower bulk substrate. Thus, the structure 800 may be fabricated from a starting semiconductor-on-insulator substrate. Alternatively, the structure 800 is formed directly from a bulk substrate and local oxidation is used to form electrically insulative portions in place of the above

described upper insulator layer. In another alternative embodiment, the structure **800** is formed directly from a bulk substrate and doping is used to form electrically isolated active regions, such as nanowires, thereon. In one such embodiment, the first nanowire (i.e., proximate the substrate) is in the form of an omega-FET type structure.

**[0151]** In an embodiment, the nanowires **804** may be sized as wires or ribbons, as described below, and may have squared-off or rounder corners. In an embodiment, the nanowires **804** are composed of a material such as, but not limited to, silicon, germanium, or a combination thereof. In one such embodiment, the nanowires are single-crystalline. For example, for a silicon nanowire **804**, a single-crystalline nanowire may be based from a (100) global orientation, e.g., with a <100> plane in the z-direction. As described below, other orientations may also be considered. In an embodiment, the dimensions of the nanowires **804**, from a cross-sectional perspective, are on the nano-scale. For example, in a specific embodiment, the smallest dimension of the nanowires **804** is less than approximately 20 nanometers. In an embodiment, the nanowires **804** are composed of a strained material, particularly in the channel regions **806**.

**[0152]** Referring to FIGS. **8C**, in an embodiment, each of the channel regions **806** has a width ( $W_c$ ) and a height ( $H_c$ ), the width ( $W_c$ ) approximately the same as the height ( $H_c$ ). That is, in both cases, the channel regions **806** are square-like or, if corner-rounded, circle-like in cross-section profile. In another aspect, the width and height of the channel region need not be the same, such as the case for nanoribbons as described throughout.

**[0153]** In an embodiment, as described throughout, an integrated circuit structure includes non-planar devices such as, but not limited to, a finFET or a tri-gate device with corresponding one or more overlying nanowire structures. In such an embodiment, a corresponding semiconducting channel region is composed of or is formed in a three-dimensional body with one or more discrete nanowire channel portions overlying the three-dimensional body. In one such embodiment, the gate structures surround at least a top surface and a pair of sidewalls of the three-dimensional body, and further surrounds each of the one or more discrete nanowire channel portions.

**[0154]** In an embodiment, the structure of FIGS. **8A-8C** is formed using a pre-spacer-deposition cut gate approach, such as described in association with FIGS. **1A**, **1B**, **2A-2G** and **3I**, and can be fabricated together with associated defect test structures such as described in association with FIGS. **1C-1E**.

**[0155]** In an embodiment, as described throughout, an underlying substrate may be composed of a semiconductor material that can withstand a manufacturing process and in which charge can migrate. In an embodiment, the substrate is a bulk substrate composed of a crystalline silicon, silicon/germanium or germanium layer doped with a charge carrier, such as but not limited to phosphorus, arsenic, boron, gallium or a combination thereof, to form an active region. In one embodiment, the concentration of silicon atoms in a bulk substrate is greater than 97%. In another embodiment, a bulk substrate is composed of an epitaxial layer grown atop a distinct crystalline substrate, e.g. a silicon epitaxial layer grown atop a boron-doped bulk silicon mono-crystalline substrate. A bulk substrate may alternatively be composed of a group III-V material. In an embodiment, a bulk substrate is composed of a group III-V material such as, but not

limited to, gallium nitride, gallium phosphide, gallium arsenide, indium phosphide, indium antimonide, indium gallium arsenide, aluminum gallium arsenide, indium gallium phosphide, or a combination thereof. In one embodiment, a bulk substrate is composed of a group III-V material and the charge-carrier dopant impurity atoms are ones such as, but not limited to, carbon, silicon, germanium, oxygen, sulfur, selenium or tellurium.

**[0156]** Embodiments disclosed herein may be used to manufacture a wide variety of different types of integrated circuits and/or microelectronic devices. Examples of such integrated circuits include, but are not limited to, processors, chipset components, graphics processors, digital signal processors, micro-controllers, and the like. In other embodiments, semiconductor memory may be manufactured. Moreover, the integrated circuits or other microelectronic devices may be used in a wide variety of electronic devices known in the arts. For example, in computer systems (e.g., desktop, laptop, server), cellular phones, personal electronics, etc. The integrated circuits may be coupled with a bus and other components in the systems. For example, a processor may be coupled by one or more buses to a memory, a chipset, etc. Each of the processor, the memory, and the chipset, may potentially be manufactured using the approaches disclosed herein.

**[0157]** FIG. **9** illustrates a computing device **900** in accordance with one implementation of an embodiment of the present disclosure. The computing device **900** houses a board **902**. The board **902** may include a number of components, including but not limited to a processor **904** and at least one communication chip **906**. The processor **904** is physically and electrically coupled to the board **902**. In some implementations the at least one communication chip **906** is also physically and electrically coupled to the board **902**. In further implementations, the communication chip **906** is part of the processor **904**.

**[0158]** Depending on its applications, computing device **900** may include other components that may or may not be physically and electrically coupled to the board **902**. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

**[0159]** The communication chip **906** enables wireless communications for the transfer of data to and from the computing device **900**. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip **906** may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as

any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device **900** may include a plurality of communication chips **906**. For instance, a first communication chip **906** may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip **906** may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0160] The processor **904** of the computing device **900** includes an integrated circuit die packaged within the processor **904**. The integrated circuit die of the processor **904** may include one or more structures, such as integrated circuit structures having pre-spacer-deposition cut gates and associated defect test structures, built in accordance with implementations of embodiments of the present disclosure. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0161] The communication chip **906** also includes an integrated circuit die packaged within the communication chip **906**. The integrated circuit die of the communication chip **906** may include one or more structures, such as integrated circuit structures having pre-spacer-deposition cut gates and associated defect test structures, built in accordance with implementations of embodiments of the present disclosure.

[0162] In further implementations, another component housed within the computing device **900** may contain an integrated circuit die that includes one or structures, such as integrated circuit structures having pre-spacer-deposition cut gates and associated defect test structures, built in accordance with implementations of embodiments of the present disclosure.

[0163] In various implementations, the computing device **900** may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device **900** may be any other electronic device that processes data.

[0164] FIG. 10 illustrates an interposer **1000** that includes one or more embodiments of the present disclosure. The interposer **1000** is an intervening substrate used to bridge a first substrate **1002** to a second substrate **1004**. The first substrate **1002** may be, for instance, an integrated circuit die. The second substrate **1004** may be, for instance, a memory module, a computer motherboard, or another integrated circuit die.

[0165] Generally, the purpose of an interposer **1000** is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer **1000** may couple an integrated circuit die to a ball grid array (BGA) **1006** that can subsequently be coupled to the second substrate **1004**. In some embodiments, the first and second substrates **1002/1004** are attached to opposing sides of the interposer **1000**. In other embodiments, the first and second substrates **1002/1004** are attached to the same side of the interposer **1000**. And in further embodiments, three or more substrates are interconnected by way of the interposer **1000**.

[0166] The interposer **1000** may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic mate-

rial, or a polymer material such as polyimide. In further implementations, the interposer **1000** may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

[0167] The interposer **1000** may include metal interconnects **1008** and vias **1010**, including but not limited to through-silicon vias (TSVs) **1012**. The interposer **1000** may further include embedded devices **1014**, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer **1000**. In accordance with embodiments of the disclosure, apparatuses or processes disclosed herein may be used in the fabrication of interposer **1000** or in the fabrication of components included in the interposer **1000**.

[0168] Thus, embodiments of the present disclosure include integrated circuit structures having pre-spacer-deposition cut gates and associated defect test structures, and methods of fabricating integrated circuit structures having pre-spacer-deposition cut gates and associated defect test structures.

[0169] The above description of illustrated implementations of embodiments of the disclosure, including what is described in the Abstract, is not intended to be exhaustive or to limit the disclosure to the precise forms disclosed. While specific implementations of, and examples for, the disclosure are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the disclosure, as those skilled in the relevant art will recognize.

[0170] These modifications may be made to the disclosure in light of the above detailed description. The terms used in the following claims should not be construed to limit the disclosure to the specific implementations disclosed in the specification and the claims. Rather, the scope of the disclosure is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

[0171] Example embodiment 1: An integrated circuit structure includes a first fin and a second fin. A first gate stack is over the first fin, and a second gate stack is over the second fin. An end of the second gate stack is spaced apart from an end of the first gate stack by a gap. The integrated circuit structure also includes a dielectric structure having a first portion forming a gate spacer along sidewalls of the first gate stack, a second portion forming a gate spacer along sidewalls of the second gate stack, and a third portion completely filling the gap, the third portion continuous with the first and second portions. The integrated circuit structure also includes an array having a periodic arrangement of alternating floating and grounded conductive trench contacts along a direction parallel with the first gate stack and the second gate stack.

[0172] Example embodiment 2: The integrated circuit structure of example embodiment 1, wherein the array having the periodic arrangement of alternating floating and grounded conductive trench contacts is a test structure configured for voltage contrast (VC) measurements

[0173] Example embodiment 3: The integrated circuit structure of example embodiment 1 or 2, further including a first pair of epitaxial source or drain structures at first and second ends of the first fin, and a second pair of epitaxial source or drain structures at first and second ends of the second fin.

[0174] Example embodiment 4: The integrated circuit structure of example embodiment 3, further including a first pair of conductive contacts on the first pair of epitaxial source or drain structures; and a second pair of conductive contacts on the second pair of epitaxial source or drain structures.

[0175] Example embodiment 5: The integrated circuit structure of example embodiment 3 or 4, wherein the first and second pairs of epitaxial source or drain structures are first and second pairs of non-discrete epitaxial source or drain structures.

[0176] Example embodiment 6: An integrated circuit structure includes a first vertical arrangement of horizontal nanowires and a second vertical arrangement of horizontal nanowires. A first gate stack is over the first vertical arrangement of horizontal nanowires, and a second gate stack is over the second vertical arrangement of horizontal nanowires. An end of the second gate stack is spaced apart from an end of the first gate stack by a gap. The integrated circuit structure also includes a dielectric structure having a first portion forming a gate spacer along sidewalls of the first gate stack, a second portion forming a gate spacer along sidewalls of the second gate stack, and a third portion completely filling the gap, the third portion continuous with the first and second portions. The integrated circuit structure also includes an array having a periodic arrangement of alternating floating and grounded conductive trench contacts along a direction parallel with the first gate stack and the second gate stack.

[0177] Example embodiment 7: The integrated circuit structure of example embodiment 6, wherein the array having the periodic arrangement of alternating floating and grounded conductive trench contacts is a test structure configured for voltage contrast (VC) measurements.

[0178] Example embodiment 8: The integrated circuit structure of example embodiment 6 or 7, further including a first pair of epitaxial source or drain structures at first and second ends of the first vertical arrangement of horizontal nanowires, and a second pair of epitaxial source or drain structures at first and second ends of the second vertical arrangement of horizontal nanowires.

[0179] Example embodiment 9: The integrated circuit structure of example embodiment 8, further including a first pair of conductive contacts on the first pair of epitaxial source or drain structures; and a second pair of conductive contacts on the second pair of epitaxial source or drain structures.

[0180] Example embodiment 10: The integrated circuit structure of example embodiment 8 or 9, wherein the first and second pairs of epitaxial source or drain structures are first and second pairs of non-discrete epitaxial source or drain structures.

[0181] Example embodiment 11: A computing device includes a board, and a component coupled to the board. The component includes an integrated circuit structure including a first fin or vertical arrangement of horizontal nanowires and a second fin or vertical arrangement of horizontal nanowires. A first gate stack is over the first fin or vertical

arrangement of horizontal nanowires, and a second gate stack is over the second fin or vertical arrangement of horizontal nanowires. An end of the second gate stack is spaced apart from an end of the first gate stack by a gap. The integrated circuit structure also includes a dielectric structure having a first portion forming a gate spacer along sidewalls of the first gate stack, a second portion forming a gate spacer along sidewalls of the second gate stack, and a third portion completely filling the gap, the third portion continuous with the first and second portions. The integrated circuit structure also includes an array having a periodic arrangement of alternating floating and grounded conductive trench contacts along a direction parallel with the first gate stack and the second gate stack.

[0182] Example embodiment 12: The computing device of example embodiment 11, including the first fin and the second fin.

[0183] Example embodiment 13: The computing device of example embodiment 11 or 12, including the first vertical arrangement of horizontal nanowires and the second vertical arrangement of horizontal nanowires.

[0184] Example embodiment 14: The computing device of example embodiment 11, 12 or 13, further including a memory coupled to the board.

[0185] Example embodiment 15: The computing device of example embodiment 11, 12, 13 or 14, further including a communication chip coupled to the board.

[0186] Example embodiment 16: The computing device of example embodiment 11, 12, 13, 14 or 15, further including a battery coupled to the board.

[0187] Example embodiment 17: The computing device of example embodiment 11, 12, 13, 14, 15 or 16, further including a camera coupled to the board.

[0188] Example embodiment 18: The computing device of example embodiment 11, 12, 13, 14, 15, 16 or 17, further including a display coupled to the board.

[0189] Example embodiment 19: The computing device of example embodiment 11, 12, 13, 14, 15, 16, 17 or 18, wherein the component is a packaged integrated circuit die.

[0190] Example embodiment 20: The computing device of example embodiment 11, 12, 13, 14, 15, 16, 17, 18 or 19, wherein the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor.

What is claimed is:

1. An integrated circuit structure, comprising:

- a first fin;
- a second fin;
- a first gate stack over the first fin;
- a second gate stack over the second fin, an end of the second gate stack spaced apart from an end of the first gate stack by a gap;
- a dielectric structure comprising a first portion forming a gate spacer along sidewalls of the first gate stack, a second portion forming a gate spacer along sidewalls of the second gate stack, and a third portion completely filling the gap, the third portion continuous with the first and second portions; and
- an array having a periodic arrangement of alternating floating and grounded conductive trench contacts along a direction parallel with the first gate stack and the second gate stack.

2. The integrated circuit structure of claim 1, wherein the array having the periodic arrangement of alternating floating

and grounded conductive trench contacts is a test structure configured for voltage contrast (VC) measurements.

3. The integrated circuit structure of claim 1, further comprising:

- a first pair of epitaxial source or drain structures at first and second ends of the first fin; and
- a second pair of epitaxial source or drain structures at first and second ends of the second fin.

4. The integrated circuit structure of claim 3, further comprising:

- a first pair of conductive trench contacts on the first pair of epitaxial source or drain structures; and
- a second pair of conductive trench contacts on the second pair of epitaxial source or drain structures.

5. The integrated circuit structure of claim 3, wherein the first and second pairs of epitaxial source or drain structures are first and second pairs of non-discrete epitaxial source or drain structures.

6. An integrated circuit structure, comprising:

- a first vertical arrangement of horizontal nanowires;
- a second vertical arrangement of horizontal nanowires;
- a first gate stack over the first vertical arrangement of horizontal nanowires;
- a second gate stack over the second vertical arrangement of horizontal nanowires, an end of the second gate stack spaced apart from an end of the first gate stack by a gap;
- a dielectric structure comprising a first portion forming a gate spacer along sidewalls of the first gate stack, a second portion forming a gate spacer along sidewalls of the second gate stack, and a third portion completely filling the gap, the third portion continuous with the first and second portions; and

an array having a periodic arrangement of alternating floating and grounded conductive trench contacts along a direction parallel with the first gate stack and the second gate stack.

7. The integrated circuit structure of claim 6, wherein the array having the periodic arrangement of alternating floating and grounded conductive trench contacts is a test structure configured for voltage contrast (VC) measurements.

8. The integrated circuit structure of claim 6, further comprising:

- a first pair of epitaxial source or drain structures at first and second ends of the first vertical arrangement of horizontal nanowires; and
- a second pair of epitaxial source or drain structures at first and second ends of the second vertical arrangement of horizontal nanowires.

9. The integrated circuit structure of claim 8, further comprising:

- a first pair of conductive trench contacts on the first pair of epitaxial source or drain structures; and
- a second pair of conductive trench contacts on the second pair of epitaxial source or drain structures.

10. The integrated circuit structure of claim 8, wherein the first and second pairs of epitaxial source or drain structures are first and second pairs of non-discrete epitaxial source or drain structures.

11. A computing device, comprising:

a board; and

a component coupled to the board, the component including an integrated circuit structure, comprising:

a first fin or vertical arrangement of horizontal nanowires;

a second fin or vertical arrangement of horizontal nanowires;

a first gate stack over the first fin or vertical arrangement of horizontal nanowires;

a second gate stack over the second fin or vertical arrangement of horizontal nanowires, an end of the second gate stack spaced apart from an end of the first gate stack by a gap;

a dielectric structure comprising a first portion forming a gate spacer along sidewalls of the first gate stack, a second portion forming a gate spacer along sidewalls of the second gate stack, and a third portion completely filling the gap, the third portion continuous with the first and second portions; and

an array having an arrangement of alternating electrically isolated conductive trench contacts and conductive trench contacts coupled to ground, the alternating trench contacts along a direction parallel with the first gate stack and the second gate stack.

12. The computing device of claim 11, comprising the first fin and the second fin.

13. The computing device of claim 11, comprising the first vertical arrangement of horizontal nanowires and the second vertical arrangement of horizontal nanowires.

14. The computing device of claim 11, further comprising:

a memory coupled to the board.

15. The computing device of claim 11, further comprising:

a communication chip coupled to the board.

16. The computing device of claim 11, further comprising:

a battery coupled to the board.

17. The computing device of claim 11, further comprising:

a camera coupled to the board.

18. The computing device of claim 11, further comprising:

a display coupled to the board.

19. The computing device of claim 11, wherein the component is a packaged integrated circuit die.

20. The computing device of claim 11, wherein the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor.

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