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(54) **SEMICONDUCTOR DEVICES AND METHODS OF FABRICATION THEREOF**

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Publication Classification

(51) **Int. Cl.**

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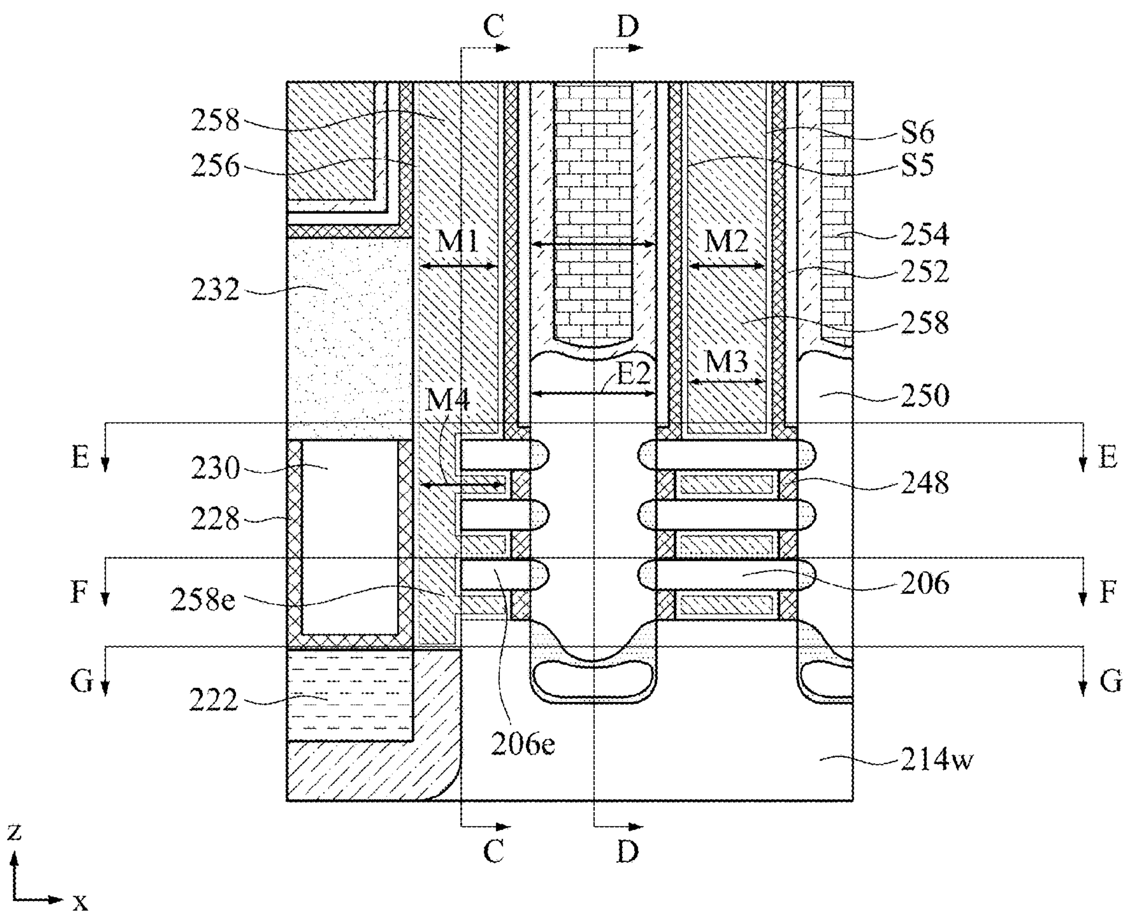
H10D 64/01	(2025.01)
H10D 84/01	(2025.01)
H10D 84/03	(2025.01)
H10D 84/83	(2025.01)

(52) **U.S. Cl.**

CPC ***H10D 30/6735*** (2025.01); ***H01L 21/3065*** (2013.01); ***H10D 62/121*** (2025.01); ***H10D 64/017*** (2025.01); ***H10D 84/014*** (2025.01); ***H10D 84/038*** (2025.01); ***H10D 84/83*** (2025.01)

(57) **ABSTRACT**

A cyclic process including an etching process, a passivation process, and a pumping out process is provided to prevent over etching of the sacrificial gate electrode, particularly when near a high-k dielectric feature. The cyclic process solves the problems of failed gate electrode layer at an end of channel region and enlarges filling windows for replacement gate structures, thus improving channel control. Compared to state-of-art solutions, embodiments of the present disclosure also enlarge volume of source/drain regions, thus improving device performance.



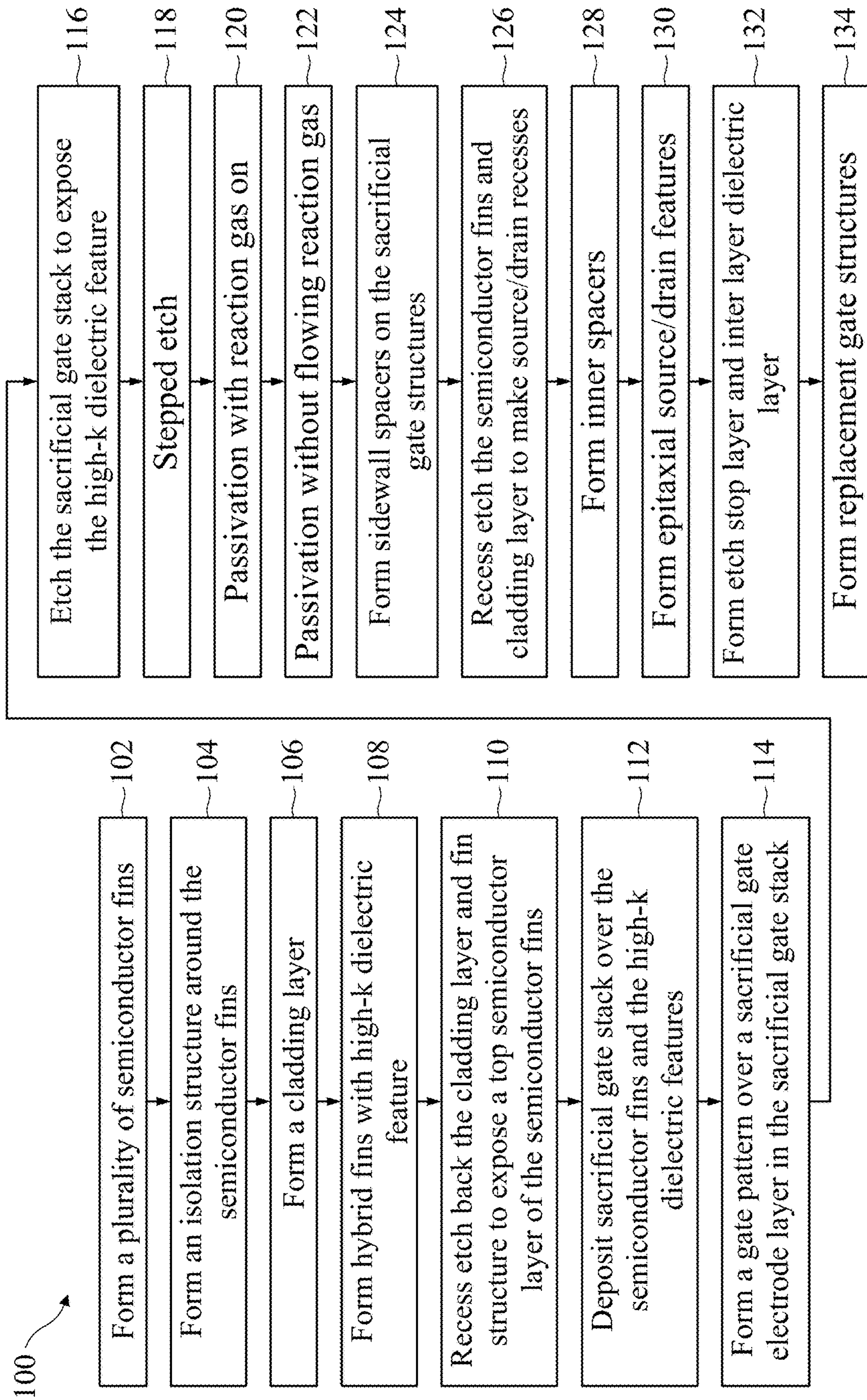

100
Form a plurality of semiconductor fins
102
Form an isolation structure around the semiconductor fins
104
Form a cladding layer
106
Form hybrid fins with high-k dielectric feature
108
Recess etch back the cladding layer and fin structure to expose a top semiconductor layer of the semiconductor fins
110
Deposit sacrificial gate stack over the semiconductor fins and the high-k dielectric features
112
Form a gate pattern over a sacrificial gate electrode layer in the sacrificial gate stack
114
Etch the sacrificial gate stack to expose the high-k dielectric feature
116
Stepped etch
118
Passivation with reaction gas on
120
Passivation without flowing reaction gas
122
Form sidewall spacers on the sacrificial gate structures
124
Recess etch the semiconductor fins and cladding layer to make source/drain recesses
126
Form inner spacers
128
Form epitaxial source/drain features
130
Form etch stop layer and inter layer dielectric layer
132
Form replacement gate structures
134

FIG. 1

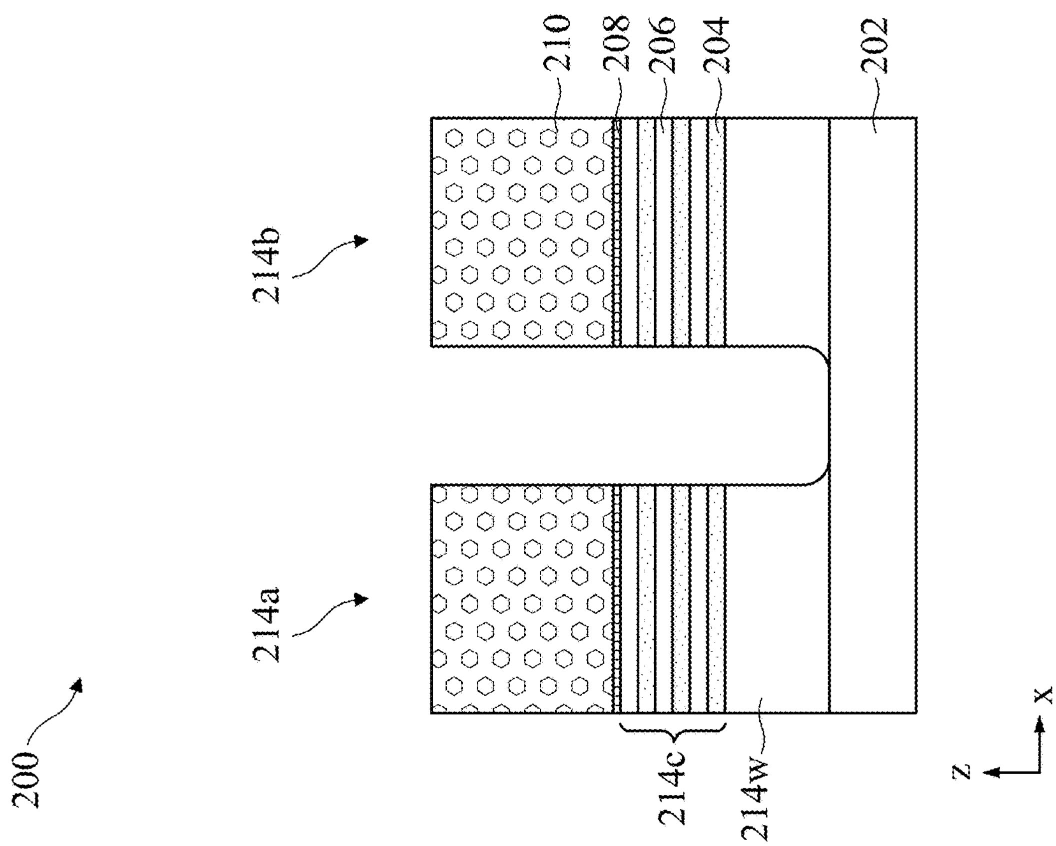

200
214a
214b
210
208
206
204
202
214c
214w
z
x

FIG. 2B

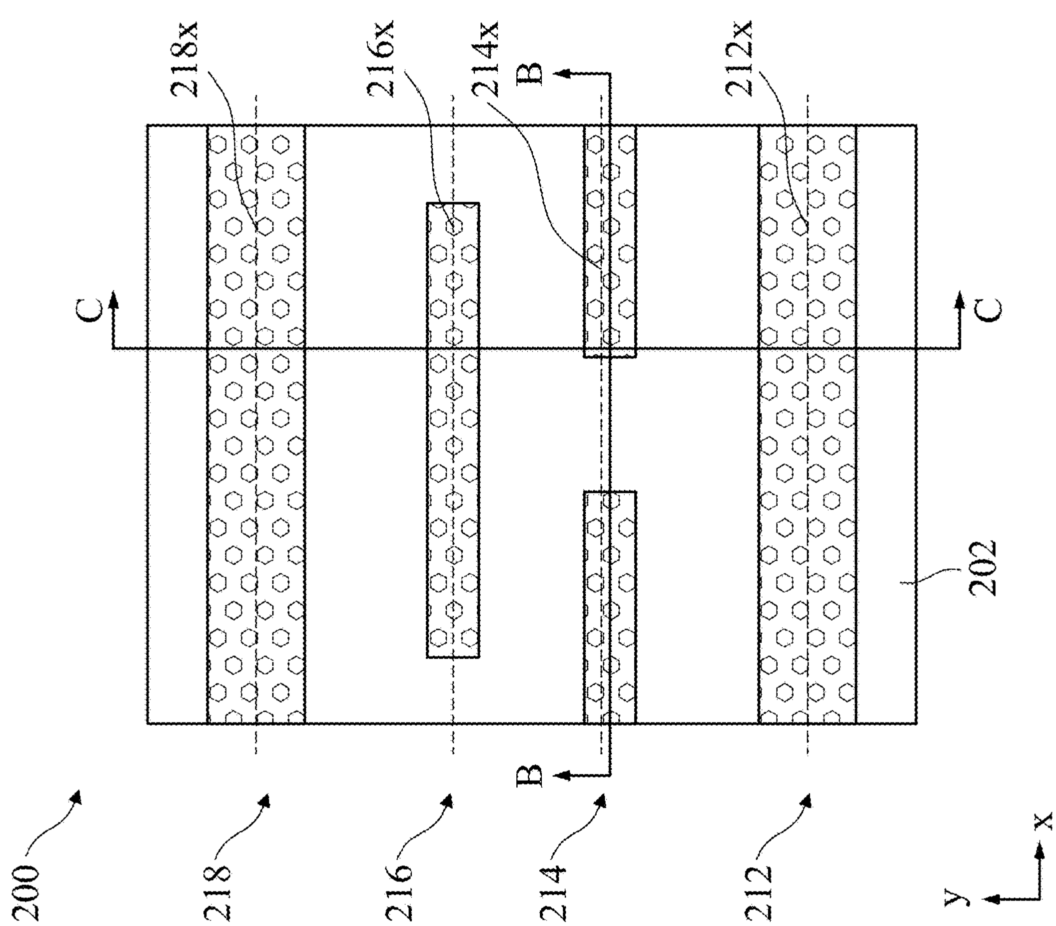

200
218
216
214
212
218x
216x
214x
212x
B
B
C
C
202
y
x

FIG. 2A

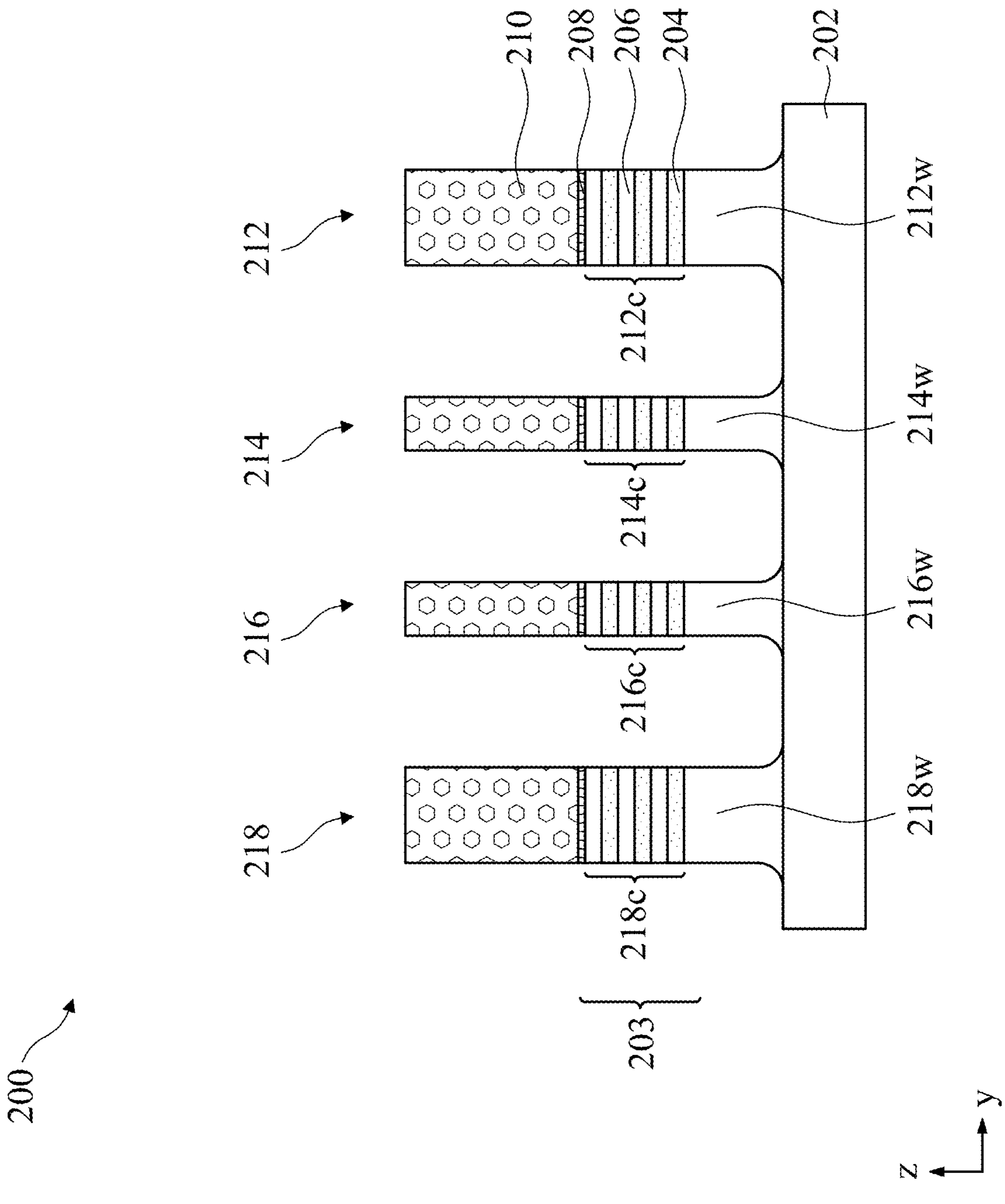

200
203
202
204
206
208
210
212
214
216
218
212w
214w
216w
218w
212c
214c
216c
218c
y
z

FIG. 2C

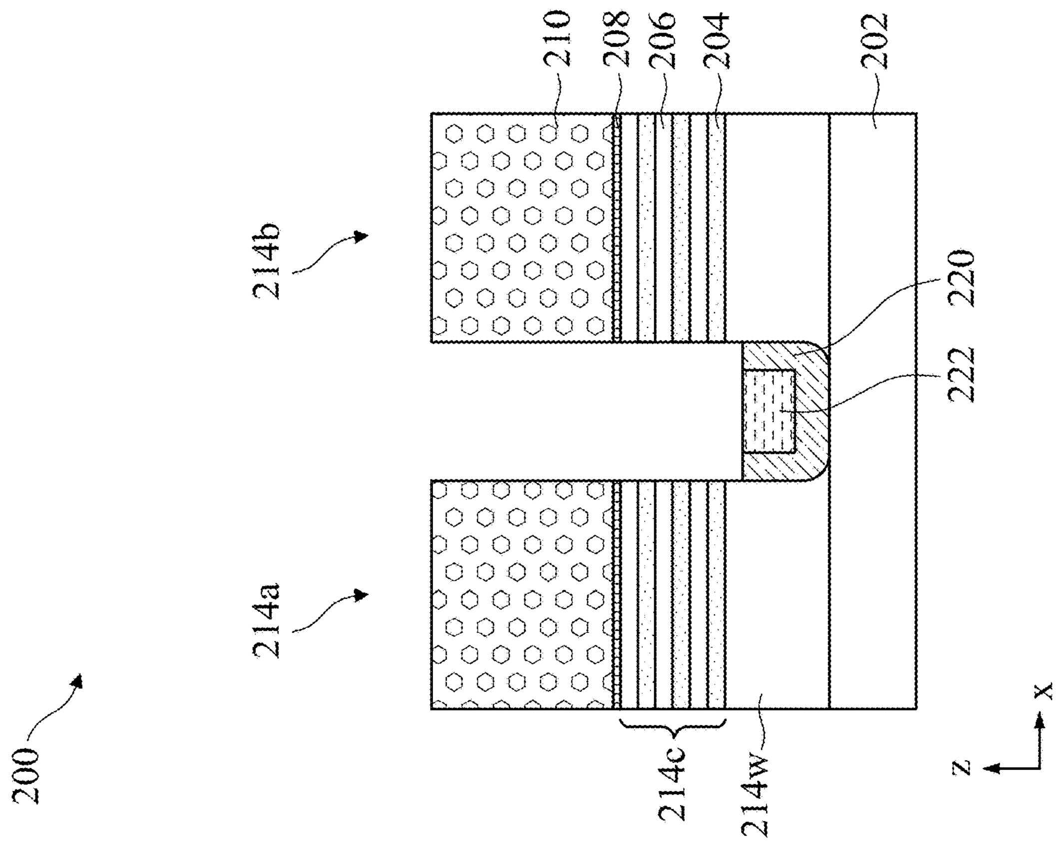

200
214a
214b
210
208
206
204
202
220
222
214c
214w
z
x

FIG. 3B

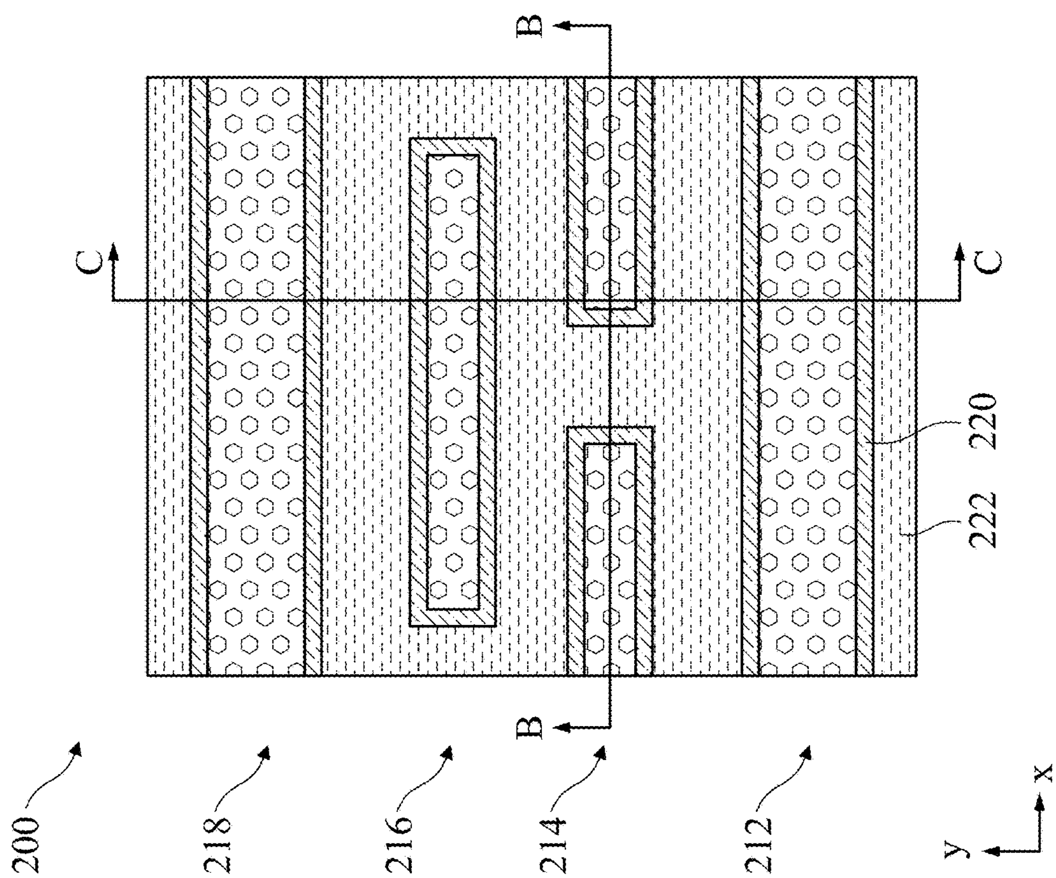

200
218
216
214
212
C
C
B
B
220
222
y
x

FIG. 3A

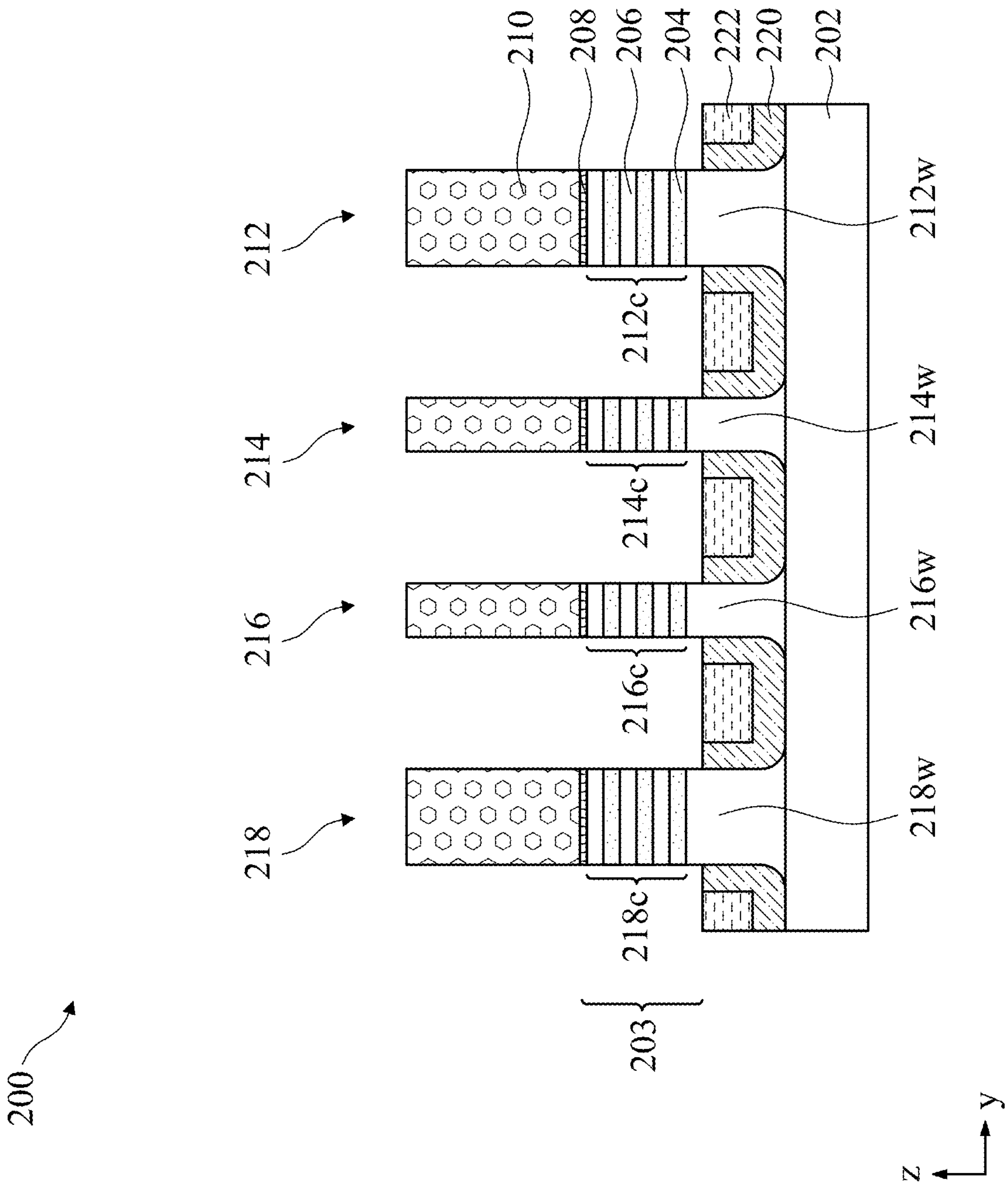

200
203
210
208
206
204
222
220
202
212
214
216
218
212c
214c
216c
218c
212w
214w
216w
218w
z
y

FIG. 3C

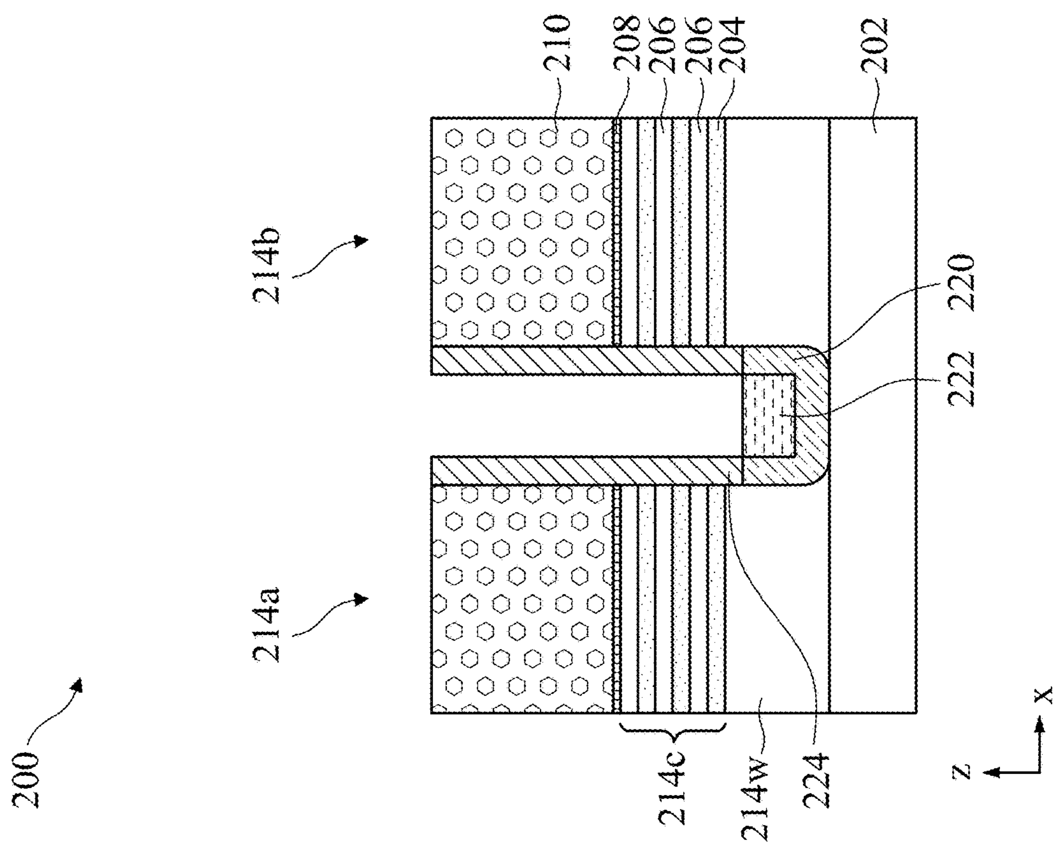

200
214a
214b
210
208
206
206
204
202
220
222
224
214c
214w
z
x

FIG. 4B

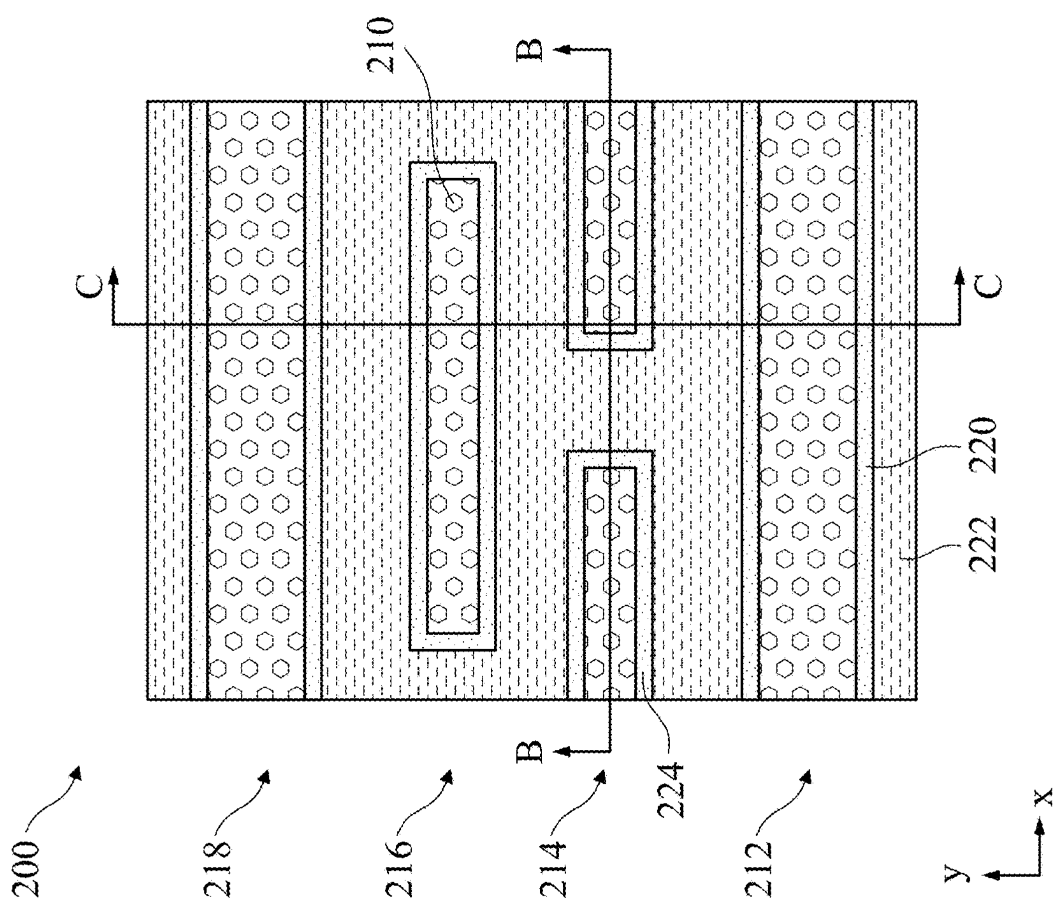

200
218
216
214
212
224
210
220
222
B
C
y
x

FIG. 4A

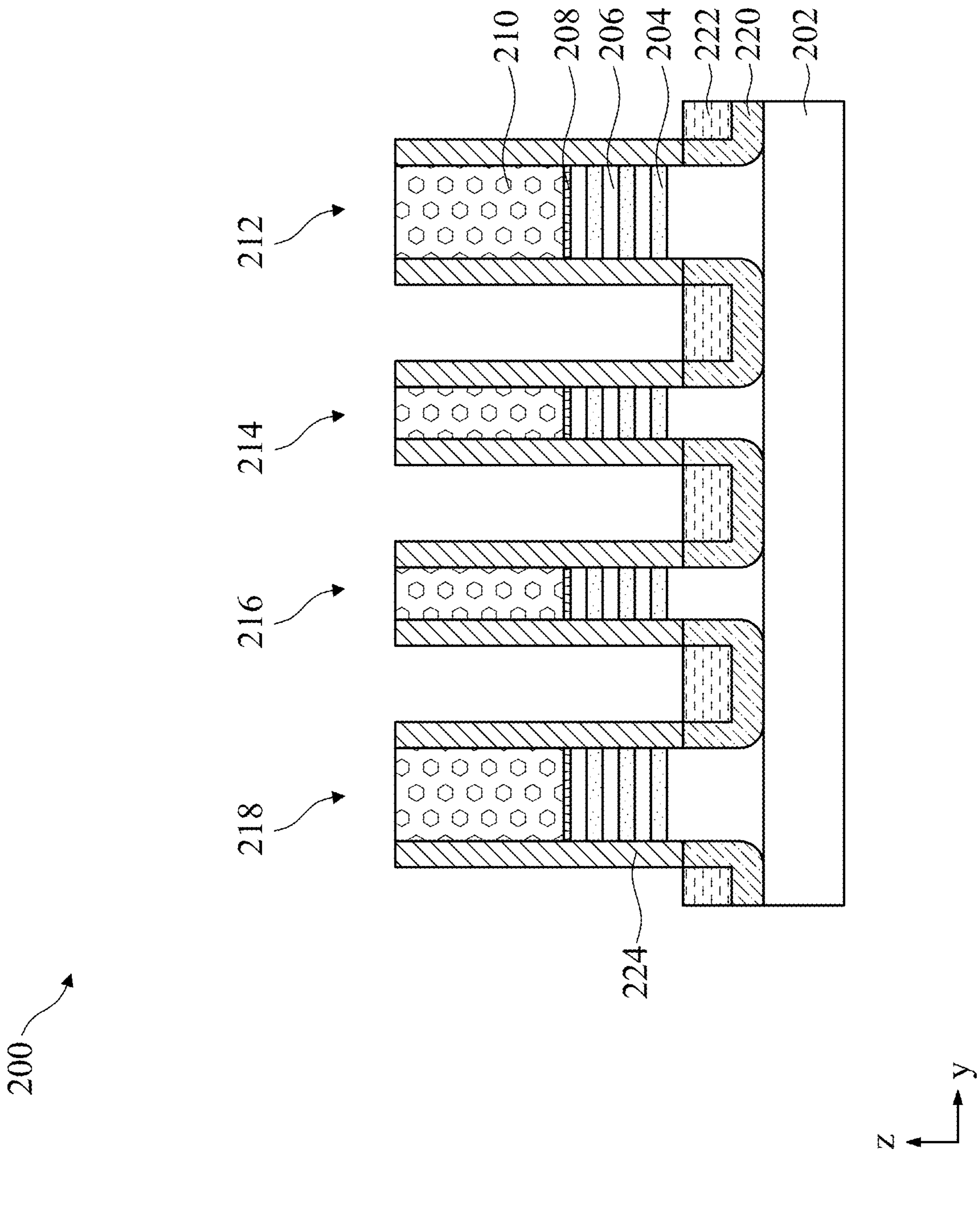


FIG. 4C

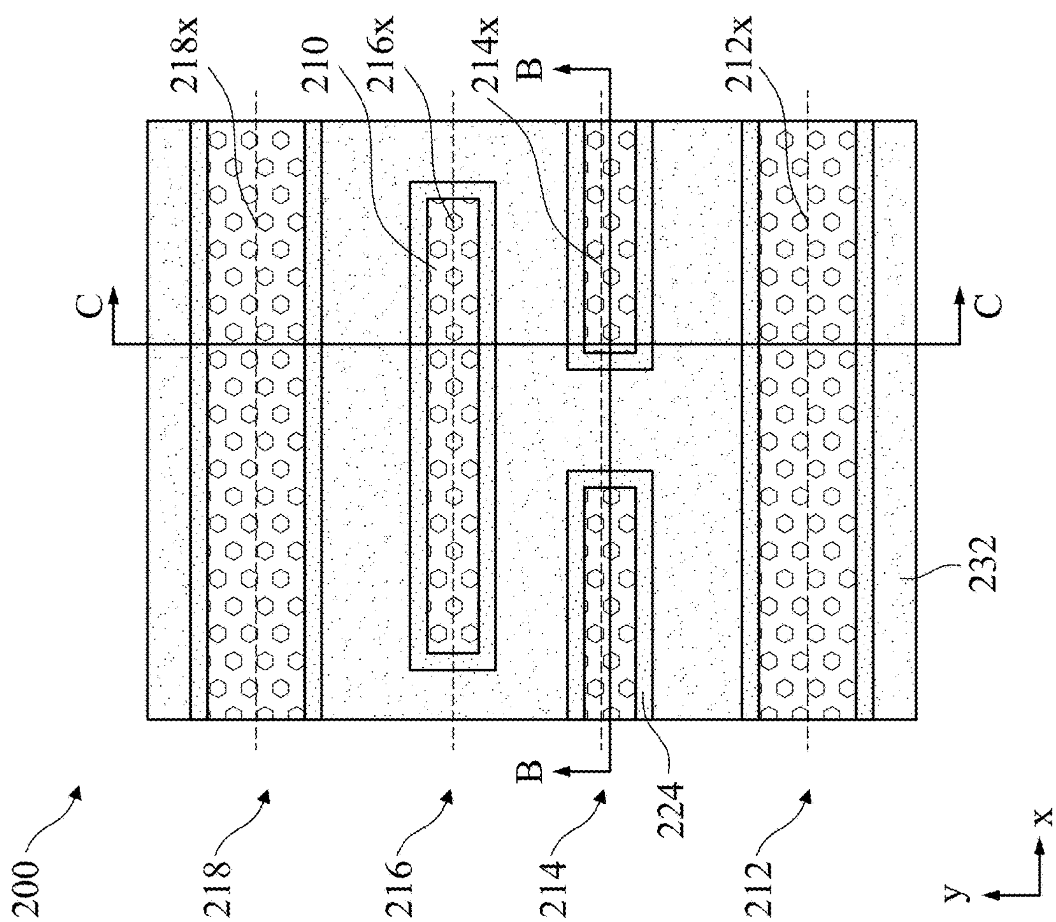

200
218
216
214
212
218x
210
216x
214x
212x
B
B
C
C
224
232
y
x

FIG. 5A

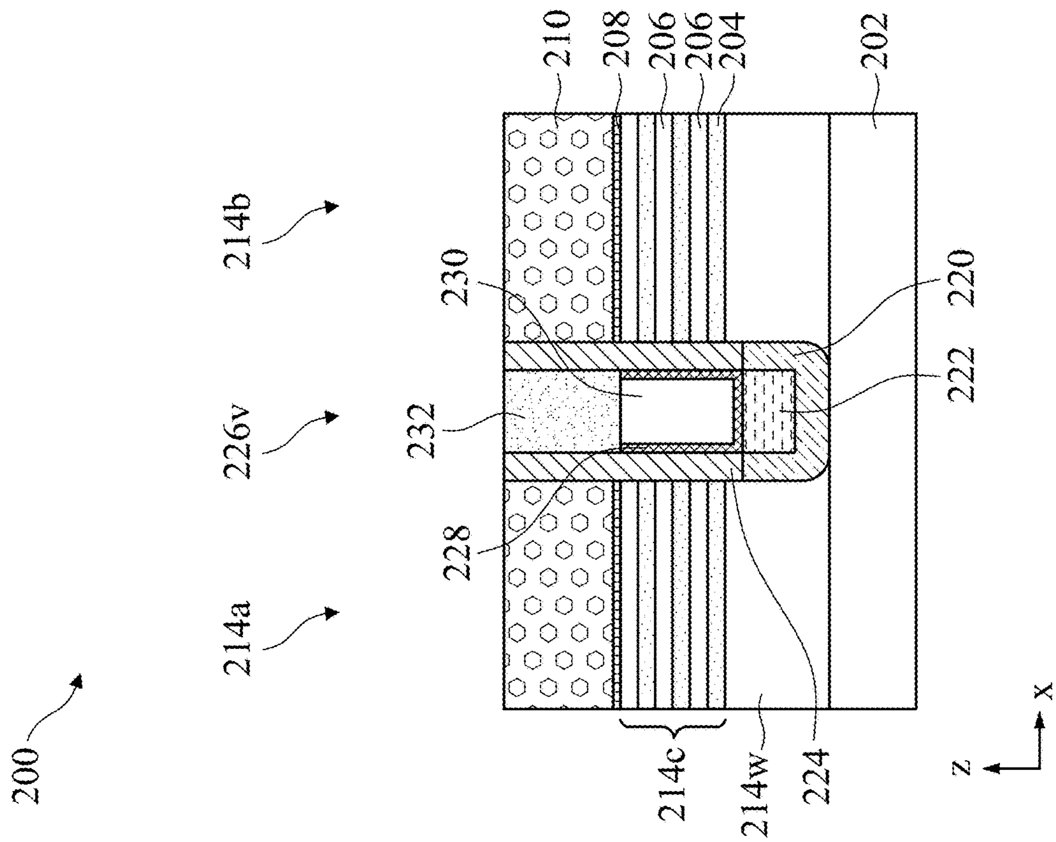

200
214a
226v
214b
210
208
206
206
204
202
230
220
222
232
228
224
214c
214w
z
x

FIG. 5B

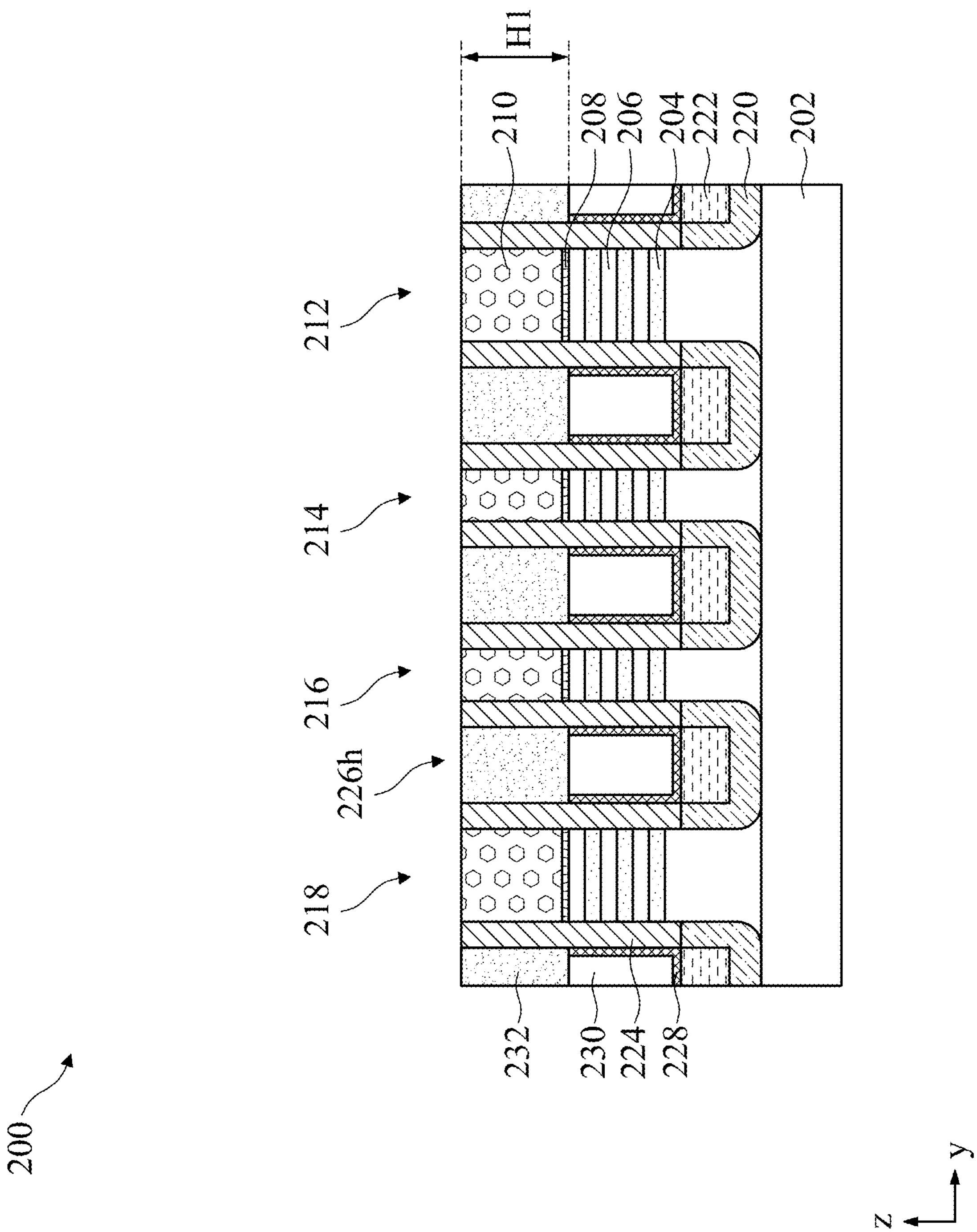

200
212
214
216
218
226h
H1
210
208
206
204
222
220
202
232
230
224
228
z
y

FIG. 5C

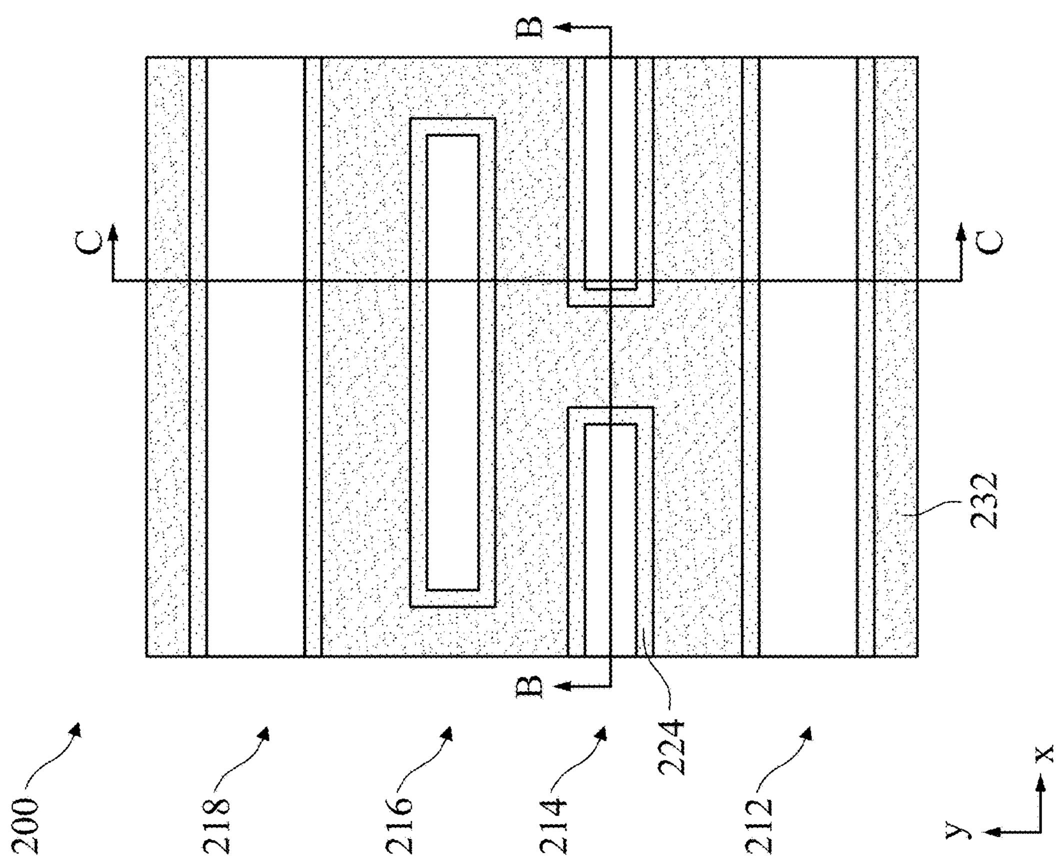

200
218
216
214
224
212
C
C
B
B
232
y
x

FIG. 6A

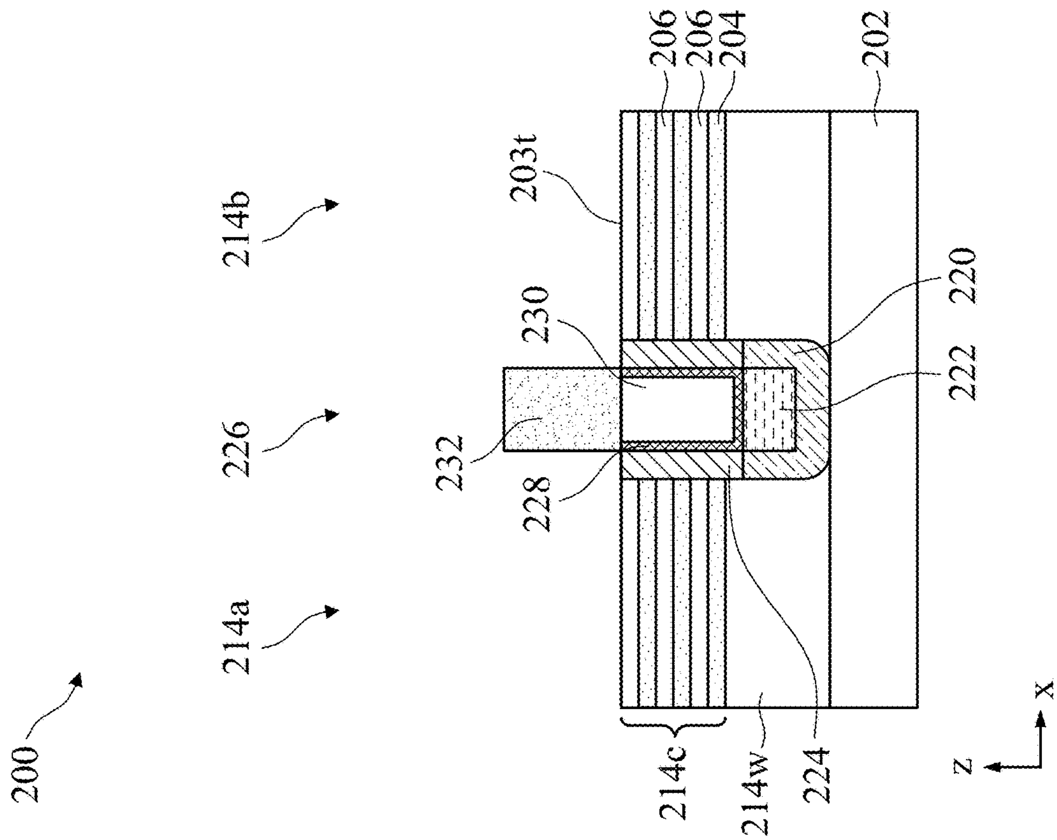

200
214a
226
214b
206
206
204
202
203t
230
232
228
220
222
224
214c
214w
z
x

FIG. 6B

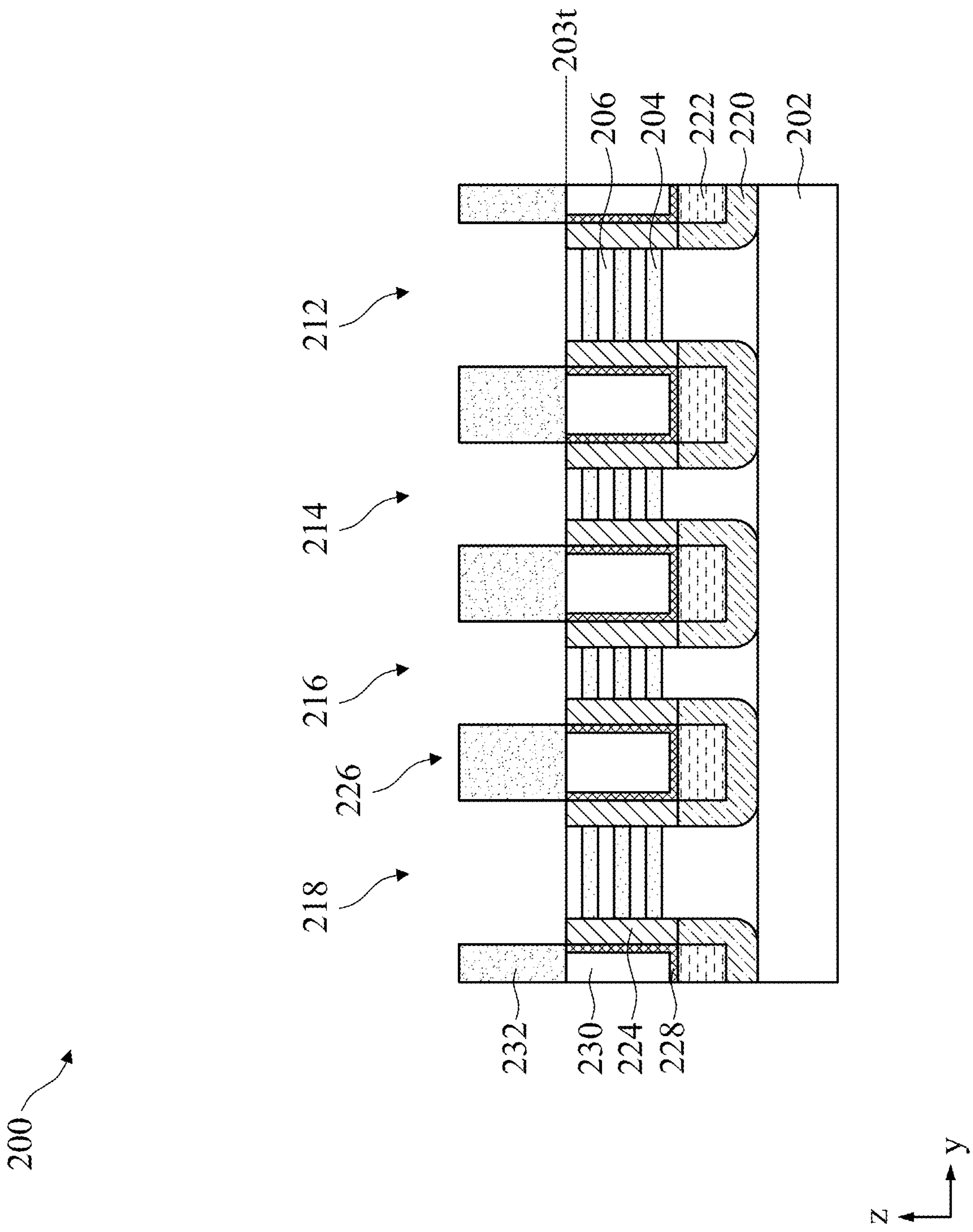

200
203t
206
204
222
220
202
212
214
216
226
218
232
230
224
228
z
y

FIG. 6C

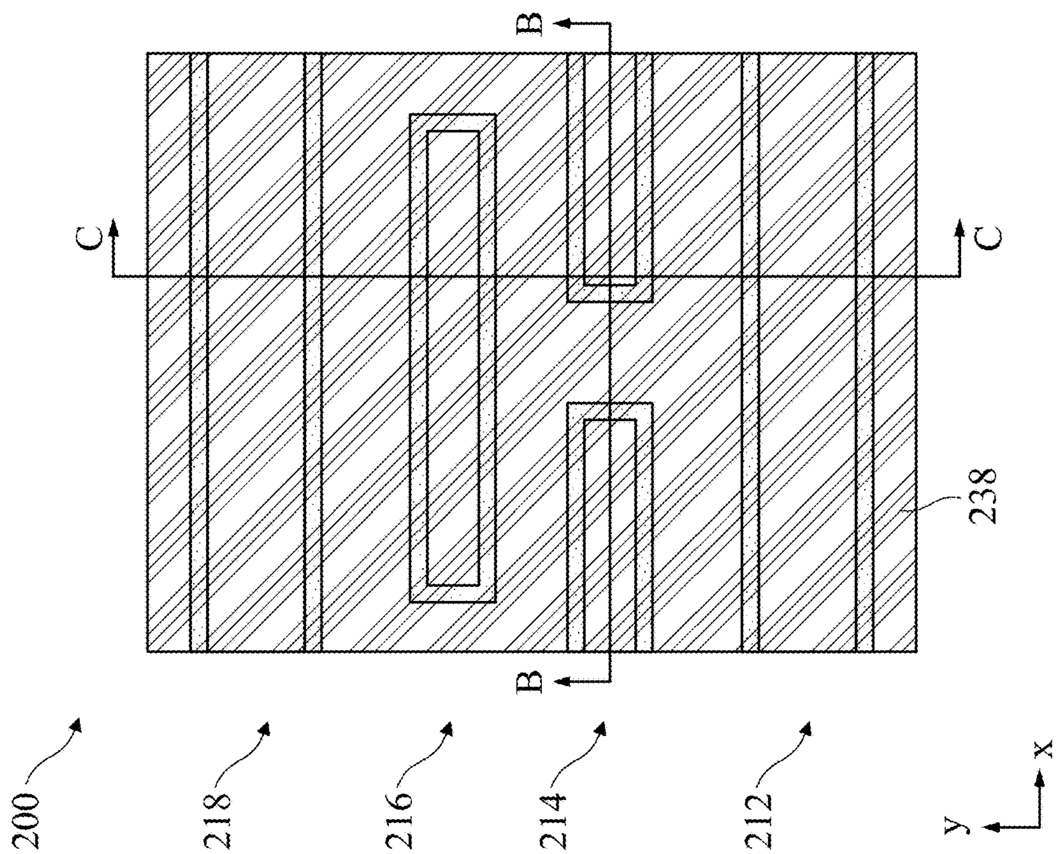

200
218
216
214
212
B
B
C
C
238
y
x

FIG. 7A

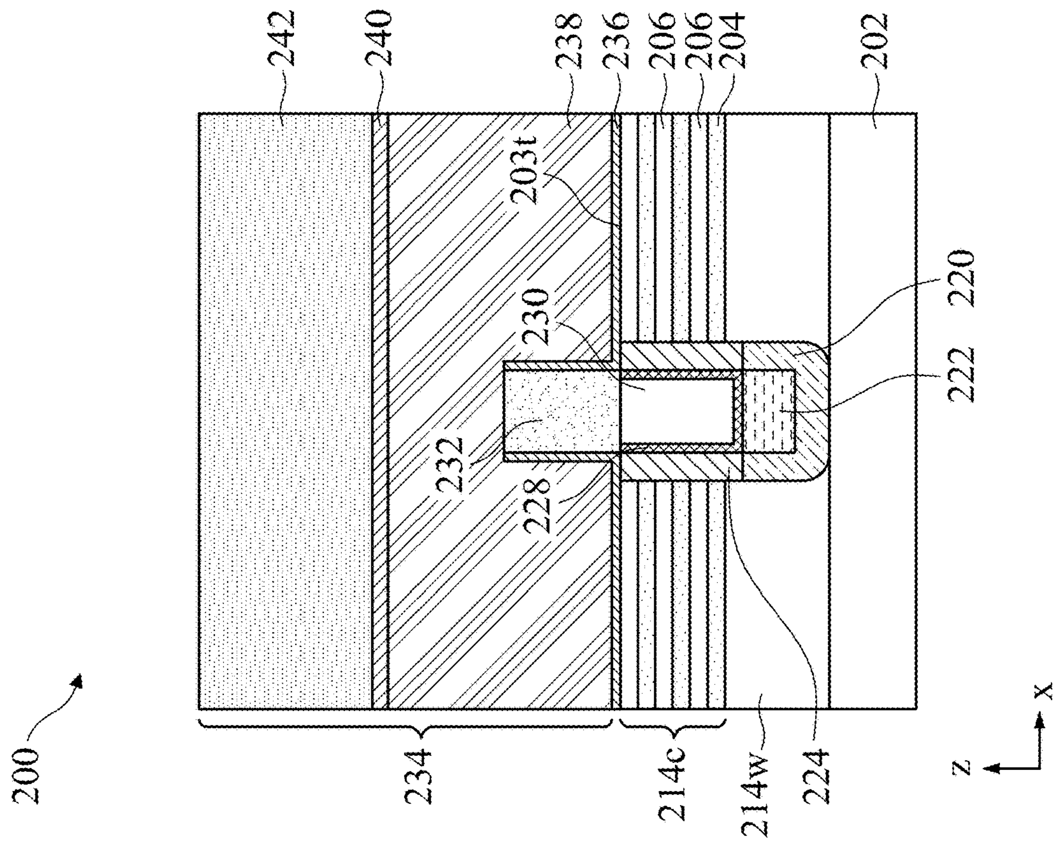

200
242
240
238
236
206
206
204
202
203t
230
232
228
220
222
234
214c
214w
224
z
x

FIG. 7B

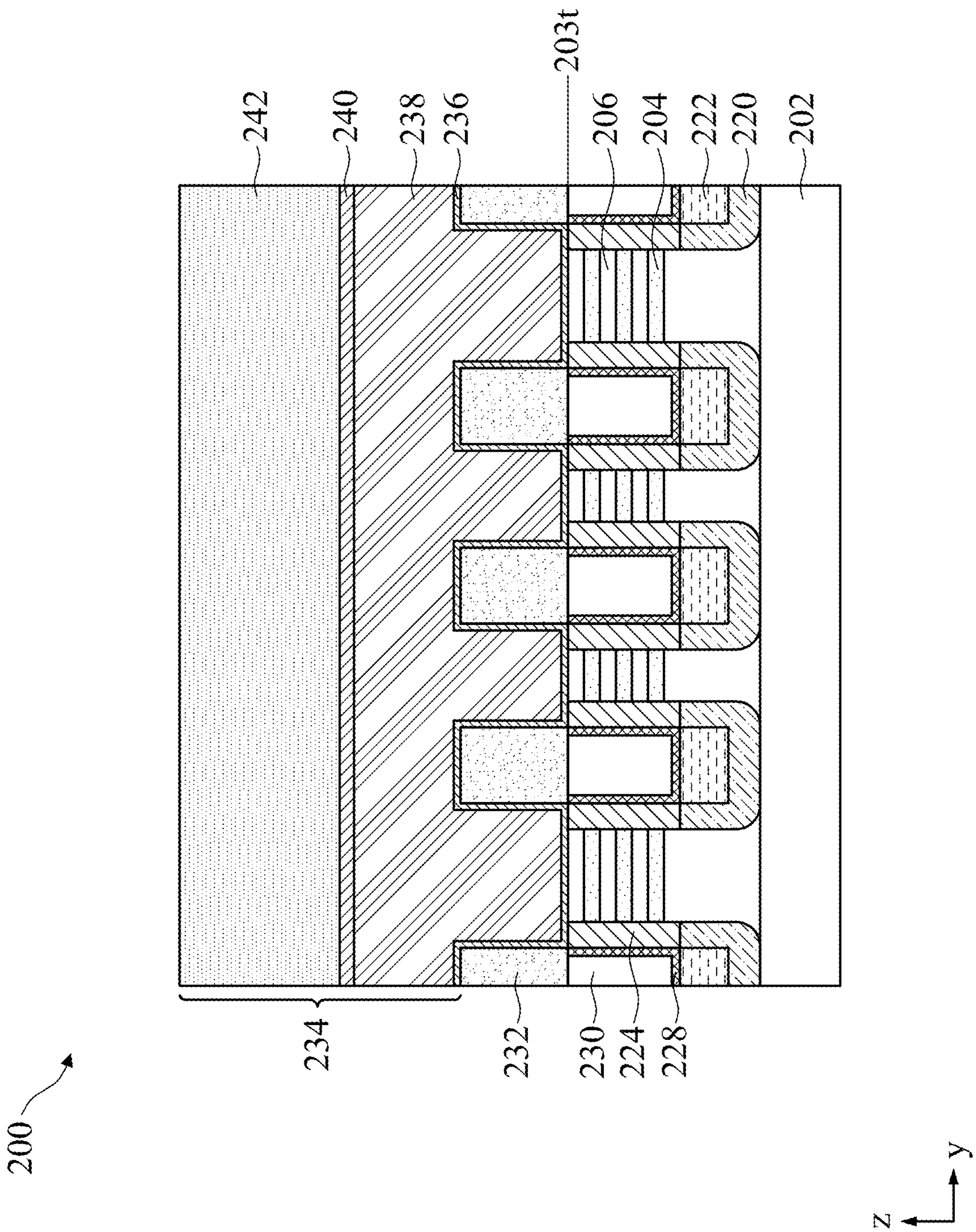

200
203t
242
240
238
236
206
204
222
220
202
234
232
230
224
228
z
y

FIG. 7C

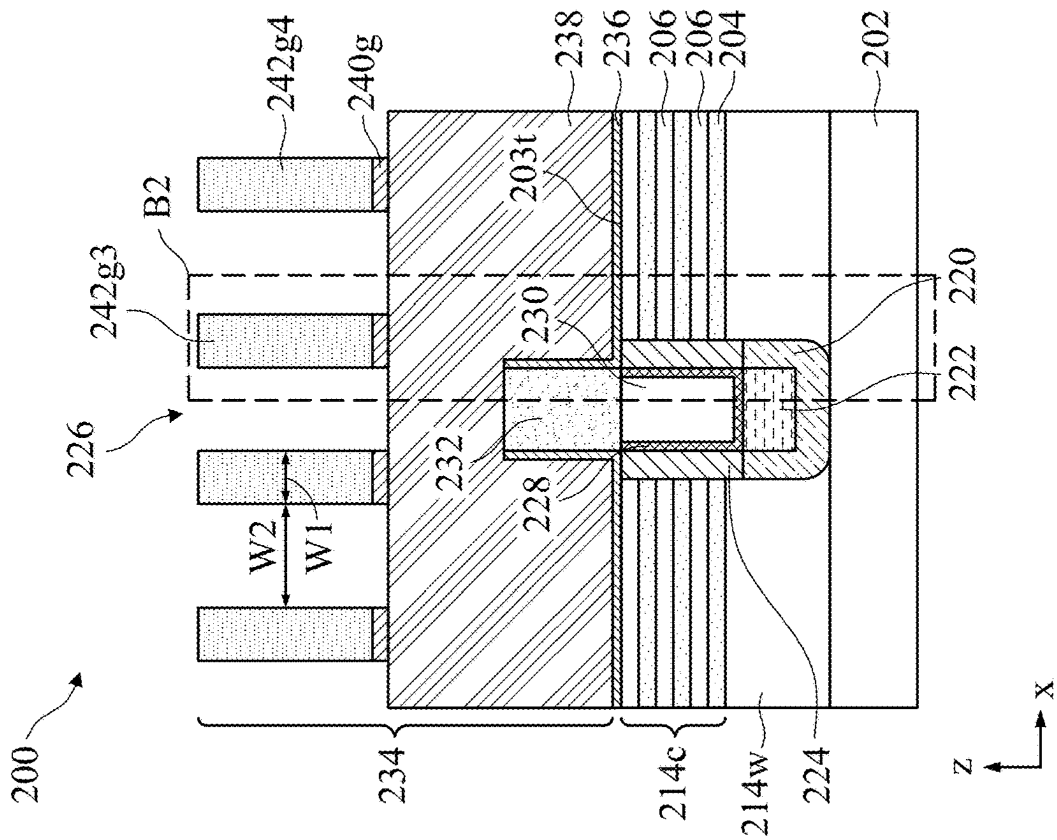

200
226
242g4
240g
242g3
B2
W2
W1
238
236
206
206
204
202
203t
230
232
228
220
222
224
234
214c
214w
z
x

FIG. 8B

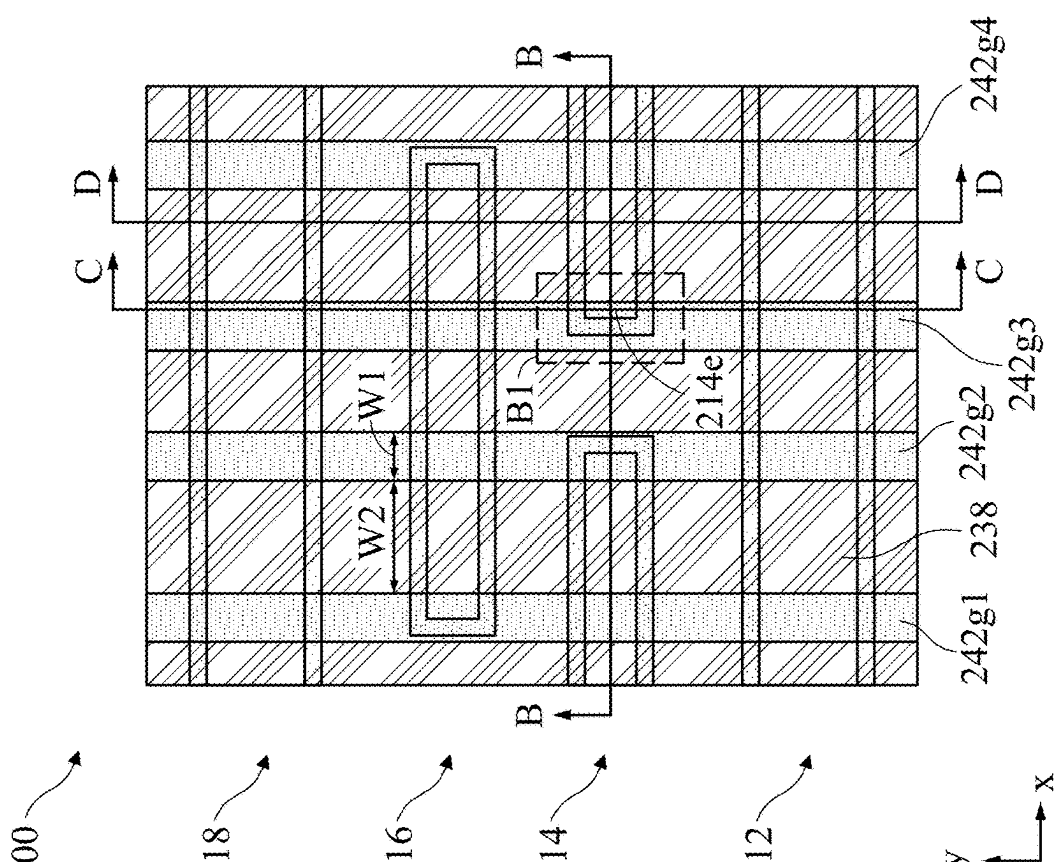

200
218
216
214
212
B
B
D
D
C
C
W1
W2
B1
214e
242g4
242g3
242g2
238
242g1
y
x

FIG. 8A

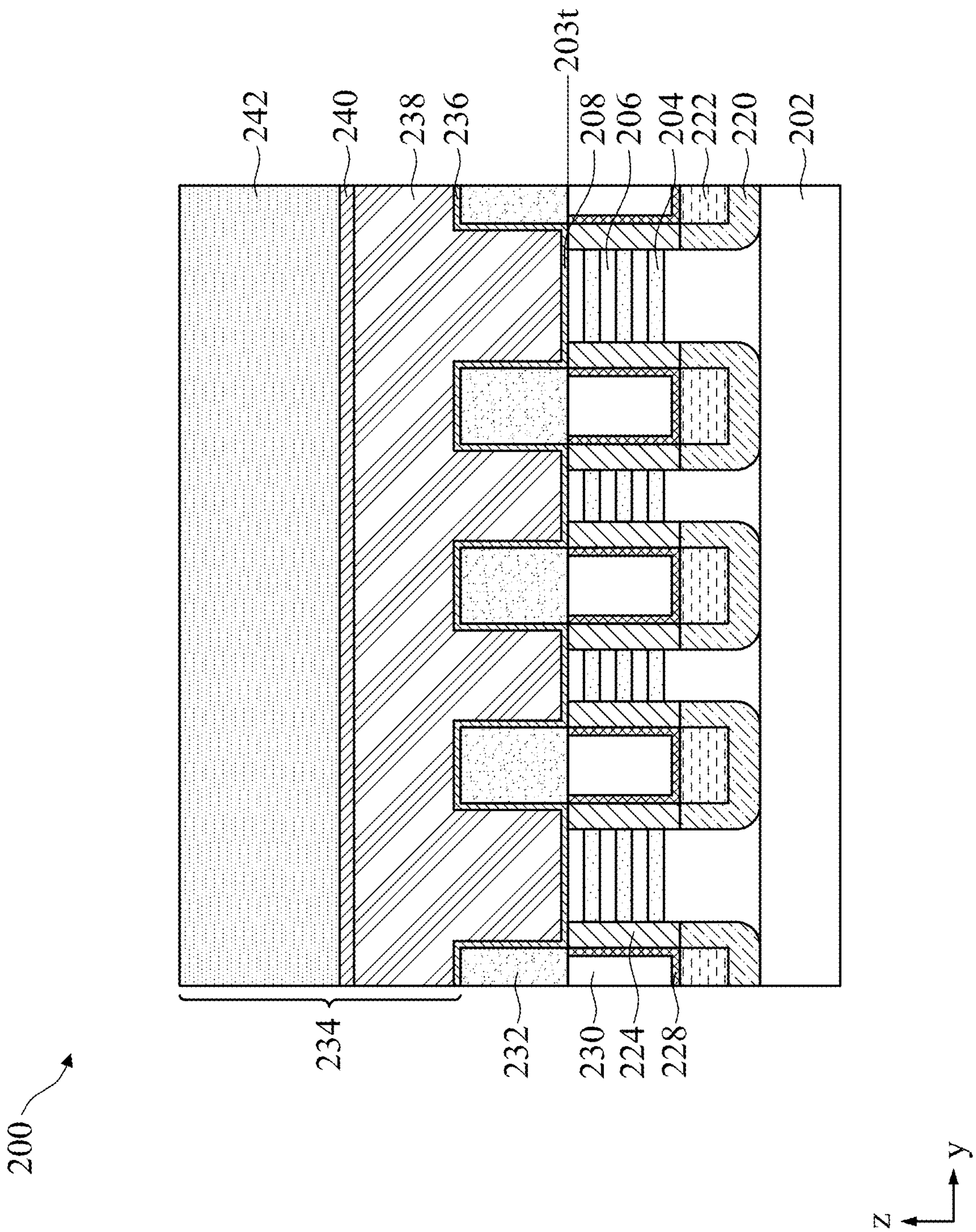

200
242
240
238
236
203t
208
206
204
222
220
202
234
232
230
224
228
z
y

FIG. 8C

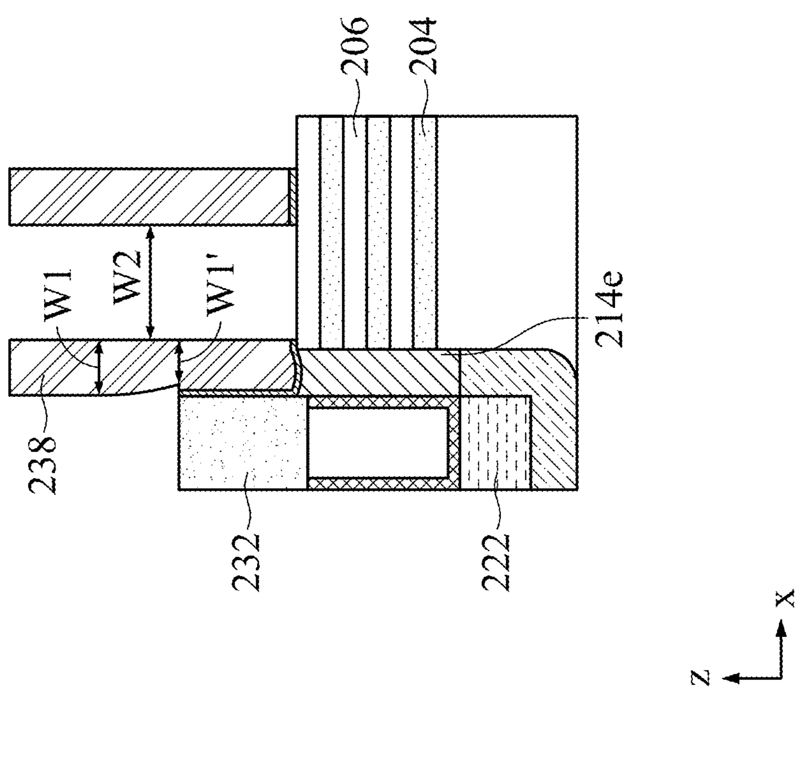


FIG. 8D

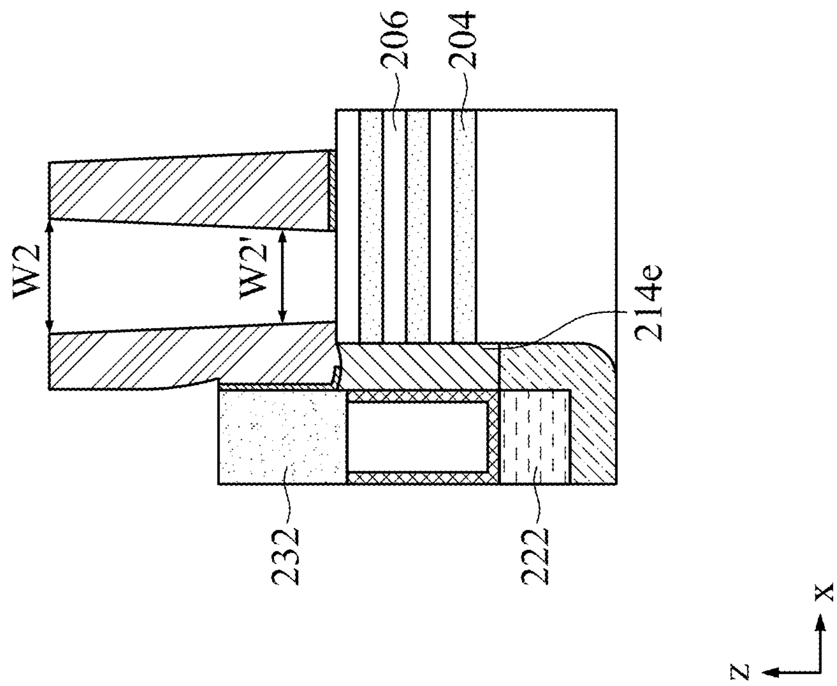


FIG. 8E

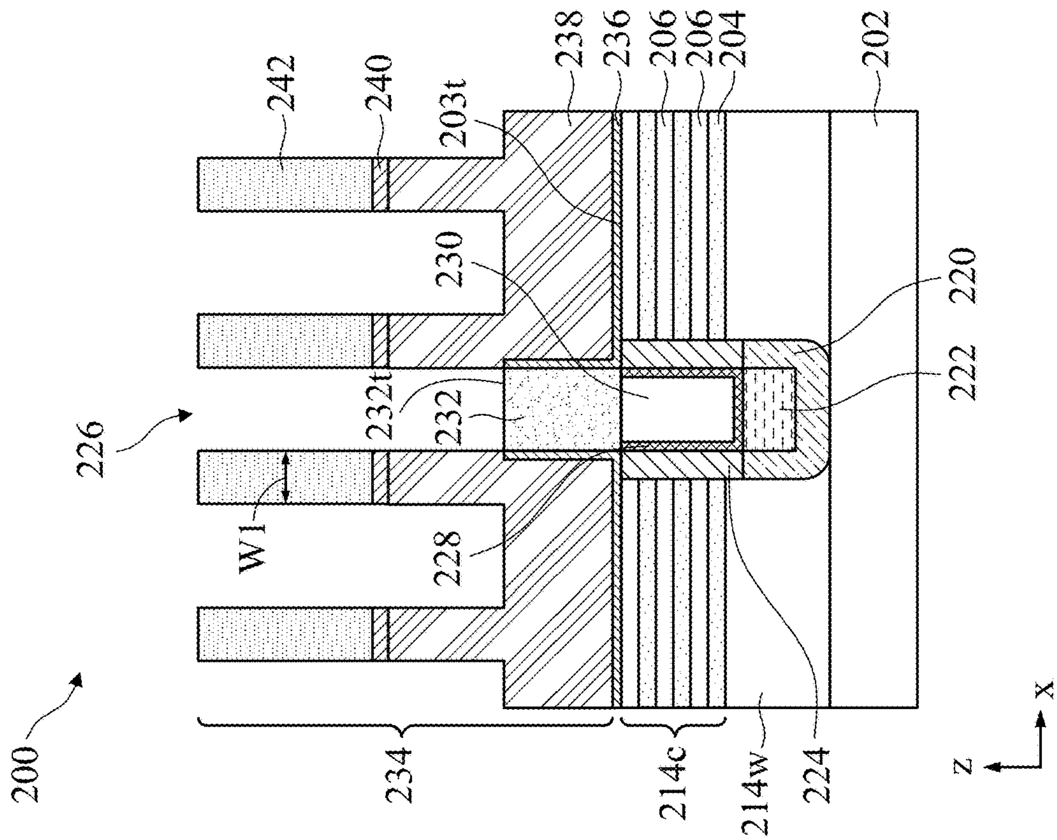

200
234
214c
214w
224
226
W1
228
232t
232
230
222
220
242
240
203t
238
236
206
206
204
202
z
x

FIG. 9B

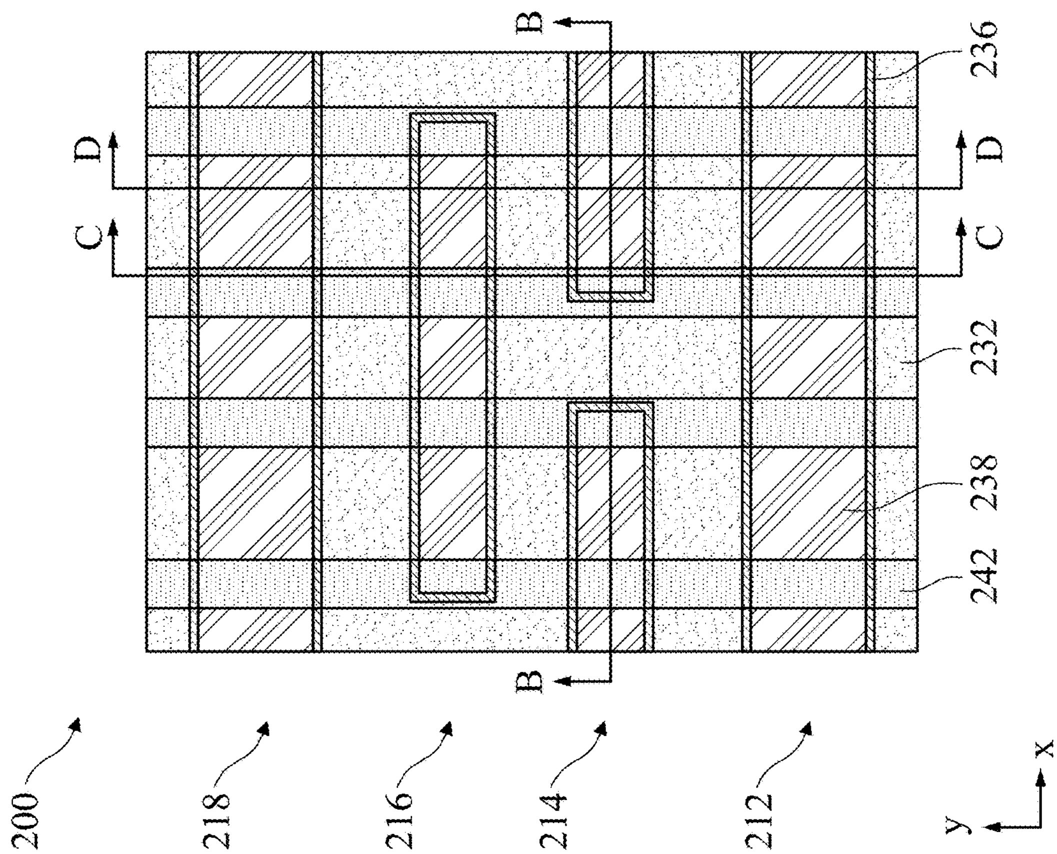
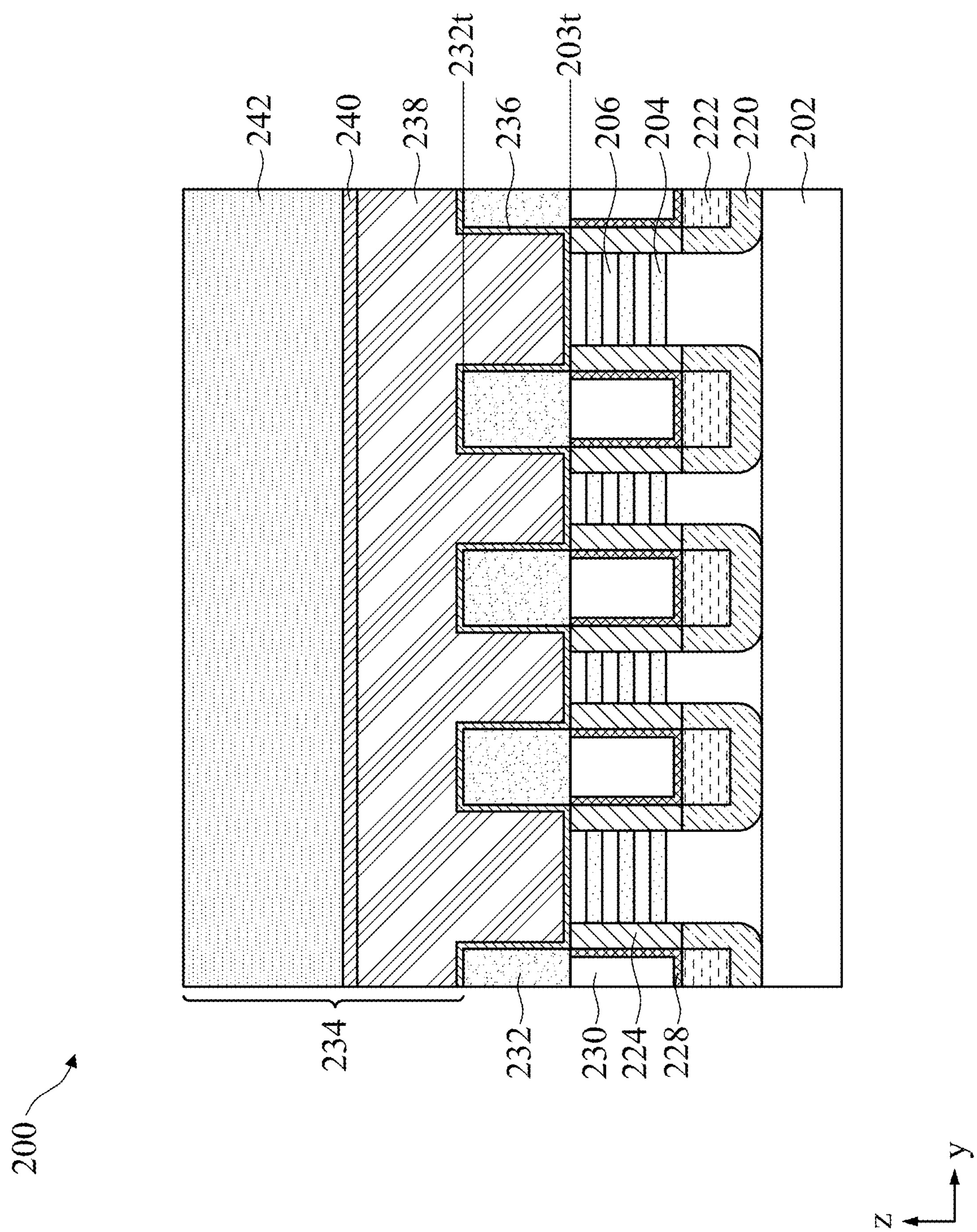

200
218
216
214
212
B
B
C
C
D
D
236
232
238
242
y
x

FIG. 9A



200
242
240
238
232t
236
203t
206
204
222
220
202
234
232
230
224
228
z
y

FIG. 9C

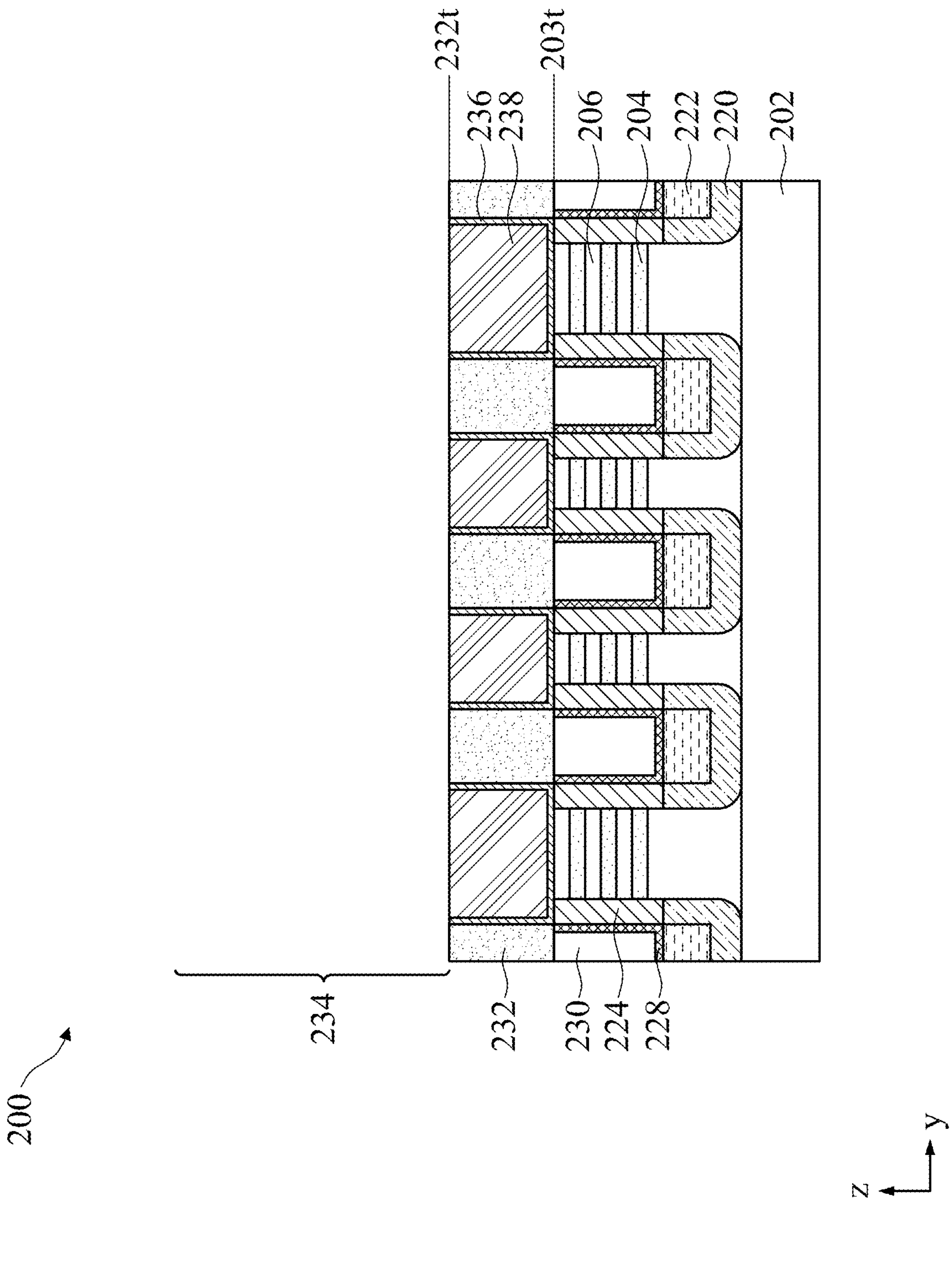


FIG. 9D

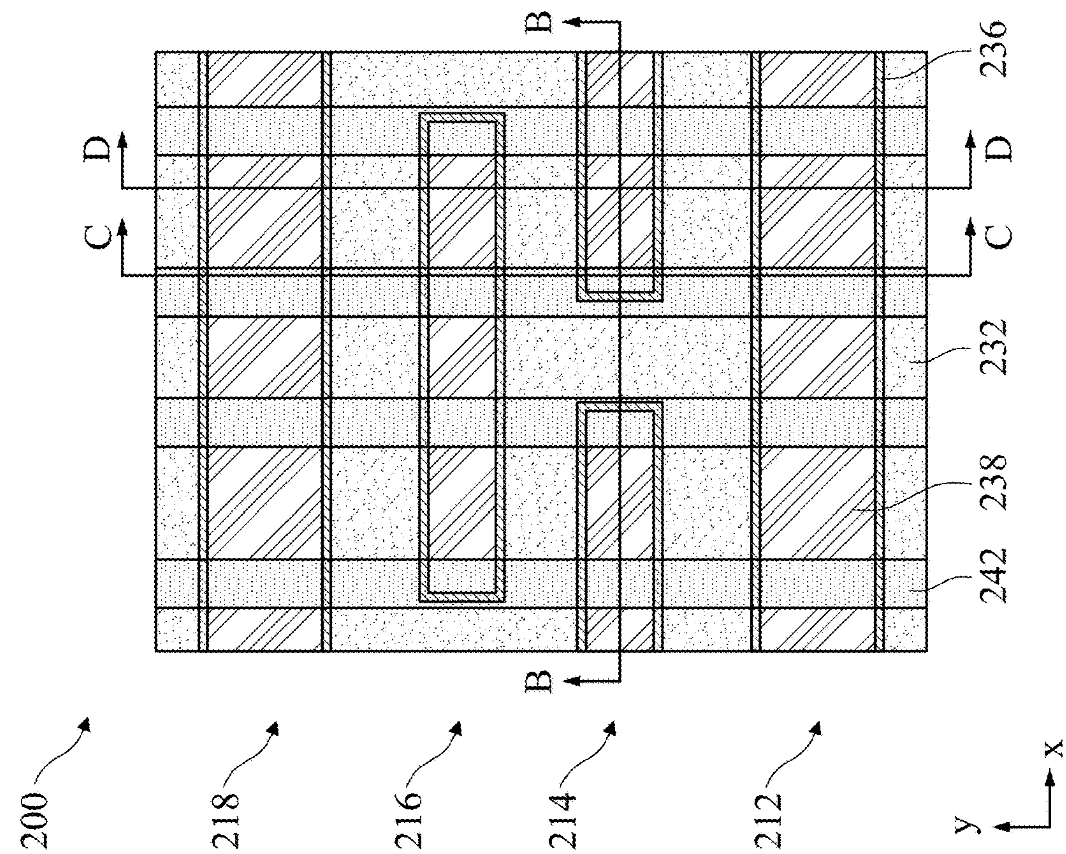


FIG. 10A

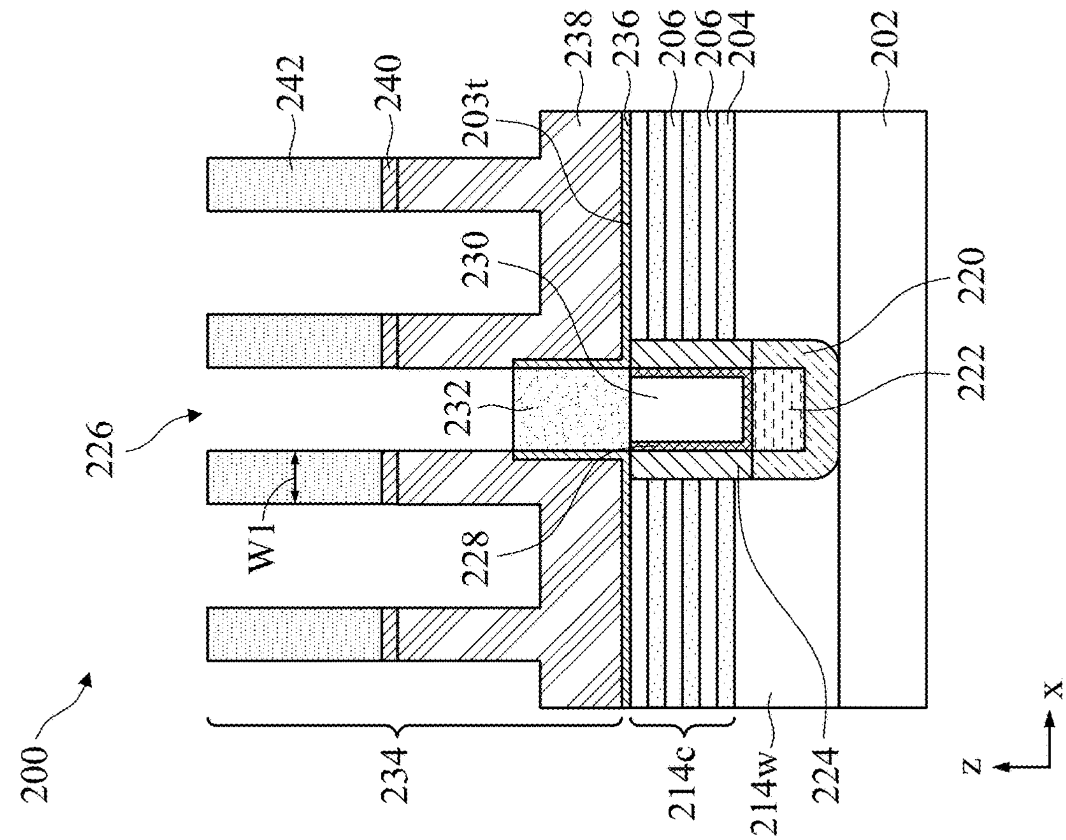


FIG. 10B

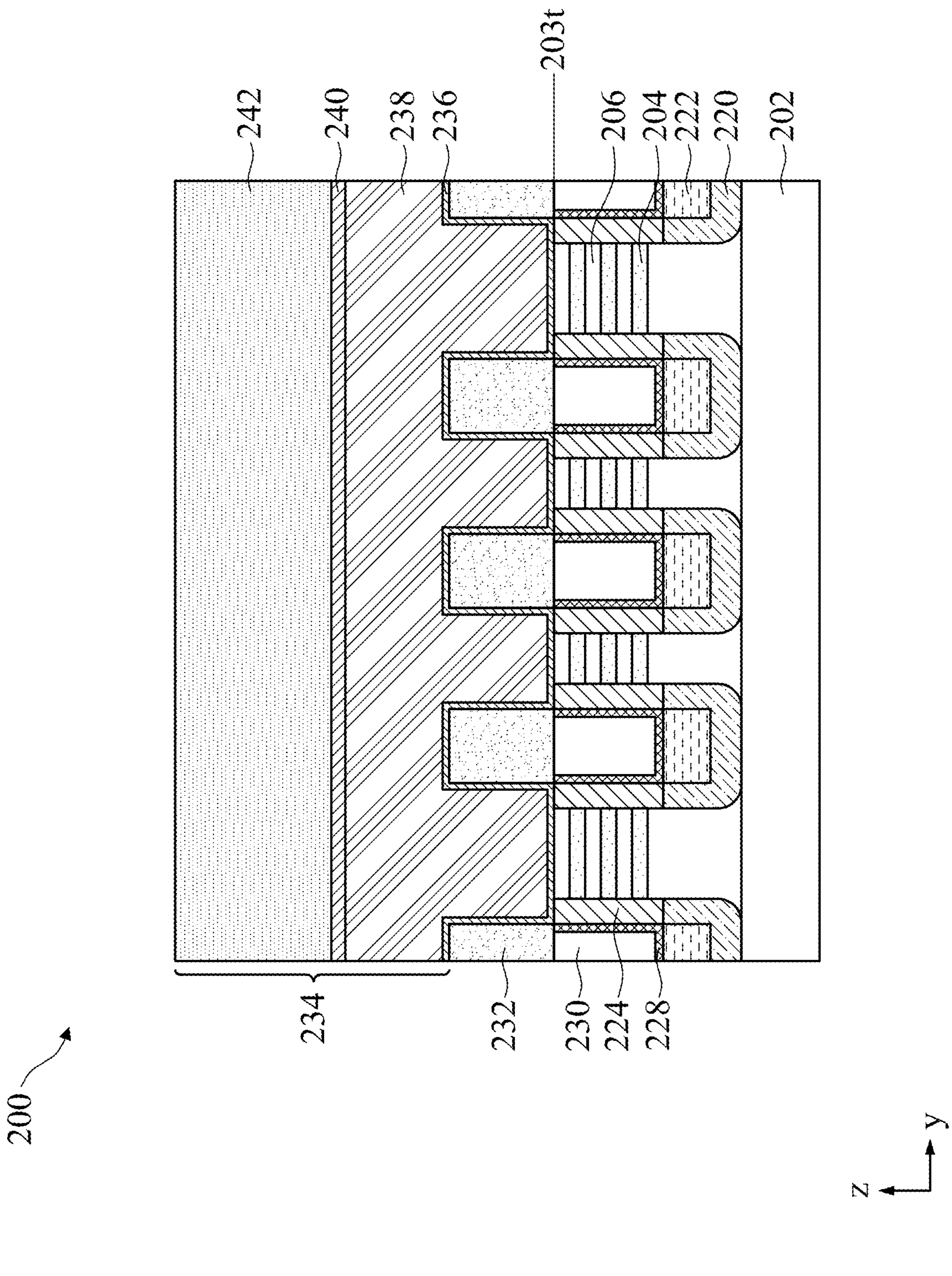

200
242
240
238
236
203t
206
204
222
220
202
234
232
230
224
228
y
z

FIG. 10C

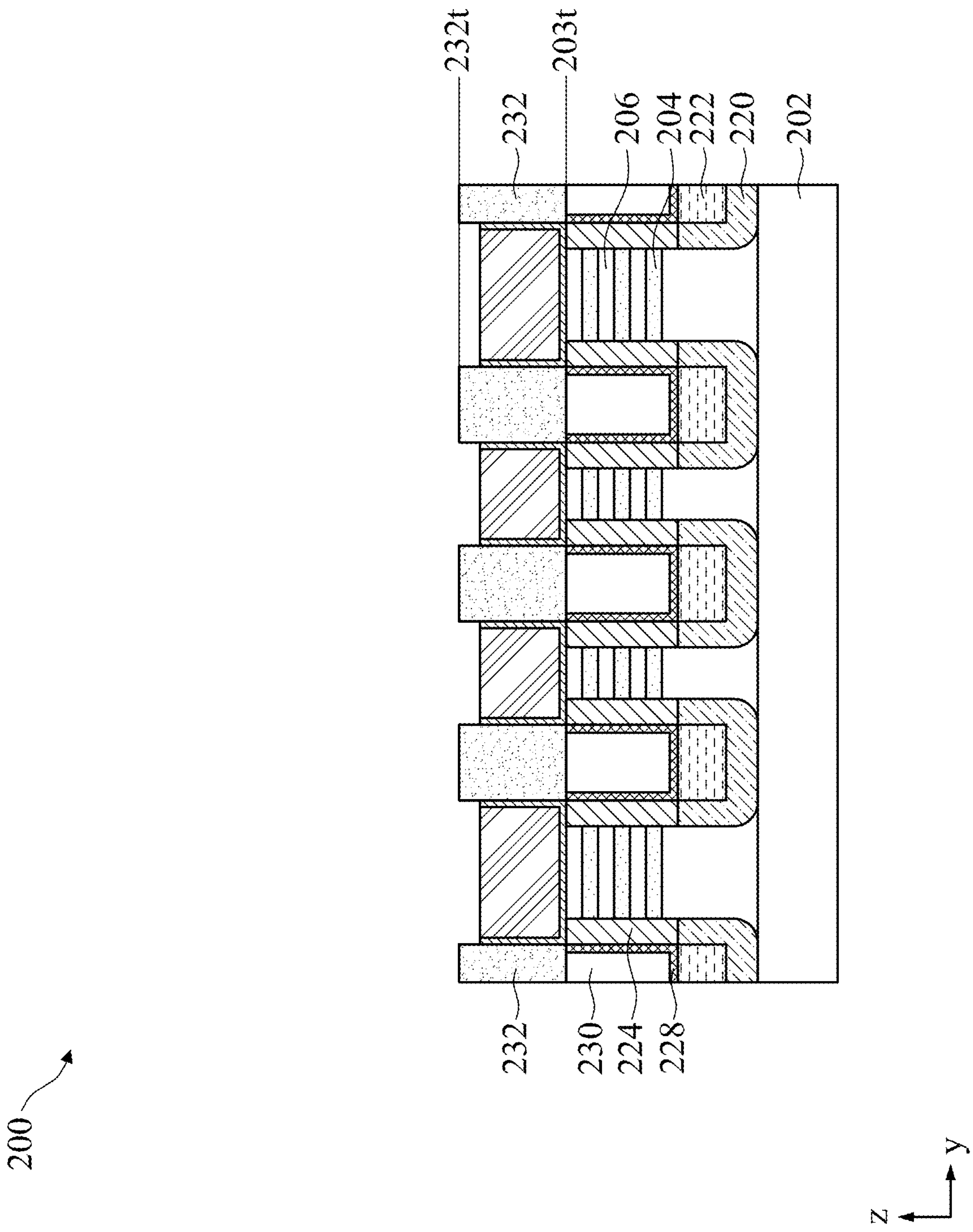
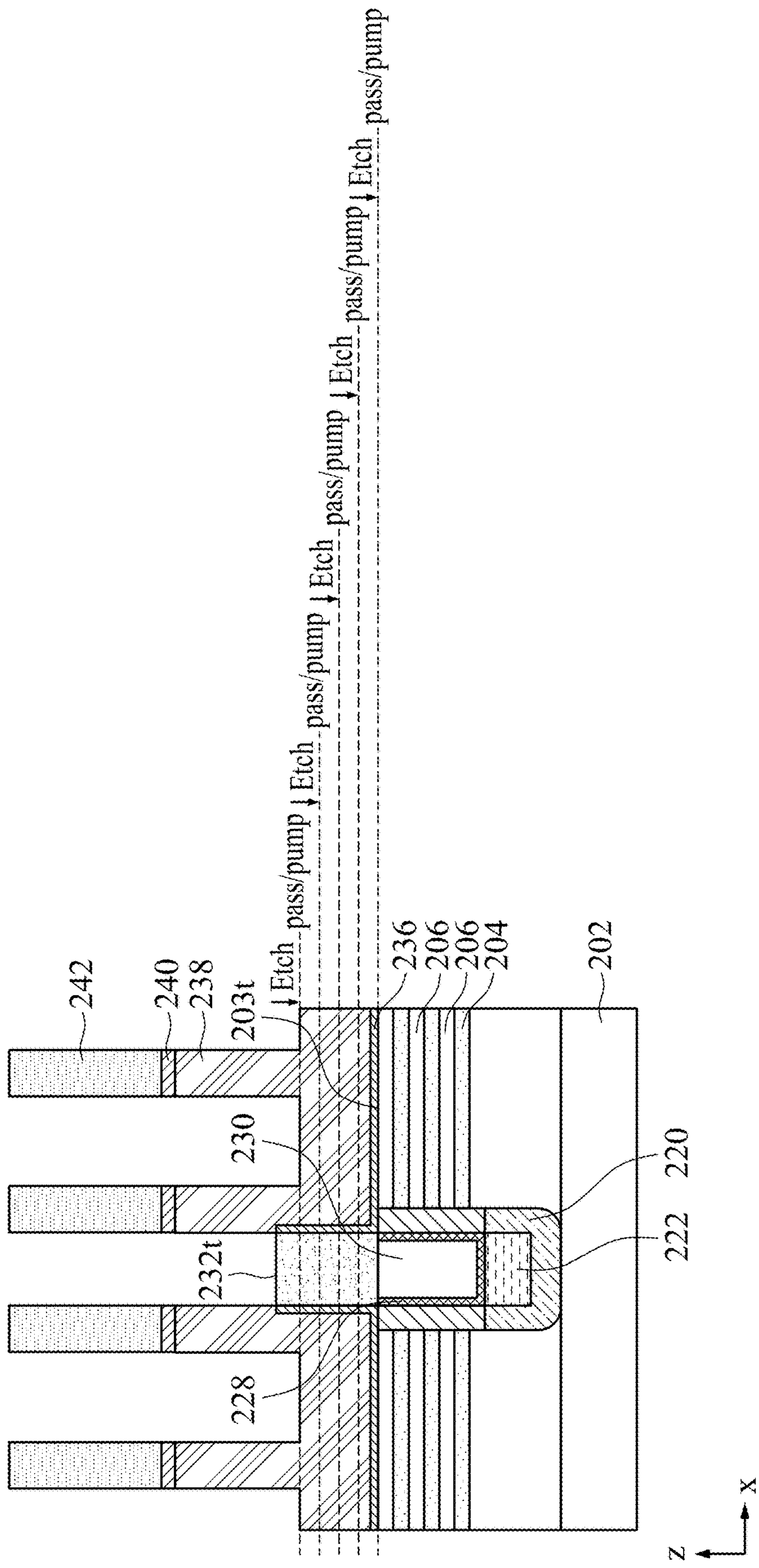


FIG. 10D



242
240
238
203t
Etch
pass/pump
Etch
pass/pump
Etch
pass/pump
Etch
pass/pump
Etch
pass/pump
236
206
206
204
202
230
220
222
232t
228
z
x

FIG. 10E

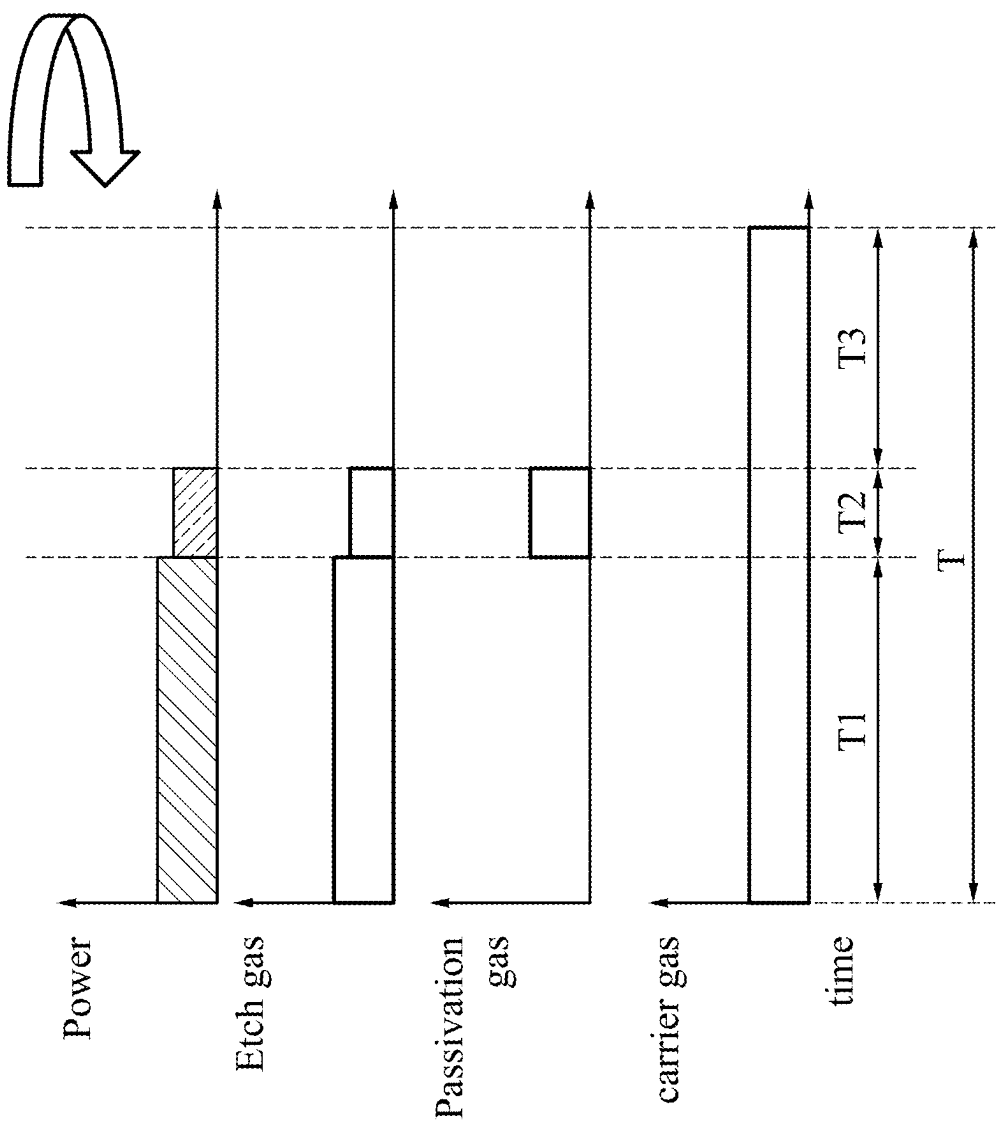


FIG. 10F

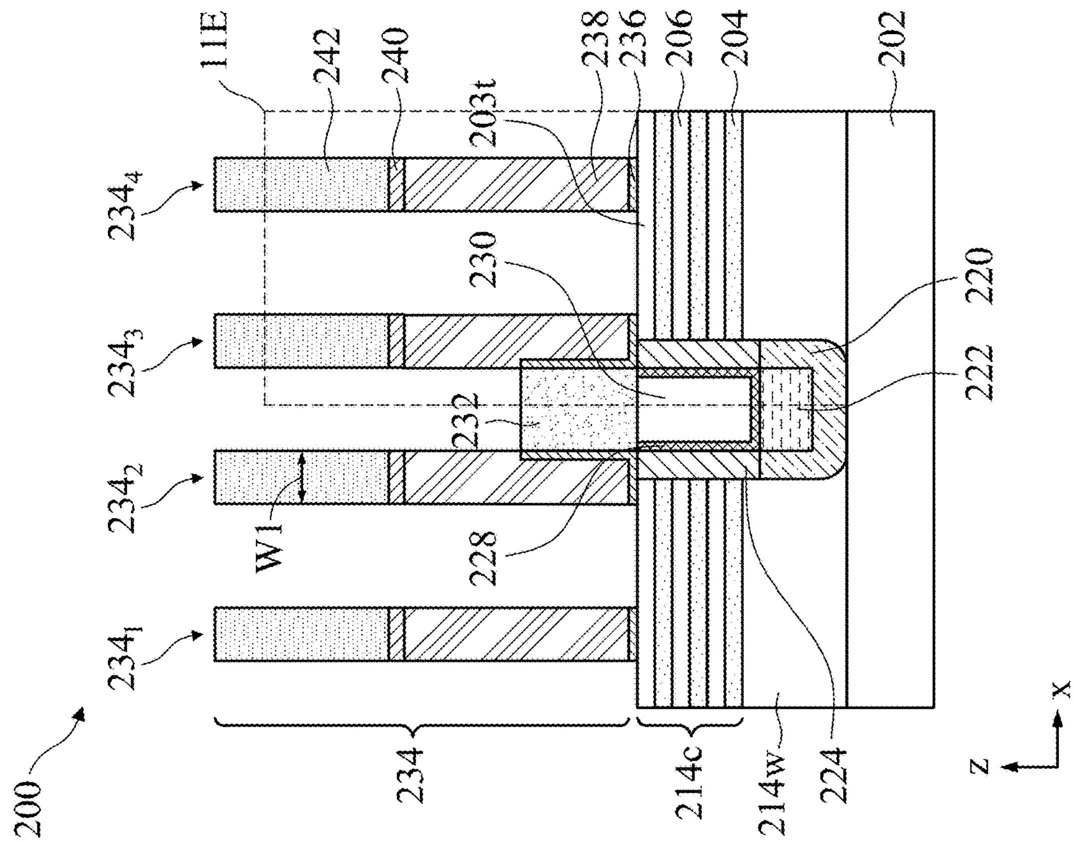


FIG. 11B

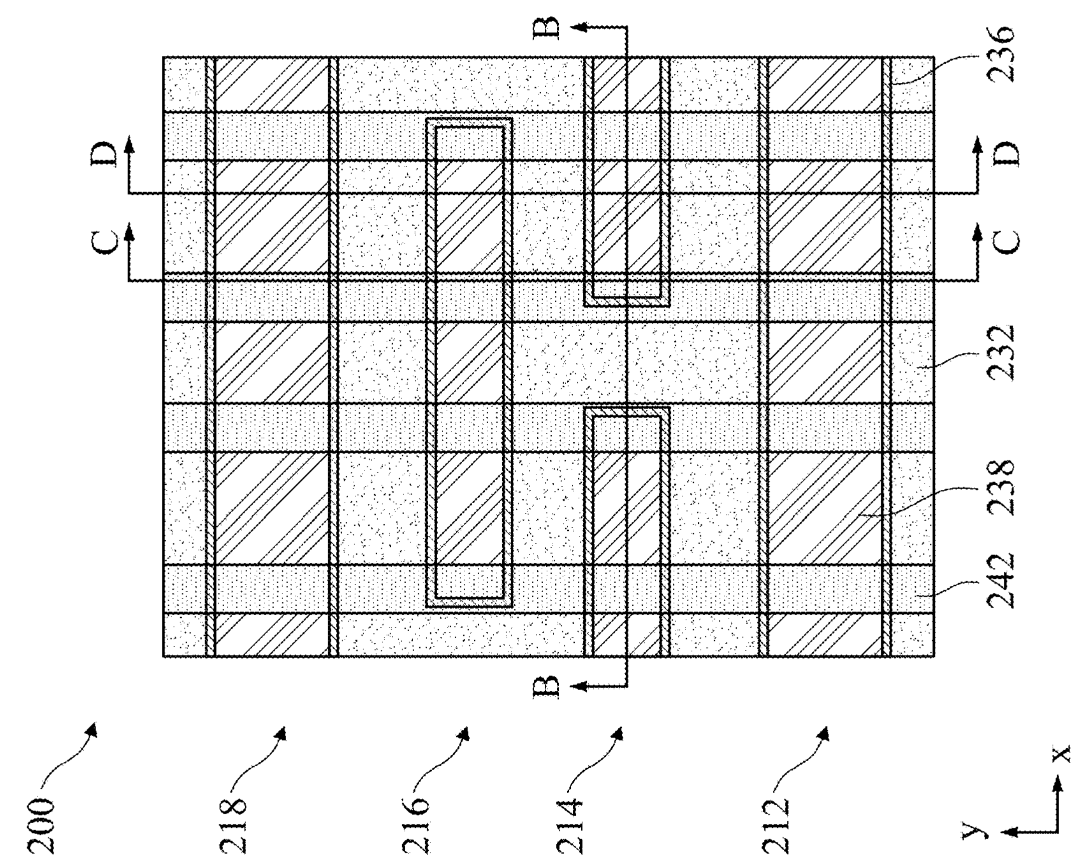


FIG. 11A

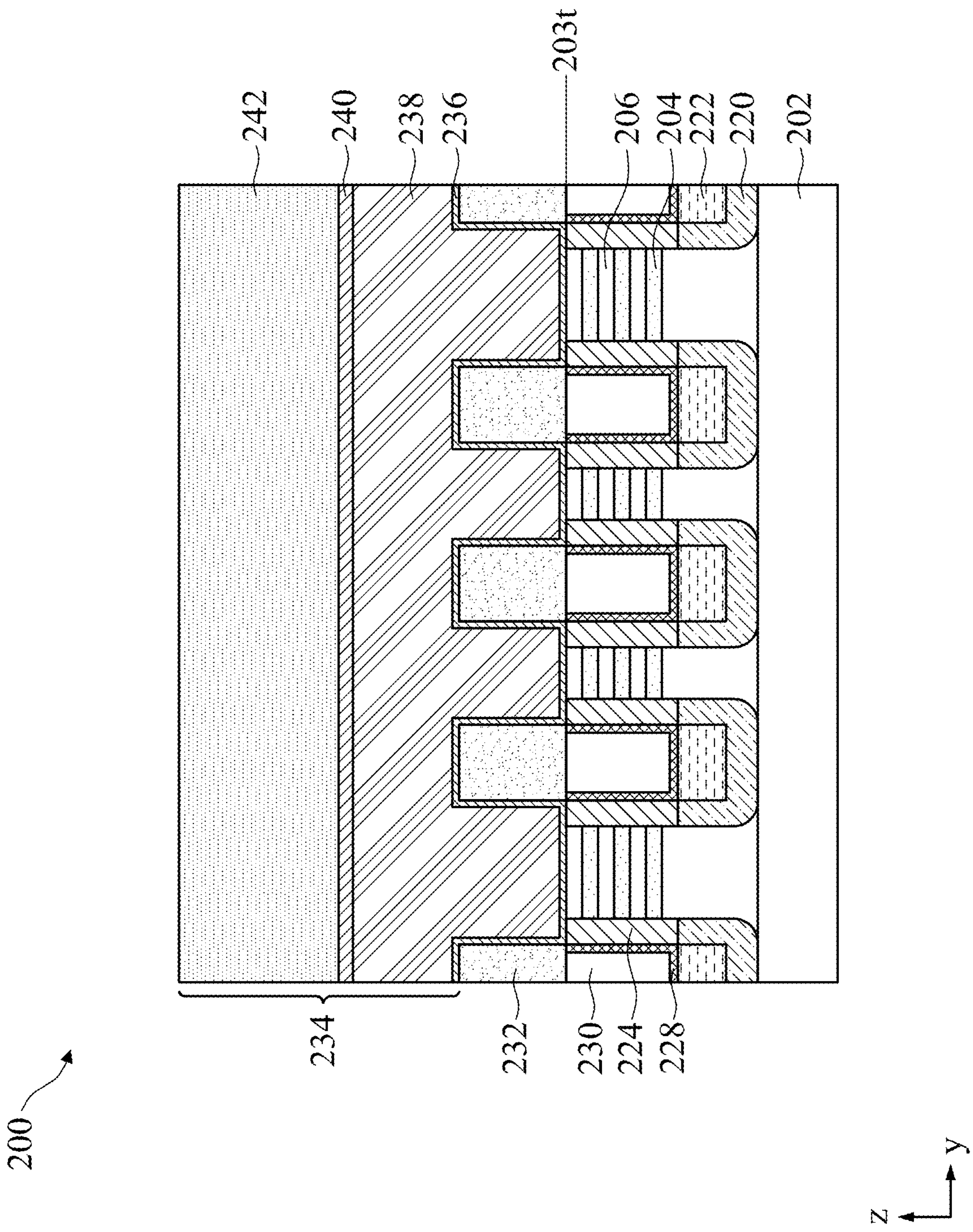

242
240
238
236
203t
206
204
222
220
202
234
232
230
224
228
200
y
z

FIG. 11C

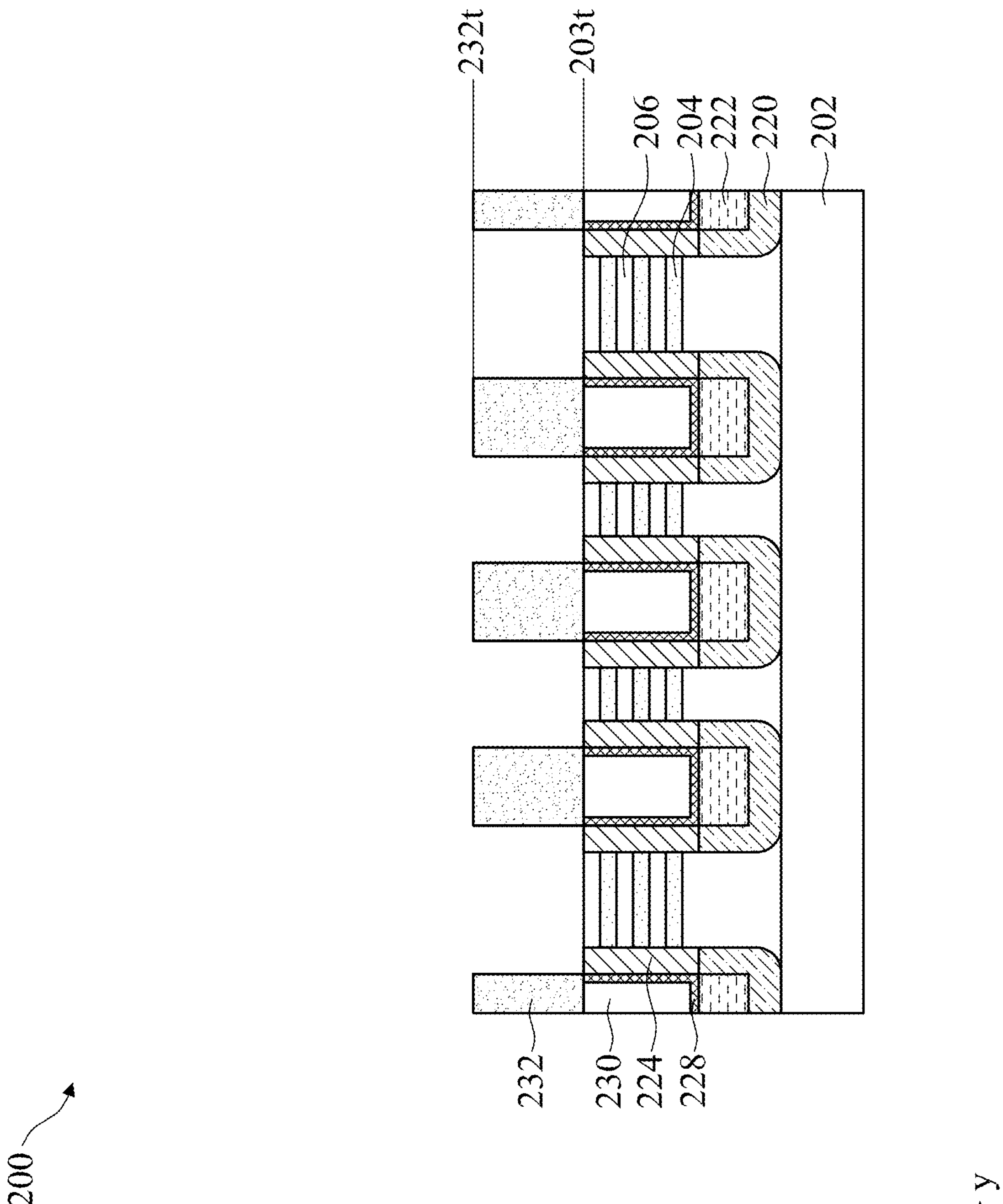


FIG. 11D

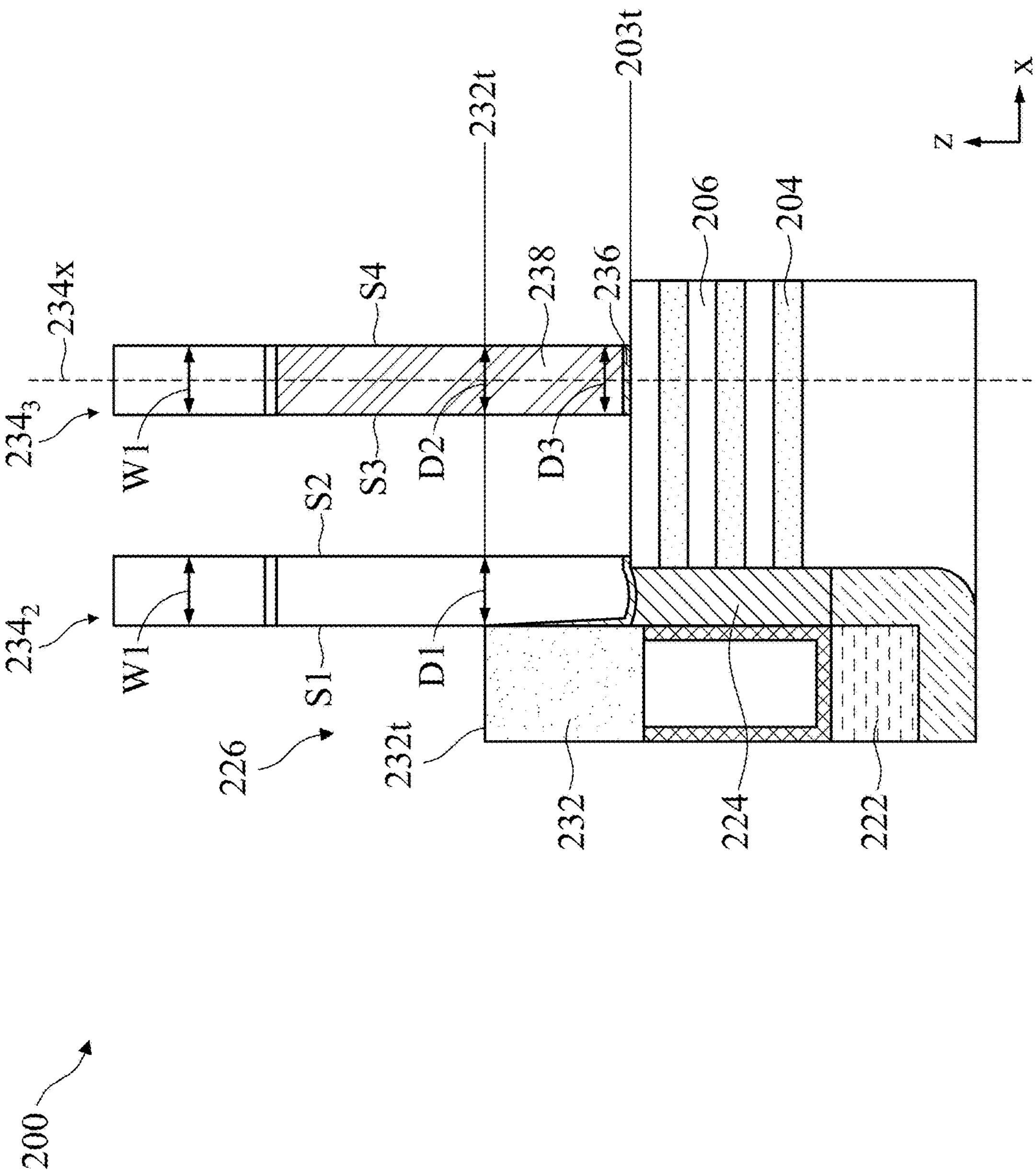

200
226
232t
232
224
222
234_2
234_3
234x
W1
W1
S1
S2
S3
S4
D1
D2
D3
236
238
232t
203t
206
204
z
x

FIG. 11E

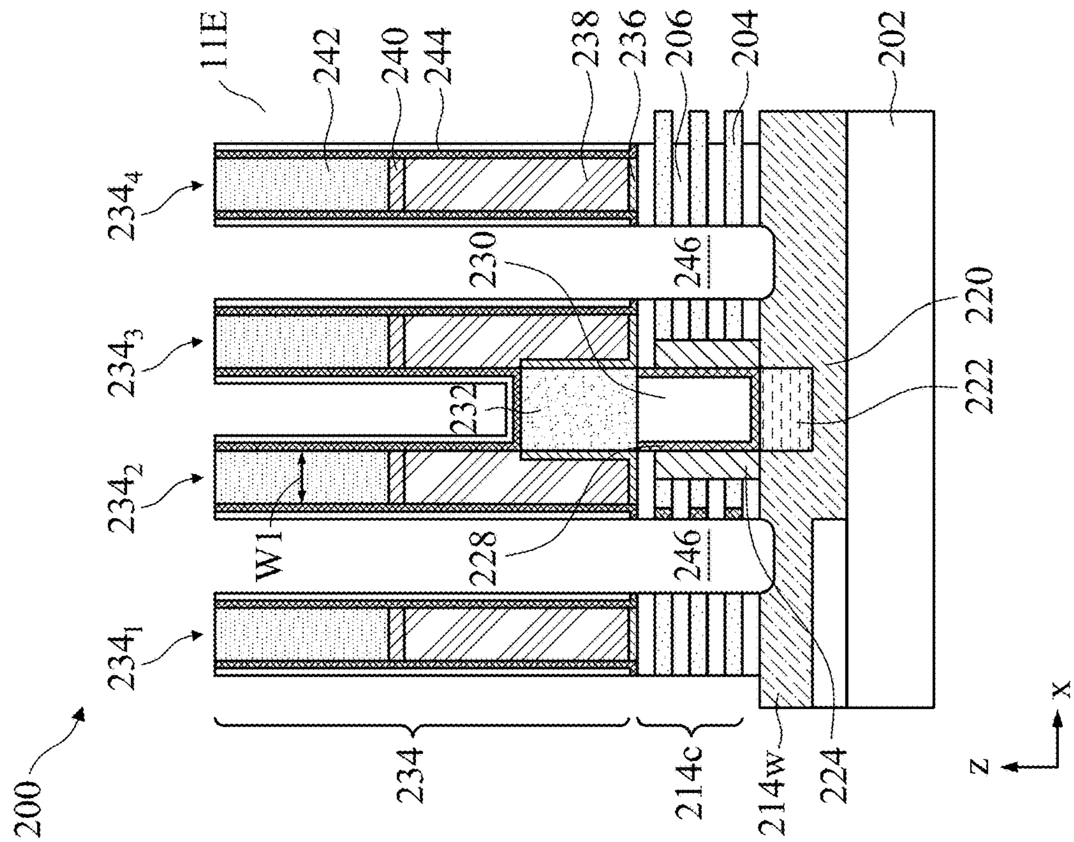


FIG. 12B

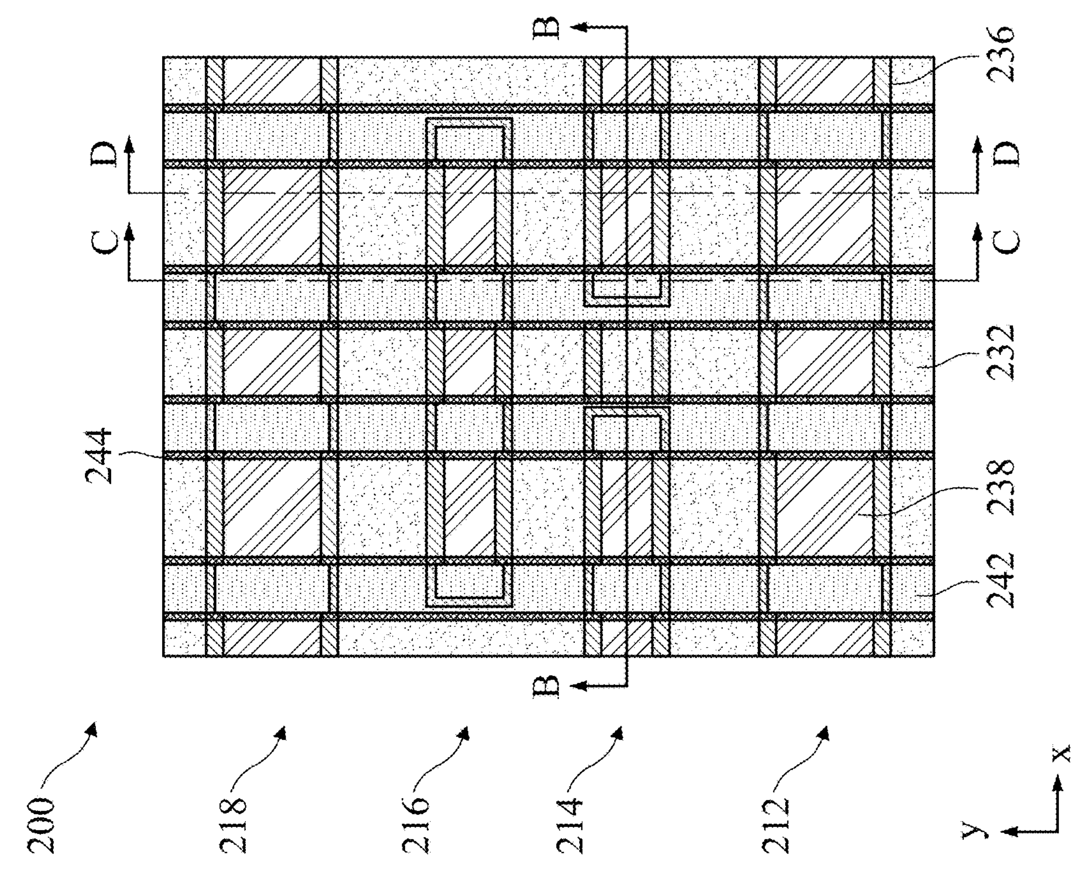
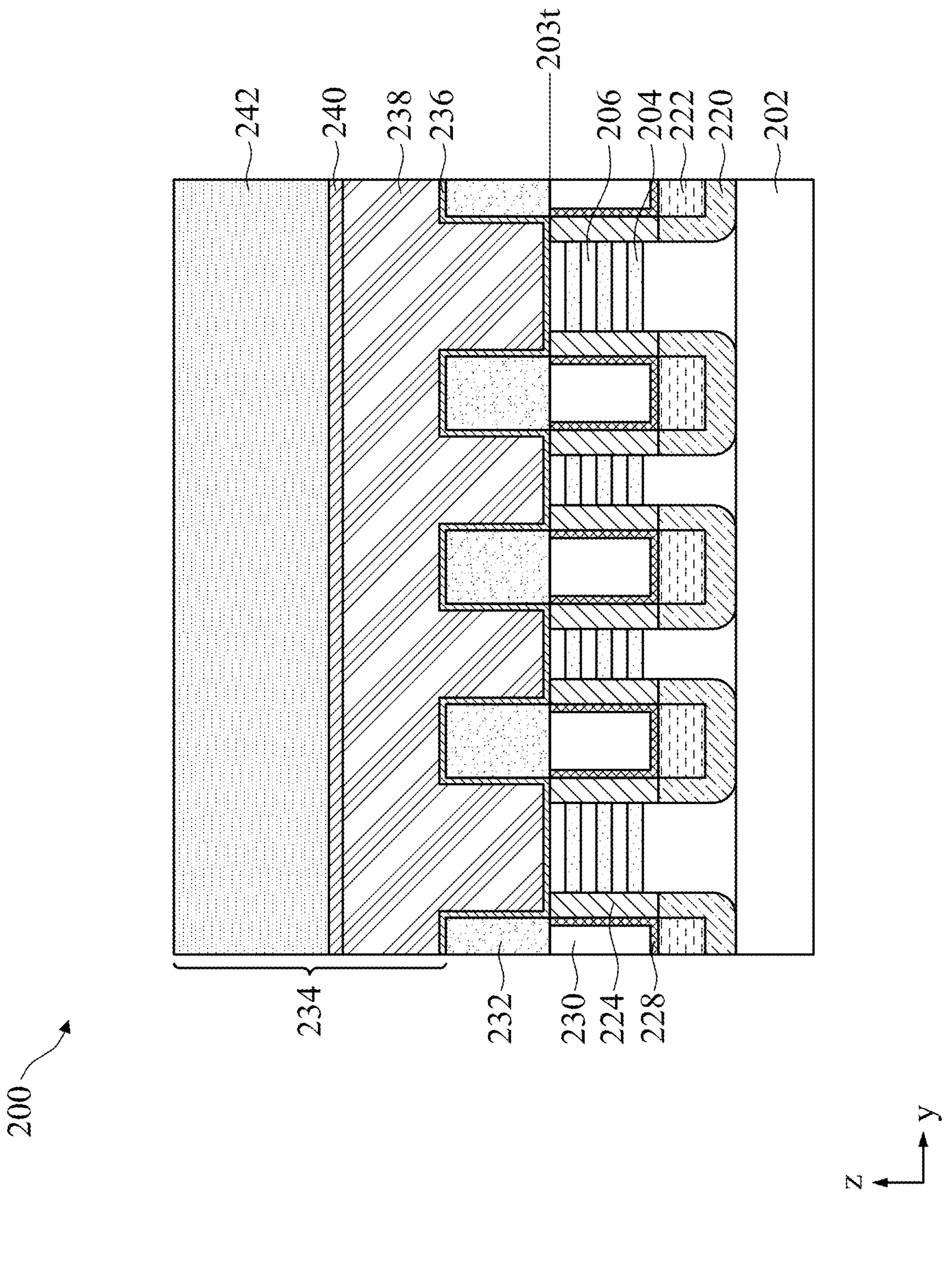


FIG. 12A



200
234
232
230
224
228
242
240
238
236
203t
206
204
222
220
202
z
y

FIG. 12C

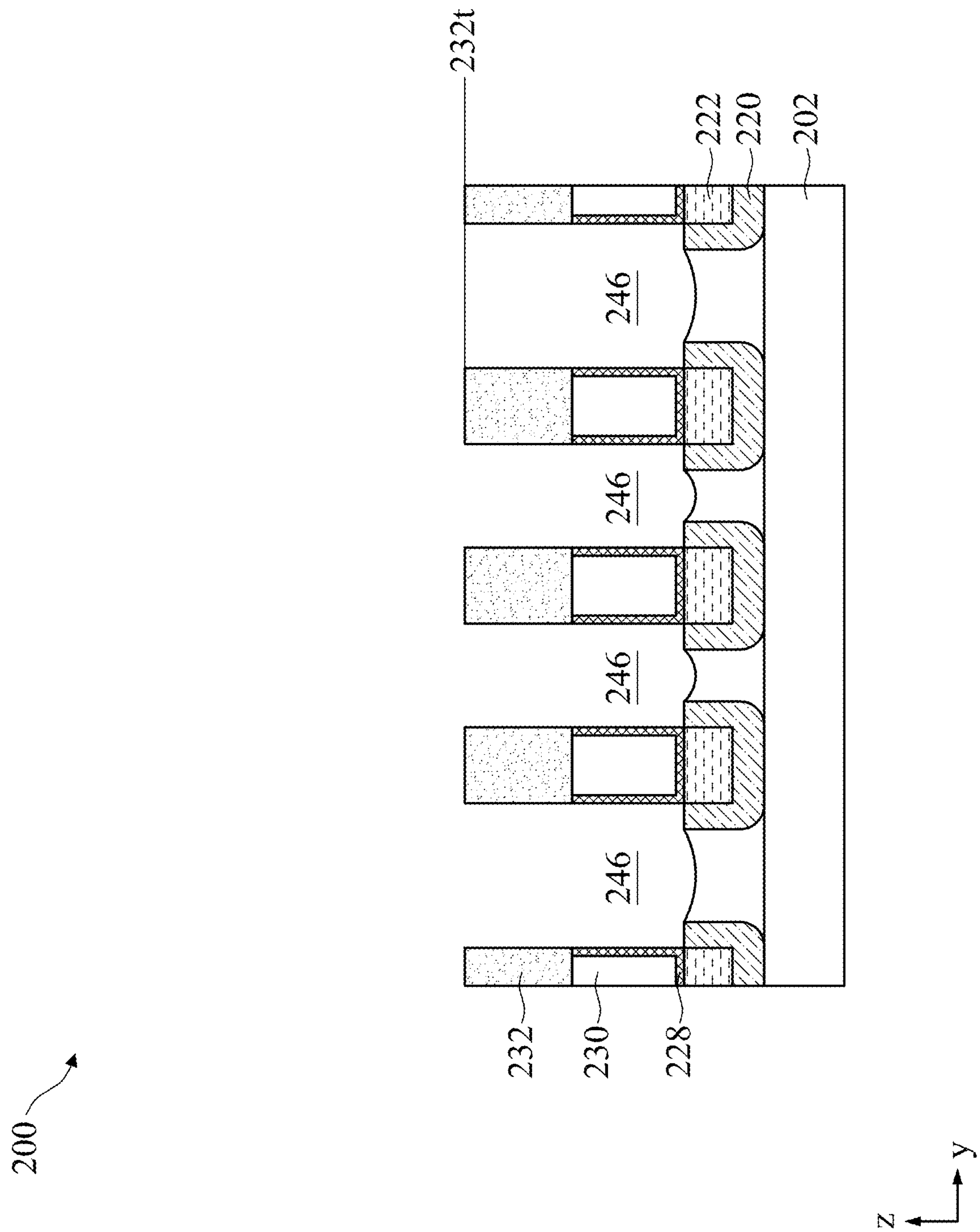


FIG. 12D

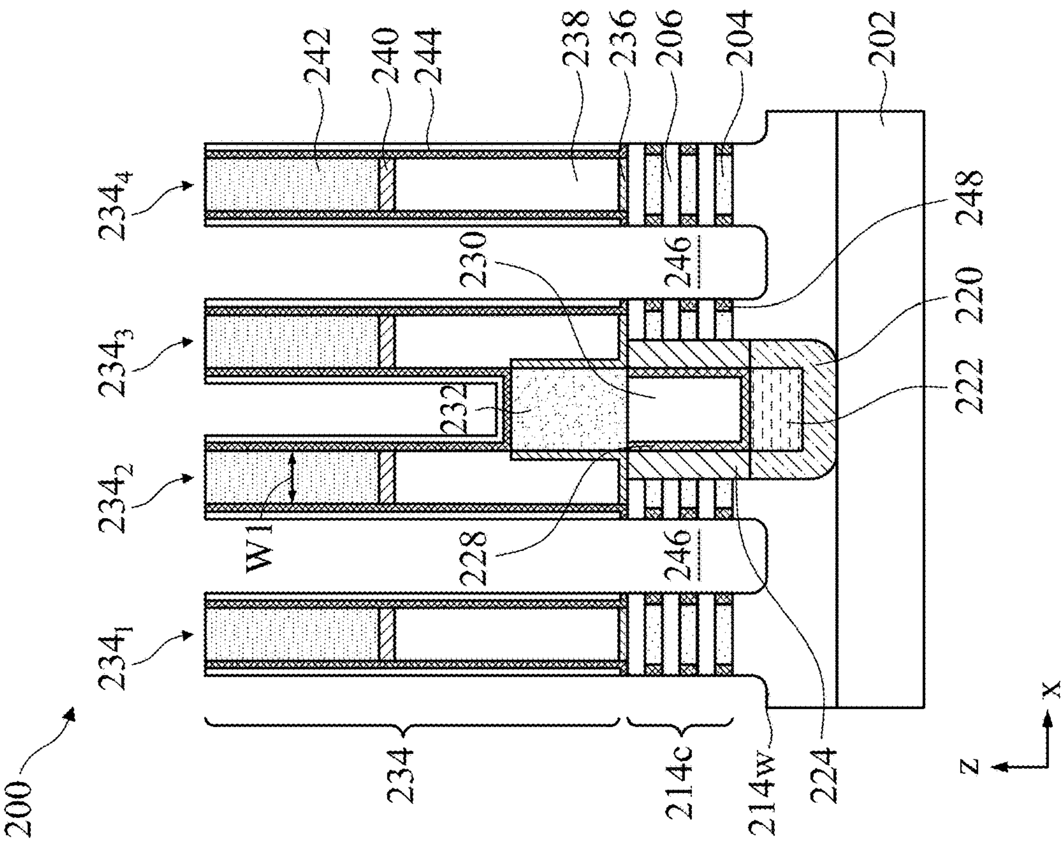


FIG. 13B

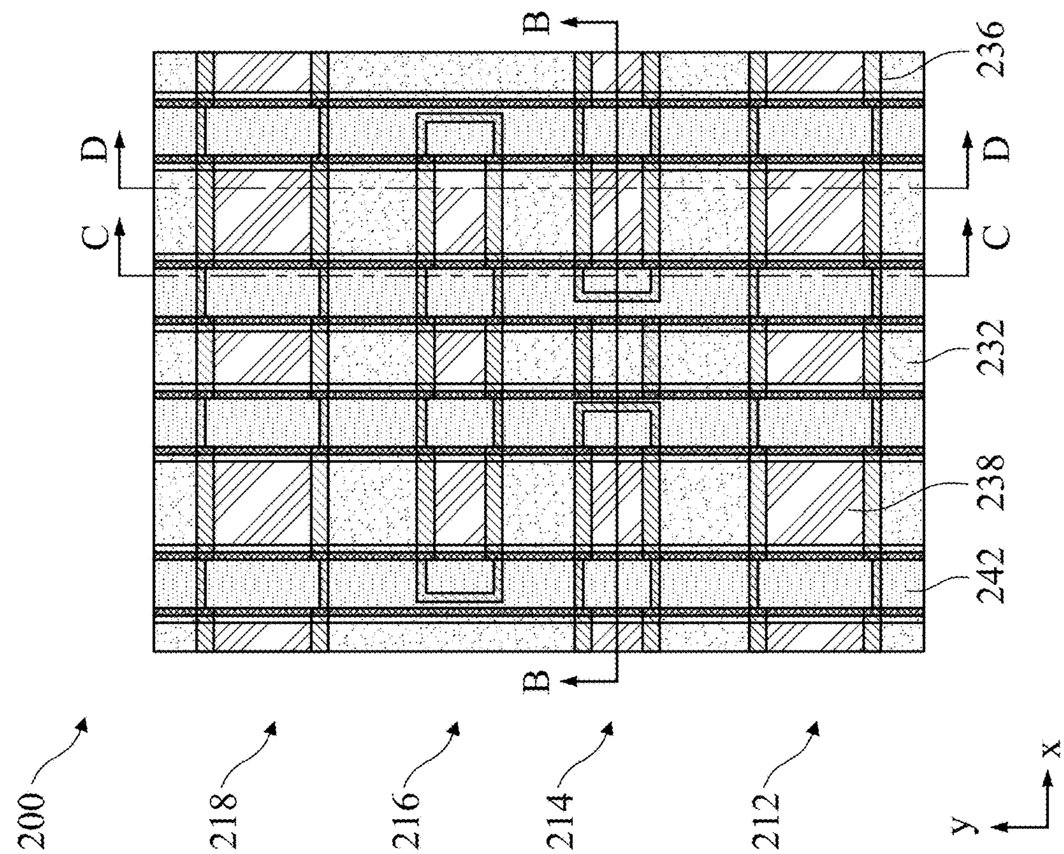


FIG. 13A

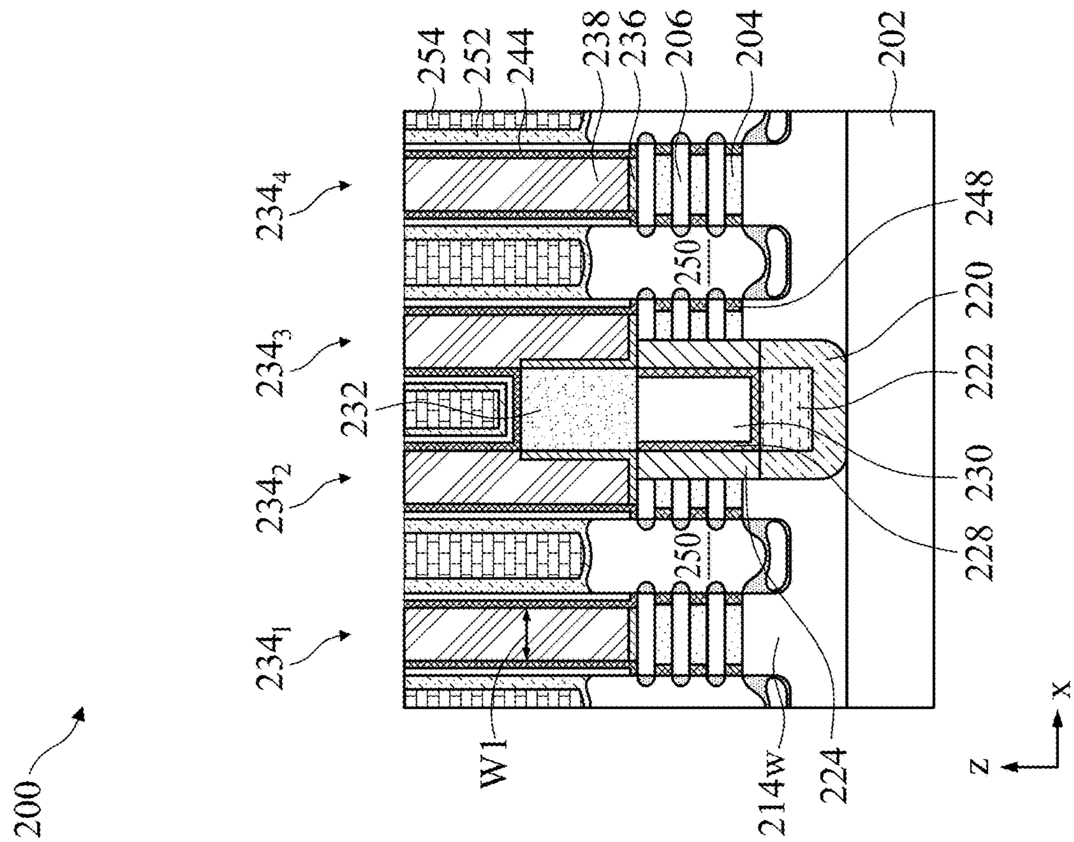


FIG. 14B

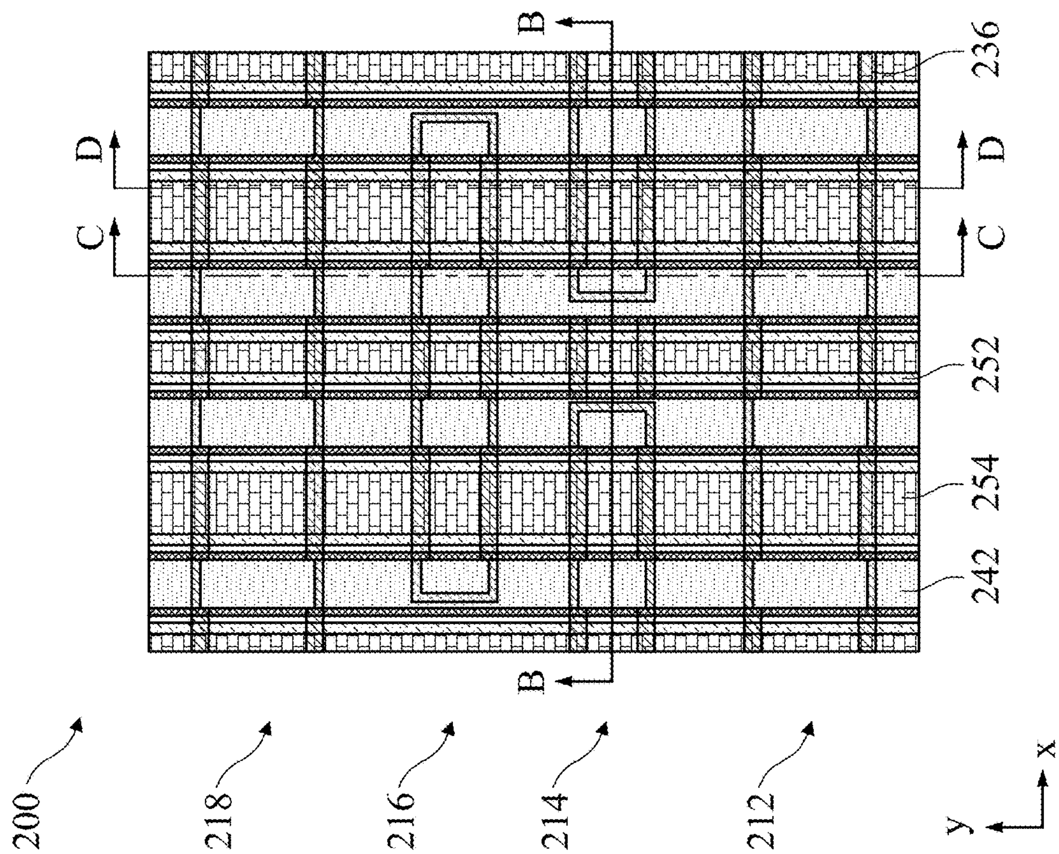


FIG. 14A

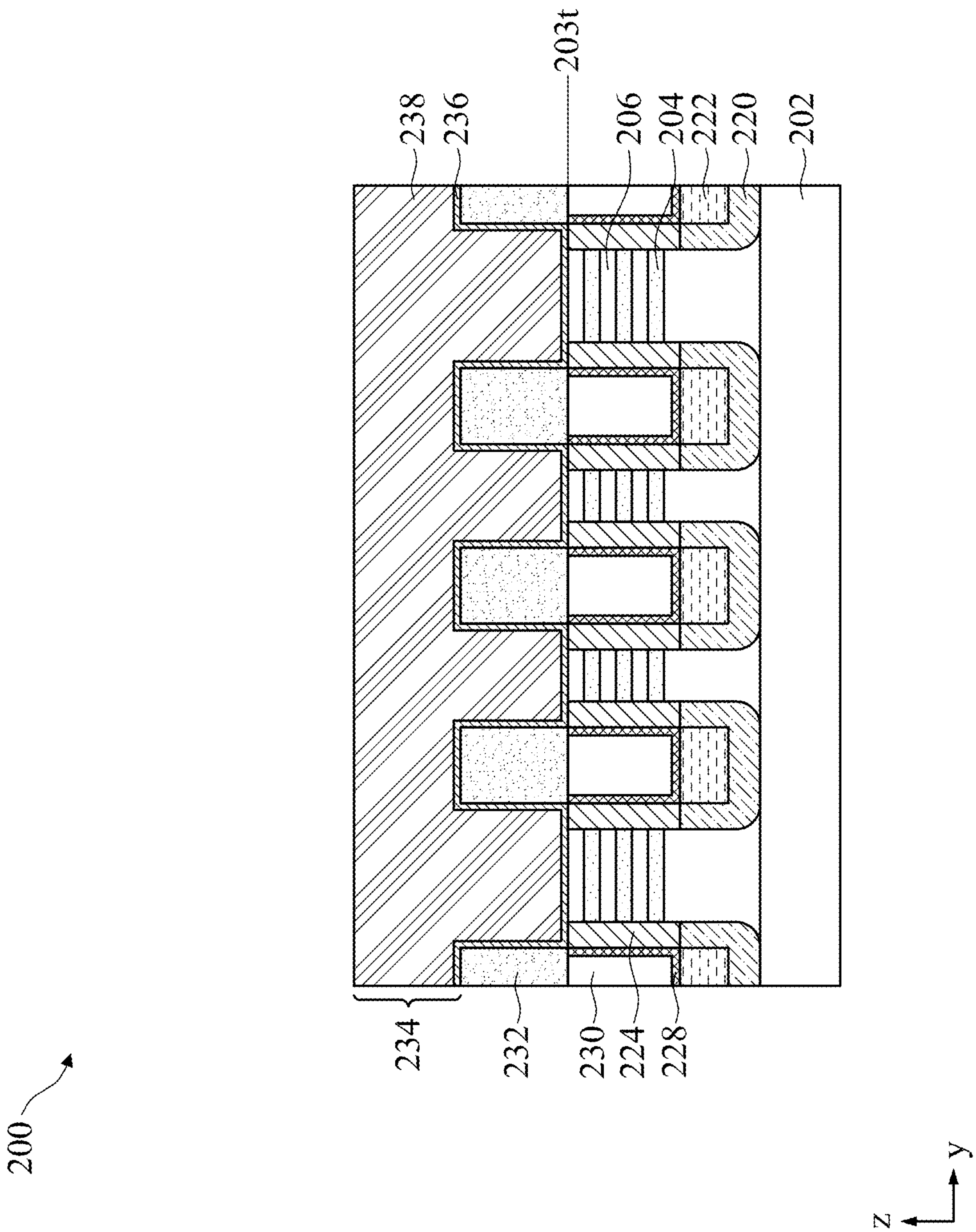


FIG. 14C

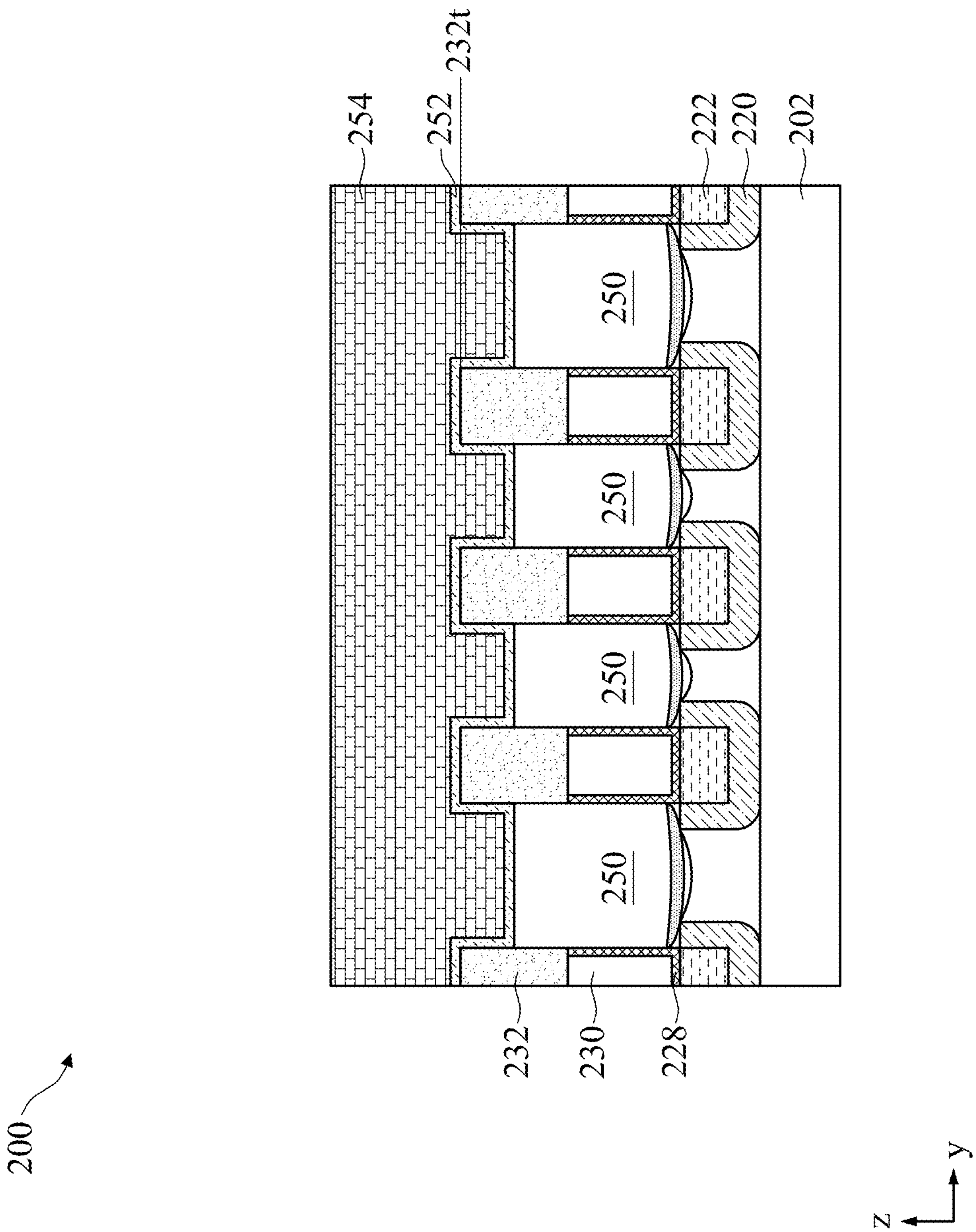


FIG. 14D

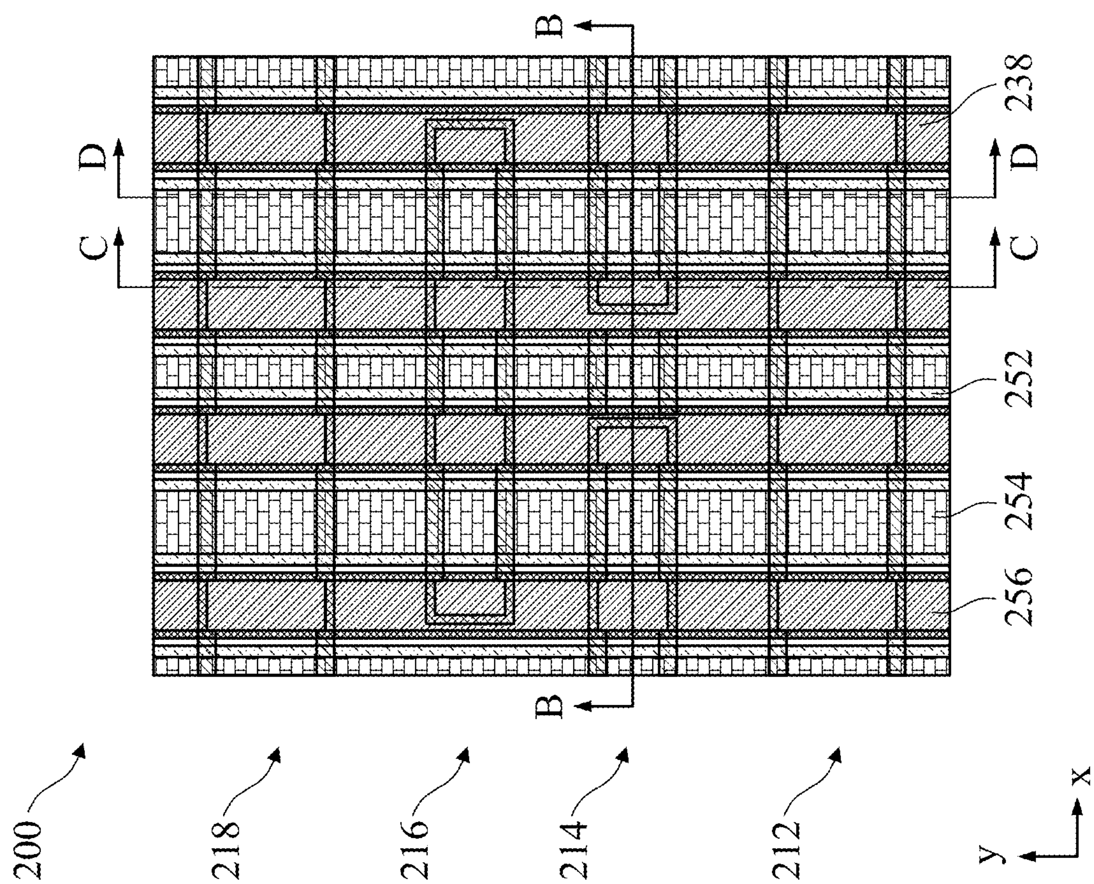


FIG. 15A

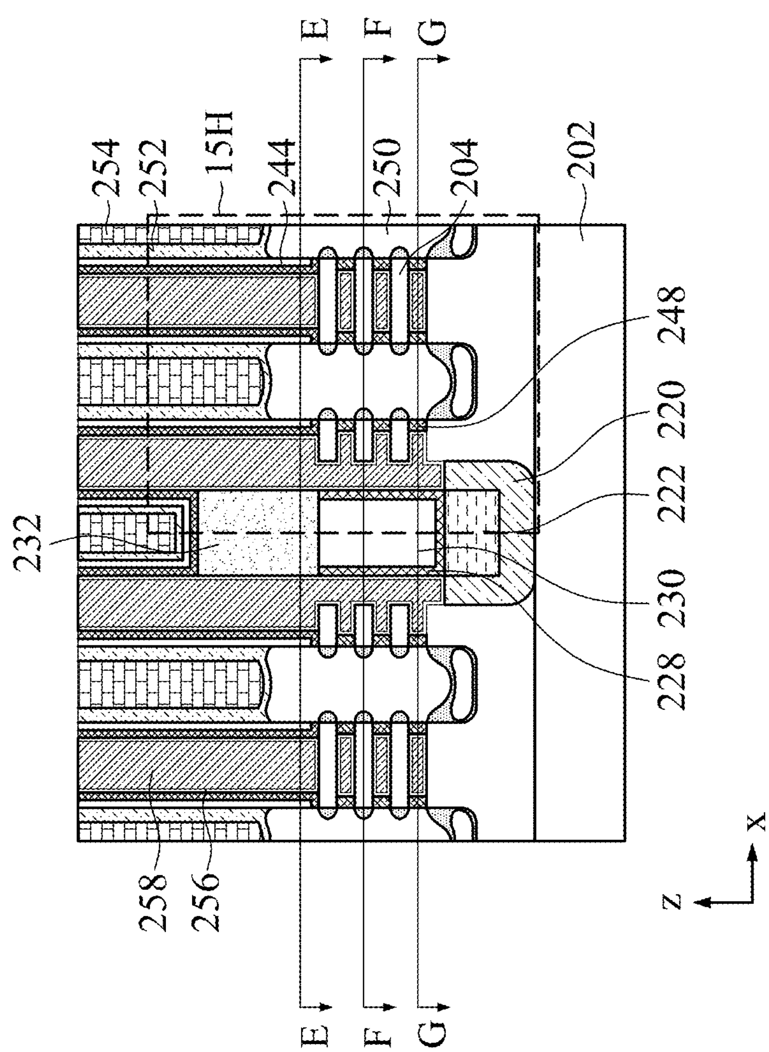

254
252
15H
244
250
204
202
248
220
222
230
228
232
258
256
E
F
G
E
F
G
z
x

FIG. 15B

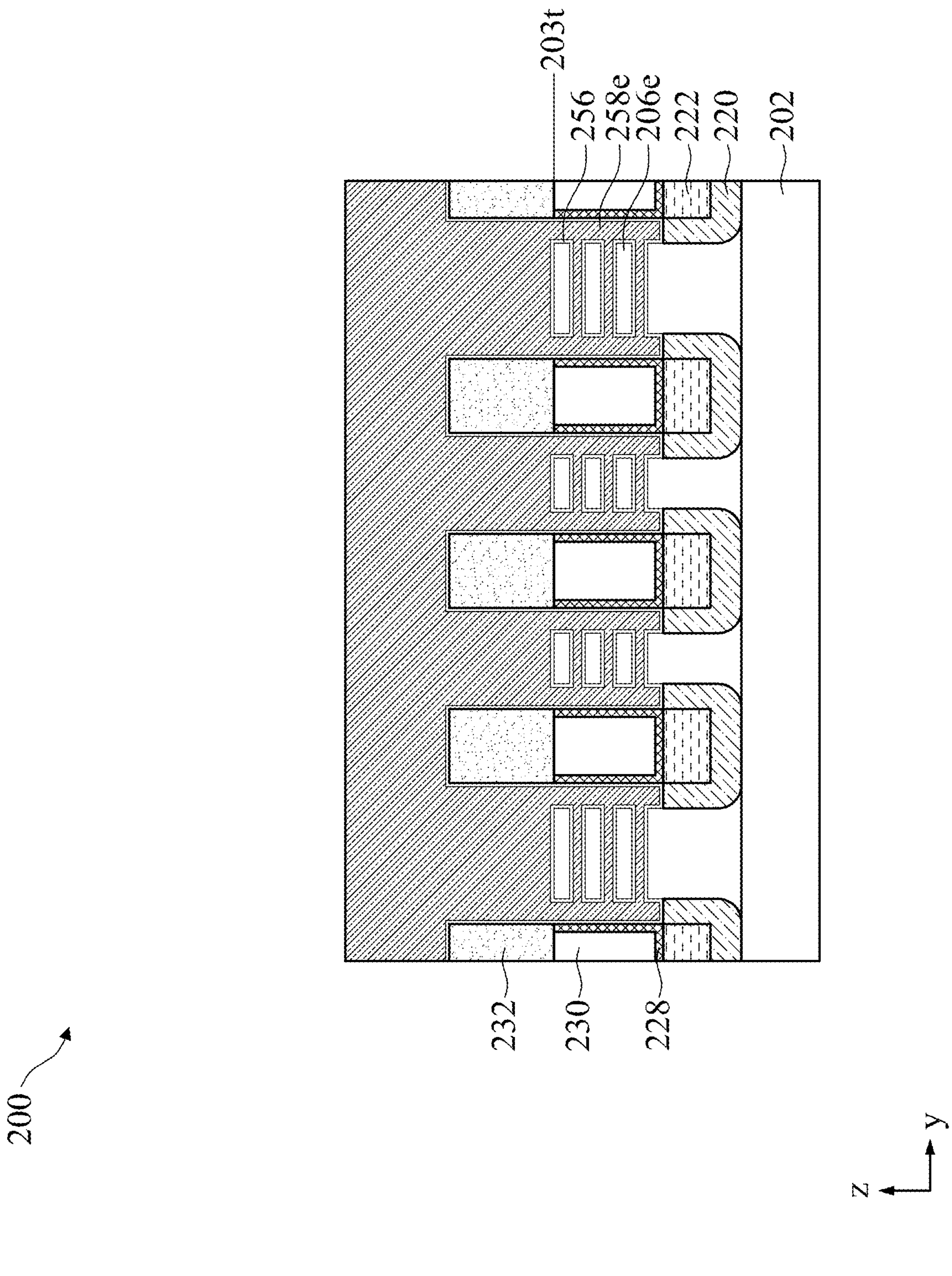


FIG. 15C

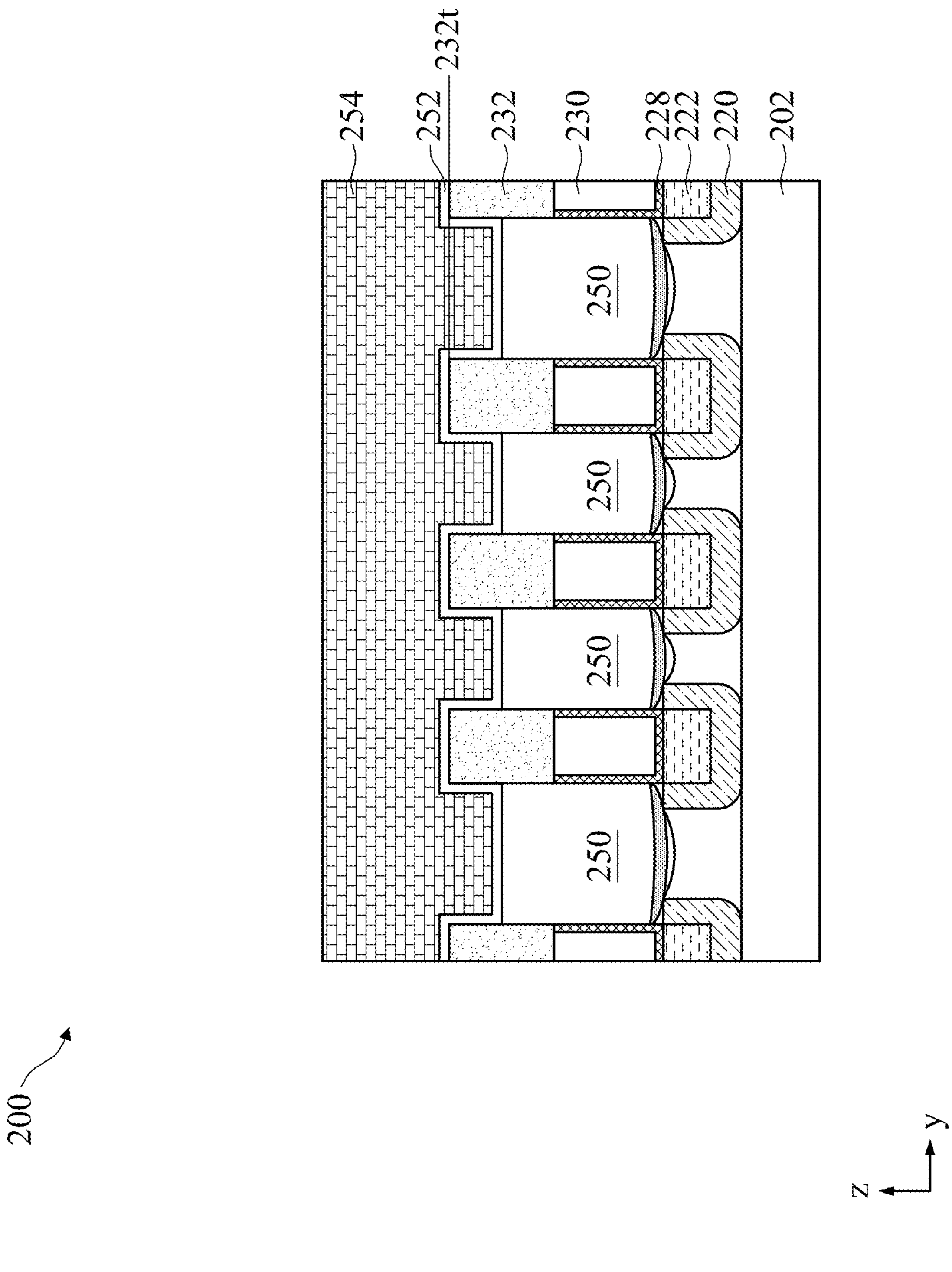


FIG. 15D

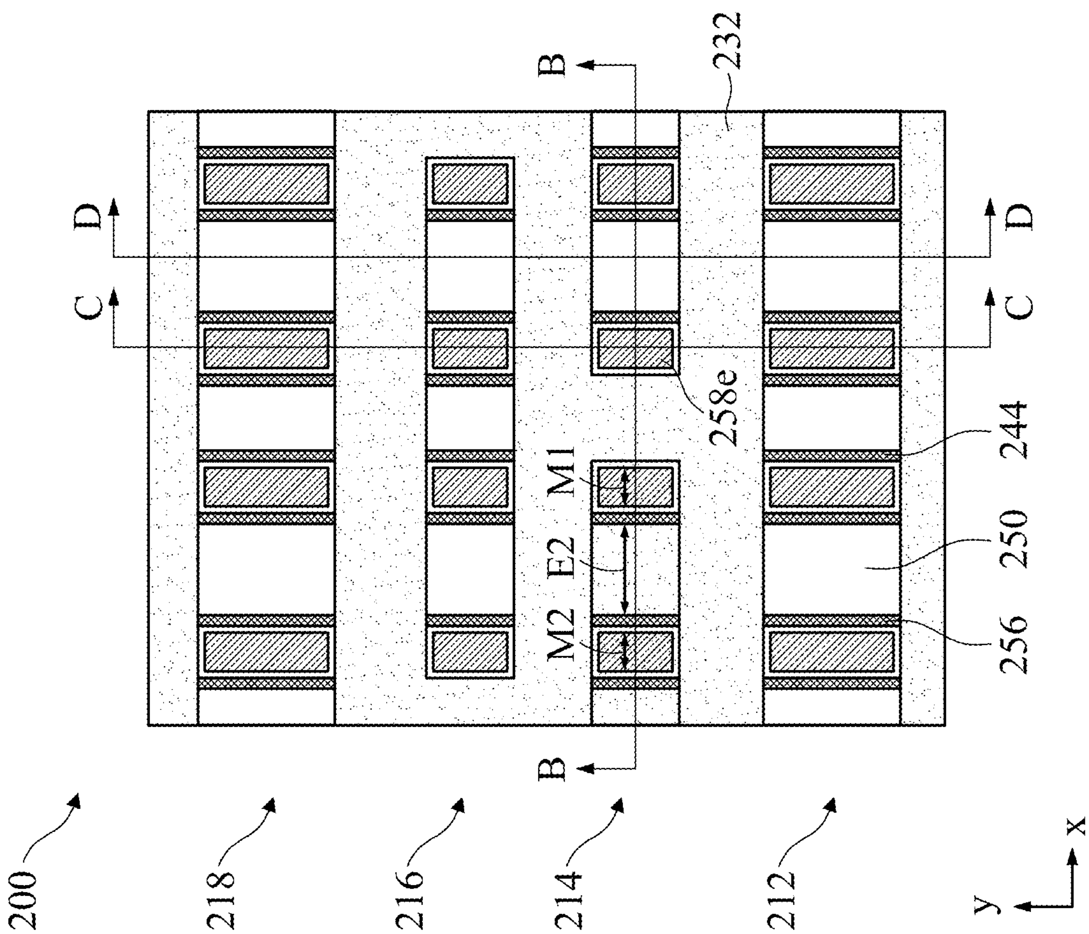


FIG. 15E

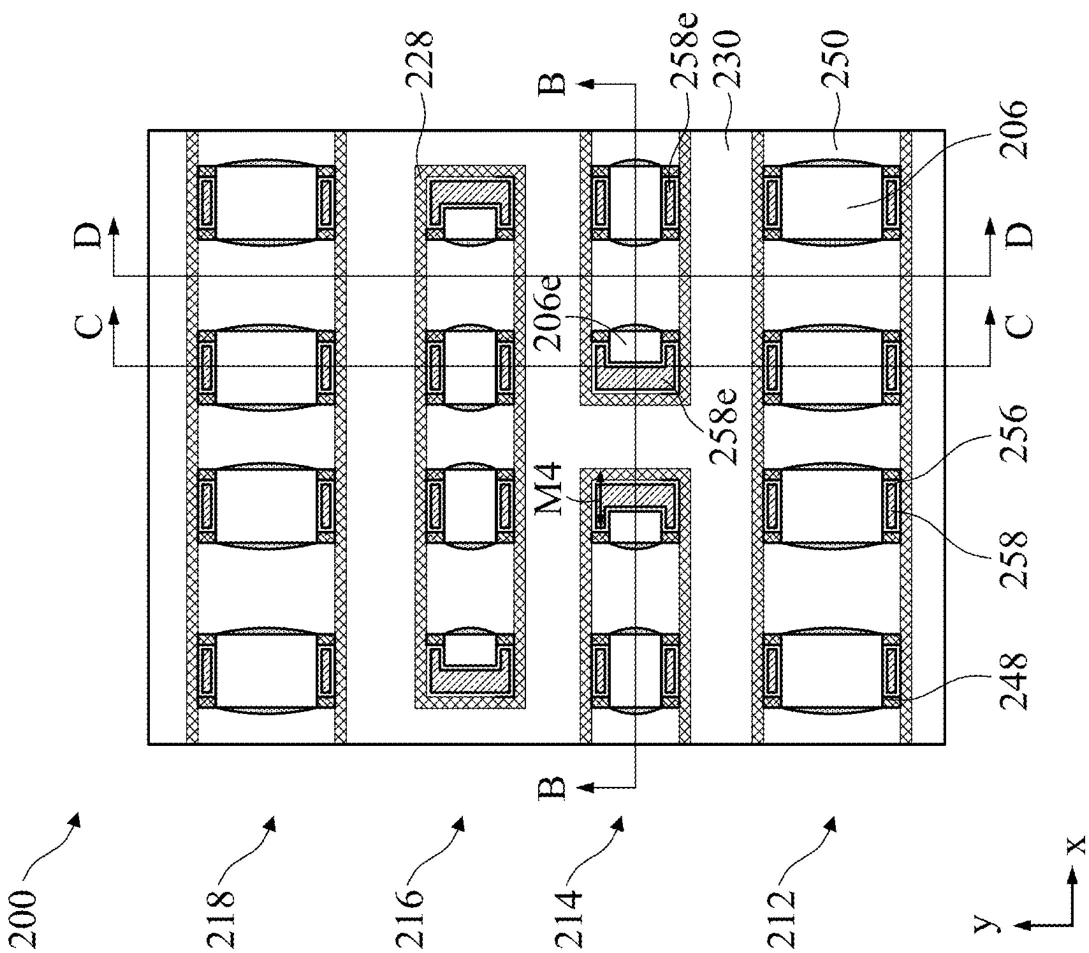
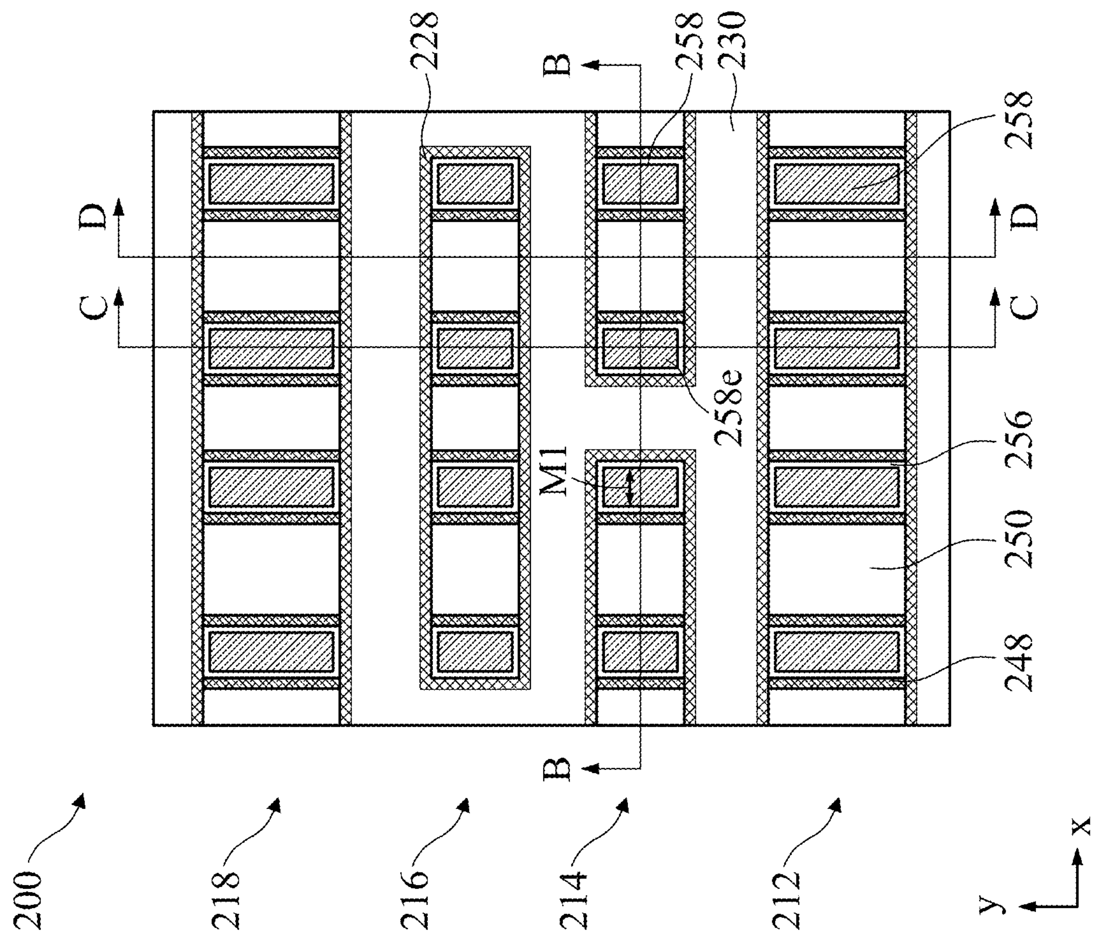

200
218
216
214
212
228
B
B
C
C
D
D
258e
230
250
206
206e
258e
M4
256
258
248
x
y

FIG. 15F



200
218
216
214
212
228
258
230
258
B
B
D
D
C
C
258e
M1
256
250
248
y
x

FIG. 15G

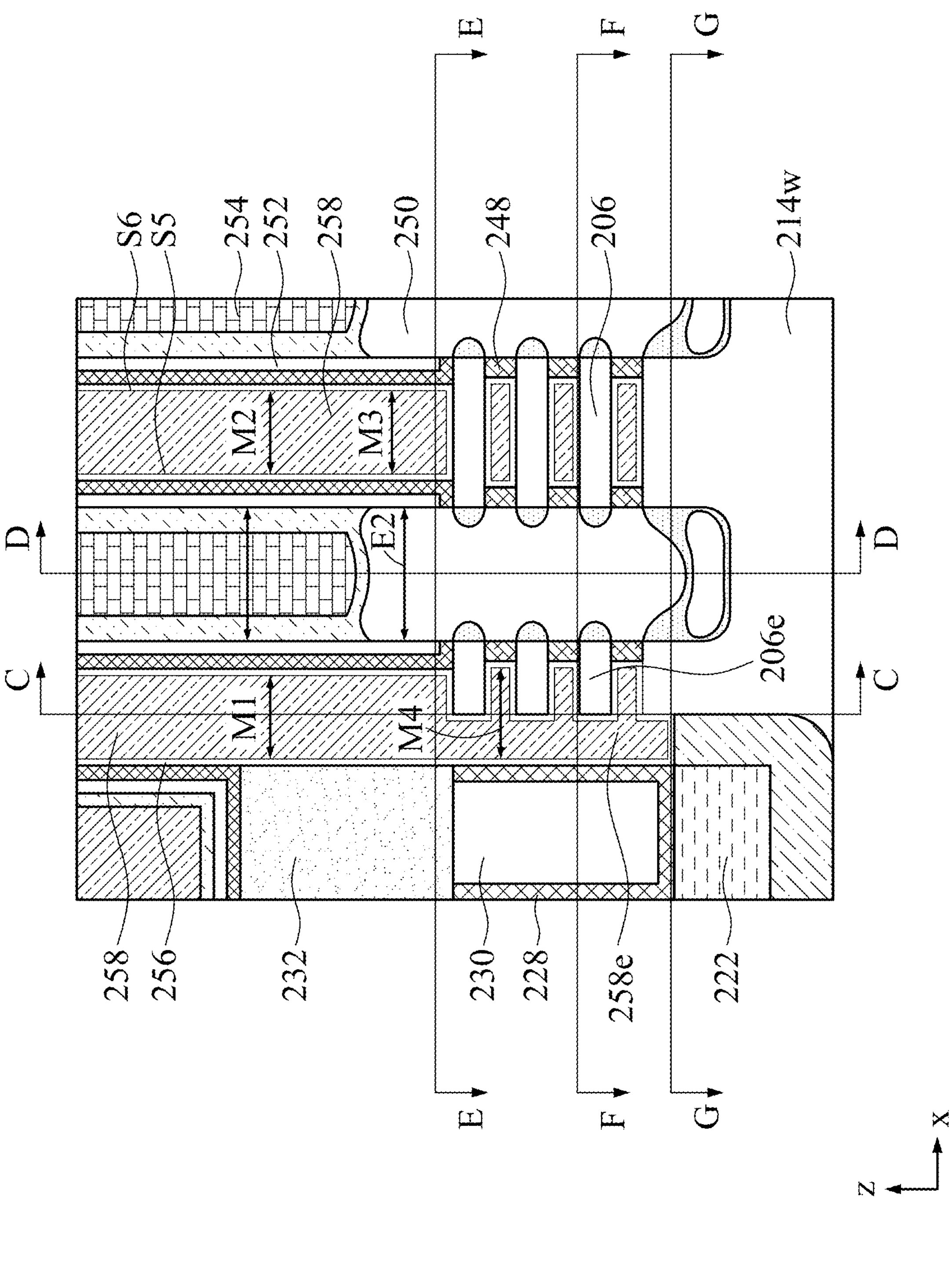

S6
S5
254
252
258
250
248
206
214w
E
F
G
D
C
M1
M2
M3
M4
E2
206e
258
256
232
230
228
258e
222
z
x

FIG. 15H

SEMICONDUCTOR DEVICES AND METHODS OF FABRICATION THEREOF

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional application of U.S. patent application Ser. No. 17/831,054 filed Jun. 2, 2022, which is incorporated by reference in its entirety.

BACKGROUND

[0002] The semiconductor industry has experienced continuous rapid growth due to constant improvements in the integration density of various electronic components. For the most part, this improvement in integration density has come from repeated reductions in minimum feature size, allowing more components to be integrated into a given chip area.

[0003] As minimum feature size reduces, the aspect ratio of sacrificial gate structures increases. The increased aspect ratio causes difficulties to fill gate electrode layer in the high aspect ratio space during replacement gate process, particularly for gate structures near dielectric fins. Therefore, there is a need to solve the above problems.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0005] FIG. **1** is a flow chart of a method for manufacturing of a semiconductor device according to embodiments of the present disclosure.

[0006] FIGS. **2**A-**2**C, **3**A-**3**C, **4**A-**4**C, **5**A-**5**C, **6**A-**6**C, **7**A-**7**C, **8**A-**8**E, **9**A-**9**D, **10**A-**10**F, **11**A-**11**E, **12**A-**12**D, **13**A-**13**B, **14**A-**14**D, and **15**A-**15**H schematically illustrate various stages of manufacturing a semiconductor device according to embodiments of the present disclosure.

DETAILED DESCRIPTION

[0007] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0008] Further, spatially relative terms, such as "beneath," "below," "lower," "above," "over," "top," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 64 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0009] The foregoing broadly outlines some aspects of embodiments described in this disclosure. While some embodiments described herein are described in the context of nanosheet channel FETs, implementations of some aspects of the present disclosure may be used in other processes and/or in other devices, such as planar FETs, Fin-FETs, Horizontal Gate All Around (HGAA) FETs, Vertical Gate All Around (VGAA) FETs, and other suitable devices. A person having ordinary skill in the art will readily understand other modifications that may be made are contemplated within the scope of this disclosure. In addition, although method embodiments may be described in a particular order, various other method embodiments may be performed in any logical order and may include fewer or more steps than what is described herein. In the present disclosure, a source/drain region(s) may refer to a source or a drain, individually or collectively dependent upon the context.

[0010] The gate all around (GAA) transistor structures may be patterned by any suitable method. For example, the structures may be patterned using one or more photolithography processes, including double-patterning or multi-patterning processes. Generally, double-patterning or multi-patterning processes combine photolithography and self-aligned processes, allowing patterns to be created that have, for example, pitches smaller than what is otherwise obtainable using a single, direct photolithography process. For example, in one embodiment, a sacrificial layer is formed over a substrate and patterned using a photolithography process. Spacers are formed alongside the patterned sacrificial layer using a self-aligned process. The sacrificial layer is then removed, and the remaining spacers may then be used to pattern the GAA structure.

[0011] Embodiments of the present disclosure provide a method for forming sacrificial gate structure over dielectric fins, such as dielectric fins with high-k dielectric tops. Embodiments of the present disclosure may be used to improve quality of contact features to gate electrodes and source/drain regions in various transistors, such as nanosheet Gate-all-around FET (GAAFET/NSFET), Forksheet FET, CFET, NS SBI. In some embodiments, a cyclic operation is used to etch sacrificial gate stacks and form sacrificial gate structures. The cyclic operation includes two or more cycles of etching and passivation. In some embodiments, the passivation process is performed with pulsing power supply.

[0012] FIG. **1** is a flow chart of a method **100** for manufacturing of a semiconductor device **200** according to embodiments of the present disclosure. FIGS. **2**A-**2**C, **3**A-**3**C, **4**A-**4**C, **5**A-**5**C, **6**A-**6**C, **7**A-**7**C, **8**A-**8**E, **9**A-**9**D, **10**A-**10**F, **11**A-**11**E, **12**A-**12**D, **13**A-**13**B, **14**A-**14**D, and **15**A-**15**H schematically illustrate various stages of manufacturing a semiconductor device according to embodiments of the present disclosure. Additional operations can be provided before, during, and after operations/processes in the method **100**, and some of the operations described below can be replaced or eliminated, for additional embodiments of the method. The order of the operations/processes may be interchangeable.

[0013] The method **100** begins at operation **102** where a plurality of semiconductor fins **212**, **214**, **216**, **218** are formed over a substrate **202**, as shown in FIGS. **2**A-**2**C. FIG. **2**A is a schematic top view of the semiconductor device **200**. FIG. **2**B is a schematic sectional view of the semiconductor device **200** along the line B-B on FIG. **2**A. FIG. **2**C is a schematic sectional view of the semiconductor device **200** along the line C-C on FIG. **2**A.

[0014] The semiconductor device **200** is built in and on the substrate **202** is provided to form a semiconductor device thereon. The substrate **202** may include a single crystalline semiconductor material such as, but not limited to Si, Ge, SiGe, GaAs, InSb, GaP, GaSb, InAlAs, InGaAs, GaSbP, GaAsSb, and InP. The substrate **202** may include various doping configurations depending on circuit design. For example, different doping profiles, e.g., n-wells, p-wells, may be formed in the substrate **202** in regions designed for different device types, such as n-type field effect transistors (nFET), and p-type field effect transistors (pFET). In some embodiments, the substrate **202** may be a silicon-on-insulator (SOI) substrate including an insulator structure (not shown) for enhancement.

[0015] A semiconductor stack **203** is formed over the substrate **202**. The semiconductor stack **203** includes alternating semiconductor layers made of different materials to facilitate formation of nanosheet channels in a multi-gate device, such as nanosheet channel FETs. In some embodiments, the semiconductor stack **203** includes first semiconductor layers **204** interposed by second semiconductor layers **206**. The first semiconductor layers **204** and second semiconductor layers **206** have different compositions. In some embodiments, the two semiconductor layers **204** and **206** provide for different oxidation rates and/or different etch selectivity. In later fabrication stages, portions of the second semiconductor layers **206** form nanosheet channels in a multi-gate device. Three first semiconductor layers **204** and three second semiconductor layers **206** are alternately arranged as illustrated in FIGS. **2**A-**2**C as an example. More or less semiconductor layers **204** and **206** may be included in the semiconductor stack **203** depending on the desired number of channels in the semiconductor device to be formed. In some embodiments, the number of semiconductor layers **204** and **206** is between 1 and 10.

[0016] In some embodiments, the first semiconductor layer **204** may include silicon germanium (SiGe). The first semiconductor layer **204** may be a SiGe layer including more than 25% Ge in molar ratio. For example, the first semiconductor layer **204** may be a SiGe layer including Ge in a molar ration in a range between 25% and 50%.

[0017] The second semiconductor layer **206** may include different materials for different types for devices. For n-type devices, the second semiconductor layer **206** may include silicon (Si). In some embodiments, the second semiconductor layer **206** may include n-type dopants, such as phosphorus (P), arsenic (As), etc. The second semiconductor layer **206** may include silicon, Ge, a compound semiconductor such as SiC, GeAs, GaP, InP, InAs, and/or InSb, an alloy semiconductor such as SiGe, GaAsP, AllnAs, AlGaAs, InGaAs, GaInP, and/or GaInAsP, or combinations thereof.

[0018] The semiconductor layers **204**, **206** may be formed by a molecular beam epitaxy (MBE) process, a metalorganic chemical vapor deposition (MOCVD) process, and/or other suitable epitaxial growth processes. Semiconductor layers **204**, **206** for n-type and p-type devices may be formed by different processes at different areas.

[0019] In some embodiments, each semiconductor layer **206** has a thickness in a range between about 5 nm and about 30 nm. The semiconductor layers **204** may eventually be removed and serve to define a vertical distance between adjacent channel regions for a subsequently formed multi-gate device. In some embodiments, the thickness of the semiconductor layer **204** is equal to or greater than the thickness of the semiconductor layer **206**. In some embodiments, each semiconductor layer **204** has a thickness in a range between about 5 nm and about 50 nm.

[0020] The semiconductor fins **212**, **214**, **216**, **218** are formed from the semiconductor stack **203**, and a portion of the substrate **202** underneath. The semiconductor fins **212**, **214**, **216**, **218** may be formed by patterning a pad layer **208** and a hard mask **210** formed on the semiconductor stack **203** and one or more etching processes. Each semiconductor fin **212**, **214**, **216**, **218** has a channel portion **212***c*, **214***c*, **216***c*, **218***c* formed from the semiconductor stack **203**, and a well portion **212***w*, **214***w*, **216***w*, **218***w* formed from the substrate **202**. In FIGS. **2**A-**2**C, the semiconductor fins **212**, **214**, **216**, **218** are formed along longitudinal axis **212***x*, **214***x*, **216***x*, **218***x* along the x-direction and substantially parallel to each other. Widths of the semiconductor fins **212**, **214**, **216**, **218** along the Y direction may be in a range between about 3 nm and about 44 nm. In some embodiments, widths of the semiconductor fins **212**, **214**, **216**, **218** may be different according to circuit design.

[0021] In some embodiments, the semiconductor device **200** may be an array of memory cells, such as a static random-access memory ("SRAM") array. The semiconductor fins **212**, **218** may be intended to be channels for n-type devices, such as pull-down transistors and pass transistors. The semiconductor fins **214**, **216** may be intended to be channels for p-type devices, such as pull-up transistors. In some embodiments, the semiconductor fins **212**, **218** may have width greater than the width of the semiconductor fins **214**, **216**. The semiconductor fins **212**, **218** may extend continuously along the x-direction for the array of memory cells. The semiconductor fins **214**, **216** may be cut into sections for each memory cell. In some embodiments, the semiconductor fins **214**, **216** may be first formed as a continuous fin. A subsequent cutting process may be performed to cut the semiconductor fins **214**, **216** into sections. As shown in FIGS. **2**A, **2**B, the semiconductor fin **214** may be cut into two sections **214***a*, **214***b*.

[0022] In operation **104**, an isolation layer **222** is formed over the substrate **202** and around the semiconductor fins **212**, **214**, **216**, **218** as shown in FIGS. **3**A-**3**C. FIG. **3**A is a schematic top view of the semiconductor device **200**. FIG. **3**B is a schematic sectional view of the semiconductor device **200** along the line B-B on FIG. **3**A. FIG. **3**C is a schematic sectional view of the semiconductor device **200** along the line C-C on FIG. **3**A.

[0023] The isolation layer **222** is formed over the substrate **202** to cover at least a part of around the well portions **212***w*, **214***w*, **216***w*, **218***w* of the semiconductor fins **212**, **214**, **216**, **218**. The isolation layer **222** may be formed by a high-density plasma chemical vapor deposition (HDP-CVD), a flowable CVD (FCVD), or other suitable deposition process. In some embodiments, a liner layer **220** may be deposited prior to deposition of the isolation layer **222**. In some embodiments, the isolation layer **222** may include silicon oxide, silicon nitride, silicon oxynitride, fluorine-doped silicate glass (FSG), a low-k dielectric, combinations thereof. The liner layer **220** may include silicon nitride, silicon oxynitride, or the like. In some embodiments, the isolation layer **222** is formed to cover the semiconductor fins **212**, **214**, **216**, **218** by a suitable deposition process to fill the trenches between the semiconductor fins **212**, **214**, **216**, **218**. The isolation layer **222** and the liner layer **220** are then recess etched using a suitable anisotropic etching process to expose the channel portions **212***c*, **214***c*, **216***c*, **218***c* of the semiconductor fins **212**, **214**, **216**, **218**. In some embodiments, the isolation layer **222** is etched to expose a portion of the well portions **212***w*, **214***w*, **216***w*, **218***w* of the semiconductor fins **212**, **214**, **216**, **218**.

[0024] In operation **106**, a cladding layer **224** is formed by an epitaxial process over exposed portion of the semiconductor fins **212**, **214**, **216**, **218** as shown in FIGS. **4**A-**4**C. FIG. **4**A is a schematic top view of the semiconductor device **200**. FIG. **4**B is a schematic sectional view of the semiconductor device **200** along the line B-B on FIG. **4**A. FIG. **4**C is a schematic sectional view of the semiconductor device **200** along the line C-C on FIG. **4**A.

[0025] In some embodiments, a semiconductor liner (not shown) may be first formed over the semiconductor fins **212**, **214**, **216**, **218** including the pad layer **208** and the hard mask **210**, and the cladding layer **224** is then formed over the semiconductor liner by an epitaxial process. In some embodiments, the cladding layer **224** includes a semiconductor material, for example SiGe. In some embodiments, the cladding layer **224** may have a composition similar to the composition of the first semiconductor layer **204**, thus may be selectively removed from the second semiconductor layer **206**.

[0026] In operation **108**, dielectric fins **226** are formed in the trenches between the neighboring semiconductor fins **212**, **214**, **216**, **218** after formation of the cladding layer **224** as shown in FIGS. **5**A-**5**C. FIG. **5**A is a schematic top view of the semiconductor device **200**. FIG. **5**B is a schematic sectional view of the semiconductor device **200** along the line B-B on FIG. **5**A. FIG. **5**C is a schematic sectional view of the semiconductor device **200** along the line C-C on FIG. **5**A.

[0027] The dielectric fins **226**, also referred to as dummy fins or hybrid fins, are dielectric materials filled the recessed spaces above the isolation layer **222** and between the semiconductor fins **212**, **214**, **216**, **218**. The dielectric fins **226** are fin like structures. Depending on circuit design, some dielectric fins **226** are parallel dielectric fins **226***p* that extend along the x-direction, parallel to the semiconductor fins **212**, **214**, **216**, **218**. These parallel dielectric fins **226***p* may function to divide gate electrodes into electrically isolated sections. Some dielectric fins **226** are perpendicular dielectric fins **226***v* that extend along the y-direction, perpendicular to the semiconductor fins **212**, **214**, **216**, **218**. These perpendicular dielectric fins **226***v* function to cut channels in the same semiconductor fin into electrically isolated sections.

[0028] The dielectric fins **226** may include one or more layers of dielectric materials, such as a high-k dielectric material layer, a low-k dielectric material layer, or a bi-layer dielectric material including high-k upper part and a low-k lower part. In some embodiments, the dielectric fins **226** include a high-k metal oxide, such as HfO_2, ZrO_2, HfAlOx, HfSiOx, Al_2O_3, and the like, a low-k material such as SiOCN, SiCN, SiOC, or other dielectric material. In the example of FIGS. **5**A-**5**C, the dielectric fin **226** may include a bi-layer lower portion and a high-k upper portion. The bi-layer lower portion includes a dielectric liner layer **228** and a dielectric filling layer **230**. In some embodiments, the dielectric liner layer **228** may include a low-k material, such as SiOCN, SiCN, SiOC, or other dielectric material, that provide etch resistance during replacement gate processes. The dielectric filling layer **230** may be a low-k dielectric material, such as silicon oxide.

[0029] The dielectric liner layer **228** may be conformally deposited over exposed surfaces, such as the isolation layer **222** and the cladding layer **224**. The dielectric filling layer **230** is then deposited over the dielectric liner layer **228** to fill the trenches. The dielectric liner layer **228** and the dielectric filling layer **230** are then recess etched. The recess may be performed by any suitable process, such as dry etch, wet etch, or a combination thereof. The etch process may be a selective etch process that does not remove the semiconductor material of the cladding layer **224**. The recess process may be controlled so that the dielectric liner layer **228** and the dielectric filling layer **230** are substantially at the same level as a top surface of the topmost second semiconductor layer **206**. As a result of the recess etch, recesses are formed between the semiconductor fins **212**, **214**, **216**, **218**.

[0030] A high-k dielectric materials is then deposited to fill the recesses. In some embodiments, the high-k dielectric features **232** are formed by a blanket deposition followed by a planarization process. The high-k dielectric features **232** may include a material having a k value greater than 7, such as HfO, TaN, Al_2O_3, SiO, SIN, SiCN, SiOCN, HfO_2, ZrO_2, HfAlOx, HfSiOx, or the similar. Any suitable deposition process, such as a CVD, PECVD, FCVD, or ALD process, may be used to deposit the high-k dielectric material. The planarization process is the performed. After the planarization, the high-k dielectric feature **232** may have a height H**1** along the z-direction. In some embodiments, the height H**1** is in a range between about 10 nm and about 30 nm.

[0031] In operation **110**, the pad layer **208** and the hard mask **210** are removed exposing the topmost semiconductor layer **206**, and the cladding layer **224** is recessed to level with a top surface **203***t* of the semiconductor stack **203**, as shown in FIGS. **6**A-**6**C. FIG. **6**A is a schematic top view of the semiconductor device **200**. FIG. **6**B is a schematic sectional view of the semiconductor device **200** along the line B-B on FIG. **6**A. FIG. **6**C is a schematic sectional view of the semiconductor device **200** along the line C-C on FIG. **6**A. The high-k dielectric features **232** protrude over the semiconductor fins **212**, **214**, **216**, **218** and the lower portion of the dielectric fins **226**. The high-k dielectric features **232** may function to separate gate structures formed over the semiconductor fins **212**, **214**, **216**, **218**.

[0032] In operation **112**, a sacrificial gate stack **234** are formed as shown in FIGS. **7**A-**7**C. FIG. **7**A is a schematic top view of the semiconductor device **200**. FIG. **7**B is a schematic sectional view of the semiconductor device **200** along the line B-B on FIG. **7**A. FIG. **7**C is a schematic sectional view of the semiconductor device **200** along the line C-C on FIG. **7**A. The sacrificial gate stack **234** is deposited over the semiconductor fins **212**, **214**, **216**, **218** and the dielectric fins **226**. The sacrificial gate stack **234** may include a sacrificial gate dielectric layer **236**, a sacrificial gate electrode layer **238**, a pad layer **240**, and a mask layer **242**.

[0033] The sacrificial gate dielectric layer **236** may be deposited conformally over the semiconductor fins **212**, **214**, **216**, **218** and the high-k dielectric features **232**. In some embodiments, the sacrificial gate dielectric layer **236** may be deposited by a CVD process, a sub-atmospheric CVD (SACVD) process, a FCVD process, an ALD process, a PVD process, or other suitable process. The sacrificial gate dielectric layer **236** may include one or more layers of dielectric material, such as SiO_2, SiN, a high-k dielectric material, and/or other suitable dielectric material. In some embodiments, the sacrificial gate dielectric layer **236** includes a material different than that of the high-k dielectric features **232**.

[0034] The sacrificial gate electrode layer **238** may be blanket deposited over the sacrificial gate dielectric layer **236**. The sacrificial gate electrode layer **238** includes silicon such as polycrystalline silicon or amorphous silicon. The thickness of the sacrificial gate electrode layer is in a range between about 70 nm and about 200 nm. In some embodiments, the sacrificial gate electrode layer **238** is subjected to a planarization operation. The sacrificial gate electrode layer **238** may be deposited using CVD, including LPCVD and PECVD, PVD, ALD, or other suitable process.

[0035] The pad layer **240** and the mask layer **242** are subsequently formed over the sacrificial gate electrode layer **238** and used to transfer a gate pattern to the sacrificial gate dielectric layer **236** and the gate electrode layer **238**.

[0036] The pad layer **240** may be a thin film comprising silicon oxide formed, for example, using a thermal oxidation process. The pad layer **240** may act as an adhesion layer between the sacrificial gate electrode layer **238** and the mask layer **242**. The pad layer **240** may also act as an etch stop layer for etching the mask layer **242**. In some embodiments, the mask layer **242** is formed of silicon nitride, for example, using low-pressure chemical vapor deposition (LPCVD) or plasma enhanced chemical vapor deposition (PECVD). The mask layer **242** is used as a hard mask during subsequent patterning processes.

[0037] In operation **114**, a gate pattern is formed over the sacrificial gate electrode layer **238** in the sacrificial gate stack **234**, as shown in FIGS. **8**A-**8**C. FIG. **8**A is a schematic top view of the semiconductor device **200**. FIG. **8**B is a schematic sectional view of the semiconductor device **200** along the line B-B on FIG. **8**A. FIG. **8**C is a schematic sectional view of the semiconductor device **200** along the line C-C on FIG. **8**A. Particularly, a gate pattern is formed in the mask layer **242** and the pad layer **240**, by one or more suitable lithographic process. As shown in FIGS. **8**A-**8**B, gate mandrels **242***g***1**, **242***g***2**, **242***g***3**, **242***g***4** (collectively **242***g*) are formed over the sacrificial gate electrode layer **238**. The gate mandrels **242***g* extend along the y-direction, substantially perpendicular to the semiconductor fins **212**, **214**, **216**, **218**. In some embodiments, the gate mandrels **242***g* have a width W**1** along the x-direction. Spacings between the gate electrodes **242***g* may have a width W**2** along the x-direction. In some embodiments, the width W**1** is substantially the same for the gate mandrels **242***g***1**, **242***g***2**, **242***g***3**, **242***g***4**. In some embodiments, the width W**1** in a range between about 5 nm and 20 nm, for example between about 10 nm and 12 nm. In some embodiments, the width W**2** in a range between about 15 nm and 40 nm, for example between about 25 nm and 35 nm.

[0038] The gate mandrel **242***g* may overlap with an end portion of the semiconductor fin **214**, **216** and adjacent the perpendicular dielectric fin **226***v*. The gate mandrel **242***g* overlapping the end portion of a semiconductor fin may be designed to form a gate structure for controlling channels in the end portions of the semiconductor fins. For example, as shown box B**1** in FIG. **8**A and box B**2** in FIG. **8**B, the gate mandrels **242***g***3** is positioned at an end portion **214***e* of the section **214***b* of the semiconductor fin **214**. The gate mandrel **242***g***3** may be positioned to flash against or slightly overlap with the perpendicular dielectric fin **226***v* between the sections **214***a*, **214***b* of the semiconductor fin **214**.

[0039] When performing an etch process to transfer the gate pattern from the gate mandrel **242***g* to the sacrificial gate electrode layer **238**, etch charge effect over the high-k dielectric features **232** induces lateral over etching of the sacrificial gate electrode layer **238** under the gate mandrel **242***g*, resulting in reduced width of the sacrificial gate structure. FIG. **8**D is a schematic cross-sectional view of a semiconductor device with over etched sacrificial gate electrode. Width of the sacrificial gate electrode near the high-k dielectric feature **232** reduces to W**1'**. In some situations, the ratio of width W**1'** over width W**1** may be as low as 0.5. To avoid defects caused by the over etch, conventional technology either widening the width W**1** of the gate mandrel over the end portion of a semiconductor fin is widened to provide allowance for over etching or under etching during pattern transferring reducing dimension of the source/drain regions between the gates. FIG. **8**E is a schematic cross-sectional view of a semiconductor device with an under etched sacrificial gate electrode. Even though under etch avoided reduction of the width W**1** of the sacrificial gate electrode, the width W**2** of the spacings between the sacrificial gate electrodes reduces to a width W**2'**. The reduced width W**2'** results in reduced volume of source/drain regions to be formed there, thus, negatively affect device performance.

[0040] Embodiments of the present disclosure provides a method for forming sacrificial gate structures to prevent lateral over etching near the dielectric fins and improve yield. The method is described in operations **116**, **118**, **120**, **122** below. Particularly, the gate pattern may be transferred from the mask layer **242** to the sacrificial gate electrode layer **238** using a bulk etching operation described in operation **116** and a cyclic fine etching described in operations **118**, **120**, and **122**. It should be noted that operations **116**, **118**, **120**, **122** may be performed continuously in the same processing tool even though the method is described in separated operations **116**, **118**, **120**, **122** for clarity.

[0041] In operation **116**, a bulk etch process is performed to etch the sacrificial gate electrode layer **238** using the gate mandrel **242***g* as a mask, as shown in FIGS. **9**A-**9**D. FIG. **9**A is a schematic top view of the semiconductor device **200**. FIG. **9**B is a schematic sectional view of the semiconductor device **200** along the line B-B on FIG. **9**A. FIG. **9**C is a schematic sectional view of the semiconductor device **200** along the line C-C on FIG. **9**A. FIG. **9**D is a schematic sectional view of the semiconductor device **200** along the line D-D on FIG. **9**A. In some embodiments, the bulk etch process is performed to expose a top surface **232***t* of the high-k dielectric features **232** or to remove the sacrificial gate electrode layer **238** above the top surface **232***t* of the high-k dielectric features **232**.

[0042] In some embodiments, the bulk etch process may be performed by a plasma etching process using an etching gas. In some embodiments, the etching gas may include Cl_2, HBr, CH_2F_2, CHF_3, CF_4, $CHClF_2$, or a combination thereof. In some embodiments, a carrier gas or dilute gas may be used with the etching gas. In some embodiments, the carrier gas or dilute gas may include helium, argon, nitrogen, or a combination thereof. In some embodiments, the flow of the etching gas and carrier gas may be in a range between about 20 sccm and about 3000 sccm. In some embodiments, the bulk etch process may be performed at a pressure in a range between about 1 mtorr to about 800 mtorr. The plasma power may be in a range between about 10 W and about 4000 W. In some embodiments, the bulk etch may be performed at an etch rate in a range between 200 angstroms per minute and 2000 angstroms per minute.

[0043] After the bulk etch in operation **116**, a cyclic fine etch process as described in operations **118**, **120**, **122** is then performed to remove sacrificial gate electrode layer **238** between the top surface **232***t* of the high-k dielectric features **232** and the top surface **203***t* of the semiconductor stack **203**. FIGS. **10**A-**10**D schematically illustrate the semiconductor device **200** in an interim stage of the cyclic fine etch process. FIG. **10**A is a schematic top view of the semiconductor device **200**. FIG. **10**B is a schematic sectional view of the semiconductor device **200** along the line B-B on FIG. **10**A. FIG. **10**C is a schematic sectional view of the semiconductor device **200** along the line C-C on FIG. **10**A. FIG. **10**D is a schematic sectional view of the semiconductor device **200** along the line D-D on FIG. **10**A. FIG. **10**E is a schematic sectional view of the semiconductor device **200** along the line B-B on FIG. **10**A showing stepped progression of the cyclic fine etch process. FIG. **10**F schematically illustrates gas and power duty cycle during one period of the cyclic fine etch process.

[0044] In some embodiments, each cycle in the cyclic fine etch includes three process steps, an etching process to be described in operation **118**, a passivation process to be described in operation **120**, and a pumping out process to be described in operation **122**. Each cycle may be performed in a time period T in a range between about 30 seconds to about 60 seconds.

[0045] In operation **118**, an etching process is performed to remove a layer of material from exposed surface. The etching process may be performed for a time period T**1**. In some embodiments, the time period T**1** may be in a range between 20 seconds and 40 seconds. In some embodiments, the time period T**1** may be in a range between about 40% and 60% of the cycle period T. In some embodiments, the etching process may be a plasma etch using a processing chemistry similar to the bulk etch in operation **116**. For example, the etching process is performed using etching gas comprising Cl_2, HBr, CH_2F_2, CHF_3, CF_4, $CHClF_2$, or a combination thereof. A carrier gas or dilute gas may be used with the etching gas. In some embodiments, the carrier gas or dilute gas may include helium, argon, nitrogen, or a combination thereof. In some embodiments, the flow of the etching gas and carrier gas may be in a range between about 20 sccm and about 3000 sccm. In some embodiments, the etching process may be performed at a pressure in a range between about 1 mtorr to about 800 mtorr. The plasma power may be in a range between about 10 W and about 4000 W. In some embodiments, the etching process may be performed at an etch rate in a range 50 angstroms per minute and 200 angstroms per minute. In some embodiments, the plasma power level in this etching process is between about 40% and about 60% of the plasma power level in operation **116**. In some embodiments, the flow rate of etch agent in this etching process is between about 40% and about 60% of the flow rate of etch agent in operation **116**. In some embodiments, the pressure in this etching process is between about 60% and about 80% of the pressure in operation **116**.

[0046] In operation **120**, a passivation process is performed for a time period T**2**. In some embodiments, the time period T**2** may be in a range between 2 seconds and 6 seconds. In some embodiments, the time period T**2** may be in a range between about 2% and 10% of the cycle period T. During passivation, a passivation film may form on exposed material, such as polycrystalline silicon in the sacrificial gate electrode layer **238**. The passivation film protects the material underneath from etching chemistry in the etching process of the subsequent cycle, therefore, preventing over etch of the sacrificial gate electrode layer **238** near the high-k dielectric features **232**. In some embodiments, the passivation process may be a plasma process using a passivation gas comprising N_2, O_2, CO_2, CH_4, SO_2, or a combination thereof. A carrier gas or dilute gas may be used with the passivation gas. In some embodiments, the carrier gas or dilute gas may include helium, argon, nitrogen, or a combination thereof. In some embodiments, the flow of the passivation gas and carrier gas may be in a range between about 20 sccm and about 3000 sccm. In some embodiments, the passivation process may be performed at a pressure in a range between about 1 mtorr to about 800 mtorr. The plasma power may be in a range between about 10 W and about 4000 W. In some embodiments, the power level during the passivation process is different from the power level during the etch step in operation **118**. For example, a ratio of the power level during the passivation process over the power level during the etch step in operation **118** is in a range between 0.8 and 1.2.

[0047] In operation **122**, a pumping out process is performed to remove reactant gas and byproducts. The pumping out process may be performed for a time period T**3**. In some embodiments, the time period T**3** may be in a range between 24 seconds and 36 seconds. In some embodiments, the time period T**3** may be in a range between about 40% and 60% of the cycle period T. In some embodiments, the time period T**2** is in a range between about 5% and about 20% of a summation of the time period T**2** and the time period T**3**. During pumping out process, the plasma power is turned off. In some embodiments, a carrier gas is continuously flowing with the passivation gas and the etching gas turned off. In some embodiments, the carrier gas or dilute gas may include helium, argon, nitrogen, or a combination thereof. In some embodiments, the flow of the carrier gas may be in a range between about 20 sccm and about 3000 sccm. In some embodiments, the pumping out process may be performed at a pressure in a range between about 1 mtorr to about 800 mtorr.

[0048] FIG. **10**F includes an example duty cycle of the cyclic fine etch according to the present disclosure. FIG. **10**E schematically illustrates the cyclic fine etch with five etch, passivation and pumping cycles. More or less cycles may be used according to etch thickness and aspect ratio.

[0049] The cyclic fine etch is performed in cycles until complete the formation of sacrificial gate structures **2341**, **2342**. **2343**. **2344** as shown FIGS. **11**A-**11**E. FIG. **11**A is a schematic top view of the semiconductor device **200**. FIG. **11**B is a schematic sectional view of the semiconductor device **200** along the line B-B on FIG. **11**A. FIG. **11**C is a schematic sectional view of the semiconductor device **200** along the line C-C on FIG. **11**A. FIG. **11**D is a schematic sectional view of the semiconductor device **200** along the line D-D on FIG. **11**A. FIG. **11**E is a schematic enlarged partial view of FIG. **11**B showing dimension of the sacrificial gate structures $\mathbf{234}_2$. $\mathbf{234}_3$. In the area shown in FIG. **11**E, the sacrificial gate structure **2342** has one side **S1** flushed against the dielectric fin **226** and another side **S2** facing a side S4 of the sacrificial gate structures $\mathbf{234}_3$ while both sides S3 and S4 of the sacrificial gate structures $\mathbf{234}_3$ are not flushed against any dielectric fins **226**. As noted in FIG. **11**E, the sacrificial gate structures $\mathbf{234}_2$ has a width D**1** and the sacrificial gate structures $\mathbf{234}_3$ has a width D**2** at the level of the top surface **232***t* of the high-k dielectric feature **232**. Because the cyclic fine etching described above has prevented over etching on the side **S1** of the sacrificial gate structures $\mathbf{234}_2$ near the top surface **232***t*, the width D**1** is substantially equal to the width D**2**. In some embodiments, the difference between width D**1** and width D**2** is less than about 5% of the width D**2**. In some embodiments, a ratio of the width D**1** over the width D**2** is in a range between 0.9 and 1.1. The sacrificial gate structures $\mathbf{234}_3$ has a width D**3** at a level between the top surface **232***t* and the top surface **203***t*. Because the cyclic fine etching described above has prevented under etching of the sacrificial gate structures $\mathbf{234}_3$, the width D**3** is substantially equal to the width D**2**. In some embodiments, the difference between width D**3** and width D**2** is less than about 5% of the width D**2**. In some embodiments, a ratio of the width D**3** over the width D**2** is in a range between 0.9 and 1.0. In some embodiments, the widths D**1**, D**2**, D**3** are in a range between 14 nm and 16 nm. Because there is no under etch of the sacrificial gate structures $\mathbf{234}_3$, the sides S3 and S4 of the sacrificial gate structures **2343** are substantially parallel to each other.

[0050] In operation **124**, sidewall spacers **244** are formed on sidewalls of each sacrificial gate structure **234**, as shown in FIGS. **12**A-**12**D. FIG. **12**A is a schematic top view of the semiconductor device **200**. FIG. **12**B is a schematic sectional view of the semiconductor device **200** along the line B-B on FIG. **12**A. FIG. **12**C is a schematic sectional view of the semiconductor device **200** along the line C-C on FIG. **12**A. FIG. **12**D is a schematic sectional view of the semiconductor device **200** along the line D-D on FIG. **12**A. After the sacrificial gate structure **234** is formed, the sidewall spacers **244** are formed by a blanket deposition of an insulating material followed by anisotropic etch to remove insulating material from horizontal surfaces. The sidewall spacers **244** may include one or more layers of dielectric materials. In some embodiments, the sidewall spacers **244** may have a thickness in a range between about 4 nm and about 7 nm. In some embodiments, the insulating material of the sidewall spacers **244** is a silicon nitride-based material, such as SiN, SiON, SiOCN or SiCN and combinations thereof.

[0051] In operation **126**, source/drain recesses **246** are formed, as shown in FIG. **12**A-**12**D. The semiconductor fins **212**, **214**, **216**, **218** and the cladding layer **224** not covered by the sacrificial gate stack **234** are etched forming source/drain recesses **246** between the neighboring dielectric fins **226** on either side of the sacrificial gate structure **234**. The source/drain recesses **246** extend into the well portions **212***w*, **214***w*, **216***w*, **218***w* of the semiconductor fins **212**, **214**, **216**, **218**.

[0052] In operation **128**, inner spacers **248** are formed as shown in FIGS. **13**A-**13**D. FIG. **13**A is a schematic top view of the semiconductor device **200**. FIG. **13**B is a schematic sectional view of the semiconductor device **200** along the line B-B on FIG. **13**A.

[0053] The first semiconductor layers **204** and the cladding layers **224** exposed to the source/drain recesses **246** are first etched to form spacer cavities for the inner spacers **248**. The first semiconductor layers **204** and cladding layer **224** are etched horizontally along the X direction to form cavities. In some embodiments, the first semiconductor layers **204** can be selectively etched by using a wet etchant such as, but not limited to, ammonium hydroxide (NH_4OH), tetramethylammonium hydroxide (TMAH), ethylenediamine pyrocatechol (EDP), or potassium hydroxide (KOH) solutions. In some embodiments, an etching thickness of the first semiconductor layer **204** and the cladding layer **224** is in a range between about 2 nm and about 10 nm along the X direction. The inner spacers **248** are formed in the spacer cavities by conformally deposit and then partially remove an insulating layer. The insulating layer can be formed by ALD or any other suitable method. The subsequent etch process removes most of the insulating layer except inside the cavities, resulting in the inner spacers **248**. In some embodiments, the inner spacers **248** may include one of silicon nitride (SiN) and silicon oxide (SiO_2), SiOCN, or a combination thereof. The inner spacers **248** have a thickness along the x-direction in a range from about 4 nm to about 7 nm.

[0054] In operation **130**, epitaxial source/drain regions **250** are formed in the source/drain recesses **246**, as shown in FIGS. **14**A-**14**D. FIG. **14**A is a schematic top view of the semiconductor device **200**. FIG. **14**B is a schematic sectional view of the semiconductor device **200** along the line B-B on FIG. **14**A. FIG. **14**C is a schematic sectional view of the semiconductor device **200** along the line C-C on FIG. **14**A. FIG. **14**D is a schematic sectional view of the semiconductor device **200** along the line D-D on FIG. **14**A.

[0055] For n-type devices, the epitaxial source/drain regions **250** may include one or more layers of Si, SiP, SiC and SiCP. The epitaxial source/drain regions **250** also include n-type dopants, such as phosphorus (P), arsenic (As), etc. In some embodiments, the epitaxial source/drain regions **250** may be a Si layer includes phosphorus dopants. For p-type devices, the epitaxial source/drain regions **250** may include one or more layers of Si, SiGe, Ge with p-type dopants, such as boron (B). In some embodiments, the epitaxial source/drain regions **250** may be SiGeB material, wherein boron is a dopant.

[0056] It should be noted that operations **126**, **128**, and **130** may be performed separately for n-type devices and p-type devices, using suitable masks.

[0057] In operation **132**, a contact etch stop layer (CESL) **252** and an interlayer dielectric (ILD) layer **254** are formed over the exposed surfaces as shown in FIGS. **14**A-**14**D. The CESL **252** is formed on the epitaxial source/drain regions **250**, the sidewall spacers **244**, and the high-k dielectric features **232**. In some embodiments, the CESL **252** has a thickness in a range between about 4 nm and about 7 nm.

The CESL **252** may include $SisN_4$, SiON, SiCN or any other suitable material, and may be formed by CVD, PVD, or ALD.

[0058] The interlayer dielectric (ILD) layer **254** is formed over the CESL **252**. The materials for the ILD layer **254** include compounds comprising Si, O, C, and/or H, such as silicon oxide, SiCOH and SiOC. Organic materials, such as polymers, may be used for the ILD layer **254**. The ILD layer **254** protects the epitaxial source/drain regions **250** during the removal of the sacrificial gate stack **234**. A planarization operation, such as CMP, is performed to expose the sacrificial gate electrode layer **238** for subsequent removal of the sacrificial gate stack **234**. The planarization process removes portions of the ILD layer **254** and the CESL **252**, the hard mask layer **242** and the pad layer **240** to expose the sacrificial gate electrode layer **238**.

[0059] In operation **134**, the sacrificial gate dielectric layer **236** and the sacrificial gate electrode layer **238** are removed and replacement gate structures are formed therein, as shown in FIGS. **15**A-**15**G. FIG. **15**A is a schematic top view of the semiconductor device **200**. FIGS. **15**B-G are schematic sectional view of the semiconductor device **200** along the lines B-B, C-C, D-D, E-E, F-F, and G-G on various views. FIG. **15**H is a partial enlarged view of FIG. **15**B.

[0060] The sacrificial gate electrode layer **238** can be removed using plasma dry etching and/or wet etching. When the sacrificial gate electrode layer **238** is polysilicon, a wet etchant such as a Tetramethylammonium hydroxide (TMAH) solution can be used to selectively remove the sacrificial gate electrode layer **238** without removing the dielectric materials in the ILD layer **254** and the CESL **252**.

[0061] After removal of the sacrificial gate electrode layer **238**, the sacrificial gate dielectric layer **236** is exposed. An etch process may be performed to selectively remove the sacrificial gate dielectric layer **236** exposing the high-k dielectric features **232**, and the top layer of the second semiconductor layers **206**. A suitable etch process is then performed to selective remove the cladding layers **224**. The cladding layer **224** can be removed using plasma dry etching and/or wet etching. After removal of the cladding layers **224**, the first semiconductor layers **204** are exposed and subsequently removed resulting in gate cavities having nanosheets of the second semiconductor layers **206**. In some embodiments, the first semiconductor layers **204** can be removed during the same etch process for removal of the cladding layers **224**. In other embodiments, the first semiconductor layers **204** can be selectively removed using a wet etchant such as, but not limited to, ammonium hydroxide (NH_4OH), tetramethylammonium hydroxide (TMAH), ethylenediamine pyrocatechol (EDP), or potassium hydroxide (KOH) solution.

[0062] A gate dielectric layers **256** and gate electrode layer **258** are formed in the gate cavities. The gate dielectric layer **256** and the gate electrode layer **258** may be referred to as a replacement gate structure. The gate dielectric layers **256** for n-type devices and p-type devices may have different composition and dimensions and are formed separately using patterned mask layers and different deposition recipes.

[0063] The gate dielectric layer **256** may include one or more layers of a dielectric material, such as silicon oxide, silicon nitride, or high-k dielectric material, other suitable dielectric material, and/or combinations thereof. Examples of high-k dielectric material include HfO_2, HfSiO, HfSiON, HfTaO, HfTiO, HfZrO, zirconium oxide, aluminum oxide, titanium oxide, hafnium dioxide-alumina (HfO_2—Al_2O_3) alloy, other suitable high-k dielectric materials, and/or combinations thereof.

[0064] The gate dielectric layer **256** is formed on exposed surfaces of each nanosheet of the second semiconductor layer **206**, exposed surfaces of the inner spacer **248**, exposed surfaces of the sidewall spacer **244**, and exposed surfaces of the epitaxial features **250**. The gate dielectric layers **256** may be formed by CVD, ALD or any suitable method. In one embodiment, the gate layers **256** are formed using a highly conformal deposition process such as ALD in order to ensure the formation of the gate dielectric layers **256** having a uniform thickness around each of the semiconductor layers **206**. In some embodiments, the thickness of the gate dielectric layers **256** is in a range between about 1 nm and about 6 nm. In some embodiments, an interfacial layer (not shown) is formed between the semiconductor layers **206** and the gate dielectric layers **256**.

[0065] The gate electrode layer **258** is then formed on the gate dielectric layers **256** to fill the gate cavities. The gate electrode layer **258** includes one or more layers of conductive material, such as polysilicon, aluminum, copper, titanium, tantalum, tungsten, cobalt, molybdenum, tantalum nitride, nickel silicide, cobalt silicide, TiN, WN, TiAl, TiAlN, TaCN, TaC, TaSiN, metal alloys, other suitable materials, and/or combinations thereof. In some embodiments, the gate electrode layer **258** may be formed by CVD, ALD, electro-plating, or other suitable method. After the formation of the gate electrode layer **258**, a planarization process, such as a CMP process, is performed to remove excess deposition of the gate electrode material and expose the top surface of the ILD layer **254**. Subsequently, conductive contact features may selective be formed in the ILD layer **254** to connect the source/drain regions **250**. An interconnect structure may be then formed over on a second ILD layer to with conductive routes for signal lines and power lines.

[0066] As shown in FIGS. **15**B, **15**C, **15**F, and **15**H, an end gate electrode layer **258*e*** is formed adjacent to the perpendicular dielectric fin **226*v*** and wraps around end portions **206*e*** of the semiconductor layers **206**. As shown in FIG. **15**F, the end gate electrode layer **258*e*** has a U-shape cross section along a plane of a channel layer, or a x-y plane, such as the semiconductor layer **206**. The U-shape portion of the end gate electrode layer **258*e*** wraps the end portion **206*e*** from three sides. Structures similar to the end gate electrode layer **258*e*** may be used in various devices, such as the butt connection in SRAM cell. The end gate electrode layer **258*e*** is prune to have voids or undesireable seams therein because a high-k dielectric feature, such as the high-k dielectric feature **232**, causes over etching of the sacrificial gate structure, which subsequently results in a cavity with a choked entrance for filling the end gate electrode layer **258*e***. By using the process described in operations **116**, **118**, **120**, **122**, embodiments of the present disclosure, the sacrificial gate electrode layer **238** is not over etched near the high-k dielectric feature **232**. When the sacrificial gate electrode layer **238** is removed in operation **134**, the gate cavity is not choked near the high-k dielectric features **232**, and the end gate electrode layer **258*e*** is formed without any voids or seams. As shown in FIG. **15**H, the end gate electrode layer **258*e*** has a width **M1** and a normal gate electrode layer **258** has a width **M2** at the level near the high-k dielectric feature **232**. In some embodiments, the width **M1** is substantially equal to the width M2. In some embodiments, the difference between width M1 and width M2 is less than about 5% of the width M2. In some embodiments, a ratio of the width M1 over the width M2 is in a range between 0.9 and 1.1. Additionally, the gate electrode layer **258** also has substantially vertical sidewalls S5, S6 along the y-z plane. As a result, a width M3 at the level of source/drain regions **250** is substantially equal to the width M2. In some embodiments, the difference between width M3 and width M2 is less than about 5% of the width M2. In some embodiments, a ratio of the width M3 over the width M2 is in a range between 0.9 and 1.0. In some embodiments, the widths M1, M2, M3 are in a range between 10 nm and 12 nm. As shown in FIG. **15**F, the U-shape of the end gate electrode layer **258***e* also has a width M4. In some embodiments, the difference between width M4 and width M2 is less than about 5% of the width M2. In some embodiments, a ratio of the width M4 over the width M2 is in a range between 0.9 and 1.1.

[0067] The substantially vertical sidewalls S5, S6 of the gate electrode layer **258** also avoid narrowing of the epitaxial source/drain regions **250**. As shown in FIG. **15**H, the opening of source/drain regions has a width E1 at the level near the high-k dielectric feature **232** and a width E2 at the level of the semiconductor layers **206** along the x-direction. In some embodiments, the width E1 is substantially equal to the width E2. In some embodiments, the difference between width E1 and width E2 is less than about 5% of the width E2. In some embodiments, a ratio of the width E1 over the width E2 is in a range between 1.0 and 1.1.

[0068] Even though a GAA device with multiple channels is described above, embodiments of the present disclosure may be used in single channel devices, such as FinFET device.

[0069] Various embodiments or examples described herein offer multiple advantages over the state-of-art technology. Embodiments of the present disclosure solve the problems of failed gate electrode layer at an end of channel region, thus increasing yield. The cyclic etching, passivation and pumping out process prevents over etching of the sacrificial gate electrode, particularly when near a high-k dielectric feature, thus, enlarging filling windows for replacement gate structures, thus improving channel control. Compared to state-of-art solutions, embodiments of the present disclosure also enlarge volume of source/drain region, thus improving device performance.

[0070] It will be understood that not all advantages have been necessarily discussed herein, no particular advantage is required for all embodiments or examples, and other embodiments or examples may offer different advantages.

[0071] Some embodiments of the present provide a method. The method comprises forming a semiconductor fin having a longitudinal axis along a first direction; wherein the semiconductor fin has a first end, forming a dielectric fin against the first end of the semiconductor fin, wherein the dielectric fin includes a high-k dielectric feature; depositing a sacrificial gate stack over the semiconductor fin and the dielectric fin; forming a gate pattern over the sacrificial gate stack, wherein the gate pattern includes a first mandrel and a second mandrel along a second direction substantially perpendicular to the first direction; etching the sacrificial gate stack using the gate pattern until a top surface of the high-k dielectric feature is exposed; performing a cyclic process to expose a top surface of the semiconductor fin, wherein the cyclic process comprises two or more cycles of: performing an etching process; and performing a passivation process; and forming sidewall spacers; etching the semiconductor fin to form source/drain recesses; forming source/drain regions in the source/drain recesses; and replacing the sacrificial gate stack with a gate dielectric layer and a gate electrode.

[0072] Some embodiments of the present disclosure provide a method. The method comprises depositing a semiconductor stack over a substrate, wherein the semiconductor stack comprises alternatively arranged first semiconductor layers and second semiconductor layers; etching the semiconductor stack and the substrate to form a first semiconductor fin and a second semiconductor fin, wherein the first and second semiconductor fins share a longitudinal axis along a first direction and are separated by a recess; forming a cladding layer on sidewalls of the first and second semiconductor fins; forming a dielectric fin in the recess between the first and second semiconductor fins, wherein the dielectric fin include a high-k dielectric feature; depositing a sacrificial gate stack over the first and second semiconductor fins and the dielectric fin; performing a cyclic process to etch the sacrificial gate stack and form a first sacrificial gate structure and a second sacrificial gate structure, wherein the first sacrificial gate structure overlaps an end portion of the first semiconductor fin and the dielectric fin, the second sacrficial gate structure and dielectric fin are disposed on opposite sides of the first sacrificial gate structure, and the cyclic process comprises two or more cycles of: an etching process; a passivation process; and a pumping out process; forming sidewall spacers on sidewalls of the first and second sacrificial gate structures; and replacing the first sacrificial gate structure and second sacrificial gate structure with a first gate structure and a second gate structure.

[0073] Some embodiments of the present disclosure provide a semiconductor device, comprising a first source/drain region; a second source/drain region; a dielectric fin comprising a high-k dielectric feature, wherein the dielectric fin, the first source/drain region and the second source/drain region are positioned along an axis along a first direction; a first semiconductor channel disposed between and in contact with the first and second source/drain regions; a semiconductor channel extending from the first source/drain region towards the dielectric fin; a first gate structure extending along a second direction substantially perpendicular to the first direction, wherein the first gate structure is disposed between the first and second source/drain regions and surrounds the first semiconductor channel; and a second gate structure extending along the second direction, wherein the second gate structure is disposed between the first source/drain region and the dielectric fin and surrounds the second semiconductor channel, wherein the second gate structure has a first width along the first direction at a level of a top surface the high-k dielectric feature, the first gate structure has a second width along the first direction at the level of the top surface of the high-k dielectric feature and a third width along the first direction at a level of the first source/drain region, a ratio of the first width over the second width is in a range between 0.9 and 1.1, and a ratio of the third width over the second width is in a range between 0.9 and 1.0.

[0074] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

1. A semiconductor device, comprising:
- a first source/drain region;
- a second source/drain region;
- a dielectric fin comprising a high-k dielectric feature, wherein the dielectric fin, the first source/drain region and the second source/drain region are positioned along an axis along a first direction;
- a first semiconductor channel disposed between and in contact with the first and second source/drain regions;
- a second semiconductor channel extending from the first source/drain region towards the dielectric fin;
- a first gate structure extending along a second direction substantially perpendicular to the first direction, wherein the first gate structure is disposed between the first and second source/drain regions and surrounds the first semiconductor channel; and
- a second gate structure extending along the second direction, wherein the second gate structure is disposed between the first source/drain region and the dielectric fin and surrounds the second semiconductor channel,
- wherein the second gate structure has a first width along the first direction at a level of a top surface the high-k dielectric feature, the first gate structure has a second width along the first direction at the level of the top surface of the high-k dielectric feature and a third width along the first direction at a level of the first source/drain region, a ratio of the first width over the second width is in a range between 0.9 and 1.1, and a ratio of the third width over the second width is in a range between 0.9 and 1.0.

2. The semiconductor device of claim **1**, wherein the first width is in a range between 10 nm and 12 nm.

3. The semiconductor device of claim **1**, wherein the first semiconductor channel and the second semiconductor channel each comprises two or more vertically stacked semiconductor layers.

4. The semiconductor device of claim of **3**, wherein the second gate structure has a U-shape cross section along a plane defined by the first direction and second direction and wraps an end portion of the second semiconductor channel from three sides.

5. The semiconductor device of claim **4**, wherein the second gate structure has a fourth width, and a ratio of the fourth width over the second width is in a range between 0.9 and 1.1.

6. A semiconductor device, comprising:
- a first source/drain region;
- a second source/drain region, wherein the first source/drain region and the second source/drain region are positioned along an axis along a first direction;
- a first gate structure;
- a second gate structure;
- a third gate structure;
- a fourth gate structure, wherein the first, second, third, and fourth gate structures extend along a second direction substantially perpendicular to the first direction, the source/drain region is disposed between the first and second gate structures, and the second source/drain region is disposed between the third and the fourth gate structure; and
- a dielectric structure disposed between the second and third gate structure, wherein the dielectric structure comprises:
  - a lower portion comprising a low-k dielectric material; and
  - an upper portion comprising a high-k dielectric material.

7. The semiconductor device of claim **6**, wherein a top surface of the upper portion of the dielectric structure is above a top surface of the first source/drain region, and a bottom surface of the upper portion of the dielectric structure is lower than the top surface of the first source/drain region.

8. The semiconductor device of claim **6**, wherein the lower portion comprises:
- a dielectric liner layer; and
- a dielectric filling layer.

9. The semiconductor device of claim **6**, wherein the second gate structure comprises:
- a gate dielectric layer;
- a gate electrode layer; and
- a gate sidewall spacer layer, wherein the gate dielectric layer is in contact with sidewalls of the dielectric structure, and the gate sidewall spacer is in contact with a top surface of the upper portion of the dielectric structure.

10. The semiconductor device of claim **6**, further comprising
- a first semiconductor channel in contact with the first source/drain region, wherein the first gate structure is formed around the first semiconductor channel; and
- a second semiconductor channel in contact with the first source/drain region, wherein the second gate structure is formed around the second semiconductor channel.

11. The semiconductor device of claim **10**, wherein the second gate structure has a U-shape cross section along a plane defined by the first direction and second direction and wraps an end portion of the second semiconductor channel from three sides.

12. The semiconductor device of claim **11**, wherein the second gate structure has a first width along the first direction at a top surface of the dielectric structure, a second width along the first direction a top surface of the first source/drain region, and a ratio of the first width over the second width is in a range between 0.9 and 1.1.

13. The semiconductor device of claim **11**, wherein the first semiconductor channel and the second semiconductor channel each comprises two or more vertically stacked semiconductor layers.

14. A semiconductor device, comprising:
- a first source/drain region;
- a second source/drain region;
- a dielectric structure comprising a high-k dielectric feature, wherein the dielectric structure, the first source/drain region and the second source/drain region are positioned along an axis along a first direction;
- a first semiconductor channel disposed between the first and second source/drain regions;
- a second semiconductor channel extending from the first source/drain region towards the dielectric structure;

a first gate structure extending along a second direction substantially perpendicular to the first direction, wherein the first gate structure is disposed between the first and second source/drain regions and surrounds the first semiconductor channel; and

a second gate structure extending along the second direction, wherein the second gate structure is disposed between the first source/drain region and the dielectric structure and surrounds the second semiconductor channel, the second gate structure has a U-shape cross section along a plane defined by the first direction and second direction and wraps an end portion of the second semiconductor channel from three sides.

15. The semiconductor device of claim **14**, wherein the dielectric structure comprises:

a lower portion comprising a low-k dielectric material; and

an upper portion comprising a high-k dielectric material.

16. The semiconductor device of claim **15**, wherein the lower portion comprises:

a dielectric liner layer; and

a dielectric filling layer.

17. The semiconductor device of claim **15**, wherein a top surface of the upper portion of the dielectric structure is above a top surface of the first source/drain region.

18. The semiconductor device of claim **17**, wherein the second gate structure comprises:

a gate dielectric layer;

a gate electrode layer; and

a gate sidewall spacer layer, wherein the gate dielectric layer is in contact with sidewalls of the dielectric structure, and the gate sidewall spacer is in contact with a top surface of the upper portion of the dielectric structure.

19. The semiconductor device of claim **18**, further comprising an etch stop layer disposed over the top surface of the upper portion of the dielectric structure.

20. The semiconductor device of claim **14**, wherein the first semiconductor channel and the second semiconductor channel each comprises two or more vertically stacked semiconductor layers.

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