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Hyun et al.

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(54) **TIME DOMAIN ANALOG-TO-DIGITAL CONVERTER AND ANALOG-TO-DIGITAL CONVERTING METHOD**

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H03M 1/12 (2006.01)

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CPC **H03M 1/38** (2013.01); **H03M 1/245** (2013.01)

(58) **Field of Classification Search**
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(Continued)

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Primary Examiner — Peguy Jean Pierre

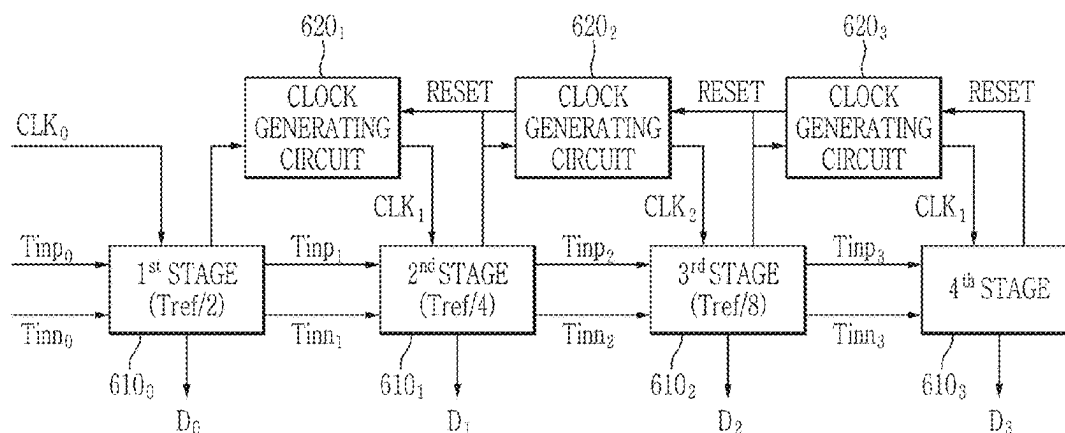
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(57) **ABSTRACT**

In analog-to-digital conversion, a plurality of stages configured in a sequence to sequentially decide a plurality of bits in successive-approximation, each of the plurality of stages configured to operate in response to a corresponding clock among a plurality of clocks, and decide a corresponding bit among the plurality of bits from a corresponding positive pulse among a plurality of positive pulses and a corresponding negative pulse among a plurality of negative pulses; and a plurality of clock generating circuits respectively corresponding to a plurality of first stages among the plurality of stages, each of the plurality of clock generating circuit configured to generate the corresponding clock of a corresponding stage among the plurality of first stages based on an operation of a previous stage among the plurality of stages, the previous stage being before the corresponding stage in the sequence.

20 Claims, 11 Drawing Sheets

600



(58) **Field of Classification Search**

USPC 341/161, 155

See application file for complete search history.

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FIG. 1

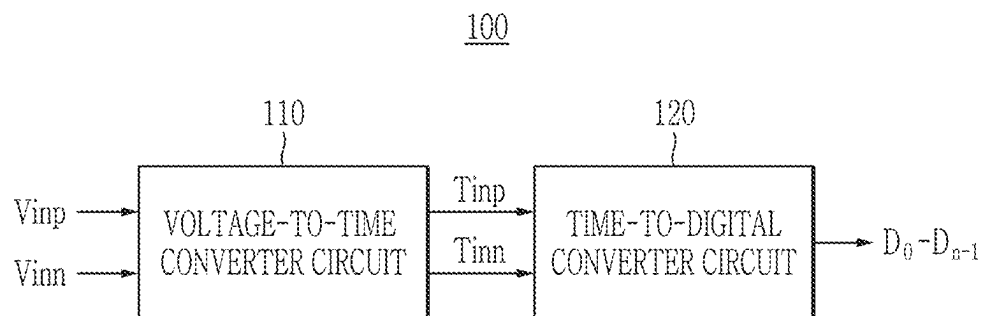


FIG. 2

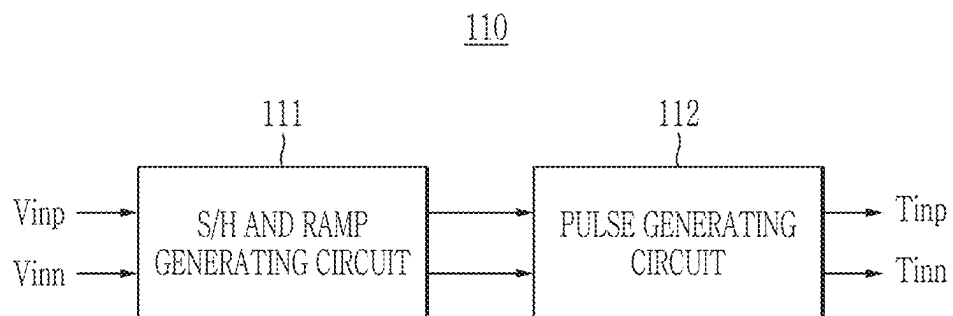


FIG. 3

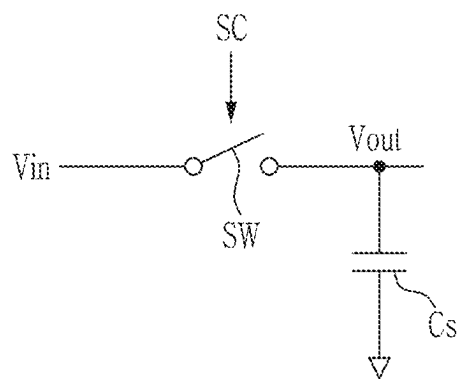


FIG. 4

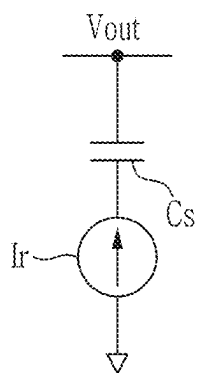


FIG. 5

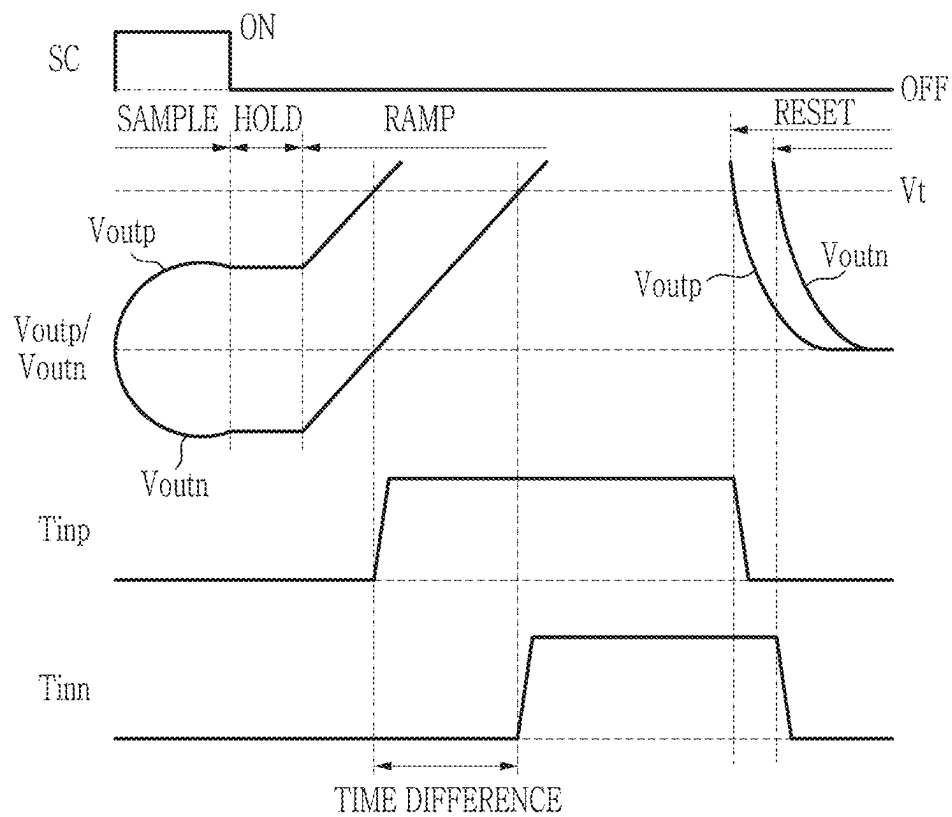


FIG. 6

600

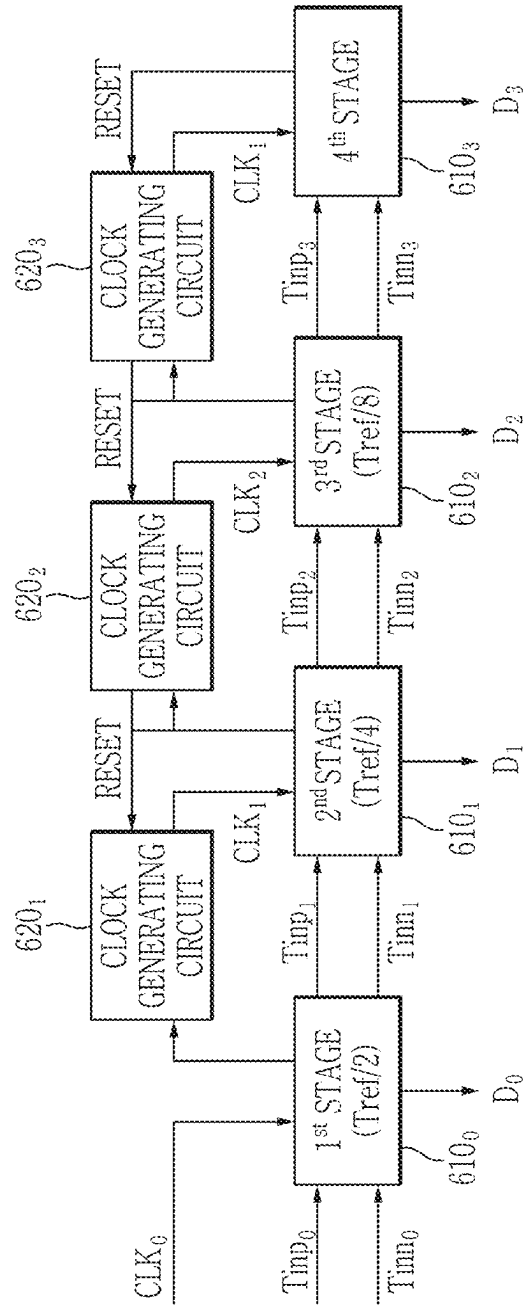


FIG. 7

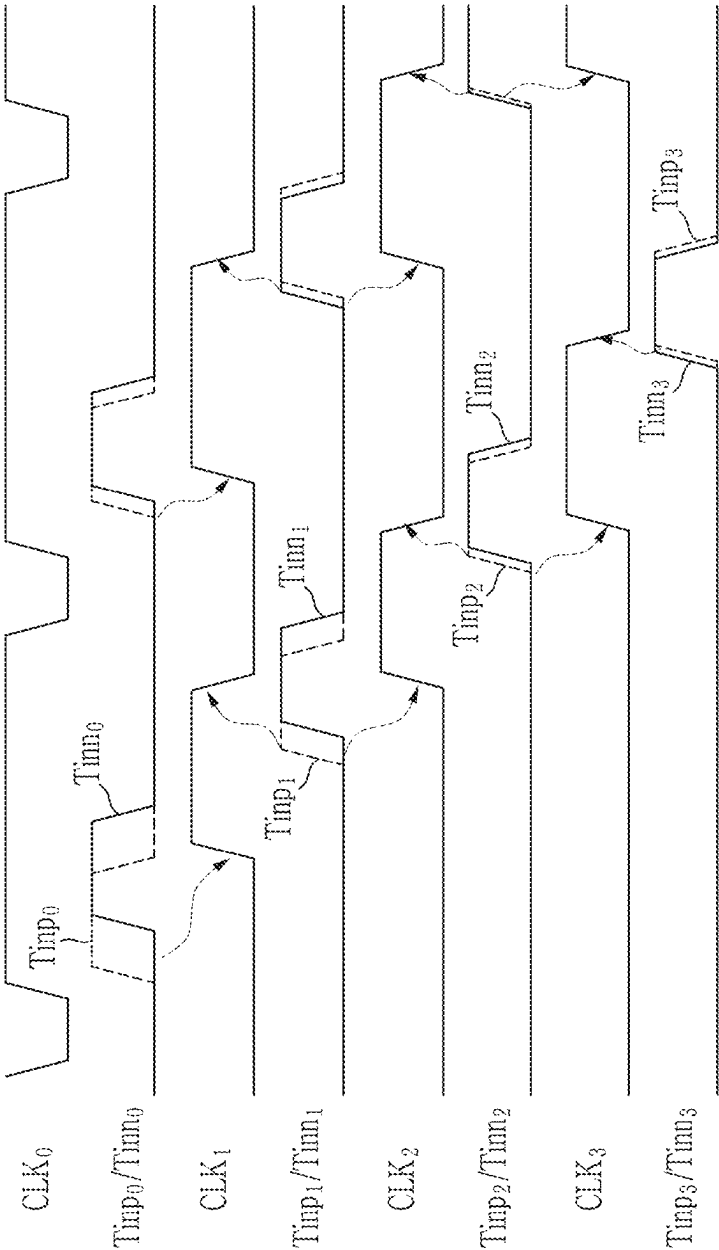


FIG. 8

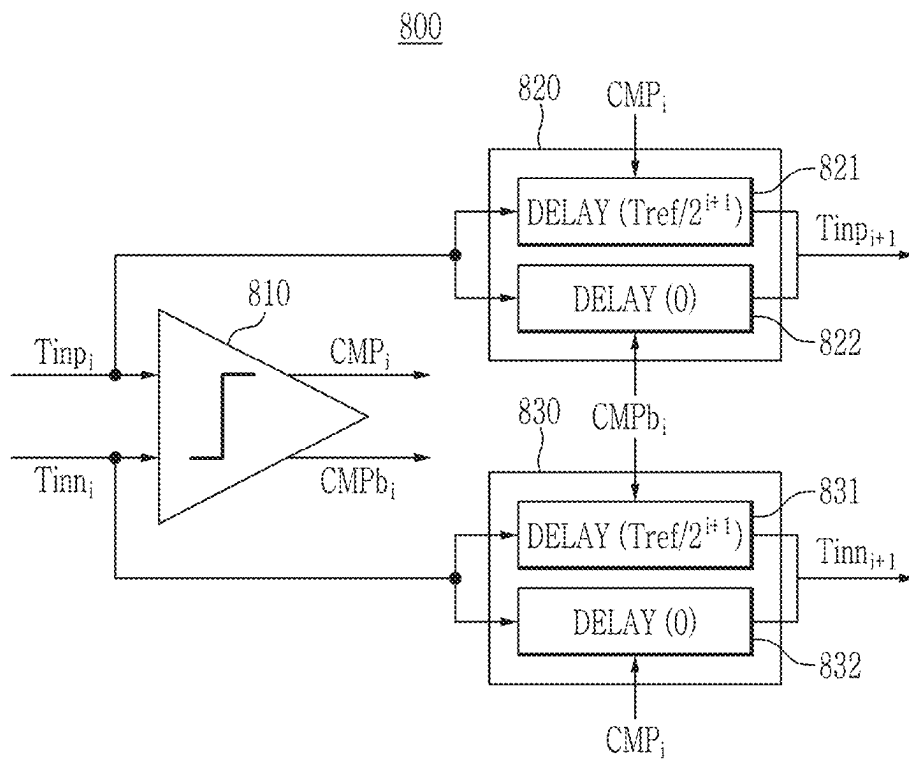


FIG. 9

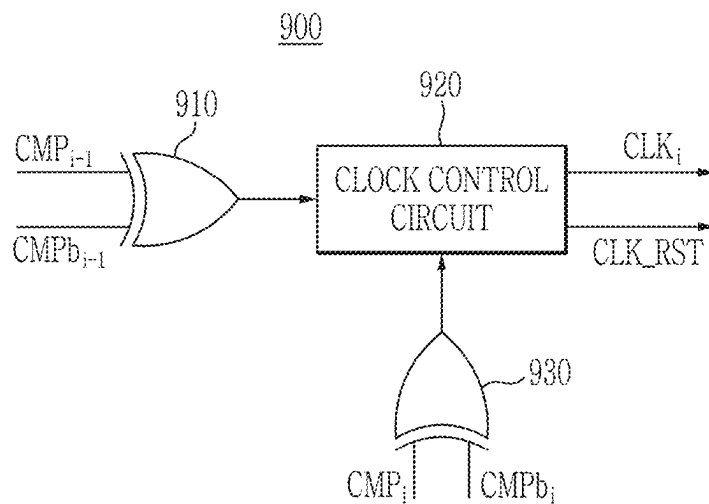


FIG. 10

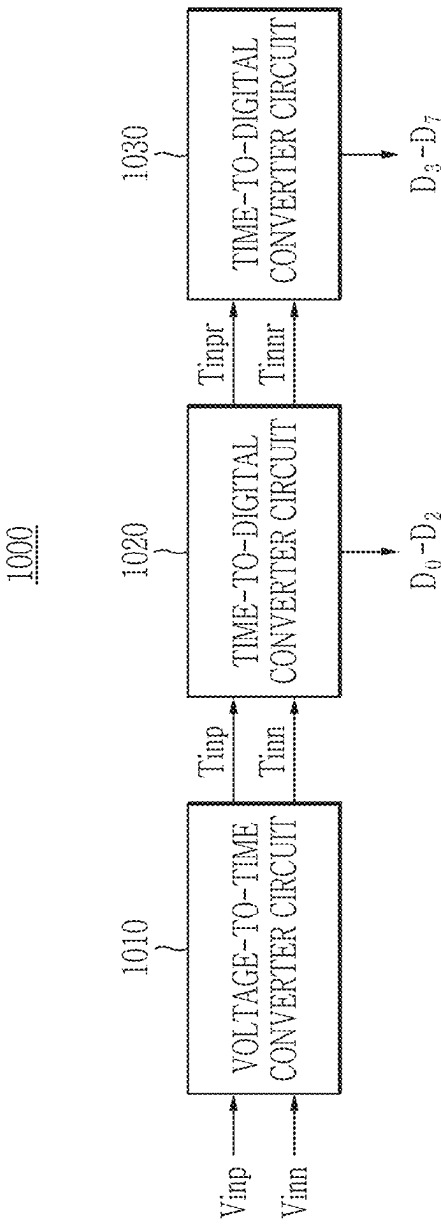


FIG. 11
1100

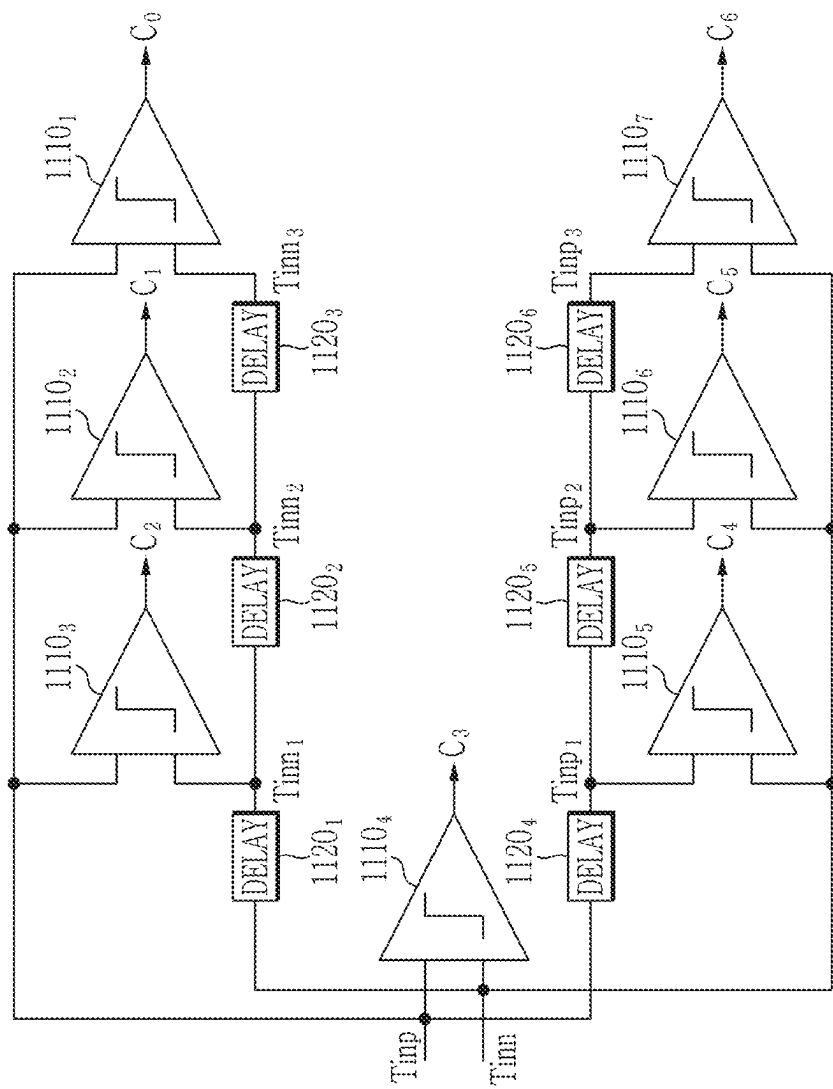


FIG. 12

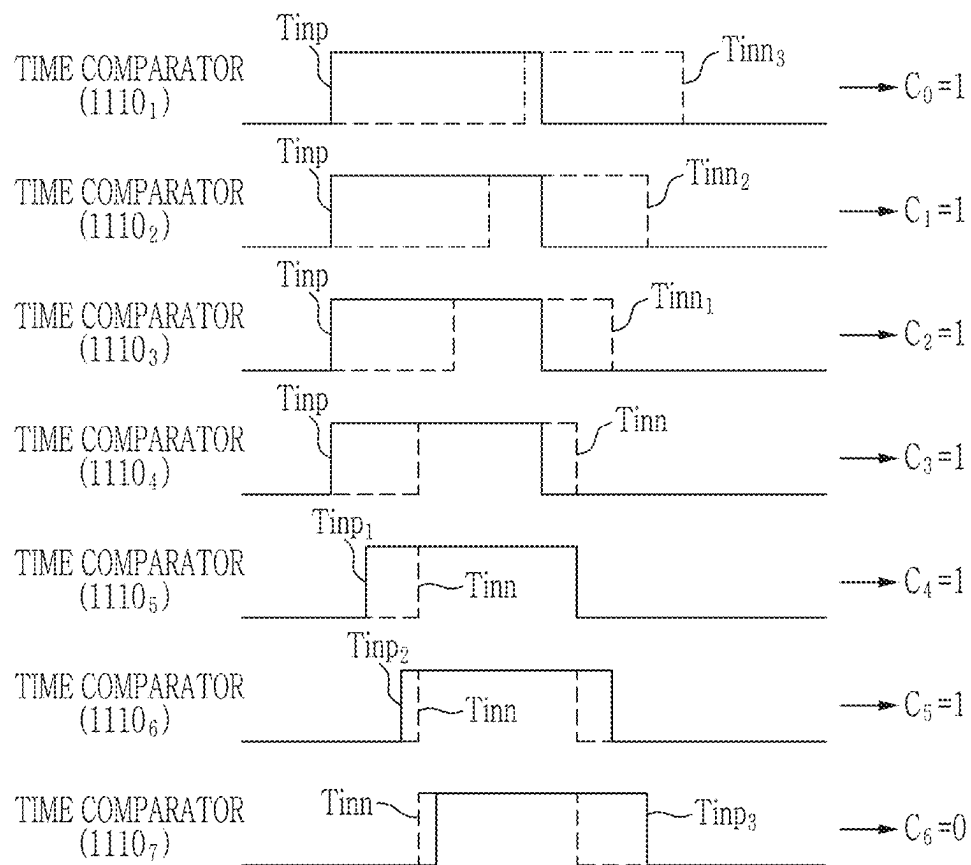


FIG. 13

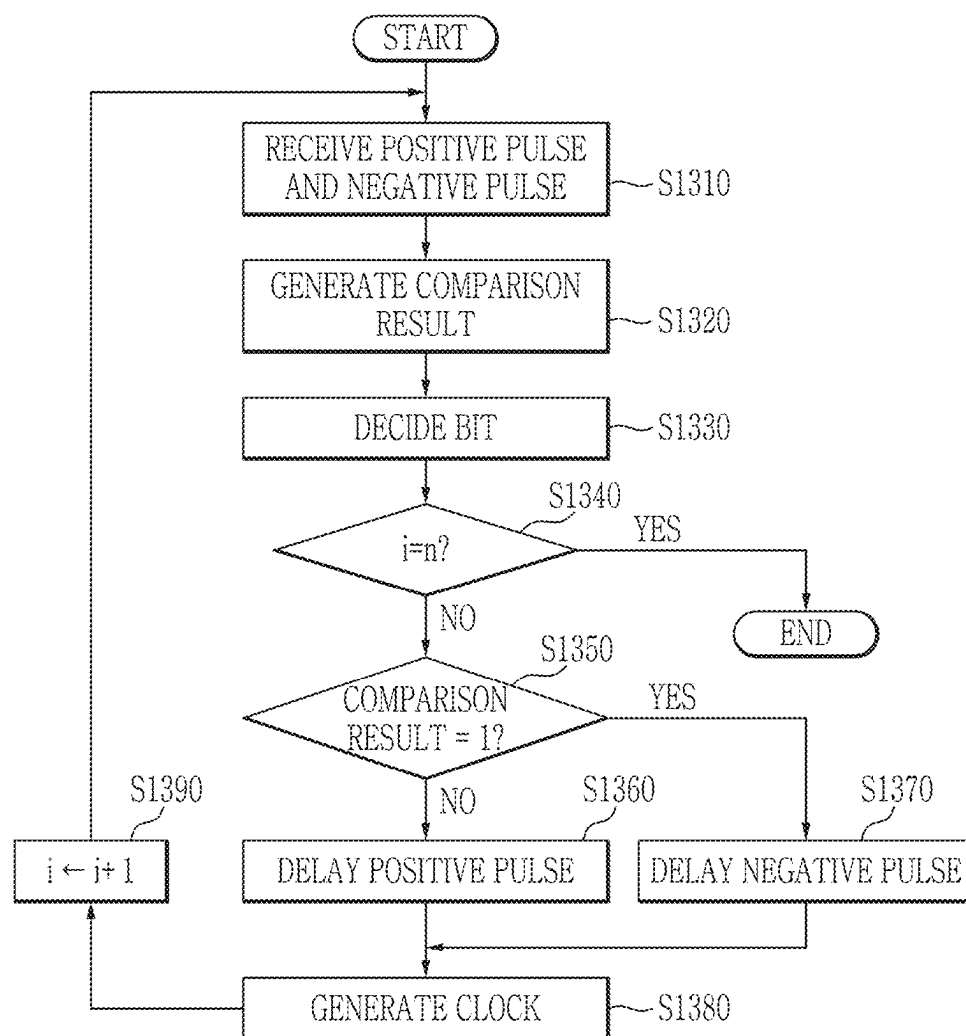


FIG. 14

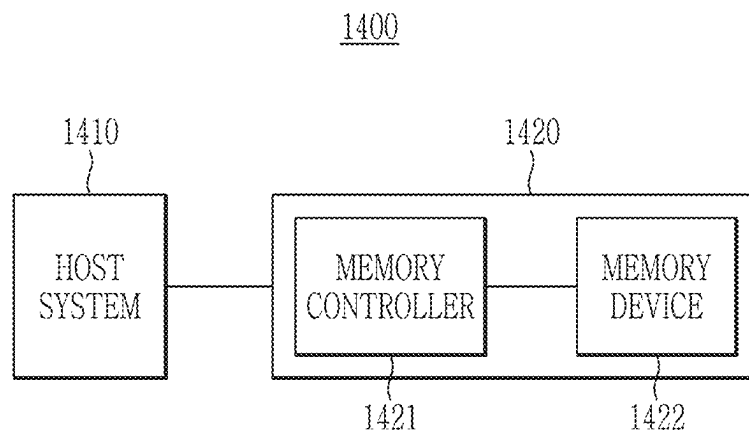
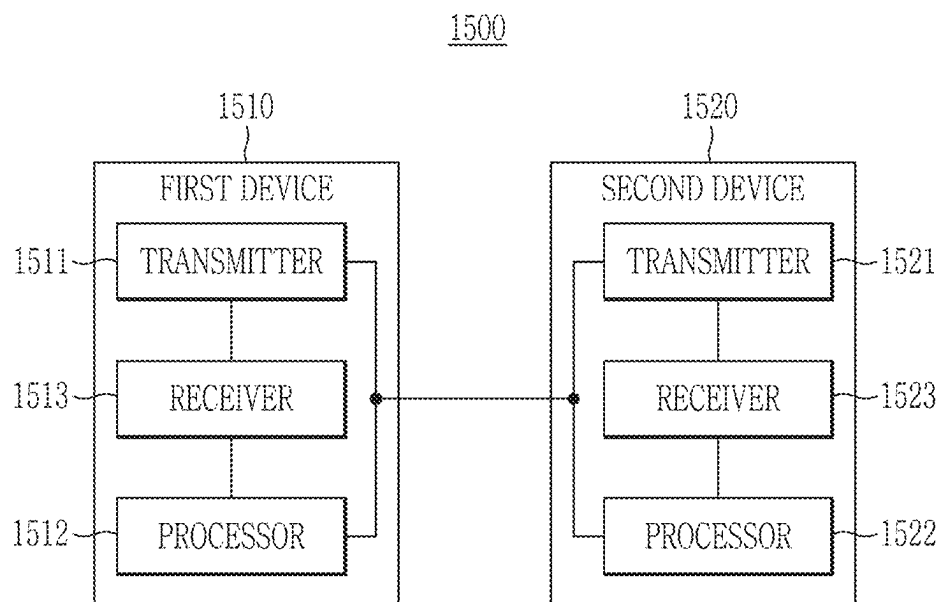


FIG. 15



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TIME DOMAIN ANALOG-TO-DIGITAL CONVERTER AND ANALOG-TO-DIGITAL CONVERTING METHOD

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority to and the benefit of Korean Patent Application No. 10-2022-0161571 filed in the Korean Intellectual Property Office on Nov. 28, 2022, the entire contents of which are incorporated herein by reference.

BACKGROUND

(a) Field

The disclosure relates to a time domain analog-to-digital converter and an analog-to-digital converting method.

(b) Description of the Related Art

An analog-to-digital converter (ADC) receives an analog input voltage and converts it into a digital signal that can be sent to other devices. ADCs may be used in various signal processing devices.

A voltage domain ADC outputs the difference in input voltages as a digital value. This process may take a while due to a settling time of a capacitor and a decision time of a comparator.

SUMMARY

Some example embodiments may provide a time domain analog-to-digital converter and an analog-to-digital converting method for reducing a waiting time.

According to some example embodiments, an analog-to-digital converter may include a plurality of stages and a plurality of clock generating circuits. The plurality of stages may be configured in a sequence to sequentially decide a plurality of bits in a successive-approximation. Each of the plurality of stages configured to operate in response to a corresponding clock among a plurality of clocks, and decide a corresponding bit among the plurality of bits from a corresponding positive pulse among a plurality of positive pulses and a corresponding negative pulse among a plurality of negative pulses, the plurality of positive pulses respectively input to the plurality of stages and the plurality of negative pulses respectively input to the plurality of stages. The plurality of clock generating circuits respectively correspond to a plurality of first stages among the plurality of stages. Each of the plurality of clock generating circuit may generate the corresponding clock of a corresponding stage among the plurality of first stages based on an operation of a previous stage among the plurality of stages, the previous stage being before the corresponding stage in the sequence.

According to some example embodiments, an analog-to-digital converter may include a first time comparator, a first delay circuit, a clock generating circuit, a second time comparator, and a second delay circuit. The first time comparator may operate in response to a first clock and decide a first bit based on a first comparison result of comparing a first positive pulse and a first negative pulse. The first delay circuit may delay either one of the first positive pulse and the first negative pulse by a first reference time based on a value of the first comparison result. The clock generating circuit may generate a second clock in

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response to the first comparison result. The second time comparator may operate in response to the second clock and decide a second bit based on a second comparison result of comparing a second positive pulse and a second negative pulse output from the first delay circuit. The second delay circuit may delay either one of the second positive pulse and the second negative pulse by a second reference time based on a value of the second comparison result.

According to some example embodiments, an analog-to-digital converting method may be provided. The analog-to-digital converting method may include receiving a first positive pulse and a first negative pulse, comparing the first positive pulse and the first negative pulse in response to a first clock to generate a first comparison result, deciding a first bit based on a value of the first comparison result, outputting a second positive pulse and a second negative pulse by delaying either one of the first positive pulse and the first negative pulse by a first reference time based on a value of the first comparison result, generating a second clock in response to the first comparison result, comparing the second positive pulse and the second negative pulse in response to the second clock to generate a second comparison result, and deciding a second bit based on a value of the second comparison result.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating an example of an analog-to-digital converter according to some example embodiments.

FIG. 2 is a block diagram showing an example of a voltage-to-time converter circuit of an analog-to-digital converter according to some example embodiments.

FIG. 3 is a circuit diagram illustrating an example of a sample/hold and ramp generating circuit in a voltage-to-time converter circuit shown in FIG. 2.

FIG. 4 is a circuit diagram illustrating an example of a pulse generating circuit in a voltage-to-time converter circuit shown in FIG. 2.

FIG. 5 is a diagram illustrating an example of a signal generated by a voltage-to-time converter circuit shown in FIG. 2.

FIG. 6 is a block diagram illustrating an example of a voltage-to-time converter circuit of an analog-to-digital converter according to some example embodiments.

FIG. 7 is a diagram illustrating an example of a signal generated by a voltage-to-time converter circuit shown in FIG. 6.

FIG. 8 is a block diagram illustrating an example of a stage in a voltage-to-time converter circuit of an analog-to-digital converter according to some example embodiments.

FIG. 9 is a diagram illustrating an example of a clock generating circuit in a voltage-to-time converter circuit of an analog-to-digital converter according to some example embodiments.

FIG. 10 is a block diagram illustrating an example of an analog-to-digital converter according to some example embodiments.

FIG. 11 is a block diagram illustrating an example of a flash voltage-to-time converter circuit according to some example embodiments.

FIG. 12 is a diagram showing an example of a signal generated in a flash voltage-to-time converter circuit shown in FIG. 11.

FIG. 13 is a flowchart illustrating an example of an analog-to-digital converting method according to some example embodiments.

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FIG. 14 is a block diagram illustrating an example of a computing device according to some example embodiments.

FIG. 15 is a block diagram illustrating an example of a communication system according to some example embodiments.

DETAILED DESCRIPTION OF THE EXAMPLE EMBODIMENTS

In the following detailed description, only certain example embodiments of the present invention have been shown and described, simply by way of illustration. As those skilled in the art would realize, the described example embodiments may be modified in various different ways, all without departing from the spirit or scope of the present invention.

Accordingly, the drawings and description are to be regarded as illustrative in nature and not restrictive. Like reference numerals designate like elements throughout the specification. The sequence of operations or steps is not limited to the order presented in the claims or figures unless specifically indicated otherwise. The order of operations or steps may be changed, several operations or steps may be merged, a certain operation or step may be divided, and a specific operation or step may not be performed.

As used herein, the singular forms “a” and “an” are intended to include the plural forms as well, unless the context clearly indicates otherwise. Although the terms first, second, and the like may be used herein to describe various elements, components, steps and/or operations, these terms are only used to distinguish one element, component, step or operation from another element, component, step, or operation.

FIG. 1 is a block diagram illustrating an example of an analog-to-digital converter according to some example embodiments.

Referring to FIG. 1, an analog-to-digital converter 100 according to some example embodiments may include a voltage-to-time converter (VTC) circuit 110 and a time-to-digital converter (TDC) circuit 120.

The VTC circuit 110 may receive an analog signal and convert the analog signal into a time domain to generate a pulse. The analog signal may include a differential input voltage V_{inp} and V_{inn} . The pulse may include a positive pulse (or non-inverting pulse) T_{inp} generated based on a positive input voltage (or non-inverting input voltage) V_{inp} of the differential input voltage and a negative pulse (or inverting pulse) T_{inn} generated based on a negative input voltage (or inverting input voltage) V_{inn} of the differential input voltage. A time difference between a start edge (e.g., a rising edge) of the positive pulse T_{inp} and a start edge (e.g., a rising edge) of the negative pulse T_{inn} may be decided based on a voltage difference (e.g., correspond to a voltage difference) between the positive input voltage V_{inp} and the negative input voltage V_{inn} .

The TDC circuit 120 may receive the pulses T_{inn} and T_{inp} as input values in a time domain, and sequentially decide a plurality of bits (e.g., n bits) D_0 to D_{n-1} from the pulses T_{inn} and T_{inp} in a successive-approximation. When deciding a bit D_i in a stage, the TDC circuit 120 may generate a clock to be used in a next stage. Here, i is an integer between 1 and n . That is, each stage of the TDC circuit 120 may decide a bit D_i in response to a clock generated according to an operation of a previous stage. In this case, the first stage (or a start stage) of the TDC circuit 120 may decide the first bit (e.g., the most significant bit among the plurality of bits) D_0 in response to an input clock.

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FIG. 2 is a block diagram showing an example of a VDC circuit of an analog-to-digital converter according to some example embodiments, FIG. 3 is a circuit diagram illustrating an example of a sample/hold (S/H) and ramp generating circuit in a VDC circuit shown in FIG. 2, FIG. 4 is a circuit diagram illustrating an example of a pulse generating circuit in a VDC circuit shown in FIG. 2, and FIG. 5 is a diagram illustrating an example of a signal generated by a VDC circuit shown in FIG. 2.

Referring to FIG. 2, a VTC circuit 110 according to some example embodiments may include an S/H and ramp generating circuit 111 and a pulse generating circuit 112.

The S/H and ramp generating circuit 111 may sample a positive input voltage V_{inn} and hold the sampled voltage at a predetermined (or alternatively, desired) point in time. Similarly, the S/H and ramp generating circuit 111 may sample a negative input voltage V_{inp} and hold the sampled voltage at a predetermined (or alternatively, desired) point in time. In some example embodiments, as shown in FIG. 3 and FIG. 5, the S/H and ramp generating circuit 111 may close a switch SW in response to an ON level of a sampling control signal SC to sample an input voltage V_{in} to a capacitor C_s . In addition, the S/H and ramp generating circuit 111 may hold a voltage V_{out} sampled in the capacitor C_s by opening the switch SW in response to an OFF level of the sampling control signal SC. In FIG. 3, the input voltage V_{in} may be the positive input voltage V_{inp} or the negative input voltage V_{inn} shown in FIG. 2, and the sampled voltage V_{out} may be a positive voltage V_{outp} or a negative voltage V_{outn} shown in FIG. 5.

The S/H and ramp generating circuit 111 may increase the voltage V_{outp} obtained from sampling the positive input voltage V_{inp} in a ramp form, and increase the voltage V_{outn} obtained from sampling the negative input voltage V_{inn} in a ramp form as well. In some example embodiments, as shown in FIG. 4 and FIG. 5, the S/H and ramp generating circuit 111 may inject a current I_r into the capacitor C_s to increase the voltage V_{out} sampled in the capacitor C_s in the ramp form. In FIG. 4, the voltage V_{out} may be the positive voltage V_{outp} or the negative voltage V_{outn} shown in FIG. 5.

The pulse generating circuit 112 may generate a pulse T_{inp} having a predetermined (or alternatively, desired) level (or a first level) from a point in time at which the voltage V_{outp} , which increases in the ramp form, becomes a predetermined (or alternatively, desired) voltage V_t , and the voltage V_{outp} increases in a ramp form, and generate a pulse T_{inn} having the predetermined (or alternatively, desired) level from a point in time at which the voltage V_{outn} becomes the predetermined (or alternatively, desired) voltage V_t . The predetermined (or alternatively, desired) level may be, for example, a high level. In this case, the pulses T_{inp} and T_{inn} may be switched from a low level to the high level at the point in time when the voltages V_{outp} and V_{outn} , which increase in the ramp form, become the predetermined (or alternatively, desired) voltage V_t . In FIG. 5, since the positive input voltage V_{inp} is higher than the negative input voltage V_{inn} , a start edge (e.g., a rising edge) of the pulse V_{inp} generated based on the positive input voltage V_{inp} may be earlier than a start edge (e.g., a rising edge) of the pulse V_{inn} generated based on the negative input voltage V_{inn} . Next, the pulse generating circuit 112 may reset the voltages V_{inp} and V_{inn} increasing in the ramp form at appropriate timings. When the voltages V_{inp} and V_{inn} fall below the predetermined (or alternatively, desired) voltage V_t , the pulses T_{inp} and T_{inn} may be switched to the low level (or a second level). Accordingly, the pulse generating circuit

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112 may generate the pulses T_{inp} and T_{inn} in the time domain. In this case, the time difference between the start edge of the pulse T_{inp} and the start edge of the pulse T_{inn} may be determined based on the voltage difference between the input voltage V_{in} and the input voltage V_{in} .

FIG. 6 is a block diagram illustrating an example of a TDC circuit of an analog-to-digital converter according to some example embodiments, and FIG. 7 is a diagram illustrating an example of a signal generated by a TDC circuit shown in FIG. 6.

Referring to FIG. 6, a TDC circuit 600 according to some example embodiments may include a plurality of stages 610₀, 610₁, 610₂, and 610₃, and one or more clock generating circuits 620₁, 620₂, and 620₃. Although FIG. 6 shows four stages 610₀ to 610₃ and three clock generating circuits 620₁ to 620₃, the number of stages 610₀ to 610₃ and the number of clock generating circuits 620₁ to 620₃ are not limited thereto. The stages 610₀ to 610₃ are in a sequence with one of the clock generating circuits 620₁ to 620₃ between each of the stages. The clock generating circuits 620₁ to 620₃ may also be in a sequence. A next stage may refer to a stage which receives input from a previous stage in the sequence. Restated a previous stage may provide an input to a next stage. For example, when the TDC circuit 600 decide n bits, the TDC circuit 600 may include n stages and (n-1) clock generating circuits.

Each stage 610_i may receive a positive pulse T_{inp} and a negative pulse T_{inn} . Here, i is an integer between 0 and 3. Each stage 610_i may compare the positive pulse T_{inp} and the negative pulse T_{inn} in response to an input clock CLK_i of a corresponding stage 610_i, and decide a bit D_i of the corresponding stage 610_i based on a comparison result. In some example embodiments, each stage 610_i may compare a start edge of the positive pulse T_{inp} with a start edge of the negative pulse T_{inn} , decide the bit D_i as '1' if the start edge of the positive pulse T_{inp} is earlier than the start edge of the negative pulse T_{inn} , and decide the bit D_i as '0' if the start edge of the negative pulse T_{inn} is earlier than the start edge of the positive pulse T_{inp} . When the TDC circuit 600 includes the four stages 610₀ to 610₃, the TDC circuit 600 may decide four bits D_0 to D_3 . In this case, among the four bits, the first stage 610₀ (or start stage) may decide the most significant bit D_0 , the second stage 610₁ may decide the second most significant bit D_1 , the third stage 610₂ may decide the third most significant bit D_2 , and the fourth stage 610₃ may decide the least significant bit D_3 . The start stage does not have a previous stage in the sequence of stages.

Each stage 610_i may output input pulses $T_{inp_{i+1}}$ and $T_{inn_{i+1}}$ of a next stage 610_{i+1} by delaying either the positive pulse T_{inp} or the negative pulse T_{inn} by a reference time of the corresponding stage 610_i based on the comparison result (e.g., the decided bit) and without delaying the other pulse by the reference time of the corresponding stage 610_i. In some example embodiments, the stage 610_i may delay two pulses T_{inp} and T_{inn} by a basic delay value, and then output the input pulses $T_{inp_{i+1}}$ and $T_{inn_{i+1}}$ of the next stage 610_{i+1} by delaying one pulse by the reference time of the corresponding stage 610_i, and without delaying the other pulse. For example, when the comparison result indicates that the start edge of the positive pulse T_{inp} is earlier than the start edge of the negative pulse T_{inn} (e.g., when the decided bit D_i is '1'), the stage 610_i may output the pulse $T_{inp_{i+1}}$ by delaying the positive pulse T_{inp} by the reference time, and output the pulse $T_{inn_{i+1}}$ without delaying the negative pulse T_{inn} . When the comparison result indicates that the start edge of the negative pulse T_{inn} is earlier than the start edge of the positive pulse T_{inp} (e.g., when the decided bit D_i is

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'0'), the stage 610_i may output the pulse $T_{inp_{i+1}}$ without delaying the positive pulse T_{inp} , and output the pulse $T_{inn_{i+1}}$ by delaying the negative pulse T_{inn} by the reference time. In this case, the first stage 610₀ may receive pulses input to the TDC circuit 600 (e.g., output pulses T_{inp} and T_{inn} of the VTC circuit shown in FIG. 2) as the input pulses T_{inp_0} and T_{inn_0} . Further, since the last stage 610₃ does not have a next stage, the last stage 610₃ may not delay the input pulses T_{inp_3} and T_{inn_3} .

The TDC circuit 600 may use a binary search. Accordingly, each stage 610_{i+1} may use half of the reference time of the previous stage 610_i as its own reference time. In this case, the first stage 610₀ may use half of a reference time T_{ref} of the TDC circuit 600 as its own reference time $T_{ref}/2$. Accordingly, the second stage 610₁ may use $T_{ref}/4$ as its own reference time, and the third stage 610₂ may use $T_{ref}/8$ as its own reference time.

The first stage 610₀ may receive an input clock CLK_0 of the TDC circuit 600 as its own clock and decide the bit D_0 of the corresponding stage 610₀ in response to the input clock CLK_0 . Each (or alternatively, at least one) of stages 610_i other than the first stage 610₀ may decide the bit D_i of the corresponding stage 610_i in response to a clock CLK_i generated by the corresponding clock generating circuit 620_i. Here, i is an integer between 1 and 3. The clock generating circuit 620_i may generate the clock CLK_i of the corresponding stage 620_i in response to an operation of the previous stage 620_{i-1}. In some example embodiments, the clock generating circuit 620_i may generate a start edge (e.g., a rising edge) of the clock CLK_i of the corresponding stage 620_i in response to the operation of the previous stage 620_{i-1}. In some example embodiments, the clock generating circuit 620_i may reset the clock CLK_i of the corresponding stage 620_i in response to an operation of the corresponding stage 620_i. In some other example embodiments, the clock generating circuit 620_i may reset the clock CLK_i of the corresponding stage 620_i when the clock CLK_{i+1} is generated in the next clock generating circuit 620_{i+1}. In some example embodiments, the clock generating circuit 620_i may reset the clock CLK_i by generating an end edge (e.g., a falling edge) of the clock CLK_i of the corresponding stage 620_i.

In some example embodiments, the operation of the stage 620_i may be a comparison operation in the stage 620_i. In this case, the clock generating circuit 620_i may generate the clock CLK_i of the corresponding stage 620_i in response to the comparison result (e.g., the decision result) of the previous stage 620_{i-1}. The clock generating circuit 620_i may reset the clock CLK_i of the corresponding stage 620_i in response to the comparison result (e.g., the decision result) of the corresponding stage 620_i.

In some example embodiments, when the clock CLK_i of the stage 620_i is reset, the comparison result of the corresponding stage 620_i may be reset for the next operation.

As shown in FIG. 7, for example, a positive pulse T_{inp_0} and a negative pulse T_{inn_0} later than the positive pulse T_{inp_0} may be input to the first stage 610₀. When the input clock CLK_0 has an active level (e.g., a high level as a logic level) by a start edge (e.g., a rising edge) of the input clock CLK_0 , the first stage 610₀ may compare the positive pulse T_{inp_0} and the negative pulse T_{inn_0} . In an example shown in FIG. 7, because the positive pulse T_{inp_0} is earlier than the negative pulse T_{inn_0} , the first stage 610₀ may decide '1' based on a comparison result. Further, because the positive pulse T_{inp_0} is earlier than the negative pulse T_{inn_0} , the first stage 610₀ may output an input pulse T_{inp_1} of the second stage 610₁ by delaying the positive pulse T_{inp_0} by half $T_{ref}/2$ of the

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reference time T_{ref} of the TDC circuit **600**, and output an input pulse T_{inn_1} of the second stage **610₁** without delaying the negative pulse T_{inn_0} by half $T_{ref}/2$ of the reference time T_{ref} . The first clock generating circuit **620₁** may activate a clock CLK_1 when the comparison is completed in the stage **610₀** (e.g., when the comparison result is generated in the stage **610₀**). The first clock generating circuit **620₁** may activate the clock CLK_1 by generating a start edge (e.g., a rising edge) of the clock CLK_1 .

When the clock CLK_1 output from the clock generating circuit **620₁** has the active level, the second stage **610₁** may compare the positive pulse T_{inp_1} and the negative pulse T_{inn_1} input from the first stage **610₀**. In the example shown in FIG. 7, because the positive pulse T_{inp_1} is earlier than the negative pulse T_{inn_1} , the second stage **610₁** may decide '1' based on a comparison result. Further, because the positive pulse T_{inp_1} is earlier than the negative pulse T_{inn_1} , the second stage **610₁** may output an input pulse T_{inp_2} of the third stage **610₂** by delaying the positive pulse T_{inp_1} by half $T_{ref}/4$ of the reference time $T_{ref}/2$ of the previous stage **610₀**, and output an input pulse T_{inn_2} of the third stage **610₂** without delaying the negative pulse T_{inn_1} by half $T_{ref}/4$ of the reference time $T_{ref}/2$. The first clock generating circuit **620₁** may deactivate the clock CLK_1 when the comparison is completed in the stage **610₁**. The first clock generating circuit **620₁** may deactivate the clock CLK_1 by generating an end edge (e.g., a falling edge) of the clock CLK_1 . Further, the second clock generating circuit **620₂** may activate a clock CLK_2 when the comparison is completed in the stage **610₁**.

When the clock CLK_2 output from the clock generating circuit **620₂** has the active level, the third stage **610₂** may compare the positive pulse T_{inp_2} and the negative pulses T_{inn_2} input from the second stage **610₁**. In the example shown in FIG. 7, because the positive pulse T_{inp_2} is earlier than the negative pulse T_{inn_2} , the third stage **610₂** may decide '1' based on a comparison result. Further, because the positive pulse T_{inp_2} is earlier than the negative pulse T_{inn_2} , the third stage **610₂** may output an input pulse T_{inp_3} of the fourth stage **610₃** by delaying the positive pulse T_{inp_2} by half $T_{ref}/8$ of the reference time $T_{ref}/4$ of the previous stage **610₁**, and output an input pulse T_{inn_3} of the fourth stage **610₃** without delaying the negative pulse T_{inn_2} by half $T_{ref}/8$ of the reference time $T_{ref}/4$. The second clock generating circuit **620₂** may deactivate the clock CLK_2 when the comparison is completed in the stage **610₂**. Further, the third clock generating circuit **620₃** may activate a clock CLK_3 when the comparison is completed in the stage **610₂**.

When the clock CLK_3 output from the clock generating circuit **620₃** has the active level, the fourth stage **610₃** may compare the positive pulse T_{inp_3} and negative pulse T_{inn_3} input from the third stage **610₂**. In the example shown in FIG. 7, because the negative pulse T_{inn_3} is earlier than the positive pulse T_{inp_3} , the fourth stage **610₃** may decide '0' based on a comparison result. The third clock generating circuit **620₃** may deactivate the clock CLK_3 when the comparison is completed in the stage **610₃**.

Through the above-described processes, the TDC circuit **600** may convert the input voltage into a digital signal D_0 to D_3 having "1110".

If each stage **610_i** does not use its own clock CLK_i and the plurality of stages **610₀** to **610₃** use the same clock, the clock should maintain the active level until the input pulse is propagated through the plurality of stages **610₀** to **610₃**. Therefore, because each stage **610_i** may operate again in the next clock cycle after the decision at the plurality of stages **610₀** to **610₃** is completed, a waiting time of the stage **610_i**

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may increase. However, according to the above-described example embodiments, each stage **610_i** may operate in response to its own clock CLK_i without waiting for the completion of the decision at the other stages, so that the waiting time may be reduced. That is, a pipelined successive-approximation TDC circuit may be provided.

Further, a method of generating a clock of a next stage by delaying the input clock CLK_0 may be used. This method may increase power consumption in a delay line for delaying the clock, and reset the comparator of the stage before the comparison is completed. However, since the pipelined successive-approximation TDC circuit described above does not use the delay line, power consumption can be reduced. Further, since a decision of a stage is completed and then a next stage operates in response to the clock, the comparator may not be reset before the operation is completed.

FIG. 8 is a block diagram illustrating an example of a stage in a TDC circuit of an analog-to-digital converter according to some example embodiments, and FIG. 9 is a diagram illustrating an example of a clock generating circuit in a TDC circuit of an analog-to-digital converter according to some example embodiments.

Referring to FIG. 8, a stage **800** may include a time comparator **810**, and delay circuits **820** and **830**.

The time comparator **810** may compare an input positive pulse T_{inp_i} and an input negative pulse T_{inn_i} . The time comparator **810** may compare a time of a start edge of the positive pulse T_{inp_i} and a time of a start edge of the negative pulse T_{inn_i} , and output a comparison result CMP_i . In some example embodiments, an output of the time comparator **810** may include the output CMP_i and a complementary output CMP_{b_i} having a complementary value of the output. In some example embodiments, the time comparator **810** may output '1' as the output CMP_i when the start edge of the positive pulse T_{inp_i} is earlier than the start edge of the negative pulse T_{inn_i} , and output '0' as the output CMP_i when the start edge of the positive pulse T_{inp_i} is later slower than the start edge of the negative pulse T_{inn_i} . The time comparator **810** may output '0' as the complementary output CMP_{b_i} when outputting '1' as the output CMP_i , and output '1' as the complementary output CMP_{b_i} when outputting '0' as the output CMP_i . The output CMP_i of the time comparator **810** may be a decision value of the stage **800**.

The delay circuit **820** may receive the positive pulse T_{inp_i} and operate in response to the output CMP_i of the time comparator **810**. When the output CMP_i of the time comparator **810** has a first value (e.g., '1'), the delay circuit **820** may output an input pulse $T_{inp_{i+1}}$ of a next stage by delaying the positive pulse T_{inp_i} by a reference time $T_{ref}/2^{i+1}$ of the stage **800**. When the output CMP_i of the time comparator **810** has a second value (e.g., '0'), the delay circuit **820** may output the input pulse $T_{inp_{i+1}}$ of the next stage without delaying the positive pulse T_{inp_i} by the reference time $T_{ref}/2^{i+1}$ of the stage **800**. In some example embodiments, the delay circuit **820** may include a delay circuit that operates in response to the output CMP_i of the time comparator **810** and delays an input by the reference time $T_{ref}/2^{i+1}$, and a delay circuit **822** that operates in response to the complementary output CMP_{b_i} of the time comparator **810** and does not delay an input by the reference time $T_{ref}/2^{i+1}$.

The delay circuit **830** may receive the negative pulse T_{inn_i} and operate in response to the output CMP_i of the time comparator **810**. When the output CMP_i of the time comparator **810** has the second value, the delay circuit **830** may output an input pulse $T_{inn_{i+1}}$ of the next stage by delaying the negative pulse T_{inn_i} by the reference time $T_{ref}/2^{i+1}$ of the

stage **800**. When the output CMP_i of the time comparator **810** has the first value, the delay circuit **820** may output the input pulse $Tinn_{i+1}$ of the next stage without delaying the negative pulse $Tinn_i$ by the reference time $Tref/2^{i+1}$ of the stage **800**. In some example embodiments, the delay circuit **830** may include a delay circuit that operates in response to the complementary output CMP_i of the time comparator **810** and delays an input by the reference time $Tref/2^{i+1}$, and a delay circuit **832** that operates in response to the output CMP_i of the time comparator **810** and does not delay an input by the reference time $Tref/2^{i+1}$.

In some example embodiments, the delay circuits **820** and **830** may delay the pulses $Tinp_i$ and $Tinn_i$ by a basic delay value, respectively.

Referring to FIG. 9, a clock generating circuit **900** may include a logic circuit **910** and a clock control circuit **920**, and may receive a comparison result of a previous stage.

The logic circuit **910** may output a signal having a predetermined (or alternatively, desired) level when a comparison between a positive pulse and a negative pulse is completed in the previous stage. In some example embodiments, when the comparison in the previous stage is completed, either one of an output CMP_{i-1} and a complementary output $CMPb_{i-1}$ may have '1' and the other may have '0' in a time comparator of the previous stage. Accordingly, the logic circuit **910** may be an exclusive OR (XOR) gate **910**. The XOR gate **910** may receive the output CMP_{i-1} and the complementary output $CMPb_{i-1}$ in the time comparator of the previous stage, and output a signal having '1' when the comparison is completed.

The clock control circuit **920** may generate a clock CLK_i of a corresponding stage when the output of the logic circuit **910** has the predetermined (or alternatively, desired) level (e.g., action level, or action value) (e.g., the action value may be a high level ('1') as a logic level). In some example embodiments, the clock control circuit **920** may generate the clock CLK_i by generating a start edge of the clock CLK_i of the corresponding stage.

In some example embodiments, the clock control circuit **920** may further include a logic circuit **930** that outputs a signal having a predetermined (or alternatively, desired) level when a comparison between the positive pulse and the negative pulse is completed in the corresponding stage. The logic circuit **930** may be an XOR gate that receives an output CMP_i and a complementary output $CMPb_i$ in a time comparator of the corresponding stage. Accordingly, the clock control circuit **920** may transfer a clock reset signal CLK_RST to the corresponding stage to reset the clock CLK_i when an output of the logic circuit **930** has the predetermined (or alternatively, desired) level (e.g., the high level ('1') as a logic level).

In some other example embodiments, when the output of the logic circuit **910** has the predetermined (or alternatively, desired) level, the clock control circuit **920** may transfer the clock reset signal CLK_RST to the clock control circuit **920** corresponding to the previous stage. The clock control circuit **920** corresponding to the previous stage may reset the clock CLK_{i-1} in response to the clock reset signal CLK_RST . In this case, the clock control circuit **920** may reset the clock CLK_i in response to the clock reset signal CLK_RST transferred from the clock control circuit **920** corresponding to a next stage.

In some example embodiments, when the clock CLK_i of a stage is reset, a time comparator (e.g., **810** in FIG. 8) of the corresponding stage may be reset for a next operation. When the time comparator **810** is reset, the time comparator **810**

may output the same value (e.g., '0') as the output CMP_i and the complementary output $CMPb_i$.

FIG. 10 is a block diagram illustrating an example of an analog-to-digital converter according to some example embodiments.

Referring to FIG. 10, an analog-to-digital converter **1000** may include a VTC circuit **1010**, a first TDC circuit **1020**, and a second TDC circuit **1030**. The analog-to-digital converter **1000** may convert analog input voltages $Vinp$ and $Vinn$ into a digital signal having a plurality of bits (e.g., eight bits). In this case, the analog-to-digital converter **1000** may perform a fine decision after performing a coarse decision.

As described with reference to FIG. 1, the VTC circuit **1010** may convert the input voltages $Vinp$ and $Vinn$ into time domain pulses $Tinp$ and $Tinn$.

The first TDC circuit **1020** may perform the coarse decision. The first TDC circuit **1020** may decide a predetermined (or alternatively, desired) number (e.g., three) of the most significant bits D_0 to D_2 among the eight bits from the input pulses $Tinp$ and $Tinn$, and output a positive pulse $Tinpr$ and a negative pulse $Tinnr$ as a residual signal corresponding to remaining bits (e.g., the lower five bits) D_3 to D_7 .

The second TDC circuit **1030** may perform the fine decision. The second TDC circuit **1030** may receive the residual signal $Tinpr$ and $Tinnr$ output from the first TDC circuit **1020** as input pulses, and decide the five bits D_3 to D_7 from the input pulses $Tinpr$ and $Tinnr$.

In some example embodiments, both the first TDC circuit **1020** and the second TDC circuit **1030** may be implemented as a pipelined successive-approximation TDC described above.

In some other example embodiments, the second TDC circuit **1030** may be implemented as the pipelined successive-approximation TDC, and the first TDC circuit **1020** may be implemented as a faster TDC than the pipelined successive-approximation TDC. For example, the first TDC circuit **1020** may be implemented as a flash TDC.

FIG. 11 is a block diagram illustrating an example of a flash TDC circuit according to some example embodiments, and FIG. 12 is a diagram showing an example of a signal generated in a flash TDC circuit shown in FIG. 11.

Referring to FIG. 11, a flash TDC circuit **1100** may include a plurality of time comparators **1110**₁, **1110**₂, **1110**₃, **1110**₄, **1110**₅, **1110**₆, and **1110**₇, and a plurality of delay circuits **1120**₁, **1120**₂, **1120**₃, **1120**₄, **1120**₅, and **1120**₆. Although FIG. 11 shows seven time comparators **1110**₁ to **1110**₇ and six delay circuits **1120**₁ to **1120**₆, the number of time comparators **1110**₁ to **1110**₇ and the number of delay circuits **1120**₁ to **1120**₆ are not limited thereto. For example, if the flash TDC circuit **1100** decides n bits, the flash TDC circuit **1100** may include $(2^n - 1)$ time comparators and $(2^n - 2)$ delay circuits.

Each (or alternatively, at least one) of the delay circuits **1120**₁ to **1120**₆ may delay an input pulse by a reference time. When the flash TDC circuit **1100** decides the n bits, the reference time may be $1/2^n$ of a reference time $Tref$ of the flash TDC circuit **1100**. In an example shown in FIG. 11 and FIG. 12, the reference time may be $Tref/4$. The delay circuit **1120**₁ may output a negative pulse $Tinn$ by delaying an input negative pulse $Tinn$ by the reference time $Tref/4$, the delay circuit **1120**₂ may output a negative pulse $Tinn_2$ by delaying the negative pulse $Tinn_1$ output from delay circuit **1120**₁ by the reference time $Tref/4$, and the delay circuit **1120**₃ may output a negative pulse $Tinn_3$ by delaying the negative pulse $Tinn_2$ output from delay circuit **1120**₂ by the reference time $Tref/4$. Accordingly, the negative pulse $Tinn_2$ may be

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delayed by $2T_{ref}/4$ from the input negative pulse T_{inn} , and the negative pulse T_{inn_2} may be delayed by $3T_{ref}/4$ from the input negative pulse T_{inn} . The delay circuit **1120₄** may output a positive pulse T_{inp_1} by delaying an input positive pulse T_{inp} by the reference time $T_{ref}/4$, the delay circuit **1120₅** may output a positive pulse T_{inp_2} by delaying the positive pulse T_{inp_1} output from delay circuit **1120₄** by the reference time $T_{ref}/4$, and the delay circuit **1120₆** may output a positive pulse T_{inp_3} by delaying the positive pulse T_{inp_2} output from delay circuit **1120₅** by the reference time $T_{ref}/4$. Accordingly, the positive pulse T_{inp_2} may be delayed by $2T_{ref}/4$ from the input positive pulse T_{inp} , and the positive pulse T_{inp_3} may be delayed by $3T_{ref}/4$ from the input positive pulse T_{inp} .

Each (or alternatively, at least one) of the time comparators **1110₁** to **1110₇** may compare a positive pulse and a negative pulse, and decide a corresponding one among bits C_0 to C_6 based on a comparison result. In some example embodiments, the time comparators **1110₁** to **1110₇** may compare a start edge of the positive pulse with a start edge of the negative pulse, decide '1' if the start edge of the positive pulse is earlier than the start edge of the negative pulse, and decide '0' if the start edge of the negative pulse is earlier than the start edge of the positive pulse.

The time comparators **1110₁** to **1110₄** may receive the input positive pulse T_{inp} as the positive pulse, and the time comparators **1110₄** to **1110₇** may receive the input negative pulse T_{inn} as the negative pulse. The time comparator **1110₁** may receive the negative pulse T_{inn_3} output from the delay circuit **1120₃** as the negative pulse, the time comparator **1110₂** may receive the negative pulse T_{inn_2} output from the delay circuit **1120₂** as the negative pulse, and the time comparator **1110₃** may receive the negative pulse T_{inn_1} output from the delay circuit **1120₁** as the negative pulse. The time comparator **1110₅** may receive the positive pulse T_{inp_1} output from the delay circuit **1120₄** as the positive pulse, the time comparator **1110₆** may receive the positive pulse T_{inp_2} output from the delay circuit **1120₅** as the positive pulse, and the time comparator **1110₇** may receive the positive pulse T_{inp_3} output from the delay circuit **1120₆** as the positive pulse.

As shown in FIG. 12, for example, the input positive pulse T_{inp} and the input negative pulse T_{inn} may be input to the TDC circuit **1200**, and the input negative pulse T_{inn} may be later than the input positive pulse T_{inp} by a time longer than $2T_{ref}/4$ and shorter than $3T_{ref}/4$. Then, because the input positive pulse T_{inp} is earlier than the negative pulse T_{inn_3} delayed by $3T_{ref}/4$ from the input negative pulse T_{inn} , the time comparator **1110₁** may decide the bit C_0 as '1'. Because the input positive pulse T_{inp} is earlier than the negative pulse T_{inn_2} delayed by $2T_{ref}/4$ from the input negative pulse T_{inn} , the time comparator **1110₂** may also decide the bit C_1 as '1'. Because the input positive pulse T_{inp} is earlier than the negative pulse T_{inn_1} delayed by $T_{ref}/4$ from the input negative pulse T_{inn} , the time comparator **1110₃** may also decide the bit C_2 as '1'. Because the input positive pulse T_{inp} is earlier than the input negative pulse T_{inn} , the time comparator **1110₄** may also decide the bit C_3 as '1'. Because the positive pulse T_{inp_1} delayed by $T_{ref}/4$ from the input positive pulse T_{inp} is earlier than the input negative pulse T_{inn} , the time comparator **1110₅** may also decide the bit C_4 as '1'. Because the positive pulse T_{inp_1} delayed by $2T_{ref}/4$ from the input positive pulse T_{inp} is earlier than the input negative pulse T_{inn} , the time comparator **1110₆** may also decide the bit C_5 as '1'. Because the positive pulse T_{inp_1} delayed by $3T_{ref}/4$ from the input positive pulse T_{inp} is later

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than the input negative pulse T_{inn} , the time comparator **1110₇** may decide the bit C_6 as '0'.

Therefore, the flash TDC circuit **1100** may output a decision code C_0 to C_6 of "1111110". The decision code C_0 to C_6 of "1111110" may be a thermometer code, and may correspond to "110" in a binary digital code. Since the flash TDC circuit **1100** may output all digital values in one clock cycle, it may operate faster than a pipelined successive-approximation TDC circuit.

As described above, in some example embodiments, when the flash TDC circuit is used as the first TDC circuit **1020** in FIG. 10, the analog-to-digital converter may operate faster. In some example embodiments, when the pipelined successive-approximation TDC circuit is used as the first TDC circuit **1020** in FIG. 10, the number of time comparators may be reduced. For example, for n-bit decision, n time comparators may be used in the pipelined successive-approximation TDC circuit, whereas $(2^n - 1)$ time comparators may be used in the flash TDC circuit.

FIG. 13 is a flowchart illustrating an example of an analog-to-digital converting method according to some example embodiments.

Referring to FIG. 13, an analog-to-digital converter may receive the i^{th} positive pulse and the i^{th} negative pulse at the i^{th} stage in **S1310**. In some example embodiments, the first positive pulse and the first negative pulse of the first stage may be pulses generated by converting an input voltage into a time domain. In some example embodiments, the first positive pulse and the first negative pulse may be pulses that is remained after some bits (or alternatively, at least one bit) are decided from the pulses generated by converting the input voltage into the time domain.

In the i^{th} stage, the analog-to-digital converter may generate the i^{th} comparison result by comparing the i^{th} positive pulse and the i^{th} negative pulse in response to the i^{th} clock in **S1320**. The analog-to-digital converter may decide the i^{th} bit based on the i^{th} comparison result in **S1330**. When the i^{th} stage is the last stage (e.g., the n^{th} stage) in **S1340**, the analog-to-digital converter may end the decision.

When the i^{th} stage is not the last stage in **S1340**, the analog-to-digital converter may output the $(i+1)^{th}$ positive pulse and the $(i+1)^{th}$ negative pulse by delaying either one of the i^{th} positive pulse and the i^{th} negative pulse by the i^{th} reference time based on a value of the i^{th} comparison result in **S1350**, **S1360**, and **S1370**. Further, the analog-to-digital converter may generate the $(i+1)^{th}$ clock in response to the i^{th} comparison result in **S1380**. In some example embodiments, the analog-to-digital converter may generate a first value (e.g., '1') as the i^{th} comparison result if the i^{th} positive pulse is earlier than the i^{th} negative pulse, and generate a second value (e.g., '0') different from the first value as the i^{th} comparison result if the i^{th} negative pulse is earlier than the i^{th} positive pulse. In some example embodiments, when the i^{th} comparison result has the first value in **S1350**, the analog-to-digital converter may delay the i^{th} positive pulse by the i^{th} reference time in **S1360**. When the i^{th} comparison result has the second value in **S1350**, the analog-to-digital converter may delay the i^{th} negative pulse by the i^{th} reference time in **S1370**.

Next, the analog-to-digital converter may perform a decision at the $(i+1)^{th}$ stage in **S1390**.

FIG. 14 is a block diagram illustrating an example of a computing device according to some example embodiments.

Referring to FIG. 14, a computing device **1400** may include a host system **1410** and a memory system **1420**. The host system **1410** and the memory system **1420** may com-

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municate through an interface. The memory system **1420** may include a memory controller **1421** and a memory device **1422**.

The memory controller **1421** may control a memory operation of the memory device **1422** by providing a signal to the memory device **1422** in response to a request from the host system **1410**. The signal may include a command and an address. The memory controller **1421** may read data from the memory device **1422** by providing a read signal to the memory device **1422**. Further, the memory controller **1421** may write data into the memory device **1422** by providing a write signal and the data to the memory device **1422**.

In some example embodiments, the memory device **1422** may include a volatile memory such as a dynamic random-access memory (DRAM). In some example embodiments, the memory device **1422** may include a non-volatile memory such as a flash memory, a phase-change memory, a resistive memory, a magnetoresistive memory, a ferroelectric memory, or a polymer memory. In some example embodiments, the memory device **1422** may be used as a system memory of host system **1410**. In this case, the memory controller **1421** may be provided as a separate chip from a processor of the host system **1410**, or may be provided as an internal component of the processor. In some example embodiments, the memory system **1420** may be used as a storage device for the host system **1410**.

An analog-to-digital converter described with reference to FIG. 1 to FIG. 13 may be included in the host system **1410**, the memory controller **1421**, and/or the memory device **1422** to convert an analog voltage into a digital signal.

FIG. 15 is a block diagram illustrating an example of a communication system according to some example embodiments.

Referring to FIG. 15, a communication system **1500** may include a first device **1510** and a second device **1520**.

The first device **1510** may include a transmitter **1511**, a receiver **1512**, and a processor **1513**, and the second device **1520** may include a transmitter **1521**, a receiver **1522**, and a processor **1523**. The transmitter **1511** of the first device **1510** may transmit data to the second device **1520**, and the receiver **1522** of the second device **1520** may receive the data. Similarly, the transmitter **1521** of the second device **1520** may transmit data to the first device **1510**, and the receiver **1512** of the first device **1510** may receive the data. The processor **1513** may control operations of the transmitter **1511** and the receiver **1512**, and the processor **1523** may control operations of the transmitter **1521** and the receiver **1522**.

An analog-to-digital converter described with reference to FIG. 1 to FIG. 13 may be included in the transmitter **1511**, the receiver **1512**, the transmitter **1521**, and/or the receiver **1522** to convert an analog voltage into a digital signal.

Although FIG. 14 and FIG. 15 shows the computing device and the communication system in which the analog-to-digital converter is used, a system or device to which the analog-to-digital converter is used is not limited thereto. The analog-to-digital converter may be used to convert an analog voltage to a digital signal in a variety of devices.

In some example embodiments, each (or alternatively, at least one) of the components, elements, modules, or units represented by a block as illustrated in FIG. 1 to FIG. 12 may be implemented as various numbers of hardware, software, and/or firmware structures that execute respective functions described above, according to some example embodiments. For example, at least one of these components, elements, modules, or units may include various hardware components including a digital circuit, a programmable or non-program-

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mable logic device or array, an application specific integrated circuit (ASIC), or other circuitry using a digital circuit structure, such as a memory, a processor, a logic circuit, a look-up table, etc., that may execute the respective functions through controls of one or more microprocessors or other control apparatuses. Further, at least one of these components, elements, modules, or units may include a module, a program, or a part of code, which contains one or more executable instructions for performing specified logic functions, and executed by one or more microprocessors or other control apparatuses. Furthermore, at least one of these components, elements, modules, or units may further include or may be implemented by a processor that performs the respective functions. Functional aspects of example embodiments may be implemented in algorithms that execute on one or more processors.

Any of the elements and/or functional blocks disclosed above may include or be implemented in processing circuitry such as hardware including logic circuits; a hardware/software combination such as a processor executing software; or a combination thereof. For example, the clock control circuit **920** and memory controller **1421** may be implemented as processing circuitry. The processing circuitry specifically may include, but is not limited to, a central processing unit (CPU), an arithmetic logic unit (ALU), a digital signal processor, a microcomputer, a field programmable gate array (FPGA), a System-on-Chip (SoC), a programmable logic unit, a microprocessor, application-specific integrated circuit (ASIC), etc. The processing circuitry may include electrical components such as at least one of transistors, resistors, capacitors, etc. The processing circuitry may include electrical components such as logic gates including at least one of AND gates, OR gates, NAND gates, NOT gates, etc.

Processor(s), controller(s), and/or processing circuitry may be configured to perform actions or steps by being specifically programmed to perform those action or steps (such as with an FPGA or ASIC) or may be configured to perform actions or steps by executing instructions received from a memory, or a combination thereof.

While this invention has been described in connection with what is presently considered to be practical example embodiments, it is to be understood that the invention is not limited to the disclosed example embodiments. On the contrary, it is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

What is claimed is:

1. An analog-to-digital converter comprising:

a plurality of stages configured in a sequence to sequentially decide a plurality of bits in successive approximation, each of the plurality of stages configured to operate in response to a corresponding clock among a plurality of clocks, and decide a corresponding bit among the plurality of bits from a corresponding positive pulse among a plurality of positive pulses and a corresponding negative pulse among a plurality of negative pulses, the plurality of positive pulses respectively input to the plurality of stages and the plurality of negative pulses respectively input to the plurality of stages; and

a plurality of clock generating circuits respectively corresponding to a plurality of first stages among the plurality of stages, each of the plurality of clock generating circuits configured to generate the corresponding clock of a corresponding stage among the plurality of first stages based on an operation of a previous stage

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among the plurality of stages, the previous stage being before the corresponding stage in the sequence.

2. The analog-to-digital converter of claim 1, wherein each of the plurality of stages is further configured to compare the corresponding positive pulse and the corresponding negative pulse to decide the corresponding bit, and

each of a plurality of second stages among the plurality of stages is configured to generate a positive pulse to be input to a next stage among the plurality of positive pulses and a negative pulse to be input to the next stage among the plurality of negative pulses, by delaying either one of the corresponding positive pulse and the corresponding negative pulse by a corresponding reference time among a plurality of reference times respectively corresponding to the plurality of second stages, the plurality of second stages not including a last stage in the sequence among the plurality of stages, the next stage being a stage after the corresponding stage in the sequence, the last stage not having a next stage in the sequence.

3. The analog-to-digital converter of claim 2, wherein the operation of the previous stage comprises a comparison operation of a positive pulse input to the previous stage among the plurality of positive pulses and a negative pulse input to the previous stage among the plurality of negative pulses.

4. The analog-to-digital converter of claim 3, wherein each of the plurality of clock generating circuits is further configured to generate the corresponding clock of the corresponding stage in response to a result of the comparison operation in the previous stage.

5. The analog-to-digital converter of claim 3, wherein each of the plurality of clock generating circuits is further configured to reset the corresponding clock of the corresponding stage in response to a result of the comparison operation in the corresponding stage.

6. The analog-to-digital converter of claim 3, wherein each of the plurality of clock generating circuits is further configured to reset the corresponding clock of the corresponding stage in response to generation of a clock in a next clock generating circuit among the plurality of clock generating circuits.

7. The analog-to-digital converter of claim 2, wherein each of the plurality of second stages is further configured to delay the corresponding positive pulse by the corresponding reference time when deciding the corresponding bit as a first value, or

delay the corresponding negative pulse by the corresponding reference time when deciding the corresponding bit as a second value different from the first value.

8. The analog-to-digital converter of claim 2, wherein, the plurality of second stages include a start stage in the sequence and at least one third stage, the start stage in the sequence not having a previous stage in the sequence, the corresponding reference time of each of the at least one third stage is half of a reference time corresponding to the previous stage among the plurality of reference times.

9. The analog-to-digital converter of claim 1, wherein the plurality of first stages are stages not including a start stage among the plurality of stages in the sequence, the start stage in the sequence not having a previous stage in the sequence.

10. The analog-to-digital converter of claim 9, wherein the corresponding clock of the start stage is an input clock of the analog-to-digital converter.

11. The analog-to-digital converter of claim 1, further comprising a voltage-to-time converter circuit configured to

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convert a positive input voltage and a negative input voltage into a time domain to generate an input positive pulse and an input negative pulse to be input to a start stage among the plurality of stages in the sequence as the corresponding positive pulse and the corresponding negative pulse of the start stage, respectively, the start stage in the sequence not having a previous stage in the sequence.

12. The analog-to-digital converter of claim 1, further comprising:

a voltage-to-time converter circuit configured to convert a positive input voltage and a negative input voltage into a time domain to generate an input positive pulse and an input negative pulse; and

a time-to-digital converter circuit configured to decide at least one bit based on the input positive pulse and the input negative pulse, and then output a residual positive pulse and a residual negative pulse to be input to a start stage among the plurality of stages in the sequence as the corresponding positive pulse and the corresponding negative pulse, respectively, the start stage in the sequence not having a previous stage in the sequence.

13. An analog-to-digital converter comprising:

a first time comparator configured to operate in response to a first clock, and decide a first bit based on a first comparison result of comparing a first positive pulse and a first negative pulse;

a first delay circuit configured to delay either one of the first positive pulse and the first negative pulse by a first reference time based on a value of the first comparison result;

a clock generating circuit configured to generate a second clock in response to the first comparison result;

a second time comparator configured to operate in response to the second clock, and decide a second bit based on a second comparison result of comparing a second positive pulse and a second negative pulse output from the first delay circuit; and

a second delay circuit configured to delay either one of the second positive pulse and the second negative pulse by a second reference time based on a value of the second comparison result.

14. The analog-to-digital converter of claim 13, wherein the clock generating circuit is further configured to reset the second clock in response to the second comparison result.

15. The analog-to-digital converter of claim 13, wherein the first time comparator is further configured to

output a first value as the first comparison result in response to the first positive pulse being earlier than the first negative pulse, or

output a second value different from the first value as the first comparison result in response to the first negative pulse being earlier than the first positive pulse,

wherein the second time comparator is further configured to

output the first value as the second comparison result in response to the second positive pulse being earlier than the second negative pulse, or

output the second value different as the second comparison result in response to the second negative pulse being earlier than the second positive pulse.

16. The analog-to-digital converter of claim 15, wherein the first delay circuit is further configured to

delay the first positive pulse by the first reference time in response to the first value of the first comparison result, and

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- delay the first negative pulse by the first reference time in response to the second value of the first comparison result, and
 wherein the second delay circuit is further configured to delay the second positive pulse by the second reference time in response to the first value of the second comparison result, and
 delay the second negative pulse by the second reference time in response to the second value of the second comparison result.
17. The analog-to-digital converter of claim 13, wherein the first time comparator is further configured to output a first complementary comparison result having a complementary value of the first comparison result, and
 wherein the clock generating circuit is further configured to generate the second clock in response to a result of a logical operation on the first comparison result and the first complementary comparison result having an action value.
18. The analog-to-digital converter of claim 17, wherein the logical operation is an exclusive OR operation, and wherein the action value is '1'.
19. The analog-to-digital converter of claim 17, wherein the second time comparator is further configured to output a second complementary comparison result having a complementary value of the second comparison result, and

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- wherein the clock generating circuit is further configured to reset the second clock when a result of a logical operation on the second comparison result and the second complementary comparison result has the action value.
20. An analog-to-digital converting method comprising:
 receiving a first positive pulse and a first negative pulse;
 comparing the first positive pulse and the first negative pulse in response to a first clock to generate a first comparison result;
 deciding a first bit based on a value of the first comparison result;
 outputting a second positive pulse and a second negative pulse by delaying either one of the first positive pulse and the first negative pulse by a first reference time based on the value of the first comparison result;
 generating a second clock in response to the first comparison result;
 comparing the second positive pulse and the second negative pulse in response to the second clock to generate a second comparison result; and
 deciding a second bit based on a value of the second comparison result.

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