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Semiconductor Device for driving a display and A Display driving device including the same

Abstract

A semiconductor device for driving a display according to the embodiment may include a first conductivity type base layer, a second conductivity type doping area on the first conductivity type base layer, a source area on the second conductivity type doping area, a drain area on the first conductivity type base layer, a gate insulating film disposed between the source area and the drain area, a gate electrode disposed on the gate insulating film and one or more device isolating areas disposed on the base layer. The active area including the second conductivity type doping area and the source area may include an active corner cut area in a corner area facing the drain area.

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims the benefits of priority to Korean Patent Application No. 10-2024-0024602, filed on Feb. 20, 2024, which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] An embodiment relates to a semiconductor device for driving a display and a display driving device including the same. For example, the embodiment may relate to a high voltage (HV) MOSFET semiconductor device for driving a display, but is not limited thereto.

BACKGROUND

[0003] A display driver integrated circuit DDIC for driving the display panel may be connected to the display panel.

[0004] The display driver integrated circuit (DDIC) uses a medium voltage (MV) semiconductor device or a high voltage (HV) semiconductor device for panel control.

[0005] FIG. **1** is a partial cross-sectional photograph of a high voltage (HV) MOSFET device according to the prior art.

[0006] In the active corner of a conventional high-voltage (HV) MOSFET structure, a gate oxide thinning (TT) occurs, which makes it difficult to manage a process for leakage and breakdown voltage distribution characteristics of semiconductor devices.

[0007] As a result, there is a problem of difficulty in securing reliability during TDDB (time dependent dielectric breakdown) testing.

[0008] In particular, due to a recent ultra-miniaturization of semiconductor processes, ultra-fine CMOS transistors of 28 nm or less from the existing 40 nm are being adopted, and along with this, a thickness of the gate oxide is also becoming thinner. Accordingly, the reliability of semiconductor devices becomes more vulnerable due to acceleration of gate oxide thinning due to electric field concentration at the active corner.

SUMMARY

[0009] One of the technical objects of the embodiment is to improve the breakdown voltage distribution characteristics by improving leakage in a classic semiconductor device.

[0010] A semiconductor device for driving a display according to the embodiment may include a first conductivity type base layer **205**, a second conductivity type doping area **207** disposed on the first conductivity type base layer **205**, a source area **210** disposed on the second conductivity type doping area **207**, a drain area **220** disposed on the first conductivity type base layer **205**, a gate insulating film **232** disposed between the source area **210** and the drain area **220**, a gate electrode **230** disposed on the gate insulating film **232** and one or more device isolating areas **250** disposed on the base layer **205**.

[0011] The active area **200**A including the second conductivity type doping area **207** and the source area **210** may include an active corner cut area **200**AC in the corner area facing the drain area **220**.

[0012] The active area **200**A may include a first active area **200**A**1** at the center of the gate electrode **230** and a second active area **200**A**2** outside where the active corner cut area **200**AC is located, and a width Wa**1** of the first active area **200**A**1** at the center may be larger than the width Wa**2** of the second active area **200**A**2** at the outside.

[0013] The active corner cut area **200**AC may include a right-angled triangle shape.

[0014] The active corner cut area **200**AC may include a first active corner cut area disposed at an upper edge of the second active area **200**A**2** facing the drain area **220**, and a second active corner cut area disposed at a lower edge of the second active area **200**A**2** facing the drain area **220**.

[0015] In the embodiment, a distance from the first active area **200**A**1** at the center to the drain area **220** may be shorter than a distance from the second active area **200**A**2** at the outside to the drain area **220**.
[0016] In the embodiment, a distance from the first active area **200**A**1** in the center to the outside of the gate electrode in the direction of the drain area **220** may be shorter than a distance from the outer second active area **200**A**2** to the gate electrode in the drain area **220**
[0017] The active corner cut area **200**AC may include a first side (a) of the active corner cut area **200**AC and a second side (b) perpendicular thereto.
[0018] A length of the first side (a) and a length of the second side (b) may be the same.
[0019] The active area **200**A may not include an active corner cut area in the corner area facing the source area **210**.
[0020] Also, a semiconductor device for driving a display according to the embodiment may include a first conductivity type base layer, a second conductivity type doping area disposed on the first conductivity type base layer, a source area disposed on the second conductivity type doping area, a drain area disposed on the first conductivity type base layer, a gate insulating film disposed between the source area and the drain area, a gate electrode disposed on the gate insulating film. And the second conductivity type doping area may include an active corner cut area in a corner area facing the drain area in a plan view.
[0021] Also, an active area may include the second conductivity type doping area and the source area and the active area may include a first active area at a first region vertically overlapping the gate electrode and a second active area at a second region laterally overlapping the active corner cut area.
[0022] Also, a lateral width of the first active area may be larger than a lateral width of the second active area.
[0023] Also, the active corner cut area may include a first active corner cut area disposed at an upper edge of the second active area facing the drain area, and a second active corner cut area disposed at a lower edge of the second active area facing the drain area.
[0024] Also, a distance from the first active area to the drain area may be shorter than a distance from the second active area to the drain area.
[0025] Also, a distance from the first active area to the outside of the gate electrode in a direction of the drain area may be shorter than a distance from the second active area to the gate electrode in a direction of the drain area.
[0026] Also, the active corner cut area may include a right-angled triangle shape.
[0027] Also, the active corner cut area may include a first side and a second side perpendicular to the first side of the active corner cut area, and a length of the first side and a length of the second side may be the same.
[0028] Also, the active area may not include the active corner cut area in the corner area facing the source area.
[0029] The display driving device according to the embodiment may include any of the semiconductor devices for driving the display.
[0030] According to the embodiment, the gate oxide thinning can be improved by blocking electric field concentration through an active corner cut in a classic semiconductor device. Accordingly, the embodiment has the technical effect of improving breakdown voltage distribution characteristics by improving leakage characteristics in a classic semiconductor device.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0031] FIG. **1** is a partial cross-sectional photograph of a high voltage (HV) MOSFET device

according to the prior art.
[0032] FIG. **2**A is an exemplary configuration diagram of a display system to which a display driving device according to an embodiment is applied.
[0033] FIG. **2**B is a partial block diagram of a gate driver according to an embodiment.
[0034] FIG. **3** is a plan view of a semiconductor device **200** for driving a display according to an embodiment.
[0035] FIG. **4** is a cross-sectional view taken along line A**1**-A**2** of the semiconductor device **200** for driving a display according to the embodiment shown in FIG. **3**.
[0036] FIG. **5** is an enlarged view of the active area **200**A of the semiconductor device **200** for driving a display according to the embodiment shown in FIG. **3**.
[0037] FIG. **6** shows comparative data of the breakdown voltage distribution characteristic (E) of the semiconductor device **200** for driving a display according to the embodiment and the breakdown voltage distribution characteristic (R) of the comparative example.

DETAILED DESCRIPTION

[0038] Hereinafter, embodiments disclosed in the present specification will be described in detail with reference to the attached drawings, but identical or similar components will be assigned the same reference numbers regardless of the reference numerals, and duplicate descriptions thereof will be omitted. The suffixes 'module' and 'part' for components used in the following description are given or used interchangeably in consideration of ease of specification preparation, and do not have distinct meanings or roles in themselves. Additionally, the attached drawings are intended to facilitate easy understanding of the embodiments disclosed in this specification, and the technical idea disclosed in this specification is not limited by the attached drawings. Additionally, when an element such as a layer, region or substrate is referred to as being 'on' another component, this includes either directly on the other element or there may be other intermediate elements in between.

Embodiment

[0039] FIG. **2**A is an exemplary configuration diagram of a display system to which a display driving device according to an embodiment is applied, and FIG. **2**B is a partial block diagram of a gate driver according to the embodiment.
[0040] Referring to FIG. **2**A, a display system to which a display driving device according to the embodiment is applied may include a timing controller **101**, a gate driver **201**, a source driver (not shown), and a display panel **301**.
[0041] The gate driver **201** may receive the gate clock signal GCLK and control signal ALL from the timing controller **101** and provide gate driving signals (VOUT**1** to VOUT**5**) to the display panel **301**.
[0042] The timing controller **101** may provide a control signal and a gate clock signal GCLK to control the operation of the gate driver **201**. The control signal may include a gate enable signal for enabling the operation of the gate driver **201** or a control signal ALL for a power down mode, but is not limited thereto.
[0043] The display panel **301** may be a variety of flat display panels, such as a liquid crystal display panel, a light emitting diode display panel, and an organic light emitting diode display panel.
[0044] Additionally, the display system of the embodiment may include devices such as a source driver (not shown) and a power supply (not shown). The source driver may provide a source driving signal corresponding to data provided from the timing controller **101** to the display panel **301**. And, the power supply unit may provide voltages necessary for the operation of the timing controller **101**, gate driver **201**, and source driver.
[0045] Next, referring to FIG. **2**B, the gate driver **201** of the embodiment may include a gate signal processing unit **202**, a control unit (not shown), and an output circuit **203**.
[0046] The gate signal processing unit **202** may receive the gate clock signal GCLK provided from

the timing controller **101** and may output a gate signal G corresponding to the gate driving signal VOUT**1** to be provided to the display panel **301**.

[0047] The control unit may receive the control signal ALL and generate driving control signals having a time difference in activation time in response to the control signal ALL, but is not limited thereto.

[0048] Next, each output circuit **203** may include a level shifter **203***a* and an output buffer **203***b*, and may be configured in numbers corresponding to the output channels of the gate driver **201**. The output circuits **203** may respectively receive a gate signal G and a driving control signal ALL, and output gate driving signals VOUT**1** to VOUT**5**, respectively.

[0049] At this time, the level shifter **203***a* may compensate the level of the gate signal G in response to the inactive driving control signal ALL, may provide a gate signal G with compensated level to output buffer **203***b*. And the level shift **203***a* may perform an inverter operation for input, but is not limited to this.

[0050] As previously described, the display driver integrated circuit DDIC according to the embodiment may use a medium voltage MV semiconductor device or a high voltage HV semiconductor device such as TFT for panel control.

[0051] For example, the output buffer **203***b* of the embodiment may include a PMOS transistor and an NMOS transistor, and may have a configuration in which the drains of the PMOS transistor and the NMOS transistor are commonly connected. Accordingly, the output buffer **203***b* may be configured as a buffer composed of a CMOS transistor. And, in the output buffer **203***b*, a gate high voltage VGH may be applied to the PMOS transistor and a gate low voltage VGL may be applied to the NMOS transistor.

[0052] Additionally, a node where the drains of the PMOS transistor and the NMOS transistor of the output buffer **203***b* are commonly connected may form an output terminal that outputs the gate driving signal VOUT**1**.

[0053] By the above structure, the output buffer **203***b* may output a gate high voltage VGH when a low level signal is output from the level shifter **203***a*, and may output a gate low voltage VGL when a high level signal is output from the level shifter **203***a*.

[0054] Meanwhile, one of the technical objects of the embodiment is to improve the breakdown voltage distribution characteristics by improving leakage in a high-voltage semiconductor device.

[0055] As ultra-fine CMOS transistors of 28 nm or less is adopted due to the recent ultra-miniaturization of semiconductor processes, the thickness of the gate oxide becomes thinner.

[0056] So, there is a problem in securing the reliability of high-voltage semiconductor devices due to gate oxide thinning due to electric field concentration at the active corner.

[0057] FIG. **3** is a plan view of a semiconductor device **200** for driving a display according to an embodiment, FIG. **4** is a cross-sectional view taken along line A**1**-A**2** of the semiconductor device **200** for driving a display according to the embodiment shown in FIG. **3**, and FIG. **5** is an enlarged view of the active area **200**A of the semiconductor device **200** for driving a display according to the embodiment shown in FIG. **3**.

[0058] First, referring to FIG. **4**, the semiconductor device **200** for driving a display according to an embodiment may include a first conductivity type base layer **205**, a second conductivity type doping area **207** disposed on the first conductivity type base layer **205**, a source area **210** disposed on the second conductivity type doping area **207**, a drain area **220** disposed on the first conductivity type base layer **205**, a gate insulating film **232** disposed between the source area **210** and the drain area **220**, and a gate electrode **230** disposed on the gate insulating film **232**. And a device isolating area **250** may be disposed on the base layer **205**.

[0059] The semiconductor device **200** for driving a display according to the embodiment may be a MOSFET with an asymmetric structure, but is not limited thereto.

[0060] Referring to FIGS. **3** and **5**, the semiconductor device **200** for driving a display according to the embodiment may include an active area **200**A including the second conductivity type doping

area **207** and the source area **210**.
[0061] Additionally, the semiconductor device **200** for driving a display according to the embodiment may include an active corner cut area **200**AC in the active area **200**A in a plan view.
[0062] The active corner cut area **200**AC may have a right-angled triangle shape, but is not limited thereto. For example, the active corner cut area **200**AC may include a first side a and a second side b perpendicular to it. The length of the first side a and the length of the second side b may be the same, but are not limited thereto. The length of the first side a and the second side b may each be 1 μm or less, but are not limited thereto.
[0063] In addition, in the semiconductor device **200** for driving a display according to the embodiment, the active area **200**A may include a first active area **200**A**1** at the center of the gate electrode **230** and a second active area **200**A**2** outside where the active corner cut area **200**AC is located.
[0064] In the embodiment, a width Wa**1** of the first active area **200**A**1** in the center may be larger than the width Wa**2** of the second active area **200**A**2** on the outside.
[0065] In the embodiment, the difference between the width Wa**1** of the first active area **200**A**1** in the center and the width Wa**2** of the second active area **200**A**2** on the outside may not result in an actual increase in operating voltage.
[0066] According to the embodiment, by providing an active corner cut area **200**AC in the active area **200**A in a high voltage semiconductor device, gate oxide thinning can be improved by blocking electric field concentration in the corner area. Accordingly, the embodiment has the technical effect of improving breakdown voltage distribution characteristics by improving leakage characteristics in a high-voltage semiconductor device.
[0067] For example, FIG. **6** shows data on the breakdown voltage distribution characteristic E of the semiconductor device **200** for driving a display according to the embodiment and the breakdown voltage distribution characteristic R of the comparative example.
[0068] According to embodiment E, compared to comparative example R, by providing an active corner cut area **200**AC in the active area **200**A, there is a technical effect of improving leakage distribution characteristics in a high-voltage semiconductor device by blocking electric field concentration at the corner.
[0069] According to an embodiment, gate oxide thinning can be improved by blocking electric field concentration through an active corner cut in a classic semiconductor device. Accordingly, the embodiment has the technical effect of improving breakdown voltage distribution characteristics by improving leakage characteristics in a classic semiconductor device.
[0070] Although the above description focuses on embodiments, this is only an example and does not limit the embodiments, so those of ordinary skill in the field to which the embodiment belongs will recognize that various modifications and applications not exemplified above are possible without departing from the essential characteristics of the present embodiment. For example, each component specifically shown in the examples can be modified and implemented. And these variations and differences related to application should be interpreted as being included in the scope of the embodiments set forth in the appended claims.

Claims

1. A semiconductor device for driving a display comprising: a first conductivity type base layer; a second conductivity type doping area disposed on the first conductivity type base layer; a source area disposed on the second conductivity type doping area; a drain area disposed on the first conductivity type base layer; a gate insulating film disposed between the source area and the drain area; a gate electrode disposed on the gate insulating film; and one or more device isolating areas disposed on the base layer; wherein an active area having the second conductivity type doping area and the source area comprises an active corner cut area in a corner area facing the drain area.

2. The semiconductor device according to claim 1, wherein the active area comprises a first active area at a center of the gate electrode and a second active area at the active corner cut area.
3. The semiconductor device according to claim 2, wherein a width of the first active area is larger than a width of the second active area.
4. The semiconductor device according to claim 2, wherein the active corner cut area comprises a first active corner cut area disposed at an upper edge of the second active area facing the drain area, and a second active corner cut area disposed at a lower edge of the second active area facing the drain area.
5. The semiconductor device according to claim 2, wherein a distance from the first active area to the drain area is shorter than a distance from the second active area to the drain area.
6. The semiconductor device according to claim 2, wherein a distance from the first active area to the outside of the gate electrode in a direction of the drain area is shorter than a distance from the second active area to the gate electrode in a direction of the drain area.
7. The semiconductor device according to claim 1, wherein the active corner cut area comprises a right-angled triangle shape.
8. The semiconductor device according to claim 7, wherein the active corner cut area comprises a first side and a second side perpendicular to the first side of the active corner cut area, and wherein a length of the first side and a length of the second side are the same.
9. The semiconductor device according to claim 1, wherein the active area does not comprise the active corner cut area in the corner area facing the source area.
10. A display driving device comprising the semiconductor device for driving the display according to claim 1.
11. A semiconductor device for driving a display comprising: a first conductivity type base layer; a second conductivity type doping area disposed on the first conductivity type base layer; a source area disposed on the second conductivity type doping area; a drain area disposed on the first conductivity type base layer; a gate insulating film disposed between the source area and the drain area; and a gate electrode disposed on the gate insulating film; wherein the second conductivity type doping area comprises an active corner cut area in a corner area facing the drain area in a plan view.
12. The semiconductor device according to claim 11, wherein an active area comprises the second conductivity type doping area and the source area, and wherein the active area comprises a first active area at a first region vertically overlapping the gate electrode and a second active area at a second region laterally overlapping the active corner cut area.
13. The semiconductor device according to claim 12, wherein a lateral width of the first active area is larger than a lateral width of the second active area.
14. The semiconductor device according to claim 12, wherein the active corner cut area comprises a first active corner cut area disposed at an upper edge of the second active area facing the drain area, and a second active corner cut area disposed at a lower edge of the second active area facing the drain area.
15. The semiconductor device according to claim 12, wherein a distance from the first active area to the drain area is shorter than a distance from the second active area to the drain area.
16. The semiconductor device according to claim 12, wherein a distance from the first active area to the outside of the gate electrode in a direction of the drain area is shorter than a distance from the second active area to the gate electrode in a direction of the drain area.
17. The semiconductor device according to claim 11, wherein the active corner cut area comprises a right-angled triangle shape.
18. The semiconductor device according to claim 17, wherein the active corner cut area comprises a first side and a second side perpendicular to the first side of the active corner cut area, and wherein a length of the first side and a length of the second side are the same.
19. The semiconductor device according to claim 11, wherein the active area does not comprise the

active corner cut area in the corner area facing the source area.

20. A display driving device comprising the semiconductor device for driving the display according to claim 11.