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Display Substrate, Manufacturing Method Thereof, and Display Apparatus

Abstract

A display substrate, a preparation method thereof, and a display apparatus are provided, wherein the display substrate includes a display area and an edge area, and the display substrate further comprises a substrate and a power supply line arranged on the substrate and located in the edge area, the power supply line includes a first power supply portion and a second power supply portion connected with each other, the second power supply portion being located on a side of the first power supply portion far away from the substrate; the display area including a plurality of display units, at least one display unit includes a pixel driving circuit and a light emitting device, the pixel driving circuit being electrically connected with an anode of the light emitting device, the power supply line being electrically connected with a cathode of the light emitting device.

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATION [0001] The present application is a U.S. National Phase Entry of International Application No. PCT/CN2022/073243 having an international filing date of Jan. 21, 2022. The above-identified application is hereby incorporated by reference.

TECHNICAL FIELD
[0002] The present disclosure relates to, but is not limited to, the field of display technologies, and in particular to a display substrate, a preparation method thereof, and a display apparatus.
BACKGROUND
[0003] An Organic Light Emitting Diode (OLED for short) is an active light emitting display device, which has advantages of auto-luminescence, a wide viewing angle, a high contrast ratio, low power consumption, an extremely high response speed, lightness and thinness, bendability, and a low cost, etc. With constant development of display technologies, a flexible display apparatus (Flexible Display) using an OLED as a light emitting device and performing signal control using a Thin Film Transistor (TFT for short) has become a mainstream product in the field of display at present.
SUMMARY
[0004] The following is a summary of subject matters described herein in detail. The summary is not intended to limit the protection scope of claims.
[0005] In a first aspect, the invention provides a display substrate, which includes a display area and an edge area located on a side of the display area, and the display substrate further includes a substrate and a power supply line arranged on the substrate and located in the edge area, wherein the power supply line includes a first power supply portion and a second power supply portion connected with each other, and the second power supply portion is located on a side of the first power supply portion away from the substrate;
[0006] The display area includes a plurality of display units, wherein at least one display unit includes a pixel driving circuit and a light emitting device, wherein the pixel driving circuit is electrically connected with an anode of the light emitting device, and the power supply line is electrically connected with a cathode of the light emitting device, an orthographic projection of the second power supply portion on the substrate is at least partially overlapped with an orthographic projection of the first power supply portion on the substrate, and a distance between an end of the second power supply portion away from the display area and the display area is greater than or equal to a distance between an end of the first power supply portion away from the display area and the display area.
[0007] In some possible implementations, the edge area includes a circuit region and an isolation dam region sequentially arranged in a direction away from the display area, wherein the circuit region includes: a first circuit region, a second circuit region, and a third circuit region sequentially arranged in a direction away from the display area; [0008] the pixel driving circuit includes a writing transistor, a compensation transistor, a light emitting transistor, a first scan signal line, a second scan signal line and a light emitting signal line; wherein the first scan signal line is electrically connected to a control electrode of the writing transistor, the second scan signal line is electrically connected to a control electrode of the compensation transistor, and the light emitting

signal line is electrically connected to a control electrode of the light emitting transistor; and the writing transistor and the compensation transistor have different transistor types; [0009] the display substrate further includes a first driving circuit located in the first circuit region, a second driving circuit located in the second circuit region, and a third driving circuit located in the third circuit region and the isolation dam region; [0010] the first driving circuit is electrically connected with the first scan signal line, the second driving circuit is electrically connected with the second scan signal line, and the third driving circuit is electrically connected with the light emitting signal line; [0011] the first power supply portion is located in the isolation dam region, and the second power supply portion is located in the isolation dam region and the circuit region; and [0012] an orthographic projection of the second power supply portion on the substrate is at least partially overlapped with an orthographic projection of the third driving circuit on the substrate, and has no overlapping area with an orthographic projection of the second driving circuit on the substrate.

[0013] In some possible implementations, the display substrate further includes: a crack detection line located in the isolation dam region, wherein the crack detection line is arranged in the same layer as the first power supply portion and located on a side of the first power supply portion away from the display area; and a distance between the first power supply portion and the crack detection line is greater than or equal to 1 micron and less than or equal to 6 microns.

[0014] In some possible implementations, a distance between the first power supply portion and the third driving circuit is greater than or equal to 1 micron and less than or equal to 6 microns.

[0015] In some possible implementations, the display substrate further includes a first planarization layer located in the display area, the circuit region and the isolation dam region and a first protective layer located in the isolation dam region; the first planarization layer is arranged between the first power supply portion and the second power supply portion and is arranged in the same layer as the first protective layer; and an orthographic projection of the first protective layer on the substrate covers an orthographic projection of the crack detection line on the substrate and at least partially overlaps with an orthographic projection of the first power supply portion on the substrate.

[0016] In some possible implementations, the third driving circuit includes a clock signal line located in the isolation dam region; wherein the clock signal line is arranged in the same layer as the first power supply portion and is located on a side of the first power supply portion close to the display area; and an orthographic projection of the first planarization layer on the substrate covers an orthographic projection of the clock signal line on the substrate, and has no overlapping area with an orthographic projection of the first power supply portion on the substrate.

[0017] In some possible implementations, the second power supply portion is provided with a plurality of second vias exposing the first planarization layer, and the plurality of second vias are arranged in a matrix; and an orthographic projection of the plurality of second vias on the substrate overlaps at least partially with an orthographic projection of the third driving circuit on the substrate.

[0018] In some possible implementations, the display substrate further includes a second planarization layer located in the display area and the circuit region and a second protective layer located in the isolation dam region; the second planarization layer is located on a side of the second power supply portion away from the substrate and is arranged in the same layer as the second protective layer; an orthographic projection of the second protective layer on the substrate covers an orthographic projection of the first protective layer on the substrate, and an orthographic projection of the second planarization layer on the substrate covers an orthographic projection of the second vias on the substrate.

[0019] In some possible implementations, the display substrate further includes an auxiliary power supply line located in the edge area; the anode is located on a side of the second planarization layer away from the substrate and is arranged in the same layer as the auxiliary power supply line; the auxiliary power supply line is electrically connected with the second power supply portion; and an orthographic projection of the auxiliary power supply line on the substrate overlaps at least

partially with orthographic projections of the first driving circuit, the second driving circuit, and the third driving circuit on the substrate.

[0020] In some possible implementations, the auxiliary power supply line is provided with a plurality of fifth vias exposing the second planarization layer, and the plurality of fifth vias are arranged in a matrix; the plurality of fifth vias are located in the first circuit region, the second circuit region and the third circuit region; and an orthographic projection of the fifth vias located in the third circuit region on the substrate at least partially overlaps an orthographic projection of second vias on the substrate.

[0021] In some possible implementations, the display substrate further includes a pixel definition layer located in the display area and an isolation layer located in the circuit region; the pixel definition layer is located on a side of the anode away from the substrate and is arranged in the same layer as the isolation layer; and a distance between an end of the isolation layer away from the display area and the display area is less than or equal to a distance between an end of the second planarization layer away from the display area and the display area, and an orthographic projection of the isolation layer on the substrate covers an orthographic projection of fifth vias on the substrate.

[0022] In some possible implementations, the display substrate further includes: an organic light emitting layer sequentially stacked on the substrate and located in the display area and a cathode located in the display area and the circuit region; and the cathode is electrically connected with the auxiliary power supply line.

[0023] In some possible implementations, the isolation dam region further includes a first isolation dam and a second isolation dam; the second isolation dam is located on a side of the first isolation dam away from the display area and located on a side of the second protective layer close to the display area.

[0024] In some possible implementations, the display substrate further includes a first dam foundation, a third dam foundation, a fifth dam foundation, and a seventh dam foundation which are located in the isolation dam region; the first dam foundation is arranged in the same layer as the first planarization layer, the third dam foundation is arranged in the same layer as the second planarization layer, the fifth dam foundation is arranged in the same layer as the pixel definition layer, and the seventh dam foundation is located on a side of the pixel definition layer away from the substrate; the second power supply portion covers the first dam foundation, the third dam foundation is arranged on the second power supply portion covering the first dam foundation and an orthographic projection of the third dam foundation on the substrate covers an orthographic projection of the first dam foundation on the substrate, the fifth dam foundation is arranged on the third dam foundation and an orthographic projection of the fifth dam foundation on the substrate covers the orthographic projection of the third dam foundation on the substrate, and the seventh dam foundation is arranged on the fifth dam foundation and the orthographic projection of the fifth dam foundation on the substrate covers an orthographic projection of the seventh dam foundation on the substrate; the auxiliary power supply line partially covers the third dam foundation; and the first dam foundation, the second power supply portion covering the first dam foundation, the third dam foundation, the fifth dam foundation, and the seventh dam foundation form a second isolation dam.

[0025] In some possible implementations, the display substrate further includes a second dam foundation, a fourth dam foundation and a sixth dam foundation located in the isolation dam region; the second dam foundation is arranged in the same layer as the second planarization layer, the fourth dam foundation is arranged in the same layer as the pixel definition layer, and the sixth dam foundation is arranged in the same layer as the seventh dam foundation; the second dam foundation is arranged on the second power supply portion, the fourth dam foundation is arranged on the auxiliary power supply line covering the second dam foundation and an orthographic projection of the fourth dam foundation on the substrate covers an orthographic projection of the

second dam foundation on the substrate, and the sixth dam foundation is arranged on the fourth dam foundation and the orthographic projection of the fourth dam foundation on the substrate covers an orthographic projection of the sixth dam foundation on the substrate; and the second dam foundation, the auxiliary power supply line covering the second dam foundation, the fourth dam foundation and the sixth dam foundation form a first isolation dam.

[0026] In some possible implementations, an orthographic projection of the first isolation dam on a substrate at least partially overlaps with the clock signal line.

[0027] In a second aspect, the present disclosure further provides a display apparatus, including the display substrate described above.

[0028] In a third aspect, the present disclosure further provides a method for preparing a display substrate, which is arranged for preparing the display substrate described above, wherein the display substrate includes display area and an edge area located around the display area, and the preparation method includes: providing the substrate; and sequentially forming a first power supply portion and a second power supply portion on the substrate to form a power supply line located in the edge area, an orthographic projection of the second power supply portion on the substrate being at least partially overlapped with an orthographic projection of the first power supply portion on the substrate, and a distance between an end of the second power supply portion away from the display area and the display area being greater than or being equal to a distance between an end of the first power supply portion away from the display area and the display area.

[0029] In some possible implementations, sequentially forming the first power supply portion and the second power supply portion on the substrate includes: [0030] forming a pixel driving circuit in a display area on the substrate, a first driving circuit and a second driving circuit located in the circuit region, a third driving circuit located in the third circuit region, a first power supply portion and a crack detection line located in the isolation dam region; [0031] forming a first planarization layer located in the display area and the circuit region and a first dam foundation and a first protective layer located in the isolation dam region on the substrate on which the first power supply portion is formed; [0032] forming a connection electrode located in a display area and a second power supply portion located in a circuit region and an isolation dam region on the substrate on which the first planarization layer is formed; [0033] forming a second planarization layer located in the display area and the circuit region, a second dam foundation, a third dam foundation and a second protective layer located in the isolation dam region on the substrate on which the second power supply portion is formed; [0034] forming an anode located in a display area and an auxiliary power supply line located in an edge area on the substrate on which the second planarization layer is formed; [0035] forming a pixel definition layer located in a display area, an isolation layer located in a circuit region, and a fourth dam foundation and a fifth dam foundation located in an isolation dam region on the substrate on which the auxiliary power supply line is formed; [0036] and forming an organic light emitting layer located in the display area, a cathode located in the display area and the circuit region, and a sixth dam foundation and a seventh dam foundation located in the isolation dam region on the substrate on which the pixel definition layer is formed.

[0037] Other aspects may be understood upon reading and understanding the drawings and the detailed description.

Description

BRIEF DESCRIPTION OF DRAWINGS

[0038] Accompanying drawings are used for providing further understanding of technical solutions of the present disclosure, constitute a part of the specification, and together with the embodiments of the present disclosure, are used for explaining the technical solutions of the present disclosure but not to constitute limitations on the technical solutions of the present disclosure. Shapes and

sizes of various components in the drawings do not reflect actual scales, but are only intended to schematically illustrate contents of the present disclosure.

[0039] FIG. **1** is a schematic diagram of a structure of a display substrate;

[0040] FIG. **2** is a schematic diagram of an equivalent circuit of a pixel drive circuit;

[0041] FIG. **3** is a schematic diagram of a structure of a display substrate according to an embodiment of the present disclosure;

[0042] FIG. **4** is a top view of a display substrate according to an embodiment of the present disclosure;

[0043] FIG. **5** is a top view of a part of a film layer of a display substrate provided by an embodiment of the present disclosure;

[0044] FIG. **6** is a schematic diagram of a structure of a display substrate according to an exemplary embodiment.

[0045] FIG. **7** is a schematic diagram after a display circuit layer is formed.

[0046] FIG. **8** is a cross-sectional view along an A-A direction of FIG. **7**.

[0047] FIG. **9** is a schematic diagram after a first organic layer is formed.

[0048] FIG. **10** is a cross-sectional view along an A-A direction of FIG. **9**.

[0049] FIG. **11** is a schematic diagram after a second source-drain metal layer is formed.

[0050] FIG. **12** is a schematic diagram along an A-A direction in FIG. **11**.

[0051] FIG. **13** is a schematic diagram after a second organic layer is formed.

[0052] FIG. **14** is a cross-sectional view along an A-A direction of FIG. **13**.

[0053] FIG. **15** is a schematic diagram after a transparent conductive layer is formed.

[0054] FIG. **16** is a cross-sectional view along an A-A direction of FIG. **15**.

[0055] FIG. **17** is a schematic diagram after a third organic layer is formed.

[0056] FIG. **18** is a schematic diagram along an A-A direction in FIG. **17**.

[0057] FIG. **19** is a schematic diagram after an organic light emitting layer is formed.

[0058] FIG. **20** is a cross-sectional view along an A-A direction of FIG. **19**.

[0059] FIG. **21** is a schematic diagram after a cathode is formed.

[0060] FIG. **22** is a cross-sectional view along an A-A direction of FIG. **21**.

DETAILED DESCRIPTION

[0061] To make objectives, technical solutions, and advantages of the present disclosure clearer, the embodiments of the present disclosure will be described in detail with reference to the accompanying drawings. It is to be noted that implementation modes may be implemented in multiple different forms. Those of ordinary skills in the art may easily understand such a fact that implementations and contents may be transformed into various forms without departing from the purpose and scope of the present disclosure. Therefore, the present disclosure should not be explained as being limited to contents described in following implementation modes only. The embodiments in the present disclosure and features in the embodiments may be combined randomly with each other if there is no conflict.

[0062] In the drawings, a size of each constituent element, a thickness of a layer, or a region is exaggerated sometimes for clarity. Therefore, one implementation mode of the present disclosure is not necessarily limited to the sizes, and shapes and sizes of various components in the drawings do not reflect actual scales. In addition, the drawings schematically illustrate ideal examples, and one implementation of the present disclosure is not limited to the shapes, numerical values, or the like shown in the drawings.

[0063] Ordinal numerals such as “first”, “second”, and “third” in the specification are set to avoid confusion of constituent elements, but not to set a limit in quantity.

[0064] In the specification, for convenience, wordings indicating orientation or positional relationships, such as “middle”, “upper”, “lower”, “front”, “back”, “vertical”, “horizontal”, “top”, “bottom”, “inside”, and “outside”, are used for illustrating positional relationships between constituent elements with reference to the drawings, and are merely for facilitating the description

of the specification and simplifying the description, rather than indicating or implying that a referred apparatus or element must have a particular orientation and be constructed and operated in the particular orientation. Therefore, they cannot be understood as limitations on the present disclosure. The positional relationships between the constituent elements may be changed as appropriate according to directions for describing the various constituent elements. Therefore, appropriate replacements may be made according to situations without being limited to the wordings described in the specification.

[0065] In the specification, unless otherwise specified and defined explicitly, terms “mount”, “mutually connect”, and “connect” should be understood in a broad sense. For example, a connection may be a fixed connection, or a detachable connection, or an integrated connection. It may be a mechanical connection or an electrical connection. It may be a direct mutual connection, or an indirect connection through middleware, or internal communication between two components. Those of ordinary skill in the art may understand specific meanings of these terms in the present disclosure according to specific situations.

[0066] In the specification, a transistor refers to a component which includes at least three terminals, i.e., a gate electrode, a drain electrode and a source electrode. The transistor has a channel region between the drain electrode (drain electrode terminal, drain region, or drain) and the source electrode (source electrode terminal, source region, or source), and a current may flow through the drain electrode, the channel region, and the source electrode. It is to be noted that, in the specification, the channel region refers to a region through which the current mainly flows.

[0067] In the specification, a first electrode may be a drain electrode, and a second electrode may be a source electrode. Or, the first electrode may be the source electrode, and the second electrode may be the drain electrode. In cases that transistors with opposite polarities are used, a current direction changes during operation of a circuit, or the like, functions of the “source electrode” and the “drain electrode” are sometimes interchangeable. Therefore, the “source electrode” and the “drain electrode” are interchangeable in the specification.

[0068] In the specification, “electrical connection” includes a case that constituent elements are connected together through an element with a certain electrical effect. The “element with the certain electrical effect” is not particularly limited as long as electrical signals may be sent and received between the connected constituent elements. Examples of the “element with the certain electrical effect” not only include electrodes and wirings, but also include switch elements such as transistors, resistors, inductors, capacitors, other elements with various functions, etc.

[0069] In the specification, “parallel” refers to a state in which an angle formed by two straight lines is above −10° and below 10°, and thus also includes a state in which the angle is above −5° and below 5°. In addition, “perpendicular” refers to a state in which an angle formed by two straight lines is above 80° and below 100°, and thus also includes a state in which the angle is above 85° and below 95°.

[0070] In the specification, a “film” and a “layer” are interchangeable. For example, a “conductive layer” may be replaced with a “conductive film” sometimes. Similarly, an “insulating film” may be replaced with an “insulation layer” sometimes.

[0071] In the present disclosure, “about” refers to that a boundary is defined not so strictly and numerical values within process and measurement error ranges are allowed.

[0072] A low-temperature polycrystalline oxide display product provides a low-voltage signal to a display area through a power supply line. Because of the impedance of the power supply line and the voltage drop of the voltage signal transmission, the voltage loss of the power supply line reduces the uniformity of the display brightness of the display products and increases the power consumption of the display products, which has become an important factor affecting the high-quality display.

[0073] FIG. **1** is a schematic diagram of a structure of a display substrate. As shown in FIG. **1**, the display substrate may include a display area **100**, a bonding area **200** on a side of the display area

100, and an edge area **300** on other sides of the display area **100**.
[0074] In an exemplary embodiment, the display area **100** at least includes a plurality of display units (sub-pixels) arranged regularly.
[0075] In an exemplary embodiment, within a plane perpendicular to the display substrate, a display unit may include a driving structure layer arranged on a substrate, a light emitting device arranged on the driving structure layer, and an encapsulation layer arranged on the emitting device. Among them, the driving structure layer may include a pixel driving circuit, the light emitting device is configured to emit light and is connected with the pixel driving circuit, and the pixel driving circuit is configured to drive the light emitting device to emit light.
[0076] In an exemplary embodiment, the pixel driving circuit may include a plurality of thin film transistors (abbreviated as TFT) and a storage capacitor, such as 3T1C, 4T1C, 5T1C, 6T1C or 7T1C, which is not limited in the present disclosure.
[0077] FIG. **2** is a schematic diagram of an equivalent circuit of a pixel driving circuit. As shown in FIG. **2**, the pixel driving circuit may include seven transistors (a first transistor T**1** to a seventh transistor T**7**), one storage capacitor C, and seven signal lines (a data signal line D, a first scan signal line S**1**, a second scan signal line S**2**, a third scan signal line S**3**, a light emitting signal line E, an initial signal line INIT, a first power supply line VDD, and a second power supply line VSS).
[0078] In an exemplary embodiment, a first end of the storage capacitor C is connected with the first power supply line VDD, and a second end of the storage capacitor C is connected with the second node N**2**, namely the second end of the storage capacitor C is connected with a control electrode of the third transistor T**3**.
[0079] In an exemplary embodiment, a control electrode of the first transistor T**1** is connected to the third scan signal line S**3**, a first electrode of the first transistor T**1** is connected to the initial signal line INIT, and a second electrode of the first transistor is connected to a second node N**2**. When a scan signal with an on-level is applied to the third scan signal line S**3**, the first transistor T**1** transmits an initialization voltage to the control electrode of the third transistor T**3** so as to initialize a charge amount of the control electrode of the third transistor T**3**.
[0080] In an exemplary embodiment, a control electrode of the second transistor T**2** is connected with the second scan signal line S**2**, a first electrode of the second transistor T**2** is connected with the second node N**2**, and a second electrode of the second transistor T**2** is connected with a third node N**3**. The second transistor T**2** may be a compensation transistor, and when a scan signal with an on-level is applied to the second scan signal line S**2**, the second transistor T**2** enables the control electrode of the third transistor T**3** to be connected with a second electrode of the third transistor T**3**.
[0081] In an exemplary embodiment, the control electrode of the third transistor T**3** is connected with the second node N**2**, namely the control electrode of the third transistor T**3** is connected with the second terminal of the storage capacitor C, a first electrode of the third transistor T**3** is connected with a first node N**1**, and the second electrode of the third transistor T**3** is connected with the third node N**3**. The third transistor T**3** may be referred to as a driving transistor, and the third transistor T**3** determines an amount of a drive current flowing between the first power supply line VDD and the second power supply line VSS according to a potential difference between the control electrode and the first electrode of the third transistor T**3**.
[0082] In an exemplary embodiment, a control electrode of the fourth transistor T**4** is connected with the first scan signal line S**1**, a first electrode of the fourth transistor T**4** is connected with the data signal line D, and a second electrode of the fourth transistor T**4** is connected with the first node N**1**. The fourth transistor T**4** may be referred to as a writing transistor, and when a scan signal with an on-level is applied to the first scan signal line S**1**, the fourth transistor T**4** enables a data voltage of the data signal line D to be input to the pixel driving circuit.
[0083] In an exemplary embodiment, a control electrode of the fifth transistor T**5** is connected with the light emitting signal line E, a first electrode of the fifth transistor T**5** is connected with the first

power supply line VDD, and a second electrode of the fifth transistor T**5** is connected with the first node N**1**. A control electrode of the sixth transistor T**6** is connected with the light emitting signal line E, a first electrode of the sixth transistor T**6** is connected with the third node N**3**, and a second electrode of the sixth transistor T**6** is connected with a first electrode of a light emitting device. The fifth transistor T**5** and the sixth transistor T**6** may be referred to as light emitting transistors. When a light emitting signal with an on-level is applied to the light emitting signal line E, the fifth transistor T**5** and the sixth transistor T**6** enable the light emitting device to emit light by forming a driving current path between the first power supply line VDD and the second power supply line VSS.

[0084] In an exemplary embodiment, a control electrode of the seventh transistor T**7** is connected with the third scan signal line S**3**, a first electrode of the seventh transistor T**7** is connected with the initial signal line INIT, and a second electrode of the seventh transistor T**7** is connected with the first electrode of the light emitting device. When a scan signal with an on-level is applied to the third scan signal line S**3**, the seventh transistor T**7** transmits an initialization voltage to the first electrode of the light emitting device so as to initialize a charge amount accumulated in the first electrode of the light emitting device or release a charge amount accumulated in the first electrode of the light emitting device.

[0085] In an exemplary embodiment, a cathode of the light emitting device is connected with the second power supply line VSS.

[0086] In an exemplary embodiment, the first power supply line VDD continuously provides a high level signal, and the second power supply line VSS continuously provides a low level signal.

[0087] In an exemplary embodiment, the first transistor T**1** to the seventh transistor T**7** may include a P-type transistor and an N-type transistor.

[0088] In an exemplary embodiment, the first transistor T**1** and the second transistor T**2** are N-type metal oxide transistors, and the third transistors T**3** to the seventh transistors T**7** are P-type low-temperature polysilicon thin film transistors.

[0089] In an exemplary embodiment, the writing transistor and the compensation transistor have different transistor types.

[0090] In an exemplary embodiment, the first scan signal line S**1**, the second scan signal line S**2**, the third scan signal line S**3**, the light emitting signal line E and the initial signal line INIT extend along a first direction, and the second power supply line VSS, the first power supply line VDD and the data signal line D extend along a second direction, the first direction intersecting with the second direction.

[0091] In an exemplary embodiment, the light emitting device may be an Organic light emitting Diode (OLED), including a first electrode (anode), an organic light emitting layer, and a second electrode (cathode) that are stacked. The anode of the light emitting device is connected with the pixel driving circuit.

[0092] The display substrate provided by the embodiment of the present disclosure may be a low-temperature polycrystalline oxide display substrate.

[0093] In an exemplary embodiment, the bonding region **200** at least includes isolation dams and bonding circuits connecting signal lines of plurality of display units to an external drive apparatus, and the edge area **300** at least includes isolation dams, gate driving circuits and a power line for transmitting voltage signals to the plurality of display units. The isolation dams of the bonding region **200** and the edge area **300** form an annular structure surrounding the display area **100**.

[0094] FIG. **3** is a structural schematic diagram of the display substrate provided by the embodiment of the present disclosure, and is an enlarged view of the C area in FIG. **1**. FIG. **4** is a top view of the display substrate provided by the embodiment of the present disclosure, and FIG. **3** is a cross-sectional view along an A-A direction of FIG. **4**. FIG. **5** is a top view of a part of film layers of the display substrate provided by the embodiment of the present disclosure. As shown in FIG. **3** to FIG. **5**, in a direction parallel to the display substrate, the edge area **300** includes a circuit

region **301** and an isolation dam region **302** which are sequentially arranged along a direction away from the display area **100**. The circuit region **301** includes a first circuit region **301**A, a second circuit region **301**B, and a third circuit region **301**C that are sequentially arranged along a direction away from the display area **100**.

[0095] In an exemplary embodiment, the circuit region **301** includes at least a gate driving circuit. Among them, the gate driving circuit is electrically connected to the first scan signal line, the second scan signal line and the light emitting signal line of the pixel driving circuit **101** in the display area **100** respectively.

[0096] In an exemplary embodiment, the gate driving circuit located in the edge area **300** may include a first driving circuit **201**, a second driving circuit **202** and a third driving circuit **203**.

[0097] In an exemplary embodiment, the first driving circuit **201** is electrically connected to a first scan signal line.

[0098] In an exemplary embodiment, the second driving circuit **202** is electrically connected to a second scan signal line. Among them, the second driving circuit **202** may further include a clock signal line CLK.

[0099] In an exemplary embodiment, the third driving circuit **203** is electrically connected to a light emitting signal line and may further include a clock signal line ECLK.

[0100] In an exemplary embodiment, the first driving circuit **201** may have an 8T2C circuit structure or other circuit structures.

[0101] In an exemplary embodiment, a second driving circuit **202** may have a 10T3C circuit structure or a 13T3C circuit structure, which is not limited in the present disclosure.

[0102] In an exemplary embodiment, the first driving circuit **201** is located in the first circuit region **301**A, the second driving circuit **202** is located in the second circuit region **301**B, and the third driving circuit **203** is located in the third circuit region **301**C and the isolation dam region **302**.

[0103] In an exemplary embodiment, the isolation dam region **302** at least includes a power supply line **310** connected to a cathode of the light emitting device, a first isolation dam **410**, a second isolation dam **420**, a crack detection line **320**, and a clock signal line ECLK of the third driving circuit **203**.

[0104] In an exemplary embodiment, the power supply line **310** extends along a direction parallel to an edge of a display area and is connected to a second power supply line VSS of a pixel driving circuit **101** in the display area **100**.

[0105] In an exemplary embodiment, the power supply line **310** includes a first power supply portion **310**A and a second power supply portion **310**B connected to each other, wherein the second power supply portion **310**B is located on a side of the first power supply portion **310**A away from the substrate.

[0106] In an exemplary embodiment, an orthographic projection of the second power supply portion **310**B on the substrate overlaps at least partially with an orthographic projection of the first power supply portion **310**A on the substrate, and a distance between an end of the second power supply portion **310**B away from the display area **100** and the display area **100** is greater than or equal to a distance between an end of the first power supply portion **310**A away from the display area **100** and the display area **100**.

[0107] In an exemplary embodiment, the first power supply portion **310**A is located in an isolation dam region **302**.

[0108] In an exemplary embodiment, the second power supply portion **310**B is located at least in an isolation dam region **302** and a third circuit region **301**C. The second power supply portion **310**B may be located in a second circuit region **301**B, wherein an orthographic projection of the second power supply portion **310**B on the substrate overlaps at least partially an orthographic projection of the third driving circuit **203** on the substrate, and has no overlapping area with an orthographic projection of the second driving circuit **202** on the substrate.

[0109] In an exemplary embodiment, the second driving circuit includes a clock signal line CLK. A distance between an end of the second power supply portion **310**B close to an end of a display area **100** and the display area **100** is greater than a distance between an end of the clock signal line CLK away from the display area **100** and the display area **100**. That is, there is no overlapping area between an orthographic projection of the second power supply portion **310**B on the substrate and an orthographic projection of the clock signal line CLK on the substrate.
[0110] In an exemplary embodiment, the crack detection line **320** extends along a direction parallel to an edge of a display area and is located on a side of a power supply line **310** away from the display area **100**. The crack detection line is arranged to detect whether there is a crack in the display substrate.
[0111] In an exemplary embodiment, the first isolation dam **410** and second isolation dam **420** extend along a direction parallel to an edge of a display area and are configured to block water vapor entering the display area **100** from an edge area **300**.
[0112] In an exemplary embodiment, a distance between a first isolation dam **410** and a display area **100** is less than a distance between a second isolation dam **420** and the display area **100**. That is, the second isolation dam **420** is arranged on a side of the first isolation dam **410** away from the display area **100**.
[0113] In an exemplary embodiment, the needed low voltage of a light emitting device connected with the pixel driving circuit in the display area **100** is introduced from a bonding pad of the bonding area **200**, enters the edge area **300** after passing through the bonding area **200**, and is transmitted to the second power supply line VSS of each pixel driving circuit through the annular power supply line **310** of the edge area **300**.
[0114] In the present disclosure, FIG. **3** illustrates a cross-sectional structure of a display area and a peripheral area of a top emission type OLED. According to a light emission direction, OLED can be categorized as a bottom-emission type, a top-emission type and a double-sided emission type. Compared with bottom-emission OLED, top-emission OLED has advantages of high aperture ratio, high color purity and easy to achieve high pixels per inch (abbreviated as PPI), which has gradually become a mainstream structure at present. For the top-emission OLED, because the light exit direction is at a cathode side, in order to ensure a good light transmittance, the cathode is required to be very thin, therefore, the voltage drop of the power supply line providing a low voltage for the cathode has an important effect on improving the uniformity of the display brightness.
[0115] As shown in FIG. **3** to FIG. **6**, combined with FIG. **7** to FIG. **22**, the display substrate of an exemplary embodiment of the present disclosure includes a display area **100** and an edge area **300**, wherein the edge area **300** includes a circuit region **301**, and an isolation dam region **302** which are sequentially arranged along a direction away from the display area **100**.
[0116] In an exemplary embodiment, the display area **100** of the display substrate includes: a substrate **10**; a first insulation layer **11** arranged on the substrate **10**; an active layer arranged on the first insulation layer **11**, the active layer at least including a first active layer; a second insulation layer **12** covering the active layer; a first gate metal layer, a third insulation layer **13**, a second gate metal layer and a fourth insulation layer **14** arranged sequentially on the second insulation layer **12**, the first gate metal layer including at least a first gate electrode; and the second insulation layer **12**, the third insulation layer **13**, and the fourth insulation layer **14** being provided with vias exposing the first active layer.
[0117] A first source-drain metal layer arranged on the fourth insulation layer **14**, wherein the source-drain metal layer at least includes a first source electrode and a first drain electrode, and the first source electrode and the first drain electrode are respectively connected to the first active layer through the vias exposing the first active layer; a first organic layer arranged on the first source-drain metal layer, the first organic layer at least comprises: a first planarization layer **15** covering the first source-drain metal layer, the first planarization layer **15** being provided with a first via exposing the first drain electrode; a second source-drain electrode layer arranged on the first

organic layer, wherein the second source-drain metal layer at least includes a connection electrode **17** arranged on the first planarization layer **15**, the connection electrode **17** being connected with the first drain electrode through the first via; a second organic layer arranged on the second source-drain electrode layer, wherein the second organic layer at least includes a second planarization layer **16** covering the connection electrode **17**, on which a second via exposing the connection electrode **17** is provided; a transparent conductive layer arranged on the second organic layer, wherein the transparent conductive layer at least includes an anode **21** arranged on the second planarization layer **16**, the anode **21** being connected with the connection electrode **17** through the second via; a third organic layer arranged on the transparent conductive layer, wherein the third organic layer at least includes a pixel definition layer **22** arranged on the anode **21**, the pixel definition layer **22** being provided with a fifth via exposing the anode **21**; an organic light emitting layer **24** arranged in the fifth via, wherein the organic light emitting layer **24** is connected to the anode **22**; a cathode **25** arranged on the organic light emitting layer **24** and the pixel definition layer **22**, wherein the cathode **25** is connected to the organic light emitting layer **24**.

[0118] In an exemplary embodiment, the edge area **300** of the display substrate includes: a substrate **10**; a first insulation layer **11** arranged on the substrate **10**; an active layer arranged on the first insulation layer **11**, wherein the active layer at least includes a second active layer, a third active layer and a fourth active layer located in a circuit region **301**; a second insulation layer **12** covering the active layer; a first gate metal layer arranged on the second insulation layer **12**, wherein the first gate metal layer at least includes a second gate electrode and a first capacitive electrode located in a first circuit region **301**A, a third gate electrode and a second capacitive electrode located in a second circuit region **301**B, a fourth gate electrode and a third capacitive electrode located in a third circuit region **301**C; a third insulation layer **13** covering the first metal gate layer; a second gate metal layer arranged in the third insulation layer **13**, wherein the second gate metal layer includes at least a fourth capacitive electrode located in the first circuit region **301**A, a fifth capacitive electrode located in the second circuit region **301**B, and a sixth capacitive electrode located in the third circuit region **301**C; [0119] a fourth insulation layer **14** covering the second gate metal layer, wherein a plurality of vias exposing the second active layer, the third active layer and the fourth active layer are provided on the fourth insulation layer **14** of the circuit region **301**; [0120] a first source-drain metal layer arranged on the fourth insulation layer **14**, wherein the first source-drain metal layer at least includes a second source electrode, a second drain electrode, a third source electrode, a third drain electrode, a fourth source electrode and a fourth drain electrode located in the circuit region **301**, and a power supply portion **310**A, a clock signal line ECLK and a crack detection line **320** located in the isolation dam region **302**; the second source electrode and the second drain electrode being respectively connected to the second active layer through the via exposing the second active layer, the third source electrode and the third drain electrode being respectively connected to the third active layer through the via exposing the third active layer, and the fourth source electrode and the fourth drain electrode being respectively connected to the fourth active layer through the via exposing the fourth active layer; [0121] a first organic layer arranged on the first source-drain metal layer, wherein the first organic layer at least includes a first planarization layer **15** located in the circuit region **301** and the isolation dam region **302**, and a first dam foundation **421** and a first protective layer **431** formed in the isolation dam region **302**; the first dam foundation **421** of the isolation dam region **302** being arranged on the first power supply portion **310**A, the first protective layer **431** being arranged on the crack detection line **320** and the first power supply portion **310**A, the first protective layer **431** covering the crack detection line **320** and covering an end of the first power supply portion **310**A far away from the display area, and the first planarization layer **15** covering the clock signal line ECLK; [0122] a second source-drain electrode layer arranged on the first organic layer, wherein the second source-drain metal layer at least includes a second power supply portion **310**B located in the isolation dam region **302**, the second power supply portion **310**B on which is provided with a second via

exposing the first planarization layer covering the first dam foundation **421**; [0123] a second organic layer arranged on the second source-drain electrode layer, wherein the second organic layer at least includes a second planarization layer **16** in the circuit region **301**, and a second dam foundation **411**, a third dam foundation **422** and a second protective layer **432** arranged in the isolation dam region **302**, the third dam foundation **422** being arranged on the second power supply portion **310**B covering the first dam foundation **421**, the second dam foundation **411** being arranged on the second power supply portion **310**B located at a side of the first dam foundation **421** adjacent to the display area **100**, the second protective layer **432** being arranged on the first protective layer **431** and covering an end of the second power supply portion **310**B far away from the display area, and the second planarization layer **16** being provided with a fourth via exposing the second power supply portion **310**B; [0124] a transparent conductive layer arranged on the second organic layer, wherein the transparent conductive layer at least includes an auxiliary power supply line **330** located in the circuit region **301** and the isolation dam region **302**, a plurality of fifth vias being provided in the auxiliary power supply line **330** located in the circuit region **301**; the auxiliary power supply line **330** in the isolation dam region **302** covering the second dam foundation **411** and partially covering the third dam foundation **422**; both the auxiliary power supply line **330** located on a side of the second dam foundation **411** adjacent to the display area **100** and the auxiliary power supply line **330** located on a side of the second dam foundation **402** away from the display area **100** being lapped on the second power supply portion **310**B; [0125] a third organic layer arranged on the transparent conductive layer, wherein the third organic layer at least includes an isolation layer **23** located in the circuit region **301**, and a fourth dam foundation **412** and a fifth dam foundation **423** located in the isolation dam region **302**, the isolation layer **23** being provided with a seventh via exposing the auxiliary power supply line **330**, the fourth dam foundation **412** being arranged on the auxiliary power supply line **330** covering the second dam foundation **411**, and a fifth dam foundation **423** being arranged on the third dam foundation **422**; [0126] a cathode **25** arranged in the circuit region **301**, wherein the cathode **25** is electrically connected to the auxiliary power supply line **330** through a seventh via; [0127] and a sixth dam foundation **413** and a seventh dam foundation **424** arranged in the isolation dam region **302**, wherein the sixth dam foundation **413** is located on the fourth dam foundation **412**, and the seventh dam foundation **424** is located on the fifth dam foundation

[0128] In an exemplary embodiment, the sixth dam foundation **413** and the seventh dam foundation **424** may be multiplexed as post spacers.

[0129] The second dam foundation **402**, the auxiliary power supply line **330** covering the second dam foundation, the fourth dam foundation **412**, and the sixth dam foundation **413** form a first isolation dam **410**.

[0130] In an exemplary embodiment, the first dam foundation **421**, the second power source portion **310**B covering the first dam foundation, the third dam foundation **422**, the fifth dam foundation **423**, and the seventh dam foundation **424** form a second isolation dam **420**.

[0131] FIG. **6** is a first schematic diagram of a structure of a display substrate according to an exemplary embodiment. As shown in FIG. **6**, a display substrate provided by an exemplary embodiment further includes an encapsulation layer **26**. The encapsulation layer **26** may include a first encapsulation layer **261**, a second encapsulation layer **262**, and a third encapsulation layer **263** which are stacked sequentially on the substrate. The encapsulation layer of the display area **100** and the circuit region **301** has a stacked structure of a first encapsulation layer/a second encapsulation layer/a third encapsulation layer, and the encapsulation layer of the isolation dam region **302** has a stacked structure of a first encapsulation layer/a third encapsulation layer.

[0132] Exemplary description is made below through a preparation process for the display substrate. A “patterning process” mentioned in the present disclosure includes coating with a photoresist, mask exposure, development, etching, photoresist stripping, and other treatments for a metal material, an inorganic material, or a transparent conductive material, and includes coating

with an organic material, mask exposure, development, and other treatments for an organic material. Deposition may be any one or more of sputtering, evaporation, and chemical vapor deposition. Coating may be any one or more of spray coating, spin coating, and ink-jet printing. Etching may be any one or more of dry etching and wet etching, which is not limited in present disclosure. A “thin film” refers to a layer of thin film made of a material on a substrate through a process such as deposition, coating, etc. If the “thin film” does not need a patterning process in an entire preparation process, the “thin film” may also be called a “layer”. If the “thin film” needs a patterning process in an entire preparation process, it is called a “thin film” before the patterning process, and called a “layer” after the patterning process. The “layer” after the patterning process includes at least one “pattern”. “A and B being arranged on a same layer” mentioned in the present disclosure means that A and B are formed simultaneously through a same patterning process, and a “thickness” of a film layer is a dimension of the film layer in a direction perpendicular to a display substrate. In an exemplary embodiment of the present disclosure, “an orthographic projection of B is within a range of an orthographic projection of A” refers to a boundary of the orthographic projection of B falling within a range of a boundary of the orthographic projection of A, or a boundary of the orthographic projection of A is overlapped with a boundary of the orthographic projection of B.

[0133] In an exemplary embodiment, as show in FIG. **7** to FIG. **22**, the display substrate includes a display area **100** and an edge area **300**, and the edge area **300** includes a circuit region **301** and an isolation dam region **302** which are sequentially arranged along a direction away from the display area **100**. The circuit region **301** includes a first circuit region **301**A, a second circuit region **301**A, and a third circuit region **301**C that are sequentially arranged along a direction away from the display area **100**. The display area **100** includes a pixel driving circuit **101**; the first circuit region **301**A includes a first driving circuit **201**; the second circuit region **301**A includes a second driving circuit **202**; and the isolation dam region **302** and the third circuit region **301**C include a third driving circuit **203**. A plurality of transistors and at least one capacitor are at least included in the pixel driving circuit **101**, the first driving circuit **201**, the second driving circuit **202** and the third driving circuit **203**, and only one transistor in the pixel driving circuit and one transistor and one capacitor in the first driving circuit to third driving circuit are shown as in FIG. **7** to FIG. **22**.

[0134] A preparation process of a display substrate provided by an exemplary embodiment may include:

[0135] (1) providing a substrate **10** and preparing patterns of a display circuit layer on the substrate **10**, wherein the patterns of the display circuit layer includes the patterns of a driving structure layer located in a display area **100** and a circuit structure layer located in a peripheral area **300**. The driving structure layer of the display area **100** includes a pixel driving circuit **101**, and the circuit structure layer of the peripheral area **300** includes a first driving circuit **201** located in a first circuit region **301**A, a second driving circuit **202** located in a second circuit region **301**B, and a third driving circuit **203** located in a third circuit region **301**C, and the circuit structure layer further includes a first power supply portion **310**A, a clock signal line ECLK of the third driving circuit **203** and the crack detection line **320** located in the isolation dam region **302**, as shown in FIG. **7** and FIG. **8**. FIG. **7** is a schematic diagram after the display circuit layer is formed, and FIG. **8** is a cross-sectional view along the A-A direction of FIG. **7**.

[0136] In an exemplary embodiment, the substrate **10** may include a first flexible material layer, a first inorganic material layer, a semiconductor layer, a second flexible material layer, and a second inorganic material layer which are stacked. Materials of the first flexible material layer and second flexible material layer may be polyimide (PI), polyethylene terephthalate (PET), or a polymer soft film subjected to surface treatment, etc. Materials of the first inorganic material layer and second inorganic material layer may be silicon nitride (SiNx), silicon oxide (SiOx), or the like, so as to improve water-oxygen resistance capability of the substrate. The first inorganic material layer and second inorganic material layer are also referred to as barrier layers. A material of the

semiconductor layer may be amorphous silicon (a-si). After this process, both the display area **100** and the peripheral area **300** include the substrate **10**.

[0137] In an exemplary embodiment, a preparation process of the display circuit layer may include: sequentially depositing a first insulation thin film and a semiconductor film on the substrate **10**, and patterning the semiconductor film by a patterning process to form a first insulation layer **11** covering the whole substrate **10** and form a semiconductor layer pattern arranged on the first insulation layer **11**, wherein the semiconductor layer pattern at least includes a first active layer located in the display area **100**, a second active layer located in a first circuit region **301**A, a third active layer located in a second circuit region **301**B and a fourth active layer located in a third circuit region **301**C.

[0138] Then, sequentially depositing a second insulation thin film and a first metal thin film, and patterning the first metal thin film by a patterning process to form a second insulation layer **12** covering the pattern of the semiconductor layer and covering the whole substrate, and form a pattern of a first gate metal layer arranged on the second insulation layer **12**, wherein the pattern of the first gate metal layer at least includes a first gate electrode located in the display area **100**, a second gate electrode and a first capacitive electrode located in the first circuit region **301**A, a third gate electrode and a second capacitive electrode located in the second circuit region **301**B, and a fourth gate electrode and a third capacitive electrode located in the third circuit region **301**C.

[0139] Subsequently, sequentially depositing a third insulation thin film and a second metal thin film, and patterning the second metal thin film by a patterning process to form a third insulation layer **13** covering the pattern of the first gate metal layer and covering the whole substrate, and form a pattern of a second gate metal layer arranged on the third insulation layer, wherein the pattern of the second gate metal layer at least includes a fourth capacitive electrode located in first circuit region **301**A, a fifth capacitive electrode located in second circuit region **301**B, a sixth capacitive electrode located in third circuit region **301**C.

[0140] In an exemplary embodiment, an orthographic projection of the first capacitive electrode on the substrate at least partially overlaps with an orthographic projection of the fourth capacitive electrode on the substrate, and the first capacitive electrode and the fourth capacitive electrode form a capacitor in the first driving circuit.

[0141] In an exemplary embodiment, an orthographic projection of the second capacitive electrode on the substrate at least partially overlaps with an orthographic projection of the fifth capacitive electrode on the substrate, and the second capacitive electrode and the fifth capacitive electrode form a capacitor in the second driving circuit.

[0142] In an exemplary embodiment, an orthographic projection of the third capacitive electrode on the substrate at least partially overlaps with an orthographic projection of the sixth capacitive electrode on the substrate, and the third capacitive electrode and the sixth capacitive electrode form a capacitor in the third driving circuit.

[0143] Then, a fourth insulation thin film is deposited, and the fourth insulation thin film is patterned by a patterning process to form a fourth insulation layer **14** covering a pattern of the second metal layer and covering the whole substrate. Among them, the second insulation layer **12**, the third insulation layer **13**, and the fourth insulation layer **14** are provided with vias exposing a first active layer in a display area **100**, vias exposing a second active layer in a first circuit region **301**A, vias exposing a third active layer in a second circuit region **301**B, and vias exposing a fourth active layer in a third circuit region **301**C.

[0144] Subsequently, a third metal thin film is deposited, and the third metal thin film is patterned by a patterning process to form a pattern of a first source-drain metal layer on the fourth insulation layer **14**, wherein the pattern of the first source-drain metal layer at least includes a first source electrode and a first drain electrode located in the display area **100**, a second source electrode and a second drain electrode located in the first circuit region **301**A, a third source electrode and a third drain electrode located in the second circuit region **301**B, a fourth source electrode and a fourth

drain electrode located in the third circuit region **301**C, a first power supply portion **310**A, a clock signal line ECLK of the third driving circuit, and a crack detection line **320** which are formed in the isolation dam region **302**.

[0145] In an exemplary embodiment, a first power supply portion **310**A, a clock signal line ECLK of the third driving circuit and a crack detection line **320** which are formed in the isolation dam region **302** are arranged on the fourth insulation layer **14**, wherein the crack detection line **320** is arranged at an end of the first power supply portion **310**A away from the display area **100**, and the clock signal line ECLK of the third driving circuit is located at an end of the first power supply portion **310**A close to the display area **100**.

[0146] In an exemplary embodiment, the first source electrode and the first drain electrode are connected to a first active layer through vias of a second insulation layer **12**, a third insulation layer **13** and a fourth insulation layer **14**, respectively, the second source electrode and the second drain electrode are connected to a second active layer through the second insulation layer **12**, the third insulation layer **13** and the fourth insulation layer **14**, respectively, the third source electrode and the third drain electrode are connected to the third active layer through the second insulation layer **12**, the third insulation layer **13** and the fourth insulation layer **14**, respectively, and the fourth source electrode and the fourth drain electrode are connected to a fourth active layer through the second insulation layer **12**, the third insulation layer **13** and the fourth insulation layer **14**, respectively.

[0147] So far, the pattern of the display circuit layer is prepared on the substrate.

[0148] In an exemplary embodiment, the first active layer may include active layers of all transistors in the pixel driving circuit, the first gate electrode may include gate electrodes of active layers of all transistors in the pixel driving circuit, the first source electrode may include source electrodes of all transistors in the pixel driving circuit, and the first drain electrode may include drain electrodes of all transistors in the pixel driving circuit.

[0149] In an exemplary embodiment, the second active layer may include active layers of all transistors in the first driving circuit, the second gate electrode may include gate electrodes of active layers of all transistors in the first driving circuit, the second source electrode may include source electrodes of all transistors in the first driving circuit, and the second drain electrode may include drain electrodes of all transistors in the first driving circuit.

[0150] In an exemplary embodiment, the third active layer may include active layers of all transistors in the second driving circuit, the third gate electrode may include gate electrodes of active layers of all transistors in the second driving circuit, the third source electrode may include source electrodes of all transistors in the second driving circuit, and the third drain electrode may include drain electrodes of all transistors in the second driving circuit.

[0151] In an exemplary embodiment, the fourth active layer may include active layers of all transistors in the third driving circuit, the fourth gate electrode may include gate electrodes of active layers of all transistors in the third driving circuit, the fourth source electrode may include source electrodes of all transistors in the third driving circuit, and the fourth drain electrode may include drain electrodes of all transistors in the third driving circuit.

[0152] In an exemplary embodiment, a distance L**1** between the first power supply portion **310**A and the third driving circuit **203** is greater than or equal to 3 microns and less than or equal to 5 microns, and as an example, the distance between the first power supply portion **310**A and the third driving circuit **203** may be 4 microns, which is not limited in this disclosure.

[0153] In an exemplary embodiment, a distance L**1** between the first power supply portion **310**A and the third driving circuit **203** may refer to a shortest distance between the first power supply portion and a clock signal line ECLK of the third driving circuit.

[0154] In an exemplary embodiment, a distance L**2** between the first power supply portion **310**A and the crack detection line **320** is greater than or equal to 3 microns and less than or equal to 5 microns, and as an example, the distance between the first power supply portion **310**A and the

crack detection line **320** may be 4 microns, which is not limited in this disclosure.
[0155] In an exemplary embodiment, a distance L**1** between the first power supply portion **310**A and the third driving circuit **203** may be equal to or may not be equal to a distance L**2** between the first power supply portion **310**A and the crack detection line **320**, which is not limited in this disclosure.
[0156] In an exemplary embodiment, a thickness of the first source-drain metal layer may be about 700 nm to 1000 nm. As an example, the thickness of the first source-drain metal layer may be about 860 nm.
[0157] (2) Coating a first organic film on a substrate on which the pattern described above is formed, and patterning a first planarization film by a patterning process to form a pattern of a first organic layer, wherein the pattern of the first organic layer includes a first planarization layer **15** located in the display area **100**, the circuit region **301**, and the isolation dam region **302**, and a first dam foundation **421** and a first protective layer **431** located in the isolation dam region **302**, as shown in FIG. **9** and FIG. **10**. FIG. **9** is a schematic diagram after the first organic layer is formed, and FIG. **10** is a cross-sectional view in the A-A direction of FIG. **9**.
[0158] In an exemplary embodiment, the first planarization layer **15** is provided with a first via V**1** exposing a first drain electrode.
[0159] In an exemplary embodiment, an orthographic projection of the first planarization layer **15** on the substrate covers an orthographic projection of a clock signal line ECLK of the third driving circuit on the substrate, and has no overlapping area with an orthographic projection of the first power supply portion **310**A on the substrate.
[0160] In an exemplary embodiment, in a plane parallel to the display substrate, a shape of the first via V**1** may be a triangle, a rectangle, a polygon, a circle, an ellipse, or the like.
[0161] In an exemplary embodiment, a shape of the first via V**1** may be a rectangular, a length of the rectangle may be about 10 μm to 40 μm, a width of the rectangle may be about 10 μm to 40 μm, and a distance between adjacent first vias V**5** may be about 10 μm to 40 μm.
[0162] In an exemplary embodiment, a surface of the first planarization layer located in the isolation dam region **302** is not planarization. Among them, the first planarization layer located in the isolation dam region **302** includes a first sub-planarization layer P**1** and a second sub-planarization layer P**2**, wherein the first sub-planarization layer P**1** is located on a side of the second sub-planarization layer P**2** away from the display area **100**, and has a thickness that is smaller than that of the second sub-planarization layer P**2**.
[0163] In an exemplary embodiment, an orthographic projection of the second sub-planarization layer P**2** on the substrate covers a third driving circuit **203**.
[0164] In an exemplary embodiment, a thickness of the first sub-planarization layer P**1** may be equal to a thickness of the first power supply portion **310**A, and a thickness of the second sub-planarization layer P**2** may be equal to a thickness of the first planarization layer located in the display area **100**.
[0165] In an exemplary embodiment, the first dam foundation **421** is located on a side of the first power supply portion **310**A away from the substrate, and an orthographic projection of the first power supply portion **310**A on the base overlaps at least partially with an orthographic projection of the first dam foundation **421** on the substrate.
[0166] In an exemplary embodiment, a length of the first dam foundation **421** along the first direction is smaller than a length of the first power supply portion **310**A along the first direction. That is, both a side of the first dam foundation **421** close to the display area and a side of the first dam foundation **421** away from the display area expose the first power supply portion **310**A.
[0167] In an exemplary embodiment, the first protective layer **431** is located on a side of the first dam foundation **421** away from the display area **100**.
[0168] In an exemplary embodiment, an orthographic projection of the first protective layer **431** on the substrate covers an orthographic projection of the crack detection line **320** on the substrate, and

at least partially overlaps with an orthographic projection of the first power supply portion **310**A on the substrate. That is, the first protective layer **431** covers the crack detection line **320** and an end of the first power supply portion **310**A away from the display area **100**.

[0169] In an exemplary embodiment, a length of the first dam foundation **421** along a first direction may be about 20 μm to 60 μm, and the first dam foundation **421** is configured to form a second isolation dam.

[0170] In an exemplary embodiment, in a plane perpendicular to the display substrate, a cross-sectional shape of the first dam foundation **421** may be a trapezoid or a rectangle. When the cross-sectional shape of the first dam foundation **421** is a trapezoid, a length of the surface on a side away from the substrate is smaller than a length of the surface on a side close to the substrate, and the length of the surface on the side away from the substrate may be about 20 μm to 40 μm.

[0171] (3) Depositing a fourth metal film on the substrate on which the pattern described above is formed, and patterning the fourth metal film by a patterning process to form a pattern of a second source-drain metal layer, wherein the pattern of the second source-drain metal layer at least includes a connection electrode **17** located in the display area **100** and a second power supply portion **310**B located in the circuit region **301** and the isolation dam region **302**, as shown in FIG. **11** and FIG. **12**. FIG. **11** is a schematic diagram after the second source-drain metal layer is formed, and FIG. **12** is a schematic diagram along an A-A direction of FIG. **11**.

[0172] In an exemplary embodiment, the connection electrode **17** is electrically connected to the first drain electrode through a first via V**1**.

[0173] In an exemplary embodiment, the second power supply portion **310**B is located at least in an isolation dam region **302** and a third circuit region **301**C.

[0174] In an exemplary embodiment, the second power supply portion **310**B may alternatively be located in a second circuit region **301**B.

[0175] In an exemplary embodiment, an orthographic projection of the second power supply portion **310**B on the substrate covers an orthographic projection of the first power supply portion **310**A and the third driving circuit **203** on the substrate and partially overlaps with an orthographic projection of the first protective layer **431** on the substrate.

[0176] In an exemplary embodiment, a distance between an end of the second power supply portion **310**B away from the display area and the display area may be greater than or equal to a distance between an end of the first power supply portion **310**A away from the display area and the display area. FIG. **12** illustrates an example in which a distance between an end of the second power supply portion **310**B away from the display area and the display area is equal to a distance between an end of the first power supply portion **310**A away from the display area and the display area.

[0177] In an exemplary embodiment, there is an overlapping area between an orthographic projection of the second power supply portion **310**B on the substrate and an orthographic projection of the second driving circuit on the substrate. A distance between an end of the second power supply portion **310**B close to the display area **100** and the display area **100** is greater than a distance between the clock signal line in the second driving circuit **202** and the display area **100**. That is, an orthographic projection of the second power supply portion **310**B on the substrate does not overlap with an orthographic projection of the clock signal line in the second driving circuit **202** on the substrate, and the orthographic projection of the second power supply portion **310**B on the substrate does not overlap with the orthographic projection of the clock signal line in the second driving circuit **202** on the substrate, which may ensure the display effect of the display substrate.

[0178] In an exemplary embodiment, the second power supply portion **310**B covers a surface of the first dam foundation **421**, and is arranged on the first power supply portion **310**A exposed on both sides of the first dam foundation **421** to achieve a connection between the second power supply portion **310**B and the first power supply portion **310**A.

[0179] In an exemplary embodiment, a distance between an end of the crack detection line **320**

close to the display area and the display area is greater than a distance between an end of the second power supply portion **310**B away from the display area and the display area. That is, an orthographic projection of the second power supply portion **310**B on the substrate does not overlap with an orthographic projection of the crack detection line **320** on the substrate.

[0180] In an exemplary embodiment, the second power supply portion **310**B is provided with a plurality of second vias V**2** exposing the first planarization layer **15**. The second via V**2** is arranged to release the gas in the first planarization layer **15** to form a deflation channel, and discharge a gas generated by a planarization film layer during a process, so as to avoid peeling of a film layer and improve the process quality.

[0181] In an exemplary embodiment, there are a plurality of second vias V**2**, and the plurality of second vias V**2** are arranged in a matrix to uniformly release the gas in the first planarization layer **15**.

[0182] In this way, the power supply portion **310**A of the first source-drain metal layer and the second power supply portion **310**B of the second source-drain metal layer form a double-layer power supply line in an edge area **300**. By lapping in the isolation dam region **302**, a double-layer power wiring with a parallel structure is achieved, which reduces a resistance of a power wiring in the edge area, minimizes voltage drop of voltage signals, and improves display brightness uniformity of the display area, and thereby improving display quality.

[0183] In an exemplary embodiment, a shape of the second via may be a triangle, a rectangle, a polygon, a circle, an ellipse, or the like. In an exemplary embodiment, a shape of the second via may be a rectangular, a length of the rectangle may be about 10 μm to 40 μm, a width of the rectangle may be about 10 μm to 40 μm, and a distance between adjacent second vias may be about 10 μm to 40 μm.

[0184] In an exemplary embodiment, the first dam foundation **421** includes a first surface, a first proximal side and a first distal side. The second power supply portion **310**B covering the surface of the first dam foundation **401** may refer that the second power supply portion **310**B completely covers the first surface, the first proximal side and the first distal side of the first dam foundation **401**. That is, the second power supply portion **310**B wraps the first surface, the first proximal side and the first distal side of the first dam foundation **401**.

[0185] In an exemplary embodiment, a thickness of the second source drain metal layer may be about 700 nm to 1000 nm. In some possible embodiments, the thickness of the second source drain metal layer may be about 860 nm.

[0186] (4) Coating a second organic film on a substrate on which the pattern described above is formed, and patterning a second organic film by a patterning process to form a pattern of a second organic layer, wherein the pattern of the second organic layer includes a first planarization layer **16** located in the display area **100** and the circuit region **301**, and a second dam foundation **411**, a third dam foundation **422** and a second protective layer **432** located in the isolation dam region **302**, as shown in FIG. **13** and FIG. **14**. FIG. **13** is a schematic diagram after the second organic layer is formed, and FIG. **14** is a cross-sectional view in the A-A direction of FIG. **13**.

[0187] In an exemplary embodiment, the second planarization layer **16** is provided with a third via V**3** exposing the connection electrode **17** and a fourth via V**4** exposing a surface of the second power supply portion **310**B.

[0188] In an exemplary embodiment, an orthographic projection of the fourth via V**4** on the substrate does not overlap with an orthographic projection of the second via V**2** on the substrate.

[0189] In an exemplary embodiment, a width W**1** of the fourth Via V**4** along a first direction is smaller than a distance W**2** between two adjacent second vias arranged in the first direction.

[0190] In an exemplary embodiment, in a plane parallel to the display substrate, shapes of the third via V**3** and the fourth via V**4** may be triangles, rectangles, polygons, circles, ellipses, or the like.

[0191] In an exemplary embodiment, shapes of the third via V**3** and the fourth via V**4** may be rectangles, a length of the rectangles may be about 10 μm to 40 μm, a width of the rectangle may

be about 10 μm to 40 μm, and distances between adjacent third vias and adjacent fourth vias may be about 10 μm to 40 μm.

[0192] In an exemplary embodiment, the second planarization layer **16** covers an end of the second power supply portion **310**B close to the display area **100**, and an orthographic projection of the second planarization layer **16** on the substrate covers an orthographic projection of the second via on the substrate.

[0193] In an exemplary embodiment, a distance between an end of the second planarization layer **16** away from the display area **100** and the display area **100** is smaller than a distance between an end of the third driving circuit **203** away from the display area **100** and the display area **100**, and the distance between the end of the second planarization layer **16** away from the display area **100** and the display area **100** is smaller than a distance between an end of the first planarization layer **15** away from the display area **100** and the display area **100**.

[0194] In an exemplary embodiment, the second dam foundation **411** is arranged on a second power supply portion **310**B on a side of the first dam foundation **421** adjacent to the display area **100**.

[0195] In an exemplary embodiment, an orthographic projection of the second dam foundation **411** on the substrate at least partially overlaps with an orthographic projection of a clock signal line of the third driving circuit on the substrate.

[0196] In an exemplary embodiment, a side of the second dam foundation **411** adjacent to the display area **100** and a side of the second dam foundation **411** away from the display area **100** both expose the second power supply portion **310**B.

[0197] In an exemplary embodiment, in a plane perpendicular to the display substrate, a cross-sectional shape of the second dam foundation **411** may be a trapezoid or a rectangle. When the cross-sectional shape of the second dam foundation **411** is a trapezoid, a length of the surface of the second dam foundation **411** on a side away from the substrate is smaller than a length of the surface of the second dam foundation **411** on a side close to the substrate, and the length of the surface on the side away from the substrate may be about 20 μm to 40 μm.

[0198] In an exemplary embodiment, a length of the second dam foundation **411** along a first direction may be about 20 μm to 60 μm, and the second dam foundation **411** is configured to form a first isolation dam.

[0199] In an exemplary embodiment, the third dam foundation **422** is arranged on a second power source portion **310**B covering the first dam foundation **421**, and an orthographic projection of the third dam foundation **422** on the substrate covers an orthographic projection of the first dam foundation **421** on the substrate.

[0200] In an exemplary embodiment, in a plane perpendicular to the display substrate, a cross-sectional shape of the third dam foundation **422** may be a trapezoid or a rectangle. When the cross-sectional shape of the third dam foundation **422** is a trapezoid, a length of the surface of the third dam foundation **422** on a side away from the substrate is smaller than a length of the surface of the third dam foundation **422** on a side close to the substrate, and the length of the surface on the side away from the substrate may be about 20 μm to 40 μm.

[0201] In an exemplary embodiment, an orthographic projection of the second protective layer **432** on the substrate covers an orthographic projection of the first protective layer **431** on the substrate. That is, the second protective layer **432** covers an end of the second power supply portion **310**B away from the display area **100**.

[0202] In an exemplary embodiment, a length of the third dam foundation **422** along a first direction may be about 20 μm to 60 μm, and the first dam foundation **421** and the third dam foundation **422** are configured to form a second isolation dam.

[0203] (5) Depositing a transparent conductive film on the substrate on which the pattern described above is formed, and patterning the transparent conductive film by a patterning process to form a pattern of a transparent conductive layer, wherein the pattern of the transparent conductive layer

includes an anode **21** located in the display area **100** and an auxiliary power supply line **330** located in the edge area **300**, as shown in FIG. **15** and FIG. **16**. FIG. **15** is a schematic diagram after the transparent conductive layer is formed, and FIG. **16** is a cross-sectional diagram along an A-A direction of FIG. **15**.

[0204] In an exemplary embodiment, the anode **21** is formed on a second planarization layer **16** in the display area **100**, and the anode **21** is connected with the connection electrode **17** through a third via.

[0205] In an exemplary embodiment, the auxiliary power supply line **330** is electrically connected to a second power supply portion **310**B, wherein a part of the auxiliary power supply line **330** is lapped on the second power supply portion **310**B, and the other part of the auxiliary power supply line **330** is connected to the second power supply portion **310**B through a fourth via V**4**.

[0206] In an exemplary embodiment, an orthographic projection of the auxiliary power supply line **330** on the substrate at least partially overlaps with an orthographic projection of the third dam foundation **422** on the substrate, and a distance between an end of the auxiliary power supply line **330** away from the display area **100** and the display area **100** is less than a distance between an end of the third dam foundation **422** away from the display area **100** and the display area **100**. That is, the auxiliary power supply line **330** partially covers the third dam foundation **422**.

[0207] In an exemplary embodiment, the third dam foundation **422** includes a third surface, a third proximal side and a third distal side. The auxiliary power supply line **330** partially covering the third dam foundation **422** may mean that the auxiliary power supply line **330** partially covers the third surface of the third dam foundation **422** and completely covers a second proximal side of the third dam foundation.

[0208] In an exemplary embodiment, an orthographic projection of the auxiliary power supply line **330** on the base covers an orthographic projection of the second dam foundation **411** on the substrate. That is, the auxiliary power supply line **330** covers the second dam foundation **411**.

[0209] In an exemplary embodiment, the second dam foundation **411** includes a second surface, a second proximal side and a second distal side. The auxiliary power supply line **330** covering the second dam foundation **411** may mean that the auxiliary power supply line **330** completely covers the second surface, the second proximal side and the second distal side of the second dam foundation **411**. That is, the auxiliary power supply line **330** wraps the second surface, the second proximal side and the second distal side of the second dam foundation **411**.

[0210] In an exemplary embodiment, an orthographic projection of the auxiliary power supply line **330** on the substrate at least partially overlaps with an orthographic projection of the second power supply portions **310**B exposed on both sides of the second dam foundation **411** on the substrate. That is, the auxiliary power supply line **330** covers and is electrically connected with the second power supply portions **310**B exposed on both sides of the second dam foundation **411**. Because the auxiliary power supply line **330** is connected to the second power supply portion **310**B, a connection between the auxiliary power supply line **330** and the power supply line **310** is achieved.

[0211] In an exemplary embodiment, an orthographic projection of the auxiliary power supply line **330** on the substrate at least partially overlaps with an orthographic projection of the first driving circuit **201**, the second driving circuit **202**, and the third driving circuit **203** on the substrate.

[0212] In an exemplary embodiment, the auxiliary power supply line **330** is provided with a fifth Via V**5** exposing the second planarization layer **16**, wherein the fifth via V**5** is located in a first circuit region **301**A, a second circuit region **301**B, and a third circuit region **301**C.

[0213] In an exemplary embodiment, an orthographic projection of the fifth via V**5** on the substrate located in a third circuit region **301**C at least partially overlaps with an orthographic projection of the second via V**2** on the substrate.

[0214] In an exemplary embodiment, the fifth via V**5** is arranged to release the gas in the second planarization layer **16** to form a deflation channel, and discharge a gas generated by a planarizing film layer during a process, so as to avoid peeling of a film layer and improve the process quality.

[0215] In an exemplary embodiment, there are a plurality of fifth vias V**5**, and the plurality of fifth vias V**5** are arranged in a matrix to uniformly release the gas in the second planarization layer **16**.
[0216] In an exemplary embodiment, in a plane parallel to the display substrate, a shape of the fifth via V**5** may be a triangle, a rectangle, a polygon, a circle, an ellipse, or the like.
[0217] In an exemplary embodiment, a shape of the fifth via V**5** may be a rectangular, a length of the rectangle may be about 10 μm to 40 μm, a width of the rectangle may be about 10 μm to 40 μm, and a distance between adjacent fifth vias V**5** may be about 10 μm to 40 μm.
[0218] (6) Coating a third organic film on the substrate on which the pattern described above is formed, and patterning the third organic film by a patterning process to form a pattern of a third organic layer, wherein the pattern of the third organic layer includes a pixel definition layer **22** located in the display area **100**, an isolation layer **23** located in the circuit region **301**, and a fourth dam foundation **412** and a fifth dam foundation **423** located in the isolation dam region **302**. FIG. **17** is a schematic diagram after the third organic layer is formed, and FIG. **18** is a schematic diagram along an A-A direction of FIG. **17**.
[0219] In an exemplary embodiment, the pixel definition layer **22** is provided with a sixth via V**6** exposing an anode **21**.
[0220] In an exemplary embodiment, in a plane parallel to the display substrate, a shape of the sixth via may be a triangle, a rectangle, a polygon, a circle, an ellipse, or the like.
[0221] In an exemplary embodiment, a shape of the six via may be a rectangular, a length of the rectangle may be about 10 μm to 40 μm, a width of the rectangle may be about 10 μm to 40 μm, and a distance between adjacent six vias may be about 10 μm to 40 μm.
[0222] In an exemplary embodiment, a distance between an end of the isolation layer **23** close to the display area **100** and the display area **100** is equal to a distance between an end of the pixel definition layer **22** away from the display area **100** and the display area **100**, and a distance between an end of the isolation layer **23** away from the display area **100** and the display area **100** is less than or equal to a distance between an end of the second planarization layer **16** away from the display area **100** and the display area **100**.
[0223] In an exemplary embodiment, a distance between an end of the isolation layer **23** away from the display area and the display area is less than or equal to a distance between an end of the second planarization layer away from the display area and the display area.
[0224] In an exemplary embodiment, an orthographic projection of the isolation layer **23** on the substrate covers an orthographic projection of the fifth via on the substrate.
[0225] In an exemplary embodiment, the isolation layer **23** is provided with a plurality of seventh via V**7** exposing an auxiliary power supply line **330**. The plurality of seventh vias V**7** may be arranged in an array or the plurality of seventh vias may be interconnected. FIG. **17** and FIG. **18** illustrate examples that the plurality of seventh vias may be interconnected.
[0226] In an exemplary embodiment, the plurality of seventh vias V**7** are located in a first circuit region **301**A, a second circuit region **301**B, and a third circuit region **301**C.
[0227] In an exemplary embodiment, an orthographic projection of the seventh via V**7** located in a third circuit region **301**C on the substrate at least partially overlaps with an orthographic projection of the fourth via V**4** on the substrate.
[0228] In an exemplary embodiment, the fourth dam foundation **412** is arranged on an auxiliary power supply line **330** covering the second dam foundation **411**, and an orthographic projection of the fourth dam foundation **412** on the substrate covers an orthographic projection of the second dam foundation **411** on the substrate.
[0229] In an exemplary embodiment, a length of the fourth dam foundation **412** along a first direction may be from about 20 mum to 60 mum.
[0230] In an exemplary embodiment, in a plane perpendicular to the display substrate, a cross-sectional shape of the fourth dam foundation **412** may be a trapezoid or a rectangle. When the cross-sectional shape of the fourth dam foundation **412** is a trapezoid, a length of the surface of the

fourth dam foundation **412** on a side away from the substrate is smaller than a length of the surface of the fourth dam foundation **412** on a side close to the substrate, and the length of the surface on the side away from the substrate may be about 20 μm to 40 μm.

[0231] In an exemplary embodiment, the fifth dam foundation **423** is arranged on a third dam foundation **422**, and an orthographic projection of the fifth dam foundation **423** on the substrate overlaps with an orthographic projection of the third dam foundation **422** on the substrate.

[0232] In an exemplary embodiment, the fifth dam foundation **423** may be about 20 μm to 60 μm along a first direction.

[0233] In an exemplary embodiment, in a plane perpendicular to the display substrate, a cross-sectional shape of the fifth dam foundation **423** may be a trapezoid or a rectangle. When the cross-sectional shape of the fifth dam foundation **423** is a trapezoid, a length of the surface on a side away from the substrate is smaller than a length of the surface on a side close to the substrate, and the length of the surface on the side away from the substrate may be about 20 μm to 40 μm.

[0234] In an exemplary embodiment, an auxiliary power supply line **330** is exposed between the fourth dam foundation **412** and the fifth dam foundation **423**, and the auxiliary power supply line **330** is exposed on a side of the fourth dam foundation **412** adjacent to the display area **100**.

[0235] (7) Forming an organic light-emitting layer **24** on the substrate on which the pattern described above is formed, as shown in FIG. **19** and FIG. **20**. FIG. **19** is a schematic diagram after the organic light-emitting layer is formed, and FIG. **20** is a cross-sectional view along the A-A direction of FIG. **19**.

[0236] In an exemplary embodiment, the organic light emitting layer **24** is formed in a six via V**6** of the pixel definition layer **22** in the display area **100** to achieve a connection between the organic light emitting layer **24** and the anode **21**. Because the anode **21** is connected to the connection electrode **17**, and the connection electrode **17** is connected to the first drain electrode, a connection between the organic light-emitting layer **24** and the first drain electrode is thereby achieved.

[0237] In an exemplary embodiment, the organic emitting layer **24** may include a Hole Injection Layer (HIL for short), a Hole Transport Layer (HTL for short), an Electron Block Layer (EBL for short), an Emitting Layer (EML for short), a Hole Block Layer (HBL for short), an Electron Transport Layer (ETL for short), and an Electron Injection Layer (EIL for short) that are stacked. In an exemplary implementation mode, hole injection layers of all sub-pixels may be a common layer connected together, electron injection layers of all the sub-pixels may be a common layer connected together, hole transport layers of all the sub-pixels may be a common layer connected together, electron transport layers of all the sub-pixels may be a common layer connected together, hole block layers of all the sub-pixels may be a common layer connected together, emitting layers of adjacent sub-pixels may be overlapped slightly or may be isolated from each other, and electron block layers of adjacent sub-pixels may be overlapped slightly or may be isolated from each other.

[0238] (8) Forming a cathode **25** located in the display area **100** and the circuit region **301**, and a sixth dam foundation **413** and a seventh dam foundation **424** located in the isolation dam region **302** on the substrate on which the pattern described above is formed, as shown in FIG. **21** and FIG. **22**. FIG. **21** is a schematic diagram after the cathode is formed, and FIG. **22** is a cross-sectional diagram in an A-A direction of FIG. **21**.

[0239] In an exemplary embodiment, a distance between an end of the cathode **25** away from the display area **100** and the display area **100** is less than a distance between a side of the isolation layer **23** away from the display area **100** and the display area **100**.

[0240] In an exemplary embodiment, a part of the cathode **25** is formed on an organic light emitting layer **24** in the display area **100**, the cathode **25** is connected to the organic light emitting layer **24**, and the other part of the cathode **25** is connected to the auxiliary power supply line **330** through a seventh via.

[0241] In an exemplary embodiment, because the cathode **25** is connected to an auxiliary power supply line **330** and the auxiliary power supply line **330** is electrically connected to a second power

supply portion **310**B of the power supply line **310**, a connection between the cathode **25** and the power supply line **310** is thereby achieved.

[0242] In an exemplary embodiment, the cathode may be made of any one or more of magnesium (Mg), silver (Ag), aluminum (Al), copper (Cu), and lithium (Li), or an alloy made of any one or more of the above metals.

[0243] In an exemplary embodiment, the sixth dam foundation **413** is arranged on the fourth dam foundation **412**, and an orthographic projection of the fourth dam foundation on the substrate overlaps with an orthographic projection of the sixth dam foundation **413** on the substrate.

[0244] In an exemplary embodiment, the sixth dam foundation **413** may be about 20 μm to 60 μm along a first direction.

[0245] In an exemplary embodiment, in a plane perpendicular to the display substrate, a cross-sectional shape of the sixth dam foundation **413** may be a trapezoid or a rectangle. When the cross-sectional shape of the sixth dam foundation **413** is a trapezoid, a length of the surface of the sixth dam foundation **413** on a side away from the substrate is smaller than a length of the surface of the sixth dam foundation **413** on a side close to the substrate, and the length of the surface of the sixth dam foundation **413** on the side away from the substrate may be about 20 μm to 40 μm.

[0246] In an exemplary embodiment, the second dam foundation **402**, the auxiliary power supply line **330** covering the second dam foundation, the fourth dam foundation **411**, and the sixth dam foundation **413** form a first isolation dam **410**.

[0247] In an exemplary embodiment, the seventh dam foundation **424** is arranged on the fifth dam foundation **423**, and an orthographic projection of the fifth dam foundation **423** on the substrate covers an orthographic projection of the seventh dam foundation **424** on the substrate.

[0248] In an exemplary embodiment, the seventh dam foundation **424** may be about 20 μm to 60 μm along a first direction.

[0249] In an exemplary embodiment, in a plane perpendicular to the display substrate, a cross-sectional shape of the seventh dam foundation **424** may be a trapezoid or a rectangle. When the cross-sectional shape of the seventh dam foundation **424** is a trapezoid, a length of the surface of the seventh dam foundation **424** on a side away from the substrate is smaller than a length of the surface of the seventh dam foundation **424** on a side close to the substrate, and the length of the surface on the side away from the substrate may be about 20 μm to 40 μm.

[0250] In an exemplary embodiment, the first dam foundation **421**, the second power source portion **310**B covering the first dam foundation, the third dam foundation **422**, the fifth dam foundation **423**, and the seventh dam foundation **424** form a second isolation dam **420**.

[0251] In an exemplary embodiment, a distance between the first isolation dam **410** and the display area **100** is smaller than that between the second isolation dam **420** and the display area **100**.

[0252] In an exemplary embodiment, a length of an orthographic projection of the first isolation dam **410** and the second isolation dam **420** on the substrate **10** may be about 20 μm to about 60 μm, and a distance between the first isolation dam **410** and the second isolation dam **420** may be about 20 μm to about 60 μm.

[0253] In an exemplary embodiment, in a plane perpendicular to the display substrate, cross-sectional shapes of the first isolation dam **410** and the second isolation dam **420** may be trapezoids.

[0254] In an exemplary embodiment, the sixth dam foundation **413** and the seventh dam foundation **424** are of an integrally formed structures. Cathode **25** may be formed before or after the formation of a sixth dam foundation **413** and a seventh dam foundation **424**.

[0255] In an exemplary embodiment, an orthographic projection of the first isolation dam **410** on the substrate at least partially overlaps with an orthographic projection of a clock signal line of the third driving circuit on the substrate.

[0256] (9) Forming an encapsulation layer **26** on a basis of forming the patterns described above, wherein the encapsulation layer **26** is formed in the display area **100**, the circuit region **301**, and the isolation dam region **302**, as shown in FIG. **5**.

[0257] In an exemplary embodiment, the encapsulation layer **26** of the display area **100** and the circuit region **301** has a stacked structure of a first encapsulation layer **261**, a second encapsulation layer **262** and a third encapsulation layer **263**, and the encapsulation layer **26** of the isolation dam region **302** has a stacked structure of a first encapsulation layer **261**, and a third encapsulation layer **263**.

[0258] In an exemplary embodiment, the first encapsulation layer may be made of an inorganic material, covering a cathode **25** in the display area **100**, covering a post spacer layer **23** in the circuit region **301**, and wrapping a first isolation dam **410** and a second isolation dam **420** in the isolation dam region **302**. The second encapsulation layer may be made of an organic material, and is arranged in the display area **100** and the circuit region **301**. The third encapsulation layer may be made of an inorganic material, covering the second encapsulation layer of the display area **100** and the circuit region **301**, and covering the first encapsulation layer in the isolation dam region **302**. That is, the encapsulation layer **26** of the display area **100** and the circuit region **301** has a laminated structure of an inorganic material/an organic material/an inorganic material, an organic material layer is arranged between two inorganic material layers, and the encapsulation layer **26** of the isolation dam region **302** has a laminated structure of inorganic material/inorganic material.

[0259] In an exemplary embodiment, the first insulation layer, the second insulation layer, the third insulation layer and the fourth insulation layer may be made of any one or more of silicon oxide (SiOx), silicon nitride (SiNx) and silicon oxynitride (SiON), and may be a single-layer, a multi-layer or a composite layer. The first insulation layer is called a buffer layer, which is used to improve the water and oxygen resistance of the substrate. The second insulation layer and the third insulation layer are called gate insulating (GI) layers. The fourth insulation layer is called an interlayer insulating (ILD) layer.

[0260] In an exemplary embodiment, the first metal thin film, the second metal thin film, the third metal thin film, and the fourth metal thin film may be made of metal materials, such as any one or more of silver (Ag), copper (Cu), aluminum (Al), titanium (Ti), and molybdenum (Mo), or alloy materials of the above metals, such as AlNd alloy or MoNb alloy, and may be a single-layer structure or a multi-layer composite structure, such as Ti/Al/Ti. The transparent conductive thin film may include Indium Tin Oxide (ITO) or Indium Zinc Oxide (IZO). The pixel definition layer may be made of polyimide, acrylic, polyethylene terephthalate, or the like. An active layer thin film may be made of an amorphous Indium Gallium Zinc Oxide (a-IGZO), Zinc OxyNitride (ZnON), Indium Zinc Tin Oxide (IZTO), amorphous Silicon (a-Si), polycrystalline Silicon (p-Si), hexathiophene, polythiophene, and other materials, that is, the present disclosure is applicable to transistors manufactured based on an oxide technology, a silicon technology, and an organic matter technology.

[0261] According to the exemplary embodiment of the present disclosure, a first power supply portion **310**A of the power supply line **310** is formed by a first source-drain metal layer, and a second power supply portion **310**B of the power supply line **310** is formed by a second source-drain metal layer, so that a double-layer power supply line **310** is formed in an edge area **300**, achieving a double-layer power supply wiring in a parallel structure, reducing a resistance of power supply wiring in the edge area **300**, minimizing voltage drop of voltage signals to the maximum extent, and improving display brightness uniformity in the display area **100** and display quality.

[0262] In an exemplary embodiment, a distance between the first power supply portion **310**A and the third driving circuit **203** is greater than or equal to 1 micron and less than or equal to 6 microns, and as an example, the distance between the first power supply portion **310**A and the third driving circuit **203** may be 4 microns, which is not limited in this disclosure.

[0263] In an exemplary embodiment, a distance between the first power supply portion **310**A and the crack detection line **320** is greater than or equal to 1 micron and less than or equal to 6 microns, and as an example, the distance between the first power supply portion **310**A and the crack detection line **320** may be 4 microns, which is not limited in this disclosure.

[0264] In the present disclosure, a distance between the first power supply portion **310**A and the third driving circuit **203** and a distance between the first power supply portion **310**A and the crack detection line **320** are arranged such that a width of the first power supply portion **310**A is sufficiently large in a situation that the requirements of the display substrate exposure, etching and other processes and signal interference can be satisfied, thereby reducing the voltage drop of the power supply line, being able to improve the display uniformity of the display substrate, and reducing the power consumption of the display substrate.
[0265] In the present disclosure, a distance between the first power supply portion **310**A and the third driving circuit **203** may be equal to or may not be equal to a distance between the first power supply portion **310**A and the crack detection line **320**, which is not limited in this disclosure.
[0266] In the present disclosure, an orthographic projection of the second power supply portion **310**B on the substrate **10** covers an orthographic projection of the first power supply portion **310**A and the third driving circuit **203** on the substrate **10**. In the present disclosure, the second power supply portion **310**B is arranged in such a manner that a length of the second power supply portion **310**B along a first direction is sufficiently large, thereby reducing the voltage drop of the power supply line, being able to improve the display uniformity of the display substrate, and reducing the power consumption of the display substrate.
[0267] In the present disclosure, a distance between the end of the second power supply portion **310**B close to the display area **100** and the display area **100** is greater than a distance between a clock signal line CLK in the second driving circuit **202** and the display area **100**, thereby reducing a load of the clock signal line CLK in the second driving circuit **202** and ensuring a normal display of a display unit in the display area **100**.
[0268] In the present disclosure, the first protective layer **431** wraps an end of the first power supply portion **310**A away from the display area **100**, and the second protective layer **432** wraps an end of the second power supply portion **310**B away from the display area **100**, thereby preventing corrosion and dark spots.
[0269] In the present disclosure, the second planarization layer **16** covers a second power supply portion located at the edge of the second via, thereby preventing corrosion and dark spots.
[0270] In the present disclosure, due to manners of arrangements of the second power supply portion **310**B and the second planarization layer, a distance between an end of the first isolation dam **410** close to the display area **100** and an end of the second power supply portion **310**B close to the display area may be large, and the packaging reliability of the display substrate can be improved.
[0271] In the present disclosure, the auxiliary power supply line **330** covers the first driving circuit **201**, the second driving circuit **202**, and the third driving circuit **203**, so that the voltage drop of the power supply line can be reduced, and the interference of external environment or signals on the first driving circuit **201**, the second driving circuit **202**, and the third driving circuit **203** can also be shielded.
[0272] According to the exemplary embodiment of the present disclosure, a second via and a fifth via are respectively arranged on the second power supply portion **310**B and the auxiliary power supply line **330** to form a deflation channel, so that gases generated by a plat layer may be effectively discharged in the process, thereby avoiding peeling of a film layer and improving process quality. The preparation process of the display substrate in the exemplary embodiment of the present disclosure has good process compatibility, simple process achievement, easy implementation, a high production efficiency, a low production cost, and a high yield.
[0273] The description of the structure and preparation process of the display substrate according to the present disclosure is merely illustrative. In an exemplary embodiment, a corresponding structure may be changed and a patterning process may be increased or decreased according to actual needs, which is not limited in the present disclosure.
[0274] The embodiment of the disclosure further provides a preparation method of the display

substrate, which is arranged to prepare a display substrate, wherein the display substrate comprises a display area and an edge area and the preparation method for the display substrate provided by the embodiment of the disclosure may include the following steps:

[0275] In step S**1**, providing a substrate.

[0276] In step S**2**, sequentially forming a first power supply portion and a second power supply portion on the substrate to form a power supply line located in an edge area.

[0277] In an exemplary embodiment, an orthographic projection of the second power supply portion on the substrate is at least partially overlapped with an orthographic projection of the first power supply portion on the substrate, and a distance between an end of the second power supply portion far away from the display area and the display area is greater than or equal to a distance between an end of the first power supply portion far away from the display area and the display area.

[0278] The display substrate is the display substrate according to any of the aforementioned embodiments, and has similar implementation principles and implementation effects, which will not be repeated here.

[0279] In an exemplary embodiment, the step S**2** may include the following steps:

[0280] forming a pixel driving circuit in a display area on the substrate, a first driving circuit and a second driving circuit located in the circuit region, a third driving circuit located in the third circuit region, and a first power supply portion and a crack detection line located in the isolation dam region; forming a first planarization layer located in the display area and the circuit region and a first dam foundation and a first protective layer located in the isolation dam region on the substrate on which the first power supply portion is formed; forming a connection electrode located in a display area and a second power supply portion located in a circuit region and an isolation dam region on the substrate on which the first planarization layer is formed; forming a second planarization layer located in the display area and the circuit region, a second dam foundation, a third dam foundation and a second protective layer located in the isolation dam region on the substrate on which the second power supply portion is formed; forming an anode located in a display area and an auxiliary power supply line located in an edge area on the substrate on which the second planarization layer is formed; forming a pixel definition layer located in a display area, an isolation layer located in a circuit region, and a fourth dam foundation and a fifth dam foundation located in an isolation dam region on the substrate on which the auxiliary power supply line is formed; and forming an organic light emitting layer located in the display area, a cathode located in the display area and the circuit region, and a sixth dam foundation and a seventh dam foundation located in the isolation dam region on the substrate on which the pixel definition layer is formed.

[0281] An embodiment of the present disclosure further provides a display apparatus, including a display substrate.

[0282] The display substrate is the display substrate according to any of the aforementioned embodiments, and has similar implementation principles and implementation effects, which will not be repeated here.

[0283] In an exemplary embodiment, the display apparatus may be any product or component with a display function, such as a mobile phone, a tablet computer, a television, a display, a notebook computer, a digital photo frame, or a navigator.

[0284] Although the embodiments disclosed in the present disclosure are as above, the described contents are only embodiments used for convenience of understanding the present disclosure and are not intended to limit the present disclosure. Any skilled in the art to which the present disclosure pertains, without departing from the spirit and scope disclosed in the present disclosure, may make any modifications and changes in a form and details of implementation. However, the scope of patent protection of the present application should still be subject to the scope defined by the appended claims.

Claims

1. A display substrate, comprising a display area and an edge area located on a side of the display area, the display substrate comprising a substrate and a power supply line arranged on the substrate and located in the edge area, wherein: the power supply line comprises a first power supply portion and a second power supply portion connected with each other, and the second power supply portion is located on a side of the first power supply portion away from the substrate; the display area comprises a plurality of display units, wherein at least one display unit of the plurality of display units comprises a pixel driving circuit and a light emitting device, wherein the pixel driving circuit is electrically connected with an anode of the light emitting device, and the power supply line is electrically connected with a cathode of the light emitting device; and an orthographic projection of the second power supply portion on the substrate is at least partially overlapped with an orthographic projection of the first power supply portion on the substrate, and a distance between an end of the second power supply portion away from the display area and the display area is greater than or equal to a distance between an end of the first power supply portion away from the display area and the display area.

2. The display substrate according to claim 1, wherein: the edge area comprises a circuit region and an isolation dam region sequentially arranged in a direction away from the display area, the circuit region comprising a first circuit region, a second circuit region and a third circuit region sequentially arranged in a direction away from the display area; the pixel driving circuit comprises a writing transistor, a compensation transistor, a light emitting transistor, a first scan signal line, a second scan signal line and a light emitting signal line; the first scan signal line is electrically connected to a control electrode of the writing transistor, the second scan signal line is electrically connected to a control electrode of the compensation transistor, and the light emitting signal line is electrically connected to a control electrode of the light emitting transistor; and the writing transistor and the compensation transistor have different transistor types; the display substrate further comprises a first driving circuit located in the first circuit region, a second driving circuit located in the second circuit region, and a third driving circuit located in the third circuit region and the isolation dam region; the first driving circuit is electrically connected with the first scan signal line, the second driving circuit is electrically connected with the second scan signal line, and the third driving circuit is electrically connected with the light emitting signal line; the first power supply portion is located in the isolation dam region, and the second power supply portion is located in the isolation dam region and the circuit region; and an orthographic projection of the second power supply portion on the substrate is at least partially overlapped with an orthographic projection of the third driving circuit on the substrate, and there is no overlapping area between the orthographic projection of the second power supply portion on the substrate and an orthographic projection of the second driving circuit on the substrate.

3. The display substrate according to claim 2, further comprising a crack detection line located in the isolation dam region, wherein the crack detection line is arranged in a same layer as the first power supply portion and is located on a side of the first power supply portion away from the display area; and a distance between the first power supply portion and the crack detection line is greater than or equal to 1 micron and less than or equal to 6 microns.

4. The display substrate according to claim 2, wherein a distance between the first power supply portion and the third driving circuit is greater than or equal to 1 micron and less than or equal to 6 microns.

5. The display substrate of claim 3, further comprising a first planarization layer located in the display area, the circuit region and the isolation dam region, and a first protective layer located in the isolation dam region, wherein the first planarization layer is located between the first power supply portion and the second power supply portion and is arranged in a same layer as the first

protective layer; and an orthographic projection of the first protective layer on the substrate covers an orthographic projection of the crack detection line on the substrate and is at least partially overlapped with the orthographic projection of the first power supply portion on the substrate.

6. The display substrate according to claim 5, wherein the third driving circuit comprises a clock signal line located in the isolation dam region; the clock signal line is arranged in a same layer as the first power supply portion and is located on a side of the first power supply portion close to the display area; and an orthographic projection of the first planarization layer on the substrate covers an orthographic projection of the clock signal line on the substrate, and there is no overlapping area between the orthographic projection of the first planarization layer on the substrate and the orthographic projection of the first power supply portion on the substrate.

7. The display substrate according to claim 5, wherein the second power supply portion is provided with a plurality of second via holes exposing the first planarization layer, the plurality of second vias being arranged in a matrix; and an orthographic projection of the plurality of second via holes on the substrate is at least partially overlapped with the orthographic projection of the third driving circuit on the substrate.

8. The display substrate of claim 7, further comprising a second planarization layer located in the display area and the circuit region and a second protective layer located in the isolation dam region, wherein: the second planarization layer is located on a side of the second power supply portion away from the substrate and is arranged in a same layer as the second protective layer; and an orthographic projection of the second protective layer on the substrate covers the orthographic projection of the first protective layer on the substrate, and an orthographic projection of the second planarization layer on the substrate covers the orthographic projection of the second via holes on the substrate.

9. The display substrate according to claim 8, further comprising an auxiliary power supply line located in the edge area, wherein: the anode is located on a side of the second planarization layer away from the substrate, and is arranged in a same layer as the auxiliary power supply line; the auxiliary power supply line is electrically connected with the second power supply portion; and an orthographic projection of the auxiliary power supply line on the substrate is at least partially overlapped with orthographic projections of the first driving circuit, the second driving circuit, and the third driving circuit on the substrate.

10. The display substrate according to claim 9, wherein the auxiliary power supply line is provided with a plurality of fifth via holes exposing the second planarization layer, the plurality of fifth via holes being arranged in a matrix; the plurality of fifth via holes are located in the first circuit region, the second circuit region and the third circuit region; and an orthographic projection of the fifth via holes located in the third circuit region on the substrate is at least partially overlapped with an orthographic projection of the second via holes on the substrate.

11. The display substrate according to claim 10, further comprising a pixel definition layer located in the display area and an isolation layer located in the circuit region, wherein: the pixel definition layer is located on a side of the anode away from the substrate, and is arranged in a same layer as the isolation layer; and a distance between an end of the isolation layer away from the display area and the display area is less than or equal to a distance between an end of the second planarization layer away from the display area and the display area, and an orthographic projection of the isolation layer on the substrate covers the orthographic projection of the fifth via holes on the substrate.

12. The display substrate according to claim 11, further comprising an organic light emitting layer sequentially stacked on the substrate and located in the display area, and the cathode located in the display area and the circuit region, wherein the cathode is electrically connected with the auxiliary power supply line.

13. The display substrate of claim 12, wherein the isolation dam region further comprises a first isolation dam and a second isolation dam; and the second isolation dam is located on a side of the

first isolation dam away from the display area, and is located on a side of the second protective layer close to the display area.

14. The display substrate of claim 13, further comprising a first dam foundation, a third dam foundation, a fifth dam foundation, and a seventh dam foundation located in the isolation dam region, wherein: the first dam foundation is arranged in a same layer as the first planarization layer, the third dam foundation is arranged in a same layer as the second planarization layer, the fifth dam foundation is arranged in a same layer as the pixel definition layer, and the seventh dam foundation is located on a side of the pixel definition layer away from the substrate; the second power supply portion covers the first dam foundation, the third dam foundation is arranged on the second power supply portion covering the first dam foundation and an orthographic projection of the third dam foundation on the substrate covers an orthographic projection of the first dam foundation on the substrate, the fifth dam foundation is arranged on the third dam foundation and an orthographic projection of the fifth dam foundation on the substrate covers the orthographic projection of the third dam foundation on the substrate, and the seventh dam foundation is arranged on the fifth dam foundation and the orthographic projection of the fifth dam foundation on the substrate covers an orthographic projection of the seventh dam foundation on the substrate; the auxiliary power supply line partially covers the third dam foundation; and the first dam foundation, the second power supply portion covering the first dam foundation, the third dam foundation, the fifth dam foundation, and the seventh dam foundation form the second isolation dam.

15. The display substrate of claim 14, further comprising a second dam foundation, a fourth dam foundation, and a sixth dam foundation located in the isolation dam region, wherein: the second dam foundation is arranged in a same layer as the second planarization layer, the fourth dam foundation is arranged in a same layer as the pixel definition layer, and the sixth dam foundation is arranged in a same layer as the seventh dam foundation; the second dam foundation is arranged on the second power supply portion, the fourth dam foundation is arranged on the auxiliary power supply line covering the second dam foundation and an orthographic projection of the fourth dam foundation on the substrate covers an orthographic projection of the second dam foundation on the substrate, and the sixth dam foundation is arranged on the fourth dam foundation and the orthographic projection of the fourth dam foundation on the substrate covers an orthographic projection of the sixth dam foundation on the substrate; and the second dam foundation, the auxiliary power supply line covering the second dam foundation, the fourth dam foundation and the sixth dam foundation form the first isolation dam.

16. The display substrate according to claim 13- or **15**, wherein an orthographic projection of the first isolation dam on the substrate is at least partially overlapped with a clock signal line on the substrate.

17. A display apparatus, comprising the display substrate according to claim 1.

18. A method for preparing a display substrate, arranged to prepare the display substrate according to claim 1, the display substrate comprising the display area and the edge area located on the side of the display area, the method comprising: providing the substrate; and sequentially forming the first power supply portion and the second power supply portion on the substrate to form the power supply line located in the edge area, wherein the orthographic projection of the second power supply portion on the substrate is at least partially overlapped with the orthographic projection of the first power supply portion on the substrate, and the distance between the end of the second power supply portion away from the display area and the display area is greater than or equal to the distance between the end of the first power supply portion away from the display area and the display area.

19. The method according to claim 18, wherein sequentially forming the first power supply portion and the second power supply portion on the substrate comprises: forming a pixel driving circuit in the display area on the substrate, a first driving circuit and a second driving circuit located in the circuit region, a third driving circuit located in the third circuit region, and the first power supply

portion and a crack detection line located in the isolation dam region; forming a first planarization layer located in the display area and the circuit region, and a first dam foundation and a first protective layer located in the isolation dam region on the substrate on which the first power supply portion is formed; forming a connection electrode located in the display area and the second power supply portion located in the circuit region and the isolation dam region on the substrate on which the first planarization layer is formed; forming a second planarization layer located in the display area and the circuit region, a second dam foundation, a third dam foundation and a second protective layer located in the isolation dam region on the substrate on which the second power supply portion is formed; forming the anode located in the display area and an auxiliary power supply line located in the edge area on the substrate on which the second planarization layer is formed; forming a pixel definition layer located in the display area, an isolation layer located in the circuit region, and a fourth dam foundation and a fifth dam foundation located in the isolation dam region on the substrate on which the auxiliary power supply line is formed; and forming an organic light emitting layer located in the display area, the cathode located in the display area and the circuit region, and a sixth dam foundation and a seventh dam foundation located in the isolation dam region on the substrate on which the pixel definition layer is formed.

20. The display substrate according to claim 15, wherein an orthographic projection of the first isolation dam on the substrate is at least partially overlapped with a clock signal line on the substrate.