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SEMICONDUCTOR DIE AND METHOD FOR FORMING THE SAME

Abstract

The semiconductor die includes a substrate and first and second semiconductor devices over the substrate. The first memory array includes first semiconductor devices stacked in a vertical direction, a first source line, and a first bit line. The first source line electrically connects to the first semiconductor devices and extends downwardly from a topmost one of the first semiconductor devices to a lowermost one of the first semiconductor devices. The first bit line electrically connects to the first semiconductor devices and extends downwardly from the topmost one of the first semiconductor devices to the lowermost one of the first semiconductor devices. The second memory array includes second semiconductor devices stacked in the vertical direction, a second source line, and a second bit line. The second source line electrically connects to the second semiconductor devices and is disposed below the plurality of second semiconductor devices.

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Background/Summary

PRIORITY CLAIM AND CROSS-REFERENCE [0001] The present application is a Divisional application of the U.S. application Ser. No. 17/580,500, filed Jan. 20, 2022, which is herein incorporated by reference in its entirety.

BACKGROUND
[0002] The present disclosure generally relates to semiconductor devices, and particularly to methods of making a 3-dimensional (3D) memory device.
[0003] The semiconductor industry has experienced rapid growth due to continuous improvements in the integration density of a variety of electronic components (e.g., transistors, diodes, resistors, capacitors, etc.). For the most part, this improvement in integration density has come from repeated reductions in minimum feature size, which allows more components to be integrated into a given area.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0004] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.
[0005] FIG. **1**A is a perspective view of a semiconductor die having a first array of a first set of computing three-dimensional memory devices disposed on a first side of the semiconductor die, and a second array of a second set of storage three-dimensional memory devices disposed on a second side of the semiconductor die, in accordance with some embodiments of the present disclosure.
[0006] FIG. **1**B illustrates a perspective view of a semiconductor die having a first set of computing three-dimensional memory devices, and a second set of storage three-dimensional memory devices, the first set of the computing three-dimensional memory devices being disposed adjacent to the second set of the storage three-dimensional memory devices in at least a first direction, a second direction perpendicular to the first direction, or the first direction and the second direction, in accordance with some embodiments of the present disclosure.
[0007] FIG. **2**A illustrates a perspective view of a portion of the semiconductor die of FIG. **1**A including the first set of the computing three-dimensional memory devices indicated by the arrow A in FIG. **1**A, in accordance with some embodiments of the present disclosure.
[0008] FIG. **2**B illustrates a cross-section view of the computing three-dimensional memory devices, taken along the line X-X in FIG. **2**A, in accordance with some embodiments of the present disclosure.
[0009] FIG. **3**A illustrates a perspective view of a portion of the semiconductor die of FIG. **1**A including the second set of the storage three-dimensional memory devices indicated by the arrow B in FIG. **1**A, in accordance with some embodiments of the present disclosure.
[0010] FIG. **3**B illustrates a cross-section view of the storage three-dimensional memory devices,

taken along the line Y-Y in FIG. **3**A, in accordance with to some embodiments of the present disclosure.
[0011] FIGS. **3**C-**3**F illustrate cross-section views of different storage three-dimensional memory devices than FIG. **3**B in accordance with to some embodiments of the present disclosure.
[0012] FIGS. **4**A to **4**C are a method M of manufacturing computing three-dimensional memory devices and storage three-dimensional memory devices of an integrated circuit structure in accordance with some embodiments of the present disclosure.
[0013] FIGS. **5**A to **27**B illustrate various views of an integrated circuit structure (or a portion of the example semiconductor die) during various fabrication stages, made by the method of FIGS. **4**A and **4**B, in accordance with some embodiments of the present disclosure.
[0014] FIG. **28**A a schematic diagram illustrating a relationship between voltage and bit current count of computing three-dimensional memory devices in accordance with some embodiments of the present disclosure.
[0015] FIG. **28**B a schematic diagram illustrating a relationship between voltage and bit current count of storage three-dimensional memory devices in accordance with some embodiments of the present disclosure.

DETAILED DESCRIPTION

[0016] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.
[0017] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper” and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.
[0018] As used herein, “around,” “about,” “approximately,” or “substantially” may mean within 20 percent, or within 10 percent, or within 5 percent of a given value or range. One skilled in the art will realize, however, that the value or range recited throughout the description are merely examples, and may be reduced with the down-scaling of the integrated circuits. Numerical quantities given herein are approximate, meaning that the term “around,” “about,” “approximately,” or “substantially” can be inferred if not expressly stated.
[0019] For next generation semiconductor devices, particularly memory devices, it is desirable to include memories that can perform high speed computing as well as memories that can provide long term storage (i.e., low leakage). Current semiconductor die manufacturing processes and semiconductor dies formed therefrom include high speed computing devices and the long term storage devices formed on separate dies, which are then integrated together using a chip integration process (e.g., using an interposer, or a 2.5 dimensional process). However, the separation between the two dies causes propagation delay as data is being transferred between computing and storage memory devices which can reduce data fidelity and increase processing time.
[0020] Therefore, the present disclosure in various embodiments provides a semiconductor die

including a plurality of computing 3-dimensional (3D) memory devices (e.g., AND memory devices) that provide high speed computing and a plurality of storage 3D memory devices (e.g., NAND memory devices) that provide high density storage for a multi-level cell. The computing and storage 3D memory devices are used to a computing in memory (CIM) application and formed monolithically in the same die, which in turn allows for improving a propagation delay issue while data is transferred between the computing and storage 3D memory devices and achieving a within-wafer multiple memory integration. This beneficially reduces computing power needed to perform the same operation, reduces propagation losses, and reduces manufacturing cost, time, and complexity.

[0021] Various embodiments provide a three-dimensional memory array with a plurality of vertically stacked memory cells. Each memory cell includes transistor having a word line region acting as a gate electrode, a bit line region acting as a first source/drain electrode, and a source line region acting as a second source/drain electrode. Each transistor further includes a memory film (e.g., as a gate dielectric) and a channel region over the word line region.

[0022] FIG. **1**A is a perspective view of a semiconductor die **100**, according to an embodiment. The semiconductor die **100** has a first memory array **103***a* of a first set **104***a* of semiconductor devices **110***a* (hereinafter "first semiconductor devices **110***a*") disposed at a first location of the semiconductor die **100**, and a second memory array **103***b* of a second set **104***b* of semiconductor devices **110***b* (hereinafter "second semiconductor devices **110***b*") disposed at a second location of the semiconductor die **100** different from the first location. In some embodiments, the semiconductor die **100** can be interchangeably referred to as a chip area. In some embodiments, the first semiconductor devices **110***a* can be interchangeably referred to as a first memory cell or a first memory device, and the second semiconductor devices **110***b* can be interchangeably referred to as a second memory cell or a second memory device. The first semiconductor device **110***a* may be a computing memory device (e.g. AND memory device), and the second semiconductor device **110***b* may be a storage memory device (e.g. NAND memory device) in this context. The first semiconductor devices **110***a* being the AND memory device may have a higher cell current and a higher speed computing than the second semiconductor devices **110***b* that allow the first semiconductor devices **110***a* to be used for data processing and computing operations relative to the second semiconductor devices **110***b*. In contrast, the second semiconductor devices **110***b* being the NAND memory device may have a higher density storage than the first semiconductor devices **110***a* that allow the second semiconductor devices **110***b* to be used for a larger data storage relative to the first semiconductor devices **110***a*. Thus, the second semiconductor devices **110***b* can be used for high density storage of data generated after processing and computing by the first semiconductor devices **110***a*. Therefore, the semiconductor die **100** integrates processing and computing, as well as a high density storage in a single die reducing processing time, increasing processing speed, and reducing lag and propagation delays, and data loss.

[0023] As shown in FIG. **1**A, the first memory array **103***a* is disposed on a first side **102***a* (or first portion) of the semiconductor die **100** in a first direction (e.g., the X-direction), and the second memory array **103***b* is disposed on a second side **102***b* of the semiconductor die **100** in the first direction (e.g., the X-direction). An array isolation layer **109** is interposed between the first memory array **103***a* and the second memory array **103***b* and serves to electrically isolate the first memory array **103***a* from the second memory array **103***b* and extends in a second direction (e.g., the Y-direction) that is perpendicular to the first direction. The array isolation layer **109** may be formed from an electrically insulative material, for example, silicon dioxide (SiO.sub.2), silicon nitride (SiN), silicon oxide (SiO), silicon carbide nitride (SiCN), silicon oxycarbonitride (SiOCN), silicon oxynitride (SiON), HfO.sub.2, TaO.sub.x, TiO.sub.x, AlO.sub.x, any other suitable material, or combination thereof.

[0024] The first semiconductor devices **110***a* included in each of the first set **104***a* of the first memory array **103***a* are disposed in a 3D configuration. For example, the first semiconductor

devices **110***a* in the first set **104***a* are stacked on top of each other in the vertical direction (e.g., the Z-direction), and disposed adjacent to each other in the first direction (e.g., the X-direction) and the second direction (e.g., the Y-direction). In other words, the first set **104***a* of the first semiconductor devices **110***a* are arranged in a cube formation. A first set of isolation layers **106***a* is interposed between each of the first set **104***a* of the first set of semiconductor devices **110***a* to electrically isolate each of the first set **104***a* of first semiconductor devices **110***a* from each other. For example, the first set of isolation layers **106***a* may include first portions that extend in the first direction (e.g., the X-direction) from a second portion that extends in the second direction (e.g., the Y-direction). The first set of isolation layers **106***a* may be formed from an electrically insulative material, for example, silicon dioxide (SiO.sub.2), silicon nitride (SiN), silicon oxide (SiO), silicon carbide nitride (SiCN), silicon oxycarbonitride (SiOCN), silicon oxynitride (SiON), HfO.sub.2, TaO.sub.x, TiO.sub.x, AlO.sub.x, any other suitable material, or combination thereof.

[0025] Similarly, the second semiconductor devices **110***b* included in each of the second set **104***b* of the second memory array **103***b* are disposed in a 3D configuration, for example, stacked on top of each other in the vertical direction (e.g., the Z-direction), and disposed adjacent to each other in the first direction (e.g., the X-direction) and the second direction (e.g., the Y-direction), similar to the first set **104***a* of the first semiconductor devices **110***a*. A second set of isolation layers **106***b* is interposed between each of the second set **104***b* of the second set of semiconductor devices **110***b* to electrically isolate each of the second set **104***b* of second semiconductor devices **110***b* from each other. For example, the second set of isolation layers **106***b* may include first portions that extend in the first direction (e.g., the X-direction) from a second portion that extends in the second direction (e.g., the Y-direction). The second set of isolation layers **106***b* may be formed from the same material as the first set of isolation layers **106***a*.

[0026] FIG. **1**B is a perspective view of a semiconductor die **200**, according to another embodiment. The semiconductor die **200** includes the first set **104***a* of first semiconductor devices **110***a* and the second set **104***b* of second semiconductor devices **110***b* as described with respect to the semiconductor die **100**. However, different from the semiconductor die **100**, the first set **104***a* of first semiconductor devices **110***a* in the semiconductor die **200** is disposed adjacent to the second set **104***b* of the second semiconductor devices **110***b* in at least the first direction (e.g., the X-direction), the second direction (e.g., the Y-direction), or the first direction and the second direction. In other words, the first set **104***a* of the semiconductor die **200** is disposed alternately with the second set **104***b* in the X-direction as well as the Y-direction throughout a length and a width of the semiconductor die **200**. A set isolation layer **206** interposed between each of the first set **104***a* and the second set **104***b* in the semiconductor die **200**. For example, the set isolation layer **206** of the semiconductor die **200** may include first portions that extend in the first direction (e.g., the X-direction) from a second portion that extends in the second direction (e.g., the Y-direction). The set isolation layer **206** may be formed from an electrically insulative material, for example, silicon dioxide (SiO.sub.2), silicon nitride (SiN), silicon oxide (SiO), silicon carbide nitride (SiCN), silicon oxycarbonitride (SiOCN), silicon oxynitride (SiON), HfO.sub.2, TaO.sub.x, TiO.sub.x, AlO.sub.x, any other suitable material, or combination thereof.

[0027] It should be appreciated that while semiconductor die **100** and semiconductor die **200** illustrate particular embodiments of the first set **104***a* of first semiconductor devices **110***a* and the second set **104***b* of the second semiconductor dies **110***b* arranged in specific configurations, in other embodiments the first set **104***a* of the first semiconductor devices **110***a* and the second set **104***b* of the second semiconductor devices **110***b* can be arranged in any suitable configuration or arrangement in a semiconductor die with an isolation layer electrical isolating adjacent sets **104***a*/**104***b* from each other. All such arrangements are contemplated and should be considered to be within the scope of the present disclosure.

[0028] Reference is made to FIGS. **1**A and **2**A-**3**B. FIG. **2**A is a perspective view of a first portion of the semiconductor die **100** of FIG. **1**A including the first set **104***a* of the first semiconductor

devices **110***a* indicated by the arrow A in FIG. **1**A, and FIG. **3**A is a perspective view of a second portion of the semiconductor die **100** indicated by the arrow B in FIG. **1**A that includes the second set **104***b* of the second semiconductor devices **110***b*, in accordance with some embodiments of the present disclosure. FIG. **2**B illustrates a cross-section view of the first semiconductor devices **110***a*, taken along the line X-X in FIG. **2**A, and FIG. **3**B illustrates a cross-section view of the second semiconductor devices **110***b*, taken along the line Y-Y in FIG. **3**A, in accordance with some embodiments of the present disclosure. While FIGS. **2**A-**3**B show some embodiments of the first and semiconductor devices **110***a* and **110***b*, various configurations of first and second semiconductor devices can be employed in the first set **104***a* and the second set **104***b* of the semiconductor die **100**, the semiconductor die **200**, or any other semiconductor die described herein.

[0029] As shown in FIGS. **1**A, **2**A, and **2**B, the first memory array **103***a* (see FIG. **1**A) may be an AND memory array. Each first semiconductor device **110***a* in the first memory array **103***a* may be a transistor. The first semiconductor device **110***a* (see FIG. **2**B) may include a gate layer **124***a* that can serve as a gate electrode, a memory layer **114***a* that can serve as a gate dielectric, a channel layer **116***a* that can serve as a channel region, and conductive lines **120***a* and **122***a* (see FIG. **2**A) that can serve as source and drain electrodes. In some embodiments, the gate layer **124***a* is electrically coupled to a respective word line and can be interchangeably referred to as a word line metal. In some embodiments, the conductive line **120***a* is electrically coupled to a respective global source line, which electrically couples the conductive line **120***a* to ground, and can be interchangeably referred to as a conductive source line. In some embodiments, the conductive line **122***a* (see FIG. **2**A) is electrically coupled to a respective global bit line and can be interchangeably referred to as a conductive bit line. The first semiconductor device **110***a* may be disposed in an array of vertically stacked rows and columns. The first semiconductor devices **110***a* in a same horizontal row of the first memory array **103***a* (see FIG. **1**A) may share a common word line while the first semiconductor devices **110***a* in a same vertical column of the first memory array **103***a* may share a common source line or a common bit line. Therefore, the first semiconductor devices **110***a* may withstand a higher cell current and process a higher speed computing than the second semiconductor devices **110***b*, which in turn allows the first semiconductor devices **110***a* to be used for data processing and computing operations relative to the second semiconductor devices **110***b*.

[0030] As shown in FIGS. **1**A, **3**A, and **3**B, the second memory array **103***b* (see FIG. **1**A) may be an NAND memory array. Each second semiconductor device **110***b* in the second memory array **103***b* may be a transistor. The second semiconductor device **110***b* (see FIG. **3**B) may include a gate layer **124***b* that can serve as a gate electrode, a memory layer **114***b* that can serve as a gate dielectric, a channel layer **116***b* that can serve as a channel region, and conductive lines **120***b* and **122***b* that can serve as source and drain electrodes. In some embodiments, the gate layer **124***b* is electrically coupled to a respective word line and can be interchangeably referred to as a word line metal. In some embodiments, the conductive line **120***b* is electrically coupled to a respective global source line, which electrically couples the conductive line **120***b* to ground, and can be interchangeably referred to as a conductive source line. In some embodiments, the conductive line **122***b* is electrically coupled to a respective global bit line and can be interchangeably referred to as a conductive bit line. The second semiconductor device **110***b* may be disposed in an array of vertically stacked rows and columns. The second semiconductor devices **110***b* in a same horizontal row of the second memory array **103***b* (see FIG. **1**A) may share a common word line while the second semiconductor devices **110***b* in a same vertical column of the second memory array **103***b* may share a common source line and a common bit line. Therefore, the second semiconductor devices **110***b* may have a higher density storage than the first semiconductor devices **110***a*, which in turn allows the second semiconductor devices **110***b* to be used for a larger data storage relative to the first semiconductor devices **110***a*.

[0031] Reference is made to FIGS. **2**A-**3**B. The semiconductor die **100** includes a substrate **107** on

which the plurality of semiconductor devices **110***a/b* are disposed. The first semiconductor devices **110***a* and the second semiconductor devices **110***b* are respectively arranged in a plurality of rows within their respective sets **104***a/b* (see FIGS. **2**A and **3**A), each of which extend in a first direction (e.g., the direction). Each semiconductor device **110***a/b* is separated and electrically isolated from an adjacent semiconductor device **110***a/b* within a row by a device spacer **113***a/b* (see FIGS. **2**A and **3**A). In some embodiments, the substrate **107** may be a semiconductor substrate, such as a bulk semiconductor, a semiconductor-on-insulator (SOI) substrate, or the like, which may be doped (e.g., with a p-type or an n-type impurity) or un-doped. The substrate **107** may be a wafer, such as a silicon wafer. Generally, a SOI substrate is a layer of a semiconductor material formed on an insulator layer. The insulator layer may be, for example, a buried oxide (BOX) layer, a silicon oxide layer, or the like. The insulator layer is provided on a substrate, typically a silicon or glass substrate. Other substrates, such as a multi-layered or gradient substrate may also be used. In some embodiments, the semiconductor material of the substrate **107** may include silicon; germanium; a compound semiconductor including silicon carbide, gallium arsenide, gallium phosphide, indium phosphide, indium arsenide, and/or indium antimonide; an alloy semiconductor including silicon germanium, gallium arsenide phosphide, aluminum indium arsenide, aluminum gallium arsenide, gallium indium arsenide, gallium indium phosphide, and/or gallium indium arsenide phosphide; combinations thereof; or the like. In some embodiments, the device spacer **113***a/b* be formed from an electrically insulating material (e.g., silicon oxide (SiO.sub.2), silicon nitride (SiN), silicon oxide (SiO), silicon carbide nitride (SiCN), silicon oxycarbonitride (SiOCN), silicon oxynitride (SiON), HfO.sub.2, TaO.sub.x, TiO.sub.x, AlO.sub.x, etc.). In some embodiments, an etch stop layer **101** may be formed between the substrate **107** and the semiconductor devices **110***a/b*. In some embodiments, the etch stop layer **101** may include SiN, SiO, SiO.sub.2, SiCN, SiOCN, SiON, HfO.sub.2, TaO.sub.x, TiO.sub.x, AlO.sub.x, a metal carbide, any other suitable material or combination thereof, and may include a single layer or various sublayers.

[0032] In FIGS. **2**A and **2**B, the semiconductor device **110***a* may include the conductive line **120***a*, and the conductive line **122***a* spaced apart from the conductive line **120***a* in a first direction (e.g., the X-direction). The conductive line **120***a* extends from a top surface of a stacked structure **108***a* to the etch stop layer **101** in a vertical direction (e.g., the Z-direction). The conductive line **122***a* extends from the top surface of the stacked structure **108***a* to the etch stop layer **101** in the vertical direction. Although FIG. **2**B illustrates a cross-sectional view that only shows the conductive line **120***a*, a cross-sectional view of the conductive line **122***a* may be similar. In some embodiments, the conductive line **120***a* and the conductive line **122***a* may include a conductive material, for example, metals such as Al, Ti, TiN, TaN, Co, Ag, Au, Cu, Ni, Cr, Hf, Ru, W, Pt, WN, any other suitable material or a combination or alloy thereof. In some embodiments, the conductive line **120***a* and/or the conductive line **122***a* may include a semiconductor material, for example, an n or p-doped semiconductor such as Si, SiGe, or any other semiconductor material (e.g., IGZO, ITO, IZO, ZnO, IWO, poly silicon, amorphous Si, etc.), and may be formed using a deposition process, an epitaxial growth process, or any other suitable process.

[0033] The semiconductor device **110***a* may include reduced parasitic resistance capacitance (RC) layers **150***a* and **152***a* that have lower parasitic resistance capacitances relative to the conductive lines **120***a* and **122***a*. The reduced parasitic RC layers **150***a* and **152***a* cup undersides of the conductive lines **120***a* and **122***a* to reduce parasitic resistance between the conductive lines **120***a* and **122***a* and the channel layers **116***a*, which in turn allows for forming an ohmic contact and keeping a target threshold voltage V.sub.t to be positive. Therefore, the semiconductor die **100** may have a higher processing speed and lower power consumption during a read operation than that without reduced parasitic RC layers. In some embodiments, the reduced parasitic RC layers **150***a* and/or **152***a* may include a conductive material, for example, metals such as Al, Ti, TiN, TaN, Co, Ag, Au, Cu, Ni, Cr, Hf, Ru, W, Pt, WN, any other suitable material or a combination or alloy thereof. In some embodiments, the reduced parasitic RC layers **150***a* and/or **152***a* may include a

semiconductor material, for example, an n or p-doped semiconductor such as Si, SiGe, or any other semiconductor material (e.g., IGZO, ITO, IZO, ZnO, IWO, poly silicon, amorphous Si, etc.). In some embodiments, the reduced parasitic RC layer **150***a* and/or **152***a* may have a higher doped concentration than the channel layer **116***a*. By way of example and not limitation, the reduced parasitic RC layer **150***a* and/or **152***a* may be a doped layer, but the channel layer **116***a* may be an un-doped layer.

[0034] The semiconductor device **110***a* may include a first inner spacer **118***a* as shown in FIG. **2**A extending between the conductive lines **120***a* and **122***a* and from the top surface of the stacked structure **108***a* to the etch stop layer **101** in a vertical direction (e.g., the Z-direction). In some embodiments, the first inner spacer **118***a* may be formed from an electrically insulating material, for example, silicon nitride (SiN), silicon oxide (SiO), SiO.sub.2, silicon carbide nitride (SiCN), silicon oxycarbonitride (SiOCN), silicon oxynitride (SiON), HfO.sub.2, TaO.sub.x, TiO.sub.x, AlO.sub.x, etc.

[0035] The semiconductor device **110***a* may include the channel layer **116***a* disposed outwards of a radially outer surface of the conductive line **120***a* and the conductive line **122***a* in a second direction (e.g., the Y-direction) perpendicular to a first direction (e.g., the X-direction) and is in electrical contact with the conductive line **120***a* and the conductive line **122***a*. The channel layer **116***a* extends in the first direction (e.g., the X-direction) from an axially outward edge of the conductive line **120***a* to an opposite axially outward edge of the conductive line **122***a*. In some embodiments, each semiconductor device **110***a* includes a pair of channel layers **116***a*. One of the pair of channel layers **116***a* is disposed radially outwards of first radially outer surfaces of the conductive line **120***a* and the conductive line **122***a* in the second direction (e.g., the Y-direction), and the other of the pair of channel layers **116***a* is disposed radially outwards of second radially outer surfaces of the conductive line **120***a* and the conductive line **122***a* opposite the first radially outer surfaces. In some embodiments, each semiconductor device **110***a* may include a single channel layer **116***a* disposed radially outwards of the first or the second radially outer surfaces of the conductive line **120***a* and the conductive line **122***a*. The channel layer **116***a* extends from the top surface of the stacked structure **108***a* to the etch stop layer **101** in a vertical direction (e.g., the Z-direction). In some embodiments, the channel layer **116***a* may include a doped material (e.g., a doped semiconductor), doped with a first concentration of a dopant (e.g., an n-type or p-type dopant). In some embodiments, the channel layer **116***a* may be free of a dopant. In some embodiments, the channel layer **116***a* may be formed from a semiconductor material, for example, Si (e.g., polysilicon or amorphous silicon), Ge, SiGe, silicon carbide (SiC), IGZO, ITO, ZnO, IWO, etc. and can be an n-type or p-type doped semiconductor.

[0036] The semiconductor device **110***a* may include the memory layer **114***a* disposed on a radially outer surface of the channel layer **116***a* in the second direction (e.g., the Y-direction) and extends in the first direction (e.g., the X-direction), such that each semiconductor device **110***a* located in a row of the array of semiconductor devices **110***a* including a portion of the memory layer **114***a*, and the memory layer **114***a* is connected to each of the semiconductor devices **110***a* included in a corresponding row. In some embodiments, the memory layer **114***a* extends from the top surface of the stacked structure **108***a* to the etch stop layer **101** in a vertical direction (e.g., the Z-direction). In some embodiments, the memory layer **114***a* may include a ferroelectric material, for example, lead zirconate titanate (PZT), PbZr/TiO.sub.3, BaTiO.sub.3, PbTiO.sub.2, HfO.sub.2, Hr.sub.1-xZr.sub.xO.sub.2, ZrO.sub.2, TiO.sub.2, NiO, TaO.sub.x, Cu.sub.2O, Nb.sub.2O.sub.5, AlO.sub.x, etc.

[0037] The semiconductor device **110***a* may include a stacked structure **108***a* disposed on outer surfaces of the memory layer **114***a* in the second direction and over the substrate **107**. The stacked structure **108***a* include a plurality of insulating layers **112***a*, and a plurality of gate layers **124***a* alternatively stacked on top of one another in a vertical direction (e.g., the Z-direction), and extending in the first direction (e.g., the X-direction). In some embodiments, a topmost layer and/or

a bottommost layer of the stacked structure **108***a* may be the insulating layer **112***a*. This is described in greater detail with reference to FIGS. **2**A and **2**B, the semiconductor device **110***a* may include at least one gate layer **124***a* disposed on a radially outer surface of the memory layer **114***a* in the second direction (e.g., the Y-direction), and extending in the first direction (e.g., the X-direction). Within the stacked structure **108***a*, two parallel gate layers **124***a* are located adjacent to each other and interposed between two vertically separated insulating layers **112***a* in the vertical direction (e.g., the Z-direction), each of the two gate layers **124***a* associated with a different semiconductor device **110***a*. A spacer layer **111***a* is laterally interposed between the two gate layers **124***a* in the second direction (e.g., the Y-direction) and serves to electrically isolate the two gate layers **124***a* from each other.

[0038] In some embodiments, the insulating layer **112***a* may include silicon nitride (SiN), silicon oxide (SiO), SiO.sub.2, silicon carbide nitride (SiCN), silicon oxycarbonitride (SiOCN), silicon oxynitride (SiON), HfO.sub.2, TaO.sub.x, TiO.sub.x, AlO.sub.x, etc. In some embodiments, the first gate layer **124***a* may include an n-type or n-doped semiconductor material. Example n-type workfunction metals that may include Ti, Ag, TaAl, TaAlC, TiAlN, TaC, TaCN, TaSiN, Mn, Zr, other suitable n-type workfunction materials, or combinations thereof. In some embodiments, the first gate layer **124***a* may include a p-type or p-doped material. Example p-type workfunction metals that may include TiN, TaN, Ru, Mo, Al, WN, ZrSi.sub.2, MoSi.sub.2, TaSi.sub.2, NiSi.sub.2, WN, other suitable p-type workfunction materials, or combinations thereof. While shown as including a single layer, each of the gate layers **124***a* may include multi-layers of the workfunction material, or combinations thereof.

[0039] In some embodiments, an adhesive layer may be interposed between the gate layer **124***a* and the adjacent insulating layers **112***a* as well as the spacer layer **111***a* disposed therebetween, and facilitate adhesion of the gate layer **124***a* to the insulating layer **112***a*, and may also serve as a spacer between two parallel gate layers **124***a* that are interposed between the same vertically separated insulating layers **112***a*. In some embodiments, the adhesion layer (e.g., the adhesive layer) may include e.g., titanium (Ti), chromium (Cr), TiN, TaN, WN, or any other suitable adhesive material.

[0040] Reference is made to FIGS. **3**A and **3**B. The semiconductor device **110***b* may include the conductive line **120***b*, and the conductive line **122***b* spaced apart from the conductive line **120***b* in a vertical direction (e.g., the Z-direction). The conductive line **120***b* extends in the substrate **107**. The conductive line **122***b* extends from the top surface of the stacked structure **108***b* and terminates prior to reaching the etch stop layer **101** in the vertical direction. In some embodiments, the conductive line **122***b* terminates at a position higher than a bottom surface of a topmost one of insulating layers **112***b* in a stacked structure **108***b*. In some embodiments, the conductive line **120***b* and the conductive line **122***b* may include a conductive material, for example, metals such as Al, Ti, TiN, TaN, Co, Ag, Au, Cu, Ni, Cr, Hf, Ru, W, Pt, WN, any other suitable material or a combination or alloy thereof. In some embodiments, the conductive line **120***b* and/or the conductive line **122***b* may include a semiconductor material, for example, an n or p-doped semiconductor such as Si, SiGe, or any other semiconductor material (e.g., IGZO, ITO, IZO, ZnO, IWO, poly silicon, amorphous Si, etc.), and may be formed using a deposition process, an epitaxial growth process, or any other suitable process.

[0041] The semiconductor device **110***b* may include reduced parasitic RC layers **150***b* and **152***b* that have lower resistance capacitances relative to the conductive lines **120***b* and **122***b*. An underside of the reduced parasitic RC layer **150***b* is cupped by the conductive line **120***b* and the reduced parasitic RC layer **152***b* cup an underside of the conductive line **122***b*, so as parasitic resistances between the conductive lines **120***b* and **122***b* and the channel layers **116***b* may be to reduced, which in turn allows for forming an ohmic contact and keeping a target threshold voltage V.sub.t to be positive. Therefore, the semiconductor die **100** may have a higher processing speed and lower power consumption during a read operation than that without reduced parasitic RC

layers. In some embodiments, the reduced parasitic RC layers **150***b* and/or **152***b* may include a conductive material, for example, metals such as Al, Ti, TiN, TaN, Co, Ag, Au, Cu, Ni, Cr, Hf, Ru, W, Pt, WN, any other suitable material or a combination or alloy thereof. In some embodiments, the reduced parasitic RC layers **150***b* and/or **152***b* may include a semiconductor material, for example, an n or p-doped semiconductor such as Si, SiGe, or any other semiconductor material (e.g., IGZO, ITO, IZO, ZnO, IWO, poly silicon, amorphous Si, etc.). In some embodiments, the reduced parasitic RC layer **150***b* and/or **152***b* may have a higher doped concentration than the channel layer **116***b*. By way of example and not limitation, the reduced parasitic RC layer **150***b* and/or **152***b* may be a doped layer, but the channel layer **116***b* may be an un-doped layer.

[0042] The semiconductor device **110***b* may include a channel layer **116***b* disposed outwards of a radially outer surface of the conductive line **120***b* and the conductive line **122***b* in a second direction (e.g., the Y-direction) perpendicular to a first direction (e.g., the X-direction) and is in electrical contact with the conductive line **120***b* and the conductive line **122***b*. The channel layer **116***b* extends in the vertical direction (e.g., the Z-direction) from an axially upward edge of the conductive line **120***b* upwardly to an axially upward edge of the conductive line **122***b*. In some embodiments, the channel layer **116***b* has a U-shaped cross section taken along the line Y-Y as shown in FIG. **3**B. In some embodiments, a combination of the conductive line **120***b* and the reduced parasitic RC layers **150***b* may have a width, taken along the line X-X in FIG. **2**B, substantially the same as a width of the channel layer **116***b*. In some embodiments, a combination of the conductive line **120***b* and the reduced parasitic RC layers **150***b* may have a width less or greater than a width of the channel layer **116***b*. In some embodiments, the conductive line **120***b* and/or the reduced parasitic RC layers **152***b* may have a flat bottom surface. In some embodiments, the conductive line **120***b* and/or the reduced parasitic RC layers **152***b* may have a convex bottom surface or a concave bottom surface. In some embodiments, the channel layer **116***b* may include a doped material (e.g., a doped semiconductor), doped with a first concentration of a dopant (e.g., an n-type or p-type dopant). In some embodiments, the channel layer **116***b* may be free of a dopant. In some embodiments, the channel layer **116***b* may be formed from a semiconductor material, for example, Si (e.g., polysilicon or amorphous silicon), Ge, SiGe, silicon carbide (SiC), IGZO, ITO, ZnO, IWO, etc. and can be an n-type or p-type doped semiconductor.

[0043] The semiconductor device **110***b* may include a memory layer **114***b* disposed on a radially outer surface of the channel layer **116***b* in the second direction (e.g., the Y-direction) and extends in the first direction (e.g., the X-direction), such that each semiconductor device **110***b* located in a row of the array of semiconductor devices **110***b* including a portion of the memory layer **114***b*, and the memory layer **114***b* is connected to each of the semiconductor devices **110***b* included in a corresponding row. In some embodiments, the memory layer **114***b* extends from the stacked structure **108***b* to the etch stop layer **101** in a vertical direction (e.g., the Z-direction). In some embodiments, the memory layer **114***b* may include a ferroelectric material, for example, lead zirconate titanate (PZT), PbZr/TiO.sub.3, BaTiO.sub.3, PbTiO.sub.2, HfO.sub.2, Hr.sub.1-xZr.sub.xO.sub.2, ZrO.sub.2, TiO.sub.2, NiO, TaO.sub.x, Cu.sub.2O, Nb.sub.2O.sub.5, AlO.sub.x, etc.

[0044] The semiconductor device **110***b* may include a stacked structure **108***a* disposed on outer surfaces of the memory layer **114***b* in the second direction and over the substrate **107**. The stacked structure **108***b* include a plurality of insulating layers **112***b*, and a plurality of gate layers **124***b* alternatively stacked on top of one another in a vertical direction (e.g., the Z-direction), and extending in the first direction (e.g., the X-direction). In some embodiments, a topmost layer and/or a bottommost layer of the stacked structure **108***a* may be the insulating layer **112***b*. This is described in greater detail with reference to FIGS. **3**A and **3**B, the semiconductor device **110***b* may include at least one gate layer **124***b* disposed on a radially outer surface of the memory layer **114***b* in the second direction (e.g., the Y-direction), and extending in the first direction (e.g., the X-direction). Within the stacked structure **108***a*, two parallel gate layers **124***b* are located adjacent to

each other and interposed between two vertically separated insulating layers **112***b* in the vertical direction (e.g., the Z-direction), each of the two gate layers **124***b* associated with a different semiconductor device **110***b*. A spacer layer **111***a* is laterally interposed between the two gate layers **124***b* in the second direction (e.g., the Y-direction) and serves to electrically isolate the two gate layers **124***b* from each other.

[0045] In some embodiments, the insulating layer **112***b* may include silicon nitride (SiN), silicon oxide (SiO), SiO.sub.2, silicon carbide nitride (SiCN), silicon oxycarbonitride (SiOCN), silicon oxynitride (SiON), HfO.sub.2, TaO.sub.x, TiO.sub.x, AlO.sub.x, etc. In some embodiments, the first gate layer **124***b* may include an n-type or n-doped semiconductor material. Example n-type workfunction metals that may include Ti, Ag, TaAl, TaAlC, TiAlN, TaC, TaCN, TaSiN, Mn, Zr, other suitable n-type workfunction materials, or combinations thereof. In some embodiments, the first gate layer **124***b* may include a p-type or p-doped material. Example p-type workfunction metals that may include TiN, TaN, Ru, Mo, Al, WN, ZrSi.sub.2, MoSi.sub.2, TaSi.sub.2, NiSi.sub.2, WN, other suitable p-type workfunction materials, or combinations thereof. While shown as including a single layer, each of the gate layers **124***b* may include multi-layers of the workfunction material, or combinations thereof.

[0046] In some embodiments, an adhesive layer may be interposed between the gate layer **124***b* and the adjacent insulating layers **112***b* as well as the spacer layer **111***b* disposed therebetween, and facilitate adhesion of the gate layer **124***b* to the insulating layer **112***b*, and may also serve as a spacer between two parallel gate layers **124***b* that are interposed between the same vertically separated insulating layers **112***b*. In some embodiments, the adhesion layer (e.g., the adhesive layer) may include e.g., titanium (Ti), chromium (Cr), TiN, TaN, WN, or any other suitable adhesive material.

[0047] In some embodiments, material and manufacturing method of the conductive lines **120***b* and **122***b*, reduced parasitic RC layers **150***b* and **152***b*, the gate layer **124***b*, the channel layer **116***b*, the memory layers **114***b*, the spacer layer **111***b*, the insulating layer **112***b*, and the device spacer **113***b* included in the second semiconductor devices **110***b*, are substantially the same as those of the conductive lines **120***a* and **122***a*, reduced parasitic RC layers **150***a* and **152***a*, the gate layer **124***a*, the channel layer **116***a*, the memory layers **114***a*, the spacer layer **111***a*, the insulating layer **112***a*, and the device spacer **113***a*, i.e., are formed from the same material and are structurally and functionally similar to each other. This beneficially reduces computing power needed to perform the same operation, reduces propagation losses, and reduces manufacturing cost, time, and complexity.

[0048] While FIGS. **2**A-**3**B show some embodiments of the first and semiconductor devices **110***a* and **110***b*, various configurations of first and second semiconductor devices can be employed in the first set **104***a* and the second set **104***b* of the semiconductor die **100**, the semiconductor die **200**, or any other semiconductor die described herein. Example embodiments of first semiconductor devices and second semiconductor devices that can be included in the semiconductor die **100** or the semiconductor die **200** are shown and described in FIGS. **3**C to **3**F. It should be appreciated that the semiconductor die **100**, **200**, or any other semiconductor die described herein can include any combination of first and second semiconductor devices as described with respect to FIGS. **2**A-**3**F.

[0049] In some embodiments, a combination of the conductive line **120***b* and the reduced parasitic RC layers **150***b* as shown in FIG. **3**B may have a width less than or greater than a width of the channel layer **116***b*. FIGS. **3**C and **3**D are cross-section views of second semiconductor devices **210***b* and **310***b*. As shown in FIG. **3**C, the combination of the conductive line **220***b* and the reduced parasitic RC layers **250***b* may have a width less than a width of the channel layer **216***b*. In some embodiments, material and manufacturing method of the etch stop layer **201**, the substrate **207**, the conductive lines **220***b* and **222***b*, reduced parasitic RC layers **250***b* and **252***b*, the gate layer **224***b*, the channel layer **216***b*, the memory layer **214***b*, the spacer layer **211***b*, and the insulating layer **212***b* included in the second semiconductor devices **210***b*, are substantially the same as those of the

etch stop layer **101**, the substrate **107**, the conductive lines **120***b* and **122***b*, reduced parasitic RC layers **150***b* and **152***b*, the gate layer **124***b*, the channel layer **116***b*, the memory layer **114***b*, the spacer layer **111***b*, and the insulating layer **112***b* as shown in FIGS. **3**A and **3**B, and the related detailed descriptions may refer to the foregoing paragraphs, and are not described again herein.

[0050] As shown in FIG. **3**D, the combination of the conductive line **320***b* and the reduced parasitic RC layers **350***b* may have a width greater than a width of the channel layer **316***b*. In some embodiments, material and manufacturing method of the etch stop layer **301**, the substrate **307**, the conductive lines **320***b* and **322***b*, reduced parasitic RC layers **350***b* and **352***b*, the gate layer **324***b*, the channel layer **316***b*, the memory layer **314***b*, the spacer layer **311***b*, and the insulating layer **312***b* included in the second semiconductor devices **210***b*, are substantially the same as those of the etch stop layer **101**, the substrate **107**, the conductive lines **120***b* and **122***b*, reduced parasitic RC layers **150***b* and **152***b*, the gate layer **124***b*, the channel layer **116***b*, the memory layer **114***b*, the spacer layer **111***b*, and the insulating layer **112***b* as shown in FIGS. **3**A and **3**B, and the related detailed descriptions may refer to the foregoing paragraphs, and are not described again herein.

[0051] In some embodiments, the conductive line **122***b* and/or the reduced parasitic RC layers **152***b* as shown in FIG. **3**B may have a convex bottom surface or a concave bottom surface. FIGS. **3**E and **3**F are cross-section views of second semiconductor devices **410***b* and **510***b*. As shown in FIG. **3**E, the conductive line **422***b* and/or the reduced parasitic RC layers **452***b* may have a convex bottom surface. In some embodiments, material and manufacturing method of the etch stop layer **401**, the substrate **407**, the conductive lines **420***b* and **422***b*, reduced parasitic RC layers **450***b* and **452***b*, the gate layer **424***b*, the channel layer **416***b*, the memory layer **414***b*, the spacer layer **411***b*, and the insulating layer **412***b* included in the second semiconductor devices **410***b*, are substantially the same as those of the etch stop layer **101**, the substrate **107**, the conductive lines **120***b* and **122***b*, reduced parasitic RC layers **150***b* and **152***b*, the gate layer **124***b*, the channel layer **116***b*, the memory layer **114***b*, the spacer layer **111***b*, and the insulating layer **112***b* as shown in FIGS. **3**A and **3**B, and the related detailed descriptions may refer to the foregoing paragraphs, and are not described again herein.

[0052] As shown in FIG. **3**F, the conductive line **522***b* and/or the reduced parasitic RC layers **552***b* may have a concave bottom surface. In some embodiments, material and manufacturing method of the etch stop layer **501**, the substrate **507**, the conductive lines **520***b* and **522***b*, reduced parasitic RC layers **550***b* and **552***b*, the gate layer **524***b*, the channel layer **516***b*, the memory layer **514***b*, the spacer layer **511***b*, and the insulating layer **512***b* included in the second semiconductor devices **510***b*, are substantially the same as those of the etch stop layer **101**, the substrate **107**, the conductive lines **120***b* and **122***b*, reduced parasitic RC layers **150***b* and **152***b*, the gate layer **124***b*, the channel layer **116***b*, the memory layer **114***b*, the spacer layer **111***b*, and the insulating layer **112***b* as shown in FIGS. **3**A and **3**B, and the related detailed descriptions may refer to the foregoing paragraphs, and are not described again herein.

[0053] Referring now to FIGS. **4**A to **4**C, illustrated is a flowchart of an exemplary method M for fabrication of a semiconductor die **100** in accordance with some embodiments. The method M includes a relevant part of the entire manufacturing process. It is understood that additional operations may be provided before, during, and after the operations shown by FIGS. **4**A to **4**C, and some of the operations described below can be replaced or eliminated for additional embodiments of the method. The order of the operations/processes may be interchangeable. The method M includes fabrication of the semiconductor die **100**. However, the fabrication of the semiconductor die **100** is merely an example for describing the manufacturing process according to some embodiments of the present disclosure.

[0054] FIGS. **5**A-**27**B illustrate the method M in various stages of forming the semiconductor die **100** in accordance with some embodiments of the present disclosure. FIGS. **5**A, **6**A, **7**A, **8**A, **9**A, **10**A, **11**A, **12**A, **13**A, **14**A, **15**A, **16**A, **17**A, **18**A, **19**A, **20**A, **21**A, **22**C, **23**A, **24**A, **25**A, **26**A, and **27**A illustrate perspective views of a portion of the semiconductor die of FIG. **1**A including the first

set of the computing three-dimensional memory devices indicated by the arrow A in FIG. **1**A, in accordance with some embodiments of the present disclosure. FIG. **22**A illustrates a top view of the computing three-dimensional memory devices of FIG. **22**C in accordance with some embodiments of the present disclosure. FIGS. **15**C, **21**C, **24**C, and **26**C illustrate cross-section view of the computing three-dimensional memory devices, taken along the line X-X in FIGS. **15**A, **21**A, **24**A, and **26**A, in accordance with some embodiments of the present disclosure. FIGS. **5**B, **6**B, **7**B, **8**B, **9**B, **10**B, **11**B, **12**B, **13**B, **14**B, **15**B, **16**B, **17**B, **18**B, **19**B, **20**B, **21**B, **22**D, **23**B, **24**B, **25**B, **26**B, and **27**B illustrate perspective views of a portion of the semiconductor die of FIG. **1**A including the second set of the storage three-dimensional memory devices indicated by the arrow B in FIG. **1**A, in accordance with some embodiments of the present disclosure. FIG. **22**B illustrates a top view of the storage three-dimensional memory devices of FIG. **22**D in accordance with some embodiments of the present disclosure. FIGS. **15**D, **21**D, **24**D, and **26**D illustrate cross-section view of the storage three-dimensional memory devices, taken along the line Y-Y in FIGS. **15**B, **21**B, **24**B, and **26**B, in accordance with some embodiments of the present disclosure.

[0055] The method M begins at block S**101** where an etch stop layer is formed over a computing memory region and a storage memory region of a substrate. Referring to FIGS. **5**A and **5**B, in some embodiments of block S**101**, the substrate **107** may be a semiconductor substrate, such as a bulk semiconductor, a semiconductor-on-insulator (SOI) substrate, or the like, which may be doped (e.g., with a p-type or an n-type impurity) or un-doped. The substrate **107** may be a wafer, such as a silicon wafer. Generally, a SOI substrate is a layer of a semiconductor material formed on an insulator layer. The insulator layer may be, for example, a buried oxide (BOX) layer, a silicon oxide layer, or the like. The insulator layer is provided on a substrate, typically a silicon or glass substrate. Other substrates, such as a multi-layered or gradient substrate may also be used. In some embodiments, the semiconductor material of the substrate **107** may include silicon; germanium; a compound semiconductor including silicon carbide, gallium arsenide, gallium phosphide, indium phosphide, indium arsenide, and/or indium antimonide; an alloy semiconductor including silicon germanium, gallium arsenide phosphide, aluminum indium arsenide, aluminum gallium arsenide, gallium indium arsenide, gallium indium phosphide, and/or gallium indium arsenide phosphide; combinations thereof; or the like. In some embodiments, the device spacer **113***a/b* be formed from an electrically insulating material (e.g., silicon oxide (SiO.sub.2), silicon nitride (SiN), silicon oxide (SiO), silicon carbide nitride (SiCN), silicon oxycarbonitride (SiOCN), silicon oxynitride (SiON), HfO.sub.2, TaO.sub.x, TiO.sub.x, AlO.sub.x, etc.). The substrate **107** may have a computing three-dimensional memory region T1 as shown in FIG. **5**A that will have the first semiconductor devices (e.g. AND memory device) to be formed thereon and a storage three-dimensional memory region T2 as shown in FIG. **5**B that will have the second semiconductor devices (e.g. NAND memory device) to be formed thereon.

[0056] In some embodiments, an etch stop layer **101** may be formed over the substrate **107** by using a plasma deposition process, for example, using PVD, CVD, LPCVD, PECVD, ALD, MBE, HARP, any other suitable process or a combination thereof. In some embodiments, the etch stop layer **101** may include SiN, SiO, SiO.sub.2, SiCN, SiOCN, SiON, HfO.sub.2, TaO.sub.x, TiO.sub.x, AlO.sub.x, a metal carbide, any other suitable material or combination thereof, and may include a single layer or various sublayers.

[0057] Subsequently, a patterned hard mask layer **105** may be formed on the etch stop layer **101**. The etch stop layer **101** may be etched through the patterned hard mask layer **105** to form trenches **101***t* as shown in FIG. **6**B therein. In some embodiments, the patterned hard mask layer **105** may be formed by patterning a hard mask material using a combination of photolithography and etching. For example, a hard mask material may be deposited over the etch stop layer **101** in the computing three-dimensional memory region T1 as shown in FIG. **5**A and the storage three-dimensional memory region T2 as shown in FIG. **5**B. The hard mask material can be formed by using, such as a spin-on technique. Subsequently, the hard mask material may be patterned to form the patterned

mask layer **105** to define the trenches **101***t* (see FIG. **6**B) on the etch stop layer **101** in the storage three-dimensional memory region T2. As shown in FIGS. **5**A and **5**B, the patterned hard mask layer **105** in the storage three-dimensional memory region T2 have a conductive line pattern, but the patterned hard mask layer **105** in the computing three-dimensional memory region T1 is free of the conductive line pattern. In other words, the etch stop layer **101** in the computing three-dimensional memory region T1 is entirely covered by a first side of the patterned hard mask layer **105** without having any conductive line pattern thereon, and the etch stop layer **101** in the storage three-dimensional memory region T2 is partially exposed through a second side of the patterned hard mask layer **105** with the conductive line pattern thereon.

[0058] Referring back to FIG. **4**A, the method M then proceeds to block S**102** where the etch top layer is etched to form first conductive line trenches in the storage memory region while remains the etch top layer in the computing memory region not to be etched. With reference to FIGS. **6**A and **6**B, in some embodiments of block S**102**, the etch stop layer **101** in the storage three-dimensional memory region T2 is etched through the second side of the patterned hard mask layer **105** with the conductive line pattern thereon as shown in FIG. **5**B to form the trenches **101***t* (see FIG. **6**B), but remains the etch top layer **101** in the computing three-dimensional memory region T1 not to be etched (see FIG. **6**A) and covered by the first side of the patterned hard mask layer **105** without the conductive line pattern thereon as shown in FIG. **5**A. A pattern of the conductive line trenches **101***t* may correspond to the conductive line pattern on the patterned hard mask layer **105**.

[0059] In some embodiments, the etching may be any acceptable etch process, such as by wet or dry etching, a reactive ion etch (RIE), neutral beam etch (NBE), the like, or a combination thereof. The etching may be anisotropic. The etching process may use an etchant that etches the etch stop layer **101** without significantly etching the patterned hard mask layer **105**. After the trenches **101***t* are formed, the patterned hard mask layer **105** is subsequently stripped, such as by wet stripping or plasma ashing.

[0060] Referring back to FIG. **4**A, the method M then proceeds to block S**103** where a reduced RC layer and a first conductive material are deposited over the etch stop layer and in the first conductive line trenches within the computing memory region and the storage memory region. With reference to FIGS. **7**A and **7**B, in some embodiments of block S**103**, a conductive material **119** is conformally formed over the etch stop layer **101** and in the conductive line trenches **101***t* within the computing three-dimensional memory region T1 and the storage three-dimensional memory region T2. In some embodiments, the conductive material **119** may include a conductive material, for example, metals such as Al, Ti, TiN, TaN, Co, Ag, Au, Cu, Ni, Cr, Hf, Ru, W, Pt, WN, any other suitable material or a combination or alloy thereof. In some embodiments, the conductive material **119** may include a semiconductor material, for example, an n or p-doped semiconductor such as Si, SiGe, or any other semiconductor material (e.g., IGZO, ITO, IZO, ZnO, IWO, poly silicon, amorphous Si, etc.), and may be formed using a deposition process, an epitaxial growth process, or any other suitable process. In some embodiments, the conductive material **119** may be formed by using, for example, CVD, ALD, PVD, PECVD, or the like.

[0061] Subsequently, a reduced parasitic RC layer **150***b* is deposited over the conductive material **119** within the computing three-dimensional memory region T1 and the storage three-dimensional memory region T2. In some embodiments, the reduced parasitic RC layer **150***b* may include a conductive material, for example, metals such as Al, Ti, TiN, TaN, Co, Ag, Au, Cu, Ni, Cr, Hf, Ru, W, Pt, WN, any other suitable material or a combination or alloy thereof. In some embodiments, the reduced parasitic RC layer **150***b* may include a semiconductor material, for example, an n or p-doped semiconductor such as Si, SiGe, or any other semiconductor material (e.g., IGZO, ITO, IZO, ZnO, IWO, poly silicon, amorphous Si, etc.). In some embodiments, the reduced parasitic RC layer **150***b* may be formed by using, for example, CVD, ALD, PVD, PECVD, or the like.

[0062] Referring back to FIG. **4**A, the method M then proceeds to block S**104** where a planarized

process is performed on the reduced parasitic RC layer and the first conductive material until the etch stop layer is exposed to form first conductive lines of storage memory devices electrically coupled to respective source lines within the storage memory region. With reference to FIGS. **8**A and **8**B, in some embodiments of block S**104**, a planarized process (e.g., a CMP, etch back, or the like) is performed to remove excess portions of the reduced parasitic RC layer **150***b* and the conductive material **119** over the etch stop layer **101** until the etch stop layer **101** is exposed. The remaining conductive lines **120***b* and the reduced parasitic RC layers **150***b* fill the trenches **101***t* in the etch stop layer **101** and form the reduced parasitic RC layer **150***b* and the conductive lines **120***b* cupped by the conductive line **120***b* as shown in FIG. **3**B that can be electrically coupled to respective global source lines. In some embodiments, the conductive lines **120***b* can be interchangeably referred to as conductive source lines. In some embodiments, the conductive lines **120***b* can be electrically coupled to respective global bit lines and can be interchangeably referred to as conductive bit lines.

[0063] Referring back to FIG. **4**A, the method M then proceeds to block S**105** where a multi-layered stack having insulating layers and spacer layers alternately stacked on top of each other in a vertical direction is formed over the etch stop layer within the computing memory region and the storage memory region. With reference to FIGS. **9**A and **9**B, in some embodiments of block S**105**, a multi-layered stack **108** is formed over the etch stop layer **101** within the computing three-dimensional memory region T1 as shown in FIG. **9**A and the storage three-dimensional memory region T2 as shown in FIG. **9**B. The multi-layered stack **108** includes a plurality of insulating layers **112** and a plurality of spacer layers **111** alternately stacked on top of each other in the vertical direction (e.g., the Z-direction). For example, one of the spacer layers **111** is disposed over one of the insulating layers **112**, and then another one of the insulating layers **112** is disposed on the spacer layer **111**, so on and so forth. As shown in FIGS. **9**A and **9**B, a topmost layer (e.g., a layer distal most from the substrate **107**) and/or a bottommost layer (e.g., a layer most proximate to the substrate **107**) of the multi-layered stack **108** may be an insulating layer **112**. While FIGS. **9**A and **9**B show the multi-layered stack **108** as including five insulating layers **112** and four spacer layers **111**, the multi-layered stack **108** may include any number of insulating layers **112** and spacer layers **111** (e.g., 4, 5, 6, 7, 8, 16, 24, 48, 64, 128, or even more). In some embodiments, if the number of spacer layers **111** in the multi-layered stack **108** is n, a number of insulating layers **112** in the multi-layered stack **108** may be n+1, wherein n is an integral greater than or equal to one.

[0064] In some embodiments, each of the plurality of insulating layers **112** may have about the same thickness, for example, in a range of about 5 nm to about 100 nm, inclusive. Moreover, the spacer layers **111** may have the same thickness or different thickness from the insulating layers **112**. The thickness of the spacer layers **111** may range from a few nanometers to few tens of nanometers (e.g., in a range of 5 nm to 100 nm, inclusive, but other ranges and values are also contemplated and are within the scope of this disclosure). In some embodiments, a topmost spacer layer **111** and/or a bottom most spacer layer **111** may be thicker (e.g., 1.2×, 1.4×, 1.6×, 1.8×, 2×, 2.5×, or 3× thicker) than the other spacer layers **111** disposed therebetween.

[0065] The insulating layers **112** and the spacer layers **111** have different compositions. In some embodiments, the insulating layers **112** and the spacer layers **111** have compositions that provide for different oxidation rates and/or different etch selectivity between the respective layers. In some embodiments, the insulating layers **112** may be formed from silicon oxide (SiO.sub.x), and the spacer layers **111** may be formed from silicon nitride (SiN). In some embodiments, the insulating layers **112** may be formed from any suitable first material (e.g., an insulating material) as described with respect to the semiconductor die **100**, and the spacer layers **111** may be formed from a second material (e.g., also an insulating material) that is different from the first material. In some embodiments, the spacer layers may **111** include SiN, HfO.sub.2, TaO.sub.x, TiO.sub.x, AlO.sub.x, or any other material that has a high etch selectivity relative to the insulating layers **112** (e.g., an etch selectivity ratio of at least 1:100).

[0066] In some embodiments, the insulating layers **112** and/or the spacer layers **111** may be epitaxially grown from the substrate **107**. For example, each of the insulating layers **112** and the spacer layers **111** may be grown by a MBE process, a CVD process such as a metal organic CVD (MOCVD) process, a furnace CVD process, and/or other suitable epitaxial growth processes. In some embodiments, the insulating layers **112** and the spacer layers **111** may be grown using an atomic layer deposition (ALD) process.

[0067] Referring back to FIG. **4**A, the method M then proceeds to block S**106** where a plurality of first trenches are formed through the multi-layered stack within the computing memory region to form a plurality of first stacked structures while remains the multi-layered stack within the computing memory region not to be etched. With reference to FIGS. **10**A and **10**B, in some embodiments of block S**106**, a plurality of first trenches **132***a* extending in the first direction (e.g., the X-direction) are formed through the multi-layered stack **108** within the computing three-dimensional memory region T1 from the topmost insulating layer **112** to the etch stop layer **101** to form stacked structures **108***a*, while remains the multi-layered stack **108** within the storage three-dimensional memory region T2 not to be etched.

[0068] A patterned hard mask layer **138** may be formed on the multi-layered stack **108**. In some embodiments, the patterned hard mask layer **138** may be formed by patterning a hard mask material using a combination of photolithography and etching. For example, a hard mask material may be deposited over the multi-layered stack **108** in a computing three-dimensional memory region T1 as shown in FIG. **10**A and a storage three-dimensional memory region T2 as shown in FIG. **10**B. The hard mask material can be formed by using, such as a spin-on technique. Subsequently, the hard mask material may be patterned to form the patterned mask layer **138** to define the first trenches **132***a* (see FIG. **10**A) on the multi-layered stack **108** in the computing three-dimensional memory region T1. As shown in FIGS. **10**A and **10**B, the patterned hard mask layer **138** in the computing three-dimensional memory region T1 has a strip pattern, but the patterned hard mask layer **138** in the storage three-dimensional memory region T2 is free of the strip pattern. In other words, the multi-layered stack **108** in the computing three-dimensional memory region T1 is partially exposed through a first side of the patterned hard mask layer **138** with the strip pattern thereon, and the multi-layered stack **108** in the storage three-dimensional memory region T2 is entirely covered by a second side of the patterned hard mask layer **138** without having any strip pattern thereon.

[0069] Subsequently, the multi-layered stack **108** in the computing three-dimensional memory region T1 is etched through the first side of the patterned hard mask layer **138** with the strip pattern thereon to form the first trenches **132***a* (see FIG. **10**A), but remains the multi-layered stack **108** in the storage three-dimensional memory region T2 covered by the second side of the patterned hard mask layer **138** without the strip pattern thereon and not to be etched (see FIG. **10**B). A pattern of the first trenches **132***a* may correspond to the strip pattern on the patterned hard mask layer **138**. In some embodiments, the multi-layered stack **108** may be etched using a plasma etching process (including radical plasma etching, remote plasma etching, and other suitable plasma etching processes, RIE, DRIE), gas sources such as Cl.sub.2, HBr, CF.sub.4, CHF.sub.3, CH.sub.2F.sub.2, CH.sub.3F, C.sub.4F.sub.6, BCl.sub.3, SF.sub.6, H.sub.2, NF.sub.3, and other suitable etch gas sources and combinations thereof can be used with passivation gases such as N.sub.2, O.sub.2, CO.sub.2, SO.sub.2, CO, CH.sub.4, SiCl.sub.4, and other suitable passivation gases and combinations thereof. Moreover, for the plasma etching process, the gas sources and/or the passivation gases can be diluted with gases such as Ar, He, Ne, and other suitable dilutive gases and combinations thereof to form the first trenches **132***a*. As a non-limiting example, a source power of 10 Watts to 3,000 Watts, a bias power of 0 watts to 3,000 watts, a pressure of 1 millitorr to 5 torr, and an etch gas flow of 0 sccm to 5,000 sccm may be used in the etching process. However, it is noted that source powers, bias powers, pressures, and flow rates outside of these ranges are also contemplated. In some embodiments, after the first trenches **132***a* are formed, the patterned hard mask layer **138** is subsequently stripped, such as by wet stripping or plasma ashing.

[0070] Referring back to FIG. **4**A, the method M then proceeds to block S**107** where exposed surfaces of the spacer layers within the first trenches are partially etched so as to reduce widths of the spacer layers relative to the insulating layers to form first cavities in the first stacked structures. With reference to FIGS. **11**A and **11**B, in some embodiments of block S**107**, exposed surfaces of the spacer layers **111** extending along the X-direction within the first trenches **132***a* are partially etched so as to reduce widths of the spacer layers relative to the insulating layers **112** in the Y-direction on either side of the spacer layers **111**, such that cavities **117***a* in the stacked structures **108***a* are formed whose boundaries are formed by top and bottom surfaces of adjacent insulating layers **112** and a surface of the partially etched spacer layers **111** that face the first trenches **132***a* and extend along the X-direction.

[0071] In some embodiments, the spacer layers **111** may be etched using a wet etch process (e.g., hydrofluoric etch, buffered hydrofluoric acid, phosphoric acid, etc.). In some embodiments, the exposed surfaces of the spacer layers **111** may be partially etched using a plasma etching process (including radical plasma etching, remote plasma etching, and other suitable plasma etching processes, RIE, DRIE), gas sources such as Cl.sub.2, HBr, CF.sub.4, CHF.sub.3, CH.sub.2F.sub.2, CH.sub.3F, C.sub.4F.sub.6, BCl.sub.3, SF.sub.6, H.sub.2, NF.sub.3, and other suitable etch gas sources and combinations thereof can be used with passivation gases such as N.sub.2, O.sub.2, CO.sub.2, SO.sub.2, CO, CH.sub.4, SiCl.sub.4, and other suitable passivation gases and combinations thereof. Moreover, for the plasma etching process, the gas sources and/or the passivation gases can be diluted with gases such as Ar, He, Ne, and other suitable dilutive gases and combinations thereof. As a non-limiting example, a source power of 10 Watts to 3,000 Watts, a bias power of 0 watts to 3,000 watts, a pressure of 1 millitorr to 5 torr, and an etch gas flow of 0 sccm to 5,000 sccm may be used in the etching process. However, it is noted that source powers, bias powers, pressures, and flow rates outside of these ranges are also contemplated.

[0072] Referring back to FIG. **4**A, the method M then proceeds to block S**108** where a plurality of first gate layers are formed in the first cavities of the first stacked structure. With reference to FIGS. **12**A and **12**B, in some embodiments of block S**108**, a first gate metal layer may be deposited over the computing three-dimensional memory region T1 and the storage three-dimensional memory region T2. Subsequently, an etching back process is performed on the first gate metal layer to form first gate layers **124***a* in the cavities **117***a*. This is described in greater detail with reference to FIGS. **12**A and **12**B, the gate metal layer may be etched back to expose sidewalls of the first insulating layers **112***a* within the first trenches **132***a* (see FIG. **12**A) and a topmost surface of the stacked structures **108***a* within the computing three-dimensional memory region T1 and a topmost surface of the multi-layered stack **108** in the storage three-dimensional memory region T2 (see FIGS. **12**A and **12**B). Therefore, the remaining first gate metal layer fills the cavities **117***a* in the stacked structures **108***a* and serves as the first gate layer **124***a* as shown in FIG. **12**A. In other words, the first gate layers **124***a* may be covered by sidewalls of the spacer layers **111***a* and top and/or bottom surfaces of the insulating layers **112***b*. Although, each of the first gate layers **124***a* shown in FIG. **12**A is shown as a single layer. In some embodiments, each of the first gate layers **124***a* can be formed as a multi-layer stack (e.g., including a first gate dielectric layer and a first gate metal layer).

[0073] The etch back of the first gate metal layer to form the first gate layers **124***a* may be performed with an acceptable process such as a wet etch or a dry etch. In some embodiments, the first gate metal layer may be etched back with a wet etch using KOH, NH.sub.4OH, H.sub.2O.sub.2, the like, or a combination thereof. In some embodiments, the first gate metal layer may be recessed with a dry etch using NH.sub.3, NF.sub.3, HF, the like, or a combination thereof. In some embodiments, a planarization such as a CM P is performed to remove excess portions of the first gate metal layer remaining over the topmost surface of the stacked structures **108***a* within the computing three-dimensional memory region T1 and the topmost surface of the multi-layered stack **108** in the storage three-dimensional memory region T2.

[0074] In some embodiments, the first gate layer **124***a* may include a stack of multiple metal materials. In some embodiments, the first gate layer **124***a* may include a p-type workfunction layer, an n-type workfunction layer, multi-layers thereof, or combinations thereof. The workfunction layer may also be referred to as a workfunction metal. Example p-type workfunction metals that may include TiN, TaN, Ru, Mo, Al, WN, ZrSi.sub.2, MoSi.sub.2, TaSi.sub.2, NiSi.sub.2, WN, other suitable p-type workfunction materials, or combinations thereof. Example n-type workfunction metals that may include Ti, Ag, TaAl, TaAlC, TiAlN, TaC, TaCN, TaSiN, Mn, Zr, other suitable n-type workfunction materials, or combinations thereof. A workfunction value is associated with the material composition of the workfunction layer, and thus, the material of the workfunction layer is chosen to tune its workfunction value so that a target threshold voltage V.sub.t is achieved in the device that is to be formed. The first gate metal layer may be deposited by CVD, PVD, ALD, and/or other suitable process.

[0075] Referring back to FIG. **4**A, the method M then proceeds to block S**109** where a first memory material and a first channel material are conformally formed over the computing memory region and the storage memory region. With reference to FIGS. **13**A and **13**B, in some embodiments of block S**109**, a first memory material **134** may be conformally formed over the computing three-dimensional memory region T1 and the storage three-dimensional memory region T2. Subsequently, a first channel material **136** may be conformally formed over the first memory material **134**.

[0076] In some embodiments, the first memory material **134** may include a ferroelectric material, for example, lead zirconate titanate (PZT), PbZr/TiO.sub.3, BaTiO.sub.3, PbTiO.sub.2, HfO.sub.2, Hr.sub.1-xZr.sub.xO.sub.2, ZrO.sub.2, TiO.sub.2, NiO, TaO.sub.x, Cu.sub.2O, Nb.sub.2O.sub.5, AlO.sub.x, etc. The first memory material **134** may be formed using PVD, CVD, LPCVD, PECVD, ALD, MBE, any other suitable process or a combination thereof. A conformal coating may be deposited such that the first memory material **134** is continuous on the walls of the first trenches **132***a*. In some embodiments, the first channel material **136** may be formed from a semiconductor material, for example, Si (e.g., polysilicon or amorphous silicon), Ge, SiGe, silicon carbide (SiC), IGZO, ITO, ZnO, IWO, etc. and can be an n-type or p-type doped semiconductor. The first channel material **136** may be formed using PVD, CVD, LPCVD, PECVD, ALD, MBE, any other suitable process or a combination thereof. A conformal coating may be deposited such that the first channel material **136** is continuous on the first trenches **132***a*.

[0077] Referring back to FIG. **4**B, the method M then proceeds to block S**110** where the first memory material and the first channel material are patterned to form a plurality of first memory layers and a plurality of first channel layers on sidewalls of the first trenches within the computing memory region. With reference to FIGS. **14**A and **14**B, in some embodiments of block S**110**, the first memory material **134** and the first channel material **136** are patterned to form a plurality of first memory layers **114***a* and a plurality of first channel layers **116***a* on sidewalls of the first trenches **132***a* within the computing three-dimensional memory region T1. This is described in greater detail with reference to FIGS. **14**A and **14**B, an etching process is performed to remove lateral portions of the first memory material **134** and the first channel material **136** as shown in FIGS. **12**A and **12**B such that the topmost surface of the first stacked structures **108** within the computing three-dimensional memory region T1 and the topmost surface of the multi-layered stack **108** in the storage three-dimensional memory region T2 are exposed, and remain vertical portions of the first memory material **134** and the first channel material **136** on the sidewalls of the first trenches **132***a* within the computing three-dimensional memory region T1 to form the first memory layers **114***a* and the first channel layers **116***a*. Therefore, the first channel material **136** is broken to form first memory layers **114***a* lining opposite sidewalls in the trenches **132***a* which in turn prevents short-circuiting from occurring between conductive lines **120***a* and **122***a* (see FIG. **23**A) that will be formed in subsequent steps.

[0078] The etching process may be, for example, an anisotropic etching process. The etching

process may include a single step or multiple steps. In some embodiments, the etching process is a dry etching process. By way of example and not limitation, a dry etching process may implement an oxygen-containing gas, a fluorine-containing gas (e.g., CF.sub.4, SF.sub.6, CH.sub.2F.sub.2, CHF.sub.3, and/or C.sub.4F.sub.6, C.sub.4F.sub.8), a chlorine-containing gas (e.g., Cl.sub.2, CHCl.sub.3, CCl.sub.4, and/or BCl.sub.3), a bromine-containing gas (e.g., HBr and/or CHBr.sub.3), an iodine-containing gas, other suitable gases and/or plasmas, and/or combinations thereof.

[0079] Referring back to FIG. **4**B, the method M then proceeds to block S**111** where a plurality of first inner spacers are formed to fill the first trenches within the computing memory region. With reference to FIGS. **15**A-**15**D, in some embodiments of block S**111**, the first inner spacers **118***a* are formed to fill the first trenches **132***a* within the computing three-dimensional memory region T1. An exemplary method of forming the first inner spacers **118***a* may include depositing a first insulating material over the computing three-dimensional memory region T1 and the storage three-dimensional memory region T2 and fills in the first trenches **132***a*. Subsequently, a CM P process is performed to remove excessive insulating material outside the first trenches **132***a* until the topmost surface of the first stacked structures **108** within the computing three-dimensional memory region T1 and the topmost surface of the multi-layered stack **108** in the storage three-dimensional memory region T2 are exposed, and a remainder of the insulating material in the first trenches **132***a* serves as the first inner spacers **118***a*. The insulating material may be deposited in the first trenches **132***a* to form the first isolation layers **140***a* using any suitable method, for example, MBD, ALD, CVD, PECVD, MOCVD, epitaxial growth, and the like. The first inner spacers **118***a* may include SiO.sub.2, SiON, SiN, SiCN, HfO.sub.2, TaO.sub.x, TiO.sub.x, AlO.sub.x, etc. In some embodiments, the first inner spacers **118***a* may be formed from the same material of the first insulating layers **112***a*.

[0080] Referring back to FIG. **4**B, the method M then proceeds to block S**112** where a plurality of second trenches are formed through the stack within the storage memory region to form a plurality of second stacked structures while remains the first stacked structure, the first memory layers, the first channel layers, and the first inner spacers within the computing memory region not to be etched. With reference to FIGS. **16**A and **16**B, in some embodiments of block S**112**, a plurality of second trenches **132***b* extending in the first direction (e.g., the X-direction) are formed through the multi-layered stack **108** within the storage three-dimensional memory region T2 from the topmost insulating layer **112** to the etch stop layer **101** to form second stacked structures **108***b* while remains the stacked structure **108***a* within the computing three-dimensional memory region T1 not to be etched.

[0081] A patterned hard mask layer **148** may be formed on the computing three-dimensional memory region T1 and the storage three-dimensional memory region T2. In some embodiments, the patterned hard mask layer **148** may be formed by patterning a hard mask material using a combination of photolithography and etching. For example, a hard mask material may be deposited over the storage three-dimensional memory region T1 as shown in FIG. **16**A and the storage three-dimensional memory region T2 as shown in FIG. **16**B. The hard mask material can be formed by using, such as a spin-on technique. Subsequently, the hard mask material may be patterned to form the patterned mask layer **148** to define the second trenches **132***b* (see FIG. **16**B) on the multi-layered stack **108** in the storage three-dimensional memory region T2. As shown in FIGS. **16**A and **16**B, the patterned hard mask layer **148** in the storage three-dimensional memory region T2 has a strip pattern, but the patterned hard mask layer **148** in the computing three-dimensional memory region T1 is free of the strip pattern. In other words, the stacked structure **108***a* in the computing three-dimensional memory region T1 is entirely covered by a first side of the patterned hard mask layer **148** without having any strip pattern thereon, and the multi-layered stack **108** in the storage three-dimensional memory region T2 is partially exposed through a second side of the patterned hard mask layer **148** with the strip pattern thereon.

[0082] Subsequently, the multi-layered stack **108** in the storage three-dimensional memory region T2 is etched through the second side of the patterned hard mask layer **148** with the strip pattern thereon to form the second trenches **132***b* to form second stacked structures **108***b* (see FIG. **16**A), but remains the stacked structure **108***a* in the computing three-dimensional memory region T1 not to be etched (see FIG. **10**B) and covered by the first side of the patterned hard mask layer **148** without the strip pattern thereon. A pattern of the second trenches **132***b* may correspond to the strip pattern on the patterned hard mask layer **148**. In some embodiments, the multi-layered stack **108** may be etched using a plasma etching process (including radical plasma etching, remote plasma etching, and other suitable plasma etching processes, RIE, DRIE), gas sources such as Cl.sub.2, HBr, CF.sub.4, CHF.sub.3, CH.sub.2F.sub.2, CH.sub.3F, C.sub.4F.sub.6, BCl.sub.3, SF.sub.6, H.sub.2, NF.sub.3, and other suitable etch gas sources and combinations thereof can be used with passivation gases such as N.sub.2, O.sub.2, CO.sub.2, SO.sub.2, CO, CH.sub.4, SiCl.sub.4, and other suitable passivation gases and combinations thereof. Moreover, for the plasma etching process, the gas sources and/or the passivation gases can be diluted with gases such as Ar, He, Ne, and other suitable dilutive gases and combinations thereof to form the second trenches **132***b*. As a non-limiting example, a source power of 10 Watts to 3,000 Watts, a bias power of 0 watts to 3,000 watts, a pressure of 1 millitorr to 5 torr, and an etch gas flow of 0 sccm to 5,000 sccm may be used in the etching process. However, it is noted that source powers, bias powers, pressures, and flow rates outside of these ranges are also contemplated. In some embodiments, after the second trenches **132***b* are formed, the patterned hard mask layer **148** is subsequently stripped, such as by wet stripping or plasma ashing.

[0083] Referring back to FIG. **4**B, the method M then proceeds to block S**113** where exposed surfaces of the spacer layers within the second trenches are partially etched so as to reduce widths of the spacer layers relative to the insulating layers to form second cavities in the second stacked structures. With reference to FIGS. **17**A and **17**B, in some embodiments of block S**113**, exposed surfaces of the spacer layers **111** extending along the X-direction within the first trenches **132***b* are partially etched so as to reduce widths of the spacer layers relative to the insulating layers **112** in the Y-direction on either side of the spacer layers **111**, such that cavities **117***b* in the second stacked structures **108***b* are formed whose boundaries are formed by top and bottom surfaces of adjacent insulating layers **112** and a surface of the partially etched spacer layers **111** that face the first trenches **132***b* and extend along the X-direction.

[0084] In some embodiments, the spacer layers **111** may be etched using a wet etch process (e.g., hydrofluoric etch, buffered hydrofluoric acid, phosphoric acid, etc.). In some embodiments, the exposed surfaces of the spacer layers **111** may be partially etched using a plasma etching process (including radical plasma etching, remote plasma etching, and other suitable plasma etching processes, RIE, DRIE), gas sources such as Cl.sub.2, HBr, CF.sub.4, CHF.sub.3, CH.sub.2F.sub.2, CH.sub.3F, C.sub.4F.sub.6, BCl.sub.3, SF.sub.6, H.sub.2, NF.sub.3, and other suitable etch gas sources and combinations thereof can be used with passivation gases such as N.sub.2, O.sub.2, CO.sub.2, SO.sub.2, CO, CH.sub.4, SiCl.sub.4, and other suitable passivation gases and combinations thereof. Moreover, for the plasma etching process, the gas sources and/or the passivation gases can be diluted with gases such as Ar, He, Ne, and other suitable dilutive gases and combinations thereof. As a non-limiting example, a source power of 10 Watts to 3,000 Watts, a bias power of 0 watts to 3,000 watts, a pressure of 1 millitorr to 5 torr, and an etch gas flow of 0 sccm to 5,000 sccm may be used in the etching process. However, it is noted that source powers, bias powers, pressures, and flow rates outside of these ranges are also contemplated.

[0085] Referring back to FIG. **4**B, the method M then proceeds to block S**114** where a plurality of second gate layers are formed in the second cavities of the second stacked structures. With reference to FIGS. **18**A and **18**B, in some embodiments of block S**114**, a second gate metal layer may be deposited over the computing three-dimensional memory region T1 and the storage three-dimensional memory region T2. Subsequently, an etching back process may be performed on the

second gate metal layer to form second gate layers **124***b* in the cavities **117***b* of the second stacked structures **108***b*. This is described in greater detail with reference to FIGS. **18**A and **18**B, the second gate metal layer may be etched back to expose sidewalls of the second insulating layers **112***b* within the second trenches **132***b* (see FIG. **18**A) and a topmost surface of the stacked structure **108***a* and **108***b* within the computing three-dimensional memory region T1 and the storage three-dimensional memory region T2 (see FIGS. **18**A and **18**B). Therefore, the remaining second gate metal layer fills the cavities **117***b* in the second stacked structures **108***b* and serves as the second gate layer **124***b* as shown in FIG. **16**A. In other words, the second gate layers **124***b* may be covered by sidewalls of the spacer layers **111***b* and top and/or bottom surfaces of the insulating layers **112***b*. Although, each of the second gate layers **124***b* shown in FIG. **16**A is shown as a single layer, In some embodiments, each of the second gate layers **124***b* can be formed as a multi-layer stack (e.g., including a second gate dielectric layer and a second gate metal layer), while remaining within the scope of the present disclosure.

[0086] The etch back of the second gate metal layer to form the first gate layers **124***b* may be performed with an acceptable process such as a wet etch or a dry etch. In some embodiments, the second gate metal layer may be etched back with a wet etch using KOH, NH.sub.4OH, H.sub.2O.sub.2, the like, or a combination thereof. In some embodiments, the second gate metal layer may be recessed with a dry etch using NH.sub.3, NF.sub.3, HF, the like, or a combination thereof. In some embodiments, a planarization such as a CMP is performed to remove excess portions of the second gate metal layer remaining over top surfaces of the stacked structures **108***a* and **108***b*.

[0087] In some embodiments, the second gate layer **124***b* may include a stack of multiple metal materials. In some embodiments, the second gate layer **124***b* may include a p-type workfunction layer, an n-type workfunction layer, multi-layers thereof, or combinations thereof. The workfunction layer may also be referred to as a workfunction metal. Example p-type workfunction metals that may include TiN, TaN, Ru, Mo, Al, WN, ZrSi.sub.2, MoSi.sub.2, TaSi.sub.2, NiSi.sub.2, WN, other suitable p-type workfunction materials, or combinations thereof. Example n-type workfunction metals that may include Ti, Ag, TaAl, TaAlC, TiAlN, TaC, TaCN, TaSiN, Mn, Zr, other suitable n-type workfunction materials, or combinations thereof. A workfunction value is associated with the material composition of the workfunction layer, and thus, the material of the workfunction layer is chosen to tune its workfunction value so that a target threshold voltage V.sub.t is achieved in the device that is to be formed. The second gate metal layer may be deposited by CVD, PVD, ALD, and/or other suitable process.

[0088] Referring back to FIG. **4**B, the method M then proceeds to block S**115** where a second memory material is conformally formed over the computing memory region and the storage memory region. With reference to FIGS. **19**A and **19**B, in some embodiments of block S**115**, a second memory material **144** may be conformally formed over the computing three-dimensional memory region T1 and the storage three-dimensional memory region T2. In some embodiments, the second memory material **144** may include a ferroelectric material, for example, lead zirconate titanate (PZT), PbZr/TiO.sub.3, BaTiO.sub.3, PbTiO.sub.2, HfO.sub.2, Hr.sub.1-xZr.sub.xO.sub.2, ZrO.sub.2, TiO.sub.2, NiO, TaO.sub.x, Cu.sub.2O, Nb.sub.2O.sub.5, AlO.sub.x, etc. The second memory material **144** may be formed using PVD, CVD, LPCVD, PECVD, ALD, MBE, any other suitable process or a combination thereof. A conformal coating may be deposited such that the second memory material **144** is continuous on the walls of the second trenches **132***b*. In some embodiments, the second memory material **144** within the storage three-dimensional memory region T2 may have a same material as the first memory material **134** within the storage three-dimensional memory region T1. In some embodiments, the second memory material **144** within the storage three-dimensional memory region T2 may have a different material than the memory layer **114***a* within the storage three-dimensional memory region T1.

[0089] Referring back to FIG. **4**B, the method M then proceeds to block S**116** where the second

memory material is patterned to form a plurality of second memory layers on sidewalls of the second trenches within the storage memory region. With reference to FIGS. **20**A and **20**B, in some embodiments of block S**116**, the second channel material **146** are patterned to form a plurality of second channel layers **116***b* on sidewalls of the second trenches **132***b* within the storage three-dimensional memory region T2. This is described in greater detail with reference to FIGS. **20**A and **20**B, an etching process is performed to remove lateral portions of the second memory material **144** as shown in FIGS. **20**A and **20**B such that the topmost surfaces of the stacked structures **108***a* and **108***b* within the computing three-dimensional memory region T1 and the storage three-dimensional memory region T2 are exposed, and remain vertical portions of the second memory material **144** on the sidewalls of the first trenches **132***b* within the storage three-dimensional memory region T2 to form the second memory layers **114***b*.

[0090] The etching process may be, for example, an anisotropic etching process. The etching process may include a single step or multiple steps. In some embodiments, the etching process is a dry etching process. By way of example and not limitation, a dry etching process may implement an oxygen-containing gas, a fluorine-containing gas (e.g., CF.sub.4, SF.sub.6, CH.sub.2F.sub.2, CHF.sub.3, and/or C.sub.4F.sub.6, C.sub.4F.sub.8), a chlorine-containing gas (e.g., Cl.sub.2, CHCl.sub.3, CCl.sub.4, and/or BCl.sub.3), a bromine-containing gas (e.g., HBr and/or CHBr.sub.3), an iodine-containing gas, other suitable gases and/or plasmas, and/or combinations thereof.

[0091] Referring back to FIG. **4**B, the method M then proceeds to block S**117** where a plurality of second channel layers and a plurality of second inner spacers are formed in the second trenches and over the second memory layers within the storage memory region. With reference to FIGS. **21**A-**21**D, in some embodiments of block S**117**, second channel layers **116***b* and second inner spacers **118***b* are formed in the second trenches **132***b* within the storage three-dimensional memory region T2. An exemplary method of forming the second channel layers **116***b* and second inner spacers **118***b* may include conformally depositing a second channel material over the computing three-dimensional memory region T1 and the storage three-dimensional memory region T2, and depositing a second insulating material over the second channel material and fills in the second trenches **132***b*. Subsequently, a CM P process is performed to remove excessive second channel material and insulating material outside the second trenches **132***b* until the topmost surface of the stacked structures **108***a* and **108***b* within the computing three-dimensional memory region T1 and the storage three-dimensional memory region T2 are exposed, and remainders of the second channel material and insulating material in the second trenches **132***b* serve as the second channel layers **116***b* and the second inner spacers **118***b*. As shown in FIG. **21**D, the second channel layer **116***b* has a U-shaped cross section and in contact with the conductive line **120***b*.

[0092] In some embodiments, the second channel layer **116***b* may be formed from a semiconductor material, for example, Si (e.g., polysilicon or amorphous silicon), Ge, SiGe, silicon carbide (SiC), IGZO, ITO, ZnO, IWO, etc. and can be an n-type or p-type doped semiconductor. The second channel layer **116***b* may be formed using PVD, CVD, LPCVD, PECVD, ALD, MBE, any other suitable process or a combination thereof. A conformal coating may be deposited such that the second channel layer **116***b* is continuous on the second trenches **132***b*. In some embodiments, the second channel layer **116***b* within the storage three-dimensional memory region T2 may have a same material as the first channel layer **116***a* within the storage three-dimensional memory region T1. In some embodiments, the second channel layer **116***b* within the storage three-dimensional memory region T2 may have a different material than the first channel layer **116***a* within the storage three-dimensional memory region T1. The second insulating material may be deposited in the second trenches **132***b* to form the second inner spacers **118***b* using any suitable method, for example, MBD, ALD, CVD, PECVD, MOCVD, epitaxial growth, and the second like. The inner spacers **118***b* may include SiO.sub.2, SiON, SiN, SiCN, HfO.sub.2, TaO.sub.x, TiO.sub.x, AlO.sub.x, etc. In some embodiments, the second inner spacers **118***b* may be formed from the same

material of the second insulating layers **112***b*.

[0093] Referring back to FIG. **4**B, the method M then proceeds to block S**118** where the first and second channel layers and the first and second inner spacers within the computing memory region and the storage memory region are etched and cut into multiple discrete sections while remains the first and second memory layers not to be etched. With reference to FIGS. **22**A-**22**D, in some embodiments of block S**118**, the first channel layers **116***a* and the first inner spacers **118***a* within the computing three-dimensional memory region T1 are etched from the top surface of the stacked structure **108***a* down to the etch stop layer **101** to form cavities **128***a* and cut into multiple sections. The second channel layers **116***b* and the second inner spacers **118***b* within the storage three-dimensional memory region T2 are etched from the stacked structure **108***b* down to the etch stop layer **101** to form cavities **128***b* and cut into multiple sections. The remaining first channel layers **116***a* within the computing three-dimensional memory region T1 are co-extensive with the remaining first inner spacers **118***a*, and the remaining second channel layers **116***b* within the storage three-dimensional memory region T2 are co-extensive with the remaining second inner spacers **118***b*.

[0094] In some embodiments, the first and second channel layers **116***a* and **116***b* and the first and second inner spacers **118***a* and **118***b* may be etched simultaneously or sequentially, using a dry etch, for example, a plasma etching process (including radical plasma etching, remote plasma etching, and other suitable plasma etching processes, RIE, DRIE), gas sources such as Cl.sub.2, HBr, CF.sub.4, CHF.sub.3, CH.sub.2F.sub.2, CH.sub.3F, C.sub.4F.sub.6, BCl.sub.3, SF.sub.6, H.sub.2, NF.sub.3, and other suitable etch gas sources and combinations thereof can be used with passivation gases such as N.sub.2, O.sub.2, CO.sub.2, SO.sub.2, CO, CH.sub.4, SiCl.sub.4, and other suitable passivation gases and combinations thereof. Moreover, for the plasma etching process, the gas sources and/or the passivation gases can be diluted with gases such as Ar, He, Ne, and other suitable dilutive gases and combinations thereof. As a non-limiting example, a source power of 10 Watts to 3,000 Watts, a bias power of 0 watts to 3,000 watts, a pressure of 1 millitorr to 5 torr, and an etch gas flow of 0 sccm to 5,000 sccm may be used in the etching process.

[0095] Referring back to FIG. **4**C, the method M then proceeds to block S**119** where a plurality of first device spacers are formed to interpose between the discrete first channel layers and between the discrete first inner spacers and a plurality of second device spacers are formed to interpose between the discrete second channel layers and between the discrete second inner spacers. With reference to FIGS. **22**A-**22**D, in some embodiments of block S**119**, first device spacers **113***a* are formed to interpose between the discrete first channel layers **116***a* and between the discrete first inner spacers **118***a* and second device spacers **113***b* are formed to interpose between the discrete second channel layers **116***b* and between the discrete second inner spacers **118***b*. The first device spacers **113***a* disposed at regular intervals separating adjacent semiconductor devices **110***a* that will be formed in subsequent steps in the semiconductor die **100** within the computing three-dimensional memory region T1. The second device spacers **113***b* disposed at regular intervals separating adjacent semiconductor devices **110***b* that will be formed in subsequent steps in the semiconductor die **100** within the storage three-dimensional memory region T2.

[0096] An exemplary method of forming the first and second device spacers **113***a* and **113***b* may include depositing an insulating material over the stacked structures **108***a* and **108***b* within the computing three-dimensional memory region T1 and the storage three-dimensional memory region T2 to fill the cavities **128***a* and **128***b*. In some embodiments, the insulating material may be formed by using, for example, MBD, ALD, CVD, PECVD, MOCVD, epitaxial growth, and the like. Subsequently, a planarized process (e.g., a CMP, etch back, or the like) is performed to remove excess portions of the insulating material over the stacked structures **108***a* and **108***b* until the stacked structures **108***a* and **108***b* are exposed. The remaining insulating material filling the cavities **128***a* and **128***b* can be served as the first and second device spacers **113***a* and **113***b*. In some embodiments, the first and/or second device spacers **113***a* and/or **113***b* may be made of an

electrically insulating material, for example, silicon nitride (SiN), silicon oxide (SiO), SiO.sub.2, silicon carbide nitride (SiCN), silicon oxycarbonitride (SiOCN), silicon oxynitride (SiON), HfO.sub.2, TaO.sub.x, TiO.sub.x, AlO.sub.x, etc.

[0097] Referring back to FIG. **4**C, the method M then proceeds to block S**120** where a plurality of second and third conductive line trenches are formed through the first inner spacers within the computing memory region. With reference to FIGS. **23**A and **23**B, in some embodiments of block S**120**, a plurality of conductive line trenches **118***c* and **118***d* are formed through the first inner spacers **118***a* within the computing three-dimensional memory region T1 from the top surface of the stacked structure **108***a* to the etch stop layer **101** for forming a conductive line **120***a* and a conductive line **122***a* (see FIGS. **24**A and **24**C) that will be formed in subsequent steps in the semiconductor die **100** while remains the storage three-dimensional memory region T2 not to be etched.

[0098] A patterned hard mask layer **158** may be formed over the computing three-dimensional memory region T1 as shown in FIG. **23**A and over the storage three-dimensional memory region T2 as shown in FIG. **23**B. In some embodiments, the patterned hard mask layer **158** may be formed by patterning a hard mask material using a combination of photolithography and etching. For example, a hard mask material may be deposited over the computing three-dimensional memory region T1 and the storage three-dimensional memory region T2. The hard mask material can be formed by using, such as a spin-on technique. Subsequently, the hard mask material may be patterned to form the patterned mask layer **158** to define the conductive line trenches **118***c* and **118***d* (see FIG. **23**A) on the first inner spacers **118***a* in the computing three-dimensional memory region T1. As shown in FIGS. **23**A and **23**B, the patterned hard mask layer **158** in the computing three-dimensional memory region T1 has a strip pattern, but the patterned hard mask layer **158** in the storage three-dimensional memory region T2 is free of the strip pattern. In other words, the first inner spacers **118***a* in the computing three-dimensional memory region T1 is partially exposed through a first side of the patterned hard mask layer **158** with the strip pattern thereon, and the first inner spacers **118***a* in the storage three-dimensional memory region T2 is entirely covered by a second side of the patterned hard mask layer **158** without having any strip pattern thereon.

[0099] Subsequently, the first inner spacers **118***a* in the computing three-dimensional memory region T1 is etched through the first side of the patterned hard mask layer **158** with the strip pattern thereon to form the conductive line trenches **118***c* and **118***d* (see FIG. **23**A), but remains the second inner spacers **118***b* in the storage three-dimensional memory region T2 covered by the second side of the patterned hard mask layer **158** without the strip pattern thereon and not to be etched (see FIG. **23**B). A pattern of the conductive line trenches **118***c* and **118***d* may correspond to the strip pattern on the patterned hard mask layer **158**. In some embodiments, the first inner spacers **118***a* may be etched using a plasma etching process (including radical plasma etching, remote plasma etching, and other suitable plasma etching processes, RIE, DRIE), gas sources such as Cl.sub.2, HBr, CF.sub.4, CHF.sub.3, CH.sub.2F.sub.2, CH.sub.3F, C.sub.4F.sub.6, BCl.sub.3, SF.sub.6, H.sub.2, NF.sub.3, and other suitable etch gas sources and combinations thereof can be used with passivation gases such as N.sub.2, O.sub.2, CO.sub.2, SO.sub.2, CO, CH.sub.4, SiCl.sub.4, and other suitable passivation gases and combinations thereof. Moreover, for the plasma etching process, the gas sources and/or the passivation gases can be diluted with gases such as Ar, He, Ne, and other suitable dilutive gases and combinations thereof to form the conductive line trenches **118***c* and **118***d*. As a non-limiting example, a source power of 10 Watts to 3,000 Watts, a bias power of 0 watts to 3,000 watts, a pressure of 1 millitorr to 5 torr, and an etch gas flow of 0 sccm to 5,000 sccm may be used in the etching process. However, it is noted that source powers, bias powers, pressures, and flow rates outside of these ranges are also contemplated. In some embodiments, after the conductive line trenches **118***c* and **118***d* are formed, the patterned hard mask layer **158** is subsequently stripped, such as by wet stripping or plasma ashing.

[0100] Referring back to FIG. **4**C, the method M then proceeds to block S**121** where the second

and third conductive line trenches are filled with a first reduced parasitic RC material and a second conductive material to form a plurality of second and third conductive lines of computing memory devices that will be electrically coupled to respective source and bit lines subsequently formed. With reference to FIGS. **24**A and **24**B, in some embodiments of block S**121**, a first reduced parasitic RC material is conformally formed over the computing three-dimensional memory region T1 and the storage three-dimensional memory region T2 and in the conductive line trenches **118***c* and **118***d*. In some embodiments, the first reduced parasitic RC material may include a conductive material, for example, metals such as Al, Ti, TiN, TaN, Co, Ag, Au, Cu, Ni, Cr, Hf, Ru, W, Pt, WN, any other suitable material or a combination or alloy thereof. In some embodiments, the first reduced parasitic RC material may include a semiconductor material, for example, an n or p-doped semiconductor such as Si, SiGe, or any other semiconductor material (e.g., IGZO, ITO, IZO, ZnO, IWO, poly silicon, amorphous Si, etc.). In some embodiments, the first reduced parasitic RC material may be formed by using, for example, CVD, ALD, PVD, PECVD, or the like.

[0101] Subsequently, a first conductive material is deposited over the first reduced parasitic RC material within the computing three-dimensional memory region T1 and the storage three-dimensional memory region T2. In some embodiments, the first conductive material may include a conductive material, for example, metals such as Al, Ti, TiN, TaN, Co, Ag, Au, Cu, Ni, Cr, Hf, Ru, W, Pt, WN, any other suitable material or a combination or alloy thereof. In some embodiments, the first conductive material may include a semiconductor material, for example, an n or p-doped semiconductor such as Si, SiGe, or any other semiconductor material (e.g., IGZO, ITO, IZO, ZnO, IWO, poly silicon, amorphous Si, etc.), and may be formed using a deposition process, an epitaxial growth process, or any other suitable process. In some embodiments, the first conductive material may be formed by using, for example, CVD, ALD, PVD, PECVD, or the like.

[0102] Subsequently, a planarized process (e.g., a CMP, etch back, or the like) is performed to remove excess portions of the first reduced parasitic RC material and the first conductive material over the stacked structures **108***a* and **108***b* until the stacked structures **108***a* and **108***b* are exposed. The remaining first reduced parasitic RC material and the first conductive material fill the conductive line trenches **118***c* and **118***d* in the first inner spacers **118***a* and from the conductive lines **120***a*, the reduced parasitic RC layers **150***a* cupping undersides of the conductive lines **120***a*, the conductive lines **122***a*, and the reduced parasitic RC layers **152***a* cupping undersides of the conductive lines **122***a* as shown in FIG. **24**A and can be electrically coupled to respective global source lines and bit lines. In some embodiments, the conductive lines **120***a* can be interchangeably referred to as conductive source lines, and the conductive lines **122***b* can be interchangeably referred to as conductive bit lines. In some embodiments, the conductive lines **120***a* can be electrically coupled to respective global bit lines and can be interchangeably referred to as conductive bit lines, and the conductive lines **122***b* can be electrically coupled to respective global source lines can be interchangeably referred to as conductive source lines.

[0103] Referring back to FIG. **4**C, the method M then proceeds to block S**122** where a plurality of fourth conductive line trenches are formed through the second inner spacers within the storage memory region. With reference to FIGS. **25**A and **25**B, in some embodiments of block S**122**, a plurality of conductive line trenches **118***e* are formed through the second inner spacers **118***b* within the storage three-dimensional memory region T2 from the top surface of the stacked structure **108***b* to the etch stop layer **101** for forming a conductive line **122***b* (see FIGS. **26**B and **26**D) that will be formed in subsequent steps in the semiconductor die **100** while remains the computing three-dimensional memory region T1 not to be etched.

[0104] A patterned hard mask layer **168** may be formed over the computing three-dimensional memory region T1 as shown in FIG. **25**A and over the storage three-dimensional memory region T2 as shown in FIG. **25**B. In some embodiments, the patterned hard mask layer **168** may be formed by patterning a hard mask material using a combination of photolithography and etching. For example, a hard mask material may be deposited over the computing three-dimensional memory

region T1 and the storage three-dimensional memory region T2. The hard mask material can be formed by using, such as a spin-on technique. Subsequently, the hard mask material may be patterned to form the patterned mask layer **168** to define the conductive line trenches **118***e* (see FIG. **25**A) on the second inner spacers **118***b* in the storage three-dimensional memory region T2. As shown in FIGS. **25**A and **25**B, the patterned hard mask layer **168** in the storage three-dimensional memory region T2 has a strip pattern, but the patterned hard mask layer **168** in the computing three-dimensional memory region T1 is free of the strip pattern. In other words, the first inner spacers **118***a* in the computing three-dimensional memory region T1 is entirely covered by a first side of the patterned hard mask layer **168** without having any strip pattern thereon, and the second inner spacers **118***b* in the storage three-dimensional memory region T2 is partially exposed through a second side of the patterned hard mask layer **168** with the strip pattern thereon.

[0105] Subsequently, the second inner spacers **118***b* in the storage three-dimensional memory region T2 is etched through the second side of the patterned hard mask layer **168** with the strip pattern thereon to form the conductive line trenches **118***e* (see FIG. **25**B), but remains the first inner spacers **118***a* in the computing three-dimensional memory region T1 covered by the first side of the patterned hard mask layer **168** without the strip pattern thereon and not to be etched (see FIG. **25**A). A pattern of the conductive line trenches **118***e* may correspond to the strip pattern on the patterned hard mask layer **168**. The conductive line trenches **118***e* extend from the top surface of the stacked structure **108***b* and terminate prior to reaching the etch stop layer **101** in the vertical direction. In some embodiments, the conductive line trenches **118***e* terminate at a position higher than a bottom surface of a topmost one of the insulating layers **112***b* in the stacked structure **108***b*. In some embodiments, the second inner spacers **118***e* may be etched using a plasma etching process (including radical plasma etching, remote plasma etching, and other suitable plasma etching processes, RIE, DRIE), gas sources such as Cl.sub.2, HBr, CF.sub.4, CHF.sub.3, CH.sub.2F.sub.2, CH.sub.3F, C.sub.4F.sub.6, BCl.sub.3, SF.sub.6, H.sub.2, NF.sub.3, and other suitable etch gas sources and combinations thereof can be used with passivation gases such as N.sub.2, O.sub.2, CO.sub.2, SO.sub.2, CO, CH.sub.4, SiCl.sub.4, and other suitable passivation gases and combinations thereof. Moreover, for the plasma etching process, the gas sources and/or the passivation gases can be diluted with gases such as Ar, He, Ne, and other suitable dilutive gases and combinations thereof to form the conductive line trenches **118***e*. As a non-limiting example, a source power of 10 Watts to 3,000 Watts, a bias power of 0 watts to 3,000 watts, a pressure of 1 millitorr to 5 torr, and an etch gas flow of 0 sccm to 5,000 sccm may be used in the etching process. However, it is noted that source powers, bias powers, pressures, and flow rates outside of these ranges are also contemplated. In some embodiments, after the conductive line trenches **118***e* are formed, the patterned hard mask layer **168** is subsequently stripped, such as by wet stripping or plasma ashing.

[0106] Referring back to FIG. **4**C, the method M then proceeds to block S**123** where the fourth conductive line trenches are filled with a second reduced parasitic RC material and a second conductive material to form a plurality of fourth conductive lines of storage memory devices that will be electrically coupled to respective bit lines subsequently formed. With reference to FIGS. **26**A-**26**D, in some embodiments of block S**123**, a second reduced parasitic RC material is conformally formed over the computing three-dimensional memory region T1 and the storage three-dimensional memory region T2 and in the conductive line trenches **118***e*. In some embodiments, the second reduced parasitic RC material may include a conductive material, for example, metals such as Al, Ti, TiN, TaN, Co, Ag, Au, Cu, Ni, Cr, Hf, Ru, W, Pt, WN, any other suitable material or a combination or alloy thereof. In some embodiments, the second reduced parasitic RC material may include a semiconductor material, for example, an n or p-doped semiconductor such as Si, SiGe, or any other semiconductor material (e.g., IGZO, ITO, IZO, ZnO, IWO, poly silicon, amorphous Si, etc.). In some embodiments, the second reduced parasitic RC material may be formed by using, for example, CVD, ALD, PVD, PECVD, or the like.

[0107] Subsequently, a second conductive material is deposited over the second reduced parasitic RC material within the computing three-dimensional memory region T1 and the storage three-dimensional memory region T2. In some embodiments, the second conductive material may include a conductive material, for example, metals such as Al, Ti, TiN, TaN, Co, Ag, Au, Cu, Ni, Cr, Hf, Ru, W, Pt, WN, any other suitable material or a combination or alloy thereof. In some embodiments, the second conductive material may include a semiconductor material, for example, an n or p-doped semiconductor such as Si, SiGe, or any other semiconductor material (e.g., IGZO, ITO, IZO, ZnO, IWO, poly silicon, amorphous Si, etc.), and may be formed using a deposition process, an epitaxial growth process, or any other suitable process. In some embodiments, the second conductive material may be formed by using, for example, CVD, ALD, PVD, PECVD, or the like.
[0108] Subsequently, a planarized process (e.g., a CMP, etch back, or the like) is performed to remove excess portions of the second reduced parasitic RC material and the second conductive material over the stacked structures **108***a* and **108***b* until the stacked structures **108***a* and **108***b* are exposed. The remaining second reduced parasitic RC material and the second conductive material fill the conductive line trenches **118***e* in the second inner spacers **118***b* and form the conductive lines **122***b* and the reduced parasitic RC layers **152***b* cupping undersides of the conductive lines **122***b* as shown in FIG. **26**B that that can be electrically coupled to respective global bit lines subsequently formed. In some embodiments, the conductive lines **122***b* can be interchangeably referred to as conductive bit lines.
[0109] Referring back to FIG. **4**C, the method M then proceeds to block S**124** where a plurality of first global source lines and first global bit lines are formed on the first stacked structure within the computing memory region and electrically coupled to the corresponding second and third conductive lines and a plurality of second global bit lines are formed on the second stacked structure within the storage memory region and electrically coupled to the corresponding fourth conductive lines. With reference to FIGS. **27**A and **27**B, in some embodiments of block S**124**, first global source lines **160***a* and first global drain lines **170***a* are formed on the stacked structure **108***a* within the computing three-dimensional memory region T1 (see FIG. **27**A) and electrically coupled to the corresponding conductive lines **120***a* and **122***a* (see FIG. **26**A) through first source vias **162***a* and first drain vias **172***a*, and second global drain lines **170***b* are formed on the stacked structure **108***b* within the storage three-dimensional memory region T2 (see FIG. **27**B) and electrically coupled to the corresponding conductive line **122***b* (see FIG. **26**B) through second drain vias **172***b*. The global drain lines **170***a* may be formed simultaneously with the global source lines **160***a*. Each of the global source lines **160***a* and the global drain lines **170***a* extend in the Y-direction.
[0110] The global source lines **160***a* and the global drain lines **170***a/b* may be formed from a conductive material, for example, tungsten (W), copper (Cu), cobalt (Co), etc. In some embodiments, the source vias **162***a/b* and the drain vias **172***b* may be formed from a conductive material for example, tungsten (W), copper (Cu), cobalt (Co), etc. In some embodiments, the source vias **162***a/b* and the drain vias **172***b* may be formed using a dual damascene process. The global source lines **160***a* and the global drain lines **170***a/b* may be used to communicate an electrical signal (e.g., a current or voltage) to corresponding conductive lines **120***a/b*, and the global drain lines **170***a/b* may be used to receive an electrical signal (e.g., a current or voltage) from a corresponding conductive lines **122***a/b*, when the gate layer **124***a/b* is activated.
[0111] Reference is made to FIGS. **28**A and **28**B. FIG. **28**A a schematic diagram illustrating a relationship between voltage and bit current count of computing three-dimensional memory devices (e.g., AND memory devices) in accordance with some embodiments of the present disclosure. FIG. **28**B a schematic diagram illustrating a relationship between voltage and bit current count of storage three-dimensional memory devices (e.g., NAND memory devices) in accordance with some embodiments of the present disclosure.
[0112] As shown in FIG. **28**A, the computing three-dimensional memory device has two memory

statuses to form 1 bit based on a program voltage PGM3 relative to an erased voltage. As shown in FIG. **28**B, the storage three-dimensional memory device has four memory statuses to form 2 bit based on three different program voltages V.sub.PGM1, V.sub.PGM2, and V.sub.PGM3 relative to the erased voltage V.sub.ERS. Because the computing and storage three-dimensional memory devices are formed monolithically in the same wafer, which in turn allows for simultaneously operating the computing and storage three-dimensional memory devices in the same program voltage V.sub.PGM3 and the same erased voltage V.sub.ERS. This beneficially reduces computing power needed to perform the same operation. By way of example and not limitation, the first and second semiconductor devices **110***a* and **110***b* as shown in FIGS. **2**A-**3**B can be simultaneously operated in the same program voltage V.sub.PGM3 and the same erased voltage V.sub.ERS. It should be appreciated that while the first and second semiconductor devices **110***a* and **110***b* illustrate particular embodiments of operations in the same program voltage V.sub.PGM3 and the same erased voltage V.sub.ERS, in other embodiments the first and second semiconductor devices **110***a* and **110***b* arranged in the same semiconductor die in any suitable configuration or arrangement can also be simultaneously operated in the same program voltage V.sub.PGM3 and the same erased voltage V.sub.ERS. All such arrangements are contemplated and should be considered to be within the scope of the present disclosure.

[0113] Based on the above discussions, it can be seen that the present disclosure offers advantages. It is understood, however, that other embodiments may offer additional advantages, and not all advantages are necessarily disclosed herein, and that no particular advantage is required for all embodiments. The present disclosure in various embodiments provides a semiconductor die including a plurality of computing 3D memory devices (e.g., AND memory devices) that provide high speed computing and a plurality of storage 3D memory devices (e.g., NAND memory devices) that provide high density storage for a multi-level cell. The computing and storage 3D memory devices are used to a computing in memory (CIM) application and formed monolithically in the same wafer, which in turn allows for improving a propagation delay issue while date is transferred between the computing and storage 3D memory devices and achieving a within-wafer multiple memory integration. This beneficially reduces computing power needed to perform the same operation, reduces propagation losses, and reduces manufacturing cost, time, and complexity.

[0114] In some embodiments, the method includes forming a multi-layered stack having a plurality of insulating layers and a plurality of spacer layers alternately stacked on top of each other in a vertical direction over a substrate in a chip area having a first memory region and a second memory region; forming a first mask layer covering the second memory region, while leaving the first memory region partially exposed; with the first mask layer in place, etching the multi-layered stack to form a plurality of first trenches defining a plurality of first memory stacked structures in the first memory region; forming a plurality of first gate layers, a first memory layer, and a first channel layer in the plurality of first trenches; removing the first mask layer; forming a second mask layer covering the first memory region, while leaving the second memory region partially exposed; with the second mask layer in place, etching the multi-layered stack to form a plurality of second trenches defining a plurality of second memory stacked structures in the second memory region; forming a plurality of second gate layers, a second memory layer, and a second channel layer in the plurality of second trenches. In some embodiments, the first memory stacked structures are of an AND memory, and the second memory stacked structures are of a NAND memory. In some embodiments, the method further includes laterally recessing the plurality of spacer layers within the first trenches to form a plurality of first cavities in the first memory stacked structures. In some embodiments, the first gate layers are formed in the plurality of first cavities of the first memory stacked structures. In some embodiments, the first memory layer is deposited over the plurality of first gate layers, and the first channel layer is deposited over the first memory layer. In some embodiments, the method further includes forming a plurality of conductive source lines and a plurality of conductive bit lines extending through the plurality of first memory stacked structures

in the first memory region. In some embodiments, the method further includes forming a plurality of conductive bit lines extending downwardly from top surfaces of the plurality of second memory stacked structures and terminating prior to reaching bottom surfaces of the plurality of second memory stacked structures in the second memory region. In some embodiments, the method further includes forming a plurality of reduced parasitic resistance capacitance layers cupping undersides of the plurality of conductive bit lines. In some embodiments, the method further includes after forming the plurality of second gate layers, the second memory layer, and the second channel layer, removing the second mask layer; and after removing the second mask layer, laterally recessing the plurality of spacer layers within the second trenches to form a plurality of second cavities in the second memory stacked structures. In some embodiments, the plurality of second gate layers are formed in the plurality of second cavities of the second memory stacked structures. In some embodiments, the second memory layer is deposited over the plurality of second gate layers, and the second channel layer is deposited over the second memory layer.

[0115] In some embodiments, the method includes forming a first set of a plurality of first semiconductor devices over a substrate at a first location of a semiconductor die, the first set of the plurality of first semiconductor devices being of an AND memory; forming a second set of a plurality of second semiconductor devices over the substrate at a second location of the semiconductor die different from the first location, the second set of the plurality of second semiconductor devices being of a NAND memory. In some embodiments, the method includes forming a third set of a plurality of third semiconductor devices over the substrate and being of the AND memory, the third set of the plurality of third semiconductor devices located between the first set of the plurality of the first semiconductor devices and the second set of the plurality of the second semiconductor devices. In some embodiments, the method includes forming a third set of a plurality of third semiconductor devices over the substrate and being of the AND memory, the second set of the plurality of second semiconductor devices located between the first set of the plurality of the first semiconductor devices and the third set of the plurality of the third semiconductor devices. In some embodiments, the method includes forming a third set of a plurality of third semiconductor devices over the substrate and being of the NAND memory, the third set of the plurality of third semiconductor devices located between the first set of the plurality of the first semiconductor devices and the second set of the plurality of the second semiconductor devices. In some embodiments, the method includes forming a third set of a plurality of third semiconductor devices over the substrate and being of the NAND memory, the first set of the plurality of first semiconductor devices located between the second set of the plurality of the second semiconductor devices and the third set of the plurality of the third semiconductor devices.

[0116] In some embodiments, the semiconductor die includes a substrate, a first memory array, and a second memory array. The first memory array is over the substrate and includes a plurality of first semiconductor devices, a first source line, and a first bit line. The first semiconductor devices are stacked in a vertical direction. The first source line electrically connects to the first semiconductor devices and extends downwardly from a topmost one of the first semiconductor devices to a lowermost one of the first semiconductor devices. The first bit line electrically connects to the first semiconductor devices and extending downwardly from the topmost one of the first semiconductor devices to the lowermost one of the first semiconductor devices. The second memory array is over the substrate and includes a plurality of second semiconductor devices, a second source line, and a second bit line. The second semiconductor devices are stacked in the vertical direction. The second source line electrically connects to the second semiconductor devices and is disposed below the second semiconductor devices. The second bit line electrically connects to the second semiconductor devices and is disposed above the second source line. In some embodiments, the semiconductor die further includes a first channel layer shared by the plurality of first semiconductor devices, the first channel layer extending downwardly from a top end of the first source line to a bottom end of the first source line. In some embodiments, the semiconductor die

further includes a second channel layer shared by the plurality of second semiconductor devices, the second channel layer having a different cross-sectional profile than the first channel layer. In some embodiments, the second channel layer is contact with a top surface of the second source line.

[0117] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

Claims

1. A semiconductor die, comprising: a substrate; a first memory array over the substrate and comprising: a plurality of first semiconductor devices stacked in a vertical direction; a first source line electrically connecting to the plurality of first semiconductor devices and extending downwardly from a topmost one of the first semiconductor devices to a lowermost one of the first semiconductor devices; and a first bit line electrically connecting to the plurality of first semiconductor devices and extending downwardly from the topmost one of the first semiconductor devices to the lowermost one of the first semiconductor devices; and a second memory array over the substrate and comprising: a plurality of second semiconductor devices stacked in the vertical direction; a second source line electrically connecting to the plurality of second semiconductor devices and disposed below the plurality of second semiconductor devices; a second bit line electrically connecting to the plurality of second semiconductor devices and disposed above the second source line; and a first conductive layer that cups an underside of the second bit line, wherein the first memory array is an AND memory, and the second memory array is a NAND memory.

2. The semiconductor die of claim 1, wherein the first conductive layer is made of a material having a lower resistance capacitance than the second bit line.

3. The semiconductor die of claim 1, wherein the first conductive layer has a concave bottom surface.

4. The semiconductor die of claim 1, wherein the first conductive layer has a convex bottom surface.

5. The semiconductor die of claim 1, further comprising: a second conductive layer cupping an underside of the first source line.

6. The semiconductor die of claim 1, further comprising: a second conductive layer cupping an underside of the first bit line.

7. The semiconductor die of claim 1, further comprising: a second conductive layer that is cupped by the second source line.

8. A semiconductor die, comprising: a substrate; a first memory array over the substrate and comprising: a plurality of first semiconductor devices stacked in a vertical direction; a first source line electrically connecting to the plurality of first semiconductor devices and extending downwardly from a topmost one of the first semiconductor devices to a lowermost one of the first semiconductor devices; a first bit line electrically connecting to the plurality of first semiconductor devices and extending downwardly from the topmost one of the first semiconductor devices to the lowermost one of the first semiconductor devices; and at least one conductive layer that cups undersides of at least one of the first source line and the first bit line; and a second memory array over the substrate and comprising: a plurality of second semiconductor devices stacked in the

vertical direction; a second source line electrically connecting to the plurality of second semiconductor devices and disposed below the plurality of second semiconductor devices; and a second bit line electrically connecting to the plurality of second semiconductor devices and disposed above the second source line.

9. The semiconductor die of claim 8, wherein the conductive layer comprises Al, Ti, TiN, TaN, Co, Ag, Au, Cu, Ni, Cr, Hf, Ru, W, WN, PT, or combinations thereof.

10. The semiconductor die of claim 8, wherein the first memory array and the second memory array are different forms of memory devices.

11. The semiconductor die of claim 8, further comprising: a first channel layer shared by the first semiconductor devices, wherein the first channel layer extends downwardly from a top end of the first source line to a bottom end of the first source line.

12. The semiconductor die of claim 11, further comprising: a second channel layer shared by the second semiconductor devices, wherein the second channel layer having a different cross-sectional profile than the first channel layer.

13. The semiconductor die of claim 11, wherein the first channel layer has a U-shaped cross-sectional profile.

14. A semiconductor die, comprising: a substrate; an etch stop layer disposed over the substrate; a first memory array over the substrate and comprising: a plurality of first semiconductor devices stacked in a vertical direction; a first source line electrically connecting to the plurality of first semiconductor devices and extending downwardly from a topmost one of the first semiconductor devices to a lowermost one of the first semiconductor devices; and a first bit line electrically connecting to the plurality of first semiconductor devices and extending downwardly from the topmost one of the first semiconductor devices to the lowermost one of the first semiconductor devices; and a second memory array over the substrate and comprising: a plurality of second semiconductor devices stacked in the vertical direction; a second source line electrically connecting to the plurality of second semiconductor devices and embedded in the etch stop layer; a second bit line electrically connecting to the plurality of second semiconductor devices and disposed above the second source line; and a conductive layer that is cupped by the second source line.

15. The semiconductor die of claim 14, wherein the conductive layer is made of a material having a lower resistance capacitance than the second source line.

16. The semiconductor die of claim 14, further comprising: a channel layer shared by the second semiconductor devices, wherein the channel layer has a U-shaped profile in a cross-sectional view.

17. The semiconductor die of claim 16, wherein, in the cross-sectional view, a width of the conductive layer is greater than a lateral dimension of the channel layer.

18. The semiconductor die of claim 16, wherein, in the cross-sectional view, a width of the conductive layer is less than a lateral dimension of the channel layer.

19. The semiconductor die of claim 16, wherein, in the cross-sectional view, a width of the conductive layer is substantially equal to a lateral dimension of the channel layer.

20. The semiconductor die of claim 16, wherein the channel layer is contact with a top surface of the conductive layer.