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(54) **STACKED MULTI-GATE DEVICE WITH CONTACT FEATURE AND METHODS FOR FORMING THE SAME**

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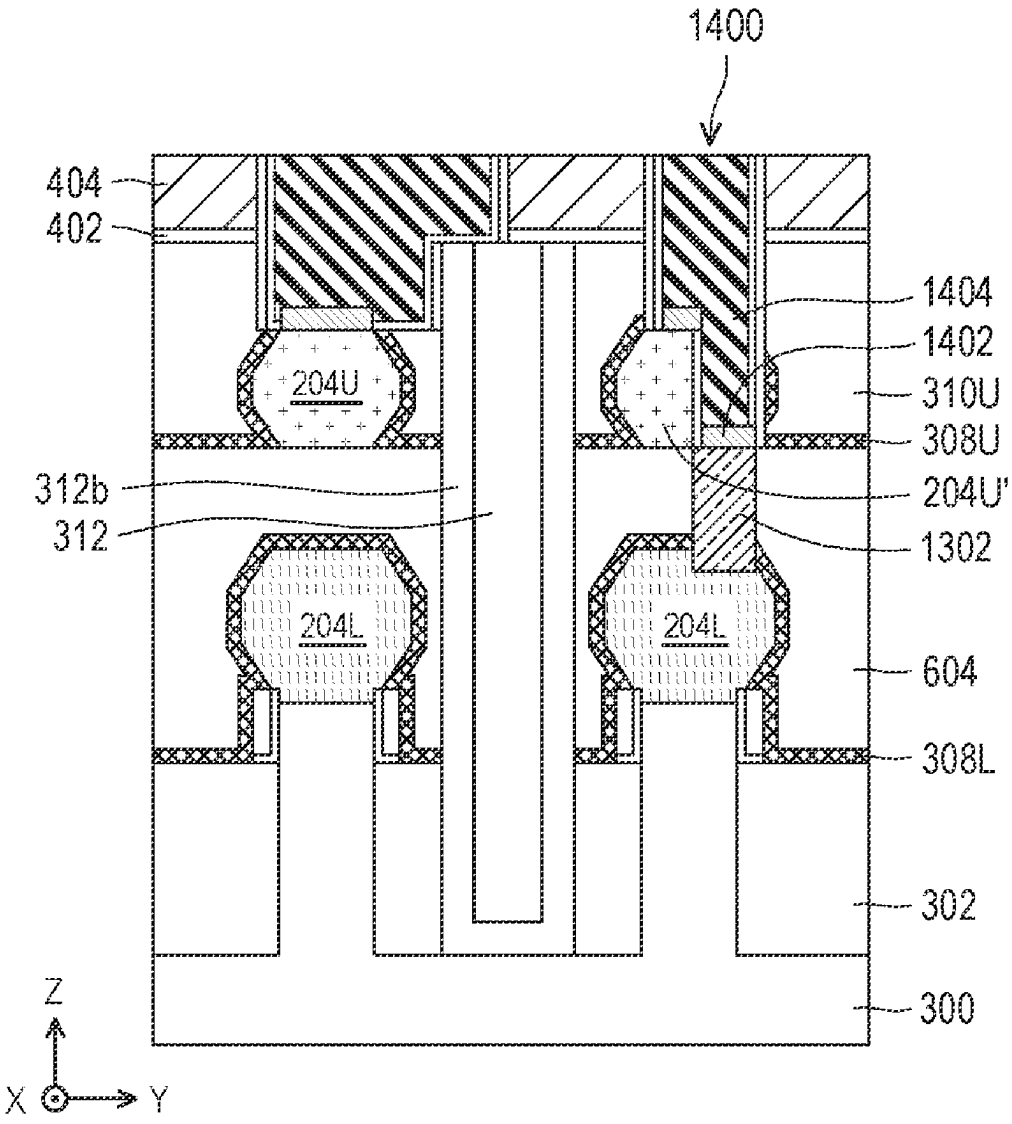
H01L 21/02	(2006.01)
H01L 27/12	(2006.01)

(52) **U.S. Cl.**

CPC ***H10D 84/038*** (2025.01); ***H10D 87/00*** (2025.01); ***H10D 88/01*** (2025.01); *H01L 21/0234* (2013.01)

(57) **ABSTRACT**

Methods and devices that include forming a first epitaxial region and a second epitaxial region above the first epitaxial region. An opening may be formed extending from the first region to the second region. And a liner layer is deposited on a sidewall and a bottom of the opening. A plasma treatment is performed on the liner layer, which can form a conditioned or passivated region of the first epitaxial region that may be maintained during the growth of additional epitaxial material on the second epitaxial region.



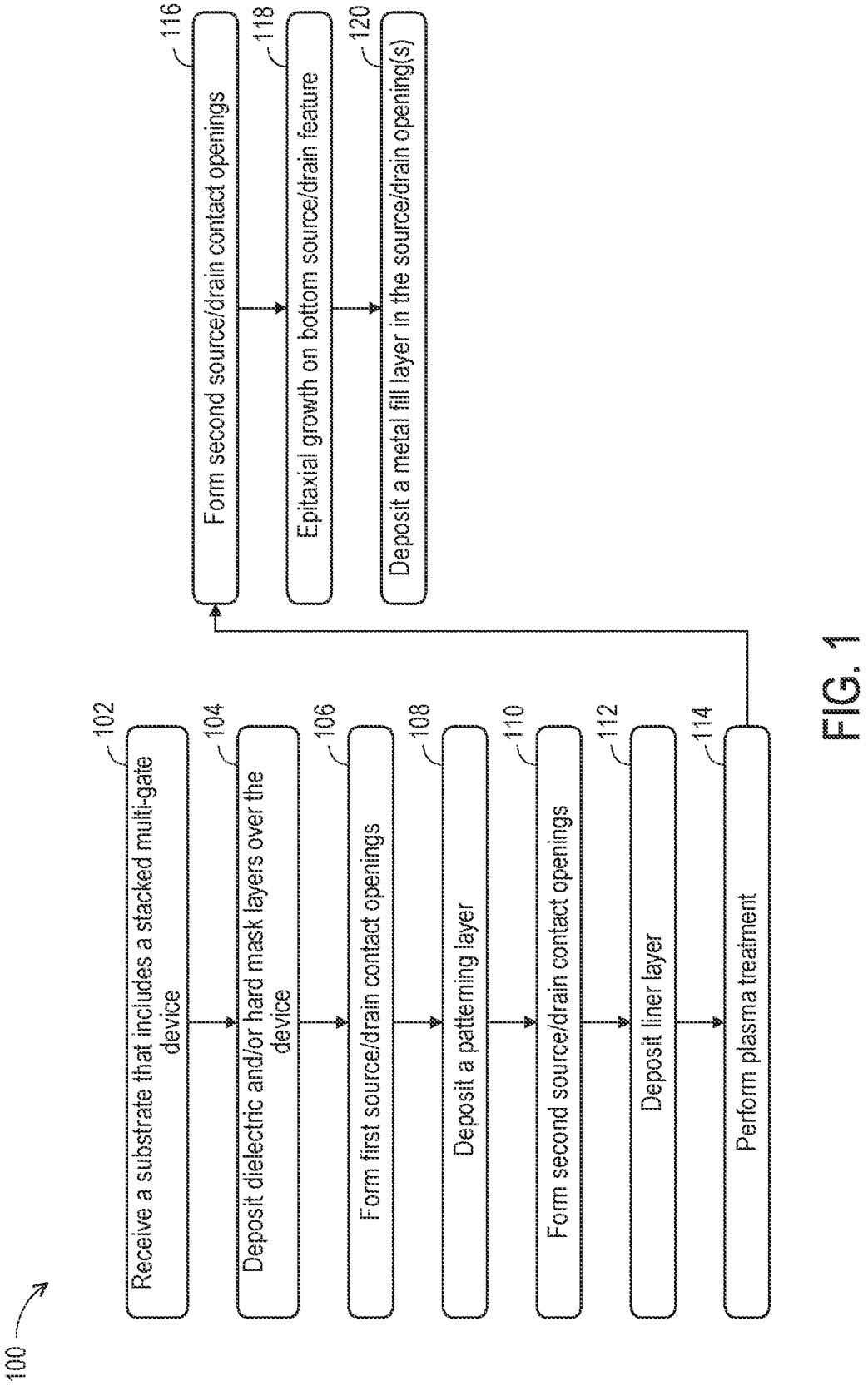
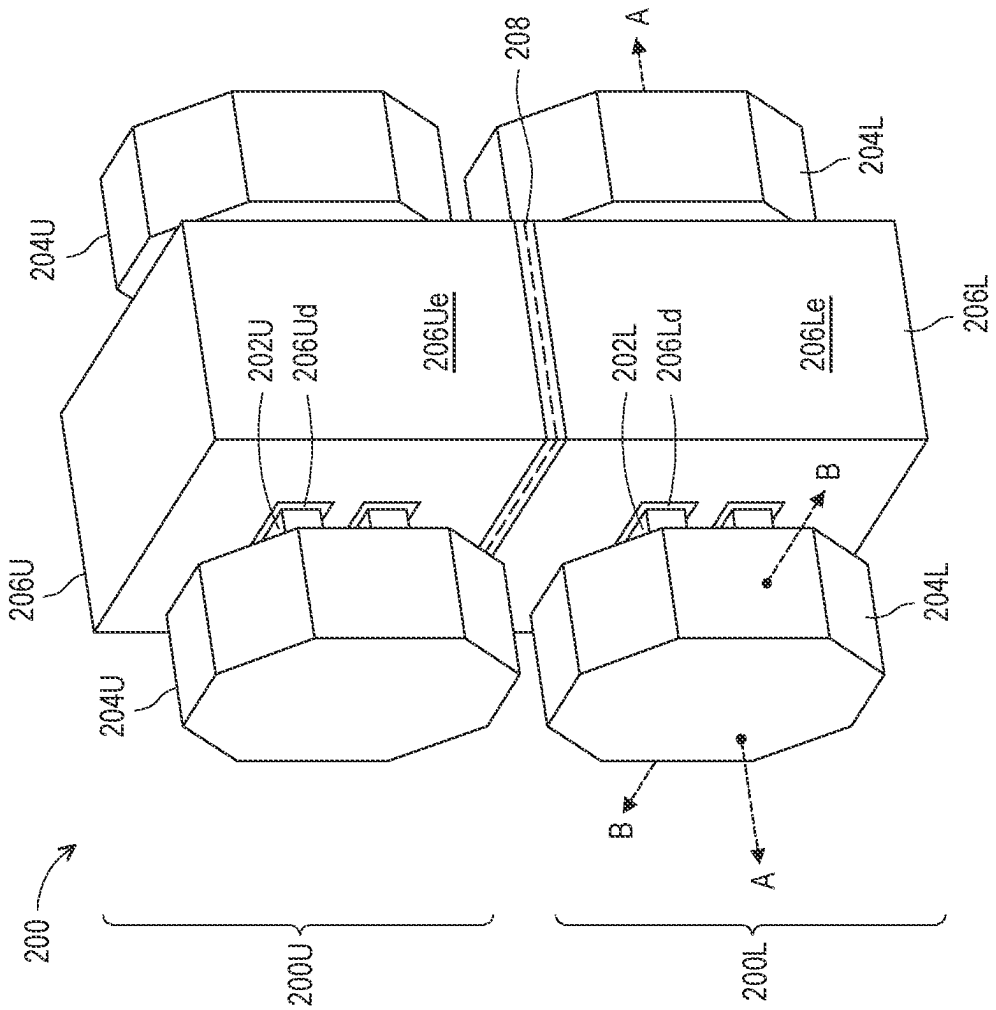

100
102
Receive a substrate that includes a stacked multi-gate device
104
Deposit dielectric and/or hard mask layers over the device
106
Form first source/drain contact openings
108
Deposit a patterning layer
110
Form second source/drain contact openings
112
Deposit liner layer
114
Perform plasma treatment
116
Form second source/drain contact openings
118
Epitaxial growth on bottom source/drain feature
120
Deposit a metal fill layer in the source/drain opening(s)

FIG. 1


208
A
204L
204U
206L
202U
206Ud
206Ue
202L
206Ld
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206U
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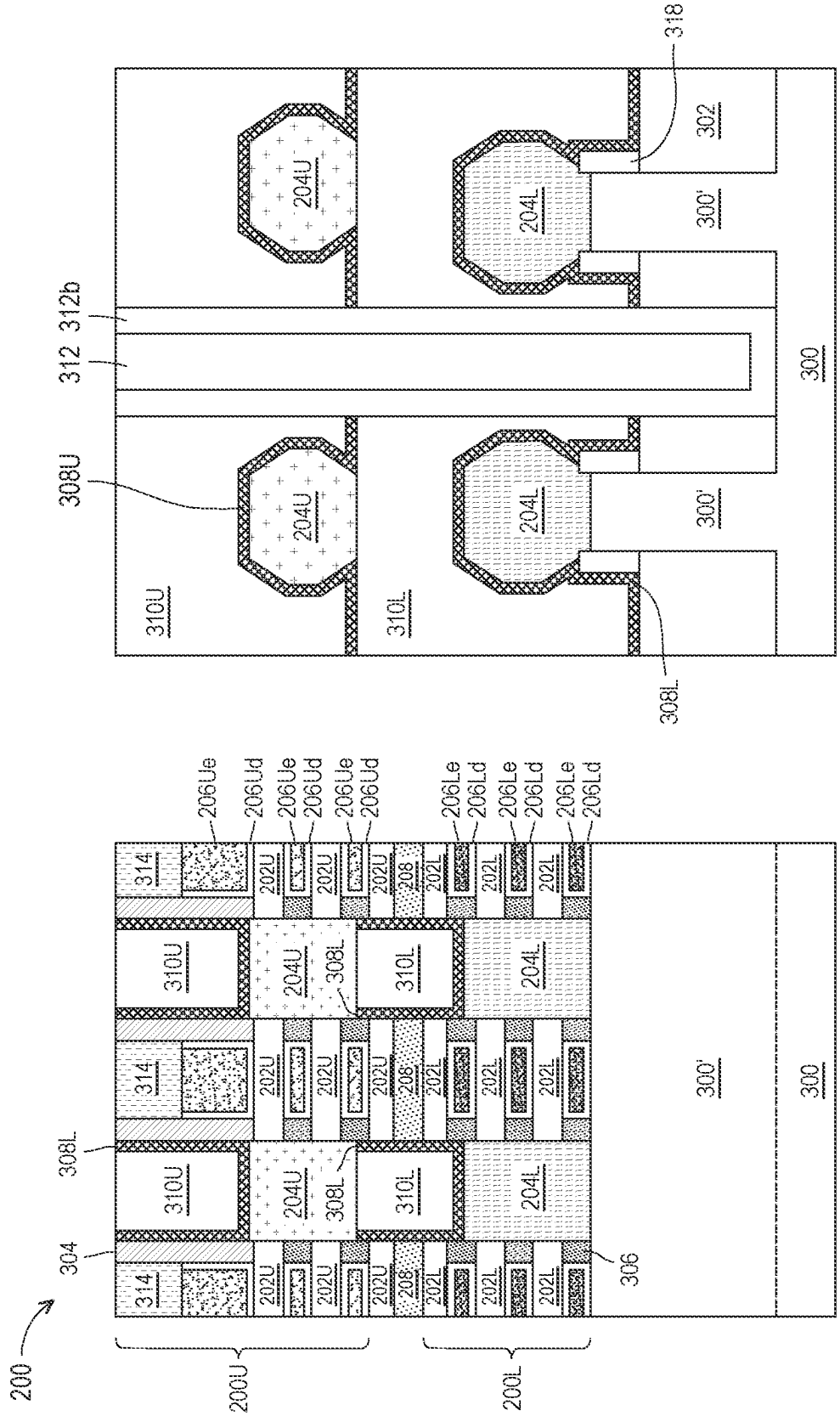
A
200
200U
200L

FIG. 2


200
200U
200L
304
308L
310U
310L
314
202U
202L
204U
204L
206Ue
206Ud
206Le
206Ld
208
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300'
300
312
312b
308U
318
302

FIG. 3A

FIG. 3B

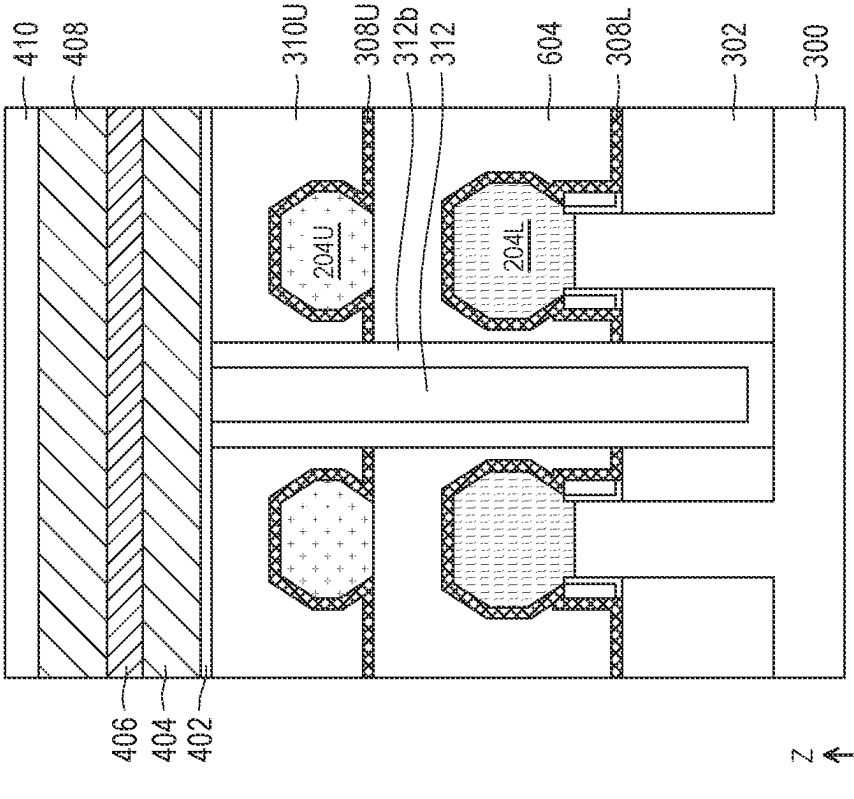
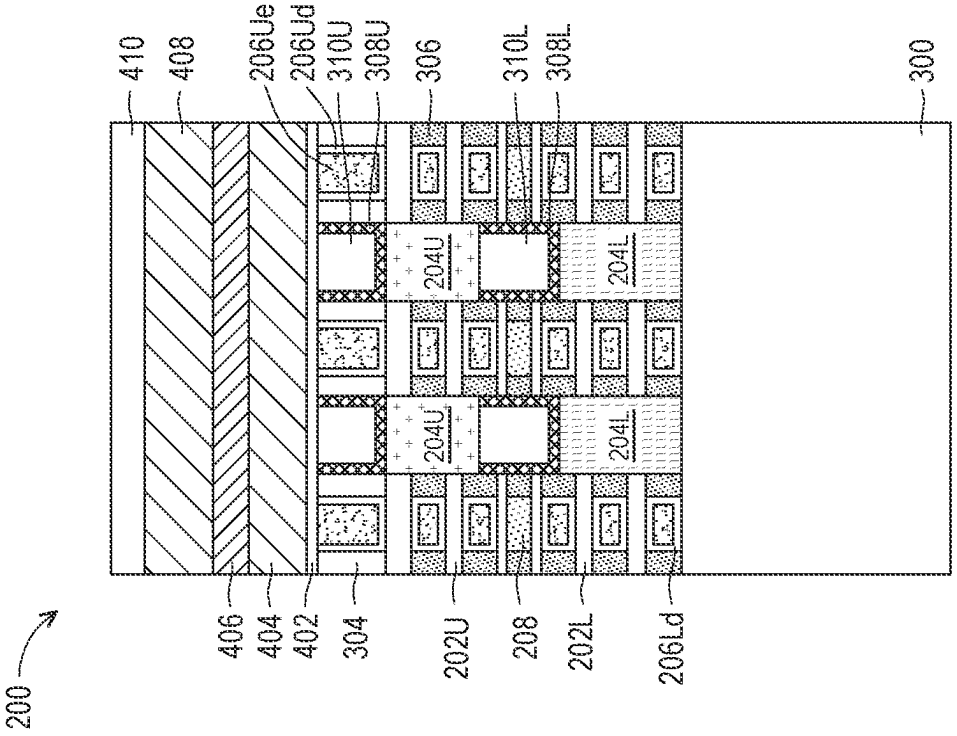

410
408
310U
308U
312b
312
604
308L
302
300
204U
204L
406
404
402
Z
Y
X

FIG. 4B


410
408
206Ue
206Ud
310U
308U
306
310L
308L
300
204U
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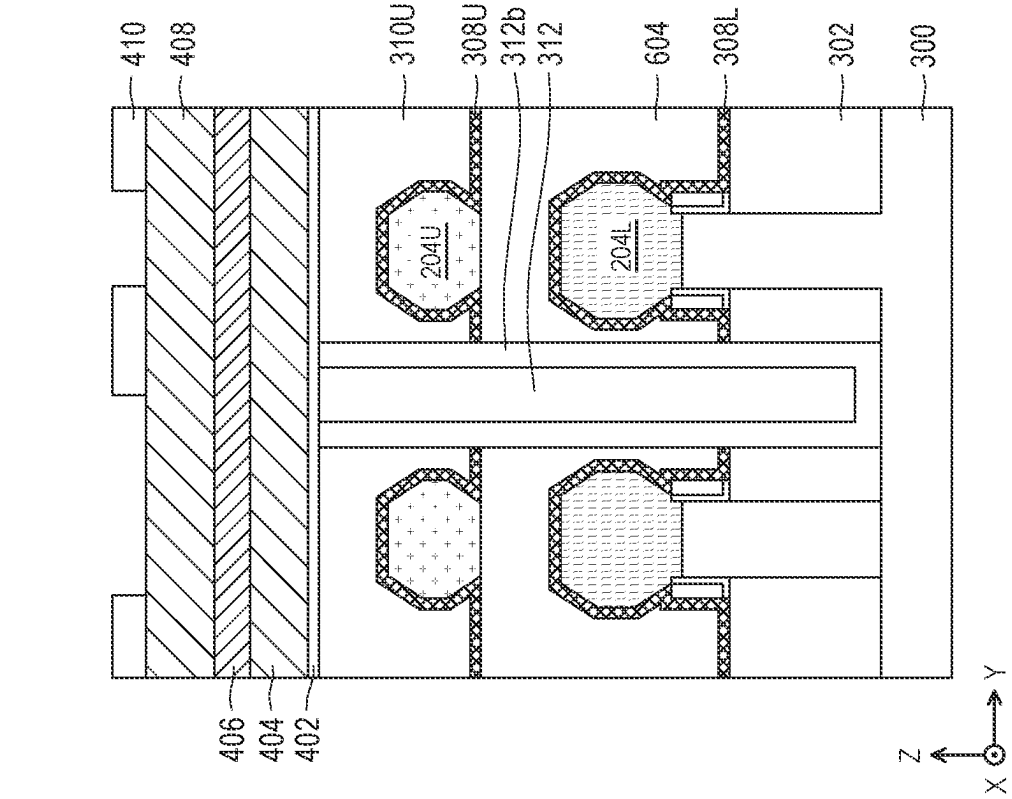
304
202U
208
202L
206Ld
200

FIG. 4A


410
408
310U
308U
312b
312
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308L
302
300
204U
204L
406
404
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Y
X

FIG. 5B

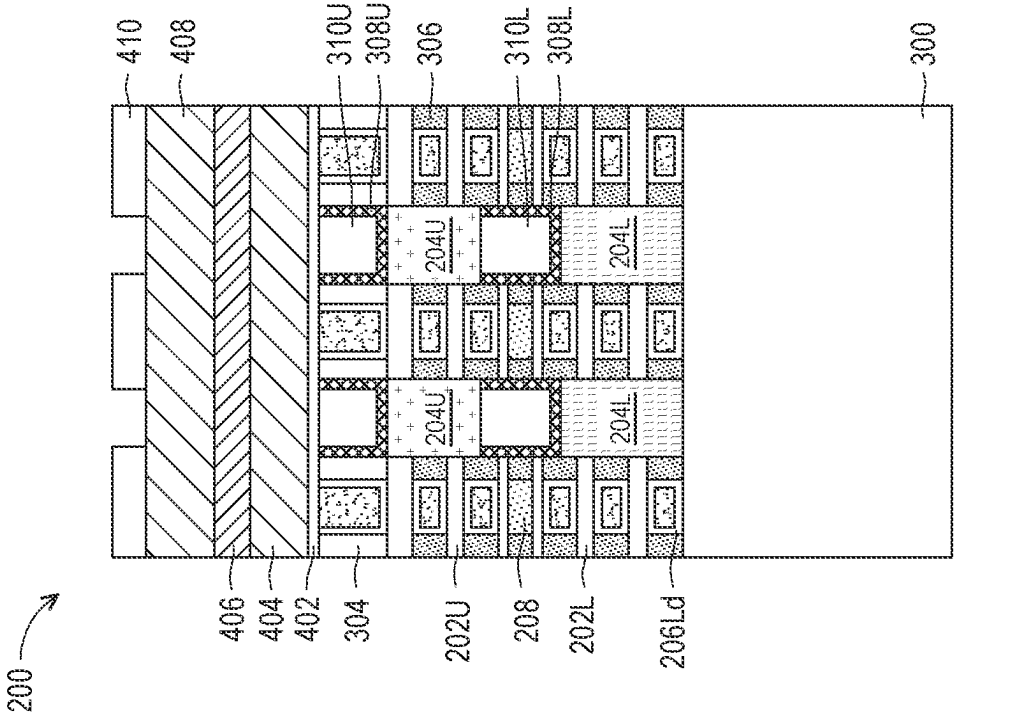
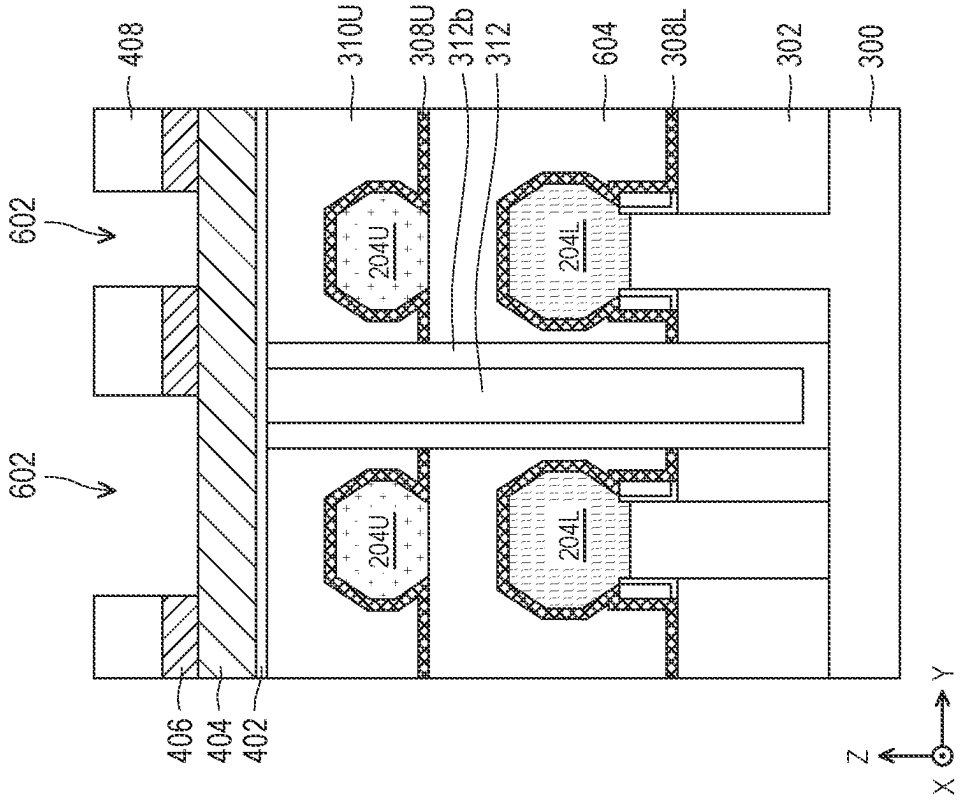

410
408
310U
308U
306
310L
308L
300
204U
204L
406
404
402
304
202U
208
202L
206Ld
200

FIG. 5A


408
310U
308U
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312
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308L
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204U
204L
204U
204L
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402
Z
Y
X

FIG. 6B

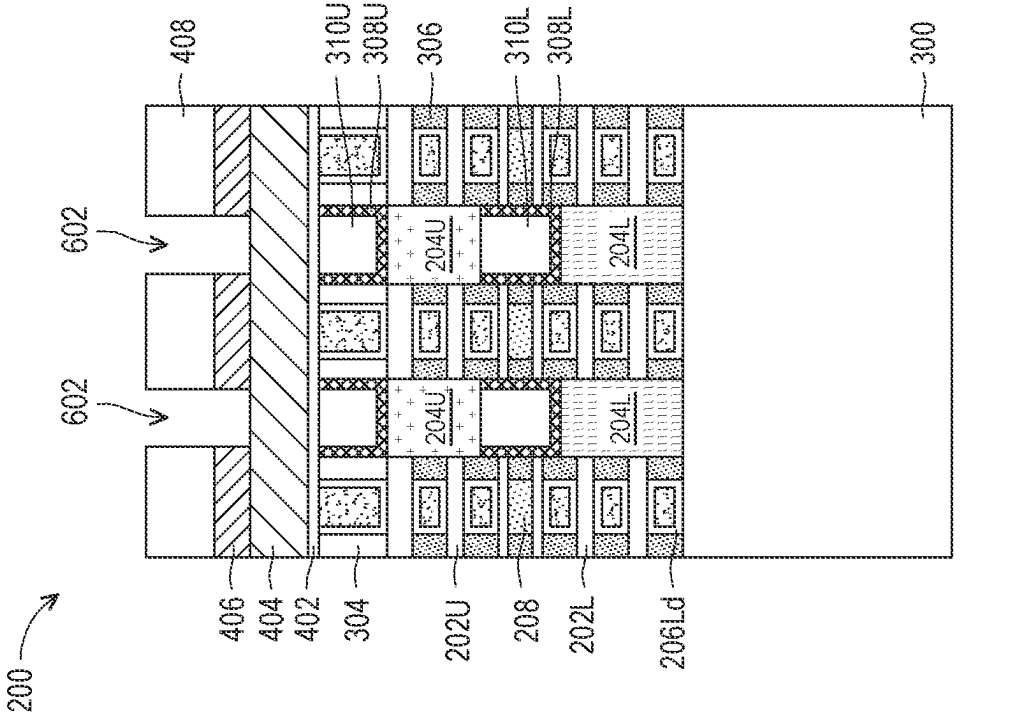
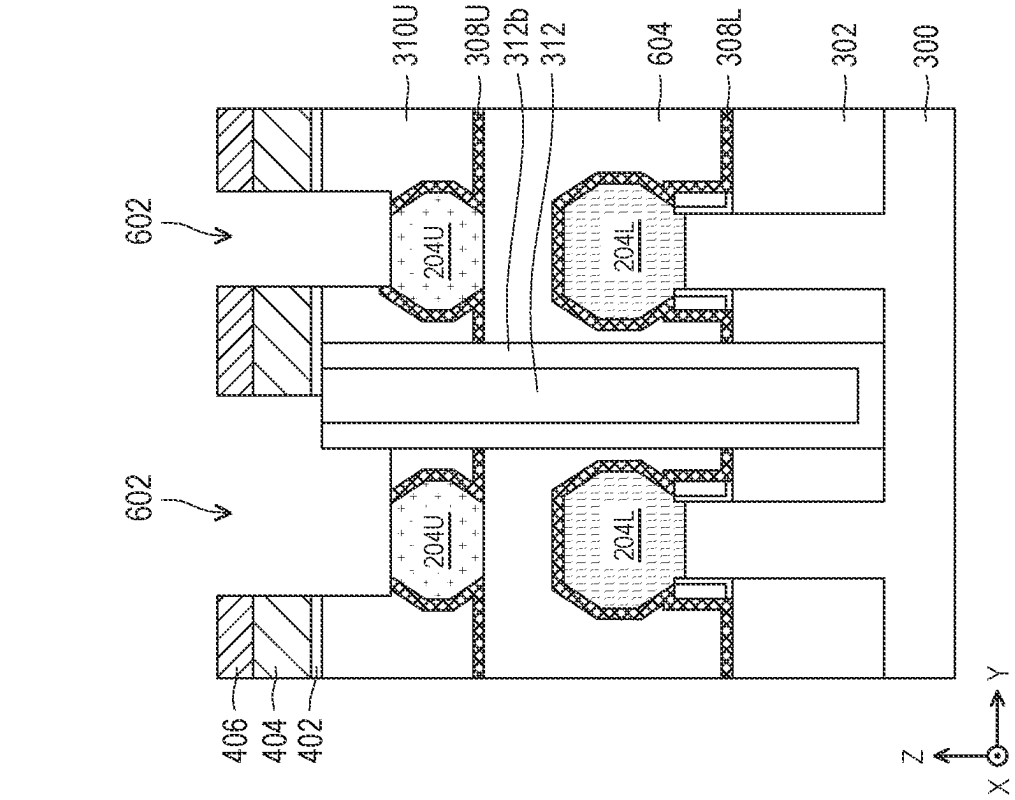

200
408
310U
308U
306
310L
308L
300
602
602
602
204U
204L
204U
204L
406
404
402
304
202U
208
202L
206Ld

FIG. 6A


310U
308U
312b
312
604
308L
302
300
602
602
204U
204U
204L
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406
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Z
Y
X

FIG. 7B

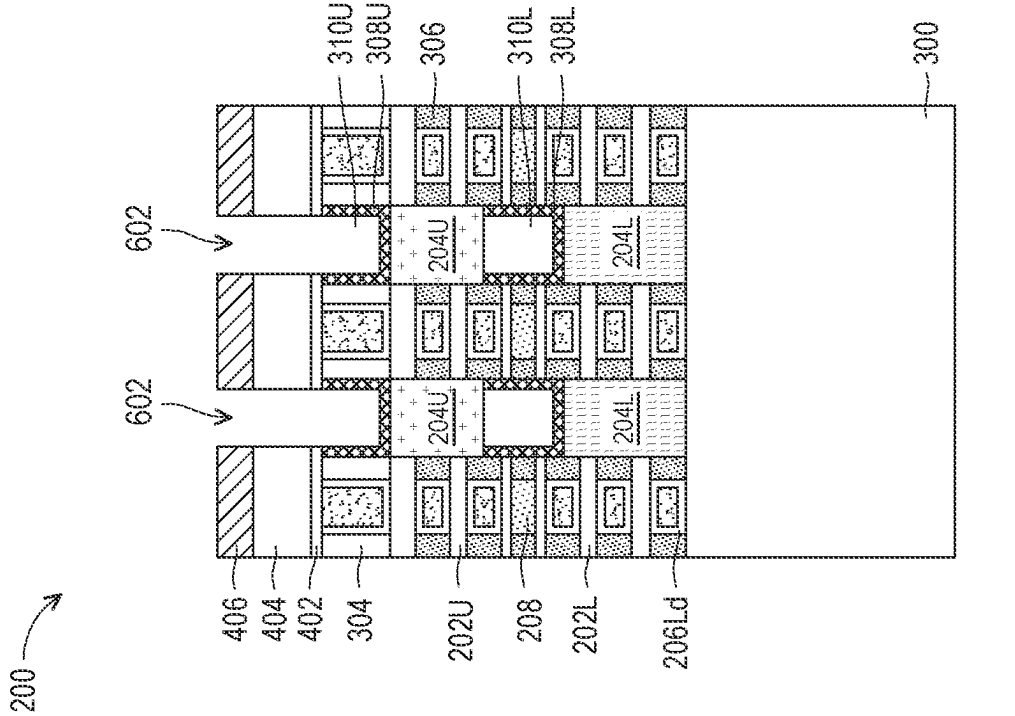
310U
308U
306
310L
308L
300
602
602
602
204U
204U
204U
204L
204L
204L
406
404
402
304
202U
208
202L
206Ld
200

FIG. 7A

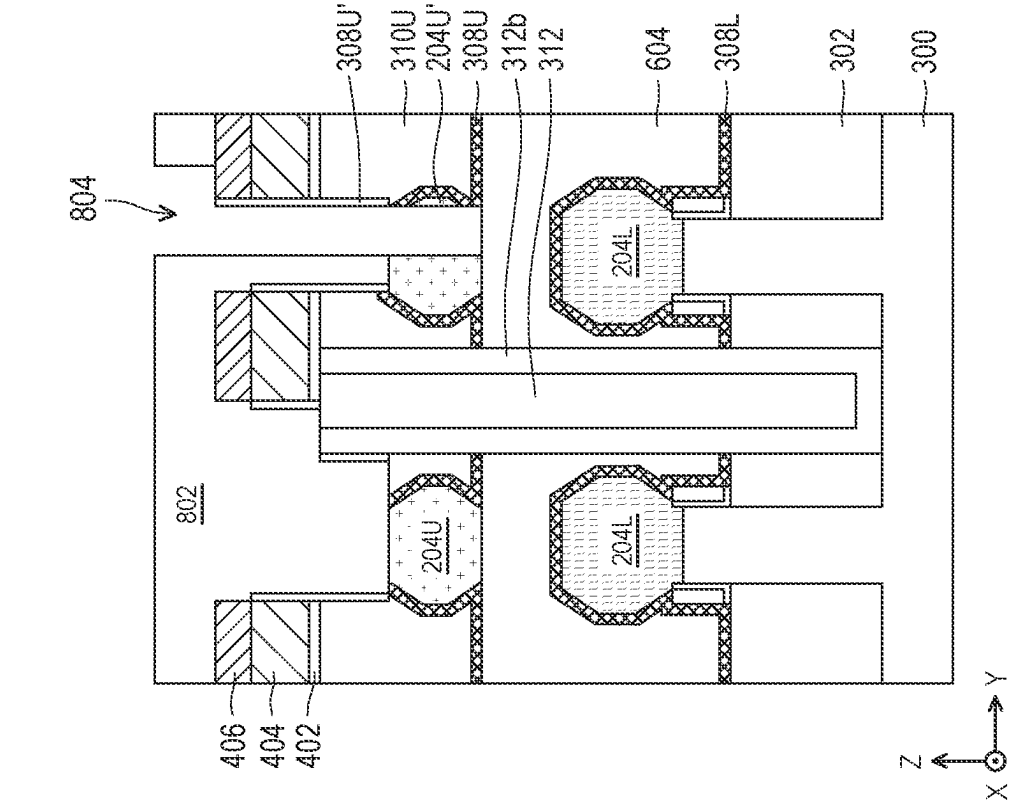
308U'
310U
204U'
308U
312b
312
604
308L
302
300
804
802
204L
204U
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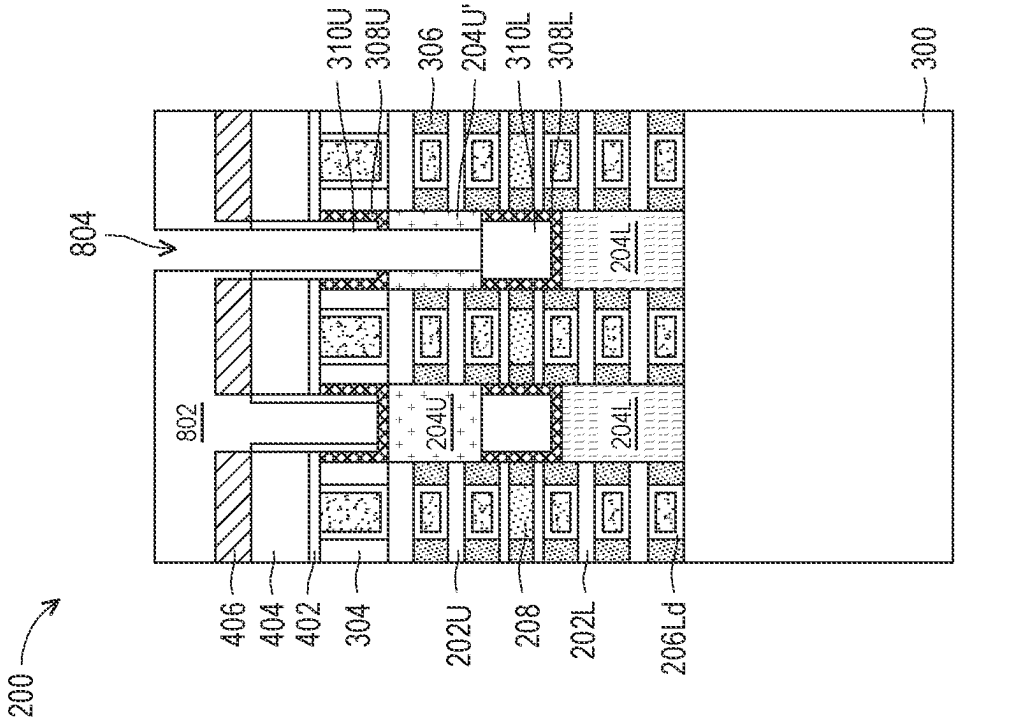
FIG. 8B


310U
308U
306
204U'
310L
308L
300
804
802
204L
204U'
406
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402
304
202U
208
202L
206Ld
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FIG. 8A

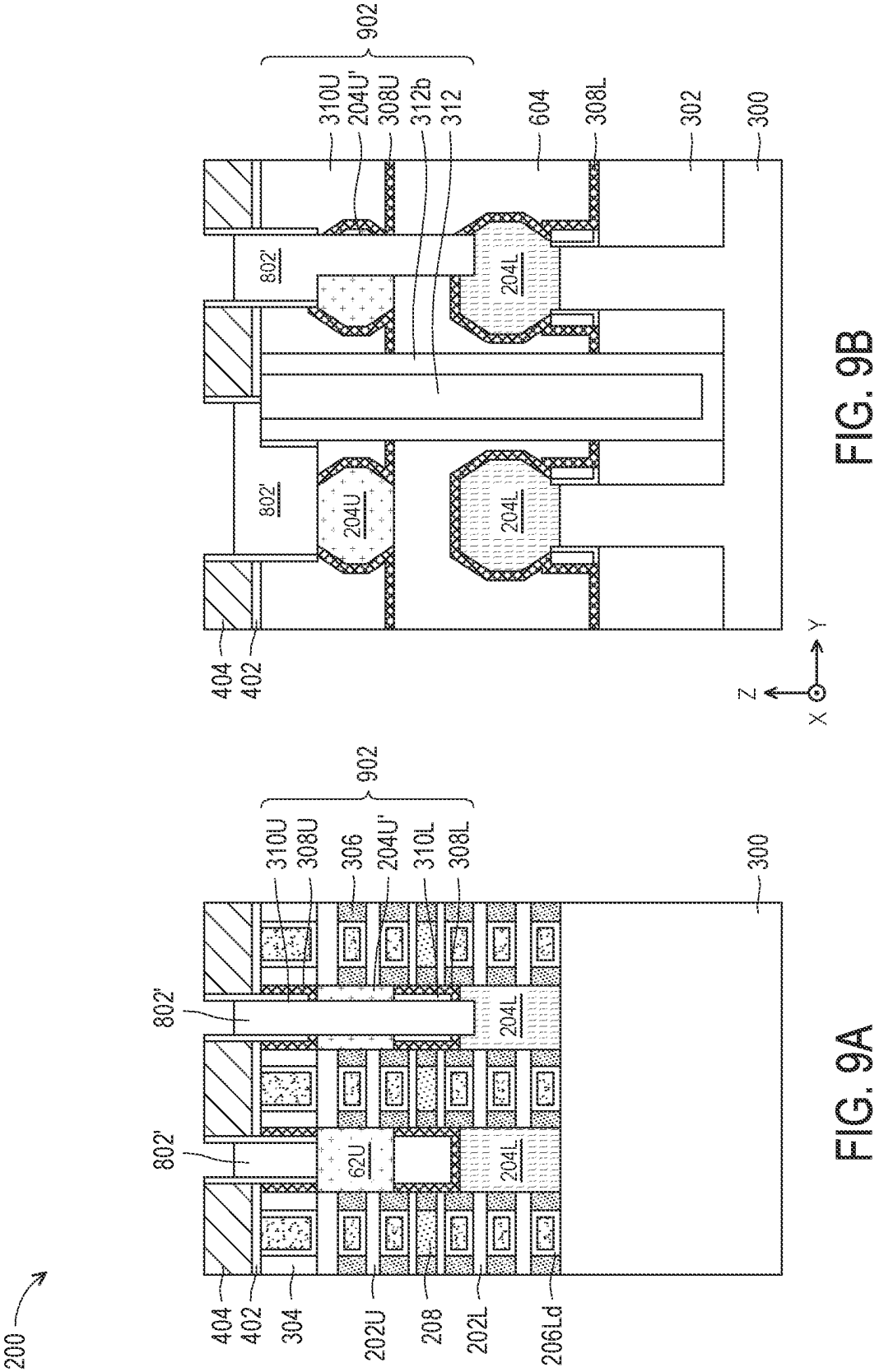
902
310U
204U'
308U
312b
312
604
308L
302
300
802'
204L
802'
204U
204L
404
402
Y
Z
X
902
310U
308U
306
204U'
310L
308L
300
802'
204L
802'
62U
204L
200
404
402
304
202U
208
202L
206Ld

FIG. 9B

FIG. 9A

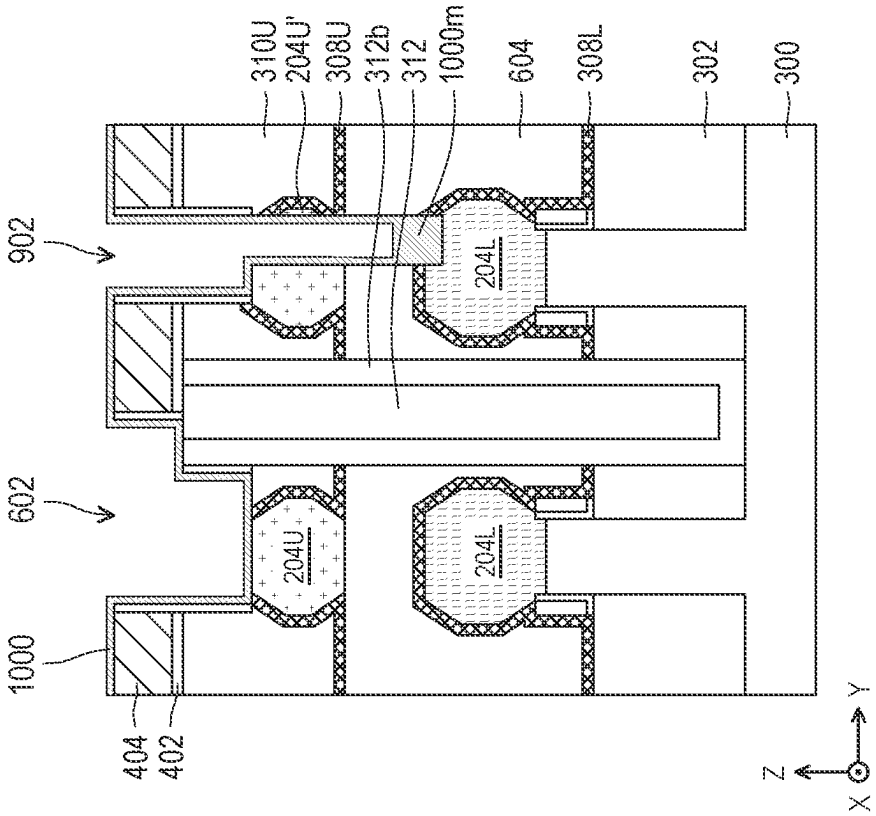

FIG. 10B

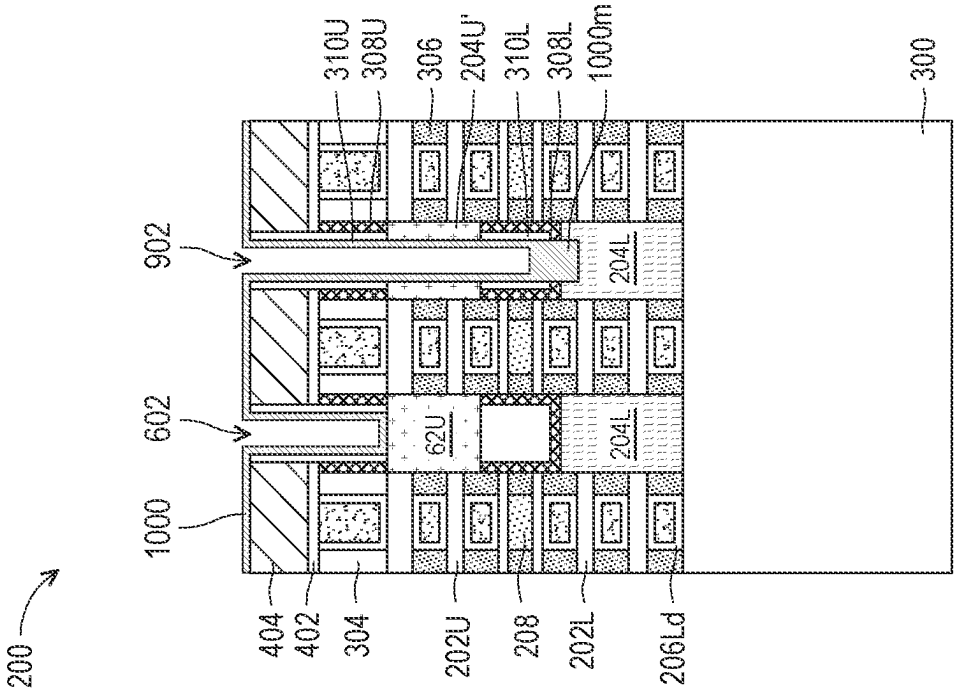

FIG. 10A

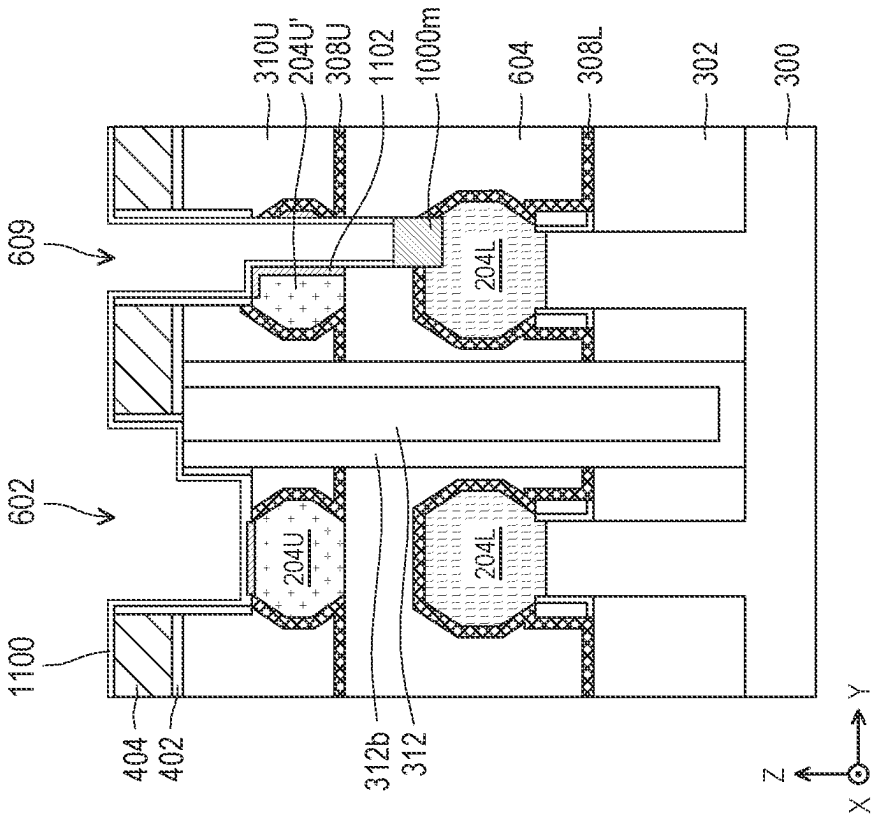

FIG. 11B

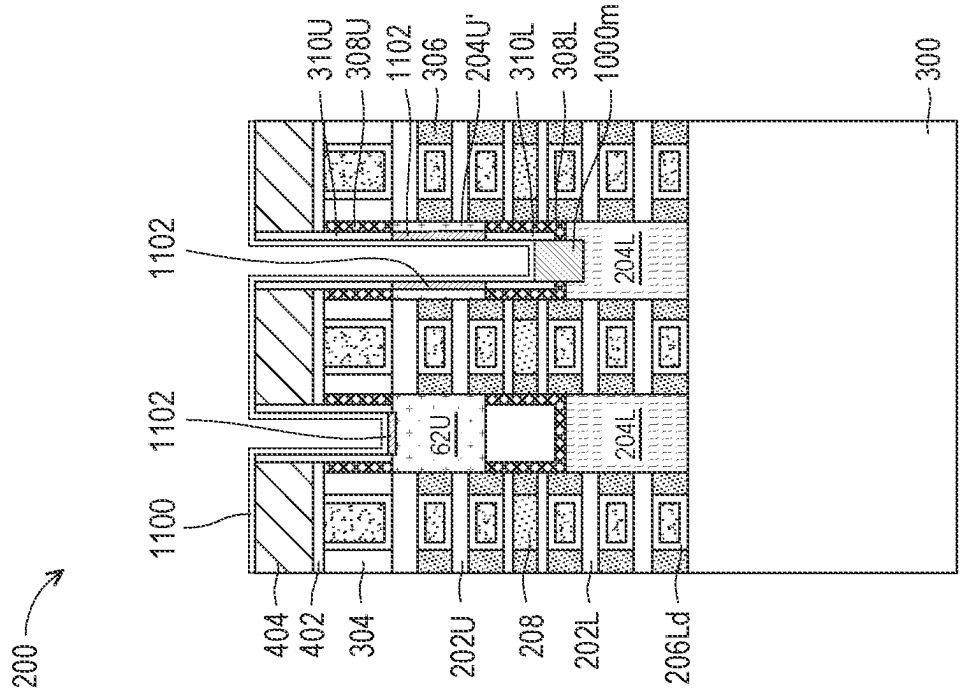

FIG. 11A

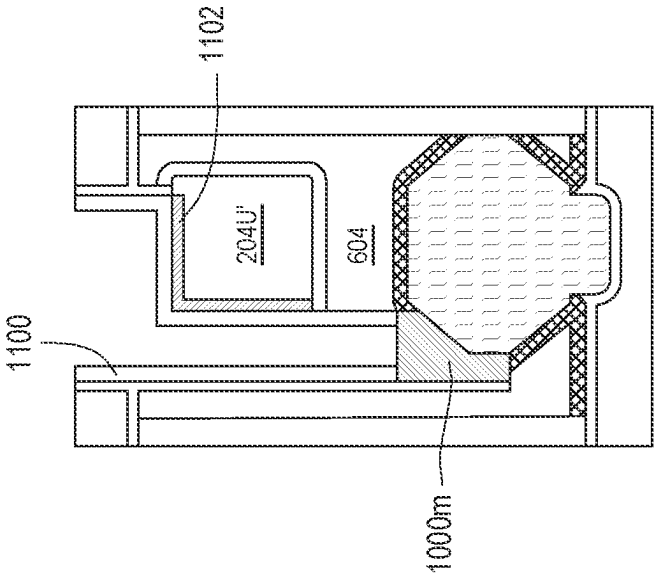

FIG. 11D

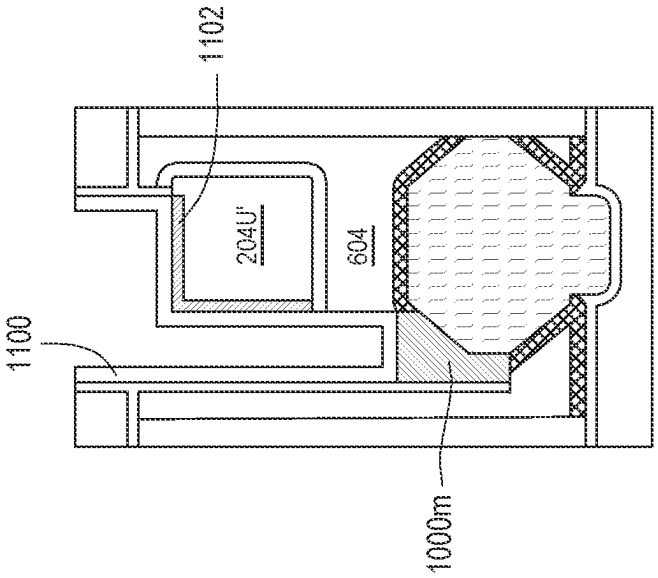

FIG. 11C

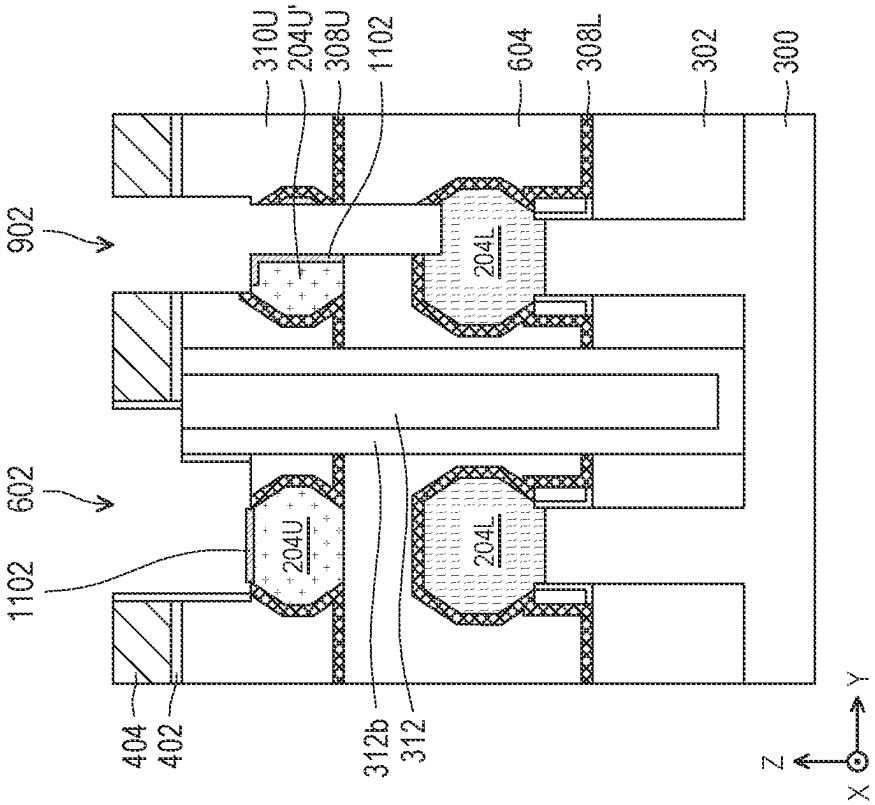

FIG. 12B

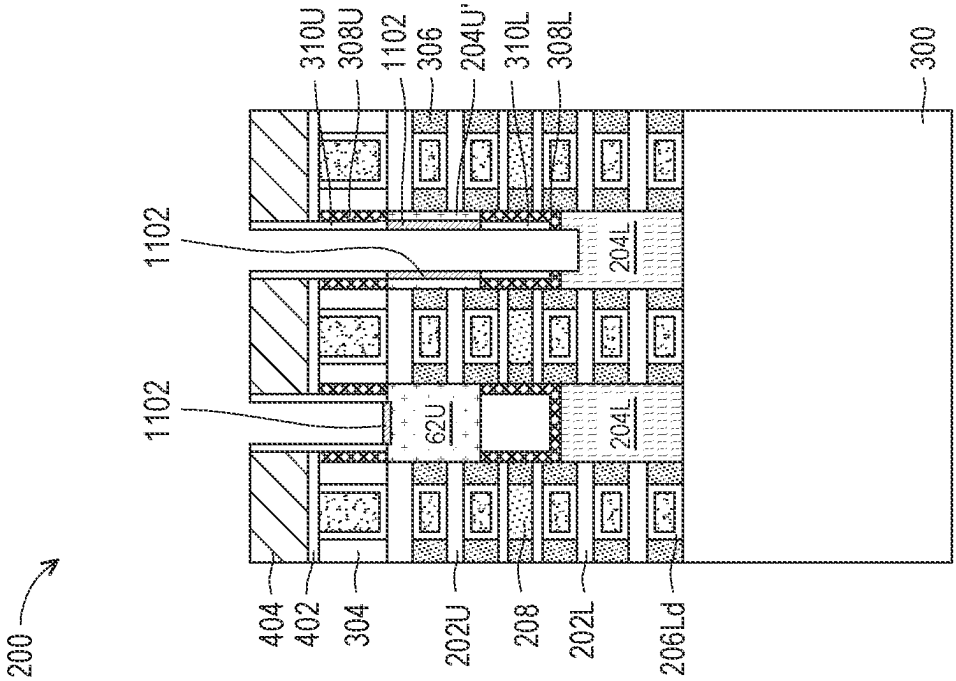

FIG. 12A

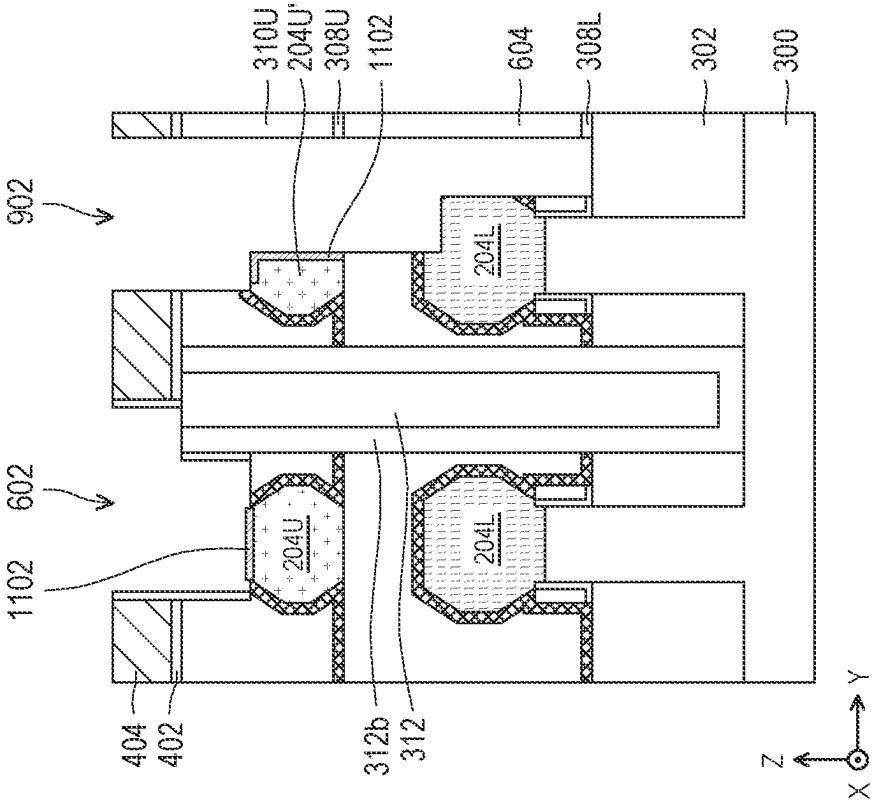

FIG. 12D

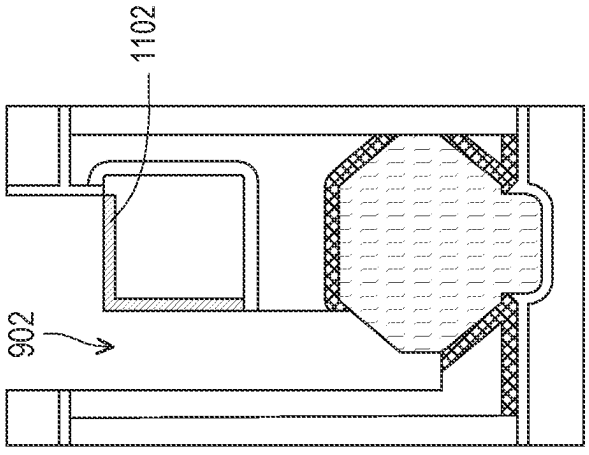

FIG. 12C

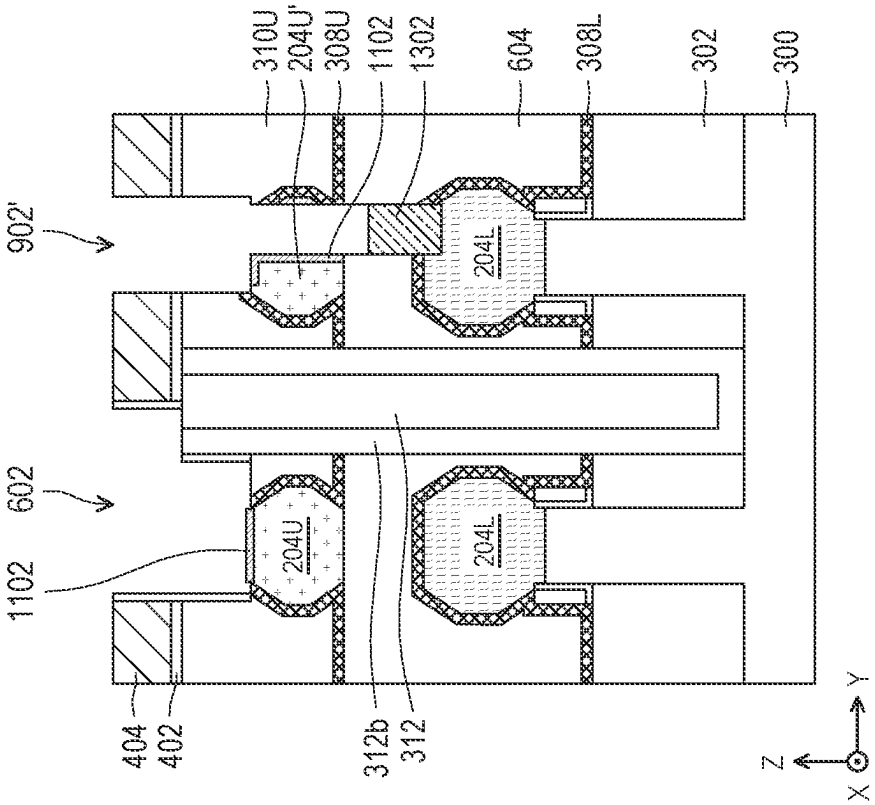

FIG. 13B

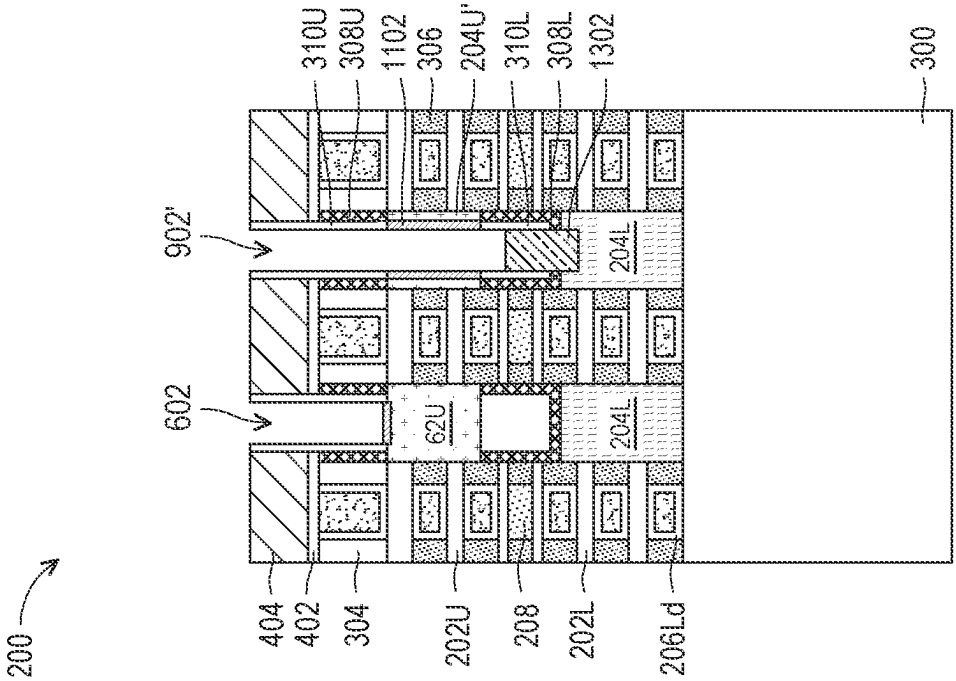

FIG. 13A

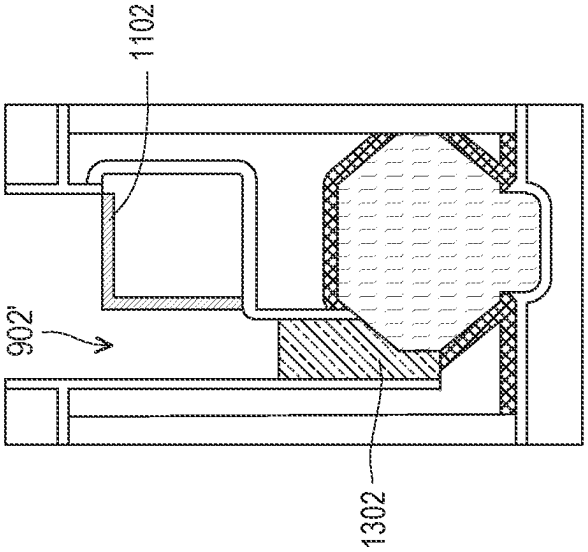

FIG. 13D

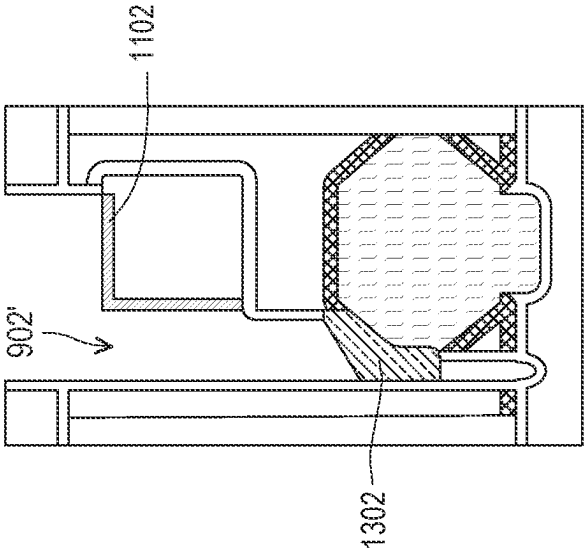

FIG. 13C

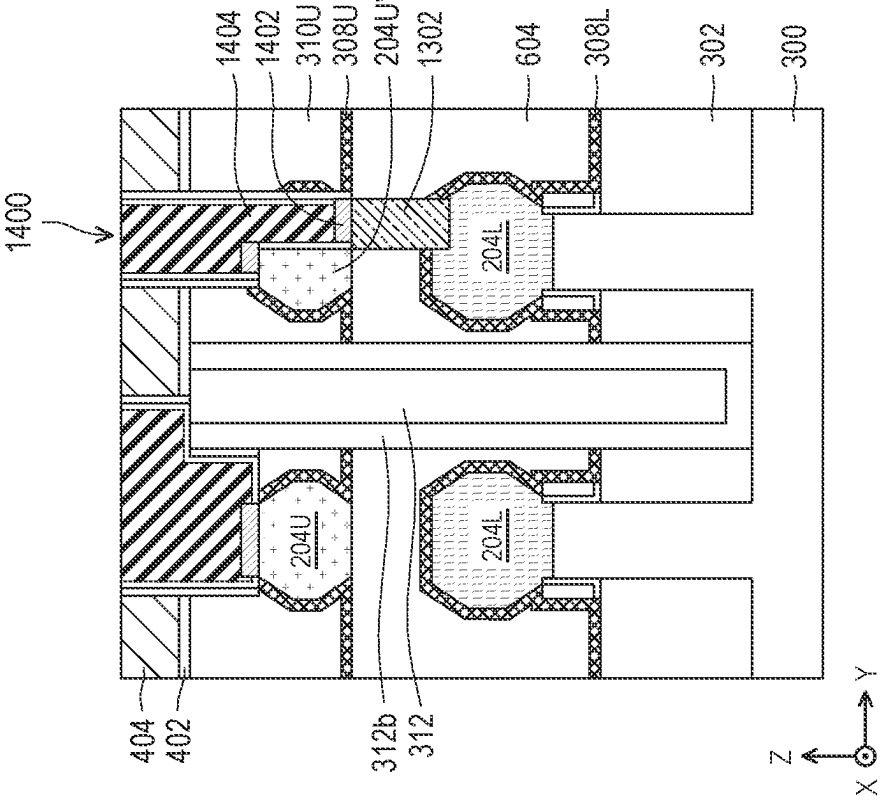

FIG. 14B

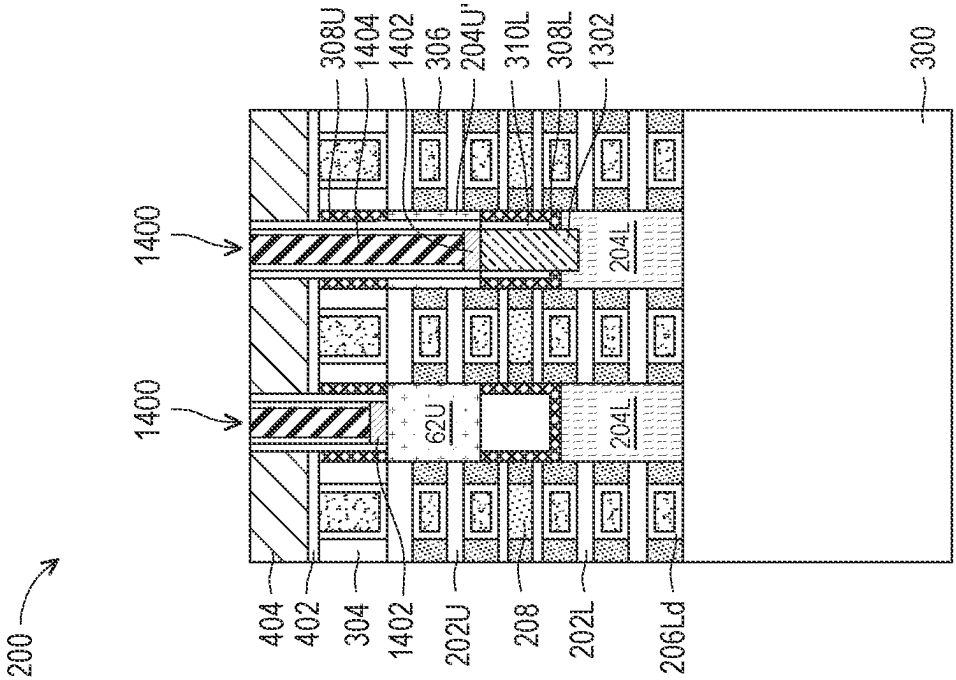

FIG. 14A

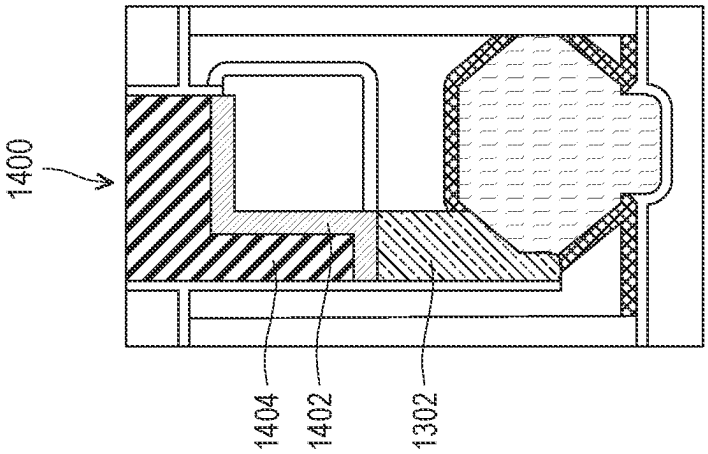

FIG. 14D

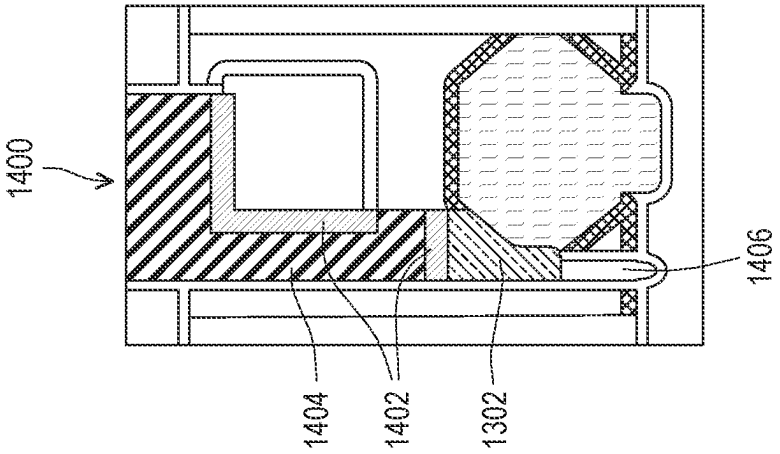

FIG. 14C

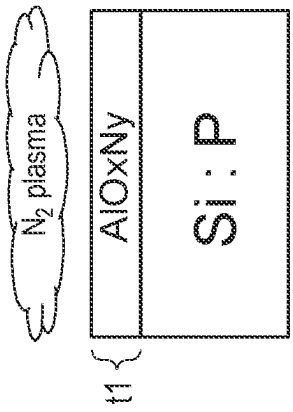

FIG. 15A

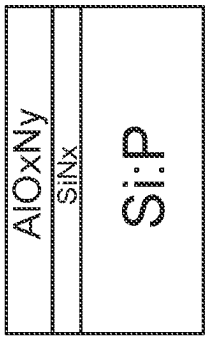

FIG. 15C

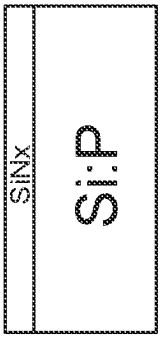

FIG. 15E

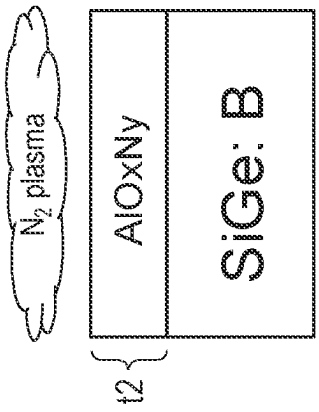

FIG. 15B

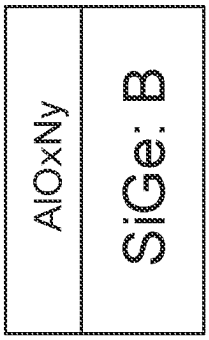

FIG. 15D

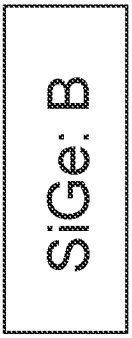

FIG. 15F

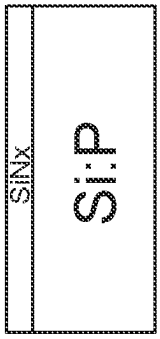

FIG. 15G

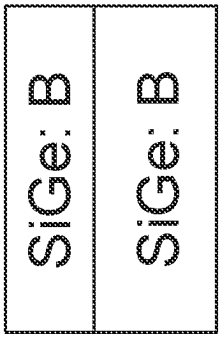

FIG. 15H

STACKED MULTI-GATE DEVICE WITH CONTACT FEATURE AND METHODS FOR FORMING THE SAME

BACKGROUND

[0001] The semiconductor integrated circuit (IC) industry has experienced exponential growth. Technological advances in IC materials and design have produced generations of ICs where each generation has smaller and more complex circuits than the previous generation. In the course of IC evolution, functional density (i.e., the number of interconnected devices per chip area) has generally increased while geometry size (i.e., the smallest component (or line) that can be created using a fabrication process) has decreased. This scaling down process generally provides benefits by increasing production efficiency and lowering associated costs. Such scaling down has also increased the complexity of processing and manufacturing ICs.

[0002] For example, as integrated circuit (IC) technologies progress towards smaller technology nodes, multi-gate devices have been introduced to improve gate control by increasing gate-channel coupling, reducing off-state current, and reducing short-channel effects (SCEs). A multi-gate device generally refers to a device having a gate structure, or portion thereof, disposed over more than one side of a channel region. And they have become popular and promising candidates for high performance and low leakage applications. A multi-gate transistor has a gate structure that can extend, partially or fully, around a channel region to provide access to the channel region on two or more sides. Because its gate structure surrounds the channel regions, some multi-gate transistors be referred to as a surrounding gate transistor (SGT) or a gate-all-around (GAA) transistor. The channel region of such transistors may be formed from nanowires, nanosheets, other nanostructures, and/or other suitable structures. The shapes of the channel region have also given transistors alternative names such as a nanosheet transistor or a nanowire transistor.

[0003] As the semiconductor industry further progresses into sub-10 nanometer (nm) technology process nodes in pursuit of higher device density, higher performance, and lower costs, challenges from both fabrication and design issues are leading to development of stacked device structure configurations, such as complementary field effect transistors (C-FET) where a first type of transistor (e.g., n-type multi-gate transistor) and a second type of transistor (e.g., p-type multi-gate transistor) are stacked vertically. While existing C-FET structures are generally adequate for their intended purposes, they are not satisfactory in all aspects.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] The present disclosure is best understood from the following detailed description when read with the accompanying figures. It is emphasized that, in accordance with the standard practice in the industry, various features are not drawn to scale and are used for illustration purposes only. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0005] FIG. **1** illustrates a flow chart of a method for forming a C-FET device including source/drain contacts, according to one or more aspects of the present disclosure.

[0006] FIG. **2** illustrates fragmentary representative perspective view of a device such as a C-FET device fabricated according to aspects of the method of FIG. **1**;

[0007] FIGS. **3**A, **4**A, **5**A, **6**A, **7**A, **8**A, **9**A, **10**A, **11**A, **12**A, **13**A, and **14**A illustrate fragmentary cross-sectional views of a device undergoing various fabrication processes in the method of FIG. **1** and along cut A-A of FIG. **2**, according to one or more aspects of the present disclosure;

[0008] FIGS. **3**B, **4**B, **5**B, **6**B, **7**B, **8**B, **9**B, **10**B, **11**B, **11**C, **11**D, **12**B, **12**C, **12**D, **13**B, **13**C, **13**D, **14**B, **14**C, and **14**D illustrate fragmentary cross-sectional views of a device undergoing various fabrication processes in the method of FIG. **1** and along cut B-B of FIG. **2**, according to one or more aspects of the present disclosure; and

[0009] FIGS. **15**A, **15**B, **15**C, **15**D, **15**E, **15**F, **15**G, **15**H illustrate fragmentary cross-sectional views of a surface of a semiconductor feature undergoing various fabrication processes according to one or more aspects of the present disclosure.

DETAILED DESCRIPTION

[0010] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0011] Spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0012] Further, when a number or a range of numbers is described with "about," "approximate," and the like, the term is intended to encompass numbers that are within a reasonable range considering variations that inherently arise during manufacturing as understood by one of ordinary skill in the art. For example, the number or range of numbers encompasses a reasonable range including the number described, such as within +/−10% of the number described, based on known manufacturing tolerances associated with manufacturing a feature having a characteristic associated with the number. For example, a material layer having a thickness of "about 5 nm" can encompass a dimension range from 4.25 nm to 5.75 nm where manufacturing tolerances associated with depositing the material layer are known to be +/−15% by one of ordinary skill in the art. Still further,

the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0013] A stacked multi-gate device refers to a semiconductor device that includes a first multi-gate device and a second multi-gate device stacked over the first multi-gate device. When the first multi-gate device and the second multi-gate device are of different conductivity types, the stacked multi-gate device may be a complementary field effect transistor (C-FET). The multi-gate devices in a C-FET may be GAA transistors. The present disclosure is illustrated through a plurality of embodiments of a C-FET device. However, one appreciates other device types that may benefit from the present disclosure.

[0014] The vertical stacking of some device types such as C-FET can create challenges providing contacts to features within the stack. In some instances, a contact feature may extend through a source/drain feature of an upper device to contact a source/drain feature of a lower device. Exposure of the top source/drain feature and the bottom source/drain feature creates challenges in selectively processing one feature, while avoiding processing of another feature. For example, additional epitaxial material may be desired on a bottom source/drain feature, but undesired on a top source/drain feature. The present disclosure provides process to selectively deposit epitaxial material on a bottom source/drain feature with minimal or no impact to the upper source/drain feature. This may allow contact metal and silicide to be effectively and efficiently formed to provide contacts having sufficiently low contact resistance to provide for a desired C-FET device.

[0015] The various aspects of the present disclosure will now be described in more detail with reference to the figures. In that regard, FIG. **1** is a flowchart illustrating method **100** for forming a device having a stacked multi-gate structure and including source/drain contacts. Method **100** is merely an example and is not intended to limit the present disclosure to what is explicitly illustrated in method **100**. Additional steps may be provided before, during and after method **100**, and some steps described can be replaced, eliminated, or moved around for additional embodiments of the method. Not all steps are described herein in detail for reasons of simplicity.

[0016] Method **100** is described below in conjunction with FIGS. **2**A-**14**B, which are fragmentary cross-sectional views of a device **200** at different stages of fabrication according to embodiments of method **100**. Throughout the present application, like reference numerals denote like features, unless otherwise excepted. Source/drain region(s) or feature (s) may refer to a source or a drain, individually or collectively dependent upon the context.

[0017] The method **100** includes a block **102** where a substrate having a semiconductor device such as a C-FET device disposed thereon is provided. For ease of reference, FIG. **2** provides a perspective view of a device **200** that is a C-FET device. The C-FET device **200** includes a lower device **200**L (e.g., a p-type transistor) and an upper device **200**U (e.g., an n-type transistor) over the lower device **200**L. The lower and upper devices may be of opposite type (e.g., n-type/p-type). The lower device **200**L includes source/drain features **204**L (e.g., p-type epitaxial source/drain features), a plurality of channel layers **202**L, and a gate structure **206**L wrapping the channel layers **202**L. The gate structure **206**L includes a gate dielectric layer **206**Ld and a gate electrode layer **206**Le. The upper device **200**U includes source/drain features **204**U (e.g., n-type epitaxial source/drain features), a plurality of channel layers **202**U, and a gate structure **206**U wrapping the channel layers **202**U. The gate structure **206**U includes a gate dielectric layer **206**Ud and a gate electrode layer **206**Ue. An isolation layer **208** is disposed between the upper device **200**U and the lower device **200**L and isolates the gate structure **206**L from the gate structure **206**U. The configuration of the device **200** is exemplary only and not intended to be limiting. For example, two channel layers **202** are illustrated in each device for ease of illustration, but any number and configuration of channel layers may be provided based on the desired implementation. It is understood that some features are omitted in this figure for ease of understanding.

[0018] The device **200** of FIG. **2** illustrates two cross-sectional cuts. A first cross-sectional cut is provided along plane A-A, which extends through the source/drain and channel regions of the C-FET device. A second cross-sectional cut is provided along plane B-B, which is through the source/drain feature of the C-FET and perpendicular to the cut A-A.

[0019] FIGS. **3**A, **4**A, **5**A, **6**A, **7**A, **8**A, **9**A, **10**A, **11**A, **12**A, **13**A, and **14**A illustrate fragmentary cross-sectional views of a device undergoing various fabrication processes in the method of FIG. **1** and along cut A-A of FIG. **2**; FIGS. **3**B, **4**B, **5**B, **6**B, **7**B, **8**B, **9**B, **10**B, **11**B, **11**C, **11**D, **12**B, **12**C, **12**D, **13**B, **13**C, **13**D, **14**B, **14**C, **14**D illustrate fragmentary cross-sectional views of a device undergoing various fabrication processes in the method of FIG. **1** and along cut B-B of FIG. **2**.

[0020] Referring now to FIGS. **3**A and **3**B, an embodiment of the device **200** including a substrate **300**, isolation regions **302** interposing portions of the substrate **300** denoted **300**' providing fin type regions (e.g., active regions) extending from the substrate **300**.

[0021] The substrate **300** may include an elementary (single element) semiconductor, such as silicon (Si), germanium (Ge), and/or other suitable materials; a compound semiconductor (i.e., alloy semiconductor), such as silicon carbide (SiC), gallium arsenic (GaAs), gallium phosphide (GaP), indium phosphide (InP), indium arsenide (InAs), indium antimonide (InSb), silicon germanium (SiGe), gallium arsenic phosphide (GaAsP), aluminum indium arsenide (AlInAs), aluminum gallium arsenide (AlGaAs), gallium indium arsenide (GaInAs), gallium indium phosphide (GaInP), gallium indium phosphide (GaInAsP), and/or other suitable materials. The substrate **300** may be a single-layer material having a uniform composition. Alternatively, the substrate may include multiple material layers having similar or different compositions suitable for IC device manufacturing. In one example, the substrate may be a silicon-on-insulator (SOI) substrate having a silicon layer formed on a buried silicon oxide (BOX) layer. In some embodiments, the substrate includes various doped regions, such as n-type wells or p-type wells. The doped regions may be doped with n-type dopants, such as phosphorus (P) or arsenic (As), and/or p-type dopants, such as boron (B) or BF_2, depending on design requirements. Doped regions may be formed by implantation of dopant atoms, in-situ doped epitaxial growth, and/or other suitable techniques. In an embodiment, the substrate **300** includes silicon (Si).

[0022] As shown in FIGS. **3**A-**3**B, each fin-shaped structure **300'** extends vertically along the Z direction from the substrate **300** and extends lengthwise along the Y direction. The fin-shaped structures **300'** may be patterned using suitable processes including double-patterning or multi-patterning processes. Generally, double-patterning or multi-patterning processes combine photolithography and self-aligned processes, allowing patterns to be created that have, for example, pitches smaller than what is otherwise obtainable using a single, direct photolithography process.

[0023] The isolation feature **302** may also be referred to as a shallow trench isolation (STI) feature **302**. The isolation feature **302** may be formed using CVD, subatmospheric CVD (SACVD), flowable CVD, spin-on coating, and/or other suitable process. Then the deposited dielectric material is planarized and/or recessed to form the isolation feature **302** having the fin structure **300'** extending there above. The dielectric material for the isolation feature **302** may include silicon oxide, silicon oxynitride, fluorine-doped silicate glass (FSG), a low-k dielectric, combinations thereof, and/or other suitable materials. The isolation feature **302** may include a multi-layer structure including for example, liner layers and fill layers.

[0024] The gate structures **206** include a gate dielectric layer **206**Ud/**206**Ld and a gate electrode layer **206**Ue/**206**Le respectively. The dielectric layer **206**Ud and/or **206**Ld is formed of high-K dielectric materials. As used and described herein, high-k dielectric materials include dielectric materials having a high dielectric constant, for example, greater than that of thermal silicon oxide (~3.9). In an implementation, the gate dielectric layer **206**Ue/**206**Le includes hafnium oxide. Alternatively, the gate dielectric layer **206**Ue/**206**Le may include other high-K dielectrics, such as titanium oxide (TiO_2), hafnium zirconium oxide (HfZrO), tantalum oxide (Ta_2O_5), hafnium silicon oxide ($HfSiO_4$), zirconium oxide (ZrO_2), zirconium silicon oxide ($ZrSiO_2$), lanthanum oxide (La_2O_3), aluminum oxide (Al_2O_3), zirconium oxide (ZrO), yttrium oxide (Y_2O_3), $SrTiO_3$ (STO), $BaTiO_3$ (BTO), BaZrO, hafnium lanthanum oxide (HfLaO), lanthanum silicon oxide (LaSiO), aluminum silicon oxide (AlSiO), hafnium tantalum oxide (HfTaO), hafnium titanium oxide (HfTiO), (Ba,Sr) TiO_3 (BST), silicon nitride (SiN), silicon oxynitride (SiON), combinations thereof, or other suitable material. The gate electrode layer **206**Ue and/or **206**Le provide a suitable work function for the respective device. In an embodiment, a p-type work function layer **206**Le and a n-type work function layer **206**Ue are provided. The gate electrode layer **206**Ue/**206**Le may include a single layer or alternatively a multi-layer structure. By way of example, the p-type work function material may include titanium nitride (TiN), tantalum nitride (TaN), ruthenium (Ru), molybdenum (Mo), aluminum (Al), tungsten nitride (WN), zirconium silicide ($ZrSi_2$), molybdenum silicide ($MoSi_2$), tantalum silicide ($TaSi_2$), nickel silicide ($NiSi_2$), other p-type work function material, or combinations thereof. The n-type work function material may include titanium (Ti), aluminum (Al), silver (Ag), manganese (Mn), zirconium (Zr), titanium aluminum (TiAl), titanium aluminum carbide (TiAlC), tantalum carbide (TaC), tantalum carbonitride (TaCN), tantalum silicide nitride (TaSiN), tantalum aluminum (TaAl), tantalum aluminum carbide (TaAlC), titanium aluminum nitride (TiAlN), other n-type work function material, or combinations thereof. In some implementations, the gate electrode layer also includes a fill metal layer such as tungsten (W), liner layer(s), adhesion layer(s), barrier layer(s), silicide layer(s), and/or other conductive structures. In some implementations, a capping layer **314** is provided over the gate **206**Ue. Gate spacers **304** and inner spacers **306** may be disposed adjacent the gate structure **206**. The spacers **304**, **306** include a dielectric material. In some embodiments, the spacers **304** and/or inner spacer features **306** include silicon oxide, silicon nitride, silicon oxycarbide, silicon oxycarbonitride, silicon carbonitride, metal nitride, silicon germanium oxide, combinations thereof, and/or other suitable dielectrics. In some implementations, the gate structure **206** is formed by a replacement gate process where a sacrificial dummy gate (e.g., polysilicon gate) is formed and subsequently removed for positioning of the gate structure **206**.

[0025] Bottom source/drain features **204**L may be formed for the lower device **200**L. The bottom source/drain features **204**L may be formed using an epitaxial process, such as vapor-phase epitaxy (VPE), ultra-high vacuum chemical vapor deposition (UHV-CVD), molecular beam epitaxy (MBE), and/or other suitable processes. The epitaxial growth process may use gaseous and/or liquid precursors, which interact with the composition of the substrate **300** (e.g., fin **300'**) as well as exposed surfaces of the channel layers **202**L. In an embodiment, the bottom source/drain features **204**L are p-type source/drain features and may include germanium, gallium-doped silicon germanium, boron-doped silicon germanium, or other suitable material and may be in-situ doped during the epitaxial process by introducing a p-type dopant, such as boron, or ex-situ doped using a junction implant process.

[0026] A bottom contact etch stop layer (CESL) **308**L and a bottom interlayer dielectric (ILD) layer **310**L are deposited over the bottom source/drain features **204**L. The bottom CESL **308**L may include silicon nitride, silicon oxynitride, and/or other materials and may be formed by CVD, ALD, plasma-enhanced chemical vapor deposition (PECVD) process and/or other suitable deposition or oxidation processes. The bottom ILD layer **310**L may include materials such as tetraethylorthosilicate (TEOS) oxide, un-doped silicate glass, or doped silicon oxide such as borophosphosilicate glass (BPSG), fused silica glass (FSG), phosphosilicateglass (PSG), boron doped silicon glass (BSG), and/or other suitable dielectric materials and may be formed by CVD, ALD, PECVD processes and/or other suitable deposition processes.

[0027] Upper source/drain features **204**U may be formed for the upper device **200**U. The upper source/drain features **204**U may be formed using an epitaxial process, such as VPE, UHV-CVD, MBE, and/or other suitable processes. The epitaxial growth process may use gaseous and/or liquid precursors, which interact with exposed surfaces of the channel layers **202**U. In an embodiment, the upper source/drain features **204**U are n-type features and may include silicon, phosphorus-doped silicon, arsenic-doped silicon, antimony-doped silicon, or other suitable material and may be in-situ doped during the epitaxial process by introducing an n-type dopant, such as phosphorus, arsenic, or antimony, or ex-situ doped using a junction implant process. An upper CESL **308**U and upper ILD layer **310**U may be formed over the source/drain features **204**U and may be substantially similar to the bottom CESL **308**L and bottom ILD layer **310**L respectively.

[0028] In some implementations, a leakage block layer includes an undoped semiconductor material, such as undoped silicon (Si), undoped silicon germanium (SiGe), or undoped germanium (Ge) that may be formed in the fin. In these embodiments, the leakage block layer may be deposited using vapor-phase epitaxy (VPE), ultra-high vacuum chemical vapor deposition (UHV-CVD), molecular beam epitaxy (MBE), and/or other suitable epitaxy deposition processes. Spacers or blocking material **318** may be disposed adjacent the bottom source/drain feature **204**L.

[0029] In some implementations, contact features of the device may include a conductive fill portion and a liner layer such as a silicon nitride. liner and a conductive fill portion may include ruthenium (Ru), nickel (Ni), cobalt (Co), copper (Cu), combinations thereof, and/or other suitable materials. The contact features may provide an interconnection to a feature of the device such as a source/drain region (e.g., **204**L).

[0030] It is noted that while the device **200** as illustrated in FIGS. **2**, **3**A, **3**B illustrates a C-FET of an exemplary configuration, other device types and other configures may also be possible. For example, in some implementations, other devices having a first epitaxial region and an overlying second epitaxial region where processing is selective between the two epitaxial regions.

[0031] The method **100** includes block **104** where dielectric layer(s) and/or hard mask layer(s) are formed over the device. Referring to the example of FIGS. **4**A and **4**B, dielectric and/or hard mask layers **402**, **404**, **406** and **408** are illustrated. In an embodiment, layer **402** is an etch stop layer. In some implementations, the layer **402** is substantially similar to the CESL **308**L and/or **308**U. In an embodiment, layer **404** is an interlayer dielectric (ILD). In some implementations, the layer **404** is substantially similar to the ILD **310**L and/or ILD **310**U. In some implementations, the layer **406** and/or **408** are patterning layers provided for reproducing a pattern from an overlying photosensitive layer such as layer **410**. In an embodiment, the layer **408** and/or **408** are a hard mask layer. In an embodiment, the layer **408** includes a-silicon. In an embodiment, layer **406** is a silicon nitride and layer **408** is a silicon oxide. Though other compositions are possible. Patterning layer **410** is disposed over the device and stack of dielectric/hard mask layers. In an embodiment, the patterning layer **410** includes a photosensitive material such as a photoresist.

[0032] Using photolithography and etching processes, the patterning layer **410** is patterned to provide a plurality of features defining a contact scheme for the device **200**. In some implementations, the contact scheme includes the contacts for the source/drain regions of the C-FET device **200**. The patterned layers are illustrated in an example at FIGS. **5**A, **5**B. The photolithography process may include photoresist coating (e.g., spin-on coating), soft baking, mask aligning, exposure, post-exposure baking, photoresist developing, rinsing, drying (e.g., spin-drying and/or hard baking), other suitable lithography techniques, and/or combinations thereof. The etching process may include dry etching (e.g., RIE etching), wet etching, and/or other etching methods. In an embodiment, the patterning processes provide openings corresponding to contact features desired for the source/drain features of the device **200**. In some implementations, at least one contact feature is provided to couple a source/drain region of the lower device with the source/drain feature of the upper device.

[0033] The method **100** includes block **106** where the source/drain contact openings are formed. In some implementations, the source/drain contact openings are provided as defined by the patterned layers of block **104**, discussed above. Referring to the example of FIGS. **6**A and **6**B, openings **602** are formed first in layers **406** and **408** above the C-FET device **200**. The openings **602** may correspond with the desired source/drain contacts. Referring to the example of FIGS. **7**A and **7**B, openings **602** are extended through the dielectric stack **402**, **404**, **406** to form openings **602** that expose a top surface of the upper source/drain feature **204**U. In some implementations, the patterning of block **106** includes patterning a source/drain contact opening extending to one or more or all of the top source/drain features of the upper device.

[0034] The method **100** includes a block **108** where a dummy patterning layer or sacrificial layer is deposited in the source/drain contact openings formed in block **106**. In some implementations, the dummy patterning layer is a bottom anti-reflective coating (BARC) material. Referring to the example of FIGS. **8**A and **8**B, the openings **602** are filled with patterning material **802**. In some implementations, a dielectric (illustrated as **308'**) may be formed between the patterning material **802** and the underlying layers. The dielectric may be substantially similar to the ILD, CESL, and/or omitted.

[0035] The method **100** includes block **110** where a select source/drain contact opening is patterned from the openings provided in block **106**. In some implementations, the patterning of block **110** includes patterning a source/drain contact opening that is intended to extend to a source/drain feature of the bottom device.

[0036] After filling the openings of block **106** with patterning material **802** in block **108**, a patterning process of block **110** is performed to define a source/drain contact opening **804** for a contact extending from the upper source/drain feature **204**U to contact the bottom source/drain feature **204**L. In some implementations, a photolithography patterning process defines the opening in patterning layers disposed over the patterning material **802**, which are used as masking elements when etching the opening **804** in the patterning material **802**. In an embodiment, the opening **804** is first etched to the upper CESL **308**U and/or the upper ILD **310**U as illustrated in FIGS. **8**A and **8**B. Portions of the upper source/drain feature **204**U are removed to provide **204**U'.

[0037] In some implementations of block **110**, the opening **804** is then extended to expose an upper surface of the bottom source/drain feature **204**L illustrated as opening **902**. The opening may continue to etch into an uppermost surface of the bottom source/drain feature **204**L to provide an overetch region as illustrated in FIGS. **9**A and **9**B, which illustrate contact opening **902'** extending into the bottom source/drain feature **204**L. In some implementations, the opening **902** exposes a sidewall of the bottom source/drain feature **204**L Sec, e.g., FIG. **12**C. In some further implementations, the opening **902** exposes a sidewall of the bottom source/drain feature **204**L and extends into dielectric materials (e.g., ILD **310**L, **308**L) below the bottom source/drain feature **204**L. See, e.g., FIG. **12**D.

[0038] After forming the opening **902** extending to the bottom source/drain feature **204**L, layer **406** may be removed from the device **200**. The dummy patterning layer **802** may be maintained and/or additional dummy patterning

layer **802'** may be included in the opening **902** extending to the bottom source/drain feature **204**L for protection during processing. The patterning material **802**, **802'** may then be removed.

[0039] The method **100** includes block **112** including forming a liner layer along the surfaces of the contact openings. In an embodiment, the liner layer is formed along the sidewalls of the contact openings and a bottom surface of the contact openings. Referring to the example of FIGS. **10**A and **10**B, a liner **1000** is deposited along the openings **602** and **902**. In an embodiment, the liner layer **1000** is deposited in openings **602** including on an exposed surface of the upper source/drain feature **204**U. In an embodiment, the liner layer **1000** is deposited in openings **902** including an exposed surface of the lower source/drain feature **204**L and exposed surface(s) of the upper source/drain feature **204**U. In an implementation, the liner layer **1000** is conformally deposited. In an embodiment, the liner layer **1000** is deposited by atomic layer deposition (ALD). An exemplary thickness of the liner layer **1000** is between approximately 1 nanometer (nm) and approximately 5 nm. In some implementations, the thickness of the liner layer **1000** is determined based on the desired conditioned or passivation region desired (discussed below), a thicker liner layer **1000** can reduce the thickness of the conditioned layer. Exemplary compositions for the liner layer **1000** include Al_2O_3, ZrO, SiN, combinations thereof, and/or other suitable dielectrics.

[0040] It is noted as illustrated in FIGS. **10**A and **10**B, the liner layer **1000** includes merged portions **1000***m* disposed at a bottom of the opening **902**. In an embodiment, the merged portion **1000***m* includes a thickness such that an upper surface of the merged portion **1000***m* is higher than an upper surface of the bottom source/drain feature **204**L. In an embodiment, the merged portion **1000***m* includes a thickness such that an upper surface of the merged portion **1000***m* is higher than the bottom CESL **308**L. In an embodiment, the merged portion **1000***m* includes a thickness (e.g., measured vertically) of between approximately 2 nm and approximately 20 nm. The merged portion **1000***m* provides a liner layer **1000** thickness adjacent the bottom source/drain feature **204**L that is greater than the thickness of the liner layer **1000** adjacent the top source/drain feature **204**U. That is, the thickness of the liner layer **1000** as measured from the surface of the epitaxial feature outwards is greater at the lower device.

[0041] The method **100** includes block **114** where a plasma treatment is performed. The plasma treatment introduces ions to the liner layer described above with reference to block **112**. In an embodiment, the plasma treatment includes introduction of nitrogen (N), oxygen (O), fluorine (F), chlorine (Cl), or other suitable plasma.

[0042] The introduction of the plasma treatment results in a plasma treated liner layer **1100**, referred to as a treated liner **1100**. The treated liner **1100** may be comprised of AlxOyNz, AlxOyFz, AlxOyClz, ZrxOyNz, ZrxOyFz, ZrxOyClz, SixNyOz, SixNyFz, SixNyClz, where x, y and z are greater than 0, and/or other suitable materials. In an embodiment, the material of the plasma treated liner layer **1100** may be the material of the liner layer **1000** having an additional atomic element originating from the plasma (e.g., N, O, F, Cl).

[0043] In some implementations, the plasma treatment forms a conformal treated layer **1100** across the device **200**. In some implementations, the plasma treatment is directional such that portions of the liner layer **1000** remain untreated. For example, the liner layer **1000** at the bottom of the opening **904** may be untreated. That is a top surface of the liner layer merged portion **1000***m* in some implementations remains untreated. See FIG. **11**D. In some implementations, a top surface of the liner layer **1000***m* is treated. See FIG. **11**C. The treated liner layer **1100** may be approximately 1 nm to 5 nm in thickness. The directional treatment may be achieved by tuning of plasma parameters power and/or bias voltage to control the treatment location including as illustrated in the present figures.

[0044] In some implementations, plasma species may penetrate the liner layer **1000** when forming the treated liner layer **1100** to provide a conditioned region **1102** of a semiconductor material underlying the liner layer **1000**. The conditioned region **1102** may also be referred to as a passivation region. As an example, the treatment of the liner layer **1000** over the upper source/drain feature **204**U may result in a conditioned region **1102** of the upper source/drain feature **204**U. In some implementations, the upper source/drain feature **204**U includes silicon composition (e.g., silicon doped with phosphorous) prior to the plasma treatment of block **114**. The conditioned region **1102** is formed of the upper source/drain feature **204**U such that the conditioned region **1102** includes silicon and one or more atomic species present in the plasma. For example, the condition region **1102** may include SiNx, SiOx, SiFx, SiClx, where x is greater than zero. In some implementations, the conditioned region **1102** interfaces a Si: P (e.g., silicon doped with P) portion of the upper source/drain feature **204**U. A thickness of the conditioned region **1102** may be approximately 1 nm to 5 nm in thickness.

[0045] In an embodiment, the treated liner layer comprises AlON; the conditioned region **1102** comprises SiN; and the upper source/drain **204** comprises silicon (e.g., epitaxially grown silicon and suitable dopants such as phosphorous).

[0046] Exemplary conditions for the plasma treatment include a treatment of between approximately 2500 seconds and approximately 4500 seconds. In an embodiment, the treatment is approximately 3600 seconds. Exemplary conditions for the plasma treatment include a treatment at a pressure between approximately 10 Pa and 150 Pa. In an embodiment, the treatment pressure is between approximately 20 Pa and 130 Pa. Exemplary conditions for the plasma treatment include a treatment at a power between approximately 1000 Watts and approximately 4000 Watts. In an embodiment, the treatment is approximately 1500 Watts. In an embodiment, the treatment is approximately 2500 Watts or 3300 Watts. In an embodiment, the plasma is approximately 2% He/N2. In an embodiment, the plasma is approximately 10% Ar/N2. In a further embodiment, the plasma is between approximately 15% Ar/N2 and approximately 25% Ar/N2.

[0047] In an embodiment, the plasma is performed with a microwave source, a source frequency of approximately 2.45 GHZ, and a source power between approximately 1 and approximately 5 KW. In an embodiment, the plasma is performed with capacitively coupled plasma (CCP), a bias frequency of approximately 13.56 MHZ, and a power of between approximately 0 and 1000 Watts.

[0048] The method **100** includes block **116** where the liner layer is removed. Block **116** may be performed after block **114**. In some embodiments, the treated portion of the liner layer and the untreated portions of the liner layer are both removed. The removal may be performed by a wet etching

process. In some implementations, the removal of the liner layer (e.g., treated and/or untreated) may be selective to other layers such as, for example, selective to the conditioned region of the upper source/drain feature such that the conditioned regions are not etched. The removal may be performed by a dilute hydrofluoric (dHF) etch. After the etching process, the conditioned region such as the region comprising a plasma introduced element (e.g., SiNx) remains on the device.

[0049] Referring to the example of FIGS. **12**A and **12**B, the liner layer **1000** and the treated liner **1100** are removed from the device **200**. The conditioned region **1102** remains on the upper source/drain feature **204**U. In some implementations, the CESL **308**L/**308**U, ILD **310**L/**310**U, dielectric layers **402** and **404** also remain substantially unetched.

[0050] The method **100** includes block **118** where an additional epitaxial growth process is performed. In an embodiment, the additional epitaxial growth process grows epitaxial material from a seed of an exposed surface of the lower source/drain feature **204**L. As illustrated in the examples of FIGS. **12**A, **12**B, **12**C and **12**D and the discussion of block **116**, the liner layer has been removed from the device **200**, which exposes a surface of the lower source/drain feature **204**L. In an embodiment, the additional epitaxial growth includes epitaxial growth of silicon and/or germanium with an p-type dopant. In an embodiment, the additional epitaxial growth includes silicon, germanium (Ge) at an atomic percentage of between approximately 20 and 60%. In a further embodiment, a boron dopant at a concentration of between approximately 1E20 and 9E20 is also provided. In some implementations, the dopant is provided in situ during the growth. The additional epitaxial material may include a same dopant type as the material of the lower source/drain feature **204**L.

[0051] During the additional epitaxial growth process, the conditioned region **1102** is provided over the upper source/drain feature **204**U. The conditioned region **1102** acts as a passivation inhibiting and/or preventing epitaxial growth on the upper source/drain feature **204**U during the additional epitaxial growth on the lower source/drain feature **204**L. Thus, in some implementations, the additional epitaxial growth can be targeted to the device type of the bottom device.

[0052] Referring to the examples of FIGS. **13**A, **13**B, **13**C, and **13**D, an additional epitaxial portion **1302** is grown on the lower source/drain feature **204**L. The additional epitaxial portion **1302** may extend to an opposing sidewall of the opening **902**. Thus, in some implementations, a portion of the opening **902** is blocked. The additional epitaxial portion **1302** reduces the depth of the previous contact opening **902** to modified contact opening **902'** having a bottom surface of a top surface of the additional epitaxial portion **1302**. The opening **902'** has an aspect ratio reduced from the opening **902**. This may provide a benefit in the gap fill of conductive material discussed below.

[0053] In some implementations, the epitaxial growth of block **118** includes a low temperature epitaxial growth. In an embodiment, the process temperature is between about 300 Celsius and 500. Celsius. In an embodiment, a low temperature epitaxial growth is considered a growth process less than approximately 600 Celsius. Exemplary precursors for the epitaxial growth include dichlorosilane (DCS), trichlorosilane (TCS), and/or other suitable precursors. In an embodiment, DCS or TCS precursors are provided in the epitaxial growth process. In some implementations, a conditioned region comprises H or Cl surfaces inhibiting growth. In an embodiment, a hydrogen-based precursor is provided in the epitaxial growth process. In some implementations, a conditioned region comprises SiH4-nCln and the hydrogen-based precursor is provided. The Clx groups are inert to the hydrogen-based precursor inhibiting growth.

[0054] The method **100** includes block **120** where the contact openings are filled with conductive material to form conductive contacts. In an embodiment, the conditioned region on the upper source/drain region is removed prior to the deposition of conductive material. The conditioned region may be removed by suitable wet etching selective to the conditioned material composition.

[0055] In some implementations, the contacts are formed by first forming a silicide layer on the upper source/drain feature **204**U and the lower source/drain feature **204**L. In an embodiment, the silicide is a titanium silicide. In some implementations, the silicide is formed concurrently or after the filling with a metal. A fill metal may include a suitable conductive material such as tungsten (W), cobalt (Co), Mo, Ru, and/or other suitable materials. Liner or barrier layers may be formed prior to the fill metal. Referring to the example of FIGS. **14**A, **14**B, **14**C, and **14**D, the openings **902'** and **602** are filled with conductive material to form source/drain contacts **1400**. The source/drain contacts include a silicide layer **1402** and a fill layer **1404**. As discussed above, one or more other conductive layers may also be included in the contacts **1400**. In an embodiment, the contact opening **902'** is filled with conductive material to provide a coupling of the upper source/drain feature **204**U and the lower source/drain feature **204**L. Depending on the growth of the additional epitaxial portion, the silicide layer **1402** may be contiguous between the upper source/drain feature **204**U and the lower source/drain feature **204**L as illustrated in FIG. **14**D. In some implementations, the opening **902'** extends below the lower source/drain feature **204**L as discussed above. In such an implementation, a gap may be disposed below the additional epitaxial portion **1302**. FIG. **14**C illustrates a gap **1406**. In an embodiment, the gap is an air gap.

[0056] One or more embodiments of the present disclosure may provide benefits of allowing selective epitaxial growth one device type. The selective growth may serve to reduce the aspect ratio that is required of the fill metal in block **120**. Further, the selective growth in some implementations provides a performance boost to the device having highly doped epitaxial material. In some implementations, there is a reduction of in the resistance of the source/drain contact e.g, Rcsd.

[0057] Referring now to FIGS. **15**A-**15**H, illustrated is an embodiment of an exemplary semiconductor feature **1502** in FIGS. **15**A, **15**C, **15**E, and **15**G and an exemplary semiconductor feature **1504** in FIGS. **15**B, **15**D, **15**F, and **15**H. In an embodiment, the semiconductor feature **1502** is an epitaxial feature suitable for a first device type. For example, in an embodiment, the semiconductor feature **1502** is an n-type epitaxial material such Si doped with phosphorous (or other suitable dopant). In an embodiment, the semiconductor feature **1502** provides a source/drain region for a transistor device such as, for example, the source/drain feature **204**U discussed above. In an embodiment, the semiconductor feature **1504** is an epitaxial feature suitable for a second device type. For example, in an embodiment, the semicon-

ductor feature **1504** is an p-type epitaxial material such Si and Ge doped with boron (or arsenic or other suitable dopant). In an embodiment, the semiconductor feature **1504** provides a source/drain region for a transistor device such as, for example, the source/drain feature **204**L discussed above. The semiconductor features **1502** and **1504** may be present on a same substrate.

[0058] A liner layer is disposed on the top surface of each of the semiconductor feature **1502** and the semiconductor feature **1504**. In an embodiment, the thickness of the liner layer formed over the semiconductor feature **1502** is T**1**. In an embodiment, the thickness of the liner layer formed over the semiconductor feature **1504** is T**2**. Thickness T**2** is greater than thickness T**1**. In an embodiment, thickness T**2** is at least two times the thickness T**1**. In an embodiment, the liner layer may be substantially similar to the liner layer **1000** discussed above. In an embodiment, the liner layer as deposited includes aluminum oxide. However, other compositions are possible including as discussed above.

[0059] In FIGS. **15**A and **15**B, a plasma treatment is performed, which may be substantially similar to the plasma treatment of block **114** of FIG. **1** discussed above. In an embodiment as illustrated the plasma is an N2 plasma. In an embodiment, the treated plasma layers include AlOxNy as illustrated in FIGS. **15**A and **15**B. However, numerous other compositions are possible including as discussed above.

[0060] FIGS. **15**C and **15**D illustrate the semiconductor features **1502** and **1504** respectively after the performance of the plasma treatment. As illustrated in FIG. **15**C, for a liner layer with thickness T**1**, a passivation or conditioned layer is formed between the plasma treated liner layer and the semiconductor feature **1502**. The conditioned layer may be formed by introduction of plasma species into the semiconductor feature **1502**, for example, by penetrating through the liner layer of thickness T**1**. In an embodiment, the conditioned layer is SixN. However, numerous other compositions are possible including as discussed above. As illustrated in FIG. **15**D, for a liner layer with thickness T**2**, the semiconductor feature **1504** is unchanged.

[0061] FIGS. **15**E and **15**F illustrate a removal of the plasma treated liner layer. In an embodiment, FIGS. **15**E and **15**F are substantially similar to block **116** of the method **100** in FIG. **1**. In some implementations, the removal is by wet etching selective to the plasma treated liner layer.

[0062] FIGS. **15**G and **15**H illustrate the semiconductor features **1502** and **1504** respectively after an epitaxial growth process. In an embodiment, the epitaxial growth process may be substantially similar to block **118** of the method **100** of FIG. **1**. In some implementations, an epitaxial material having the same dopant type as the semiconductor feature **1504** is grown. In a further embodiment, an epitaxial material including silicon, germanium, and a p-type dopant such as boron is formed on the semiconductor feature **1504**. Due to the presence of the conditioned layer (e.g., SixN) on the semiconductor feature **1502**, no or minimal epitaxial growth occurs on the semiconductor feature **1502**.

[0063] In one exemplary aspect, the present disclosure is directed to a semiconductor structure. The semiconductor structure includes a first semiconductor device and a second semiconductor device. The first semiconductor device includes a first gate structure, a first source/drain feature, and a second source/drain feature. The second semiconductor device is disposed over the first semiconductor device and includes a second gate structure, a third source/drain feature, and a fourth source/drain feature. An etch stop layer is disposed on a first surface of the first source/drain feature, wherein an epitaxial portion of the first source/drain feature has an uppermost surface above the etch stop layer. A dielectric layer is over the etch stop layer and between the first source/drain feature and the third source/drain feature. And a contact structure extends through the third source/drain feature, the etch stop layer, and the dielectric layer to the epitaxial portion of the first source/drain feature.

[0064] In a further embodiment, the contact structure includes a silicide region on the epitaxial portion of the third source/drain feature. And in some implementations, the device includes an air gap disposed below the contact structure. In an embodiment, the epitaxial portion of the first source/drain feature includes epitaxial material comprising silicon and germanium.

[0065] In yet another exemplary aspect, the present disclosure is directed to a method. The method includes forming a lower transistor comprising a first channel layer, a first gate structure around the first channel layer, and a first source/drain region. And forming an upper transistor over the lower transistor, the upper transistor comprising a second channel layer, a second gate structure around the second channel layer, and a second source/drain region. An opening is etched extending to expose a surface of the second source/drain region of the upper transistor and a surface of the first source/drain region of the lower transistor. A liner layer is conformably deposited on a sidewall and a bottom of the opening. A plasma treatment is performed on the liner layer—the plasma treatment forms a passivation layer between the liner layer and the second source/drain region of the upper transistor. After performing the plasma treatment, an epitaxial material portion is grown on the surface of the first source/drain region of the lower transistor while the passivation layer is disposed on the second source/drain region.

[0066] In a further embodiment, the method includes filling the opening with a conductive material, as the conductive material is disposed on the epitaxial material portion. In some implementations, filling the opening includes forming a silicide on the epitaxial material portion. In an embodiment, conformally depositing the liner layer includes depositing Al_2O_3, ZrO, or SiN. And in some implementations, forming the passivation layer includes SiNx, SiOx, SiFx, or SiClx where x is greater than zero.

[0067] In another of the broader embodiments, a method is provided. The method includes epitaxially growing a first epitaxial feature of silicon and a first dopant type and epitaxially growing a second epitaxial feature of silicon and a second dopant type. The second epitaxial feature is disposed above the first epitaxial feature. A surface of each of the first epitaxial feature and the second epitaxial feature is exposed. And liner layer is deposited on the exposed surfaces where the liner layer is formed having a first thickness over the first epitaxial feature and a second thickness over the second epitaxial feature, the second thickness being less than the first thickness. The method continues to perform a plasma treatment on the liner layer that forms a conditioned region between the liner layer and the second epitaxial feature. The liner layer after the plasma treatment is removed after treatment. And another epitaxial material is grown on the first epitaxial feature while the conditioned region is disposed on the second epitaxial feature.

[0068] In a further embodiment, the method includes depositing the liner layer by merging a first portion of the liner layer with a second portion of the liner layer to form the first thickness. In an embodiment, performing the plasma treatment does not form a conditioned region feature on the first epitaxial feature. In some implementations, the exposing the surface of each of the first epitaxial feature and the second epitaxial feature includes etching an opening extending from above the first epitaxial feature to the second epitaxial feature. In an embodiment, growing another epitaxial material includes a low temperature epitaxial growth process. Removing the liner layer may expose the conditioned region. And in some cases the conditioned region inhibits epitaxial growth on the second epitaxial feature during the growing another epitaxial material. In an embodiment, growing the another epitaxial material includes growing a material comprising silicon and the first dopant type. Performing the plasma treatment on the liner layer forms a treated liner layer of at least one of AlxOyNz, AlxOyFz, AlxOyClz, ZrxOyNz, ZrxOyFz, ZrxOyClz, SixNyOz, SixNyFz, or SixNyClz, where x, y and z are greater than zero.

[0069] The foregoing outlines features of several embodiments so that those of ordinary skill in the art may better understand the aspects of the present disclosure. Those of ordinary skill in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those of ordinary skill in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A semiconductor structure, comprising:

a first semiconductor device, the first semiconductor device comprising:

a first gate structure, a first source/drain feature, and a second source/drain feature;

a second semiconductor device disposed over the first semiconductor device, the second semiconductor device comprising:

a second gate structure, a third source/drain feature, and a fourth source/drain feature;

an etch stop layer disposed on a first surface of the first source/drain feature, wherein an epitaxial portion of the first source/drain feature has an uppermost surface above the etch stop layer;

a dielectric layer over the etch stop layer and between the first source/drain feature and the third source/drain feature; and

a contact structure extending through the third source/drain feature, the etch stop layer, and the dielectric layer to the epitaxial portion of the first source/drain feature.

2. The semiconductor structure of claim **1**, wherein the contact structure includes a silicide region on the epitaxial portion of the third source/drain feature.

3. The semiconductor structure of claim **1**, further comprising:

an air gap disposed below the contact structure.

4. The semiconductor structure of claim **1**, wherein the epitaxial portion of the first source/drain feature includes epitaxial material comprising silicon and germanium.

5. The semiconductor structure of claim **1**, another contact structure extending to the fourth source/drain feature.

6. The semiconductor structure of claim **1**, wherein the contact structure comprises:

a first silicide portion interfacing the third source/drain feature; and

a second silicide portion interfacing the first source/drain feature.

7. A method, comprising:

forming a lower transistor comprising a first channel layer, a first gate structure around the first channel layer, and a first source/drain region;

forming an upper transistor over the lower transistor, the upper transistor comprising a second channel layer, a second gate structure around the second channel layer, and a second source/drain region;

etching an opening extending to expose a surface of the second source/drain region of the upper transistor and a surface of the first source/drain region of the lower transistor;

conformally depositing a liner layer on a sidewall and a bottom of the opening;

performing a plasma treatment on the liner layer, wherein the plasma treatment forms a passivation layer between the liner layer and the second source/drain region of the upper transistor; and

after performing the plasma treatment, growing an epitaxial material portion on the surface of the first source/drain region of the lower transistor while the passivation layer is disposed on the second source/drain region.

8. The method of claim **7**, further comprising:

filling the opening with a conductive material, wherein the conductive material is disposed on the epitaxial material portion.

9. The method of claim **8**, wherein the filling the opening includes forming a silicide on the epitaxial material portion.

10. The method of claim **7**, wherein the conformally depositing the liner layer includes depositing Al_2O_3, ZrO, or SiN.

11. The method of claim **10**, wherein the forming the passivation layer includes SiNx, SiOx, SiFx, or SiClx where x is greater than zero.

12. A method of fabricating a semiconductor device, comprising:

epitaxially growing a first epitaxial feature, wherein the first epitaxial feature includes silicon and a first dopant type;

epitaxially growing a second epitaxial feature, wherein the second epi feature includes silicon and a second dopant type, wherein the second epitaxial feature is disposed above the first epitaxial feature;

exposing a surface of each of the first epitaxial feature and the second epitaxial feature;

depositing a liner layer on the exposed surfaces wherein the liner layer is formed having a first thickness over the first epitaxial feature and a second thickness over the second epitaxial feature, the second thickness being less than the first thickness;

performing a plasma treatment on the liner layer, wherein the performing the plasma treatment includes forming a conditioned region between the liner layer and the second epitaxial feature;

removing the liner layer after the plasma treatment; and

growing another epitaxial material on the first epitaxial feature while the conditioned region is disposed on the second epitaxial feature.

13. The method of claim **12**, wherein depositing the liner layer includes merging a first portion of the liner layer with a second portion of the liner layer to form the first thickness.

14. The method of claim **12**, wherein the performing the plasma treatment does not form a conditioned region feature on the first epitaxial feature.

15. The method of claim **12**, wherein the exposing the surface of each of the first epitaxial feature and the second epitaxial feature includes etching an opening extending from above the first epitaxial feature to the second epitaxial feature.

16. The method of claim **12**, wherein the growing another epitaxial material includes a low temperature epitaxial growth process.

17. The method of claim **16**, wherein removing the liner layer exposes the conditioned region.

18. The method of claim **16**, wherein the conditioned region inhibits epitaxial growth on the second epitaxial feature during the growing another epitaxial material.

19. The method of claim **16**, wherein the growing the another epitaxial material includes growing a material comprising silicon and the first dopant type.

20. The method of claim **11**, wherein the performing the plasma treatment on the liner layer forms a treated liner layer of at least one of AlxOyNz, AlxOyFz, AlxOyClz, ZrxOyNz, ZrxOyFz, ZrxOyClz, SixNyOz, SixNyFz, or SixNyClz, where x, y and z are greater than zero.

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