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(54) **APPARATUSES FOR TIMING CONTROL IN WRITE PATH**

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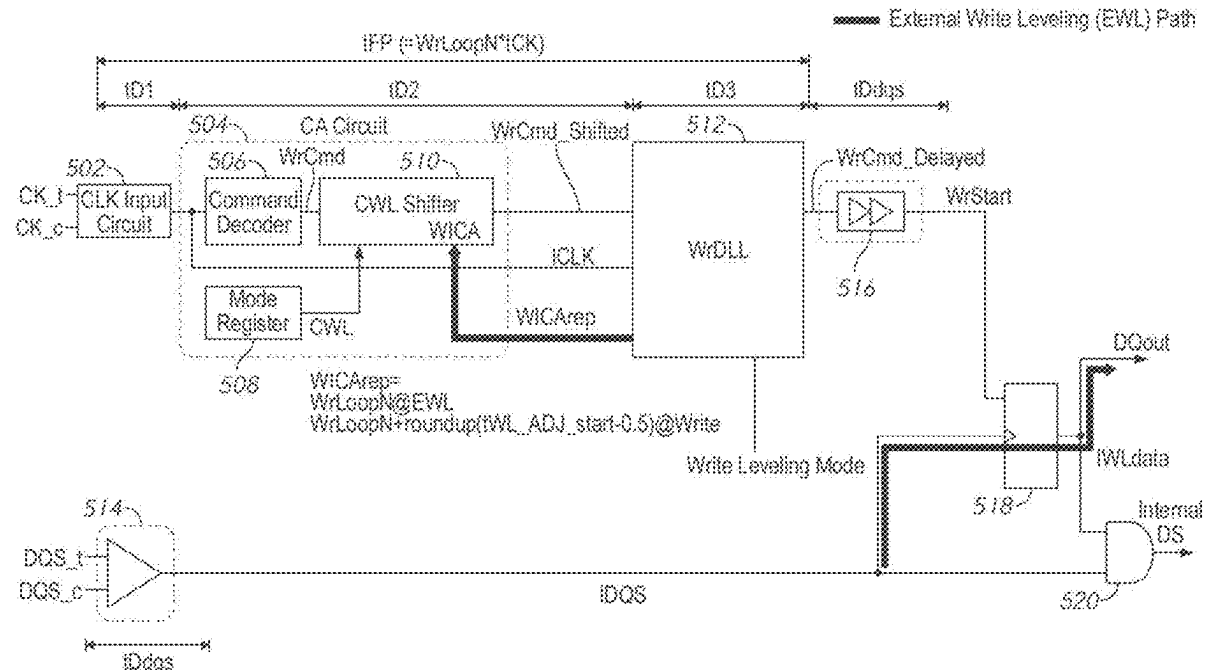
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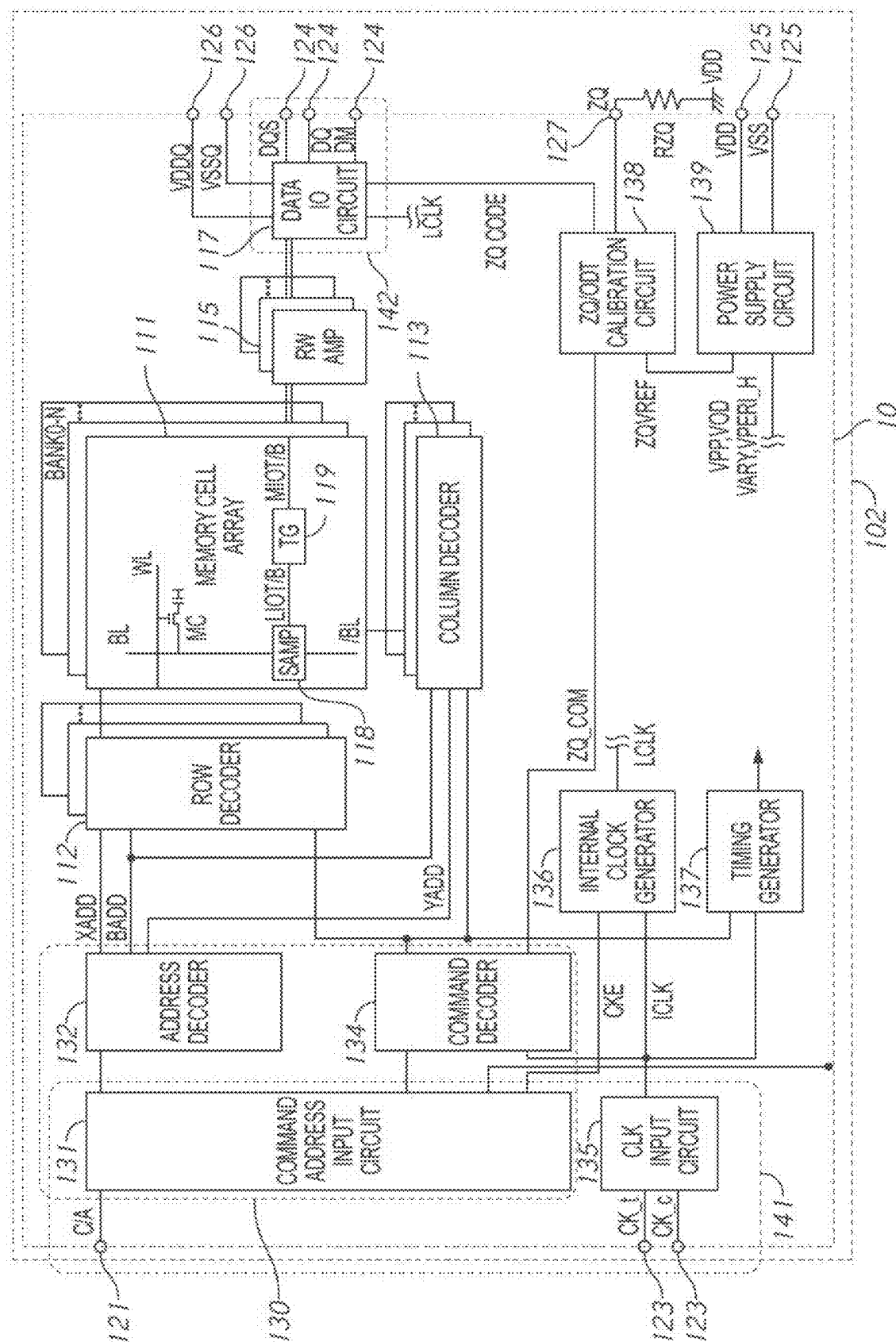
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(57) **ABSTRACT**

Apparatuses for timing control in a write path are disclosed. An example apparatus includes: a clock input circuit that receives a clock signal and provides an internal clock signal; a command decoder that receives command signals and the internal clock signal, and provides an active write command signal when the command signals indicates a write operation; a write latency shifter that receives the write command signal, a latency value and a WICA value, adjusts timing of the write command signal responsive to the latency value and the WICA value, and provides a shifted write command signal; and a write DLL including a delay line that receives the shifted write command signal and provides a delayed write command signal. The write DLL provides the WICA value to set a propagation time from the clock input circuit to the write DLL to be a multiple of a period of the clock signal.





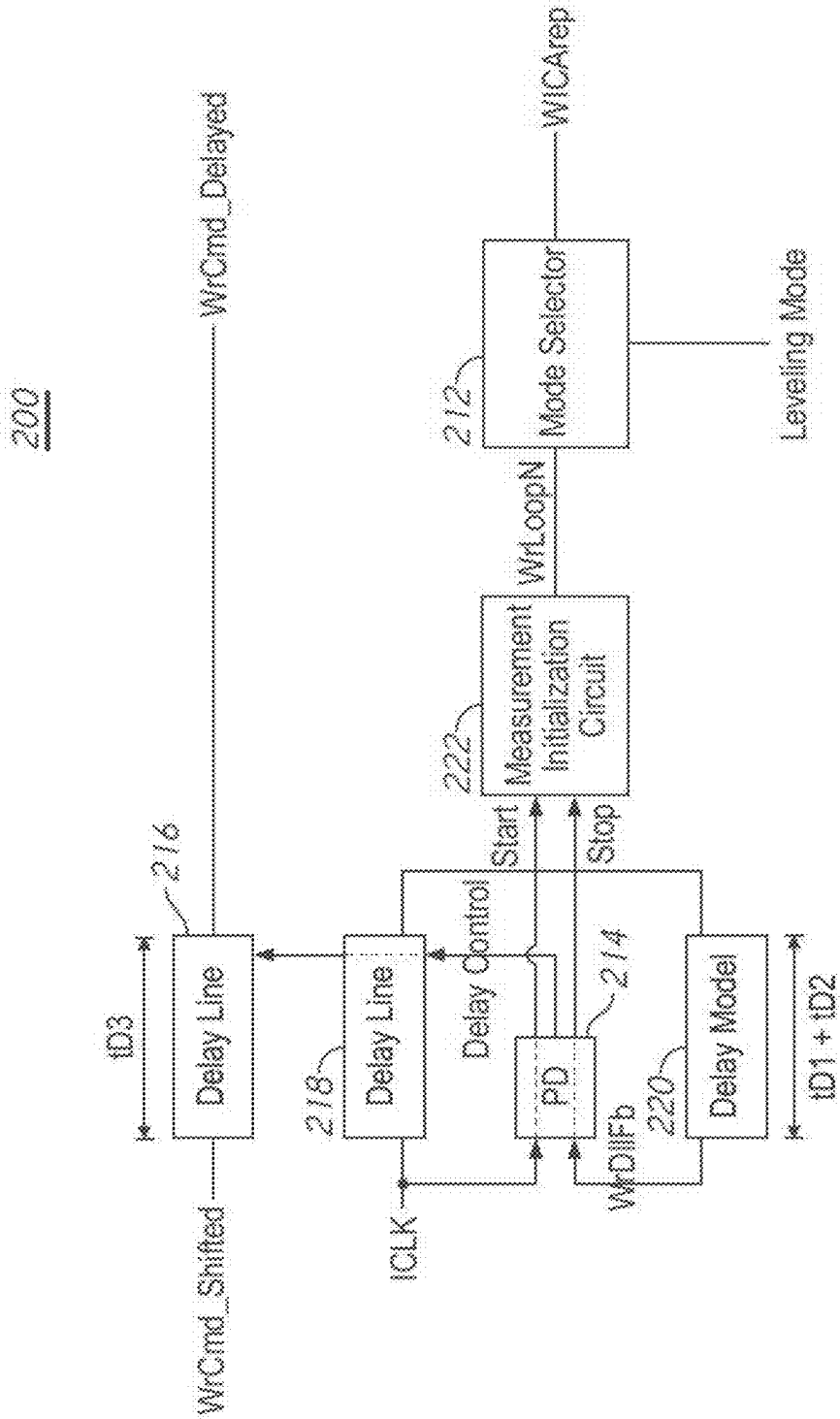
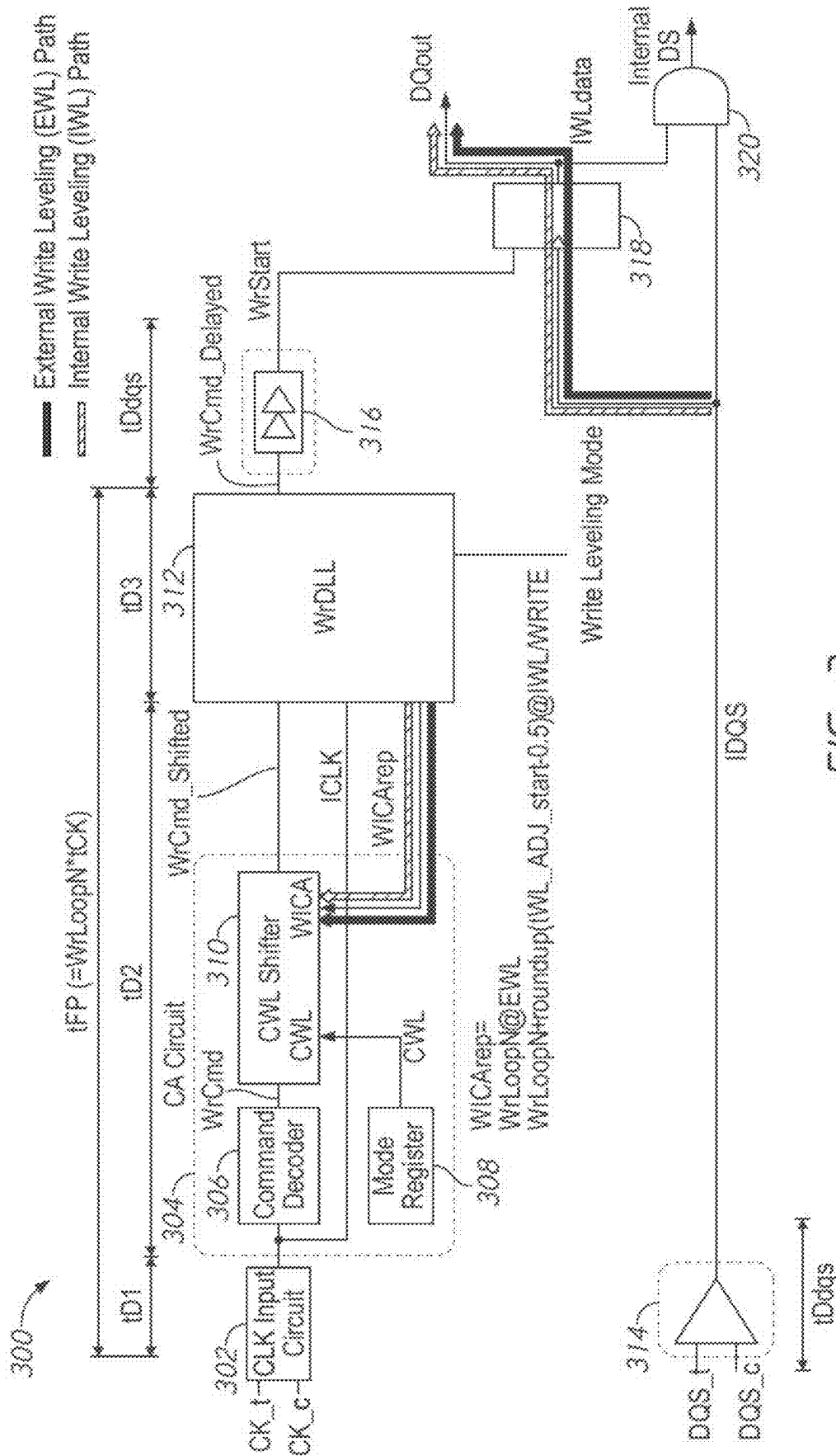


FIG. 2



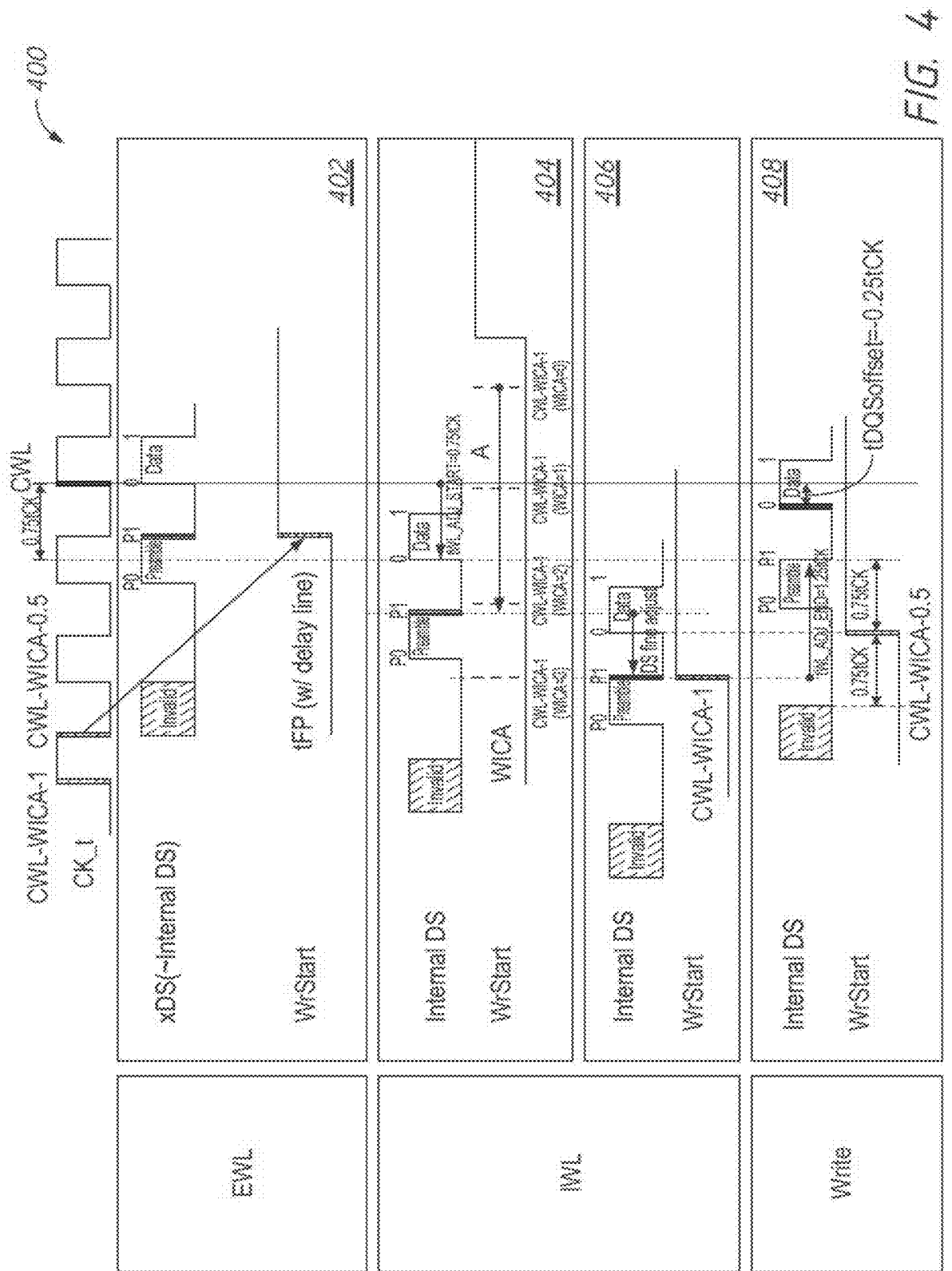
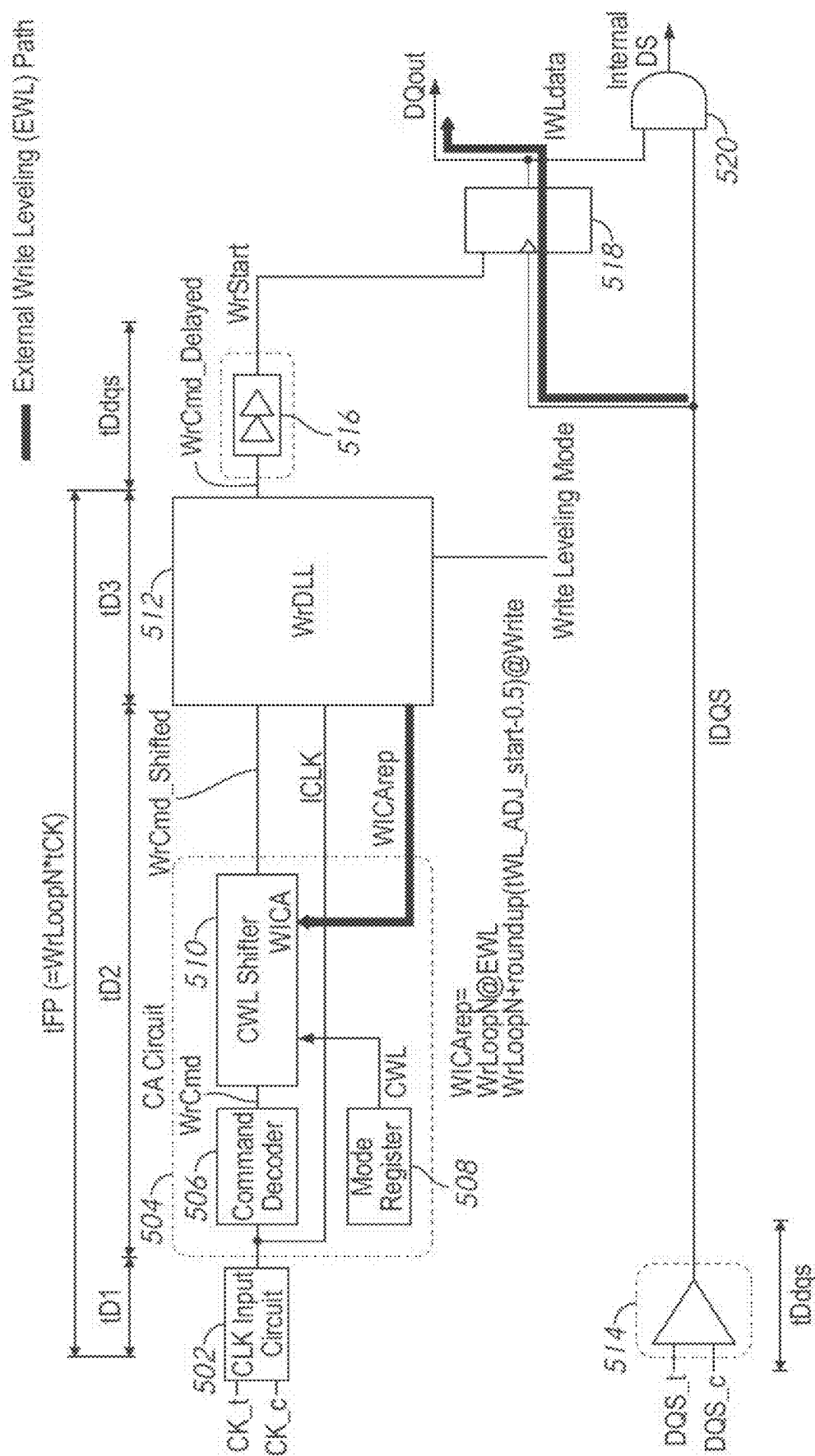
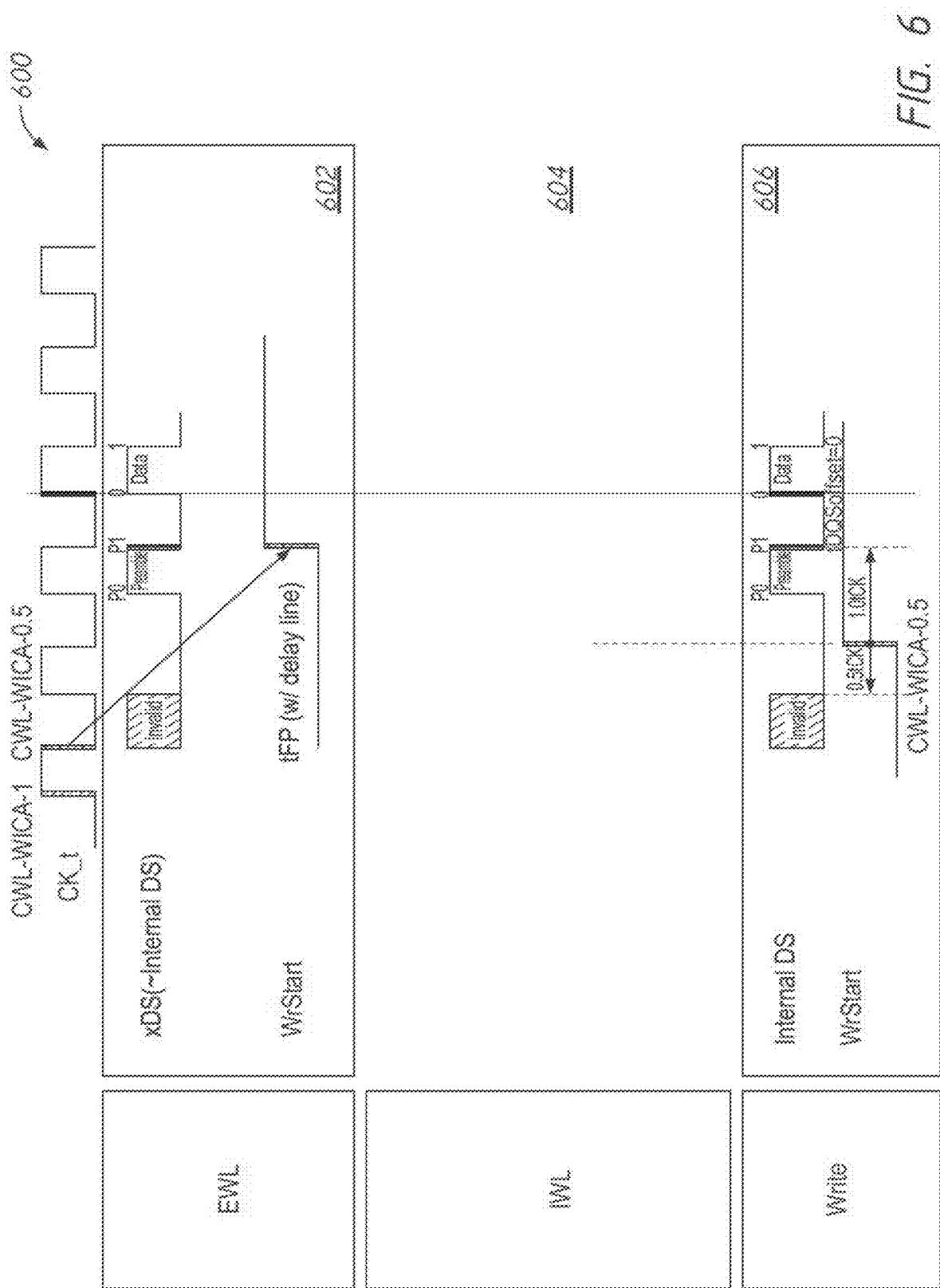


FIG. 4





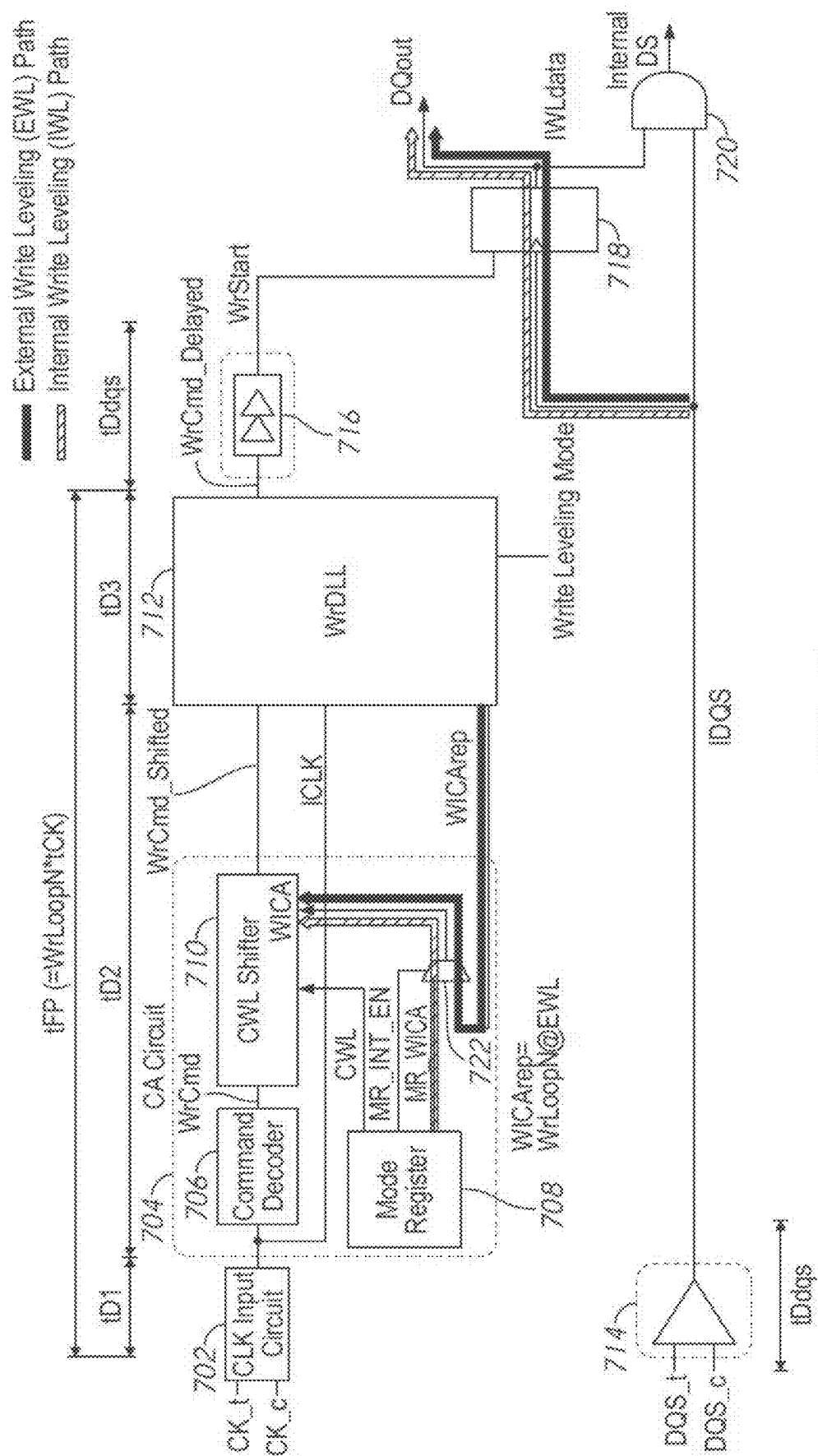
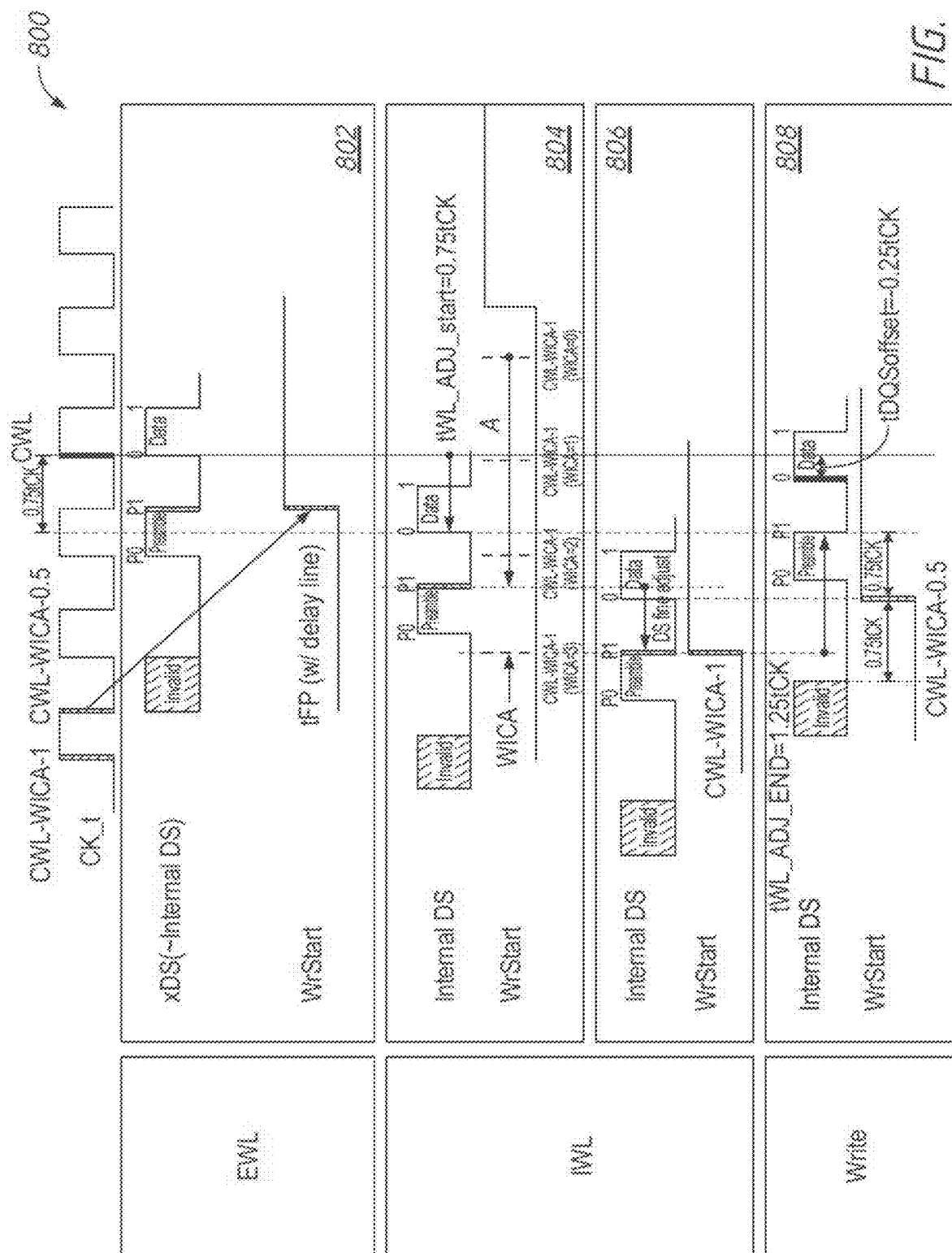


FIG. 7





## APPARATUSES FOR TIMING CONTROL IN WRITE PATH

### CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional of U.S. patent application Ser. No. 17/860,064, filed Jul. 7, 2022. This application is incorporated by reference herein in its entirety and for all purposes.

### BACKGROUND

[0002] High data reliability, high speed memory access, lower power consumption and reduced chip size are features that are demanded from semiconductor memory. To achieve higher memory access speed, operational timing in the semiconductor memory is adjusted using a clock signal (CK) and a data queue strobe signal (DQS) as reference signals.

[0003] Recent semiconductor memory includes fly-by topology layouts of commands, addresses, control signals, and timing signals, including the clock signal and the data queue strobe signal for writing data entering into memory chips. A fly-by topology layout includes fewer stubs with reduced lengths, causing less noise. However, the fly-by topology layout may cause time skews in the clock signal and the data queue strobe signal. To address the skew issues, write level training may be performed.

[0004] A flow of the write level training may include external write leveling and internal write leveling. The external write leveling of the semiconductor memory allows a memory controller outside the semiconductor memory to compensate a difference in delays due to misalignment between external clock and DQS pins. In order to perform the external write leveling, a delay that is equivalent to a command path is provided on a path for DQS.

[0005] The internal write leveling of the semiconductor memory compensates a difference in internal delays between the clock signal and the data queue strobe signal within the semiconductor memory. The semiconductor memory provides a programmable delay setting including a write leveling internal cycle alignment (WICA) that may be performed by the memory controller. A WICA value stored in a mode register is specific to each device, its write preamble setting, and the operating frequency being used. The memory controller may control delays in a write path to align with a CAS write latency (CWL) delay after a write command instructing a write operation using the write level training and the WICA value. During the internal write leveling, the delay equivalent to the command path is omitted from the path for DQS.

[0006] During the internal write leveling, the WICA setting is calculated by rounding up time delays and start up time by a cycle of the clock signal. Thus, fine adjustment of DQS calculated merely using the WICA value may be affected, and a maximum difference of the fine adjustment may be in a range of one clock cycle. Thus, a better calculation of the fine adjustment of DQS to improve an offset of the DQS may be desired.

### BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. 1 is a block diagram of a semiconductor device, according to an embodiment of the present disclosure.

[0008] FIG. 2 is a block diagram of a write delay-locked loop, according to an embodiment of the present disclosure.

[0009] FIG. 3 is a schematic diagram of a write path, according to an embodiment of the present disclosure.

[0010] FIG. 4 is a timing diagram of signals during external and internal write levelings, according to the embodiment of the present disclosure.

[0011] FIG. 5 is a schematic diagram of a write path, according to an embodiment of the present disclosure.

[0012] FIG. 6 is a timing diagram of signals during an internal write leveling, according to the embodiment of the present disclosure.

[0013] FIG. 7 is a schematic diagram of a write path, according to an embodiment of the present disclosure.

[0014] FIG. 8 is a timing diagram of signals during external and internal write levelings, according to the embodiment of the present disclosure.

### DETAILED DESCRIPTION

[0015] Various embodiments of the present disclosure will be explained below in detail with reference to the accompanying drawings. The following detailed description refers to the accompanying drawings that show, by way of illustration, specific aspects and embodiments of the disclosure. The detailed description includes sufficient detail to enable those skilled in the art to practice the embodiments of the disclosure. Other embodiments may be utilized, and structural, logical and electrical changes may be made without departing from the scope of the present disclosure. The various embodiments disclosed herein are not necessarily mutually exclusive, as some disclosed embodiments can be combined with one or more other disclosed embodiments to form new embodiments.

[0016] A write forward path includes a CWL shifter and a write delay-locked loop coupled to the CWL shifter. The write delay-locked loop provides WICA information for write level internal cycle alignment between a clock signal and a DQS signal while providing a signal indicating a start timing of a write operation from the CWL shifter with a delay controlled based on a phase difference between the clock signal and a feedback signal from a replica circuit. The write delay-locked loop actively controls its delay on the write forward path in a manner that a total propagation time of the write forward path from an input node of a clock input circuit to an output node of the write delay-locked loop becomes an integral multiple of a clock period. As a result, a time offset of the data strobe signal tDQsoffset may be controlled within a desirable range, and alignment between a clock signal and a DQS signal in a write path may be improved.

[0017] FIG. 1 is a block diagram of a semiconductor device 10 in accordance with one embodiment of the present disclosure. The semiconductor device 10 may be a dynamic random-access memory (DRAM), such as a double data rate SDRAM integrated into a single semiconductor chip, for example. The semiconductor device 10 may be mounted on an external substrate 102, for example, a memory module substrate, a mother board or the like.

[0018] As shown in FIG. 1, the semiconductor device 10 includes a memory cell array 111. The memory cell array 111 includes a plurality of banks, each bank including a plurality of word lines WL, a plurality of bit lines BL, and a plurality of memory cells MC arranged at intersections of the plurality of word lines WL and the plurality of bit lines BL. The

selection of the word line WL is performed by a row decoder **112** and the selection of the bit line BL is performed by a column decoder **113**. Sense amplifiers **118** are coupled to corresponding bit lines BL and connected to local I/O line pairs LIOT/B. Local IO line pairs LIOT/B are connected to main IO line pairs MIOT/B via transfer gates TG which function as selector circuits.

[0019] Turning to the explanation of a plurality of external terminals included in the semiconductor device **10**, the plurality of external terminals includes command/address terminals **121**, clock terminals **123**, data terminals **124**, power supply terminals **125** and **126**, and a calibration terminal ZQ **127**. An input signal block **141** may include the command/address terminals **121**. The command/address terminals **121** and signal lines coupled to the command/address terminal **121** may include a first set of terminals and signal lines that are configured to receive the command signals and a separate, second set of terminals and signal lines that configured to receive the address signals, in some examples. In other examples, the terminals **121** and signal lines associated with command/address terminals **121** may include common terminals and signal lines that are configured to receive both command signal and address signals. The input signal block **141** may include the clock terminals **123** which include input buffers. A data interface block **142** includes the data terminals **124** that will be later described, according to one embodiment. The data terminals **124** may be coupled to output buffers for read operations of memories. Alternatively, the data terminals **124** may be coupled to input buffers for read/write access of the memories. FIG. 1 shows an example of dynamic random access memory (DRAM), however, any device having external terminals for signal input/output may be included as the external terminals of embodiments of the present disclosure. Each terminal of the plurality of external terminals may include a pad. A plurality of pads in the plurality of external terminals **124** will be explained below in detail.

[0020] The semiconductor device **10** includes a command/address circuit **130**. In some embodiments, the command/address circuit **130** may include a command/address input circuit **131**, an address decoder **132** and a command decoder **134**. The command/address input circuit **131** may receive an address signal ADD and a bank address signal BADD from the command/address terminals **121** and transmit the address signal ADD and the bank address signal BADD to the address decoder **132**. The address decoder **132** may decode the address signal ADD and provide a decoded row address signal XADD to the row decoder **112**, and a decoded column address signal YADD to the column decoder **113**. The address decoder **132** also may also receive the bank address signal BADD and provide the bank address signal BADD to the row decoder **112** and the column decoder **113**.

[0021] The command/address input circuit **131** may receive a command signal from outside, such as, for example, a memory controller, at the command/address terminals **121**. The command/address input circuit **131** may provide the command signal to the command decoder **134**. The command decoder **134** may decode the command signal and generate various internal command signals. The internal command signals may be used to control operation and timing of various circuits of the semiconductor device **10**. For example, the internal command signals may include a row command signal, such as an active command, to select a word line and a column command signal, such as a read

command or a write command, to select a bit line, and a calibration signal ZQ\_COM to a ZQ calibration circuit **138**.

[0022] Accordingly, when an active command is issued with a row address and a column address is timely supplied with a read command, read data is read from a memory cell MC in the memory cell array **111** designated by these row address and column address. The read data DQ is output externally from the data terminals **124** via a read/write amplifier **115** and a data input/output circuit **117**. When the write command is issued and a column address is timely supplied with this command, and then write data DQ is supplied to the data terminals **124** in synchronization with a data strobe signal DQS while a data mask signal DM allowing masking of invalid write data is not active. The write data DQ is supplied via the data input/output circuit **117** and the read/write amplifier **115** to the memory cell array **111** and written in the memory cell MC designated by the row address and the column address.

[0023] The clock terminals **123** are supplied with external clock signals CK\_t and CK\_c, respectively. These external clock signals CK\_t and CK\_c are complementary to each other and are supplied to a clock input circuit **135**. The clock input circuit **135** receives the external clock signals CK\_t and CK\_c and generates an internal clock signal ICLK. The internal clock signal ICLK is supplied to an internal clock generator **136** and thus a phase controlled internal clock signal LCLK is generated based on the received internal clock signal ICLK and a clock enable signal CKE from the command/address input circuit **131**. The phase controlled internal clock signal LCLK is supplied to the data input/output circuit **117** and is used as a timing signal for determining an output timing of the read data DQ. The internal clock signal ICLK is also supplied to a timing generator **137** and thus various internal clock signals can be generated.

[0024] The power supply terminals **125** are supplied with power supply potentials VDD and VSS. These power supply potentials VDD and VSS are supplied to an internal power supply circuit **139**. The internal power supply circuit **139** generates various internal potentials, for example, VPP, VOD, VARY, VPERI, and a reference potential ZQVREF based on the power supply potentials VDD and VSS. The internal potential VPP is mainly used in the row decoder **112**, the internal potentials VOD and VARY are mainly used in the sense amplifiers **118** included in the memory cell array **111**, and the internal potential VPERI may be used in many other circuit blocks in a peripheral region outside the memory cell array **111**. The reference potential ZQVREF is used in the ZQ calibration circuit **138**.

[0025] The power supply terminals **126** are supplied with power supply potentials VDDQ and VSSQ. These power supply potentials VDDQ and VSSQ are supplied to the data input/output circuit **117**. The power supply potentials VDDQ and VSSQ may be the same potentials as the power supply potentials VDD and VSS that are supplied to the power supply terminals **125**, respectively. However, the power supply potentials VDDQ and VSSQ may be used for the data input/output circuit **117** so that power supply noise generated by the input/output circuit **117** does not propagate to the other circuit blocks.

[0026] The calibration terminal ZQ **127** is connected to the calibration circuit **138**. The calibration terminal ZQ **127** is also connected to an external resistor Rzo included in the external substrate **102**. The ZQ calibration circuit **138** performs a calibration operation with reference to an impedance

of the external resistance  $R_{zo}$  and the reference potential  $ZQVREF$  responsive to the calibration signal  $ZQ\_COM$  and provide an impedance code  $ZQCODE$  may be provided by the calibration operation, thus impedances of input buffers and output buffers in the data input/output circuit 117 can be adjusted.

[0027] FIG. 2 is a block diagram of a write delay-locked loop 200, according to an embodiment of the present disclosure. The write delay-locked loop 200 may include a phase detector 214, delay lines 216 and 218, a delay model 220, a measurement initialization circuit 222, and a mode selector 212. The delay line 216 may receive a shifted write command signal  $WrCmd\_Shifted$  that includes CAS write latency (CWL) adjustment (e.g., shift) from a write command signal (e.g.,  $WrCmd$  in FIG. 3) from a command/address circuit (e.g., the command/address circuit 130). The delay line 216 may receive a delay control signal from the phase detector 214 and may further provide a shifted write command signal  $WrCmd\_Shifted$  with a line delay as controlled by the delay control signal. The delay 216 has a propagation delay  $tD3$ , thus a total propagation delay (e.g.,  $tFP$  in FIGS. 3, 5 and 7) of a write forward from an input node of a clock input circuit (e.g., the clock input circuit 135) to an output node of the write delay-locked loop 200 becomes a product of a clock period  $tCK$  and a number of cycles  $WrLoopN$ . The delay 216 may receive the shifted write command signal  $WrCmd\_Shifted$  with the CWL adjustment with the line delay of the delay 216 and may provide a delayed write command  $WrCmd\_Delayed$ .

[0028] The delay line 218 may receive the internal clock signal  $ICLK$  and the control signal from the phase detector 214. The delay line 218 may provide the internal clock signal  $ICLK$  with the line delay as controlled by the delay control signal to the delay model 220. The delay model 220 may represent a delay equivalent to a sum of propagation delays on a write forward path that is described later in details referring to FIG. 3. For example, the sum of the propagation delays include a propagation delay  $tD1$  in a clock input circuit (e.g., the clock input circuit 135) and a propagation delay  $tD2$  in the command/address circuit (e.g., the command/address circuit 130). The delay model 220 may receive the internal clock signal  $ICLK$  with the line delay and provide a feedback signal  $WrDlIFb$  that is delayed by the sum of the propagation delays ( $tD1+tD2$ ).

[0029] The phase detector 214 and the measurement initialization circuit 222 may receive the feedback signal  $WrDlIFb$  and the internal clock signal  $ICLK$ . The phase detector 214 may detect a phase shift between the feedback signal  $WrDlIFb$  and the internal clock signal  $ICLK$ , and provide the delay control signal to the delay lines 216 and 218 to reduce the phase shift. The measurement initialization circuit 222 may receive the internal clock signal  $ICLK$  at a start node and the feedback signal  $WrDlIFb$  at a stop node. The measurement initialization circuit 222 may provide a number of cycles  $WrLoopN$  that indicates a number of cycles to propagate a signal in a write forward path that is described later in details referring to FIGS. 3, 5 and 7. In some embodiments, the measurement initialization circuit 222 may initially calculate the number of cycles  $WrLoopN$  when the write delay-locked loop 200 is reset. As described earlier, the phase detector 214 may provide the delay control signal to the delay lines 216 and 218 to control the delay lines 216 and 218. By controlling the delay lines 216 and 218, a total propagation time  $tFP$  of the write forward path

from an input node of the clock input circuit to an output node of the write delay-locked loop 200 that provides a delayed write command  $WrCmd\_Delayed$  becomes a product of a clock period  $tCK$  and the number of cycles  $WrLoopN$ .

[0030] The mode selector 212 may adjust the number of cycles  $WrLoopN$  to provide a number of cycles  $WICArep$  from the write delay-locked loop 200 based on a current write leveling mode that is either an external write leveling mode (EWL) or an internal write leveling mode (IWL). Adjustments of the cycles  $WICArep$  according to the current write leveling mode will be described in detail in later referring to FIGS. 3-8.

[0031] FIG. 3 is a schematic diagram of a write path 300, according to an embodiment of the present disclosure. The write path 300 includes a write forward path including a clock input circuit 302, a command/address circuit 304 and a write delay-locked loop 312.

[0032] The clock input circuit 302 may provide an internal clock signal  $ICLK$ . The clock input circuit 302 may have a propagation delay  $tD1$  from a reception of the input clock signal  $CK\_t$  to a transmission of the internal clock signal  $ICLK$ . In some embodiments, the clock input circuit 302 may include a clock input buffer without a divider. The clock input buffer may receive an input clock signal  $CK\_t$  and its complementary signal  $CK\_c$ , and may further provide the input clock signal  $CK\_t$  as the internal clock signal  $ICLK$ . In some embodiments, the clock input circuit 302 may include a clock input buffer and a divider (not shown). The clock input buffer may receive an input clock signal  $CK\_t$  and its complementary signal  $CK\_c$ , and may further provide the input clock signal  $CK\_t$ . The divider may receive the clock signal  $CK\_t$  and may further provide the internal clock signal  $ICLK$  that has a half frequency of the input clock signal  $CK\_t$ .

[0033] In some embodiments, command/address circuit 304 may be the command/address circuit 130 in FIG. 1. The command/address circuit 304 may include a command decoder 306, a CWL shifter 310 and a mode register 308. In some embodiments, the command decoder 306 may be the command decoder 134 in FIG. 1. The command decoder 306 may receive command signals from a command/address input circuit, such as the command/address input circuit 131 of FIG. 1. The command decoder 306 may receive the internal clock signal  $ICLK$  from the clock input circuit 302. The command decoder 306 may decode the command signals and may further provide a write command signal  $WrCmd$  in an active state to the CWL shifter 310, if the command signals are indicative of a write operation. The command decoder 306 may have a propagation delay  $tD2$  between a reception of the internal clocks signal  $ICLK$  and a transmission of the write command signal  $WrCmd$  based on a decoding process. In some embodiments, a delay (not shown) may be coupled in parallel to the command decoder 306 between the clock input circuit 302 and the CWL shifter 310. The delay may provide the internal clock signal  $ICLK$  with a delay equivalent to the propagation delay  $tD2$  to the write delay-locked loop 312 and the CWL shifter 310 in place of the internal clock signal  $ICLK$ .

[0034] The CWL shifter 310 may receive the write command signal  $WrCmd$  from the command decoder 306. The CWL shifter 310 may further receive the internal clock signal  $ICLK$ . The CWL shifter 310 may further receive a CAS write latency (CWL). In some embodiments, the CWL

may be provided by the mode register 308 preprogrammed by an external memory controller (not shown). In some embodiments, a number of bits representing the CWL may be seven. The CWL shifter 310 may further receive a number of cycles WICAre<sub>p</sub> from the write delay-locked loop 312 at write leveling internal cycle alignment (WICA) nodes. In some embodiments, a number of bits representing the number of cycles WICAre<sub>p</sub> may be four. The CWL shifter 310 may provide a shifted write command signal WrCmd\_Shifted that is the write command signal WrCmd with time adjustment (e.g., shift) based on a product of one cycle tCK and a number of cycles that is a difference of the CWL and the number of cycles WICAre<sub>p</sub>. The time adjustment may be performed in a manner that the CWL shifter 310 advances the received write command signal WrCmd by the number of cycles WICAre<sub>p</sub> with regards to the CWL to provide the shifted write command signal WrCmd\_Shifted.

[0035] In some embodiments, the write delay-locked loop 312 may include the write delay-locked loop 200. The write delay-locked loop 312 may receive the shifted write command signal WrCmd\_Shifted from the CWL shifter 310. The write delay-locked loop 312 may further receive the internal clock signal ICLK. The write delay-locked loop 312 may provide a delayed write command WrCmd\_Delayed as described referring to FIG. 2 from its output node.

[0036] The write path 300 may also include a DQS delay model 316 coupled to the output node of the write delay-locked loop 312. The DQS delay model 316 has a delay tDdqs equivalent to a propagation delay of a DQS input buffer 314 on a DQS path. The DQS delay model 316 may receive the delayed write command WrCmd\_Delayed and provide a write command start signal WrStart that is delayed by the tDdqs from the delayed write command WrCmd\_Delayed. The write path 300 may further include a write path output latch 318. The DQS input buffer 314 may receive a data strobe signal DQS<sub>t</sub> and its complementary signal DQS<sub>c</sub>, and provide an internal DQS signal IDQS.

[0037] The write path output latch 318 may receive the write command start signal WrStart and the internal DQS signal at a data input node and a clock input node, respectively. The write path output latch 318 may provide an internal write leveling data signal IWLdata to a data queue output node DQout responsive to the write command start signal WrStart and the internal DQS signal IDQS.

[0038] The DQS path also includes a logic circuit 320 that may receive the internal DQS signal IDQS and the internal write leveling data signal IWLdata. In some embodiments, the logic circuit 320 may be a logic AND gate. The logic circuit 320 may provide an internal data strobe signal Internal DS that is a combined signal of the internal DQS signal IDQS and the internal write leveling data signal IWLdata.

[0039] The number of cycles WICAre<sub>p</sub> may be configured in a manner that a total propagation time tFP of the write forward path from the input node of the clock input circuit 302 to the output node of the write delay-locked loop 312 becomes a product of a clock period tCK and the number of cycles WrLoopN that is described referring to FIG. 2. In some embodiments, the write delay-locked loop 312 may receive a current write leveling mode. The write delay-locked loop 312 may provide the number of cycles WICAre<sub>p</sub> by adjusting the number of cycles WrLoopN

based on a current write leveling mode that is either an external write leveling mode (EWL) or an internal write leveling mode (IWL).

[0040] FIG. 4 is a timing diagram 400 of signals during external and internal write levelings, according to the embodiment of the present disclosure. A panel 402 represents a timing relationship between the write command start signal WrStart and an external data strobe signal xDS that is similar to the internal data strobe signal Internal DS when the current write leveling mode is an external write leveling mode (EWL). The write delay-locked loop 312 may provide the number of cycles WICAre<sub>p</sub> that is the number of cycles WrLoopN responsive to the current write leveling mode being the external write leveling mode (EWL). A rising edge of the clock signal CK<sub>t</sub> representing a cycle CWL may be synchronized with a rising edge of the external data strobe signal xDS that indicates a time 0 to start data transmission. When the total propagation time tFP with the write delay-locked loop 312 is a duration of two clock periods 2 tCK, a rising edge of the write command start signal WrStart may be synchronized with a falling edge of a preamble at time PI that is half a period before the time 0 that may be delayed from a falling edge of the clock signal CK<sub>t</sub> at a cycle (CWL-WICA-0.5), when the number of cycles WICAre<sub>p</sub> is provided to the CWL shifter 310 as a WICA value.

[0041] A panel 404 represents a timing relationship between the write command start signal WrStart and the internal data strobe signal Internal DS when the current write leveling mode enters an internal write leveling mode (IWL). The WICAre<sub>p</sub> value may be adjusted, depending on a write preamble between the data strobe signals DQS<sub>t</sub> and DQS<sub>c</sub>. For example, in FIG. 4, when the write preamble is two, the write delay-locked loop 312 may provide the number of cycles WICAre<sub>p</sub> that is configured as a sum of the number of cycles WrLoopN and roundup (WL\_ADJ\_START -0.5). The time tWL\_ADJ\_START represents an offset that a memory controller applies to timings of the data strobe signals DQS<sub>t</sub> and DQS<sub>c</sub> while switching from the EWL mode to the IWL mode. In the example of the panel 404, the time tWL\_ADJ\_START is 0.75 times of the clock period (0.75 tCK). Thus, the number of cycles WICAre<sub>p</sub> is computed as {2+round up (0.75-0.5)}=3. Thus, the WICA value=3 is provided to the CWL shifter 310.

[0042] A panel 406 represents a timing relationship between the write command start signal WrStart and the internal data strobe signal Internal DS while conducting a data strobe fine adjustment in the internal write leveling mode (IWL). The internal data strobe signal Internal DS has been shifted by 0.75 tCK earlier and a falling edge of the preamble at time PI is synchronized with the rising edge of the write command start signal WrStart that corresponds to a cycle (CWL-WICA-1). The data strobe fine adjustment value DS fine adjust is computed as (-WICA+A) where A is computed as {tFP+t (WL\_ADJ\_START -0.5)}. Thus, the data strobe fine adjustment value DS fine adjust is computed as (-3+2+0.75-0.5) tCK=-0.75 tCK.

[0043] A panel 408 represents a timing relationship between the write command start signal WrStart and the internal data strobe signal Internal DS after the internal write leveling mode (IWL). WICA training starts with an offset that is set to "0". By the time the internal write leveling ends at the time tWL\_ADJ\_END, that is 1.25 tCK, the rising edge of the internal data strobe signal Internal DS that corresponds to the time 0 to start data transmission is 0.25 tCK

earlier than the initial time 0 in the panel 402. Thus, a time offset of the data strobe signal tDQSoffset is controlled to  $-0.25\text{ tCK}$ .

[0044] As described earlier, FIG. 4 illustrated a case when the write preamble is two and the time tWL\_ADJ\_START is  $0.75\text{ tCK}$ . When the write preamble is two and the time tWL\_ADJ\_START is  $-0.75\text{ tCK}$ , the time offset of the data strobe signal tDQSoffset is controlled to  $-0.25\text{ tCK}$ . When the write preamble is three and the time tWL\_ADJ\_START is  $-1.25\text{ tCK}$ , the time offset of the data strobe signal tDQSoffset is controlled to  $0.25\text{ tCK}$ . When the write preamble is four and the time tWL\_ADJ\_START is  $-2.25\text{ tCK}$ , the time offset of the data strobe signal tDQSoffset is controlled to  $0.25\text{ tCK}$ .

[0045] Because the number of cycles WICAreP may be configured in a manner that a total propagation time tFP of the write forward path from the input node of the clock input circuit 302 to the output node of the write delay-locked loop 312 becomes a product of a clock period tCK and the number of cycles WrLoopN. Depending on the write preamble and the time tWL\_ADJ\_START, the time offset of the data strobe signal tDQSoffset can be controlled to  $-0.25\text{ tCK}$  or  $0.25\text{ tCK}$ .

[0046] A write delay-locked loop provides WICA information for write level internal cycle alignment between a clock signal and a DQS signal. A time offset of the data strobe signal tDQSoffset is controlled within a desirable range, thus alignment between a clock signal and a DQS signal in a write path may be improved without the WICA information programmed by an external memory controller on a mode register.

[0047] In some embodiments, an internal write leveling may not be performed after an external write leveling. FIG. 5 is a schematic diagram of a write path 500, according to an embodiment of the present disclosure. The write path 500 includes a write forward path including a clock input circuit 502, a command/address circuit 504 and a write delay-locked loop 512.

[0048] The clock input circuit 502 may provide an internal clock signal ICLK. The clock input circuit 502 may have a propagation delay tD1 from a reception of the input clock signal CK\_t to a transmission of the internal clock signal ICLK. In some embodiments, the clock input circuit 502 may include a clock input buffer without a divider. The clock input buffer may receive an input clock signal CK\_t and its complementary signal CK\_c, and may further provide the input clock signal CK\_t as the internal clock signal ICLK. In some embodiments, the clock input circuit 502 may include a clock input buffer and a divider (not shown). The clock input buffer may receive an input clock signal CK\_t and its complementary signal CK\_c, and may further provide the input clock signal CK\_t. The divider may receive the clock signal CK\_t and may further provide the internal clock signal ICLK that has a half frequency of the input clock signal CK\_t.

[0049] In some embodiments, command/address circuit 504 may be the command/address circuit 130 in FIG. 1. The command/address circuit 504 may include a command decoder 506, a CWL shifter 510 and a mode register 508. In some embodiments, the command decoder 506 may be the command decoder 134 in FIG. 1. The command decoder 506 may receive the internal clock signal ICLK and command signals from a command/address input circuit, such as the command/address input circuit 131 of FIG. 1. The command

decoder 506 may decode the command signals and may further provide a write command signal WrCmd in an active state to the CWL shifter 510, if the command signals are indicative of a write command. The command decoder 506 may have a propagation delay tD2 between a reception of the internal clocks signal ICLK and a transmission of the write command signal WrCmd based on a decoding process. In some embodiments, a delay (not shown) may be coupled in parallel to the command decoder 506 between the clock input circuit 502 and the CWL shifter 510. The delay may provide the internal clock signal ICLK with a delay equivalent to the propagation delay tD2 to the write delay-locked loop 512 and the CWL shifter 510 in place of the internal clock signal ICLK.

[0050] The CWL shifter 510 may receive the write command signal WrCmd from the command decoder 506. The CWL shifter 510 may further receive the internal clock signal ICLK. The CWL shifter 510 may further receive a CAS write latency (CWL), that is a number of clock cycles equivalent to a propagation delay tFP in a write forward path from a reception of clock signals by the clock input circuit 502 to a transmission of a signal provided by the write delay-locked loop 512. In some embodiments, the CWL may be provided by the mode register 508 preprogrammed by an external memory controller (not shown). In some embodiments, a number of bits representing the CWL may be seven. The CWL shifter 510 may further receive a number of cycles WICAreP from the write delay-locked loop 512 at write leveling internal cycle alignment (WICA) nodes. In some embodiments, a number of bits representing the number of cycles WICAreP may be four. The CWL shifter 510 may provide a shifted write command signal WrCmd\_Shifted that is the write command signal WrCmd with time adjustment (e.g., shift) based on a product of one cycle tCK and a number of cycles that is a difference of the CWL and the number of cycles WICAreP. The time adjustment may be performed in a manner that the CWL shifter 510 advances the received write command signal WrCmd by the number of cycles WICAreP with regards to the CWL to provide the shifted write command signal WrCmd\_Shifted.

[0051] In some embodiments, the write delay-locked loop 512 may include the write delay-locked loop 200. The write delay-locked loop 512 may receive the shifted write command signal WrCmd\_Shifted from the CWL shifter 510. The write delay-locked loop 512 may further receive the internal clock signal ICLK. The write delay-locked loop 512 may provide a delayed write command WrCmd\_Delayed as described referring to FIG. 2 from its output node.

[0052] The write path 500 may also include a DQS delay model 516 coupled to the output node of the write delay-locked loop 512. The DQS delay model 516 has a delay tDdqs equivalent to a propagation delay of a DQS input buffer 514 on a DQS path. The DQS delay model 516 may receive the delayed write command WrCmd\_Delayed and provide a write command start signal WrStart that is delayed by the tDdqs from the delayed write command WrCmd\_Delayed. The write path 500 may further include a write path output latch 518. The DQS input buffer 514 may receive a data strobe signal DQS\_t and its complementary signal DQS\_c, and provide an internal DQS signal IDQS.

[0053] The write path output latch 518 may receive the write command start signal WrStart and the internal DQS signal at a data input node and a clock input node, respectively. The write path output latch 518 may provide an

internal write leveling data signal IWLdata to a data queue output node DQout responsive to the write command start signal WrStart and the internal DQS signal IDQS.

**[0054]** The DQS path also includes a logic circuit **520** that may receive the internal DQS signal IDQS and the internal write leveling data signal IWLdata. In some embodiments, the logic circuit **520** may be a logic AND gate. The logic circuit **520** may provide an internal data strobe signal Internal DS that is a combined signal of the internal DQS signal IDQS and the internal write leveling data signal IWLdata.

**[0055]** The number of cycles WICArep may be configured in a manner that a total propagation time tFP of the write forward path from the input node of the clock input circuit **502** to the output node of the write delay-locked loop **512** becomes a product of a clock period tCK and the number of cycles WrLoopN that is described referring to FIG. **2**. In some embodiments, the write delay-locked loop **512** may receive a current write leveling mode. The write delay-locked loop **512** may provide the number of cycles WICArep by adjusting the number of cycles WrLoopN when a current write leveling mode is an external write leveling mode (EWL).

**[0056]** FIG. **6** is a timing diagram **600** of signals during external write leveling, according to the embodiment of the present disclosure. A panel **602** represents a timing relationship between the write command start signal WrStart and an external data strobe signal xDS that is similar to the internal data strobe signal Internal DS when the current write leveling mode is an external write leveling mode (EWL). The write delay-locked loop **512** may provide the number of cycles WICArep that is the number of cycles WrLoopN responsive to the current write leveling mode being the external write leveling mode (EWL). A rising edge of the clock signal CK\_t representing a cycle CWL may be synchronized with a rising edge of the external data strobe signal xDS that indicates a time **0** to start data transmission. When the total propagation time tFP with the write delay-locked loop **512** is a duration of two clock periods 2 tCK, a rising edge of the write command start signal WrStart may be synchronized with a falling edge of a preamble at time PI that is half a period before the time **0** that may be delayed from a falling edge of the clock signal CK\_t at a cycle (CWL-WICA-0.5), when the number of cycles WICArep is provided to the CWL shifter **510** as a WICA value. A panel **604** represents that an internal write leveling is skipped.

**[0057]** A panel **606** represents a timing relationship between the write command start signal WrStart and the internal data strobe signal Internal DS after the external write leveling mode (EWL). The write command start signal WrStart has been advanced by one clock cycle (1.0 tCK) earlier by the number of cycles WICArep provided in the EWL, and a falling edge of the preamble PI of the internal data strobe signal Internal DS occurs one clock cycle after a rising edge of the write command start signal WrStart that corresponds to a cycle (CWL-WICA-0.5). The rising edge of the internal data strobe signal Internal DS that corresponds to the time **0** to start data transmission has not been adjusted. Thus, a time offset of the data strobe signal tDQsoffset is maintained as zero. Because the number of cycles WICArep may be configured in a manner that a total propagation time tFP of the write forward path from the input node of the clock input circuit **502** to the output node of the write delay-locked loop **512** becomes a product of a

clock period tCK and the number of cycles WrLoopN, the time offset of the data strobe signal tDQsoffset can be maintained zero. As described earlier, FIG. **6** illustrated a case when the write preamble is two. The rising edge of the write command start signal WrStart advances a data strobe signal DQS by 0.25 tCK (-0.25 tCK) after applying the WICA value. This timing is sufficient to receive the write command without performing the internal write leveling.

**[0058]** A write delay-locked loop provides WICA information for write level internal cycle alignment between a clock signal and a DQS signal during an external write leveling. A time offset of the data strobe signal tDQsoffset is maintained. Alignment between a clock signal and a DQS signal in a write path may be acceptable without performing the internal write leveling.

**[0059]** FIG. **7** is a schematic diagram of a write path **700**, according to an embodiment of the present disclosure. The write path **700** includes a write forward path including a clock input circuit **702**, a command/address circuit **704** and a write delay-locked loop **712**.

**[0060]** The clock input circuit **702** may provide an internal clock signal ICLK. The clock input circuit **702** may have a propagation delay tD1 from a reception of the input clock signal CK\_t to a transmission of the internal clock signal ICLK. In some embodiments, the clock input circuit **702** may include a clock input buffer without a divider. The clock input buffer may receive an input clock signal CK\_t and its complementary signal CK\_c, and may further provide the input clock signal CK\_t as the internal clock signal ICLK. In some embodiments, the clock input circuit **702** may include a clock input buffer and a divider (not shown). The clock input buffer may receive an input clock signal CK\_t and its complementary signal CK\_c, and may further provide the input clock signal CK\_t. The divider may receive the clock signal CK\_t and may further provide the internal clock signal ICLK that has a half frequency of the input clock signal CK\_t.

**[0061]** In some embodiments, command/address circuit **704** may be the command/address circuit **130** in FIG. **1**. The command/address circuit **704** may include a command decoder **706**, a CWL shifter **710**, a mode register **708** and a selector **722**. In some embodiments, the command decoder **706** may be the command decoder **134** in FIG. **1**. The command decoder **706** may receive the internal clock signal ICLK and command signals from a command/address input circuit, such as the command/address input circuit **131** of FIG. **1**. The command decoder **706** may decode the command signals, and may further provide a write command signal WrCmd in an active state to the CWL shifter **710**, if the command signals are indicative of a write operation. The command decoder **706** may have a propagation delay tD2 between a reception of the internal clocks signal ICLK and a transmission of the write command signal WrCmd based on a decoding process. In some embodiments, a delay (not shown) may be coupled in parallel to the command decoder **706** between the clock input circuit **702** and the CWL shifter **710**. The delay may provide the internal clock signal ICLK with a delay equivalent to the propagation delay tD2 to the write delay-locked loop **712** and the CWL shifter **710** in place of the internal clock signal ICLK.

**[0062]** The CWL shifter **710** may receive the write command signal WrCmd from the command decoder **706**. The CWL shifter **710** may further receive the internal clock signal ICLK. The CWL shifter **710** may further receive a

CAS write latency (CWL), that is a number of clock cycles equivalent to a propagation delay tFP in a write forward path from a reception of clock signals by the clock input circuit 702 to a transmission of a signal provided by the write delay-locked loop 712. In some embodiments, the CWL may be provided by a mode register 708 preprogrammed by an external memory controller (not shown). In some embodiments, a number of bits representing the CWL may be seven.

[0063] The CWL shifter 710 may further receive a number of cycles represented by a WICA value from the write delay-locked loop 712 at write leveling internal cycle alignment (WICA) nodes. The selector 722 may provide the WICA value to the WICA nodes of the CWL shifter. In some embodiments, a number of bits representing the WICA value may be four. The mode register 708 may provide a control signal MR\_INT\_EN. The control signal MR\_INT\_EN instructs the selector 722 to provide either a number of cycles WICAre<sub>p</sub> from the write delay-locked loop 712 during an external write leveling mode or a number of cycles MR\_WICA from the mode register 708 during an internal write leveling mode as the WICA value. In some embodiments, the number of cycles MR\_WICA may be preprogrammed by an external memory controller (not shown) on the mode register 708.

[0064] The CWL shifter 710 may provide a shifted write command signal WrCmd\_Shifted that is the write command signal WrCmd with time adjustment (e.g., shift) based on a product of one cycle tCK and a number of cycles that is a difference of the CWL and the number of cycles WICA. The time adjustment may be performed in a manner that the CWL shifter 710 advances the received write command signal WrCmd by the number of cycles WICA with regards to the CWL to provide the shifted write command signal WrCmd\_Shifted.

[0065] In some embodiments, the write delay-locked loop 712 may include the write delay-locked loop 200. The write delay-locked loop 712 may receive the shifted write command signal WrCmd\_Shifted from the CWL shifter 710. The write delay-locked loop 712 may further receive the internal clock signal ICLK. The write delay-locked loop 712 may provide a delayed write command WrCmd\_Delayed as described referring to FIG. 2 from its output node.

[0066] The write path 700 may also include a DQS delay model 716 coupled to the output node of the write delay-locked loop 712. The DQS delay model 716 has a delay tDdqs equivalent to a propagation delay of a DQS input buffer 714 on a DQS path. The DQS delay model 716 may receive the delayed write command WrCmd\_Delayed and provide a write command start signal WrStart that is delayed by the tDdqs from the delayed write command WrCmd\_Delayed. The write path 700 may further include a write path output latch 718. The DQS input buffer 714 may receive a data strobe signal DQS<sub>t</sub> and its complementary signal DQS<sub>c</sub>, and provide an internal DQS signal IDQS.

[0067] The write path output latch 718 may receive the write command start signal WrStart and the internal DQS signal at a data input node and a clock input node, respectively. The write path output latch 718 may provide an internal write leveling data signal IWLdata to a data queue output node DQout responsive to the write command start signal WrStart and the internal DQS signal IDQS.

[0068] The DQS path also includes a logic circuit 720 that may receive the internal DQS signal IDQS and the internal write leveling data signal IWLdata. In some embodiments,

the logic circuit 720 may be a logic AND gate. The logic circuit 720 may provide an internal data strobe signal Internal DS that is a combined signal of the internal DQS signal IDQS and the internal write leveling data signal IWLdata.

[0069] The number of cycles WICAre<sub>p</sub> may be configured in a manner that a total propagation time tFP of the write forward path from the input node of the clock input circuit 702 to the output node of the write delay-locked loop 712 becomes a product of a clock period tCK and the number of cycles WrLoopN that is described referring to FIG. 2. In some embodiments, the write delay-locked loop 712 may receive a current write leveling mode. The write delay-locked loop 712 may provide the number of cycles WICAre<sub>p</sub> by adjusting the number of cycles WrLoopN when a current write leveling mode is an external write leveling mode (EWL).

[0070] FIG. 8 is a timing diagram 800 of signals during external and internal write levelings, according to the embodiment of the present disclosure. A panel 802 represents a timing relationship between the write command start signal WrStart and an external data strobe signal xDS that is similar to the internal data strobe signal Internal DS when the current write leveling mode is an external write leveling mode (EWL). The write delay-locked loop 712 may provide the number of cycles WICAre<sub>p</sub> that is the number of cycles WrLoopN responsive to the current write leveling mode being the external write leveling mode (EWL). A rising edge of the clock signal CK<sub>t</sub> representing a cycle CWL may be synchronized with a rising edge of the external data strobe signal xDS that indicates a time 0 to start data transmission. When the total propagation time tFP with the write delay-locked loop 712 is a duration of two clock periods 2 tCK, a rising edge of the write command start signal WrStart may be synchronized with a falling edge of a preamble at time PI that is half a period before the time 0 that may be delayed from a falling edge of the clock signal CK<sub>t</sub> at a cycle (CWL-WICA -0.5), when the selector 722 provides the number of cycles WICAre<sub>p</sub> from the write delay-locked loop 712 to the CWL shifter 710 as a WICA value.

[0071] A panel 804 represents a timing relationship between the write command start signal WrStart and the internal data strobe signal Internal DS when the current write leveling mode enters an internal write leveling mode (IWL). The selector 722 provides a number of cycles MR\_WICA as a WICA value to the CWL shifter 710. For example, in FIG. 8, when the write preamble is two, the selector 722 may provide the number of cycles MR\_WICA (e.g., three) from the mode register 708. The time tWL\_ADJ\_START represents an offset that a memory controller applies to timings of the data strobe signals DQS<sub>t</sub> and DQS<sub>c</sub> while switching from the EWL mode to the IWL mode. In the example of the panel 804, the time tWL\_ADJ\_START is 0.75 times of the clock period (0.75 tCK). Thus, the number of cycles MR\_WICA is approximated as {2+round up (0.75-0.5)}=3. Thus, WICA value=3 is provided to the CWL shifter 710.

[0072] A panel 806 represents a timing relationship between the write command start signal WrStart and the internal data strobe signal Internal DS while conducting a data strobe fine adjustment in the internal write leveling mode (IWL). The internal data strobe signal Internal DS has been advanced by 0.75 tCK and a falling edge of the preamble PI is synchronized with the rising edge of the write



command start signal WrStart that corresponds to a cycle (CWL-WICA-1). The data strobe fine adjustment value DS fine adjust is computed as  $(-WICA+A)$  where A is computed as  $\{tFP+t(WL\_ADJ\_START-0.5)\}$ . Thus, the data strobe fine adjustment value DS fine adjust is computed as  $(-3+2+0.75-0.5)tCK=-0.75tCK$ .

**[0073]** A panel 808 represents a timing relationship between the write command start signal WrStart and the internal data strobe signal Internal DS after the internal write leveling mode (IWL). WICA training starts with an offset that is set to "0". By the time the internal write leveling ends at the time  $tWL\_ADJ\_END$ , that is  $1.25tCK$ , the rising edge of the internal data strobe signal Internal DS that corresponds to the time 0 to start data transmission is  $0.25tCK$  earlier than the initial time 0 in the panel 802. Thus, a time offset of the data strobe signal  $tDQSO\text{ffset}$  is controlled to  $-0.25tCK$ .

**[0074]** As described earlier, FIG. 8 illustrated a case when the write preamble is two and the time  $tWL\_ADJ\_START$  is  $0.75tCK$ . When the write preamble is two and the time  $tWL\_ADJ\_START$  is  $-0.75tCK$ , the time offset of the data strobe signal  $tDQSO\text{ffset}$  is controlled to  $-0.25tCK$ . When the write preamble is three and the time  $tWL\_ADJ\_START$  is  $-1.25tCK$ , the time offset of the data strobe signal  $tDQSO\text{ffset}$  is controlled to  $0.25tCK$ . When the write preamble is four and the time  $tWL\_ADJ\_START$  is  $-2.25tCK$ , the time offset of the data strobe signal  $tDQSO\text{ffset}$  is controlled to  $0.25tCK$ .

**[0075]** Because the number of cycles  $WICArep$  may be configured in a manner that a total propagation time  $tFP$  of the write forward path from the input node of the clock input circuit 702 to the output node of the write delay-locked loop 712 becomes a product of a clock period  $tCK$  and the number of cycles  $WrLoopN$ , regardless of the write preamble and the time  $tWL\_ADJ\_START$ , the time offset of the data strobe signal  $tDQSO\text{ffset}$  can be controlled between  $-0.25tCK$  and  $0.25tCK$ .

**[0076]** A write delay-locked loop provides WICA information for write level internal cycle alignment between a clock signal and a DQS signal during an external write leveling and a mode register provide WICA information programmed by a memory controller during an internal write leveling. A time offset of the data strobe signal  $tDQSO\text{ffset}$  is controlled within a desirable range, thus alignment between a clock signal and a DQS signal in a write path may be improved.

**[0077]** Various embodiments of apparatus and methods for write level internal alignment between a clock signal and a DQS signal in a write forward path have been described. A write forward path includes a CWL shifter and a write delay-locked loop coupled to the CWL shifter. In some embodiments, the write delay-locked loop provides WICA information while providing a write start signal with a delay controlled based on a phase difference between the clock signal and a feedback signal from a replica circuit. In some embodiments, the write delay-locked loop provides different WICA values between an external write leveling and an internal write leveling. In some embodiments, the write delay-locked loop provides a WICA value in an external write leveling and the write forward path does not perform an internal write leveling. In some embodiments, the write delay-locked loop provides a WICA value in an external write leveling and a mode register provides a WICA value programmed by a memory controller in an internal write

leveling. By actively controlling a delay in the write forward path by the write delay-locked loop in a manner that a total propagation time  $tFP$  of a write forward path from an input node of the clock input circuit to an output node of the write delay-locked loop becomes an integral multiple of a clock period, a time offset of the data strobe signal  $tDQSO\text{ffset}$  is controlled within a desirable range, thus alignment between a clock signal and a DQS signal in a write path may be improved.

**[0078]** Although various embodiments have been disclosed, it will be understood by those skilled in the art that the disclosure extends beyond the specifically disclosed embodiments to other alternative embodiments and/or uses of the embodiments and obvious modifications and equivalents thereof. In addition, other modifications which are within the scope of the disclosure will be readily apparent to those of skill in the art based on this disclosure. It is also contemplated that various combination or sub-combination of the specific features and aspects of the embodiments may be made and still fall within the scope of the disclosure. It should be understood that various features and aspects of the disclosed embodiments can be combined with or substituted for one another in order to form varying modes of the disclosed embodiments. Thus, it is intended that the scope of at least some of the present disclosure should not be limited by the particular disclosed embodiments described above.

What is claimed is:

1. An apparatus comprising:

a write forward path comprising:

- a clock input circuit configured to receive an external clock signal and further configured to provide an internal clock signal;
- a command/address circuit configured to receive the internal clock signal and command signals and further configured to provide a write command signal with time adjustment; and

a write delay-locked loop comprising:

- a delay line configured to receive the internal clock signal and further configured to provide a delayed internal clock signal;
- a delay model having a model propagation delay equivalent to a sum of a first propagation delay in the clock input circuit and a second propagation delay in the command/address circuit, the delay model configured to receive the delayed internal clock signal and further configured to provide a feedback signal; and

- a measurement initialization circuit configured to receive the internal clock signal at a start node and the feedback signal at a stop node, and further configured to provide a WICA value that indicates a number of cycles equivalent to a propagation time from an input node of the clock input circuit to an output node of the write delay-locked loop,

wherein the write delay-locked loop is configured to provide the WICA value to the command/address circuit to set the propagation time.

2. The apparatus of claim 1, wherein the propagation time is set to be an integral multiple of a period of the external clock signal.

3. The apparatus of claim 1, wherein the command/address circuit comprises a write latency shifter configured to receive the write command signal, a latency value and the WICA value and further configured to adjust timing of the

write command signal responsive to the latency value and the WICA value, and further configured to provide the write command signal with time adjustment.

4. The apparatus of claim 3, wherein the write delay-locked loop further comprises a second delay line configured to receive the write command signal with time adjustment and provide a delayed write command signal having a third propagation delay.

5. The apparatus of claim 4, wherein the write forward path further comprises a second delay model coupled to the write delay-locked loop and configured to receive the delayed write command and provide a write command start signal that is delayed by a fourth propagation delay.

6. The apparatus of claim 4, wherein the write delay-locked loop further comprises a phase detector configured to receive the internal clock signal and the feedback signal, configured to detect a phase shift between the feedback signal and the internal clock signal, and further configured to provide a delay control signal to the first and second delay lines to reduce the phase shift.

7. The apparatus of claim 1, wherein the WICA value is a first WICA value, wherein the write delay-locked loop further comprises a mode selector configured to receive a current write leveling mode, configured to provide the first WICA value if the current write leveling mode is an external write leveling mode.

8. The apparatus of claim 7, wherein the mode selector is further configured to provide a second WICA value if the current write leveling mode is an internal write leveling mode.

9. The apparatus of claim 8, wherein the second WICA value during the internal write leveling mode is based on the first WICA value and a round up of an offset to a timing of a data strobe signal while switching from the external write leveling mode to the internal write leveling mode.

10. The apparatus of claim 1, wherein the measurement initialization circuit is further configured to provide the WICA value when the write delay-locked loop is reset.

11. An apparatus comprising:

a clock input circuit configured to receive an external clock signal and further configured to provide an internal clock signal;

a command/address circuit configured to receive the internal clock signal and command signals and further configured to provide a write command signal with time adjustment; and

a write delay-locked loop comprising:

a delay line configured to receive the internal clock signal and further configured to provide a delayed internal clock signal;

a second delay line configured to receive the write command signal with time adjustment and provide a delayed write command signal;

a delay model having a model propagation delay equivalent to a sum of a first propagation delay in the clock input circuit and a second propagation delay in the command/address circuit, the delay model configured to receive the delayed internal clock signal and further configured to provide a feedback signal; and

a phase detector configured to receive the internal clock signal and the feedback signal, configured to detect a phase shift between the feedback signal and the internal clock signal, and further configured to provide

a delay control signal to the first and second delay lines to reduce the phase shift.

12. The apparatus of claim 11, further comprising: a measurement initialization circuit configured to receive the internal clock signal at a start node and the feedback signal at a stop node, and further configured to provide a WICA value that indicates a number of cycles equivalent to a propagation time from an input node of the clock input circuit to an output node of the write delay-locked loop.

13. The apparatus of claim 12, further comprising a mode selector configured to adjust the number of cycles based on a current write leveling mode.

14. The apparatus of claim 13, wherein the current write leveling mode is either an external write leveling mode or an internal write leveling mode.

15. The apparatus of claim 11, wherein the write delay-locked loop is configured to provide the WICA value to the command/address circuit to set the propagation time.

16. The apparatus of claim 11, wherein the measurement initialization circuit is further configured to provide the WICA value when the write delay-locked loop is reset.

17. An apparatus comprising:

a clock input circuit configured to receive an external clock signal and further configured to provide an internal clock signal, the clock input circuit having a first propagation delay;

a command/address circuit configured to receive the internal clock signal and command signals and further configured to decode the command signals to provide a write command signal with time adjustment, the command decoder having a second propagation delay; and

a write delay-locked loop comprising:

a delay line configured to receive the internal clock signal and further configured to provide a delayed internal clock signal;

a delay model having a model propagation delay equivalent to a sum of the first propagation delay and the second propagation delay, the delay model configured to receive the delayed internal clock signal and further configured to provide a feedback signal indicative of the sum of the first propagation delay and the second propagation delay;

a phase detector configured to receive the internal clock signal and the feedback signal and detect a phase shift between the feedback signal and the internal clock signal; and

a measurement initialization circuit configured to receive the internal clock signal at a start node and the feedback signal at a stop node.

18. The apparatus of claim 17, wherein the measurement initialization circuit is further configured to provide a WICA value that indicates a number of cycles equivalent to a propagation time from an input node of the clock input circuit to an output node of the write delay-locked loop.

19. The apparatus of claim 18, wherein the write delay-locked loop is configured to provide the WICA value to the command/address circuit to set the propagation time.

20. The apparatus of claim 17, wherein the write delay-locked loop further comprises: a second delay line configured to receive the write command signal with time adjustment and provide a delayed write command signal, and

wherein the phase detector is further configured to provide a delay control signal to the first and second delay lines to reduce the phase shift.

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