



US 20250267877A1

(19) **United States**  
(12) **Patent Application Publication** (10) **Pub. No.: US 2025/0267877 A1**  
Lin et al. (43) **Pub. Date: Aug. 21, 2025**

(54) **SEMICONDUCTOR DEVICE AND METHOD FOR FORMING THE SAME**

**Publication Classification**

(71) Applicant: **Taiwan Semiconductor Manufacturing Co., Ltd.**, Hsinchu (TW)  
(72) Inventors: **Shy-Jay Lin**, Jhudong Township (TW); **Chien-Min Lee**, Hsinchu (TW); **Hiroki Noguchi**, Hsinchu (TW); **MingYuan Song**, Hsinchu (TW); **Yen-Lin Huang**, Hsinchu (TW); **William Joseph Gallagher**, Hsinchu (TW)

(51) **Int. Cl.**  
*H10B 61/00* (2023.01)  
*H01L 21/768* (2006.01)  
*H01L 23/528* (2006.01)  
*H10D 84/01* (2025.01)  
*H10D 84/03* (2025.01)  
(52) **U.S. Cl.**  
CPC ..... *H10B 61/22* (2023.02); *H01L 21/76898* (2013.01); *H01L 23/528* (2013.01); *H10D 84/0149* (2025.01); *H10D 84/038* (2025.01)

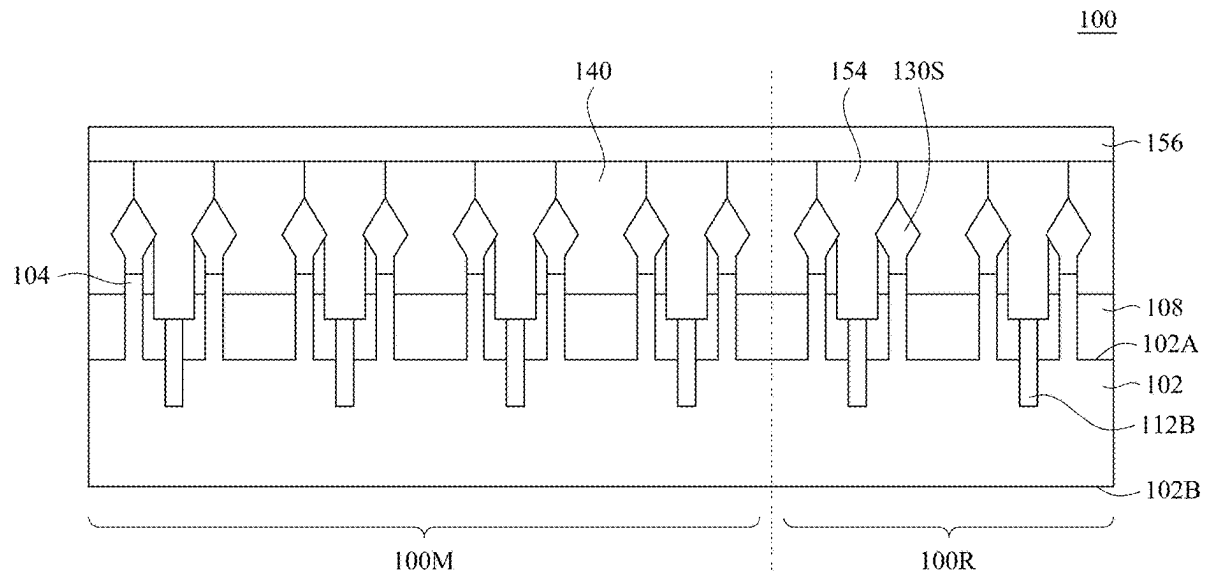
(21) Appl. No.: **19/197,289**  
(22) Filed: **May 2, 2025**

**Related U.S. Application Data**

(60) Continuation of application No. 18/679,002, filed on May 30, 2024, now Pat. No. 12,317,513, which is a division of application No. 18/335,816, filed on Jun. 15, 2023, now Pat. No. 12,022,665, which is a division of application No. 17/216,162, filed on Mar. 29, 2021, now Pat. No. 11,723,218.  
(60) Provisional application No. 63/045,285, filed on Jun. 29, 2020.

**ABSTRACT**

A device includes a substrate having a first side and a second side, a first transistor that includes a first gate over a first protrusion and a first source region and a first drain region interposing the first protrusion, a first buried contact disposed adjacent to the first protrusion and having at least a portion extending into the substrate, a first contact plug disposed over the first drain region, first conductive lines disposed over the first contact plug and electrically connecting to the first drain region by the first contact plug, first via penetrating through the substrate and connecting the first buried contact; and second conductive lines disposed over the second side of the substrate and electrically connecting to the first via. The first buried contact is electrically connecting to the first source region or the first gate.



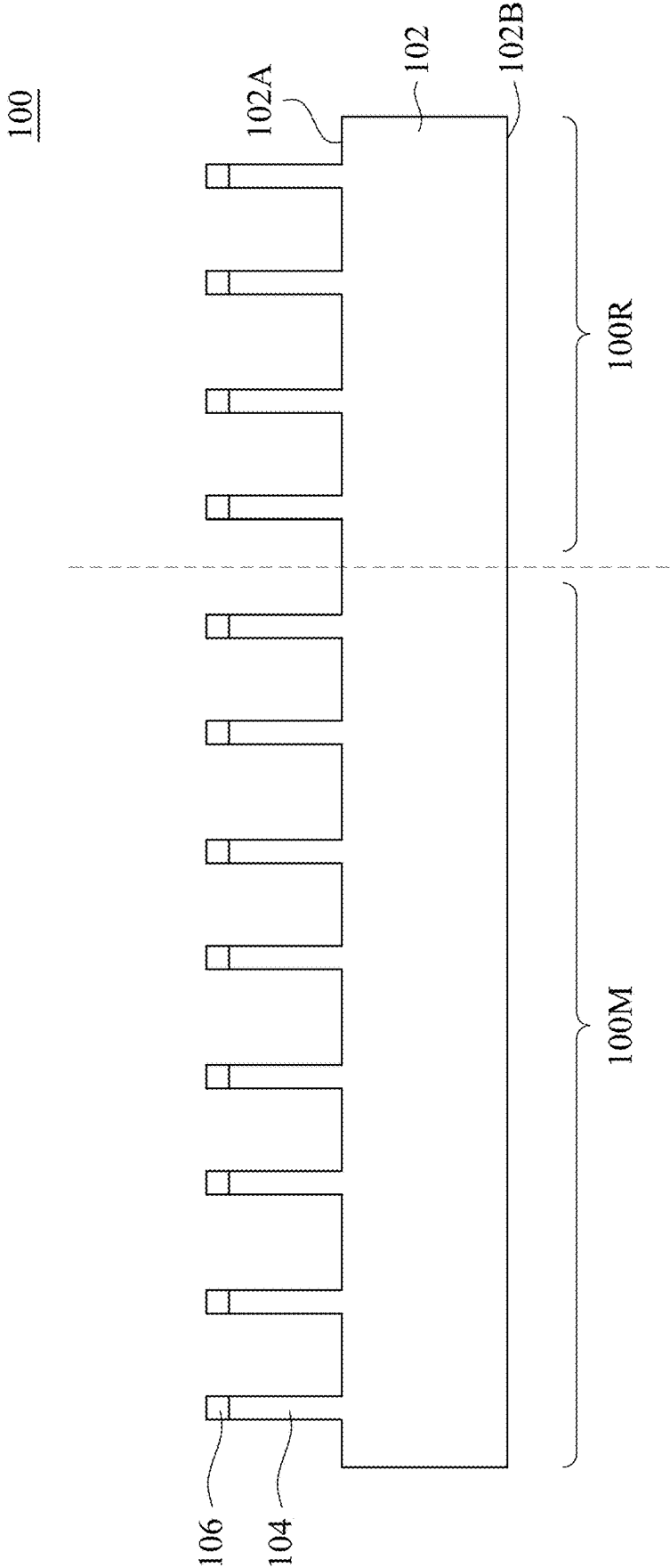


FIG. 1A

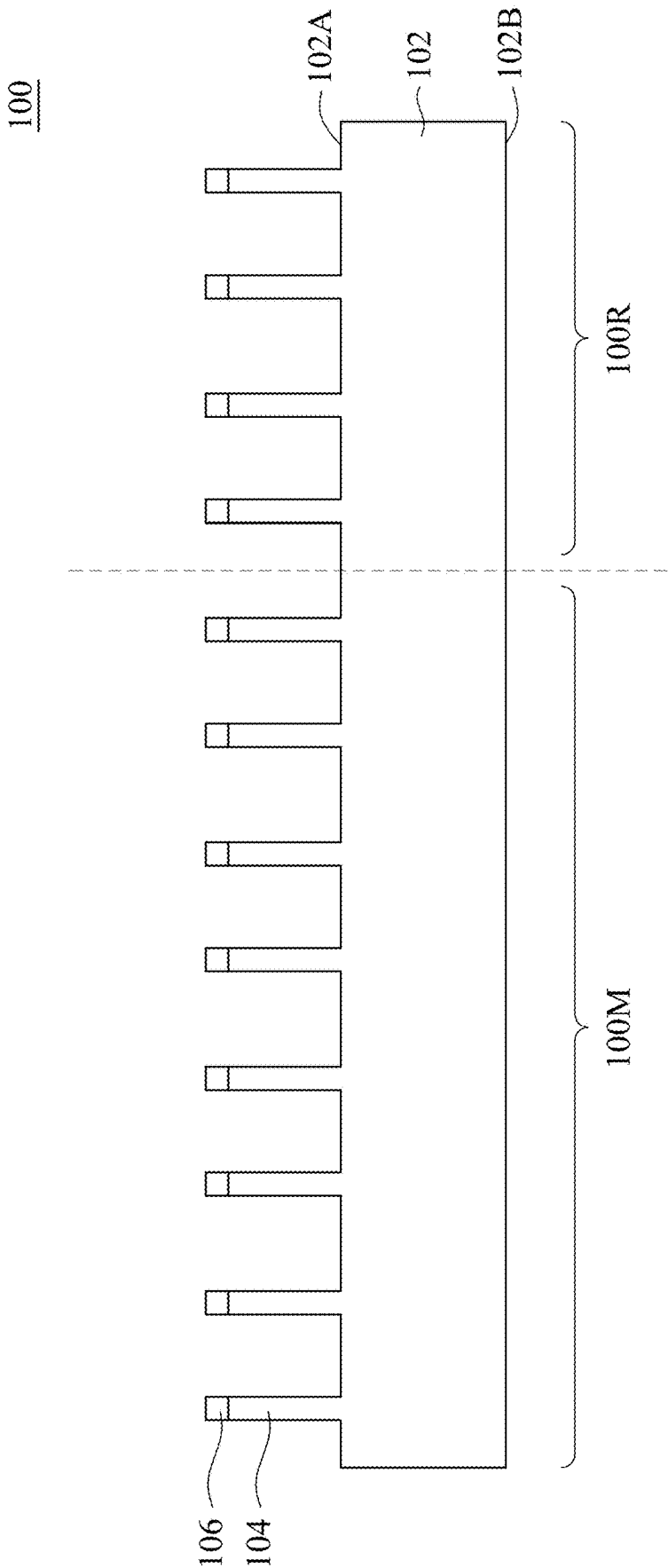


FIG. 1B

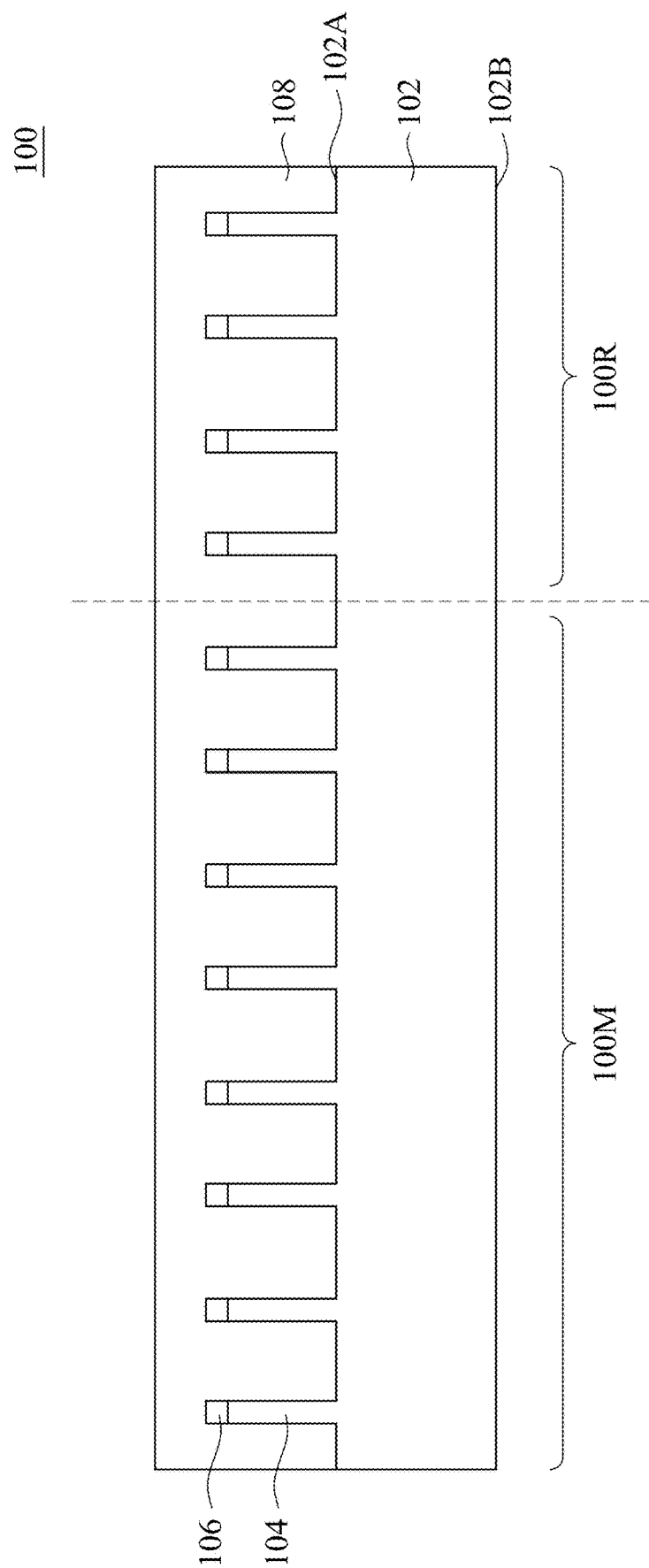


FIG. 2A

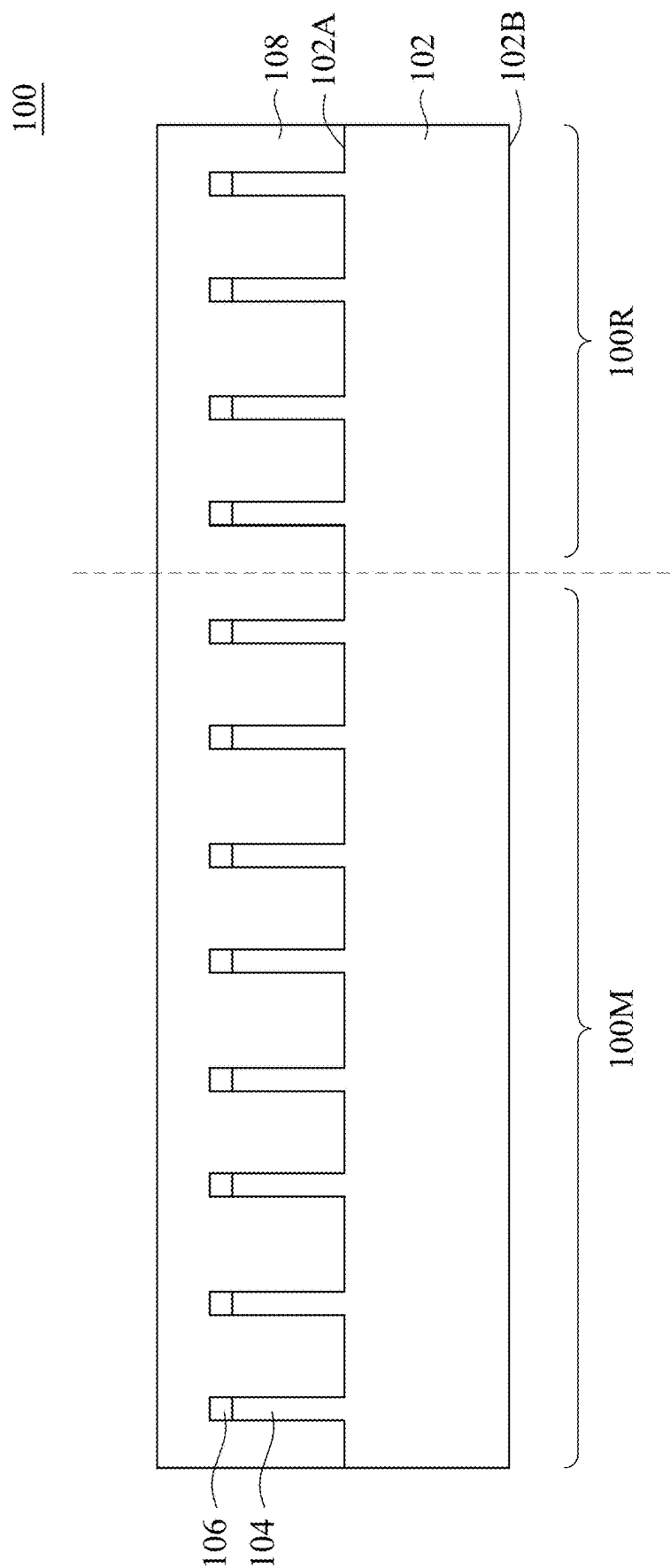


FIG. 2B

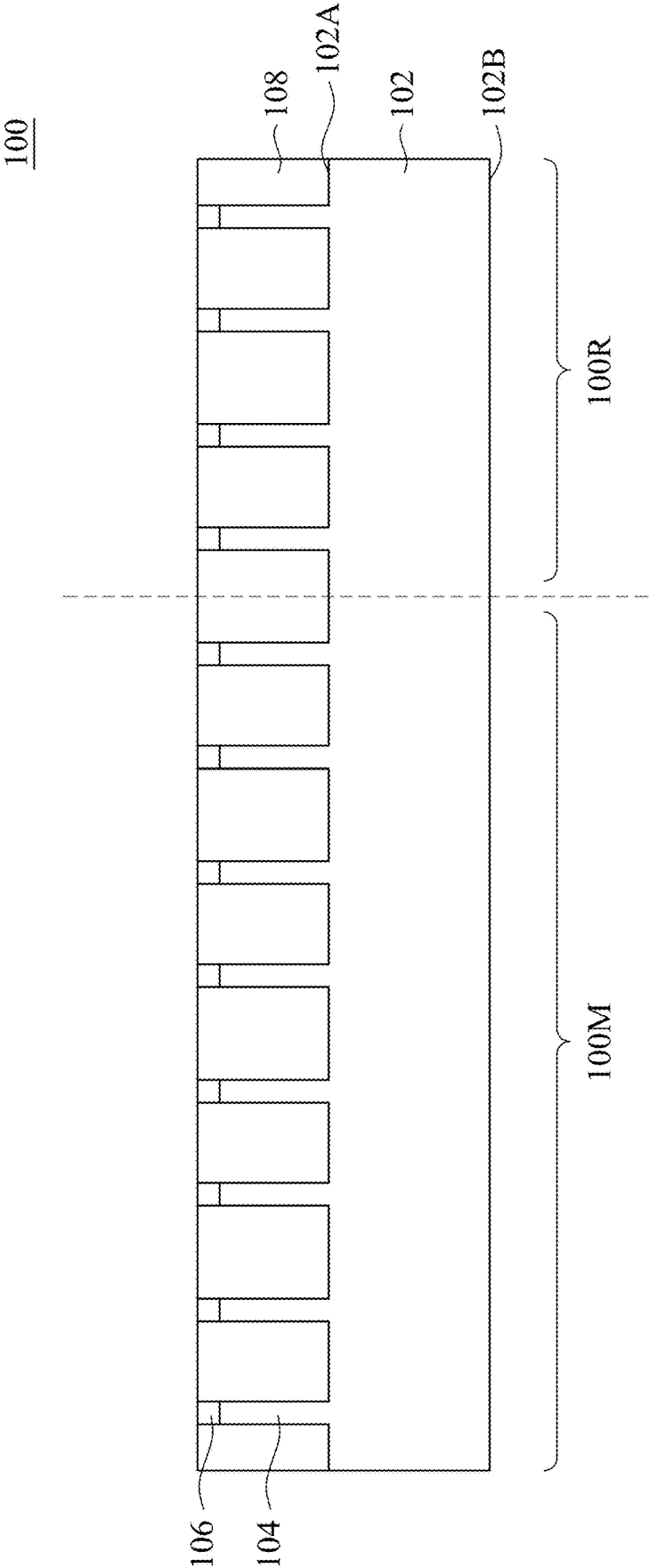


FIG. 3A

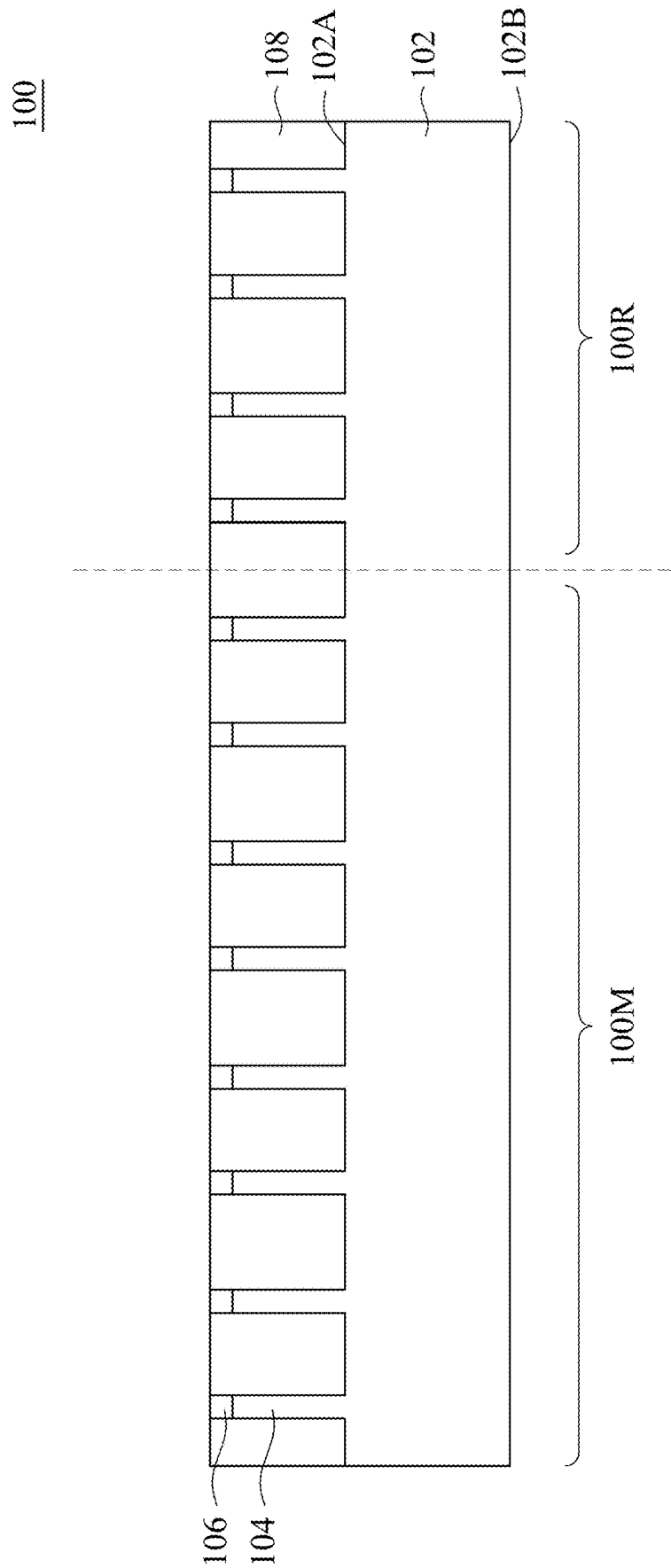


FIG. 3B

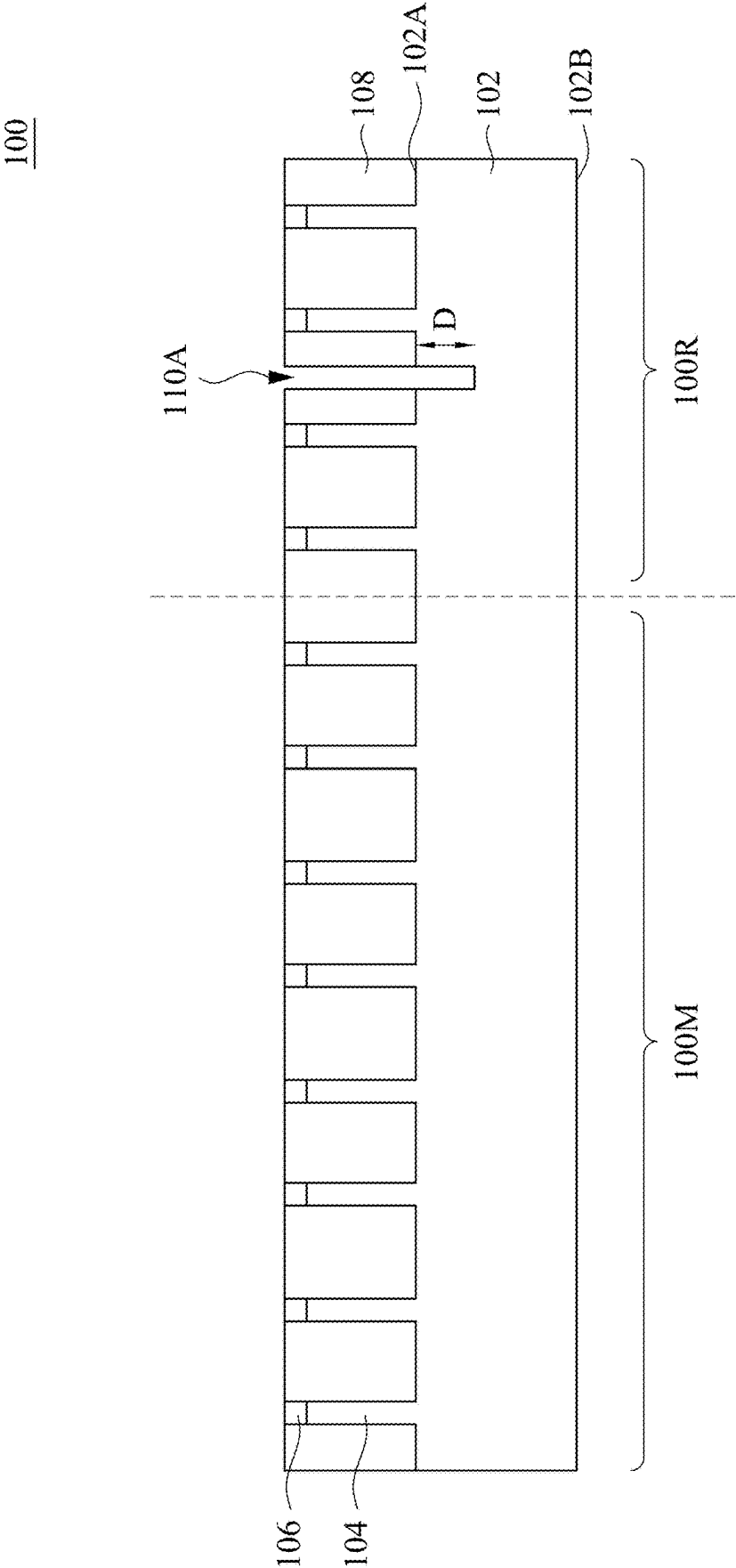


FIG. 4A



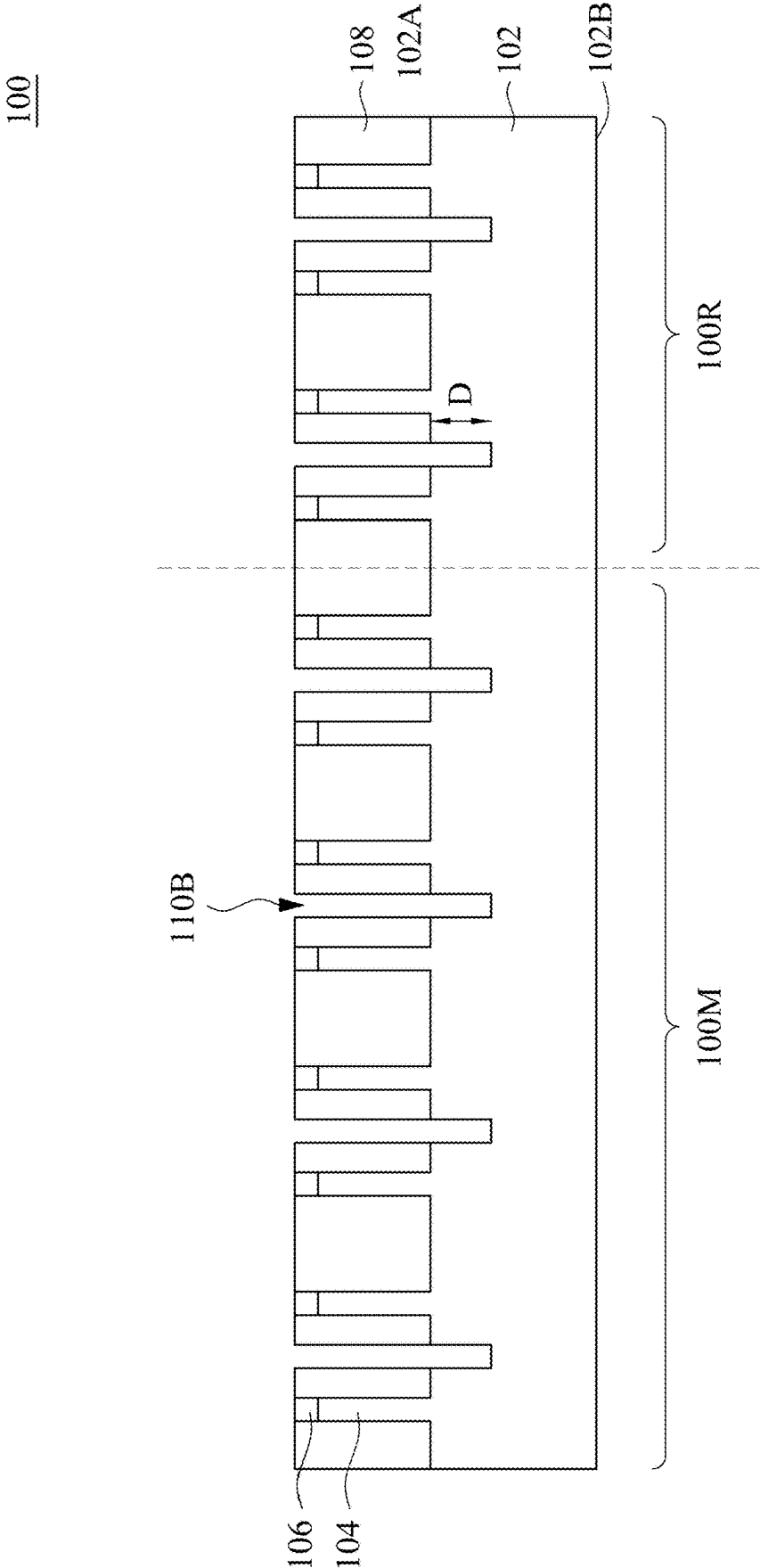


FIG. 4B

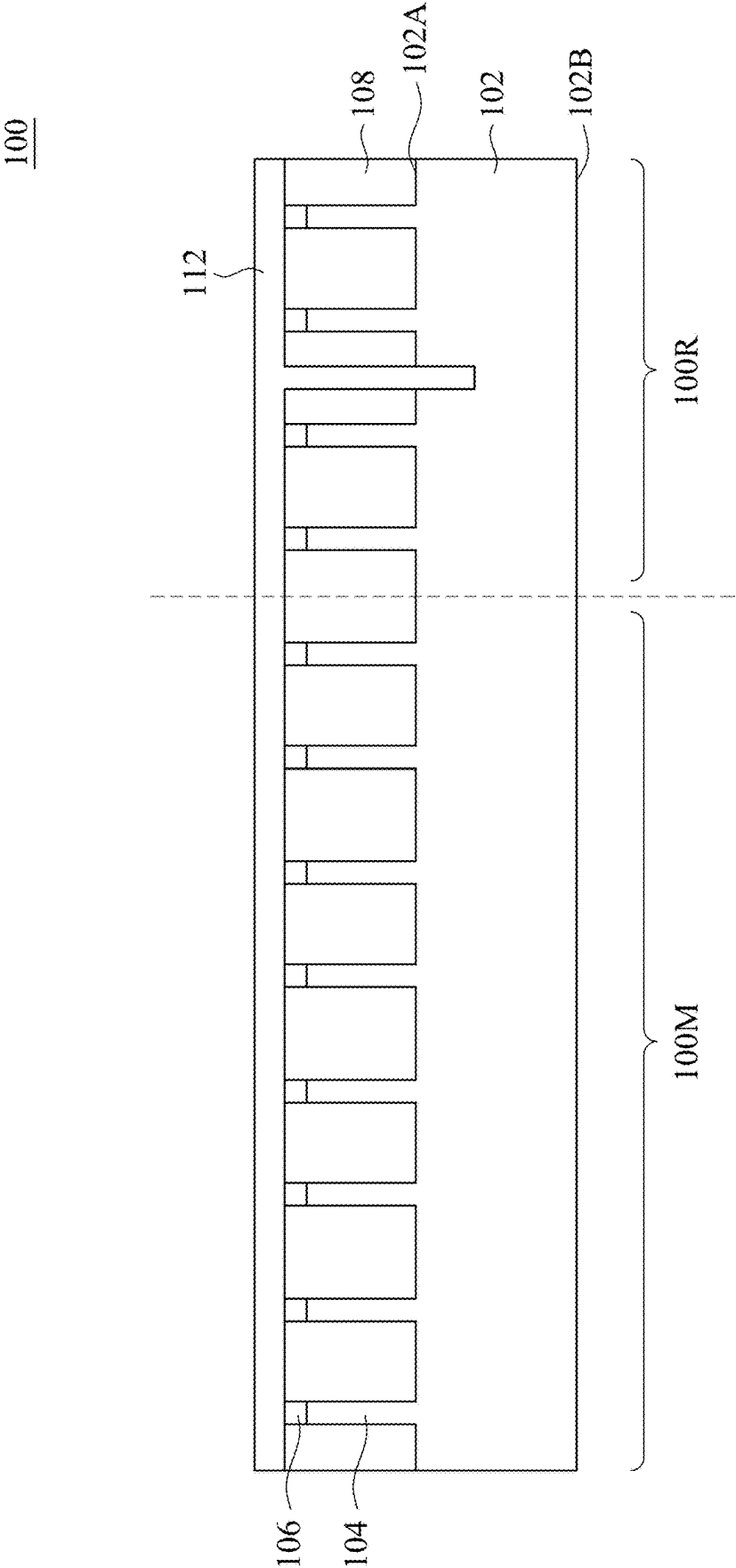


FIG. 5A

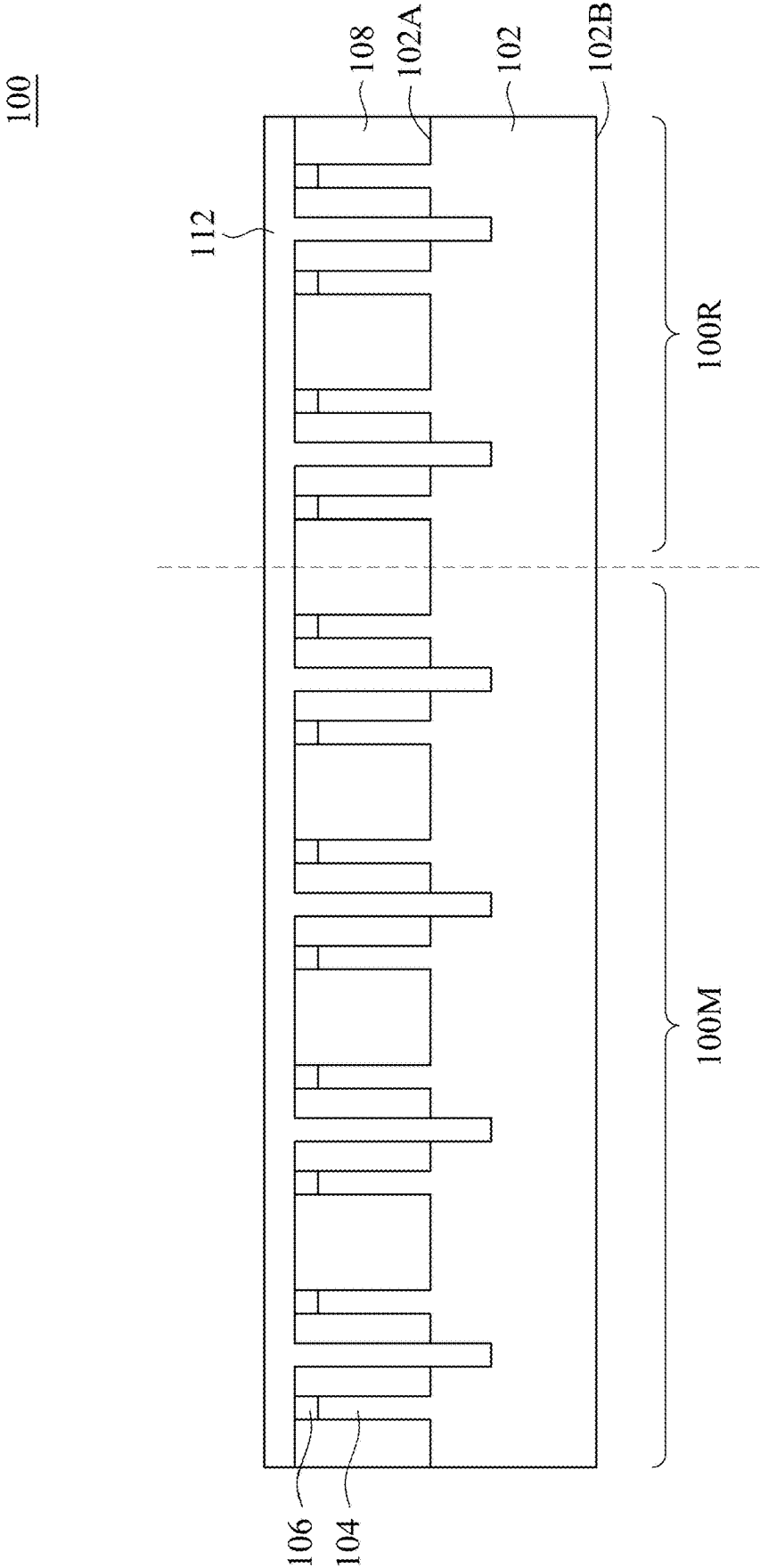


FIG. 5B

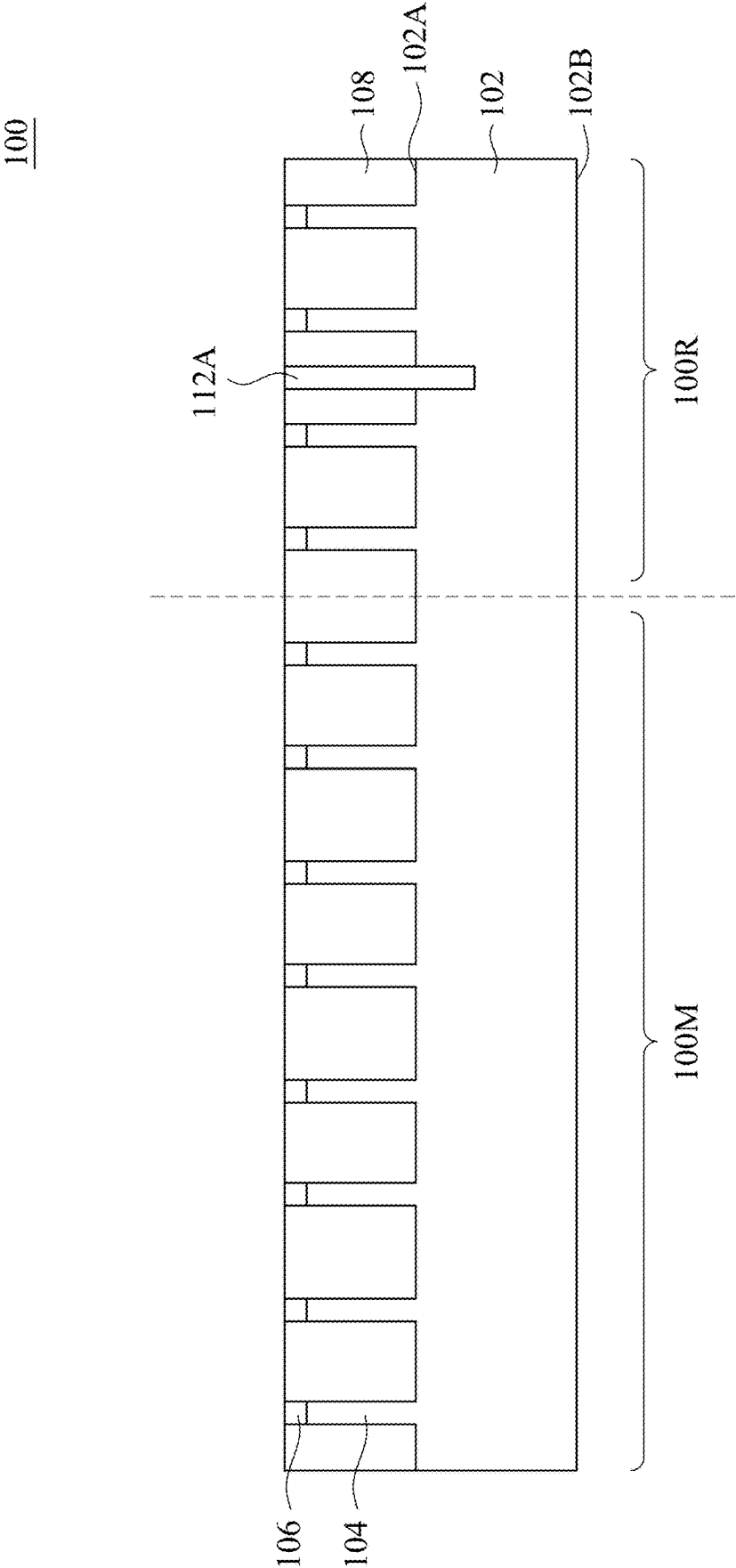


FIG. 6A

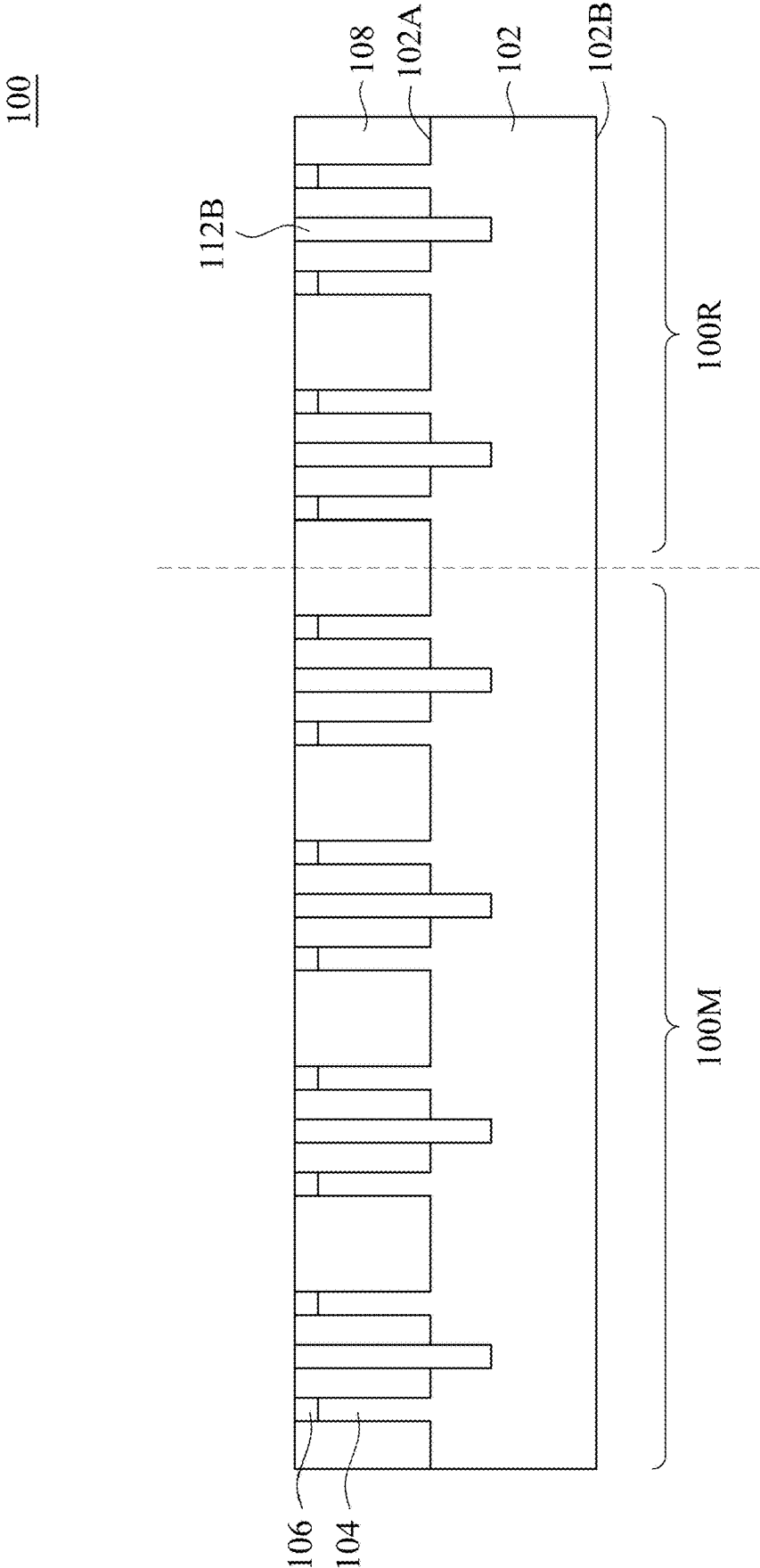


FIG. 6B

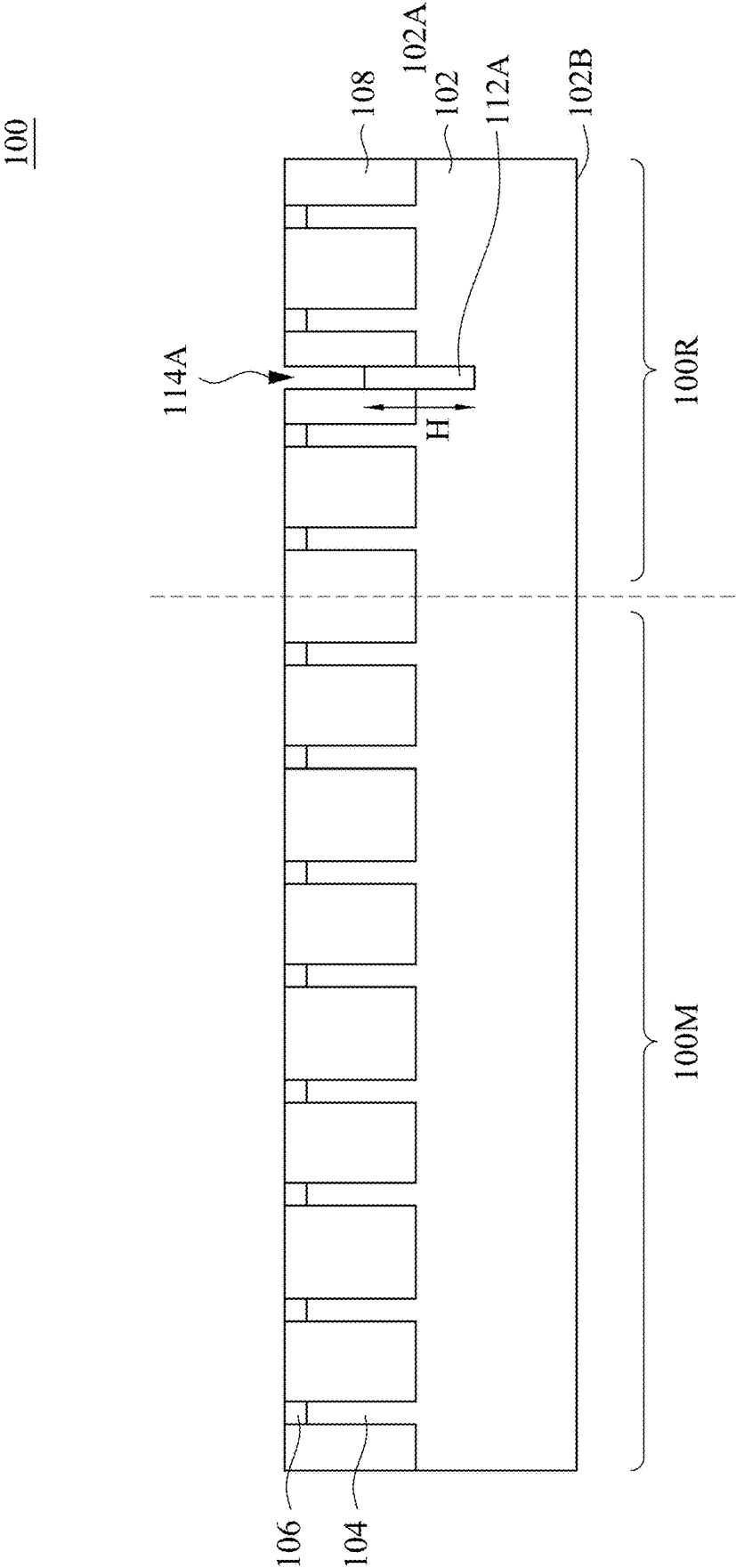


FIG. 7A

100

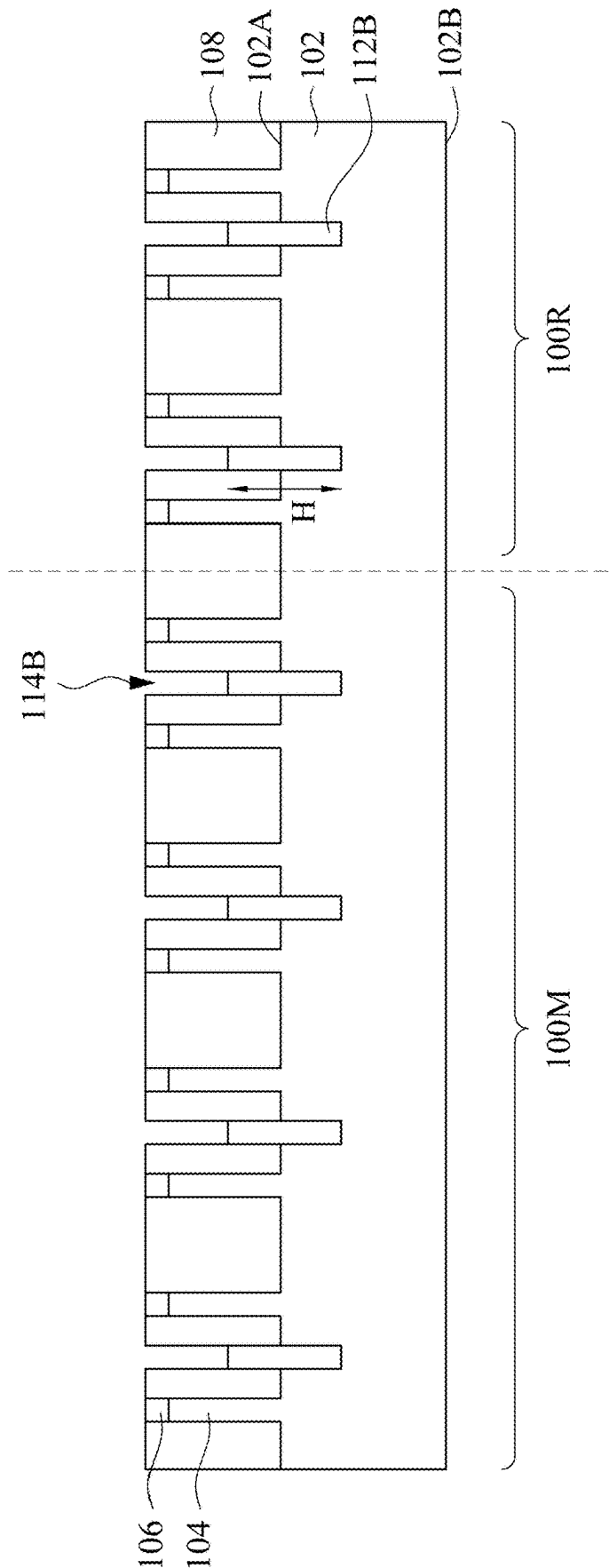


FIG. 7B

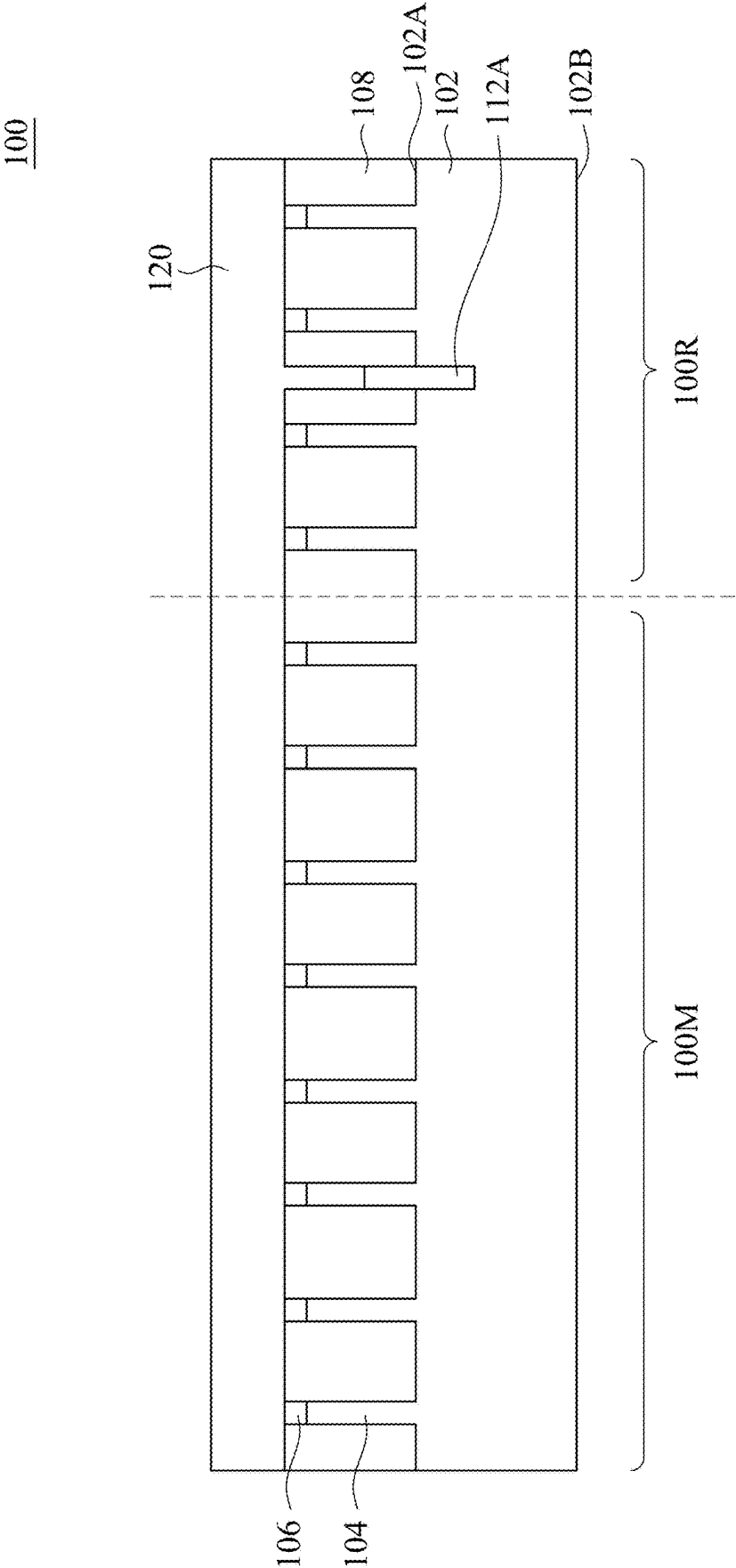
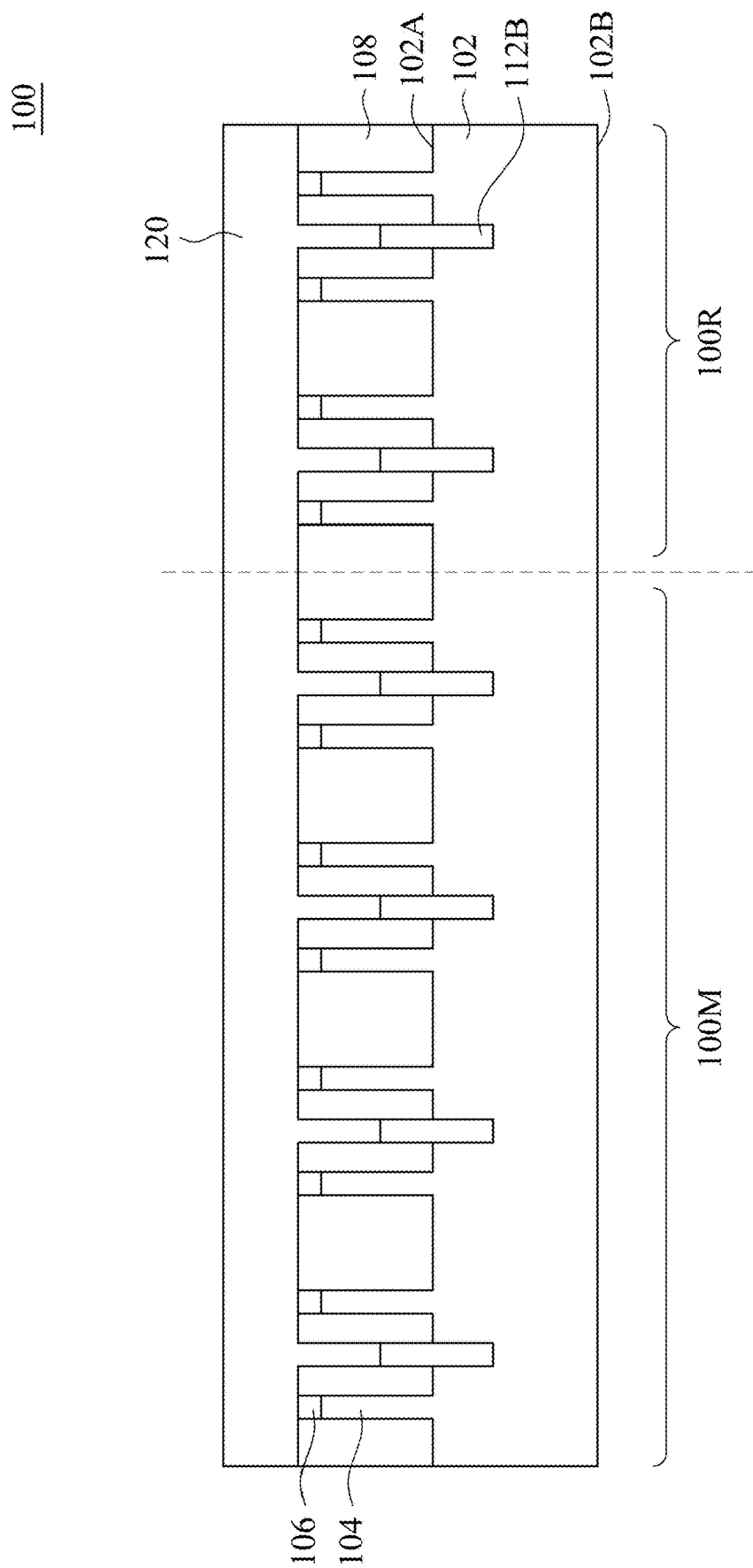


FIG. 8A





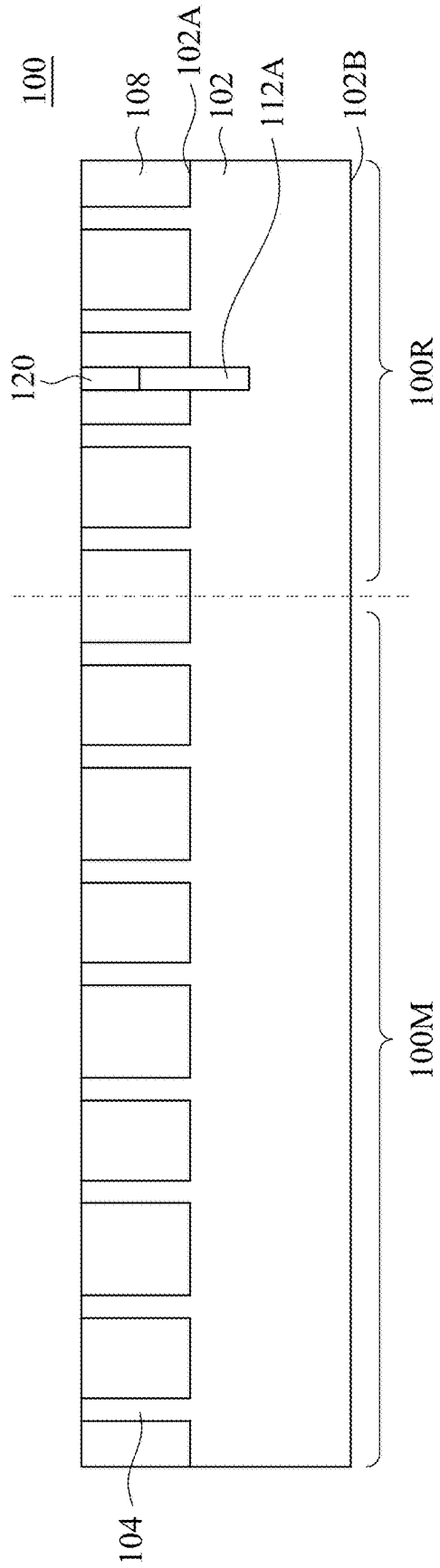


FIG. 9A

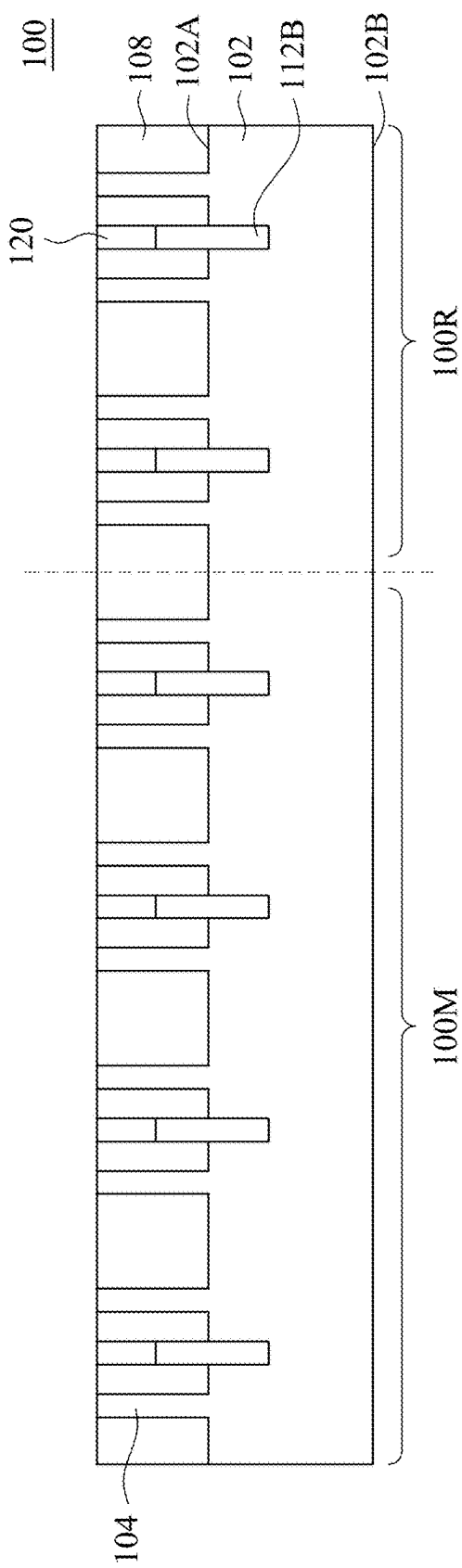


FIG. 9B

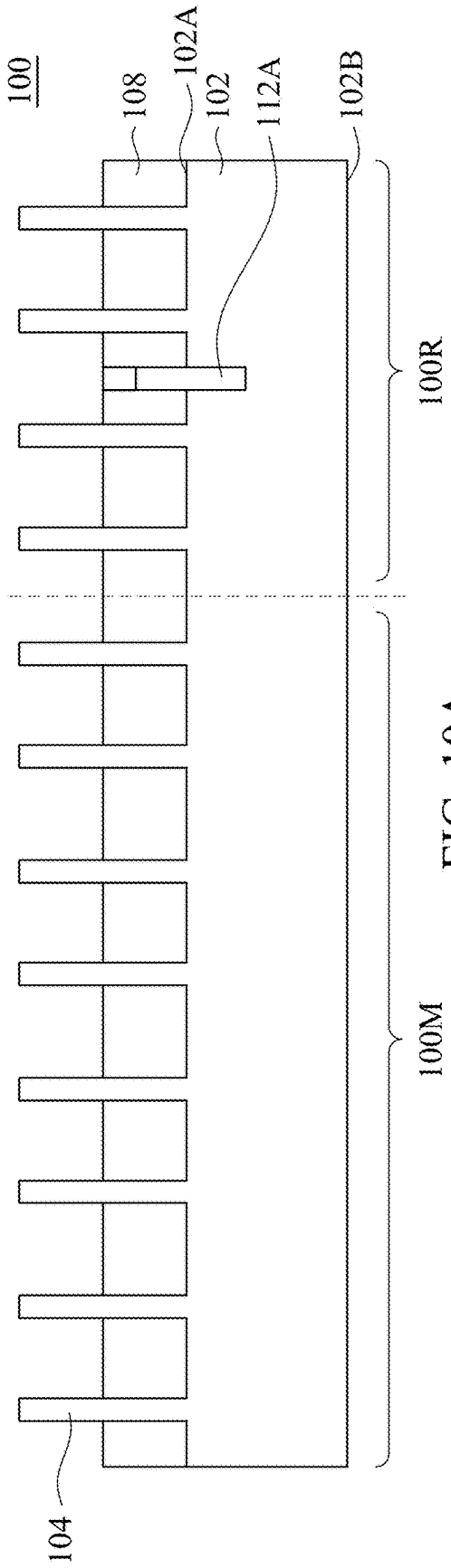


FIG. 10A

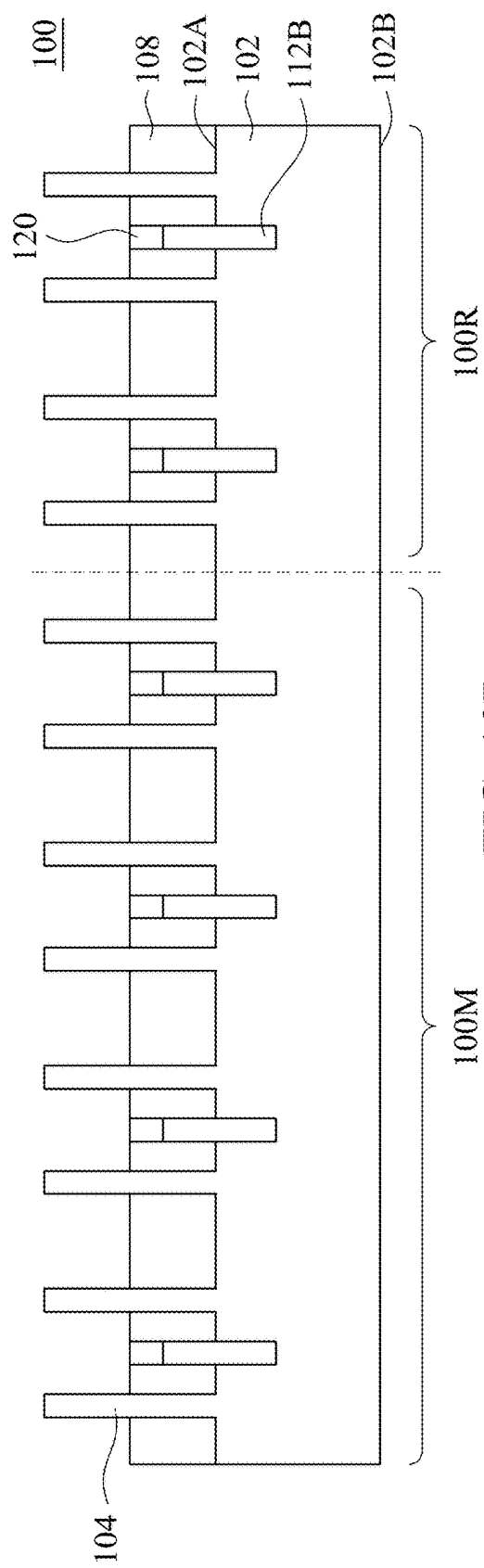
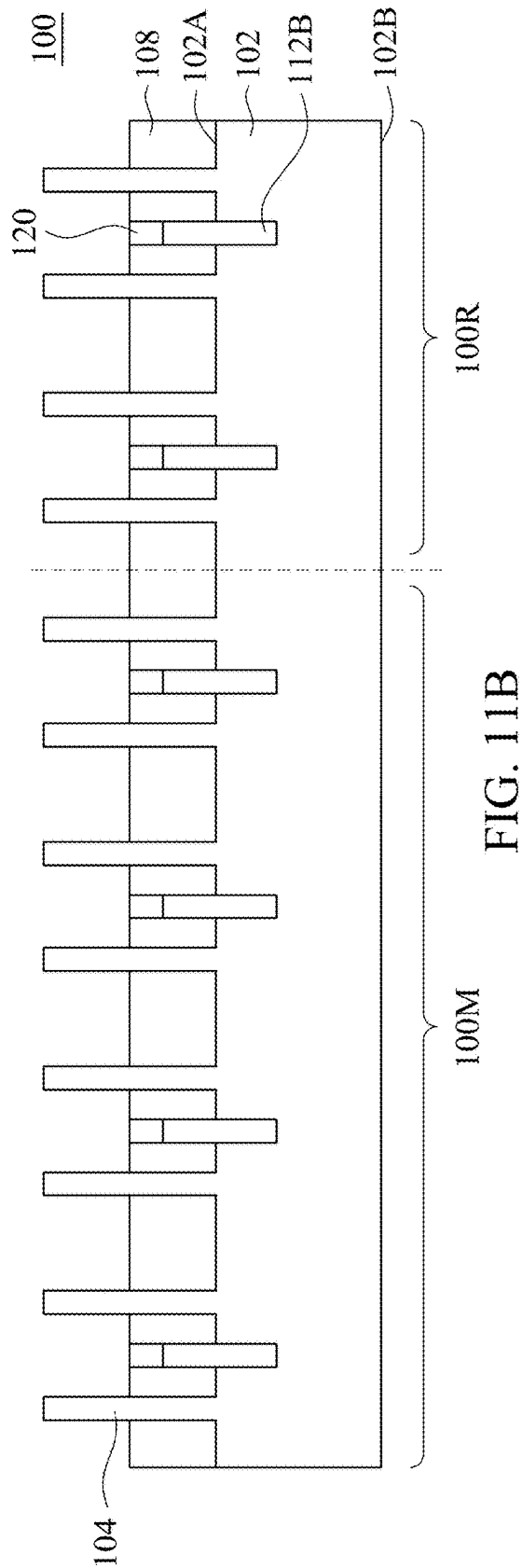
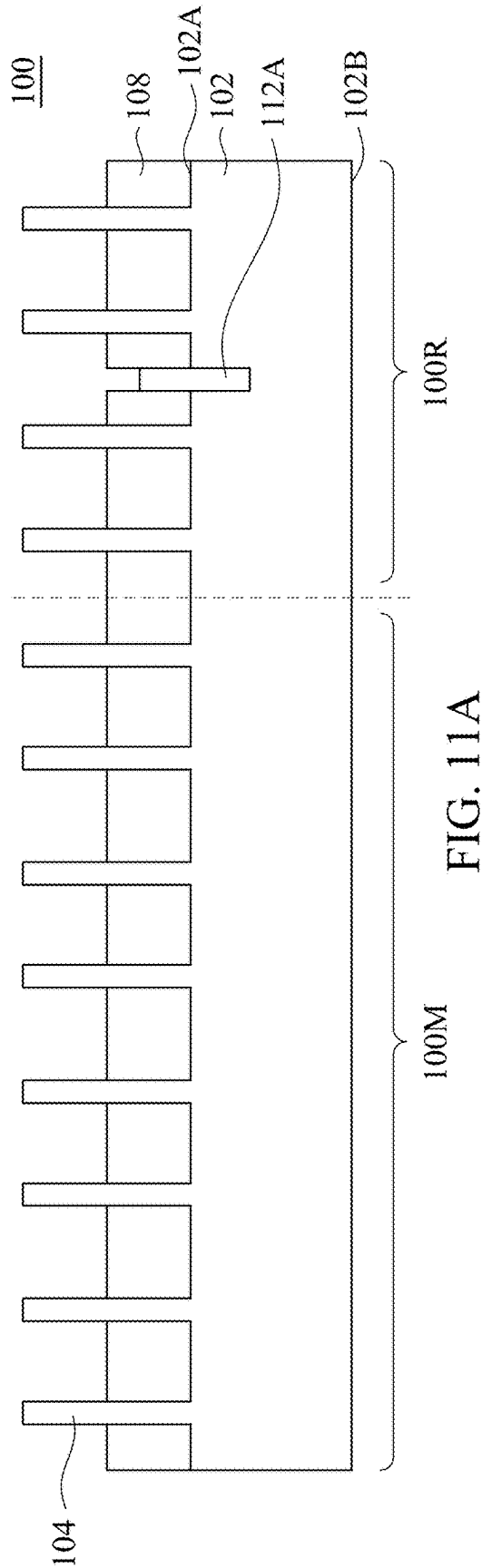


FIG. 10B



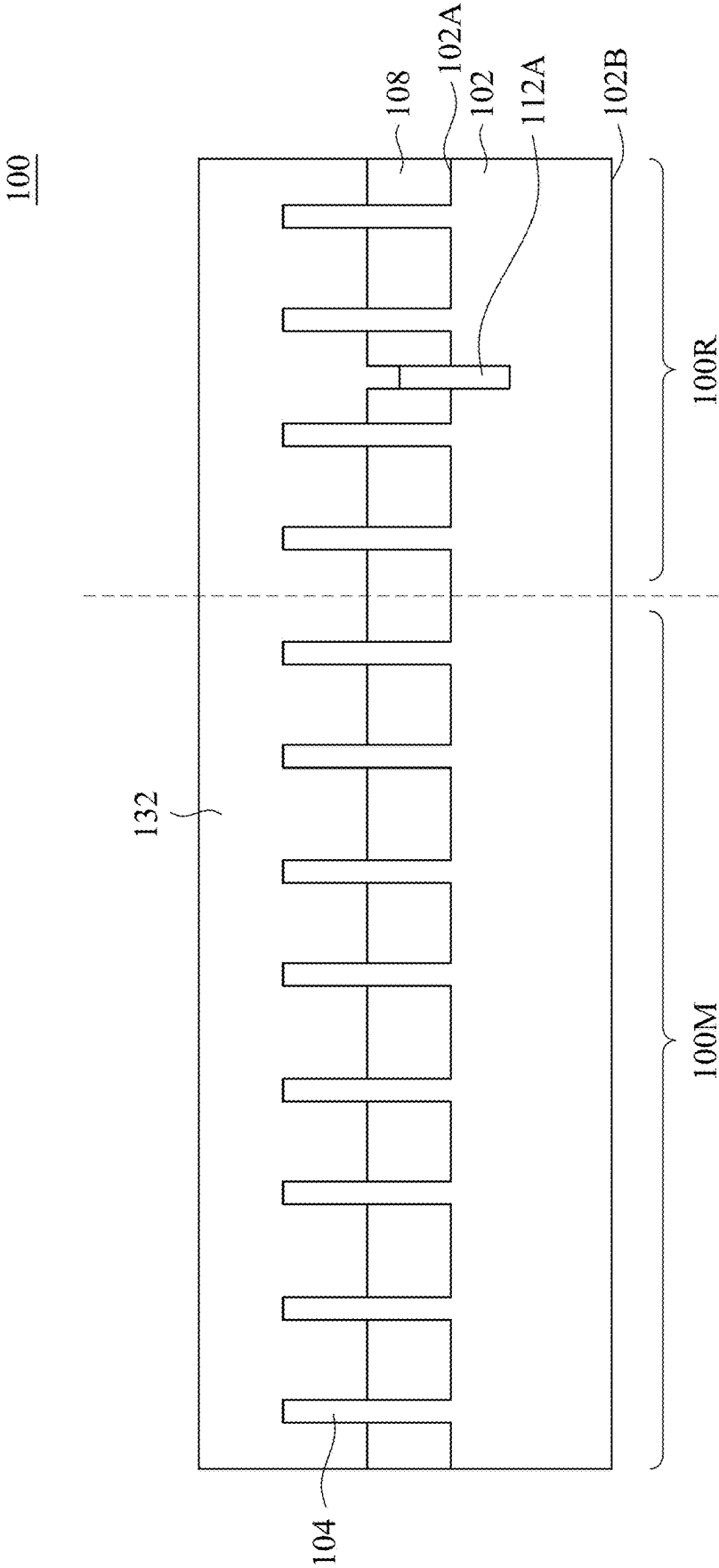


FIG. 12A

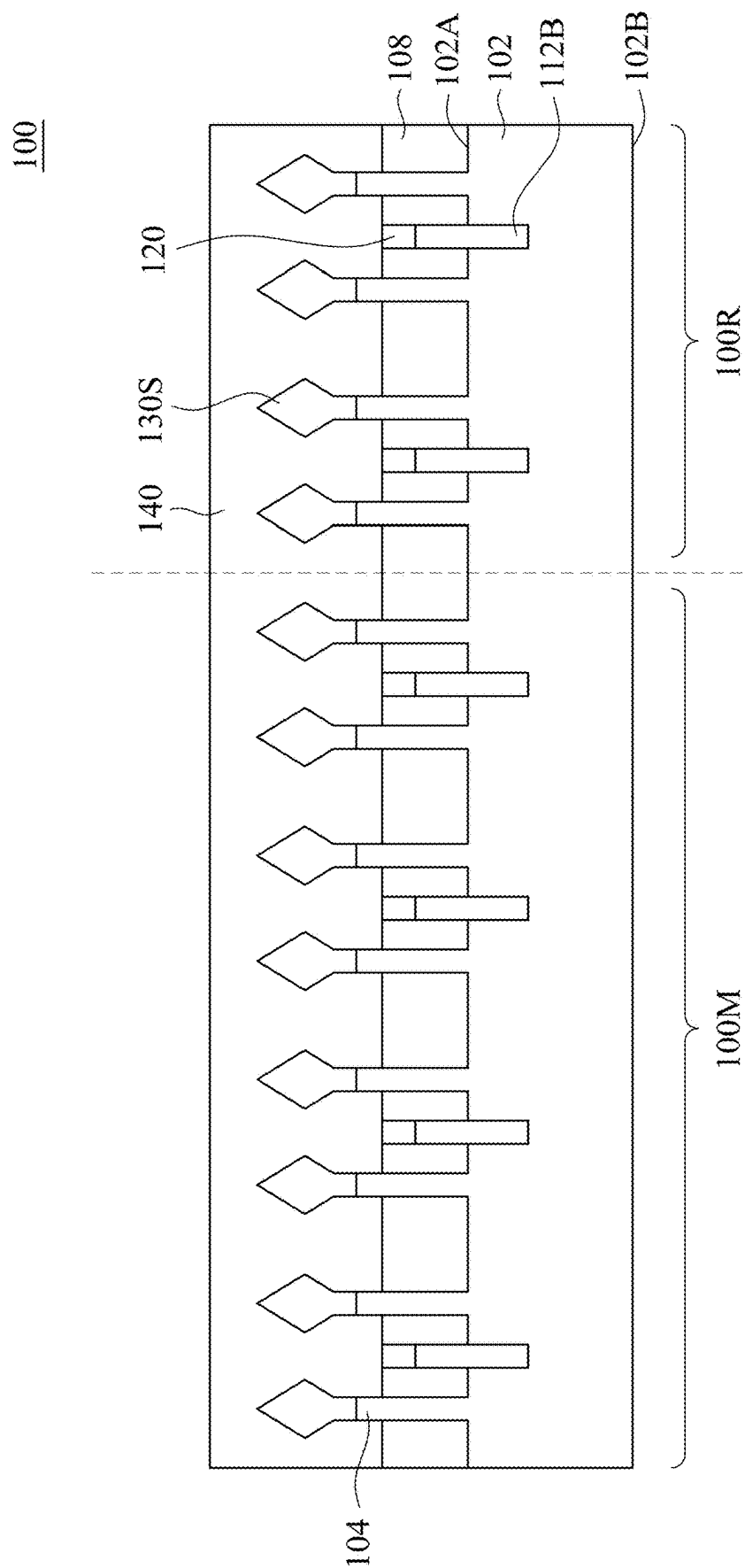


FIG. 12B

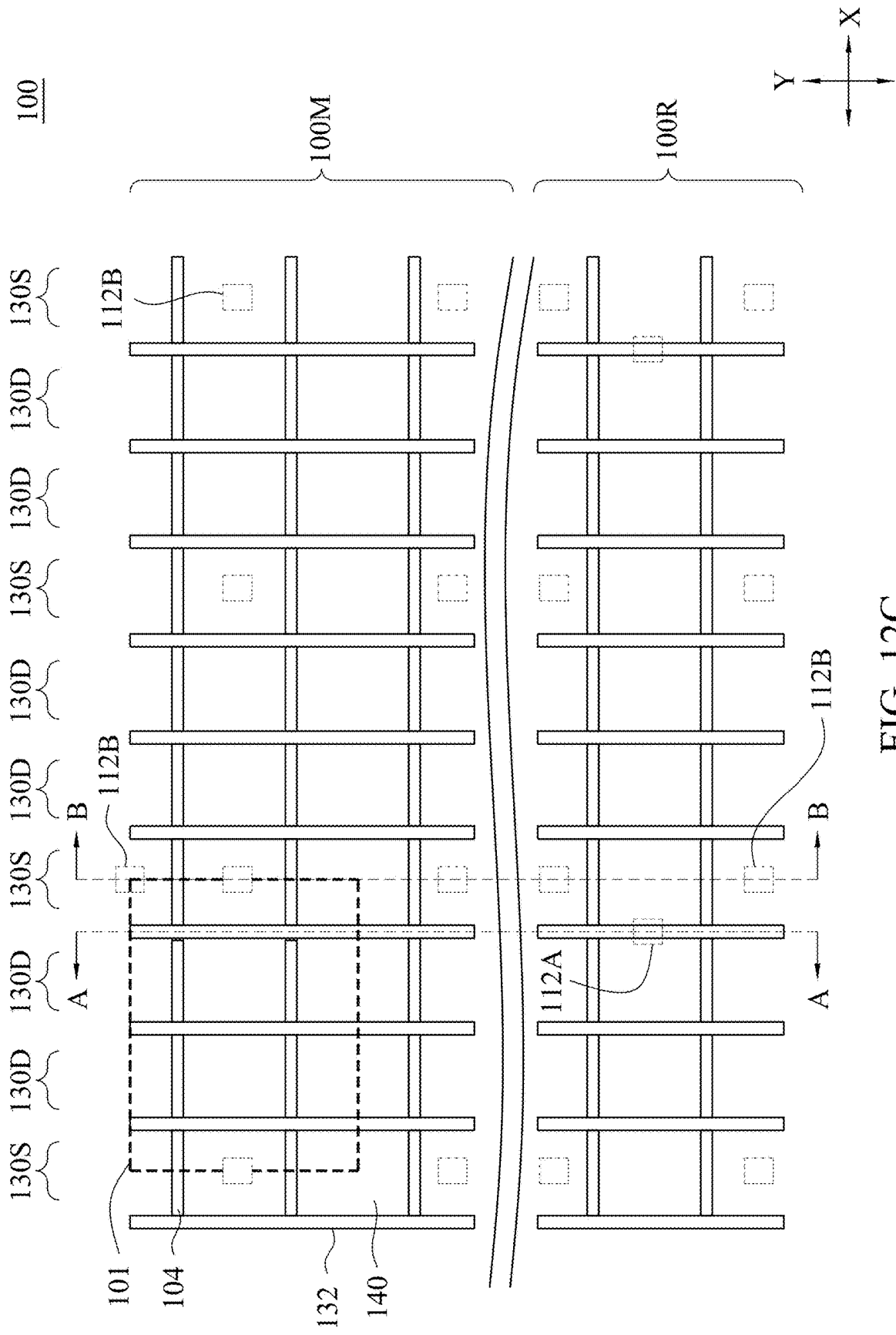


FIG. 12C

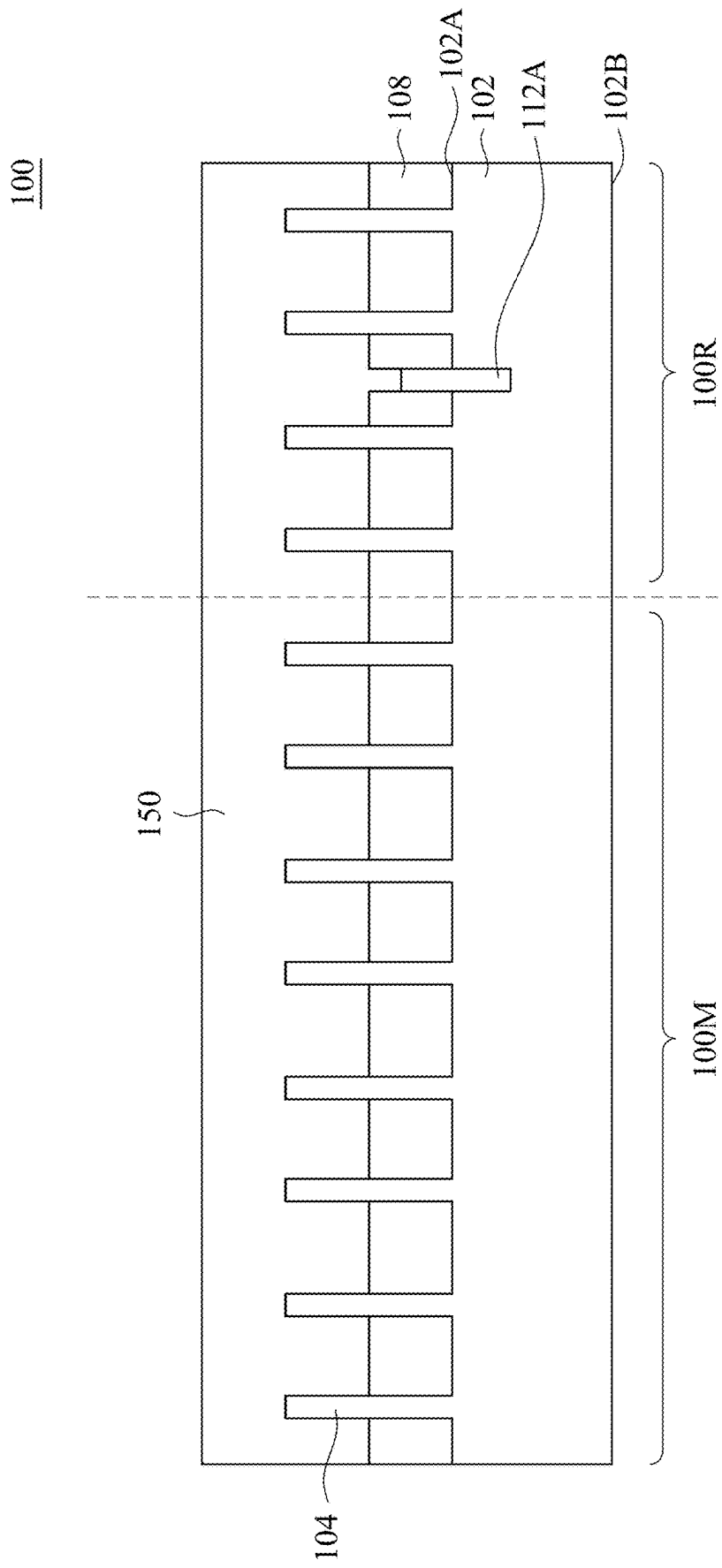


FIG. 13A



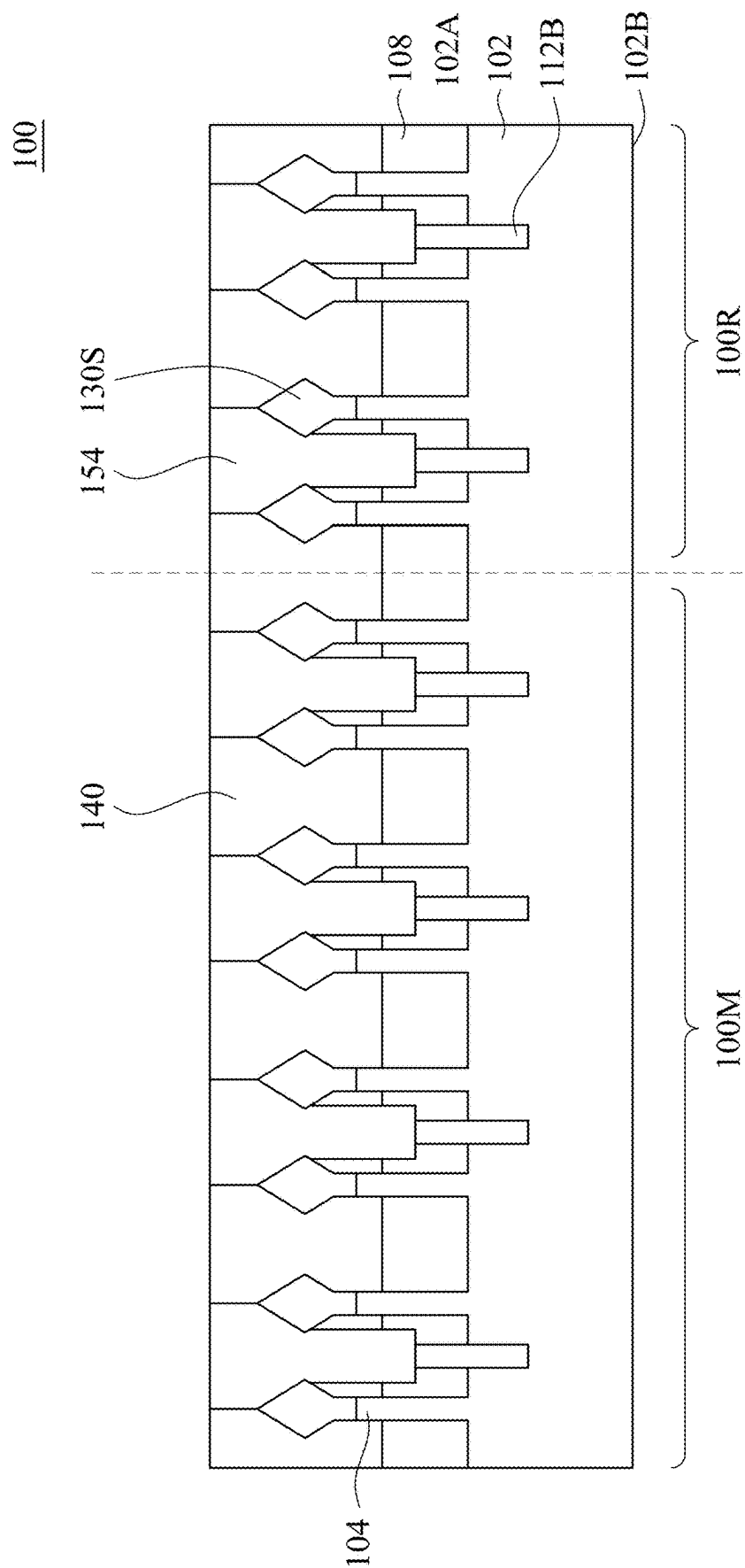


FIG. 13B

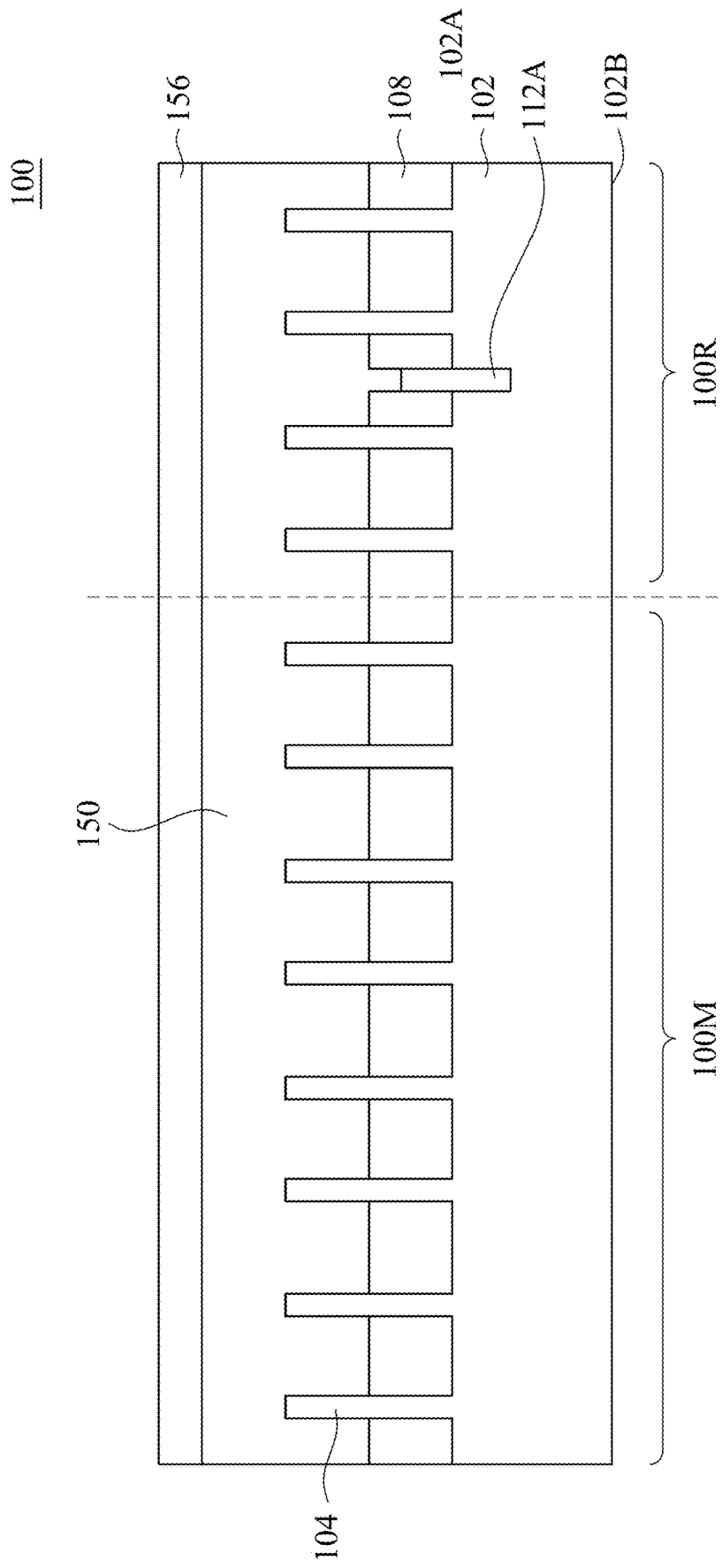


FIG. 14A

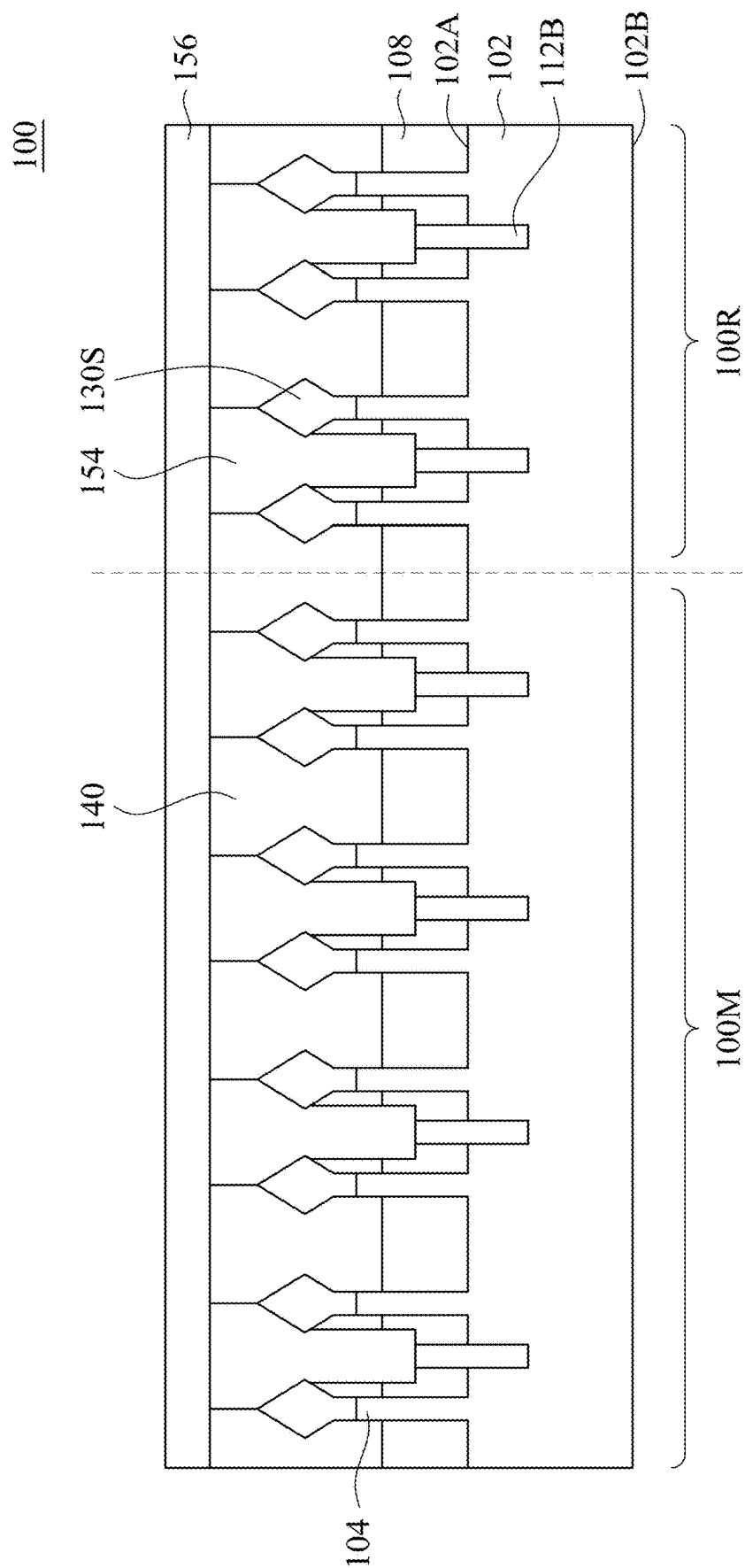
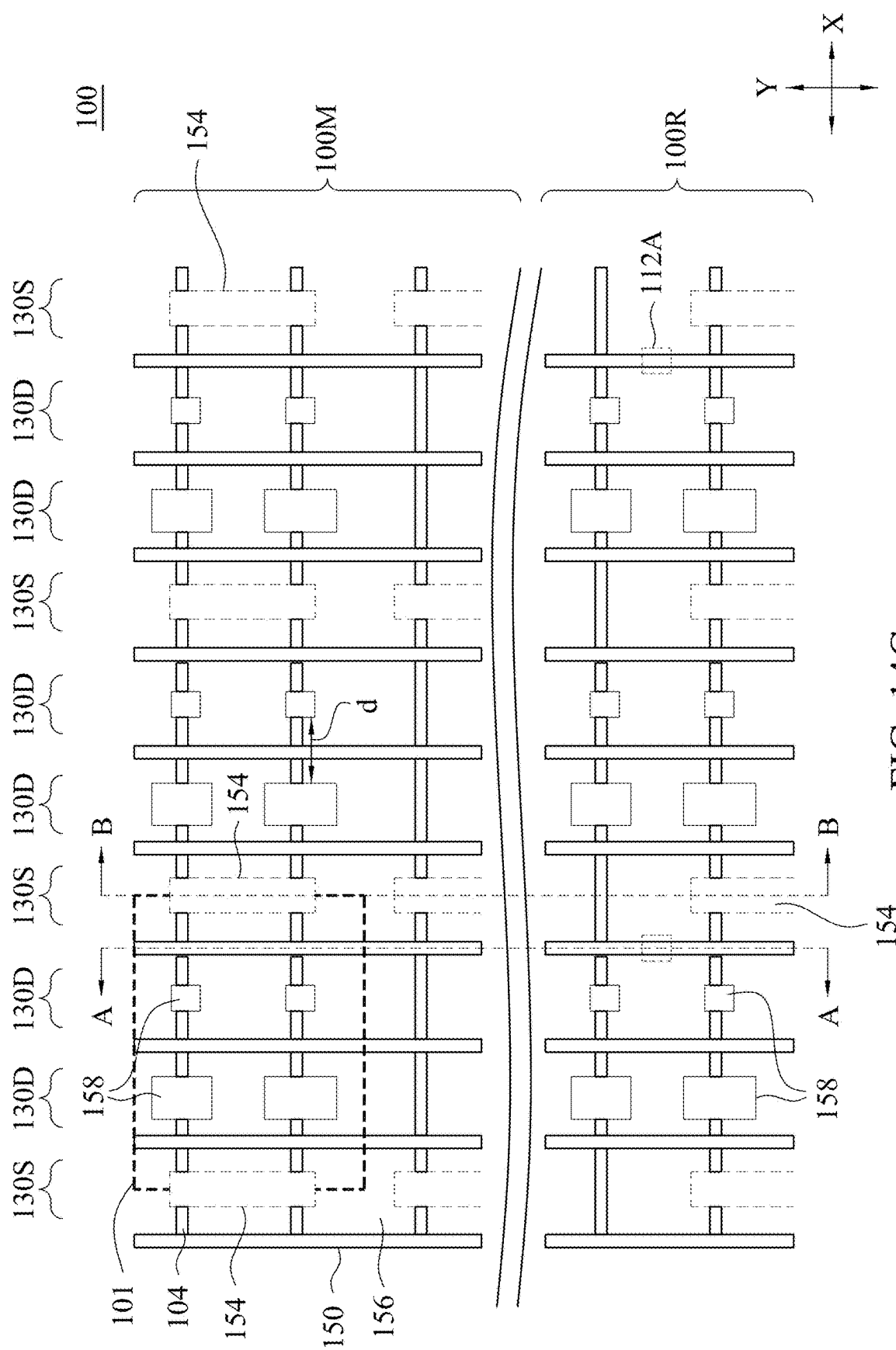


FIG. 14B



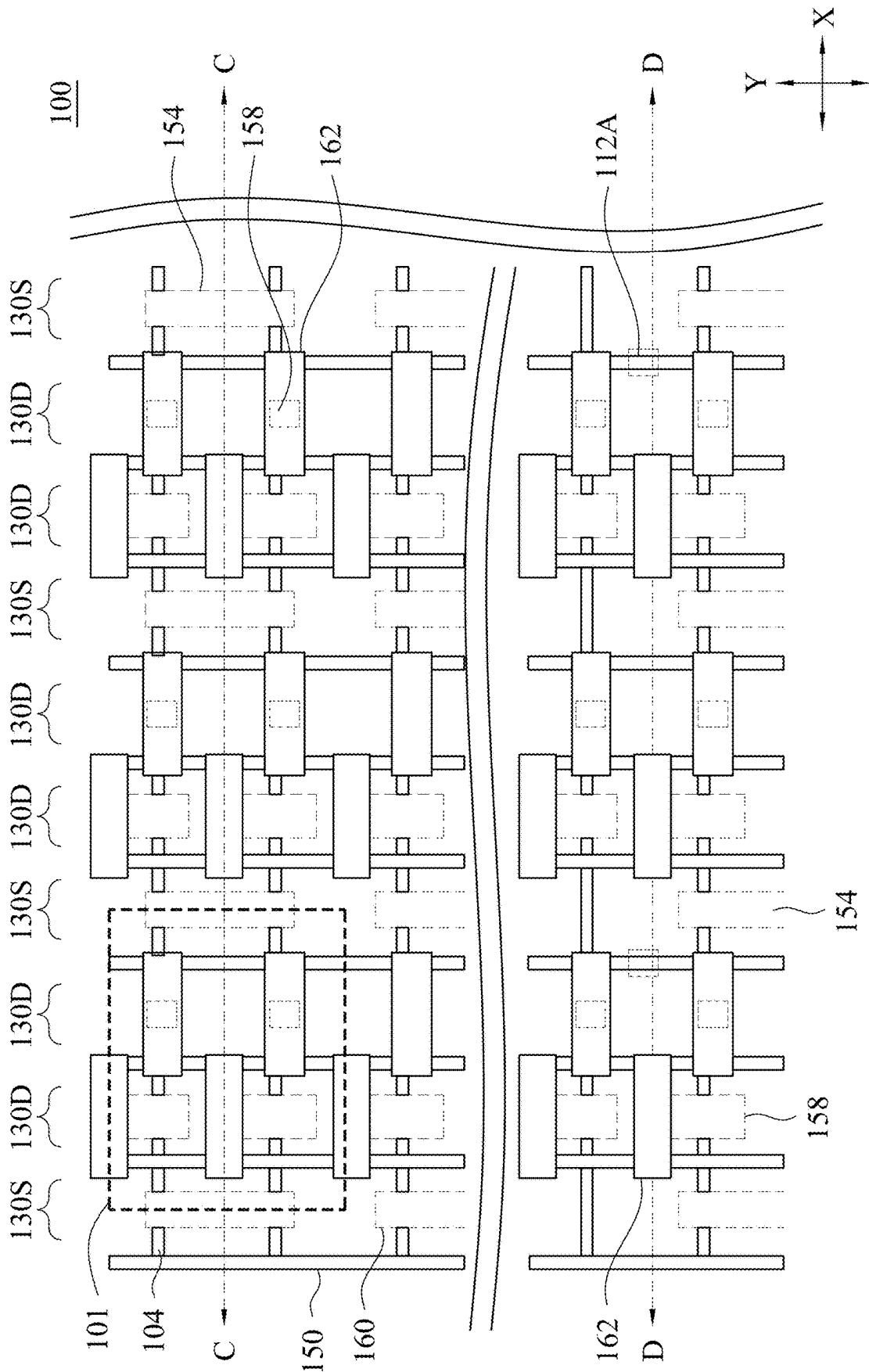


FIG. 15

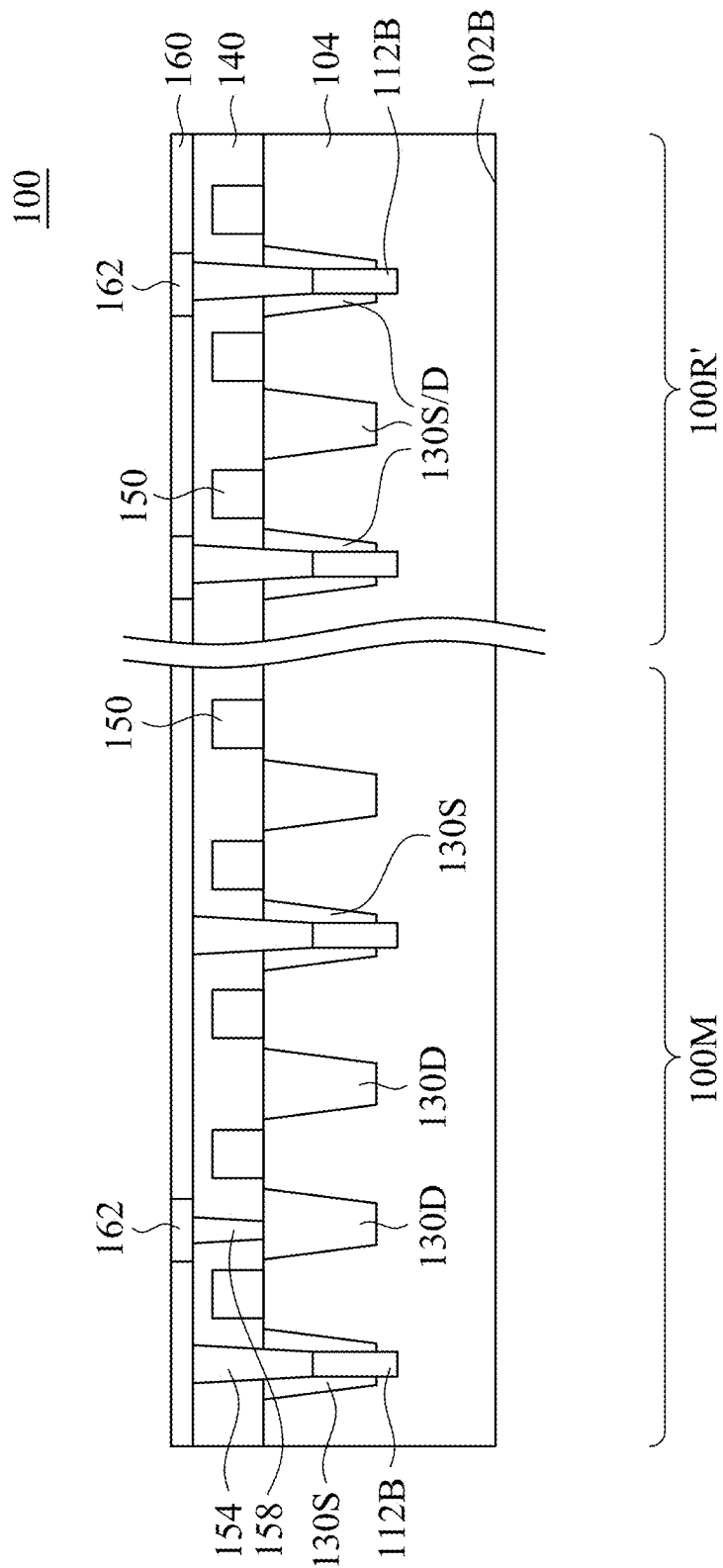


FIG. 16

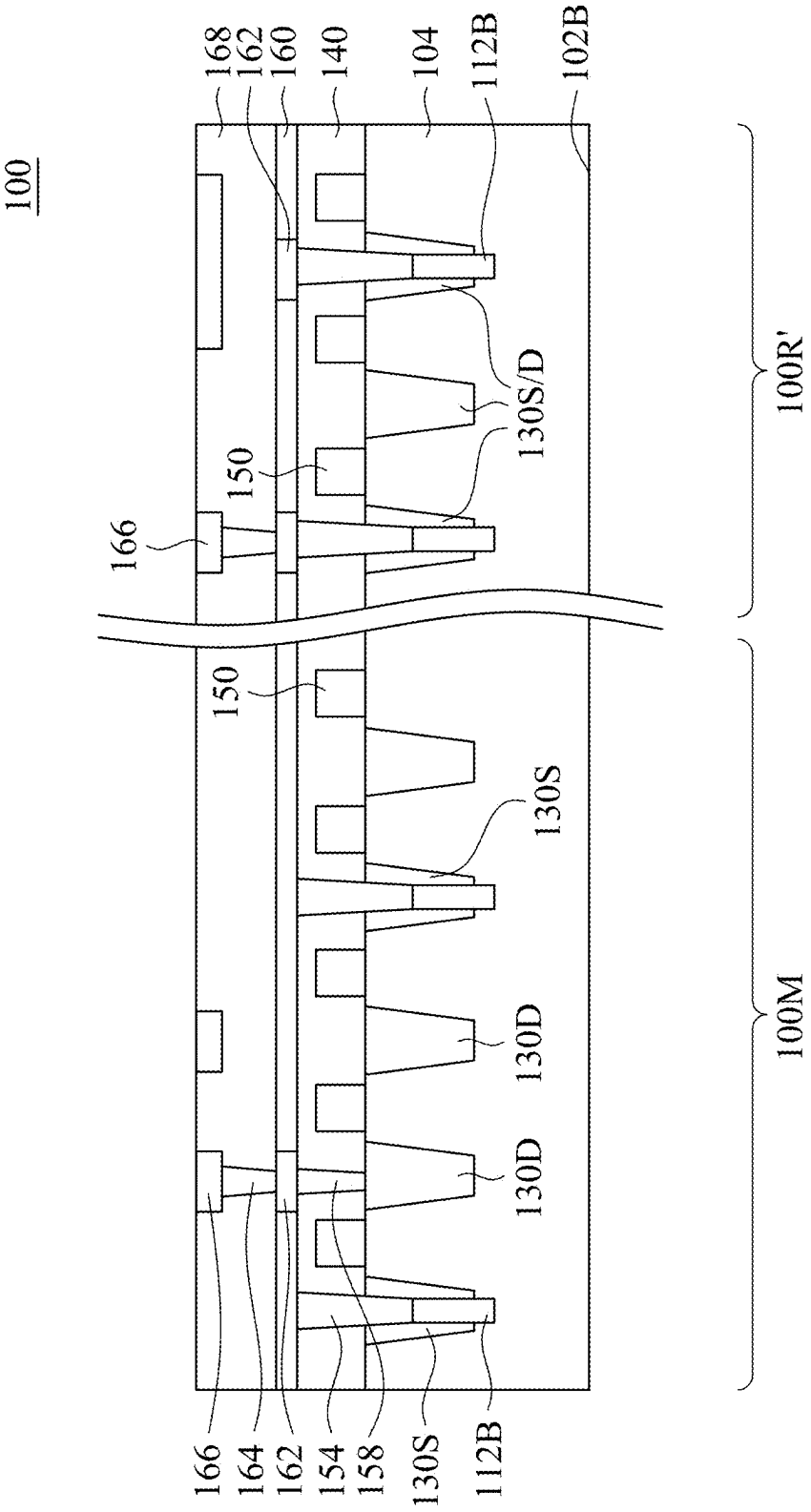


FIG. 17

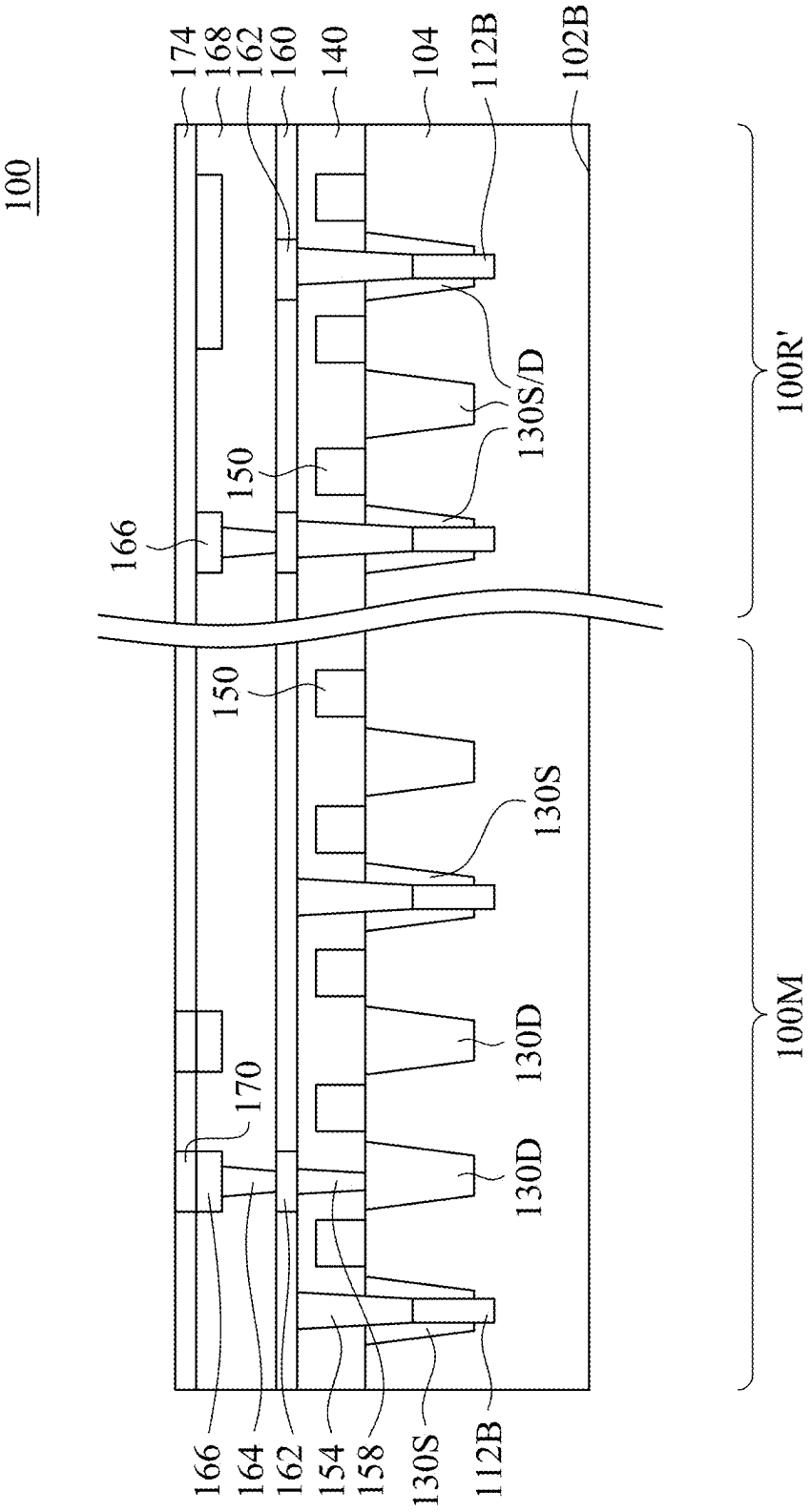


FIG. 18



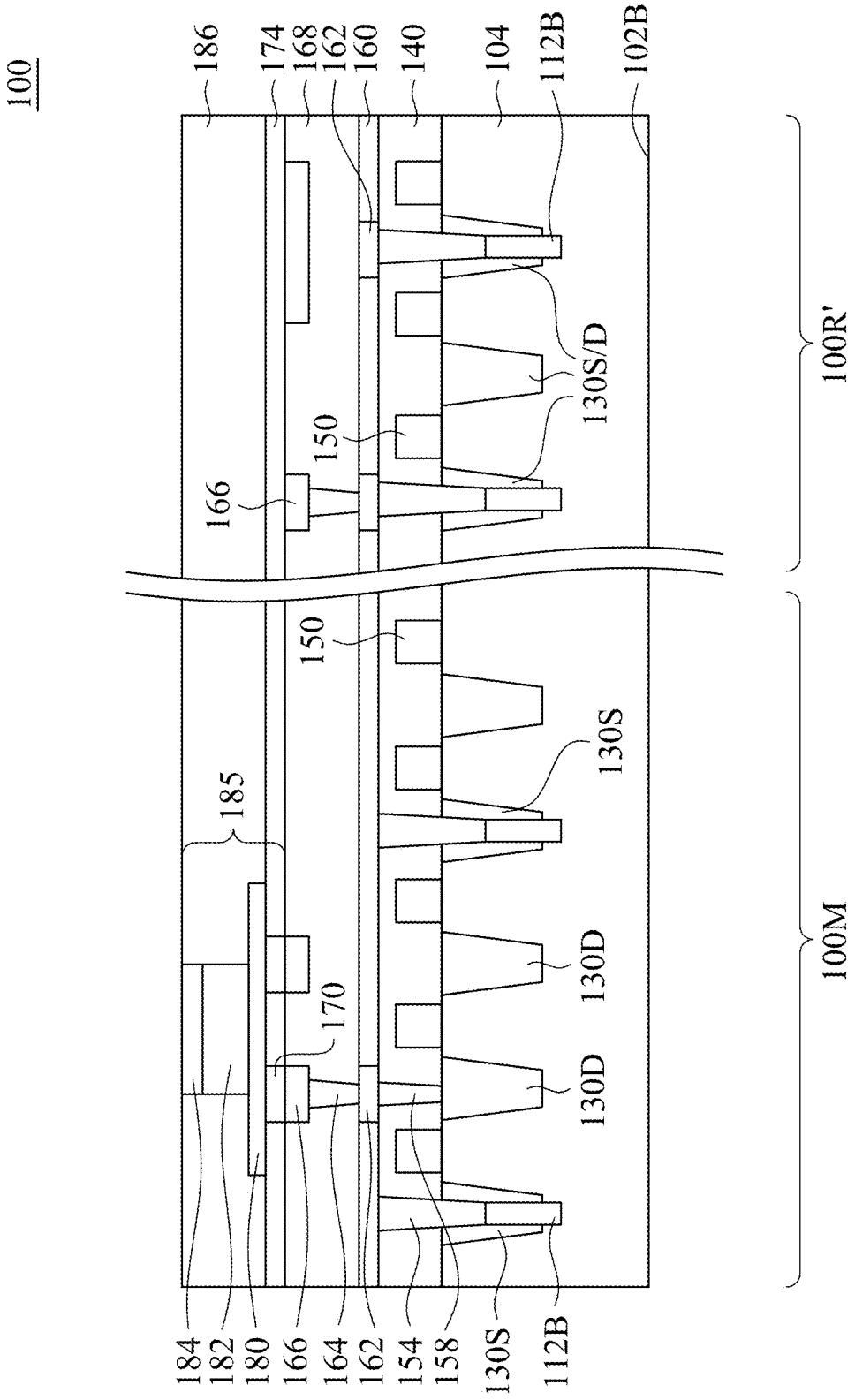


FIG. 19

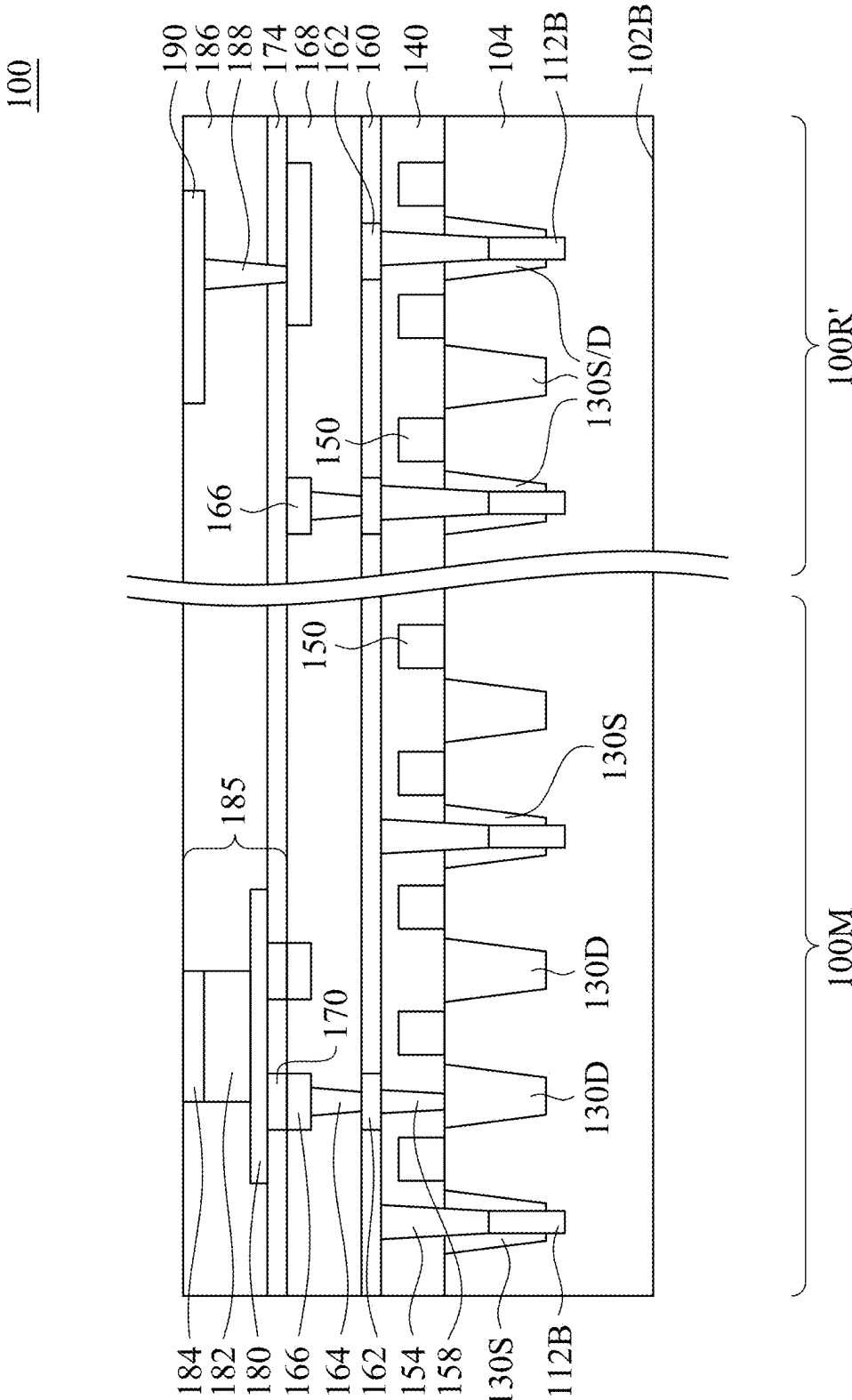


FIG. 20

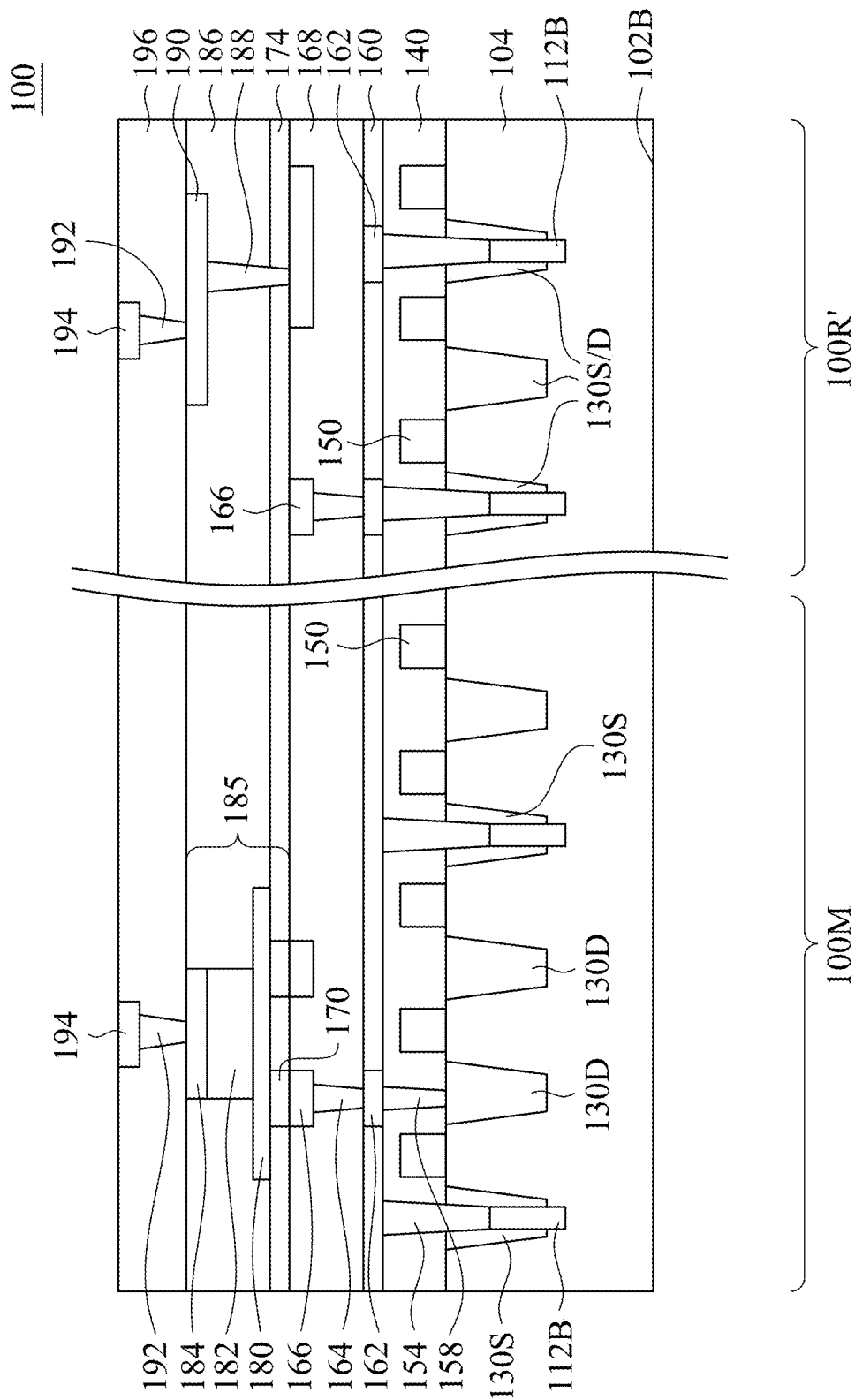


FIG. 21

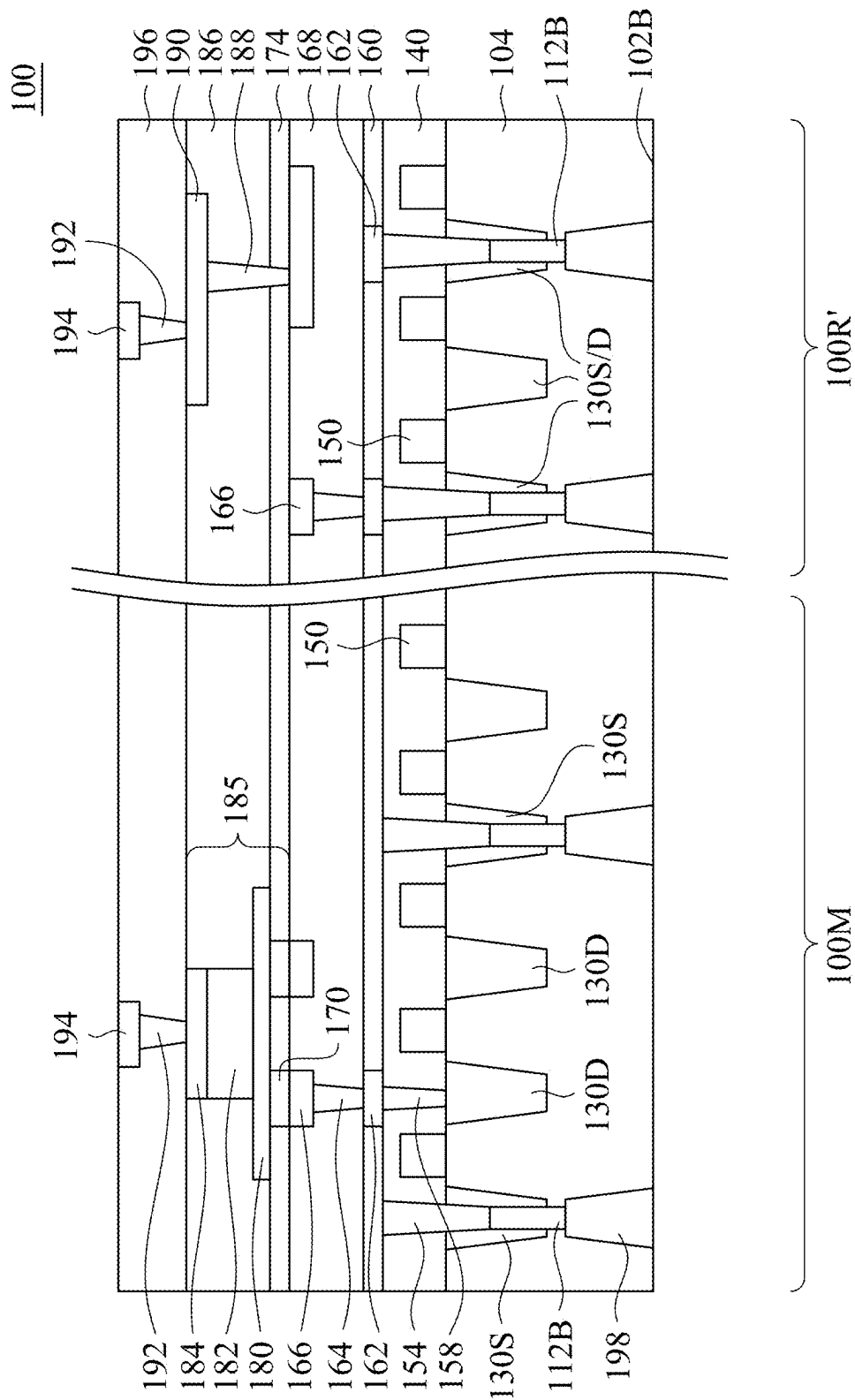


FIG. 22

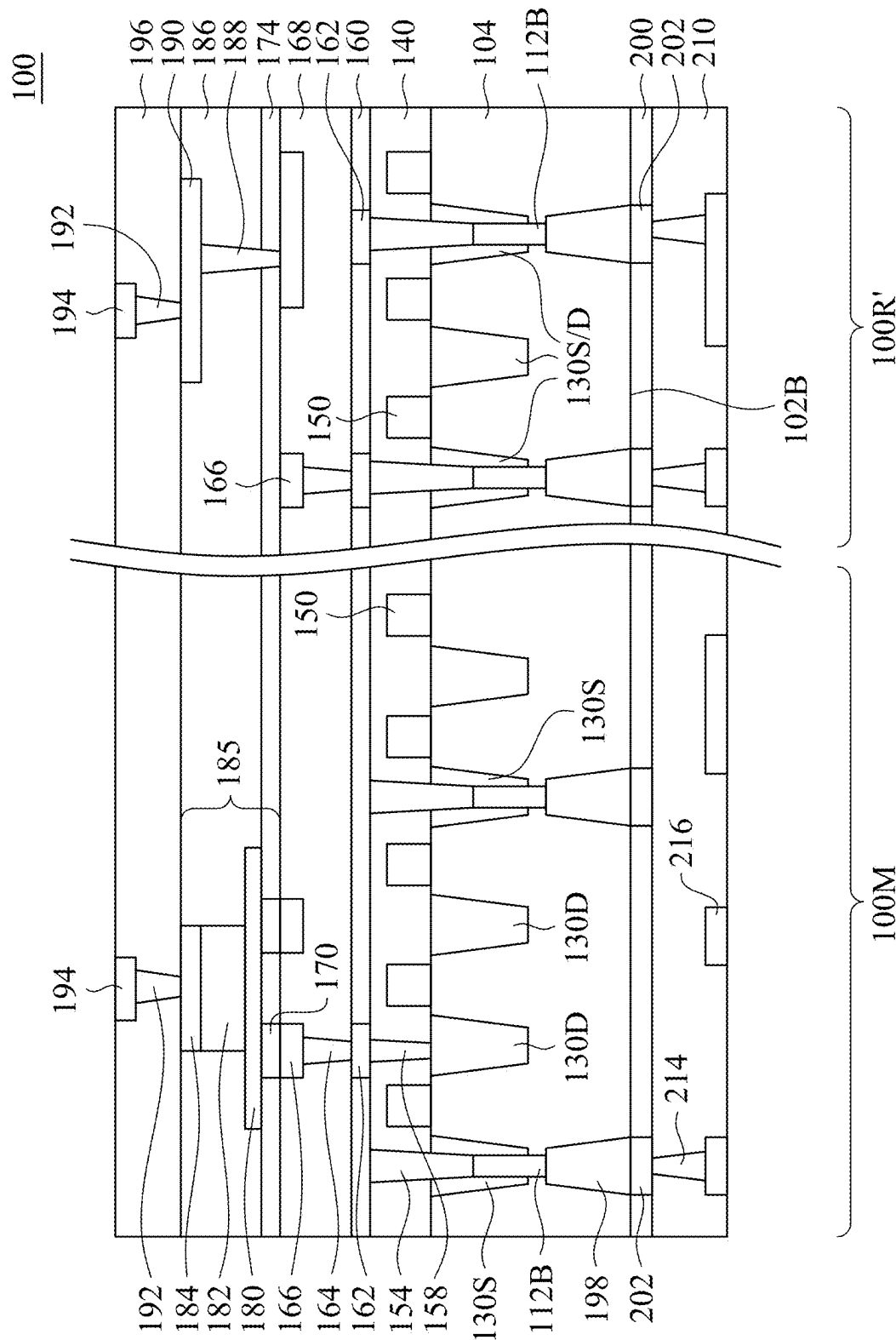


FIG. 23

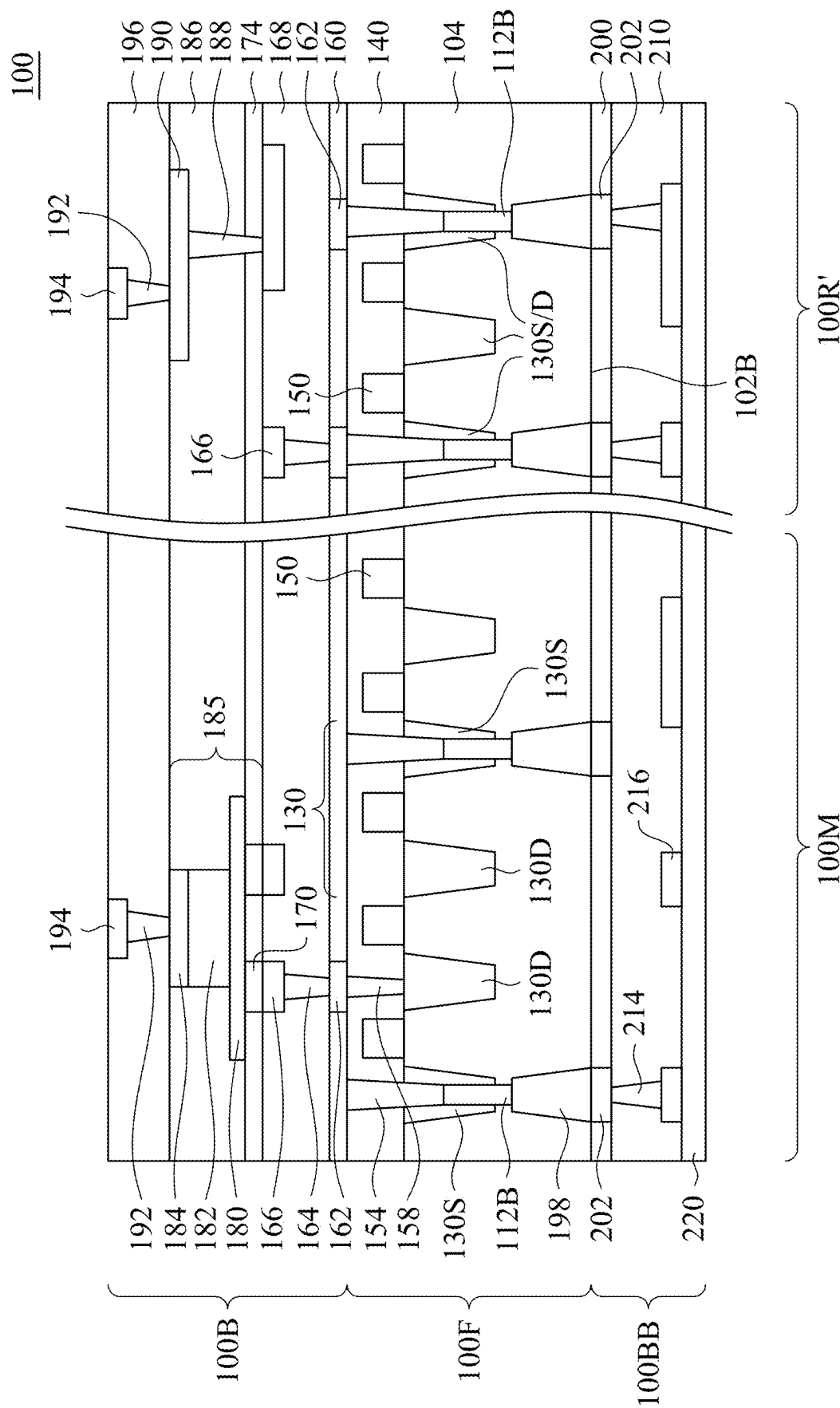


FIG. 24

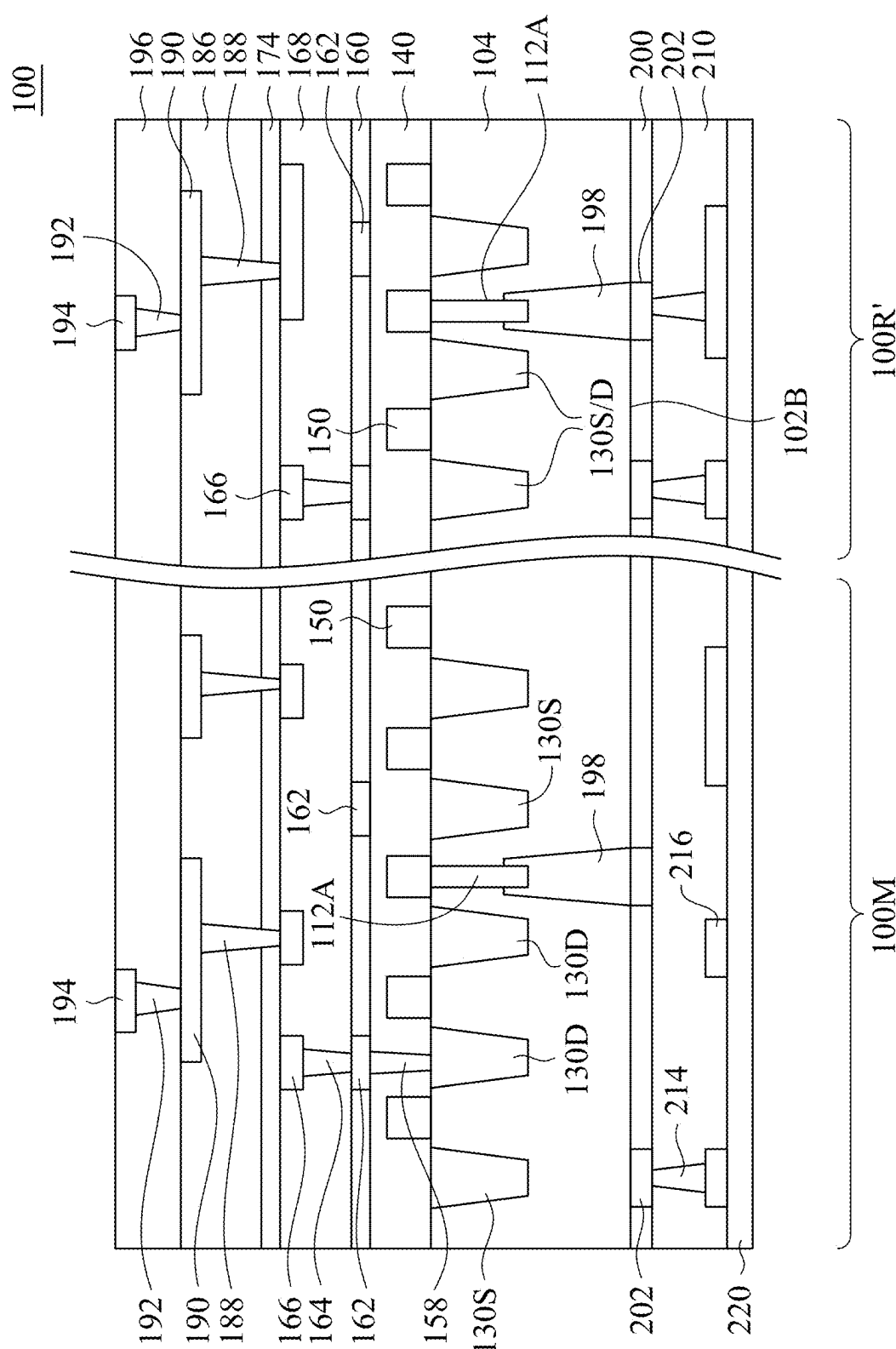


FIG. 25

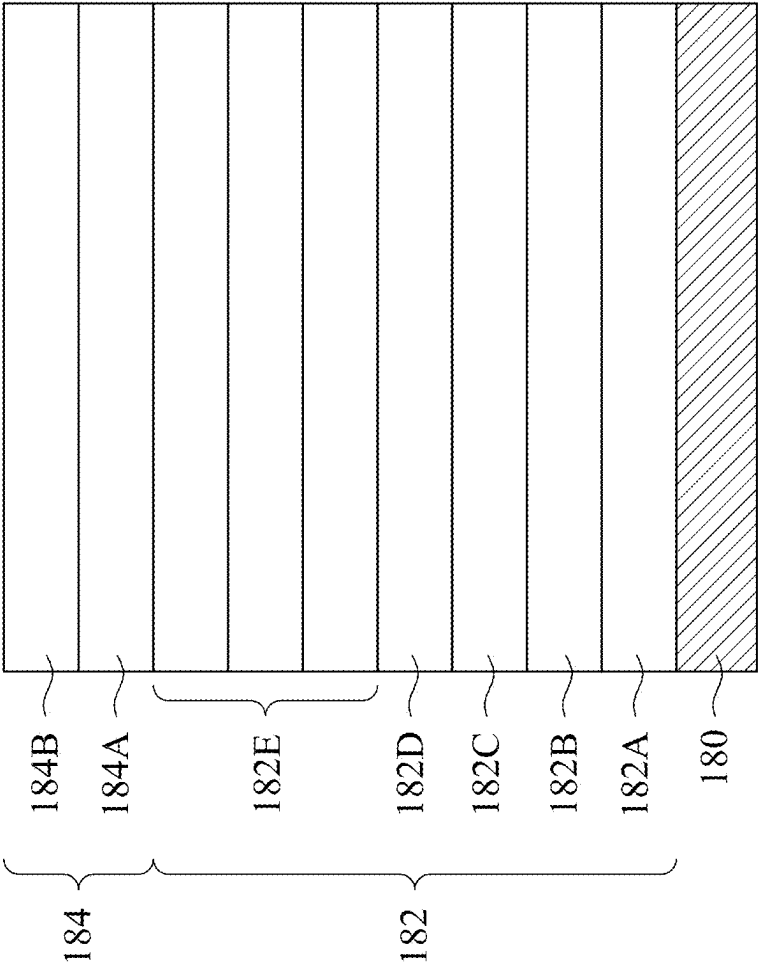


FIG. 26



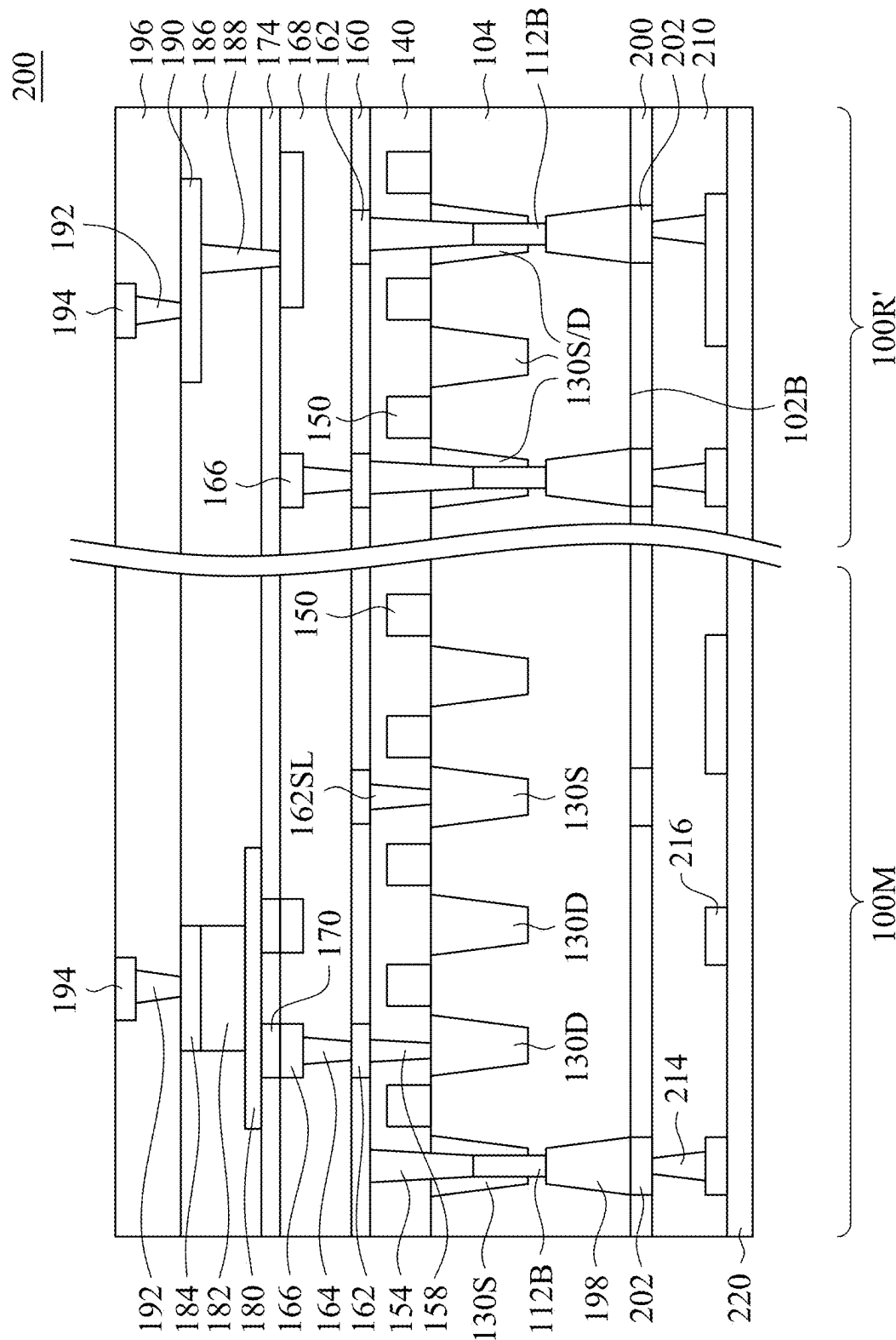


FIG. 27

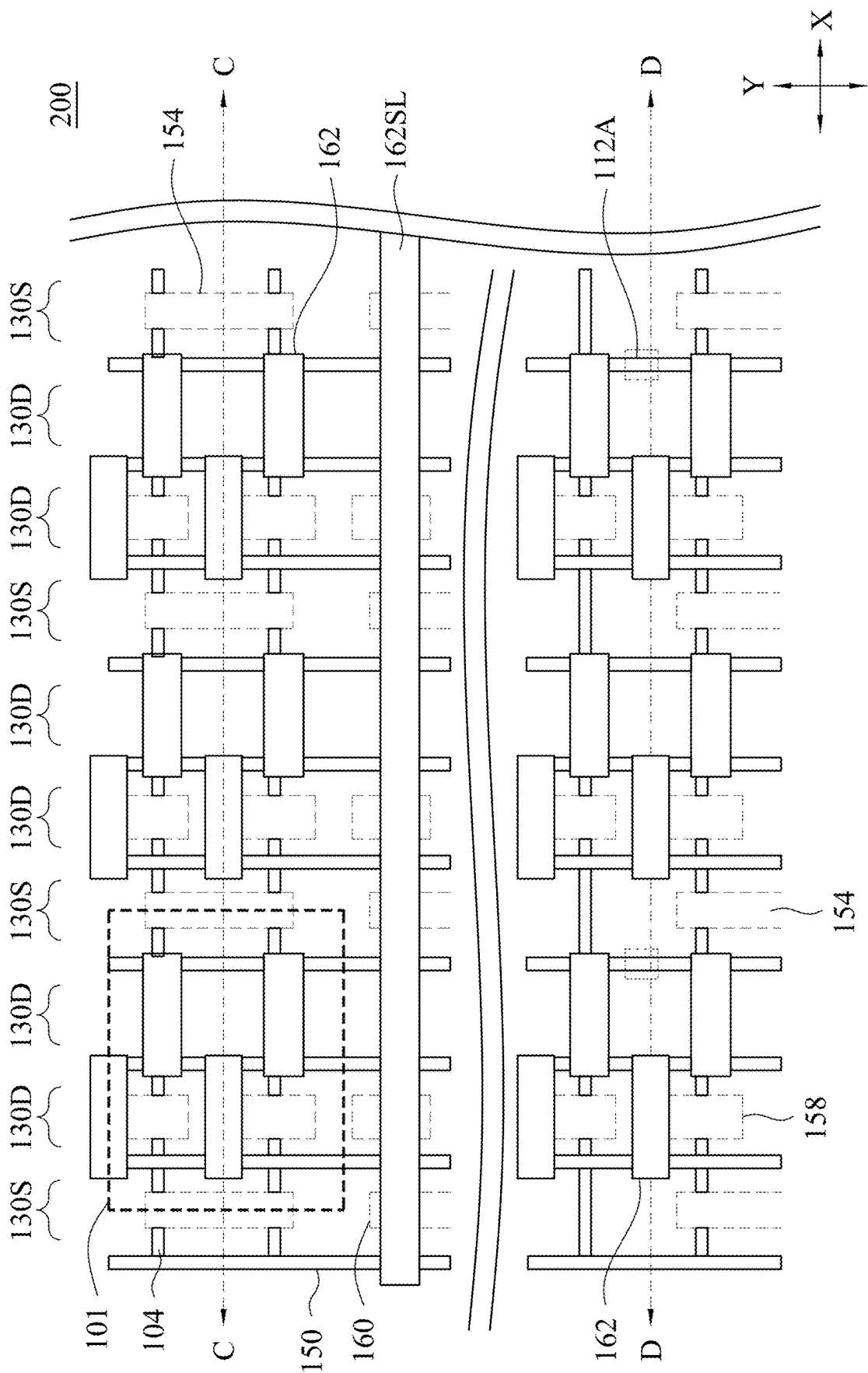
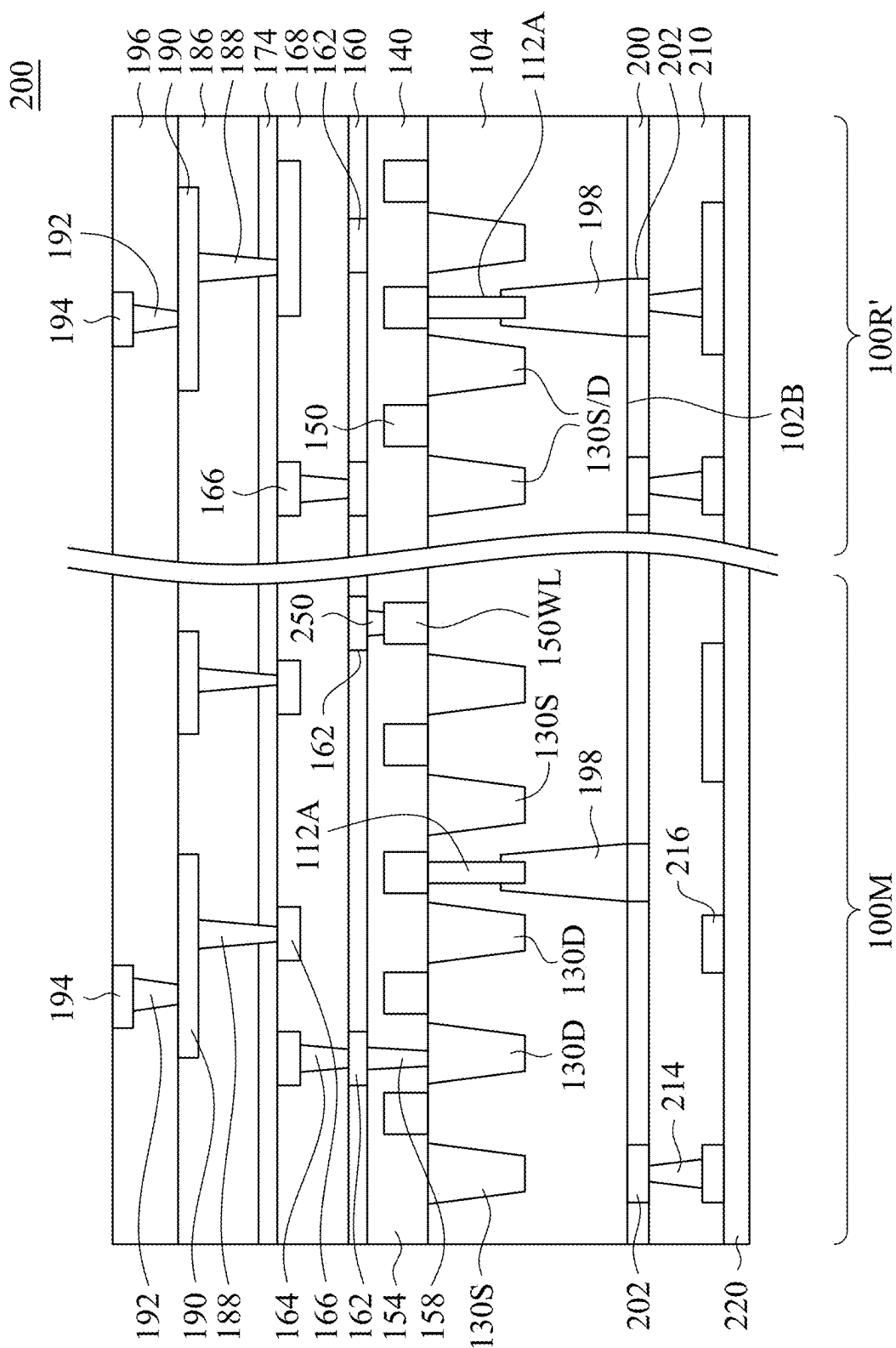


FIG. 28



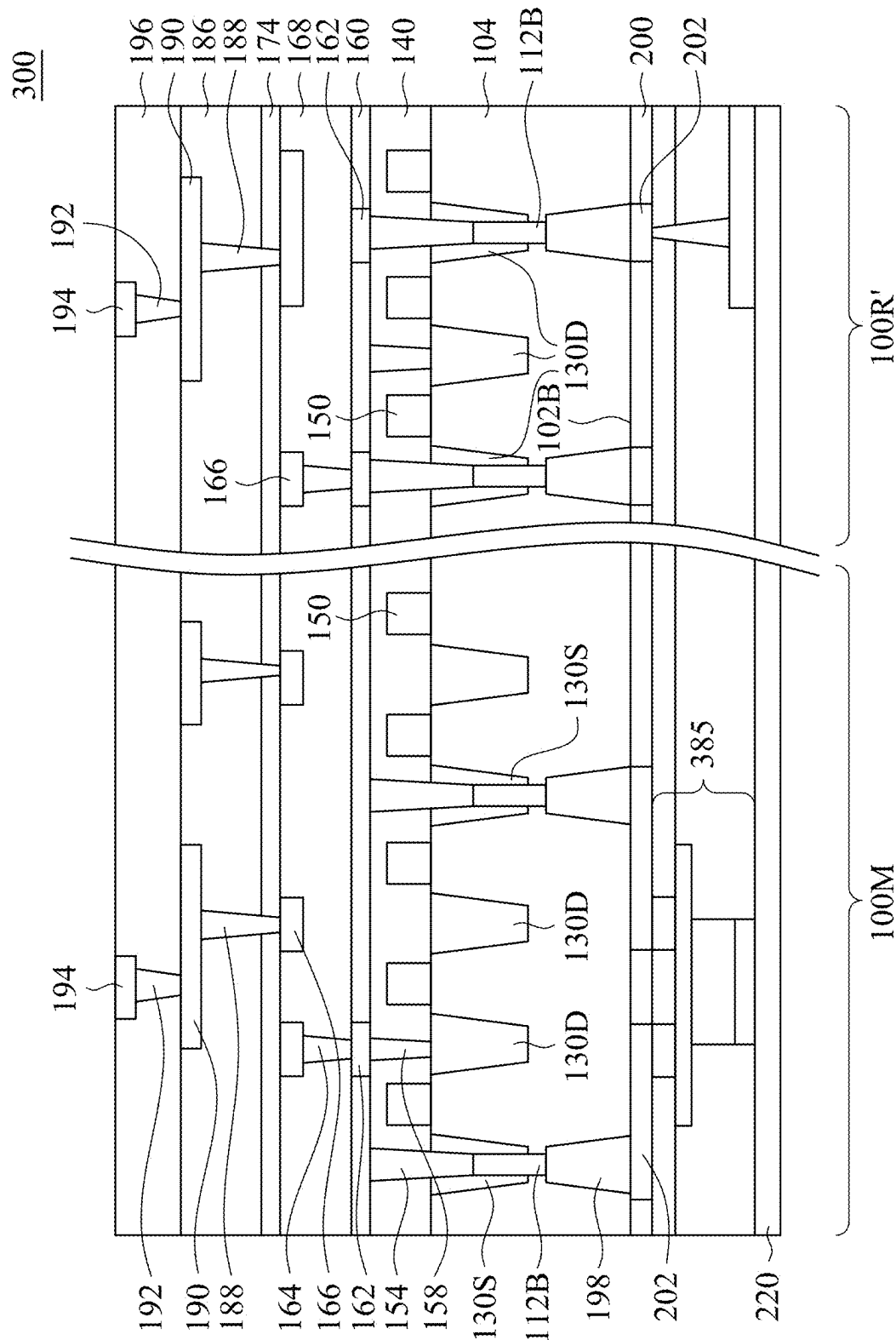


FIG. 30

## SEMICONDUCTOR DEVICE AND METHOD FOR FORMING THE SAME

### PRIORITY

[0001] This application is a continuation of U.S. patent application Ser. No. 18/679,002, filed on May 30, 2024, and entitled “Semiconductor Device and Method for Forming the Same,” which is a divisional of U.S. patent application Ser. No. 18/335,816, filed Jun. 15, 2023, now U.S. Pat. No. 12,022,665 issued on Jun. 25, 2024, and entitled “Semiconductor Device and Method for Forming the Same,” which is a divisional of U.S. patent application Ser. No. 17/216,162, filed Mar. 29, 2021, now U.S. Pat. No. 11,723,218 issued on Aug. 8, 2023, and entitled “Semiconductor Device and Method for Forming the Same,” which application claims priority to of U.S. Provisional Patent Application No. 63/045,285 filed Jun. 29, 2020, and entitled “SOT MRAM with Alternative Power Rails,” which applications are incorporated herein by reference.

### BACKGROUND

[0002] Semiconductor memories are used in integrated circuits for electronic applications, including cell phones and personal computing devices, as examples. One type of semiconductor memory device is Magneto-Resistive Random Access Memory (MRAM), which involves spin electronics that combines semiconductor technology and magnetic materials and devices. The spins of electrons, through their magnetic moments, rather than the charge of the electrons, are used to store bit values.

[0003] Conventional MRAM cells are Spin-Transfer Torque (STT) MRAM cells. A typical STT-MRAM cell may include a Magnetic Tunnel Junction (MTJ) stack, which includes a pinning layer, a pinned layer over the pinning layer, a tunnel layer over the pinned layer, and a free layer over the tunnel layer. During the formation of the MRAM cell, multiple blanket layers are deposited first. The blanket layers are then patterned through a photolithography and etching process to form the MTJ stack.

[0004] The STT-MRAM cells suffer from a reliability problem because programming currents have to pass through the tunnel layer, and hence degrade or damage the tunnel layer. Accordingly, Spin Orbit Torque (SOT) MRAM was developed. In the programming of the SOT-MRAM cells, the programming current does not pass through the tunnel layer, and thus the reliability of the SOT-MRAM is improved over the STT-MRAM.

### BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

[0006] FIGS. 1A-14A, 1B-14B, 12C, 14C, 15-26 illustrate the cross-sectional views and plan views of intermediate stages in the formation of a semiconductor device in accordance with some embodiments.

[0007] FIGS. 27-29 illustrate the cross-sectional views and plan views of intermediate stages in the formation of a semiconductor device in accordance with some embodiments.

[0008] FIG. 30 illustrates the cross-sectional views of intermediate stages in the formation of SOT-MRAM devices in accordance with some embodiments.

### DETAILED DESCRIPTION

[0009] The following disclosure provides many different embodiments, or examples, for implementing different features of the invention. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0010] Further, spatially relative terms, such as “underlying,” “below,” “lower,” “overlying,” “upper” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0011] Embodiments discussed herein are to provide examples to enable making or using the subject matter of this disclosure, and a person having ordinary skill in the art will readily understand modifications that can be made while remaining within contemplated scopes of different embodiments. Throughout the various views and illustrative embodiments, like reference numbers are used to designate like elements. Although method embodiments may be discussed as being performed in a particular order, other method embodiments may be performed in any logical order.

[0012] FIGS. 1A to 14A, 1B to 14B, 12C, 14C, and 15 to 30 are exemplary cross-sectional views and plan views of intermediate stages in the formation of semiconductor devices in accordance with various embodiments of the present disclosure. The cross-sectional views in FIGS. 1A to 14A correspond to a cross-section of the plan view shown in FIGS. 12C, 14C, and 15, such as example the cross-section A-A labeled in FIG. 12C. The cross-sectional views in FIGS. 1B to 14B correspond to a cross-section of the plan view shown in FIGS. 12C, 14C, and 15, such as example the cross-section B-B labeled in FIG. 12C. The cross-sectional views in FIGS. 16 to 24, 26, and 30 correspond to a cross-section of the plan view shown in FIG. 15, such as example the cross-section C-C labeled in FIG. 15. The cross-sectional view in FIG. 27 corresponds to a cross-section of the plan view shown in FIG. 28, such as example

the cross-section C-C labeled in FIG. 28. FIGS. 25 and 29 corresponds to a cross-section of the plan view shown in FIGS. 15 and 28, such as example the cross-section D-D labeled in FIGS. 15.

[0013] Referring to FIG. 24, in some embodiments, the semiconductor device 100 includes a front end of line (FEOL) portion 100F and a back end of line (BEOL) portion 100B disposed over a side of the FEOL portion 100F. The semiconductor device 100 also includes a backside BEOL portion 100BB disposed over the other side of the FEOL portion 100F.

[0014] The semiconductor device 100 may include various regions for disposing of various kinds of devices. In some embodiments, the semiconductor device 100 includes a cell region for a memory device, a logic region for logic circuits, routing regions for serving vertical routings, regions for other functional circuits, or a combination thereof. For example, referring to FIGS. 15 and 24, the semiconductor device 100 may include a memory device that includes multiple memory cells 101 arranged in an array within a cell region 100M. Each cell 101 of the memory device includes a memory stack 185 disposed in the BEOL portion 100B in accordance with some embodiments. Each of the memory stacks 185 may be electrically connected to one or more transistors 130 disposed in the FEOL portion 100F within the cell region 100M. Each memory stack 185 may store a single bit, which may be read or written. In some embodiments, the transistors 130 are fin field-Effect transistors (FinFETs) or gate-all-around field-effect transistors (GAAFETs).

[0015] In some embodiments, a routing region 100R is formed adjacent to the cell region 100M in the Y-direction as illustrated in FIG. 15. Alternatively, a routing region 100R' (e.g., referring to FIG. 24) may be formed adjacent to the cell region 100M in a direction perpendicular to the Y-direction (for example, the X-direction as illustrated in FIG. 15). In some embodiments, the routing region 100R and the routing region 100R' are connected. The routing regions 100R and 100R' provide vertical routings for making electrical connection between the BEOL portion 100B and the backside BEOL portion 100BB. However, in accordance with some embodiments, the routing regions 100R and 100R' are omitted, and the vertical routings are integrated into any regions of the semiconductor device 100, such as the cell region 100M and/or the logic regions.

[0016] Turning to FIG. 1A and 1B and FIG. 12C, intermediate stages in the formation of the semiconductor device 100 are illustrated. Substrate 102 includes a first side 102A and a second side 102B opposite to the first side 102A. The substrate 102 may be a semiconductor substrate, such as silicon, doped or undoped, or an active layer of a semiconductor-on-insulator (SOI) substrate. The semiconductor substrate may include other semiconductor materials, such as germanium; a compound semiconductor including silicon carbide, gallium arsenic, gallium phosphide, gallium nitride, indium phosphide, indium arsenide, and/or indium antimonide; an alloy semiconductor including silicon germanium (SiGe), GaAsP, AlInAs, AlGaAs, GaInAs, GaInP, and/or GaInAsP; or combinations thereof. Other substrates, such as multi-layered or gradient substrates, may also be used.

[0017] Multiple protrusions 104 are formed over the first side 102A of the substrate 102 in accordance with some embodiments. The protrusions 104 may include fins or

stacks of laterally extended nanowires. The protrusions 104 extend along with the X-direction as illustrated in FIG. 12C. A mask layer 106 is formed over the protrusions 104 in accordance with some embodiments. The mask layer 106 may help to define patterns of the protrusions 104 and protect the protrusions 104 from being damaged in subsequent processes. In some embodiments, the mask layer 106 includes a pad layer and a hard mask over the pad layer. The pad layer may include an oxide such as silicon oxide. The hard mask may include a nitride such as silicon nitride, aluminum nitride, or a combination thereof. The protrusions 104 may be formed from the substrate 102 or by epitaxial depositing. For example, the protrusions 104 have the same material as the substrate 102 in accordance with some embodiments. However, in other embodiments, the protrusions 104 have a material different from the substrate 102.

[0018] In FIGS. 2A and 2B, an insulating layer 108 is formed between neighboring protrusions 104 and covers the mask layer 106 and the protrusions 104 in accordance with some embodiments. In some embodiments, the insulating layer 108 includes a multi-layer structure, such as having isolation features disposed over one or more liners. The one or more liners may be formed over the sidewalls of the protrusions 104 and the upper surface of the first side 102A of the substrate 102. In some embodiments, the liners include silicon oxide, silicon nitride, silicon oxynitride, or a combination thereof. The isolation features may include silicon oxide, silicon oxynitride, a spin-on dielectric material, or a low-k dielectric such as porous silicon oxide or other suitable dielectric materials having a dielectric constant lower than 3.9. The isolation features may be formed by flowable CVD (FCVD) (e.g., a CVD-based material deposition in a remote plasma system and post curing to make it convert to another material, such as an oxide), high-density plasma chemical vapor deposition (HDP-CVD), sub-atmospheric CVD (SACVD), or by spin on.

[0019] Turning to FIGS. 3A and 3B, a polishing process such as chemical mechanical polish (CMP) is performed to remove a portion of the insulating layer 108 in accordance with some embodiments. The polishing process may be performed using the mask layer 106 as an etching stop. In some embodiments, this polishing process is omitted.

[0020] In FIGS. 4A and 4B, buried contact holes 110A and buried contact holes 110B are formed in the insulating layer 108 and adjacent to the protrusions 104 in accordance with some embodiments. In FIGS. 5A and 5B, the buried contact holes 110A and 110B are filled with a conductive material in accordance with some embodiments. In FIGS. 6A and 6B, a planarizing process such as CMP is performed to remove excessive portions of the conductive material to form buried contacts 112A and buried contacts 112B in accordance with some embodiments. For example, a portion of the conductive material over the insulating layer 108 and the mask layer 106 is removed.

[0021] In some embodiments, the buried contact holes 110A and 110B have a round shape, a square, or a rounded square in a plan view. In other embodiments, the buried contact holes 110A and 110B have a shape, such as an ellipse, a rectangle, or a rounded rectangle, that has a long axis substantially parallel with the protrusions 104 (e.g., substantially parallel with the X-direction illustrated in FIG. 12C) in a plan view. In some embodiments, the buried contact holes 110A and 110B have a bottom that is lower than the bottom of the protrusions 104 and the top surface

**102A** of the substrate **102**. For example, the buried contact holes **110A** and **110B** may have a depth *D* of about 10 nm to about 50 nm deeper than the bottom of the protrusions **104** or the top surface **102A** of the substrate **102**. The buried contact holes **110A** and the buried contact holes **110B** may have a diameter of about 10 nm to about 40 nm. In some embodiments, the buried contact holes **110A** or the buried contact holes **110B** have an aspect ratio of about 1:10 to about 1:100. The buried contact holes **110A** and the buried contact holes **110B** may be formed in the same lithography and etching processes. Alternatively, the buried contact holes **110A** and the buried contact holes **110B** are formed in the same etching process but with separate lithography processes.

**[0022]** The buried contacts **112A** are formed underlying the subsequently formed gate electrode **132** (e.g., referring to FIG. **13A**) in the routing regions **100R** in accordance with some embodiments. The buried contacts **112A** may also be formed in any regions of the semiconductor device **100**, including, for example but not limited, the cell region **100M**, the logic region, other routing regions, or combinations thereof. The buried contacts **112B** are formed underlying the subsequently formed source features **130S** of transistors **130** (e.g., referring to FIG. **12B**) in the cell region **100M** and the routing region **100R** in accordance with some embodiments. The buried contacts **112B** may also be formed in any regions of the semiconductor device **100**, including, for example but not limited, the logic regions, other routing regions, or combinations thereof. In some embodiments, as illustrated in FIG. **12C**, the buried contacts **112A** and the buried contacts **112B** are staggered from each other in the Y-direction.

**[0023]** In some embodiments, the conductive material of the buried contacts **112A** and **112B** includes a conductive layer over a barrier layer. The conductive layer of the buried contacts **112A** and **112B** may include tungsten, cobalt, ruthenium, rhodium, alloys thereof, or a combination thereof. The barrier layer may be a layer formed along the buried contact holes **110A** and **110B**. The barrier layer of the buried contacts **112A** and **112B** may include titanium, titanium nitride, tantalum, tantalum nitride, tungsten nitride, ruthenium, rhodium, platinum, other noble metals, other refractory metals, their nitrides, combinations of these, or the like. In other embodiments, the barrier layer may be not employed with the buried contacts, however. The conductive material may be deposited by sputtering, physical vapor deposition (PVD), CVD, or atomic layer deposition (ALD).

**[0024]** Turning to FIGS. **7A** and **7B**, the buried contacts **112A** and **112B** are etched back (e.g., etched from top) by an etching process in accordance with some embodiments. Cavities **114A** and **114B** are formed over and expose the buried contacts **112A** and **112B**, respectively. The etching process may be a dry etching process such as reactive ion etching or ion beam etching, a wet etching process, or other suitable etching processes. For example, the buried contact may be etched by a fluorine-based material, such as SF<sub>6</sub>. The etching back process leaves a height *H* of the buried contacts **112A** and **112B** in the buried contact holes **110A** and **110B**. In some embodiments, the height *H* is about 30 nm to about 100 nm.

**[0025]** Turning to FIGS. **8A** and **8B**, a protection layer **120** is formed over the insulating layer **108** and fills the cavities **114A** and **114B** in accordance with some embodiments. The protection layer **120** may include silicon oxide, silicon

oxynitride, a spin-on dielectric material, a photoresist, or a low-*k* dielectric such porous silicon oxide or other suitable dielectric materials having a dielectric constant lower than 3.9. The protection layer **120** may be formed by CVD, HDP-CVD, SACVD, FCVD, or by spin on. In some embodiments, the protection layer **120** includes the same material as the isolation features of the insulating layer **108**.

**[0026]** Turning to FIGS. **9A** and **9B**, a polishing process such as CMP is performed in accordance with some embodiments. In an embodiment, the mask layer **106**, a portion of the insulating layer **108**, and a portion of the protection layer **120** are removed by the polishing process. In some embodiments, upper portions of protrusions **104** are also removed by the polishing process.

**[0027]** Turning to FIGS. **10A** and **10B**, the insulating layer **108** and the protection layer **120** are etched back (e.g., etched from the top) by an etching process in accordance with some embodiments. A portion of the insulating layer **108** and a portion of the protection layer **120** may be removed, and the protrusions **104** may protrude over the top surface of insulating layer **108**. In some embodiments, the insulating layer **108** and the protection layer **120** are etched in the same etching process. In other embodiments, the insulating layer **108** and the protection layer **120** are etched in different etching processes. For example, one of the insulating layer **108** and the protection layer **120** may be etched while the other layer is covered by a patterned photoresist layer, and the other layer is then etched, with or without applying another photoresist layer, after the patterned photoresist layer is removed. In some embodiments, the protection layer **120** has a top surface higher than or substantially level with the top surface of the insulating layer **108**.

**[0028]** In FIGS. **11A** and **11B**, a portion of the protection layer **120** over the buried contacts **112A** is removed by an etching process in accordance with some embodiments. Accordingly, the buried contacts **112A** are exposed while the buried contacts **112B** are still covered by the protection layer **120**. In some embodiments, the etching process illustrated in FIG. **10A** may also include removing the portion of the protection layer **120** over the buried contacts **112A**, and a separate etching process to expose the buried contacts **112A** is thus omitted.

**[0029]** Turning to FIG. **12A**, dummy gate strips **132** are formed over the exposed buried contacts **112A**. As illustrated in FIG. **12C**, the dummy gate strips **132** extend along with the Y-direction and across the protrusions **104**. Although FIG. **12A** only shows the dummy gate strips **132** partially wrap over the protrusion **104**, the dummy gate strips **132** may fully wrap around the protrusions **104** when the protrusions **104** are made of a stack of nanowires, in accordance with some embodiments. The dummy gate strips **132** may include polysilicon. The dummy gate strips **132** may be formed by a method that includes: depositing a dummy gate layer covering the protrusions **104**, the exposed buried contacts **112A**, and the insulating layer **108**; forming a photoresist layer that has strip patterns over the dummy gate layer; and etching the dummy gate layer according to the patterns of the photoresist layer. The photoresist layer may be removed during or after the etching process of etching the polysilicon layer. In some embodiments, gate spacers (not shown in Figures) are formed on exposed surfaces of the dummy gate strips **132**. Any suitable methods of forming gate spacers may be used. In some embodiments,

a deposition such as ALD, CVD, or the like may be used to form the gate spacers. In some embodiments, the gate spacers have a thickness of about 1 nm to about 5 nm. The gate spacers may include any suitable material. For example, the gate spacers may include a dielectric material such as silicon oxide, silicon nitride, silicon carbide, silicon oxynitride, or a combination thereof.

**[0030]** Turning to FIG. 12B and FIG. 12C, source features **130S** and drain features **130D** of transistors **130** are formed over the protrusions **104**, beside the dummy gate strips **132**, in accordance with some embodiments. The source features **130S** and the drain features **130D** are separated by the dummy gate strips **132** (and hence, only source features **130S** are visible in the cross-sectional plane illustrated in FIG. 12B). In some embodiments, the protrusions **104**, beside the portion under the dummy gate strips **132**, are recessed to form recesses, and then the source/drain features **130S** and **130D** are formed over in the recesses by epitaxial growing processes, including CVD deposition techniques (e.g., vapor-phase epitaxy (VPE) and/or ultra-high vacuum CVD (UHV-CVD)), molecular beam epitaxy, and/or other suitable processes. The source/drain features **130S** and **130D** may include Ge, Si, GaAs, aluminum gallium arsenide (AlGaAs), SiGe, gallium arsenide phosphide (GaAsP), GaSb, InSb, indium gallium arsenide (InGaAs), InAs, or other suitable materials. After the recesses are filled with the source/drain feature **130S** and **130D**, further epitaxial growth of a top layer of the source/drain features **130S** and **130D** expands horizontally and facets may start to form, such as diamond shape facets. The source/drain features **130S** and **130D** may be in-situ doped during the epi processes. In some embodiments, the source/drain features **130S** and **130D** is not in-situ doped, and an implantation process is performed to dope the source/drain features **130S** and **130D**. One or more annealing processes may be performed to activate dopants. The annealing processes comprise rapid thermal annealing (RTA) and/or laser annealing processes. Each of the source/drain features **130S** and **130D** may have an impurity concentration from about  $10^{19} \text{ cm}^{-3}$  to about  $10^{21} \text{ cm}^{-3}$ .

**[0031]** In some embodiments, an etching stop layer (not shown in Figures) is conformally formed over the source/drain features **130S** and **130D**. The etching stop layer may be formed of a dielectric material that has a different film property than the source/drain features **130S** and **130D**, to improve the etching selectivity when an etching process is performed in the subsequent manufacturing stages. In some embodiments, the etching stop layer includes silicon nitride, silicon carbide, silicon oxynitride, or combinations thereof.

**[0032]** An insulating layer **140** is disposed between each of the dummy gate strips **132** and over the source/drain features **130S** and **130D**. The insulating layer **140** may include silicon oxide, silicon oxynitride, a spin-on dielectric material, or a low-k dielectric such as porous silicon oxide or other suitable dielectric materials having a dielectric constant lower than 3.9. The insulating layer may be formed by FCVD, HDP-CVD, SACVD, or by spin on. The insulating layer **140** may include a single layer or multiple layers. The insulating layer **140** may have the same material as the isolation features of the insulating layer **108**. In some embodiments, the insulating layer **140** has a top surface substantially level with the top surface of the dummy gate

strips **132** by polishing back. In other embodiments, the insulating layer **140** covers the top of the dummy gate strips **132**.

**[0033]** Turning to FIGS. 13A and 13B, a gate structure **150** is formed over the first side **102A** of the substrate **102** by replacing the dummy gate strips **132** in accordance with some embodiments. The gate structure **150** includes a work function metal layer formed over a gate dielectric layer (or alternatively, multiple work function metal layers). A metal gate electrode is disposed on the work function metal layer. However, numerous other layers, such as an interface layer, liner layer, barrier layer, or other suitable layers, may be included in the gate structure as needed. The gate dielectric layer of the gate structure **150** may include silicon oxide. The silicon oxide may be formed by suitable oxidation and/or deposition methods. Alternatively, the gate dielectric layer of the gate structure **150** may include a high-k dielectric layer such as hafnium oxide ( $\text{HfO}_2$ ),  $\text{TiO}_2$ ,  $\text{HfZrO}$ ,  $\text{Ta}_2\text{O}_3$ ,  $\text{HfSiO}_4$ ,  $\text{ZrO}_2$ ,  $\text{ZrSiO}_2$ , combinations thereof, or other suitable material. The high-k dielectric layer may be formed by ALD and/or other suitable methods.

**[0034]** The work function metal layer is formed for tuning the work function of the later formed metal gate structures in an NMOS or a PMOS. Thus, the work function metal layer may be p-type work function metal materials for PMOS devices or n-type work function metal materials for NMOS devices. Suitable examples of the p-type work function metals, which may have a work function ranging between 4.8 eV and 5.2 eV, include TiN, TaN, Ru, Mo, Al, WN,  $\text{ZrSi}_2$ ,  $\text{MoSi}_2$ ,  $\text{TaSi}_2$ ,  $\text{NiSi}_2$ , WN, other suitable p-type work function metal materials, and combinations thereof. Suitable examples of the n-type work function metal materials, which may have a work function ranging between 3.9 eV and 4.3 eV, include Ti, Ag, TaAl, TaAlC, HfAl, TiAl, TiAlN, TaC, TaCN, TaSiN, Mn, Zr, other suitable n-type work function metal materials, or combinations thereof.

**[0035]** A work function value is associated with the material composition of the work function metal layer. The material of the work function metal layer is chosen to tune a work function value so that the desired threshold voltage ( $V_t$ ) is achieved in the device that is to be formed in the respective region. The work function metal layer can provide uniform threshold voltage ( $V_t$ ) and drain voltage. The work function metal layer may be deposited by CVD, PVD, ALD, and/or other suitable processes. In one example depicted herein, the work function metal layer is formed using an ALD process.

**[0036]** In FIG. 13B, source contact plugs **154** are formed over the source features **130S**. In some embodiments, each of the source contact plugs **154** connects at least two or more adjacent source features **130S** to one of the buried contacts **112B**, as illustrated in FIG. 13B. In other embodiments, each of the source contact plugs **154** connects one source feature **130S** to one of the buried contacts **112B**. The source contact plugs **154** may be formed by suitable lithography, etching, and deposition processes. For example, a photoresist layer may be deposited over the insulating layer **140**. The photoresist layer is patterned to have openings aligning the buried contacts **112B** and their adjacent source features **130S** by a lithography process. The insulating layer **140**, the etch stop layer, and the protection layer **120** over the buried contacts **112B** are etched according to the openings of the photoresist layer to form openings that expose the buried contacts **112B** and the source features **130S**. The openings are filled with a



conductive material with a suitable deposition process. A planarizing process such as a CMP process is then performed to remove excess conductive material over the insulating layer 140. In some embodiments, before the photoresist layer is deposited, one or more dielectric layers (not shown in Figures) is formed over the insulating layer 140 and then etched together with the insulating layer 140 and remain in the final structure of the semiconductor device 100.

[0037] In some embodiments, the source contact plugs 154 include a conductive layer over a barrier layer. The barrier layer of the source contact plugs 154 may be formed of one or more layers of titanium, titanium nitride, tantalum, tantalum nitride, tungsten nitride, ruthenium, rhodium, platinum, other noble metals, other refractory metals, their nitrides, combinations of these, or the like. The conductive layer of the source contact plugs 154 may be a metal material such as tungsten, cobalt, ruthenium, rhodium, alloys thereof, the like, or combinations thereof. The barrier layer or the conductive layer of the source contact plugs 154 may be formed using a suitable process such as CVD, PVD, ALD, plating, or the like.

[0038] Turning to FIGS. 14A, 14B, and 14C, a dielectric layer 156 is deposited over the gate structure 150, the insulating layer 140, and the source contact plugs 154. In some embodiments, the dielectric layer 156 may include silicon oxide, silicon oxynitride, silicon nitride, silicon oxycarbide, polymer, a low-k dielectric, or a combination thereof. The dielectric layer 156 may be formed by FCVD, HDP-CVD, SACVD, or by spin on. In some embodiments, the dielectric layer 156 is omitted.

[0039] Drain contact plugs 158 are then formed over the drain features 130D of the transistors 130 in accordance with some embodiments. The drain contact plugs 158 may be formed by suitable lithography, etching, and deposition processes. For example, a photoresist layer may be blanket deposited over the dielectric layer 156. The photoresist layer is patterned to have openings aligning to the drain features 130D by a lithography process. The dielectric layer 156, the insulating layer 140, and the etch stop layer are etched according to the openings of the photoresist layer to form openings that expose the drain features 130D. The openings are filled with a conductive material with a suitable deposition process. A planarizing process such as the CMP process is then performed to remove the excess conductive material over the dielectric layer 156.

[0040] In some embodiments, the drain contact plugs 158 include a conductive layer over a barrier layer. The barrier layer of the drain contact plugs 158 may be formed of one or more layers of titanium, titanium nitride, tantalum, tantalum nitride, tungsten nitride, ruthenium, rhodium, platinum, other noble metals, other refractory metals, their nitrides, combinations of these, or the like. The conductive material of the drain contact plugs 158 may be a metal material such as tungsten, cobalt, ruthenium, rhodium, alloys thereof, the like, or combinations thereof. The barrier layer or the conductive material of the drain contact plugs 158 may be formed using a suitable process such as CVD, PVD, ALD, plating, or the like.

[0041] As illustrated in FIG. 14C, the drain contact plugs 158 may have at least two different shapes. For example, in an embodiment, one column of a pair of adjacent drain contact plugs 158 has a relatively longer length in the Y-direction (i.e., along with the direction of columns) as

illustrated in FIG. 14C and has a rectangular-like or ellipse-like shape in a plan view. The other column of the pair of adjacent drain contact plugs 158 has a relatively shorter length in the Y-direction as illustrated in FIG. 14C and has a square-like or a circular-like shape in a plan view. In one embodiment, each of the drain contact plugs 158 connects to one drain feature 130D as illustrated in FIG. 14C. In other embodiments, each of the drain contact plugs 158 may connect to two or more drain features 130D. In some embodiments, two adjacent drain contact plugs 158 have a distance of about 30 nm to about 150 nm in the X-direction.

[0042] At the stage illustrated in FIGS. 14A, 14B, and 14C, the processes of manufacturing the FEOL portion 100F have been completed. FIGS. 15 to 26 illustrate intermediate stages of manufacturing the BEOL portion 100B and the backside BEOL portion 100BB in cross-sectional views and plan views. In FIGS. 15 and 16 (corresponding to section C-C labeled in FIG. 15), a dielectric layer 160 is formed over the insulating layer 140 (or the dielectric 156, not shown in FIG. 16), and conductive lines 162 are formed in the dielectric layer 160. In some embodiments, some of the conductive lines 162 are physically and electrically connected to respective drain contact plugs 158 in at least the cell region 100M. For example, as illustrated in FIG. 15, the conductive lines 162 may have a plurality of two adjacent columns. One of the adjacent columns of conductive lines 162 is aligned and connected to the drain contact plugs 158 that has a relatively longer length in the Y-direction (i.e., along with the direction of columns), and the other one of the adjacent columns of conductive lines 162 are aligned and connected to the drain contact plugs 158 that has a relatively short length in the Y-direction. According to this arrangement, two adjacent columns of the drain contact plugs 158 may be partially or completely misaligned from each other in the Y-direction (i.e., along with the direction of columns) but may overlap in the X-direction (i.e., perpendicular to the direction of columns). For example, in FIG. 15, the two adjacent columns of the drain contact plugs 158 are completely misaligned in the Y-direction.

[0043] The conductive lines 162 may be formed using a suitable technique such as damascene, dual-damascene, plating, deposition, the like, or combinations thereof. In some embodiments, the conductive lines 162 are formed by first depositing the dielectric layer 160 and patterning the dielectric layer 160 to form openings (e.g., using a suitable photolithography and etching process), and filling the openings in the dielectric layer 160 with a barrier layer and a conductive layer. The barrier layer of the conductive lines 162 may be formed of one or more layers of titanium, titanium nitride, tantalum, tantalum nitride, tungsten nitride, ruthenium, rhodium, platinum, other noble metals, other refractory metals, their nitrides, combinations of these, or the like. The conductive layer of the conductive lines 162 may be a metal material such as copper, aluminum, cobalt, alloys thereof, the like, or combinations thereof. The barrier layer or the conductive layer of the conductive lines 162 may be formed using a suitable process such as CVD, PVD, ALD, plating, or the like.

[0044] Although not illustrated in the figures, in some embodiments, some of the conductive lines 162 are also physically and electrically connected to the source contact plugs 154 in the routing regions 100R and 100R' for forming vertical routing which providing electrical connections between the BEOL portion 100B and the backside BEOL

portion 100BB (e.g., referring to FIG. 24). In some embodiments, when there are one or more dielectric layers (e.g., dielectric layer 156, not shown in FIG. 16) between the dielectric layers 160 and the source contact plugs 154, the one or more dielectric layers are patterned to expose the source contact plugs 154 within the routing regions 100R and 100R' while manufacturing the conductive lines 162. In some embodiments, the conductive lines 162 within the cell region 100M and the conductive lines 162 within the routing regions 100R and 100R' are formed by separate damascene processes. For example, the conductive lines 162 within the cell region 100M may be formed by a single damascene process, and the conductive lines 162 within the routing regions may be formed by a dual damascene process.

[0045] Turning to FIG. 17, one or more levels of vias 164 and conductive lines 166 are formed within a dielectric layer 168 to make electrical connection to the conductive lines 162. In some embodiments, the dielectric layer 168 is first formed over the conductive lines 162 and the dielectric layer 160. The dielectric layer 168 may be formed of a material similar to those described above for the dielectric layer 160 and may be formed using similar techniques. Openings may be formed in the dielectric layer 168 to expose the conductive lines 162 using suitable photolithography and etching processes. Conductive material may fill the openings to form the vias 164 and the conductive lines 166. A planarization process may be used to remove excess conductive material. In some embodiments, the vias 164 and the conductive lines 166 includes a material similar to those described above for the conductive lines 162.

[0046] Turning to FIG. 18, bottom electrodes 170 are formed to electrically connect the subsequently formed memory stack 185 (e.g., referring to FIG. 19) to the conductive lines 166. The bottom electrodes 170 may be formed within a dielectric layer 174 that is formed over the dielectric layer 168. The dielectric layer 174 may be formed of a material similar to those described above for dielectric layer 160 and may be deposited using similar techniques as dielectric layer 160.

[0047] In some embodiments, the bottom electrodes 170 are formed of multiple layers of material. The material of the bottom electrodes 170 may include Cu, Al, Ti, Ta, W, Pt, Ni, Cr, Ru, Co,  $\text{Co}_x\text{Fe}_y\text{B}_z\text{W}_w$ , titanium nitride (TiN), tantalum nitride (TaN), the like, combinations thereof, or multiple layers thereof. For example, the bottom electrodes 170 may include a tantalum nitride layer and a titanium nitride layer formed over the tantalum nitride layer. The material of the bottom electrodes 170 may be deposited using one or more suitable techniques such as CVD, ALD, PVD, sputtering, plating, the like, or combinations thereof.

[0048] In some embodiments, the bottom electrodes 170 are formed by first depositing the material of the bottom electrodes 170 as one or more blanket layers over the dielectric layer 168 and the conductive lines 166. The material of the bottom electrodes 170 may then be patterned using, for example, a suitable photolithography and etching process to form the bottom electrodes 170. The dielectric layer 174 may then be deposited over the bottom electrodes 170 and a planarization process performed to expose the bottom electrodes 170.

[0049] In some embodiments, the bottom electrodes 170 are formed by first depositing the dielectric layer 174 and patterning the dielectric layer 174 to form openings (e.g., using a suitable photolithography and etching process), and

then filling the openings in the dielectric layer 174 with the material of the bottom electrodes 170. In some embodiments, a planarization process such as a CMP process or a grinding process may be performed to remove excess portions of the material of the bottom electrodes 170.

[0050] Turning to FIG. 19, the formation of a memory stack 185 in the cell region 100M is shown, in accordance with some embodiments. The memory stack 185 may be a SOT-MRAM stack 185. The SOT-MRAM stack 185 includes multiple layers that provide the magnetic memory functionality of the cells 101 of semiconductor device 100. For example, each cell 101 in the cell region 100M may include one SOT-MRAM stack 185. In some embodiments, the SOT-MRAM stack 185 is formed by depositing multiple layers as blanket layers and then patterning the layers to form the SOT-MRAM stack 185 having the desired shape and configuration. In some embodiments, the layers of the SOT-MRAM stack 185 include a Spin-Orbit Torque (SOT) layer 180, a Magnetic Tunnel Junction (MTJ) stack 182, and a top electrode 184. The SOT layer 180, the MTJ stack 182, and/or the top electrode 184 of the SOT-MRAM stacks 185 may each include one or more layers of one or more materials.

[0051] The layers of the SOT-MRAM stack 185 are deposited as blanket layers (see FIG. 26), in accordance with some embodiments. The SOT layer 180 may first be deposited over the dielectric layer 174 and the bottom electrodes 170. The MTJ stack 182 may then be deposited over the SOT layer 180, and the top electrode 184 may then be deposited over the MTJ stack 182. The SOT layer 180, the MTJ stack 182, and/or the top electrode 184 may be deposited using one or more suitable deposition techniques, depending on the material being deposited. The deposition techniques may include techniques such as CVD, PVD, ALD, sputtering, plating, the like, or a combination thereof.

[0052] Referring to FIG. 26, the layers deposited to form the SOT layer 180, the MTJ stack 182, and the top electrode 184 of a SOT-MRAM stack 185 are shown, in accordance with some embodiments. The layers of the SOT-MRAM stack 185 described in FIG. 26 are a representative example, and SOT-MRAM stacks, SOT layers, MTJ stacks, or top electrodes having other layers, materials, arrangements, compositions, or dimensions are considered within the scope of the present disclosure.

[0053] In some embodiments, the SOT layer 180 is first deposited and makes electrical contact with the bottom electrodes 170. Within a cell 101 in the memory device of the semiconductor device 100, the SOT layer 180 acts as a generator of a spin polarized current. By conducting a current through the SOT layer 180 of the cell 101, spin polarized currents are generated in transverse directions, and these spin polarized currents are used to control the magnetic moment of the overlying free layer 182A of the MTJ stack 182. By forming the SOT layer 180 below the MTJ stack 182 instead of above the MTJ stack 182, the number of process steps may be reduced. For example, additional process steps to form a via adjacent the MTJ stack 182 that connects to the SOT layer 180 are avoided.

[0054] In some embodiments, the SOT layer 180 is formed of heavy metal or a metal alloy, such as W, Ta, Pt, AuPt,  $\text{W}_3\text{Ta}$ ,  $\text{Bi}_x\text{Se}_y$ , BiSeTe, multi-layers thereof, alloys thereof, the like, or combinations thereof. The thickness of the SOT layer 180 may be between about 1 nm and about 20 nm, such as about 5 nm. In some cases, the thickness of the SOT layer

**180** may be optimized for the composition or other characteristics of the SOT layer **180**. For example, the use of a thicker SOT layer **180** can increase the spin polarized current that is generated, but spin diffusion can also reduce the efficiency of thicker SOT layers **180**. The amount of spin diffusion in an SOT layer **180** can depend on the spin diffusion length of the material of the SOT layer **180**. In this manner, a thickness of the SOT layer **180** can be chosen to maximize the performance of the cell **101** for a given application and a given material used for the SOT layer **180**.

[0055] The MTJ stack **182** is then formed over the SOT layer **180**, which includes a free layer **182A**, a barrier layer **182B**, a reference layer **182C**, a spacer layer **182D**, and a Synthetic Anti-Ferromagnetic (SAF) layer **182E** in some embodiments. The free layer **182A** of the MTJ stack **182** may be deposited over the SOT layer **180**. Within the MTJ stack **182** of a cell **101**, the free layer **182A** acts as a state-keeping layer, and its magnetic state determines the state of the cell **101**. For example, the magnetic moment of the free layer **182A** is controllable (e.g., by controlling a current flowing in the SOT layer **180**), and by controlling the magnetic moment of the free layer **182A** in this manner, the resistance of the cell **101** may be put in a high-resistance state or a low-resistance state. Whether the cell **101** is in a high-resistance state or a low-resistance state depends on the relative orientations of the spin polarizations of the free layer **182A** and the reference layer **182C**. The free layer **182A** may be formed of one or more ferromagnetic materials, such as one or more layers of CoFe, NiFe, CoFeB, CoFeBW, Ru, alloys thereof, the like, or combinations thereof. The free layer **182A** may include multiple layers of different materials, such as a layer of Ru between two layers of CoFeB, though other configurations of layers or materials may be used. In some embodiments, the material of the free layer **182A** includes a crystalline material deposited to have a particular crystalline orientation, such as a (100) orientation. The thickness of the free layer **182A** may be between about 0.4 nm and about 4 nm. In some embodiments, a free layer **182A** having an in-plane magnetic anisotropy (IMA) may have a thickness between about 1.3 nm and about 4 nm, or a free layer **182A** having a perpendicular-to-plane magnetic anisotropy (PMA) may have a thickness between about 0.4 nm and about 1.3 nm. A suitable thickness of the free layer **182A** may be determined by the composition of the free layer **182A** or the magnetic properties of the free layer **182A**.

[0056] The barrier layer **182B** may be deposited over the free layer **182A**. In some embodiments, the barrier layer **182B** is formed of one or more materials such as MgO, AlO, AlN, the like, or combinations thereof. In some embodiments, the material of the barrier layer **182B** includes a crystalline material deposited to have a particular crystalline orientation, such as a (100) orientation. The material of the barrier layer **182B** may be deposited to have the same crystalline orientation as the free layer **182A**. In some embodiments, the barrier layer **182B** may have a thickness between about 0.6 nm and about 3 nm, such as about 1 nm. In some cases, controlling the thickness of the barrier layer **182B** may control the resistance ( $R_{MTJ}$ ) of the MTJ stack **182**. For example, a thicker barrier layer **182B** may increase the resistance of the MTJ stack **182**. In some embodiments, the performance of a cell **101** can be improved by controlling the resistance  $R_{MTJ}$  of the MTJ stack **182** to match the parasitic resistance of the circuit(s) connected to the cell

**101**. In some cases, matching the resistances in this manner can increase the ranges of operating conditions over which the cell **101** can be read. The barrier layer **182B** may be thin enough such that electrons are able to tunnel through the barrier layer **182B**.

[0057] The reference layer **182C** may be deposited over the barrier layer **182B**. The reference layer **182C** may be formed of a ferromagnetic material, such as one or more layers of CoFe, NiFe, CoFeB, CoFeBW, alloys thereof, the like, or combinations thereof. In some embodiments, the material of the reference layer **182C** includes a crystalline material deposited to have a particular crystalline orientation, such as a (100) orientation. The material of the reference layer **182C** may be deposited to have the same crystalline orientation as the barrier layer **182B**. The thickness of the reference layer **182C** may be between about 1 nm and about 1.3 nm, in some embodiments. In some cases, controlling the thickness of the reference layer **182C** may control the resistance ( $R_{MTJ}$ ) of the MTJ stack **182**. For example, a thicker reference layer **182C** may increase the resistance of the MTJ stack **182**. The thickness of the reference layer **182C** may be controlled in this manner to match the resistance  $R_{MTJ}$  of the MTJ stack **182** to the parasitic resistance of the associated circuit, as described previously.

[0058] The spacer layer **182D** may be deposited over the reference layer **182C**. In some embodiments, the spacer layer **182D** is formed of a material such as W, Mo, the like, or combinations thereof. In some embodiments, the spacer layer **182D** may have a thickness between about 2 Å and about 1 nm. In some embodiments, a thicker spacer layer **182D** may be used to reduce the effects of crystalline lattice mismatch on the reference layer **182C** or free layer **182A** from overlying layers. The spacer layer **182D** may be thin enough such that electrons are able to tunnel through the spacer layer **182D**.

[0059] The Synthetic Anti-Ferromagnetic (SAF) layer **182E** may be formed over the spacer layer **182D**. The SAF layer **182E** is used to pin the spin polarization direction of the reference layer **182C** in a fixed direction. Pinning the spin polarization direction of the reference layer **182C** allows the cell **101** to be toggled between a low-resistance state and a high-resistance state by changing the spin polarization direction of the free layer **182A** relative to the reference layer **182C**.

[0060] The SAF layer **182E** may include multiple layers of different materials, in some embodiments. For example, the SAF layer **182E** may comprise a stack of one or more ferromagnetic layers and one or more non-magnetic layers. For example, the SAF layer **182E** may be formed from a non-magnetic layer sandwiched between two ferromagnetic layers or a stack of alternating non-magnetic layers and ferromagnetic layers. The ferromagnetic layers may be formed of a material such as Co, Fe, Ni, CoFe, NiFe, CoFeB, CoFeBW, alloys thereof, the like, or combinations thereof. The non-magnetic layers may be formed of a material such as Cu, Ru, Ir, Pt, W, Ta, Mg, the like, or combinations thereof. In some embodiments, the ferromagnetic layer(s) of the SAF layer **182E** may have a thickness between about 1 nm and about 3 nm. In some embodiments, a thicker SAF layer **182E** may have stronger antiferromagnetic properties, or may be more robust against external magnetic fields or thermal fluctuation. In some embodiments, the non-magnetic layer(s) of the SAF layer **182E** may have a thickness

between about 2 Å and about 1 nm. For example, the SAF layer **182E** may include a layer of Ru that has a thickness of about 0.4 nm or about 0.85 nm, though other layers or thicknesses are possible. In some embodiments, one or more layers of the SAF layer **182E** includes a crystalline material deposited to have a particular crystalline orientation, such as a (111) orientation.

[0061] The top electrode **184** may include one or more layers deposited over the MTJ stack **182** to protect the MTJ stack **182** and provide electrical connection to the top of the MTJ stack **182**. For example, the top electrode **184** may include one or more layers deposited over the SAF layer **182E** of the MTJ stack **182**, as shown in FIG. 26. The top electrode **184** may include one or more layers of materials such as Cu, Al, Ti, Ta, W, Pt, Ni, Cr, Ru, Co, Zr, titanium nitride (TiN), tantalum nitride (TaN), the like, combinations thereof, or multiple layers thereof. For example, the top electrode **184** may include a Ru layer **184A** and a Ta layer **184B** formed over the Ru layer. In some embodiments, the top electrode **184** may have a thickness between about 1 nm and about 5 nm, such as about 4 nm. For example, the top electrode **184** may include a Ru layer having a thickness of about 2 nm and a Ta layer having a thickness of about 2 nm that is formed over the Ru layer. In other embodiments, the top electrode **184** may include different layers and/or layers of different thicknesses than this example. In some cases, the top electrode **184** may be considered a “capping layer,” or one or more layers within the top electrode **184** may be considered “capping layers.”

[0062] In some embodiments after SOT layer **180**, the MTJ stack **182** and the top electrode **184** are deposited, a first patterning process is performed to pattern the SOT layer **180**, the MTJ stack **182**, and the top electrode **184** to a first shape. The first patterning process may include a suitable photolithography and etching process. In some embodiments, the pattern etched in the SOT layer **180** by the first patterning process defines the shape, size, or lateral dimensions of the SOT layer **180** of each cell **101**. For example, each cell **101** may include a SOT layer **180** having a length between about 50 nm and about 500 nm and a width between about 10 nm and about 100 nm. In some embodiments, the SOT layer **180** may have an area between about 500 nm<sup>2</sup> and about 50000 nm<sup>2</sup>.

[0063] Afterwards, a second patterning process is performed to pattern the MTJ stack **182** and the top electrode **184**, forming the SOT-MRAM stack **185**. The second patterning process may include a suitable photolithography and etching process. In some embodiments, the SOT layer **180** is used as an etch stop layer. In this manner, the second patterning process reshapes the MTJ stack **182** and the top electrode **184** to have the desired shape and size over the SOT layer **180**. As shown in FIG. 19, the second patterning process etches the MTJ stack **182** and the top electrode **184** such that the MTJ stack **182** and the top electrode **184** have a smaller lateral area than the SOT layer **180**. The resulting shape of the MTJ stack **182** and top electrode **184** may have an approximately circular shape, or may have an oblong shape, such an elliptical shape, rounded rectangle shape, or the like.

[0064] Turning to FIG. 20, after the SOT-MRAM stack **185** is formed, vias **188** and conductive lines **190** are formed in the dielectric layer **186** and the dielectric layer **168** in the routing regions **100R** and/or **100R'** to make electrical connection with the conductive lines **166** and make the vertical

routing in the routing regions **100R** and/or **100R'**. In some embodiments, the vias **188** and the conductive lines **190** are formed by a dual damascene process. The conductive lines and the vias **188** may be formed of a material similar to those described above for conductive lines **162**.

[0065] In FIG. 21, vias **192** and conductive lines **194** are formed in a dielectric layer **196** to make electrical connection to the top electrodes **184** in the cell region **100M** and make electrical connection to the conductive lines **190** in the routing regions **100R** and/or **100R'**, in accordance with some embodiments. In some embodiments, the dielectric layer **196** may have one or more layers. The dielectric layer **196** may be formed of a material similar to those described above for the dielectric layer **160** and may be formed using similar techniques. The vias **192** and the conductive lines **196** may be formed of a material similar to those described above for the vias **164** and the conductive lines **166** and may be formed using similar techniques. In some embodiments, some of the conductive lines **194** in the cell regions **100M** are used as a Read Bit Lines (“RBL”) for each cell **101** of the memory device of the semiconductor device **100**.

[0066] One or more sets of additional vias and conductive lines (not shown in Figures) may be formed over the conductive lines **194** and the dielectric layers **196** in accordance with some embodiments. The additional sets of vias and conductive lines may be formed in a similar manner as the vias **164** and conductive lines **166**. In some embodiments, bonding pads and bumps (not shown in Figures) are also formed over the additional sets of vias and conductive lines to complete the BEOL portion **100B**.

[0067] Turning to FIG. 22, through substrate vias **198** are formed in the substrate **102** and physically and electrically connect to the buried contacts **112B**. In some embodiments, the through substrate vias **198** physically and electrically connect to the buried contacts **112A** underlying the gate electrode **150** (e.g., referring to FIG. 25). The vias (sometimes referred to as through silicon vias or through substrate vias) **198** may be formed by a drilling process, such as a laser drilling process or a mechanical drilling process, from the second side **102B** of the substrate **102**. The drilling process forms through holes that expose the buried contacts **112A** and **112B**. A conductive material is then filled into through holes. Excess conductive material over the second side **102B** of the substrate **102** is removed by a planarizing process such as CMP or a grinding process. Because the buried contacts **112A** and **112B** have a bottom lower than the bottom of the protrusions **104** and first side **102A** of the substrate **102**, the tolerance of forming the thorough substrate vias **198** is increased, which may prevent features formed over the first side **102A** of the substrate **102** from being harmed during the formation of the through substrate vias **198**. In some embodiments, the through substrate vias **198** may be formed of a material similar to those described above for the vias **164**. In some embodiments, the buried contacts **112A** and **112B** have a portion protruding into the through substrate vias **198**.

[0068] Turning to FIG. 23, one or more level of backside conductive lines is formed. For example, as illustrated in FIG. 23, two levels of conductive lines **202** and **216** are formed. Conductive lines **202** are formed in a dielectric layer **200**. Vias **214** and conductive lines **216** are formed in a dielectric layer **210**. In some embodiments, at least some of the conductive lines **202** and/or at least some of the conductive lines **216** are electrically connected to the buried

contacts 112B by the through substrate vias 198. By making electrical connection to the buried contacts 112B and source features 130S of transistors 130, at least a portion of the conductive lines 200 and/or a least a portion of the conductive lines 216 act as source lines configured to operate the SOT-MRAM stack 185, in accordance with some embodiments. Referring to FIG. 25, at least some of the conductive lines 202 and/or at least some of the conductive lines 216 are electrically connected to the buried contacts 112A underlying the gate structure 150 by the through substrate vias 198. By making electrical connection to the buried contacts 112A and gate structure 150 of transistors 130, at least a portion of the conductive lines 202 and/or a least a portion of the conductive lines 216 act as word lines configured to operate the SOT-MRAM stack 185, in accordance with some embodiments. In some embodiments, at least a portion of the backside conductive lines 202 act as the source lines configured to operate the SOT-MRAM stack 185, and at least a portion of the backside conductive lines 216 act as the word lines configured to operate the SOT-MRAM stack 185, or vice versa. Although FIG. 23 only shows (portions of) the cell region 100M and routing regions 100R', a person skilled in the art would know that the backside conductive lines 202 and 216 are not limited to be disposed in the regions described above. For example, the backside BEOL 100BB may occupy similar areas as FEOL portion 100F and the BEOL portion 100B. In some embodiments, the backside conductive lines 202 and 216 may be disposed in or across to other regions, such as logic regions or other routing regions such as the routing region 100R.

[0069] In some embodiment, the arrangement of the source features and the drain features are not limited to the arrangement of the source/drain features as illustrated in the cell region 100M. The buried contacts 112B are not limited to connect to the source features 130S of transistors 130 in accordance with some embodiments. For example, the buried contacts 112B may be formed adjacent to source features, drain features, or a combination thereof in routing regions 100R, 100R' or other regions of the semiconductor device 100. In other words, in alternative embodiments, buried contacts 112B may be used to make electrical connections to drain features 130D, and contact plugs 154 may be used to make electrical connections to source features 130S. In still other embodiments, buried contacts may be employed to connect to both source features 130S and drain features 130D, and contact plugs may be employed to electrically connect to other source features 130S and drain features 130D.

[0070] Turning to FIG. 24, a passivation layer is formed over the dielectric layer 210 and the conductive lines 216 to protect the backside conductive lines from being damaged by moisture. The passivation layer 220 may include silicon nitride, silicon oxynitride, aluminum oxide, aluminum nitride, or a combination thereof. The passivation 220 may be formed by CVD, PVD, or by spin on.

[0071] FIGS. 27 to 29 illustrate immediate stages in the formation of the semiconductor device 200 in accordance with another embodiment of the present disclosure in cross-sectional and plan views. In FIGS. 27 and 28 (FIG. 27 corresponding to section C-C labeled in FIG. 28), a semiconductor device 200 is illustrated. The semiconductor device 200 is the same as the semiconductor device 100 except that only a portion of source lines are disposed in the backside BEOL portion 100BB, and some of the conductive

lines 162 (label as "162SL") act as source lines configured to operate the SOT-MRAM stack 185. In the semiconductor device 200, word lines configured to operate the SOT-MRAM stack 185 may be disposed in the BEOL portion 100B, the backside BEOL portion 100BB, or a combination thereof. For example, referring to FIG. 29 (corresponding to section D-D labeled in FIG. 28), some of the gate structure 150 (labeled as "150WL") acts as a part of the word lines configured to operate the SOT-MRAM stack 185 and electrically connected to the conductive lines 162 by vias 250, and the word lines (e.g., conductive lines 202 or conductive line 216) configured to operate the SOT-MRAM stack 185 are extended to conductive lines 202 and/or 216 in the backside BEOL portion 100BB by buried contacts 112A and through substrate vias 198. In FIG. 30, a semiconductor device 300 is illustrated. The semiconductor device 300 is the same as the semiconductor device 100 or 200 except the SOT-MRAM stack 385 is disposed in the backside BEOL portion 100BB. The SOT-MRAM stack 385 may be electrically connected to the source feature 130S of transistors 130 by the conductive lines 202, through substrate vias 198, buried contacts 112B, and buried contact plugs 154. The SOT-MRAM stack 385 may be electrically connected to the gate structure 150 of transistors by the conductive lines 202, through substrate vias 198, and buried contacts 112A. In some embodiments, the SOT-MRAM stack 385 is electrically connected to the drain features 130D of transistors 130 by the vertical routing in the routing regions 100R' and conductive lines 162. Alternatively, the SOT-MRAM stack 385 may be electrically connected to the drain features 130D of transistors 130 by buried contacts adjacent to the drain features and making electrical connection to the drain regions in a manner similar to the source regions.

[0072] The embodiments of the present disclosure have some advantageous features. For example, the semiconductor device 100, 200, or 300 of the present disclosure provides conductive lines (i.e., interconnection structure of BEOL) formed over both sides of the substrate, which provides more flexibility of routing designs. In some cases, when the pitch of the drain contact plugs is too small, device designers or manufacturers may have a problem to dispose the conductive lines that are used to electrically connect the underlying drain contact plugs because, at the first level of BEOL, most of the space is occupied by the conductive lines acting as source lines of the memory device. According to some embodiments of the present disclosure, by moving at least a portion of source lines would create space to dispose the conductive lines that are used to electrically connect the underlying drain plugs. For example, adjacent columns of the conductive lines (e.g., the conductive lines 162) may be partially or completely misaligned in a direction of the columns. Alternatively, adjacent columns of the conductive lines (e.g., the conductive lines 162) may partially overlap in a direction perpendicular to the direction of columns. Additionally, the backside BEOL provides extra space to integrate more embedded devices, in accordance with some embodiments of the present disclosure.

[0073] In an embodiment, a device includes a substrate having a first side and a second side; and a memory device that includes: a transistor disposed over the first side of the substrate, wherein the transistor includes a gate and a source feature and a drain feature interposing the gate; first conductive lines disposed over the transistor; a memory stack disposed over the first conductive lines; and second conduc-

tive lines disposed over the second side of the substrate, wherein at least one of the second conductive lines is a source line or a word line of the memory device.

**[0074]** In an embodiment, a device includes a substrate having a first side and a second side; a first transistor, wherein the first transistor comprises a first gate over a first protrusion and a first source region and a first drain region interposing the first protrusion; a first buried contact disposed adjacent to the first protrusion and having at least a portion extending into the substrate, wherein the first buried contact is electrically connecting to the first source region or the first gate; a first contact plug disposed over the first drain region; first conductive lines disposed over the first contact plug and electrically connecting to the first drain region by the first contact plug; a first via penetrating through the substrate and connecting to the first buried contact; and second conductive lines disposed over the second side of the substrate and electrically connecting to the first via.

**[0075]** In an embodiment, a device includes a substrate having a first side and a second side; and a memory device that includes: a transistor disposed over the first side of the substrate, wherein the transistor includes a gate and a source feature and a drain feature interposing the gate; first conductive lines disposed over the transistor; a memory stack disposed over the first conductive lines; and second conductive lines disposed over the second side of the substrate, wherein at least one of the second conductive lines is a source line or a word line of the memory device.

**[0076]** In an embodiment, a method includes: forming a protrusion over a side of a substrate; forming a buried contact adjacent to the protrusion, wherein the buried contact has a portion extending into the substrate; forming a gate wrapping over the protrusion; forming epitaxial features interposing protrusions, wherein the gate or the epitaxial features is electrically connected to the buried contact; forming first conductive lines over the gate and the epitaxial features; forming a via penetrating through the substrate and connecting to the buried contact; and forming second conductive lines over another side of the substrate, wherein the second conductive lines are electrically connected to the via.

**[0077]** Some embodiments described herein provide for a device including a substrate having a first side and a second side. The device also includes a first transistor disposed on the first side, where the first transistor may include a first gate over a first protrusion, and a first source feature and a first drain feature on respective sides of the first gate. The device also includes a first buried contact disposed adjacent to the first protrusion and having at least a portion extending into the substrate, where the first buried contact is electrically connected to the first source feature or the first gate. The device yet further includes a first contact plug disposed over the first drain feature. The device also includes first conductive lines disposed over the first contact plug and electrically connecting to the first drain feature by the first contact plug a first via penetrating through the substrate and connecting the first buried contact. The device also includes second conductive lines disposed over the second side of the substrate and electrically connecting to the first via.

**[0078]** Other embodiments described herein provide for a device including a protrusion over a front side of a substrate. The device also includes a buried contact adjacent to the protrusion, a portion of the buried contact extending into the substrate. The device also includes a gate wrapping over the protrusion, and further includes an epitaxial feature in a

region of the protrusion, where the gate or the epitaxial feature is electrically connected to the buried contact. The device also includes conductive lines over the gate and the epitaxial features, and a via penetrating through the substrate and connecting to the buried contact. The device yet further includes second conductive lines over a back side of the substrate, where the second conductive lines are electrically connected to the via.

**[0079]** Still other embodiments described herein provide for a device having a substrate having a first side and a second side, with a first transistor disposed on the first side, the first transistor including a first source feature and a first drain feature on respective sides of a first gate. The device also includes a first buried contact having at least a portion extending into the substrate, where the first buried contact is electrically connected to transistor. The device also includes a first contact plug disposed over the first drain feature. The device further includes a first conductive line disposed over the first contact plug and electrically connected to the first drain feature by the first contact plug a first via penetrating through the substrate and connected the first buried contact. The device yet further includes a second conductive line disposed over the second side of the substrate and electrically connecting to the first via.

**[0080]** The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

**[0081]** Some embodiments described herein may include a method of forming a protrusion over a first side of a substrate. The method also includes forming a buried contact adjacent to the protrusion, where the buried contact has a portion extending into the substrate. The method also includes forming a gate wrapping over the protrusion. The method also includes forming an epitaxial feature in a region of the protrusion, where the gate or the epitaxial feature is electrically connected to the buried contact. The method also includes forming first conductive lines over the gate and the epitaxial features. The method also includes forming a conductive via penetrating through the substrate and connecting to the buried contact. The method also includes forming second conductive lines over another side of the substrate, where the second conductive lines are electrically connected to the conductive via.

**[0082]** Some other embodiments described herein may include a method of forming a semiconductor device, forming a first protrusion and a second protrusion over a first side of a substrate. The method also includes forming a buried contact interjacent the first protrusion and the second protrusion, where the buried contact has a portion extending into the substrate. The method also includes epitaxially growing a first source/drain feature in the first protrusion and a second source/drain feature in the second protrusion. The method also includes forming a contact plug electrically contacting the first source/drain feature, the second source/

drain feature, and the buried contact. The method also includes forming first conductive lines over the first protrusion and the second protrusion. The method also includes forming a conductive via penetrating from a second side of the substrate, opposite the first side of the substrate, and connecting to the buried contact. The method also includes forming second conductive lines over the second side of the substrate, where at least one of the second conductive lines is electrically connected to the conductive via.

**[0083]** Some other embodiments described herein may include a method for manufacturing a semiconductor device, which includes providing a substrate with a first side and a second side. The method also includes forming a plurality of protrusions on the first side of the substrate. The method also includes etching the substrate to form buried contact holes adjacent to respective protrusions. The method also includes filling the buried contact holes with conductive material to form respective buried contacts. The method also includes forming one or more gate structures over the plurality of protrusions and the buried contacts. The method also includes creating source/drain features in respective ones of the plurality of protrusions. The method also includes forming electrical connections to the buried contacts through the formation of conductive lines above the first side of the substrate, and through conductive vias that extend from the second side to respective buried contacts.

1. A device comprising:
  - a substrate having a first side and a second side opposite the first side;
  - a protrusion extending from the first side of the substrate, the protrusion including a channel region of a transistor;
  - a gate extending over the protrusion and at least partially surrounding the channel region;
  - a source/drain region adjacent the channel region;
  - a first buried contact extending from the first side of the substrate to the second side of the substrate, the first buried contact being under and electrically contacting the gate;
  - a second buried contact extending from the first side of the substrate to the second side of the substrate, the second buried contact electrically contacting the source/drain region;
  - a first conductive line on the second side of the substrate and electrically contacting the first buried contact; and
  - a second conductive line on the second side of the substrate and electrically contacting the second buried contact.

2. The device of claim 1, wherein the protrusion comprises a fin structure.

3. The device of claim 1, wherein the channel region comprises a vertical stack of channel regions and further wherein the gate surrounds individual channel regions of the vertical stack of channel regions.

4. The device of claim 1, wherein the second buried contact further electrically contacts a second source/drain region/.

5. The device of claim 1, wherein the first buried contact comprises a first conductor extending from the first side of the substrate and a second conductor extending from the second side of the substrate, wherein the first conductor and the second conductor physically and electrically contact at an intermediate point between the first side and the second side of the substrate.

6. The device of claim 5, wherein the second conductor has a greater width in an x direction than the first conductor, when viewed from a cross-sectional perspective.

7. The device of claim 1, wherein the second buried contact passes through the source/drain region when viewed in a cross-sectional perspective.

8. The device of claim 1, further comprising a memory cell over the first side of the substrate, the memory cell being electrically connected to the transistor.

9. The device of claim 8, wherein the memory cell is a part of an array of memory cells, and further wherein the array of memory cells is located in a memory region of the substrate, and further wherein the first buried contact and the second buried contact are located in a routing region of the substrate, the routing region of the substrate being non-overlapping with the memory region of the substrate.

10. A device comprising:

- a substrate having a first side and a second side opposite the first side;
- a transistor disposed on the first side, wherein the transistor comprises a gate over a protrusion, and a source/drain feature;
- a buried contact disposed adjacent to the protrusion and extending through the substrate, wherein the buried contact is electrically connected to the source/drain feature or to the gate;
- a stack of metal interconnect layers embedded within respective dielectric layers over the transistor;
- a memory cell vertically interposed between two of the stack of metal interconnect layers; and
- a conductive line on the second side of the substrate, the conductive line being electrically coupled to the memory cell through the transistor and the buried contact.

11. The device of claim 10, wherein the transistor is a FinFET device.

12. The device of claim 10, wherein the memory cell is a magneto-resistive random access memory device.

13. The device of claim 10, wherein the buried contact includes a first conductor extending from the first side of the substrate and a second conductor extending from the second side of the substrate, and further wherein the first conductor and the second conductor physically connect at an intermediate point between the first side and the second side of the substrate.

14. The device of claim 10, wherein the conductive line is configured as a word line for the memory cell.

15. The device of claim 10, wherein the buried contact is electrically connected to the source/drain feature and is surrounded by the source/drain feature on at least two sides when viewed from a cross-sectional perspective.

16. A device comprising:

- a substrate having a front side and a back side;
- a device layer on the front side of the substrate, the device layer including:
  - a row of transistors, the row of transistors extending in an x direction,
  - a first transistor of the row of transistors having a first gate electrode extending in a y direction, a first drain region on a first side of the first gate electrode, and a first source region on an opposite side of the first gate electrode, and
  - a second transistor of the row of transistors having a second gate electrode extending in the y direction, a

second source region on a first side of the second gate electrode, and a second drain region on an opposite side of the second gate electrode

a first drain contacting extending above and physically contacting the first drain region, the first drain contact extending a first distance in the y direction when viewed from a top down perspective,

a second drain contacting extending above and physically contacting the second drain region, the second drain contact extending a second distance greater than the first distance in the y direction when viewed from the top down perspective,

a first source contact extending above and physically contacting the first source region,

a first buried contact below and electrically and physically contacting the first gate electrode, the first buried contact extending to the back side of the substrate, and

a second buried contact below and physically contacting the first source region, the second buried contact extending to the back side of the substrate;

an interconnect layer above the device layer, the interconnect layer including a first conductive line physically and electrically contacting the first source contact

and a second conductive line physically and electrically contacting the first drain contact; and

a back side layer on the back side of the substrate, the back side layer including a first back side conductive line electrically contacting the first buried contact, and a second back side conductive line electrically contacting the second buried contact.

**17.** The device of claim **16**, wherein the first source region and the second source region are a common source region.

**18.** The device of claim **16**, wherein the first buried contact comprises a first conductor extending from the front side of the substrate and a second conductor extending from the back side of the substrate, wherein the first conductor and the second conductor physically and electrically contact at an intermediate point between the front side and the back side of the substrate.

**19.** The device of claim **16**, wherein the transistors of the row of transistors are formed in a common fin structure, the common fin structure extending in the x direction.

**20.** The device of claim **16**, wherein the interconnect layer includes a stack of metal layers, the stack extending in a z direction, and a memory cell interjacent two metal layers of the stack of metal layers.

\* \* \* \* \*