US012394763B2

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Choi et al.

(10) **Patent No.: US 12,394,763 B2**
(45) **Date of Patent: Aug. 19, 2025**

(54) **DISPLAY DEVICE AND METHOD OF FABRICATING THE SAME**

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(73) Assignee: **Samsung Display Co., Ltd.**, Yongin-si (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 521 days.

(21) Appl. No.: **17/815,170**

(22) Filed: **Jul. 26, 2022**

(65) **Prior Publication Data**

US 2023/0044786 A1 Feb. 9, 2023

(30) **Foreign Application Priority Data**

Aug. 9, 2021 (KR) 10-2021-0104920

(51) **Int. Cl.**

H01L 25/075	(2006.01)
H10H 20/01	(2025.01)
H10H 20/812	(2025.01)
H10H 20/816	(2025.01)
H10H 20/831	(2025.01)
H10H 20/857	(2025.01)
H10H 29/14	(2025.01)

(52) **U.S. Cl.**

CPC ***H01L 25/0753*** (2013.01); ***H10H 20/01*** (2025.01); ***H10H 20/812*** (2025.01); ***H10H 20/8162*** (2025.01); ***H10H 20/8312*** (2025.01); ***H10H 20/857*** (2025.01); *H10H 20/032* (2025.01); *H10H 20/0364* (2025.01)

(58) **Field of Classification Search**

CPC H01L 25/0753; H01L 25/0756; H10H 20/8312; H10H 20/018; H10H 29/142; H10H 29/14

See application file for complete search history.

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* cited by examiner

Primary Examiner — Mohsen Ahmadi

(74) *Attorney, Agent, or Firm* — Womble Bond Dickinson (US) LLP

(57) **ABSTRACT**

A display device includes light-emitting elements arranged on a circuit board, and extending in a thickness direction of the circuit board, wherein the light-emitting elements include a first light-emitting element configured to emit a first light, and a second light-emitting element configured to emit a second light, wherein the first light-emitting element and the second light-emitting element are on different layers, and wherein a width of the first light-emitting element is greater than a width of the second light-emitting element.

15 Claims, 34 Drawing Sheets

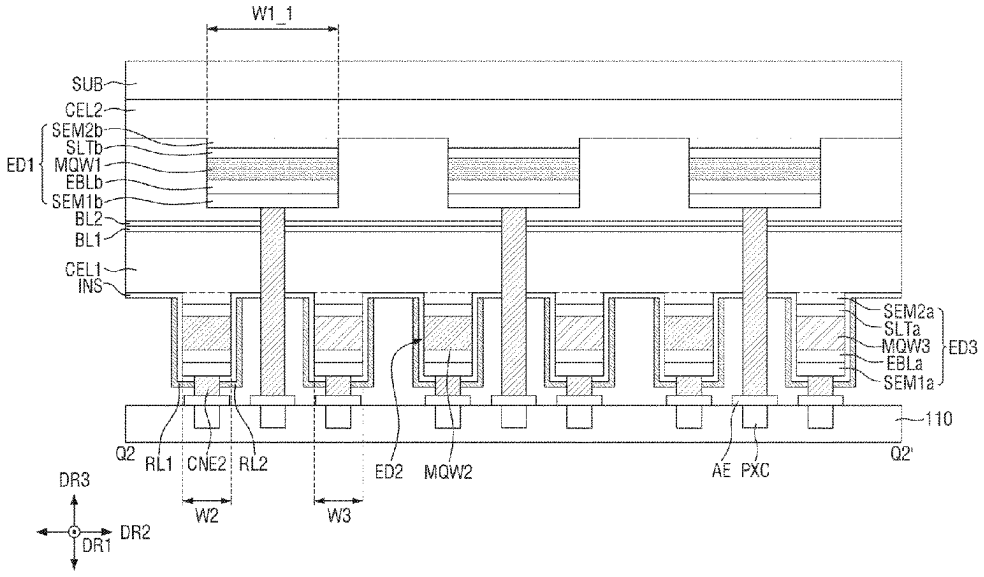


FIG. 1

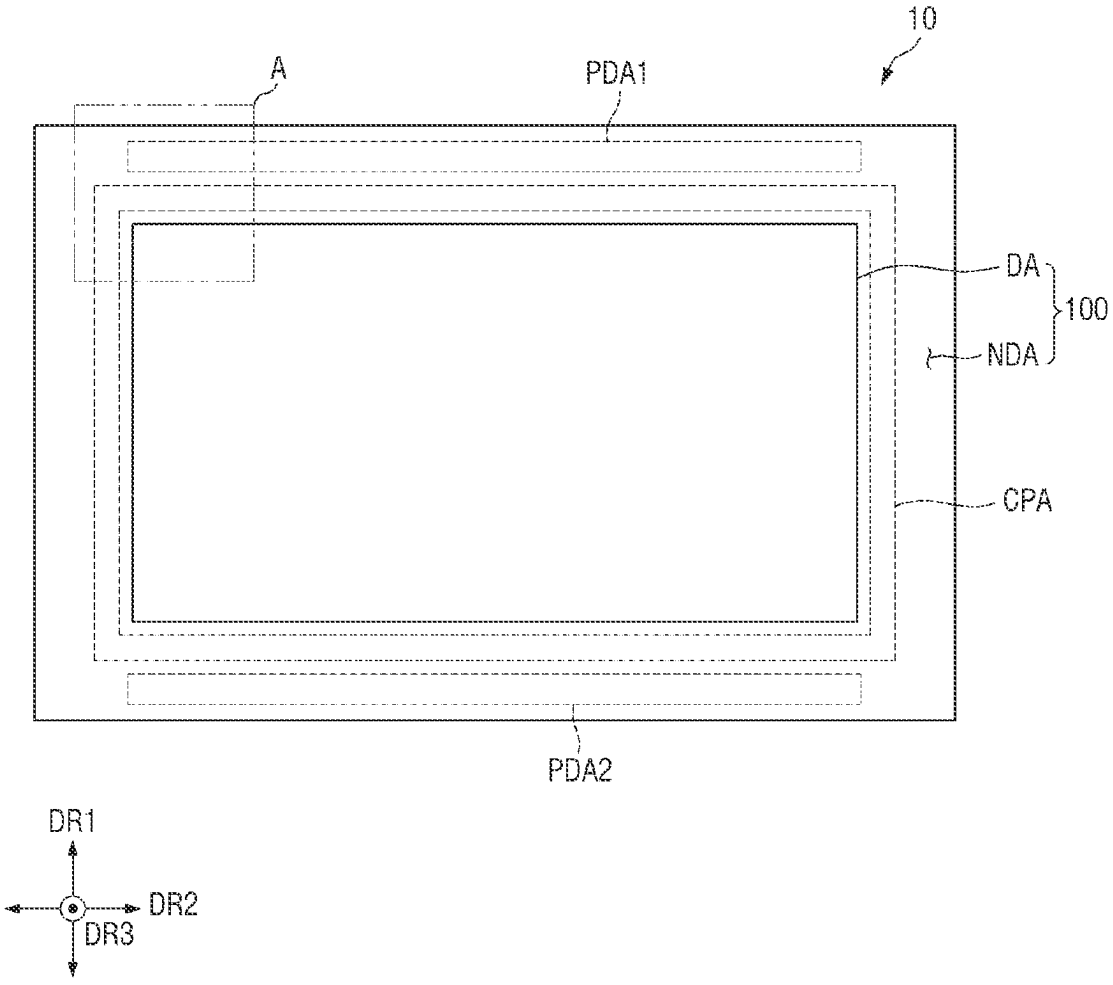


FIG. 2

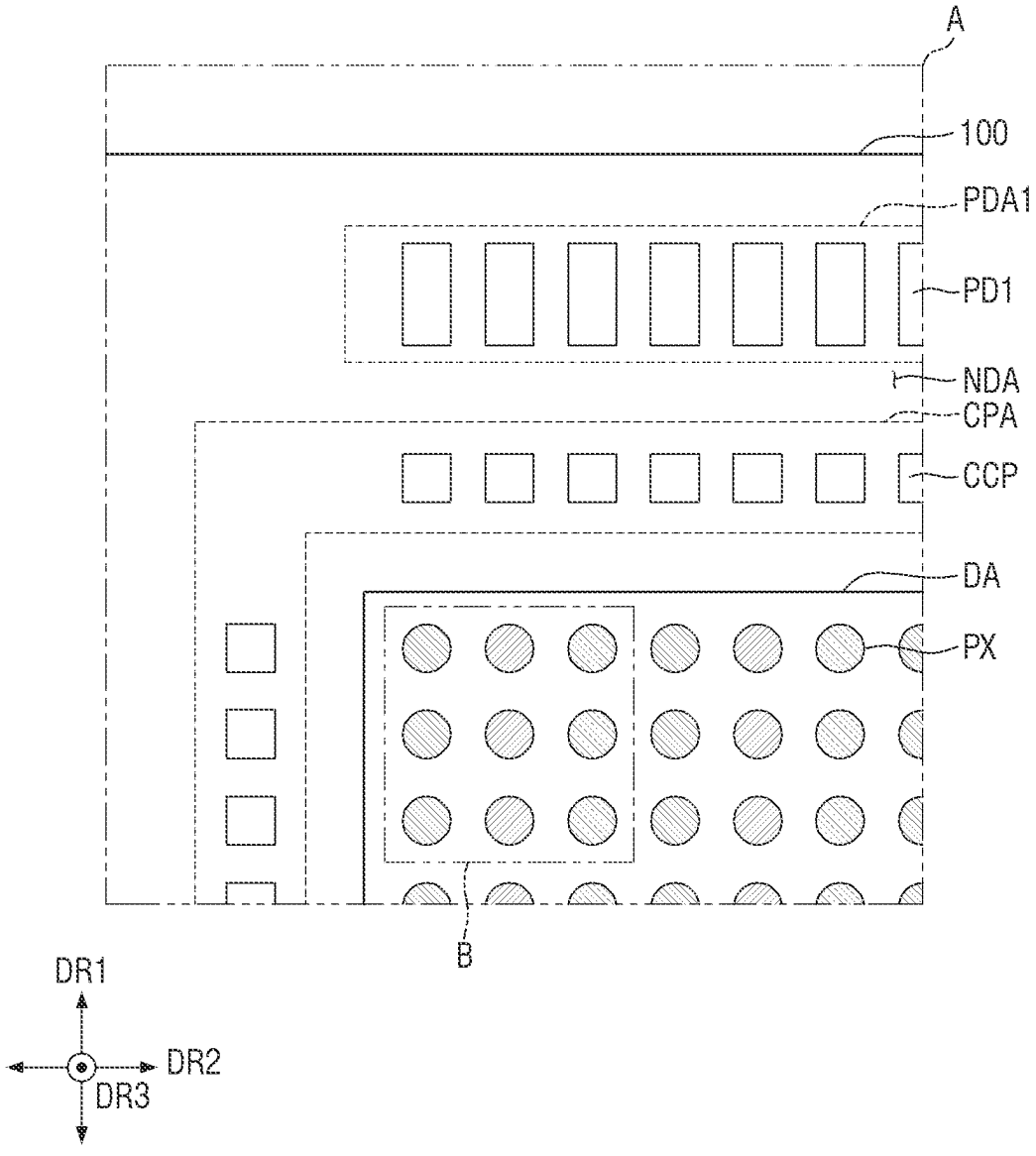


FIG. 3

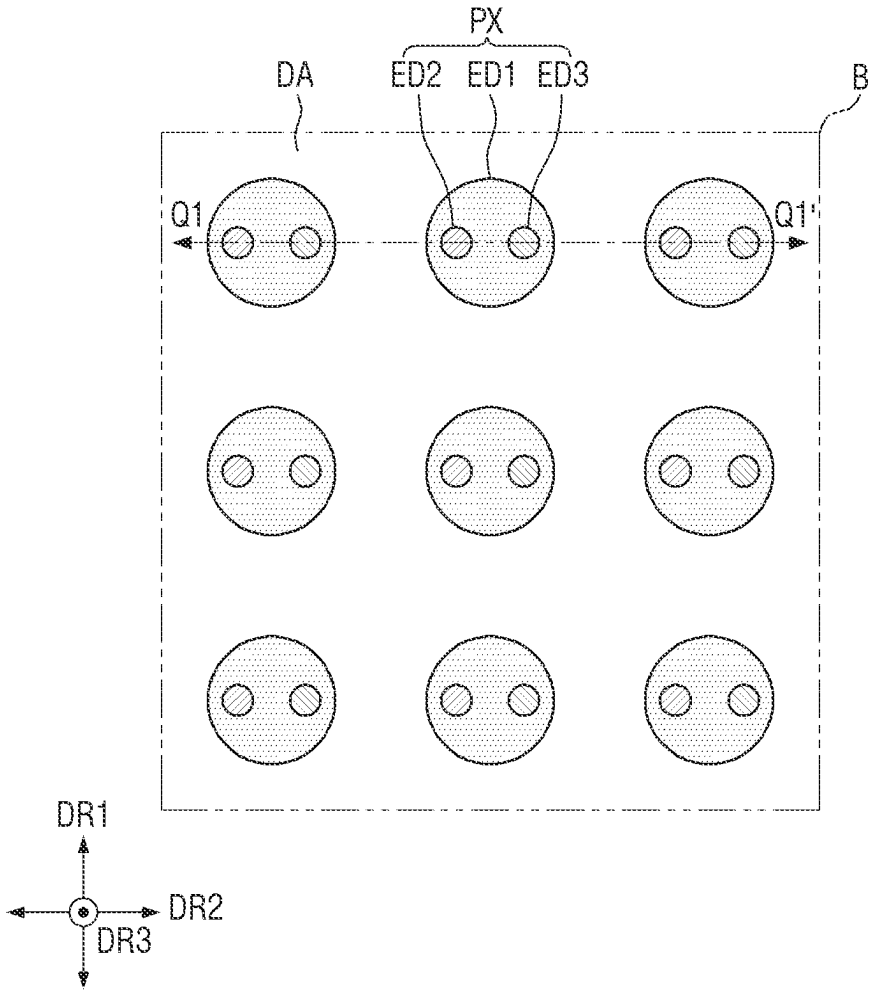


FIG. 4

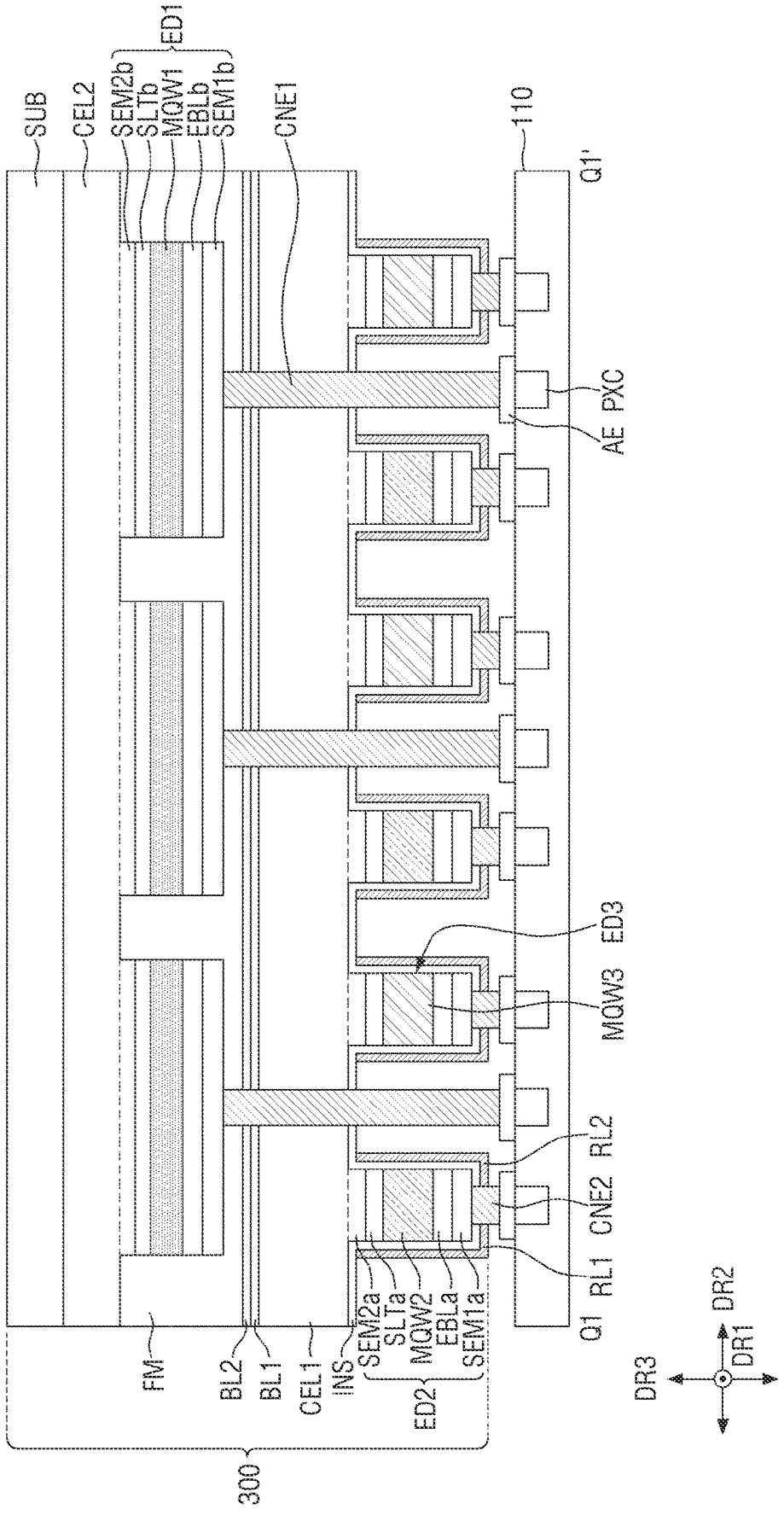

SUB
CEL2
SEM2b
SLTb
MQW1
EBLb
SEM1b
ED1
CNE1
110
Q1'
PXC
AE
ED3
MQW3
RL2
CNE2
RL1
Q1
SEM2a
SLTa
MQW2
EBLa
SEM1a
ED2
INS
CEL1
BL1
BL2
FM
300
DR1
DR2
DR3

FIG. 5

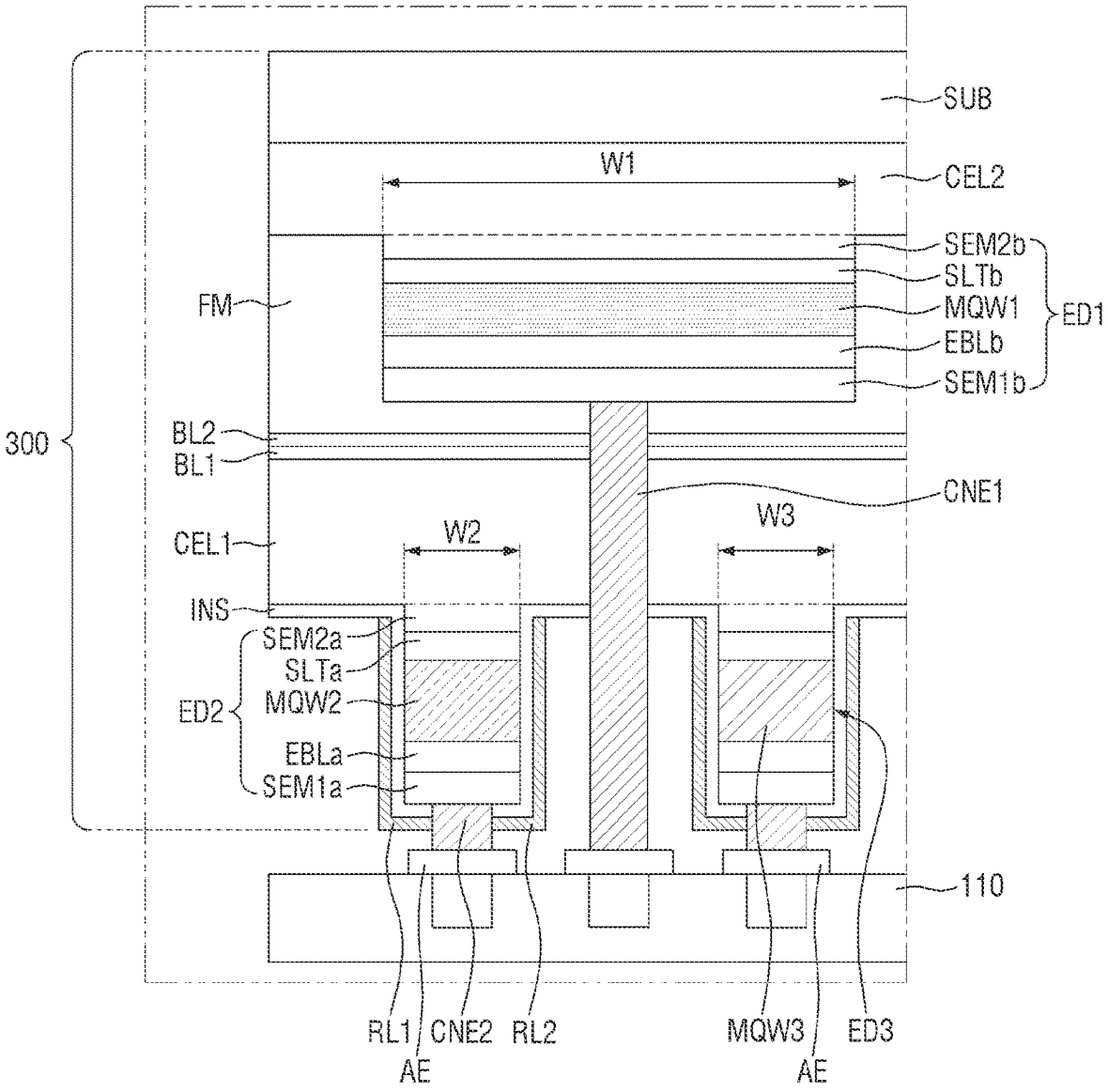

SUB
W1
CEL2
SEM2b
SLTb
MQW1
EBLb
SEM1b
ED1
FM
300
BL2
BL1
CNE1
W2
W3
CEL1
INS
SEM2a
SLTa
MQW2
EBLa
SEM1a
ED2
110
RL1
AE
CNE2
RL2
MQW3
AE
ED3

FIG. 6

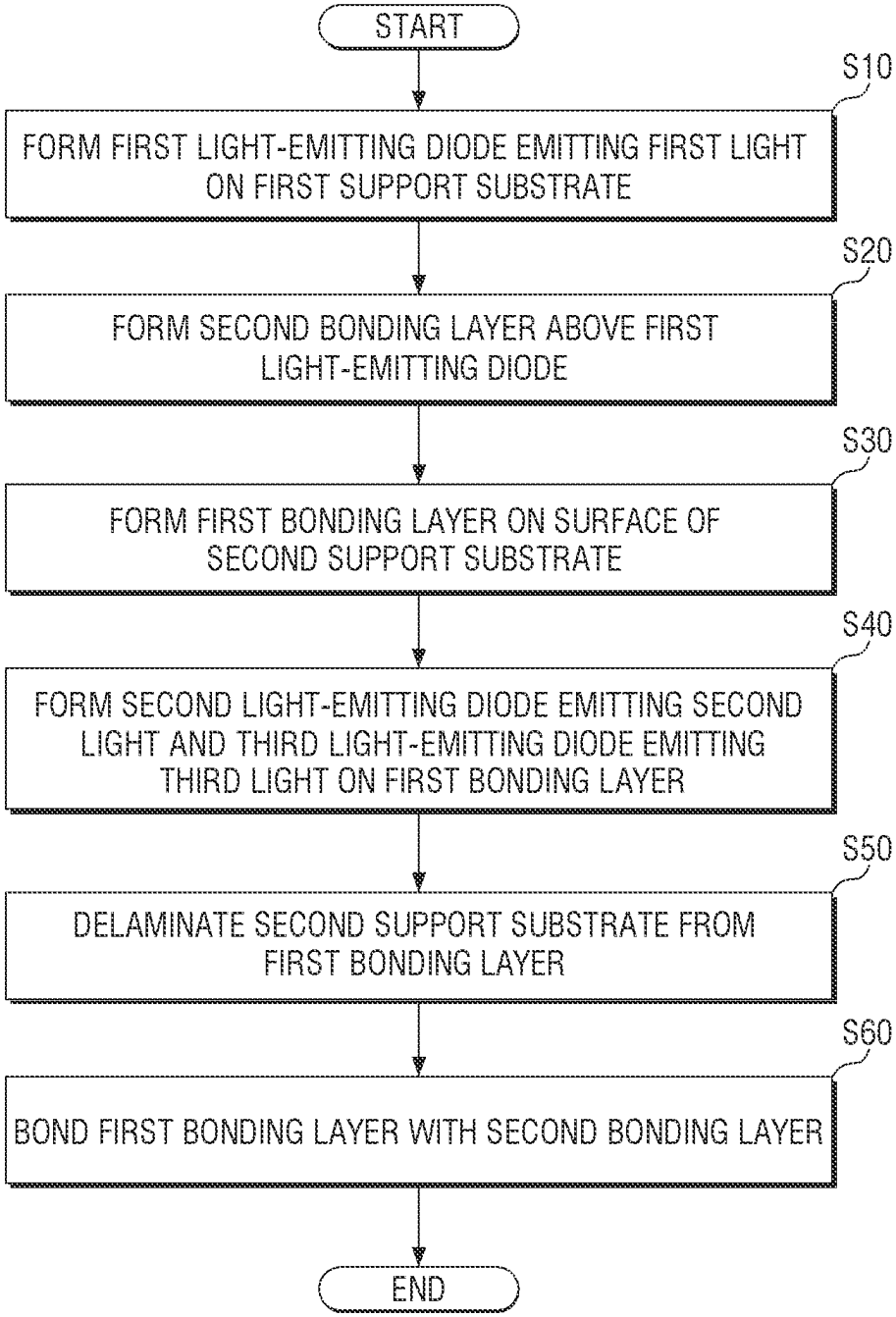

START
S10
FORM FIRST LIGHT-EMITTING DIODE EMITTING FIRST LIGHT ON FIRST SUPPORT SUBSTRATE
S20
FORM SECOND BONDING LAYER ABOVE FIRST LIGHT-EMITTING DIODE
S30
FORM FIRST BONDING LAYER ON SURFACE OF SECOND SUPPORT SUBSTRATE
S40
FORM SECOND LIGHT-EMITTING DIODE EMITTING SECOND LIGHT AND THIRD LIGHT-EMITTING DIODE EMITTING THIRD LIGHT ON FIRST BONDING LAYER
S50
DELAMINATE SECOND SUPPORT SUBSTRATE FROM FIRST BONDING LAYER
S60
BOND FIRST BONDING LAYER WITH SECOND BONDING LAYER
END

FIG. 7

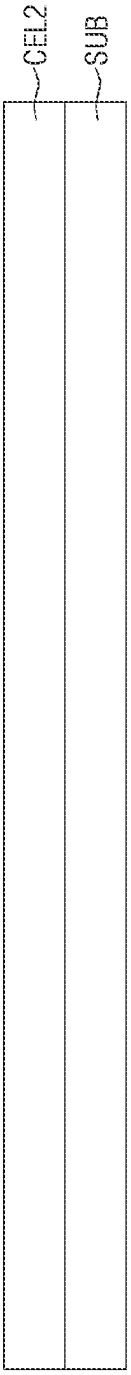


FIG. 8

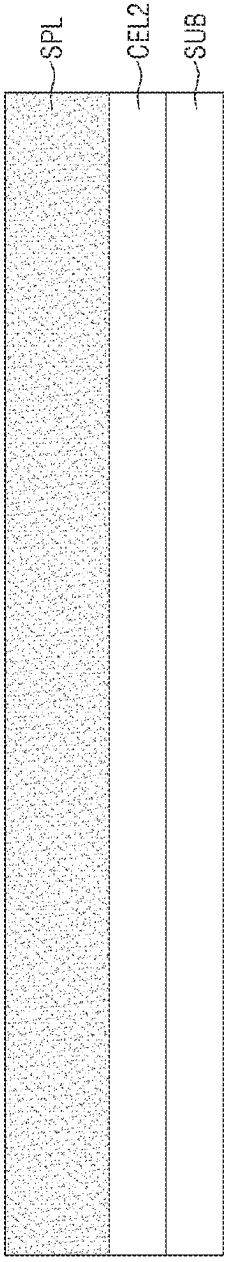


FIG. 9

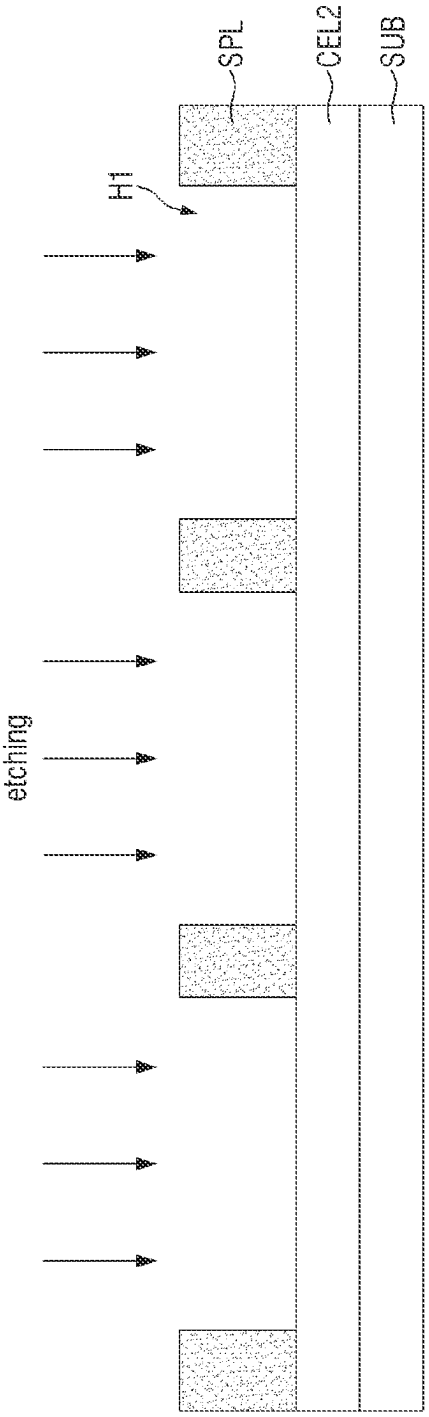


FIG. 10

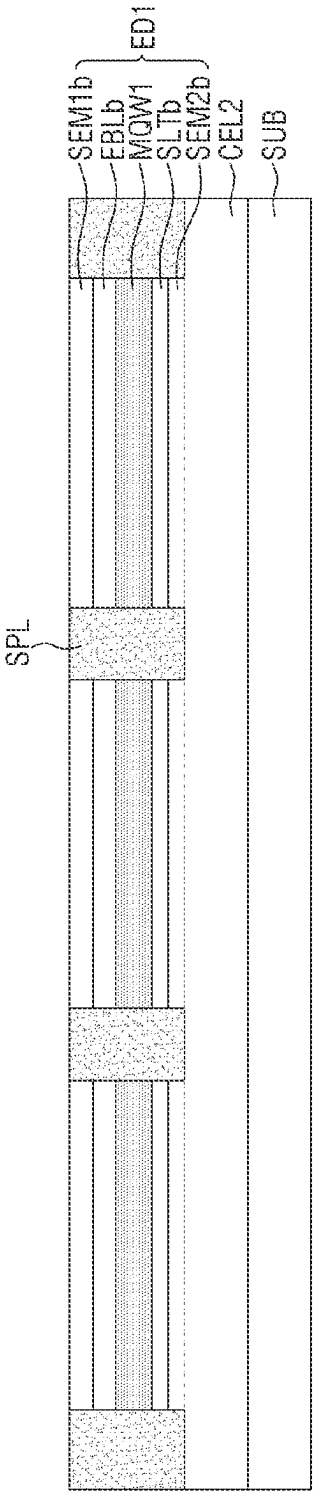


FIG. 11

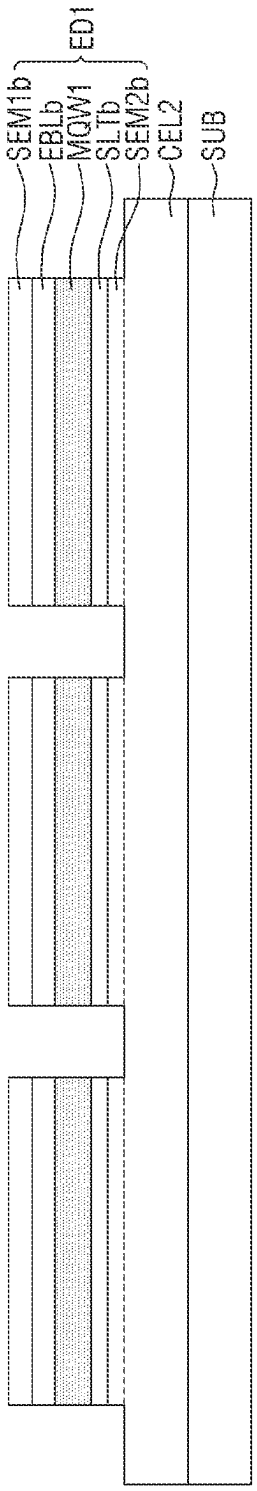


FIG. 12

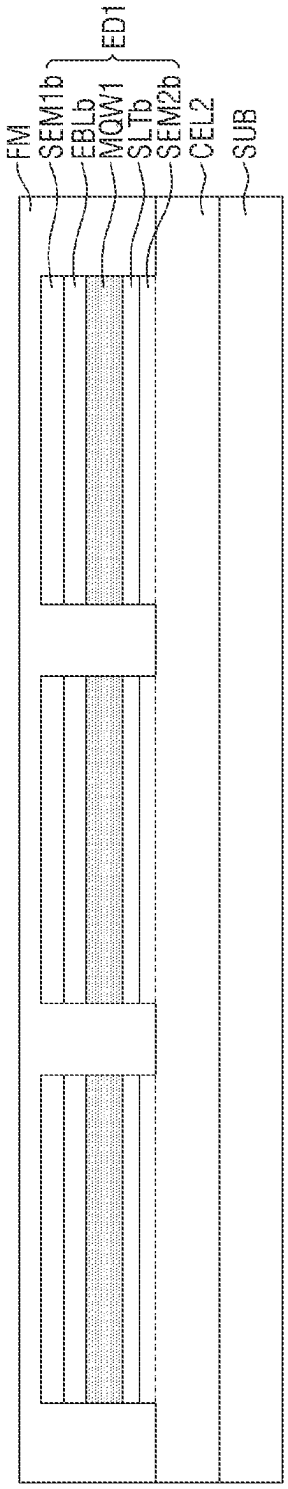


FIG. 13

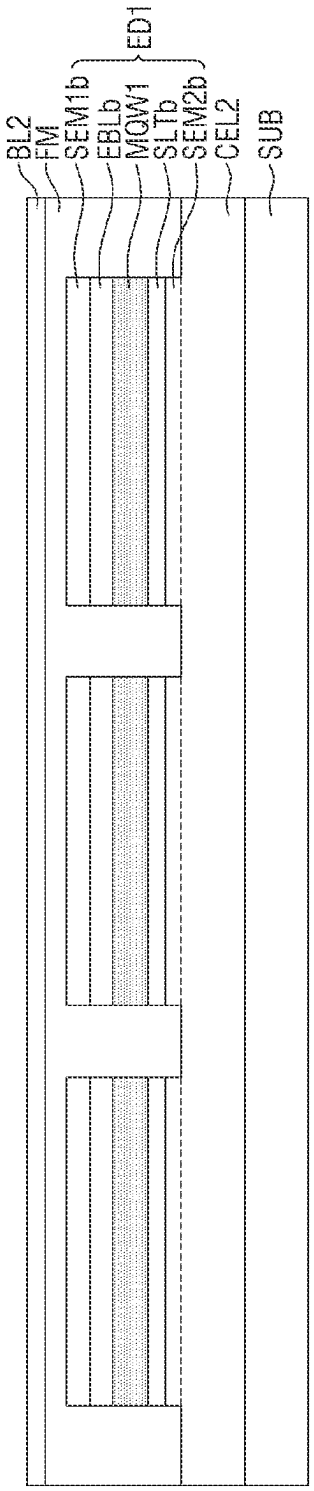


FIG. 14

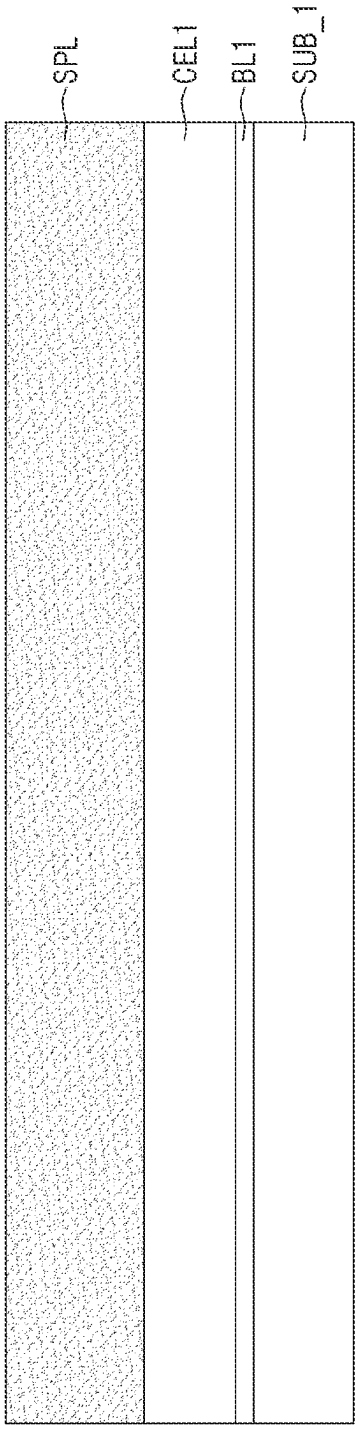


FIG. 15

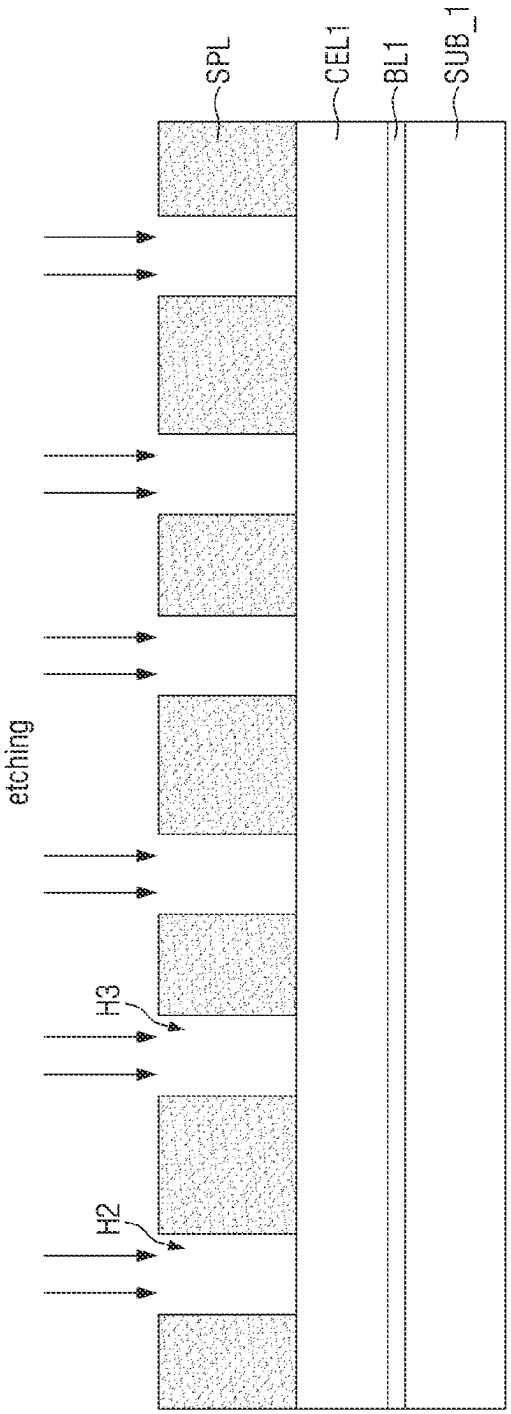


FIG. 16

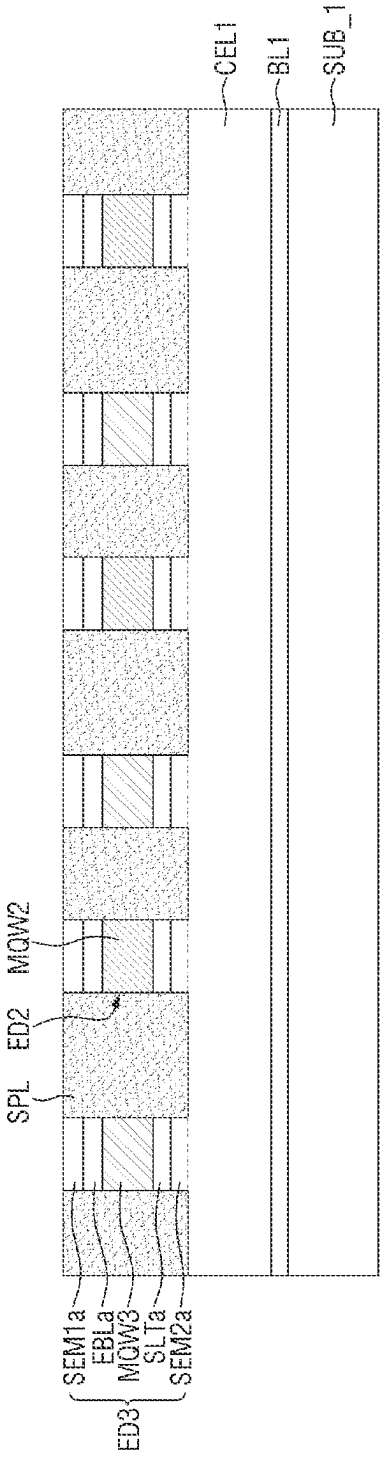


FIG. 17

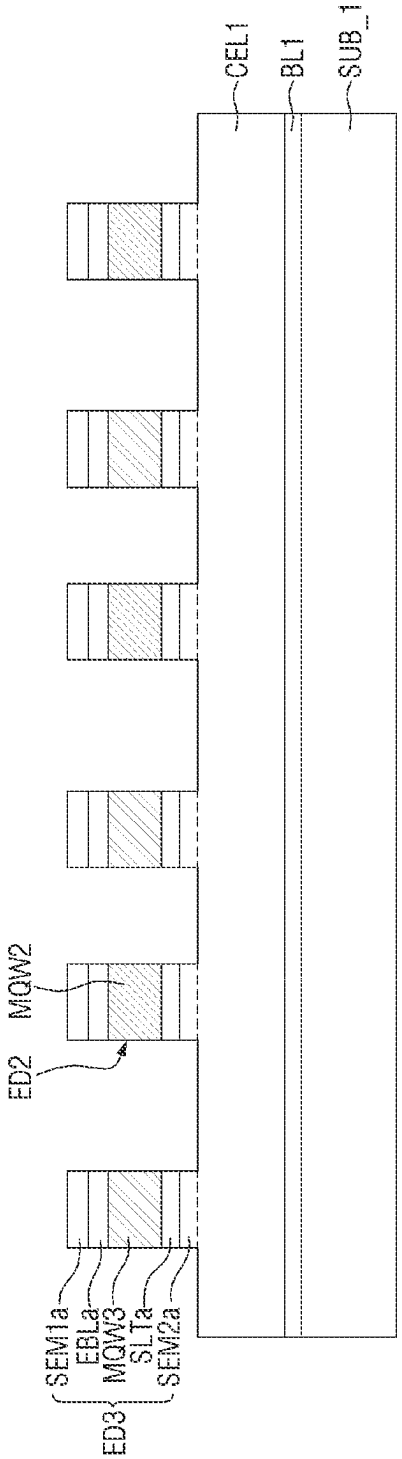


FIG. 18

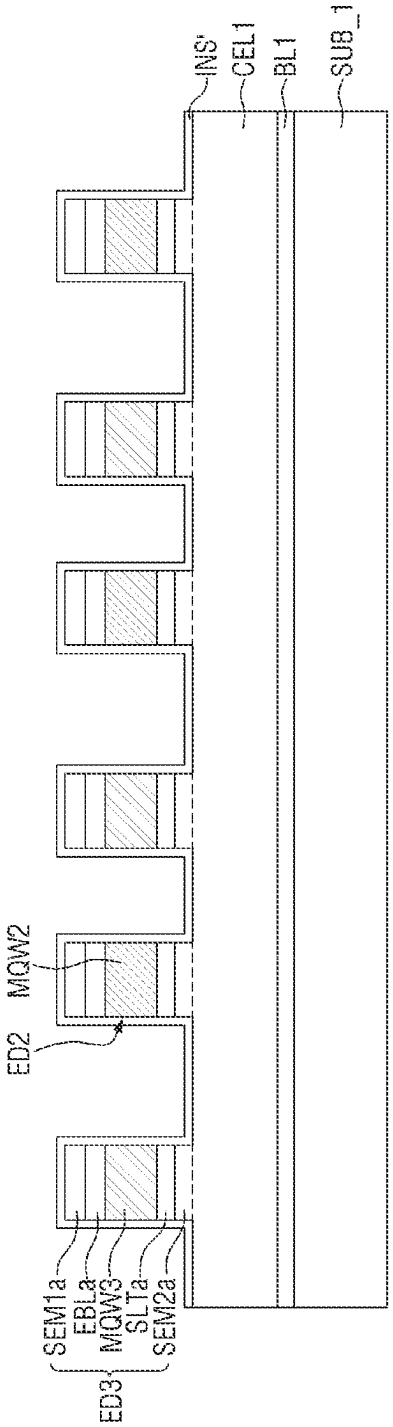


FIG. 19

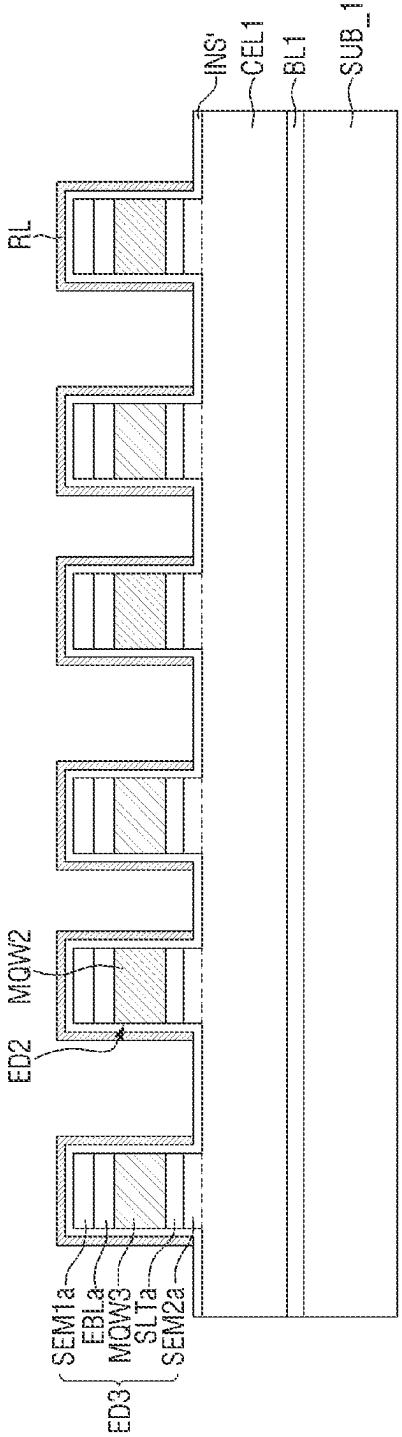


FIG. 20

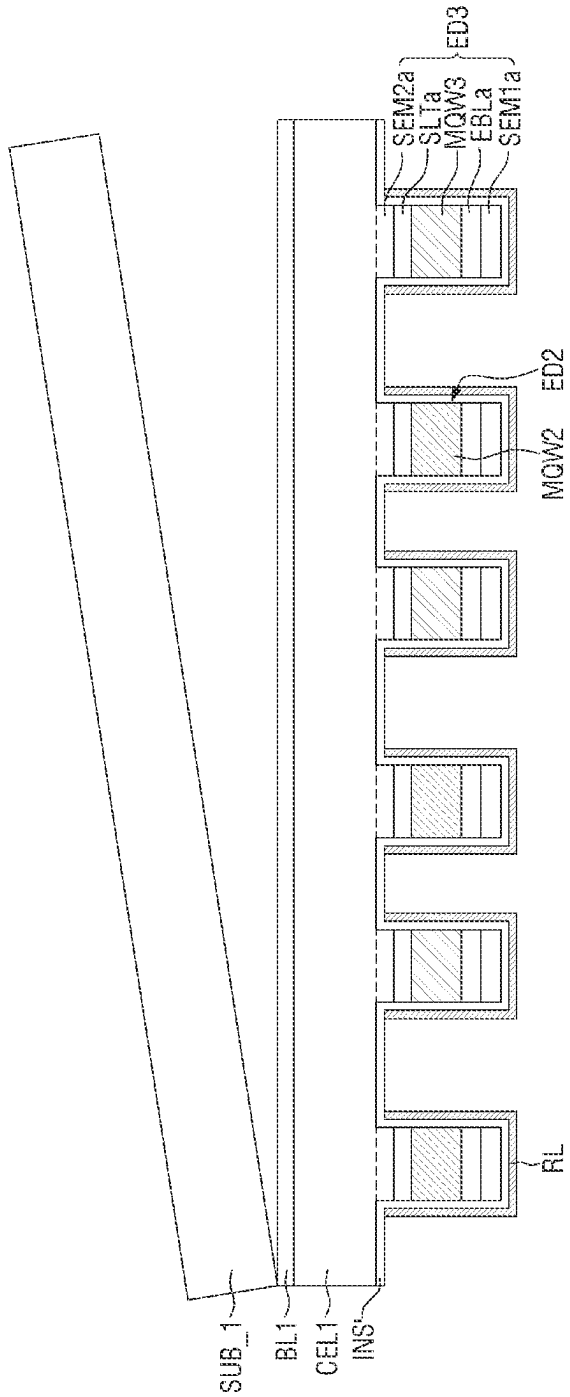


FIG. 21

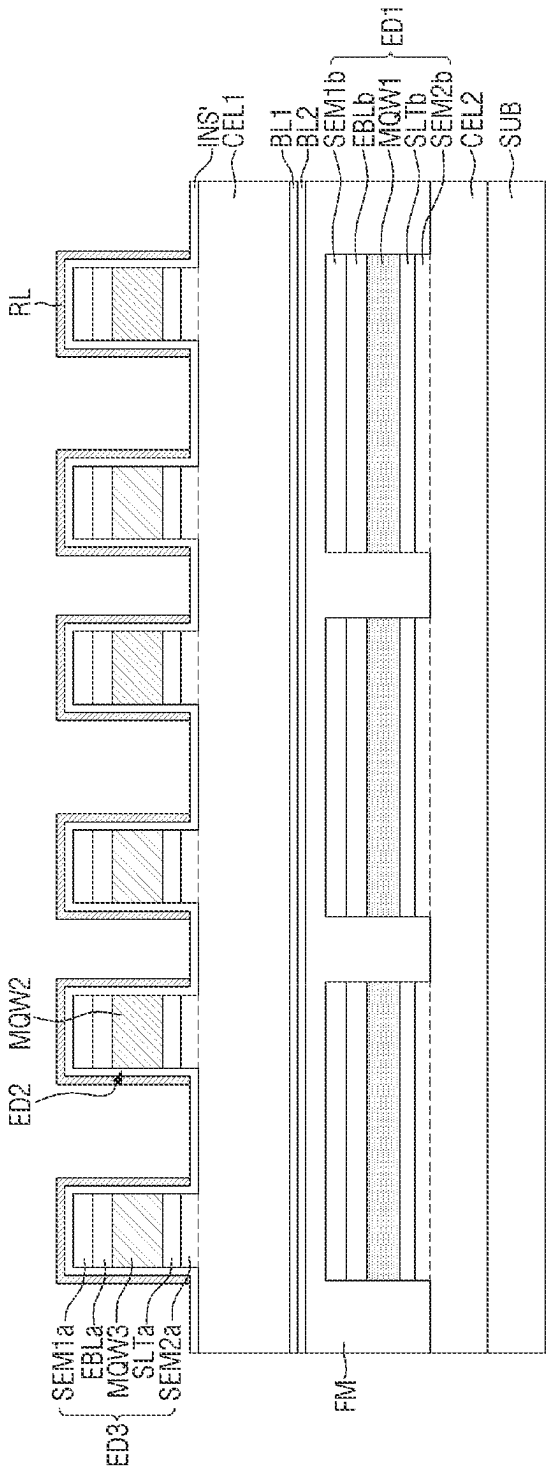

INS'
CEL1
BL1
BL2
SEM1b
EBLb
MQW1
SLTb
SEM2b
ED1
CEL2
SUB
RL
MQW2
ED2
SEM1a
EBLa
MQW3
SLTa
SEM2a
ED3
FM

FIG. 22

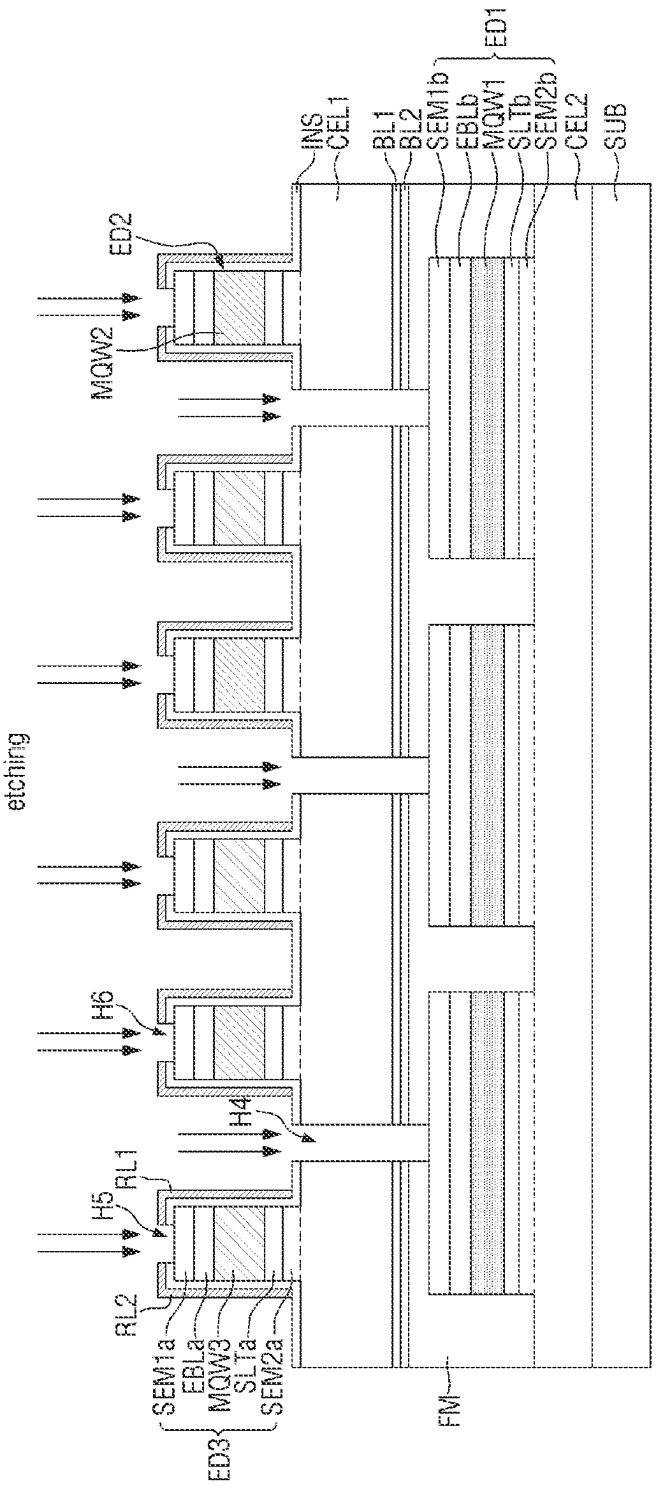

ED1
INS
CEL1
BL1
BL2
SEM1b
EBLb
MQW1
SLTb
SEM2b
CEL2
SUB
ED2
MQW2
etching
H6
H4
RL1
H5
RL2
SEM1a
EBLa
MQW3
SLTa
SEM2a
ED3
FM

FIG. 23

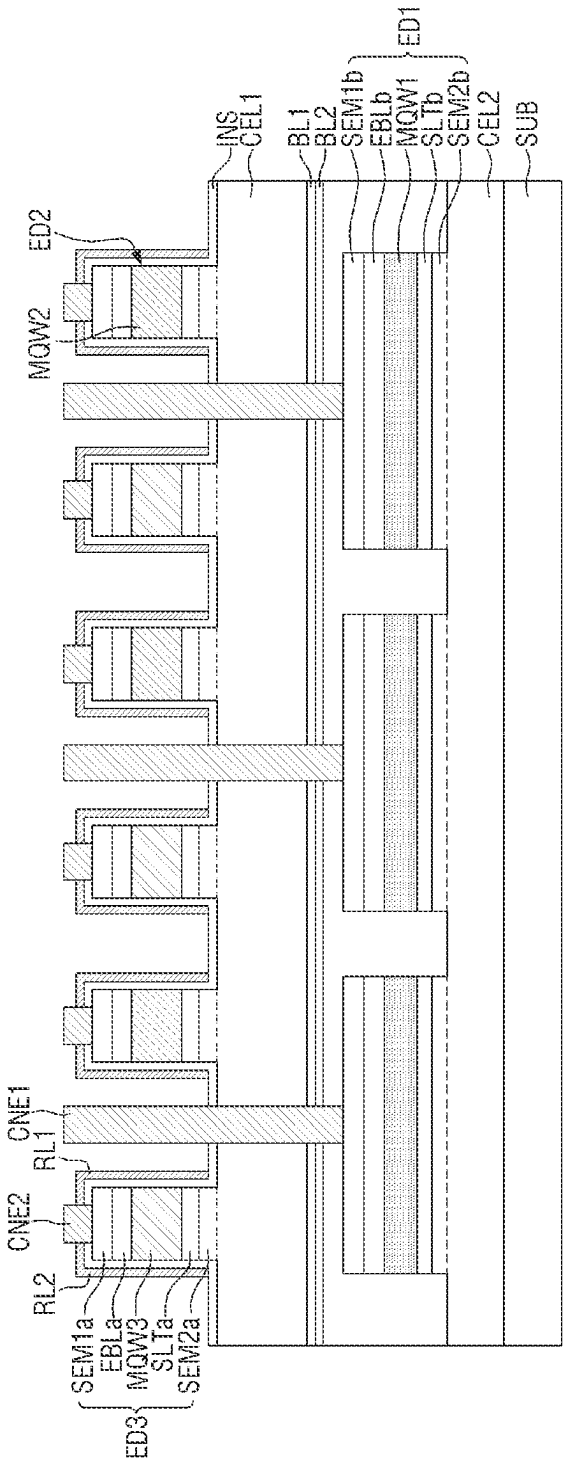

INS
CEL1
BL1
BL2
SEM1b
EBLb
MQW1
SLTb
SEM2b
ED1
CEL2
SUB
ED2
MQW2
CNE1
RL1
CNE2
RL2
SEM1a
EBLa
MQW3
SLTa
SEM2a
ED3

FIG. 24

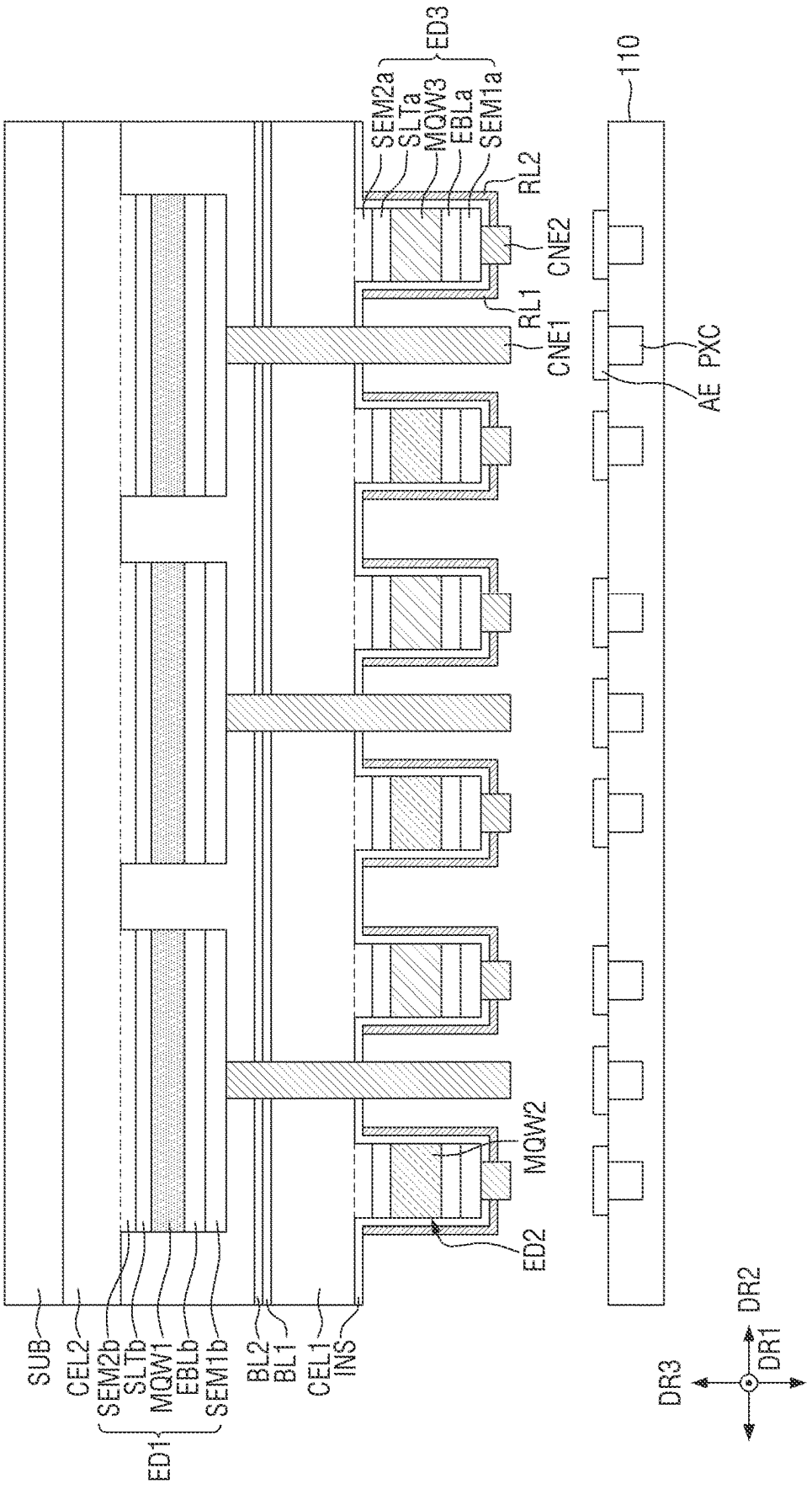

ED3
SEM2a
SLTa
MQW3
EBLa
SEM1a
110
RL2
CNE2
RL1
CNE1
PXC
AE
MQW2
ED2
SUB
CEL2
SEM2b
SLTb
MQW1
EBLb
SEM1b
ED1
BL2
BL1
CEL1
INS
DR2
DR1
DR3

FIG. 25

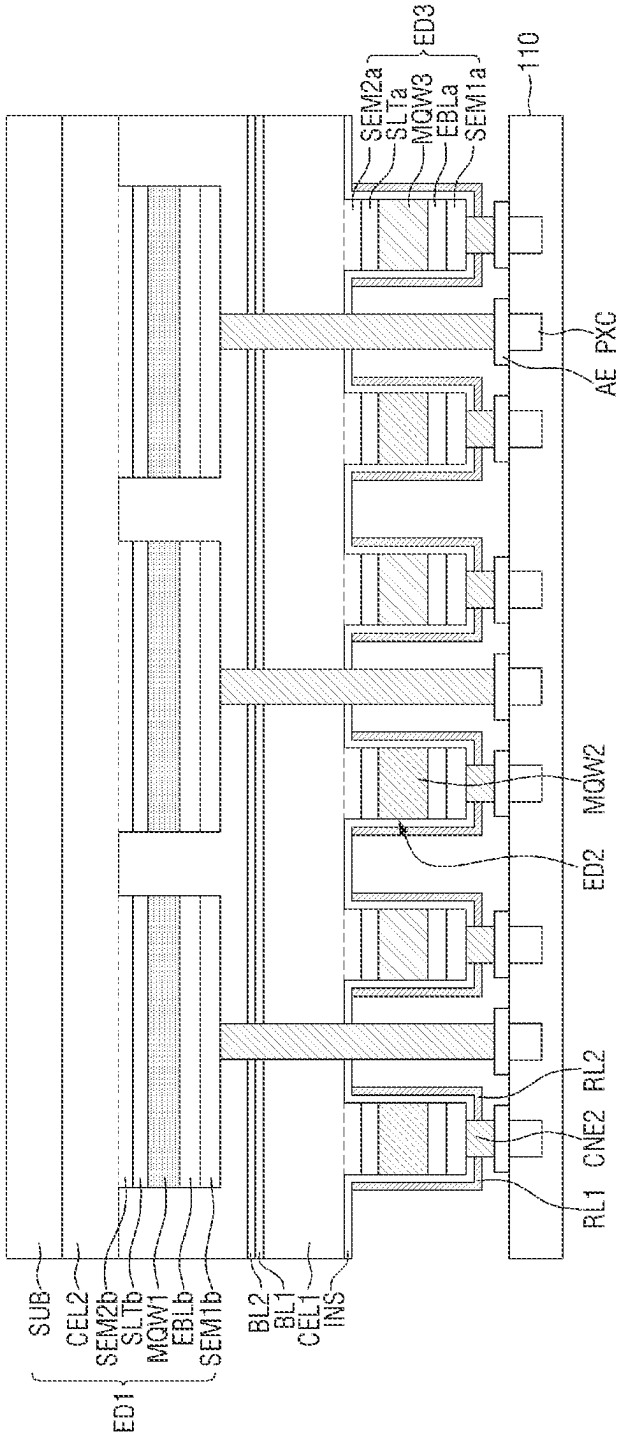

SUB
CEL2
SEM2b
SLTb
MQW1
EBLb
SEM1b
ED1
BL2
BL1
CEL1
INS
SEM2a
SLTa
MQW3
EBLa
SEM1a
ED3
110
AE
PXC
MQW2
ED2
RL2
CNE2
RL1

FIG. 26

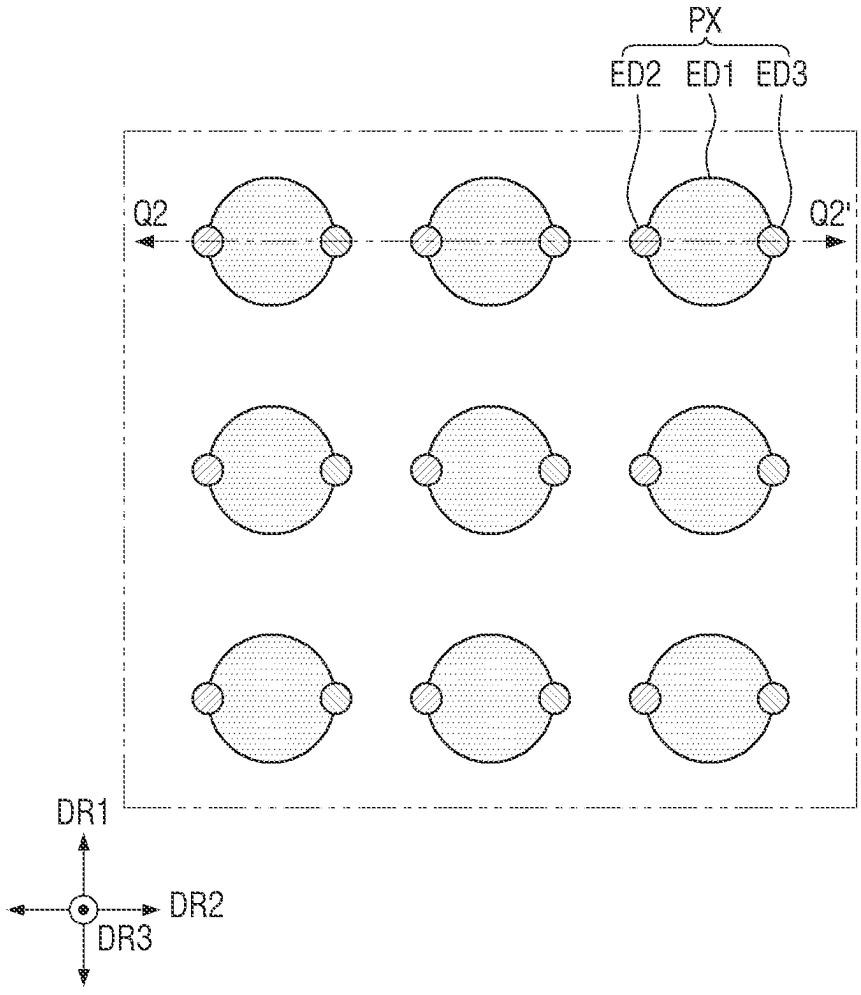
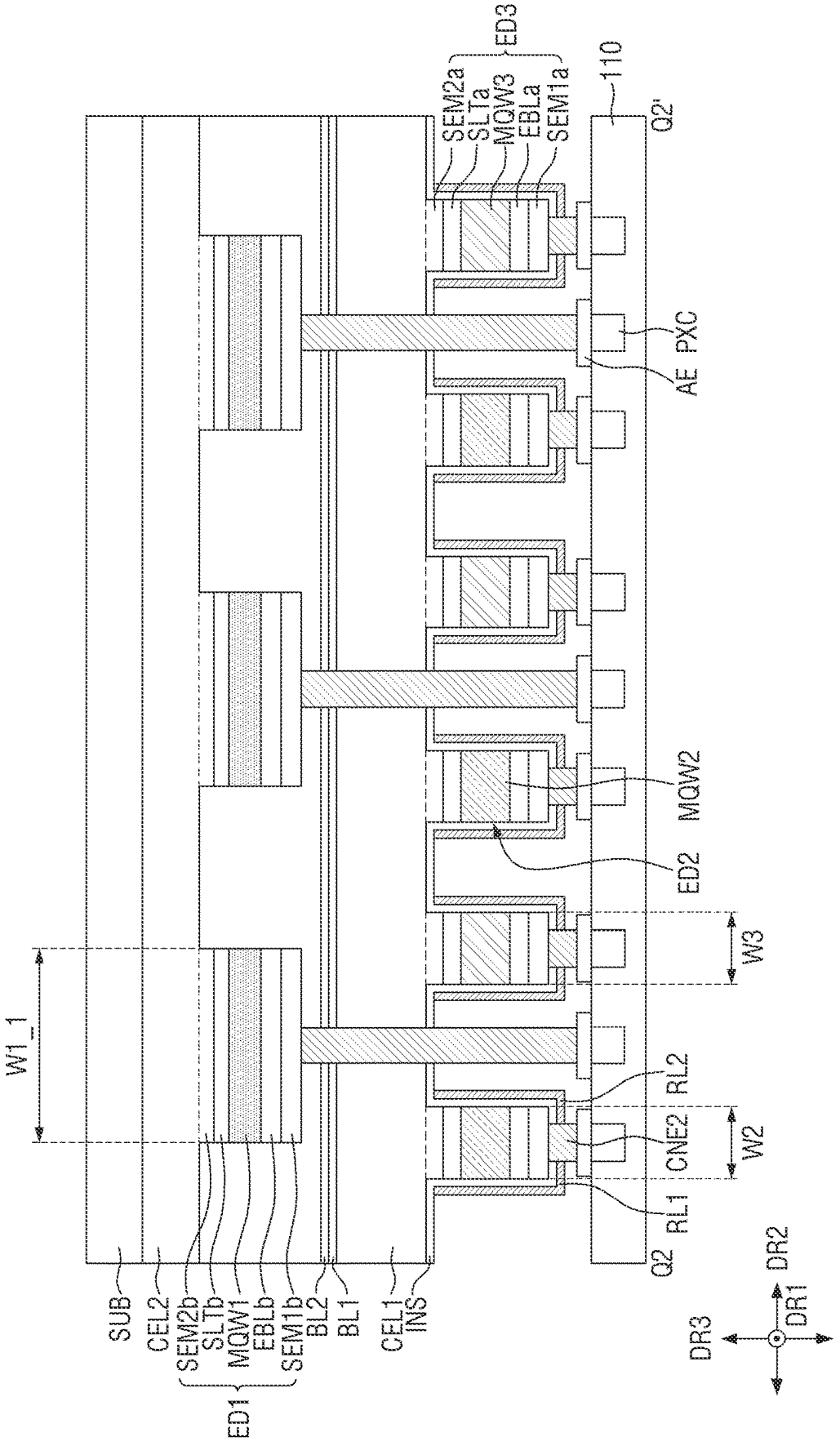


FIG. 27


ED3
SEM2a
SLTa
MQW3
EBLa
SEM1a
110
Q2'
PXC
AE
MQW2
ED2
W3
W1_1
RL2
CNE2
W2
RL1
Q2
SUB
CEL2
SEM2b
SLTb
MQW1
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SEM1b
BL2
BL1
CEL1
INS
ED1
DR2
DR1
DR3

FIG. 28

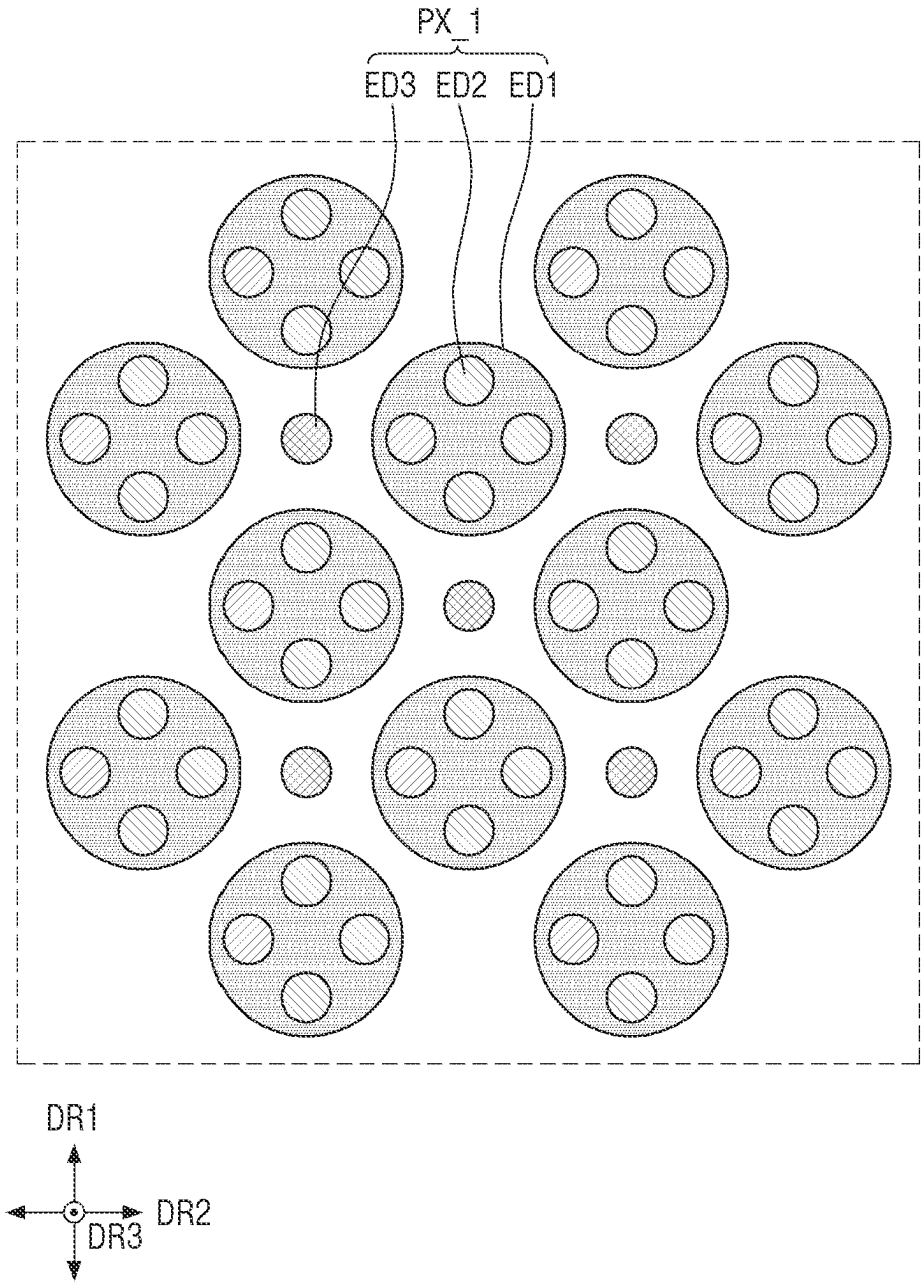
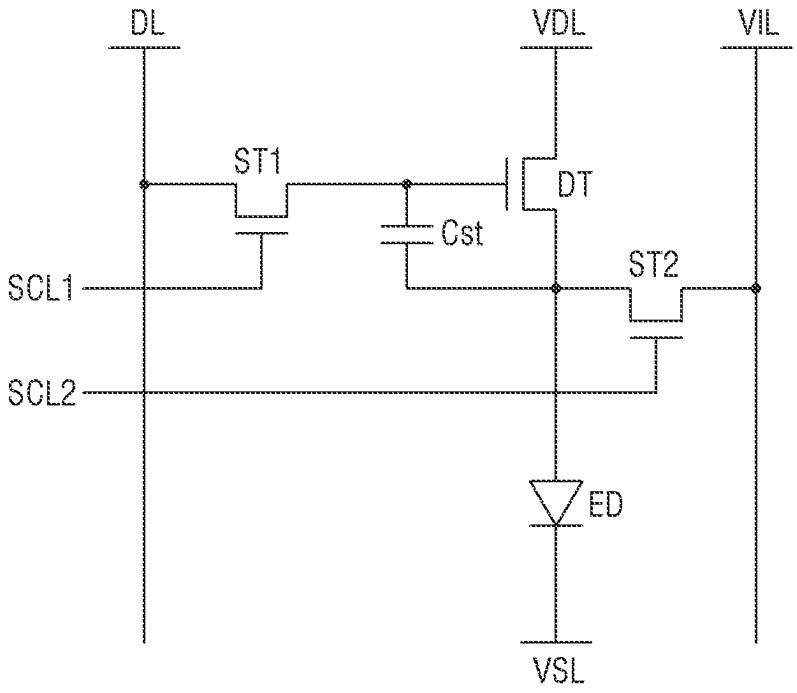


FIG. 29



ED: ED1, ED2, ED3

FIG. 30

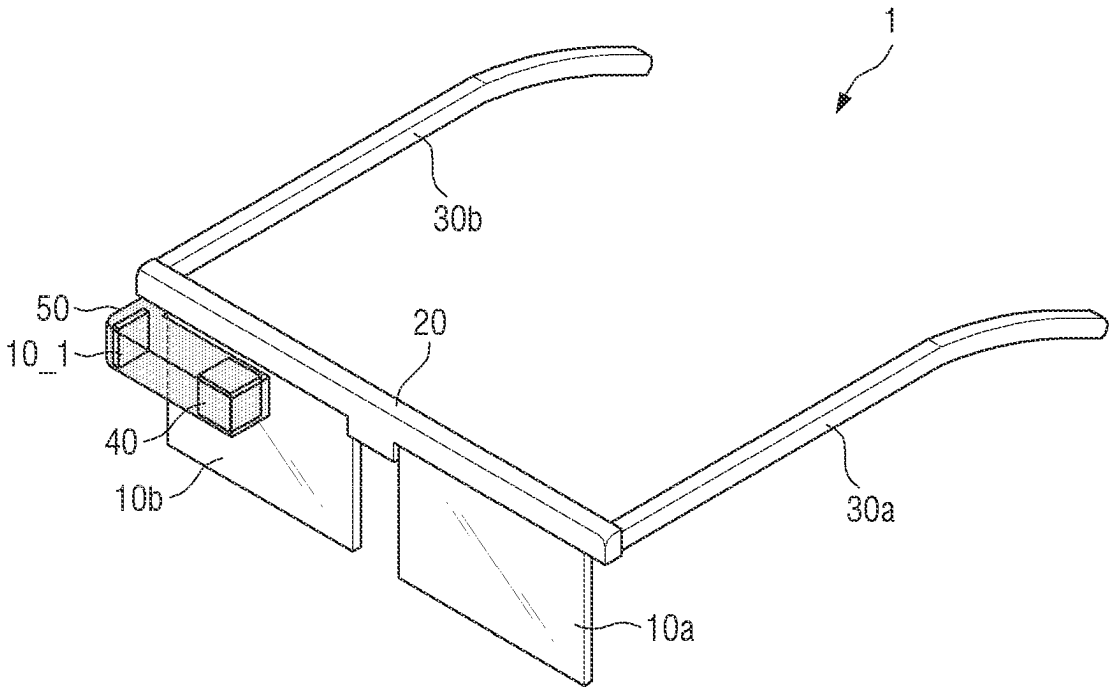


FIG. 31

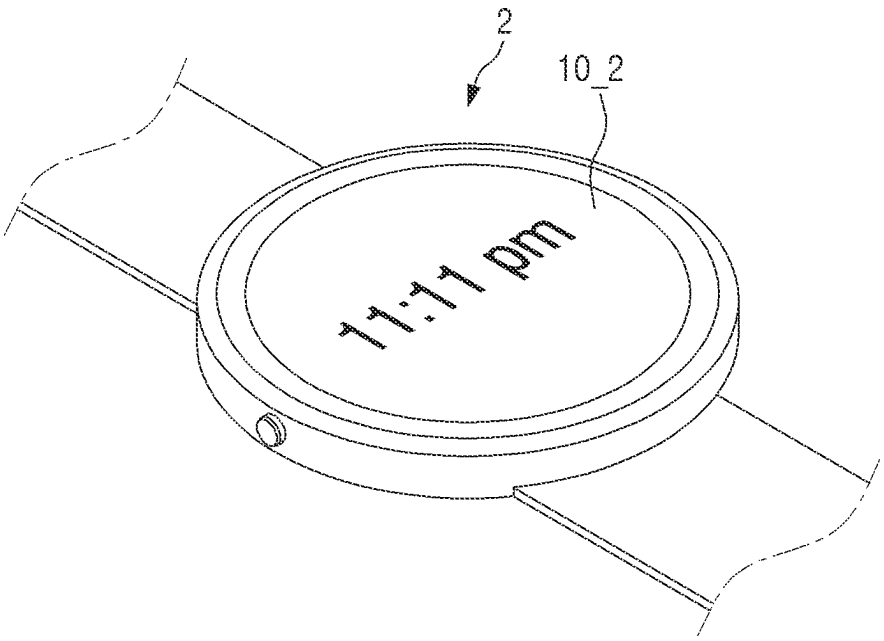


FIG. 32

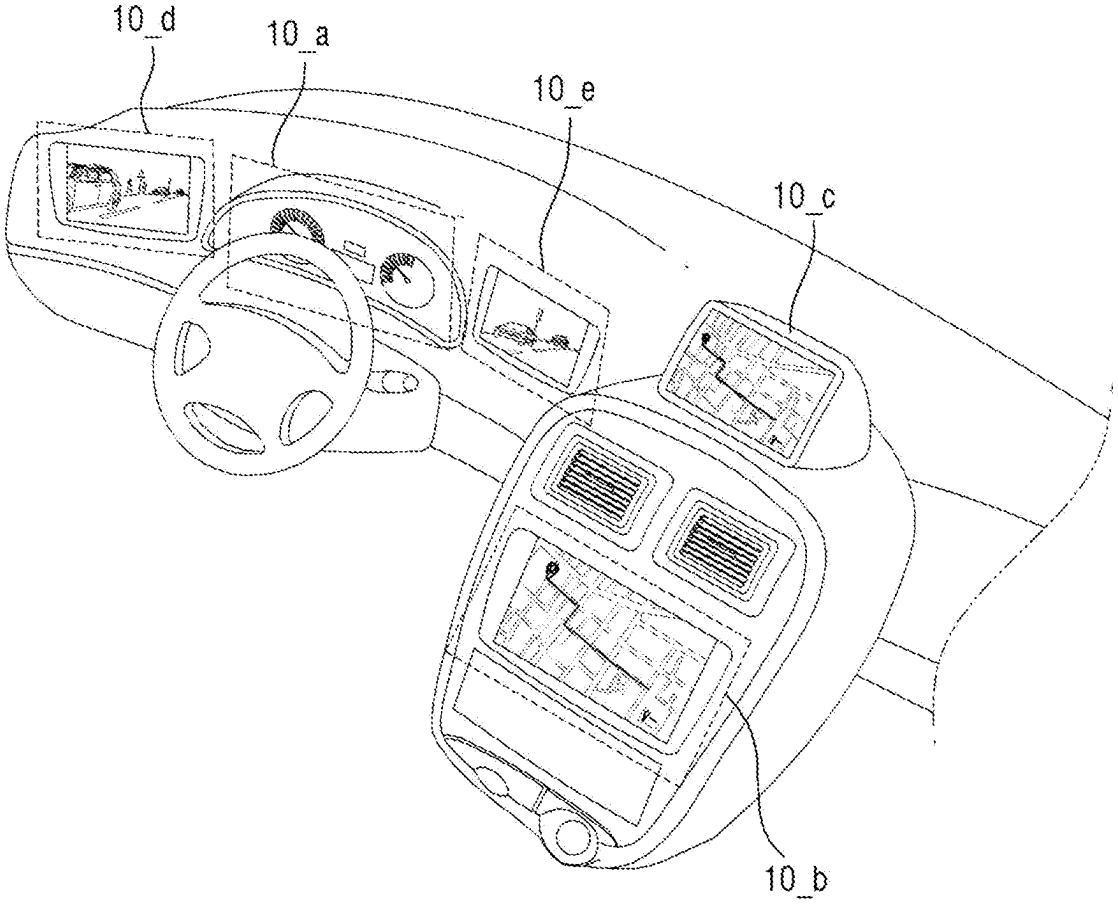


FIG. 33

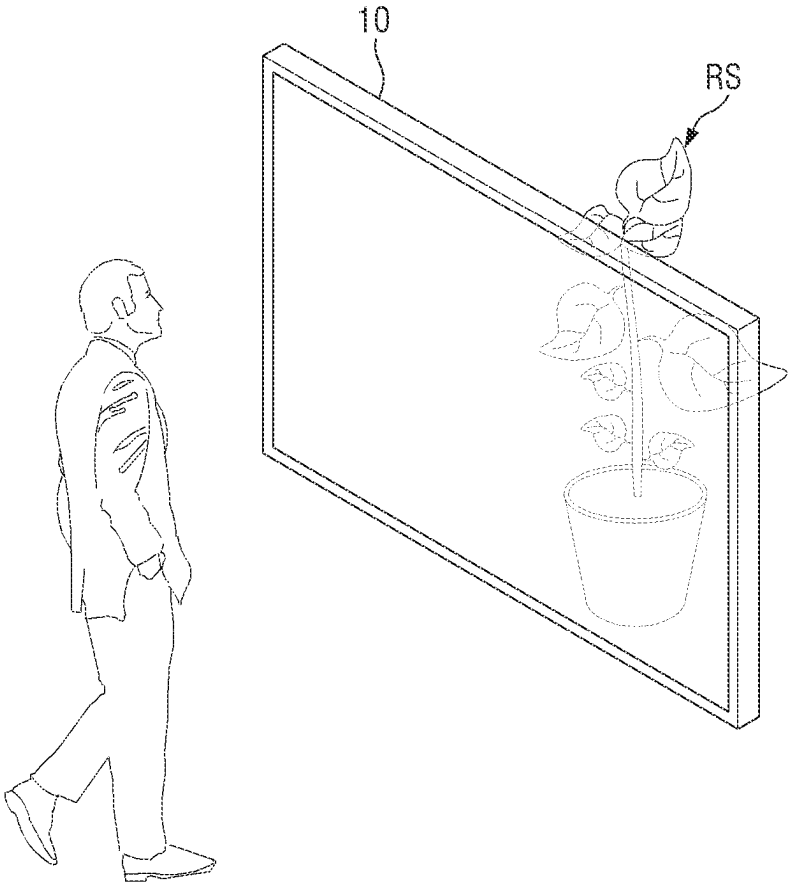
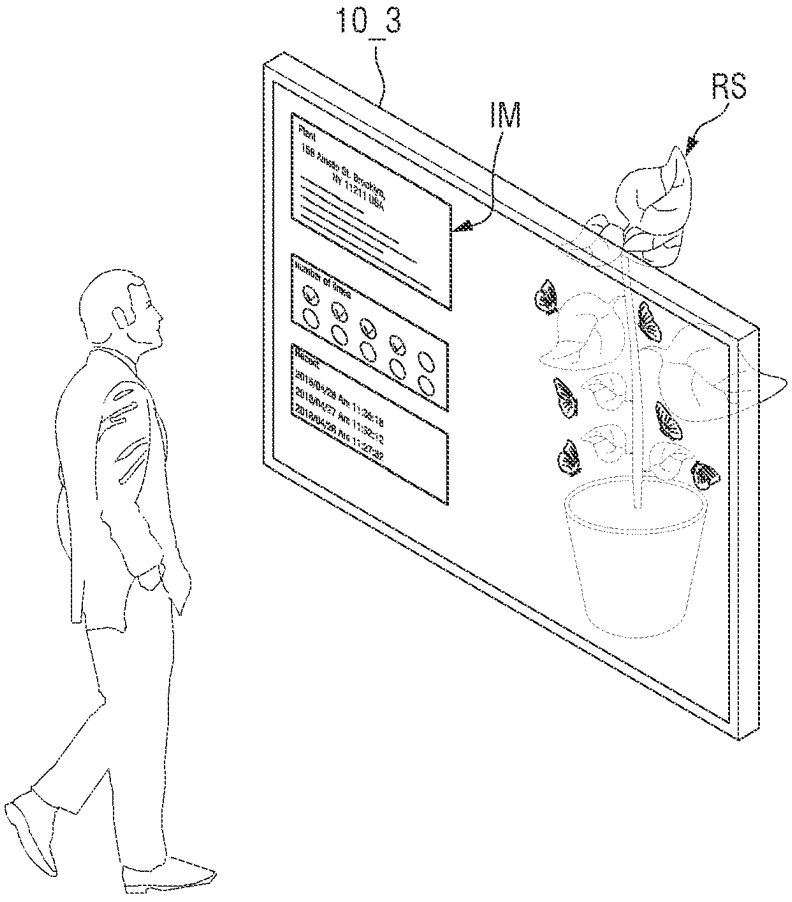


FIG. 34



DISPLAY DEVICE AND METHOD OF FABRICATING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority to, and the benefit of, Korean Patent Application No. 10-2021-0104920 filed on Aug. 9, 2021 in the Korean Intellectual Property Office, the disclosure of which is incorporated herein by reference in its entirety.

BACKGROUND

1. Field

The present disclosure relates to a display device and a method of fabricating the same.

2. Description of the Related Art

As the information-oriented society evolves, various demands for display devices are ever increasing. Display devices may be flat panel display devices, such as a liquid-crystal display device, a field emission display device, and a light-emitting display device. Light-emitting display devices may include an organic light-emitting display device including organic light-emitting diodes as the light-emitting elements, an inorganic light-emitting display device including inorganic semiconductor elements as the light-emitting elements, and a micro-LED display device including light-emitting diodes as the light-emitting elements.

Recently, a head mounted display including a light-emitting display device has been developed. A head mounted display (HMD) is a glasses-type monitor device providing virtual reality (VR) or augmented reality (AR) that is worn on a user's body in the form of glasses or a helmet to form a focus close to the user's eyes.

A high-resolution micro-LED display panel including micro light-emitting diodes is applied to head mounted displays.

SUMMARY

Aspects of the present disclosure provide a display device in which internal quantum efficiency is improved by increasing the area of a first light-emitting element.

Aspects of the present disclosure also provide a method of fabricating a display device in which internal quantum efficiency is improved by increasing the area of a first light-emitting element.

It should be noted that aspects of the present disclosure are not limited to the above-mentioned object, and other aspects of the present disclosure will be apparent to those skilled in the art from the following descriptions.

According to an aspect of the present disclosure, there is provided a display device including light-emitting elements arranged on a circuit board, and extending in a thickness direction of the circuit board, wherein the light-emitting elements include a first light-emitting element configured to emit a first light, and a second light-emitting element configured to emit a second light, wherein the first light-emitting element and the second light-emitting element are on different layers, and wherein a width of the first light-emitting element is greater than a width of the second light-emitting element.

The light-emitting elements may further include a third light-emitting element configured to emit a third light, and on a different layer from the first light-emitting element.

The third light-emitting element may be on a same layer as the second light-emitting element.

The width of the first light-emitting element may be greater than a width of the third light-emitting element.

The first light-emitting element may overlap the second light-emitting element and the third light-emitting element in a plan view.

The first light-emitting element may completely cover the second light-emitting element and the third light-emitting element in the plan view.

The light-emitting elements may each include a first semiconductor layer on the circuit board, an active layer on the first semiconductor layer, and a second semiconductor layer on the active layer.

The light-emitting elements may further include an electron blocking layer between the first semiconductor layer and the active layer, and a superlattice layer between the active layer and the second semiconductor layer.

The circuit board may further include pixel electrodes, wherein the first semiconductor layer of each of the light-emitting elements is connected to a respective one of the pixel electrodes.

The display device may further include connection electrodes respectively between the first semiconductor layers of the light-emitting elements and the pixel electrodes.

A length of the connection electrode corresponding to the first light-emitting element may be greater than a length of the connection electrode corresponding to the second light-emitting element.

The display device may further include a first common electrode layer between the second semiconductor layer of the second light-emitting element and the first semiconductor layer of the first light-emitting element.

The display device may further include a first bonding layer between the first common electrode layer and the first semiconductor layer of the first light-emitting element, and a second bonding layer between the first bonding layer and the first semiconductor layer of the first light-emitting element, and in direct contact with the first bonding layer.

The connection electrode of the first light-emitting element may penetrate through the first bonding layer, the second bonding layer, and the first common electrode layer.

According to another aspect of the present disclosure, there is provided a method of fabricating a display device, the method including forming a first light-emitting element configured to emit a first light on a first substrate, forming a first bonding layer above the first light-emitting element, forming a second bonding layer on a surface of a second substrate, forming a second light-emitting element configured to emit a second light, and a third light-emitting element configured to emit a third light, on the second bonding layer, delaminating the second substrate from the second bonding layer, and bonding the first bonding layer with the second bonding layer.

Each of the light-emitting elements may include a first semiconductor layer on a circuit board, an active layer on the first semiconductor layer, and a second semiconductor layer on the active layer.

The method may further include connecting pixel electrodes of the circuit board with the light-emitting elements, respectively, after bonding the first bonding layer with the second bonding layer.

The method may further include forming connection electrodes respectively between the first semiconductor lay-

ers of the light-emitting elements and the pixel electrodes, after bonding the first bonding layer with the second bonding layer and before connecting pixel electrodes of the circuit board with the light-emitting elements, respectively.

A width of the first light-emitting element may be greater than a width of the second light-emitting element and may be greater than a width of the third light-emitting element.

The first light-emitting element may overlap the second light-emitting element and the third light-emitting element in a plan view.

The details of one or more embodiments of the subject matter described in this specification are set forth in the accompanying drawings and the description below.

According to embodiments of the present disclosure, it is possible to improve the internal quantum efficiency of a display device by increasing the area of a first light-emitting element.

It should be noted that aspects of the present disclosure are not limited to those described above and other aspects of the present disclosure will be apparent to those skilled in the art from the following descriptions.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other aspects of the present disclosure will become more apparent by describing in detail embodiments thereof with reference to the attached drawings, in which:

FIG. **1** is a view showing a layout of a display device according to some embodiments of the present disclosure.

FIG. **2** is a view showing a layout of area A of FIG. **1**.

FIG. **3** is a plan view showing area B of FIG. **2** in detail.

FIG. **4** is a cross-sectional view showing an example of a display panel, taken along the line Q**1**-Q**1'** of FIG. **3**.

FIG. **5** is a cross-sectional view showing the display panel of FIG. **4** in more detail.

FIG. **6** is a flowchart for illustrating a method for fabricating a display device according to some embodiments of the present disclosure.

FIGS. **7** to **25** are cross-sectional views illustrating processing operations of a method of fabricating a display device according to some embodiments of the present disclosure.

FIG. **26** is a plan view showing a layout of first to third light-emitting diodes according to other embodiments.

FIG. **27** is a cross-sectional view showing the display panel, taken along the line Q**2**-Q**2'** of FIG. **26**.

FIG. **28** is a plan view showing a layout of first to third light-emitting diodes according to other embodiments.

FIG. **29** is an equivalent circuit diagram of a pixel of a display device according to some embodiments of the present disclosure.

FIGS. **30** to **32** are cross-sectional views showing applications of a display device according to some embodiments of the present disclosure.

FIGS. **33** and **34** are views showing an example of a transparent display device including a display device according to some embodiments.

DETAILED DESCRIPTION

Aspects of some embodiments of the present disclosure and methods of accomplishing the same may be understood more readily by reference to the detailed description of embodiments and the accompanying drawings. Hereinafter, embodiments will be described in more detail with reference to the accompanying drawings. The described embodiments, however, may have various modifications and may be embodied in various different forms, and should not be construed as being limited to only the illustrated embodiments herein. Rather, these embodiments are provided as examples so that this disclosure will be thorough and complete, and will fully convey the aspects of the present disclosure to those skilled in the art, and it should be understood that the present disclosure covers all the modifications, equivalents, and replacements within the idea and technical scope of the present disclosure. Accordingly, processes, elements, and techniques that are not necessary to those having ordinary skill in the art for a complete understanding of the aspects of the present disclosure may not be described.

Unless otherwise noted, like reference numerals, characters, or combinations thereof denote like elements throughout the attached drawings and the written description, and thus, descriptions thereof will not be repeated. Further, parts that are not related to, or that are irrelevant to, the description of the embodiments might not be shown to make the description clear.

In the drawings, the relative sizes of elements, layers, and regions may be exaggerated for clarity. Additionally, the use of cross-hatching and/or shading in the accompanying drawings is generally provided to clarify boundaries between adjacent elements. As such, neither the presence nor the absence of cross-hatching or shading conveys or indicates any preference or requirement for particular materials, material properties, dimensions, proportions, commonalities between illustrated elements, and/or any other characteristic, attribute, property, etc., of the elements, unless specified.

Various embodiments are described herein with reference to sectional illustrations that are schematic illustrations of embodiments and/or intermediate structures. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Further, specific structural or functional descriptions disclosed herein are merely illustrative for the purpose of describing embodiments according to the concept of the present disclosure. Thus, embodiments disclosed herein should not be construed as limited to the particular illustrated shapes of regions, but are to include deviations in shapes that result from, for instance, manufacturing.

For example, an implanted region illustrated as a rectangle will, typically, have rounded or curved features and/or a gradient of implant concentration at its edges rather than a binary change from implanted to non-implanted region. Likewise, a buried region formed by implantation may result in some implantation in the region between the buried region and the surface through which the implantation takes place.

Thus, the regions illustrated in the drawings are schematic in nature and their shapes are not intended to illustrate the actual shape of a region of a device and are not intended to be limiting. Additionally, as those skilled in the art would realize, the described embodiments may be modified in various different ways, all without departing from the spirit or scope of the present disclosure.

In the detailed description, for the purposes of explanation, numerous specific details are set forth to provide a thorough understanding of various embodiments. It is apparent, however, that various embodiments may be practiced without these specific details or with one or more equivalent arrangements. In other instances, well-known structures and devices may be shown in block diagram form in order to avoid unnecessarily obscuring various embodiments.

Spatially relative terms, such as "beneath," "below," "lower," "under," "above," "upper," and the like, may be used herein for ease of explanation to describe one element

or feature's relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or in operation, in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as "below" or "beneath" or "under" other elements or features would then be oriented "above" the other elements or features. Thus, the example terms "below" and "under" can encompass both an orientation of above and below. The device may be otherwise oriented (e.g., rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein should be interpreted accordingly. Similarly, when a first part is described as being arranged "on" a second part, this indicates that the first part is arranged at an upper side or a lower side of the second part without the limitation to the upper side thereof on the basis of the gravity direction.

Further, in this specification, the phrase "on a plane," or "plan view," means viewing a target portion from the top, and the phrase "on a cross-section" means viewing a cross-section formed by vertically cutting a target portion from the side.

It will be understood that when an element, layer, region, or component is referred to as being "formed on," "on," "connected to," or "coupled to" another element, layer, region, or component, it can be directly formed on, on, connected to, or coupled to the other element, layer, region, or component, or indirectly formed on, on, connected to, or coupled to the other element, layer, region, or component such that one or more intervening elements, layers, regions, or components may be present. In addition, this may collectively mean a direct or indirect coupling or connection and an integral or non-integral coupling or connection. For example, when a layer, region, or component is referred to as being "electrically connected" or "electrically coupled" to another layer, region, or component, it can be directly electrically connected or coupled to the other layer, region, and/or component or intervening layers, regions, or components may be present. However, "directly connected/directly coupled," or "directly on," refers to one component directly connecting or coupling another component, or being on another component, without an intermediate component. Meanwhile, other expressions describing relationships between components such as "between," "immediately between" or "adjacent to" and "directly adjacent to" may be construed similarly. In addition, it will also be understood that when an element or layer is referred to as being "between" two elements or layers, it can be the only element or layer between the two elements or layers, or one or more intervening elements or layers may also be present.

For the purposes of this disclosure, expressions such as "at least one of," when preceding a list of elements, modify the entire list of elements and do not modify the individual elements of the list. For example, "at least one of X, Y, and Z," "at least one of X, Y, or Z," and "at least one selected from the group consisting of X, Y, and Z" may be construed as X only, Y only, Z only, any combination of two or more of X, Y, and Z, such as, for instance, XYZ, XYY, YZ, and ZZ, or any variation thereof. Similarly, the expression such as "at least one of A and B" may include A, B, or A and B. As used herein, "or" generally means "and/or," and the term "and/or" includes any and all combinations of one or more of the associated listed items. For example, the expression such as "A and/or B" may include A, B, or A and B.

It will be understood that, although the terms "first," "second," "third," etc., may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are used to distinguish one element, component, region, layer or section from another element, component, region, layer or section. Thus, a first element, component, region, layer or section described below could be termed a second element, component, region, layer or section, without departing from the spirit and scope of the present disclosure. The description of an element as a "first" element may not require or imply the presence of a second element or other elements. The terms "first", "second", etc. may also be used herein to differentiate different categories or sets of elements. For conciseness, the terms "first", "second", etc. may represent "first-category (or first-set)", "second-category (or second-set)", etc., respectively.

In the examples, the x-axis, the y-axis, and/or the z-axis are not limited to three axes of a rectangular coordinate system, and may be interpreted in a broader sense. For example, the x-axis, the y-axis, and the z-axis may be perpendicular to one another, or may represent different directions that are not perpendicular to one another. The same applies for first, second, and/or third directions.

The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the present disclosure. As used herein, the singular forms "a" and "an" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "have," "having," "includes," and "including," when used in this specification, specify the presence of the stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

When one or more embodiments may be implemented differently, a specific process order may be performed differently from the described order. For example, two consecutively described processes may be performed substantially at the same time or performed in an order opposite to the described order.

As used herein, the term "substantially," "about," "about," and similar terms are used as terms of approximation and not as terms of degree, and are intended to account for the inherent deviations in measured or calculated values that would be recognized by those of ordinary skill in the art. "About" or "about," as used herein, is inclusive of the stated value and means within an acceptable range of deviation for the particular value as determined by one of ordinary skill in the art, considering the measurement in question and the error associated with measurement of the particular quantity (i.e., the limitations of the measurement system). For example, "about" may mean within one or more standard deviations, or within ±30%, 20%, 10%, 5% of the stated value. Further, the use of "may" when describing embodiments of the present disclosure refers to "one or more embodiments of the present disclosure."

Also, any numerical range disclosed and/or recited herein is intended to include all sub-ranges of the same numerical precision subsumed within the recited range. For example, a range of "1.0 to 10.0" is intended to include all subranges between (and including) the recited minimum value of 1.0 and the recited maximum value of 10.0, that is, having a minimum value equal to or greater than 1.0 and a maximum value equal to or less than 10.0, such as, for example, 2.4 to 7.6. Any maximum numerical limitation recited herein is

intended to include all lower numerical limitations subsumed therein, and any minimum numerical limitation recited in this specification is intended to include all higher numerical limitations subsumed therein. Accordingly, Applicant reserves the right to amend this specification, including the claims, to expressly recite any sub-range subsumed within the ranges expressly recited herein. All such ranges are intended to be inherently described in this specification such that amending to expressly recite any such subranges would comply with the requirements of 35 U.S.C. § 112(a) and 35 U.S.C. § 132(a).

Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which the present disclosure belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and/or the present specification, and should not be interpreted in an idealized or overly formal sense, unless expressly so defined herein.

Features of various embodiments of the present disclosure may be combined partially or totally. As will be clearly appreciated by those skilled in the art, technically various interactions and operations are possible. Various embodiments can be practiced individually or in combination.

Hereinafter, embodiments of the present disclosure will be described with reference to the accompanying drawings.

FIG. **1** is a view showing a layout of a display device according to some embodiments of the present disclosure. FIG. **2** is a view showing a layout of area A of FIG. **1**. FIG. **3** is a plan view showing area B of FIG. **2** in detail.

In the example shown in FIGS. **1** to **3**, the display device according to some embodiments is a micro light-emitting diode display device including a micro light-emitting diode as a light-emitting element. It should be understood, however, that the present disclosure is not limited thereto.

In addition, in the example shown in FIGS. **1** to **3**, the display device according to some embodiments is implemented as a light-emitting diode on silicon (LEDoS) microdisplay (e.g., light-emitting diodes are located on a semiconductor circuit board formed via a semiconductor process). It should be understood, however, that embodiments of the present disclosure are not limited thereto.

In FIGS. **1** to **3**, a first direction DR**1** indicates the vertical direction of the display panel **100**, a second direction DR**2** indicates the horizontal direction of the display panel **100**, and a third direction DR**3** indicates the thickness direction of the display panel **100**. As used herein, the terms "left," "right," "upper" and "lower" sides indicate relative positions when the display panel **100** is viewed from the top/viewed in a plan view. For example, the right side refers to one side in the second direction DR**2**, the left side refers to the opposite side in the second direction DR**2**, the upper side refers to one side in the first direction DR**1**, and the lower side refers to the opposite side in the first direction DR**1**. In addition, the upper portion refers to the side indicated by the arrow of the third direction DR**3**, while the lower portion refers to the opposite side in the third direction DR**3**.

Referring to FIGS. **1** to **3**, a display device **10** according to some embodiments includes a display panel **100** including a display area DA and a non-display area NDA.

The display panel **100** may have a quadrangular shape having shorter sides in the first direction DR**1** and longer sides in the second direction DR**2** when viewed from the top/viewed in a plan view. It should be understood, however, that the shape of the display panel **100** when viewed from the top is not limited thereto. It may have a polygonal, circular, oval, or irregular shape other than the rectangular shape when viewed from the top.

In the display area DA, images may be displayed. In the non-display area NDA, images may not be displayed. The shape of the display area DA may follow the shape of the display panel **100** when viewed from the top. In the example shown in FIG. **1**, the display area DA has a rectangular shape when viewed from the top. The display area DA may be located at the central area of the display panel **100**. The non-display area NDA may be located around the display area DA. The non-display area NDA may surround the display area DA.

The display area DA of the display panel **100** may include a plurality of pixels PX. Each of the pixels PX may be defined as a minimum light-emitting unit for displaying white light.

Each of the pixels PX may include a plurality of emission areas, from each of which light exits. Light-emitting diodes ED**1**, ED**2**, and ED**3** may be located in each of the emission areas. Although each of the plurality of pixels PX includes three emission areas according to some embodiments, the present disclosure is not limited thereto. For example, each of the plurality of pixels PX may include four emission areas. In addition, it may be interpreted that each of the pixels PX includes three light-emitting diodes ED**1**, ED**2**, and ED**3**.

Each of the plurality of emission areas may include a first light-emitting diode ED**1** for emitting a first light, a second light-emitting diode ED**2** for emitting a second light, and a third light-emitting diode ED**3** for emitting a third light. Although the light-emitting diodes ED**1**, ED**2**, and ED**3** have a circular shape when viewed from the top in the example shown, embodiments of the present disclosure are not limited thereto. For example, the light-emitting diodes ED**1**, ED**2**, and ED**3** may have a polygonal, oval, or irregular shape other than a circular shape.

Each of the first emission areas refers to an area for emitting the first light. Each of the first emission areas may output the first light emitted from the first light-emitting diode ED**1** as it is. The first light may be light in a red wavelength range. The red wavelength range may be about 600 nm to about 750 nm, but embodiments of the present disclosure are not limited thereto.

Each of the second emission areas refers to an area for emitting the second light. Each of the second emission areas may output the second light emitted from the second light-emitting diode ED**2**. The second light may be light in a green wavelength range. The green wavelength range may be about 480 nm to about 560 nm, but embodiments of the present disclosure are not limited thereto.

Each of the third emission areas refers to an area for emitting the third light. Each of the third emission areas may output the third light emitted from the third light-emitting diode ED**3**. The third light may be light in a blue wavelength range. The blue wavelength range may be about 370 nm to about 460 nm, but embodiments of the present disclosure are not limited thereto.

As shown in FIG. **3**, the pixels PX may be arranged in the first direction DR**1** and the second direction DR**2**. The width of the first light-emitting diode ED**1** included in the pixel PX may be greater than the width of the second light-emitting diode ED**2** and the width of the third light-emitting diode ED**3**. The first light-emitting diode ED**1** may overlap the second light-emitting diode ED**2** and the third light-emitting diode ED**3** when viewed from the top. According to some embodiments of the present disclosure, the first light-emit-

ting diode ED1 may completely cover the second light-emitting diode ED2 and the third light-emitting diode ED3 when viewed from the top. In a single pixel PX, the second light-emitting diode ED2 may be located on the left side of the center of the first light-emitting diode ED1 while the third light-emitting diode ED3 may be located on the right side thereof in the second direction DR2. It should be understood, however, that the present disclosure is not limited thereto.

The non-display area NDA may include a first pad area PDA1 and a second pad area PDA2.

The first pad area PDA1 may be located in the non-display area NDA. The first pad area PDA1 may be located at the upper portion of the display panel **100**. The first pad area PDA1 may include first pads PD1 connected to an external circuit board.

The second pad area PDA2 may be located in the non-display area NDA. The second pad area PDA2 may include second pads connected to an external circuit board. The second pad area PDA2 may be omitted.

In addition, the non-display area NDA may further include a common electrode connection area CPA surrounding the display area DA.

The common electrode connection area CPA may be located in the non-display area NDA, and may be located between the first pad area PDA1 and the display area DA, and between the second pad area PDA2 and the display area DA. In addition, the common electrode connection area CPA may be located on one side and on the opposite side of the display area DA in the first direction DR1, and may be located on one side and on the opposite side in the second direction DR2. The common electrode connection area CPA may include a plurality of connection electrodes CCP to be connected to the semiconductor circuit board.

Although the common electrode connection area CPA completely surrounds the display area DA in the example shown in FIG. **1**, the present specification is not limited thereto. For example, the common electrode connection area CPA may be located on one side, on both sides, or on at least three sides of the display area DA.

FIG. **4** is a cross-sectional view showing an example of a display panel, taken along the line Q1-Q1' of FIG. **3**. FIG. **5** is a cross-sectional view showing the display panel of FIG. **4** in more detail.

Referring to FIGS. **4** and **5** in conjunction with FIGS. **1** to **3**, in the display device **10** according to some embodiments, the display panel **100** (see FIG. **1**) may include a circuit board and a display substrate **300**. The circuit board may include a first substrate **110** and pixel circuits PXC, and the display substrate **300** may include light-emitting diodes ED1, ED2, and ED3.

The first substrate **110** may be a semiconductor circuit board. The first substrate **110** is a silicon wafer substrate formed using a semiconductor process, and may include a plurality of pixel circuits PXC. Each of the pixel circuits PXC may be formed via a process of forming a semiconductor circuit on a silicon wafer. Each of the plurality of pixel circuits PXC may include at least one transistor and at least one capacitor formed via a semiconductor process. For example, the plurality of pixel circuits PXC may include CMOS circuit.

The plurality of pixel circuits PXC may be located in the display area DA and the non-display area NDA. Among the plurality of pixel circuits PXC, the pixel circuits PXC located in the display area DA may be electrically connected to the pixel electrodes AE, respectively. The plurality of pixel circuits PXC located in the display area DA may be associated with the plurality of pixel electrodes AE, respectively. They may respectively overlap the light-emitting diodes ED1, ED2, and ED3 located in the display area DA in the third direction DR3, which is the thickness direction.

The plurality of light-emitting diodes ED1, ED2, and ED3 of the display substrate **300** may be located in the display area DA of the display substrate **300**, and may be associated with the plurality of pixel electrodes AE of the first substrate **110**, respectively.

The light-emitting diodes ED1, ED2, and ED3 may be inorganic light-emitting diodes. The light-emitting diodes ED1, ED2, and ED3 may include semiconductor layers and active layers. The active layers may include first to third active layers MQW1, MQW2, and MQW3. The light-emitting diodes ED1, ED2, and ED3 may be electrically connected to the pixel circuits PXC of the first substrate **110** to emit light from the active layers MQW1, MQW2, and MQW3.

The light-emitting diodes ED1, ED2, and ED3 may have a shape extended in the third direction DR3. The length of the pixel electrodes of the light-emitting diodes ED1, ED2, and ED3 in the third direction DR3 may be smaller than the length thereof in the horizontal direction. For example, the length of the light-emitting diodes ED1, ED2, and ED3 in the third direction DR3 may be about 1 μm to about 5 μm. The light-emitting diodes ED1, ED2, and ED3 may have a cylindrical shape, a disk shape, or a rod shape having the width that is greater than the height. It should be understood, however, that the present disclosure is not limited thereto. The light-emitting diodes ED1, ED2, and ED3 may have a shape of a rod, wire, tube, etc., a shape of a polygonal column such as a cube, a cuboid, or a hexagonal column, or may have a shape extended in a direction with a partially inclined outer surface.

The first light-emitting diode ED1 may include a first semiconductor layer SEM1*b*, an electron blocking layer EBLb, an active layer MQW1, a superlattice layer SLTb, and a second semiconductor layer SEM2*b*. The first semiconductor layer SEM1*b*, the electron blocking layer EBLb, the active layer MQW1, the superlattice layer SLTb, and the second semiconductor layer SEM2*b* may be stacked on one another in order in the third direction DR3.

The second light-emitting diodes ED2 and/or the third light-emitting diodes ED3 may include a first semiconductor layer SEM1*a*, an electron blocking layer EBLa, active layers MQW2 and/or MQW3, a superlattice layer SLTa, and a second semiconductor layer SEM2*a*. The first semiconductor layer SEM1*a*, the electron blocking layer EBLa, the active layers MQW2 and/or MQW3, the superlattice layer SLTa, and the second semiconductor layer SEM2*a* may be stacked on one another in order in the third direction DR3.

The material of the first semiconductor layer SEM1*b* of the first light-emitting diode ED1 may be the same as the material of the first semiconductor layer SEM1*a* of the second light-emitting diode ED2 and/or the third light-emitting diode ED3. The material of the second semiconductor layer SEM2*b* of the first light-emitting diode ED1 may be the same as the material of the second semiconductor layer SEM2*a* of the second light-emitting diode ED2 and/or the third light-emitting diode ED3.

The first semiconductor layer SEM1*a* and SEM1*b* may include a p-type semiconductor, and may include a semiconductor material having the chemical formula $Al_xGa_yIn_{1-x-y}N$ ($0 \le x \le 1$, $0 \le y \le 1$, and $0 \le x+y \le 1$). For example, the first semiconductor layer SEM1*a* and SEM1*b* may be at least one of p-type doped AlGaInN, GaN, AlGaN, InGaN, AlN, and InN. The first semiconductor layers SEM1*a* and

SEM1*b* may be doped with a p-type dopant, and the p-type dopant may be Mg, Zn, Ca, Ba, etc. For example, the first semiconductor layers SEM1*a* and SEM1*b* may be p-GaN doped with p-type Mg.

The electron blocking layers EBLa and EBLb may be located on the first semiconductor layers SEM1*a* and SEM1*b*, respectively. The electron blocking layers EBLa and EBLb may reduce or prevent electrons flowing into the active layers MQW1, MQW2, and MQW3 that fail to recombine with holes in the active layers MQW1, MQW2, and MQW3 and that are then injected into other layers. For example, the electron blocking layers EBLa and EBLb may be p-AlGaN doped with p-type Mg. The thickness of the electron blocking layers EBLa and EBLb may be in a range of about 10 nm to about 50 nm, but the present disclosure is not limited thereto. In some embodiments, the electron blocking layers EBLa and EBLb may be omitted.

The active layers MQW1, MQW2, and MQW3 may be respectively located on the electron blocking layers EBLa and EBLb. The active layer MQW1, MQW2, and MQW3 may emit light as electrons and holes are recombined therein in response to an emission signal applied through the first semiconductor layers SEM1*a* and SEM1*b* and the second semiconductor layers SEM2*a* and SEM2*b*. The active layers MQW1, MQW2, and MQW3 may include a material having a single or multiple quantum well structure. When the active layers MQW1, MQW2, and MQW3 include a material having the multiple quantum well structure, well layers and barrier layers may be alternately stacked on one another in the structure. The well layers may be made of InGaN, and the barrier layers may be made of GaN or AlGaN, but the present disclosure is not limited thereto. For example, each of the active layers MQW1, MQW2, and MQW3 may have a structure in which a semiconductor material having a large band gap energy and a semiconductor material having a small band gap energy are alternately stacked on one another, and may include other Group III to Group V semiconductor materials depending on the wavelength range of the emitted light.

The superlattice layers SLTa and SLTb are located on the active layers MQW1, MQW2, and MQW3. The superlattice layers SLTa and SLTb may relieve stress due to a difference in lattice constants between the second semiconductor layers SEM2*a* and SEM2*b* and the active layers MQW1, MQW2, and MQW3. For example, the superlattice layers SLTa and SLTb may be made of InGaN or GaN. The thickness of the superlattice layers SLTa and SLTb may be about 50 nm to about 200 nm. It should be noted that the superlattice layers SLTa and SLTb may be omitted.

The second semiconductor layers SEM2*a* and SEM2*b* may be located on the superlattice layers SLTa and SLTb. The second semiconductor layers SEM2*a* and SEM2*b* may be n-type semiconductors. The second semiconductor layers SEM2*a* and SEM2*b* may include a semiconductor material having the chemical formula $Al_xGa_yIn_{1-x-y}N$ ($0 \le x \le 1$, $0 \le y \le 1$, and $0 \le x+y \le 1$). For example, it may be at least one of n-type doped AlGaInN, GaN, AlGaN, InGaN, AlN, and InN. The second semiconductor layers SEM2*a* and SEM2*b* may be doped with an n-type dopant, and the n-type dopant may be Si, Ge, Sn, etc. For example, the second semiconductor layers SEM2*a* and SEM2*b* may be n-GaN doped with n-type Si. The thickness of the second semiconductor layers SEM2*a* and SEM2*b* may range from about 2 μm to about 4 μm, but is not limited to.

According to some embodiments, some of the light-emitting diodes ED1, ED2, and ED3 of the display device **10** may include different active layers MQW1, MQW2, and MQW3 to emit light of different colors. For example, the first light-emitting diode ED1 may include a first active layer MQW1, the second light-emitting diode ED2 may include a second active layer MQW2, and the third light-emitting diode ED3 may include a third active layer MQW3. The first light-emitting diode ED1 may emit red light of a first color, the second light-emitting diode ED2 may emit green light of a second color, and the third light-emitting diode ED3 may emit blue light of a third color. The first light-emitting diode ED1, the second light-emitting diode ED2, and the third light-emitting diode ED3 may have different concentrations of dopants doped in the first semiconductor layers SEM1*a* and SEM1*b*, the electron blocking layers EBLa and EBLb, the active layers MQW1, MQW2, and MQW3, the superlattice layers SLTa and SLTb, and the second semiconductor layers SEM2*a* and SEM2*b*, or may have different values of x and yin the formula $Al_xGa_yIn_{1-x-y}N$ ($0 \le x \le 1$, $0 \le y \le 1$, and $0 \le x+y \le 1$). The first to third light-emitting diodes ED1, ED2, and ED3 may have substantially the same structure and material, but may include different component ratios at the semiconductor layers to emit lights of different colors.

For example, the first active layer MQW1 may emit light when electrons and holes are recombined therein in response to an electrical signal applied through the first semiconductor layer SEM1*b* and the second semiconductor layer SEM2*b*. The first active layer MQW1 may emit first light having a main peak wavelength in the range of about 600 nm to about 750 nm (e.g., light of the red wavelength range).

The second active layer MQW2 may emit light as electrons and holes are recombined therein in response to an electrical signal applied through the first semiconductor layer SEM1*a* and the second semiconductor layer SEM2*a*. The second active layer MQW2 may emit second light having a main peak wavelength in the range of about 480 nm to about 560 nm (e.g., light of the green wavelength range).

The third active layer MQW3 may emit light as electrons and holes are recombined therein in response to an electrical signal applied through the first semiconductor layer SEM1*a* and the second semiconductor layer SEM2*a*. The third active layer MQW3 may emit third light having a main peak wavelength in the range of about 370 nm to about 460 nm (e.g., light of the blue wavelength range).

In some embodiments in which each of the first active layer MQW1, the second active layer MQW2, and the third active layer MQW3 contains InGaN, they may emit lights of different colors depending on the content, or amount, of indium (In). For example, as the content of indium (In) increases, the wavelength range of light output from the first to third active layers MQW1, MQW2, and MQW3 may move to the red wavelength range, and as the content of indium (In) decreases, the wavelength range of the output light may move to the blue wavelength range. The content of indium (In) in the first active layer MQW1 may be greater than the content of indium (In) in the second active layer MQW2, and the content of indium (In) in the second active layer MQW2 may be greater than the content of indium (In) in the third active layer MQW3. For example, the content of indium (In) in the third active layer MQW3 may be 15%, the content of indium (In) in the second active layer MQW2 may be 25%, and the content of indium (In) in the first active layer MQW1 may be 35% or more.

Similarly, in some embodiments where the first semiconductor layers SEM1*a* and SEM1*b*, the second semiconductor layers SEM2*a* and SEM2*b*, the superlattice layers SLTa and SLTb, and the electron blocking layers EBLa and EBLb of the first to third light-emitting diodes ED1, ED2, and ED3 contain InGaN, they may have different contents of indium

(In). Like the first to third active layers MQW1, MQW2, and MQW3, the first semiconductor layers SEM1*a* and SEM1*b*, the second semiconductor layers SEM2*a* and SEM2*b*, the superlattice layers SLTa and SLTb, and the electron blocking layers EBLa and EBLb of the first to third light-emitting diodes ED1, ED2, and ED3 may have a higher or lower content of indium (In) than that of the other light-emitting diodes ED1, ED2, and ED3.

An insulating layer INS may surrounds side surfaces of the second light-emitting diode ED2 and/or the third light-emitting diode ED3, and a part of the insulating layer INS may be located on the first common electrode layer CEL1. The insulating layer INS may be located on the surface of the first common electrode layer CEL1 that faces the first substrate **110**, and may cover a part of the surface of the first semiconductor layer SEM1*a* in addition to the side surfaces of the second light-emitting diode ED2 and/or the third light-emitting diode ED3. A second connection electrode CNE2 may be located on a part of a surface of the second light-emitting diode ED2 and/or the third light-emitting diode ED3 where the insulating layer INS is not located (e.g., where a portion of the insulating layer INS is omitted). The second connection electrode CNE2 may connect the first semiconductor layer SEM1*a* with the pixel electrode AE. The surface of the first semiconductor layer SEM1*b* of the first light-emitting diode ED1 may be connected to the pixel electrode AE through a first connection electrode CNE1. The insulating layer INS may protect the plurality of light-emitting diodes ED1, ED2, and ED3, and may insulate them from other layers. The insulating layer INS may include an inorganic insulating material, such as silicon oxide (SiO_x), silicon nitride (SiN_x), silicon oxynitride ($Si_xO_yN_y$), aluminum oxide (AlO_y), and aluminum nitride (AlN_x).

A first reflective layer RL1 and a second reflective layer RL2 may be located on the insulating layer INS and may surround the side surfaces of the second light-emitting diode ED2 and/or the third light-emitting diode ED3. The first reflective layer RL1 and the second reflective layer RL2 might not be formed on parts of the insulating layer INS between the second light-emitting diodes ED2 and/or the third light-emitting diodes ED3. In the example shown in FIG. **4**, the first reflective layer RL1 may be located on the left side of the second light-emitting diode ED2 and/or the third light-emitting diode ED3, and the second reflective layer RL2 may be located on the right side of the second light-emitting diode ED2 and/or the third light emitting device ED3. Because the second connection electrode CNE2 directly connects the first semiconductor layer SEM1*a* with the pixel electrode AE, the reflective layers RL1 and RL2 and the insulating layer INS may be in contact with the side surfaces of the second connection electrode CNE2. The first reflective layer RL1 and the second reflective layer RL2 may include a metal material having high reflectance, such as aluminum (Al).

The connection electrodes CNE1 and CNE2 may be respectively located between the light-emitting diodes ED1, ED2, and ED3 and the first substrate **110**. The connection electrodes CNE1 and CNE2 may include the first connection electrode CNE1 located between the first light-emitting diode ED1 and the pixel electrode AE, and the second connection electrode CNE2 located between the second light-emitting diode ED2 and/or the third light-emitting diode ED3 and the pixel electrode AE.

The first connection electrodes CNE1 and the second connection electrodes CNE2 may be respectively located in line with the light-emitting diodes ED1, ED2, and ED3 and the pixel electrodes AE in the display area DA. The first connection electrodes CNE1 may be located on the surfaces of the first semiconductor layers SEM1*b* of the first light-emitting diodes ED1, while the second connection electrodes CNE2 may be located on the surfaces of the first semiconductor layers SEM1*a* of the second light-emitting diodes ED2 and/or the third light-emitting diodes ED3.

The connection electrodes CNE1 and CNE2 may be respectively electrically connected to the pixel electrode AE to transmit emission signals applied to the pixel electrodes AE to the light-emitting diodes ED1, ED2, and ED3. The connection electrodes CNE1 and CNE2 may be ohmic connection electrodes. It is, however, to be understood that the present disclosure is not limited thereto. The connection electrodes CNE1 and CNE2 may be Schottky connection electrodes. The width of the connection electrodes CNE1 and CNE2 may be less than the width of the light-emitting diodes ED1, ED2, and ED3. The second connection electrode CNE2 may be located on only a part of the surface of the first semiconductor layer SEM1*a*, and the insulating layer INS may be located on the other part.

In some embodiments, a sub-connection electrode may be further located between the connection electrodes CNE1 and CNE2 and the first semiconductor layers SEM1*a* and SEM1*b*. When the light-emitting diodes ED1, ED2, and ED3 are electrically connected to the connection electrodes CNE1 and CNE2, the sub-connection electrode may reduce the resistance by contact between the light-emitting diodes ED1, ED2, and ED3 and the connection electrodes CNE1 and CNE2.

The connection electrodes CNE1 and CNE2 may be located directly on the pixel electrodes AE and may be in contact with them. The connection electrodes CNE1 and CNE2 may work as bonding metals for bonding the pixel electrodes AE with the light-emitting diodes ED1, ED2, and ED3 during the fabricating process. The connection electrodes CNE1 and CNE2 may include a material that may be electrically connected to the pixel electrodes AE and the light-emitting diodes ED1, ED2, and ED3. For example, the connection electrodes CNE1 and CNE2 may include at least one of gold (Au), copper (Cu), aluminum (Al) and tin (Sn), or may include a transparent conductive oxide such as indium tin oxide (ITO) and indium zinc oxide (IZO). Alternatively, the connection electrodes CNE1 and CNE2 may include a first layer including one of gold (Au), copper (Cu), aluminum (Al), and tin (Sn), a second layer including another one of gold (Au), copper (Cu), aluminum (Al), and tin (Sn).

The display substrate **300** may include the first common electrode layer CEL1 connected to the second semiconductor layers SEM2*a* of the second light-emitting diodes ED2 and/or the third light-emitting diodes ED3 as a single common layer. The first common electrode layer CEL1 may be generally located throughout the entire surface of the display substrate **300**. The first common electrode layer CEL1 may include the same material as the second semiconductor layers SEM2*a* and SEM2*b*. The first common electrode layer CEL1 and the second semiconductor layer SEM2*a* may be integrally formed.

A first bonding layer BL1 may be located on the first common electrode layer CEL1. The first bonding layer BL1 may include a material bonded with a second bonding layer BL2 to be described later. Although not limited thereto, each of the first bonding layer BL1 and the second bonding layer BL2 may include at least one of gold (Au), copper (Cu),

aluminum (Al), and tin (Sn), or a transparent conductive oxide such as indium tin oxide (ITO) and indium zinc oxide (IZO).

The display substrate **300** may include a second substrate SUB facing the first substrate **110**. The second substrate SUB may be a transparent substrate. The second substrate SUB may include a sapphire substrate (Al_2O_3) or a transparent substrate such as glass. It is, however, to be understood that the present disclosure is not limited thereto. The second substrate SUB may be formed as a conductive substrate such as GaN, SiC, ZnO, Si, GaP, and GaAs. According to some embodiments of the present disclosure, the second substrate SUB may be a sapphire substrate (Al_2O_3).

A second common electrode layer CEL**2** may be located between the second substrate SUB and the first light-emitting diode ED**1**. The second common electrode layer CEL**2** may include the same material as the above-described first common electrode layer CEL**1**. The second common electrode layer CEL**2** may be located throughout the entire surface of the display substrate **300**. The second common electrode layer CEL**2** and the second semiconductor layer SEM**2***b* may be integrally formed. The second semiconductor layer SEM**2***b*, the superlattice layer SLTb, the first active layer MQW**1**, the electron blocking layer EBLb, and the first semiconductor layer SEM**1***b* may be arranged in this order downward in the third direction DR**3**. The second semiconductor layer SEM**2***b*, the superlattice layer SLTb, the first active layer MQW**1**, the electron blocking layer EBLb, and the first semiconductor layer SEM**1***b* form the first light-emitting diode ED**1** (see FIG. **3**).

A filling layer FM may be located on the first light-emitting diode ED**1** and on a surface of the second common electrode layer CEL**2**. The filling layer FM may be located on the surface of the second common electrode layer CEL**2** where the first light-emitting diode ED**1** is not located, the side surfaces of the first light-emitting diode ED**1**, and the upper surface of the first light-emitting diode ED**1**. The filling layer FM may include an inorganic insulating material or an organic insulating material. Examples of the inorganic insulating material include, but are not limited to, an insulating material such as silicon oxide (SiO_x), silicon nitride (SiN_x), and silicon oxynitride (SiO_xN_y). Examples of the organic insulating material may include, but are not limited to, polyimide (PI).

The second bonding layer BL**2** may be located between the filling layer FM and the first bonding layer BL**1**. As described above, the second bonding layer BL**2** may be bonded with the first bonding layer BL**2**. As shown in FIG. **4**, the first connection electrode CNE**1** may be connected to the pixel electrode AE through the filling layer FM, the bonding layers BL**1** and BL**2**, the first common electrode layer CEL**1**, the insulating layer INS, and the reflective layers RL**1** and RL**2**. In other words, the first connection electrodes CNE**1** may be longer than the second connection electrodes CNE**2** connected to the pixel electrodes AE through only the insulating layer INS and the reflective layer RL**1**/RL**2** in the thickness direction.

Incidentally, when the active layers MQW**1**, MQW**2**, and MQW**3** of the light-emitting diodes ED**1**, ED**2**, and ED**3** are made of InGaN, the internal quantum efficiency (IQE) may decrease at a high current density when the first active layer MQW**1** emits red light, which is the first light. Accordingly, to lower the current density in the first active layer MQW**1**, it may be suitable that the area of the first active layer MQW**1** is greater than the areas of the second and third active layers MQW**2** and/or MQW**3**. If the first to third light-emitting diodes ED**1**, ED**2**, and ED**3** are located on the same layer, it may be difficult to increase the area of the first active layer MQW**1** of the first light-emitting diodes ED**1** in the given area. In contrast, according to some embodiments of the present disclosure, the layer on which the first light-emitting diodes ED**1** including the first active layer MQW**1** are located is different from the layer on which the second light-emitting diodes ED**2** and the third light-emitting diodes ED**3** are located, and thus it may be suitable to increase the area (or width) of the first active layer MQW**1**.

The layer on which the first light-emitting diodes ED**1** including the first active layer MQW**1** are located is different from the layer on which the second light-emitting diodes ED**2** and/or the third light-emitting diodes ED**3** are located, and thus the width W**1** of the first light-emitting diodes ED**1** may be greater than the respective widths W**2** and/or W**3** of the second light-emitting diodes ED**2** and/or the third light-emitting diodes ED**3** by utilizing the additional area, it is possible to lower the current density of the first active layer MQW**1**. As a result, it is possible to reduce or prevent a decrease in the internal quantum efficiency (IQE).

Hereinafter, processing operations of fabricating the display device **10** will be described with reference to other drawings.

FIG. **6** is a flowchart for illustrating a method for fabricating a display device according to some embodiments of the present disclosure. FIGS. **7** to **25** are cross-sectional views illustrating processing operations of a method of fabricating a display device according to some embodiments of the present disclosure.

Referring to FIG. **6**, a method of fabricating a display device **10** according to some embodiments of the present disclosure may include: forming a first light-emitting diode for emitting a first light on a first support substrate (S**10**); forming a second bonding layer above the first light-emitting diode (S**20**); forming a first bonding layer on a surface of a second support substrate (S**30**); forming a second light-emitting diode for emitting a second light and a third light-emitting diode for emitting a third light on the first bonding layer (S**40**); delaminating the second support substrate from the first bonding layer (S**50**); and bonding the first bonding layer with the second bonding layer. (S**60**)

In FIG. **6**, the first support substrate may be the second substrate SUB of FIG. **4**, and the second support substrate may be the first substrate **110** of FIG. **4**.

Hereinafter, a method of fabricating the display device **10** according to some embodiments will be described in more detail with reference to FIGS. **6** to **25**.

Initially, referring to FIGS. **6** and **7**, the second common electrode layer CEL**2** is formed on the second substrate SUB. As described above with reference to FIG. **4**, the second common electrode layer CEL**2** may include the same material as the second semiconductor layers SEM**2***a* and SEM**2***b*. The second common electrode layer CEL**2** may be formed by epitaxial growth. The epitaxial growth may be carried out by electron beam deposition, physical vapor deposition (PVD), chemical vapor deposition (CVD), plasma laser deposition (PLD), dual-type thermal evaporation, sputtering, metal-organic chemical vapor deposition (MOCVD), etc. For example, the epitaxial growth may be carried out by, but is not limited to, metal-organic chemical vapor deposition (MOCVD). The first common electrode layer CEL**1** and the second semiconductor layers SEM**2***a* and SEM**2***b*, which will be described later, may also be formed by epitaxial growth.

Subsequently, referring to FIG. **8**, a support layer SPL is formed on the second common electrode layer CEL**2**. The

support layer SPL may be located entirely on the second common electrode layer CEL2. The support layer SPL may include an insulating material, such as silicon oxide (SiO_x), silicon nitride (SiN_x), and silicon oxynitride (SiO_xN_y), and may work as a mask for a process for forming light-emitting diodes.

Subsequently, referring to FIG. **9**, holes H1 penetrating through the support layer SPL are formed. Thereafter, first light-emitting diodes ED1 are formed in the holes H1. The holes H1 may be formed by etching.

Subsequently, referring to FIGS. **6** and **10**, the first light-emitting diodes ED1 are formed in the plurality of holes H1 (S10). The structure of the first light-emitting diodes ED1 have been described above with reference to FIGS. **4** and **5**. Therefore, redundant descriptions thereof will be omitted.

Subsequently, referring to FIG. **11**, the support layer SPL is removed.

Subsequently, referring to FIG. **12**, the filling layer FM used to fill areas adjacent the upper surface and the side surfaces of the first light-emitting diodes ED1 is formed or shaped. The filling layer FM is used to fill the space between the first light-emitting diodes ED1 and a space over the surfaces (or the upper surfaces, which are depicted as the lower surfaces in FIG. **4**) of the first light-emitting diodes ED1 to provide a flat surface. The material of the filling layer FM include, but are not limited to, an insulating material such as silicon oxide (SiO_x), silicon nitride (SiN_x), and silicon oxynitride (SiO_xN_y).

Subsequently, referring to FIGS. **6** and **13**, the second bonding layer BL2 is formed entirely on the filling layer FM (S20). The second bonding layer BL2 may include a material to be bonded with the first bonding layer BL1 to be described later. Each of the first bonding layer BL1 and the second bonding layer BL2 may include at least one of gold (Au), copper (Cu), aluminum (Al), and tin (Sn), or a transparent conductive oxide such as indium tin oxide (ITO) and indium zinc oxide (IZO).

Subsequently, referring to FIGS. **6** and **14**, a preliminary substrate SUB_1 is prepared, on which the first bonding layer BL1 (S30), and the first common electrode layer CEL1 on the first bonding layer BL1, are located. (S30) Subsequently, a support layer SPL is formed on the first common electrode layer CEL1. The support layer SPL may be located entirely on the first common electrode layer CEL1. The support layer SPL may include an insulating material such as silicon oxide (SiO_x), silicon nitride (SiN_x), and silicon oxynitride (SiO_xN_y), and may work as a mask for a process for forming semiconductor elements. As described above with reference to FIG. **4**, the first common electrode layer CEL1 may include the same material as the second semiconductor layers SEM2*a* and SEM2*b*. The first common electrode layer CEL1 may be formed by epitaxial growth.

Subsequently, referring to FIG. **15**, holes H2 and H3 penetrating through the support layer SPL are formed. Thereafter, second light-emitting diodes ED2 and third light-emitting diodes ED3 are formed in the holes H2 and H3. The holes H2 and H3 may be formed by etching.

Subsequently, referring to FIGS. **6** and **16**, the second light-emitting diodes ED2 and the third light-emitting diodes ED3 are respectively formed in the plurality of holes H2 and H3 (S40). The structure of the second light-emitting diodes ED2 and the third light-emitting diodes ED3 have been described above with reference to FIGS. **4** and **5**. Therefore, redundant descriptions thereof will be omitted.

Subsequently, referring to FIG. **17**, the support layer SPL is removed.

Subsequently, referring to FIG. **18**, an insulating layer INS' is formed entirely on the side surfaces of the second light-emitting diode ED2 and the third light-emitting diode ED3 and on the first common electrode layer CEL1. The insulating layer INS' may be formed directly on the side surfaces of the second light-emitting diodes ED2 and the third light-emitting diodes ED3, and on parts of the surface of the first common electrode layer CEL1 where the second light-emitting diodes ED2 and the third light-emitting diodes ED3 are not located. The insulating layer INS' may include an inorganic insulating material such as silicon oxide (SiO_x), silicon nitride (SiN_x), silicon oxynitride (SiO_xN_y), aluminum oxide (AlO_y), and aluminum nitride (AlN_x).

Subsequently, referring to FIG. **19**, a reflective layer RL is formed. The reflective layer RL might not be formed above parts of the first common electrode layer CEL1 located between the second light-emitting diodes ED2 and the third light-emitting diodes ED3 in a plan view. The reflective layer RL may include a metal material having high reflectivity, such as aluminum (Al).

Subsequently, referring to FIG. **20**, the preliminary substrate SUB_1 is delaminated from the first bonding layer BL1 (S50). The first bonding layer BL1 is exposed after the preliminary substrate SUB_1 has been delaminated.

Subsequently, as shown in FIG. **21**, the first bonding layer BL1 and the second bonding layer BL2 are bonded with each other (S60). As described above, each of the first bonding layer BL1 and the second bonding layer BL2 may include at least one of gold (Au), copper (Cu), aluminum (Al) and tin (Sn), or a transparent conductive oxide such as indium tin oxide (ITO), and indium zinc oxide (IZO).

Subsequently, as shown in FIG. **22**, fourth to sixth holes H4 to H6 are formed. As shown in FIG. **22**, the fourth hole H4 penetrates the insulating layer INS, the first common electrode layer CEL1, the bonding layers BL1 and BL2, and the filling layer FM, and exposes one surface of the first semiconductor layer SEM1*b*. The fifth and sixth holes H5 and H6 penetrate the reflective layer RL and the insulating layer INS, and exposes one surface of the first semiconductor layer SEM1*a*. The fourth to sixth holes H4 to H6 may be formed by etching.

Subsequently, as shown in FIG. **23**, the first and second connection electrodes CNE1 and CNE2 are formed. The connection electrodes CNE1 and CNE2 may include the first connection electrodes CNE1 on the first light-emitting diodes ED1, and the second connection electrodes CNE2 formed on the second light-emitting diodes ED2 and/or the third light-emitting diodes ED3.

The first connection electrodes CNE1 and the second connection electrodes CNE2 may be respectively located in line with the light-emitting diodes ED1, ED2, and ED3 and pixel electrodes AE to be described later in the display area DA. The first connection electrodes CNE1 may be located on the surfaces of the first semiconductor layers SEM1*b* of the first light-emitting diodes ED1, and the second connection electrodes CNE2 may be located on the surfaces of the first semiconductor layers SEM1*a* of the second light-emitting diodes ED2 and/or the third light-emitting diodes ED3.

The connection electrodes CNE1 and CNE2 may be electrically connected to respective pixel electrodes AE to transmit emission signals, which are applied to the pixel electrodes AE, to the light-emitting diodes ED1, ED2, and ED3. The connection electrodes CNE1 and CNE2 may be ohmic connection electrodes. It is, however, to be understood that the present disclosure is not limited thereto. The

connection electrodes CNE1 and CNE2 may be Schottky connection electrodes. The width of the connection electrodes CNE1 and CNE2 may be less than the width of the light-emitting diodes ED1, ED2, and ED3. The second connection electrode CNE2 may be located on only a part of the surface of the first semiconductor layer SEM1*a*, and the insulating layer INS may be located on the other part.

The connection electrodes CNE1 and CNE2 may be located directly on the pixel electrodes AE and may be in contact with them. The connection electrodes CNE1 and CNE2 may work as bonding metals for bonding the pixel electrodes AE with the light-emitting diodes ED1, ED2, and ED3 during the fabricating process. The connection electrodes CNE1 and CNE2 may include a material that may be electrically connected to the pixel electrodes AE and the light-emitting diodes ED1, ED2, and ED3. For example, the connection electrodes CNE1 and CNE2 may include at least one of gold (Au), copper (Cu), aluminum (Al), and tin (Sn), or may include a transparent conductive oxide such as indium tin oxide (ITO) and indium zinc oxide (IZO). Alternatively, the connection electrodes CNE1 and CNE2 may include a first layer including one of gold (Au), copper (Cu), aluminum (Al), and tin (Sn), a second layer including another one of gold (Au), copper (Cu), aluminum (Al), and tin (Sn). In addition, the first connection electrodes CNE1 may be connected to the pixel electrodes AE through the filling layer FM, the bonding layers BL1 and BL2, the first common electrode layer CEL1, the insulating layer INS, and the reflective layer RL. In other words, the first connection electrodes CNE1 may be longer than the second connection electrodes CNE2 that are connected to the pixel electrodes AE through only the insulating layer INS and the reflective layer RL in the thickness direction.

Subsequently, referring to FIGS. **24** and **25**, the pixel electrodes AE and the connection electrodes CNE1 and CNE2 are placed such that they face each other on the first substrate **110**, and then the pixel electrodes AE and the connection electrodes CNE1 and CNE2 are connected with each other, respectively.

Hereinafter, other embodiments of the present disclosure will be described.

FIG. **26** is a plan view showing a layout of first to third light-emitting diodes according to other embodiments. FIG. **27** is a cross-sectional view showing the display panel, taken along the line Q2-Q2' of FIG. **26**.

The embodiments corresponding to FIGS. **26** and **27** are different from the embodiments corresponding to FIGS. **3** and **4** in that a first light-emitting diode ED1 covers, or overlaps, only a part of a second light-emitting diode ED2 and/or a third light-emitting diode ED3 when viewed from the top/in a plan view.

The display panel according to the present described embodiments is different from the display panel of FIG. **4** in that a width W1_1 of the first light-emitting diode ED1 is greater than widths W2 and W3 of a second light-emitting diodes ED2 and/or a third light-emitting diode ED3, and that the first light-emitting diode ED1 partially covers the second light-emitting diodes ED2 and/or the third light-emitting diode ED3 (e.g., does not completely cover) when viewed from the top.

The other elements are identical to those described above with reference to FIG. **4**. Therefore, redundant description thereof will be omitted.

FIG. **28** is a plan view showing a layout of first to third light-emitting diodes according to other embodiments.

A pixel PX_1 according to the embodiments corresponding to FIG. **28** is different from the pixel PX of FIG. **3** in that the first to third light-emitting diodes ED1, ED2, and ED3 are arranged in a PenTile™ matrix (e.g., a PENTILE™ matrix structure, a PENTILE™ structure, or an RGBG matrix/structure). PENTILE™ is a registered trademark of Samsung Display Co., Ltd., Republic of Korea.

For example, the first light-emitting diode ED1 of one pixel PX_1 may overlap four second light-emitting diodes ED2 while not overlapping any third light-emitting diode ED3 when viewed from the top. A third light-emitting diode ED3 of a particular pixel PX_1 may be located between a first light-emitting diode ED1 of an adjacent pixel PX_1 on a side of (e.g., on the left side of) the particular pixel PX_1 and a first light-emitting diode ED1 of the particular pixel PX_1. Furthermore, the third light-emitting diode ED3 may be located between a first light-emitting diode ED1 of a pixel PX_1 on the upper left side of the first light-emitting diode ED1 of the particular pixel PX_1, and a first light-emitting diode ED1 of a pixel PX_1 on the lower left side of the first light-emitting diode ED1 of the particular pixel PX_1. The plurality of pixels PX_1 may be arranged in a zigzag pattern in the horizontal direction, and rows of the pixels arranged in the zigzag pattern may be spaced apart from one another by a distance (e.g., a predetermined distance) in the vertical direction.

FIG. **29** is an equivalent circuit diagram of a pixel of a display device according to some embodiments of the present disclosure. FIG. **29** shows an example of a pixel circuit diagram included in one pixel PX of FIG. **3**.

Referring to FIG. **29**, the light-emitting diodes ED1, ED2, and ED3 emit light in response to the driving current. The amount of the light emitted from the light-emitting diodes ED1, ED2, and ED3 may be proportional to the driving current. Each of the light-emitting diodes ED1, ED2, and ED3 may be an inorganic light-emitting element including an anode electrode, a cathode electrode, and an inorganic semiconductor located between the anode electrode and the cathode electrode.

The anode electrode of the light-emitting diodes ED1, ED2, and ED3 may be connected to the source electrode of a driving transistor DT, and the cathode electrode may be connected to a second supply voltage line VSL from which a low-level voltage, which is lower than the high-level voltage, is applied.

The driving transistor DT adjusts a current flowing from a first supply voltage line VDL, from which the first supply voltage is supplied, to the light-emitting diodes ED1, ED2, and ED3 according to the voltage difference between the gate electrode and the source electrode of the driving transistor DT. The gate electrode of the driving transistor DT may be connected to a first electrode of a first transistor ST1, the source electrode thereof may be connected to the anode electrode of the light-emitting diodes ED1, ED2, and ED3, and the drain electrode thereof may be connected to the first supply voltage line VDL to which a high-level voltage is applied.

The first transistor ST1 is turned on by a first scan signal of a first scan line SCL1 to connect a data line DL with the gate electrode of the driving transistor DT. The gate electrode of the first transistor ST1 may be connected to the first scan line SCL1, the first electrode thereof may be connected to the gate electrode of the driving transistor DT, and the second electrode thereof may be connected to the data line DL.

The second transistor ST2 is turned on by a second scan signal of a second scan line SCL2 to connect an initialization voltage line VIL with the source electrode of the driving transistor DT. The gate electrode of the second transistor

ST2 may be connected to the second scan line SCL2, the first electrode thereof may be connected to the initialization voltage line VIL, and the second electrode thereof may be connected to the source electrode of the driving transistor DT.

The first electrode of each of the first and second transistors ST1 and ST2 may be a source electrode, and the second electrode may be a drain electrode, but the present disclosure is not limited thereto. That is to say, the first electrode of each of the first and second transistors ST1 and ST2 may be a drain electrode, and the second electrode thereof may be a source electrode.

The capacitor Cst may be formed between the gate electrode and the source electrode of the driving transistor DT. The capacitor Cst stores the voltage equal to the difference between the gate voltage and the source voltage of the driving transistor DT.

Although FIG. **29** shows that each of the driving transistor DT and the first and second transistors ST1 and ST2 is implemented as an n-type MOSFET (metal oxide semiconductor field effect transistor), it is to be noted that the present disclosure is not limited thereto. Each of the driving transistor DT and the first and second transistors ST1 and ST2 may be implemented as a p-type MOSFET.

It should be noted that the display device for displaying an image according to some embodiments may be applied to various apparatuses and devices.

FIG. **30** shows a virtual reality device **1** to which the display device **10** according to some embodiments is applied. FIG. **31** shows a smart watch **2** to which the display device **10** according to some embodiments is applied. FIG. **32** shows a vehicle in which display devices **10**_*a*, **10**_*b*, **10**_*c*, **10**_*d* and **10**_*e* according to some embodiments are applied as displays.

Referring to FIG. **30**, the virtual reality device **1** according to some embodiments may be a device in the form of glasses. The virtual reality device **1** according to some embodiments of the present disclosure may include a display device **10_1**, a left eye lens **10***a*, a right eye lens **10***b*, a support frame **20**, eyeglass temples **30***a* and **30***b*, a reflective member **40**, and a display device case **50**. Although the virtual reality device **1** including the eyeglass temples **30***a* and **30***b* is shown in the drawing, a head mounted display with a head strap, instead of the eyeglass temples **30***a* and **30***b*, may be employed as the virtual reality device **1** according to some embodiments of the present disclosure. It is to be understood that the virtual reality device **1** is not limited to that shown in the drawings but may be applied in a variety of electronic devices in a variety of forms.

The display device case **50** may include the display device **10_1** and the reflective member **40**. An image displayed on the display device **10_1** may be reflected by the reflective member **40** and provided to the user's right eye through the right eye lens **10***b*. Accordingly, the user may watch a virtual reality image displayed on the display device **10_1** through the right eye.

Although the display device case **50** may be located at the right end of the support frame **20**, the embodiments of the present disclosure are not limited thereto. For example, the display device case **50** may be located at the left end of the support frame **20**. In such case, an image displayed on the display device **10_1** is reflected by the reflective member **40** and provided to the user's left eye through the left eye lens **10***a*. Accordingly, the user may watch a virtual reality image displayed on the display device **10_1** through the left eye. Alternatively, the display device cases **50** may be located at both the left and right ends of the support frame **20**, respectively. In such case, the user may watch a virtual reality image displayed on the display device **10_1** through both the left and right eyes.

Referring to FIG. **31**, a display device **10_2** according to some embodiments may be applied to a smart watch **2** that is one of smart devices.

Referring to FIG. **32**, display devices **10**_*a*, **10**_*b* and **10**_*c* according to some embodiments of the present disclosure may be applied to the instrument cluster of a vehicle, may be applied to the center fascia of a vehicle, or may be applied to a center information display (CID) located on the dashboard of a vehicle. In addition, the display devices **10**_*d* and **10**_*e* according to some embodiments of the present disclosure may be applied to room mirror displays, which may replace side mirrors of the vehicle.

FIGS. **33** and **34** are views showing an example of a transparent display device including a display device according to some embodiments.

Referring to FIGS. **33** and **34**, a display device **10_3** according to some embodiments may be applied to a transparent display device. The transparent display device may transmit light while displaying images IM. A user located on the front side of the transparent display device may not only watch the images IM displayed on the display device **10_3** but also watch an object RS or the background located on the rear side of the transparent display device.

Although embodiments of the invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims, with functional equivalents thereof to be included therein.

What is claimed is:

1. A display device comprising:

light-emitting elements arranged on a circuit board comprising pixel electrodes, and extending in a thickness direction of the circuit board, wherein the light-emitting elements comprise:

a first light-emitting element configured to emit a first light;

a second light-emitting element configured to emit a second light; and

a first semiconductor layer,

wherein the first semiconductor layer of each of the light-emitting elements is connected to a respective one of the pixel electrodes; and

connection electrodes respectively between the first semiconductor layers of the light-emitting elements and the pixel electrodes,

wherein the first light-emitting element and the second light-emitting element are on different layers,

wherein a width of the first light-emitting element is greater than a width of the second light-emitting element, and

wherein a length of the connection electrode corresponding to the first light-emitting element is greater than a length of the connection electrode corresponding to the second light-emitting element.

2. The display device of claim **1**, wherein the light-emitting elements further comprise a third light-emitting element configured to emit a third light, and on a different layer from the first light-emitting element.

3. The display device of claim **2**, wherein the third light-emitting element is on a same layer as the second light-emitting element.

4. The display device of claim 3, wherein the width of the first light-emitting element is greater than a width of the third light-emitting element.

5. The display device of claim 3, wherein the first light-emitting element overlaps the second light-emitting element and the third light-emitting element in a plan view.

6. The display device of claim 5, wherein the first light-emitting element completely covers the second light-emitting element and the third light-emitting element in the plan view.

7. The display device of claim 1, wherein the light-emitting elements each further comprise:

an active layer on the first semiconductor layer; and

a second semiconductor layer on the active layer.

8. The display device of claim 7, wherein the light-emitting elements further comprise:

an electron blocking layer between the first semiconductor layer and the active layer; and

a superlattice layer between the active layer and the second semiconductor layer.

9. The display device of claim 7, further comprising a first common electrode layer between the second semiconductor layer of the second light-emitting element and the first semiconductor layer of the first light-emitting element.

10. The display device of claim 9, further comprising:

a first bonding layer between the first common electrode layer and the first semiconductor layer of the first light-emitting element; and

a second bonding layer between the first bonding layer and the first semiconductor layer of the first light-emitting element, and in direct contact with the first bonding layer.

11. The display device of claim 10, wherein the connection electrode corresponding to the first light-emitting element penetrates through the first bonding layer, the second bonding layer, and the first common electrode layer.

12. A method of fabricating a display device, the method comprising:

forming a first light-emitting element configured to emit a first light on a first substrate;

forming a first bonding layer above the first light-emitting element;

forming a second bonding layer on a surface of a second substrate;

forming a second light-emitting element configured to emit a second light, and a third light-emitting element configured to emit a third light, on the second bonding layer;

delaminating the second substrate from the second bonding layer; and

bonding the first bonding layer with the second bonding layer;

wherein a width of the first light-emitting element is greater than a width of the second light-emitting element and greater than a width of the third light-emitting element, and

wherein the first light-emitting element overlaps the second light-emitting element and the third light-emitting element in a plan view.

13. The method of claim 12, wherein each of the light-emitting elements comprises:

a first semiconductor layer on a circuit board;

an active layer on the first semiconductor layer; and

a second semiconductor layer on the active layer.

14. The method of claim 13, further comprising connecting pixel electrodes of the circuit board with the light-emitting elements, respectively, after bonding the first bonding layer with the second bonding layer.

15. The method of claim 14, further comprising forming connection electrodes respectively between the first semiconductor layers of the light-emitting elements and the pixel electrodes, after bonding the first bonding layer with the second bonding layer and before connecting pixel electrodes of the circuit board with the light-emitting elements, respectively.

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