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United States Patent Application Publication	20250259913
Kind Code	A1
Publication Date	August 14, 2025
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SEMICONDUCTOR PACKAGE HAVING COMPOSITE SEED-BARRIER LAYER AND METHOD OF FORMING THE SAME

Abstract

A semiconductor package includes a substrate, a composite seed-barrier layer, a routing via, and a semiconductor die. The substrate has a through hole formed therethrough. The composite seed-barrier layer extends on sidewalls of the through hole and includes a first barrier layer, a seed layer, and a second barrier layer sequentially stacked on the sidewalls of the through hole. The routing via fills the through hole and is separated from the substrate by the composite seed-barrier layer. The semiconductor die is electrically connected to the routing via. Along the sidewalls of the through holes, at a level height corresponding to half of a total thickness of the substrate, the seed layer is present as inclusions of seed material surrounded by barrier material of the first barrier layer and the second barrier layer.

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Appl. No.: **19/192276**

Filed: **April 28, 2025**

Related U.S. Application Data

parent US continuation 18482006 20231005 parent-grant-document US 12322682 child US 19192276
parent US continuation 17458610 20210827 parent-grant-document US 11823981 child US 18482006

Publication Classification

Int. Cl.: **H01L23/48** (20060101); **H01L21/285** (20060101); **H01L21/768** (20060101); **H01L23/31** (20060101)

U.S. Cl.:

CPC **H01L23/481** (20130101); **H01L21/2855** (20130101); **H01L21/76879** (20130101); **H01L23/3157** (20130101);

Background/Summary

CROSS-REFERENCE TO RELATED APPLICATION [0001] This application is a continuation application of and claims the priority benefit of a prior application Ser. No. 18/482,006, filed on Oct. 5, 2023, now allowed. The prior application Ser. No. 18/482,006 is a continuation application of and claims the priority benefit of a prior application Ser. No. 17/458,610, filed on Aug. 27, 2021, now patented. The entirety of the above-mentioned patent application is hereby incorporated by reference herein and made a part of this specification.

BACKGROUND
[0002] Semiconductor devices and integrated circuits used in a variety of electronic apparatus, such as cell phones and other mobile electronic equipment, are typically manufactured on a single semiconductor wafer. The dies of the wafer may be processed and packaged with other semiconductor devices or dies at the wafer level, and various technologies and applications have been developed for wafer level packaging. Integration of multiple semiconductor devices has become a challenge in the field.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0003] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.
[0004] FIG. **1** is a schematic flow chart illustrating some steps of a manufacturing method of a semiconductor package according to some embodiments of the disclosure.
[0005] FIG. **2**A to FIG. **2**T are schematic cross-sectional views illustrating structures formed during a manufacturing process of a semiconductor package according to some embodiments of the disclosure.
[0006] FIG. **3** is a schematic cross-sectional view of a semiconductor package according to some embodiments of the disclosure.
[0007] FIG. **4** is a schematic flow chart illustrating some steps of a manufacturing method of a semiconductor package according to some embodiments of the disclosure.
[0008] FIG. **5**A to FIG. **5**L are schematic cross-sectional views illustrating structures formed during a manufacturing process of a semiconductor package according to some embodiments of the disclosure.
[0009] FIG. **6** is a schematic flow chart illustrating some steps of a manufacturing method of a semiconductor package according to some embodiments of the disclosure.

[0010] FIG. **7**A to FIG. **7**H are schematic cross-sectional views illustrating structures formed during a manufacturing process of a semiconductor package according to some embodiments of the disclosure.

DETAILED DESCRIPTION

[0011] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0012] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper” and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0013] Other features and processes may also be included. For example, testing structures may be included to aid in the verification testing of the 3D packaging or 3DIC devices. The testing structures may include, for example, test pads formed in a redistribution layer or on a substrate that allows the testing of the 3D packaging or 3DIC, the use of probes and/or probe cards, and the like. The verification testing may be performed on intermediate structures as well as the final structure. Additionally, the structures and methods disclosed herein may be used in conjunction with testing methodologies that incorporate intermediate verification of known good dies to increase the yield and decrease costs.

[0014] FIG. **1** is a schematic flow chart illustrating some steps of a manufacturing method of a semiconductor package SP**10** according to some embodiments of the disclosure. FIG. **2**A to FIG. **2**T are schematic cross-sectional views illustrating structures formed during a manufacturing process of the semiconductor package SP**10** according to some embodiments of the disclosure. In FIG. **2**A, a substrate **200** (e.g., an interposer) is provided. In some embodiments, the substrate **200** is a wafer of an inorganic material. For example, the substrate **200** may be a wafer including a ceramic material. Examples of ceramic materials include metal oxides such as binary oxides (e.g., silicon oxide, barium oxide, aluminum oxide, zirconium oxide, beryllium oxide, zinc oxide, neodymium oxide, etc.) as well as ternary or higher oxides (e.g., titanates, aluminates, silicates, doped metal oxides, etc.), nitrides (e.g., silicon nitride, aluminum nitride, etc.), carbides (e.g., silicon carbides), etc. These materials may be used alone, or in combinations of two or more. In some embodiments, the substrate **200** includes aluminum nitride.

[0015] In some embodiments, through holes **210** are formed in the substrate **200**, extending all the way from the frontside surface **200***f* of the substrate **200** to the opposite backside surface **200***b*, for the entire thickness T**200** of the substrate **200**. In some embodiments, the through holes **210** are formed by laser drilling. For example, the material of the substrate **200** may be ablated by firing a laser towards the substrate **200** in the intended locations of the through holes **210** from the side of the frontside surface **200***f*. This may result in the through holes **210** having tapered sidewalls **210***s*, so that a width W**210***f* of the through holes **210** at the frontside surface **200***f* of the substrate **200** is greater than a width W**210***b* of the through holes **210** at the backside surface **200***b* of the substrate

200. Alternatively stated, the through holes **210** may become narrower proceeding from the frontside surface **200***f* towards the backside surface **200***b* along the thickness direction of the substrate **200**. The tapering angle α defined by the frontside surface **200***f* of the substrate **200** and the sidewalls **210***s* of the through holes **210** may be greater than 90 degrees, for example in the range between 90 degrees and 120 degrees.

[0016] In FIG. **2**B, a backside film **220** is bonded to the backside surface **200***b* of the substrate (step S**110** in FIG. **1**). The backside film **220** may be or include an organic material, such as an adhesive tape, an organic polymer (e.g., polyimide, epoxy, etc.), a dry photoresist or the like, which is disposed on the substrate **200**. In some embodiments, the backside film **220** may include fillers. For example, the backside film may include an epoxy resin with fillers dispersed therein. In some alternative embodiments, the backside film **220** may be a carrier (e.g., a glass carrier) which is removably attached to the substrate **200**, for example via a de-bonding layer. In some embodiments, the backside film **220** may be removed, when required, via suitable removal processes such as by irradiation of the de-bonding layer (e.g., in case of LTHC materials), etching (e.g., plasma etching, chemical etching, etc.) or the like. The backside film **220** may cover most or all of the backside surface **200***b*. Most notably, the backside film **220** extends at the bottom of the through holes **210**, so that the through holes **210** are plugged at the side of the backside surface **200***b*. That is, the through holes **210** may in fact appear as blind holes by way of the backside film **220**.

[0017] In some embodiments, the substrate **200** with the backside film **220** bonded thereto is introduced in a sputtering chamber to perform a sputtering process from the side of the frontside surface **200***f* (step S**120** in FIG. **1**). In some embodiments, the sputtering process S**120** includes a surface preparation step S**122**, a barrier layer sputtering step S**124** and a seed layer sputtering step S**126**. In the preparation step S**122**, the frontside surface **200***f* and the sidewalls **210***s* of the through holes **210** are pre-treated for subsequent material deposition. In some embodiments, a cleaning step, for example via plasma treatment, is performed to remove impurities which may have deposited or otherwise formed on the frontside surface **200***f* and the sidewalls **210***s*. After cleaning, the sputtering chamber may be brought to the target temperature and pressure for the subsequent sputtering operations.

[0018] In FIG. **2**C, the material of a frontside barrier layer **230** is sputtered on the frontside surface **200***f* of the substrate **200** and the sidewalls **210***s* of the through holes **210** (step S**124** in FIG. **1**). For example, one or more sputtering targets **240** are hit with high energy incident atoms or ions **242** to eject sputtered material **244** which is then deposited on the substrate **200**. In some embodiments, the pressure of the sputtering chamber and the energy of the incident atoms or ions **242** are selected so that the mean free path of the sputtered material **244** is sufficiently long to form the frontside barrier layer **230** also on the backside film **220** at the bottom of the through holes **210**. It should be noted that while a single target **240** is illustrated in FIG. **2**C, the disclosure is not limited thereto. For example, depending on the desired composition of the frontside barrier layer **230**, multiple sputtering targets **240** may be used. In some embodiments, the frontside barrier layer **230** includes a metallic material, such as titanium, tantalum, a nitride thereof, or a combination thereof. In some embodiments, the frontside barrier layer **230** is a titanium-containing layer, including a titanium-based material such as titanium, titanium nitride, or a combination thereof. In some embodiments, the frontside barrier layer **230** is a tantalum-containing layer, including a tantalum-based material such as tantalum, tantalum nitride, or a combination thereof.

[0019] In some embodiments, the sputtered material **244** reaches the substrate **200** from the side of the frontside surface **200***f*. The resulting frontside barrier layer **230** may thus include sections **232** extending on the frontside surface **200***f* of the substrate **200**, sections **234** extending on the sidewalls **210***s* of the through holes **210**, and sections **236** extending at the bottom of the through holes **210** on the frontside surface **220***f* of the backside film **220**. In some embodiments, the thicknesses T**232**, T**234**, T**236** of the individual sections **232**, **234**, **236** of the frontside barrier layer

230 may become increasingly smaller proceeding from the frontside surface **200***f* to the backside surface **200***b*. The thicknesses T**232**, T**234**, T**236** may be measured along directions normal to the surfaces **200***f*, **210***s*, **220***f* on which the corresponding sections **232**, **234**, **236** of the frontside barrier layer **230** extend. So, for example, the thicknesses T**232**, T**236** may be measured along a direction normal to the frontside surface **200***f*, and the thickness T**234** may be measured along a direction normal to the sidewalls **210***s*. The sections **232** located on the frontside surface **200***f* may have a substantially constant thickness T**232** and the sections **234** located on the sidewalls **210***s* of the through holes **210** may have a decreasing thickness T**234** proceeding towards the backside surface **200***b*. The sections **236** at the bottom of the through holes **210** may have a thickness T**236** comparable to the thickness T**234** of the sections **234** in proximity of the backside surface **200***b*. In some embodiments, the thickness T**236** of the sections **236** may be slightly larger towards the center of the through holes **210** than closer to the sidewalls **210***s*. In some embodiments, the frontside barrier layer **230** is formed to have a thickness T**232** in the range from 0.5 micrometers to 10 micrometers, such as of about 2 micrometers.

[0020] In FIG. **2**D, the material of a frontside seed layer **250** is sputtered on the frontside barrier layer **230** (step S**126** in FIG. **1**). For example, one or more sputtering targets **260** are hit with high energy incident atoms or ions **262** to eject sputtered material **264** which is then deposited on the frontside barrier layer **230**. In some embodiments, the pressure of the sputtering chamber and the energy of the incident atoms or ions **262** are selected so that the mean free path of the sputtered material **264** is sufficiently long to form the frontside seed layer **250** also on the section **236** of the frontside barrier layer **230** at the bottom of the through holes **210**. It should be noted that while a single target **260** is illustrated in FIG. **2**D, the disclosure is not limited thereto. For example, depending on the desired composition of the frontside seed layer **250**, multiple sputtering targets **260** may be used. In some embodiments, the frontside seed layer **250** includes a metallic material, such as copper, silver, gold, nickel, titanium, alloys thereof, a combination thereof, or the like. In some embodiments, the frontside seed layer **250** is a copper-containing layer, including copper-based materials such as copper or copper alloys.

[0021] In some embodiments, the sputtered material **264** reaches the substrate **200** from the side of the frontside surface **200***f*. The resulting frontside seed layer **250** may thus have a shape similar to the one described before for the frontside barrier layer **230**, including sections **252** extending on the sections **232** over the frontside surface **200***f* of the substrate **200**, sections **254** extending on the sections **234** over the sidewalls **210***s* of the through holes **210**, and sections **256** extending on the sections **236** at the bottom of the through holes **210** over the frontside surface **220***f* of the backside film **220**. In some embodiments, the thicknesses T**252**, T**254**, T**256** of the individual sections **252**, **254**, **256** of the frontside seed layer **250** may become increasingly smaller proceeding from the frontside surface **200***f* to the backside surface **200***b*, similar to what was previously described with respect to the frontside barrier layer **230**. The thicknesses T**252**, T**254**, T**256** are measured along directions normal to the surfaces **200***f*, **210***s*, **220***f* on which the corresponding sections **252**, **254**, **256** of the frontside seed layer **250** extend. So, for example, the sections **252** located over the frontside surface **200***f* may have a substantially constant thickness T**252** and the sections **234** located over the sidewalls **210***s* of the through holes **210** have a decreasing thickness T**254** proceeding towards the backside surface **200***b*. The sections **256** at the bottom of the through holes **210** may have a thickness T**256** comparable to the thickness T**254** of the sections **254** in proximity of the bottom surface **200***b*. In some embodiments, the thickness T**256** of the sections **256** may be slightly larger towards the center of the through holes **210** than closer to the sidewalls **210***s*. In some embodiments, the frontside seed layer **250** is formed to have a thickness T**236** in the range from 1 micrometers to 10 micrometers, such as of about 5 micrometers. In some embodiments, the frontside barrier layer **230** may decrease or even prevent diffusion of the material of the frontside seed layer **250** into the substrate **200**.

[0022] In some embodiments, once the frontside barrier layer **230** and the frontside seed layer **250** are formed, the substrate **200** may be taken out of the sputtering chamber for further processing. For example, as illustrated in FIG. **2**E to FIG. **2**I, a frontside redistribution layer (RDL) **340** may be formed on the frontside surface **200***f* (step S**130** in FIG. **1**). In FIG. **2**E, a patterned mask **270** is formed on the frontside seed layer **250**, over the frontside surface **200***f* of the substrate **200**. In some embodiments, the patterned mask **270** includes a positive or a negative photoresist, and is formed, for example, through a sequence of deposition (e.g., spin on), exposure, and development steps. In some embodiments, the patterned mask **270** is patterned to include a plurality of openings **272** extending in regions where the through holes **210** are located. That is, the through holes **210** are exposed at the bottom of the openings **272**.

[0023] Referring to FIG. **2**E and FIG. **2**F, a conductive material is deposited in the openings **272** of the patterned mask **270** to form the patterned conductive traces **280**. In some embodiments, the patterned conductive traces **280** includes routing patterns **282** extending on the horizontal sections **252** of the frontside seed layer **250**, and routing vias **284** filling the through holes **210** in between the sidewalls **210***s*. The routing vias **284** may extend from the level height of the sections **252** (at the bottom of the routing patterns **282**) to the sections **256** of the frontside seed layer **250** extending on the backside film **220**. In some embodiments, the conductive material includes cobalt (Co), tungsten (W), copper (Cu), titanium (Ti), tantalum (Ta), aluminum (Al), zirconium (Zr), hafnium (Hf), a combination thereof, or other suitable metallic materials. In some embodiments, the conductive material may be deposited via one or more plating steps. In some embodiments, the routing vias **284** and the routing patterns **282** are integrally formed (e.g., formed as a single piece during a same plating step), so that electrical connection with low resistance is established between the routing vias **284** and the routing patterns **282**. Referring to FIG. **2**F and FIG. **2**G, the patterned mask **270** is removed, for example via ashing or stripping. The portions of the frontside seed layer **250** and the frontside barrier layer **230** originally covered by the patterned mask **270** are also removed, for example via one or more etching steps. Difference in etching rates between the materials of the frontside barrier layer **230** and the frontside seed layer **250** with respect to the conductive material of the patterned conductive traces **280** may be exploited to selectively remove the exposed portions of the frontside seed layer **250** and the frontside barrier layer **230**, thus revealing again the frontside surface **200***f* of the substrate **200**. Sections **252** of the frontside seed layer **250** and sections **232** of the frontside barrier layer **230** remain underneath the regions of the routing patterns **282** extending on the frontside surface **200***f* of the substrate; sections **254** of the frontside seed layer **250** and sections **234** of the frontside barrier layer **230** remain between the routing vias **284** and the sidewalls **210***s* of the through holes **210**; and sections **256** of the frontside seed layer **250** and sections **236** of the frontside barrier layer **230** remains at the bottom of the routing vias **280**, separating the routing vias **284** from the backside film **220**. In some embodiments, the routing patterns **282** may be formed rather thick, for example with a thickness T**282** in the range from 20 micrometers to 60 micrometers.

[0024] In FIG. **2**H, a dielectric layer **290** is formed on the frontside surface **200***f* of the substrate **200**, embedding the conductive traces **280**. The dielectric layer **290** may be formed to be thicker than the conductive traces **280**, and may be patterned to include openings **292** exposing at their bottom portions of the conducive traces **280**. In some embodiments, the dielectric layer **290** includes an organic dielectric, for example a polymer such as polyimide, epoxy resin, acrylic resin, phenol resin, benzocyclobutene (BCB), polybenzoxazole (PBO), a combination thereof, or the like. In some embodiments, the dielectric layer **290** may be formed by spin-on coating, and patterned to include the openings **292**. Auxiliary mask (not shown) may be employed to define the positions and shapes of the openings **292**.

[0025] In FIG. **2**I, the upper conductive layers **300**, **320** and dielectric layers **310**, **330** of the frontside RDL **340** are formed, following similar processes as previously described. For example, the conductive material of the conductive layer **300** is deposited on the dielectric layer **290** to form routing patterns extending on the dielectric layer **290** and routing vias extending in the openings

292 of the dielectric layer **290** to contact the conductive traces **280**. The dielectric layer **310** may then be formed to embed the conductive layer **300**, and the process may be repeated to form the conductive layer **320** and the dielectric layer **330**. In some embodiments, the upper conductive layers **300**, **320** are thinner than the conductive traces **280**, for example with thicknesses T**300**, T**320** (measured in correspondence of the routing patterns) in the range from 4 micrometers to 7 micrometers. At the manufacturing stage illustrated in FIG. **2**I, the outermost dielectric layer **330** may completely cover the uppermost conductive layer **320**.

[0026] Referring to FIG. **2**I and FIG. **2**J, in some embodiments a carrier **350** is detachably bonded to the outermost dielectric layer **330** of the frontside RDL **340**. In some embodiments, the carrier **350** is a glass substrate, a metal plate, a plastic supporting board, or the like, but other suitable substrate materials may be used as long as the materials are able to withstand the subsequent steps of the process. In some embodiments, a de-bonding layer is provided on the carrier **350** to facilitate peeling the carrier **350** away from the structure when required by the manufacturing process. In some embodiments, the de-bonding layer includes a light-to-heat conversion (LTHC) release layer. The backside film **220** is removed (e.g., peeled) away from the backside surface **200***b* of the substrate **200**, which backside surface **200***b* is thus exposed. In correspondence of the through holes **210**, the sections **236** of the frontside barrier layers **230** are exposed, substantially coplanar with the backside surface **200***b*.

[0027] In some embodiments, the substrate **200** with the carrier **350** bonded thereto is introduced in a sputtering chamber to perform a sputtering process from the side of the backside surface **200***b* (step S**140** in FIG. **1**). In some embodiments, the sputtering process S**140** includes a surface preparation step S**142**, a barrier layer sputtering step S**144** and a seed layer sputtering step S**146**. In the preparation step S**142**, the backside surface **200***b* is pre-treated for subsequent material deposition. In some embodiments, a cleaning step, for example via plasma treatment, is performed to remove impurities which may have deposited or otherwise formed on the backside surface **200***b*, including possible oxidation products of the exposed sections **236** of the frontside barrier layer **230** (and, possibly, of the frontside seed layer **250**, if any portion of it is also exposed at the level of the backside surface **200***b*). After cleaning, the sputtering chamber may be brought to the target temperature and pressure for the subsequent sputtering operations, as previously described.

[0028] In FIG. **2**K, the material of a backside barrier layer **360** is sputtered on the backside surface **200***b* of the substrate **200**, including on the exposed sections **236** of the frontside barrier layer **230** (step S**44** of FIG. **1**). For example, one or more sputtering targets **370** are hit with high energy incident atoms or ions **372** to eject sputtered material **374** which is then deposited on the substrate **200**. It should be noted that while a single target **370** is illustrated in FIG. **2**K, the disclosure is not limited thereto. For example, depending on the desired composition of the backside barrier layer **360**, multiple sputtering targets **370** may be used. In some embodiments, the backside barrier layer **360** includes a metallic material, such as titanium, tantalum, a nitride thereof, or a combination thereof. In some embodiments, the backside barrier layer **360** is a titanium-containing layer, including a titanium-based material such as titanium, titanium nitride, or a combination thereof. In some embodiments, the backside barrier layer **360** is a tantalum-containing layer, including a tantalum-based material such as tantalum, tantalum nitride, or a combination thereof. In some embodiments, the backside barrier layer **360** and the frontside barrier layer **230** have substantially the same composition. In some embodiments, the sputtered material **374** reaches the substrate **200** from the side of the backside surface **200***b*. The resulting backside barrier layer **360** is blanketly deposited over the backside surface **200***b* with a substantially homogeneous thickness T**360**. In some embodiments, the target thickness T**360** may be in the range from 0.02 micrometers to 2 micrometers. In correspondence of the through holes **210**, barrier material may be present with a thickness T**1** larger than the thickness T**360** of the backside barrier layer **360**, in correspondence of the sections **236** of the frontside barrier layers **230**. In some alternative embodiments, the sections **236** of the frontside barrier layers **230** may be removed before depositing the backside barrier layer

360.

[0029] In FIG. **2**L, the material of a backside seed layer **380** is sputtered on the backside barrier layer **360** (step S**146** in FIG. **1**). For example, one or more sputtering targets **390** are hit with high energy incident atoms or ions **392** to eject sputtered material **394** which is then deposited on the backside barrier layer **360**. It should be noted that while a single target **390** is illustrated in FIG. **2**L, the disclosure is not limited thereto. For example, depending on the desired composition of the backside seed layer **380**, multiple sputtering targets **390** may be used. In some embodiments, the backside seed layer **380** includes a metallic material, such as copper, silver, gold, nickel, titanium, alloys thereof, a combination thereof, or the like. In some embodiments, the backside seed layer **380** is a copper-containing layer, including copper-based materials such as copper or copper alloys. In some embodiments, the composition of the backside seed layer **380** may be substantially the same as the composition of the frontside seed layer **250**. In some embodiments, the sputtered material **394** reaches the substrate **200** from the side of the backside surface **200***b*. The resulting backside seed layer **380** is blanketly deposited on the backside barrier layer **360** with a substantially homogeneous thickness T**380**. In some embodiments, the target thickness T**380** may be in the range from 0.05 micrometers to 5 micrometers.

[0030] In some embodiments, once the backside barrier layer **360** and the backside seed layer **380** are formed, the substrate **200** may be taken out of the sputtering chamber for further processing. For example, as illustrated in FIG. **2**M to FIG. **2**P, a backside RDL **440** may be formed on the backside surface **200***b* (step S**150** in FIG. **1**). In FIG. **2**M, a patterned mask **400** is formed on the backside seed layer **380**, with similar materials and process steps as previously described for the patterned mask **270** of FIG. **2**E. The patterned mask **400** includes openings **402** exposing at their bottom sections of the backside seed layer **380** extending over the sections **236** of the frontside barrier layer **230** at the bottom of the through holes **210**. A conductive material is disposed within the openings **402** to form the conductive blocks **410**. The conductive blocks **410** may be routing patterns extending on the backside seed layer **380**, electrically connected (via the respective seed layers **250**, **380** and barrier layers **230**, **360**) to the conductive traces **280** filling the through holes **210**. Materials and processes to form the conductive blocks **410** may be similar to the ones previously described for the conductive traces **280**, with the additional conductive material being formed on the backside seed layer **380** (e.g., without being deposited in the through holes **210**, which through holes **210** are already filled by the routing vias **284**). Referring to FIG. **2**M and FIG. **2**N, the patterned mask **400** and the underlying portions of backside seed layer **380** and backside barrier layer **360** are removed to expose the backside surface **200***b* of the substrate, similar to what was previously described with reference to FIG. **2**G. Portions of the backside seed layer **380** and the backside barrier layer **360** remains at the bottom of the conductive blocks **410**, between the conductive blocks **410** and the substrate **200**.

[0031] In FIG. **2**O, one or more semiconductor dies **420** are disposed on the substrate **200**, amongst the conductive blocks **410**. Briefly, a semiconductor die **420** may include a semiconductor substrate **422** in which active and/or passive devices are formed, conductive pads **424** formed on a side of the semiconductor substrate **422** to establish electrical connection to the active and/or passive devices, a protection layer **426** in which the conductive pads **424** are embedded, and an adhesive layer **428** securing the semiconductor substrate **422** to the substrate **200**. In some embodiments, the semiconductor die **420** may be a memory die, such as a high-bandwidth memory, a logic die, such as a central processing unit (CPU) die, a graphic processing unit (GPU) die, a micro control unit (MCU) die, an input-output (I/O) die, a baseband (BB) die, or an application processor (AP) die, and so on. In some embodiments, the semiconductor die **420** is a signal processing die.

[0032] In some embodiments, an encapsulant **430** is formed on the substrate **200** to laterally encapsulate the semiconductor die **420** and the conductive blocks **410**. A material of the encapsulant **430** includes a molding compound, a polymeric material, such as polyimide, epoxy resin, acrylic resin, phenol resin, benzocyclobutene (BCB), polybenzoxazole (PBO), a combination thereof, or other suitable polymer-based dielectric materials. In some embodiments, the encapsulant is formed by a sequence of over-molding and planarization steps, whereby the material of the encapsulant **430** is removed until the conductive pads **424** of the semiconductor die **420** and the top surfaces of the conductive blocks **410** are exposed. In some embodiments, the conductive blocks **410** are formed of comparable thickness T**410** to the semiconductor die **420**, so that the conductive blocks **410** can provide vertical connection through the encapsulant **430**. In some embodiments, the thickness T**410** of the conductive blocks **410** may be greater than about 100 micrometers, for example in the range from 100 micrometers up to 250 micrometers.

[0033] In FIG. **2**P, the backside RDL **440** is formed on the encapsulated semiconductor die **420** and the conductive blocks **410**, by alternately forming the dielectric layers **441**, **443**, **445** and the conductive layers **442**, **444**, following similar processes as previously described for the frontside RDL **340**. In some embodiments, the outermost dielectric layer **445** is patterned to include openings **446** exposing portions of the outermost conductive layer **444**. In some embodiments, the conducive layers **442**, **444** are formed to be thinner than the conductive blocks **410**, for example with thicknesses T**442**, T**444** independently in the range from 4 micrometers to 7 micrometers.

[0034] In FIG. **2**Q, through insulator vias (TIVs) **450** are formed in correspondence of the openings **446** of the backside RDL **440**, to contact the uppermost conductive layer **444**. In some embodiments, the TIVs **450** are formed by disposing a conductive material in the openings of a patterned mask (not shown). The conductive material may be disposed by any suitable process, such as a plating step or the like. In some embodiments, a semiconductor die **460** is placed on the backside RDL **440** amongst the TIVs **450**. Briefly, the semiconductor die **460** may include a semiconductor substrate **462** in which active and/or passive devices are formed, conductive pads **464** formed on a side of the semiconductor substrate **462** to establish electrical connection to the active and/or passive devices, a protection layer **466** in which the conductive pads **464** are embedded, and an adhesive layer **468** securing the semiconductor substrate **462** to the backside RDL **440**. In some embodiments the semiconductor die **460** is a micro-electromechanical system, and may be adapted to sense external stimuli such as radiation, sounds, pressure or the like. In some embodiments, the TIVs **450** and the semiconductor die **460** may be encapsulated in the encapsulant **470**, which may be formed with similar materials and processes as previously described for the encapsulant **430**.

[0035] In FIG. **2**R, an additional RDL **480** is formed on the encapsulated semiconductor die **460** and the TIVs **450**, following similar processes as previously described for the backside RDL **440**. In some embodiments, the RDL **480** includes dielectric layers **482**, **484** and at least one conductive layer **486** alternately stacked, with the conductive layer **486** interconnecting the conductive pads **464** of the semiconductor die **460** to the TIVs **450**. In some embodiments, the RDL **480** may be formed to include at least one opening **488** exposing a sensing area of the semiconductor die **460**. For example, a mask (not shown) may be disposed on the sensing area of the semiconductor die **460** to prevent the materials of the RDL **480** being deposited on the sensing area. The mask may then be removed, resulting in the opening **488**. In some embodiments, the die **460** may sense an incoming stimulus (e.g., radiation, sound wave, etc.) in correspondence of the opening **488** of the RDL **480**, and may generate a signal in response which is then transmitted for further processing to the semiconductor die **420** through the RDLs **480**, **440** and the TIVs **450**. It will be apparent that, depending on the type of semiconductor die **460** and the type of stimulus to be sensed, the opening **488** (and, more in general, the structure of the RDL **480**) may be adapted accordingly.

[0036] Referring to FIG. **2**R and FIG. **2**S, an auxiliary carrier **490** may be bonded to the RDL **480**, and the carrier **350** may be removed. For example, if an LHTC layer is included in the debonding layer, the LHTC may be irradiated to release the carrier **350**. The outermost dielectric layer **330** of the frontside RDL **340** may thus be available for further processing. In some embodiments, openings are formed in the dielectric layer **330**, for example via laser drilling, to expose regions of the underlying conductive layer **320**. Conductive terminals **500** (optionally with underlying metallurgies, not shown) are formed in the openings to contact the exposed regions of the conductive layer **320**. In some embodiments, the conductive terminals **500** include solder balls, ball grid array (BGA) connectors, metal pillars, controlled collapse chip connection (C4) bumps, micro bumps, bumps formed via electroless nickel—electroless palladium—immersion gold technique (ENEPIG), a combination thereof (e. g, a metal pillar with a solder ball attached), or the like.

[0037] Referring to FIG. **2**S and FIG. **2**T, in some embodiments, if the process has been performed at wafer level, a singulation step may be included to separate individual semiconductor packages SP**10**, and the carrier **490** may then be removed. Based on the process just described, it is possible to form semiconductor packages SP**10** in which the redistribution structures (e.g., the frontside RDL **340** and the backside RDL **440** with the conductive blocks **410**) at opposite sides of the substrate **200** are interconnected by through substrate vias (e.g., the routing vias **284**) formed in through holes **210** of the substrate **200**. What is more, by temporarily masking the through holes **210** as blind holes by way of the backside film **220**, the plating steps at opposite sides of the substrate **200** may be performed at different manufacturing stages. This allows not only to build asymmetrical redistribution structures at the opposite sides of the substrate **200**, but also to use, for example, single-side plating tools rather than double-side plating tools. What is more, at least one the frontside RDL **340** is directly connected to the routing vias **284** without intervening barrier layers, thus lowering the resistance of the electrical connection. In some embodiments, the redistribution structures at opposite side of the substrate **200** may be formed through a simple sequence of steps. In some embodiments, the frontside barrier layer **230** is interposed between the conductive material of the routing vias **284** and the substrate **200**, thus enhancing adhesion and preventing or reducing delamination failures. Furthermore, out-diffusion of the conductive material to the substrate **200** may also be prevented or reduced.

[0038] In some embodiments, the semiconductor package SP**10** may be integrated with additional components. For example, in FIG. **3**, the semiconductor package SP**12** has substantially the same structure as the semiconductor package SP**10** of FIG. **2**T, with additional integrated passive devices **510** connected to the RDL **480**, for example in between the semiconductor die **460** and the TIVs **450**. In some embodiments, the integrated passive devices **510** may preliminary transform the signal transmitted by the semiconductor die **460** upon detection of an external stimulus. It will be apparent that the structures illustrated for the semiconductor packages SP**10**, SP**12** are only exemplary, and that different components may be formed at the two sides of the substrate **200** (e.g., different types or number of semiconductor dies **420**, **460**, RDLs **440**, **480**, etc.). Furthermore, all semiconductor packages disclosed may include additional components (such as the integrated passive devices **510**), or may be integrated in larger electronic devices (for example, by connecting to printed circuit boards or the like via the conductive terminals **500**).

[0039] FIG. **4** is a schematic flow chart illustrating some steps of a manufacturing method of a semiconductor package SP**14** according to some embodiments of the disclosure. FIG. **5**A to FIG. **5**L are schematic cross-sectional views illustrating structures formed during a manufacturing process of the semiconductor package SP**14** according to some embodiments of the disclosure. In FIG. **5**A, a substrate **700** (e.g., an interposer) is provided. In some embodiments, the substrate **700** is a wafer of an inorganic material, and the inorganic material may be selected as described above for the substrate **200** of FIG. **2**A.

[0040] In some embodiments, through holes **710** are formed in the substrate **700**, extending all the way from the frontside surface **700***f* of the substrate **700** to the opposite backside surface **700***b*, for the entire thickness T**700** of the substrate **700**. In some embodiments, the thickness of the substrate **700** is larger than 200 micrometers, 300 micrometers, or even 500 micrometers, for example in the range between 300 micrometers and 1 millimeter. In some embodiments, the through holes **710** are formed by laser drilling, as previously described for the substrate **200** of FIG. **2**A, and have tapered sidewalls **710***s*, so that a width W**710***f* of the through holes **710** at the frontside surface **700***f* of the substrate **700** is greater than a width W**710***b* of the through holes **710** at the backside surface **700***b* of the substrate **700**. The tapering angle α defined by the frontside surface **700***f* of the substrate **700** and the sidewalls **710***s* of the through holes **710** may be greater than 90 degrees, for example in the range between 90 degrees and 120 degrees. In some embodiments, the through holes **710** have a high aspect ratio (e.g., the ratio between the thickness T**700** of the substrate and the width W**710***f* of the through holes **710** at the frontside surface **700***f* of the substrate **700**), for example in the range from 1.5 to 5.

[0041] In some embodiments, the substrate **700** is introduced in a sputtering chamber to perform a sputtering process from the side of the backside surface **700***b* (step S**610** in FIG. **4**). In some embodiments, the sputtering process S**610** includes a surface preparation step S**612**, a barrier layer sputtering step S**614** and a seed layer sputtering step S**616**. In the surface preparation step S**612**, the backside surface **700***b* and the sidewalls **710***s* of the through holes **710** are pre-treated for subsequent material deposition. In some embodiments, a cleaning step, for example via plasma treatment, is performed to remove impurities which may have deposited or otherwise formed on the backside surface **700***b* and the sidewalls **710***s*. After cleaning, the sputtering chamber may be brought to the target temperature and pressure for the subsequent sputtering operations.

[0042] In FIG. **5**B, the material of a backside barrier layer **720** is sputtered on the backside surface **700***b* of the substrate **700** and at least part of the sidewalls **710***s* of the through holes **710** (step S**614** in FIG. **4**). For example, one or more sputtering targets **730** are hit with high energy incident atoms or ions **732** to eject sputtered material **734** which is then deposited on the substrate **700**. In some embodiments, the pressure of the sputtering chamber and the energy of the incident atoms or ions **732** are selected so that the mean free path of the sputtered material **734** is sufficiently long to deposit on the sidewalls **710***s* of the through holes **710** close to the frontside surface **700***f*. It should be noted that while a single target **730** is illustrated in FIG. **5**B, the disclosure is not limited thereto. For example, depending on the desired composition of the backside barrier layer **720**, multiple sputtering targets **730** may be used. In some embodiments, the backside barrier layer **720** includes a metallic material, such as titanium, tantalum, a nitride thereof, or a combination thereof. In some embodiments, the backside barrier layer **720** is a titanium-containing layer, including a titanium-based material such as titanium, titanium nitride, or a combination thereof. In some embodiments, the backside barrier layer **720** is a tantalum-containing layer, including a tantalum-based material such as tantalum, tantalum nitride, or a combination thereof.

[0043] In some embodiments, the sputtered material **734** reaches the substrate **700** from the side of the backside surface **700***b*. The resulting backside barrier layer **720** may thus include sections **722** extending on the backside surface **700***b* of the substrate **700** and sections **724** extending on the sidewalls **710***s* of the through holes **710**. The thicknesses T**722**, T**724** may be measured along directions normal to the surfaces **700***b*, **710***s* on which the corresponding sections **722**, **724** of the frontside barrier layer **720** extend. In some embodiments, the sections **722** located on the backside surface **700***b* may have a substantially constant thickness T**722** and the sections **724** located on the sidewalls **710***s* of the through holes **710** have a decreasing thickness T**724** proceeding towards the frontside surface **700***f*. In some embodiments, the backside barrier layer **720** is formed to have a thickness T**722** in the range from 1 micrometer to 10 micrometers.

[0044] In FIG. **5**C, the material of a backside seed layer **740** is sputtered on the backside barrier layer **720** (step S**616** in FIG. **4**). For example, one or more sputtering targets **750** are hit with high energy incident atoms or ions **752** to eject sputtered material **754** which is then deposited on the backside barrier layer **720**. In some embodiments, the pressure of the sputtering chamber and the energy of the incident atoms or ions **752** are selected so that the mean free path of the sputtered material **264** is sufficiently long to form the backside seed layer **740** also on the section **724** of the backside barrier layer **720** on the sidewalls **710***s* of the through holes **710**. It should be noted that while a single target **750** is illustrated in FIG. **5**C, the disclosure is not limited thereto. For example, depending on the desired composition of the backside seed layer **740**, multiple sputtering targets **750** may be used. In some embodiments, the backside seed layer **740** includes a metallic material, such as copper, silver, gold, nickel, titanium, alloys thereof, a combination thereof, or the like. In some embodiments, the backside seed layer **740** is a copper-containing layer, including copper-based materials such as copper or copper alloys.

[0045] In some embodiments, the sputtered material **754** reaches the substrate **700** from the side of the backside surface **700***b*. The resulting backside seed layer **740** may thus have a shape similar to the one described before for the backside barrier layer **720**, including sections **742** extending on the sections **722** over the backside surface **700***b* of the substrate **700** and sections **744** extending on the sections **724** over the sidewalls **710***s* of the through holes **710**. In some embodiments, the thicknesses T**742**, T**744** of the individual sections **742**, **744** of the backside seed layer **740** may become increasingly smaller proceeding from the backside surface **700***b* to the frontside surface **700***f*, similar to what was previously described with respect to the backside barrier layer **720**. The thicknesses T**742**, T**744** are measured along directions normal to the surfaces **700***b*, **710***s* on which the corresponding sections **742**, **744** of the backside seed layer **740** extend. So, for example, the sections **742** located over the backside surface **200***b* may have a substantially constant thickness T**742** and the sections **744** located over the sidewalls **710***s* of the through holes **710** have a decreasing thickness T**744** proceeding towards the frontside surface **700***f*. In some embodiments, the backside seed layer **740** is formed to have a thickness T**742** in the range from 1 micrometers to 10 micrometers. In some embodiments, the backside barrier layer **720** may decrease or even prevent diffusion of the material of the backside seed layer **740** into the substrate **700**.

[0046] In some embodiments, once the backside barrier layer **720** and the backside seed layer **740** are formed, the substrate **700** may be taken out of the sputtering chamber for further processing. In some embodiments, after the sputtering process S**610** is performed on the backside surface **700***b* of the substrate **700**, the through holes **710** may still be open at both ends, i.e., at the side of both the frontside surface **700***f* and the backside surface **200***b*. In FIG. **5**D, a backside film **760** is bonded to the backside surface **700***b* of the substrate **700** (step S**620** in FIG. **4**). The backside film **760** may be selected from similar options as described above for the backside film **220** of FIG. **2**B. In some embodiments, the backside film **760** is adhered to the backside seed layer **740**, covering most or all of the backside surface **700***b*. Most notably, the backside film **760** extends at the bottom (the narrower ends) of the through holes **710**, so that the through holes **710** are plugged at the side of the backside surface **700***b* where the backside barrier layer **720** and the backside seed layer **740** have been formed. That is, the through holes **710** may in fact be masked as blind holes by way of the backside film **760**.

[0047] In some embodiments, the substrate **700** with the backside barrier layer **720** and the backside seed layer **740** formed thereon and the backside film **760** bonded thereto is introduced in a sputtering chamber to perform a sputtering process from the side of the frontside surface **700***f* (step S**630** in FIG. **4**). In some embodiments, the sputtering process S**630** includes a surface preparation step S**632**, a barrier layer sputtering step S**634**, and a seed layer sputtering step S**636**. In the preparation step S**632**, the frontside surface **700***f* of the substrate and the backside seed layer **740** on the sidewalls **710***s* of the through holes **710** are pre-treated for subsequent material deposition. In some embodiments, the preparation step S**632** includes a cleaning step, for example via plasma treatment, which cleaning step is performed to remove impurities deposited or otherwise formed, such as oxidation impurities of the material of the backside seed layer **740**. After cleaning, the sputtering chamber may be brought to the target temperature and pressure for the subsequent sputtering operations.

[0048] In FIG. **5**E, the material of a frontside barrier layer **770** is sputtered on the frontside surface **700***f* of the substrate **700** and on the backside seed layer **740** on the sidewalls **710***s* of the through holes **710** (step S**634** in FIG. **4**). For example, one or more sputtering targets **780** are hit with high energy incident atoms or ions **782** to eject sputtered material **784** which is then deposited on the substrate **700**. In some embodiments, the pressure of the sputtering chamber and the energy of the incident atoms or ions **782** are selected so that the mean free path of the sputtered material **784** is sufficiently long to form the frontside barrier layer **770** also on the backside film **760** at the bottom of the through holes **710**. It should be noted that while a single target **780** is illustrated in FIG. **5**E, the disclosure is not limited thereto. For example, depending on the desired composition of the frontside barrier layer **770**, multiple sputtering targets **780** may be used. In some embodiments, the frontside barrier layer **770** includes a metallic material, such as titanium, tantalum, a nitride thereof, or a combination thereof. In some embodiments, the frontside barrier layer **770** is a titanium-containing layer, including a titanium-based material such as titanium, titanium nitride, or a combination thereof. In some embodiments, the frontside barrier layer **770** is a tantalum-containing layer, including a tantalum-based material such as tantalum, tantalum nitride, or a combination thereof. In some embodiments, the backside barrier layer **720** and the frontside barrier layer **770** have substantially the same composition.

[0049] In some embodiments, the sputtered material **784** reaches the substrate **700** from the side of the frontside surface **700***f*. The resulting frontside barrier layer **770** may thus include sections **772** extending on the frontside surface **700***f* of the substrate **700**, sections **774** extending on sections **744** of the backside seed layer **740** on the sidewalls **710***s* of the through holes **710**, and sections **776** extending at the bottom of the through holes **710** on the frontside surface **760***f* of the backside film **760**. In some embodiments, the thicknesses T**772**, T**774**, T**776** of the individual sections **772**, **774**, **776** of the frontside barrier layer **770** may become increasingly smaller proceeding from the frontside surface **700***f* to the backside surface **700***b*. The thicknesses T**772**, T**776** may be measured along a direction normal to the surface **700***f*, and the thickness T**774** may be measured along a direction normal to the surface **710***s*. So, for example, the sections **772** located on the frontside surface **700***f* may have a substantially constant thickness T**772** and the sections **774** located on the sidewalls **710***s* of the through holes **710** have a decreasing thickness T**774** proceeding towards the backside surface **200***b*. The sections **776** at the bottom of the through holes **710** may have a thickness T**776** comparable to the thickness T**774** of the sections **774** in proximity of the bottom surface **700***b*. In some embodiments, the thickness T**776** of the sections **776** may be slightly larger towards the center of the through holes **710** than closer to the sidewalls **710***s*. In some embodiments, the frontside barrier layer **770** is formed to have a thickness T**772** in the range from 1 micrometers to 10 micrometers.

[0050] In FIG. **5**F, the material of a frontside seed layer **790** is sputtered on the frontside barrier layer **770** (step S**636** in FIG. **4**). For example, one or more sputtering targets **800** are hit with high energy incident atoms or ions **802** to eject sputtered material **804** which is then deposited on the frontside barrier layer **770**. In some embodiments, the pressure of the sputtering chamber and the energy of the incident atoms or ions **802** are selected so that the mean free path of the sputtered material **804** is sufficiently long to form the frontside seed layer **790** also on the section **776** of the frontside barrier layer **770** at the bottom of the through holes **710**. It should be noted that while a single target **800** is illustrated in FIG. **5**F, the disclosure is not limited thereto. For example, depending on the desired composition of the frontside seed layer **790**, multiple sputtering targets **800** may be used. In some embodiments, the frontside seed layer **790** includes a metallic material, such as copper, silver, gold, nickel, titanium, alloys thereof, a combination thereof, or the like. In some embodiments, the frontside seed layer **790** is a copper-containing layer, including copper-based materials such as copper or copper alloys. In some embodiments, the backside seed layer **740** and the frontside seed layer **790** have substantially the same composition.

[0051] In some embodiments, the sputtered material **804** reaches the substrate **700** from the side of the frontside surface **700***f*. The resulting frontside seed layer **790** may thus have a shape similar to the one described before for the frontside barrier layer **770**, including sections **792** extending on the sections **772** over the frontside surface **700***f* of the substrate **700**, sections **794** extending on the sections **774** over the sidewalls **710***s* of the through holes **710**, and sections **796** extending on the sections **776** at the bottom of the through holes **710** over the frontside surface **760***f* of the backside film **760**. In some embodiments, the thicknesses T**792**, T**794**, T**796** of the individual sections **792**,

794, **796** of the frontside seed layer **790** may become increasingly smaller proceeding from the frontside surface **700***f* to the backside surface **700***b* of the substrate **700**, similar to what was previously described with respect to the frontside barrier layer **770**. The thicknesses T**792**, T**796** may be measured along a direction normal to the surface **700***f*, and the thickness T**794** may be measured along a direction normal to the surface **710***s*. So, for example, the sections **792** located over the frontside surface **700***f* may have a substantially constant thickness T**792** and the sections **794** located over the sidewalls **710***s* of the through holes **710** have a decreasing thickness T**794** proceeding towards the backside surface **700***b*. The sections **796** at the bottom of the through holes **710** may have a thickness T**796** comparable to the thickness T**794** of the sections **794** in proximity of the bottom surface **700***b*. In some embodiments, the thickness T**796** of the sections **796** may be slightly larger towards the center of the through holes **710** than closer to the sidewalls **710***s*. In some embodiments, the frontside seed layer **790** is formed to have a thickness T**792** in the range from 1 micrometers to 10 micrometers. In some embodiments, the frontside barrier layer **770** may decrease or even prevent diffusion of the material of the frontside seed layer **790** into the substrate **700**.

[0052] In some embodiments, by sputtering the material of the backside barrier layer **720** and of the backside seed layer **740** from the side of the backside surface **700***b* and the material of the frontside barrier layer **770** and of the frontside seed layer **790** from the side of the frontside surface **700***f*, a composite seed-barrier layer **810** is formed along the sidewalls **710***s* of the through holes **710** by the sections **724**, **744**, **774**, **794** of the barrier layers **720**, **770** and the seed layers **740**, **790** extending along the sidewalls **710***s*. In some embodiments, the dual-side sputtering process just described results in good coverage of the surfaces **700***b*, **700***b*, **710***s* of the substrate **700**, even when the through holes **710** have a high aspect ratio. In some embodiments, an indication of the degree of the coverage may be obtained by comparing the thicknesses T**2**-T**4** of the composite seed-barrier layer **810** at its thickest (e.g., T**2** or T**3**) and thinnest (e.g., T**4**) points, where the thicknesses T**2**-T**4** correspond to combined thicknesses of the barrier layers **720**, **770** and seed layers **740**, **790**. For example, at regions closer to the frontside surface **700***f* or backside surface **700***b*, the thicknesses T**2** and T**3** of the composite seed-barrier layer **810** may be greater than the thickness T**4** of the composite seed-barrier layer **810** at about the middle of the through holes **710** (e.g., at about half of the thickness T**700** of the substrate **700**). In some embodiments, the ratio of the thickness T**4** to the thickness T**2** or T**3** (whatever is greater) may be in the range from 0.05 to 0.8 or more, also as a function of the aspect ratio of the through holes **710**. By way of example and not of limitation, when the aspect ratio of the through holes **710** is about 1.5, the ratio of the thicknesses T**4** to the thickness T**2** or T**3** may be about in the range from 0.5 to 0.8; when the aspect ratio of the through holes **710** is about 3, the ratio of the thickness T**4** to the thickness T**2** or T**3** may be about in the range from 0.15 to 0.5; and when the aspect ratio of the through holes **710** is about 5, the ratio of the thickness T**4** to the thickness T**2** or T**3** may be about in the range from 0.05 to 0.4.

[0053] In some embodiments, because a backside film **760** is installed on the backside surface **700***b* after depositing the backside barrier layer **720** and the backside seed layer **740**, the material of the frontside barrier layer **770** and the frontside seed layer **790** also extends at the bottom of the through holes **710** as if they were blind holes. In the secondary inset in FIG. **5**F, is shown a schematic cartoon of the spatial intensity distribution of the energy disperse signal (EDS) of the material of the frontside seed layer **790** at the bottom of the through holes **710**. In the example shown in the inset, the frontside seed layer **790** is a copper-containing layer, and the EDS signal observed is the one of copper. As can be seen from the inset of FIG. **5**F, a continuous copper signal spanning the distance between opposite sidewalls **710***s* at the bottom of the through holes **710** can be observed, indicating that the frontside seed layer **790** also extends at the bottom of the through holes **710**.

[0054] In some embodiments, once the frontside barrier layer **770** and the frontside seed layer **790** are formed, the substrate **700** may be taken out of the sputtering chamber for further processing. For example, as illustrated in FIG. **5**G to FIG. **5**I, a frontside RDL **840** may be formed on the frontside surface **700***f* (step S**640** in FIG. **4**). In FIG. **2**G, a patterned mask **820** including openings **825** in correspondence of the through holes **710** is formed on the frontside seed layer **790**, with similar material and processes as previously described for the patterned mask **270** with reference to FIG. **2**E. Then, a conductive material is filled in the openings **825** and the through holes **710** to form the patterned conductive traces **830**, with similar material and processes as previously described for the patterned conductive traces **830** of FIG. **2**F. In some embodiments, the patterned conductive traces **830** include routing patterns **832** extending on the horizontal sections **792** of the frontside seed layer **790**, and routing vias **834** filling the through holes **710** in between the sidewalls **710***s*. The routing vias **834** may extend from the level height of the sections **792** (at the bottom of the routing patterns **832**) to the sections **796** of the frontside seed layer **790** extending on the backside film **760**. The routing vias **834** may be integrally formed with the routing patterns **832**.

[0055] The secondary insets of FIG. **5**G are schematic cartoons of the spatial intensity distributions of the EDSs of the materials of the composite seed-barrier layer **810**, the conductive traces **830**, and the substrate **700**. In the examples shown in the insets, the substrate **700** is an aluminum-containing substrate, the backside seed layer **740** and the frontside seed layer **790** are copper-containing layers, the patterned conductive traces **830** include a copper-containing conductive material, and the backside barrier layer **720** and the frontside barrier layer **770** are titanium-containing layers. The cartoons of the insets show the spatial intensity distribution of the EDSs of copper, aluminum, and titanium. In some embodiments, the composite seed-barrier layer **810** may present different microstructures in regions at different level heights along the direction of the thickness T**700** of the substrate **700**, which regions are located at different distances from the sputtering targets **730**, **750**, **780**, **800** during the sputtering processes S**610**, S**630**. For example, in proximity of the bottom of the through vias **710**, the backside barrier layer **720**, the backside seed layer **740**, the frontside barrier layer **770**, and the frontside seed layer **790** are sequentially stacked over each other, resulting in a multilayered structure as shown in the lower of the two secondary insets. Such multilayered structure may be visible, for example, at a depth corresponding to approximately 95% of the thickness T**700** of the substrate **700**. For example, if the thickness T**700** of the substrate **700** (and hence the depth of the through holes **710**) is about 500 micrometers, the multilayered structure of the bottom inset may be visible at about 480 micrometers from the frontside surface **700***f*. At the level height of the line I-I′ illustrated in the inset, the individual layers **720**, **740**, **770**, **790** of the composite seed-barrier layer **810** may have relative thicknesses of 3:6:1:2, respectively, where the thickness ratio of the frontside seed layer **790** and the frontside barrier layer **770** has been obtained from separate measurements (a sample on which single side sputter is performed).

[0056] On the other hand, at about halfway along the through holes **710**, the composite seed-barrier layer **810** may present a different structure, as illustrated in the upper secondary inset. Halfway along the through holes **710** may correspond, for example, to a depth at about 50% of the thickness T**700** of the substrate **700**. For example, around the middle of the through holes **710**, the section **724** of the backside barrier layer **720** may cover, substantially completely, the substrate **700**, while the section **744** of the backside seed layer **740** may be discontinuous, presenting one or more gaps. The section **774** of the frontside barrier layer **770** may then fill the gaps of the backside seed layer **740**, contacting the backside barrier layer **720**. That is, the backside seed layer **740** may be present in the form of inclusions **748** (completely) surrounded by the material of the backside barrier layer **720** and the material of the frontside barrier layer **770**. For example, adjacent inclusions **748** of the backside seed layer **740** may be separated from each other by protrusions **778** of the frontside barrier layer **770**, which protrusions **778** contact the backside seed layer **720**. The frontside seed layer **790** may continuously extend on the frontside barrier layer **770**, to seed the deposition of the conductive material of the patterned conductive traces **830**. That is, by forming the composite seed-barrier layer **810** via dual-side sputtering, discontinuities in the seed layer first deposited (e.g., the backside seed layer **740**) may be filled by the later deposited barrier layer (e.g., the frontside barrier layer **770**), and the seed layer finally deposited (e.g., the frontside seed layer **790**) may substantially continuously line the through holes **710** to effectively seed the subsequent deposition of conductive material. In some embodiments, in correspondence of one of the inclusions **748** of the backside seed layer **740**, for example at the level height of the line II-II′, the individual layers **720**, **740**, **770**, **790** of the composite seed-barrier layer **810** may have relative thicknesses of 1:2:2:4, respectively, where the thickness ratio of the frontside seed layer **790** and the frontside barrier layer **770** has been obtained from separate measurements (a sample on which single side sputter is performed).

[0057] Referring to FIG. **5**G and FIG. **5**H, the patterned mask **820** and the underlying portions of the frontside seed layer **790** and the frontside barrier layer **770** are removed, for example via stripping, ashing, and/or etching, as previously described with reference to FIG. **2**G. The frontside seed layer **790** and the frontside barrier layer **770** still remain on the frontside surface **700***f* of the substrate **700** underneath the patterned conductive traces **830**. In some embodiments, the patterned conductive traces **830** may be formed with routing patterns **832** having a thickness T**832** in the range from 20 micrometers to 60 micrometers. Elsewhere, the frontside surface **700***f* of the substrate **700** may be (temporarily) exposed. In FIG. **5**I, the dielectric layers **841**, **843**, **845** and the conductive layers **842**, **844** of the frontside RDL **840** are formed as previously described with reference to FIG. **2**H and FIG. **2**I.

[0058] Referring to FIG. **51** and FIG. **5**L, in some embodiments, a backside RDL **890** may be formed on the backside surface **700***b* (step S**650** in FIG. **4**). For example, referring to FIG. **5**J, a carrier **850** is detachably bonded to the uppermost dielectric layer **845** of the frontside RDL **840**, with similar material and processes as previously described for the carrier **350** of FIG. **2**J. The backside film **760** is removed (e.g., peeled) away from the backside surface **700***b* of the substrate **700**, thus exposing the sections **742** of the backside seed layer **740**. In correspondence of the through holes **710**, the sections **776** of the frontside barrier layer **770** are exposed in between the sections **742** of the backside seed layer **740**, substantially coplanar with the backside seed layer **740**.

[0059] In FIG. **5**K, conductive blocks **860** are formed on the backside seed layer **740** following a similar process as previously described for the conductive blocks **410** with reference to FIGS. **2**M and **2**N. The conductive blocks **860** may be routing patterns extending on the backside seed layer **740**, electrically connected (via the respective seed layers **740**, **790** and barrier layers **720**, **770**) to the conductive traces **830** filling the through holes **710**. The portions of backside seed layer **740** and backside barrier layer **720** not covered by the conductive blocks **860** are removed to expose the backside surface **700***b* of the substrate **700**, similar to what was previously described with reference to FIG. **2**N, while portions of the backside seed layer **740** and the backside barrier layer **720** remains at the bottom of the conductive blocks **860**. As illustrated in the inset of FIG. **5**K, the conductive blocks **860** may contact the section **776** of the frontside barrier layer **770**, as well as the backside seed layer **740**. In some alternative embodiments, the section **776** of the frontside barrier layer **770** may be removed before forming the conductive blocks **860**.

[0060] In some embodiments, the semiconductor package SP**14** of FIG. **5**L may be obtained from the structure illustrated in FIG. **5**K following similar processes as previously described with reference to FIG. **2**O to FIG. **2**T. Briefly, a semiconductor die **870** may be disposed on the substrate **700** amongst the conductive blocks **860**, as previously described for the semiconductor die **420**. In some embodiments, the semiconductor die **870** is a logic die, such as a signal processing die. In some embodiments, the conductive blocks **860** are formed of a thickness T**860** comparable to the semiconductor die **870**, for example greater than 100 micrometers, such as in the range from 100 micrometers to 250 micrometers. The encapsulant **880** may be formed on the substrate **700** to laterally wrap the conductive blocks **860** and the semiconductor die **870**. The backside RDL **890** may then be formed on the encapsulated semiconductor die **870**, electrically contacting the semiconductor die **870** and connecting the semiconductor die **870** to the conductive blocks **860**.

Through insulator vias **900** are then formed on the backside RDL **890**, on an opposite side of the backside RDL **890** with respect to the semiconductor die **870** and the conductive blocks **860**. A semiconductor die **910** may be bonded on the backside RDL **890** amongst the TIVs **900**. The semiconductor die **910** may be a microelectromechanical system, capable of sensing external stimuli such as radiation, sound waves, touch, pressure, or the like. The semiconductor die **910** and the TIVs **900** may be encapsulated in the encapsulant **920**, and the additional RDL **930** may then be formed. The RDL **930** may leave exposed a sensing area of the semiconductor die **910**. The semiconductor die **910** may be connected to the conductive blocks **860** and the semiconductor die **870** via the RDLs **890**, **930** and the TIVs **900**, so that signals generated by the semiconductor die **910** in response to detected external stimuli may be transmitted to the semiconductor die **870** for further processing. Conductive terminals **940** may be installed on the frontside RDL **840** at an opposite side with respect to the substrate **700**, to integrate the semiconductor package SP**14** within larger devices.
[0061] Based on the process just described, it is possible to form semiconductor packages SP**14** in which the redistribution structures (e.g., the frontside RDL **840** and the backside RDL **890** with the conductive blocks **860**) at opposite sides of the substrate **700** are interconnected by through substrate vias (e.g., the routing vias **834**) formed in through holes **710** of the substrate **700**. In some embodiments, a composite seed-barrier layer **810** is formed on the sidewalls **710***s* of the through holes **710**, by sputtering the backside barrier layer **720** and the backside seed layer **740** from the one side of the substrate **700**, and sputtering the frontside barrier layer **770** and the frontside seed layer **790** from the opposite side of the substrate **700**. By doing so, adequate coverage may be achieved even when the through holes **710** have a high aspect ratio, so that the composite seed-barrier layer **810** may effectively seed the deposition of the conductive material of the routing vias **834** while enhancing adhesion to the substrate **700**. Furthermore, out-diffusion of the conductive material to the substrate **700** may also be prevented or reduced. What is more, by temporarily masking the through holes **710** as blind holes by way of the backside film **760** (illustrated, e.g., in FIG. **5**D) after sputtering on one side of the substrate **700**, the plating steps at opposite sides of the substrate **700** may be performed at different manufacturing stages. This allows not only to build asymmetrical redistribution structures at the opposite sides of the substrate **700**, but also to use, for example, single-side plating tools rather than double-side plating tools. In some embodiments, the routing pattern **832** of the bottommost layer of the frontside RDL **840** are integrally formed with the routing vias **834** (e.g., without an intervening barrier layer), thus lowering the resistance of the electrical connection. In some embodiments, the redistribution structures at opposite sides of the substrate **700** may be formed through a simple sequence of steps.
[0062] FIG. **6** is a schematic flow chart illustrating some steps of a manufacturing method of a semiconductor package SP**16** according to some embodiments of the disclosure. FIG. **7**A to FIG. **7**H are schematic cross-sectional views illustrating structure s formed during a manufacturing process of the semiconductor package SP**14** according to some embodiments of the disclosure. In some embodiments, the structure of FIG. **7**A may be obtained following substantially the same steps previously discussed with reference to FIG. **5**A to FIG. **5**C. Briefly, the substrate **1100** is provided, and the through holes **1110** are formed in the substrate **1100**, extending all the way from the frontside surface **1100***f* of the substrate **1100** to the opposite backside surface **1100***b*. In some embodiments, the thickness of the substrate **1100** is larger than 200 micrometers, 300 micrometers, or even 500 micrometers, for example in the range between 300 micrometers and 1 millimeter. In some embodiments, the through holes **1110** have a high aspect ratio, for example in the range from 1.5 to 5.
[0063] In some embodiments, the substrate **1100** is introduced in a sputtering chamber to perform a sputtering process from the side of the backside surface **1100***b* (step S**1010** in FIG. **6**). In some embodiments, the sputtering process S**1010** includes preparing the backside surface **1100***b* (e.g., step S**1012** in FIG. **6**), and then sputtering the backside barrier layer **1120** (step S**1014** in FIG. **6**)

and the backside seed layer **1130** (step S**1016** in FIG. **6**) from the side of the backside surface **100***b*. The backside barrier layer **1120** thus includes sections **1122** extending on the backside surface **1100***b* and sections **1124** extending on the sidewalls **1110***s* of the through holes **1110**, and the backside seed layer **1130** includes sections **1132** extending on the sections **1122** and sections **1134** extending on the sections **1124**. In some embodiments, the backside barrier layer **1120** includes a metallic material, such as titanium, tantalum, a nitride thereof, or a combination thereof. In some embodiments, the backside barrier layer **1120** is a titanium-containing layer, including a titanium-based material such as titanium, titanium nitride, or a combination thereof. In some embodiments, the backside barrier layer **1120** is a tantalum-containing layer, including a tantalum-based material such as tantalum, tantalum nitride, or a combination thereof. In some embodiments, the backside seed layer **1130** includes a metallic material, such as copper, silver, gold, nickel, titanium, alloys thereof, a combination thereof, or the like. In some embodiments, the backside seed layer **1130** is a copper-containing layer, including copper-based materials such as copper or copper alloys. In some embodiments, once the backside barrier layer **1120** and the backside seed layer **1130** are formed, the substrate **1100** may be flipped (step S**1020** in FIG. **6**), and a sputtering process S**1030** may be performed from the side of the frontside surface **1100***f*. For example, the frontside surface **1100***b* may be prepared (e.g., plasma cleaned; step S**1032** in FIG. **6**) for subsequent deposition of material.

[0064] In FIG. **7**B, the material of a frontside barrier layer **1140** is sputtered on the frontside surface **1100***f* of the substrate **1100** and on the backside seed layer **1130** on the sidewalls **1110***s* of the through holes **1110** (step S**1034** in FIG. **6**). For example, one or more sputtering targets **1150** are hit with high energy incident atoms or ions **1152** to eject sputtered material **1154** which is then deposited on the substrate **1100**. It should be noted that while a single target **1150** is illustrated in FIG. **7**B, the disclosure is not limited thereto. For example, depending on the desired composition of the frontside barrier layer **1140**, multiple sputtering targets **1150** may be used. In some embodiments, the frontside barrier layer **1140** includes a metallic material, such as titanium, tantalum, a nitride thereof, or a combination thereof. In some embodiments, the frontside barrier layer **1140** is a titanium-containing layer, including a titanium-based material such as titanium, titanium nitride, or a combination thereof. In some embodiments, the frontside barrier layer **1140** is a tantalum-containing layer, including a tantalum-based material such as tantalum, tantalum nitride, or a combination thereof. In some embodiments, the backside barrier layer **1120** and the frontside barrier layer **1140** have substantially the same composition.

[0065] In some embodiments, the sputtered material **1154** reaches the substrate **1100** from the side of the frontside surface **1100***f*. The resulting frontside barrier layer **1140** may thus include sections **1142** extending on the frontside surface **1100***f* of the substrate **1100** and sections **1144** extending on sections **1134** of the backside seed layer **1130** on the sidewalls **1110***s* of the through holes **1110**. In some embodiments, a difference between the present embodiment and the embodiment of FIG. **5**E lies in that the through holes **1110** have not been plugged (e.g., by the backside film **760**) when the frontside barrier layer **1140** is deposited. Therefore, the frontside barrier layer **1140** may not include a section extending approximately parallel to the backside surface **1100***b* of the substrate **1100** to contact the backside seed layer **1130** on opposite sidewalls **1110***s* of the through holes **1110**. That is, during the frontside sputtering process S**1030**, the through holes **1110** may still be at least partially open at both ends. Other aspects of the frontside barrier layer **1140** may be the same as what was previously described for the frontside barrier layer **770** of FIG. **5**E.

[0066] In FIG. **7**C, the material of a frontside seed layer **1160** is sputtered on the frontside barrier layer **1140** (step S**1036** in FIG. **6**). For example, one or more sputtering targets **1170** are hit with high energy incident atoms or ions **1172** to eject sputtered material **1174** which is then deposited on the frontside barrier layer **1140**. It should be noted that while a single target **1170** is illustrated in FIG. **7**C, the disclosure is not limited thereto. For example, depending on the desired composition of the frontside seed layer **1160**, multiple sputtering targets **1170** may be used. In some embodiments, the frontside seed layer **1160** includes a metallic material, such as copper, silver, gold, nickel, titanium, alloys thereof, a combination thereof, or the like. In some embodiments, the frontside seed layer **1160** is a copper-containing layer, including copper-based materials such as copper or copper alloys. In some embodiments, the backside seed layer **1130** and the frontside seed layer **1160** have substantially the same composition.

[0067] In some embodiments, the sputtered material **1174** reaches the substrate **1100** from the side of the frontside surface **1100***f*. The resulting frontside seed layer **1160** may thus include sections **1162** extending on the sections **1142** of the frontside barrier layer **1140** on the frontside surface **1100***f* of the substrate **1100** and sections **1164** extending on sections **1144** of the frontside barrier layer **1140** on the sidewalls **1110***s* of the through holes **1110**. In some embodiments, a composite seed-barrier layer **1180** is thus formed along the sidewalls **1110***s* of the through holes **1110**, similar to what was previously described for the composite seed-barrier layer **810** of FIG. **5**F. In some embodiments, similar degrees of coverage as previously described for the composite seed-barrier layer **810** may be achieved also for the composite seed-barrier layer **1180**. In some embodiments, a difference between the present embodiment and the embodiment of FIG. **5**F lies in that the through holes **1110** have not been plugged (e.g., by the backside film **760**) when the frontside seed layer **1160** is deposited. Therefore, the frontside seed layer **1160** may not include a section extending approximately parallel to the backside surface **1100***b* of the substrate **1100** to contact the frontside barrier layer **1140** on opposite sidewalls **1110***s* of the through holes **1110**. That is, even after the frontside sputtering process S**1030**, the through holes **1110** may still be at least partially open at both ends. Other aspects of the frontside seed layer **1160** may be the same as what was previously described for the frontside seed layer **790** of FIG. **5**F.

[0068] In some embodiments, after the backside sputtering process S**1010** and the frontside sputtering process S**1030**, the substrate **1100** may be taken out of the sputtering chamber for further processing. In FIG. **7**D, a backside film **1190** is bonded to the backside surface **1110***b* of the substrate **1100** (step S**1040** in FIG. **6**). The backside film **1190** may be selected from similar options as described above for the backside film **220** of FIG. **2**B. In some embodiments, the backside film **1190** is adhered to the backside seed layer **1130**, covering most or all of the backside surface **1100***b*. Most notably, the backside film **1190** extends at the bottom (the narrower ends) of the through holes **1110**, so that the through holes **1110** are plugged at the side of the backside surface **1100***b* were the backside barrier layer **1120** and the backside seed layer **1130** have been formed. That is, the through holes **1110** may in fact be masked as blind holes by way of the backside film **1190**.

[0069] Referring to FIG. **7**E and FIG. **7**F, after the backside film **1190** is bonded to the substrate **1110**, the frontside RDL **1220** may be formed (step S**1050** in FIG. **6**), for example with similar materials and processes as previously described. In FIG. **7**E, a patterned mask **1200** including openings **1205** in correspondence of the through holes **1110** is formed on the frontside seed layer **1160**, with similar material and processes as previously described for the patterned mask **270** with reference to FIG. **2**E. Then, a conductive material is filled in the openings **1205** and the through holes **1110** to form the patterned conductive traces **1210**, with similar material and processes as previously described for the patterned conductive traces **830** of FIG. **2**F. In some embodiments, the patterned conductive traces **1210** include routing patterns **1212** extending on the horizontal sections **1162** of the frontside seed layer **1160**, and routing vias **1214** filling the through holes **1110** in between the sidewalls **1110***s*. The routing vias **1214** may extend from the level height of the sections **1162** (at the bottom of the routing patterns **1212**) all the way to the backside film **1190**, in between the sections **1132** of the backside seed layer **1130**. The routing vias **1214** and he routing patterns **1212** may be integrally formed.

[0070] The secondary insets of FIG. **7**E are schematic cartoons of the spatial intensity distributions of the EDSs of the materials of the composite seed-barrier layer **1180**, the conductive traces **1210**, and the substrate **1100**. In the examples shown in the secondary insets, the substrate **1100** is an aluminum-containing substrate, the backside seed layer **1130** and the frontside seed layer **1160** are copper-containing layers, the patterned conductive traces **1210** include copper-containing material, and the backside barrier layer **1120** and the frontside barrier layer **1140** are titanium-containing layers. The cartoons of the insets show the spatial intensity distribution of the EDSs of copper, aluminum, and titanium. In some embodiments, the composite seed-barrier layer **1110** may present different microstructures in regions at different level heights along the direction of the thickness T**1100** of the substrate **1100**, as previously described for the composite seed-barrier layer **810** of FIG. **5**G. For example, in proximity of the bottom of the through vias **1110**, the backside barrier layer **1120**, the backside seed layer **1130**, the frontside barrier layer **1140**, and the frontside seed layer **1160** are sequentially stacked over each other, resulting in a multilayered structure as shown in the lower of the two secondary insets. Such multilayered structure may be visible, for example, at a depth corresponding to approximately 95% of the thickness T**1100** of the substrate **1100**. For example, if the thickness T**1100** of the substrate **1100** (and hence the depth of the through holes **1110**) is about 500 micrometers, the multilayered structure of the bottom inset may be visible at about 480 micrometers from the frontside surface **1100***f*. At the level height of the line III-III′ illustrated in the lower secondary inset, the individual layers **1120**, **1130**, **1140**, **1160** of the composite seed-barrier layer **1180** may have relative thicknesses of 3:6:1:2, respectively, where the thickness of the frontside seed layer **1160** has been obtained before depositing the conductive material of the patterned conductive traces **1210**.

[0071] On the other hand, at about halfway along the through holes **1110**, the composite seed-barrier layer **1180** may present a different structure, as illustrated in the upper secondary inset. Halfway along the through holes **1110** may correspond, for example, to a depth at about 50% of the thickness T**1100** of the substrate **1100**. For example, around the middle of the through holes **1110**, the section **1124** of the backside barrier layer **1120** may cover, substantially completely, the substrate **1100**, while the section **1134** of the backside seed layer **1130** may be discontinuous, presenting one or more gaps. The section **1144** of the frontside barrier layer **1140** may then fill the gaps of the backside seed layer **1130**, contacting the backside barrier layer **1120**. That is, the backside seed layer **1130** may be present in the form of inclusions **1138** (completely) surrounded by the material of the backside barrier layer **1120** and the material of the frontside barrier layer **1140**. For example, adjacent inclusions **1138** of the backside seed layer **1130** may be separated from each other by protrusions **1148** of the frontside barrier layer **1140**, which protrusions **1148** contact the backside barrier layer **1120**. The frontside seed layer **1160** may continuously extend on the frontside barrier layer **1140**, to seed the deposition of the conductive material of the patterned conductive traces **1210**. That is, by forming the composite seed-barrier layer **1180** via dual-side sputtering, discontinuities in the seed layer first deposited (e.g., the backside seed layer **1130**) may be filled by the later deposited barrier layer (e.g., the frontside barrier layer **1140**), and the seed layer finally deposited (e.g., the frontside seed layer **1160**) may substantially continuously line the through holes **1110** to effectively seed the subsequent deposition of conductive material. In some embodiments, in correspondence of one of the inclusions **1138** of the backside seed layer **1130**, for example at the level height of the line IV-IV′, the individual layers **1120**, **1130**, **1140**, **1160** of the composite seed-barrier layer **1180** may have relative thicknesses of 1:2:2:4, respectively, where the thickness of the frontside seed layer **1160** has been obtained before depositing the conductive material of the patterned conductive traces **1210**

[0072] Referring to FIG. **7**E and FIG. **7**F, the patterned mask **1200** and the underlying portions of the frontside seed layer **1160** and the frontside barrier layer **1140** are removed, for example via stripping, ashing, and/or etching, as previously described with reference to FIG. **2**G. The frontside seed layer **1160** and the frontside barrier layer **1140** still remain on the frontside surface **1100***f* of the substrate **1100** underneath the patterned conductive traces **1210**. Then, the dielectric layers and the conductive layers of the frontside RDL **1220** are formed as previously described with reference to FIG. **2**H and FIG. **2**I. After the frontside RDL **1220** is formed, a carrier **1230** is detachably bonded to the frontside RDL **1220** at an opposite side with respect to the substrate **1100**, with similar material and processes as previously described for the carrier **350** of FIG. **2**J. The backside film **1190** is removed (e.g., peeled) away from the backside surface **1100***b* of the substrate **1100**, thus exposing the sections **1162** of the backside seed layer **1162**. In correspondence of the through holes **1110**, the routing vias **1214** of the patterned conductive traces **1210** are exposed in between the sections **1162** of the backside seed layer **1160**, substantially coplanar with the backside seed layer **1160**.

[0073] Referring to FIG. **7**G and FIG. **7**H, in some embodiments, a backside RDL **1270** may be formed on the backside surface **1100***b* (step S**1060** in FIG. **6**). In FIG. **7**G, conductive blocks **1240** are formed on the backside seed layer **1130** following a similar process as previously described for the conductive blocks **410** with reference to FIGS. **2**M and FIG. **2**N. The portions of backside seed layer **1130** and backside barrier layer **1120** not covered by the conductive blocks **1240** are removed to expose the backside surface **1100***b* of the substrate **1100**, similar to what was previously described with reference to FIG. **2**N, while portions of the backside seed layer **1130** and the backside barrier layer **1120** remains at the bottom of the conductive blocks **1240**. As illustrated in the inset of FIG. **7**G, the conductive blocks **1240** may be routing patterns extending on the backside seed layer **1130**, and may be directly connected to the conductive traces **1210** filling the through holes **1110**. That is, because the frontside seed layer **1160** and the frontside barrier layer **1140** are formed before the backside film **1190** (illustrated e.g., in FIG. **7**E) is installed, no barrier material is disposed between the routing vias **1214** and the conductive blocks **1240**, and lower contact resistance may be achieved.

[0074] In some embodiments, the semiconductor package SP**16** of FIG. **7**H may be obtained from the structure illustrated in FIG. **7**G following similar processes as previously described with reference to FIG. **2**O to FIG. **2**T. Briefly, a semiconductor die **1250** may be disposed on the substrate **1100** amongst the conductive blocks **1240**, as previously described for the semiconductor die **420**. In some embodiments, the semiconductor die **1250** is a logic die, such as a signal processing die. In some embodiments, the conductive blocks **1240** are formed of a thickness T**1240** comparable to the semiconductor die **1250**, for example greater than 100 micrometers, such as in the range from 100 micrometers to 250 micrometers. In some embodiments, the conductive blocks **1240** may be thicker than the routing patterns **1212** of the patterned conductive traces **1210**. For example, the thickness T**1212** of the routing patterns **1212** may be in the range from 20 micrometers to 60 micrometers. In some embodiments, the encapsulant **1260** is formed on the substrate **1100** to laterally wrap the conductive blocks **1240** and the semiconductor die **1250**. The backside RDL **1270** may then be formed on the encapsulated semiconductor die **1250**, electrically contacting the semiconductor die **1250** and connecting the semiconductor die **1250** to the conductive blocks **1240**. Through insulator vias **1280** are then formed on the backside RDL **1270**, on an opposite side of the backside RDL**1270** with respect to the semiconductor die **1250** and the conductive blocks **1240**. A semiconductor die **1290** may be bonded on the backside RDL **1270** amongst the TIVs **1280**. The semiconductor die **1290** may be a microelectromechanical system, capable of sensing external stimuli such as radiation, sound waves, touch, pressure, or the like. The semiconductor die **1290** and the TIVs **1280** may be encapsulated in the encapsulant **1300**, and the additional RDL **1310** may then be formed. The RDL **1310** may leave exposed a sensing area of the semiconductor die **1290**. The semiconductor die **1290** may be connected to the conductive blocks **1240** and the semiconductor die **1250** via the RDLs **1310**, **1270** and the TIVs **1280**, so that signals generated by the semiconductor die **1290** in response to detected external stimuli may be transmitted to the semiconductor die **1250** for further processing. Conductive terminals **1320** may be installed on the frontside RDL **1220** at an opposite side with respect to the substrate **1100**, to integrate the semiconductor package SP**16** within larger devices.

[0075] Based on the process just described, it is possible to form semiconductor packages SP**16** in which the redistribution structures (e.g., the frontside RDL **1220** and the backside RDL **1270** and the conductive blocks **1240**) at opposite sides of the substrate **1100** are interconnected by through substrate vias (e.g., the routing vias **1214**) formed in through holes **1110** of the substrate **1100**. In some embodiments, a composite seed-barrier layer **1180** is formed on the sidewalls **1110***s* of the through holes **1110**, by sputtering the backside barrier layer **1120** and the backside seed layer **1130** from the one side of the substrate **1100**, and sputtering the frontside barrier layer **1140** and the frontside seed layer **1160** from the opposite side of the substrate **1100**. By doing so, adequate coverage may be achieved even when the through holes **1110** have a high aspect ratio, so that the composite seed-barrier layer **1180** may effectively seed the deposition of the conductive material of the routing vias **1214** while enhancing adhesion to the substrate **1100**. Furthermore, out-diffusion of the conductive material to the substrate **1100** may also be prevented or reduced. In some embodiments, by temporarily masking the through holes **1110** as blind holes by way of the backside film **1190** (illustrated, e.g., in FIG. **7**E) after sputtering on the composite seed-barrier layer **1180** on the substrate **1100**, the plating steps at opposite sides of the substrate **1100** may be performed at different manufacturing stages. This allows not only to build asymmetrical redistribution structures at the opposite sides of the substrate **1100**, but also to use, for example, single-side plating tools rather than double-side plating tools. What is more, by bonding the backside film **1190** after the composite seed-barrier layer **1180** has been formed, the two redistribution structures may be directly connected to each other without intervening barrier material, thus lowering the resistance of the electrical connection. In some embodiments, the redistribution structures at opposite sides of the substrate **1100** may be formed through a simple sequence of steps.

[0076] In accordance with some embodiments of the disclosure, a semiconductor package includes a substrate, a composite seed-barrier layer, a routing via, and a semiconductor die. The substrate has a through hole formed therethrough. The composite seed-barrier layer extends on sidewalls of the through hole and includes a first barrier layer, a seed layer, and a second barrier layer sequentially stacked on the sidewalls of the through hole. The routing via fills the through hole and is separated from the substrate by the composite seed-barrier layer. The semiconductor die is electrically connected to the routing via. Along the sidewalls of the through holes, at a level height corresponding to half of a total thickness of the substrate, the seed layer is present as inclusions of seed material surrounded by barrier material of the first barrier layer and the second barrier layer.

[0077] In accordance with some embodiments of the disclosure, a semiconductor package includes a substrate, a barrier layer, a seed layer, a patterned conductive trace, and a conductive block. The substrate has a frontside surface and a backside surface opposite to the frontside surface and connected to the frontside surface by tapered sidewalls of the substrate. The barrier layer extends on the frontside surface and over the tapered sidewalls of the substrate. The seed layer extends on the barrier layer. The patterned conductive trace includes a routing pattern and a routing via. The routing pattern extends on a section of the seed layer disposed over the frontside surface. The routing via is formed as a single piece with the routing pattern and extends on a section of the seed layer disposed over the tapered sidewalls. The conductive block extends over the backside surface and is electrically connected to the patterned conductive trace. Sections of the barrier layer and the seed layer are disposed between the conductive block and the routing via.

[0078] In accordance with some embodiments of the disclosure, a manufacturing method of a semiconductor package includes the following steps. A first barrier material is sputtered on a substrate having through holes extending from a frontside surface to a backside surface. The first barrier material is sputtered towards the frontside surface. A first seed material is sputtered on the sputtered first barrier material towards the frontside surface. A backside film is bonded to a backside surface of the substrate. The through holes are blocked at one end by the backside film. A first conductive material is plated on the sputtered seed material after the backside film is bonded to the substrate. The plated first conductive material is formed in the through holes and over the frontside surface of the substrate. The backside film is removed after the first conductive material is plated.

[0079] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

Claims

1. A semiconductor package, comprising: a substrate, having a frontside surface and a backside surface opposite to each other, and a through hole connecting the frontside surface and the backside surface; a conductive material, filled into the through hole to form a conductive via; and a composite seed-barrier layer, extending between a sidewall of the through hole and the conductive via, wherein a first region of the composite seed-barrier layer adjacent to the backside surface comprises a first barrier layer, a seed layer and a second barrier layer sequentially stacked on the sidewall of the through hole, and a second region of the composite seed-barrier layer adjacent to the frontside surface has the seed layer present as inclusions of a seed material surrounded by a barrier material of the first barrier layer and the second barrier layer.
2. The semiconductor package of claim 1, wherein the seed material comprises copper, silver, gold, nickel, titanium, alloys thereof, or a combination thereof, and the barrier material comprises titanium, tantalum, a nitride thereof, or a combination thereof, and has a different composition than the seed material.
3. The semiconductor package of claim 1, wherein the first barrier layer and the seed layer further extend over the backside surface of the substrate, and the second barrier layer further extends on the frontside surface of the substrate.
4. The semiconductor package of claim 1, wherein the composite seed-barrier layer further comprises another seed layer stacked on the second barrier layer.
5. The semiconductor package of claim 3, further comprising a conductive block extending over the backside surface of the substrate and electrically contacting the conductive via, wherein the conductive block extends on sections of the seed layer and the conductive via.
6. The semiconductor package of claim 5, further comprising a semiconductor die disposed over the backside surface of the substrate and beside the conductive block.
7. The semiconductor package of claim 6, further comprising: an encapsulant, laterally encapsulating the conductive block and the semiconductor die; and a redistribution layer (RDL) structure, overlying the encapsulant, the semiconductor die, and conductive block, wherein conductive layers of the RDL structure electrically connect the conductive block to the semiconductor die.
8. The semiconductor package of claim 6, wherein the semiconductor die and the conductive block are at the same level.
9. A method of forming a semiconductor package, comprising: providing a substrate having a frontside surface and a backside surface opposite to each other, wherein the substrate comprises a through hole connecting the frontside surface and the backside surface; forming a composite seed-barrier layer along a sidewall of the through hole; and forming a conductive material into the through hole to form a conductive via, wherein a first region of the composite seed-barrier layer adjacent to the backside surface comprises a first barrier layer, a seed layer and a second barrier layer sequentially stacked on the sidewall of the through hole, and a second region of the composite seed-barrier layer adjacent to the frontside surface has the seed layer present as inclusions of a seed material surrounded by a barrier material of the first barrier layer and the second barrier layer.
10. The method of claim 9, wherein forming the composite seed-barrier layer comprises: sputtering

a first barrier material on the backside surface of the substrate; sputtering a first seed material on the sputtered first barrier material; sputtering a second barrier material on the frontside surface of the substrate; sputtering a second seed material on the sputtered second barrier material; bonding a backside film to the backside surface of the substrate, so that the through hole is blocked at one end by the backside film after sputtering the second seed material and before forming the conductive material; and removing the backside film after the conductive via is formed.

11. The method of claim 9, wherein forming the composite seed-barrier layer comprises: sputtering a first barrier material on the backside surface of the substrate; sputtering a first seed material on the sputtered first barrier material; sputtering a second barrier material on the frontside surface of the substrate; sputtering a second seed material on the sputtered second barrier material; bonding a backside film to the backside surface of the substrate, so that the through hole is blocked at one end by the backside film after sputtering the first seed material and before sputtering the second barrier material; and removing the backside film after the conductive via is formed.

12. The method of claim 9, wherein the first barrier layer and the seed layer further extend over the backside surface of the substrate, and the second barrier layer further extends on the frontside surface of the substrate.

13. The method of claim 9, wherein the composite seed-barrier layer further comprises another seed layer formed on the second barrier layer.

14. The method of claim 9, further comprising forming a conductive block on the backside surface of the substrate to electrically contact the conductive via.

15. The method of claim 14, wherein the conductive block is in direct contact with the conductive via.

16. A method of forming a semiconductor package, comprising: providing a substrate having a frontside surface and a backside surface opposite to each other, wherein the substrate comprises a through hole connecting the frontside surface and the backside surface; bonding a backside film to the backside surface of the substrate to block one end of the through hole; forming a first composite seed-barrier layer on the frontside surface of the substrate, wherein the first composite seed-barrier layer covers a bottom surface and a sidewall of the conductive via, wherein an average thickness of the first composite seed-barrier layer covering the bottom surface of the conductive via is substantially less than an average thickness of the first composite seed-barrier layer covering the sidewall of the conductive via; forming a conductive material on the first composite seed-barrier layer, wherein the conductive material fills into the through hole to form a conductive via, after forming the conductive via, removing the backside film to expose the first composite seed-barrier layer; and forming a second composite seed-barrier layer on the backside surface of the substrate, wherein the second composite seed-barrier layer is in contact with the first composite seed-barrier layer and the substrate at a same plane extending along the backside surface of the substrate.

17. The method of claim 16, wherein the forming the first composite seed-barrier layer comprises: with the backside film in place, sputtering a first barrier material towards the frontside surface of the substrate, so that the first barrier material is in contact with the backside film; and sputtering a first seed material on the sputtered first barrier material towards the frontside surface of the substrate, wherein the first seed material and the first barrier material have different material compositions.

18. The method of claim 16, wherein the forming the second composite seed-barrier layer comprises: after removing the backside film, sputtering a second barrier material towards the backside surface of the substrate, so that the second barrier material is in contact with the first barrier material; and sputtering a second seed material on the sputtered second barrier material towards the backside surface of the substrate, wherein the second seed material and the second barrier material have different material compositions.

19. The method of claim 16, further comprising: forming a conductive block on the second composite seed-barrier layer, wherein the conductive block has a sidewall substantially aligned with a sidewall of the second composite seed-barrier layer.

20. The method of claim 19, further comprising: mounting a semiconductor die aside the conductive block; forming an encapsulant to laterally encapsulate the semiconductor die and the conductive block; and forming a redistribution layer (RDL) structure over the encapsulant, the conductive block and the semiconductor die, wherein the semiconductor die is electrically connected to the conductive block by the RDL structure.