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REDUCED GATE DRIVE FOR POWER CONVERTER WITH DYNAMICALLY SWITCHING RATIO

Abstract

Circuits and methods for selectable conversion ratio power converters that include low-dropout (LDO) power supplies adapted to select voltage inputs based on the selected conversion ratio while achieving high efficiency. The LDO power supplies limit current through power FETs of power converters, thereby mitigating or eliminating potentially damaging events. In some embodiments, first and second full gate-drive LDOs have “wired-OR” outputs which may power a target circuit such as a pre-driver (and optionally, a level-shifter) coupled to the gate of a power FET. In some embodiments, first and second reduced gate-drive LDOs have “wired-OR” outputs that may power a final driver coupled to the gate of a power FET. Some embodiments have dual full gate-drive LDOs that power a target circuit such as a pre-driver (and optionally, a level-shifter), while dual reduced gate-drive LDOs that power a final driver coupled to the gate of the power FET.

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATIONS [0001] The present application is a continuation of U.S. application Ser. No. 17/960,712 filed Oct. 5, 2022, entitled “Reduced Gate Drive for Power Converter with Dynamically Switching Ratio”, U.S. application Ser. No. 17/960,712 may be related to the U.S. patent application Ser. No. 17/331,594, filed May 26, 2021, entitled “Dynamic Division Ratio Charge Pump Switching”, which are hereby incorporated by reference in their entirety. [0002] The present application is a continuation of International Patent Application No. PCT/US2023/075821 filed Oct. 3, 2023, entitled “Reduced Gate Drive for Power Converter with Dynamically Switching Ratio”, International Patent Application No. PCT/US2023/075821 is a continuation of U.S. application Ser. No. 17/960,712 filed Oct. 5, 2022, entitled “Reduced Gate Drive for Power Converter with Dynamically Switching Ratio”, which are hereby incorporated by reference in their entirety.

BACKGROUND
(1) Technical Field
[0003] This invention relates to electronic circuits, and more particularly to power converter circuits, including DC-DC converter circuits, and current limiting circuits for such converter circuits.
(2) Background
[0004] Many electronic products, particularly mobile computing and/or communication products and components (e.g., notebook computers, ultra-book computers, tablet devices, LCD and LED displays) require multiple voltage levels. For example, radio frequency (RF) transmitter power amplifiers may require relatively high voltages (e.g., 12V or more), whereas logic circuitry may require a low voltage level (e.g., 1-2V). Still other circuitry may require an intermediate voltage level (e.g., 5-10V).
[0005] Power converters are often used to generate a lower or higher voltage from a common power source, such as a battery. One type of power converter comprises a converter circuit (e.g., a charge pump based on a switch-capacitor network), control circuitry, and, in some embodiments, auxiliary circuitry such as bias voltage generator(s), a clock generator, a voltage regulator, a voltage control circuit, etc. As used in this disclosure, the term “charge pump” refers to a switched-capacitor network configured to boost or buck V.sub.IN to V.sub.OUT. Examples of such charge pumps include cascade multiplier, Dickson, Ladder, Series-Parallel, Fibonacci, and Doubler switched-capacitor networks, all of which may be configured as a multi-phase or a single-phase network. Switched-capacitor network DC-DC converters are generally integrated circuits (ICs) that may have some external components (such as capacitors) and in most cases are characterized as having a fixed V.sub.IN to V.sub.OUT conversion ratio (e.g., division by 2 or by 3). As is known in the art, an AC-DC power converter can be built up from a DC-DC power converter by, for example, first rectifying an AC input to a DC voltage and then applying the DC voltage to a DC-

DC power converter.
[0006] To provide greater flexibility to system designers, and to deal with applications where a power source may change that requires different conversion ratios (e.g., as a battery discharges and outputs a lower voltage, or when the power source to a device is switched between a battery and an AC-DC power line source), it is useful to utilize a DC-DC power converter having a selectable conversion ratio. For example, U.S. Pat. No. 10,263,514 B1, issued Apr. 16, 2019, entitled “Selectable Conversion Ratio DC-DC Converter”, assigned to the assignee of the present invention and hereby incorporated by this reference, describes a Dickson DC-DC power converter that may be switched between a divide-by-2 (DIV2) mode of operation and a divide-by-3 (DIV3) mode of operation. As another example, U.S. Pat. No. 9,203,299 B2, issued Dec. 1, 2015, entitled “Controller-Driven Reconfiguration of Switched-Capacitor Power Converter”, now assigned to the assignee of the present invention and hereby incorporated by this reference, describes other DC-DC power converter architectures having reconfigurable conversion ratios.
[0007] A general problem with many FET-based DC-DC power converter architectures is that excessive current in-rush needs to be avoided during startup of the power converter. For example, for a selectable conversion ratio DC-DC converter of the type shown in U.S. Pat. No. 10,263,514 B1, absent sufficient guard circuitry, when an input voltage V.sub.IN is first applied, none of the capacitors (sometimes known as “fly capacitors”) would be charged initially and accordingly current rushes into the circuit. For instance, if the ON resistance, R.sub.ON, of the FET power switches is 1 milliohm (0.001 ohms), and V.sub.IN is 10V, then as a result of Ohm's law, V=I×R, the in-rush current will be a spike of about 10,000 amps. In integrated circuit implementations, parasitic inductances exist (for example, due to on-die conductor routing and printed circuit board conductor routing) which transform a current spike to a voltage spike in accordance with inductor theory: V=L×dI/dt. Such voltage spikes electrically overstress the charge pump power switches, affecting their reliability, potentially to destruction. For a 1 ns 100 A pulse to generate 10V across the charge pump power switches, the parasitic inductance need only be about 100 pH. The resulting 10V spike may exceed the breakdown voltage of many of the FET switches, and of course, a larger current spike results in a larger voltage spike for the same parasitic inductance.
[0008] A related problem occurs when the fly capacitors of a DC-DC power converter are out of balance, meaning that a charge difference exists between fly capacitors connected by power switches. If charge balance is not maintained, current spikes and resulting damaging voltage spikes can occur.
[0009] A further design challenge is attaining high efficiency, especially important for devices (e.g., cell phones, “smart” watches, and fitness wearables), having constrained battery space.
[0010] Accordingly, it would be useful to be able to mitigate or eliminate what may be characterized as “potentially damaging events” in power converters (e.g., damaging current spikes that may occur for a variety of reasons, including in-rush current, charge transfer current, short circuits, EMI events, and the like) while achieving high efficiency.

SUMMARY

[0011] The present invention provides circuits and methods for selectable conversion ratio power converters that include low-dropout (LDO) power supplies adapted to select voltage inputs based on the selected conversion ratio while achieving high efficiency. The LDO power supplies limit current through power FETs of power converters, thereby mitigating or eliminating potentially damaging events. Such circuits and methods provide protection against potentially damaging events such as current spikes during a “soft-start” for power converters and during dynamic charge balancing, without requiring added circuitry directed to those functions.
[0012] The present invention recognizes that basing the gate voltage to all of the non-top level power switches of a power converter on V.sub.IN or a similar voltage level is inefficient, since those supply voltages are higher than needed to switch the lower-level power FETs. Accordingly, one aspect of the present invention is the utilization of internal voltage nodes of the power

converter itself to efficiently power the gates of the lower-level power switches. A complicating factor in using such internal voltage nodes is that the division ratio of the power converter may be dynamically switched, which affects the voltage available at some of the utilized internal voltage nodes because of the change of switching phases for some power FETs (e.g., power switch S**2**). Further, during transitions between DIV2 and DIV3 operation, an incorrect LDO configuration can cause cascading effects that can damage the power converter. Accordingly, another aspect of the present invention is an adaptive circuit architecture that functionally allows dynamic switching between different voltage supply sources for the LDOs powering associated level shifters and pre-drivers and for the LDOs powering the associated final drivers.

[0013] In one embodiment, the invention encompasses a dual low-dropout circuit configuration including: a first low-dropout circuit including a FET circuit configured to be coupled between a first voltage source and a target circuit, the first low-dropout circuit configured to selectively apply a first voltage to a voltage input node of the target circuit; and a second low-dropout circuit including a FET circuit configured to be coupled between a second voltage source and the target circuit, the second low-dropout circuit configured to selectively apply a second voltage to the voltage input node of the target circuit.

[0014] In some embodiments, the first and second low-dropout circuits are full gate-drive LDOs having "wired-OR" outputs which may, for example, provide power to a target circuit such as a pre-driver (and optionally, a level-shifter) coupled to the gate of a power FET. In some embodiments, the first and second low-dropout circuits are reduced gate-drive LDOs having "wired-OR" outputs that may, for example, provide power to a final driver coupled to the gate of a power FET. Some embodiments, dual full gate-drive LDOs having "wired-OR" outputs provide power to a target circuit such as a pre-driver (and optionally, a level-shifter) coupled to the gate of a power FET, while dual reduced gate-drive LDOs having "wired-OR" outputs provide power to a final driver coupled to the gate of the power FET.

[0015] The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

Description

DESCRIPTION OF THE DRAWINGS

[0016] FIG. **1** is a block diagram of one embodiment of a DC-DC selectable conversion ratio power converter.

[0017] FIG. **2** is a block diagram of one section of a power converter showing details for a FET implementation of the power switches of that section.

[0018] FIG. **3**A is a schematic diagram of one embodiment of the level-shifter/driver block and the LDO block of FIG. **2**.

[0019] FIG. **3**B is a block diagram showing details of one embodiment of a switch control block **316**.

[0020] FIG. **4** is a schematic block diagram of one embodiment of a charge pump.

[0021] FIG. **5**A is a block diagram of one embodiment of a "source switching" LDO configured to provide regulated power to a level shifter/pre-driver (comparable to the level shifter and pre-driver of FIG. **3**A) and a final driver (comparable to the final driver of FIG. **3**A).

[0022] FIG. **5**B is a block diagram of the dual full gate-drive LDO sections of FIG. **5**A, showing greater detail.

[0023] FIG. **5**C is a block diagram of the dual reduced gate-drive LDO sections of FIG. **5**A, showing greater detail.

[0024] FIG. **5**D is a block diagram of an alternative embodiment of the dual reduced gate-drive

LDO sections of FIG. **5**A.

[0025] FIG. **6** is a schematic diagram of dual full gate-drive LDO sections in a DIV2 configuration for power switch S**2**.

[0026] FIG. **7**A is a schematic diagram of dual reduced gate-drive LDO sections for an LDO transitioning from a DIV3 to a DIV2 mode.

[0027] FIG. **7**B is a set of graphs of current and voltage as a function of time for a dual reduced gate-drive LDO depicting the issue of ON-time overlap.

[0028] FIG. **7**C is a set of graphs of current and voltage as a function of time for a dual reduced gate-drive LDO that includes the fast-discharge switch M.sub.FD of FIG. **7**A.

[0029] FIG. **8** is a top plan view of a substrate that may be, for example, a printed circuit board or chip module substrate (e.g., a thin-film tile).

[0030] FIG. **9** is a process flow chart showing a method of providing power to a voltage input node of a target circuit.

[0031] FIG. **10** is a process flow chart showing a method of providing power to a voltage input node of a driver circuit for a power FET having a gate, and to the gate of the power FET.

[0032] Like reference numbers and designations in the various drawings indicate like elements.

DETAILED DESCRIPTION

[0033] The present invention provides circuits and methods for selectable conversion ratio power converters that include low-dropout (LDO) power supplies adapted to select voltage inputs based on the selected conversion ratio while achieving high efficiency. The LDO power supplies limit current through power FETs of power converters, thereby mitigating or eliminating potentially damaging events. Such circuits and methods provide protection against potentially damaging events such as current spikes during a “soft-start” for power converters and during dynamic charge balancing, without requiring added circuitry directed to those functions.

Example Selectable Conversion Ratio Power Converter

[0034] FIG. **1** is a block diagram of one embodiment of a DC-DC selectable conversion ratio power converter **100**. The specific illustrated power converter **100** may be selectably configured to be either a divide-by-2 (DIV2) Dickson converter or a divide-by-3 (DIV3) Dickson converter using the same basic circuit. The same power converter **100** may be used in general for DC-to-DC boost conversion by reversing the voltage input and voltage output, possibly with some relatively minor design changes. The illustrated power converter **100** includes two parallel sections **102***a*, **102***b* that are coupled between a voltage source V.sub.IN and a reference potential **104** such as circuit ground. Each section **102***a*, **102***b* includes 3 series-connected switches S**1**-S**3** coupled in series to a first branch comprising 2 series-connected switches S**4**-S**5**, and to a second branch comprising 2 series-connected switches S**6**-S**7**. Each switch may comprise, for example, one or more FETs, including one or more MOSFETs.

[0035] In each section **102***a*, **102***b*, coupled between a first upper pair of switches S**1**, S**2** and a first branch pair of switches S**4**, S**5** is a first capacitor C**1***a*, C**1***b*, and coupled between a second upper pair of switches S**2**, S**3** and a second branch pair of switches S**6**, S**7** is a second capacitor C**2***a*, C**2***b*. The first capacitors C**1***a*, C**1***b*, when charged, have a voltage of V.sub.IN/2 across them at respective nodes V.sub.C1a and V.sub.C1b. The second capacitors C**2***a*, C**2***b*, when charged, have a voltage of either V.sub.IN/2 (DIV/2) or V.sub.IN/3 (DIV/3) across them at respective nodes V.sub.C2a and V.sub.C2b. Depending on the output ratio configuration (divide-by-2 or divide-by-3), each section **102***a*, **102***b* may generate an output voltage at a node V.sub.X that is coupled to an output capacitor C.sub.OUT.

[0036] At least some of the switches S**1**-S**7** may be selectively controlled to be in an ON (conductive) or OFF (blocking) state by control circuitry (not shown). At least some of the switches S**1**-S**7** may be selectively coupled to one of two non-overlapping complementary clock phases, P**1** or P**2**. Some of the switches S**1**-S**7** may be permanently coupled to one of the two complementary clock phases, P**1** or P**2**. TABLE 1 below shows the configuration of the state or associated clock phase for each of the switches S**1**-S**7** of the two parallel sections **102***a*, **102***b* for both a divide-by-2 configuration and a divide-by-3 configuration.

TABLE-US-00001 TABLE 1 Divide-by-2 Configuration Divide-by-3 Configuration Section 102a Section 102b Section 102a Section 102b S1 = P1 S1 = P2 S1 = P1 S1 = P2 S2 = ON S2 = ON S2 = P2 S2 = P1 S3 = P2 S3 = P1 S3 = P1 S3 = P2 S4 = P1 S4 = P2 S4 = P1 S4 = P2 S5 = P2 S5 = P1 S5 = P2 S5 = P1 S6 = P1 S6 = P2 S6 = P2 S6 = P1 S7 = P2 S7 = P1 S7 = P1 S7 = P2

[0037] Note that the clock phase associations for section **102***b* are the complements of the clock phase associations for section **102***a*. The complementary phasing of the two parallel sections **102***a*, **102***b* provides output ripple smoothing, more constant output drive current, and additional current capacity. Additional sections may be included to provide even more current capacity. Complimentary pairs of additional sections may be controlled by clock signal phases that are 180° apart and that have a different phase than P**1** or P**2** to provide even more output ripple smoothing (e.g., 45° or 60°—or multiples of those values—out of phase with respect to P**1** and P**2**).

[0038] In a FET-based implementation, ON/OFF control signals or clock phase signals are coupled to the gate of each switch S**1**-S**7** through at least a driver circuit, and in many cases through both a level shifter circuit and a driver circuit (see FIG. **2** for more details).

[0039] In either configuration, the non-overlapping complementary clock signals P**1**, P**2** open or close associated power switches, causing charge to be transferred from the fly capacitors C**1***a*, C**1***b*, C**2***a*, C**2***b* into C.sub.OUT, resulting in a voltage across C.sub.OUT of V.sub.IN/X, where X=2 or 3. Further details of the operation of this and similar DC-DC selectable conversion ratio power converters are set forth in U.S. Pat. No. 10,263,514 B1.

Limiting In-Rush Current During Soft-Starts

[0040] As noted above, damaging current spikes in power converters may occur for a variety of reasons, including in-rush current, charge transfer current, short circuits, and the like. For example, with respect to DC-DC power converters having selectable conversion ratios, switching from one conversion ratio (e.g., DIV2) to another conversion ratio (e.g., DIV3) may result in a charge imbalance across the fly capacitors, resulting in potentially damaging in-rush currents. Accordingly, a common practice for avoiding potentially damaging events has been to switch the DC-DC power converter OFF, allow the fly capacitors to discharge, change the conversion ratio configuration (e.g., by changing clock phasing to the switches S**1**-S**7** as needed), and turn the power back ON, relying on conventional startup circuitry to mitigate in-rush current spikes. A disadvantage of this practice is that the process can take several milliseconds to complete and cannot be completed under load.

[0041] One aspect of the present invention encompasses circuits and method for mitigating or eliminating potentially damaging events if they occur or are to occur (e.g., are known in advance, as when a conversion ratio is to be dynamically changed). Mitigating or eliminating potentially damaging events enables switching selectable conversion ratios DC-DC power converters from one conversion ratio to another conversion ratio under load without turning off the power converter circuitry or suspending switching of the charge pump power switches.

[0042] As described in U.S. patent application Ser. No. 17/331,594, it is desirable, and often necessary, to limit the current drawn by a power converter from an input supply during startup to avoid high in-rush currents, particularly when dynamically changing the conversion ratio of the power converter. Referring to FIG. **1**, a conceptual solution during a “soft-start” period before steady-state operation of the power converter **100** is to enable current sources **106***a*, **106***b*, respectively coupled to the sections **102***a*, **102***b*, and operate the switches S**2**-S**7** so as to allow the fly capacitors C**1***a*, C**1***b*, C**2***a*, C**2***b* to be charged by the current sources **106***a*, **106***b* to a sufficient state to prevent current spikes. More specifically, the current sources **106***a*, **106***b* may be coupled between V.sub.IN and a node between switches S**1** and S**2** that also couples to a respective fly capacitor C**1***a*, C**1***b*. Closing switch S**2** during the soft-start period also couples the current sources **106***a*, **106***b* to a respective fly capacitor C**2***a*, C**2***b*; switch S**1** is OPEN during the soft-start period when using the current sources **106***a*, **106***b* to limit current flow, and in essence all other switches run as normal. Hence, the power converter **100** is running as a charge pump but with limited current flow.

[0043] One way to implement the current sources **106***a*, **106***b* is by means of a power switch coupled in series with a resistor between V.sub.IN and the node between switches S**1** and S**2** (the power switch and resistor are thus coupled in parallel with switch S**1**). Closing the power switch creates a high resistive path during the soft-start period to limit the start-up current. Once the power converter output voltage V.sub.OUT nears its regulated value, the power switch is opened. However, such an implementation requires a very large FET for the power switch in order to withstand the voltage and current at startup, and thus requires a large amount of integrated circuit (IC) die area (as much as about 25% in some embodiments).

[0044] In U.S. patent application Ser. No. 17/331,594, it was realized that switch S**1** and its driver circuitry could be adapted to perform the functions of the current sources **106***a*, **106***b*, thus eliminating the need for additional large power switches and resistors. In particular, it was realized that the power converter switches S**1**-S**7** are normally operated in an "over-driven" or "full drive" condition when set to an ON (conducting) state. An overdriven FET gate creates a stronger conduction channel, effectively lowering the ON resistance, R.sub.ON, of the FET. With that insight, it was further realized that increasing R.sub.ON for some or all of the power FETs in a power converter (especially switch S**1**) during potentially damaging events (e.g., during startup or when dynamically re-configuring the conversion ratio of the power converter) reduces current flow through the FETs and thus protects against excessive current spikes.

[0045] FIG. **2** is a block diagram of one section **102***a* of a power converter **200** showing details for a FET implementation of the power switches S**1**-S**7** of that section. While section **102***a* is shown, a similar configuration exists for section **102***b*. In the illustrated example, power switches S**1**-S**7** are implemented as FETs M.sub.CP1-M.sub.CP7 (generically, "M.sub.CPx"). The gate of each FET M.sub.CPx is coupled to a level-shifter/driver block **202** (not all instances are numbered to avoid clutter). In some cases (e.g., power switches S**6** and S**7**), the level-shifter/driver block **202** may include only a driver, as level shifting may not be needed, depending upon the V.sub.IN and V.sub.OUT voltages. A level shifter translates an input signal from one voltage domain (e.g., digital logic voltages) to another voltage domain (e.g., transistor control voltages). The output of the level shifter thus follows the input signal but in a different voltage range. Power to each level-shifter/driver block **202** is provided by a corresponding LDO block **204**. A clock phase (P**1** or P**2** in this example) or an ON/OFF control signal may be coupled through a level-shifter/driver block **202** to the gate of the corresponding power FET M.sub.CPx.

[0046] As described in U.S. patent application Ser. No. 17/331,594, referenced above, at least some of the LDO blocks **204** can selectively increase R.sub.ON for an associated power FET in a power converter by actively controlling the driver voltage to the gate of the power FET. During normal power converter operation, the power FET driver voltage may be set to overdrive the FET gate to lower R.sub.ON to a desired level that allows high current flow for a particular application. However, for other scenarios (e.g., during soft-startup, charge balancing, or conversion ratio mode changes), the power FET driver voltage may be reduced so as to increase R.sub.ON and thus impede current flow through the power FET to a desired level.

LDO Power Supply Embodiment with Reduced Gate-Drive Capability

[0047] FIG. **3**A is a schematic diagram of one embodiment of the level-shifter/driver block **202** and the LDO block **204** of FIG. **2**. As in FIG. **2**, the LDO block **204** provides power to a level-shifter/driver block **202** coupled to the gate of an associated power FET M.sub.CPx. The input to the level-shifter/driver block **202**, φ.sub.x (e.g., either clock signal P**1** or clock signal P**2**, or an ON or OFF control signal), is applied to the input of a level shifter **302**. The output of the level shifter **302** is coupled to the input of a driver circuit **304**, the output of which is coupled to the gate of the associated FET M.sub.CPx. In the illustrated example, the driver circuit **304** includes a pre-driver

304*a* (comprising a set of three series-coupled inverters in this example) and a series-coupled final driver **304***b*. Internally, the final driver **304***b* has at least one NMOS FET n and one PMOS FET p with coupled conduction channels, drain-to-drain, with each FET n, p having a gate driven by the output of the pre-driver **304***a*. The drains of PMOS FET p and of NMOS FET n are coupled to the gate of the associated power FET M.sub.CPx. Note that for some embodiments, the level shifter **302** may be interposed after the pre-driver **304***a*, or between a pair of the inverters comprising the pre-driver **304***a*.
[0048] In some embodiments, the inverters may increase in physical size from inverter to inverter in order to provide sufficient current drive capability to charge or discharge the gate of FET M.sub.CPx. For example, in a driver circuit **304** having three series-coupled inverters in the pre-driver **304***a*, the first inverter may have a relative size of "1", the second inverter may be 3 times larger than the first inverter, and the third inverter may be 9 times larger than the first inverter. Lastly, the final driver **304***b* may be 27 times larger than the first inverter in the pre-driver **304***a*. The multipliers for the stages may differ from the 1×, 3×, 9×, and 27× ratios, although generally each stage is larger than the previous one to avoid having very slow rising and falling edges. In alternative embodiments, the number of inverter stages may be fewer or greater, and non-inverting stages (buffer amplifiers) may be used rather than inverting stages. Accordingly, the illustrated driver circuit **304** is exemplary only, and other circuits may be used to couple the output of the level shifter **302** to the gate of the associated FET M.sub.CPx.
[0049] Power to the level shifter **302** and the driver circuit **304** is provided by the LDO block **204**. In the illustrated example, the power source for the level shifter **302** and the pre-driver **304***a* is provided by a first LDO section **310**. The first LDO section **310** comprises a source follower (common drain) FET M.sub.LDO1 coupled between a capacitor C.sub.O1 and a supply voltage V.sub.DD-FGD. The capacitor C.sub.O1 is also coupled to a floating reference potential **308**. The source of the FET M.sub.LDO1 provides a drive voltage V.sub.LDO_OUT1 to the level shifter **302** and the pre-driver **304***a*.
[0050] A current source I.sub.BIAS1 is coupled in series with a Zener diode D**1** between a supply voltage V.sub.BIAS1 and the reference potential **308**. A current source may be configured from transistors and/or diodes using a variety of circuits, as well as a pull-up resistor. One terminal of the Zener diode D**1** is coupled to the gate of FET M.sub.LDO1. A resistor R**1** and a capacitor C**1** are coupled in parallel with the Zener diode D**1**. The resistor R**1** serves to discharge the gate of FET M.sub.LDO1 when transitioning M.sub.LDO1 from an ON state to an OFF state. Since the output of the LDO block **204** drives a switching circuit, there is potential for noise to be coupled to the gate of M.sub.LDO1 which may modulate the output drive voltage V.sub.LDO_OUT1. Such noise is mitigated by capacitor C**1**. Alternative embodiments may use a push-pull drive to the gate of M.sub.LDO1.
[0051] The output of the current source V.sub.BIAS1 before the Zener diode D**1** provides an essentially constant bias voltage to the gate of FET M.sub.LDO1. The bias current I.sub.BIAS1 flows through the Zener diode D**1** and ensures that the diode is always in reverse bias. Unlike a conventional diode that blocks any flow of current through itself when reverse biased, as soon as the reverse voltage reaches a pre-determined value, a Zener diode begins to conduct. This applied reverse voltage remains almost constant even with large changes in current (so long as the current remains between a breakdown minimum current and a maximum current rating for the Zener diode). A Zener diode continues to regulate its voltage until the holding current of the diode falls below the minimum current value in the reverse breakdown region.
[0052] The final driver **304***b* is powered by a second LDO section **312** that includes a FET M.sub.LDO2 having its conduction channel (between drain and source) coupled between a supply voltage V.sub.DD-RGD and the final driver **304***b*. The gate of FET M.sub.LDO2 is coupled to a separate gate driver circuit that is independent of the gate driving circuitry for FET M.sub.LDO1. A principal function of the gate driver circuit of the second LDO section **312** is to enable at least two

different voltage levels at Node A to be coupled to the gate of FET M.sub.LDO2, which in turn determines the output voltage level V.sub.GATE provided by the final driver **304***b* driving the associated power FET M.sub.CPx. The associated power FET M.sub.CPx thus can be placed into (1) an overdriven or "full gate-drive" ON state having low R.sub.ON for normal power converter operation, or (2) at least one current-limiting reduced gate-drive ON state having a higher R.sub.ON and/or being in a saturation mode whereby current is limited. Saturation mode looks like an increased R.sub.ON but is not quite the same—in saturation mode, the FET M.sub.CPx behaves like an ON-OFF switch that can only pass a maximum fixed current regardless of applied voltage, while a resistor implies that a greater voltage allows a greater current. The current-limiting state is selected to provide protection against potentially damaging events (e.g., in-rush or charge transfer current). Potentially damaging eventsmay occur during dynamic re-configuration of the conversion ratio of the power converter, during power converter startup, when balancing charge among fly capacitors within the power converter, or during fault events such as short circuit events.

[0053] A resistor R**2** and a capacitor C**2** are coupled in parallel with the Zener diode D**2** and function in essentially the same manner as resistor R**1** and capacitor C**1**. A reservoir capacitor C.sub.O2 is coupled between the source of FET M.sub.LDO2 and the floating reference potential **308**, and provides some initial charge to the gate of the FET M.sub.CPx as well as isolation from the floating reference potential **308**.

[0054] The gate driver circuit for FET M.sub.LDO2 includes a variable current source I.sub.BIAS2 coupled in series with a Zener diode D**2** between a supply voltage V.sub.BIAS2 and the reference potential **308**. The gate of FET M.sub.LDO2 is coupled to Node A between the current source I.sub.BIAS2 and the Zener diode D**2**. The output of the current source I.sub.BIAS2 before the Zener diode D**2** at Node A provides an essentially constant bias voltage V.sub.GS_SE to the gate of FET M.sub.LDO2. The source of FET M.sub.LDO2 provides a drive voltage V.sub.LDO_OUT2 to the final driver **304***b*.

[0055] In parallel with the Zener diode D**2** is a voltage control circuit **314** comprising a reduced gated-drive P-type FET switch M.sub.SW series-coupled to a first diode-connected FET M.sub.D0 and at least one additional diode-connected FET M.sub.DN, where N≥1. The gate of FET switch M.sub.SW is coupled to a switch control block **316** that is coupled to an ENABLE signal EN.sub.RGD; details of the switch control block **316** are discussed below.

[0056] The conduction channels of the first diode-connected FET M.sub.D0 and the at least one additional diode-connected FET MIN are coupled in series. As illustrated, the conduction channel of the switch FET switch M.sub.SW is coupled between Node A and the conduction channel of the first diode-connected FET M.sub.D0. The conduction channel of the last-in-series additional diode-connected FET M.sub.DN is coupled to the floating reference potential **308**. Note that the switch FET switch M.sub.SW may be positioned anywhere along the voltage control circuit **314** to interrupt or enable current flow through that circuit. However, positioning the FET switch M.sub.SW as shown in FIG. **3** may reduce parasitic influences on FET M.sub.LDO2 due, for example, to the capacitances of diode-connected FETs M.sub.D0 and/or M.sub.DN.

[0057] A function of the diode-connected FET M.sub.D0 is to offset FET M.sub.LDO2, since the threshold voltages of FET M.sub.D0 and FET M.sub.LDO2 effectively cancel. A function of the additional diode-connected FETs M.sub.DN is to set the current I.sub.MAIN through FET M.sub.CPx in proportion to the ratio of the sizes of FET M.sub.CPx to FET M.sub.DN when FET switch M.sub.SW is CLOSED and the current mirror function of the voltage control circuit **314** is engaged. More particularly, the current I.sub.MAIN through FET M.sub.CPx is proportional to the current from the current source I.sub.BIAS2 and the size ratio of FET M.sub.DN to FET M.sub.CPx. For example, if the current source I.sub.BIAS2 output is 1 mA, and FET M.sub.CPx is 1,000 times the size of FET M.sub.DN (W/L M.sub.CPx=1000×W/L M.sub.DN), then the maximum current through FET M.sub.CPx will be 1,000×1 mA=1 A. This is achieved by ensuring the gate-to-source voltage V.sub.GS of FET M.sub.DN is the same as that of FET M.sub.CPx. The maximum gate voltage of FET M.sub.CPx is the voltage at Node A minus the threshold voltage V.sub.TH of FET M.sub.LDO2. Including FET M.sub.D0 increases the voltage at Node A by a second threshold voltage V.sub.GS, so the voltage at Node A=(V.sub.GS of FET M.sub.DN)+(V.sub.TH of FET M.sub.D0), or 2V.sub.GS. If FET M.sub.LDO2 and FET M.sub.D0 are matched (ratiometrically), then the maximum the V.sub.GS of FET M.sub.CPx can reach is the same as the V.sub.GS of FET M.sub.DN, and this equality tracks over process, temperature, etc.

[0058] As noted, the diode-connected FET(s) M.sub.DN are ratioed in size with respect to FET M.sub.CPx. In some embodiments, FETs M.sub.LDO1, M.sub.LDO2, M.sub.D0, and M.sub.CPx may be segmented FETs, meaning that a device intended to function as a large FET is fabricated as multiple (e.g., 10,000) small FETs coupled in parallel (the individual small FETs may be called “fingers”, reflecting typical aspects of their physical layout on an IC die). The diode-connected FET(s) M.sub.D0, M.sub.DN may be fabricated using the same technology, but can be made with a much smaller number of FET fingers (e.g., as few as one finger). Because of the configuration of FET M.sub.LDO2 and the final driver **304***b*, a small change in current flow through the voltage control circuit **314** affecting the voltage V.sub.GS_SF at the gate of FET M.sub.LDO2 causes a proportionally larger current flow I.sub.MAIN through power FET M.sub.CPx determined by the size ratio of FET M.sub.CPx to FET M.sub.DN.

[0059] Adding more than one diode-connected FET M.sub.DN allows adjustment of the size ratio of FET M.sub.CPx to FET M.sub.DN. For instance, if FET M.sub.CPx has a width of 100 and 1,000 fingers, a first FET M.sub.DN should also have a width of 100 to match, but may only have 1 finger. Hence the size ratio of FET M.sub.DN to FET M.sub.CPx is 1,000 to 1, and 1 mA from the current source I.sub.BIAS2 means 1 A through FET M.sub.CPx. To change the size ratio to 2,000 to 1, two diode-connected FETs MON may be coupled in series (source to drain). If the FET width is still 100, the effective number of fingers of the two diode-connected FETs M.sub.DN is one-half, giving a size ratio of 2,000 to 1 with respect to FET M.sub.CPx.

[0060] As noted above, an important function of the gate driver circuit is that it provides a selectable amount of regulated gate bias voltage V.sub.GS_SF to FET M.sub.LDO2, which in turn controls the power supply to, and voltage output of, the final driver **304***b*. When FET switch M.sub.SW is OPEN, then the voltage control circuit **314** is disconnected from Node A—and therefore from the gate of FET M.sub.LDO2—and thus has essentially no effect on the output of FET M.sub.LDO2; accordingly, the final driver **304***b* can fully overdrive the gate of FET M.sub.CPx to a selected level determined by the Zener diode D**2**.

[0061] When FET switch M.sub.SW is CLOSED—such as during startup of the power converter or when dynamically switching conversion ratios or rebalancing charge amount fly capacitors—then the voltage control circuit **314** operates as a bypass to divert current around diode D**2** and lower the voltage at Node A, thus reducing the drive voltage to FET M.sub.LDO2. The reduced gate-drive voltage to FET M.sub.LDO2 in turn reduces the power to the final driver **304***b* and thus reduces the gate-drive voltage V.sub.GATE to the power FET M.sub.CPx. Accordingly, FET M.sub.CPx receives a reduced gate-drive voltage that results in an increased R.sub.ON value and/or limited saturation current compared to the full overdriven state. That increased limitation of current flow through at least some of the power FETs M.sub.CPx of a power converter may inhibit excessive current spikes, thus protecting the power FETs (as well as other coupled circuitry) from large voltage spikes. Selectively varying the I.sub.BIAS2 current controls the value of V.sub.GATE applied to the power FET M.sub.CPx, thus enabling selection of different current flow limitations.

[0062] In some embodiments, reduced gate-drive operation of a power FET M.sub.CPx in the ON state to limit current spikes during potentially damaging events may be enabled (triggered) by a control circuit (not shown) as a function of a measured parameter, such as the value of V.sub.IN, V.sub.OUT, pump capacitor voltages, or load current, and/or as the result of sensed events, such as short circuit events and/or charge imbalances on the pump capacitors. In some embodiments, reduced gate-drive operation of a power FET M.sub.CPx in the ON state to limit current spikes during potentially damaging events may be enabled (triggered) based on an external ENABLE signal EN.sub.GRD for FET switch M.sub.SW that is asserted in advance of a known impending event, such as dynamic switching of conversion ratios.

[0063] The duration of reduced gate-drive operation for the power FETs may be set as a fixed time suitable for a particular application or may be determined based on some criteria. For example, reduced gate-drive operation for the power FETs may be a function of output load, or a function of output load and a selected maximum duration (i.e., a time-out parameter), or a function of the voltage across the fly capacitors having reached some percentage (e.g., 95%) of a desired target level, or some combination of these values and/or the values of other parameters.

[0064] An advantage of using diode-connected FETs in the voltage control circuit **314** fabricated using the same technology as the power FETs M.sub.CPx (e.g., NMOSFET) is that the devices should essentially have matching characteristics with respect to process/voltage/temperature (PVT) variations.

[0065] In summary, a principal function of the gate driver circuit for FET M.sub.LDO2 is to enable at least two different voltage levels at Node A to be coupled to the gate of FET M.sub.LDO2. More specifically, the voltage control circuit **314** can selectably shift the voltage at Node A between a first voltage level, in which the voltage control circuit **314** is not engaged (FET switch M.sub.SW is OPEN) and at least a second voltage level, in which the voltage control circuit **314** is engaged (FET switch M.sub.SW is CLOSED).

[0066] It should be appreciated that the second LDO section **312** illustrated in FIG. **3**A is simple to implement, requiring little power and circuit area. However, other devices or circuits that provide the same or similar function may be used in other embodiments. For example, Node A could be coupled through FET switch M.sub.SW to an amplifier having a level-shifted reference voltage as an input.

[0067] Note that the LDO block **204** of FIG. **3**A, including the second LDO section **312**, may be used to power all of the FET switches in a power converter **100** to limit currents through such switches as may be needed (for example, when dynamically changing the conversion ratio of the power converter **100**). In some instances, a level shifter **302** circuit may not be required for some FET switches (e.g., power switches S**5** and S**7** in FIG. **1**), in which case ox may be applied directly to the associated pre-driver **304***a*. In such a case, LDO section **310** may not be needed, and LDO section **312** may be used to drive the pre-drivers **304***a*, thus saving IC area. Note also that the LDO block **204** may be used to provide a regulated power supply to other types of target circuit, and not just to a level-shifter/driver block **202**.

[0068] FIG. **3**B is a block diagram showing details of one embodiment of a switch control block **316**. The switch control block **316** is coupled to components of the voltage control circuit **314** as shown, and includes a NFET M having a first end of its conduction channel coupled by a resistor Ra to node A, and a second end of its conduction channel coupled to the floating reference potential **308**. The drain of NFET M is coupled to the gate of the P-type FET switch M.sub.SW. A switch Sw, a current source I.sub.BIAS, and a resistor Rb are coupled in series as shown between a voltage V.sub.BIAS and the floating reference potential **308**. The gate of NFET M is coupled between the current source I.sub.BIAS and the resistor Rb. In an alternative embodiment, a standard level shifter may be used to drive the gate of FET switch M.sub.SW, but possibly at the cost of larger IC area.

[0069] In operation, if the ENABLE signal EN.sub.RGD is a logical “1”, then switch Sw closes, causing and NFET M to conduct and pull the gate of P-type FET switch M.sub.SW down to the floating reference potential **308**. The result is an application of a negative V.sub.GS to the P-type FET switch M.sub.SW, thus setting M.sub.SW to a conductive state (i.e., closing the switch). Conversely, if the ENABLE signal EN.sub.RGD is a logical “0”, then switch Sw opens and NFET M does not conduct; accordingly, the V.sub.GS to the P-type FET switch M.sub.SW will be zero, thus setting M.sub.SW to a non-conductive state (i.e., opening the switch).

LDO Supply Voltages

[0070] The LDO block **204** for each power switch S**1**-S**7** in FIG. **2** requires at least one voltage supply. In FIG. **3**A, four voltage sources are shown, V.sub.BIAS1, V.sub.DD-FGD, V.sub.BIAS2, and V.sub.DD-RGD. In some embodiments, V.sub.BIAS1 and V.sub.BIAS2 may have the same value. In some embodiments, V.sub.DD-FGD and V.sub.DD-RGD may have the same value. In some embodiments, combination that V.sub.BIAS1 and V.sub.BIAS2, and V.sub.DD-FGD and V.sub.DD-RGD may have different values.

[0071] Each LDO block **204** should generate a voltage, V.sub.GATE, sufficient to switch the associated power FET M.sub.CPx. For a FET implementation of power switch S**1**, since the drain voltage to M.sub.CP1 is V.sub.IN, the corresponding gate voltage V.sub.GATE should equal or exceed V.sub.IN plus the V.sub.GS of the FET M.sub.CP1. Accordingly, V.sub.DD-FGD and V.sub.DD-RGD for the LDO block **204** coupled to the level-shifter/driver block **202** for power FET M.sub.CP1 should ultimately provide this value of V.sub.GATE. The voltages V.sub.DD-FGD and V.sub.DD-RGD may be supplied by external circuitry coupled to each section **102***a*, **102***b* that provides a voltage V.sub.BOOST1 that is greater than V.sub.IN, such as 3V to 5V above V.sub.IN. Each such external circuit may comprise, for example, a simple charge pump coupled to a boot capacitor. In the simplest implementation, the voltage supplies V.sub.DD-FGD and V.sub.DD-RGD for power switches S**2**-S**7** may be V.sub.BOOST1 or V.sub.IN (since such switches are at voltage levels less than V.sub.IN).

[0072] Since V.sub.DD-FGD and V.sub.DD-RGD for power switch S**1** are set to V.sub.BOOST1, which is greater than V.sub.IN, the gate voltages to the FETs M.sub.LDO1-M.sub.LDO2 should be greater than V.sub.BOOST1 in order to properly switch ON. Accordingly, V.sub.BIAS1 and V.sub.BIAS2 may be provided by external circuitry coupled to each section **102***a*, **102***b* to provide a voltage V.sub.BOOST2 that is greater than V.sub.BOOST1, such as V.sub.IN +5.5V. Each such external circuit may comprise, for example, a simple charge pump coupled to a boot capacitor. In the simplest implementation, the voltage supplies V.sub.BIAS1 and V.sub.BIAS2 for power switches S**2**-S**7** may be V.sub.BOOST2 or V.sub.IN (since such switches are at lower voltage levels).

[0073] FIG. **4** is a schematic block diagram of one embodiment of a charge pump **400**. Separate instance of the charge pump **400** may be used to generate V.sub.BOOST1 and V.sub.BOOST2 (generically, “V.sub.BOOSTx”). The clock signals P**1** and P**2** are complementary and non-overlapping phases, while the/P**1** and/P**2** clock signals are inverted versions of P**1** and P**2**. PFET M**1** and NFET M**3** conduct and block charge flow at the same times, while NFET M**2** and PFET M**4** conduct and block charge flow at the same times (but complementary to PFET M**1** and NFET M**3**). FETs M**1** and M**2** and FETs M**4** and M**3** are respectively coupled in series between a voltage source V.sub.DD and a relative circuit ground. A cross-coupled set of FET pairs (NFET M**5** and PFET M**6** on the left, NFET M**8** and PFET M**7** on the right) is coupled between V.sub.IN and a capacitor C.sub.OUT, which in turn is coupled to the relative circuit ground. Toggling of the P**1** and P**2** clocks signals (and their complementary versions) periodically connects V.sub.IN through FETs M**5** and M**8** to the “top” plates of capacitors C.sub.A and C.sub.B, thus charging those capacitors to V.sub.IN, and then periodically connects V.sub.DD through FETs M**1** and M**4** to the “bottom” plates of capacitors C.sub.A and C.sub.B, thus adding V.sub.DD on the fly to V.sub.IN. In greater detail, in a first phase, capacitor C.sub.A is charged to V.sub.IN through switches M**5** and M**2** in closed (ON) states, or capacitor C.sub.B is charged to V.sub.IN through switches M**8** and M**3** in closed states. In a second phase, capacitor C.sub.A is discharged to the output with a voltage of V.sub.BOOSTx=V.sub.IN+V.sub.DD through switches M**1** and M**6** in closed states, or capacitor C.sub.B is discharged to the output with a voltage of V.sub.BOOSTx=V.sub.IN+V.sub.DD through switches M**4** and M**7** in closed states.

[0074] Referring back to FIG. **2**, it should be appreciated that the different power switches S**1**-S**7** are subjected to different voltage ranges, and that only power switch S**1** needs to withstand

V.sub.IN when in an OFF state. The remaining power switches S**2**-S**7** can be designed to withstand lower voltage levels. The present invention recognizes that basing the V.sub.GATE voltage to all of the lower-level power switches S**2**-S**7** on V.sub.BOOST1 or V.sub.IN is inefficient, since those supply voltages are higher than needed to switch the lower-level power FETs. Accordingly, one aspect of the present invention is the utilization of internal voltage nodes of the power converter itself to supply V.sub.DD-FGD and V.sub.DD-RGD in order to efficiently power the lower-level power switches S**2**-S**7**. A complicating factor in using such internal voltage nodes is that the division ratio of the power converter may be dynamically switched, which affects the voltage available at some of the utilized internal voltage nodes because of the change of switching phases for some power FETs (e.g., power switch S**2**). Further, during transitions between DIV2 and DIV3 operation, an incorrect LDO configuration can cause cascading effects that can damage the power converter. Accordingly, another aspect of the present invention is an adaptive circuit architecture that functionally allows dynamic switching between different voltage supply sources for the LDOs powering the level shifters **302** and pre-drivers **304***a* and for the LDOs powering the final drivers **304***b*.

Source-Switching LDOs

[0075] FIG. **5**A is a block diagram of one embodiment of a “source switching” LDO **502** configured to provide regulated power to a level shifter/pre-driver **504** (comparable to the level shifter **302** and pre-driver **304***a* of FIG. **3**A) and a final driver **506** (comparable to the final driver **304***b* of FIG. **3**A), both coupled to a floating reference potential **308** referenced to the source of the associated power FET M.sub.CPx. The illustrated LDO **502** includes dual full gate-drive LDO sections **508***a*, **508***b*, and dual reduced gate-drive LDO sections **510***a*, **510***b*. Full gate-drive LDO section **508***a* and reduced gate-drive LDO section **510***a* are operational when the power converter is in a DIV2 configuration and generate respective outputs V.sub.LDO_OUT1_DIV2 and V.sub.LDO_OUT2_DIV2. Full gate-drive LDO section **508***b* and reduced gate-drive LDO section **510***b* are operational when the power converter is in a DIV3 configuration and generate respective outputs V.sub.LDO_OUT1_DIV3 and V.sub.LDO_OUT2_DIV3.

[0076] As illustrated, the outputs of the dual full gate-drive LDO sections **508***a*, **508***b* may be directly connected (a “wired-OR” or multiplex connection) to the level shifter/pre-driver **504**, as shown, or coupled through a switch (not shown). Similarly, the outputs of the dual reduced gate-drive LDO sections **510***a*, **510***b* may be directly connected to the final driver **506**. For power FETs M.sub.CPx for which a reduced gate-drive voltage is not needed or desired, the LDO **502** may include only the dual full gate-drive LDO sections **508***a*, **508***b*, and V.sub.LDO_OUT1_DIV2 and V.sub.LDO_OUT1_DIV3 would be connected directly to the final driver **506** by a conductor **512** (shown as a dashed line).

[0077] FIG. **5**B is a block diagram of the dual full gate-drive LDO sections **508***a*, **508***b* of FIG. **5**A, showing greater detail. As a comparison with FIG. **3**A indicates, each full gate-drive LDO section **508***a*, **508***b* is essentially an instance of the full gate-drive LDO section **310** of FIG. **3**A, the only differences being that LDO section **508***a* is supplied by a first voltage V.sub.DD-FGD1 while LDO section **508***b* is supplied by a second voltage V.sub.DD-FGD2.

[0078] In DIV3 mode, the I.sub.BIAS1b current to full gate-drive LDO section **508***b* is turned ON while the I.sub.BIAS1a current to full gate-drive LDO section **508***a* is turned OFF. The gates of FET M.sub.LDO1 in full gate-drive LDO section **508***a* is pulled down by corresponding resistor R**1** to a floating ground. FET M.sub.LDO1 in LDO section **508***a* is OFF, and M.sub.LDO1 in LDO section **508***b* is ON, providing power to the associated level shifter/pre-driver **504** (and in some cases, to the final driver **506**). In DIV2 mode, the reverse configuration is presented, with the I.sub.BIAS1a current to full gate-drive LDO section **508***a* being turned ON while the I.sub.BIAS1b current to full gate-drive LDO section **508***a* is turned OFF. Consequently, full gate-drive LDO section **508***a* provides power to the associated level shifter/pre-driver **504** (and in some cases, to the final driver **506**) and full gate-drive LDO section **508***b* is OFF.

[0079] FIG. **5**C is a block diagram of the dual reduced gate-drive LDO sections **510***a*, **510***b* of FIG. **5**A, showing greater detail. As a comparison with FIG. **3**A indicates, each reduced gate-drive LDO section **510***a*, **510***b* is essentially an instance of the reduced gate-drive LDO section **312** of FIG. **3**A, the only differences being that LDO section **510***a* is supplied by a first voltage V.sub.DD-RGD1 while LDO section **510***b* is supplied by a second voltage V.sub.DD-RGD2.

[0080] In DIV3 mode, the I.sub.BIAS1b current to full gate-drive LDO section **510***b* is turned ON while the I.sub.BIAS1a current to full gate-drive LDO section **510***a* is turned OFF. Accordingly, V.sub.GS_SF in reduced gate-drive LDO section **510***b* is set by I.sub.BIAS2 to that section, and V.sub.GS_SE in reduced gate-drive LDO section **510***a* is pulled down by corresponding resistor R**2** to a floating ground. FET M.sub.LDO2 in LDO section **510***a* is OFF, and FET M.sub.LDO2 in LDO section **510***b* is ON, providing power to the associated final driver **506**. In DIV2 mode, the reverse configuration is presented, with the I.sub.BIAS2a current to reduced gate-drive LDO section **510***a* being turned ON while the I.sub.BIAS2b current to reduced gate-drive LDO section **510***a* is turned OFF. Consequently, reduced gate-drive LDO section **510***a* provides power to the associated final driver **506** and reduced gate-drive LDO section **510***b* is OFF.

[0081] FIG. **5**D is a block diagram of an alternative embodiment of the dual reduced gate-drive LDO sections **510***a*, **510***b* of FIG. **5**A. In the illustrated embodiment, one instance **520** of each of the variable current source I.sub.BIAS2, the voltage control circuit **314**, and the diode D**2** is shared by means of a switch Sw with either a DIV2 circuit **522***a* or a DIV3 circuit **522***b*. The state of the switch Sw would be determined by the control circuitry (not shown) that reconfigures the power converter between the DIV2 and DIV3 modes of operation. Setting switch Sw to couple diode D**2** to the DIV2 circuit **522***a* essentially creates a first reduced gate drive circuit, while setting switch Sw to couple diode D**2** to the DIV3 circuit **522***b* essentially creates a second reduced gate drive circuit.

[0082] Keeping in mind that a power converter generally has two parallel sections **102***a*, **102***b* (see FIG. **1**), the type of LDO and the voltage supplies to the LDO associated with each power FET M.sub.CPx can be selected for high efficiency. For example, the LDO for power switch S**1** in both parallel sections **102***a*, **102***b* preferably is of the type shown in FIG. **3**A, since a reduced gate-drive capability is generally needed to limit in-rush current but support of “source switching” is not required. The V.sub.DD inputs to the full gate-drive LDO section **310** and the reduced gate-drive LDO section **312** may all be supplied by a V.sub.BOOST1 circuit, as described above, since changing division ratios for the power converter is not a factor. In some embodiments, it may be useful to “wire-OR” the outputs of the V.sub.BOOST1 circuits to to save IC area. The V.sub.BIAS inputs to the full gate-drive LDO section **310** and the reduced gate-drive LDO section **312** may be supplied by a V.sub.BOOST2 circuit, as described above.

[0083] As another example, the LDOs for power switches S**6** and S**7** in both parallel sections **102***a*, **102***b* may be just instances of the first LDO section **310** of FIG. **3**A, since a reduced gate-drive capability is generally not needed to limit in-rush current and support of “source switching” is not required. The V.sub.DD input to the LDO sections **310** may all be supplied by the V.sub.X node voltage. The V.sub.BIAS inputs to the to the LDO sections **310** may all be supplied by a V.sub.BOOST1 circuit, as described above.

[0084] In an efficient implementation of a power converter, some of the power FET switches may require dual gate-drive LDO circuits in order to support “source switching”. For example, power switches S**2** and S**4** may use different power supply sources for DIV2 versus DIV3 operational modes for better efficiency. In particular, the V.sub.DD-FGD1 and V.sub.DD-RGD1 sources in DIV2 mode for power switch S**2** in section **102***a* of a power converter may come from the V.sub.BOOST1 circuit of the other section **102***b* of the power converter. Conversely, the V.sub.DD-FGD1 and V.sub.DD-RGD1 sources in DIV3 mode for the power switch S**2** in section **102***a* of the power converter may come from the V.sub.BOOST1 circuit coupled to the same section **102***a*.

[0085] As another example, the V.sub.DD-FGD1 and V.sub.DD-RGD1 sources in DIV2 mode for the power switch S**4** in section **102***a* of a power converter may come from the V.sub.C1b node of the other section **102***b* of the power converter. Conversely, the V.sub.DD-FGD1 and V.sub.DD-RGD1 sources in DIV3 mode for the power switch S**4** in section **102***a* of the power converter may come from the V.sub.C1b node of the same section **102***a*.

[0086] TABLE 2 below shows one set of LDO types and assignments of voltage sources that may be used in conjunction with an efficient power converter. "FGD/RGD" means a full gate-drive/reduced gate-drive LDO of the type shown in FIG. **3**A. "FGD" means just the full gate-drive LDO section **310** shown in FIG. **3**A (no RGD LDO needed). "Dual FGD/Dual RGD" means a dual full gate-drive/dual reduced gate-drive LDO of the type shown in FIG. **5**A. "Dual FGD" means just the dual full gate-drive LDOs **508***a*, **508***b* shown in FIG. **5**A (no RGD LDOs needed). "Same section" means the section **102***a*, **102***b* in which a switch is located. "Other section" means the section **102***a*, **102***b* in which a switch is not located (e.g., if a switch is located in section **102***a*, then section **102***b* would be the "other section").

TABLE-US-00002 TABLE 2 DIV2 Voltage DIV3 Voltage Sources for Sources for V.sub.DD-FGD1 & V.sub.DD-FGD2 & Switch LDO Type V.sub.DD-RGD1 V.sub.DD-RGD2 S1 FGD/RGD V.sub.BOOST1 same V.sub.BOOST1 same section section S2 Dual FGD or V.sub.BOOST1 same V.sub.BOOST1 other Dual FGD/ section or section or Dual RGD V.sub.C2 other section V.sub.C2 other section S3 FGD/RGD or V.sub.C1 other section V.sub.C1 other section FGD S4 Dual FGD or V.sub.C1 same section V.sub.C1 same section Dual FGD/ Dual RGD S5 FGD or FGD/ V.sub.C1 same section V.sub.C1 same section RGD S6 FGD or FGD/ V.sub.X same section V.sub.X same section RGD S7 FGD or FGD/ V.sub.X same section V.sub.X same section RGD

[0087] Note that for power switch S**2** in DIV2 mode, the voltage source could be "V.sub.C2 other section". However, using "V.sub.BOOST1 same section" provides more headroom across pass transistors since "V.sub.BOOST1 same section" is greater than "V.sub.C2 other section", and may have other advantages.

ENHANCED EMBODIMENTS

[0088] In some applications using "source switching" dual gate-drive LDOs, situations may arise that affect performance or even cause damage due to the "wired-OR′ing" of two LDO outputs, as shown in FIG. **5**A.

[0089] As a first example, at high values of V.sub.IN, a problem may occur in the LDOs for power switch S**2** (FET M.sub.CP2). More specifically, when in the DIV2 mode, the DIV3 side **508***b* of a dual full gate-driver LDO or the DIV3 side **510***b* of a dual reduced gate-driver LDO—either of which should be OFF in the DIV2 mode for power switch S**2**—may be turned ON at high values of V.sub.IN, creating an undesired discharge path through the DIV3 side circuitry.

[0090] For example, FIG. **6** is a schematic diagram of dual full gate-drive LDO sections **508***a*, **508***b* in a DIV2 configuration for power switch S**2**. V.sub.BIAS1 on the DIV3 side **508***b* is zero, and thus the gate of FET M.sub.LDO1 in the DIV3 side **508***b* is pulled down to the floating ground, which is V.sub.IN for power switch S**2**. However, if V.sub.IN is greater than 2*V.sub.Z (the voltage drop across the Zener diodes D**1**), then FET M.sub.LDO1 in the DIV3 side **508***b* switches to an ON state (assuming that V.sub.TH=0V for FET M.sub.LDO1 in this example). Accordingly, current passing through FET M.sub.LDO1 in the DIV2 side **508***a* may discharge through path **602**, leaving no or inadequate voltage for the associated level shifter/pre-driver **504** and/or final driver **506**. Note that while FIG. **6** shows dual full gate-drive LDO sections **508***a*, **508***b*, the same problem exists for dual reduced gate-drive LDO sections **510***a*, **510***b*.

[0091] FIG. **6** shows a solution to this problem in the form of an added FET pull-up switch M.sub.PU (inside dotted oval **604**) on the DIV3 side **508***b*. The conduction channel of FET pull-up switch M.sub.PU is coupled between the gate of DIV3-side FET M.sub.LDO1 and the voltage source coupled to the drain of DIV3-side FET M.sub.LDO1 (V.sub.DD-FGD2 in this example). The gate of FET pull-up switch M.sub.PU is coupled to the gates of DIV3-side FET M.sub.LDO1. FET pull-up switch Mpy turns ON when V.sub.IN>2*V.sub.Z and pulls the gates of DIV3-side FET

M.sub.LDO1 to “V.sub.BOOST1 other” (which is greater than V.sub.IN), thus assuring that DIV3-side FET M.sub.LDO1 is OFF at high values of V.sub.IN, thereby closing off the discharge path **602**.

[0092] As a second example of a situation that may arise that affects performance or even causes damage, during DIV3 to DIV2 mode switching, the DIV3 side **508***b* of a dual full gate-driver LDO or the DIV3 side **510***b* of a dual reduced gate-driver LDO may not fully turn OFF before the corresponding DIV2 side turns ON, which can cause shoot-through which may damage the power converter.

[0093] For example, FIG. **7**A is a schematic diagram of dual reduced gate-drive LDO sections **510***a*, **510***b* for an LDO transitioning from a DIV3 to a DIV2 mode. FIG. **7**B is a set of graphs of current and voltage as a function of time for a dual reduced gate-drive LDO depicting the issue of ON-time overlap. Note that while FIG. **7**A shows dual full gate-drive LDO sections **508***a*, **508***b*, the same problem exists for dual reduced gate-drive LDO sections **510***a*, **510***b*.

[0094] Referring to FIG. **7**B, when the bias current I.sub.BIAS_DIV3 to the DIV3-side of a dual full gate-driver LDO is high, then the gate voltage V.sub.GS_SF_DIV3 to the DIV3-side FET M.sub.LDO2 is high and that FET conducts (i.e., the DIV3 side is ON). When the bias current I.sub.BIAS_DIV2 to the DIV2-side of a dual full gate-driver LDO is low, then the gate voltage Vas SF DIV2 to the DIV2-side FET M.sub.LDO2 is low and that FET conducts (i.e., the DIV2 side is OFF). Without a corrective circuit, when the dual full gate-driver LDO switches from DIV3 mode to DIV2 mode, the gate of the DIV3-side FET M.sub.LDO2 takes an appreciable time (the C**2***R**2** time constant for the DIV3 side) to discharge as the FET transitions from ON to OFF. Thus, there is a period of time when both the DIV3-side and the DIV2-side of the dual full gate-driver LDO are ON. Accordingly, current passing through the DIV2-side FET M.sub.LDO2 may discharge through path **702**, leaving no or inadequate voltage for the associated level shifter/pre-driver **504** and/or final driver **506**.

[0095] To resolve this potential problem, a fast-discharge switch MED (inside dotted oval **704**) is added with its conduction channel coupled to node A and a floating ground. The gate of the fast-discharge switch MED would be coupled to a control signal CTRL that sets MED to an ON (conductive) state during DIV3 to DIV2 transitions, thus enabling the gate of the DIV3-side FET M.sub.LDO2 to quickly discharge. The result is that the DIV3 side quickly turns OFF before the DIV2 side turns ON, ensuring no overlap between the LDO ON states and eliminating the possible discharge path **702**. FIG. **7**C is a set of graphs of current and voltage as a function of time for a dual reduced gate-drive LDO that includes the fast-discharge switch MED of FIG. **7**A. During a transition from a DIV3 mode to a DIV2 mode, control circuitry (not shown) would assert the CTRL signal, thus turning MED ON and thereby coupling the gates of the DIV3-side FET M.sub.LDO2 to the floating ground, consequently rapidly discharging those gates. Accordingly, the DIV3-side FET M.sub.LDO2 quickly turns OFF before the DIV2-side FET M.sub.LDO2 turns ON.

[0096] It should be appreciated that a dual gate-drive LDO embodiment may include both the fast-discharge switch MED of FIG. **7**A and the pull-up switch M.sub.PU of FIG. **6**. The use of a fast-discharge switch MED and/or a pull-up switch M.sub.PU with “wired-OR” connections of “source switching” dual gate-drive LDOs avoids having to place extra switches in the output paths of the LDO sections, which increases efficiency.

Benefits

[0097] Embodiments of the present invention may some or all of the following advantages: a current limiting value that is independent of a power converter switching frequency, device mismatches and process, voltage, and/or temperature (PVT) variations; accurate soft-start current limiting; reliable operation of power FETs in power converters having reconfigurable conversion ratios when dynamically changing conversion ratios; the ability to keep a level output voltage when a power converter operates at full load in different operating and PVT conditions; and high efficiency through the use of existing voltage nodes within a power converter to power specific power FETs.

Circuit Embodiments

[0098] Circuits and devices in accordance with the present invention may be used alone or in combination with other components, circuits, and devices. Embodiments of the present invention may be fabricated as integrated circuits (ICs), which may be encased in IC packages and/or in modules for ease of handling, manufacture, and/or improved performance. In particular, IC embodiments of this invention are often used in modules in which one or more of such ICs are combined with other circuit components or blocks (e.g., filters, amplifiers, passive components, and possibly additional ICs) into one package. The ICs and/or modules are then typically combined with other components, often on a printed circuit board, to form part of an end-product such as a cellular telephone, laptop computer, or electronic tablet, or to form a higher-level module which may be used in a wide variety of products, such as vehicles, test equipment, medical devices, etc. Through various configurations of modules and assemblies, such ICs typically enable a mode of communication, often wireless communication.

[0099] As one example of further integration of embodiments of the present invention with other components, FIG. **8** is a top plan view of a substrate **800** that may be, for example, a printed circuit board or chip module substrate (e.g., a thin-film tile). In the illustrated example, the substrate **800** includes multiple ICs **802***a*-**802***d* having terminal pads **804** which would be interconnected by conductive vias and/or traces on and/or within the substrate **800** or on the opposite (back) surface of the substrate **800** (to avoid clutter, the surface conductive traces are not shown and not all terminal pads are labelled). The ICs **802***a*-**802***d* may embody, for example, signal switches, active filters, amplifiers (including one or more LNAs), and other circuitry. For example, IC **802***b* may incorporate one or more instances of an enhanced LDO power supply circuit like the circuits shown in FIGS. **3**A, **5**A-**5**D, **6**, and/or **7**A.

[0100] The substrate **800** may also include one or more passive devices **806** embedded in, formed on, and/or affixed to the substrate **800**. While shown as generic rectangles, the passive devices **806** may be, for example, filters, capacitors, inductors, transmission lines, resistors, planar antennae elements, transducers (including, for example, MEMS-based transducers, such as accelerometers, gyroscopes, microphones, pressure sensors, etc.), batteries, etc., interconnected by conductive traces on or in the substrate **800** to other passive devices **806** and/or the individual ICs **802***a*-**802***d*. The front or back surface of the substrate **800** may be used as a location for the formation of other structures.

System Aspects

[0101] Embodiments of the present invention are useful in a wide variety of applications, including portable computing devices (e.g., laptops, notebooks, cell phones, tablets), datacenters and telecom centers that have battery backup systems, household appliances and electronics, vehicles (e.g., automobiles, drones, planes, boats, trains, ships), general purpose DC/DC and AC/DC power converters, and radio frequency (RF) circuits and systems.

[0102] Radio system usage may include wireless RF systems (including base stations, relay stations, and hand-held transceivers) that use various technologies and protocols, including various types of orthogonal frequency-division multiplexing ("OFDM"), quadrature amplitude modulation ("QAM"), Code-Division Multiple Access ("CDMA"), Time-Division Multiple Access ("TDMA"), Wide Band Code Division Multiple Access ("W-CDMA"), Global System for Mobile Communications ("GSM"), Long Term Evolution ("LTE"), 5G, 6G, and WiFi (e.g., 802.11a, b, g, ac, ax, be) protocols, as well as other radio communication standards and protocols.

Methods

[0103] Another aspect of the invention includes methods providing power to at least one voltage input node of a target circuit. For example, FIG. **9** is a process flow chart **900** showing a method of providing power to a voltage input node of a target circuit. The method includes: coupling a first low-dropout circuit between a first voltage source and the voltage input node of the target circuit, the first low-dropout circuit including a first transistor (e.g., FET) circuit configured to selectively apply a first voltage to the voltage input node of the target circuit [Block **902**]; and coupling a second low-dropout circuit between a second voltage source and the voltage input node of the target circuit, the second low-dropout circuit including a second transistor (e.g., FET) circuit configured to selectively apply a second voltage to the voltage input node of the target circuit [Block **904**].

[0104] For example, FIG. **10** is a process flow chart **1000** showing a method of providing power to a voltage input node of a driver circuit for a power FET having a gate, and to the gate of the power FET. The method includes: coupling a first low-dropout circuit between a first voltage source and the voltage input node of the driver circuit, the first low-dropout circuit including a first FET circuit configured to selectively apply a first voltage to the voltage input node of the driver circuit [Block **1002**]; coupling a second low-dropout circuit between a second voltage source and the voltage input node of the driver circuit, the second low-dropout circuit including a second FET circuit configured to selectively apply a second voltage to the voltage input node of the driver circuit [Block **1004**]; coupling a first reduced-drive low-dropout circuit between a third voltage source and the gate of the power FET, the first reduced-drive circuit including a third FET circuit configured to selectively apply at least a third voltage or a lower fourth voltage to the gate of the power FET such that current flow through the power FET in an ON state is higher when the third voltage is applied and lower when the lower fourth voltage is applied [Block **1006**]; and coupling a second reduced-drive low-dropout circuit between a fourth voltage source and the gate of the power FET, the second reduced-drive circuit including a fourth FET circuit configured to selectively apply at least a fifth voltage or a lower sixth voltage to the gate of the power FET such that current flow through the power FET in an ON state is higher when the fifth voltage is applied and lower when the lower sixth voltage is applied [Block **1008**].

[0105] Additional aspects of the above methods may include one or more of the following: wherein the first voltage source is the same as the second voltage source; wherein the first voltage source is different from the second voltage source; wherein the third voltage source is the same as the fourth voltage source; wherein the third voltage source is different from the fourth voltage source; selectively applying one of the lower fourth voltage or the lower sixth voltage to restrict flow of excess current through the power FET; wherein the first FET circuit or the third FET circuit of at least one of the first full-drive low-dropout circuit or the first reduced-drive low-dropout circuit includes a FET having a gate, and further including coupling a conduction channel of a pull-up FET between the gate of the FET and a respective one of the first voltage source or the third voltage source, and coupling a gate of the pull-up FET to the gate of the FET; wherein the first FET circuit or the third FET circuit of at least one of the first full-drive low-dropout circuit or the first reduced-drive low-dropout circuit includes a FET having a gate, and further including coupling a conduction channel of a fast-discharge FET between the gate of the FET and a reference potential, coupling a gate of the fast-discharge FET to a control signal, and selectively asserting the control signal to cause the fast-discharge FET to discharge the gate of the FET; and/or wherein the first reduced-drive low-dropout circuit and the second reduced-drive low-dropout circuit each include a voltage control circuit, wherein each voltage control circuit includes a switch, a first diode-connected FET, and at least one additional diode-connected FET, wherein the switch, the first diode-connected FET, and the at least one additional diode-connected FET are coupled in series between a reference potential and the respective first or second FET circuit.

Fabrication Technologies & Options

[0106] FIGS. **5**B and **5**C show the LDO sections as being “wired-OR” to a level shifter/pre-driver, final driver, or power FET gate on the source side of the FETs M.sub.LDO1 or M.sub.LDO2. In alternative embodiments of power converters implemented with P-type FETs (PFETs), the LDO sections may be essentially “flipped” upside-down and implemented with PFETs to provide a suitable polarity output voltage from the drain side of the FETs. Thus, for example, the ground connection shown in FIGS. **5**B and **5**C would become a positive voltage rail V.sub.IN, and the various voltage sources (e.g., V.sub.BIAS1, V.sub.BIAS2, V.sub.DD-FGD1, V.sub.DD-FGD2, V.sub.DD-RGD1, and V.sub.DD-RGD2) would be negative voltages with respect to V.sub.IN. The current sources would become current sinks, and the polarity of the diodes D**1**, D**2** would be reversed (e.g., cathode coupled to V.sub.IN). The "wired-OR" connection to a level shifter/pre-driver, final driver, or power FET gate would be from the drain side of the FETs within the LDO sections. Otherwise, operation remains essentially the same as an N-type FET embodiment. As should be apparent, the circuits of FIGS. **5**D, **6**, and **7**A may also be implemented with PFETs.

[0107] The term "MOSFET", as used in this disclosure, includes any field effect transistor (FET) having an insulated gate whose voltage determines the conductivity of the transistor, and encompasses insulated gates having a metal or metal-like, insulator, and/or semiconductor structure. The terms "metal" or "metal-like" include at least one electrically conductive material (such as aluminum, copper, or other metal, or highly doped polysilicon, graphene, or other electrical conductor), "insulator" includes at least one insulating material (such as silicon oxide or other dielectric material), and "semiconductor" includes at least one semiconductor material.

[0108] As used in this disclosure, the term "radio frequency" (RF) refers to a rate of oscillation in the range of about 3 kHz to about 300 GHz. This term also includes the frequencies used in wireless communication systems. An RF frequency may be the frequency of an electromagnetic wave or of an alternating voltage or current in a circuit.

[0109] With respect to the figures referenced in this disclosure, the dimensions for the various elements are not to scale; some dimensions may be greatly exaggerated vertically and/or horizontally for clarity or emphasis. In addition, references to orientations and directions (e.g., "top", "bottom", "above", "below", "lateral", "vertical", "horizontal", etc.) are relative to the example drawings, and not necessarily absolute orientations or directions.

[0110] Various embodiments of the invention can be implemented to meet a wide variety of specifications. Unless otherwise noted above, selection of suitable component values is a matter of design choice. Various embodiments of the invention may be implemented in any suitable integrated circuit (IC) technology (including but not limited to MOSFET structures), or in hybrid or discrete circuit forms. Integrated circuit embodiments may be fabricated using any suitable substrates and processes, including but not limited to standard bulk silicon, high-resistivity bulk CMOS, silicon-on-insulator (SOI), and silicon-on-sapphire (SOS). Unless otherwise noted above, embodiments of the invention may be implemented in other transistor technologies such as BJT, BiCMOS, LDMOS, BCD, GaAs HBT, GaN HEMT, GaAs pHEMT, and MESFET technologies. However, embodiments of the invention are particularly useful when fabricated using an SOI or SOS based process, or when fabricated with processes having similar characteristics. Fabrication in CMOS using SOI or SOS processes enables circuits with low power consumption, the ability to withstand high power signals during operation due to FET stacking, good linearity, and high frequency operation (i.e., radio frequencies up to and exceeding 300 GHz). Monolithic IC implementation is particularly useful since parasitic capacitances generally can be kept low (or at a minimum, kept uniform across all units, permitting them to be compensated) by careful design.

[0111] Voltage levels may be adjusted, and/or voltage and/or logic signal polarities reversed, depending on a particular specification and/or implementing technology (e.g., NMOS, PMOS, or CMOS, and enhancement mode or depletion mode transistor devices). Component voltage, current, and power handling capabilities may be adapted as needed, for example, by adjusting device sizes, serially "stacking" components (particularly FETs) to withstand greater voltages, and/or using multiple components in parallel to handle greater currents. Additional circuit components may be added to enhance the capabilities of the disclosed circuits and/or to provide additional functionality without significantly altering the functionality of the disclosed circuits.

CONCLUSION

[0112] A number of embodiments of the invention have been described. It is to be understood that various modifications may be made without departing from the spirit and scope of the invention. For example, some of the steps described above may be order independent, and thus can be performed in an order different from that described. Further, some of the steps described above may be optional. Various activities described with respect to the methods identified above can be executed in repetitive, serial, and/or parallel fashion.

[0113] It is to be understood that the foregoing description is intended to illustrate and not to limit the scope of the invention, which is defined by the scope of the following claims, and that other embodiments are within the scope of the claims. In particular, the scope of the invention includes any and all feasible combinations of one or more of the processes, machines, manufactures, or compositions of matter set forth in the claims below. (Note that the parenthetical labels for claim elements are for ease of referring to such elements, and do not in themselves indicate a particular required ordering or enumeration of elements; further, such labels may be reused in dependent claims as references to additional elements without being regarded as starting a conflicting labeling sequence).

Claims

1. A dual low-dropout circuit configuration including: (a) a first low-dropout circuit including a first transistor circuit configured to be coupled between a first voltage source and a target circuit, the first low-dropout circuit configured to selectively apply a first voltage to a voltage input node of the target circuit; and (b) a second low-dropout circuit including a second transistor circuit configured to be coupled between a second voltage source and the target circuit, the second low-dropout circuit configured to selectively apply a second voltage to the voltage input node of the target circuit.