

US Patent & Trademark Office

Patent Public Search | Text View

United States Patent	12395246
Kind Code	B2
Date of Patent	August 19, 2025
Inventor(s)	Kalman; Robert et al.

Optically-enhanced multichip packaging

Abstract

Optical chip-to-chip interconnects may use microLEDs as light sources. The interconnected chips may be on a same substrate. A pair of endpoint chips may each have associated optical transceiver subsystems, with transceiver circuitry in transceiver chips. Optical communications may be provided between the optical transceiver subsystems, with the optical transceiver subsystems in communication with their associated endpoint chips by way of metal layers in the substrate.

Inventors: Kalman; Robert (Menlo Park, CA), Pezeshki; Bardia (Menlo Park, CA), Tselikov; Alexander (Sunnyvale, CA), Danesh; Cameron (Sunnyvale, CA)

Applicant: AvicenaTech Corp. (Sunnyvale, CA)

Family ID: 1000008764697

Assignee: AvicenaTech, Corp. (Sunnyvale, CA)

Appl. No.: 18/215056

Filed: June 27, 2023

Prior Publication Data

Document Identifier	Publication Date
US 20230344518 A1	Oct. 26, 2023

Related U.S. Application Data

continuation parent-doc US 17229652 20210413 US 11728894 child-doc US 18215056
us-provisional-application US 63009161 20200413

Publication Classification

Int. Cl.: H04B10/40 (20130101); **G02B6/42** (20060101); **G02B6/43** (20060101); **H04B10/50** (20130101)

U.S. Cl.:

CPC H04B10/40 (20130101); **G02B6/4246** (20130101); **G02B6/43** (20130101); **H04B10/502** (20130101);

Field of Classification Search

CPC: H04B (10/40); H04B (10/502); G02B (6/4246); G02B (6/43)

References Cited

U.S. PATENT DOCUMENTS

Patent No.	Issued Date	Patentee Name	U.S. Cl.	CPC
4422088	12/1982	Gfeller	385/16	G02B 6/42
5335361	12/1993	Ghaem	N/A	N/A
5638469	12/1996	Feldman et al.	N/A	N/A
5848214	12/1997	Haas et al.	N/A	N/A
6160943	12/1999	Davis et al.	N/A	N/A
6236786	12/2000	Aoki	385/14	G02B 6/43
6330377	12/2000	Kosemura	385/47	H04B 10/801
6434308	12/2001	Trezza	385/115	G02B 6/4249
6780661	12/2003	Liu	N/A	N/A
7459726	12/2007	Kato et al.	N/A	N/A
7539366	12/2008	Baks	385/33	G02B 6/4201
7619441	12/2008	Rahman	326/38	H03K 19/17796
7915699	12/2010	Krishnamoorthy et al.	N/A	N/A
8148202	12/2011	Krishnamoorthy et al.	N/A	N/A
11054593	12/2020	Chua	N/A	N/A
2002/0018628	12/2001	Kim et al.	N/A	N/A
2003/0185484	12/2002	Chakravorty et al.	N/A	N/A
2004/0126053	12/2003	Ouchi	385/14	G02B 6/12004
2004/0159777	12/2003	Stone	250/216	G02B 6/4246
2004/0208416	12/2003	Chakravorty	385/14	G02B 6/43
2005/0141823	12/2004	Han	385/89	G02B 6/4204
2005/0169591	12/2004	Broeng	385/129	G02B 6/13
2006/0008223	12/2005	Gunn, III et al.	N/A	N/A
2007/0297713	12/2006	Lu et al.	N/A	N/A

2009/0212317	12/2008	Kolodin	257/E21.511	H01L 25/0753
2013/0111744	12/2012	Tischler et al.	N/A	N/A
2013/0230280	12/2012	Kadar-Kallen	N/A	N/A
2013/0230650	12/2012	Lee	427/163.2	G02B 6/43
2014/0327902	12/2013	Giger	356/5.01	G01S 17/08
2015/0333831	12/2014	Lai	250/208.2	G02B 6/428
2015/0341119	12/2014	Fincato	398/139	H05K 3/30
2016/0020353	12/2015	Chu	N/A	N/A
2016/0170120	12/2015	Shani et al.	N/A	N/A
2016/0172020	12/2015	Baker et al.	N/A	N/A
2016/0233269	12/2015	Choi et al.	N/A	N/A
2017/0276874	12/2016	Kashyap et al.	N/A	N/A
2018/0052281	12/2017	Kuo	N/A	G02B 6/1221
2018/0239096	12/2017	Houbertz et al.	N/A	N/A
2018/0269191	12/2017	England et al.	N/A	N/A
2019/0011652	12/2018	Chang	N/A	N/A
2019/0049367	12/2018	Zou	N/A	N/A
2019/0066571	12/2018	Goward	N/A	N/A
2019/0137703	12/2018	Heroux et al.	N/A	N/A
2019/0189603	12/2018	Wang et al.	N/A	N/A
2019/0287908	12/2018	Dogiamis	N/A	H01P 3/121
2020/0111771	12/2019	Su et al.	N/A	N/A

FOREIGN PATENT DOCUMENTS

Patent No.	Application Date	Country	CPC
109904141	12/2018	CN	N/A
110718593	12/2020	CN	N/A
2002-101051	12/2001	JP	N/A
2011-014932	12/2010	JP	N/A

OTHER PUBLICATIONS

Bamiedakis et al. “Ultra-Low Cost High-Density Two-Dimensional Visible-Light Optical Interconnects”, Journal of Lightwave Technology, vol. 37, No. 13, Jul. 1, 2019, pp. 3305-3314. cited by applicant

Brusberg et al., “Optoelectronic Glass Substrate for Co-packaged Optics and ASICs”, Optical Fiber Communication Conference, Mar. 12, 2020, San Diego, CA, pp. 1-24. cited by applicant

Carreira et al., “Direct integration of Micro-LEDs and a SPAD Detector on a Silicon CMOS Chip for Data Communications and Time-of-Flight Ranging”, Optics Express, vol. 28, No. 5, Mar. 2, 2020, pp. 6909-6917. cited by applicant

Corbett et al., “Chapter Three—Transfer Printing for Silicon Photonics, Semiconductors and Semimetals”, vol. 99, 2018, ISSN 0080-8784, pp. 43-70. cited by applicant

Dangel et al., “Polymer Waveguides Enabling Scalable Low-Loss Adiabatic Optical Coupling for Silicon Photonics”, IEEE Journal of Selected Topics In Quantum Electronics, vol. 24, No. 4, Jul./Aug. 2018, 11 pages. cited by applicant

Dawson, “Micro-LEDs for Technological Convergence Between Displays, Optical Communications, & Sensing and Imaging Systems”, SID Display Week 2020, Session 44, Invited paper No. 44.1, 27 pages. cited by applicant

Extended European Search Report from the European Patent Office in related EP Application No. 21787727.3 dated Aug. 1, 2023. cited by applicant

International Search Report on related PCT Application No. PCT/US2021/027135 from International Searching Authority (KIPO) dated Jul. 26, 2021. cited by applicant

Lee et al., “Low-Cost and Robust 1-Gbit/s Plastic Optical Fiber Link Based on Light-Emitting Diode Technology”, in Proc. Opt. Fiber Commun. Conf. Expo./Nat. Fiber Opt. Eng. Conf., 2008. cited by applicant

Liu et al., “On-Chip Optical Interconnect on Silicon by Transfer Printing”, In: CLEO: Science and Innovations 2018, San Jose, California, USA, May 13-18, 2018, pp. 1-2. cited by applicant

Miller, “Optical Interconnects”, IAA Workshop, Jul. 22, 2008, pp. 1-26. cited by applicant

Vlasov, “Silicon Photonics for Next Generation Computing Systems”, Tutorial given at the European Conference on Optical Communications, Sep. 22, 2008. cited by applicant

Wang et al., “On-chip Optical Interconnects using InGaN Light-Emitting Diodes Integrated with Si-CMOS”, In: AAIS Communications and Photonics Conference 2014, Shanghai, China, Nov. 11-14, 2014, pp. 1-3. cited by applicant

Written Opinion on related PCT Application No. PCT/US2021/027135 from International Searching Authority (KIPO) dated Jul. 26, 2021. cited by applicant

Yahav et al., “Multi-Gigabit Spatial-Division Multiplexing Transmission Over Multicore Plastic Optical Fiber”, Journal of Lightwave Technology, vol. 39, No. 8, Apr. 15, 2021, pp. 2296-2304. cited by applicant

Zhang et al., “Hybrid Photonic Integration on a Polymer Platform”, Photonics 2015, 2, pp. 1005-1026. cited by applicant

Office Action issued by China National Intellectual Property Administration (“CNIPA”) in related Chinese Patent Application No. 202180033921.6 dated Apr. 27, 2025. cited by applicant

Primary Examiner: Barua; Pranesh K

Background/Summary

CROSS-REFERENCE TO RELATED APPLICATIONS (1) This application is a Continuation Application of U.S. application Ser. No. 17/229,652, filed on Apr. 13, 2021, which claims the benefit of the filing date of U.S. Provisional Patent Application No. 63/009,161, filed on Apr. 13, 2020, the disclosures of each of which are incorporated by reference herein.

FIELD OF THE INVENTION

(1) The present invention relates generally to optical communication systems, and more generally to optical communications between chips using microLEDs.

BACKGROUND OF THE INVENTION

(2) Computing and networking performance requirements are seemingly ever-increasing. Prominent applications driving these requirements include data center servers, high-performance computing clusters, artificial neural networks, and network switches.

(3) For decades, dramatic integrated circuit (IC) performance and cost improvements were driven by shrinking transistor dimensions combined with increasing die sizes, summarized in the famous Moore's Law. Transistor counts in the billions have allowed consolidation onto a single system-on-a-chip (SoC) of functionality that was previously fragmented across multiple ICs.

(4) However, Moore's Law appears to be reaching its limits as shrinking feature sizes below 10 nm results in decreasing marginal performance benefits with decreased yields and increased per-transistor costs. Beyond these limitations, a single IC can only contain so much functionality, and

that functionality is constrained because the IC's process cannot be simultaneously optimized for different functionality, e.g. logic, DRAM, and I/O.

(5) There are significant benefits to “de-integrating” SoCs into smaller “chiplets”, including:

(6) The process for each chiplet can be optimized to its function, e.g. logic, DRAM, high-speed I/O, etc.

(7) Chiplets are well-suited to reuse in multiple designs.

(8) Chiplets are less expensive and quicker to develop.

(9) Chiplets have higher yield because they contain fewer devices.

(10) There is, however, a major drawback to chiplets compared to SoCs: use of chiplets generally requires far more chip-to-chip connections. Compared to the on-chip connections between functional blocks in SoCs, chip-to-chip connections are typically much less dense and require far more power (for example normalized as energy per bit).

BRIEF SUMMARY OF THE INVENTION

(11) Some embodiments provide optical chip-to-chip interconnects with microLEDs as light sources. In some embodiments the interconnects have a linear connection density >10 Tbps/mm. In some embodiments the interconnects have an area interconnect density >1 Pbps/cm². In some embodiments the interconnects have power consumption <100 fJ/bit. In some embodiments the interconnects have an interconnect lengths >10 cm with no additional power dissipation. In some embodiments the interconnects have a latency approaching that limited by the speed of light.

(12) In some embodiments the microLEDs are modulated at rates >1 Gbps. In some embodiments parallel optical links (POLs) include microLEDs as light sources. In some embodiments the parallel optical links provide interconnect networks for high-performance processing and networking applications.

(13) Some embodiments provide optically interconnected integrated circuits, comprising: a substrate; a first integrated circuit (IC) chip, including logic circuitry, mounted to the substrate; a first optical transceiver subsystem mounted to the substrate; a second optical transceiver subsystem mounted to the substrate; a second IC chip, including logic circuitry, mounted to the substrate; the substrate including metal signal layers connecting the first IC chip and the first optical transceiver subsystem, and connecting the second IC chip and the second optical transceiver subsystem; and a plurality of waveguide cores optically connecting the first optical transceiver subsystem and the second optical transceiver subsystem.

(14) In some embodiments the substrate includes metal signal layers connecting the first IC chip and the second IC chip. In some embodiments the substrate does not include metal signal layers connecting the first IC chip and the second IC chip. In some embodiments the substrate is in a package. In some such embodiments the substrate is coupled to the package by solder balls. In some such embodiments the substrate includes first through-substrate vias connecting at least some of the solder balls coupling the substrate and package with the first IC chip. In some such embodiments the substrate includes second through-substrate vias connecting at least some other of the solder balls coupling the substrate and package with the second IC chip.

(15) In some embodiments the first optical transceiver subsystem comprises a first array of microLEDs and photodetectors, first microLED driver circuitry to drive microLEDs, of the first array of microLEDs and photodetectors, to emit light in accordance with information from the first IC chip, and first receiver circuitry to process signals received by photodetectors, of the first array of microLEDs and photodetectors, to provide information to the first IC chip. In some such embodiments the first microLED driver circuitry and the receiver circuitry is in a first transceiver IC chip. In some such embodiments the first microLED driver circuitry comprises a first array of microLED driver circuitry and the first receiver circuitry comprises a first array of receiver circuitry. In some such embodiments the microLEDs, of the first array of microLEDs and photodetectors, are bonded to the first transceiver IC chip. In some such embodiments the photodetectors, of the first array of microLEDs and photodetectors, are monolithically integrated in

the first transceiver IC chip. In some such embodiments the first array of microLEDs and photodetectors are arranged in tiles.

(16) In some embodiments the first optical transceiver subsystem comprises a first array of microLEDs and photodetectors, first microLED driver circuitry to drive microLEDs, of the first array of microLEDs and photodetectors, to emit light in accordance with information from the first IC chip, and first receiver circuitry to process signals received by photodetectors, of the first array of microLEDs and photodetectors, to provide information to the first IC chip, and the second optical transceiver subsystem comprises a second array of microLEDs and photodetectors, second microLED driver circuitry to drive microLEDs, of the second array of microLEDs and photodetectors, to emit light in accordance with information from the second IC chip, and second receiver circuitry to process signals received by photodetectors, of the second array of microLEDs and photodetectors, to provide information to the second IC chip. In some such embodiments the first microLED driver circuitry and the receiver circuitry is in a first transceiver IC chip, and the second microLED driver circuitry and the receiver circuitry is in a second transceiver IC chip. In some such embodiments the second microLED driver circuitry comprises a second array of microLED driver circuitry and the second receiver circuitry comprises a second array of receiver circuitry. In some such embodiments the microLEDs, of the second array of microLEDs and photodetectors, are bonded to the second transceiver IC chip. In some such embodiments the photodetectors, of the first second of microLEDs and photodetectors, are monolithically integrated in the second transceiver IC chip. In some such embodiments the second array of microLEDs and photodetectors are arranged in tiles.

(17) In some embodiments wherein the plurality of waveguide cores are part of a multi-layer planar waveguide stack.

(18) In some embodiments the first optical transceiver subsystem comprises a first array of microLEDs and photodetectors, first microLED driver circuitry to drive microLEDs, of the first array of microLEDs and photodetectors, to emit light in accordance with information from the first IC chip, and first receiver circuitry to process signals received by photodetectors, of the first array of microLEDs and photodetectors, to provide information to the first IC chip, and the plurality of waveguide cores are cores of a multicore fiber. In some such embodiments the multicore fiber is a coherent imaging fiber. In some such embodiments the cores are sufficiently small and closely spaced such that light from each microLED will form a spot spanning multiple cores.

(19) In some embodiments the first optical transceiver subsystem comprises a first array of microLEDs and photodetectors, first microLED driver circuitry to drive microLEDs, of the first array of microLEDs and photodetectors, to emit light in accordance with information from the first IC chip, and first receiver circuitry to process signals received by photodetectors, of the first array of microLEDs and photodetectors, to provide information to the first IC chip, and the plurality of waveguide cores are cores of a multicore fiber, and further comprising a turning mirror optically between the first array of microLEDs and photodetectors and the multicore fiber. Some such embodiments further comprise at least one lens optically between the first array of microLEDs and photodetectors and the multicore fiber.

(20) These and other aspects of the invention are more fully comprehended upon review of this disclosure.

Description

BRIEF DESCRIPTION OF THE FIGURES

(1) FIG. 1 is a block diagram showing an electrical architecture of a first optically-interconnected IC, in accordance with aspects of the invention.

(2) FIG. 2a shows a substrate with optoelectronic (OE) devices coupled to a transceiver IC by way

of direct bonds, in accordance with aspects of the invention.

(3) FIG. 2*b* shows a substrate with OE devices coupled to a transceiver IC by way of solder balls, in accordance with aspects of the invention.

(4) FIG. 2*c* shows OE devices monolithically integrated into a transceiver IC, in accordance with aspects of the invention.

(5) FIGS. 3*a-c* show different physical configurations for implementing a transceiver subsystem, in accordance with aspects of the invention.

(6) FIG. 4 shows integration of planar optical links within a package, in accordance with aspects of the invention.

(7) FIG. 5 shows integration of optical links within an interposer and package, in accordance with aspects of the invention.

(8) FIGS. 6*a-e* show various optoelectronic device configurations, in accordance with aspects of the invention.

(9) FIG. 7*a* shows a cross-sectional view of a multicore fiber, in accordance with aspects of the invention.

(10) FIG. 7*b* shows a cross-sectional view of coherent imaging fiber, with an exploded view of a portion of the fiber, in accordance with aspects of the invention.

(11) FIG. 7*c* shows a multi-layer planar waveguide stack, in accordance with aspects of the invention.

(12) FIG. 8*a* shows a hole in a substrate that allows an optical connection to traverse to the other side of the substrate, in accordance with aspects of the invention.

(13) FIG. 8*b* shows an example of use of a transparent substrate, in accordance with aspects of the invention.

(14) FIG. 9*a* show an optoelectronic (OE) subassembly in accordance with aspects of the invention.

(15) FIG. 9*b* shows an MW subassembly, in accordance with aspects of the invention.

(16) FIG. 9*c* shows the use of a turning mirror to turn a light beam by ninety degrees, in accordance with aspects of the invention.

(17) FIG. 9*d* shows the use of two turning mirrors to turn a light beam by one hundred eighty degrees, in accordance with aspects of the invention.

DETAILED DESCRIPTION

(18) FIG. 1 is a block diagram showing an electrical architecture including a first optically-interconnected IC. The IC includes IC circuitry **111** for performing logic and/or other functions. Transceiver circuitry **113** is coupled to the IC circuitry. The transceiver circuitry comprises, and in some embodiments consists of, an array of microLED driver circuitry **115** and an array of receiver circuitry **117**. The transceiver circuitry is part of a transceiver subsystem **119**. The transceiver subsystem also includes an array of microLEDs **121** and photodetectors **123**. In some embodiments the transceiver circuitry may be monolithically integrated into the same IC containing the endpoint IC circuitry. In some embodiments the transceiver circuitry or may be contained in one or more separate transceiver ICs. The microLED driver circuitry drives the array of microLEDs to emit light **125** to carry information provided to the driver circuitry from the endpoint IC circuitry. An N-bit wide unidirectional parallel bus connection may be implemented with N optical links from the transceiver subsystem to a second IC (not shown in FIG. 1), or, in some embodiments, a plurality of second ICs. A corresponding unidirectional parallel bus may be implemented by adding N additional optical links from the transceiver subsystem of the second IC to the transceiver subsystem of the first IC. The photodetectors receive light **127** from the corresponding parallel bus, the light carrying information from the second IC. The photodetectors provide electrical signals carrying the received information to the receiver circuitry, which processes the signals and provides the information to the endpoint IC circuitry.

(19) The optoelectronic (OE) devices, for example the microLEDs and photodetectors, may include

structures that enhance optical coupling efficiency. For instance, microLEDs may include various structures that improve the light extract efficiency (LEE), including surface roughening, particular LED shapes, and encapsulation in high-index materials. They may also include structures such as mirrors and lenses that collect the light from the LED's large intrinsic emission solid angle into a smaller solid angle that is better matched to the numerical aperture of the rest of the optical link. MicroLEDs are amenable to this reduction of angular cone due to their small size and thus relatively small etendue.

(20) In some embodiments the OE devices can be integrated with the transceiver IC through hybrid integration techniques. FIG. 2a shows an embodiment in which the hybrid integration technique is direct bonding. In FIG. 2a, a substrate with OE devices **211** is coupled to a transceiver IC **213** by way of direct bonds **215**. FIG. 2b shows an embodiment in which the hybrid integration technique is solder bump bonding. In FIG. 2b, the substrate with OE devices **211** is coupled to the transceiver IC **213** by way of solder bumps **217**. In some embodiments OE devices **221** can be monolithically integrated into a transceiver IC **223**, as illustrated in FIG. 2c. The viability of monolithic integration may be strongly dependent on the IC material and the source wavelength. Silicon generally supports monolithic integration of photodetectors for wavelengths $<1\text{ }\mu\text{m}$ but may be not viable for monolithic optical source integration because it is an indirect bandgap material. By contrast, GaAs, InP, and GaN support monolithic integration of both photodetectors and optical sources. It is possible to mix monolithic and hybrid integration on a single transceiver IC. For instance, a transceiver IC may include microLEDs that are directly bonded to the IC along with monolithically-integrated photodiodes.

(21) The transceiver subsystem can be implemented in a number of different physical configurations, for example as illustrated in FIGS. 3a-c. The configurations include a substrate, which may be rigid or flexible. Rigid substrate materials include silicon, glass, and laminates that include epoxy or resin. Flexible substrates may be made from various polymers.

(22) In FIG. 3a, a first transceiver IC **311a** is mounted to the top of a substrate **313** with an active side facing up. A first OE device **315a** is on top of the transceiver IC. The first transceiver IC in some embodiments is a very thin “micro-IC” that is only a few tens of microns thick. Electrical connections from a first endpoint IC (not shown in FIG. 3a) to the first transceiver IC are made by deposited metal traces **316** that traverse the top of the substrate, and the side and top surfaces of the first transceiver IC. The first OE device is shown on the active side of the first transceiver IC. The first OE device receives signals from and/or provides signals to the first transceiver IC. The first OE device is shown as embedded or encapsulated in a waveguide core **317**. The waveguide core extends to a second transceiver IC **311b**, with waveguide cladding **319** being shown as on top of the substrate between the first and second transceiver ICs. A second OE device **315b** is shown as on an active side of the second transceiver IC, with the second OE device also shown as embedded or encapsulated in the waveguide core. The second transceiver IC and the second OE may be as discussed with respect to the first transceiver IC and the first OE. As with the first transceiver IC, the second transceiver IC has electrical connections from a second endpoint IC (not shown in FIG. 3a). The first and second transceiver ICs, OE devices, and waveguide therefore may provide for optical communications substantially between the first endpoint IC and the second endpoint IC.

(23) In FIG. 3b, the transceiver ICs **311a,b** are placed in a cavity in the substrate **313**. A material may be used to fill any gaps between the ICs and the substrate. This, for example, allows planar electrical connections from the substrate to the ICs. As with FIG. 3a, the OE devices **315a,b** are on top of the transceiver ICs.

(24) In FIG. 3c, the transceiver ICs **311a,b** are mounted to the substrate **313** with their active sides facing down. Such may simplify electrical connections from the substrate to the transceiver ICs. In FIG. 3c, part of each of the transceiver ICs containing the OE devices **315a,b** hangs over a cavity in the substrate. The OE devices are on the bottom of the transceiver ICs, in the cavity in the substrate.

(25) For the embodiments of FIGS. 3a-c, the wave guide cores may be an array of planar optical waveguides, for example comprised of a bottom cladding and an array of cores, each of which guides light from a microLED at one end to a photodetector at the other end. Alternatively, both a microLED and photodetector can be located at both ends of each waveguide. This enables bidirectional transmission through each waveguide, supporting a duplex link.

(26) In the embodiments of FIGS. 3a-c, a waveguide cladding layer is deposited in an appropriate region of the substrate. A layer of waveguides cores is fabricated on top of (or below for FIG. 3c) the cladding layer in a manner such that each OE device is encased in a separate waveguide core.

(27) FIG. 4 shows integration of planar optical links within a package. A first endpoint IC 411a is mounted to pads on a package 413 by way of solder bumps 415. Some pads connect to traces in metal signal layers 417 of the package (or a substrate 418 of the package), providing connection to a first transceiver subsystem 419a. The first transceiver subsystem may be as discussed previously. One or more waveguide cores 421 couple the first transceiver subsystem to a second transceiver subsystem 419b, which may also be as discussed previously. For example, the waveguide cores may be separated from substrate by waveguide cladding 423. The second transceiver subsystem is connected to a second endpoint IC 411b, also by traces in metal signal layers of the package (or a substrate of the package). In FIG. 4, the metal signal layers of the package do not provide for electrical communications between the first endpoint IC and the second endpoint IC, although in some embodiments such may be additionally provided.

(28) FIG. 5 shows the integration of planar optical links within an interposer and package. A first endpoint IC 511a is mounted to pads on the interposer 513 with solder bumps 515. Some of the pads connect to through-substrate vias (TSVs) 517 that, in turn, connect to the package 519 via solder bumps. Other pads of the interposer connect to traces in metal signal layers 520 of the interposer providing connection to a first transceiver subsystem 521a. The first transceiver subsystem may be as discussed previously. One or more waveguide cores 523 couple the first transceiver subsystem to a second transceiver subsystem 521b, which may also be as discussed previously. The second transceiver subsystem is connected to a second endpoint IC 511b, also by traces in metal signal layers of the interposer. In FIG. 5, the metal signal layers of the interposer provide for electrical communications between the first endpoint IC and the second endpoint IC, although in some embodiments such is not provided.

(29) FIGS. 2a-c showed examples of optoelectronic devices integrated onto the active side of an IC. In a vertically-launched parallel optical link (VLPOL), a 2D array of OE devices is integrated with the IC. The optoelectronic (OE) devices, comprise, and in some embodiments consist of, a combination of microLEDs and photodetectors.

(30) As discussed above, the OE devices can be monolithically-integrated or hybrid-integrated with the IC. Generally, the viability of monolithic integration depends on the IC material and link wavelength. In the case of heterogeneous integration, die with large arrays of LEDs or photodetectors may be attached to the IC in a single attachment process.

(31) Note that the OE devices may, in general, be located anywhere on the IC surface. This ability to place optical 10 anywhere on the IC surface may provide a number of benefits, including: interconnect density that scales with IC area rather than edge length, enabling increased chip-to-chip interconnect density; and ability to place off-chip interconnects very close to associated processing logic, allowing for more flexible optimized IC layout and reducing on-chip interconnect resources.

(32) It is frequently desired that the links be bidirectional. In the case of highly parallel bussed optical connections, it may be desirable to have both directions of the link in close physical proximity to each other. This can be accomplished by various optoelectronic device configurations as shown in FIGS. 6a-e. In FIG. 6a, microLEDs 611 and photodetectors 613 are alternated with each other on a rectangular grid. In FIG. 6b the microLEDs and photodetectors are alternated on a hexagonal grid. Both of these configurations have each photodiode close to multiple microLEDs,

which can create electrical and optical crosstalk problems. These configurations may also be unattractive from a manufacturing/assembly standpoint because it may be easier to fabricate and assemble monolithic arrays of OE devices.

(33) The problems associated with these alternating configurations can be overcome or reduced by “tiling” alternating arrays of microLEDs and photodetectors. FIG. 6c shows hexagonal tiles of microLEDs and photodetectors, with individual devices on a hexagonal grid. FIG. 6d shows rectangular tiles of microLEDs and photodetectors, with individual devices on a rectangular grid. FIG. 6e shows approximately rectangular tiles of microLEDs and photodetectors, with individual devices on a hexagonal grid.

(34) The two-dimensional OE device array may be butt-coupled into an array of multicore waveguides. Various types of multicore waveguides may be used. FIG. 7a shows a cross-sectional view of a multicore fiber in which each core may be coupled to one microLED on one end and one photodetector on the other end. The multicore fiber of FIG. 7a includes a plurality of waveguide cores 711, with each core surrounded by cladding 713.

(35) FIG. 7b shows a cross-sectional view of coherent imaging fiber, with an exploded view of a portion of the fiber. The fiber is comprised of a large number of very small diameter “micro-cores” 721 with the cores surrounded by cladding 723. The term “coherent imaging fiber” refers to the fact that the optical intensity distribution at an input face of the fiber is approximately reproduced at the output face of the fiber. More accurately, the output optical distribution is a spatially sampled version of the input optical distribution, where the spatial sampling frequency is determined by the center-to-center spacing of the micro-cores. In some embodiments the cores are sufficiently small and closely spaced that the light from each microLED forms a spot spanning multiple cores, and multiple cores thus transport the light from each input microLED to each photodetector. Such an arrangement flexibly accommodates various optical configurations (e.g., different numbers of OE devices, different spot sizes from the microLEDs). Differential phase shifts across cores could cause output speckle problems with a spatially coherent input, but the low spatial and temporal coherence associated with a microLED source generally reduces or eliminates speckle problems.

(36) FIG. 7c shows a multi-layer planar waveguide stack. The multi-layer planar waveguide stack includes a plurality of planar layers, with each planar layer including a plurality of waveguide cores 731, surrounded by waveguide cladding 733. Planar waveguides may be commonly used in a single-layer configuration. Multiple layers can be stacked to implement a 2D array of waveguides. The waveguide array may be fabricated on a rigid or flexible planar substrate, but there are significant advantages to the use of flexible substrate, including: for highly interconnected architectures with ICs lying in a plane, many connections may cross over each other; and if we have the freedom to distribute ICs across multiple substrates which may or may not be lying in a plane, the use of flexible waveguides may traverse the third dimension.

(37) Even with high-performance optical links, ICs still generally use many electrical connections for power, ground, and control lines. Therefore, optical links should coexist with electrical packaging. High-performance packaging typically uses solder bumps or direct bonding to create dense connections from an active circuit side of an IC to a substrate with good electrical and thermal characteristics.

(38) It is advantageous to make optical connections from this same active circuit side of the IC. However, this potentially creates problems because the substrate is very close to the IC when using bumps or direct bonding. To allow adequate space for the optical connections, it may be advantageous for the optical connections to traverse the substrate. FIG. 8a shows a hole in a substrate that allows an optical connection to traverse to the other side of the substrate. An optical coupling assembly and a multicore waveguide assembly both fit within the hole. As shown in FIG. 8a, an IC 811 is mounted to a substrate 813. The substrate includes a hole 815, with the hole over a portion of the IC (or under a portion of the IC, depending on orientation). An OE device array 816 is mounted on the IC, within a volume of the hole. An optical coupling assembly 817 is on the OE

device array, with a multicore waveguide coupling assembly **819** coupled to the optical coupling assembly. Both the optical coupling assembly and the multicore waveguide coupling assembly are within the hole in the substrate, in the embodiment illustrated in FIG. **8a**. A multicore waveguide **821** extends from the multicore waveguide coupling assembly, out through a side of the substrate opposite that of the IC.

(39) The use of a substrate that is transparent at the link's wavelength enables an alternative approach. FIG. **8b** shows an example of use of a transparent substrate. In FIG. **8b**, the IC **811** is mounted to a transparent substrate **851**. The optoelectronic (OE) device array **816** is on the IC and coupled to the multicore waveguide assembly through the substrate by optical coupling assemblies placed on both sides of the substrate, with FIG. **8b** showing an optical coupling assembly **853** on the OE device array and a multicore waveguide coupling assembly **855** on an opposing side (from the IC) of the transparent substrate. The multicore waveguide **821** extends from the multicore waveguide coupling assembly and away from the substrate. Some embodiments may include a cavity on the OE side of the substrate to accommodate the optical coupling assembly, for example as shown in FIG. **8b**.

(40) An exemplary optical coupling assembly implementation comprises, and in some embodiments consists of, an optoelectronic (OE) subassembly and a multi-waveguide (MW) subassembly. FIG. **9a** show an OE subassembly. In the OE subassembly, a lens **911** may be placed approximately one focal length from an OE device array **913**. In the example of FIG. **9a**, the OE device array is shown mounted to an IC **915** by solder bumps **917**. FIG. **9b** shows an MW subassembly. In the MW subassembly, a lens **921** may be placed approximately one focal length from a multicore waveguide (MW) array **923**. The space between the two lenses can span a relatively large range, allowing its use both of the aforementioned substrate traversal arrangements with a wide variety of different substrate thicknesses. The large tolerance of the space between lenses simplifies assembly and may allow for increases manufacturing yields.

(41) The ability to accommodate a large space between the lenses also allows the insertion of additional optical elements such as turning mirrors. In FIG. **9c**, an OE device array **951** is on an IC **953**. Light to or from the OE device array passes through a first lens **955**. The first lens, and in some embodiments also the OE device array, may be considered an OE coupling assembly **957**. A turning mirror **959** reflects, or turns, the light by 90 degrees, to or from a second lens **961**. The light passing through the second lens arrives at or comes from a multicore waveguide **963**. The second lens, and in some embodiments an end face of the multicore waveguide, may be considered a MW coupling subassembly **965**. FIG. **9c** shows the use of the turning mirror to turn the beam by 90°. This is a powerful technique for decreasing the size of systems using vertically launched parallel optical links (VLPOLs). As shown in FIG. **9d**, two turning mirrors **959a,b** can be used inserted between the first and second lenses **955**, **961** to turn light 180°, which can be useful in various circumstances, for example if a direction of emission orientation of a microLED is opposite that of a desired signal path or a variety of other circumstances.

(42) Although the invention has been discussed with respect to various embodiments, it should be recognized that the invention comprises the novel and non-obvious claims supported by this disclosure.

Claims

1. Optically interconnected integrated circuits, comprising: a substrate having a first hole and a second hole, the first hole and the second hole each extending through the substrate; a first integrated circuit (IC) chip, including logic circuitry, mounted to the substrate; a first transceiver IC chip electrically connected to the first IC chip and mounted to the substrate and having a first active side facing the substrate with a portion of the first active side having a first plurality optoelectronic devices hanging over the first hole of the substrate; the first plurality of optoelectronic devices

having a first array of microLEDs and a first array of photodetectors; the first plurality of optoelectronic devices coupled to the first transceiver IC chip by way of direct bonds; a second IC chip, including logic circuitry, mounted to the substrate; a second transceiver IC chip electrically connected to the second IC chip and mounted to the substrate, the second transceiver IC chip having a second active side facing the substrate with a portion of the second active side having a second plurality optoelectronic devices hanging over the second hole of the substrate; the second plurality of optoelectronic devices having a second array of microLEDs and a second array of photodetectors; the second plurality of optoelectronic devices coupled to the second transceiver IC chip by way of direct bonds; a first optical coupling assembly on the first plurality of optoelectronic devices and a second optical coupling assembly on the second plurality of optoelectronic devices, the first optical coupling assembly at least in part in the first hole in the substrate and the second optical coupling assembly at least in part in the second hole in the substrate; a waveguide having a plurality of waveguide cores inside the first hole and the second hole of the substrate and optically coupling the first and second plurality of optoelectronic devices.

2. The optically interconnected integrated circuits of claim 1, wherein the substrate is made from a rigid material.

3. The optically interconnected integrated circuits of claim 1, wherein the substrate is made from a flexible material.

4. The optically interconnected integrated circuits of claim 1, wherein a first lens is placed between the first plurality of optoelectronic devices and the waveguide, and a second lens is placed between the second plurality of optoelectronic devices and the waveguide.

5. The optically interconnected integrated circuits of claim 4, wherein the first lens is spaced apart from the first plurality of optoelectronic devices by one focal length and the second lens is spaced apart from the second plurality of optoelectronic devices by one focal length.

6. The optically interconnected integrated circuits of claim 1, further comprising a first turning mirror between the first plurality of optoelectronic devices and the waveguide and a second turning mirror between the second plurality of optoelectronic devices and the waveguide.

7. The optically interconnected integrated circuits of claim 1, wherein the substrate includes metal signal layers connecting the first IC chip and the second IC chip.

8. The optically interconnected integrated circuits of claim 1, wherein the first array of microLEDs and the first array of photodetectors are arranged in a first set of tiles and the second array of microLEDs and the second array of photodetectors are arranged in a second set of tiles.
