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(54) IMAGE SENSORS FOR ADVANCED DRIVER ASSISTANCE SYSTEMS UTILIZING REGULATOR VOLTAGE VERIFICATION CIRCUITRY TO DETECT MALFUNCTIONS

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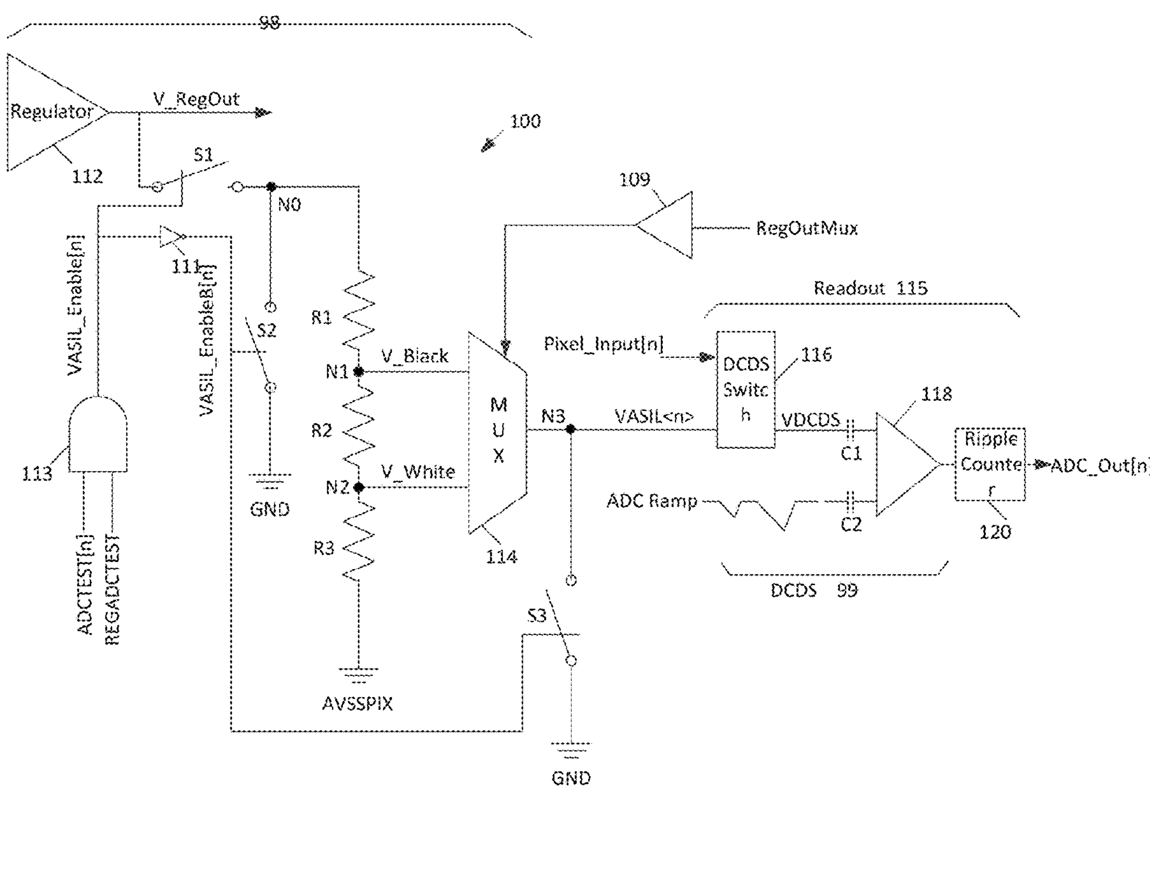
(57) **ABSTRACT**

A regulator voltage verification circuit for an Advanced Driver Assistance System (ADAS) enables testing of voltage regulators in a pixel array. The circuit generates test voltages representing expected black and white pixel values as a function of the regulator's output voltage. The test voltages are selectively passed to an analog-to-digital conversion circuit in a test mode, while pixel outputs are processed in normal mode. A voltage divider connected to the regulator output creates upper and lower test voltages, which are selected by a multiplexer. The test voltages are routed through a digital correlated double sampling switch to a comparator and ripple counter, converting the analog test values to digital data. By comparing the digital output to expected values, the system can detect regulator malfunctions and issue appropriate warnings. The circuit can be implemented across multiple rows of a pixel array, with test results optionally averaged for accuracy.



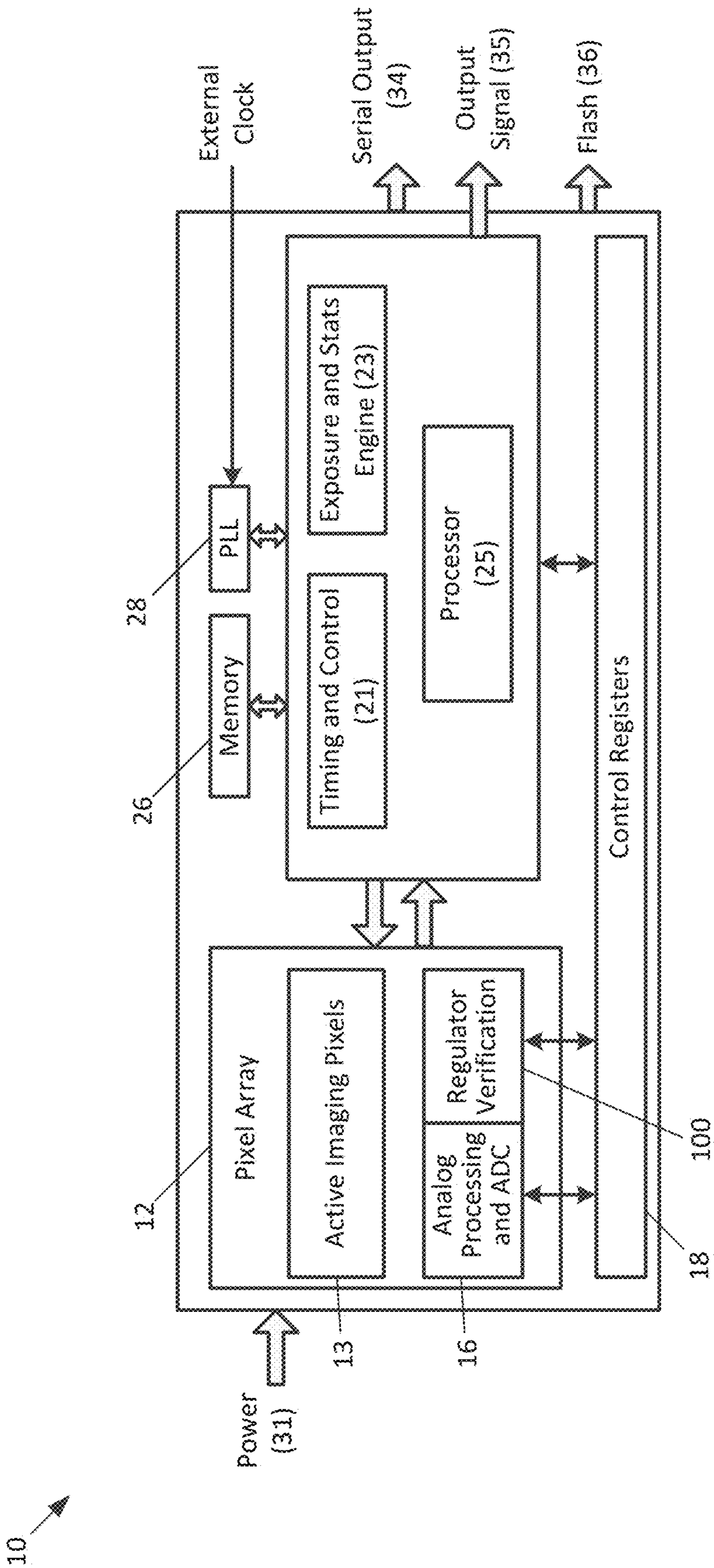
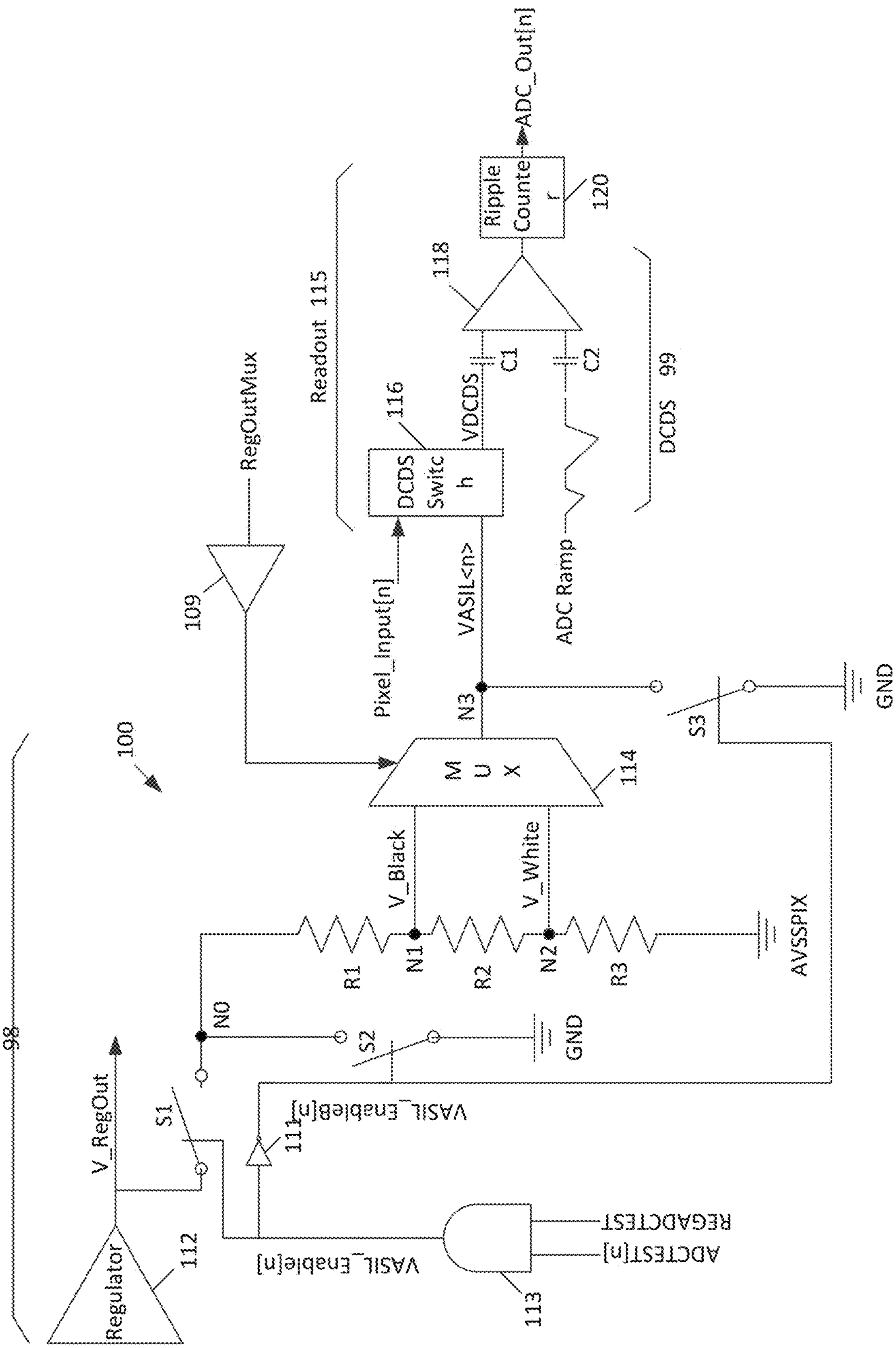

External Clock
Serial Output (34)
Output Signal (35)
Flash (36)
28
PLL
26
Memory
Exposure and Stats Engine (23)
Timing and Control (21)
Processor (25)
Control Registers
12
Pixel Array
Active Imaging Pixels
Regulator Verification
Analog Processing and ADC
100
18
13
16
Power (31)
10

FIG. 1



Regulator
112
V_RegOut
98
100
S1
N0
S2
GND
R1
N1
R2
N2
R3
AVSSPIX
V_Black
V_White
MUX
114
109
RegOutMux
N3
S3
GND
VASIL_Enable[n]
VASIL_EnableB[n]
111
113
REGADCTEST
ADCTEST[n]
Pixel_Input[n]
VASIL<n>
ADC Ramp
DCDS Switch
116
VDCDS
C1
C2
118
Ripple Counter
120
ADC_Out[n]
Readout 115
DCDS 99

FIG. 2

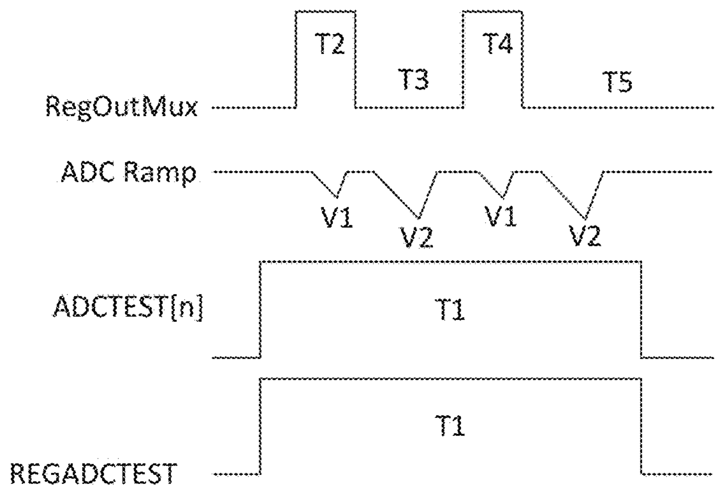

T2
T3
T4
T5
RegOutMux
ADC Ramp
V1
V2
V1
V2
ADCTEST[n]
T1
T1
REGADCTEST

FIG. 3

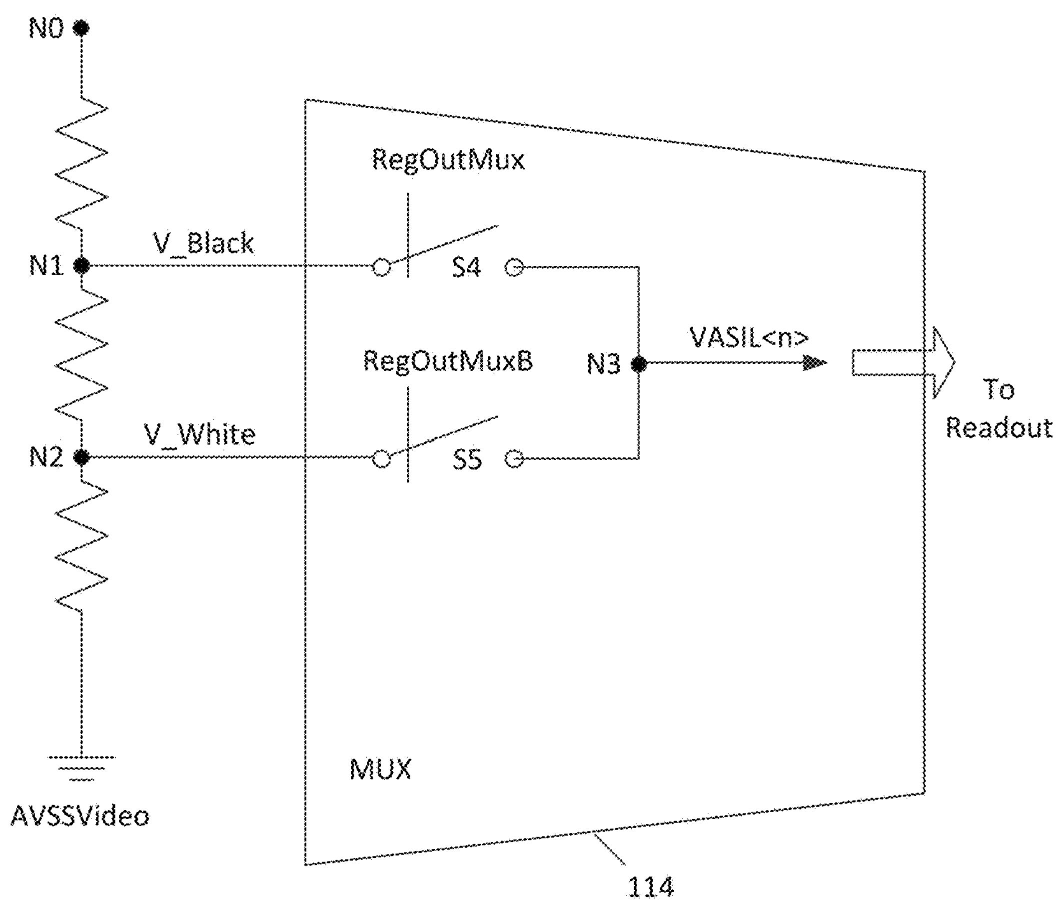

N0
RegOutMux
V_Black
N1
S4
VASIL<n>
RegOutMuxB
N3
To
Readout
N2
V_White
S5
MUX
AVSSVideo
114

FIG. 4

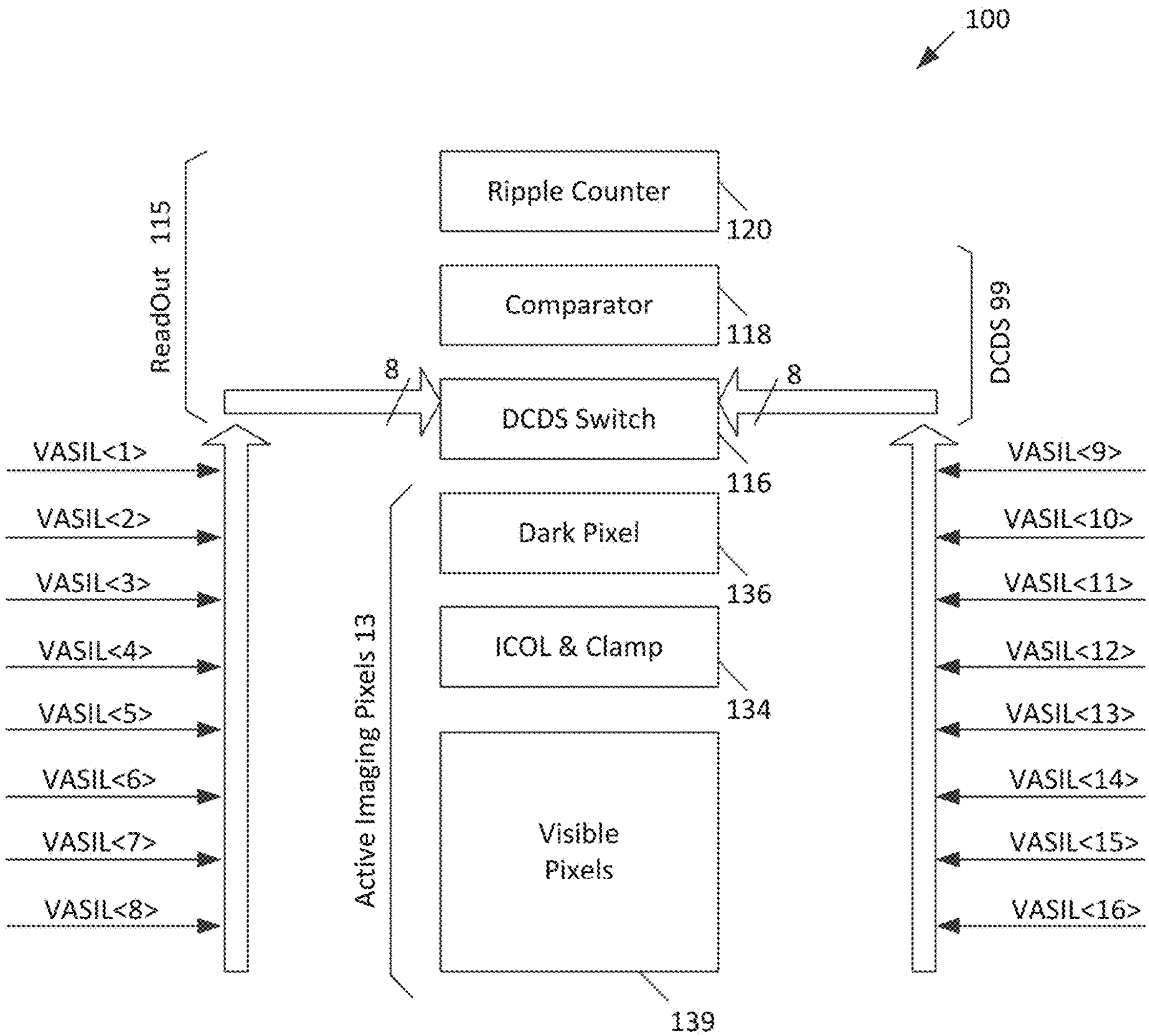

100
ReadOut 115
Ripple Counter
120
Comparator
118
DCDS 99
8
DCDS Switch
8
116
VASIL<1>
VASIL<2>
VASIL<3>
VASIL<4>
VASIL<5>
VASIL<6>
VASIL<7>
VASIL<8>
VASIL<9>
VASIL<10>
VASIL<11>
VASIL<12>
VASIL<13>
VASIL<14>
VASIL<15>
VASIL<16>
Dark Pixel
136
ICOL & Clamp
134
Active Imaging Pixels 13
Visible Pixels
139

FIG. 5

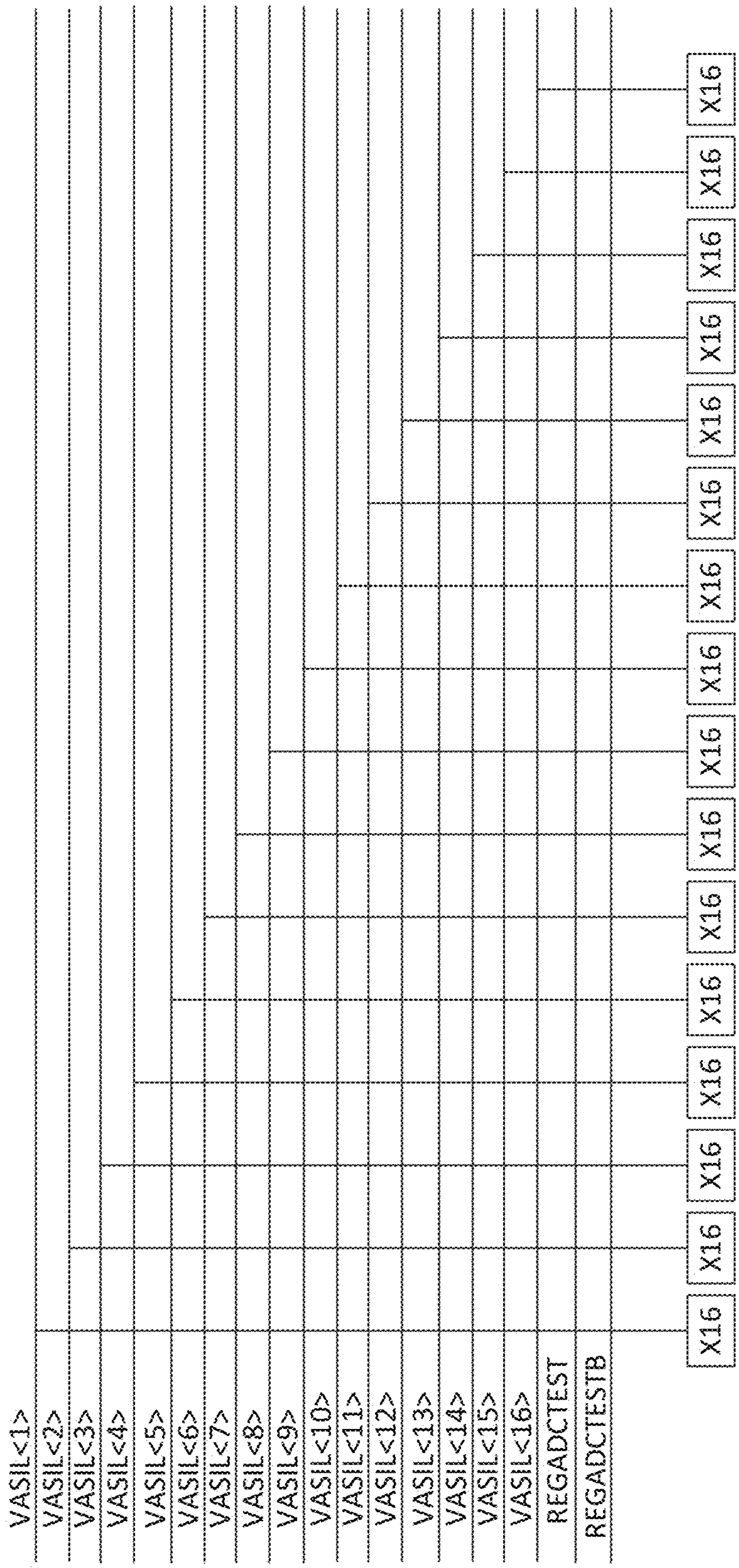

VASIL<1>
VASIL<2>
VASIL<3>
VASIL<4>
VASIL<5>
VASIL<6>
VASIL<7>
VASIL<8>
VASIL<9>
VASIL<10>
VASIL<11>
VASIL<12>
VASIL<13>
VASIL<14>
VASIL<15>
VASIL<16>
REGADCTEST
REGADCTESTB
X16
X16
X16
X16
X16
X16
X16
X16
X16
X16
X16
X16
X16
X16
X16
X16

FIG. 6

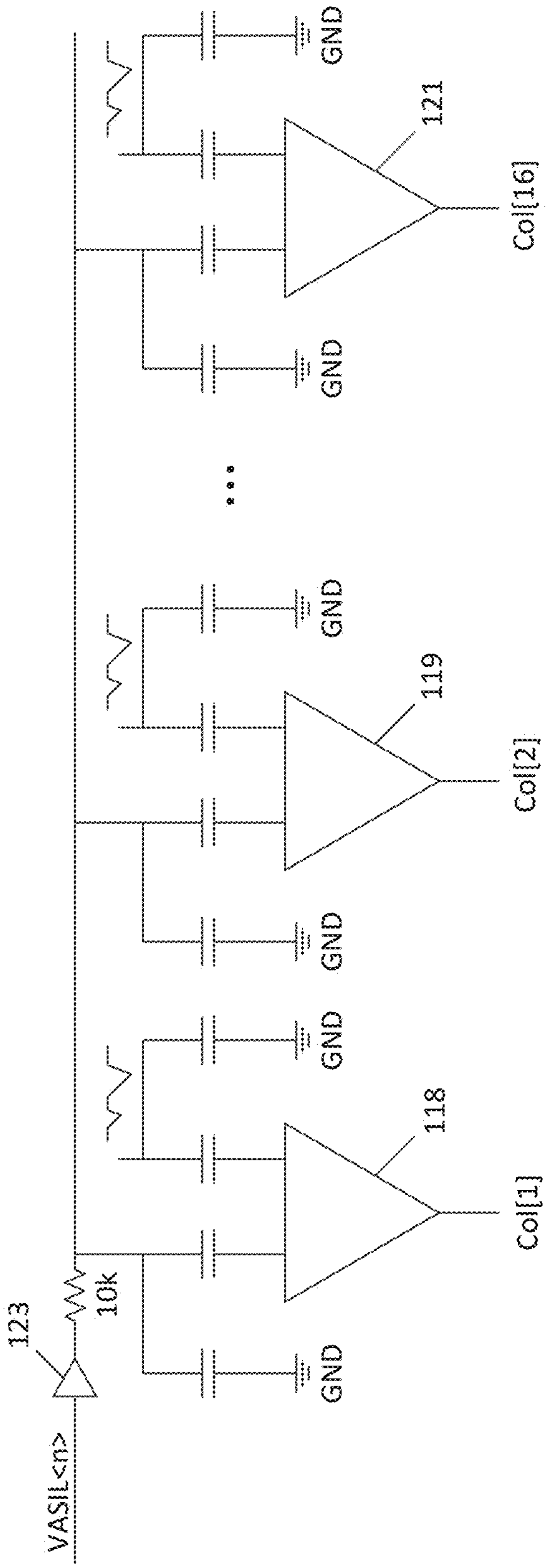


FIG. 7

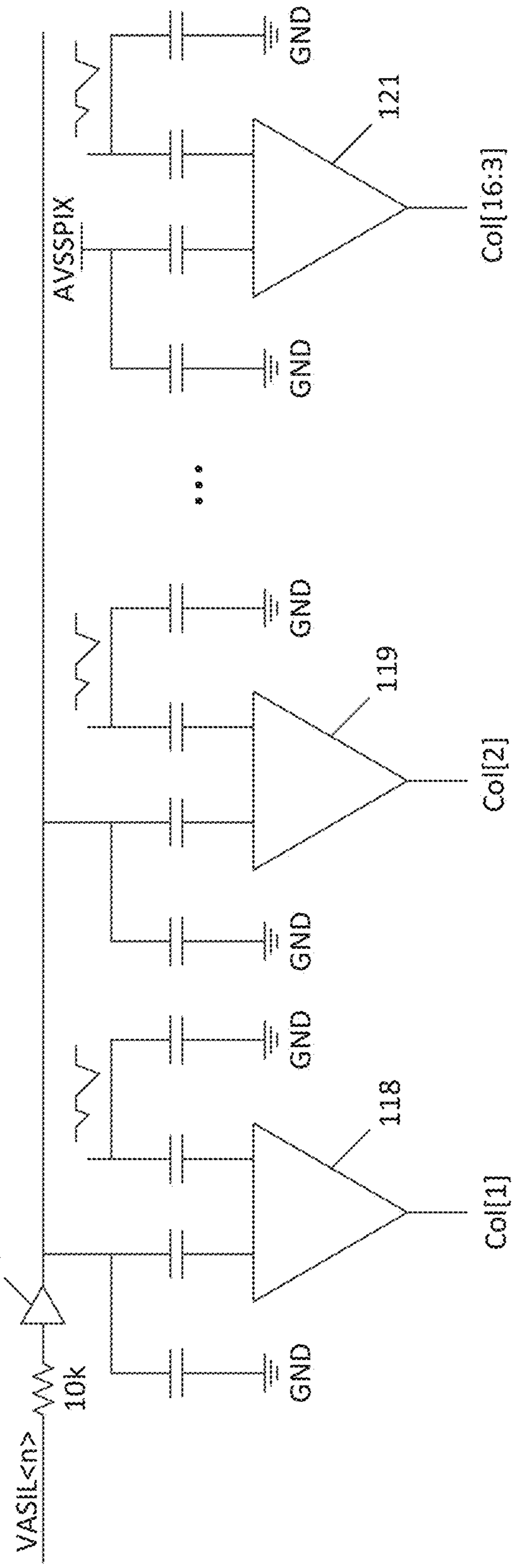
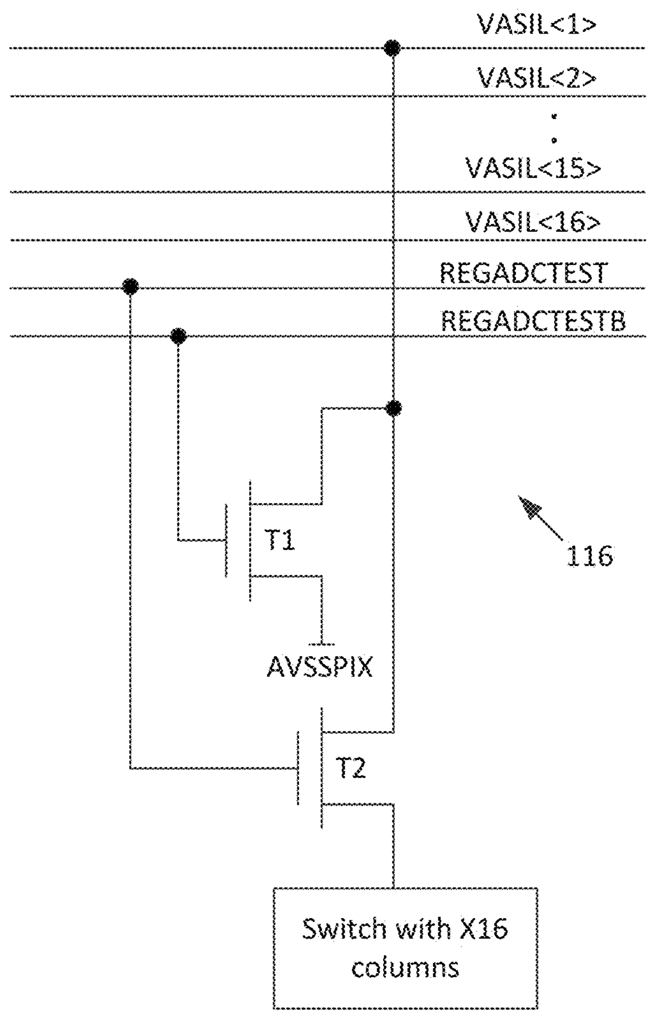

GND
121
Col[16:3]
AVSSPIX
GND
GND
119
Col[2]
GND
GND
118
Col[1]
123
GND
10k
VASIL<n>

FIG. 8



VASIL<1>
VASIL<2>
VASIL<15>
VASIL<16>
REGADCTEST
REGADCTESTB
T1
116
AVSSPIX
T2
Switch with X16 columns

FIG. 9

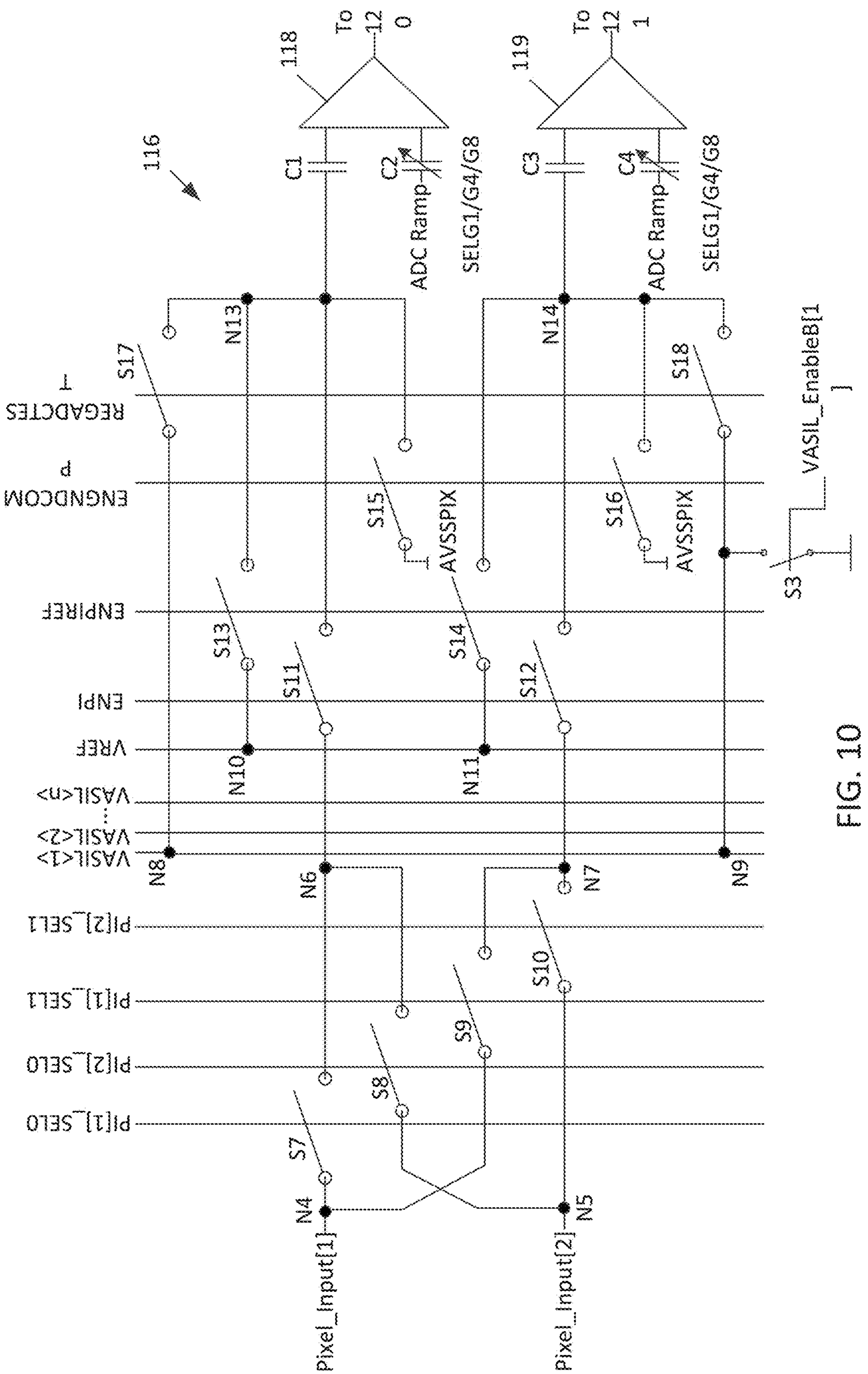

116
118
119
To 120
To 121
C1
C2
C3
C4
ADC Ramp
SELG1/G4/G8
N4
N5
N6
N7
N8
N9
N10
N11
N13
N14
S3
S7
S8
S9
S10
S11
S12
S13
S14
S15
S16
S17
S18
AVSSPIX
VASIL_EnableB[1]
Pixel_Input[1]
Pixel_Input[2]
PI[1]_SEL0
PI[2]_SEL0
PI[1]_SEL1
PI[2]_SEL1
VASIL<1>
VASIL<2>
VASIL<n>
VREF
ENPI
ENPIREF
ENGNDCOMp
REGADCTEST

FIG. 10

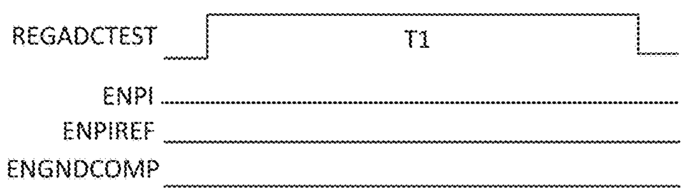

REGADCTEST
T1
ENPI
ENPIREF
ENGNDCOMP

FIG. 11

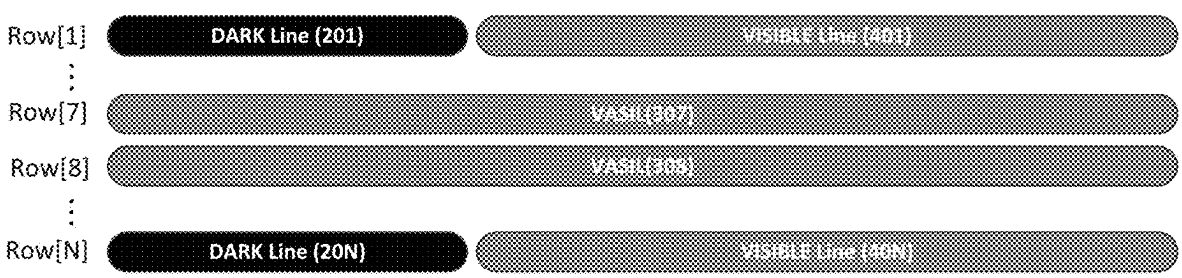

Row[1]
DARK Line (201)
VISIBLE Line (401)
Row[7]
VASIL(307)
Row[8]
VASIL(308)
Row[N]
DARK Line (20N)
VISIBLE Line (40N)

FIG. 12

IMAGE SENSORS FOR ADVANCED DRIVER ASSISTANCE SYSTEMS UTILIZING REGULATOR VOLTAGE VERIFICATION CIRCUITRY TO DETECT MALFUNCTIONS

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a division of U.S. application for patent Ser. No. 17/736,504, filed May 4, 2022, itself a division of U.S. application for patent Ser. No. 16/514,695, filed Jul. 17, 2019, (now U.S. Pat. No. 11,356,654), which claims priority to U.S. Provisional Application for Patent No. 62/713,175, filed on Aug. 1, 2018, the contents of all of which are incorporated by reference to the maximum extent allowable under the law.

TECHNICAL FIELD

[0002] This disclosure is related to the field of image sensors for advanced driver assistance systems and, more particularly, to circuits and techniques for the verification of the production of proper voltages by voltage regulators used with such image sensors to detect improper function of those regulators.

BACKGROUND

[0003] Modern vehicles are increasingly equipped with advanced driver assistance systems (ADAS).

[0004] ADAS enable vehicle features such as automated lighting, adaptive cruise control, automatic braking, collision warnings, proximity warnings, traffic and road condition warnings, connectivity with smartphones, lane keep assist, blind spot monitoring, and automated driving modes. In addition to being used for driver comfort and assistance, these systems may be used for collision avoidance to increase safety. For example, if a driver fails to respond to a proximity warning, automatic braking may allow the vehicle to stop on its own, avoiding a potential collision. Automated driving may function so as to steer the vehicle around dangers, or to steer the vehicle back into its lane if the driver begins to drift out of the lane.

[0005] ADAS rely on inputs from multiple data sources, including digital imaging, light detection and ranging, radar, image processing, computer vision, and in-car networking. Additional inputs are possible from other sources separate from the primary vehicle platform, such as other vehicles (referred to as vehicle-to-vehicle systems) or from infrastructure such as cellular data or wireless internet systems (referred to as vehicle-to-infrastructure systems).

[0006] A primary sensor for many ADAS systems is an image sensor. As ADAS systems have progressed from driver assistance to include the automation and safety functions discussed above, the safe operation of a vehicle employing an ADAS system will depend more and more on the reliability of the image sensor and imaging system. Therefore, the reliable operation of the image sensor has become a critical safety component in many modern vehicles.

[0007] As a consequence, the ISO 26262 standard was developed to include the Automotive Safety Integrity Level (ASIL) risk classification scheme. The ASIL levels range from the lowest, ASIL-A (lowest), to ASIL-D (highest). An ASIL level is determined by three factors, namely the severity of a failure, the probability of a failure occurring, and the ability for the effect of the failure to be controlled.

[0008] Faults in the image sensors or image sensing or image sensing subsystems of ADAS systems may arise from a number of causes, including improperly operating voltage regulators. Due to the importance of the operation of an image sensor in an ADAS system, it is therefore desired to detect faults in the operation of an image sensor in an ADAS system or in an image sensing subsystem as quickly as possible.

SUMMARY

[0009] In one embodiment, the disclosure provides a circuit comprising a supply voltage node, at least one pixel that includes an imaging element and an analog-to-digital conversion circuit, and a test voltage generation circuit configured to generate a test voltage as a function of the supply voltage. In this embodiment, the analog-to-digital conversion circuit operates in a standard operational mode by sampling the output of the imaging pixel to produce digital data and, in a test mode, by sampling the test voltage to produce digital data. In some cases, a processor is further included to receive the digital data in the test mode, compare the received data to an expected value, and take corrective action if the digital data does not substantially match the expected value.

[0010] In additional embodiments, the test voltage generation circuit is designed to generate both an upper test voltage and a lower test voltage representing, respectively, upper and lower expected voltages of the imaging pixel's output. The circuit may include a voltage divider coupled between the supply voltage node and a reference node to derive these voltages, along with a multiplexer that selects the appropriate test voltage based on a select signal. A logic circuit may combine a primary test mode enable signal with an individual pixel test mode enable signal to provide a test mode enable signal, and a series of switches selectively couple the supply voltage or shunt circuit elements to ground based on this enable signal. Moreover, the analog-to-digital conversion circuit can incorporate a switching circuit, a comparison circuit, and a counter that begins counting at the start of each test cycle and stops when the comparison circuit, which may use capacitive coupling and a voltage ramping signal, detects a coincidence in voltage. In various embodiments, the circuit is also configured to couple the test voltage to multiple columns—or a subset of columns for improved settling time and reduced capacitive loading—in a pixel array, with the test voltage generation circuitry sometimes integrated into consecutive rows to allow averaged test results.

[0011] In another embodiment, the disclosure provides a method for verifying a voltage regulator in an advanced driver assistance system. The method comprises providing power from the voltage regulator to at least one pixel that includes an imaging pixel and an analog-to-digital conversion circuit, and generating a test voltage as a function of the regulator's output voltage. In a test mode, the analog-to-digital conversion circuit samples the test voltage to produce digital data, while in an operational mode the analog-to-digital conversion circuit samples the output from the imaging pixel. The method further includes comparing the obtained digital data to an expected value and, if the values are not substantially equal, taking corrective action. Additional steps of the method involve generating upper and

lower test voltages using a voltage divider, selecting between these voltages via a multiplexer responsive to a select signal, and routing power through switches controlled by a test mode enable signal derived from primary and individual enable signals. The method further comprises sampling the test voltage through a switching circuit and a comparator arrangement that uses a periodically ramping analog-to-digital conversion signal, coupling the test voltage across multiple columns and rows of a pixel array to generate averaged test results, and, upon detecting a deviation from the expected digital data, outputting commands that alert a vehicle to a malfunction in the advanced driver assistance system.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] FIG. **1** is a block diagram of an advanced driver assistance system (ADAS) in accordance with this disclosure.

[0013] FIG. **2** is a block diagram for a regulator voltage verification circuit such as may be used in the ADAS of FIG. **1**.

[0014] FIG. **3** is a timing diagram of the regulator voltage verification circuit of FIG. **2** in operation.

[0015] FIG. **4** is a more detailed block diagram of the multiplexer of the regulator voltage verification circuit of FIG. **2**.

[0016] FIG. **5** is a block diagram of the regulator voltage verification circuit of FIG. **2** as implemented in a pixel array along with the analog processing and A/D conversion block of FIG. **1**.

[0017] FIG. **6** is a wiring diagram illustrating how the DCDS switch of FIGS. **2** and **5** couple different voltages VASIL to different groups of the columns of the pixel array.

[0018] FIG. **7** is a block diagram of one of the ways in which the DCDS switch of FIGS. **2**, **5**, and **6** can couple the different voltages VASIL to different groups of the columns of the pixel array.

[0019] FIG. **8** is a block diagram of a different one of the ways in which the DCDS switch of FIGS. **2**, **5**, and **6** can couple the different voltages VASIL to different groups of the columns of the pixel array.

[0020] FIG. **9** is a schematic diagram showing the circuitry used to make the connections shown in FIGS. **6-8** between voltages VASIL and columns of the pixel array.

[0021] FIG. **10** is a detailed schematic diagram of the DCDS switch of FIGS. **2**, **5**, and **6**.

[0022] FIG. **11** is a timing diagram of the operation of the DCDS switch circuitry shown in FIG. **10**.

[0023] FIG. **12** is a diagram showing the order for the data read from each row of the pixel array of FIG. **2**.

DETAILED DESCRIPTION

[0024] The following disclosure enables a person skilled in the art to make and use the subject matter disclosed herein. The general principles described herein may be applied to embodiments and applications other than those detailed above without departing from the spirit and scope of this disclosure. This disclosure is not intended to be limited to the embodiments shown, but is to be accorded the widest scope consistent with the principles and features disclosed or suggested herein.

[0025] An advanced driver assistance system **10** is now described with reference to FIG. **1**. The advanced driver assistance system **10** can be incorporated into an automobile, such as a car or light duty truck, or can be incorporated into commercial vehicles, such as class **8** vehicles (sometimes referred to as a “semi” or an “**18** wheeler”). The advanced driver assistance system **10** includes a pixel array **12** with active imaging pixels **13**, an analog to digital conversion (ADC) block **16**, and a regulator voltage verification circuit **100**. The active imaging pixels **13** capture image data in an analog format and provides the image data, in an analog fashion, to the analog processing and analog to digital conversion (ADC) block **16**, which filters the image data in the analog domain and converts the image data to the digital domain to produce digital image data. The analog processing and analog to digital conversion block **16** passes the digital image data to the processor **25**, which, pursuant to settings received from the control registers **18**, performs desired digital processing functions, such as determining that the vehicle into which the advanced driver assistance system **10** is incorporated is headed toward an imminent collision, or whether the pixel array **12** is operating properly. A regulator voltage verification circuit **100** checks the voltages of voltage regulators used by the analog processing and analog to digital conversion block **16** as well as the active imaging pixels **13**. The processor **25** provides its output signal **35** via a suitable data interface, such as a parallel data interface or a serial data interface, either directly to other components of the vehicle into which the advanced driver assistance system **10** is associated, or to such components via a data bus.

[0026] A phase locked loop (PLL) **28** provides a clock signal for use by the processor **25**, and a memory **26** provides non-volatile or volatile data storage for use by the processor **25**.

[0027] Further details of the pixel array **12** are now given with additional reference to FIG. **2**. The regulator voltage verification circuit **100** shown in FIG. **2** and described below will be replicated multiple times. Therefore, the usage of [n] in the descriptions below is generic and used to indicate that a signal so labeled is specific to each instance of the regulator voltage verification circuit **100** and not global to all. It should be noted that signals not labeled with [n] may also in some instances be specific to each instance of the regulator voltage verification circuit **100**. So, [n] is used herein is not limiting and is just an aid to ease reading.

[0028] The regulator voltage verification circuit **100** receives a regulator voltage V_RegOut from a voltage regulator **112** (which is common to the row of the pixel array **12** in which the regulator voltage verification circuit **100** resides).

[0029] AND gate **113** performs a logical AND operation on the ADCTEST[n] signal and the REGADCTEST signal to produce the VASIL_Enable[n] signal. REGADCTEST is fed to each AND gate **113** of each occurrence of the regulator voltage verification circuit **100**, and serves as a master enable signal of the test operation, while a different ADCTEST[n] signal is fed to each AND gate **113** of each occurrence of the regulator voltage verification circuit **100**, and serves as an enable signal for that particular regulator voltage verification circuit **100**.

[0030] Switch S**1** selectively couples V_RegOut to node N**0** in response to assertion of the VASIL_Enable[n] signal. Switch S**2** selectively shunts node N**0** to ground in response to an inverse of the VASIL_Enable signal (inverted by inverter **111**), labeled here as VASIL_EnableB[n] signal.

[0031] When testing of the voltage regulator 112 is desired, the VASIL_Enable[n] signal is asserted, closing switch S1 and opening switch S2. It follows that when testing of the voltage regulator 112 is not desired, the VASIL_Enable signal is deasserted, opening switch S1 and closing switch S2, shunting node N0 to ground.

[0032] Resistors R1, R2, and R3 are coupled in series between node N0 and reference voltage AVSSPIX to form a resistive divider circuit. A test voltage V_Black is produced at the tap N1 between resistors R1 and R2, and a test voltage V_White is produced at the tap N2 between resistors R2 and R3. V_Black is similar to the voltage that would be produced by a properly operating voltage regulator 112 at node N1 to simulate a pixel of the active imaging pixels 13 not detecting light, while V_White is similar to the voltage that would be produced by a properly operating voltage regulator 112 at node N2 to simulate a pixel of the active imaging pixels 13 being saturated with light.

[0033] Multiplexer 114 receives V_Black and V_white as inputs, and selectively outputs those voltages as VASIL<n> to the digital correlated double sampling (DCDS) switch unit 116 at node N3, in response to the RegOutM ux signal as amplified by buffer 109. The switch S3 selectively shunts node N3 to ground in response to assertion of the VASIL_EnableB signal.

[0034] The voltage regulator 112, AND gate 113, inverter 111, switches S1-S3, resistors R1-R3, and multiplexer 114 can collectively be referred to as the VASIL voltage generation circuitry 98.

[0035] The DCDS switch unit 116 receives VASIL<n> and an output Pixel_Input[n] from a pixel of the array of pixels 12, and selectively outputs one of those voltages as VDCDS through capacitor C1 to comparator 118.

[0036] The comparator 118 receives the output of the DCDS switch 116 through capacitor C1 as voltage VDCDS and a ramp signal through capacitor C2, and provides output to the ripple counter 120. Note that the DCDS switch 116 and comparator 118 can collectively be referred to as simply the DCDS 99, which is part of the analog processing and analog to digital conversion block 16.

[0037] At the beginning of a cycle of the ramp signal, the ripple counter 120 is reset, and begins to count. The comparator 118 asserts its output when VDCDS is equal to the ramp signal, stopping the ripple counter 120. At this point, the output ADC_Out[n] of the ripple counter 120 is proportional to VDCDS, effectuating the conversion of VASIL<n> (or Pixel_Input[n]) from an analog voltage to a digital value. Thus, the comparator 118 is functioning as the digital to analog converter of the analog processing and analog to digital conversion block 16 of FIG. 1.

[0038] The processor 25, by comparing ADC_Out to an expected value, can determine whether V_RegOut is an expected value, and if it is not, can infer that the voltage regulator 112 is not operating properly, and the advanced driver assistance system 10 can output commands causing the vehicle into which the advanced driver assistance system 10 is incorporated to take an appropriate action, such as provide warning to a driver that the advanced driver assistance system 10 is malfunctioning.

[0039] Note that the DSCS switch 116, comparator 118, and ripple counter 120 can collectively be referred to as the readout path 115.

[0040] An example of operation of the regulator voltage verification circuit 100 is now described with additional reference to the timing diagram of FIG. 3. During time period T1, the REGADCTEST and ADCTEST[n] signals are asserted, so the output of the AND gate 113 goes high, asserting the VASIL_Enable[n] signal, which when inverted by inverter 111 would mean that the VASIL_EnableB[n] signal is deasaserted. This in turn closes switch S1 and opens switches S2 and S3, allowing test operation to begin. The REGADCTEST and ADCTEST[n] signals remain asserted during the test operation.

[0041] During time period T2, beginning after the start of time period T1, RegOutM ux is asserted, resulting in the multiplexer 114 selecting the test black signal V_Black to output as VASIL<n>. In addition, at the start of the time period T2, the ripple counter 120 is reset and begins to run. The ADC ramp signal falls from high to a first voltage V1 during time period T2.

[0042] As the ADC ramp signal falls to V1, at some point, the voltage VASIL<n> will be equal to the ADC ramp signal, resulting in the comparator 118 asserting its output, stopping the ripple counter 120. The output of the ripple counter 120, as ADC_Out[n], during time period T 2 thus represents the value of VASIL<n> when V_Black is selected by the multiplexer 114. If this value is not as expected, it can be inferred that the voltage regulator 112 is malfunctioning.

[0043] During time period T3, beginning after the end of time period T2, RegOutM ux is deasserted, causing selection of the test white voltage V_White by the multiplexer 114 and its corresponding output as VASIL<n>. In addition, the ripple counter 120 is reset and begins counting again at the start of time period T3. The ADC ramp signal (having charged back to high by the end of time period T2) now falls from high to a second voltage V2 that is lower than the first voltage V1, representing a longer integration time.

[0044] As the ADC ramp signal falls to V2, at some point, the voltage of VASIL<n> will be equal to the A DC ramp signal, resulting in the comparator 118 asserting its output, stopping the ripple counter 120. The output of the ripple counter 120, as ADC_Out[n], during time period T3 thus represents the value of VASIL<n> when V_White is selected by the multiplexer 114. If this value is not as expected, it can be inferred that the voltage regulator 112 is malfunctioning.

[0045] The operations described above with reference to time periods T2 and T3 are performed for row 7 of the pixel array 12. The operations described below with reference to time periods T4 and T5 will be performed for row 8 of the pixel array 12.

[0046] During time period T4, beginning after the end of time period T3, RegOutM ux is asserted, resulting in the multiplexer 114 selecting the test black signal V_Black to output as VASIL<n>. In addition, at the start of the time period T4, the ripple counter 120 is reset and begins to run again. The ADC ramp signal (having charged back high by the end of time period T3) falls from high to a first voltage V1 during time period T4.

[0047] As the ADC ramp signal falls to V1, at some point, the voltage of VASIL<n> will be equal to the ADC ramp signal, resulting in the comparator 118 asserting its output, stopping the ripple counter 120. The output of the ripple counter 120, as ADC_Out[n], during time period T4 thus represents the value of VASIL<n> when V_Black is selected by the multiplexer 114. If this value is not as expected, it can be inferred that the voltage regulator 112 is malfunctioning.

[0048] During time period T5, beginning after the end of time period T4, RegOutMux is deasserted, causing selection of the test white voltage V_White by the multiplexer 114 and its corresponding output as VASIL<n>. In addition, the ripple counter 120 is reset and begins counting again at the start of time period T5. The ADC ramp signal (having charged back to high by the end of time period T4) now falls from high to a second voltage V2 that is lower than the first voltage V1, representing a longer integration time.

[0049] As the ADC ramp signal falls to V2, at some point, the voltage of VASIL<n> will be equal to the ADC ramp signal, resulting in the comparator 118 asserting its output, stopping the ripple counter 120. The output of the ripple counter 120, as ADC_Out[n], during time period T5 thus represents the value of VASIL<n> when V_White is selected by the multiplexer 114. If this value is not as expected, it can be inferred that the voltage regulator 112 is malfunctioning.

[0050] The end of time period T1 results in REGADCTEST and ADCTEST[n] falling low, resulting in VASIL_Enable[n] being output as low by the AND gate 113, and VASIL_EnableB[n] being output as high by the inverter 111. This opens switch S1, and closes switches S2 and S3, shunting nodes N0 and N3 to ground, removing the effect of the regulator voltage verification circuit 100 from the other circuitry, and grounding VASIL<n>.

[0051] Further details of the multiplexer 114 are now described with additional reference to FIG. 4. The multiplexer 114 includes switch S4 coupled between nodes N1 and N3 and switch S5 selectively coupled between nodes N2 and N3. Switch S4 selectively couples V_Black at Node N1 to node N3 in response the RegOutM ux signal, while switch S5 selectively couples switch V_White at node N2 to node N3 in response to a complement of the RegOutM UX signal, labeled here as RegOutM uxB.

[0052] When output of V_Black is desired, the RegOutM ux signal is asserted, closing switch S4 and opening switch S5, causing V_Black to be produced as VASIL<n>. It follows that when output of V_White is desired, the RegOutM ux signal is deasserted, opening switch S4 and closing switch S5, causing V_White to be output as VASIL<n>.

[0053] With additional reference to FIG. 5, the regulator voltage verification circuit 100 as implemented with the active imaging pixels 13 and analog processing and analog to digital conversion block 16 is now described. Here, the DCDS switch 116 receives the voltages VASIL<1>-VASIL<16>. It should be appreciated that sixteen instances of the VASIL voltage generation circuitry 98 (from FIG. 2) are used to generate the sixteen voltages VASIL<1>-VASIL<16>, and that when in test mode (REGADCTEST being asserted, and ADCTEST[n] for each VASIL voltage generation circuitry 98 being asserted), each of the voltages VASIL<1>-VASIL<16> selectively cycles between the test black voltage V_Black for that voltage or the test white voltage V_White for that voltage.

[0054] The DCDS 99 properly routes and couples the voltages VASIL<1>-VASIL<16> to other components of the pixel array 12, such as the readout path 115. Of note here is that the active imaging pixels 13 include visible (non-occluded) pixels 139, bias current generation and clamping block 134, and dark (occluded) pixels 136. By occluded, it is meant that other components are covering those pixels, so those pixels can return no value but a dark value.

[0055] The connections made by the DCDS switch 116 and the other components of the pixel array 12 are shown in FIG. 6. Here, it can be seen that each of the voltages VASIL<1>-VASIL<16> is potently coupled to sixteen (shown as X16) columns of the pixel array 12. As will be explained below, each of the voltages VASIL<1>-VASIL<16> may be coupled to every column of a respective group of sixteen, to two columns of a respective group of sixteen (which improves settling time), or to any number of columns of a respective group of sixteen.

[0056] An example shown in FIG. 7 is a scenario where the comparators 118, 119, and 121 of Col[1], Col[2], . . . , Col[16] are coupled to VASIL<n>. An optional buffer 123 is coupled to VASIL<n> to improve settling time.

[0057] An example shown in FIG. 8 is a scenario where the comparators 118 and 119 of Col[1] and Col[2] in a group of sixteen are coupled to VASIL<n>, while other comparators of the other columns are not. An optional buffer 123 is coupled to VASIL<n>to improve settling time. In addition, here, the selection of two out of sixteen columns also reduces capacitive loading to approximately one eighth of what it would be if all sixteen columns were coupled to VASIL<n>.

[0058] The switching circuitry used to couple the groups of sixteen columns to the voltages VASIL<1>-VASIL<16> is shown in FIG. 9. Here, NMOS transistor T1 has its source coupled to ground, its gate coupled to an inverse of the REGADCTEST signal, shown here as REGADCTESTB, and its drain coupled to VASIL<1>. NMOS transistor T2 has its source coupled to one group of sixteen columns, its gate coupled to the REGADCTEST signal, and its drain coupled to VASIL<1>. Thus, when REGADCTEST is not asserted, meaning that REGADCTESTB will be asserted, NMOS transistor T1 will turn on, while NM OS transistor T2 will turn off, resulting in the shunting of VASIL<1> to the reference voltage AVSSPIX. Likewise, when REGADCTEST is asserted, meaning that REGADCTESTB will not be asserted, NMOS transistor T1 will turn off, while transistor T2 turns on, resulting in NMOS transistor T2 acting as a switch and providing an output proportional to VASIL<1>.

[0059] The remainder of the circuitry used to couple the groups of sixteen columns to the voltages VASIL<1>-VASIL<16> is shown in FIG. 10. It is first noted that each of the switches S17 and S18 shown as abbreviations are actually NMOS transistor T2 (replicated for each of S17 and S18), while switch S3 is actually the NMOS transistor T1 (replicated as needed).

[0060] Nodes N4 and N5 respectively receive Pixel_Input [1] and Pixel_Input[2]. Switch S7 selectively couples node N4 to node N6 in response to the PI1_SELO signal. Switch S8 selectively couples node N5 to node N6 in response to the PI2_SELO signal. Switch S9 selectively couples node N4 to node N7 in response to the PI1_SEL1 signal. Switch S10 selectively couples node N5 to node N7 in response to the PI2_SEL1 signal.

[0061] Nodes N8 and N9 respectively receive the voltage VASIL<1>. Switches S17 and S18 selectively couple nodes N8 and N9 to nodes N13 and N14 in response to the REGADCTEST signal. Nodes N10 and N11 respectively receive the reference voltage signal VREF. Switches S13 and S14 selectively couple the nodes N10 and N11 to nodes N13 and N14 in response to the ENPIREF signal.

[0062] Switches S11 and S12 selectively couple nodes N6 and N7 to nodes N13 and N14 in response to the ENPI signal. Switches S15 and S16 selectively couple nodes N13 and N14 to the reference voltage AVSSPIX in response to the ENGNDCOMP signal.

[0063] The comparator **118** receives the signal at node N**13** through capacitor C**1** and the ADC ramp signal through capacitor C**2**. The comparator **119** receives the signal at node N**14** through capacitor C**3** and the ADC ramp signal through capacitor C**4**. Of note is that the capacitors C**2** and C**4** may in some instances, such as that shown, be variable capacitors and have capacitances that change responsive to the signals SELG**1**/SELG**4**/SELG**8** signal.

[0064] Operation of the DCDS switch **116** is now described with further reference to FIG. **11**. During the test operation, which occurs during time period T**1**, the REGADCTEST signal and VASIL_Enable[**1**] signal are asserted (deasserting VASIL_EnableB[**1**]), while the ENPI, ENPIREF, ENGNDCOMP, PI[**1**]_SEL**0**, PI**1**[**2**]_SEL**0**, PI[**1**]_SEL**1**, and PI[**2**]_SEL**1** signals are deasserted. This serves to close switches S**17**-S**18**, and open switches S**3**, S**7**-S**10**, and S**11**-S**16**. As a result, the voltage VASIL<**1**> is passed to nodes N**13** and N**14**. Functionality continues as explained above with reference to FIG. **2**, with the comparators **118** and **119** asserting their outputs when the voltages on nodes N**13** and N**14** are equal to the ADC ramp voltage.

[0065] Operation of the DCDS switch **116** during normal operations to perform digital correlated double sampling is not necessary, and proceeds according to those known techniques.

[0066] Referring back to FIG. **2**, and referring additionally to FIG. **12**, each row of the pixel array **12** is sequentially read out. This read out is diagrammatically shown in FIG. **12**. Here, it can be seen that in a pixel array **12** having N rows, for rows **1**-**6** and **9**-N, first the dark (occluded by other structures) columns of a given row of the active imaging pixels **13**, labeled here as **201** and **20**N, are read out. Then, the visible columns of a given row of the active imaging pixels **13**, labeled here as **401** and **40**N, are read out. In this specific example, rows **7** and **8** of the pixel array **12** include the regulator voltage verification circuit **100**. For these rows, only the voltage VASIL, labeled here as **307** and **308**, is read out. The test results provided by the ADCOUT[**7**] and ADCOUT[**8**] signals, for this instance, may optionally be averaged.

[0067] It should be appreciated however that any number of the rows may include the regulator voltage verification circuit **100**. For example, row **7** may include the regulator voltage verification circuit **100**.

[0068] While the disclosure has been described with respect to a limited number of embodiments, those skilled in the art, having benefit of this disclosure, will appreciate that other embodiments can be envisioned that do not depart from the scope of the disclosure as disclosed herein. Accordingly, the scope of the disclosure shall be limited only by the attached claims.

1. A circuit, comprising:

a supply voltage node;

at least one pixel powered from the supply voltage node, the at least one pixel including an imaging pixel and an analog to digital conversion circuit; and

a test voltage generation circuit configured to generate a test voltage as a function of a voltage at the supply voltage node;

wherein the analog to digital conversion circuit is configured to, in a normal mode, sample output from the imaging pixel and provide its output as digital data; and

wherein the analog to digital conversion circuit is configured to, in a test mode, sample the test voltage and provide its output as the digital data.

2. The circuit of claim **1**, further comprising a processor configured to, in the test mode, receive the digital data from the analog to digital conversion circuit, compare the digital data to an expected value, and to take corrective action based upon the digital data not being substantially equal to the expected value.

3. The circuit of claim **1**, wherein the test voltage generation circuit is configured to generate upper and lower test voltages representing upper and lower expected voltages of the output of the imaging pixel; wherein the test voltage generation circuit is configured to pass the upper test voltage as the test voltage in response to assertion of a multiplexer select signal, and to pass the lower test voltage as the test voltage in response to deassertion of the multiplexer select signal.

4. The circuit of claim **3**, wherein the test voltage generation circuit comprises:

a voltage divider coupled between the supply voltage node and a reference node, with a first tap of the voltage divider producing the upper test voltage and a second tap of the voltage divider producing the lower test voltage;

a multiplexer having inputs coupled to the first and second taps of the voltage divider to receive the upper and lower test voltages, and to pass one of the upper or lower test voltages as output based upon a logic level of the multiplexer select signal;

a logic circuit configured to receive as input a master test mode enable signal and an individual pixel test mode enable signal, and to generate a test mode enable signal as a result of a logical operation between the master test mode enable signal and the individual pixel test mode enable signal;

a first switch selectively coupling the supply voltage node to the voltage divider in response to the test mode enable signal;

a second switch selectively shunting the voltage divider to ground in response to an inverse of the test mode enable signal; and

a third switch selectively shunting the output of the multiplexer to ground in response to the inverse of the test mode enable signal.

5. The circuit of claim **4**, wherein the analog to digital conversion circuit comprises:

a switching circuit configured to receive the test voltage and output from the imaging pixel, and to pass the test voltage as output when in the test mode;

a comparison circuit configured to receive the output from the switching circuit and an analog to digital conversion signal, and to assert a counter reset signal when the output from the switching circuit and the analog to digital conversion signal are equal in voltage; and

a counter configured to begin counting at a beginning of each test cycle within the test mode, to stop counting upon assertion of the counter reset signal, and to output its count upon stopping counting.

6. The circuit of claim **5**, wherein the comparison circuit comprises a comparator configured to receive the output from the switching circuit at a first terminal through a first capacitor and the output from the analog to digital conversion signal at a second terminal through a second capacitor;

and wherein the analog to digital conversion signal comprises a voltage ramping signal ramping in a repeating pattern between, in order, a base voltage, a first voltage, the base voltage, and a second voltage, with the first voltage being unequal to the second voltage, and with the first and second voltages being different from the base voltage.

7. The circuit of claim **6**, wherein the ramping signal ramps to the first voltage when the multiplexer is set by the multiplexer select signal to pass the upper test voltage and ramps to the second voltage when the multiplexer is set by the multiplexer select signal to pass the lower test voltage.

8. The circuit of claim **5**, wherein the circuit is incorporated into an advanced driver assistance system for a vehicle; and wherein the switching circuit is configured to couple the test voltage to multiple columns of a pixel array.

9. The circuit of claim **8**, wherein the switching circuit is configured to couple the test voltage to a subset of columns within a group of columns to improve settling time and reduce capacitive loading.

10. The circuit of claim **9**, wherein the switching circuit couples the test voltage to two columns out of a group of sixteen columns.

11. The circuit of claim **1**, wherein the analog to digital conversion circuit includes a comparator and a ripple counter, the ripple counter configured to count until the comparator asserts its output when the test voltage equals a ramp signal.

12. The circuit of claim **1**, wherein the imaging pixel is part of a pixel array comprising multiple rows, and wherein at least one row of the pixel array includes the test voltage generation circuit.

13. The circuit of claim **12**, wherein the test voltage generation circuit is included in two consecutive rows of the pixel array.

14. The circuit of claim **13**, wherein digital data output from the analog to digital conversion circuit for the two consecutive rows is averaged to produce a test result.

15. A method for verifying a voltage regulator in an advanced driver assistance system, the method comprising:

providing power from the voltage regulator to at least one pixel, the at least one pixel including an imaging pixel and an analog to digital conversion circuit;

generating a test voltage as a function of an output voltage of the voltage regulator;

in a test mode, sampling the test voltage with the analog to digital conversion circuit to produce digital data; and

in a normal mode, sampling output from the imaging pixel with the analog to digital conversion circuit to produce the digital data.

16. The method of claim **15**, further comprising:

comparing the digital data to an expected value; and

taking corrective action based upon the digital data not being substantially equal to the expected value.

17. The method of claim **15**, wherein generating the test voltage comprises:

generating an upper test voltage and a lower test voltage representing upper and lower expected voltages of the output of the imaging pixel;

passing the upper test voltage as the test voltage in response to assertion of a multiplexer select signal; and

passing the lower test voltage as the test voltage in response to deassertion of the multiplexer select signal.

18. The method of claim **17**, wherein generating the upper test voltage and the lower test voltage comprises:

dividing the output voltage of the voltage regulator using a voltage divider coupled between a supply voltage node and a reference node to produce the upper test voltage at a first tap of the voltage divider and the lower test voltage at a second tap of the voltage divider.

19. The method of claim **18**, further comprising:

receiving a master test mode enable signal and an individual pixel test mode enable signal;

performing a logical operation between the master test mode enable signal and the individual pixel test mode enable signal to generate a test mode enable signal;

selectively coupling the supply voltage node to the voltage divider in response to the test mode enable signal;

selectively shunting the voltage divider to ground in response to an inverse of the test mode enable signal; and

selectively shunting an output of a multiplexer to ground in response to the inverse of the test mode enable signal.

20. The method of claim **17**, wherein sampling the test voltage comprises:

receiving the test voltage at a switching circuit;

passing the test voltage as output from the switching circuit when in the test mode;

comparing the output from the switching circuit to an analog to digital conversion signal at a comparison circuit;

asserting a counter reset signal when the output from the switching circuit and the analog to digital conversion signal are equal in voltage;

beginning counting at a counter at a beginning of each test cycle within the test mode;

stopping counting upon assertion of the counter reset signal; and

outputting a count upon stopping counting.

21. The method of claim **20**, wherein comparing the output from the switching circuit to the analog to digital conversion signal comprises:

receiving the output from the switching circuit at a first terminal of a comparator through a first capacitor;

receiving the analog to digital conversion signal at a second terminal of the comparator through a second capacitor; and

wherein the analog to digital conversion signal comprises a voltage ramping signal ramping in a repeating pattern between, in order, a base voltage, a first voltage, the base voltage, and a second voltage, with the first voltage being unequal to the second voltage, and with the first and second voltages being unequal to the base voltage.

22. The method of claim **21**, wherein the ramping signal ramps to the first voltage when a multiplexer is set by a multiplexer select signal to pass the upper test voltage and ramps to the second voltage when the multiplexer is set by the multiplexer select signal to pass the lower test voltage.

23. The method of claim **15**, further comprising providing the test voltage to multiple columns of a pixel array.

24. The method of claim **23**, further comprising providing the test voltage to a subset of columns within a group of columns to improve settling time and reduce capacitive loading.

25. The method of claim **15**, further comprising:

providing the test voltage to a first row of a pixel array to produce a first test result;

providing the test voltage to a second row of the pixel array to produce a second test result; and

averaging the first test result and the second test result.

26. The method of claim **15**, further comprising, upon determining that the digital data is not substantially equal to an expected value, outputting commands causing a vehicle to provide a warning that the advanced driver assistance system is malfunctioning.

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