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(54) **MODULE, APPARATUS, METHOD, AND NON-TRANSITORY COMPUTER READABLE STORAGE MEDIUM FOR LINEAR POWER-AMPLIFICATION USING CLASS-AB POWER AMPLIFIERS**

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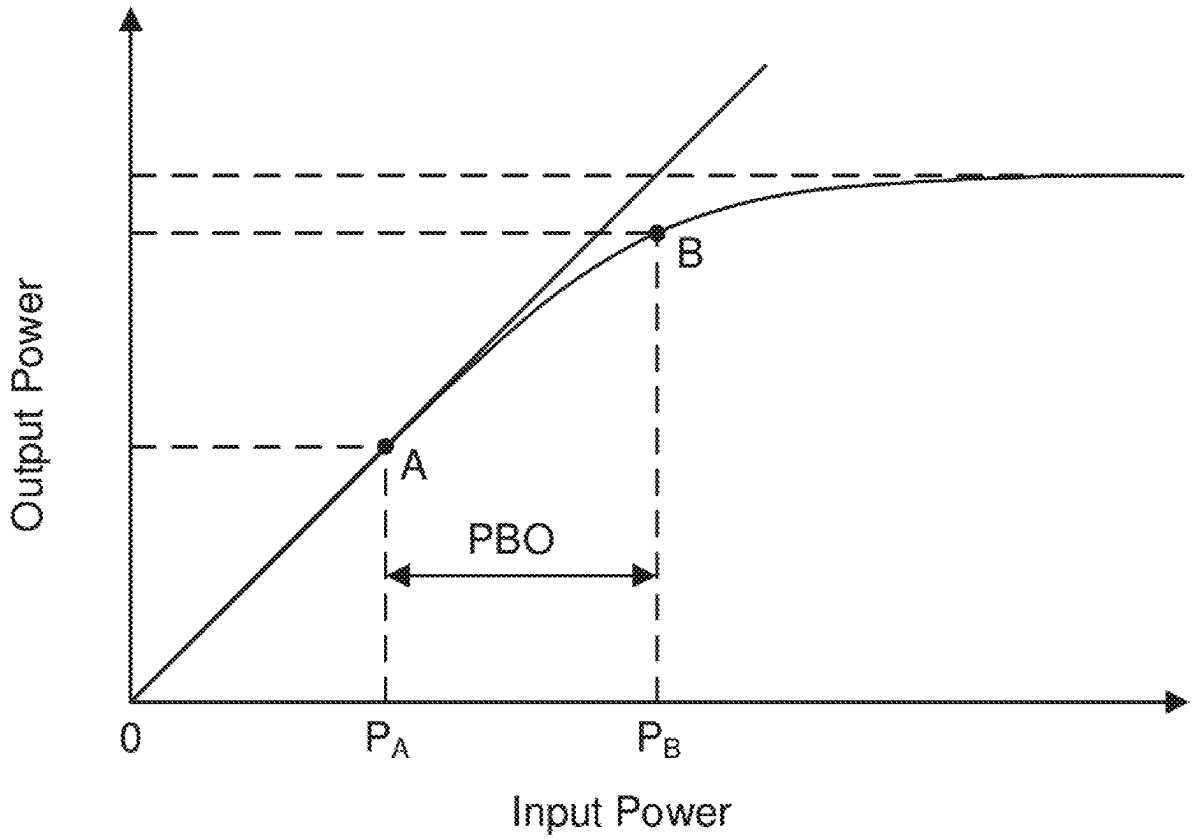
(57) **ABSTRACT**

A linear power-amplifier module has a splitter for splitting an input signal into a plurality split signals, a plurality of circuit branches connected to the splitter, each circuit branch for receiving one of the plurality of split signals, and an output connected to the plurality of circuit branches for combining outputs of the plurality of circuit branches and outputting an output signal. Each circuit branch is for receiving one of the plurality of split signals, each circuit branch comprises a class-AB PA operable under a biasing voltage, and one or more circuit branches each has a respective control circuit connected to an input of the class-AB PA thereof.



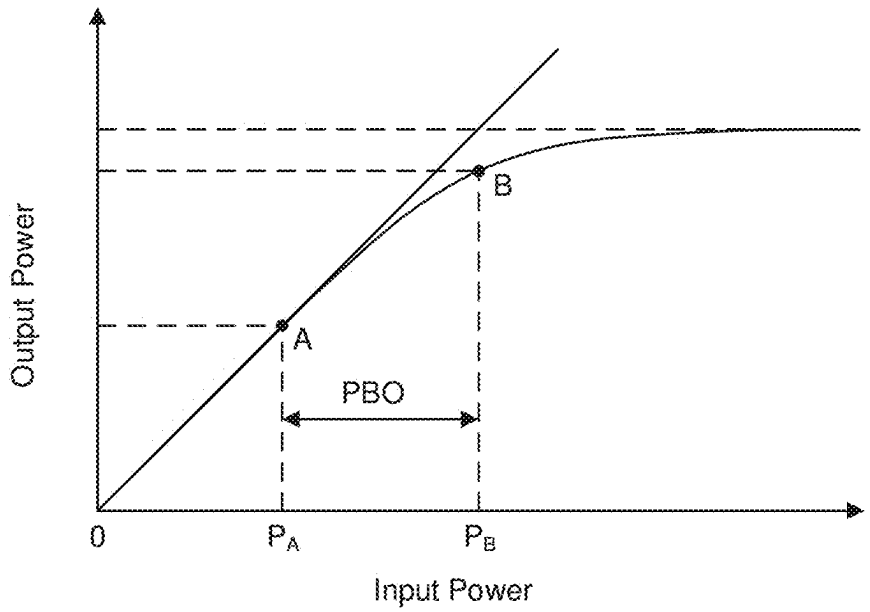


FIG. 1

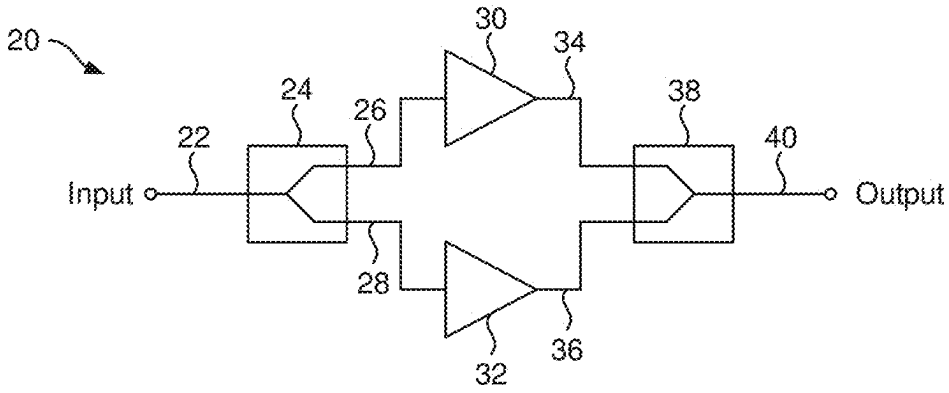


FIG. 2 (Prior Art)

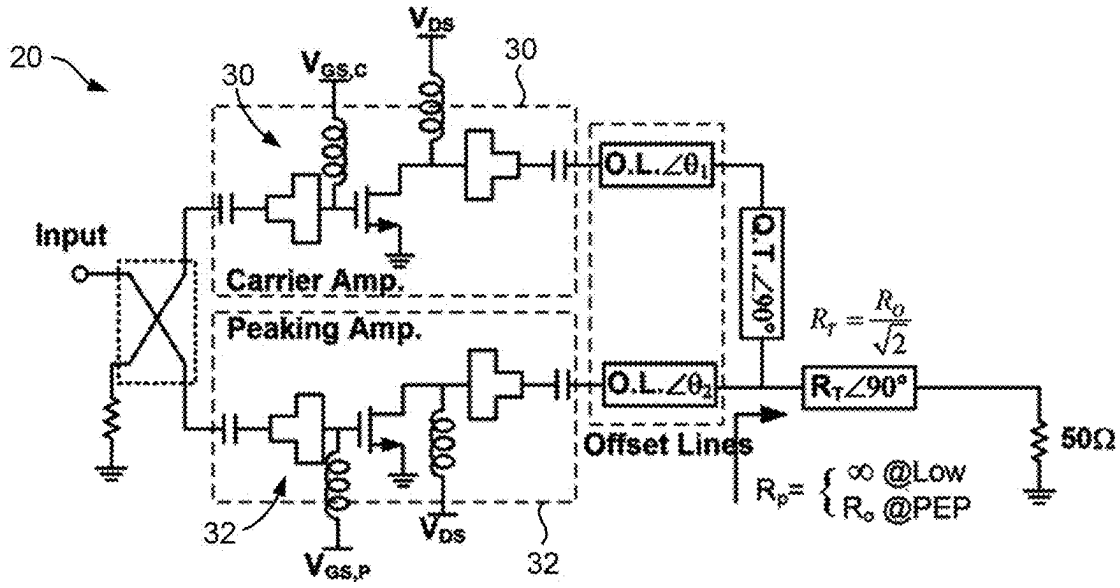


FIG. 3 (Prior Art)

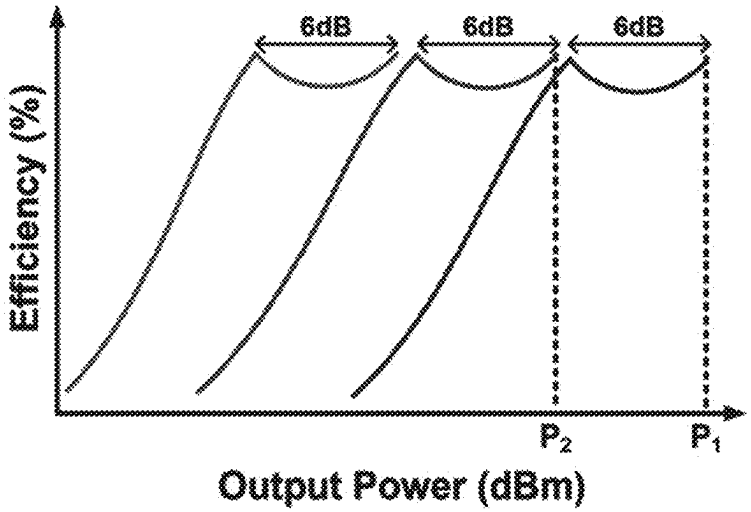


FIG. 4 (Prior Art)

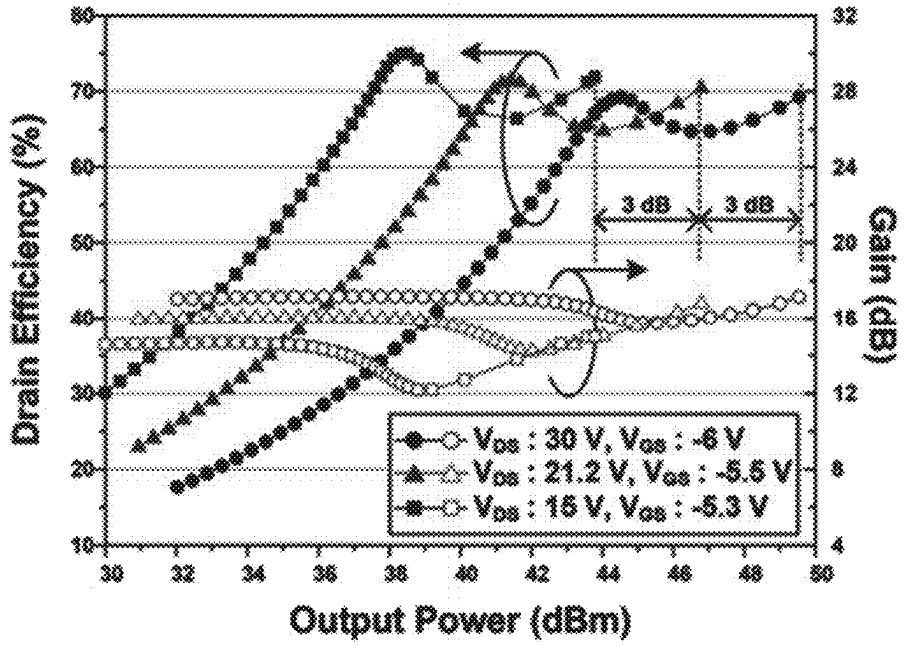


FIG. 5 (Prior Art)

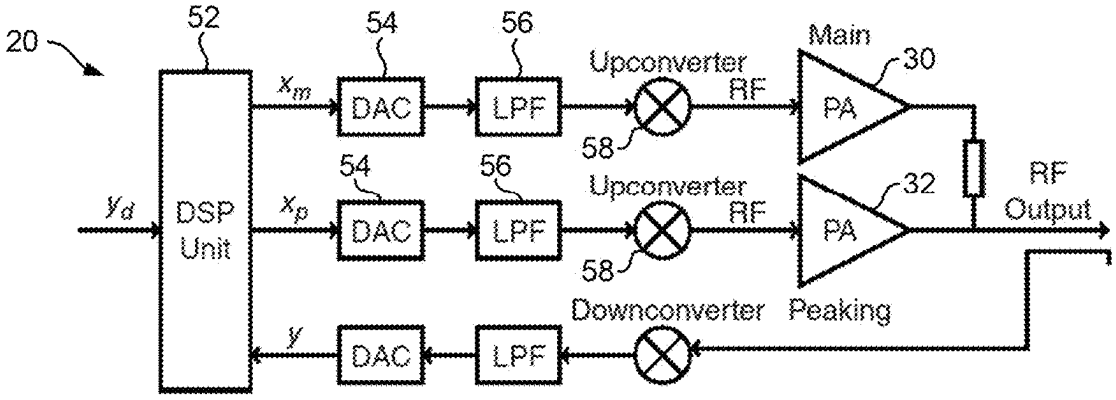


FIG. 6 (Prior Art)

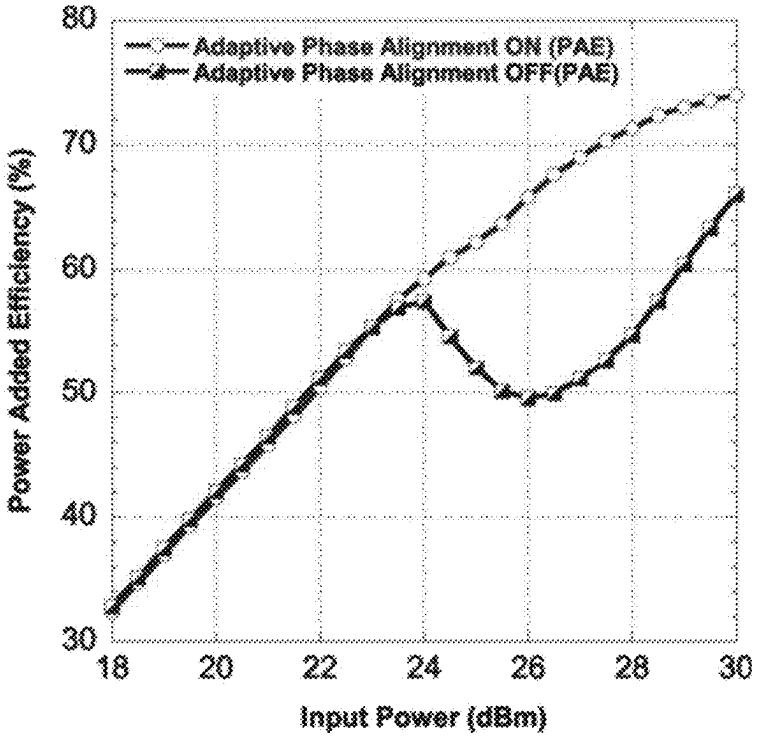


FIG. 7 (Prior Art)

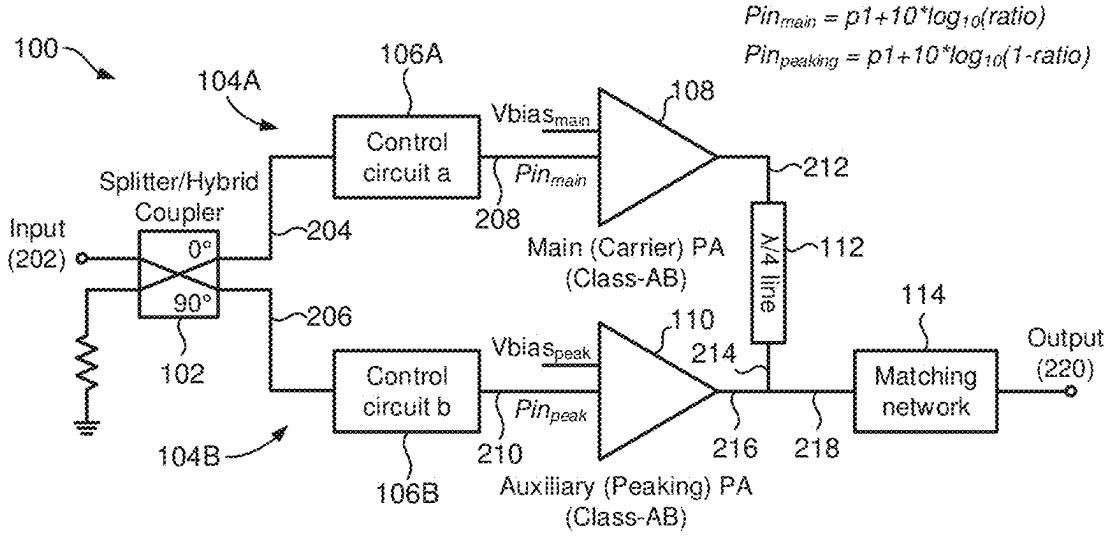


FIG. 8

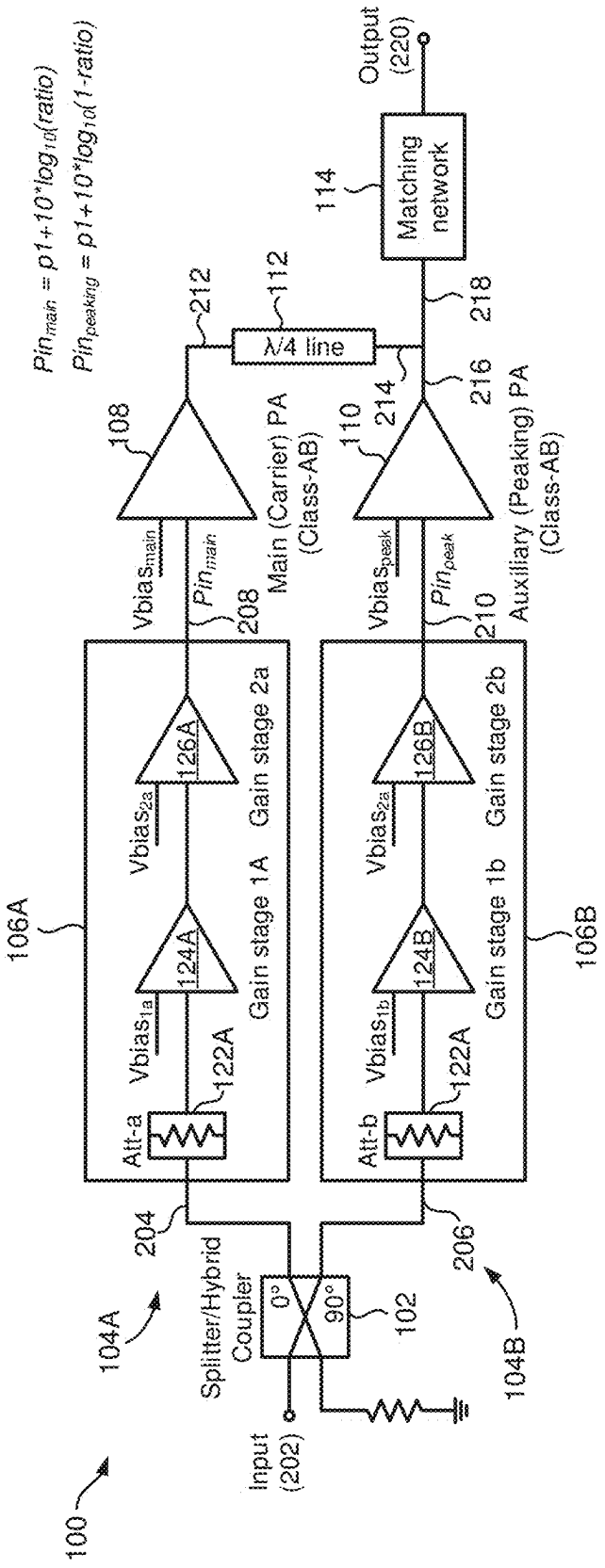

$Pin_{main} = p1+10*log_{10}(ratio)$
$Pin_{peaking} = p1+10*log_{10}(1-ratio)$
100
Input (202)
Splitter/Hybrid Coupler
0°
90°
102
104A
104B
204
206
106A
106B
Gain stage 1A
Gain stage 2a
Gain stage 1b
Gain stage 2b
Att-a
Att-b
122A
124A
124B
126A
126B
$Vbias_{1a}$
$Vbias_{1b}$
$Vbias_{2a}$
$Vbias_{main}$
$Vbias_{peak}$
208
210
Pin_{main}
Pin_{peak}
Main (Carrier) PA (Class-AB)
Auxiliary (Peaking) PA (Class-AB)
108
110
212
214
216
112
λ/4 line
218
114
Matching network
Output (220)

FIG. 9

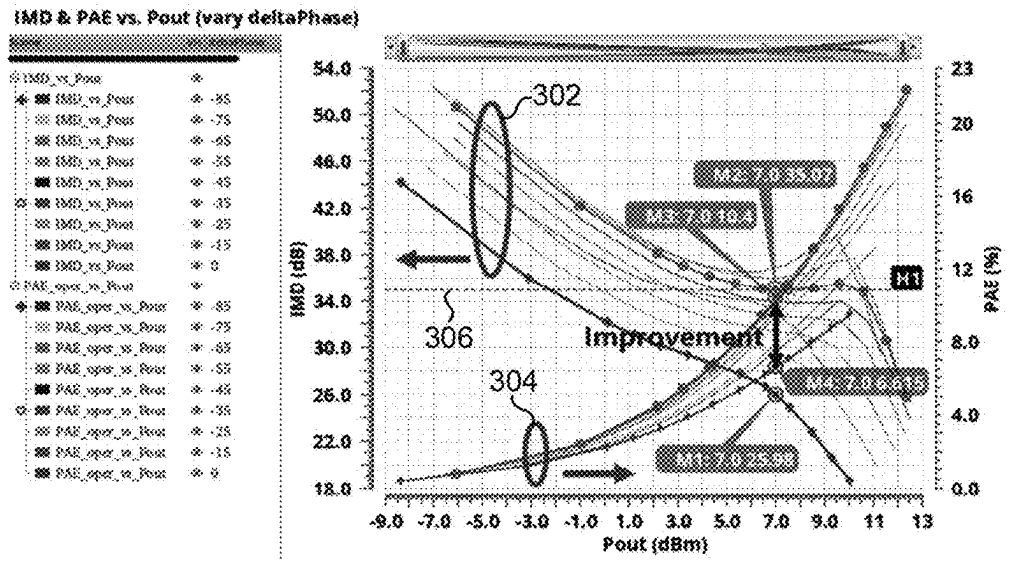

IMD & PAE vs. Pout (vary deltaPhase)
302
306
304
Improvement
IMD (dB)
PAE (%)
Pout (dBm)

FIG. 10

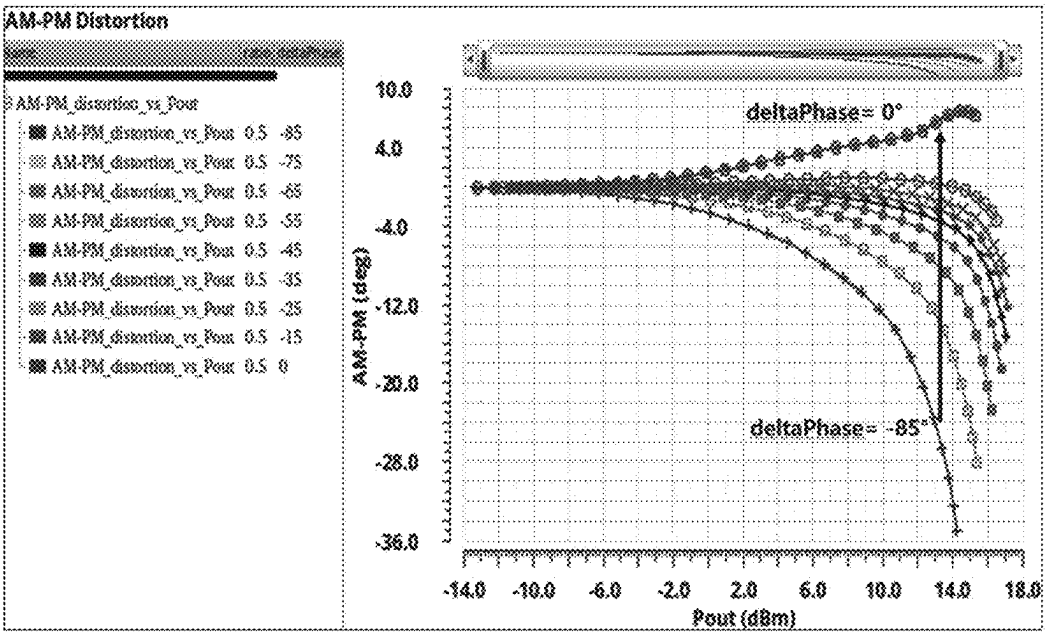

AM-PM Distortion
deltaPhase= 0°
deltaPhase= -85°
AM-PM (deg)
Pout (dBm)

FIG. 11

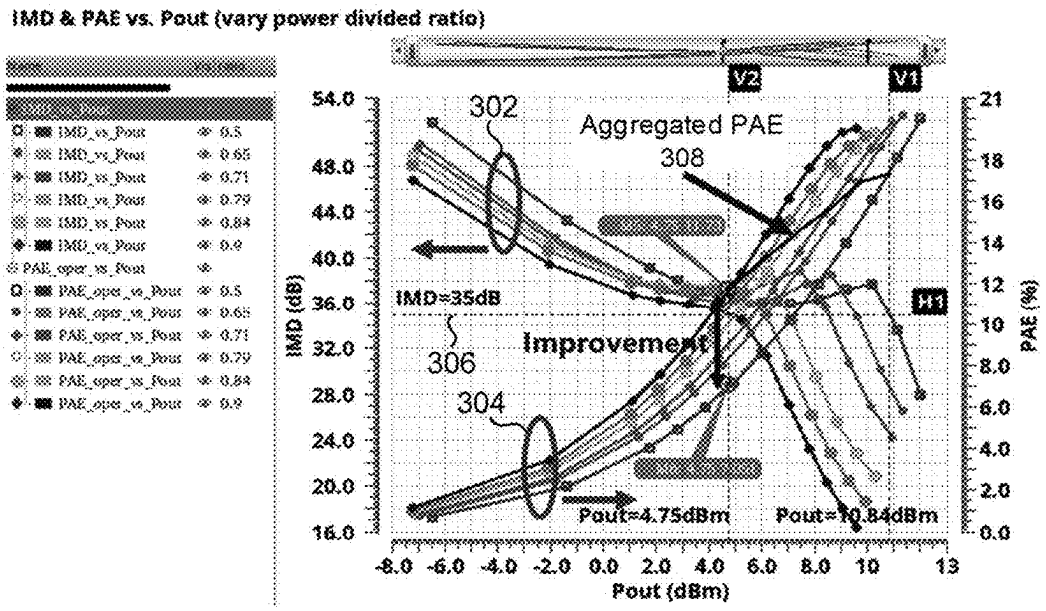

IMD & PAE vs. Pout (vary power divided ratio)
V2
V1
302
Aggregated PAE
308
IMD=35dB
306
Improvement
304
M1
Pout=4.75dBm
Pout=10.84dBm
IMD (dB)
PAE (%)
Pout (dBm)
54.0
48.0
44.0
40.0
36.0
32.0
28.0
24.0
20.0
16.0
21
18
16
14
12
10
8.0
6.0
4.0
2.0
0.0
-8.0
-6.0
-4.0
-2.0
0.0
2.0
4.0
6.0
8.0
10
13

FIG. 12

MODULE, APPARATUS, METHOD, AND NON-TRANSITORY COMPUTER READABLE STORAGE MEDIUM FOR LINEAR POWER-AMPLIFICATION USING CLASS-AB POWER AMPLIFIERS

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application is a continuation of Patent Cooperation Treaty Application No. PCT/CN2023/071459, entitled "MODULE, APPARATUS, METHOD, AND NON-TRANSITORY COMPUTER READABLE STORAGE MEDIUM FOR LINEAR POWER-AMPLIFICATION USING CLASS-AB POWER AMPLIFIERS," filed on Jan. 9, 2023, the entirety of which is incorporated by reference herein.

TECHNICAL FIELD

[0002] The present disclosure relates generally to module, apparatus, method, and non-transitory computer readable storage medium for linear power-amplification, and in particular to module, apparatus, method, and non-transitory computer readable storage medium for linear power-amplification using class-AB power amplifiers.

BACKGROUND

[0003] Wireless communication systems such as millimeter-wave (mmWave) fifth-generation (5G) systems, sixth-generation (6G) systems, and the like typically employ phase arrays with high-order quadrature amplitude modulations (QAMs) to overcome the high path-loss of free space and to provide high data-throughput and low latency. Such systems often require amplitude adjustment and/or reduction of power levels of signals to facilitate beam shaping. However, the low and variable power levels may reduce the operation efficiency and make the designing of the systems under a fixed, maximum power requirement inefficient.

[0004] The complex QAM signals usually have high peak-to-average power ratio (PAPR), which may cause power amplifiers (PAs) to operate at higher power back-off (PBO) from the peak to maintain linearity, and thus greatly reduce the efficiency at the low output powers for conventional Class-A, Class-AB and Class-B PAs.

SUMMARY

[0005] According to one aspect of this disclosure, there is provided a linear power-amplification module comprising: a splitter for splitting an input signal into a plurality split signals; a plurality of circuit branches connecting to the splitter, each circuit branch for receiving one of the plurality of split signals; and an output connecting to the plurality of circuit branches for combining outputs of the plurality of circuit branches and outputting an output signal; each circuit branch is for receiving one of the plurality of split signals; each circuit branch comprises a class-AB power-amplifier (PA) operable under a biasing voltage; and one or more circuit branches each comprises a respective control circuit connected to an input of the class-AB PA thereof.

[0006] In some embodiments, each circuit branch comprises the respective control circuit connected to the input of the respective class-AB PA thereof.

[0007] In some embodiments, the one or more control circuits of the one or more circuit branches are configured for adjusting input powers of the class-AB PAs.

[0008] In some embodiments, the one or more control circuits of the one or more circuit branches are configured for adjusting the input powers of the class-AB PAs by adjusting power-division percentages of the input powers of the class-AB PAs in accordance with

$$\mathrm{Pin}_i = P1 + 10\log_{10}(x_i)$$

[0009] where P1 is an power proportional to power of the input signal, i=1, 2, . . . , N is the index of the class-AB PAs, N is the total number of the class-AB PAs, Pin_i is the input power of the i-th class-AB PA, x_i is the power-division percentage of the input power of the i-th class-AB PA, $1 \geq x_i \geq 0$, and $\Sigma_{i=1}^{N} x_i = 1$.

[0010] In some embodiments, the one or more control circuits of the one or more circuit branches are configured for adjusting the biasing voltage of at least one of the class-AB PAs.

[0011] In some embodiments, the one or more control circuits of the one or more circuit branches are configured for adjusting the biasing voltage of at least one of the class-AB PAs by adjusting biasing current of the of at least one of the class-AB PAs.

[0012] In some embodiments, the one or more control circuits of the one or more circuit branches are configured for applying phase adjustment between input signals of the class-AB PAs of the circuit branches.

[0013] In some embodiments, at least one of the one or more control circuits of the one or more circuit branches comprises at least one of an attenuator and one or more adjustment amplifiers.

[0014] In some embodiments, the one or more control circuits of the one or more circuit branches are configured for adjusting the input powers of the class-AB PAs by adjusting at least one of an attenuation of the attenuator and biasing voltage of each of the one or more adjustment amplifiers.

[0015] In some embodiments, the one or more control circuits of the one or more circuit branches are configured for adjusting the phase shift between the input signals of the class-AB PAs of the circuit branches by adjusting biasing voltage of at least one of the one or more adjustment amplifiers.

[0016] In some embodiments, the linear power-amplification module comprises two circuit branches each comprising the respective control circuit connected to the input of the respective class-AB PA thereof.

[0017] In some embodiments, the one or more control circuits of the one or more circuit branches are configured for adjusting input powers of the class-AB PAs a parameter r in accordance with

$$\mathrm{Pin}_{main} = P1 + 10\log_{10}(r)$$

$$\mathrm{Pin}_{peaking} = P1 + 10\log_{10}(1 - r)$$

[0018] where P1 is a power proportional to the power of the input signal, Pin_{main} and $Pin_{peaking}$ are the input powers of the two class-AB PAs, respectively, and $1 \geq r \geq 0$.

[0019] In some embodiments, $1 \geq r \geq 0.5$.

[0020] In some embodiments, the two control circuits of the two circuit branches are configured for adjusting the bias voltages of the two class-AB PAs, or for adjusting the biasing voltage of a peaking PA of the two class-AB PAs while maintaining the biasing voltage of a main PA of the two class-AB PAs constant.

[0021] In some embodiments, at least one of the plurality of circuit branches comprises an impedance inverter coupled to an output of the class-AB PA.

[0022] In some embodiments, the plurality of circuit branches are connected to the output via a matching network.

[0023] According to one aspect of this disclosure, there is provided a method for determining a phase-adjustment value for used in the above-described linear power-amplification module, the method comprising: introducing a series of phase-shift values to the plurality of circuit branches while fixing power proportionality and the biasing voltages of the class-AB PAs; for each of the series of phase-shift values, inputting signals of different powers to the linear power-amplification module and determining a set of intermodulation distortion (IMD) values and a set of power-added-efficiency (PAE) values for the phase-shift value, thereby obtaining a plurality of sets of IMD values and a plurality of sets of PAE values; identifying one or more phase-shift values whose corresponding IMD values within a target power output or power input range are greater than an IMD threshold; and for each of a plurality of power output or power input values within the target power output or power input range, selecting, from the identified one or more phase-shift values, a phase-shift value with greatest PAE value as the phase-adjustment value for the power output or power input value.

[0024] According to one aspect of this disclosure, there is provided a method for determining a plurality of power proportionality values of the class-AB PAs for used in the above-described linear power-amplification module, the method comprising: introducing a series of power-proportionality values of the class-AB PAs; for each of the series of power-proportionality values, inputting signals of different powers to the linear power-amplification module and determining a set of IMD values and a set of PAE values for the phase-shift value, thereby obtaining a plurality of sets of IMD values and a plurality of sets of PAE values; identifying one or more power-proportionality values whose corresponding IMD values within a target power output or power input range are greater than an IMD threshold; and for each of a plurality of power output or power input values within the target power output or power input range, selecting, from the identified one or more power-proportionality values, a power-proportionality value with greatest PAE value as the determined power-proportionality value for the power output or power input value.

[0025] According to one aspect of this disclosure, there is provided a method for determining one or more values of one or more parameters for used in the above-described linear power-amplification module, the method comprising: introducing a plurality of sets of parameter values of the one or more parameters to the linear power-amplification module; for each set of the parameter values, inputting signals of different powers to the linear power-amplification module and determining a set of IMD values and a set of PAE values for the set of parameter values, thereby obtaining a plurality of sets of IMD values and a plurality of sets of PAE values; identifying one or more sets of parameter values whose corresponding IMD values within a target power output or power input range are greater than an IMD threshold; and for each of a plurality of power output or power input values within the target power output or power input range, selecting, from the identified one or more set of parameter values, a set of parameter values with greatest PAE value as the determined power-proportionality value for the power output or power input value.

[0026] In some embodiments, the one or more parameters comprise at least one of phase-adjustment between the circuit branches, and power proportionality of the class-AB PAs.

[0027] According to one aspect of this disclosure, there is provided a non-transitory computer readable storage medium having stored thereon computer-executable instructions that, when executed by a computer, cause the computer to perform the method shown above.

[0028] The linear power-amplification module disclosed herein provides various benefits, such as:

[0029] both the main and peaking PAs are operated in their linear Class-AB regions, and thus there is no need for matching of peaking and compression response at final response;

[0030] the adaptive biasing of both main and peaking PAs improves the efficiency and linearity of the linear power-amplification module at the same time, and thus the main PA may be maintained at ideal load for required output power to ensure linearity and efficiency performance without dynamic load variation;

[0031] by using the simple LUT method to digitally control the attenuators, the gain amplifiers, and the driver amplifiers to reconfigure the input power-division ratio and phase shift, the system complexity is reduced due to analog linearization with simple LUT digital-control instead of using complex DSP and/or DPD and changing drain biasing as in prior art;

[0032] the linear power-amplification module disclosed herein is not frequency dependent and does not need complex high-speed DSP, DAC and DPD; and

[0033] the linear power-amplification module disclosed herein may be used in embodiments using phase array tapering for changing the relative output power with improved efficiency while maintaining required linearity.

BRIEF DESCRIPTION OF THE DRAWINGS

[0034] For a more complete understanding of the disclosure, reference is made to the following description and accompanying drawings, in which:

[0035] FIG. **1** is a plot showing the input/output relationship of a linear power amplifier (PA);

[0036] FIG. **2** is a schematic diagram showing the structure of a conventional average-power tracking Doherty power amplifier (DPA);

[0037] FIG. **3** is a circuit diagram of a conventional average-power tracking DPA;

[0038] FIG. **4** is a plot showing the behavior of the average-power tracking DPA shown in FIG. **2**;

[0039] FIG. **5** is a plot showing simulation results of the average-power tracking DPA shown in FIG. **2** with reduced power operation;

[0040] FIG. **6** is a schematic diagram showing a dual-input DPA transmitter architecture;

[0041] FIG. **7** is a plot showing the simulated power-added-efficiency (PAE) of the dual-input DPA shown in FIG. **6** with and without adaptive phase alignment;

[0042] FIG. **8** is a schematic diagram showing an analog linear power-amplification module, according to some embodiments of this disclosure;

[0043] FIG. **9** is a schematic diagram showing the detail of the linear power-amplification module shown in FIG. **8**, according to some embodiments of this disclosure;

[0044] FIG. **10** is a plot showing the sample simulation results of the intermodulation distortion (IMD) and PAE of the linear power-amplification module shown in FIG. **9** vs. the output power thereof at different input-signal phase-shifts but with fixed input power-division ratio;

[0045] FIG. **11** is a plot showing the sample simulation results of the amplitude-to-phase (AM-PM) distortion of the linear power-amplification module shown in FIG. **9** vs. the output power thereof at different input-signal phase-shifts but with fixed input power-division ratio; and

[0046] FIG. **12** is a plot showing the sample simulation results of the IMD and PAE of the linear power-amplification module shown in FIG. **9** vs. the output power thereof with different input power-division ratios at a fixed phase shift.

DETAILED DESCRIPTION

A. Linear Power Amplifier

[0047] Conventional linear-mode power amplifiers (PAs) generally include Class-A, Class-B, and Class-AB PAs defined by the varying conduction angles. More specifically, Class-A PAs have a conduction angle of 360°, Class-B PAs have a conduction angle of 180°, and class-AB PAs have a conduction angle between 180° and 360°.

[0048] A linear-mode PA generally has a limited linear range. FIG. **1** shows the input/output power relationship of a linear-mode PA. As shown, the input/output power relationship is generally linear (that is, the output power is a linear amplification of the input power) between the origin and the P1dB point B (thereby defining an input linear range from zero (0) to PB), wherein the P1dB point is the point where the output power is one (1) decibel (dB) smaller than the otherwise linearly amplified power value. When the input power is greater than PB, the output is significantly distorted (that is, no longer a linear amplification of the input power) and eventually saturated to a maximum output power.

[0049] Signals having high peak-to-average power ratio (PAPR) such as the quadrature amplitude modulation (QAM) signals generally have maximum powers significantly greater than the average powers thereof. Thus, when using a PA to amplify a signal with high PAPR, the operation point A of the PA (corresponding to the average power of the signal) has to sufficiently "back off" from the saturation point S. In other words, the average power PA of the signal input to the PA has to be sufficiently smaller than PB (the upper bound of the PA's linear range) to ensure that the entire signal may be linearly amplified without significant distortion. The difference between PB and PA is denoted power back-off (PBO). A high PBO may greatly reduce the efficiency at the low output powers for conventional linear-mode PAs, thereby causing a low PBO efficiency problem.

[0050] The Doherty power amplifier (DPA) provides a solution to the low PBO efficiency problem. As shown in FIG. **2**, the conventional DPA **20** comprises a splitter or hybrid coupler **24** to split the input signal **22** into two signals **26** and **28** with a 90° phase shift therebetween. The signal **26** passes through a main PA **30** (also denoted a "carrier PA") which is a Class-A or Class-AB PA operating on the entire input signal **26**. The signal **28** passes through a peak PA **32** (also denoted a "peaking PA") which is a Class-C PA only operating on a peak-power portion of the input signal **28** (that is, the peak PA **32** is off on a major portion of the input signal **28** and is turned on only when the power of the input signal **28** is greater than a threshold). By carefully choosing the parameters of the PAs **30** and **32**, the peak PA **32** may be on and operate when the main PA **30** starts to saturate. The outputs **34** and **36** of the PAs **30** and **32** are combined (with an inverse 90° phase shift) by a combiner **38** to use the output **36** of the peak PA **32** to compensate for the peak distortion/saturation of the output **34** of the main PA **30**. The combined output signal **40** is then a substantially linearly amplified version of the input signal **22**.

[0051] The conventional DPA **20** suffers from potential linearity issue of final response (that is, the output signal **40**). First, at low input power level, only the main PA **30** is on and operates at peak or near peak power-added-efficiency (PAE) at the PBO. Second, at high input power levels, the peak PA **32** begins to conduct and rely on active load modulation to change the load seen at the main PA **30**. Any additional un-wanted non-linearity caused by this load modulation would directly affect the final response.

[0052] FIG. **3** is a circuit diagram of an average-power tracking DPA **20** described in Reference [1], wherein the carrier PA **30** is a Class-A or Class-AB PA, and the peaking PA **32** is a Class-C PA. The average-power tracking DPA **20** provides further extended efficiency range (greater than 6 dB at PBO) by changing the drain-bias voltage V_{DS} and the gate-bias voltages $V_{GS,C}$ and $V_{GS,P}$ of the carrier and the peak PAS **30** and **32**.

[0053] FIG. **4** is a plot showing the behavior of the average-power tracking DPA **20** shown in FIG. **3**. When the peak output power is decreased from P_1 to P_2, the average-power tracking DPA **20** needs to reduce the drain-bias and gate-bias voltages V_{DS}, $V_{GS,C}$, and $V_{GS,P}$ to achieve high efficiency at a low peak power P2. Sample simulation results of the average-power tracking DPA **20** are shown in FIG. **5**. As those skilled in the art will understand, in the average-power tracking DPA **20** shown in FIG. **3**, changing the drain-bias voltage requires digital trimming of the internal or external power supply regulator, which may further increase the system complexity and power consumption, and the power efficiency improvement thereof may be degraded.

[0054] FIG. **6** is a schematic diagram showing a DPA **20** proposed in Reference [2] and described in Reference [3], wherein the carrier PA **30** is a Class-A or Class-AB PA, and the peaking PA **32** is a Class-C PA. The DPA **20** shown in FIG. **6** improves the PAE with the adaptive phase alignment. As shown, the dual input signals Y_d (comprising the In-phase and Quadrature (I/Q) components and upconverters **58**) are processed by the digital signal processing (DSP) unit **52** and the digital-to-analog convertors (DACs) **54** (also passing the lowpass filters (LPFs) **56**) to adaptively align the

phases of the carrier and peaking paths for all power levels when the peaking PA **32** is on in order to optimize the overall efficiency of the DPA **20**. FIG. **7** is a plot showing the improvement of the PAE.

[0055] However, the dual inputs with DSP technique only take care of the phase alignment of the main and peaking PAs **30** and **32** to prevent efficiency degradation.

[0056] Digital predistortion (DPD) can potentially solves the linearity problem with the DPAs. For example, the DPAs shown in FIGS. **3** and **6** may use advanced DPD algorithms to improve the linearity performance thereof. However, DPD may not be preferable due to low output power levels in millimeter-wave (mmWave) applications and the system complexity thereof (because of high signal bandwidth and large number of PAs requiring linearization).

[0057] High efficiency and high linearity PAs are always desirable in wireless communication systems, especially in mmWave, 5G, beyond-the-fifth-generation (B5G), 6G phase arrays with the complex modulation methods for high throughputs, wherein the systems require PAs to operate with high PAPR and at the PBO from the peak power.

[0058] In the following, a cost-effective analog linear PA is disclosed, which may be suitable for use in wireless communication systems such as 5G and 6G systems with improved efficiency and linearity of the PA at the PBO. The linear PA disclosed here may be considered an improved DPA for providing a cost-effective solution to optimize the power efficiency and linearity at the PBO region to satisfy the system requirement of phase arrays with high-order QAMs. The PBO efficiency and linearity of the DPA are optimized at the same time in the analog domain without using DPD linearization, thereby effectively reducing the overall system complexity.

[0059] Turning now to FIG. **8**, an analog linear power-amplification module according to some embodiments of this disclosure is shown and is generally identified using reference numeral **100**. In various embodiments, the linear power-amplification module **100** may be used in any suitable wireless communication systems such as in the RF, mmWave, 5G, beyond the fifth generation (B5G), 6G transceivers thereof with complex modulation methods for high throughputs and requiring high efficiency and high linearity PAs to operate with high PAPR at the PBO from the peak power. The linear power-amplification module **100** allows a range of operating output powers with improved efficiency but maintain reasonable linearity.

[0060] As shown, the linear power-amplification module **100** has a modified DPA structure and comprises a splitter or hybrid coupler **104** to split an input signal **202** into a first split signal **204** and a second split signal **206**. In these embodiments, the first and second signals **204** and **206** are of substantially equal amplitudes and with a phase shift such as a 90° phase-shift therebetween.

[0061] The first signal **204** goes through a first branch or path **104**A, passing a first control circuit **106**A and then being amplified by a main PA **108** which in these embodiments is a Class-AB PA. The amplified first signal **212** the passes an impedance inverter **112** such as a quarter-wave (V**4**, where) is the wavelength of the first signal **204**) transmission line, which modulates the load seen at the output of the main PA **108** and applies a –90° phase shift to the amplified first signal **212** to counter the phase shift introduced by the splitter **104**. An amplified and phase-corrected first signal **214** is then output from the impedance inverter **112**. In the simplest embodiment, the control circuit **106**A may only comprise gain stages with no level adjustment or bias control. The control circuit **106**A may also contain a phase adjustment.

[0062] The second signal **206** goes through a second branch or path **104**B, passing a second control circuit **106**B and then being amplified by a peaking PA **110** which in these embodiments is a Class-AB PA. The amplified second signal **216** and the amplified and phase-corrected first signal **214** (which are in-phase) are combined to form a combined signal **218** which is a linear amplification of the input signal **202**. Those skilled in the art will recognized that signal **216** when combined with signal **212** may vary the impedance seen by the main amplifier **108** in an inverse relationship to the relative levels of signal **216** and **212**. In these embodiments, the combined signal **218** passes a matching network **114** for output. As those skilled in the art will appreciate, the matching network **114** is used to transform the load to a desired impedance at the output connection of the peaking and main PAs **108** and **110** in order to optimize the overall efficiency and linearity. Those skilled in the art will also appreciate that other DPA topologies such as those employing for example series- or parallel-coupled transformers or other means of splitting signal **202** into signals **204/206** and combining signals **212/216** into signal **218** may be improved in a similar manner.

[0063] In these embodiments, the control circuits **106**A and/or **106**B use an adaptive control method such as a calibration-based control method or a look-up table (LUT) based control method (described in more detail later) to adaptively control the input powers Pin_{main} and $Pin_{peaking}$ of the main PA **108** and the peaking PA **110**, respectively, and the operation points thereof if the output characteristics are repeatable and depending on the required/expected target output power.

[0064] For example, in some embodiments where non-constant-envelope signals (that is, the signals whose envelope (that is, the peaks thereof) are non-constant) such as QAM signals are used as the input signal **202**, the output signal **220** is a linearly amplified version of the input QAM signals. In these embodiments, the input and output powers of the linear power-amplification module **100**, and Pin_{main} and $Pin_{peaking}$ of the main PA **108** and the peaking PA **110** refer to the respective powers in accordance with a non-constant-envelope signal input to the linear power-amplification module **100**.

[0065] The control circuits **106**A and/or **106**B may use the adaptive control method to adjust Pin_{main} and $Pin_{peaking}$ of the main PA **108** and the peaking PA **110** and the operation points thereof based on the target output power (or equivalently, the input power, for example, the power of each input QAM signal) to achieve linear amplification of the input signal **202** with improved PAE, wherein the amplification linearity may be measured by the intermodulation distortion (IMD) of the output signal **220**. For example, the output signal **220** may be represented as:

$$y(t) = \alpha x(t) + d(t) \quad (1)$$

[0066] where y(t) is the output signal **220**, x(t) is the input signal **202**, α is the amplification factor, and d(t)

is the distortion introduced by the nonlinearity of the linear power-amplification module **100**. Then, the IMD may be defined as:

$$IMD = P_x - P_d \quad (2)$$

[0067] where P_x and P_d are the power in dB or decibel-milliwatts (dBm) of x(t) and d(t).

[0068] For example, in some embodiments, the control circuits **106**A and/or **106**B may use the adaptive control method to adjust a power-division ratio r ($1 \geq r \geq 0$) for adjusting Pin_{main} and $Pin_{peaking}$ for varying the load on main PA **108** as follows:

$$Pin_{main} = P1 + 10\log_{10}(r) \quad (3)$$

$$Pin_{peaking} = P1 + 10(1 - r) \quad (4)$$

[0069] where P1 is a power proportional to the input power (that is, the power of an input QAM signal as the input signal **220**) which corresponds to the target output power (that is, the target power of the output signal **220**). In these embodiments, the power-division ratio $1 \geq r \geq 0.5$.

[0070] With the adjustment of Pin_{main} and $Pin_{peaking}$ of the main PA **108** and the peaking PA **110**, the adaptive control method may also accordingly adjust the bias voltage $Vbias_{main}$ of the main PA **108** and the bias voltage $Vbias_{peak}$) of the peaking PA **110** to ensure that they operate within their Class-AB linear regions. In some embodiments, the bias voltages $Vbias_{main}$ and $Vbias_{peak}$ of the main and peaking PAs **108** and **110** may be adjusted, for example, by adjusting their bias currents as follows:

$$Iref_{main} = I_{main} - (m - 0.5) \times I_{sub} \quad (5)$$

$$Iref_{peaking} = Iref_{main} * (1 - (m - 0.5)/0.5) \quad (6)$$

[0071] where $Iref_{main}$ is the reference bias current of the main PA **108** (that is, the bias current of the main PA **108** to be adjusted thereto), $Iref_{peaking}$ is the reference bias current of the peaking PA **110**, I_{main} is the input current of the main PA **108**, I_{sub} is a predefined current value, and m is the current mirror ratio. In these embodiments, I_{main} and I_{sub} are constant currents depending on the required or expected target output power range of the linear power-amplification module **100** (equivalent to the input power range), and the current mirror ratio m has the same value as the power-division ratio r (that is, m=r).

[0072] Based on Equations (5) and (6), the adaptive control method may use various ways to adjust or control the biasing voltage $Vbias_{main}$ and $Vbias_{peak}$ of the main and peaking PAS **108** and **110**. For example, in one embodiment, the adaptive control method may set the reference bias current $Iref_{main}$ (and thus the biasing voltage $Vbias_{main}$) of the main PA **108** and thus the biasing voltage $Vbias_{main}$ thereof to a constant level (except possible variation thereof for typical process and temperature compensation, which is out of the scope of this disclosure and is omitted), and adjusts or controls the reference bias current $Iref_{peaking}$ of the peaking PA **110** to set the $Vbias_{peak}$. In another embodiment, the adaptive control method may adjust or control both reference bias currents $Iref_{main}$ and $Iref_{peaking}$ to set the $Vbias_{main}$ and $Vbias_{peak}$.

[0073] FIG. **9** is a schematic diagram showing the detail of the linear power-amplification module **100** according to some embodiments of this disclosure. As shown, the first control circuit **106**A comprises a high-resolution attenuator (Att-a) **122**A such as a digital-control attenuator for receiving the first signal **204**, a gain amplifier (Gain stage **1***a*) **124**A connecting to the attenuator **122**A, and a driver amplifier (Gain stage **2***a*) **126**A connecting the gain amplifier **124**A to the main PA **108**.

[0074] Similarly, the second control circuit **106**B comprises a high-resolution attenuator (Att-b) **122**B such as a digital-control attenuator for receiving the second signal **206**, a gain amplifier (Gain stage **1***b*) **124**B connecting to the attenuator **122**B, and a driver amplifier (Gain stage **2***b*) **126**B connecting the gain amplifier **124**B to the peaking PA **110**. In these embodiments, the corresponding components **122**A and **122**B, **124**A and **124**B, and **126**A and **126**B of the main path **106**A and the peaking path **106**B are substantially identical. For ease of description, the gain amplifiers **124**A and **124**B and the driver amplifiers **126**A and **126**B may be collectively denoted "adjustment amplifiers".

[0075] In these embodiments, the adaptive control method adaptively controls the attenuations of the attenuators **122**A and **122**B, and the biasing voltages $Vbias_{1a}$ of the gain amplifier **124**A, $Vbias_{1b}$ of the gain amplifier **124**B, $Vbias_{2a}$ of the driver amplifier **126**A, and $Vbias_{2b}$ of the driver amplifier **124**B to adjust the power-division ratio r as described above. The adaptive control method also controls the reference bias currents $Iref_{main}$ and $Iref_{peaking}$ to set the $Vbias_{main}$ and $Vbias_{peak}$ so as to operate the main and peaking PAS **108** and **110** within their linear range.

[0076] In some embodiments, the phase shift introduced by the impedance inverter **112** may not fully match (that is, fully compensate for) the phase shift introduced by the splitter **102**. In these embodiments, the adaptive control method may also adaptively control the control circuits **106**A and/or **106**B for adjusting the phase shift between the input signals **208** and **210** of main and peaking amplifiers **108** and **110** for aligning the amplified first and second signals **214** and **216** to be in phase.

[0077] For example, in the example shown in FIG. **9**, the attenuators **122**A and **122**B generally have relatively constant phase shift within its attenuation range. To achieve a required input power-division ratio with suitable phase shift in the range between Pin_{main} and $Pin_{peaking}$, each of the attenuators **122**A and **122**B may be set to a desired attenuation setting (determined by a calibration procedure; described in more detail below) and the bias voltages of the gain amplifiers **124**A and **124**B and driver amplifiers **126**A and **126**B may be also set to a suitable value (determined by the calibration procedure; described in more detail below) to satisfy the relationship in Equations (3) and (4). The phase shift between the two branches **104**A and **104**B may then be fine-tuned while setting the constant power relative levels between Pin_{main} and $Pin_{peaking}$ (for example, by setting the power-division ratio r) to optimize the efficiency and linearity of the linear power-amplification module **100**. For phase array tapering, the output power of each path driving

an element or group of elements may not be constant. The relative output power of each path may be set through the same mechanism as above without adjusting the power supply voltage while the efficiency and linearity of the power-amplification module **100** is optimized at the same time.

[0078] In some embodiments, a calibration procedure may be used for determining the control parameters used by the adaptive control method.

[0079] The calibration procedure first determines a phase adjustment for compensating the possibly mismatched phase shifts introduced by the splitter **102** and the impedance inverter **112**. With reference to FIG. **10**, the power-division ratio r (that is, the power proportionality of the input powers of the main and peaking PAs **108** and **110**) and the biasing voltages $Vbias_{main}$ and $Vbias_{peak}$ of the main and peaking PAs **108** and **110** are set to fixed values, and the control circuits **106**A and/or **106**B are tuned to introduce a series of phase-adjustment values (such as from 0° to 85° in the example shown in FIG. **10**) between the input signals **208** and **210** of main and peaking amplifiers **108** and **110** (thus introducing the phase-adjustment values between the amplified signals **212** and **216**). For each phase-adjustment value, signals **102** of different powers are input to the linear power-amplification module **100**. The IMD and PAE are calculated based on the output signal **220**. A plurality of IMD curves **302** (each IMD curve having a plurality of IMD values with each IMD value corresponding to a target output power or a target input power) and a plurality of PAE curves **304** (each PAE curve having a plurality of PAE values with each PAE value corresponding to a target output power or a target input power) are then obtained with each IMD curve and each PAE curve corresponding to a specific phase-adjustment value, and each IMD curve corresponding to a PAE curve. As can be seen, the IMD curves **302** generally decrease with the increase of the output power Pout, and the PAE curves **304** generally increase with the increase of Pout.

[0080] The requirement of linearity of the linear power-amplification module **100** is satisfied when the IMD is greater than an IMD threshold, where the value of the IMD threshold depends on the application or use scenario. In the example shown in FIG. **10**, the requirement of linearity of the linear power-amplification module **100** is satisfied when the IMD is greater than an IMD threshold of 35 dB (represented by the dashed line **306**). Within a desired or required target Pout range, for example between 4.5 dBm and 12 dBm, some phase-adjustment values are eliminated because their IMD values are smaller than the IMD threshold. The PAE curves of the remaining phase-adjustment values are used to select a phase-adjustment value with the largest PAE value among the remaining PAE curves for each Pout value within the target Pout range. For example, for Pout=7 dBm, the phase-adjustment value of −35° gives rise to an IMD greater than 35 dBm and the largest PAE value, which improves the IMD from 26 dB to 35 dB and improves the PAE from 6.6% to 10.4% (about 36.5% power reduction at the same output power level).

[0081] FIG. **11** is a plot showing the simulation results with fixed $Pin_{peaking}$ and Pin_{main} power-division ratio r and biasing points for the main and peaking PAs **108** and **110** but with different phase alignments (phase shift) between the input signals of the main and peaking PAs **108** and **110**. As can be seen, the amplitude-to-phase (AM-PM) distortion is optimized while IMD is improved.

[0082] After the phase-adjustment values are determined, the calibration procedure then determines the values of the power-division ratio r (that is, the power proportionality of input powers of the main and peaking PAS **108** and **110**) for different output powers Pout (or for different input powers). As shown in FIG. **12**, the control circuits **106**A and/or **106**B introduce the determined phase-adjustment value, and are tuned to set a series of values of the power-division ratio r. For each power-division ratio r, signals **102** of different powers are input to the linear power-amplification module **100**. The IMD and PAE are calculated based on the output signal **220**. A plurality of IMD curves **302** and a plurality of PAE curves **304** are then obtained with each IMD curve and each PAE curve corresponding to a specific phase adjustment-value, and each IMD curve corresponding to a PAE curve. As can be seen, the IMD curves **302** generally decrease with the increase of the output power Pout, and the PAE curves **304** generally increase with the increase of Pout.

[0083] The requirement of linearity of the linear power-amplification module **100** is satisfied when the IMD is greater than an IMD threshold, where the value of the IMD threshold depends on the application or use scenario. In the example shown in FIG. **11**, the requirement of linearity of the linear power-amplification module **100** is satisfied when the IMD is greater than an IMD threshold of 35 dB (represented by the dashed line **306**). Within a target Pout range, for example between 4.5 dBm and 12 dBm, some r values are eliminated because their IMD values are smaller than the IMD threshold. For each Pout value within the target Pout range, the PAE curves of the remaining r values are used to select an r value with the largest PAE value among the remaining PAE curves, giving rise to an aggregated PAE curve **308**. For example, for Pout=4.75 dBm, r=0.9 gives rise to an IMD greater than 35 dBm and the largest PAE value which improves the PAE from 7.1% to 11.7% (about 4.7% PAE improvement at 6 dB reduction from peak operating power, which is about 40% power reduction at the same output power level).

[0084] The aggregated PAE curve **308** may be used by the adaptive control method for adaptively adjusting the power-division ratio during the operation of the linear power-amplification module **100**. For example, in some embodiments, a LUT may be obtained from the aggregated PAE curve **308** with a lookup column of different Pout values (or corresponding input power values) and a column of the corresponding r values. The adaptive control method may use the LUT to select a suitable r value based on the required output power (or based on the input power).

[0085] Those skilled in the art will appreciate that, in these embodiments, the adaptive control method uses the biasing to adjust the IMD and PAE curve. Consequently, the PBO for each curve is substantially the same. However, the P1dB is shifted to maintain the linearity (IMD) and efficiency (PAE).

[0086] In above embodiments, the calibration procedure separately determines the phase-adjustment values and the values of the power-division ratio r (that is, the power proportionality between the input powers of the main PA **108** and the peaking PA **110**).

[0087] When determining the phase-adjustment values, the calibration procedure introduces a series of phase-adjustment values between the circuit branches **104**A and **104**B while fixing the power proportionality and the biasing voltages of the main PA **108** and the peaking PA **110**. For

each of the series of phase-adjustment values, the calibration procedure inputs signals of different powers to the linear power-amplification module **100** and determines a set of IMD values and a set of PAE values for the phase-adjustment value, thereby obtaining a plurality of sets of IMD values (wherein each IMD value corresponds to a target output power or a target input power of the linear power-amplification module **100**; and each set of IMD values may be visually represented by an IMD curve as shown in FIG. **10**) and a plurality of sets of PAE values (wherein each PAE value corresponds to a target output power or a target input power of the linear power-amplification module **100**; and each set of PAE values may be visually represented by a PAE curve as shown in FIG. **10**).

[0088] The calibration procedure identifies one or more phase-adjustment values whose corresponding IMD values within a target power output or power input range are greater than an IMD threshold. Then, for each of a plurality of power output or power input values within the target power output or power input range, the calibration procedure selects, from the identified one or more phase-adjustment values that correspond to the power output or power input value, a phase-adjustment value with the greatest PAE value as the phase-adjustment value for that power output or power input value.

[0089] Similarly, when determining the values of the power-division ratio r (that is, the power-proportionality values), the calibration procedure introduces a series of power-proportionality values for the main PA **108** and the peaking PA **110**. For each of the series of power-proportionality values, the calibration procedure inputs signals of different powers to the linear power-amplification module **100** and determines a set of IMD values and a set of PAE values for the power-proportionality value, thereby obtaining a plurality of sets of IMD values (wherein each IMD value corresponds to a target output power or a target input power of the linear power-amplification module **100**; and each set of IMD values may be visually represented by an IMD curve as shown in FIG. **12** and a plurality of sets of PAE values (wherein each PAE value corresponds to a target output power or a target input power of the linear power-amplification module **100**; and each set of PAE values may be visually represented by a PAE curve as shown in FIG. **10**).

[0090] The calibration procedure identifies one or more power-proportionality values whose corresponding IMD values within a target power output or power input range are greater than an IMD threshold. Then, for each of a plurality of power output or power input values within the target power output or power input range, the calibration procedure selects, from the identified one or more power-proportionality values that correspond to the power output or power input value, a power-proportionality value with the greatest PAE value as the determined power-proportionality value for that power output or power input value.

[0091] In some embodiments, the calibration procedure may determine the phase-adjustment values and the power-proportionality values together.

[0092] In these embodiments, the calibration procedure introduces a plurality of combinations of the phase-adjustment values and the power-proportionality values to the linear power-amplification module **100**. For each combination of the phase-adjustment value and the power-proportionality value, the calibration procedure inputs signals of different powers to the linear power-amplification module **100** and determines a set of IMD values and a set of PAE values for the power-proportionality value, thereby obtaining a plurality of sets of IMD values (wherein each IMD value corresponds to a target output power or a target input power of the linear power-amplification module **100**; and each set of IMD values may be visually represented by an IMD curve as shown in FIG. **12** and a plurality of sets of PAE values (wherein each PAE value corresponds to a target output power or a target input power of the linear power-amplification module **100**; and each set of PAE values may be visually represented by a PAE curve as shown in FIG. **10**).

[0093] The calibration procedure identifies one or more combinations of the phase-adjustment values and the power-proportionality values whose corresponding IMD values within a target power output or power input range are greater than an IMD threshold. Then, for each of a plurality of power output or power input values within the target power output or power input range, the calibration procedure selects, from the identified one or more combinations of the phase-adjustment values and the power-proportionality values that correspond to the power output or power input value, a combination of the phase-adjustment value and the power-proportionality value with the greatest PAE value as the determined combination of the phase-adjustment value and the power-proportionality value for that power output or power input value.

[0094] In some embodiments, the calibration procedure does not determine the phase-adjustment values (thus, assume the phase shifts introduced by the splitter **102** and the impedance inverter **112** match, and any phase-shift mismatch may introduce IMD).

[0095] In above embodiments, the splitter **104** performs the 90° signal split. In some other embodiments, other suitable component or circuit may be used for the 90° signal split. Moreover, in various embodiments, the attenuators **122**A and **122**B may be any suitable attenuators such as analog-control attenuators, digital variable gain amplifiers (VGAs), analog VGAs, and/or the like to operate the main and peaking PAS **108** and **110** in their Class-AB region but with changing of the P1dB operating point.

[0096] As those skilled in the art will appreciate, the phase shift introduced by the splitter **102** is for compensating for the phase shift caused by the impedance transformer **112**. In some embodiments wherein the impedance transformer **112** causes a phase shift θ (not necessarily 90° and may be) 0° between the first and second split signals **204** and **206**, the splitter **102** may introduce an inverse phase shift −θ. In some embodiments, the splitter **102** may introduce the inverse phase shift −θ. Rather, a separate phase shifter may be included in the first control circuit **106**A and/or second control circuit **106**B to compensate for the phase shift caused by the impedance transformer **112**.

[0097] In some embodiments, the first and/or second control circuits **106**A and/or **106**B may not comprise any attenuators.

[0098] In some embodiments, the first control circuit **106**A may comprise a plurality of gain amplifiers **124**A, and the first control circuit **106**A may comprise a plurality of gain amplifiers **124**B depending on the overall gain requirement of the linear power-amplification module **100**. Each of the gain amplifiers **124**A and **124**B may comprise its dedi-

cated digital control for its bias voltage to facilitate the optimization of the power efficiency and linearity at the same time.

[0099] In some embodiments, the gain amplifier **124**A and the driver amplifier **126**A may be combined into a single amplifier. Similarly, the gain amplifier **124**B and the driver amplifier **126**B may be combined into a single amplifier.

[0100] In some embodiments, the linear power-amplification module **100** may not comprise any gain and/or driver amplifiers **124**A, **124**B, **126**A, and/or **126**B, and the adjustment of the power-division ratio is conducted by the attenuators **122**A and **122**B. However, the effectiveness of the linear power-amplification module **100** in these embodiments may be reduced.

[0101] In some embodiments wherein phase array tapering is used, the output power of each phase-array channel may not be constant. In these embodiments, the linear power-amplification module **100** may be used with changeable relative output power. That is, by controlling the bias voltages of the amplifiers **124**A, **124**B, **126**A, **126**B, **108**, and **110**, the output power may be adjusted without adjusting the input power of the linear power-amplification module **100** and thus without adjusting the power supply voltage for each channel of the phase array.

[0102] In above embodiments, the adaptive control method adjusts the bias voltage $Vbias_{main}$ of the main PA **108**, in some other embodiments, the adaptive control method may not adjust the bias voltage $Vbias_{main}$ of the main PA **108**.

[0103] In above embodiments, the splitter **102** splits the input signal to the first and second signals with substantially equal powers. In some embodiments, the first and second signals may have different powers.

[0104] In some of above embodiments, the adaptive control method is configured for adjusting the power-division ratio r in accordance with Equations (3) and (4). Those skilled in the art will appreciate that adjusting the power-division ratio r is equivalent to adjusting the power-division percentages of the input powers Pin_{main} and $Pin_{peaking}$ of the main and peaking PAs **108** and **110**, that is:

$$Pin_{main} = P1 + 10\log_{10}(x_{main}) \quad (7)$$

$$Pin_{peaking} = P1 + 10(x_{peaking}) \quad (8)$$

[0105] where x_{main} and $x_{peaking}$ are the power-division percentages of the input powers Pin_{main} and $Pin_{peaking}$, respectively, $1>x_{main}>0$, $1>x_{peaking}>0$, and $x_{main}+x_{peaking}=1$. In some embodiments, the power-division ratio $1>x_{main}\geq 0.5$.

[0106] In above embodiments, the linear power-amplification module **100** comprises two branches **104**A and **104**B. In some embodiments, the linear power-amplification module **100** may comprise more than two branches. One or more splitters may be used to provide split signals to the branches. Moreover, the adaptive control method is configured for adjusting the power-division percentages of the input powers of the PAs of the than two branches in accordance with:

$$Pin_i = P1 + 10\log_{10}(x_i) \quad (9)$$

[0107] where i=1, 2, ... N is the index of the PAs (where N is the total number of the PAs), Pin_i is the input power of the i-th PA, x_i is the power-division percentage of the input power of the i-th PA, $1\geq x_i\geq 0$, and $\Sigma_{i=1}^{N} x_i$.

[0108] While in above embodiments, each branch comprises a control circuit, in some embodiments, some branches may not comprise the control circuits.

[0109] In some embodiments, the linear power-amplification module **100** may not comprise any matching network **114**.

[0110] The linear power-amplification module **100** disclosed herein provides various benefits, such as:

[0111] both the main and peaking PAS **108** and **110** are operated in their linear Class-AB regions, and thus there is no need for matching of peaking and compression response at final response;

[0112] the adaptive biasing of both main and peaking PAS **108** and **110** improves the efficiency and linearity of the linear power-amplification module **100** at the same time, and thus the main PA **108** may be maintained at ideal load for required output power to ensure linearity and efficiency performance without dynamic load variation;

[0113] by using the simple LUT method to digitally control the attenuators **122**A and **122**B, the gain amplifiers **124**A and **124**B, and the driver amplifiers **126**A and **126**B to reconfigure the input power-division ratio and phase shift, the system complexity is reduced due to analog linearization with simple LUT digital-control instead of using complex DSP and/or DPD and changing drain biasing as in prior art;

[0114] the linear power-amplification module **100** disclosed herein is not frequency dependent and does not need complex high-speed DSP, DAC and DPD; and

[0115] the linear power-amplification module **100** disclosed herein may be used in embodiments using phase array tapering for changing the relative output power with improved efficiency while maintaining required linearity.

B. Acronym Key

[0116] Digital Predistortion: DPD
[0117] Digital Signal Processing: DSP
[0118] Doherty Power Amplifier: DPA
[0119] Intermodulation Distortion: IMD
[0120] "In-phase" and "Quadrature": I/Q
[0121] Look-Up Table: LUT
[0122] Millimeter Wave: mmWave
[0123] Peak-to-Average Power Ratio: PAPR
[0124] Power Added Efficiency: PAE
[0125] Power Amplifier: PA
[0126] Power Back-Off: PBO
[0127] Quadrature Amplitude Modulation: QAM
[0128] Variable Gain Amplifier: VGA

C. References

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[0132] Although embodiments have been described above with reference to the accompanying drawings, those of skill in the art will appreciate that variations and modifications may be made without departing from the scope thereof as defined by the appended claims.

1. A linear power-amplification circuit, comprising:

a splitter for splitting an input signal into a plurality split signals;

a plurality of circuit branches connected to the splitter, each circuit branch of the plurality of circuit branches for receiving a respective split signal of a plurality of split signals; and

an output connected to the plurality of circuit branches for combining outputs of the plurality of circuit branches and outputting an output signal;

wherein each circuit branch of the plurality of circuit branches comprises a respective class-AB power-amplifier (PA) operable under a biasing voltage; and

wherein one or more circuit branches of the plurality of circuit branches each comprise a respective control circuit connected to an input of the respective class-AB PA.

2. The linear power-amplification circuit of claim **1**, wherein each circuit branch of the plurality of circuit branches comprises the respective control circuit connected to the input of the respective class-AB PA.

3. The linear power-amplification circuit of claim **1**, wherein one or more control circuits of the one or more circuit branches are configured for adjusting input powers of respective class-AB PAS.

4. The linear power-amplification circuit of claim **3**, wherein the one or more control circuits of the one or more circuit branches are configured for adjusting the input powers of the respective class-AB PAs by adjusting power-division percentages of the input powers of the respective class-AB PAs in accordance with

$$\mathrm{Pin}_i = P1 + 10\log_{10}(x_i)$$

wherein P1 is a power proportional to a power of the input signal, i=1, 2, ... N and is an index of the respective class-AB PAs, N is a total number of the respective class-AB PAS, Pin_i is an input power of an i-th class-AB PA, x_i is a power-division percentage of the input power of the i-th class-AB PA, $1 \geq x_i \geq 0$, and $\Sigma_{i=1}^{N} x_i = 1$.

5. The linear power-amplification circuit of claim **1**, wherein one or more control circuits of the one or more circuit branches are configured for adjusting the biasing voltage of at least one class-AB PA of respective class-AB PAs.

6. The linear power-amplification circuit of claim **5**, wherein the one or more control circuits of the one or more circuit branches are configured for adjusting the biasing voltage of the at least one class-AB PA of the respective class-AB PAs by adjusting biasing current of the at least one class-AB PA.

7. The linear power-amplification circuit of claim **1**, wherein one or more control circuits of the one or more circuit branches are configured for applying phase adjustment between input signals of respective class-AB PAs of the one or more circuit branches.

8. The linear power-amplification circuit of claim **1**, wherein at least one control circuit of one or more control circuits of the one or more circuit branches comprises at least one of an attenuator or one or more adjustment amplifiers.

9. The linear power-amplification circuit of claim **8**, wherein the one or more control circuits of the one or more circuit branches are configured for adjusting input powers of respective class-AB PAs by adjusting at least one of an attenuation of the attenuator or biasing voltage of each of the one or more adjustment amplifiers.

10. The linear power-amplification circuit of claim **8**, wherein the one or more control circuits of the one or more circuit branches are configured for adjusting a phase shift between the input signals of respective class-AB PAs of the one or more circuit branches by adjusting biasing voltage of at least one of the one or more adjustment amplifiers.

11. The linear power-amplification circuit of claim **1**, further comprising:

two circuit branches each comprising the respective control circuit connected to an input of the respective class-AB PA.

12. The linear power-amplification circuit of claim **11**, wherein one or more control circuits of the one or more circuit branches are configured for adjusting input powers of class-AB PAs with a parameter r in accordance with

$$\mathrm{Pin}_{main} = P1 + 10\log_{10}(r)$$

$$\mathrm{Pin}_{peaking} = P1 + 10(1 - r)$$

wherein P1 is a power proportional to the power of the input signal, Pin_{main} and $\mathrm{Pin}_{peaking}$ are the input powers of two class-AB PAs, respectively, and $1 \geq r \geq 0$.

13. The linear power-amplification circuit of claim **12**, wherein $1 \geq r \geq 0.5$.

14. The linear power-amplification circuit of claim **12**, wherein two control circuits of the two circuit branches are configured for adjusting bias voltages of the two class-AB PAs, or for adjusting a biasing voltage of a peaking PA of the two class-AB PAs while maintaining a biasing voltage of a main PA of the two class-AB PAs constant.

15. The linear power-amplification circuit of claim **1**, wherein at least one circuit branch of the plurality of circuit branches comprises an impedance inverter coupled to an output of the respective class-AB PA.

16. The linear power-amplification circuit of claim **1**, wherein the plurality of circuit branches are connected to the output via a matching network.

17. A method, comprising:

introducing a plurality of sets of parameter values of one or more parameters to a linear power-amplification circuit;

for each set of the plurality of sets of parameter values, inputting signals of different powers to the linear power-amplification circuit and determining a set of intermodulation distortion (IMD) values and a set of power-added-efficiency (PAE) values for the each set, thereby obtaining a plurality of sets of IMD values and a plurality of sets of PAE values;

identifying one or more sets of parameter values whose corresponding IMD values within a target power output or power input range are greater than an IMD threshold; and

for each of a plurality of power output or power input values within the target power output or power input range, selecting, from the one or more set of parameter values, a set of parameter values with a greatest PAE value as a determined power-proportionality value for a power output or power input value of the plurality of power output or power input values.

18. The method of claim **17**, wherein the one or more parameters comprise at least one of phase-adjustment between circuit branches of the linear power-amplification circuit, or a power proportionality of class-AB PAs of the linear power-amplification circuit.

19. A non-transitory computer readable storage medium having stored thereon computer-executable instructions that, when executed by a computer, cause the computer to perform:

introducing a plurality of sets of parameter values of one or more parameters to a linear power-amplification circuit;

for each set of the plurality of sets of parameter values, inputting signals of different powers to the linear power-amplification circuit and determining a set of intermodulation distortion (IMD) values and a set of power-added-efficiency (PAE) values for the each set, thereby obtaining a plurality of sets of IMD values and a plurality of sets of PAE values;

identifying one or more sets of parameter values whose corresponding IMD values within a target power output or power input range are greater than an IMD threshold; and

for each of a plurality of power output or power input values within the target power output or power input range, selecting, from the one or more set of parameter values, a set of parameter values with a greatest PAE value as a determined power-proportionality value for a power output or power input value of the plurality of power output or power input values.

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