



(12) **United States Patent**
Huang et al.

(10) **Patent No.:** **US 12,396,186 B2**
(45) **Date of Patent:** **Aug. 19, 2025**

(54) **METHOD OF MAKING SEMICONDUCTOR
DEVICE INCLUDING METAL INSULATOR
METAL CAPACITOR**

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(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 0 days.

(21) Appl. No.: **18/522,752**

(22) Filed: **Nov. 29, 2023**

(65) **Prior Publication Data**

US 2024/0096929 A1 Mar. 21, 2024

Related U.S. Application Data

(60) Division of application No. 17/534,431, filed on Nov.
23, 2021, now Pat. No. 11,855,126, which is a
continuation of application No. 16/780,686, filed on
Feb. 3, 2020, now Pat. No. 11,201,206, which is a
(Continued)

(51) **Int. Cl.**
H10D 1/68 (2025.01)
H01L 23/522 (2006.01)
H10D 1/00 (2025.01)
H10B 41/30 (2023.01)

(Continued)

(52) **U.S. Cl.**

CPC **H10D 1/692** (2025.01); **H01L 23/5223**
(2013.01); **H10D 1/042** (2025.01); **H10D**
1/714 (2025.01); **H01L 23/5222** (2013.01);
H01L 2924/00 (2013.01); **H01L 2924/0002**
(2013.01); **H10B 41/30** (2023.02); **H10D 1/68**
(2025.01); **H10D 64/035** (2025.01); **H10D**
89/10 (2025.01)

(58) **Field of Classification Search**

CPC H01L 28/60; H01L 23/5223; H01L 28/87;
H01L 23/5222; H01L 27/0207; H01L
28/40; H01L 29/40114; H01L 2924/00;
H01L 2924/0002; H10B 41/30; H10D
1/692; H10D 1/042; H10D 1/714; H10D
1/68; H10D 64/035; H10D 89/10; H05K
5/13; A61K 40/31; H02K 15/0434
See application file for complete search history.

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Primary Examiner — Patricia D Valenzuela

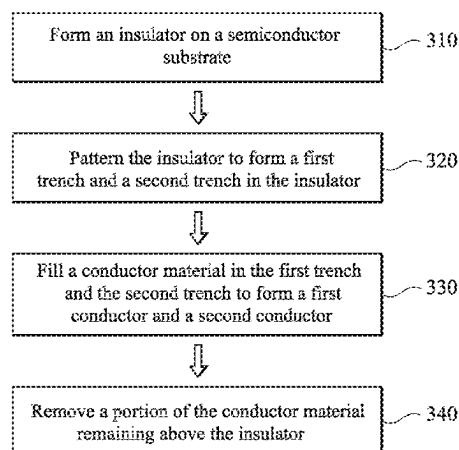
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(57) **ABSTRACT**

A method of making a semiconductor device includes form-
ing a circuit layer over a substrate. The method further
includes depositing an insulator over the substrate. The
method further includes patterning the insulator to define a
test line trench, a first trench, and a second trench, wherein
the first trench is on a portion of the substrate exposed by the
circuit layer. The method further includes filling the test line
trench to define a test line electrically connected to the
circuit layer. The method further includes filling the first
trench and the second trench to define a capacitor.

20 Claims, 14 Drawing Sheets

300



Related U.S. Application Data

division of application No. 14/103,651, filed on Dec.
11, 2013, now Pat. No. 10,553,672.

(51) **Int. Cl.**

H10D 64/01 (2025.01)
H10D 89/10 (2025.01)

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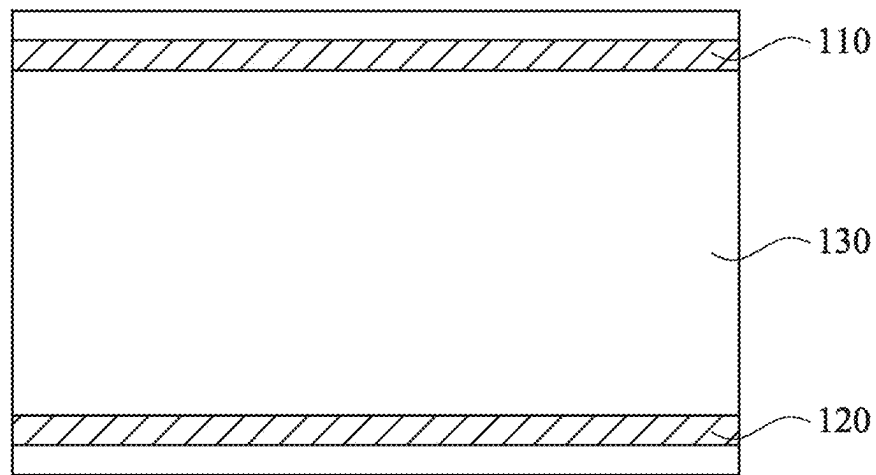
100

FIG. 1A

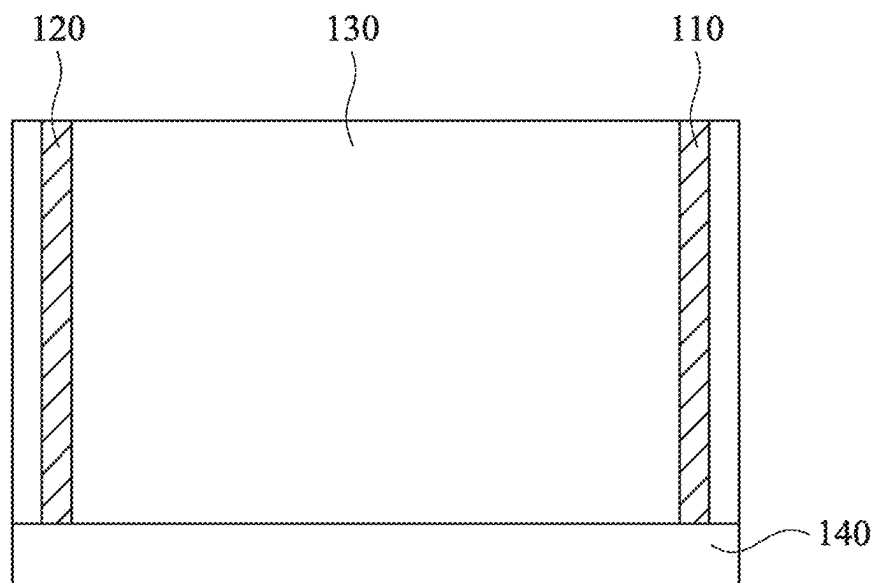
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FIG. 1B

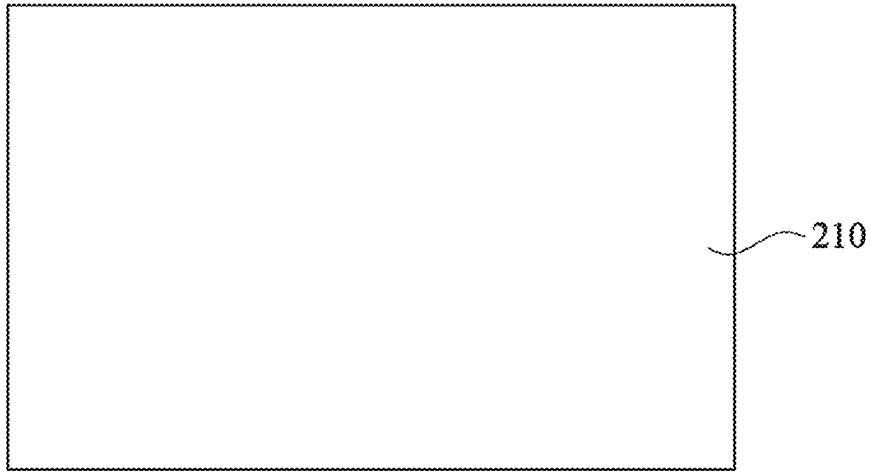


FIG. 2A

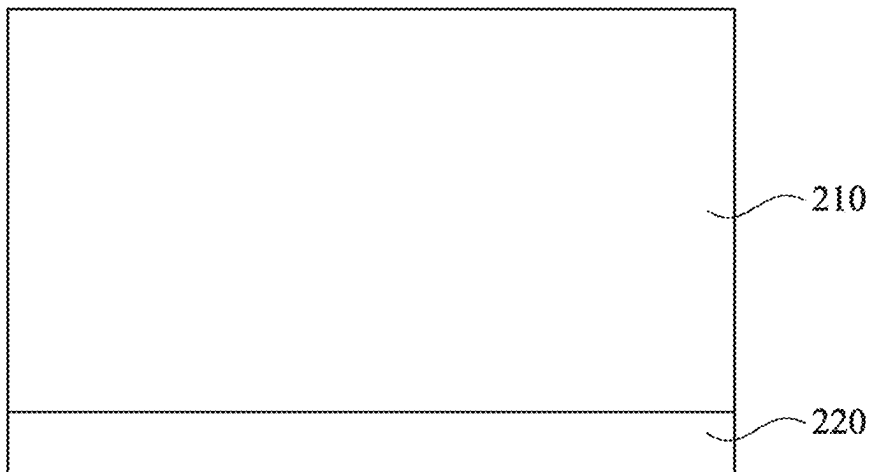


FIG. 2B

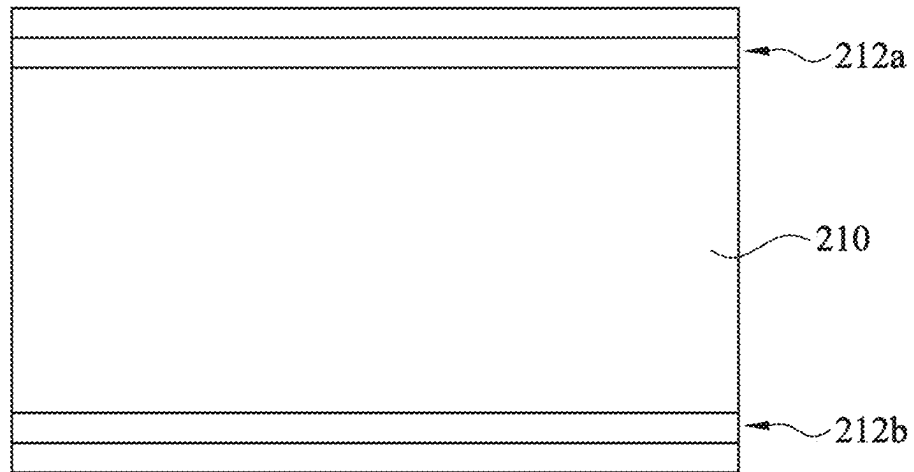


FIG. 2C

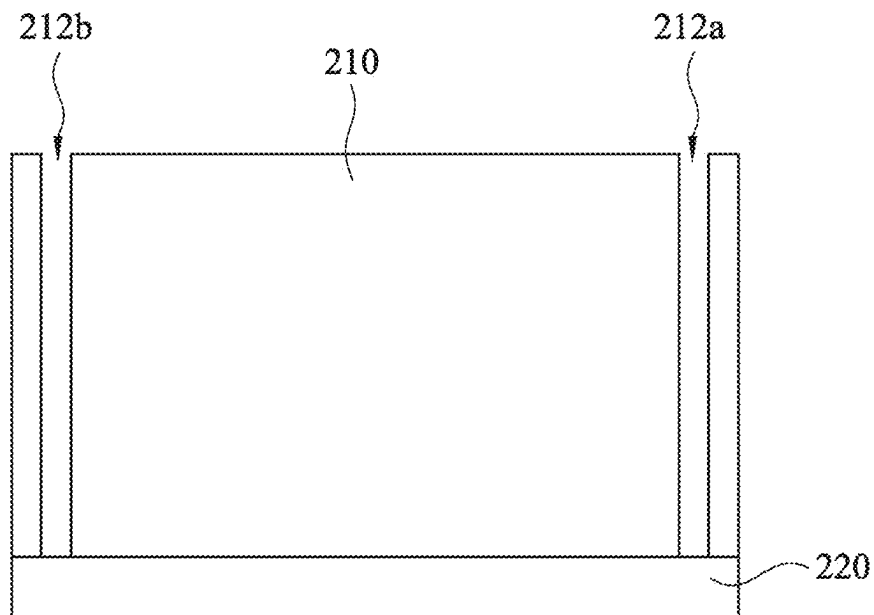


FIG. 2D

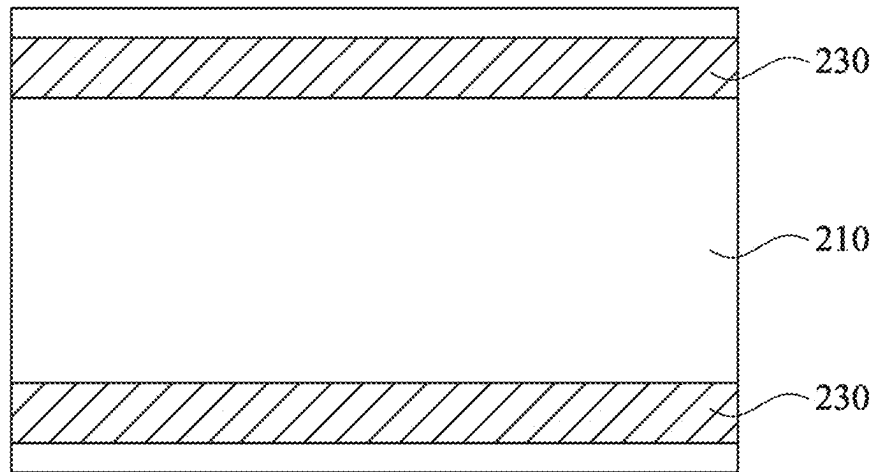


FIG. 2E

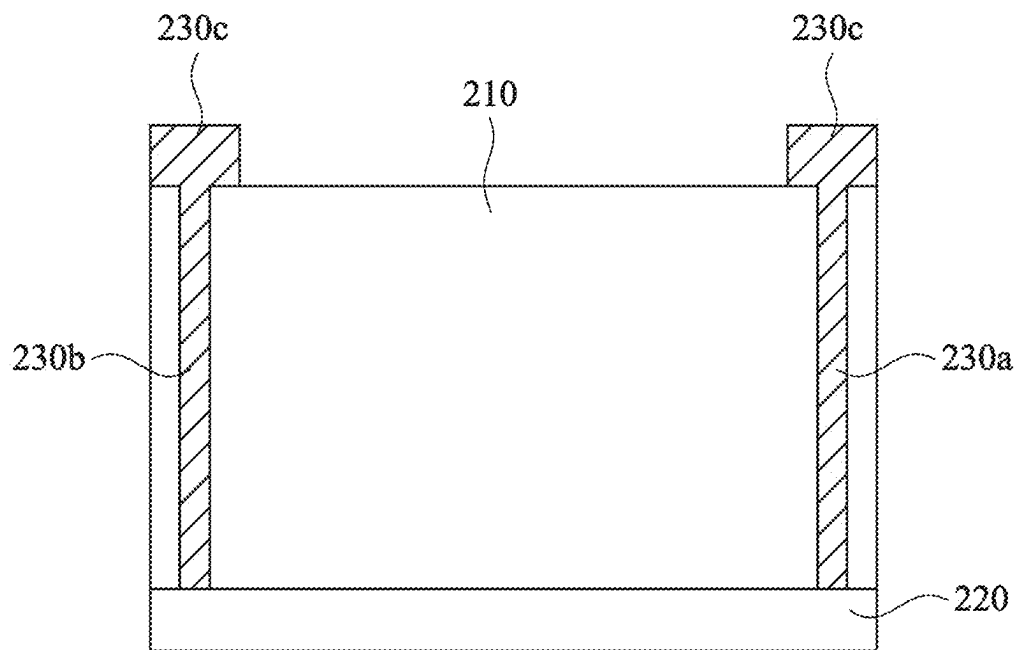


FIG. 2F

200

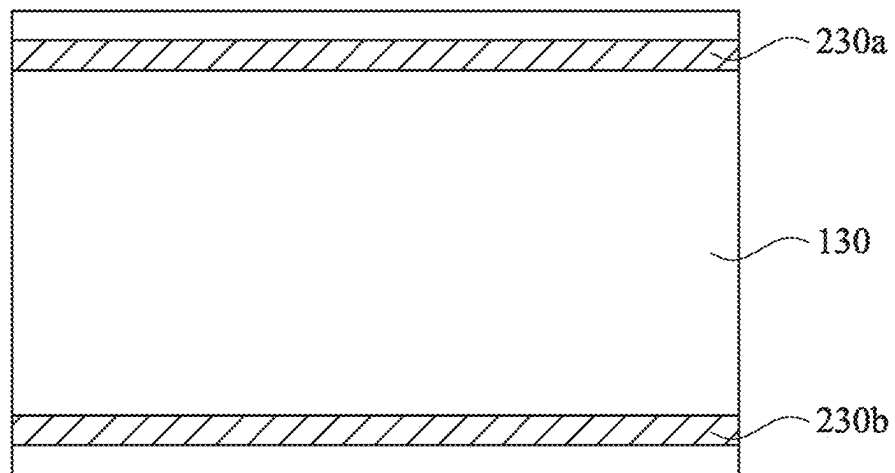


FIG. 2G

200

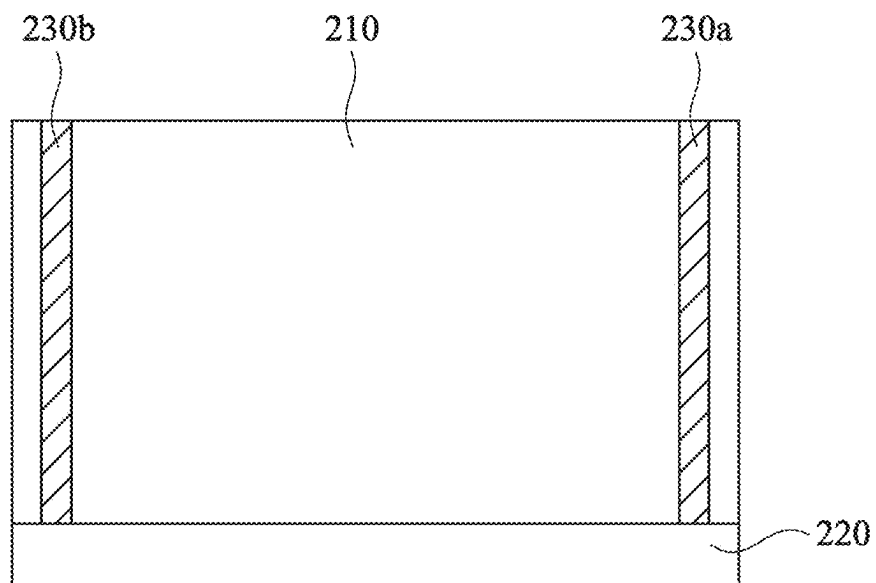


FIG. 2H

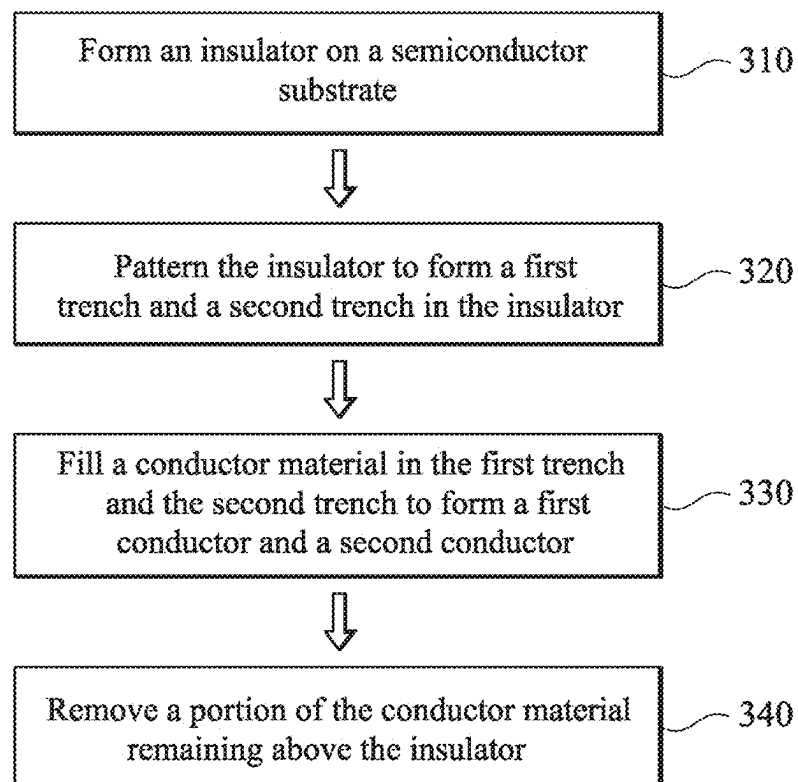
300

FIG. 3

400

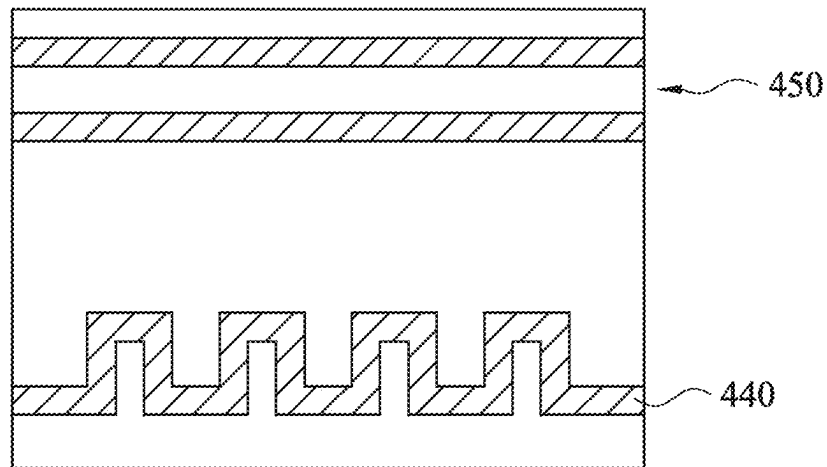


FIG. 4A

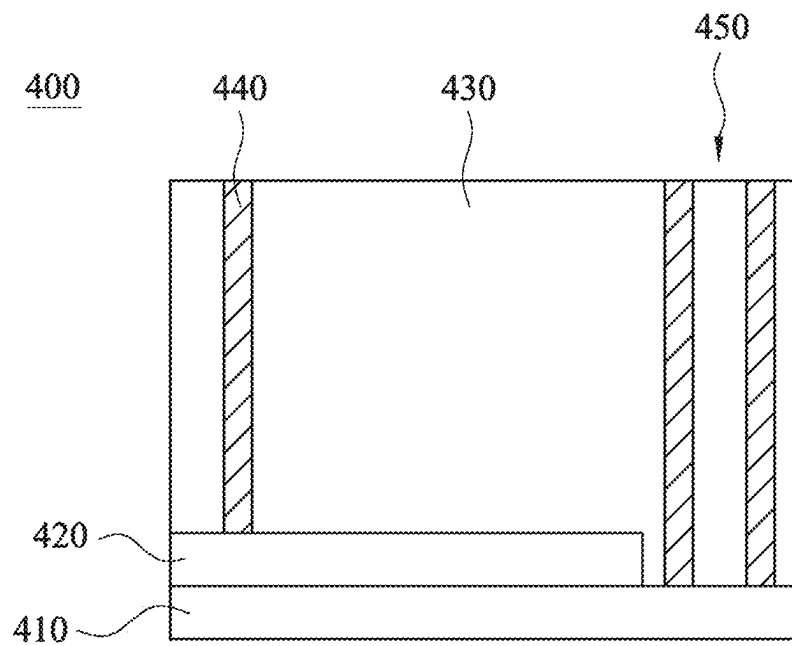


FIG. 4B

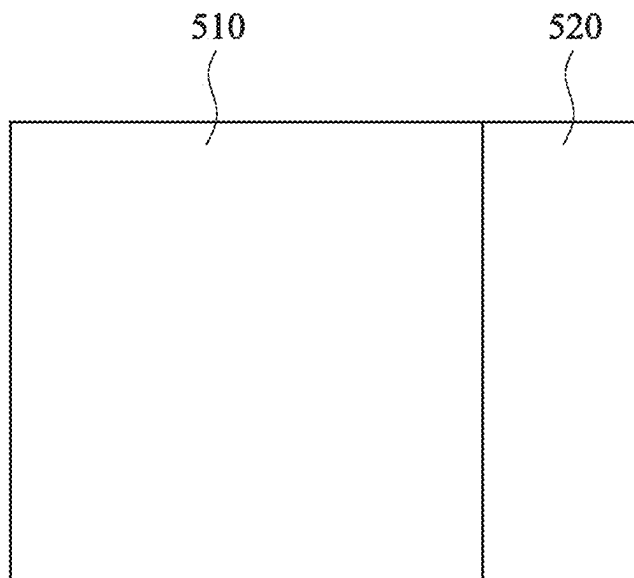


FIG. 5A

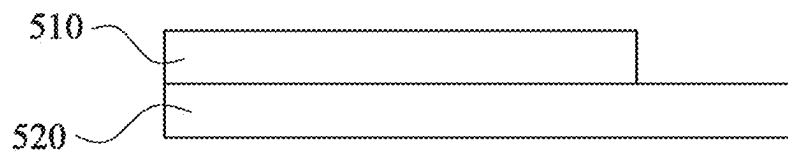


FIG. 5B

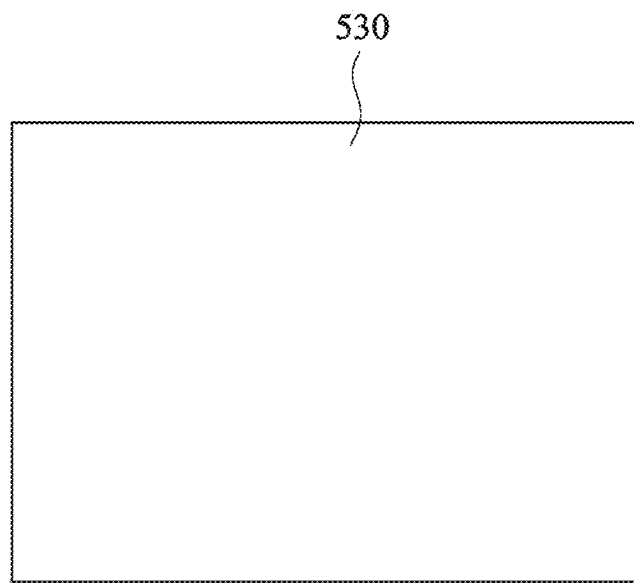


FIG. 5C

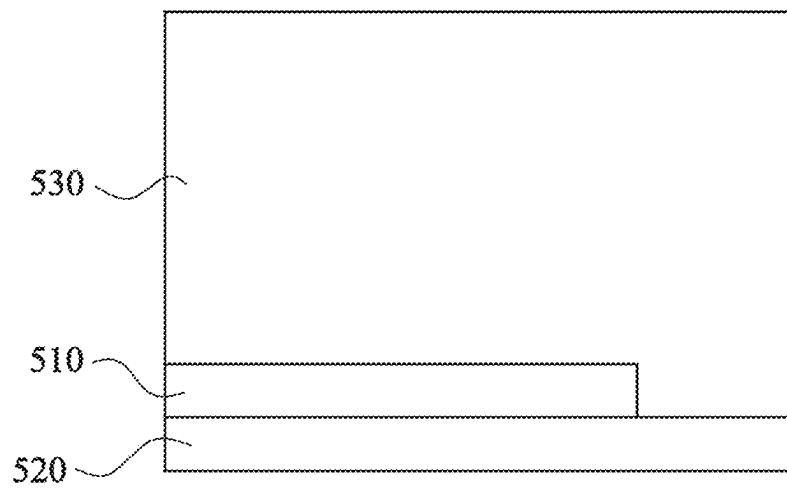


FIG. 5D

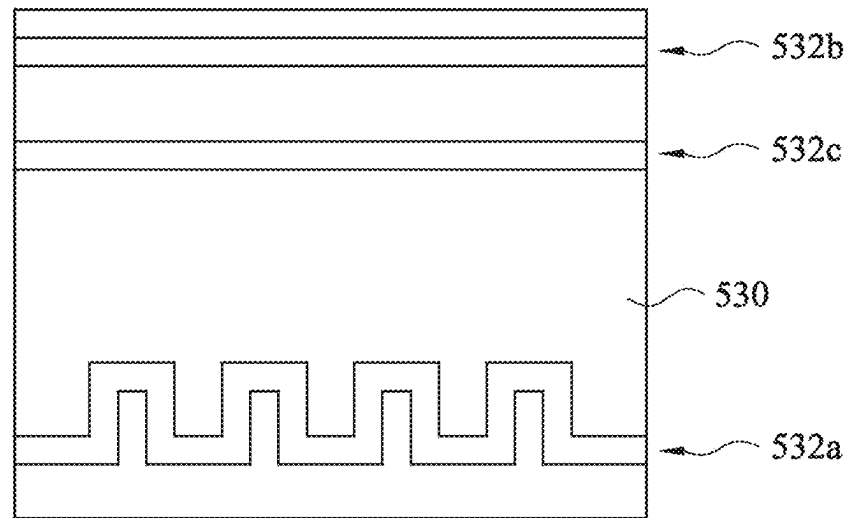


FIG. 5E

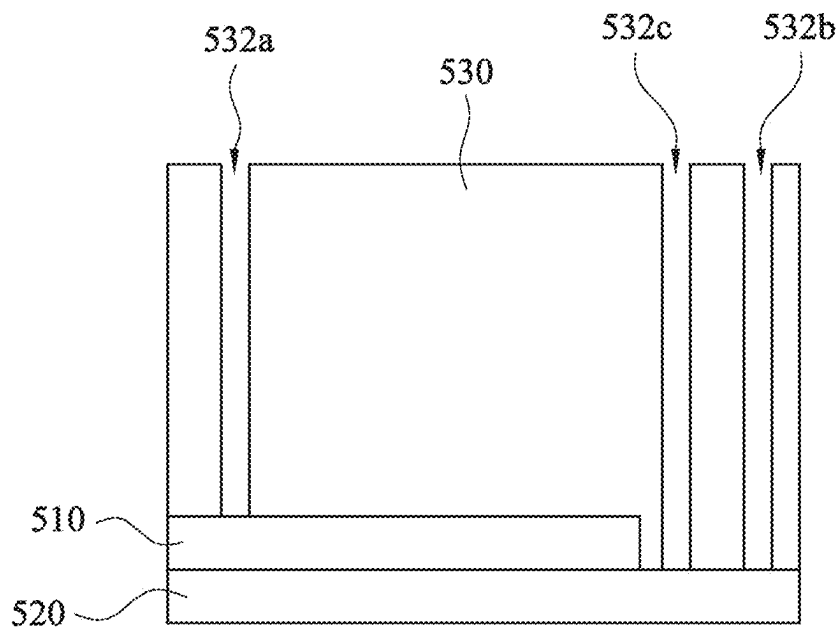


FIG. 5F

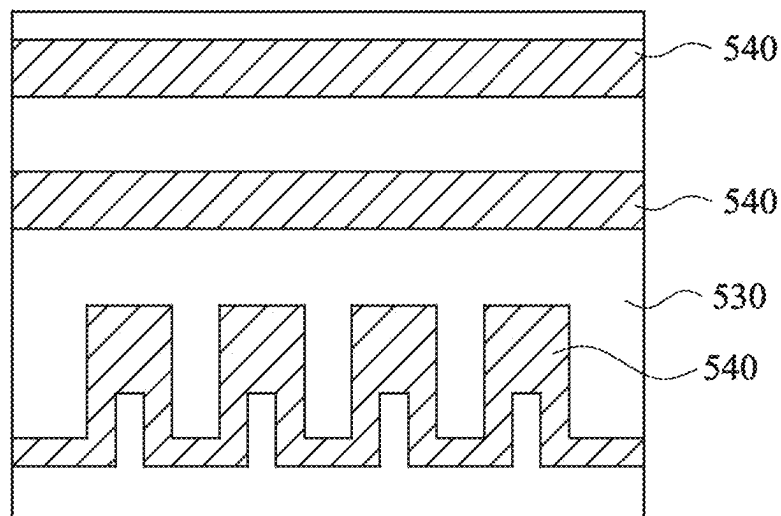


FIG. 5G

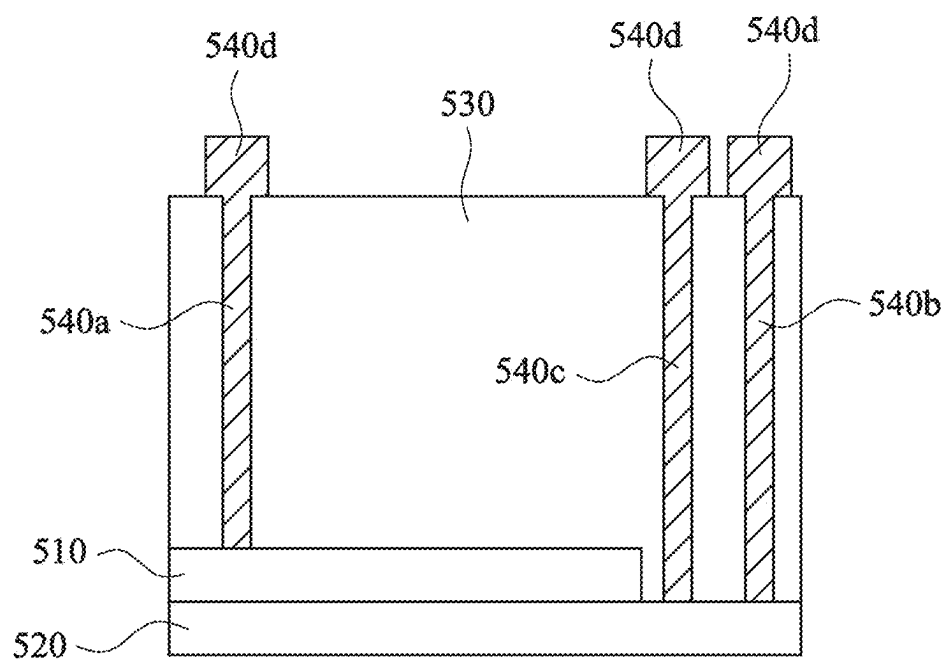


FIG. 5H

500

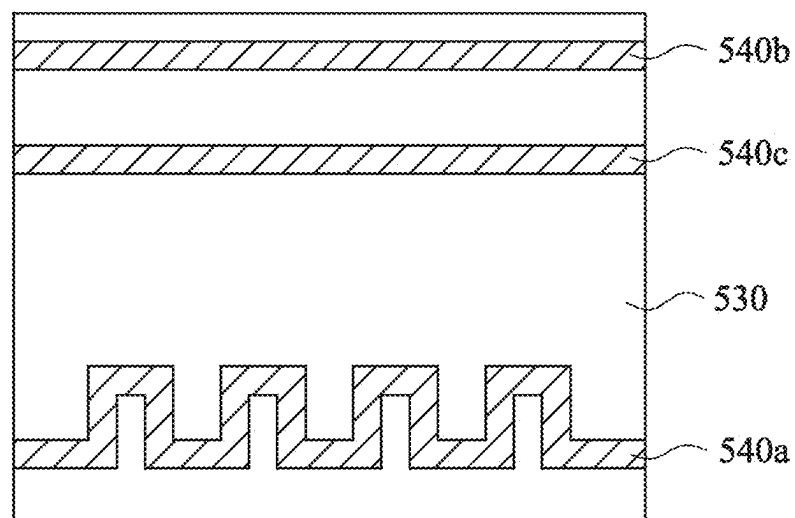


FIG. 5I

500

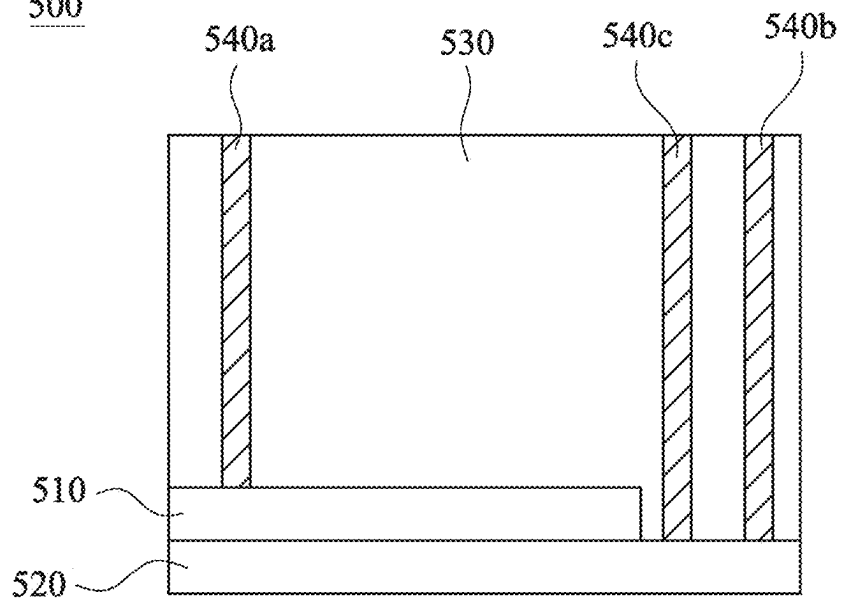


FIG. 5J

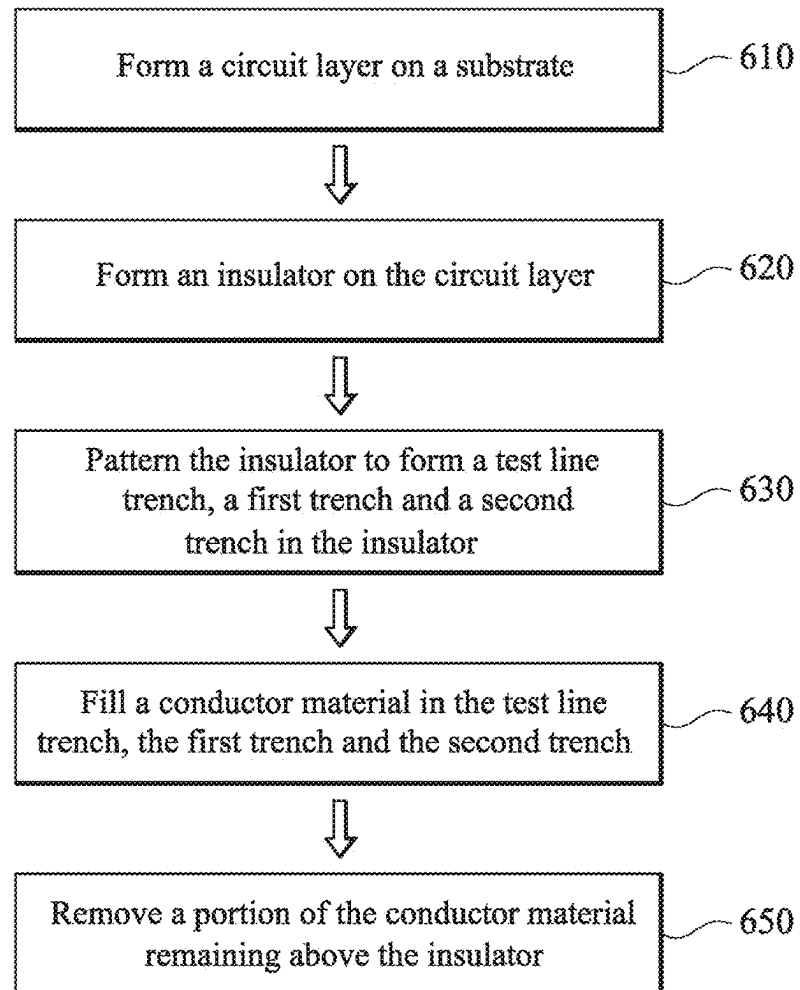


FIG. 6

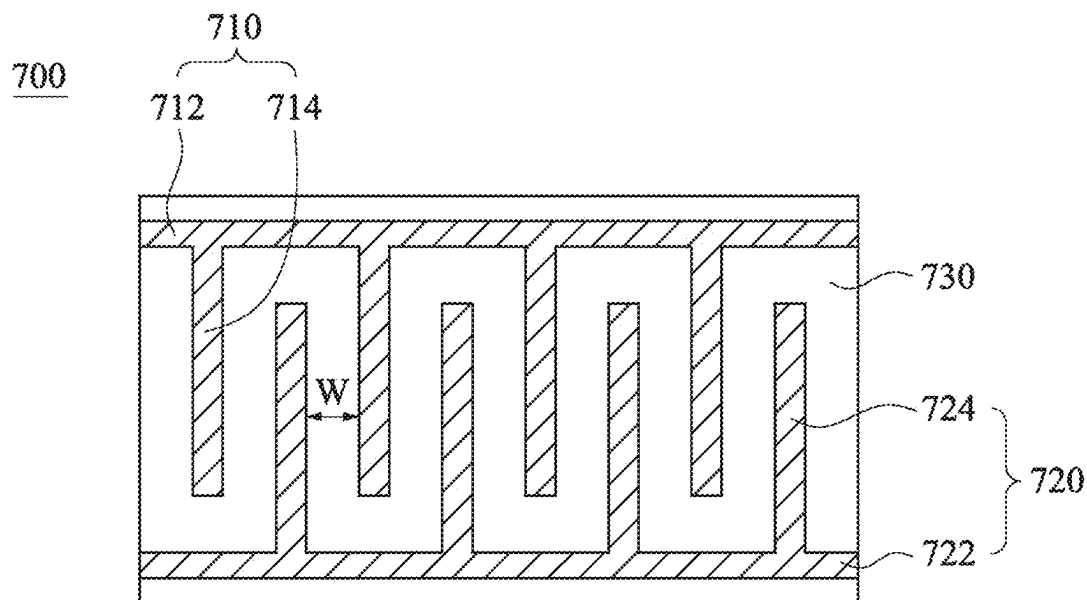


FIG. 7A

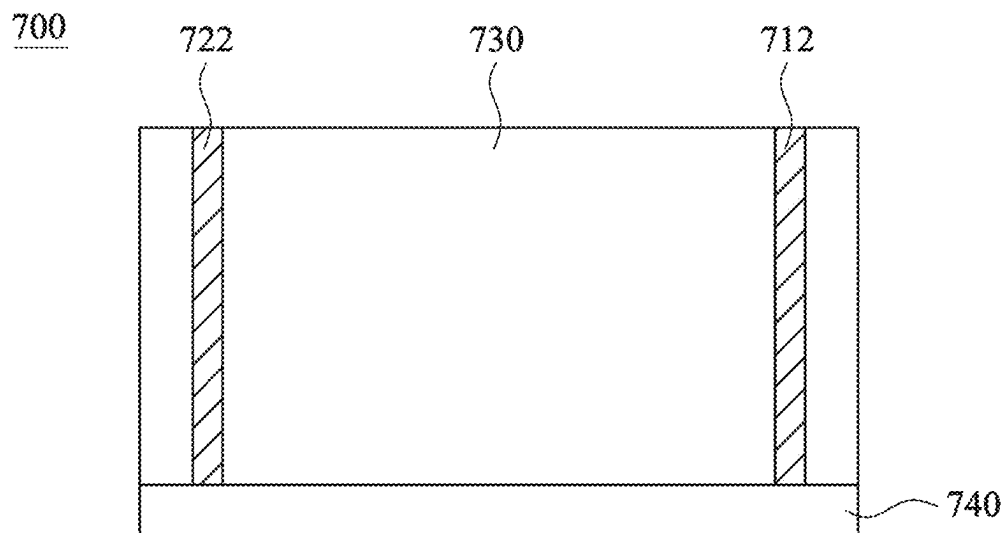


FIG. 7B

METHOD OF MAKING SEMICONDUCTOR DEVICE INCLUDING METAL INSULATOR METAL CAPACITOR

RELATED APPLICATION

This application is a divisional of U.S. application Ser. No. 17/534,431, filed Nov. 23, 2021, now U.S. Pat. No. 11,855,126, issued Dec. 26, 2023, which is a continuation of U.S. application Ser. No. 16/780,686, filed Feb. 3, 2020, now U.S. Pat. No. 11,201,206, issued Dec. 14, 2021, which is a divisional of U.S. application Ser. No. 14/103,651, filed Dec. 11, 2013, now U.S. Pat. No. 10,553,672, issued Feb. 4, 2020, the entire contents of which are hereby incorporated by reference.

BACKGROUND

Metal-insulator-metal (MIM) capacitors can be used in various integrated circuits such as analog frequency tuning circuits, switched capacitor circuits, filters, resonators, up-conversion and down-conversion mixers, and A/D converters. A conventional MIM capacitor includes a top metal layer, an insulator layer and a bottom metal layer, in which the top metal layer, the insulator layer and the bottom metal layer are vertically stacked on a semiconductor substrate and occupy quite a large surface area of the semiconductor substrate, and thus the capacitance of the conventional MIM capacitor is restricted by the limited area of the semiconductor substrate, and a device formed thereby will be constrained due to chip design rules. The conventional MIM capacitor requires many masks, and has a complicated manufacturing process.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention can be more fully understood by reading the following detailed description of the embodiment, with reference made to the accompanying drawings as follows:

FIG. 1A and FIG. 1B are respective schematic top and side views showing a MIM capacitor according to various embodiments;

FIG. 2A, FIG. 2C, FIG. 2E and FIG. 2G are schematic top views of intermediate stages according to a method for forming a MIM capacitor in some embodiments;

FIG. 2B, FIG. 2D, FIG. 2F and FIG. 2H are schematic cross-sectional views of intermediate stages according to the method for forming the MIM capacitor in some embodiments;

FIG. 3 is a flow chart of a method for fabricating a MIM capacitor in accordance with various embodiments;

FIG. 4A and FIG. 4B are respective schematic top and side views showing a semiconductor device according to various embodiments;

FIG. 5A, FIG. 5C, FIG. 5E, FIG. 5G and FIG. 5I are schematic top views of intermediate stages according to a method for forming a semiconductor device in some embodiments;

FIG. 5B, FIG. 5D, FIG. 5F, FIG. 5H and FIG. 5J are schematic cross-sectional views of intermediate stages according to the method for forming the semiconductor device in some embodiments;

FIG. 6 is a flow chart of a method for fabricating a MIM capacitor in accordance with various embodiments; and

FIG. 7A and FIG. 7B are respective schematic top and side views showing a MIM capacitor according to various embodiments.

DETAILED DESCRIPTION

The making and using of the present embodiments are discussed in detail below. It should be appreciated, however, that the present disclosure provides many applicable concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the disclosed subject matter, and do not limit the scope of the different embodiments. The present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

The terms used in this specification generally have their ordinary meanings in the art and in the specific context where each term is used. The use of examples in this specification, including examples of any terms discussed herein, is illustrative only, and in no way limits the scope and meaning of the disclosure or of any exemplified term. Likewise, the present disclosure is not limited to various embodiments given in this specific

It will be understood that, although the terms “first,” “second,” etc., may be used herein to describe various elements, these elements should not be limited by these terms. These terms are used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the embodiments. As used herein, the term “and/or” includes any and all combinations of one or more of the associated listed items.

As used herein, the terms “comprising,” “including,” “having,” “containing,” “involving,” and the like are to be understood to be open-ended, i.e., to mean including but not limited to.

Reference throughout the specification to “one embodiment” or “an embodiment” means that a particular feature, structure, implementation, or characteristic described in connection with the embodiment is included in at least one embodiment of the present disclosure. Thus, uses of the phrases “in one embodiment” or “in an embodiment” in various places throughout the specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, implementation, or characteristics may be combined in any suitable manner in one or more embodiments.

Embodiments of the present disclosure are directed to structures of Metal-insulator-metal (MIM) capacitors and methods for forming the MIM capacitors. In various embodiments, a MIM capacitor includes two conductors disposed upright on a semiconductor substrate and an insulator disposed between the conductors, and thus the method for forming the MIM capacitor is simplified and cost effective.

FIG. 1A and FIG. 1B are respective schematic top and side views showing a MIM capacitor 100 according to various embodiments. The MIM capacitor 100 includes a first conductor 110, a second conductor 120, an insulator 130, and a semiconductor substrate 140. The first conductor 110, the second conductor 120 and the insulator 130 are disposed vertically on the semiconductor substrate 140, and the insulator 130 is disposed between the first conductor 110 and the second conductor 120 to insulate the first conductor 110 from the second conductor 120. The first conductor 110 and the second conductor 120 are disposed upright on the semiconductor substrate 140 to be used as electrodes of the

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MIM capacitor **100**. Since the MIM capacitor **100** is vertically disposed on the semiconductor substrate **120**, the surface area occupied by the MIM capacitor **100** is relatively small. Thus, the capacitance of the conventional MIM capacitor **100** can be relatively large, and there is more space to design a device formed thereby.

The semiconductor substrate **140** is defined as any construction including semiconductor materials, including, but is not limited to, bulk silicon, a semiconductor wafer, a silicon-on-insulator (SOI) substrate, or a silicon germanium substrate. Other semiconductor materials including group III, group IV, and group V elements may also be used. The material of the first conductor **110** and the second conductor **120** includes, but is not limited to aluminum (Al), copper (Cu), silver (Ag), gold (Au), nickel (Ni), tungsten (W), or an alloy thereof. The material of the insulator **130** includes, but is not limited to aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), silicon carbide (SiC), silicon nitride, tantalum oxide (Ta_2O_5), tantalum oxynitride, titanium oxide, lead zirconate titanate (PZT), strontium bismuth tantalite (SBT), bismuth strontium tantalite (BST), strontium tantalite (ST), magnesium oxide, calcium oxide, hafnium silicon oxide, hafnium silicon oxynitride, zirconium oxide, yttrium oxide, strontium oxide, lanthanum oxide, barium oxide, or combinations thereof.

Referring to FIG. 2A-FIG. 2H, FIG. 2A, FIG. 2C, FIG. 2E and FIG. 2G are schematic top views of intermediate stages according to a method for forming a MIM capacitor in some embodiments, and FIG. 2B, FIG. 2D, FIG. 2F and FIG. 2H are schematic cross-sectional views of intermediate stages according to the method for forming the MIM capacitor in some embodiments.

As shown in FIG. 2A and FIG. 2B, an insulator **210** is formed on a semiconductor substrate **220**. The methods for forming the insulator **210** include, but not limit to a chemical vapor deposition (CVD) process and a physical vapor deposition (PVD) process. As shown in FIG. 2C and FIG. 2D, the insulator **210** is patterned to form a first trench **212a** and a second trench **212b** in the insulator **210**. In some embodiments, the first trench **212a** and the second trench **212b** are vertical to the substrate **220** and are parallel to each other. The method for patterning the insulator **210** includes a photolithographic process.

As shown in FIG. 2E and FIG. 2F, a conductor material **230** fills the first trench **212a** and the second trench **212b** to form a first conductor **230a** and a second conductor **230b** used as electrodes of a MIM capacitor. Since the first trench **212a** and the second trench **212b** are vertical to the substrate **220** and are parallel to each other, the first conductor **230a** and the second conductor **230b** therein are also vertical to the substrate **220** and are parallel to each other. The methods for filling the first trench **212a** and the second trench **212b** include, but not limited to a CVD process and a PVD process. In some embodiments, a portion **230c** of the conductor material **230** remains above a top of the insulator **210** after the operation for filling first trench **212a** and the second trench **212b** is performed. As shown in FIG. 2G and FIG. 2H, the portion **230c** of the conductor material **230** remaining above the top of the insulator **210** may be optionally removed, and a MIM capacitor **200** is formed accordingly. In some embodiments, the portion **230c** of the conductor material **230** may not be removed in the MIM capacitor. The method for removing the remaining portion **230c** includes, but not limited to a chemical mechanical polish (CMP) process.

Referring to FIG. 3 with FIG. 2A-FIG. 2H, FIG. 3 is a flow chart of a method **300** for fabricating a MIM capacitor

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in accordance with various embodiments. The method **300** begins at operation **310**, where an insulator **210** is formed on a semiconductor substrate **220**, as shown in FIG. 2A and FIG. 2B. At operation **320**, the insulator **210** is patterned to form a first trench **212a** and a second trench **212b** in the insulator **210**, as shown in FIG. 2C and FIG. 2D. At operation **330**, a conductor material **230** fills the first trench **212a** and the second trench **212b** to form a first conductor **230a** and a second conductor **230b**, as shown in FIG. 2E and FIG. 2F. In some embodiments, operation **340** may be optionally performed to remove a portion **230c** of the conductor material **230** remaining above the insulator **210**, as shown in FIG. 2G and FIG. 2H.

Comparing with the conventional method for fabricating a conventional MIM capacitor in which a top metal layer, an insulator layer and a bottom metal layer are vertically stacked on a semiconductor substrate, the method **300** needs fewer masks to fabricate the MIM capacitor **200**, and thus the method **300** is cost effective.

FIG. 4A and FIG. 4B are respective schematic top and side views showing a semiconductor device **400** according to various embodiments. The semiconductor device **400** includes a semiconductor substrate **410**, a circuit layer **420**, an insulator **430**, a test line **440** and a MIM capacitor **450**. The test line **440** can be disposed directly on the semiconductor substrate **410** to be electrically connected to the circuit layer **420**. In some embodiments, via structures can be used to electrically connect the test line **440** with the circuit layer **420**. The circuit layer **420** is horizontally disposed on the semiconductor substrate **410**. The circuit layer **420** includes a circuit device using the MIM capacitor **450**, such as a memory or other device. The MIM capacitor **450** is disposed on the substrate **410**. In some embodiments, The MIM capacitor **450** can be directly disposed on the circuit layer **420**.

Referring to FIG. 5A-FIG. 5H, FIG. 5A, FIG. 5C, FIG. 5E, FIG. 5G and FIG. 5I are schematic top views of intermediate stages according to a method for forming a semiconductor device **500** in some embodiments, and FIG. 5B, FIG. 5D, FIG. 5F, FIG. 5H and FIG. 5J are schematic cross-sectional views of intermediate stages according to the method for forming the semiconductor device **500** in some embodiments.

As shown in FIG. 5A and FIG. 5B, a circuit layer **510** is formed on a substrate **520**. The circuit layer **510** includes a circuit device using a MIM capacitor, such as a memory or other device. As shown in FIG. 5C and FIG. 5D, an insulator **530** is formed on the circuit layer **510**. As shown in FIG. 5E and FIG. 5F, the insulator **530** is patterned to form a test line trench **532a**, a first trench **532b** and a second trench **532c** in the insulator **530**. In some embodiments, the first trench **532b** and the second trench **532c** are vertical to the substrate **520** and are parallel to each other. The methods for patterning the insulator **530** include a photolithographic process, and thus a mask including a test line pattern and a capacitor pattern with a first trench pattern and a second trench pattern are used in the photolithographic process.

As shown in FIG. 5G and FIG. 5H, a conductor material **540** fills the test line trench **532a**, the first trench **532b** and the second trench **532c**, thereby forming a test line **540a**, a first conductor **540b** and a second conductor **540c**. The first conductor **540b** and the second conductor **540c** are used to be electrodes of a MIM capacitor. Since the first trench **532b** and the second trench **532c** are vertical to the substrate **520** and are parallel to each other, the first conductor **540b** and the second conductor **540c** therein are also vertical to the substrate **520** and are parallel to each other. In some embodi-

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ments, a portion **540d** of the conductor material **540** remains above a top of the insulator **530** after the operation for filling the test line trench **532a**, the first trench **532b** and the second trench **532c**. As shown in FIG. 5I and FIG. 5J, the portion **540d** of the conductor material **540** remaining above the insulator **530** is removed.

Referring to FIG. 6 with FIG. 5A-FIG. 5J, FIG. 6 is a flow chart of a method **600** for fabricating a MIM capacitor in accordance with various embodiments. The method **600** begins at operation **610**, where a circuit layer **510** is formed on a substrate **520**. At operation **620**, an insulator **530** is formed on the circuit layer **510**, as shown in FIG. 5C and FIG. 5G. At operation **630**, the insulator **530** is patterned to form a test line trench **532a**, a first trench **532b** and a second trench **532c** in the insulator **530**, as shown in FIG. 5E and FIG. 5F.

At operation **640**, a conductor material **540** fills the test line trench **532a**, the first trench **532b** and the second trench **532c**, thereby forming a test line **540a**, a first conductor **540b** and a second conductor **540c**, as shown in FIG. 5G and FIG. 5H. In some embodiments, a portion **540d** of the conductor material **540** remains above the insulator **530** after the operation for filling the test line trench **532a**, the first trench **532b** and the second trench **532c** is performed, and thus at operation **650**, the portion **540d** of the conductor material **540** remaining above the top of the insulator **530** is removed, as shown in FIG. 5I and FIG. 5J. In some embodiments, the portion **540d** of the conductor material **540** may not be removed in the MIM capacitor.

Comparing with the conventional method for fabricating a conventional MIM capacitor in which a top metal layer, an insulator layer and a bottom metal layer are vertically stacked on a semiconductor substrate, the method **600** integrates a process forming a MIM capacitor and a process forming a test line together. For example, in the operation **630**, patterns corresponding to the test line trench **532a**, the first trench **532b** and the second trench **532c** are formed one the same mask, thereby forming the test line trench **532a**, the first trench **532b** and the second trench **532c** in the insulator **530** simultaneously. For another example, in the operation **640**, the test line **540a**, the first conductor **540b** and the second conductor **540c** are formed in the same process (a CVD process, a PVD process, or the like), thereby forming the test line **540a**, the first conductor **540b** and the second conductor **540c** in the insulator **530** simultaneously. Therefore, the method **600** needs fewer masks to fabricate the MIM capacitor **500**, and thus the method **600** is cost effective.

FIG. 7A and FIG. 7B are respective schematic top and side views showing a MIM capacitor **700** according to various embodiments. The MIM capacitor **700** includes a first conductor **710**, a second conductor **720**, an insulator **730**, and a semiconductor substrate **740**. The first conductor **710**, the second conductor **720** and the insulator **730** are disposed vertically on the semiconductor substrate **740**, and the insulator **730** is disposed between the first conductor **710** and the second conductor **720** to insulate the first conductor **710** from the second conductor **720**. The first conductor **710** and the second conductor **720** are disposed upright on the semiconductor substrate **740** to be used as electrodes of the MIM capacitor **700**. The first conductor **710** includes a main portion **712** and branch portions **714**. Similarly, the second conductor **720** includes a main portion **722** and branch portions **724**. In some embodiments, the main portion **712** is vertical to the branch portions **714**, and the main portion **722** is vertical to the branch portions **724**.

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The main portion **712** of the first conductor **710** is parallel to the main portion **722** of the second conductor **720**, and the branch portions **714** of the first conductor **710** is parallel to the branch portions **724** of the second conductor **720**, in which a capacitance of the MIM capacitor **700** is determined in accordance with a width **W** between the branch portion **714** and the branch portion **724**.

In accordance with some embodiments, the present disclosure discloses a semiconductor device including a semiconductor substrate and a capacitor device disposed on the semiconductor substrate. The capacitor device includes a first conductor, a second conductor and an insulator. The first conductor and the second conductor are upright on the semiconductor substrate. The insulator is disposed between the first conductor and the second conductor on the semiconductor substrate for insulating the first conductor from the second conductor. The insulator has a first trench receiving the first conductor and a second trench receiving the second conductor.

In accordance with certain embodiments, the present disclosure disclosed a method for fabricating a semiconductor device. In this method, an insulator is formed on a semiconductor substrate. Then, at least two trenches are formed in the insulator. Thereafter, a conductor material fills the two trenches.

In accordance with certain embodiments, the present disclosure disclosed a method for fabricating a semiconductor device. In this method, a circuit layer is formed on a semiconductor substrate. Then, an insulator is formed on the circuit layer. Thereafter, a mask including a test line pattern and a capacitor pattern with a first trench pattern and a second trench pattern is provided. Then, a test line trench, a first trench and a second trench are formed in the insulator by using the mask. Thereafter, a conductor material fills the test line trench, the first trench and the second trench to form a test line conductor, a first conductor and a second conductor electrically connected to the circuit layer respectively.

Although the present invention has been described in considerable detail with reference to certain embodiments thereof, other embodiments are possible. Therefore, the spirit and scope of the appended claims should not be limited to the description of the embodiments contained herein.

An aspect of this description relates to a method of making a semiconductor device. The method includes forming a circuit layer over a substrate. The method further includes depositing an insulator over the substrate. The method further includes patterning the insulator to define a test line trench, a first trench, and a second trench, wherein the first trench is on a portion of the substrate exposed by the circuit layer. The method further includes filling the test line trench to define a test line electrically connected to the circuit layer. The method further includes filling the first trench and the second trench to define a capacitor. In some embodiments, filling the test line trench includes filling the test line trench simultaneously with filling the first trench. In some embodiments, the method further includes electrically connecting the circuit layer to the capacitor. In some embodiments, filling the test line trench includes defining the test line in direct connection with the circuit layer.

An aspect to this description relates to a method of making a semiconductor device. The method includes forming a circuit layer over a first portion of a substrate, wherein the circuit layer exposes a second portion of the substrate. The method further includes forming a test line electrically connected to the circuit layer. The method further includes forming a capacitor entirely over the second portion of the

substrate. In some embodiments, forming the test line includes depositing an insulator over the substrate; patterning the insulator to define a first opening; and filling the first opening with a first conductive material. In some embodiments, forming the capacitor includes patterning the insulator to define a second opening and a third opening; and filling the second opening and the third opening with a second conductive material. In some embodiments, filling the second opening and the third opening is performed simultaneously with filling the first opening. In some embodiments, patterning the insulator to define the second opening and the third opening is performed simultaneously with patterning the insulator to define the first opening. In some embodiments, forming the capacitor further includes removing the second conductive material from a top surface of the insulator. In some embodiments, forming the capacitor further includes patterning the insulator to define a plurality of fourth openings extending perpendicular to the second opening; and patterning the insulator to define a plurality of fifth openings extending perpendicular to the third opening. In some embodiments, patterning the insulator includes defining one of the plurality of fifth openings between adjacent fourth openings of the plurality of fourth openings. In some embodiments, forming the capacitor further includes filling the plurality of fourth openings and the plurality of fifth openings with the second conductive material. In some embodiments, forming the test line includes forming the test line having a serpentine shape.

An aspect of this description relates to a method of making a semiconductor device. The method includes forming a circuit layer over a substrate. The method further includes depositing an insulator over the substrate. The method further includes patterning the insulator to define a test line trench, a first trench, and a second trench, wherein the test line trench has a first depth, each of the first trench and the second trench have a second depth, and the second depth is greater than the first depth. The method further includes filling the test line trench to define a test line electrically connected to the circuit layer. The method further includes filling the first trench and the second trench to define a capacitor. In some embodiments, patterning the insulator includes defining the first trench and the second trench over a portion of the substrate exposed by the circuit layer. In some embodiments, patterning the insulator includes defining the test line trench having a serpentine shape. In some embodiments, filling the test line trench and filling the first trench and second trench includes depositing a conductive material. In some embodiments, patterning the insulator includes defining a plurality of third trenches connected to the first trench, wherein each of the plurality of third trenches extends perpendicular to the first trench; and defining a fourth trench connected to the second trench, wherein the fourth trench extends perpendicular to the second trench. In some embodiments, defining the fourth trench includes defining the fourth trench between adjacent third trenches of the plurality of third trenches.

It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims.

What is claimed is:

1. A method of making a semiconductor device, the method comprising:
forming a circuit layer over a substrate;

depositing an insulator over the substrate;
patterning the insulator to define a test line trench, a first trench, and a second trench, wherein the first trench exposes a portion of the substrate exposed by the circuit layer;
filling the test line trench to define a test line electrically connected to the circuit layer; and
filling the first trench and the second trench to define a capacitor.

2. The method of claim 1, wherein filling the test line trench comprises filling the test line trench simultaneously with filling the first trench.

3. The method of claim 1, further comprising electrically connecting the circuit layer to the capacitor.

4. The method of claim 1, wherein filling the test line trench comprises defining the test line in direct connection with the circuit layer.

5. A method of making a semiconductor device, the method comprising:

forming a circuit layer over a first portion of a substrate, wherein the circuit layer exposes a second portion of the substrate;

forming a test line electrically connected to the circuit layer; and

forming a capacitor entirely over the second portion of the substrate.

6. The method of claim 5, wherein forming the test line comprises:

depositing an insulator over the substrate;

patterning the insulator to define a first opening; and
filling the first opening with a first conductive material.

7. The method of claim 6, wherein forming the capacitor comprises:

patterning the insulator to define a second opening and a third opening; and

filling the second opening and the third opening with a second conductive material.

8. The method of claim 7, wherein filling the second opening and the third opening is performed simultaneously with filling the first opening.

9. The method of claim 7, wherein patterning the insulator to define the second opening and the third opening is performed simultaneously with patterning the insulator to define the first opening.

10. The method of claim 7, wherein forming the capacitor further comprises removing the second conductive material from a top surface of the insulator.

11. The method of claim 7, wherein forming the capacitor further comprises:

patterning the insulator to define a plurality of fourth openings extending perpendicular to the second opening; and

patterning the insulator to define a plurality of fifth openings extending perpendicular to the third opening.

12. The method of claim 11, wherein patterning the insulator comprises defining one of the plurality of fifth openings between adjacent fourth openings of the plurality of fourth openings.

13. The method of claim 11, wherein forming the capacitor further comprises filling the plurality of fourth openings and the plurality of fifth openings with the second conductive material.

14. The method of claim 5, wherein forming the test line comprises forming the test line having a serpentine shape.

15. A method of making a semiconductor device, the method comprising:
forming a circuit layer over a substrate;

depositing an insulator over the substrate;
patterning the insulator to define a test line trench, a first
trench, and a second trench, wherein the test line trench
has a first depth, each of the first trench and the second
trench have a second depth, and the second depth is 5
greater than the first depth;
filling the test line trench to define a test line electrically
connected to the circuit layer; and
filling the first trench and the second trench to define a
capacitor. 10

16. The method of claim **15**, wherein patterning the
insulator comprises defining the first trench and the second
trench over a portion of the substrate exposed by the circuit
layer.

17. The method of claim **15**, wherein patterning the 15
insulator comprises defining the test line trench having a
serpentine shape.

18. The method of claim **15**, wherein filling the test line
trench and filling the first trench and second trench com-
prises depositing a conductive material. 20

19. The method of claim **15**, wherein patterning the
insulator comprises:
defining a plurality of third trenches connected to the first
trench, wherein each of the plurality of third trenches
extends perpendicular to the first trench; and 25
defining a fourth trench connected to the second trench,
wherein the fourth trench extends perpendicular to the
second trench.

20. The method of claim **19**, wherein defining the fourth
trench comprises defining the fourth trench between adja- 30
cent third trenches of the plurality of third trenches.

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