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BUCK-BOOST DC-DC CONVERTER CIRCUIT AND CORRESPONDING METHOD OF OPERATION

Abstract

A buck-boost converter circuit includes a mode selection circuit that asserts a buck enable signal if an input voltage is higher than a lower threshold, and asserts a boost enable signal if the input voltage is lower than an upper threshold. A control circuit asserts a buck PWM signal upon a pulse in a buck clock and de-asserts the buck PWM signal if a buck ramp is higher than a buck control signal, and it keeps the buck PWM signal asserted if the buck enable signal is de-asserted. The control circuit asserts a boost PWM signal upon a pulse in a boost clock and de-asserts the boost PWM signal if a boost ramp is higher than a boost control signal, and it keeps the boost PWM signal de-asserted if the boost enable signal is de-asserted.

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATIONS [0001] This application is a continuation of U.S. application Ser. No. 18/297,998, filed on Apr. 10, 2023, which claims priority to Italian Patent Application No. 102022000008108, filed on Apr. 22, 2022, which application is hereby incorporated by reference herein in its entirety.

TECHNICAL FIELD

[0002] The present disclosure relates to buck-boost DC-DC switching converters (e.g., non-inverting converters).

BACKGROUND

[0003] Voltage converters are conventionally used in power management systems to convert a DC input voltage V.sub.in into a DC output voltage V.sub.out. Various topologies of switching mode power supply (SMPS) can be adopted to achieve high conversion efficiency. Buck converters provide a step-down conversion of the input voltage (i.e., V.sub.out<V.sub.in), and boost converters provide a step-up conversion (i.e., V.sub.out>V.sub.in). Non-inverting buck-boost converters are adopted when the output voltage V.sub.out can be higher or lower than the input voltage V.sub.in, thus enabling both step-up and step-down voltage conversion.

SUMMARY

[0004] In one or more embodiments the present disclosure provides buck-boost DC-DC converters with improved efficiency and lower complexity.

[0005] One or more embodiments may relate to a corresponding method of operating a buck-boost DC-DC converter.

[0006] In one or more embodiments, a buck-boost DC-DC converter circuit includes a switching stage configured to receive a converter input voltage, a buck pulse-width modulated control signal and a boost pulse-width modulated control signal, and produce a converter output voltage as a function thereof. The converter includes an error amplifier circuit configured to sense the converter output voltage and a reference voltage, and produce an error signal indicative of a difference between the reference voltage and the converter output voltage. The converter includes an operation mode selection circuit configured to compare the converter input voltage to a lower threshold and an upper threshold.

[0007] The operation mode selection circuit is configured to assert a buck mode enable signal in response to the converter input voltage being higher than the lower threshold, and de-assert the buck mode enable signal in response to the converter input voltage being lower than the lower threshold. The operation mode selection circuit is configured to assert a boost mode enable signal in response to the converter input voltage being lower than the upper threshold, and de-assert the boost mode enable signal in response to the converter input voltage being higher than the upper threshold.

[0008] The converter includes a voltage shifter circuit configured to produce a buck control signal and a boost control signal as a function of the error signal, the buck mode enable signal, and the boost mode enable signal. The converter includes a ramp generator circuit configured to produce a buck ramp signal as a function of a buck clock signal and produce a boost ramp signal as a function of a boost clock signal. The converter includes a control circuit configured to compare the buck control signal to the buck ramp signal.

[0009] The control circuit is configured to assert the buck pulse-width modulated control signal in response to a pulse in the buck clock signal and de-assert the buck pulse-width modulated control signal in response to the buck ramp signal being higher than the buck control signal, provided that the buck mode enable signal is asserted. The control circuit is configured to keep the buck pulse-width modulated control signal asserted, provided that the buck mode enable signal is de-asserted. The control circuit is configured to compare the boost control signal to the boost ramp signal.

[0010] The control circuit is configured to assert the boost pulse-width modulated control signal in response to a pulse in the boost clock signal and de-assert the boost pulse-width modulated control signal in response to the boost ramp signal being higher than the boost control signal, provided that the boost mode enable signal is asserted. The control circuit is configured to keep the boost pulse-width modulated control signal de-asserted, provided that the boost mode enable signal is de-asserted. The voltage shifter circuit is configured to set V.sub.C,buck=V.sub.EA, where V.sub.C,buck is the value of the buck control signal and V.sub.EA is the value of the error signal, in response to the buck mode enable signal being asserted and the boost mode enable signal being de-asserted. The voltage shifter circuit is configured to set V.sub.C,boost=(V.sub.EA−V.sub.FF), where V.sub.C,boost is the value of the boost control signal, V.sub.EA is the value of the error signal, and V.sub.FF is the value of a feedforward voltage of the buck-boost DC-DC converter circuit, in response to the buck mode enable signal being de-asserted and the boost mode enable signal being asserted. The voltage shifter circuit is configured to set V.sub.C,buck=(V.sub.EA−k2.Math.V.sub.ref1) and V.sub.C,boost=(V.sub.EA−(k1+k2)−V.sub.ref1), where V.sub.C,buck is the value of the buck control signal, V.sub.EA is the value of the error signal, V.sub.ref1 is the value of the reference voltage, V.sub.C,boost is the value of the boost control signal, and k1 and k2 are values

(e.g., constant values) that satisfy the conditions k1+2.Math.k2=1 and 0<k1<1, in response to the buck mode enable signal being asserted and the boost mode enable signal being asserted.
[0011] One or more embodiments may thus provide a buck-boost DC-DC converter that automatically switches between buck, boost, and buck-boost operation modes with improved efficiency and low complexity.
[0012] In one or more embodiments, the voltage shifter circuit includes a voltage divider circuit including a first node, a second node, a third node, a fourth node, a first resistor coupled between the first node and the second node, a second resistor coupled between the second node and the third node, and a third resistor coupled between the third node and the fourth node. The first node is configured to produce the boost control signal, the second node is configured to produce the buck control signal, and the fourth node is configured to receive the error signal. The voltage shifter circuit includes a first current generator circuit configured to supply to the voltage divider circuit a current proportional to the feedforward voltage. The voltage shifter circuit includes a second current generator circuit configured to supply to the voltage divider circuit a current proportional to the reference voltage. The voltage shifter circuit includes a plurality of switches controllable by the buck mode enable signal and the boost mode enable signal. The plurality of switches are arranged to couple the voltage divider circuit to the first current generator circuit to receive the current proportional to the feedforward voltage in response to the buck mode enable signal being de-asserted; couple the voltage divider circuit to the second current generator circuit to receive the current proportional to the reference voltage in response to the buck mode enable signal being asserted; bypass the second resistor in response to the boost mode enable signal being de-asserted; and bypass the third resistor in response to the buck mode enable signal being asserted.
[0013] In one or more embodiments, the voltage shifter circuit includes a first voltage-to-current converter arrangement configured to sense the feedforward voltage and control the first current generator circuit, and a second voltage-to-current converter arrangement configured to sense the reference voltage and control the second current generator circuit.
[0014] In one or more embodiments, the ratio between the current produced by the first current generator circuit and the feedforward voltage is equal to 1/R, the ratio between the current produced by the second current generator circuit and the reference voltage is equal to 1/R, the first resistor has a resistance value equal to k1.Math.R, the second resistor has a resistance value equal to k2.Math.R, and the third resistor has a resistance value equal to (1−k1−k2).Math.R.
[0015] In one or more embodiments, the operation mode selection circuit comprises a voltage divider circuit configured to receive the converter input voltage and produce a first signal proportional to the converter input voltage and a second signal proportional to the converter input voltage. The proportionality factor of the first signal to the converter input voltage is higher than the proportionality factor of the second signal to the converter input voltage. The operation mode selection circuit comprises a first comparator configured to assert the buck mode enable signal in response to the first signal being higher than a further reference voltage, and de-assert the buck mode enable signal in response to the first signal being lower than the further reference voltage. The operation mode selection circuit comprises a second comparator configured to assert the boost mode enable signal in response to the further reference voltage being higher than the second signal, and de-assert the boost mode enable signal in response to the further reference voltage being lower than the second signal.
[0016] In one or more embodiments, the further reference voltage is linearly dependent on the reference voltage, or is proportional to the reference voltage, or is the same as the reference voltage.
[0017] In one or more embodiments, the control circuit includes a first comparator circuit configured to compare the buck control signal to the buck ramp signal, assert a buck comparison signal in response to the buck control signal being higher than the buck ramp signal, and de-assert the buck comparison signal in response to the buck control signal being lower than the buck ramp signal. The control circuit includes a second comparator circuit configured to compare the boost control signal to the boost ramp signal, assert a boost comparison signal in response to the boost control signal being higher than the boost ramp signal, and de-assert the boost comparison signal in response to the boost control signal being lower than the boost ramp signal. The control circuit includes a logic circuit configured to assert the buck pulse-width modulated control signal in response to the buck comparison signal being asserted and de-assert the buck pulse-width modulated control signal in response to the buck comparison signal being de-asserted, if the buck mode enable signal is asserted. The logic circuit is configured to assert the boost pulse-width modulated control signal in response to the boost comparison signal being asserted and de-assert the boost pulse-width modulated control signal in response to the boost comparison signal being de-asserted, if the boost mode enable signal is asserted.
[0018] According to another aspect of the present disclosure, a method of operating a buck-boost DC-DC converter circuit comprises receiving a converter input voltage, a buck pulse-width modulated control signal and a boost pulse-width modulated control signal, and producing a converter output voltage as a function thereof; sensing the converter output voltage and a reference voltage, and producing an error signal indicative of a difference between the reference voltage and the converter output voltage; comparing the converter input voltage

to a lower threshold and an upper threshold; asserting a buck mode enable signal in response to the converter input voltage being higher than the lower threshold, and de-asserting the buck mode enable signal in response to the converter input voltage being lower than the lower threshold; asserting a boost mode enable signal in response to the converter input voltage being lower than the upper threshold, and de-asserting the boost mode enable signal in response to the converter input voltage being higher than the upper threshold; producing a buck control signal and a boost control signal as a function of the error signal, the buck mode enable signal and the boost mode enable signal; producing a buck ramp signal as a function of a buck clock signal and a boost ramp signal as a function of a boost clock signal; comparing the buck control signal to the buck ramp signal; if the buck mode enable signal is asserted, asserting the buck pulse-width modulated control signal in response to a pulse in the buck clock signal and de-asserting the buck pulse-width modulated control signal in response to the buck ramp signal being higher than the buck control signal; if the buck mode enable signal is de-asserted, keeping the buck pulse-width modulated control signal asserted; comparing the boost control signal to the boost ramp signal; if the boost mode enable signal is asserted, asserting the boost pulse-width modulated control signal in response to a pulse in the boost clock signal and de-asserting the boost pulse-width modulated control signal in response to the boost ramp signal being higher than the boost control signal; if the boost mode enable signal is de-asserted, keeping the boost pulse-width modulated control signal de-asserted; setting V.sub.C,buck=V.sub.EA, where V.sub.C,buck is the value of the buck control signal and V.sub.EA is the value of the error signal, in response to the buck mode enable signal being asserted and the boost mode enable signal being de-asserted; setting V.sub.C,boost= (V.sub.EA−V.sub.FF), where V.sub.C,boost is the value of the boost control signal, V.sub.EA is the value of the error signal, and V.sub.FF is the value of a feedforward voltage of the buck-boost DC-DC converter circuit, in response to the buck mode enable signal being de-asserted and the boost mode enable signal being asserted; and setting V.sub.C,buck=(V.sub.EA−k2.Math.V.sub.ref1) and V.sub.C,boost=(V.sub.EA−(k1+k2).Math.V.sub.ref1), where V.sub.C,buck is the value of the buck control signal, V.sub.EA is the value of the error signal, V.sub.ref1 is the value of the reference voltage, V.sub.C,boost is the value of the boost control signal, and k1 and k2 are constant values that satisfy the conditions k1+2.Math.k2=1 and 0<k1<1, in response to the buck mode enable signal being asserted and the boost mode enable signal being asserted.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] For a more complete understanding of the present disclosure, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0020] FIG. **1** is a circuit diagram exemplary of a four-switch switching stage of a buck-boost converter;

[0021] FIG. **2** is a time diagram exemplary of the coil current flowing through a coil coupled to the switching stage of FIG. **1** when the converter operates in a two-phase control mode;

[0022] FIG. **3** is a diagram exemplary of possible operating areas of a buck-boost converter;

[0023] FIG. **4** is a time diagram exemplary of possible time evolution of the coil current and of the converter clock signal for a buck-boost converter that operates in pure buck mode inside the dead zone;

[0024] FIG. **5** is a circuit block diagram exemplary of a buck-boost converter according to one or more embodiments of the present disclosure;

[0025] FIG. **6** is a circuit block diagram exemplary of possible implementation details of an error amplifier circuit of a buck-boost converter according to one or more embodiments of the present disclosure;

[0026] FIG. **7** is a schematic time diagram exemplary of the possible time evolution of signals in a buck-boost converter according to one or more embodiments of the present disclosure;

[0027] FIG. **8** is a circuit block diagram exemplary of possible implementation details of an operating mode selection circuit of a buck-boost converter according to one or more embodiments of the present disclosure;

[0028] FIG. **9** is a time diagram exemplary of the possible time evolution of signals in an operating mode selection circuit as exemplified in FIG. **8**;

[0029] FIG. **10** is a circuit block diagram exemplary of possible implementation details of an analog voltage shifter circuit of a buck-boost converter according to one or more embodiments of the present disclosure; and

[0030] FIG. **11** is a time diagram exemplary of the possible time evolution of signals in a buck-boost converter according to one or more embodiments of the present disclosure.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0031] In the ensuing description, one or more specific details are illustrated, aimed at providing an in-depth understanding of examples of embodiments of this disclosure. The embodiments may be obtained without one or more of the specific details, or with other methods, components, materials, etc. In other cases, known structures, materials, or operations are not illustrated or described in detail so that certain aspects of embodiments will not be

obscured.
[0032] Reference to “an embodiment” or “one embodiment” in the framework of the present disclosure is intended to indicate that a particular configuration, structure, or characteristic described in relation to the embodiment is included in at least one embodiment. Hence, phrases such as “in an embodiment” or “in one embodiment” that may be present in one or more points of the present disclosure do not necessarily refer to one and the same embodiment. Moreover, particular configurations, structures, or characteristics may be combined in any adequate way in one or more embodiments. The headings/references used herein are provided merely for convenience and hence do not define the extent of protection or the scope of the embodiments.
[0033] Throughout the figures annexed herein, unless the context indicates otherwise, like parts or elements are indicated with like references/numerals and a corresponding disclosure will not be repeated for the sake of brevity.
[0034] FIG. **1** is a circuit diagram exemplary of the switching stage **10** of a buck-boost converter **1**, particularly a four-switch non-inverting buck-boost converter. The switching stage **10** comprises an input node **102** configured to receive an input voltage V.sub.in, an output node **104** configured to produce an output voltage V.sub.out, and a reference voltage node **106** (or ground node) configured to provide a reference voltage (or ground voltage) V.sub.gnd (e.g., 0 V). A first half-bridge circuit (buck half-bridge circuit) is arranged between the input node **102** and the ground node **106**, and includes a first high-side switch S**1** arranged between the input node **102** and a first intermediate node (or switching node) **108**, and a first low-side switch S**2** arranged between the first switching node **108** and the ground node **106**. A second half-bridge circuit (boost half-bridge circuit) is arranged between the output node **104** and the ground node **106**, and includes a second high-side switch S**3** arranged between the output node **104** and a second intermediate node (or switching node) **110**, and a second low-side switch S**4** arranged between the second switching node **110** and the ground node **106**. A coil L (e.g., an inductor, possibly external to the integrated circuit that incorporates the converter **1**) is arranged between the switching nodes **108** and **110**.
[0035] FIG. **2** is a time diagram exemplary of the time evolution of the coil current i.sub.L flowing through the coil L coupled to converter **1** when the converter operates in a two-phase control mode, i.e., when each switching cycle comprises two phases. In a first phase PH**1**, switches S**1** and S**4** are closed and switches S**2** and S**3** are open, so that the coil L is energized (e.g., magnetized, charged) by being coupled between the input node **102** at voltage V.sub.in and the ground node **106** at voltage V.sub.gnd, with current i.sub.L flowing from node **102** to node **106** as exemplified by the dash-and-dot line in FIG. **2**. In a second phase PH**2**, switches S**2** and S**3** are closed and switches S**1** and S**4** are open, so that the coil L is de-energized (e.g., demagnetized, discharged) by being coupled between the ground node **106** at voltage V.sub.gnd and the output node **104** at voltage V.sub.out, with current i.sub.L flowing from node **106** to node **104** as exemplified by the dotted line in FIG. **2**. The two-phase operation mode can be used for every combination of input and output voltages, since it does not depend on the difference between the input voltage V.sub.in and the output voltage V.sub.out. However, the two-phase operation mode may result in a high coil current ripple Δi.sub.L and a high root mean square (rms) value of the coil current i.sub.L, which lead to poor efficiency and low usability of this control scheme. For instance, with V.sub.in=V.sub.out=12 V, an inductance of the coil L equal to 2 μH and a switching frequency f.sub.SW of about 1 MHz, the coil current ripple Δi.sub.L may be about 3 A.
[0036] Some solutions aiming at reducing the coil current ripple Δi.sub.L may rely on increasing the inductance value of the coil L or increasing the switching frequency of the converter **1**, which however may result in a large area occupation on the printed circuit board (PCB), a high cost, low efficiency, or a combination of both.
[0037] To overcome these drawbacks, a buck-boost converter can be forced to operate in pure buck mode by stopping the switching activity of the boost half-bridge circuit S**3**, S**4** when V.sub.in>V.sub.out or in pure boost mode by stopping the switching activity of the buck half-bridge circuit S**1**, S**2** when V.sub.in<V.sub.out. To this regard, FIG. **3** is a diagram exemplary of possible operating areas of a buck-boost converter, which depend on the values of the input voltage V.sub.in and of the output voltage V.sub.out. In particular, the buck-boost converter may operate in pure boost mode (i.e., with switch S**1** steadily closed and switch S**2** steadily open) when in the operating area Z**1**, and in pure buck mode (i.e., with switch S**3** steadily closed and switch S**4** steadily open) when in the operating area Z**2**. However, when operating in the operating area Z**3** where V.sub.in≈V.sub.out, a so-called “dead zone” has to be taken into consideration, whose limits depend on the minimum turn-off time T.sub.off and turn-on time T.sub.on that can be managed by the gate drivers that drive the first and second half-bridge circuits (i.e., that drive switching of switches S**1**, S**2**, S**3**, S**4**).
[0038] In conventional fixed-frequency systems, the turn-on and turn-off timings suitable for operating in the dead zone Z**3** cannot be provided by the gate drivers, resulting in some switching pulses possibly being skipped (e.g., missed) and the coil current ripple Δi.sub.L increasing again as exemplified in the time diagrams of FIG. **4**, which illustrate a possible time evolution of the coil current i.sub.L and of the converter clock signal CLK for a buck-boost converter that operates in pure buck mode inside the dead zone Z**3** of FIG. **3**. This unwanted behavior (i.e., unexpected pulse skipping) may in turn cause system meta-stability and oscillations of the converter.
[0039] Some solutions to control a buck-boost converter in the dead zone Z**3** may resort to a three-phase control

scheme. In the third phase that follows the second phase, the coil L is coupled between the input node **102** and the output node **104** (i.e., switches S**1** and S**3** are closed, and switches S**2** and S**4** are open), with the coil current i.sub.L being almost flat during such a third phase.

[0040] FIG. **5** is a circuit block diagram exemplary of a fixed-frequency, dual-ramp buck-boost non-inverting converter **5** according to one or more embodiments of the present disclosure. In particular, FIG. **5** is exemplary of the control architecture of converter **5**. Converter **5** comprises an error amplifier circuit **50** (e.g., a differential amplifier) configured to compare the converter output voltage V.sub.out to a reference voltage V.sub.ref1 and produce an error signal V.sub.EA indicative of the difference between V.sub.ref1 and V.sub.out. For instance, the error amplifier circuit **50** may comprise a first input node **501** configured to receive the converter output voltage V.sub.out, a second input node **502** configured to receive the reference voltage V.sub.ref1, and an output node **503** configured to produce the error signal V.sub.EA. The error amplifier circuit **50** may comprise an operational amplifier circuit **504** having a first (e.g., non-inverting) input coupled to node **502** to receive voltage V.sub.ref1 and a second (e.g., inverting) input coupled to node **501** via a feedback circuitry block **505** to receive voltage V.sub.out. The error amplifier circuit **50** may comprise another feedback circuitry block **506** coupled between the second input and the output node **503** to close the feedback loop of the amplifier circuit **50**.

[0041] For instance, as exemplified in FIG. **6**, the feedback circuitry block **505** may comprise a feedback voltage divider arranged between node **501** and the ground node (e.g., **106**). The feedback voltage divider may comprise a first resistor R.sub.FB1 arranged between node **501** and the inverting input of amplifier **504**, and a second resistor R.sub.FB2 arranged between the inverting input of amplifier **504** and the ground node. Resistor R.sub.FB2 may have a resistance value lower than the resistance value of resistor R.sub.FB1 (e.g., R.sub.FB2=R.sub.FB1/9). Additionally, the feedback circuitry block **505** may comprise a resistor R.sub.S and a capacitor C.sub.S arranged in series between node **501** and the inverting input of amplifier **504** (i.e., in parallel to resistor R.sub.FB1). The feedback circuitry block **506** may comprise a capacitor C.sub.P arranged between the inverting input of amplifier **504** and the output node **503** of amplifier **504**. The feedback circuitry block **506** may further comprise a resistor R.sub.F and a capacitor C.sub.F arranged in series between the inverting input of amplifier **504** and the output node **503** of amplifier **504** (i.e., in parallel to capacitor C.sub.P). The feedback loop of converter **5** operates so that, in steady state conditions, the voltage at the inverting input of amplifier **504**, i.e., a scaled replica of the output voltage V.sub.out (e.g., V.sub.out/10 in case R.sub.FB2=R.sub.FB1/9) is equal to the reference voltage V.sub.ref1.

[0042] Again, with reference to FIG. **5**, converter **5** comprises a mode selection circuit **51** configured to produce a buck mode enable signal EN.sub.buck and a boost mode enable signal EN.sub.boost as a function of the value of the converter input voltage V.sub.in and (indirectly) of the value of converter output voltage V.sub.out. For instance, the mode selection circuit **51** may comprise a first input node **511** configured to receive the converter input voltage V.sub.in, and a second input node **512** configured to receive a reference voltage V.sub.ref2. Reference voltage V.sub.ref2 may be equal to reference voltage V.sub.ref1, or proportional to reference voltage V.sub.ref1, or linearly dependent to reference voltage V.sub.ref1, which in turn is related to the output voltage V.sub.out. Alternatively, reference voltage V.sub.ref2 may be set independently from reference voltage V.sub.ref1, using proper trimming depending on the application.

[0043] The mode selection circuit **51** may be configured to assert (e.g., set to a high value, logic 1) the buck mode enable signal EN.sub.buck in response to the input voltage V.sub.in being higher than a first threshold V.sub.th,buck, and de-assert (e.g., set to a low value, logic 0) the buck mode enable signal EN.sub.buck in response to the input voltage V.sub.in being lower than the first threshold V.sub.th,buck. The mode selection circuit **51** may be configured to assert (e.g., set to a high value, logic 1) the boost mode enable signal EN.sub.boost in response to the input voltage V.sub.in, being lower than a second threshold V.sub.th,boost, and de-assert (e.g., set to a low value, logic 0) the boost mode enable signal EN.sub.boost in response to the input voltage V.sub.in being higher than the second threshold V.sub.th,boost. The second threshold V.sub.th,boost may be higher than the first threshold V.sub.th,buck. The buck mode enable signal EN.sub.buck and the boost mode enable signal EN.sub.boost are used to control the operating mode of converter **5** (e.g., pure buck, pure boost or buck-boost) as further disclosed in the following.

[0044] Converter **5** comprises a voltage shifter circuit **52** (e.g., an analog voltage shifter) configured to produce a buck control signal V.sub.C,buck and a boost control signal V.sub.C,boost as a function of the value of the error signal V.sub.EA, and depending on the current operating mode of the converter **5** (e.g., pure buck, pure boost or buck-boost) determined by the values of signals EN.sub.buck and EN.sub.boost. Further details of voltage shifter circuit **52** are disclosed in the following.

[0045] Converter **5** comprises a dual ramp generator circuit **53** configured to produce a buck ramp signal V.sub.R,buck and a boost ramp signal V.sub.R,boost as a function of a buck clock signal CLK.sub.buck and a boost clock signal CLK.sub.boost, respectively. For instance, the ramp signals V.sub.R,buck and V.sub.R,boost may have a triangular or saw-tooth waveform produced according to the conventional operation of switching converters. The ramp signals V.sub.R,buck and V.sub.R,boost may be time-shifted with respect to one another. The

ramp signals V.sub.R,buck and V.sub.R,boost may be used to control the buck half-bridge and the boost half-bridge of the switching stage **10** separately.

[0046] Converter **5** comprises a first comparator circuit **54** having a first (e.g., non-inverting) input configured to receive the buck control signal V.sub.C,buck and a second (e.g., inverting) input configured to receive the buck ramp signal V.sub.R,buck to produce a buck comparison signal C.sub.buck. Therefore, the buck comparison signal C.sub.buck may be asserted (e.g., set to a high logic value, logic 1) when V.sub.C,buck>V.sub.R,buck and de-asserted (e.g., set to a low logic value, logic 0) when V.sub.C,buck<V.sub.R,buck.

[0047] Converter **5** comprises a second comparator circuit **55** having a first (e.g., non-inverting) input configured to receive the boost control signal V.sub.C,boost and a second (e.g., inverting) input configured to receive the boost ramp signal V.sub.R,boost to produce a boost comparison signal C.sub.boost. Therefore, the boost comparison signal C.sub.boost may be asserted (e.g., set to a high logic value, logic 1) when V.sub.C,boost>V.sub.R,boost and de-asserted (e.g., set to a low logic value, logic 0) when V.sub.C,boost<V.sub.R,boost.

[0048] Converter **5** comprises a logic and driver circuit **56** (e.g., a control circuit) configured to receive signals EN.sub.buck, EN.sub.boost, C.sub.buck, C.sub.boost, CLK.sub.buck and CLK.sub.boost and produce, as a function thereof, a pulse-width modulated (PWM) buck signal P.sub.buck and a pulse-width modulated (PWM) boost signal P.sub.boost for controlling the commutation of switches S**1**, S**2**, S**3** and S**4**, thereby determining the commutation duty-cycle D.sub.buck of the buck half-bridge circuit (i.e., switches S**1** and S**2**) and the commutation duty-cycle D.sub.boost of the boost half-bridge circuit (i.e., switches S**3** and S**4**). It is assumed herein that when the PWM buck signal P.sub.buck is asserted, switch S**1** is closed (e.g., on, conductive) and switch S**2** is open (e.g., off, non-conductive), while when the PWM buck signal P.sub.buck is de-asserted, switch S**1** is open and switch S**2** is closed. Similarly, when the PWM boost signal P.sub.boost is asserted, switch S**3** is open and switch S**4** is closed, while when the PWM boost signal P.sub.boost is de-asserted, switch S**3** is closed and switch S**4** is open.

[0049] In particular, the PWM signals P.sub.buck and P.sub.boost may be produced by circuit **56** according to the following logic. Provided that the enable signal EN.sub.buck is asserted, signal P.sub.buck may be asserted (e.g., a rising edge may be generated therein) in response to a pulse in the clock signal CLK.sub.buck, and may be de-asserted (e.g., a falling edge may be generated therein) in response to the ramp signal V.sub.R,buck exceeding the control signal V.sub.C,buck (i.e., in response to the comparison signal C.sub.buck being de-asserted). Otherwise, if the enable signal EN.sub.buck is de-asserted, signal P.sub.buck may be kept asserted independently from the value of the comparison signal C.sub.buck.

[0050] Provided that the enable signal EN.sub.boost is asserted, signal P.sub.boost may be asserted (e.g., a rising edge may be generated therein) in response to a pulse in the clock signal CLK.sub.boost, and may be de-asserted (e.g., a falling edge may be generated therein) in response to the ramp signal V.sub.R,boost exceeding the control signal V.sub.C,boost (i.e., in response to the comparison signal C.sub.boost being de-asserted). Otherwise, if the enable signal EN.sub.boost is de-asserted, signal P.sub.boost may be kept de-asserted independently from the value of the comparison signal C.sub.boost.

[0051] Operation of converter **5** as described with reference to FIG. **5** may be further understood by referring to FIG. **7**, which illustrates time diagrams exemplary of signals V.sub.in, V.sub.out, V.sub.th,buck, V.sub.th,boost, EN.sub.buck, EN.sub.boost, CLK.sub.buck, CLK.sub.boost, V.sub.R,buck, V.sub.R,boost, V.sub.C,buck, V.sub.C,boost, C.sub.buck, C.sub.boost, P.sub.buck and P.sub.boost in the converter **5** when passing from boost mode operation, to buck-boost mode operation, to buck mode operation.

[0052] As exemplified in FIG. **7**, when the input voltage V.sub.in is lower than the mode detector threshold V.sub.th,buck, the buck enable signal EN.sub.buck is de-asserted (e.g., low) and the boost enable signal EN.sub.boost is asserted (e.g., high). The converter **5** operates in boost mode: signal P.sub.buck is kept asserted—that is, switch S**1** is kept conductive (on) and switch S**2** is kept non-conductive (off)—while the pulses of clock signal CLK.sub.boost and the value of comparison signal C.sub.boost define the shape and duty-cycle of the boost PWM signal P.sub.boost that controls switches S**3** and S**4**.

[0053] As exemplified in FIG. **7**, when the input voltage V.sub.in is higher than the mode detector threshold V.sub.th,boost, the buck enable signal EN.sub.buck is asserted (e.g., high) and the boost enable signal EN.sub.boost is de-asserted (e.g., low). The converter **5** operates in buck mode: signal P.sub.boost is kept de-asserted—that is, switch S**3** is kept conductive (on) and switch S**4** is kept non-conductive (off)—while the pulses of clock signal CLK.sub.buck and the value of comparison signal C.sub.buck define the shape and duty-cycle of the buck PWM signal P.sub.buck that controls switches S**1** and S**2**.

[0054] Still as exemplified in FIG. **7**, when the input voltage V.sub.in is between the mode detector thresholds V.sub.th,buck and V.sub.th,boost, both signals EN.sub.buck and EN.sub.boost are asserted (e.g., high) and the converter **5** operates in buck-boost mode. Both the buck half-bridge circuit and the boost half-bridge circuit switch with different duty-cycles under control of PWM signals P.sub.buck and P.sub.boost, respectively. In buck-boost mode, the shape and duty-cycle of signal P.sub.buck depend on the pulses of clock signal CLK.sub.buck and on

the value of comparison signal C.sub.buck, while the shape and duty-cycle of signal P.sub.boost depend on the pulses of clock signal CLK.sub.boost and on the value of comparison signal C.sub.boost.

[0055] FIG. **8** is a circuit diagram exemplary of possible implementation details of a mode selection circuit **51** according to one or more embodiments. FIG. **9** is a time diagram exemplary of signals EN.sub.buck and EN.sub.boost as a function of voltage V.sub.in, and is exemplary of operation of the mode selection circuit **51**. Mode selection circuit **51** may comprise a voltage divider circuit for producing two signals V.sub.1 and V.sub.2 proportional to the input voltage V.sub.in. For instance, a resistive voltage divider may comprise a first resistor R**1**, a second resistor R**2** and a third resistor R**3** arranged in series between the reference voltage node **106** (at voltage V.sub.gnd, e.g., 0 V) and the input node **511** (at voltage V.sub.in). A first comparator circuit **513** (e.g., a comparator with hysteresis) may have a first (e.g., non-inverting) input coupled to a node intermediate resistors R**3** and R**2** to receive signal V.sub.1, and a second (e.g., inverting) input coupled to node **512** to receive the reference voltage V.sub.ref2. Signal EN.sub.buck may be produced at the output of comparator **513**. Therefore, signal EN.sub.buck may be asserted if V.sub.ref2<V.sub.1 where V.sub.1=V.sub.in.Math.(R**1**+R**2**)/(R**1**+R**2**+R**3**) or, in other terms, if V.sub.in>V.sub.th,buck where V.sub.th,buck=V.sub.ref2.Math.(R**1**+R**2**+R**3**)/(R**1**+R**2**). A second comparator circuit **514** (e.g., a comparator with hysteresis) may have a first (e.g., inverting) input coupled to a node intermediate resistors R**2** and R**1** to receive signal V.sub.2, and a second (e.g., non-inverting) input coupled to node **512** to receive the reference voltage V.sub.ref2. Signal EN.sub.boost may be produced at the output of comparator **514**. Therefore, signal EN.sub.boost may be asserted if V.sub.ref2>V.sub.2 where V.sub.2=V.sub.in.Math.R**1**/(R**1**+R**2**+R**3**) or, in other terms, if V.sub.in<V.sub.th,boost where V.sub.th,boost=V.sub.ref2.Math.(R**1**+R**2**+R**3**)/R**1**. From the equations above, it is also noted that V.sub.th,boost>V.sub.th,buck.

[0056] Therefore, the following operating regions can be identified, depending on the value of voltage V.sub.in, as exemplified in FIG. **9**. If V.sub.in<V.sub.th,buck, then EN.sub.buck=0 and EN.sub.boost=1, and converter **5** operates in boost mode. If V.sub.th,buck<V.sub.in<V.sub.th,boost, then EN.sub.buck=1 and EN.sub.boost=1, and converter **5** operates in buck-boost mode. If V.sub.in>V.sub.th,boost, then EN.sub.buck=1 and EN.sub.boost=0, and converter **5** operates in buck mode. The values of the thresholds, V.sub.th,buck and V.sub.th,boost, define the limits of the buck-boost operating region and control the minimum T.sub.on (respectively, T.sub.off) that the converter can reach in boost (respectively, buck) operation mode. The size of the buck-boost operating region may be defined as a trade-off between the converter efficiency and the minimum T.sub.on/T.sub.off achievable by the gate drivers.

[0057] Providing smooth transitions between the three operating regions of converter **5** along with input voltage feed-forward is a desirable feature. Therefore, in one or more embodiments the analog voltage shifter circuit **52** may be configured to implement three different relationships between the control signals V.sub.C,buck and V.sub.C,boost and the error signal V.sub.EA, so as to keep the error signal V.sub.EA ideally constant throughout the ranges of V.sub.in and V.sub.out, as disclosed in the following.

[0058] Considering the step-down buck portion of converter **5**, the input/output voltage relationship V.sub.out=D.sub.buck.Math.V.sub.in leads to the following steady state value for D.sub.buck (equation 1):

[00001] $D_{buck} = V_{out} / V_{in}$ (1)

[0059] In a fixed-frequency architecture as considered herein, the value of the duty-cycle D.sub.buck follows from the comparison of the buck control signal V.sub.C,buck with the buck ramp signal V.sub.R,buck, which shapes the buck PWM signal P.sub.buck. If the height of the ramp signal V.sub.R,buck (i.e., the difference between the ramp maximum value and the ramp minimum value, which is also equal to the ramp slew rate multiplied the clock period) is equal to the feed-forward voltage V.sub.FF=V.sub.in/α (where α=V.sub.out/V.sub.ref1; consequently, V.sub.FF=V.sub.ref1.Math.V.sub.in/V.sub.out) and the control voltage V.sub.C,buck is equal to the error signal V.sub.EA, then the duty-cycle D.sub.buck can be computed according to equation 2 below:

[00002] $D_{buck} = V_{EA} / V_{FF}$ (2)

[0060] Combining equations 1 and 2 above, the steady state value of the error signal V.sub.EA can be written as V.sub.EA=V.sub.out/α and does not depend on the value of the converter input voltage V.sub.in.

[0061] Considering now the step-up boost portion of converter **5**, the input/output voltage relationship V.sub.out=V.sub.in/(1−D.sub.boost) leads to the following steady state value for D.sub.boost: D.sub.boost=1−V.sub.in/V.sub.out. In a fixed-frequency architecture as considered herein, the value of the duty-cycle D.sub.boost follows from the comparison of the boost control signal V.sub.C,boost with the boost ramp signal V.sub.R,boost, which shapes the boost PWM signal P.sub.boost. If the height of the ramp signal V.sub.R,boost is equal to the reference voltage V.sub.ref1=V.sub.out/α and the control voltage V.sub.C,boost is equal to the difference between the error signal V.sub.EA and the feed-forward voltage V.sub.FF (V.sub.C,boost=V.sub.EA−V.sub.FF), then the duty-cycle D.sub.boost can be computed as: D.sub.boost= (V.sub.EA−V.sub.FF)/V.sub.ref1. The steady state value of the error signal V.sub.EA can thus be written as

V.sub.EA=V.sub.out/α, which is the same obtained previously for the step-down buck converter, and does not depend on the value of the converter input voltage V.sub.in.

[0062] In one or more embodiments, the analog voltage shifter circuit **52** may thus be configured to produce control voltages V.sub.C,buck and V.sub.C,boost so that, when converter **5** operates in the buck-boost mode, the error signal V.sub.EA maintains a value V.sub.EA=V.sub.out/α, which facilitates smooth transitions between the converter operating modes.

[0063] Considering the buck-boost operation of converter **5**, the input/output voltage relationship can be written according to equation 3 below:

[00003] $V_{out} = (D_{buck} / (1 - D_{boost}))$ .Math. V_{in} (3)

[0064] If the height of the buck ramp signal V.sub.R,buck is equal to the feed-forward voltage V.sub.FF=V.sub.in/α (as considered before) and the buck control voltage V.sub.C,buck is shifted with respect to the error signal V.sub.EA by a quantity k2.Math.V.sub.ref1 (i.e., V.sub.C,buck=V.sub.EA−k2.Math.V.sub.ref1 with k2 being a constant), then the duty-cycle D.sub.buck can be computed according to equation 4 below:

[00004] $D_{buck} = (V_{EA} - k2$ .Math. $V_{\text{ref1}}) / V_{\text{FF}}$ (4)

[0065] Similarly, if the height of the boost ramp signal V.sub.R,boost is equal to reference voltage V.sub.ref1 (as considered before) and the boost control voltage V.sub.C,boost is shifted with respect to the error signal V.sub.EA by a quantity (k1+k2).Math.V.sub.ref1 (i.e., V.sub.C,boost=V.sub.EA−(k1+k2).Math.V.sub.ref1 or, in other terms, V.sub.C,buck−V.sub.C,boost=k1.Math.V.sub.ref1, with k1 being a constant), then the duty-cycle D.sub.boost can be computed according to equation 5 below:

[00005] $D_{boost} = (V_{EA} - (k1 + k2)$ .Math. $V_{\text{ref1}}) / V_{\text{ref1}}$ (5)

[0066] Combining equations 4 and 5 into equation 3 above, the steady state value of the error signal V.sub.EA can be written according to equation 6 below:

[00006] $V_{EA} = V_{\text{ref1}}$ .Math. $(1 + k1 + 2$ .Math. $k2) / 2$ (6)

[0067] If the condition k1+2.Math.k2=1 holds true, and a value of k1 between 0 and 1 is selected (i.e., 0<k1<1), the steady state value of the error signal V.sub.EA can be written as V.sub.EA=V.sub.out/α, which is the same obtained previously for the step-down buck conversion and the step-up boost conversion, resulting in continuity of operation throughout the three operating modes of converter **5**.

[0068] FIG. **10** is a circuit diagram exemplary of possible implementation details of a voltage shifter circuit **52** according to one or more embodiments, which operates according to the principle disclosed in the foregoing.

[0069] As exemplified in FIG. **10**, voltage shifter circuit **52** may comprise a voltage divider circuit including a first resistor R**4** arranged between node **901** and node **902**, a second resistor R**5** arranged between node **902** and node **903**, and a third resistor R**6** arranged between node **903** and node **904**. The second resistor R**5** may be by-passed via a switch S**5** arranged between node **902** and node **903** (i.e., in parallel to resistor R**5**); switch S**5** is controlled by the complement of the boost enable signal EN.sub.boost, e.g., switch S**5** is closed when signal EN.sub.boost is de-asserted and is open when signal EN.sub.boost is asserted. The third resistor R**6** may be by-passed via a switch S**6** arranged between node **903** and node **904** (i.e., in parallel to resistor R**6**); switch S**6** is controlled by the buck enable signal EN.sub.buck, e.g., switch S**6** is closed when signal EN.sub.buck is asserted and is open when signal EN.sub.buck is de-asserted. Node **904** is configured to receive the error signal V.sub.EA from the error amplifier circuit **50**. Node **902** is configured to produce the buck control signal V.sub.C,buck and node **901** is configured to produce the boost control signal V.sub.C,boost.

[0070] As exemplified in FIG. **10**, a first current generator **911** may be selectively coupled between node **901** and the ground node **106** at voltage V.sub.gnd by closing a switch S**11** that is controlled by the complement of the buck enable signal EN.sub.buck, e.g., switch S**11** is closed when signal EN.sub.buck is de-asserted and is open when signal EN.sub.buck is asserted. The first current generator **911** may be configured to sink from node **901** a current proportional to the feed-forward voltage V.sub.FF, as further disclosed in the following. A second current generator **912** may be selectively coupled between node **901** and the ground node **106** at voltage V.sub.gnd by closing a switch S**12** that is controlled by the buck enable signal EN.sub.buck, e.g., switch S**12** is closed when signal EN.sub.buck is asserted and is open when signal EN.sub.buck is de-asserted. In other words, switches S**11** and S**12** operate complementarily. The second current generator **912** may be configured to sink from node **901** a current proportional to the reference voltage V.sub.ref1, as further disclosed in the following.

[0071] As exemplified in FIG. **10**, a third current generator **913** may be selectively coupled between a supply voltage node **920** at voltage V.sub.DD and node **904** by closing a switch S**13** that is controlled by the complement of the buck enable signal EN.sub.buck, e.g., switch S**13** is closed when signal EN.sub.buck is de-asserted and is open when signal EN.sub.buck is asserted. The third current generator **913** may be configured to source to node **904** a current proportional to the feed-forward voltage V.sub.FF, as further disclosed in the following. A fourth current generator **914** may be selectively coupled between the supply voltage node **920** at voltage V.sub.DD and

node **904** by closing a switch S**14** that is controlled by the buck enable signal EN.sub.buck, e.g., switch S**14** is closed when signal EN.sub.buck is asserted and is open when signal EN.sub.buck is de-asserted. In other words, switches S**13** and S**14** operate complementarily; switch S**13** operates synchronously with switch S**11**; and switch S**14** operates synchronously with switch S**12**. The fourth current generator **914** may be configured to source to node **904** a current proportional to the reference voltage V.sub.ref1, as further disclosed in the following.

[0072] As exemplified in FIG. **10**, voltage shifter circuit **52** may comprise a first voltage-to-current converter circuit **93** configured to produce a signal proportional to the feed-forward voltage V.sub.FF to control the first current generator **911** and the third current generator **913**. In particular, circuit **93** may comprise an operational amplifier circuit **931** configured to receive voltage V.sub.FF at its non-inverting input, and arranged in a voltage buffer configuration (i.e., having its inverting input directly connected to its output) to pass voltage V.sub.FF to a first terminal of a resistor R**93** having a resistance value equal to R. The second terminal of resistor R**93** is coupled to the ground node **106** at voltage V.sub.gnd. By sensing the current flowing through resistor R**93**, a signal proportional to V.sub.FF (in particular, equal to V.sub.FF/R) is produced and used to control the current generators **911** and **913**.

[0073] As exemplified in FIG. **10**, voltage shifter circuit **52** may comprise a second voltage-to-current converter circuit **94** configured to produce a signal proportional to the reference voltage V.sub.ref1 to control the second current generator **912** and the fourth current generator **914**. In particular, circuit **94** may comprise an operational amplifier circuit **941** configured to receive voltage V.sub.ref1 at its non-inverting input, and arranged in a voltage buffer configuration (i.e., having its inverting input directly connected to its output) to pass voltage V.sub.ref1 to a first terminal of a resistor R**94** having a resistance value equal to R. The second terminal of resistor R**94** is coupled to the ground node **106** at voltage V.sub.gnd. By sensing the current flowing through resistor R**94**, a signal proportional to V.sub.ref1 (in particular, equal to V.sub.ref1/R) is produced and used to control the current generators **912** and **914**.

[0074] In one or more embodiments as exemplified in FIG. **10**, resistor R**4** may have a resistance value equal to k1.Math.R, resistor R**5** may have a resistance value equal to k2.Math.R, and resistor R**6** may have a resistance value equal to (1−k1−k2).Math.R. By resorting to such dimensioning criteria, and considering that the topology of the analog voltage shifter circuit **52** is determined by the operation mode of converter **5** (buck, boost or buck-boost) via switches S**5**, S**6**, S**11**, **512**, S**13** and S**14**, operation of converter **5** as previously discussed can be achieved. For instance, when the converter **5** operates in buck mode, resistors R**5** and R**6** are by-passed via closed switches S**5** and S**6**, node **902** is directly coupled to node **904** and thus V.sub.C,buck=V.sub.EA. When the converter **5** operates in boost mode, both switches S**5** and S**6** are open, and thus V.sub.C,boost=V.sub.EA−(R**4**+R**5**+R**6**).Math.V.sub.FF/R=V.sub.EA−(k1.Math.R+k2.Math.R+(1−k1−k2).Math.R).Math.V.sub.FF/R=V.sub.EA−V.sub.FF. When the converter **5** operates in buck-boost mode, switch S**5** is open and switch S**6** is closed, and thus:

[00007] $V_{C,\text{buck}} = V_{EA} - R_5 \text{ .Math. } V_{\text{ref1}} / R = V_{EA} - k2 \text{ .Math. } R \text{ .Math. } V_{\text{ref1}} / R = V_{EA} - k2 \text{ .Math. } V_{\text{ref1}}$

$V_{C,\text{boost}} = V_{EA} - (R_4 + R_5) \text{ .Math. } V_{\text{ref1}} / R = V_{EA} - (k1 + k2) \text{ .Math. } R \text{ .Math. } V_{\text{ref1}} / R = V_{EA} - (k1 + k2) \text{ .Math. } V_{\text{ref1}}$

[0075] Since all the voltage shifts are proportional to resistor ratios, high accuracy can be achieved in an integrated circuit including converter **5** by matching the resistors.

[0076] Table I at the end of the description provides examples of the minimum T.sub.on and T.sub.off times for all operation modes of buck and boost bridges in accordance with some embodiments. As far as buck and boost modes are concerned, the minimum T.sub.off and T.sub.on, respectively, may be guaranteed by the mode detector thresholds. On the other hand, the minimum T.sub.off and T.sub.on within the buck-boost operating region are guaranteed by selecting the value of the constant k1. Therefore, in order to improve the converter efficiency, the buck-boost operating region (where all the four switches S**1**, S**2**, S**3** and S**4**, e.g., power MOS transistors, are switching) should be as little as possible, while the buck and boost regions (where only two of the four switches S**1**, S**2**, S**3** and S**4** are switching) should be extended. By knowing the minimum on/off time managed by the gate drivers (e.g., included in the driver circuit **56**), it is possible to avoid by design the dead zone and improving converter efficiency, by selecting the proper values of k1 and mode detector thresholds.

[0077] Operation of one or more embodiments of converter **5** may be further understood by referring to FIG. **11**, which illustrates time diagrams exemplary of signals V.sub.out, i.sub.L, V.sub.R,buck, V.sub.R,boost, V.sub.C,buck, V.sub.C,boost, V.sub.EA, EN.sub.buck and EN.sub.boost in the converter **5** when passing from boost mode operation (until instant t.sub.1, with EN.sub.buck=0 and EN.sub.boost=1), to buck-boost mode operation (from instant t.sub.1 to instant t.sub.2, with EN.sub.buck=1 and EN.sub.boost=1), to buck mode operation (from instant t.sub.2, with EN.sub.buck=1 and EN.sub.boost=0).

[0078] One or more embodiments may thus provide a DC-DC buck-boost converter having improved efficiency that relies on pure buck operation mode and pure boost operation mode only, avoids operation of the converter in the dead-zone, reduces coil current ripple in the buck-boost region, or both. Without prejudice to the underlying

principles, the details and embodiments may vary, even significantly, with respect to what has been described by way of example only, without departing from the extent of protection.
TABLE-US-00001 TABLE I Boost mode Buck-boost mode Buck mode T.sub.on (boost bridge) [00008] T_{SW} .Math. (1 - $\frac{V_{in}}{V_{out}}$) [00009]T_{SW} .Math. ($\frac{1-k1}{2}$) S.sub.4 always OFF T.sub.off (buck bridge) S.sub.1 always ON [00010]T_{SW} .Math. [1 - ($\frac{1+k1}{2}$) .Math. $\frac{V_{out}}{V_{in}}$] [00011]T_{SW} .Math. (1 - $\frac{V_{out}}{V_{in}}$)

Claims

1. A DC-DC converter control system, comprising: an operation mode selection circuit configured to: compare an input voltage to a lower threshold and an upper threshold, assert a buck mode enable signal in response to the input voltage exceeding the lower threshold and de-assert the buck mode enable signal in response to the input voltage falling below the lower threshold, and assert a boost mode enable signal in response to the input voltage being below the upper threshold and de-assert the boost mode enable signal in response to the input voltage exceeding the upper threshold; and a voltage shifter circuit configured to: receive an error signal representing a difference between an output voltage and a reference voltage, generate a buck control signal and a boost control signal based on the error signal, the buck mode enable signal, and the boost mode enable signal, wherein the voltage shifter circuit applies different relationships between the buck control signal, the boost control signal, and the error signal based on the states of the buck mode enable signal and the boost mode enable signal, and wherein the relationships are selected to maintain a constant error signal value across transitions between operating modes.
2. The DC-DC converter control system of claim 1, wherein the voltage shifter circuit is configured to: set the buck control signal equal to the error signal in response to the buck mode enable signal being asserted and the boost mode enable signal being de-asserted; set the boost control signal equal to a difference between the error signal and a feedforward voltage in response to the buck mode enable signal being de-asserted and the boost mode enable signal being asserted; and set the buck control signal equal to a difference between the error signal and a product of a first constant and the reference voltage, and set the boost control signal equal to a difference between the error signal and a product of a sum of the first constant and a second constant and the reference voltage, in response to the buck mode enable signal being asserted and the boost mode enable signal being asserted, wherein the first constant and the second constant satisfy a predetermined relationship.
3. The DC-DC converter control system of claim 1, further comprising: a ramp generator circuit configured to produce a buck ramp signal as a function of a buck clock signal and produce a boost ramp signal as a function of a boost clock signal; and a control circuit configured to: compare the buck control signal to the buck ramp signal; assert a buck pulse-width modulated control signal in response to a pulse in the buck clock signal and de-assert the buck pulse-width modulated control signal in response to the buck ramp signal being higher than the buck control signal, provided that the buck mode enable signal is asserted; retain the buck pulse-width modulated control signal asserted, provided that the buck mode enable signal is de-asserted; compare the boost control signal to the boost ramp signal; assert a boost pulse-width modulated control signal in response to a pulse in the boost clock signal and de-assert the boost pulse-width modulated control signal in response to the boost ramp signal being higher than the boost control signal, provided that the boost mode enable signal is asserted; and retain the boost pulse-width modulated control signal de-asserted, provided that the boost mode enable signal is de-asserted.
4. The DC-DC converter control system of claim 1, wherein the voltage shifter circuit comprises: a voltage divider circuit including a first node, a second node, a third node, a fourth node, a first resistor coupled between the first node and the second node, a second resistor coupled between the second node and the third node, and a third resistor coupled between the third node and the fourth node, wherein the first node is configured to produce the boost control signal, the second node is configured to produce the buck control signal, and the fourth node is configured to receive the error signal; a first current generator circuit configured to supply to the voltage divider circuit a current proportional to a feedforward voltage; a second current generator circuit configured to supply to the voltage divider circuit a current proportional to the reference voltage; and a plurality of switches controllable by the buck mode enable signal and the boost mode enable signal.
5. The DC-DC converter control system of claim 4, wherein the plurality of switches are arranged to: couple the voltage divider circuit to the first current generator circuit to receive the current proportional to the feedforward voltage in response to the buck mode enable signal being de-asserted; couple the voltage divider circuit to the second current generator circuit to receive the current proportional to the reference voltage in response to the buck mode enable signal being asserted; bypass the second resistor in response to the boost mode enable signal being de-asserted; and bypass the third resistor in response to the buck mode enable signal being asserted.
6. The DC-DC converter control system of claim 4, wherein the voltage shifter circuit further comprises: a first voltage-to-current converter arrangement configured to sense the feedforward voltage and control the first current generator circuit; and a second voltage-to-current converter arrangement configured to sense the reference voltage

and control the second current generator circuit.

7. The DC-DC converter control system of claim 1, wherein the operation mode selection circuit comprises: a voltage divider circuit configured to receive the input voltage and produce a first signal proportional to the input voltage and a second signal proportional to the input voltage, wherein a proportionality factor of the first signal to the input voltage is higher than a proportionality factor of the second signal to the input voltage; a first comparator configured to assert the buck mode enable signal in response to the first signal being higher than a further reference voltage, and de-assert the buck mode enable signal in response to the first signal being lower than the further reference voltage; and a second comparator configured to assert the boost mode enable signal in response to the further reference voltage being higher than the second signal, and de-assert the boost mode enable signal in response to the further reference voltage being lower than the second signal.

8. A method of operating a DC-DC converter, comprising: comparing an input voltage to a lower threshold and an upper threshold; asserting a buck mode enable signal in response to the input voltage exceeding the lower threshold and de-asserting the buck mode enable signal in response to the input voltage falling below the lower threshold; asserting a boost mode enable signal in response to the input voltage being below the upper threshold and de-asserting the boost mode enable signal in response to the input voltage exceeding the upper threshold; generating an error signal representing a difference between an output voltage and a reference voltage; producing a buck control signal and a boost control signal based on the error signal, the buck mode enable signal, and the boost mode enable signal; applying different relationships between the buck control signal, the boost control signal, and the error signal based on states of the buck mode enable signal and the boost mode enable signal, wherein the relationships are selected to maintain a constant error signal value across transitions between operating modes; and controlling a switching stage based on the buck control signal and the boost control signal to generate the output voltage.

9. The method of claim 8, further comprising: generating a buck ramp signal based on a buck clock signal; generating a boost ramp signal based on a boost clock signal; comparing the buck control signal to the buck ramp signal; comparing the boost control signal to the boost ramp signal; asserting a buck pulse-width modulated control signal in response to a pulse in the buck clock signal and de-asserting the buck pulse-width modulated control signal in response to the buck ramp signal being higher than the buck control signal, provided that the buck mode enable signal is asserted; retaining the buck pulse-width modulated control signal asserted, provided that the buck mode enable signal is de-asserted; asserting a boost pulse-width modulated control signal in response to a pulse in the boost clock signal and de-asserting the boost pulse-width modulated control signal in response to the boost ramp signal being higher than the boost control signal, provided that the boost mode enable signal is asserted; and retaining the boost pulse-width modulated control signal de-asserted, provided that the boost mode enable signal is de-asserted.

10. The method of claim 8, wherein producing the buck control signal and the boost control signal comprises: setting the buck control signal equal to the error signal in response to the buck mode enable signal being asserted and the boost mode enable signal being de-asserted; setting the boost control signal equal to a difference between the error signal and a feedforward voltage in response to the buck mode enable signal being de-asserted and the boost mode enable signal being asserted; and setting the buck control signal equal to a difference between the error signal and a product of a first constant and the reference voltage, and setting the boost control signal equal to a difference between the error signal and a product of a sum of the first constant and a second constant and the reference voltage, in response to the buck mode enable signal being asserted and the boost mode enable signal being asserted, wherein the first constant and the second constant satisfy a predetermined relationship.

11. The method of claim 8, wherein comparing the input voltage to the lower threshold and the upper threshold comprises: generating a first signal proportional to the input voltage with a first proportionality factor; generating a second signal proportional to the input voltage with a second proportionality factor lower than the first proportionality factor; comparing the first signal to a further reference voltage to generate the buck mode enable signal; and comparing the second signal to the further reference voltage to generate the boost mode enable signal.

12. The method of claim 11, wherein: the buck mode enable signal is asserted in response to the first signal being higher than the further reference voltage, and de-asserted in response to the first signal being lower than the further reference voltage; and the boost mode enable signal is asserted in response to the further reference voltage being higher than the second signal, and de-asserted in response to the further reference voltage being lower than the second signal.

13. The method of claim 8, wherein the lower threshold and the upper threshold are selected to avoid a dead zone of operation in which minimum on-time or minimum off-time constraints would cause pulse skipping.

14. The method of claim 8, further comprising: operating the DC-DC converter in a buck mode in response to the buck mode enable signal being asserted and the boost mode enable signal being de-asserted; operating the DC-DC converter in a boost mode in response to the buck mode enable signal being de-asserted and the boost mode enable signal being asserted; and operating the DC-DC converter in a buck-boost mode in response to both the buck mode

enable signal and the boost mode enable signal being asserted.

15. A DC-DC converter circuit, comprising: a switching stage having a buck half-bridge circuit including a first high-side switch and a first low-side switch, and a boost half-bridge circuit including a second high-side switch and a second low-side switch; a coil coupled between the buck half-bridge circuit and the boost half-bridge circuit; an error amplifier circuit configured to generate an error signal based on a difference between an output voltage and a reference voltage; an operation mode selection circuit configured to: compare an input voltage to a lower threshold and an upper threshold, assert a buck mode enable signal in response to the input voltage exceeding the lower threshold and de-assert the buck mode enable signal in response to the input voltage falling below the lower threshold, and assert a boost mode enable signal in response to the input voltage being below the upper threshold and de-assert the boost mode enable signal in response to the input voltage exceeding the upper threshold; a voltage shifter circuit configured to generate a buck control signal and a boost control signal based on the error signal, the buck mode enable signal, and the boost mode enable signal, wherein the voltage shifter circuit applies different relationships between the buck control signal, the boost control signal, and the error signal based on states of the buck mode enable signal and the boost mode enable signal; a ramp generator circuit configured to generate a buck ramp signal based on a buck clock signal and a boost ramp signal based on a boost clock signal; and a control circuit configured to generate a buck pulse-width modulated control signal and a boost pulse-width modulated control signal to control the switching stage based on comparisons between the control signals and the ramp signals.

16. The DC-DC converter circuit of claim 15, wherein the control circuit is configured to: assert the buck pulse-width modulated control signal in response to a pulse in the buck clock signal and de-assert the buck pulse-width modulated control signal in response to the buck ramp signal being higher than the buck control signal, provided that the buck mode enable signal is asserted; retain the buck pulse-width modulated control signal as asserted, provided that the buck mode enable signal is de-asserted; assert the boost pulse-width modulated control signal in response to a pulse in the boost clock signal and de-assert the boost pulse-width modulated control signal in response to the boost ramp signal being higher than the boost control signal, provided that the boost mode enable signal is asserted; and retain the boost pulse-width modulated control signal as de-asserted, provided that the boost mode enable signal is de-asserted.

17. The DC-DC converter circuit of claim 15, wherein the voltage shifter circuit is configured to: set the buck control signal equal to the error signal in response to the buck mode enable signal being asserted and the boost mode enable signal being de-asserted; set the boost control signal equal to a difference between the error signal and a feedforward voltage in response to the buck mode enable signal being de-asserted and the boost mode enable signal being asserted; and set the buck control signal equal to a difference between the error signal and a product of a first constant and the reference voltage, and set the boost control signal equal to a difference between the error signal and a product of a sum of the first constant and a second constant and the reference voltage, in response to the buck mode enable signal being asserted and the boost mode enable signal being asserted, wherein the first constant and the second constant satisfy a predetermined relationship.

18. The DC-DC converter circuit of claim 15, wherein the voltage shifter circuit comprises: a voltage divider circuit including a first node, a second node, a third node, a fourth node, a first resistor coupled between the first node and the second node, a second resistor coupled between the second node and the third node, and a third resistor coupled between the third node and the fourth node, wherein the first node is configured to produce the boost control signal, the second node is configured to produce the buck control signal, and the fourth node is configured to receive the error signal; a first current generator circuit configured to supply to the voltage divider circuit a current proportional to a feedforward voltage; a second current generator circuit configured to supply to the voltage divider circuit a current proportional to the reference voltage; and a plurality of switches controllable by the buck mode enable signal and the boost mode enable signal.

19. The DC-DC converter circuit of claim 18, wherein the plurality of switches are arranged to: couple the voltage divider circuit to the first current generator circuit to receive the current proportional to the feedforward voltage in response to the buck mode enable signal being de-asserted; couple the voltage divider circuit to the second current generator circuit to receive the current proportional to the reference voltage in response to the buck mode enable signal being asserted; bypass the second resistor in response to the boost mode enable signal being de-asserted; and bypass the third resistor in response to the buck mode enable signal being asserted.

20. The DC-DC converter circuit of claim 15, wherein the operation mode selection circuit comprises: a voltage divider circuit configured to receive the input voltage and produce a first signal proportional to the input voltage and a second signal proportional to the input voltage, wherein a proportionality factor of the first signal to the input voltage is higher than a proportionality factor of the second signal to the input voltage; a first comparator configured to assert the buck mode enable signal in response to the first signal being higher than a further reference voltage, and de-assert the buck mode enable signal in response to the first signal being lower than the further reference voltage; and a second comparator configured to assert the boost mode enable signal in response

to the further reference voltage being higher than the second signal, and de-assert the boost mode enable signal in response to the further reference voltage being lower than the second signal.