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Time domain analog-to-digital converter and analog-to-digital converting method

Abstract

In analog-to-digital conversion, a plurality of stages configured in a sequence to sequentially decide a plurality of bits in successive-approximation, each of the plurality of stages configured to operate in response to a corresponding clock among a plurality of clocks, and decide a corresponding bit among the plurality of bits from a corresponding positive pulse among a plurality of positive pulses and a corresponding negative pulse among a plurality of negative pulses; and a plurality of clock generating circuits respectively corresponding to a plurality of first stages among the plurality of stages, each of the plurality of clock generating circuit configured to generate the corresponding clock of a corresponding stage among the plurality of first stages based on an operation of a previous stage among the plurality of stages, the previous stage being before the corresponding stage in the sequence.

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATION

(1) This application claims priority to and the benefit of Korean Patent Application No. 10-2022-0161571 filed in the Korean Intellectual Property Office on Nov. 28, 2022, the entire contents of which are incorporated herein by reference.

BACKGROUND

(a) Field

(2) The disclosure relates to a time domain analog-to-digital converter and an analog-to-digital converting method.

(b) Description of the Related Art

(3) An analog-to-digital converter (ADC) receives an analog input voltage and converts it into a digital signal that can be sent to other devices. ADCs may be used in various signal processing devices.

(4) A voltage domain ADC outputs the difference in input voltages as a digital value. This process may take a while due to a settling time of a capacitor and a decision time of a comparator.

SUMMARY

(5) Some example embodiments may provide a time domain analog-to-digital converter and an analog-to-digital converting method for reducing a waiting time.

(6) According to some example embodiments, an analog-to-digital converter may include a plurality of stages and a plurality of clock generating circuits. The plurality of stages may be configured in a sequence to sequentially decide a plurality of bits in a successive-approximation. Each of the plurality of stages configured to operate in response to a corresponding clock among a plurality of clocks, and decide a corresponding bit among the plurality of bits from a corresponding positive pulse among a plurality of positive pulses and a corresponding negative pulse among a plurality of negative pulses, the plurality of positive pulses respectively input to the plurality of stages and the plurality of negative pulses respectively input to the plurality of stages. The plurality of clock generating circuits respectively correspond to a plurality of first stages among the plurality of stages. Each of the plurality of clock generating circuit may generate the corresponding clock of a corresponding stage among the plurality of first stages based on an operation of a previous stage among the plurality of stages, the previous stage being before the corresponding stage in the sequence.

(7) According to some example embodiments, an analog-to-digital converter may include a first time comparator, a first delay circuit, a clock generating circuit, a second time comparator, and a second delay circuit. The first time comparator may operate in response to a first clock and decide a first bit based on a first comparison result of comparing a first positive pulse and a first negative pulse. The first delay circuit may delay either one of the first positive pulse and the first negative pulse by a first reference time based on a value of the first comparison result. The clock generating circuit may generate a second clock in response to the first comparison result. The second time comparator may operate in response to the second clock and decide a second bit based on a second comparison result of comparing a second positive pulse and a second negative pulse output from

the first delay circuit. The second delay circuit may delay either one of the second positive pulse and the second negative pulse by a second reference time based on a value of the second comparison result.
(8) According to some example embodiments, an analog-to-digital converting method may be provided. The analog-to-digital converting method may include receiving a first positive pulse and a first negative pulse, comparing the first positive pulse and the first negative pulse in response to a first clock to generate a first comparison result, deciding a first bit based on a value of the first comparison result, outputting a second positive pulse and a second negative pulse by delaying either one of the first positive pulse and the first negative pulse by a first reference time based on a value of the first comparison result, generating a second clock in response to the first comparison result, comparing the second positive pulse and the second negative pulse in response to the second clock to generate a second comparison result, and deciding a second bit based on a value of the second comparison result.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
(1) FIG. **1** is a block diagram illustrating an example of an analog-to-digital converter according to some example embodiments.
(2) FIG. **2** is a block diagram showing an example of a voltage-to-time converter circuit of an analog-to-digital converter according to some example embodiments,
(3) FIG. **3** is a circuit diagram illustrating an example of a sample/hold and ramp generating circuit in a voltage-to-time converter circuit shown in FIG. **2**.
(4) FIG. **4** is a circuit diagram illustrating an example of a pulse generating circuit in a voltage-to-time converter circuit shown in FIG. **2**.
(5) FIG. **5** is a diagram illustrating an example of a signal generated by a voltage-to-time converter circuit shown in FIG. **2**.
(6) FIG. **6** is a block diagram illustrating an example of a voltage-to-time converter circuit of an analog-to-digital converter according to some example embodiments.
(7) FIG. **7** is a diagram illustrating an example of a signal generated by a voltage-to-time converter circuit shown in FIG. **6**.
(8) FIG. **8** is a block diagram illustrating an example of a stage in a voltage-to-time converter circuit of an analog-to-digital converter according to some example embodiments.
(9) FIG. **9** is a diagram illustrating an example of a clock generating circuit in a voltage-to-time converter circuit of an analog-to-digital converter according to some example embodiments.
(10) FIG. **10** is a block diagram illustrating an example of an analog-to-digital converter according to some example embodiments.
(11) FIG. **11** is a block diagram illustrating an example of a flash voltage-to-time converter circuit according to some example embodiments.
(12) FIG. **12** is a diagram showing an example of a signal generated in a flash voltage-to-time converter circuit shown in FIG. **11**.
(13) FIG. **13** is a flowchart illustrating an example of an analog-to-digital converting method according to some example embodiments.
(14) FIG. **14** is a block diagram illustrating an example of a computing device according to some example embodiments.
(15) FIG. **15** is a block diagram illustrating an example of a communication system according to some example embodiments.
DETAILED DESCRIPTION OF THE EXAMPLE EMBODIMENTS
(16) In the following detailed description, only certain example embodiments of the present

invention have been shown and described, simply by way of illustration. As those skilled in the art would realize, the described example embodiments may be modified in various different ways, all without departing from the spirit or scope of the present invention.

(17) Accordingly, the drawings and description are to be regarded as illustrative in nature and not restrictive. Like reference numerals designate like elements throughout the specification. The sequence of operations or steps is not limited to the order presented in the claims or figures unless specifically indicated otherwise. The order of operations or steps may be changed, several operations or steps may be merged, a certain operation or step may be divided, and a specific operation or step may not be performed.

(18) As used herein, the singular forms “a” and “an” are intended to include the plural forms as well, unless the context clearly indicates otherwise. Although the terms first, second, and the like may be used herein to describe various elements, components, steps and/or operations, these terms are only used to distinguish one element, component, step or operation from another element, component, step, or operation.

(19) FIG. **1** is a block diagram illustrating an example of an analog-to-digital converter according to some example embodiments.

(20) Referring to FIG. **1**, an analog-to-digital converter **100** according to some example embodiments may include a voltage-to-time converter (VTC) circuit **110** and a time-to-digital converter (TDC) circuit **120**.

(21) The VTC circuit **110** may receive an analog signal and convert the analog signal into a time domain to generate a pulse. The analog signal may include a differential input voltage Vinp and Vinn. The pulse may include a positive pulse (or non-inverting pulse) Tinp generated based on a positive input voltage (or non-inverting input voltage) Vinp of the differential input voltage and a negative pulse (or inverting pulse) Tinn generated based on a negative input voltage (or inverting input voltage) Vinn of the differential input voltage. A time difference between a start edge (e.g., a rising edge) of the positive pulse Tinp and a start edge (e.g., a rising edge) of the negative pulse Tinn may be decided based on a voltage difference (e.g., correspond to a voltage difference) between the positive input voltage Vinp and the negative input voltage Vinn.

(22) The TDC circuit **120** may receive the pulses Tinn and Tinp as input values in a time domain, and sequentially decide a plurality of bits (e.g., n bits) D.sub.0 to D.sub.n-1 from the pulses Tinn and Tinp in a successive-approximation. When deciding a bit D.sub.i in a stage, the TDC circuit **120** may generate a clock to be used in a next stage. Here, i is an integer between 1 and n). That is, each stage of the TDC circuit **120** may decide a bit D.sub.i in response to a clock generated according to an operation of a previous stage. In this case, the first stage (or a start stage) of the TDC circuit **120** may decide the first bit (e.g., the most significant bit among the plurality of bits) D.sub.0 in response to an input clock.

(23) FIG. **2** is a block diagram showing an example of a VDC circuit of an analog-to-digital converter according to some example embodiments, FIG. **3** is a circuit diagram illustrating an example of a sample/hold (S/H) and ramp generating circuit in a VDC circuit shown in FIG. **2**, FIG. **4** is a circuit diagram illustrating an example of a pulse generating circuit in a VDC circuit shown in FIG. **2**, and FIG. **5** is a diagram illustrating an example of a signal generated by a VDC circuit shown in FIG. **2**.

(24) Referring to FIG. **2**, a VTC circuit **110** according to some example embodiments may include an S/H and ramp generating circuit **111** and a pulse generating circuit **112**.

(25) The S/H and ramp generating circuit **111** may sample a positive input voltage Vinn and hold the sampled voltage at a predetermined (or alternatively, desired) point in time. Similarly, the S/H and ramp generating circuit **111** may sample a negative input voltage Vinp and hold the sampled voltage at a predetermined (or alternatively, desired) point in time. In some example embodiments, as shown in FIG. **3** and FIG. **5**, the S/H and ramp generating circuit **111** may close a switch SW in response to an ON level of a sampling control signal SC to sample an input voltage Vin to a

capacitor Cs. In addition, the S/H and ramp generating circuit **111** may hold a voltage Vout sampled in the capacitor Cs by opening the switch SW in response to an OFF level of the sampling control signal SC. In FIG. **3**, the input voltage Vin may be the positive input voltage Vinp or the negative input voltage Vinn shown in FIG. **2**, and the sampled voltage Vout may be a positive voltage Voutp or a negative voltage Voutn shown in FIG. **5**.

(26) The S/H and ramp generating circuit **111** may increase the voltage Voutp obtained from sampling the positive input voltage Vinp in a ramp form, and increase the voltage Voutn obtained from sampling the negative input voltage Vinn in a ramp form as well. In some example embodiments, as shown in FIG. **4** and FIG. **5**, the S/H and ramp generating circuit **111** may inject a current Ir into the capacitor Cs to increase the voltage Vout sampled in the capacitor Cs in the ramp form. In FIG. **4**, the voltage Vout may be the positive voltage Voutp or the negative voltage Voutn shown in FIG. **5**.

(27) The pulse generating circuit **112** may generate a pulse Tinp having a predetermined (or alternatively, desired) level (or a first level) from a point in time at which the voltage Voutp, which increases in the ramp form, becomes a predetermined (or alternatively, desired) voltage Vt, and the voltage Voutp increases in a ramp form, and generate a pulse Tinn having the predetermined (or alternatively, desired) level from a point in time at which the voltage Voutn becomes the predetermined (or alternatively, desired) voltage Vt. The predetermined (or alternatively, desired) level may be, for example, a high level. In this case, the pulses Tinp and Tinn may be switched from a low level to the high level at the point in time when the voltages Voutp and Voutn, which increase in the ramp form, become the predetermined (or alternatively, desired) voltage Vt. In FIG. **5**, since the positive input voltage Vinp is higher than the negative input voltage Vinn, a start edge (e.g., a rising edge) of the pulse Vinp generated based on the positive input voltage Vinp may be earlier than a start edge (e.g., a rising edge) of the pulse Vinn generated based on the negative input voltage Vinn. Next, the pulse generating circuit **112** may reset the voltages Vinp and Vinn increasing in the ramp form at appropriate timings. When the voltages Vinp and Vinn fall below the predetermined (or alternatively, desired) voltage Vt, the pulses Tinp and Tinn may be switched to the low level (or a second level). Accordingly, the pulse generating circuit **112** may generate the pulses Tinp and Tinn in the time domain. In this case, the time difference between the start edge of the pulse Tinp and the start edge of the pulse Tinn may be determined based on the voltage difference between the input voltage Vinp and the input voltage Vinn.

(28) FIG. **6** is a block diagram illustrating an example of a TDC circuit of an analog-to-digital converter according to some example embodiments, and FIG. **7** is a diagram illustrating an example of a signal generated by a TDC circuit shown in FIG. **6**.

(29) Referring to FIG. **6**, a TDC circuit **600** according to some example embodiments may include a plurality of stages **610**.sub.0, **610**.sub.1, **610**.sub.2, and **610**.sub.3, and one or more clock generating circuits **620**.sub.1, **620**.sub.2, and **620**.sub.3. Although FIG. **6** shows four stages **610**.sub.0 to **610**.sub.3 and three clock generating circuits **620**.sub.1 to **620**.sub.3, the number of stages **610**.sub.0 to **610**.sub.3 and the number of clock generating circuits **620**.sub.1 to **620**.sub.3 are not limited thereto. The stages **610**.sub.0 to **610**.sub.3 are in a sequence with one of the clock generating circuits **620**.sub.1 to **620**.sub.3 between each of the stages. The clock generating circuits **620**.sub.1 to **620**.sub.3 may also be in a sequence. A next stage may refer to a stage which receives input from a previous stage in the sequence. Restated a previous stage may provide an input to a next stage. For example, when the TDC circuit **600** decide n bits, the TDC circuit **600** may include n stages and (n−1) clock generating circuits.

(30) Each stage **610**.sub.i may receive a positive pulse Tinp.sub.i and a negative pulse Tinn.sub.i. Here, i is an integer between 0 and 3. Each stage **610**.sub.i may compare the positive pulse Tinp.sub.i and the negative pulse Tinn.sub.i in response to an input clock CLK.sub.i of a corresponding stage **610**.sub.i, and decide a bit D.sub.i of the corresponding stage **610**.sub.i based on a comparison result. In some example embodiments, each stage **610**.sub.i may compare a start

edge of the positive pulse Tinp.sub.i with a start edge of the negative pulse Tinn.sub.i, decide the bit D.sub.i as '1' if the start edge of the positive pulse Tinp.sub.i is earlier than the start edge of the negative pulse Tinn.sub.i, and decide the bit D.sub.i as '0' if the start edge of the negative pulse Tinn.sub.i is earlier than the start edge of the positive pulse Tinp.sub.i. When the TDC circuit **600** includes the four stages **610**.sub.0 to **610**.sub.3, the TDC circuit **600** may decide four bits D.sub.0 to D.sub.3. In this case, among the four bits, the first stage **610**.sub.0 (or start stage) may decide the most significant bit D.sub.0 the second stage **610**.sub.1 may decide the second most significant bit D.sub.1, the third stage **610**.sub.2 may decide the third most significant bit D.sub.2, and the fourth stage **610**.sub.3 may decide the least significant bit D.sub.3. The start stage does not have a previous stage in the sequence of stages.

(31) Each stage **610**.sub.i may output input pulses Tinp.sub.i+1 and Tinn.sub.i+1 of a next stage **610**.sub.i+1 by delaying either the positive pulse Tinp.sub.i or the negative pulse Tinn.sub.i by a reference time of the corresponding stage **610**.sub.i based on the comparison result (e.g., the decided bit) and without delaying the other pulse by the reference time of the corresponding stage **610**.sub.i. In some example embodiments, the stage **610**.sub.i may delay two pulses Tinp.sub.i and Tinn.sub.i by a basic delay value, and then output the input pulses Tinp.sub.i+1 and Tinn.sub.i+1 of the next stage **610**.sub.i+1 by delaying one pulse by the reference time of the corresponding stage **610**.sub.i and without delaying the other pulse. For example, when the comparison result indicates that the start edge of the positive pulse Tinp.sub.i is earlier than the start edge of the negative pulse Tinn.sub.i (e.g., when the decided bit D.sub.i is '1'), the stage **610**.sub.i may output the pulse Tinp.sub.i+1 by delaying the positive pulse Tinp.sub.i by the reference time, and output the pulse Tinn.sub.i+1 without delaying the negative pulse Tinn.sub.i. When the comparison result indicates that the start edge of the negative pulse Tinn.sub.i is earlier than the start edge of the positive pulse Tinp.sub.i (e.g., when the decided bit D.sub.i is '0'), the stage **610**.sub.i may output the pulse Tinp.sub.i+1 without delaying the positive pulse Tinp.sub.i, and output the pulse Tinn.sub.i+1 by delaying the negative pulse Tinn.sub.i by the reference time. In this case, the first stage **610**.sub.0 may receive pulses input to the TDC circuit **600** (e.g., output pulses Tinp and Tinn of the VTC circuit shown in FIG. **2**) as the input pulses Tinp.sub.0 and Tinn.sub.0. Further, since the last stage **610**.sub.3 does not have a next stage, the last stage **610**.sub.3 may not delay the input pulses Tinp.sub.3 and Tinn.sub.3.

(32) The TDC circuit **600** may use a binary search. Accordingly, each stage **610**.sub.i+1 may use half of the reference time of the previous stage **610**.sub.i as its own reference time. In this case, the first stage **610**.sub.0 may use half of a reference time Tref of the TDC circuit **600** as its own reference time Tref/2. Accordingly, the second stage **610**.sub.1 may use Tref/4 as its own reference time, and the third stage **610**.sub.1 may use Tref/8 as its own reference time.

(33) The first stage **610**.sub.0 may receive an input clock CLK.sub.0 of the TDC circuit **600** as its own clock and decide the bit D.sub.0 of the corresponding stage **610**.sub.0 in response to the input clock CLK.sub.0. Each (or alternatively, at least one) of stages **610**.sub.i other than the first stage **610**.sub.0 may decide the bit D.sub.i of the corresponding stage **610**.sub.i in response to a clock CLK.sub.i generated by the corresponding clock generating circuit **620**.sub.i. Here, i is an integer between 1 and 3. The clock generating circuit **620**.sub.i may generate the clock CLK.sub.i of the corresponding stage **620**.sub.i in response to an operation of the previous stage **620**.sub.i−1. In some example embodiments, the clock generating circuit **620**.sub.i may generate a start edge (e.g., a rising edge) of the clock CLK.sub.i of the corresponding stage **620**.sub.i in response to the operation of the previous stage **620**.sub.i−1. In some example embodiments, the clock generating circuit **620**.sub.i may reset the clock CLK.sub.i of the corresponding stage **620**.sub.i in response to an operation of the corresponding stage **620**.sub.i. In some other example embodiments, the clock generating circuit **620**.sub.i may reset the clock CLK.sub.i of the corresponding stage **620**.sub.i when the clock CLK.sub.i+1 is generated in the next clock generating circuit **620**.sub.i+1. In some example embodiments, the clock generating circuit **620**.sub.i may reset the clock CLK.sub.i by

generating an end edge (e.g., a falling edge) of the clock CLK.sub.i of the corresponding stage **620**.sub.i.

(34) In some example embodiments, the operation of the stage **620**.sub.i may be a comparison operation in the stage **620**.sub.i. In this case, the clock generating circuit **620**.sub.i may generate the clock CLK.sub.i of the corresponding stage **620**.sub.i in response to the comparison result (e.g., the decision result) of the previous stage **620**.sub.i−1. The clock generating circuit **620**.sub.i may reset the clock CLK.sub.i of the corresponding stage **620**.sub.i in response to the comparison result (e.g., the decision result) of the corresponding stage **620**.sub.i.

(35) In some example embodiments, when the clock CLK.sub.i of the stage **620**.sub.i is reset, the comparison result of the corresponding stage **620**.sub.i may be reset for the next operation.

(36) As shown in FIG. **7**, for example, a positive pulse Tinp.sub.0 and a negative pulse Tinn**0** later than the positive pulse Tinp.sub.0 may be input to the first stage **610**.sub.0. When the input clock CLK.sub.0 has an active level (e.g., a high level as a logic level) by a start edge (e.g., a rising edge) of the input clock CLK.sub.0. the first stage **610**.sub.0 may compare the positive pulse Tinp.sub.0 and the negative pulse Tinn.sub.0. In an example shown in FIG. **7**, because the positive pulse Tinp.sub.0 is earlier than the negative pulse Tinn.sub.0, the first stage **610**.sub.0 may decide '1' based on a comparison result. Further, because the positive pulse Tinp.sub.0 is earlier than the negative pulse Tinn.sub.0, the first stage **610**.sub.0 may output an input pulse Tinp.sub.1 of the second stage **610**.sub.1 by delaying the positive pulse Tinp.sub.0 by half Tref/2 of the reference time Tref of the TDC circuit **600**, and output an input pulse Tinn.sub.1 of the second stage **610**.sub.1 without delaying the negative pulse Tinn.sub.0 by half Tref/2 of the reference time Tref. The first clock generating circuit **620**.sub.1 may activate a clock CLK.sub.1 when the comparison is completed in the stage **610**.sub.0 (e.g., when the comparison result is generated in the stage **610**.sub.0). The first clock generating circuit **620**.sub.1 may activate the clock CLK.sub.1 by generating a start edge (e.g., a rising edge) of the clock CLK.sub.1.

(37) When the clock CLK.sub.1 output from the clock generating circuit **620**.sub.1 has the active level, the second stage **610**.sub.1 may compare the positive pulse Tinp.sub.1 and the negative pulse Tinn.sub.1 input from the first stage **610**.sub.0. In the example shown in FIG. **7**, because the positive pulse Tinp.sub.1 is earlier than the negative pulse Tinn.sub.1, the second stage **610**.sub.1 may decide '1' based on a comparison result. Further, because the positive pulse Tinp.sub.1 is earlier than the negative pulse Tinn.sub.1, the second stage **610**.sub.1 may output an input pulse Tinp.sub.2 of the third stage **610**.sub.2 by delaying the positive pulse Tinp.sub.1 by half Tref/4 of the reference time Tref/2 of the previous stage **610**.sub.0, and output an input pulse Tinn.sub.2 of the third stage **610**.sub.2 without delaying the negative pulse Tinn.sub.1 by half Tref/4 of the reference time Tref/2. The first clock generating circuit **620**.sub.1 may deactivate the clock CLK.sub.1 when the comparison is completed in the stage **610**.sub.1. The first clock generating circuit **620**.sub.1 may deactivate the clock CLK.sub.1 by generating an end edge (e.g., a falling edge) of the clock CLK.sub.1. Further, the second clock generating circuit **620**.sub.2 may activate a clock CLK.sub.2 when the comparison is completed in the stage **610**.sub.1.

(38) When the clock CLK.sub.2 output from the clock generating circuit **620**.sub.2 has the active level, the third stage **610**.sub.2 may compare the positive pulse Tinp.sub.2 and the negative pulses Tinn.sub.2 input from the second stage **610**.sub.1. In the example shown in FIG. **7**, because the positive pulse Tinp.sub.2 is earlier than the negative pulse Tinn.sub.2, the third stage **610**.sub.2 may decide '1' based on a comparison result. Further, because the positive pulse Tinp.sub.2 is earlier than the negative pulse Tinn.sub.2, the third stage **610**.sub.2 may output an input pulse Tinp.sub.3 of the fourth stage **610**.sub.3 by delaying the positive pulse Tinp.sub.2 by half Tref/8 of the reference time Tref/4 of the previous stage **610**.sub.1, and output an input pulse Tinn.sub.3 of the fourth stage **610**.sub.3 without delaying the negative pulse Tinn.sub.2 by half Tref/8 of the reference time Tref/4. The second clock generating circuit **620**.sub.2 may deactivate the clock CLK.sub.2 when the comparison is completed in the stage **610**.sub.2. Further, the third clock

generating circuit **620**.sub.3 may activate a clock CLK.sub.3 when the comparison is completed in the stage **610**.sub.2.
(39) When the clock CLK.sub.2 output from the clock generating circuit **620**.sub.2 has the active level, the fourth stage **610**.sub.3 may compare the positive pulse Tinp.sub.3 and negative pulse Tinn.sub.3 input from the third stage **610**.sub.2. In the example shown in FIG. **7**, because the negative pulse Tinn.sub.3 is earlier than the positive pulse Tinp.sub.3, the fourth stage **610**.sub.3 may decide '0' based on a comparison result. The third clock generating circuit **620**.sub.3 may deactivate the clock CLK.sub.3 when the comparison is completed in the stage **610**.sub.3.
(40) Through the above-described processes, the TDC circuit **600** may convert the input voltage into a digital signal D.sub.0 to D.sub.3 having "1110".
(41) If each stage **610**.sub.i does not use its own clock CLK.sub.i and the plurality of stages **610**.sub.0 to **610**.sub.3 use the same clock, the clock should maintain the active level until the input pulse is propagated through the plurality of stages **610**.sub.0 to **610**.sub.3. Therefore, because each stage **610**.sub.i may operate again in the next clock cycle after the decision at the plurality of stages **610**.sub.0 to **610**.sub.3 is completed, a waiting time of the stage **610**.sub.i may increase. However, according to the above-described example embodiments, each stage **610**.sub.i may operate in response to its own clock CLK.sub.i without waiting for the completion of the decision at the other stages, so that the waiting time may be reduced. That is, a pipelined successive-approximation TDC circuit may be provided.
(42) Further, a method of generating a clock of a next stage by delaying the input clock CLK.sub.0 may be used. This method may increase power consumption in a delay line for delaying the clock, and reset the comparator of the stage before the comparison is completed. However, since the pipelined successive-approximation TDC circuit described above does not use the delay line, power consumption can be reduced. Further, since a decision of a stage is completed and then a next stage operates in response to the clock, the comparator may not be reset before the operation is completed.
(43) FIG. **8** is a block diagram illustrating an example of a stage in a TDC circuit of an analog-to-digital converter according to some example embodiments, and FIG. **9** is a diagram illustrating an example of a clock generating circuit in a TDC circuit of an analog-to-digital converter according to some example embodiments.
(44) Referring to FIG. **8**, a stage **800** may include a time comparator **810**, and delay circuits **820** and **830**.
(45) The time comparator **810** may compare an input positive pulse Tinp.sub.i and an input negative pulse Tinn.sub.i. The time comparator **810** may compare a time of a start edge of the positive pulse Tinp.sub.i and a time of a start edge of the negative pulse Tinn.sub.i, and output a comparison result CMP.sub.i. In some example embodiments, an output of the time comparator **810** may include the output CMP.sub.i and a complementary output CMPb.sub.i having a complementary value of the output. In some example embodiments, the time comparator **810** may output '1' as the output CMP.sub.i when the start edge of the positive pulse Tinp.sub.i is earlier than the start edge of the negative pulse Tinp.sub.i, and output '0' as the output CMP.sub.i when the start edge of the positive pulse Tinp.sub.i is later slower than the start edge of the negative pulse Tinn.sub.i. The time comparator **810** may output '0' as the complementary output CMPb.sub.i when outputting '1' as the output CMP.sub.i, and output '1' as the complementary output CMPb.sub.i when outputting '0' as the output CMP.sub.i. The output CMP.sub.i of the time comparator **810** may be a decision value of the stage **800**.
(46) The delay circuit **820** may receive the positive pulse Tinp.sub.i and operate in response to the output CMP.sub.i of the time comparator **810**. When the output CMP.sub.i of the time comparator **810** has a first value (e.g., '1'), the delay circuit **820** may output an input pulse Tinp.sub.i+1 of a next stage by delaying the positive pulse Tinp.sub.i by a reference time Tref/2.sup.i+1 of the stage **800**. When the output CMP.sub.i of the time comparator **810** has a second value (e.g., '0'), the

delay circuit **820** may output the input pulse Tinp.sub.i+1 of the next stage without delaying the positive pulse Tinp.sub.i by the reference time Tref/2.sup.i+1 of the stage **800**. In some example embodiments, the delay circuit **820** may include a delay circuit that operates in response to the output CMP.sub.i of the time comparator **810** and delays an input by the reference time Tref/2.sup.i+1, and a delay circuit **822** that operates in response to the complementary output CMPb.sub.i of the time comparator **810** and does not delays an input by the reference time Tref/2.sup.i+1.

(47) The delay circuit **830** may receive the negative pulse Tinn.sub.i and operate in response to the output CMP.sub.i of the time comparator **810**. When the output CMP.sub.i of the time comparator **810** has the second value, the delay circuit **830** may output an input pulse Tinn.sub.i+1 of the next stage by delaying the negative pulse Tinn.sub.i by the reference time Tref/2.sup.i+1 of the stage **800**. When the output CMP.sub.i of the time comparator **810** has the first value, the delay circuit **820** may output the input pulse Tinn.sub.i+1 of the next stage without delaying the negative pulse Tinn.sub.i by the reference time Tref/2.sup.i+1 of the stage **800**. In some example embodiments, the delay circuit **830** may include a delay circuit that operates in response to the complementary output CMP.sub.i of the time comparator **810** and delays an input by the reference time Tref/2.sup.i+1, and a delay circuit **832** that operates in response to the output CMP.sub.i of the time comparator **810** and does not delay an input by the reference time Tref/2.sup.i+1.

(48) In some example embodiments, the delay circuits **820** and **830** may delay the pulses Tinp.sub.i and Tinn.sub.i by a basic delay value, respectively.

(49) Referring to FIG. **9**, a clock generating circuit **900** may include a logic circuit **910** and a clock control circuit **920**, and may receive a comparison result of a previous stage.

(50) The logic circuit **910** may output a signal having a predetermined (or alternatively, desired) level when a comparison between a positive pulse and a negative pulse is completed in the previous stage. In some example embodiments, when the comparison in the previous stage is completed, either one of an output CMP.sub.i−1 and a complementary output CMPb.sub.i−1 may have ‘1’ and the other may have ‘0’ in a time comparator of the previous stage. Accordingly, the logic circuit **910** may be an exclusive OR (XOR) gate **910**. The XOR gate **910** may receive the output CMP.sub.i−1 and the complementary output CMPb.sub.i−1 in the time comparator of the previous stage, and output a signal having ‘1’ when the comparison is completed.

(51) The clock control circuit **920** may generate a clock CLK.sub.i of a corresponding stage when the output of the logic circuit **910** has the predetermined (or alternatively, desired) level (e.g., action level, or action value) (e.g., the action value may be a high level (‘1’) as a logic level). In some example embodiments, the clock control circuit **920** may generate the clock CLK.sub.i by generating a start edge of the clock CLK.sub.i of the corresponding stage.

(52) In some example embodiments, the clock control circuit **920** may further include a logic circuit **930** that outputs a signal having a predetermined (or alternatively, desired) level when a comparison between the positive pulse and the negative pulse is completed in the corresponding stage. The logic circuit **930** may be an XOR gate that receives an output CMP.sub.i and a complementary output CMPb.sub.i in a time comparator of the corresponding stage. Accordingly, the clock control circuit **920** may transfer a clock reset signal CLK_RST to the corresponding stage to reset the clock CLK.sub.i when an output of the logic circuit **930** has the predetermined (or alternatively, desired) level (e.g., the high level (‘1’) as a logic level).

(53) In some other example embodiments, when the output of the logic circuit **910** has the predetermined (or alternatively, desired) level, the clock control circuit **920** may transfer the clock reset signal CLK_RST to the clock control circuit **920** corresponding to the previous stage. The clock control circuit **920** corresponding to the previous stage may reset the clock CLK.sub.i−1 in response to the clock reset signal CLK_RST. In this case, the clock control circuit **920** may reset the clock CLK.sub.i in response to the clock reset signal CLK_RST transferred from the clock control circuit **920** corresponding to a next stage.

(54) In some example embodiments, when the clock CLK.sub.i of a stage is reset, a time comparator (e.g., **810** in FIG. **8**) of the corresponding stage may be reset for a next operation. When the time comparator **810** is reset, the time comparator **810** may output the same value (e.g., '0') as the output CMP.sub.i and the complementary output CMPb.sub.i.
(55) FIG. **10** is a block diagram illustrating an example of an analog-to-digital converter according to some example embodiments.
(56) Referring to FIG. **10**, an analog-to-digital converter **1000** may include a VTC circuit **1010**, a first TDC circuit **1020**, and a second TDC circuit **1030**. The analog-to-digital converter **1000** may convert analog input voltages Vinp and Vinn into a digital signal having a plurality of bits (e.g., eight bits). In this case, the analog-to-digital converter **1000** may perform a fine decision after performing a coarse decision.
(57) As described with reference to FIG. **1**, the VTC circuit **1010** may convert the input voltages Vinp and Vinn into time domain pulses Tinp and Tinn.
(58) The first TDC circuit **1020** may perform the coarse decision. The first TDC circuit **1020** may decide a predetermined (or alternatively, desired) number (e.g., three) of the most significant bits D.sub.0 to D.sub.2 among the eight bits from the input pulses Tinp and Tinn, and output a positive pulse Tinpr and a negative pulse Tinnr as a residual signal corresponding to remaining bits (e.g., the lower five bits) D.sub.3 to D.sub.7.
(59) The second TDC circuit **1030** may perform the fine decision. The second TDC circuit **1030** may receive the residual signal Tinpr and Tinnr output from the first TDC circuit **1020** as input pulses, and decide the five bits D.sub.3 to D.sub.7 from the input pulses Tinpr and Tinnr.
(60) In some example embodiments, both the first TDC circuit **1020** and the second TDC circuit **1030** may be implemented as a pipelined successive-approximation TDC described above.
(61) In some other example embodiments, the second TDC circuit **1030** may be implemented as the pipelined successive-approximation TDC, and the first TDC circuit **1020** may be implemented as a faster TDC than the pipelined successive-approximation TDC. For example, the first TDC circuit **1020** may be implemented as a flash TDC.
(62) FIG. **11** is a block diagram illustrating an example of a flash TDC circuit according to some example embodiments, and FIG. **12** is a diagram showing an example of a signal generated in a flash TDC circuit shown in FIG. **11**.
(63) Referring to FIG. **11**, a flash TDC circuit **1100** may include a plurality of time comparators **1110**.sub.1, **1110**.sub.2, **1110**.sub.3, **1110**.sub.4, **1110**.sub.5, **1110**.sub.6, and **1110**.sub.7, and a plurality of delay circuits **1120**.sub.1, **1120**.sub.2, **1120**.sub.3, **1120**.sub.4, **1120**.sub.5, and **1120**.sub.6. Although FIG. **11** shows seven time comparators **1110**.sub.1 to **1110**.sub.7 and six delay circuits **1120**.sub.1 to **1120**.sub.6, the number of time comparators **1110**.sub.1 to **1110**.sub.7 and the number of delay circuits **1120**.sub.1 to **1120**.sub.6 are not limited thereto. For example, if the flash TDC circuit **1100** decides n bits, the flash TDC circuit **1100** may include (2.sup.n−1) time comparators and (2.sup.n−2) delay circuits.
(64) Each (or alternatively, at least one) of the delay circuits **1120**.sub.1 to **1120**.sub.6 may delay an input pulse by a reference time. When the flash TDC circuit **1100** decides the n bits, the reference time may be ½.sup.n of a reference time Tref of the flash TDC circuit **1100**. In an example shown in FIG. **11** and FIG. **12**, the reference time may be Tref/4. The delay circuit **1120**.sub.1 may output a negative pulse Tinn by delaying an input negative pulse Tinn by the reference time Tref/4, the delay circuit **1120**.sub.2 may output a negative pulse Tinn.sub.2 by delaying the negative pulse Tinn.sub.1 output from delay circuit **1120**.sub.1 by the reference time Tref/4, and the delay circuit **1120**.sub.3 may output a negative pulse Tinn.sub.3 by delaying the negative pulse Tinn.sub.2 output from delay circuit **1120**.sub.2 by the reference time Tref/4. Accordingly, the negative pulse Tinn.sub.2 may be delayed by 2Tref/4 from the input negative pulse Tinn, and the negative pulse Tinn.sub.3 may be delayed by 3Tref/4 from the input negative pulse Tinn. The delay circuit **1120**.sub.4 may output a positive pulse Tinp.sub.1 by delaying an input positive pulse Tinp by the

reference time Tref/4, the delay circuit **1120**.sub.5 may output a positive pulse Tinp.sub.2 by delaying the positive pulse Tinp.sub.1 output from delay circuit **1120**.sub.4 by the reference time Tref/4, and the delay circuit **1120**.sub.6 may output a positive pulse Tinp.sub.3 by delaying the positive pulse Tinp.sub.2 output from delay circuit **1120**.sub.5 by the reference time Tref/4. Accordingly, the positive pulse Tinp.sub.2 may be delayed by 2Tref/4 from the input positive pulse Tinp, and the positive pulse Tinp.sub.3 may be delayed by 3Tref/4 from the input positive pulse Tinp.

(65) Each (or alternatively, at least one) of the time comparators **1110**.sub.1 to **1110**.sub.7 may compare a positive pulse and a negative pulse, and decide a corresponding one among bits C.sub.0 to C.sub.6 based on a comparison result. In some example embodiments, the time comparators **1110**.sub.1 to **1110**.sub.7 may compare a start edge of the positive pulse with a start edge of the negative pulse, decide '1' if the start edge of the positive pulse is earlier than the start edge of the negative pulse, and decide '0' if the start edge of the negative pulse is earlier than the start edge of the positive pulse.

(66) The time comparators **1110**.sub.1 to **1110**.sub.4 may receive the input positive pulse Tinp as the positive pulse, and the time comparators **1110**.sub.4 to **1110**.sub.7 may receive the input negative pulse Tinn as the negative pulse. The time comparator **1110**.sub.1 may receive the negative pulse Tinn.sub.3 output from the delay circuit **1120**.sub.3 as the negative pulse, the time comparator **1110**.sub.2 may receive the negative pulse Tinn.sub.2 output from the delay circuit **1120**.sub.2 as the negative pulse, and the time comparator **1110**.sub.3 may receive the negative pulse Tinn.sub.1 output from the delay circuit **1120**.sub.1 as the negative pulse. The time comparator **1110**.sub.5 may receive the positive pulse Tinp.sub.1 output from the delay circuit **1120**.sub.4 as the positive pulse, the time comparator **1110**.sub.6 may receive the positive pulse Tinp.sub.2 output from the delay circuit **1120**.sub.5 as the positive pulse, and the time comparator **1110**.sub.7 may receive the positive pulse Tinp.sub.3 output from the delay circuit **1120**.sub.6 as the positive pulse.

(67) As shown in FIG. **12**, for example, the input positive pulse Tinp and the input negative pulse Tinn may be input to the TDC circuit **1200**, and the input negative pulse Tinn may be later than the input positive pulse Tinp by a time longer than 2Tref/4 and shorter than 3Tref/4. Then, because the input positive pulse Tinp is earlier than the negative pulse Tinn.sub.3 delayed by 3Tref/4 from the input negative pulse Tinn, the time comparator **1110**.sub.1 may decide the bit C.sub.0 as '1'. Because the input positive pulse Tinp is earlier than the negative pulse Tinn.sub.2 delayed by 2Tref/4 from the input negative pulse Tinn, the time comparator **1110**.sub.2 may also decide the bit C.sub.1 as '1'. Because the input positive pulse Tinp is earlier than the negative pulse Tinn.sub.2 delayed by Tref/4 from the input negative pulse Tinn, the time comparator **1110**.sub.3 may also decide the bit C.sub.2 as '1'. Because the input positive pulse Tinp is earlier than the input negative pulse Tinn, the time comparator **1110**.sub.4 may also decide the bit C.sub.3 as '1'. Because the positive pulse Tinp.sub.1 delayed by Tref/4 from the input positive pulse Tinp is earlier than the input negative pulse Tinn, the time comparator **1110**.sub.5 may also decide the bit C.sub.4 as '1'. Because the positive pulse Tinp.sub.1 delayed by 2Tref/4 from the input positive pulse Tinp is earlier than the input negative pulse Tinn, the time comparator **1110**.sub.6 may also decide the bit C.sub.5 as '1'. Because the positive pulse Tinp.sub.1 delayed by 3Tref/4 from the input positive pulse Tinp is later than the input negative pulse Tinn, the time comparator **1110**.sub.7 may decide the bit C.sub.6 as '0'.

(68) Therefore, the flash TDC circuit **1100** may output a decision code C.sub.0 to C.sub.6 of "1111110". The decision code C.sub.0 to C.sub.6 of "1111110" may be a thermometer code, and may correspond to "110" in a binary digital code. Since the flash TDC circuit **1100** may output all digital values in one clock cycle, it may operate faster than a pipelined successive-approximation TDC circuit.

(69) As described above, in some example embodiments, when the flash TDC circuit is used as the

first TDC circuit **1020** in FIG. **10**, the analog-to-digital converter may operate faster. In some example embodiments, when the pipelined successive-approximation TDC circuit is used as the first TDC circuit **1020** in FIG. **10**, the number of time comparators may be reduced. For example, for n-bit decision, n time comparators may be used in the pipelined successive-approximation TDC circuit, whereas (2.sup.n−1) time comparators may be used in the flash TDC circuit.

(70) FIG. **13** is a flowchart illustrating an example of an analog-to-digital converting method according to some example embodiments.

(71) Referring to FIG. **13**, an analog-to-digital converter may receive the i.sup.th positive pulse and the i.sup.th negative pulse at the i.sup.th stage in S**1310**. In some example embodiments, the first positive pulse and the first negative pulse of the first stage may be pulses generated by converting an input voltage into a time domain. In some example embodiments, the first positive pulse and the first negative pulse may be pulses that is remained after some bits (or alternatively, at least one bit) are decided from the pulses generated by converting the input voltage into the time domain.

(72) In the i.sup.th stage, the analog-to-digital converter may generate the i.sup.th comparison result by comparing the i.sup.th positive pulse and the i.sup.th negative pulse in response to the i.sup.th clock in S**1320**. The analog-to-digital converter may decide the i.sup.th bit based on the i.sup.th comparison result in S**1330**. When the i.sup.th stage is the last stage (e.g., the n.sup.th stage) in S**1340**, the analog-to-digital converter may end the decision.

(73) When the i.sup.th stage is not the last stage in S**1340**, the analog-to-digital converter may output the (i+1).sup.th positive pulse and the (i+1).sup.th negative pulse by delaying either one of the i.sup.th positive pulse and the i.sup.th negative pulse by the i.sup.th reference time based on a value of the i.sup.th comparison result in S**1350**, S**1360**, and S**1370**. Further, the analog-to-digital converter may generate the (i+1).sup.th clock in response to the i.sup.th comparison result in S**1380**. In some example embodiments, the analog-to-digital converter may generate a first value (e.g., ‘1’) as the i.sup.th comparison result if the i.sup.th positive pulse is earlier than the i.sup.th negative pulse, and generate a second value (e.g., ‘0’) different from the first value as the i.sup.th comparison result if the i.sup.th negative pulse is earlier than the i.sup.th positive pulse. In some example embodiments, when the i.sup.th comparison result has the first value in S**1350**, the analog-to-digital converter may delay the i.sup.th positive pulse by the i.sup.th reference time in S**1360**. When the i.sup.th comparison result has the second value in S**1350**, the analog-to-digital converter may delay the i.sup.th negative pulse by the i.sup.th reference time in S**1370**.

(74) Next, the analog-to-digital converter may perform a decision at the (i+1).sup.th stage in S**1390**.

(75) FIG. **14** is a block diagram illustrating an example of a computing device according to some example embodiments.

(76) Referring to FIG. **14**, a computing device **1400** may include a host system **1410** and a memory system **1420**. The host system **1410** and the memory system **1420** may communicate through an interface. The memory system **1420** may include a memory controller **1421** and a memory device **1422**.

(77) The memory controller **1421** may control a memory operation of the memory device **1422** by providing a signal to the memory device **1422** in response to a request from the host system **1410**. The signal may include a command and an address. The memory controller **1421** may read data from the memory device **1422** by providing a read signal to the memory device **1422**. Further, the memory controller **1421** may write data into the memory device **1422** by providing a write signal and the data to the memory device **1422**.

(78) In some example embodiments, the memory device **1422** may include a volatile memory such as a dynamic random-access memory (DRAM). In some example embodiments, the memory device **1422** may include a non-volatile memory such as a flash memory, a phase-change memory, a resistive memory, a magnetoresistive memory, a ferroelectric memory, or a polymer memory. In some example embodiments, the memory device **1422** may be used as a system memory of host

system **1410**. In this case, the memory controller **1421** may be provided as a separate chip from a processor of the host system **1410**, or may be provided as an internal component of the processor. In some example embodiments, the memory system **1420** may be used as a storage device for the host system **1410**.

(79) An analog-to-digital converter described with reference to FIG. **1** to FIG. **13** may be included in the host system **1410**, the memory controller **1421**, and/or the memory device **1422** to convert an analog voltage into a digital signal.

(80) FIG. **15** is a block diagram illustrating an example of a communication system according to some example embodiments.

(81) Referring to FIG. **15**, a communication system **1500** may include a first device **1510** and a second device **1520**.

(82) The first device **1510** may include a transmitter **1511**, a receiver **1512**, and a processor **1513**, and the second device **1520** may include a transmitter **1521**, a receiver **1522**, and a processor **1523**. The transmitter **1511** of the first device **1510** may transmit data to the second device **1520**, and the receiver **1522** of the second device **1520** may receive the data. Similarly, the transmitter **1521** of the second device **1520** may transmit data to the first device **1510**, and the receiver **1512** of the first device **1510** may receive the data. The processor **1513** may control operations of the transmitter **1511** and the receiver **1512**, and the processor **1523** may control operations of the transmitter **1521** and the receiver **1522**.

(83) An analog-to-digital converter described with reference to FIG. **1** to FIG. **13** may be included in the transmitter **1511**, the receiver **1512**, the transmitter **1521**, and/or the receiver **1522** to convert an analog voltage into a digital signal.

(84) Although FIG. **14** and FIG. **15** shows the computing device and the communication system in which the analog-to-digital converter is used, a system or device to which the analog-to-digital converter is used is not limited thereto. The analog-to-digital converter may be used to convert an analog voltage to a digital signal in a variety of devices.

(85) In some example embodiments, each (or alternatively, at least one) of the components, elements, modules, or units represented by a block as illustrated in FIG. **1** to FIG. **12** may be implemented as various numbers of hardware, software, and/or firmware structures that execute respective functions described above, according to some example embodiments. For example, at least one of these components, elements, modules, or units may include various hardware components including a digital circuit, a programmable or non-programmable logic device or array, an application specific integrated circuit (ASIC), or other circuitry using a digital circuit structure, such as a memory, a processor, a logic circuit, a look-up table, etc., that may execute the respective functions through controls of one or more microprocessors or other control apparatuses. Further, at least one of these components, elements, modules, or units may include a module, a program, or a part of code, which contains one or more executable instructions for performing specified logic functions, and executed by one or more microprocessors or other control apparatuses. Furthermore, at least one of these components, elements, modules, or units may further include or may be implemented by a processor that performs the respective functions. Functional aspects of example embodiments may be implemented in algorithms that execute on one or more processors.

(86) Any of the elements and/or functional blocks disclosed above may include or be implemented in processing circuitry such as hardware including logic circuits; a hardware/software combination such as a processor executing software; or a combination thereof. For example, the clock control circuit **920** and memory controller **1421** may be implemented as processing circuitry. The processing circuitry specifically may include, but is not limited to, a central processing unit (CPU), an arithmetic logic unit (ALU), a digital signal processor, a microcomputer, a field programmable gate array (FPGA), a System-on-Chip (SoC), a programmable logic unit, a microprocessor, application-specific integrated circuit (ASIC), etc. The processing circuitry may include electrical components such as at least one of transistors, resistors, capacitors, etc. The processing circuitry

may include electrical components such as logic gates including at least one of AND gates, OR gates, NAND gates, NOT gates, etc.
(87) Processor(s), controller(s), and/or processing circuitry may be configured to perform actions or steps by being specifically programmed to perform those action or steps (such as with an FPGA or ASIC) or may be configured to perform actions or steps by executing instructions received from a memory, or a combination thereof.
(88) While this invention has been described in connection with what is presently considered to be practical example embodiments, it is to be understood that the invention is not limited to the disclosed example embodiments. On the contrary, it is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

Claims

1. An analog-to-digital converter comprising: a plurality of stages configured in a sequence to sequentially decide a plurality of bits in successive-approximation, each of the plurality of stages configured to operate in response to a corresponding clock among a plurality of clocks, and decide a corresponding bit among the plurality of bits from a corresponding positive pulse among a plurality of positive pulses and a corresponding negative pulse among a plurality of negative pulses, the plurality of positive pulses respectively input to the plurality of stages and the plurality of negative pulses respectively input to the plurality of stages; and a plurality of clock generating circuits respectively corresponding to a plurality of first stages among the plurality of stages, each of the plurality of clock generating circuits configured to generate the corresponding clock of a corresponding stage among the plurality of first stages based on an operation of a previous stage among the plurality of stages, the previous stage being before the corresponding stage in the sequence.
2. The analog-to-digital converter of claim 1, wherein each of the plurality of stages is further configured to compare the corresponding positive pulse and the corresponding negative pulse to decide the corresponding bit, and each of a plurality of second stages among the plurality of stages is configured to generate a positive pulse to be input to a next stage among the plurality of positive pulses and a negative pulse to be input to the next stage among the plurality of negative pulses, by delaying either one of the corresponding positive pulse and the corresponding negative pulse by a corresponding reference time among a plurality of references times respectively corresponding to the plurality of second stages, the plurality of second stages not including a last stage in the sequence among the plurality of stages, the next stage being a stage after the corresponding stage in the sequence, the last stage not having a next stage in the sequence.
3. The analog-to-digital converter of claim 2, wherein the operation of the previous stage comprises a comparison operation of a positive pulse input to the previous stage among the plurality of positive pulses and a negative pulse input to the previous stage among the plurality of negative pulses.
4. The analog-to-digital converter of claim 3, wherein each of the plurality of clock generating circuits is further configured to generate the corresponding clock of the corresponding stage in response to a result of the comparison operation in the previous stage.
5. The analog-to-digital converter of claim 3, wherein each of the plurality of clock generating circuits is further configured to reset the corresponding clock of the corresponding stage in response to a result of the comparison operation in the corresponding stage.
6. The analog-to-digital converter of claim 3, wherein each of the plurality of clock generating circuits is further configured to reset the corresponding clock of the corresponding stage in response to generation of a clock in a next clock generating circuit among the plurality of clock generating circuits.
7. The analog-to-digital converter of claim 2, wherein each of the plurality of second stages is

further configured to delay the corresponding positive pulse by the corresponding reference time when deciding the corresponding bit as a first value, or delay the corresponding negative pulse by the corresponding reference time when deciding the corresponding bit as a second value different from the first value.

8. The analog-to-digital converter of claim 2, wherein, the plurality of second stages include a start stage in the sequence and at least one third stage, the start stage in the sequence not having a previous stage in the sequence, the corresponding reference time of each of the at least one third stage is half of a reference time corresponding to the previous stage among the plurality of reference times.

9. The analog-to-digital converter of claim 1, wherein the plurality of first stages are stages not including a start stage among the plurality of stages in the sequence, the start stage in the sequence not having a previous stage in the sequence.

10. The analog-to-digital converter of claim 9, wherein the corresponding clock of the start stage is an input clock of the analog-to-digital converter.

11. The analog-to-digital converter of claim 1, further comprising a voltage-to-time converter circuit configured to convert a positive input voltage and a negative input voltage into a time domain to generate an input positive pulse and an input negative pulse to be input to a start stage among the plurality of stages in the sequence as the corresponding positive pulse and the corresponding negative pulse of the start stage, respectively, the start stage in the sequence not having a previous stage in the sequence.

12. The analog-to-digital converter of claim 1, further comprising: a voltage-to-time converter circuit configured to convert a positive input voltage and a negative input voltage into a time domain to generate an input positive pulse and an input negative pulse; and a time-to-digital converter circuit configured to decide at least one bit based on the input positive pulse and the input negative pulse, and then output a residual positive pulse and a residual negative pulse to be input to a start stage among the plurality of stages in the sequence as the corresponding positive pulse and the corresponding negative pulse, respectively, the start stage in the sequence not having a previous stage in the sequence.

13. An analog-to-digital converter comprising: a first time comparator configured to operate in response to a first clock, and decide a first bit based on a first comparison result of comparing a first positive pulse and a first negative pulse; a first delay circuit configured to delay either one of the first positive pulse and the first negative pulse by a first reference time based on a value of the first comparison result; a clock generating circuit configured to generate a second clock in response to the first comparison result; a second time comparator configured to operate in response to the second clock, and decide a second bit based on a second comparison result of comparing a second positive pulse and a second negative pulse output from the first delay circuit; and a second delay circuit configured to delay either one of the second positive pulse and the second negative pulse by a second reference time based on a value of the second comparison result.

14. The analog-to-digital converter of claim 13, wherein the clock generating circuit is further configured to reset the second clock in response to the second comparison result.

15. The analog-to-digital converter of claim 13, wherein the first time comparator is further configured to output a first value as the first comparison result in response to the first positive pulse being earlier than the first negative pulse, or output a second value different from the first value as the first comparison result in response to the first negative pulse being earlier than the first positive pulse, wherein the second time comparator is further configured to output the first value as the second comparison result in response to the second positive pulse being earlier than the second negative pulse, or output the second value different as the second comparison result in response to the second negative pulse being earlier than the second positive pulse.

16. The analog-to-digital converter of claim 15, wherein the first delay circuit is further configured to delay the first positive pulse by the first reference time in response to the first value of the first

comparison result, and delay the first negative pulse by the first reference time in response to the second value of the first comparison result, and wherein the second delay circuit is further configured to delay the second positive pulse by the second reference time in response to the first value of the second comparison result, and delay the second negative pulse by the second reference time in response to the second value of the second comparison result.

17. The analog-to-digital converter of claim 13, wherein the first time comparator is further configured to output a first complementary comparison result having a complementary value of the first comparison result, and wherein the clock generating circuit is further configured to generate the second clock in response to a result of a logical operation on the first comparison result and the first complementary comparison result having an action value.

18. The analog-to-digital converter of claim 17, wherein the logical operation is an exclusive OR operation, and wherein the action value is ‘1’.

19. The analog-to-digital converter of claim 17, wherein the second time comparator is further configured to output a second complementary comparison result having a complementary value of the second comparison result, and wherein the clock generating circuit is further configured to reset the second clock when a result of a logical operation on the second comparison result and the second complementary comparison result has the action value.

20. An analog-to-digital converting method comprising: receiving a first positive pulse and a first negative pulse; comparing the first positive pulse and the first negative pulse in response to a first clock to generate a first comparison result; deciding a first bit based on a value of the first comparison result; outputting a second positive pulse and a second negative pulse by delaying either one of the first positive pulse and the first negative pulse by a first reference time based on the value of the first comparison result; generating a second clock in response to the first comparison result; comparing the second positive pulse and the second negative pulse in response to the second clock to generate a second comparison result; and deciding a second bit based on a value of the second comparison result.