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Wang et al.

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(54) **METHOD FOR FABRICATING SEMICONDUCTOR STRUCTURE AND SEMICONDUCTOR STRUCTURE**

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CPC **H10N 50/80** (2023.02); **H10N 50/01** (2023.02)

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See application file for complete search history.

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Primary Examiner — Sue A Purvis

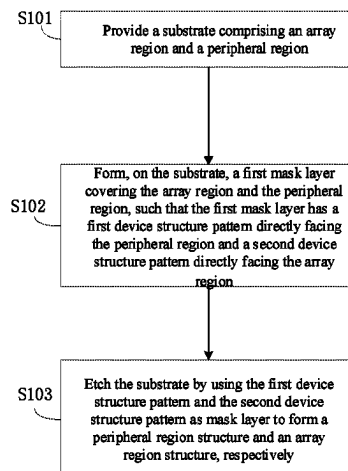
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(57) **ABSTRACT**

Embodiments relate to the field of semiconductor manufacturing technology, and more particularly, to a method for fabricating a semiconductor structure and a semiconductor structure. The fabricating method includes: providing a substrate including an array region and a peripheral region; and forming, on the substrate, a first mask layer covering the array region and the peripheral region, the first mask layer having a first device structure pattern directly facing the array region and a second device structure pattern directly facing the peripheral region. Through the method for fabricating a semiconductor structure, the first mask layer having

(Continued)



the first device structure pattern and the second device structure pattern is formed on the substrate, and then the substrate is etched by using the first device structure pattern and the second device structure pattern as mask layer to synchronously form a peripheral region structure and an array region structure on the substrate.

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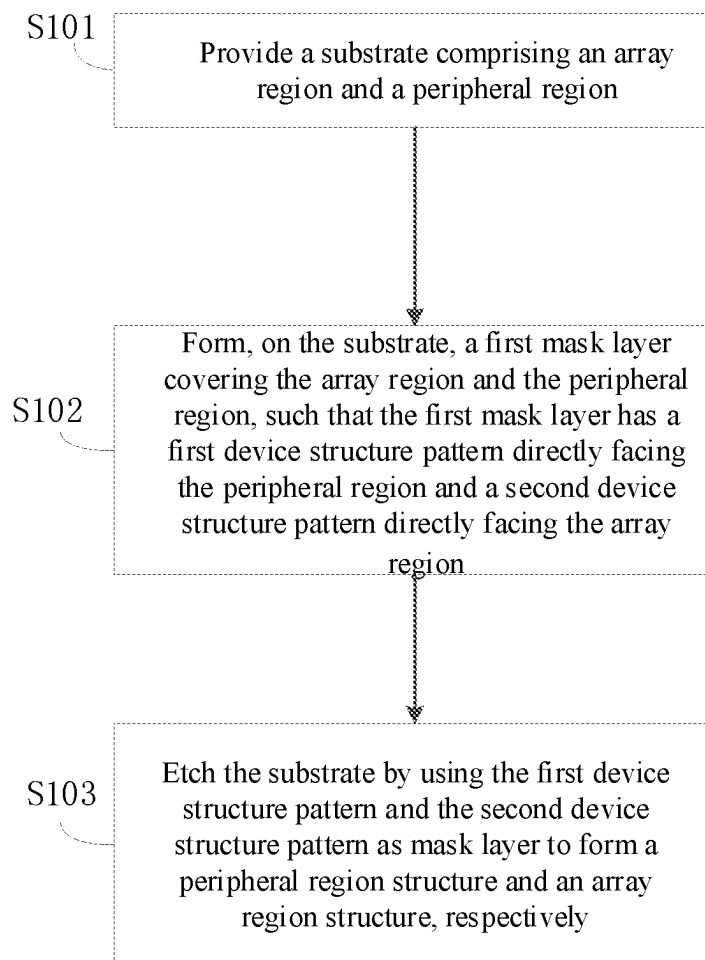


Fig. 1

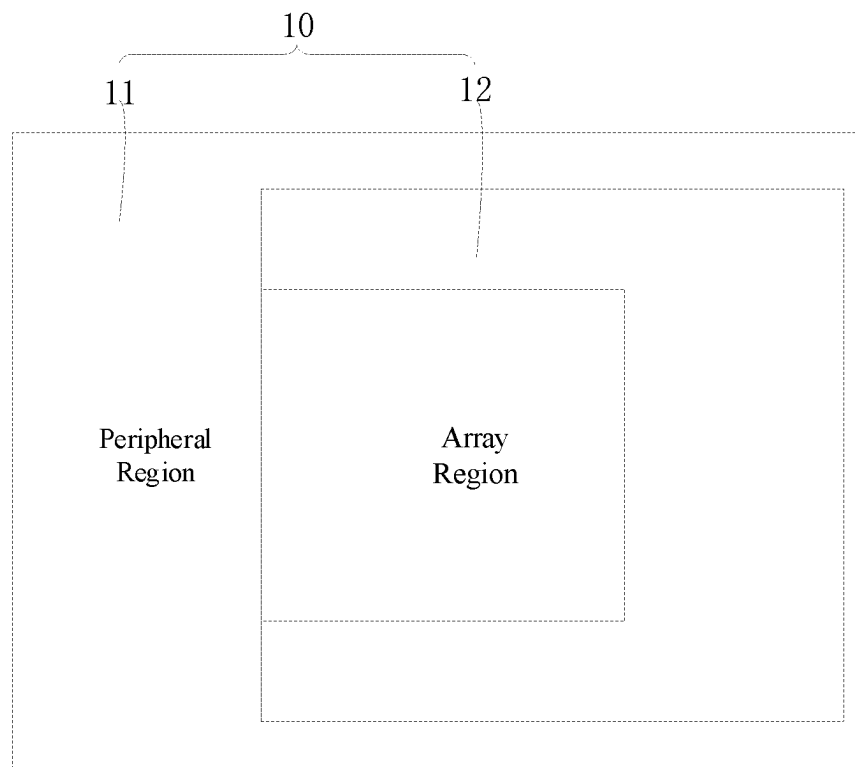


Fig. 2

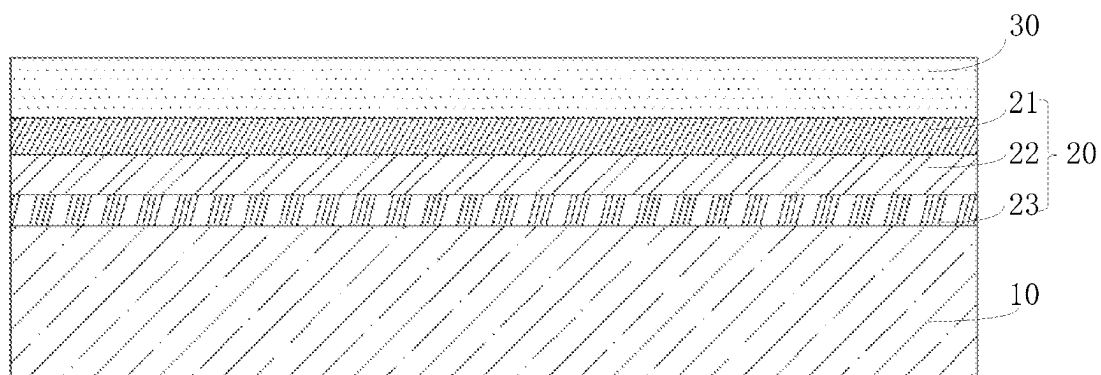


Fig. 3

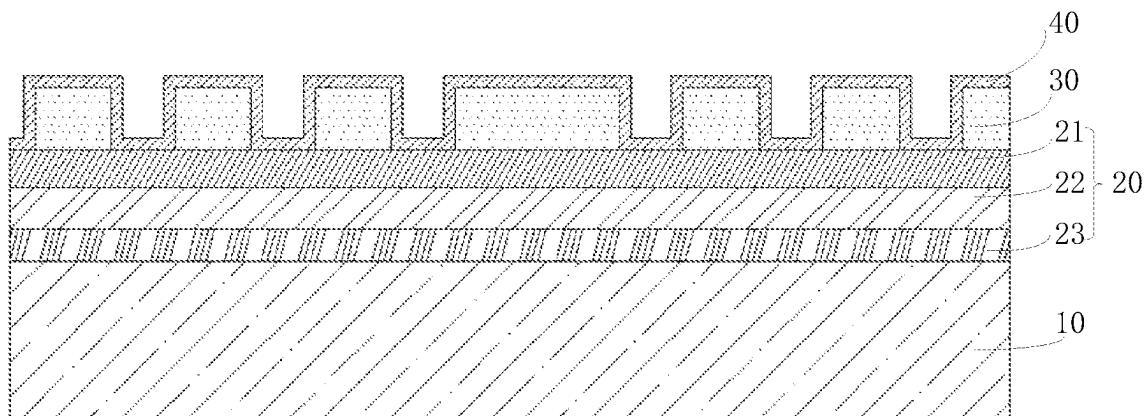


Fig. 4

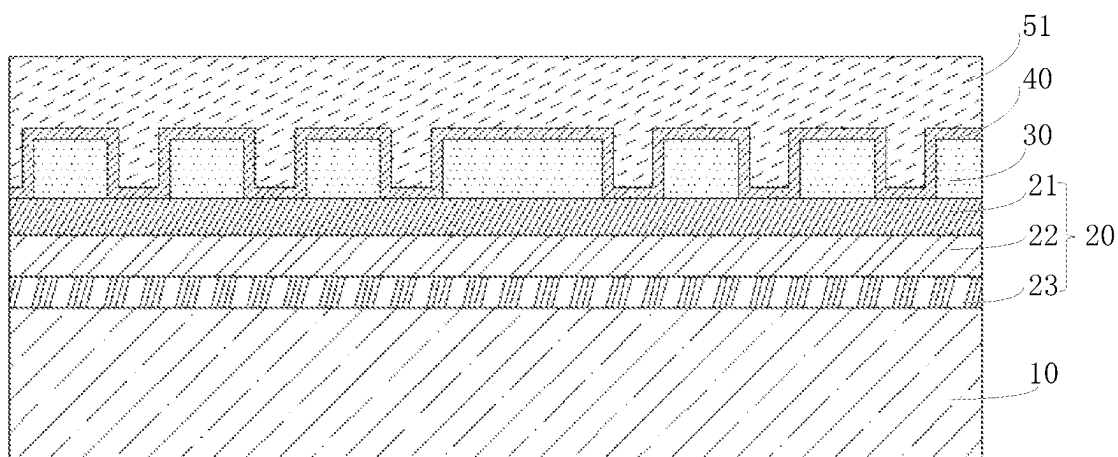


Fig. 5

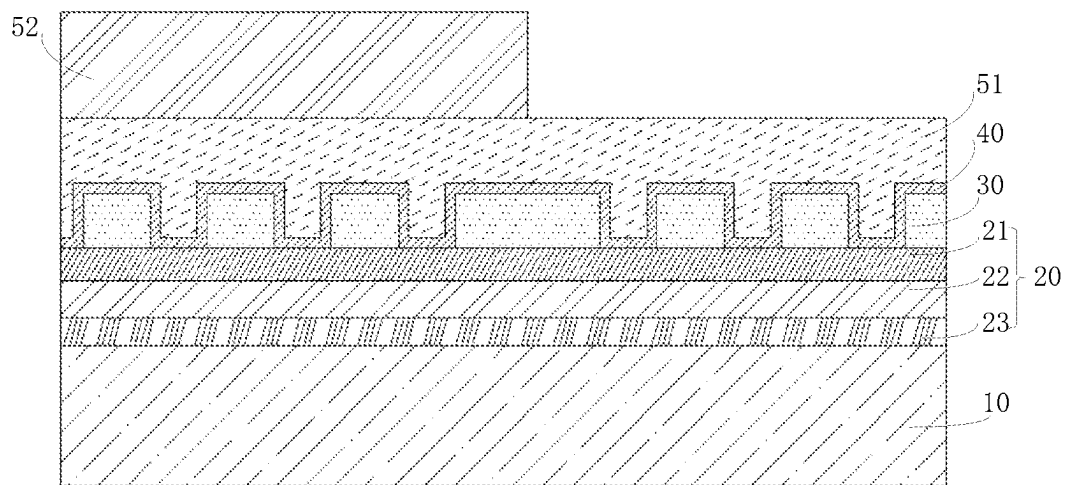


Fig. 6

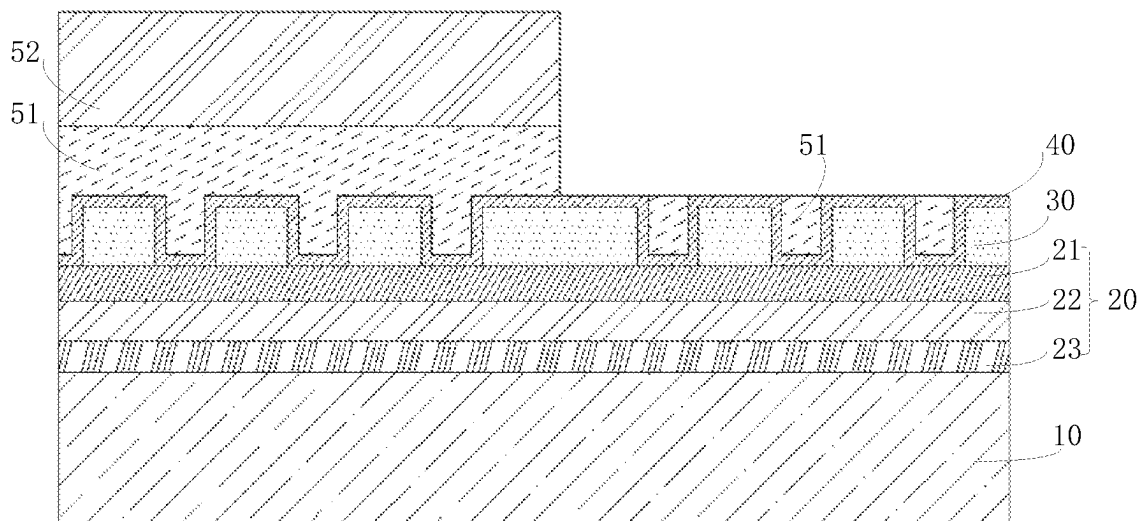


Fig. 7

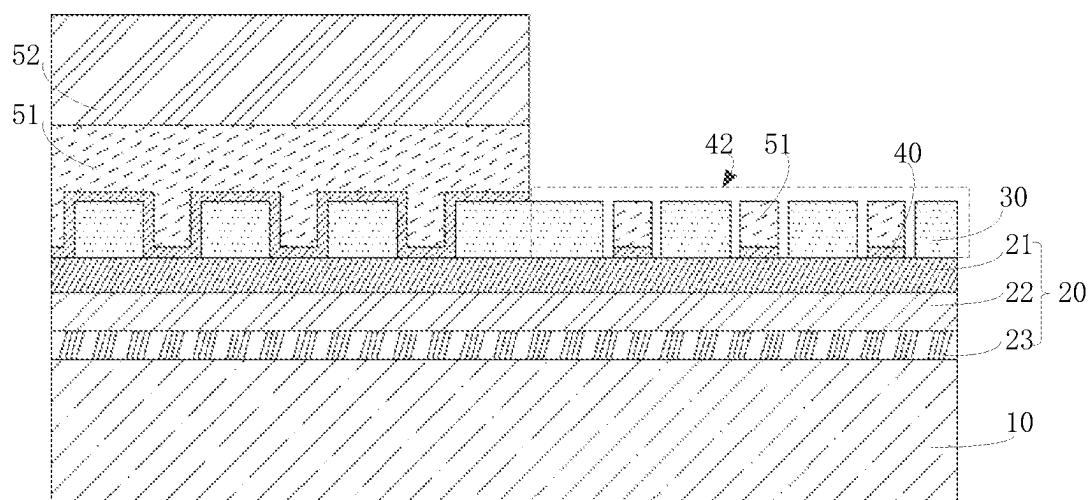


Fig. 8

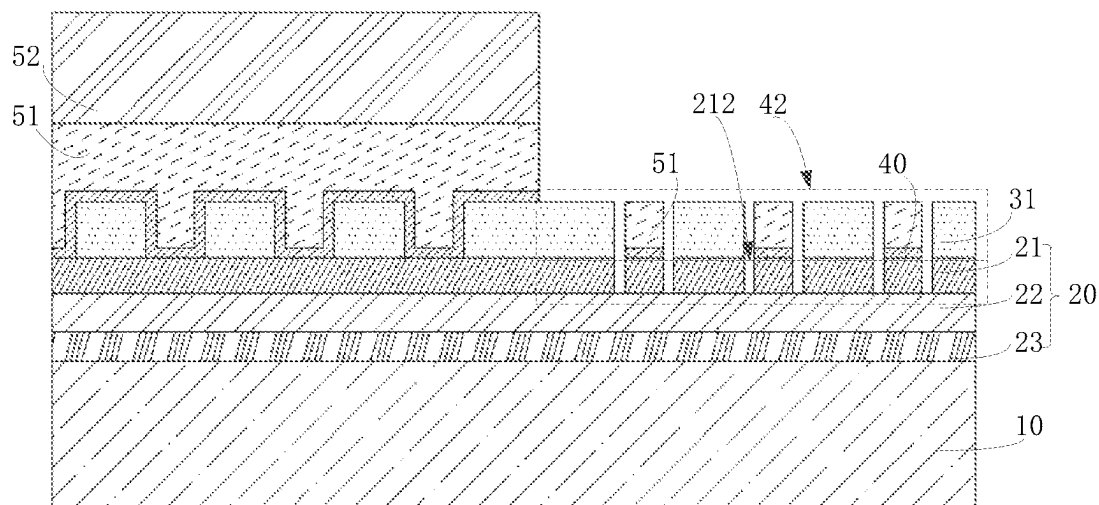


Fig. 9

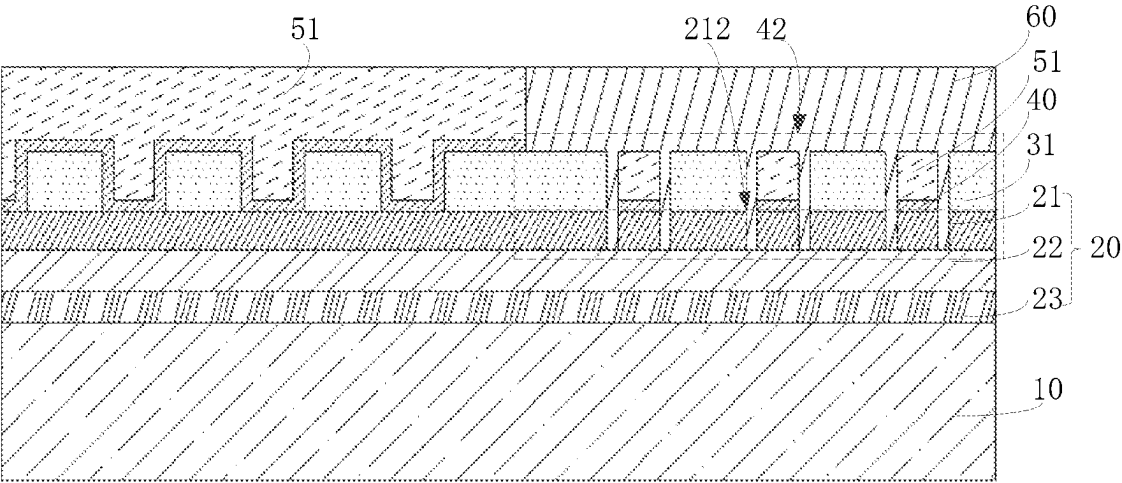


Fig. 10

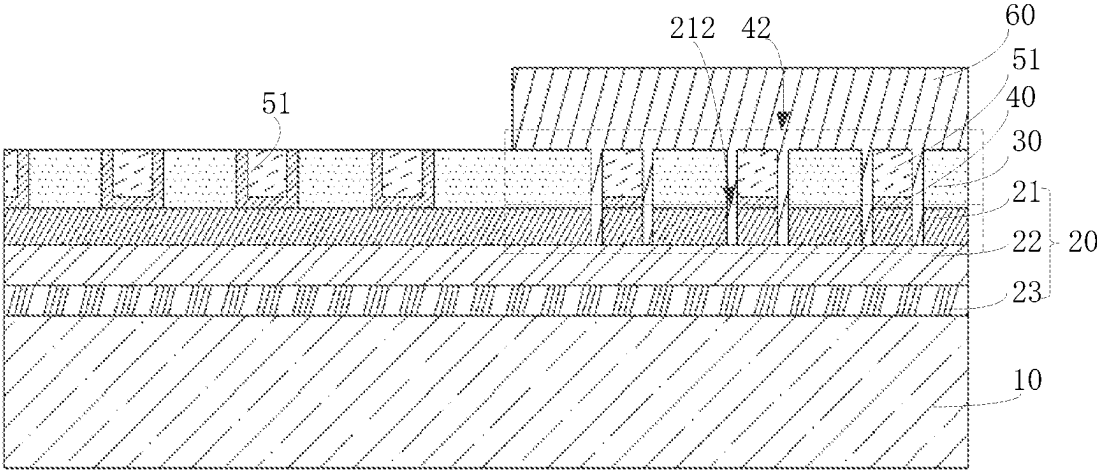


Fig. 11

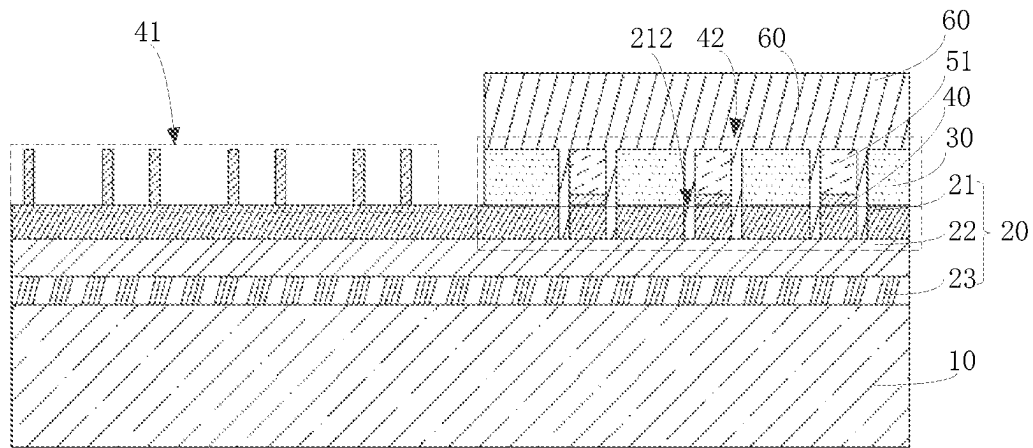


Fig. 12

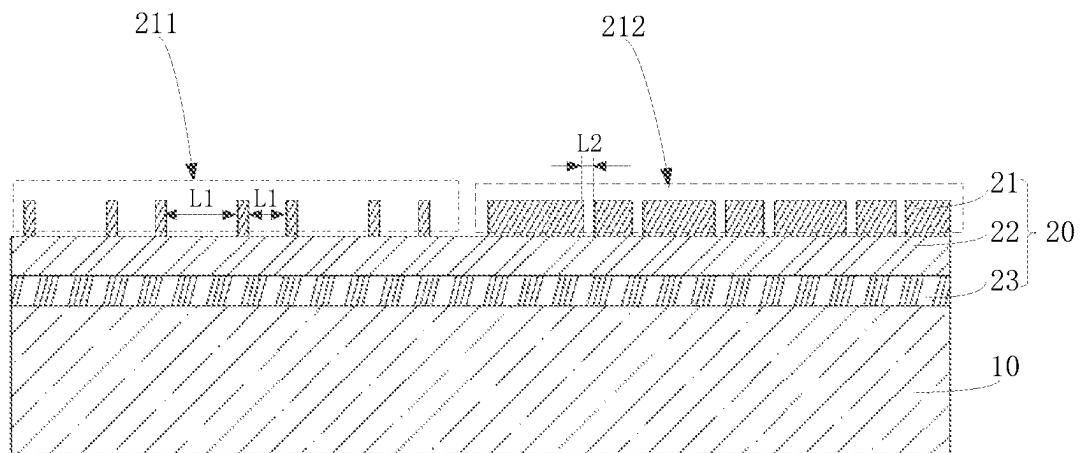


Fig. 13

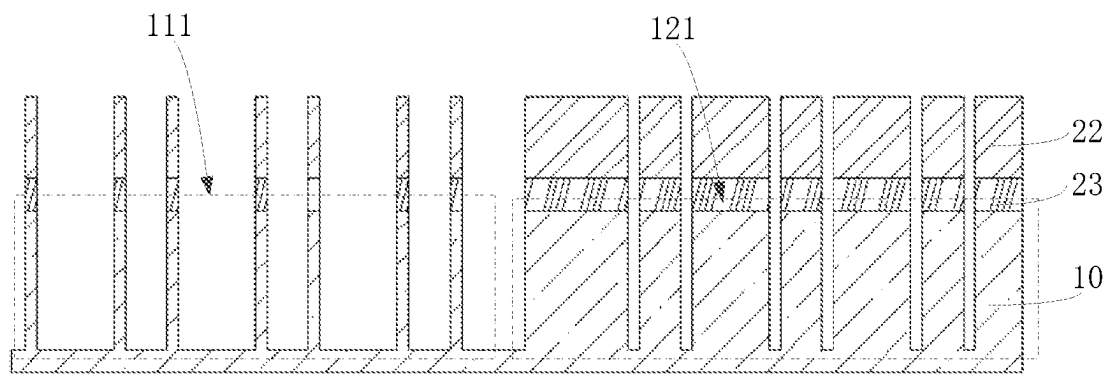


Fig. 14

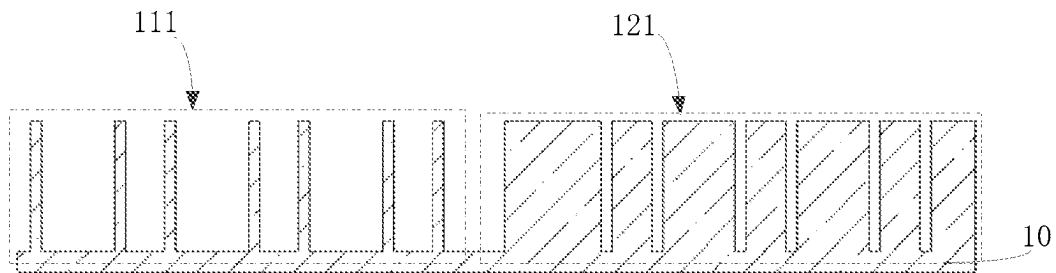


Fig. 15

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METHOD FOR FABRICATING SEMICONDUCTOR STRUCTURE AND SEMICONDUCTOR STRUCTURE

CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation of PCT/CN2022/077794, filed on Feb. 25, 2022, which claims priority to Chinese Patent Application No. 202111447165X titled “METHOD FOR FABRICATING SEMICONDUCTOR STRUCTURE AND SEMICONDUCTOR STRUCTURE” and filed to the State Intellectual Property Office on Nov. 30, 2021, the entire contents of which are incorporated herein by reference.

TECHNICAL FIELD

Embodiments of the present disclosure relate to the field of semiconductor manufacturing technology, and more particularly, to a method for fabricating a semiconductor structure and a semiconductor structure.

BACKGROUND

A semiconductor structure (such as a memory) includes a substrate and a device layer arranged on the substrate. Furthermore, the semiconductor structure also includes a peripheral region and an array region adjacent to the peripheral region. Corresponding device layers in the array region and the peripheral region are provided with corresponding Metal Oxide Semiconductor Field Effect Transistors (MOS transistors); and the substrate in the array region and the substrate in the peripheral region have mating structures configured to mate with the corresponding device layers. During fabrication, the mating structures in the array region and the peripheral region are fabricated separately, and then the device layers are formed to complete the fabrication of the semiconductor structure.

However, in related technologies, the mating structures on the substrate of the array region and the substrate of the peripheral region need to be fabricated separately, resulting in lower production efficiency.

SUMMARY

According to some embodiments, a first aspect of the present disclosure provides a method for fabricating a semiconductor structure, including: providing a substrate comprising an array region and a peripheral region; forming, on the substrate, a first mask layer covering the array region and the peripheral region, such that the first mask layer has a first device structure pattern over the peripheral region and a second device structure pattern over the array region; and etching the substrate by using the first device structure pattern and the second device structure pattern as mask layer to form a peripheral region structure and an array region structure, respectively.

According to some embodiments, a second aspect of the present disclosure also provides a semiconductor structure, which is formed by the above method for fabricating a semiconductor structure.

Embodiments of the present disclosure provide a method for fabricating a semiconductor structure and a semiconductor structure. The method includes: providing a substrate comprising an array region and a peripheral region; forming, on the substrate, a first mask layer covering the array region

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and the peripheral region, such that the first mask layer has a first device structure pattern directly facing the array region and a second device structure pattern directly facing the peripheral region; and etching the substrate by using the first device structure pattern and the second device structure pattern as mask layer to form a peripheral region structure and an array region structure, respectively. According to the method for fabricating a semiconductor structure provided by the embodiments of the present disclosure, the first mask layer having the first device structure pattern and the second device structure pattern is first formed on the substrate, and then the substrate is etched by using the first device structure pattern and the second device structure pattern as mask layer to synchronously form a peripheral region structure and an array region structure on the substrate, thereby simplifying technological processes, reducing fabrication difficulties, and improving production efficiencies.

BRIEF DESCRIPTION OF THE DRAWINGS

To describe the technical solutions in the embodiments of the present disclosure or the existing technologies more clearly, the accompanying drawings required for describing the embodiments or the existing technologies will be briefly introduced below. Apparently, the accompanying drawings in the following description are merely some embodiments of the present disclosure. To those of ordinary skills in the art, other accompanying drawings may also be derived from these accompanying drawings without creative efforts.

FIG. 1 is a flowchart showing steps of a method for fabricating a semiconductor structure according to an embodiment of the present disclosure;

FIG. 2 is a vertical view of a substrate provided in the method for fabricating a semiconductor structure according to an embodiment of the present disclosure;

FIG. 3 is a schematic structural diagram of the substrate provided in the method for fabricating a semiconductor structure according to an embodiment of the present disclosure;

FIG. 4 is a schematic structural diagram showing a first mask pattern and a first dielectric layer formed in the method for fabricating a semiconductor structure according to an embodiment of the present disclosure;

FIG. 5 is a schematic structural diagram showing a twenty-first mask layer formed in the method for fabricating a semiconductor structure according to an embodiment of the present disclosure;

FIG. 6 is a schematic structural diagram obtained after a part of a twenty-second mask layer is removed in the method for fabricating a semiconductor structure according to an embodiment of the present disclosure;

FIG. 7 is a schematic structural diagram obtained after a part of the twenty-first mask layer is removed in the method for fabricating a semiconductor structure according to an embodiment of the present disclosure;

FIG. 8 is a schematic structural diagram showing a second mask pattern formed in the method for fabricating a semiconductor structure according to an embodiment of the present disclosure;

FIG. 9 is a schematic structural diagram showing a second device structure pattern formed in the method for fabricating a semiconductor structure according to an embodiment of the present disclosure;

FIG. 10 is a schematic structural diagram showing a third mask layer formed in the method for fabricating a semiconductor structure according to an embodiment of the present disclosure;

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FIG. 11 is a schematic structural diagram obtained after a part of a second mask layer is removed in the method for fabricating a semiconductor structure according to an embodiment of the present disclosure;

FIG. 12 is a schematic structural diagram showing the first mask pattern formed in the method for fabricating a semiconductor structure according to an embodiment of the present disclosure;

FIG. 13 is a schematic structural diagram showing a first device structure pattern and a second device structure pattern formed in the method for fabricating a semiconductor structure according to an embodiment of the present disclosure;

FIG. 14 is a schematic structural diagram obtained after a part of the first mask layer is removed in the method for fabricating a semiconductor structure according to an embodiment of the present disclosure; and

FIG. 15 is a schematic structural diagram showing a peripheral region structure and an array region structure formed in the method for fabricating a semiconductor structure according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

Several implementation manners of the present disclosure are introduced below in conjunction with the accompanying drawings. Those skilled in the art should understand that the following implementation manners are only illustrative, and are not exhaustive enumerations. On the basis of these implementation manners, those skilled in the art may replace, concatenate or combine some features or some examples, which should still be regarded as disclosed contents of the present disclosure.

Referring to FIG. 1 and FIG. 2, an embodiment of the present disclosure provides a method for fabricating a semiconductor structure. The semiconductor structure generally includes a substrate 10 and a device layer arranged on the substrate 10. This method is configured for forming, on the substrate 10, a mating structure configured to mate with a device layer, including following steps.

Step S101: providing a substrate including an array region and a peripheral region.

As shown in FIG. 2 and FIG. 3, the substrate 10 also includes a peripheral region 11 (a left side of a position as shown in FIG. 3) and an array region 12 (a right side of the position as shown in FIG. 3), and the array region 12 is adjacent to the peripheral region 11. Referring to FIG. 2, the peripheral region 11 may be arranged at the periphery of the array region 12. Of course, in some other examples, relative positions of the peripheral region 11 and the array region 12 may also be set according to actual needs, which is not restricted in this embodiment. The peripheral region 11 may be configured to, for example, form a mating structure configured to mate with a peripheral circuit, and the array region 12 may be configured to, for example, form a mating structure configured to mate with a memory cell. The array region 12 may also include different regions to mate with different types of memory cells. Of course, in some other examples, the mating structures of the peripheral region 11 and the array region 12 may also be configured to mate with other devices.

In this embodiment, the substrate 10 may be a semiconductor substrate 10 such as single-crystal silicon, polysilicon, or amorphous structure such as silicon or silicon germanium (SiGe), or may be a hybrid semiconductor structure, such as silicon carbide, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium

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arsenide or gallium antimonide, an alloy semiconductor, or a combination thereof. However, in this embodiment, types of the substrate 10 are not limited thereto.

Step S102: forming, on the substrate, a first mask layer covering the array region and the peripheral region, such that the first mask layer has a first device structure pattern directly facing the peripheral region and a second device structure pattern directly facing the array region.

In this embodiment, a part of a first mask layer 20 may be removed by means of etching, and then a first device structure pattern 211 and a second device structure pattern 212 are formed on the first mask layer 20. The first device structure pattern 211 directly faces the peripheral region 11, which is advantageous to forming a peripheral region structure 111 subsequently by using the first device structure pattern 211 as mask layer. The second device structure pattern 212 directly faces the array region 12, which is advantageous to forming an array region structure 121 by using the second device structure pattern 212 as mask layer.

As shown in FIG. 3, the first mask layer 20 includes an eleventh mask layer 21 and a twelfth mask layer 22, where the eleventh mask layer 21 is positioned on the twelfth mask layer 22. A material of the eleventh mask layer 21 may include an inorganic material, for example, a dielectric anti-reflective coating (DARC) such as silicon oxide (SiO₂), silicon (Si), and silicon-rich silicon oxynitride (SiON). For forming patterns with pitches close to resolution limit of photolithography, light reflection may be minimized by providing the eleventh mask layer 21 to enhance resolution, thereby increasing precision of photoengraving an edge of a definable pattern, such that precision of forming mask patterns on the eleventh mask layer 21 can be improved. A material of the twelfth mask layer 22 may include amorphous carbon, which is a material highly transparent to light (i.e., "transparent carbon"), and which provides improvement of alignment by being transparent to a wavelength of light for optical alignment. Further, the amorphous carbon has very high etching selectivity relative to a hard mask material used in the related technologies, which can further improve accuracy of forming a mask pattern on the twelfth mask layer 22.

With continued reference to FIG. 3, the first mask layer 20 further includes a thirteenth mask layer 23, which is positioned between the twelfth mask layer 22 and the substrate 10. A material of the thirteenth mask layer 23 may also include silicon nitride, silicon oxide, and silicon oxynitride, etc. When a photoengraving pattern is formed on the eleventh mask layer 21 and the twelfth mask layer 22, the substrate 10 can be protected by providing the thirteenth mask layer 23.

In this embodiment, after the forming, on the substrate 10, a first mask layer 20 covering the array region 12 and the peripheral region 11, such that the first mask layer 20 has a first device structure pattern 211 directly facing the peripheral region 11 and a second device structure pattern 212 directly facing the array region 12, the method also includes:

Step S103: etching the substrate by using the first device structure pattern and the second device structure pattern as mask layer to form the peripheral region structure and the array region structure, respectively.

In some embodiments, a pattern density of the first device structure pattern 211 may be smaller than that of the second device structure pattern 212. As shown in FIG. 13, in the first device structure pattern 211, there is a first distance L1 between adjacent two of the plurality of rectangular blocks. It is worth noting that the first device structure pattern 211 in FIG. 13 is only exemplary. According to actual setting

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needs, the first distance L1 between any adjacent two of the plurality of rectangular blocks may be the same (that is, the plurality of rectangular blocks are arranged at equal distance) or may be different (that is, the plurality of rectangular blocks are arranged at unequal intervals). The second device structure pattern 212 includes a plurality of rectangular blocks arranged at intervals, and there is a second distance L2 between adjacent two of the plurality of rectangular blocks, where any first distance L1 is greater than the second distance L2. That is, the pattern density of the first device structure pattern 211 is smaller than that of the second device structure pattern 212. According to the embodiments of the present disclosure, the second device structure pattern 212 having a larger pattern density is first formed, then the first device structure pattern 211 having a smaller pattern density is formed, and then the substrate is synchronously etched. In this way, it is advantageous to protecting the first device structure pattern 211 having the smaller pattern density, and solving a problem of collapse of the first device structure pattern 211 having the smaller pattern density at a periphery. Moreover, it is advantageous to subsequently forming a corresponding peripheral region structure 111 and an array region structure 121 in the substrate 10, and ensuring a pattern density of the peripheral region structure 111 to be smaller than that of the array region structure 121, such that it is advantageous to subsequent formation of corresponding device layers on the peripheral region structure 111 and the array region structure 121.

In this embodiment, after the substrate 10 is etched by using the first device structure pattern 211 and the second device structure pattern 212 as mask layer to form the peripheral region structure 111 and the array region structure 121 respectively, the method also includes: forming a first storage structure and a second storage structure on the array region structure 121 to adapt to different usage requirements in the array region 12. In this embodiment, the first storage structure and the second storage structure may include different types of memory cells. The first storage structure may include, for example, a plurality of dynamic random access memory cells, and each of the plurality of dynamic random access memory cells includes a transistor structure and a capacitor structure. The second storage structure may include, for example, a plurality of magnetic random access memory cells, and each of the plurality of magnetic random access memory cells includes a transistor structure and a magnetoresistive tunnel junction interposed between two metal lines. A resistance value of the magnetoresistive tunnel junction is changed by controlling transistors in the transistor structure, to read/write data. Of course, in some other examples, the first storage structure and the second storage structure may also include memory cells using other storage principles.

An embodiment of the present disclosure provides a method for fabricating a semiconductor structure. The method includes: providing a substrate 10 comprising an array region 12 and a peripheral region 11; forming, on the substrate 10, a first mask layer 20 covering the array region 12 and the peripheral region 11, such that the first mask layer 20 has a first device structure pattern 211 directly facing the array region 12 and a second device structure pattern 212 directly facing the peripheral region 11; and etching the substrate 10 by using the first device structure pattern 211 and the second device structure pattern 212 as mask layer to form a peripheral region structure 111 and an array region structure 121, respectively. According to the method for fabricating a semiconductor structure provided by the embodiment of the present disclosure, the first mask layer 20

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having the first device structure pattern 211 and the second device structure pattern 212 is first formed on the substrate 10, and then the substrate 10 is etched by using the first device structure pattern 211 and the second device structure pattern 212 as mask layer to synchronously form a peripheral region structure 111 and an array region structure 121 on the substrate 10, thereby simplifying technological processes, reducing fabrication difficulties, and improving production efficiencies.

In this embodiment, after the forming, on the substrate 10, a first mask layer 20 covering the array region 12 and the peripheral region 11, such that the first mask layer 20 has a first device structure pattern 211 directly facing the peripheral region 11 and a second device structure pattern 212 directly facing the array region 12, the method also includes: forming a first mask pattern 30 on the first mask layer 20.

As shown in FIG. 4, a projection of the first mask pattern 30 on the substrate 10 is positioned in the array region 12 and the peripheral region 11, such that the corresponding mating structures are respectively formed in the array region 12 and the peripheral region 11 of the substrate 10 subsequently by means of the first mask pattern 30.

In some embodiments, a pattern density of the first mask pattern 30 on the array region 12 is the same as a pattern density of the first mask pattern 30 on the peripheral region 11. The pattern density of the first mask pattern 30 on the array region 12 is the same as the pattern density of the first mask pattern 30 on the peripheral region 11, which simplifies the technological processes of forming the first mask pattern 30 and improves the production efficiencies.

Further, the first mask pattern 30 includes an elongated pattern. Exemplarily, the first mask pattern 30 includes a plurality of elongated patterns arranged at intervals. In this embodiment, the elongated patterns may be rectangular, for example. It should be noted that in some embodiments of the present disclosure, the peripheral region structure 111 and the array region structure 121 formed correspondingly by means of the first mask pattern 30 having the plurality of elongated patterns are also elongated. The peripheral region structure 111 and the array region structure 121 may be configured to form a part (e.g., a fin) of a Fin Field-Effect Transistor (FinFET), to improve performance of the semiconductor structure.

In a concrete implementation manner, a material of the first mask pattern 30 may include a hard mask material. A formation process of the first mask pattern 30 may include: forming a hard mask material layer on the first mask layer 20, and then etching the hard mask material layer to remove a part of the hard mask material, to form the corresponding first mask pattern 30. The hard mask material layer may be, for example, Spin on Hardmasks (SOH). As an auxiliary material for forming semiconductor fine patterns, the SOH is used as a membrane under a photoresist, and is used for facilitating a circuit to be transcribed to a target membrane to improve accuracy of the fine patterns and play an appropriate role of a defense film in the subsequent etching process. It should be noted that the material of the SOH is advantageous to achieving graphic accuracy of fine line width, thereby further improving the graphic accuracy of the first mask pattern 30.

In this embodiment, in the step of forming, on the substrate 10, a first mask layer 20 covering the array region 12 and the peripheral region 11, such that the first mask layer 20 has a first device structure pattern 211 directly facing the peripheral region 11 and a second device structure pattern 212 directly facing the array region 12, after the forming a first mask pattern 30 on the first mask layer 20, the method

also includes: forming a first dielectric layer **40** on the first mask layer **20** and the first mask pattern **30**.

As shown in FIG. 4, the first mask pattern **30** may cover a part of surface of the first mask layer **20**. In the embodiment where the first mask pattern **30** includes a plurality of rectangular blocks arranged at intervals, the first mask layer **20** is exposed between adjacent two of the plurality of rectangular blocks. That is, the first mask pattern **30** may cover a part of surface of the first mask layer **20**.

The forming a first dielectric layer **40** on the first mask layer **20** and the first mask pattern **30** also includes: conformally covering, by the first dielectric layer **40**, a top surface and a sidewall of the first mask pattern **30** and the exposed surface of the first mask layer **20**. With continued reference to FIG. 4, in this embodiment, the first dielectric layer **40** covers a sidewall of a given one of the plurality of rectangular blocks and an end surface (that is, the top surface of the first mask pattern **30**) of the given rectangular block facing away from the substrate **10**. The first dielectric layer **40** also covers the first mask layer **20** between adjacent two of the plurality of rectangular blocks (i.e., covering the exposed surface of the first mask layer **20**).

In a concrete implementation manner, a material of the first dielectric layer **40** may include silicon oxide, silicon nitride, and silicon oxynitride, etc., such that the first dielectric layer **40** can protect the first mask pattern **30**.

In this embodiment, in the step of forming, on the substrate **10**, a first mask layer **20** covering the array region **12** and the peripheral region **11**, such that the first mask layer **20** has a first device structure pattern **211** directly facing the peripheral region **11** and a second device structure pattern **212** directly facing the array region **12**, after the forming a first dielectric layer **40** on the first mask layer **20** and the first mask pattern **30**, the method also includes: forming a second mask layer on the first dielectric layer **40** in the peripheral region **11**.

In this embodiment, the step of forming a second mask layer on the first dielectric layer **40** in the array region **12** may include: forming a twenty-first mask layer **51** on the first dielectric layer **40**, and forming a twenty-second mask layer **52** on the twenty-first mask layer **51**. As shown in FIG. 5, a projection of the twenty-first mask layer **51** on the substrate **10** is positioned in the array region **12** and the peripheral region **11**, and the twenty-second mask layer **52** is positioned on the twenty-first mask layer **51**.

In this embodiment, a sidewall of the first dielectric layer **40** is positioned on a surface of the first dielectric layer **40** covering the sidewall of the first mask pattern **30**, and a top surface of the first dielectric layer **40** is positioned on the surface of the first dielectric layer **40** covering the top surface of the first mask layer **20**. As shown in FIG. 5, the twenty-first mask layer **51** may cover the top surface and the sidewall of the first dielectric layer **40**. Further, the sidewall of the first dielectric layer **40** and the first dielectric layer **40** covering the exposed first mask layer **20** may surround and form a groove, and the twenty-first mask layer **51** also fills up the groove.

In a concrete implementation manner, a material of the twenty-first mask layer **51** may include a hard mask material, such as SOH. It is to be noted that a material of the SOH may have characteristics of filling gaps, increasing flatness and enhancing corrosion resistance, which may facilitate the twenty-first mask layer **51** to fill up the groove of the first dielectric layer **40** and facilitate to maintain the flatness of the twenty-first mask layer **51**. Further, the twenty-first mask layer **51** can also protect the first dielectric layer **40**.

In this embodiment, in the step of forming, on the substrate **10**, a first mask layer **20** covering the array region **12** and the peripheral region **11**, such that the first mask layer **20** has a first device structure pattern **211** directly facing the peripheral region **11** and a second device structure pattern **212** directly facing the array region **12**, after the forming a second mask layer on the first dielectric layer **40** in the peripheral region **11**, the method also includes: forming a second mask pattern **42** on the array region **12**; and forming the second device structure pattern **212** on the first mask layer **20** by using the second mask pattern **42** as mask layer.

In this embodiment, referring to FIG. 6, the step of forming a second mask pattern **42** on the peripheral region **11** includes: removing the twenty-second mask layer **52** on the array region **12** and the twenty-first mask layer **51** and the first dielectric layer **40** on the top of the first mask pattern **30**; and removing the first dielectric layer **40** positioned on the sidewall of the first mask pattern **30** on the array region **12** to form the second mask pattern **42**.

It is to be noted that referring to FIG. 7, the twenty-second mask layer **52** and a part of the twenty-first mask layer **51** may be removed first to expose the first dielectric layer **40** covering the top surface of the first mask pattern **30**.

In a concrete implementation manner, a material of the twenty-second mask layer **52** may include a photoresist. A formation process of the twenty-second mask layer **52** is briefly described as below by taking an example where the material of the twenty-second mask layer **52** is a positive photoresist. The positive photoresist is coated on the twenty-first mask layer **51** to form the twenty-second mask layer **52**, then a photomask is formed on the twenty-second mask layer **52**, such that the photomask can shield the positive photoresist whose projection is in the peripheral region **11**, and then exposure and development are performed on rest of the exposed positive photoresist to remove the initial twenty-second mask layer **52** whose projection is in the array region **12**.

After the twenty-second mask layer **52** on the array region **12** is removed, the first dielectric layer **40** covering the top surface of the first mask pattern **30** is removed, and a part of the twenty-first mask layer **51** is removed synchronously, such that an end surface of the twenty-first mask layer **51** facing away from the substrate **10** is flush with the top surface of the first mask pattern **30**. Next, the first dielectric layer **40** covering the sidewall of the first mask pattern **30** is removed, to retain the first mask pattern **30**, a part of the first dielectric layer **40** and a part of the twenty-first mask layer **51** in the array region **12**. In this way, the second mask pattern **42** is formed.

With reference to FIG. 8, the second mask pattern **42** may include a plurality of rectangular blocks arranged at intervals. Of course, in some other examples, a shape of the second mask pattern **42** may be adjusted by setting a shape of the first mask pattern **30** and a film-forming thickness of the first dielectric layer **40**, where the shape of the second mask pattern **42** is not particularly limited in this embodiment.

In this embodiment, after the second mask pattern **42** is formed on the array region **12**, the method also includes: forming the second device structure pattern **212** on the first mask layer **20** by using the second mask pattern **42** as mask layer.

Referring to FIG. 8 and FIG. 9, to form the second device structure pattern **212**, it is required to remove a part of the first mask layer **20** by using the second mask pattern **42** as mask layer. In this embodiment, the eleventh mask layer **21** on the array region **12** is etched by using the second mask

pattern 42 as mask layer to form the second device structure pattern 212. As shown in FIG. 12 and FIG. 13, a shape of the second device structure pattern 212 is the same as that of the second mask pattern 42, where the second device structure pattern 212 may include a plurality of rectangular blocks arranged at intervals. Further, in some other examples, the shape of the second device structure pattern 212 may be adjusted by setting the shape of the second mask pattern 42, and the shape of the second device structure pattern 212 is not particularly limited in this embodiment.

In this embodiment, in the step of forming, on the substrate 10, a first mask layer 20 covering the array region 12 and the peripheral region 11, such that the first mask layer 20 has a first device structure pattern 211 directly facing the peripheral region 11 and a second device structure pattern 212 directly facing the array region 12, after the forming a second mask pattern 42 on the array region 12 and forming the second device structure pattern 212 on the first mask layer 20 by using the second mask pattern 42 as mask layer, the method also includes: forming a third mask layer 60 on the second device structure pattern 212.

As shown in FIG. 9, in the embodiment where in the first mask layer 20, the second device structure pattern 212 is shaped like a plurality of rectangular blocks arranged at intervals, the second device structure pattern 212 is formed in the eleventh mask layer 21, and the second device structure pattern 212 covers a part of the twelfth mask layer 22, such that a part of the twelfth mask layer 22 is exposed between adjacent two of the plurality of rectangular blocks. The third mask layer 60 conformally covers the eleventh mask layer 21 and the exposed twelfth mask layer 22.

In this embodiment, the step of forming a third mask layer 60 on the second device structure pattern 212 may include: forming an initial third mask layer 60 on the first dielectric layer 40, and then removing the initial third mask layer 60 on the peripheral region 11 to form the third mask layer 60.

In a concrete implementation manner, a material of the third mask layer 60 may include a photoresist. A formation process of the third mask layer 60 is briefly described as below by taking an example where the material of the third mask layer 60 is a positive photoresist. The positive photoresist is coated on the second device structure pattern 212 and the second mask layer to form the initial third mask layer 60, then a photomask is formed on the initial third mask layer 60, such that the photomask can shield the positive photoresist whose projection is in the array region 12, and then exposure and development are performed on rest of the exposed positive photoresist to remove the initial third mask layer 60 whose projection is in the peripheral region 11. That is, the initial third mask layer 60 covered on the second mask layer is removed. In this way, the third mask layer 60 is formed.

It is to be noted that in an embodiment where the material of the third mask layer 60 and the material of the twenty-second mask layer 52 are both the positive photoresist, a photomask is formed on the initial third mask layer 60, such that the photomask can shield the photoresist whose projection is in the array region 12, and then exposure and development are performed on rest of the exposed photoresist to remove the initial third mask layer 60 whose projection is in the peripheral region 11, such that the twenty-second mask layer 52 is exposed. At this moment, the twenty-second mask layer 52 covering the peripheral region 11 may be further removed by means of exposure and development to expose the twenty-first mask layer 51, which may facilitate to further remove the twenty-first mask layer 51 subsequently to form a third mask pattern 41 on the

peripheral region 11. In some other examples, both the material of the third mask layer 60 and the material of the twenty-second mask layer 52 may also be a negative photoresist, and the process thereof is not to be repeated here.

In this embodiment, in the step of forming, on the substrate 10, a first mask layer 20 covering the array region 12 and the peripheral region 11, such that the first mask layer 20 has a first device structure pattern 211 directly facing the peripheral region 11 and a second device structure pattern 212 directly facing the array region 12, after the forming a third mask layer 60 on the second device structure pattern 212, the method also includes: forming a third mask pattern 41 on the peripheral region 11; and forming the first device structure pattern 211 on the first mask layer 20 by using the third mask pattern 41 as mask layer.

In this embodiment, the step of forming a third mask pattern 41 on the peripheral region 11 includes: removing the first mask pattern 30 and a part of the first dielectric layer 40 on the peripheral region 11, and retaining the first dielectric layer 40 positioned on a sidewall of the first mask pattern 30 to form a second mask pattern 42.

It is to be noted that before removing the first mask pattern 30 and a part of the first dielectric layer 40 on the peripheral region 11, the second mask layer on the peripheral region 11 needs to be first removed to expose the first mask pattern 30 and the first dielectric layer 40.

As shown in FIG. 10, FIG. 11 and FIG. 12, in this embodiment, the first dielectric layer 40 covering the top surface of the first mask pattern 30 may be removed first to expose the first mask pattern 30. Next, the first mask pattern 30 and the first dielectric layer 40 covering the first mask layer 20 are removed, and the first dielectric layer 40 covering the sidewalls of the first mask pattern 30 is retained to form the third mask pattern 41.

With continued reference to FIG. 12, the third mask pattern 41 may include a plurality of rectangular blocks arranged at intervals. Of course, in some other examples, a shape of the third mask pattern 41 may be adjusted by setting the shape of the first mask pattern 30 and a film-forming thickness of the first dielectric layer 40, where the shape of the third mask pattern 41 is not particularly limited in this embodiment.

In this embodiment, after the third mask pattern 41 is formed on the peripheral region 11, the method also includes: forming the first device structure pattern 211 on the first mask layer 20 by using the third mask pattern 41 as mask layer.

Referring to FIG. 13, FIG. 14 and FIG. 15, to form the first device structure pattern 211, it is required to remove a part of the first mask layer 20 by using the third mask pattern 41 as mask layer. In this embodiment, the eleventh mask layer 21 on the peripheral region 11 is etched by using the third mask pattern 41 as mask layer to form the first device structure pattern 211. As shown in FIG. 12 and FIG. 13, a shape of the first device structure pattern 211 is the same as that of the third mask pattern 41, where the first device structure pattern 211 may include a plurality of rectangular blocks arranged at intervals. Further, in some other examples, the shape of the first device structure pattern 211 may be adjusted by setting the shape of the third mask pattern 41, and the shape of the first device structure pattern 211 is not particularly limited in this embodiment.

In this embodiment, before etching the substrate 10 by using the second device structure pattern 212 as mask layer, the method further includes: removing the third mask layer 60 to expose the second device structure pattern 212 and a part of the substrate 10 positioned in the array region 12,

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which facilitates to etch the substrate **10** subsequently by using the second device structure pattern **212** as mask layer.

Further, as shown in FIG. **14**, before etching the substrate **10** by using the first device structure pattern **211** as mask layer, the method also includes: removing the first mask pattern **30**, the first dielectric layer **40** and the twenty-first mask layer **51** in the array region **11**, to expose the first device structure pattern **211** in the array region **11** and a part of the substrate **10**, which may facilitate subsequent etching of the substrate **10** by using the first device structure pattern **211** as mask layer.

In this embodiment, before etching the substrate **10** by using the first device structure pattern **211** and the second device structure pattern **212** as mask layer, the method also includes: etching the twelfth mask layer **22** and the thirteenth mask layer **23** by using the first device structure pattern **211** and the second device structure pattern **212** as mask layer, to avoid a subsequent etching effect on the substrate **10**.

An embodiment of the present disclosure also provides a semiconductor structure including a substrate **10**, which includes an array region **12** and a peripheral region **11**, where the peripheral region **11** has a peripheral region structure **111**, and the array region **12** has an array region structure **121**. A method for fabricating the peripheral region structure **111** and the array region structure **121** includes: forming, on the substrate **10**, a first mask layer **20** covering the array region **12** and the peripheral region **11**; forming a first mask pattern **30** on the first mask layer **20**; forming a first dielectric layer **40** on the first mask layer **20** and the first mask pattern **30**, and forming a second mask layer on the first dielectric layer **40** of the array region **12**; forming a second mask pattern **42** on the peripheral region **11**; forming a first device structure pattern **211** on the first mask layer **20** by using the second mask pattern **42** as mask layer; forming a third mask layer **60** on the first dielectric layer **40** of the peripheral region **11**; forming a third mask pattern **41** on the array region **12**; forming a second device structure pattern **212** on the first mask layer **20** by using the third mask pattern **41** as mask layer; and etching the substrate **10** by using the first device structure pattern **211** and the second device structure pattern **212** as mask layer to form the peripheral region structure **111** and the array region structure **121**, respectively. According to the method for fabricating a semiconductor structure provided by the embodiment of the present disclosure, the first mask layer **20** having the first device structure pattern **211** and the second device structure pattern **212** is first formed on the substrate **10**, and then the substrate **10** is etched by using the first device structure pattern **211** and the second device structure pattern **212** as mask layer to synchronously form a peripheral region structure **111** and an array region structure **121** on the substrate **10**, thereby simplifying technological processes, reducing fabrication difficulties, and improving production efficiencies.

Those skilled in the art may clearly understand that for the convenience and brevity of description, division of the above functional modules is merely taken as an example for illustration. In actual applications, the foregoing functions may be allocated to different functional modules and implemented according to needs. That is, an internal structure of an apparatus is divided into different functional modules to implement all or a part of the functions described above. For a detailed working process of the apparatus described above, reference may be made to the corresponding process in the foregoing method embodiments, and details are not described herein again.

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Finally, it should be noted that the foregoing embodiments are merely intended for describing the technical solutions of the present disclosure, but not for limiting the present disclosure. Although the present disclosure is described in detail with reference to the foregoing embodiments, persons of ordinary skill in the art should understand that they may still make modifications to the technical solutions described in the foregoing embodiments or make equivalent replacements to some or all technical features thereof, which does not make corresponding technical solutions in essence depart from the scope of the technical solutions of the embodiments of the present disclosure.

What is claimed is:

1. A method for fabricating a semiconductor structure, comprising:
 - providing a substrate comprising an array region and a peripheral region;
 - forming, on the substrate, a first mask layer covering the array region and the peripheral region, such that the first mask layer has a first device structure pattern over the peripheral region and a second device structure pattern over the array region; and
 - etching the substrate by using the first device structure pattern and the second device structure pattern as mask layer to form a peripheral region structure and an array region structure, respectively,
 wherein the forming, on the substrate, a first mask layer covering the array region and the peripheral region, such that the first mask layer has a first device structure pattern directly facing the peripheral region and a second device structure pattern directly facing the array region comprises:
 - forming a first mask pattern on the first mask layer;
 - forming a first dielectric layer on the first mask layer and the first mask pattern;
 - forming a second mask layer on the first dielectric layer;
 - forming a second mask pattern on the array region; and
 - forming the second device structure pattern on the first mask layer by using the second mask pattern as mask layer;
 - forming a third mask layer on the second device structure pattern; and
 - forming a third mask pattern on the peripheral region; and
 - forming the first device structure pattern on the first mask layer by using the third mask pattern as mask layer.
2. The method for fabricating a semiconductor structure according to claim 1, wherein the first mask layer comprises an eleventh mask layer and a twelfth mask layer, the eleventh mask layer being positioned on the twelfth mask layer;
 - etching the eleventh mask layer above the array region by using the second mask pattern as mask layer to form the second device structure pattern; and
 - etching the eleventh mask layer on the peripheral region by using the third mask pattern as mask layer to form the first device structure pattern.
3. The method for fabricating a semiconductor structure according to claim 2, wherein the first mask layer further comprises a thirteenth mask layer positioned between the twelfth mask layer and the substrate; and
 - before etching the substrate by using the first device structure pattern and the second device structure pattern as mask layer, the twelfth mask layer and the thirteenth mask layer are etched in sequence by using the first device structure pattern and the second device structure pattern as mask layer.

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4. The method for fabricating a semiconductor structure according to claim 1, wherein the forming a second mask pattern on the array region comprises:

removing a part of the second mask layer on the array region and the first dielectric layer positioned on a sidewall of the first mask pattern on the array region to form the second mask pattern.

5. The method for fabricating a semiconductor structure according to claim 4, wherein the second mask layer comprises a twenty-first mask layer and a twenty-second mask layer, the twenty-first mask layer covering a top surface and a sidewall of the first dielectric layer, and the twenty-second mask layer being positioned on the twenty-first mask layer.

6. The method for fabricating a semiconductor structure according to claim 5, wherein the twenty-second mask layer on the array region, the twenty-first mask layer and the first dielectric on a top of the first mask pattern are removed; and the first dielectric layer positioned on the sidewall of the first mask pattern on the array region is removed to form the second mask pattern.

7. The method for fabricating a semiconductor structure according to claim 1, wherein the forming a third mask pattern on the peripheral region comprises:

removing the first mask pattern and a part of the first dielectric layer on the peripheral region, and retaining the first dielectric layer positioned on a sidewall of the first mask pattern to form the third mask pattern.

8. The method for fabricating a semiconductor structure according to claim 1, wherein the forming a first dielectric layer on the first mask layer and the first mask pattern comprises:

covering, by the first mask pattern, a part of surface of the first mask layer; and

conformally covering, by the first dielectric layer, a top surface and a sidewall of the first mask pattern and an exposed surface of the first mask layer.

9. The method for fabricating a semiconductor structure according to claim 1, wherein before etching the substrate by using the first device structure pattern and the second device structure pattern as mask layer, the method further comprises:

removing the third mask layer.

10. The method for fabricating a semiconductor structure according to claim 1, wherein a pattern density of the first device structure pattern is smaller than a pattern density of the second device structure pattern.

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11. The method for fabricating a semiconductor structure according to claim 1, wherein a pattern density of the first mask pattern on the array region is the same as a pattern density of the first mask pattern on the peripheral region.

12. The method for fabricating a semiconductor structure according to claim 11, wherein the first mask pattern comprises an elongated pattern.

13. The method for fabricating a semiconductor structure according to claim 1, wherein after etching the substrate by using the first device structure pattern and the second device structure pattern as mask layer, the method further comprises:

forming a first storage structure and a second storage structure on the array region structure.

14. A semiconductor structure being formed by means of a method, wherein the method comprises:

providing a substrate comprising an array region and a peripheral region;

forming, on the substrate, a first mask layer covering the array region and the peripheral region, such that the first mask layer has a first device structure pattern over the peripheral region and a second device structure pattern over the array region; and

etching the substrate by using the first device structure pattern and the second device structure pattern as mask layer to form a peripheral region structure and an array region structure, respectively, wherein the forming, on the substrate, a first mask layer covering the array region and the peripheral region, such that the first mask layer has a first device structure pattern directly facing the peripheral region and a second device structure pattern directly facing the array region comprises:

forming a first mask pattern on the first mask layer;

forming a first dielectric layer on the first mask layer and the first mask pattern;

forming a second mask layer on the first dielectric layer; forming a second mask pattern on the array region; and

forming the second device structure pattern on the first mask layer by using the second mask pattern as mask layer;

forming a third mask layer on the second device structure pattern; and

forming a third mask pattern on the peripheral region; and forming the first device structure pattern on the first mask layer by using the third mask pattern as mask layer.

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