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(54) **SEMICONDUCTOR DEVICE**

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(30) **Foreign Application Priority Data**

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(52) **U.S. Cl.**

CPC ..... **H10D 30/6755** (2025.01); **H10B 12/312**  
(2023.02)

(57) **ABSTRACT**

A semiconductor device that can be easily miniaturized is provided. In addition, a semiconductor device that can be highly integrated is provided. The semiconductor device includes first to third conductive layers, a semiconductor layer, and first to third insulating layers. The first insulating layer is positioned over the first conductive layer and includes a slit reaching the first conductive layer. The second conductive layer is positioned over the first insulating layer. The semiconductor layer includes a portion in contact with a side surface of the second conductive layer, a portion in contact with a side surface of the first insulating layer in the slit, and a portion in contact with a top surface of the first conductive layer in the slit. The second insulating layer covers the semiconductor layer inside the slit. The third conductive layer covers the second insulating layer inside the slit. The top surfaces of the second conductive layer, the semiconductor layer, the second insulating layer, and the third conductive layer are substantially level with each other. The third insulating layer is in contact with the top surfaces of the second conductive layer, the semiconductor layer, the second insulating layer, and the third conductive layer.

**Publication Classification**

(51) **Int. Cl.**

**H10D 30/67** (2025.01)  
**H10B 12/00** (2023.01)

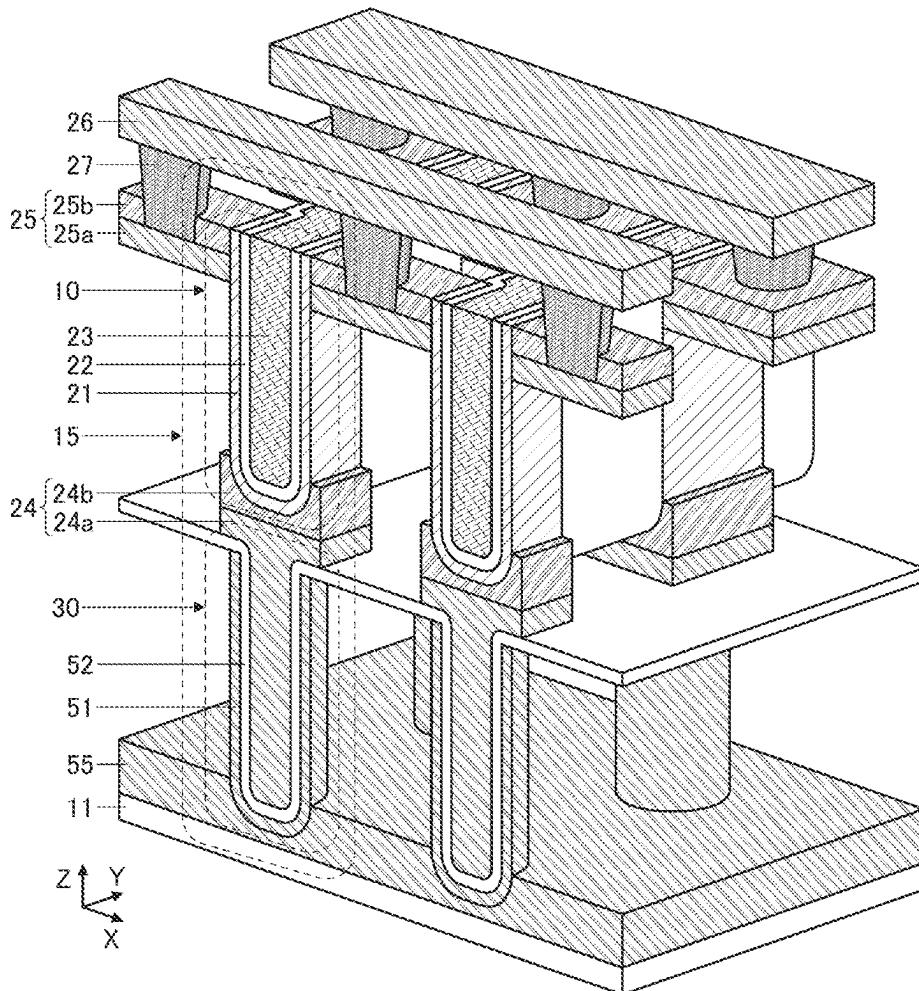


FIG. 1A

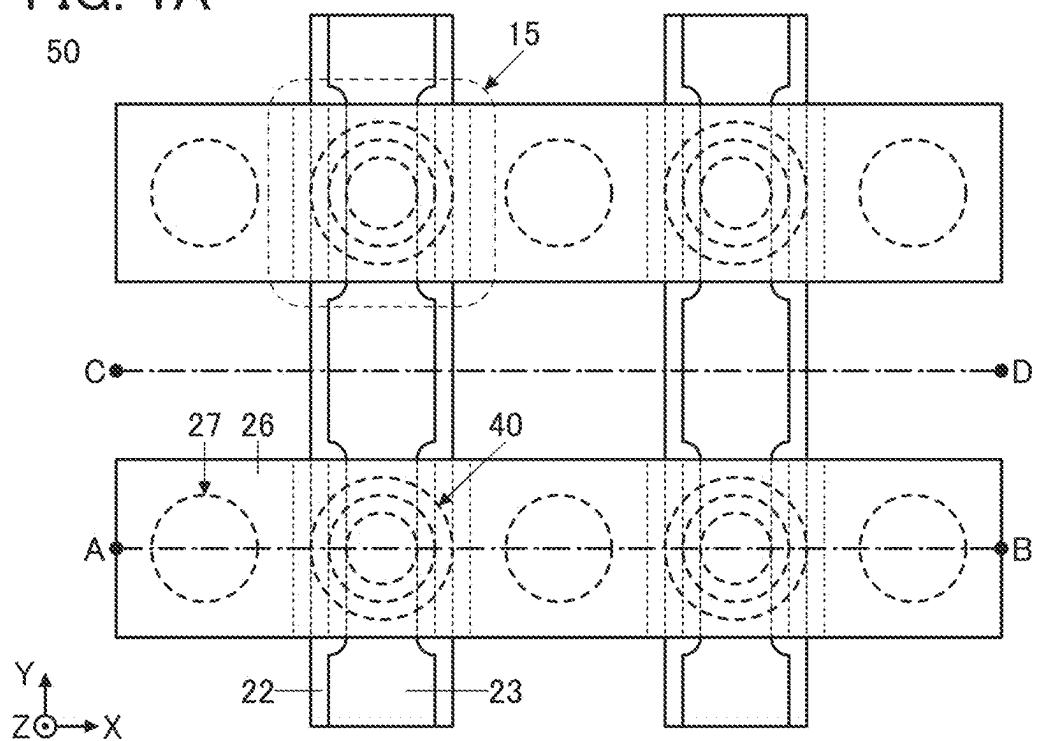


FIG. 1B

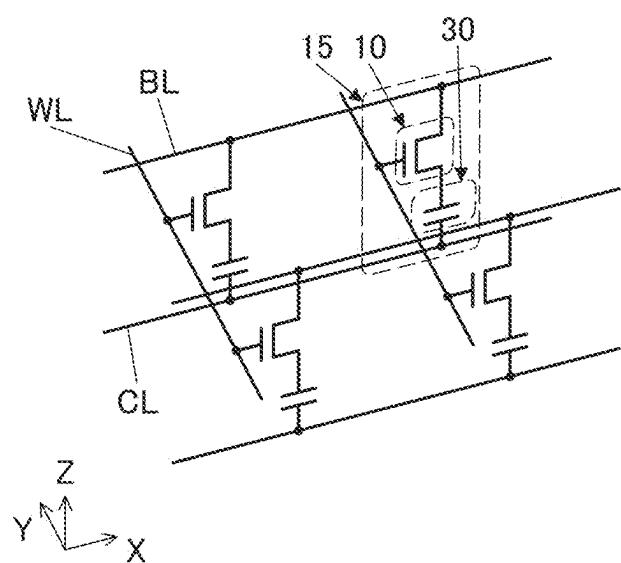


FIG. 2

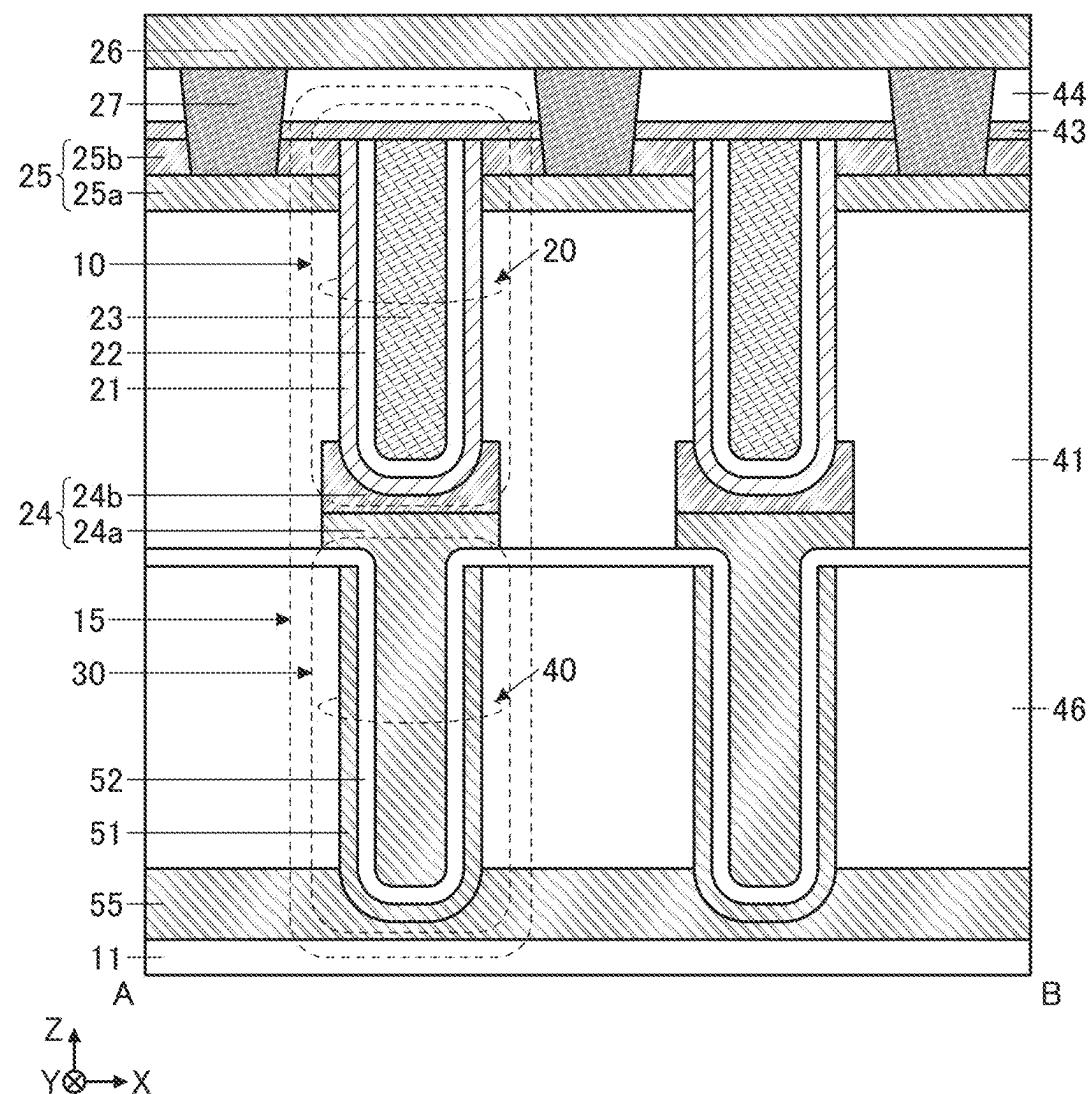


FIG. 3

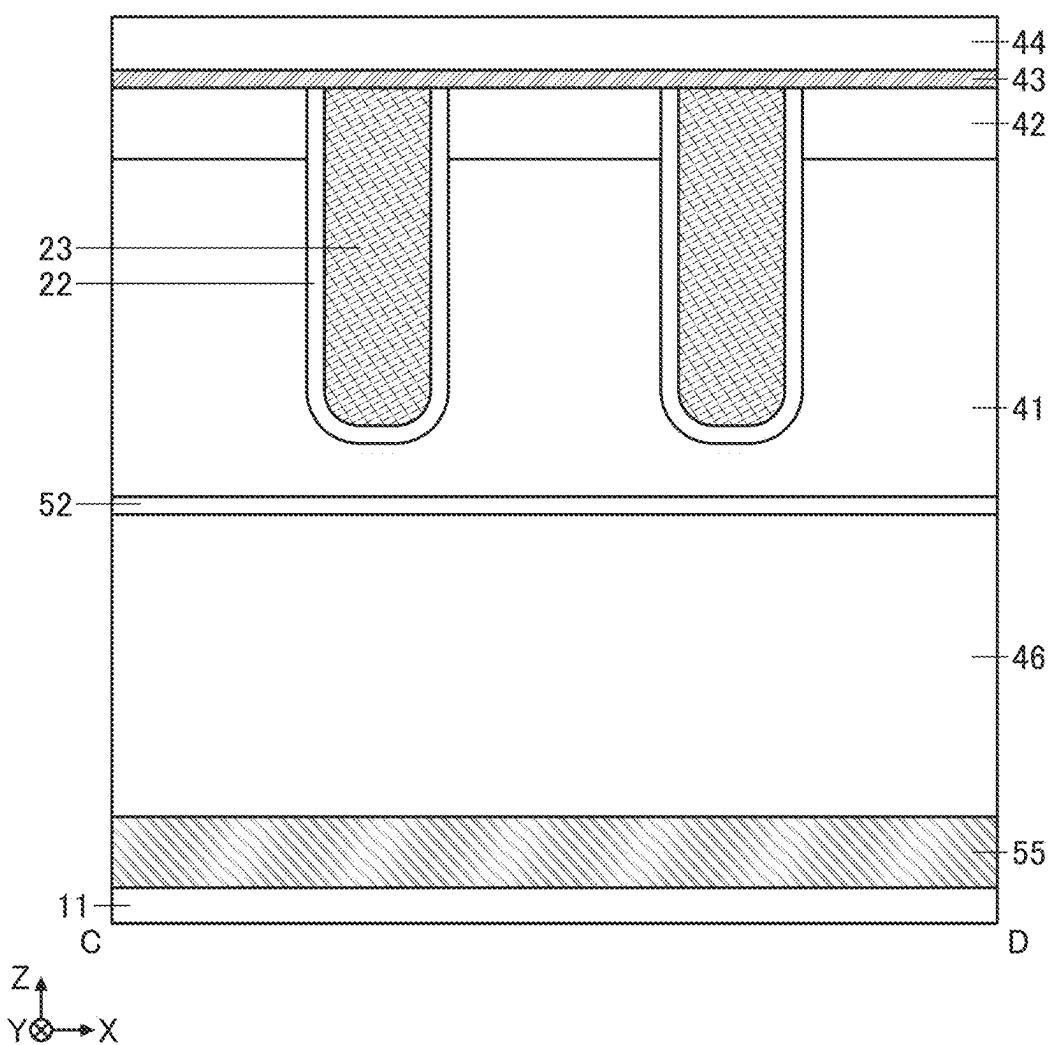


FIG. 4

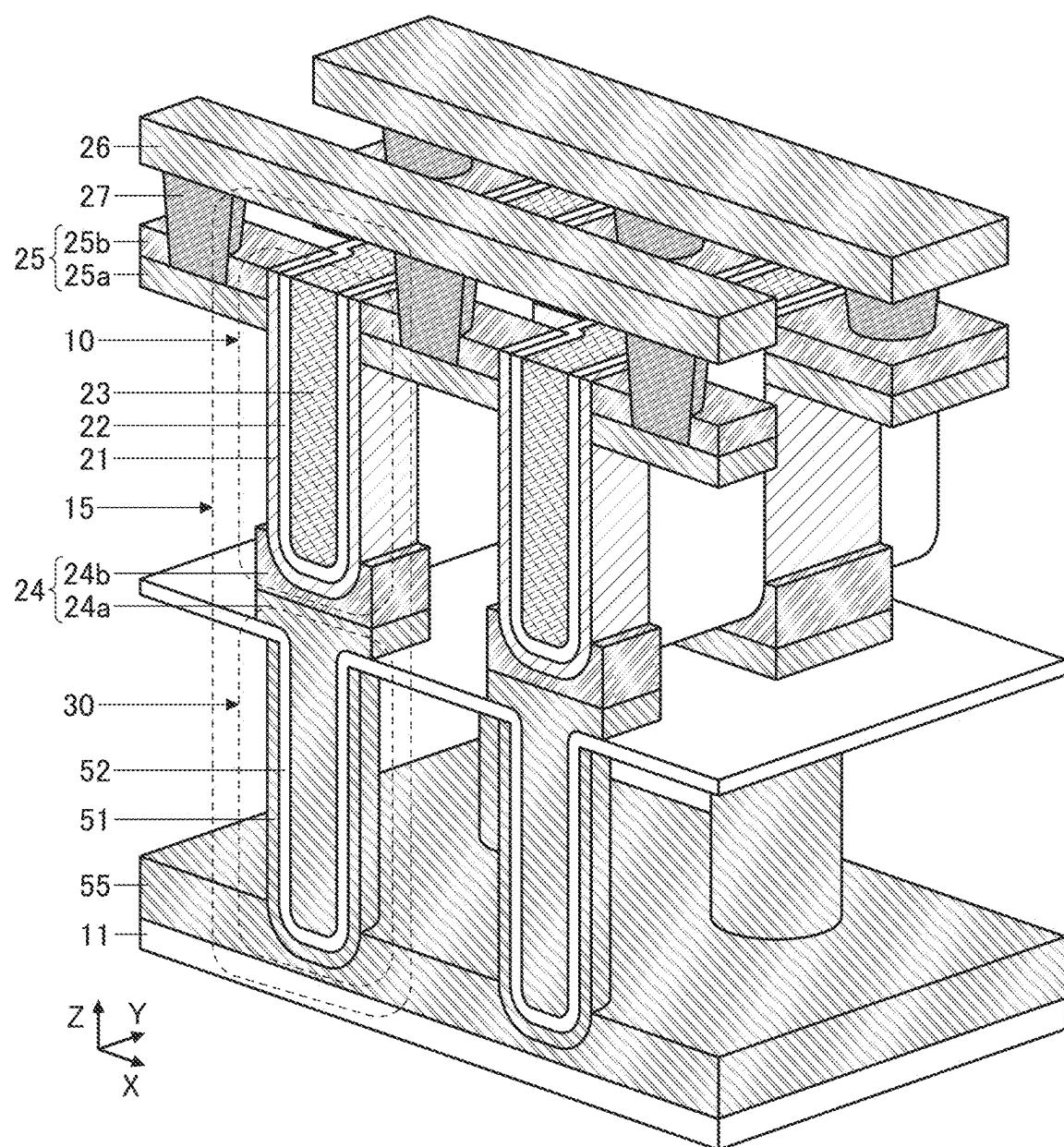


FIG. 5

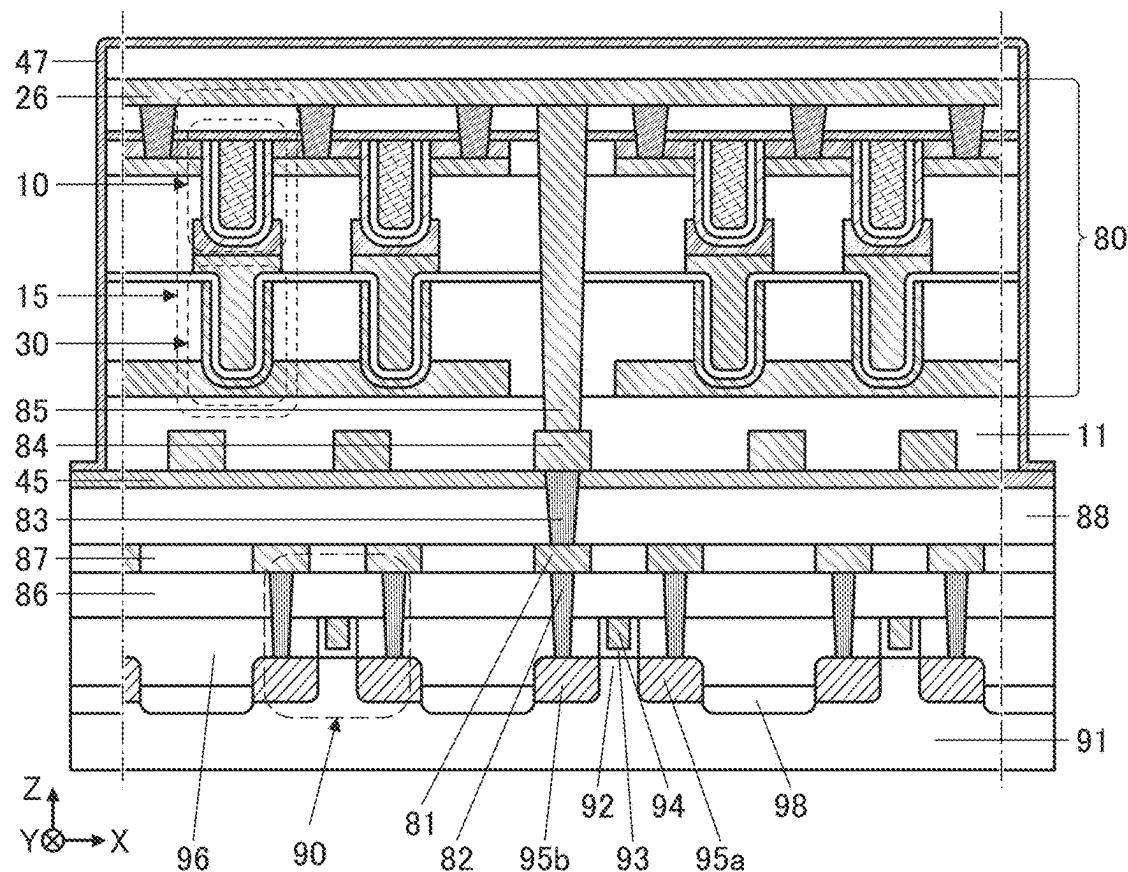


FIG. 6

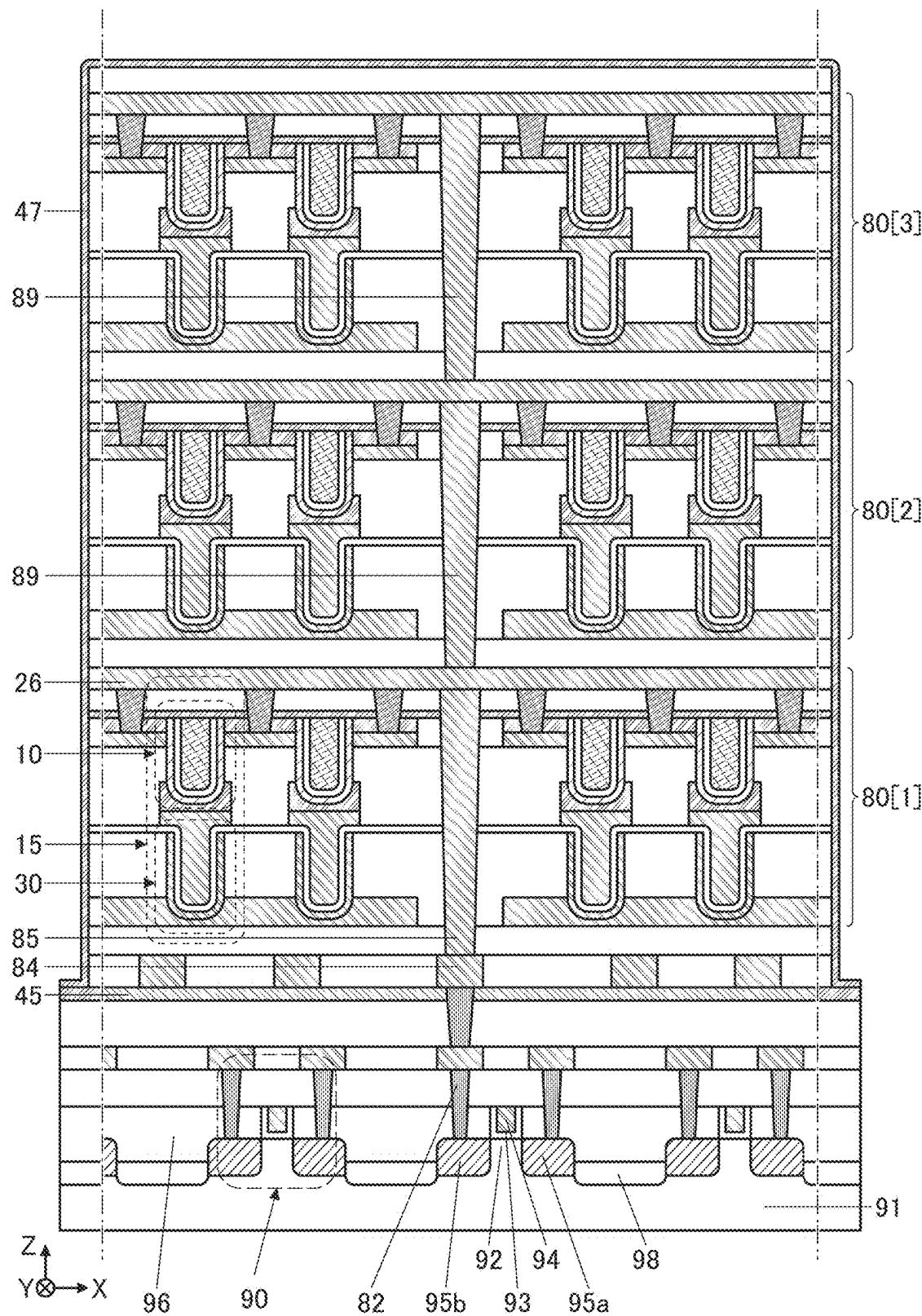


FIG. 7

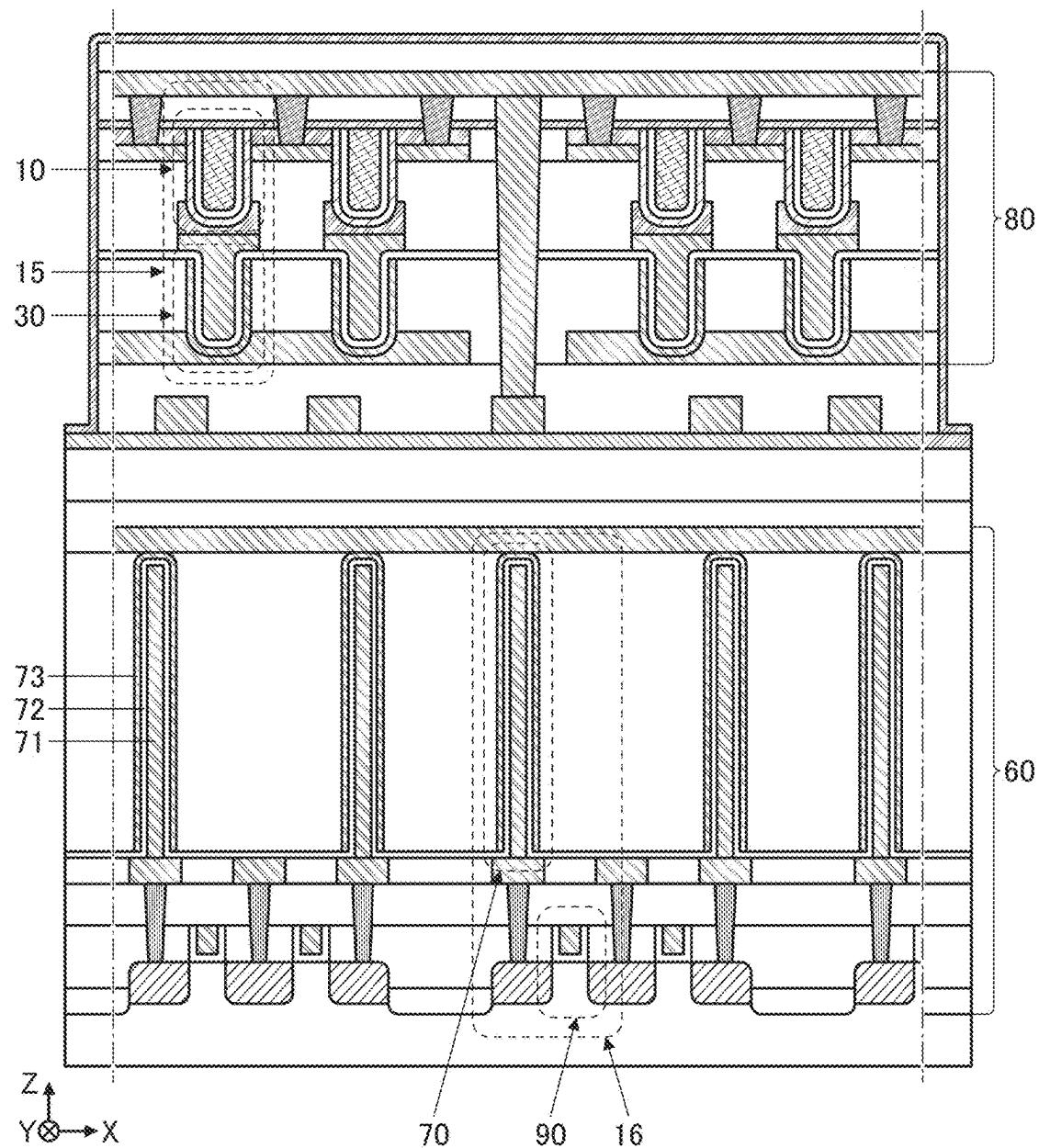


FIG. 8

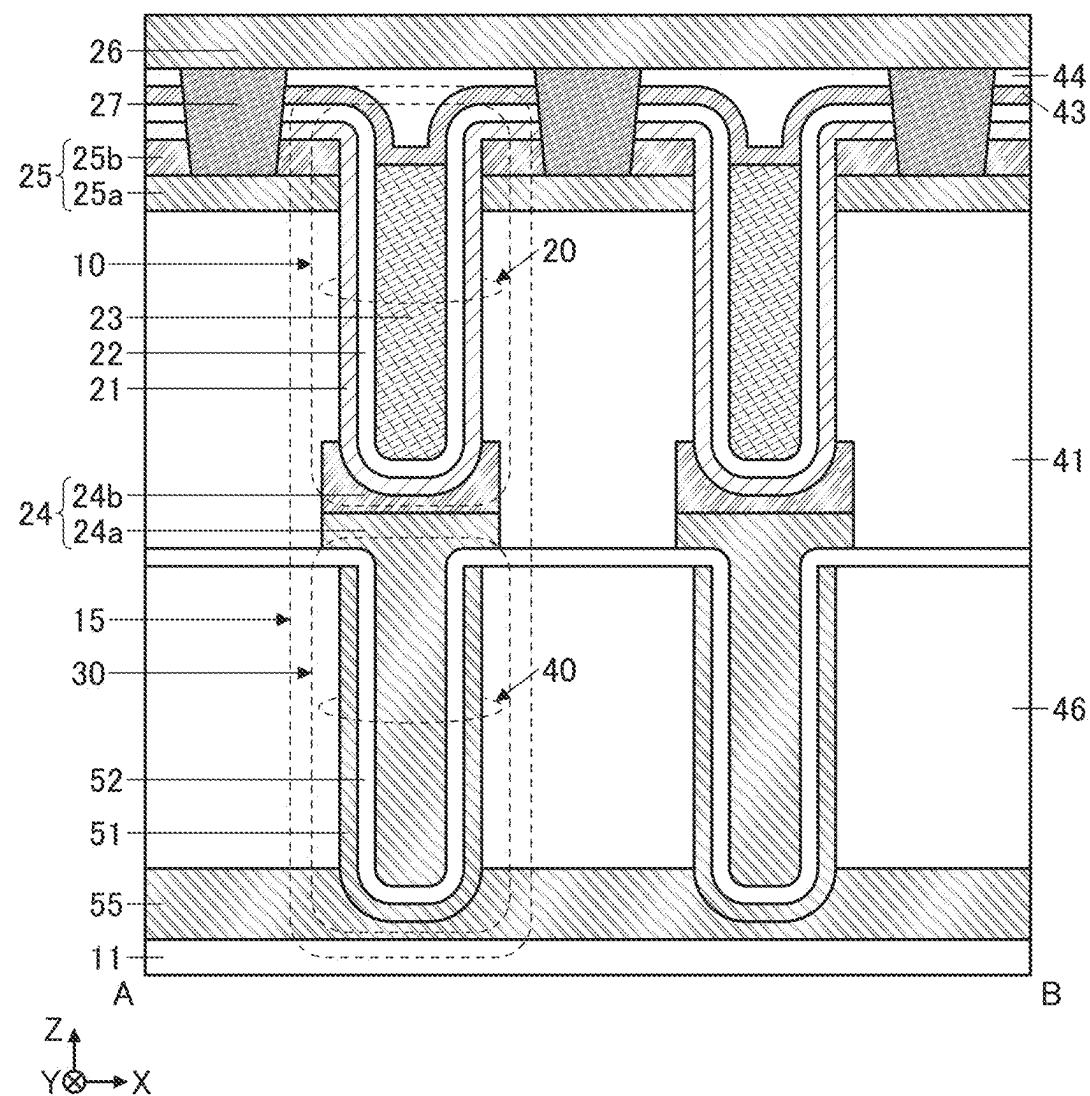


FIG. 9

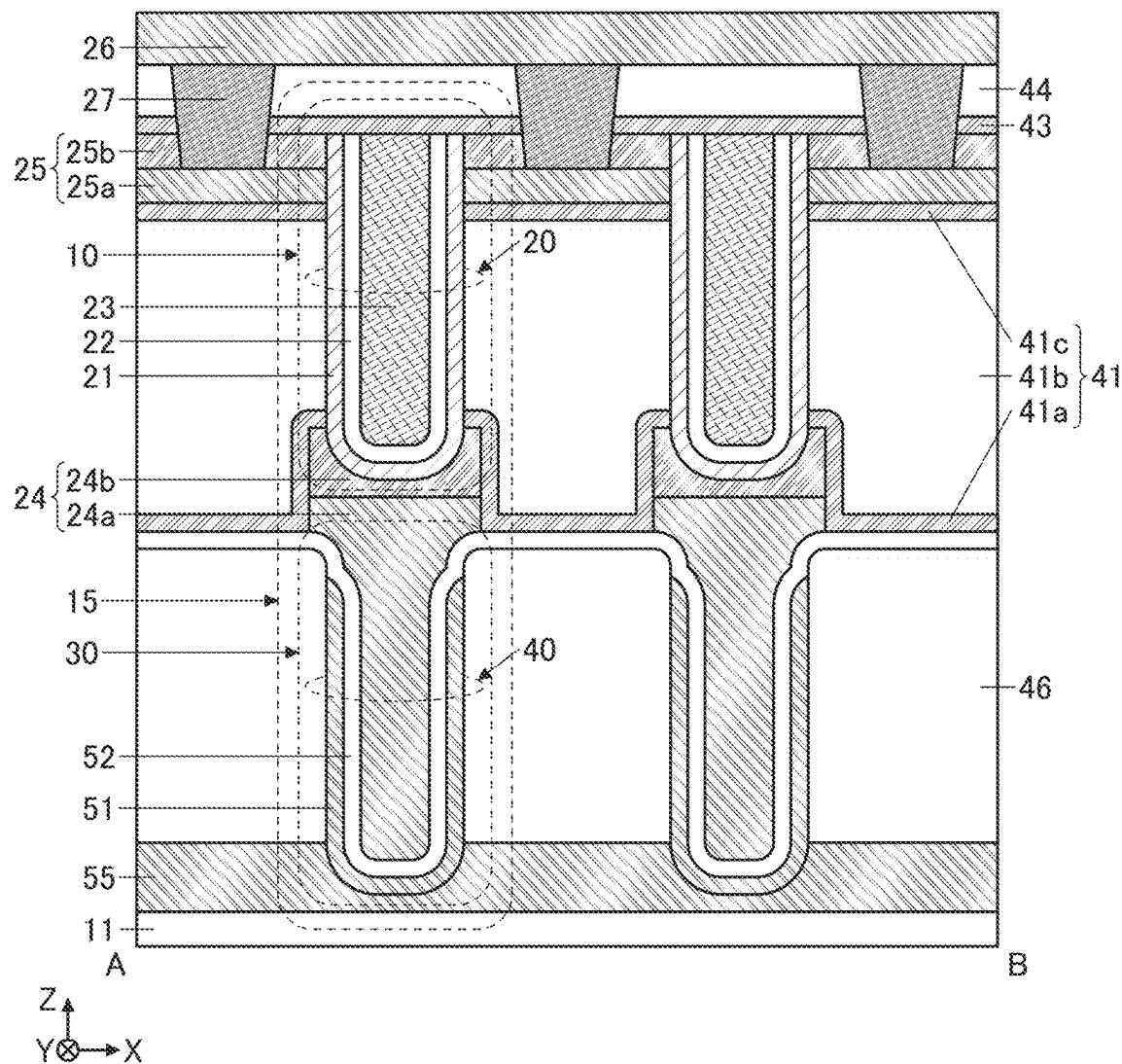


FIG. 10A

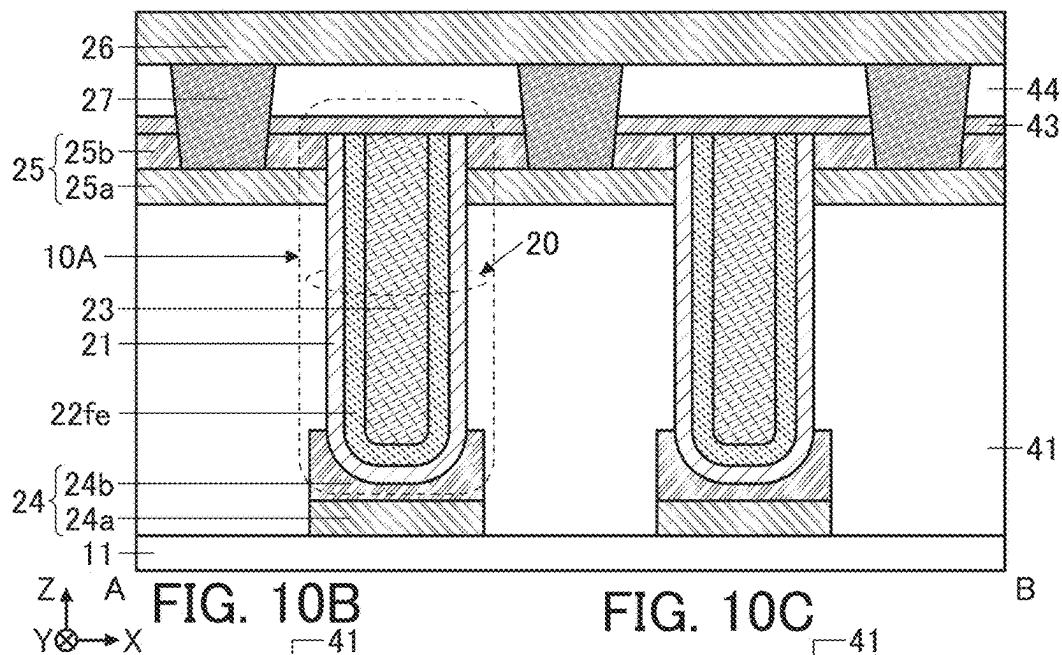


FIG. 10B

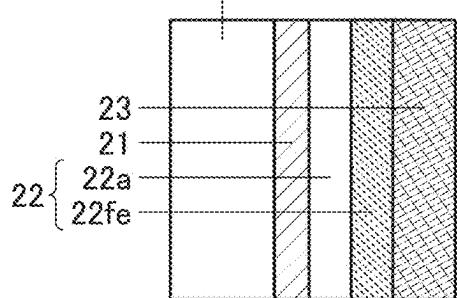


FIG. 10D

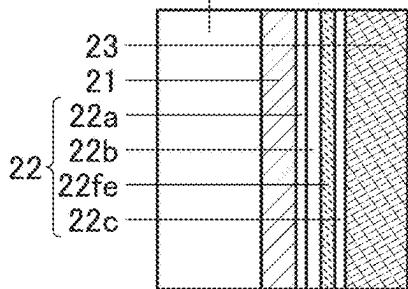


FIG. 10F

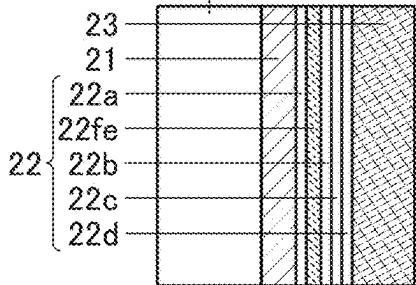


FIG. 10C

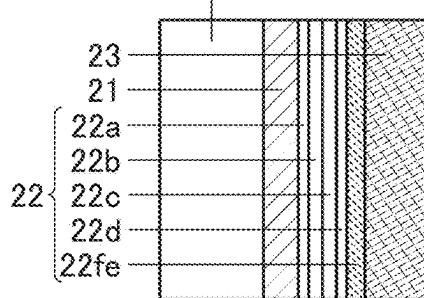


FIG. 10E

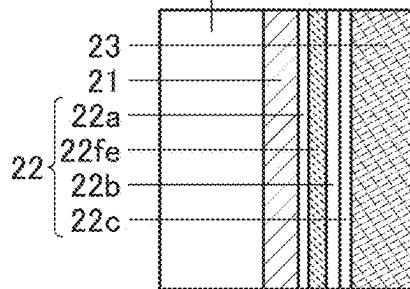


FIG. 10G

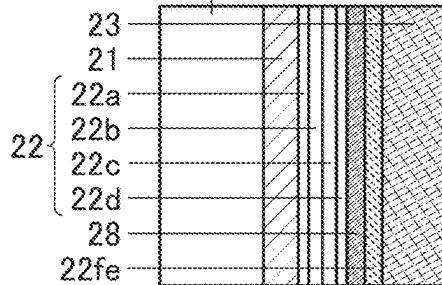


FIG. 11A

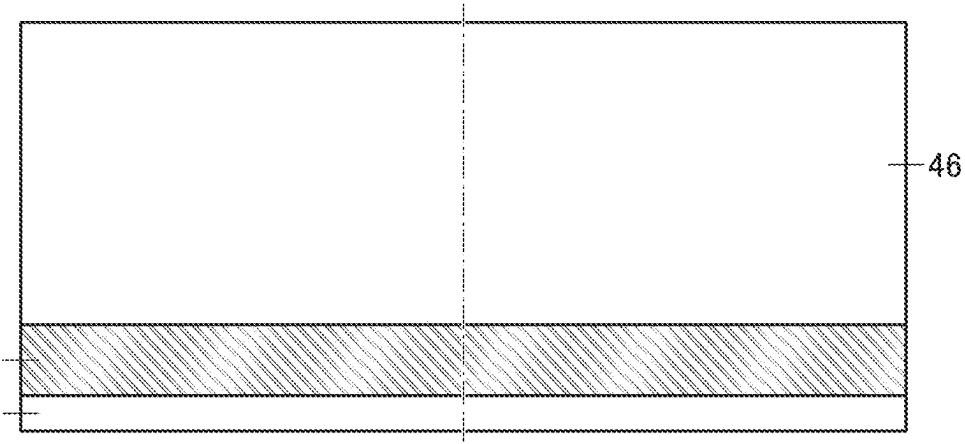


FIG. 11B

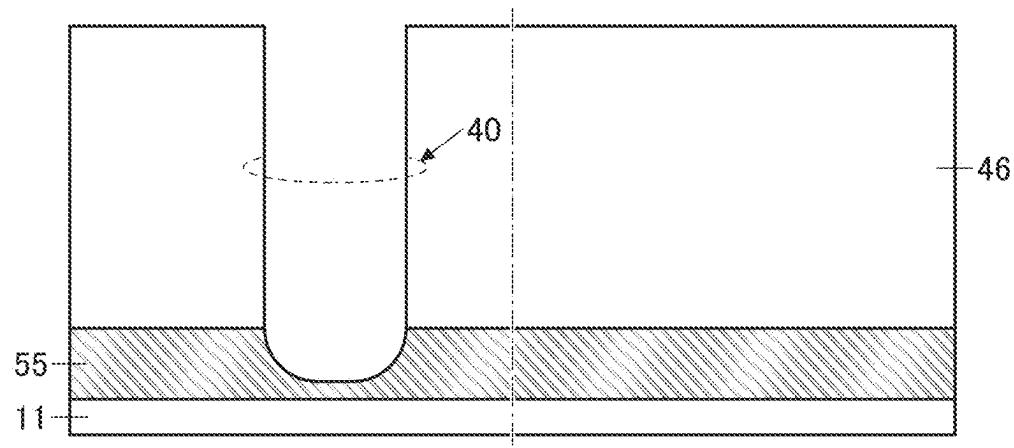


FIG. 11C

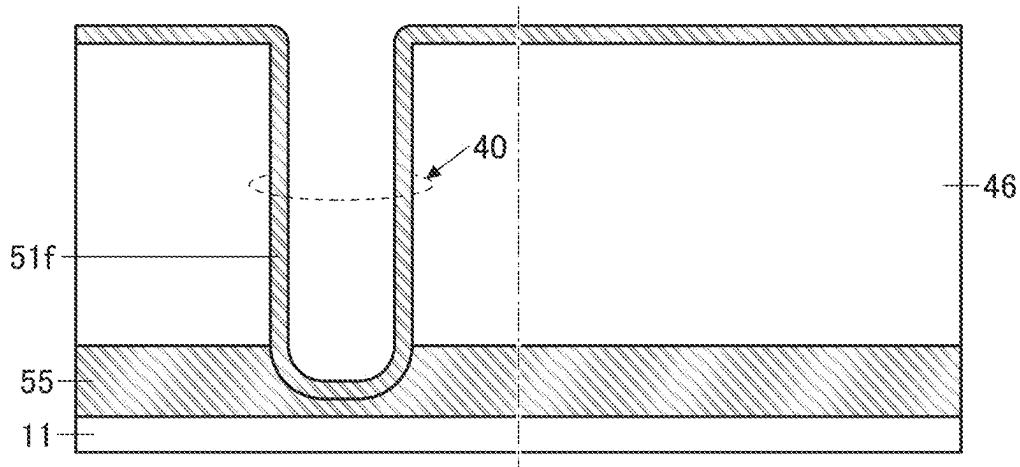


FIG. 12A

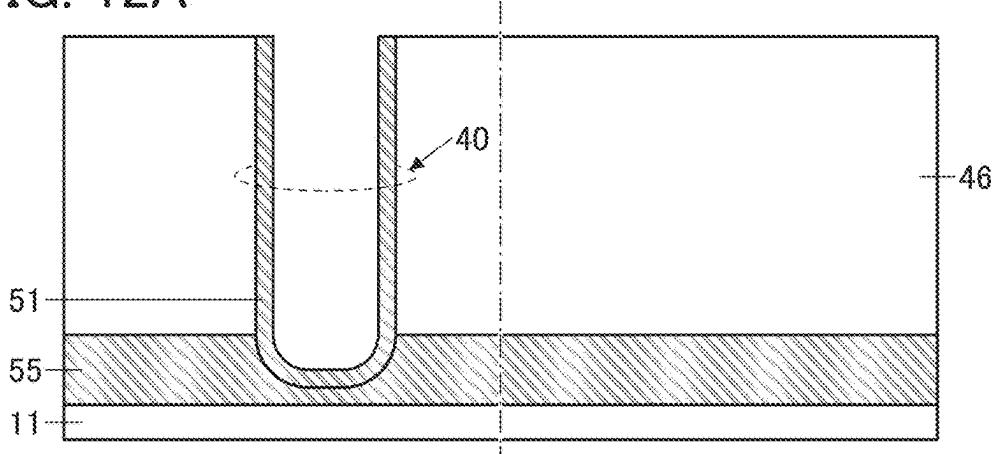


FIG. 12B

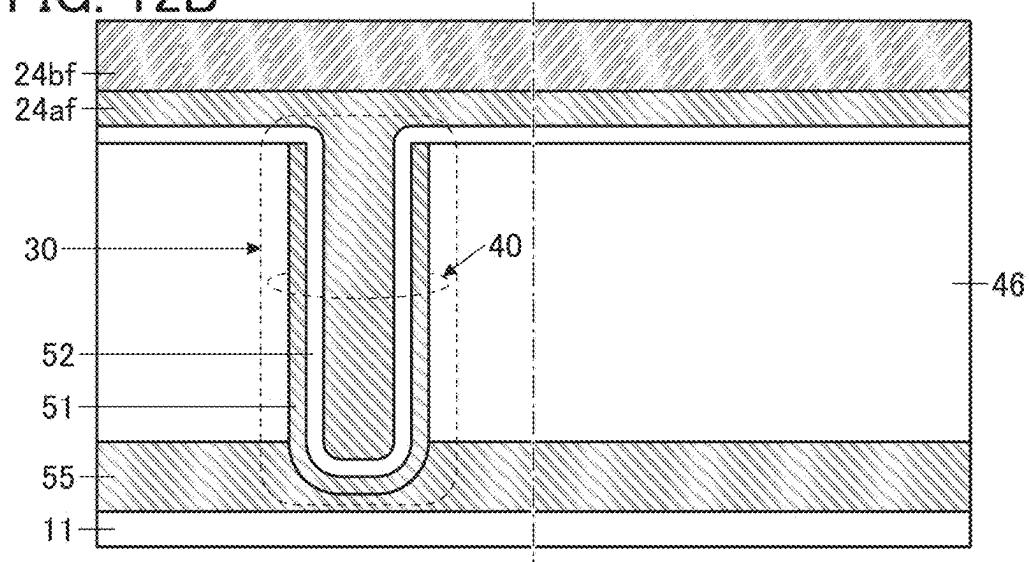


FIG. 12C

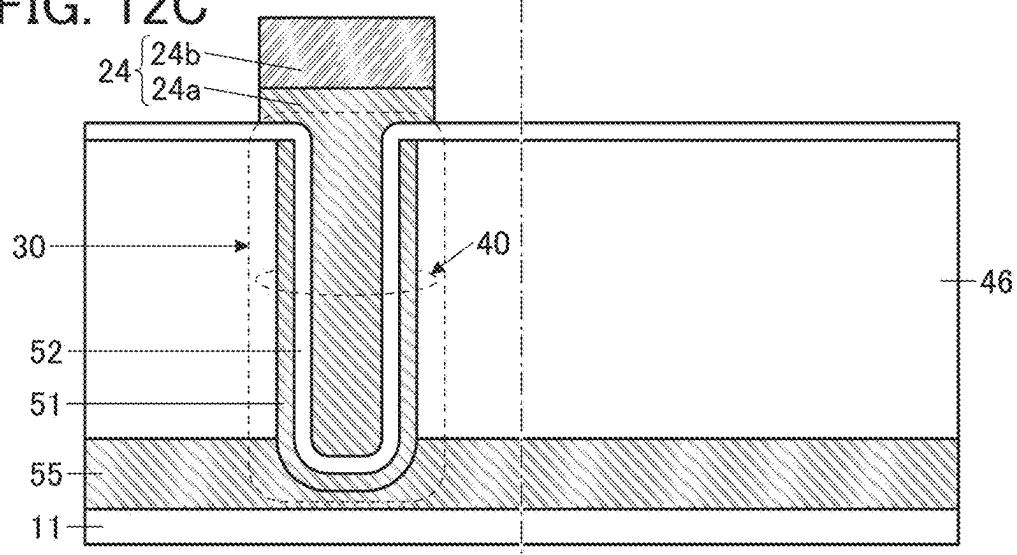


FIG. 13A

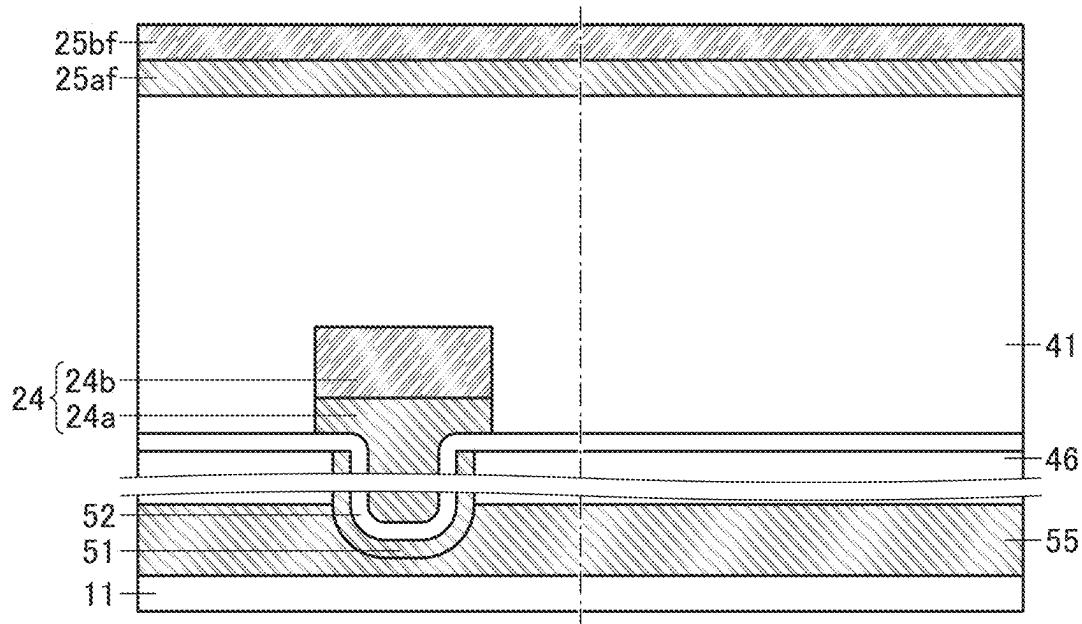


FIG. 13B

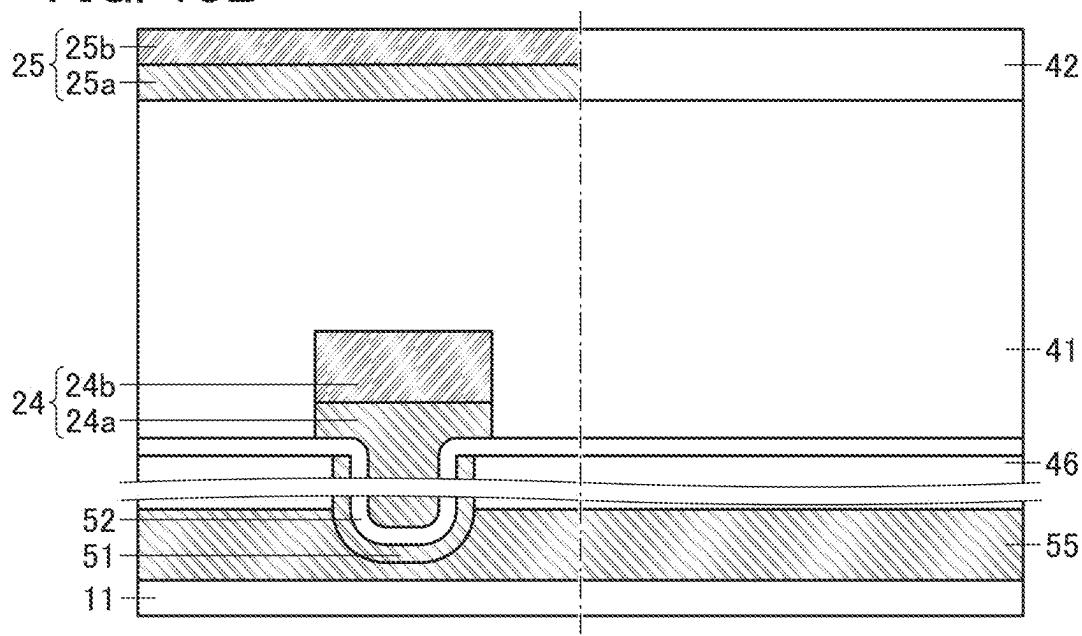


FIG. 14A

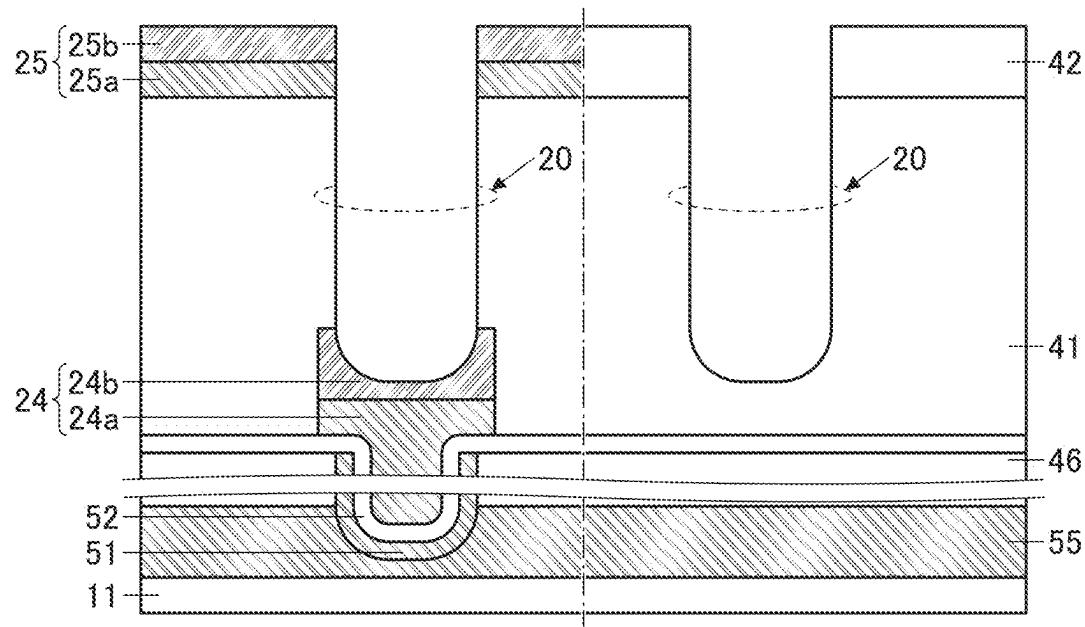


FIG. 14B

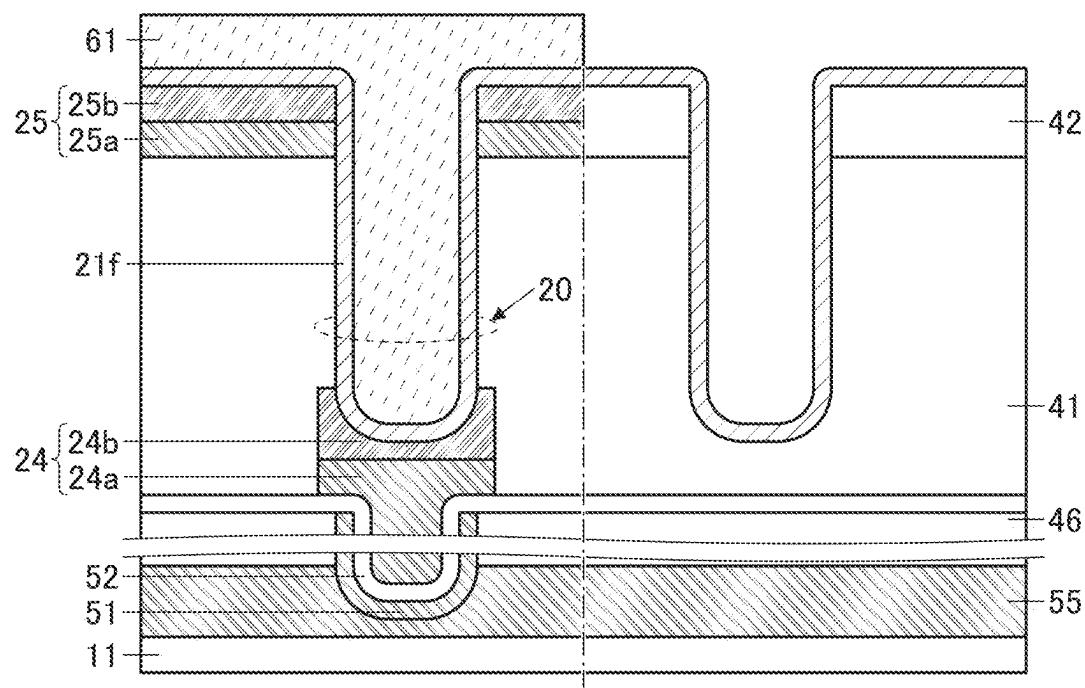


FIG. 15A

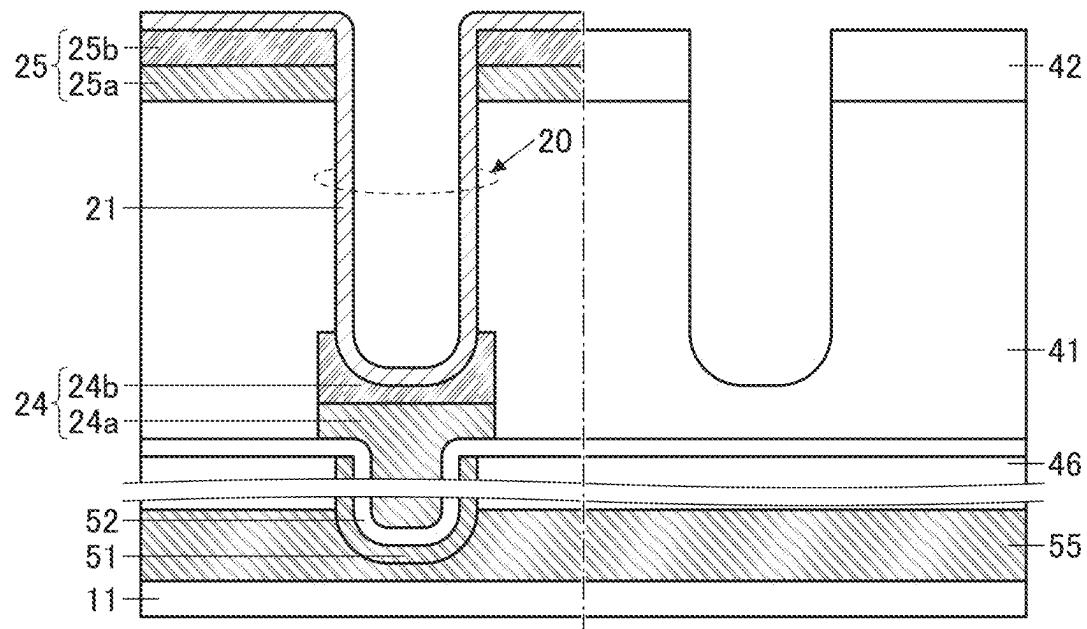


FIG. 15B

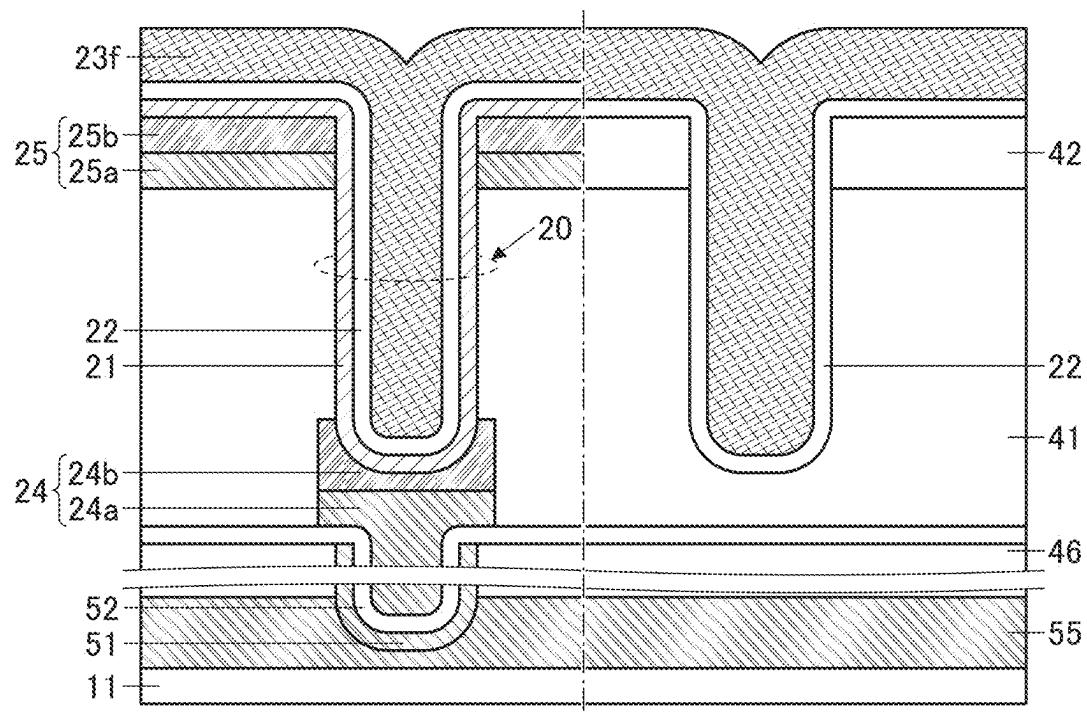


FIG. 16A

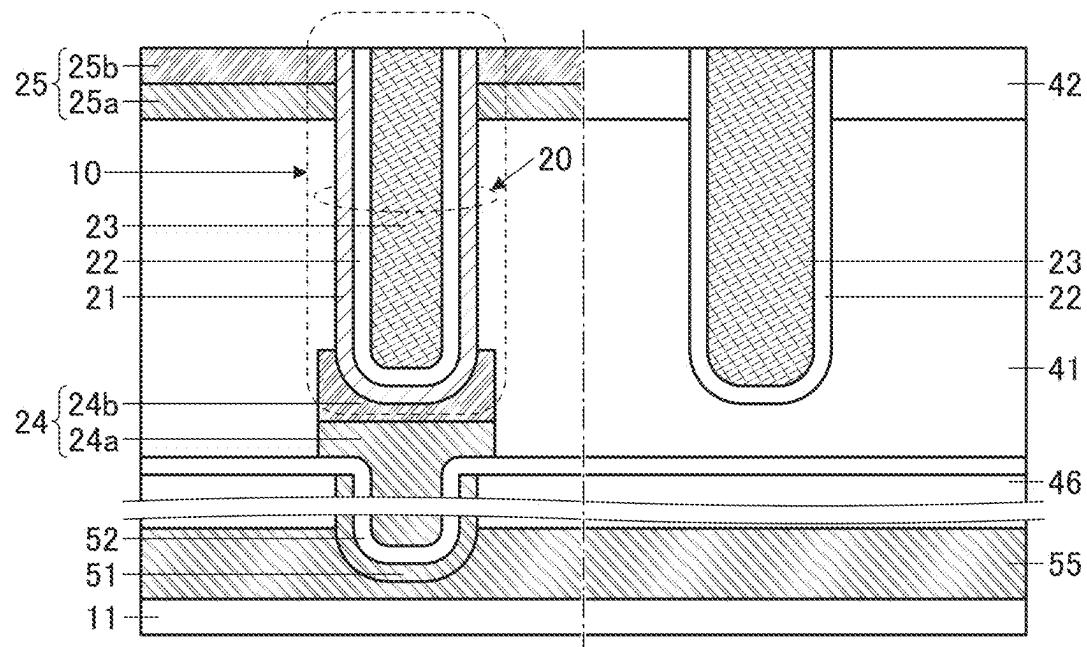


FIG. 16B

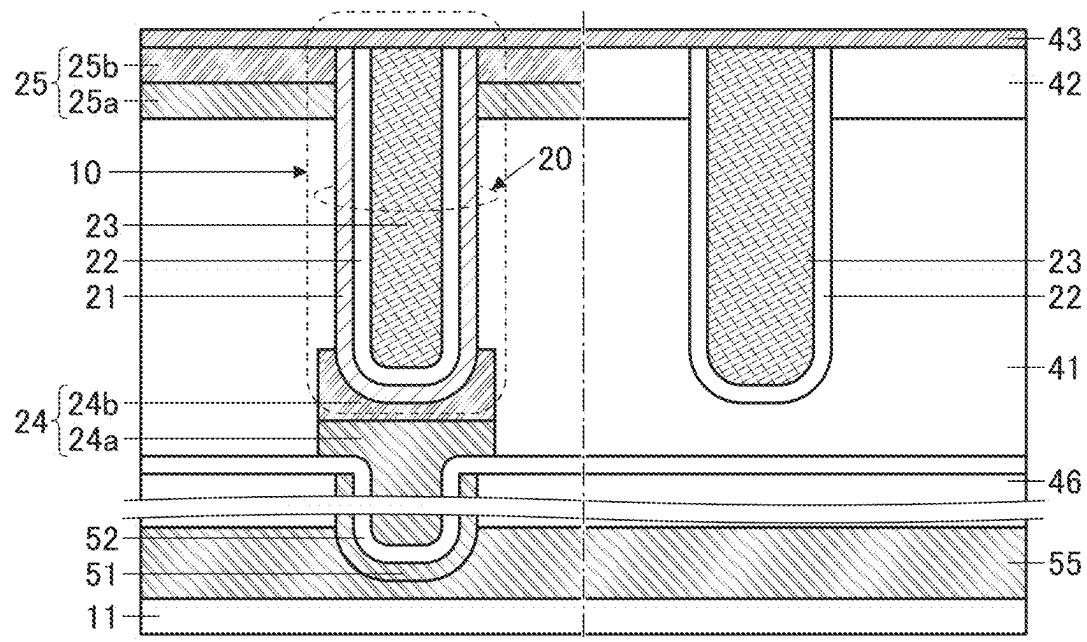


FIG. 17A

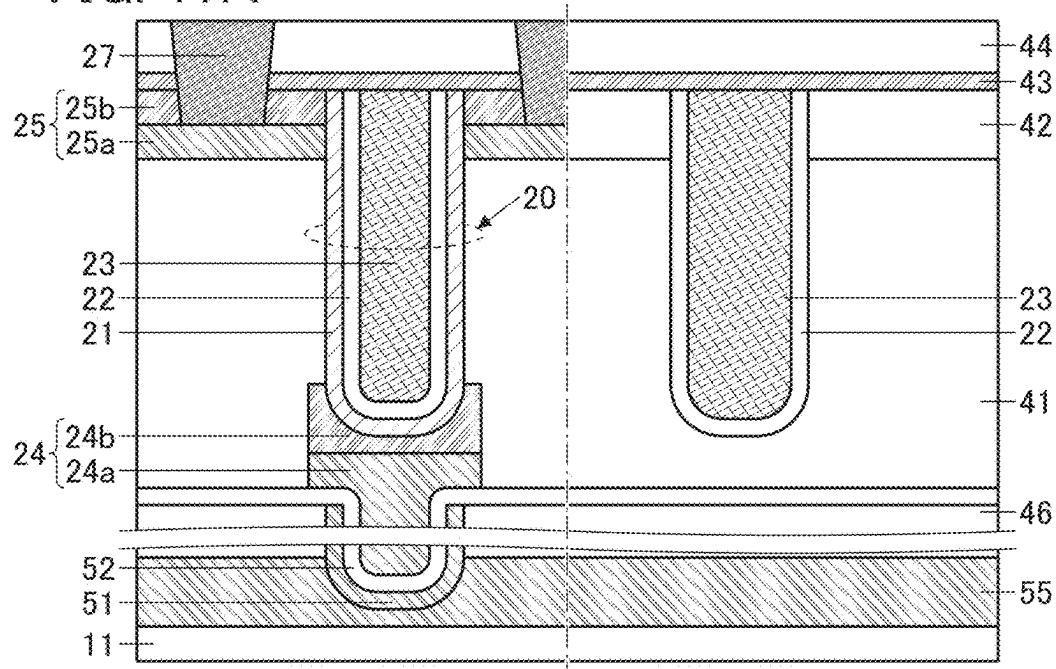


FIG. 17B

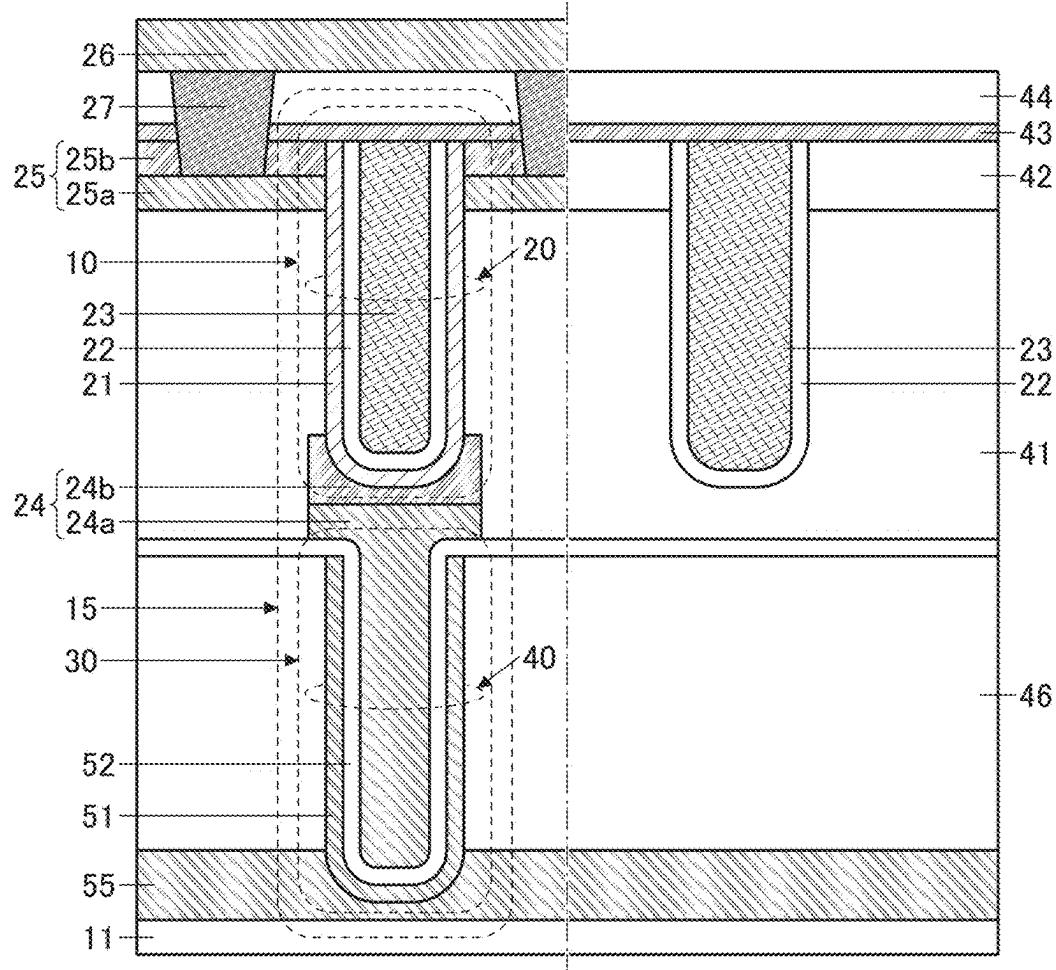


FIG. 18  
900

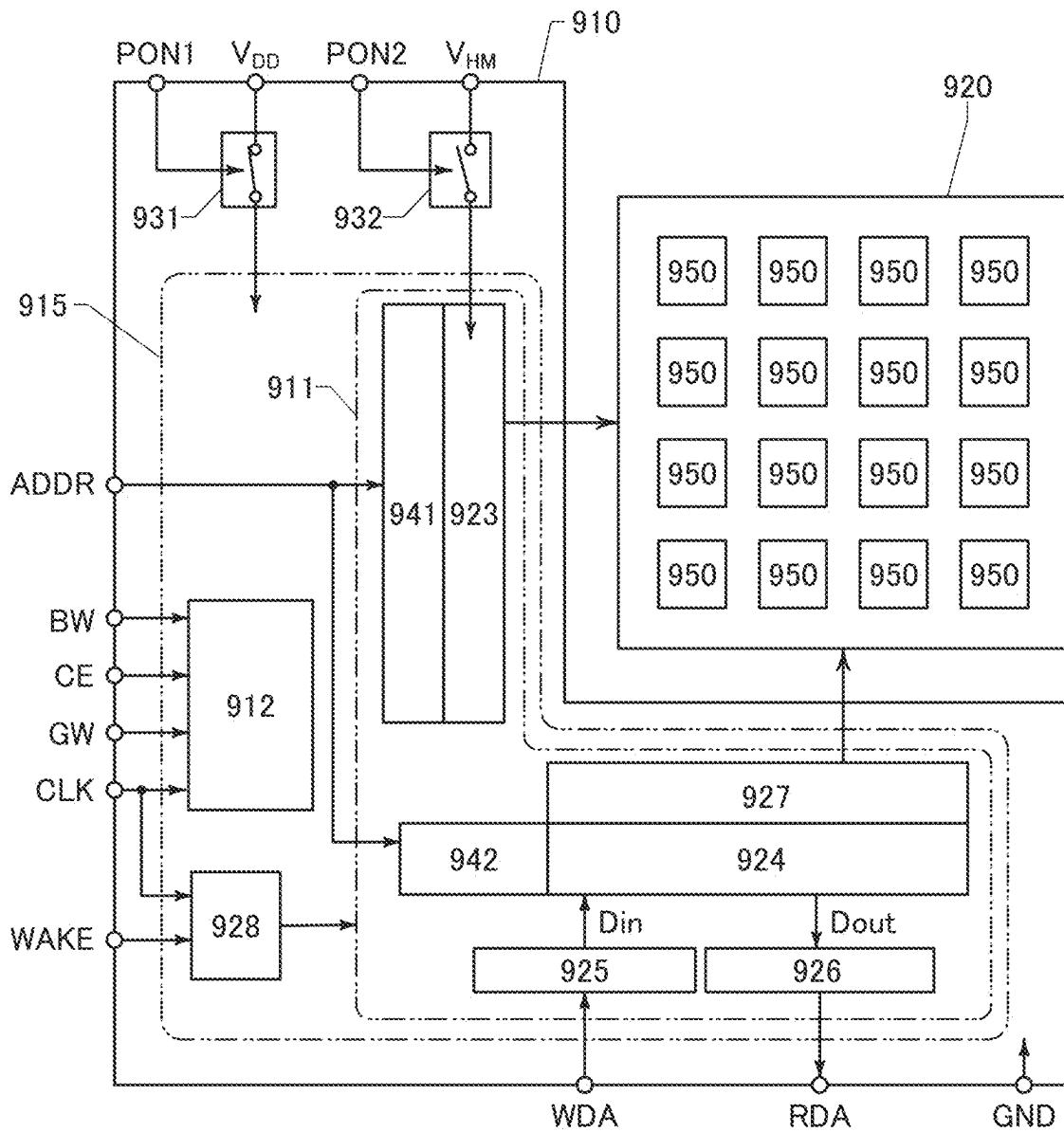


FIG. 19A

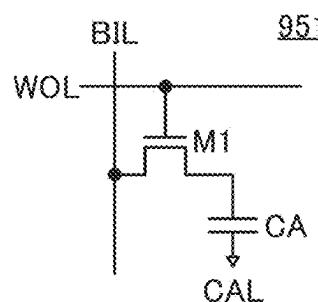


FIG. 19B

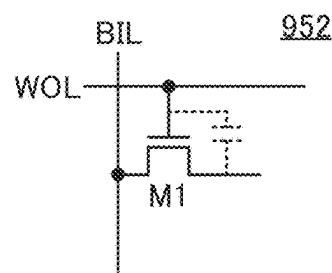


FIG. 19C

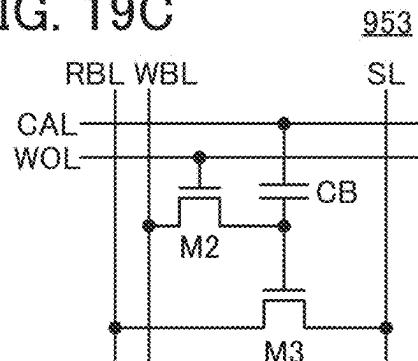


FIG. 19D

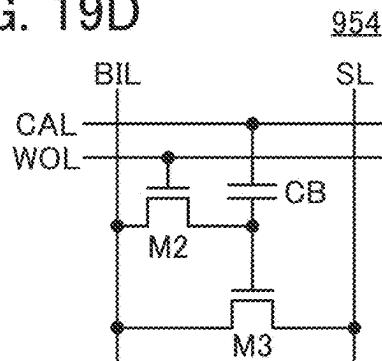


FIG. 19E

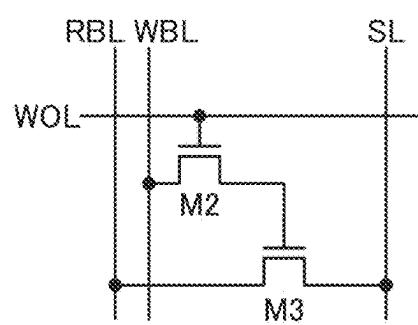


FIG. 19F

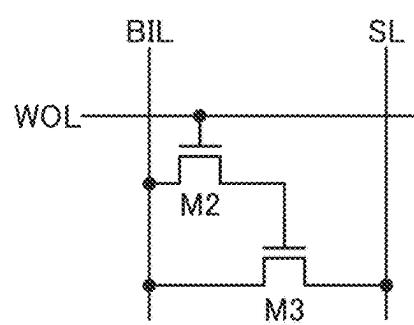


FIG. 19G

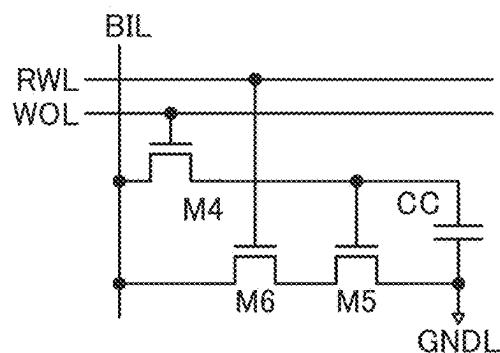


FIG. 19H

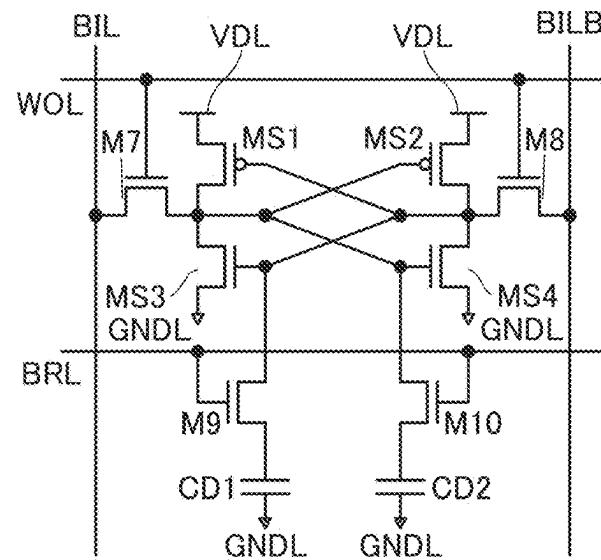


FIG. 20A

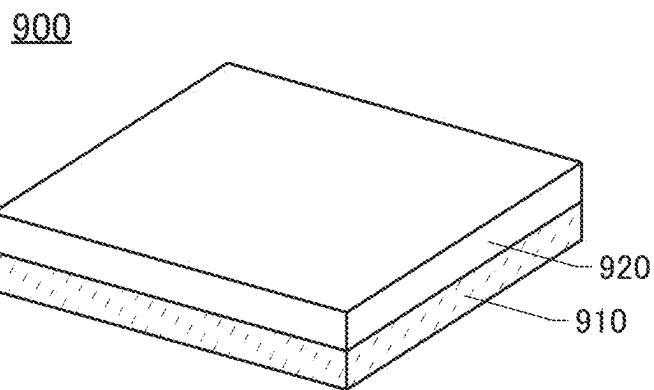


FIG. 20B

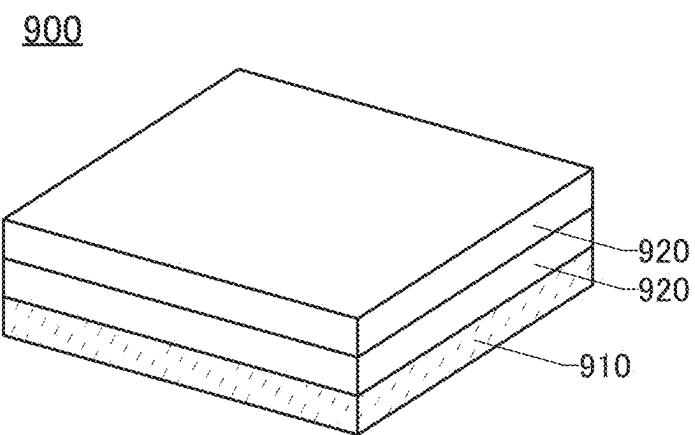


FIG. 21

960

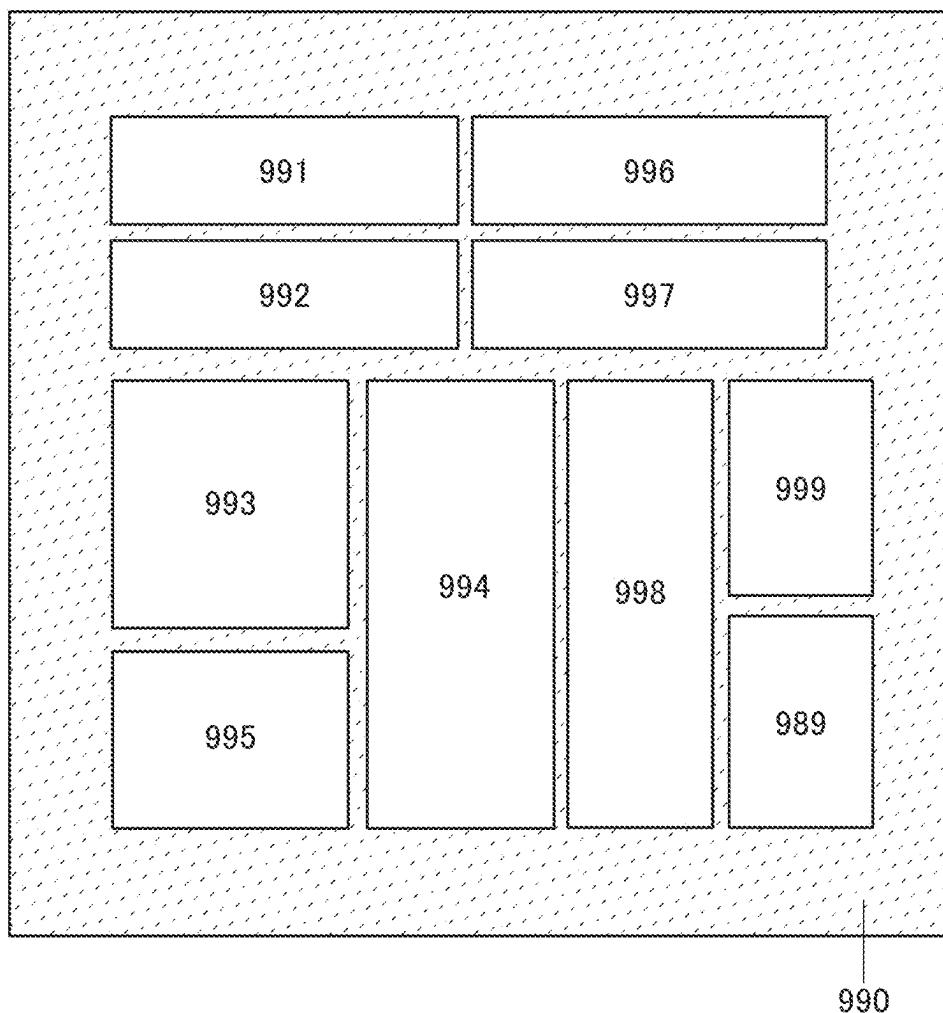


FIG. 22A

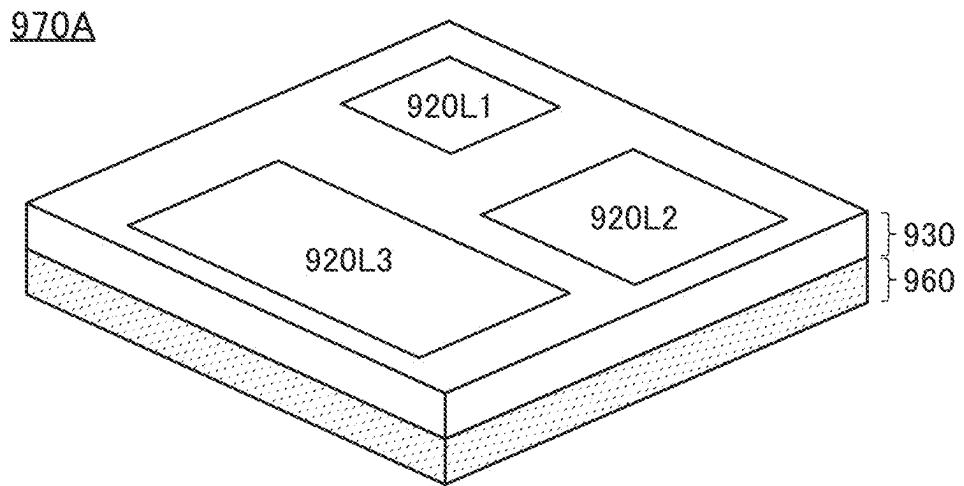


FIG. 22B

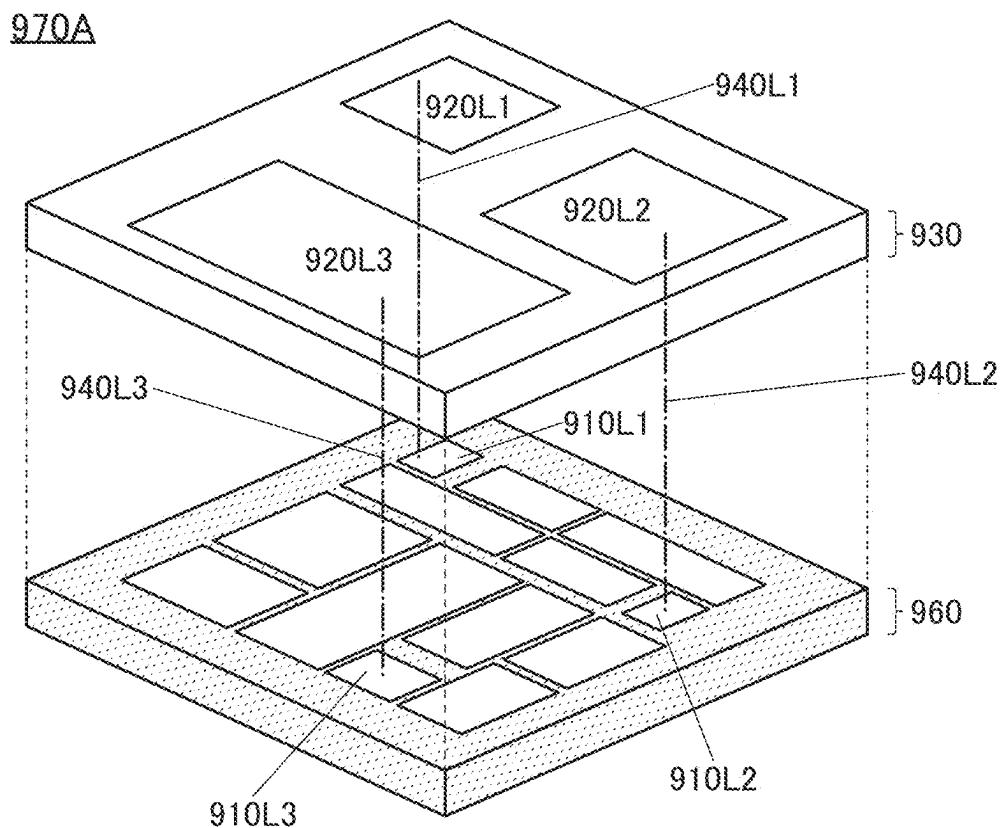


FIG. 23A

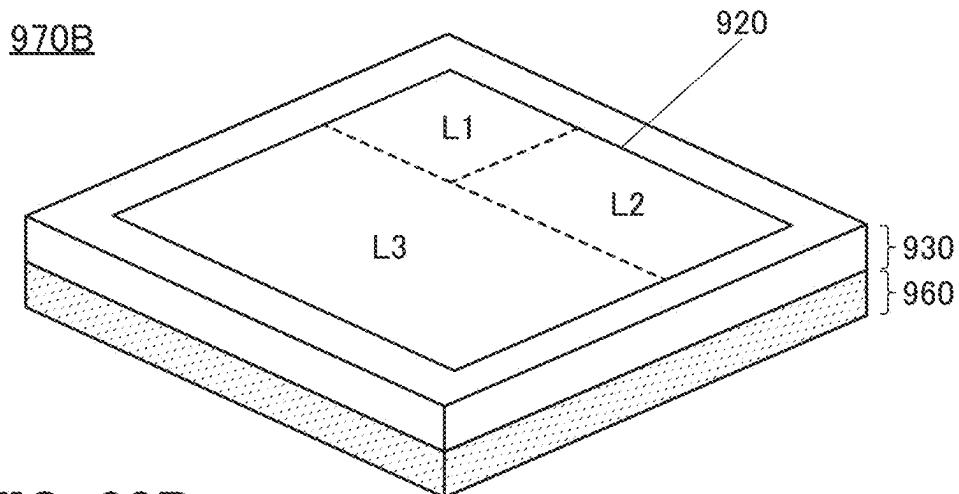


FIG. 23B

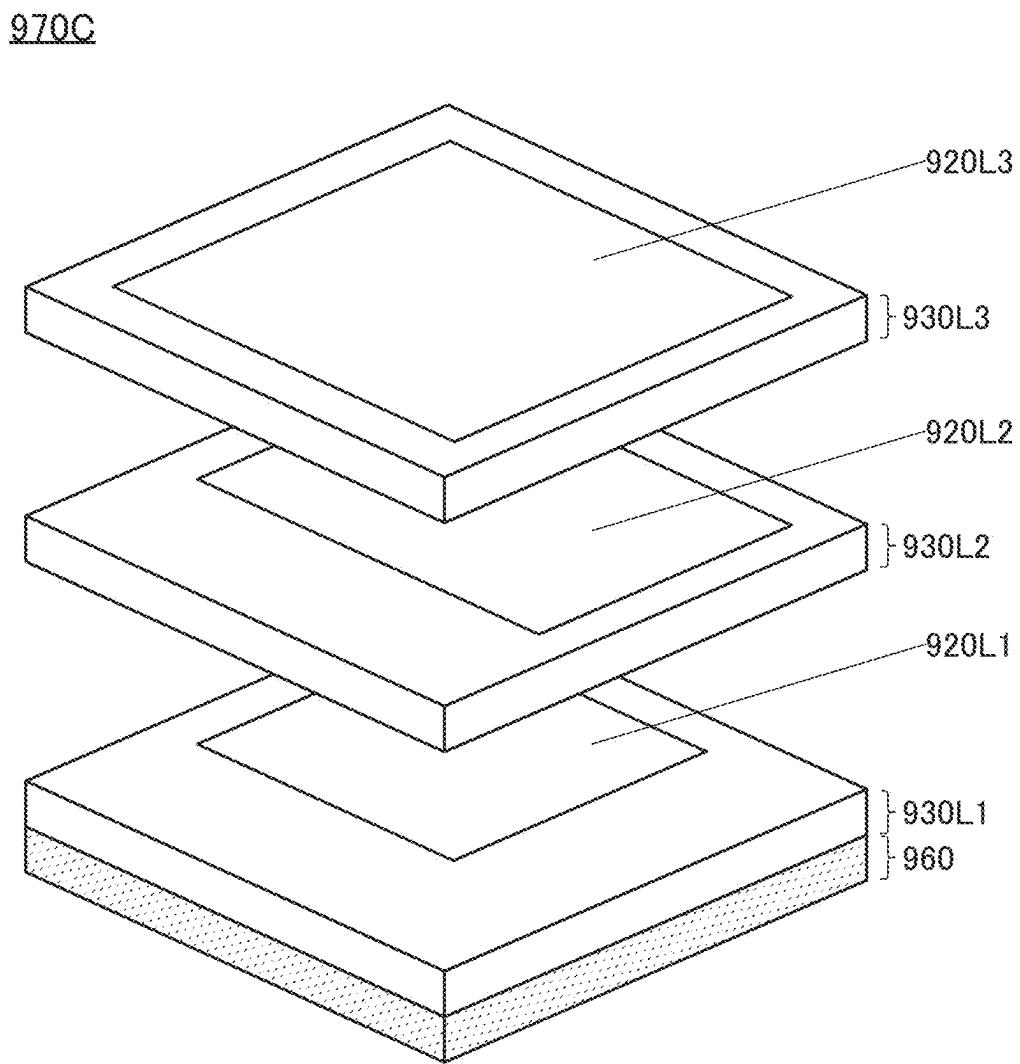


FIG. 24

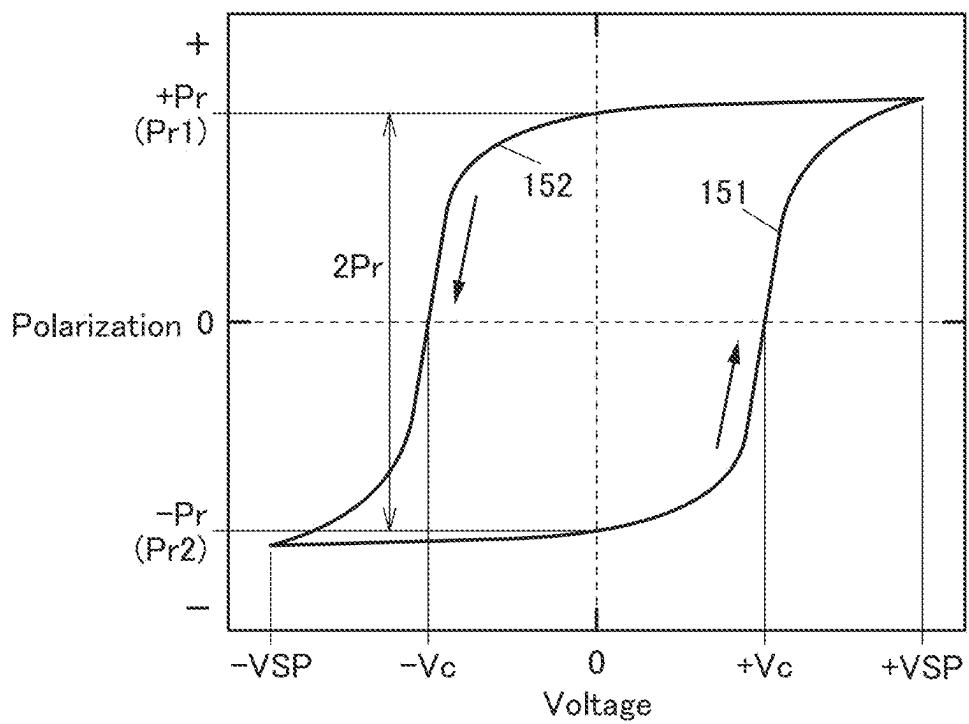


FIG. 25A

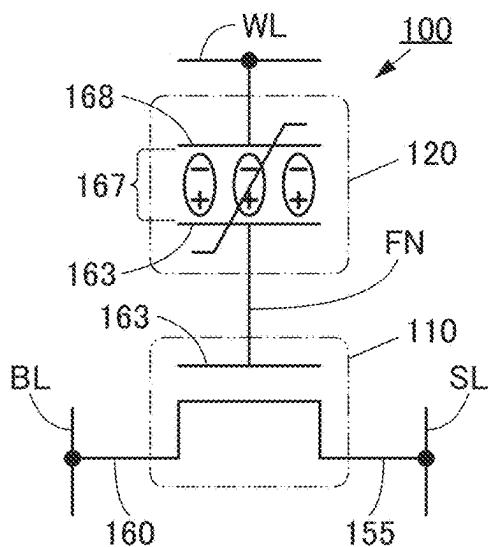


FIG. 25B

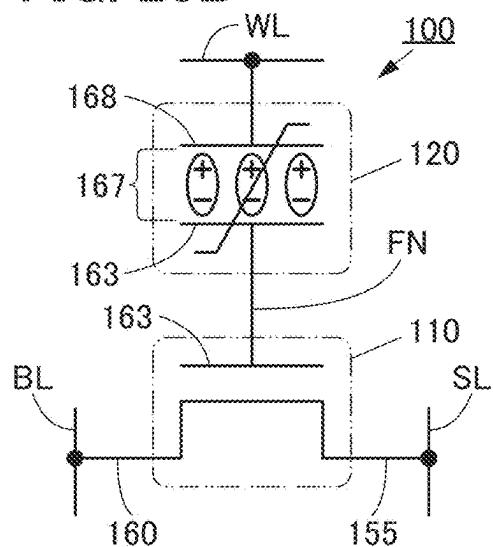


FIG. 25C

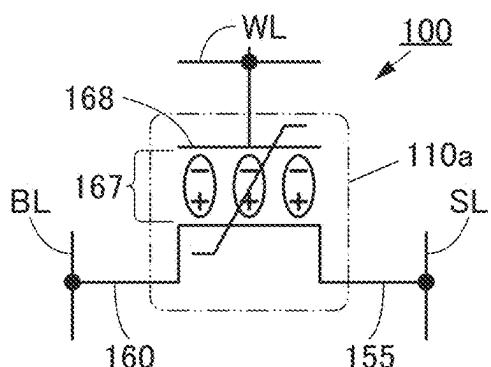


FIG. 25D

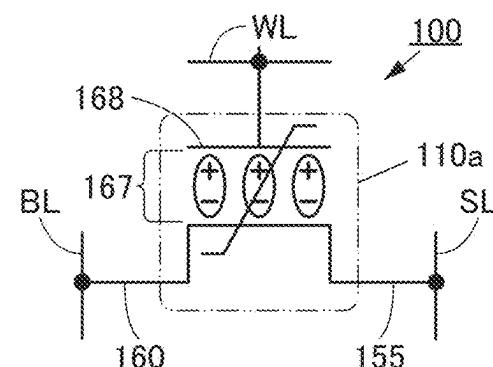


FIG. 25E

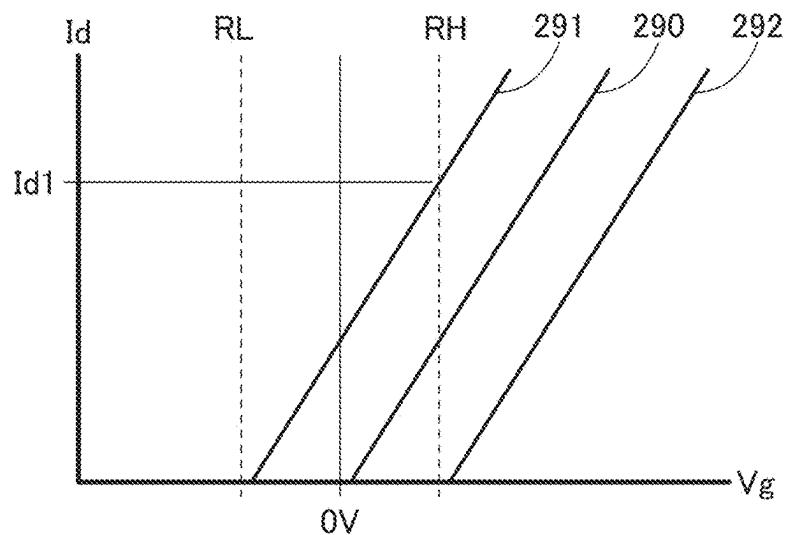


FIG. 26A

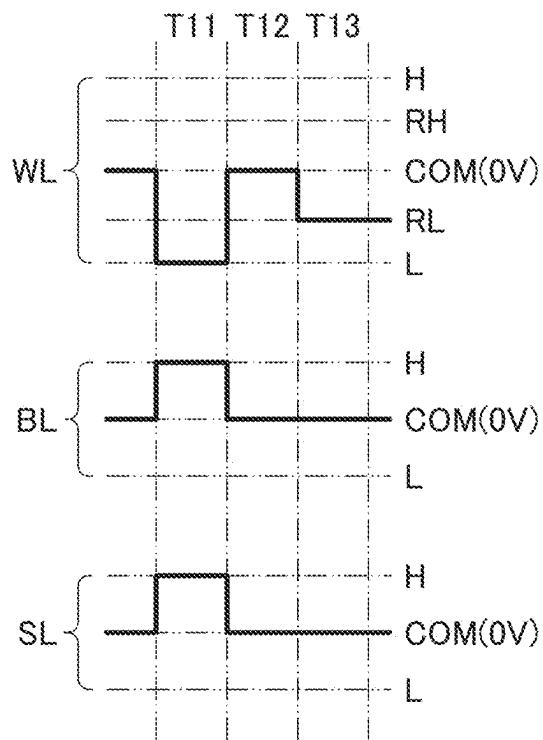


FIG. 26B

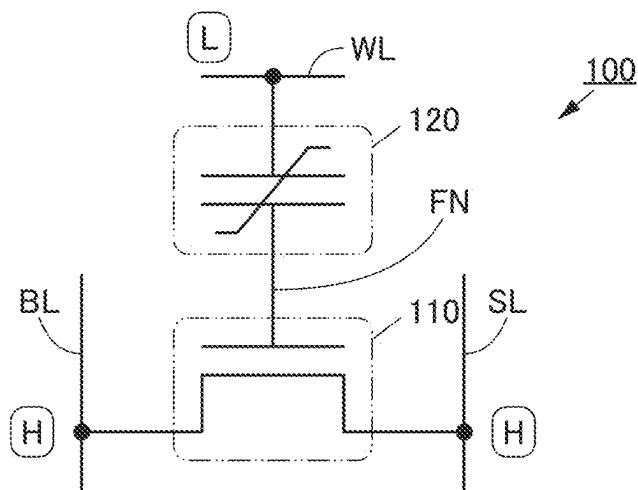


FIG. 27A

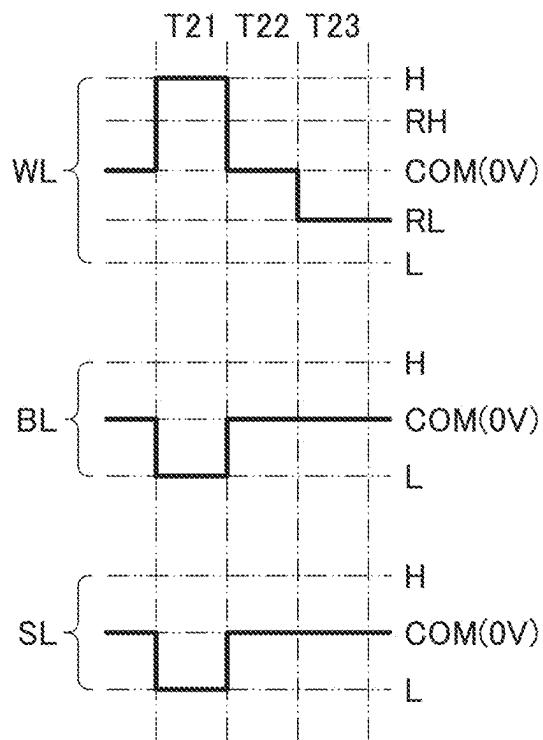


FIG. 27B

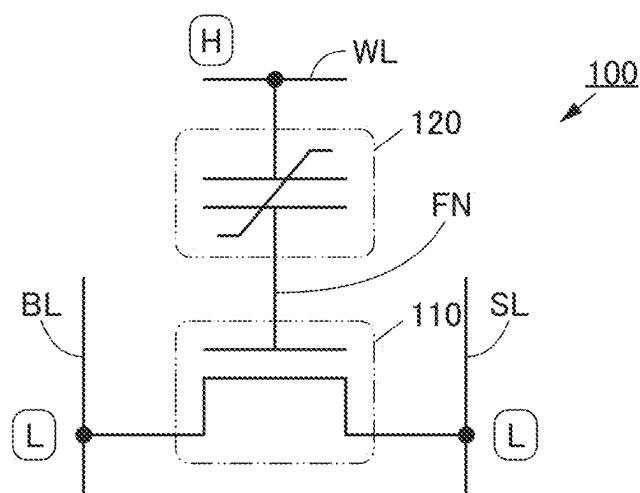


FIG. 28A

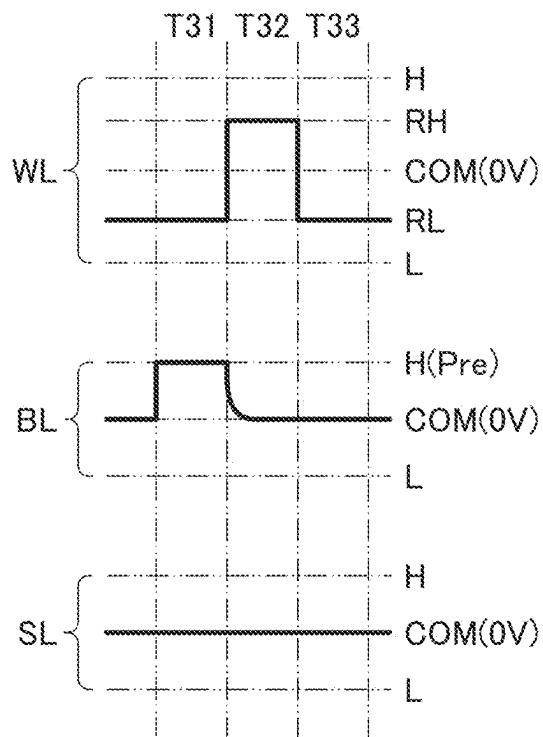


FIG. 28B

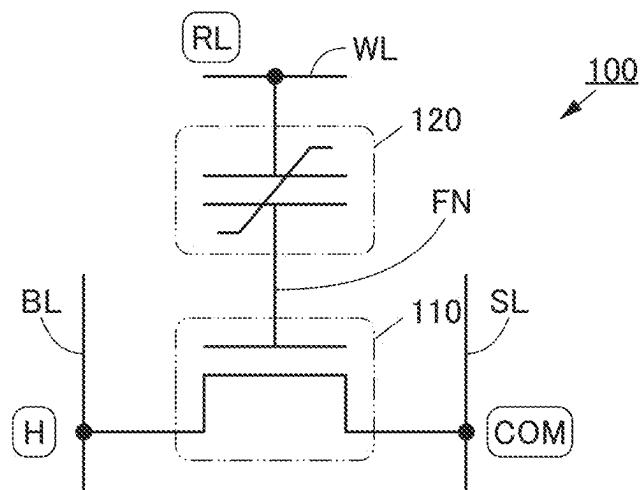


FIG. 29A

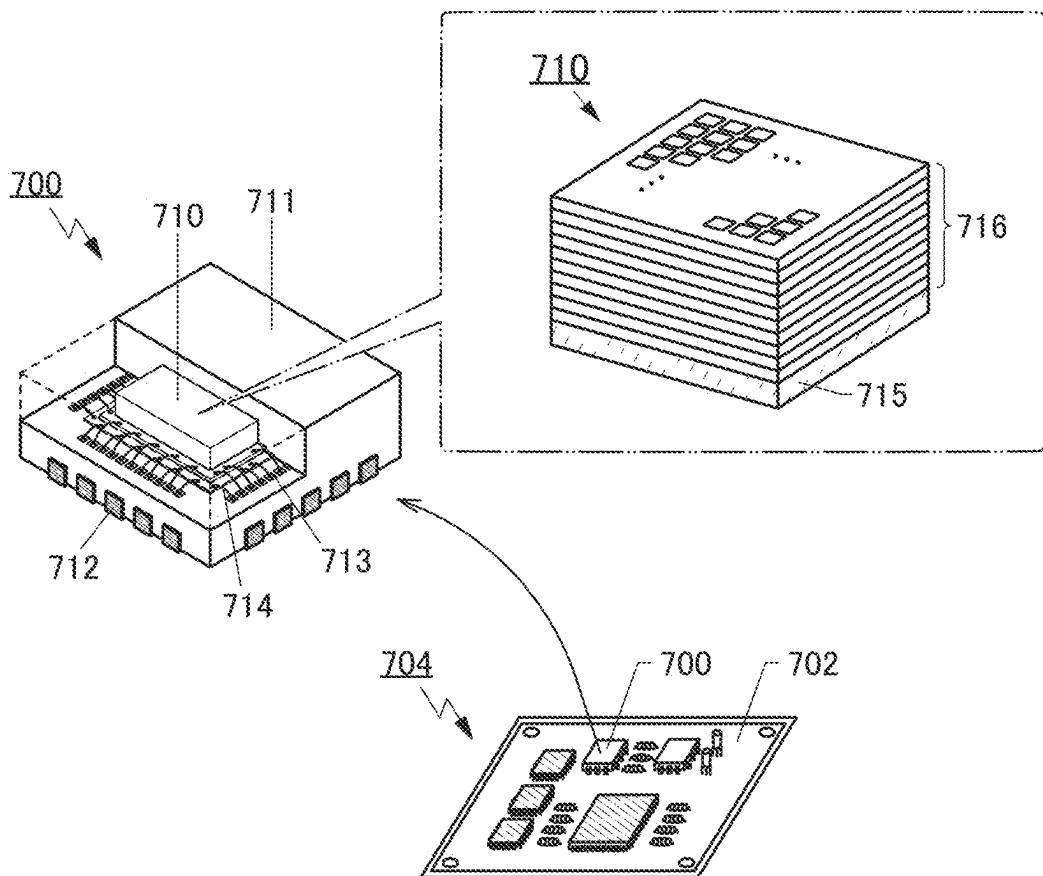


FIG. 29B

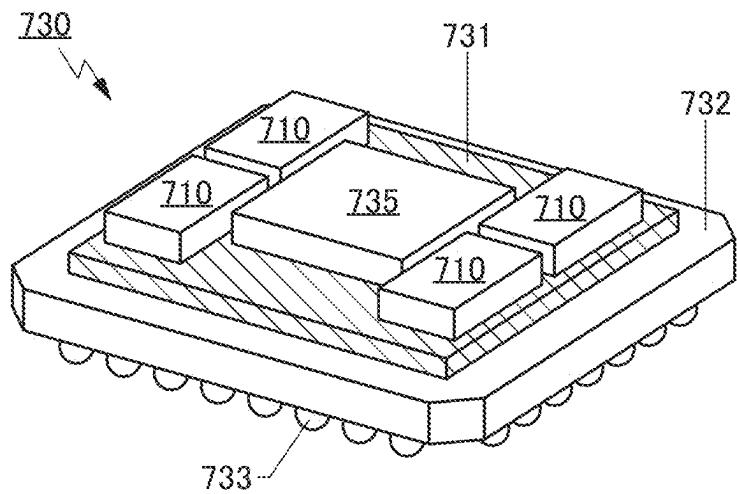


FIG. 30A

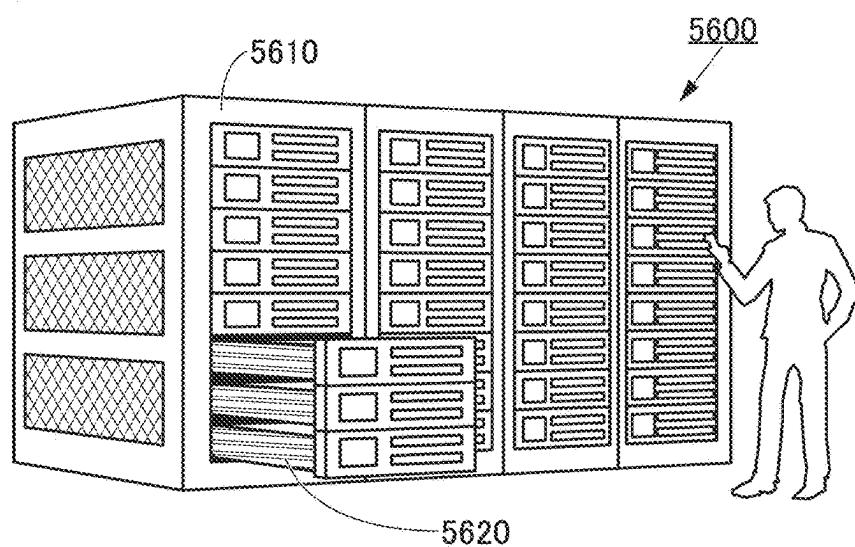


FIG. 30B

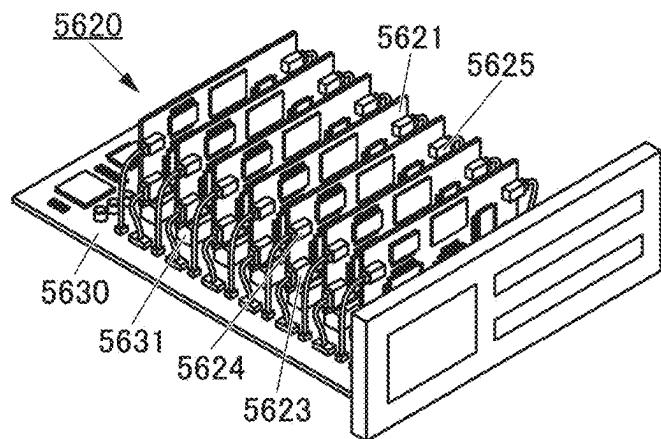


FIG. 30C

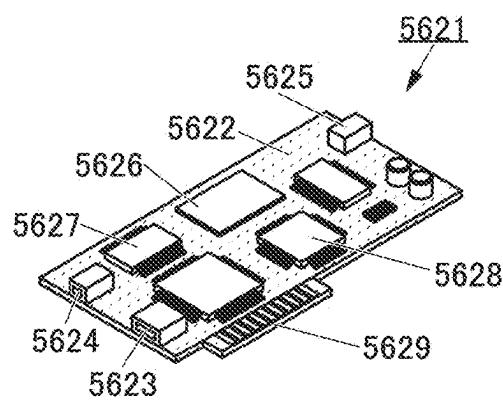


FIG. 31A

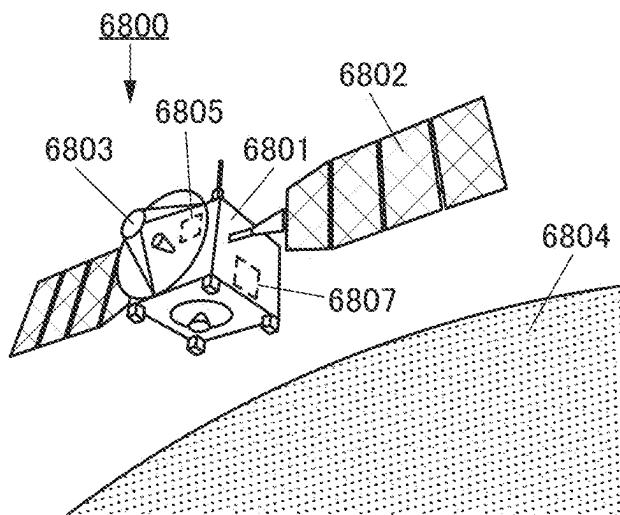


FIG. 31B

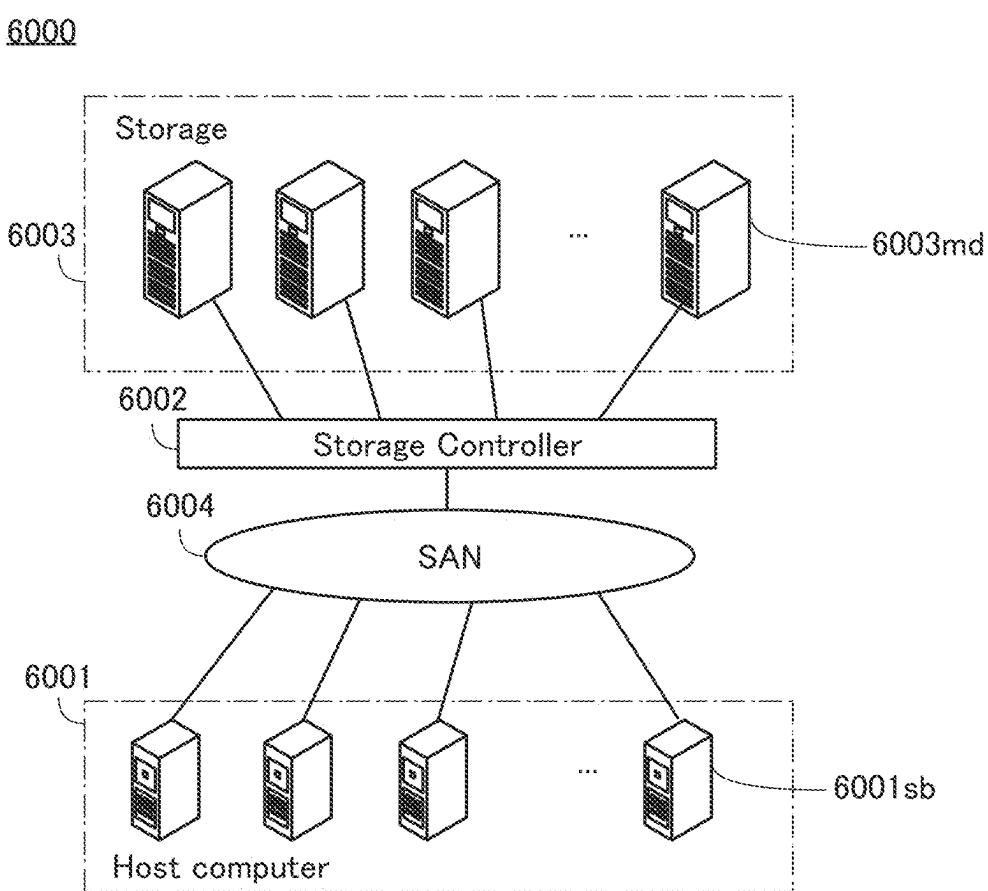


FIG. 32A

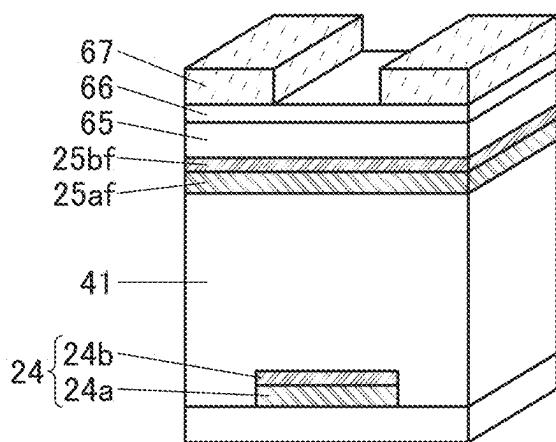


FIG. 32B

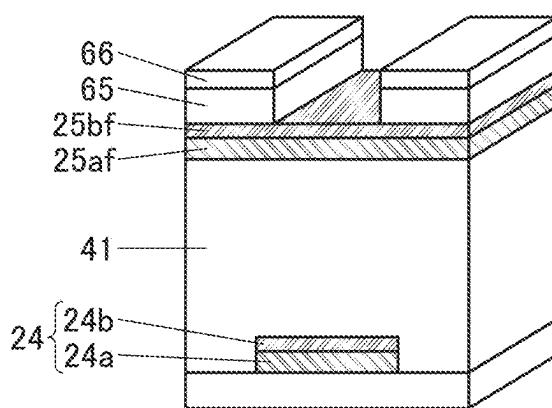


FIG. 32C

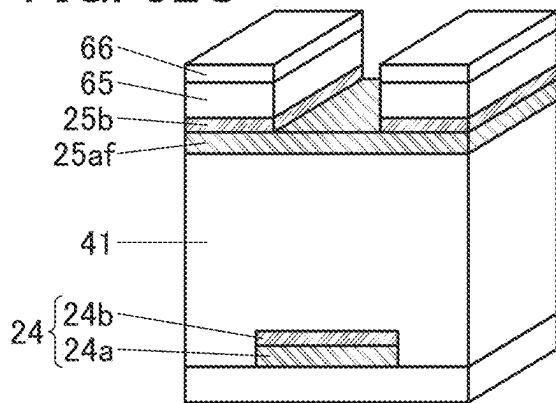


FIG. 32D

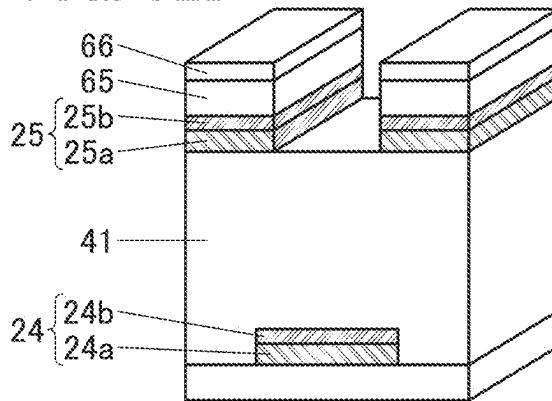
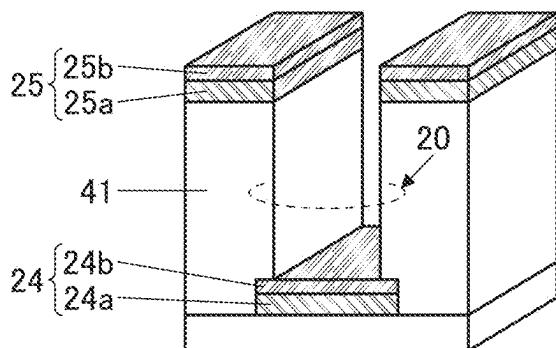
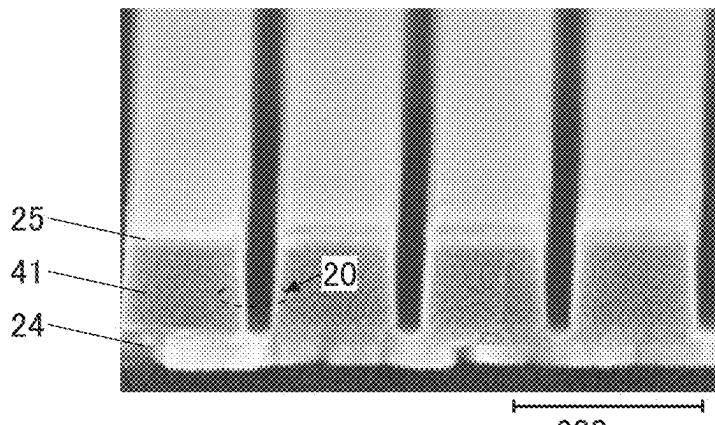


FIG. 32E



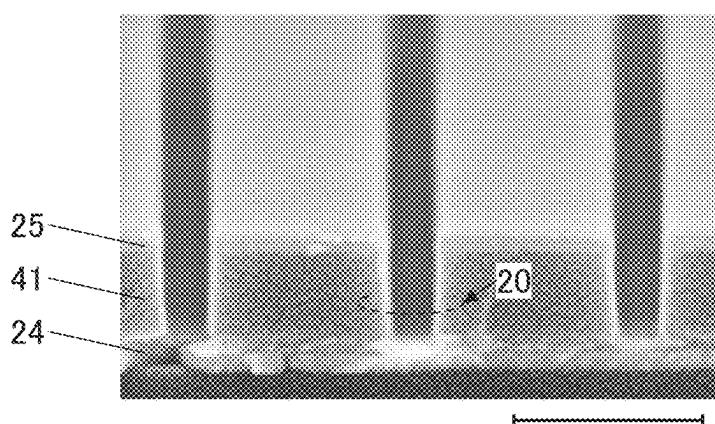
**FIG. 33A**

Line/Space 40 nm/120 nm



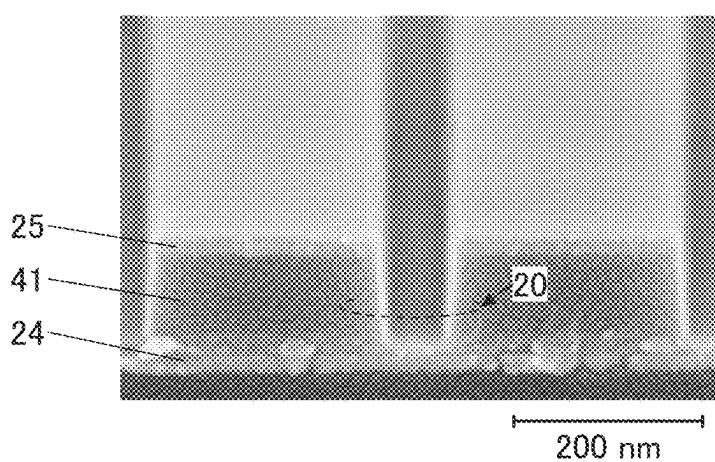
**FIG. 33B**

Line/Space 60 nm/180 nm



**FIG. 33C**

Line/Space 80 nm/240 nm



## SEMICONDUCTOR DEVICE

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

[0001] One embodiment of the present invention relates to a semiconductor device. One embodiment of the present invention relates to a transistor. One embodiment of the present invention relates to a memory device.

[0002] Note that one embodiment of the present invention is not limited to the above technical field. Examples of the technical field of one embodiment of the present invention disclosed in this specification and the like include a semiconductor device, a display device, a light-emitting device, a power storage device, a memory device, an electronic device, a lighting device, an input device, an input/output device, a driving method thereof, and a manufacturing method thereof. A semiconductor device generally means a device that can function by utilizing semiconductor characteristics.

#### 2. Description of the Related Art

[0003] In recent years, semiconductor devices have been developed to be used mainly for a CPU, a memory, and other LSI. A CPU is an aggregation of semiconductor elements; the CPU includes a semiconductor integrated circuit (including at least a transistor and a memory) formed into a chip by processing a semiconductor wafer, and is provided with an electrode that is a connection terminal.

[0004] A semiconductor circuit (IC chip) of a CPU, a memory, or other LSI is mounted on a circuit board, for example, a printed wiring board, to be used as one of components of a variety of electronic devices.

[0005] A technique by which a transistor is formed using a semiconductor thin film formed over a substrate having an insulating surface has been attracting attention. The transistor is used in a wide range of electronic devices such as an integrated circuit and an image display device (also simply referred to as a display device). A silicon-based semiconductor material is widely known as a material of a semiconductor thin film that can be used in a transistor. As another material, an oxide semiconductor has been attracting attention.

[0006] It is known that a transistor including an oxide semiconductor has an extremely low leakage current in a non-conducting state. For example, Patent Document 1 discloses a low-power CPU utilizing the characteristic of a low leakage current. Furthermore, for example, Patent Document 2 discloses a memory device that can retain stored data for a long time.

[0007] In recent years, demand for an integrated circuit with higher density has risen with reductions in size and weight of electronic devices. In addition, the productivity of a semiconductor device including an integrated circuit is desired to be improved. For example, Patent Document 3 discloses a technique to achieve an integrated circuit with higher density by making a plurality of memory cells overlap with each other by stacking a first transistor including an oxide semiconductor film and a second transistor including an oxide semiconductor film. For example, Patent Document 4 discloses a vertical transistor in which a side surface of an oxide semiconductor is covered with a gate electrode with a gate insulator therebetween.

### REFERENCE

#### Patent Document

[0008] [Patent Document 1] Japanese Published Patent Application No. 2012-257187

[0009] [Patent Document 2] Japanese Published Patent Application No. 2011-151383

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### SUMMARY OF THE INVENTION

[0012] An object of one embodiment of the present invention is to provide a semiconductor device which is easily miniaturized. Another object is to provide a semiconductor device that can be highly integrated. Another object is to provide a semiconductor device in which the load on a wiring is reduced. Another object is to provide a highly reliable semiconductor device. Another object is to provide a semiconductor device showing excellent electrical characteristics. Another object is to provide a semiconductor device which operates at high speed.

[0013] Another object is to provide a semiconductor device, a memory device, or an electronic device having a novel structure. Another object of one embodiment of the present invention is to at least alleviate at least one of problems in the conventional art.

[0014] Note that the description of these objects does not preclude the presence of other objects. One embodiment of the present invention does not need to achieve all these objects. Objects other than these can be derived from the description of the specification, the drawings, the claims, and the like.

[0015] One embodiment of the present invention is a semiconductor device including a first conductive layer, a second conductive layer, a third conductive layer, a semiconductor layer, a first insulating layer, a second insulating layer, and a third insulating layer. The first insulating layer is positioned over the first conductive layer and includes a slit reaching the first conductive layer. The second conductive layer is positioned over the first insulating layer. The semiconductor layer includes a portion in contact with a side surface of the second conductive layer, a portion in contact with a side surface of the first insulating layer in the slit, and a portion in contact with a top surface of the first conductive layer in the slit. Inside the slit, the second insulating layer covers the semiconductor layer. Inside the slit, the third conductive layer covers the second insulating layer. Top surfaces of the second conductive layer, the semiconductor layer, the second insulating layer, and the third conductive layer are substantially level with each other. The third insulating layer is in contact with the top surfaces of the second conductive layer, the semiconductor layer, the second insulating layer, and the third conductive layer.

[0016] In the above, it is preferable to further include a connection electrode and a fourth conductive layer. In that case, the slit preferably extends in a first direction. The third conductive layer preferably extends in the first direction in the slit. The fourth conductive layer is preferably positioned over the third insulating layer and extends in a second direction intersecting with the first direction. The connection electrode is preferably in contact with the second conductive

layer and the fourth conductive layer through the opening portion in the third insulating layer.

[0017] In the above, the first conductive layer preferably has a depressed portion in a region overlapping with the slit. In that case, bottom portions of the semiconductor layer, the second insulating layer, and the third conductive layer are preferably provided along the depressed portion.

[0018] In the above, the semiconductor layer preferably includes a first metal oxide. The first conductive layer preferably includes a second metal oxide. In that case, the first metal oxide and the second metal oxide preferably include the same element(s) that is/are one or more selected from In, Sn, Zn, Ga, and Ti, and particularly preferably include In.

[0019] In the above, the semiconductor layer preferably includes the first metal oxide. The second conductive layer preferably includes a third metal oxide. In that case, the first metal oxide and the third metal oxide preferably include the same element(s) that is/are one or more selected from In, Sn, Zn, Ga, and Ti, and particularly preferably include In.

[0020] In the above, the second insulating layer preferably includes a film exhibiting an insulating property and a film exhibiting ferroelectricity. Here, the film exhibiting ferroelectricity preferably includes hafnium oxide, zirconium oxide, or an oxide containing hafnium and zirconium.

[0021] In the above, it is preferable that a fifth conductive layer and a fourth insulating layer are preferably provided below the first conductive layer. At that time, the fourth insulating layer preferably includes a portion positioned between the first conductive layer and the fifth conductive layer.

[0022] In the above, the fifth conductive layer includes a depressed portion. In that case, the fourth insulating layer preferably includes a portion provided along the depressed portion. Furthermore, the first conductive layer preferably includes a portion positioned in the depressed portion with the fourth insulating layer therebetween, and the bottom portion of the first conductive layer positioned in the depressed portion preferably has a convex surface.

[0023] In any of the above, the fourth insulating layer preferably includes a material exhibiting ferroelectricity. Here, the material exhibiting ferroelectricity is preferably one or more of hafnium oxide, zirconium oxide, and an oxide containing hafnium and zirconium.

[0024] According to one embodiment of the present invention, a semiconductor device which is easily miniaturized can be provided. A semiconductor device that can be highly integrated can be provided. A semiconductor device in which the load on a wiring is reduced can be provided. A highly reliable semiconductor device can be provided. A semiconductor device showing excellent electrical characteristics can be provided. A semiconductor device which operates at high speed can be provided.

[0025] One embodiment of the present invention can provide a semiconductor device, a memory device, or an electronic device having a novel structure. According to one embodiment of the present invention, at least one of problems in the conventional art can be at least alleviated.

[0026] Note that the description of these effects does not preclude the existence of other effects. One embodiment of the present invention does not necessarily have all these effects. Effects other than these can be derived from the description of the specification, the drawings, the claims, and the like.

#### BRIEF DESCRIPTION OF THE DRAWINGS

- [0027] In the accompanying drawings:
- [0028] FIGS. 1A and 1B illustrate a structure example of a semiconductor device;
- [0029] FIG. 2 illustrates a structure example of a semiconductor device;
- [0030] FIG. 3 illustrates a structure example of a semiconductor device;
- [0031] FIG. 4 illustrates a structure example of a semiconductor device;
- [0032] FIG. 5 illustrates a structure example of a semiconductor device;
- [0033] FIG. 6 illustrates a structure example of a semiconductor device;
- [0034] FIG. 7 illustrates a structure example of a semiconductor device;
- [0035] FIG. 8 illustrates a structure example of a semiconductor device;
- [0036] FIG. 9 illustrates a structure example of a semiconductor device;
- [0037] FIGS. 10A to 10G illustrate structure examples of a semiconductor device;
- [0038] FIGS. 11A to 11C illustrate an example of a method for manufacturing a semiconductor device;
- [0039] FIGS. 12A to 12C illustrate an example of a method for manufacturing a semiconductor device;
- [0040] FIGS. 13A and 13B illustrate an example of a method for manufacturing a semiconductor device;
- [0041] FIGS. 14A and 14B illustrate an example of a method for manufacturing a semiconductor device;
- [0042] FIGS. 15A and 15B illustrate an example of a method for manufacturing a semiconductor device;
- [0043] FIGS. 16A and 16B illustrate an example of a method for manufacturing a semiconductor device;
- [0044] FIGS. 17A and 17B illustrate an example of a method for manufacturing a semiconductor device;
- [0045] FIG. 18 is a block diagram illustrating a structure example of a semiconductor device;
- [0046] FIGS. 19A to 19H each illustrate a circuit structure example of a memory cell;
- [0047] FIGS. 20A and 20B are perspective views each illustrating a structure example of a semiconductor device;
- [0048] FIG. 21 is a block diagram illustrating a CPU;
- [0049] FIGS. 22A and 22B are perspective views illustrating a semiconductor device;
- [0050] FIGS. 23A and 23B are perspective views each illustrating a semiconductor device;
- [0051] FIG. 24 is a graph showing an example of hysteresis characteristics;
- [0052] FIGS. 25A to 25D are equivalent circuit diagrams of a semiconductor device, and FIG. 25E shows Id-Vg characteristics of a transistor;
- [0053] FIG. 26A is a timing chart, and FIG. 26B is a circuit diagram;
- [0054] FIG. 27A is a timing chart, and FIG. 27B is a circuit diagram;
- [0055] FIG. 28A is a timing chart, and FIG. 28B is a circuit diagram;
- [0056] FIGS. 29A and 29B each illustrate a structure example of an electronic component;
- [0057] FIGS. 30A to 30C illustrate a structure example of a large computer;

[0058] FIG. 31A illustrates a structure example of a space equipment, and FIG. 31B illustrates a structure example of a storage system;

[0059] FIGS. 32A to 32E illustrate a method for forming a slit in Example; and

[0060] FIGS. 33A to 33C are SEM images in Example.

#### DETAILED DESCRIPTION OF THE INVENTION

[0061] Embodiments will be described below with reference to the drawings. Note that the embodiments can be implemented with many different modes, and it will be readily understood by those skilled in the art that modes and details thereof can be changed in various ways without departing from the spirit and scope thereof. Therefore, the present invention should not be construed as being limited to the description of embodiments below.

[0062] Note that in structures of the invention described below, the same portions or portions having similar functions are denoted by the same reference numerals in different drawings, and the description thereof is not repeated. The same hatching pattern is used for portions having similar functions, and the portions are not denoted by specific reference numerals in some cases.

[0063] Note that in each drawing described in this specification, the size, the layer thickness, or the region of each component is exaggerated for clarity in some cases. Therefore, the size, the layer thickness, or the region is not limited to the illustrated scale.

[0064] Note that in this specification and the like, ordinal numbers such as "first" and "second" are used in order to avoid confusion among components and do not limit the number of components.

[0065] A transistor is a kind of semiconductor element and enables amplification of a current or a voltage, switching operation for controlling conduction or non-conduction, and the like. A transistor in this specification includes an insulated-gate field effect transistor (IGFET) and a thin film transistor (TFT).

[0066] The functions of a "source" and a "drain" are sometimes replaced with each other when a transistor of different polarity is used or when the direction of current flow is changed in circuit operation, for example. Thus, the terms "source" and "drain" can be used interchangeably in this specification.

[0067] In this specification and the like, the term "electrically connected" includes the case where components are connected through an "object having any electric function". There is no particular limitation on the "object having any electric function" as long as electric signals can be transmitted and received between components that are connected through the object. Examples of the "object having any electric function" are a switching element such as a transistor, a resistor, a coil, and an element with a variety of functions as well as an electrode and a wiring.

[0068] Note that in this specification and the like, "electrical connection" does not include the case where two nodes are connected to each other with an insulator (e.g., a dielectric of a capacitor, a gate insulating film of a transistor, or an interlayer insulating film) provided between the two nodes.

[0069] In this specification and the like, the expression "having substantially the same top surface shapes" means that the outlines of stacked layers at least partly overlap with

each other. For example, the case of patterning or partly patterning an upper layer and a lower layer with the use of the same mask pattern is included. The expression "having substantially the same top surface shapes" also sometimes includes the case where the outlines do not completely overlap with each other; for instance, the edge of the upper layer may be positioned on the inner side or the outer side of the edge of the lower layer.

[0070] Note that in this specification and the like, a top surface shape of a component means the outline of the component in the plan view. A plan view means that the component is observed from a normal direction of a surface where the component is formed or from a normal direction of a surface of a support (e.g., a substrate) where the component is formed.

[0071] Note that the expressions indicating directions such as "over" and "under" are basically used to correspond to the directions of drawings. However, in some cases, the term "over" or "under" in the specification indicates a direction that does not correspond to the apparent direction in the drawings, for the purpose of easy description or the like. For example, in the description of the stacked order (formation order) of a stacked body or the like, even in the case where a surface on which the stacked body is provided (e.g., a formation surface, a support surface, a bonding surface, or a planarization surface) is located over the stacked body in the drawings, the following expressions are used in some cases: the formation surface side is under the stacked body or the stacked body side is over the formation surface side.

[0072] Note that in this specification and the like, the channel length direction of a transistor refers to one of directions parallel to the shortest straight line connecting a source region and a drain region. That is, the channel length direction corresponds to one of directions of current flow in a semiconductor layer when a transistor is in an on state. The channel width direction refers to a direction orthogonal to the channel length direction. Each of the channel length direction and the channel width direction is not fixed to one direction in some cases depending on the structure or the shape of a transistor.

[0073] In this specification and the like, the terms "film" and "layer" can be interchanged with each other. For example, in some cases, the term "insulating layer" can be interchanged with the term "insulating film".

[0074] Unless otherwise specified, an off-state current in this specification and the like refers to a drain current of a transistor in an off state (also referred to as a non-conduction state or a cutoff state). Unless otherwise specified, the off state of an n-channel transistor means that a gate-source voltage  $V_{gs}$  is lower than a threshold voltage  $V_{th}$ , and the off state of a p-channel transistor means that  $V_{gs}$  is higher than  $V_{th}$ .

#### Embodiment 1

[0075] In this embodiment, structure examples of a semiconductor device of one embodiment of the present invention and a manufacturing method example thereof are described. The semiconductor device described below can be applied to a memory device.

[0076] The semiconductor device of one embodiment of the present invention includes a plurality of memory cells. The memory cell includes one transistor and one memory element. As the memory element, any of a variety of elements that can retain stored data, such as a capacitor, a

resistive random access element, a ferroelectric element, a charge trap element, and a floating-gate element, can be used.

[0077] In the transistor included in the memory cell, a source electrode and a drain electrode are positioned at different heights, so that a current flows in a semiconductor layer in the height direction. In other words, the channel length direction includes a height (vertical) component, so that one embodiment of the present invention can be referred to as a vertical field effect transistor (VFET), a vertical transistor, a vertical-channel transistor, or the like.

[0078] More specifically, a first insulating layer functioning as a spacer is provided above a lower electrode (a first conductive layer) which is one of the source electrode and the drain electrode, and an upper electrode (a second conductive layer) which is the other of the source electrode and the drain electrode is provided above the first insulating layer. The first insulating layer is provided with a slit extending in a first direction and reaching the lower electrode. The slit has a side surface substantially perpendicular to a substrate surface. The semiconductor layer includes a portion in contact with a side surface of the upper electrode, a portion in contact with a side surface of the first insulating layer in the slit, and a portion in contact with a top surface of the lower electrode in the slit. A gate insulating layer (a second insulating layer) is provided to cover the semiconductor layer inside the slit. A gate electrode (a third conductive layer) is provided to cover the gate insulating layer inside the slit. The gate electrode is preferably provided to fill the slit.

[0079] It is also preferable that at least the gate electrode not include a portion protruding above the top surface of the upper electrode. Specifically, the top surface of the gate electrode is preferably level with or lower than the top surface of the upper electrode. In that case, the gate electrode and the upper electrode do not overlap with each other in a plan view, so that parasitic capacitance therebetween can be reduced. Thus, a transistor capable of high-speed operation can be achieved.

[0080] Top surfaces of the semiconductor layer, the gate insulating layer, and the gate electrode are preferably planarized. In that case, the top surfaces of the semiconductor layer, the gate insulating layer, and the gate electrode are preferably planarized such that they are substantially level with the top surface of the upper electrode. Furthermore, an insulating layer functioning as a protective layer is preferably provided in contact with the top surfaces of the semiconductor layer, the gate insulating layer, the gate electrode, and the upper electrode. The formation surface of the insulating layer can be substantially flat with this structure, and thus coverage with the insulating layer is improved and the function of the insulating layer as the protective layer can be enhanced.

[0081] A capacitor included in the memory cell can be provided below the transistor. Stacking the transistor and the capacitor enables the memory cells to be arranged at high density. The capacitor can be what is called a metal-insulator-metal (MIM) capacitor, in which a dielectric is provided between a pair of electrodes. In that case, the lower electrode of the transistor also preferably functions as the upper electrode of the capacitor. In that case, the upper electrode of the transistor preferably functions as a bit line. When a ferroelectric is used as the dielectric included in the capaci-

tor, the capacitor can be a ferroelectric capacitor. Thus, a nonvolatile memory device can be achieved.

[0082] The semiconductor layer preferably includes a metal oxide exhibiting semiconductor characteristics (an oxide semiconductor). For example, to form a source region and a drain region using silicon, which is a typical material of a semiconductor, the regions need to be doped with an impurity functioning as a donor or an acceptor. However, in the vertical transistor of one embodiment of the present invention, it may be difficult to perform impurity doping on the semiconductor layer with high accuracy because the levels of a source and a drain are different from each other and the channel formation region is oriented in the vertical direction with respect to the substrate surface, for example. In contrast, the oxide semiconductor can form a low-resistance region without such impurity doping and can be connected to the source electrode and the drain electrode favorably; thus, a transistor having a three-dimensional structure as in one embodiment of the present invention can be fabricated with high yield.

[0083] Here, the lower electrode preferably has a stacked-layer structure in which a first conductive film and a second conductive film thereover are stacked. In that case, the second conductive film is in contact with the semiconductor layer. Furthermore, the second conductive film preferably includes a conductive metal oxide (an oxide conductor). A metal oxide is preferably used for the conductive film which is in contact with the semiconductor layer including a metal oxide, in which case contact resistance between the conductive film and the semiconductor layer can be reduced and the load on a wiring can be reduced. It is particularly preferable that the second conductive film include the same metal element as the semiconductor layer, in which case the contact resistance can be further reduced. Specifically, the semiconductor layer and the second conductive film preferably include one or more of In, Sn, Zn, Ga, and Ti. For the first conductive film, a low-resistance metal material can be used. Accordingly, both the contact resistance and the wiring resistance can be reduced, so that the load on a wiring can be further reduced.

[0084] Like the lower electrode, the upper electrode preferably includes a conductive metal oxide. Thus, contact resistance between the upper electrode and the semiconductor layer can be reduced. Specifically, the semiconductor layer and the upper electrode preferably include one or more of In, Sn, Zn, Ga, and Ti. Note that the upper electrode may have a stacked-layer structure of a conductive film including a metal oxide and a conductive film including a low-resistance metal material.

[0085] More specific examples are described below with reference to drawings.

#### [Structure Example]

[0086] FIG. 1A is a schematic top view of a semiconductor device 50. FIG. 2 and FIG. 3 are schematic cross-sectional views taken along line A-B and line C-D in FIG. 1A, respectively. FIG. 4 is a perspective view of the semiconductor device 50. Some components (e.g., insulating layer) are omitted in FIG. 4. In each drawing, the arrows indicate directions of X, Y, and Z.

[0087] The semiconductor device 50 has a structure in which a plurality of memory cells 15 are arranged in the X direction and the Y direction. In the semiconductor device 50, a conductive layer 26 functioning as a bit line extends in

the X direction and a conductive layer 23 functioning as a word line extends in the Y direction. As illustrated in FIG. 2, the memory cell 15 includes a transistor 10 and a capacitor 30 thereunder.

[0088] FIG. 1B is a circuit diagram corresponding to the semiconductor device 50. FIG. 1B illustrates a plurality of wirings BL functioning as bit lines, a plurality of wirings WL being orthogonal to the bit lines and functioning as word lines, and a wiring CL. Although FIG. 1B illustrates an example in which the wiring CL is parallel to the wiring BL, the wiring CL can be parallel to the wiring WL or can be placed in a lattice shape. Alternatively, the wiring CL may be a flat plate-like (also referred to as plate-like) conductive film.

[0089] The memory cell 15 includes one transistor 10 and one capacitor 30. A gate of the transistor 10 is connected to the wiring WL, one of a source and a drain of the transistor 10 is connected to the wiring BL, and the other of the source and the drain of the transistor 10 is connected to one electrode of the capacitor 30. The other electrode of the capacitor 30 is connected to the wiring CL.

[0090] The wiring BL functions as a wiring for writing and reading data. The wiring WL functions as a wiring for controlling on and off states (conduction and non-conduction states) of the transistor 10 serving as a switch. The wiring CL has a function of a constant potential line connected to the capacitor 30.

[0091] As illustrated in FIG. 2, the transistor 10 and the capacitor 30 are provided over an insulating layer 11 provided over a substrate (not illustrated). The insulating layer 11 serves as a base insulating layer.

[0092] The transistor 10 includes a semiconductor layer 21, an insulating layer 22 serving as a gate insulating layer, the conductive layer 23 serving as a gate electrode, a conductive layer 24 functioning as one of a source electrode and a drain electrode, and a conductive layer 25 functioning as the other of the source electrode and the drain electrode. Here, an example is described in which the conductive layer 24 includes a conductive film 24a and a conductive film 24b positioned thereover, and the conductive layer 25 includes a conductive film 25a and a conductive film 25b positioned thereover.

[0093] The capacitor 30 is provided over a conductive layer 55 functioning as the wiring CL. The capacitor 30 includes a conductive layer 51 functioning as a lower electrode, the conductive layer 24 functioning as an upper electrode, and an insulating layer 52 positioned therebetween and functioning as a dielectric. In this manner, the conductive layer 24 preferably serves as the lower electrode of the transistor 10 and the upper electrode of the capacitor 30. In that case, the manufacturing process can be simplified and the manufacturing cost can be reduced. In the case where the conductive layer 24 has a stacked-layer structure of the conductive film 24a and the conductive film 24b as illustrated in FIG. 2 and the like, the lower conductive film 24a can function as the upper electrode of the capacitor 30. In this case, it can be said that the upper conductive film 24b functions as a connection electrode for connecting the conductive film 24a and the semiconductor layer 21.

[0094] The conductive layer 55 is provided over the insulating layer 11. Although an example in which the conductive layer 55 has a two-dimensional flat plate-like (plate-like) shape is described here, a wiring (a linear shape) extending in the X direction, the Y direction, or any of the

other directions can also be employed. Alternatively, a lattice shape in which two or more portions extending in different directions are combined can be employed.

[0095] An insulating layer functioning as a protective insulating layer can be provided between the insulating layer 11 and the conductive layer 55. Alternatively, the insulating layer 11 may function as a protective insulating layer. The insulating layer has a function of preventing diffusion of impurities such as hydrogen into the semiconductor layer 21 from the insulating layer 11 or from below the insulating layer 11. For example, a film which is less likely to allow diffusion of hydrogen (which has a higher barrier property against hydrogen) than a silicon oxide film, such as a silicon nitride film, a silicon nitride oxide film, an aluminum oxide film, a magnesium oxide film, a hafnium oxide film, or a gallium oxide film, can be used. Specifically, a silicon nitride film or a silicon nitride oxide film is preferably used.

[0096] Note that in this specification and the like, oxynitride refers to a material in which an oxygen content is higher than a nitrogen content, and nitride oxide refers to a material in which a nitrogen content is higher than an oxygen content. For example, silicon oxynitride refers to a material that contains more oxygen than nitrogen, and silicon nitride oxide refers to a material that contains more nitrogen than oxygen.

[0097] An insulating layer 46 is provided over the conductive layer 55. The insulating layer 46 functions as an interlayer insulating layer. The insulating layer 46 includes a plurality of openings 40 reaching the conductive layer 55, and one capacitor 30 is provided for each of the openings 40. The conductive layer 51 includes a portion provided along a side surface of the insulating layer 46 in the opening 40 and a portion in contact with a top surface of the conductive layer 55. In other words, the conductive layer 51 has a cylindrical shape with the bottom (also referred to as a cup-like shape) and includes a depressed portion. The insulating layer 52 includes a portion provided along the depressed portion of the conductive layer 51, a portion in contact with the top surface of the conductive layer 51, and a portion in contact with the top surface of the insulating layer 46. The conductive layer 24 is provided to fill the depressed portion of the conductive layer 51 with the insulating layer 52 therebetween. The conductive layer 24 includes a portion provided over the insulating layer 46 with the insulating layer 52 therebetween. The conductive layers 51 are provided for the respective memory cells 15, and the conductive layers 51 are connected to each other by the conductive layer 55. The conductive layers 24 are provided for the respective memory cells 15.

[0098] Although FIG. 1A and FIG. 4 and the like illustrate an example in which the outline of the conductive layer 51 in the plan view (outline of the opening 40) is circular, one embodiment of the present invention is not limited thereto. The cross-sectional shape of the conductive layer 51 in the horizontal direction is not limited to a circular ring shape and only needs to be a ring shape. For example, the shape of the outline of the conductive layer 51 in the plan view and the cross-sectional shape of the conductive layer 51 in the horizontal direction are not limited to circular shapes and can each be an elliptical shape, a quadrangular shape with rounded corners, or the like. Alternatively, a regular polygonal shape such as a regular triangular shape, a square shape, or a regular pentagonal shape or a polygonal shape other than the regular polygonal shape may be employed. By

employing a depressed polygonal shape in which at least one interior angle is greater than 180°, such as a star polygonal shape, the capacity can be increased. Alternatively, a quadrangular shape with rounded corners, a closed curve in which a straight line and a curve are combined, or the like can be employed.

[0099] The capacitor 30 illustrated in FIG. 2 and the like is what is called a cylinder capacitor or a trench capacitor. The structure of the capacitor 30 is not limited thereto, and a pillar capacitor may be used, for example.

[0100] FIG. 2 and FIG. 4 illustrate an example in which the bottom portion of the conductive layer 51 is rounded (has a concave surface). Furthermore, the bottom portion of the insulating layer 52 provided along the conductive layer 51 and the bottom portion of the conductive layer 24 provided along the insulating layer 52 each have a rounded shape (a convex surface). When the conductive layer 51 which forms the formation surface of the insulating layer 52 has no corner portion in this manner, the insulating layer 52 can be prevented from being locally thinned. Furthermore, when the bottom portion of the conductive layer 51 has no corner portion, local concentration of electric fields can be prevented. This can reduce a leakage current of the capacitor, so that the reliability can be increased.

[0101] Moreover, the top surface of the conductive layer 55 is provided with a round depression, and the bottom portion of the conductive layer 51 is provided to be fitted in the round depression. Such a structure can increase the contact area between the conductive layer 55 and the conductive layer 51 and reduce contact resistance therebetween. The round depression of the conductive layer 55 can be formed by etching part of the upper portion of the conductive layer 55 at the time of forming the opening in the insulating layer 46.

[0102] The conductive film 24a is preferably formed using a conductive material having lower resistance than the conductive film 24b. In particular, a metal material is preferably included. For the conductive film 24b, a conductive metal oxide (an oxide conductor) is preferably used.

[0103] The conductive metal oxide is preferably used for the conductive film 24b which is in contact with the semiconductor layer 21 including a metal oxide, in which case contact resistance between the conductive film 24b and the semiconductor layer 21 can be reduced and a load on a wiring can be reduced. It is particularly preferable that the conductive film 24b include the same metal element as the metal element included in the semiconductor layer 21, in which case the contact resistance can be further reduced. Specifically, the semiconductor layer 21 and the conductive film 24b preferably include the same element(s) that is/are one or more selected from In, Sn, Zn, Ga, and Ti. When a metal material having a lower resistance than the conductive film 24b is used for the conductive film 24a, both the contact resistance and the wiring resistance can be reduced, so that the load on a wiring can be further reduced.

[0104] An insulating layer 41 is provided above the conductive layer 24 and the insulating layer 52. The insulating layer 41 includes a belt-like slit 20 extending in the Y direction. A side surface of the insulating layer 41 in the slit 20 is preferably substantially perpendicular to the substrate surface. The height of the insulating layer 41 is preferably larger than the width of the slit 20 in the X direction.

[0105] In this specification and the like, the expression "two surfaces are perpendicular to each other" indicates a

state where the interior angle between them is greater than or equal to 80° and less than or equal to 100°. Moreover, the expression "two surfaces are substantially perpendicular to each other" indicates a state where the interior angle between them is greater than or equal to 60° and less than or equal to 120° (including a state where the surfaces are perpendicular to each other). In this specification and the like, the expression "two surfaces are parallel to each other" indicates a state where the interior angle between them is greater than or equal to -10° and less than or equal to 10°. Moreover, the expression "two surfaces are substantially parallel to each other" indicates a state where the interior angle between them is greater than or equal to -30° and less than or equal to 30° (including a state where the surfaces are parallel to each other).

[0106] The conductive layer 25 is provided over the insulating layer 41. In the example described here, the conductive layer 25 has a stacked-layer structure of the conductive film 25a and the conductive film 25b provided over the conductive film 25a. The conductive layer 25 is provided with a slit overlapping with the slit 20, and the conductive layer 25 is divided into two layers with the slit as a boundary. That is, a pair of the conductive layers 25 are provided over the insulating layer 41 such that one slit 20 is positioned between the conductive layers 25. As illustrated in FIG. 4, the island-shaped conductive layers 25 are arranged at regular intervals along the extending direction of the slit 20.

[0107] The semiconductor layer 21, the insulating layer 22, and the conductive layer 23 each include a portion positioned inside the slit 20. The semiconductor layer 21 and the insulating layer 22 are provided along the side surface of the insulating layer 41 in the slit 20 and a top surface of the conductive layer 24 in the slit 20. The conductive layer 23 is provided to fill a depressed portion of the insulating layer 22.

[0108] The semiconductor layer 21 includes a portion in contact with a side surface of the conductive layer 25, a portion in contact with the side surface of the insulating layer 41 in the slit 20, and a portion in contact with the top surface of the conductive film 24b. Here, a conductive metal oxide similar to that used for the above-described conductive film 24b is preferably used for one of the conductive film 25a and the conductive film 25b included in the conductive layer 25. For the other of the conductive film 25a and the conductive film 25b, a low-resistance metal material is preferably used. When a conductive film with low contact resistance with the semiconductor layer 21 and a conductive film with low wiring resistance are stacked, both the contact resistance and the wiring resistance can be reduced, so that the load on a wiring can be further reduced. An example in which a conductive metal oxide is used for the conductive film 25b and a metal material is used for the conductive film 25a is described below, but a conductive metal oxide can be used for the conductive film 25a and a metal material can be used for the conductive film 25b.

[0109] One of the conductive films 25a and 25b which includes a conductive metal oxide preferably includes the same metal element as the semiconductor layer 21, in which case the contact resistance can be further reduced. Specifically, the semiconductor layer 21 and one of the conductive films 25a and 25b preferably include the same element(s) that is/are one or more selected from In, Sn, Zn, Ga, and Ti.

[0110] In the transistor **10**, the source electrode and the drain electrode are located at different heights, so that a current flows in the height direction in the semiconductor. In other words, the channel length direction includes a height (vertical) component, and thus the transistor of one embodiment of the present invention can also be referred to as a VFET, a vertical transistor, a vertical channel transistor, or the like. Since two or more of the source electrode, the semiconductor, and the drain electrode can overlap with each other in the transistor **10**, the area occupied by the transistor **10** can be significantly smaller than that occupied by what is called a planar transistor (also referred to as a lateral transistor, a lateral FET (LFET), or the like) in which a semiconductor is positioned over a flat plane.

[0111] The channel length of the transistor **10** can be precisely adjusted by the thickness of the insulating layer **41** serving as a spacer; thus, a variation in the channel length can be extremely smaller than that of a planar transistor. Furthermore, by reducing the thickness of the insulating layer **41**, a transistor with an extremely short channel length can be manufactured. For example, it is possible to manufacture a transistor with a channel length of 2 μm or shorter, 1 μm or shorter, 500 nm or shorter, 300 nm or shorter, 200 nm or shorter, 100 nm or shorter, 50 nm or shorter, 30 nm or shorter, or 20 nm or shorter, and 5 nm or longer, 7 nm or longer, or 10 nm or longer. Thus, it is possible to achieve a transistor with an extremely short channel length that could not be achieved with a light-exposure apparatus for mass production. Moreover, a transistor with a channel length shorter than 10 nm can also be achieved without using an extremely expensive light-exposure apparatus used in the latest LSI technology.

[0112] A variety of semiconductor materials can be used for the semiconductor layer **21**; in particular, an oxide semiconductor including a metal oxide is preferably used. The use of an oxide semiconductor formed under an appropriate condition allows a transistor having both a high on-state current and an extremely low off-state current to be achieved at a low cost. Described below are structure examples of the case where an oxide semiconductor is used for the semiconductor layer **21** unless otherwise specified.

[0113] Here, FIG. 2 illustrates an example in which the top surface of a region of the conductive film **24b** overlapping with the slit **20** has a round depression (a concave surface). Thus, inside the slit **20**, bottom portions of the semiconductor layer **21**, the insulating layer **22**, and the conductive layer **23** are provided along the concave surface of the conductive film **24b** and have rounded projecting portion (convex surfaces). Accordingly, a structure in which an electric field is less likely to be concentrated can be achieved as in the conductive layer **51** of the capacitor **30**. Thus, a transistor having a low leakage current and high reliability can be achieved.

[0114] It is preferable that the upper portions of the semiconductor layer **21**, the insulating layer **22**, and the conductive layer **23** be planarized such that the top surfaces of the semiconductor layer **21**, the insulating layer **22**, and the conductive layer **23** are at substantially the same levels (e.g., substantially the same levels from the substrate surface). Furthermore, the top surfaces of the semiconductor layer **21**, the insulating layer **22**, and the conductive layer **23** are preferably substantially level with the top surface of the conductive layer **25** (specifically, the conductive film **25b**). With such a structure, the conductive layer **25** and the

conductive layer **23** do not overlap with each other in a plan view, so that parasitic capacitance between the conductive layer **25** and the conductive layer **23** can be reduced. Accordingly, a semiconductor device capable of high-speed operation can be achieved.

[0115] An insulating layer **43** is provided in contact with the top surfaces of the conductive layer **25**, the semiconductor layer **21**, the insulating layer **22**, and the conductive layer **23**. The insulating layer **43** functions as a barrier film that prevents diffusion of impurities such as hydrogen into the semiconductor layer **21** from above the insulating layer **43**. For example, a film which is less likely to allow diffusion of hydrogen (which has a higher barrier property against hydrogen) than a silicon oxide film, such as a silicon nitride film, a silicon nitride oxide film, an aluminum oxide film, a magnesium oxide film, a hafnium oxide film, or a gallium oxide film, can be used. Specifically, a silicon nitride film or a silicon nitride oxide film is preferably used.

[0116] The insulating layer **43** preferably has a stacked-layer structure of an insulating film functioning as the above-described barrier film and an insulating film on the semiconductor layer **21** side having a function of capturing or fixing hydrogen. Accordingly, hydrogen that may diffuse into the semiconductor layer **21** by heat applied during the manufacturing process of the transistor **10** or the memory cell **15** can be captured or fixed by the insulating film, so that the concentration of hydrogen contained in the semiconductor layer **21** can be reduced. Thus, the transistor **10** or the semiconductor device **50** can have favorable electrical characteristics and high reliability. As the insulating film that captures or fixes hydrogen, a hafnium oxide film, a hafnium silicate film, an aluminum oxide film, a hafnium zirconium oxide film, or the like is preferably used.

[0117] An insulating layer **44** functioning as an interlayer insulating film is provided over the insulating layer **43**. Note that the insulating layer **44** is not necessarily provided when not needed.

[0118] The conductive layer **26** functioning as a bit line is provided over the insulating layer **44**. A plug **27** for connecting the conductive layer **25** and the conductive layer **26** to each other through an opening which is provided in the insulating layer **44** and the insulating layer **43** is provided. Thus, a plurality of the conductive layers **25** arranged in the X direction with the slits **20** therebetween can be connected to each other by the conductive layer **26**.

[0119] Here, in the semiconductor device **50**, a layer where the memory cell **15** is provided and a layer where a functional circuit is provided are preferably stacked. As the functional circuit, a driver circuit for driving the memory cell **15**, an arithmetic circuit, a power supply circuit, or the like can be provided, for example. The driver circuit includes, for example, one or more of a row decoder, a column decoder, a row driver, a column driver, an input circuit, an output circuit, and a sense amplifier. Accordingly, the footprint of the semiconductor chip including the semiconductor device **50** can be reduced, and wiring length can be shorter than that in the case where the functional circuit and the memory cell **15** are arranged side by side; hence, high-speed operation and low power consumption can be achieved.

[0120] FIG. 5 illustrates an example in which a transistor **90** included in the functional circuit is provided below a layer **80** provided with the memory cell **15**. Here, an example in which one of a source electrode and a drain

electrode of the transistor **90** is connected to the conductive layer **26** functioning as a bit line is illustrated.

[0121] The transistor **90** is a transistor whose channel is formed in part of a substrate **91**, which is a single crystal semiconductor substrate. For the substrate **91**, single crystal silicon can be typically used. For the substrate **91**, a semiconductor of a single element such as germanium, or a compound semiconductor of silicon carbide, silicon germanium, gallium arsenide, indium phosphide, zinc oxide, gallium oxide, or gallium nitride can be used, for example. The above semiconductor substrate in which an insulator region is included, e.g., a silicon on insulator (SOI) substrate, may be used as the substrate **91**.

[0122] The transistor **90** is provided on the substrate **91** and includes a conductive layer **94** serving as a gate, an insulating layer **93** serving as a gate insulating layer, a semiconductor region **92** that is a part of the substrate **91**, and a low-resistance region **95a** and a low-resistance region **95b** serving as a source region and a drain region. As the transistor **90**, either a p-channel transistor or an n-channel transistor can be used. In the substrate **91**, an element isolation layer **98** is provided between two adjacent transistors **90**.

[0123] In the transistor **90**, the semiconductor region **92** where a channel is formed has a projecting shape (fin shape). Although not illustrated in FIG. 5, the conductive layer **94** is provided to cover a side surface and the top surface of the semiconductor region **92** with the insulating layer **93** therebetween in the Y direction. A transistor like the transistor **90** is also referred to as a FIN transistor.

[0124] An insulating layer **96** is provided to cover the transistor **90**, an insulating layer **86** is provided over the insulating layer **96**, and an insulating layer **87** is provided over the insulating layer **86**. A conductive layer **81** is provided to be embedded in the insulating layer **87**. An insulating layer **88** is provided to cover the conductive layer **81** and the insulating layer **87**, an insulating layer **45** is provided over the insulating layer **88**, and the insulating layer **11** is provided over the insulating layer **45**. A plug **82** is provided in the opening provided in the insulating layer **96** and the insulating layer **86**, and the conductive layer **81** and the low-resistance region **95b** are connected to each other through the plug **82**. A conductive layer **84** is provided over the insulating layer **45**, and the conductive layer **84** is connected to the conductive layer **81** through a plug **83** provided in an opening provided in the insulating layer **45** and the insulating layer **88**. The conductive layer **84** and the conductive layer **26** are connected to each other through a plug **85** provided in an opening provided in each of the insulating layers between the conductive layer **84** and the conductive layer **26**. Thus, one of a source and a drain of the transistor **90** is connected to the conductive layer **26**.

[0125] Although an example in which the conductive layer **81** is provided as a wiring layer is described here, a structure in which an interlayer insulating layer and a wiring layer are alternately stacked (also referred to as a multilayer wiring layer) can be provided between the layer where the transistor **90** is provided and the layer **80** where the memory cell **15** is provided.

[0126] Here, in a region outside a memory cell array including the memory cell **15** or outside the functional circuit including the transistor **90**, the insulating layers included in the layer **80** are etched, and an insulating layer **47** is provided to cover the top surface and a side surface of

the insulating layer **80**. The insulating layer **47** is in contact with the top surface of the insulating layer **45**. Accordingly, all the memory cells **15** included in the layer **80** can be surrounded by the insulating layer **47** and the insulating layer **45**.

[0127] As the insulating layer **45** and the insulating layer **47**, the above-described film having a barrier property against hydrogen can be used. Specifically, a silicon nitride film or a silicon nitride oxide film is preferably used.

[0128] Furthermore, the insulating layer **45** and the insulating layer **47** preferably have a stacked-layer structure in which the insulating film functioning as the above-described barrier film and the insulating film having a function of capturing or fixing hydrogen on the inner side (the transistor **10** side). For example, a hafnium oxide film, a hafnium silicate film, an aluminum oxide film, a hafnium zirconium oxide film, or the like is preferably used.

[0129] In that case, diffusion of hydrogen from the outside into a region surrounded by the insulating layer **45** and the insulating layer **47** is inhibited, and the hydrogen concentration in the region is reduced. Accordingly, hydrogen that might be diffused into the semiconductor layer **21** of the transistor **10** can be effectively reduced, so that the transistor **10** with high reliability can be achieved.

[0130] FIG. 6 illustrates an example in which the layers **80** including the memory cells **15** are stacked. Although FIG. 6 illustrates an example in which three of the layers **80** (layers **80[1]** to **80[3]** from the substrate **91** side) are stacked, the number of layers **80** to be stacked may be two or four or more.

[0131] The plug **85** connects the conductive layer **84** to the conductive layer **26** included in the layer **80[1]**. Furthermore, a plug **89** connects the conductive layer **26** included in one layer **80** to the conductive layer **26** included in another layer **80**. Thus, three of the conductive layers **26** included in the layers **80[1]** to **80[3]** are connected to the one of the source and the drain of the transistor **90**.

[0132] The insulating layer **47** is provided to surround the layers **80[1]** to **80[3]**. Note that without limitation to this structure, the insulating layer **47** can be provided for each of the layers **80**.

[0133] Although the structure in which the layer **80** is stacked directly over the substrate **91** where the transistor **90** is provided is described here, one embodiment of the present invention is not limited thereto. For example, the substrate **91** provided with the transistor **90** and the substrate provided with the memory cell **15** may be bonded to each other. For example, two substrates can be bonded to each other by direct bonding (hybrid bonding) using a direct bonding technique typified by Cu—Cu bonding. Alternatively, a method may be used in which two or more layers are bonded to each other with their insulating surfaces and then a through electrode is formed to connect electrodes or the like provided in the layers to each other. A method using direct bonding or a through electrode is particularly preferably used, in which case the pitch width between the connection electrodes can be extremely narrowed and thus a large amount of connection electrodes can be arranged at high density, whereby a larger amount of data can be transmitted between layers.

[0134] When two layers are bonded, any of a chip on chip (CoC) bonding, a chip on wafer (CoW) bonding, or a wafer on wafer (WoW) bonding may be used as a bonding method. The WoW bonding bonds wafers to each other and is thus

excellent in productivity; however, since the WoW bonding bonds all the chips, including defective and non-defective chips, to each other, the yield is reduced in some cases. Meanwhile, the CoW bonding where a chip is bonded to a wafer and the CoC bonding where chips are bonded to each other are inferior to the WoW bonding in terms of productivity; however, the CoW bonding and the CoC bonding can bond non-defective chips to each other and thus achieve a significantly improved yield. Although the CoC bonding is less productive than the other two bonding methods, the CoC bonding can bond two layers with largely different sizes and thus has high versatility.

[0135] Note that a wiring layer such as an interposer may be provided between two layers. Thus, the positions of the bonding electrodes and the like do not need to be aligned between the two adjacent layers, so that the design flexibility of the layers can be increased and a semiconductor device with higher performance can be achieved.

[0136] FIG. 7 illustrates an example in which a layer 60 including a memory cell 16 that can be used as a dynamic random access memory (DRAM) is stacked with the layer 80. The memory cell 16 includes the transistor 90 and a capacitor 70.

[0137] The one of the source electrode and the drain electrode of the transistor 90 is connected to the bit line, and the other of the source electrode and the drain electrode of the transistor 90 is connected to the capacitor 70. The capacitor 70 includes a conductive layer 71, a conductive layer 73, and an insulating layer 72 sandwiched therebetween. The structure illustrated in FIG. 7 includes the columnar (pillar-shaped) conductive layer 71, and the insulating layer 72 and the conductive layer 73 which are provided to cover the conductive layer 71.

[0138] FIG. 7 illustrates an example in which two of the transistors 90 are connected to the same bit line. With such a structure, the memory cells can be arranged at a high density.

[0139] Although FIG. 7 illustrates an example in which the layer 80 is stacked directly over the layer 60, the layer 60 and the layer 80 may be formed separately and bonded to each other. In that case, the stacking order of the layer 60 and the layer 80 is not limited, and the layer 60 may be stacked over the layer 80. There is also no limitation on the vertical orientation of the layer 60 and the layer 80. In each of the layer 60 and the layer 80, the substrate side (the formation surface side) may be a bonding surface or the surface opposite to the substrate side may be a bonding surface.

#### [Components]

#### <Substrate>

[0140] As a substrate where a transistor is formed, an insulator substrate, a semiconductor substrate, or a conductor substrate can be used, for example. Examples of the insulator substrate include a glass substrate, a quartz substrate, a sapphire substrate, a stabilized zirconia substrate (e.g., an yttria-stabilized zirconia substrate), and a resin substrate. Examples of the semiconductor substrate include a semiconductor substrate of silicon or germanium and a compound semiconductor substrate of silicon carbide, silicon germanium, gallium arsenide, indium phosphide, zinc oxide, gallium oxide, or gallium nitride. Other examples include the above semiconductor substrate including an insulator region, e.g., a silicon on insulator (SOI) substrate.

Examples of the conductor substrate include a graphite substrate, a metal substrate, an alloy substrate, and a conductive resin substrate. Other examples of the conductor substrate include a substrate including a nitride of a metal and a substrate including an oxide of a metal. Moreover, other examples of the conductor substrate include an insulator substrate provided with a conductive layer or a semiconductor layer, a semiconductor substrate provided with a conductive layer or an insulating layer, and a conductor substrate provided with a semiconductor layer or an insulating layer. Alternatively, these substrates provided with elements may be used. Examples of the elements provided over the substrates include a capacitor, a resistor, a switching element (such as a transistor), a light-emitting element, and a memory element.

#### <Semiconductor Layer>

[0141] The semiconductor layer 21 preferably includes a metal oxide (an oxide semiconductor).

[0142] Examples of the metal oxide that can be used for the semiconductor layer 21 include an In oxide, a Ga oxide, and a Zn oxide. The metal oxide preferably contains at least In or Zn. The metal oxide preferably includes two or three elements selected from In, an element M, and Zn. The element M is a metal element or metalloid element that has a high bonding energy with oxygen, such as a metal element or metalloid element whose bonding energy with oxygen is higher than that of In. Specific examples of the element M include Al, Ga, Sn, Y, Ti, V, Cr, Mn, Fe, Co, Ni, Zr, Mo, Hf, Ta, W, La, Ce, Nd, Mg, Ca, Sr, Ba, B, Si, Ge, and Sb. The element M contained in the metal oxide is preferably one or more kinds selected from the above elements. Specifically, the element M is preferably one or more kinds selected from Al, Ga, Y, and Sn, further preferably Ga. Hereinafter, a metal oxide containing In, M, and Zn is referred to as In-M-Zn oxide in some cases. In this specification and the like, a metal element and a metalloid element may be collectively referred to as a "metal element", and a "metal element" in this specification and the like may refer to a metalloid element.

[0143] When the metal oxide is an In-M-Zn oxide, the proportion of the number of In atoms is preferably higher than or equal to that of the number of M atoms in the In-M-Zn oxide. Examples of the atomic ratio of the metal elements of such In-M-Zn oxide include In:M:Zn=1:1:1, In:M:Zn=1:1:1.2, In:M:Zn=2:1:3, In:M:Zn=3:1:2, In:M:Zn=4:2:3, In:M:Zn=4:2:4.1, In:M:Zn=5:1:3, In:M:Zn=5:1:6, In:M:Zn=5:1:7, In:M:Zn=5:1:8, In:M:Zn=6:1:6, and In:M:Zn=5:2:5 and a composition in the vicinity thereof. Note that the vicinity of the atomic ratio includes  $\pm 30\%$  of an intended atomic ratio. By increasing the proportion of the number of In atoms in the metal oxide, the on-state current, field-effect mobility, or the like of the transistor can be improved.

[0144] The proportion of the number of In atoms may also be lower than that of the number of element M atoms in the In-M-Zn oxide. Examples of the atomic ratio of the metal elements of such In-M-Zn oxide include In:M:Zn=1:3:2, In:M:Zn=1:3:3, and In:M:Zn=1:3:4 and a composition in the vicinity of any of the above atomic ratios. By increasing the proportion of the number of element M atoms in the metal oxide, generation of oxygen vacancies can be inhibited.

[0145] For the semiconductor layer 21, for example, In oxide, In—Zn oxide, In—Ga oxide, In—Sn oxide, In—Ti

oxide, In—Ga—Al oxide, In—Ga—Sn oxide, In—Ga—Zn oxide, In—Sn—Zn oxide, In—Al—Zn oxide, In—Ti—Zn oxide, In—Ga—Sn—Zn oxide, or In—Ga—Al—Zn oxide can be used. Alternatively, Ga—Zn oxide may be used. A material that does not contain Zn like indium oxide is preferred in that it improves the compatibility with an LSI manufacturing process. By contrast, a material that contains Zn is preferred in that crystallinity can be easily increased.

[0146] Instead of indium or in addition to indium, the metal oxide may contain one or more kinds of metal elements whose period number in the periodic table is large. The larger the overlap between orbits of metal elements is, the more likely it is that the metal oxide will have high carrier conductivity. Thus, when a metal element with a large period number is contained in the metal oxide, the field-effect mobility of the transistor can be increased in some cases. Examples of the metal element with a large period number include metal elements belonging to Period 5 and metal elements belonging to Period 6. Specific examples of the metal element include Y, Zr, Ag, Cd, Sn, Sb, Ba, Pb, Bi, La, Ce, Pr, Nd, Pm, Sm, and Eu. Note that La, Ce, Pr, Nd, Pm, Sm, and Eu are referred to as light rare earth elements.

[0147] The metal oxide may contain one or more kinds selected from nonmetallic elements. A transistor including the metal oxide including a nonmetallic element can have high field-effect mobility in some cases. Examples of the nonmetallic element include carbon, nitrogen, phosphorus, sulfur, selenium, fluorine, chlorine, bromine, and hydrogen.

[0148] For the formation of a metal oxide, a sputtering method or an atomic layer deposition (ALD) method can be suitably used. In particular, a film of the metal oxide is preferably formed by an ALD method, which enables good coverage. Note that in the case where the metal oxide is formed by a sputtering method, the composition of the formed metal oxide film may be different from the composition of a target. In particular, the zinc content percentage of the formed metal oxide film may be reduced to approximately 50% of that of the target.

[0149] In this specification and the like, the content of a certain metal element in a metal oxide refers to the proportion of the number of atoms of the metal element to the total number of metal element atoms contained in the metal oxide. In the case where a metal oxide contains a metal element X, a metal element Y, and a metal element Z whose atomic numbers are respectively represented by  $A_X$ ,  $A_Y$ , and  $A_Z$ , the content of the metal element X can be represented by  $A_X/(A_X+A_Y+A_Z)$ . Moreover, in the case where the atomic ratio of the metal element X to the metal element Y and the metal element Z contained in the metal oxide is represented by  $B_X:B_Y:B_Z$ , the content of the metal element X can be represented by  $B_X/(B_X+B_Y+B_Z)$ .

[0150] In the case of using a metal oxide containing In, for example, an increase in the In content enables a transistor to have a high on-state current.

[0151] When the semiconductor layer 21 includes a metal oxide not containing Ga or having a low Ga content, a transistor can have high reliability against positive bias application. That is, the transistor can show a small amount of change in the threshold voltage in the positive bias temperature stress (PBTS) test. In the case of using a metal oxide containing Ga, the Ga content is preferably lower than the In content. Accordingly, the transistor can have high mobility and high reliability.

[0152] Meanwhile, a transistor having a high Ga content can have high reliability against light. That is, the transistor can show a small amount of change in the threshold voltage of the transistor in the negative bias temperature illumination stress (NBTIS) test. Specifically, a metal oxide in which the proportion of the number of Ga atoms is greater than or equal to that of the number of In atoms has a wider band gap and can reduce the amount of change in the threshold voltage of the transistor in the NBTIS test.

[0153] Furthermore, a metal oxide having a high zinc content has high crystallinity whereby diffusion of impurities can be inhibited. Consequently, a change in electrical characteristics of the transistor is suppressed and the transistor can have high reliability.

[0154] The semiconductor layer 21 may have a stacked-layer structure including two or more metal oxide layers. The two or more metal oxide layers included in the semiconductor layer 21 may have the same composition or substantially the same compositions. Employing a stacked-layer structure of metal oxide layers having the same composition can reduce the manufacturing cost because the metal oxide layers can be formed using the same sputtering target. Note that a stacked-layer structure including two or more oxide semiconductor layers having different compositions may be employed. The use of an ALD method can form a metal oxide layer with a composition that continuously changes in the thickness direction. This not only increases the range of choices for design without need for use of a film with a predetermined composition but also prevents generation of an interface state or the like between two layers with different compositions; thus, the electrical characteristics and reliability can be improved. A metal oxide layer having a stacked-layer structure may be formed by both a sputtering method and an ALD method.

[0155] In the case where the semiconductor layer 21 has a two-layer structure, the second layer, i.e., the layer closer to the gate electrode, preferably includes a material with higher mobility (higher conductivity) than the first layer. This structure enables the transistor to have normally-off characteristics and a high on-state current. Consequently, both low power consumption and high performance can be achieved. Alternatively, the first layer, i.e., the layer in contact with the source electrode and the drain electrode, may include a material having higher mobility than the second layer. In that case, contact resistance between the semiconductor layer 21 and the source electrode or the drain electrode can be reduced and the parasitic resistance can be reduced accordingly, so that the transistor can have a high on-state current.

[0156] In the case where the semiconductor layer 21 has a three-layer structure, the second layer preferably includes a material having higher mobility than the first and third layers. This structure enables the transistor with a high on-state and high reliability.

[0157] The above-described differences in the mobility and conductivity can be replaced with a difference in the indium content percentage, for example. In addition, the mobility and the conductivity are affected by whether or not an element that contributes to an improvement in conductivity is contained in addition to indium, by the content of the element, or the like. Examples of the high-mobility material include a material having an atomic ratio of In:Ga:Zn=4:3:2 or in the vicinity thereof, a material having an atomic ratio of In:Zn=1:1 or in the vicinity thereof, a material having an atomic ratio of In:Zn=2:1 or in the vicinity thereof, a

material having an atomic ratio of In:Zn=4:1 or in the vicinity thereof, and a material having an atomic ratio of In:Sn:Zn=40:X:10 (X is greater than or equal to 0.1 and less than or equal to 5, typically X=1) or in the vicinity thereof. Examples of a material having lower mobility or conductivity than the above-described materials include a material having an atomic ratio of In:Ga:Zn=1:3:2 or in the vicinity thereof, a material having an atomic ratio of In:Ga:Zn=1:3:4 or in the vicinity thereof, a material having an atomic ratio of In:Ga:Zn=2:2:1 or in the vicinity thereof, a material having an atomic ratio of In:Ga:Zn=1:1:1 or in the vicinity thereof, and a material having an atomic ratio of In:Ga:Zn=1:1:2 or in the vicinity thereof.

[0158] It is preferable to use a metal oxide layer having crystallinity as the semiconductor layer **21**. For example, a metal oxide layer having a c-axis aligned crystal (CAAC) structure, a polycrystalline structure, a nano-crystal (nc) structure, or the like can be used. By using a metal oxide layer having crystallinity as the semiconductor layer **21**, the density of defect states in the semiconductor layer **21** can be reduced, which enables the semiconductor device to have high reliability.

[0159] As the crystallinity of the metal oxide layer used as the semiconductor layer **21** becomes higher, the density of defect states in the semiconductor layer **21** can be reduced. By contrast, the use of a metal oxide layer having low crystallinity enables a transistor to flow a high current.

[0160] A transistor including an oxide semiconductor (hereinafter referred to as an OS transistor) has much higher field-effect mobility than a transistor including amorphous silicon. In addition, the OS transistor has an extremely low leakage current between a source and a drain in an off state (hereinafter also referred to as an off-state current), and electric charge accumulated in a capacitor that is connected in series to the transistor can be held for a long period. Furthermore, the power consumption of the semiconductor device can be reduced with the OS transistor.

[0161] The semiconductor device of one embodiment of the present invention can be applied to a processor, a memory device, or any of a variety of ICs, for example. The transistor of one embodiment of the present invention can make a high current flow therethrough and has a feature of an extremely low off-state current; thus, high-speed operation of a circuit and a reduction in power consumption can be achieved at the same time.

[0162] The semiconductor device of one embodiment of the present invention can also be used for a display device, for example. To increase the luminance of a light-emitting device included in a pixel circuit of a display device, it is necessary to increase the amount of current flowing through the light-emitting device. To increase the current amount, the source-drain of a driving transistor included in the pixel circuit needs to be increased. Since an OS transistor has a higher withstand voltage between a source and a drain than a transistor including silicon (hereinafter referred to as a Si transistor), a high voltage can be applied between the source and the drain of the OS transistor. Therefore, when an OS transistor is used as the driving transistor in the pixel circuit, the amount of current flowing through the light-emitting device can be increased, so that the luminance of the light-emitting device can be increased.

[0163] When transistors operate in a saturation region, a change in source-drain current relative to a change in gate-source voltage can be smaller in an OS transistor than

in a Si transistor. Accordingly, when an OS transistor is used as the driving transistor included in the pixel circuit, the amount of current flowing through the light-emitting device can be precisely controlled. Consequently, the number of gray levels expressed by the pixel circuit can be increased. Moreover, a stable current can flow through the light-emitting device even when the electrical characteristics (e.g., resistance) of the light-emitting device change or the electrical characteristics of the light-emitting devices vary.

[0164] As described above, with use of an OS transistor as a driving transistor included in a pixel circuit, it is possible to achieve "inhibition of black floating", "increase in emission luminance", "increase in gray level", "reduction in influence of manufacturing variation in light-emitting devices", and the like.

[0165] A change in electrical characteristics of an OS transistor due to irradiation with radiation is small, that is, an OS transistor has high resistance to radiation; thus, an OS transistor can be suitably used even in an environment where radiation can enter. It can also be said that an OS transistor has high reliability against radiation. For example, an OS transistor can be suitably used for a pixel circuit of an X-ray flat panel detector. Moreover, an OS transistor can be suitably used for a semiconductor device used in space. Examples of radiation include electromagnetic radiation (e.g., X-rays and gamma rays) and particle radiation (e.g., alpha rays, beta rays, a proton beam, and a neutron beam).

[0166] Note that a semiconductor material that can be used for the semiconductor layer **21** is not limited to an oxide semiconductor. For example, a single-element semiconductor or a compound semiconductor can be used. Examples of the single-element semiconductor include silicon (such as single crystal silicon, polycrystalline silicon, microcrystalline silicon, and amorphous silicon) and germanium. Examples of the compound semiconductor include gallium arsenide and silicon germanium. Examples of the compound semiconductor include an organic semiconductor, a nitride semiconductor, and an oxide semiconductor. These semiconductor materials may contain impurities as dopants.

[0167] Alternatively, the semiconductor layer **21** may include a layered material functioning as a semiconductor. The layered material generally refers to a group of materials having a layered crystal structure. In the layered crystal structure, layers formed by covalent bonding or ionic bonding are stacked with bonding such as the van der Waals binding, which is weaker than covalent bonding or ionic bonding. The layered material has high electrical conductivity in a unit layer, that is, high two-dimensional electrical conductivity. When a material that functions as a semiconductor and has high two-dimensional electrical conductivity is used for a channel formation region, the transistor can have a high on-state current.

[0168] Examples of the layered material include graphene, silicene, and chalcogenide. Chalcogenide is a compound containing chalcogen (an element belonging to Group 16). Examples of chalcogenide include transition metal chalcogenide and chalcogenide of Group 13 elements. Specific examples of the transition metal chalcogenide which can be used for a semiconductor layer of a transistor include molybdenum sulfide (typically MoS<sub>2</sub>), molybdenum selenide (typically MoSe<sub>2</sub>), molybdenum telluride (typically MoTe<sub>2</sub>), tungsten sulfide (typically WS<sub>2</sub>), tungsten selenide (typically WSe<sub>2</sub>), tungsten telluride (typically WTe<sub>2</sub>), haf-

nium sulfide (typically  $\text{HfS}_2$ ), hafnium selenide (typically  $\text{HfSe}_2$ ), zirconium sulfide (typically  $\text{ZrS}_2$ ), and zirconium selenide (typically  $\text{ZrSe}_2$ ).

[0169] There is no particular limitation on the crystallinity of a semiconductor material used for the semiconductor layer 21, and any of an amorphous semiconductor, a single crystal semiconductor, and a semiconductor having other crystallinity than single crystal (a polycrystalline semiconductor, a microcrystalline semiconductor, or a semiconductor partly including crystal regions) may be used. A semiconductor having crystallinity is preferably used, in which case deterioration of transistor characteristics can be suppressed.

#### <Gate Insulating Layer>

[0170] The insulating layer 22 functions as a gate insulating layer of the transistor. In the case where the semiconductor layer 21 is formed using an oxide semiconductor, an oxide insulating film is preferably used for at least a part of the insulating layer 22 that is in contact with the semiconductor layer 21. For example, one or more of silicon oxide, silicon oxynitride, aluminum oxide, aluminum oxynitride, hafnium oxide, hafnium oxynitride, gallium oxide, gallium oxynitride, yttrium oxide, yttrium oxynitride, and  $\text{Ga-Zn}$  oxide can be used. In addition, as the insulating layer 22, a nitride insulating film of silicon nitride, silicon nitride oxide, aluminum nitride, or aluminum nitride oxide can also be used. The insulating layer 22 may have a stacked-layer structure, e.g., a stacked-layer structure including at least one oxide insulating film and at least one nitride insulating film.

[0171] The insulating layer 22 preferably has a stacked-layer structure using an insulating material that includes a high-k material. A stacked-layer structure including a high dielectric constant (high-k) material and a material having higher dielectric strength than the high-k material is preferably used. For example, as the insulating layer 22, an insulating film (also referred to as ZAZ) in which zirconium oxide, aluminum oxide, and zirconium oxide are stacked in this order can be used. An insulating film (also referred to as ZAZA) in which zirconium oxide, aluminum oxide, zirconium oxide, and aluminum oxide are stacked in this order can be used, for example. For another example, an insulating film in which hafnium zirconium oxide, aluminum oxide, hafnium zirconium oxide, and aluminum oxide are stacked in this order can be used. The stacking of such an insulator having relatively high dielectric strength, such as aluminum oxide, can increase the dielectric strength and inhibit electrostatic breakdown of the capacitor.

[0172] Alternatively, a material that exhibits ferroelectricity may be used for the insulating layer 22. Examples of the material that exhibits ferroelectricity include metal oxides such as hafnium oxide, zirconium oxide, and  $\text{HfZrO}_X$  ( $X$  is a real number greater than 0). A metal oxide obtained by adding Y (yttrium) to  $\text{HfZrO}_X$  can also be used. When Y is added to  $\text{HfZrO}_X$ , the ferroelectricity can be enhanced.

[0173] In the case where the insulating layer 22 has a two-layer structure, an insulating film having a function of capturing or fixing hydrogen is preferably used as a film in contact with the semiconductor layer 21, and an insulating film having a barrier property against hydrogen is preferably used as a film closer to the conductive layer 23 functioning as the gate electrode. This can inhibit diffusion of hydrogen

into the semiconductor layer 21 from the conductive layer 23 side, so that the transistor can have high reliability.

[0174] As the insulating film that captures or fixes hydrogen, a hafnium oxide film, a hafnium silicate film, an aluminum oxide film, or the like is preferably used. As the insulating film having a barrier property against hydrogen, a silicon nitride film, a silicon nitride oxide film, an aluminum oxide film, a magnesium oxide film, a hafnium oxide film, a gallium oxide film, or the like is preferably used.

[0175] Alternatively, an insulating film that releases oxygen by heating may be used as the film in contact with the semiconductor layer 21, and an insulating film having a barrier property against hydrogen may be used as the film positioned on the conductive layer 23 side. Alternatively, an insulating film that releases oxygen by heating may be used as the film in contact with the semiconductor layer 21, and an insulating film having a function of capturing or fixing hydrogen may be used as the film positioned on the conductive layer 23 side.

[0176] In the case where the insulating layer 22 has a three-layer structure, it is preferable that an insulating film including a material having a lower dielectric constant than other films be used as the film in contact with the semiconductor layer 21, an insulating film having a barrier property against hydrogen and oxygen be used as the film positioned on the conductive layer 23 side, and an insulating film having a function of capturing or fixing hydrogen be used as a film positioned between the film in contact with the semiconductor layer 21 and the film positioned on the conductive layer 23 side. As a low-dielectric-constant material, silicon oxide or silicon oxynitride can be used. With such a structure, oxygen can be supplied from the film in contact with the semiconductor layer 21 to the semiconductor layer 21. The film positioned on the conductive layer 23 side can prevent diffusion of oxygen to the conductive layer 23 side and inhibit oxidation of the conductive layer 23.

[0177] As an insulating film having a barrier property against oxygen, an aluminum oxide film, a silicon nitride film, a hafnium oxide film, a hafnium silicate film, or the like is preferably used. As an insulating film having a barrier property against oxygen and hydrogen, an aluminum oxide film, a silicon nitride film, a hafnium oxide film, or the like is preferably used.

[0178] In the case where the insulating layer 22 has a four-layer structure, it is preferable that an insulating film having a barrier property against oxygen be provided as the film in contact with the semiconductor layer 21, and an insulating film including a material having a lower dielectric constant than other films, an insulating film having a function of capturing or fixing hydrogen, and an insulating film having a barrier property against hydrogen and oxygen be provided in this order from the side closer to the semiconductor layer 21. That is, a structure in which the film in contact with the semiconductor layer 21 is added to the above-described three-layer structure can be employed. When an insulating film having a barrier property against oxygen is used as the film in contact with the semiconductor layer 21, release of oxygen from the semiconductor layer 21 can be inhibited. In that case, an aluminum oxide film is suitably used as the film in contact with the semiconductor layer 21. Aluminum oxide has a function of capturing or fixing hydrogen in addition to having a barrier property against oxygen, and thus has an effect of preventing diffusion of hydrogen into the semiconductor layer 21.

[0179] In the case where the insulating layer **22** has a stacked-layer structure, each insulating film thereof is preferably a thin film. For example, when the insulating layer **22** has a thickness greater than or equal to 1 nm and less than or equal to 20 nm, preferably greater than or equal to 3 nm and less than or equal to 10 nm, the subthreshold swing value (also referred to as S value) of the transistor can be reduced. The thickness of each insulating layer is preferably greater than or equal to 0.1 nm and less than or equal to 10 nm, further preferably greater than or equal to 0.1 nm and less than or equal to 5 nm, further preferably greater than or equal to 0.5 nm and less than or equal to 5 nm, further preferably greater than or equal to 1 nm and less than 5 nm, further preferably greater than or equal to 1 nm and less than or equal to 3 nm.

[0180] As a specific example, a four-layer structure in which an aluminum oxide film, a silicon oxide film, a hafnium oxide film, and a silicon nitride film are stacked in this order from the semiconductor layer **21** side is preferably employed, and their thicknesses are preferably 1 nm, 2 nm, 2 nm, and 1 nm from the semiconductor layer **21** side.

[0181] Note that in this specification and the like, the barrier property refers to a property that does not easily allow diffusion of a target substance (also referred to as a property that does not easily allow passage of a target substance, a property with low permeability of a target substance, or a function of inhibiting diffusion of a target substance). Note that hydrogen described as a target substance refers to at least one of a hydrogen atom, a hydrogen molecule, and a substance bonded to hydrogen, such as a water molecule or OH, for example. Unless otherwise specified, an impurity described as a target substance refers to an impurity in a channel formation region or a semiconductor layer, and for example, refers to at least one of a hydrogen atom, a hydrogen molecule, a water molecule, a nitrogen atom, a nitrogen molecule, a nitrogen oxide molecule (e.g., N<sub>2</sub>O, NO, or NO<sub>2</sub>), and a copper atom. Oxygen described as a target substance refers to, for example, at least one of an oxygen atom and an oxygen molecule.

[0182] Here, a transistor including a metal oxide film can have stable electrical characteristics when surrounded by an insulating film having a function of inhibiting passage of impurities and oxygen. The insulating film having a function of inhibiting passage of impurities and oxygen can have, for example, a single-layer structure or a stacked-layer structure of an insulating film containing one or more of boron, carbon, nitrogen, oxygen, fluorine, magnesium, aluminum, silicon, phosphorus, chlorine, argon, gallium, germanium, yttrium, zirconium, lanthanum, neodymium, hafnium, and tantalum. Specifically, as a material for the insulating film having a function of inhibiting passage of impurities and oxygen, a metal oxide such as aluminum oxide, magnesium oxide, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, or tantalum oxide or a nitride such as aluminum nitride, silicon nitride oxide, or silicon nitride can be used.

[0183] Specifically, as a material for the insulating film having a function of inhibiting passage of oxygen and impurities such as water and hydrogen, a metal oxide such as aluminum oxide, magnesium oxide, gallium oxide, germanium oxide, yttrium oxide, zirconium oxide, lanthanum oxide, neodymium oxide, hafnium oxide, or tantalum oxide can be used. Other examples of the material for the insulating film having a function of inhibiting passage of oxygen

and impurities such as water and hydrogen include oxides containing aluminum and hafnium (hafnium aluminate). Other examples of the material for the insulating layer having a function of inhibiting passage of oxygen and impurities such as water and hydrogen include nitrides such as aluminum nitride, aluminum titanium nitride, silicon nitride oxide, and silicon nitride.

[0184] Examples of a material for an insulating film having a function of capturing or fixing hydrogen include metal oxides such as an oxide containing hafnium, an oxide containing magnesium, an oxide containing aluminum, and an oxide containing aluminum and hafnium (hafnium aluminate). Furthermore, these metal oxides may further contain zirconium, and an example of such a metal oxide is an oxide containing hafnium and zirconium. Note that in a metal oxide having an amorphous structure, some oxygen atoms have a dangling bond, which allows the metal oxide to have a high property of capturing or fixing hydrogen. Thus, these metal oxides preferably have an amorphous structure. For example, these oxides may have an amorphous structure by containing silicon. For example, an oxide containing hafnium and silicon (hafnium silicate) is preferably used. Note that the metal oxide may partly include one or both of a crystal region and a crystal grain boundary.

#### <Conductive Layer>

[0185] The conductive layers **24** and **25** are in contact with the semiconductor layer **21**. Here, when the semiconductor layer **21** is formed using an oxide semiconductor and a part of the conductive layer **24** or the conductive layer **25** in contact with the semiconductor layer **21** is formed using, for example, a metal that is likely to be oxidized such as aluminum, an insulating oxide (e.g., aluminum oxide) may be formed between the conductive layer **24** or **25** and the semiconductor layer **21**, which may inhibit electrical continuity between the conductive layer and the semiconductor layer. Therefore, at least a part of the conductive layer **24** or the conductive layer **25** in contact with the semiconductor layer **21** is preferably formed using a conductive material that is less likely to be oxidized, a conductive material that maintains low electric resistance even when oxidized, or an oxide conductive material.

[0186] For a conductive film in contact with the semiconductor layer **21**, for example, titanium, tantalum nitride, titanium nitride, a nitride containing titanium and aluminum, a nitride containing tantalum and aluminum, ruthenium, ruthenium oxide, ruthenium nitride, an oxide containing strontium and ruthenium, or an oxide containing lanthanum and nickel is preferably used. These materials are preferable because they are conductive materials that are less likely to be oxidized or materials that maintain the conductivity even when oxidized.

[0187] It is also possible to use a conductive oxide such as indium oxide, zinc oxide, In—Sn oxide, In—Zn oxide, In—W oxide, In—W—Zn oxide, In—Ti oxide, In—Ti—Sn oxide, In—Sn—Si oxide, or Ga—Zn oxide. A conductive oxide containing indium is particularly preferable because of its high conductivity. Alternatively, the above-described oxide material such as In—Ga—Zn oxide that can be used for the semiconductor layer **21** can be used for the conductive layer when the carrier concentration is increased.

[0188] For each of the conductive layers **24** and **25**, any of the following structures can be used: a single-layer structure of the above conductive oxide film, a three-layer structure in

which a titanium nitride film, a tungsten film, and a titanium nitride are stacked in this order, a two-layer structure in which a ruthenium film or a ruthenium oxide film is stacked over a tungsten film, a two-layer structure in which a ruthenium film or a ruthenium oxide film is stacked over the above conductive oxide film, a two-layer structure in which the above conductive oxide film is stacked over a ruthenium film or a ruthenium oxide film, or the like, for example.

[0189] The conductive layer 23 serves as a gate electrode and can be formed using a variety of conductive materials. The conductive layer 23 can be formed using, for example, a metal element selected from aluminum, chromium, copper, silver, gold, platinum, tantalum, nickel, cobalt, titanium, molybdenum, tungsten, hafnium, vanadium, niobium, manganese, magnesium, zirconium, beryllium, indium, ruthenium, iridium, strontium, lanthanum, and the like; or an alloy containing any of the above metal elements. It is also possible to use a nitride or an oxide of any of the above metals or the alloy. For example, tantalum nitride, titanium nitride, a nitride containing titanium and aluminum, a nitride containing tantalum and aluminum, ruthenium oxide, ruthenium nitride, an oxide containing strontium and ruthenium, an oxide containing lanthanum and nickel, or the like is preferably used. Alternatively, a semiconductor having high electric conductivity, typified by polycrystalline silicon containing an impurity element such as phosphorus, or silicide such as nickel silicide may be used.

[0190] For the conductive layer 23, the nitride and the oxide that can be used for the conductive layers 24 and 25 may be used.

[0191] The conductive layers 23, 24, and 25 also serve as wirings and thus are preferably formed using stacked low-resistance conductive materials. For example, the above-described low-resistance conductive material that can be used for the conductive layer 23 can also be used for the conductive films 24a and 25b.

#### <Insulating Layer>

[0192] The insulating layer 41 can be used as an interlayer insulating film. The insulating layer 41 is preferably formed by a film formation method such as a sputtering method or a plasma CVD method, for example. It is particularly preferable to employ a sputtering method, in which a hydrogen gas does not need to be used as a deposition gas, to form a film having an extremely low hydrogen content. Consequently, supply of hydrogen to the semiconductor layer 21 is inhibited and the electrical characteristics of the transistor 10 can be stabilized.

[0193] The insulating layer 41 is in contact with the channel formation region of the semiconductor layer 21 and therefore is preferably formed using an oxide insulating film. In particular, an oxide insulating film that releases oxygen by heating is preferably used. An oxide insulating film that can be used as the gate insulating layer can be used as the insulating layer 41.

[0194] Since the insulating layer 41 serves as an interlayer insulating layer, it is preferably formed by a film formation method that enables a higher film formation rate than those of the other insulating layers. For example, a silicon oxide film formed by a plasma CVD method using tetraethyl orthosilicate (TEOS) whose chemical formula is  $\text{Si}(\text{OC}_2\text{H}_5)_4$  (also referred to as a TEOS film) may be used as the insulating layer 41. The productivity can be thus increased.

[0195] The insulating layer 11, an insulating layer 42, the insulating layer 44, the insulating layer 46, and the insulating layer 47 each function as an interlayer insulating layer. For the insulating layer 11, the insulating layer 42, the insulating layer 44, the insulating layer 46, and the insulating layer 47, an insulating material that can be used for the insulating layer 41 can be used.

[0196] The insulating layer 52 functions as the dielectric of the capacitor 30. An insulating material similar to that of the insulating layer 22 can be applied to the insulating layer 52. When the above-described material exhibiting ferroelectricity is used for the insulating layer 52, the capacitor 30 can be a ferroelectric capacitor, which enables a nonvolatile memory device. Note that as the capacitor 30, a resistive random access memory element utilizing a colossal electro resistance (CER) effect can also be used.

[0197] The above is the description of the components.

#### MODIFICATION EXAMPLES

[0198] A structure example partly different from the above structure examples will be described below. Note that portions similar to those described above are denoted by the same reference numerals as those described above and are not described.

##### Modification Example 1

[0199] The structure illustrated in FIG. 8 is different from the above structure example mainly in the shapes of the semiconductor layer 21, the insulating layer 22, and the conductive layer 23.

[0200] In FIG. 8, the semiconductor layer 21 includes a portion in contact with the top surface of the conductive film 25b. The insulating layer 22 is provided to cover the semiconductor layer 21 and includes a portion overlapping with the conductive film 25b with the semiconductor layer 21 therebetween. Thus, in the structure illustrated in FIG. 8, the top surfaces of the semiconductor layer 21 and the insulating layer 22 are not planarized.

[0201] The top surface of the conductive layer 23 is positioned lower than the top surface of the conductive film 25b. Thus, the parasitic capacitance between the conductive layer 23 and the conductive layer 26 and that between the conductive layer 23 and the conductive layer 25 can be reduced. For example, in the case where the upper portion of the conductive layer 23 is removed not by planarization treatment but by etching, the level of the top surface of the conductive layer 23 can be reduced by overetching.

[0202] Here, when the level of the top surface of the conductive layer 23 is lower than the level of the bottom surface of the conductive layer 25, what is called an offset region, to which a gate electric field is not applied, can be formed in the semiconductor layer 21. Meanwhile, when the level of the top surface of the conductive layer 23 is higher than the level of the bottom surface of the conductive layer 25, an offset region is not formed; thus, a transistor with a high on-state current can be achieved. The level of the top surface of the conductive layer 23 can be adjusted in accordance with characteristics needed for the transistor.

##### Modification Example 2

[0203] The structure illustrated in FIG. 9 is different from the above structure examples mainly in the shape of the

conductive layer **51** included in the capacitor **30** and in that the insulating layer **41** has a stacked-layer structure.

[0204] In FIG. 9, an upper end of the conductive layer **51** is positioned below the top surface of the insulating layer **46**, and the upper end of the conductive layer **51** and an upper end of the insulating layer **46** are each rounded. When the conductive layer **51** and the insulating layer **46** that form the formation surface of the insulating layer **52** are not provided with corner portions in this manner, coverage with the insulating layer **52** can be improved and the insulating layer **52** can be prevented from being locally thinned. This can reduce a leakage current of the capacitor **30** can be reduced, so that the reliability can be increased.

[0205] In the example illustrated in FIG. 9, the insulating layer **41** has a stacked-layer structure in which an insulating layer **41a**, an insulating layer **41b**, and an insulating layer **41c** are stacked in this order from the insulating layer **52** side.

[0206] The semiconductor layer **21** is provided in contact with the inner wall of the slit **20** in the insulating layer **41**. An oxide insulating film is preferably used as the insulating layer **41b**. In particular, an oxide insulating film that releases oxygen by heating is preferably used. Furthermore, the insulating layer **41b** is preferably interposed between the insulating layers **41a** and **41c** having a barrier property against oxygen. This enables oxygen contained in the insulating layer **41b** to be enclosed in a region surrounded by the insulating layers **41a** and **41c** and the semiconductor layer **21**. Furthermore, oxygen in the insulating layer **41b** can be prevented from decreasing by being released during the process. Accordingly, oxygen can be supplied to the semiconductor layer **21** more efficiently.

[0207] A part of the semiconductor layer **21** that is in contact with the insulating layer **41b** is a region where oxygen vacancies are reduced, i.e., an i-type region. The other part of the semiconductor layer **21** that is not in contact with the insulating layer **41b** is preferably an n-type region including a large amount of carriers. That is, the part of the semiconductor layer **21** that is in contact with the insulating layer **41b** can be referred to as a channel formation region and regions of the outer side of the channel formation region can be referred to as low-resistance regions (or a source region or a drain region).

[0208] The insulating layer **41b** is preferably a film that includes hydrogen as little as possible because the insulating layer **41b** is in contact with the semiconductor layer **21**. Bonding of oxygen vacancies in the semiconductor layer **21** and hydrogen causes generation of carriers, which might affect the threshold voltage of the transistor **10**, for example. Thus, the insulating layer **41b** may be an insulating film which does not easily allow diffusion of hydrogen other than an oxide insulating film. For example, a single layer of an insulating film having a barrier property against hydrogen and oxygen can be used as the insulating layer **41**.

[0209] Since the semiconductor layer **21** and the insulating layer **22** are formed along the inner wall of the slit **20** in the insulating layer **41**, the thicknesses of the semiconductor layer **21** and the insulating layer **22** are sometimes reduced in the slit **20** by some film formation methods. For example, when a film formation method such as a sputtering method or a plasma CVD method is used, a film formed on a surface inclined with respect to the substrate surface or a surface perpendicular to the substrate surface tends to be thinner than a film formed on a surface parallel to the substrate

surface. By contrast, a film formation method such as an atomic layer deposition (ALD) method or a thermal CVD method allows a film with a uniform thickness to be formed on a surface with any angle. The semiconductor layer **21** and the insulating layer **22** are preferably formed by an ALD method when an angle formed by a side wall of the slit **20** in the insulating layer **41** and the substrate surface is 75° or more, 80° or more, or 85° or more, for example.

[0210] The insulating layer **41b** can be used as an interlayer insulating film. The insulating layer **41b** is preferably formed by a film formation method such as a sputtering method or a plasma CVD method, for example. It is particularly preferable to employ a sputtering method, in which a hydrogen gas does not need to be used as a deposition gas, to form a film having an extremely low hydrogen content. Consequently, supply of hydrogen to the semiconductor layer **21** is inhibited and the electrical characteristics of the transistor **10** can be stabilized.

[0211] The insulating layer **41b** is in contact with the channel formation region of the semiconductor layer **21** and therefore is preferably formed using an oxide insulating film. In particular, an oxide insulating film that releases oxygen by heating is preferably used. An oxide insulating film that can be used as the gate insulating layer can be used as the insulating layer **41b**. Since the insulating layer **41b** serves as an interlayer insulating layer, it is preferably formed by a film formation method that enables a higher film formation rate than those of the other insulating layers. For example, an insulating film formed by a plasma CVD method using tetraethyl orthosilicate (TEOS) whose chemical formula is  $\text{Si}(\text{OC}_2\text{H}_5)_4$  may be used as the insulating layer **41**. The productivity can be thus increased.

[0212] As the insulating layers **41a** and **41c**, films which does not easily allow diffusion of hydrogen are preferably used. The layers **41a** and **41c** which does not easily allow diffusion of hydrogen are provided above and below the insulating layer **41b**, respectively, thereby preventing entry of hydrogen from the outside into the insulating layer **41b** in contact with the semiconductor layer **21**.

[0213] For the insulating layer **41a** and the insulating layer **41c**, for example, one or more of silicon nitride, silicon nitride oxide, silicon oxynitride, aluminum oxide, aluminum oxynitride, aluminum nitride, hafnium oxide, and hafnium aluminate can be used. Silicon nitride and silicon nitride oxide are particularly suitable for the insulating layer **41a** and the insulating layer **41c** because they release fewer impurities (e.g., water and hydrogen) and are less likely to transmit oxygen and hydrogen.

### Modification Example 3

[0214] The structure of the transistor **10A** illustrated in FIG. 10A is different from the above structure example mainly in including an insulating layer **22fe** functioning as a ferroelectric instead of the insulating layer **22** and not including the capacitor **30**.

[0215] When the insulating layer **22fe** functioning as a ferroelectric is used as a gate insulating layer of the transistor **10A**, the transistor **10A** can be used as a ferroelectric transistor (ferroelectric field effect transistor: FeFET). Another example of the structure of the ferroelectric transistor is a structure in which a ferroelectric capacitor is connected to a gate of the transistor. The threshold voltage of the ferroelectric transistor can be changed when a certain voltage or higher is applied to the gate thereof. Thus, data

can be retained, and the ferroelectric transistor can function as a nonvolatile memory element. Thus, the capacitor 30 for retaining data is not necessary.

[0216] A material exhibiting ferroelectricity is used for the insulating layer 22<sup>e</sup>. Examples of the material exhibiting ferroelectricity include oxides such as hafnium oxide, zirconium oxide, and hafnium zirconium oxide. A material obtained by adding a Group 3 (Group IIIa) element to any of these oxides is preferably used. For example, the oxide preferably contains one or more of scandium, yttrium, and an element belonging to lanthanoid. In particular, yttrium, lanthanum, or scandium is preferable because it is relatively easy to handle and has high compatibility with a semiconductor manufacturing process. When such an element is added, not only stable ferroelectricity can be exhibited but also degradation of characteristics caused by rewriting repeatedly can be inhibited, so that reliability can be improved. Furthermore, the withstand voltage of the insulating layer 22<sup>e</sup> can be increased. For example, the element is preferably added at higher than or equal to 0.5 at % and lower than or equal to 10 at %. Other examples of the additive element include silicon, aluminum, gadolinium, and scandium. Note that for the insulating layer 22<sup>e</sup>, not only a material exhibiting ferroelectricity but also a material exhibiting anti-ferroelectricity can be used.

[0217] An oxide containing one or both of hafnium and zirconium exhibits ferroelectricity easily even when it is used in an extremely thin film formed by a formation method of a thin film, such as a sputtering method or an atomic layer deposition (ALD) method, and thus the oxide has high compatibility with a semiconductor manufacturing process and can reduce the manufacturing cost.

[0218] For the insulating layer 22<sup>e</sup>, a piezoelectric ceramic having a perovskite structure, such as barium titanate, lead titanate, strontium titanate, barium strontium titanate (BST), lead zirconate titanate (PZT), strontium bismuth tantalate (SBT), or bismuth ferrite (BFO), may be used.

[0219] For the insulating layer 22<sup>e</sup>, an organic ferroelectric such as polyvinylidene fluoride (PVDF) or a copolymer of vinylidene fluoride (VDF) and trifluoroethylene (TrFE).

[0220] As the material exhibiting ferroelectricity, a mixture or compound containing a plurality of materials selected from the above-listed materials can be used, for example. Alternatively, the insulating layer 22<sup>e</sup> can have a stacked-layer structure of a plurality of materials selected from the above-listed materials.

[0221] Specifically, as the material exhibiting ferroelectricity, hafnium oxide, a material containing hafnium oxide and zirconium oxide (HZO), and a material containing yttrium in addition to HZO (HYZO) are preferable because they exhibit ferroelectricity even when being a thin film of several nanometers. With a film containing hafnium oxide, HZO, or HYZO, the thickness of the insulating layer 22<sup>e</sup> can be greater than or equal to 3 nm and less than or equal to 100 nm, preferably greater than or equal to 3 nm and less than or equal to 50 nm, further preferably greater than or equal to 3 nm and less than or equal to 20 nm, still further preferably greater than or equal to 4 nm and less than or equal to 10 nm.

[0222] In the case where hafnium zirconium oxide (Hf<sub>x</sub>ZrO<sub>x</sub> (X is a real number greater than 0)) is used as the material exhibiting ferroelectricity, film formation is preferably performed by an ALD method, particularly a thermal ALD method. It is preferable to use an ALD method

(including a thermal ALD method) using plasma to increase reactivity (plasma enhanced ALD (PEALD) method).

[0223] In the case of using a thermal ALD method, a material containing an organometallic compound can be used as a precursor. For example, in the case where hafnium zirconium oxide is used, an organometallic compound such as tetrakis(ethylmethylamide)hafnium (TEMAHf) can be used as a precursor containing hafnium, and an organometallic compound such as tetrakis(ethylmethylamide)zirconium (TEMAZr) can be used as a precursor containing zirconium. Alternatively, a material that does not contain hydrocarbon can be used. Examples of the precursor that does not contain hydrocarbon include a chlorine-based material. Note that in the case of using hafnium zirconium oxide, a chlorine-based precursor such as HfCl<sub>4</sub> or ZrCl<sub>4</sub> can be used as a precursor.

[0224] Note that in the case where an oxide such as hafnium oxide, zirconium oxide, or hafnium zirconium oxide is used for the insulating layer 22<sup>e</sup>, the remanent polarization can sometimes be increased when an appropriate amount of carbon is contained. In this case, for example, the element is preferably added at higher than or equal to 0.5 at % and lower than or equal to 10 at %.

[0225] In the case where a film of hafnium zirconium oxide is used for the insulating layer 22<sup>e</sup>, it is preferable that hafnium and zirconium be alternately deposited at a ratio of 1:1 by a thermal ALD method or an ALD method using plasma.

[0226] As an oxidizer used for the thermal ALD method or the ALD method using plasma, H<sub>2</sub>O or O<sub>3</sub> can be used. Note that the oxidizer is not limited thereto; O<sub>2</sub>, O<sub>3</sub>, N<sub>2</sub>O, NO<sub>2</sub>, H<sub>2</sub>O, H<sub>2</sub>O<sub>2</sub>, or the like can be used, and two or more of them may be used. In particular, to reduce the hydrogen concentration and the nitrogen concentration in the film, O<sub>2</sub> or O<sub>3</sub> is preferably used as the oxidizer, and O<sub>3</sub> is further preferably used.

[0227] The hydrogen concentration in a film used for the insulating layer 22<sup>e</sup> is preferably low. This can prevent diffusion of hydrogen from the insulating layer 22<sup>e</sup> into the semiconductor layer 21 and an increase in the carrier concentration in the semiconductor layer 21. Specifically, the hydrogen concentration in the film is preferably lower than or equal to 5×10<sup>20</sup> atoms/cm<sup>3</sup>, further preferably lower than or equal to 1×10<sup>20</sup> atoms/cm<sup>3</sup>.

[0228] A crystal structure of the film used for the insulating layer 22<sup>e</sup> is not particularly limited as long as the crystal structure is non-centrosymmetric and has polarity. For example, a crystal system except a cubic crystal system can be employed as the crystal structure of the film used for the insulating layer 22<sup>e</sup>. The film used for the insulating layer 22<sup>e</sup> may have a single crystal structure or a polycrystalline structure, or may have a composite structure including an amorphous structure and a crystal structure.

[0229] The conductive layer 23 that is in contact with the insulating layer 22<sup>e</sup> or positioned in the vicinity of the insulating layer 22<sup>e</sup> is preferably formed using a conductive material having a function of absorbing oxygen. Accordingly, oxygen can be absorbed from the insulating layer 22<sup>e</sup>, so that the concentration of oxygen vacancies in the insulating layer 22<sup>e</sup> can be increased. Thus, the remanent polarization of the insulating layer 22<sup>e</sup> can be increased. As a conductive material having a function of absorbing oxygen, a metal or an alloy is preferably used. In particular, tungsten, molybdenum, titanium, tantalum, or the like is

preferably used. Tungsten, which easily increases the remanent polarization of the insulating layer **22/e** in terms of stress, is particularly preferable.

[0230] Moreover, the conductive layer **23** that is in contact with the insulating layer **22/e** or positioned in the vicinity of the insulating layer **22/e** is preferably formed using a conductive material which does not easily allow diffusion of oxygen. Accordingly, the withstand voltage of the insulating layer **22/e** can be increased, and the rewrite endurance of the ferroelectric capacitor can be improved. It is particularly preferable to use a metal nitride such as titanium nitride or tantalum nitride.

[0231] The conductive layer **23** may have a stacked-layer structure. In that case, a low-resistance conductive material is preferably used for a layer not in contact with the insulating layer **22/e**. For example, as the low-resistance conductive material, a metal or an alloy containing one or more selected from aluminum, chromium, copper, silver, gold, platinum, zinc, tantalum, nickel, titanium, iron, cobalt, molybdenum, tungsten, hafnium, vanadium, niobium, manganese, magnesium, zirconium, beryllium, indium, ruthenium, iridium, strontium, lanthanum, and the like can be used. It is particularly preferable to use a high-melting-point material such as tungsten, molybdenum, tantalum, ruthenium, or hafnium because the temperature of heat treatment performed later can be high. Note that in addition to the above low-resistance conductive material, an oxide material such as indium tin oxide, indium tin oxide to which silicon is added, indium zinc oxide, or indium gallium zinc oxide may be used.

[0232] The insulating layer **22/e** may have a function of capturing or fixing hydrogen. As an insulating film that captures or fixes hydrogen, a hafnium oxide film, a hafnium silicate film, an aluminum oxide film, a hafnium zirconium oxide film, or the like is preferably used. With the insulating layer **22/e** having a function of capturing or fixing hydrogen, hydrogen that might diffuse into the semiconductor layer **21** can be reduced, so that a highly reliable transistor can be provided. Furthermore, the above-described insulating film having a barrier property against hydrogen is preferably provided outside the insulating layer **22/e** (on the conductive layer **23** side), in which case diffusion of hydrogen from the conductive layer **23** side can be inhibited. It is particularly preferable to use a silicon nitride film or a silicon nitride oxide film as the insulating film having a barrier property against hydrogen.

[0233] Although the insulating layer **22/e** is used instead of the insulating layer **22** in FIG. 10A, the insulating layer **22** may have a stacked-layer structure, and the insulating layer **22/e** may be used as one of the stacked layers.

[0234] FIGS. 10B to 10G are enlarged views of part of the insulating layer **41**, part of the semiconductor layer **21**, part of the insulating layer **22**, and part of the conductive layer **23**.

[0235] FIG. 10B illustrates an example in which the insulating layer **22** has a stacked-layer structure in which an insulating layer **22/a** and the insulating layer **22/e** are stacked in this order from the semiconductor layer **21** side. A material similar to that of the insulating layer **22** can be used for the insulating layer **22/a**. A leakage current between the conductive layer **23** and the semiconductor layer **21** can be inhibited by including the insulating layer **22/a**.

[0236] FIG. 10C illustrates an example in which the insulating layer **22** has a five-layer structure in which the

insulating layer **22/a**, an insulating layer **22/b**, an insulating layer **22/c**, an insulating layer **22/d**, and the insulating layer **22/e** are stacked in this order from the semiconductor layer **21** side.

[0237] The insulating layer **22/a**, the insulating layer **22/b**, the insulating layer **22/c**, and the insulating layer **22/d** can be individually formed using any of the insulating materials that can be used for the insulating layer **22**. For example, it is preferable to use an aluminum oxide film as the insulating layer **22/a**, a silicon oxide film as the insulating layer **22/b**, a hafnium oxide film as the insulating layer **22/c**, and a silicon nitride film as the insulating layer **22/d**, and it is also preferable that the thicknesses of the insulating layers be 1 nm, 2 nm, 2 nm, and 1 nm in this order from the semiconductor layer **21** side.

[0238] FIG. 10D illustrates an example in which the insulating layer **22** has a four-layer structure in which the insulating layer **22/a**, the insulating layer **22/b**, the insulating layer **22/e**, and the insulating layer **22/c** are stacked in this order from the semiconductor layer **21** side. For example, it is preferable to use an aluminum oxide film as the insulating layer **22/a**, a silicon oxide film as the insulating layer **22/b**, and a silicon nitride film as the insulating layer **22/c**.

[0239] FIG. 10E illustrates an example in which the insulating layer **22** has a four-layer structure in which the insulating layer **22/a**, the insulating layer **22/e**, the insulating layer **22/b**, and the insulating layer **22/c** are stacked in this order from the semiconductor layer **21** side. For example, it is preferable to use an aluminum oxide film as the insulating layer **22/a**, a silicon oxide film as the insulating layer **22/b**, and a silicon nitride film as the insulating layer **22/c**.

[0240] FIG. 10F illustrates an example in which the insulating layer **22** has a five-layer structure in which the insulating layer **22/a**, the insulating layer **22/e**, the insulating layer **22/b**, the insulating layer **22/c**, and the insulating layer **22/d** are stacked in this order from the semiconductor layer **21** side. For example, it is preferable to use an aluminum oxide film as the insulating layer **22/a**, a silicon nitride film as the insulating layer **22/b**, a silicon oxide film as the insulating layer **22/c**, and a silicon nitride film as the insulating layer **22/d**. In that case, either the insulating layer **22/b** or the insulating layer **22/d** may be omitted.

[0241] FIG. 10G illustrates an example in which a conductive layer **28** is provided between the insulating layer **22** and the insulating layer **22/e**. A ferroelectric capacitor can be formed by the conductive layer **28**, the insulating layer **22/e**, and the conductive layer **23**. For the conductive layer **28**, any of the above-described conductive materials that can be used for the conductive layer **23** can be used. For example, titanium or titanium nitride is preferably used for the conductive layer **28**.

[0242] FIG. 10G illustrates an example in which the insulating layer **22** has a four-layer structure in which the insulating layer **22/a**, the insulating layer **22/b**, the insulating layer **22/c**, and the insulating layer **22/d** are stacked in this order from the semiconductor layer **21** side.

[0243] Note that the stacked-layer structure of the insulating layer **22** is not limited to the examples described above with reference to FIGS. 10C to 10G, and any of the insulating films that can be used as the insulating layer **22** can be stacked as appropriate.

[0244] The above is the description of the modification examples.

## [Manufacturing Method Example]

[0245] An example of a method for manufacturing a semiconductor device of one embodiment of the present is described below. Here, the semiconductor device including the memory cell 15 described in the above structure example is described as an example.

[0246] Note that thin films included in the semiconductor device (e.g., insulating films, semiconductor films, and conductive films) can be formed by a sputtering method, a chemical vapor deposition (CVD) method, a vacuum evaporation method, a pulsed laser deposition (PLD) method, an atomic layer deposition (ALD) method, or the like.

[0247] Alternatively, the thin films included in the semiconductor device (e.g., an insulating film, a semiconductor film, and a conductive film) can be formed by a method such as spin coating, dipping, spray coating, inkjet printing, dispensing, screen printing, or offset printing or with a doctor knife, a slit coater, a roll coater, a curtain coater, or a knife coater.

[0248] Examples of the sputtering method include an RF sputtering method using a high-frequency power source for a sputtering power source, a DC sputtering method using a DC power source, and a pulsed DC sputtering method in which voltage applied to an electrode is changed in a pulsed manner. For film formation using an insulating target, an RF sputtering method is preferably used. A DC sputtering method is used mainly in the case of film formation using a conductive target. In a DC sputtering method, not only formation of a conductive film but also formation of an insulating film is possible by reactive sputtering using a pulsed DC sputtering method. The pulsed DC sputtering method can be specifically used for forming a film of a compound such as an oxide, a nitride, or a carbide by a reactive sputtering method.

[0249] CVD methods can be classified into a plasma enhanced CVD (PECVD) method using plasma, a thermal CVD (TCVD) method using heat, a photo CVD method using light, and the like. Moreover, CVD methods can be classified into a metal CVD (MCVD) method and a metal organic CVD (MOCVD) method according to a source gas.

[0250] A high-quality film can be obtained at a relatively low temperature through a plasma CVD method. A thermal CVD method does not use plasma and thus causes less plasma damage to an object. A thermal CVD method yields a film with few defects because of no plasma damage during film formation.

[0251] As an ALD method, a thermal ALD method, in which a precursor and a reactant react with each other only by a thermal energy, a PEALD method, in which a reactant excited by plasma is used, or the like can be used.

[0252] Unlike a sputtering method, a CVD method and an ALD method are less likely to be influenced by the shape of an object to be processed and thus enable favorable step coverage. In particular, an ALD method allows excellent step coverage and excellent thickness uniformity and can be suitably used to cover a surface of an opening portion with a high aspect ratio, for example. Note that an ALD method has a relatively low film formation rate; hence, in some cases, an ALD method is preferably combined with another film formation method with a high film formation rate, such as a CVD method.

[0253] By a CVD method, a film with a certain composition can be formed by adjusting the flow rate ratio of the source gases. For example, a CVD method enables forma-

tion of a film whose composition is gradually changed by changing the flow rate ratio of the source gases during film formation. In the case where a film is formed while the flow rate ratio of the source gases is changed, as compared with the case where a film is formed using a plurality of film formation chambers, the time taken for the film formation can be shortened because the time taken for transfer or pressure adjustment is not required. Hence, the productivity of the semiconductor device can be improved in some cases.

[0254] An ALD method, in which a plurality of different kinds of precursors are introduced at a time, enables formation of a film with a desired composition. In the case where a plurality of different kinds of precursors are introduced, the number of cycles for each precursor is controlled, whereby a film with a desired composition can be formed. Furthermore, a film whose composition is continuously changed can be formed as in the CVD method.

[0255] Thin films included in the semiconductor device can be formed by a photolithography method or the like. Besides, a nanoimprinting method, a sandblasting method, a lift-off method, or the like may be employed to process the thin films. Alternatively, island-shaped thin films may be directly formed by a film formation method using a shielding mask such as a metal mask.

[0256] There are two typical examples of photolithography methods. In one of the methods, a resist mask is formed over a thin film to be processed, the thin film is processed by etching or the like, and then the resist mask is removed. In the other method, a photosensitive thin film is formed and then processed into a desired shape by light exposure and development.

[0257] As light for exposure in a photolithography method, it is possible to use light with the i-line (wavelength: 365 nm), light with the g-line (wavelength: 436 nm), light with the h-line (wavelength: 405 nm), or light in which the i-line, the g-line, and the h-line are mixed. Alternatively, ultraviolet light, KrF laser light, ArF laser light, or the like can be used. Exposure may be performed by liquid immersion exposure technique. As the light for exposure, extreme ultraviolet (EUV) light or X-rays may also be used. Instead of the light for exposure, an electron beam can be used. EUV, X-rays, or an electron beam is preferably used to enable extremely minute processing. Note that a photomask is not needed when exposure is performed by scanning with a beam such as an electron beam.

[0258] For etching of thin films, a dry etching method, a wet etching method, a sandblast method, or the like can be used.

[0259] FIG. 11A to FIG. 17B are schematic cross-sectional views corresponding to steps in the manufacturing method example described below. Each drawing illustrates a cross section corresponding to FIG. 2 on the left side of the dashed-dotted line, and a cross section corresponding to FIG. 3 on the right side.

[0260] First, a substrate (not illustrated) is prepared, and the insulating layer 11 is formed over the substrate.

[0261] As the substrate, a substrate that has heat resistance high enough to withstand at least heat treatment performed later can be used.

[0262] An inorganic insulating film such as a silicon oxide film or a silicon oxynitride film can be used as the insulating layer 11. The insulating layer 11 can be formed by a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like. In the case where the

formation surface of the insulating layer 11 is not flat, planarization treatment may be performed after the deposition of the insulating layer 11 so that the insulating layer 11 has a flat top surface.

[0263] Next, a conductive film to be the conductive layer 55 is formed over the insulating layer 11. The conductive film can be formed by a film formation method such as a sputtering method, an ALD method, or a CVD method. Next, a resist mask is formed over the conductive film, and an unnecessary portion of the conductive film is removed by etching, whereby the conductive layer 55 is formed. The conductive layer 55 can have a plate-like shape, a line-like shape, or a lattice-like shape.

[0264] Next, an insulating film may be formed to cover the conductive layer 55, and then planarization treatment may be performed until the top surface of the conductive layer 55 is exposed. Thus, the conductive layer 55 can be embedded in an insulating layer (not illustrated). Although an example in which the insulating layer (not illustrated) is formed after the formation of the conductive layer 55 is described here, the conductive layer 55 and the insulating layer may be formed in the following manner: an insulating film is formed, an opening (or a depressed portion) for embedding the conductive layer 55 is formed in the insulating film, a conductive film to be the conductive layer 55 is formed, and planarization treatment is performed until the surface of the insulating film is exposed. For the planarization treatment, a chemical mechanical polishing (CMP) method, a dry etching method, or the like can be used, for example.

[0265] Next, the insulating layer 46 is formed over the conductive layer 55 (FIG. 11A). The insulating layer 46 can be formed by a film formation method such as a sputtering method, an ALD method, or a CVD method.

[0266] Note that in the case where the conductive layer 55 is not embedded in the insulating layer which is not illustrated, the top surface of the insulating layer 46 after its formation can have an unevenness reflecting the shape of the conductive layer 55. In that case, planarization treatment is preferably performed on the top surface of the insulating layer 46.

[0267] Next, the opening 40 reaching the conductive layer 55 is formed in the insulating layer 46 (FIG. 11B). At this time, part of the top surface of the conductive layer 55 is etched in some cases. Etching is preferably performed such that a curved surface is formed at the upper portion of the conductive layer 55.

[0268] Next, a conductive film 51f to be the conductive layer 51 is formed to cover the top surface of the insulating layer 46, the side surface of the insulating layer 46 in the opening 40, and the top surface of the conductive layer 55 in the opening 40 (FIG. 11C). The conductive film 51f can be formed by a CVD method, an ALD method, a sputtering method, or the like. In terms of coverage, the conductive film 51f is particularly preferably formed by a CVD method.

[0269] A sacrificial layer is formed over the conductive film to cover the depressed portion in the opening 40, planarization treatment is performed until the top surface of the insulating layer 46 is exposed, and the sacrificial layer is removed, whereby the conductive layer 51 positioned only inside the opening 40 can be formed (FIG. 12A).

[0270] Here, at the time of planarization treatment or removal of the sacrificial layer, the level of the top surface of the conductive layer 51 is lower than the level of the top surface of the insulating layer 46 in some cases. In addition,

the edges of the upper end portion of the conductive layer 51 and the upper end portion of the insulating layer 46 in the opening 40 are removed and rounded in some cases. Thus, the structure illustrated in FIG. 9 can be obtained.

[0271] Next, the insulating layer 52 is formed along the surfaces of the insulating layer 46 and the conductive layer 51. The insulating layer 52 can be formed by a film formation method such as a sputtering method, an ALD method, or a CVD method; particularly, an ALD method is preferable in terms of coverage. Next, a conductive film 24af to be the conductive film 24a is formed over the insulating layer 52 to fill the depressed portion in the opening 40 of the insulating layer 46. After that, the top surface of the conductive film 24af may be planarized as needed. Next, a conductive film 24bf to be the conductive film 24b is formed over the conductive film 24af (FIG. 12B). The conductive films 24af and 24bf can be formed by a film formation method such as a sputtering method, an ALD method, or a CVD method.

[0272] Next, a resist mask is formed over the conductive film 24bf and unnecessary portions of the conductive films are removed by etching, whereby the conductive layer 24 including the conductive film 24a and the conductive film 24b is formed (FIG. 12C). At this time, the capacitor 30 can be formed.

[0273] Next, the insulating layer 41 is formed to cover the conductive layer 24, and planarization treatment is performed on the top surface of the insulating layer 41. The insulating layer 41 can be formed by a film formation method such as a sputtering method, an ALD method, or a CVD method.

[0274] The insulating layer 41 is preferably an oxide film including a large amount of oxygen so that oxygen is released by heating and including a small amount of hydrogen. The insulating layer 41 can be formed by a film formation method such as a PECVD method, a sputtering method, or an ALD method, and is particularly preferably formed by a sputtering method. In particular, when a gas containing not hydrogen but oxygen is used as a deposition gas, an insulating film including an extremely small amount of hydrogen and an excess amount of oxygen can be formed. When the insulating layer 41 is deposited in this manner, oxygen can be supplied to the channel formation region of the semiconductor layer 21 from the insulating layer 41, so that oxygen vacancies can be reduced.

[0275] Next, heat treatment may be performed. The heat treatment is preferably performed at a temperature higher than or equal to 250°C. and lower than or equal to 650°C., preferably higher than or equal to 300°C. and lower than or equal to 500°C., further preferably higher than or equal to 320°C. and lower than or equal to 450°C. Note that the heat treatment is performed in a nitrogen gas atmosphere, an inert gas atmosphere, or an atmosphere containing an oxidizing gas at 10 ppm or more, 1% or more, or 10% or more. For example, in the case where the heat treatment is performed in a mixed atmosphere of a nitrogen gas and an oxygen gas, the proportion of the oxygen gas is preferably approximately 20%. The heat treatment may be performed under reduced pressure. Alternatively, the heat treatment may be performed in such a manner that heat treatment is performed in a nitrogen gas atmosphere or an inert gas atmosphere, and then another heat treatment is performed in an atmosphere containing an oxidizing gas at 10 ppm or more, 1% or more, or 10% or more in order to compensate for released oxygen. By the above-described heat treatment, impurities such as

water and hydrogen included in the insulating layer 41, for example, can be reduced before an oxide semiconductor film to be the semiconductor layer is formed.

[0276] The gas used in the above heat treatment is preferably highly purified. For example, the amount of moisture contained in the gas used in the above-described heat treatment is preferably 1 ppb (0.001 ppm) or less, preferably 0.1 ppb or less, and further preferably 0.05 ppb or less. The heat treatment using a highly purified gas can, for example, prevent the entry of moisture into the insulating layer 41 as much as possible.

[0277] After the formation of the insulating layer 41, treatment for supplying oxygen to the insulating layer 41 may be performed. Accordingly, oxygen can be supplied from the insulating layer 41 to a semiconductor film 21f by heat applied after the formation of the semiconductor film 21f later, or the like.

[0278] Examples of the treatment for supplying oxygen include heat treatment in an oxygen-containing atmosphere, plasma treatment in an oxygen-containing atmosphere (including microwave plasma), and the like, or an oxide film (preferably a metal oxide film) may be formed by a sputtering method in an oxygen-containing atmosphere to supply oxygen to the insulating layer. The formed oxide film may be removed immediately or left as it is. Note that examples of the atmosphere containing oxygen include not only an atmosphere containing an oxygen gas ( $O_2$ ) but also an atmosphere containing a gas of a compound containing oxygen, such as ozone ( $O_3$ ) or dinitrogen monoxide ( $N_2O$ ).

[0279] Next, a conductive film 25af to be the conductive film 25a and a conductive film 25bf to be the conductive film 25b are stacked over the insulating layer 41 (FIG. 13A). The conductive film 25af and the conductive film 25bf can each be formed by a film formation method such as a sputtering method, an ALD method, or a CVD method.

[0280] Next, a resist mask is formed over the conductive film 25bf, and unnecessary portions of the conductive films are removed, whereby the conductive films 25a and 25b are formed. Next, an insulating film to be the insulating layer 42 is formed and planarization treatment is performed until the top surface of the conductive film 25b is exposed, whereby the insulating layer 42 can be formed (FIG. 13B). Thus, the conductive film 25a and the conductive film 25b can be embedded in the insulating layer 42.

[0281] Next, a resist mask is formed over the conductive film 25b and the insulating layer 42, and the slit 20 is formed in the conductive film 25b, the conductive film 25a, the insulating layer 42, and the insulating layer 41 (FIG. 14A). At the time of forming the slit 20, part of the conductive film 24b positioned at the bottom portion of the slit 20 is preferably etched to form a depressed portion in the conductive film 24b. At this time, etching is preferably performed so that a concave surface is formed at an upper portion of the conductive film 24b. As illustrated on the right side in FIG. 14A, a concave surface is preferably formed also on the top surface of the insulating layer 41 positioned at the bottom portion of the slit 20 in a portion where the conductive film 24b is not provided.

[0282] At the time of forming the slit 20, sidewalls of the slit 20 (side surfaces of the conductive film 25b, the conductive film 25a, the insulating layer 42, and the insulating layer 41) are preferably processed by anisotropic dry etching so as to be substantially perpendicular to the formation surface. Note that the sidewall of the slit 20 may be inclined

relative to the direction perpendicular to the formation surface to have a tapered shape, depending on the processing conditions.

[0283] Next, the semiconductor film 21f to be the semiconductor layer 21 is formed to cover the top and side surfaces of the conductive film 25b, the side surface of the conductive film 25a, the side and top surfaces of the insulating layer 41, and the top surface of the conductive film 24b.

[0284] As the semiconductor film 21f, a metal oxide film having semiconductor characteristics (oxide semiconductor film) can be used. The formation of the metal oxide film can be performed by appropriately using a sputtering method, a CVD method, an MBE method, a PLD method, an ALD method, or the like. Here, the metal oxide film is preferably formed in contact with the substantially perpendicular side surface of the insulating layer 41. Thus, the metal oxide film is preferably formed by a film formation method with favorable coverage, and is further preferably formed by an ALD method.

[0285] The metal oxide film preferably has crystallinity. It is particularly preferable that the metal oxide film of one embodiment of the present invention include a metal oxide having a CAAC structure.

[0286] Note that treatment for increasing the crystallinity of the metal oxide film is preferably performed during or after the formation of the metal oxide film. Examples of the treatment for increasing the crystallinity of the metal oxide film include heat treatment, plasma treatment, microwave (typically, 2.45 GHz) treatment, microwave plasma treatment, and light (e.g., ultraviolet light) irradiation treatment. Some of these treatments may be performed concurrently or sequentially. For example, heat treatment and microwave plasma treatment can be performed concurrently. Alternatively, microwave plasma treatment can be performed after heat treatment.

[0287] It is further preferable that the treatment for increasing the crystallinity of the metal oxide film be performed a plurality of times during the formation of the metal oxide film. For example, in the case where the metal oxide film is formed by an ALD method, microwave plasma treatment is preferably performed every time an atomic layer is formed. Alternatively, the treatment for increasing crystallinity is preferably performed every time the metal oxide film with a thickness in a predetermined range is formed, in which case the productivity can be increased. Specifically, the metal oxide film is preferably formed in the following manner: a first metal oxide film with a thickness greater than or equal to 1 nm and less than or equal to 10 nm is formed, first microwave plasma treatment is performed, a second metal oxide film with a thickness greater than or equal to 1 nm and less than or equal to 10 nm is formed, and then second microwave plasma treatment is performed.

[0288] Note that methods for forming the first metal oxide film and the second metal oxide film are not particularly limited, and can be an ALD method or a sputtering method. It is particularly preferable to form the first metal oxide film by an ALD method, in which case entry (also referred to as mixing) of an element of a layer on which the first metal oxide film is formed into the first and second metal oxide films can be prevented. Forming the first metal oxide film by an ALD method is particularly preferable in the case where the element of the layer on which the first metal oxide film is formed hinders crystallization of a metal oxide (e.g., the

case where silicon, carbon, or the like is contained in the layer). The first metal oxide film and the second metal oxide film may have different compositions. Although the stacked-layer structure of the first metal oxide film and the second metal oxide film is exemplified here, one embodiment of the present invention is not limited thereto. Treatment similar to the above treatment can be performed on the metal oxide film having a single-layer structure or a stacked-layer structure of three or more layers.

[0289] The treatment for increasing the crystallinity of the metal oxide film may be performed after the formation of the metal oxide film. Specifically, after the formation of the metal oxide film, the treatment may be performed directly on the metal oxide film, or may be performed on the metal oxide film through another film such as an insulating film formed over the metal oxide film layer. For example, microwave plasma treatment may be performed on the metal oxide film after the formation of the metal oxide film; alternatively, an insulating film (e.g., a silicon nitride film, a silicon oxide film, or an aluminum oxide film) may be formed after the deposition of the metal oxide film, and then heat treatment or microwave plasma treatment may be performed on the metal oxide film through the insulating film.

[0290] Note that the treatment for increasing the crystallinity of the metal oxide film can also serve as treatment for removing impurities contained in the metal oxide film. For example, carbon, hydrogen, nitrogen, and the like contained in the metal oxide film can be suitably removed. Alternatively, by performing the treatment for increasing the crystallinity of the metal oxide film layer in an oxygen gas atmosphere, oxygen vacancies in the metal oxide film layer can be reduced.

[0291] During the treatment for increasing the crystallinity of the metal oxide film, the temperature of the heat treatment (or the substrate temperature) is preferably higher than or equal to room temperature (e.g., 25° C.), higher than or equal to 100° C. and lower than or equal to 700° C., higher than or equal to 100° C. and lower than or equal to 600° C., or higher than or equal to 300° C. and lower than or equal to 450° C.

[0292] By increasing the crystallinity of the metal oxide film, a highly reliable transistor can be obtained.

[0293] The metal oxide film can be formed by a sputtering method using a metal oxide target, for example.

[0294] The metal oxide film is preferably a dense film with as few defects as possible. The metal oxide film is preferably a highly purified film in which impurities such as hydrogen and water are reduced as much as possible. It is particularly preferable to use a metal oxide film having crystallinity as the metal oxide film.

[0295] In forming the metal oxide film, an oxygen gas and an inert gas (such as a helium gas, an argon gas, or a xenon gas) may be mixed. Note that the higher the proportion of the oxygen gas in the whole deposition gas (hereinafter also referred to as oxygen flow rate ratio) is in forming the metal oxide film, the higher the crystallinity of the metal oxide film can be, achieving a highly reliable transistor. By contrast, the lower the oxygen flow rate ratio is, the lower the crystallinity of the metal oxide film is, offering a transistor with increased on-state current.

[0296] In forming the metal oxide film, as the substrate temperature becomes higher, a denser metal oxide film having higher crystallinity can be formed. On the other

hand, as the substrate temperature becomes lower, a metal oxide film having lower crystallinity and higher electrical conductivity can be formed.

[0297] The metal oxide film is preferably formed at a substrate temperature higher than or equal to room temperature and lower than or equal to 250° C., preferably higher than or equal to room temperature and lower than or equal to 200° C., further preferably higher than or equal to room temperature and lower than or equal to 140° C. For example, the substrate temperature is preferably set to be higher than or equal to room temperature and lower than 140° C. because the productivity is increased. When the metal oxide film is formed at a substrate temperature set to room temperature or without intentional heating, the metal oxide film can have low crystallinity.

[0298] In the case of employing an ALD method, a film formation method such as a thermal ALD method or a PEALD method is preferably employed. The thermal ALD method is preferable because of its capability of forming a film with extremely high step coverage. The PEALD method is preferable because of its capability of forming a film at low temperatures, in addition to its capability of forming a film with high step coverage.

[0299] For example, the semiconductor layer 21 including a metal oxide can be formed by an ALD method using a precursor containing a constituent metal element and an oxidizer.

[0300] For example, a film of In—Ga—Zn oxide can be formed using a precursor containing indium, a precursor containing gallium, and a precursor containing zinc. Alternatively, a precursor containing indium and a precursor containing gallium and zinc may be used.

[0301] As the precursor containing indium, it is possible to use triethylindium, trimethylindium, tris(2,2,6,6-tetramethyl-3,5-heptanedionato)indium, cyclopentadienylindium, indium(III) chloride, (3-(dimethylamino)propyl)dimethylindium, or the like.

[0302] As the precursor containing gallium, it is possible to use trimethylgallium, triethylgallium, tris(dimethylamido)gallium(III), gallium(III) acetylacetone, tris(2,2,6,6-tetramethyl-3,5-heptanedionato) gallium, dimethylchlorogallium, diethylchlorogallium, gallium(III) chloride, or the like.

[0303] As the precursor containing zinc, it is possible to use dimethylzinc, diethylzinc, bis(2,2,6,6-tetramethyl-3,5-heptanedionato) zinc, zinc chloride, or the like.

[0304] Ozone, oxygen, water, or the like can be used as the oxidizer.

[0305] As an example of a method for controlling the composition of a film to be formed, adjusting the flow rate ratio, flowing time, flowing order, or the like of the source gases is given. By adjusting such conditions, a film whose composition is gradually changed can be formed. Furthermore, two or more films having different compositions can be formed successively.

[0306] After the metal oxide film is formed, heat treatment is preferably performed. The heat treatment is preferably performed at a temperature higher than or equal to 250° C. and lower than or equal to 650° C., preferably higher than or equal to 400° C. and lower than or equal to 600° C. so that the above-described metal oxide film does not become polycrystals. Note that the heat treatment is performed in a nitrogen gas atmosphere, an inert gas atmosphere, or an atmosphere containing an oxidizing gas at 10 ppm or more, 1% or more, or 10% or more. For example, in the case where

the heat treatment is performed in a mixed atmosphere of a nitrogen gas and an oxygen gas, the proportion of the oxygen gas is preferably approximately 20%. The heat treatment may be performed under reduced pressure. Alternatively, the heat treatment may be performed in such a manner that heat treatment is performed in an atmosphere of a nitrogen gas or an inert gas, and then another heat treatment is performed in an atmosphere containing an oxidizing gas at 10 ppm or more, 1% or more, or 10% or more in order to compensate for released oxygen.

[0307] The gas used in the above heat treatment is preferably highly purified. For example, the amount of moisture contained in the gas used in the above-described heat treatment is preferably 1 ppb (0.001 ppm) or less, preferably 0.1 ppb or less, and further preferably 0.05 ppb or less. The heat treatment using a highly purified gas can, for example, prevent the entry of moisture into the metal oxide film as much as possible.

[0308] Although the semiconductor film 21f is illustrated as a single layer in the drawings, a stacked-layer structure may be employed. For example, a two-layer structure formed by an ALD method, a three-layer structure formed by an ALD method, a two-layer structure in which the first layer is formed by an ALD method and the second-layer is formed by a sputtering method, or a three-layer structure in which the first layer is formed by an ALD method, the second layer is formed by a sputtering method, and the third layer is formed by an ALD method or a sputtering method can be employed. The first layer is preferably formed by an ALD method, which can inhibit mixing; alternatively, the first layer can also be formed by a sputtering method. Note that the semiconductor film 21f may have a stacked-layer structure of four or more layers.

[0309] Then, a resist mask 61 is formed over the semiconductor film 21f (FIG. 14B). In that case, in order to reduce variation in the thickness of the resist mask 61, an organic material or an inorganic material formed by a coating method may be provided between the resist mask 61 and the semiconductor film 21f as a planarization film that fills the slit 20. More specifically, a coating insulating film such as a spin on carbon (SOC) film or a spin on glass (SOG) film can be used, for example.

[0310] Next, part of the semiconductor film 21f that is not covered with the resist mask 61 is removed by etching, and then the resist mask 61 is removed, whereby the semiconductor layer 21 can be formed (FIG. 15A). In the etching of the semiconductor layer 21, it is difficult to remove part of the semiconductor layer 21 in contact with the side surface of the insulating layer 41 only by anisotropic dry etching; thus, the etching is preferably performed by a combination of isotropic dry etching or wet etching. Alternatively, treatment may be performed in advance on a region of the semiconductor film 21f that is not covered with the resist mask 61 so that the quality of part of the semiconductor film 21f is changed to facilitate etching. Examples of the treatment include plasma treatment, doping (including ion implantation) treatment, and wet treatment.

[0311] Next, the insulating layer 22 is formed to cover the semiconductor layer 21 and the insulating layer 41. The insulating layer 22 can be formed by a film formation method such as a sputtering method, an ALD method, or a CVD method. The insulating layer 22 is preferably provided to have as uniform a thickness as possible on the surface of the vertical portion of the semiconductor layer 21. Thus, the

insulating layer 22 is particularly preferably formed by an ALD method, which is a film formation method with extremely excellent coverage. Note that in the case where the insulating layer 41 has a sidewall with a tapered shape, the insulating layer 22 can be formed by a film formation method such as a sputtering method or a CVD method.

[0312] Next, a conductive film 23f to be the conductive layer 23 later is formed to cover the insulating layer 22 (FIG. 15B). The conductive film 23f can be formed by a CVD method, an ALD method, a sputtering method, or the like. In terms of coverage, the conductive film 23f is particularly preferably formed by a CVD method.

[0313] Next, planarization treatment is performed on the conductive film 23f, the insulating layer 22, and the semiconductor layer 21 (FIG. 16A). The planarization treatment is performed until the top surface of the conductive film 25b is exposed. Thus, the semiconductor layer 21, the insulating layer 22, and the conductive layer 23 positioned inside the slit 20 are formed. By planarization treatment, the top surfaces of the conductive film 25b, the conductive layer 23, the insulating layer 22, and the semiconductor layer 21 are substantially level with each other (e.g., at substantially the same height from the substrate surface).

[0314] At this time, the transistor 10 can be formed.

[0315] Next, the insulating layer 43 is formed to cover the conductive film 25b, the semiconductor layer 21, the insulating layer 22, and the conductive layer 23 (FIG. 16B). Then, the insulating layer 44 is formed over the insulating layer 43. The insulating layers 43 and 44 can be formed by a CVD method, an ALD method, a sputtering method, or the like.

[0316] Then, an opening reaching the conductive film 25a is formed in the insulating layer 44, the insulating layer 43, and the conductive film 25b. After that, a conductive film that fills the opening is formed and planarization treatment is performed until the top surface of the insulating layer 44 is exposed, so that the plug 27 can be formed (FIG. 17A).

[0317] Next, a conductive film is formed over the insulating layer 44 and the plug 27, and an unnecessary portion is removed by etching, whereby the conductive layer 26 is formed (FIG. 17B).

[0318] Through the above-described steps, a semiconductor device provided with the memory cell 15 in which the transistor 10 and the capacitor 30 are included can be manufactured.

[0319] The above is the description of the manufacturing method example.

[0320] At least part of this embodiment can be implemented as appropriate in combination with any of the other embodiments described in this specification.

## Embodiment 2

[0321] In this embodiment, a semiconductor device 900 of one embodiment of the present invention, which is different from the above embodiment, will be described. The semiconductor device 900 can function as a memory device.

[0322] FIG. 18 is a block diagram illustrating a structure example of the semiconductor device 900. The semiconductor device 900 illustrated in FIG. 18 includes a driver circuit 910 and a memory array 920. The memory array 920 includes one or more of a memory cell 950. FIG. 18 illustrates an example in which the memory array 920 includes a plurality of memory cells 950 arranged in a matrix.

[0323] The memory cell 15 or the like exemplified in the above embodiment can be used as the memory cell 950.

[0324] The driver circuit 910 includes a power switch (PSW) 931, a PSW 932, and a peripheral circuit 915. The peripheral circuit 915 includes a peripheral circuit 911, a control circuit 912, and a voltage generator circuit 928.

[0325] In the semiconductor device 900, the circuits, signals, and voltages can be appropriately selected as needed. Another circuit or another signal may be added. Signals BW, CE, GW, CLK, WAKE, ADDR, WDA, PON1, and PON2 are signals input from the outside, and a signal RDA is a signal output to the outside. The signal CLK is a clock signal.

[0326] The signals BW, CE, and GW are control signals. The signal CE is a chip enable signal. The signal GW is a global write enable signal. The signal BW is a byte write enable signal. The signal ADDR is an address signal. The signal WDA is a write data signal, and the signal RDA is a read data signal. The signals PON1 and PON2 are power gating control signals. Note that the signals PON1 and PON2 may be generated in the control circuit 912.

[0327] The control circuit 912 is a logic circuit having a function of controlling the overall operation of the semiconductor device 900. For example, the control circuit 912 performs logical operation on the signals CE, GW, and BW to determine the operating mode (e.g., write operation or read operation) of the semiconductor device 900. The control circuit 912 generates a control signal for the peripheral circuit 911 so that the operating mode is executed.

[0328] The voltage generator circuit 928 has a function of generating a negative voltage. The signal WAKE has a function of controlling the input of the signal CLK to the voltage generator circuit 928. For example, when an H-level signal is applied as the signal WAKE, the signal CLK is input to the voltage generator circuit 928, and the voltage generator circuit 928 generates a negative voltage.

[0329] The peripheral circuit 911 is a circuit for writing and reading data to/from the memory cell 950. The peripheral circuit 911 includes a row decoder 941, a column decoder 942, a row driver 923, a column driver 924, an input circuit 925, an output circuit 926, and a sense amplifier 927.

[0330] The row decoder 941 and the column decoder 942 have a function of decoding the signal ADDR. The row decoder 941 is a circuit for specifying a row to be accessed. The column decoder 942 is a circuit for specifying a column to be accessed. The row driver 923 has a function of selecting the row specified by the row decoder 941. The column driver 924 has a function of writing data to the memory cell 950, reading data from the memory cell 950, and retaining the read data, for example.

[0331] The input circuit 925 has a function of retaining the signal WDA. Data retained in the input circuit 925 is output to the column driver 924. Data output from the input circuit 925 is data (Din) written to the memory cell 950. Data (Dout) read from the memory cell 950 by the column driver 924 is output to the output circuit 926. The output circuit 926 has a function of retaining Dout. Moreover, the output circuit 926 has a function of outputting Dout to the outside of the semiconductor device 900. The data output from the output circuit 926 is the signal RDA.

[0332] The PSW 931 has a function of controlling the supply of VDD to the peripheral circuit 915. The PSW 932 has a function of controlling the supply of VHIM to the row driver 923. Here, in the semiconductor device 900, a high

power supply voltage is VDD and a low power supply voltage is GND (ground potential). In addition, VHM is a high power supply voltage used for setting a word line to high level, and is higher than VDD. The on/off state of the PSW 931 is controlled by the signal PON1, and the on/off state of the PSW 932 is controlled by the signal PON2. The number of power domains to which VDD is supplied is one in the peripheral circuit 915 in FIG. 18 but can be more than one. In that case, a power switch is preferably provided for each power domain.

[0333] Structure examples of other memory cells that can be used as the memory cell 950 are described with reference to FIGS. 19A to 19H.

[0334] In the following description, the expression “two components are connected to each other” includes the case where the two components are electrically connected through a circuit element (a transistor, a switch, a diode, a resistor, or the like). The term “electrical connection” means a possibility that a current flows between two components. Note that the case where two components are connected through a switch or a transistor is included as electrical connection because a current can flow when the components are in an on state.

#### [DOSRAM]

[0335] FIG. 19A illustrates a circuit structure example of a memory cell for a DRAM. In this specification and the like, a DRAM using an OS transistor is referred to as a dynamic oxide semiconductor random access memory (DOSRAM). A memory cell 951 includes a transistor M1 and a capacitor CA.

[0336] Note that the transistor M1 may include a front gate (simply referred to as a gate in some cases) and a back gate. Here, the back gate may be connected to a wiring supplied with a constant potential or a signal, and the front gate and the back gate may be connected to each other.

[0337] A first terminal of the transistor M1 is connected to a first terminal of the capacitor CA. A second terminal of the transistor M1 is connected to a wiring BIL. The gate of the transistor M1 is connected to a wiring WOL. A second terminal of the capacitor CA is connected to a wiring CAL.

[0338] The wiring BIL functions as a bit line, and the wiring WOL functions as a word line. The wiring CAL functions as a wiring for applying a predetermined potential to the second terminal of the capacitor CA. At the time of data writing and reading, a low-level potential (referred to as a reference potential in some cases) is preferably applied to the wiring CAL.

[0339] Data writing and data reading are performed in such a manner that a high-level potential is applied to the wiring WOL to turn on the transistor M1 and establish electrical continuity between the wiring BIL and the first terminal of the capacitor CA (make a state where a current can flow therethrough).

[0340] The memory cell that can be used as the memory cell 950 is not limited to the memory cell 951, and the circuit structure can be changed. For example, a structure of a memory cell 952 illustrated in FIG. 19B can be employed. The memory cell 952 is an example including neither the capacitor CA nor the wiring CAL. The first terminal of the transistor M1 is in an electrically floating state.

[0341] In the memory cell 952, a potential written through the transistor M1 is retained in a capacitor (also referred to as parasitic capacitance) between the first terminal and the

gate, which is shown by a dashed line. With such a structure, the structure of the memory cell can be greatly simplified. [0342] Note that an OS transistor is preferably used as the transistor M1. An OS transistor has a characteristic of an extremely low off-state current. The use of an OS transistor as the transistor M1 enables an extremely low leakage current of the transistor M1. That is, with the use of the transistor M1, written data can be retained for a long time, and thus the frequency of refresh operation for the memory cell can be decreased. Alternatively, refresh operation for the memory cell can be omitted. In addition, owing to an extremely low leakage current, multilevel data or analog data can be retained in the memory cells 951 and 952.

#### [NOSRAM]

[0343] FIG. 19C illustrates a circuit structure example of a gain-cell memory cell including two transistors and one capacitor. A memory cell 953 includes a transistor M2, a transistor M3, and a capacitor CB. In this specification and the like, a memory device including a gain-cell memory cell using an OS transistor as the transistor M2 is referred to as a nonvolatile oxide semiconductor RAM (NOSRAM).

[0344] A first terminal of the transistor M2 is connected to a first terminal of the capacitor CB. A second terminal of the transistor M2 is connected to a wiring WBL. A gate of the transistor M2 is connected to the wiring WOL. A second terminal of the capacitor CB is connected to the wiring CAL. A first terminal of the transistor M3 is connected to a wiring RBL. A second terminal of the transistor M3 is connected to a wiring SL. A gate of the transistor M3 is connected to the first terminal of the capacitor CB.

[0345] The wiring WBL functions as a write bit line, the wiring RBL functions as a read bit line, and the wiring WOL functions as a word line. The wiring CAL functions as a wiring for applying a predetermined potential to the second terminal of the capacitor CB. In the time of data writing, data retention, and data reading, a low-level potential (sometimes referred to as a reference potential) is preferably applied to the wiring CAL.

[0346] Data writing is performed in such a manner that a high-level potential is applied to the wiring WOL to turn on the transistor M2 and establish electrical continuity between the wiring WBL and the first terminal of the capacitor CB. Specifically, when the transistor M2 is on, a potential corresponding to data to be stored is applied to the wiring WBL, and the potential is written to the first terminal of the capacitor CB and the gate of the transistor M3. Then, a low-level potential is applied to the wiring WOL to turn off the transistor M2, whereby the potential of the first terminal of the capacitor CB and the potential of the gate of the transistor M3 are retained.

[0347] Data reading is performed by applying a predetermined potential to the wiring SL. A current flowing between the source and the drain of the transistor M3 and the potential of the first terminal of the transistor M3 are determined by the potential of the gate of the transistor M3 and the potential of the second terminal of the transistor M3. Accordingly, by reading a potential of the wiring RBL connected to the first terminal of the transistor M3, a potential retained in the first terminal of the capacitor CB (or the gate of the transistor M3) can be read. That is, data written to the memory cell can be read on the basis of the potential retained in the first terminal of the capacitor CB (or the gate of the transistor M3).

[0348] As another example, one wiring BIL may be provided instead of the wiring WBL and the wiring RBL. A circuit structure example of the memory cell is illustrated in FIG. 19D. In a memory cell 954, one wiring BIL is provided instead of the wiring WBL and the wiring RBL in the memory cell 953, and the second terminal of the transistor M2 and the first terminal of the transistor M3 are electrically connected to the wiring BIL. In other words, one wiring BIL operates as the write bit line and the read bit line in the memory cell 954.

[0349] A memory cell 955 illustrated in FIG. 19E is an example in which the capacitor CB and the wiring CAL in the memory cell 953 are omitted. A memory cell 956 illustrated in FIG. 19F is an example in which the capacitor CB and the wiring CAL in the memory cell 954 are omitted. Such structures enable high integration of memory cells.

[0350] Note that an OS transistor is preferably used as at least the transistor M2. In particular, an OS transistor is preferably used as each of the transistors M2 and M3.

[0351] Since the OS transistor has a characteristic of an extremely low off-state current, written data can be retained for a long time with the use of the transistor M2, and thus the frequency of refresh operation for the memory cell can be decreased. Alternatively, refresh operation for the memory cell can be omitted. In addition, owing to an extremely low leakage current, multilevel data or analog data can be retained in the memory cells 953, 954, 955, and 956.

[0352] The memory cells 953, 954, 955, and 956 each using the OS transistor as the transistor M2 are embodiments of a NOSRAM.

[0353] Note that a Si transistor may be used as the transistor M3. The Si transistor can have high field-effect mobility and can be formed as a p-channel transistor, so that circuit design flexibility can be increased.

[0354] When the OS transistor is used as the transistor M3, the memory cell can be configured with only n-type transistors.

[0355] FIG. 19G illustrates an example of a gain memory cell 957 including three transistors and one capacitor. The memory cell 957 includes transistors M4 to M6 and a capacitor CC.

[0356] A first terminal of the transistor M4 is connected to a first terminal of the capacitor CC. A second terminal of the transistor M4 is connected to the wiring BIL. A gate of the transistor M4 is connected to the wiring WOL. A second terminal of the capacitor CC is connected to a first terminal of the transistor M5 and a wiring GNDL. A second terminal of the transistor M5 is connected to a first terminal of the transistor M6. A gate of the transistor M5 is connected to the first terminal of the capacitor CC. A second terminal of the transistor M6 is electrically connected to the wiring BIL. A gate of the transistor M6 is connected to a wiring RWL.

[0357] The wiring BIL functions as a bit line. The wiring WOL functions as a write word line. The wiring RWL functions as a read word line. The wiring GNDL is a wiring for supplying a low-level potential.

[0358] Data writing is performed in such a manner that a high-level potential is applied to the wiring WOL to turn on the transistor M4 and establish electrical continuity between the wiring BIL and the first terminal of the capacitor CC. Specifically, when the transistor M4 is on, a potential corresponding to data to be stored is applied to the wiring BIL, and the potential is written to the first terminal of the

capacitor CC and the gate of the transistor M5. Then, a low-level potential is applied to the wiring WOL to turn off the transistor M4, whereby the potential of the first terminal of the capacitor CC and the potential of the gate of the transistor M5 are retained.

[0359] Data reading is performed by precharging the wiring BIL with a predetermined potential, and then making the wiring BIL in an electrically floating state and applying a high-level potential to the wiring RWL. Since the wiring RWL has the high-level potential, the transistor M6 is turned on, so that electrical continuity is established between the wiring BIL and the second terminal of the transistor M5. At this time, the potential of the wiring BIL is applied to the second terminal of the transistor M5; the potential of the second terminal of the transistor M5 and the potential of the wiring BIL change depending on the potential retained in the first terminal of the capacitor CC (or the gate of the transistor M5). Here, the potential retained in the first terminal of the capacitor CC (or the gate of the transistor M5) can be read by reading the potential of the wiring BIL. That is, data written to the memory cell can be read on the basis of the potential retained in the first terminal of the capacitor CC (or the gate of the transistor M5).

[0360] Note that an OS transistor is preferably used as at least the transistor M4.

[0361] Note that Si transistors may be used as the transistors M5 and M6. As described above, a Si transistor may have higher field-effect mobility than the OS transistor depending on the crystal state of silicon used in a semiconductor layer, for example.

[0362] When OS transistors are used as the transistors M5 and M6, the memory cell can be configured with only n-type transistors.

#### [OS-SRAM]

[0363] FIG. 19H illustrates an example of a static random access memory (SRAM) using an OS transistor. In this specification and the like, an SRAM using an OS transistor is referred to as an oxide semiconductor SRAM (OS-SRAM). A memory cell 958 illustrated in FIG. 19H is a memory cell of an SRAM capable of backup operation.

[0364] The memory cell 958 includes transistors M7 to M10, transistors MS1 to MS4, a capacitor CD1, and a capacitor CD2. The transistors MS1 and MS2 are p-channel transistors, and the transistors MS3 and MS4 are n-channel transistors.

[0365] A first terminal of the transistor M7 is connected to the wiring BIL. A second terminal of the transistor M7 is connected to a first terminal of the transistor MS1, a first terminal of the transistor MS3, a gate of the transistor MS2, a gate of the transistor MS4, and a first terminal of the transistor M10. A gate of the transistor M7 is connected to the wiring WOL. A first terminal of the transistor M8 is connected to a wiring BILB. A second terminal of the transistor M8 is connected to a first terminal of the transistor MS2, a first terminal of the transistor MS4, a gate of the transistor MS1, a gate of the transistor MS3, and a first terminal of the transistor M9. A gate of the transistor M8 is connected to the wiring WOL.

[0366] A second terminal of the transistor MS1 is connected to a wiring VDL. A second terminal of the transistor MS2 is connected to the wiring VDL. A second terminal of

the transistor MS3 is connected to the wiring GNDL. A second terminal of the transistor MS4 is connected to the wiring GNDL.

[0367] A second terminal of the transistor M9 is connected to a first terminal of the capacitor CD1. A gate of the transistor M9 is connected to a wiring BRL. A second terminal of the transistor M10 is connected to a first terminal of the capacitor CD2. A gate of the transistor M10 is connected to the wiring BRL.

[0368] A second terminal of the capacitor CD1 is connected to the wiring GNDL. A second terminal of the capacitor CD2 is connected to the wiring GNDL.

[0369] The wirings BIL and BILB function as bit lines. The wiring WOL functions as a word line. The wiring BRL controls the on/off states of the transistors M9 and M10.

[0370] The wiring VDL supplies a high-level potential. The wiring GNDL supplies a low-level potential.

[0371] Data writing is performed by applying a high-level potential to the wiring WOL and the wiring BRL. Specifically, when the transistor M10 is on, a potential corresponding to data to be stored is applied to the wiring BIL, and the potential is written to the second terminal side of the transistor M10.

[0372] In the memory cell 958, the transistors MS1 and MS2 form an inverter loop; hence, an inversion signal of a data signal corresponding to the potential is input to the second terminal side of the transistor M8. Since the transistor M8 is on, an inversion signal of the potential that has been applied to the wiring BIL (i.e., the signal that has been input to the wiring BIL) is output to the wiring BILB. Since the transistors M9 and M10 are on, the potential of the second terminal of the transistor M7 is retained in the first terminal of the capacitor CD2, and the potential of the second terminal of the transistor M8 is retained in the first terminal of the capacitor CD1. After that, a low-level potential is applied to the wiring WOL and the wiring BRL to turn off the transistors M7 to M10, whereby the potential of the first terminal of the capacitor CD1 and the potential of the first terminal of the capacitor CD2 are retained.

[0373] Data reading will be described. First, the wiring BIL and the wiring BILB are precharged to a predetermined potential in advance. Next, a high-level potential is applied to the wiring WOL, and a high-level potential is applied to the wiring BRL. At this time, the potential of the first terminal of the capacitor CD1 is refreshed by the inverter loop in the memory cell 958 and output to the wiring BILB. Furthermore, the potential of the first terminal of the capacitor CD2 is refreshed by the inverter loop in the memory cell 958 and output to the wiring BIL. Since the potentials of the wiring BIL and the wiring BILB are changed from the precharged potentials to the potentials of the first terminal of the capacitor CD2 and the first terminal of the capacitor CD1, the potential retained in the memory cell can be read on the basis of the potentials of the wiring BIL and the wiring BILB.

[0374] Note that the transistors M7 to M10 are preferably OS transistors. In this case, with the use of the transistors M7 to M10, written data can be retained for a long time, and thus the frequency of refresh operation for the memory cell can be decreased. Alternatively, refresh operation for the memory cell can be omitted.

[0375] Note that the transistors MS1 to MS4 may be Si transistors.

[0376] The driver circuit 910 and the memory array 920 included in the semiconductor device 900 may be provided on the same plane. Alternatively, as illustrated in FIG. 20A, the driver circuit 910 and the memory array 920 may be provided to overlap each other. Overlapping the driver circuit 910 and the memory array 920 can shorten a signal propagation distance. As illustrated in FIG. 20B, a plurality of memory cell arrays 920 may be stacked over the driver circuit 910.

[0377] Next, description is made on an example of an arithmetic processing device that can include the semiconductor device, such as the memory device described above.

[0378] FIG. 21 is a block diagram of an arithmetic device 960. The arithmetic device 960 illustrated in FIG. 21 can be used for a central processing unit (CPU), for example. The arithmetic device 960 can also be used for a processor including a larger number of (several tens to several hundreds of) processor cores capable of parallel processing than a CPU, such as a graphics processing unit (GPU), a tensor processing unit (TPU), or a neural processing unit (NPU).

[0379] The arithmetic device 960 illustrated in FIG. 21 includes, over a substrate 990, an arithmetic logic unit (ALU) 991, an ALU controller 992, an instruction decoder 993, an interrupt controller 994, a timing controller 995, a register 996, a register controller 997, a bus interface 998, a cache 999, and a cache interface 989. A semiconductor substrate, an SOI substrate, a glass substrate, or the like is used as the substrate 990. The arithmetic device 960 may also include a rewritable ROM and a ROM interface. The cache 999 and the cache interface 989 may be provided in a separate chip.

[0380] The cache 999 is connected via the cache interface 989 to a main memory provided in another chip. The cache interface 989 has a function of supplying part of data retained in the main memory to the cache 999. The cache interface 989 also has a function of outputting part of data retained in the cache 999 to the ALU 991, the register 996, or the like through the bus interface 998.

[0381] As described later, the memory array 920 can be stacked over the arithmetic device 960. The memory array 920 can be used as a cache. Here, the cache interface 989 may have a function of supplying data retained in the memory array 920 to the cache 999. Moreover, in this case, the driver circuit 910 is preferably included in part of the cache interface 989.

[0382] Note that it is also possible that the cache 999 is not provided and only the memory array 920 is used as a cache.

[0383] The arithmetic device 960 illustrated in FIG. 21 is only an example with a simplified structure, and the actual arithmetic device 960 has a variety of structures depending on the application. For example, what is called a multicore structure is preferably employed in which a plurality of cores each including the arithmetic device 960 in FIG. 21 operate in parallel. The larger number of cores can further enhance the arithmetic performance. The number of cores is preferably larger; for example, the number is preferably 2, further preferably 4, still further preferably 8, still further preferably 12, yet still further preferably 16 or larger. For application requiring extremely high arithmetic performance, e.g., a server, it is preferable to employ the multicore structure including 16 or more, preferably 32 or more, further preferably 64 or more cores. The number of bits that

the arithmetic device 960 can handle with an internal arithmetic circuit, a data bus, or the like can be 8, 16, 32, or 64, for example.

[0384] An instruction input to the arithmetic device 960 through the bus interface 998 is input to the instruction decoder 993 and decoded, and then input to the ALU controller 992, the interrupt controller 994, the register controller 997, and the timing controller 995.

[0385] The ALU controller 992, the interrupt controller 994, the register controller 997, and the timing controller 995 conduct various controls in accordance with the decoded instruction. Specifically, the ALU controller 992 generates signals for controlling the operation of the ALU 991. The interrupt controller 994 judges and processes an interrupt request from an external input/output device, a peripheral circuit, or the like on the basis of its priority, a mask state, or the like while the arithmetic device 960 is executing a program. The register controller 997 generates the address of the register 996, and reads/writes data from/to the register 996 in accordance with the state of the arithmetic device 960.

[0386] The timing controller 995 generates signals for controlling operation timings of the ALU 991, the ALU controller 992, the instruction decoder 993, the interrupt controller 994, and the register controller 997. For example, the timing controller 995 includes an internal clock generator for generating an internal clock signal on the basis of a reference clock signal, and supplies the internal clock signal to the above circuits.

[0387] In the arithmetic device 960 in FIG. 21, the register controller 997 selects operation of retaining data in the register 996 in accordance with an instruction from the ALU 991. That is, the register controller 997 selects whether data is retained by a flip-flop or by a capacitor in a memory cell included in the register 996. When data retention by the flip-flop is selected, a power supply voltage is supplied to the memory cell in the register 996. When data retention by the capacitor is selected, the data is rewritten into the capacitor, and supply of the power supply voltage to the memory cell in the register 996 can be stopped.

[0388] The memory array 920 and the arithmetic device 960 can be provided to overlap with each other. FIGS. 22A and 22B are perspective views of a semiconductor device 970A. The semiconductor device 970A includes a layer 930 provided with memory arrays over the arithmetic device 960. A memory array 920L1, a memory array 920L2, and a memory array 920L3 are provided in the layer 930. The arithmetic device 960 and each of the memory arrays overlap with each other. For easy understanding of the structure of the semiconductor device 970A, the arithmetic device 960 and the layer 930 are separately illustrated in FIG. 22B.

[0389] Overlapping the arithmetic device 960 and the layer 930 including the memory arrays can shorten the connection distance therebetween. Accordingly, the communication speed therebetween can be increased. Moreover, a short connection distance leads to lower power consumption.

[0390] As a method for stacking the layer 930 including the memory arrays and the arithmetic device 960, either of the following methods may be employed: a method in which the layer 930 including the memory arrays is stacked directly on the arithmetic device 960, which is also referred to as monolithic stacking, and a method in which the

arithmetic device 960 and the layer 930 are formed over two different substrates, the substrates are bonded to each other, and the arithmetic device 960 and the layer 930 are electrically connected to each other with a through via or by a technique for bonding conductive films (e.g., Cu—Cu bonding). The former method does not require consideration of misalignment in bonding; thus, not only the chip size but also the manufacturing cost can be reduced.

[0391] Here, it is possible that the arithmetic device 960 does not include the cache 999 and the memory arrays 920L1, 920L2, and 920L3 provided in the layer 930 are each used as a cache. In this case, for example, the memory array 920L1, the memory array 920L2, and the memory array 920L3 can be used as an L1 cache (also referred to as a level 1 cache), an L2 cache (also referred to as a level 2 cache), and an L3 cache (also referred to as a level 3 cache), respectively. Among the three memory arrays, the memory array 920L3 has the highest capacity and the lowest access frequency. The memory array 920L1 has the lowest capacity and the highest access frequency. Note that in the case where the cache 999 provided in the arithmetic device 960 is used as the L1 cache, the memory arrays provided in the layer 930 can each be used as the lower-level cache or the main memory. The main memory has higher capacity and lower access frequency than the cache.

[0392] As illustrated in FIG. 22B, a driver circuit 910L1, a driver circuit 910L2, and a driver circuit 910L3 are provided. The driver circuit 910L1 is connected to the memory array 920L1 through a connection electrode 940L1. Similarly, the driver circuit 910L2 is connected to the memory array 920L2 through a connection electrode 940L2, and the driver circuit 910L3 is connected to the memory array 920L3 through a connection electrode 940L3.

[0393] Note that although the case where three memory arrays function as caches is described here, the number of memory arrays can be one, two, or four or more.

[0394] In the case where the memory array 920L1 is used as a cache, the driver circuit 910L1 may function as part of the cache interface 989 or the driver circuit 910L1 may be connected to the cache interface 989. Similarly, each of the driver circuits 910L2 and 910L3 may function as part of the cache interface 989 or be connected thereto.

[0395] Whether the memory array 920 functions as the cache or the main memory is determined by the control circuit 912 included in each of the driver circuits 910. The control circuit 912 can make some of the memory cells 950 in the semiconductor device 900 function as RAM in accordance with a signal supplied from the arithmetic device 960.

[0396] In the semiconductor device 900, some of the memory cells 950 can function as the cache and the other memory cells 950 can function as the main memory. That is, the semiconductor device 900 can have both the function of the cache and the function of the main memory. The semiconductor device 900 of one embodiment of the present invention can function as a universal memory, for example.

[0397] The layer 930 including one memory array 920 may be provided to overlap with the arithmetic device 960. FIG. 23A is a perspective view of a semiconductor device 970B.

[0398] In the semiconductor device 970B, one memory array 920 can be divided into a plurality of areas having different functions. FIG. 23A illustrates an example in which

a region L1, a region L2, and a region L3 are used as the L1 cache, the L2 cache, and the L3 cache, respectively.

[0399] In the semiconductor device 970B, the capacity of each of the regions L1 to L3 can be changed depending on circumstances. For example, the capacity of the L1 cache can be increased by increasing the area of the region L1. With such a structure, the arithmetic processing efficiency can be improved and the processing speed can be improved.

[0400] Alternatively, a plurality of memory arrays may be stacked. FIG. 23B is a perspective view of a semiconductor device 970C.

[0401] In the semiconductor device 970C, a layer 930L1 including the memory array 920L1, a layer 930L2 including the memory array 920L2 over the layer 930L1, and a layer 930L3 including the memory array 920L3 over the layer 930L2 are stacked. The memory array 920L1 physically closest to the arithmetic device 960 can be used as a high-level cache, and the memory array 920L3 physically farthest from the arithmetic device 960 can be used as a low-level cache or a main memory. Such a structure can increase the capacity of each memory array, leading to higher processing capability.

[0402] At least part of this embodiment can be implemented as appropriate in combination with any of the other embodiments described in this specification.

### Embodiment 3

[0403] In this embodiment, an example of an operation method of the memory device of one embodiment of the present invention is described. The memory cell 15 exemplified in Embodiment 1 can be used as a memory cell described below.

#### [Hysteresis Characteristics of Ferroelectric]

[0404] A ferroelectric has hysteresis characteristics. FIG. 24 is a graph showing an example of hysteresis characteristics of a ferroelectric. The hysteresis characteristics can be measured using a capacitor including a ferroelectric (a ferroelectric capacitor). In FIG. 24, the horizontal axis represents voltage (electric field) applied to the ferroelectric. The voltage is a potential difference between one electrode and the other electrode of the ferroelectric capacitor. Note that the electric field strength can be obtained by dividing the potential difference by the thickness of the ferroelectric.

[0405] In FIG. 24, the vertical axis represents polarization of the ferroelectric. Positive polarization indicates that positive charge in the ferroelectric is biased toward one electrode side of the capacitor and negative charge is biased toward the other electrode side of the capacitor. By contrast, negative polarization indicates that negative charge in the ferroelectric is biased toward one electrode side of the capacitor and positive charge is biased toward the other electrode side of the capacitor.

[0406] Alternatively, the polarization represented by the vertical axis of the graph in FIG. 24 may be regarded as being positive when negative charge is concentrated on the one electrode side of the capacitor and positive charge is concentrated on the other electrode side of the capacitor, and regarded as being negative when positive charge is concentrated on the one electrode side of the capacitor and negative charge is concentrated on the other electrode side of the capacitor.

[0407] As shown in FIG. 24, the hysteresis characteristics of the ferroelectric can be represented by a curve 151 and a curve 152. Voltages at the intersections of the curve 151 and the curve 152 are referred to as saturated polarization voltage +VSP (also referred to as “+VSP”) and saturated polarization voltage -VSP (also referred to as “-VSP”). It can be said that +VSP and -VSP have different polarities.

[0408] A voltage lower than or equal to -VSP is applied to the ferroelectric, and the voltage applied to the ferroelectric is increased, in which case the polarization of the ferroelectric is increased along the curve 151. On the other hand, a voltage higher than or equal to +VSP is applied to the ferroelectric, and then the voltage applied to the ferroelectric is decreased, in which case the polarization of the ferroelectric is decreased along the curve 152. Note that +VSP is sometimes referred to as a “positive saturated polarization voltage” or a “first saturated polarization voltage”. Moreover, -VSP is sometimes referred to as a “negative saturated polarization voltage” or a “second saturated polarization voltage”. The absolute value of the first saturated polarization voltage may be the same as or different from the absolute value of the second saturated polarization voltage.

[0409] Here, the voltage at the time when the polarization of the ferroelectric changes along the curve 151 to reach 0 is referred to as a coercive voltage +Vc. The voltage at the time when the polarization of the ferroelectric changes along the curve 152 to reach 0 is referred to as a coercive voltage -Vc. The value of +Vc and the value of -Vc are each a value between +VSP and -VSP. In some cases, +Vc is referred to as a “positive coercive voltage” or a “first coercive voltage”, and -Vc is referred to as a “negative coercive voltage” or a “second coercive voltage”. The absolute value of the first coercive voltage may be the same as or different from the absolute value of the second coercive voltage.

[0410] The maximum value of polarization when voltage is not applied to the ferroelectric (when voltage is 0 V) is referred to as remanent polarization +Pr or remanent polarization Pr1, and the minimum value thereof is referred to as remanent polarization -Pr or remanent polarization Pr2. The absolute value of the difference between the remanent polarization +Pr and the remanent polarization -Pr is referred to as remanent polarization 2Pr. A larger remanent polarization 2Pr increases the range of a change in the capacitance value of the ferroelectric capacitor due to polarization reversal. The remanent polarization 2Pr is preferably as large as possible.

#### [Relation Between Polarization of Ferroelectric and Id-Vg Characteristics]

[0411] Next, a structure in which a gate of a transistor is provided with a capacitor including a ferroelectric is described. The relation between the polarization of the ferroelectric included in a capacitor 120 and the Id-Vg characteristics of a transistor 110 is described below.

[0412] FIGS. 25A and 25B are equivalent circuit diagrams of a semiconductor device 100 including the transistor 110 and the capacitor 120 that is a ferroelectric capacitor. The capacitor 120 includes an electrode 163 serving as a gate of the transistor 110, an electrode 168 connected to the wiring WL, and an insulating layer 167 therebetween. The transistor 110 includes the electrode 163, an electrode 160 connected to the wiring BL, and an electrode 155 connected to the wiring SL. The electrode 160 functions as one of a source electrode and a drain electrode, and the electrode 155

serves as the other of the source electrode and the drain electrode. The insulating layer 167 functions as a ferroelectric layer. FIGS. 25A and 25B schematically illustrate the polarization of the insulating layer 167. The electrode 163 can also be referred to as a node FN.

[0413] Note that although the structure in which the capacitor 120 that is a ferroelectric capacitor is connected to the gate of the transistor 110 is described below, the operation principle and the operation method described below can be applied to the structure in which a ferroelectric is used as the gate insulating layer of the transistor, as described in Embodiment 1. FIGS. 25C and 25D illustrate the semiconductor device 100 including a transistor 110a in which a ferroelectric is used for a gate insulating layer.

[0414] FIG. 25E is a diagram showing the Id-Vg characteristics of the transistor 110 at the time when the voltage between the source and the drain (also referred to as a “drain voltage” or “Vd”) is constant. In FIG. 25E, the horizontal axis represents a voltage between the source and the gate (also referred to as a “gate voltage” or “Vg”), and the vertical axis represents a current flowing between the source and the drain (also referred to as a “drain current” or “Id”).

[0415] In FIG. 25E, characteristics 290 show Id-Vg characteristics of the transistor 110 at the time when polarization is not caused in the insulating layer 167 included in the capacitor 120.

[0416] In FIG. 25E, characteristics 291 show Id-Vg characteristics at the time when the polarization of the insulating layer 167 is the remanent polarization Pr1. FIG. 25A schematically illustrates the polarization of the insulating layer 167 included in the capacitor 120 when the transistor 110 has the characteristics 291.

[0417] Since the remanent polarization Pr1 is positive polarization, a positive voltage is generated at the node FN. Thus, the Id-Vg characteristics of the characteristics 290 shift in the negative direction of Vg to be the characteristics 291. In other words, the threshold voltage of the transistor 110 shifts in the negative direction of Vg.

[0418] In FIG. 25E, characteristics 292 show Id-Vg characteristics at the time when the polarization of the insulating layer 167 is the remanent polarization Pr2. FIG. 25B schematically illustrates the polarization of the insulating layer 167 included in the capacitor 120 when the transistor 110 has the characteristics 292.

[0419] Since the remanent polarization Pr2 is negative polarization, a negative voltage is generated at the node FN. Thus, Id-Vg characteristics of the characteristics 290 shift in the positive direction of Vg to be the characteristics 292. In other words, the threshold voltage of the transistor 110 shifts in the positive direction of Vg.

[0420] As illustrated in FIGS. 25A to 25D, the Id-Vg characteristics of the transistor 110 and the transistor 110a can be changed in accordance with the polarization of the insulating layer 167, which is a ferroelectric layer. In other words, by controlling the polarization of the insulating layer 167, the threshold voltages of the transistor 110 and the transistor 110a can be controlled. Thus, the semiconductor device 100 including the transistor 110 and the capacitor 120 and the semiconductor device 100 including the transistor 110a can each function as a memory cell that can retain binary data.

[0421] For example, when binary data of data “0” or “1” is written to the semiconductor device 100 functioning as a memory cell, the polarization of the insulating layer 167 is

changed to the remanent polarization Pr1 to write the data “1”, and the polarization of the insulating layer 167 is changed to the remanent polarization Pr2 to write the data “0”. The Id-Vg characteristics of the semiconductor device 100 to which the data “1” has been written become the characteristics 291. Furthermore, the Id-Vg characteristics of the semiconductor device 100 to which the data “0” has been written become the characteristics 292.

[0422] Next, erasing, writing, retaining, and reading operations of the semiconductor device 100 will be described.

#### <Erasing Operation>

[0423] Before data is written to the semiconductor device 100 functioning as a memory cell, data needs to be erased. In this embodiment, operation of writing data “0” to the semiconductor device 100 is performed as erasing operation. That is, the polarization of the insulating layer 167 is changed to the remanent polarization Pr2.

[0424] FIG. 26A is a timing chart for explaining the erasing operation. FIG. 26B is a circuit diagram illustrating a state of the semiconductor device 100 in Period T11. Note that in a circuit diagram and the like, for easy understanding of a potential of a wiring or the like, a symbol showing the potential of the wiring is sometimes illustrated adjacent to the wiring or the like. Furthermore, an enclosed character is sometimes written near a wiring or the like whose potential has changed.

[0425] In Period T11, a potential L is supplied to the wiring WL, and a potential H is supplied to the wiring BL and the wiring SL.

[0426] Note that a gate capacitance of the transistor 110 and the capacitor 120 are connected in series between the wiring WL and the wiring BL and between the wiring WL and the wiring SL. A voltage applied to the capacitor 120 is determined by the ratio of the gate capacitance of the transistor 110 and the capacitance of the capacitor 120. In this embodiment, the ratio of the gate capacitance of the transistor 110 and the capacitance of the capacitor 120 is 1:1. Accordingly, the potential difference between the potential H and the potential L is set to twice or more the absolute value of VSP. In order to change the polarization of the insulating layer 167 to the remanent polarization Pr2, the potential H is supplied to the wiring BL and the wiring SL, and the potential L is supplied to the wiring WL. The potential H is higher than the potential L.

[0427] For example, in the case where a potential COM is a reference potential (0 V), the potential H is higher than the potential COM and is different from the potential COM by +VSP. Similarly, the potential L is lower than the potential COM and is different from the potential COM by -VSP.

[0428] Under the above conditions, the potential L is supplied to the wiring WL and the potential H is supplied to the wirings BL and SL, whereby -VSP is applied to the capacitor 120. Next, in Period T12, 0V is supplied to the wirings WL, BL, and SL. That is, the wirings WL, BL, and SL are made to have the same potential.

[0429] In Period T12, the polarization of the insulating layer 167 becomes the remanent polarization Pr2 (see FIG. 24). Since the remanent polarization Pr2 is negative polarization as described above, a negative voltage is generated at the node FN. Thus, Id-Vg characteristics of the characteristics 290 shift in the positive direction of Vg to be the

characteristics 292. That is, the threshold voltage of the transistor 110 is shifted in the positive direction of Vg (see FIG. 25E).

[0430] In Period T13, a potential RL is supplied to the wiring WL. The potential RL will be described in detail in the description of the retention operation. Note that the period T12 may be omitted and the period T13 may follow the period T11. A negative voltage is generated at the node FN through Period T11 even when Period T12 is omitted.

#### <Writing Operation>

[0431] Next, operation of writing the data “1” to the semiconductor device 100 functioning as a memory cell will be described. FIG. 27A is a timing chart for describing the operation in the writing operation. FIG. 27B is a circuit diagram illustrating a state of the semiconductor device 100 in Period T21.

[0432] After the erasing operation is performed in Period T11, the potential H is supplied to the wiring WL and the potential L is supplied to the wirings BL and SL in Period T21. Then, +VSP is applied to the capacitor 120, and the polarization of the insulating layer 167 changes along the curve 151 (see FIG. 24). Then, in Period T22, 0 V is supplied to the wirings WL, BL, and SL. That is, the wirings WL, BL, and SL are made to have the same potential.

[0433] In Period T22, the polarization of the insulating layer 167 becomes the remanent polarization Pr1 (see FIG. 24). As described above, since the remanent polarization Pr1 is positive polarization, a positive voltage is generated at the node FN. Thus, Id-Vg characteristics of the characteristics 290 shift in the negative direction of Vg to be the characteristics 291. That is, the threshold voltage of the transistor 110 is shifted in the negative direction of Vg (see FIG. 25E).

[0434] Data “1” can be written to the semiconductor device 100 in such a manner. Since the capacitor 120 is a ferroelectric capacitor, the polarization of the insulating layer 167, which is a ferroelectric, is maintained even when power supply to the semiconductor device 100 stops. Thus, data written to the semiconductor device 100 is maintained even when power supply to the semiconductor device 100 stops. Accordingly, the semiconductor device 100 functions as a nonvolatile memory cell.

[0435] The operation of writing data “0” to the semiconductor device 100 is the same as the above-described erasing operation. Accordingly, there is no need to perform the operation of writing data “0” after the erasing operation.

#### <Retaining Operation>

[0436] After data is written to the semiconductor device 100, the potential RL is supplied to the wiring WL in Period T23. The potential RL is a potential at which the transistor 110 is turned off even when the Id-Vg characteristics of the transistor 110 are the characteristics 291 (see FIG. 25E). Thus, the potential RL is set to a potential lower than the threshold voltage of the characteristics 291. Moreover, in order to hardly cause a change in polarization of the insulating layer 167, the potential RL is set to a voltage with which a voltage applied to the capacitor 120 is higher than or equal to the coercive voltage -Vc.

[0437] After the writing operation, the potential of the wiring WL is preferably the potential RL until the reading operation is performed. When the potential of the wiring WL remains as the potential RL, the transistor 110 is surely

brought into an off state; thus, the power consumption of the semiconductor device **100** is reduced. Moreover, in the case where the semiconductor devices **100** are arranged in a matrix to form a memory cell array, interference in a reading operation of another memory cell (the semiconductor device **100**) can be prevented. Consequently, the memory cell array can have higher reliability.

[0438] Note that the period T22 may be omitted and the period T23 may follow the period T21.

#### <Reading Operation>

[0439] Next, operation of reading data retained in the semiconductor device **100** functioning as a memory cell will be described. FIG. 28A is a timing chart for describing the reading operation. FIG. 28B is a circuit diagram illustrating a state of the semiconductor device **100** in Period T31.

[0440] In this embodiment, the reading operation of the semiconductor device **100** that retains data “1” is described.

[0441] In Period T31, the wiring BL is precharged to the potential H. That is, after the potential of the wiring BL is set to the potential H, the wiring BL is brought into a floating state (a state where electric power is supplied from nowhere). In addition, the potential COM is supplied to the wiring SL.

[0442] Next, in Period T32, a potential RH that is a reading potential is supplied to the wiring WL. The potential RH is a potential higher than or equal to the threshold voltage of the characteristics **291** and lower than the threshold voltage of the characteristics **292**. Moreover, in order to hardly cause a change in polarization of the insulating layer **167**, the potential RH is set to a voltage with which the voltage applied to the capacitor **120** is lower than or equal to the coercive voltage +Vc.

[0443] In the case where the data “1” is retained in the semiconductor device **100**, when the potential RH is supplied to the wiring WL, the transistor **110** is turned on, and a current Id1 flows between the source and the drain (see FIG. 25E). Thus, electrical continuity is established between the wiring BL and the wiring SL, and the potential of the wiring BL that is in a floating state changes toward the potential COM.

[0444] The case where the potential of the wiring BL changes after the potential RH is supplied to the wiring WL can be determined that the data “1” has been written to the semiconductor device **100**. The case where it is judged that the potential of the wiring BL does not change even when the potential RH is supplied to the wiring WL can be determined that the data “0” has been written to the semiconductor device **100**.

[0445] After the reading operation, the potential RL is supplied to the wiring WL in Period T33. Since the potential RH is set to a voltage with which the voltage applied to the capacitor **120** is lower than or equal to the coercive voltage +Vc, the polarization of the insulating layer **167** included in the capacitor **120** is less likely to change. Thus, non-destructive reading of the semiconductor device **100** can be achieved.

[0446] Note that the hysteresis properties of the ferroelectric change depending on the material, the structure, and the manufacturing method. Accordingly, the potential RH is preferably a voltage with which the voltage applied to the capacitor **120** is 0.8 times or less, preferably 0.6 times or less the coercive voltage +Vc. Moreover, the potential RL is preferably a voltage with which the voltage applied to the

capacitor **120** is 0.8 times or more, preferably 0.6 times or more the coercive voltage -Vc.

[0447] The above is the description of the method for operating the memory device.

[0448] At least part of this embodiment can be implemented as appropriate in combination with any of the other embodiments described in this specification.

#### Embodiment 4

[0449] In this embodiment, application examples of the semiconductor device of one embodiment of the present invention are described. The semiconductor device of one embodiment of the present invention can be used for an electronic component, an electronic device, a large computer, space equipment, and a data center (also referred to as DC), for example. An electronic component, an electronic device, a large computer, space equipment, and a data center each employing the semiconductor device of one embodiment of the present invention are effective in improving performance, for example, reducing power consumption.

#### [Electronic Component]

[0450] FIG. 29A is a perspective view of a substrate (a circuit board **704**) provided with an electronic component **700**. The electronic component **700** illustrated in FIG. 29A includes a semiconductor device **710** in a mold **711**. FIG. 29A omits some components to show the inside of the electronic component **700**. The electronic component **700** includes a land **712** outside the mold **711**. The land **712** is electrically connected to an electrode pad **713**, and the electrode pad **713** is electrically connected to the semiconductor device **710** through a wire **714**. The electronic component **700** is mounted on a printed circuit board **702**, for example. A plurality of such electronic components are combined and electrically connected to each other on the printed circuit board **702**, which forms the circuit board **704**.

[0451] The semiconductor device **710** includes a driver circuit layer **715** and a memory layer **716**. The memory layer **716** has a structure where a plurality of memory cell arrays are stacked. A stacked-layer structure of the driver circuit layer **715** and the memory layer **716** can be a monolithic stacked-layer structure. In the monolithic stacked-layer structure, layers can be connected to each other without using a through electrode technique such as a through silicon via (TSV) technique and a bonding technique such as Cu-to-Cu direct bonding. The monolithic stacked-layer structure of the driver circuit layer **715** and the memory layer **716** enables, for example, what is called an on-chip memory structure in which a memory is directly formed on a processor. The on-chip memory structure allows an interface portion between the processor and the memory to operate at high speed.

[0452] With the on-chip memory structure, the sizes of a connection wiring and the like can be smaller than those in the case where the through electrode technique such as TSV is used, which means that the number of connection pins can be increased. The increase in the number of connection pins enables parallel operations, which can improve the bandwidth of the memory (also referred to as a memory bandwidth).

[0453] It is preferable that the plurality of memory cell arrays included in the memory layer **716** be formed with OS transistors and be monolithically stacked. Monolithically

stacking the plurality of memory cell arrays can improve one or both of a memory bandwidth and a memory access latency. Note that the bandwidth refers to the data transfer volume per unit time, and the access latency refers to a period of time from data access to the start of data transmission. Note that in the case where the memory layer 716 is formed with Si transistors, the monolithic stacked-layer structure is difficult to form compared with the case where the memory layer 716 is formed with OS transistors. Therefore, an OS transistor is superior to a Si transistor in the monolithic stacked-layer structure.

**[0454]** The semiconductor device 710 may be called a die. Note that in this specification and the like, a die refers to a chip obtained by, for example, forming a circuit pattern on a disc-like substrate (also referred to as a wafer) or the like and cutting the substrate with the pattern into dices in a process of manufacturing a semiconductor chip. Examples of semiconductor materials that can be used for the die include silicon (Si), silicon carbide (SiC), and gallium nitride (GaN). For example, a die obtained from a silicon substrate (also referred to as a silicon wafer) is referred to as a silicon die in some cases.

**[0455]** FIG. 29B is a perspective view of an electronic component 730. The electronic component 730 is an example of a system in package (SiP) or a multi-chip module (MCM). In the electronic component 730, an interposer 731 is provided over a package substrate 732 (printed circuit board), and a semiconductor device 735 and a plurality of semiconductor devices 710 are provided over the interposer 731.

**[0456]** The electronic component 730 using the semiconductor device 710 as a high bandwidth memory (HBM) is illustrated as an example. The semiconductor device 735 can be used for an integrated circuit such as a central processing unit (CPU), a graphics processing unit (GPU), a neural processing unit (NPU) or an field programmable gate array (FPGA).

**[0457]** As the package substrate 732, a ceramic substrate, a plastic substrate, or a glass epoxy substrate can be used, for example. As the interposer 731, a silicon interposer or a resin interposer can be used, for example.

**[0458]** The interposer 731 includes a plurality of wirings and has a function of electrically connecting a plurality of integrated circuits with different terminal pitches. The plurality of wirings are provided in a single layer or multiple layers. In addition, the interposer 731 has a function of electrically connecting an integrated circuit provided on the interposer 731 to an electrode provided on the package substrate 732. Accordingly, the interposer is referred to as a “redistribution substrate” or an “intermediate substrate” in some cases. Furthermore, a through electrode is provided in the interposer 731 and the through electrode is used to electrically connect an integrated circuit and the package substrate 732 in some cases. Moreover, in the case of using a silicon interposer, a TSV can also be used as the through electrode.

**[0459]** An HBM needs to be connected to many wirings to achieve a wide memory bandwidth. Therefore, an interposer on which an HBM is mounted requires minute and densely formed wirings. For this reason, a silicon interposer is preferably used as the interposer on which an HBM is mounted.

**[0460]** In a SiP, an MCM, or the like using a silicon interposer, a decrease in reliability due to a difference in the coefficient of expansion between an integrated circuit and the interposer is less likely to occur. Furthermore, a surface of a silicon interposer has high planarity; thus, poor connection between the silicon interposer and an integrated circuit provided on the silicon interposer is less likely to occur. It is particularly preferable to use a silicon interposer for a 2.5D package (2.5-dimensional mounting) in which a plurality of integrated circuits are arranged side by side on the interposer.

**[0461]** In the case where a plurality of integrated circuits with different terminal pitches are electrically connected with use of a silicon interposer, a TSV, and the like, a space for a width of the terminal pitch and the like is needed. Accordingly, in the case where the size of the electronic component 730 is reduced, the width of the terminal pitch becomes an issue, which sometimes makes it difficult to provide a large number of wirings for obtaining a wide memory bandwidth. For this reason, the above-described monolithic stacked-layer structure with use of OS transistors is suitable. A composite structure combining memory cell arrays stacked using a TSV and monolithically stacked memory cell arrays may be employed.

**[0462]** In addition, a heat sink (a radiator plate) may be provided to overlap with the electronic component 730. In the case of providing a heat sink, the heights of integrated circuits provided on the interposer 731 are preferably equal to each other. For example, in the electronic component 730 described in this embodiment, the heights of the semiconductor devices 710 and the semiconductor device 735 are preferably equal to each other.

**[0463]** To mount the electronic component 730 on another substrate, an electrode 733 may be provided on a bottom portion of the package substrate 732. FIG. 29B illustrates an example where the electrode 733 is formed of a solder ball. Solder balls are provided in a matrix on the bottom portion of the package substrate 732, so that ball grid array (BGA) mounting can be achieved. Alternatively, the electrode 733 may be formed of a conductive pin. When conductive pins are provided in a matrix on the bottom portion of the package substrate 732, pin grid array (PGA) mounting can be achieved.

**[0464]** The electronic component 730 can be mounted on another substrate by various mounting methods other than BGA and PGA. Examples of a mounting method include staggered pin grid array (SPGA), land grid array (LGA), quad flat package (QFP), quad flat J-leaded package (QFJ), and quad flat non-leaded package (QFN).

[Large Computer]

**[0465]** FIG. 30A is a perspective view of a large computer 5600. In the large computer 5600 illustrated in FIG. 30A, a plurality of rack mount computers 5620 are stored in a rack 5610. Note that the large computer 5600 may be referred to as a supercomputer.

**[0466]** FIG. 30B is a perspective view of an example of the computer 5620. The computer 5620 includes a motherboard 5630. The motherboard 5630 is provided with a plurality of slots 5631 and a plurality of connection terminals. A PC card 5621 is inserted in the slot 5631. In addition, the PC card 5621 includes a connection terminal 5623, a connection terminal 5624, and a connection terminal 5625, each of which is connected to the motherboard 5630.

[0467] FIG. 30C illustrates an example of the PC card 5621. The PC card 5621 is a processing board provided with a CPU, a GPU, a memory device, and the like, for example. The PC card 5621 includes a board 5622 and components mounted on the board 5622, such as the connection terminal 5623, the connection terminal 5624, the connection terminal 5625, an electronic component 5626, an electronic component 5627, an electronic component 5628, and a connection terminal 5629. Note that FIG. 30C illustrates components other than the electronic component 5626, the electronic component 5627, and the electronic component 5628.

[0468] The connection terminal 5629 has a shape with which the connection terminal 5629 can be inserted in the slot 5631 of the motherboard 5630, and the connection terminal 5629 functions as an interface for connecting the PC card 5621 and the motherboard 5630. An example of the standard for the connection terminal 5629 is PCIe.

[0469] The connection terminal 5623, the connection terminal 5624, and the connection terminal 5625 can each serve as, for example, an interface for performing power supply, signal input, or the like to the PC card 5621. For another example, they can each serve as an interface for outputting a signal calculated by the PC card 5621. Examples of the standard for each of the connection terminal 5623, the connection terminal 5624, and the connection terminal 5625 include Universal Serial Bus (USB), Serial ATA (SATA), and Small Computer System Interface (SCSI). In the case where video signals are output from the connection terminal 5623, the connection terminal 5624, and the connection terminal 5625, an example of the standard therefor is HDMI (registered trademark).

[0470] The electronic component 5626 includes a terminal (not illustrated) for inputting and outputting signals, and when the terminal is inserted in a socket (not illustrated) of the board 5622, the electronic component 5626 and the board 5622 can be electrically connected to each other.

[0471] The electronic components 5627 and 5628 include a plurality of terminals; when the terminals are reflow-soldered, for example, to the wirings of the board 5622, the electronic components 5627 and 5628 can be mounted. Examples of the electronic component 5627 include an FPGA, a GPU, and a CPU. As the electronic component 5627, the electronic component 730 can be used, for example. Examples of the electronic component 5628 include a memory device. As the electronic component 5628, the electronic component 700 can be used, for example.

[0472] The large computer 5600 can also function as a parallel computer. When the large computer 5600 is used as a parallel computer, large-scale computation necessary for artificial intelligence learning and inference can be performed, for example.

#### [Space Equipment]

[0473] The semiconductor device of one embodiment of the present invention can be suitably used as space equipment.

[0474] The semiconductor device of one embodiment of the present invention includes an OS transistor. A change in electrical characteristics of the OS transistor due to radiation irradiation is small. That is, the OS transistor is highly resistant to radiation, and thus can be suitably used in an environment where radiation can enter. For example, the OS transistor can be suitably used in outer space. Specifically,

the OS transistor can be used as a transistor in a semiconductor device provided in a space shuttle, an artificial satellite, or a space probe. Examples of radiation include X-rays and a neutron beam. Note that although outer space refers to, for example, space at an altitude greater than or equal to 100 km, outer space described in this specification includes one or more of thermosphere, mesosphere, and stratosphere.

[0475] FIG. 31A illustrates an artificial satellite 6800 as an example of a space equipment. The artificial satellite 6800 includes a body 6801, a solar panel 6802, an antenna 6803, a secondary battery 6805, and a control device 6807. In FIG. 31A, a planet 6804 in outer space is illustrated as an example.

[0476] Although not illustrated in FIG. 31A, a battery management system (also referred to as BMS) or a battery control circuit may be provided in the secondary battery 6805. The battery management system or the battery control circuit preferably uses the OS transistor, in which case low power consumption and high reliability are achieved even in outer space.

[0477] The amount of radiation in outer space is 100 or more times that on the ground. Examples of radiation include electromagnetic waves (electromagnetic radiation) typified by X-rays and gamma rays and particle radiation typified by alpha rays, beta rays, neutron beam, proton beam, heavy-ion beams, and meson beams.

[0478] When the solar panel 6802 is irradiated with sunlight, electric power required for operation of the artificial satellite 6800 is generated. However, for example, in the situation where the solar panel is not irradiated with sunlight or the situation where the amount of sunlight with which the solar panel is irradiated is small, the amount of generated electric power is small. Accordingly, a sufficient amount of electric power required for operation of the artificial satellite 6800 might not be generated. In order to operate the artificial satellite 6800 even with a small amount of generated electric power, the artificial satellite 6800 is preferably provided with the secondary battery 6805. Note that a solar panel is referred to as a solar cell module in some cases.

[0479] The artificial satellite 6800 can generate a signal. The signal is transmitted through the antenna 6803, and can be received by a ground-based receiver or another artificial satellite, for example. When the signal transmitted by the artificial satellite 6800 is received, the position of a receiver that receives the signal can be measured. Thus, the artificial satellite 6800 can construct a satellite positioning system.

[0480] The control device 6807 has a function of controlling the artificial satellite 6800. The control device 6807 is formed with one or more selected from a CPU, a GPU, and a memory device, for example. Note that the semiconductor device including the OS transistor of one embodiment of the present invention is suitably used for the control device 6807. A change in electrical characteristics due to radiation irradiation is smaller in an OS transistor than in a Si transistor. Accordingly, the OS transistor has high reliability and thus can be suitably used even in an environment where radiation can enter.

[0481] The artificial satellite 6800 can include a sensor. For example, with a structure including a visible light sensor, the artificial satellite 6800 can have a function of detecting sunlight reflected by a ground-based object. Alternatively, with a structure including a thermal infrared sensor, the artificial satellite 6800 can have a function of detecting

thermal infrared rays emitted from the surface of the earth. Thus, the artificial satellite **6800** can function as an earth observing satellite, for example.

**[0482]** Although the artificial satellite is described as an example of a device for space in this embodiment, one embodiment of the present invention is not limited to this example. The semiconductor device of one embodiment of the present invention can be suitably used for a device for space such as a spacecraft, a space capsule, or a space probe, for example.

**[0483]** As described above, an OS transistor has excellent effects of achieving a wide memory bandwidth and high radiation tolerance as compared with a Si transistor.

#### [Data Center]

**[0484]** The semiconductor device of one embodiment of the present invention can be suitably used for, for example, a storage system in a data center or the like. Long-term management of data, such as guarantee of data immutability, is required for the data center. The long-term management of data needs setting a storage and a server for retaining a huge amount of data, stable power supply for retaining data, cooling equipment for retaining data, an increase in building size, and the like.

**[0485]** With use of the semiconductor device of one embodiment of the present invention for a storage system in a data center, electric power used for retaining data can be reduced and a semiconductor device for retaining data can be downsized. Accordingly, downsizing of the storage system and the power supply for retaining data, downscaling of the cooling equipment, and the like can be achieved. Therefore, a space of the data center can be reduced.

**[0486]** Since the semiconductor device of one embodiment of the present invention has low power consumption, heat generation from a circuit can be reduced. Accordingly, adverse effects of the heat generation on the circuit itself, the peripheral circuit, and the module can be reduced. Furthermore, the use of the semiconductor device of one embodiment of the present invention can achieve a data center that operates stably even in a high temperature environment. Thus, the reliability of the data center can be increased.

**[0487]** FIG. 31B illustrates a storage system that can be used in a data center. A storage system **6000** illustrated in FIG. 31B includes a plurality of servers **6001sb** as a host **6001** (indicated as "Host Computer" in the diagram). The storage system **6000** includes a plurality of memory devices **6003md** as a storage **6003** (indicated as "Storage" in the diagram). In the illustrated example, the host **6001** and the storage **6003** are connected to each other through a storage area network **6004** (indicated as "SAN" in the diagram) and a storage control circuit **6002** (indicated as "Storage Controller" in the diagram).

**[0488]** The host **6001** corresponds to a computer that accesses data stored in the storage **6003**. The host **6001** may be connected to another host **6001** through a network.

**[0489]** The data access speed, i.e., the time taken for storing and outputting data, of the storage **6003** is shortened by using a flash memory, but is still considerably longer than the data access speed of a DRAM that can be used as a cache memory in a storage. In the storage system, in order to solve the problem of low access speed of the storage **6003**, a cache memory is normally provided in the storage to shorten the time taken for data storage and output.

**[0490]** The above-described cache memory is used in the storage control circuit **6002** and the storage **6003**. The data transmitted between the host **6001** and the storage **6003** is stored in the cache memories in the storage control circuit **6002** and the storage **6003** and then output to the host **6001** or the storage **6003**.

**[0491]** With a structure in which an OS transistor is used as a transistor for storing data in the cache memory to retain a potential based on data, the frequency of refreshing can be decreased, so that power consumption can be reduced. Furthermore, downscaling is possible by stacking memory cell arrays.

**[0492]** The use of the semiconductor device of one embodiment of the present invention for one or more selected from an electronic component, an electronic device, a large computer, space equipment, and a data center will produce an effect of reducing power consumption. While the demand for energy is expected to increase with higher performance or higher integration of semiconductor devices, the emission amount of greenhouse effect gases typified by carbon dioxide ( $\text{CO}_2$ ) can be reduced with use of the semiconductor device of one embodiment of the present invention. Furthermore, the semiconductor device of one embodiment of the present invention has low power consumption and thus is effective as a global warming countermeasure.

**[0493]** At least part of this embodiment can be implemented as appropriate in combination with any of the other embodiments described in this specification.

#### Example

**[0494]** In this example, a slit that can be used for the semiconductor device described in Embodiment 1 was formed and the shape was examined.

**[0495]** First, a method for forming a slit described in this example is described with reference to FIGS. 32A to 32E. Note that portions similar to those described in Embodiment 1 are denoted by the same reference numerals as those described above and are not described in detail in some cases.

**[0496]** First, as illustrated in FIG. 32A, the conductive film **24a**, the conductive film **24b**, the insulating layer **41**, the conductive film **25af**, and the conductive film **25bf** were stacked.

**[0497]** In this example, an approximately 20-nm-thick tungsten film was used as the conductive film **24a** and an approximately 20-nm-thick In—Sn—Si oxide (ITSO) film was used as the conductive film **24b**. The insulating layer **41** was formed using a layered film of an approximately 5-nm-thick silicon nitride film, an approximately 80-nm-thick silicon oxide film, and an approximately 10-nm-thick silicon nitride film. Moreover, an approximately 15-nm-thick tungsten film was used as the conductive film **25af**, and an approximately 10-nm-thick ITSO film was used as the conductive film **25bf**.

**[0498]** Next, an insulating layer **65**, an insulating layer **66**, and a resist mask **67** were formed over the conductive film **25bf**. An SOC film and an SOG film were used as the insulating layer **65** and the insulating layer **66**, respectively.

**[0499]** Next, as illustrated in FIG. 32B, the insulating layer **66** was etched by a dry etching method first. A  $\text{CF}_4$  gas was used as an etching gas. Next, the insulating layer **65** and the resist mask **67** were etched by a dry etching method. A hydrogen gas and a nitrogen gas were used as an etching gas.

[0500] Next, as illustrated in FIG. 32C, the conductive film 25bf was etched by a dry etching method using the insulating layer 66 as a hard mask to form the conductive film 25b. A CH<sub>4</sub> gas and an argon gas were used as an etching gas. After that, an etching residue was washed with a diluted hydrofluoric acid.

[0501] Next, as illustrated in FIG. 32D, the conductive film 25af was etched by a dry etching method using the insulating layer 66 as a hard mask to form the conductive film 25a. A chlorine gas, an oxygen gas, and a CF<sub>4</sub> gas were used as an etching gas.

[0502] Next, as illustrated in FIG. 32E, the insulating layer 41 was etched by a dry etching method to form the slit 20. A CH<sub>2</sub>F<sub>2</sub> gas, a CHF<sub>3</sub> gas, an oxygen gas, a CF<sub>4</sub> gas, and an argon gas were used as an etching gas. This etching was performed under the condition where the insulating layer 66 was also etched at the same time. The remaining insulating layer 65 was removed by ashing treatment using oxygen plasma after the formation of the slit 20.

[0503] After that, an etching residue in the slit was removed using the diluted hydrofluoric acid.

[0504] In the above manner, the slit 20 was formed.

[0505] FIGS. 33A to 33C show scanning electron microscope (SEM) images of the formed slit. FIG. 33A is a SEM image of the case where a slit width (Line) is 40 nm and a distance between slits (Space) is 120 nm as the design values (written as “Line/Space=40 nm/120 nm”). FIG. 33B is a SEM image of the case of “Line/Space=60 nm/180 nm”, and FIG. 33C is a SEM image of the case of “Line/Space=80 nm/240 nm”.

[0506] As described above, it was confirmed that the processing method in this example can form the slit even with an extremely minute width of 40 nm. Furthermore, it was confirmed that the taper angle of the sidewall of the slit (the side surface of the insulating layer 41), which is the angle between the side surface of the insulating layer 41 and the top surface of the conductive layer 24, was greater than or equal to 85° and the sidewall was substantially perpendicular to the substrate surface.

[0507] This application is based on Japanese Patent Application Serial No. 2024-021960 filed with Japan Patent Office on Feb. 16, 2024, the entire contents of which are hereby incorporated by reference.

What is claimed is:

1. A semiconductor device comprising:  
a first conductive layer;  
a second conductive layer;  
a third conductive layer;  
a semiconductor layer;  
a first insulating layer;  
a second insulating layer; and  
a third insulating layer,  
wherein the first insulating layer is positioned over the first conductive layer and comprises a slit reaching the first conductive layer,  
wherein the second conductive layer is positioned over the first insulating layer,  
wherein the semiconductor layer comprises a portion in contact with a side surface of the second conductive layer, a portion in contact with a side surface of the first insulating layer in the slit, and a portion in contact with a top surface of the first conductive layer in the slit,

wherein in the slit, the second insulating layer covers the semiconductor layer,

wherein in the slit, the third conductive layer covers the second insulating layer,

wherein top surfaces of the second conductive layer, the semiconductor layer, the second insulating layer, and the third conductive layer are substantially level with each other, and

wherein the third insulating layer is in contact with the top surfaces of the second conductive layer, the semiconductor layer, the second insulating layer, and the third conductive layer.

2. The semiconductor device according to claim 1, further comprising:

a connection electrode; and  
a fourth conductive layer,  
wherein the slit extends in a first direction,  
wherein the third conductive layer extends in the first direction in the slit,

wherein the fourth conductive layer is positioned over the third insulating layer and extends in a second direction intersecting with the first direction, and

wherein the connection electrode is in contact with the second conductive layer and the fourth conductive layer through an opening portion in the third insulating layer.

3. The semiconductor device according to claim 1,  
wherein the first conductive layer comprises a depressed portion in a region overlapping with the slit, and  
wherein bottom portions of the semiconductor layer, the second insulating layer, and the third conductive layer are provided along the depressed portion.

4. The semiconductor device according to claim 1,  
wherein the semiconductor layer comprises a first metal oxide,  
wherein the first conductive layer comprises a second metal oxide, and

wherein the first metal oxide and the second metal oxide comprise the same element that is one or more selected from In, Sn, Zn, Ga, and Ti.

5. The semiconductor device according to claim 1,  
wherein the semiconductor layer comprises a first metal oxide,  
wherein the first conductive layer comprises a second metal oxide, and

wherein the first metal oxide and the second metal oxide each comprise In.

6. The semiconductor device according to claim 1,  
wherein the semiconductor layer comprises a first metal oxide,  
wherein the second conductive layer comprises a third metal oxide, and

wherein the first metal oxide and the third metal oxide comprise the same element that is one or more selected from In, Sn, Zn, Ga, and Ti.

7. The semiconductor device according to claim 1,  
wherein the semiconductor layer comprises a first metal oxide,  
wherein the second conductive layer comprises a third metal oxide, and  
wherein the first metal oxide and the third metal oxide each comprise In.

8. The semiconductor device according to claim 1, wherein the second insulating layer comprises a film exhibiting an insulating property and a film exhibiting ferroelectricity, and wherein the film exhibiting ferroelectricity comprises hafnium oxide, zirconium oxide, or an oxide comprising hafnium and zirconium.
9. The semiconductor device according to claim 1, further comprising:
  - a fifth conductive layer; and
  - a fourth insulating layer, wherein the fifth conductive layer and the fourth insulating layer are positioned below the first conductive layer, and wherein the fourth insulating layer comprises a portion positioned between the first conductive layer and the fifth conductive layer.
10. The semiconductor device according to claim 9, wherein the fifth conductive layer comprises a depressed portion, wherein the fourth insulating layer comprises a portion provided along the depressed portion, and wherein the first conductive layer comprises a portion positioned inside the depressed portion with the fourth insulating layer therebetween.
11. The semiconductor device according to claim 9, wherein the fourth insulating layer comprises a material exhibiting ferroelectricity.
12. The semiconductor device according to claim 11, wherein the material exhibiting ferroelectricity is one or more of hafnium oxide, zirconium oxide, and an oxide comprising hafnium and zirconium.

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