

(12) **United States Patent**  
Lee et al.

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(54) **DEVICE AND METHOD FOR UBM/RDL ROUTING**

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(Continued)

(71) Applicant: **Taiwan Semiconductor Manufacturing Co., Ltd.**, Hsinchu (TW)

(58) **Field of Classification Search**  
None  
See application file for complete search history.

(72) Inventors: **Meng-Tsan Lee**, Hsinchu (TW);  
**Wei-Cheng Wu**, Hsinchu (TW);  
**Tsung-Shu Lin**, New Taipei (TW)

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(73) Assignee: **Taiwan Semiconductor Manufacturing Company, Ltd.**, Hsin-Chu (TW)

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(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 102 days.

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(22) Filed: **Jan. 20, 2021**

Primary Examiner — Jarrett J Stark

(74) Attorney, Agent, or Firm — Slater Matsil, LLP

(65) **Prior Publication Data**  
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(57) **ABSTRACT**

**Related U.S. Application Data**

(60) Continuation of application No. 16/562,990, filed on Sep. 6, 2019, which is a division of application No. 15/157,312, filed on May 17, 2016.

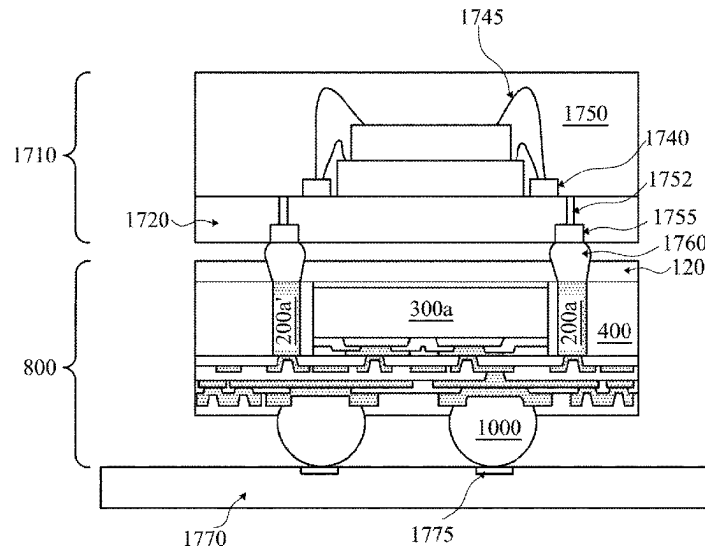
An under bump metallurgy (UBM) and redistribution layer (RDL) routing structure includes an RDL formed over a die. The RDL comprises a first conductive portion and a second conductive portion. The first conductive portion and the second conductive portion are at a same level in the RDL. The first conductive portion of the RDL is separated from the second conductive portion of the RDL by insulating material of the RDL. A UBM layer is formed over the RDL. The UBM layer includes a conductive UBM trace and a conductive UBM pad. The UBM trace electrically couples the first conductive portion of the RDL to the second conductive portion of the RDL. The UBM pad is electrically coupled to the second conductive portion of the RDL. A conductive connector is formed over and electrically coupled to the UBM pad.

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*H01L 25/065* (2023.01)  
*H01L 21/56* (2006.01)  
(Continued)

(52) **U.S. Cl.**  
CPC ..... *H01L 25/0657* (2013.01); *H01L 21/565* (2013.01); *H01L 21/78* (2013.01); *H01L 23/3121* (2013.01); *H01L 23/481* (2013.01);  
*H01L 23/49811* (2013.01); *H01L 23/5389*

**20 Claims, 21 Drawing Sheets**

1700



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						10/2018	Yonezawa	H05K 1/11
						10/2018	Shinohara	H05K 3/323
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						1/2019	Tsukao	H01B 1/22
						2/2019	Won	H01L 27/3276
						5/2019	Nakayama	G06F 3/0443
						8/2019	Tanaka	H05K 3/323
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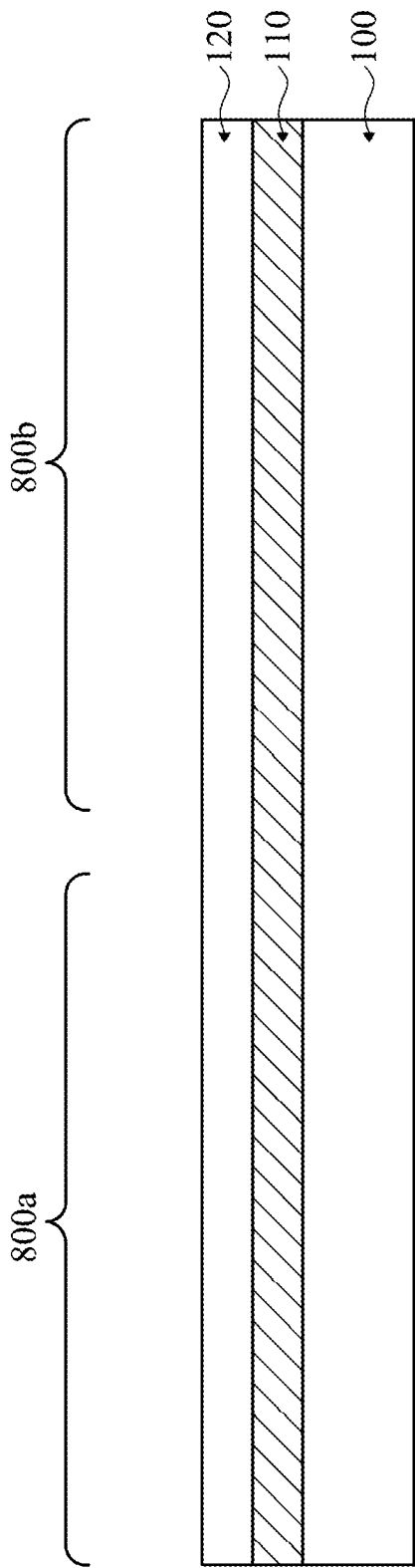


FIG. 1

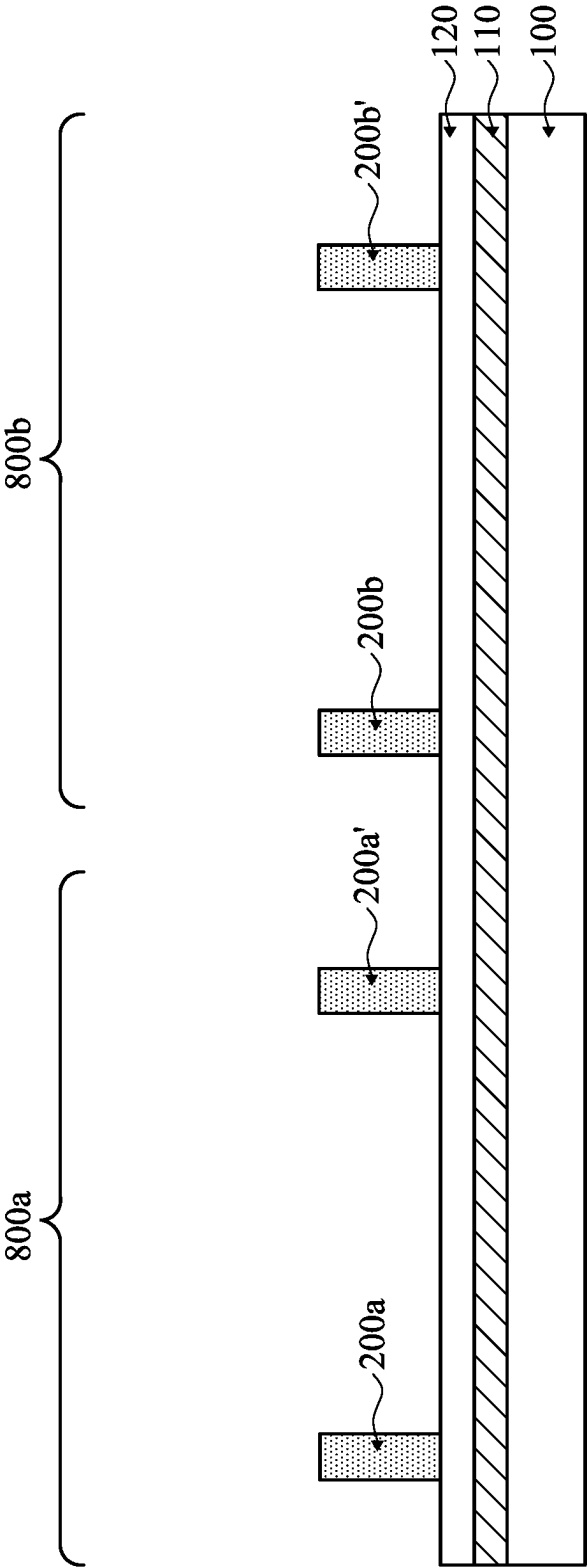


FIG. 2

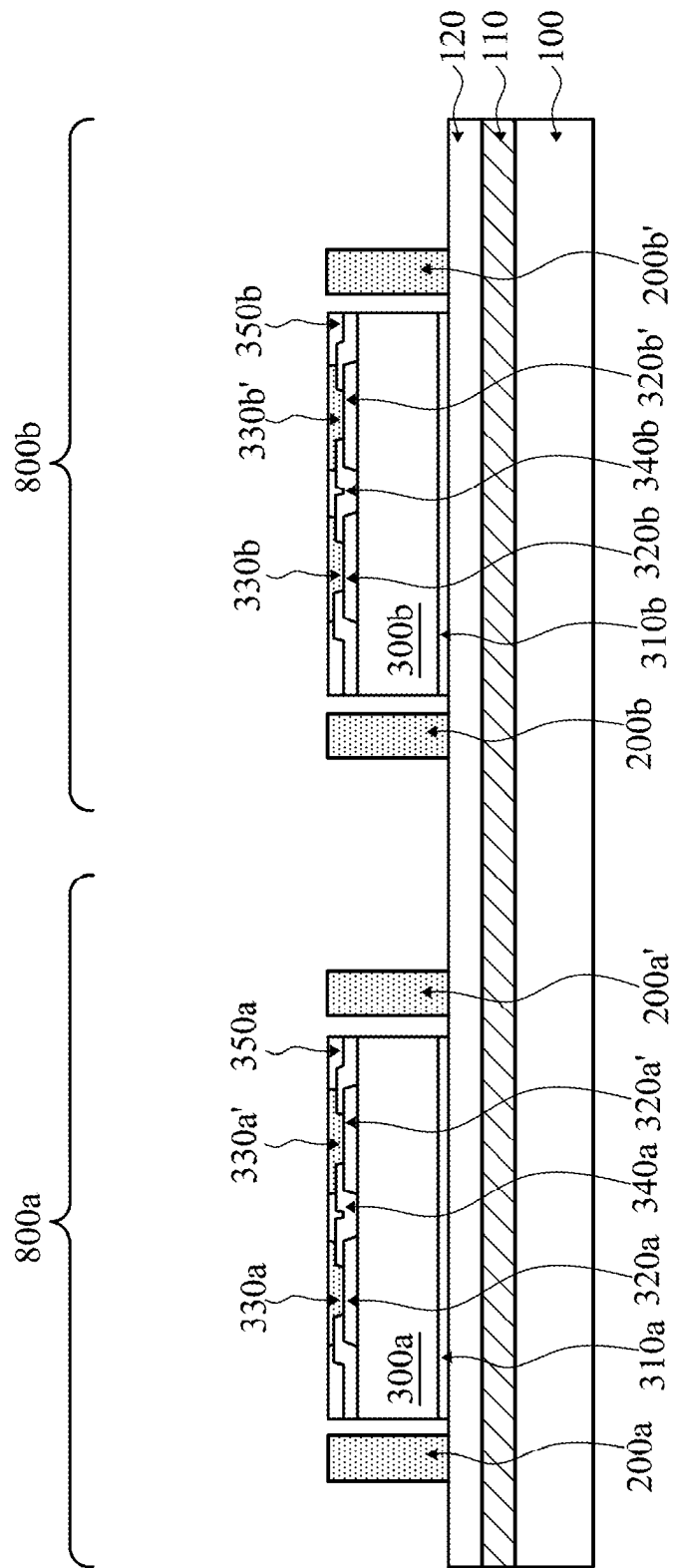


FIG. 3

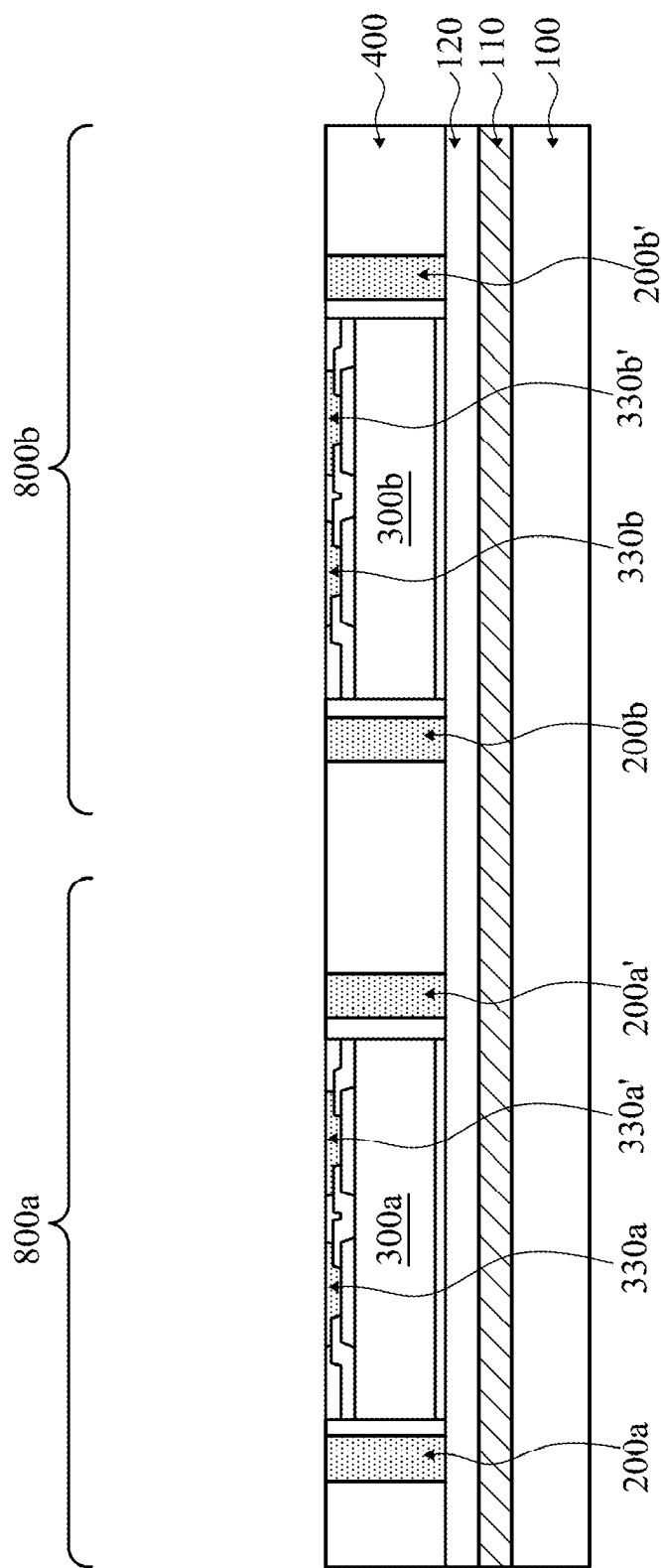


FIG. 4

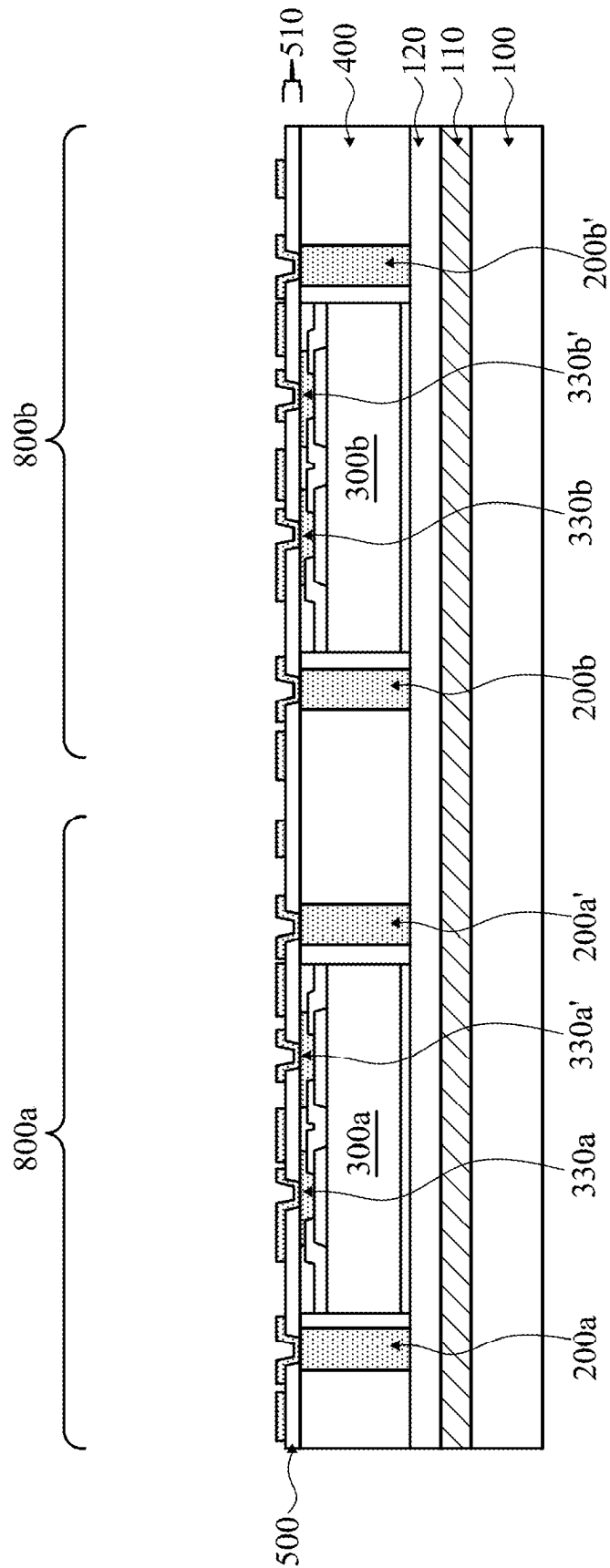


FIG. 5



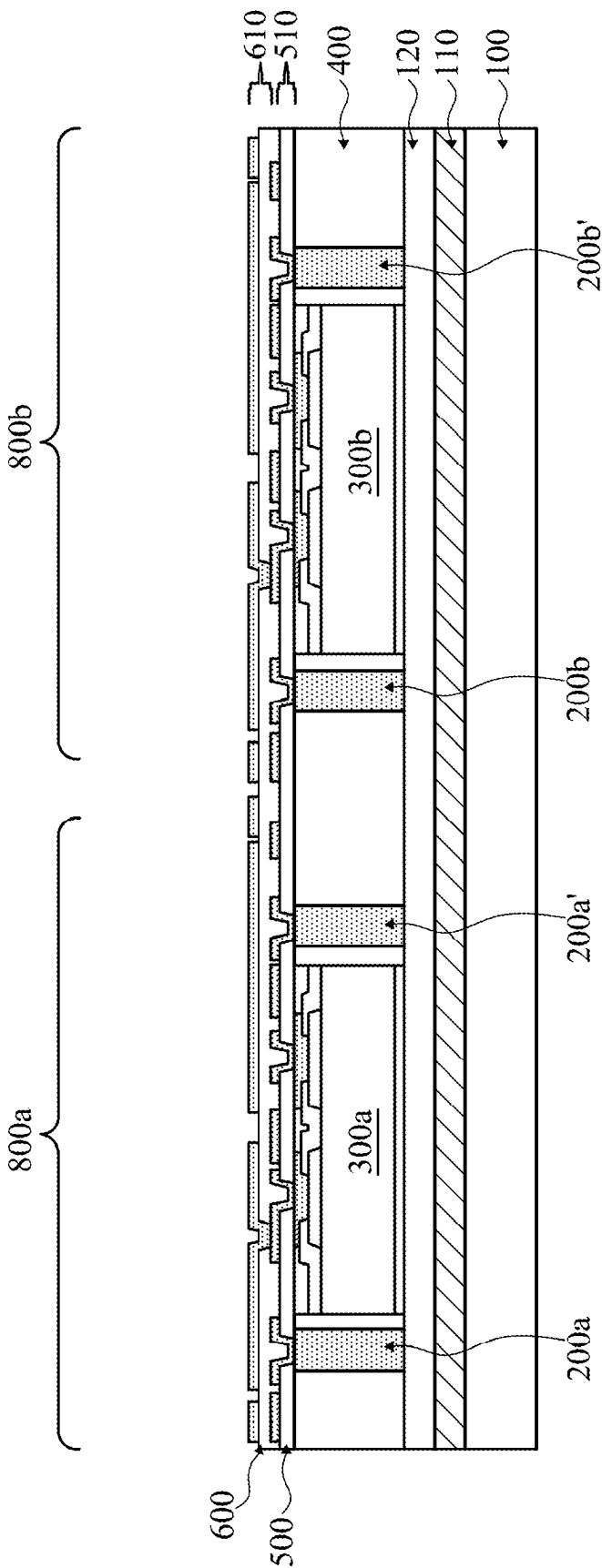


FIG. 6

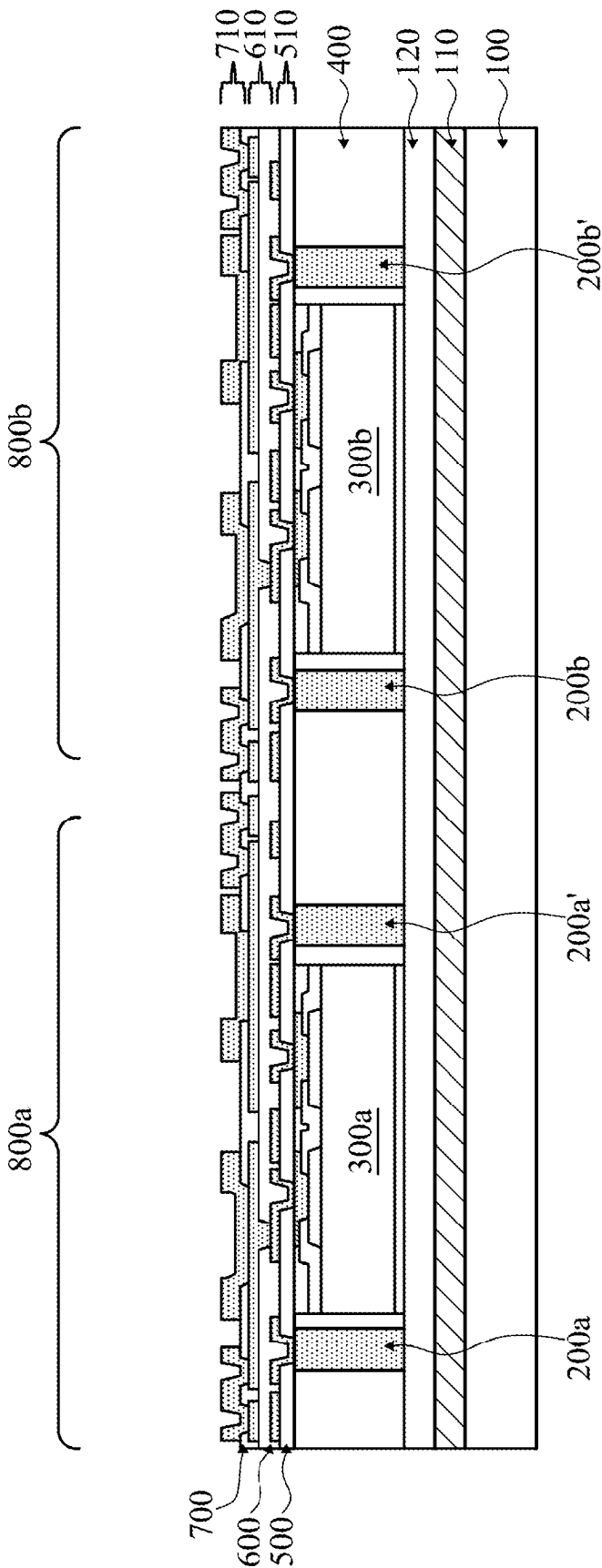


FIG. 7

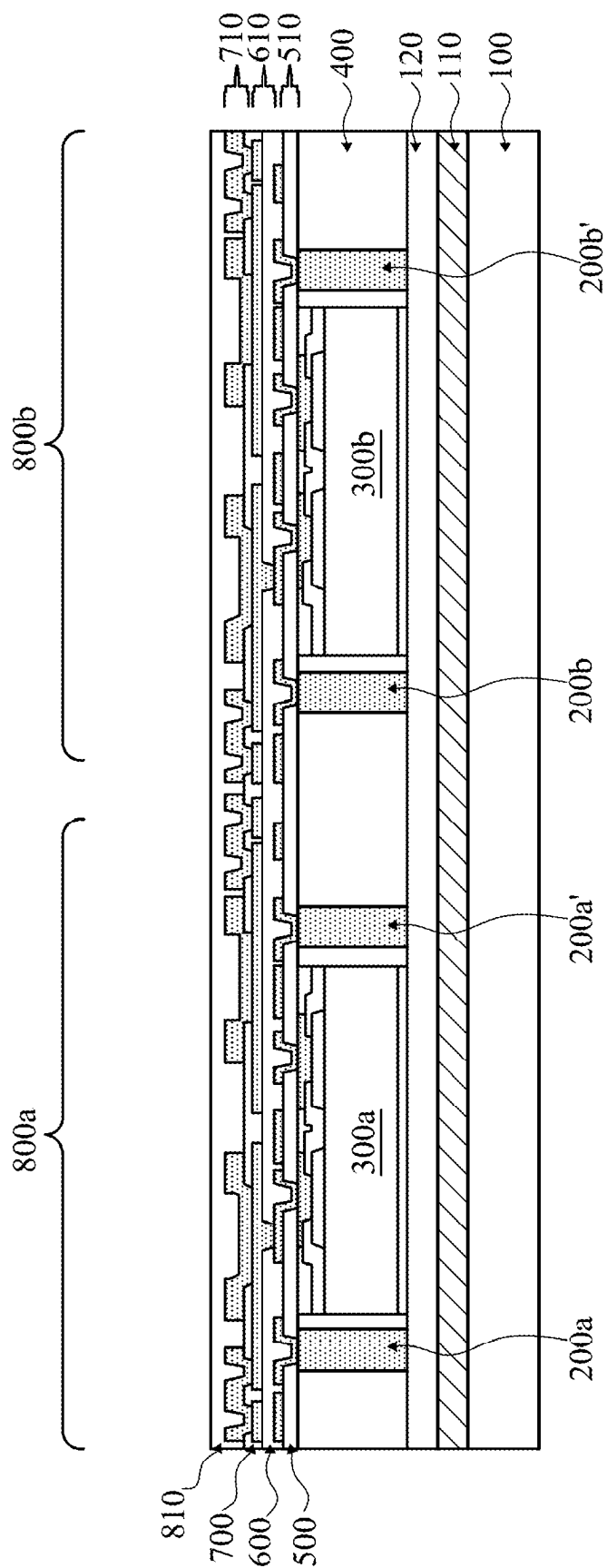


FIG. 8

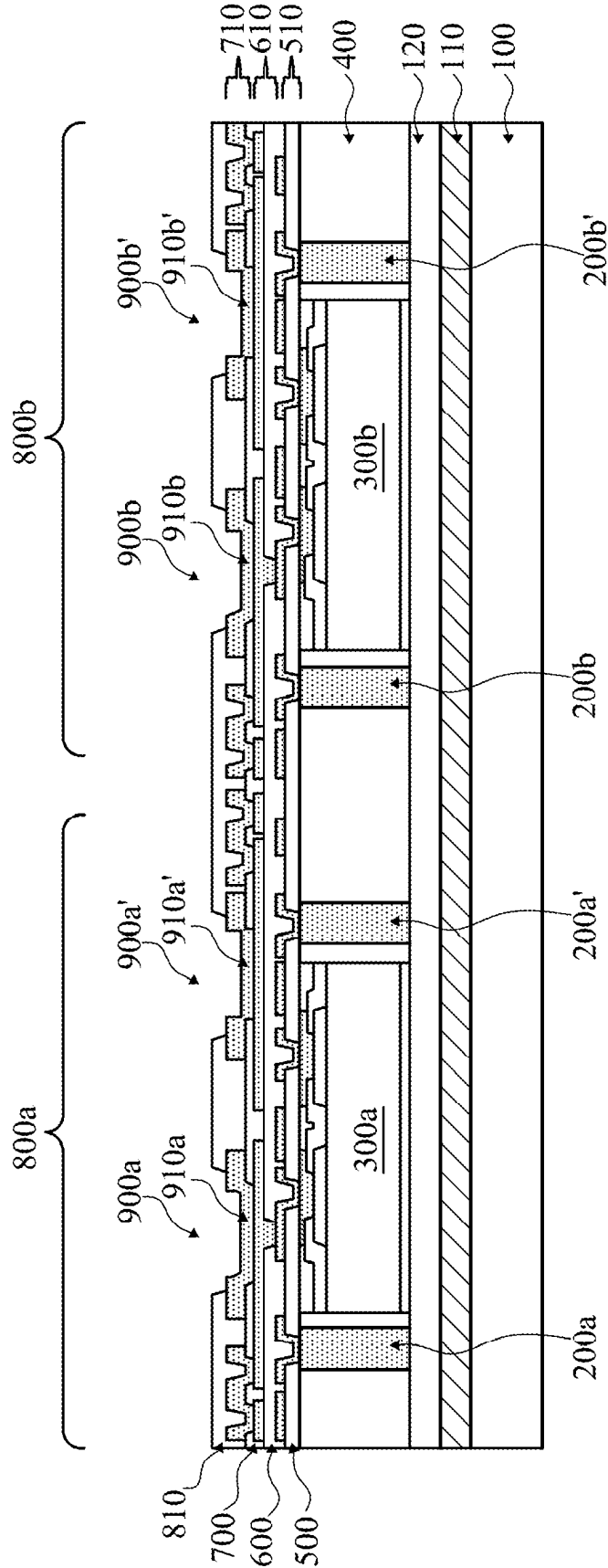


FIG. 9

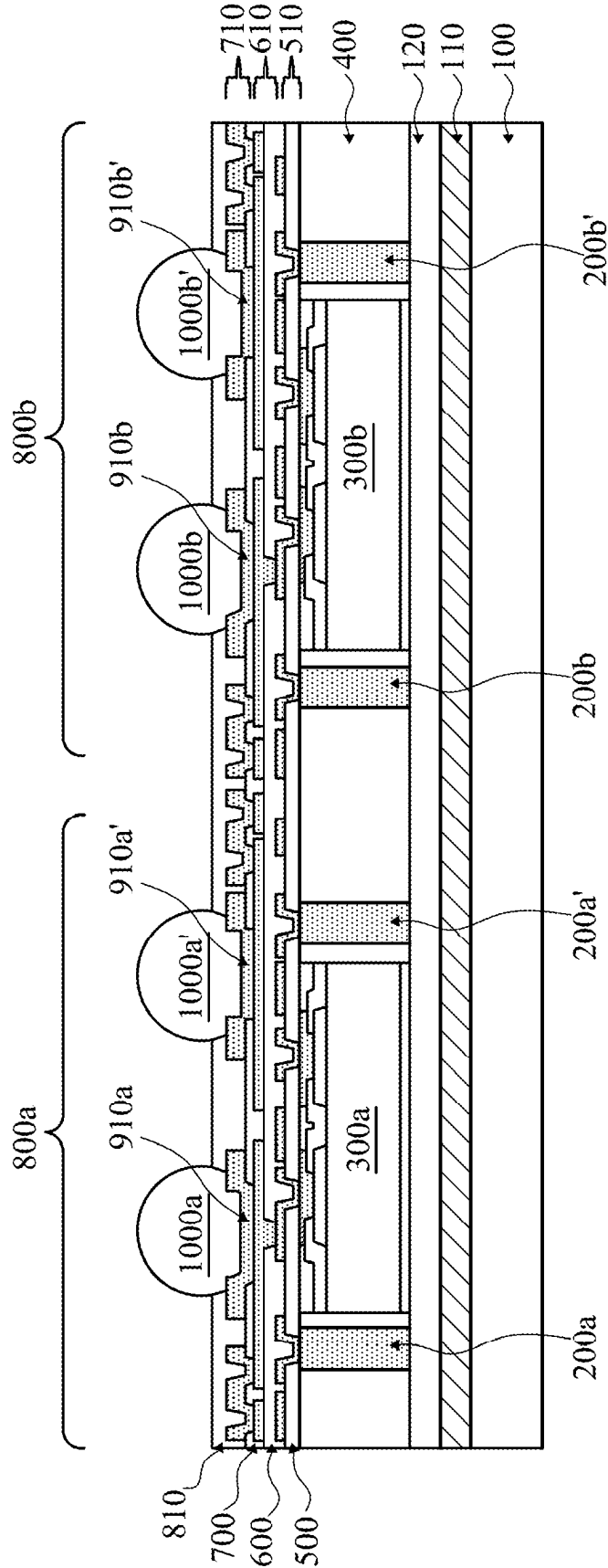


FIG. 10

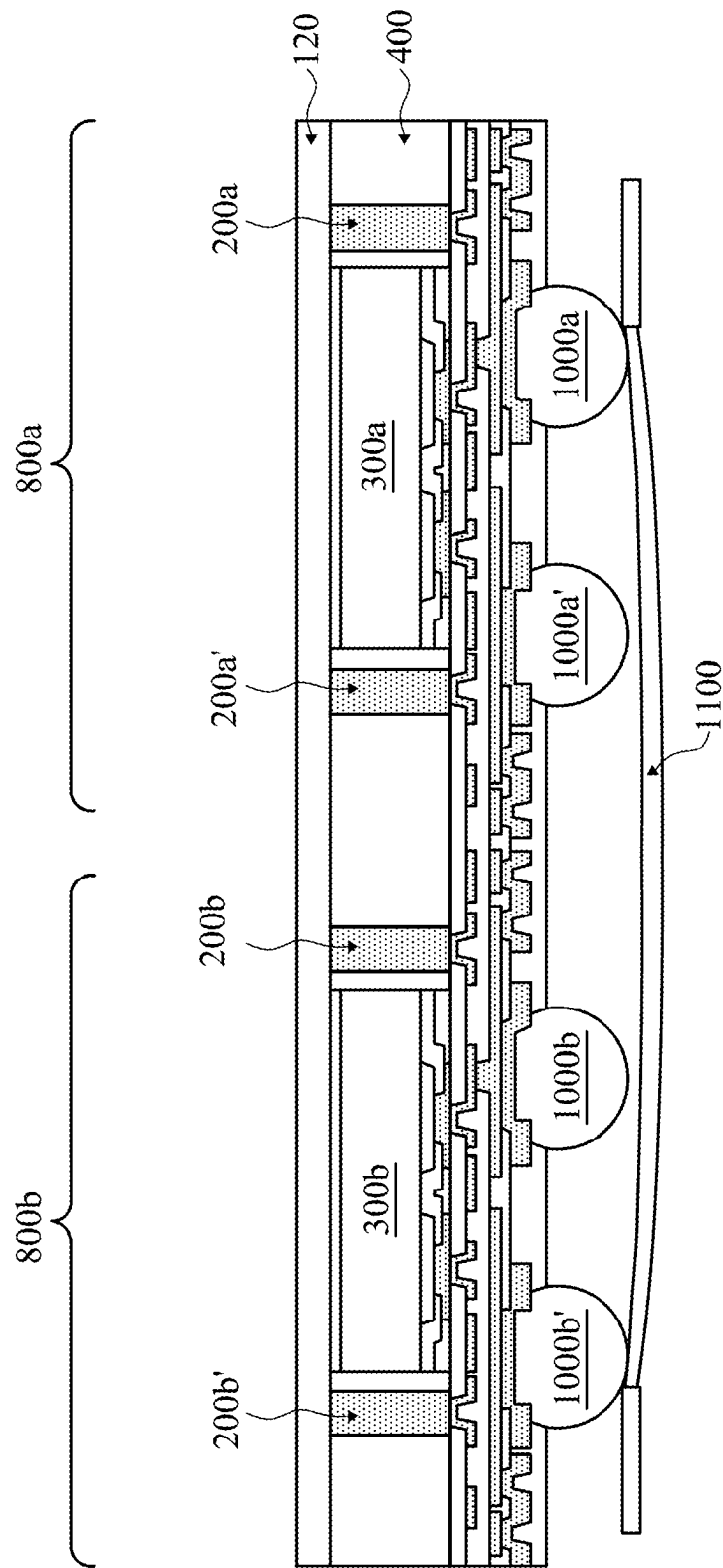


FIG. 11

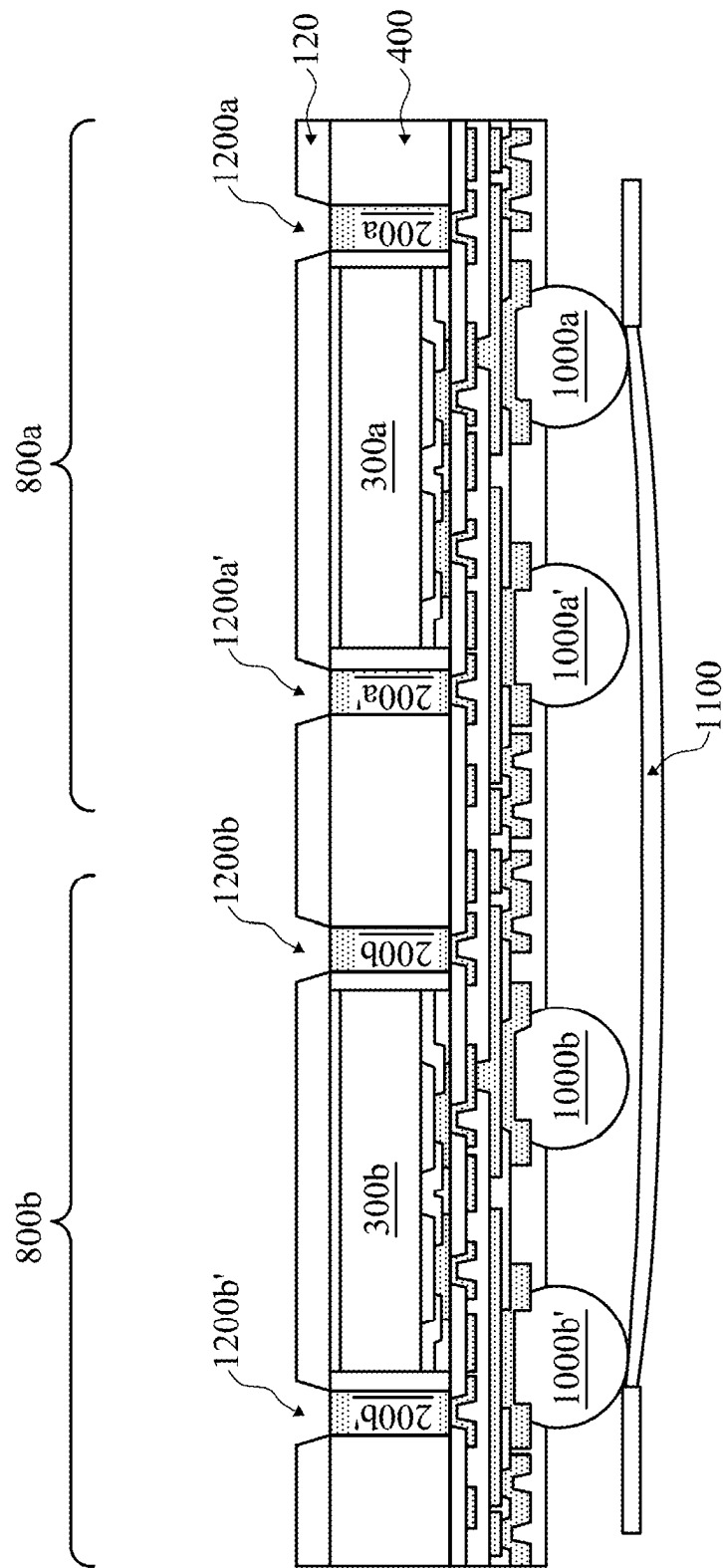


FIG. 12

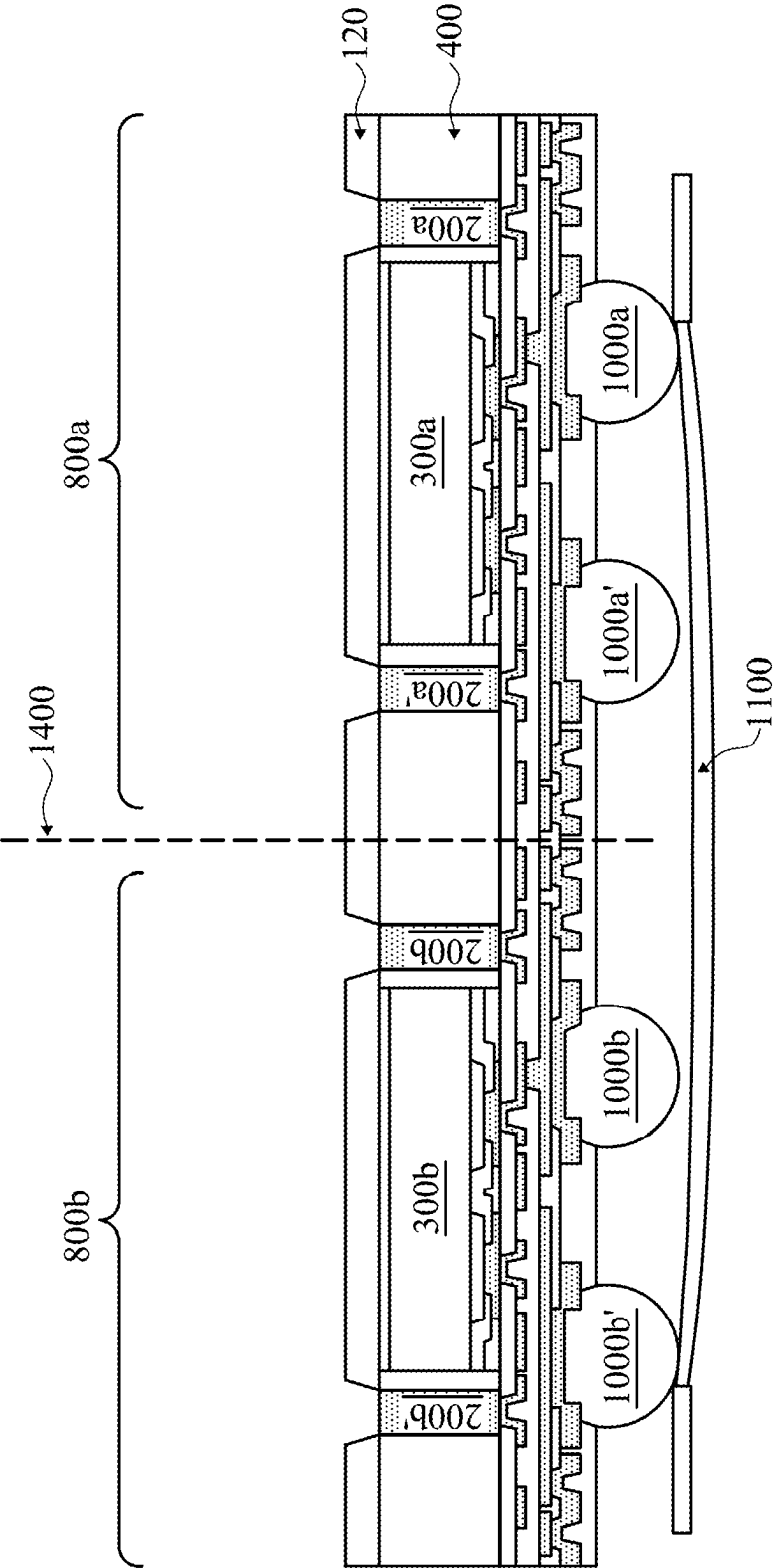


FIG. 13



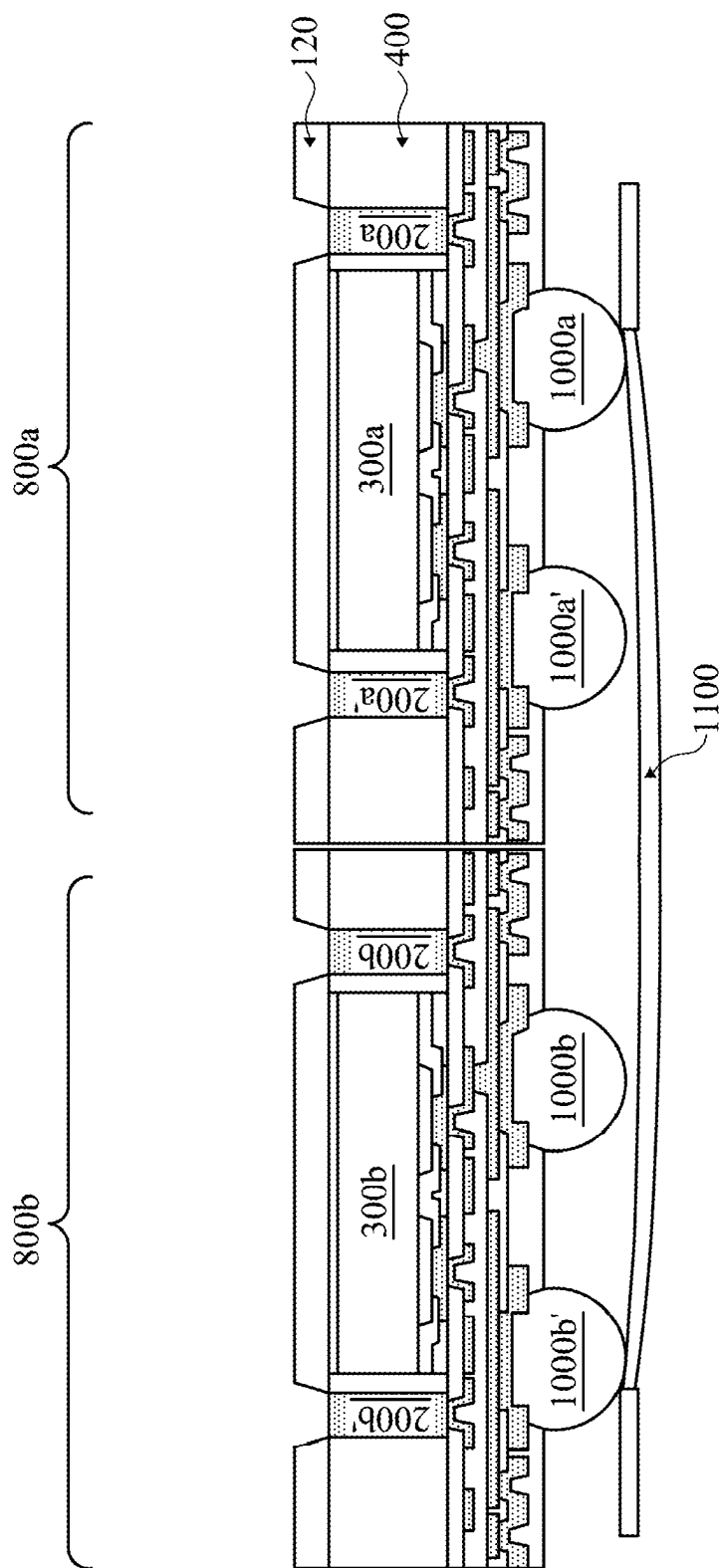


FIG. 14

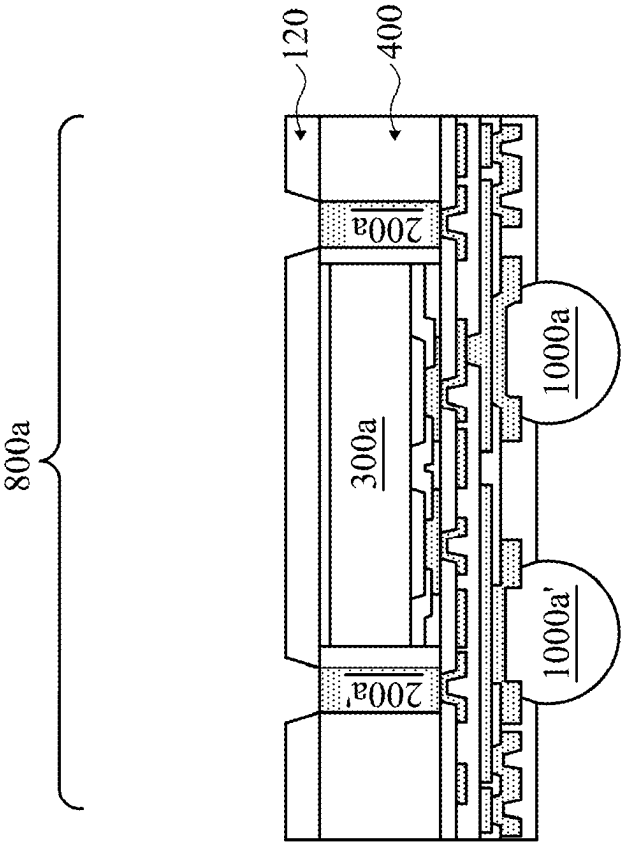


FIG. 15

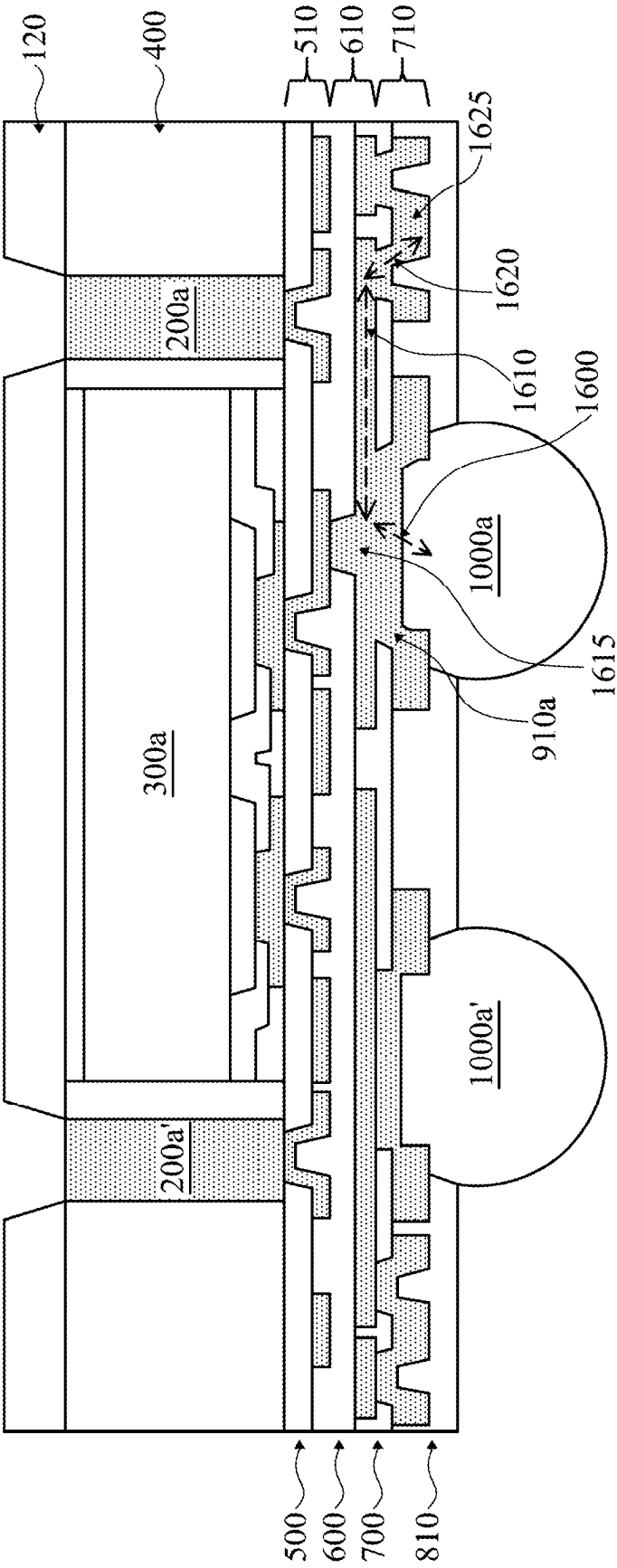


FIG. 16a

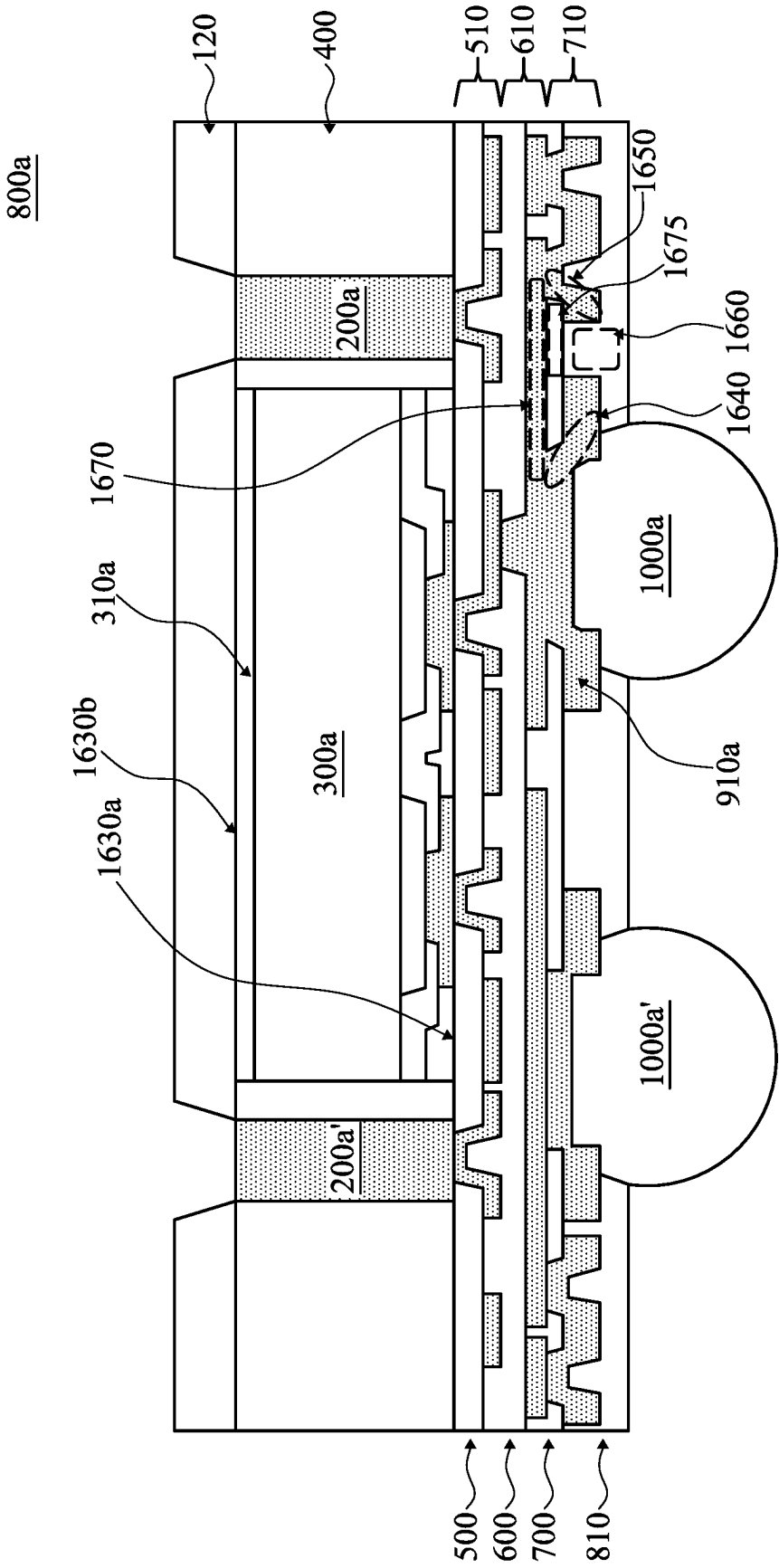


FIG. 16b

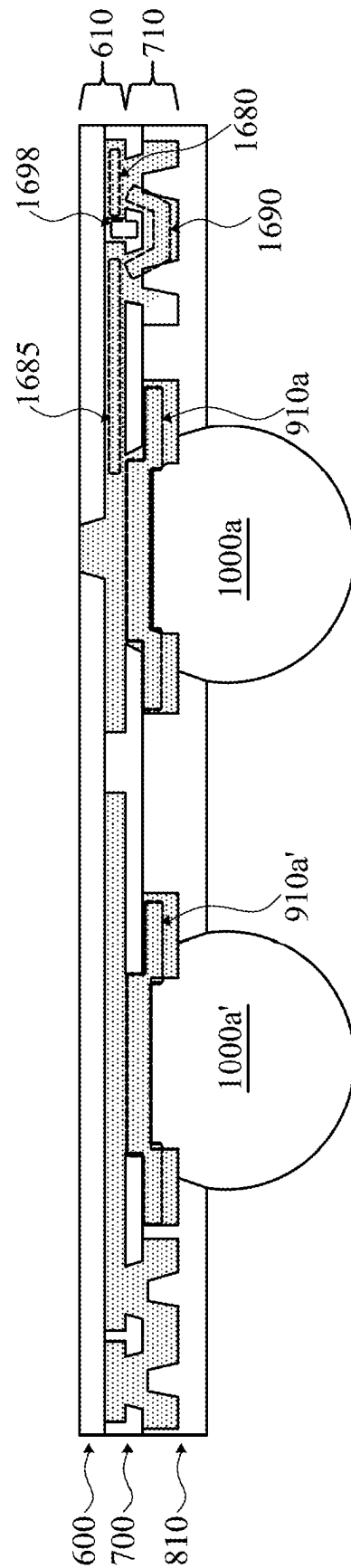


FIG. 16c

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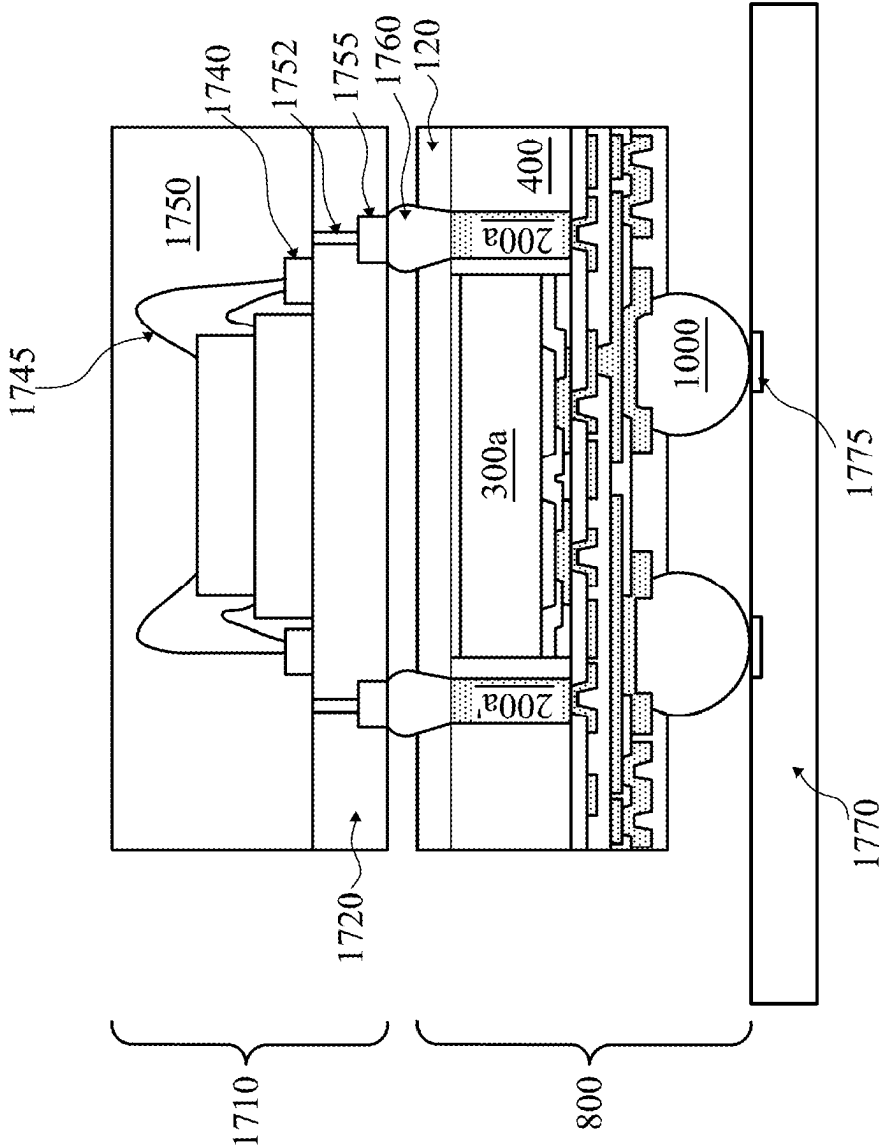


FIG. 17

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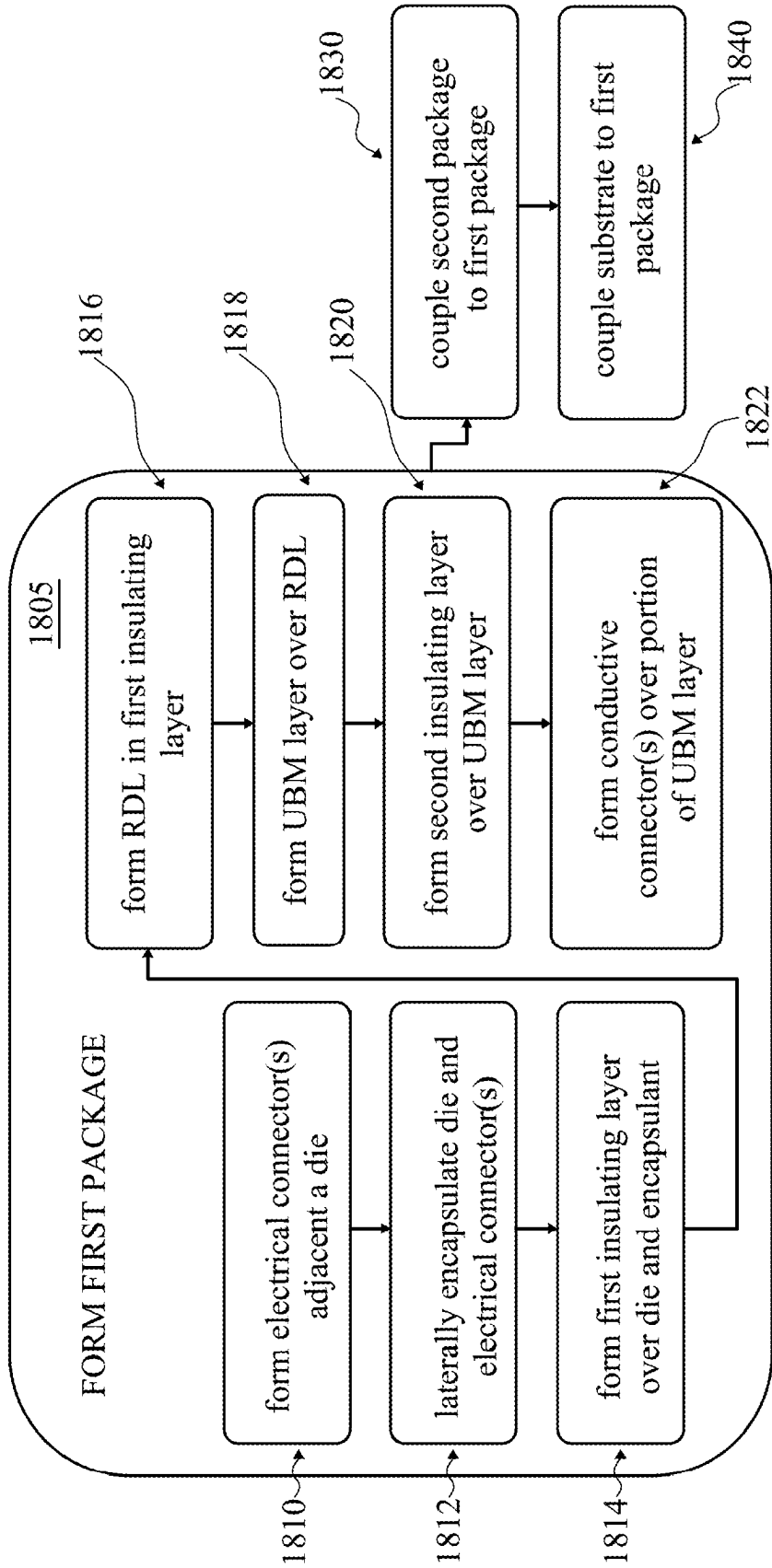


FIG. 18a

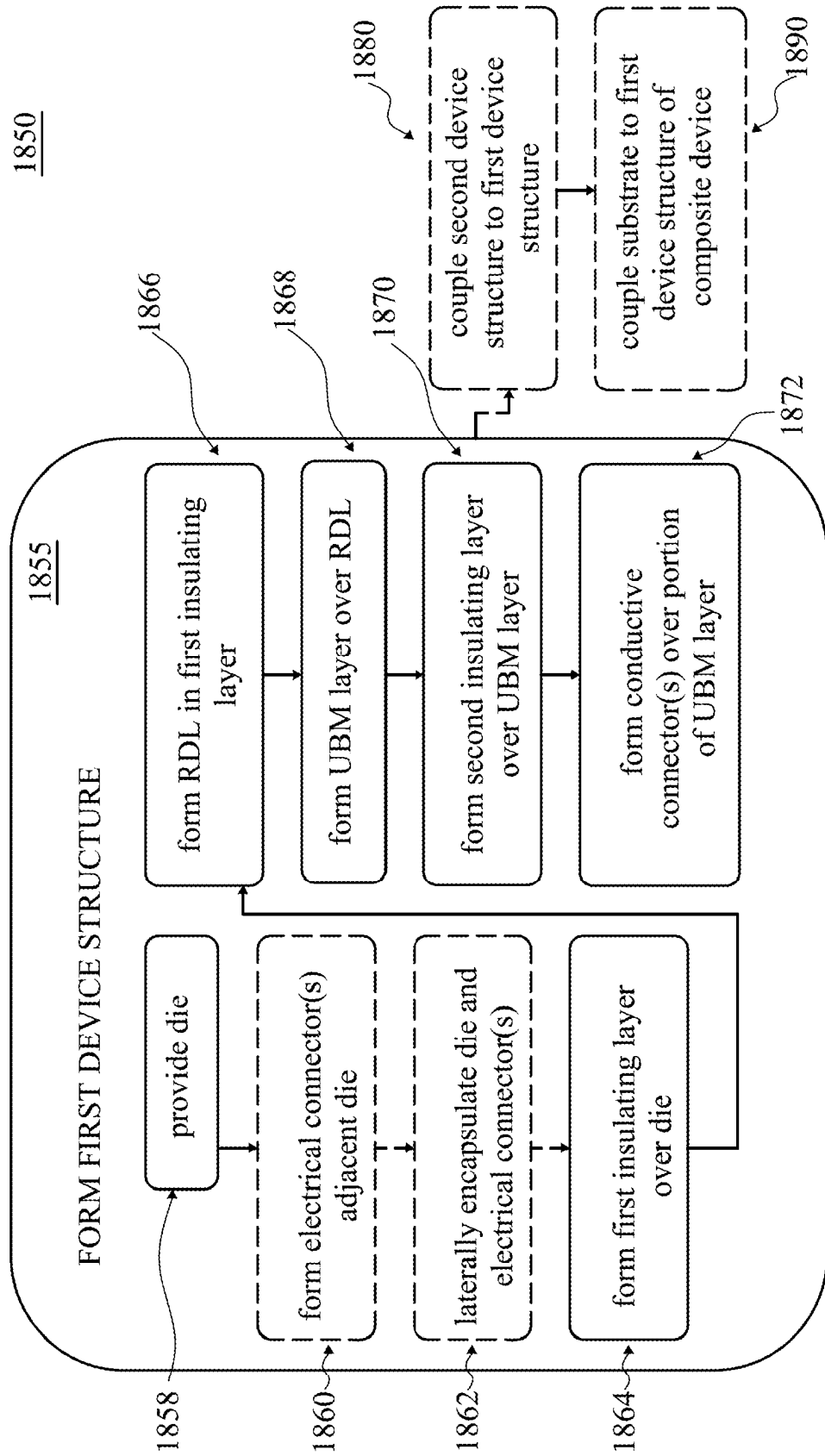


FIG. 18b



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## DEVICE AND METHOD FOR UBM/RDL ROUTING

### CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 16/562,990 filed on Sep. 6, 2019, entitled "Device and Method for UBM/RDL Routing" which is a division of U.S. patent application Ser. No. 15/157,312, filed on May 17, 2016, entitled "Device and Method for UBM/RDL Routing," which applications are hereby incorporated herein by reference in their entirety.

### BACKGROUND

The semiconductor industry has experienced rapid growth due to ongoing improvements in the integration density of a variety of electronic components (e.g., transistors, diodes, resistors, capacitors, etc.). For the most part, improvement in integration density has resulted from iterative reduction of minimum feature size, which allows more components to be integrated into a given area. As the demand for shrinking electronic devices has grown, a need for smaller and more creative packaging techniques of semiconductor dies has emerged. An example of such packaging systems is Package-on-Package (PoP) technology. In a PoP device, a top semiconductor package is stacked on top of a bottom semiconductor package to provide a high level of integration and component density. PoP technology generally enables production of semiconductor devices with enhanced functionalities and small footprints on a printed circuit board (PCB).

### BRIEF DESCRIPTION OF THE DRAWINGS

Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various features are not drawn to scale. In fact, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion.

FIGS. 1 through 15 illustrate cross-sectional views of intermediate steps during a process to form a first package structure, in accordance with some embodiments.

FIGS. 16a, 16b, and 16c illustrate cross-sectional views of various under bump metallurgy (UBM) and redistribution layer (RDL) routing features of a first package structure, in accordance with some embodiments.

FIG. 17 illustrates a cross-sectional view of a Package-on-Package (PoP) structure, in accordance with some embodiments.

FIGS. 18a and 18b are flowcharts illustrating packaging and UBM/RDL fabrication methods, in accordance with some embodiments.

### DETAILED DESCRIPTION

The following disclosure provides many different embodiments, or examples, for implementing different features of the invention. Specific examples of components and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and

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second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

Further, spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to one or more other elements or features as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

Embodiments described herein may be discussed in a specific context, namely electrical routing for under bump metallurgy (UBM) and redistribution layer (RDL) structures in a packaged device. Representative implementations of package structures may include, e.g., a fan-out package. Representatively disclosed embodiments herein are applicable to any package structure, including one or more integrated circuit dies. Other embodiments contemplate other applications, such as different package types and/or different configurations that would be readily apparent to a person of ordinary skill in the art upon reading this disclosure. It should be noted that embodiments discussed herein may not necessarily illustrate every component or feature that may be present in a particular structure. For example, various components may be omitted from a figure, such as when discussion of one or more other components may be sufficient to describe a particular embodiment.

UBM/RDL routing designs of representative embodiments improve reliability considerations relating to, e.g., electromigration, susceptibility to drop damage, and thermal cycling integrity. Accordingly, an improved UBM/RDL routing structure is desirable to provide robust and reliable device package structures.

FIGS. 1 through 15 illustrate cross-sectional views of intermediate steps during a process to form a first package structure in accordance with representative embodiments. FIG. 1 illustrates a carrier substrate 100 and a release layer 110 formed on the carrier substrate 100. A first package region 800a and a second package region 800b, for the formation of a first package and a second package, respectively, are illustrated.

Carrier substrate 100 may be a glass carrier substrate, a ceramic carrier substrate, or the like. Carrier substrate 100 may be a wafer; such that multiple packages can be formed on carrier substrate 100 substantially simultaneously. Release layer 110 may be formed of a polymer-based material, which may be removed along with carrier substrate 100 from overlying structures formed in subsequent steps. In some embodiments, release layer 110 may comprise an epoxy-based, thermal-release material, which loses adhesion when heated, such as a Light-to-Heat-Conversion (LTHC) release coating. In other embodiments, release layer 110 may comprise an ultra-violet (UV) glue, which loses adhesion when exposed to UV light. Release layer 110 may be dispensed as a liquid and cured, may be laminated as a film

on carrier substrate **100**, or the like. The top surface of release layer **110** may be leveled, or otherwise processed to provide acceptable planarity.

An insulating layer **120** is formed on release layer **110**. The bottom surface of insulating layer **120** may be in contact with the top surface of release layer **110**. In some embodiments, insulating layer **120** may be formed of a polymer, such as polybenzoxazole (PBO), polyimide, benzocyclobutene (BCB), or the like. In other embodiments, insulating layer **120** may be formed of a dielectric, a nitride (e.g., silicon nitride), an oxide (e.g., silicon oxide), a glass (e.g., phosphosilicate glass (PSG), borosilicate glass (BSG), boron-doped phosphosilicate glass (BPSG)), or the like. Insulating layer **120** may be formed by any acceptable deposition process, such as spin coating, chemical vapor deposition (CVD), lamination, or the like, or a combination thereof.

As representatively illustrated in FIG. 2, electrical connectors **200a**, **200a'**, **200b**, **200b'** are formed over insulating layer **120**. Electrical connectors **200a** and **200a'** are formed in first package region **800a**. Electrical connectors **200b** and **200b'** are formed in second package region **800b**. As a representative example to form electrical connectors **200a**, **200a'**, **200b**, **200b'**, a seed layer (not shown) is formed on insulating layer **120**. In some embodiments, the seed layer comprises a metal layer, which may be a single layer or a composite layer having a plurality of sub-layers formed of different materials. In some embodiments, the seed layer comprises a titanium layer and a copper layer over the titanium layer. The seed layer may be formed using, e.g., PVD, or the like. Photoresist is formed and patterned on the seed layer. The photoresist may be formed by spin coating, or the like, and may be exposed to light for patterning. The pattern of the photoresist corresponds to subsequently formed electrical connectors **200a**, **200a'**, **200b**, **200b'**. Patterning forms openings through the photoresist to expose the seed layer. A conductive material is formed in the openings of the photoresist and on exposed portions of the seed layer. The conductive material may be formed by plating, such as electroplating or electroless plating, or the like. The conductive material may comprise a metal, e.g., copper, titanium, tungsten, aluminum, or the like. The photoresist and portions of the seed layer on which the conductive material is not formed are removed. The photoresist may be removed by an acceptable ashing or stripping process, e.g., using an oxygen plasma, or the like. Once the photoresist is removed, exposed portions of the seed layer are removed, such as by using an acceptable etching process, e.g., wet or dry etching. Remaining portions of the seed layer and the conductive material form electrical connectors **200a**, **200a'**, **200b**, **200b'**.

As representatively illustrated in FIG. 3, integrated circuit (IC) dies **300a**, **300b** are adhered to insulating layer **120** by an adhesive **310a**, **310b**, respectively. IC dies **300a**, **300b** are adhered in respective first package region **800a** and second package region **800b**. In other embodiments, more or fewer IC dies may be adhered in each region. IC dies **300a**, **300b** may comprise logic dies (e.g., central processing unit, microcontrollers, etc.), memory dies (e.g., dynamic random access memories (DRAM), static random access memories (SRAM), etc.), power management dies (e.g., power management integrated circuits (PMIC)), radio frequency (RF) dies, sensor dies, micro-electro-mechanical-system (MEMS) dies, signal processing dies (e.g., digital signal processors (DSP)), front-end dies (e.g., analog front-end (AFE) dies), or the like, or a combination thereof. In representative embodiments, IC dies **300a**, **300b** may be

different sizes. In other embodiments, IC dies **300a**, **300b** may be substantially the same size.

As provided, IC die **300a** may comprise overlying electrical contact features **320a**, **320a'** (e.g., one or more contact pads), metallization features **330a**, **330a'** (e.g., one or more metallization layers), passivation features **340a** (e.g., one or more passivation layers), insulating features **350a** (e.g., one or more dielectric layers), or the like, or combinations thereof. As provided, IC die **300b** may comprise overlying electrical contact features **320b**, **320b'**, metallization features **330b**, **330b'**, passivation features **340b**, insulating features **350b**, or the like, or combinations thereof. In representative embodiments, a plurality of metallization features and insulating features of IC dies **300a**, **300b** may comprise one or more RDLs.

Electrical contact features **320a**, **320a'**, **320b**, **320b'** may comprise pads, such as aluminum pads, to which external connections may be made. The pads may be disposed on what may be referred to as respective active sides of IC dies **300a**, **300b**. Passivation features **340a**, **340b** may comprise passivation films on IC dies **300a**, **300b** and on portions of the pads. Openings may be formed through the passivation films to the pads. Metallization features **330a**, **330a'**, **330b**, **330b'** may comprise die connectors, such as conductive pillars (e.g., comprising a metal such as copper), in the openings through the passivation films, and may be mechanically and electrically coupled to respective pads. The die connectors may be formed by, for example, plating, or the like. The die connectors provide an electrical connection to respective integrated circuits of IC dies **300a**, **300b**.

Insulating features **350a**, **350b** may comprise insulating material disposed on active sides of IC dies **300a**, **300b**, such as on the passivation films and the die connectors. The insulating material may laterally encapsulate the die connectors and may be substantially laterally co-terminus with lateral extents of respective IC dies **300a**, **300b**. The insulating material may be a polymer (e.g., PBO, polyimide, BCB), a nitride (e.g., silicon nitride), an oxide (e.g., silicon oxide), a glass (e.g., PSG, BSG, BPSG), a dielectric material, and/or the like, or a combination thereof, and may be formed, for example, by spin coating, lamination, CVD, or the like.

Before being adhered to insulating layer **120**, IC dies **300a**, **300b** may be processed according to applicable manufacturing processes to form integrated circuits in IC dies **300a**, **300b**. For example, IC dies **300a**, **300b** may each comprise a semiconductor substrate, such as silicon (doped or undoped) or an active layer of a semiconductor-on-insulator (SOI) substrate. A semiconductor substrate may include other semiconductor material, e.g., germanium, a compound semiconductor (e.g., silicon carbide, gallium arsenic, gallium phosphide, indium phosphide, indium arsenide, indium antimonide), an alloy semiconductor (e.g., SiGe, GaAsP, AlInAs, AlGaAs, GaInAs, GaInP, GaInAsP), and/or the like. Other substrates, such as multi-layered or gradient substrates, may also be used. Devices, such as transistors, diodes, capacitors, resistors, inductors, etc., may be formed in and/or on the semiconductor substrate, and may be interconnected by interconnect structures formed by, e.g., metallization patterns in one or more insulating layers on the semiconductor substrate to form an integrated circuit.

Adhesive **310a**, **310b** is disposed on back-side surfaces of IC dies **300a**, **300b**, respectively, and adheres IC dies **300a**, **300b** to insulating layer **120** (or, in alternative embodiments later described herein, respective back-side redistribution structures). Adhesive **310a**, **310b** may be any suitable adhe-

sive, epoxy, die attach film (DAF), or the like. Adhesive **310a**, **310b** may be applied to a back-side of IC dies **300a**, **300b** prior to die placement, such as to a back-side of a respective semiconductor wafer. IC dies **300a**, **300b** may be subsequently singulated (e.g., such as by sawing or dicing) while adhered to insulating layer **120** by adhesive **310a**, **310b** using, e.g., a pick-and-place tool.

As representatively illustrated in FIG. 4, an encapsulant **400** is formed on and between various components. Encapsulant **400** may at least laterally encapsulate IC dies **300a**, **300b** and electrical connectors **200a**, **200a'**, **200b**, **200b'**. Encapsulant **400** may be a molding compound, epoxy, or the like, and may be applied by compression molding, transfer molding, or the like. After curing, encapsulant **400** may undergo a grinding or other planarization process to expose electrical connectors **200a**, **200a'**, **200b**, **200b'** and die connectors **330a**, **330a'**, **330b**, **330b'**. Top surfaces of electrical connectors **200a**, **200a'**, **200b**, **200b'**, die connectors **330a**, **330a'**, **330b**, **330b'**, and encapsulant **400** may be substantially co-planar (or otherwise share a substantially common topography) after planarization. In some embodiments, grinding or planarization may be omitted; for example, if electrical connectors **200a**, **200a'**, **200b**, **200b'** and die connectors **330a**, **330a'**, **330b**, **330b'** are already exposed.

FIGS. 5 through 8 representatively illustrate formation of a front-side redistribution structure. As representatively illustrated in FIG. 8, the front-side redistribution structure comprises insulating layers **500**, **600**, **700**, metallization patterns **510**, **610**, **710**, and insulating layer **810**.

As representatively illustrated in FIG. 5, insulating layer **500** is deposited on encapsulant **400**, electrical connectors **200a**, **200a'**, **200b**, **200b'**, and die connectors **330a**, **330a'**, **330b**, **330b'**. In some embodiments, insulating layer **500** is formed from and comprises a polymer, which may be a photo-sensitive material such as PBO, polyimide, BCB, or the like, that may be patterned using a lithography mask. In other embodiments, insulating layer **500** may be formed of a nitride (e.g., silicon nitride), an oxide (e.g., silicon oxide), a glass (e.g., PSG, BSG, BPSG), a dielectric material, and/or the like, or a combination thereof. Insulating layer **500** may be formed by spin coating, lamination, CVD, or the like, or a combination thereof.

Insulating layer **500** is patterned to form openings to expose portions of electrical connectors **200a**, **200a'**, **200b**, **200b'** and die connectors **330a**, **330a'**, **330b**, **330b'**. Patterning may be accomplished by any suitable process, such as by employing lithographic exposure of a photo-sensitive material, followed by development and etching; e.g., an anisotropic etch. If insulating layer **500** is a photo-sensitive material, insulating layer **500** can be patterned by exposing, developing, and curing the photosensitive material in accordance with the desired pattern.

Metallization pattern **510** with vias may be formed on insulating layer **500**. For example, a seed layer (not shown) may be formed over insulating layer **500** and in openings through insulating layer **500**. In some embodiments, the seed layer may comprise a metal layer, which may be a single layer or a composite layer having a plurality of sub-layers formed of different materials. In some embodiments, the seed layer comprises a titanium layer and a copper layer over the titanium layer. The seed layer may be formed using, for example, PVD, or the like. Photoresist may then be formed and patterned on the seed layer. The photoresist may be formed by spin coating, or the like, and may be exposed to light for patterning. The pattern of the photoresist corresponds to subsequently formed metallization pattern **510**. Patterning forms openings through the photoresist to expose

the seed layer. A conductive material is formed in the openings of the photoresist and on the exposed portions of the seed layer. The conductive material may be formed by plating, such as electroplating or electroless plating, or the like. The conductive material may comprise a metal, e.g., copper, titanium, tungsten, aluminum, or the like. Thereafter, photoresist and portions of the seed layer on which the conductive material is not formed are removed. The photoresist may be removed by an acceptable ashing or stripping process, e.g., using an oxygen plasma, or the like. Once the photoresist is removed, exposed portions of the seed layer may be removed, such as by using an acceptable etching process, e.g., wet or dry etching. Remaining portions of the seed layer and conductive material form the metallization pattern **510** with vias. The vias of metallization pattern **510** are formed in openings through the insulating layer **500** to electrical connectors **200a**, **200a'**, **200b**, **200b'** and die connectors **330a**, **330a'**, **330b**, **330b'**. In other embodiments, the metallization pattern may be formed by depositing a conductive layer and patterning the conductive layer.

As representatively illustrated in FIG. 6, insulating layer **600** is deposited over and on metallization pattern **510** and insulating layer **500**. In some embodiments, insulating layer **600** is formed of a polymer, which may be a photo-sensitive material such as PBO, polyimide, BCB, or the like, that may be patterned using a lithography mask. In other embodiments, insulating layer **600** may be formed of a nitride (e.g., silicon nitride), an oxide (e.g., silicon oxide), a glass (e.g., PSG, BSG, BPSG), a dielectric material, and/or the like, or a combination thereof. Insulating layer **600** may be formed by spin coating, lamination, CVD, or the like, or a combination thereof.

Insulating layer **600** is patterned to form openings to expose portions of metallization pattern **510**. Patterning may be accomplished by any suitable process, such as by employing lithographic exposure of a photo-sensitive material, followed by development and etching; e.g., an anisotropic etch. If insulating layer **600** is a photo-sensitive material, insulating layer **600** can be patterned by exposing, developing, and curing the photosensitive material in accordance with the desired pattern.

Metallization pattern **610** with vias may be formed on insulating layer **600** in a substantially similar manner as discussed above with reference to metallization pattern **510** with vias on insulating layer **500**.

As representatively illustrated in FIG. 7, insulating layer **700** is deposited over and on metallization pattern **610** and insulating layer **600**. In some embodiments, insulating layer **700** is formed of a polymer, which may be a photo-sensitive material such as PBO, polyimide, BCB, or the like, that may be patterned using a lithography mask. In other embodiments, insulating layer **700** may be formed of a nitride (e.g., silicon nitride), an oxide (e.g., silicon oxide), a glass (e.g., PSG, BSG, BPSG), a dielectric material, and/or the like, or a combination thereof. Insulating layer **700** may be formed by spin coating, lamination, CVD, or the like, or a combination thereof.

Insulating layer **700** is patterned to form openings to expose portions of metallization pattern **610**. Patterning may be accomplished by any suitable process, such as by employing lithographic exposure of a photo-sensitive material, followed by development and etching. If insulating layer **700** is a photo-sensitive material, insulating layer **700** can be patterned by exposing, developing, and curing the photosensitive material in accordance with the desired pattern.

Metallization pattern **710** with vias may be formed on insulating layer **700** in a substantially similar manner as discussed above with reference to metallization pattern **510** with vias on insulating layer **500**.

In a representative embodiment insulating layer **500** and metallization pattern **510** comprise a first RDL, insulating layer **600** and metallization pattern **610** comprise a second RDL, and metallization pattern **710** comprises a UBM layer. Accordingly, a representative front-side redistribution structure may comprise a first RDL (e.g., first insulating layer **500**, first metallization pattern **510**), a second RDL (e.g., second insulating layer **600**, second metallization pattern **610**), and a UBM layer (e.g., third insulating layer **700**, third metallization pattern **710**). In various other embodiments, more or fewer insulating layers and metallization patterns may be formed in a front-side redistribution structure. If fewer insulating layers and metallization patterns are to be formed, representative steps and processes discussed above may be omitted. If more insulating layers and metallization patterns are to be formed, representative steps and processes discussed above may be repeated. One having ordinary skill in the art will readily understand which steps and processes would be omitted or repeated.

Accordingly, various representative embodiments provide a path of electrical routing (as later discussed with reference to FIGS. **16a**, **16b**, and **16c**) from a portion of a UBM layer, down to an RDL line, up to a UBM pad of the UBM layer, then to an external interconnect electrically connected to the UBM pad.

As representatively illustrated in FIG. **8**, insulating layer **810** is deposited over and on metallization pattern **710** and insulating layer **700**. In some embodiments, insulating layer **810** may comprise a polymer, which may be a photo-sensitive material such as PBO, polyimide, BCB, or the like, that may be patterned using a lithography mask. In other embodiments, insulating layer **810** may be formed of a nitride (e.g., silicon nitride), an oxide (e.g., silicon oxide), a glass (e.g., PSG, BSG, BPSG), a dielectric material, and/or the like. Insulating layer **810** may be formed by spin coating, lamination, CVD, or the like, or a combination thereof.

As representatively illustrated in FIG. **9**, insulating layer **810** is patterned to form openings **900a**, **900a'**, **900b**, **900b'** to expose portions (e.g., UBM pad portions **910a**, **910a'**, **910b**, **910b'**) of metallization pattern **710**. Openings **900a**, **900a'**, **900b**, **900b'** are formed on an exterior side of the front-side redistribution structure. Patterning may be accomplished by any suitable process, such as by employing lithographic exposure of a photo-sensitive material, followed by development and etching. Subsequent to forming openings **900a**, **900a'**, **900b**, **900b'**, a trace portion (**1690** as later described with reference to FIG. **16c**) of UBM metallization pattern **710** remains covered by material of insulating layer **810**.

As representatively illustrated in FIG. **10**, conductive connectors **1000a**, **1000a'**, **1000b**, **1000b'** are formed on and coupled to UBM pad portions **910a**, **910a'**, **910b**, **910b'** of metallization pattern **710**. Conductive connectors **1000a**, **1000a'**, **1000b**, **1000b'** may comprise ball grid array (BGA) connectors, solder balls, metal pillars, controlled collapse chip connection (C4) bumps, micro bumps, electroless nickel-electroless palladium-immersion gold technique (ENEPIG) formed bumps, or the like. Conductive connectors **1000a**, **1000a'**, **1000b**, **1000b'** may include a conductive material such as solder, copper, aluminum, gold, nickel, silver, palladium, tin, or the like, or a combination thereof. In some embodiments, conductive connectors **1000a**, **1000a'**, **1000b**, **1000b'** may be formed by initially depositing

a layer of solder with commonly used methods, e.g., evaporation, electroplating, printing, solder transfer, ball placement, or the like. Once a layer of solder has been formed on the structure, a reflow may be performed in order to shape the material into the desired bump shapes. In another embodiment, conductive connectors **1000a**, **1000a'**, **1000b**, **1000b'** may comprise metal pillars (e.g., a copper pillar) formed by sputtering, printing, electroplating, electroless plating, CVD, or the like. The metal pillars may be substantially solder-free and have substantially vertical sidewalls. In some embodiments, a metal cap layer may be formed on the top of the metal pillar connectors. The metal cap layer may include nickel, tin, tin-lead, gold, silver, palladium, indium, nickel-palladium-gold, nickel-gold, or the like, or a combination thereof, and may be formed by a plating process. In accordance with a representative embodiment, conductive connectors **1000a**, **1000a'**, **1000b**, **1000b'** may comprise solder balls having a diameter ranging from, e.g., about 150  $\mu\text{m}$  to about 300  $\mu\text{m}$ .

As representatively illustrated in FIG. **10** (with benefits and advantages further described herein with reference to FIGS. **16a**, **16b**, and **16c**), a representative UBM/RDL structure is provided for routing UBM electrical signals through underlying RDL portions, as compared to, e.g., direct routing through a UBM layer alone.

Testing may be performed after conductive connectors **1000a**, **1000a'**, **1000b**, **1000b'** have been formed, e.g., to identify defective package structures. Thereafter, as representatively illustrated in FIG. **11**, a carrier substrate debonding procedure may be performed to detach (de-bond) carrier substrate **100** from insulating layer **120** (or in accordance with other representative embodiments, a back-side redistribution structure). In accordance with some embodiments, de-bonding includes projecting electromagnetic energy (e.g., laser, UV, or the like) on the release layer **110** so that the release layer **110** decomposes, or otherwise detaches, to permit removal of carrier substrate **100**. The structure is then flipped over and placed on a tape **1100** for further processing.

In accordance with an alternative embodiment, plural insulating layers and metallization layers may be formed over insulating layer **120** before formation of electrical connectors **200a**, **200a'**, **200b**, **200b'** or after carrier substrate **100** removal to produce a back-side redistribution structure that includes one or more insulating layers and one or more metallization layers. Back-side redistribution structures so formed may include any number of insulating layers, metallization patterns, and vias. For example, vias may be formed during the formation of a metallization pattern by forming a seed layer and conductive material of the metallization pattern in an opening of underlying insulating layers. The vias may therefore interconnect and electrically couple various metallization layers in a resulting back-side redistribution structure. The back-side redistribution structure may be formed in a similar manner as discussed above with reference to formation of front-side RDLs.

As representatively illustrated in FIG. **12**, insulating layer **120** is patterned to form openings **1200b'**, **1200b**, **1200a'**, **1200a** to expose back-side portions of electrical connectors **200b'**, **200b**, **200a'**, **200a**. Patterning may be accomplished by any acceptable process, such as by employing lithographic exposure of a photo-sensitive material, followed by development and etching. If insulating layer **120** is a photo-sensitive material, insulating layer **120** can be developed after exposure. Alternatively, openings **1200b'**, **1200b**, **1200a'**, **1200a** may be formed by laser drilling, or the like.

As representatively illustrated in FIG. 13 and FIG. 14, packages **800a**, **800b** are singulated to produce discrete packages. Singulation may be performed by sawing along scribe line **1400**, e.g., between adjacent package regions **800a** and **800b**. Sawing separates first package region **800a** from second package region **800b**. In an embodiment, singulation produces discrete package **800a**, as representatively illustrated in FIG. 15 after removal from tape **1100**. In accordance with various representative embodiments, discrete package **800a** may comprise an integrated fan-out (InFO) package.

In accordance with an embodiment, as representatively illustrated in FIG. 16a, discrete package **800a** may be configured to provide a first electrical connection **1600** to/from a UBM pad **910a** of metallization pattern **710** (and conductive connector **1000a** coupled thereto) from/to a conductive line **1615** of underlying metallization pattern **610**, a second electrical connection **1610** along conductive line **1615** in metallization pattern **610**, and a third electrical connection **1620** to/from conductive line **1615** from/to a UBM layer portion **1625** of overlying metallization pattern **710**. The second electrical connection **1610** provides an electrical connection between the first electrical connection **1600** and the third electrical connection **1620**, such that UBM layer portion **1625** of metallization pattern **710** is in electrical connection (but otherwise not in mechanical or physical contact) with UBM pad **910a**. Consequently, electrical signals can be routed through underlying redistribution layers (for the benefit of, e.g., added protection afforded by overlying material layers) before being routed to laterally disposed portions of overlying UBM metallization pattern **710**. Accordingly, UBM metallization pattern **710**, in addition to providing one or more points of external connection to/from discrete package **800a**, also provides electrical routing within discrete package **800a**.

As representatively illustrated in FIG. 16b, a package **800a** includes molding compound **400** at least laterally encapsulating IC die **300a** and adjacent electrical connectors **200a**, **200a'**. Insulating layers **500**, **600**, **700** are disposed over a top surface **1630a** of IC die **300a**, molding compound **400**, and electrical connectors **200a**, **200a'**. Insulating layer **500** and metallization layer **510** comprise a first RDL. Insulating layer **600** and metallization layer **610** comprise a second RDL. Metallization layer **710** comprises a UBM layer. Bottom surface **1630b** of IC die **300a** (as provided for attachment to insulating layer **120**) comprises an adhesive layer **310a** in contact with back-side insulating layer **120**. At least a portion of conductive connector **1000a** is disposed over and on a first portion **1640** of UBM pad **910a** in UBM metallization layer **710**. A second portion **1650** of UBM metallization layer **710** is separated from the first portion **1640** by insulating material portion **1660** (a first insulating region) of insulating layer **810**. A third portion **1670** of RDL metallization layer **610** electrically couples the first portion **1640** to the second portion **1650**. First portion **1640**, second portion **1650**, and third portion **1670** are electrically coupled to conductive connector **1000a**. Insulating material portion **1675** (a second insulating region) of insulating layer **700** is disposed between and interposes the third portion **1670** of RDL metallization layer **610** and the insulating material portion **1660** of insulating layer **810**.

In accordance with a representative embodiment, insulating material portion **1660** comprises a different material layer than insulating material portion **1675** of insulating layer **700**. In accordance with another representative embodiment, insulating material portion **1660** comprises a different material than insulating material portion **1675** of

insulating layer **700**. In accordance with another representative embodiment, the first portion **1640** and the second portion **1650** may comprise a same material layer formed in a same process step. In accordance with a representative aspect, the first portion **1640** and the second portion **1650** of UBM metallization layer **710** may comprise a same material. In another representative embodiment, the first portion **1640** and the second portion **1650** may comprise a different material than the third portion **1670** of RDL metallization layer **610**. In an embodiment, metallization layer **610** of the second RDL and metallization layer **710** of the UBM layer electrically connects IC die **300a** to conductive connector **1000a**.

As generally illustrated in FIG. 16c, an interconnect design in accordance with a representative embodiment for providing a UBM/RDL routing structure (e.g., sans die) is provided. Insulating layer **600** and metallization layer **610** comprise an RDL. Metallization layer **710** comprises a UBM layer. The UBM layer overlies the RDL. At least a portion of a first conductive connector **1000a** is disposed over and on a first UBM pad **910a**. Conductive connector **1000a** is electrically coupled to first UBM pad **910a**. A first portion **1680** of RDL metallization layer **610** is separated from a second portion **1685** of RDL metallization layer **610** by insulating material **1698** of RDL insulating layer **700**. A UBM trace **1690** is disposed over the RDL and in the UBM metallization layer **710**. The UBM trace **1690** electrically couples the first portion **1680** of the RDL to the second portion **1685** of the RDL. UBM metallization layer **710** comprises the first UBM pad **910a**. Second portion **1685** of RDL metallization layer **610** is electrically coupled to first UBM pad **910a**. Accordingly, first portion **1680** of RDL metallization layer **610** is electrically coupled (thru UBM trace **1690** of the UBM layer, second portion **1685** of metallization layer **610** of the RDL, and first UBM pad **910a** of the UBM layer) to conductive connector **1000a**. UBM trace **1690** of UBM metallization layer **710** is electrically coupled (thru second portion **1685** of metallization layer **610** of the RDL) to first UBM pad **910a**. Notwithstanding the preceding, with respect to metal features within metallization layer **710** of the UBM layer, UBM trace **1690** is not otherwise physically or mechanically coupled to first UBM pad **910a**. That is to say, there is no configuration or distribution of metal features within the UBM layer that would physically connect UBM trace **1690** to first UBM pad **910a** either directly or indirectly.

In a representative embodiment, metallization layer **710** of the UBM layer comprises a second UBM pad **910a'**. At least a portion of a second conductive connector **1000a'** is disposed over and on second UBM pad **910a'**. Second conductive connector **1000a'** is electrically coupled to second UBM pad **910a'**. In accordance with a representative embodiment, second conductive connector **1000a'** and second UBM pad **910a'** are electrically isolated from first UBM pad **910a** and first conductive connector **1000a**. In another representative embodiment, second UBM pad **910a'** and second conductive connector **1000a'** are electrically isolated from first portion **1680** in the underlying RDL. In a further representative embodiment, UBM trace **1690** is electrically isolated from second conductive connector **1000a'** and second UBM pad **910a'**.

In accordance with a representative embodiment, insulating material **1698** of insulating layer **700** comprises a different material layer than insulating material of insulating layer **810**. In accordance with a representative embodiment, insulating material **1698** of insulating layer **700** comprises a different material than insulating material of insulating layer

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**810.** In accordance with a representative embodiment, the first portion **1680** and the second portion **1685** of RDL metallization layer **610** may comprise a same material layer formed in a same process step. In accordance with a representative aspect, the first portion **1680** and the second portion **1685** of RDL metallization layer **610** may comprise a same material. In another representative embodiment, the first portion **1680** and the second portion **1685** may comprise a different material than material forming UBM trace **1690**.

Accordingly, various representative embodiments provide a path of electrical routing from a portion of a UBM layer, to an underlying RDL line, to a UBM pad of the UBM layer, then to an external interconnect.

FIG. **17** representatively illustrates a Package-on-Package (PoP) structure **1700** including package **800** (alternatively referred to as a first package), a second package **1710**, and a substrate **1770**. Second package **1710** includes a substrate **1720** and one or more stacked dies **1730** (**1730a** and **1730b**) coupled to substrate **1720**. Substrate **1720** is, in one embodiment, based on an insulating core such as a fiberglass reinforced resin core, and may include contact pad **1775** for mounting conductive connector **1000**. A representative core material comprises fiberglass resin such as FR4. Alternatives for the core material include bismaleimide-triazine (BT) resin, or alternatively, other printed circuit board (PCB) materials or films. Build up films, such as Ajinomoto build-up film (ABF) or other laminates, may be used for substrate **1720**.

Substrate **1720** may include active and passive devices (not shown in FIG. **17**). As one of ordinary skill in the art will appreciate, a variety of devices, such as transistors, capacitors, resistors, inductors, and/or the like, may be used to provide structural and functional requirements of the design for PoP structure **1700**. Such devices may be formed using any suitable methods.

Substrate **1720** may also include metallization layers (not shown) and through vias **1752**. The metallization layers may be formed over active and passive devices, and are designed to connect various device components to form functional circuitry. The metallization layers may be formed of alternating layers of insulating (e.g., low-k dielectric) and conductive material (e.g., copper), with vias interconnecting the layers of conductive material, and may be formed using any suitable process (e.g., deposition, damascene, dual damascene, or the like). In some embodiments, substrate **1720** is substantially free of active and passive devices.

Substrate **1720** may have bond pads **1740** on a first side of substrate **1720** to couple to stacked dies **1730**, and bond pads **1755** on a second side of substrate **1720**, the second side being opposite the first side of substrate **1720**, to couple to conductive connectors **1760**. Stacked dies **1730** are coupled to substrate **1720** by wire bonds **1745**, although other connections may be used, such as conductive bumps. In an embodiment, stacked dies **1730** may comprise, e.g., stacked memory dies. For example, stacked memory dies **1730** may include low-power (LP) double data rate (DDR) memory modules, such as LPDDR1, LPDDR2, LPDDR3, or like memory modules, or combinations thereof. In some embodiments, stacked dies **1730** and wire bonds **1745** may be encapsulated by a molding material **1750**.

After second packages **1710** are formed, second packages **1710** are bonded to first packages **800** by way of conductive connectors **1760**, bond pads **1755**, and electrical connectors **200**. In some embodiments, stacked memory dies **1730** may be coupled to IC dies **300** through wire bonds **1745**, bond pads **1740** and **1755**, through vias **1752**, conductive connectors **1760**, and electrical connectors **200**. Conductive

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connectors **1760** may be similar to conductive connectors **1000** described above, and the description is not repeated herein, although conductive connectors **1760** and **1000** need not be the same.

Semiconductor package **1700** includes packages **800** and **1710** being mounted to a substrate **1770**. Substrate **1770** may be referred to as a package substrate **1770**. Second package **1710** is mounted to package substrate **1770** through first package **800** using conductive connectors **1000**. Package substrate **1770** may include active and passive devices (not shown in FIG. **17**). As one of ordinary skill in the art will appreciate, a variety of devices, such as transistors, capacitors, resistors, inductors, and/or the like, may be used to meet structural and functional requirements of the design for PoP package **1700**, and may be formed using any suitable methods. In some embodiments, package substrate **1770** is substantially free of active and passive devices.

As generally illustrated in FIG. **18a**, a representative method **1800** for forming a PoP structure **1700** begins with a first process **1805** to form a first package. In step **1810**, one or more electrical connectors are formed adjacent a die. In step **1812**, the die and electrical connector(s) are encapsulated with an encapsulating material (e.g., molding compound). In step **1814**, a first insulating layer is formed over the die and electrical connector(s). In step **1816**, an RDL is formed in the first insulating layer. In step **1818**, a UBM layer is formed over the RDL. In step **1820**, a second insulating layer is formed over the UBM layer. In step **1822**, one or more conductive connectors are formed over at least a portion of the UBM layer. In a representative embodiment, first process **1805** comprises steps **1810**, **1812**, **1814**, **1816**, **1818**, **1820**, and **1822**. Processing may continue with step **1830**, where the first package is coupled to a second package. In step **1840**, the first package of the combined PoP structure is coupled to a substrate.

As generally illustrated in FIG. **18b**, a representative method **1850** for forming a UBM/RDL routing structure begins with a first process **1855** to form a first device structure. In step **1858**, a die is provided. In step **1860**, one or more electrical connectors are optionally (as denoted by dashed lines in FIG. **18b**) formed adjacent the die. In step **1862**, the die and optional electrical connector(s) are optionally encapsulated with an encapsulating material (e.g., molding compound). In step **1864**, a first insulating layer is formed over the die. In step **1866**, an RDL is formed in the first insulating layer. In step **1868**, a UBM layer is formed over the RDL. In step **1870**, a second insulating layer is formed over the UBM layer. In step **1872**, one or more conductive connectors are formed over at least a portion of the UBM layer. In a representative embodiment, first process **1855** comprises steps **1858**, **1864**, **1866**, **1868**, **1870**, and **1872**. In another representative embodiment, first process **1855** comprises steps **1858**, **1864**, **1866**, **1868**, **1870**, **1872**, and optionally one or both of steps **1860** and **1862**. Processing may continue with step **1880**, where the first device structure may be optionally coupled to a second device structure. In step **1890**, a composite device comprising the coupled second device structure and first device structure may be optionally coupled to a substrate.

Embodiments of representative devices and methods may have several advantages. For example, ball fatigue (normalized to designs employing direct UBM routing) is reduced by a factor of about 67% with utilization of a routing design in accordance with representative embodiments. The predicted package lifespan (normalized to designs employing direct UBM routing) is increased by a factor of about 82% with utilization of a routing design in accordance with

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representative embodiments. Additionally, the current capacity of an electrical routing design in accordance with representative embodiments for simulated failure at an operating temperature of 110° C. for 10 years (normalized to designs employing direct UBM routing) is improved by a factor of about 300%. Benefits, other advantages, and solutions to problems have been described with regard to specific embodiments; however, benefits, advantages, solutions to problems, and any component(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or component.

In accordance with a representative embodiment, a method includes the steps of: forming a redistribution layer (RDL) over a first side of a first die, the first die having a second side opposite the first side, the RDL comprising a first portion and a second portion, the first portion separated from the second portion by insulating material of the RDL, the first portion and the second portion at a same level in the RDL; forming an under bump metallurgy (UBM) layer over the RDL, the UBM layer comprising a UBM trace and a UBM pad, the UBM trace electrically coupling the first portion to the second portion, the UBM pad electrically coupled to the second portion; and forming a first conductive connector over and electrically coupled to the UBM pad. A first electrical connector is formed adjacent the first die. The RDL and the UBM pad electrically connect the first die to the first conductive connector. The first die and the first electrical connector are at least laterally encapsulated with a molding compound to form a first package. A second package is coupled to the first package using a second set of conductive connectors, the second package being proximate the second side of the first die, the second package comprising a second die. The first portion and the second portion may comprise a same material. The first portion and the second portion may be formed in a same step. An insulating layer may be formed over the UBM layer.

In accordance with another representative embodiment, a method includes forming a first package by: at least laterally encapsulating a first die and a first electrical connector with a molding compound, the first electrical connector adjacent the first die, the first die having a first side and a second side, the second side opposite the first side; forming an insulating layer over the first side of the first die and the molding compound; forming a metallization pattern in the insulating layer; forming an under bump metallurgy (UBM) layer over the metallization pattern; forming an insulating layer over the UBM layer; and forming a first conductive connector over a first portion of the UBM layer, the UBM layer comprising a second portion separated from the first portion by insulating material of the insulating layer, the metallization pattern comprising a third portion that electrically couples the first portion and the second portion, the first portion, the second portion, and the third portion electrically coupled to the first conductive connector, and insulating material of the UBM layer interposed between the third portion and the insulating material, wherein the insulating material is in a different material layer than the insulating material. The metallization pattern and the UBM layer electrically connects the first die to the first conductive connector. The UBM layer may be conformally deposited. The first portion and the second portion may comprise a same material. The first portion and the second portion may comprise a different material than the third portion. The first portion and the second portion may be formed in a same step. The first portion may comprise a UBM pad. A second package may be coupled to the first package using a second

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set of conductive connectors, the second package being proximate the second side of the first die. A substrate may be coupled to the first package using the first conductive connector, and the second package comprises a second die.

In accordance with another representative embodiment, a package structure has a first package including: a molding compound laterally encapsulating a die and an electrical connector, the electrical connector adjacent the die, the die having a first side and a second side opposite the first side; a redistribution layer (RDL) over the first side of the die and the molding compound; an under bump metallurgy (UBM) layer over the RDL; an insulating layer over the UBM layer; and a first conductive connector over a first portion of the UBM layer; wherein: the UBM layer comprises a second portion separated from the first portion by insulating material of the insulating layer; the RDL comprises a third portion disposed under and electrically coupling the first portion and second portion; the first portion, second portion, and third portion electrically connected to the first conductive connector; insulating material of the UBM layer is interposed between the third portion and the insulating material; and the insulating material is a different material layer than the insulating material. The RDL and the UBM layer electrically connects the die to the first conductive connector. A second package may be coupled to the first package using a second set of conductive connectors, the second package being proximate the second side of the die.

The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A micro-electromechanical systems (MEMS) package structure, comprising:

- a circuit layer;
- a MEMS die on the circuit layer;
- an adhesive in physical contact with the MEMS die;
- a conductive pillar having a top surface and disposed on the circuit layer adjacent to the MEMS die;
- an encapsulant on the circuit layer and encapsulating the MEMS die and the conductive pillar, the encapsulant being a single material and having a constant thickness, wherein the conductive pillar has a height at least as high as a largest height of the encapsulant and at least as high as a largest height of a combination of the MEMS die and the adhesive in physical contact with the MEMS die; and
- a polymer layer disposed on the encapsulant and on the top surface of the conductive pillar, wherein the polymer layer defines a recess that exposes at least a portion of the top surface of the conductive pillar, wherein the polymer layer comprises openings, wherein the openings are the only openings through the polymer layer, the recess being one of the openings, and wherein each of the openings within the polymer layer exposes a conductive material, the conductive pillar being part of the conductive material.

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2. The MEMS package structure of claim 1, further comprising a seed layer.

3. The MEMS package structure of claim 1, wherein a sidewall of the conductive pillar directly contacts the encapsulant.

4. The MEMS package structure of claim 1, wherein the polymer layer comprises polyimide (PI) or polybenzoxazole (PBO).

5. The MEMS package structure of claim 1, further comprising an external connector located within the recess and in physical contact with the top surface of the conductive pillar.

6. The MEMS package structure of claim 5, further comprising a package bonded to the external connector.

7. The MEMS package structure of claim 1, wherein the conductive pillar has a straight sidewall as the conductive pillar extends through the encapsulant.

8. A micro-electromechanical systems (MEMS) package structure, comprising:

a polymer layer adjacent to a conductive pillar;  
a recess defined through the polymer layer, wherein the recess exposes at least a portion of the conductive pillar, wherein the recess is one of a plurality of recesses, and wherein each of the plurality of recesses recess within the polymer layer exposes a conductive material;

an encapsulant on the polymer layer and encapsulating the conductive pillar and a MEMS die, wherein the conductive pillar has a height at least as high as a largest height of the encapsulant and at least as high as a largest height of a combination of the MEMS die and an adhesive in physical contact with the MEMS die; and a circuit layer on both the conductive pillar and the MEMS die.

9. The MEMS package structure of claim 8, wherein a sidewall of the conductive pillar directly contacts the encapsulant.

10. The MEMS package structure of claim 8, further comprising a seed layer.

11. The MEMS package structure of claim 8, wherein the polymer layer comprises polyimide (PI) or polybenzoxazole (PBO).

12. The MEMS package structure of claim 8, further comprising an external connector located within the recess and in physical contact with a top surface of the conductive pillar.

13. The MEMS package structure of claim 12, further comprising a package bonded to the external connector.

14. The MEMS package structure of claim 8, wherein the circuit layer comprises:

an underbump metallization layer with a trace portion and an external connection portion, the external connection portion being in physical contact with an external connector;

a passivation layer in physical contact with the external connector, the passivation layer electrically isolating each top surface of the trace portion;

a dielectric material underlying the trace portion, the dielectric material having eight straight surfaces in a single cross-sectional view, wherein:

each one of the eight straight surfaces is at a non-zero angle to each adjacent one of the eight straight surfaces;

only three of the eight straight surfaces are in physical contact with a continuous portion of the trace portion;

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only two of the eight straight surfaces are in physical contact with a first portion of a metallization layer, the first portion of the metallization layer being in physical contact with the trace portion;

only two of the eight straight surfaces are in physical contact with a second portion of the metallization layer, the second portion of the metallization layer being in physical contact with the trace portion and the second portion of the metallization layer being separated from the first portion of the metallization layer by the dielectric material; and

only one of the eight straight surfaces being in physical contact with an underlying dielectric layer.

15. A micro-electromechanical systems (MEMS) package structure, comprising:

an encapsulant comprising a first material throughout the encapsulant, wherein the encapsulant has a constant thickness;

a MEMS die encapsulated by the encapsulant;

an adhesive in direct physical contact with the MEMS die;

a conductive pillar extending from a first side of the encapsulant to a second side of the encapsulant opposite the first side, wherein a first side of the conductive pillar is planar with the MEMS die and a second side of the conductive pillar is planar with the adhesive, wherein both the first side of the conductive pillar and the second side of the conductive pillar are planar with the first material, and wherein the conductive pillar has a height at least as high as a largest height of the encapsulant and at least as high as a largest height of a combination of the MEMS die and the adhesive in direct physical contact with the MEMS die;

a circuit layer on a first side of the encapsulant; and

a polymer layer on a second side of the encapsulant opposite the first side of the encapsulant, wherein the conductive pillar is exposed by a first opening within the polymer layer, wherein the first opening is one of a plurality of openings, and wherein each of the plurality of openings extending from a surface of the polymer layer exposes a conductive material.

16. The MEMS package structure of claim 15, wherein a sidewall of the conductive pillar directly contacts the encapsulant.

17. The MEMS package structure of claim 15, further comprising a seed layer.

18. The MEMS package structure of claim 15, wherein the polymer layer comprises polyimide (PI) or polybenzoxazole (PBO).

19. The MEMS package structure of claim 15, wherein the circuit layer has an underbump metallization layer, wherein a continuous portion of the underbump metallization layer completely covers, in a single cross-section, a mushroom shaped dielectric material with no more than eight straight sides in the cross-section, the continuous portion of the underbump metallization layer in physical contact with three of the straight sides, four of the straight sides being in physical contact with a metallization layer, and a single side being in physical contact with an underlying second dielectric material.

20. The MEMS package structure of claim 15, wherein the conductive pillar has a constant width through the encapsulant.