United States Patent Application Publication	20250267934
Kind Code	A1
Publication Date	August 21, 2025
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SEMICONDUCTOR DEVICE INCLUDING TRANSISTORS WITH DIFFERENT THRESHOLD VOLTAGES AND METHOD OF FABRICATING THE SAME

Abstract

A semiconductor device includes: a plurality of transistors on a substrate, each transistor of the plurality of transistors including a source region, a drain region, a gate structure, a polarization modulation portion, and a polarization layer. The polarization modulation portion of each of the plurality of transistors is on the polarization layer, the plurality of transistors includes a first transistor having a first threshold voltage that has a first fixed value, and the plurality of transistors includes a second transistor having a second threshold voltage that has a second fixed value different from the first fixed value.

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Family ID: **1000008576787**

Appl. No.: **19/199778**

Filed: **May 06, 2025**

Related U.S. Application Data

parent US continuation 18629823 20240408 parent-grant-document US 12317587 child US 19199778
parent US continuation 18104734 20230201 parent-grant-document US 11973078 child US 18629823
parent US continuation 17330851 20210526 parent-grant-document US 11581310 child US 18104734
parent US continuation 16576525 20190919 parent-grant-document US 11024626 child US

17330851
us-provisional-application US 62753618 20181031

Publication Classification

Int. Cl.: **H10D84/84** (20250101); **H03K17/687** (20060101); **H10D30/01** (20250101); **H10D30/47** (20250101); **H10D64/60** (20250101); **H10D84/05** (20250101)

U.S. Cl.:

CPC **H10D84/84** (20250101); **H03K17/6871** (20130101); **H10D30/015** (20250101); **H10D30/475** (20250101); **H10D64/602** (20250101); **H10D84/05** (20250101);

Background/Summary

CROSS-REFERENCE TO RELATED APPLICATIONS [0001] This application is a continuation application of U.S. patent application Ser. No. 18/629,823, filed Apr. 8, 2024, which is a continuation application of U.S. patent application Ser. No. 18/104,734, filed Feb. 1, 2023, now U.S. Pat. No. 11,973,078, issued Apr. 30, 2024, which is a continuation application of U.S. patent application Ser. No. 17/330,851, filed May 26, 2021, now U.S. Pat. No. 11,581,310, issued Feb. 14, 2023, which is a continuation application of U.S. patent application Ser. No. 16/576,525, filed Sep. 19, 2019, now U.S. Pat. No. 11,024,626, issued Jun. 1, 2021, which claims priority to U.S. Provisional Patent Application No. 62/753,618, entitled “TRANSISTORS HAVING MULTIPLE THRESHOLD VOLTAGES AND METHODS OF FABRICATING THE SAME,” and filed on Oct. 31, 2018, each of which is incorporated in its entirety by reference herein.

BACKGROUND
[0002] In an integrated circuit (IC), an enhancement-mode N-type transistor, e.g., enhancement-mode high-electron-mobility transistor (E-HEMT), may be used as a pull-up device to minimize static current. In order to achieve near full-rail pull-up voltage and fast slew rate, a significantly large over-drive voltage is needed for an N-Type enhancement-mode transistor. That is, the voltage difference between gate and source (Vgs) should be much larger than the threshold voltage (Vt), i.e., (Vgs−Vt>>0). It is imperative to use a multi-stage E-HEMT-based driver for integrated circuit to minimize static current. Nevertheless, multi-stage E-HEMT based drivers will not have enough over-drive voltage (especially for the last-stage driver) due to one Vt drop across each stage of E-HEMT pull-up device and one forward voltage (Vf) drop across boot-strap diode. Although one can reduce the Vt for the pull-up E-HEMT transistors and Vf of diode-connected E-HEMT rectifier of multi-stage drivers to provide significantly enough over-drive voltage and dramatically reduce static current, the noise immunity will be compromised.
[0003] In an existing semiconductor wafer, transistors formed on the wafer have identical structures such that they have a same threshold voltage Vt. When Vt of one transistor is reduced, Vt's of other transistors on the wafer are reduced accordingly. As Vt being reduced in this case, a power switch HEMT driven by the HEMT-based driver will have a poor noise immunity because the power switch HEMT cannot withstand a large back-feed-through impulse voltage to its gate. Thus, existing apparatus and circuits including multiple transistors are not entirely satisfactory.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Aspects of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that various features are not necessarily drawn to scale. In fact, the dimensions and geometries of the various features may be arbitrarily increased or reduced for clarity of discussion. Like reference numerals denote like features throughout the specification and drawings.

[0005] FIG. **1** illustrates an exemplary circuit having a multi-stage boot-strapped driver, in accordance with some embodiments of the present disclosure.

[0006] FIGS. **2**A, **2**B, **2**C, **2**D, **2**E, and **2**F illustrate cross-sectional views of exemplary semiconductor devices each including transistors with different threshold voltages, in accordance with some embodiments of the present disclosure.

[0007] FIGS. **3**A, **3**B, **3**C, **3**D, **3**E, **3**F, **3**G, **3**H, **3**I, **3**J, **3**K, **3**L, **3**M, **3**N, **3**O, **3**P, and **3**Q illustrate cross-sectional views of an exemplary semiconductor device during various fabrication stages, in accordance with some embodiments of the present disclosure.

[0008] FIGS. **4**A and **4**B show a flow chart illustrating an exemplary method for forming a semiconductor device including transistors with different threshold voltages, in accordance with some embodiments of the present disclosure.

DETAILED DESCRIPTION

[0009] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of components, values, operations, materials, arrangements, or the like, are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. Other components, values, operations, materials, arrangements, or the like, are contemplated. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0010] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper” and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly. Terms such as “attached,” “affixed,” “connected” and “interconnected,” refer to a relationship wherein structures are secured or attached to one another either directly or indirectly through intervening structures, as well as both movable or rigid attachments or relationships, unless expressly described otherwise.

[0011] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and the present disclosure, and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0012] Reference will now be made in detail to the present embodiments of the disclosure, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0013] An enhancement-mode high-electron-mobility transistor (HEMT), e.g., a gallium nitride (GaN) HEMT, has superior characteristics to enable high performance and smaller form factor in power conversion and radio frequency power amplifier and power switch applications compared to silicon based transistors. But there is no viable p-type HEMT available mostly due to much lower p-type mobility and partly due to two dimensional hole gas (2DHG) band structure. While n-type GaN HEMTs are used in an integrated circuit, to minimize static current, the pull-up devices are mostly based on enhancement-mode n-type transistors rather than depletion-mode n-type transistors.

[0014] A multi-stage HEMT based driver can be used for an integrated circuit to minimize static current. But multi-stage HEMT-based drivers will not have enough over-drive voltage (especially for the last-stage driver) due to one threshold voltage (Vt) drop across each stage of HEMT pull-up device and one forward voltage (Vf) drop across boot-strap diode. Although one can reduce the Vt for the pull-up HEMT transistors and Vf of diode-connected HEMT rectifier of multi-stage drivers to provide significantly enough over-drive voltage and dramatically reduce static current, the noise immunity will be compromised.

[0015] Instead of reducing a single value of the threshold voltage (Vt) of the HEMT transistors in an IC, the present teaching discloses apparatuses and circuits including multiple Vt transistors and their fabrication process. In one embodiment, a plurality of transistors formed on a same wafer have different Vt's. The wafer has an active layer comprising a plurality of active portions, and a polarization modulation layer comprising a plurality of polarization modulation portions each of which is disposed on a corresponding one of the plurality of active portions. Each of the plurality of transistors includes a source region, a drain region, and a gate structure formed on a corresponding one of the plurality of polarization modulation portions. The transistors have at least three different threshold voltages.

[0016] The different threshold voltages among the plurality of transistors are achieved by manners selected from the following: different gate materials (e.g. tungsten, nickel), different p-type doping materials (e.g. magnesium, beryllium) in corresponding polarization modulation portions, different thicknesses of corresponding active portions, different material compositions (e.g. aluminum compositions) of corresponding active portions, and different material structures (e.g. homogeneous or graded) of corresponding active portions. While a lower work-function gate material, e.g., tungsten (W) or titanium/tungsten/titanium-nitride (Ti/W/TiN) metal stack, can be used for implementing a high-Vt HEMT; a higher work-function gate material, e.g., nickel (Ni) or titanium/nickel/titanium-nitride (Ti/Ni/TiN) metal stack, can be used for implementing a low-Vt HEMT. GaN transistors having different Vt's can be implemented by depositing different gate materials.

[0017] The active layers may be aluminum gallium nitride (AlGaN) layers on a same GaN layer, which is a channel layer for the transistors. Different thicknesses of the AlGaN layers can change the amount of spontaneous polarization and piezoelectric polarization between the AlGaN layer and the GaN layer. A thicker AlGaN layer introduces higher polarizations and hence creates more amount of two dimensional electron gas (2DEG) to lower the Vt. In addition, different material compositions of the AlGaN layers can also change the polarization amount between the AlGaN layer and the GaN layer. A higher Al composition (concentration) introduces higher polarizations and hence creates more amount of 2DEG to lower the Vt. Further, different material structures of the AlGaN layers can also change the polarization amount between the AlGaN layer and the GaN layer. For example, one transistor's active AlGaN layer has a graded structure that includes a plurality of sub-layers each of which comprises AlGaN with a different Al proportion, while the other transistor's active AlGaN layer has a homogeneous structure that comprises AlGaN with a single constant Al proportion. The graded AlGaN has less polarizations, introduces less amount of 2DEG, and hence increases the Vt. Hence, GaN transistors having different Vt's can be implemented by depositing AlGaN layers with different Al compositions, different thicknesses, and/or different material structures.

[0018] In addition, different p-type doping materials of the polarization modulation portions (i.e., GaN gate stacks) may be chosen to obtain different Vt transistors correspondingly. Several column I and column II elements, e.g., magnesium (Mg), lithium (Li), sodium (Na), beryllium (Be), calcium (Ca), can be chosen as doping materials for the p-typed doped GaN (pGaN) gate stacks for the GaN based transistors. Different p-type doping materials will induce different work functions of the pGaN gate to achieve different-Vt GaN devices. For instance, a Mg-doped pGaN gate stack will induce a higher Vt than a Be-doped pGaN gate stack.

[0019] In one embodiment, the plurality of transistors includes three transistors having three different Vt's respectively. Among the three transistors, the first transistor and the second transistor are different in terms of a first manner selected from the above manners; the second transistor and the third transistor are different in terms of a second manner selected from the above manners. The first manner is different from the second manner. For example, the first transistor and the second transistor have different gate materials, while the second transistor and the third transistor have different p-type doping materials in the corresponding polarization modulation portions.

[0020] The disclosed apparatus can adjust the work function difference between the gate electrode and the AlGaN layer, and the polarization amount between the AlGaN layer and the GaN layer to create multiple-Vt (or various-Vt) transistors on a same semiconductor wafer; and generate different amount of 2DEG for transistors at different locations of the same wafer. The present disclosure is applicable to any transistor-based IC. The proposed apparatus and methods can enable a transistor-based IC to reduce the static current significantly and have significantly large over-drive voltages for drivers of concern; without compromising noise immunity while increasing over-drive voltages and reducing static currents. In addition, the disclosed apparatus and methods can provide IC designers the flexibility of using different Vt devices for specific functions of improving performance, reducing static current, improving noise immunity, etc.

[0021] FIG. **1** illustrates an exemplary circuit **100** having a multi-stage boot-strapped driver, in accordance with some embodiments of the present disclosure. As shown in FIG. **1**, the circuit **100** includes a driver having multiple stages **110**, **120**, **130** serially connected to drive an output power switch transistor (power switch HEMT) **175**. Each stage includes multiple transistors.

[0022] The stage **110** in this example includes transistors **141**, **151**, **152**, **153**, **154**, **155**, **156**. In one embodiment, among these transistors, the transistor **154** is a low voltage depletion-mode high electron mobility transistor (LV D-HEMT) **192**; while each of the other transistors **141**, **151**, **152**, **153**, **155**, **156** is a low voltage enhancement-mode high electron mobility transistor (LV E-HEMT) **191**.

[0023] As shown in FIG. **1**, the gate of the transistor **151** is electrically connected to an input pin **131** of the circuit **100**. The input pin **131** has an input voltage Vin ranged from a low logic state voltage (e.g., 0 V) to a high logic state voltage (e.g., 6V). When the circuit **100** is turned off, the Vin is 0. The circuit **100** is turned on after the Vin is increased to 6V. The transistor **151** has a source electrically connected to ground Vss **111** which has a ground voltage 0V; and has a drain electrically connected to a source of the transistor **154**. The transistor **152** in this example has a gate electrically connected to the input pin **131**, a source electrically connected to the ground Vss **111** which has a ground voltage 0V, and a drain electrically connected to a source of the transistor **155**. Similarly, the transistor **153** in this example has a gate electrically connected to the input pin **131**, a source electrically connected to the ground Vss **111** which has a ground voltage 0V, and a drain electrically connected to a source of the transistor **156**.

[0024] The transistor **154** in this example has a gate electrically connected to its own source, which is electrically connected to the drain of the transistor **151**. Drain of the transistor **154** is electrically connected to a source of the transistor **141**. The transistor **155** in this example has a gate electrically connected to the source of the transistor **154** and electrically connected to the drain of the transistor **151**. The transistor **155** has a source electrically connected to the drain of the transistor **152**, and a drain electrically connected to a power supply pin VDD **101** which has a positive power supply voltage (e.g., 6V). Similarly, the transistor **156** in this example has a gate electrically connected to the source of the transistor **154** and electrically connected to the drain of the transistor **151**, a source electrically connected to the drain of the transistor **153**, and a drain electrically connected to the power supply pin VDD **101** which has a positive power supply voltage 6V.

[0025] The transistor **141** in this example has a gate electrically connected to its own drain, which is electrically connected to the power supply pin VDD **101** which has a positive power supply voltage 6V. The transistor **141** connected in this specific configuration is functioning like a rectifier or diode and is conventionally called as a diode-connected transistor. Source of the transistor **141** is electrically connected to the drain of the transistor **154**. The stage **110** further includes a capacitor **121** coupled between the source of the transistor **141** and the source of the transistor **155**.

[0026] The stage **120** in this example includes transistors **142**, **161**, **162**, **163**, **164**, **165**, **166**. In one embodiment, among these transistors, the transistor **164** is a low voltage depletion-mode high electron mobility transistor (LV D-HEMT) **192**; while each of the other transistors **142**, **161**, **162**, **163**, **165**, **166** is a low voltage enhancement-mode high electron mobility transistor (LV E-HEMT) **191**.

[0027] As shown in FIG. **1**, the gate of the transistor **161** is electrically connected to a node **181**, which is electrically connected to the source of the transistor **156** and the drain of the transistor **153**. The node **181** has a voltage ranged between Vss and VDD (0 and 6V). When the circuit **100** is turned off, the Vin is 0, such that the transistor **153** is turned off and the transistor **156** is turned on. The node **181** has the same voltage 6V as the power supply pin VDD **101**. When the circuit **100** is turned on and the Vin has a voltage of 6V, the transistor **153** is turned on and the transistor **156** is turned off. The node **181** has the same voltage 0V as the ground Vss **111**.

[0028] The transistor **161** has a source electrically connected to ground Vss **111** which has a ground voltage 0V; and has a drain electrically connected to a source of the transistor **164**. The transistor **162** in this example has a gate electrically connected to the node **181**, a source electrically connected to the ground Vss **111** which has a ground voltage 0V, and a drain electrically connected to a source of the transistor **165**. Similarly, the transistor **163** in this example has a gate electrically connected to the node **181**, a source electrically connected to the ground Vss **111** which has a ground voltage 0V, and a drain electrically connected to a source of the transistor **166**.

[0029] The transistor **164** in this example has a gate electrically connected to its own source, which is electrically connected to the drain of the transistor **161**. Drain of the transistor **164** is electrically connected to a source of the transistor **142**. The transistor **165** in this example has a gate electrically connected to a node **185**, which is electrically connected to the source of the transistor **164** and electrically connected to the drain of the transistor **161**. The transistor **165** has a source electrically connected to the drain of the transistor **162**, and a drain electrically connected to the source of the transistor **142**. The transistor **166** in this example has a gate electrically connected to a node **186**, which is electrically connected to the source of the transistor **165** and electrically connected to the drain of the transistor **162**, a source electrically connected to the drain of the transistor **163**, and a drain electrically connected to a power supply pin VDD **102** which has a positive power supply voltage (e.g., 6V).

[0030] The transistor **142** in this example has a gate electrically connected to its own drain (i.e., diode-connected to act like a rectifier or a diode), which is electrically connected to the power supply pin VDD **102** which has a positive power supply voltage 6V. Source of the transistor **142** is electrically connected to the drain of the transistor **164** and the drain of the transistor **165**. The stage **120** further includes a capacitor **122** coupled between a node **184** electrically connected to the source of the transistor **142** and a node **183** electrically connected to the source of the transistor **166**.

[0031] The stage **130** in this example includes transistors **143**, **171**, **172**, **173**, **174**. In one embodiment, each of these transistors is a low voltage enhancement-mode high electron mobility transistor (LV E-HEMT) **191**. As shown in FIG. **1**, the gate of the transistor **171** is electrically connected to a node **182**, which is electrically connected to the node **181**, the source of the transistor **156** and the drain of the transistor **153**. Same as the node **181**, the node **182** has a voltage ranged between Vss and VDD (0 and 6V). When the circuit **100** is turned off, the Vin is 0, such that the transistor **153** is turned off and the transistor **156** is turned on. The node **181** and the node **182** have the same voltage 6V as the power supply pin VDD **101**. When the circuit **100** is turned on and the Vin has a voltage of 6V, the transistor **153** is turned on and the transistor **156** is turned off. The node **181** and the node **182** have the same voltage 0V as the ground Vss **111**.

[0032] The transistor **171** has a source electrically connected to ground Vss **111** which has a ground voltage 0V; and has a drain electrically connected to a source of the transistor **173**. The transistor **172** in this example has a gate electrically connected to the node **182**, a source electrically connected to the ground Vss **111** which has a ground voltage 0V, and a drain electrically connected to a source of the transistor **174**.

[0033] The transistor **173** in this example has a gate electrically connected to the node **186**, which is electrically connected to the source of the transistor **165**. The transistor **173** has a source electrically connected to the drain of the transistor **171**, and a drain electrically connected to a source of the transistor **143**. The transistor **174** in this example has a gate electrically connected to a node **187**, which is electrically connected to the source of the transistor **173** and electrically connected to the drain of the transistor **171**. The transistor **174** has a source electrically connected to the drain of the transistor **172**, and a drain electrically connected to a power supply pin VDD **103** which has a positive power supply voltage 6V.

[0034] The transistor **143** in this example has a gate electrically connected to its own drain (i.e., diode-connected to act like a rectifier or diode), which is electrically connected to the power supply pin VDD **103** which has a positive power supply voltage 6V. Source of the transistor **143** is electrically connected to the drain of the transistor **173**. The stage **130** further includes a capacitor **123** coupled between a node **189** electrically connected to the source of the transistor **143** and a node **188** electrically connected to the source of the transistor **174**.

[0035] As such, the stages **110**, **120**, **130** are serially connected to form a multi-stage driver that drives the power switch HEMT **175**. In one embodiment, the power switch HEMT **175** is a high voltage enhancement-mode high electron mobility transistor (HV E-HEMT) **193**. As shown in FIG. **1**, the power switch HEMT **175** has a gate electrically connected to the node **188**, a source electrically connected to ground Vss **112** which has a ground voltage 0V, and a drain electrically connected to an output pin **133** of the circuit **100**. In some embodiments, the circuit **100** can serve as a low-side driver in a half-bridge or full-bridge power converter, where the output pin **133** serves as a low-side voltage output (LoVout).

[0036] Most transistors in FIG. **1** are enhancement-mode N-type transistors. That is, the circuit **100** uses mostly enhancement-mode N-type transistors as pull-up devices to minimize static current. In order to achieve near full-rail pull-up voltage and fast slew rate, a significantly large over-drive voltage is needed for the N-Type enhancement-mode transistor. That is, the voltage difference between gate and source (Vgs) should be much larger than the threshold voltage (Vt), i.e., (Vgs−Vt>>0). While the multi-stage driver of the circuit **100** can minimize static current, each stage of E-HEMT pull-up device consumes at least one Vt voltage drop.

[0037] As discussed above, the node **181** has a voltage ranged between Vss and VDD (0 and 6V). When the circuit **100** is turned off, the Vin is 0, such that the transistor **153** is turned off and the transistor **156** is turned on. The node **181** has the same voltage 6V as the power supply pin VDD **101**, which enables the transistors **161**, **162**, **163** to be turned on. As such, the node **185** is electrically connected to the ground Vss **111**, and has a voltage close to 0V. As such, the transistor **165** is turned off, and the node **186** is electrically connected to the ground Vss **111** and has a voltage 0V. Accordingly, the transistor **166** is turned off, and the node **183** is electrically connected to the ground Vss **111** and has a voltage 0V. In this case, the capacitor **122** is charged by the power supply pin VDD **102** via the transistor **142**. In this example, the transistor **142** is a diode-connected HEMT used as a rectifying diode, which naturally has a forward voltage (Vf). That is, the voltage at the node **184** will maximally be charged to 6V−Vf. In a first example, assuming the forward voltages and threshold voltages of all transistors in FIG. **1** are equal to 1.5V, the maximum voltage at the node **184** when the circuit **100** is turned off is 6V−1.5V=4.5V.

[0038] When the circuit **100** is turned on and the Vin has a voltage of 6V, the transistor **153** is turned on and the transistor **156** is turned off. The node **181** has the same voltage 0V as the ground Vss **111**, which enables the transistors **161**, **162**, **163** to be turned off. As such, the node **185** is electrically connected to the node **184**, and has a same voltage as the node **184**. This induces the transistor **165** to be turned on, which enables the node **186** to be charged by the voltage at the node **184**. This in turn induces the transistor **166** to be turned on, which enables the node **183** to be charged by the power supply pin VDD **102**. As such, the voltage at the node **183** can maximally be charged to 6V, same as the voltage of the power supply pin VDD **102**. Based on the 4.5V voltage difference stored by the capacitor **122** when the circuit **100** is off, the voltage at the node **184** can maximally be charged and increased to 6V+4.5V=10.5V, i.e., the voltage at the node **184** is boot-strapped to 10.5V. Accordingly, the node **185**, which is electrically connected to both the source and the gate of the transistor **164**, is charged to 10.5V as well.

[0039] While the node **186** is also charged by the voltage 10.5V at the node **184**, the voltage of the node **186** cannot reach 10.5V. Because the node **186** is electrically connected to the source of the transistor **165**, to keep the transistor **165** on, the gate source voltage difference Vgs of the transistor **165** must be larger than the threshold voltage (Vt) of the transistor **165**. As it is assumed Vt=1.5V in the first example, the maximum voltage the node **186** can reach in the first example when the circuit **100** is turned on is 10.5V−Vt=10.5V−1.5V=9V. As such, an enhancement-mode high-electron-mobility transistor (E-HEMT) pull-up device consumes at least one Vt voltage drop.

[0040] The node **182** is electrically connected to the node **181** and has a same voltage as that of the node **181**. That is, when the circuit **100** is turned off, the node **182** has the voltage 6V; when the circuit **100** is turned on, the node **182** has the voltage 0V. When the circuit **100** is turned off, the 6V voltage at the node **182** enables the transistors **171**, **172** to be turned on. As such, the node **187** is electrically connected to the ground Vss **111**, and has a voltage 0V. Here, the transistor **173** is turned off due to the 0V voltage at the node **186** when the circuit **100** is turned off as discussed above. Because the node **187** has the voltage 0V, the transistor **174** is turned off, and the node **188** is electrically connected to the ground Vss **111** and has a voltage 0V. In this case, the capacitor **123** is charged by the power supply pin VDD **103** via the transistor **143**. In this example, the transistor **143** is a diode-connected HEMT used as a rectifying diode, which naturally has a forward voltage (Vf). That is, the voltage at the node **189** will maximally be charged to 6V-Vf. In the first example, assuming the forward voltages and threshold voltages of all transistors in FIG. **1** are equal to 1.5V, the maximum voltage at the node **189** when the circuit **100** is turned off is 6V-1.5V=4.5V.

[0041] When the circuit **100** is turned on, the node **182**, like the node **181**, has the same voltage 0V as the ground Vss **111**, which enables the transistors **171**, **172** to be turned off. As discussed above, the node **186**, which is electrically connected to the gate of the transistor **173**, has a maximum voltage of 9V when the circuit **100** is turned on. As such, the transistor **173** is turned on and the node **187** is charged by the node **189**. This induces the transistor **174** to be turned on, which enables the node **188** to be charged by the power supply pin VDD **103**. As such, the voltage at the node **188** can maximally be charged to 6V, same as the voltage of the power supply pin VDD **102**. Based on the 4.5V voltage difference stored by the capacitor **123** when the circuit **100** is off, the voltage at the node **189** can maximally be charged and increased to 6V+4.5V=10.5V, i.e., the voltage at the node **189** is boot-strapped to 10.5V.

[0042] While the node **187** is charged by the voltage 10.5V at the node **189**, the voltage of the node **187** cannot reach 10.5V. Because the node **187** is electrically connected to the source of the transistor **173**, to keep the transistor **173** on, the gate source voltage difference Vgs of the transistor

173 must be larger than the threshold voltage (Vt) of the transistor **173**. The gate of the transistor **173** is electrically connected to the node **186**, which has a maximum voltage 9V when the circuit **100** is turned on. As it is assumed Vt=1.5V in the first example, the maximum voltage the node **187** can reach in the first example when the circuit **100** is turned on is 9V−Vt=9V−1.5V=7.5V. Now the transistor **174** has a gate source voltage difference Vgs=7.5V−6V=1.5V, which is exactly equal to the threshold voltage Vt=1.5V of the transistor **174**. This leaves no voltage margin at the last stage of the multi-stage boot-strapped driver. That is, in the first example where Vf=Vt=1.5V, there is not enough over-drive voltage to drive the power switch HEMT **175**. Even if the power switch HEMT **175** can be driven, it would be significantly slow as the current flowing through the transistor **174** and the node **188** would be very slow due to no Vgs margin compared to the Vt. The above conclusion has not even taken into consideration of the Vt variation (e.g., 3-σ variation of 0.5V), which typically exists in all process technologies. After counting the 3-σ variation of 0.5V, the circuit **100**, under the Vt=1.5V assumption, may not be able to drive the power switch HEMT **175** at all.

[0043] In a second example, it is assumed the forward voltages and threshold voltages of all transistors in FIG. **1** are equal to 1V. In this case, when the circuit **100** is turned off, the node **181** has the same voltage 6V, which enables the transistors **161**, **162**, **163** to be turned on. As such, the node **185** is electrically connected to the ground Vss **111** and has a voltage 0V. As such, the transistor **165** is turned off, and the node **186** is electrically connected to the ground Vss **111** and has a voltage 0V. Accordingly, the transistor **166** is turned off, and the node **183** is electrically connected to the ground Vss **111** and has a voltage 0V. The capacitor **122** is charged by the power supply pin VDD **102** via the transistor **142**. Because the transistor **142** is a diode-connected HEMT used as a rectifying diode which naturally has a forward voltage (Vf), the node **184** can have a maximum voltage of 6V−Vf=6V−1V=5V.

[0044] When the circuit **100** is turned on, the node **181** has the same voltage 0V as the ground Vss **111**, which enables the transistors **161**, **162**, **163** to be turned off. As such, the node **185** is electrically connected to the node **184**, and has a same voltage as the node **184**. This induces the transistor **165** to be turned on, which enables the node **186** to be charged by the voltage at the node **184**. This in turn induces the transistor **166** to be turned on, which enables the node **183** to be charged by the power supply pin VDD **102**. As such, the node **183** has a maximum voltage of 6V, same as the voltage of the power supply pin VDD **102**. Based on the 5V voltage difference stored by the capacitor **122** when the circuit **100** is off, the voltage at the node **184** can maximally be charged and increased to 6V+5V=11V, i.e., the voltage at the node **184** is boot-strapped to 11V. Accordingly, the node **185**, which is electrically connected to both the source and the gate of the transistor **164**, is charged to 11V as well. While the node **186** is also charged by the voltage 11V at the node **184**, the voltage of the node **186** cannot reach 11V. Because the node **186** is electrically connected to the source of the transistor **165**, to keep the transistor **165** on, the gate source voltage difference Vgs of the transistor **165** must be larger than the threshold voltage (Vt) of the transistor **165**. As it is assumed Vt=1V in the second example, the maximum voltage the node **186** can reach in the second example when the circuit **100** is turned on is 11V−Vt=11V−1V=10V.

[0045] The node **182** is electrically connected to the node **181** and has a same voltage as that of the node **181**. That is, when the circuit **100** is turned off, the node **182** has the voltage 6V; when the circuit **100** is turned on, the node **182** has the voltage 0V. When the circuit **100** is turned off, the 6V voltage at the node **182** enables the transistors **171**, **172** to be turned on. As such, the node **187** is electrically connected to the ground Vss **111**, and has a voltage 0V. Here, the transistor **173** is turned off due to the 0V voltage at the node **186** when the circuit **100** is turned off as discussed above. Because the node **187** has the voltage 0V, the transistor **174** is turned off, and the node **188** is electrically connected to the ground Vss **111** and has a voltage 0V. In this case, the capacitor **123** is charged by the power supply pin VDD **103** via the transistor **143**. Because the transistor **143** is a diode-connected HEMT used as a rectifying diode which naturally has a forward voltage (Vf), the node **189** has a maximum voltage of 6V−Vf=6V−1V=5V.

[0046] When the circuit **100** is turned on, the node **182**, like the node **181**, has the same voltage 0V as the ground Vss **111**, which enables the transistors **171**, **172** to be turned off. As discussed above, the node **186**, which is electrically connected to the gate of the transistor **173**, has a maximum voltage of 10V when the circuit **100** is turned on. As such, the transistor **173** is turned on and the node **187** is charged by the node **189**. This induces the transistor **174** to be turned on, which enables the node **188** to be charged by the power supply pin VDD **103**. As such, the voltage at the node **188** can maximally be charged to 6V, same as the voltage of the power supply pin VDD **103**. Based on the 5V voltage difference stored by the capacitor **123** when the circuit **100** is off, the voltage at the node **189** can maximally be charged and increased to 6V+5V=11V, i.e., the voltage at the node **189** is boot-strapped to 11V.

[0047] While the node **187** is charged by the voltage 11V at the node **189**, the voltage of the node **187** cannot reach 11V. Because the node **187** is electrically connected to the source of the transistor **173**, to keep the transistor **173** on, the gate source voltage difference Vgs of the transistor **173** must be larger than the threshold voltage (Vt) of the transistor **173**. The gate of the transistor **173** is electrically connected to the node **186**, which has a maximum voltage 10V when the circuit **100** is turned on. As it is assumed Vt=1V in the second example, the maximum voltage the node **187** can reach in the second example when the circuit **100** is turned on is 10V−Vt=10V−1V=9V. Now the transistor **174** has a gate source voltage difference Vgs=9V−6V=3V, which is much larger than the threshold voltage Vt=1V of the transistor **174**. This leaves enough voltage margin at the last stage of the multi-stage boot-strapped driver. That is, in the second example where Vf=Vt=1V, there is enough over-drive voltage to drive the power switch HEMT **175**. However, since all transistors, including the power switch HEMT **175**, in FIG. **1** are using a same Vt, a reduced Vt at the power switch HEMT **175** may cause the noise immunity of the power switch HEMT **175** to become significantly worse due to not being able to withstand a large back-feed-through impulse (di/dt) voltage to the gate of the power switch HEMT **175**. Because there is inevitable parasitic capacitance between the drain and the gate of the power switch HEMT **175**, a voltage impulse will feed back from the drain of the power switch HEMT **175** to the gate of the power switch HEMT **175** through the parasitic capacitance. This could accidently turn on the power switch HEMT **175** so long as the noise voltage is larger than the reduced Vt of the power switch HEMT **175**, even when the circuit **100** is turned off.

[0048] As such, in a third example, the forward voltages and threshold voltages of all transistors in FIG. **1** are not all the same. In the third example, it is assumed that the transistors **142**, **143**, **174** have an ultra-low Vt of 0.5V, the transistors **165**, **173** have a low Vt of 1V, while the other transistors in FIG. **1** have a high Vt of 1.5V. In this case, when the circuit **100** is turned off, the node **181** has the same voltage 6V, which enables the transistors **161**, **162**, **163** to be turned on. As such, the node **185** is electrically connected to the ground Vss **111** and has a voltage 0V. As such, the transistor **165** is turned off, and the node **186** is electrically connected to the ground Vss **111** and has a voltage 0V. Accordingly, the transistor **166** is turned off, and the node **183** is electrically connected to the ground Vss **111** and has a voltage 0V. The capacitor **122** is charged by the power supply pin VDD **102** via the transistor **142**. Because the transistor **142** has a forward voltage Vf equal to its Vt, the node **184** can have a maximum voltage of 6V−Vf=6V−0.5V=5.5V.

[0049] When the circuit **100** is turned on, the node **181** has the same voltage 0V as the ground Vss **111**, which enables the transistors **161**, **162**, **163** to be turned off. As such, the node **185** is electrically connected to the node **184**, and has a same voltage as the node **184**. This induces the transistor **165** to be turned on, which enables the node **186** to be charged by the voltage at the node **184**. This in turn induces the transistor **166** to be turned on, which enables the node **183** to be charged by the power supply pin VDD **102**. As such, the node **183** has a maximum voltage of 6V, same as the voltage of the power supply pin VDD **102**. Based on the 5.5V voltage difference stored by the capacitor **122** when the circuit **100** is off, the voltage at the node **184** can maximally be charged and increased to 6V+5.5V=11.5V, i.e., the voltage at the node **184** is boot-strapped to 11.5V. Accordingly, the node **185**, which is electrically connected to both the source and the gate of the transistor **164**, is charged to 11.5V as well. While the node **186** is also charged by the voltage 11.5V at the node **184**, the voltage of the node **186** cannot reach 11.5V. Because the node **186** is electrically connected to the source of the transistor **165**, to keep the transistor **165** on, the gate source voltage difference Vgs of the transistor **165** must be larger than the Vt=1V of the transistor **165**. So the maximum voltage the node **186** can reach in the third example when the circuit **100** is turned on is 11.5V−1V=10.5V.

[0050] The node **182** is electrically connected to the node **181** and has a same voltage as that of the node **181**. That is, when the circuit **100** is turned off, the node **182** has the voltage 6V; when the circuit **100** is turned on, the node **182** has the voltage 0V. When the circuit **100** is turned off, the 6V voltage at the node **182** enables the transistors **171**, **172** to be turned on. As such, the node **187** is electrically connected to the ground Vss **111**, and has a voltage 0V. Here, the transistor **173** is turned off due to the 0V voltage at the node **186** when the circuit **100** is turned off as discussed above. Because the node **187** has the voltage 0V, the transistor **174** is turned off, and the node **188** is electrically connected to the ground Vss **111** and has a voltage 0V. In this case, the capacitor **123** is charged by the power supply pin VDD **103** via the diode-connected transistor **143**. Because the diode-connected transistor **143** has a forward voltage Vf equal to its Vt, the node **189** has a maximum voltage of 6V−Vf=6V−0.5V=5.5V.

[0051] When the circuit **100** is turned on, the node **182**, like the node **181**, has the same voltage 0V as the ground Vss **111**, which enables the transistors **171**, **172** to be turned off. As discussed above, the node **186**, which is electrically connected to the gate of the transistor **173**, has a maximum voltage of 10.5V when the circuit **100** is turned on. As such, the transistor **173** is turned on and the node **187** is charged by the node **189**. This induces the transistor **174** to be turned on, which enables the node **188** to be charged by the power supply pin VDD **103**. As such, the voltage at the node **188** can maximally be charged to 6V, same as the voltage of the power supply pin VDD **102**. Based on the 5.5V voltage difference stored by the capacitor **123** when the circuit **100** is off, the voltage at the node **189** can maximally be charged and increased to 6V+5.5V=11.5V, i.e., the voltage at the node **189** is boot-strapped to 11.5V.

[0052] While the node **187** is charged by the voltage 11.5V at the node **189**, the voltage of the node **187** cannot reach 11.5V. Because the node **187** is electrically connected to the source of the transistor **173**, to keep the transistor **173** on, the gate source voltage difference Vgs of the transistor **173** must be larger than the threshold voltage Vt=1V of the transistor **173**. Because the gate of the transistor **173** is electrically connected to the node **186**, which has a maximum voltage 10.5V when the circuit **100** is turned on, the maximum voltage the node **187** can reach in the third example when the circuit **100** is turned on is 10.5V−Vt=10.5V−1V=9.5V. Now the transistor **174** has a gate source voltage difference Vgs=9.5V−6V=3.5V, which is much larger than the threshold voltage Vt=0.5V of the transistor **174**. This leaves enough voltage margin at the last stage of the multi-stage boot-strapped driver. That is, in the third example, there is enough over-drive voltage to drive the power switch HEMT **175**. In addition, since the power switch HEMT **175** has a larger Vt=1.5V, the noise immunity of the power switch HEMT **175** will be better than the second example, because a larger Vt of the power switch HEMT **175** can significantly withstand impulse voltage noise fed back from the drain of the power switch HEMT **175** to the gate of the power switch HEMT **175**. In various embodiments, the power switch HEMT **175** may have an even larger Vt like 2V. The disclosed circuit design for multi-Vt transistors can reduce Vt of the pull-up E-HEMT transistors and Vf of the diode-connected E-HEMT rectifiers of the multi-stage driver to provide enough over-drive voltage and dramatically reduce static current, without compromising the noise immunity of the output power switch. To manufacture multi-Vt transistors in a same IC on a same wafer, the transistors may be different in terms of: different gate materials (e.g. tungsten, nickel), different p-type doping materials (e.g. magnesium, beryllium) in corresponding polarization modulation portions, different thicknesses of corresponding active portions, different material compositions (e.g. aluminum compositions) of corresponding active portions, and/or different material structures (e.g. homogeneous or graded) of corresponding active portions.

[0053] FIG. **2**A illustrates a cross-sectional view of an exemplary semiconductor device **200-1** including transistors with different threshold voltages, in accordance with some embodiments of the present disclosure. As shown in FIG. **2**A, the semiconductor device **200-1** in this example includes a silicon layer **210** and a transition layer **220** disposed on the silicon layer **210**. The semiconductor device **200-1** further includes a first layer **230** comprising a first III-V semiconductor material formed over the transition layer **220**.

[0054] The semiconductor device **200-1** further includes a second layer **240** (a polarization layer) comprising a second III-V semiconductor material disposed on the first layer **230**. The second III-V semiconductor material is different from the first III-V semiconductor material. For example, the first III-V semiconductor material may be gallium nitride (GaN); while the second III-V semiconductor material may be aluminum gallium nitride (AlGaN).

[0055] As shown in FIG. **2**A, the semiconductor device **200-1** further includes a first transistor **201** and a second transistor **202** formed over the first layer **230**. The first transistor **201** comprises a first gate structure **251** comprising a first material, a first source region **281** and a first drain region **291**. The second transistor **202** comprises a second gate structure **252** comprising a second material, a second source region **282** and a second drain region **292**. According to various embodiments, the first material is different from the second material.

[0056] The semiconductor device **200-1** further includes a polarization modulation layer **241**, **242** disposed on the second layer **240**, and a passivation layer **250** disposed partially on the polarization modulation layer and partially on the second layer **240**. In one embodiment, the polarization modulation layer comprises p-type doped GaN (pGaN).

[0057] The source regions **281**, **282** and the drain regions **291**, **292** of the two transistors **201**, **202** are formed through the second layer **240** and the passivation layer **250**, and disposed on the first layer **230**. The first gate structure **251** is disposed on the pGaN portion **241** and between the first source region **281** and the first drain region **291**. The second gate structure **252** is disposed on the pGaN portion **242** and between the second source region **282** and the second drain region **292**.

[0058] In one embodiment, the first transistor **201** and the second transistor **202** are high electron mobility transistors to be used in a same multi-stage driver circuit. For example, the first transistor **201** is used as a power switch transistor and has a first threshold voltage. The second transistor **202** is used as a driver transistor and has a second threshold voltage that is lower than the first threshold voltage. Accordingly, the first material of the first gate structure **251** has a lower work-function than the second material of the second gate structure **252**. For example, the first material comprises tungsten (W) and/or a titanium/tungsten/titanium-nitride (Ti/W/TiN) metal stack; and the second material comprises nickel (Ni) and/or a titanium/nickel/titanium-nitride (Ti/Ni/TiN) metal stack.

[0059] In addition, the semiconductor device **200-1** includes an interlayer dielectric (ILD) layer **260** disposed partially on the passivation layer **250** and partially on the first transistor **201** and the second transistor **202**. The semiconductor device **200-1** also includes metal contacts **271** disposed on and in contact with the source regions **281**, **282** and the drain regions **291**, **292** respectively, and includes a first metal layer **272** on the metal contacts **271**.

[0060] FIG. **2**B illustrates a cross-sectional view of an exemplary semiconductor device **200-2** including transistors with different threshold voltages, in accordance with some embodiments of the present disclosure. The semiconductor device **200-2** in FIG. **2**B is similar to the semiconductor device **200-1** in FIG. **2**A, except that the metal gates of the first transistor **201** and the second transistor **202** in the semiconductor device **200-2** has a same gate material. As shown in FIG. **2**B, the first pGaN portion **241** of the first transistor **201** in this example includes a different p-type doping material from that in the second pGaN portion **242** of the second transistor **202**.

[0061] In one embodiment, the first transistor **201** and the second transistor **202** are high electron mobility transistors to be used in a same multi-stage driver circuit. For example, the first transistor **201** is used as a power switch transistor and has a first threshold voltage. The second transistor **202** is used as a driver transistor and has a second threshold voltage that is lower than the first threshold voltage. Accordingly, the p-type doping material of the first polarization modulation portion **241** has a higher (larger) work-function than the p-type doping material of the second polarization modulation portion **242**. For example, the first polarization modulation portion **241** is doped with Be, while the second polarization modulation portion **242** is doped with Mg.

[0062] FIG. **2**C illustrates a cross-sectional view of an exemplary semiconductor device **200-3** including transistors with different threshold voltages, in accordance with some embodiments of the present disclosure. The semiconductor device **200-3** in FIG. **2**C is similar to the semiconductor device **200-1** in FIG. **2**A, except that the metal gates of the first transistor **201** and the second transistor **202** in the semiconductor device **200-2** have a same gate material. As shown in FIG. **2**C, the active AlGaN portions **231**, **232** in the semiconductor device **200-3** under the first transistor **201** and the second transistor **202** have different Al compositions. As shown in FIG. **2**C, the active AlGaN layer in this example includes a first active portion **231** under the gate of the first transistor **201** and a second active portion **232** under the gate of the second transistor **202**. The first active portion **231** has a different Al composition (x) from the Al composition (y) of the second active portion **232**.

[0063] In one embodiment, the first transistor **201** and the second transistor **202** are high electron mobility transistors to be used in a same multi-stage driver circuit. For example, the second transistor **202** is used as a power switch transistor and has a first threshold voltage. The first transistor **201** is used as a driver transistor and has a second threshold voltage that is lower than the first threshold voltage. Accordingly, the first active portion **231** under the gate of the first transistor **201** has a higher Al composition than the second active portion **232** under the gate of the second transistor **202** to introduce a higher polarization.

[0064] FIG. **2**D illustrates a cross-sectional view of an exemplary semiconductor device **200-4** including transistors with different threshold voltages, in accordance with some embodiments of the present disclosure. The semiconductor device **200-4** in FIG. **2**D is similar to the semiconductor device **200-1** in FIG. **2**A, except that the metal gates of the first transistor **201** and the second transistor **202** in the semiconductor device **200-2** has a same gate material. As shown in FIG. **2**D, the active AlGaN portions **233**, **234** in the semiconductor device **200-3** under the first transistor **201** and the second transistor **202** have different thicknesses. As shown in FIG. **2**D, the active AlGaN layer in this example includes a first active portion **233** under the gate of the first transistor **201** and a second active portion **234** under the gate of the second transistor **202**. The first active portion **233** is thicker than the second active portion **234**.

[0065] In one embodiment, the first transistor **201** and the second transistor **202** are high electron mobility transistors to be used in a same multi-stage driver circuit. For example, the second transistor **202** is used as a power switch transistor and has a first threshold voltage. The first transistor **201** is used as a driver transistor and has a second threshold voltage that is lower than the first threshold voltage. Accordingly, the first active portion **233** under the gate of the first transistor **201** is thicker than the second active portion **234** under the gate of the second transistor **202** to introduce a higher polarization.

[0066] FIG. **2**E illustrates a cross-sectional view of an exemplary semiconductor device **200-5** including transistors with different threshold voltages, in accordance with some embodiments of the present disclosure. The semiconductor device **200-5** in FIG. **2**E is similar to the semiconductor device **200-1** in FIG. **2**A, except that the metal gates of the first transistor **201** and the second transistor **202** in the semiconductor device **200-2** has a same gate material. The active AlGaN portions **235**, **236** in the semiconductor device **200-5** under the first transistor **201** and the second transistor **202** have different material structures. As shown in FIG. **2**E, the active AlGaN layer in this example includes a first active portion **235** under the gate of the first transistor **201** and a second active portion **236** under the gate of the second transistor **202**. While the first active portion **235** has a homogeneous structure that comprises AlGaN with a single constant Al proportion, the second active portion **236** has graded structure that includes a plurality of sub-layers each of which comprises AlGaN with a different Al proportion. In one embodiment, the first transistor **201** and the second transistor **202** are high electron mobility transistors to be used in a same multi-stage driver circuit. For example, the second transistor **202** is used as a power switch transistor and has a first threshold voltage. The first transistor **201** is used as a driver transistor and has a second threshold voltage that is lower than the first threshold voltage.

[0067] In some embodiments, the aluminum composition in the second active portion **236** goes from low to high from its bottom, when the first III-V semiconductor material is GaN in the first layer **230** and when the second III-V semiconductor material is Al.sub.xGa.sub.1-xN in the second active portion **236**. For example, x=0% at the interface between the second active portion **236** and the first layer **230**. Then x is increased gradually from 0% to e.g., ˜50% for the second active portion **236**. The graded Al.sub.xGa.sub.1-xN layer can significantly conform (pseudomorphic) to the GaN layer to get a virtually misfit-dislocation-free (and threading-dislocation-free) Al.sub.xGa.sub.1-xN/GaN interface as a result in trap free.

[0068] FIG. **2**F illustrates a cross-sectional view of an exemplary semiconductor device **200-6** including transistors with different threshold voltages, in accordance with some embodiments of the present disclosure. The semiconductor device **200-6** in FIG. **2**F is similar to the semiconductor device **200-2** in FIG. **2**B, except that: in addition to the p-type doping material difference in the pGaN portions **241**, **242**, the active AlGaN portions **237**, **238** in the semiconductor device **200-6** under the first transistor **201** and the second transistor **202** have different thicknesses and different material structures. As shown in FIG. **2**F, the active AlGaN layer in this example includes a first active portion **237** under the gate of the first transistor **201** and a second active portion **238** under the gate of the second transistor **202**. While the first active portion **237** has a homogeneous structure that comprises AlGaN with a single constant Al proportion, the second active portion **238** has graded structure that includes a plurality of sub-layers each of which comprises AlGaN with a different Al proportion. In addition, the second active portion **238** is thinner than the first active portion **237**. In one embodiment, the first transistor **201** and the second transistor **202** are high electron mobility transistors to be used in a same multi-stage driver circuit. For example, the second transistor **202** is used as a power switch transistor and has a first threshold voltage. The first transistor **201** is used as a driver transistor and has a second threshold voltage that is lower than the first threshold voltage.

[0069] FIGS. **3**A, **3**B, **3**C, **3**D, **3**E, **3**F, **3**G, **3**H, **3**I, **3**J, **3**K, **3**L, **3**M, **3**N, **3**O, **3**P, and **3**Q illustrate cross-sectional views of an exemplary semiconductor device during various fabrication stages, in accordance with some embodiments of the present disclosure. In some embodiments, the semiconductor device may be included in an integrated circuit (IC). In addition, FIGS. **3**A through **3**Q are simplified for a better understanding of the concepts of the present disclosure. For example, although the figures illustrate two transistors, it is understood the semiconductor device may include more than two transistors, and the IC may include a number of other devices comprising resistors, capacitors, inductors, fuses, etc., which are not shown in FIGS. **3**A through **3**Q, for purposes of clarity of illustration.

[0070] FIG. **3**A is a cross-sectional view of the semiconductor device including a substrate **310**, which is provided at one of the various stages of fabrication, according to some embodiments of the present disclosure. The substrate **310** may be formed of silicon, as shown in FIG. **3**A, or another semiconductor material.

[0071] FIG. **3**B is a cross-sectional view of the semiconductor device including a transition or buffer layer **320**, which is formed on the substrate **310** at one of the various stages of fabrication, according to some embodiments of the present disclosure. The transition or buffer layer **320** may be formed by epitaxial growth. According to various embodiments, the transition or buffer layer

320 includes a nucleation layer of aluminum nitride (AlN) and serves as a buffer to reduce the stress between the substrate **310** and the layer on top of the transition or buffer layer **320**. In one embodiment, the transition or buffer layer **320** and the operation step shown in FIG. **3**B is optional and can be removed.

[0072] FIG. **3**C is a cross-sectional view of the semiconductor device including a first III-V semiconductor material layer **330**, which is formed optionally on the transition or buffer layer **320** or directly on the substrate **310** at one of the various stages of fabrication, according to some embodiments of the present disclosure. The first III-V semiconductor material layer **330** may be formed by epitaxial growth. According to various embodiments, the first III-V semiconductor material layer **330** includes a gallium nitride (GaN). When the first III-V semiconductor material layer **330** is formed on the transition or buffer layer **320**, the transition or buffer layer **320** can reduce the stress between the substrate **310** and the first III-V semiconductor material layer **330**. After transistors are formed over the first III-V semiconductor material layer **330**, the first III-V semiconductor material layer **330** serves as a channel layer for the transistors.

[0073] FIG. **3**D is a cross-sectional view of the semiconductor device including a second III-V semiconductor material layer **331**, which is formed on the first III-V semiconductor material layer **330** at one of the various stages of fabrication, according to some embodiments of the present disclosure. The second III-V semiconductor material layer **331** may be formed by epitaxial growth. According to various embodiments, the second III-V semiconductor material layer **331** includes an aluminum gallium nitride (AlGaN). After transistors are formed over the first III-V semiconductor material layer **330** and the second III-V semiconductor material layer **331**, a two dimensional electron gas (2DEG) will be formed at the interface between the first III-V semiconductor material layer **330** and the second III-V semiconductor material layer **331**.

[0074] FIG. **3**E is a cross-sectional view of the semiconductor device including a third III-V semiconductor material layer **332**, which is formed on a portion of the second III-V semiconductor material layer **331** with a mask **335** at one of the various stages of fabrication, according to some embodiments of the present disclosure. The third III-V semiconductor material layer **332** may be formed by epitaxial growth. According to various embodiments, the third III-V semiconductor material layer **332** includes an aluminum gallium nitride (AlGaN). That is, while the second III-V semiconductor material layer **331** is a first AlGaN layer on the GaN layer **330**, the third III-V semiconductor material layer **332** is a second AlGaN layer on the GaN layer **330**. As shown in FIG. **3**E, with the mask **335** covering the right portion of the first AlGaN layer **331**, the second AlGaN layer **332** is disposed on the left and middle portions of the first AlGaN layer **331**, i.e., disposed over the left and middle portions of the first III-V semiconductor material layer **330**. In this example, the second AlGaN layer **332** has a same Al composition as the first AlGaN layer **331**.

[0075] FIG. **3**F is a cross-sectional view of the semiconductor device, where the mask **335** is removed from the first AlGaN layer **331** after the second AlGaN layer **332** is formed, at one of the various stages of fabrication, according to some embodiments of the present disclosure. After the mask **335** is removed, the AlGaN layer on the GaN layer **330** has different thicknesses at different locations of the wafer. In particular, the left and middle portions of the AlGaN layer are thicker than the right portion of the AlGaN layer.

[0076] FIG. **3**G is a cross-sectional view of the semiconductor device including a p-type doped GaN (pGaN) layer **341**, **342**, **343** which is formed on the AlGaN layers **331**, **332** at one of the various stages of fabrication, according to some embodiments of the present disclosure. The pGaN layer **341**, **342**, **343** is patterned to form island regions shown in FIG. **3**G. The patterning of the pGaN layer includes, e.g., (i) forming a masking layer (e.g., photoresist, etc.) over the pGaN layer, the masking layer including openings over the portions of the pGaN layer that are to be removed, and (ii) removing the portions of the pGaN layer that are left exposed by the masking layer (e.g., via a wet or dry etch procedure). The pGaN layer **341**, **342**, **343** may be called a polarization modulation layer, which modulates the dipole concentration in the AlGaN layers **331**, **332** to result

in changing the 2DEG concentration in the AlGaN/GaN interface channel. While the polarization modulation layer is formed for an enhancement-mode (normally off) AlGaN/GaN HEMT, the polarization modulation layer is not needed in a depletion-mode (normally on) AlGaN/GaN HEMT.
[0077] FIG. **3**H is a cross-sectional view of the semiconductor device including a passivation layer **350**, which is formed on the AlGaN layers **331**, **332**, and the polarization modulation layer at one of the various stages of fabrication, according to some embodiments of the present disclosure. The passivation layer **350** is formed over the AlGaN layers **331**, **332** and over the remaining portions of the polarization modulation layer **341**, **342**, **343**. According to various embodiments, the passivation layer **350** is formed using a deposition procedure (e.g., chemical deposition, physical deposition, etc.). The passivation layer **350** may comprise silicon oxide, silicon nitride, silicon oxynitride, carbon doped silicon oxide, carbon doped silicon nitride, carbon doped silicon oxynitride, zinc oxide, zirconium oxide, hafnium oxide, titanium oxide, or another suitable material. In one embodiment, after depositing the passivation layer **350**, the passivation layer **350** undergoes a polishing and/or etching procedure. The polishing and/or etching procedure includes, e.g., a chemical-mechanical planarization (CMP) (i.e., chemical-mechanical polishing) process that is used to polish the surface of the passivation layer **350** and remove topographical irregularities.
[0078] FIG. **3**I is a cross-sectional view of the semiconductor device including source and drain contacts **381**, **391**, **382**, **392**, **383**, **393**, which are formed through the AlGaN layers **331**, **332**, and the passivation layer **350** and disposed on the first III-V semiconductor material layer **330** at one of the various stages of fabrication, according to some embodiments of the present disclosure. The source and drain contacts may be formed as non-rectifying electrical junctions, i.e., ohmic contacts.
[0079] FIG. **3**J is a cross-sectional view of the semiconductor device including a mask **355**, which is formed on the passivation layer **350** at one of the various stages of fabrication, according to some embodiments of the present disclosure. At this stage, the mask **355** has a pattern to expose portions of the passivation layer **350** on top of the pGaN portions **341**, **342**. As such, a first opening **357** is formed on the pGaN portion **341** between the first pair of source contact **381** and drain contact **391** by etching the passivation layer **350** with the patterned mask **355**; and a second opening **358** is formed on the pGaN portion **342** between the second pair of source contact **382** and drain contact **392** by etching the passivation layer **350** with the patterned mask **355**.
[0080] FIG. **3**K is a cross-sectional view of the semiconductor device including a first gate **351** and a second gate **352**, which are deposited and polished in the first opening **357** and the second opening **358** respectively at one of the various stages of fabrication, according to some embodiments of the present disclosure. According to various embodiments, the first gate **351** and the second gate **352** may be formed of metal materials like: tungsten (W), nickel (Ni), titanium/tungsten/titanium-nitride (Ti/W/TiN) metal stack, or titanium/nickel/titanium-nitride (Ti/Ni/TiN) metal stack.
[0081] FIG. **3**L is a cross-sectional view of the semiconductor device including the patterned mask **355**, which is formed on the passivation layer **350** at one of the various stages of fabrication, according to some embodiments of the present disclosure. At this stage, the mask **355** has a pattern to expose a portion of the passivation layer **350** on top of the pGaN portion **343**. As such, a third opening **359** is formed on the pGaN portion **343** between a third pair of source contact **383** and drain contact **393** by etching the passivation layer **350** with the patterned mask **355**.
[0082] FIG. **3**M is a cross-sectional view of the semiconductor device including a third gate **353**, which is deposited and polished in the third opening **359** at one of the various stages of fabrication, according to some embodiments of the present disclosure. According to various embodiments, the third gate **353** may be formed of metal materials like: tungsten (W), nickel (Ni), titanium/tungsten/titanium-nitride (Ti/W/TiN) metal stack, or titanium/nickel/titanium-nitride (Ti/Ni/TiN) metal stack. In this example, the third gate **353** has a gate material different from those of the first gate **351** and the second gate **352**.
[0083] FIG. **3**N is a cross-sectional view of the semiconductor device, where the mask **355** is

removed from the passivation layer **350** after the metal gates are formed, at one of the various stages of fabrication, according to some embodiments of the present disclosure. After the mask **355** is removed, each of the source contacts **381**, **382**, **383**, the drain contacts **391**, **392**, **393**, and the gates **351**, **352**, **353** has an exposed portion on top of the passivation layer **350**.

[0084] FIG. **3**O is a cross-sectional view of the semiconductor device including an interlayer dielectric (ILD) layer **360**, which is formed on the passivation layer **350**, at one of the various stages of fabrication, according to some embodiments of the present disclosure. The ILD layer **360** covers the passivation layer **350** and the exposed portions of the source contacts **381**, **382**, **383**, the drain contacts **391**, **392**, **393**, and the gates **351**, **352**, **353** that are formed at the stage shown in FIG. **3**N. The ILD layer **360** is formed of a dielectric material and may be patterned with holes for metal interconnects or contacts for the source and drain contacts **381**, **382**, **383**, **391**, **392**, **393** as well as the gates **351**, **352**, **353**.

[0085] FIG. **3**P is a cross-sectional view of the semiconductor device including metal contacts **371**, each of which is formed on a source or drain contact, at one of the various stages of fabrication, according to some embodiments of the present disclosure. As discussed above, the ILD layer **360** is patterned with holes each of which is on one of the source and drain contacts **381**, **382**, **383**, **391**, **392**, **393**. As such, the metal contacts **371** can be formed in these holes to be in contact with the source and drain contacts **381**, **382**, **383**, **391**, **392**, **393**, respectively.

[0086] FIG. **3**Q is a cross-sectional view of the semiconductor device including a first metal layer **372**, which is formed on the metal contacts **371**, at one of the various stages of fabrication, according to some embodiments of the present disclosure. The first metal layer **372** includes metal material and is formed over the ILD layer **360** and in contact with the metal contacts **371**. As such, among the three transistors formed on the same wafer in FIG. **3**Q, the left and the middle transistors have different gate materials but a same AlGaN portion thickness, while the middle and the right transistors have different AlGaN portion thicknesses but a same gate material.

[0087] FIG. **4**A and FIG. **4**B show a flow chart illustrating an exemplary method **400** for forming a semiconductor device including transistors with different threshold voltages, in accordance with some embodiments of the present disclosure. As shown in FIG. **4**A, at operation **402**, a transition/buffer layer is formed on a semiconductor substrate by epitaxial growth. A GaN layer is formed at operation **404** on the transition/buffer layer by epitaxial growth. At operation **406**, a first Al.sub.xGa.sub.1-xN layer is formed on the GaN layer by epitaxial growth. At operation **408**, a second Al.sub.xGa.sub.1-xN layer is formed with a mask on the first Al.sub.xGa.sub.1-xN layer by epitaxial growth. At operation **410**, the mask on the AlGaN layers is removed. At operation **412**, a polarization modulation layer is deposited and defined on the AlGaN layers. At operation **414**, a passivation layer is deposited and polished on the polarization modulation layer and the AlGaN layers. At operation **415**, source and drain ohmic contacts are formed through the passivation layer and the AlGaN layers. The process then goes to the operation **416** in FIG. **4**B.

[0088] As shown in FIG. **4**B, at operation **416**, first openings of a mask are defined on the polarization modulation layer for a first type of gates. At operation **417**, a first gate material is deposited and polished in the first openings to form the first type of gates. At operation **418**, second openings of a mask are defined on the polarization modulation layer for a second type of gates. At operation **420**, a second gate material is deposited and polished in the second openings to form the second type of gates. At operation **422**, the mask on the passivation layer is removed. At operation **424**, a dielectric layer is deposited and polished on the sources, drains, gates and the passivation layer. Metal contacts are formed and defined at operation **426** on the sources, drains and gates. At operation **428**, a first metal layer is formed and defined on the dielectric layer and the metal contacts. The order of the operations shown in FIG. **4**A and FIG. **4**B may be changed according to different embodiments of the present disclosure.

[0089] In some embodiments, a semiconductor device includes a plurality of transistors on a substrate, each transistor of the plurality of transistors including a source region, a drain region, a gate structure, a polarization modulation portion, and a polarization layer. The polarization modulation portion of each of the plurality of transistors is on the polarization layer, the plurality of transistors includes a first transistor having a first threshold voltage that has a first fixed value, and the plurality of transistors includes a second transistor having a second threshold voltage that has a second fixed value different from the first fixed value.

[0090] In some embodiments, the plurality of transistors includes high electron mobility transistors in a same multi-stage driver circuit. In some embodiments, the plurality of transistors further includes a third transistor, a third threshold voltage of the third transistor has a third fixed value that is lower than the second fixed value, and the second threshold voltage is lower than the first threshold voltage. In some embodiments, the first transistor and the second transistor are different in terms of a first manner selected from a group of manners including: different gate materials, different materials of corresponding polarization modulation portions, different thicknesses of corresponding active portions, different material compositions of corresponding active portions, and different structures of corresponding active portions; and the second transistor and the third transistor are different in terms of a second manner selected from the group of manners, wherein the first manner is different from the second manner. In some embodiments, at least two of the first transistor, the second transistor, and the third transistor are different in terms of at least two manners selected from a group of manners including: different gate materials, different materials of corresponding polarization modulation portions, different thicknesses of corresponding active portions, different material compositions of corresponding active portions, and different structures of corresponding active portions. In some embodiments, the different gate materials are metal materials with different work functions; the different materials of corresponding polarization modulation portions are gallium nitride doped by different p-type doping material selected from column I and column II elements; the different material compositions of corresponding active portions are aluminum gallium nitride with different aluminum proportions; and the different structures of corresponding active portions include: (a) a graded structure that includes a plurality of sub-layers each of which includes aluminum gallium nitride with a different aluminum proportion and (b) a homogeneous structure that includes aluminum gallium nitride with a single constant aluminum proportion. In some embodiments, the semiconductor device further includes a channel layer over the substrate, the polarization layer includes a first active portion corresponding to the first transistor, the polarization layer includes a second active portion corresponding to the second transistor, the channel layer is below the first and second active portions, the channel layer includes a first III-V semiconductor material, and the first and second active portions include a second III-V semiconductor material that is different from the first III-V semiconductor material. In some embodiments, the first III-V semiconductor material includes gallium nitride, the second III-V semiconductor material includes aluminum gallium nitride, and the first and second active portions have different aluminum concentrations.

[0091] In some embodiments, a semiconductor device includes: a first transistor on a substrate, the first transistor including a first source region, a first drain region, a first gate structure, a first polarization modulation portion, and a first polarization layer, wherein the first polarization modulation portion is on the first polarization layer; and a second transistor on the substrate, the second transistor including a second source region, a second drain region, a second gate structure, a second polarization modulation portion, and a second polarization layer, wherein the second polarization modulation portion is on the second polarization layer. The second polarization modulation portion includes a different material from the first polarization modulation portion, the first transistor has a first threshold voltage that has a first fixed value, and the second transistor has a second threshold voltage that has a second fixed value different from the first fixed value.

[0092] In some embodiments, the first and second polarization modulation portions include different doping materials. In some embodiments, a third threshold voltage of the third transistor is a third fixed value that is lower than the second fixed value, and the second threshold voltage is

lower than the first threshold voltage. In some embodiments, at least two of the first transistor, the second transistor, and the third transistor are different in terms of at least two manners selected from a group of manners including: different gate materials, different materials of corresponding polarization modulation portions, different thicknesses of corresponding active portions, different material compositions of corresponding active portions, and different structures of corresponding active portions. In some embodiments, the first transistor is at least one of: a high voltage enhancement-mode high electron mobility transistor, a low voltage enhancement-mode high electron mobility transistor, or a low voltage depletion-mode high electron mobility transistor; and each of the second transistor and the third transistor is a low voltage enhancement-mode high electron mobility transistor. In some embodiments, the first polarization layer and the second polarization layer have a same composition. In some embodiments, the second threshold voltage is lower than the first threshold voltage. In some embodiments, the first and second polarization modulation portions include p-doped gallium nitride having respectively different dopants, and the first and second polarization layers include aluminum gallium nitride. In some embodiments, a first one of the first source region and the first drain region is electrically connected to a ground voltage source; and a second one of the first source region and the first drain region is electrically connected to an output pin.
[0093] In some embodiments, a method of forming a semiconductor device includes: forming a polarization layer on a substrate; forming for each of a first transistor and a second transistor: a source region; a drain region; a gate structure; and a polarization modulation portion. The polarization modulation portion of each of the first and second transistors is formed on the polarization layer, the first transistor is formed to have a first threshold voltage that has a first fixed value, and the second transistor is formed to have a second threshold voltage that has a second fixed value different from the first fixed value.
[0094] In some embodiments, the forming the polarization layer includes: forming a first active portion corresponding to the first transistor and forming a second active portion corresponding to the second transistor, the first active portion is formed to have a graded structure that includes a plurality of sub-layers, and the second active portion is formed to have a homogeneous structure. In some embodiments, the first active portion is formed to include Al.sub.xGa.sub.1-xN, and the second active portion is formed to include Al.sub.yGa.sub.1-yN, x and y being different numbers.
[0095] The foregoing outlines features of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

Claims

1. A semiconductor device comprising: a plurality of transistors on a substrate, each transistor of the plurality of transistors including a source region, a drain region, a gate structure, a polarization modulation portion, and a polarization layer, wherein: the polarization modulation portion of each of the plurality of transistors is on the polarization layer, the plurality of transistors includes a first transistor having a first threshold voltage that has a first fixed value, and the plurality of transistors includes a second transistor having a second threshold voltage that has a second fixed value different from the first fixed value.
2. The semiconductor device of claim 1, wherein the plurality of transistors includes high electron mobility transistors in a same multi-stage driver circuit.

3. The semiconductor device of claim 1, wherein: the plurality of transistors further includes a third transistor, a third threshold voltage of the third transistor has a third fixed value that is lower than the second fixed value, and the second threshold voltage is lower than the first threshold voltage.
4. The semiconductor device of claim 3, wherein: the first transistor and the second transistor are different in terms of a first manner selected from a group of manners including: different gate materials, different materials of corresponding polarization modulation portions, different thicknesses of corresponding active portions, different material compositions of corresponding active portions, and different structures of corresponding active portions; and the second transistor and the third transistor are different in terms of a second manner selected from the group of manners, wherein the first manner is different from the second manner.
5. The semiconductor device of claim 3, wherein: at least two of the first transistor, the second transistor, and the third transistor are different in terms of at least two manners selected from a group of manners including: different gate materials, different materials of corresponding polarization modulation portions, different thicknesses of corresponding active portions, different material compositions of corresponding active portions, and different structures of corresponding active portions.
6. The semiconductor device of claim 5, wherein: the different gate materials are metal materials with different work functions; the different materials of corresponding polarization modulation portions are gallium nitride doped by different p-type doping material selected from column I and column II elements; the different material compositions of corresponding active portions are aluminum gallium nitride with different aluminum proportions; and the different structures of corresponding active portions include: (a) a graded structure that includes a plurality of sub-layers each of which includes aluminum gallium nitride with a different aluminum proportion and (b) a homogeneous structure that includes aluminum gallium nitride with a single constant aluminum proportion.
7. The semiconductor device of claim 1, further comprising a channel layer over the substrate, wherein: the polarization layer includes a first active portion corresponding to the first transistor, the polarization layer includes a second active portion corresponding to the second transistor, the channel layer is below the first and second active portions, the channel layer includes a first III-V semiconductor material, and the first and second active portions include a second III-V semiconductor material that is different from the first III-V semiconductor material.
8. The semiconductor device of claim 7, wherein: the first III-V semiconductor material includes gallium nitride, the second III-V semiconductor material includes aluminum gallium nitride, and the first and second active portions have different aluminum concentrations.
9. A semiconductor device comprising: a first transistor on a substrate, the first transistor including a first source region, a first drain region, a first gate structure, a first polarization modulation portion, and a first polarization layer, wherein the first polarization modulation portion is on the first polarization layer; and a second transistor on the substrate, the second transistor including a second source region, a second drain region, a second gate structure, a second polarization modulation portion, and a second polarization layer, wherein the second polarization modulation portion is on the second polarization layer, wherein: the second polarization modulation portion includes a different material from the first polarization modulation portion, the first transistor has a first threshold voltage that has a first fixed value, and the second transistor has a second threshold voltage that has a second fixed value different from the first fixed value.
10. The semiconductor device of claim 9, wherein: the first and second polarization modulation portions include different doping materials.
11. The semiconductor device of claim 9, further comprising: a third transistor, wherein: a third threshold voltage of the third transistor is a third fixed value that is lower than the second fixed value, and the second threshold voltage is lower than the first threshold voltage.
12. The semiconductor device of claim 11, wherein: at least two of the first transistor, the second

transistor, and the third transistor are different in terms of at least two manners selected from a group of manners including: different gate materials, different materials of corresponding polarization modulation portions, different thicknesses of corresponding active portions, different material compositions of corresponding active portions, and different structures of corresponding active portions.

13. The semiconductor device of claim 11, wherein: the first transistor is at least one of: a high voltage enhancement-mode high electron mobility transistor, a low voltage enhancement-mode high electron mobility transistor, or a low voltage depletion-mode high electron mobility transistor; and each of the second transistor and the third transistor is a low voltage enhancement-mode high electron mobility transistor.

14. The semiconductor device of claim 9, wherein: the first polarization layer and the second polarization layer have a same composition.

15. The semiconductor device of claim 9, wherein: the second threshold voltage is lower than the first threshold voltage.

16. The semiconductor device of claim 9, wherein: the first and second polarization modulation portions include p-doped gallium nitride having respectively different dopants, and the first and second polarization layers include aluminum gallium nitride.

17. The semiconductor device of claim 9, wherein: a first one of the first source region and the first drain region is electrically connected to a ground voltage source; and a second one of the first source region and the first drain region is electrically connected to an output pin.

18. A method of forming a semiconductor device, the method comprising: forming a polarization layer on a substrate; and forming for each of a first transistor and a second transistor: a source region; a drain region; a gate structure; and a polarization modulation portion, wherein: the polarization modulation portion of each of the first and second transistors is formed on the polarization layer, the first transistor is formed to have a first threshold voltage that has a first fixed value, and the second transistor is formed to have a second threshold voltage that has a second fixed value different from the first fixed value.

19. The method of claim 18, wherein: the forming the polarization layer includes: forming a first active portion corresponding to the first transistor and forming a second active portion corresponding to the second transistor, the first active portion is formed to have a graded structure that includes a plurality of sub-layers, and the second active portion is formed to have a homogeneous structure.

20. The method of claim 19, wherein: the first active portion is formed to include Al.sub.xGa.sub.1-xN, and the second active portion is formed to include Al.sub.yGa.sub.1-yN, wherein x and y are different numbers.