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(54) **INTEGRATED CIRCUIT READING DATA AND SEMICONDUCTOR DEVICE INCLUDING THE SAME**

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(57) **ABSTRACT**

Provided is a semiconductor device including: a logic die; and a memory device connected to the logic die, the logic die including: a deserializer configured to output first parallel data based on input data received from the memory device using a first clock signal having a first phase and output second parallel data based on the input data using a second clock signal having a second phase, the first phase differing from the second phase; and a first-in first-out circuit configured to: sample the first parallel data using the second clock signal and store the sampled first parallel data as first sampling data, sample the second parallel data using the second clock signal and store the sampled second parallel data as second sampling data, output the first and second sampling data as first and second output data in response to a rising edge of a memory clock signal.

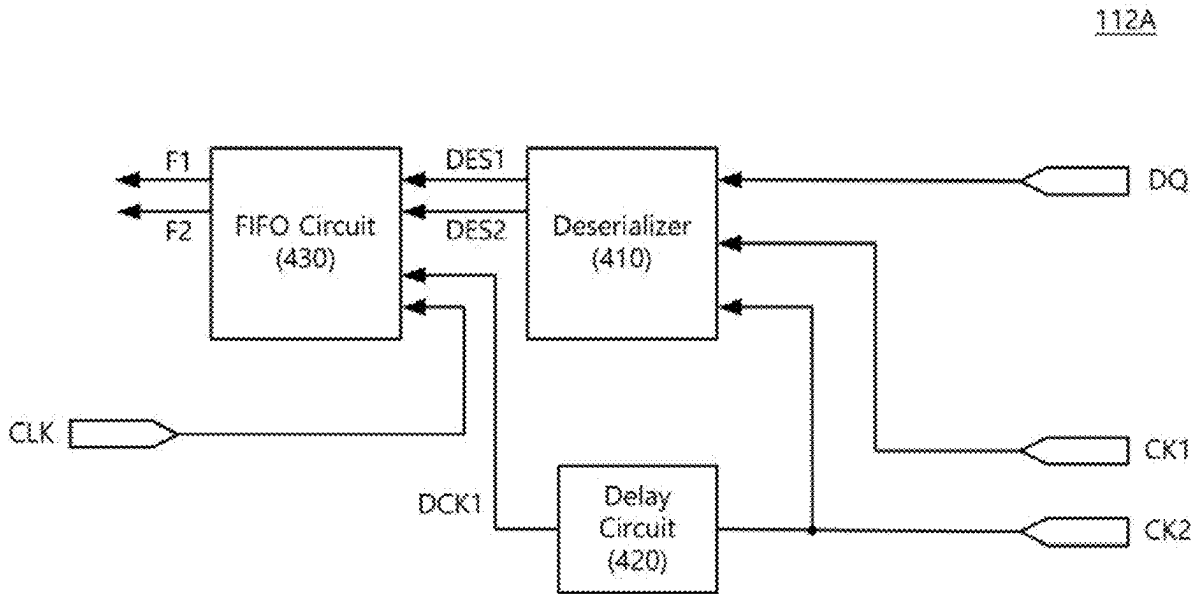


FIG. 1A

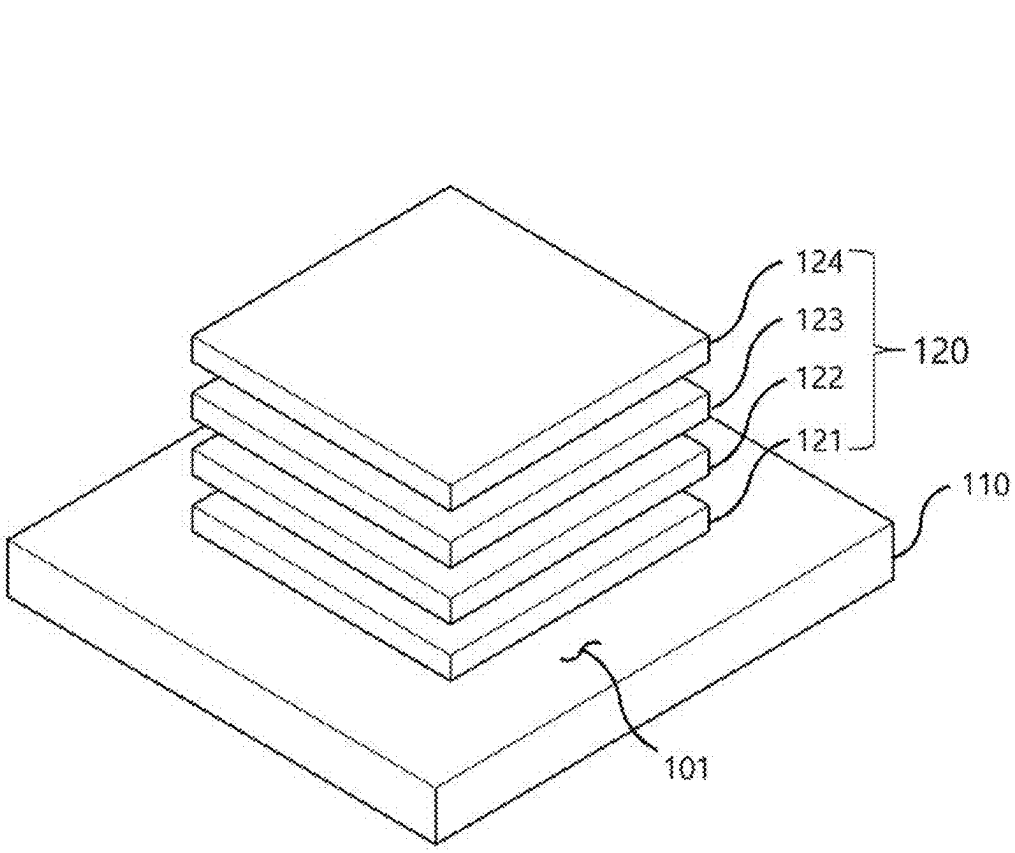


FIG. 1B

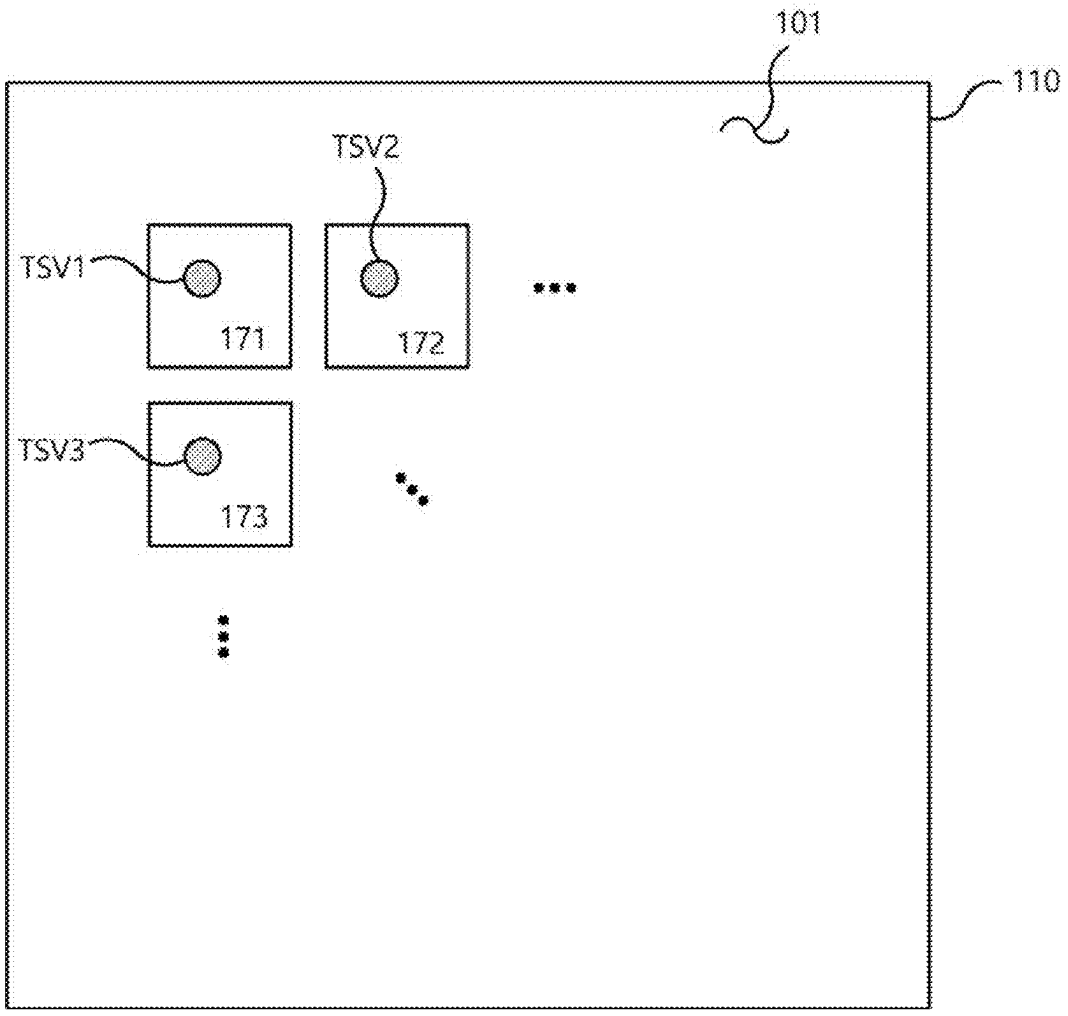


FIG. 1C

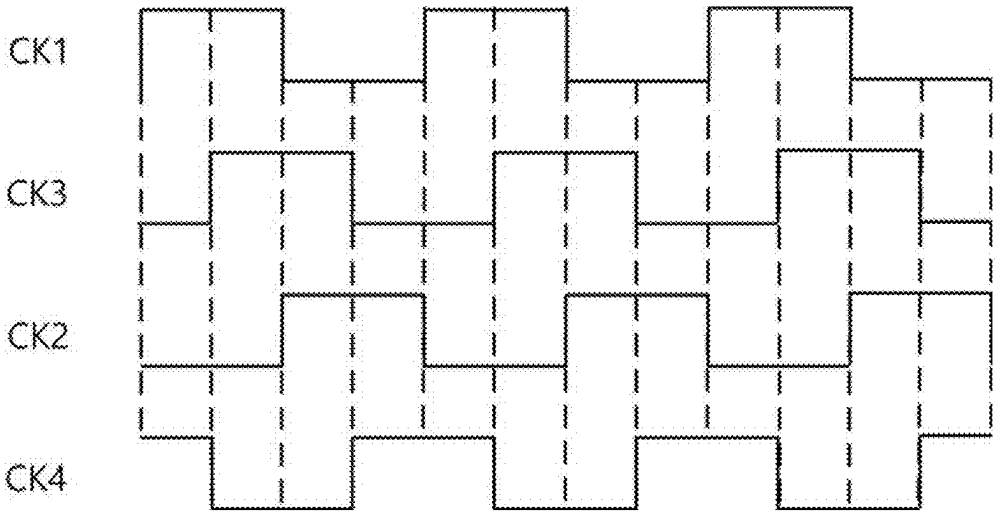


FIG. 2

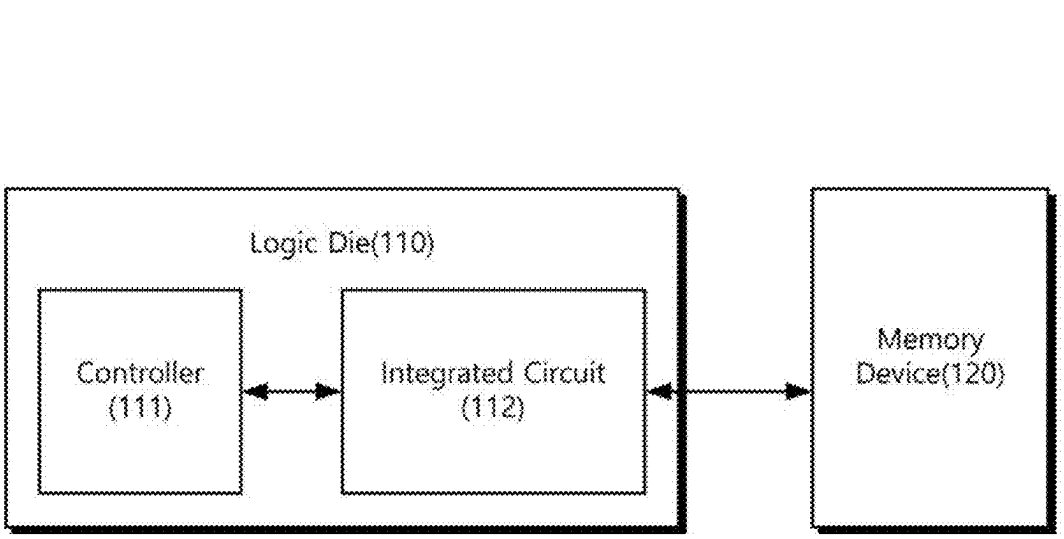

100
Logic Die(110)
Controller
(111)
Integrated Circuit
(112)
Memory
Device(120)

FIG. 3A

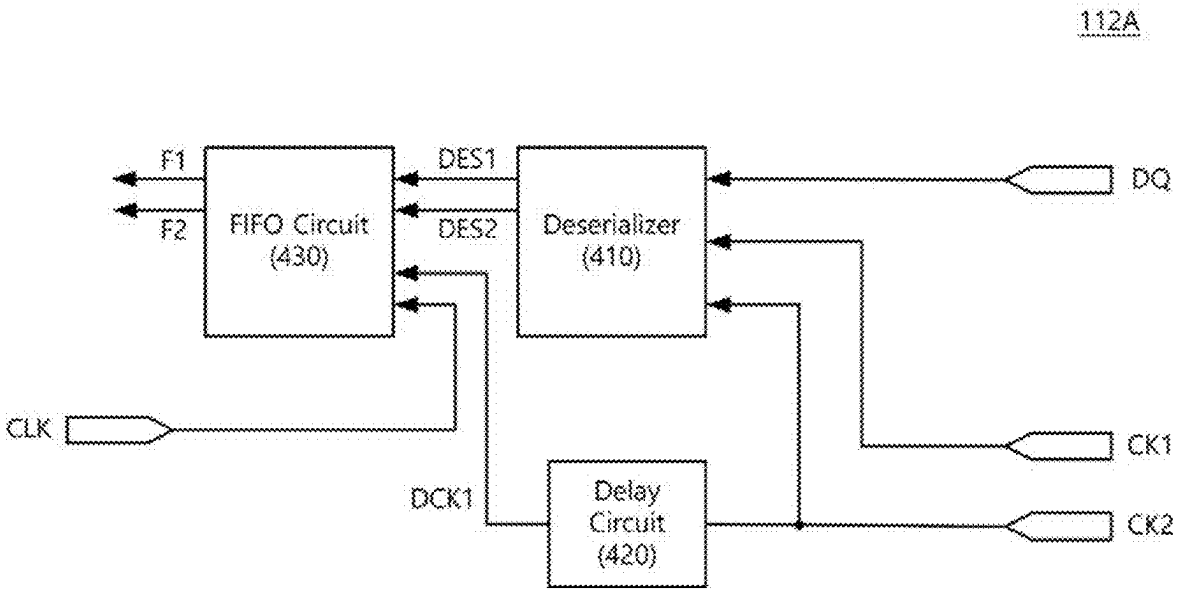

112A
F1
F2
FIFO Circuit
(430)
DES1
DES2
Deserializer
(410)
DQ
CLK
DCK1
Delay
Circuit
(420)
CK1
CK2

FIG. 3B

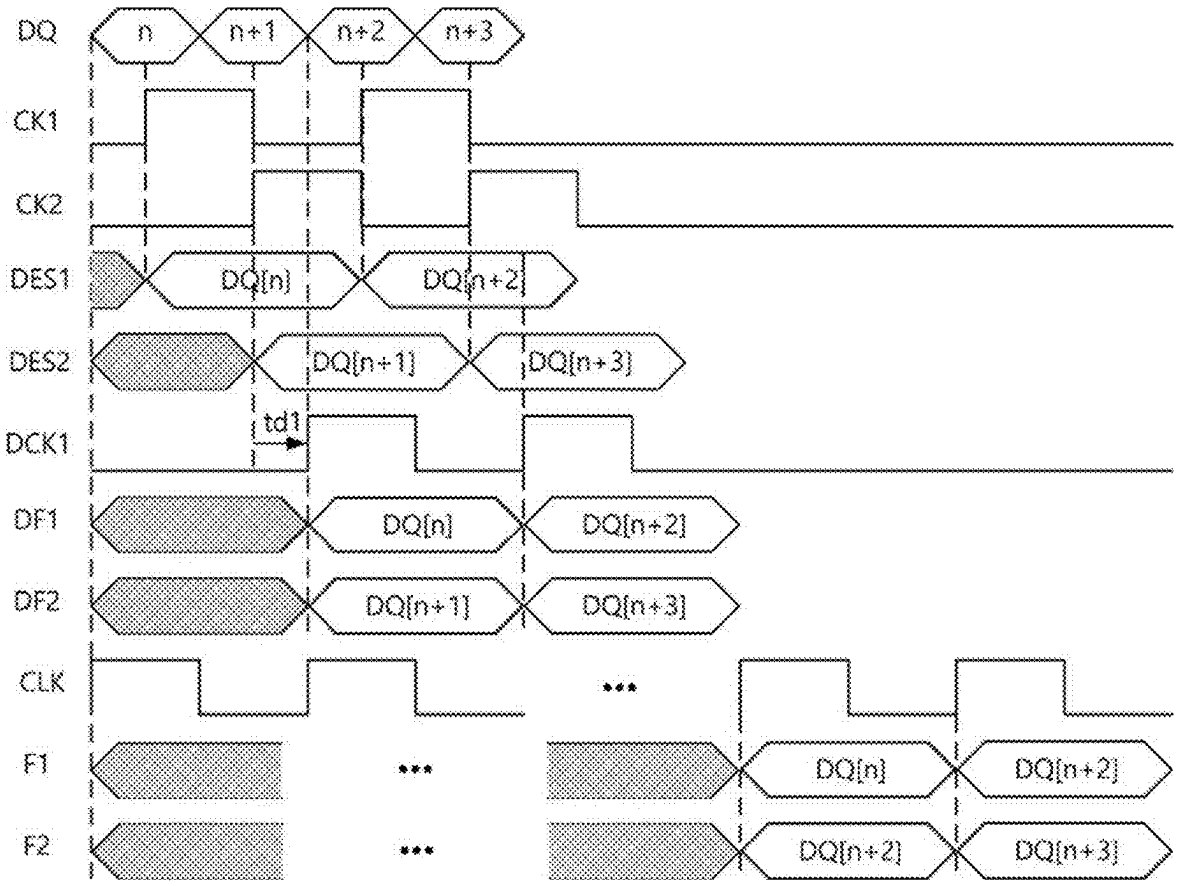

DQ
n
n+1
n+2
n+3
CK1
CK2
DES1
DQ[n]
DQ[n+2]
DES2
DQ[n+1]
DQ[n+3]
DCK1
td1
DF1
DQ[n]
DQ[n+2]
DF2
DQ[n+1]
DQ[n+3]
CLK
F1
DQ[n]
DQ[n+2]
F2
DQ[n+2]
DQ[n+3]

FIG. 4

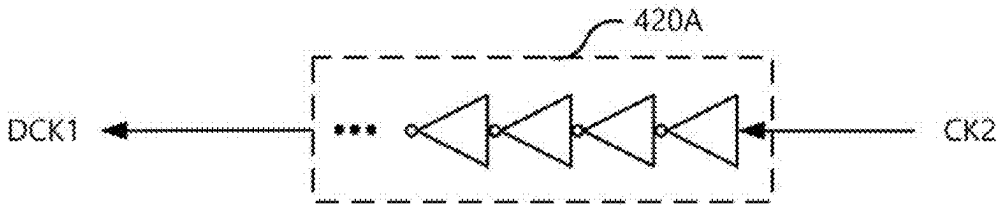


FIG. 5

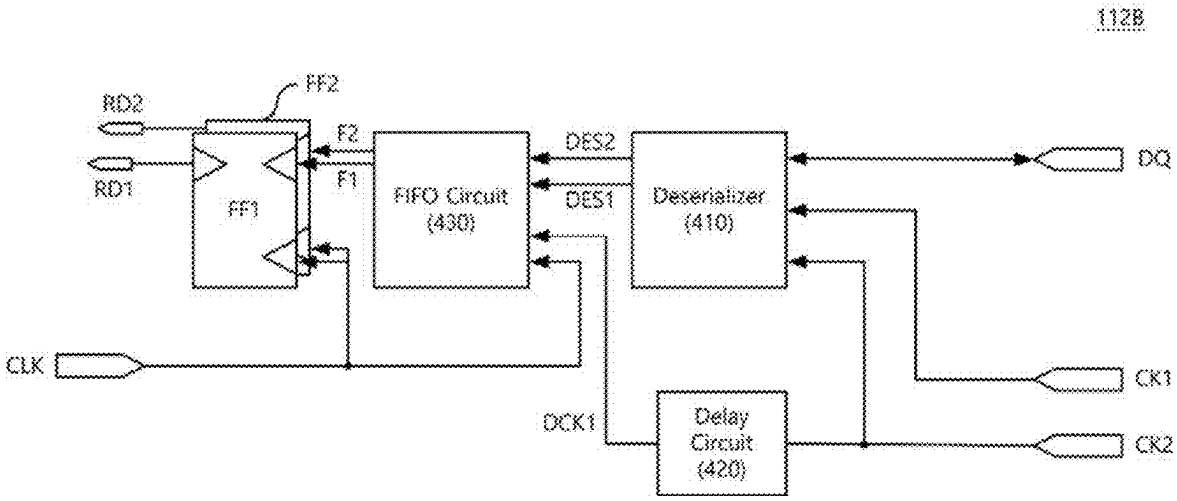

112B
RD2
RD1
FF2
FF1
F2
F1
FIFO Circuit
(430)
DES2
DES1
Deserializer
(410)
DQ
CLK
CK1
DCK1
Delay
Circuit
(420)
CK2

FIG. 6

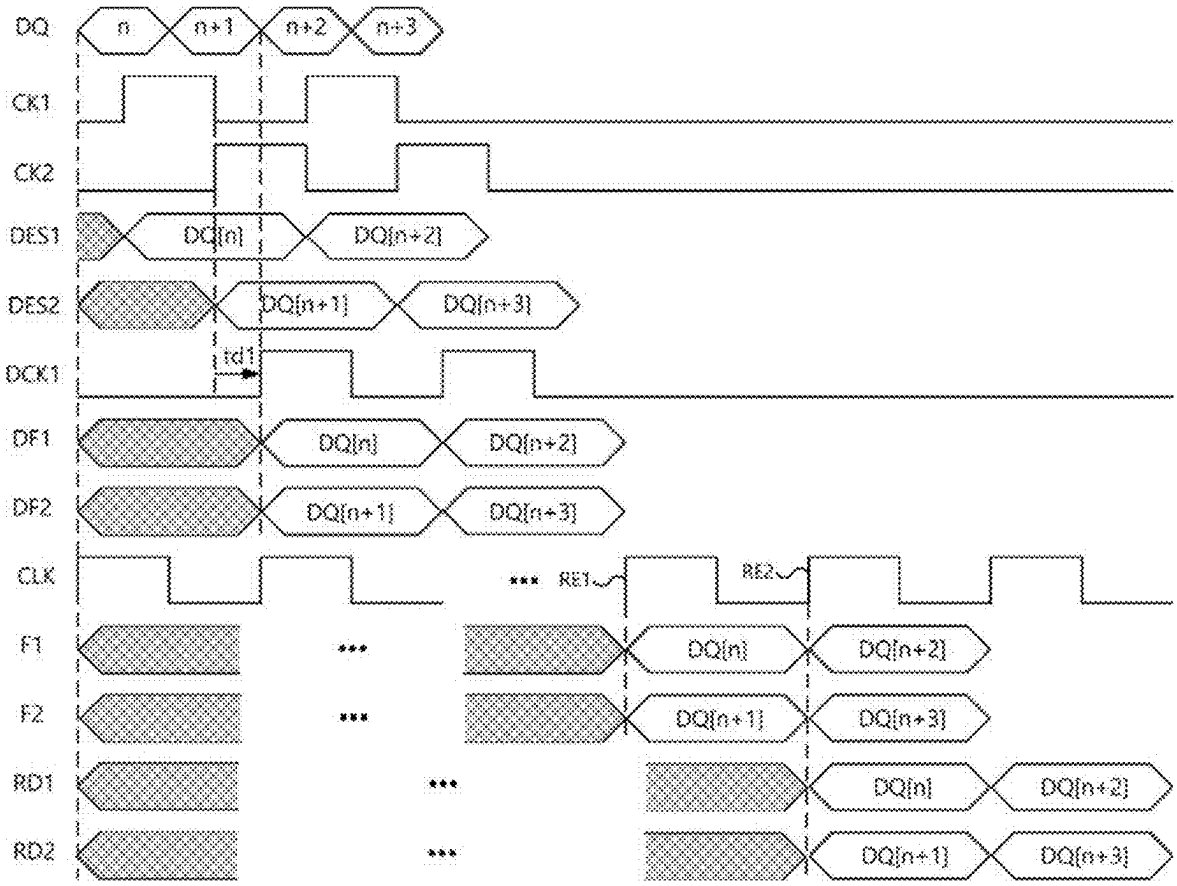

DQ
n
n+1
n+2
n+3
CK1
CK2
DES1
DQ[n]
DQ[n+2]
DES2
DQ[n+1]
DQ[n+3]
DCK1
td1
DF1
DQ[n]
DQ[n+2]
DF2
DQ[n+1]
DQ[n+3]
CLK
RE1
RE2
F1
DQ[n]
DQ[n+2]
F2
DQ[n+1]
DQ[n+3]
RD1
DQ[n]
DQ[n+2]
RD2
DQ[n+1]
DQ[n+3]

FIG. 7A

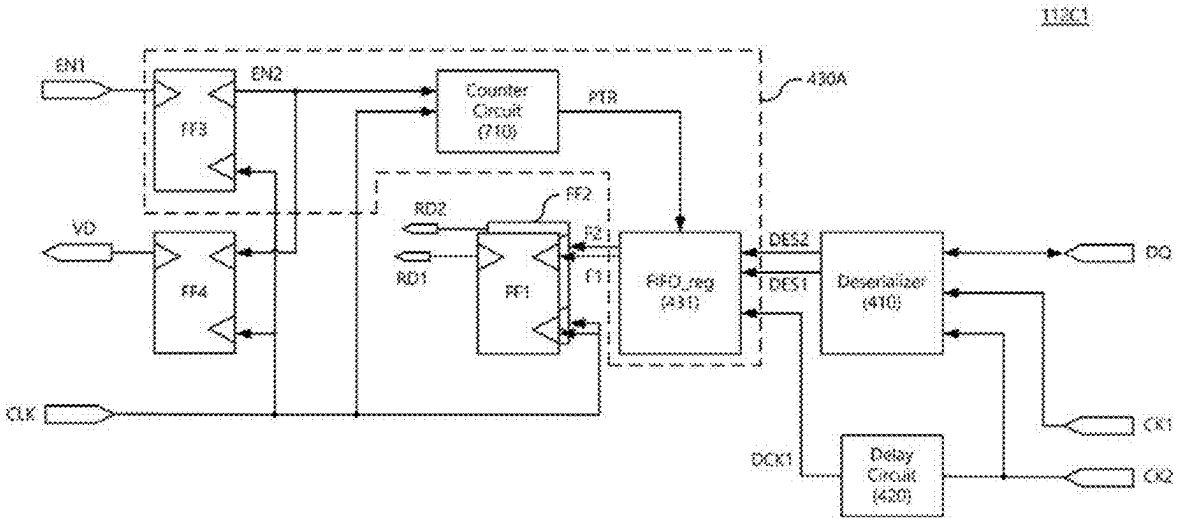

112C1
EN1
EN2
FF3
Counter Circuit (710)
PTR
430A
RD2
FP2
VD
FF4
RD1
FP1
FIFO_reg (431)
DES2
DES1
Deserializer (410)
DQ
CLK
DCK1
Delay Circuit (420)
CK1
CK2

FIG. 7B

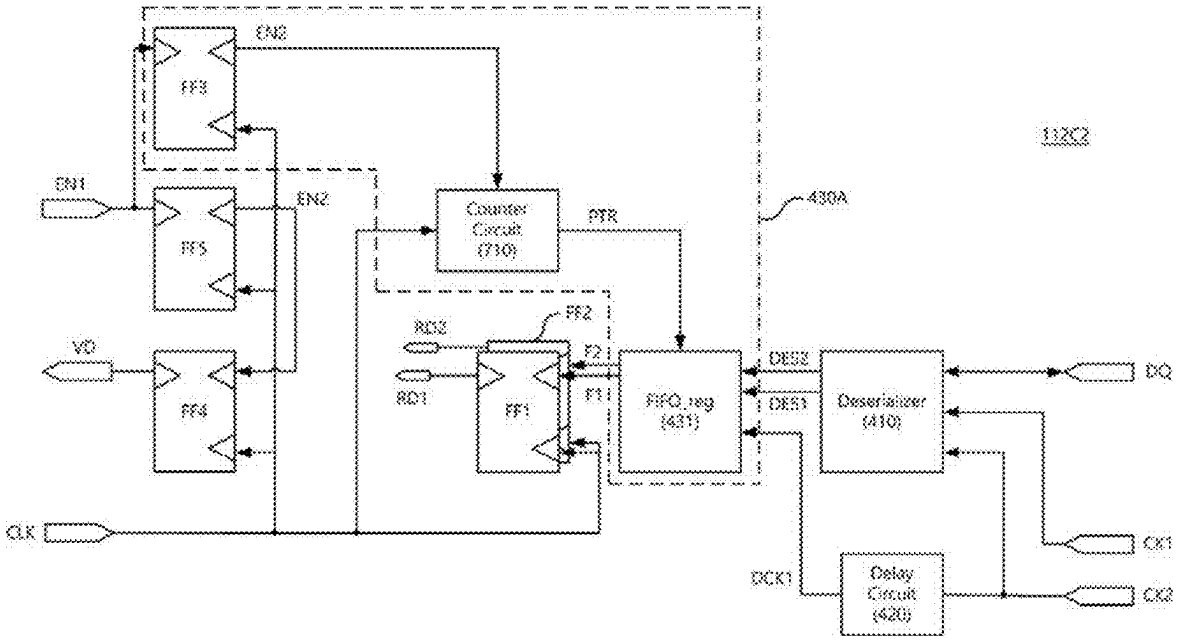

EN2
FF3
112C2
EN1
FF5
EN2
Counter Circuit (710)
PTR
430A
RD2
FF2
VD
F2
RD1
FF4
FF1
F1
FIFO_reg (431)
DES2
DES1
Deserializer (410)
DQ
CK1
CLK
DCK1
Delay Circuit (420)
CK2

FIG. 8

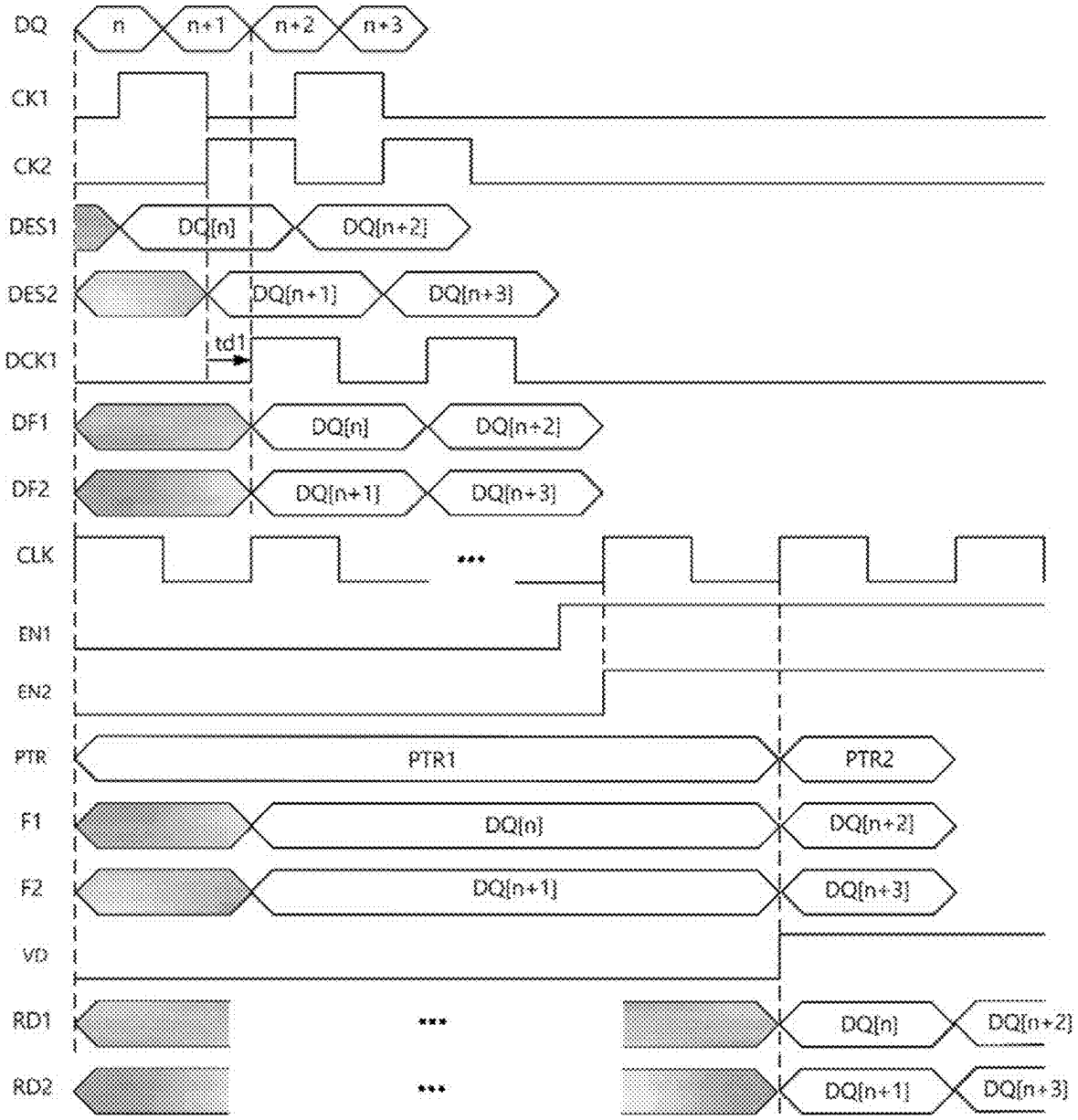

DQ
n
n+1
n+2
n+3
CK1
CK2
DES1
DQ[n]
DQ[n+2]
DES2
DQ[n+1]
DQ[n+3]
tD1
DCK1
DF1
DQ[n]
DQ[n+2]
DF2
DQ[n+1]
DQ[n+3]
CLK
EN1
EN2
PTR
PTR1
PTR2
F1
DQ[n]
DQ[n+2]
F2
DQ[n+1]
DQ[n+3]
VD
RD1
DQ[n]
DQ[n+2]
RD2
DQ[n+1]
DQ[n+3]

FIG. 9

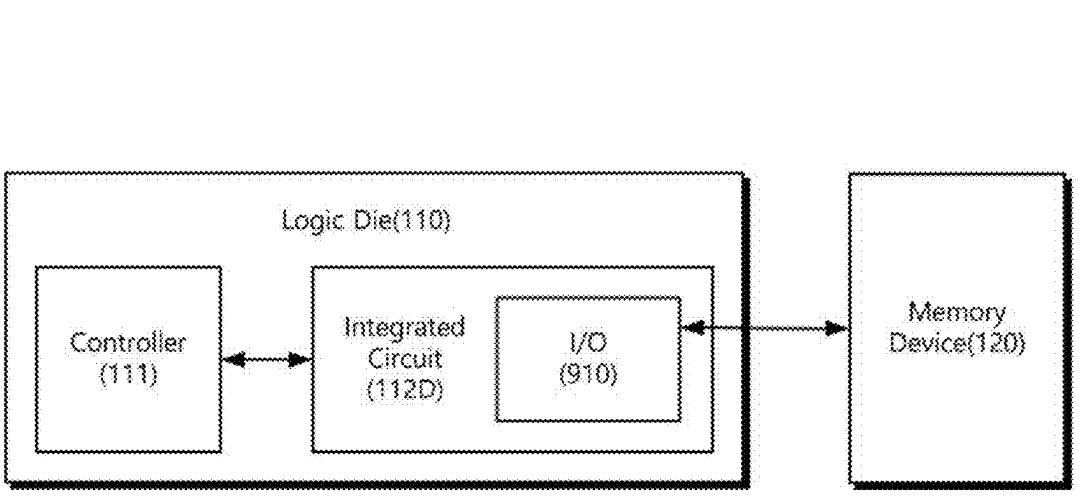

100A
Logic Die(110)
Controller (111)
Integrated Circuit (112D)
I/O (910)
Memory Device(120)

FIG. 10

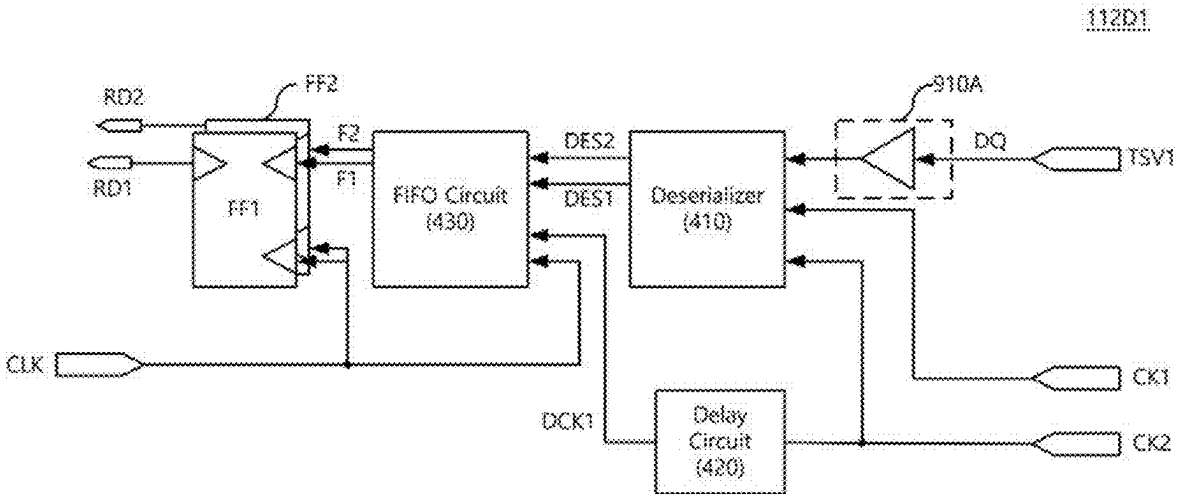
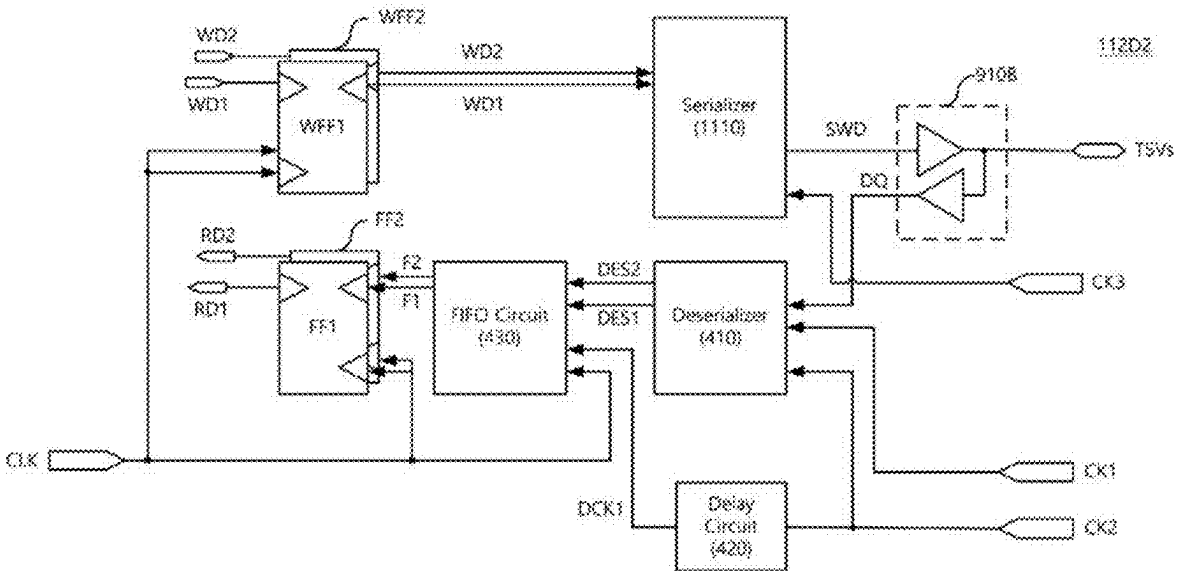

112D1
RD2
RD1
FF2
FF1
F2
F1
FIFO Circuit (430)
DES2
DES1
Deserializer (410)
910A
DQ
TSV1
CLK
DCK1
Delay Circuit (420)
CK1
CK2

FIG. 11


WD2
WD1
WFF2
WFF1
WD2
WD1
Serializer (1110)
112D2
910B
SWD
DQ
TSVs
RD2
RD1
FF2
FF1
F2
F1
FIFO Circuit (430)
DES2
DES1
Deserializer (410)
CK3
CLK
CK1
CK2
DCK1
Delay Circuit (420)

INTEGRATED CIRCUIT READING DATA AND SEMICONDUCTOR DEVICE INCLUDING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is based on and claims priority to Korean Patent Application Nos. 10-2024-0025338, filed on Feb. 21, 2024, and 10-2024-0049641, filed on Apr. 12, 2024, in the Korean Intellectual Property Office, the disclosures of which are incorporated herein by reference in their entireties.

BACKGROUND

1. Field

[0002] The disclosure relates to an integrated circuit configured to read data and a semiconductor device including the same.

2. Description of Related Art

[0003] With the growing demand for high-speed data processing in semiconductor memory devices, high-bandwidth memory (HBM) devices are being used to facilitate high-speed data transfers.

[0004] In order for a controller of an HBM to read data from a memory die, a first-in first-out (FIFO) circuit is required.

[0005] When the FIFO circuit of the HBM operates based on a single-phase clock signal, both a rising edge and a falling edge of the clock signal should be used to read data output from the memory die in a double data rate (DDR) scheme.

[0006] Therefore, a duty of the clock signal should be maintained at a constant level to perform a stable read operation of the HBM.

[0007] However, the clock signal input to the FIFO circuit should be distributed to each of a plurality of through-silicon vias (TSVs) connected to a memory die. As an electrical distance for distributing the clock signal increases, there is the increasing likelihood that the duty of the clock signal is not maintained.

SUMMARY

[0008] Provided is a semiconductor device for stably reading data using clock signals having different phases.

[0009] According to an aspect of the disclosure, a semiconductor device includes: a logic die; and a memory device connected to the logic die, wherein the logic die includes: a deserializer configured to output first parallel data based on input data received from the memory device using a first clock signal having a first phase and output second parallel data based on the input data using a second clock signal having a second phase, wherein the first phase is different from the second phase; and a first-in first-out (FIFO) circuit configured to: sample the first parallel data using the second clock signal and store the sampled first parallel data as first sampling data, sample the second parallel data using the second clock signal and store the sampled second parallel data as second sampling data, output the first sampling data as first output data in response to a rising edge of a memory clock signal, and output the second sampling data as second output data in response to the rising edge of the memory clock signal.

[0010] According to an aspect of the disclosure, an integrated circuit includes: a deserializer configured to output first parallel data based on input data using a first clock signal having a first phase and output second parallel data based on the input data using a second clock signal having a second phase, wherein the first phase is different from the second phase; a delay circuit configured to delay the second clock signal by a first delay time and output a first delay clock signal; and a first-in first-out (FIFO) circuit configured to: sample the first parallel data in response to a rising edge of the first delay clock signal and store the sampled first parallel data as first sampling data, sample the second parallel data in response to the rising edge of the first delay clock signal and store the sampled second parallel data as second sampling data, output the first sampling data as first output data in response to a rising edge of a memory clock signal, and output the second sampling data as second output data in response to the rising edge of the memory clock signal.

[0011] According to an aspect of the disclosure, a semiconductor device includes: a logic die; and a plurality of memory dies stacked on one surface of the logic die and configured to operate using a plurality of clock signals having different phases, wherein the logic die includes: a deserializer configured to output first parallel data based on input data received from the plurality of memory dies using a first clock signal having a first phase and output second parallel data from the input data using a second clock signal having a second phase, wherein the first phase is different from the second phase; a delay circuit configured to delay the second clock signal by a first delay time and output a first delay clock signal; and a first-in first-out (FIFO) circuit configured to: sample the first parallel data in response to a rising edge of the first delay clock signal and store the sampled first parallel data as first sampling data, sample the second parallel data in response to the rising edge of the first delay clock signal and store the sampled second parallel data as second sampling data, and output the first sampling data as first output data and output the second sampling data as second output data in response to a rising edge of a memory clock signal in a FIFO scheme.

BRIEF DESCRIPTION OF DRAWINGS

[0012] The above and other aspects and features of certain embodiments of the present disclosure will be more apparent from the following description taken in conjunction with the accompanying drawings, in which:

[0013] FIG. **1**A is a perspective view illustrating a semiconductor device according to an embodiment of the disclosure;

[0014] FIG. **1**B is a plan view illustrating a first surface of a logic die of FIG. **1**A;

[0015] FIG. **1**C is a diagram illustrating a plurality of clock signals having different phases;

[0016] FIG. **2** is a block diagram illustrating a configuration of a semiconductor device according to an embodiment of the disclosure;

[0017] FIG. **3**A is a circuit diagram illustrating an integrated circuit configured to read data according to an embodiment of the disclosure;

[0018] FIG. **3**B is a diagram illustrating data output through the integrated circuit of FIG. **3**A;

[0019] FIG. **4** is a circuit diagram illustrating a configuration of a delay circuit of FIG. **3**A;

[0020] FIG. **5** is a circuit diagram illustrating an integrated circuit reading data according to an embodiment of the disclosure;

[0021] FIG. **6** is a diagram illustrating data output through the integrated circuit of FIG. **5**;

[0022] FIG. **7**A is a circuit diagram illustrating an integrated circuit configured to read data according to an embodiment of the disclosure;

[0023] FIG. **7**B is a circuit diagram illustrating an integrated circuit further including a fifth flip-flop in the configuration of FIG. **7**A;

[0024] FIG. **8** is a diagram illustrating data output through the integrated circuit of FIG. **7**A;

[0025] FIG. **9** is a circuit diagram illustrating a semiconductor device according to an embodiment of the disclosure;

[0026] FIG. **10** is a circuit diagram illustrating an integrated circuit including an input/output circuit configured to obtain data read from a memory device according to an embodiment of the disclosure; and

[0027] FIG. **11** is a circuit diagram illustrating an integrated circuit including an input/output circuit configured to exchange data with a memory device according to an embodiment of the disclosure.

DETAILED DESCRIPTION

[0028] Hereinafter, example embodiments will be described with reference to the accompanying drawings.

[0029] The terms, such as "first," "second," or the like, may represent various elements regardless of order and/or importance. Such terms may only be used to distinguish one element from another element, and do not limit the order and/or importance of the elements.

[0030] In the following description, like reference numerals refer to like elements throughout the specification. Terms such as "unit", "module", "member", and "block" may be embodied as hardware or software. As used herein, a plurality of "units", "modules", "members", and "blocks" may be implemented as a single component, or a single "unit", "module", "member", and "block" may include a plurality of components.

[0031] It will be understood that when an element is referred to as being "connected" with or to another element, it can be directly or indirectly connected to the other element, wherein the indirect connection may include "connection via a wireless communication network".

[0032] Also, when a part "includes" or "comprises" an element, unless there is a particular description contrary thereto, the part may further include other elements, not excluding the other elements.

[0033] Throughout the description, when a member is "on" another member, this includes not only when the member is in contact with the other member, but also when there is another member between the two members.

[0034] As used herein, the expressions "at least one of a, b or c" and "at least one of a, b and c" indicate "only a," "only b," "only c," "both a and b," "both a and c," "both b and c," and "all of a, b, and c."

[0035] As used herein, the singular forms "a," "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise.

[0036] With regard to any method or process described herein, an identification code may be used for the convenience of the description but is not intended to illustrate the order of each step or operation. Each step or operation may be implemented in an order different from the illustrated order unless the context clearly indicates otherwise. One or more steps or operations may be omitted unless the context of the disclosure clearly indicates otherwise.

[0037] FIG. **1**A is a perspective view illustrating a semiconductor device according to an example embodiment. FIG. **1**B is a plan view illustrating a first surface of a logic die of FIG. **1**A. FIG. **1**C is a diagram illustrating a plurality of clock signals having different phases.

[0038] Referring to FIG. **1**A, a semiconductor device **100** according to an example embodiment may include a logic die **110** and a memory device **120**.

[0039] For example, a semiconductor device **100** may include a logic die **110** controlling the memory device **120**.

[0040] The logic die **110** according to an example embodiment may write data to the memory device **120** or read data from the memory device **120**. For example, the logic die **110** may input and output data to the memory device **120**.

[0041] In addition, for example, the logic die **110** may execute applications, supported by the semiconductor device **100**, using the memory device **120**.

[0042] In addition, the semiconductor device **100** may include a memory device **120** disposed on a first surface **101** of the logic die **110**.

[0043] For example, the semiconductor device **100** may include a memory device **120** disposed on the first surface **101** of the logic die **110** and connected to the logic die **110**.

[0044] According to an example embodiment, the memory device **120** may include a plurality of memory dies **121**, **122**, **123**, and **124** stacked on the first surface **101** of the logic die **110**.

[0045] Therefore, the memory device **120** may be referred to as a high-bandwidth memory (HBM) including a plurality of memory dies **121**, **122**, **123**, and **124** in a stacked configuration. In addition, each of the plurality of memory dies **121**, **122**, **123**, and **124** may be referred to as an HBM DRAM device.

[0046] Furthermore, when the memory device **120** is referred to as an HBM, the semiconductor device **100** may be understood to have a three-dimensional HBM (**3**D HBM) structure in which the HBM is disposed on the first surface of the logic die **110**.

[0047] Referring to FIGS. **1**A and **1**B, the semiconductor device **100** may include a plurality of through-silicon vias (TSVs) TSV1, TSV2, and TSV3.

[0048] For example, the semiconductor device **100** according to an example embodiment may include a plurality of TSVs TSV1, TSV2, and TSV3 connected to the logic die **110** through the first surface **101** of the logic die **110**.

[0049] For example, the plurality of TSVs TSV1, TSV2, and TSV3 may be connected to the first surface **101** of the logic die **110** in the form of an array.

[0050] For example, the plurality of TSVs TSV1, TSV2, and TSV3 may be formed to penetrate at least a portion of the first surface **101** through the first surface **101**.

[0051] In addition, the plurality of TSVs TSV1, TSV2, and TSV3 may be connected to the memory device **120** through a surface of the first memory die **121**, adjacent to the first memory die **121**. For example, the plurality of TSVs

TSV1, TSV2, and TSV3 may be formed to penetrate through at least a portion of the plurality of memory dies **121**, **122**, **123**, and **124**.

[0052] For example, the logic die **110** and the memory device **120** may be connected through the plurality of TSVs TSV1, TSV2, and TSV3. For example, the logic die **110** and the memory device **120** may exchange data through the plurality of TSVs TSV1, TSV2, and TSV3.

[0053] For example, the logic die **110** may read data, stored in the memory device **120**, from the memory device **120** through the plurality of TSVs TSV1, TSV2, and TSV3. In addition, for example, the logic die **110** may write data in the memory device **120** through the plurality of TSVs TSV1, TSV2, and TSV3.

[0054] Referring to FIG. **1**B, the logic die **110** may include a plurality of integrated circuits **171**, **172**, and **173**, respectively disposed adjacent to the plurality of TSVs TSV1, TSV2, and TSV3.

[0055] For example, the logic die **110** may include a plurality of integrated circuits **171**, **172**, and **173**, respectively connected to the plurality of TSVs TSV1, TSV2, and TSV3.

[0056] For example, the logic die **110** may include a first integrated circuit **171** disposed adjacent to the first TSV TSV1 to be connected to the first TSV TSV1.

[0057] For example, the plurality of integrated circuits **171**, **172**, and **173** may be disposed in the form of an array.

[0058] According to an example embodiment, the plurality of integrated circuits **171**, **172**, and **173** may obtain data received through the plurality of TSVs TSV1, TSV2, and TSV3, respectively.

[0059] For example, the first integrated circuit **171** may obtain first input data transmitted from the memory device **120** through the first TSV TSV1 in a process of reading data from the memory device **120**

[0060] According to an example embodiment, the plurality of integrated circuits **171**, **172**, and **173** may transmit data to the memory device **120** through the plurality of TSVs TSV1, TSV2, and TSV3, respectively.

[0061] For example, the second integrated circuit **172** may transmit the second input data to the memory device **120** through the second TSV TSV2 in a process of writing data in the memory device **120**

[0062] For example, the plurality of integrated circuits **171**, **172**, and **173** may deserialize the data received through the plurality of TSVs TSV1, TSV2, and TSV3, respectively.

[0063] Data, transmitted from the memory device **120**, may be transmitted in a double data rate (DDR) scheme.

[0064] Accordingly, the plurality of integrated circuits **171**, **172**, and **173** may deserialize the data received through the plurality of TSVs TSV1, TSV2, and TSV3 and output the parallel data in a single data rate (SDR) scheme.

[0065] Referring to FIGS. **1**A and **1**C, the memory device **120** may operate using a plurality of clock signals CK1, CK2, CK3, and CK4 having different phases.

[0066] For example, the memory device **120** may operate using at least a portion of the first clock signal CK1 to the fourth clock signal CK4 having a phase difference of 90 degrees.

[0067] For example, the memory device **120** may operate using the first clock signal CK1, the second clock signal CK2 having an anti-phase of the first clock signal CK1, the third clock signal CK3 having a phase difference of 90 degrees from the first clock signal CK1, and the fourth clock signal CK4 having an anti-phase of the third clock signal CK3.

[0068] According to an example embodiment, the logic die **110** may deserialize data transmitted from the memory device **120** using at least two clock signals, among the plurality of clock signals CK1, CK2, CK3, and CK4 used in the memory device **120**.

[0069] For example, referring to FIGS. **1**B and **1**C, the first integrated circuit **171** may deserialize first input data, transmitted through the first TSV TSV1, using the first clock signal CK1 and the second clock signal CK2.

[0070] For example, the first integrated circuit **171** may generate first parallel data from the first input data, transmitted through the first TSV TSV1, using the first clock signal CK1. In addition, the first integrated circuit **171** may generate second parallel data from the first input data, transmitted through the first TSV TSV1, using the second clock signal CK2.

[0071] The first parallel data and the second parallel data may be output in an SDR scheme.

[0072] Referring to the above-described configurations, the logic die **110** according to an example embodiment may output data, received from the memory device **120** in the SDR scheme, using a rising edge of each of the plurality of clock signals CK1 and CK2 having different phases in the DDR scheme.

[0073] The above-described configurations may allow the semiconductor device **100** to reliably read data stored in the memory device **120**, regardless of a duty of each clock signal. Thus, the logic die **110** may improve the performance of the semiconductor device **100**.

[0074] In addition, the logic die **110** according to an example embodiment may output parallel data in a first-in first-out (FIFO) manner using one of the clock signals used to deserialize the data transmitted from the memory device **120**.

[0075] For example, the logic die **110** may delay a single clock signal, among clock signals used to deserialize the data transmitted from the memory device **120**, by a predetermined time.

[0076] Furthermore, the logic die **110** may capture and store (or hold) the parallel data in response to a rising edge of the delay clock signal.

[0077] For example, the first integrated circuit **171** may delay the second clock signal CK2 by a predetermined time.

[0078] Furthermore, the first integrated circuit **171** may capture and store the first parallel data and the second parallel data in response to the rising edge of the second clock signal CK2 delayed by the predetermined time.

[0079] Furthermore, the first integrated circuit **171** may output the stored data in a FIFO manner.

[0080] Referring to the above-described configurations, the logic die **110** according to an example embodiment may store two parallel data using a single rising edge of the clock signal delayed by the predetermined time.

[0081] As a result, the semiconductor device **100** may significantly reduce the number of cycles of the clock signal required to output data read from the memory device **120** in a FIFO manner.

[0082] FIG. **2** is a block diagram illustrating a configuration of a semiconductor device according to an example embodiment.

[0083] Referring to FIG. **2**, a semiconductor device **100** according to an example embodiment may include a logic die **110** and a memory device **120**. In addition, the logic die **110** may include a controller **111** and an integrated circuit **112**.

[0084] The semiconductor device **100** illustrated in FIG. **2** may be understood as an example of the semiconductor device **100** illustrated in FIG. **1**A. In addition, the integrated circuit **112** illustrated in FIG. **2** may be understood to have substantially the same configuration as the first integrated circuit **171** illustrated in FIG. **1**B.

[0085] Therefore, the same or substantially the same components are denoted by the same or substantially the same reference numerals, and redundant descriptions are omitted to avoid repetition.

[0086] The logic die **110** may include a controller **111** controlling an operation of the logic die **110**.

[0087] The controller **111** may execute software (or programs) to control at least a portion of one or more other components (for example, the integrated circuit **112**) of the logic die **110** and perform various data processing or operations. In addition, the controller **111** may include a central processing unit, a microprocessor, or the like, and may control the overall operation of the logic die **110**. Therefore, an operation performed by the logic die **110** may be understood to be performed under the control of the controller **111**.

[0088] The controller **111** may write data in the memory device **120** or read data stored in the memory device **120**.

[0089] For example, the controller **111** may transmit a read command to the memory device **120** to read data stored in the memory device **120**. Furthermore, the controller **111** may obtain data, output in response to the read command, from the memory device **120**.

[0090] In addition, the controller **111** may transmit data and a write command to the memory device **120** to write the data in the memory device **120**.

[0091] In addition, the logic die **110** may include an integrated circuit **112** exchanging data with the memory device **120**.

[0092] For example, the integrated circuit **112** may transmit the read command, output from the controller **111**, to the memory device **120**.

[0093] In addition, the integrated circuit **112** may obtain data, output in response to the read command, from the memory device **120**. The integrated circuit **112** may transmit the data, obtained from the memory device **120**, to the controller **111**.

[0094] For example, data output from the memory device **120** in response to the read command may be transmitted to the integrated circuit **112** through at least portion of the TSVs.

[0095] In addition, the integrated circuit **112** may transmit the write command and data, transmitted from the controller **111**, to the memory device **120**.

[0096] For example, the integrated circuit **112** may include a double data rate physical layer (DDR PHY). In addition, the integrated circuit **112** may communicate with the controller **111** and/or the memory device **120** with a DDR PHY interface (DPI).

[0097] In addition, for example, the integrated circuit **112** may support features of the DDR and/or low-power DDR (LPDDR) protocols of the Joint Electron Device Engineering Council (JEDEC) standard.

[0098] According to an example embodiment, the integrated circuit **112** may deserialize data received from the memory device **120**. The data, transmitted from the memory device **120**, may be transmitted in a DDR scheme.

[0099] Accordingly, the integrated circuit **112** may deserialize the data received from the memory device **120** and output the parallel data in an SDR scheme.

[0100] According to an example embodiment, the integrated circuit **112** may deserialize data, received from the memory device **120**, using at least two clock signals, among the plurality of clock signals CK1, CK2, CK3, and CK4 used in the memory device **120**.

[0101] For example, the integrated circuit **112** may generate first parallel data from first input data, transmitted from the memory device **120**, using the first clock signal CK1. In addition, the first integrated circuit **171** may generate second parallel data from the first input data using the second clock signal CK2.

[0102] The first parallel data and the second parallel data may be output in an SDR scheme.

[0103] Referring to the above-described configurations, the integrated circuit **112** according to an example embodiment may output data received from the memory device **120** in an SDR scheme using a rising edge of each of the plurality of clock signals CK1 and CK2 having different phases.

[0104] The above-described configurations may allow the semiconductor device **100** to reliably read data stored in the memory device **120**, regardless of a duty of each clock signal.

[0105] In addition, the integrated circuit **112** according to an example embodiment may output the parallel data in a first-in first-out (FIFO) manner using one of the clock signals used to deserialize the data transmitted from the memory device **120**.

[0106] For example, the integrated circuit **112** may delay one of the clock signals, used to deserialize the data transmitted from the memory device **120**, by a predetermined time.

[0107] Furthermore, the integrated circuit **112** may capture and store (or hold) the parallel data in response to a rising edge of the delay clock signal.

[0108] For example, the integrated circuit **112** may delay the second clock signal CK2 by a predetermined time.

[0109] Furthermore, the integrated circuit **112** may capture and store the first parallel data and the second parallel data in response to the rising edge of the second clock signal CK2 delayed by the predetermined period.

[0110] Furthermore, the integrated circuit **112** may output the stored data in a FIFO manner.

[0111] Referring to the above-described configurations, the integrated circuit **112** according to an example embodiment may store two parallel data using a single rising edge of a clock signal delayed for a predetermined time.

[0112] As a result, the semiconductor device **100** may significantly reduce the number of cycles of the clock signal required to output data read from the memory device **120** in a FIFO manner.

[0113] FIG. **3**A is a circuit diagram illustrating an integrated circuit reading data according to an example embodiment, and FIG. **3**B is a diagram illustrating data output through the integrated circuit of FIG. **3**A. FIG. **4** is a circuit diagram illustrating a configuration of a delay circuit of FIG. **3**A.

[0114] Referring to FIG. **3**A, the integrated circuit **112**A according to an example embodiment may include a deserializer **410**, a delay circuit **420**, and a FIFO circuit **430**.

[0115] The integrated circuit **112**A illustrated in FIG. **3**A may be understood as an example of the integrated circuit **112** illustrated in FIG. **2**.

[0116] According to an example embodiment, the integrated circuit **112**A may include a deserializer **410** obtaining input data DQ from the memory device **120**.

[0117] In here, the deserializer **410** may be referred to as a circuit that converts input serial data into parallel data and outputs it. For example, the deserializer **410** may include at least one flip-flop that outputs data in response to a clock signal.

[0118] For example, the deserializer **410** may deserialize the input data DQ using a first clock signal CK1 and a second clock signal CK2. The first clock signal CK1 and the second clock signal CK2 may have a phase difference of 180 degrees.

[0119] Referring to FIGS. **3**A and **3**B, the deserializer **410** may output first parallel data DES1 from the input data DQ using the first clock signal CK1.

[0120] For example, the deserializer **410** may output first parallel data DES1 including "DQ[n]" and "DQ[n+2]" corresponding to a rising edge of the first clock signal CK1, among bits of the input data DQ.

[0121] For example, the deserializer **410** may output first parallel data DES1 including odd bits, among the bits of the input data DQ, using the first clock signal CK1.

[0122] In addition, the deserializer **410** may output second parallel data DES2 from the input data DQ using the second clock signal CK2.

[0123] For example, the deserializer **410** may output second parallel data DES2 including "DQ[n+1]" and "DQ[n+3]" corresponding to a rising edge of the second clock signal CK2, among the bits of the input data DQ.

[0124] For example, the deserializer **410** may output second parallel data DES2 including even bits, among the bits of the input data DQ, using the second clock signal CK2.

[0125] Referring to the above-described configurations, the deserializer **410** according to an example embodiment may deserialize the input data DQ using the rising edge of each of the clock signals CK1 and CK2 having different phases.

[0126] As a result, the integrated circuit **112**A according to an example embodiment may reliably read data transmitted from the memory device **120**, regardless of a duty of each of the clock signals CK1 and CK2.

[0127] In addition, the integrated circuit **112**A may include a delay circuit **420** delaying the second clock signal CK2 by a first delay time td1.

[0128] For example, the delay circuit **420** may delay the phase of the second clock signal CK2 by the first delay time td1 to output a first delay clock signal DCK1.

[0129] Referring to FIG. **4**, a delay circuit **420**A according to an example embodiment may include an even number of inverters connected in series. The delay circuit **420**A may be understood as an example of the delay circuit **420** illustrated in FIG. **3**A.

[0130] The delay circuit **420**A may delay a phase of a second clock signal CK2 in proportion to the number of paired inverters.

[0131] According to an example embodiment, the delay circuit **420** may include a plurality of buffers connected in series.

[0132] The delay circuit **420** may delay a phase of the second clock signal CK2 in proportion to the number of buffers.

[0133] However, the configuration of the delay circuit **420** is not limited to the above-described examples, and the delay circuit **420** may have various configurations to delay the phase of the second clock signal CK2 by the first delay time td1.

[0134] In addition, the integrated circuit **112**A may include a FIFO circuit **430** processing first parallel data DES1 and second parallel data DES2 in a FIFO manner. In here, the FIFO circuit **430** may be referred to as a circuit that outputs data according to the order of input data in a first-in, first out manner in response to a clock signal.

[0135] For example, the FIFO circuit **430** may sample the first parallel data DES1 and the second parallel data DES2 using the second clock signal CK2.

[0136] According to an example embodiment, the FIFO circuit **430** may sampling the first parallel data DES1 and the second parallel data DES2 using the first delay clock signal DCK1 generated based on the second clock signal CK2.

[0137] According to an example embodiment, the FIFO circuit **430** may capture and hold the first parallel data DES1 and the second parallel data DES2 using a rising edge of the first delay clock signal DCK1.

[0138] Referring to FIGS. **3**A and **3**B, the FIFO circuit **430** according to an example embodiment may capture "DQ[n]" of the first parallel data DES1 and "DQ[n+1]" of the second parallel data DES2 in response to the rising edge of the first delay clock signal DCK1.

[0139] In addition, the FIFO circuit **430** may capture "DQ[n+2]" of the first parallel data DES1 and "DQ[n+3]" of the second parallel data DES2 in response to the rising edge of the first delay clock signal DCK1.

[0140] For example, referring to the above-described configurations, the FIFO circuit **430** may capture the first parallel data DES1 and the second parallel data DES2 together in response to one rising edge of the first delay clock signal DCK1.

[0141] As a result, the integrated circuit **112**A may significantly reduce the number of cycles of a clock signal required to process data read from the memory device **120** in a FIFO manner.

[0142] Referring to the above-described configurations, the integrated circuit **112**A according to an example embodiment may capture the first parallel data DES1 and the second parallel data DES2 using the first delay clock signal DCK1 generated by delaying the second clock signal CK2 by the first delay time td1.

[0143] Thus, the two parallel data DES1 and DES2 may be captured with a relatively small amount of delay time, compared to the case in which the two parallel data DES1 and DES2 are captured using a signal generated by delaying the first clock signal CK1.

[0144] For example, the integrated circuit **112**A may capture the two parallel data DES1 and DES2 using the first delay clock signal DCK1, generated by delaying the second clock signal CK2, to significantly reduce a delay time caused by the delay circuit **420**.

[0145] As a result, the integrated circuit **112**A according to an example embodiment may significantly reduce power

consumed by the delay circuit **420**. In addition, the integrated circuit **112**A may significantly reduce an area of the delay circuit **420**.

[0146] According to one or more embodiments, among the components of the integrated circuit **112**, the delay circuit **420** may be omitted.

[0147] For example, the FIFO circuit **430** according to an example embodiment may capture (or store) the first parallel data DES1 and the second parallel data DES2 in response to the second clock signal CK2.

[0148] For example, the FIFO circuit **430** may capture "DQ[n]" of the first parallel data DES1 and "DQ[n+1]" of the second parallel data DES2 in response to the rising edge of the second clock signal CK2.

[0149] In addition, the FIFO circuit **430** may capture "DQ[n+2]" of the first parallel data DES1 and "DQ[n+3]" of the second parallel data DES2 in response to the rising edge of the second clock signal CK2.

[0150] Furthermore, the FIFO circuit **430** may store a results of sampling the first parallel data DES1 and the second parallel data DES2.

[0151] For example, the FIFO circuit **430** may store the first sampling data DF1 as a result of sampling the first parallel data DES1. In addition, the FIFO circuit **430** may store the second sampling data DF2 as a result of sampling the second parallel data DES2.

[0152] In addition, the FIFO circuit **430** may output the stored data in a FIFO manner.

[0153] For example, the FIFO circuit **430** may output first sampling data DF1 and second sampling data DF2 in response to the memory clock signal CLK.

[0154] For example, the memory clock signal CLK may be understood as a clock signal controlling an operation of a controller (for example, the controller **111** of FIG. **2**) of a logic die (for example, the logic die **110** of FIG. **2**).

[0155] For example, the FIFO circuit **430** may output the first sampling data DF1 and the second sampling data DF2 in response to the rising edge of the memory clock signal CLK.

[0156] Referring to FIG. **3**B, the FIFO circuit **430** may output the first sampling data DF1 as first output data F1 in response to the rising edge of the memory clock signal CLK.

[0157] In addition, the FIFO circuit **430** may output the second sampling data DF2 as second output data F2 in response to the rising edge of the memory clock signal CLK.

[0158] Each of the first output data F1 and the second output data F2 may be output in an SDR scheme.

[0159] For example, the integrated circuit **112**A may convert the input data DQ, read from the memory device **120** in a DDR scheme, in an SDR scheme and output the converted data using the plurality of clock signals CK1 and CK2 having different phases (for example, an anti-phase).

[0160] As a result, the integrated circuit **112**A according to an example embodiment may output data transmitted from the memory device **120** in the SDR scheme, regardless of a duty of each of the clock signals CK1 and CK2.

[0161] FIG. **5** is a circuit diagram illustrating an integrated circuit reading data according to an example embodiment. FIG. **6** is a diagram illustrating data output through the integrated circuit of FIG. **5**.

[0162] Referring to FIG. **5**, the integrated circuit **112**B according to an example embodiment may include a deserializer **410**, a delay circuit **420**, a FIFO circuit **430**, a first flip-flop FF1, and a second flip-flop FF2.

[0163] The integrated circuit **112**B illustrated in FIG. **5** may be understood as an example of the integrated circuit **112** illustrated in FIG. **2**.

[0164] In addition, the integrated circuit **112**B of FIG. **5** may be understood as an example that further includes a first flip-flop FF1 and a second flip-flop FF2, in addition to the configuration of the integrated circuit **112**A illustrated in FIG. **3**A.

[0165] Therefore, the same or substantially the same components are denoted by the same or substantially the same reference numerals, and redundant descriptions are omitted to avoid repetition.

[0166] According to an example embodiment, the integrated circuit **112**B may include a first flip-flop FF1 and a second flip-flop FF2 that output the data output from the FIFO circuit **430**.

[0167] For example, each of the first flip-flop FF1 and the second flip-flop FF2 may output data transmitted from the FIFO circuit **430** in response to a memory clock signal CLK.

[0168] Referring to FIG. **6**, the first flip-flop FF1 may output first output data F1 as first read data RD1 in response to the memory clock signal CLK.

[0169] For example, the first flip-flop FF1 may output the first output data F1, output from the FIFO circuit **430**, as the first read data RD1 in response to a rising edge of the memory clock signal CLK.

[0170] The second flip-flop FF2 may output second output data F2 as second read data RD2 in response to the memory clock signal CLK.

[0171] For example, the second flip-flop FF2 may output the second output data F2, output from the FIFO circuit **430**, as second read data RD2 in response to the rising edge of the memory clock signal CLK.

[0172] For example, the FIFO circuit **430** may output the first output data F1 and the second output data F2 in response to a first rising edge RE1 of the memory clock signal CLK.

[0173] Furthermore, the first flip-flop FF1 may output the first output data F1 as the first read data RD1 in response to a second rising edge RE2, subsequent to the first rising edge RE1 of the memory clock signal CLK.

[0174] The second flip-flop FF2 may output the second output data F2 as the second read data RD2 in response to the second rising edge RE2 of the memory clock signal CLK.

[0175] Each of the first flip-flop FF1 and the second flip-flop FF2 may output the first read data RD1 and the second read data RD2 to a controller (for example, the controller **111** of FIG. **2**).

[0176] Each of the first read data RD1 and the second read data RD2 may be output in an SDR scheme.

[0177] For example, the integrated circuit **112**B may convert input data DQ, read from the memory device **120** in a DDR scheme, in an SDR scheme and output the converted data using rising edges of a plurality of clock signals CK1 and CK2 having different phases (for example, an anti-phase).

[0178] As a result, the integrated circuit **112**B according to an example embodiment may reliably read data output from the memory device **120**, regardless of a duty of each of the clock signals CK1 and CK2.

[0179] FIG. **7**A is a circuit diagram illustrating an integrated circuit reading data according to an example embodiment, and FIG. **7**B is a circuit diagram illustrating an

integrated circuit further including a fifth flip-flop in the configuration of FIG. **7**A. FIG. **8** is a diagram illustrating data output through the integrated circuit of FIG. **7**A.

[0180] Referring to FIG. **7**A, the integrated circuit **112**C**1** according to an example embodiment may include a deserializer **410**, a delay circuit **420**, and a FIFO circuit **430**A. The FIFO circuit **430**A may include a third flip-flop FF3, a counter circuit **710**, and a FIFO register (FIFO_reg) **431**.

[0181] The integrated circuit **112**C**1** illustrated in FIG. **7**A may be understood as an example of the integrated circuit **112** illustrated in FIG. **2**. In addition, the FIFO circuit **430**A illustrated in FIG. **7**A may be understood as an example of the FIFO circuit **430** illustrated in FIG. **5**.

[0182] In addition, the integrated circuit **112**C**1** illustrated in FIG. **7**A may be understood as an example that further includes a fourth flip-flop FF4, in addition to the configuration of the integrated circuit **112**B illustrated in FIG. **5**.

[0183] Therefore, the same or substantially the same components are denoted by the same or substantially the same reference numerals, and redundant descriptions are omitted to avoid repetition.

[0184] According to an example embodiment, the FIFO circuit **430**A may include a third flip-flop FF3 receiving a first enable signal EN1.

[0185] For example, the third flip-flop FF3 may receive the first enable signal EN1 from a controller (for example, the controller **111** of FIG. **2**).

[0186] In addition, the third flip-flop FF3 may output a second enable signal EN2 in response to the memory clock signal CLK.

[0187] For example, the third flip-flop FF3 may output a second enable signal EN2 from the first enable signal EN1 in response to a rising edge of the memory clock signal CLK.

[0188] For example, the third flip-flop FF3 may output the first enable signal EN1, delayed by ¼ of a cycle of the memory clock signal CLK, as a second enable signal EN2.

[0189] Referring to FIG. **7**B according to an example embodiment, an integrated circuit **112**C**2** may further include a fifth flip-flop FF5 receiving a first enable signal EN1.

[0190] For example, the fifth flip-flop FF5 may receive the first enable signal EN1 from a controller (for example, the controller **111** of FIG. **2**).

[0191] In addition, the fifth flip-flop FF5 may output a second enable signal EN2 in response to the memory clock signal CLK.

[0192] For example, the fifth flip-flop FF5 may output the second enable signal EN2 from the first enable signal EN1 in response to a rising edge of the memory clock signal CLK.

[0193] For example, the fifth flip-flop FF5 may output the first enable signal EN1, delayed by ¼ of a cycle of the memory clock signal CLK, as the second enable signal EN2. Referring to FIGS. **7**A and **7**B, the FIFO circuit **430**A according to an example embodiment may include a counter circuit **710** obtaining the second enable signal EN2.

[0194] That is, in here, the counter circuit **710** may be referred to as a circuit that counts and outputs the number of times a rising edge of an input clock signal occurs over a certain period of time.

[0195] For example, the counter circuit **710** may count the number of rising edges of the memory clock signal CLK while the second enable signal EN2 is maintained at a logic high level.

[0196] The counter circuit **710** may output a pointer signal PTR according to the rising edge of the memory clock signal CLK while the second enable signal EN2 is maintained at a logic high level.

[0197] For example, referring to FIG. **8**, the counter circuit **710** may output a first pointer signal PTR1 until a first rising edge of the memory clock signal CLK occurs after the second enable signal EN2 transitions to a logic high level.

[0198] In addition, the counter circuit **710** may output a second pointer signal PTR2 in response to the first rising edge of the memory clock signal CLK occurring while the second enable signal EN2 is maintained at a logic high level.

[0199] According to an example embodiment, the FIFO circuit **430**A may include a FIFO register **431** outputting first output data F1 and second output data F2.

[0200] According to an example embodiment, the FIFO register **431** may sample (or store) first parallel data DES1 and second parallel data DES2 in response to a first delay clock signal DCK1.

[0201] For example, the FIFO register **431** may sample the first parallel data DES1 in response to a rising edge of the first delay clock signal DCK1 and store the sampled data as first sampling data DF1.

[0202] In addition, the FIFO register **431** may sample the second parallel data DES2 in response to the rising edge of the first delay clock signal DCK1 and store the sampled data as second sampling data DF2.

[0203] Furthermore, the FIFO register **431** may output the first output data F1 and the second output data F2 based on the pointer signal PTR transmitted from the counter circuit **710**.

[0204] For example, the FIFO register **431** may output data, corresponding to the pointer signal PTR transmitted from the counter circuit **710**, from data stored in the FIFO register **431**.

[0205] For example, the FIFO register **431** may output a data bit "DQ[n]" corresponding to the first pointer signal PTR1, among bits of the first sampling data DF1, as the first output data F1 in response to the first pointer signal PTR1.

[0206] In addition, the FIFO register **431** may output a data bit "DQ[n+1]" corresponding to the first pointer signal PTR1, among bits of the second sampling data DF2, as the second output data F2 in response to the first pointer signal PTR1.

[0207] For example, the FIFO register **431** may output a data bit "DQ[n+2]" corresponding to the second pointer signal PTR2, among the bits of the first sampling data DF1, as the first output data F1 in response to the second pointer signal PTR2.

[0208] In addition, the FIFO register **431** may output a data bit "DQ[n+3]" corresponding to the second pointer signal PTR2, among the bits of the second sampling data DF2, as the second output data F2 in response to the second pointer signal PTR2.

[0209] The integrated circuits **112**C**1** and **112**C**2** according to an example embodiment may include a fourth flip-flop FF4 outputting a valid signal VD based on the second enable signal EN2.

[0210] For example, the fourth flip-flop FF4 may obtain the second enable signal EN2 output from the third flip-flop FF3 or the fifth flip-flop FF5.

[0211] Referring to FIG. **8**, the fourth flip-flop FF4 may output a valid signal VD having a logic high level in response to the rising edge of the memory clock signal CLK.

[0212] For example, the fourth flip-flop FF4 may output a high-level valid signal VD to the controller **111** in response to the rising edge of the memory clock signal CLK.

[0213] The controller **111** may obtain the first read data RD1 and the second read data RD2 output from the first flip-flop FF1 in response to the high-level valid signal VD being received.

[0214] For example, the controller **111** may identify the first read data RD1 and the second read data RD2 as data that has been validly read from the memory device **120**, in response to the high-level valid signal VD being received.

[0215] For example, the controller **111** may identify (or obtain) data output while the valid signal VD is maintained at a logic high level, among data output from the first flip-flop FF1, as data that has been validly read from the memory device **120**.

[0216] Referring to the above-described configurations, the integrated circuits **112**C**1** and **112**C**2** according to an example embodiment may transmit the first read data RD1 and the second read data RD2 to the controller **111** based on the first enable signal EN1 received from the controller **111**.

[0217] The controller **111** may identify (or obtain) the data, transmitted while the valid signal VD is maintained at a logic high level, as the data that has been validly read from the memory device **120**.

[0218] As a result, the semiconductor device **100** according to an example embodiment may significantly reduce power consumption for reading data from the memory device **120**.

[0219] FIG. **9** is a circuit diagram illustrating a semiconductor device according to an example embodiment. FIG. **10** is a circuit diagram illustrating an integrated circuit including an input/output circuit obtaining data read from a memory device according to an example embodiment. FIG. **11** is a circuit diagram illustrating an integrated circuit including an input/output circuit exchanging data with a memory device according to an example embodiment.

[0220] Referring to FIG. **9**, a semiconductor device **100**A according to an example embodiment may include a logic die **110** and a memory device **120**. The logic die **110** may include a controller **111** and an integrated circuit **112**D.

[0221] The integrated circuit **112**D according to an example embodiment may further include an input/output circuit **910** exchanging data with the memory device **120**.

[0222] The semiconductor device **100**A illustrated in FIG. **9** may be understood as an example of the semiconductor device **100** illustrated in FIG. **2**. In addition, the semiconductor device **100**A illustrated in FIG. **9** may be understood as an example that further includes an input/output circuit **910**, in addition to the configuration of the semiconductor device **100** illustrated in FIG. **2**.

[0223] Therefore, the same or substantially the same components are denoted by the same or substantially the same reference numerals, and redundant descriptions are omitted to avoid repetition.

[0224] According to an example embodiment, the controller **111** may exchange data with the memory device **120** through the input/output circuit **910** included in the integrated circuit **112**D.

[0225] In here, the input/output circuit **910** may be referred to as a circuit that controls data exchange between the logic die **110** and the memory device **120**.

[0226] For example, the controller **111** may obtain data, transmitted from the memory device **120** through a plurality of TSVs, using the input/output circuit **910**.

[0227] In addition, the controller **111** may transmit data to be written in the memory device **120** to the memory device **120** through a plurality of TSVs using the input/output circuit **910**.

[0228] For example, the input/output circuit **910** according to an example embodiment may exchange data with the memory device **120** through a plurality of TSVs connecting the logic die **110** and the memory device **120**.

[0229] According to an example embodiment, the logic die **110** and the memory device **120** may be connected through a plurality of through back-end-of-line (BEOL) vias (TBVs).

[0230] Accordingly, the input/output circuit **910** may exchange data with the memory device **120** through a plurality of TBVs connecting the logic die **110** and the memory device **120**.

[0231] According to an example embodiment, the input/output circuit **910** may include a DDR physical layer (DDR PHY). The input/output circuit **910** may communicate with the controller **111** and/or the memory device **120** with a DDR PHY interface (DFI).

[0232] Referring to FIG. **10**, the integrated circuit **112**D**1** according to an example embodiment may include a deserializer **410**, a delay circuit **420**, a FIFO circuit **430**, a first flip-flop FF1, a second flip-flop FF2, and an input/output circuit **910**A.

[0233] The integrated circuit **112**D**1** may include an input/output circuit **910**A obtaining input data DQ received from the memory device **120** through a first TSV TSV1.

[0234] The input/output circuit **910**A illustrated in FIG. **10** may be understood as an example of the input/output circuit **910** illustrated in FIG. **9**. In addition, the integrated circuit **112**D**1** may be understood as an example that further includes an input/output circuit **910**A, in addition to the configuration of the integrated circuit **112**B illustrated in FIG. **5**.

[0235] Therefore, the same or substantially the same components are denoted by the same or substantially the same reference numerals, and redundant descriptions are omitted to avoid repetition.

[0236] According to an example embodiment, the input/output circuit **910**A may obtain input data DQ transmitted from the memory device **120** through the first TSV TSV1.

[0237] In addition, the controller **111** according to an example embodiment may control the input/output circuit **910**A to control a voltage level of a signal received through the first TSV TSV1.

[0238] For example, when the memory device **120** and the logic die **110** operate using different levels of operating voltage, the controller **111** may control the voltage level of the signal obtained through the first TSV TSV1 to correspond to the level of the operating voltage of the logic die **110**, using the input/output circuit **910**A.

[0239] Referring to FIG. **11**, an integrated circuit **112**D**2** according to an example embodiment may include a deserializer **410**, a delay circuit **420**, a FIFO circuit **430**, a first flip-flop FF1, a second flip-flop FF2, an input/output circuit **910**B, a serializer **1110**, a first write flip-flop WFF1, and a second write flip-flop WFF2.

[0240] The integrated circuit **112**D**2** may include an input/output circuit **910**B exchanging data with the memory device **120** through a plurality of through-silicon vias (TSVs).

[0241] The plurality of TSVs may be understood as having substantially the same configuration as the plurality of TSVs TSV1, TSV2, and TSV3 illustrated in FIG. **1***b*.

[0242] In addition, the input/output circuit **910**B may be understood as an example of the input/output circuit **910** illustrated in FIG. **9**.

[0243] The integrated circuit **112**D**2** illustrated in FIG. **11** may be understood as an example that further includes an input/output circuit **910**B, a serializer **1110**, a first write flip-flop WFF1, and a second write flip-flop WFF2, in addition to the configuration of the integrated circuit **112**B illustrated in FIG. **5**.

[0244] Therefore, the same or substantially the same components are denoted by the same or substantially the same reference numerals, and redundant descriptions are omitted to avoid repetition.

[0245] According to an example embodiment, the input/output circuit **910**B may obtain input data DQ transmitted from a memory device **120** through a first TSV TSV1.

[0246] In addition, the input/output circuit **910**B may transmit serial write data SWD to the memory device **120** through a second TSV TSV2.

[0247] The integrated circuit **112**D**2** according to an example embodiment may further include a first write flip-flop WFF1 and a second write flip-flop WFF2, respectively obtaining first write data WD1 and second write data WD2 from the controller **111**.

[0248] For example, the first write flip-flop WFF1 may output the first write data WD1, obtained from the controller **111**, in response to the memory clock signal CLK.

[0249] In addition, the second write flip-flop WFF2 may output the second write data WD2, obtained from the controller **111**, in response to the memory clock signal CLK.

[0250] In addition, the integrated circuit **112**D**2** may include a serializer **1110** serializing the first write data WD1 and the second write data WD2.

[0251] In here, a serializer **1110** may be referred to as a circuit that converts input parallel data into serial data and outputs it. For example, the serializer **1110** may include a plurality of flip-flops that are connected to each other.

[0252] For example, the serializer **1110** may serialize the first write data WD1 and the second write data WD2 using a third clock signal CK3.

[0253] For example, the serializer **1110** may output serial write data SWD, consisting of bits of the first write data WD1 and the second write data WD2, in response to a rising edge of the third clock signal CK3.

[0254] Furthermore, the input/output circuit **910**B may transmit the serial write data SWD to the memory device **120** through a first TSV TSV1.

[0255] Referring to the above-described configurations, the semiconductor device **100**A according to an example embodiment may read data stored in the memory device **120** or store data in the memory device **120** through the integrated circuit **112**D.

[0256] The integrated circuit **112**D may output the input data DQ, transmitted from the memory device **120**, as first read data RD1 and second read data RD2 using rising edges of the clock signals CK1 and CK2 having different phases.

[0257] For example, the integrated circuit **112**D may output the input data DQ, received from the memory device **120** in a DDR scheme, in an SDR scheme using the rising edge of each of the clock signals CK1 and CK2 having different phases.

[0258] As a result, the semiconductor device **100**A may reliably read data stored in the memory device **120** regardless of a duty of each clock signal.

[0259] As described above, the integrated circuit **112** according to an example embodiment may output data, received from the memory device **120** in the DDR scheme, in the SDR scheme using the rising edge of each of the plurality of clock signals CK1 and CK2 having different phases.

[0260] As a result, the semiconductor device **100** may reliably read data stored in the memory device **120** regardless of a duty of each clock signal.

[0261] In addition, referring to the above-described configurations, the integrated circuit **112** according to an example embodiment may store two parallel data using a single rising edge of a clock signals delayed by a predetermined time.

[0262] As a result, the semiconductor device **100** may significantly reduce the number of cycles of a clock signal required to output data read from the memory device **120** in a first-in first-out (FIFO) manner.

[0263] In addition, referring to the above-described configurations, the integrated circuit **112** according to an example embodiment may capture first parallel data DES1 and second parallel data DES2 using the first delay clock signal DCK1 generated by delaying the second clock signal CK2 by a first delay time td1.

[0264] The two parallel data DES1 and DES2 may be captured with a relatively small amount of delay time, compared to the case in which the two deserialized data DES1 and DES2 are captured using a signal generated by delaying the first clock signal CK1.

[0265] For example, the integrated circuit **112** may capture the two parallel data DES1 and DES2 using the first delay clock signal DCK1, generated by delaying the second clock signal CK2, to significantly reduce a delay time caused by the delay circuit.

[0266] As a result, the integrated circuit **112** according to the example embodiment may significantly reduce power consumption caused by the delay circuit **420**. In addition, the integrated circuit **112** may significantly reduce an area of the delay circuit **420**.

[0267] As set forth above, a semiconductor device according to example embodiments may stably read data, regardless of a duty of each clock signal, using clock signals having different phases.

[0268] At least one of the components, elements, modules, units, or the like (collectively "components" in this paragraph) represented by a block or an equivalent indication (collectively "block") in the above embodiments including the drawings such as FIGS. **2**, **3**A, **5**, **7**A, **7**B, **9**, **10** and **11**, for example, deserializer, serializer, FIFO circuit, delay

circuit, controller, counter circuit, flip-flop, latch, or the like, may carry out the above-described function or functions. These blocks may be physically implemented by analog and/or digital circuits such as logic gates, integrated circuits, microprocessors, microcontrollers, memory circuits, passive electronic components, active electronic components, optical components, hardwired circuits and the like, and may optionally be driven by a firmware. The circuits may, for example, be embodied in one or more semiconductor chips, or on substrate supports such as printed circuit boards and the like. The circuits constituting a block may be implemented by dedicated hardware, or by a processor (e.g., one or more programmed microprocessors and associated circuitry), or by a combination of dedicated hardware to perform some functions of the block and a processor to perform other functions of the block. Each block of the embodiments may be physically separated into two or more interacting and discrete blocks without departing from the scope of the disclosure. Likewise, the blocks of the embodiments may be physically combined into more complex blocks without departing from the scope of the disclosure.

[0269] While example embodiments have been shown and described above, it will be apparent to those skilled in the art that modifications and variations could be made without departing from the scope of the present disclosure as defined by the appended claims.

What is claimed is:

1. A semiconductor device comprising:

a logic die; and

a memory device connected to the logic die,

wherein the logic die comprises:

a deserializer configured to output first parallel data based on input data received from the memory device using a first clock signal having a first phase and output second parallel data based on the input data using a second clock signal having a second phase, wherein the first phase is different from the second phase; and

a first-in first-out (FIFO) circuit configured to:

sample the first parallel data using the second clock signal and store the sampled first parallel data as first sampling data,

sample the second parallel data using the second clock signal and store the sampled second parallel data as second sampling data,

output the first sampling data as first output data in response to a rising edge of a memory clock signal, and

output the second sampling data as second output data in response to the rising edge of the memory clock signal.

2. The semiconductor device of claim **1**,

wherein the logic die further comprises a first flip-flop and a second flip-flop,

wherein the first and the second flip-flops are connected to the FIFO circuit,

wherein the first flip-flop is configured to output the first output data as first read data in response to the memory clock signal, and

wherein the second flip-flop is configured to output the second output data as second read data in response to the memory clock signal.

3. The semiconductor device of claim **2**,

wherein the logic die further comprises:

a controller configured to execute one or more instructions which cause the controller to extract data from the memory device;

a third flip-flop configured to output a second enable signal based on a first enable signal, received from the controller, in response to the memory clock signal; and

a counter circuit configured to output a pointer signal in response to the rising edge of the memory clock signal while the second enable signal is maintained at a logic high level, and

wherein the FIFO circuit is further configured to output data corresponding to the pointer signal transmitted from the counter circuit.

4. The semiconductor device of claim **3**,

wherein the counter circuit is further configured to output a first pointer signal in response to a first rising edge of the memory clock signal while the second enable signal is maintained at a logic high level, and

wherein the FIFO circuit is further configured to:

output a data bit corresponding to the first pointer signal, among bits of the first sampling data, as the first output data; and

output a data bit corresponding to the first pointer signal, among bits of the second sampling data, as the second output data.

5. The semiconductor device of claim **3**,

wherein the logic die further comprises a fourth flip-flop configured to output a valid signal based on the second enable signal in response to the rising edge of the memory clock signal, and

wherein the controller is further configured to execute the one or more instructions which cause the controller to, based on the valid signal being logic high, obtain the first read data and the second read data.

6. The semiconductor device of claim **3**,

wherein the input data is received in a double data rate (DDR) scheme, and

wherein the controller is further configured to execute the one or more instructions which cause the controller to read the first read data and the second read data in a single data rate (SDR) scheme.

7. The semiconductor device of claim **3**,

wherein the memory device comprises a plurality of memory dies stacked on one surface of the logic die, and

wherein the plurality of memory dies are configured to exchange data with the logic die through a plurality of through-silicon vias (TSVs).

8. The semiconductor device of claim **7**,

wherein the logic die further comprises an input/output circuit configured to receive the input data through a first TSV, and

wherein the controller is further configured to execute the one or more instructions which cause the controller to control a voltage level of a signal received through the first TSV, using the input/output circuit.

9. The semiconductor device of claim **1**,

wherein the logic die further comprises a delay circuit configured to delay the second clock signal by a first delay time and output a first delay clock signal, and

wherein the FIFO circuit is further configured to sample the first parallel data and the second parallel data in response to a rising edge of the first delay clock signal.

10. The semiconductor device of claim **8**,

wherein the memory device operates using the first clock signal, the second clock signal, a third clock signal having a phase difference of 90 degrees from the first clock signal, and a fourth clock signal having an anti-phase of the third clock signal, and

wherein the logic die receives the first clock signal and the second clock signal from the memory device through at least a portion of the plurality of TSVs.

11. An integrated circuit comprising:

a deserializer configured to output first parallel data based on input data using a first clock signal having a first phase and output second parallel data based on the input data using a second clock signal having a second phase, wherein the first phase is different from the second phase;

a delay circuit configured to delay the second clock signal by a first delay time and output a first delay clock signal; and

a first-in first-out (FIFO) circuit configured to:

sample the first parallel data in response to a rising edge of the first delay clock signal and store the sampled first parallel data as first sampling data,

sample the second parallel data in response to the rising edge of the first delay clock signal and store the sampled second parallel data as second sampling data,

output the first sampling data as first output data in response to a rising edge of a memory clock signal, and

output the second sampling data as second output data in response to the rising edge of the memory clock signal.

12. The integrated circuit of claim **11**, further comprising:

a first flip-flop and a second flip-flop,

wherein the first and the second flip-flops are connected to the FIFO circuit,

wherein the first flip-flop is configured to output the first output data as first read data in response to the memory clock signal, and

wherein the second flip-flop is configured to output the second output data as second read data in response to the memory clock signal.

13. The integrated circuit of claim **11**, further comprising:

a third flip-flop configured to output a second enable signal based on a first enable signal in response to the memory clock signal; and

a counter circuit configured to count a number of rising edges of the memory clock signal while the second enable signal is maintained at a logic high level,

wherein the FIFO circuit is further configured to output data corresponding to a pointer signal transmitted from the counter circuit.

14. The integrated circuit of claim **11**, further comprising:

an input/output circuit configured to receive the input data through a first through-silicon via (TSV),

wherein the input/output circuit is configured to control a voltage level of a signal received through the first TSV.

15. The integrated circuit of claim **14**, further comprising:

a first write flip-flop configured to output first write data in response to the rising edge of the memory clock signal;

a second write flip-flop configured to output second write data in response to the rising edge of the memory clock signal; and

a serializer configured to output serial write data based on the first write data and the second write data using a third clock signal,

wherein the input/output circuit is further configured to output the serial write data through a second TSV.

16. A semiconductor device comprising:

a logic die; and

a plurality of memory dies stacked on one surface of the logic die and configured to operate using a plurality of clock signals having different phases,

wherein the logic die comprises:

a deserializer configured to output first parallel data based on input data received from the plurality of memory dies using a first clock signal having a first phase and output second parallel data from the input data using a second clock signal having a second phase, wherein the first phase is different from the second phase;

a delay circuit configured to delay the second clock signal by a first delay time and output a first delay clock signal; and

a first-in first-out (FIFO) circuit configured to:

sample the first parallel data in response to a rising edge of the first delay clock signal and store the sampled first parallel data as first sampling data,

sample the second parallel data in response to the rising edge of the first delay clock signal and store the sampled second parallel data as second sampling data, and

output the first sampling data as first output data and output the second sampling data as second output data in response to a rising edge of a memory clock signal in a FIFO scheme.

17. The semiconductor device of claim **16**,

wherein the plurality of memory dies are connected to the logic die through a plurality of through-silicon vias (TSVs), and

wherein the logic die further comprises an input/output circuit configured to receive the input data through a first TSV.

18. The semiconductor device of claim **17**,

wherein the second clock signal has an anti-phase of the first clock signal, and

wherein the logic die is configured to obtain the first clock signal and the second clock signal through at least a portion of the plurality of TSVs.

19. The semiconductor device of claim **16**,

wherein the logic die further comprises a first flip-flop and a second flip-flop,

wherein the first and the second flip-flops are connected to the FIFO circuit,

wherein the first flip-flop is configured to output the first output data as first read data in response to the memory clock signal, and

wherein the second flip-flop is configured to output the second output data as second read data in response to the memory clock signal.

20. The semiconductor device of claim **19**,

wherein the logic die further comprises:

a controller configured execute one or more instructions which cause the controller to read data from the plurality of memory dies,

a third flip-flop configured to output a second enable signal in response to a first enable signal being input from the controller; and

a fourth flip-flop configured to output a valid signal based on the second enable signal in response to the rising edge of the memory clock signal, and

wherein the controller is further configured to execute the one or more instructions which cause the controller to obtain the first read data and the second read data in response to the valid signal being high.

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