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(54) **SEMICONDUCTOR DEVICE**

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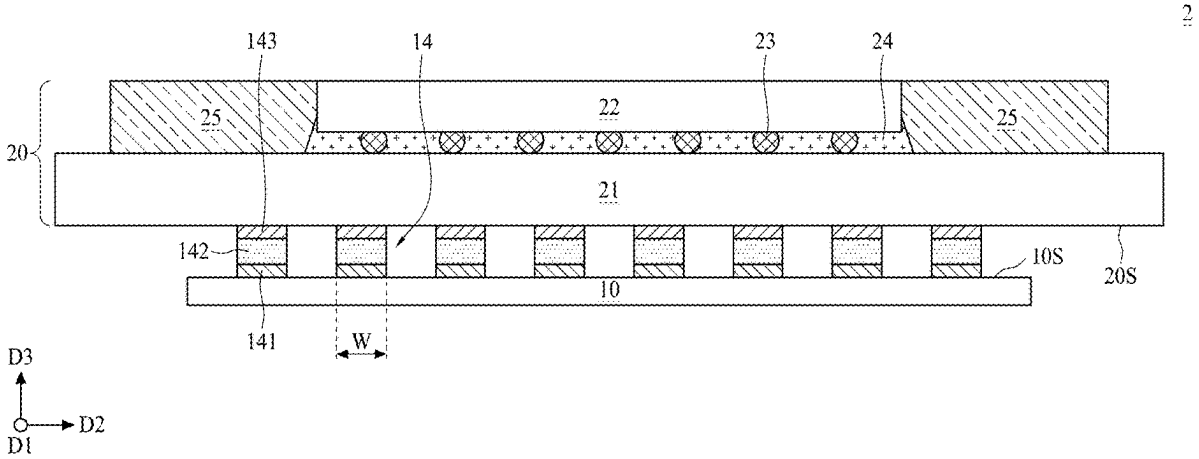
(52) **U.S. Cl.**

CPC ***H01L 25/0657*** (2013.01); ***H01L 23/49833*** (2013.01); ***H01L 23/50*** (2013.01); ***H01L 23/5386*** (2013.01); ***H01L 24/03*** (2013.01); ***H01L 25/16*** (2013.01); ***H01L 25/50*** (2013.01); *H01L 23/13* (2013.01); *H01L 2224/16145* (2013.01); *H01L 2224/16225* (2013.01); *H01L 2224/16227* (2013.01); *H01L 2224/32225* (2013.01); *H01L 2224/73204* (2013.01); *H01L 2225/06513* (2013.01); *H01L 2225/06517* (2013.01); *H01L 2225/06568* (2013.01); *H01L 2225/06572* (2013.01); *H01L 2924/14* (2013.01); *H01L 2924/15159* (2013.01); *H01L 2924/15321* (2013.01); *H01L 2924/181* (2013.01); *H01L 2924/18161* (2013.01); *H01L 2924/19011* (2013.01); *H01L 2924/19104* (2013.01); *H10D 1/716* (2025.01)

(57) **ABSTRACT**

A semiconductor device includes a first electronic component, a second electronic component, a third electronic component, and a plurality of first interconnection structures. The first electronic component is disposed between the second electronic component and the third electronic component. The first interconnection structures are electrically connected to the first electronic component and the second electronic component. Each of the first interconnection structures has a length along a first direction and a width along a second direction substantially perpendicular to the first direction. The length is larger than the width. The third electronic component has a cavity, and the first electronic component is disposed within the cavity.



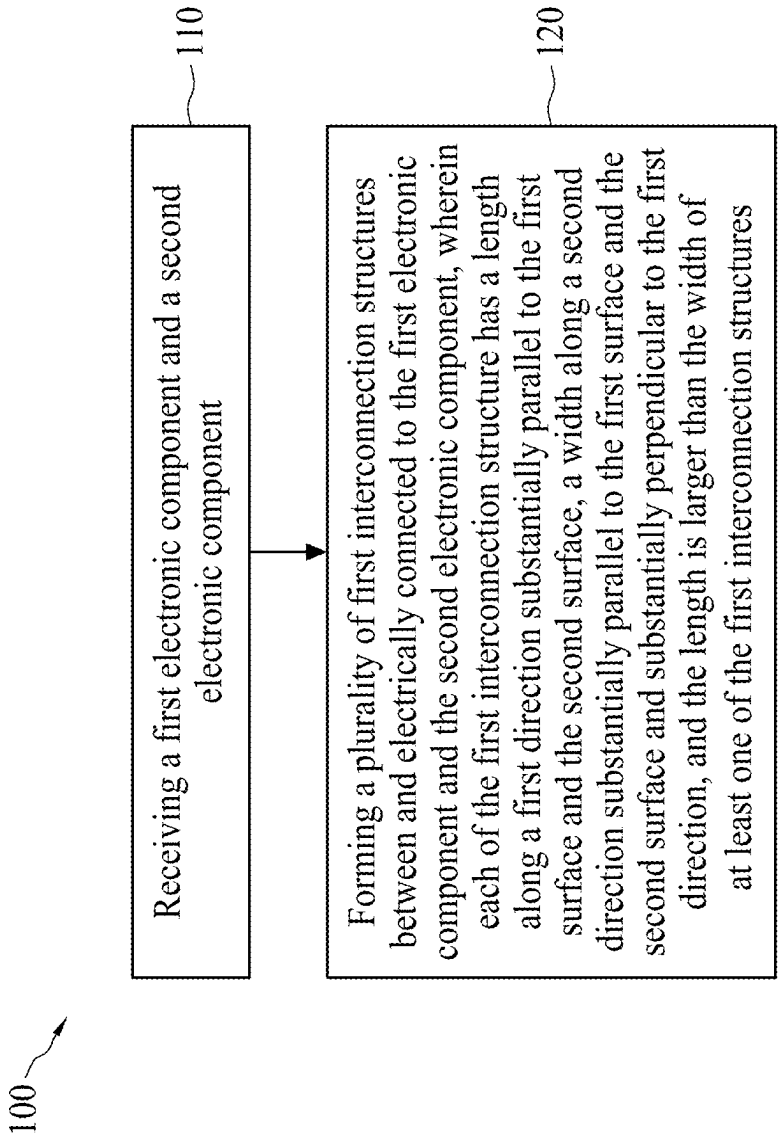

100
110
Receiving a first electronic component and a second electronic component
120
Forming a plurality of first interconnection structures between and electrically connected to the first electronic component and the second electronic component, wherein each of the first interconnection structure has a length along a first direction substantially parallel to the first surface and the second surface, a width along a second direction substantially parallel to the first surface and the second surface and substantially perpendicular to the first direction, and the length is larger than the width of at least one of the first interconnection structures

FIG. 1

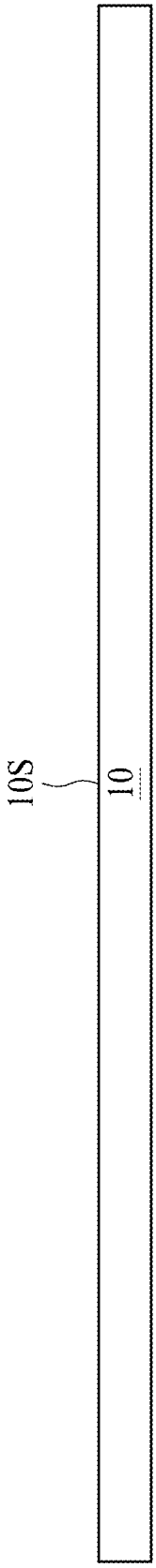


FIG. 2A

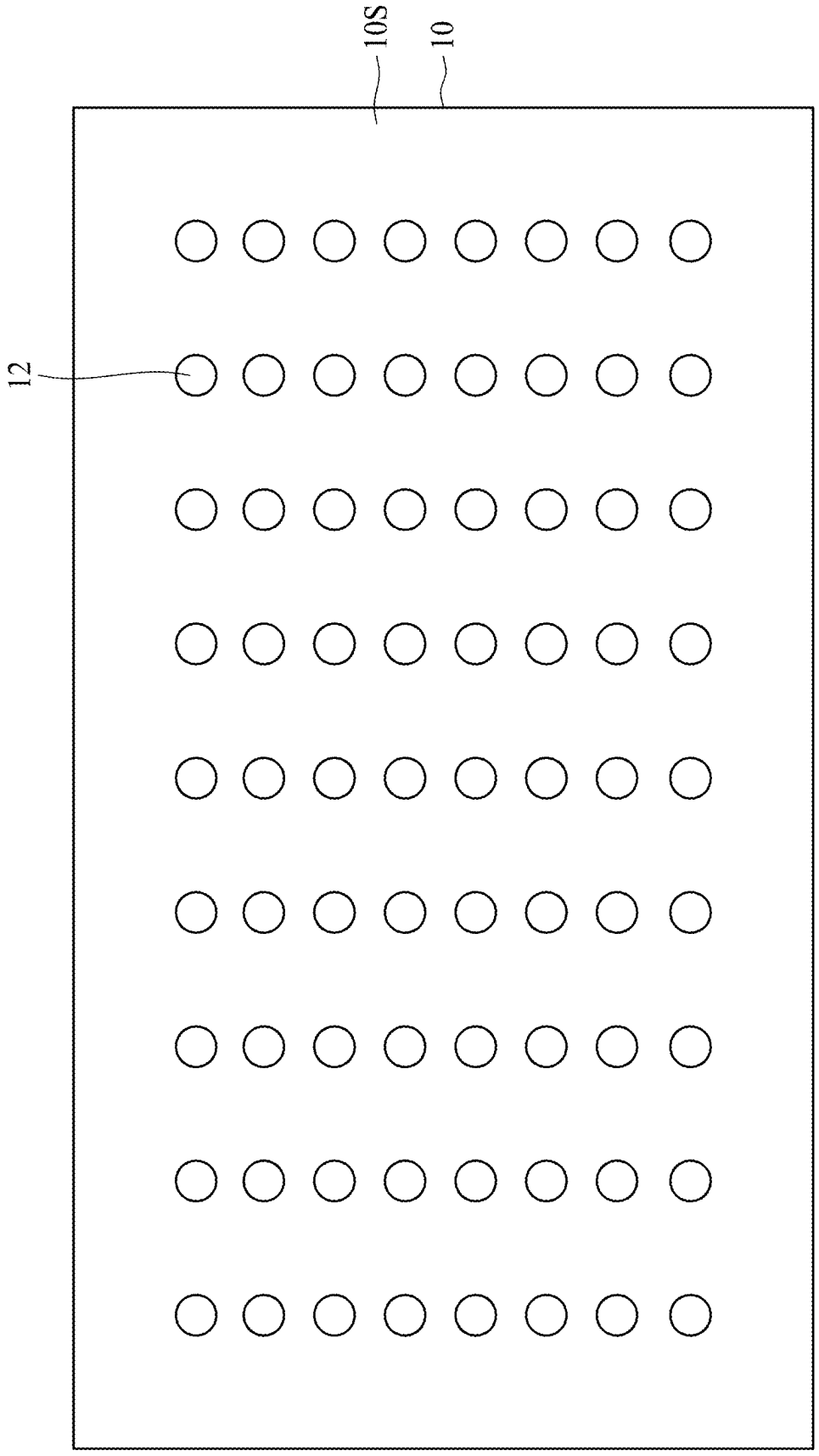


FIG. 2B

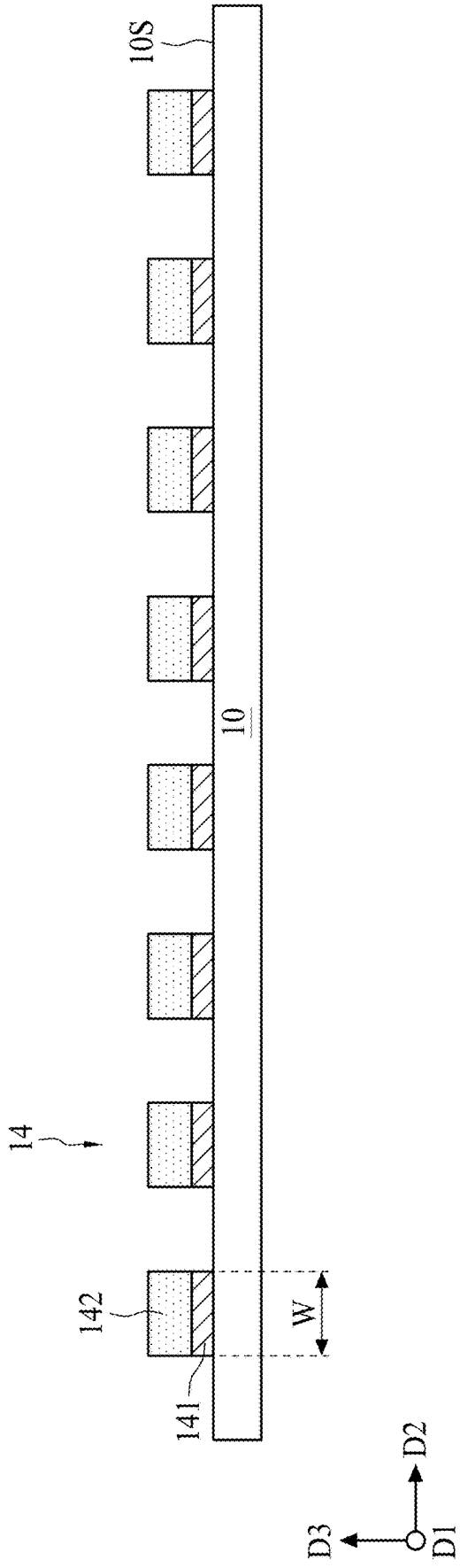


FIG. 2C

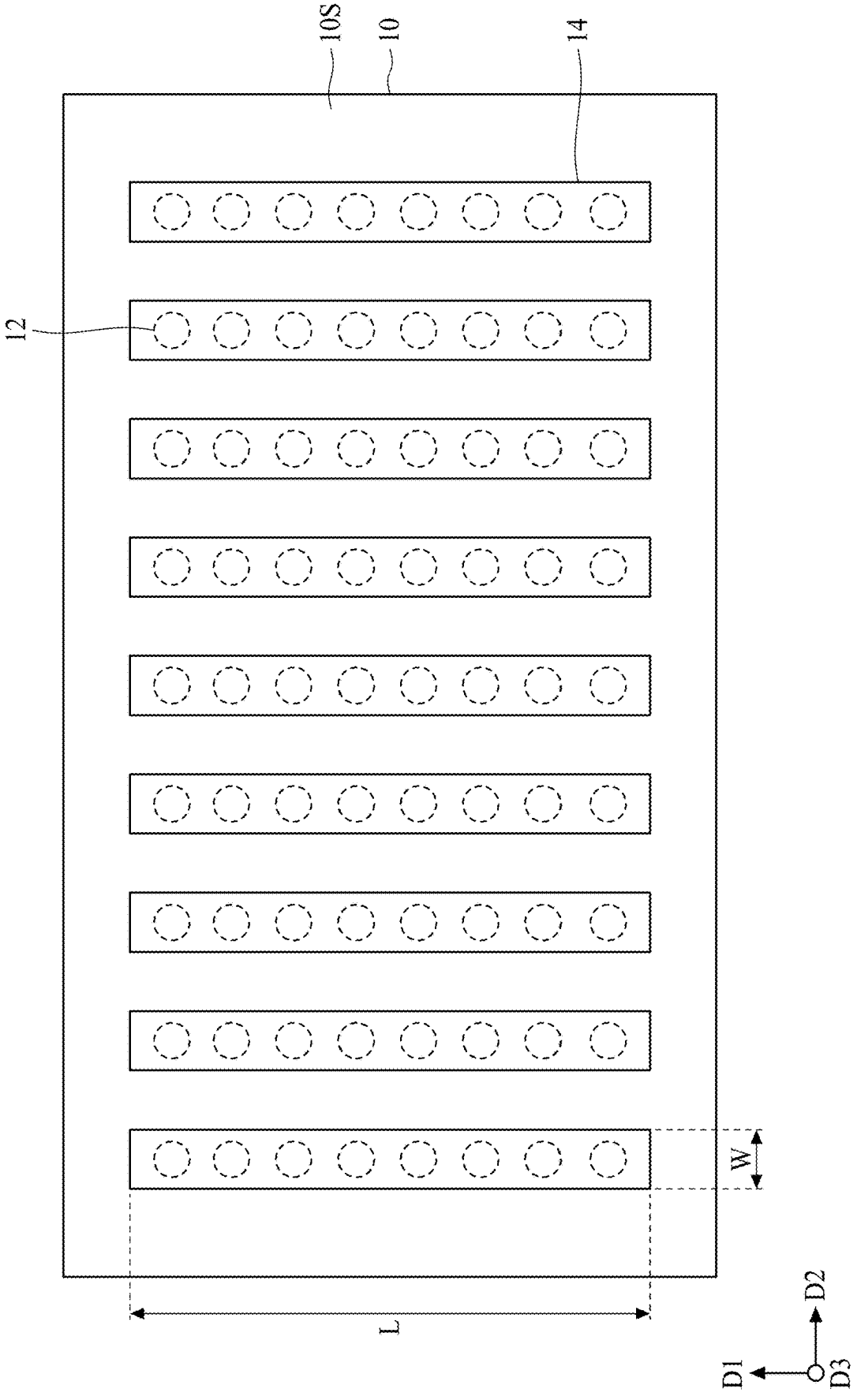


FIG. 2D

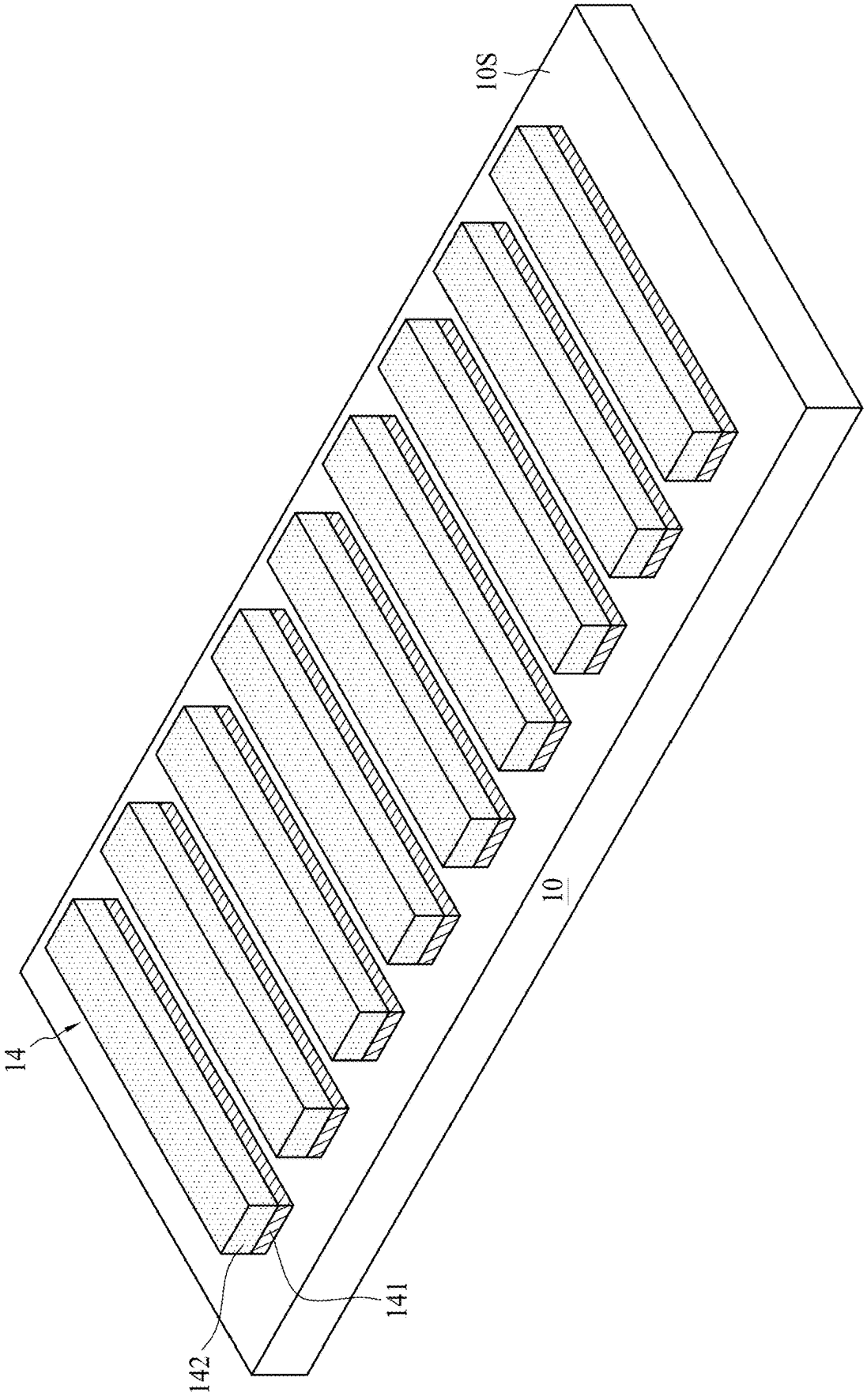


FIG. 2E

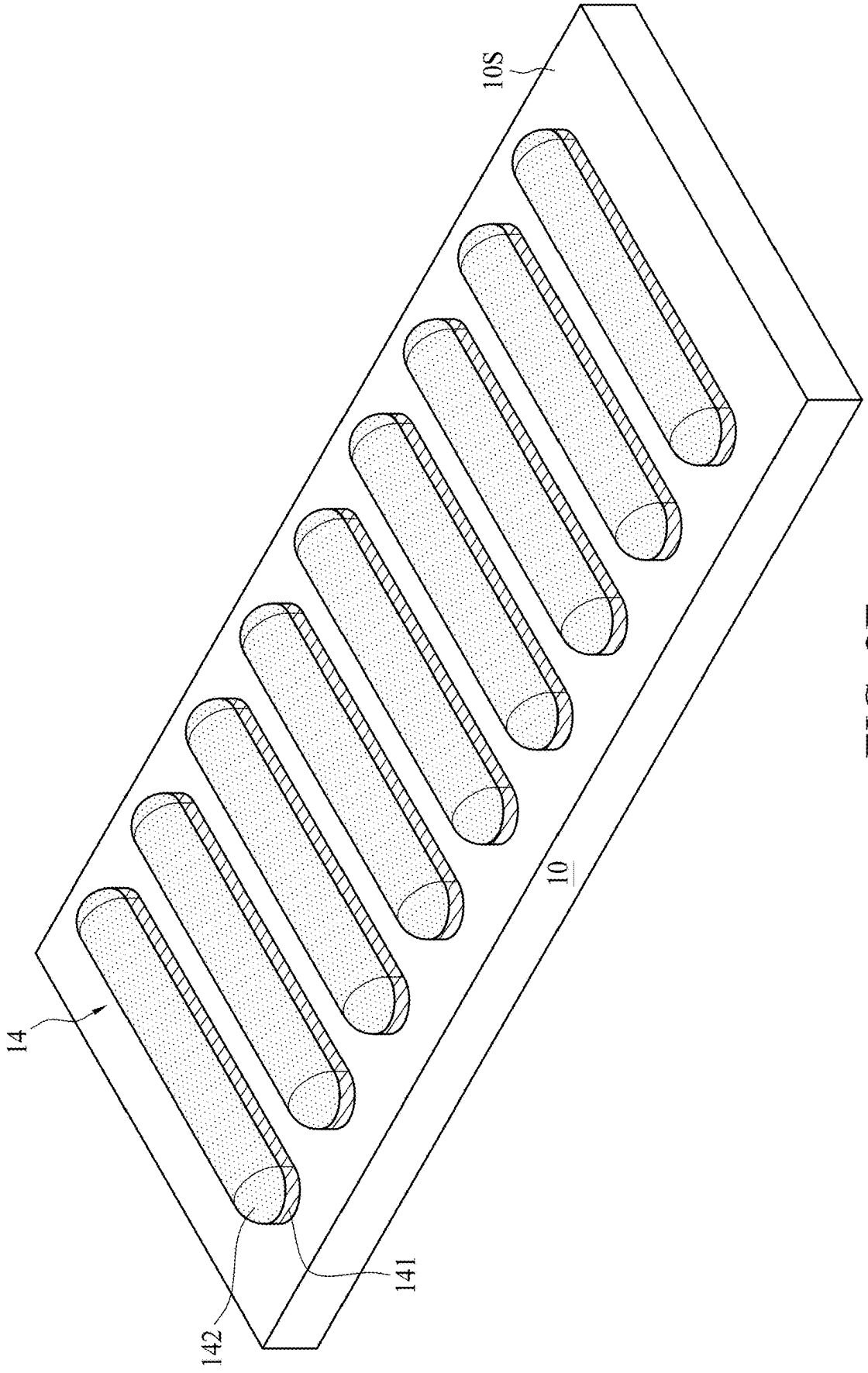


FIG. 2F

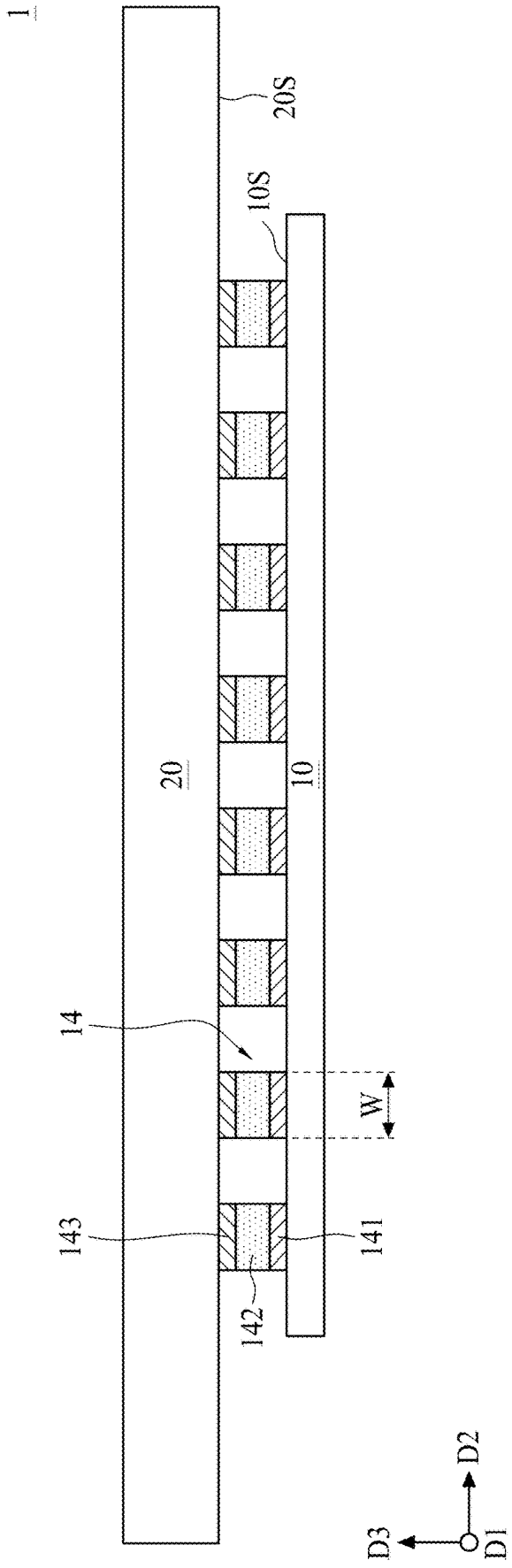


FIG. 2G

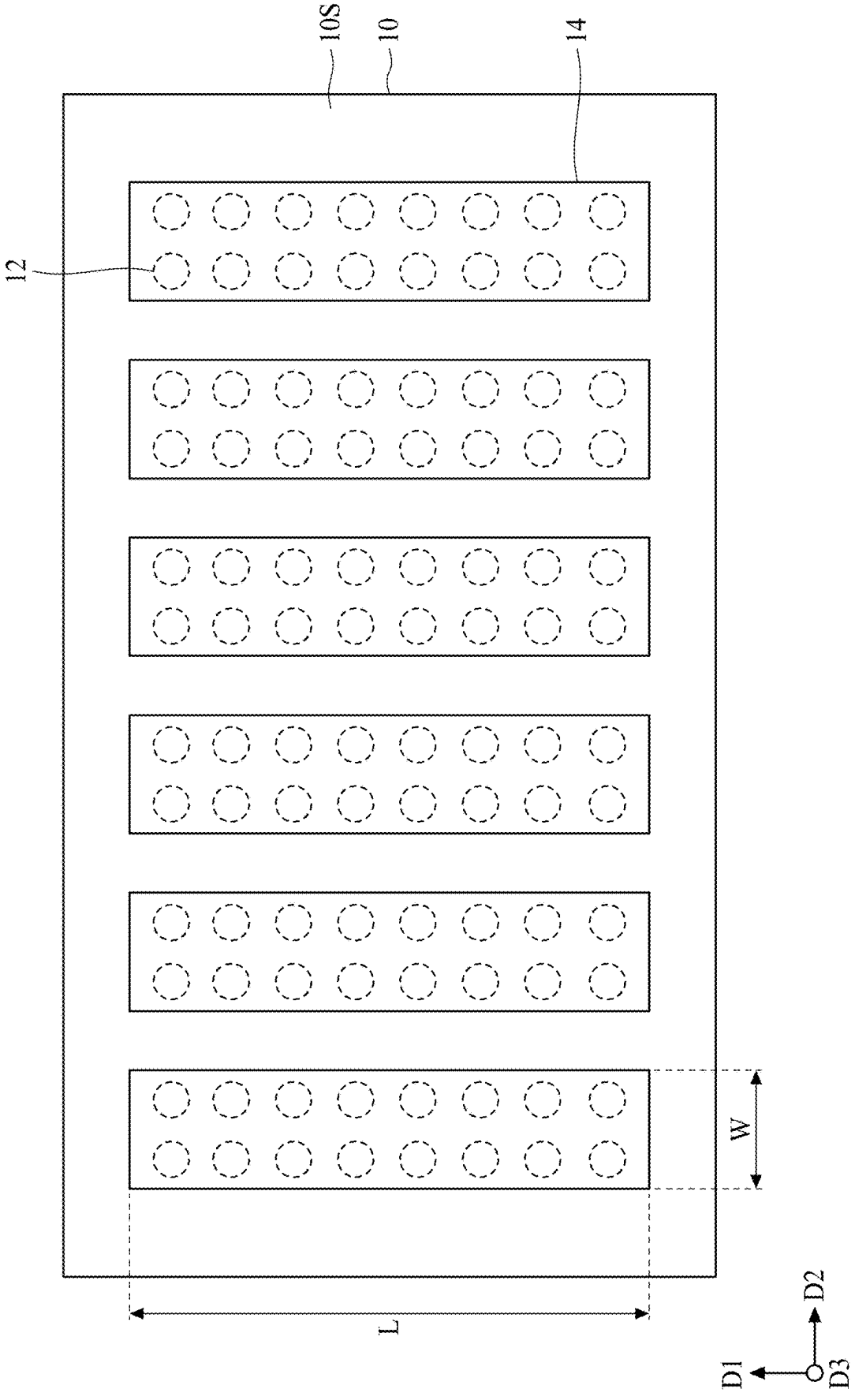


FIG. 3

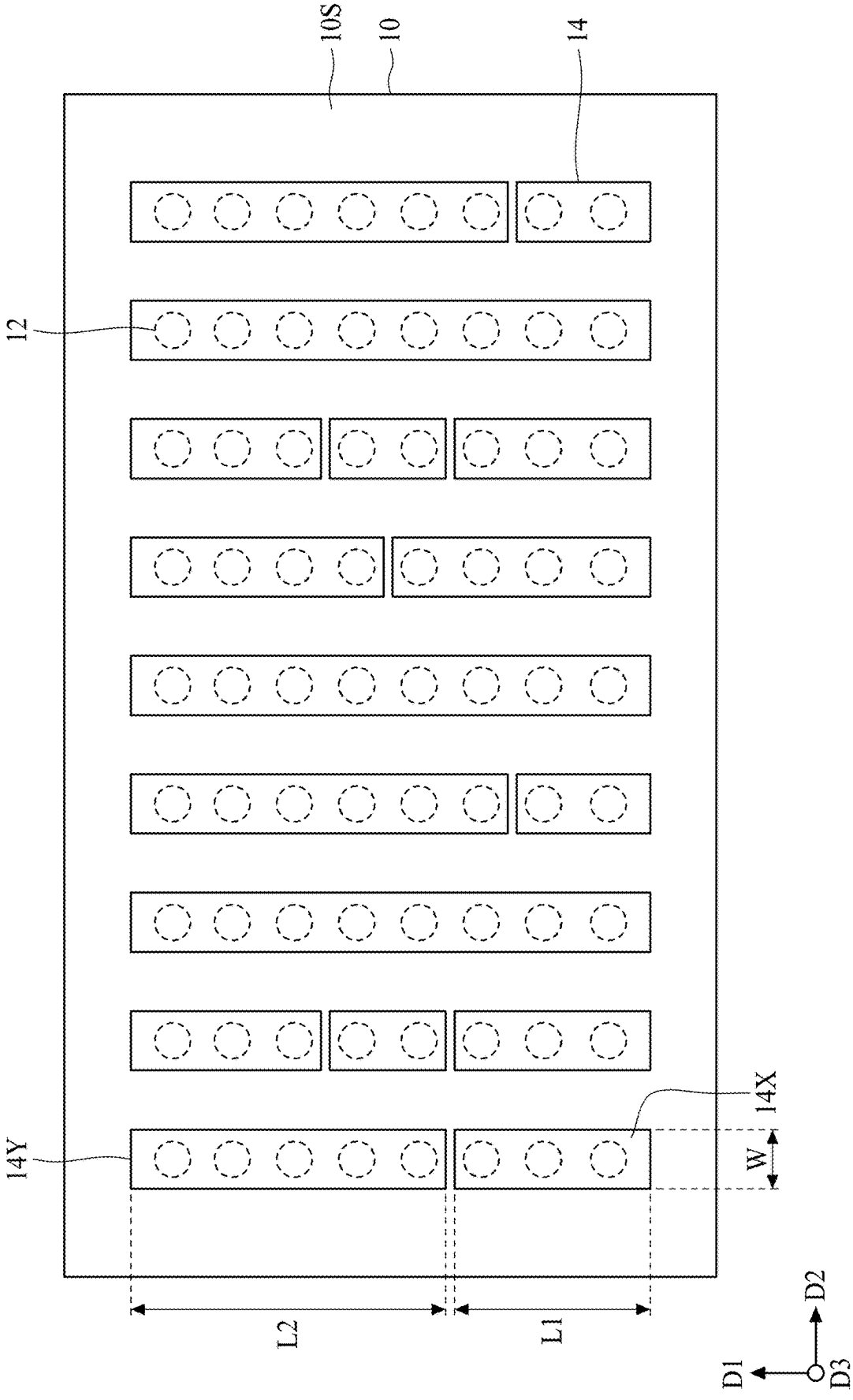


FIG. 4

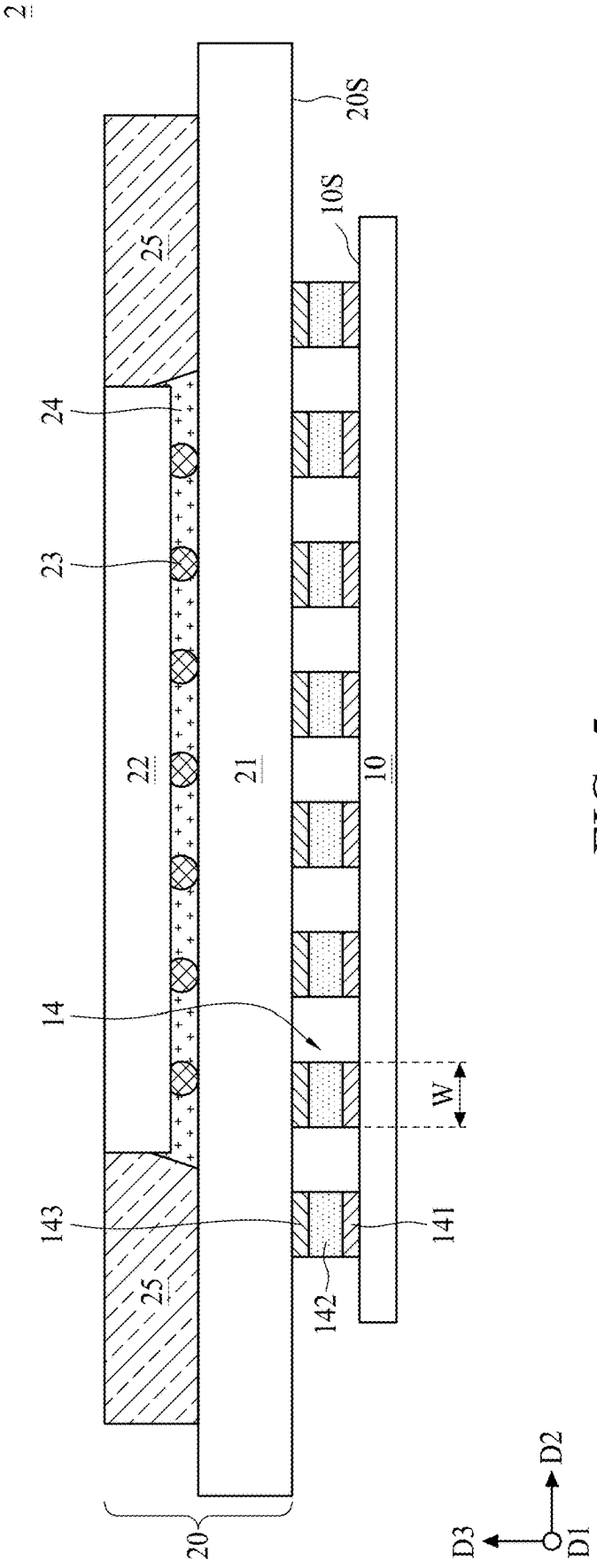


FIG. 5

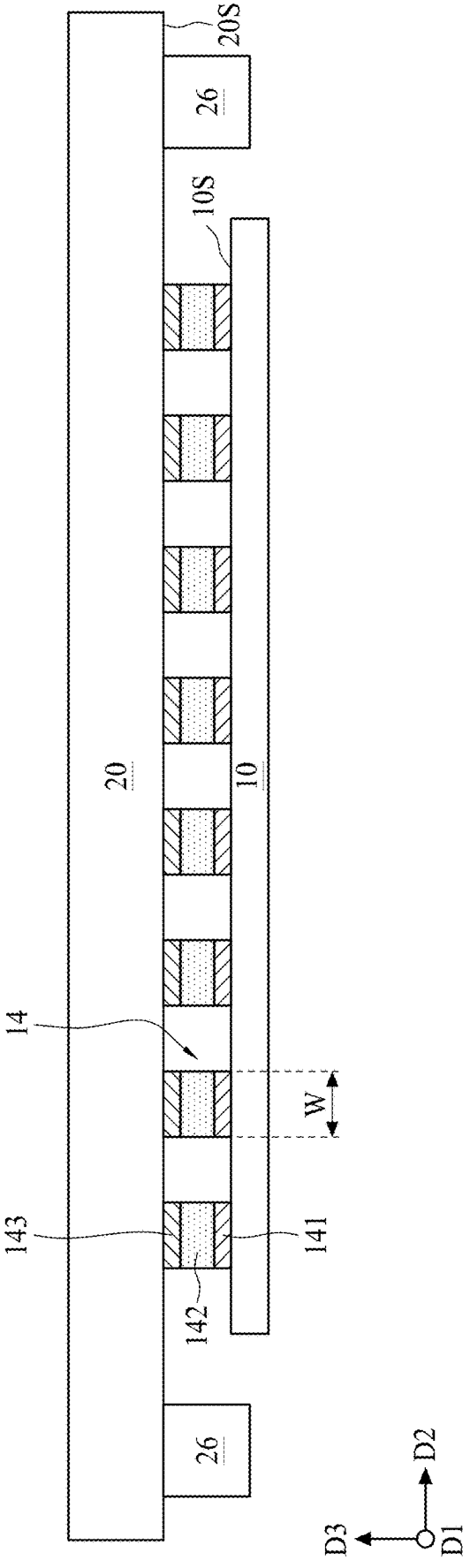


FIG. 6A

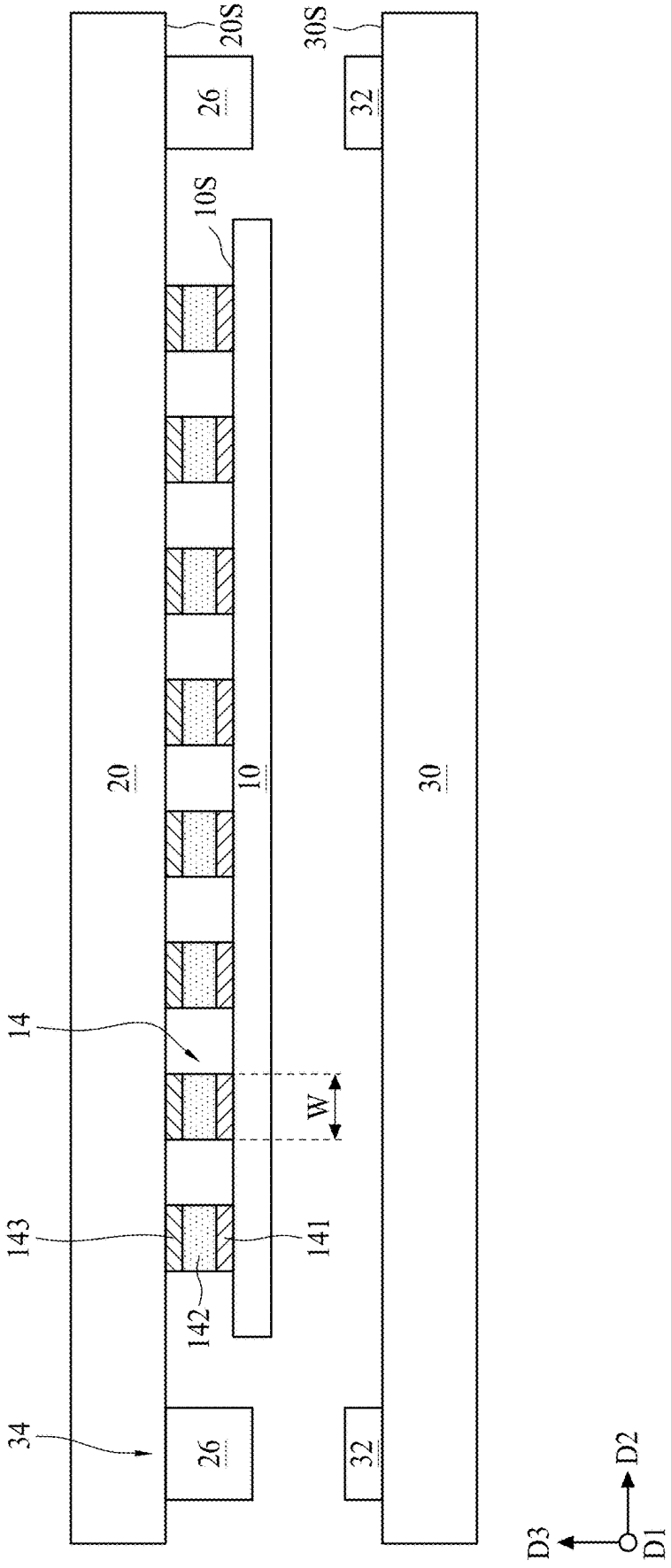


FIG. 6B

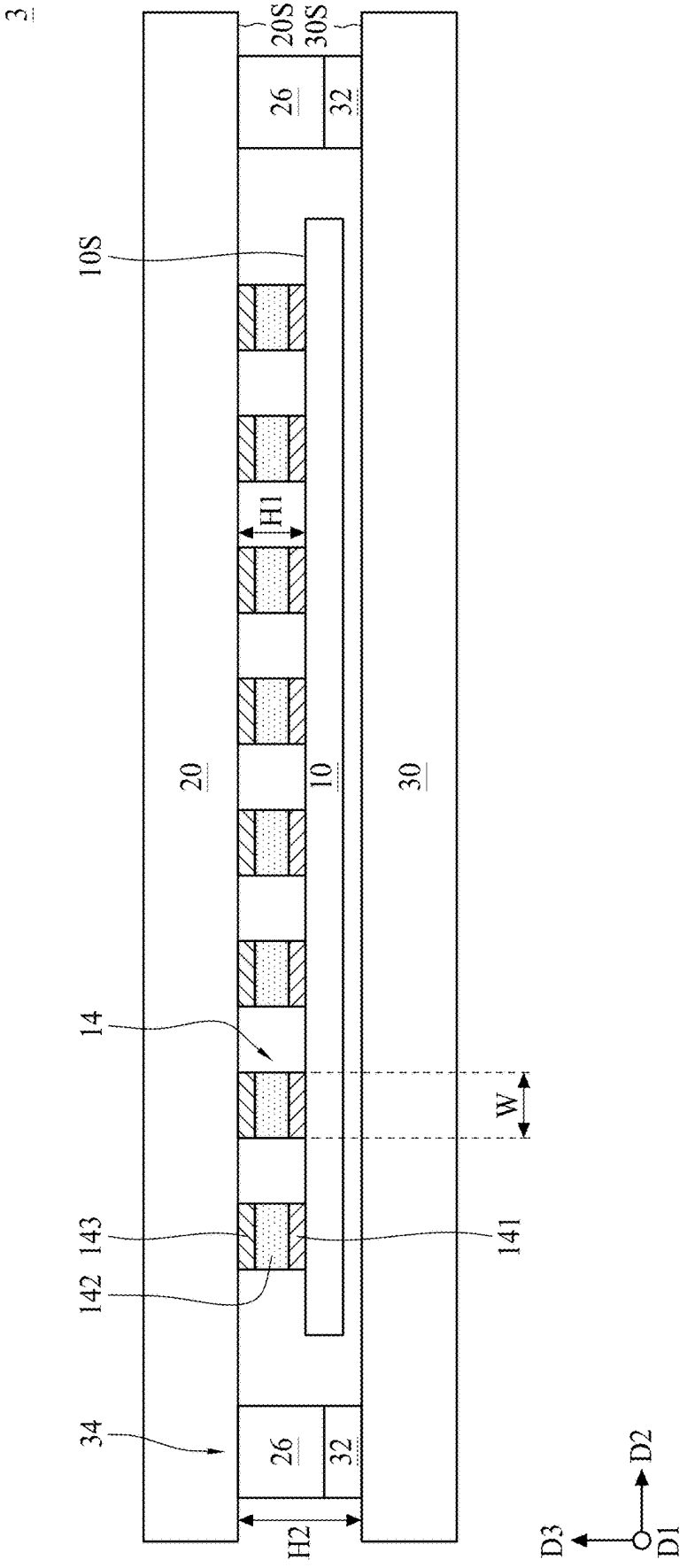


FIG. 6C

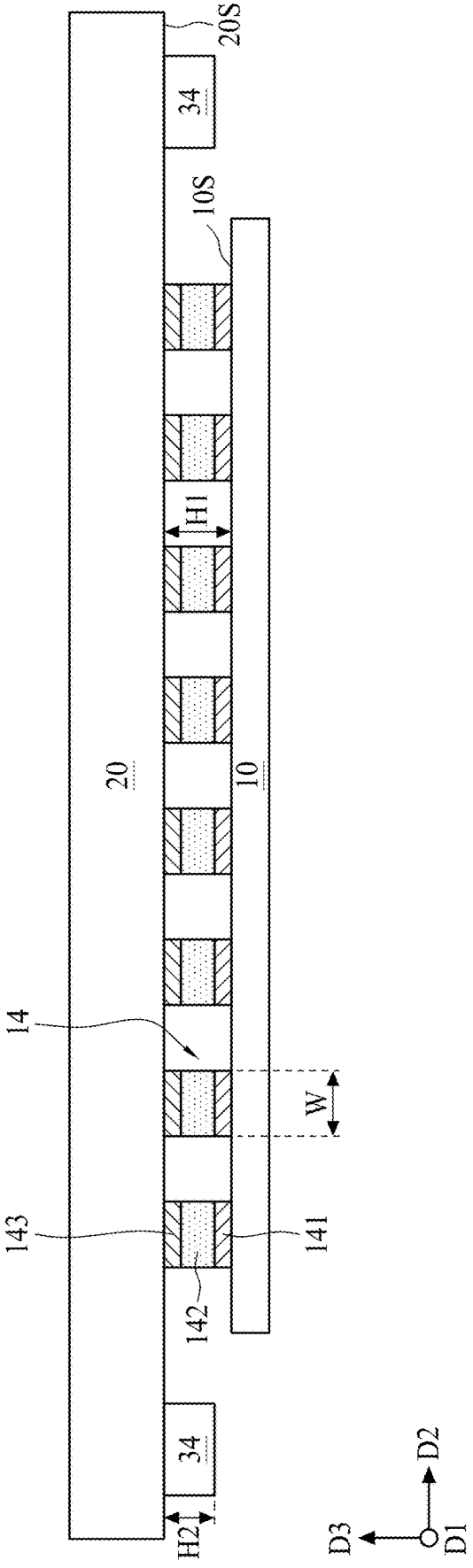


FIG. 7A

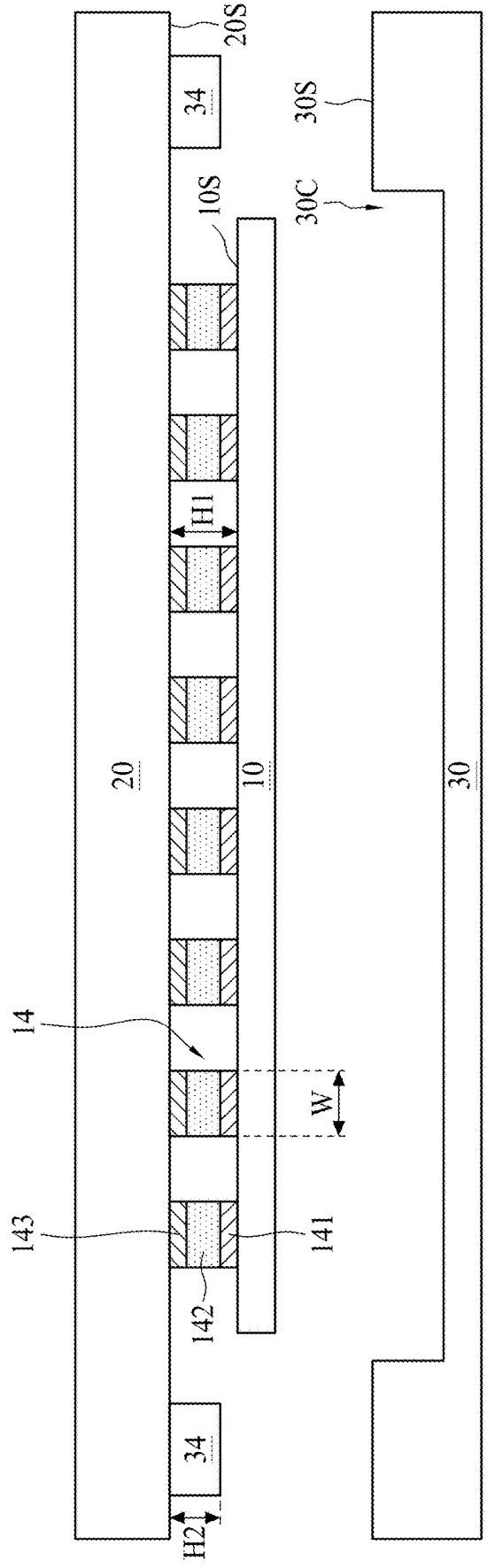


FIG. 7B

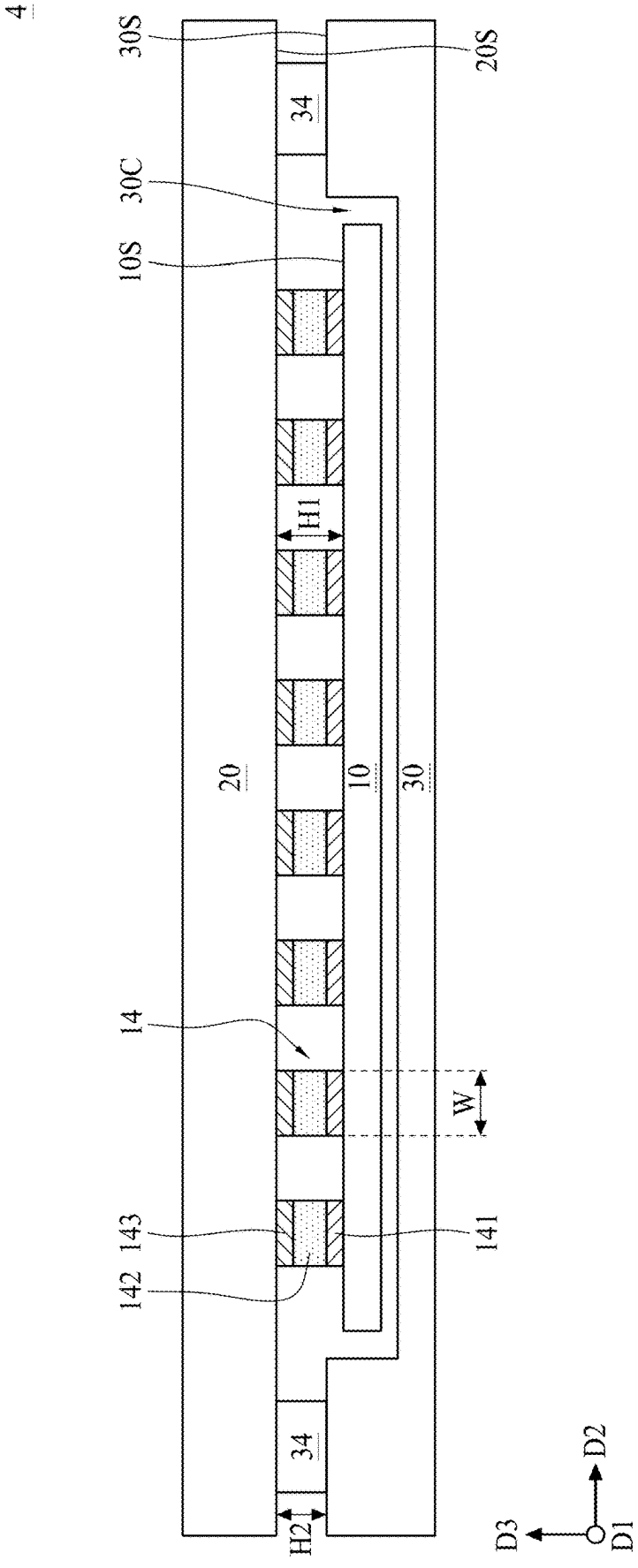


FIG. 7C

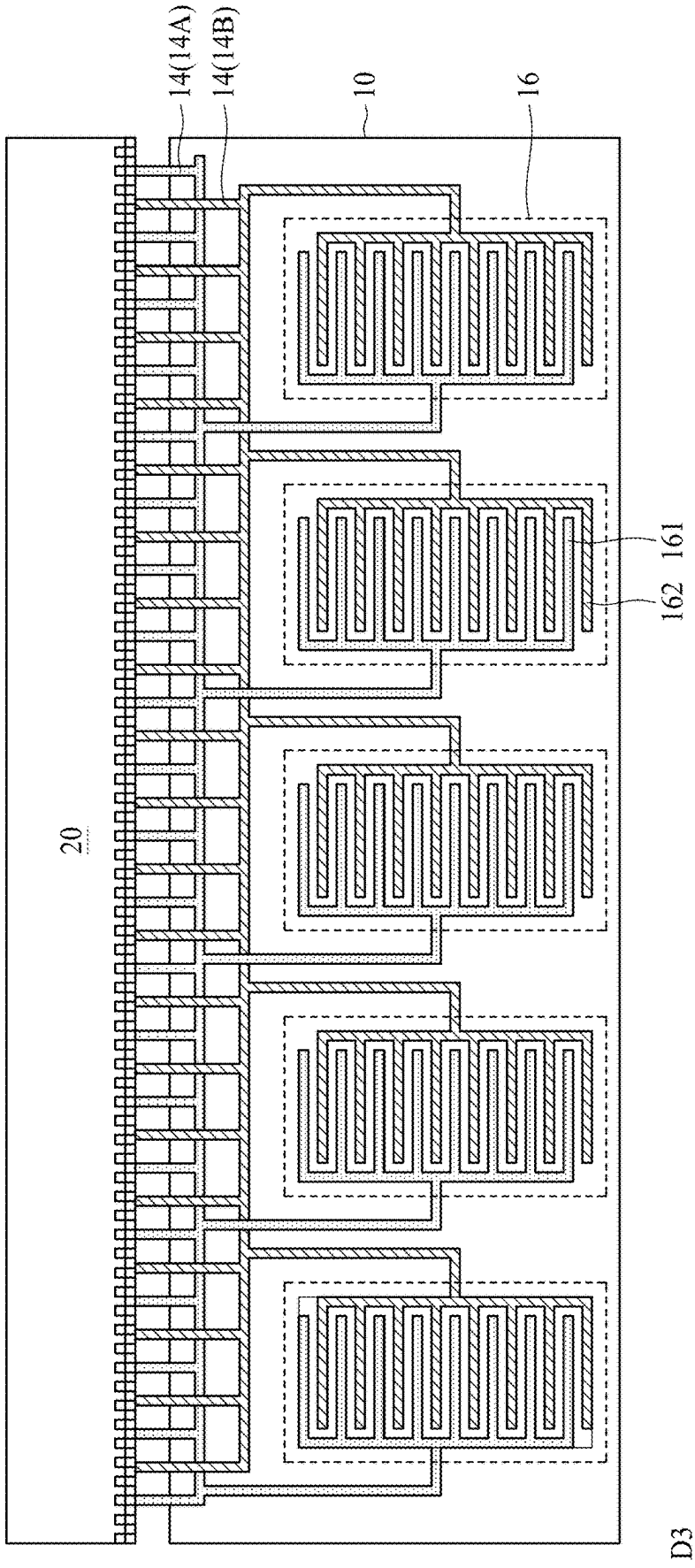


FIG. 8

SEMICONDUCTOR DEVICE

PRIORITY CLAIM AND CROSS-REFERENCE

[0001] This patent is a divisional application of U.S. patent application Ser. No. 18/057,222 filed on Nov. 20, 2022, entitled of "SEMICONDUCTOR DEVICE", which is a divisional application of U.S. patent application Ser. No. 16/716,225 flied on Dec. 16, 2019, entitled of "SEMICONDUCTOR DEVICE", which is a divisional application of U.S. patent application Ser. No. 15/725,240 filed on Oct. 4, 2017, entitled of "SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME", which claims priority of U.S. provisional application Ser. No. 62/522,474 filed on 20 Jun. 2017, the entire contents of all of which are hereby incorporated by reference.

BACKGROUND

[0002] Integrated passive devices (IPDs) are passive devices such as capacitors and inductors that are fabricated in the form of integrated circuit. Recently, the IPDs are employed in SOCs, and built in the package structure. Problems with the integration of IPDs may include, for example, the electrical resistance of the interconnection structures between the IPDs and the active devices being too high, and thus adversely influencing electrical performance of the package structure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Aspects of the embodiments of the present disclosure are best understood from the following detailed description when read with the accompanying figures. It is noted that, in accordance with the standard practice in the industry, various structures are not drawn to scale. In fact, the dimensions of the various structures may be arbitrarily increased or reduced for clarity of discussion.

[0004] FIG. **1** is a flow chart illustrating a method for manufacturing a semiconductor device according to various aspects of one or more embodiments of the present disclosure.

[0005] FIG. **2**A, FIG. **2**B, FIG. **2**C, FIG. **2**D, FIG. **2**E, FIG. **2**F and FIG. **2**G are schematic views at one of various operations of manufacturing a semiconductor device according to one or more embodiments of the present disclosure.

[0006] FIG. **3** is a schematic view at one of various operations of manufacturing a semiconductor device according to one or more embodiments of the present disclosure.

[0007] FIG. **4** is a schematic view at one of various operations of manufacturing a semiconductor device according to one or more embodiments of the present disclosure.

[0008] FIG. **5** is a schematic view of a semiconductor device according to some embodiments of the present disclosure.

[0009] FIG. **6**A, FIG. **6**B and FIG. **6**C are schematic views at one of various operations of manufacturing a semiconductor device according to one or more embodiments of the present disclosure.

[0010] FIG. **7**A, FIG. **7**B and FIG. **7**C are schematic views at one of various operations of manufacturing a semiconductor device according to one or more embodiments of the present disclosure.

[0011] FIG. **8** is a schematic view of a semiconductor device according to one or more embodiments of the present disclosure.

DETAILED DESCRIPTION

[0012] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of elements and arrangements are described below to simplify the present disclosure. These are, of course, merely examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows may include embodiments in which the first and second features are formed in direct contact, and may also include embodiments in which additional features may be formed between the first and second features, such that the first and second features may not be in direct contact. In addition, the present disclosure may repeat reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0013] Further, spatially relative terms, such as "beneath", "below", "lower", "above", "upper", "on" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0014] As used herein, the terms such as "first," "second" and "third" describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms may be only used to distinguish one element, component, region, layer or section from another. The terms such as "first," "second" and "third" when used herein do not imply a sequence or order unless clearly indicated by the context.

[0015] As used herein, the terms "approximately," "substantially," "substantial" and "about" are used to describe and account for small variations. When used in conjunction with an event or circumstance, the terms can refer to instances in which the event or circumstance occurs precisely as well as instances in which the event or circumstance occurs to a close approximation. For example, when used in conjunction with a numerical value, the terms can refer to a range of variation of less than or equal to ±10% of that numerical value, such as less than or equal to ±5%, less than or equal to ±4%, less than or equal to ±3%, less than or equal to ±2%, less than or equal to ±1%, less than or equal to ±0.5%, less than or equal to ±0.1%, or less than or equal to ±0.05%. For example, two numerical values can be deemed to be "substantially" the same or equal if a difference between the values is less than or equal to ±10% of an average of the values, such as less than or equal to ±5%, less than or equal to ±4%, less than or equal to ±3%, less than or equal to ±2%, less than or equal to ±1%, less than or equal to ±0.5%, less than or equal to ±0.1%, or less than or equal to ±0.05%. For example, "substantially" parallel can refer to a range of angular variation relative to 0° that is less than or equal to ±10°, such as less than or equal to ±5°, less than or equal to ±4°, less than or equal to ±3°, less than or equal to ±2°, less than or equal to ±1°, less than or equal to ±0.5°, less than or equal to ±0.1°, or less than or equal to ±0.05°. For

example, "substantially" perpendicular can refer to a range of angular variation relative to 90° that is less than or equal to ±10°, such as less than or equal to ±5°, less than or equal to ±4°, less than or equal to ±3°, less than or equal to ±2°, less than or equal to ±1°, less than or equal to ±0.5°, less than or equal to ±0.1°, or less than or equal to ±0.05°.

[0016] Other features and processes may also be included. For example, testing structures may be included to aid in the verification testing of the 3D packaging or 3DIC devices. The testing structures may include, for example, test pads formed in a redistribution layer or on a substrate that allows the testing of the 3D packaging or 3DIC, the use of probes and/or probe cards, and the like. The verification testing may be performed on intermediate structures as well as the final structure. Additionally, the structures and methods disclosed herein may be used in conjunction with testing methodologies that incorporate intermediate verification of known good dies to increase the yield and decrease costs.

[0017] In one or more embodiments of the present disclosure, a semiconductor device including a bar-shaped interconnection is provided. The bar-shaped interconnection has a length lager than a width. The bar-shaped interconnection is configured to electrically connect two or more electronic components. Each of the bar-shaped interconnection is electrically connected to plural of electrical terminals, and has reduced resistance due to its increased area. Thus, the bar-shaped interconnections help to improve electrical performance of the semiconductor device. In some embodiments of the present disclosure, the interconnection structures covers plural of electrical terminals, which helps to increase the alignment tolerance between the electronic components, and thus the reliability can be increased.

[0018] FIG. **1** is a flow chart illustrating a method for manufacturing a semiconductor device according to various aspects of one or more embodiments of the present disclosure. The method **100** begins with operation **110** in which a first electronic component and a second electronic component are received. The method proceeds with operation **120** in which a plurality of first interconnection structures are formed between and electrically connected to the first electronic component and the second electronic component. Each of the first interconnection structures has a length along a first direction substantially parallel to the first surface and the second surface, a width along a second direction substantially parallel to the first surface and the second surface and substantially perpendicular to the first direction, and the length is larger than the width of at least one of the interconnection structures.

[0019] The method **100** is merely an example, and is not intended to limit the present disclosure beyond what is explicitly recited in the claims. Additional operations can be provided before, during, and after the method **100**, and some operations described can be replaced, eliminated, or moved around for additional embodiments of the method.

[0020] FIG. **2**A, FIG. **2**B, FIG. **2**C, FIG. **2**D, FIG. **2**E, FIG. **2**F and FIG. **2**G are schematic views at one of various operations of manufacturing a semiconductor device according to one or more embodiments of the present disclosure, where FIG. **2**A, FIG. **2**C and FIG. **2**G are cross-sectional views at one of various operations of manufacturing a semiconductor device, FIG. **2**B and FIG. **2**D are top views at one of various operations of manufacturing a semiconductor device, and FIG. **2**E and FIG. **2**F are oblique views at one of various operations of manufacturing a semiconductor device. As depicted in FIG. **2**A, an electronic component such as a first electronic component **10** is received. The first electronic component **10** includes a surface such as a first surface **10**S. In some embodiments, the first electronic component **10** may include an integrated passive device, an active device, an interposer, a package structure, a package substrate, a printed circuit board or the like. In some embodiments, the first electronic component **10** may include one or more integrated passive devices, which are in a form of integrated circuit, such as capacitors, inductors, resistors, or combinations thereof. In some embodiments, the first electronic component **10** may include, but is not limited to, a deep trench capacitor (DTC). As depicted in FIG. **2**B, the first electronic component **10** may include electrical terminals **12** electrically connected to the integrated circuit inside the first electronic component **10** and exposed from the first surface **10**S. By way of example, the electrical terminals **12** may include, but is not limited to, a bonding pad or the like.

[0021] As depicted in FIG. **2**C, FIG. **2**D and FIG. **2**E, a plurality of interconnection structures such as first interconnection structures **14** are formed over the first surface **10**S of the first electronic component **10**. In some embodiments, each of the first interconnection structures **14** has a length L along a first direction D**1** substantially parallel to the first surface **10**S, a width W along a second direction D**2** substantially parallel to the first surface **10**S and substantially perpendicular to the first direction D**1**, and the length L is larger than the width W of at least one or all of the first interconnection structures **14**. In some embodiments, the length L of each of the first interconnection structures **14** is larger than the width W of the respective first interconnection structure **14**. In some embodiments, the ratio of the length L to the width W of at least one of the first interconnection structures **14** is greater than or equal to 2, greater than or equal to 5, or greater than or equal to 10. In some embodiments, the ratio of the length L to the width W of each of the first interconnection structures **14** is greater than or equal to 2, greater than or equal to 5, or greater than or equal to 10.

[0022] In some exemplary embodiments, the length L of at least one or all of the first interconnection structures **14** is larger than or equal to 100 micrometers such as ranging from about 300 micrometers to about 1 millimeter, but is not limited thereto. In some exemplary embodiments, the width W of the first interconnection structure **14** is smaller than or equal to 50 micrometers, but is not limited thereto. In some embodiments, the first interconnection structure **14** covers more than one of the electrical terminals **12** of the first electronic component **10** such that the first interconnection structure **14** is electrically connected to more than one of the electrical terminals **12** of the first electronic component **10**. In some embodiments, each of the first interconnection structures **14** is electrically connected to the electrical terminals **12** arranged in a single column. In some embodiments, the first interconnection structures **14** are arranged in the second direction D**2**, and each of the first interconnection structures **14** are extended along the first direction D**1**.

[0023] In some embodiments, the first interconnection structure **14** includes more than one conductive layers stacked to one another. In some embodiments, the first interconnection structure **14** includes a first conductive layer **141** and a second conductive layer **142** stacked on the first conductive layer **141**. In some embodiments, the first conductive layer **141** may include, but is not limited to, an under

bump metallurgy (UBM) or the like electrically connected to the electrical terminals **12** of the first electronic component **10**. In some embodiments, the second conductive layer **142** may include, but is not limited to, a conductive bump, a conductive ball, a conductive paste or the like electrically connected to the first conductive layer **141**. In some embodiments, the length and width of the first conductive layer **141** and the second conductive layer **142** may be substantially the same, which may be substantially equal to the length L and the width W of the first interconnection structure **14**. In some embodiments, the thickness of the second conductive layer **142** is thicker than that of the first conductive layer **141**. In some embodiments, the ratio of the thickness of the second conductive layer **142** to the thickness of the first conductive layer **141** is larger than or equal to 2, but is not limited thereto. By way of examples, the thickness of the second conductive layer **142** is ranging from about 15 micrometers to about 50 micrometers such as about 25 micrometers, but not limited thereto. By way of examples, the thickness of the first conductive layer **141** is ranging from about 5 micrometers to about 15 micrometers such as 10 micrometers, but not limited thereto. As depicted in FIG. **2**F, a reflow operation may be carried out on the second conductive layer **142**.

[0024] As depicted in FIG. **2**G, another electronic component such as a second electronic component **20** is received. The second electronic component **20** includes a surface such as a second surface **20**S. In some embodiments, the second electronic component **20** may include an integrated passive device, an active device, an interposer, a package structure, a package substrate, a printed circuit board or the like. In some embodiments, the second electronic component **20** may include an active device such as a logic device or the like. In some embodiments, the second electronic component **20** includes third conductive layers **143** formed over the second surface **20**S. In some embodiments, the length and the width of the third conductive layer **143** are substantially equal to that of the first conductive layer **141** and the second conductive layer **142**. In some embodiments, the third conductive layer **143** may include, but is not limited to, an under bump metallurgy (UBM) or the like electrically connected to the second electronic component **20**. In some embodiments, the thickness of the third conductive layer **143** is ranging from about **3** micrometers to about 10 micrometers such as about 5 micrometers, but is not limited thereto. The second electronic component **20** and the first electronic component **10** are oriented with the second surface **20**S facing the first surface **10**S. The third conductive layers **143** are then coupled to respective second conductive layers **142** and first conductive layers **141** to form a plurality of first interconnection structures **14** stacked by the first conductive layer **141**, the second conductive layer **142** and the third conductive layer **143**. Accordingly, the second electronic component **20** and the first electronic component **10** are electrically connected through the first interconnection structures **14**, forming a semiconductor device **1**.

[0025] In some embodiments of the present disclosure, the first interconnection structures **14** are bar-shaped interconnections, and each of which electrically connected to plural of electrical terminals **12**. The bar-shaped interconnection has increased cross-sectional area perpendicular to the direction of current flow between the first electronic component **10** and the second electronic component **20**, i.e. the third direction D**3**, and thus the resistance of the interconnection between the first electronic component **10** and the second electronic component **20** is reduced. Thus, the bar-shaped interconnections help to improve electrical performance of the semiconductor device **1**. In some embodiments of the present disclosure, the first interconnection structures **14** covers plural of electrical terminals **12**, and thus help to increase the alignment tolerance between the first electronic component **10** and the second electronic component **20**.

[0026] FIG. **3** is a schematic view at one of various operations of manufacturing a semiconductor device according to one or more embodiments of the present disclosure. In contrast to FIG. **2**D, each of the first interconnection structures **14** is electrically connected to the electrical terminals **12** arranged in an array of a plurality of columns and rows as depicted in FIG. **3**. In some embodiments, the first interconnection structures **14** covers more electrical terminals **12**, and thus help to increase the alignment tolerance between the first electronic component **10** and the second electronic component **20**.

[0027] FIG. **4** is a schematic view at one of various operations of manufacturing a semiconductor device according to one or more embodiments of the present disclosure. In contrast to FIG. **2**D, at least one of the first interconnection structures **14** may include segmented interconnection structures such as a first segmented interconnection structure **14**X, and a second segmented interconnection structure **14**Y. In some embodiments, the first segmented interconnection structure **14**X has a length L**1** along the first direction D**1**, and the second segmented interconnection structure **14**Y has a length L**2** along the first direction D**1**. In some embodiments, the length L**1** may be different from the length L**2**. In some embodiments, the first segmented interconnection structure **14**X and the second segmented interconnection structure **14**Y may be electrically disconnected from each other.

[0028] The semiconductor device and its manufacturing method of the present disclosure are not limited to the above-mentioned embodiments, and may have other different embodiments. To simplify the description and for the convenience of comparison between each of the embodiments of the present disclosure, the identical components in each of the following embodiments are marked with identical numerals. For making it easier to compare the difference between the embodiments, the following description will detail the dissimilarities among different embodiments and the identical features will not be redundantly described.

[0029] FIG. **5** is a schematic view of a semiconductor device according to some embodiments of the present disclosure. As depicted in FIG. **5**, in contrast to the semiconductor device **1** of FIG. **2**G, the semiconductor device **2** may include a chip on wafer on substrate (CoWoS) package structure, and the second electronic component **20** of the semiconductor device **2** may include a chip on wafer (CoW) die. In some embodiments, the second electronic component **20** includes an interposer **21**, one or more semiconductor dies **22**, conductors **23**, an underfill layer **24** and an encapsulant **25**. In some embodiments, the interposer **21** may include through vias such as through substrate vias (TSVs) or the like electrically connected to the conductors **23** disposed over the interposer **21** and the first interconnection structures **14** under the interposer **21**. In some embodiments, the semiconductor die **22** is disposed over the interposer **21**, and electrically connected to the interposer **21** through the

conductors **23**. In some embodiments, the conductors **23** may include, but are not limited to be, conductive bumps, conductive pastes, conductive balls or the like. In some embodiments, the underfill layer **24** is disposed between the semiconductor die **22** and the interposer **21** and encloses the conductors **23**. In some embodiments, the encapsulant **25** such as a molding compound may encapsulate at least a portion of the semiconductor die **22**.

[0030] The features of the first interconnection structure **14** of the semiconductor device **2** may be similar to that of the semiconductor device **1**, and are shown in FIG. **2**D, FIG. **2**E and FIG. **2**F in some exemplary examples, or shown in FIG. **3** and FIG. **4** in some alternative exemplary examples. In some embodiments, the length L of at least one of the first interconnection structures **14** is larger than the width W of the respective first interconnection structure **14**. In some embodiments, the ratio of the length L to the width W of at least one of the first interconnection structures **14** is greater than or equal to 2, greater than or equal to 5, or greater than or equal to 10. In some exemplary embodiments, the length L of the first interconnection structure **14** is larger than or equal to 100 micrometers such as ranging from about 300 micrometers to about 1 millimeter, but is not limited thereto. In some exemplary embodiments, the width W of the first interconnection structure **14** is smaller than or equal to 50 micrometers, but is not limited thereto. In some embodiments, the first interconnection structure **14** covers more than one of the electrical terminals **12** of the first electronic component **10** such that the first interconnection structure **14** is electrically connected to more than one of the electrical terminals **12** of the first electronic component **10**. In some embodiments, each of the first interconnection structures **14** is electrically connected to the electrical terminals **12** arranged in a single column as shown in FIG. **2**D. In some embodiments, each of the first interconnection structures **14** is electrically connected to the electrical terminals **12** arranged in an array of a plurality of columns and rows as depicted in FIG. **3**. In some embodiments, at least one of the first interconnection structures **14** may include segmented interconnection structures as depicted in FIG. **4**.

[0031] FIG. **6**A, FIG. **6**B and FIG. **6**C are schematic views at one of various operations of manufacturing a semiconductor device according to one or more embodiments of the present disclosure. In some embodiments, the manufacturing of a semiconductor device of FIG. **6**A, FIG. **6**B and FIG. **6**C may be implemented followed by FIG. **2**G. As depicted in FIG. **6**A, a plurality of first conductive structures **26** may be formed over the surface **20**S of the second electronic component **20**. In some embodiments, the first conductive structures **26** may be formed before the second electronic component **20** and the first electronic component **10** are connected. In some embodiments, the first conductive structure **26** may include, but is not limited to, a bonding pad, a UBM, a conductive bump, a conductive ball, a conductive paste, the like or combinations thereof electrically connected to the second electronic component **20**.

[0032] As depicted in FIG. **6**B, a third electronic component **30** is received. The third electronic component **30** includes a surface such as a third surface **30**S. In some embodiments, the third electronic component **30** may include an integrated passive device, an active device, an interposer, a package structure, a package substrate, a printed circuit board or the like. In some embodiments, the third electronic component **30** may include, but is not limited to a package substrate or the like. In some embodiments, the third electronic component **30** may further include a plurality of second conductive structures **32** over the surface **30**S. In some embodiments, the second conductive structures **32** may include, but are not limited to a bonding pad, a UBM, a conductive bump, a conductive ball, a conductive paste, the like or combinations thereof electrically connected to the third electronic component **30**.

[0033] As depicted in FIG. **6**C, the second electronic component **20** and the third electronic component **30** are oriented with the second surface **20**S facing the third surface **30**S. The first conductive structures **26** are then coupled to the respective second conductive structures **32** to form a plurality of second interconnection structures **34**, and the second electronic component **20** and the third electronic component **30** are electrically connected through the second interconnection structures **34** to form a semiconductor device **3**. In some embodiments, the height H**2** of the second interconnection structure **34** is larger than the height H**1** of the first interconnection structure **14** such that the first electronic component **10** is apart from the third electronic component **30**.

[0034] The features of the first interconnection structure **14** of the semiconductor device **3** may be similar to that of the semiconductor device **1**, and are shown in FIG. **2**D, FIG. **2**E and FIG. **2**F for example. In some embodiments, the length L of at least one of the first interconnection structures **14** is larger than the width W of the respective first interconnection structure **14**. In some embodiments, the ratio of the length L to the width W of at least one of the first interconnection structures **14** is greater than or equal to 2, greater than or equal to 5, or greater than or equal to 10. In some exemplary embodiments, the length L of the first interconnection structure **14** is larger than or equal to 100 micrometers such as ranging from about 300 micrometers to about 1 millimeter, but is not limited thereto. In some exemplary embodiments, the width W of the first interconnection structure **14** is smaller than or equal to 50 micrometers, but is not limited thereto. In some embodiments, the first interconnection structure **14** covers more than one of the electrical terminals **12** of the first electronic component **10** such that the first interconnection structure **14** is electrically connected to more than one of the electrical terminals **12** of the first electronic component **10**. In some embodiments, each of the first interconnection structures **14** is electrically connected to the electrical terminals **12** arranged in a single column as shown in FIG. **2**D. In some embodiments, each of the first interconnection structures **14** is electrically connected to the electrical terminals **12** arranged in an array of a plurality of columns and rows as depicted in FIG. **3**. In some embodiments, at least one of the first interconnection structures **14** may include segmented interconnection structures as depicted in FIG. **4**.

[0035] FIG. **7**A, FIG. **7**B and FIG. **7**C are schematic views at one of various operations of manufacturing a semiconductor device according to one or more embodiments of the present disclosure. In some embodiments, the manufacturing of a semiconductor device of FIG. **7**A, FIG. **7**B and FIG. **7**C may be implemented followed by FIG. **2**G. As depicted in FIG. **7**A, a plurality of second interconnection structures **34** may be formed over the surface **20**S of the second electronic component **20**. In some embodiments, the second interconnection structures **34** may be formed before the second electronic component **20** and the first electronic

component **10** are connected. In some embodiments, second interconnection structure **34** may include, but is not limited to, a bonding pad, a UBM, a conductive bump, a conductive ball, a conductive paste, the like or combinations thereof electrically connected to the second electronic component **20**. In some embodiments, the height H**2** of the second interconnection structure **34** may be smaller than the height H**1** of the first interconnection structure **14**.

[0036] As depicted in FIG. **7**B, a third electronic component **30** is received. The third electronic component **30** includes a surface such as a third surface **30**S. In some embodiments, the third electronic component **30** may include, but is not limited to, a package substrate, a printed circuit or the like. In some embodiments, the third electronic component **30** may further include a plurality of conductive structures (not shown) over the surface **30**S configured to electrically connect the second interconnection structures **34** of the second electronic component **20**. In some embodiments, the third electronic component **30** of the semiconductor device **4** may include a cavity **30**C recessed from the third surface **30**S and configured to accommodate the first electronic component **10** such that the first electronic component **10** may not be in contact with the third electronic component **30** after the second electronic component **20** and the third electronic component **30** are coupled.

[0037] As depicted in FIG. **7**C, the second electronic component **20** and the third electronic component **30** are oriented with the second surface **20**S facing the third surface **30**S. The second interconnection structures **34** are then coupled to and electrically connected to the third electronic component **30** to form a semiconductor device **4**.

[0038] The features of the first interconnection structure **14** of the semiconductor device **4** may be similar to that of the semiconductor device **1**, and are shown in FIG. **2**D, FIG. **2**E and FIG. **2**F for example. In some embodiments, the length L of at least one of the first interconnection structures **14** is larger than the width W of the respective first interconnection structure **14**. In some embodiments, the ratio of the length L to the width W of at least one of the first interconnection structures **14** is greater than or equal to 2, greater than or equal to 5, or greater than or equal to 10. In some exemplary embodiments, the length L of the first interconnection structure **14** is larger than or equal to 100 micrometers such as ranging from about 300 micrometers to about 1 millimeter, but is not limited thereto. In some exemplary embodiments, the width W of the first interconnection structure **14** is smaller than or equal to 50 micrometers, but is not limited thereto. In some embodiments, the first interconnection structure **14** covers more than one of the electrical terminals **12** of the first electronic component **10** such that the first interconnection structure **14** is electrically connected to more than one of the electrical terminals **12** of the first electronic component **10**. In some embodiments, each of the first interconnection structures **14** is electrically connected to the electrical terminals **12** arranged in a single column as shown in FIG. **2**D. In some embodiments, each of the first interconnection structures **14** is electrically connected to the electrical terminals **12** arranged in an array of a plurality of columns and rows as depicted in FIG. **3**. In some embodiments, at least one of the first interconnection structures **14** may include segmented interconnection structures as depicted in FIG. **4**.

[0039] FIG. **8** is a schematic view of a semiconductor device according to one or more embodiments of the present disclosure. As depicted in FIG. **8**, the semiconductor device **5** may include a first set **14**A and a second set **14**B of the first interconnection structures **14**. In some embodiments, the first interconnection structures **14** of the first set **14**A are electrically connected to each other, and the first interconnection structures **14** of the second set **14**B are electrically connected to each other. In some embodiments, the interconnection structures **14** of the first set **14**A and the second set **14**B are arranged alternately in the second direction D**2** but electrically disconnected from one another. In some embodiments, the first electronic component **10** includes a plurality of deep trench capacitors **16**, and each of which includes first electrodes **161** and second electrodes **162** overlapping to each other. In some embodiments, the first electrodes **161** of the deep trench capacitors **16** are electrically connected to the second electronic component **20** through the first set **14**A of the first interconnection structures **14**, while the second electrodes **162** of the deep trench capacitors **16** are electrically connected to the second electronic component **20** through the second set **14**B of the first interconnection structures **14**.

[0040] In some embodiments of the present disclosure, the bar-shaped interconnection is configured to electrically connect two or more electronic components. Each of the bar-shaped interconnection is electrically connected to plural of electrical terminals, and has reduced resistance due to its increased area. Thus, the bar-shaped interconnections help to improve electrical performance of the semiconductor device. In some embodiments of the present disclosure, the interconnection structures covers plural of electrical terminals, which helps to increase the alignment tolerance between the electronic components, and thus the reliability can be increased.

[0041] In one exemplary aspect, a semiconductor device is provided. The semiconductor device includes a first electronic component, a second electronic component, a third electronic component, a plurality of first interconnection structures, and a plurality of second interconnection structures. Each of the first electronic component, the second electronic component and the third electronic component includes a first surface and a second surface opposite to the first surface. The first surface of the second electronic component faces the first electronic component, and the first surface of the third electronic component faces the second electronic component. The first electronic component is between the second electronic component and the third electronic component. The first interconnection structures are disposed between the first surface of the first electronic component and the first surface of the second electronic component. Each of the first interconnection structures has a length along a first direction substantially parallel to a surface of the first electronic component, and a width along a second direction substantially parallel to the surface and substantially perpendicular to the first direction. The length is larger than the width. The second interconnection structures are between the first surface of the second electronic component and the first surface of the third electronic component, and electrically connected to the second electronic component and the third electronic component. A height of each second interconnection structure is less than a height of each first interconnection structure.

[0042] In another aspect, a semiconductor device is provided. The semiconductor device includes a first electronic component, a second electronic component, a third elec-

tronic component, a plurality of first interconnection structures, and a plurality of second interconnection structures. Each of the first electronic component, the second electronic component and the third electronic component has a first surface and a second surface opposite to the first surface. The first surface of the second electronic component faces the first surface of the first electronic component, and the first surface of the third electronic component faces the second electronic component. The first electronic component is between the second electronic component and the third electronic component. The first interconnection structures are between the first surface of the first electronic component and the first surface of the second electronic component, and electrically connected to the first and second electronic components. Each of the first interconnection structures has a length along a first direction substantially parallel to a surface of the first electronic component and a width along a second direction substantially parallel to the surface and substantially perpendicular to the first direction. The length is larger than the width. The second interconnection structures are between the first surface of the second electronic component and the first surface of the third electronic component, and electrically connected to the second electronic component and the third electronic component. A height of each second interconnection structure is greater than a height of each second interconnect structure.

[0043] In yet another aspect, a semiconductor device is provided. The semiconductor device includes a first electronic component, a second electronic component, a third electronic component, a plurality of first interconnection structures, and a plurality of second interconnection structures. Each of the first electronic component, the second electronic component, the third electronic component has a first surface and a second surface opposite to the first surface. The first surface of the second electronic component faces the first electronic component, and the first surface of the third electronic component faces the second electronic component. The first electronic component is between the second electronic component and the third electronic component. The first interconnection structures are between the first surface of the first electronic component and the first surface of the second electronic component. The first interconnection structures are electrically connected to the first electronic component and the second electronic component. Each of the first interconnection structures has a length along a first direction substantially parallel to the first surface of the first electronic component and a width along a second direction substantially parallel to the first surface of the first electronic component and substantially perpendicular to the first direction. The length is larger than the width. The second interconnection structures are between the first surface of the second electronic component and the first surface of the third electronic component. The second interconnection structures are electrically connected to the second electronic component and the third electronic component. A height of each second interconnection structure is different from a height of each first interconnection structure. The width of each first interconnection structure is consistent from a top view, and the height of each first interconnection structure is consistent.

[0044] In one exemplary aspect, a semiconductor device is provided. The semiconductor device includes a first electronic component, a second electronic component, a third electronic component, a plurality of first interconnection structures, and a plurality of second interconnection structures. The first electronic component has a first surface and a second surface opposite to the first surface. The second electronic component has a first surface facing the first electronic component, and a second surface opposite to the first surface. The third electronic component has a first surface facing the second electronic component, and a second surface opposite to the first surface. The first electronic component is disposed between the second electronic component and the third electronic component. The first interconnection structures are disposed between the first surface of the first electronic component and the first surface of the second electronic component, and electrically connected to the first electronic component and the second electronic component. Each of the first interconnection structures has a length along first direction substantially parallel to the first surface of the first electronic component, and a width along a second direction substantially parallel to the first surface of the first electronic component and substantially perpendicular to the first direction. The length is larger than the width. The second interconnection structures are disposed between the first surface of the second electronic component and the first surface of the third electronic component, and electrically connected to the second electronic component and the third electronic component. A height of each of the second interconnection structures is less than a height of each of the first interconnection structures.

[0045] In another aspect, a semiconductor device is provided. The semiconductor device includes a first electronic component, a second electronic component, a third electronic component, a plurality of first interconnection structures, and a plurality of second interconnection structures. The first electronic component has a first surface and a second surface opposite to the first surface. The second electronic component has a first surface facing the first electronic component, and a second surface opposite to the first surface. The third electronic component has a first surface facing the second electronic component, and a second surface opposite to the first surface. The first electronic component is disposed between the second electronic component and the third electronic component. The first interconnection structures are disposed between the first surface of the first electronic component and the first surface of the second electronic component, and electrically connected to the first electronic component and the second electronic component. Each of the first interconnection structures has a length along a first direction substantially parallel to the first surface of the first electronic component, and a width along a second direction substantially parallel to the first surface of the first electronic component and substantially perpendicular to the first direction. The length is larger than the width. The second interconnection structures are disposed between the first surface of the second electronic component and the first surface of the third electronic component, and electrically connected to the second electronic component and the third electronic component. The first surface of the third electronic component is between the first surface of the first electronic component and the first surface of the second electronic component in a third direction.

[0046] In yet another aspect, a semiconductor device is provided. The semiconductor device includes a first electronic component, a second electronic component, a third

electronic component, and a plurality of first interconnection structures. The first electronic component is disposed between the second electronic component and the third electronic component. The first interconnection structures are electrically connected to the first electronic component and the second electronic component. Each of the first interconnection structures has a length along a first direction and a width along a second direction substantially perpendicular to the first direction. The length is larger than the width. The third electronic component has a cavity, and the first electronic component is disposed within the cavity.

[0047] The foregoing outlines structures of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

What is claimed is:

1. A semiconductor device, comprising:

a first electronic component having a first surface and a second surface opposite to the first surface;

a second electronic component having a first surface facing the first electronic component and a second surface opposite to the first surface;

a third electronic component having a first surface facing the second electronic component and a second surface opposite to the first surface, wherein the first electronic component is between the second electronic component and the third electronic component;

a plurality of first interconnection structures between the first surface of the first electronic component and the first surface of the second electronic component, and electrically connected to the first electronic component and the second electronic component, wherein each of the first interconnection structures has a length along a first direction substantially parallel to the first surface of the first electronic component and a width along a second direction substantially parallel to the first surface of the first electronic component and substantially perpendicular to the first direction, and the length is larger than the width; and

a plurality of second interconnection structures between the first surface of the second electronic component and the first surface of the third electronic component, and electrically connected to the second electronic component and the third electronic component, wherein a height of each of the second interconnection structures is less than a height of each of the first interconnection structures.

2. The semiconductor device of claim **1**, wherein a ratio of the length to the width of at least one of the first interconnection structures is greater than 2.

3. The semiconductor device of claim **1**, wherein the first electronic component comprises a plurality of electrical terminals, and each of the first interconnection structures is electrically connected to more than one of the plurality of electrical terminals of the first electronic component.

4. The semiconductor device of claim **1**, wherein the first interconnection structures comprises a first set of and a second set, the first set and the second set are arranged alternately in the second direction, the first interconnection structures of the first set are electrically connected, the first interconnection structures of the second set are electrically connected, and the first set and the second set are electrically disconnected from each other.

5. The semiconductor device of claim **1**, wherein the third electronic component further comprises a third surface facing the first electronic component and opposite to the second surface, and the first electronic component is disposed between the first surface and the third surface of the third electronic component.

6. A semiconductor device, comprising:

a first electronic component having a first surface and a second surface opposite to the first surface;

a second electronic component having a first surface facing the first electronic component and a second surface opposite to the first surface;

a third electronic component having a first surface facing the second electronic component and a second surface opposite to the first surface, wherein the first electronic component is between the second electronic component and the third electronic component;

a plurality of first interconnection structures between the first surface of the first electronic component and the first surface of the second electronic component, and electrically connected to the first electronic component and the second electronic component, wherein each of the first interconnection structures has a length along a first direction substantially parallel to the first surface of the first electronic component and a width along a second direction substantially parallel to the first surface of the first electronic component and substantially perpendicular to the first direction, and the length is larger than the width; and

a plurality of second interconnection structures between the first surface of the second electronic component and the first surface of the third electronic component, and electrically connected to the second electronic component and the third electronic component, wherein the first surface of the third electronic component is between the first surface of the first electronic component and the first surface of the second electronic component in a third direction.

7. The semiconductor device of claim **6**, wherein the third direction is perpendicular to the first direction and the second direction.

8. The semiconductor device of claim **6**, wherein a ratio of the length to the width of at least one of the first interconnection structures is greater than 2.

9. The semiconductor device of claim **6**, wherein the third electronic component has a third surface parallel with and between the first surface and the second surface of the third component, and the first component is disposed between the first surface and the third surface.

10. The semiconductor device of claim **9**, wherein the third component is separated from the first component.

11. The semiconductor device of claim **6**, wherein a height of each second interconnection structure is different from a height of each of first interconnection structure.

12. The semiconductor device of claim **11**, wherein the height of each second interconnection structure is less than the height of each first interconnection structure.

13. The semiconductor device of claim **6**, wherein the first interconnection structures comprises a first set of and a second set, the first set and the second set are arranged alternately in the second direction, the first interconnection structures of the first set are electrically connected, the first interconnection structures of the second set are electrically connected, and the first set and the second set are electrically disconnected from each other.

14. A semiconductor device, comprising:

a first electronic component;

a second electronic component;

a third electronic component, wherein the first electronic component is between the second electronic component and the third electronic component; and

a plurality of first interconnection structures electrically connected to the first electronic component and the second electronic component, wherein each of the first interconnection structures has a length along a first direction and a width along a second direction substantially perpendicular to the first direction, and the length is larger than the width, wherein the third electronic component has a cavity, and the first electronic component is disposed within the cavity.

15. The semiconductor device of claim **14**, wherein the first electronic component comprises a plurality of electrical terminals, and each of the first interconnection structures is electrically connected to more than one of the plurality of electrical terminals of the first electronic component.

16. The semiconductor device of claim **14**, further comprising a plurality of second interconnection structures electrically connected to the second electronic component and the third electronic component.

17. The semiconductor device of claim **16**, wherein a height of each second interconnection structure is less than a height of each first interconnection structure.

18. The semiconductor device of claim **14**, wherein the first interconnection structures comprises a first set of and a second set, the first set and the second set are arranged alternately in the second direction, the first interconnection structures of the first set are electrically connected, the first interconnection structures of the second set are electrically connected, and the first set and the second set are electrically disconnected from each other.

19. The semiconductor device of claim **14**, wherein the first electronic component is separated from a bottom surface of the cavity.

20. The semiconductor device of claim **14**, wherein a thickness of the first electronic component is less than a depth of the cavity.

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