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(54) **POWER DISTRIBUTION ARCHITECTURE WITH SERIES-CONNECTED BUS CONVERTER**

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(Continued)

(58) **Field of Classification Search**
CPC H02M 3/33576
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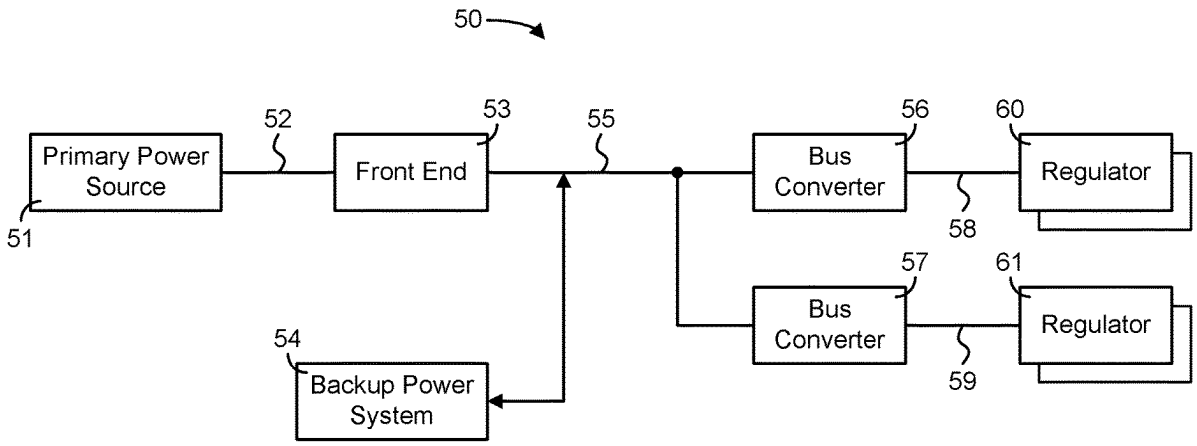
(57) **ABSTRACT**

Apparatus for power conversion are provided. One apparatus includes a power converter including an input circuit and an output circuit. The power converter is configured to receive power from a source for providing power at a DC source voltage V_S. The power converter is adapted to convert power from the input circuit to the output circuit at a substantially fixed voltage transformation ratio $K_{DC}=V_{OUT}/V_{IN}$ at an output current, wherein V_{IN} is an input voltage and V_{OUT} is an output voltage. The input circuit and at least a portion of the output circuit are connected in series across the source, such that an absolute value of the input voltage V_{IN} applied to the input circuit is approximately equal to the absolute value of the DC source voltage V_S minus a number N times the absolute value of the output voltage V_{OUT}, where N is at least 1.

95 Claims, 7 Drawing Sheets



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continuation of application No. 16/781,070, filed on Feb. 4, 2020, now Pat. No. 11,075,583, which is a continuation of application No. 16/022,636, filed on Jun. 28, 2018, now Pat. No. 10,594,223, which is a continuation of application No. 13/933,252, filed on Jul. 2, 2013, now Pat. No. 10,199,950.

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(58) **Field of Classification Search**
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See application file for complete search history.

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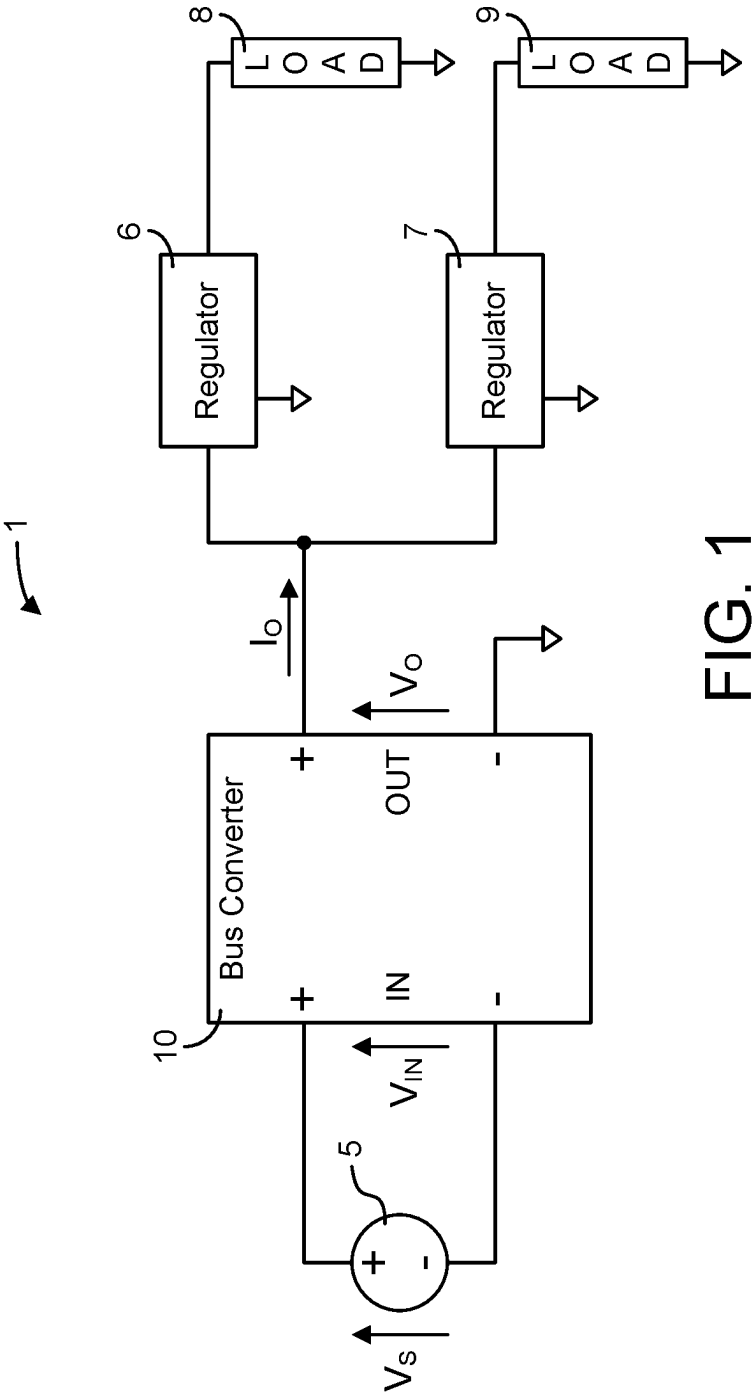

1
8
LOAD
9
LOAD
6
Regulator
7
Regulator
I_O
V_O
Bus Converter
+
OUT
-
+
IN
-
10
V_{IN}
5
+
-
V_S

FIG. 1

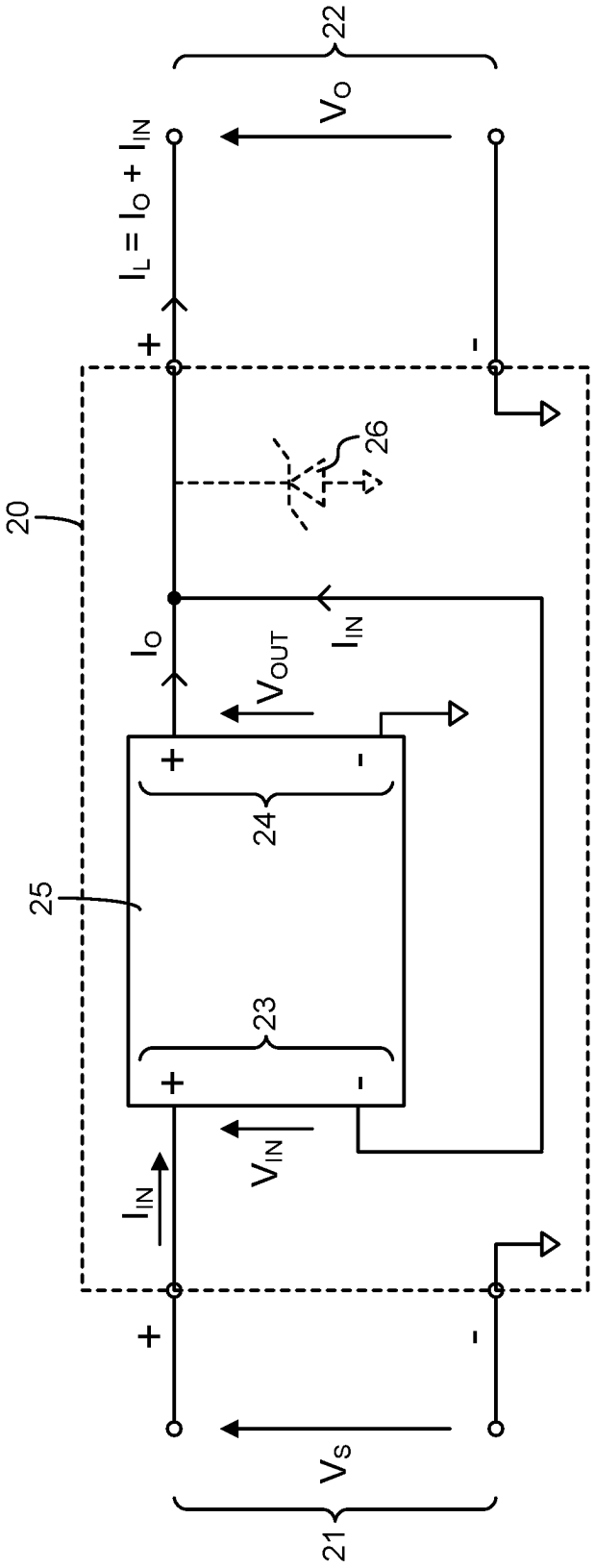


FIG. 2

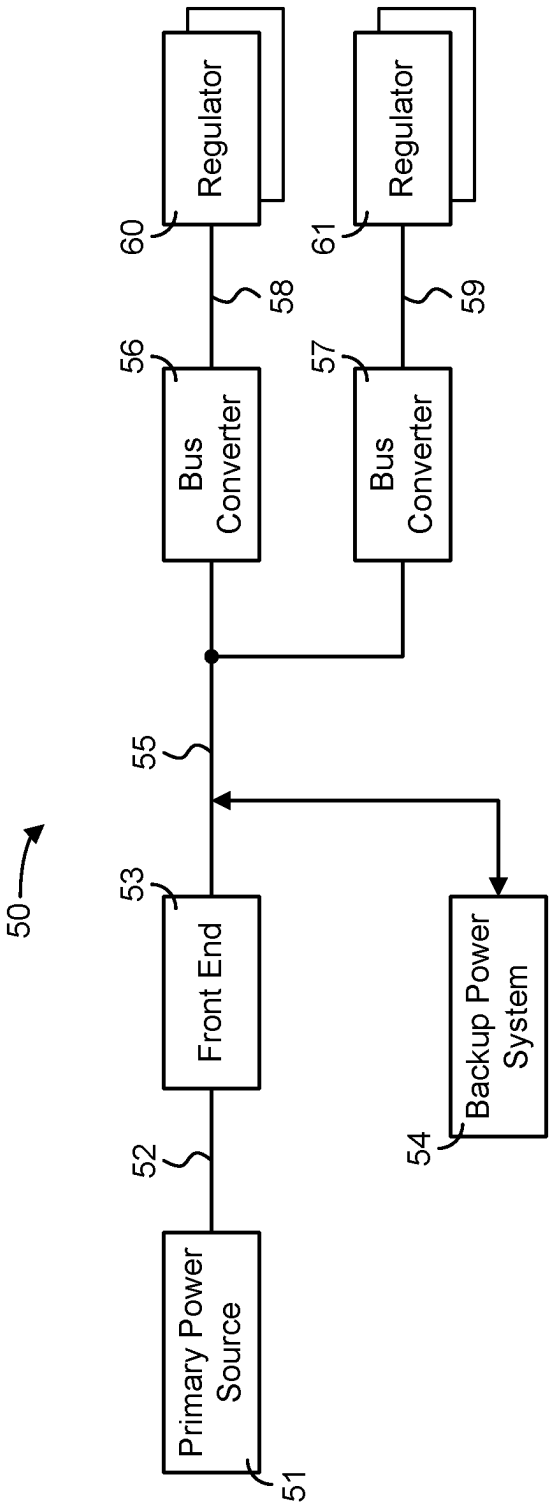
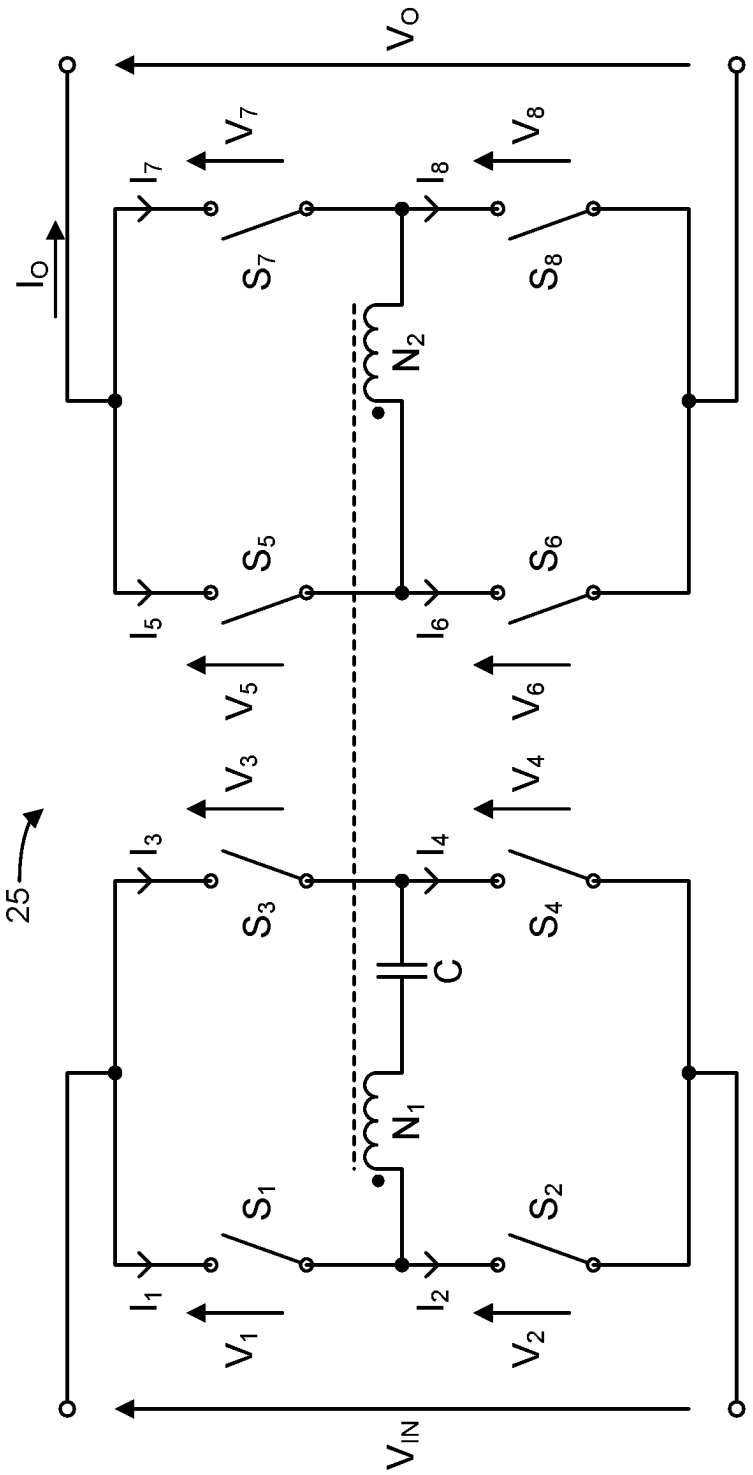

50
Primary Power Source
51
52
Front End
53
Backup Power System
54
55
Bus Converter
56
Bus Converter
57
Regulator
60
Regulator
61
58
59

FIG. 3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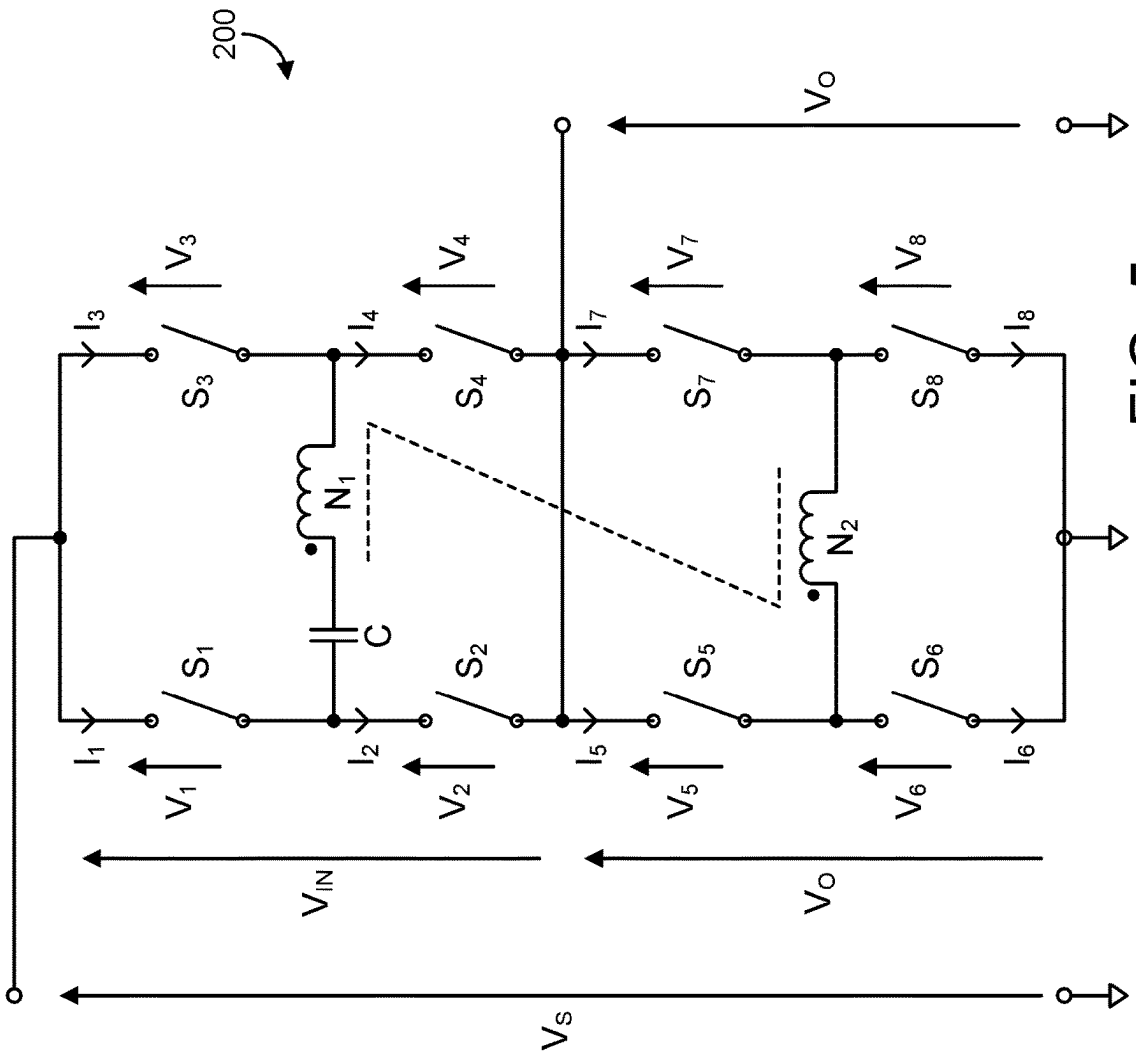
V_7
V_8
I_7
I_8
I_O
S_7
S_8
N_2
S_5
S_6
I_5
I_6
V_5
V_6
V_3
V_4
25
I_3
I_4
S_3
S_4
C
N_1
S_1
S_2
I_1
I_2
V_1
V_2
V_{IN}

FIG. 4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V_O
V_3
V_4
V_7
V_8
I_3
I_4
I_7
I_8
S_3
S_4
S_7
S_8
N_1
N_2
C
S_1
S_2
S_5
S_6
I_1
I_2
I_5
I_6
V_1
V_2
V_5
V_6
V_{IN}
V_O
V_S

FIG. 5

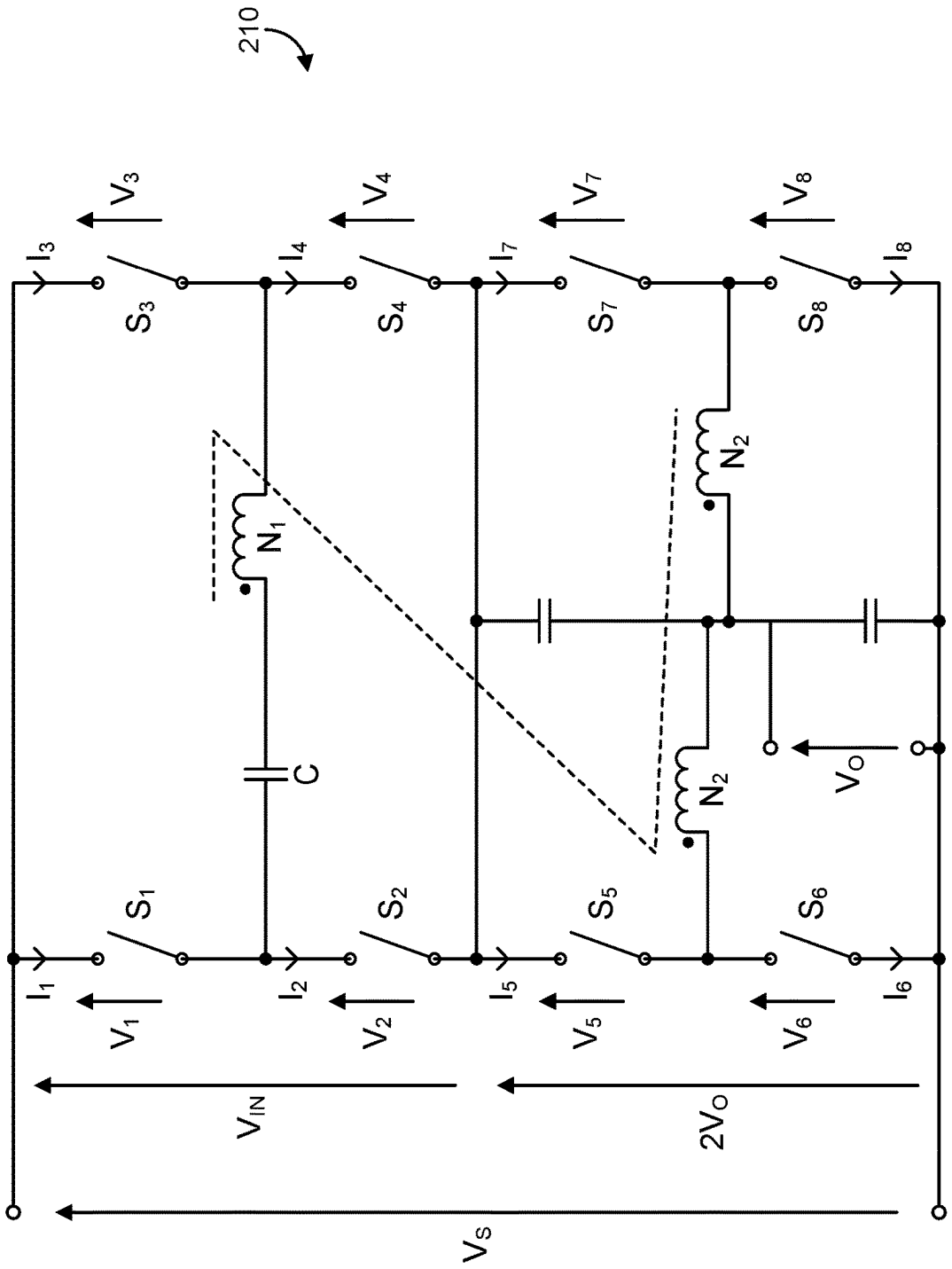
210
V3
V4
V7
V8
I3
I4
I7
I8
S3
S4
S7
S8
N1
N2
N2
C
VO
S1
S2
S5
S6
I1
I2
I5
I6
V1
V2
V5
V6
VIN
2VO
VS

FIG. 6

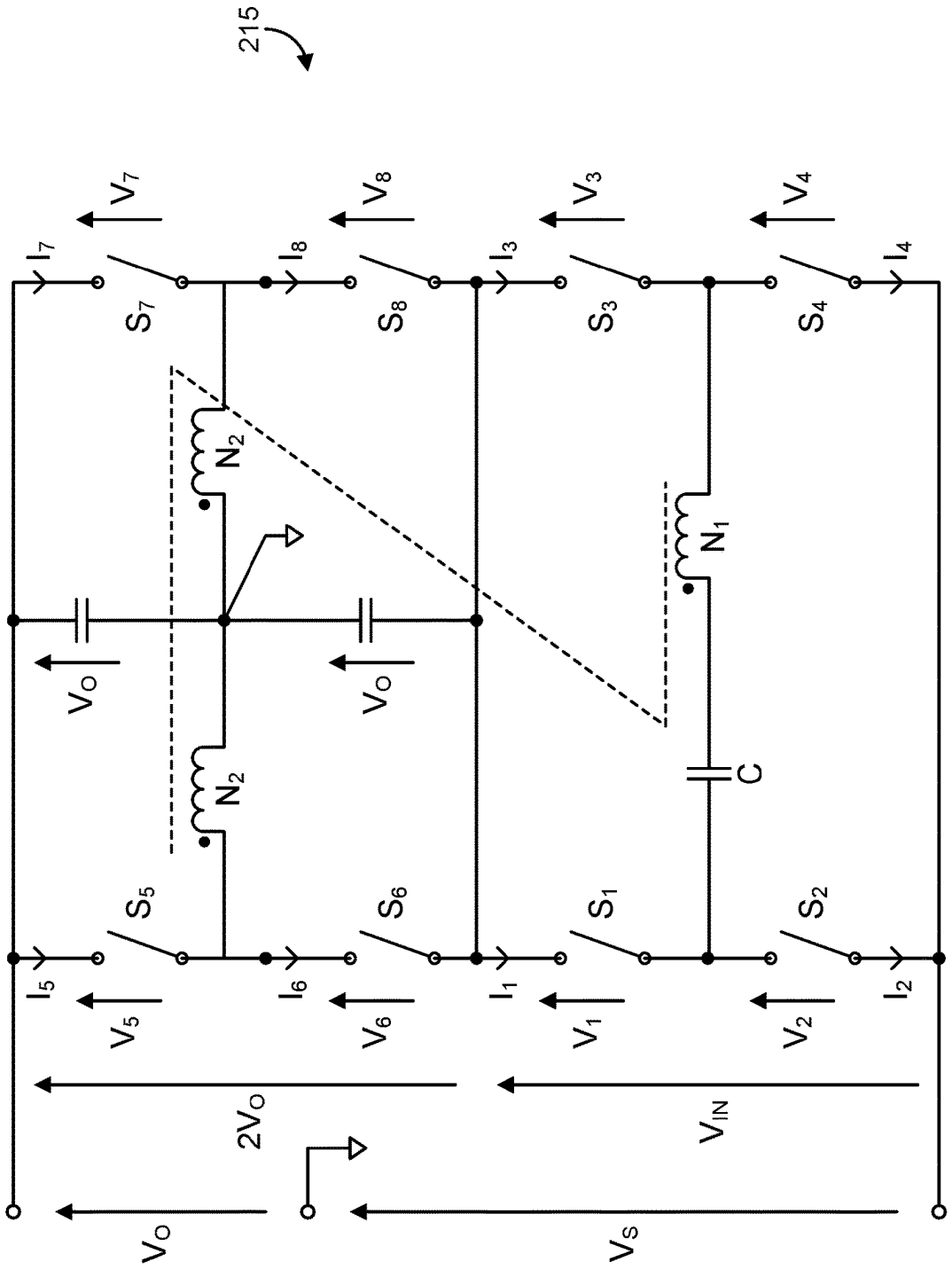
215
V7
V8
V3
V4
I7
I8
I3
I4
S7
S8
S3
S4
N2
N1
VO
VO
N2
C
S5
S6
S1
S2
I5
I6
I1
I2
V5
V6
V1
V2
2VO
VIN
VO
VS

FIG. 7

POWER DISTRIBUTION ARCHITECTURE WITH SERIES-CONNECTED BUS CONVERTER

CROSS-REFERENCE TO RELATED PATENT APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 17/385,384 filed Jul. 26, 2021, which is a continuation of U.S. patent application Ser. No. 16/781,070, filed Feb. 4, 2020 (now U.S. Pat. No. 11,075,583), which is a continuation of U.S. patent application Ser. No. 16/022,636, filed Jun. 28, 2018 (now U.S. Pat. No. 10,594,223), which is a continuation of U.S. patent application Ser. No. 13/933,252, filed Jul. 2, 2013 (now U.S. Pat. No. 10,199,950), each of which are incorporated herein by reference in their entirety.

BACKGROUND

Referring to FIG. **1**, a prior art power distribution system **1** such as an Intermediate Bus Architecture ("IBA") is shown having a DC power source **5**, supplying power at a source voltage, V_S, to the input of a bus converter **10**. The output of the bus converter **10** supplies power to one or more down-stream regulators, e.g. regulators **6**, **7** which in turn provide regulated power, e.g. regulated voltage, to respective loads **8**, **9**. The bus converter **10** may include a DC Transformer which is a switching power converter that may provide voltage transformation from its input to output at an essentially fixed voltage gain and also provide galvanic isolation between its input and output. The bus converter **10** may adjust its output slightly during predetermined operating conditions to provide in-rush current limiting, e.g. during start up and may provide partial regulation over selected portions of the source voltage range. Although a single bus converter is shown in FIG. **1**, a plurality of bus converters may be connected to receive power from a single source **5** and provide power at one or more voltages to a plurality of down-stream regulators, such as regulators **6** and **7**. Additionally, two or more bus converters or two or more DC Transformers may be connected in parallel to increase power throughput or to provide a measure of fault tolerance.

SUMMARY

One embodiment of the disclosure relates to an apparatus that includes a power distribution system comprising a source for providing power at a DC source voltage V_S. The apparatus further includes a bus converter that includes an input circuit and an output circuit. The bus converter is adapted to convert power from the input circuit to the output circuit at a substantially fixed voltage transformation ratio K_{DC} at an output current. An input voltage V_{IN} is applied to the input circuit and an output voltage V_{OUT} is produced by the output of the bus converter, and the substantially fixed voltage transformation ratio can be represented as $K_{DC}=V_{OUT}/V_{IN}$. The apparatus further includes a power distribution bus connected to distribute power from the output circuit of the bus converter at the output voltage V_{OUT}. The apparatus further includes a plurality of regulators. Each regulator includes a regulator input connected to the power distribution bus to receive power from the output circuit of the bus converter and a regulator output connected to supply power to a respective load. The plurality of regulators each are separated by a distance from the bus converter. The input circuit of the bus converter and at least a portion of the output circuit of the bus converter are connected in series across the source such that an absolute value of the input voltage V_{IN} applied to the input circuit is approximately equal to the absolute value of the DC source voltage V_S minus a number N times the absolute value of the output voltage V_{OUT}, where Nis at least 1.

Another embodiment relates to an apparatus that includes a power converter including an input circuit and an output circuit. The power converter is configured to receive power from a power distribution system comprising a source for providing power at a DC source voltage V_S. The power converter is adapted to convert power from the input circuit to the output circuit at a substantially fixed voltage transformation ratio K_{DC} at an output current. An input voltage V_{IN} is applied to the input circuit and an output voltage V_{OUT} is produced by the output of the power converter. The substantially fixed voltage transformation ratio can be represented as $K_{DC}=V_{OUT}/V_{IN}$. The power converter further includes a series connection between the input circuit of the power converter and at least a portion of the output circuit of the power converter across the source, such that an absolute value of the input voltage V_{IN} applied to the input circuit is approximately equal to the absolute value of the DC source voltage V_S minus a number N times the absolute value of the output voltage V_{OUT}, where N is at least 1.

Yet another embodiment relates to an apparatus that includes a bus converter including an input circuit and an output circuit. The bus converter is configured to receive power from a power distribution system including a source for providing power at a DC source voltage V_S. The bus converter is adapted to convert power from the input circuit to the output circuit at a substantially fixed voltage transformation ratio K_{DC} at an output current. An input voltage V_{IN} is applied to the input circuit and an output voltage V_{OUT} is produced by the output of the bus converter, and the substantially fixed voltage transformation ratio can be represented as $K_{DC}=V_{OUT}/V_{IN}$. The apparatus further includes a power distribution bus connected to distribute power from the output circuit of the bus converter at the output voltage V_{OUT}. The apparatus further includes a plurality of regulators. Each regulator includes a regulator input connected to the power distribution bus to receive power from the output circuit of the bus converter and a regulator output connected to supply power to a respective load. The plurality of regulators each are separated by a distance from the bus converter. The input circuit of the bus converter and at least a portion of the output circuit of the bus converter are connected in series across the source such that an absolute value of the input voltage V_{IN} applied to the input circuit is approximately equal to the absolute value of the DC source voltage V_S minus a number N times the absolute value of the output voltage V_{OUT}, where N is at least 1.

Another embodiment relates to an apparatus comprising an intermediate bus architecture power distribution system for a telecommunications system comprising a source for providing power at a DC source voltage; a circuit board comprising a bus converter, the bus converter comprising an input circuit, the input circuit comprising a primary transformer winding, the bus converter further comprising an output circuit, the output circuit comprising a secondary transformer winding, wherein the primary and secondary transformer windings are galvanically connected in series, and wherein the bus converter is configured to provide power to a power distribution bus that is not galvanically isolated from the source; and the circuit board further comprising a plurality of regulators, wherein each regulator comprises a regulator input connected to the power distri-

bution bus to receive power from the output circuit of the bus converter and a regulator output connected to supply power to a respective load, the plurality of regulators each being separated by a distance from the bus converter.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a schematic block diagram of a prior art IBA power distribution system according to an illustrative embodiment.

FIG. **2** shows a functional block diagram of a series-connected DC Transformer according to an illustrative embodiment.

FIG. **3** shows a schematic diagram of a new power distribution architecture according to an illustrative embodiment.

FIG. **4** shows a schematic diagram of an isolated SAC-based DC Transformer according to an illustrative embodiment.

FIG. **5** shows a schematic diagram of a series-connected SAC-based DC Transformer according to an illustrative embodiment.

FIG. **6** shows a schematic diagram of a series-connected SAC-based DC Transformer having a center-tapped winding in the output circuit according to an illustrative embodiment.

FIG. **7** shows a schematic diagram of a series-connected DC Transformer for receiving power from a negative input source and delivering power at a positive output voltage according to an illustrative embodiment.

DETAILED DESCRIPTION

Power Distribution Architecture

A power distribution system **50** is shown in FIG. **3** having a primary power source **51** delivering power via a connection **52** to a front-end power-processing unit **53**. The primary power source **51** may be an AC utility line, and the front end unit **53** may be a power conversion stage that converts power from the power source **51** delivering power at a relatively high but safe DC voltage to a power distribution bus **55**, e.g. the DC voltage may vary from a minimum, e.g. 38 Volts, to a maximum, e.g. 55 Volts. Preferably, the front-end unit **53** provides voltage step down and isolation and may optionally provide power factor correction, regulation, or both. An optional backup power system **54** is shown connected to the power distribution bus **55** to provide power in the event of a loss of power from the primary power source **52**. The backup power system may include batteries, a charger for maintaining the batteries, and a switchover mechanism that connects the batteries to the bus in response to predetermined events, such as a decline in voltage or loss of power from the output of the front end **53** or the primary power source **51**.

One or more bus converters, e.g. bus converters **56**, **57**, may be connected to the power distribution bus **55** downstream from the front end **53** as shown in the example of FIG. **3** to convert power received from the relatively high voltage power distribution bus **55** for delivery to a respective lower voltage bus. As shown, bus converters **56** and **57** respectively supply power to buses **58** and **59** at voltages, e.g. at or near the requisite load voltages, that are lower than the voltage of the power distribution bus **55**, providing step-down voltage transformation. The bus converters **56**, **57** are generally separated by a distance from their respective regulators **60**, **61**. For example, in a typical system, one or more system circuit boards housed in a common enclosure may each include one or more bus converters, preferably located near the edge of, or other location on, the board where power connections are made to the board. A down-stream regulator receiving power from the bus converter(s) may be preferably located adjacent to the circuitry, e.g. a processor, ASIC, or other circuitry, to which it or they supply power. The physical distance separating the bus converter and a respective down-stream regulator in such an example may range from as much as a dimension of the system circuit board, i.e. a diagonal dimension where the bus converter and regulator located at opposite corners, a length or width dimension where they are located at opposite edges, a half-length or width where one is situated closer to the middle and the other is at an edge, etc. In another example, a bus converter may be located off of the system board in which case the electrical distance could be greater than a dimension of the system board. Naturally, the distance separating the bus converter and a respective down-stream regulator will depend on the system layout. However, a bus converter housed in a self-contained assembly adapted to be installed as a unit at a location remote from the down-stream regulator(s) may be separated by a distance from a down-stream regulator regardless of their respective mounting locations at the system level.

The output of each bus converter **56**, **57** may, in turn, provide power via its respective bus **58**, **59** to a respective plurality of regulators, preferably at or near the point of load, such as point-of-load switching voltage regulators **60**, **61**. It should be understood that although two bus converters **56**, **57** are shown in the example of FIG. **3**, any number of bus converters, e.g. one, may be used. Similarly, although regulators **60** and **61** are shown in FIG. **3** as comprising a plurality of individual regulators, any suitable number of regulators, e.g. one, may be connected to a particular bus converter within the constraints of the physical devices used. The regulators **60**, **61** may supply power to respective loads (not shown). The loads can be a variety of devices, including integrated circuits and electromechanical devices (such as storage and cooling devices).

The bus converters **56**, **57** shown in the system of FIG. **3**, however, preferably do not provide galvanic isolation between their respective output busses **58**, **59** and the power distribution bus **55** as described in additional detail below.

Series-Connected DC Transformer

Referring to FIG. **2**, a functional block diagram of a series-connected power conversion system **20** suitable for use as a bus converter in the power distribution system **50** of FIG. **3** is shown. The power conversion system **20** includes an input **21** for receiving power from a source at a source voltage, V_S, and an output **22** for delivering power to a load at an output voltage, V_O, that is less than V_S, and a DC Transformer **25**. The DC Transformer **25** may be implemented preferably using the Sine-Amplitude Converter ("SAC") topologies and timing architectures described in Vinciarelli, Factorized Power Architecture and Point of Load Sine Amplitude Converters, U.S. Pat. No. 6,930,893 and in Vinciarelli, Point of Load Sine Amplitude Converters and Methods, U.S. Pat. No. 7,145,786 both assigned to VLT., Inc. and incorporated here in their entirety by reference (hereinafter the "SAC Patents"). Alternatively, other converter topologies, such as hard-switching, fixed ratio DC-DC converters, may be used. The DC Transformer **25** converts power received from its input **23** (distinguished from the input **21** of the bus converter **20**) at an input voltage, V_{IN}, for delivery to its output **24** at an output voltage, V_{OUT}, using an essentially fixed voltage gain or voltage transformation ratio.

The voltage gain or voltage transformation ratio of a system as defined generally herein is the ratio of its output voltage to its input voltage at a specified current such as an output current. For the system **20** in FIG. **2**, the voltage transformation ratio may be expressed as $K_{SYS}=V_O/V_S$ @ I_L. Similarly, the voltage transformation ratio of the DC Transformer **25** may be stated as $K_{DC}=V_{OUT}/V_{IN}$ @ I_O. Note that the system output voltage, V_O, and the DC Transformer output voltage, V_{OUT}, are the same in the configuration shown. However, the input **23** and output **24** of the DC Transformer **25** are shown in a series-connected configuration across the system input **21**. As a result, the input voltage, V_{IN}, to the DC Transformer input **23** is less than the input voltage, V_S, to the system input **21** by an amount equal to the output voltage:

$$V_{IN}=V_S-V_O. \tag{1}$$

Similarly as shown in FIG. **2**, the current, I_L, drawn by the load from the system output **22** is greater than the current produced at the output **24** of the DC Transformer **25** by an amount equal to the input current:

$$I_O=I_L-I_{IN}. \tag{2}$$

The system voltage transformation ratio, K_{SYS}, using the series-connected DC Transformer **25**, may be expressed as a function of the DC Transformer voltage transformation ratio, K_{DC}:

$$K_{SYS}=K_{DC}/(K_{DC}+1) \tag{3}$$

The above equation (3) may be rearranged to express the DC Transformer **25** voltage transformation ratio, KDC, required in a series-connected system as a function of the system voltage transformation ratio, K_{SYS}:

$$K_{DC}=K_{SYS}/(1-K_{SYS}) \tag{4}$$

Referring to FIG. **4**, an isolated SAC that may be utilized for DC Transformer **25**, according to one embodiment, is shown having a full-bridge input circuit, including switches S1, S2, S3, and S4, connected to drive the resonant circuit including capacitor C and the input winding, having N1 turns, with the input voltage V_{IN}. The isolated SAC is shown having a full-bridge output circuit, including switches S5, S6, S7, and S8, connected to rectify the voltage impressed across the output winding, having N2 turns, and delivering the output voltage, V_O. The voltage transformation ratio of the SAC will be essentially a function of the turns ratio: $K_{DC}=V_O/V_{IN}=N2/N1$.

A series-connected SAC **200** is shown in FIG. **5**. By way of comparison, the series-connected SAC **200** uses the same full-bridge input circuit topology, including switches S1, S2, S3, and S4, driving the resonant circuit including capacitor C and the input winding, having N1 turns, with the input voltage V_{IN}. SAC **200** also uses the same full-bridge output topology, including switches S5, S6, S7, and S8, connected to rectify the voltage impressed across the output winding, having N2 turns, and delivering the output voltage, V_O. The voltage transformation ratio of the series-connected SAC **200** from the input circuit to output circuit is also essentially a function of the transformer turns ratio N2/N1 and the same as the isolated SAC **25** in FIG. **4**: $K_{DC}=V_O/V_{IN}=N2/N1$. However, when evaluated in terms of the system, i.e. using V_S applied across the series-connected input and output, the voltage transformation ratio becomes: $K_{SYS}=V_O/V_S=N2/(N2+N1)$.

Many contemporary applications use a voltage transformation ratio equal to ⅕ requiring an odd transformer turns ratio (N2/N1=⅕) which is generally not optimal. Referring to equation (4) above, the K_{SYS}=⅕ bus converter may be implemented using a K_{DC}=¼ series-connected topology (e.g. as shown in FIGS. **2**, **4**, and **5**), allowing the use of an even, i.e. 1:4, turns ratio in the transformer. An even transformer turns ratio may provide greater transformer layout flexibility and efficiency.

Note that the series-connected converter **200** may be implemented by connecting an off-the-shelf isolated DC Transformer, such as the isolated converter shown in FIG. **4**, as shown in FIG. **2**. Alternatively, the converter **200** may be implemented as series-connected input and output circuits, e.g. as shown in FIGS. **5**, **6**, and **7** discussed below, in an integrated converter, optionally providing greater power density eliminating the isolation imposed design constraints, eliminating control circuit bias currents from flowing through to the output and the potential need for an output clamp, and providing system-ground referenced control circuitry (not shown) for interface signals that are referenced to ground rather than the output for the reconfigured off-the-shelf isolated converter.

Connecting the input and output of the DC Transformer **25** in series eliminates galvanic isolation between the input and output of the series-connected bus converter **20**, which is counterintuitive. However, when used in the architecture of FIG. **3**, isolation is deployed at an intermediate stage where the isolation may be superfluous. The architecture of FIG. **3**, therefore, trades isolation at this stage for efficiency gain and reduced component stress. If isolation is required, e.g. for safety reasons, in the architecture of FIG. **3**, it may preferably be provided by an upstream power conversion stage such as the front-end converter **53**.

Efficiency

The power processed by the isolated SAC shown in FIG. **4** may be compared with that of the series-connected SAC **200** (FIG. **5**) by summing the product of maximum voltage across (V_n) and average current (I_n) through each switch (n=1 through 8).

$$P_{Processed}=\sum_{n=1}^{n=8n}(Vn*In) \tag{5}$$

Each input switch (S1, S2, S3 and S4) in the full bridge input circuits (FIGS. **4**, **5**) is subjected to the input voltage, V_{IN}, (distinguished from the source voltage V_S) and an average of one half of the input current, I_{IN}. The sinusoidal nature of the current in the SAC topology represents a difference between the RMS and average currents, which is unimportant for the following comparison between two converters using the same topology. The power processed by the input circuits is:

$$P_{IN}=2*V_{IN}*I_{IN} \tag{6}$$

Similarly, each output switch (S5, S6, S7 and S8) in the full bridge output circuit of FIG. **4** will be subjected to the full output voltage, V_O, and will carry an average of one half of the output current, I_O. Note that the output current in the case of the isolated converter is equal to the load current, I_L and in the case of the series-connected converter (discussed below) is not. The power processed by the output circuits may therefore be reduced to:

$$P_{OUT}=2*V_O*I_O \tag{7}$$

Combining equations (6) and (7) and making the appropriate substitutions using $K_{DC}=V_O/V_{IN}$ and the corollary

$I_{IN}=K_{DC}*I_O$, the total power processed by the converters reduces to:

$$P=4*V_O*I_O \quad (8)$$

In the isolated converter of FIG. **4**, the output current equals the load current ($I_O=I_L$), therefore, the power processed by the isolated converter, P_{ISO}, may be reduced to the following function of load power, $P_{Load}=V_O*I_L$:

$$P_{ISO}=4*P_{Load} \quad (9)$$

Neglecting fixed losses in the converter, the input current may be expressed as a function of the output current and voltage transformation ratio as follows:

$$I_{IN}=I_O*K_{DC} \quad (10)$$

Combining equations (2), (4), and (10), the output current of the series-connected converter may be expressed as a function of load current and voltage transformation ratio as follows:

$$I_{O\text{-}Series}=I_L*(1-K_{SYS}) \quad (11)$$

Substituting equation (11) into equation (8) produces the total power processed by the series-connected converter as a function of load power ($P_{Load}=V_O*I_L$) and system voltage transformation ratio:

$$P_{SERIES}=4*P_{Load}*(1-K_{SYS}) \quad (12)$$

Accordingly, the efficiency advantage of the series-connected converter over the isolated converter—the ratio of equations (12) and (9)—reduces to:

$$P_{SERIES}/P_{ISO}=(1-K_{SYS}) \quad (13)$$

From equation (13) it can be seen that the series-connected converter offers a significant efficiency advantage. Consider a typical example for comparison, using a bus converter to convert power from a nominal 50 Volt power distribution bus for delivery to a 10 volt load ($K_{SYS}=1/5$) at 100 amps: the series-connected converter processes only 80% of the power, offering a 20% efficiency savings compared to the isolated converter.

In a typical isolated DC Transformer, like most DC-DC converters, the control circuitry is configured to operate from power drawn from the input producing a quiescent component of the input current. Use of such a converter, e.g. an off-the-shelf DC Transformer, in a series-connected configuration could, therefore, allow the quiescent input current to flow unregulated into a load connected to the output, which would be problematic while the power train is not operating and, therefore, incapable of regulating the output voltage. It may, for that reason, be desirable to clamp the output voltage using a zener diode, such as zener diode **26** in FIG. **2**, or other clamp circuit or device appropriately scaled in breakdown voltage and power dissipation to carry the quiescent input current, protecting the load and perhaps the output circuitry of the converter. Integrating the series-connected input and output circuitry into a non-isolated converter topology such as shown in FIGS. **5**, **6**, and **7** affords the opportunity to configure the control circuitry to draw power from the input to ground preventing that component of the input current from flowing out to the load. Additionally, a DC blocking capacitor may be used in the power train to avoid leakage current from flowing from the input to the output. One or both of the above measures may be used to avoid the need to clamp the output.

Configuring the control circuitry to reference the system ground in the integrated converter (rather than the input return in the off-the-shelf isolated converter) easily allows any interface signals to be ground-referenced (rather than output referenced) which is advantageous from the perspective of the system integrator.

Center-Tap Secondary

Another series-connected SAC **210** is shown in FIG. **6**. By way of comparison, the series-connected SAC **210** uses the same full-bridge input circuit topology, including switches S1, S2, S3, and S4, driving the resonant circuit including capacitor C and the input winding, having N1 turns, with the input voltage V_{IN}, as shown in FIG. **5**. However, a center-tap output winding, having 2*N2 turns, is used in the output circuit, which includes switches S5, S6, S7, and S8, connected to rectify the voltage impressed across the output windings and delivering the output voltage, V_O. The system voltage transformation ratio of the series-connected SAC **210** (FIG. **6**) is essentially a function of the transformer turns ratio: $K_{SYS}=V_O/V_{SYS}=N2/(N1+2*N2)$; as is the voltage transformation ratio from input circuit to output circuit: $K_{DC}=V_O/V_{IN}=N2/N1$.

The converter **210** of FIG. **6** differs from the series-connected converter **200** (FIG. **5**) in that the input voltage, V_{IN}, presented to the input circuit is equal to the source voltage, V_S, reduced by twice the output voltage, V_O:

$$V_{IN\text{-}210}=V_S-2V_O \quad (14)$$

as suggested by the addition of N2 turns in the output winding of the transformer. Also, each output switch (S5, S6, S7 and S8) in the converter **210** is subjected to twice the output voltage, V_O, with the upper output switches (S5 and S7) each carrying an average of half of the input current, I_{IN}, and the lower output switches (S6 and S8) each carrying an average of half of the difference between the load current, I_L, and the input current, I_{IN}. Using the same analysis as described above, summing the product of maximum voltage across (V_n) and average current (I_n) through each switch (N=1 through 8), the total power processed by the converter **210** of FIG. **6** is:

$$P_{210}=2*V_{IN}*I_{IN}+2*V_O*I_{IN}+2*V_O*(I_L-I_{IN}) \quad (15)$$

Using the system voltage transformation ratio, $K_{SYS}=V_O/V_S$ in equation (14), the input voltage may be expressed as:

$$V_{IN\text{-}210}=V_O*((1/K_{SYS})-2) \quad (16)$$

Recognizing that in an ideal converter the input power equals the output power $V_S*I_{IN}=V_O*I_L$ the input current may be expressed as:

$$I_{IN}=K_{SYS}*I_L \quad (17)$$

Making the appropriate substitutions into equation (15), the total power processed by series-connected converter **210** (FIG. **6**) reduces to:

$$P_{210}=4*V_O*I_L*(1-K_{SYS}) \quad (18)$$

which may be further reduced to express the total power processed by the series-connected converter **210** using a center-tap output winding as shown in FIG. **6** as a function of load power ($P_{Load}=V_O*I_L$) and system voltage transformation ratio:

$$P_{210}=4*P_{Load}*(1-K_{SYS}) \quad (19)$$

Which is the same result obtained in equation (12) above for the series-connected converter **200** in FIG. **5**.

There may be certain advantages of one series-connected topology over the other depending upon the application. For example, the transformer in the converter **200** (FIG. **5**) has N2 fewer turns than in the transformer of the converter **210** (FIG. **6**) offering reduced winding losses. However, the input switches (S1, S2, S3 and S4) in the converter **210** (FIG.

6) are exposed to lower voltages than in the converter **200** (FIG. **5**) which may afford lower switch conduction losses. Also, two of the output switches (S5 and S7) in converter **210** (FIG. **6**) carry much less current and may be implemented with smaller and more cost effective devices than in converter **200** (FIG. **5**).

Negative Input-Positive Output

Referring to FIG. **7**, another series-connected SAC-based converter **215** is shown configured to receive a negative source voltage, V_S, and deliver a positive output voltage. (The topology shown in FIG. **7** may alternatively be adapted to receive a positive source voltage and deliver a negative output voltage.) Converter **215** may be viewed as a variation of the converter **210** (FIG. **6**) in which the input and output circuit positions have been rearranged with the output terminal serving as the common terminal. The converter **215** of FIG. **7** differs from the converter **210** (FIG. **6**) in that the absolute value of the input voltage, V_{IN}, presented to the input circuit is equal to the absolute value of the source voltage, V_S, reduced by the absolute value of the output voltage, V_O (compared to twice the output voltage in FIG. **6**) because of the polarity change from input to output:

$$|V_{IN\text{-}215}|=|V_S|-|V_O| \tag{20}$$

as also suggested by the transformer configuration. Also, the upper output switches (S5 and S7) each carry an average of half of the output current, I_O, which equals the load current, I_L in FIG. **7**, compared to the difference between the load current, I_L, and the input current, I_{IN}, in FIG. **6**. Once again, summing the product of maximum voltage across (V_n) and average current (I_n) through each switch (N=1 through 8) as described above, the total power processed by the converter **215** of FIG. **7** is:

$$P_{215}=2*V_{IN}*I_{IN}+2*V_O*I_{IN}+2*V_O*I_L \tag{21}$$

which, when reduced using equations (17) and (20), becomes:

$$P_{215}=4*P_{Load} \tag{22}$$

A comparison of the power processed by the converter **215** (equation (22); FIG. **7**) with the power processed by the isolated converter **25** (equation (9); FIG. **4**) may indicate no efficiency advantage, however, the input switches (S1, S2, S3 and S4) in the series-connected converter **215** of FIG. **7** are subjected to lower voltages potentially affording use of better figure of merit switches leading to potential efficiency improvements. Furthermore, the absence of isolation-related design constraints in such an integrated converter may be used to increase power density.

The converters **20** (FIG. **2**), **200** (FIG. **5**), **210** (FIG. **6**), and **215** (FIG. **7**) are examples of a class of series-connected converters in which at least a portion of the output circuit is connected in series with the input circuit such that the absolute value of the voltage, V_{IN}, presented to the input circuit is equal to the absolute value of the source voltage V_S, minus N times the absolute value of the output voltage, V_O, where the value of N is at least 1:

$$|V_{IN}|=|V_S|-N*|V_O| \tag{23}$$

The value of N will vary depending upon the converter topology used, e.g. a center-tap secondary or not, polarity reversing or not, etc. In the examples described above: N=1 for converters **20** (FIG. **2**), **200** (FIG. **5**), and **215** (FIG. **7**) and N=2 for converter **210** (FIG. **6**) as shown in equation 14. Although a full bridge switch configuration is preferred for its superior noise performance, half-bridge switch configurations may also be deployed in the input circuitry, the output circuitry, or both.

The disclosure is described above with reference to drawings. These drawings illustrate certain details of specific embodiments that implement the systems, apparatus, and/or methods of the present disclosure. However, describing the disclosure with drawings should not be construed as imposing on the disclosure any limitations that may be present in the drawings. No claim element herein is to be construed under the provisions of 35 U.S.C. § 112, sixth paragraph, unless the element is expressly recited using the phrase "means for." Furthermore, no element, component or method step in the present disclosure is intended to be dedicated to the public, regardless of whether the element, component or method step is explicitly recited in the claims.

It should be noted that although the disclosure provided herein may describe a specific order of method steps, it is understood that the order of these steps may differ from what is described. Also, two or more steps may be performed concurrently or with partial concurrence. It is understood that all such variations are within the scope of the disclosure.

The foregoing description of embodiments of the disclosure have been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the disclosure to the precise form disclosed, and modifications and variations are possible in light of the above teachings or may be acquired from practice of the disclosure. The embodiments were chosen and described in order to explain the principals of the disclosure and its practical application to enable one skilled in the art to utilize the disclosure in various embodiments and with various modifications as are suited to the particular use contemplated.

What is claimed is:

1. An apparatus, comprising:

a bus converter circuit having a first terminal, a second terminal, and a common terminal and being configured to convert power in a direction, the direction being one of the following:

(a) a first direction in which the first terminal and common terminal form an input for receiving input power at a first voltage, V1, and the second terminal and the common terminal form an output for delivering output power at a second voltage, V2, or

(b) a second direction in which the second terminal and the common terminal form an input for receiving input power at the second voltage, V2, and the first terminal and the common terminal form an output for delivering output power at the first voltage, V1;

wherein the input and output are galvanically connected;

wherein over a range of input voltages the bus converter circuit uses an essentially fixed voltage transformation ratio, K, equal to the second voltage, V2 divided by the first voltage, V1, (K=V2/V1), to convert power in the direction, such that output power delivered in the first direction is at the second voltage, V2=K×V1, and output power delivered in the second direction is at the first voltage, V1=V2/K;

wherein the first voltage, V1, is greater than the second voltage, V2;

wherein the bus converter circuit includes (i) a transformer having a first winding and a second winding, (ii) a plurality of switches, and (iii) a controller configured to operate the plurality of switches in a series of converter operating cycles;

wherein each converter operating cycle includes a first and a second power transfer interval, the first and second power transfer intervals having essentially equal durations, and wherein during the first power transfer interval a first set of the plurality of switches is

ON and power is converted in the direction, and during the second power transfer interval a second set of the plurality of switches is ON and power is converted in the direction;

wherein the bus converter circuit is configured during the first power transfer interval (a) to form a first series circuit in which at least the following elements are all connected in series without regard to order: at least one of the first or second terminals, at least one of the first or second windings of the transformer, at least one of the plurality of switches in the first set, and at least one capacitor, and (b) to conduct current in the direction between the first terminal and the second terminal;

wherein the bus converter circuit is configured during the second power transfer interval (a) to form a second series circuit in which at least the following elements are all connected in series without regard to order: at least one of the first or second terminals, at least one of the first or second windings of the transformer, at least one of the plurality of switches in the second set, and at least one capacitor, and (b) to conduct current in the direction between the first terminal and the second terminal;

wherein the bus converter circuit is configured to, before the first power transfer interval, reduce a voltage across a first ZVS switch prior to turning the first ZVS switch ON, such that the voltage across the first ZVS switch is reduced when the first ZVS switch is turned ON, the first ZVS switch being at least one of the plurality of switches in the first set; and

wherein the bus converter circuit is configured to, before the second power transfer interval, reduce a voltage across a second ZVS switch prior to turning the second ZVS switch ON, such that the voltage across the second ZVS switch is reduced when the second ZVS switch is turned ON, the second ZVS switch being at least one of the plurality of switches in the second set.

2. The apparatus of claims **1**, wherein the bus converter circuit is a self-contained assembly adapted to be installed as a unit.

3. A computer apparatus, comprising:

a power distribution system including an input bus for receiving power at a relatively high safe voltage, preferably approximately 48 Volts;

one or more bus converter circuits of claim **1**, connected to receive power from the input bus;

one or more power busses connected to receive power from the one or more bus converter circuits;

a plurality of regulators, each having an input connected to receive power from the one or more power busses and an output for delivering a regulated output; and

one or more semiconductor processors connected to receive power from one or more of the plurality of regulators.

4. The apparatus of claim **1**, wherein forming the first and second series circuits comprises at least two of the first and second terminals.

5. The apparatus of claim **4**, further comprising:

a power distribution bus connected to distribute power from the output; and

a plurality of voltage regulators, wherein each voltage regulator comprises a regulator input connected to the power distribution bus to receive power from the output and a regulator output connected to supply power to a respective load, the plurality of voltage regulators each being separated by a distance from the bus converter circuit.

6. The apparatus of claim **5**, wherein the direction is the first direction.

7. The apparatus of claim **6**, wherein the respective load comprises a computer processor.

8. A computer apparatus, comprising:

a power distribution system including an input bus for receiving power at a relatively high safe voltage, preferably approximately 48 Volts;

one or more bus converter circuits of claim **4**, connected to receive power from the input bus;

one or more power busses connected to receive power from the one or more bus converter circuits;

a plurality of regulators, each having an input connected to receive power from the one or more power busses and an output for delivering a regulated output; and

one or more semiconductor processors connected to receive power from one or more of the plurality of regulators.

9. The apparatus of claim **4**, wherein the bus converter circuit is further capable of converting power in either of the first direction or the second direction and the direction is a function of conditions external to the bus converter circuit.

10. A computer apparatus, comprising:

a power distribution system including an input bus for receiving power at a relatively high safe voltage, preferably approximately 48 Volts;

one or more bus converter circuits of claim **9**, connected to receive power from the input bus;

one or more power busses connected to receive power from the one or more bus converter circuits;

a plurality of regulators, each having an input connected to receive power from the one or more power busses and an output for delivering a regulated output; and

one or more semiconductor processors connected to receive power from one or more of the plurality of regulators.

11. The apparatus of claim **4**, wherein the first series circuit comprises one or more of the following: (a) at least one component that is not in the second series circuit, (b) at least one component that is in the second series circuit but is connected in an order that is different from in the second series circuit, or (c) at least one component that is in the second series circuit but is connected to carry a current that flows in a direction that is opposite from a current that the component carries in the second series circuit.

12. A computer apparatus, comprising:

a power distribution system including an input bus for receiving power at a relatively high safe voltage, preferably approximately 48 Volts;

one or more bus converter circuits of claim **11**, connected to receive power from the input bus;

one or more power busses connected to receive power from the one or more bus converter circuits;

a plurality of regulators, each having an input connected to receive power from the one or more power busses and an output for delivering a regulated output; and

one or more semiconductor processors connected to receive power from one or more of the plurality of regulators.

13. The apparatus of claim **4**, wherein the first set of switches includes one or more switches that are not in the second set of switches.

14. The apparatus of claim **4**, wherein the first set of switches does not include any switches that are in the second set of switches.

15. The apparatus of claim 4, wherein at least one winding of the first series circuit is different than at least one winding of the second series circuit.

16. The apparatus of claim 4, wherein at least one winding of the first series circuit is the same as at least one winding of the second series circuit.

17. The apparatus of claim 16, wherein the at least one winding is configured in the first series circuit to carry current in one direction and in the second series circuit to carry current in another direction opposite to the one direction.

18. The apparatus of claim 16, wherein the first series circuit and the second series circuit each comprises at least two windings of the transformer.

19. The apparatus of claims 18, wherein the bus converter circuit is a self-contained assembly adapted to be installed as a unit.

20. A computer apparatus, comprising:

a power distribution system including an input bus for receiving power at a relatively high safe voltage, preferably approximately 48 Volts;

one or more bus converter circuits of claim 18, connected to receive power from the input bus;

one or more power busses connected to receive power from the one or more bus converter circuits;

a plurality of regulators, each having an input connected to receive power from the one or more power busses and an output for delivering a regulated output; and

one or more semiconductor processors connected to receive power from one or more of the plurality of regulators.

21. The apparatus of claim 18, wherein the at least two windings in the first and second series circuits each comprises the first winding and the second winding, and the first winding and the second winding are configured in the first series circuit to carry current in one direction and are configured in the second series circuit to carry current in another direction opposite to the one direction.

22. The apparatus of claim 21, wherein the first and second windings are configured in a first order in the first series circuit and in a second different order in the second series circuit.

23. The apparatus of claim 22, wherein the first and second windings are configured in the first series circuit for current to flow in the first direction and in the second series circuit for current to flow in the another direction.

24. The apparatus of claim 18, wherein the first and second series circuits form a first and a second series resonant circuit, each having a characteristic resonant period; and the essentially equal duration of the first and second power transfer intervals is less than each characteristic resonant period.

25. The apparatus of claims 24, wherein the bus converter circuit is a self-contained assembly adapted to be installed as a unit.

26. The apparatus of claim 18, wherein the transformer comprises a third winding and the first and second series circuits each further comprises the third winding.

27. The apparatus of claim 26, wherein the first, second, and third windings are configured in the first series circuit to carry current in one direction and in the second series circuit to carry current in another direction opposite to the one direction.

28. The apparatus of claim 26, wherein the first set of switches includes one or more switches that are not in the second set of switches.

29. The apparatus of claim 26, wherein the first set of switches does not include any switches that are in the second set of switches.

30. The apparatus of claim 16, wherein the transformer comprises a third winding and the first series circuit and the second series circuit each comprises at least two windings of the transformer.

31. The apparatus of claims 30, wherein the bus converter circuit is a self-contained assembly adapted to be installed as a unit.

32. A computer apparatus, comprising:

a power distribution system including an input bus for receiving power at a relatively high safe voltage, preferably approximately 48 Volts;

one or more bus converter circuits of claim 30, connected to receive power from the input bus;

one or more power busses connected to receive power from the one or more bus converter circuits;

a plurality of regulators, each having an input connected to receive power from the one or more power busses and an output for delivering a regulated output; and

one or more semiconductor processors connected to receive power from one or more of the plurality of regulators.

33. The apparatus of claim 4, wherein the voltage across the first ZVS switch is reduced to nearly zero before the first ZVS switch is turned ON and the voltage across the second ZVS switch is reduced to nearly zero before the second ZVS switch is turned ON.

34. The apparatus of claim 1, wherein the voltage across the first ZVS switch is reduced to nearly zero before the first ZVS switch is turned ON and the voltage across the second ZVS switch is reduced to nearly zero before the second ZVS switch is turned ON.

35. The apparatus of claim 1, wherein at least one of the windings is coupled to the input and at least one of the windings is coupled to the output during the power transfer intervals.

36. The apparatus of claim 35, wherein the first winding is coupled to the input during the first power transfer interval and the second winding is coupled to the output during the first power transfer interval.

37. The apparatus of claim 36, wherein the transformer comprises a third winding and the third winding is coupled to the output during the second power transfer interval.

38. The apparatus of claim 1, wherein the bus converter circuit is a self-contained assembly adapted to be installed as a unit.

39. The apparatus of claim 38, wherein the direction is the first direction.

40. The apparatus of claim 6, wherein the respective load comprises a computer processor.

41. The apparatus of claim 1, wherein the first series circuit comprises one or more of the following: (a) at least one component that is not in the second series circuit, (b) at least one component that is in the second series circuit but is connected in an order that is different from in the second series circuit, or (c) at least one component that is in the second series circuit but is connected to carry a current that flows in a direction that is opposite from a current that the component carries in the second series circuit.

42. A computer apparatus, comprising:

a power distribution system including an input bus for receiving power at a relatively high safe voltage, preferably approximately 48 Volts;

one or more bus converter circuits of claim 41, connected to receive power from the input bus;

one or more power busses connected to receive power from the one or more bus converter circuits;

a plurality of regulators, each having an input connected to receive power from the one or more power busses and an output for delivering a regulated output; and

one or more semiconductor processors connected to receive power from one or more of the plurality of regulators.

43. The apparatus of claim **1**, wherein the first set of switches includes one or more switches that are not in the second set of switches.

44. The apparatus of claim **1**, wherein the first set of switches does not include any switches that are in the second set of switches.

45. The apparatus of claim **1**, wherein at least one winding of the first series circuit is different than at least one winding of the second series circuit.

46. The apparatus of claim **1**, wherein at least one winding of the first series circuit is the same as at least one winding of the second series circuit.

47. The apparatus of claim **46**, wherein the at least one winding is configured in the first series circuit to carry current in one direction and in the second series circuit to carry current in another direction opposite to the one direction.

48. The apparatus of claim **46**, wherein the first series circuit and the second series circuit each comprises at least two windings of the transformer.

49. A computer apparatus, comprising:

a power distribution system including an input bus for receiving power at a relatively high safe voltage, preferably approximately 48 Volts;

one or more bus converter circuits of claim **41**, connected to receive power from the input bus;

one or more power busses connected to receive power from the one or more bus converter circuits;

a plurality of regulators, each having an input connected to receive power from the one or more power busses and an output for delivering a regulated output; and

one or more semiconductor processors connected to receive power from one or more of the plurality of regulators.

50. The apparatus of claim **49**, wherein the bus converter circuit is a self-contained assembly adapted to be installed as a unit.

51. The apparatus of claim **48**, wherein the at least two windings in the first and second series circuits each comprises the first winding and the second winding, and the first winding and the second winding are configured in the first series circuit to carry current in one direction and are configured in the second series circuit to carry current in another direction opposite to the one direction.

52. The apparatus of claim **51**, wherein the first and second windings are configured in a first order in the first series circuit and in a second different order in the second series circuit.

53. The apparatus of claim **52**, wherein the first and second windings are configured in the first series circuit for current to flow in the one direction and in the second series circuit for current to flow in the another direction.

54. The apparatus of claim **51**, wherein the transformer comprises a third winding and the first and second series circuits each further comprise the third winding.

55. The apparatus of claim **54**, wherein the first, second, and third windings are configured in the first series circuit to carry current in the one direction and in the second series circuit to carry current in the another direction.

56. The apparatus of claim **54**, wherein the first set of switches does not include any switches that are in the second set of switches.

57. The apparatus of claim **54**, wherein the first set of switches does not include any switches that are in the second set of switches.

58. The apparatus of claim **56**, wherein the bus converter circuit is a self-contained assembly adapted to be installed as a unit.

59. The apparatus of claim **58**, wherein the bus converter circuit is a self-contained assembly adapted to be installed as a unit.

60. The apparatus of claim **46**, wherein the transformer comprises a third winding and the first series circuit and the second series circuit each comprises at least two windings of the transformer.

61. A computer apparatus, comprising:

a power distribution system including an input bus for receiving power at a relatively high safe voltage, preferably approximately 48 Volts;

one or more bus converter circuits of claim **60**, connected to receive power from the input bus;

one or more power busses connected to receive power from the one or more bus converter circuits;

a plurality of regulators, each having an input connected to receive power from the one or more power busses and an output for delivering a regulated output; and

one or more semiconductor processors connected to receive power from one or more of the plurality of regulators.

62. The apparatus of claim **61**, wherein one or more of the bus converter circuits is a self-contained assembly adapted to be installed as a unit.

63. The apparatus of claim **1**, wherein the first winding and the second winding are connected together at a node and the second terminal is connected to receive power from the node.

64. The apparatus of claim **63**, wherein the first winding and the second winding comprise an equal number of turns and the bus converter circuit is further capable of converting power in either the first direction or the second direction.

65. The apparatus of claim **64**, wherein the transformer further comprises a third winding, and the first and second series circuits each include at least two windings.

66. The apparatus of claim **1**, wherein the first winding and second winding are connected together at a node and the common terminal is connected to the node.

67. The apparatus of claim **66**, wherein the first winding and the second winding comprise an equal number of turns, and the bus converter circuit is further capable of converting power in either the first direction or a second opposite direction.

68. A method, comprising:

providing a bus converter circuit having a first terminal, a second terminal, and a common terminal and being configured to convert power in a direction, the direction being one of the following:

(a) a first direction in which the first terminal and common terminal form an input for receiving input power at a first voltage, V1, and the second terminal and the common terminal form an output for delivering output power at a second voltage, V2, or

(b) a second direction in which the second terminal and the common terminal form an input for receiving input power at the second voltage, V2, and the first

terminal and the common terminal form an output for delivering output power at the first voltage, V1;

galvanically connecting the input and the output;

wherein over a range of input voltages the bus converter circuit a uses an essentially fixed voltage transformation ratio, K, equal to the second voltage, V2 divided by the first voltage, V1, (K=V2/V1), to convert power in the direction, such that output power delivered in the first direction is at the second voltage, V2=K×V1, and output power delivered in the second direction is at the first voltage, V1=V2/K;

wherein the first voltage, V1, is greater than the second voltage, V2;

wherein the bus converter circuit includes (i) a transformer having a first winding and a second winding, (ii) a plurality of switches, and (iii) a controller;

operating, by the controller, the plurality of switches in a series of converter operating cycles including a first and a second power transfer interval, the first and second power transfer intervals having essentially equal durations, and wherein during the first power transfer interval a first set of the plurality of switches is ON and power is converted in the direction, and during the second power transfer interval a second set of the plurality of switches is ON and power is converted in the direction;

forming, by the bus converter circuit, during the first power transfer interval a first series circuit in which at least the following elements are all connected in series without regard to order: at least one of the first or second terminals, at least one of the first or second windings of the transformer, at least one of the plurality of switches in the first set, and at least one capacitor, and conducting, by the bus converter circuit, current in the direction between the first terminal and the second terminal;

forming, by the bus converter circuit, during the second power transfer interval a second series circuit in which at least the following elements are all connected in series without regard to order: at least one of the first and second terminals, at least one of the first or second windings of the transformer, at least one of the plurality of switches in the second set, and at least one capacitor, and conducting, by the bus converter circuit, current in the direction between the first terminal and the second terminal;

before the first power transfer interval, reducing, by the bus converter circuit, a voltage across a first ZVS switch prior to turning the first ZVS switch ON, such that the voltage across the first ZVS switch is reduced when the first ZVS switch is turned ON, the first ZVS switch being at least one of the plurality of switches in the first set; and

reducing, by the bus converter circuit, a voltage across a second ZVS switch prior to turning the second ZVS switch ON, such that the voltage across the second ZVS switch is reduced when the second ZVS switch is turned ON, the second ZVS switch being at least one of the plurality of switches in the second set.

69. The method of claim **68**, further comprising providing inrush current control at least during start-up of the bus converter circuit.

70. The method of claim **68**, further comprising providing the bus converter circuit as a self-contained assembly.

71. The method of claim **68**, wherein forming the first and second series circuits includes at least two of the first and second terminals.

72. The method of claim **71**, wherein the bus converter circuit is capable of converting power in either of the first direction or the second direction and the direction is a function of conditions external to the bus converter circuit.

73. The method of claim **71**, wherein at least one winding of the first series circuit is the same as at least one winding of the second series circuit; and the at least one winding of the first series circuit is connected to carry current in one direction and the at least one winding of the second series circuit is connected to carry current in another direction opposite to the one direction.

74. The method of claim **71**, wherein at least one winding of the first series circuit is different than at least one winding of the second series circuit.

75. The method of claim **74**, comprising connecting the first, second, and third windings in the first series circuit to carry current in one direction and in the second series circuit to carry current in another direction opposite to the one direction.

76. The method of claim **71**, wherein the voltage across the first ZVS switch is reduced to nearly zero before the first ZVS switch is turned ON and the voltage across the second ZVS switch is reduced to nearly zero before the second ZVS switch is turned ON.

77. The method of claim **68**, wherein the first series circuit and the second series circuit each comprises at least two windings of the transformer.

78. The method of claim **77**, comprising:

connecting the first winding and the second winding in the first series circuit to carry current in the one direction; and

connecting the first winding and the second winding in the second series circuit to carry current in the another direction.

79. The method of claim **77**, comprising connecting the first and second windings in a first order in the first series circuit and in a second different order in the second series circuit.

80. The method of claim **77**, wherein the first and second series circuits include the first and second terminals.

81. The method of claim **80**, wherein the transformer comprises a third winding and the first and second series circuits each further comprises the third winding.

82. The apparatus of claim **68**, wherein the first and second series circuits form a first and a second series resonant circuit, each having a characteristic resonant period; and the essentially equal duration of the first and second power transfer intervals is less than each characteristic resonant period.

83. The method of claim **68**, wherein the voltage across the first ZVS switch is reduced to nearly zero before the first ZVS switch is turned ON and the voltage across the second ZVS switch is reduced to nearly zero before the second ZVS switch is turned ON.

84. The method of claim **68**, further comprising:

providing an input power bus connected to supply power to the input of the bus converter circuit;

providing a power distribution bus connected to receive power at a relatively high safe voltage, preferably approximately 48 Volts, from the output of the bus converter circuit;

providing a plurality of regulators, each having an input connected to receive power from the power distribution bus and an output for delivering a regulated output; and

one or more semiconductor processors connected to receive power from one or more of the plurality of regulators.

85. A method of powering a computer processor, the method comprising:

using an input bus to distribute input power at a first voltage, V1;

using one or more non-isolated bus converters to convert power received from the input bus for delivery to an output at a second voltage, V2;

using one or more output power busses to distribute power from the one or more bus converters at the second voltage, V2, to one or more loads;

using a plurality of regulators to regulate power received from the output power busses for delivery via a regulator output to the one or more loads; and

wherein one or more of the loads comprise a computer processor;

wherein the one or more non-isolated bus converters have a first terminal, a second terminal, and a common terminal, and the first terminal and common terminal form an input connected to receive power from the input bus at the first voltage, V1, and the second terminal and the common terminal form an output for delivering output power at the second voltage, V2, to the one or more power busses;

wherein the input is galvanically connected to the output;

using an essentially fixed voltage transformation ratio, K, equal to the second voltage, V2 divided by the first voltage, V1, (K=V2/V1), to convert power in the one or more bus converters from the input for delivery to the output at the second voltage, V2=K×V1, over a range of input voltages;

wherein the first voltage, V1, is greater than the second voltage, V2;

wherein the one or more non-isolated bus converters include (i) a transformer having a first winding and a second winding, (ii) a plurality of switches, and (iii) a controller;

using the controller to operate the plurality of switches in a series of converter operating cycles including a first and a second power transfer interval, the first and second power transfer intervals having essentially equal durations, and wherein during the first power transfer interval a first set of the plurality of switches is ON and power is converted from the input to the output, and during the second power transfer interval a second set of the plurality of switches is ON and power is converted from the input to the output;

wherein the one or more non-isolated bus converters are configured, during the first power transfer interval to (a) form a first series circuit in which at least the following elements are all connected in series without regard to order: at least one of the first or second terminals, at least one of the first or second windings of the transformer, at least one of the plurality of switches in the first set, and at least one capacitor, and (b) convert current flowing through the first terminal into current flowing through the second terminal in inverse proportion to the essentially fixed voltage transformation ratio, K;

wherein the one or more non-isolated bus converters are configured during the second power transfer interval to (a) form a second series circuit in which at least the following elements are all connected in series without regard to order: at least one of the first and second terminals, at least one of the first or second windings of the transformer, at least one of the plurality of switches in the second set, and at least one capacitor, and (b) convert current flowing through the first terminal into current flowing through the second terminal in inverse proportion to the essentially fixed voltage transformation ratio, K;

wherein the one or more non-isolated bus converters are configured before the first power transfer interval, to reduce a voltage across a first ZVS switch prior to turning the first ZVS switch ON, such that the voltage across the first ZVS switch is reduced when the first ZVS switch is turned ON, the first ZVS switch being at least one of the plurality of switches in the first set; and

wherein the one or more non-isolated bus converters are configured before the second power transfer interval, to reduce a voltage across a second ZVS switch prior to turning the second ZVS switch ON, such that the voltage across the second ZVS switch is reduced when the second ZVS switch is turned ON, the second ZVS switch being at least one of the plurality of switches in the second set.

86. The method of claim 85, further comprising converting power from an AC utility line for delivery at a DC voltage, the converting providing voltage step down and galvanic isolation to provide a relatively high safe voltage, preferably approximately 48 Volts and wherein the first voltage, V1, is approximately 48 Volts.

87. The method of claim 85, wherein the first winding and the second winding are connected together at a node and further comprising delivering power via the node to the second terminal.

88. The method of claim 87, wherein the first winding comprises a first number of turns and the second winding comprise a second number of turns, and the first number and second number are equal.

89. A computer apparatus comprising:

a power distribution system including an input bus for receiving power at a relatively high safe voltage, preferably approximately 48 Volts;

one or more bus converter circuits connected to receive power from the input bus;

one or more power busses connected to receive power from the one or more bus converter circuits;

a plurality of regulators, each having an input connected to receive power from the one or more power busses and an output for delivering a regulated output; and

one or more semiconductor processors connected to receive power from one or more of the regulators;

wherein at least one of the one or more bus converter circuits has a first terminal, a second terminal, and a common terminal and is configured to convert power in a first direction in which the first terminal and common terminal form an input for receiving input power at a first voltage, V1, and the second terminal and the common terminal form an output for delivering output power at a second voltage, V2;

wherein the input and output are galvanically connected;

wherein over a range of input voltages the at least one of the one or more bus converter circuits uses an essentially fixed voltage transformation ratio, K, equal to the second voltage, V2 divided by the first voltage, V1, (K=V2/V1), to convert power in the first direction, such that output power delivered is at the second voltage, V2=K×V1;

wherein the first voltage, V1, is greater than the second voltage, V2;

wherein the at least one of the one or more bus converter circuits includes (i) a transformer having a first winding and a second winding, (ii) a plurality of switches, and

(iii) a controller configured to operate the plurality of switches in a series of converter operating cycles;

wherein each converter operating cycle includes a first and a second power transfer interval, the first and second power transfer intervals having essentially equal durations, and wherein during the first power transfer interval a first set of the plurality of switches is ON and power is converted in the first direction, and during the second power transfer interval a second set of the plurality of switches is ON and power is converted in the first direction;

wherein the at least one of the one or more bus converter circuits is configured during the first power transfer interval to (a) form a first series circuit in which at least the following elements are all connected in series without regard to order: at least one of the first or second terminals, at least one of the first or second windings of the transformer, at least one of the plurality of switches in the first set, and at least one capacitor, and (b) convert in the first direction current flowing through the first terminal into current flowing through the second terminal in inverse proportion to the essentially fixed voltage transformation ratio, K;

wherein the at least one of the one or more bus converter circuits is configured during the second power transfer interval to (a) form a second series circuit in which at least the following elements are all connected in series without regard to order: at least one of the first or second terminals, at least one of the first or second windings of the transformer, at least one of the plurality of switches in the second set, and at least one capacitor, and (b) convert in the first direction current flowing through the first terminal into current flowing through the second terminal in inverse proportion to the essentially fixed voltage transformation ratio, K;

wherein the at least one of the one or more bus converter circuits is configured to, before the first power transfer interval, reduce a voltage across a first ZVS switch prior to turning the first ZVS switch ON, such that the voltage across the first ZVS switch is reduced when the first ZVS switch is turned ON, the first ZVS switch being at least one of the plurality of switches in the first set; and

wherein the at least one of the one or more bus converter circuits is configured to, before the second power transfer interval, reduce a voltage across a second ZVS switch prior to turning the second ZVS switch ON, such that the voltage across the second ZVS switch is reduced when the second ZVS switch is turned ON, the second ZVS switch being at least one of the plurality of switches in the second set.

90. The apparatus of claim **89**, wherein the first series circuit comprises one or more of the following: (a) at least one component that is not in the second series circuit, (b) at least one component that is in the second series circuit but is connected in an order that is different from in the second series circuit, or (c) at least one component that is in the second series circuit but is connected to carry a current that flows in a direction that is opposite from a current that the component carries in the second series circuit.

91. The apparatus of claim **90**, wherein the first winding and the second winding are connected together at a node and the common terminal is connected to the node.

92. The apparatus of claim **91**, wherein the first winding and the second winding comprise an equal number of turns and the at least one of the one or more bus converter circuits is further capable of converting power in either the first direction or a second opposite direction.

93. The apparatus of claim **92**, wherein the transformer further comprises a third winding, and the first and second series circuits each include at least two windings.

94. The apparatus of claim **1**, wherein the first winding and second winding are connected together at a node and the second terminal is connected to receive power from the node.

95. The apparatus of claim **93**, wherein the first winding and the second winding comprise an equal number of turns, and the at least one of the one or more bus converter circuits is further capable of converting power in either the first direction or a second opposite direction.

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