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(54) **SEMICONDUCTOR PACKAGE AND METHOD OF MANUFACTURING THE SEMICONDUCTOR PACKAGE**

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(72) Inventor: **Hyunsoo Chung**, Suwon-si (KR)

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(52) **U.S. Cl.**
CPC ***H01L 25/0657*** (2013.01); ***H01L 23/06*** (2013.01); *H01L 2225/06541* (2013.01)

(57) **ABSTRACT**

A semiconductor package includes a buffer die, a plurality of core die blocks sequentially stacked on the buffer die, a top core die on an uppermost core die block of the plurality of core die blocks, and a molding member surrounding outer side surfaces of the plurality of core die blocks and the top core die on the buffer die. Each of the core die blocks includes a plurality of core dies sequentially stacked, and a plurality of gap filling portions surrounding outer side surfaces of at least two stages of core dies of the plurality of core dies. Outer side surfaces of the plurality of gap filling portions of each of the plurality of core die blocks are coplanar.

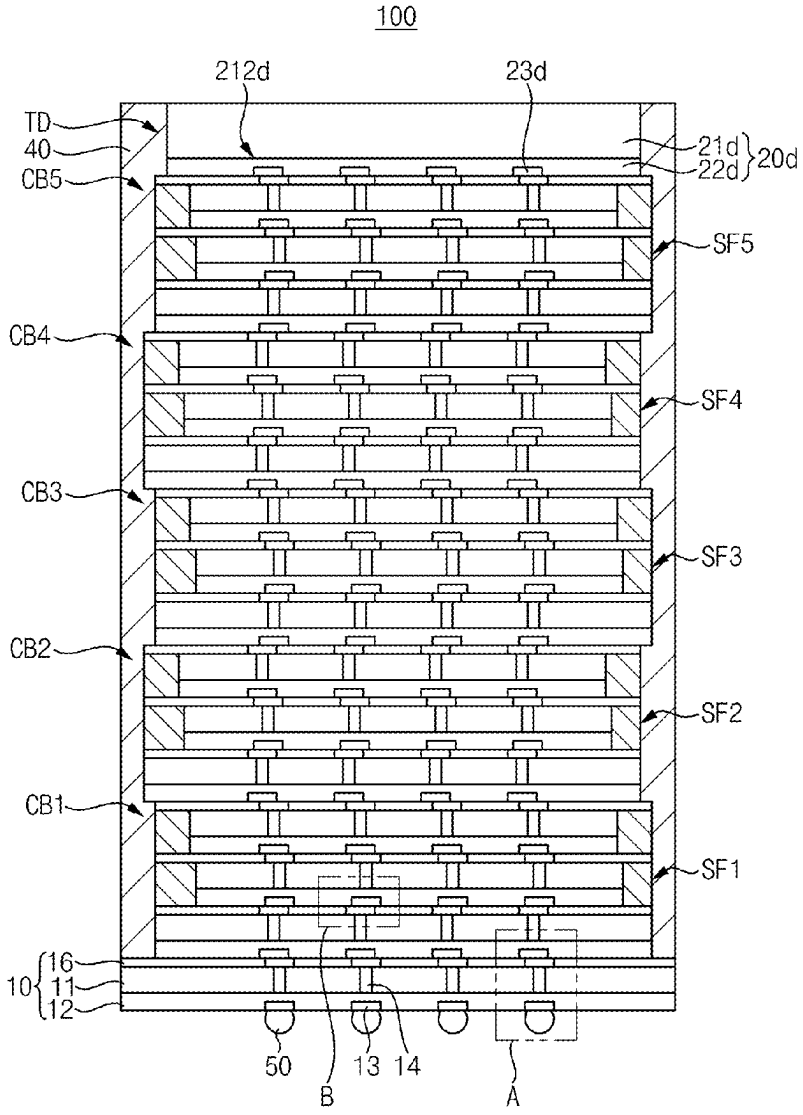


FIG. 1

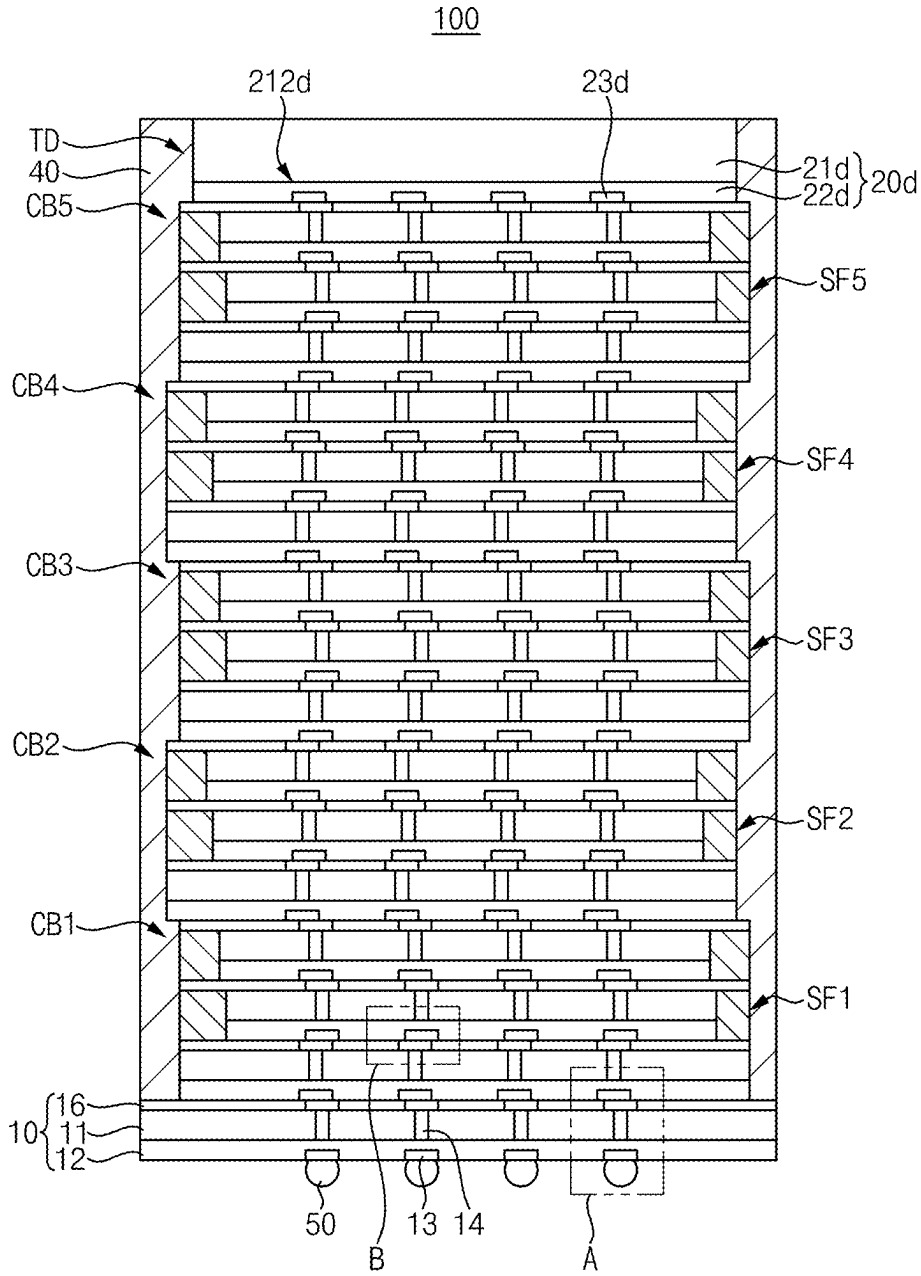

100
212d
23d
TD
40
CB5
21d
22d
20d
SF5
CB4
SF4
CB3
SF3
CB2
SF2
CB1
SF1
10
16
11
12
50
B
13
14
A

FIG. 2

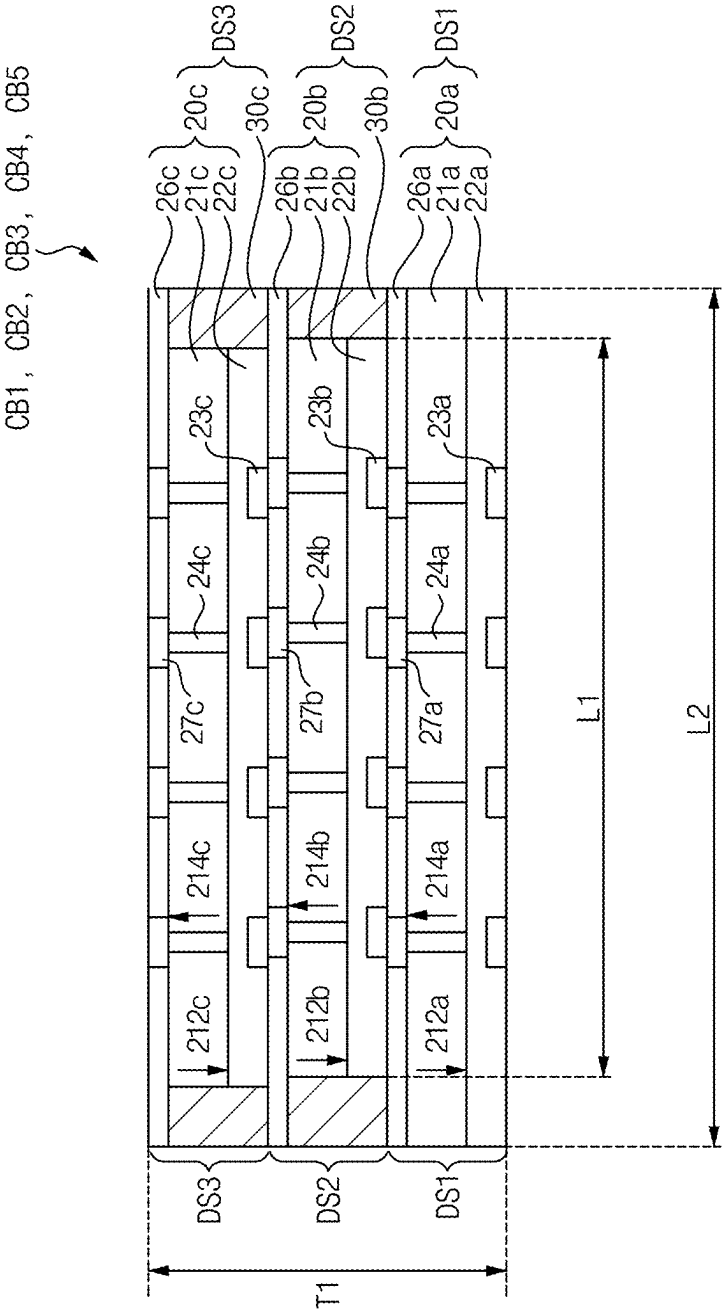

CB1, CB2, CB3, CB4, CB5
DS3
DS2
DS1
20c
20b
20a
30c
30b
26c
21c
22c
26b
21b
22b
26a
21a
22a
23c
23b
23a
24c
24b
24a
27c
27b
27a
214c
214b
214a
212c
212b
212a
L1
L2
T1

FIG. 3

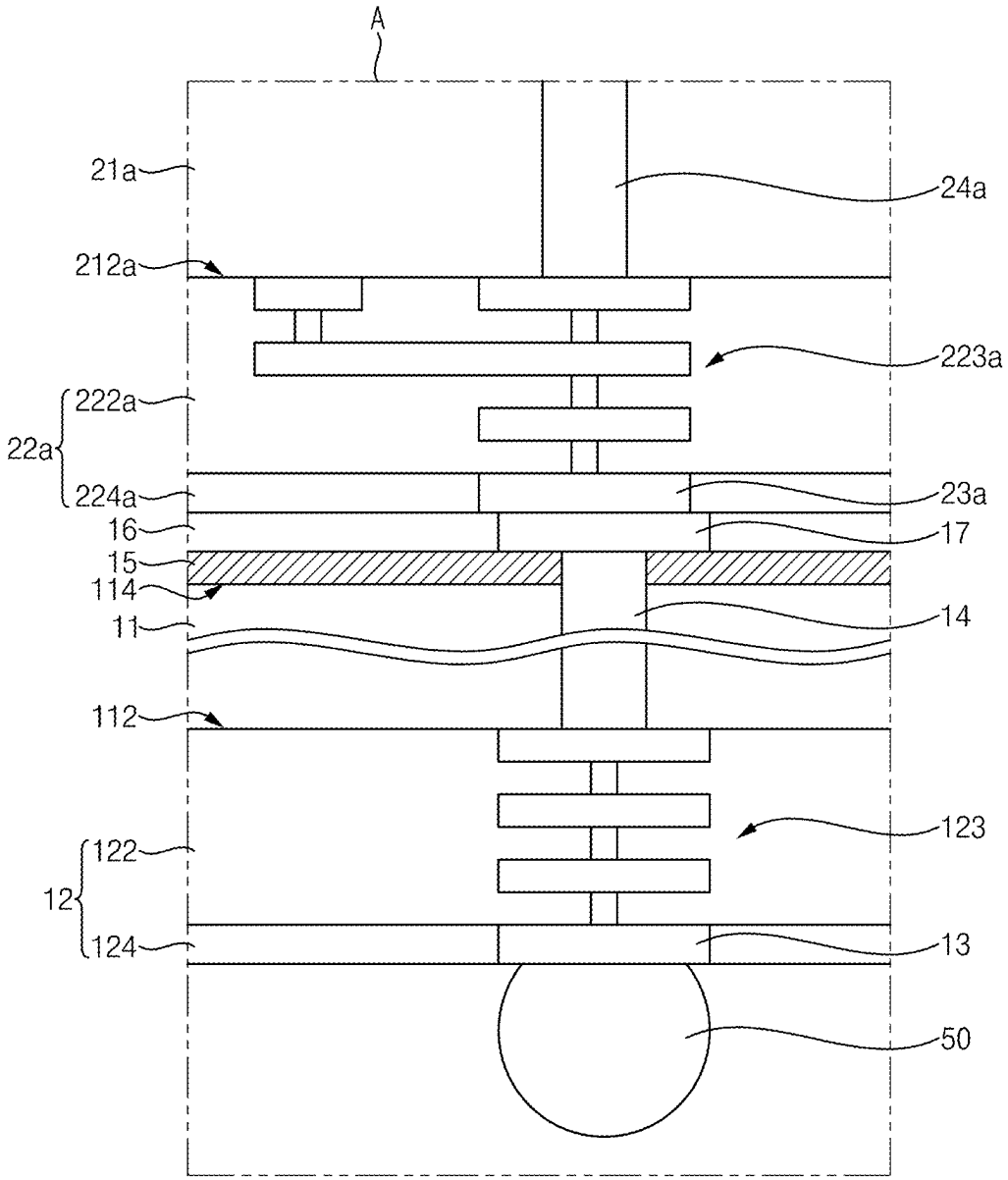

A
21a
24a
212a
223a
22a
222a
224a
23a
16
17
15
114
14
11
112
123
12
122
124
13
50

FIG. 4

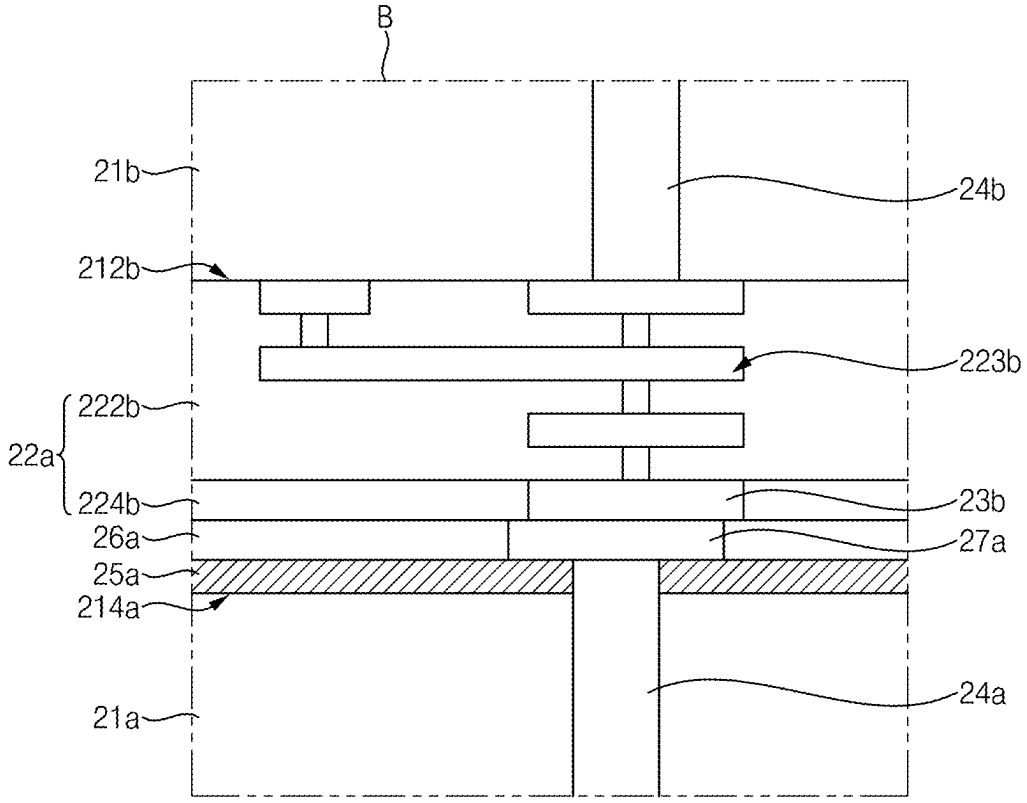


FIG. 5

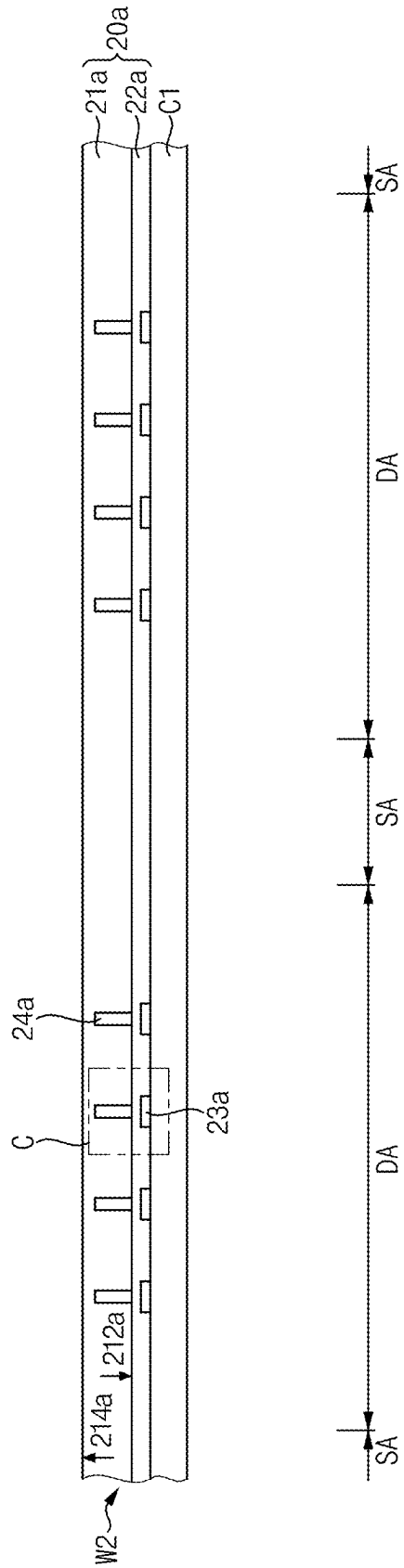


FIG. 6

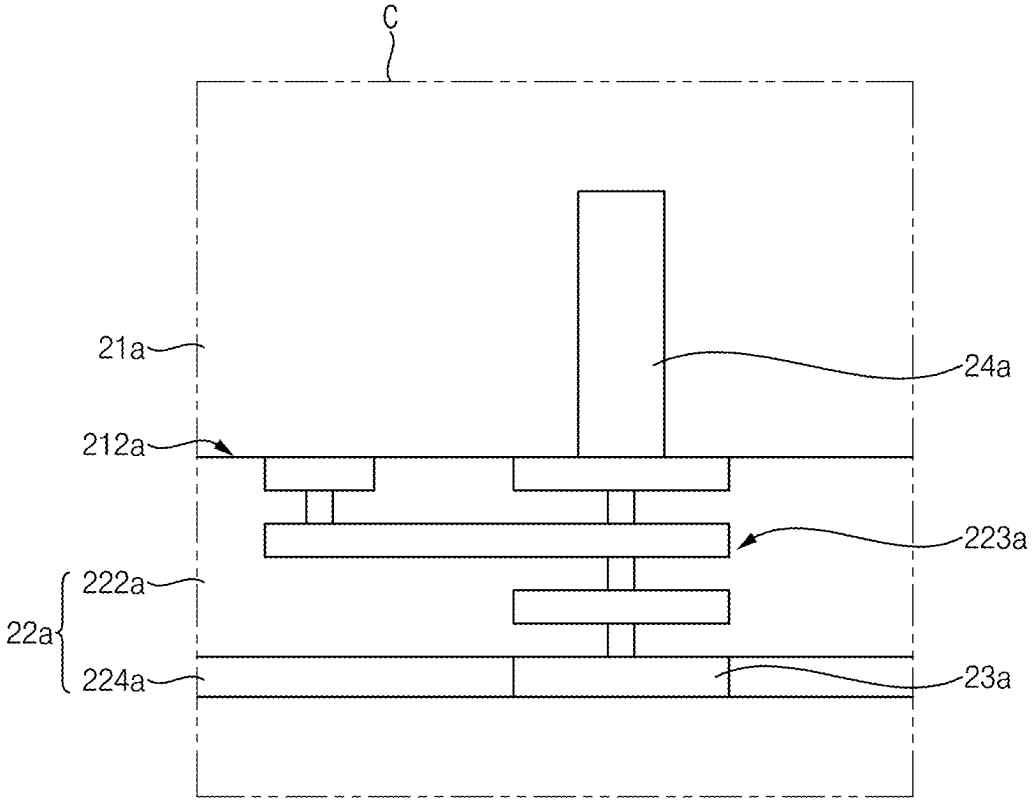


FIG. 7

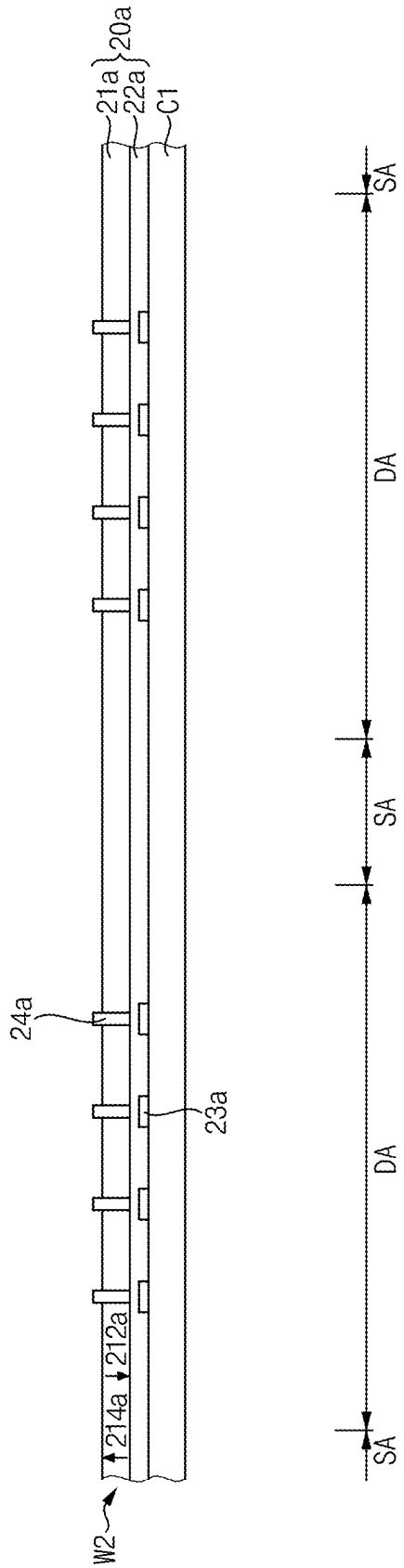


FIG. 8

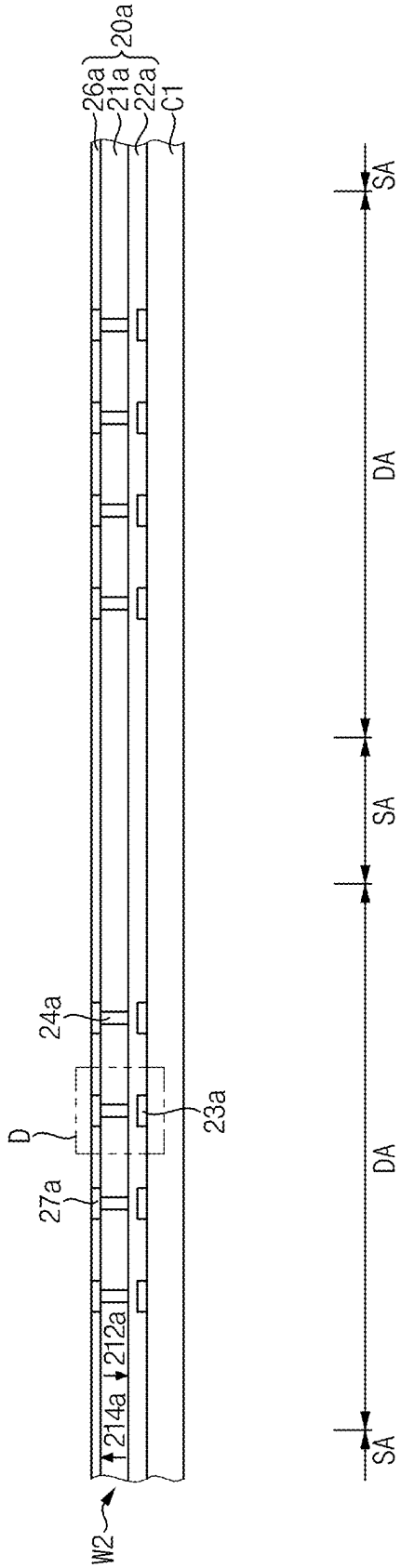


FIG. 9

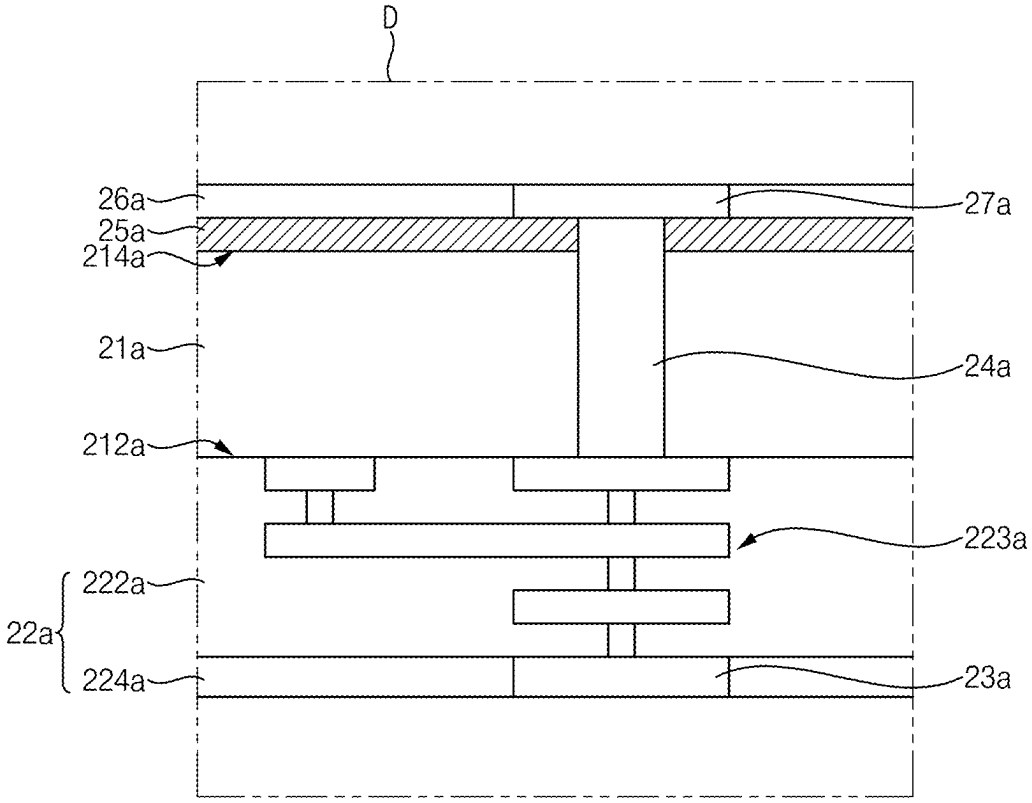


FIG. 10

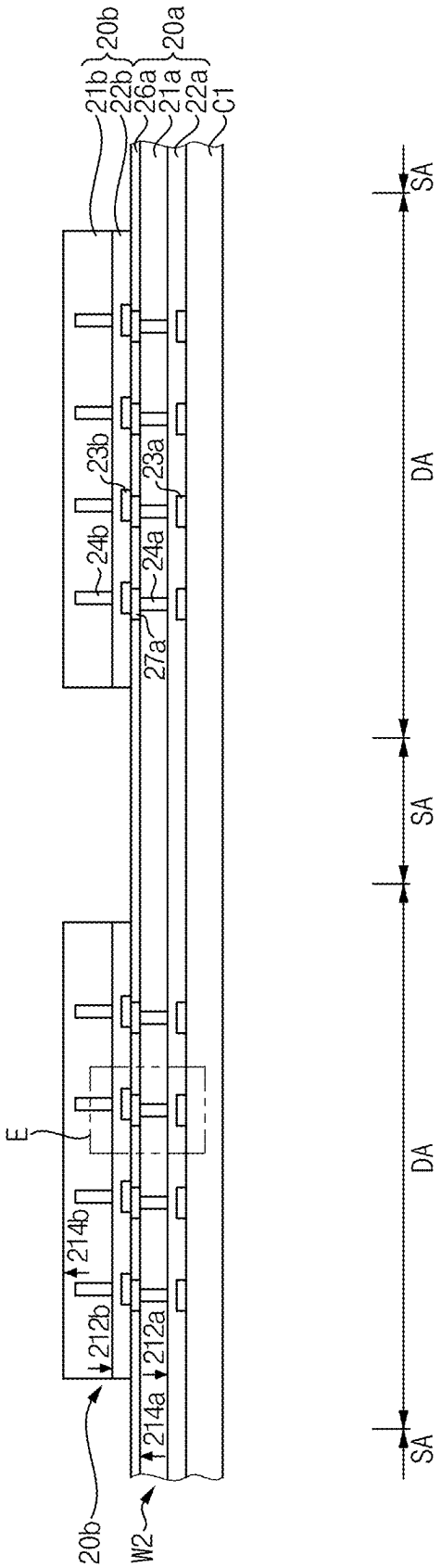

20b
20a
21b
22b
26a
21a
22a
C1
23b
23a
24b
24a
27a
E
214b
212b
212a
214a
20b
W2
SA
DA
SA
DA
SA

FIG. 11

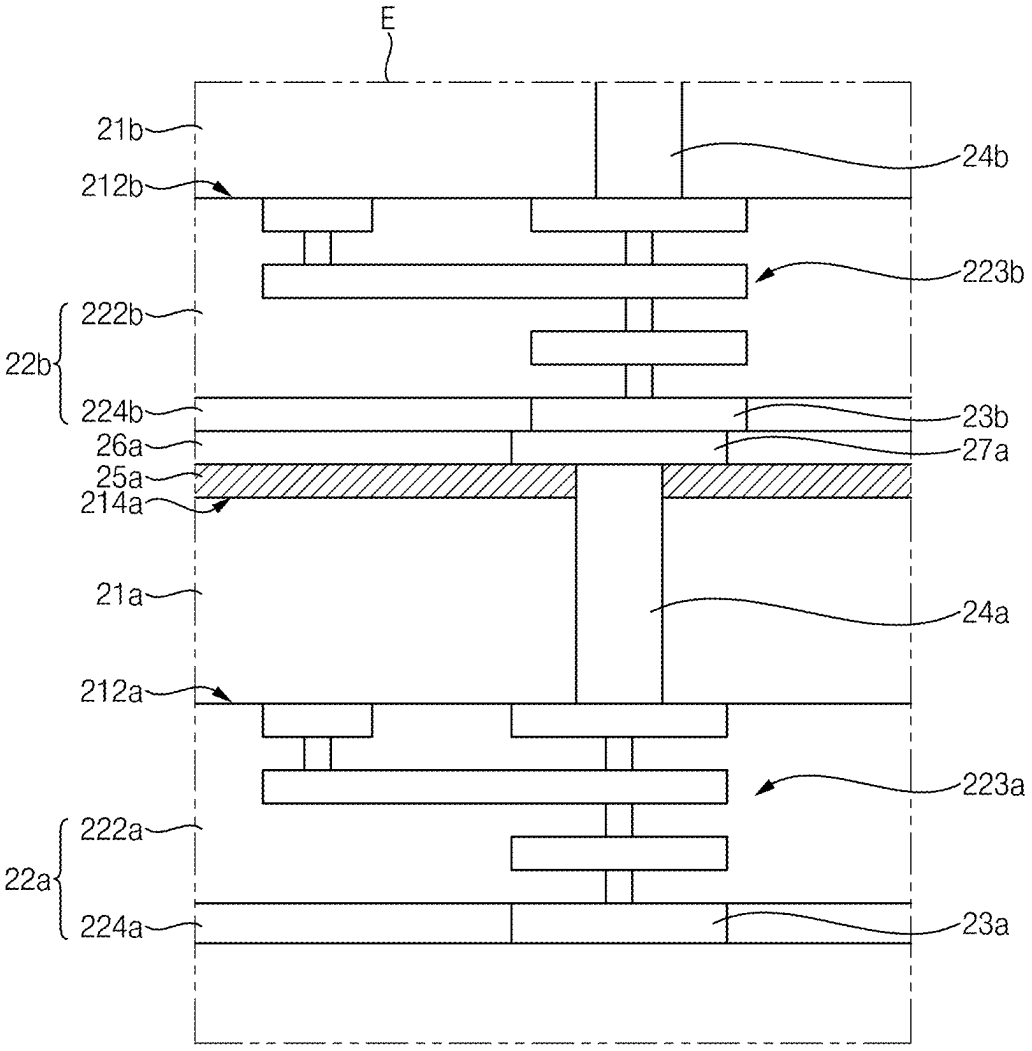

E
21b
24b
212b
223b
22b
222b
224b
23b
26a
27a
25a
214a
21a
24a
212a
223a
22a
222a
224a
23a

FIG. 12

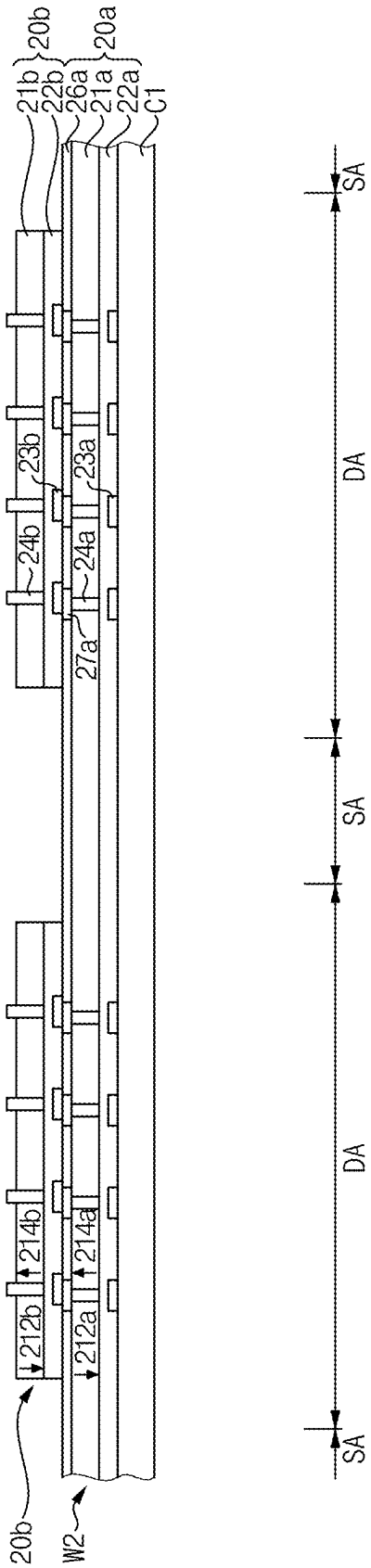

20b
20a
21b
22b
26a
21a
22a
C1
23b
23a
24b
24a
27a
214b
214a
212b
212a
20b
W2
SA
DA
SA
DA
SA

FIG. 13

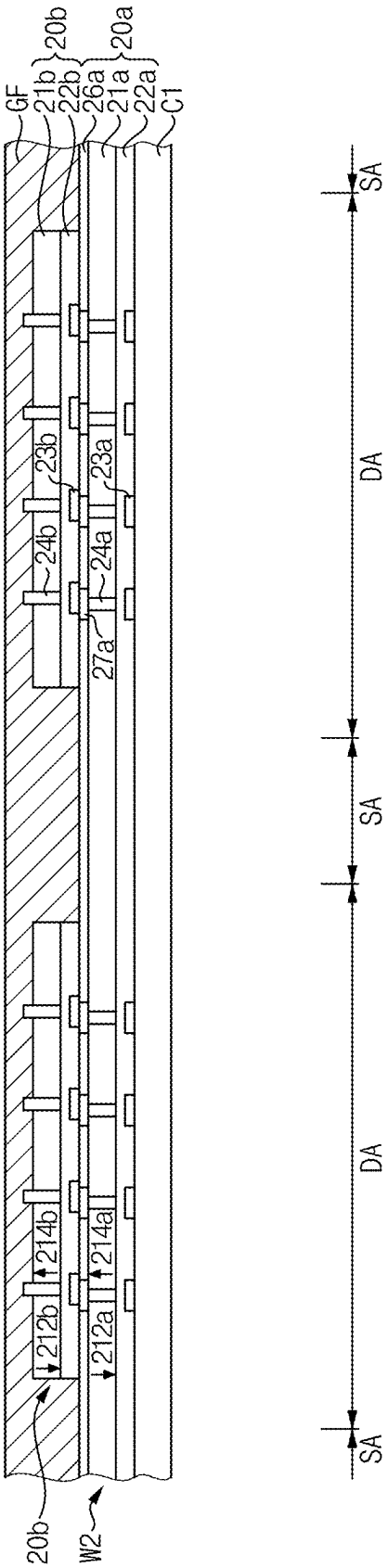

GF
21b
22b
20b
26a
21a
22a
20a
C1
23b
23a
24b
24a
27a
214b
214a
212b
212a
20b
W2
SA
DA
SA
DA
SA

FIG. 14

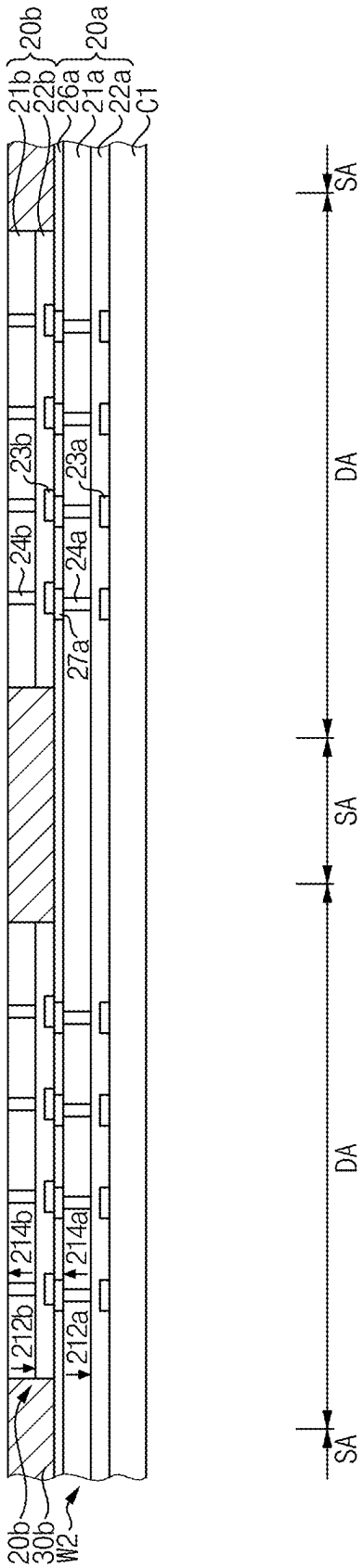

20b
21b
22b
26a
20a
21a
22a
C1
23b
23a
24b
24a
27a
214b
214a
212b
212a
20b
30b
W2
SA
DA
SA
DA
SA

FIG. 15

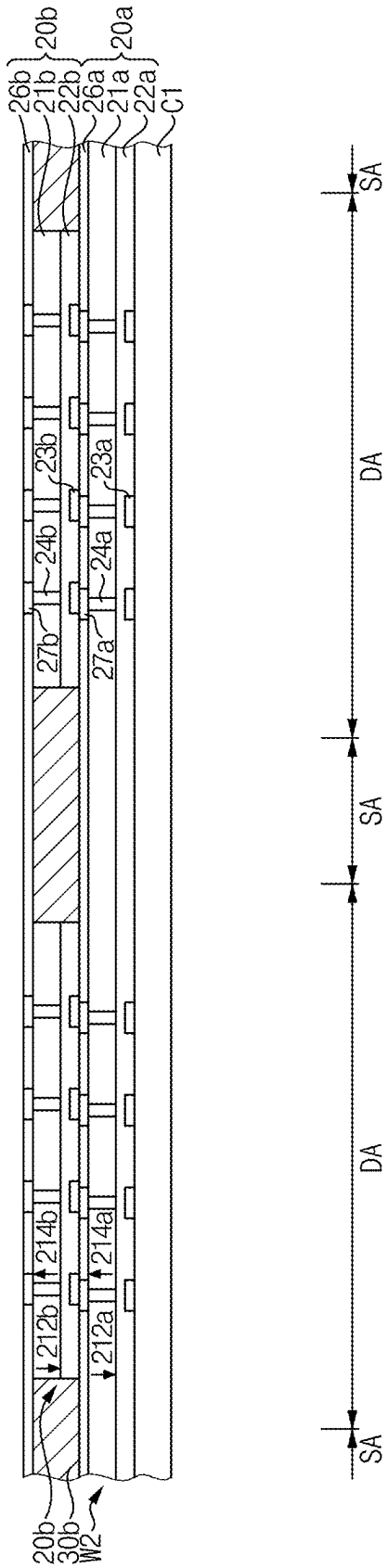

20b
20a
26b
21b
22b
26a
21a
22a
C1
23b
23a
24b
24a
27b
27a
214b
214a
212b
212a
20b
30b
W2
SA
DA
SA
DA
SA

FIG. 16

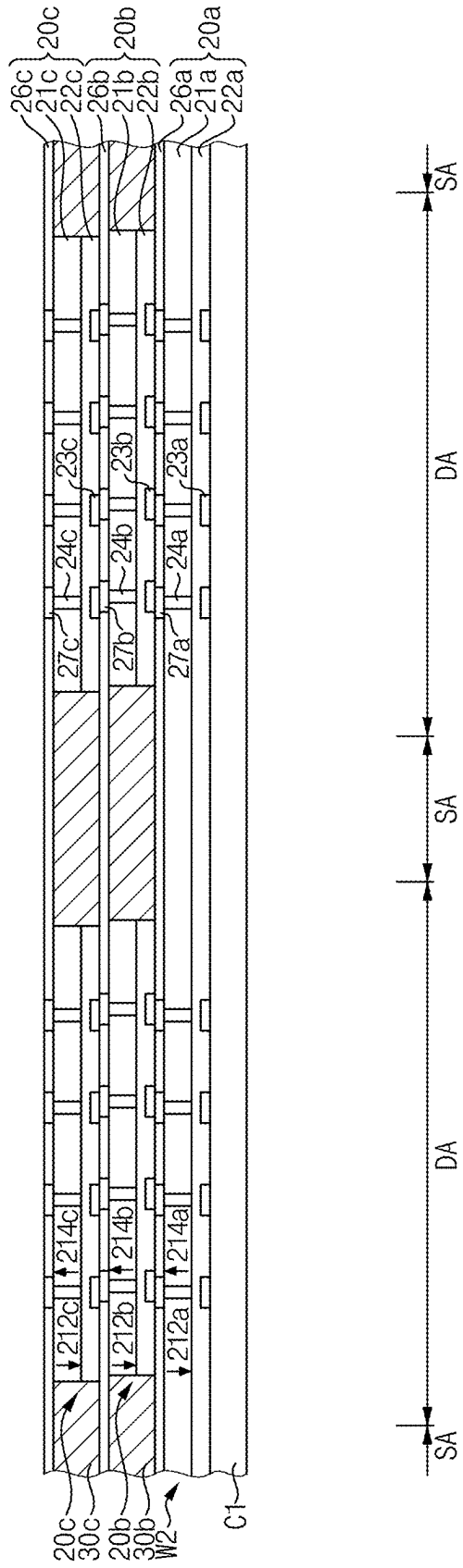

20c
20b
20a
26c
21c
22c
26b
21b
22b
26a
21a
22a
23c
23b
23a
24c
24b
24a
27c
27b
27a
214c
214b
214a
212c
212b
212a
20c
30c
20b
30b
W2
C1
SA
DA
SA
DA
SA

FIG. 17

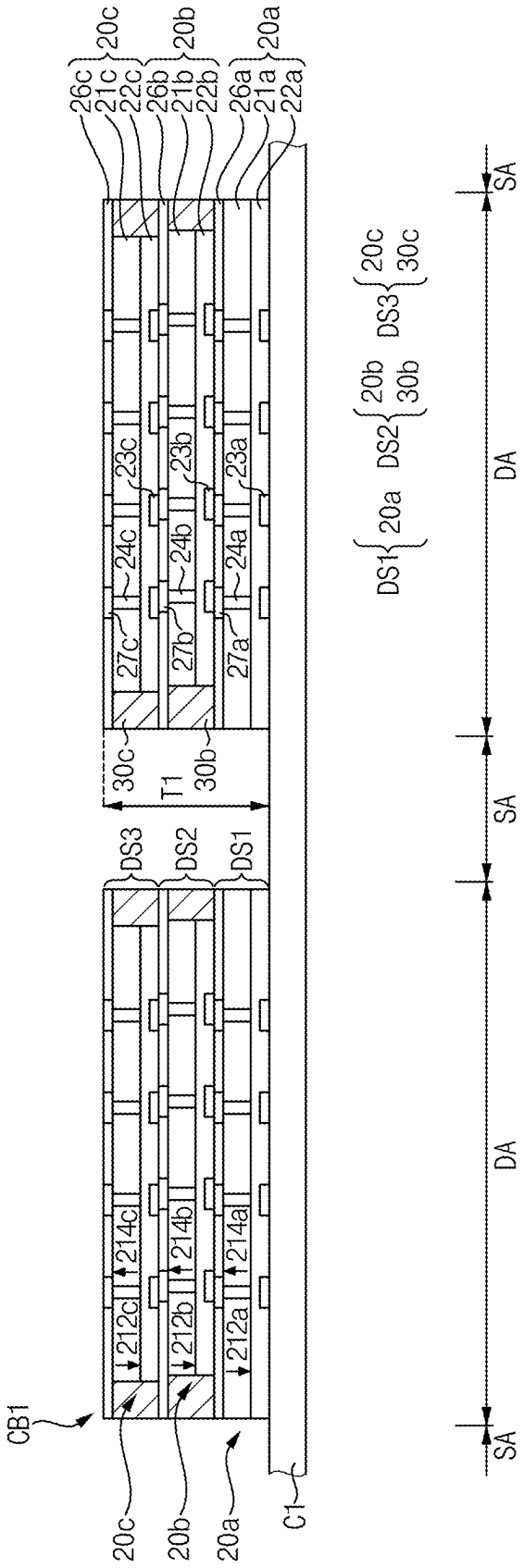

20c
20b
20a
26c
21c
22c
26b
21b
22b
26a
21a
22a
23c
23b
23a
24c
24b
24a
27c
27b
27a
30c
T1
30b
DS3
DS2
DS1
212c
214c
212b
214b
212a
214a
CB1
C1
SA
DA
SA
DA
SA
DS1 20a
DS2 20b 30b
DS3 20c 30c

FIG. 18

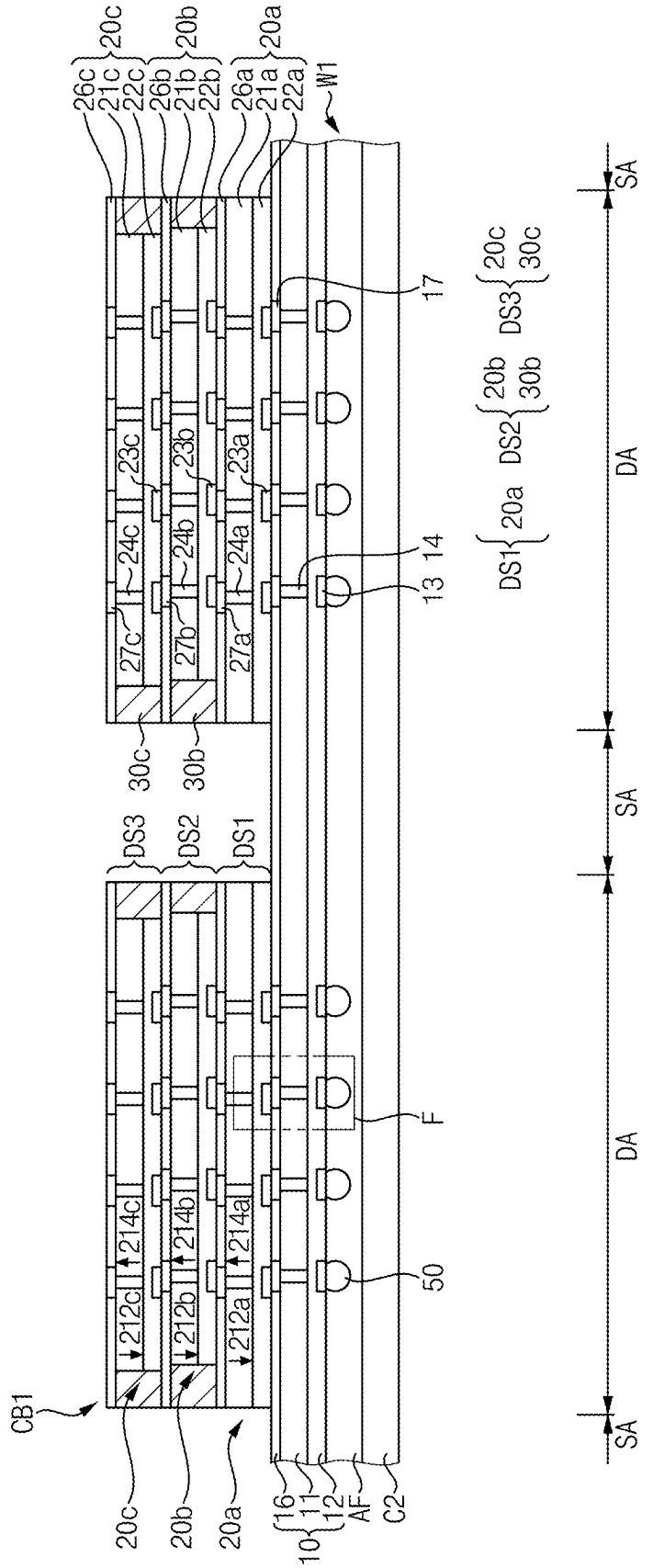

20c
20b
20a
26c
21c
22c
26b
21b
22b
26a
21a
22a
W1
17
13
14
23c
23b
23a
24c
24b
24a
27c
27b
27a
30c
30b
DS3
DS2
DS1
F
50
CB1
212c
214c
212b
214b
212a
214a
16
11
12
AF
C2
10
SA
DA
SA
DA
SA

FIG. 19

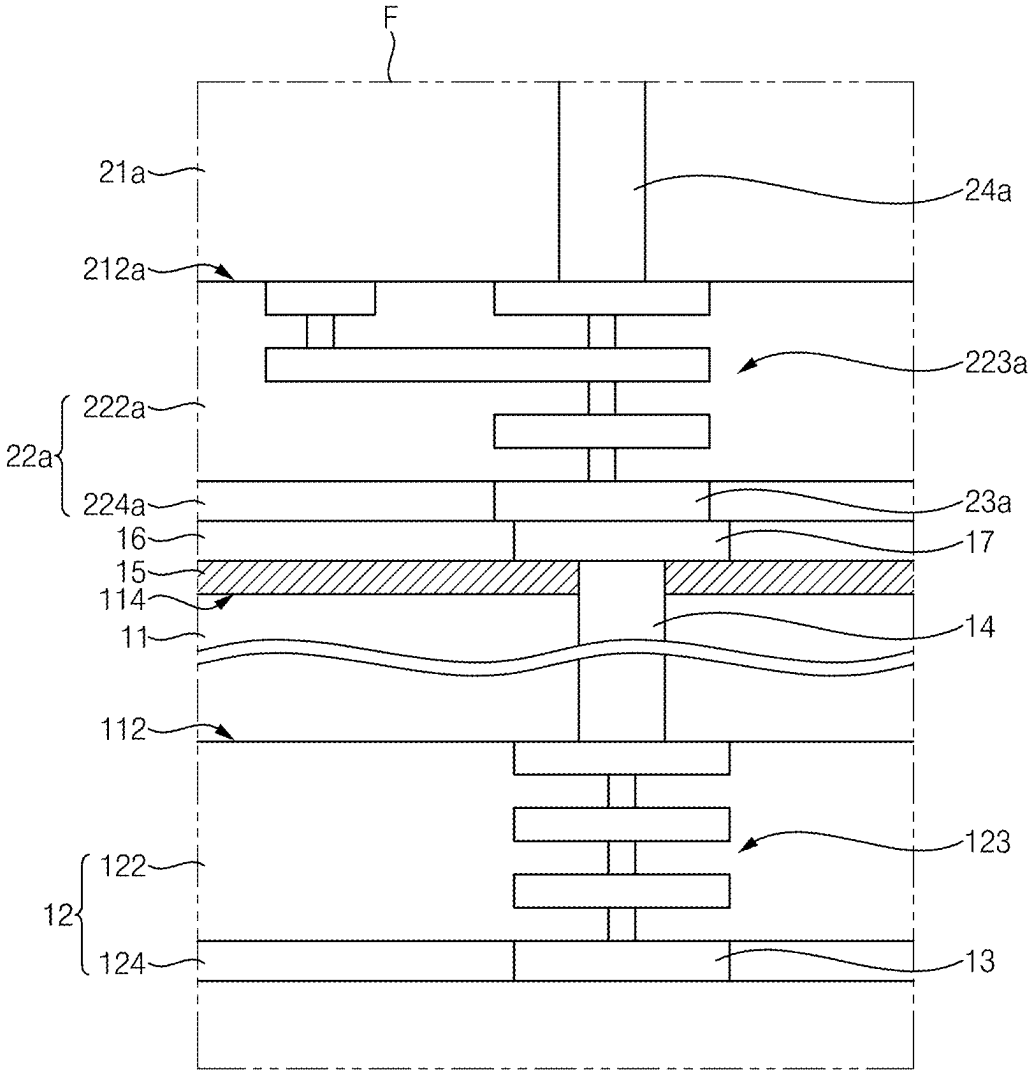

F
21a
24a
212a
223a
222a
22a
224a
23a
16
17
15
114
14
11
112
123
122
12
124
13

FIG. 20

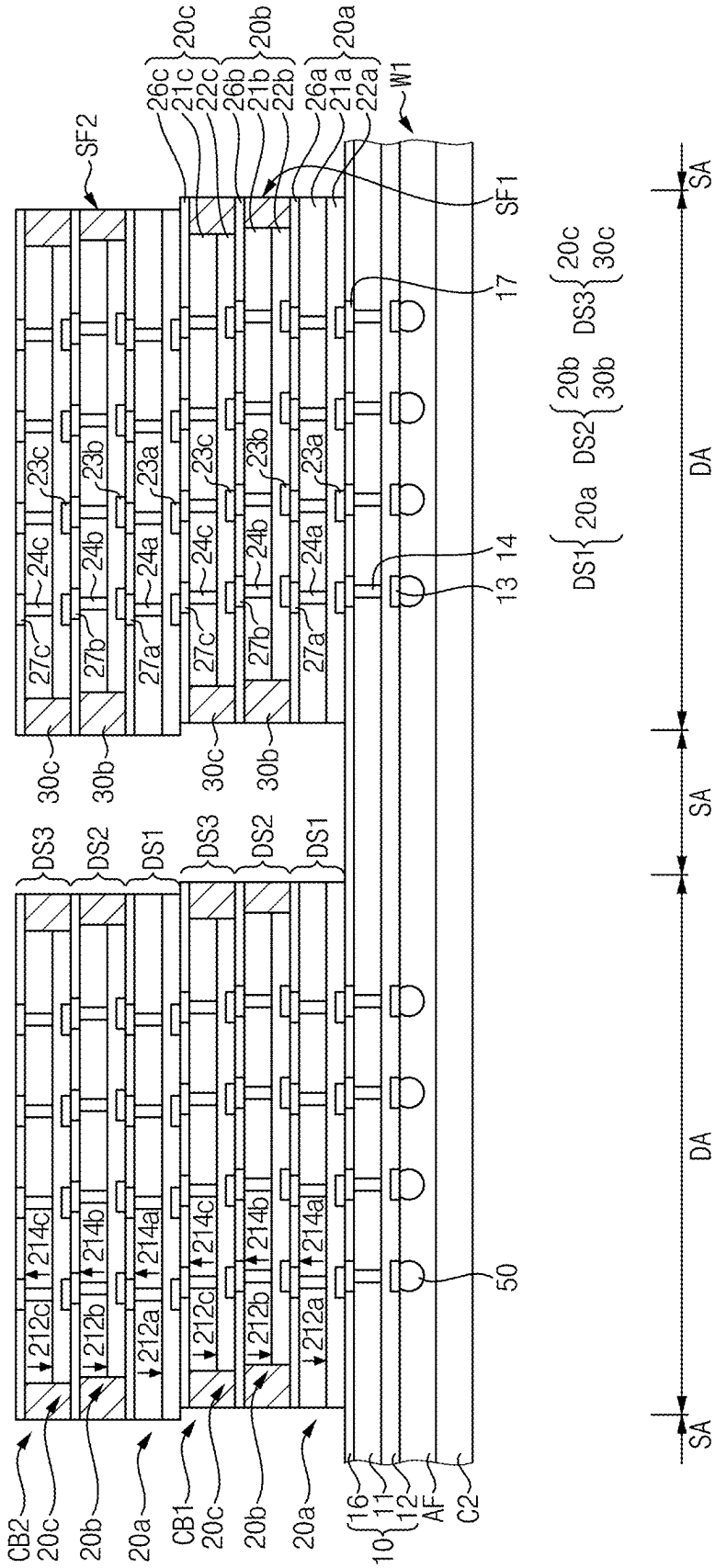

SF2
SF1
W1
17
13
14
50
DS1
DS2
DS3
20a
20b
20c
30b
30c
CB1
CB2
10
11
12
16
AF
C2
SA
DA

FIG. 21

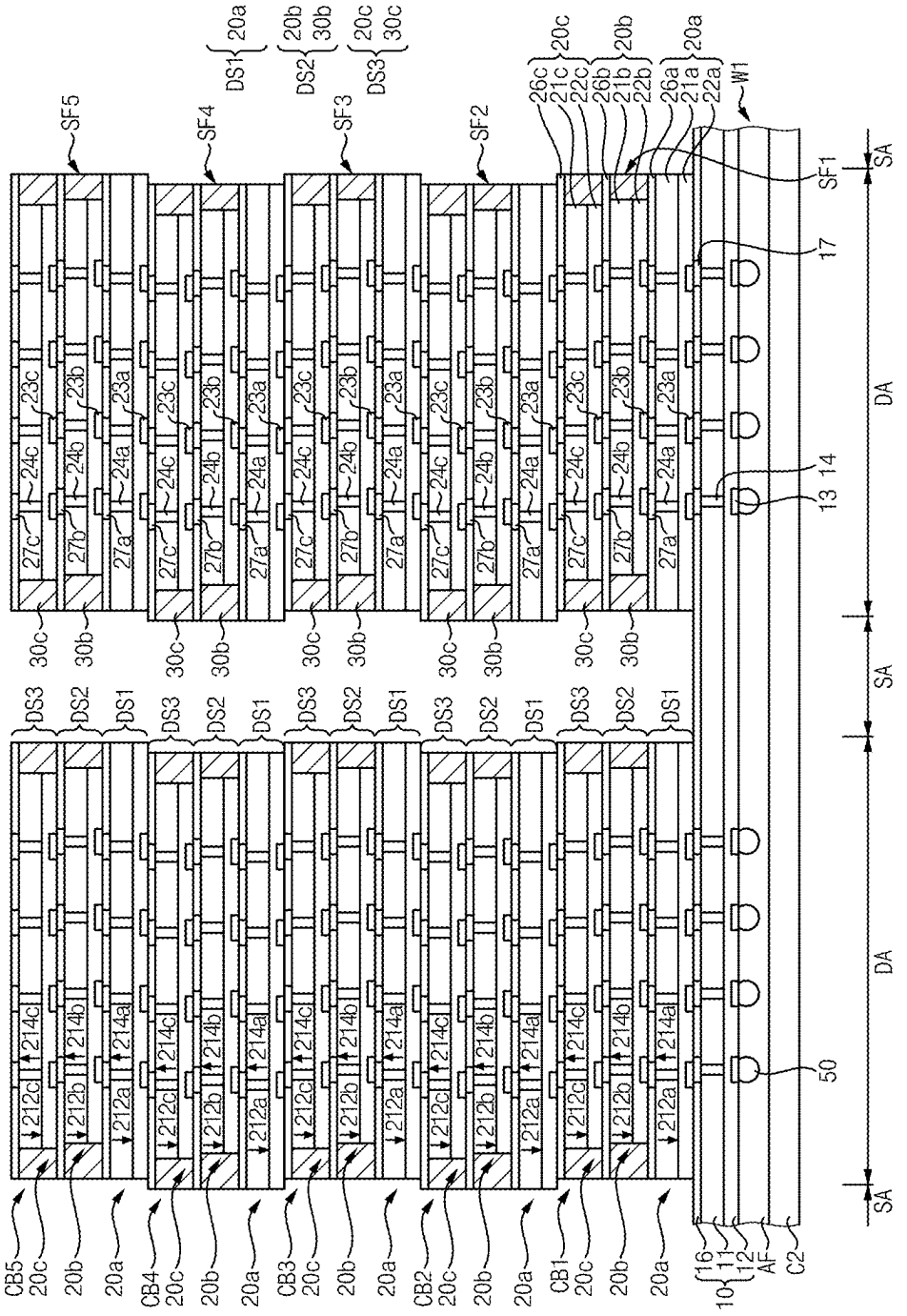

SF5
SF4
SF3
SF2
SF1
DS1
DS2
DS3
W1
17
14
13
50
SA
DA
CB5
CB4
CB3
CB2
CB1
AF
C2

FIG. 22

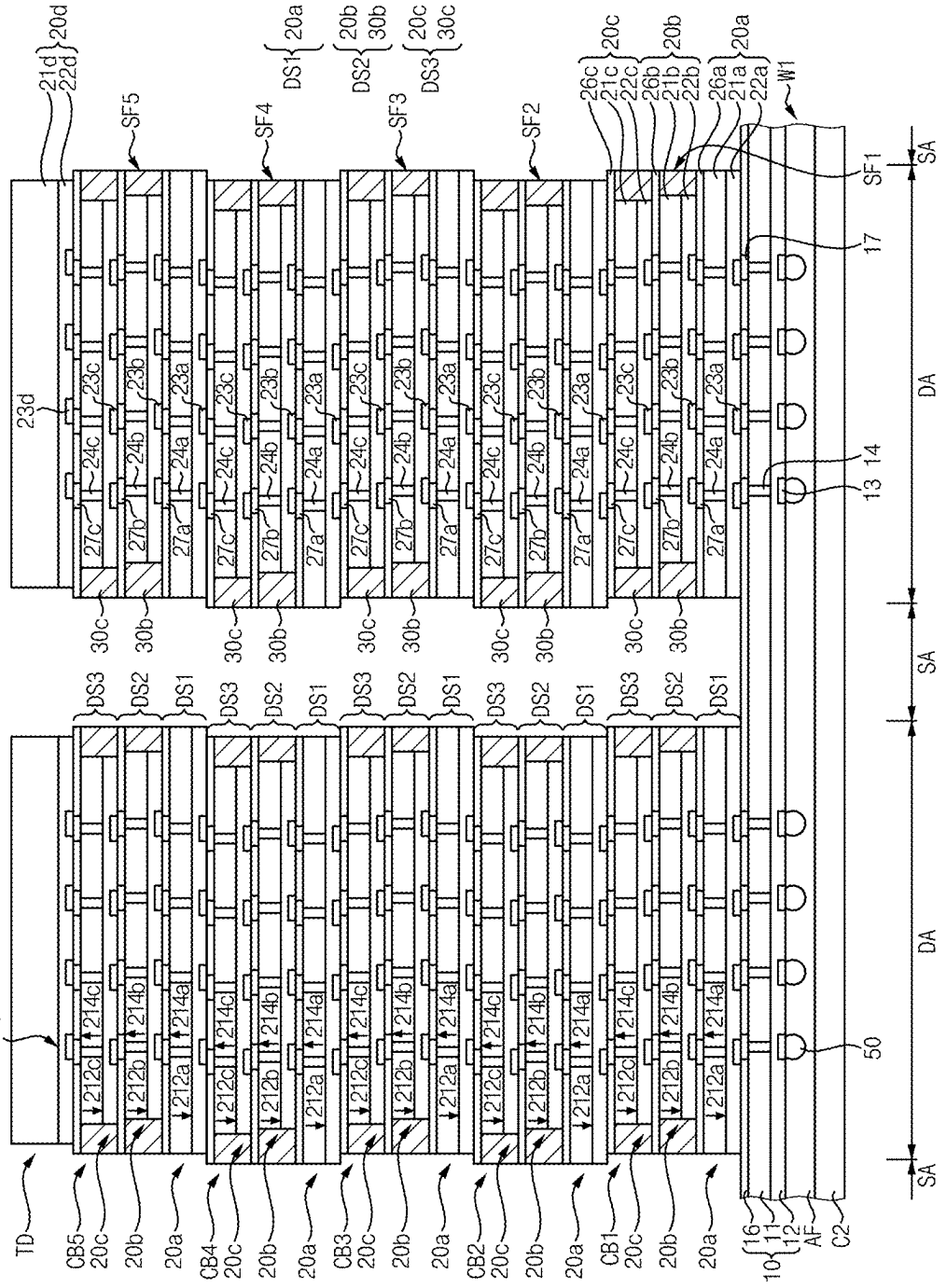

21d
22d
20d
SF5
SF4
DS1
20a
DS2
20b
30b
SF3
DS3
20c
30c
SF2
26c
21c
22c
26b
21b
22b
26a
21a
22a
W1
SF1
SA
17
DA
13 14
SA
DA
SA
50
23d
27c
24c
23c
27b
24b
23b
27a
24a
23a
30c
30b
DS3
DS2
DS1
212d
214c
214b
214a
212c
212b
212a
TD
CB5
CB4
CB3
CB2
CB1
20c
20b
20a
16
11
12
AF
C2
10

FIG. 23

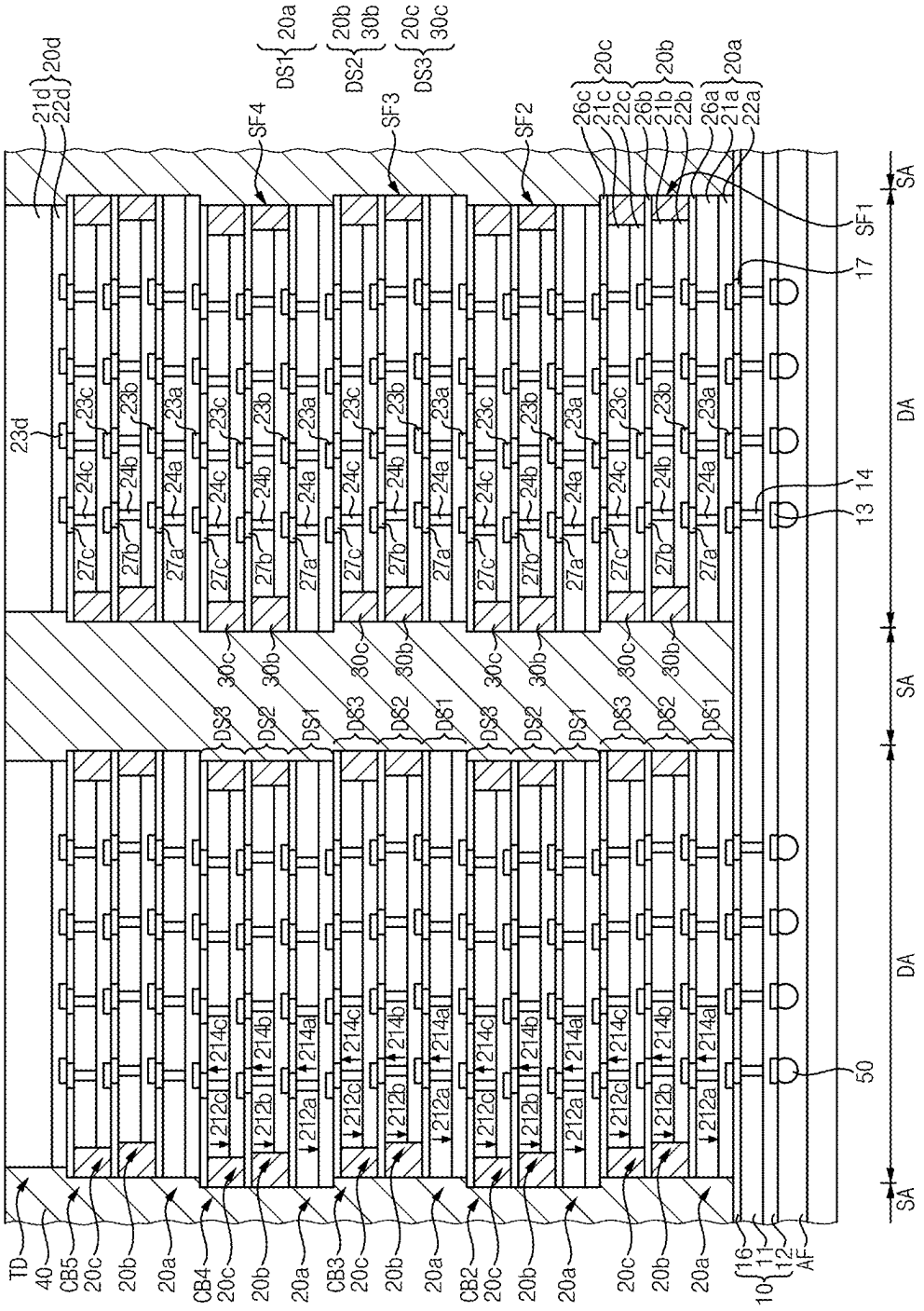

TD
40
CB5
20c
20b
20a
CB4
CB3
CB2
10
16
11
12
AF
50
13
14
17
SF1
SF2
SF3
SF4
DA
SA
DS1
DS2
DS3
21d
22d
20d
20a
20b
30b
20c
30c
26c
21c
22c
26b
21b
22b
26a
21a
22a
23d
23c
23b
23a
24c
24b
24a
27c
27b
27a
212c
212b
212a
214c
214b
214a

FIG. 24

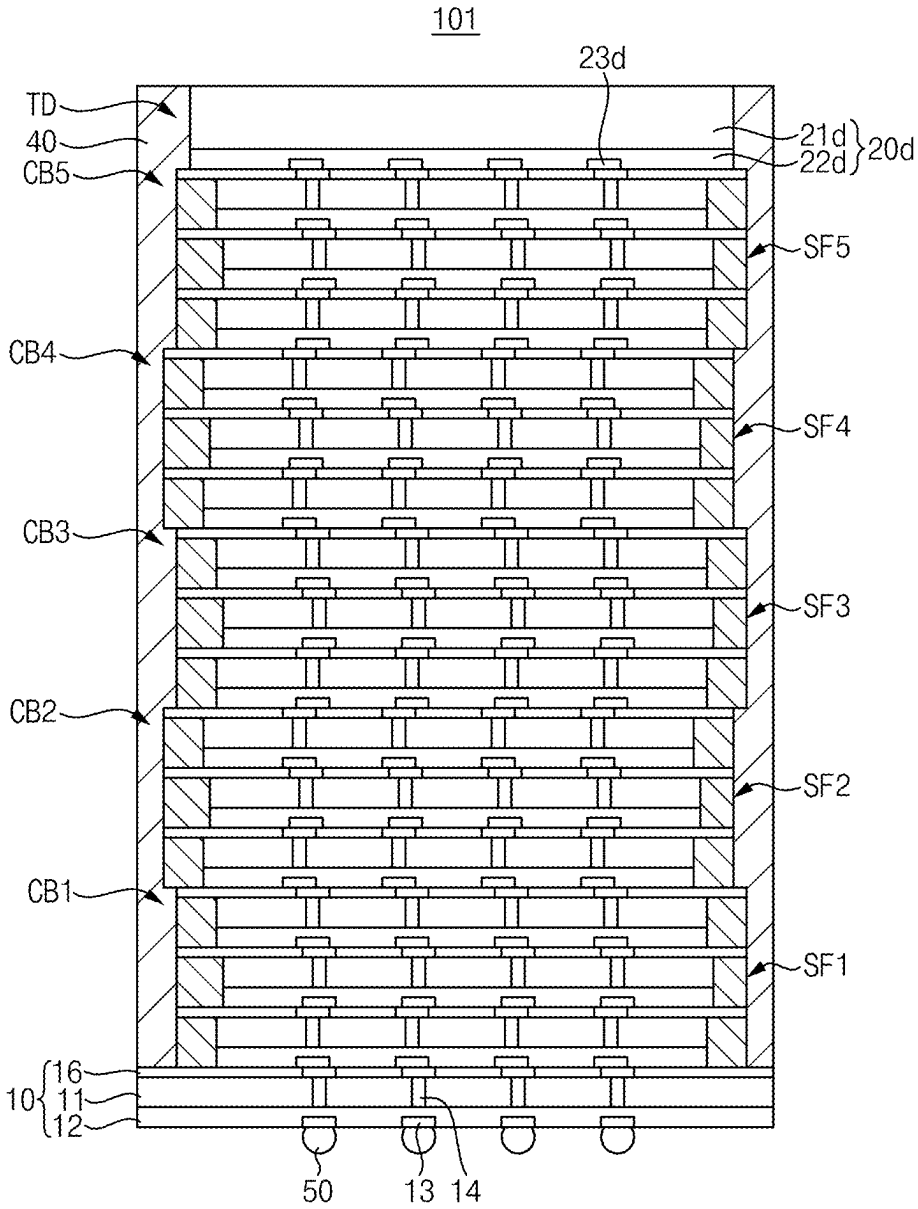

101
23d
TD
40
CB5
21d
22d
20d
SF5
CB4
SF4
CB3
SF3
CB2
SF2
CB1
SF1
16
10
11
12
50
13
14

FIG. 25

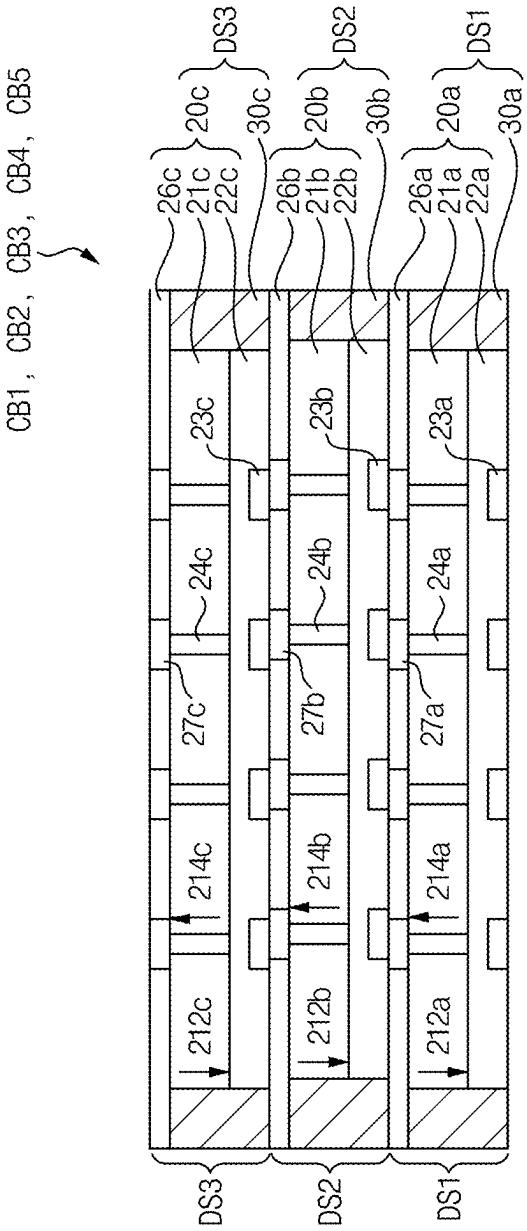

CB1, CB2, CB3, CB4, CB5
DS3
DS2
DS1
20c
20b
20a
30c
30b
30a
26c
21c
22c
26b
21b
22b
26a
21a
22a
23c
23b
23a
24c
24b
24a
27c
27b
27a
214c
214b
214a
212c
212b
212a

FIG. 26

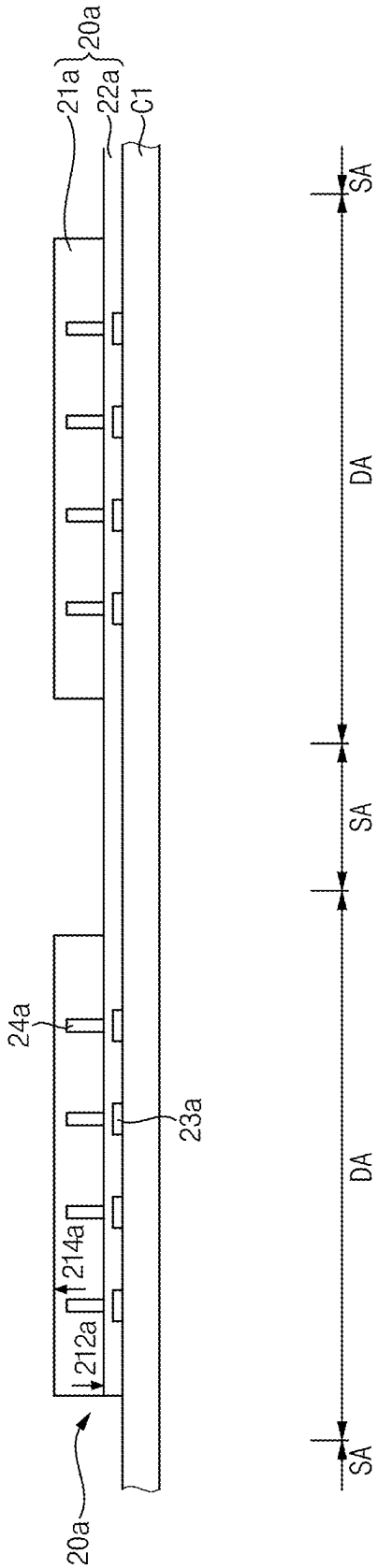


FIG. 27

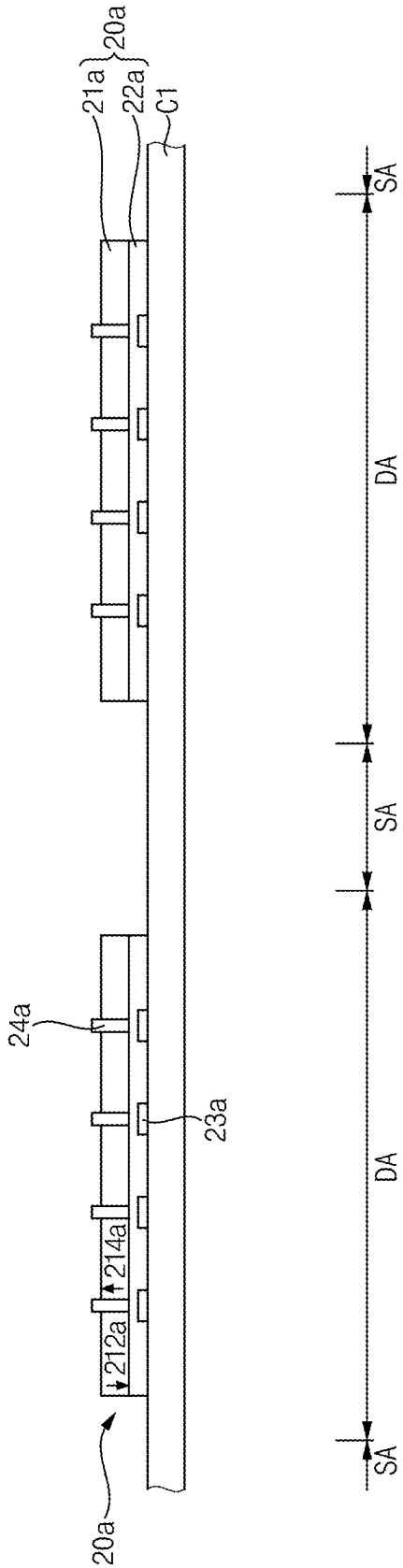


FIG. 28

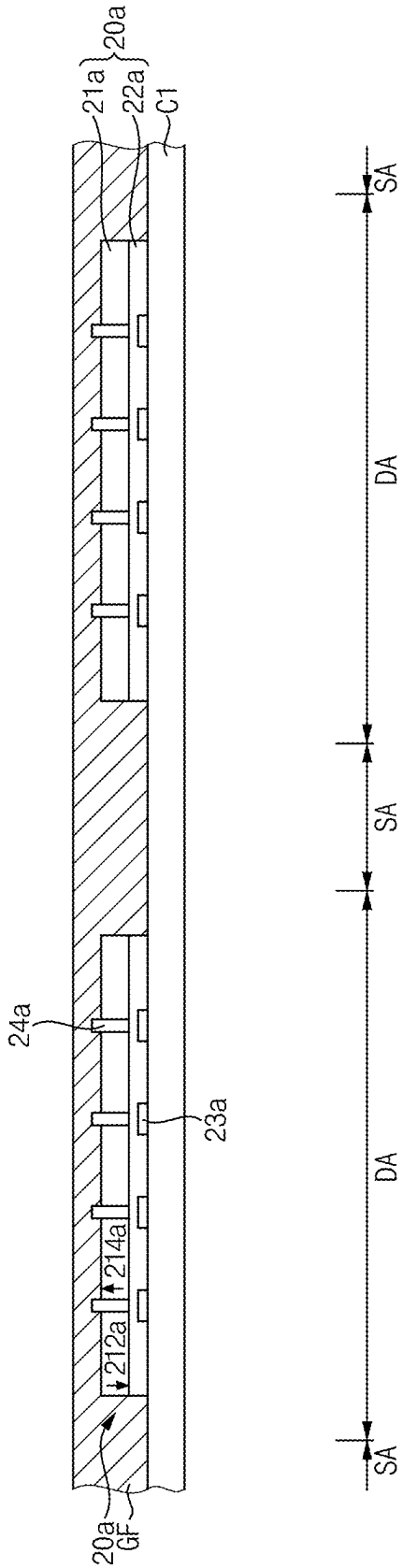


FIG. 29

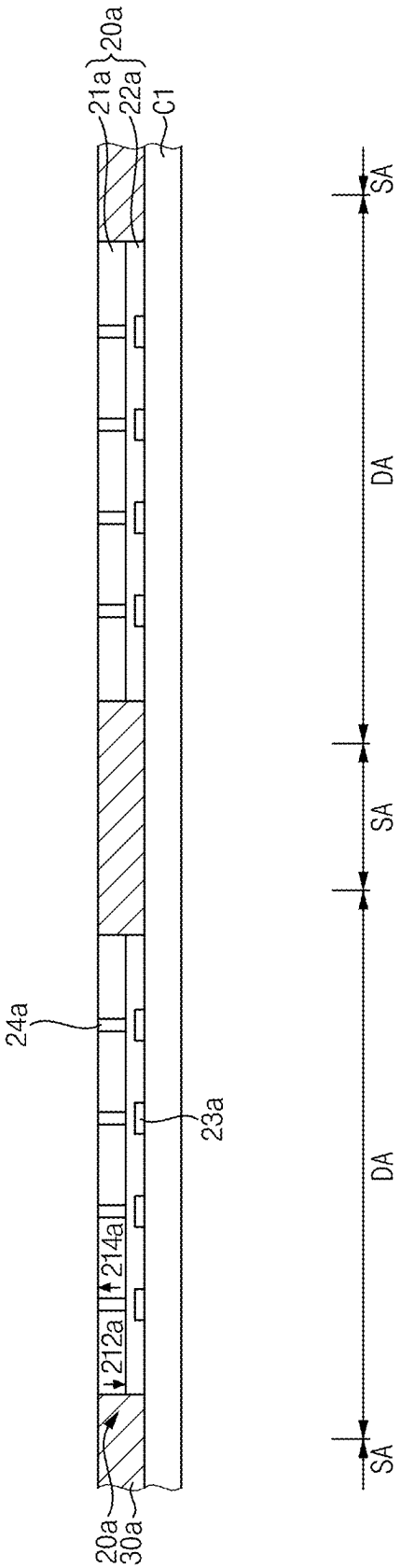


FIG. 30

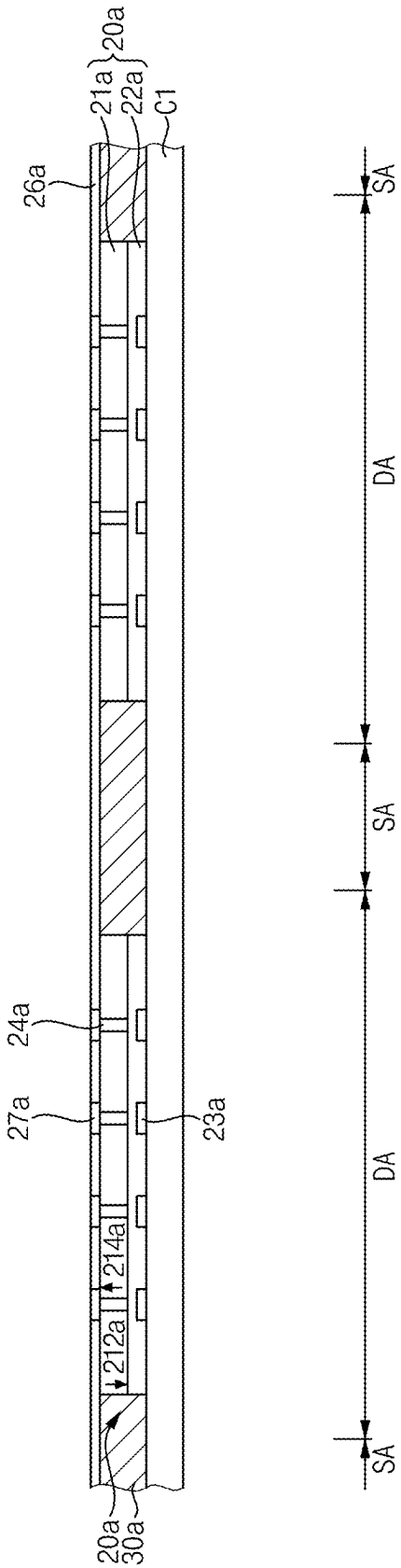


FIG. 31

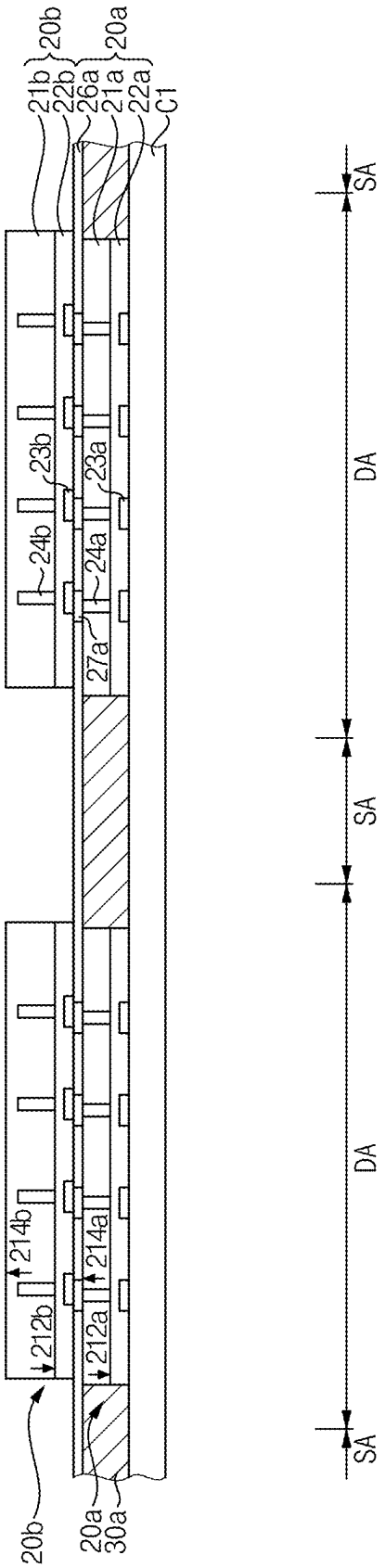

20b
20a
21b
22b
26a
21a
22a
C1
23b
23a
24b
24a
27a
214b
214a
212b
212a
20b
20a
30a
SA
DA
SA
DA
SA

FIG. 32

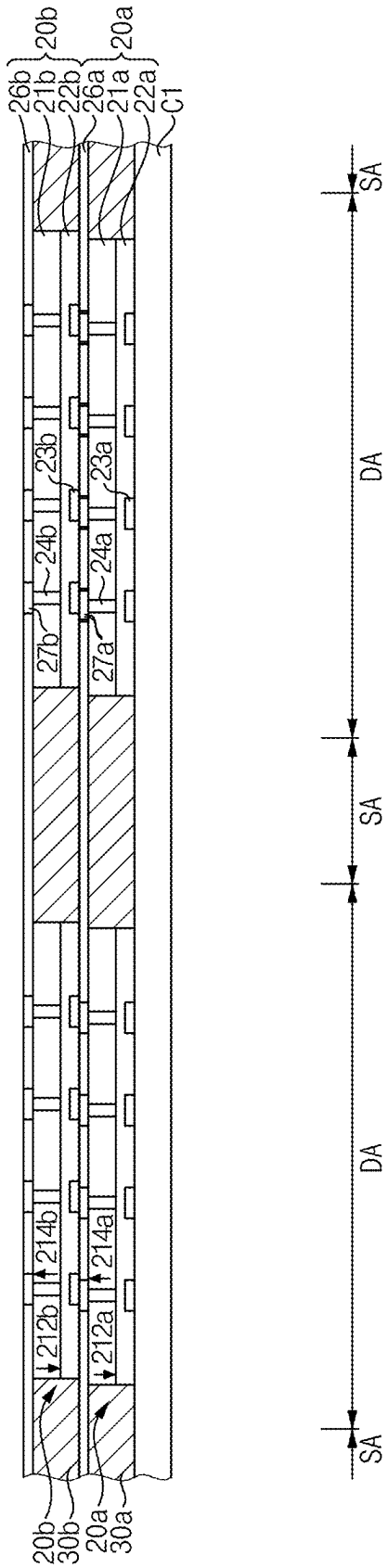

20b
20a
26b
21b
22b
26a
21a
22a
C1
23b
23a
24b
24a
27b
27a
214b
214a
212b
212a
20b
30b
20a
30a
SA
DA
SA
DA
SA

FIG. 33

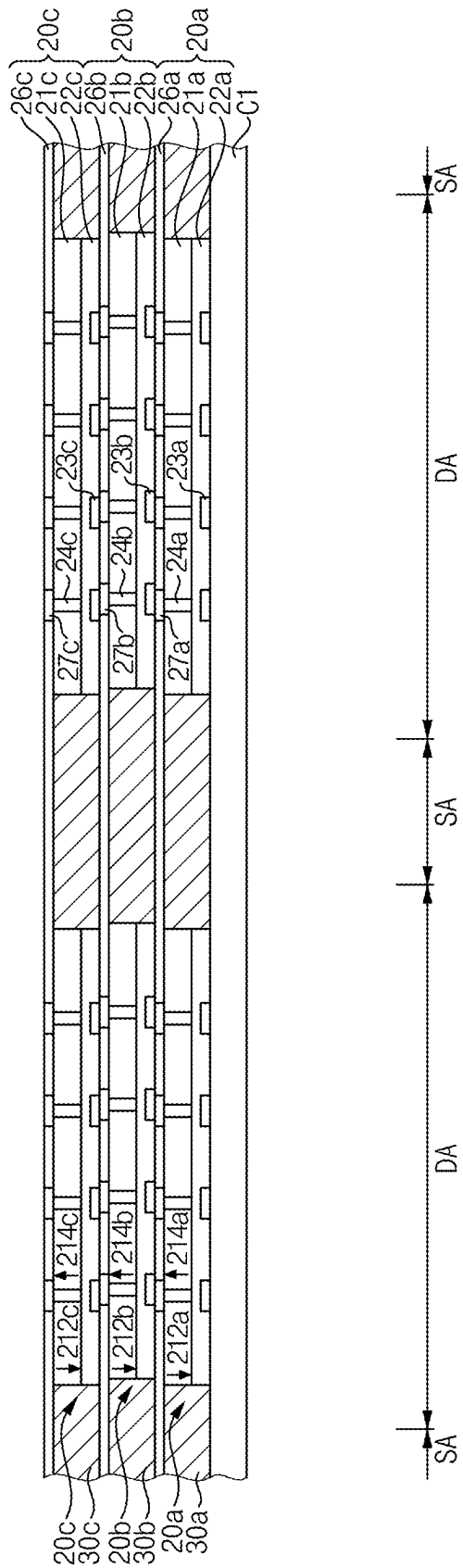
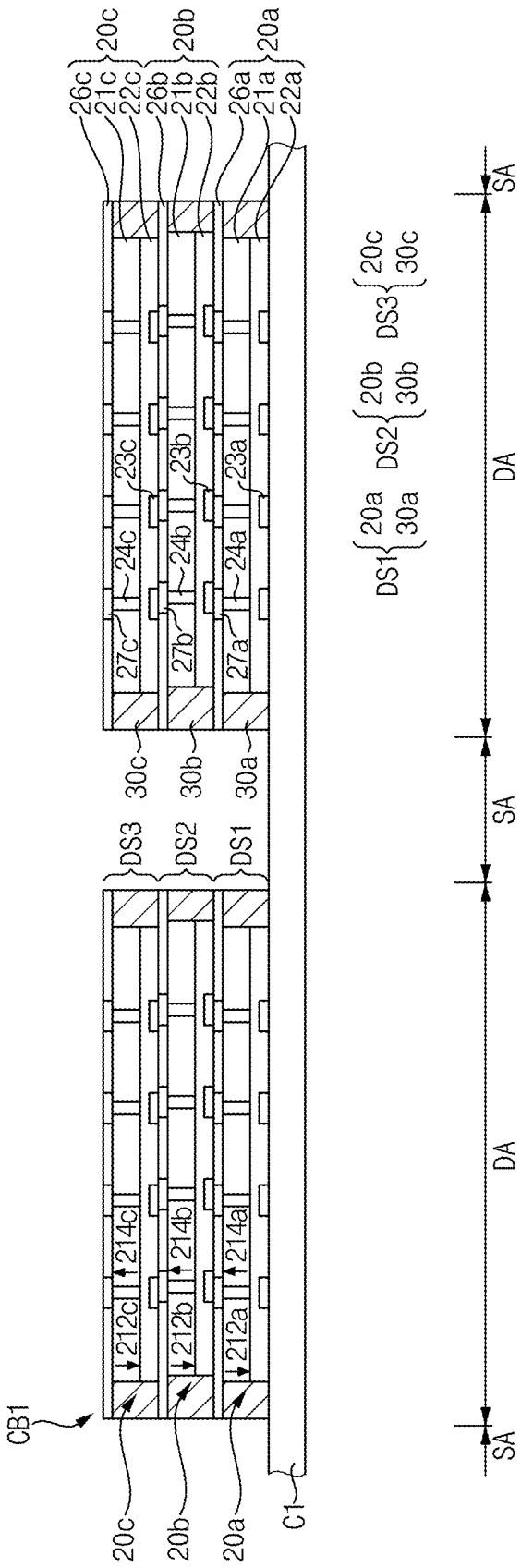

20c
20b
20a
26c
21c
22c
26b
21b
22b
26a
21a
22a
C1
23c
23b
23a
24c
24b
24a
27c
27b
27a
214c
214b
214a
212c
212b
212a
20c
30c
20b
30b
20a
30a
SA
DA
SA
DA
SA

FIG. 34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SEMICONDUCTOR PACKAGE AND METHOD OF MANUFACTURING THE SEMICONDUCTOR PACKAGE

PRIORITY STATEMENT

[0001] This application claims priority under 35 U.S.C. § 119 to Korean Patent Application No. 10-2024-0022230, filed on Feb. 16, 2024 in the Korean Intellectual Property Office (KIPO), the contents of which are herein incorporated by reference in their entirety.

FIELD

[0002] Example embodiments relate to a semiconductor package and a method of manufacturing the semiconductor package. More particularly, example embodiments relate to a semiconductor package including a plurality of sequentially stacked semiconductor chips and a method of manufacturing the same.

BACKGROUND

[0003] To manufacture a multi-chip package in which at least sixteen semiconductor chips are stacked, core dies may be attached to a buffer die on a carrier substrate by a die-to-wafer bonding method. In the die-to-wafer bonding method, as a thickness of the stacked core dies decreases, warpage increases and process difficulty increases, making it difficult to stack core dies with a thickness of about 30 μm or less at a high level (e.g., an ultra-high level). In addition, as the number of the stacked core dies increases, the interfacial bonding quality deteriorates and the yield decreases.

SUMMARY

[0004] Example embodiments provide a semiconductor package having improved bonding quality and including stacked dies at a high level (e.g., an ultra-high-level).

[0005] Example embodiments provide a method of manufacturing the semiconductor package.

[0006] According to example embodiments, a semiconductor package includes a buffer die, a plurality of core die blocks sequentially stacked on the buffer die, a top core die on an uppermost core die block of the plurality of core die blocks, and a molding member surrounding outer side surfaces of the plurality of core die blocks and the top core die on the buffer die. Each of the core die blocks includes a plurality of core dies sequentially stacked, and a plurality of gap filling portions surrounding outer side surfaces of at least two stages of core dies of the plurality of core dies. Outer side surfaces of the plurality of gap filling portions of each of the plurality of core die blocks are coplanar.

[0007] According to example embodiments, a semiconductor package includes a buffer die, a plurality of core die blocks sequentially stacked on the buffer die, each of the plurality of core die blocks including a plurality of die structures that are sequentially stacked, and a sealing member surrounding outer side surfaces of the plurality of core die blocks on the buffer die. Each of the plurality of die structures includes a substrate, a front insulating layer on a front surface of the substrate and including a first bonding pad therein, a backside insulating layer on a backside surface of the substrate and including a second bonding pad therein, and a gap filling portion surrounding outer side surfaces of the substrate and the front insulating layer.

[0008] According to example embodiments, a semiconductor package includes a buffer die, a plurality of core die blocks sequentially stacked on the buffer die, and a sealing member on outer side surfaces of the plurality of core die blocks on the buffer die. Each of the plurality of core die blocks includes a plurality of core dies sequentially stacked, and a plurality of gap filling portions on outer side surfaces of at least two stages of core dies of the plurality of core dies.

[0009] According to example embodiments, a semiconductor package may include a plurality of core die blocks sequentially stacked on a buffer die, and a molding member that is on, covers, or surrounds outer side surfaces of the plurality of core die blocks. Each of the core die blocks may include a plurality of core dies sequentially stacked, and a plurality of gap filling portions on, covering, or surrounding outer side surfaces of at least two stages of core dies of the plurality of core dies. Outer side surfaces of the plurality of gap filling portions of each of the plurality of core die blocks may be coplanar.

[0010] The semiconductor package may include the plurality of sequentially stacked core die blocks that are made of module blocks respectively. An ultra-high-end HBM may be implemented by forming the core die block having the core dies stacked using a die-to-wafer bonding method and sequentially stacking the core die blocks on the buffer die. Since the core die blocks are stacked in module units, it may be possible to stack the core dies having a thickness of about 30 μm or less at an extremely high level. Further, since the core dies and the core die blocks are each bonded by a hybrid bonding method, a total thickness may be reduced and heat dissipation characteristics may be improved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Example embodiments will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings. FIGS. **1** to **34** represent non-limiting, example embodiments as described herein.

[0012] FIG. **1** is a cross-sectional view illustrating a semiconductor package in accordance with example embodiments.

[0013] FIG. **2** is a cross-sectional view illustrating a core die block of the semiconductor package in FIG. **1**.

[0014] FIG. **3** is an enlarged cross-sectional view illustrating portion 'A' in FIG. **1**.

[0015] FIG. **4** is an enlarged cross-sectional view illustrating portion 'B' in FIG. **1**.

[0016] FIGS. **5** to **23** are views illustrating a method of manufacturing a semiconductor package in accordance with example embodiments.

[0017] FIG. **24** is a cross-sectional view illustrating a semiconductor package in accordance with example embodiments.

[0018] FIG. **25** is a cross-sectional view illustrating a core die block of the semiconductor package in FIG. **24**.

[0019] FIGS. **26** to **34** are views illustrating a method of manufacturing a semiconductor package in accordance with example embodiments.

DETAILED DESCRIPTION

[0020] Hereinafter, example embodiments will be explained in detail with reference to the accompanying drawings.

[0021] FIG. **1** is a cross-sectional view illustrating a semiconductor package in accordance with example embodiments. FIG. **2** is a cross-sectional view illustrating a core die block of the semiconductor package in FIG. **1**. FIG. **3** is an enlarged cross-sectional view illustrating portion 'A' in FIG. **1**. FIG. **4** is an enlarged cross-sectional view illustrating portion 'B' in FIG. **1**.

[0022] Referring to FIGS. **1** to **4**, a semiconductor package **100** may include semiconductor chips (dies) stacked therein. The semiconductor package **100** may include a buffer die **10** and a plurality of core die blocks CB**1**, CB**2**, CB**3**, CB**4**, CB**5** sequentially stacked on the buffer die **10**. Each of the core die blocks CB**1**, CB**2**, CB**3**, CB**4**, CB**5** may include a plurality of die structures DS**1**, DS**2**, DS**33** sequentially stacked. Each of the core die blocks CB**1**, CB**2**, CB**3**, CB**4**, CB**5** may include a plurality of core dies **20***a*, **20***b*, **20***c* sequentially stacked on one another and a plurality of gap filling portions **30***b*, **30***c* covering or surrounding outer side surfaces of at least two stages of core dies **20***b*, **20***c* of the plurality of core dies **20***a*, **20***b*, **20***c*, respectively. Additionally, the semiconductor package **100** may further include a top core die stack TD stacked on an uppermost core die block CB**5** among the plurality of core die blocks CB**1**, CB**2**, CB**3**, CB**4**, CB**5**, and a molding member or sealing member **40** that covers or surrounds outer side surfaces of the plurality of core die blocks CB**1**, CB**2**, CB**3**, CB**4**, CB**5**.

[0023] Each of the core die blocks may include a plurality of semiconductor chips (dies) **20***a*, **20***b*, **20***c* that are stacked vertically. In example embodiments, the semiconductor chips (dies) **20***a*, **20***b*, **20***c* may be substantially the same as or similar to each other. Accordingly, same or like reference numerals will be used to refer to the same or like elements and repeated descriptions of the same elements may be omitted in the interest of brevity.

[0024] The number of the core die blocks sequentially stacked on the buffer die **10** may be determined depending on the total number of the core dies stacked on the buffer die **10** and the number of the core dies in each core die block. One core die block may include at least two core dies stacked.

[0025] In example embodiments, the semiconductor package as a multi-chip package is as illustrated as including sixteen stacked semiconductor chips **20***a*, **20***b*, **20***c* on the buffer die **10**, however, it may not limited thereto. For example, the semiconductor package may include 20 or 24 stacked semiconductor chips.

[0026] Each of the semiconductor chips **20***a*, **20***b*, **20***c* may include an integrated circuit chip completed by performing semiconductor manufacturing processes. Each semiconductor chip may include, for example, a memory chip or a logic chip. The semiconductor package **100** may include a memory device. The memory device may include a high bandwidth memory (HBM) device.

[0027] As illustrated in FIG. **2**, each of first, second, third, fourth and fifth core die blocks CB**1**, CB**2**, CB**3**, CB**4** and CB**5** may include first, second and third die structures DS**1**, DS**2** and DS**3** sequentially stacked. The first die structure DS**1** may include a first core die **20***a*. The second die structure DS**2** may include a second core die **20***b* and a gap filling portion or member **30***b* that covers or surrounds an outer side surface of the second core die **20***b*. The third die structure DS**3** may include a third core die **20***c* and a gap filling portion or member **30***b* that covers or surrounds an outer side surface of the third core die **20***c*. Each of the core die blocks may include the first, second and third core dies **20***a*, **20***b*, and **20***c* sequentially stacked, and the gap filling portions **30***b*, and **30***c* respectively covering or surrounding the outer side surfaces of the second, and third core dies **20***b*, and **20***c* stacked in at least two stages. In example embodiments, one core die block CB**1**, CB**2**, CB**3** may include the core dies **20***a*, **20***b*, and **20***c* stacked in three stages, but it will be understood that the present inventive concept is not limited thereto.

[0028] The first, second, third, fourth and fifth core die blocks CB**1**, CB**2**, CB**3**, CB**4** and CB**5** may be substantially identical to each other. Each of the first, second, third, fourth and fifth core die blocks CB**1**, CB**2**, CB**3**, CB**4** and CB**5** may have a rectangular parallelepiped shape. A lower surface of the first die structure DS**1** may serve as a lower surface of each core die block, and an upper surface of the third die structure DS**3** may serve as an upper surface of each core die block.

[0029] In example embodiments, the first, second, third, fourth and fifth core die blocks CB**1**, CB**2**, CB**3**, CB**4** and CB**5** may be sequentially stacked on the buffer die **10**. The first core die blocks CB**1** may be bonded to a wafer including the buffer die **10** by hybrid bonding. The second core die block CB**2** may be bonded to the first core die block CB**1**. Accordingly, misalignment may occur between the first core die block CB**1** and the second core die block CB**2**, and an outer side surface SF**1** of the first core die block CB**1** and an outer side surface SF**2** of the second core die block CB**2** may be positioned on different planes, respectively. Similarly, the third core die block CB**3** may be bonded to the second core die block CB**2**. Accordingly, misalignment may occur between the second core die block CB**2** and the third core die block CB**3**, and the outer side surface SF**2** of the second core die block CB**2** and an outer side surface SF**3** of the third core die block CB**3** may be positioned on different planes, respectively. Similarly, the fourth core die block CB**4** may be bonded to the third core die block CB**3**. Accordingly, misalignment may occur between the third core die block CB**3** and the fourth core die block CB**4**, and the outer side surface SF**3** of the third core die block CB**3** and an outer side surface SF**4** of the fourth core die block CB**4** may be positioned on different planes, respectively. Similarly, the fifth core die block CB**5** may be bonded to the fourth core die block CB**4**. Accordingly, misalignment may occur between the fourth core die block CB**4** and the fifth core die block CB**5**, and the outer side surface SF**4** of the fourth core die block CB**4** and an outer side surface SF**5** of the fifth core die block CB**5** may be positioned on different planes, respectively. A (horizontal) width of the buffer die **10** may be greater than a width of each of the first, second, third, fourth and fifth core die blocks CB**1**, CB**2**, CB**3**, CB**4** and CB**5**.

[0030] Each core die block may have a thickness T**1** of at least 40 μm. Each of the first to third core dies **20***a*, **20***b*, and **20***c* may have a thickness within a range of about 10 μm to 30 μm. The first core die **20***a* may have a first planar area, and the second and third core dies **20***b* and **20***c* may have a second planar area that is less than the first planar area. The first core die **20***a* may have a first (horizontal) width, and the second and third core dies **20***b* and **20***c* may have a second (horizontal) width less than the first width.

[0031] In example embodiments, the buffer die **10** may include a substrate **11**, a front insulating layer **12**, a plurality of first bonding pads **13**, a plurality of through electrodes **14**, a backside insulating layer **16**, and a plurality of second

bonding pads **17**. Additionally, the buffer die **10** may further include conductive bumps **50** as conductive connection members respectively provided on the first bonding pads **13**. The buffer die **10** may be mounted on a package substrate or an interposer via the conductive bumps **50**. For example, the conductive bump **50** may include a solder bump. Alternatively, the conductive bump **50** may include a pillar bump and a solder bump formed on the pillar bump.

[0032] The substrate **11** may have a first surface **112** and a second surface **114** opposite to the first surface **112**. The first surface **112** may be an active surface, and the second surface **114** may be a non-active surface. Circuit patterns may be provided on the first surface **112** of the substrate **11**. The first surface **112** may be referred to as a front surface on which the circuit patterns are formed, and the second surface may be referred to as a backside surface.

[0033] For example, the substrate **11** may be a single crystal silicon substrate. The circuit patterns may include transistors, capacitors, diodes, etc. The circuit patterns may constitute circuit elements. Accordingly, the buffer die **10** may be a semiconductor device having a plurality of circuit elements formed therein.

[0034] As illustrated in FIG. **3**, the front insulating layer **12** as an insulation interlayer may be formed on the first surface **112** of the substrate **11**, that is, the front surface. The front insulating layer **12** may include a plurality of insulating layers **122** and **124** and wirings **123** in the insulating layers. Additionally, the first bonding pad **13** may be provided in an outermost or lowermost insulating layer of the front insulating layer **12**.

[0035] For example, the front insulating layer **12** may include a metal wiring layer **122** and a first passivation layer **124**. The metal wiring layer **122** may include a plurality of wirings **123** therein. For example, the metal wiring layer **122** may include a metal wiring structure including a plurality of wirings **123** vertically stacked in buffer layers and insulating layers. The first bonding pad **13** may be formed on a lowermost wiring among the plurality of wirings **123**. For example, the wirings may include aluminum (Al), copper (Cu), tin (Sn), nickel (Ni), gold (Au), platinum (Pt), or an alloy thereof.

[0036] The first passivation layer **124** may be formed on the metal wiring layer **122** and may expose at least a portion of the first bonding pad **13**. The first passivation layer **124** may include a plurality of stacked insulating layers. For example, the first passivation layer **124** may include a first protective layer including an oxide layer and a second protective layer including a nitride layer, sequentially stacked. The first protective layer may include silicon oxide, and the second protective layer may include silicon nitride or silicon carbonitride.

[0037] The first bonding pad **13** may be provided in the first passivation layer **124**. The first bonding pad **13** may be exposed through an outer surface of the first passivation layer **124**. An upper surface of the first bonding pad **13** may be coplanar with an upper surface of the first passivation layer **124** and/or a lower surface of the first bonding pad **13** may be coplanar with a lower surface of the first passivation layer **124**. Although not illustrated in the figures, an insulation interlayer may be provided on the first surface **112** of the substrate **11** to cover the circuit patterns. The insulation interlayer may be formed to include, for example, silicon oxide or a low dielectric material. The insulation interlayer may include lower wiring therein, which are electrically connected to the circuit patterns. Accordingly, the circuit pattern may be electrically connected to the first bonding pad **13** by the lower wirings and the wirings.

[0038] The through electrode (e.g., through silicon via, TSV) **14** may vertically penetrate the insulation interlayer and may extend from the first surface **112** to the second surface **114** of the substrate **11**. The through electrode **14** may contact an uppermost wiring of the metal wiring structure. Accordingly, the through electrode **24** may be electrically connected to the first bonding pad **13** by the wirings **123**.

[0039] The backside insulating layer **16** may be formed on the second surface **114** of the substrate **11**, that is, the backside surface. The second bonding pad **17** may be provided in the backside insulating layer **16**. For example, the second bonding pad **17** may be disposed on an exposed surface of the through electrode **14**. An upper surface of the second bonding pad **17** may be coplanar with an upper surface of the backside insulating layer **16** and/or a lower surface of the second bonding pad **17** may be coplanar with a lower surface of the backside insulating layer **16**. The backside insulating layer **16** may include silicon oxide, carbon-doped silicon oxide, silicon carbonitride (SiCN), etc. Accordingly, the first and second bonding pads **13** and **17** may be electrically connected to each other by the through electrode **24**

[0040] As illustrated in FIGS. **3** and **4**, the first core die **20***a* of the first die structure CD**1** of the first core die block CB**1** may include a substrate **21***a*, a front insulating layer **22***a*, a plurality of first bonding pads **23***a*, a plurality of through electrodes **24***a*, a backside insulating layer **26***a* and a plurality of second bonding pads **27***a*.

[0041] The substrate **21***a* may have a first surface **212***a* and a second surface **214***a* opposite to the first surface **212***a*. The first surface **212***a* may be an active surface, and the second surface **214***a* may be a non-active side. Circuit patterns may be provided on the first surface **212***a* of the substrate **21***a*. The front insulating layer **22***a* as an insulation interlayer may be formed on the first surface **212***a* of the substrate **21***a*, that is, a front surface. The front insulating layer **22***a* may include a plurality of insulating layers **222***a* and **224***a* and wirings **223***a* in the insulating layers **222***a* and **224***a*. Additionally, the first bonding pad **23***a* may be provided in an outermost or lowermost insulating layer of the front insulating layer **22***a*. For example, the front insulating layer **22***a* may include a metal wiring layer **222***a* and a first passivation layer **224***a*. The metal wiring layer **222***a* may include a plurality of wirings **223***a* therein.

[0042] The through electrode **24***a* may extend vertically from the first surface **212***a* to the second surface **214***a* of the substrate **21***a*. The through electrode **24***a* may be electrically connected to the first bonding pad **23***a* by the wirings **223***a*. The backside insulating layer **26***a* may be formed on the second surface **214***a* of the substrate **21***a*, that is, a backside surface. The second bonding pad **27***a* may be provided in the backside insulating layer **26***a*. Accordingly, the first and second bonding pads **23***a* and **27***a* may be electrically connected to each other by the through electrode **24***a*.

[0043] Similarly, the second core die **20***b* of the second die structure CD**2** may include a substrate **21***b*, a front insulating layer **22***b*, a plurality of first bonding pads **23***b*, a plurality of through electrodes **24***b*, a backside insulating layer **26***b*, and a plurality of second bonding pads **27***b*. Since the core dies **20***a*, **20***b* and **20***c* are substantially the same as or similar to

each other, same or like reference numerals will be used to refer to the same or like elements and repeated descriptions of the same elements may be omitted in the interest of brevity.

[0044] The backside insulating layer **26***b* of the second die structure DS**2** may protrude or extend inwardly in a horizontal direction from the outer side surfaces of the substrate **21***b* and the front insulating layer **22***b*. The substrate **21***b* and the front insulating layer **22***b* may have a length in a first direction, that is, a first width L**1**, and the backside insulating layer **26***b* may has a second width L**2** greater than the first width L**1**. The substrate **21***a* may have the second width L**2**.

[0045] As illustrated in FIG. **3**, the first core die **20***a* of the first core die block CB**1** and the buffer die **10** may be bonded to each other by hybrid bonding. The second bonding pad **17** of the buffer die **10** and the first bonding pad **23***a* of the first core die **20***a* may be bonded to each other by copper-copper hybrid bonding (Cu—Cu Hybrid Bonding). A front surface of the first core die **20***a*, that is, the front side insulating layer **22***a* on the first surface **212***a* of the substrate **21***a* may be directly bonded to the backside insulating layer **16** of the substrate **11** of the buffer die **10**.

[0046] As illustrated in FIG. **4**, the second core die **20***b* and the first core die **20***a* may be bonded to each other by hybrid bonding. The second bonding pad **27***a* of the first core die **20***a* and the first bonding pad **23***b* of the second core die **20***b* may be bonded to each other by copper-copper hybrid bonding (Cu—Cu Hybrid Bonding).

[0047] The front insulating layer **22***b* on a front surface of the second core die **20***b* may be directly bonded to the backside insulating layer **26***a* on a backside surface of the first core die **20***a*. The outermost insulating layers of the backside insulating layer **26***a* and the front insulating layer **22***b* may include an insulating material that contacts each other and provides excellent bonding strength, thereby providing a bonding structure. The backside insulating layer **26***a* and the front insulating layer **22***b* may be bonded to each other by a high temperature annealing process while in contact with each other. Here, the bonding structure may have a relatively stronger bonding strength by covalent bonding.

[0048] Similarly, the third core die **20***c* and the second core die **20***b* may be bonded to each other by hybrid bonding.

[0049] The gap filling portion **30***b* of the second die structure DS**2** may at least partially cover or surround the outer side surface of the second core die **20***b*. The gap filling portion **30***b* may cover or surround outer side surfaces of the substrate **21***b* and the front insulating layer **22***b* of the second core die **20***b*. The backside insulating layer **26***b* of the second core die **20***b* may cover an upper surface of the gap filling portion **30***b*. The backside insulating layer **26***b* may protrude or extend inwardly in a horizontal direction from the outer side surfaces of the substrate **21***b* and the front insulating layer **22***b*, and the protruding portion of the backside insulating layer **26***b* may cover the upper surface of the gap filling portion **30***b*. An outer side surface of the backside insulating layer **26***b* and an outer side surface of the gap filling portion **30***b* may be coplanar or positioned on the same plane.

[0050] For example, the gap filling portion **30***b* may be formed by a conformal deposition process such as an atomic layer deposition (ALD) process or a chemical vapor deposition (CVD) process. The gap filling portion may include an inorganic dielectric layer or an organic dielectric layer. The inorganic dielectric layer may include silicon oxide, silicon oxynitride, phosphosilicate glass (PSG), boro-phosphosilicate glass (BPSG), etc. The organic dielectric layer may include a polymer or the like.

[0051] Alternatively, the gap filling portion **30***b* of the second die structure DS**2** may cover or surround the entire outer side surface of the second core die **20***b*. The gap filling portion **30***b* of the second die structure DS**2** may cover the outer side surfaces of the substrate **21***b*, the front insulating layer **22***b*, and the backside insulating layer **26***b* of the second core die **20***b*. In this case, the backside insulating layer **26***b* may not protrude in the horizontal direction from the outer side surfaces of the substrate **21***b* and the front insulating layer **22***b*, and the outer side surface of the backside insulating layer **26***b* and the outer side surfaces of the substrate **21***b* and the front insulating layer **22***b* may be coplanar or positioned on the same plane.

[0052] Similarly, the gap filling portion **30***c* of the third die structure DS**3** may at least partially cover or surround the outer side surface of the third core die **20***c*. The gap filling portion **30***c* may cover or surround outer side surfaces of a substrate **21***c* and a front insulating layer **22***c* of the third core die **20***c*. A backside insulating layer **26***c* of the third core die **20***c* may cover an upper surface of the gap filling portion **30***c*. The backside insulating layer **26***c* may protrude or extend inwardly in a horizontal direction from the outer side surfaces of the substrate **21***c* and the front insulating layer **22***c*, and the protruding portion of the backside insulating layer **26***c* may cover the upper surface of the gap filling portion **30***c*. An outer side surface of the backside insulating layer **26***c* and the outer side surface of the gap filling portion **30***c* may be coplanar or positioned on the same plane.

[0053] The backside insulating layer **26***a* of the first die structure DS**1** may cover or be on a lower surface of the gap filling portion **30***b* of the second die structure DS**2**. The backside insulating layer **26***b* of the second die structure DS**2** may cover or be on a lower surface of the gap filling portion **30***c* of the third die structure RD**3**. Additionally, the outer side surfaces of the gap filling portions **30***b*, **30***c* of the first core die block CB**1** may be coplanar or positioned on the same plane.

[0054] In example embodiments, the top core die stack TD may include a top core die **20***d*. The top core die **20***d* and the fifth core die block CB**5** may be bonded to each other by hybrid bonding. A front surface of the top core die **20***d*, that is, a front side insulating layer **22***d* on a first surface **212***d* of a substrate **21***d* may be directly bonded to a backside insulating layer **26***c* of a third core die **20***c* of the fifth core die block.

[0055] A second bonding pad **27***c* of the third core die **20***c* of the fifth core die block and a first bonding pad **23***d* of the top core die **20***d* may make contact with each other. When the fifth core die block and the top core die **20***d* are bonded to each other by die-to-wafer bonding, the second bonding pad **27***c* of the third core die **20***c* of the fifth core die block and the first bonding pads **23***d* of the top core die **20***d* may be bonded to each other by copper-copper hybrid bonding (Cu—Cu Hybrid Bonding).

[0056] A thickness of the top core die **20***d* may be greater than thicknesses of the middle core dies **20***a*, **20***b*, and **20***c*. The thickness of the top core die **20***d* may be within a range of 50 μm to 300 μm.

[0057] In example embodiments, the molding member **40** (also referred to herein as the sealing member **40**) may be provided to cover or surround outer side surfaces of the first, second, third, fourth and fifth core die blocks CB**1**, CB**2**, CB**3**, CB**4** and CB**5** and the top core die **20***d*. The molding member **40** may cover or surround outer side surfaces of the first to third die structures DS**1**, DS**2** and DS**3** of each of the first, second, third, fourth and fifth core die blocks CB**1**, CB**2**, CB**3**, CB**4** and CB**5**. The molding member **40** may directly contact the gap filling portions **30***b*, **30***c* of the second and third die structures DS**2** and DS**3**.

[0058] For example, the molding member **40** may include a molding material such as a thermosetting resin. The molding material may include an epoxy mold compound (EMC). The molding material may include UV resin, polyurethane resin, silicone resin, silica filler, etc.

[0059] As mentioned above, the semiconductor package **100** may include the first, second, third, fourth and fifth core die blocks CB**1**, CB**2**, CB**3**, CB**4** and CB**5** sequentially stacked on the buffer die **10**, and the molding member **40** that covers or surrounds the outer side surfaces of the first, second, third, fourth and fifth core die blocks CB**1**, CB**2**, CB**3**, CB**4** and CB**5**. Each of the first, second, third, fourth and fifth core die blocks CB**1**, CB**2**, CB**3**, CB**4** and CB**3** may include the first, second and third die structures DS**1**, DS**2** and DS**3** sequentially stacked. The first die structure DS**1** may include the first core die **20***a*. The second die structure DS**2** may include the second core die **20***b* and the gap filling portion **30***b* covering or surrounding the outer side surface of the second core die **20***b*. The third die structure DS**3** may include the third core die **20***c* and the gap filling portion **30***c* covering or surrounding the outer side surface of the third core die **20***c*.

[0060] The semiconductor package **100** may include a plurality of the sequentially stacked first, second, third, fourth and fifth core die blocks CB**1**, CB**2**, CB**3**, CB**4** and CB**5** that are made of module blocks respectively. An ultra-high-end HBM may be implemented by forming the core die blocks each having the core dies stacked using a die-to-wafer bonding method and sequentially stacking the core die blocks on the buffer die **10**. Since the core die blocks are stacked in module units, it may be possible to stack the core dies having a thickness of about 30 μm or less at an extremely high level. Further, since the core dies and the core die blocks are each bonded by a hybrid bonding method, a total thickness may be reduced and heat dissipation characteristics may be improved.

[0061] Hereinafter, a method of manufacturing the semiconductor package of FIG. **1** will be described. A case where the semiconductor package includes a high bandwidth memory (HBM) device will be described. However, it will be understood that a method of manufacturing a semiconductor package in accordance with example embodiments is not limited thereto.

[0062] FIGS. **5** to **23** are views illustrating a method of manufacturing a semiconductor package in accordance with example embodiments. FIG. **6** is an enlarged cross-sectional view illustrating portion 'C' in FIG. **5**. FIG. **9** is an enlarged cross-sectional view illustrating portion 'D' in FIG. **8**. FIG. **11** is an enlarged cross-sectional view illustrating portion 'E' in FIG. **10**. FIG. **19** is an enlarged cross-sectional view illustrating portion 'F' in FIG. **18**.

[0063] Referring to FIGS. **5** to **12**, first, first die structures may be formed on a first carrier substrate C**1**.

[0064] As illustrated in FIGS. **5** and **6**, a plurality of first semiconductor chips (first core dies) **20***a* diced from a wafer may be placed on the first carrier substrate C**1**.

[0065] In example embodiments, the first carrier substrate C**1** may include a wafer substrate as a base substrate on which a plurality of die structures are stacked at a wafer level. The first carrier substrate C**1** may have a shape corresponding to a wafer on which the semiconductor process is performed. For example, the first carrier substrate may include a silicon substrate, a glass substrate, a non-metallic or metallic plate, etc.

[0066] The first carrier substrate C**1** may include a die region DA where the die structure is disposed and a cutting region SA surrounding the die region DA. As will be described below, a gap filling layer covering or surrounding the core dies on the first carrier substrate C**1** may be cut along the cutting region SA by a first sawing process to be individualized.

[0067] As illustrated in FIG. **5**, the second wafer W**2** may include a substrate **21***a* and a front insulating layer **22***a* having first bonding pads **23***a* that are provided in an outer surface thereof. Additionally, the second wafer W**2** may include a plurality of through electrodes **24***a* that are provided in the substrate **21***a* and are electrically connected to the first bonding pads **23***a*.

[0068] The substrate **21***a* may have a first surface **212***a* and a second surface **214***a* opposite to each other. Circuit patterns may be provided on the first surface **212***a* of the substrate **21***a*. For example, the substrate **21***a* may include silicon, germanium, silicon-germanium, or III-V compounds, e.g., GaP, GaAs, GaSb, etc. In some embodiments, the substrate **21***a* may be a silicon-on-insulator (SOI) substrate, or a germanium-on-insulator (GOI) substrate.

[0069] The circuit patterns may include transistors, capacitors, diodes, etc. The circuit patterns may constitute circuit elements. Accordingly, the semiconductor chip may be a semiconductor device with a plurality of the circuit elements formed therein. The circuit patterns may be formed on the first surface **212***a* of the substrate **21***a* by performing a FEOL (Front End of Line) process for manufacturing semiconductor devices. The surface of the substrate on which the FEOL process is performed may be referred to as a front surface of the substrate, and a surface opposite to the front surface may be referred to as a backside surface.

[0070] The circuit element may include a plurality of memory devices. Examples of the memory devices include a volatile semiconductor memory device and a non-volatile semiconductor memory device. Examples of the volatile semiconductor memory device may be DRAM, SRAM, etc. Examples of the non-volatile semiconductor memory devices may be EPROM, EEPROM, Flash EEPROM, etc.

[0071] As illustrated in FIG. **6**, the front insulating layer **22***a* may be formed as an insulation interlayer on the first surface **212***a* of the substrate **21***a*, that is, the front surface. The front insulating layer **22***a* may include a plurality of insulating layers **222***a* and **224***a* and wirings **223***a* in the insulating layers. Additionally, the first bonding pad **23***a* may be provided in an outermost or lowermost insulating layer of the front insulating layer **22***a*.

[0072] For example, the front insulating layer **22***a* may include a metal wiring layer **222***a* and a first passivation layer **224***a*. The metal wiring layer **222***a* may include the plurality of wirings **223***a* therein. For example, the metal wiring layer **222***a* may include a metal wiring structure

including the plurality of wirings **223***a* vertically stacked in buffer layers and insulating layers. The first bonding pad **23***a* may be formed on a lowermost wiring among the plurality of wirings **223***a*. For example, the wirings may include aluminum (Al), copper (Cu), tin (Sn), nickel (Ni), gold (Au), platinum (Pt), or alloys thereof.

[0073] The first passivation layer **224***a* may be formed on the metal wiring layer **222***a* and may expose at least a portion of the first bonding pad **23***a*. The first passivation layer **224***a* may include a plurality of stacked insulating layers. For example, the first passivation layer **224***a* may include a first protective layer including an oxide layer and a second protective layer including a nitride layer, sequentially stacked. The first protective layer may include silicon oxide, and the second protective layer may include silicon nitride or silicon carbonitride.

[0074] The first bonding pad **23***a* may be provided in the first passivation layer **224***a*. The first bonding pad **23***a* may be exposed through a side surface of the first passivation layer **224***a*. An upper surface of the first bonding pad **23***a* may be coplanar with an upper surface of the first passivation layer **224***a* and/or a lower surface of the first bonding pad **23***a* may be coplanar with a lower surface of the first passivation layer **224***a*. Although not illustrated in the figures, an insulation interlayer may be provided on the first surface **212***a* of the substrate **21***a* to cover the circuit patterns. The insulation interlayer may be formed to include, for example, silicon oxide or a low dielectric material. The insulation interlayer may include lower wiring therein, which are electrically connected to the circuit patterns. Accordingly, the circuit pattern may be electrically connected to the first bonding pad **23***a* by the lower wirings and the wirings.

[0075] The through electrode (e.g., through silicon via, TSV) **24***a* may vertically penetrate or extend through the insulation interlayer and extend from the first surface **212***a* of the substrate **21***a* to a predetermined depth. The through electrode **24***a* may contact an uppermost wiring of the metal wiring structure. Accordingly, the through electrode **24***a* may be electrically connected to the first bonding pad **23***a* by the wirings **223***a*.

[0076] A liner layer may be provided on a side surface of the through electrode **24***a*. The liner layer may include silicon oxide or carbon-doped silicon oxide. The liner layer may electrically insulate the through electrode **24***a* from the substrate **21***a* and the metal wiring layer **222***a*.

[0077] The through electrode **24***a* and the first bonding pad **23***a* may include a same metal. For example, the metal may include copper (Cu). However, it is not limited thereto, and the through electrode and the first bonding pad may include a material (e.g., gold (Au)) that can be bonded by inter-diffusion of metals by a high-temperature annealing process.

[0078] As illustrated in FIG. **7**, the second surface **214***a* of the substrate **21***a* may be partially removed to expose one end portion of the through electrode **24***a*.

[0079] In example embodiments, first, a grinding process such as a back lap process may be performed to partially remove the second surface **214***a* of the substrate **21***a*, and then an etching process such as a silicon recess process may be performed to expose the end portion of the through electrode **24***a*. Accordingly, a thickness of the substrate **21***a* may be reduced to a desired thickness. For example, the substrate **21***a* may have the thickness in a range of about 10 μm to about 30 μm.

[0080] In the back lap process, the entire second surface **214***a* of the substrate **21***a* may be grinded. In the silicon recess process, only the silicon in the second surface **214***a* of the substrate **21***a* may be selectively etched. The etching process may be an isotropic dry etching process. The etching process may include a plasma etching process, etc. The plasma etching process may be performed using inductively coupled plasma, capacitively coupled plasma, microwave plasma, etc.

[0081] As illustrated in FIGS. **8** and **9**, a backside insulating layer **26***a* having second bonding pads **27***a* in an outer surface thereof may be formed on the second surface **214***a* of the substrate **21***a*.

[0082] For example, a polishing stop layer may be formed on the second surface **214***a* of the substrate **21***a*, and a sacrificial layer may be formed on the polishing stop layer. The polishing stop layer may be conformally formed to cover end portions of the through electrodes **24***a* that protrude from the second surface **214***a* of the substrate **21***a*. For example, the polishing stop layer may have a thickness within a range of 0.1 μm to 1 μm. The polishing stop layer may include a material that can be used to detect a polishing end point in a subsequent chemical mechanical polishing process. The polishing stop layer may include a silicon nitride layer. The thickness and material of the polishing stop layer may be selected in consideration of a polishing selectivity and polishing conditions in the subsequent chemical mechanical polishing process.

[0083] The sacrificial layer may be formed to fill a gap between the protruding end portions of the through electrodes **24***a*. The sacrificial layer may include silicon oxide such as TEOS.

[0084] Then, a chemical mechanical polishing (CMP) process using the polishing stop layer to detect a polishing end point may be performed to remove the sacrificial layer to expose the end portions of the through electrodes **24***a*. Through the CMP process, the end portions of the through electrodes **24***a* and portions of the polishing stop layer covering or on them may be removed to form a polishing stop layer pattern **25***a* on the second surface **214***a* of the substrate **21***a*.

[0085] The polishing stop layer pattern **25***a* may expose end portions of the through electrodes **24***a*. The end portions of the through electrodes **24***a* may protrudes from the second surface **214***a* of the substrate **21***a*, and the polishing stop layer pattern **25***a* may cover or surround sidewalls of the end portions of the through electrodes **24***a* that protrude from the second surface **214***a* of the substrate **21***a*. Accordingly, upper surfaces of the through electrodes **24***a* may be exposed by the polishing stop layer pattern **25***a*. The upper surface of the polishing stop layer pattern **25***a* and the exposed upper surfaces of the through electrodes **24***a* may be coplanar or positioned on the same plane.

[0086] Then, the backside insulating layer **26***a* as a second passivation layer having the second bonding pad **27***a* that is electrically connected to the through electrode **24***a* may be formed on the polishing stop layer pattern **25***a* on the second surface **214***a* of the substrate **21***a*.

[0087] For example, after the backside insulating layer **26***a* is formed on the polishing stop layer pattern **25***a* on the second surface **214***a* of the substrate **21***a*, an opening may be

formed in the backside insulating layer **26***a* to expose the through electrode **24***a*, and a plating process may be performed to form the second bonding pad **27***a* in the opening of the backside insulating layer **26***a*. The second bonding pad **27***a* may be disposed on the exposed upper surface of the through electrode **24***a*. An upper surface of the second bonding pad **27***a* may be coplanar with an upper surface of the backside insulating layer **26***a* and/or a lower surface of the second bonding pad **27***a* may be coplanar with a lower surface of the backside insulating layer **26***a*. The backside insulating layer **26***a* may include silicon oxide, carbon-doped silicon oxide, silicon carbonitride (SiCN), etc. Accordingly, the first and second bonding pads **23***a* and **27***a* may be electrically connected to each other by the through electrode **24***a*.

[0088] Thus, the plurality of first die structures each including a first core die **20***a* may be formed on the first carrier substrate C**1**. The first core dies **20***a* may be arranged on the first carrier substrate C**1** such that the first surface **212***a* of the substrate **21***a* of each of the first core dies **20***a* faces the first carrier substrate C**1**. Each of the first core dies **20***a* may include the substrate **21***a*, the front insulating layer **22***a*, and the backside insulating layer **26***a*.

[0089] Referring to FIGS. **10** to **16**, second die structures may be stacked respectively on the first die structures on the first carrier substrate C**1**.

[0090] As illustrated in FIGS. **10** and **11**, a plurality of second core dies **20***b* may be attached on the first die structures on the first carrier substrate C**1** (die-to-wafer hybrid bonding process).

[0091] In example embodiments, the second core dies **20***b* may be disposed on the first die structures respectively to correspond to the first core dies **20***a* of the first die structures. The second core dies **20***b* may be stacked such that a first surface **212***b* of a substrate **21***b* of each of the second core dies **20***b* faces the first carrier substrate C**1**.

[0092] A die bonding apparatus may pick up the second core die **20***b* individualized through a sawing process and may bond it to the first die structure. The die bonding apparatus may attach the second core die **20***b* to the first die structure by performing a thermal compression process at a predetermined temperature (for example, about 400° C. or less). By the thermal compression process, the second core die **20***b* and the first die structure may be bonded to each other through hybrid bonding. That is, a front surface of the second core die **20***b*, that is, a front insulating layer **22***b* on a first surface **212***b* of a substrate **21***b* may be directly bonded to the backside insulating layer **26***a* of the first die structure.

[0093] The second bonding pad **27***a* of the first die structure and a first bonding pad **23***b* of the second core die **20***b* may make contact with each other. When the first die structure and the second core die **20***b* are bonded to each other by die-to-wafer bonding, the second bonding pad **27***a* of the first die structure and the first bonding pads **23***b* of the second core die **20***b* may be bonded to each other by copper-copper hybrid bonding (Cu—Cu Hybrid Bonding).

[0094] As illustrated in FIG. **12**, the second surface **214***b* of the substrate **21***b* of the second core die **20***b* may be partially removed to expose one end portion of a through electrode **24***b*. First, a grinding process such as a back lap process may be performed to partially remove the second surface **214***b* of the substrate **21***b*, and then an etching process such as a silicon recess process may be performed to expose the end portion of the through electrode **24***b*. Accordingly, a thickness of the substrate **21***b* may be reduced to a desired thickness. For example, the substrate **21***a* may have the thickness in a range of about 10 μm to about 30 μm.

[0095] As illustrated in FIG. **13**, a gap filling layer GF may be formed on the first die structure to cover the second core dies **20***b*.

[0096] For example, a polishing stop layer may be formed on the second wafer W**2** along a profile of the second core dies **20***b*. The polishing stop layer may be conformally formed to cover end portions of the through electrodes **24***b* that protrude from the second surface **214***b* of the substrate **21***b*. For example, the polishing stop layer may have a thickness within a range of 0.1 μm to 1 μm. The polishing stop layer may include a material that can be used to detect a polishing end point in a subsequent chemical mechanical polishing process. The polishing stop layer may include a silicon nitride layer. The thickness and material of the polishing stop layer may be selected in consideration of a polishing selectivity and polishing conditions in the subsequent chemical mechanical polishing process.

[0097] Although it is not illustrated in the figures, a sacrificial layer may be formed on the polishing stop layer. The sacrificial layer may be formed to fill a gap between the protruding end portions of the through electrodes **24***b*. The sacrificial layer may include silicon oxide such as TEOS.

[0098] Then, a chemical mechanical polishing (CMP) process using the polishing stop layer to detect a polishing end point may be performed to remove the sacrificial layer to expose the end portions of the through electrodes **24***a*. Through the CMP process, the end portions of the through electrodes **24***a* and portions of the polishing stop layer covering them may be removed to form a polishing stop layer pattern **25***a* on the second surface **214***a* of the substrate **21***a*.

[0099] The polishing stop layer pattern **25***a* may expose end portions of the through electrodes **24***a*. The end portions of the through electrodes **24***a* may protrudes from the second surface **214***a* of the substrate **21***a*, and the polishing stop layer pattern **25***a* may cover sidewalls of the end portions of the through electrodes **24***a* that protrude from the second surface **214***a* of the substrate **21***a*. Accordingly, upper surfaces of the through electrodes **24***a* may be exposed by the polishing stop layer pattern **25***a*. The upper surface of the polishing stop layer pattern **25***a* and the exposed upper surfaces of the through electrodes **24***a* may be coplanar or positioned on the same plane.

[0100] Then, the gap filling layer GF may be formed on the second wafer W**2** to cover the polishing stop layer on the second core dies **20***b*. The gap filling layer GF may cover or surround an outer side surface and upper surfaces of the second core dies **20***b*. For example, the gap filling layer GF may be formed by a conformal deposition process such as an atomic layer deposition (ALD) process or a chemical vapor deposition (CVD) process. The gap filling layer may include an inorganic dielectric layer or an organic dielectric layer. The inorganic dielectric layer may include silicon oxide, silicon oxynitride, phosphosilicate glass (PSG), boro-phosphosilicate glass (BPSG), etc. The organic dielectric layer may include a polymer or the like.

[0101] As illustrated in FIG. **14**, an upper portion of the gap filling layer GF may be removed to form a gap filling portion or member **30***b* that covers or surrounds the outer

side surface of the second core die **20***b* and exposes the upper surface of the second core die **20***b*. A chemical mechanical polishing (CMP) process using the polishing stop layer to detect a polishing end point may be performed to remove the upper portion of the gap filling layer GF and the sacrificial layer to expose end portions of the through electrodes **24***b*. Through the CMP process, the end portions of the through electrodes **24***b* and portions of the polishing stop layer covering them may be removed to form a polishing stop layer pattern on the second surface **214***b* of the substrate **21***b*.

[0102] The gap filling portion **30***b* may expose the polishing stop layer pattern and the end portions of the through electrodes **24***b* on the second surface **214***b* of the substrate **21***b*. The gap filling portion **30***b* may cover or surround outer side surfaces of the substrate **21***b* and the front insulating layer **22***b*.

[0103] As illustrated in FIG. **15**, a backside insulating layer **26***b* having second bonding pads **27***b* in an outer surface thereof may be formed on the second surface **214***b* of the substrate **21***b*.

[0104] In particular, the backside insulating layer **26***b* as a second passivation layer having the second bonding pad **27***b* that is electrically connected to the through electrode **24***b* may be formed on the polishing stop layer pattern **25***b* on the second surface **214***b* of the substrate **21***b*.

[0105] The polishing stop layer pattern may expose end portions of the through electrodes **24***b*. The end portions of the through electrodes **24***b* may protrude from the second surface **214***b* of the substrate **21***b*, and the polishing stop layer pattern **25***b* may cover or surround sidewalls of the end portions of the through electrodes **24***b* that protrude from the second surface **214***b* of the substrate **21***b*. Accordingly, upper surfaces of the through electrodes **24***b* may be exposed by the polishing stop layer pattern. An upper surface of the polishing stop layer pattern and the exposed upper surfaces of the through electrodes **24***a* may be coplanar or positioned on the same plane.

[0106] For example, after the backside insulating layer **26***a* is formed on the polishing stop layer pattern and the gap filling portion **30***b* on the second surface **214***b* of the substrate **21***b*, an opening may be formed in the backside insulating layer **26***b* to expose the through electrode **24***b*, and a plating process may be performed to form the second bonding pad **27***b* in the opening of the backside insulating layer **26***b*. The second bonding pad **27***b* may be disposed on the exposed upper surface of the through electrode **24***b*. The backside insulating layer **26***b* may include silicon oxide, carbon-doped silicon oxide, silicon carbonitride (SiCN), etc. Accordingly, the first and second bonding pads **23***b* and **27***b* may be electrically connected to each other by the through electrode **24***b*.

[0107] Thus, the second die structures each including a second core die **20***b* and the gap filling portion **30***b* covering or surrounding the outer side surface of the second core die **20***b* may be formed on the first die structures on the first carrier substrate C**1**. The second core dies **20***b* may be spaced apart from each other at the wafer level on the first die structures. The second core dies **20***b* may be arranged on the first die structures on the first carrier substrate C**1** such that the first surface **212***b* of the substrate **21***b* of each of the second core dies **20***b* faces the first carrier substrate C**1**. Each of the second core dies **20***b* may include the substrate **21***b*, the front insulating layer **22***b*, and the backside insulating layer **26***b*. The gap filling portion **30***b* may cover the outer side surfaces of the substrate **21***b* and the front insulating layer **22***b* of the second core die **20***b*. The backside insulating layer **26***b* may extend laterally from or along the second surface **214***b* of the substrate **21***b* to cover an upper surface of the gap fill portion **30***b*.

[0108] Referring to FIG. **16**, processes the same as or similar to the processes described with reference to FIGS. **10** to **15** may be performed to form a third die structure on the second die structure.

[0109] The third die structure including a third core die **20***c* and a gap filling portion **30***c* covering or surrounding an outer side surface of the third core die **20***c* may be formed on the second die structure. The third core dies **20***c* may be spaced apart from each other at the wafer level on the second die structures. The third core dies **20***c* may be arranged on the second die structure such that a first surface **212***c* of a substrate **21***c* of the third core die **20***c* faces the first carrier substrate C**1**. Each of the third core dies **20***c* may include a substrate **21***c*, a front insulating layer **22***c*, and a backside insulating layer **26***c*. The gap filling portion **30***c* may cover or surround outer side surfaces of the substrate **21***c* and the front insulating layer **22***c* of the third core die **20***c*. The backside insulating layer **26***c* may extend laterally from or along a second surface **214***c* of the substrate **21***c* to cover an upper surface of the gap fill portion **30***c*.

[0110] The second bonding pad **27***b* of the second die structure and a first bonding pad **23***c* of the third core die **20***c* may make contact with each other. When the second die structure and the third core die **20***c* are bonded to each other by die-to-wafer bonding, the second bonding pad **27***b* of the second die structure and the first bonding pads **23***c* of the third core die **20***c* may be bonded to each other by copper-copper hybrid bonding (Cu—Cu Hybrid Bonding). A front surface of the third core die **20***c*, that is, the front insulating layer **22***c* on the first surface **212***c* of the substrate **21***c* may be directly bonded to the backside insulating layer **26***b* of the second die structure.

[0111] Referring to FIG. **17**, the stacked first to third die structures may be cut along the cutting region SA, that is, a scribe lane region, by a first sawing process to form individual core die blocks CB**1** on the first carrier substrate C**1**.

[0112] Each of the core die blocks CB**1** may include first, second and third die structures DS**1**, DS**2**, and DS**3** sequentially stacked. The first die structure DS**1** may include the first core die **20***a*. The second die structure DS**2** may include the second core die **20***b* and the gap filling portion **30***b*. The third die structure DS**3** may include the third core die **20***c* and the gap filling portion **30***c*. In example embodiments, the core die block CB**1** may include the core dies **20***a*, **20***b*, and **20***c* stacked in three stages, but it will be understood that the present inventive concept is not limited thereto.

[0113] The core die block CB**1** may have a rectangular parallelepiped shape. A lower surface of the first die structure DS**1** may serve as a lower surface of the core die block CB**1**, and an upper surface of the third die structure DS**3** may serve as an upper surface of the core die block CB**1**.

[0114] The core die block CB**1** may have a thickness T**1** of at least 40 μm. Each of the first to third core dies **20***a*, **20***b*, and **20***c* may have a thickness within a range of about 10 μm to 30 μm. The first core die **20***a* may have a first planar area, and the second and third core dies **20***b* and **20***c* may have a second planar area that is less or smaller than the first planar area. The first core die **20***a* may have a first (horizontal)

width, and the second and third core dies **20***b* and **20***c* may have a second (horizontal) width less than the first width.

[0115] Since the core die block CB**1** is formed by cutting the stacked first, second and third die structures through the first sawing process, outer side surfaces of the first, second, and third die structures, that is, outer side surface of the gap filling portions **30***b* and **30***c*, of the core die block CB**1** may be coplanar or positioned on the same plane.

[0116] Referring to FIGS. **18** and **19**, the first core die blocks CB**1** may be attached in a first stage on a first wafer W**1** including buffer dies (die-to-wafer hybrid bonding process).

[0117] In example embodiments, first, conductive bumps **50** may be formed on a front surface of the first wafer W**1** and an adhesive film AF may be formed on the front surface of the first wafer W**1** to cover the conductive bumps **50**. Then, the first wafer W**1** may be attached to a second carrier substrate C**2** using the adhesive film AF.

[0118] Then, the first core die blocks CB**1** may be disposed on the first wafer W**1** to correspond to die regions DA. The first core die blocks CB**1** may be stacked such that the lower surface of the first core die block CB**1**, that is, the lower surface of the first die structure DS**1** faces the first wafer W**1**.

[0119] A die bonding apparatus may pick up the first core die block CB**1** individualized through the first sawing process and may bond it to the first wafer W**1**. The die bonding apparatus may attach the first core die block CB**1** to the first wafer W**1** by performing a thermal compression process at a predetermined temperature (for example, about 400° C. or less). By the thermal compression process, the first core die block CB**1** and the first wafer W**1** may be bonded to each other through hybrid bonding. That is, the lower surface of the first core die block CB**1**, that is, the front insulating layer **22***a* of the first die structure DS**1** may be directly bonded to a backside insulating layer **16** of a substrate **11** of the first wafer W**1**.

[0120] A second bonding pad **17** of the first wafer W**1** and the first bonding pad **23***a* of the first die structure DS**1** of the first core die block CB**1** may make contact with each other. The lower surface of the first core die block CB**1**, that is the front surface of the first core die **20***a* of the first die structure DS**1** and a backside surface of the first wafer W**1** may be bonded to face each other. When the first wafer W**1** and the first core die block CB**1** are bonded to each other by die-to-wafer bonding, the second bonding pad **17** of the first wafer and the first bonding pads **23***a* of the first core die **20***a* may be bonded to each other by copper-copper hybrid bonding (Cu—Cu Hybrid Bonding).

[0121] Referring to FIG. **20**, processes the same as or similar to the processes described with reference to FIGS. **18** and **19** may be performed to attach a plurality of second core die blocks CB**2** in a second stage on the first core die blocks CB**1** on the first wafer W**1** (die-to-wafer hybrid bonding process).

[0122] A lower surface of the second core die block CB**2** of the second stage may be stacked to face the upper surface of the first core die block CB**1** of the first stage. Through a thermal compression process, the second core die block CB**2** of the second stage and the first core die block CB**1** of the first stage may be bonded to each other through hybrid bonding. That is, a front insulating layer **22***a* of a first core die **20***a* of the second core die block CB**2** may be directly bonded to the backside insulating layer **26***c* of the third core die **20***c* of the first core die block CB**1** of the first stage. When the first core die block CB**1** of the first stage and the second core die block CB**2** of the second stage are bonded to each other by die-to-die bonding, the second bonding pad **27***c* of the third core die **20***c* of the first core die block CB**1** of the first stage and a first bonding pad **23***a* of the first core die **20***a* of the second core die block CB**2** of the second stage may be bonded to each other by copper-copper hybrid bonding (Cu—Cu Hybrid Bonding).

[0123] Since the first core die block CB**1** and the second core die block CB**2** are bonded to each other by die-to-die bonding, misalignment between the first core die block CB**1** and the second core die block CB**2** may occur. Accordingly, an outer side surface SF**1** of the first core die block CB**1** and an outer side surface SF**2** of the second core die block CB**2** may be positioned on different planes respectively.

[0124] Referring to FIG. **21**, processes the same as or similar to the processes described with reference to FIG. **20** may be performed to attach a plurality of third core die blocks CB**3** in a third stage on the second core die blocks CB**2** (die-to-wafer hybrid bonding process), to attach a plurality of fourth core die blocks CB**4** in a fourth stage on the third core die blocks CB**3** (die-to-wafer hybrid bonding process), and to attach a plurality of fifth core die blocks CB**5** in a fifth stage on the fourth core die blocks CB**4** (die-to-wafer hybrid bonding process).

[0125] A lower surface of the third core die block CB**3** of the third stage may be stacked to face an upper surface of the second core die block CB**2** of the second stage. Through a thermal compression process, the third core die block CB**3** of the third stage and the second core die block CB**2** of the second stage may be bonded to each other through hybrid bonding. That is, a front insulating layer **22***a* of a first core die **20***a* of the third core die block CB**3** may be directly bonded to a backside insulating layer **26***c* of a third core die **20***c* of the second core die block CB**2** of the second stage. When the second core die block CB**2** of the second stage and the third core die block CB**3** of the third stage are bonded to each other by die-to-die bonding, a second bonding pad **27***c* of the third core die **20***c* of the second core die block CB**2** of the second stage and a first bonding pad **23***a* of the first core die **20***a* of the third core die block CB**3** of the third stage may be bonded to each other by copper-copper hybrid bonding (Cu—Cu Hybrid Bonding).

[0126] Since the second core die block CB**2** and the third core die block CB**3** are bonded to each other by die-to-die bonding, misalignment between the second core die block CB**2** and the third core die block CB**3** may occur. Accordingly, the outer side surface SF**2** of the second core die block CB**2** and an outer side surface SF**3** of the third core die block CB**3** may be positioned on different planes respectively.

[0127] Then, a lower surface of the fourth core die block CB**4** of the fourth stage may be stacked to face an upper surface of the third core die block CB**3** of the third stage. Through a thermal compression process, the fourth core die block CB**4** of the fourth stage and the third core die block CB**3** of the third stage may be bonded to each other through hybrid bonding. That is, a front insulating layer **22***a* of a first core die **20***a* of the fourth core die block CB**4** may be directly bonded to a backside insulating layer **26***c* of a third core die **20***c* of the third core die block CB**3** of the third stage. When the third core die block CB**3** of the third stage and the fourth core die block CB**4** of the fourth stage are bonded to each other by die-to-die bonding, a second

bonding pad **27***c* of the third core die **20***c* of the third core die block CB**3** of the third stage and a first bonding pad **23***a* of the first core die **20***a* of the fourth core die block CB**4** of the fourth stage may be bonded to each other by copper-copper hybrid bonding (Cu—Cu Hybrid Bonding).

[0128] Since the third core die block CB**3** and the fourth core die block CB**4** are bonded to each other by die-to-die bonding, misalignment between the third core die block CB**3** and the fourth core die block CB**4** may occur. Accordingly, the side surface SF**3** of the third core die block CB**3** and a side surface SF**4** of the fourth core die block CB**4** may be positioned on different planes respectively.

[0129] Then, a lower surface of the fifth core die block CB**5** of the fifth stage may be stacked to face an upper surface of the fourth core die block CB**4** of the fourth stage. Through a thermal compression process, the fifth core die block CB**5** of the fifth stage and the fourth core die block CB**4** of the fourth stage may be bonded to each other through hybrid bonding. That is, a front insulating layer **22***a* of a first core die **20***a* of the fifth core die block CB**5** may be directly bonded to a backside insulating layer **26***c* of a third core die **20***c* of the fourth core die block CB**4** of the fourth stage. When the fourth core die block CB**4** of the fourth stage and the fifth core die block CB**5** of the fifth stage are bonded to each other by die-to-die bonding, a second bonding pad **27***c* of the third core die **20***c* of the fourth core die block CB**4** of the fourth stage and a first bonding pad **23***a* of the first core die **20***a* of the fifth core die block CB**5** of the fifth stage may be bonded to each other by copper-copper hybrid bonding (Cu—Cu Hybrid Bonding).

[0130] Since the fourth core die block CB**4** and the fifth core die block CB**5** are bonded to each other by die-to-die bonding, misalignment between the fourth core die block CB**4** and the fifth core die block CB**5** may occur. Accordingly, the outer side surface SF**4** of the fourth core die block CB**4** and an outer side surface SF**5** of the fifth core die block CB**5** may be positioned on different planes respectively.

[0131] The number of the core die blocks sequentially stacked on the first wafer W**1** may be determined according to the total number of core dies stacked on the buffer die and the number of the core dies in each core die block.

[0132] Referring to FIG. **22**, a top core die stack TD may be attached to the fifth core die block CB**5**.

[0133] In example embodiments, the top core die stack TD may include a top core die **20***d*. The top core dies **20***d* may be disposed on the fifth core die blocks CB**5** to correspond to the first core dies **20***c* of the fifth core die blocks CB**5**. A first surface **212***d* of a substrate **21***d* of the top core die **20***d* may be stacked to face the fifth core die block CB**5**.

[0134] A die bonding apparatus may pick up the top core die **20***d* individualized through a sawing process and may bond it to the fifth core die block. The die bonding apparatus may attach the top core die **20***d* to the fifth core die block by performing a thermal compression process at a predetermined temperature (for example, about 400° C. or less). By the thermal compression process, the top core die **20***d* and the fifth core die block may be bonded to each other through hybrid bonding. That is, a front surface of the top core die **20***d*, that is, a front insulating layer **22***d* on the first surface **212***d* of the substrate **21***d* may be directly bonded to a backside insulating layer **26***c* of the third core die **20***c* of the fifth core die block.

[0135] A second bonding pad **27***c* of the third core die **20***c* of the fifth core die block and a first bonding pad **23***d* of the top core die **20***d* may make contact with each other. When the fifth core die block and the top core die **20***d* are bonded to each other by die-to-wafer bonding, the second bonding pad **27***c* of the third core die **20***c* of the fifth core die block and the first bonding pads **23***d* of the top core die **20***d* may be bonded to each other by copper-copper hybrid bonding (Cu—Cu Hybrid Bonding).

[0136] A thickness of the top core die **20***d* may be greater than thicknesses of the middle core dies **20***a*, **20***b*, and **20***c*. The thickness of the top core die **20***d* may be within a range of 50 μm to 300 μm.

[0137] Referring to FIG. **23**, a molding member **40** may be formed to fill or be in gaps between the first, second, third, fourth and fifth core die blocks CB**1**, CB**2**, CB**3**, CB**4** and CB**5** sequentially stacked on the first wafer W**1**.

[0138] For example, the molding member **40** as a gap filling portion may be formed on the first wafer W**1** to fill the gap between the first, second, and third core die blocks CB**1**, CB**2**, and CB**3**. The molding member **40** may expose an upper surface of the top core die **20***d*. An upper surface of the molding member **40** and an upper surface of the top core die **20***d* may be coplanar. The molding member **40** may directly contact the outer side surfaces SF**1**, SF**2**, SF**3**, SF**4** and SF**5** of the first, second, third, fourth and fifth core die blocks CB**1**, CB**2**, CB**3**, CB**4** and CB**5**.

[0139] For example, the molding member may include a thermosetting resin. The molding material may include an epoxy mold compound (EMC). The molding material may include UV resin, polyurethane resin, silicone resin, silica filler, etc.

[0140] Then, portions of the first wafer W**1** and the molding member **40** may be cut along a cutting region SA, that is, a scribe lane region by a second sawing process to complete the semiconductor package **100** of FIG. **1**.

[0141] FIG. **24** is a cross-sectional view illustrating a semiconductor package in accordance with example embodiments. FIG. **25** is a cross-sectional view illustrating a core die block of the semiconductor package in FIG. **24**. The semiconductor package is substantially the same as or similar to the semiconductor package described with reference to FIG. **1** except for a configuration of a core die block. Thus, same reference numerals will be used to refer to the same or like elements and any further repetitive explanation concerning the above elements may be omitted in the interest of brevity.

[0142] Referring to FIGS. **24** and **25**, a semiconductor package **101** may include a buffer die **10**, and a plurality of core die blocks CB**1**, CB**2**, CB**3**, CB**4**, CB**5** sequentially stacked on the buffer die **10**. Each of the core die blocks CB**1**, CB**2**, CB**3**, CB**4**, CB**5** may include first, second and third die structures DS**1**, DS**2** and DS**3** sequentially stacked. Each of the core die blocks CB**1**, CB**2**, CB**3**, CB**4**, CB**5** may include a plurality of core dies **20***a*, **20***b*, and **20***c* sequentially stacked, and a plurality of gap filling portions or members **30***a*, **30***b*, and **30***c* respectively covering or surrounding outer side surfaces of the plurality of core dies **20***a*, **20***b*, and **20***c* stacked in at least two stages.

[0143] In example embodiments, the gap filling portion **30***a* of the first die structure DS**1** may at least partially cover or surround the outer side surface of the first core die **20***a*. The gap filling portion **30***a* may cover or surround outer side surfaces of a substrate **21***a* and a front insulating layer **22***a* of the first core die **20***a*. A backside insulating layer **26***a* of the first core die **20***a* may cover an upper surface of the gap

filling portion **30***a*. The backside insulating layer **26***a* may protrude or extend in a horizontal direction from the outer side surfaces of the substrate **21***a* and the front insulating layer **22***a*, and the protruding portion of the backside insulating layer **26***a* may cover the upper surface of the gap filling portion **30***a*. An outer side surface of the backside insulating layer **26***b* and an outer side surface of the gap filling portion **30***a* may be coplanar or positioned on the same plane.

[0144] Similarly, the gap filling portion **30***b* of the second die structure DS**2** may at least partially cover or surround the outer side surface of the second core die **20***b*. The gap filling portion **30***b* may cover or surround outer side surfaces of a substrate **21***b* and a front insulating layer **22***b* of the second core die **20***b*. A backside insulating layer **26***b* of the second core die **20***b* may cover an upper surface of the gap filling portion **30***b*. The backside insulating layer **26***b* may protrude or extend in a horizontal direction from the outer side surfaces of the substrate **21***b* and the front insulating layer **22***b*, and the protruding portion of the backside insulating layer **26***b* may cover the upper surface of the gap filling portion **30***b*. An outer side surface of the backside insulating layer **26***b* and an outer side surface of the gap filling portion **30***b* may be coplanar or positioned on the same plane.

[0145] Similarly, the gap filling portion **30***c* of the third die structure DS**3** may at least partially cover or surround the outer side surface of the third core die **20***c*. The gap filling portion **30***c* may cover or surround outer side surfaces of a substrate **21***c* and a front insulating layer **22***c* of the third core die **20***c*. A backside insulating layer **26***c* of the third core die **20***c* may cover an upper surface of the gap filling portion **30***c*. The backside insulating layer **26***c* may protrude or extend in a horizontal direction from the outer side surfaces of the substrate **21***c* and the front insulating layer **22***c*, and the protruding portion of the backside insulating layer **26***c* may cover the upper surface of the gap filling portion **30***c*. An outer side surface of the backside insulating layer **26***c* and the outer side surface of the gap filling portion **30***c* may be coplanar or positioned on the same plane.

[0146] The backside insulating layer **26***a* of the first die structure DS**1** may cover or be on a lower surface of the gap filling portion **30***b* of the second die structure DS**2**. The backside insulating layer **26***b* of the second die structure DS**2** may cover or be on a lower surface of the gap filling portion **30***c* of the third die structure RD**3**. Additionally, the outer side surfaces of the gap filling portions **30***a*, **30***b*, **30***c* of the first core die block CB**1** may be coplanar or positioned on the same plane.

[0147] Hereinafter, a method of manufacturing the semiconductor package of FIGS. **24** and **25** will be described.

[0148] FIGS. **26** to **34** are views illustrating a method of manufacturing a semiconductor package in accordance with example embodiments.

[0149] Referring to FIGS. **26** to **30**, first die structures may be formed on a first carrier substrate C**1**.

[0150] As illustrated in FIG. **26**, a plurality of first semiconductor chips (first core dies) **20***a* diced from a wafer may be placed on the first carrier substrate C**1**.

[0151] The first core die **20***a* may include a substrate **21***a* and a front insulating layer **22***a* having first bonding pads **23***a* that are provided in an outer surface thereof. Additionally, the first core die **20***a* may include a plurality of through electrodes **24***a* that are provided in the substrate **21***a* and are electrically connected to the first bonding pads **23***a*.

[0152] As illustrated in FIG. **27**, a second surface **214***a* of the substrate **21***a* may be partially removed to expose one end portion of the through electrode **24***a*.

[0153] In example embodiments, first, a grinding process such as a back lap process may be performed to partially remove the second surface **214***a* of the substrate **21***a*, and then an etching process such as a silicon recess process may be performed to expose the end portion of the through electrode **24***a*. Accordingly, a thickness of the substrate **21***a* may be reduced to a desired thickness. For example, the substrate **21***a* may have the thickness in a range of about 10 μm to about 30 μm.

[0154] In the back lap process, the entire second surface **214***a* of the substrate **21***a* may be grinded. In the silicon recess process, only the silicon in the second surface **214***a* of the substrate **21***a* may be selectively etched. The etching process may be an isotropic dry etching process. The etching process may include a plasma etching process, etc. The plasma etching process may be performed using inductively coupled plasma, capacitively coupled plasma, microwave plasma, etc.

[0155] As illustrated in FIG. **28**, a gap filling layer GF may be formed on the first carrier substrate C**1** to cover the first core dies **20***a*.

[0156] First, a polishing stop layer may be formed along a profile of the first core dies **20***a* on the first carrier substrate C**1**. The polishing stop layer may be conformally formed to cover the end portions of the through electrodes **24***a* that protrude from the second surface **214***a* of the substrate **21***a*. Although it is not illustrated in the figures, a sacrificial layer may be formed on the polishing stop layer. The sacrificial layer may be formed to fill a gap between the protruding end portions of the through electrodes **24***a*.

[0157] Then, the gap filling layer GF may be formed to cover the polishing stop layer on the first core dies **20** on the first carrier substrate C**1**. The gap filling layer GF may cover or surround side surfaces and upper surfaces of the first core dies **20***a*. For example, the gap filling layer GF may be formed by a conformal deposition process such as an atomic layer deposition (ALD) process or a chemical vapor deposition (CVD) process. The gap filling layer may include an inorganic dielectric layer or an organic dielectric layer. The inorganic dielectric layer may include silicon oxide, silicon oxynitride, phosphosilicate glass (PSG), boro-phosphosilicate glass (BPSG), etc. The organic dielectric layer may include a polymer or the like.

[0158] As illustrated in FIG. **29**, an upper portion of the gap filling layer GF may be removed to form a gap filling portion **30***a* that covers or surrounds an outer side surface of the first core die **20***a* and exposes an upper surface of the first core die **20***a*. A chemical mechanical polishing (CMP) process using the polishing stop layer to detect a polishing end point may be performed to remove the upper portion of the gap filling layer GF and the sacrificial layer to expose the end portions of the through electrodes **24***a*. Through the CMP process, the end portions of the through electrodes **24***a* and portions of the polishing stop layer covering them may be removed to form a polishing stop layer pattern on the second surface **214***a* of the substrate **21***a*.

[0159] The gap filling portion **30***a* may expose the polishing stop layer pattern and end portions of the through electrodes **24***a* on the second surface **214***a* of the substrate

21*a*. The gap filling portion **30***a* may cover or surround outer side surfaces of the substrate **21***a* and the front insulating layer **22***a*.

[0160] As illustrated in FIG. **30**, a backside insulating layer **26***a* having a second bonding pad **27***a* in an outer surface thereof may be formed on the second surface **214***a* of the substrate **21***a*.

[0161] In particular, the backside insulating layer **26***a* as a second passivation layer having the second bonding pad **27***a* that is electrically connected to the through electrode **24***a* may be formed on the etch stop layer pattern **25***a* on the second surface **214***a* of the substrate **21***a*.

[0162] The polishing stop layer pattern may expose the end portions of the through electrodes **24***a*. The end portions of the through electrodes **24***a* may protrude from the second surface **214***a* of the substrate **21***a*, and the polishing stop layer pattern may cover or surround sidewalls of the end portions of the through electrodes **24***a* that protrude from the second surface **214***a* of the substrate **21***a*. Accordingly, the upper surfaces of the through electrodes **24***a* may be exposed by the polishing stop layer pattern. An upper surface of the polishing stop layer pattern and the exposed upper surfaces of the through electrodes **24***a* may be coplanar or positioned on the same plane.

[0163] For example, after the backside insulating layer **26***a* is formed on the polishing stop layer pattern and the gap filling portion **30***a* on the second surface **214***a* of the substrate **21***a*, an opening may be formed in the backside insulating layer **26***a* to expose the through electrode **24***a*, and a plating process may be performed to form the second bonding pad **27***a* in the opening of the backside insulating layer **26***a*. The second bonding pad **27***a* may be disposed on the exposed surface of the through electrode **24***a*. The backside insulating layer **26***a* may include silicon oxide, carbon-doped silicon oxide, silicon carbonitride (SiCN), etc. Accordingly, the first and second bonding pads **23***a* and **27***a* may be electrically connected to each other by the through electrode **24***a*.

[0164] Thus, the first die structure including the first core die **20***a* and the gap filling portion **30***a* covering or surrounding the outer side surface of the first core die **20***a* may be formed on the first carrier substrate C**1**. The first core dies **20***a* may be spaced apart from each other at the wafer level on the first carrier substrate C**1**. The first core dies **20***a* may be arranged on the first carrier substrate C**1** such that the first surface **212***a* of the substrate **21***a* of the first core die **20***a* faces the first carrier substrate C**1**. Each of the first core dies **20***a* may include the substrate **21***a*, the front insulating layer **22***a*, and the backside insulating layer **26***a*. The gap filling portion **30***a* may cover or surround the outer side surfaces of the substrate **21***a* and the front insulating layer **22***a* of the first core die **20***a*. The backside insulating layer **26***a* may extend laterally from or along the second surface **214***a* of the substrate **21***a* to cover an upper surface of the gap fill portion **30***a*.

[0165] Referring to FIGS. **31** and **32**, processes the same as or similar to the processes described with reference to FIGS. **27** to **30** may be performed to stack a second die structure on the first die structure on the first carrier substrate C**1**.

[0166] As illustrated in FIG. **31**, a plurality of second core dies **20***b* may be attached on the first die structures on the first carrier substrate C**1** (die-to-wafer hybrid bonding process).

[0167] In example embodiments, the second core dies **20***b* may be disposed on the first die structures respectively to correspond to the first core dies **20***a* of the first die structures. The second core dies **20***b* may be stacked such that a first surface **212***b* of a substrate **21***b* of each of the second core dies **20***b* faces the first carrier substrate C**1**.

[0168] A die bonding apparatus may pick up the second core die **20***b* individualized through a sawing process and may bond it to the first die structure. The die bonding apparatus may attach the second core die **20***b* to the first die structure by performing a thermal compression process at a predetermined temperature (for example, about 400° C. or less). By the thermal compression process, the second core die **20***b* and the first die structure may be bonded to each other through hybrid bonding. That is, a front surface of the second core die **20***b*, that is, a front insulating layer **22***b* on a first surface **212***b* of a substrate **21***b* may be directly bonded to the backside insulating layer **26***a* of the first die structure.

[0169] The second bonding pad **27***a* of the first die structure and a first bonding pad **23***b* of the second core die **20***b* may make contact with each other. When the first die structure and the second core die **20***b* are bonded to each other by die-to-wafer bonding, the second bonding pad **27***a* of the first die structure and the first bonding pad **23***b* of the second core die **20***b* may be bonded to each other by copper-copper hybrid bonding (Cu—Cu Hybrid Bonding).

[0170] As illustrated in FIG. **32**, the second surface **214***b* of the substrate **21***b* of the second core die **20***b* may be partially removed to expose one end portion of a through electrode **24***b*. Then, a gap filling layer may be formed on the first die structure to cover the second core dies **20***b*, and an upper portion of the gap filling layer may be removed to form a gap filling portion **30***b* that covers or surrounds an outer side surface of the second core die **20***b* and exposes an upper surface of the second core die **20***b*. Then, a backside insulating layer **26***b* having second bonding pads **27***b* in an outer surface thereof may be formed on the second surface **214***b* of the substrate **21***b*.

[0171] Thus, the second die structures each including a second core die **20***b* and the gap filling portion **30***b* covering or surrounding the outer side surface of the second core die **20***b* may be formed on the first die structures on the first carrier substrate C**1**. The second core dies **20***b* may be spaced apart from each other at the wafer level on the first die structures. The second core dies **20***b* may be arranged on the first die structures on the first carrier substrate C**1** such that the first surface **212***b* of the substrate **21***b* of each of the second core dies **20***b* faces the first carrier substrate C**1**. Each of the second core dies **20***b* may include the substrate **21***b*, the front insulating layer **22***b*, and the backside insulating layer **26***b*. The gap filling portion **30***b* may cover or surround the outer side surfaces of the substrate **21***b* and the front insulating layer **22***b* of the second core die **20***b*. The backside insulating layer **26***b* may extend laterally from or along the second surface **214***b* of the substrate **21***b* to cover an upper surface of the gap fill portion **30***b*.

[0172] Referring to FIG. **33**, processes the same as or similar to the processes described with reference to FIGS. **31** and **32** may be performed to stack a third die structure on a second die structure on the first carrier substrate C**1**.

[0173] The third die structure including a third core die **20***c* and a gap filling portion **30***c* covering or surrounding an outer side surface of the third core die **20***c* may be formed

on the second die structure. The third core dies **20***c* may be spaced apart from each other at the wafer level on the second die structures. The third core dies **20***c* may be arranged on the second die structure such that a first surface **212***c* of a substrate **21***c* of the third core die **20***c* faces the first carrier substrate C**1**. Each of the third core dies **20***c* may include a substrate **21***c*, a front insulating layer **22***c*, and a backside insulating layer **26***c*. The gap filling portion **30***c* may cover or surround outer side surfaces of the substrate **21***c* and the front insulating layer **22***c* of the third core die **20***c*. The backside insulating layer **26***c* may extend laterally from or along a second surface **214***c* of the substrate **21***c* to cover an upper surface of the gap fill portion **30***c*.

[0174] The second bonding pad **27***b* of the second die structure and a first bonding pad **23***c* of the third core die **20***c* may make contact with each other. When the second die structure and the third core die **20***c* are bonded to each other by die-to-wafer bonding, the second bonding pad **27***b* of the second die structure and the first bonding pads **23***c* of the third core die **20***c* may be bonded to each other by copper-copper hybrid bonding (Cu—Cu Hybrid Bonding). A front surface of the third core die **20***c*, that is, the front insulating layer **22***c* on the first surface **212***c* of the substrate **21***c* may be directly bonded to the backside insulating layer **26***b* of the second die structure.

[0175] Referring to FIG. **34**, processes the same as or similar to the processes described with reference to FIG. **17** may be performed to cut the stacked first to third die structures along a cutting region, that is, a scribe lane region, by a first sawing process to form individual core die blocks CB**1** on the first carrier substrate C**1**.

[0176] Each of the core die blocks CB**1** may include first, second and third die structures DS**1**, DS**2** and DS**3** sequentially stacked. Each of the first, second and third die structures DS**1**, DS**2** and DS**3** may include a core die **20** and a gap filling portion **30** that covers or surrounds an outer side surface of the core die **20**. The core die block CB**1** may include first, second and third core dies **20***a*, **20***b* and **20***c*, collectively **20**, which are sequentially stacked, and first, second and third gap filling portions **30***a*, **30***b* and **30***c*, collectively **30** respectively covering or surrounding outer side surfaces of the first, second and third core dies **20***a*, **20***b* and **20***c*. In example embodiments, the core die block CB**1** may include the core dies **20***a*, **20***b*, and **20***c* stacked in three stages, but it will be understood that the present inventive concept is not limited thereto.

[0177] Then, processes the same as or similar to the processes described with reference to FIGS. **18** to **22** may be performed to sequentially stack first to fifth core die blocks CB**1**, CB**2**, CB**3**, CB**4**, and CB**5** and a top core die stack TD on a first wafer W**1** including buffer dies.

[0178] Then, processes the same as or similar to the processes described with reference to FIG. **23** may be performed to form a molding member **40** on the first wafer W**1** to at least partially fill gaps between the first, second, third, fourth and fifth core die blocks CB**1**, CB**2**, CB**3**, CB**4**, and CB**5**.

[0179] Then, portions of the first wafer W**1** and the molding member **40** may be cut along a cutting region SA, that is, a scribe lane region by a second sawing process to complete the semiconductor package **101** of FIG. **24**.

[0180] The semiconductor package may include semiconductor devices such as logic devices or memory devices. The semiconductor package may include logic devices such as central processing units (CPUs), main processing units (MPUs), or application processors (APs), or the like, and volatile memory devices such as DRAM devices, HBM devices, or non-volatile memory devices such as flash memory devices, PRAM devices, MRAM devices, ReRAM devices, or the like.

[0181] The foregoing is illustrative of example embodiments and is not to be construed as limiting thereof. Although a few example embodiments have been described, those skilled in the art will readily appreciate that many modifications are possible in example embodiments without materially departing from the novel teachings and advantages of the present inventive concept. Accordingly, all such modifications are intended to be included within the scope of example embodiments as defined in the claims.

What is claimed is:

1. A semiconductor package, comprising:
- a buffer die;
- a plurality of core die blocks sequentially stacked on the buffer die;
- a top core die on an uppermost core die block of the plurality of core die blocks; and
- a molding member surrounding outer side surfaces of the plurality of core die blocks and the top core die on the buffer die,
- wherein each of the core die blocks includes:
- a plurality of core dies sequentially stacked; and
- a plurality of gap filling portions surrounding outer side surfaces of at least two stages of core dies of the plurality of core dies, and
- wherein outer side surfaces of the plurality of gap filling portions of each of the plurality of core die blocks are coplanar.

2. The semiconductor package of claim **1**, wherein an outer side surface of a first core die block among the plurality of core die blocks and an outer side surface of a second core die block stacked on the first core die block are positioned on different planes respectively.

3. The semiconductor package of claim **1**, wherein each of the core dies includes:
- a substrate;
- a front insulating layer on a front surface of the substrate and having a first bonding pad therein; and
- a backside insulating layer on a backside surface of the substrate and having a second bonding pad therein.

4. The semiconductor package of claim **3**, wherein the backside insulating layer of a first core die among the plurality of core dies and the front insulating layer of a second core die stacked on the first core die are directly bonded to each other, and
- the second bonding pad of the first core die and the first bonding pad of the second core die are directly bonded to each other.

5. The semiconductor package of claim **3**, wherein each of the core dies further includes a through electrode that penetrates the substrate and is electrically connected to the first and second bonding pads.

6. The semiconductor package of claim **3**, wherein the gap filling portion surrounds outer side surfaces of the substrate and the front insulating layer.

7. The semiconductor package of claim **6**, wherein the backside insulating layer extends laterally along the backside surface of the substrate to cover an upper surface of the gap filling portion.

8. The semiconductor package of claim **1**, wherein each of the core dies has a thickness within a range of about 10 μm to 30 μm.

9. The semiconductor package of claim **1**, wherein the gap filling portion includes an inorganic dielectric or an organic dielectric.

10. The semiconductor package of claim **1**, wherein the molding member is in direct contact with an outer side surface of a first stage of core die of the plurality of core dies.

11. A semiconductor package, comprising:

a buffer die;

a plurality of core die blocks sequentially stacked on the buffer die, each of the plurality of core die blocks including a plurality of die structures that are sequentially stacked; and

a sealing member surrounding outer side surfaces of the plurality of core die blocks on the buffer die,

wherein each of the plurality of die structures includes:

a substrate;

a front insulating layer on a front surface of the substrate and including a first bonding pad therein;

a backside insulating layer on a backside surface of the substrate and including a second bonding pad therein; and

a gap filling portion surrounding outer side surfaces of the substrate and the front insulating layer.

12. The semiconductor package of claim **11**, wherein outer side surfaces of the gap filling portions of each of the core die blocks are coplanar.

13. The semiconductor package of claim **11**, wherein an outer side surface of a first core die block among the plurality of core die blocks and an outer side surface of a second core die block stacked on the first core die block are positioned on different planes.

14. The semiconductor package of claim **11**, wherein the backside insulating layer of a first die structure among the plurality of die structures and the front insulating layer of a second die structure stacked on the first die structure are directly bonded to each other, and

the second bonding pad of the first die structure and the first bonding pad of the second die structure are directly bonded to each other.

15. The semiconductor package of claim **11**, wherein each of the die structures further includes a through electrode that penetrates the substrate and is electrically connected to the first and second bonding pads.

16. The semiconductor package of claim **11**, wherein the backside insulating layer extends laterally along the backside surface of the substrate to cover an upper surface of the gap filling portion.

17. The semiconductor package of claim **11**, wherein the gap filling portion includes an inorganic dielectric or an organic dielectric.

18. The semiconductor package of claim **11**, wherein the sealing member includes a thermosetting resin.

19. The semiconductor package of claim **11**, wherein the sealing member is in direct contact with the gap filling portions.

20. A semiconductor package, comprising:

a buffer die;

a plurality of core die blocks sequentially stacked on the buffer die; and

a sealing member on outer side surfaces of the plurality of core die blocks on the buffer die,

wherein each of the plurality of core die blocks includes:

a plurality of core dies sequentially stacked; and

a plurality of gap filling portions on outer side surfaces of at least two stages of core dies of the plurality of core dies.

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