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PIXEL CIRCUIT, AND DISPLAY DEVICE

Abstract

The present disclosure provides a pixel circuit, and a display device. The pixel circuit includes a light-emitting element, a first resetting circuit, a control circuit and a driving circuit. The first resetting circuit writes a first initial voltage into a first node under the control of a first resetting control signal. The control circuit controls a control terminal of the driving circuit to be electrically connected to the first node under the control of a first control signal from the first control terminal, and controls the first node to be electrically connected to the first terminal of the driving circuit under the control of a second control signal from a second control terminal. A first terminal of the driving circuit is electrically connected to the light-emitting element, and the driving circuit is configured to drive the light-emitting element to emit light.

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATION [0001] This application is a continuation application of U.S. patent application Ser. No. 18/025,952 filed on Mar. 13, 2023, the U.S. patent Application is the U.S. national phase of PCT Application No. PCT/CN2022/095193 filed on May 26, 2022, disclosures of which are incorporated by reference herein in their entireties.

TECHNICAL FIELD
[0002] The present disclosure relates to the field of display technology, in particular to a pixel circuit, and a display device.
BACKGROUND
[0003] Recently, along with the development of intelligent display technologies, an organic light-emitting diode (OLED) has become one of the research hotspots in display devices. Due to the thinning of the display panel, the narrowing of the bezel and the development of low-frequency technologies of the display screen, it is difficult to realize the optimization design of the display panel.
[0004] In the related art, during the operation of a pixel circuit, the hysteresis phenomenon occurs severely, thereby to adversely affect the display effect.
SUMMARY
[0005] In a first aspect, the present disclosure provides in some embodiments a pixel circuit, including a light-emitting element, a first resetting circuit, a control circuit and a driving circuit. The first resetting circuit is electrically connected to a first resetting control terminal, a first initial voltage terminal and a first node, and configured to write a first initial voltage from the first initial voltage terminal into the first node under control of a first resetting control signal from the first resetting control terminal. The control circuit is electrically connected to a first control terminal, a second control terminal, the first node, a control terminal of the driving circuit and a first terminal of the driving circuit, and configured to control the control terminal of the driving circuit to be electrically connected to the first node under control of a first control signal from the first control terminal, and control the first node to be electrically connected to the first terminal of the driving circuit under control of a second control signal from the second control terminal. The first terminal of the driving circuit is electrically connected to the light-emitting element, and the driving circuit is configured to drive the light-emitting element to emit light.
[0006] Optionally, in at least one embodiment of the present disclosure, the pixel circuit further includes a second resetting circuit. The second resetting circuit is electrically connected to a second resetting control terminal, a second initial voltage terminal and the first node, and configured to write a second initialization voltage from the second initial voltage terminal into the first node under control of a second resetting control signal from the second resetting control terminal.
[0007] Optionally, in at least one embodiment of the present disclosure, the pixel circuit further includes an energy storage circuit, a data written-in circuit, a first light-emission control circuit and a second light-emission control circuit. A first terminal of the energy storage circuit is electrically connected to the control terminal of the driving circuit, a second terminal of the energy storage

circuit is electrically connected to a first voltage terminal, and the energy storage circuit is configured to store electric energy. The first light-emission control circuit is electrically connected to a light-emission control terminal, the first voltage terminal and a second terminal of the driving circuit, and configured to control the first voltage terminal to be electrically connected to the second terminal of the driving circuit under control of a light-emission control signal from the light-emission control terminal. The second light-emission control circuit is electrically connected to the light-emission control terminal, the first terminal of the driving circuit and a first electrode of the light-emitting element, and configured to control the first terminal of the driving circuit to be electrically connected to the first electrode of the light-emitting element under control of the light-emission control signal. The data written-in circuit is electrically connected to a written-in control terminal, a data line and the second terminal of the driving circuit, and configured to write a data voltage from the data line into the second terminal of the driving circuit under control of a written-in control signal from the written-in control terminal. A second electrode of the light-emitting element is electrically connected to a second voltage terminal.

[0008] Optionally, in at least one embodiment of the present disclosure, the pixel circuit further includes a third resetting circuit. The third resetting circuit is electrically connected to a third resetting control terminal, the first electrode of the light-emitting element and a third initial voltage terminal, and configured to write a third initial voltage from the third initial voltage terminal into the first electrode of the light-emitting element under control of a third resetting control signal from the third resetting control terminal.

[0009] Optionally, in at least one embodiment of the present disclosure, the first resetting circuit includes a first transistor, a control electrode of the first transistor is electrically connected to the first resetting control terminal, a first electrode of the first transistor is electrically connected to the first initial voltage terminal, and a second electrode of the first transistor is electrically connected to the first node.

[0010] Optionally, in at least one embodiment of the present disclosure, the control circuit includes a second transistor and a third transistor. A control electrode of the second transistor is electrically connected to the first control terminal, a first electrode of the second transistor is electrically connected to the first node, and a second electrode of the second transistor is electrically connected to the control terminal of the driving circuit. A control electrode of the third transistor is electrically connected to the second control terminal, a first electrode of the third transistor is electrically connected to the first node, and a second electrode of the third transistor is electrically connected to the first terminal of the driving circuit.

[0011] Optionally, in at least one embodiment of the present disclosure, the second resetting circuit includes a fourth transistor, a control electrode of the fourth transistor is electrically connected to the second resetting control terminal, a first electrode of the fourth transistor is electrically connected to the second initial voltage terminal, and a second electrode of the fourth transistor is electrically connected to the first node.

[0012] Optionally, in at least one embodiment of the present disclosure, the energy storage circuit includes a storage capacitor, the first light-emission control circuit includes a fifth transistor, the second light-emission control circuit includes a sixth transistor, the driving circuit includes a driving transistor, and the data written-in circuit includes a seventh transistor. A control electrode of the fifth transistor is electrically connected to the light-emission control terminal, a first electrode of the fifth transistor is electrically connected to the first voltage terminal, and a second electrode of the fifth transistor is electrically connected to the second terminal of the driving circuit. A control electrode of the sixth transistor is electrically connected to the light-emission control terminal, a first electrode of the sixth transistor is electrically connected to the first terminal of the driving circuit, and a second electrode of the sixth transistor is electrically connected to the first electrode of the light-emitting element. A control electrode of the seventh transistor is electrically connected to the written-in control terminal, a first electrode of the seventh transistor is electrically

connected to the data line, and a second electrode of the seventh transistor is electrically connected to the second terminal of the driving circuit. A first terminal of the storage capacitor is electrically connected to the control terminal of the driving circuit, and a second terminal of the storage capacitor is electrically connected to the first voltage terminal. A control electrode of the driving transistor is the control terminal of the driving circuit, a first electrode of the driving transistor is the first terminal of the driving circuit, and a second electrode of the driving transistor is the second terminal of the driving circuit.

[0013] Optionally, in at least one embodiment of the present disclosure, the third resetting circuit includes an eighth transistor, a control electrode of the eighth transistor is electrically connected to the third resetting control terminal, a first electrode of the eighth transistor is electrically connected to the third initial voltage terminal, and a second electrode of the eighth transistor is electrically connected to the first electrode of the light-emitting element.

[0014] In a second aspect, the present disclosure provides in some embodiments a method for driving the above-mentioned pixel circuit. A display period includes a first resetting stage and a second resetting stage arranged one after another, and the method includes: at the first resetting stage, writing, by the first resetting circuit, the first initial voltage from the first initial voltage terminal into the first node under control of the first resetting control signal, controlling, by the control circuit, the control terminal of the driving circuit to be electrically connected to the first node under control of the first control signal, and controlling, by the control circuit, the first node to be electrically connected to the first terminal of the driving circuit under control of the second control signal; at the second resetting stage, controlling, by the control circuit, the control terminal of the driving circuit to be electrically connected to the first node under control of the first control signal, and controlling, by the control circuit, the first node to be electrically connected to the first terminal of the driving circuit under control of the second control signal.

[0015] Optionally, in at least one embodiment of the present disclosure, the pixel circuit further includes a second resetting circuit, and the method further includes: at the second resetting stage, writing, by the second resetting circuit, a second initialization voltage from a second initial voltage terminal into the first node under control of a second resetting control signal.

[0016] Optionally, in at least one embodiment of the present disclosure, the pixel circuit further includes an energy storage circuit, a data written-in circuit, a first light-emission control circuit and a second light-emission control circuit, the display period further includes a charging stage and a first light-emission stage after the second resetting stage, and the method further includes: at the charging stage, writing, by the data written-in circuit, a data voltage from a data line into a second terminal of the driving circuit under control of a written-in control signal, controlling, by the control circuit, the control terminal of the driving circuit to be electrically connected to the first node under control of the first control signal, and controlling, by the control circuit, the first node to be electrically connected to the first terminal of the driving circuit under control of the second control signal; at the beginning of the charging stage, controlling, by the driving circuit, the first terminal of the driving circuit to be electrically connected to the second terminal of the driving circuit under control of a potential at the control terminal of the driving circuit, to charge the energy storage circuit via the data voltage, thereby to change the potential at the control terminal of the driving circuit until the first terminal of the driving circuit is electrically disconnected from the second terminal of the driving circuit; at the first light-emission stage, controlling, by the first light-emission control circuit, a first voltage terminal to be electrically connected to the second terminal of the driving circuit under control of a light-emission control signal, controlling, by the second light-emission control circuit, the first terminal of the driving circuit to be electrically connected to a first electrode of the light-emitting element under control of the light-emission control signal, and driving, by the driving circuit, the light-emitting element to emit light.

[0017] Optionally, in at least one embodiment of the present disclosure, the pixel circuit further includes a third resetting circuit, the display period further includes a third resetting stage between

the second resetting stage and the charging stage, and the method further includes: at the third resetting stage, writing, by the third resetting circuit, a third initial voltage from the third initial voltage terminal into the first electrode of the light-emitting element under control of a third resetting control signal.

[0018] Optionally, in at least one embodiment of the present disclosure, during low frequency display, a display period includes a refresh frame and a maintaining frame, the refresh frame is the display period, the maintaining frame includes a fourth resetting stage, a fifth resetting stage, a sixth resetting stage, a seventh resetting stage and a second light-emission stage arranged one after another, and the method further includes: in the maintaining frame, controlling, by the control circuit, the control terminal of the driving circuit to be electrically disconnected from the first node under control of the first control signal from the first control terminal; at the fourth resetting stage, writing, by the first resetting circuit, the first initial voltage from the first initial voltage terminal into the first node under control of the first resetting control signal, and controlling, by the control circuit, the first node to be electrically connected to the first terminal of the driving circuit under control of the second control signal, to write the first initial voltage into the first terminal of the driving circuit; at the fifth resetting stage, writing, by the second resetting circuit, the second initialization voltage from the second initial voltage terminal into the first node under control of the second resetting control signal, and controlling, by the control circuit, the first node to be electrically connected to the first terminal of the driving circuit under control of the second control signal, to write the second initialization voltage into the first terminal of the driving circuit; at the sixth resetting stage, writing, by the third resetting circuit, the third initial voltage from the third initial voltage terminal into the first electrode of the light-emitting element under control of the third resetting control signal; at the seventh resetting stage, writing, by the data written-in circuit, a voltage signal from the data line into the second terminal of the driving circuit under control of the written-in control signal; at the second light-emission stage, controlling, by the first light-emission control circuit, the first voltage terminal to be electrically connected to the second terminal of the driving circuit under control of the light-emission control signal, controlling, by the second light-emission control circuit, the first terminal of the driving circuit to be electrically connected to the first electrode of the light-emitting element under control of the light-emission control signal, and driving, by the driving circuit, the light-emitting element to emit light.

[0019] In a third aspect, the present disclosure further provides in some embodiments a display device including the above-mentioned pixel circuit.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] FIG. **1** is a schematic view showing a pixel circuit according to one embodiment of the present disclosure;

[0021] FIG. **2** is another schematic view showing the pixel circuit according to at least one embodiment of the present disclosure;

[0022] FIG. **3** is yet another schematic view showing the pixel circuit according to at least one embodiment of the present disclosure;

[0023] FIG. **4** is a still yet another schematic view showing the pixel circuit according to at least one embodiment of the present disclosure;

[0024] FIG. **5** is a circuit diagram of the pixel circuit according to at least one embodiment of the present disclosure;

[0025] FIG. **6** is a sequence diagram of the pixel circuit in FIG. **5**;

[0026] FIG. **7**A is a schematic view showing an operation state of the pixel circuit in FIG. **5** at a first resetting stage according to at least one embodiment of the present disclosure;

[0027] FIG. **7**B is a schematic view showing an operation state of the pixel circuit in FIG. **5** at a second resetting stage according to at least one embodiment of the present disclosure;
[0028] FIG. **7**C is a schematic view showing an operation state of the pixel circuit in FIG. **5** at a charging stage according to at least one embodiment of the present disclosure;
[0029] FIG. **7**D is a schematic view showing an operation state of the pixel circuit in FIG. **5** at a first light-emission stage according to at least one embodiment of the present disclosure; and
[0030] FIG. **8** is another sequence diagram of the pixel circuit in FIG. **5**.

DETAILED DESCRIPTION

[0031] In order to make the objects, the technical solutions and the advantages of the present disclosure more apparent, the present disclosure will be described hereinafter in a clear and complete manner in conjunction with the drawings and embodiments. Apparently, the following embodiments merely relate to a part of, rather than all of, the embodiments of the present disclosure, and based on these embodiments, a person skilled in the art may, without any creative effort, obtain the other embodiments, which also fall within the scope of the present disclosure.
[0032] In the embodiments of the present disclosure, each transistor maybe a triode, a thin film transistor (TFT), a field effect transistor (FET), or any other element having a same characteristic. In order to differentiate two electrodes other than a gate electrode from each other, one of the two electrodes is called as first electrode and the other is called as second electrode.
[0033] In actual use, when the transistor is a triode, the control electrode may be a base, the first electrode may be a collector and the second electrode may be an emitter, or the control electrode may be a base, the first electrode may be an emitter and the second electrode may be a collector.
[0034] In actual use, when the transistor is a TFT or FET, the control electrode may be a gate electrode, the first electrode may be a drain electrode and the second electrode may be a source electrode, or the control electrode may be a gate electrode, the first electrode may be a source electrode and the second electrode may be a drain electrode.
[0035] As shown in FIG. **1**, the present disclosure provides in some embodiments a pixel circuit including a light-emitting element **10**, a first resetting circuit **11**, a control circuit **12** and a driving circuit **13**.
[0036] The first resetting circuit **11** is electrically connected to a first resetting control terminal PR**1**, a first initial voltage terminal I**1** and a first node N**1**, and configured to write a first initial voltage Vi**1** from the first initial voltage terminal I**1** into the first node N**1** under control of a first resetting control signal from the first resetting control terminal PR**1**.
[0037] The control circuit **12** is electrically connected to a first control terminal NG**1**, a second control terminal NG**2**, the first node N**1**, a control terminal of the driving circuit **13** and a first terminal of the driving circuit **13**, and configured to control the control terminal of the driving circuit **13** to be electrically connected to the first node N**1** under control of a first control signal from the first control terminal NG**1**, and control the first node N**1** to be electrically connected to the first terminal of the driving circuit **13** under control of a second control signal from the second control terminal NG**2**.
[0038] The first terminal of the driving circuit **13** is electrically connected to the light-emitting element **10**, and the driving circuit **13** is configured to drive the light-emitting element **10** to emit light.
[0039] In at least one embodiment of the present disclosure, a voltage value of the first initial voltage Vi**1** may be, but not limited to, larger than or equal to 5V and smaller than or equal to 8V.
[0040] During the operation of the pixel circuit in at least one embodiment of the present disclosure, a display period includes a first resetting stage and a second resetting stage arranged one after another.
[0041] At the first resetting stage, the first resetting circuit **11** writes the first initial voltage Vi**1** from the first initial voltage terminal I**1** into the first node N**1** under the control of the first resetting control signal, the control circuit **12** controls the control terminal of the driving circuit **13** to be

electrically connected to the first node N**1** under the control of the first control signal, and the control circuit **12** controls the first node N**1** to be electrically connected to the first terminal of the driving circuit **13** under the control of the second control signal.

[0042] At the second resetting stage, the control circuit **12** controls the control terminal of the driving circuit **13** to be electrically connected to the first node N**1** under control of the first control signal, and the control circuit **12** controls the first node N**1** to be electrically connected to the first terminal of the driving circuit **13** under control of the second control signal.

[0043] According to the embodiments of the present disclosure, the pixel circuit includes the first resetting circuit **11** and the control circuit **12**, at the first resetting stage, the first resetting circuit **11** writes the first initial voltage Vi**1** into the first node N**1**, the control circuit **12** controls the control terminal of the driving circuit **13** to be electrically connected to the first node N**1**, and controls the first node N**1** to be electrically connected to the first terminal of the driving circuit **13**, so as to enable a potential at the control terminal of the driving circuit **13** and a potential at the first terminal of the driving circuit **13** to be the first initial voltage Vi**1**, thereby to apply a bias voltage to a driving transistor of the driving circuit **13**, enable the driving transistor of the driving circuit **13** to be in a bias state, mitigate a hysteresis phenomenon, and improve a display effect.

[0044] Due to the pixel circuit in the embodiments of the present disclosure, it is able mitigate a flicker phenomenon during low frequency display.

[0045] During the low-frequency display, the display period includes a refresh frame and a maintaining frame, during a partial time period of the maintaining frame, the driving transistor of the driving circuit **13** is biased and reset, and during the maintaining frame, a potential at a source electrode of the driving transistor and a potential at the drain electrode of the driving transistor of the driving circuit **13** are consistent with those in the refresh frame, so as to mitigate the flicker phenomenon.

[0046] In at least one embodiment of the present disclosure, the display period may be one frame during high frequency display, and the display period may be the refresh frame during the low frequency display.

[0047] As shown in FIG. **2**, on the basis of the pixel circuit in FIG. **1**, the pixel circuit further includes a second resetting circuit **21**.

[0048] The second resetting circuit **21** is electrically connected to a second resetting control terminal PG**1**, a second initial voltage terminal I**2** and the first node N**1**, and configured to write a second initialization voltage Vi**2** from the second initial voltage terminal I**2** into the first node N**1** under the control of a second resetting control signal from the second resetting control terminal PG**1**.

[0049] In at least one embodiment of the present disclosure, a voltage value of the second initial voltage Vi**2** may be, but not limited to, larger than or equal to −5V and smaller than or equal to −2V.

[0050] During the operation of the pixel circuit in FIG. **2**, at the second resetting stage, the second resetting circuit **21** writes the second initialization voltage Vi**2** from the second initial voltage terminal I**2** into the first node N**1** under the control of the second resetting control signal, so as to enable the driving transistor to be turned on at the beginning of the charging stage after the second resetting stage for threshold voltage compensation.

[0051] As shown in FIG. **3**, on the basis of the pixel circuit in FIG. **2**, the pixel circuit further includes an energy storage circuit **31**, a data written-in circuit **32**, a first light-emission control circuit **33** and a second light-emission control circuit **34**.

[0052] A first terminal of the energy storage circuit **31** is electrically connected to the control terminal of the driving circuit **13**, a second terminal of the energy storage circuit **31** is electrically connected to a first voltage terminal V**1**, and the energy storage circuit **31** is configured to store electric energy.

[0053] The light-emission control circuit **33** is electrically connected to a light-emission control

terminal E**1**, the first voltage terminal V**1** and a second terminal of the driving circuit **13**, and configured to control the first voltage terminal V**1** to be electrically connected to the second terminal of the driving circuit **13** under control of a light-emission control signal from the light-emission control terminal E**1**.

[0054] The second light-emission control circuit **34** is electrically connected to the light-emission control terminal E**1**, the first terminal of the driving circuit **13** and a first electrode of the light-emitting element **10**, and configured to control the first terminal of the driving circuit **13** to be electrically connected to the first electrode of the light-emitting element **10** under control of the light-emission control signal.

[0055] The data written-in circuit **32** is electrically connected to a written-in control terminal PG**2**, a data line D**1** and the second terminal of the driving circuit **13**, and configured to write a data voltage Vdata from the data line D**1** into the second terminal of the driving circuit **13** under control of a written-in control signal from the written-in control terminal PG**2**.

[0056] A second electrode of the light-emitting element **10** is electrically connected to a second voltage terminal V**2**.

[0057] In at least one embodiment of the present disclosure, the first voltage terminal V**1** may be, but not limited to, a high voltage terminal, and the second voltage terminal V**2** may be, but not limited to, a low voltage terminal.

[0058] During the operation of the pixel circuit in FIG. **3**, the display period further includes a charging stage and a first light-emission stage after the second resetting stage.

[0059] At the charging stage, the data written-in circuit **32** writes the data voltage Vdata from the data line D**1** into the second terminal of the driving circuit **13** under the control of the written-in control signal, the control circuit **12** controls the control terminal of the driving circuit **13** to be electrically connected to the first node N**1** under the control of the first control signal, the control circuit **12** controls the first node N**1** to be electrically connected to the first terminal of the driving circuit **13** under the control of the second control signal.

[0060] At the beginning of the charging stage, the driving circuit **13** controls the first terminal of the driving circuit **13** to be electrically connected to the second terminal of the driving circuit **13** under control of the potential at the control terminal of the driving circuit, so as to charge the energy storage circuit **31** via the data voltage Vdata, thereby to change the potential at the control terminal of the driving circuit **13** until the first terminal of the driving circuit **13** is electrically disconnected from the second terminal of the driving circuit **13**, and realize the threshold voltage compensation.

[0061] At the light-emission stage, the first light-emission control circuit **33** controls the first voltage terminal V**1** to be electrically connected to the second terminal of the driving circuit **13** under the control of the light-emission control signal, the second light-emission control circuit **34** controls the first terminal of the driving circuit **13** to be electrically connected to the first electrode of the light-emitting element **10** under control of the light-emission control signal, and the driving circuit **13** drives the light-emitting element **10** to emit light.

[0062] As shown in FIG. **4**, on the basis of the pixel circuit in FIG. **3**, the pixel circuit further includes a third resetting circuit **41**.

[0063] The third resetting circuit **41** is electrically connected to a third resetting control terminal PR**2** and the first electrode of the light-emitting element **10** and a third initial voltage terminal I**3**, and configured to write a third initial voltage Vi**3** from the third initial voltage terminal I**3** into the first electrode of the light-emitting element **10** under the control of a third resetting control signal from the third resetting control terminal PR**2**.

[0064] During the operation of the pixel circuit in FIG. **4**, the display period further includes a third resetting stage between the second resetting stage and the charging stage.

[0065] At the third resetting stage, the third resetting circuit **41** writes the third initial voltage Vi**3** from the third initial voltage terminal I**3** into the first electrode of the light-emitting element **10**

under control of the third resetting control signal, so as to control the light-emitting element **10** not to emit light, and release residual charges at the first electrode of the light-emitting element **10**.

[0066] In at least one embodiment of the present disclosure, a voltage value of the third initial voltage Vi**3** may be, but not limited to, larger than or equal to −5V and smaller than or equal to −2V.

[0067] During the operation of the pixel circuit in FIG. **4**, the display period includes the refresh frame and the maintaining frame during low frequency display, the refresh frame may be the display period, and the maintaining frame may include a fourth resetting stage, a fifth resetting stage, a sixth resetting stage, a seventh resetting stage and a second light-emission stage arranged one after another.

[0068] In the maintaining frame, the control circuit **12** controls the control terminal of the driving circuit **13** to be electrically disconnected from the first node N**1** under control of the first control signal from the first control terminal NG**1**.

[0069] At the fourth resetting stage, the first resetting circuit **11** writes the first initial voltage Vi**1** from the first initial voltage terminal I**1** into the first node N**1** under the control of the first resetting control signal. The control circuit **12** controls the first node N**1** to be electrically connected to the first terminal of the driving circuit **13** under the control of the second control signal, so as to write the first initial voltage Vi**1** into the first terminal of the driving circuit **13**, thereby to reset the potential at the first terminal of the driving circuit **13**.

[0070] At the fifth resetting stage, the second resetting circuit **21**, under the control of the second resetting control signal, writes the second initialization voltage Vi**2** from the second initial voltage terminal I**2** into the first node N**1**, and the control circuit I**2**, under the control of the second control signal, controls the first node N**1** to be electrically connected to the first terminal of the driving circuit **13**, so as to write the second initialization voltage Vi**2** into the first terminal of the driving circuit **13**.

[0071] At the sixth resetting stage, the third resetting circuit **41** writes the third initial voltage Vi**3** from the third initial voltage terminal I**3** into the first electrode of the light-emitting element **10** under the control of the third resetting control signal, so as to control the light-emitting element **10** not to emit light, and release residual charges at the first electrode of the light-emitting element **10**.

[0072] At the seventh resetting stage, the data written-in circuit **32** writes a voltage signal from the data line D**1** into the second terminal of the driving circuit **13** under control of the written-in control signal.

[0073] At the second light-emission stage, the first light-emission control circuit **33** controls the first voltage terminal V**1** to be electrically connected to the second terminal of the driving circuit **13** under the control of the light-emission control signal, the second light-emission control circuit **34** controls the first terminal of the driving circuit **13** to be connected to the first electrode of the light-emitting element **10** under control of the light-emission control signal, and the driving circuit **13** drives the light-emitting element **10** to emit light.

[0074] During the implementation, at the seventh resetting stage, the voltage signal from the data line D**1** may be a data voltage Vdata from the data line D**1** at the charging stage, and a voltage value of the data voltage Vdata may be, e.g., greater than or equal to 1V and less than or equal to 6.5V.

[0075] Alternatively, at the seventh resetting stage, the voltage signal from the data line D**1** may be a resetting voltage signal, and a voltage value of the resetting voltage signal may be greater than or equal to 4.6V and less than or equal to 7V. However, the present disclosure is not limited thereto.

[0076] During the operation of the pixel circuit in at least one embodiment of the present disclosure, at the seventh resetting stage, the data written-in circuit **32** writes the voltage signal from the data line D**1** into the second terminal of the driving circuit **13** under the control of the written-in control signal, so as to apply a bias voltage to the driving transistor of the driving circuit **13**, thereby to enable the driving transistor of the driving circuit **13** to be in a bias state, and

mitigate the hysteresis phenomenon.
[0077] In at least one embodiment of the present disclosure, when the pixel circuit is in low-frequency display, e.g., a refresh frequency is 1 Hz, the display period may include one refresh frame and maintaining frames after the refresh frame, and at the seventh resetting stage in each of the maintaining frames, the potential at the second terminal of the driving circuit **13** may be reset via the voltage signal from the data line D**1**, so as to mitigate the hysteresis phenomenon.
[0078] During the operation of the pixel circuit in FIG. **4**, at the fourth resetting stage, the driving circuit **13** controls the first terminal of the driving circuit **13** to be electrically connected to the second terminal of the driving circuit **13** under the control of the potential of the control terminal of the driving circuit **13**. However, the present disclosure is not limited thereto.
[0079] When the pixel circuit in FIG. **4** operates in low frequency display, in the maintaining frame, at the fourth resetting stage, the first initial voltage Vi**1** is written into the first terminal of the driving circuit **13**, so as to reset the potential at the first terminal of the driving circuit **13**. At the fifth reset stage, the second initialization voltage Vi**2** is written into the first terminal of the driving circuit **13**. At the seventh resetting stage, the voltage signal from the data line D**1** is written into the second terminal of the driving circuit **13**, so that the potential at the first terminal of the driving circuit **13** and the potential at the second terminal of the driving circuit **13** in the maintaining frame are consistent with those in the refresh frame, thereby to mitigate the flicker phenomenon.
[0080] Optionally, in at least one embodiment of the present disclosure, the first resetting circuit includes a first transistor, a control electrode of the first transistor is electrically connected to the first resetting control terminal, a first electrode of the first transistor is electrically connected to the first initial voltage terminal, and a second electrode of the first transistor is electrically connected to the first node.
[0081] Optionally, in at least one embodiment of the present disclosure, the control circuit includes a second transistor and a third transistor.
[0082] A control electrode of the second transistor is electrically connected to the first control terminal, a first electrode of the second transistor is electrically connected to the first node, and a second electrode of the second transistor is electrically connected to the control terminal of the driving circuit.
[0083] A control electrode of the third transistor is electrically connected to the second control terminal, a first electrode of the third transistor is electrically connected to the first node, and a second electrode of the third transistor is electrically connected to the first terminal of the driving circuit.
[0084] Optionally, in at least one embodiment of the present disclosure, the second resetting circuit includes a fourth transistor, a control electrode of the fourth transistor is electrically connected to the second resetting control terminal, a first electrode of the fourth transistor is electrically connected to the second initial voltage terminal, and a second electrode of the fourth transistor is electrically connected to the first node.
[0085] Optionally, in at least one embodiment of the present disclosure, the energy storage circuit includes a storage capacitor, the first light-emission control circuit includes a fifth transistor, the second light-emission control circuit includes a sixth transistor, the driving circuit includes a driving transistor, and the data written-in circuit includes a seventh transistor.
[0086] A control electrode of the fifth transistor is electrically connected to the light-emission control terminal, a first electrode of the fifth transistor is electrically connected to the first voltage terminal, and a second electrode of the fifth transistor is electrically connected to the second terminal of the driving circuit.
[0087] A control electrode of the sixth transistor is electrically connected to the light-emission control terminal, a first electrode of the sixth transistor is electrically connected to the first terminal of the driving circuit, and a second electrode of the sixth transistor is electrically connected to the first electrode of the light-emitting element.

[0088] A control electrode of the seventh transistor is electrically connected to the written-in control terminal, a first electrode of the seventh transistor is electrically connected to the data line, and a second electrode of the seventh transistor is electrically connected to the second terminal of the driving circuit.
[0089] A first terminal of the storage capacitor is electrically connected to the control terminal of the driving circuit, and a second terminal of the storage capacitor is electrically connected to the first voltage terminal.
[0090] A control electrode of the driving transistor is the control terminal of the driving circuit, a first electrode of the driving transistor is the first terminal of the driving circuit, and a second electrode of the driving transistor is the second terminal of the driving circuit.
[0091] Optionally, in at least one embodiment of the present disclosure, the third resetting circuit includes an eighth transistor, a control electrode of the eighth transistor is electrically connected to the third resetting control terminal, a first electrode of the eighth transistor is electrically connected to the third initial voltage terminal, and a second electrode of the eighth transistor is electrically connected to the first electrode of the light-emitting element.
[0092] As shown in FIG. **5**, on the basis of the pixel circuit in FIG. **4**, the first resetting circuit **11** includes a first transistor T**1**, the driving circuit **13** includes a driving transistor T**0**, and the light-emitting element is an organic light-emitting diode O**1**.
[0093] A gate electrode of the first transistor T**1** is electrically connected to the first resetting control terminal PR**1**, a source electrode of the first transistor T**1** is electrically connected to the first initial voltage terminal I**1**, and a drain electrode of the first transistor T**1** is electrically connected to the first node N**1**.
[0094] The control circuit I**2** includes a second transistor T**2** and a third transistor T**3**.
[0095] A gate electrode of the second transistor T**2** is electrically connected to the first control terminal NG**1**, a source electrode of the second transistor T**2** is electrically connected to the first node N**1**, and a drain electrode of the second transistor T**2** is electrically connected to the gate electrode of the driving transistor T**0**.
[0096] A gate electrode of the third transistor T**3** is electrically connected to the second control terminal NG**2**, a source electrode of the third transistor T**3** is electrically connected to the first node N**1**, and a drain electrode of the third transistor T**3** is electrically connected to the source electrode of the driving transistor T**0**.
[0097] The second resetting circuit **21** includes a fourth transistor T**4**, a gate electrode of the fourth transistor T**4** is electrically connected to the second resetting control terminal PG**1**, a source electrode of the fourth transistor T**4** is electrically connected to the second initial voltage end I**2**, and a drain electrode of the fourth transistor T**4** is electrically connected to the first node N**1**.
[0098] The energy storage circuit **31** includes a storage capacitor C**0**, the first light-emission control circuit **33** includes a fifth transistor T**5**, the second light-emission control circuit **34** includes a sixth transistor T**6**, and the data written-in circuit **32** includes a seventh transistor T**7**.
[0099] A gate electrode of the fifth transistor T**5** is electrically connected to the light-emission control terminal E**1**, a source electrode of the fifth transistor T**5** is electrically connected to the high voltage terminal VDD, and a drain electrode of the fifth transistor T**5** is electrically connected to the drain electrode of the driving transistor T**0**.
[0100] A gate electrode of the sixth transistor T**6** is electrically connected to the light-emission control terminal E**1**, a source electrode of the sixth transistor T**6** is electrically connected to the source electrode of the driving transistor T**0**, and a drain electrode of the sixth transistor T**6** is electrically connected to an anode of the organic light-emitting diode O**1**.
[0101] A gate electrode of the seventh transistor T**7** is electrically connected to the written-in control terminal PG**2**, a source electrode of the seventh transistor T**7** is electrically connected to the data line D**1**, and a drain electrode of the seventh transistor T**7** is electrically connected to the drain electrode of the driving transistor T**0**.

[0102] A first terminal of the storage capacitor C**0** is electrically connected to the gate electrode of the driving transistor T**0**, and a second terminal of the storage capacitor C**0** is electrically connected to the high voltage terminal VDD.
[0103] The third resetting circuit **41** includes an eighth transistor T**8**, a gate electrode of the eighth transistor T**8** is electrically connected to the third resetting control terminal PR**2**, a source electrode of the eighth transistor T**8** is electrically connected to the third initial voltage terminal I**3**, and a drain electrode of the eighth transistor T**8** is electrically connected to the anode of the organic light-emitting diode O**1**.
[0104] A cathode of the organic light-emitting diode O**1** is electrically connected to the low voltage terminal VSS.
[0105] In the pixel circuit in FIGS. **5**, T**2** and T**3** are, but not limited to, both n-type thin film transistors, and T**1**, T**4**, T**5**, T**6**, T**7**, T**8** and T**0** are, but not limited to, all p-type thin film transistors.
[0106] In the pixel circuit in FIG. **5**, T**2** and T**3** are, but not limited to, IGZO (indium gallium zinc oxide) TFTs (thin film transistors), and T**1**, T**4**, T**5**, T**6**, T**7**, T**8** and T**0** are, but not limited to, all LTPS (low temperature polysilicon) TFTs.
[0107] During the operation of the pixel circuit in FIG. **5**, it is able to mitigate the hysteresis phenomenon, and provide a good display effect in FFR (first frame response) and VRR (variable refresh rate) aspects.
[0108] As shown in FIG. **6**, during the operation of the pixel circuit in FIG. **5**, the display period may include a first resetting stage S**1**, a second resetting stage S**2**, a third resetting stage S**3**, a charging stage S**4** and a first light-emission stage S**5** arranged one after another.
[0109] At the first resetting stage S**1**, PR**1** provides a low voltage signal, PG**1** provides a high voltage signal, NG**1** provides a high voltage signal, NG**2** provides a high voltage signal, PR**2** provides a high voltage signal, PG**2** provides a high voltage signal, E**1** provides a high voltage signal, as shown in FIG. **7**A, T**1**, T**2** and T**3** are all turned on, and I**1** provides a first initial voltage Vi**1**, so as to write the first initial voltage Vi**1** into the gate electrode of T**0** and the drain electrode of T**0**, thereby to apply a bias voltage to T**0**, control T**0** to be in a bias state, and mitigate the hysteresis phenomenon. The first initial voltage Vi**1** is a positive voltage.
[0110] At the first resetting stage S**1**, T**4**, T**5**, T**6**, T**7**, T**8** and T**0** are all turned off.
[0111] At the second resetting stage S**2**, PR**1** provides a high voltage signal, PG**1** provides a low voltage signal, NG**1** provides a high voltage signal, NG**2** provides a high voltage signal, PR**2** provides a high voltage signal, PG**2** provides a high voltage signal, E**1** provides a high voltage signal, as shown in FIG. **7**B, T**4**, T**2** and T**3** are all turned on, and I**2** provides a second initial voltage Vi**2**, so as to write the second initial voltage Vi**2** into the gate electrode of T**3**, thereby to enable T**0** to be turned on at the beginning of the charging stage S**4**. The second initial voltage Vi**2** is written into the drain electrode of T**3**, so as to pull down the potential at the drain electrode of T**0**, thereby to provide a fast charging process at the charging stage through the data voltage Vdata (the second initial voltage Vi**2** is a negative voltage, and the data voltage Vdata is a negative voltage).
[0112] At the second resetting stage S**2**, T**1**, T**5**, T**6**, T**7**, T**8** and T**0** are all turned off.
[0113] At the third resetting stage S**3**, PR**1** provides a high voltage signal, PG**1** provides a high voltage signal, NG**1** provides a high voltage signal, NG**2** provides a high voltage signal, PR**2** provides a high voltage signal, PG**2** provides a high voltage signal, T**8** is turned on, and I**3** provides a third initial voltage Vi**3**, so as to write the third initial voltage Vi**3** into the anode of O**1**, thereby to control the O**1** not to emit light, and release residual charges at the anode of O**1**.
[0114] At the third resetting stage S**3**, T**1**, T**2**, T**3**, T**4**, T**5**, T**6**, T**7** and T**0** are all turned off.
[0115] At the charging stage S**4**, PR**1** provides a high voltage signal, PG**1** provides a high voltage signal, NG**1** provides a high voltage signal, NG**2** provides a high voltage signal, PR**2** provides a high voltage signal, PG**2** provides a low voltage signal, E**1** provides a high voltage signal, as shown in FIG. **7**C, T**7** is turned on, T**2** and T**3** are turned on, and D**1** provides a data voltage Vdata.

[0116] At the beginning of the charging stage S**4**, T**0** is turned on, so as to charge C**0** through the data voltage Vdata, thereby to pull up the potential at the gate electrode of T**0** until T**0** turns off, and at this time, the potential at the gate electrode of T**0** is Vdata+Vth, where Vth is a threshold voltage of T**0**.
[0117] At the charging stage S**4**, T**1**, T**4**, T**5**, T**6** and T**8** are all turned off.
[0118] At the first light-emission stage S**5**, PR**1** provides a high voltage signal, PG**1** provides a high voltage signal, NG**1** provides a low voltage signal, NG**2** provides a low voltage signal, PR**2** provides a high voltage signal, PG**2** provides a high voltage signal, E**1** provides a low voltage signal, as shown in FIG. **7**D, T**5**, T**6** and T**0** are all turned on, and T**0** drives O**1** to emit light.
[0119] At the first light-emission stage S**5**, T**1**, T**2**, T**3**, T**4**, T**7** and T**8** are all turned off.
[0120] During the operation of the pixel circuit in FIG. **5**, the display period includes the refresh frame and the maintaining frame in low frequency display, and the refresh frame may be the display period; as shown in FIG. **8**, the maintaining frame may include a fourth resetting stage S**6**, a fifth resetting stage S**7**, a sixth resetting stage S**8**, a seventh resetting stage S**9** and a second light-emission stage S**10** arranged one after another.
[0121] In the maintaining frame, NG**1** provides a low voltage signal, and T**2** is turned off to control the gate electrode of T**0** to be electrically disconnected from the first node N**1**, thereby to maintain the potential at the gate electrode of T**0**.
[0122] At the fourth resetting stage S**6**, PR**1** provides a low voltage signal, PG**1** provides a high voltage signal, NG**2** provides a high voltage signal, PR**2** provides a high voltage signal, PG**2** provides a high voltage signal, E**1** provides a high voltage signal, both T**1** and T**3** are turned on, and I**1** provides a first initial voltage Vi**1**, so as to write the first initial voltage Vi**1** into the drain electrode of T**0**. The first initial voltage Vi**1** is a positive voltage.
[0123] At the fourth resetting stage S**6**, T**4**, T**5**, T**6**, T**7** and T**8** are all turned off.
[0124] At the fifth resetting stage S**7**, PR**1** provides a high voltage signal, PG**1** provides a low voltage signal, NG**2** provides a high voltage signal, PR**2** provides a high voltage signal, PG**2** provides a high voltage signal, E**1** provides a high voltage signal, both T**4** and T**3** are turned on, I**2** provides a second initial voltage Vi**2**, so as to write the second initial voltage Vi**2** into the drain electrode of T**3**.
[0125] At the fifth resetting stage S**7**, T**1**, T**5**, T**6**, T**7**, T**8** and T**0** are all turned off.
[0126] At the sixth resetting stage S**8**, PR**1** provides a high voltage signal, PG**1** provides a high voltage signal, NG**2** provides a high voltage signal, PR**2** provides a low voltage signal, PG**2** provides a high voltage signal, E**1** provides a low voltage signal, T**8** is turned on, and I**3** provides a third initial voltage Vi**3**, so as to write the third initial voltage Vi**3** into the anode of O**1**, thereby to control the O**1** not to emit light, and release residual charges at the anode of O**1**.
[0127] At the sixth resetting stage S**8**, T**1**, T**2**, T**3**, T**4**, T**5**, T**6**, T**7** and T**0** are all turned off.
[0128] At the seventh resetting stage S**9**, PR**1** provides a high voltage signal, PG**1** provides a high voltage signal, NG**2** provides a high voltage signal, PR**2** provides a high voltage signal, PG**2** provides a low voltage signal, E**1** provides a high voltage signal, T**7** is turned on, T**3** is turned on, and D**1** provides a voltage signal, so as to write the voltage signal into the source electrode of T**0**.
[0129] At the seventh resetting stage S**9**, T**1**, T**4**, T**5**, T**6** and T**8** are all turned off.
[0130] At the second light-emission stage S**10**, PR**1** provides a high voltage signal, PG**1** provides a high voltage signal, NG**1** provides a low voltage signal, NG**2** provides a low voltage signal, PR**2** provides a high voltage signal, PG**2** provides a high voltage signal, E**1** provides a low voltage signal, T**5**, T**6** and T**0** are all turned on, and T**0** drives O**1** to emit light.
[0131] At the second light-emission stage S**10**, T**1**, T**2**, T**3**, T**4**, T**7** and T**8** are all turned off.
[0132] During the operation of the pixel circuit in FIG. **5**, at the fourth resetting stage S**6**, T**0** may be, but not limited to, turned on.
[0133] During the operation of the pixel circuit in FIG. **5**, at the seventh resetting stage, the voltage signal from the data line D**1** may be a data voltage Vdata, and a voltage value of the data voltage

Vdata may be, e.g., greater than or equal to 1V and less than or equal to 6.5 V.
[0134] Alternatively, at the seventh resetting stage, the voltage signal from the data line DI may be a resetting voltage signal, and a voltage value of the resetting voltage signal may be greater than or equal to 4.6V and less than or equal to 7 V. However, the present disclosure is not limited thereto.
[0135] During the operation of the pixel circuit in FIG. **5**, at the seventh resetting stage, T**7** is turned on to write the voltage signal from the data line D**1** into the second terminal of the driving circuit **13**, so as to apply a bias voltage to T**0**, thereby to enable T**0** to be in a bias state, and mitigate the hysteresis phenomenon.
[0136] The present disclosure provides in some embodiments a method for driving the above-mentioned pixel circuit. A display period includes a first resetting stage and a second resetting stage arranged one after another, and the method includes: at the first resetting stage, writing, by the first resetting circuit, the first initial voltage from the first initial voltage terminal into the first node under control of the first resetting control signal, controlling, by the control circuit, the control terminal of the driving circuit to be electrically connected to the first node under control of the first control signal, and controlling, by the control circuit, the first node to be electrically connected to the first terminal of the driving circuit under control of the second control signal; at the second resetting stage, controlling, by the control circuit, the control terminal of the driving circuit to be electrically connected to the first node under control of the first control signal, and controlling, by the control circuit, the first node to be electrically connected to the first terminal of the driving circuit under control of the second control signal.
[0137] In the method according to the embodiment of the present disclosure, at the first resetting stage, the first resetting circuit writes the first initial voltage into the first node, the control circuit controls the control terminal of the driving circuit to be electrically connected to the first node, and controls the first node to be electrically connected to the first terminal of the driving circuit, so as to enable the potential at the control terminal of the driving circuit and the potential at the first terminal of the driving circuit to be the first initial voltage, thereby to apply a bias voltage to the driving transistor of the driving circuit, enable the driving transistor of the driving circuit to be in a bias state, mitigate a hysteresis phenomenon, and improve a display effect.
[0138] In at least one embodiment of the present disclosure, the pixel circuit further includes a second resetting circuit, the method further includes: at the second resetting stage, writing, by the second resetting circuit, a second initialization voltage from a second initial voltage terminal into the first node under control of a second resetting control signal, so as to enable the driving transistor of the driving circuit to be turned on at the beginning of the charging stage.
[0139] In at least one embodiment of the present disclosure, the pixel circuit further includes an energy storage circuit, a data written-in circuit, a first light-emission control circuit and a second light-emission control circuit, the display period further includes a charging stage and a first light-emission stage after the second resetting stage, and the method further includes: at the charging stage, writing, by the data written-in circuit, a data voltage from a data line into a second terminal of the driving circuit under control of a written-in control signal, controlling, by the control circuit, the control terminal of the driving circuit to be electrically connected to the first node under control of the first control signal, and controlling, by the control circuit, the first node to be electrically connected to the first terminal of the driving circuit under control of the second control signal; at the beginning of the charging stage, controlling, by the driving circuit, the first terminal of the driving circuit to be electrically connected to the second terminal of the driving circuit under control of a potential at the control terminal of the driving circuit, to charge the energy storage circuit via the data voltage, thereby to change the potential at the control terminal of the driving circuit for threshold voltage compensation until the first terminal of the driving circuit is electrically disconnected from the second terminal of the driving circuit; at the first light-emission stage, controlling, by the first light-emission control circuit, a first voltage terminal to be electrically connected to the second terminal of the driving circuit under control of a light-emission

control signal, controlling, by the second light-emission control circuit, the first terminal of the driving circuit to be electrically connected to a first electrode of the light-emitting element under control of the light-emission control signal, and driving, by the driving circuit, the light-emitting element to emit light.

[0140] In at least one embodiment of the present disclosure, the pixel circuit further includes a third resetting circuit, the display period further includes a third resetting stage between the second resetting stage and the charging stage, and the method further includes: at the third resetting stage, writing, by the third resetting circuit, a third initial voltage from the third initial voltage terminal into the first electrode of the light-emitting element under control of a third resetting control signal, so as to control the light-emitting element not to emit light, and release residual charges at the first electrode of the light-emitting element.

[0141] In at least one embodiment of the present disclosure, during low frequency display, a display period includes a refresh frame and a maintaining frame, the refresh frame is the display period, the maintaining frame includes a fourth resetting stage, a fifth resetting stage, a sixth resetting stage, a seventh resetting stage and a second light-emission stage arranged one after another, and the method further includes: in the maintaining frame, controlling, by the control circuit, the control terminal of the driving circuit to be electrically disconnected from the first node under control of the first control signal from the first control terminal; at the fourth resetting stage, writing, by the first resetting circuit, the first initial voltage from the first initial voltage terminal into the first node under control of the first resetting control signal, and controlling, by the control circuit, the first node to be electrically connected to the first terminal of the driving circuit under control of the second control signal, to write the first initial voltage into the first terminal of the driving circuit; at the fifth resetting stage, writing, by the second resetting circuit, the second initialization voltage from the second initial voltage terminal into the first node under control of the second resetting control signal, and controlling, by the control circuit, the first node to be electrically connected to the first terminal of the driving circuit under control of the second control signal, to write the second initialization voltage into the first terminal of the driving circuit; at the sixth resetting stage, writing, by the third resetting circuit, the third initial voltage from the third initial voltage terminal into the first electrode of the light-emitting element under control of the third resetting control signal; at the seventh resetting stage, writing, by the data written-in circuit, a voltage signal from the data line into the second terminal of the driving circuit under control of the written-in control signal; at the second light-emission stage, controlling, by the first light-emission control circuit, the first voltage terminal to be electrically connected to the second terminal of the driving circuit under control of the light-emission control signal, controlling, by the second light-emission control circuit, the first terminal of the driving circuit to be electrically connected to the first electrode of the light-emitting element under control of the light-emission control signal, and driving, by the driving circuit, the light-emitting element to emit light.

[0142] The present disclosure further provides in some embodiments a display device including the above-mentioned pixel circuit.

[0143] The display device may be any product or member having a display function, e.g., mobile phone, tablet computer, television, display, laptop computer, digital photo frame, or navigator.

[0144] The above embodiments are for illustrative purposes only, but the present disclosure is not limited thereto. Apparently, a person skilled in the art may make further modifications and improvements without departing from the spirit of the present disclosure, and these modifications and improvements shall also fall within the scope of the present disclosure.

Claims

1. A pixel circuit, comprising a light-emitting element, a first resetting circuit, a control circuit and a driving circuit, wherein the first resetting circuit is electrically connected to a first resetting

control terminal, a first initial voltage terminal and a first node, and configured to write a first initial voltage from the first initial voltage terminal into the first node under control of a first resetting control signal from the first resetting control terminal; the control circuit is electrically connected to a first control terminal, a second control terminal, the first node, a control terminal of the driving circuit and a first terminal of the driving circuit, and configured to control the control terminal of the driving circuit to be electrically connected to the first node under control of a first control signal from the first control terminal, and control the first node to be electrically connected to the first terminal of the driving circuit under control of a second control signal from the second control terminal; the first terminal of the driving circuit is electrically connected to the light-emitting element, and the driving circuit is configured to drive the light-emitting element to emit light; wherein a voltage value of the first initial voltage is larger than or equal to 5V and smaller than or equal to 8V.

2. The pixel circuit according to claim 1, further comprising a second resetting circuit, wherein the second resetting circuit is electrically connected to a second resetting control terminal, a second initial voltage terminal and the first node, and configured to write a second initialization voltage from the second initial voltage terminal into the first node under control of a second resetting control signal from the second resetting control terminal; wherein a voltage value of the second initial voltage is larger than or equal to −5V and smaller than or equal to −2V.

3. The pixel circuit according to claim 1, further comprising an energy storage circuit, a data written-in circuit, a first light-emission control circuit and a second light-emission control circuit; wherein a first terminal of the energy storage circuit is electrically connected to the control terminal of the driving circuit, a second terminal of the energy storage circuit is electrically connected to a first voltage terminal, and the energy storage circuit is configured to store electric energy; the first light-emission control circuit is electrically connected to a light-emission control terminal, the first voltage terminal and a second terminal of the driving circuit, and configured to control the first voltage terminal to be electrically connected to the second terminal of the driving circuit under control of a light-emission control signal from the light-emission control terminal; the second light-emission control circuit is electrically connected to the light-emission control terminal, the first terminal of the driving circuit and a first electrode of the light-emitting element, and configured to control the first terminal of the driving circuit to be electrically connected to the first electrode of the light-emitting element under control of the light-emission control signal; the data written-in circuit is electrically connected to a written-in control terminal, a data line and the second terminal of the driving circuit, and configured to write a data voltage from the data line into the second terminal of the driving circuit under control of a written-in control signal from the written-in control terminal; a second electrode of the light-emitting element is electrically connected to a second voltage terminal.

4. The pixel circuit according to claim 3, further comprising a third resetting circuit, wherein the third resetting circuit is electrically connected to a third resetting control terminal, the first electrode of the light-emitting element and a third initial voltage terminal, and configured to write a third initial voltage from the third initial voltage terminal into the first electrode of the light-emitting element under control of a third resetting control signal from the third resetting control terminal; wherein a voltage value of the third initial voltage is larger than or equal to −5V and smaller than or equal to −2V.

5. The pixel circuit according to claim 1, wherein the first resetting circuit comprises a first transistor, a control electrode of the first transistor is electrically connected to the first resetting control terminal, a first electrode of the first transistor is electrically connected to the first initial voltage terminal, and a second electrode of the first transistor is electrically connected to the first node.

6. The pixel circuit according to claim 1, wherein the control circuit comprises a second transistor and a third transistor; a control electrode of the second transistor is electrically connected to the

first control terminal, a first electrode of the second transistor is electrically connected to the first node, and a second electrode of the second transistor is electrically connected to the control terminal of the driving circuit; a control electrode of the third transistor is electrically connected to the second control terminal, a first electrode of the third transistor is electrically connected to the first node, and a second electrode of the third transistor is electrically connected to the first terminal of the driving circuit.

7. The pixel circuit according to claim 2, wherein the second resetting circuit comprises a fourth transistor, a control electrode of the fourth transistor is electrically connected to the second resetting control terminal, a first electrode of the fourth transistor is electrically connected to the second initial voltage terminal, and a second electrode of the fourth transistor is electrically connected to the first node.

8. The pixel circuit according to claim 3, wherein the energy storage circuit comprises a storage capacitor, the first light-emission control circuit comprises a fifth transistor, the second light-emission control circuit comprises a sixth transistor, the driving circuit comprises a driving transistor, and the data written-in circuit comprises a seventh transistor; a control electrode of the fifth transistor is electrically connected to the light-emission control terminal, a first electrode of the fifth transistor is electrically connected to the first voltage terminal, and a second electrode of the fifth transistor is electrically connected to the second terminal of the driving circuit; a control electrode of the sixth transistor is electrically connected to the light-emission control terminal, a first electrode of the sixth transistor is electrically connected to the first terminal of the driving circuit, and a second electrode of the sixth transistor is electrically connected to the first electrode of the light-emitting element; a control electrode of the seventh transistor is electrically connected to the written-in control terminal, a first electrode of the seventh transistor is electrically connected to the data line, and a second electrode of the seventh transistor is electrically connected to the second terminal of the driving circuit; a first terminal of the storage capacitor is electrically connected to the control terminal of the driving circuit, and a second terminal of the storage capacitor is electrically connected to the first voltage terminal; a control electrode of the driving transistor is the control terminal of the driving circuit, a first electrode of the driving transistor is the first terminal of the driving circuit, and a second electrode of the driving transistor is the second terminal of the driving circuit.

9. The pixel circuit according to claim 4, wherein the third resetting circuit comprises an eighth transistor, a control electrode of the eighth transistor is electrically connected to the third resetting control terminal, a first electrode of the eighth transistor is electrically connected to the third initial voltage terminal, and a second electrode of the eighth transistor is electrically connected to the first electrode of the light-emitting element.

10. A display device comprising the pixel circuit according to claim 1.

11. The display device according to claim 10, further comprising a second resetting circuit, wherein the second resetting circuit is electrically connected to a second resetting control terminal, a second initial voltage terminal and the first node, and configured to write a second initialization voltage from the second initial voltage terminal into the first node under control of a second resetting control signal from the second resetting control terminal; wherein a voltage value of the second initial voltage is larger than or equal to −5V and smaller than or equal to −2V.

12. The display device according to claim 10, further comprising an energy storage circuit, a data written-in circuit, a first light-emission control circuit and a second light-emission control circuit; wherein a first terminal of the energy storage circuit is electrically connected to the control terminal of the driving circuit, a second terminal of the energy storage circuit is electrically connected to a first voltage terminal, and the energy storage circuit is configured to store electric energy; the first light-emission control circuit is electrically connected to a light-emission control terminal, the first voltage terminal and a second terminal of the driving circuit, and configured to control the first voltage terminal to be electrically connected to the second terminal of the driving circuit under

control of a light-emission control signal from the light-emission control terminal; the second light-emission control circuit is electrically connected to the light-emission control terminal, the first terminal of the driving circuit and a first electrode of the light-emitting element, and configured to control the first terminal of the driving circuit to be electrically connected to the first electrode of the light-emitting element under control of the light-emission control signal; the data written-in circuit is electrically connected to a written-in control terminal, a data line and the second terminal of the driving circuit, and configured to write a data voltage from the data line into the second terminal of the driving circuit under control of a written-in control signal from the written-in control terminal; a second electrode of the light-emitting element is electrically connected to a second voltage terminal.

13. The display device according to claim 12, further comprising a third resetting circuit, wherein the third resetting circuit is electrically connected to a third resetting control terminal, the first electrode of the light-emitting element and a third initial voltage terminal, and configured to write a third initial voltage from the third initial voltage terminal into the first electrode of the light-emitting element under control of a third resetting control signal from the third resetting control terminal; wherein a voltage value of the third initial voltage is larger than or equal to −5V and smaller than or equal to −2V.

14. The display device according to claim 10, wherein the first resetting circuit comprises a first transistor, a control electrode of the first transistor is electrically connected to the first resetting control terminal, a first electrode of the first transistor is electrically connected to the first initial voltage terminal, and a second electrode of the first transistor is electrically connected to the first node.

15. The display device according to claim 10, wherein the control circuit comprises a second transistor and a third transistor; a control electrode of the second transistor is electrically connected to the first control terminal, a first electrode of the second transistor is electrically connected to the first node, and a second electrode of the second transistor is electrically connected to the control terminal of the driving circuit; a control electrode of the third transistor is electrically connected to the second control terminal, a first electrode of the third transistor is electrically connected to the first node, and a second electrode of the third transistor is electrically connected to the first terminal of the driving circuit.

16. The display device according to claim 11, wherein the second resetting circuit comprises a fourth transistor, a control electrode of the fourth transistor is electrically connected to the second resetting control terminal, a first electrode of the fourth transistor is electrically connected to the second initial voltage terminal, and a second electrode of the fourth transistor is electrically connected to the first node.

17. The display device according to claim 12, wherein the energy storage circuit comprises a storage capacitor, the first light-emission control circuit comprises a fifth transistor, the second light-emission control circuit comprises a sixth transistor, the driving circuit comprises a driving transistor, and the data written-in circuit comprises a seventh transistor; a control electrode of the fifth transistor is electrically connected to the light-emission control terminal, a first electrode of the fifth transistor is electrically connected to the first voltage terminal, and a second electrode of the fifth transistor is electrically connected to the second terminal of the driving circuit; a control electrode of the sixth transistor is electrically connected to the light-emission control terminal, a first electrode of the sixth transistor is electrically connected to the first terminal of the driving circuit, and a second electrode of the sixth transistor is electrically connected to the first electrode of the light-emitting element; a control electrode of the seventh transistor is electrically connected to the written-in control terminal, a first electrode of the seventh transistor is electrically connected to the data line, and a second electrode of the seventh transistor is electrically connected to the second terminal of the driving circuit; a first terminal of the storage capacitor is electrically connected to the control terminal of the driving circuit, and a second terminal of the storage

capacitor is electrically connected to the first voltage terminal; a control electrode of the driving transistor is the control terminal of the driving circuit, a first electrode of the driving transistor is the first terminal of the driving circuit, and a second electrode of the driving transistor is the second terminal of the driving circuit.

18. The display device according to claim 13, wherein the third resetting circuit comprises an eighth transistor, a control electrode of the eighth transistor is electrically connected to the third resetting control terminal, a first electrode of the eighth transistor is electrically connected to the third initial voltage terminal, and a second electrode of the eighth transistor is electrically connected to the first electrode of the light-emitting element.