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DIGITAL FILTER CIRCUIT, DIGITAL FILTERING METHOD, AND STORAGE MEDIUM STORING DIGITAL FILTERING PROGRAM

Abstract

A digital filter circuit includes retrieve stream data as a digital signal, and cyclically operate a first phase and a second phase. The circuit includes a short-term storage unit configured to store a local state variable, a long-term storage unit configured to store a global state variable, a first phase synthesizing unit that outputs the digital signal in the first phase under an influence of the local state variable stored in the short-term storage unit, and a second phase synthesizing unit that outputs the digital signal in the second phase under an influence of the global state variable stored in the long-term storage unit, where an output from the first phase synthesizing unit and an output from the second phase synthesizing unit are caused to generate an interference due to a phase shift.

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Background/Summary

CROSS-REFERENCE TO THE RELATED APPLICATIONS [0001] This application is the national phase entry of International Application No. PCT/JP2023/034226, filed on Sep. 21, 2023, which is based upon and claims priority to Japanese Patent Application No. 2022-150133, filed on Sep. 21, 2022, the entire contents of which are incorporated herein by reference.

TECHNICAL FIELD
[0002] The present invention relates to a digital filter circuit, a digital filtering method, and a storage medium storing a digital filtering program.

BACKGROUND
[0003] Various digital filters have been developed to date.
[0004] For example, Japanese Examined Patent Application Publication No. H08-8464 discloses a digital filter in which a non-linear conversion unit is inserted into a feedback loop, whereby a distortion component attributed to the non-linear conversion unit is cumulatively generated so as to impart a harmonic component to a signal on the feedback loop, and music sound having rich sound quality can be generated like an analog filter.
[0005] Japanese Unexamined Patent Application Publication No. H10-190408 discloses a state-variable multimode digital filter in which a non-linear circuit having soft-limiter characteristics is inserted in an accumulator (an integrator) including an adder and a delay circuit configured to make a delay for one sample period, whereby the digital filter can impart appropriate distortion to an inputted signal without suddenly clipping the signal even when the adder exceeds an overflow limit.

Previous Technical Documents
Patent Documents
[0006] Patent Document 1: Japanese Examined Patent Application Publication No. H08-8464
[0007] Patent Document 2: Japanese Unexamined Patent Application Publication No. H10-190408

SUMMARY
The Problems to be Solved by the Present Invention
[0008] Here, the state-variable multimode digital filter with the non-linear circuit inserted in the accumulator (the integrator) as described above is focused on restriction of an oscillation level. This configuration achieves a very stable operation when oscillated, but exhibits quite poor emphasizing behaviors such as amplifying or sharpening an input signal.
[0009] The present invention has been made in view of the aforementioned problem of the related art. An object of the present invention is to provide a digital filter circuit, a digital filtering method, and a storage medium storing a digital filtering program, which enable a cyclic state-variable digital filter circuit to perform amplification or emphasis such as smoothening and sharpening of an input signal favorably (desirable response and characteristics).

Technical Solutions
[0010] The present invention has been made in view of the foregoing problem, and has an objective to provide a digital filter circuit. According to one aspect of the present invention, a digital filter circuit includes retrieve stream data as a digital signal, and cyclically operate a first phase and a second phase. The circuit includes a short-term storage unit configured to store a local state variable, a long-term storage unit configured to store a global state variable, a first phase synthesizing unit configured to output the digital signal in the first phase under an influence of the

local state variable stored in the short-term storage unit, and a second phase synthesizing unit configured to output the digital signal in the second phase under an influence of the global state variable stored in the long-term storage unit, wherein an output from the first phase synthesizing unit and an output from the second phase synthesizing unit are caused to generate an interference due to a phase shift.

[0011] According to another aspect of the present invention, the short-term storage unit stores, as the local state variable, data obtained by superposing charged states of respective cells constituting the digital filter circuit in a short term.

[0012] According to still another aspect of the present invention, the long-term storage unit stores, as the global state variable, data obtained by superposing the charged states of the respective cells constituting the digital filter circuit in a long term.

[0013] According to still another aspect of the present invention, the first phase synthesizing unit reaches firing and performs output when superposition of the digital signal and the local state variable exceeds a predetermined threshold in the first phase.

[0014] According to still another aspect of the present invention, the second phase synthesizing unit reaches firing and performs output when superposition of the digital signal and the global state variable exceeds a predetermined threshold in the second phase.

[0015] According to still another aspect of the present invention, the stream data is any of image data, sound data, heat data, chemical substance data, gravity data, pressure data, vibration data, magnetic wave data, electromagnetic wave data, radiation data, an attribute value pair, language data, and biological data.

[0016] According to still another aspect of the present invention, an interference pattern to be outputted from each of the first phase synthesizing unit and the second phase synthesizing unit is any of an image, a sound, a moving image, an actuator control signal, or a device control signal.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] FIG. **1** is a diagram showing a configuration of a digital filter according to a first embodiment of the present invention.

[0018] FIG. **2** is a diagram schematically showing a case where a matrix (such as a digital image signal) is inputted as an input digital signal from an external sensor to an element unit of a digital filter circuit and an interference pattern is outputted as an output matrix to an external action target.

[0019] FIGS. **3**A to **3**D are diagrams showing an example of mounting a digital filter circuit unit showing interactive relations among respective cells and processing in each time slit.

[0020] FIG. **4** is a diagram showing transition examples in time slits 1 to 8 in an input matrix inputted from the external sensor.

[0021] FIG. **5** is a diagram showing a brainwave-like waveform of time series display obtained by superposing charged states of respective cells in respective time slits.

[0022] FIG. **6**A is a diagram showing output examples outputted from the digital filter circuit of an embodiment of the present invention regarding 5×5 matrix data inputted from the external sensor, where FIG. **6**B shows the table at the lower right corner of FIG. **6**A.

[0023] FIG. **7** is a diagram showing waveform data reproduced from data corresponding to neural circuit data of the heart of a nematode.

[0024] FIG. **8** is a diagram showing fields of application of the digital filter circuit of the present invention.

[0025] FIG. **9** is a diagram showing a dataflow of present example.

[0026] FIG. **10** is a diagram showing a data structure of data used in L4t4 of the present example.

[0027] FIG. **11** is a diagram showing a data example of interaction rules and the like.

[0028] FIG. **12** is a diagram showing computational flows of respective pieces of data.

[0029] FIG. **13** is a diagram showing contents of respective applied data.

[0030] FIG. **14** is a diagram showing the contents of the applied data and examples of outputted data.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0031] An embodiment of the present invention will be described below with reference to the drawings.

[0032] FIG. **1** is a diagram showing a configuration of a digital filter according to a first embodiment of the present invention. This digital filter is a digital filter circuit that retrieves stream data as a digital signal, and cyclically operates a first phase and a second phase, which includes a first phase synthesizer **101** and a second phase synthesizer **102**. An output from the first phase synthesizer **101** and an output from the second phase synthesizer **102** are caused to generate an interference due to a phase shift. Moreover, the digital filter according to the present embodiment includes an adjuster **103**.

[0033] Among them, the first phase synthesizer **101** is a first phase synthesizing unit that outputs the digital signal in the first phase under the influence of a local state variable stored in a short-term storage unit. The short-term storage unit may be provided to the first phase synthesizer **101** itself or provided to a different constituent of the digital filter circuit. This short-term storage unit stores data obtained by superposing charged states of respective cells constituting the digital filter circuit in a short term as the local state variable. The first phase synthesizer **101** reaches firing and performs output when the superposition of the digital signal and the local state variable exceeds a predetermined threshold in the first phase.

[0034] The second phase synthesizer **102** is a second phase synthesizing unit that outputs the digital signal in the second phase under the influence of a global state variable stored in a long-term storage unit. The long-term storage unit may be provided to the second phase synthesizer **102** itself or provided to a different constituent of the digital filter circuit. This long-term storage unit stores data obtained by superposing the charged states of the respective cells constituting the digital filter circuit in a long term as the global state variable. The second phase synthesizer **102** reaches firing and performs output when the superposition of the digital signal and the local state variable exceeds a predetermined threshold in the second phase.

[0035] While an optional signal may be inputted herein, an example of stream data (also referred to as data stream) to be inputted is time-series data such as wave data. For instance, the stream data may be image data, sound data, heat data, chemical substance data, gravity data, pressure data, vibration data, magnetic wave data, electromagnetic wave data, radiation data, attribute value pairs, language data, or biological data. On the other hand, while an optional signal may be outputted in response to the inputted signal, an interference pattern to be outputted from each of the first phase synthesizer **101** and the second phase synthesizer **102** may be an image, a sound, a video, an actuator control signal, or a device control signal.

[0036] Furthermore, as a detailed example, the first phase synthesizer **101**, the second phase synthesizer **102**, and the adjuster **103** in the present embodiment are formed from cells (F**1** to F**6**, B**1**, B**2**, B**4**, B**6**, L**1**, and L**7**) as illustrated. Each cell simulates a biological cell. For example, a cell simulating a nerve cell reaches firing when the superposition of the digital signal on an input side connected like a synapse and the state variable representing the charged state exceeds a predetermined threshold, and carries out signal output to an output side connected like a synapse. Here, connection lines of the respective constituents (the first phase synthesizer **101**, the second phase synthesizer **102**, and the adjuster **103**) and the respective cells (F**1** to F**6**, B**1**, B**2**, B**4**, B**6**, L**1**, and L**7**) may be omitted in some cases in FIG. **1**, the respective constituents and/or the respective cells can be configured to be connectable with optional connection lines as needed.

[0037] The digital filter circuit according to the present embodiment is a semiconductor element unit devised based on the principle of operation of a biological neural circuit. As shown in FIG. **1**,

one unit of the digital filter circuit is formed from ten unique cells (F**1** to F**6**, B**1**, B**2**, B**4**, and B**6**) and two state retention cells (L**1** and L**7**). Here, an organ may be artificially formed by combining multiple units of the digital filter circuits of the same type, or an artificial neural network may be formed by coordinating different types of organs.

[0038] As shown in FIG. **1**, the element unit of the digital filter circuit is formed from the ten unique cells (F**1** to F**6**, B**1**, B**2**, B**4**, and B**6**) and the two state retention cells (L**1** and L**7**). The respective cells are referred to as F**3**, F**1**, F**2**, F**4**, F**5**, F**6**, B**1**, B**2**, B**4**, B**6**, L**1**, and L**7** as shown in FIG. **1**. This configuration is referred to as L4t4 (Layered Elements: 4feedforward and time sliced 4 feedback) model, which is an intelligence model formed from an assembly having seven layers (a number affixed to a name of each cell represents a number of the layer), and is configured such that four types of elements of four feedforward cells (F**3**, F**1**, F**2**, and F**4**) and four feedback cells (F**5**, B**1**, B**2**, and B**4**), respectively, are time-shared and operated synchronously with surrounding alignment cells (F**6** and B**6**). As will be described later, according to an apparatus, a method, a program, and a data structure implementing the L4t4 model, it is possible to obtain a simulation result which has been unavailable from the conventional artificial intelligence. Although not illustrated, a group of cells to detect an external change may further be provided on an input side and a group of external action target cells (such as an actuator device) may further be provided on an output side. These cells are cyclically operated synchronously and in coordination with one another. As an example, the external sensor digitalizes stream data from one or more external sources and retrieves the stream data into the external sensor. The group of external action target cells may carry out output such as display by rendering output (internal digital data) from the first phase synthesizer **101** (the cell F**4**) and the second phase synthesizer **102** (the cell B**4**) into the stream data (such as wave data), or work on a servo motor or an actuator corresponding to muscle fibers of a biological body with an output signal like robot control. Multiple element units are connected to constitute the digital filter circuit.

[0039] One operation cycle of each unit is divided into two phases. The cells F**3**, F**1**, F**2**, and F**4** constituting the first phase synthesizer **101** are mainly engaged in the first phase, and the cells F**5**, B**1**, B**2**, and B**4** constituting the second phase synthesizer **102** are mainly engaged in the second phase.

[0040] Among them, the cell L**1** is a cell that assumes a local memory. In the present embodiment, the cell L**1** is the short-term storage unit to perform short-term storage of the local state variables that make an impact on a reaction of the cell F**4**. Specifically, the cell L**1** stores the data obtained by superposing the charged states of the respective cells constituting the digital filter circuit in a short term as the local state variables.

[0041] The cell F**3** is a cell that assumes input. The cell F**3** accepts the input from the external sensor (the external source). When there is a connection target unit on the network, the cell F**3** can also receive superposed output from an internal unit.

[0042] The cell F**1** is a cell that assumes first phase intervention. The cell F**1** intervenes in signal transmission among the cells F**3**, F**2**, and F**4**.

[0043] The cell F**2** is a cell that assumes first phase synchronization. The cell F**2** mainly controls timing among the internal cells engaged in F**4** cell output in the first phase.

[0044] The cell F**4** is a cell that assumes the output in the first phase. The cell F**4** outputs a digital value obtained by the superposition of the inputted wave data depending on the state of the cell L**1**. Specifically, the cell F**4** of the first phase synthesizer **101** reaches firing and performs output in the case where the superposition of the digital signal transmitted through the cells F**3**, F**1**, and F**2** and the local state variable stored in the cell L**1** being the short-term storage unit exceeds a predetermined threshold in the first phase.

[0045] The cell F**6** is a cell that assumes in-clock. The cell F**6** receives the signal of the timing to start the first phase from the input (in) side connection unit.

[0046] The cell B**6** is a cell that assumes out-clock. The cell B**6** sends the signal of the start timing

to the connection unit on the output (out) side.

[0047] The cell F**5** is a cell that assumes pooling, which accumulates the values of the respective units in the F**4** cells. Specifically, the cell F**5** accumulates the values outputted from the cell F**4** of the connection units of the input (in) side.

[0048] The cell B**1** is a cell that assumes second phase intervention. The cell B**1** intervenes in signal transmission among the cells F**5**, B**2**, and B**4**.

[0049] The cell B**2** is a cell that assumes second phase synchronization. The cell B**2** mainly controls timing among the internal cells engaged in B**4** cell output in the second phase.

[0050] The cell B**4** is a cell that assumes the output in the second phase. The cell B**4** determines a digital value of its own unit and outputs and digital value in response to the values accumulated (aggregated) in the cell F**5** depending on the state of the cell L**7**. Specifically, the cell B**4** of the second phase synthesizer **102** reaches firing and performs output in the case where the superposition of the digital signal transmitted through the cells F**5**, B**2**, and B**1** and the global state variable stored in the cell L**7** being the long-term storage unit exceeds a predetermined threshold.

[0051] The cell L**7** is a cell that assumes the global memory. In the present embodiment, the cell L**7** is the long-term storage unit that stores the global state variables that make an impact on a reaction of the cell B**4**. Specifically, the cell L**7** stores the data obtained by superposing the charged states of the respective cells constituting the digital filter circuit in a long term as the global state variables.

[0052] Here, FIG. **2** is a diagram schematically showing a case where a matrix (such as a digital image signal) is inputted as an input digital signal from the external sensor to the element unit of the digital filter circuit and an interference pattern is outputted as an output matrix to an external action target.

[0053] As shown in FIG. **2**, the cells F**3**, F**1**, F**2**, and F**4** constituting the first phase synthesizer **101** carries out processing concerning the first phase. The cells F**5**, B**1**, B**2**, and B**4** constituting the second phase synthesizer **102** carries out processing concerning the second phase. This processing of the first phase and the second phase is carried out cyclically and repeatedly. The processing for one cycle to be executed by each cell is divided into ten sections. To be more precise, the processing is carried out in 64 time slits.

[0054] Here, FIGS. **3**A to **3**D are diagrams showing an example of mounting the digital filter circuit unit showing interactive relations among the respective cells and the processing in each time slit. This mounting example is merely an example and the present invention is not limited to this example. The present invention is not limited to this example, and the digital filter circuit can be mounted in various embodiments as long as the object and the operation and effects of the present invention are attained. An interaction rule table defines exchanges among the cells. A circuit diagram indicated by L4t4 is a diagram showing exchanges of signals. Types of connection signals are distinctively expressed in response to directions and the numbers of the signals. A connection line corresponding to a gap junction is indicated with a thick arrow and a connection line corresponding to a chemical junction is indicated with a thin arrow. A transmission side (solid) and a reception side (not solid) are distinguished by a difference of the terminal. There are three types of the signal types in response to the difference of the number of the signals. The signal having the number of the signal equal to one is issued as a reset signal, and the signals having the numbers of signals in a range from 2 to 12 is periodically issued as a synchronous trigger signal or a reset signal. The signal having the number of the signal equal to or above 12 is issued as a timer signal (a continuous pulse signal).

[0055] As described above, in the L4t4 mounting example being the mounting example of the present embodiment, the timing control is constructed from 68 time slits and 10 sections as a whole, and one section has a 7-time-slit width (however, a tenth section has a 5-time-slit width. The first phase corresponds to first to fifth sections, and the second phase corresponds to sixth to tenth sections. In this L4t4 digital filter circuit, there are three repressive cells F**6**, F**2**, and B**2**. These cells issue the reset signals and the synchronous signals in accordance with the designated

interaction rule table. Other excitatory cells transmit the pulse signal which is continuous between the cells to the cell on the other side. Depending on the intensity of the signal and the state of charges (a charged state) accumulated in a certain period, the synchronous signal serves as a trigger and the hyperpolarization and depolarization of the cells periodically occur. In the first section, the cycle (the first phase and the second phase) is initialized by processing the reset signal. In the second to fourth sections, a waveform that indicates the firing state of the cell F**4** is generated. In the sixth section, reset processing of the second phase is executed. In the seventh to ninth sections, a waveform mainly reflecting firing of the cell B**4** is generated.

[0056] As described above, in the first phase, the cell F**4** depends on the local state variable stored in the cell L**1**, and outputs the digital value obtained from the superposition of the input waveform data. In the second phase, the cell B**4** determines the digital value of its own unit and outputs and digital value in response to the values accumulated (aggregated) in the cell F**5** depending on the global state variable stored in the cell L**7**. Accordingly, the signals outputted from these two phases with a time difference interfere with each other due to a phase shift, and become an output matrix forming an interference pattern.

[0057] Accordingly, factors that the output values of this digital filter circuit unit depend on are the wave pattern of the input of the cell F**3**, the interference due to the phase shift between the cells F**4** and B**4**, changes in state values of the cells L**1** and L**7**, and changes in pooling values in the cell F**5**.

[0058] An example (a result of simulation) of the element unit of the digital filter circuit mounted as described above will be described below. FIG. **4** is a diagram showing transition examples in time slits 1 to 8 in an input matrix inputted from the external sensor. As shown in FIG. **4**, the input signal is inputted to the cell F**3** as time transient stream data (such as wave data).

[0059] FIG. **5** is a diagram showing a brainwave-like waveform of time series display obtained by superposing the charged states of the respective cells in the respective time slits. Each cell is either an excitatory cell or a repressive cell, and firing of an action potential is determined by whether or not a sum of the inputted excitatory/repressive signals reaches a predetermined value (the threshold).

[0060] FIG. **6**A is a diagram showing output examples outputted from the digital filter circuit of the present embodiment regarding 5×5 matrix data inputted from the external sensor. As shown in FIG. **6**A, an image of a change in external environment is successfully reproduced as an internal image. This indicates that the L4t4 circuit has a function of an autoencoder.

[0061] FIG. **7** is a diagram showing waveform data reproduced from data corresponding to neural circuit data of the heart of a nematode. As shown in FIG. **7**, it turns out that electrical signal of the heart can be reproduced from the neural circuit data of the heart of the nematode. Accordingly, it is possible to reproduce and output the electric signal in an artificial heart, for example. This represents that the digital filter circuit has a function that provides a function of the digital filter circuit that can perform emphasis by amplifying, smoothing, or sharpening the input signal appropriately in accordance with a heartbeat (desirable responses and characteristics).

[0062] FIG. **8** is a diagram showing fields of application of the digital filter circuit of the present invention. As shown in FIG. **8**, the present invention is applicable to various fields including a medical field, a field of nursing care, a field of agriculture, a field of transportation, a field of production, a field of disaster prevention and safety, a chemical field, and the like.

[0063] Now, data, programs and the like used in the above-described example will be explained. FIG. **9** is a diagram showing a dataflow of the present example. The stream data from the external sensor are assumed to be an n×m matrix and inputted as values of an element Sen(x, y). The external action target is outputted as a value of an element Out(x, y). Regarding an assembly of the L4t4 circuits, each element is referred to as changes in variables (e1, e2) of an element Cells(x, y, pre/post). A rule of an R2r type of the interaction rule table is referred to as a variable no of an element R2r(c1, c2, c3). A rule of an R2p type of the interaction rule table is referred to as a variable n0 of an element R2p(c1, c2, c3). The phase, the section, and the slit of the clock signal are

expressed by variables c1, c2, and c3, respectively. As for interaction application, an element R2rfunc(c1, c2) and an element R2pfunc(c1, c2) are applied. Here, a variable v1 and a variable v2 represent values of weights for firing determined at the timing of each slit. In the state transition management, a variable e11 or a variable e22 obtained by applying an element Syn(from1, c3, to1, c3+1) based on the variable v1 or the variable v2 for the interaction application is reflected to the element Cells.

[0064] FIG. **10** is a diagram showing a data structure of the data used in the L4t4 of the present example. FIG. **11** is a diagram showing a data example of the interaction rules and the like. As shown in FIG. **10**, an interaction rule table R2r is sequence data having a size of r1r×r2r(8×4), for example. A state transition management table Syn Times is sequence data having a size of (t1×t2)×(r1r+r1p)*2, for example. An interaction rule table r2p is sequence data having a size of r1p=11, r2p=19, for example. An external center matrix is formed from q0 pieces of s1×s2 (with a size n×m) sequence data. An L4t4 circuit matrix is sequence data having a size of is formed from x0×y0 (with a size n×m) sequence data, and k0=1 to 12 (corresponding to L**1** to L**7**), for example. A clock signal is sequence data of t2 slits×t1 time sections, for example. An external action target is formed from q0 pieces sequence data of a matrix s1×s2 (with a size n×m), for example.

[0065] FIG. **12** is a diagram showing computational flows of respective pieces of data. As shown in FIG. **12**, the interaction rule tables R2r and R2p are applied regarding an input matrix of values x and y, respectively, and this processing is repeatedly carried out for each time slit and each time section.

[0066] FIG. **13** is a diagram showing contents of respective applied data. FIG. **14** is a diagram showing the contents of the applied data and examples of outputted data. As a result of applying the interaction rule tables R2r and R2p as shown FIG. **13**, output Out shown in a graph was obtained in response to sensor input Sen as shown in FIG. **14**. In this way, the output of phase difference interaction by the L4t4 circuit has been confirmed. In addition, by cyclically changing the state variables, it is possible to amplify, smoothen, and sharpen an input signal into an output signal as intended. As an example, in a case where original data is acoustic wave data, the signal is more likely to be smoothened when a half a wavelength is shifted between the first phase and the second phase, and the signal is more likely to be amplified or sharpened when a wavelength is shifted. Accordingly, it is possible to set cyclic periods of the first phase and the second phase in accordance with a frequency and the like to be amplified or smoothened. By setting lengths of the long-term storage and the short-term storage with an attitude like a moving average regarding the wave, it is possible to adjust whether to react sensitively or to react roughly regarding a change in wave.

[0067] Here, it is needless to say that the digital filter circuit of the present invention can be formed by hardware. Instead, the digital filter circuit of the present invention may be realized by causing an MPU (a CPU) or a DSP of a computer and the like to execute a program for a filter. In addition, the digital filter circuit of the present invention is applicable not only to the above-described L4t4 but also to any digital filter as long as it is a filter that can perform phase different output between the first phase and the second phase.

Reference Numerals

[0068] **101** first phase synthesizer [0069] **102** second phase synthesizer [0070] **103** adjuster

Claims

1. A digital filter circuit configured to retrieve stream data as a digital signal, and to cyclically operate a first phase and a second phase, comprising: a short-term storage unit configured to store a local state variable; a long-term storage unit configured to store a global state variable; a first phase synthesizing unit configured to output the digital signal in the first phase under an influence of the local state variable stored in the short-term storage unit; and a second phase synthesizing unit

configured to output the digital signal in the second phase under an influence of the global state variable stored in the long-term storage unit, wherein an output from the first phase synthesizing unit and an output from the second phase synthesizing unit are caused to generate an interference due to a phase shift.

2. The digital filter circuit according to claim 1, wherein the short-term storage unit stores, as the local state variable, data obtained by superposing charged states of respective cells constituting the digital filter circuit in a short term.

3. The digital filter circuit according to claim 2, wherein the long-term storage unit stores, as the global state variable, data obtained by superposing the charged states of the respective cells constituting the digital filter circuit in a long term.

4. The digital filter circuit according to claim 1, wherein the first phase synthesizing unit reaches firing and performs output when superposition of the digital signal and the local state variable exceeds a predetermined threshold in the first phase.

5. The digital filter circuit according to claim 1, wherein the second phase synthesizing unit reaches firing and performs output when superposition of the digital signal and the global state variable exceeds a predetermined threshold in the second phase.

6. The digital filter circuit according to claim 1, wherein the stream data is any of image data, sound data, heat data, chemical substance data, gravity data, pressure data, vibration data, magnetic wave data, electromagnetic wave data, radiation data, an attribute value pair, language data, and biological data.

7. The digital filter circuit according to claim 1, wherein an interference pattern to be outputted from each of the first phase synthesizing unit and the second phase synthesizing unit is any of an image, a sound, a moving image, an actuator control signal, or a device control signal.

8. A digital filtering method to be executed by a digital filter circuit configured to retrieve stream data as a digital signal and to cyclically operate a first phase and a second phase, the digital filter circuit comprising a short-term storage unit configured to store a local state variable and a long-term storage unit configured to store a global state variable, the method comprising: outputting the digital signal in the first phase under an influence of the local state variable stored in the short-term storage unit, and outputting the digital signal in the second phase under an influence of the global state variable stored in the long-term storage unit wherein an output in the first phase and an output in the second phase are caused to generate an interference due to a phase shift by repeatedly executing the outputting in the first phase and the outputting in the second phase.

9. A computer-readable storage medium storing a digital filtering program to be executed by a digital filter circuit configured to retrieve stream data as a digital signal and to cyclically operate a first phase and a second phase, the digital filter circuit comprising a short-term storage unit configured to store a local state variable and a long-term storage unit configured to store a global state variable, the program causing the digital filter circuit to output the digital signal in the first phase under an influence of the local state variable stored in the short-term storage unit, and to output the digital signal in the second phase under an influence of the global state variable stored in the long-term storage unit, wherein an output in the first phase and an output in the second phase are caused to generate an interference due to a phase shift by repeatedly executing the outputting in the first phase and the outputting in the second phase.

10. The digital filter circuit according to claim 2, wherein the first phase synthesizing unit reaches firing and performs output when superposition of the digital signal and the local state variable exceeds a predetermined threshold in the first phase.

11. The digital filter circuit according to claim 3, wherein the first phase synthesizing unit reaches firing and performs output when superposition of the digital signal and the local state variable exceeds a predetermined threshold in the first phase.

12. The digital filter circuit according to claim 2, wherein the second phase synthesizing unit reaches firing and performs output when superposition of the digital signal and the global state

variable exceeds a predetermined threshold in the second phase.

13. The digital filter circuit according to claim 3, wherein the second phase synthesizing unit reaches firing and performs output when superposition of the digital signal and the global state variable exceeds a predetermined threshold in the second phase.

14. The digital filter circuit according to claim 2, wherein the stream data is any of image data, sound data, heat data, chemical substance data, gravity data, pressure data, vibration data, magnetic wave data, electromagnetic wave data, radiation data, an attribute value pair, language data, and biological data.

15. The digital filter circuit according to claim 3, wherein the stream data is any of image data, sound data, heat data, chemical substance data, gravity data, pressure data, vibration data, magnetic wave data, electromagnetic wave data, radiation data, an attribute value pair, language data, and biological data.

16. The digital filter circuit according to claim 2, wherein an interference pattern to be outputted from each of the first phase synthesizing unit and the second phase synthesizing unit is any of an image, a sound, a moving image, an actuator control signal, or a device control signal.

17. The digital filter circuit according to claim 3, wherein an interference pattern to be outputted from each of the first phase synthesizing unit and the second phase synthesizing unit is any of an image, a sound, a moving image, an actuator control signal, or a device control signal.