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SEMICONDUCTOR DEVICE WITH ESD PROTECTION

Abstract

An electro-static discharge (ESD) protection circuit includes a driver stack electrically connected between a first node that has a first reference voltage and a second node that has a second reference voltage. The ESD protection circuit further includes an input/output (I/O) pad electrically connected to the driver stack, wherein the driver stack is electrically between the I/O pad and each of the first node and the second node. The ESD protection circuit further includes a first ESD device electrically connected between the I/O pad and a third node that has a third reference voltage, wherein the I/O pad is electrically connected between the first ESD device and the driver stack.

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Background/Summary

PRIORITY CLAIM [0001] The present application is a continuation of U.S. patent application Ser. No. 17/735,095, filed May 2, 2022, now U.S. Pat. No. 12,300,692, issued May 13, 2025, which claims the priority of U.S. Provisional Application No. 63/266,226, filed Dec. 30, 2021, which are incorporated herein by reference in their entireties.

BACKGROUND
[0002] The semiconductor integrated circuit (IC) industry produces a variety of analog and digital devices to address issues in several different areas. Developments in semiconductor process technology nodes have progressively reduced component sizes and tightened spacing resulting in progressively increased transistor density. As a result, ICs have become progressively smaller.
[0003] In mobile electronic devices, a fail-safe input/output (I/O) architecture is configured to reduce system standby leakage power while protecting against electrostatic discharge (ESD). Ideally, in the event of failure, a fail safe device responds in a way that causes no harm, or at least a minimum of harm, to other devices.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0004] One or more embodiments are illustrated by way of example, and not by limitation, in the figures of the accompanying drawings, wherein elements having the same reference numeral designations represent like elements throughout. The drawings are not to scale, unless otherwise disclosed.
[0005] FIG. **1**A is a block diagram of an electro-static discharge (ESD) protection network, in accordance with some embodiments.
[0006] FIG. **1**B is a schematic diagram of an ESD protection network, in accordance with some embodiments.
[0007] FIG. **2**A is a block diagram of an ESD protection network, in accordance with some embodiments.
[0008] FIG. **2**B is a schematic diagram of a fail-safe I/O ESD circuit, in accordance with some embodiments.
[0009] FIG. **3** is a block diagram of an ESD protection network, in accordance with some embodiments.
[0010] FIG. **4** is a plot of curved line segments, in accordance with some embodiments.
[0011] FIG. **5** is a block diagram of an electronic design automation (EDA) system in accordance with some embodiments.
[0012] FIG. **6** is a block diagram of an integrated circuit (IC) manufacturing system, and an IC manufacturing flow associated therewith, in accordance with some embodiments.
[0013] FIG. **7** is a flow diagram of a method, in accordance with some embodiments.
DETAILED DESCRIPTION
[0014] The following disclosure provides many different embodiments, or examples, for implementing different features of the provided subject matter. Specific examples of elements and arrangements are described below to simplify the present disclosure. These are, of course,

examples and are not intended to be limiting. For example, the formation of a first feature over or on a second feature in the description that follows includes embodiments in which the first and second features are formed in direct contact and includes embodiments in which additional features are formed between the first and second features, such that the first and second features are unable to be in direct contact. In addition, the present disclosure repeats reference numerals and/or letters in the various examples. This repetition is for the purpose of simplicity and clarity and does not in itself dictate a relationship between the various embodiments and/or configurations discussed.

[0015] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “over,” “upper,” “on” and the like, are used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. The spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus is otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein are likewise interpreted accordingly.

[0016] As used herein, although terms such as “first,” “second” and “third” describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections are not limited by these terms. These terms are used to distinguish one element, component, region, layer, or section from another. Terms such as “first,” “second” and “third” in response to used herein do not imply a sequence or order unless clearly indicated by the context.

[0017] Notwithstanding that the numerical ranges and parameters setting forth the broad scope of the disclosure are approximations, the numerical values set forth in the specific examples are reported as precisely as possible. Any numerical value, however, inherently contains certain errors necessarily resulting from the standard deviation found in the respective testing measurements. Also, as used herein, the terms “substantially,” “approximately” and “about” generally mean within a value or range that is contemplated by people having ordinary skill in the art. Alternatively, the terms “substantially,” “approximately” and “about” mean within an acceptable standard error of the mean in response to considered by one of ordinary skill in the art. People having ordinary skill in the art understand that the acceptable standard error varies according to different technologies. Other than in the operating/working examples, or unless otherwise expressly specified, the numerical ranges, amounts, values, and percentages such as those for quantities of materials, durations of times, temperatures, operating conditions, ratios of amounts, and the likes thereof disclosed herein should be understood as modified in instances by the terms “substantially,” “approximately” or “about.” Accordingly, unless indicated to the contrary, the numerical parameters set forth in the present disclosure and attached claims are approximations that vary as desired. At the very least, each numerical parameter is construed considering the number of reported significant digits and by applying ordinary rounding techniques. Ranges are expressed herein as from one endpoint to another endpoint or between two endpoints. All ranges disclosed herein are inclusive of the endpoints, unless otherwise specified.

[0018] In some embodiments, an electro-static discharge (ESD) protection network for an input/output (I/O) pad includes a driver stack, a first ESD device and a power clamp. The driver stack has a serially-connected upper branch and a lower branch, the upper branch being electrically connected between a first node that has a first reference voltage (e.g., VDDPST) and the I/O pad, and the lower branch being electrically connected between the I/O pad and a second node that has a second reference voltage (e.g., VSS). The first ESD device (e.g., EUP device) is electrically connected between a first node and a third node that has a third reference voltage (e.g., VDDL). The power clamp is electrically connected between the third node and the second node. In some embodiments, the first ESD device includes a string of one or more, e.g., 2, diodes. In some embodiments, the ESD protection network further includes a second ESD device (e.g., EDN device) electrically connected between the I/O pad and the second node. In some embodiments, the second ESD device includes a string of one or more, e.g., 1, diodes. According to another approach, neither the first ESD device nor the second ESD device is provided, but instead a power clamp is provided between the first node and the second node as ESD protection. The power clamp according to the other approach uses gate tie-off drain-ballasting NMOS transistors. During normal operation, as contrasted with a fail safe mode for ESD-protection, the power clamp according to the other approach suffers/exhibits a substantial leakage current. By contrast, embodiments of the present application which include the first and second ESD devices exhibit smaller leakage current, and thus exhibit reduced power consumption, as compared to the power clamp according to the other approach.

[0019] Drain ballasting with larger poly-pitch according to the other approach is not process friendly in advanced process nodes such as nano-sheet processing. For example, the layout in drain ballasting transistors is different (i.e., has a larger poly-pitch) than those of neighboring transistors, and thus drain ballasting is problematic for advanced processes in which the poly-pitch is expected to be uniform for every transistor.

[0020] Snapback is a mechanism in a transistor in which avalanche breakdown or impact ionization provides a sufficient drain current to turn on the transistor. Snapback is used intentionally in the design of certain ESD protection devices integrated onto semiconductor chips. Snapback is also a parasitic failure mechanism which appears similar to latchup. Snapback is initiated by a small current from gate to drain. In the case of ESD protection devices, this current is caused by avalanche breakdown due to a sufficiently large voltage applied across the gate-drain junction. In the case of parasitic failures, the initiating current results from inadvertently turning on the transistor and a sufficiently large voltage across the gate and drain causing impact ionization, with some of the generated carriers then serving as the initiating current which flows into the drain. Once this initiating current flows into the drain, the transistor turns on and the gate voltage decreases to the snapback holding voltage. This voltage happens at the point where the processes of drain current generation and the transistor turning on are in balance: the gate-source current of the transistor decreases the drain voltage, which results in a lower electric field, which results in a smaller impact ionization or avalanche current and thus smaller base current, which weakens the action.

[0021] FIG. **1**A is a block diagram of an electro-static discharge (ESD) protection network **100**A, in accordance with some embodiments.

[0022] EDS protection network **100**A includes a fail-safe I/O ESD circuit **102**, an I/O unit **104**, a core logic circuit **106**, and a post-driver stack including a serially connected upper branch **110** and a lower branch **111**.

[0023] Core logic circuit **106** is powered by VDD at a node **152** and is between node **152** and ground **151**. In some embodiments, core logic circuit **106** is an integrated circuit (IC) that controls data transfer functions. In some embodiments, core logic circuit **106** is processing circuitry of a device or other suitable processing circuitry within the contemplated scope of the disclosure. Core logic circuit **106** receives input signals at pins **155** and/or **157** that are configured for first power domain according to a VDD reference voltage. Core logic circuit **106** routes the received signals to I/O unit **104**.

[0024] I/O unit **104** includes I/O circuitry **136** and a VDDST power clamp **134**. I/O circuitry **136** includes level shifters **138**, **140**, and **144**, high-side logic **142** and low-side logic **146**. Level shifters **138**, **140** and **144** are circuits configured to translate signals from one logic level or voltage domain to another, facilitating compatibility between integrated circuits with different voltage requirements, such as TTL and CMOS. In some embodiments, level shifters serve to bridge power domains between processors, logic, sensors, and other circuits. Level shifter **144** receives one or more signals from core logic **106** which are configured for the VDD-based power domain and shifts the same to have levels appropriate for a power domain based on a VDDL reference voltage and outputs the level-shifted signals to a low-side logic circuit **146**. Low-side logic circuit **146** is a circuit configured to operate in the VDDL-based power domain and to output signals to the post-driver stack. Each of level shifter **144** and low side logic circuit **146** is located between node **150** at/having VDDL and node **124** at/having VSS.

[0025] Level shifter **138** receives one or more signals from core logic device **106** which are configured for the VDD-based power domain, shifts the same to have levels appropriate for a power domain based on the VDDL reference voltage, and outputs the level-shifted signals to level shifter **140**. Level shifter **140** receives one or more signals from level shifter **138** which are configured for the VDDL-based power domain and shifts the same to have levels appropriate for a power domain based on VDD post-driver power (VDDPST) reference voltage. Level shifter **140** outputs the level-shifted signals to a high-side logic device **142**. High-side logic circuit **142** is a circuit configured to operate in the VDDPST-based power domain and to output signals to the post-driver stack. Each of level shifter **140** and high-side logic device **142** is located between node **126** at/having VDDPST and node **152** at/having VSSH (e.g., a high-side logic ground). In some embodiments, VSS and VSSH are the same, VSSH is zero volts, VSSH is ground, or VSSH is other suitable voltages within the contemplated scope of the disclosure.

[0026] Upper branch **110** of the post-driver stack includes PMOS transistors P**1** and P**2**. Lower branch **111** of the post-driver stack includes NMOS transistors N**1** and N**2**. PMOS transistors P**1** and P**2** are connected in series between node **126** at/having VDDPST and a node **117**. NMOS transistors N**1** and N**2** are connected in series between node **117** and node **124** at/having VSS. An I/O pad **116** is connected to node **117**. PMOS transistors P**1** and P**2** receive gate inputs from high-side logic device **142**. In response to the inputs from high-side logic device **142** being high, P**1** and P**2** will turn off. In response to the inputs from high-side logic device **142** being low, P**1** and P**2** will turn on. Transistor P**1** is located between node **126** at/having VDDPST and transistor P**2**. In response to the inputs from low-side logic device **146** being high, P**1** and P**2** will turn on. In response to the inputs from low-side logic device **146** being low, P**1** and P**2** will turn off. In some embodiments, the post-driver stack circuit is a stack of transistors (e.g., P**1**, P**2**, N**1**, and N**2**) used to control other circuits. In some embodiments, the post-driver stack circuit includes a different number of PMOS and/or a different number of NMOS transistors. In some embodiments, there is a resistor in series between node **117** and I/O pad **116**, e.g., for reliability and ESD concerns.

[0027] Fail-safe I/O ESD circuit **102** includes I/O pad **116**, an EUP device **112**, an EDN device **114** and a VDDL power clamp **128**. In some embodiments, EUP is an acronym for ESD discharge up, and EDN is an acronym for ESD discharge down. I/O pad **116** is electrically connected between node **117** and EUP device **112** and EDN device **114**. EUP device **112** is connected between I/O pad **116** and a node **122** at/having VDDL. EDN device **114** is connected between I/O pad **116** and node **124** at/having VSS. Each of EUP device **112** and EDN device **114** exhibits low leakage. In some embodiments, EUP device **112** includes a chain/string of diodes (see FIG. **1**B). In some embodiments, EUD device **112** includes one or more diodes (see FIG. **1**B).

[0028] VDDL power clamp **128** is connected between node **122** at/having VDDL and node **124** at/having VSS. VDDL power clamp **128** assists in protecting from ESD. VDDL power clamp **128** shunts ESD current (e.g., Iclamp **129**) not dissipated by EUP device **112** from the VDDL power rail, i.e., from node **122** at/having VDDL, to the VSS power rail, i.e., node **124** at/having VSS.

[0029] VDDPST power clamp **134** is connected between node **126** at/having VDDPST and node **124** at/having VSS. VDDPST power clamp **134** assists in protecting from an over-voltage circumstance. When a voltage on node **126** rises above VDDPST, VDDPST power clamp **134** shunts current from the VDDPST power rail, i.e., from node **126** at/having VDDPST, to the VSS power rail, i.e., node **124** at/having VSS.

[0030] During a fail-safe mode of operation VDDPST is powered down to zero volts (e.g., a standby mode), and VDDL is either powered on by a power management unit (PMU) (not shown) or left floating. Regardless, receipt of an ESD voltage on I/O pad **116** upwardly biases VDDL through EUP device **112**. In FIG. **1**A, assuming that the level of the ESD voltage is smaller than the breakdown voltage of EDN device **114**, current Istk_L **121** is substantially equal to the sum of currents Istk_U **118** and Iup **120** such that Istk_L≈Iskt_U+Iup.

[0031] In FIG. **1**A, when VDDL is powered up by the PMU, there is leakage associated with VDDL including leakage current Istk_L **121** through lower branch **111** of the post-driver stack, leakage current Iclamp **129** through VDDL power clamp **128**, leakage current Ipre **148** through low-side logic **146** and/or level shifter **144**, and leakage through VDDSPST power clamp **134**. In some embodiments, the value of VDDL is reduced by the PMU to reduce leakage when VDDL is powered on. In some embodiments, to avoid stress on other devices, the value of VDDL is set to be greater than or equal to the voltage on I/O pad **116**, namely VPAD, less the device operation voltage (e.g., voltage operation of fail-safe I/O ESD circuit **102**).

[0032] In response to an ESD voltage on I/O pad **116** (under the assumption that the level of the ESD voltage is smaller than the breakdown voltage of EDN device **114**), EUP device **112** conducts a current Iup **120** to node **122** which dissipates the ESD voltage so that the ESD voltage from I/O pad **116** is less than or equal to VDDL after passing through EUP device **112**. In some embodiments, also in response to an ESD voltage on I/O pad **116**, lower branch **111** of the post-driver stack also conducts a current Istk_L **121** through NMOS transistors N**1** and N**2**. Such current dissipation ensures that an ESD event does not send a high voltage from I/O pad **116** to node **122** substantially above VDDL.

[0033] Regarding FIG. **1**A, a method (in accordance with some embodiments) of protecting I/O circuitry includes: dissipating a voltage level of ESD on I/O pad **116**; and wherein the dissipating includes passing a first current from I/O pad **116** through EUP device **112** to node **122** which reduces the voltage level of the ESD to be at or below a reference voltage otherwise on node **122** but for the ESD. Such a method further includes: passing the first current through VDDL power clamp **128** to node **124**.

[0034] FIG. **1**B is a block diagram of an ESD protection network **100**B, in accordance with some embodiments.

[0035] FIG. **1**B is a version of FIG. **1**A. In particular, in some respects, FIG. **1**B is simplified with respect to FIG. **1**A in a sense that some of the components of FIG. **1**A are not reproduced in FIG. **1**B for purposes of simplifying illustration. In some respects, FIG. **1**B is more detailed than FIG. **1**A, e.g., see the discussion below of EUP device **112** and EDN device **114**. Reference numbers which are the same in each of FIGS. **1**B and **1**A correspondingly represent the same elements.

[0036] EDN device **114** includes a diode D1 **166**. EUP device **112** includes diodes DSA1 **160**, DSA2 **162**, . . . , DSAN **164**N. Diode D1 **166** is described as a reversed diode relative to a voltage across diode D1 **166** from I/O pad **116** to node **124** at/having VSS. A diode is a two-terminal electronic component that conducts current primarily in one direction (asymmetric conductance). A diode has low (ideally zero) resistance in one direction, and high (ideally infinite) resistance in the other. A semiconductor diode is a crystalline piece of semiconductor material with a p-n junction connected to two electrical terminals.

[0037] A p-n junction diode is made of semiconductor material, e.g., usually silicon, but germanium and gallium arsenide are also used as well as other suitable materials within the contemplated scope of the disclosure. Impurities are added to the diode to create a first region on one side that contains negative charge carriers (electrons), called an n-type semiconductor, and a second region on the other side that contains positive charge carriers (holes), called a p-type semiconductor. In response to the n-type and p-type materials being attached together, a momentary flow of electrons occurs from the N-side to the P-side resulting in a third region between the first and second regions where no charge carriers are present. This region is called the depletion region because there are no charge carriers (neither electrons nor holes). The diode's terminals are attached to the n-type and p-type regions. The boundary between these two regions is referred to as a p-n junction, and is responsible for the electrical behavior exhibited by a diode. Below a voltage referred to as the knee voltage or cut-in voltage, only little if any forward current is conducted by the diode. At the knee voltage, the diode starts to conduct significantly, exhibiting an exponential relationship voltage vs current. The knee voltage is equal to the barrier potential of the diode's p-n junction. In response to an electrical potential difference in which a voltage applied to the P-side (the anode A+) is higher than a voltage applied to the N-side (the cathode C−), and wherein the electrical potential difference is also equal to or greater than the knee voltage, the p-n junction allows electrons to flow through the depletion region from the N-type side to the P-type side. In response to the opposite electrical potential difference, in which the voltage applied to the P-side (the anode A+) is lower than the voltage applied to the N-side (the cathode C−) and the voltage difference is difference is less than the knee voltage, the p-n junction allows little if any electrons to flow in the opposite direction, creating, in a sense, an electrical check valve.

[0038] In EDN device **114**, diode D1 **166** is a reversed diode with the cathode connected to I/O pad **116** and the anode connected to node **124** at/having VSS.

[0039] EUP device **112** includes a string of N serially-connected diodes DSA1 **160**, DSA2 **162** through DSAN **164**, where N≥1, from I/O pad **116** to node **122** at/having VDDL. In EUP device **112**, regarding diode DSA1 **160**, the anode is connected to I/O pad **116** and the cathode is connected to the anode of diode DSA **162**. The cathode of diode DSA **162** is connected to the next diode (not shown) in the string of N diodes in EUP device **112**. The cathode of the penultimate diode (not shown) in the string of N diodes in EUP device **112** is connected the anode of diode **164**. The cathode of diode **164** is connected to the node **122** at/having VDDL. The cascaded diodes number (N) depends on a voltage difference Vδ1 between VPAD and VDDL. More particularly, N is directly proportional to Vδ1. As Vδ increases, so does N. In FIG. **1**B, each of the diodes DSA1 **160**, DSA2 **162** through DSAN **164** has substantially the same knee voltage, e.g., a reference voltage VK. The number N is an integer and is equal to or greater than one plus a floor function applied to a ratio of the difference A divided by VK such that

[00001] $1 + \left(\frac{}{\mathrm{VK}}\right) \leq N. \quad \mathrm{Eq.}\ (1)$

In FIG. **1**B, it is assumed that the diode D1 **166** has substantially the same knee voltage, e.g., a reference voltage VK. Relative to a reverse voltage across diode D1 **166** from I/O pad **116** to node **124** at/having VSS, a breakdown voltage of diode D1 **166**, VB_D1, is VB_D1≥VK*N.

[0040] FIG. **2**A is a block diagram of an ESD protection network **200**, in accordance with some embodiments.

[0041] In some embodiments, ESD protection network **200** is like ESD protection network **100**B of FIG. **1**B. FIG. **2**A uses 2-series numbering whereas FIG. **1**A uses 1-series numbering. In some embodiments, 2-series numbers in FIG. **2**A that correspond to 1-series numbers in FIG. **1**A indicate the same elements in FIG. **2**A as in FIG. **1**A.

[0042] EDS protection network **200** includes a fail-safe I/O ESD circuit **202**A, I/O circuitry **136** (not shown but see FIG. **1**A), a core logic circuit (not shown but see FIG. **1**A), and a post-driver stack. The post-driver stack includes an upper branch **210** and a lower branch **211**.

[0043] In FIG. **2**A, VDDPST power clamp **134** is removed as compared to FIG. **1**A, but ESD power to power discharge EP2P device **215** is included as compared to FIG. **1**A. In some embodiments, the term EP2P is an acronym for ESD power to power-discharge. EP2P device **215** is between node **226** at/having VDDPST and node **222** at/having VDDL. In FIG. **1**A, in some circumstances, VDDPST power clamp **134** has high leakage current, e.g., in an overdrive design (where the VDDPST operation voltage is larger than device voltage VDDL). The higher the voltage that can be clamped by VDDPST power clamp **134**, the higher the associated leakage current. EP2P device **215** takes over the ESD-protection role otherwise taken by VDDPST power clamp **134** but also exhibits low leakage current.

[0044] EP2P device **215** has low leakage current in both normal operation and fail-safe operation. During fail-safe operation, where VDDPST is powered down to zero volts by a power management unit (PMU) (not shown), VDDL is either powered on by the PMU or is left floating and biased by any voltage coming through EUP device **212**. VDDL leakage currents include leakage current Iup

220A from the post-stack driver and through EUP device **212**, leakage current Idn **220**B from the post-stack driver and through EDN device **214**, and VDDPST-to-VDDL leakage current IP2L **220**C). In some embodiments, to avoid stress on other devices, the value of VDDL is set to be greater than or equal to VPAD less than the device operation voltage (e.g., voltage operation of fail-safe I/O ESD circuit **202**A). In some embodiments, during a fail-safe event, EUP device **212** and EP2P device **215** reduce a value of the ESD voltage on I/O pad **216** so that the value of the ESD voltage is reduced/dissipated from VPAD to be less than or equal to VDDL after passing through EUP device **212** and EP2P device **215**. Current Idn **220**B is also dissipated through EDN device **214**. Such reduction/dissipation ensures that an ESD event does not send a high voltage from I/O pad **216** to node **222** which otherwise would raise the voltage on node **222** substantially above VDDL.

[0045] VDDL power clamp **228** of FIG. **2**A operates similarly to VDDL power clamp **128** of FIG. **1**A.

[0046] Regarding FIG. **2**A, a method (in accordance with some embodiments) of protecting I/O circuitry includes: dissipating a voltage level of a first ESD on I/O pad **216**; and dissipating a voltage level of a second ESD on a node **226**; and wherein the dissipating a voltage of a first ESD includes passing a first current from I/O pad **216** through EUP device **212** to node **122** which reduces the voltage level of the first ESD to be at or below a reference voltage otherwise on node **122** but for the first ESD; and the dissipating a voltage level of a second ESD includes passing a second current from node **226** through EP2P device **215** to node **122** which reduces the voltage level of the second ESD to be at or below the reference voltage otherwise on node **122** but for the second ESD. Such a method further includes: passing the first current or the second current through VDDL power clamp **128** to node **124**.

[0047] FIG. **2**B is a schematic diagram of a fail-safe I/O ESD circuit **202**B, in accordance with some embodiments.

[0048] FIG. **2**B is a version of FIG. **2**A. In particular, in some respects, FIG. **2**B is simplified with respect to FIG. **2**A in a sense that some of the components of FIG. **2**A are not reproduced in FIG. **2**B for purposes of simplifying illustration. In some respects, FIG. **1**B is more detailed than FIG. **1**A, e.g., see the discussion below of EUP device **112** and EDN device **114**.

[0049] EP2P device **215** includes a string of X serially-connected diodes DSB1 **270**, DSB2 **272**, . . . , through DSBX **274**, where X is an integer and X>1. The cascaded diodes number (X) depends on a voltage difference Vδ2 between VDDPST and VDDL. More particularly, X is directly proportional to Vδ2. As Vδ2 increases, so does X.

[0050] In FIG. **2**B, each of the diodes DSB1 **270**, DSB2 **272** through DSBX **274** has substantially the same knee voltage, e.g., a reference voltage VK. The number X is equal to or greater than one plus a floor function applied to a ratio of the difference Δ divided by VK such that

[00002] $1+\left(\frac{}{\mathrm{VK}}\right) \leq X.$ Eq. (2)

In FIG. **2**B, it is assumed that diode D1 **266** has substantially the same knee voltage, e.g., a reference voltage VK. Relative to a reverse voltage across diode D1 **266** from I/O pad **216** to node **224** at/having VSS, a breakdown voltage of diode D1 **266**, VB_D1, is VB_D1≥VK*N.

[0051] EUP device **212** includes diodes DSA1 **260**, DSA2 **262**, . . . , DSAN **264** and operates similarly to EUP device **112**, the latter including diodes DSA1 **160**, DSA2 **162**, . . . , DSAN **164**. EDN device **214** includes diode D1 **266** and operates similarly to EDN device **114**, the latter including diode D1 **166**. VDDL power clamp **228** operates similarly to VDDL power clamp **128**.

[0052] In some embodiments, and in comparison to other approaches, e.g., drain ballasting, fail-safe I/O ESD circuit **202**B has a benefit of reduced leakage current during a fail-safe operation.

[0053] In a non-limiting example in which the number N of diodes in EUP device **212** is N=1 and the number of diodes X in EP2P device **215** is X=1, and under voltage conditions in which VDDPST≈1.41*VDDL (e.g., VDDPST≈1.2 V and VDDL≈0.85 V), and under a temperature condition in which the temperature is low (e.g., ≈25° C.), at least some embodiments exhibit a reduction in leakage current of about 79.2% as compared to the other approach, e.g., drain ballasting.

[0054] In another non-limiting example in which the number N of diodes in EUP device **212** is N=1 and the number of diodes X in EP2P device **215** is X=1, and under voltage conditions in which VDDPST≈1.41*VDDL (e.g., VDDPST≈1.2 V and VDDL≈0.85 V), and under a temperature condition in which the temperature is high (e.g., ≈125° C.), at least some embodiments exhibit a reduction in leakage current of about 96.8% as compared to the other approach, e.g., drain ballasting.

[0055] In another non-limiting example in which the number N of diodes in EUP device **212** is N=2 and the number of diodes X in EP2P device **215** is X=1, and under voltage conditions in which VDDPST≈1.41*VDDL (e.g., VDDPST≈1.2 V and VDDL≈0.85 V), and under a temperature condition in which the temperature is low (e.g., ≈25° C.), at least some embodiments exhibit a reduction in leakage current of about 99.3% as compared to the other approach, e.g., drain ballasting.

[0056] In another non-limiting example in which the number N of diodes in EUP device **212** is N=2 and the number of diodes X in EP2P device **215** is X=1, and under voltage conditions in which VDDPST≈1.41*VDDL (e.g., VDDPST≈1.2 V and VDDL≈0.85 V), and under a temperature condition in which the temperature is high (e.g., ≈125° C.), at least some embodiments exhibit a reduction in leakage current of about 99.6% as compared to the other approach, e.g., drain ballasting.

[0057] In another non-limiting example in which the number N of diodes in EUP device **212** is N=2 and the number of diodes X in EP2P device **215** is X=1, and under voltage conditions in which VDDPST≈1.56*VDDL (e.g., VDDPST≈1.26 V and VDDL≈0.8075 V), and under a temperature condition in which the temperature is low (e.g., ≈25° C.), at least some embodiments exhibit a reduction in leakage current of about 97.9% as compared to the other approach, e.g., drain ballasting.

[0058] In another non-limiting example in which the number N of diodes in EUP device **212** is N=1 and the number of diodes X in EP2P device **215** is X=1, and under voltage conditions in which VDDPST≈1.56*VDDL (e.g., VDDPST≈1.26 V and VDDL≈0.8075 V), and under a temperature condition in which the temperature is high (e.g., ≈125° C.), at least some embodiments exhibit a reduction in leakage current of about 76.3% as compared to the other approach, e.g., drain ballasting.

[0059] In another non-limiting example in which the number N of diodes in EUP device **212** is N=2 and the number of diodes X in EP2P device **215** is X=1, and under voltage conditions in which VDDPST≈1.56*VDDL (e.g., VDDPST≈1.26 V and VDDL≈0.8075 V), and under a temperature condition in which the temperature is low (e.g., ≈125° C.), at least some embodiments exhibit a reduction in leakage current of about 99.1% as compared to the other approach, e.g., drain ballasting.

[0060] In another non-limiting example in which the number N of diodes in EUP device **212** is N=2 and the number of diodes X in EP2P device **215** is X=1, and under voltage conditions in which VDDPST≈1.73*VDDL (e.g., VDDPST≈1.32 V and VDDL≈0.765 V), and under a temperature condition in which the temperature is low (e.g., ≈25° C.), at least some embodiments exhibit a reduction in leakage current of about 93.9% as compared to the other approach, e.g., drain ballasting.

[0061] In another non-limiting example in which the number N of diodes in EUP device **212** is N=2 and the number of diodes X in EP2P device **215** is X=1, and under voltage conditions in which VDDPST≈1.73*VDDL (e.g., VDDPST≈1.32 V and VDDL≈0.765 V), and under a temperature condition in which the temperature is low (e.g., ≈125° C.), at least some embodiments exhibit a reduction in leakage current of about 97.8% as compared to the other approach, e.g., drain

ballasting.
[0062] FIG. **3** is a block diagram of an ESD protection network **300**, in accordance with some embodiments.
[0063] In some embodiments, ESD protection network **300** is like ESD protection network **200** of FIG. **2**A, i.e., FIG. **3** is a version of FIG. **2**A. In particular, FIG. **3** includes fewer components than
[0064] FIG. **2**A. FIG. **3** uses 3-series numbering whereas FIG. **2**A uses 2-series numbering. In some embodiments, 3-series numbers in FIG. **3** that correspond to 2-series numbers in FIG. **2**A indicate the same elements in FIG. **3** as in FIG. **2**A.
[0065] EDS protection network **300** includes a fail-safe I/O ESD circuit **302**, I/O circuitry (not shown but sec FIG. **1**A), a core logic circuit (not shown but see FIG. **1**A), and a post-driver stack, where the post-stack driver includes upper branch **210** and lower branch **211**.
[0066] In FIG. **3**, EUP **212** and EDN **214** are removed as compared to FIG. **2**A, but ESD power to power discharge (EP2P) device **315** is included in between node **226** at/having VDDPST and node **222** at/having VDDL. EP2P device **315** configured, and operates, similarly with respect to EP2P device **215** of FIGS. **2**A-**2**B.
[0067] EP2P device **315** has low current leakage in both normal operation and fail-safe operation. During fail-safe operation, where VDDPST is powered down to zero volts by the PMU (not shown), VDDL is either powered on by a power management unit (PMU) or left floating.
[0068] During fail-safe operation, EP2P device **315** and VDDL power clamp **228** shunt excess voltage to ground through power rail VDDL. During normal operation, EP2P device **315** exhibits a leakage current IP2L **220**D. Nevertheless, leakage current IP2L **220**D is smaller than a leakage current of another approach which does not use EP2P device **315** but instead uses only a power clamp similar to VDDPST power claim **134** of FIG. **1**A.
[0069] In a non-limiting example in which the number of diodes X in EP2P device **315** is where X=1, and under voltage conditions in which VDDPST≈1.41*VDDL (e.g., VDDPST≈1.2 V and VDDL≈0.85 V), and under a temperature condition in which the temperature ≈25° C.), at least some embodiments exhibit a reduction in leakage current of about 98.2% as compared to the other approach.
[0070] In a non-limiting example in which the number of diodes X in EP2P device **315** is where X=1, and under voltage conditions in which VDDPST≈1.41*VDDL (e.g., VDDPST≈1.2 V and VDDL≈0.85 V), and under a temperature condition in which the temperature ≈40° C.), at least some embodiments exhibit a reduction in leakage current of about 97.9% as compared to the other approach.
[0071] In a non-limiting example in which the number of diodes X in EP2P device **315** is where X=1, and under voltage conditions in which VDDPST≈1.41*VDDL (e.g., VDDPST≈1.2 V and VDDL≈0.85 V), and under a temperature condition in which the temperature ≈85° C.), at least some embodiments exhibit a reduction in leakage current of about 98.1% as compared to the other approach.
[0072] In a non-limiting example in which the number of diodes X in EP2P device **315** is where X=1, and under voltage conditions in which VDDPST≈1.41*VDDL (e.g., VDDPST≈1.2 V and VDDL≈0.85 V), and under a temperature condition in which the temperature ≈125° C.), at least some embodiments exhibit a reduction in leakage current of about 98.8% as compared to the other approach.
[0073] Regarding FIG. **3**, a method (in accordance with some embodiments) of protecting I/O circuitry includes: dissipating a voltage level of a first ESD on a node **226**; and wherein the dissipating a voltage level of a first ESD includes passing a first current from node **226** through EP2P device **215** to node **122** which reduces the voltage level of the first ESD voltage to be at or below a reference voltage otherwise on node **122**. Such a method further includes: passing the first current through VDDL power clamp **128** to node **124**.
[0074] FIGS. **4** is a plot **400** of curved line segments, in accordance with some embodiments.

[0075] Plot **400** relates voltage VDDL (in units of volts) on the X-axis to leakage power (in units of watts) on the Y-axis. Plot **400** includes curves **402**, **404**, **406** and **408**.
[0076] Curve **404** represents the product of the current of a VDDL power clamp (ICLMP, e.g., Iclamp **129**) and voltage VDDL. Accordingly, curve **404** is labeled PCLMP, and wherein PCLMP=ICLMP*VDDL. Curve **406** represents the product of the current of a level shifter (IPRE_DRVR, e.g., Ipre **148**) and voltage VDDL. Accordingly, curve **406** is labeled PPRE, and wherein PPRE=IPRE_DRVR*VDDL. Curve **408** represents the product of the current at the I/O pad (IPD, e.g., Istk_L **121**) and the voltage (VPAD) at the I/O pad (e.g., I/O pad **116**). Accordingly, curve **408** is labeled PPAD, and wherein PPAD=IPD*VPAD. Curve **402** represents the sum of curves **404**, **406**, and **408**. Accordingly, curve **402** is labeled as PTOTL.
[0077] Curves **404** and **406** have positive slopes whereas curve **408** has a negative slope. As a result, curve **402** has an open, upward shape. The lowest point of curve **402** represents a minimum value of power LP**412** dissipated to leakage current in an ESD protection network such as ESD protection network **100**A, or the like. The value of VDDL corresponding to LP**412** is V**410**. In some embodiments, setting VDDL to V**410** reduces, if not minimizes, leakage current in an ESD protection network such as ESD protection network **100**A, or the like.
[0078] Regarding FIG. **4**, a method (in accordance with some embodiments) of configuring an ESD protection network such as ESD protection network **100**A, or the like, to reduce (if not minimize) leakage current includes: plotting a curve **402** which is the sum of curves **404**, **406** and **408**; determining a minimum value of leakage power on curve **402**; extracting the value of VDDL that corresponds to the minimum value of curve **402**; and setting that value of VDDL in the ESD protection network equal to the value of the value of VDDL that corresponds to the minimum value of curve **402**. Next, before discussing FIGS. **5-6**, discussion turns to FIG. **7**.
[0079] FIG. **7** is a flow diagram of a method **700**, in accordance with some embodiments.
[0080] More particularly, the flowchart of FIG. **7** represents a method of protecting input/output (I/O) circuitry. While the blocks of method **700** are discussed and shown as having a particular order, each block in method **700** is configured to be performed in any order unless specifically called out otherwise. Method **700** is implemented as a set of blocks, such as blocks **702** through **412**.
[0081] In block **702** of method **700**, a voltage level of a first ESD on I/O pad of the I/O circuitry is dissipated. Examples of the I/O pad include I/O pad **166**, **266**, or the like. Block **702** includes blocks **704-706**. An example of the I/O circuitry is I/O circuitry **136**, or the like. Flow proceeds within block **702** to block **704**.
[0082] In block **704** of method **702**, a first current is passed from the I/O pad through a first ESD device to a first node which reduces the voltage level of the first ESD to be at or below a reference voltage otherwise on the first node but for the first ESD. Examples of the first current include currents **120** of FIGS. **1**A-**1**B, **220**A of FIGS. **2**A-**2**B, or the like. Examples of the first ESD device include EUP device **112** of FIGS. **1-1**B, **212** of FIGS. **2**A-**2**B, or the like. Examples of the first node include nodes **122** n FIGS. **1**A-**1**B, **222** in FIGS. **2**A-**2**B, or the like. An example of the reference voltage otherwise on the first node but for the first ESD is voltage VDDL in FIGS. **1**A-**1**B and **2**A-**2**B, or the like. Flow proceeds from block **704** to block **706**.
[0083] In block **706** of method **700**, the dissipating a voltage level of a first ESD includes progressively turning on a string of two or more serially-connected diodes which are electrically connected between the I/O pad and the first node. Examples of the string of two or more serially-connected diodes which are electrically connected between the I/O pad and the first node include didoes **160-164** of FIG. **1**B, **270-270** of FIG. **2**B, or the like. In a non-limiting operation example, during a normal mode of block, which is free of an ESD-event, limiting leakage current flows between the I/O pad and the first node by forcing a voltage which induces the leakage current to progressively turn on a string of two or more serially-connected diodes which are electrically connected between the I/O pad and the first node. From block **706**, flow exits block **702** and

proceeds to block **708**. In some embodiments, method **700** bypasses block **708** and flow proceeds from block **706** to block **712**.

[0084] In block **708** of method **700**, a voltage level of a second ESD on a second node is dissipated. An example of the second node is node **226** in each of FIGS. **2**A-**2**B, or the like. Block **708** includes block **710**. Within block **708**, flow proceeds to block **710**.

[0085] In block **710** of method **700**, the dissipating a voltage level of a second ESD includes passing a second current from the second node through a second ESD device to the first node which reduces the voltage level of the second ESD to be at or below the reference voltage otherwise on the first node but for the second ESD. Examples of the second current include currents **220**C of FIGS. **2**A-**2**B, or the like. An example of the reference voltage otherwise on the first node but for the second ESD is voltage VDDL in FIGS. **2**A-**2**B, or the like. In a non-limiting operation example, the dissipating a voltage level of a second ESD includes progressively turning on a string of two or more serially-connected diodes which are electrically connected between the second node and the first node. In another non-limiting operation example, during a normal mode of block, which is free of an ESD-event, limiting leakage current flows between the I/O pad and the first node by forcing a voltage which induces the leakage current to progressively turn on a string of two or more serially-connected diodes which are electrically connected between the second node and the first node. Flow exits block **710** and proceeds to block **712**.

[0086] In some embodiments, method **700** bypasses block **702** such that flow in method **700** begins at block **708**. In such embodiments, an example of the second node is node **226** in FIG. **3**, or the like. Also, in such embodiments, regarding block **710**, an example of the second current is current **220**D of FIG. **3**, or the like. An example of the reference voltage otherwise on the first node but for the second ESD is voltage VDDL in FIG. **3**, or the like. Again, flow exits block **710** and proceeds to block **712**.

[0087] In block **712** of method **700**, the first current and/or the second current is passed through a power clamp to a second node. Examples of the power clamp include power clamps **128** in FIGS. **1**A-**1**B, **228** in FIGS. **2**A-**2**B & **3**, or the like. An example of the second current is current **129** in FIGS. **1**A-**1**B, **2**A-**2**B, **3**, or the like. Examples of the second node include node **124** in FIGS. **1**A-**1**B, **224** in FIGS. **2**A-**2**B & **3**, or the like.

[0088] As noted, in some embodiments, method **700** bypasses block **702** and flow begins at block **708**.

[0089] FIG. **5** is a block diagram of an electronic design automation (EDA) system **500** in accordance with some embodiments.

[0090] In some embodiments, EDA system **500** is a general-purpose computing device including a hardware processor **502** and a non-transitory, computer-readable storage medium **504**. Storage medium **504**, amongst other things, is encoded with, i.e., stores, computer program code **506**, i.e., a set of executable instructions. Execution of instructions **506** by hardware processor **502** represents (at least in part) an EDA tool which implements a portion or all in accordance with one or more embodiments (hereinafter, the noted processes and/or methods).

[0091] Processor **502** is electrically coupled to computer-readable storage medium **504** via a bus **508**. Processor **502** is further electrically coupled to an I/O interface **510** by bus **508**. A network interface **512** is further electrically connected to processor **502** via bus **508**. Network interface **512** is connected to a network **514**, so that processor **502** and computer-readable storage medium **504** are capable of connecting to external elements via network **514**. Processor **502** is configured to execute computer program code **506** encoded in computer-readable storage medium **504** to cause system **500** to be usable for performing a portion or all the noted processes and/or methods. In one or more embodiments, processor **502** is a central processing unit (CPU), a multi-processor, a distributed processing system, an application specific integrated circuit (ASIC), and/or a suitable processing unit.

[0092] In one or more embodiments, computer-readable storage medium **504** is an electronic, magnetic, optical, electromagnetic, infrared, and/or a semiconductor system (or apparatus or device). For example, computer-readable storage medium **504** includes a semiconductor or solid-state memory, a magnetic tape, a removable computer diskette, a random-access memory (RAM), a read-only memory (ROM), a rigid magnetic disk, and/or an optical disk. In one or more embodiments using optical disks, computer-readable storage medium **504** includes a compact disk-read only memory (CD-ROM), a compact disk-read/write (CD-R/W), and/or a digital video disc (DVD).

[0093] In one or more embodiments, storage medium **504** stores computer program code **506** configured to cause system **500** (where such execution represents (at least in part) the EDA tool) to be usable for performing a portion or all the noted processes and/or methods. In one or more embodiments, storage medium **504** further stores information which facilitates performing a portion or all the noted processes and/or methods. In one or more embodiments, storage medium **504** stores library **507** of standard cells including such standard cells as disclosed herein.

[0094] EDA system **500** includes I/O interface **510**. I/O interface **510** is coupled to external circuitry. In one or more embodiments, I/O interface **510** includes a keyboard, keypad, mouse, trackball, trackpad, touchscreen, and/or cursor direction keys for communicating information and commands to processor **502**.

[0095] EDA system **500** further includes network interface **512** coupled to processor **502**. Network interface **512** allows system **500** to communicate with network **514**, to which one or more other computer systems are connected. Network interface **512** includes wireless network interfaces such as BLUETOOTH, WIFI, WIMAX, GPRS, or WCDMA; or wired network interfaces such as ETHERNET, USB, or IEEE-1364. In one or more embodiments, a portion or all noted processes and/or methods, is implemented in two or more systems **500**.

[0096] System **500** is configured to receive information through I/O interface **510**. The information received through I/O interface **510** includes one or more of instructions, data, design rules, libraries of standard cells, and/or other parameters for processing by processor **502**. The information is transferred to processor **502** via bus **508**. EDA system **500** is configured to receive information related to a UI through I/O interface **510**. The information is stored in computer-readable medium **504** as user interface (UI) **542**.

[0097] In some embodiments, a portion or all the noted processes and/or methods is implemented as a standalone software application for execution by a processor. In some embodiments, a portion or all the noted processes and/or methods is implemented as a software application that is a part of an additional software application. In some embodiments, a portion or all the noted processes and/or methods is implemented as a plug-in to a software application. In some embodiments, at least one of the noted processes and/or methods is implemented as a software application that is a portion of an EDA tool. In some embodiments, a portion or all the noted processes and/or methods is implemented as a software application that is used by EDA system **500**. In some embodiments, a layout which includes standard cells is generated using a tool such as VIRTUOSO® available from CADENCE DESIGN SYSTEMS, Inc., or another suitable layout generating tool.

[0098] In some embodiments, the processes are realized as functions of a program stored in a non-transitory computer readable recording medium. Examples of a non-transitory computer readable recording medium include, but are not limited to, external/removable and/or internal/built-in storage or memory unit, e.g., one or more of an optical disk, such as a DVD, a magnetic disk, such as a hard disk, a semiconductor memory, such as a ROM, a RAM, a memory card, and the like.

[0099] FIG. **6** is a block diagram of an integrated circuit (IC) manufacturing system **600**, and an IC manufacturing flow associated therewith, in accordance with some embodiments.

[0100] In FIG. **6**, IC manufacturing system **600** includes entities, such as a design house **620**, a mask house **630**, and an IC manufacturer/fabricator (“fab”) **640**, that interact with one another in the design, development, and manufacturing cycles and/or services related to manufacturing an IC device **650**. The entities in system **600** are connected by a communications network. In some embodiments, the communications network is a single network. In some embodiments, the communications network is a variety of different networks, such as an intranet and the Internet. The communications network includes wired and/or wireless communication channels. Each entity interacts with one or more of the other entities and supplies services to and/or receives services from one or more of the other entities. In some embodiments, two or more of design house **620**, mask house **630**, and IC fab **640** is owned by a single larger company. In some embodiments, two or more of design house **620**, mask house **630**, and IC fab **640** coexist in a common facility and use common resources.

[0101] Design house (or design team) **620** generates an IC design layout **622**. IC design layout **622** includes various geometrical patterns designed for an IC device **650**. The geometrical patterns correspond to patterns of metal, oxide, or semiconductor layers that make up the various components of IC device **650** to be fabricated. The various layers combine to form various IC features. For example, a portion of IC design layout **622** includes various IC features, such as an active region, gate electrode, source and drain, metal lines or vias of an interlayer interconnection, and openings for bonding pads, to be formed in a semiconductor substrate (such as a silicon wafer) and various material layers disposed on the semiconductor substrate. Design house **620** implements a proper design procedure to form IC design layout **622**. The design procedure includes one or more of logic design, physical design or place and route. IC design layout **622** is presented in one or more data files having information of the geometrical patterns. For example, IC design layout **622** is expressed in a GDSII file format or DFII file format.

[0102] Mask house **630** includes data preparation **632** and mask fabrication **634**. Mask house **630** uses IC design layout **622** to manufacture one or more masks to be used for fabricating the various layers of IC device **650** according to IC design layout **622**. Mask house **630** performs mask data preparation **632**, where IC design layout **622** is translated into a representative data file ("RDF"). Mask data preparation **632** supplies the RDF to mask fabrication **634**. Mask fabrication **634** includes a mask writer. A mask writer converts the RDF to an image on a substrate, such as a mask (reticle) or a semiconductor wafer. The design layout is manipulated by mask data preparation **632** to comply with characteristics of the mask writer and/or requirements of IC fab **640**. In FIG. **6**, mask data preparation **632**, mask fabrication **634**, and mask **635** are illustrated as separate elements. In some embodiments, mask data preparation **632** and mask fabrication **634** are collectively referred to as mask data preparation.

[0103] In some embodiments, mask data preparation **632** includes optical proximity correction (OPC) which uses lithography enhancement techniques to compensate for image errors, such as those that arise from diffraction, interference, other process effects and the like. OPC adjusts IC design layout **622**. In some embodiments, mask data preparation **632** includes further resolution enhancement techniques (RET), such as off-axis illumination, sub-resolution assist features, phase-shifting masks, other suitable techniques, and the like or combinations thereof. In some embodiments, inverse lithography technology (ILT) is further used, which treats OPC as an inverse imaging problem.

[0104] In some embodiments, mask data preparation **632** includes a mask rule checker (MRC) that checks the IC design layout that has undergone processes in OPC with a set of mask creation rules which contain certain geometric and/or connectivity restrictions to ensure sufficient margins, to account for variability in semiconductor manufacturing processes, and the like. In some embodiments, the MRC modifies the IC design layout to compensate for limitations during mask fabrication **634**, which undoes part of the modifications performed by OPC to meet mask creation rules.

[0105] In some embodiments, mask data preparation **632** includes lithography process checking (LPC) that simulates processing that is implemented by IC fab **640** to fabricate IC device **650**. LPC simulates this processing based on IC design layout **622** to create a simulated manufactured device, such as IC device **650**. The processing parameters in LPC simulation include parameters associated with various processes of the IC manufacturing cycle, parameters associated with tools used for manufacturing the IC, and/or other aspects of the manufacturing process. LPC considers various factors, such as aerial image contrast, depth of focus (“DOF”), mask error enhancement factor (“MEEF”), other suitable factors, and the like or combinations thereof. In some embodiments, after a simulated manufactured device has been created by LPC, if the simulated device is not close enough in shape to satisfy design rules, OPC and/or MRC are be repeated to further refine IC design layout **622**.

[0106] The above description of mask data preparation **632** has been simplified for the purposes of clarity. In some embodiments, data preparation **632** includes additional features such as a logic operation (LOP) to modify the IC design layout according to manufacturing rules. Additionally, the processes applied to IC design layout **622** during data preparation **632** may be executed in a variety of different orders.

[0107] After mask data preparation **632** and during mask fabrication **634**, a mask **635** or a group of masks are fabricated based on the modified IC design layout. In some embodiments, an electron-beam (e-beam) or a mechanism of multiple e-beams is used to form a pattern on a mask (photomask or reticle) based on the modified IC design layout. The masks are formed in various technologies. In some embodiments, the mask is formed using binary technology. In some embodiments, a mask pattern includes opaque regions and transparent regions. A radiation beam, such as an ultraviolet (UV) beam, used to expose the image sensitive material layer (e.g., photoresist) which has been coated on a wafer, is blocked by the opaque region, and transmits through the transparent regions. In one example, a binary mask includes a transparent substrate (e.g., fused quartz) and an opaque material (e.g., chromium) coated in the opaque regions of the mask. In another example, the mask is formed using a phase shift technology. In the phase shift mask (PSM), various features in the pattern formed on the mask are configured to have proper phase difference to enhance the resolution and imaging quality. In various examples, the phase shift mask is an attenuated PSM or alternating PSM. The mask(s) generated by mask fabrication **634** is used in a variety of processes. For example, such a mask(s) is used in an ion implantation process to form various doped regions in the semiconductor wafer, in an etching process to form various etching regions in the semiconductor wafer, and/or in other suitable processes.

[0108] IC fab **640** is an IC fabrication business that includes one or more manufacturing facilities for the fabrication of a variety of different IC products. In some embodiments, IC Fab **640** is a semiconductor foundry. For example, there may be a manufacturing facility for the front-end fabrication of a plurality of IC products (front-end-of-line (FEOL) fabrication), while a second manufacturing facility supplies the back-end fabrication for the interconnection and packaging of the IC products (back-end-of-line (BEOL) fabrication), and a third manufacturing facility may supply other services for the foundry business.

[0109] IC fab **640** uses the mask (or masks) fabricated by mask house **630** to fabricate IC device **650**. Thus, IC fab **640** at least indirectly uses IC design layout **622** to fabricate IC device **650**. In some embodiments, a semiconductor wafer **643** is fabricated by fabrication tools **642** using the mask (or masks) to form IC device **650**. Semiconductor wafer **643** includes a silicon substrate or other proper substrate having material layers formed thereon. Semiconductor wafer further includes one or more of various doped regions, dielectric features, multilevel interconnects, and the like (formed at subsequent manufacturing steps).

[0110] In some embodiments, an electro-static discharge (ESD) protection network for an input/output (I/O) pad includes: a driver stack including a serially-connected upper branch and a lower branch, the upper branch being electrically connected between a first node that has a first reference voltage and the I/O pad, and the lower branch being electrically connected between the I/O pad and a second node that has a second reference voltage; a first ESD device electrically connected between the I/O pad and a third node that has a third reference voltage; and a power clamp between the third node and the second node.

[0111] In some embodiments, the protection network further includes a second ESD device electrically connected between the second node and the I/O pad. In some embodiments, the protection network further includes a third ESD device electrically connected between the third node and the I/O pad. In some embodiments, the third ESD device includes a diode that includes a diode cathode connected to the third reference voltage and a diode anode connected to the I/O pad and the second ESD device. In some embodiments, the second ESD device includes a number of N diodes connected in series, N being a positive integer and 2≤N; and the number N diodes are based on a difference between the second reference voltage and a voltage of the I/O pad. In some embodiments, the first ESD device includes a number of P diodes connected in series, P being a positive integer and 1≤P. In some embodiments, the upper branch of the driver stack includes series-connected positive-channel metal oxide semiconductor (PMOS) transistors between the first node and the I/O pad. In some embodiments, the lower branch of the driver stack includes series-connected negative-channel metal oxide semiconductor (NMOS) transistors between the I/O pad and the second node.

[0112] In some embodiments, an electro-static discharge (ESD) protection network for an input/output (I/O) pad includes a first ESD device electrically connected between a first node having a first reference voltage and the I/O pad; and a second ESD device electrically connected between a second node having a second reference voltage and the I/O pad; and wherein the first ESD device has a number N of diodes connected in series, N being a positive integer and 2≤N; and the number Nis based on a difference between the first reference voltage and a voltage of the I/O pad.

[0113] In some embodiments, the number N of diodes are of a first size, the second ESD device includes a diode of a second size, and the second size is greater than N multiple of the first size. In some embodiments, the difference is referred to by a variable Δ; each of the diodes has substantially a same knee voltage as a reference voltage VK; and the number N is equal to or greater than one plus a floor function applied to a ratio of the difference A divided by VK such that

[00003] $1 + \left(\frac{}{\mathrm{VK}}\right) \leq N$.

In some embodiments, the protection network further includes a power clamp between the first node and the second node. In some embodiments, the protection network further includes a first group of series-connected transistors between a third node at a third reference voltage and the I/O pad. In some embodiments, the protection network further includes a second group of series-connected transistors between the I/O pad and the second node. In some embodiments, the protection network further includes a first power clamp between the third node and the second node. In some embodiments, the protection network further includes a second power clamp between the first node and the second node.

[0114] In some embodiments, a method (of protecting input/output (I/O) circuitry) includes: dissipating a voltage level of a first ESD on I/O pad of the I/O circuitry; and wherein the dissipating a voltage level of a first ESD includes passing a first current from the I/O pad through a first ESD device to a first node which reduces the voltage level of the first ESD to be at or below a reference voltage otherwise on the first node but for the first ESD.

[0115] In some embodiments, the dissipating a voltage level of a first ESD includes: progressively turning on a string of two or more serially-connected diodes which are electrically connected between the I/O pad and the first node. In some embodiments, the method further includes: during a normal mode of operation which is free of an ESD-event, limiting leakage current that flows between the I/O pad and the first node by forcing a voltage which induces the leakage current to progressively turn on a string of two or more serially-connected diodes which are electrically connected between the I/O pad and the first node. In some embodiments, the method further includes: dissipating a voltage level of a second ESD on a second node; and wherein the dissipating a voltage level of a second ESD includes passing a second current from the second node through a second ESD device to the first node which reduces the voltage level of the second ESD to be at or below the reference voltage otherwise on the first node but for the second ESD. In some embodiments, the dissipating a voltage level of a second ESD includes: progressively turning on a string of two or more serially-connected diodes which are electrically connected between the second node and the first node. In some embodiments, the method further includes: during a normal mode of operation which is free of an ESD-event, limiting leakage current that flows between the I/O pad and the first node by forcing a voltage which induces the leakage current to progressively turn on a string of two or more serially-connected diodes which are electrically connected between the second node and the first node. In some embodiments, the method further includes: passing the second current through a power clamp to a second node. In some embodiments, the method further includes: passing the first current through a power clamp to a second node.

[0116] In some embodiments, an electro-static discharge (ESD) protection network for an input/output (I/O) pad includes a first ESD device electrically connected between a first node having a first reference voltage and the I/O pad; a second ESD device electrically connected between a second node having a second reference voltage and the I/O pad; a first group of series-connected transistors between a third node having a third reference voltage and the I/O pad; a second group of series-connected transistors between the I/O pad and the second node; a power clamp between the first node and the second node; and a third ESD device electrically connected between the third node and the first node.

[0117] In some embodiments, the first ESD device has a number N of diodes connected in series, N being a positive integer and 2≤N. In some embodiments, the number N is based on a difference, Δ, between the first reference voltage and a voltage of the I/O pad. In some embodiments, each of the diodes has substantially a same knee voltage as a reference voltage VK; and the number N is equal to or greater than one plus a floor function applied to a ratio of the difference Δ divided by VK such that

[00004] $1 + \left(\frac{}{\mathrm{VK}}\right) \leq N.$

The foregoing outlines structures of several embodiments so that those skilled in the art may better understand the aspects of the present disclosure. Those skilled in the art should appreciate that they may readily use the present disclosure as a basis for designing or modifying other processes and structures for carrying out the same purposes and/or achieving the same advantages of the embodiments introduced herein. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the present disclosure, and that they may make various changes, substitutions, and alterations herein without departing from the spirit and scope of the present disclosure.

[0118] An aspect of this description relates to an electro-static discharge (ESD) protection circuit. The ESD protection circuit includes a driver stack electrically connected between a first node that has a first reference voltage and a second node that has a second reference voltage. The ESD protection circuit further includes an input/output (I/O) pad electrically connected to the driver stack, wherein the driver stack is electrically between the I/O pad and each of the first node and the second node. The ESD protection circuit further includes a first ESD device electrically connected between the I/O pad and a third node that has a third reference voltage, wherein the I/O pad is electrically connected between the first ESD device and the driver stack. In some embodiments, the ESD protection device further includes a second ESD device electrically connected between the I/O pad and the second node. In some embodiments, the first ESD device includes a plurality of diodes, and the second ESD device includes at least one diode. In some embodiments, a number of diodes in the first ESD device is greater than a number of diodes in the second ESD device. In some embodiments, the ESD protection circuit further includes a first power clamp circuit between the first reference voltage and the second reference voltage. In some embodiments, the ESD protection circuit further includes a second power clamp circuit between the second reference voltage and the third reference voltage. In some embodiments, the ESD protection circuit further

includes a power to power discharge device between the first reference voltage and the third reference voltage. In some embodiments, the power to power discharge device comprises a first number of diodes, and the first ESD device comprises a second number of diodes. In some embodiments, the first number is different from the second number. In some embodiments, the first number is equal to the second number.
[0119] An aspect of this description relates to an electro-static discharge (ESD) protection device. The ESD protection device includes a first ESD device electrically connected between a first node having a first reference voltage and an input/output (I/O) pad. The ESD protection device further includes a second ESD device electrically connected between a second node having a second reference voltage and the I/O pad. The ESD protection device further includes a third ESD device electrically connected between the first node and a third node having a third reference voltage, wherein the first node is electrically between the first ESD device and the third ESD device. In some embodiments, the third reference voltage is higher than the first reference voltage. In some embodiments, the first reference voltage is greater than the second reference voltage. In some embodiments, the first ESD device comprises a first number of diodes, the second ESD device comprises a second number of diodes, and the third ESD device includes a third number of diodes. In some embodiments, the first number is greater than the second number. In some embodiments, the first number is equal to the third number. In some embodiments, the first number is different from the third number.
[0120] An aspect of this description relates to an electro-static discharge (ESD) protection device. The ESD protection device includes a first ESD device electrically connected between a first node having a first reference voltage and an input/output (I/O) pad, wherein the first ESD device comprises a plurality of first diodes, and a number of first diodes in the plurality of first diodes is based on difference between the first reference voltage and a voltage of the I/O pad. The ESD protection device further includes a second ESD device electrically connected between the first node and a second node having a second reference voltage, wherein the first node is electrically between the first ESD device and the second ESD device, the second ESD device comprises a plurality of second diodes, and a number of second diodes in the plurality of second diodes is based on difference between the second reference voltage and a voltage of the I/O pad. In some embodiments, the ESD protection device further includes a third ESD device between the I/O pad and a third node having a third reference voltage, wherein the third reference voltage is different from the first reference voltage and the second reference voltage. In some embodiments, the number of first diodes is different from the number of second diodes.

Claims

1. An electro-static discharge (ESD) protection circuit, comprising: a driver stack electrically connected between a first node that has a first reference voltage and a second node that has a second reference voltage; an input/output (I/O) pad electrically connected to the driver stack, wherein the driver stack is electrically between the I/O pad and each of the first node and the second node; a first ESD device electrically connected between the I/O pad and a third node that has a third reference voltage, wherein the I/O pad is electrically connected between the first ESD device and the driver stack.
2. The ESD protection circuit of claim 1, further comprising a second ESD device electrically connected between the I/O pad and the second node.
3. The ESD protection circuit of claim 2, wherein the first ESD device comprises a plurality of diodes, and the second ESD device comprises at least one diode.
4. The ESD protection circuit of claim 3, wherein a number of diodes in the first ESD device is greater than a number of diodes in the second ESD device.
5. The ESD protection circuit of claim 1, further comprising a first power clamp circuit between the

first reference voltage and the second reference voltage.
6. The ESD protection circuit of claim 5, further comprising a second power clamp circuit between the second reference voltage and the third reference voltage.
7. The ESD protection circuit of claim 1, further comprising a power to power discharge device between the first reference voltage and the third reference voltage.
8. The ESD protection circuit of claim 7, wherein the power to power discharge device comprises a first number of diodes, and the first ESD device comprises a second number of diodes.
9. The ESD protection circuit of claim 8, wherein the first number is different from the second number.
10. The ESD protection circuit of claim 8, wherein the first number is equal to the second number.
11. An electro-static discharge (ESD) protection device comprising: a first ESD device electrically connected between a first node having a first reference voltage and an input/output (I/O) pad; a second ESD device electrically connected between a second node having a second reference voltage and the I/O pad; and a third ESD device electrically connected between the first node and a third node having a third reference voltage, wherein the first node is electrically between the first ESD device and the third ESD device.
12. The ESD protection device of claim 11, wherein the third reference voltage is higher than the first reference voltage.
13. The ESD protection device of claim 11, wherein the first reference voltage is greater than the second reference voltage.
14. The ESD protection device of claim 11, wherein the first ESD device comprises a first number of diodes, the second ESD device comprises a second number of diodes, and the third ESD device includes a third number of diodes.
15. The ESD protection device of claim 14, wherein the first number is greater than the second number.
16. The ESD protection device of claim 15, wherein the first number is equal to the third number.
17. The ESD protection device of claim 15, wherein the first number is different from the third number.
18. An electro-static discharge (ESD) protection device comprising: a first ESD device electrically connected between a first node having a first reference voltage and an input/output (I/O) pad, wherein the first ESD device comprises a plurality of first diodes, and a number of first diodes in the plurality of first diodes is based on difference between the first reference voltage and a voltage of the I/O pad; a second ESD device electrically connected between the first node and a second node having a second reference voltage, wherein the first node is electrically between the first ESD device and the second ESD device, the second ESD device comprises a plurality of second diodes, and a number of second diodes in the plurality of second diodes is based on difference between the second reference voltage and a voltage of the I/O pad.
19. The ESD protection device of claim 18, further comprising a third ESD device between the I/O pad and a third node having a third reference voltage, wherein the third reference voltage is different from the first reference voltage and the second reference voltage.
20. The ESD protection device of claim 18, wherein the number of first diodes is different from the number of second diodes.