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THREE-DIMENSIONAL SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

Abstract

A three-dimensional semiconductor device includes a semiconductor pattern spaced apart from a substrate, and extending along a first direction parallel to a lower surface of the substrate, a word line surrounding the semiconductor pattern, and extending along a second direction parallel to the lower surface of the substrate, and crossing the first direction, and a bit line extending along a first side surface of the semiconductor pattern along a third direction perpendicular to the lower surface of the substrate, wherein the word line includes a first gate electrode, a second gate electrode on a first side surface of the first gate electrode, and a third gate electrode on a second surface opposite to the first side surface of the first gate electrode, and a work function of each of the second and third gate electrodes is smaller than a work function of the first gate electrode.

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Background/Summary

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This U.S. non-provisional patent application claims priority under 35 U.S.C. § 119 of Korean Patent Application No. 10-2024-0022731, filed on Feb. 16, 2024, in the Korean Intellectual Property Office, the entire contents of which are hereby incorporated by reference.

BACKGROUND

[0002] The present disclosure herein relates to a three-dimensional semiconductor device and a method for manufacturing the same, and more particularly, to a three-dimensional semiconductor device with more improved reliability and integration.

[0003] Semiconductor devices are attracting attention as an important component in the electronics industry due to characteristics such as miniaturization, multi-functionality, and/or low manufacturing cost. A semiconductor device may be a semiconductor memory device that stores logical data, a semiconductor logic device that computes and processes the logical data, and a hybrid semiconductor device that includes memory components and logical components.

[0004] Recently, due to high speed and low power consumption of an electronic apparatus, high operation speed, low operation voltage, and/or the like are/is also typically required for the semiconductor device built thereinto, and in order to satisfy such requirements, a more integrated semiconductor device is needed. However, as semiconductor devices become more highly integrated, electrical characteristics and production yield of the semiconductor devices may decrease. Accordingly, a lot of research on improving the electrical characteristics and the production yield of semiconductor devices is being conducted.

SUMMARY

[0005] Aspects of the present disclosure provides a three-dimensional semiconductor device with improved reliability. However, other benefits may also be realized from the various embodiments disclosed herein.

[0006] An embodiment of the inventive concept provides a three-dimensional semiconductor device including a semiconductor pattern spaced apart from a substrate, and extending along a first direction parallel to a lower surface of the substrate, a word line surrounding the semiconductor pattern, and extending along a second direction parallel to the lower surface of the substrate, and crossing the first direction, and a bit line extending along a first side surface of the semiconductor pattern along a third direction perpendicular to the lower surface of the substrate, wherein the word line includes a first gate electrode, a second gate electrode on a first side surface of the first gate electrode, and a third gate electrode on a second surface opposite to the first side surface of the first gate electrode, and a work function of each of the second and third gate electrodes is smaller than a work function of the first gate electrode.

[0007] In an embodiment of the inventive concept, a three-dimensional semiconductor device includes a semiconductor pattern spaced apart from a substrate, and extending along a first direction parallel to a lower surface of the substrate, a word line surrounding the semiconductor pattern, and extending along a second direction parallel to the lower surface of the substrate, and crossing the first direction, and a bit line extending along a first side surface of the semiconductor pattern along a third direction perpendicular to the lower surface of the substrate, wherein the word line includes a first gate electrode including a first material, a second gate electrode provided on a first side surface of the first gate electrode, and including a second material, and a third gate electrode provided on a second side surface opposite to the first side surface of the first gate electrode, and including a third material, the first material includes a material different from the

second and third materials, and a work function of each of the second material and the third material is smaller than a work function of the first material.
[0008] In an embodiment of the inventive concept, a three-dimensional semiconductor device includes a first stack structure on a substrate, and a second stack structure adjacent to the first stack structure in a first direction parallel to a lower surface of the substrate, and a data storage pattern between the first stack structure and the second stack structure, wherein the first stack structure includes a first semiconductor pattern spaced apart from the substrate, and extending along the first direction, a first word line surrounding the first semiconductor pattern, and extending along a second direction parallel to the lower surface of the substrate, and crossing the first direction, and a first bit line extending along a first side surface of the first semiconductor pattern along a third direction perpendicular to the lower surface of the substrate, the first word line includes a first gate electrode, a second gate electrode on a first side surface of the first gate electrode, and a third gate electrode on a second side surface opposite to the first side surface of the first gate electrode, and a work function of each of the second and third gate electrodes is smaller than a work function of the first gate electrode.

Description

BRIEF DESCRIPTION OF THE FIGURES
[0009] The accompanying drawings are included to provide a further understanding of the inventive concept, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the inventive concept and, together with the description, serve to explain principles of the inventive concept. In the drawings:
[0010] FIG. **1** is a circuit diagram schematically illustrating a three-dimensional semiconductor device according to an embodiment of the inventive concept;
[0011] FIGS. **2**A, **2**B, and **2**C are schematic perspective views of a three-dimensional semiconductor device according to an embodiment of the inventive concept;
[0012] FIG. **3** is a plan view of a three-dimensional semiconductor device according to an embodiment of the inventive concept;
[0013] FIG. **4** is a perspective view illustrating semiconductor patterns, word lines, bit lines, and a data storage pattern of a three-dimensional semiconductor device according to an embodiment of the inventive concept;
[0014] FIG. **5**A is a cross-sectional view corresponding to line A-A′ in FIG. **3**;
[0015] FIG. **5**B is a cross-sectional view corresponding to line B-B′ in FIG. **3**;
[0016] FIGS. **6**A to **6**C are enlarged views corresponding to PI in FIG. **5**A; and
[0017] FIGS. **7** to **20** are diagrams illustrating a method for manufacturing a three-dimensional semiconductor device according to an embodiment of the inventive concept.
DETAILED DESCRIPTION
[0018] Hereinafter, in order to specifically describe the inventive concept, embodiments according to the inventive concept will be described in more detail with reference to the accompanying drawings.
[0019] It will be understood that when an element is referred to as being “connected” or “coupled” to or “on” another element, it can be directly connected or coupled to or on the other element or intervening elements may be present. In contrast, when an element is referred to as being “directly connected” or “directly coupled” to another element, or as “contacting” or “in contact with” another element (or using any form of the word “contact”), there are no intervening elements present at the point of contact.
[0020] Terms such as “same,” “equal,” “planar,” “coplanar,” “parallel,” and “perpendicular,” as used herein encompass identicality or near identicality including variations that may occur resulting

from conventional manufacturing processes. The term “substantially” may be used herein to emphasize this meaning, unless the context or other statements indicate otherwise.
[0021] Ordinal numbers such as “first,” “second,” “third,” etc. may be used simply as labels of certain elements, steps, etc., to distinguish such elements, steps, etc. from one another. Terms that are not described using “first,” “second,” etc., in the specification, may still be referred to as “first” or “second” in a claim. In addition, a term that is referenced with a particular ordinal number (e.g., “first”) in a particular claim may be described elsewhere with a different ordinal number (e.g., “second”) in the specification or another claim.
[0022] Throughout the specification, when a component is described as “including” a particular element or group of elements, it is to be understood that the component is formed of only the element or the group of elements, or the element or group of elements may be combined with additional elements to form the component, unless the context indicates otherwise. The term “consisting of,” on the other hand, indicates that a component is formed only of the element(s) listed.
[0023] An item, layer, or portion of an item or layer described as extending “lengthwise” in a particular direction has a length in the particular direction and a width perpendicular to that direction, where the length is greater than the width, unless the context indicates otherwise.
[0024] FIG. **1** is a circuit diagram schematically illustrating a three-dimensional semiconductor device according to an embodiment of the inventive concept.
[0025] Referring to FIG. **1**, the three-dimensional semiconductor device may include a memory cell array **1**, a row decoder **2**, a sense amplifier **3**, a column decoder **4**, and a control logic **5**. A semiconductor device, as described herein, may be a semiconductor chip, for example, formed on a die and separated from a wafer. A semiconductor device as described herein may also be a stack of semiconductor chips, or a semiconductor package including one or more semiconductor chips.
[0026] The memory cell array **1** may include word lines WL, bit lines BL, source lines SL, and memory cells MC. The memory cells MC may be three-dimensionally arranged, and a memory cell MC may be connected to one word line WL, one bit line BL, and one source line SL. In an embodiment, the memory cells MC may be each composed of one transistor including a memory film or layer (or a data storage film or layer).
[0027] The row decoder **2** may decode an externally input address input to select any one among the word lines WL of the memory cell array **1**. The address decoded by the row decoder **2** may be supplied to a row driver (not shown), and the row driver may supply a predetermined voltage to each of a selected word line WL and non-selected word lines WL in response to control by control logic **5**.
[0028] The sense amplifier **3** may sense and amplify a voltage difference between a selected bit line BL according to an address decoded by the column decoder **4** and a reference bit line BL to output the same.
[0029] The column decoder **4** may provide a data transmission path between the sense amplifier **3** and an external unit (for example, a memory controller). The column decoder **4** may decode an externally input address input to select any one among the bit lines BL.
[0030] The control logic **5** may generate control signals that control an operation of writing or reading data to/from the memory cell array **1**.
[0031] FIGS. **2**A, **2**B, and **2**C are schematic perspective views of a three-dimensional semiconductor device according to an embodiment of the inventive concept.
[0032] Referring to FIG. **2**A, the three-dimensional semiconductor device may include a substrate **100**, a peripheral circuit structure PS on the substrate **100**, and a cell array structure CS on the peripheral circuit structure PS.
[0033] The peripheral circuit structure PS may include core and peripheral circuits formed on the substrate **100**. The core and peripheral circuits may include the row and column decoders **2** and **4** (see FIG. **1**), the sense amplifier **3** (see FIG. **1**), and the control logic **5** (see FIG. **1**) described with

reference to FIG. **1**.
[0034] The substrate **100** may have a form of a plate extending along a plane defined by a first direction D**1** and a second direction D**2**. The first direction D**1** and the second direction D**2** may be parallel to a lower surface of the substrate **100**, and may cross each other. For example, the first direction D**1** and the second direction D**2** may be horizontal directions perpendicular to each other. The peripheral circuit structure PS and the cell array structure CS may be sequentially stacked on the substrate **100** in a third direction D**3** orthogonal to the lower surface of the substrate **100**.
[0035] The cell array structure CS may include the bit lines BL, the source lines SL, the word lines WL, and the memory cells MC therebetween. The memory cells MC may be each connected to one word line WL, one bit line BL, and one source line SL.
[0036] Referring to FIG. **2**B, a semiconductor device may include the cell array structure CS on the substrate **100**, and the peripheral circuit structure PS on the cell array structure CS. The cell array structure CS may be disposed between the substrate **100** and the peripheral circuit structure PS. The peripheral circuit structure PS may include the core and peripheral circuits.
[0037] Referring to FIG. **2**C, the semiconductor device may have a chip to chip (C2C) structure. The peripheral circuit structure PS may include a first substrate **100***a*. Lower metal pads LMP may be provided to an uppermost portion of the peripheral circuit structure PS. The lower metal pads LMP may be electrically connected to the core and peripheral circuits. The lower metal pads LMP may be bonded to upper metal pads UMP of the cell array structure CS.
[0038] The cell array structure CS may include a second substrate **200***a*, and the upper metal pads UMP may be provided to a lowermost portion of the cell array structure CS. The upper metal pads UMP may be electrically connected to the bit lines BL, the source lines SL, and the word lines WL. The upper metal pads UMP may be electrically connected to the memory cells MC.
[0039] FIG. **3** is a plan view of a three-dimensional semiconductor device according to an embodiment of the inventive concept. FIG. **4** is a perspective view illustrating semiconductor patterns, word lines, bit lines, and a data storage pattern of a three-dimensional semiconductor device according to an embodiment of the inventive concept. FIG. **5**A is a cross-sectional view corresponding to line A-A′ in FIG. **3**. FIG. **5**B is a cross-sectional view corresponding to line B-B′ in FIG. **3**.
[0040] Referring to FIGS. **3** to **5**B, the three-dimensional semiconductor device may include a substrate **100**. For example, the substrate **100** may be a semiconductor substrate, an insulating substrate, a silicon-on-insulator (SOI) substrate, or a germanium-on-insulator (GOI) substrate. For example, the semiconductor substrate may be a silicon substrate, a germanium substrate, or a silicon-germanium substrate. The substrate **100** may have a form of a plate extending along a plane defined by the first direction D**1** and the second direction D**2**.
[0041] A cell array structure CS may be provided on the substrate **100**. The cell array structure CS may include a first stack structure ST**1** and a second stack structure ST**2** adjacent to each other in the first direction D**1**, and a data storage pattern DSP therebetween to be described later. For example, although not shown in the drawing, the cell array structure CS may be one of a plurality of cell array structures CS adjacent to each other in the first direction D**1**. Hereinafter, a single cell array structure CS will be described for convenience of description, but the description will be identically applied to other cell array structures CS.
[0042] The first stack structure ST**1** and the second stack structure ST**2** may each include semiconductor patterns SP, word lines WL, bit lines BL, first capping patterns CP**1**, second capping patterns CP**2**, and a buried insulating pattern **110**. For example, the first and second stack structures ST**1** and ST**2** may be mirror-symmetrical with respect to the data storage pattern DSP.
[0043] The semiconductor pattern SP may extend on the substrate **100** along the first direction D**1**. For example, the semiconductor pattern SP may have a form of a bar extending along the first direction D**1**. The semiconductor pattern SP may be spaced apart from the substrate **100**. For example, the semiconductor pattern SP may be floated from the substrate **100**.

[0044] The semiconductor pattern SP may include a first edge portion EA**1** and a second edge portion EA**2** spaced apart from each other in the first direction D**1**, and a channel region CH therebetween. The channel region CH of the semiconductor pattern SP may be surrounded by the word line WL to be described later. The first edge portion EA**1** of the semiconductor pattern SP may be adjacent to the bit line BL to be described later. The first edge portion EA**1** may be in contact with and may be electrically connected to the bit line BL. The second edge portion EA**2** may be adjacent to the data storage pattern DSP to be described later. The second edge portion EA**2** may be in contact with and may be electrically connected to the data storage pattern DSP.
[0045] The semiconductor pattern SP may have a first side surface S**1** and a second side surface S**2** opposed thereto. The first side surface S**1** may be a side surface of the first edge portion EA**1**, and the second side surface S**2** may be a side surface of the second edge portion EA**2**. The first side surface S**1** of the semiconductor pattern SP may be in contact with the bit line BL, and the second side surface S**2** may be in contact with the data storage pattern DSP.
[0046] The semiconductor pattern SP may include at least one of a single crystalline semiconductor, a polycrystalline semiconductor, an oxide semiconductor, or a two-dimensional material. For example, the single crystalline semiconductor may be a single crystalline silicon. For example, the polycrystalline semiconductor may be polysilicon. For example, the oxide semiconductor may be indium-gallium-zinc oxide (IGZO). For example, the two-dimensional material may be MoS.sub.2, WS.sub.2, MoSe.sub.2, or WSe.sub.2.
[0047] For example, each of the first and second edge portions EA**1** and EA**2** of the semiconductor pattern SP may include therein an impurity region doped with an impurity (for example, an N-type or P-type impurity). The impurity region may constitute a source/drain region of a transistor.
[0048] The semiconductor pattern SP may be provided in plurality. The semiconductor patterns SP may be adjacent to each other in the second direction D**2** and the third direction D**3**. The semiconductor patterns SP adjacent to each other in the third direction D**3** may vertically overlap each other. Sidewalls of the semiconductor patterns SP adjacent to each other in the third direction D**3** may be aligned with each other.
[0049] The semiconductor pattern SP may include a first semiconductor pattern SPa provided in the first stack structure ST**1** and a second semiconductor pattern SPb provided in the second stack structure ST**2**. The first semiconductor pattern SPa and the second semiconductor pattern SPb may be adjacent to each other in the first direction D**1**. The first edge portion EA**1** and the second edge portion EA**2** of the first semiconductor pattern SPa may be sequentially disposed along the first direction D**1**. The first edge portion EA**1** and the second edge portion EA**2** of the second semiconductor pattern SPb may be sequentially disposed in the first direction D**1** in an opposite orientation as the first edge portion EA**1** and the second edge portion EA**2** of the first semiconductor pattern SPa to have a mirror symmetry with first edge portion EA**1** and the second edge portion EA**2** of the first semiconductor pattern.
[0050] The word line WL may surround the channel region CH of the semiconductor pattern SP, and may extend along the second direction D**2**. For example, the word line WL may have a structure (e.g., a gate-all-around structure) in which the channel region CH of the semiconductor pattern SP is completely surrounded. One word line WL may surround the channel region CH of each of the semiconductor patterns SP adjacent to each other in the second direction D**2**. The word lines WL may be provided in plurality. Each word lines WL may surround the channel region CH of the corresponding respective semiconductor pattern SP among the semiconductor patterns SP adjacent to each other in the third direction D**3**, and may extend along the second direction D**2**.
[0051] The word line WL may include, in the first stack structure ST**1**, a first word line WLa surrounding the channel region CH of the first semiconductor pattern SPa, and may include, in the second stack structure ST**2**, a second word line WLb surrounding the channel region CH of the second semiconductor pattern SPb.
[0052] The word line WL may include a gate dielectric film Gox (also described as a gate dielectric

layer) surrounding the channel region CH of the semiconductor pattern SP, and a gate electrode GE surrounding the channel region CH of the semiconductor pattern SP on the gate dielectric film Gox.
[0053] The gate dielectric film Gox may include a single film selected from a high-k dielectric film, a silicon oxide film, a silicon nitride film, and a silicon oxynitride film, or a combination thereof. In the present disclosure, a material having a high dielectric constant (high-k) is defined as a material having a higher dielectric constant than silicon oxide.
[0054] The gate electrode GE may include a first gate electrode GE**1** having a first work function, a second gate electrode GE**2** having a second work function and disposed on one side surface (e.g., a first side surface) of the first gate electrode GE**1**, and a third gate electrode GE**3** having a third work function and disposed on the other side surface opposed to the one side surface (e.g., a second surface opposite the first side surface) of the first gate electrode GE**1**. According to some embodiments, neither the second gate electrode GE**2** nor the third gate electrode GE**3** are formed on a top surface or bottom surface of the first gate electrode GE**1**. The second gate electrode GE**2** may be adjacent to the first edge portion EA**1** of the semiconductor pattern SP, and the third gate electrode GE**3** may be adjacent to the second edge portion EA**2** of the semiconductor pattern SP. The second gate electrode GE**2** may be interposed between the first gate electrode GE**1** and the bit line BL, and the third gate electrode GE**3** may be interposed between the first gate electrode GE**1** and the data storage pattern DSP.
[0055] According to aspects of the inventive concept, the second work function of the second gate electrode GE**2** and the third work function of the third gate electrode GE**3** may be each smaller than the first work function of the first gate electrode GE**1**. For example, the second work function of the second gate electrode GE**2** and the third work function of the third gate electrode GE**3** may be the same as each other. Accordingly, during an operation of the three-dimensional semiconductor device, a gate-induced drain leakage (GIDL) phenomenon generated in the semiconductor pattern SP may be reduced. As a result, an amount of holes accumulated in the semiconductor pattern SP may be reduced, and a leakage current caused by the holes may be reduced. Therefore, reliability of the three-dimensional semiconductor device may be improved.
[0056] The first gate electrode GE**1** may include or be a first material having the first work function. The second gate electrode GE**2** may include or be a second material having the second work function. The third gate electrode GE**3** may include or be a third material having the third work function. In some embodiments, the first material may be different from each of the second material and the third material. The work function of each of the second and third materials may be smaller than the work function of the first material.
[0057] For example, the first material may include or be at least one of Ti, TiN, TiSiN, TiON, W, WN, Mo, MON, MoO.sub.xN.sub.y, Ta, TaN, or poly Si. For example, the second material and the third material may each include or be at least one of Li, Na, K, Cs, Rb, Sr, Ba, Ca, Ce, Sm, Eu, Mg, Sc, Y, Hf, Tl, As, La, Nd, Gd, Tb, Lu, Th, U, Mn, Al, Ga, In, Pb, Cd, Bi, Zr, Ti, TiN, or poly Si doped with an N-type conductive impurity. The second material may be the same material as the third material in some embodiments.
[0058] Hereinafter, various embodiment of first to third gate electrodes GE**1**, GE**2**, and GE**3** will be described with reference to FIGS. **6**A to **6**C.
[0059] Referring to FIG. **6**A, with respect to the first direction D**1**, the first gate electrode GE**1** may have a first width W**1**, the second gate electrode GE**2** may have a second width W**2**, and the third gate electrode GE**3** may have a third width W**3**. The first width W**1** may be greater than the second and third widths W**2** and W**3**, but an embodiment is not limited thereto. The second width W**2** and the third width W**3** may be substantially the same as each other.
[0060] As an example, the second gate electrode GE**2** and the third gate electrode GE**3** may include or be formed of the same material. For example, the second material and the third material may be the same as each other. Accordingly, the second work function and the third work function may be substantially the same as each other.

[0061] As another example, the second gate electrode GE**2** and the third gate electrode GE**3** may include or be formed of different materials. For example, the second material and the third material may be different from each other. According to a material included in each of the second material and the third material, the second work function may be smaller than the third work function, or the third work function may be smaller than the second work function.
[0062] As an example, when the first edge portion EA**1** of the semiconductor pattern SP is more vulnerable to the gate-induced drain leakage (GIDL) phenomenon than the second edge portion EA**2**, the second material may have a lower work function than the third material. In this example, the second work function of the second gate electrode GE**2** may be smaller than the third work function of the third gate electrode GE**3**.
[0063] As another example, when the second edge portion EA**2** of the semiconductor pattern SP is more vulnerable to the gate-induced drain leakage (GIDL) phenomenon than the first edge portion EA**1**, the third material may have a lower work function than the second material. In this example, the third work function of the third gate electrode GE**3** may be smaller than the second work function of the second gate electrode GE**2**.
[0064] Referring to FIGS. **6**B and **6**C, the second gate electrode GE**2** and the third gate electrode GE**3** may be asymmetrical with respect to the first gate electrode GE**1**. The second material may be the same as or different from the third material. The second material may be the same as or different from the second material in FIG. **6**A, and the third material may be the same as or different from the third material in FIG. **6**A.
[0065] Referring to FIG. **6**B, the second width W**2** may be greater than the third width W**3**. The second width W**2** may be greater than the second width W**2** in FIG. **6**A. Accordingly, a region in which the second gate electrode GE**2** and the semiconductor pattern SP overlap each other may be greater than a region, described with reference to FIG. **6**A, in which the second gate electrode GE**2** and the semiconductor pattern SP overlap each other. As a result, the gate-induced drain leakage (GIDL) phenomenon in the region of the semiconductor pattern SP adjacent to the second gate electrode GE**2** may be reduced further than that described with reference to FIG. **6**A.
[0066] Referring to FIG. **6**C, the third width W**3** may be greater than the second width W**2**. The third width W**3** may be greater than the third width W**3** in FIG. **6**A. Accordingly, a region in which the third gate electrode GE**3** and the semiconductor pattern SP overlap each other may be greater than a region, described with reference to FIG. **6**A, in which the third gate electrode GE**3** and the semiconductor patterns SP overlap each other. As a result, the gate-induced drain leakage (GIDL) phenomenon in the region of the semiconductor pattern SP adjacent to the third gate electrode GE**3** may be reduced further than that described with reference to FIG. **6**A.
[0067] Referring to FIGS. **3** to **5**B again, the bit line BL may be provided on the first side surface S**1** (e.g., a side surface of the first edge portion EA**1**) of the semiconductor pattern SP. The bit line BL may extend along the first side surface S**1** of the semiconductor pattern SP in the third direction D**3**. Accordingly, one bit line BL may be in contact with and may be electrically connected to the first side surface S**1** of each of the semiconductor patterns SP adjacent to each other in the third direction D**3**. The bit line BL may be provided in plurality. The bit lines BL may be adjacent to each other along the second direction D**2**.
[0068] The bit line BL may be a single film including one material or a composite film including at least two materials. For example, the bit line BL may include or be formed of at least one of a metal material (for example, Ti, Mo, W, Cu, Al, Ta, Ru, Ir, Co, or the like), a metal nitride (for example, a nitride of Ti, Mo, W, Cu, Al, Ta, Ru, Ir, Co, or the like), or a metal silicide (for example, a silicide of Ti, Mo, W, Cu, Al, Ta, Ru, Ir, Co, or the like).
[0069] The bit lines BL may include, in the first stack structure ST**1**, a first bit line BLa provided on the first side surface S**1** of the first semiconductor pattern SPa, and a second bit line BLb provided on the first side surface S**1** of the second semiconductor pattern SPb.
[0070] The data storage pattern DSP may be interposed between the first stack structure ST**1** and

the second stack structure ST**2**. The data storage pattern DSP may be interposed between the first semiconductor pattern SPa and the second semiconductor pattern SPb. The data storage pattern DSP may be in contact with the second side surface S**2** (e.g., a side surface of the second edge portion EA**2**) of the first semiconductor pattern SPa, and may be electrically connected to the first semiconductor pattern SPa. The data storage pattern DSP may be in contact with the second side surface S**2** of the second semiconductor pattern SPb, and may be electrically connected to the second semiconductor pattern SPb.

[0071] The data storage pattern DSP may include a storage electrode SE, a plate electrode PE, and a capacitor dielectric film CIL therebetween. For example, the three-dimensional semiconductor device may be a dynamic random access memory (DRAM), and in this case, the data storage pattern DSP may be used as a capacitor. The storage electrode SE may be spaced apart from the plate electrode PE by the capacitor dielectric film CIL.

[0072] The storage electrode SE and the plate electrode PE may each include a conductive material. For example, the storage electrode SE and the plate electrode PE may each include or be formed of at least one of silicon (Si) doped with an impurity, silicon germanium (SiGe) doped with an impurity, a metal material (for example, Ti, Mo, W, Cu, Al, Ta, Ru, Ir, Co, Pt, Au, Ag, or the like), a metal nitride (for example, a nitride of Ti, Mo, W, Cu, Al, Ta, Ru, Ir, Co, Pt, Au, Ag, or the like), titanium silicon nitride (for example, TiSiN), titanium aluminum nitride (for example, TiAlN), tantalum aluminum nitride (for example, TaAlN, or the like), a conductive oxide (for example, PtO, RuO.sub.2, IrO.sub.2, SRO(SrRuO.sub.3), BSRO((Ba,Sr)RuO.sub.3), CRO(CaRuO.sub.3), LSCo), or a metal silicide. The storage electrode SE and the plate electrode PE may be each a single film composed of a single material, or a composite film including at least two materials.

[0073] As an example, the capacitor dielectric film CIL may include or be at least one of a metal oxide such as HfO.sub.2, ZrO.sub.2, Al.sub.2O.sub.3, La.sub.2O.sub.3, Ta.sub.2O.sub.3, and TiO.sub.2, or a dielectric material, having a perovskite structure, such as SrTiO.sub.3 (STO), (Ba,Sr) TiO.sub.3 (BST), BaTiO.sub.3, PZT, PLZT.

[0074] As another example, the data storage pattern DSP may be a variable resistor pattern capable of being switched to two resistance states by an electrical pulse. In this case, the data storage pattern DSP may include a phase-change material of which a crystalline state is changed according to an amount of current, a perovskite compound, a transition metal oxide, a magnetic material, a ferromagnetic material, or an antiferromagnetic material.

[0075] The storage electrode SE may extend on the second side surface S**2** of the first semiconductor pattern SPa along the first direction D**1** and may protrude from the second side surface S**2** of the first semiconductor pattern SPa toward the second stack structure ST**2** in the first direction D**1**. The storage electrode SE may extend on the second side surface S**2** of the second semiconductor pattern SPb along the first direction D**1** and may protrude from the second side surface S**2** of the second semiconductor pattern SPb toward the first stack structure ST**1** in the first direction D**1**. Although not shown in the drawing, a silicide pattern (not shown) may be provided between the storage electrode SE and the first semiconductor pattern SPa, and the storage electrode SE and the second semiconductor pattern SPb. The silicide pattern may include a metal silicide (for example, a silicide of Ti, Mo, W, Cu, Al, Ta, Ru, Ir, Co, or the like). The storage electrode SE may be provided in plurality, and the storage electrodes SE may be adjacent to each other in the third direction D**3**.

[0076] The plate electrode PE may include a region partially extending along the third direction D**3**, and another region protruding from the region in the first direction D**1** or an opposite direction of the first direction D**1**. The other region of the plate electrode PE may be interposed between the storage electrodes SE adjacent to each other in the third direction D**3**.

[0077] The buried insulating pattern **110** may be provided on the substrate **100**. The buried insulating pattern **110** may cover a side surface of the cell array structure CS. The buried insulating

pattern **110** may be interposed between the bit line BL and the word line WL, between the semiconductor patterns SP adjacent to each other in the third direction D**3**, between the first edge portions EA**1** of the semiconductor patterns SP adjacent to each other in the second direction D**2**, and between the word lines WL adjacent to each other in the third direction D**3**. The buried insulating pattern **110** may be or include a single film or a composite film including an insulating material.

[0078] A capping pattern CP may be provided in the cell array structure CS. The capping pattern CP may be interposed between the word lines WL and the data storage pattern DSP. The capping pattern CP may be interposed between the semiconductor patterns SP adjacent to each other in the third direction D**3**. The capping pattern CP may be interposed between the second edge portions EA**2** of the semiconductor patterns SP adjacent to each other in the second direction D**2**.

[0079] The capping pattern CP may include a first capping pattern CP**1** surrounding the second edge portion EA**2** of the semiconductor pattern SP, and a second capping pattern CP**2** on the first capping pattern CP**1**. The first capping pattern CP**1** may conformally cover the second edge portion EA**2** of the semiconductor pattern SP and a side surface of the word line WL. The first capping pattern CP**1** and the second capping pattern CP**2** may each include an insulating material. The second capping pattern CP**2** may be or include a single film or a composite film.

[0080] A protective film PL may be provided on the cell array structure CS. The protective film PL may cover upper surfaces of the first stack structure ST**1**, the second stack structure ST**2**, and the data storage pattern DSP. The protective film PL may include a single film or a composite film including an insulating material. A plurality of upper lines (not shown) may be included in the protective film PL. A portion of the upper conductive lines may be electrically connected to the bit line BL, and the other portion of the upper conductive lines may be electrically connected to the data storage pattern DSP. In addition, although not shown in the drawing, word line pads (not shown) may be provided on a side surface of the cell array structure CS, and may be electrically connected to the word lines WL.

[0081] Hereinafter, a method for manufacturing a three-dimensional semiconductor device according to an embodiment of the inventive concept will be described with reference to FIGS. **7** to **20**. In order to simplify description, description duplicated with those made above will be omitted, and differences will be mainly described.

[0082] FIGS. **7** to **20** are diagrams illustrating a method for manufacturing a three-dimensional semiconductor device according to an embodiment of the inventive concept. More particularly, FIGS. **7** and **16** are cross-sectional views corresponding to line A-A′ in FIG. **3**. FIGS. **8**, **10**, **12**, **14**, **17**, and **19** are plan views of the three-dimensional semiconductor device according to an embodiment of the inventive concept. FIGS. **9**A, **11**A, **13**, **15**A, **18**A, and **20** are respectively cross-sectional views corresponding to line A-A′ in FIGS. **8**, **10**, **12**, **14**, **17**, and **19**. FIGS. **9**B, **11**B, **15**B, and **18**B are respectively cross-sectional views corresponding to line B-B′ in FIGS. **8**, **10**, **14**, and **17**.

[0083] Referring to FIGS. **3** and **7**, a substrate **100** may be prepared. Sacrificial layers SAL and active layers ACL may be formed to be alternately stacked on the substrate **100**. The sacrificial layers SAL and the active layers ACL may each include or be a semiconductor material. The sacrificial layers SAL may include or be a material capable of having an etching selectivity with the active layers ACL. Accordingly, when a process of removing the sacrificial layers SAL to be described later is performed, even if the sacrificial layers SAL are removed, the active layers ACL may not be removed or may be removed less than the sacrificial layers SAL. For example, the active layers ACL may include or be one among silicon (Si), germanium (Ge), and silicon germanium (SiGe), and the sacrificial layers SAL may include or be one, different from the active layers ACL, among silicon (Si), germanium (Ge), and silicon germanium (SiGe). For example, the active layers ACL may be silicon (Si), and the sacrificial layers SAL may be silicon germanium (SiGe). The sacrificial layers SAL may have a greater thickness than the active layers ACL with

respect to the third direction D**3**.
[0084] Referring to FIGS. **8** to **9**B, first holes HL**1** may be formed on the substrate **100** by partially removing each of the sacrificial layers SAL and the active layers ACL. The first holes HL**1** may be formed to be adjacent to each other in the first and second directions D**1** and D**2**. An upper surface of the substrate **100** may be partially exposed to the outside by the first holes HL**1**. Through the removing process, the sacrificial layers SAL and the active layers ACL may be formed to include regions extending long in the first direction D**1** and regions extending long in the second direction D**2**.
[0085] First preliminary filling patterns PF**1** may partially cover the exposed upper surface of the substrate **100**, and may be formed to fill the inside of the first holes HL**1**. For example, the first preliminary filling pattern PF**1** may include or be an insulating material. The first preliminary filling patterns PF**1** may be formed to be adjacent to each other in the first and second directions D**1** and D**2**.
[0086] Second holes HL**2** may be formed on the substrate **100** by partially removing regions, among the sacrificial layers SAL and the active layers ACL, extending long in the second direction D**2**. The second holes HL**2** may be formed to extend along the second direction D**2**. Both of side surfaces of the sacrificial layers SAL and the active layers ACL may be exposed to the outside by the second holes HL**2**. During a process of forming the second holes HL**2**, an upper portion of the substrate **100** may be partially recessed to a predetermined depth. The upper surface of the substrate **100** may be partially exposed to the outside by the second holes HL**2**.
[0087] Referring to FIGS. **10** to **11**B, both of the exposed side surfaces of the sacrificial layers SAL may be selectively removed through the second holes HL**2**. Accordingly, first internal regions INR**1** may be formed between the active layers ACL adjacent to each other in the third direction D**3**. During the process of removing, each of the first preliminary filling patterns PF**1** may be partially removed at the same time. The sidewalls of the first preliminary filling patterns PF**1** may be aligned with sidewalls of the sacrificial layers SAL.
[0088] A second preliminary filling pattern PF**2** may be formed to fill the first internal regions INR**1**, a region in which the first preliminary filling patterns PF**1** are partially removed, and the inside of the second holes HL**2**. The second preliminary filling pattern PF**2** may cover and surround the active layers ACL not vertically overlapping the sacrificial layers SAL. The second preliminary filling pattern PF**2** may include a single film or composite film including an insulating material. For example, the second preliminary filling pattern PF**2** may include or be formed of at least one of silicon oxide or silicon nitride.
[0089] Referring to FIGS. **12** and **13**, a third hole HL**3** may be formed on the substrate **100** by removing a region, among the sacrificial layers SAL and the active layers ACL, extending long in the second direction D**2**. During a process of forming the third holes HL**3**, one active layer ACL may be separated to the semiconductor patterns SP adjacent to each other in the second direction D**2**. The semiconductor pattern SP may include the first semiconductor pattern SPa and the second semiconductor pattern SPb adjacent to each other in the first direction D**1**. During the process of forming the third holes HL**3**, the sacrificial layers SAL may be exposed to the outside again.
[0090] The exposed sacrificial layers SAL may be entirely removed on the substrate **100** through the third holes HL**3**. Accordingly, second internal regions INR**2** may be formed between a few regions of the active layers ACL not overlapping the second preliminary filling pattern PF**2**. During the process of removing, the first preliminary filling patterns PF**1** may be entirely removed on the substrate **100**. Thereafter, a third preliminary filling pattern PF**3** may be formed to fill the second internal regions INR**2**, a region in which the first preliminary filling patterns PF**1** are removed, and the inside of the third holes HL**3**. The third preliminary filling pattern PF**3** may include a single film or composite film including an insulating material. For example, the third preliminary filling pattern PF**3** may include at least one of silicon oxide or silicon nitride.
[0091] Referring to FIGS. **14** to **15**B, the second preliminary filling pattern PF**2** may be removed

on the substrate **100**. Thereafter, the gate dielectric film Gox and preliminary gate conductive films PGLa and PGLb may be sequentially formed in the first internal regions INR**1**. The gate dielectric film Gox and the preliminary gate conductive films PGLa and PGLb may be formed to partially sequentially conformally cover the semiconductor pattern SP. The gate dielectric film Gox and the preliminary gate conductive films PGLa and PGLb may be formed to partially cover and surround the semiconductor pattern SP. One gate dielectric film Gox and one preliminary gate conductive film PGLa or PGLb may be formed to partially cover and surround each of the semiconductor patterns SP adjacent to each other in the second and third directions D**2** and D**3**. Thereafter, the buried insulating pattern **110** may be formed in a region in which the first internal regions INR**1** and the second preliminary filling pattern PF**2** are removed.

[0092] The bit lines BL may be formed to penetrate the buried insulating pattern **110** and be in contact with one side surfaces of the semiconductor patterns SP. The bit lines BL may include first bit lines BLa in contact with the first semiconductor patterns SPa and the second bit lines BLb in contact with the second semiconductor patterns SPb.

[0093] Referring to FIGS. **3** and **16**, the third preliminary filling pattern PF**3** may be removed on the substrate **100**. During the process of removing, the gate dielectric film Gox and the preliminary gate conductive films PGLa and PGLb may be removed together. Accordingly, one gate dielectric film Gox may be separated to a plurality of gate dielectric films Gox adjacent to each other in the second and third directions D**2** and D**3**. In addition, one preliminary gate conductive film PGLa or PGLb may be separated to a plurality of preliminary gate electrodes PGEa and PGEb adjacent to each other in the second and third directions D**2** and D**3**. The gate dielectric film Gox may surround a corresponding semiconductor pattern SP among the semiconductor patterns SP. The preliminary gate electrodes PGEa and PGEb may surround a corresponding semiconductor pattern SP among the semiconductor patterns SP.

[0094] During the process of removing, the second internal regions INR**2** may be exposed to the outside. One side surface of each of the preliminary gate electrodes PGEa and PGEb may be exposed to the outside by the second internal regions INR**2**.

[0095] The preliminary gate electrodes PGEa and PGEb may include first preliminary gate electrodes PGEa surrounding the first semiconductor patterns SPa and second preliminary gate electrodes PGEb surrounding the second semiconductor patterns SPb.

[0096] Referring to FIGS. **17** to **18**B, a process of removing a portion of each of the preliminary gate electrodes PGEa and PGEb exposed by the second internal regions INR**2** may be performed. After the process of removing, a remaining portion of each of the preliminary gate electrodes PGEa and PGEb may constitute the second gate electrodes GE**2** described with reference to FIGS. **3** to **5**B. Thereafter, the first gate electrode GE**1** and the third gate electrode GE**3** may be sequentially formed on a side surface of each of the second gate electrodes GE**2**. The first gate electrode GE**1** and the third gate electrode GE**3** may be formed to surround the semiconductor pattern SP.

[0097] The gate dielectric film Gox and the first to third gate electrodes GE**1**, GE**2**, and GE**3** surrounding the first semiconductor pattern SPa may constitute the first word line WLa. The gate dielectric film Gox and the first to third gate electrodes GE**1**, GE**2**, and GE**3** surrounding the second semiconductor pattern SPb may constitute the second word line WLb.

[0098] A region, of the first semiconductor pattern SPa, surrounded by the first word line WLa may constitute the channel region CH of the first semiconductor pattern SPa. A region, of the second semiconductor pattern SPb, surrounded by the second word line WLb may constitute the channel region CH of the second semiconductor pattern SPb.

[0099] Referring to FIGS. **19** and **20**, the capping pattern CP may be formed to fill a region in which the second internal regions INR**2** and the third preliminary filling pattern PF**3** are removed. The capping pattern CP may include a first capping pattern CP**1** conformally covering the second internal regions INR**2** and the second edge portion EA**2** of the semiconductor patterns SP, and a second capping pattern CP**2** filling the remining portion of the second internal regions INR**2** and

surrounding the second edge portion EA**2** of the semiconductor patterns SP.
[0100] Thereafter, a fourth hole HL**4** may be formed on the substrate **100** by partially removing the capping pattern CP. The fourth hole HL**4** may be formed to extend along the second direction D**2**. The second edge portions EA**2** of the semiconductor patterns SP may be exposed to the outside by the fourth hole HL**4**.
[0101] A process of partially removing the exposed second edge portions EA**2** of the semiconductor patterns SP may be performed by the fourth hole HL**4**. During the process of removing, a process of partially removing the first capping pattern CP**1** may be performed together.
[0102] The storage electrodes SE may be formed on the second edge portions EA**2** of the semiconductor patterns SP. For example, forming the storage electrodes SE may include forming silicide patterns (not shown) on the second edge portions EA**2** of the semiconductor patterns SP, and forming the storage electrode SE through a selective epitaxial growth (SEG) process using the silicide patterns as seeds.
[0103] Referring to FIGS. **3** to **5**B again, a process of partially removing the second capping pattern CP**2** may be performed. Accordingly, a side surface of the second capping pattern CP**2** may be aligned with a side surface of the second edge portion EA**2** of the semiconductor pattern SP. Thereafter, the capacitor dielectric film CIL may be formed to conformally cover the storage electrodes SE. The plate electrode PE may be formed to cover the space between the storage electrodes SE, and a remaining portion of the fourth hole HL**4** described with reference to FIGS. **19** and **20**. The storage electrode SE, the capacitor dielectric film CIL, and the plate electrode PE may constitute the data storage pattern DSP. Thereafter, the protective film PL may be formed to cover the cell array structure CS.
[0104] According to aspects of the inventive concept, a word line may include a first gate electrode, a second gate electrode on one side surface of the first gate electrode, and a third gate electrode on the other side surface of the first gate electrode. A work function of each of the second gate electrode and the third gate electrode may be smaller than a work function of the first gate electrode. Accordingly, during an operation of a three-dimensional semiconductor device, a gate-induced drain leakage (GIDL) phenomenon generated in a semiconductor pattern may be reduced. As a result, an amount of holes accumulated in the semiconductor pattern may decrease so that a leakage current caused by the holes may be reduced. Accordingly, reliability of the three-dimensional semiconductor device may be improved.
[0105] The above description of embodiments of the inventive concept provides an example for description of the inventive concept. Therefore, the inventive concept is not limited to the above embodiments, and it is obvious that various modifications and changes such as combining the above embodiments may be made by those skilled in the art within the technical spirit of the inventive concept.

Claims

1. A three-dimensional semiconductor device comprising: a semiconductor pattern spaced apart from a substrate and extending along a first direction parallel to a lower surface of the substrate; a word line surrounding the semiconductor pattern and extending along a second direction parallel to the lower surface of the substrate and crossing the first direction; and a bit line extending along a first side surface of the semiconductor pattern along a third direction perpendicular to the lower surface of the substrate, wherein the word line includes: a first gate electrode, a second gate electrode on a first side surface of the first gate electrode, and a third gate electrode on a second side surface opposite to the first side surface of the first gate electrode, and wherein a work function of each of the second and third gate electrodes is smaller than a work function of the first gate electrode.
2. The three-dimensional semiconductor device of claim 1, wherein the second gate electrode and

the third gate electrode comprise different materials.
3. The three-dimensional semiconductor device of claim 1, wherein the work function of the second gate electrode is smaller than the work function of the third gate electrode.
4. The three-dimensional semiconductor device of claim 1, wherein the work function of the third gate electrode is smaller than the work function of the second gate electrode.
5. The three-dimensional semiconductor device of claim 1, wherein with respect to the first direction, a width of the second gate electrode is greater than a width of the third gate electrode.
6. The three-dimensional semiconductor device of claim 1, wherein with respect to the first direction, a width of the third gate electrode is greater than a width of the second gate electrode.
7. The three-dimensional semiconductor device of claim 1, further comprising a data storage pattern on a second side surface opposite to the first side surface of the semiconductor pattern.
8. The three-dimensional semiconductor device of claim 1, wherein the first gate electrode comprises at least one of Ti, TiN, TiSiN, TiON, W, WN, Mo, MON, MoO.sub.xN.sub.y, Ta, TaN, or poly Si.
9. The three-dimensional semiconductor device of claim 1, wherein the second gate electrode comprises at least one of Li, Na, K, Cs, Rb, Sr, Ba, Ca, Ce, Sm, Eu, Mg, Sc, Y, Hf, Tl, As, La, Nd, Gd, Tb, Lu, Th, U, Mn, Al, Ga, In, Pb, Cd, Bi, Zr, Ti, TiN, or poly Si doped with an N-type conductive impurity and the third gate electrode comprises at least one of Li, Na, K, Cs, Rb, Sr, Ba, Ca, Ce, Sm, Eu, Mg, Sc, Y, Hf, Tl, As, La, Nd, Gd, Tb, Lu, Th, U, Mn, Al, Ga, In, Pb, Cd, Bi, Zr, Ti, TiN, or poly Si doped with an N-type conductive impurity.
10. A three-dimensional semiconductor device comprising: a semiconductor pattern spaced apart from a substrate and extending along a first direction parallel to a lower surface of the substrate; a word line surrounding the semiconductor pattern and extending along a second direction parallel to the lower surface of the substrate and crossing the first direction; and a bit line extending along a first side surface of the semiconductor pattern along a third direction perpendicular to the lower surface of the substrate, wherein the word line includes: a first gate electrode including a first material, a second gate electrode provided on a first side surface of the first gate electrode and including a second material, and a third gate electrode provided on a second side surface opposite to the first side surface of the first gate electrode and including a third material, the first material includes a material different from the second and third materials, and wherein a work function of each of the second material and the third material is smaller than a work function of the first material.
11. The three-dimensional semiconductor device of claim 10, wherein the first material comprises at least one of Ti, TIN, TiSiN, TiON, W, WN, Mo, MON, MoO.sub.xN.sub.y, Ta, TaN, or poly Si.
12. The three-dimensional semiconductor device of claim 10, wherein the second material comprises at least one of Li, Na, K, Cs, Rb, Sr, Ba, Ca, Ce, Sm, Eu, Mg, Sc, Y, Hf, Tl, As, La, Nd, Gd, Tb, Lu, Th, U, Mn, Al, Ga, In, Pb, Cd, Bi, Zr, Ti, TiN, or poly Si doped with an N-type conductive impurity, and the third material comprises at least one of Li, Na, K, Cs, Rb, Sr, Ba, Ca, Ce, Sm, Eu, Mg, Sc, Y, Hf, Tl, As, La, Nd, Gd, Tb, Lu, Th, U, Mn, Al, Ga, In, Pb, Cd, Bi, Zr, Ti, TiN, or poly Si doped with an N-type conductive impurity.
13. The three-dimensional semiconductor device of claim 10, wherein the second material and the third material comprise different materials.
14. The three-dimensional semiconductor device of claim 10, wherein the work function of the second material is smaller than the work function of the third material.
15. The three-dimensional semiconductor device of claim 10, wherein the work function of the third material is smaller than the work function of the second material.
16. The three-dimensional semiconductor device of claim 10, wherein with respect to the first direction, a width of the second gate electrode is greater than a width of the third gate electrode.
17. The three-dimensional semiconductor device of claim 10, wherein with respect to the first direction, a width of the third gate electrode is greater than a width of the second gate electrode.

18. A three-dimensional semiconductor device comprising: a first stack structure on a substrate, and a second stack structure adjacent to the first stack structure in a first direction parallel to a lower surface of the substrate; and a data storage pattern between the first stack structure and the second stack structure, wherein the first stack structure includes: a first semiconductor pattern spaced apart from the substrate and extending along the first direction, a first word line surrounding the first semiconductor pattern and extending along a second direction parallel to the lower surface of the substrate and crossing the first direction, and a first bit line extending along a first side surface of the first semiconductor pattern along a third direction perpendicular to the lower surface of the substrate, wherein the first word line includes: a first gate electrode, a second gate electrode on a first side surface of the first gate electrode, and a third gate electrode on a second side surface opposite to the first side surface of the first gate electrode, and a work function of each of the second and third gate electrodes is smaller than a work function of the first gate electrode.
19. The three-dimensional semiconductor device of claim 18, wherein the second stack structure comprises: a second semiconductor pattern spaced apart from the substrate and extending along the first direction; a second word line surrounding the second semiconductor pattern and extending along the second direction; and a second bit line extending on one side surface of the second semiconductor pattern along the third direction.
20. The three-dimensional semiconductor device of claim 18, wherein the second and third gate electrodes comprise different materials, and/or widths of the second and third gate electrodes along the first direction are different from each other.