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INTEGRATED CIRCUIT STRUCTURE WITH DIRECT BACKSIDE SOURCE OR DRAIN CONTACT ENABLED BY SILICON GERMANIUM ETCH STOP

Abstract

Integrated circuit structures having direct backside source or drain contacts are described. In an example, an integrated circuit structure includes first and second pluralities of horizontally stacked nanowires or fins, and first and second gate stacks. An epitaxial source or drain structure is between the first plurality of horizontally stacked nanowires or fin and the second plurality of horizontally stacked nanowires or fin, the epitaxial source or drain structure over and electrically coupled to a corresponding conductive backside contact that extends laterally beyond the epitaxial source or drain structure without contacting the first gate stack or the second gate stack.

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Background/Summary

BACKGROUND

[0001] For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips. For example, shrinking transistor size allows for the incorporation of an increased number of memory or logic devices on a chip, lending to the fabrication of products with increased capacity. The drive for ever-more capacity, however, is not without issue. The necessity to optimize the performance of each device becomes increasingly significant.

[0002] Variability in conventional and currently known fabrication processes may limit the possibility to further extend them into the 10 nanometer node or sub-10 nanometer node range. Consequently, fabrication of the functional components needed for future technology nodes may require the introduction of new methodologies or the integration of new technologies in current fabrication processes or in place of current fabrication processes.

[0003] In the manufacture of integrated circuit devices, multi-gate transistors, such as tri-gate transistors, have become more prevalent as device dimensions continue to scale down. Tri-gate transistors are generally fabricated on either bulk silicon substrates or silicon-on-insulator substrates. In some instances, bulk silicon substrates are preferred due to their lower cost and compatibility with the existing high-yielding bulk silicon substrate infrastructure.

[0004] Scaling multi-gate transistors has not been without consequence, however. As the dimensions of these fundamental building blocks of microelectronic circuitry are reduced and as the sheer number of fundamental building blocks fabricated in a given region is increased, the constraints on the semiconductor processes used to fabricate these building blocks have become overwhelming.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIGS. **1**A-**1**G illustrate angled cross-sectional views representing various operations in methods of fabricating an integrated circuit structure having direct backside source or drain contacts, in accordance with an embodiment of the present disclosure.

[0006] FIG. **2**A illustrates cross-sectional views representing various operations in a method of fabricating a nanowire and release layer stack including a bottom etch stop layer, in accordance with an embodiment of the present disclosure.

[0007] FIG. **2**B illustrates cross-sectional views representing various operations in another method of fabricating a nanowire and release layer stack including a bottom etch stop layer, in accordance with another embodiment of the present disclosure.

[0008] FIG. **3** illustrates cross-sectional views of an interconnect stack having front side power delivery and of an interconnect stack having backside power delivery, in accordance with an embodiment of the present disclosure.

[0009] FIGS. **4**-**9** illustrate angled cross-sectional views representing various operations in methods

of fabricating an integrated circuit structure having differentiated backside source or drain contact access features, in accordance with an embodiment of the present disclosure.
[0010] FIG. **10**A illustrates a plan view of a semiconductor device having a gate contact disposed over an inactive portion of a gate electrode.
[0011] FIG. **10**B illustrates a cross-sectional view of a non-planar semiconductor device having a gate contact disposed over an inactive portion of a gate electrode.
[0012] FIG. **11**A illustrates a plan view of a semiconductor device having a gate contact via disposed over an active portion of a gate electrode, in accordance with an embodiment of the present disclosure.
[0013] FIG. **11**B illustrates a cross-sectional view of a non-planar semiconductor device having a gate contact via disposed over an active portion of a gate electrode, in accordance with an embodiment of the present disclosure.
[0014] FIGS. **12**A-**12**J illustrates cross-sectional views of various operations in a method of fabricating a gate-all-around integrated circuit structure, in accordance with an embodiment of the present disclosure.
[0015] FIG. **13** illustrates a computing device in accordance with one implementation of the disclosure.
[0016] FIG. **14** illustrates an interposer that includes one or more embodiments of the disclosure.
[0017] FIG. **15** is an isometric view of a mobile computing platform employing an IC fabricated according to one or more processes described herein or including one or more features described herein, in accordance with an embodiment of the present disclosure.
[0018] FIG. **16** illustrates a cross-sectional view of a flip-chip mounted die, in accordance with an embodiment of the present disclosure.

DESCRIPTION OF THE EMBODIMENTS

[0019] Integrated circuit structures having direct backside source or drain contacts are described. In the following description, numerous specific details are set forth, such as specific integration and material regimes, in order to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to one skilled in the art that embodiments of the present disclosure may be practiced without these specific details. In other instances, well-known features, such as integrated circuit design layouts, are not described in detail in order to not unnecessarily obscure embodiments of the present disclosure. Furthermore, it is to be appreciated that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.
[0020] The following detailed description is merely illustrative in nature and is not intended to limit the embodiments of the subject matter or the application and uses of such embodiments. As used herein, the word “exemplary” means “serving as an example, instance, or illustration.” Any implementation described herein as exemplary is not necessarily to be construed as preferred or advantageous over other implementations. Furthermore, there is no intention to be bound by any expressed or implied theory presented in the preceding technical field, background, brief summary or the following detailed description.
[0021] This specification includes references to “one embodiment” or “an embodiment.” The appearances of the phrases “in one embodiment” or “in an embodiment” do not necessarily refer to the same embodiment. Particular features, structures, or characteristics may be combined in any suitable manner consistent with this disclosure.
[0022] Terminology. The following paragraphs provide definitions or context for terms found in this disclosure (including the appended claims):
[0023] “Comprising.” This term is open-ended. As used in the appended claims, this term does not foreclose additional structure or operations.
[0024] “Configured To.” Various units or components may be described or claimed as “configured to” perform a task or tasks. In such contexts, “configured to” is used to connote structure by

indicating that the units or components include structure that performs those task or tasks during operation. As such, the unit or component can be said to be configured to perform the task even when the specified unit or component is not currently operational (e.g., is not on or active). Reciting that a unit or circuit or component is "configured to" perform one or more tasks is expressly intended not to invoke 35 U.S.C. § 112, sixth paragraph, for that unit or component.
[0025] "First," "Second," etc. As used herein, these terms are used as labels for nouns that they precede, and do not imply any type of ordering (e.g., spatial, temporal, logical, etc.).
[0026] "Coupled"—The following description refers to elements or nodes or features being "coupled" together. As used herein, unless expressly stated otherwise, "coupled" means that one element or node or feature is directly or indirectly joined to (or directly or indirectly communicates with) another element or node or feature, and not necessarily mechanically.
[0027] In addition, certain terminology may also be used in the following description for the purpose of reference only, and thus are not intended to be limiting. For example, terms such as "upper", "lower", "above", and "below" refer to directions in the drawings to which reference is made. Terms such as "front", "back", "rear", "side", "outboard", and "inboard" describe the orientation or location or both of portions of the component within a consistent but arbitrary frame of reference which is made clear by reference to the text and the associated drawings describing the component under discussion. Such terminology may include the words specifically mentioned above, derivatives thereof, and words of similar import.
[0028] "Inhibit"—As used herein, inhibit is used to describe a reducing or minimizing effect. When a component or feature is described as inhibiting an action, motion, or condition it may completely prevent the result or outcome or future state completely. Additionally, "inhibit" can also refer to a reduction or lessening of the outcome, performance, or effect which might otherwise occur. Accordingly, when a component, element, or feature is referred to as inhibiting a result or state, it need not completely prevent or eliminate the result or state.
[0029] Embodiments described herein may be directed to front-end-of-line (FEOL) semiconductor processing and structures. FEOL is the first portion of integrated circuit (IC) fabrication where the individual devices (e.g., transistors, capacitors, resistors, etc.) are patterned in the semiconductor substrate or layer. FEOL generally covers everything up to (but not including) the deposition of metal interconnect layers. Following the last FEOL operation, the result is typically a wafer with isolated transistors (e.g., without any wires).
[0030] Embodiments described herein may be directed to back-end-of-line (BEOL) semiconductor processing and structures. BEOL is the second portion of IC fabrication where the individual devices (e.g., transistors, capacitors, resistors, etc.) get interconnected with wiring on the wafer, e.g., the metallization layer or layers. BEOL includes contacts, insulating layers (dielectrics), metal levels, and bonding sites for chip-to-package connections. In the BEOL part of the fabrication stage contacts (pads), interconnect wires, vias and dielectric structures are formed. For modern IC processes, more than 10 metal layers may be added in the BEOL.
[0031] Embodiments described below may be applicable to FEOL processing and structures, BEOL processing and structures, or both FEOL and BEOL processing and structures. In particular, although an exemplary processing scheme may be illustrated using a FEOL processing scenario, such approaches may also be applicable to BEOL processing. Likewise, although an exemplary processing scheme may be illustrated using a BEOL processing scenario, such approaches may also be applicable to FEOL processing.
[0032] One or more embodiments are directed to backside (BS) contacts with deep source or drain (SD) enabled with silicon germanium (SiGe) etch stop (ES) layers. One or more embodiments are directed to direct backside (BS) source drain contact enabled by increased process margin with backside gate recess. One or more embodiments described herein are directed to gate-all-around integrated circuit structures fabricated to have direct backside source or drain contacts. It is to be appreciated that, unless indicated otherwise, reference to nanowires herein can indicate nanowires

or nanoribbons or nanosheets or forksheets. One or more embodiments described herein are directed to fin-based integrated circuit structures fabricated to have direct backside source or drain contacts.

[0033] To provide context, backside (BS) power delivery decouples power wires and signal wires, allowing de-congestion of BEOL leading to further scaling of standard cells and reduction of on-chip IR droop. Nanometal vias or trenches running parallel to the standard cell are typically used to deliver the power back to the front side of the transistor.

[0034] In accordance with one or more embodiments described herein, instead of delivering power from the backside to the front side via nanometal vias or trenches, a direct power delivery is provided to a source region from the backside to offer an improved scaling option, both dimensionally and electrically. This can be achieved by direct patterning and etching of a backside (BS) via to connect the backside power wires directly to the source of the transistor. However, the proximity of gate bottom and the source bottom may require a very stringent EPE control to avoid via shorting to the gate and can pose a key limiter to enable direct source via connection. Additionally, a non-uniformity of a source/drain depth can lead to unlanded backside contact.

[0035] In an embodiment, a process flow and strategy are described to provide extended source/drain depth and backside gate recess to widen a process margin, enabling direct source connection from the backside.

[0036] To provide further context, previous approaches have involved nanometal vias or trenches running parallel to the standard cell to deliver the power to the source at the front side of the transistor. In particular, a deep trench is etched after a spacer etch and prior to SD epitaxy. The trench is then filled with a dummy metal which gets revealed during BS processing and replaced with contact metal. Disadvantages to such approaches can include the nanometal vias or trenches consuming cell area footprint and increasing the standard cell area. Also, the BS source contact formation through front side processing can add process complexity.

[0037] In an embodiment, a process scheme for increasing the source/drain depth and a backside gate etch is described. This increases the process margin and thus enables direct patterning of contact via to the source of the transistor from the backside. Advantages for implementing embodiments described herein can include simplification of a process flow and increased process margin to allow backside contact of source/drain, thus enabling direct BS power contact and delivery. Reducing the gate height (from the backside) can also reduce the parasitic capacitance (performance benefit).

[0038] As an exemplary processing scheme, FIGS. **1**A-**1**G illustrate angled cross-sectional views representing various operations in methods of fabricating an integrated circuit structure having direct backside source or drain contacts, in accordance with an embodiment of the present disclosure. It is to be appreciated that the embodiments described and illustrated may also be applicable for a fin structure in place of a stack of nanowires or nanoribbons or nanosheets or forksheets.

[0039] Referring to FIG. **1**A, a starting structure **100** includes stacks of nanowires **106**, such as stacks of silicon nanowires, which may be over a corresponding doped silicon structure **105**. The doped silicon structure **105** is on an etch stop layer **103**, such as silicon germanium etch stop layer. The etch stop layer **103** is on a corresponding sub-fin structure **102**, such as a silicon sub-fin structure, which can be within trench isolation structures **104**. A gate electrode **108**, such as a metal gate electrode which can include a workfunction layer and a conductive fill, is around the nanowires **106**. The gate electrode **108** is separated from the nanowires **106** by a gate dielectric layer, such as a high-k gate dielectric layer. A dielectric gate cap **114** can be included on the gate electrodes, as is depicted. Dielectric gate sidewall spacers, such as silicon nitride gate sidewall spacers, can be along sides of the gate electrodes **108**. Internal portions of gate sidewalls spacers can also be included vertically between adjacent nanowires.

[0040] Starting structure **100** can also include epitaxial source or drain structures **110**, such as

epitaxial silicon or silicon germanium source or drain structures, at ends of the stacks of nanowires **106**. In the case of silicon germanium source or drain structures, in one embodiment, the etch stop layer **103** has a different SiGe composition than the silicon germanium source or drain structures. Corresponding conductive trench contacts **116** are over and coupled to the epitaxial source or drain structures **110**.

[0041] Starting structure **100** also includes dielectric gate cut plugs **112**. Gate contacts **118** are included in a dielectric layer **120**. An upper portion of the structure **100** includes lower conductive lines **122**, conductive vias **124**, and upper conductive lines **126**, in various dielectric layer stacks **128**. At this stage in the process, from the bottom or backside, the starting structure **100** has been subjected to planarization to remove a bulk silicon substrate.

[0042] Referring to FIG. **1**B, the starting structure **100** is subjected to recessing of the dielectric gate cut plugs **112** to form recessed dielectric gate cut plugs **112**A, along with removal of the trench isolation structures **104**. A dielectric fill **130**, such as a silicon nitride fill, is then formed and planarized to form dielectric backside structures **130**.

[0043] Referring to FIG. **1**C, the sub-fin structures **102** are removed, e.g., by a selective etch process that lands on the etch stop layer **103**. Any exposed oxide and/or dielectric is then removed, leaving cavities **132** which expose the gate electrodes **108** and the epitaxial source or drain structures **110** from the bottom or backside of the structure.

[0044] Referring to FIG. **1**D, the etch stop layers **103** and the doped silicon structures **105** are removed. The gate electrode **108** is then recessed, e.g., using an atomic layer etch, to form recessed gate electrodes **108**A and extended cavities **132**A. The recessed gate electrodes **108**A have a bottommost surface that is vertically spaced further away from bottoms of the epitaxial source or drain structures than the starting gate electrodes **108**.

[0045] Referring to FIG. **1**E, a backside dielectric liner **133**, such as a silicon nitride liner, is formed in the extended cavities **132**A. A dielectric fill **134**, such as a silicon oxide fill, is then formed to fill the remainder of the extended cavities **132**A.

[0046] Referring to FIG. **1**F, a mask structure **136**/**138**, such as a mask including a hardmask layer **136** and a resist **138**, is formed on the bottom of the structure of FIG. **1**F. The mask **136**/**138** includes openings **140** that expose locations of select ones of the epitaxial source or drain structures **110** for ultimate backside contact. The dielectric fill **134** is then etched in those locations to form recessed dielectric fill **134**A.

[0047] Referring to FIG. **1**G, an integrated circuit structure **199** is formed by removing the mask **136**/**138** and removing exposed portions of the backside dielectric liner **133** and to expose the select ones of the epitaxial source or drain structures **110**. A silicide layer **135** may then be formed on the bottoms of the select ones of the epitaxial source or drain structures **110**. A conductive fill is then formed in the recesses and the structure is planarized to form planarized dielectric fill **130**A, planarized dielectric fill **134**B, and conductive backside contacts **142**. Integrated circuit structure **199** can include epitaxial source or drain structures **110**A coupled to corresponding conductive backside contacts **142**, and epitaxial source or drain structures **110**B that are not coupled to corresponding conductive backside contacts. In an embodiment, the conductive backside contacts **142** extends laterally beyond the corresponding epitaxial source or drain structure **110**A without contacting a neighboring gate electrode or gate stack.

[0048] In an embodiment, the epitaxial source or drain structures **110**A and the epitaxial source or drain structures **110**B are composed of a same material. In one such embodiment, the epitaxial source or drain structures **110**A and the epitaxial source or drain structures **110**B are composed of silicon, germanium and boron, e.g., such as is found in PMOS source or drain structures. In another such embodiment, the epitaxial source or drain structures **110**A and the epitaxial source or drain structures **110**B are composed of silicon and phosphorous, e.g., such as is found in NMOS source or drain structures.

[0049] As described above, one or more embodiments are directed to backside (BS) contacts with

deep source or drain (SD) enabled with silicon germanium (SiGe) etch stop (ES) layers. In an embodiment, etch stop layer **103** described above can be a silicon germanium etch stop layer, e.g., having a different SiGe composition than the silicon germanium source or drain structures **110**. In an embodiment, the etch stop layer **103** described above can be a silicon germanium etch stop layer, e.g., having a different SiGe composition than a sacrificial silicon germanium layer used in a nanowire release process, e.g., such as a nanowire release process described below in association with FIGS. **7** and **8**.

[0050] To provide context, a process scheme can be implemented to increase the source/drain depth and introduce a SiGe etch stop to ensure uniform SD depth. This approach can reduce a need for extensive over-etch. The combination of a deep SD and SiGe ES can pave the way for direct patterning of contact via to the source of the transistor from the backside. In an embodiment, the concept can be extended to enable multiple SiGe etch stop layers for front side and backside etch.

[0051] Advantages for implementing embodiments described herein can include the simplification of the process step and increased process margin to allow backside contact of source/drain, thus enabling direct BS power contact and delivery.

[0052] Detectability of the implementation of embodiments described herein can include that the SD depth of the transistors can appear to be uniform. Due to selectivity to the SiGe, there can be a minor budging of the SD at the bottom of the SD after the final SD etch. For some analog mixed signal devices as well as diodes, a Si sub-fin may not be removed, and the presence of a SiGe etch stop may be found in such devices.

[0053] As a first exemplary process scheme, FIG. **2**A illustrates cross-sectional views representing various operations in a method of fabricating a nanowire and release layer stack including a bottom etch stop layer, in accordance with an embodiment of the present disclosure.

[0054] Referring to part (a) of FIG. **2**A, a starting structure **200** includes a bottom silicon layer or substrate **202**, a silicon germanium etch stop layer **204**, an intermediate silicon layer **206**, and a plurality of alternating silicon germanium sacrificial release layers **208** and silicon nanowire layers **210**. In one embodiment, the silicon germanium sacrificial release layers **208** have a different silicon germanium composition and/or differing dopant composition than the silicon germanium etch stop layer **204**. The starting structure **200** also includes a capping layer **212**, sacrificial gate structures **214**, and gate spacers **216**.

[0055] Referring to part (b) of FIG. **2**A, The starting structure **200** is then subjected to a non-selective etch process that etches the stack to form stacks including a patterned capping layer **212**A, a plurality of alternating patterned silicon germanium sacrificial release layers **208**A and patterned silicon nanowire layers **210**A, and a patterned intermediate silicon layer **206**A. In one embodiment, the etch lands partially into the silicon germanium etch stop layer **204** to form partially patterned silicon germanium etch stop layer **204**A.

[0056] Referring to part (c) of FIG. **2**A, the partially patterned silicon germanium etch stop layer **204**A is then subjected a selective etch process that forms patterned silicon germanium etch stop layer **204**B without impacting the patterned silicon germanium sacrificial release layers **208**A of differing silicon germanium composition and/or differing dopant composition. The resulting structure **220** can later be subjected to a replacement gate and nanowire release process, examples of which are described below, and the patterned silicon germanium etch stop layer **204**B can be used in a process such as described in association with FIGS. **1**A-**1**G (e.g., as layer **103**, for example).

[0057] As a second exemplary process scheme, FIG. **2**B illustrates cross-sectional views representing various operations in a method of fabricating a nanowire and release layer stack including a bottom etch stop layer, in accordance with another embodiment of the present disclosure.

[0058] Referring to part (a) of FIG. **2**B, a starting structure **250** includes a bottom silicon layer or substrate **252**, a silicon germanium etch stop layer **254**, an intermediate silicon layer **256**, and a

plurality of alternating silicon germanium sacrificial release layers **258** and silicon nanowire layers **260**. In one embodiment, the silicon germanium sacrificial release layers **258** have a different silicon germanium composition and/or differing dopant composition than the silicon germanium etch stop layer **254**. The starting structure **250** also includes a capping layer **262**, sacrificial gate structures **264**, and gate spacers **266**.

[0059] Referring to part (b) of FIG. **2**B, The starting structure **250** is then subjected to a non-selective etch process that etches the stack to form stacks including a patterned capping layer **262**A, a plurality of alternating patterned silicon germanium sacrificial release layers **258**A and patterned silicon nanowire layers **260**A, and a partially patterned intermediate silicon layer **256**A.

[0060] Referring to part (c) of FIG. **2**B, the partially patterned intermediate silicon layer **256**A is then subjected a selective etch process that forms patterned intermediate silicon layer **256**B. The resulting structure **270** can later be subjected to a replacement gate and nanowire release process, examples of which are described below, and the silicon germanium etch stop layer **254** can be used in a process such as described in association with FIGS. **1**A-**1**G (e.g., as layer **103**, for example).

[0061] In another aspect, to provide further context, low electrical resistance power delivery solutions are needed as semiconductor scaling continues to stress interconnects into increasingly tight spaces. Backside power delivery, a scheme where a power delivery interconnect network connects directly to the transistors from the back of the wafer instead of sharing space with front side routing is a possible solution for future semiconductor technology generations.

[0062] Traditionally, power is delivered from a front side interconnect. At standard cell level, power can be delivered right on top of transistors or from a top and bottom cell boundary. Power delivered from a top and bottom cell boundary enables relatively shorter standard cell height with slightly higher power network resistance. However, a front side power network shares interconnect stack with signal routing and reduces signal routing tracks. In addition, for high performance design, top and bottom cell boundary power metal wires must be wide enough to reduce power network resistance and improve performance. This normally results in a cell height increase. In accordance with one or more embodiments of the present disclosure, delivering power from a wafer or substrate backside can be implemented to solve area and performance problems. At the cell level, wider metal 0 power at the top and bottom cell boundary may no longer be needed and, hence, cell height can be reduced. In addition, power network resistance can be significantly reduced resulting in performance improvement. At block and chip level, front side signal routing tracks are increased due to removed power routing and power network resistance is significantly reduced due to very wide wires, large vias and reduced interconnect layers.

[0063] In earlier technologies, a power delivery network from bump to the transistor required significant block resources. Such resource usage on the metal stack expressed itself in some process nodes as Standard Cell architectures with layout versioning or cell placement restrictions in the block level. In an embodiment, eliminating the power delivery network from the front side metal stack allows free sliding cell placement in the block without power delivery complications and placement related delay timing variation.

[0064] As an exemplary comparison, FIG. **3** illustrates cross-sectional views of an interconnect stack having front side power delivery and of an interconnect stack having backside power delivery, in accordance with an embodiment of the present disclosure.

[0065] Referring to FIG. **3**, an interconnect stack **300** having front side power delivery includes a transistor **302** and signal and power delivery metallization **304**. The transistor **302** includes a bulk substrate **306**, semiconductor fins **308**, a terminal **310**, and a device contact **312**. The signal and power delivery metallization **304** includes conductive vias **314**, conductive lines **316**, and a metal bump **318**.

[0066] Referring again to FIG. **3**, an interconnect stack **350** having backside power delivery includes a transistor **352**, front side signal metallization **354**A, and power delivery metallization **354**B. The transistor **352** includes semiconductor nanowires or nanoribbons **358**, a terminal **360**,

and a device contact **362**, and a boundary deep via **363**. The front side signal metallization **354**A includes conductive vias **364**A, conductive lines **366**A, and a metal bump **368**A. The power delivery metallization **354**B includes conductive vias **364**B, conductive lines **366**B, and a metal bump **368**B. It is to be appreciated that a backside power approach can also be implemented for structures including semiconductor fins.

[0067] To provide further context, a fundamental component of a backside power delivery network is an electrically functional feature that interfaces the source or drain contacts of a transistor with the backside interconnect network. Therefore, there is a need for a design and method of fabricating an interface feature that is compatible with existing library cell design conventions and transistor contact process flows.

[0068] There are presently no solutions employed in high volume manufacturing since backside power delivery has not yet been introduced in high volume manufacturing. Approaches may ultimately include a deep trench contact (TCN), direct source-drain contacts from backside, or replacing a gate contact track with a backside power contact. Depending on the proposed scheme, solutions can suffer from high resistance contacts negating the inherent value of backside power delivery co-optimization with front-end transistor processing, resulting in defect and performance risk and compromise.

[0069] In another aspect, differentiated backside access features are described.

[0070] One or more embodiments are directed to forming self-aligned access features for backside source or drain contact structures, e.g., for backside epitaxial (epi) contacts. One or more embodiments are directed to self-aligned backside access features. One or more embodiments are directed to differentiated backside access features, where deeper features can ultimately be accessed while shallower features are not accessed and effectively become dummy features, which can be referred to as a mirror (such as a titanium nitride (TiN)). One or more embodiments described herein are directed to gate-all-around integrated circuit structures fabricated using differentiated backside access features. It is to be appreciated that, unless indicated otherwise, reference to nanowires herein can indicate nanowires or nanoribbons or nanosheets or forksheets. One or more embodiments described herein are directed to fin-based integrated circuit structures fabricated using backside hardmask differentiated backside access features.

[0071] As an exemplary processing scheme, FIGS. **4**-**9** illustrate angled cross-sectional views representing various operations in methods of fabricating an integrated circuit structure having differentiated backside source or drain contact access features, in accordance with an embodiment of the present disclosure. It is to be appreciated that the embodiments described and illustrated may also be applicable for a fin structure in place of a stack of nanowires or nanoribbons or nanosheets or forksheets. It is also to be appreciated that, in an embodiment, a differentiated access approach such as described in association with FIGS. **4**-**9** can be integrated with a direct backside source or drain contact approach enabled with silicon germanium (SiGe) etch stop (ES) layers, such as described above in association with FIGS. **1**A-**1**G, **2**A and **2**B.

[0072] Referring to FIG. **4**, a starting structure **400** includes sub-fin structures **404** protruding from a substrate **402**, such as silicon sub-fin structures protruding from a silicon substrate. Isolation structures **406**, such as silicon oxide or silicon dioxide shallow trench isolation structures, separate sub-fin structures along a gate line direction. Fins **408**, such as fins of alternating stacks of silicon nanowires **410** and silicon germanium release layers **412** are over corresponding ones of the sub-fin structures **404**. A channel cap layer **415**, such as a silicon nitride channel cap, is over the fins **408**. Dummy gate structures, such as polysilicon **416** and silicon nitride **418** dummy gate structures (and, possibly dummy gate oxide **414**), extend over the fins **408**. Gate spacers **420**, such as silicon nitride gate spacers, are over and along sides of the dummy gate structures. At this stage, a protective helmet layer **422**, such as a titanium helmet, is on tops of the gate spacers **420** as an artifact from an etch process used to etch the fins **408** in locations between gate structures, e.g., for eventual source or drain formation. In an embodiment, the etch process is extended deeper than the

fins **408** to form deep trenches **424** are etched into the sub-fins **404**, as is depicted.
[0073] Referring to FIG. **5**, using a lithography patterning and then continued etch process, select ones of the deep trenches **424** are extended to form deeper trenches **426**. The etch process can be referred to as a self-aligned etch that is non-selective since deep trenches are formed in all locations.
[0074] Referring to FIG. **6**, a contact placeholder material, such as titanium nitride, is formed in the deep trenches **424** and the deeper trenches **426** and etched back to form contact placeholders **430** and dummy contact placeholders **428**. In an embodiment, contact placeholders **430** are ultimately accessed from the backside while dummy contact placeholders **428** are not.
[0075] Referring to FIG. **7**, the release layers **412** are laterally recessed relative to the nanowires **410** to form recessed release layers **412**A. An inner spacer material **432**, such as silicon nitride inner spacer material, is formed in the recesses formed by recessed release layers **412**A and on the contact placeholders **430** and dummy contact placeholders **428** to form structure **700**.
[0076] Referring to FIG. **8**, structure **700** of FIG. **7** is exposed to an epitaxial source or drain growth process, replacement gate and nanowire release process, inversion, and backside reveal process. The resulting structure includes a front side protecting dielectric layer **802**, metal gate electrodes **804**, high-k gate dielectrics **806**, a gate cap (such as silicon nitride) **808**, epitaxial source or drain structures (such as epitaxial silicon or epitaxial silicon germanium) **812** (which can be formed by patterning inner spacer material **432** to formed placeholder caps **432**A and inner spacers **432**B), front side trench contact **814**, dielectric sub-fin structures **816** (e.g., from replacement of silicon sub-fins), and dielectric gate cut plugs **818**. The contact placeholders **430** are backside revealed to form planarized contact placeholders **430**A. The dummy contact placeholders **428** are not revealed.
[0077] Referring to FIG. **9**, the contact placeholders **430** and the placeholder caps **432**A are removed and replaced with permanent backside contacts **902**, such as cobalt or tungsten contacts, to form structure **900**. The permanent backside contacts **902** contact corresponding ones **812**A of source or drain structures **812**. The dummy contact placeholders **428** remain with corresponding ones of the source or drain structures **812** that are not selected for backside contact. In an embodiment, the permanent backside contacts **902** can ultimately be coupled to one or more backside metallization lines or layers.
[0078] With reference again to FIGS. **4-9** (and in particular reference to an inverted FIG. **9**), in accordance with an embodiment of the present disclosure, an integrated circuit structure **900** includes a first plurality of horizontally stacked nanowires or fin **412** laterally spaced apart from a second plurality of horizontally stacked nanowires or fin **412**, the second plurality of horizontally stacked nanowires or fin **412** laterally spaced apart from a third plurality of horizontally stacked nanowires or fin **412**. A first gate stack **804**/**806** is over the first plurality of horizontally stacked nanowires or fin **412**, a second gate stack **804**/**806** is over the second plurality of horizontally stacked nanowires or fin **412**, and third gate stack **804**/**806** is over the third plurality of horizontally stacked nanowires or fin **412**. A first epitaxial source or drain structure **812** is between the first plurality of horizontally stacked nanowires or fin **412** and the second plurality of horizontally stacked nanowires or fin **412**, the first epitaxial source or drain structure **812** over a first conductive material **428** having a first depth below the first epitaxial source or drain structure **812**. A second epitaxial source or drain structure **812**A is between the second plurality of horizontally stacked nanowires or fin **412** and the third plurality of horizontally stacked nanowires or fin **412**, the second epitaxial source or drain structure **812**A over a second conductive material **902** having a second depth below the second epitaxial source or drain structure **812**A, the second depth greater than the first depth.
[0079] In an embodiment, the first conductive material and the second conductive material have different compositions. In an embodiment, the first conductive material includes titanium and nitrogen, and the second conductive material includes tungsten or cobalt.

[0080] In an embodiment, a dielectric spacer cap is between the first epitaxial source or drain structure **812** and the first conductive material **428**, as is depicted. In an embodiment, the second conductive material **902** is in direct contact with the second epitaxial source or drain structure **812**A, as is depicted.

[0081] It is to be appreciated that the above described direct backside source or drain contact and/or differentiated access approaches can be detectable in final products. Cross-sections may show epitaxial structures of having different widths on respective sides of a gate structure. Cross-sections may show non-accessed or short contact "placeholders." It is to be appreciated that even though the above Figures show gate-all-around-based transistors, embodiments can be applied to channels of any shape or material (fin, nanowire, nanoribbon, nanocomb/forksheet, etc.). It is to be appreciated that even though the Figures show a single layer of transistors, embodiments can be applied to multi-layer transistor architectures.

[0082] It is to be appreciated that, as used throughout the disclosure, a sub-fin, a nanowire, a nanoribbon, or a fin described herein may be a silicon sub-fin, a silicon nanowire, a silicon nanoribbon, or a silicon fin. As used throughout, a silicon layer or structure may be used to describe a silicon material composed of a very substantial amount of, if not all, silicon. However, it is to be appreciated that, practically, 100% pure Si may be difficult to form and, hence, could include a tiny percentage of carbon, germanium or tin. Such impurities may be included as an unavoidable impurity or component during deposition of Si or may "contaminate" the Si upon diffusion during post deposition processing. As such, embodiments described herein directed to a silicon layer or structure may include a silicon layer or structure that contains a relatively small amount, e.g., "impurity" level, non-Si atoms or species, such as Ge, C or Sn. It is to be appreciated that a silicon layer or structure as described herein may be undoped or may be doped with dopant atoms such as boron, phosphorous or arsenic.

[0083] It is to be appreciated that, as used throughout the disclosure, a sub-fin, a nanowire, a nanoribbon, or a fin described herein may be a silicon germanium sub-fin, a silicon germanium nanowire, a silicon germanium nanoribbon, or a silicon germanium fin. As used throughout, a silicon germanium layer or structure may be used to describe a silicon germanium material composed of substantial portions of both silicon and germanium, such as at least 5% of both. In some embodiments, the amount of germanium is greater than the amount of silicon. In particular embodiments, a silicon germanium layer or structure includes approximately 60% germanium and approximately 40% silicon (Si.sub.40Ge.sub.60). In other embodiments, the amount of silicon is greater than the amount of germanium. In particular embodiments, a silicon germanium layer or structure includes approximately 30% germanium and approximately 70% silicon (Si.sub.70Ge.sub.30). It is to be appreciated that, practically, 100% pure silicon germanium (referred to generally as SiGe) may be difficult to form and, hence, could include a tiny percentage of carbon or tin. Such impurities may be included as an unavoidable impurity or component during deposition of SiGe or may "contaminate" the SiGe upon diffusion during post deposition processing. As such, embodiments described herein directed to a silicon germanium layer or structure may include a silicon germanium layer or structure that contains a relatively small amount, e.g., "impurity" level, non-Ge and non-Si atoms or species, such as carbon or tin. It is to be appreciated that a silicon germanium layer or structure as described herein may be undoped or may be doped with dopant atoms such as boron, phosphorous or arsenic.

[0084] In another aspect, it is to be appreciated that direct backside source or drain contact structures can be implemented with front side architectures. In one example, direct backside source or drain contact structures can be implemented with contact over active gate (COAG) structures and processes. It is also to be appreciated that "color" hardmask COAG features below can be applicable to concepts regarding the above described backside contacts. One or more embodiments of the present disclosure are directed to semiconductor structures or devices having one or more gate contact structures (e.g., as gate contact vias) disposed over active portions of gate electrodes of

the semiconductor structures or devices. One or more embodiments of the present disclosure are directed to methods of fabricating semiconductor structures or devices having one or more gate contact structures formed over active portions of gate electrodes of the semiconductor structures or devices. Approaches described herein may be used to reduce a standard cell area by enabling gate contact formation over active gate regions. In accordance with one or more embodiments, tapered gate and trench contacts are implemented to enable COAG fabrication. Embodiments may be implemented to enable patterning at tight pitches.

[0085] To provide further background for the importance of a COAG processing scheme, in technologies where space and layout constraints are somewhat relaxed compared with current generation space and layout constraints, a contact to gate structure may be fabricated by making contact to a portion of the gate electrode disposed over an isolation region. As an example, FIG. **10**A illustrates a plan view of a semiconductor device having a gate contact disposed over an inactive portion of a gate electrode.

[0086] Referring to FIG. **10**A, a semiconductor structure or device **1000**A includes a diffusion or active region **1004** disposed in a substrate **1002**, and within an isolation region **1006**. One or more gate lines (also known as poly lines), such as gate lines **1008**A, **1008**B and **1008**C are disposed over the diffusion or active region **1004** as well as over a portion of the isolation region **1006**. Source or drain contacts (also known as trench contacts), such as contacts **1010**A and **1010**B, are disposed over source and drain regions of the semiconductor structure or device **1000**A. Trench contact vias **1012**A and **1012**B provide contact to trench contacts **1010**A and **1010**B, respectively. A separate gate contact **1014**, and overlying gate contact via **1016**, provides contact to gate line **1008**B. In contrast to the source or drain trench contacts **1010**A or **1010**B, the gate contact **1014** is disposed, from a plan view perspective, over isolation region **1006**, but not over diffusion or active region **1004**. Furthermore, neither the gate contact **1014** nor gate contact via **1016** is disposed between the source or drain trench contacts **1010**A and **1010**B.

[0087] FIG. **10**B illustrates a cross-sectional view of a non-planar semiconductor device having a gate contact disposed over an inactive portion of a gate electrode. Referring to FIG. **10**B, a semiconductor structure or device **1000**B, e.g. a non-planar version of device **1000**A of FIG. **10**A, includes a non-planar diffusion or active region **1004**B (e.g., a fin structure) formed from substrate **1002**, and within isolation region **1006**. Gate line **1008**B is disposed over the non-planar diffusion or active region **1004**B as well as over a portion of the isolation region **1006**. As shown, gate line **1008**B includes a gate electrode **1050** and gate dielectric layer **1052**, along with a dielectric cap layer **1054**. Gate contact **1014**, and overlying gate contact via **1016** are also seen from this perspective, along with an overlying metal interconnect **1060**, all of which are disposed in inter-layer dielectric stacks or layers **1070**. Also seen from the perspective of FIG. **10**B, the gate contact **1014** is disposed over isolation region **1006**, but not over non-planar diffusion or active region **1004**B.

[0088] Referring again to FIGS. **10**A and **10**B, the arrangement of semiconductor structure or device **1000**A and **1000**B, respectively, places the gate contact over isolation regions. Such an arrangement wastes layout space. However, placing the gate contact over active regions would require either an extremely tight registration budget or gate dimensions would have to increase to provide enough space to land the gate contact. Furthermore, historically, contact to gate over diffusion regions has been avoided for risk of drilling through other gate material (e.g., polysilicon) and contacting the underlying active region. One or more embodiments described herein address the above issues by providing feasible approaches, and the resulting structures, to fabricating contact structures that contact portions of a gate electrode formed over a diffusion or active region.

[0089] As an example, FIG. **11**A illustrates a plan view of a semiconductor device having a gate contact via disposed over an active portion of a gate electrode, in accordance with an embodiment of the present disclosure. Referring to FIG. **11**A, a semiconductor structure or device **1100**A includes a diffusion or active region **1104** disposed in a substrate **1102**, and within an isolation

region **1106**. One or more gate lines, such as gate lines **1108**A, **1108**B and **1108**C are disposed over the diffusion or active region **1104** as well as over a portion of the isolation region **1106**. Source or drain trench contacts, such as trench contacts **1110**A and **1110**B, are disposed over source and drain regions of the semiconductor structure or device **1100**A. Trench contact vias **1112**A and **1112**B provide contact to trench contacts **1110**A and **1110**B, respectively. A gate contact via **1116**, with no intervening separate gate contact layer, provides contact to gate line **1108**B. In contrast to FIG. **10**A, the gate contact **1116** is disposed, from a plan view perspective, over the diffusion or active region **1104** and between the source or drain contacts **1110**A and **1110**B.

[0090] FIG. **11**B illustrates a cross-sectional view of a non-planar semiconductor device having a gate contact via disposed over an active portion of a gate electrode, in accordance with an embodiment of the present disclosure. Referring to FIG. **11**B, a semiconductor structure or device **1100**B, e.g. a non-planar version of device **1100**A of FIG. **11**A, includes a non-planar diffusion or active region **1104**B (e.g., a fin structure) formed from substrate **1102**, and within isolation region **1106**. Gate line **1108**B is disposed over the non-planar diffusion or active region **1104**B as well as over a portion of the isolation region **1106**. As shown, gate line **1108**B includes a gate electrode **1150** and gate dielectric layer **1152**, along with a dielectric cap layer **1154**. The gate contact via **1116** is also seen from this perspective, along with an overlying metal interconnect **1160**, both of which are disposed in inter-layer dielectric stacks or layers **1170**. Also seen from the perspective of FIG. **11**B, the gate contact via **1116** is disposed over non-planar diffusion or active region **1104**B.

[0091] Thus, referring again to FIGS. **11**A and **11**B, in an embodiment, trench contact vias **1112**A, **1112**B and gate contact via **1116** are formed in a same layer and are essentially co-planar. In comparison to FIGS. **10**A and **10**B, the contact to the gate line would otherwise include and additional gate contact layer, e.g., which could be run perpendicular to the corresponding gate line. In the structure(s) described in association with FIGS. **11**A and **11**B, however, the fabrication of structures **1100**A and **1100**B, respectively, enables the landing of a contact directly from a metal interconnect layer on an active gate portion without shorting to adjacent source drain regions. In an embodiment, such an arrangement provides a large area reduction in circuit layout by eliminating the need to extend transistor gates on isolation to form a reliable contact. As used throughout, in an embodiment, reference to an active portion of a gate refers to that portion of a gate line or structure disposed over (from a plan view perspective) an active or diffusion region of an underlying substrate. In an embodiment, reference to an inactive portion of a gate refers to that portion of a gate line or structure disposed over (from a plan view perspective) an isolation region of an underlying substrate.

[0092] In an embodiment, the semiconductor structure or device **1100** is a non-planar device such as, but not limited to, a fin-FET or a tri-gate device. In such an embodiment, a corresponding semiconducting channel region is composed of or is formed in a three-dimensional body. In one such embodiment, the gate electrode stacks of gate lines **1108**A and **1108**B surround at least a top surface and a pair of sidewalls of the three-dimensional body. In another embodiment, at least the channel region is made to be a discrete three-dimensional body, such as in a gate-all-around device. In one such embodiment, the gate electrode stacks of gate lines **1108**A and **1108**B each completely surrounds the channel region.

[0093] Generally, one or more embodiments are directed to approaches for, and structures formed from, landing a gate contact via directly on an active transistor gate. Such approaches may eliminate the need for extension of a gate line on isolation for contact purposes. Such approaches may also eliminate the need for a separate gate contact (GCN) layer to conduct signals from a gate line or structure. In an embodiment, eliminating the above features is achieved by recessing contact metals in a trench contact (TCN) and introducing an additional dielectric material in the process flow (e.g., trench insulating layer (TILA)). The additional dielectric material is included as a trench contact dielectric cap layer with etch characteristics different from the gate dielectric material cap layer used for trench contact alignment in a gate aligned contact process (GAP) processing scheme

(e.g., use of a gate insulating layer (GILA)).
[0094] As an exemplary fabrication scheme, a starting structure includes one or more gate stack structures disposed above a substrate. The gate stack structures may include a gate dielectric layer and a gate electrode. Trench contacts, e.g., contacts to diffusion regions of the substrate or to epitaxial region formed within the substrate are spaced apart from gate stack structures by dielectric spacers. An insulating cap layer may be disposed on the gate stack structures (e.g., GILA). In one embodiment, contact blocking regions or “contact plugs”, which may be fabricated from an inter-layer dielectric material, are included in regions where contact formation is to be blocked.
[0095] In an embodiment, the contact pattern is essentially perfectly aligned to an existing gate pattern while eliminating the use of a lithographic operation with exceedingly tight registration budget. In one such embodiment, this approach enables the use of intrinsically highly selective wet etching (or anisotropic dry etch processes some of which are non-plasma, gas phase isotropic etches (e.g., versus classic dry or plasma etching) to generate contact openings. In an embodiment, a contact pattern is formed by utilizing an existing gate pattern in combination with a contact plug lithography operation. In one such embodiment, the approach enables elimination of the need for an otherwise critical lithography operation to generate a contact pattern, as used in other approaches. This also allows for perfect or near-perfect self-alignment with a larger edge placement error margin. In an embodiment, a trench contact grid is not separately patterned, but is rather formed between poly (gate) lines. For example, in one such embodiment, a trench contact grid is formed subsequent to gate grating patterning but prior to gate grating cuts.
[0096] Furthermore, the gate stack structures may be fabricated by a replacement gate process. In such a scheme, dummy gate material such as polysilicon or silicon nitride pillar material, may be removed and replaced with permanent gate electrode material. In one such embodiment, a permanent gate dielectric layer is also formed in this process, as opposed to being carried through from earlier processing. In an embodiment, dummy gates are removed by a dry etch or wet etch process. In one embodiment, dummy gates are composed of polycrystalline silicon or amorphous silicon and are removed with a dry etch process including SF.sub.6. In another embodiment, dummy gates are composed of polycrystalline silicon or amorphous silicon and are removed with a wet etch process including aqueous NH.sub.4OH or tetramethylammonium hydroxide. In one embodiment, dummy gates are composed of silicon nitride and are removed with a wet etch including aqueous phosphoric acid.
[0097] In an embodiment, one or more approaches described herein contemplate essentially a dummy and replacement gate process in combination with a dummy and replacement contact process. In one such embodiment, the replacement contact process is performed after the replacement gate process to allow high temperature anneal of at least a portion of the permanent gate stack. For example, in a specific such embodiment, an anneal of at least a portion of the permanent gate structures, e.g., after a gate dielectric layer is formed, is performed at a temperature greater than approximately 600 degrees Celsius. The anneal is performed prior to formation of the permanent contacts.
[0098] Next, the trench contacts may be recessed to provide recessed trench contacts that have a height below the top surface of adjacent spacers. An insulating cap layer is then formed on the recessed trench contacts (e.g., TILA). In accordance with an embodiment of the present disclosure, the insulating cap layer on the recessed trench contacts is composed of a material having a different etch characteristic than insulating cap layer on the gate stack structures.
[0099] The trench contacts may be recessed by a process selective to the materials of the spacers and the gate insulating cap layer. For example, in one embodiment, the trench contacts are recessed by an etch process such as a wet etch process or dry etch process. The trench contact insulating cap layer may be formed by a process suitable to provide a conformal and sealing layer above the exposed portions of the trench contacts. For example, in one embodiment, the trench contact insulating cap layer is formed by a chemical vapor deposition (CVD) process as a conformal layer

above the entire structure. The conformal layer is then planarized, e.g., by chemical mechanical polishing (CMP), to provide the trench contact insulating cap layer material only above the recessed trench contacts.

[0100] Regarding suitable material combinations for gate or trench contact insulating cap layers, in one embodiment, one of the pair of gate versus trench contact insulating cap material is composed of silicon oxide while the other is composed of silicon nitride. In another embodiment, one of the pair of gate versus trench contact insulating cap material is composed of silicon oxide while the other is composed of carbon doped silicon nitride. In another embodiment, one of the pair of gate versus trench contact insulating cap material is composed of silicon oxide while the other is composed of silicon carbide. In another embodiment, one of the pair of gate versus trench contact insulating cap material is composed of silicon nitride while the other is composed of carbon doped silicon nitride. In another embodiment, one of the pair of gate versus trench contact insulating cap material is composed of silicon nitride while the other is composed of silicon carbide. In another embodiment, one of the pair of gate versus trench contact insulating cap material is composed of carbon doped silicon nitride while the other is composed of silicon carbide.

[0101] In another aspect, direct backside source or drain contacts are implemented with nanowire or nanoribbon structures. In a particular example, nanowire or nanoribbon release processing may be performed through a replacement gate trench. Examples of such release processes are described below. Additionally, in yet another aspect, backend (BE) interconnect scaling can result in lower performance and higher manufacturing cost due to patterning complexity. Embodiments described herein may be implemented to enable front side and backside interconnect integration for nanowire transistors. Embodiments described herein may provide an approach to achieve a relatively wider interconnect pitch. The result may be improved product performance and lower patterning costs. Embodiments may be implemented to enable robust functionality of scaled nanowire or nanoribbon transistors with low power and high performance.

[0102] One or more embodiments described herein are directed dual epitaxial (EPI) connections for nanowire or nanoribbon transistors using partial source or drain (SD) and asymmetric trench contact (TCN) depth. In an embodiment, an integrated circuit structure is fabricated by forming source-drain openings of nanowire/nanoribbon transistors which are partially filled with SD epitaxy. A remainder of the opening is filled with a conductive material. Deep trench formation on one of the source or drain side enables direct contact to a backside interconnect level.

[0103] As an exemplary process flow for fabricating another gate-all-around device, FIGS. **12**A-**12**J illustrates cross-sectional views of various operations in a method of fabricating a gate-all-around integrated circuit structure, in accordance with an embodiment of the present disclosure.

[0104] Referring to FIG. **12**A, a method of fabricating an integrated circuit structure includes forming a starting stack which includes alternating sacrificial layers **1204** and nanowires **1206** above a fin **1202**, such as a silicon fin. The nanowires **1206** may be referred to as a vertical arrangement of nanowires. A protective cap **1208** may be formed above the alternating sacrificial layers **1204** and nanowires **1206**, as is depicted. A relaxed buffer layer **1252** and a defect modification layer **1250** may be formed beneath the alternating sacrificial layers **1204** and nanowires **1206**, as is also depicted.

[0105] Referring to FIG. **12**B, a gate stack **1210** is formed over the vertical arrangement of horizontal nanowires **1206**. Portions of the vertical arrangement of horizontal nanowires **1206** are then released by removing portions of the sacrificial layers **1204** to provide recessed sacrificial layers **1204**′ and cavities **1212**, as is depicted in FIG. **12**C.

[0106] It is to be appreciated that the structure of FIG. **12**C may be fabricated to completion without first performing the deep etch and asymmetric contact processing described below. In either case (e.g., with or without asymmetric contact processing), in an embodiment, a fabrication process involves use of a process scheme that provides a gate-all-around integrated circuit structure having epitaxial nubs, which may be vertically discrete source or drain structures.

[0107] Referring to FIG. **12**D, upper gate spacers **1214** are formed at sidewalls of the gate structure **1210**. Cavity spacers **1216** are formed in the cavities **1212** beneath the upper gate spacers **1214**. A deep trench contact etch is then optionally performed to form trenches **1218** and to form recessed nanowires **1206**′. A patterned relaxed buffer layer **1252**′ and a patterned defect modification layer **1250**′ may also be present, as is depicted.
[0108] A sacrificial material **1220** is then formed in the trenches **1218**, as is depicted in FIG. **12**E. In other process schemes, an isolated trench bottom or silicon trench bottom may be used.
[0109] Referring to FIG. **12**F, a first epitaxial source or drain structure (e.g., left-hand features **1222**) is formed at a first end of the vertical arrangement of horizontal nanowires **1206**′. A second epitaxial source or drain structure (e.g., right-hand features **1222**) is formed at a second end of the vertical arrangement of horizontal nanowires **1206**′. In an embodiment, as depicted, the epitaxial source or drain structures **1222** are vertically discrete source or drain structures and may be referred to as epitaxial nubs.
[0110] An inter-layer dielectric (ILD) material **1224** is then formed at the sides of the gate electrode **1210** and adjacent the source or drain structures **1222**, as is depicted in FIG. **12**G. Referring to FIG. **12**H, a replacement gate process is used to form a permanent gate dielectric **1228** and a permanent gate electrode **1226**. The ILD material **1224** is then removed, as is depicted in FIG. **12**I. The sacrificial material **1220** is then removed from one of the source drain locations (e.g., right-hand side) to form trench **1232**, but is not removed from the other of the source drain locations to form trench **1230**.
[0111] Referring to FIG. **12**J, a first conductive contact structure **1234** is formed coupled to the first epitaxial source or drain structure (e.g., left-hand features **1222**). A second conductive contact structure **1236** is formed coupled to the second epitaxial source or drain structure (e.g., right-hand features **1222**). The second conductive contact structure **1236** is formed deeper along the fin **1202** than the first conductive contact structure **1234**. In an embodiment, although not depicted in FIG. **12**J, the method further includes forming an exposed surface of the second conductive contact structure **1236** at a bottom of the fin **1202**. Conductive contacts may include a contact resistance reducing layer and a primary contact electrode layer, where examples can include Ti, Ni, Co (for the former and W, Ru, Co for the latter.)
[0112] In an embodiment, the second conductive contact structure **1236** is deeper along the fin **1202** than the first conductive contact structure **1234**, as is depicted. In one such embodiment, the first conductive contact structure **1234** is not along the fin **1202**, as is depicted. In another such embodiment, not depicted, the first conductive contact structure **1234** is partially along the fin **1202**.
[0113] In an embodiment, the second conductive contact structure **1236** is along an entirety of the fin **1202**. In an embodiment, although not depicted, in the case that the bottom of the fin **1202** is exposed by a backside substrate removal process, the second conductive contact structure **1236** has an exposed surface at a bottom of the fin **1202**.
[0114] In another aspect, in order to enable access to both conductive contact structures of a pair of asymmetric source and drain contact structures, integrated circuit structures described herein may be fabricated using a backside reveal of front side structures fabrication approach. In some exemplary embodiments, reveal of the backside of a transistor or other device structure entails wafer-level backside processing. In contrast to a conventional TSV-type technology, a reveal of the backside of a transistor as described herein may be performed at the density of the device cells, and even within sub-regions of a device. Furthermore, such a reveal of the backside of a transistor may be performed to remove substantially all of a donor substrate upon which a device layer was disposed during front side device processing. As such, a microns-deep TSV becomes unnecessary with the thickness of semiconductor in the device cells following a reveal of the backside of a transistor potentially being only tens or hundreds of nanometers.
[0115] Reveal techniques described herein may enable a paradigm shift from “bottom-up” device

fabrication to “center-out” fabrication, where the “center” is any layer that is employed in front side fabrication, revealed from the backside, and again employed in backside fabrication. Processing of both a front side and revealed backside of a device structure may address many of the challenges associated with fabricating 3D ICs when primarily relying on front side processing.

[0116] A reveal of the backside of a transistor approach may be employed for example to remove at least a portion of a carrier layer and intervening layer of a donor-host substrate assembly. The process flow begins with an input of a donor-host substrate assembly. A thickness of a carrier layer in the donor-host substrate is polished (e.g., CMP) and/or etched with a wet or dry (e.g., plasma) etch process. Any grind, polish, and/or wet/dry etch process known to be suitable for the composition of the carrier layer may be employed. For example, where the carrier layer is a group IV semiconductor (e.g., silicon) a CMP slurry known to be suitable for thinning the semiconductor may be employed. Likewise, any wet etchant or plasma etch process known to be suitable for thinning the group IV semiconductor may also be employed.

[0117] In some embodiments, the above is preceded by cleaving the carrier layer along a fracture plane substantially parallel to the intervening layer. The cleaving or fracture process may be utilized to remove a substantial portion of the carrier layer as a bulk mass, reducing the polish or etch time needed to remove the carrier layer. For example, where a carrier layer is 400-900 μm in thickness, 100-700 μm may be cleaved off by practicing any blanket implant known to promote a wafer-level fracture. In some exemplary embodiments, a light element (e.g., H, He, or Li) is implanted to a uniform target depth within the carrier layer where the fracture plane is desired. Following such a cleaving process, the thickness of the carrier layer remaining in the donor-host substrate assembly may then be polished or etched to complete removal. Alternatively, where the carrier layer is not fractured, the grind, polish and/or etch operation may be employed to remove a greater thickness of the carrier layer.

[0118] Next, exposure of an intervening layer is detected. Detection is used to identify a point when the backside surface of the donor substrate has advanced to nearly the device layer. Any endpoint detection technique known to be suitable for detecting a transition between the materials employed for the carrier layer and the intervening layer may be practiced. In some embodiments, one or more endpoint criteria are based on detecting a change in optical absorbance or emission of the backside surface of the donor substrate during the polishing or etching performed. In some other embodiments, the endpoint criteria are associated with a change in optical absorbance or emission of byproducts during the polishing or etching of the donor substrate backside surface. For example, absorbance or emission wavelengths associated with the carrier layer etch byproducts may change as a function of the different compositions of the carrier layer and intervening layer. In other embodiments, the endpoint criteria are associated with a change in mass of species in byproducts of polishing or etching the backside surface of the donor substrate. For example, the byproducts of processing may be sampled through a quadrupole mass analyzer and a change in the species mass may be correlated to the different compositions of the carrier layer and intervening layer. In another exemplary embodiment, the endpoint criteria is associated with a change in friction between a backside surface of the donor substrate and a polishing surface in contact with the backside surface of the donor substrate.

[0119] Detection of the intervening layer may be enhanced where the removal process is selective to the carrier layer relative to the intervening layer as non-uniformity in the carrier removal process may be mitigated by an etch rate delta between the carrier layer and intervening layer. Detection may even be skipped if the grind, polish and/or etch operation removes the intervening layer at a rate sufficiently below the rate at which the carrier layer is removed. If an endpoint criteria is not employed, a grind, polish and/or etch operation of a predetermined fixed duration may stop on the intervening layer material if the thickness of the intervening layer is sufficient for the selectivity of the etch. In some examples, the carrier etch rate:intervening layer etch rate is 3:1-10:1, or more.

[0120] Upon exposing the intervening layer, at least a portion of the intervening layer may be

removed. For example, one or more component layers of the intervening layer may be removed. A thickness of the intervening layer may be removed uniformly by a polish, for example. Alternatively, a thickness of the intervening layer may be removed with a masked or blanket etch process. The process may employ the same polish or etch process as that employed to thin the carrier, or may be a distinct process with distinct process parameters. For example, where the intervening layer provides an etch stop for the carrier removal process, the latter operation may employ a different polish or etch process that favors removal of the intervening layer over removal of the device layer. Where less than a few hundred nanometers of intervening layer thickness is to be removed, the removal process may be relatively slow, optimized for across-wafer uniformity, and more precisely controlled than that employed for removal of the carrier layer. A CMP process employed may, for example employ a slurry that offers very high selectively (e.g., 100:1-300:1, or more) between semiconductor (e.g., silicon) and dielectric material (e.g., SiO) surrounding the device layer and embedded within the intervening layer, for example, as electrical isolation between adjacent device regions.

[0121] For embodiments where the device layer is revealed through complete removal of the intervening layer, backside processing may commence on an exposed backside of the device layer or specific device regions there in. In some embodiments, the backside device layer processing includes a further polish or wet/dry etch through a thickness of the device layer disposed between the intervening layer and a device region previously fabricated in the device layer, such as a source or drain region.

[0122] In some embodiments where the carrier layer, intervening layer, or device layer backside is recessed with a wet and/or plasma etch, such an etch may be a patterned etch or a materially selective etch that imparts significant non-planarity or topography into the device layer backside surface. As described further below, the patterning may be within a device cell (i.e., “intra-cell” patterning) or may be across device cells (i.e., “inter-cell” patterning). In some patterned etch embodiments, at least a partial thickness of the intervening layer is employed as a hard mask for backside device layer patterning. Hence, a masked etch process may preface a correspondingly masked device layer etch.

[0123] The above described processing scheme may result in a donor-host substrate assembly that includes IC devices that have a backside of an intervening layer, a backside of the device layer, and/or backside of one or more semiconductor regions within the device layer, and/or front side metallization revealed. Additional backside processing of any of these revealed regions may then be performed during downstream processing.

[0124] As described throughout the present application, a substrate may be composed of a semiconductor material that can withstand a manufacturing process and in which charge can migrate. In an embodiment, a substrate is described herein is a bulk substrate composed of a crystalline silicon, silicon/germanium or germanium layer doped with a charge carrier, such as but not limited to phosphorus, arsenic, boron or a combination thereof, to form an active region. In one embodiment, the concentration of silicon atoms in such a bulk substrate is greater than 97%. In another embodiment, a bulk substrate is composed of an epitaxial layer grown atop a distinct crystalline substrate, e.g. a silicon epitaxial layer grown atop a boron-doped bulk silicon mono-crystalline substrate. A bulk substrate may alternatively be composed of a group III-V material. In an embodiment, a bulk substrate is composed of a group III-V material such as, but not limited to, gallium nitride, gallium phosphide, gallium arsenide, indium phosphide, indium antimonide, indium gallium arsenide, aluminum gallium arsenide, indium gallium phosphide, or a combination thereof. In one embodiment, a bulk substrate is composed of a group III-V material and the charge-carrier dopant impurity atoms are ones such as, but not limited to, carbon, silicon, germanium, oxygen, sulfur, selenium or tellurium.

[0125] As described throughout the present application, isolation regions such as shallow trench isolation regions or sub-fin isolation regions may be composed of a material suitable to ultimately

electrically isolate, or contribute to the isolation of, portions of a permanent gate structure from an underlying bulk substrate or to isolate active regions formed within an underlying bulk substrate, such as isolating fin active regions. For example, in one embodiment, an isolation region is composed of one or more layers of a dielectric material such as, but not limited to, silicon dioxide, silicon oxy-nitride, silicon nitride, carbon-doped silicon nitride, or a combination thereof.

[0126] As described throughout the present application, gate lines or gate structures may be composed of a gate electrode stack which includes a gate dielectric layer and a gate electrode layer. In an embodiment, the gate electrode of the gate electrode stack is composed of a metal gate and the gate dielectric layer is composed of a high-k material. For example, in one embodiment, the gate dielectric layer is composed of a material such as, but not limited to, hafnium oxide, hafnium oxy-nitride, hafnium silicate, lanthanum oxide, zirconium oxide, zirconium silicate, tantalum oxide, barium strontium titanate, barium titanate, strontium titanate, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, lead zinc niobate, or a combination thereof. Furthermore, a portion of gate dielectric layer may include a layer of native oxide formed from the top few layers of a semiconductor substrate. In an embodiment, the gate dielectric layer is composed of a top high-k portion and a lower portion composed of an oxide of a semiconductor material. In one embodiment, the gate dielectric layer is composed of a top portion of hafnium oxide and a bottom portion of silicon dioxide or silicon oxy-nitride. In some implementations, a portion of the gate dielectric is a “U”-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate.

[0127] In one embodiment, a gate electrode is composed of a metal layer such as, but not limited to, metal nitrides, metal carbides, metal silicides, metal aluminides, hafnium, zirconium, titanium, tantalum, aluminum, ruthenium, palladium, platinum, cobalt, nickel or conductive metal oxides. In a specific embodiment, the gate electrode is composed of a non-workfunction-setting fill material formed above a metal workfunction-setting layer. The gate electrode layer may consist of a P-type workfunction metal or an N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are workfunction metal layers and at least one metal layer is a conductive fill layer. For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV. In some implementations, the gate electrode may consist of a “U”-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further implementations of the disclosure, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

[0128] As described throughout the present application, spacers associated with gate lines or electrode stacks may be composed of a material suitable to ultimately electrically isolate, or contribute to the isolation of, a permanent gate structure from adjacent conductive contacts, such as

self-aligned contacts. For example, in one embodiment, the spacers are composed of a dielectric material such as, but not limited to, silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride.

[0129] In an embodiment, as used throughout the present description, interlayer dielectric (ILD) material is composed of or includes a layer of a dielectric or insulating material. Examples of suitable dielectric materials include, but are not limited to, oxides of silicon (e.g., silicon dioxide (SiO.sub.2)), doped oxides of silicon, fluorinated oxides of silicon, carbon doped oxides of silicon, various low-k dielectric materials known in the arts, and combinations thereof. The interlayer dielectric material may be formed by techniques, such as, for example, chemical vapor deposition (CVD), physical vapor deposition (PVD), or by other deposition methods.

[0130] In an embodiment, as is also used throughout the present description, metal lines or interconnect line material (and via material) is composed of one or more metal or other conductive structures. A common example is the use of copper lines and structures that may or may not include barrier layers between the copper and surrounding ILD material. As used herein, the term metal includes alloys, stacks, and other combinations of multiple metals. For example, the metal interconnect lines may include barrier layers (e.g., layers including one or more of Ta, TaN, Ti or TiN), stacks of different metals or alloys, etc. Thus, the interconnect lines may be a single material layer, or may be formed from several layers, including conductive liner layers and fill layers. Any suitable deposition process, such as electroplating, chemical vapor deposition or physical vapor deposition, may be used to form interconnect lines. In an embodiment, the interconnect lines are composed of a conductive material such as, but not limited to, Cu, Al, Ti, Zr, Hf, V, Ru, Co, Ni, Pd, Pt, W, Ag, Au or alloys thereof. The interconnect lines are also sometimes referred to in the art as traces, wires, lines, metal, or simply interconnect.

[0131] In an embodiment, as is also used throughout the present description, hardmask materials are composed of dielectric materials different from the interlayer dielectric material. In one embodiment, different hardmask materials may be used in different regions so as to provide different growth or etch selectivity to each other and to the underlying dielectric and metal layers. In some embodiments, a hardmask layer includes a layer of a nitride of silicon (e.g., silicon nitride) or a layer of an oxide of silicon, or both, or a combination thereof. Other suitable materials may include carbon-based materials. In another embodiment, a hardmask material includes a metal species. For example, a hardmask or other overlying material may include a layer of a nitride of titanium or another metal (e.g., titanium nitride). Potentially lesser amounts of other materials, such as oxygen, may be included in one or more of these layers. Alternatively, other hardmask layers known in the arts may be used depending upon the particular implementation. The hardmask layers maybe formed by CVD, PVD, or by other deposition methods.

[0132] In an embodiment, as is also used throughout the present description, lithographic operations are performed using 193 nm immersion lithography (i193), extreme ultra-violet (EUV) lithography or electron beam direct write (EBDW) lithography, or the like. A positive tone or a negative tone resist may be used. In one embodiment, a lithographic mask is a tri-layer mask composed of a topographic masking portion, an anti-reflective coating (ARC) layer, and a photoresist layer. In a particular such embodiment, the topographic masking portion is a carbon hardmask (CHM) layer and the anti-reflective coating layer is a silicon ARC layer.

[0133] In an embodiment, approaches described herein may involve formation of a contact pattern which is very well aligned to an existing gate pattern while eliminating the use of a lithographic operation with exceedingly tight registration budget. In one such embodiment, this approach enables the use of intrinsically highly selective wet etching (e.g., versus dry or plasma etching) to generate contact openings. In an embodiment, a contact pattern is formed by utilizing an existing gate pattern in combination with a contact plug lithography operation. In one such embodiment, the approach enables elimination of the need for an otherwise critical lithography operation to generate a contact pattern, as used in other approaches. In an embodiment, a trench contact grid is not

separately patterned, but is rather formed between poly (gate) lines. For example, in one such embodiment, a trench contact grid is formed subsequent to gate grating patterning but prior to gate grating cuts.

[0134] Furthermore, a gate stack structure may be fabricated by a replacement gate process. In such a scheme, dummy gate material such as polysilicon or silicon nitride pillar material, may be removed and replaced with permanent gate electrode material. In one such embodiment, a permanent gate dielectric layer is also formed in this process, as opposed to being carried through from earlier processing. In an embodiment, dummy gates are removed by a dry etch or wet etch process. In one embodiment, dummy gates are composed of polycrystalline silicon or amorphous silicon and are removed with a dry etch process including use of SF.sub.6. In another embodiment, dummy gates are composed of polycrystalline silicon or amorphous silicon and are removed with a wet etch process including use of aqueous NH.sub.4OH or tetramethylammonium hydroxide. In one embodiment, dummy gates are composed of silicon nitride and are removed with a wet etch including aqueous phosphoric acid.

[0135] In an embodiment, one or more approaches described herein contemplate essentially a dummy and replacement gate process in combination with a dummy and replacement contact process to arrive at structure. In one such embodiment, the replacement contact process is performed after the replacement gate process to allow high temperature anneal of at least a portion of the permanent gate stack. For example, in a specific such embodiment, an anneal of at least a portion of the permanent gate structures, e.g., after a gate dielectric layer is formed, is performed at a temperature greater than approximately 600 degrees Celsius. The anneal is performed prior to formation of the permanent contacts.

[0136] In some embodiments, the arrangement of a semiconductor structure or device places a gate contact over portions of a gate line or gate stack over isolation regions. However, such an arrangement may be viewed as inefficient use of layout space. In another embodiment, a semiconductor device has contact structures that contact portions of a gate electrode formed over an active region. In general, prior to (e.g., in addition to) forming a gate contact structure (such as a via) over an active portion of a gate and in a same layer as a trench contact via, one or more embodiments of the present disclosure include first using a gate aligned trench contact process. Such a process may be implemented to form trench contact structures for semiconductor structure fabrication, e.g., for integrated circuit fabrication. In an embodiment, a trench contact pattern is formed as aligned to an existing gate pattern. By contrast, other approaches typically involve an additional lithography process with tight registration of a lithographic contact pattern to an existing gate pattern in combination with selective contact etches. For example, another process may include patterning of a poly (gate) grid with separate patterning of contact features.

[0137] It is to be appreciated that pitch division processing and patterning schemes may be implemented to enable embodiments described herein or may be included as part of embodiments described herein. Pitch division patterning typically refers to pitch halving, pitch quartering etc. Pitch division schemes may be applicable to FEOL processing, BEOL processing, or both FEOL (device) and BEOL (metallization) processing. In accordance with one or more embodiments described herein, optical lithography is first implemented to print unidirectional lines (e.g., either strictly unidirectional or predominantly unidirectional) in a pre-defined pitch. Pitch division processing is then implemented as a technique to increase line density.

[0138] In an embodiment, the term “grating structure” for fins, gate lines, metal lines, ILD lines or hardmask lines is used herein to refer to a tight pitch grating structure. In one such embodiment, the tight pitch is not achievable directly through a selected lithography. For example, a pattern based on a selected lithography may first be formed, but the pitch may be halved by the use of spacer mask patterning, as is known in the art. Even further, the original pitch may be quartered by a second round of spacer mask patterning. Accordingly, the grating-like patterns described herein may have metal lines, ILD lines or hardmask lines spaced at a substantially consistent pitch and

having a substantially consistent width. For example, in some embodiments the pitch variation would be within ten percent and the width variation would be within ten percent, and in some embodiments, the pitch variation would be within five percent and the width variation would be within five percent. The pattern may be fabricated by a pitch halving or pitch quartering, or other pitch division, approach. In an embodiment, the grating is not necessarily single pitch.

[0139] In an embodiment, a blanket film is patterned using lithography and etch processing which may involve, e.g., spacer-based-double-patterning (SBDP) or pitch halving, or spacer-based-quadruple-patterning (SBQP) or pitch quartering. It is to be appreciated that other pitch division approaches may also be implemented. In any case, in an embodiment, a gridded layout may be fabricated by a selected lithography approach, such as 193 nm immersion lithography (193i). Pitch division may be implemented to increase the density of lines in the gridded layout by a factor of n. Gridded layout formation with 193i lithography plus pitch division by a factor of 'n' can be designated as 193i+P/n Pitch Division. In one such embodiment, 193 nm immersion scaling can be extended for many generations with cost effective pitch division.

[0140] It is also to be appreciated that not all aspects of the processes described above need be practiced to fall within the spirit and scope of embodiments of the present disclosure. For example, in one embodiment, dummy gates need not ever be formed prior to fabricating gate contacts over active portions of the gate stacks. The gate stacks described above may actually be permanent gate stacks as initially formed. Also, the processes described herein may be used to fabricate one or a plurality of semiconductor devices. The semiconductor devices may be transistors or like devices. For example, in an embodiment, the semiconductor devices are a metal-oxide semiconductor (MOS) transistors for logic or memory, or are bipolar transistors. Also, in an embodiment, the semiconductor devices have a three-dimensional architecture, such as a tri-gate device, an independently accessed double gate device, a FIN-FET, a nanowire, or a nanoribbon. One or more embodiments may be particularly useful for fabricating semiconductor devices at a 10 nanometer (10 nm) technology node or sub-10 nanometer (10 nm) technology node.

[0141] Additional or intermediate operations for FEOL layer or structure fabrication may include standard microelectronic fabrication processes such as lithography, etch, thin films deposition, planarization (such as chemical mechanical polishing (CMP)), diffusion, metrology, the use of sacrificial layers, the use of etch stop layers, the use of planarization stop layers, or any other associated action with microelectronic component fabrication. Also, it is to be appreciated that the process operations described for the preceding process flows may be practiced in alternative sequences, not every operation need be performed or additional process operations may be performed, or both.

[0142] Embodiments disclosed herein may be used to manufacture a wide variety of different types of integrated circuits or microelectronic devices. Examples of such integrated circuits include, but are not limited to, processors, chipset components, graphics processors, digital signal processors, micro-controllers, and the like. In other embodiments, semiconductor memory may be manufactured. Moreover, the integrated circuits or other microelectronic devices may be used in a wide variety of electronic devices known in the arts. For example, in computer systems (e.g., desktop, laptop, server), cellular phones, personal electronics, etc. The integrated circuits may be coupled with a bus and other components in the systems. For example, a processor may be coupled by one or more buses to a memory, a chipset, etc. Each of the processor, the memory, and the chipset, may potentially be manufactured using the approaches disclosed herein.

[0143] FIG. **13** illustrates a computing device **1300** in accordance with one implementation of the disclosure. The computing device **1300** houses a board **1302**. The board **1302** may include a number of components, including but not limited to a processor **1304** and at least one communication chip **1306**. The processor **1304** is physically and electrically coupled to the board **1302**. In some implementations the at least one communication chip **1306** is also physically and electrically coupled to the board **1302**. In further implementations, the communication chip **1306** is

part of the processor **1304**.
[0144] Depending on its applications, computing device **1300** may include other components that may or may not be physically and electrically coupled to the board **1302**. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).
[0145] The communication chip **1306** enables wireless communications for the transfer of data to and from the computing device **1300**. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip **1306** may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device **1300** may include a plurality of communication chips **1306**. For instance, a first communication chip **1306** may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip **1306** may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.
[0146] The processor **1304** of the computing device **1300** includes an integrated circuit die packaged within the processor **1304**. In some implementations of embodiments of the disclosure, the integrated circuit die of the processor includes one or more structures, such as integrated circuit structures built in accordance with implementations of the disclosure. The term "processor" may refer to any device or portion of a device that processes electronic data from registers or memory to transform that electronic data, or both, into other electronic data that may be stored in registers or memory, or both.
[0147] The communication chip **1306** also includes an integrated circuit die packaged within the communication chip **1306**. In accordance with another implementation of the disclosure, the integrated circuit die of the communication chip is built in accordance with implementations of the disclosure.
[0148] In further implementations, another component housed within the computing device **1300** may contain an integrated circuit die built in accordance with implementations of embodiments of the disclosure.
[0149] In various embodiments, the computing device **1300** may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultramobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device **1300** may be any other electronic device that processes data.
[0150] FIG. **14** illustrates an interposer **1400** that includes one or more embodiments of the disclosure. The interposer **1400** is an intervening substrate used to bridge a first substrate **1402** to a second substrate **1404**. The first substrate **1402** may be, for instance, an integrated circuit die. The second substrate **1404** may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer **1400** is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer **1400** may couple an integrated circuit die to a ball grid array (BGA) **1406** that can subsequently be

coupled to the second substrate **1404**. In some embodiments, the first and second substrates **1402**/**1404** are attached to opposing sides of the interposer **1400**. In other embodiments, the first and second substrates **1402**/**1404** are attached to the same side of the interposer **1400**. And in further embodiments, three or more substrates are interconnected by way of the interposer **1400**.
[0151] The interposer **1400** may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer **1400** may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.
[0152] The interposer **1400** may include metal interconnects **1408** and vias **1410**, including but not limited to through-silicon vias (TSVs) **1412**. The interposer **1400** may further include embedded devices **1414**, including both passive and active devices. Such devices include, but are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer **1400**. In accordance with embodiments of the disclosure, apparatuses or processes disclosed herein may be used in the fabrication of interposer **1400** or in the fabrication of components included in the interposer **1400**.
[0153] FIG. **15** is an isometric view of a mobile computing platform **1500** employing an integrated circuit (IC) fabricated according to one or more processes described herein or including one or more features described herein, in accordance with an embodiment of the present disclosure.
[0154] The mobile computing platform **1500** may be any portable device configured for each of electronic data display, electronic data processing, and wireless electronic data transmission. For example, mobile computing platform **1500** may be any of a tablet, a smart phone, laptop computer, etc. and includes a display screen **1505** which in the exemplary embodiment is a touchscreen (capacitive, inductive, resistive, etc.), a chip-level (SoC) or package-level integrated system **1510**, and a battery **1513**. As illustrated, the greater the level of integration in the system **1510** enabled by higher transistor packing density, the greater the portion of the mobile computing platform **1500** that may be occupied by the battery **1513** or non-volatile storage, such as a solid state drive, or the greater the transistor gate count for improved platform functionality. Similarly, the greater the carrier mobility of each transistor in the system **1510**, the greater the functionality. As such, techniques described herein may enable performance and form factor improvements in the mobile computing platform **1500**.
[0155] The integrated system **1510** is further illustrated in the expanded view **1520**. In the exemplary embodiment, packaged device **1577** includes at least one memory chip (e.g., RAM), or at least one processor chip (e.g., a multi-core microprocessor and/or graphics processor) fabricated according to one or more processes described herein or including one or more features described herein. The packaged device **1577** is further coupled to the board **1560** along with one or more of a power management integrated circuit (PMIC) **1515**, RF (wireless) integrated circuit (RFIC) **1525** including a wideband RF (wireless) transmitter and/or receiver (e.g., including a digital baseband and an analog front end module further includes a power amplifier on a transmit path and a low noise amplifier on a receive path), and a controller thereof **1511**. Functionally, the PMIC **1515** performs battery power regulation, DC-to-DC conversion, etc., and so has an input coupled to the battery **1513** and with an output providing a current supply to all the other functional modules. As further illustrated, in the exemplary embodiment, the RFIC **1525** has an output coupled to an antenna to provide to implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. In alternative implementations, each of these board-level modules may be

integrated onto separate ICs coupled to the package substrate of the packaged device **1577** or within a single IC (SoC) coupled to the package substrate of the packaged device **1577**.

[0156] In another aspect, semiconductor packages are used for protecting an integrated circuit (IC) chip or die, and also to provide the die with an electrical interface to external circuitry. With the increasing demand for smaller electronic devices, semiconductor packages are designed to be even more compact and must support larger circuit density. Furthermore, the demand for higher performance devices results in a need for an improved semiconductor package that enables a thin packaging profile and low overall warpage compatible with subsequent assembly processing.

[0157] In an embodiment, wire bonding to a ceramic or organic package substrate is used. In another embodiment, a C4 process is used to mount a die to a ceramic or organic package substrate. In particular, C4 solder ball connections can be implemented to provide flip chip interconnections between semiconductor devices and substrates. A flip chip or Controlled Collapse Chip Connection (C4) is a type of mounting used for semiconductor devices, such as integrated circuit (IC) chips, MEMS or components, which utilizes solder bumps instead of wire bonds. The solder bumps are deposited on the C4 pads, located on the top side of the substrate package. In order to mount the semiconductor device to the substrate, it is flipped over with the active side facing down on the mounting area. The solder bumps are used to connect the semiconductor device directly to the substrate.

[0158] FIG. **16** illustrates a cross-sectional view of a flip-chip mounted die, in accordance with an embodiment of the present disclosure.

[0159] Referring to FIG. **16**, an apparatus **1600** includes a die **1602** such as an integrated circuit (IC) fabricated according to one or more processes described herein or including one or more features described herein, in accordance with an embodiment of the present disclosure. The die **1602** includes metallized pads **1604** thereon. A package substrate **1606**, such as a ceramic or organic substrate, includes connections **1608** thereon. The die **1602** and package substrate **1606** are electrically connected by solder balls **1610** coupled to the metallized pads **1604** and the connections **1608**. An underfill material **1612** surrounds the solder balls **1610**.

[0160] Processing a flip chip may be similar to conventional IC fabrication, with a few additional operations. Near the end of the manufacturing process, the attachment pads are metalized to make them more receptive to solder. This typically consists of several treatments. A small dot of solder is then deposited on each metalized pad. The chips are then cut out of the wafer as normal. To attach the flip chip into a circuit, the chip is inverted to bring the solder dots down onto connectors on the underlying electronics or circuit board. The solder is then re-melted to produce an electrical connection, typically using an ultrasonic or alternatively reflow solder process. This also leaves a small space between the chip's circuitry and the underlying mounting. In most cases an electrically-insulating adhesive is then “underfilled” to provide a stronger mechanical connection, provide a heat bridge, and to ensure the solder joints are not stressed due to differential heating of the chip and the rest of the system.

[0161] In other embodiments, newer packaging and die-to-die interconnect approaches, such as through silicon via (TSV) and silicon interposer, are implemented to fabricate high performance Multi-Chip Module (MCM) and System in Package (SiP) incorporating an integrated circuit (IC) fabricated according to one or more processes described herein or including one or more features described herein, in accordance with an embodiment of the present disclosure.

[0162] Thus, embodiments of the present disclosure include integrated circuit structures having direct backside source or drain contacts.

[0163] Although specific embodiments have been described above, these embodiments are not intended to limit the scope of the present disclosure, even where only a single embodiment is described with respect to a particular feature. Examples of features provided in the disclosure are intended to be illustrative rather than restrictive unless stated otherwise. The above description is intended to cover such alternatives, modifications, and equivalents as would be apparent to a

person skilled in the art having the benefit of the present disclosure.
[0164] The scope of the present disclosure includes any feature or combination of features disclosed herein (either explicitly or implicitly), or any generalization thereof, whether or not it mitigates any or all of the problems addressed herein. Accordingly, new claims may be formulated during prosecution of the present application (or an application claiming priority thereto) to any such combination of features. In particular, with reference to the appended claims, features from dependent claims may be combined with those of the independent claims and features from respective independent claims may be combined in any appropriate manner and not merely in the specific combinations enumerated in the appended claims.
[0165] The following examples pertain to further embodiments. The various features of the different embodiments may be variously combined with some features included and others excluded to suit a variety of different applications.
[0166] Example embodiment 1: An integrated circuit structure includes a first plurality of horizontally stacked nanowires laterally spaced apart from a second plurality of horizontally stacked nanowires. A first gate stack is over the first plurality of horizontally stacked nanowires, and a second gate stack is over the second plurality of horizontally stacked nanowires. An epitaxial source or drain structure is between the first plurality of horizontally stacked nanowires and the second plurality of horizontally stacked nanowires, the epitaxial source or drain structure over and electrically coupled to a corresponding conductive backside contact that extends laterally beyond the first epitaxial source or drain structure without contacting the first gate stack or the second gate stack.
[0167] Example embodiment 2: The integrated circuit structure of example embodiment 1, wherein a bottommost surface of the first gate stack and the second gate stack is above a bottommost surface of the epitaxial source or drain structure.
[0168] Example embodiment 3: The integrated circuit structure of example embodiment 1 or 2, wherein the conductive backside contact extends laterally beneath the first gate stack and the second gate stack.
[0169] Example embodiment 4: The integrated circuit structure of example embodiment 1, 2 or 3, wherein the epitaxial source or drain structure includes silicon, germanium and boron.
[0170] Example embodiment 5: The integrated circuit structure of example embodiment 1, 2 or 3, wherein the epitaxial source or drain structure includes silicon and phosphorous.
[0171] Example embodiment 6: An integrated circuit structure includes a first fin laterally spaced apart from a second fin. A first gate stack is over the first fin, and a second gate stack is over the second fin. An epitaxial source or drain structure is between the first fin and the second fin, the epitaxial source or drain structure over and electrically coupled to a corresponding conductive backside contact that extends laterally beyond the first epitaxial source or drain structure without contacting the first gate stack or the second gate stack.
[0172] Example embodiment 7: The integrated circuit structure of example embodiment 6, wherein a bottommost surface of the first gate stack and the second gate stack is above a bottommost surface of the epitaxial source or drain structure.
[0173] Example embodiment 8: The integrated circuit structure of example embodiment 6 or 7, wherein the conductive backside contact extends laterally beneath the first gate stack and the second gate stack.
[0174] Example embodiment 9: The integrated circuit structure of example embodiment 6, 7 or 8, wherein the epitaxial source or drain structure includes silicon, germanium and boron.
[0175] Example embodiment 10: The integrated circuit structure of example embodiment 6, 7 or 8, wherein the epitaxial source or drain structure includes silicon and phosphorous.
[0176] Example embodiment 11: A computing device includes a board, and a component coupled to the board. The component includes an integrated circuit structure including a first plurality of horizontally stacked nanowires or fin laterally spaced apart from a second plurality of horizontally

stacked nanowires or fin. A first gate stack is over the first plurality of horizontally stacked nanowires or fin, and a second gate stack is over the second plurality of horizontally stacked nanowires or fin. An epitaxial source or drain structure is between the first plurality of horizontally stacked nanowires or fin and the second plurality of horizontally stacked nanowires or fin, the epitaxial source or drain structure over and electrically coupled to a corresponding conductive backside contact that extends laterally beyond the first epitaxial source or drain structure without contacting the first gate stack or the second gate stack.
[0177] Example embodiment 12: The computing device of example embodiment 11, including the first plurality of horizontally stacked nanowires and the second plurality of horizontally stacked nanowires.
[0178] Example embodiment 13: The computing device of example embodiment 11, including the first fin and the second fin.
[0179] Example embodiment 14: The computing device of example embodiment 11, 12 or 13, further including a memory coupled to the board.
[0180] Example embodiment 15: The computing device of example embodiment 11, 12, 13 or 14, further including a communication chip coupled to the board.
[0181] Example embodiment 16: The computing device of example embodiment 11, 12, 13, 14 or 15, further including a battery coupled to the board.
[0182] Example embodiment 17: The computing device of example embodiment 11, 12, 13, 14, 15 or 16, further including a camera coupled to the board.
[0183] Example embodiment 18: The computing device of example embodiment 11, 12, 13, 14, 15, 16 or 17, further including a display coupled to the board.
[0184] Example embodiment 19: The computing device of example embodiment 11, 12, 13, 14, 15, 16, 17 or 18, wherein the component is a packaged integrated circuit die.
[0185] Example embodiment 20: The computing device of example embodiment 11, 12, 13, 14, 15, 16, 17, 18 or 19, wherein the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor.

Claims

1. An integrated circuit structure, comprising: a first plurality of horizontally stacked nanowires laterally spaced apart from a second plurality of horizontally stacked nanowires; a first gate stack over the first plurality of horizontally stacked nanowires, and a second gate stack over the second plurality of horizontally stacked nanowires; and an epitaxial source or drain structure between the first plurality of horizontally stacked nanowires and the second plurality of horizontally stacked nanowires, the epitaxial source or drain structure over and electrically coupled to a corresponding conductive backside contact that extends laterally beyond the epitaxial source or drain structure without contacting the first gate stack or the second gate stack.
2. The integrated circuit structure of claim 1, wherein a bottommost surface of the first gate stack and the second gate stack is above a bottommost surface of the epitaxial source or drain structure.
3. The integrated circuit structure of claim 1, wherein the conductive backside contact extends laterally beneath the first gate stack and the second gate stack.
4. The integrated circuit structure of claim 1, wherein the epitaxial source or drain structure comprises silicon, germanium and boron.
5. The integrated circuit structure of claim 1, wherein the epitaxial source or drain structure comprises silicon and phosphorous.
6. An integrated circuit structure, comprising: a first fin laterally spaced apart from a second fin; a first gate stack over the first fin, and a second gate stack over the second fin; and an epitaxial source or drain structure between the first fin and the second fin, the epitaxial source or drain structure over and electrically coupled to a corresponding conductive backside contact that extends

laterally beyond the epitaxial source or drain structure without contacting the first gate stack or the second gate stack.

7. The integrated circuit structure of claim 6, wherein a bottommost surface of the first gate stack and the second gate stack is above a bottommost surface of the epitaxial source or drain structure.

8. The integrated circuit structure of claim 6, wherein the conductive backside contact extends laterally beneath the first gate stack and the second gate stack.

9. The integrated circuit structure of claim 6, wherein the epitaxial source or drain structure comprises silicon, germanium and boron.

10. The integrated circuit structure of claim 6, wherein the epitaxial source or drain structure comprises silicon and phosphorous.

11. A computing device, comprising: a board; and a component coupled to the board, the component including an integrated circuit structure, comprising: a first plurality of horizontally stacked nanowires or fin laterally spaced apart from a second plurality of horizontally stacked nanowires or fin; a first gate stack over the first plurality of horizontally stacked nanowires or fin, and a second gate stack over the second plurality of horizontally stacked nanowires or fin; and an epitaxial source or drain structure between the first plurality of horizontally stacked nanowires or fin and the second plurality of horizontally stacked nanowires or fin, the epitaxial source or drain structure over and electrically coupled to a corresponding conductive backside contact that extends laterally beyond the epitaxial source or drain structure without contacting the first gate stack or the second gate stack.

12. The computing device of claim 11, comprising the first plurality of horizontally stacked nanowires and the second plurality of horizontally stacked nanowires.

13. The computing device of claim 11, comprising the first fin and the second fin.

14. The computing device of claim 11, further comprising: a memory coupled to the board.

15. The computing device of claim 11, further comprising: a communication chip coupled to the board.

16. The computing device of claim 11, further comprising: a battery coupled to the board.

17. The computing device of claim 11, further comprising: a camera coupled to the board.

18. The computing device of claim 11, further comprising: a display coupled to the board.

19. The computing device of claim 11, wherein the component is a packaged integrated circuit die.

20. The computing device of claim 11, wherein the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor.