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Superconducting device including set of circuits having different operational temperature requirements with multiple thermal sinks and multiple ground planes

Abstract

An integrated circuit is provided that comprises a first thermal sink layer, a first ground plane associated with a first set of circuits that have a first operational temperature requirement, a first thermally conductive via that couples the first ground plane to the first thermal sink layer, a second thermal sink layer, a second ground plane associated with a second set of circuits that have a second operational temperature requirement that is higher than the first operational temperature requirement, and a second thermally conductive via that couples the second ground plane to the second thermal sink layer. The first thermal sink layer is cooled at a first temperature to maintain the first set of circuits at the first operational temperature requirement and the second thermal sink layer is cooled at a second temperature to maintain the second set of circuits at the second operational temperature requirement.

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Background/Summary

RELATED APPLICATIONS (1) This application is a divisional application of U.S. patent application Ser. No. 17/222,238, filed 5 Apr. 2021, issued as U.S. Pat. No. 12,027,437, which claims priority from U.S. patent application Ser. No. 16/227,965, filed 20 Dec. 2018, issued as U.S. Pat. No. 11,004,763, which is incorporated herein in its entirety.

TECHNICAL FIELD

(1) The present invention relates generally to integrated circuits, and more particularly to a superconducting device with multiple thermal sinks.

BACKGROUND

(2) Monolithic Microwave Integrated circuit (MMIC) chips operating at cryogenic temperatures have superconducting circuits that need to be thermally managed by removing the heat from the superconducting circuits down towards the substrate. Under cryogenic temperature conditions, heat load, cooling resources, temperature, and circuit complexity are strongly tied to each other. Portions of devices on the MMIC need to be maintained at lower temperatures than other components which can operate at higher temperatures. This requires the entire MMIC to be held at the colder temperature. It is far more inefficient to lift one unit of power from cryogenic temperatures to room temperature than it is if that same power is lifted from a higher temperature to room temperature. As cryogenic chips become more and more complex, a greater number and greater variation of devices are populating the MMICs. Each of these devices can have different operational temperature requirements.

(3) A typical cryogenic MMIC consists of a silicon substrate topped with alternating layers of electrically conducting material and dielectric. Multiple device types can exist in the MMIC. As an example, a MMIC may have three different device types that need to run at three different operating temperatures. For example, a first device may need to operate below 500 millikelvin (mK), a second device may need to operate below 1 Kelvin (K), and a third device may need to operate below 4 K. With a single ground plane, the entire mesh layer will be at a near uniform temperature. This is due to the ability of the electrically conducting material to transport (spread) the heat laterally in the X and Y directions. Therefore, if all devices are connected to this ground plane, all will have to be maintained to the most stringent operating requirement, for example, 500 mK. That is since the third device only needs to be kept at 4 K, but is instead maintained at 0.5 K (8 times lower temperature), then more than 8 times the cooling resources are needed to manage this sector of the MMIC.

SUMMARY

(4) In one example, an integrated circuit is provided that comprises a first thermal sink layer, a first ground plane associated with a first set of circuits that have a first operational temperature requirement, and a first thermally conductive via that couples the first ground plane to the first thermal sink layer. The integrated circuit also comprises a second thermal sink layer, a second ground plane associated with a second set of circuits that have a second operational temperature requirement that is higher than the first operational temperature requirement, and a second thermally conductive via that couples the second ground plane to the second thermal sink layer. The first thermal sink layer is cooled at a first temperature to maintain the first set of circuits at the first operational temperature requirement and the second thermal sink layer is cooled at a second temperature to maintain the second set of circuits at the second operational temperature requirement.

(5) In another example, a monolithic microwave integrated circuit (MMIC) is provided that comprises a first electrically conducting ground plane associated with a first set of superconducting circuits that have a first operational temperature requirement, a second electrically conducting

ground plane associated with a second set of superconducting circuits that have a second operational temperature requirement that is higher than the first operational temperature requirement, a first thermal sink layer disposed one of above or below the first and second electrically conducting ground planes, and a second thermal sink layer disposed the other of above or below the first and second electrically conducting ground planes. The MMIC further comprises a first set of thermally conductive vias that each couple the first electrically conducting ground plane to the first thermal sink layer through the substrate, and a second set of thermally conductive vias that each couple the second ground plane to a second thermal sink layer.

(6) In yet another example, an integrated circuit is provided that comprises a plurality of thermal sink layers with each thermal sink layer being thermally isolated from each other thermal sink layer; and a plurality of ground planes each being associated with a respective set of circuits that each have a differential operational temperature requirement than the other. Each of the plurality of ground planes are coupled to a respective thermal sink layer by a respective thermal via, wherein each thermal sink layer is cooled at a respective temperature to maintain its coupled ground plane at its respective operational temperature requirement.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

(1) FIG. **1** illustrates a cross-sectional view of a portion of an example integrated circuit.

(2) FIG. **2** illustrates a cross-sectional view of a portion of another example integrated circuit.

(3) FIG. **3** illustrates a cross-sectional view of the portion of the integrated circuit along the lines A-A of FIG. **2**.

(4) FIG. **4** illustrates a cross-sectional view of the portion of the integrated circuit along the lines B-B of FIG. **2**.

(5) FIG. **5** illustrates a cross-sectional view of a portion of yet another example integrated circuit.

DETAILED DESCRIPTION

(6) The present disclosure describes an integrated circuit (e.g., Monolithic Microwave Integrated circuit (MMIC)) that includes separate dedicated ground planes for sets of circuits that run at different operating temperature requirements. Each separate ground plane is coupled to a respective thermal sink layer by one or more associated thermal vias (contacts). Each thermal sink layer can be cooled at a given temperature appropriately in a cooling temperature zone to allow for adequate heat sinking from respective separate ground planes to maintain the respective sets of circuits at their desired operating temperature requirement. In this manner, each thermal sink layer does not need to be held at the lowest temperature to maintain an operational requirement, but only its respective operational temperature requirement, such that the necessary power to refrigerate the entire device is reduced.

(7) Certain examples will be illustrated with respect to electrically conducting ground planes and associated superconducting circuits with different operational temperature requirements. However, other examples can include mixture of electrically conducting ground planes and associated superconducting circuitry and non-superconducting ground planes and associated circuitry, or a mixture of non-superconducting circuitry and associated circuitry with different operational temperature requirements.

(8) FIG. **1** illustrates cross-sectional view of an example of a portion of an integrated circuit **10**. The portion of the integrated circuit **10** includes a first dielectric layer **16** overlying a substrate **14**, a second dielectric layer **18** overlying the first dielectric layer **16**, and a third dielectric layer **20** overlying the second dielectric layer **18**. The substrate **14** can be formed of silicon, glass or other substrate material. A first thermal sink layer **12** resides at a bottom of the substrate **14**, and a second thermal sink layer **34** resides on a top surface of the integrated circuit **10**. The first dielectric layer

16 provides a buffer layer between the substrate and the active circuits of the integrated circuit **10**. A first electrically conducting ground plane **22** and a first set of superconducting circuits **24** are disposed in the second dielectric layer **18**, and a second electrically conducting ground plane **28** and a second set of circuits **30** resides in the third dielectric layer **20**. The first electrically conducting ground plane **22** and the first set of superconducting circuits **24** have a first operating temperature requirement and the second electrically conducting ground plane **28** and a second set of superconducting circuits **30** have a second operating temperature requirement.

(9) The first operating temperature requirement is different and lower than the second operating temperature requirement, which makes the second operating temperature requirement higher than the first operating temperature requirement. The term operating temperature requirement refers to an operating temperature that a circuit material of a ground plane and set of circuits needs to operate at or below to maintain their properties. For example, the first electrically conducting ground plane and a first set of superconducting circuits may include the utilization of Aluminum, which needs to maintain an operating temperature of at or below 500 milliKelvin for proper operation, while the second electrically conducting ground plane and a second set of circuits may include the utilization of Niobium, which needs to maintain an operating temperature of at or below 4.2 Kelvin for proper operation. That means a set of circuits with a lower operating temperature requirement needs more cooling resources per watt of dissipated power than a set of circuits with a higher operating temperature requirement.

(10) A first thermal via **26** connects the first electrically conducting ground plane **22** to the first thermal sink layer **12**, and a second thermal via **32** connects the second electrically conducting ground plane **28** to the second thermal sink layer **34**. The first thermal sink layer **12** and the second thermal sink layer **34** are both formed of a thermal conductive material. A thermal conductive material is a material that is a relatively good thermal conductor, such that it readily transfers heat. A superconductive material is a good electrically conductive material but a poor thermal conductive material (compared to a normal metal that is not superconducting). Therefore, neither the first thermal sink layer **12** or the second terminal sink layer **34** are formed of a superconductive material. Additionally, the first thermal via **26** and the second thermal via **32** can be formed of a thermal conductive material. That is a material that is relatively good at conducting heat from the electrically conducting ground layers to the respective thermal sink layers. The first thermal sink layer **12** can be cooled in a first cooling temperature zone by a first external cooling source to hold the first thermal sink layer **12** at or below a first temperature, and the second thermal sink layer **34** can be cooled in a second cooling temperature zone by a second external cooling source to hold the second thermal sink layer **34** at or below a second temperature that is higher than the first temperature. The first external source and the second external source can be from different cooling devices, or different stages of the same cooling device. In one example, the first thermal sink layer **12**, the second thermal sink layer **34**, the first thermal via **26** and the second thermal via **32** are all formed of copper. Alternative examples of thermally conductive materials include gold, silver, tungsten, molybdenum, iridium, and rhodium.

(11) Dielectric layer **18** must be thick enough to prevent coupling between phonons in layer **28** and phonons in layers **22** and **24**. The minimum thickness for decoupling these layers is set by the dominant phonon wavelength in dielectric **18** at the lower operating temperature in the circuits of layer **24**. To prevent direct coupling between these layers, dielectric layer **18** should be thicker than 4 phonon wavelengths. For example, in silicon dioxide the dominant phonon wavelength at 500 mK is 21 nanometers, so a dielectric layer **18** made of silicon dioxide should be at least 84 nanometers thick. When dielectric layer **18** is thick, the thermal boundary resistance between metals and dielectrics will minimize heat flow between the metal layers. Phonons in metals do not match well to phonons in dielectrics. This acoustic boundary resistance is a significant barrier to heat flow from layer **28** into layer **18** and from layer **18** into layers **22** and **24**. A sufficiently thick dielectric layer **18** eliminates coupling between evanescent metal layer phonon waves and prevents

phonons from hopping across the dielectric barrier.
(12) Therefore, the temperature of the first electrically conducting ground plane **22** and first set of superconducting circuits **24** can be maintained at a lower temperature than the second electrically conducting ground plane **28** and second set of superconducting circuits **30** by using different thermal sink layers held at different temperature at different cooling temperature zones by different cooling sources. The first thermal sink layer **12** can be cooled to a temperature that can be at or below the first operating temperature requirement to maintain the first electrically conducting ground plane **22** and the first set of superconducting circuits **24** at the first operating temperature requirement, and the second thermal sink layer **12** can be cooled to a temperature that can be at or below the second operating temperature requirement to maintain the second electrically conducting ground plane **28** and the second set of superconducting circuits **30** at the second operating temperature requirement.
(13) Although FIG. **1** illustrates a single first thermal via **26** and a single second thermal via **32**, there can be a greater number of first thermal vias and second thermal vias to maintain the temperature of the first electrically conducting ground plane **22** and the first set of superconducting circuits **24** at or below the first operating temperature requirement, and the second electrically conducting ground plane **28** and the second set of superconducting circuits **30** at or below the second operating temperature requirement.
(14) FIG. **2** illustrates cross-sectional view of portion of another example integrated circuit **40**. The portion of the integrated circuit **40** includes a first dielectric layer **46** overlying a substrate **44**, a second dielectric layer **48** overlying the first dielectric layer **46**, and a third dielectric layer **50** overlying the second dielectric layer **48**. The substrate **44** can be formed of silicon, glass or other substrate material. A first thermal sink layer **42** resides at a bottom of the substrate **44**, and a second thermal sink layer **64** resides on a top surface of the integrated circuit **40**. The first dielectric layer **46** provides a buffer layer between the substrate **44** and the active circuits of the integrated circuit **40**. A first electrically conducting ground plane **52** and a first set of superconducting circuits **54** are disposed in the second dielectric layer **48**, and a second electrically conducting ground plane **56** and a second set of circuits **58** are disposed in the second dielectric layer **48** in an adjacent relationship to first electrically conducting ground plane **52** and the first set of superconducting circuits **54**. The first electrically conducting ground plane **52** and the first set of superconducting circuits **54** have a first operating temperature requirement and the second electrically conducting ground plane **56** and a second set of superconducting circuits **58** have a second operating temperature requirement.
(15) In this example, the first operating temperature requirement is different and lower than the second operating temperature requirement, such that the second operating temperature requirement is higher than the first operating temperature requirement similar to the example in FIG. **1**. The first electrically conducting ground plane **52** and the first set of superconducting circuits **54** may include the utilization of Aluminum, which needs to maintain an operating temperature of at or below 500 milliKelvin for proper operation, while the second superconducting ground plane **56** and the second set of superconducting circuits **58** may include the utilization of Niobium, which needs to maintain an operating temperature of at or below 4 Kelvin for proper operation.
(16) A first set of thermal vias **62** connects the first electrically conducting ground plane **52** to the first thermal sink layer **42**, and a second set of thermal vias **60** connects the second electrically conducting ground plane **56** to the second thermal sink layer **64**. The first thermal sink layer **42** and the second thermal sink layer **64** are formed of a thermal conductive material. Additionally, the first set of thermal vias **62** and the second set of thermal vias **60** can be formed of a thermal conductive material. In one example, the first thermal sink layer **42**, the second thermal sink layer **64**, the first set of thermal vias **62** and the second set of thermal vias **60** are all formed of copper.
(17) The first thermal sink layer **42** can be cooled in a first cooling temperature zone by a first external cooling source to hold the first thermal sink layer **42** at or below a first temperature, and

the second thermal sink layer **64** can be cooled in a second cooling temperature zone by a second external cooling source to hold the second thermal sink layer **64** at or below a second temperature that is higher than the first temperature. Again, the first external source and the second external source can be from different cooling devices, or different stages of the same cooling device.

(18) FIG. **3** illustrates a cross-sectional view of the portion of the integrated circuit **40** along the lines A-A. FIG. **4** illustrates a cross-sectional view of the portion of the integrated circuit **40** along the lines B-B. As illustrated in FIGS. **3-4**, the cross section of thermally conductive material associated with the first set of thermal vias **62** is the same as the cross section of thermally conductive material associated with the second set of thermal vias **60**. However, based on a desired design and cooling requirements the number and size of the thermal vias for either or both of the first and second set of thermal vias can be varied to achieve the desired cooling requirements as efficiently as possible.

(19) The examples of FIGS. **1-4** illustrate integrated circuits utilizing two different thermal sink layers subjected to two different temperature cooling zones to maintain circuits and ground planes with two different operating temperature requirements at or below their respective desired temperatures without subjecting the entire integrated circuit to the lowest temperature requirement thus saving the necessary energy required to maintain proper operation of all circuits in the integrated circuit. However, other examples can include more than two cooling temperature zones and associated thermal sink layers to maintain proper operation of circuits with three or more different operating temperature requirements based on practical limitations.

(20) FIG. **5** illustrates a cross-sectional view of a portion of yet another example of an integrated circuit **70**. The portion of the integrated circuit **70** includes a first dielectric layer **80** overlying a substrate **78**, a second dielectric layer **82** overlying the first dielectric layer **80**, and a third dielectric layer **84** overlying the second dielectric layer **82**. The substrate **78** can be formed of silicon, glass or other substrate material. A first thermal sink layer **72** resides at a first side at a bottom of the substrate **78**, and a second thermal sink layer **76** resides at a second side at the bottom of the substrate **78** separated from one another by a separation region **74** that can be, for example, an insulation region. A first electrically conducting ground plane **86** and a first set of circuits **88** are disposed in the first dielectric layer **80**, and a second electrically conducting ground plane **90** and a second set of circuits **92** resides in the first dielectric layer **80** in an adjacent relationship to first electrically conducting ground plane **86** and the first set of circuits **88**. The first electrically conducting ground plane **86** and the first set of circuits **88** have a first operating temperature requirement and the second electrically conducting ground plane **90** and the second set of circuits **92** have a second operating temperature requirement.

(21) A third thermal sink layer **110** resides at a first side at a top surface of the integrated circuit **70**, and a fourth thermal sink layer **114** resides at a second side at the top surface of the integrated circuit **70** separated from one another by a separation region **112** that can be, for example, an insulation region. A third electrically conducting ground plane **98** and a third set of circuits **100** are disposed in the second dielectric layer **82**, and a fourth electrically conducting ground plane **102** and a fourth set of circuits **104** resides in the second dielectric layer **82** in an adjacent relationship to third electrically conducting ground plane **98** and the third set of circuits **100**. The third electrically conducting ground plane **98** and the third set of circuits **100** have a third operating temperature requirement and the fourth electrically conducting ground plane **102** and the fourth set of circuits **104** have a fourth operating temperature requirement.

(22) A first thermal via **94** connects the first electrically conducting ground plane **86** to the first thermal sink layer **72**, and a second thermal via **96** connects the second electrically conducting ground plane **90** to the second thermal sink layer **76**. Additionally, a third thermal via **106** connects the third electrically conducting ground plane **98** to the third thermal sink layer **110**, and a fourth thermal via **108** connects the fourth electrically conducting ground plane **102** to the fourth thermal sink layer **114**. Each of the thermal sink layers are formed of a thermal conductive material. The

first thermal sink layer **72** can be cooled in a first cooling temperature zone by a first external cooling source to hold the first thermal sink layer **72** at or below a first temperature, and the second thermal sink layer **76** can be cooled in a second cooling temperature zone by a second external cooling source to hold the second thermal sink layer **76** at or below a second temperature that is higher than the first temperature.
(23) Furthermore, the third thermal sink layer **110** can be cooled in a third cooling temperature zone by a third external cooling source to hold the third thermal sink layer **110** at or below a third temperature, and the fourth thermal sink layer **114** can be cooled in a fourth cooling temperature zone by a fourth external cooling source to hold the fourth thermal sink layer **114** at or below a fourth temperature. Each thermal sink layer is thermally isolated from the other thermal sink layers. Each of the first temperature, the second temperature, the third temperature and the fourth temperature are different from one another. The first external source, the second external source, the third external source and the fourth external source can each be from different cooling devices, or different stages of the same cooling device. Additionally, each of the first set of circuits, the second set of circuits, the third set of circuits and the fourth set of circuits can be one of superconducting circuits or non-superconducting circuits, such that the integrated circuit can include both conventional circuits running at one or more different temperature requirements and superconducting circuits running at one or more different temperature requirements.
(24) What have been described above are examples of the invention. It is, of course, not possible to describe every conceivable combination of components or methodologies for purposes of describing the invention, but one of ordinary skill in the art will recognize that many further combinations and permutations of the invention are possible. Accordingly, the invention is intended to embrace all such alterations, modifications, and variations that fall within the scope of this application, including the appended claims.

Claims

1. A circuit comprising: a first dielectric layer comprising a first electrically conducting ground plane and a first set of circuits that have a first operational temperature requirement, the first dielectric layer further comprising a second electrically conducting ground plane and a second set of circuits that have a different operational temperature requirement than the first electrically conducting ground plane and the first set of circuits; a second dielectric layer comprising a third electrically conducting ground plane and a third set of circuits that have a third operational temperature requirement, the second dielectric layer further comprising a fourth electrically conducting ground plane and a fourth set of circuits that have a different operational temperature requirement than the third electrically conducting ground plane and the third set of circuits; a plurality of thermal sink layers; and a plurality of conductive vias, wherein at least one conductive via of the plurality of conductive vias couples one of the first, second, third, and fourth electrically conducting ground planes to one of the plurality of thermal sink layers.
2. The circuit of claim 1, wherein each thermal sink layer of the plurality of thermal sink layers is cooled at a different temperature to maintain the first, second, third, and fourth set of circuits at different operational temperatures.
3. The circuit of claim 1, wherein the first electrically conducting ground plane and the first set of circuits are adjacent to and physically separated from the second electrically conducting ground plane and the second set of circuits.
4. The circuit of claim 3, wherein the third electrically conducting ground plane and the third set of circuits are adjacent to and physically separated from the fourth electrically conducting ground plane and the fourth set of circuits.
5. The circuit of claim 1, wherein the plurality of thermal sink layers comprises: a first thermal sink layer; a second thermal sink layer; a third thermal sink layer; and a fourth thermal sink layer.

6. The circuit of claim 5, wherein the first thermal sink layer and the second thermal sink layer are separated by a first separation region, and the third thermal sink layer and the fourth thermal sink layer are separated by a second separation region.
7. The circuit of claim 6, wherein the plurality of conductive vias comprises: a first conductive via; a second conductive via; a third conductive via; and a fourth conductive via.
8. The circuit of claim 7, wherein the first conductive via couples the first electrically ground plane to the first thermal sink layer, the second conductive via couples the second electrically ground plane to the second thermal sink layer, the third conductive via couples the third electrically ground plane to the third thermal sink layer, and the fourth conductive via couples the fourth electrically ground plane to the fourth thermal sink layer.
9. The circuit of claim 1, wherein the plurality of thermal sink layers and the plurality of conductive vias are formed of copper.
10. The circuit of claim 1, wherein the first, second, third, and fourth set of circuits correspond to first, second, third, and fourth set of superconducting circuits.
11. The circuit of claim 1, wherein the circuit is a Monolithic Microwave Integrated circuit.