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Array substrate and manufacturing method thereof

Abstract

An array substrate and a manufacturing method thereof are provided. A metal film layer is formed on an active layer of the array substrate. The metal film layer protects the active layer from being damaged by an etchant liquid or dry etching process during patterning processing of a source electrode/a drain electrode. Afterwards, a portion of the metal film layer that corresponds to a channel of the active layer the channel is subjected to oxidizing processing to form an oxide layer to help keep the functional property of the active layer. In the entire manufacturing process of the array substrate, the active layer will not be subject to damage in subsequent processing and stability of the device can be maintained.

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Background/Summary

FIELD OF INVENTION
(1) The present invention relates to display technologies, and more particularly, to an array substrate and a manufacturing method thereof.
BACKGROUND OF INVENTION
(2) Oxide thin-film transistor (Indium Gallium Zinc Oxide, IGZO) technology has been considered a substitute of the amorphous silicon thin-film transistor technology as a main stream technique for the next-generation display-driving backplanes. Compared with the amorphous silicon thin-film transistor technology, the oxide thin-film transistor technology features high mobility (μ>10 cm2/Vs), good large-area homogeneity, and low production cost.
(3) Technical problem: since the oxide thin-film transistors, particularly oxide thin-film transistors adopting a back channel etch (BCE) structure, suffer certain problems in respect of stability, in the manufacturing process of a known BCE structured based oxide thin-film transistor, an oxide channel portion that is exposed is directly subjected to influences caused by an etchant liquid for source/drain metals or a dry etching process, and this leads to poor stability of the device. To prevent the oxide channel from being damaged, a conventional etch stop structure based oxide thin-film transistor includes an SiOx insulation film layer to block the damage, yet this adds one more SiOx film forming process and one more mask, and thus increases operation steps and cost.
(4) Thus, it is a technical issue to be immediately resolved to improve the stability of an oxide thin-film transistor, especially improving the stability of a BCE structure based oxide thin-film transistor.
SUMMARY OF INVENTION
(5) Embodiments of the disclosure provide an array substrate and a manufacturing method thereof, for resolving the technical issues that in a manufacturing process, an oxide channel of a known back-channel-etch type oxide thin-film transistor is exposed and may be wrongly etched easily and get damaged in subsequent operations, so as to cause lowering of the stability of the device.
(6) To resolve the above technical issues, the present invention provides an array substrate, which comprises: a base; a primary gate electrode, which is located on the base; an active layer, which is located on the primary gate electrode; an etch stop layer, which is located on the active layer; and a source electrode and a drain electrode, which are located on the etch stop layer; wherein the source electrode and the drain electrode partly cover the etch stop layer, and an area of the etch stop layer is not covered by the source electrode and the drain electrode and is arranged as an oxidized metal layer, the oxidized metal layer being arranged to correspond, in position, to the active layer and the primary gate electrode.

(7) According to an embodiment of the present invention, the source electrode and the drain electrode are both provided with a metal connection layer arranged thereon, and the drain electrode is connected through the metal connection layer to a pixel.
(8) According to an embodiment of the present invention, a material of the metal connection layer comprises any one of Mo, MoTi, and MoNi.
(9) According to an embodiment of the present invention, the base is further provided with a passivation layer arranged thereon, and the passivation layer at least covers the oxidized metal layer and the metal connection layer located on the source electrode and the drain electrode; and the passivation layer is formed with a through hole, and the through hole corresponds, in position, to the metal connection layer located on the drain electrode.
(10) According to an embodiment of the present invention, the passivation layer comprises a first sub-passivation layer and a second sub-passivation layer that are arranged to stack on each other, the first sub-passivation layer being partly in contact with the oxidized metal layer, a material of the first sub-passivation layer comprising silicon oxides.
(11) According to an embodiment of the present invention, the oxide thin-film transistor further comprises a secondary gate electrode, the secondary gate electrode being located above the oxidized metal layer and corresponding, in position, to the oxidized metal layer; and the secondary gate electrode is arranged between the first sub-passivation layer and the second sub-passivation layer.
(12) According to an embodiment of the present invention, a material of the etch stop layer comprises Ti, and a film thickness of the etch stop layer is 5 nm to 10 nm.
(13) According to an embodiment of the present invention, a thickness of a layer in which the source electrode and the drain electrode are located is 3 to 5 times of a film thickness of the etch stop layer or the metal connection layer.
(14) According to the array substrate provided in the present invention, a manufacturing method for the array substrate is further provided, the method comprising the following steps: S**10**: providing a base, and forming a primary gate electrode, a gate insulation layer, and an active layer on the base; S**20**: forming a combined metal layer on the active layer, wherein the combined metal layer comprises an etch stop layer, a source-drain metal layer, and a metal connection layer that are arranged to stack on each other; S**30**: subjecting metal layers of the combined metal layer that are other than the etch stop layer to patterning processing to form a source electrode and a drain electrode located on the etch stop layer and the metal connection layer located on the source electrode and the drain electrode; S**40**: subjecting a zone of the etch stop layer that is not covered by the source electrode and the drain electrode to oxidizing processing to form an oxidized metal layer, wherein the oxidized metal layer and the active layer are arranged to correspond, in position, to each other; and S**50**: forming a passivation layer on a film layer formed in Step S**40**.
(15) According to an embodiment of the present invention, Step S**30** comprises: subjecting the metal connection layer and the source-drain metal layer to the patterning processing with wet etching to form the source electrode and the drain electrode and the metal connection layer on the source electrode and the drain electrode.
(16) According to an embodiment of the present invention, a material of the metal connection layer comprises any one of Mo, MoTi, and MoNi.
(17) According to an embodiment of the present invention, a material of the etch stop layer comprises Ti; and
(18) "subjecting a zone of the etch stop layer that is not covered by the source electrode and the drain electrode to oxidizing processing" of Step S**40** comprises:
(19) applying O2 plasma to subject the etch stop layer to oxidizing process, wherein a zone of the etch stop layer that is subjected to the oxidizing processing reacts and forms a TiO oxide metal layer.
(20) According to an embodiment of the present invention, a film thickness of the etch stop layer is

5 nm to 10 nm.
(21) According to an embodiment of the present invention, a thickness of a layer in which the source electrode and the drain electrode are located is 3 to 5 times of a film thickness of the etch stop layer or the metal connection layer.
(22) According to an embodiment of the present invention, Step S**50** comprises: S**501**: forming a first sub-passivation layer on a film layer formed in Step S**40**; S**502**: forming a secondary gate electrode on the first sub-passivation layer, wherein the secondary gate electrode and the oxidized metal layer are arranged to correspond, in position, to each other; and S**503**: forming a second sub-passivation layer on the first sub-passivation layer, wherein the second sub-passivation layer covers the secondary gate electrode.
(23) According to an embodiment of the present invention, Step S**50** further comprises: S**504**: forming through holes in the first sub-passivation layer and the second sub-passivation layer to be in communication with each other, wherein the through holes correspond, in position, to the metal connection layer on the source electrode or the metal connection layer on the drain electrode.
(24) According to an embodiment of the present invention, a material of the first sub-passivation layer comprises silicon oxides.
(25) The beneficial effect of the present disclosure is that: compared to the prior art, the array substrate and the manufacturing thereof provided in the present invention are such that a metal film layer is formed on an active layer of an oxide thin-film transistor, and the metal film layer protects the active layer from being damaged by an etchant liquid or dry etching processing in subsequent patterning processing of source/drain electrodes, and afterwards, a portion of the metal film layer that corresponds to a channel of the active layer is subjected to oxidization processing to form an oxide layer to help keep the functional property of the active layer; and in the entire manufacturing process of the array substrate, the active layer will not be subject to damage in subsequent processing and stability of the device can be maintained.

Description

DESCRIPTION OF DRAWINGS
(1) To describe the embodiments or the technical solutions of the prior art more clearly, the following provides a brief description of drawings that are necessary for the description of the embodiments or the prior art. Obviously, the drawings as described below disclose only some embodiments, and for those having ordinary skill in the field, other drawings may be contemplated according to the attached drawings without making creative endeavor.
(2) FIG. **1** is a schematic structural diagram of an array substrate provided in the present invention.
(3) FIGS. **2***a*-**2***g* are schematic structural diagrams showing a flow of manufacturing an array substrate provided in the present invention.
(4) FIG. **3** is a flow chart of manufacturing an array substrate provided in the present invention.
DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS
(5) The description of the embodiments provided below make reference to the attached drawings to provide an example illustration of specific embodiments in which the disclosure may be implemented. Direction related terms as used herein, such as “up”, “down”, “front”, “rear”, “left”, “right”, “inside”, “outside”, and “lateral side”, indicate directions referring to the attached drawings. Thus, using the direction related terms is for illustration and understanding of the disclosure, and is not intended to limit the disclosure. In the drawings, units having similar structures are designated with the same reference numerals.
(6) A further description of the disclosure will be provided below with reference to the attached drawings and embodiments.
(7) An embodiment of the disclosure provides an array substrate, and a detailed description will be

provided below with reference to FIG. **1**.

(8) Referring to FIG. **1**, FIG. **1** is a schematic structural diagram of an array substrate provided in an embodiment of the disclosure. The array substrate provided in the present invention comprises the base **101**. A primary gate electrode **102** is formed on the base **101**. The primary gate electrode **102** is covered with a gate insulation layer **103**. An active layer **104** is formed on the gate insulation layer **103**, and the active layer **104** and the primary gate electrode **102** correspond in position to each other. A first layer of metal is formed on the active layer **104** and the gate insulation layer **103** to serve as an etch stop layer **105** of the active layer **104**. A second layer of metal is formed on the etch stop layer **105** to serve as a source electrode **1061** and a drain electrode **1062**. A third layer of metal is formed on both the source electrode **1061** and the drain electrode **1062** to serve as a metal connection layer **107** connecting the drain electrode **1062** to a pixel. A passivation layer is formed on the film stack structure that is formed as above in order to form an oxide thin-film transistor of the array substrate provided in the present invention.

(9) The etch stop layer **105** is arranged to cove the active layer **104**. The etch stop layer **105** comprises an oxidized metal area corresponding to a middle portion of the active layer **104** and non-oxidized areas oppositely arranged at two ends of the oxidized metal area. The metal oxide area of the etch stop layer **105** can be arranged as an oxidized metal layer and also functions as a channel **108** of the active layer **104**. The source electrode **1061** and the drain electrode **1062** partly cover the etch stop layer **105**. Parts of the etch stop layer **105** that are covered by the source electrode **1061** and the drain electrode **1062** are the non-oxidized areas of the etch stop layer **105**. A part of the etch stop layer **105** that is not covered by the source electrode **1061** and the drain electrode **1062** is the oxidized metal area of the etch stop layer **105**.

(10) The source electrode **1061** and the drain electrode **1062** respectively lap over two ends of the active layer **104** by means of the non-oxidized areas of the etch stop layer **105**. The source electrode **1061** and the drain electrode **1062** are spaced from each other and are arranged to avoid the oxidized metal area. Further, the source electrode **1061** and the drain electrode **1062** are each a non-planar structure and the two are arranged symmetric with respect to the active layer **104**. In the following, the source electrode **1061** is taken as an example for illustration. The source electrode **1061** comprises a first-dimension metal layer (which is a metal layer arranged horizontally) and a second-dimension metal layer (which is a metal layer arranged vertically). The first-dimension metal layer and the second-dimension metal layer are arranged to connect at an intersection thereof, wherein the first-dimension metal layer is arranged on the active layer **104** and is in electrical contact engagement with the active layer **104** by means of the etch stop layer **105** and a terminal portion of the first-dimension metal layer terminates at a border of the oxidized metal area; and the second-dimension metal layer is arranged on the gate insulation layer **103** and a side surface of the second-dimension metal layer is in electrical contact engagement with an end surface of the active layer **104** by means of the etch stop layer **105**. The drain electrode **1062** has a structure that is arranged symmetric to the source electrode, and repeated description will be omitted herein.

(11) The array substrate comprises at least one passivation layer. A surface of the passivation layer will receive a pixel electrode of a display panel to dispose thereon in a subsequent process. A through hole is formed in the passivation layer, and the through hole and the drain electrode **1062** correspond, in position, to each other. The pixel electrode is extended into the through hole and is in electrical contact engagement with the metal connection layer **107** on the source electrode **1061** or the drain electrode **1062**.

(12) For example, the array substrate comprises two passivation layers, namely a first sub-passivation layer **110** and a second sub-passivation layer **111** located on the first sub-passivation layer **110**. The first sub-passivation layer **110** and the second sub-passivation layer **111** are arranged to stack on each other. The first sub-passivation layer **110** and the second sub-passivation layer **111** are formed with through holes **113** that are in alignment with each other. The pixel electrode **114** is formed on a surface of the second sub-passivation layer **111** and the pixel electrode **114** is extended

into the through holes **113** and is in electrical contact engagement with the metal connection layer **107** on the source electrode **1061** or the drain electrode **1062**.
(13) In addition, the array substrate further comprises a secondary gate electrode **115**. The secondary gate electrode **115** is arranged to align with the oxidized metal area of the active layer **104**. In a thickness direction of the array substrate, the secondary gate electrode **115** and the primary gate electrode **102** are located on two opposite sides of the active layer **104**, and the secondary gate electrode **115** is located between the first sub-passivation layer **110** and the second sub-passivation layer **111**. For example, the secondary gate electrode **115** is located on a surface of the first sub-passivation layer **110**. Alternatively, the secondary gate electrode **115** is formed in the first sub-passivation layer **110**, and a surface of the secondary gate electrode **115** is arranged flush with a surface of the first sub-passivation layer **110**. The dual-gate structure functions to enhance the stability of the oxide thin-film transistor.
(14) Further, the first sub-passivation layer **110** and the second sub-passivation layer **111** are made of different materials. For example, the first sub-passivation layer **110** is arranged closer to the active layer **104** than the second sub-passivation layer **111**, and the first sub-passivation layer **110** covers the metal connection layer **107** on the source electrode **1061** and the drain electrode **1062** and covers the oxidized metal area of the active layer **104**, and thus, the first sub-passivation layer **110** is also made of an oxide insulation material to expand electrical induction between the oxidized metal area of the active layer **104** and the secondary gate electrode **115**, while the second sub-passivation layer **111** is made of a material that is different from the first sub-passivation layer **110**. Preferably, the first sub-passivation layer **110** is made of a SiOx material, and the second sub-passivation layer **111** is made of a SiNx material.
(15) The array substrate provided in the present invention comprises a combined metal layer that includes the etch stop layer **105**, the layer in which the source electrode **1061**/drain electrode **1062** are located, and the metal connection layer **107**, and the etch stop layer **105** covers the gate insulation layer **103** and the active layer **104**, and side surfaces of the etch stop layer **105** cover terminal portions of the active layer **104**.
(16) Further, the source electrode **1061**/drain electrode **1062** located layer is disposed between the etch stop layer **105** and the metal connection layer **107**. Film thicknesses of the etch stop layer **105** and the metal connection layer **107** are identical and the film thicknesses of the etch stop layer **105** and the metal connection layer **107** are 5 nm to 10 nm. The film thickness of the source electrode **1061**/drain electrode **1062** located layer is 3 to 5 times of the film thickness if the etch stop layer **105** or the metal connection layer **107**. Preferably, the film thickness of the source electrode **1061**/drain electrode **1062** located layer refers to a total thickness of the first-dimension metal layer and the second-dimension metal layer. The source electrode **1061**/drain electrode **1062** located layer adopts a sunk arrangement and laps over one side of the active layer **104**. Portions of the source electrode **1061**/drain electrode **1062** located layer extending beyond the active layer **104** are less than the total thickness of the source electrode **1061**/drain electrode **1062** located layer, and thus, the combined metal layer does not increase an overall thickness of the display panel.
(17) For example, the etch stop layer **105** is made of a material of Ti; the metal connection layer **107** is made of any one material of Mo, MoTi, and MoNi; the source electrode **1061**/drain electrode **1062** located layer is made of a material of Cu. Further, the material that makes the etch stop layer **105** is switchable with the metal connection layer **107**.
(18) According to the array substrate provided in the present invention, the present invention also provides a manufacturing process for such an array substrate. With reference to FIGS. **2***a*-**2***g*, FIGS. **2***a*-**2***g* are schematic structural diagrams showing a flow of manufacturing the array substrate provided in the present invention.
(19) As shown in FIG. **2***a*, a base plate is provided. A primary gate electrode **102** is formed on the base plate. A gate insulation layer **103** is formed on the base plate and the primary gate electrode **102**. A patterned active layer **104** is formed on the gate insulation layer **103**. The active layer **104** is

an oxide semiconductor layer.

(20) As shown in FIG. **2***b*, a first metal layer, which is the etch stop layer **105**, is arranged on the film structure of FIG. **2***a*, such that the first metal layer covers a surface and end faces of the active layer **104** and a surface of the gate insulation layer **103**. The first metal layer completely covers the active layer **104**. A material of the first metal layer is preferably Ti, and a thickness of the first metal layer is 5 nm to 10 nm.

(21) As shown in FIG. **2***c*, a second metal layer **109**, which is the source electrode and drain electrode metal layer, is arranged on the film structure of FIG. **2***b*, such that the second metal layer **109** is arranged on a surface of the first metal layer. The second metal layer **109** is made of a material that is different from the first metal layer and has a thickness greater than the second metal layer **109**. Preferably, the second metal layer **109** is made of a material of Cu, and the thickness of the second metal layer **109** is 3-5 times of the thickness of the first metal layer.

(22) As shown in FIG. **2***d*, a third metal layer **116** is arranged on the film structure of FIG. **2***c*, such that the third metal layer **116** is arranged on a surface of the second metal layer **109**, and the third metal layer **116** is made of a material that is different from both the second metal layer **109** and the first metal layer. Preferably, the third metal layer **116** is made of any one material of Mo, MoTi, and MoNi, and a thickness of the third metal layer **116** is less than the thickness of the second metal layer **109**. The thickness of the third metal layer **116** is identical to the thickness of the first metal layer.

(23) As shown in FIG. **2***e*, on the film structure of FIG. **2***d*, patterning processing is implanted on the second metal layer **109** and the third metal layer **116**, such that photolithography being applied to etching the second metal layer **109** and the third metal layer **116** to form the source electrode **1061** and the drain electrode **1062** that are opposite to each other and the metal connection layer **107** located on the source electrode **1061** and the drain electrode **1062**, where the first metal layer serves as the etch stop layer **105** for the active layer **104** and is preserved in the operation of forming the source electrode **1061** and the drain electrode **1062**, and functions to avoid incorrect etching to the active layer **104** during photolithography. An etching region of the second metal layer **109** and the third metal layer **116** corresponds, in position, to the active layer **104**, and the source electrode **1061** and the drain electrode **1062** are connected through the first metal layer to the active layer **104**.

(24) As shown in FIG. **2***f*, on the film structure of FIG. **2***e*, O2 plasma processing is implemented on a portion of the first metal layer that is exposed in the etching region to form an oxide metal region to serve as the channel **108** of the active layer **104**. To this point, a main structure of the oxide thin-film transistor has been completed, and an ancillary structure of the oxide thin-film transistor will be formed in a subsequent process.

(25) As shown in FIG. **2***g*, on the film structure of FIG. **2***f*, a first sub-passivation layer **110** is formed, wherein the first sub-passivation layer **110** is arranged in a laying manner and filling up the etching region of the second metal layer **109** and the third metal layer **116**. A secondary gate electrode **115** is formed on the first sub-passivation layer **110**. The secondary gate electrode **115** is arranged as being in alignment, in position, with the primary gate electrode **102**, and the secondary gate electrode **115** is arranged to be in alignment, in position, with at least the channel **108** of the active layer **104**. A second sub-passivation layer **111** is arranged on the first sub-passivation layer **110**, and the second sub-passivation layer **111** and the first sub-passivation layer **110** are made of different materials. Further, the first sub-passivation layer **110** is arranged to be relatively close to the oxide metal region of the first metal layer. The first sub-passivation layer **110** adopts an oxide material, for example the first sub-passivation layer **110** being made of a SiOx material. The second sub-passivation layer **111** is made of a SiNx material. Further, the first sub-passivation layer **110** and the second sub-passivation layer **111** are formed with a through hole **113** in a location corresponding to the source electrode **1061** or the drain electrode **1062**. The through hole **113** is filled up with a metal layer, and the metal layer has an end connected to the metal connection layer

107 on the source electrode **1061** or the drain electrode **1062** and an opposite end connected to a pixel electrode **114** of a display panel to form a complete oxide thin-film transistor. In forming the through hole **113**, the metal connection layer **107** prevents, on one hand, dry etching or etching processing from affecting the source electrode **1061** or the drain electrode **1062** to ensure intactness of the source electrode **1061** and the drain electrode **1062**, and the metal connection layer **107** also functions as an ancillary connection layer for the source electrode **1061** and the drain electrode **1062**, so as to maintain stability of connecting the source electrode **1061** and the drain electrode **1062** to the pixel electrode **114**.

(26) Referring to FIG. **3**, FIG. **3** is a flow chart of manufacturing an array substrate provided in the present invention. According to the array substrate provided in the present invention, a manufacturing method for the array substrate is also provided. The method comprises the following steps: S**10**: providing a base, and forming a primary gate electrode, a gate insulation layer, and an active layer on the base; S**20**: forming a combined metal layer on the active layer, wherein the combined metal layer comprises an etch stop layer, a source-drain metal layer, and a metal connection layer that are arranged to stack on each other; S**30**: subjecting metal layers of the combined metal layer that are other than the etch stop layer to patterning processing to form a source electrode and a drain electrode located on the etch stop layer and the metal connection layer located on the source electrode and the drain electrode; S**40**: subjecting a zone of the etch stop layer that is not covered by the source electrode and the drain electrode to oxidizing processing to form an oxidized metal layer, wherein the oxidized metal layer and the active layer are arranged to correspond, in position, to each other; and S**50**: forming a passivation layer on a film layer formed in Step S**40**.

(27) According to an embodiment of the present invention, Step S**30** comprises: subjecting the metal connection layer and the source-drain metal layer to the patterning processing with wet etching to form the source electrode and the drain electrode and the metal connection layer on the source electrode and the drain electrode.

(28) As shown in FIG. **2***e*, in Step S**30**, wet etching is applied to subject the second metal layer **109** and the third metal layer **116** to etching to form the source electrode **1061** and the drain electrode **1062** that are opposite to each other and the metal connection layer **107** that is located on the source electrode **1061** and the drain electrode **1062**. The first metal layer serves as the etch stop layer **105** for the active layer **104** and is preserved during forming of the source electrode **1061** and the drain electrode **1062** and functions to prevent incorrect etching of the active layer **104** by photolithography. The etching region of the second metal layer **109** and the third metal layer **116** and the active layer **104** are arranged to correspond in position, and the source electrode **1061** and the drain electrode **1062** are connected by the first metal layer to the active layer **104**.

(29) According to an embodiment of the present invention, the etch stop layer is made of a material of Ti. In the operation of "subjecting a zone of the etch stop layer that is not covered by the source electrode and the drain electrode to oxidizing processing" of Step S**40**, O2 plasma is applied to subject the etch stop layer to oxidizing process, and the zone of the etch stop layer that is subjected to the oxidizing processing reacts and forms a TiO oxide metal layer.

(30) According to an embodiment of the present invention, Step S**50** comprises: S**501**: forming a first sub-passivation layer on a film layer formed in Step S**40**; S**502**: forming a secondary gate electrode on the first sub-passivation layer, wherein the secondary gate electrode and the oxidized metal layer are arranged to correspond, in position, to each other; and S**503**: forming a second sub-passivation layer on the first sub-passivation layer, wherein the second sub-passivation layer covers the secondary gate electrode.

(31) According to an embodiment of the present invention, Step S**50** further comprises: S**504** in which through holes are formed in the first sub-passivation layer and the second sub-passivation layer to be in communication with each other, wherein the through holes correspond, in position, to the metal connection layer on the source electrode or the metal connection layer on the drain

electrode.
(32) As shown in FIGS. **2***b*-**2***d*, in Step S**20**, the combined metal layer comprises the first metal layer, the second metal layer **109**, and the third metal layer **116** that are stacked on each other. The first metal layer serves as the etch stop layer **105**. The first metal layer covers a surface and end faces of the active layer **104** and a surface of the gate insulation layer **103**. The first metal layer completely covers the active layer **104**. A material of the first metal layer is preferably Ti, and a thickness of the first metal layer is 5 nm to 10 nm.
(33) The second metal layer **109** is a metal layer that is subjected to etching to form the source electrode and the drain electrode. The second metal layer **109** is arranged on a surface of the first metal layer. The second metal layer **109** is made of a material different from the first metal layer and has a thickness greater than the second metal layer **109**. Preferably, the second metal layer **109** is made of a Cu material, and the thickness of the second metal layer **109** is 3 to 5 times of the thickness of the first metal layer.
(34) The third metal layer **116** serves as the metal connection layer. The third metal layer **116** is arranged on a surface of the second metal layer **109**. A material of the third metal layer **116** is different from both the second metal layer **109** and the first metal layer. Preferably, the third metal layer **116** is made of any one material of Mo, MoTi, and MoNi, and a thickness of the third metal layer **116** is far smaller than the thickness of the second metal layer **109**. The thickness of the third metal layer **116** is identical to the thickness of the first metal layer.
(35) Compared to the prior art, an embodiment of the present invention provides an array substrate, and a metal film layer is formed on an active layer of the array substrate, such that the metal film layer protects the active layer from being damaged by an etchant liquid or dry etching process during subsequent patterning processing of source/drain electrodes, and afterwards, a portion of the metal film layer that corresponds to a channel of the active layer the channel is subjected to oxidizing processing to form an oxide layer to help keep the functional property of the active layer. In the entire manufacturing process of the array substrate, the active layer will not be subject to damage in subsequent processing and stability of the device can be maintained.
(36) In summary, although the application is disclosed above by means of the preferred embodiments, such preferred embodiments that are described above are not intended to limit the application. Those having ordinary skill in the art may contemplate various alternations and modifications without departing from the sprits and scope of the application, and thus, the scope of protection that the applicant seeks for is based on the scope defined by the claims.

Claims

1. An array substrate, comprising: a base; a primary gate electrode located on the base; an active layer located on the primary gate electrode; an etch stop layer located on the active layer; a source electrode and a drain electrode located on the etch stop layer, and a metal connection layer arranged on surfaces of the source electrode and the drain electrode away from the base, wherein the drain electrode is connected to a pixel through the metal connection layer; wherein the source electrode and the drain electrode partly cover the etch stop layer, an area of the etch stop layer not covered by the source electrode and the drain electrode is configured to be an oxidized metal layer, and the oxidized metal layer corresponds to the active layer and the primary gate electrode; wherein a thickness of a portion of the source electrode extending beyond the active layer is less than a total thickness of the source electrode, and a thickness of a portion of the drain electrode extending beyond the active layer is less than a total thickness of the drain electrode.
2. The array substrate according to claim 1, wherein a material of the metal connection layer comprises any one of Mo, MoTi, and MoNi.
3. The array substrate according to claim 1, further comprising a passivation layer arranged on the base, wherein the passivation layer at least covers the oxidized metal layer and the metal

connection layer located on the source electrode and the drain electrode; and the passivation layer is formed with a through hole, and the through hole corresponds to the metal connection layer located on the drain electrode.

4. The array substrate according to claim 3, wherein the passivation layer comprises a first sub-passivation layer and a second sub-passivation layer arranged to stack on each other, the first sub-passivation layer is partly in contact with the oxidized metal layer, and a material of the first sub-passivation layer comprises silicon oxide.

5. The array substrate according to claim 4, wherein an oxide thin-film transistor further comprises a secondary gate electrode, and the secondary gate electrode is located above the oxidized metal layer and corresponding to the oxidized metal layer; and wherein the secondary gate electrode is arranged between the first sub-passivation layer and the second sub-passivation layer.

6. The array substrate according to claim 1, wherein a material of the etch stop layer comprises Ti, and a film thickness of the etch stop layer ranges from 5 nm to 10 nm.

7. The array substrate according to claim 1, wherein a film thickness of a layer the source electrode and the drain electrode are located ranges from 3 to 5 times of a film thickness of the etch stop layer or the metal connection layer.