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Power control method and device of lower radio frequency power supply and semiconductor processing equipment

Abstract

A power control method of a lower RF power supply of semiconductor processing equipment includes, when a processing chamber starts semiconductor processing, with a predetermined power compensation equation and according to a pre-obtained first RF circuit parameter set of a reference chamber and a second RF circuit parameter set of a present processing chamber performing the semiconductor processing, obtaining a power compensation coefficient of the present processing chamber relative to the reference chamber, according to the power compensation coefficient and a power setting value of the lower RF power supply of the present processing chamber, calculating a power compensation value of the present processing chamber relative to the reference chamber, and controlling the lower RF power supply to output the power compensation value.

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Background/Summary

CROSS-REFERENCES TO RELATED APPLICATIONS (1) This application is a continuation application of International Application No. PCT/CN2022/120101, filed on Sep. 21, 2022, which claims priority to Chinese Application No. 202111126996.7 filed on Sep. 26, 2021, the entire contents of all of which are incorporated herein by reference.

TECHNICAL FIELD

(1) The present disclosure generally relates to the semiconductor manufacturing field and, more particularly, to a power control method and a power control device for a lower radio frequency power supply in semiconductor processing equipment, and the semiconductor processing equipment.

BACKGROUND

(2) As the feature size of integrated circuits continues to decrease, the requirements for processing technology become increasingly strict. One important requirement is product consistency. During the processing process, strict requirements are placed on the consistency of the process results for all chambers in the semiconductor processing equipment of the same model to avoid process risks caused by consistency issues of the chambers. Therefore, strict process control is needed among different chambers to implement consistency in process results.

(3) Taking inductively coupled plasma equipment as an example, the lower RF power supply loads the RF energy to the

lower electrode (e.g., electrostatic chuck) through a matcher. Thus, an RF bias voltage is generated on the wafer surface to accelerate the etching of the ions on the wafer. When the RF power output by the lower RF power supply to the RF power changes, the bias voltage generated at the wafer can change, and the final etching processing result can change too. Thus, the consistency of the overall efficiency of the lower electrode RF circuit can be closely related to the processing result.

(4) The power loss generated in the process from outputting the RF power by the lower electrode power supply until the RF power is adopted by the plasma includes matcher loss, loss of the lower electrode for the ground capacity, and circuit contact loss. Among different chambers, since the matchers, lower electrode, and mounting contact resistance can be different in the lower RF circuit, the equivalent resistance and capacity of various parts of the lower electrode RF circuit can be different. That is, the power loss can be different. Thus, among different chambers, when the output powers of the lower electrode power supplies are the same, the power losses can be different. The power adopted by plasma can be different too. Thus, the generated RF bias voltages can be different, which affects the consistency of the processing result.

SUMMARY

(5) As a first aspect, the present disclosure provides a power control method of a lower RF power supply of semiconductor processing equipment. The method includes, when a processing chamber starts semiconductor processing, with a predetermined power compensation equation and according to a pre-obtained first RF circuit parameter set of a reference chamber and a second RF circuit parameter set of a present processing chamber performing the semiconductor processing, obtaining a power compensation coefficient of the present processing chamber relative to the reference chamber, according to the power compensation coefficient and a power setting value of the lower RF power supply of the present processing chamber, calculating a power compensation value of the present processing chamber relative to the reference chamber, and controlling the lower RF power supply to output the power compensation value.

(6) As a second aspect, the present disclosure further provides a processing chamber, a matcher, a lower RF power supply, and a power control device. A lower electrode is arranged in the processing chamber. The lower electrode is electrically connected to the lower RF power supply through the matcher. The power control device includes a calculator and a controller. The calculator is configured to, when a processing chamber starts semiconductor processing, with a predetermined power compensation equation and according to a pre-obtained first RF circuit parameter set of a reference chamber and a second RF circuit parameter set of a present processing chamber performing the semiconductor processing, obtain a power compensation coefficient of the present processing chamber relative to the reference chamber, and according to the power compensation coefficient and a power setting value of the lower RF power supply of the present processing chamber, calculate a power compensation value of the present processing chamber relative to the reference chamber. The controller is configured to control the lower RF power supply to output the power compensation value.

(7) The present disclosure has the following beneficial effects.

(8) In the technical solution of the power control method and device of the lower RF power supply in the semiconductor processing equipment of embodiments of the present disclosure, when the processing chamber starts the semiconductor processing, with the pre-determined power compensation equation and according to the pre-obtained first RF circuit parameter set and the second RF circuit parameter set of the present processing chamber performing the semiconductor processing, the power compensation coefficient can be obtained. According to the power compensation coefficient and the power setting value of the lower RF power supply of the present processing chamber, the power compensation value can be calculated. Then, the lower RF power supply can be controlled to output the power compensation value. Thus, the difference in the power utilized by the plasma between the other processing chambers except for the reference chamber and the reference chamber can be compensated. Thus, the consistency in the bias voltage values generated on the wafers between different chambers under the same processing recipe can be improved. Thus, the processing result consistency of the different processing chambers can be improved.

(9) The semiconductor processing equipment of the present disclosure, by adopting the power control device of the present disclosure, can improve the consistency of the bias voltage value generated on the wafer among different chambers under the same processing recipe to improve the consistency of processing results among different process chambers.

Description

BRIEF DESCRIPTION OF THE DRAWINGS

(1) FIG. **1** illustrates a schematic structural diagram of an inductively coupled plasma equipment.

(2) FIG. **2**A illustrates a schematic diagram showing radio frequency (RF) power loss in a lower electrode RF circuit in FIG. **1**.

(3) FIG. **2**B illustrates an equivalent circuit diagram of the lower electrode RF circuit in FIG. **1**.

(4) FIG. **3** illustrates a schematic block diagram of a power control method of a lower RF power supply in semiconductor processing equipment according to embodiments of the present disclosure.

(5) FIG. **4**A illustrates a schematic structural diagram of semiconductor processing equipment according to embodiments of the present disclosure.
(6) FIG. **4**B illustrates a schematic equivalent circuit diagram of the lower electrode RF circuit in FIG. **4**A when outputting a determined power.
(7) FIG. **5**A illustrates a schematic equivalent diagram of the lower electrode RF circuit in FIG. **4**A when performing process step Step1.
(8) FIG. **5**B illustrates a schematic equivalent diagram of the lower electrode RF circuit in FIG. **4**A when performing process step Step2.
(9) FIG. **6** illustrates schematic equivalent diagrams of lower electrode RF circuits in different processing chambers according to embodiments of the present disclosure.
(10) FIG. **7** illustrates a schematic diagram showing power compensation coefficients corresponding to different processing steps according to embodiments of the present disclosure.
(11) FIG. **8** illustrates a schematic block diagram of a power control method of a lower electrode RF power supply in the semiconductor processing equipment according to some embodiments of the present disclosure.
(12) FIG. **9** illustrates a schematic block diagram showing a principle of a power control device of the lower electrode RF power supply in the semiconductor processing equipment according to some embodiments of the present disclosure.
(13) FIG. **10** illustrates a schematic block diagram showing another principle of a power control device of the lower electrode RF power supply in the semiconductor processing equipment according to some embodiments of the present disclosure.

DETAILED DESCRIPTION OF THE EMBODIMENTS

(14) To help those skilled in the art better understand the technical solution of the present disclosure, a power control method and a power control device of lower radio frequency (RF) power supply in semiconductor processing equipment and the semiconductor processing equipment are described in detail below in conjunction with the accompanying drawings.
(15) FIG. **1** illustrates a schematic structural diagram of an inductively coupled plasma equipment. As shown in FIG. **1**, the equipment includes a processing chamber **11**. A dielectric window **6** is arranged at the top of the processing chamber. An inductive coupling coil **5** is arranged above the dielectric window **6**. The inductive coupling coil **5** is electrically connected to an upper RF power supply **1** via an upper matcher **2**. The upper RF power supply **1** can apply RF power onto the inductive coupling coil **5** via the upper matcher **2** to excite a process gas in the processing chamber **11** to form a plasma **9**. Additionally, a lower electrode **8** (e.g., an electrostatic chuck) is arranged in processing chamber **11** and is configured to carry a wafer **7**. The lower electrode **8** is electrically connected to a lower RF power supply **4** via a lower matcher **3**. The lower RF power supply **4** is configured to apply RF power onto the lower electrode **8** to generate an RF bias voltage on the wafer surface to accelerate ions to etch the wafer **7**.
(16) When the RF power of the lower RF power supply **4** is applied to the electrostatic chuck **8**, a corresponding RF bias voltage is formed on the wafer **7**. The RF bias voltage can be used to accelerate the ions to perform an etching process. When the applied RF power is different, the magnitude of the bias voltage on the wafer **7** can be changed, and the final etching process result can be changed. Thus, the overall efficiency consistency of the lower electrode circuit can be closely related to the process results.
(17) FIG. **2**A illustrates a schematic diagram showing radio frequency (RF) power loss in a lower electrode RF circuit in FIG. **1**. As shown in FIG. **2**A, the power loss during the process from the RF power output from the lower RF power supply **4** to the power utilized by the plasma **9** mainly includes losses in the matcher, losses in the lower electrode to ground capacitance, losses in circuit contact, etc. In some embodiments, if the output power of the lower RF power supply **4** is P.sub.in, the total power loss of the lower electrode RF circuit can be P.sub.0, and the remaining power utilized by the plasma **9** can be P.sub.p, P.sub.p=P.sub.in−P.sub.0. Then, the power transmission efficiency of the lower electrode RF circuit can be η, η=P.sub.p/P.sub.in.
(18) FIG. **2**B illustrates an equivalent circuit diagram of the lower electrode RF circuit in FIG. **1**. As shown in FIG. **2**B, capacitor C**1** and capacitor C**2** are variable capacitors in lower matcher **3**. A loss resistance of the lower matcher **3** and a contact resistance of the lower electrode RF circuit as a whole can be considered as a loss equivalent resistance R.sub.m of the lower electrode RF circuit. The loss equivalent resistance R.sub.m is connected in series in the main path of the lower electrode RF circuit. Moreover, an equivalent circuit connected to an output end of the main path can include two parallel branches. One of the branches can be a lower electrode-to-ground branch. The lower electrode-to-ground branch can include a lower electrode-to-ground capacitance C and an equivalent resistance R.sub.g when the lower electrode is grounded. The other branch can be a plasma sheath branch. The plasma sheath branch can include an impedance real part R.sub.p and an equivalent inductance L.sub.p of an impedance imaginary part of the plasma **9**, and an impedance real part R.sub.s and an equivalent capacitance C.sub.s of an impedance imaginary part of the plasma sheath. Additionally, the current in the lower electrode-to-ground branch can be I.sub.c, the current in the plasma sheath branch can be I.sub.s, and the current at the output end of the lower matcher **3** in the main path of the lower electrode RF circuit can be I. The current I can be equal to the sum of the currents I.sub.c and I.sub.s.
(19) Since among different chambers, the matcher in the lower electrode RF circuit, the lower electrode, the installation contact resistance, etc., are different, the equivalent resistance and capacitance of the parts of the lower electrode RF

circuit can be different among different chambers. That is, the total power loss P.sub.0 in the lower electrode RF circuit can be different. Thus, among different chambers, when the output power P.sub.in of the lower RF power supply is the same, and the total power loss P.sub.0 is different, the remaining power P.sub.p utilized by the plasma **9** (the power transmission efficiency η) can be different. Then, the RF bias voltage generated on the wafer surface can be different, which affects the consistency of the processing results.

(20) To address the above problem, FIG. **3** illustrates a schematic block diagram of a power control method of a lower RF power supply in semiconductor processing equipment according to embodiments of the present disclosure. The method includes the following steps.

(21) At **101**, when semiconductor processing begins in the processing chamber, with predetermined power compensation equation, and according to a pre-obtained first RF circuit parameter set of a reference chamber and a second RF circuit parameter set of a present processing chamber in which the semiconductor process is performed, a power compensation coefficient of the present processing chamber is obtained relative to the reference chamber.

(22) The reference chamber above can be one chamber specified from a plurality of chambers with the same structure. The first RF circuit parameter set of the reference chamber can refer to a combination of feature parameters of the lower electrode of the reference chamber. This first RF circuit parameter set can include but is not limited to the current at the output end of the lower matcher **3** in the main path of the lower electrode RF circuit, the current in the plasma sheath branch of the lower electrode RF circuit, the loss equivalent resistance and the ground equivalent resistance of the lower electrode RF circuit, and the lower electrode-to-ground capacitance.

(23) The present processing chamber above can be other processing chambers with the same structure except the reference chamber. When processing is performed in other process chambers, compensation can be performed on the output power of the lower RF power supply **4** according to the inherent parameter of the processing chambers (i.e., the second RF circuit parameter set) and in connection with the inherent parameter and the plasma sheath parameter of the reference chamber (i.e., the first RF circuit parameter set) to achieve that the RF bias voltage generated on the wafer surface when the processing is performed in the other processing chambers with the same structure is consistent with the reference chamber. The second RF circuit parameter set of the present processing chamber can include but is not limited to the loss equivalent resistance and the grounded equivalent resistance of the lower RF circuit and the lower electrode-to-ground capacitance.

(24) It should be noted that whether for the reference chamber or other process chambers, the inherent parameters such as the loss equivalent resistance R.sub.m, the grounded equivalent resistance R.sub.g, and the lower electrode-to-ground capacitance C can remain unchanged when performing the processing. The plasma sheath parameter of the lower electrode RF circuit (e.g., the RF bias voltage and the current in the plasma sheath branch) can change with different processing processes. The current I.sub.c in the lower electrode-to-ground branch is made of most of the current I (usually greater than 10 amperes). However, the current I.sub.s in the plasma sheath branch can be small (smaller than 1 ampere). Thus, the current I.sub.s in the plasma sheath branch can be regarded as a constant current. Since the remaining power P.sub.p utilized by the plasma **9** (also referred to as absorption power) is a product of the RF bias voltage and the current I.sub.s in the plasma sheath branch, the remaining power P.sub.p can also change with the processing. Based on this, the lower electrode loss feature of different chambers can be reflected by the inherent parameters and the plasma sheath parameters. The difference in the remaining power P.sub.p between the other processing chambers and the reference chamber can be compensated according to the lower electrode loss feature to allow different chambers to have the same remaining power P.sub.p. Thus, the RF bias voltages of different chambers can be ensured to be consistent, and the processing results can be consistent.

(25) In some optional embodiments, as shown in FIG. **4**A, based on the inductively coupled plasma equipment shown in FIG. **1**, a current detection unit **24** is further arranged in the circuit between the output end of the lower matcher **3** and the lower electrode **8** and is configured to detect the current I at the output end of the lower matcher **3** in the main path of the lower electrode RF circuit. Additionally, voltage detection unit **23** is connected to the lower electrode **8** and is configured to detect the RF bias voltage on the wafer surface. Furthermore, a capacitance detection unit (not shown in the figure) can be connected to the lower electrode-to-ground branch and be configured to detect the lower electrode-to-ground capacitance C.

(26) Taking the inductively coupled plasma equipment shown in FIG. **4**A as an example, as shown in FIG. **4**B, corresponding to each processing chamber (including the reference chamber and other processing chambers), the following acquisition method can be used to obtain the loss equivalent resistance R.sub.m and the grounded equivalent resistance R.sub.g.

(27) At **201**, the lower RF power supply **4** of the processing chamber (the upper RF power supply **1** is turned off) is turned on to apply a power setting value Plow on the lower electrode **8** via the lower matcher **3**.

(28) The power setting value P.sub.low can be lower than the power value normally used in the processing. When the power setting value P.sub.low is applied onto the lower electrode **8**, the determined power P.sub.low can be almost fully consumed by the lower electrode-to-ground branch when the lower matcher **3** performs matching. Since the upper RF power supply **1** is turned off, and the power setting value P.sub.low is low, the power may not be sufficient to cause the plasma in the processing chamber to ignite. Thus, no plasma load can be generated.

(29) At **202**, the current at the output end of the matcher (i.e., the lower matcher **3**) in the main path of the lower

electrode RF circuit, the present bias voltage value of the lower electrode **8**, and the lower electrode-to-ground capacitance are detected.

(30) In step **202**, the current detection unit **24** can be configured to detect the current I.sub.0 at the output end of the matcher in the main path of the lower electrode RF circuit. The voltage detection unit **23** can be configured to detect the present bias voltage value V.sub.0 of the lower electrode **8**, and the capacitance detection unit can be configured to detect the lower electrode-to-ground capacitance C.

(31) In some embodiments, the equation (1) of the power setting value P.sub.low is:

(32) $$P_{low} = I_0^2(R_m + R_g) \quad (1)$$

(33) The equation (2) of the present bias voltage value V.sub.0 of the lower electrode **8** is:

(34) $$V_0 = I_0\sqrt{R_g^2 + (\frac{1}{C})^2} \quad (2)$$

(35) The following equations (3) and (4) are derived using the above equations (1) and (2).

(36) $$R_g = \sqrt{(\frac{V_0}{I_0})^2 - (\frac{1}{C})^2} \quad (3) \quad R_m = \frac{P_{low}}{I_0^2} - R_g \quad (4)$$

where, R.sub.g denotes the grounded equivalent resistance of the lower electrode RF circuit, R.sub.m denotes the loss equivalent resistance of the lower electrode RF circuit, V.sub.0 denotes the present bias voltage value, I.sub.0 denotes the present current, ω denotes an angular frequency, C denotes the lower electrode-to-ground capacitance, and P.sub.low denotes the power setting value.

(37) At **203**, using the above equations (3) and (4), and according to the present current I.sub.0, the present bias voltage value V.sub.0, and lower electrode-to-ground capacitance C, the loss equivalent resistance R.sub.m and the grounded equivalent resistance R.sub.g of the lower electrode RF circuit are calculated.

(38) Of course, in practical applications, the loss equivalent resistance R.sub.m and the grounded equivalent resistance R.sub.g of the lower electrode RF circuit can also be obtained in any other methods, which are not limited in the present disclosure.

(39) Taking the inductively coupled plasma equipment shown in FIG. **4**A as an example of performing semiconductor processing **1**, as shown in FIG. **5**A, the equation (5) of the bias voltage value V.sub.1 of the lower electrode **8** is:

(40) $$V_1 = I_{c1}\sqrt{R_g^2 + (\frac{1}{C})^2} \quad (5)$$

where, I.sub.c1 is the current in the lower electrode-to-ground branch corresponding to semiconductor processing **1**.

(41) The equation (6) of the current I.sub.1 at the output end of the matcher in the main path of the lower electrode RF circuit corresponding to semiconductor processing **1** is:

(42) $$I_1 = I_{c1} + I_{s1} \quad (6)$$

(43) The above bias voltage value V.sub.1 and current I.sub.1 can be detected and obtained by the voltage detection unit **23** and the current detection unit **24**, respectively. The grounded equivalent resistance R.sub.g can be calculated through the equation (3). Therefore, the equation (7) of the current I.sub.s1 in the plasma sheath branch corresponding to semiconductor processing **1** is:

(44) $$I_{s1} = I_1 - \frac{V_1}{\sqrt{R_g^2 + (\frac{1}{C})^2}} \quad (7)$$

(45) For example, semiconductor processing **2** is performed by the inductively coupled plasma equipment shown in FIG. **4**A, as shown in FIG. **5**B, the equation (8) of the bias voltage value V.sub.2 of the lower electrode **8** is:

(46) $$V_2 = I_{c2}\sqrt{R_g^2 + (\frac{1}{C})^2} \quad (8)$$

where, I.sub.c2 is the current in the lower electrode-to-ground branch corresponding to semiconductor processing **2**.

(47) The equation (9) of the current I.sub.2 at the output end of the matcher in the main path of the lower electrode RF circuit corresponding to semiconductor processing **2** is:

(48) $$I_2 = I_{c2} + I_{s2} \quad (9)$$

(49) The above bias voltage value V.sub.2 and current I.sub.2 can be detected by the voltage detection unit **23** and the current detection unit **24**, respectively. The grounded equivalent resistance R.sub.g can be calculated through the equation (3) as above. Therefore, the equation (10) of the current I.sub.s2 in the plasma sheath branch corresponding to semiconductor processing **2** is:

(50) $$I_{s2} = I_2 - \frac{V_2}{\sqrt{R_g^2 + (\frac{1}{C})^2}} \quad (10)$$

(51) From the above, the equation for the current I.sub.s in the plasma sheath branch can be applied regardless of whether semiconductor processing **1**, semiconductor processing **2**, or any other different processing.

(52) Taking three process chambers (A, B, C) as an example, as shown in FIG. **6**, firstly, step **201** to step **203** can be used to obtain the loss equivalent resistance R.sub.mA and grounded equivalent resistance R.sub.gA for processing chamber A, the loss equivalent resistance R.sub.mB and ground equivalent resistance R.sub.gB for processing chamber B, the loss equivalent resistance R.sub.mC and grounded equivalent resistance Rec for processing chamber C. Additionally, the capacitance detection unit of processing chamber A can be configured to obtain the lower electrode-to-ground capacitance C.sub.A. The capacitance detection unit of processing chamber B can be configured to obtain the

lower electrode-to-ground capacitance C.sub.B. The capacitance detection unit of processing chamber C can be configured to obtain the lower electrode-to-ground capacitance C.sub.C.

(53) Since the loss equivalent resistances R.sub.m, the grounded equivalent resistances Rg, and the lower electrode-to-ground capacitances C corresponding to different chambers are different, the bias voltage values corresponding to different chambers can be different. That is, for example, semiconductor processing **1** is performed, V.sub.A1≠V.sub.B1≠V.sub.C1. Based on this, when the power setting value of the lower electrode power supply **4** of the three processing chambers (A, B, and C) is P.sub.in, remaining power P.sub.pA, remaining power P.sub.pB, and remaining power P.sub.pC utilized by the plasma **9** corresponding to the three processing chambers (A, B, and C) can have the following equations.

(54) 0 $P_{\mathrm{pA}} = V_{A1} I_{s1} = {}_{A1} P_{\mathrm{in}}$ (11) $P_{\mathrm{pB}} = V_{B1} I_{s1} = {}_{B1} P_{\mathrm{in}}$ (12) $P_{\mathrm{pC}} = V_{C1} I_{s1} = {}_{C1} P_{\mathrm{in}}$ (13)

where, η.sub.A1, η.sub.B1, and η.sub.C1 are power transmission efficiencies for the three processing chambers (A, B, and C) respectively. I.sub.s1 can be the current in the plasma sheath branch corresponding to semiconductor processing **1**.

(55) If processing chamber A is selected as the reference chamber, the equation (7) can be used to calculate the current I.sub.s1 for processing chamber A. The currents in the plasma sheath branches corresponding to semiconductor processing **1** for the other two processing chambers (B and C) can be set to be equal to I.sub.s1.

(56) When semiconductor processing **1** is performed in processing chamber B, the power compensation coefficient of processing chamber B can be set to β.sub.B1. If the remaining power P.sub.pB utilized by the plasma **9** corresponding to processing chamber B is equal to the remaining power P.sub.pC utilized by the plasma **9** corresponding to processing chamber C, the following equation exists.

(57) ${}_{B1}({}_{B1} P_{\mathrm{in}}) = V_{B1} I_{s1} \quad {}_{B1} = V_{A1} I_{s1} = {}_{A1} P_{\mathrm{in}}$ (14)

(58) According to the equation (14) above, the equation for the power compensation coefficient β.sub.B1 for processing chamber B is derived as:

(59) $${}_{B1} = \frac{V_{A1} I_{s1}}{V_{B1} I_{s1}}$$ (15)

(60) Assuming that an RF frequency applied to the lower electrode **8** is f, an impedance corresponding to the ground capacitance C.sub.A of processing chamber A is X, and

(61) $X = \frac{1}{C_A}$,

where ω=2πf, an impedance corresponding to the ground capacitance C.sub.B of processing chamber B is Y, and

(62) $Y = \frac{1}{C_B}$,

where ω=2πf. Based on this, the bias voltage values corresponding to processing chamber A and processing chamber B under the same power setting value P.sub.in, respectively, are:

(63) $V_{A1} = I_{\mathrm{cA1}} \sqrt{R_{\mathrm{gA}}^2 + (\frac{1}{C_A})^2} = I_{\mathrm{cA1}} \sqrt{R_{\mathrm{gA}}^2 + X^2}$ (16) $V_{B1} = I_{\mathrm{cB1}} \sqrt{R_{\mathrm{gB}}^2 + (\frac{1}{C_B})^2} = I_{\mathrm{cB1}} \sqrt{R_{\mathrm{gB}}^2 + Y^2}$ (17)

(64) Moreover, the currents at output ends of the matchers in the main paths of the lower RF circuits corresponding to processing chamber A and processing chamber B with the same power setting value P.sub.in, respectively, are:

(65) $I_{A1} = I_{\mathrm{cA1}} + I_{s1}$ (18) $I_{B1} = I_{\mathrm{cB1}} + I_{s1}$ (19)

(66) Then, the power setting value P.sub.in is:

(67) $P_{\mathrm{in}} = I_{A1}^2 R_{\mathrm{mA}} + I_{\mathrm{cA1}}^2 R_{\mathrm{gA}} + V_{A1} I_{s1} = I_{B1}^2 R_{\mathrm{mB}} + I_{\mathrm{cB1}}^2 R_{\mathrm{gB}} + V_{B1} I_{s1}$ (20)

(68) According to the above equations (16) to (20), the current I.sub.cB1 in the lower electrode-to-ground branch corresponding to processing chamber B is derived as:

(69) $$I_{\mathrm{cB1}} = \frac{-I_{s1}(2R_{\mathrm{mB}} + Y) + \sqrt{I_{s1}^2 (2R_{\mathrm{mB}} + Y)^2 - 4(R_{\mathrm{mB}} + R_{\mathrm{gB}})[I_{s1}^2 (R_{\mathrm{mB}} - R_{\mathrm{mA}}) - I_{\mathrm{cA1}}^2 (R_{\mathrm{mA}} + R_{\mathrm{gA}}) - 2I_{s1} I_{\mathrm{CA1}} R_{\mathrm{mA}} - I_{s1} I_{\mathrm{CA1}} X]}}{2(R_{\mathrm{mB}} + R_{\mathrm{gB}})}$$ (21)

(70) Using processing chamber A as the reference chamber, and substituting the above equation (21) into the equation (15), the power compensation equation for processing chamber B corresponding to semiconductor processing **1** is derived as:

(71)

$${}_{B1} = \frac{V_{A1} I_{s1}}{V_{B1} I_{s1}} = \frac{I_{\mathrm{CA1}} \mathrm{XI}_{s1}}{I_{\mathrm{CB1}} \mathrm{YI}_{s1}} = \frac{2(R_{\mathrm{mB}} + R_{\mathrm{gB}})(I_{A1} - I_{s1})X}{[-I_{s1}(2R_{\mathrm{mB}} + Y)]Y + Y\sqrt{I_{s1}^2 (2R_{\mathrm{mB}} + Y)^2 - 4(R_{\mathrm{mB}} + R_{\mathrm{gB}})[I_{s1}^2 (R_{\mathrm{mB}} - R_{\mathrm{mA}}) - (I_{A1} - I_{s1})^2 (R_{\mathrm{mA}} + R_{\mathrm{gA}}) - (2I_{s1} R_{\mathrm{mA}} + X)(I_{A1} - I_{s1})]}}$$ (22)

(72) Where, β.sub.B1 is the power compensation coefficient for processing chamber B corresponding to semiconductor processing **1** relative to processing chamber A.

(73) The first RF circuit parameter set of processing chamber A can include I.sub.A, I.sub.S, R.sub.mA, R.sub.gA, and X. I.sub.A1 is the current at the output end of the matcher in the main path of the lower electrode RF circuit corresponding to semiconductor processing **1**. I.sub.s1 is the current in the plasma sheath circuit branch of the lower electrode RF circuit corresponding to semiconductor processing **1**. R.sub.mA is the loss equivalent resistance of the lower electrode RF circuit of processing chamber A. R.sub.gA is the grounded equivalent resistance of the lower electrode RF circuit of processing chamber A. X is the impedance value corresponding to the lower electrode-to-ground capacitance of processing chamber A, and

(74) $0X = \frac{1}{C_A}$,
where ω is the angular frequency. C.sub.A is the lower electrode-to-ground capacitance of processing chamber A.
(75) The second RF circuit parameter set of processing chamber B can include R.sub.mB, R.sub.gB, and Y. R.sub.mB is the loss equivalent resistance of the lower electrode RF circuit of processing chamber B. R.sub.gB is the grounded equivalent resistance of the lower electrode RF circuit of processing chamber B. Y is the impedance value corresponding to the lower electrode-to-ground capacitance of processing chamber B, and
(76) $Y = \frac{1}{C_B}$,
where ω is the angular frequency. C.sub.B is the lower electrode-to-ground capacitance of processing chamber B.
(77) Similarly, using processing chamber A as the reference chamber, the power compensation equation for processing chamber C corresponding to semiconductor processing **1** is derived as:
(78)

$$C1 = \frac{V_{A1}I_{s1}}{V_{C1}I_{s1}} = \frac{I_{CA1}\mathrm{XI}_{s1}}{I_{CC1}\mathrm{ZI}_{s1}} = \frac{2(R_{mC}+R_{gC})(I_{A1}-I_{s1})X}{[-I_{s1}(2R_{mC}+Z)]Z+Z\sqrt{I_{s1}^2(2R_{mC}+Z)^2-4(R_{mC}+R_{gC})[I_{s1}^2(R_{mC}-R_{mA})-(I_{A1}-I_{s1})^2(R_{mA}+R_{gA})-(2I_{s1}R_{mA}+X)(I_{A1}-I_{s1})]}} \quad (23)$$

(79) Where β.sub.C1 is the power compensation coefficient for processing chamber C corresponding to semiconductor processing **1** relative to processing chamber A.
(80) The second RF circuit parameter set of processing chamber C can include R.sub.mC, R.sub.gC, and Z. R.sub.mC is the loss equivalent resistance of the lower electrode RF circuit of processing chamber C. R.sub.gC is the grounded equivalent resistance of the lower electrode RF circuit of processing chamber C. Z is the impedance value corresponding to the lower electrode-to-ground capacitance of processing chamber C, and
(81) $Z = \frac{1}{C_C}$,
where ω is the angular frequency. C.sub.C is the lower electrode-to-ground capacitance of processing chamber C.
(82) Similarly, using processing chamber A as the reference chamber, the power compensation equations for processing chamber B and processing chamber C corresponding to semiconductor processing **2** are derived as:
(83)

$$B2 = \frac{V_{A2}I_{s2}}{V_{B2}I_{s2}} = \frac{I_{CA2}\mathrm{XI}_{s2}}{I_{CB2}\mathrm{YI}_{s2}} = \frac{2(R_{mB}+R_{gB})(I_{A2}-I_{s2})X}{[-I_{s2}(2R_{mB}+Y)]Y+Y\sqrt{I_{s2}^2(2R_{mB}+Y)^2-4(R_{mB}+R_{gB})[I_{s2}^2(R_{mB}-R_{mA})-(I_{A2}-I_{s2})^2(R_{mA}+R_{gA})-(2I_{s2}R_{mA}+X)(I_{A2}-I_{s2})]}} \quad (24)$$

$$C2 = \frac{V_{A2}I_{s2}}{V_{C2}I_{s2}} = \frac{I_{CA2}\mathrm{XI}_{s2}}{I_{CC2}\mathrm{ZI}_{s2}} = \frac{2(R_{mC}+R_{gC})(I_{A2}-I_{s2})X}{[-I_{s2}(2R_{mC}+Z)]Z+Z\sqrt{I_{s2}^2(2R_{mC}+Z)^2-4(R_{mC}+R_{gC})[I_{s2}^2(R_{mC}-R_{mA})-(I_{A2}-I_{s2})^2(R_{mA}+R_{gA})-(2I_{s2}R_{mA}+X)(I_{A2}-I_{s2})]}} \quad (25)$$

(84) It should be noted that the semiconductor processing **1** and semiconductor processing **2** above can include two different processing recipes or two different processing steps within the same semiconductor processing.
(85) In some optional embodiments, the semiconductor processing can include a plurality of processing steps. For different processing steps, the current I.sub.s1 in the plasma sheath branch of the lower RF circuit can be different. Thus, taking processing chamber A as the reference chamber as an example, the power control method of embodiments of the present disclosure further includes the following steps.
(86) At **301**, before performing the semiconductor processing, pre-obtained I.sub.A (the current at the output end of the lower matcher **3** in the main path of the lower RF circuit) and I.sub.S (the current in the plasma sheath branch) corresponding to the processing steps are written in a parameter table. For example, the processing steps include N steps, and N is an integer greater than 1.
(87) The I.sub.A and I.sub.S corresponding to the processing steps can be calculated using the equation (7) above.
(88) Table 1 shows the parameter table of I.sub.A and I.sub.S of processing chamber A (i.e., the reference chamber) corresponding to the N processing steps.
(89) TABLE-US-00001 Step I.sub.s I.sub.A 1 I.sub.s1 I.sub.A1 2 I.sub.s2 I.sub.A2 . . . . . N I.sub.sN I.sub.AN
(90) At **302**, the pre-obtained R.sub.mA, R.sub.gA, and C.sub.A corresponding to processing chamber A and R.sub.mB, R.sub.gB, and C.sub.B corresponding to processing chamber B are called.
(91) Then, step **101** is performed. Step **101** can include: when processing chamber B begins an i-th processing step (i=1, 2, . . . , N), calling I.sub.Ai and I.sub.Si corresponding to the i-th processing step from the parameter table; and by using the power compensation equation (22) and according to I.sub.Ai, I.sub.Si, R.sub.mA, R.sub.gA, C.sub.A, R.sub.mB, R.sub.gB, and C.sub.B corresponding to the i-th processing step, obtaining the power compensation coefficient β.sub.Bi of processing chamber B corresponding to the i-th processing step.
(92) As shown in FIG. **7**, in a process of performing N processing steps (Step1, Step2, . . . , StepN), each processing step corresponds to an I.sub.s, an I.sub.A, and a power compensation coefficient.
(93) It should be noted that the method for obtaining the power compensation coefficient β.sub.Bi corresponding to the i-th processing step is illustrated here only with processing chamber B as an example. In practical applications, the other chambers with the same structure except the reference chamber can be suitable for the method for obtaining the power compensation coefficient β.sub.i corresponding to the i-th processing step.
(94) At **102**, the power compensation value of the present processing chamber relative to the reference chamber is calculated according to the power compensation coefficient and the power setting value of the lower RF power supply of the present processing chamber.
(95) In some optional embodiments, step **102** can specifically include: calculating the product of the power

compensation coefficient and the power setting value as the power compensation value.
(96) At **103**, the lower RF power supply **4** is controlled to output the power compensation value.
(97) In step **103**, the power output by the lower RF power supply **4** can be the compensated power value.
(98) For the plurality of processing steps, each time step **103** is performed until the current processing step ends, and a next processing step is performed, I.sub.A and I.sub.S corresponding to the next processing step can be called from the parameter table, and the power compensation coefficient corresponding to the next processing step can be calculated again. For the specific execution processes, reference can be made to FIG. **8**.
(99) Step **102** and step **103** are used to calculate the power compensation value and perform power compensation on the power setting value (i.e., P.sub.in) output by the lower RF power supply **4**. Thus, the remaining power P.sub.p utilized by the plasma **9** of the other chambers with the same structure except the reference chamber can be consistent with the remaining power P.sub.p of the reference chamber to ensure that the RF bias voltages of different chambers are consistent to achieve consistent processing results.
(100) As another technical solution, as shown in FIG. **9**, embodiments of the present disclosure also provide a power control device **20** of the lower RF power supply in the semiconductor processing equipment, which includes a calculation unit **21** and a control unit **22**. The calculation unit **21** can be configured to, when the semiconductor processing begins in the processing chamber, obtain the power compensation coefficient of the present processing chamber relative to the reference chamber by using the predetermined power compensation equation and according to the pre-obtained first RF circuit parameter set of the reference chamber and the second RF circuit parameter set of the present processing chamber that performs the semiconductor processing, and calculate the power compensation value of the present processing chamber relative to the reference chamber according to the power compensation coefficient and the power setting value of the lower RF power supply of the present processing chamber.
(101) The control unit **22** can be configured to control the lower RF power supply to output the power compensation value.
(102) The reference chamber can be a determined chamber from the plurality of processing chambers with the same structure. The first RF circuit parameter set of the reference chamber can be a combination of the feature parameters of the lower electrode of the reference chamber. The first RF circuit parameter set can include but is not limited to the current at the output end of the lower matcher in the main path of the lower electrode RF circuit, the current of the plasma sheath branch of the lower electrode RF circuit, the loss equivalent resistance and the grounded equivalent resistance of the lower electrode RF circuit, and the lower electrode-to-ground capacitance.
(103) The present processing chamber can be processing chambers with the same structure except the reference chamber. The second RF circuit parameter set of the present processing chamber can include but is not limited to the loss equivalent resistance and the grounded equivalent resistance of the lower RF circuit and the lower electrode-to-ground capacitance.
(104) Taking the inductively coupled plasma equipment shown in FIG. **4**A as an example, as shown in FIG. **2**B, capacitor C**1** and capacitor C**2** are both variable capacitors in the lower matcher **3**. The loss resistance of the lower matcher **3** and the contact resistance of the lower electrode RF circuit as a whole can be considered as the loss equivalent resistance R.sub.m of the lower electrode RF circuit. The loss equivalent resistance R.sub.m can be connected in series in the main path of the lower electrode RF circuit. The equivalent circuit part connected to the output end of the main path can include two parallel branches. One of the branches can be a lower electrode-to-ground branch. The lower electrode-to-ground branch can include a lower electrode-to-ground capacitance C and an equivalent resistance R.sub.g when the lower electrode is grounded. The other branch can be a plasma sheath branch. The plasma sheath branch can include an impedance real part R.sub.p and an equivalent inductance L.sub.p of an impedance imaginary part of the plasma **9**, and an impedance real part R.sub.s and an equivalent capacitance C.sub.s of an impedance imaginary part of the plasma sheath. Additionally, the current in the lower electrode-to-ground branch can be I.sub.c, the current in the plasma sheath branch can be I.sub.s, and the current at the output end of the lower matcher **3** in the main path of the lower electrode RF circuit can be I.
(105) It should be noted that whether for the reference chamber or other process chambers, the inherent parameters such as the loss equivalent resistance R.sub.m, the grounded equivalent resistance R.sub.g, and the lower electrode-to-ground capacitance C can remain unchanged when performing the processing. The plasma sheath parameter of the lower electrode RF circuit (e.g., the RF bias voltage and the current in the plasma sheath branch) can change with different processing processes. The current I.sub.c in the lower electrode-to-ground branch is made of most of the current I (usually greater than 10 amperes). However, the current I.sub.s in the plasma sheath branch can be small (smaller than 1 ampere). Thus, the current I.sub.s in the plasma sheath branch can be regarded as a constant current. Since the remaining power P.sub.p utilized by the plasma **9** (also referred to as absorption power) is a product of the RF bias voltage and the current I.sub.s in the plasma sheath branch, the remaining power P.sub.p can also change with the processing. Based on this, the lower electrode loss feature of different chambers can be reflected by the inherent parameters and the plasma sheath parameters. The difference in the remaining power P.sub.p between the other processing chambers and the reference chamber can be compensated according to the lower electrode loss feature to allow different chambers to have the same remaining power P.sub.p. Thus, the RF bias voltages of different chambers can be ensured to be consistent, and the processing results can be consistent.

(106) In some optional embodiments, the above power compensation equation is:

(107) $$\beta = \frac{2(R_{mB} + R_{gB})(I_A - I_S)X}{[-I_S(2R_{mB} + Y)]Y + Y\sqrt{I_S^2(2R_{mB} + Y)^2 - 4(R_{mB} + R_{gB})[I_S^2(R_{mB} - R_{mA}) - (I_A - I_S)^2(R_{mA} + R_{gA}) - (2I_S R_{mA} + X)(I_A - I_S)]}}$$

(108) Where β.sub.B is the power compensation coefficient of the present processing chamber (taking the processing chamber B in FIG. **6** as an example) relative to the reference chamber. The first RF circuit parameter set can include I.sub.A, I.sub.S, R.sub.mA, R.sub.gA, and X, where I.sub.A is the current at the output end of the matcher in the main path of the lower electrode RF circuit. I.sub.S is the current in the plasma sheath branch of the lower electrode RF circuit of the reference chamber. R.sub.mA is the loss equivalent resistance of the lower electrode RF circuit of the reference chamber; R.sub.gA is the grounded equivalent resistance of the lower electrode RF circuit of the reference chamber. X is the impedance value corresponding to the lower electrode-to-ground capacitance of the reference chamber, and

(109) $X = \frac{1}{\omega C_A}$,

where ω is the angular frequency. C.sub.A of the lower electrode-to-ground capacitance of the reference chamber.

(110) The second RF circuit parameter set can include R.sub.mB, R.sub.gB, and Y. R.sub.mB is the loss equivalent resistance of the lower electrode RF circuit of the present processing chamber. R.sub.gB is the grounded equivalent resistance of the lower electrode RF circuit of the present processing chamber. Y is the impedance value corresponding to the lower electrode-to-ground capacitance of the present processing chamber.

(111) $Y = \frac{1}{\omega C_B}$,

where ω is the angular frequency. C.sub.B of the lower electrode-to-ground capacitance of the present processing chamber.

(112) In some optional embodiments, taking the inductively coupled plasma equipment shown in FIG. **4**A as an example, the control unit **22** is also configured to activate the lower RF power supply **4** of the processing chamber and apply the determined power value to the lower electrode **8** through the matcher **3** to ensure that the plasma in the processing chamber does not ignite.

(113) Specifically, as shown in FIG. **4**B, corresponding to each processing chamber (including the reference chamber and the processing chamber), the lower RF power supply **4** of the processing chamber is activated (the upper RF power supply **1** is turned off). The determined power value P.sub.low is applied to the lower electrode **8** through matcher **3**.

(114) The determined power value P.sub.low can be low compared to the power value adopted by normal processing. Thus, when the determined power value P.sub.low is applied to the lower electrode, when the lower matcher **3** is paired, the determined power value P.sub.low can be consumed by the lower electrode-to-ground branch. Since the RF power supply **1** is turned off, and the determined power value P.sub.low is low, the power may not be sufficient to cause the plasma in the processing chamber to ignite. Thus, the plasma load cannot be generated.

(115) Based on this, as shown in FIG. **10**, the power control device **20** further includes a current detection unit **24**, a voltage detection unit **23**, and a capacitance detection unit **25**. The current detection unit **24** is arranged in the circuit between the output end of the matcher **3** and the lower electrode **8** and configured to detect the present current (i.e., I.sub.0) at the output end side of the lower matcher **3** in the main path of the lower electrode RF circuit. The voltage detection unit, for example, can be electrically connected to the RF electrode of the lower electrode **8** and configured to detect the present bias voltage value of the lower electrode **8** (i.e., V.sub.0). The capacitance detection unit can be configured to detect the lower electrode-to-ground capacitance (i.e., C) of the lower electrode **8**.

(116) Based on this, the calculation unit **21** can be further configured to calculate the loss equivalent resistance R.sub.m and the grounded equivalent resistance R.sub.g of the lower electrode RF circuit using the following equation and the present current I.sub.0, the present bias voltage value V.sub.0, and the lower electrode-to-ground capacitance C. The equations are as follows.

(117) $$R_g = \sqrt{\left(\frac{V_0}{I_0}\right)^2 - \left(\frac{1}{\omega C}\right)^2} \quad R_m = \frac{P_{low}}{I_0^2} - R_g$$

where, R.sub.g is the grounded equivalent resistance of the lower electrode RF circuit, R.sub.m is the loss equivalent resistance of the lower electrode RF circuit, V.sub.0 is the present bias voltage value, I.sub.0 is the present current, ω is the angular frequency, C is the lower electrode-to-ground capacitance, and P.sub.low is the determined power value.

(118) In some optional embodiments, the semiconductor processing can include a plurality of processing steps. The power control device **20** can further include a writing unit. The writing unit can be configured to write the pre-obtained I.sub.A (the current at the output end side of the lower matcher **3** in the main path of the lower electrode RF circuit) and I.sub.S (the current in the plasma sheath branch) into the parameter table.

(119) Optionally, I.sub.A and I.sub.s corresponding to the processing steps (Step) can be calculated through the equation (7) of the above embodiments.

(120) Based on this, taking processing chamber A as the reference chamber and processing chamber B as the chamber that is performing the processing as an example, the calculation unit **21** can be further configured to call R.sub.mA, R.sub.gA, C.sub.A, R.sub.mB, R.sub.gB, and C.sub.B. When processing chamber B starts to perform the i-th processing step (i=1, 2, . . . , N), I.sub.Ai and I.sub.Si corresponding to the i-th processing step can be called from the above parameter table. With the above power compensation equation, and according to I.sub.Ai, I.sub.Si, R.sub.mA, R.sub.gA, C.sub.A, R.sub.mB, R.sub.gB, and C.sub.B corresponding to the i-th processing step, the power

compensation coefficient β.sub.Bi of processing chamber B corresponding to the i-th processing step.
(121) In some optional embodiments, the calculation unit **21** can be configured to calculate the product of the power compensation coefficient and the power setting value as the power compensation value.
(122) In the technical solution of the power control method and device of the lower RF power supply in the semiconductor processing equipment of embodiments of the present disclosure, when the processing chamber starts the semiconductor processing, with the pre-determined power compensation equation and according to the pre-obtained first RF circuit parameter set and the second RF circuit parameter set of the present processing chamber performing the semiconductor processing, the power compensation coefficient can be obtained. According to the power compensation coefficient and the power setting value of the lower RF power supply of the present processing chamber, the power compensation value can be calculated. Then, the lower RF power supply can be controlled to output the power compensation value. Thus, the difference in the power utilized by the plasma between the other processing chambers except for the reference chamber and the reference chamber can be compensated. Thus, the consistency in the bias voltage values generated on the wafers between different chambers under the same processing recipe can be improved. Thus, the processing result consistency of the different processing chambers can be improved.
(123) As another technical solution, embodiments of the present disclosure further provide semiconductor processing equipment. Taking the inductively coupled plasma equipment shown in FIG. A as an example, the equipment includes processing chamber **11**. A dielectric window **6** is arranged at the top of processing chamber **11**. An inductive coupling coil **5** is arranged above the dielectric window **6**. The inductive coupling coil **5** can be electrically connected to the upper RF power supply **1** through the upper matcher **2**. The upper RF power supply **1** can apply the RF power to the inductive coupling coil **5** through the upper matcher **2** to excite the process gas in the processing chamber **11** to generate the plasma **9**. Moreover, the lower electrode **8** (e.g., the electrostatic chuck) can be arranged in the processing chamber **11** and configured to carry the wafer **7**. The lower electrode **8** can be electrically connected to the lower RF power supply **4** through the lower matcher **3**. The lower RF power supply **4** can be configured to apply the RF power to the lower electrode **8** to generate the RF bias voltage on the wafer surface to accelerate the ions to etch the wafer.
(124) The semiconductor processing equipment of embodiments of the present disclosure can adopt the power control device of embodiments of the present disclosure. With the device, the consistency in the bias voltage values generated on the wafers of different chambers under the same processing recipe can be improved. Thus, the processing result consistency of the different processing chambers can be improved.
(125) It can be noted that the above embodiments are merely exemplary embodiments used to illustrate the principle of the present disclosure. However, the present disclosure is not limited to this. For those skilled in the art, without departing from the spirit and essence of the present disclosure, various variations and improvements can be made. These variations and improvements are also within the scope of the present disclosure.

Claims

1. A power control method of a lower RF power supply of semiconductor processing equipment comprising: when a processing chamber starts semiconductor processing, with a predetermined power compensation equation and according to a pre-obtained first RF circuit parameter set of a reference chamber and a second RF circuit parameter set of a present processing chamber performing the semiconductor processing, obtaining a power compensation coefficient of the present processing chamber relative to the reference chamber; according to the power compensation coefficient and a power setting value of the lower RF power supply of the present processing chamber, calculating a power compensation value of the present processing chamber relative to the reference chamber; and controlling the lower RF power supply to output the power compensation value; wherein: the first RF circuit parameter set includes a current at an output end of a lower matcher in a main path of a lower electrode RF circuit of the reference chamber, a current in a plasma sheath branch of the lower electrode RF circuit of the reference chamber, a loss equivalent resistance and a ground equivalent resistance of the lower electrode RF circuit of the reference chamber, and a lower electrode-to-ground capacitance of the reference chamber; and the second RF circuit parameter set includes a loss equivalent resistance and aa grounded equivalent resistance of the lower RF circuit of the present processing chamber and a lower electrode-to-ground capacitance of the present processing chamber.
2. The power control method according to claim 1, wherein a power compensation equation is: $$B = \frac{2(R_{mB} + R_{gB})(I_A - I_S)X}{[-I_S(2R_{mB} + Y)]Y + Y\sqrt{I_S^2(2R_{mB} + Y)^2 - 4(R_{mB} + R_{gB})[I_S^2(R_{mB} - R_{mA}) - (I_A - I_S)^2(R_{mA} + R_{gA}) - (2I_S R_{mA} + X)(I_A - I_S)]}}$$ wherein: β.sub.B is the power compensation coefficient of the present processing chamber relative to the reference chamber; the first RF circuit parameter set includes I.sub.A, I.sub.S, R.sub.mA, R.sub.gA, and X; I.sub.A is a current at an output end of a matcher in a main path of a lower electrode RF circuit of the reference chamber; I.sub.S is a current in a plasma sheath branch of the lower electrode RF circuit of the reference chamber; R.sub.mA is a loss equivalent resistance of the lower electrode RF circuit of the reference chamber; R.sub.gA is a grounded equivalent resistance of the lower electrode RF circuit of the reference chamber; X is an impedance value corresponding to a lower electrode-to-ground capacitance of the reference chamber, and $X = \frac{1}{C_A}$, ω being an angular frequency, C.sub.A being the lower electrode-to-ground capacitance of the reference chamber; the second RF circuit parameter set includes R.sub.mB, R.sub.gB, and Y;

R.sub.mB is a loss equivalent resistance of a lower electrode RF circuit of the present processing chamber; R.sub.gB is a grounded equivalent resistance of the lower electrode RF circuit of the present processing chamber; Y is an impedance value corresponding to a lower electrode-to-ground capacitance of the present processing chamber, and $Y = \frac{1}{C_B}$, ω being the angular frequency, and C.sub.B being a lower electrode-to-ground capacitance of the present processing chamber.

3. The power control method according to claim 2, wherein acquisition methods of the loss equivalent resistance and the grounded equivalent resistance of the lower electrode RF circuit for each processing chamber include: turning on the lower RF power supply of the processing chamber to apply a determined power value to the lower electrode through the matcher to ensure that plasma in the processing chamber does not ignite; detecting a present current at an output end side of the matcher in a main path in the lower electrode RF circuit, a present bias voltage value of the lower electrode, and a lower electrode-to-ground capacitance; and using following equations to calculate the loss equivalent resistance and the grounded equivalent resistance of the lower electrode RF circuit according to the present current, the present bias voltage value, and the lower electrode-to-ground capacitance: $R_g = \sqrt{(\frac{V_0}{I_0})^2 - (\frac{1}{C})^2}$ and $R_m = \frac{P_{low}}{I_0^2} - R_g$; wherein: R.sub.g is the grounded equivalent resistance of the lower electrode RF circuit; R.sub.m is the loss equivalent resistance of the lower electrode RF circuit; V.sub.0 is the present bias voltage value; I.sub.0 is the present current; ω is the angular frequency; C is the lower electrode-to-ground capacitance; and P.sub.low is the determined power value.

4. The power control method according to claim 2, wherein the semiconductor processing includes a plurality of processing steps; the power control method further comprising: before performing the semiconductor processing, writing pre-obtained I.sub.A and I.sub.S corresponding to the processing steps into a parameter table; calling R.sub.mA, R.sub.gA, C.sub.A, R.sub.mB, R.sub.gB, and C.sub.B; and when the processing chamber starts performing the semiconductor processing, with the predetermined power compensation equation and according to the pre-obtained first RF circuit parameter set of the reference chamber and the second RF circuit parameter set of the present processing chamber performing the semiconductor processing, obtaining the power compensation coefficient of the present processing chamber relative to the reference chamber, including: when the present processing chamber starts performing the processing steps, calling I.sub.A and I.sub.S corresponding to a current processing step from the parameter table; and with the power compensation equation and according to I.sub.A, I.sub.S, R.sub.mA, R.sub.gA, C.sub.A, R.sub.mB, R.sub.gB, and C.sub.B, obtaining the power compensation coefficient.

5. The power control method according to claim 1, wherein according to the power compensation coefficient and the power setting value of the lower RF power supply of the present processing chamber, obtaining the power compensation value of the present processing chamber relative to the reference chamber includes: calculating a product of the power compensation coefficient and the power setting value as the power compensation value.

6. A power control device of a lower RF power supply in semiconductor process equipment comprising a calculation unit and a control unit, wherein: the calculation unit is configured to, when a processing chamber starts semiconductor processing, adopt a predetermined power compensation equation, a pre-obtained first RF circuit parameter set of a reference chamber, and a second RF circuit parameter set of a present processing chamber performing the semiconductor processing, obtain a power compensation coefficient of the present processing chamber relative to the reference chamber, and according to the power compensation coefficient and a power setting value of the lower RF power supply of the present processing chamber, and calculate a power compensation value of the present processing chamber relative to the reference chamber; and the control unit is configured to control the lower RF power supply to output the power compensation value; wherein: the first RF circuit parameter set includes a current at an output end of a lower matcher in a main path of a lower electrode RF circuit of the reference chamber, a current in a plasma sheath branch of the lower electrode RF circuit of the reference chamber, a loss equivalent resistance and a ground equivalent resistance of the lower electrode RF circuit of the reference chamber, and a lower electrode-to-ground capacitance of the reference chamber; and the second RF circuit parameter set includes a loss equivalent resistance and aa grounded equivalent resistance of the lower RF circuit of the present processing chamber and a lower electrode-to-ground capacitance of the present processing chamber.

7. The power control device according to claim 6, wherein the power compensation equation is: $B = \frac{2(R_{mB} + R_{gB})(I_A - I_S)X}{[-I_S(2R_{mB} + Y)]Y + Y\sqrt{I_S^2(2R_{mB} + Y)^2 - 4(R_{mB} + R_{gB})[I_S^2(R_{mB} - R_{mA}) - (I_A - I_S)^2(R_{mA} + R_{gA}) - (2I_S R_{mA} + X)(I_A - I_S)]}}$ wherein: β.sub.B is the power compensation coefficient of the present processing chamber relative to the reference chamber; the first RF circuit parameter set includes I.sub.A, I.sub.S, R.sub.mA, R.sub.gA, and X; I.sub.A is a current at an output end of a matcher in a main path of a lower electrode RF circuit; I.sub.S is a current in a plasma sheath branch of the lower electrode RF circuit of the reference chamber; R.sub.mA is a loss equivalent resistance of the lower electrode RF circuit of the reference chamber; R.sub.gA is a grounded equivalent resistance of the lower electrode RF circuit of the reference chamber; X is an impedance value corresponding to a lower electrode-to-ground capacitance of the reference chamber, and $X = \frac{1}{C_A}$, ω being an angular frequency, C.sub.A being the lower electrode-to-ground capacitance of the reference chamber; the second RF circuit parameter set includes R.sub.mB, R.sub.gB, and Y; R.sub.mB is a loss equivalent resistance of a lower electrode RF circuit of the present processing chamber; R.sub.gB is a grounded equivalent resistance of the lower electrode RF circuit of the present processing chamber; Y is an impedance value

corresponding to a lower electrode-to-ground capacitance of the present processing chamber, and $Y = \frac{1}{C_B}$, ω being the angular frequency, and C.sub.B being a lower electrode-to-ground capacitance of the present processing chamber.

8. The power control device according to claim 6, wherein the control unit is further configured to turn on the lower RF power supply of the processing chamber to apply a determined power value to the lower electrode through the matcher to ensure that a plasma in the processing chamber does not ignite; the power control device further comprising: a current detection unit configured to detect a present current at an output end of the matcher in a main path in the lower electrode RF circuit, and a present bias voltage value of the lower electrode; a voltage detection unit configured to detect the present bias voltage value of the lower electrode; a capacitance detection unit configured to detect a lower electrode-to-ground capacitance; and the calculation unit further configured to use following equations to calculate the loss equivalent resistance and the grounded equivalent resistance of the lower electrode RF circuit according to the present current, the present bias voltage value, and the lower electrode-to-ground capacitance:

$R_g = \sqrt{(\frac{V_0}{I_0})^2 - (\frac{1}{C})^2}$ and $R_m = \frac{P_{low}}{I_0^2} - R_g$; wherein: R.sub.g is the grounded equivalent resistance of the lower electrode RF circuit; R.sub.m is the loss equivalent resistance of the lower electrode RF circuit; V.sub.0 is the present bias voltage value; I.sub.0 is the present current; ω is the angular frequency; C is the lower electrode-to-ground capacitance; and P.sub.low is the determined power value.

9. The power control device according to claim 7, wherein the semiconductor processing includes a plurality of processing steps; the power control device further comprising: a writing unit configured to, before performing the semiconductor processing, write pre-obtained I.sub.A and I.sub.S corresponding to the processing steps into a parameter table; and the calculation unit further configured to call R.sub.mA, R.sub.gA, C.sub.A, R.sub.mB, R.sub.gB, and C.sub.B, when the present processing chamber starts performing the processing steps, call I.sub.A and I.sub.S corresponding to a current processing step from the parameter table, and with the power compensation equation and according to I.sub.A, I.sub.S, R.sub.mA, R.sub.gA, C.sub.A, R.sub.mB, R.sub.gB, and C.sub.B, obtain the power compensation coefficient.

10. The power control device according to claim 6, wherein the calculation unit is configured to calculate a product of the power compensation coefficient and the power setting value as the power compensation value.

11. Semiconductor processing equipment comprising: a processing chamber, a lower electrode being arranged in the processing chamber; a matcher; a lower RF power supply, the lower electrode being electrically connected to the lower RF power supply through the matcher; and a power control device including: a calculation unit configured to, when a processing chamber starts semiconductor processing, with a predetermined power compensation equation and according to a pre-obtained first RF circuit parameter set of a reference chamber and a second RF circuit parameter set of a present processing chamber performing the semiconductor processing, obtain a power compensation coefficient of the present processing chamber relative to the reference chamber, and according to the power compensation coefficient and a power setting value of the lower RF power supply of the present processing chamber, calculate a power compensation value of the present processing chamber relative to the reference chamber; and a control unit configured to control the lower RF power supply to output the power compensation value; wherein: the first RF circuit parameter set includes a current at an output end of a lower matcher in a main path of a lower electrode RF circuit of the reference chamber, a current in a plasma sheath branch of the lower electrode RF circuit of the reference chamber, a loss equivalent resistance and a ground equivalent resistance of the lower electrode RF circuit of the reference chamber, and a lower electrode-to-ground capacitance of the reference chamber; and the second RF circuit parameter set includes a loss equivalent resistance and aa grounded equivalent resistance of the lower RF circuit of the present processing chamber and a lower electrode-to-ground capacitance of the present processing chamber.