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METHOD AND APPARATUS FOR DETERMINING PHASE DIFFERENCE, STORAGE MEDIUM, AND ELECTRONIC DEVICE

Abstract

A method for determining a phase difference includes sending a first message carrying a target slot length of the target cycle template to a downstream node at a first start time of a window of a predetermined target cycle template; receiving a second message from the downstream node at a second start time of a window of the target cycle template, where the second message carries a first offset value indicating an offset of a receiving time at which the downstream node receives the first message in the target cycle template; and determining, based on the target slot length, the first offset value, and a second offset value, a phase difference between the upstream node and the downstream node, where the second offset value is used for indicating an offset of a receiving time at which the upstream node receives the second message in the target cycle template.

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Background/Summary

TECHNICAL FIELD

[0001] Embodiments of this disclosure relate to the field of communications, specifically a method and apparatus for determining a phase difference, a storage medium, and an electronic device.

BACKGROUND

[0002] With the rapid development of network communication technology, determinism becomes an important indicator and key technology for future networks. Therefore, the Internet Engineering Task Force (IETF) Deterministic Networking (DetNet) working group has proposed large-scale deterministic IP network forwarding technology (LDN). Usually, in large-scale networks, frequency synchronization is achievable, but network-wide time synchronization is difficult to achieve.

[0003] In the related art, within the LDN domain, nodes adopt a time-slot cyclic queue scheduling technique, which may support a single template or multiple cycle templates. If upstream and downstream nodes support cycle templates with the same time-slot length, there may be a certain offset between the slots of the same templates of the upstream node and the downstream node after device startup, known as the phase difference Δ. If the upstream node and the downstream node support multiple cycle templates simultaneously, slots for each cycle template have a phase difference, and the phase differences of different templates may vary. A typical example is shown in FIG. **1**, which illustrates the phase difference between slots of upstream and downstream nodes with multiple cycle templates in the related art. As shown in FIG. **1**, the upstream node and the downstream node support three cycle templates A, B, and C simultaneously, with time-slot lengths configured as T, 2T, and 4T, respectively. T is the base time-slot length or period. The phase differences corresponding to these three templates are ΔA, ΔB, and ΔC, respectively. In deterministic service path planning, it is necessary to calculate the precise end-to-end delay and jitter for each cycle template to select the optimal path. This may require obtaining the phase difference of the slots of each identical cycle template between the upstream node and the downstream node. However, the LDN technology cannot provide a precise phase difference of the slots.

[0004] Currently, no effective solution has been proposed to solve the problem of failing to accurately obtain a phase difference corresponding to the same cycle template supported by upstream and downstream nodes in the related art.

SUMMARY

[0005] Embodiments of this disclosure provide a method and apparatus for determining a phase difference, a storage medium, and an electronic device to solve at least the problem of failing to accurately obtain a phase difference corresponding to the same cycle template supported by upstream and downstream nodes in the related art.

[0006] According to an embodiment of this disclosure, a method for determining a phase difference is provided. The method is applied to an upstream node. The method includes sending a first message to a downstream node at a first start time of a window of a predetermined target cycle template, where the first message carries a target slot length of the target cycle template; receiving a second message returned by the downstream node at a second start time of a window of the target cycle template, where the second message carries a first offset value, the first offset value is used for indicating an offset of a receiving time at which the downstream node receives the first message in the target cycle template, and the target slot length is used by the downstream node for determining the target cycle template; and determining, based on the target slot length, the first

offset value, and a second offset value, a phase difference between a target cycle template used by the upstream node and a target cycle template used by the downstream node, where the second offset value is used for indicating an offset of a receiving time at which the upstream node receives the second message in the target cycle template.

[0007] According to an embodiment of this disclosure, an apparatus for determining a phase difference is provided. The apparatus is applied to an upstream node. The apparatus includes a sending module configured to send a first message to a downstream node at a first start time of a window of a predetermined target cycle template, where the first message carries a target slot length of a target cycle template; a receiving module configured to receive a second message returned by the downstream node at a second start time of a window of the target cycle template, where the second message carries a first offset value, the first offset value is used for indicating an offset of a receiving time at which the downstream node receives the first message in the target cycle template, and the target slot length is used by the downstream node for determining the target cycle template; and a determination module configured to determine, based on the target slot length, the first offset value, and a second offset value, a phase difference between a target cycle template used by the upstream node and a target cycle template used by the downstream node, where the second offset value is used for indicating an offset of a receiving time at which the upstream node receives the second message in the target cycle template.

[0008] According to an embodiment of this disclosure, a computer-readable storage medium is provided. The storage medium stores a computer program which, when executed by a processor, causes the processor to perform steps of the method of any previous method embodiment.

[0009] According to an embodiment of this disclosure, an electronic device is provided. The electronic device includes a memory and a processor. The memory stores a computer program. The processor is configured to execute the computer program to perform steps of the method of any previous method embodiment.

Description

BRIEF DESCRIPTION OF DRAWINGS

[0010] FIG. **1** is a diagram illustrating the phase difference between slots of upstream and downstream nodes with multiple cycle templates in the related art.

[0011] FIG. **2** is a block diagram of a hardware structure of a mobile terminal for a method for determining a phase difference according to an embodiment of this disclosure.

[0012] FIG. **3** is a flowchart of a method for determining a phase difference according to an embodiment of this disclosure.

[0013] FIG. **4** is an overall flowchart of phase difference measurement according to an embodiment of this disclosure.

[0014] FIG. **5** is a diagram of sending a measurement message according to an embodiment of this disclosure.

[0015] FIG. **6** is a first flowchart of measuring a phase difference corresponding to a cycle template T between N**1** and N**2** according to an embodiment of this disclosure.

[0016] FIG. **7** is a first example diagram of a principle for calculating a phase difference according to an embodiment of this disclosure.

[0017] FIG. **8** is a second flowchart of measuring a phase difference corresponding to a cycle template T between N**1** and N**2** according to an embodiment of this disclosure.

[0018] FIG. **9** is a second example diagram of a principle for calculating a phase difference according to an embodiment of this disclosure.

[0019] FIG. **10** is a diagram of a sub-TLV encapsulation format according to an embodiment of this disclosure.

[0020] FIG. **11** is a block diagram of an apparatus for determining a phase difference according to an embodiment of this disclosure.

DETAILED DESCRIPTION

[0021] Embodiments of this application are described hereinafter in detail with reference to drawings and in conjunction with embodiments.

[0022] It is to be noted that terms such as “first” and “second” in the description, claims, and drawings of this disclosure are used for distinguishing between similar objects and are not necessarily used for describing a particular order or sequence.

[0023] Method embodiments provided in the embodiments of this application may be performed in a mobile terminal, a computer terminal, or a similar computing apparatus. Using being executed in a mobile terminal as an example, FIG. **2** is a block diagram of a hardware structure of a mobile terminal for a method for determining a phase difference according to an embodiment of this disclosure. As shown in FIG. **2**, the mobile terminal may include one or more (one is shown in FIG. **2**) processors **202** (the processors **202** may include, but are not limited to, a processing apparatus such as a microcontroller unit (MCU) or a field programmable gate array (FPGA)) and a memory **204** configured to store data. The mobile terminal may also include a transmission device **206** having a communication function and an input and output device **208**. It is to be understood by those of ordinary skill in the art that the structure shown in FIG. **2** is illustrative and not intended to limit the structure of the mobile terminal. For example, the mobile terminal may also include more or fewer components than the components shown in FIG. **2** or may have a configuration different from the configuration shown in FIG. **2**.

[0024] The memory **204** may be configured to store a computer program such as a software program and a module of application software, for example, the computer program corresponding to the method for determining a phase difference in embodiments of this disclosure. The processor **202** executes the computer program stored in the memory **204** to perform various functional applications and data processing, that is, to implement the preceding method. The memory **204** may include a high-speed random-access memory and may further include a non-volatile memory such as one or more magnetic storage apparatuses, flash memories or other non-volatile solid-state memories. In some examples, the memory **204** may also be a memory remote from the processor **202** and connectable to the mobile terminal via a network. Examples of the network include, but are not limited to, the Internet, an intranet, a local area network, a mobile communication network, and a combination thereof.

[0025] The transmission device **206** is configured to receive or send data via a network. Examples of the network may include a wireless network provided by a communication provider of the mobile terminal. In an example, the transmission device **206** includes a network interface controller (NIC) that may be connected to other network devices via a base station and thus can communicate with the Internet. In an example, the transmission device **206** may be a radio frequency (RF) module configured to communicate with the Internet wirelessly.

[0026] An embodiment provides a method for determining a phase difference. FIG. **3** is a flowchart of a method for determining a phase difference according to an embodiment of this disclosure. As shown in FIG. **3**, the method includes the following steps:

[0027] In step S**302**, a first message is sent to a downstream node at a first start time of a window of a predetermined target cycle template, where the first message carries a target slot length of the target cycle template.

[0028] In step S**304**, a second message returned by the downstream node at a second start time of a window of the target cycle template is received, where the second message carries a first offset value, the first offset value is used for indicating an offset of a receiving time at which the downstream node receives the first message in the target cycle template, and the target slot length is used by the downstream node for determining the target cycle template.

[0029] In step S**306**, a phase difference between the target cycle template used by the upstream

node and the target cycle template used by the downstream node is determined based on the target slot length, the first offset value, and a second offset value, where the second offset value is used for indicating an offset of a receiving time at which the upstream node receives the second message in the target cycle template.

[0030] These steps may be performed by a network node such as a network upstream node, may be performed by a network device such as a network switch or a router, or may be performed by a unit or a terminal that has information receiving, sending, and processing capabilities.

[0031] In this embodiment, the first message may carry slot lengths corresponding to target cycle templates with different target slot lengths. For example, the first message may carry three target cycle templates: target cycle template A, target cycle template B, and target cycle template C. The target slot length of target cycle template A is T, the target slot length of target cycle template B is 2T, and the target slot length of target cycle template C is 4T. Accordingly, the phase difference corresponding to each target cycle template between the upstream node and the downstream node can be randomly determined. Additionally, the corresponding phase differences can be determined based on the priority order of these three target cycle templates. For example, if the priority order of the three target cycle templates is that the priority order of target cycle template A is greater than the priority order of target cycle template B, and the priority order of target cycle template B is greater than the priority order of target cycle template C, the phase difference corresponding to target cycle template A between the upstream node and the downstream node can be determined first, followed by the phase difference corresponding to target cycle template B, and finally the phase difference corresponding to target cycle template C. Of course, the phase differences corresponding to target cycle templates A, B, and C between the upstream node and the downstream node can also be determined simultaneously. It is to be noted that the example of different target cycle templates with different target slot lengths is an example embodiment. The target cycle templates with different target slot lengths are not limited to this example.

[0032] In this embodiment, interactions between multiple upstream and downstream nodes may also be included. For example, when there are node **1**, node **2**, node **3**, and node **4**, where node **2** is the downstream node of node **1** and the upstream node of node **3**, and node **3** is the downstream node of node **2** and the upstream node of node **4**, it is required to determine the phase difference corresponding to the same target cycle template between node **1** and node **2**, the phase difference corresponding to the same target cycle template between node **2** and node **3**, and the phase difference corresponding to the same target cycle template between node **3** and node **4**. Accordingly, the corresponding phase differences can be determined based on the priority order of the phase difference determination requirements among these multiple nodes. For example, if the priority order of the phase difference determination requirement of node **1** and node **2** is greater than the priority order of the phase difference determination requirement of node **2** and node **3**, and the priority order of the phase difference determination requirement of node **2** and node **3** is greater than the priority order of the phase difference determination requirement of node **3** and node **4**, the phase difference corresponding to the same target cycle template between node **1** and node **2** can be determined first, followed by the phase difference corresponding to the same target cycle template between node **2** and node **3**, and finally the phase difference corresponding to the same target cycle template between node **3** and node **4**. It is to be noted that the example of the upstream and downstream nodes is an example embodiment. The upstream and downstream nodes are not limited to this example.

[0033] In this embodiment, the first message carrying the target slot length of the target cycle template is sent to the downstream node at the first start time of the window of the predetermined target cycle template and the second message that is returned by the downstream node at the second start time of a window of the target cycle template and carries the first offset value used for indicating the offset of the receiving time at which the downstream node receives the first message in the target cycle template is received, the phase difference between the target cycle template used

by the upstream node and the target cycle template used by the downstream node is determined based on the target slot length, the first offset value, and the second offset value used for indicating the offset of the receiving time at which the upstream node receives the second message in the target cycle template. By using the method of this disclosure, the phase difference between the target cycle template used by the upstream node and the target cycle template used by the downstream node is determined by acquiring the slot offset generated by the downstream node receiving the first message from the upstream node, acquiring the slot offset generated by the upstream node receiving the second message from the downstream node in the same target cycle template, and acquiring the target slot length of the target cycle template, thereby achieving the purpose of determining the phase difference corresponding to the same cycle template supported by the upstream node and the downstream node in the absence of accurate link delay information, solving the problem in the related art where the phase difference corresponding to the same cycle template supported by the upstream node and the downstream node cannot be accurately acquired, and achieving the effect of accurately calculating the end-to-end delay and jitter through the slot phase difference to determine the optimal deterministic service path.

[0034] In an example embodiment, determining, based on the target slot length, the first offset value, and the second offset value, the phase difference between the target cycle template used by the upstream node and the target cycle template used by the downstream node includes determining a second relationship among the phase difference, the target slot length, the first offset value, and the second offset value based on a first relationship between the first offset value and the second offset value; in response to determining based on the second relationship that the phase difference has multiple values, determining a respective link delay range corresponding to each value of the phase difference to obtain multiple link delay ranges, where a link delay is a link delay between the upstream node and the downstream node; and determining the unique value of the phase difference based on a third relationship between each link delay range and an estimated delay obtained by pre-estimating the link delay. In this embodiment, when the target slot length is T and the values of the phase difference are $\Delta 1$ and $\Delta 2$, if it is determined that the delay range corresponding to $\Delta 1$ is [0, T/5], the delay range corresponding to $\Delta 2$ is [T/3, T], and the estimated delay offset range may be [0, T/4) (or may be, for example, [0, T/5], [T/6, T/5], or [T/5, T/4)), when the estimated delay is T/4, it is indicated that the estimated delay is neither within the delay range corresponding to $\Delta 1$ nor within the delay range corresponding to $\Delta 2$. In this case, it is feasible to determine the phase difference by adding up the estimated delay and a value taken from the estimated delay offset range. For example, T/5 is taken from the estimated delay offset range, and T/5 and T/4 are added up to obtain 9T/20, that is, the phase difference $\Delta 2$ between the target cycle template used by the upstream node and the target cycle template used by the downstream node, where $T/5<T/3<9T/20$. It is to be noted that the example of the target slot length, the phase difference, the delay range corresponding to the phase difference, and the estimated delay is an example embodiment. The target slot length, the phase difference, the delay range corresponding to the phase difference, and the estimated delay are not limited to this example.

[0035] In an example embodiment, determining the second relationship among the phase difference, the target slot length, the first offset value, and the second offset value based on the first relationship between the first offset value and the second offset value includes at least one of the following: in response to the first relationship indicating that the first offset value is less than or equal to the second offset value, determining that the second relationship satisfies the following formula: $4=(\alpha 2+T-\alpha 1)/2$ or $4=(\alpha 2-\alpha 1)/2$; or in response to the first relationship indicating that the first offset value is greater than the second offset value, determining that the second relationship satisfies the following formula: PCT/CN2023/089873 ($\alpha 2+T-\alpha$**1**)/2 or $4=(\alpha 2+2T-\alpha 1)/2$.

[0036] Here Δ denotes the phase difference, T denotes the target slot length, $\alpha 1$ denotes the first offset value, and $\alpha 2$ denotes the second offset value. In this embodiment, when α**1** is T/4 and $\alpha 2$ is T/2, A is 5T/8 or T/8 obtained by substituting $\alpha 1$ and $\alpha 2$ into the formula; and when $\alpha 1$ is T/2 and

α2 is T/4, A is 3T/8 or 7T/8 obtained by substituting α1 and α2 into the formula. That is, two phase differences can be obtained through the first offset value, the second offset value, and the formulas above. In this case, the unique value can be determined from the two phase differences through the respective delay ranges corresponding to the two phase differences and the estimated delay obtained by pre-estimating the link delay. In addition, the actual link delay can be reversely deduced from the first offset value and the two phase differences, and the estimated delay should be slightly different from the actual link delay.

[0037] In an example embodiment, determining the respective link delay range corresponding to each value of the phase difference includes at least one of the following: in response to the phase difference 4=(α2−α1)/2, determining that the link delay range is

[00001] $n * T + \frac{a1 + a2}{2} \pm \frac{T}{4}$;

in response to the first relationship indicating that the first offset value is less than or equal to the second offset value and in response to the phase difference 4=(α2+T−α1)/2, determining that the link delay range is

[00002] $n * T + \frac{a1 + a2 + T}{2} \pm \frac{T}{4}$;

in response to the first relationship indicating that the first offset value is greater than the second offset value and in response to the phase difference Δ=(α2+T−α1)/2, determining that the link delay range is

[00003] $n * T + \frac{a1 + a2 + T}{2} \pm \frac{T}{4}$;

or in response to the phase difference 4=(α2+2T−α1)/2, determining that the link delay range is

[00004] $n * T + \frac{a1 + a2}{2} \pm \frac{T}{4}$.

[0038] Here n is an integer. In this embodiment, n is an integer that is tried to be taken. For example, in the case where T=10 μs, α1=1 μs, and α2=3 μs, in the case where one phase difference (α2−α1)/2 is 1 μs and the other phase difference (α2+T−α1)/2 is 6 μs, the link delay range corresponding to Δ=1 μs is n*T+2±2.5 μs, and the link delay range corresponding to Δ=6 μs is n*T+7±2.5 μs, and when the estimated delay is 23 μs, the link delay range may be represented as 2*10+2+1 μs, that is, A=1 μs is the final value of the phase difference. When T=20 μs, α1=15 μs, and α2=5 μs, in the case where one phase difference (α2+T−α1)/2 is 5 μs and the other phase difference (α2+2T−α1)/2 is 15 μs, the link delay range corresponding to Δ=5 μs is n*T+20±5 μs, the link delay range corresponding to Δ=15 μs is n*T+10±5 μs, and when the estimated delay is 83 μs, the link delay range may be represented as 3*20+20+3 μs, that is, Δ=5 μs is the final value of the phase difference. It is to be noted that this determination manner of n and the phase value is an example embodiment. The determination manner of n and the phase value is not limited to this example.

[0039] In an example embodiment, determining the unique value of the phase difference based on the third relationship between each link delay range and the estimated delay obtained by pre-estimating the link delay includes: determining a target link delay range from the link delay ranges based on the third relationship, where the target link delay range is a range within which the estimated delay falls; and determining the unique value of the phase difference corresponding to the target link delay range. In this embodiment, when there are three link delay ranges, namely link delay range **1**, link delay range **2**, and link delay range **3**, when it is determined based on the estimated delay and the estimated delay offset range that the estimated delay range is link delay range **1**, link delay range **1** is determined as the target link delay range, that is, the phase difference corresponding to link delay range **1** is the unique value; when it is determined based on the estimated delay and the estimated delay offset range that the estimated delay range is link delay range **2**, link delay range **2** is determined as the target link delay range, that is, the phase difference corresponding to link delay range **2** is the unique value; and when it is determined based on the estimated delay and the estimated delay offset range that the estimated delay range is link delay range **3**, link delay range **3** is determined as the target link delay range, that is, the phase difference corresponding to link delay range **3** is the unique value. It is to be noted that the example of the

target link delay range is an example embodiment. The target link delay range is not limited to this example.

[0040] In an example embodiment, the first message includes a first type field and a first length field. The first type field is used for indicating that the type of the first message is a type used for measurement of the phase difference. The first length field is used for indicating the target slot length. In this embodiment, the first message may also include, for example, a field used for indicating the length of the first message.

[0041] In an example embodiment, the second message includes a second type field, a second length field, and a compensation field. The second type field is used for indicating that the type of the second message is a type used for measurement of the phase difference. The second length field is used for indicating the target slot length. The compensation field is used for indicating the first offset value. In this embodiment, the second message may also include, for example, a field used for indicating the length of the second message, a field used for carrying the first offset value, and a field used for carrying the second offset value. The second offset value may not be carried in the message.

[0042] In an example embodiment, after determining, based on the target slot length, the first offset value, and the second offset value, the phase difference between the target cycle template used by the upstream node and the target cycle template used by the downstream node, the method also includes at least one of the following: saving the phase difference locally in the upstream node; or announcing the phase difference to another network node. In this embodiment, after the phase difference is stored locally in the upstream node, when the cycle template is subsequently used again by the upstream node and the downstream node, the phase difference corresponding to the cycle template can be called locally in the upstream node. After the phase difference corresponding to the cycle template is announced to another network node, the another network node may store the phase difference corresponding to the cycle template. When the cycle template is required, the phase difference corresponding to the cycle template can be directly called.

[0043] Apparently, the preceding embodiments are some of the embodiments of this disclosure.

[0044] This disclosure is described in detail hereinafter in conjunction with embodiments.

[0045] An embodiment of this disclosure provides a process of a method for measuring a phase difference. FIG. **4** is an overall flowchart of phase difference measurement according to an embodiment of this disclosure. As shown in FIG. **4**, the process includes the following steps.

[0046] In S**402**, the process starts.

[0047] In S**404**, the upstream node and the downstream node enable the phase difference measurement function of this disclosure and specify information about a cycle template T (corresponding to the preceding target cycle template).

[0048] In S**406**, the upstream node constructs a measurement message, encapsulates the cycle template T into the measurement message, and sends the measurement message (corresponding to the first message) to the downstream at the start time (corresponding to the first start time) of a window of the cycle template (corresponding to the window of the target cycle template).

[0049] In S**408**, the downstream node receives the measurement message, records the time t**1** (corresponding to a receiving time at which the downstream node receives the first message) at which the measurement message falls locally, and extracts the cycle window T.

[0050] In S**410**, a first determination is performed to determine whether the downstream node supports the cycle template T.

[0051] In S**412**, when the first determination result is no, the process ends.

[0052] In S**414**, when the first determination result is yes, the offset value α1 (corresponding to the first offset value) in the cycle window is calculated based on t**1**.

[0053] In S**416**, the downstream node encapsulates the intra-cycle offset value α1 into the measurement message and sends the measurement message (corresponding to the second message) back to the upstream node at a start time (corresponding to the second start time) of a window of

the cycle template T.

[0054] In S**418**, the upstream node receives the measurement message, records the time t**2** (corresponding to the receiving time at which the upstream node receives the second message) at which the measurement message falls locally, and calculates the offset value α2 (corresponding to the second offset value) in the cycle window T based on t**2**.

[0055] In S**420**, the upstream node calculates two phase differences based on the cycle template T and the intra-cycle offset values α1 and α2, selects the phase difference Δ based on a rough value (corresponding to the estimated delay) of the link delay, and performs step S**412**.

[0056] In step S**408**, the downstream node extracts the cycle template window value T carried in the measurement message. If the downstream node found that the cycle template is not supported locally (that is, there is no cycle template locally), the downstream node does not perform subsequent calculation, and this measurement ends.

[0057] In step S**420**, FIG. **5** is a diagram of sending a measurement message according to an embodiment of this disclosure. As shown in FIG. **5**, according to the cycle template T and the measured intra-cycle offset values α1 and α2, and assuming that the length of the link delay is L (unknown), the calculation principle of the phase difference is based on the following relationship:

[00005]$$\begin{cases} (L - \quad)\%T = a1 \\ (L - (T - \quad))\%T = a2 \end{cases} \quad (0 \le a1, a2 < T),$$

where % denotes a modulo operation. For example, 17% 10=7, and −3% 10=7. Δ denotes the phase difference.

[0058] In the preceding formula, {circle around (2)}−{circle around (1)}=(2Δ−T) % T=α2−α1.

[0059] Since 0≤a1<T, and 0≤a2<T, the preceding formula is equivalent to: (2Δ−T) % T=(α2−α1) % T ⇔ (2Δ−T−α2+α1) % T=0.

[0060] To make the preceding formula apply, 2Δ−T−α2+α1=m*T is satisfied, and the phase difference

[00006] $= \frac{a2 - a1 + (m+1) * T}{2}$

is obtained by deforming 2Δ−T−α2+α1=m*T, where m is an integer.

[0061] 0≤Δ<T, so when α2≥α1, the possible values of m are −1 and 0; in the case where m<−1, 4<0; and in the case where m>0, Δ>T, both of the cases do not satisfy the requirements. When α2<α1, the possible values of m are 0 and 1; similarly, the cases of m>1 and m<0 do not satisfy the requirements; and the details are not repeated.

[0062] From the preceding, the calculation formula of the phase difference between the upstream node and the downstream node is as follows:

[00007] $$= \begin{cases} (a2 + T - a1) / 2 \text{or} (a2 - a1) / 2, \text{if} a2 \ge a1 \\ (a2 + T - a1) / 2 \text{or} (a2 + 2T - a1) / 2, \text{if} a2 < a1 \end{cases} . \quad \text{(formula1)}$$

[0063] For each pair of measurement values α1 and α2, two possible phase difference values can be obtained according to formula 1. Further, which value is selected as the final phase difference calculation result can be determined according to the rough value of the link delay L between the upstream node and the downstream node.

[0064] The two phase difference values obtained from the calculation can be configured to deduce the corresponding theoretical actual value of L. Therefore, to infer A from the measurement value of L, the measurement value of L should be located near the theoretical value. Since the interval between the two phase differences is T/2, when the offset of the measurement value of L from the theoretical value is not greater than T/4, one of the phase differences can be uniquely determined. Therefore, the offset range allowed for the measurement value of L is [0, T/4).

[0065] When α2>α1, if the measurement value range of L is

[00008] $n * T + \frac{a1 + a2}{2} \pm \frac{T}{4}$,

the phase difference value is

[00009]$\frac{a2 - a1}{2}$
(criterion 1). When the measurement value range of L is
[00010]$n * T + \frac{a1 + a2 + T}{2} \pm \frac{T}{4}$,
the phase difference value is
[00011]$\frac{a2 - a1 + T}{2}$
(criterion 2).
[0066] When α2≤α1, if the measurement value range of L is
[00012]$n * T + \frac{a1 + a2 + T}{2} \pm \frac{T}{4}$,
the phase difference value is
[00013]$\frac{a2 - a1 + T}{2}$
(criterion 3), and if the value range of L is
[00014]$n * T + \frac{a1 + a2}{2} \pm \frac{T}{4}$,
the phase difference value is
[00015]$\frac{a2 - a1 + 2T}{2}$
(criterion 4). Here n is an integer.
[0067] In summary, by using this method, it is not necessary to obtain the precise value of the link delay L between the upstream node and the downstream node. It is only required to acquire a rough value of L, with the allowable error range of L being [0, T/4), to obtain the precise value of the phase difference. For example, if the slot length of the cycle template is T=10 μs, the required measurement accuracy of L is approximately ±2.5 μs. If the slot length of the cycle template is T=40 μs, the required measurement accuracy of L is approximately ±10 μs. This significantly reduces the requirement for link delay accuracy. After the phase difference is obtained from measurement, the phase difference can be stored locally or announced to another node in the network.
[0068] This disclosure is further described hereinafter in conjunction with examples.
Example One
[0069] In this example, it is assumed that there are two network devices N**1** and N**2**. The two devices are synchronized in frequency but not synchronized in time. In the service direction from N**1** to N**2**, N**1** is an upstream device node, and N**2** is a downstream device node. Both N**1** and N**2** support the cycle template T=10 μs. The measured rough length of the link delay between N**1** and N**2** is approximately 23 μs. FIG. **6** is a first flowchart of measuring a phase difference corresponding to a cycle template T between N**1** and N**2** according to an embodiment of this disclosure. As shown in FIG. **6**, the process includes the following steps.
[0070] In S**602**, the process starts.
[0071] In S**604**, a phase difference measurement function between N**1** and N**2** is started, and a measurement cycle template T=10 μs is specified.
[0072] In S**606**, N**1** constructs a phase difference measurement message carrying the cycle template T=10 μs, and sends the measurement message to N**2** at the start time of a window of the cycle template T.
[0073] In S**608**, N**2** receives the measurement message, records the message receiving time, extracts the cycle template T=10 μs according to the measurement type, and calculates that the offset of the receiving time of the measurement message in the cycle template is α1=1 μs.
[0074] In S**610**, N**2** encapsulates the offset value in the window of the cycle template T into the measurement message and sends the measurement message to N**1** at the start time of a window of the cycle template T.
[0075] In S**612**, N**1** receives the measurement message, records the receiving time of the measurement message, extracts the cycle template T=10 μs according to the measurement type, and calculates that the offset of the receiving time of the measurement message in the cycle template is α2=3 μs.
[0076] In S**614**, N**1** calculates, based on the cycle template T, α1, and α2, that the phase difference

value is Δ=1 μs.
[0077] In S**616**, the process ends.
[0078] The steps of determining the phase difference are described as follows.
[0079] FIG. **7** is a first example diagram of a principle for calculating a phase difference according to an embodiment of this disclosure. As shown in FIG. **7**, since α2>α1, the value of Δ may be (α2−α1)/2=1 μs or (α2−α1+T)/2=6 μs according to formula 1.
[0080] Further, the value range of L corresponding to Δ=1 μs is n*T+2±2.5 μs (criterion 1), and the value range of L corresponding to Δ=6 μs is n*T+7±2.5 μs (criterion 2). Since the measured rough value of L is approximately 23 μs, L can be expressed as 2*10+2+1 μs, which falls within the range of n*T+2±2.5 μs. Therefore, the final value of A is lus.
Example Two
[0081] In this example, it is assumed that there are two network devices N**1** and N**2**. The two devices are synchronized in frequency but not synchronized in time. In the service direction from Nlto N**2**, N**1** is an upstream device node, and N**2** is a downstream device node. Both N**1** and N**2** support the cycle template T=20 μs. The measured rough length of the link delay between N**1** and N**2** is approximately 83 μs. FIG. **8** is a second flowchart of measuring a phase difference corresponding to a cycle template T between N**1** and N**2** according to an embodiment of this disclosure. As shown in FIG. **8**, the process includes the following steps.
[0082] In S**802**, the process starts.
[0083] In S**804**, a phase difference measurement function between N**1** and N**2** is started, and a measurement cycle template T=20 μs is specified.
[0084] In S**806**, N**1** constructs a phase difference measurement message carrying the cycle template T=20 μs, and sends the measurement message to N**2** at the start time of a window of the cycle template T.
[0085] In S**808**, N**2** receives the measurement message, records the message receiving time, extracts the cycle template T=20 μs according to the measurement type, and calculates that the offset of the receiving time of the measurement message in the cycle template is α1=15 μs.
[0086] In S**810**, N**2** encapsulates the offset value in the window of the cycle template T into the measurement message and sends the measurement message to N**1** at the start time of a window of the cycle template T.
[0087] In S**812**, N**1** receives the measurement message, records the message receiving time, extracts the cycle template T=20 μs according to the measurement type, and calculates that the offset of the receiving time of the measurement message in the cycle template is α2=5 μs.
[0088] In S**814**, N**1** calculates, based on the cycle template T, α1, and α2, that the phase difference value is Δ=5 μs.
[0089] In S**816**, the process ends.
[0090] The steps of determining the phase difference are described as follows.
[0091] FIG. **9** is a second example diagram of a principle for calculating a phase difference according to an embodiment of this disclosure. As shown in FIG. **9**, since α2<α1, the value of Δ may be (α2−α1+T)/2=5 μs or (α2−α1+2T)/2=15 μs according to formula 1.
[0092] Further, the value range of L corresponding to Δ=5 μs is n*T+20±5 μs (criterion 3), and the value range of L corresponding to Δ=15 μs is n*T+10±5 μs (criterion 4). Since the measured rough value of L is approximately 83 μs, L can be expressed as 3*20+20±3 μs, which falls within the range of n*T+20±5 μs. Therefore, the final value of A is 5 μs.
Example Three
[0093] This example provides a phase difference measurement message encapsulation example. For example, a new sub-TLV called phase-measurement sub-TLV (phase-measurement sub-type length value) can be added to a performance measurement message of an Operations, Administration and Maintenance (OAM) protocol that supports sub-TLV extension. This sub-TLV is used to carry the necessary information for phase difference measurement message. For example,

an OAM performance measurement protocol based on G-Ach is used. The measurement protocol used is not limited in this application.

[0094] FIG. **10** is a diagram of a sub-TLV encapsulation format according to an embodiment of this disclosure. As shown in FIG. **10**, the type field is used for indicating that this sub-TLV is the phase difference measurement type, with the value to be determined. The length field is used for indicating the length of this sub-TLV in units of octets (8-bit bytes) and has a value of 12. The cycle-length field is used for indicating the slot length of the cycle template to be measured, in microseconds, occupying 4 octets. For example, a value of 10 in the cycle-length field indicates that the offset of a 10-μs cycle is to be measured. offset-a1 field is used for indicating that the intra-cycle offset value α1 of the measurement message received by the downstream node, occupying 4 octets. offset-α2 field is used for indicating that the intra-cycle offset measurement value α2 of the returned measurement message received by the upstream node, also occupying 4 octets. α2 may also not be carried in the message, in which case the length field has a length of 8 octets.

[0095] Based on the analysis of the preceding embodiments, the method for determining a phase difference according to this application enables convenient phase difference measurement even in the absence of precise link delay information. The upstream node sends a measurement message to the downstream node at the start time of the cycle window. The downstream node records the position of the measurement message within the cycle window, encapsulates the offset value α1 into the measurement message, and sends the message back to the upstream node at the start time of the cycle window of the downstream node. The upstream node also records the position of the measurement message within the cycle window. Then the upstream node calculates the phase difference value based on the data recorded and carried in the measurement message.

[0096] It is to be noted that the phase difference measurement process and message encapsulation format described in the preceding embodiments are illustrative and do not limit the scope of this application.

[0097] From the description of the preceding embodiments, it is apparent to those skilled in the art that the method in the preceding embodiments may be implemented by software plus a necessary general-purpose hardware platform or may of course be implemented by hardware. However, in many cases, the former is a preferred implementation. Based on this understanding, the solutions provided by this disclosure substantially, or the part contributing to the related art, may be embodied in the form of a software product. The computer software product is stored in a storage medium (such as a ROM/a RAM, a magnetic disk or an optical disk) and includes several instructions for enabling terminal equipment (which may be a mobile phone, a computer, a server, network equipment or the like) to perform the method according to each embodiment of this disclosure.

[0098] An embodiment provides an apparatus for determining a phase difference. The apparatus is configured to implement the previous embodiments and preferred embodiments. What has been described is not repeated. As used below, the term “module” may be software, hardware, or a combination thereof capable of implementing predetermined functions. The apparatus in the embodiment described below is preferably implemented by software, but an implementation by hardware or by a combination of software and hardware is also possible and conceivable.

[0099] FIG. **11** is a block diagram of an apparatus for determining a phase difference according to an embodiment of this disclosure. As shown in FIG. **11**, the apparatus includes a sending module **1102**, a receiving module **1104**, and a determination module **1106**.

[0100] The sending module **1102** is configured to send a first message to a downstream node at a first start time of a window of a predetermined target cycle template, where the first message carries a target slot length of the target cycle template.

[0101] The receiving module **1104** is configured to receive a second message returned by the downstream node at a second start time of a window of the target cycle template, where the second message carries a first offset value, the first offset value is used for indicating an offset of a

receiving time at which the downstream node receives the first message in the target cycle template, and the target slot length is used by the downstream node for determining the target cycle template.

[0102] The determination module **1106** is configured to determine, based on the target slot length, the first offset value, and a second offset value, a phase difference between the target cycle template used by the upstream node and the target cycle template used by the downstream node, where the second offset value is used for indicating an offset of a receiving time at which the upstream node receives the second message in the target cycle template.

[0103] In an example embodiment, the determination module **1106** includes a first determination submodule, a second determination submodule, and a third determination submodule.

[0104] The first determination submodule is configured to determine a second relationship among the phase difference, the target slot length, the first offset value, and the second offset value based on a first relationship between the first offset value and the second offset value.

[0105] The second determination submodule is configured to, in response to determining based on the second relationship that the phase difference has multiple values, determine a respective link delay range corresponding to each value of the phase difference to obtain multiple link delay ranges, where a link delay is a link delay between the upstream node and the downstream node.

[0106] The third determination submodule is configured to determine the unique value of the phase difference based on a third relationship between each link delay range and an estimated delay obtained by pre-estimating the link delay.

[0107] In an example embodiment, the first determination submodule includes at least one of a first determination unit or a second determination unit.

[0108] The first determination unit is configured to, in response to the first relationship indicating that the first offset value is less than or equal to the second offset value, determine that the second relationship satisfies the following formula: 4=(α2+T−α1)/2 or 4=(α2−α1)/2.

[0109] The second determination unit is configured to, in response to the first relationship indicating that the first offset value is greater than the second offset value, determine that the second relationship satisfies the following formula: 4=(α2+T−α1)/2 or 4=(α2+2T−α1)/2.

[0110] Here Δ denotes the phase difference, T denotes the target slot length, α1 denotes the first offset value, and α2 denotes the second offset value.

[0111] In an example embodiment, the second determination submodule is configured to determine the respective link delay range corresponding to each value of the phase difference in at least one of the following manners: in response to the phase difference 4=(α2−α1)/2, determine that the link delay range is

[00016] $n * T + \frac{a1 + a2}{2} \pm \frac{T}{4}$;

in response to the first relationship indicating that the first offset value is less than or equal to the second offset value and in response to the phase difference 4=(α2+T−α1)/2, determine that the link delay range is

[00017] $n * T + \frac{a1 + a2 + T}{2} \pm \frac{T}{4}$;

in response to the first relationship indicating that the first offset value is greater than the second offset value and in response to the phase difference 4=(α2+T−α1)/2, determine that the link delay range is

[00018] $n * T + \frac{a1 + a2 + T}{2} \pm \frac{T}{4}$;

or in response to the phase difference 4=(α2+2T−α1)/2, determine that the link delay range is

[00019] $n * T + \frac{a1 + a2}{2} \pm \frac{T}{4}$.

[0112] Here n is an integer.

[0113] In an example embodiment, the third determination submodule includes a third determination unit and a fourth determination unit.

[0114] The third determination unit is configured to determine a target link delay range from the link delay ranges based on the third relationship, where the target link delay range is a range within

which the estimated delay falls.
[0115] The fourth determination unit is configured to determine the unique value of the phase difference corresponding to the target link delay range.
[0116] In an example embodiment, the first message includes a first type field and a first length field. The first type field is used for indicating that the type of the first message is a type used for measurement of the phase difference. The first length field is used for indicating the target slot length.
[0117] In an example embodiment, the second message includes a second type field, a second length field, and a compensation field. The second type field is used for indicating that the type of the second message is a type used for measurement of the phase difference. The second length field is used for indicating the target slot length. The compensation field is used for indicating the first offset value.
[0118] In an example embodiment, the apparatus also includes at least one of a saving module or an announcing module.
[0119] The saving module is configured to store the phase difference locally in the upstream node after the phase difference between the target cycle template used by the upstream node and the target cycle template used by the downstream node is determined based on the target slot length, the first offset value, and the second offset value.
[0120] The announcing module is configured to announce the phase difference to another network node after the phase difference between the target cycle template used by the upstream node and the target cycle template used by the downstream node is determined based on the target slot length, the first offset value, and the second offset value.
[0121] It is to be noted that the various modules may be implemented by software or hardware. An implementation by hardware may, but may not necessarily, be performed in the following manners: the various modules are located in the same processor, or the various modules are located in their respective processors in any combination form.
[0122] An embodiment of this disclosure also provides a computer-readable storage medium. The storage medium stores a computer program which, when executed by a processor, causes the processor to perform steps of the method of any previous method embodiment.
[0123] In an example embodiment, the storage medium may include, but is not limited to, a U disk, a read-only memory (ROM), a random-access memory (RAM), a mobile hard disk, a magnetic disk, an optical disk, or another medium capable of storing a computer program.
[0124] An embodiment of this disclosure also provides an electronic device. The electronic device includes a memory and a processor. The memory stores a computer program. The processor is configured to execute the computer program to perform steps in any previous method embodiment.
[0125] In an example embodiment, the electronic device may also include a transmission device and an input/output device. Both the transmission device and the input/output device are connected to the processor.
[0126] For examples in this embodiment, reference may be made to the examples described in the preceding embodiments and example embodiments, and the examples are not repeated in this embodiment.
[0127] Apparently, it is to be understood by those skilled in the art that each of the preceding modules or steps of this disclosure may be implemented by a general-purpose computing apparatus, the modules or steps may be concentrated on a single computing apparatus or distributed on a network composed of multiple computing apparatuses, and alternatively, the modules or steps may be implemented by program codes executable by the computing apparatus, so that the modules or steps may be stored in a storage apparatus and executed by the computing apparatus. In some circumstances, the illustrated or described steps may be executed in sequences different from those described herein, or the modules or steps may be made into various integrated circuit modules separately, or multiple modules or steps therein may be made into a single integrated circuit module

for implementation. In this manner, this disclosure is not limited to any particular combination of hardware and software.

[0128] The preceding are preferred embodiments of this disclosure and are not intended to limit this disclosure. For those skilled in the art, embodiments of this disclosure may have various modifications and variations. Any modifications, equivalent substitutions, improvements, and the like within the principle of this disclosure are within the scope of this disclosure.

Claims

1. A method for determining a phase difference, the method being applied to an upstream node and comprising: sending a first message to a downstream node at a first start time of a window of a predetermined target cycle template, wherein the first message carries a target slot length of the target cycle template; receiving a second message returned by the downstream node at a second start time of a window of the target cycle template, wherein the second message carries a first offset value, the first offset value is used for indicating an offset of a receiving time at which the downstream node receives the first message in the target cycle template, and the target slot length is used by the downstream node for determining the target cycle template; and determining, based on the target slot length, the first offset value, and a second offset value, a phase difference between the target cycle template used by the upstream node and the target cycle template used by the downstream node, wherein the second offset value is used for indicating an offset of a receiving time at which the upstream node receives the second message in the target cycle template.

2. The method of claim 1, wherein determining, based on the target slot length, the first offset value, and the second offset value, the phase difference between the target cycle template used by the upstream node and the target cycle template used by the downstream node comprises: determining a second relationship among the phase difference, the target slot length, the first offset value, and the second offset value based on a first relationship between the first offset value and the second offset value; in response to determining based on the second relationship that the phase difference has a plurality of values, determining a respective link delay range corresponding to each of the plurality of values of the phase difference to obtain a plurality of link delay ranges, wherein a link delay is a link delay between the upstream node and the downstream node; and determining a unique value of the phase difference based on a third relationship between each of the plurality of link delay ranges and an estimated delay obtained by pre-estimating the link delay.

3. The method of claim 2, wherein determining the second relationship among the phase difference, the target slot length, the first offset value, and the second offset value based on the first relationship between the first offset value and the second offset value comprises at least one of the following: in response to the first relationship indicating that the first offset value is less than or equal to the second offset value, determining that the second relationship satisfies the following formula: $\Delta=(\alpha2+T-\alpha1)/2$ or $\Delta=(\alpha2-\alpha1)/2$; or in response to the first relationship indicating that the first offset value is greater than the second offset value, determining that the second relationship satisfies the following formula: $\Delta=(\alpha2+T-\alpha1)/2$ or $\Delta=(\alpha2+2T-\alpha1)/2$; wherein Δ denotes the phase difference, T denotes the target slot length, $\alpha1$ denotes the first offset value, and $\alpha2$ denotes the second offset value.

4. The method of claim 3, wherein determining the respective link delay range corresponding to each of the plurality of values of the phase difference comprises at least one of the following: in response to the phase difference $\Delta=(\alpha2-\alpha1)/2$, determining that the link delay range is $n*T+\frac{a1+a2}{2}\pm\frac{T}{4}$; in response to the first relationship indicating that the first offset value is less than or equal to the second offset value and in response to the phase difference $\Delta=(\alpha2+T-\alpha1)/2$, determining that the link delay range is $n*T+\frac{a1+a2+T}{2}\pm\frac{T}{4}$; in response to the first relationship indicating that the first offset value is greater than the second offset value and in response to the phase difference $\Delta=(\alpha2+T-\alpha1)/2$, determining that the link delay range is $n*T+\frac{a1+a2+T}{2}\pm\frac{T}{4}$; or

in response to the phase difference Δ=(α2+2T−α1)/2, determining that the link delay range is $n * T + \frac{a1 + a2}{2} \pm \frac{T}{4}$; wherein n is an integer.

5. The method of claim 2, wherein determining the unique value of the phase difference based on the third relationship between each of the plurality of link delay ranges and the estimated delay obtained by pre-estimating the link delay comprises: determining a target link delay range from the plurality of link delay ranges based on the third relationship, wherein the target link delay range is a range within which the estimated delay falls; and determining the unique value of the phase difference corresponding to the target link delay range.

6. The method of claim 1, wherein the first message comprises a first type field and a first length field, wherein the first type field is used for indicating that a type of the first message is a type used for measurement of the phase difference, and the first length field is used for indicating the target slot length.

7. The method of claim 1, wherein the second message comprises a second type field, a second length field, and a compensation field, wherein the second type field is used for indicating that a type of the second message is a type used for measurement of the phase difference, the second length field is used for indicating the target slot length, and the compensation field is used for indicating the first offset value.

8. The method of claim 1, after determining, based on the target slot length, the first offset value, and the second offset value, the phase difference between the target cycle template used by the upstream node and the target cycle template used by the downstream node, the method further comprising at least one of the following: saving the phase difference locally in the upstream node; or announcing the phase difference to another network node.

9. (canceled)

10. A non-transitory computer-readable storage medium storing a computer program which, when executed by a processor, causes the processor to perform: sending a first message to a downstream node at a first start time of a window of a predetermined target cycle template, wherein the first message carries a target slot length of the target cycle template; receiving a second message returned by the downstream node at a second start time of a window of the target cycle template, wherein the second message carries a first offset value, the first offset value is used for indicating an offset of a receiving time at which the downstream node receives the first message in the target cycle template, and the target slot length is used by the downstream node for determining the target cycle template; and determining, based on the target slot length, the first offset value, and a second offset value, a phase difference between the target cycle template used by the upstream node and the target cycle template used by the downstream node, wherein the second offset value is used for indicating an offset of a receiving time at which the upstream node receives the second message in the target cycle template.

11. An electronic device, comprising a memory, a processor, and a computer program stored in the memory and executable on the processor, wherein when executing the computer program, the processor is configured to: send a first message to a downstream node at a first start time of a window of a predetermined target cycle template, wherein the first message carries a target slot length of the target cycle template; receive a second message returned by the downstream node at a second start time of a window of the target cycle template, wherein the second message carries a first offset value, the first offset value is used for indicating an offset of a receiving time at which the downstream node receives the first message in the target cycle template, and the target slot length is used by the downstream node for determining the target cycle template; and determine, based on the target slot length, the first offset value, and a second offset value, a phase difference between the target cycle template used by the upstream node and the target cycle template used by the downstream node, wherein the second offset value is used for indicating an offset of a receiving time at which the upstream node receives the second message in the target cycle template.

12. The non-transitory computer-readable storage medium of claim 10, wherein determining, based

on the target slot length, the first offset value, and the second offset value, the phase difference between the target cycle template used by the upstream node and the target cycle template used by the downstream node comprises: determining a second relationship among the phase difference, the target slot length, the first offset value, and the second offset value based on a first relationship between the first offset value and the second offset value; in response to determining based on the second relationship that the phase difference has a plurality of values, determining a respective link delay range corresponding to each of the plurality of values of the phase difference to obtain a plurality of link delay ranges, wherein a link delay is a link delay between the upstream node and the downstream node; and determining a unique value of the phase difference based on a third relationship between each of the plurality of link delay ranges and an estimated delay obtained by pre-estimating the link delay.

13. The non-transitory computer-readable storage medium of claim 12, wherein determining the second relationship among the phase difference, the target slot length, the first offset value, and the second offset value based on the first relationship between the first offset value and the second offset value comprises at least one of the following: in response to the first relationship indicating that the first offset value is less than or equal to the second offset value, determining that the second relationship satisfies the following formula: = ($a2 + T - a1$) / 2or = ($a2 - a1$) / 2; or in response to the first relationship indicating that the first offset value is greater than the second offset value, determining that the second relationship satisfies the following formula: Δ= ($a2 + T - a1$) / 2or = ($a2 + 2T - a1$) / 2; wherein Δ denotes the phase difference, T denotes the target slot length, α1 denotes the first offset value, and α2 denotes the second offset value.

14. The non-transitory computer-readable storage medium of claim 13, wherein determining the respective link delay range corresponding to each of the plurality of values of the phase difference comprises at least one of the following: in response to the phase difference Δ=(α2−α1)/2, determining that the link delay range is $n * T + \frac{a1 + a2}{2} \pm \frac{T}{4}$; in response to the first relationship indicating that the first offset value is less than or equal to the second offset value and in response to the phase difference Δ=(α2+T−α1)/2, determining that the link delay range is $n * T + \frac{a1 + a2 + T}{2} \pm \frac{T}{4}$; in response to the first relationship indicating that the first offset value is greater than the second offset value and in response to the phase difference Δ=(α2+T−α1)/2, determining that the link delay range is or $n * T + \frac{a1 + a2 + T}{2} \pm \frac{T}{4}$; in response to the phase difference Δ=(α2+2T−α1)/2, determining that the link delay range is $n * T + \frac{a1 + a2}{2} \pm \frac{T}{4}$; wherein n is an integer.

15. The non-transitory computer-readable storage medium of claim 12, wherein determining the unique value of the phase difference based on the third relationship between each of the plurality of link delay ranges and the estimated delay obtained by pre-estimating the link delay comprises: determining a target link delay range from the plurality of link delay ranges based on the third relationship, wherein the target link delay range is a range within which the estimated delay falls; and determining the unique value of the phase difference corresponding to the target link delay range.

16. The non-transitory computer-readable storage medium of claim 10, wherein the first message comprises a first type field and a first length field, wherein the first type field is used for indicating that a type of the first message is a type used for measurement of the phase difference, and the first length field is used for indicating the target slot length; and the second message comprises a second type field, a second length field, and a compensation field, wherein the second type field is used for indicating that a type of the second message is a type used for measurement of the phase difference, the second length field is used for indicating the target slot length, and the compensation field is used for indicating the first offset value.

17. The electronic device of claim 11, wherein when executing the computer program, the processor is further configured to: determine a second relationship among the phase difference, the target slot length, the first offset value, and the second offset value based on a first relationship

between the first offset value and the second offset value; in response to determining based on the second relationship that the phase difference has a plurality of values, determine a respective link delay range corresponding to each of the plurality of values of the phase difference to obtain a plurality of link delay ranges, wherein a link delay is a link delay between the upstream node and the downstream node; and determine a unique value of the phase difference based on a third relationship between each of the plurality of link delay ranges and an estimated delay obtained by pre-estimating the link delay.

18. The electronic device of claim 17, wherein when executing the computer program, the processor is further configured to perform at least one of the following: in response to the first relationship indicating that the first offset value is less than or equal to the second offset value, determining that the second relationship satisfies the following formula:

$= (a2 + T - a1) / 2$or $= (a2 - a1) / 2$; or in response to the first relationship indicating that the first offset value is greater than the second offset value, determining that the second relationship satisfies the following formula: $\Delta = (a2 + T - a1) / 2$or $= (a2 + 2T - a1) / 2$; wherein Δ denotes the phase difference, T denotes the target slot length, α1 denotes the first offset value, and α2 denotes the second offset value.

19. The electronic device of claim 18, wherein when executing the computer program, the processor is configured to perform at least one of the following: in response to the phase difference Δ=(α2−α1)/2, determining that the link delay range is $n * T + \frac{a1 + a2}{2} \pm \frac{T}{4}$; in response to the first relationship indicating that the first offset value is less than or equal to the second offset value and in response to the phase difference Δ=(α2+T−α1)/2, determining that the link delay range is $n * T + \frac{a1 + a2 + T}{2} \pm \frac{T}{4}$; in response to the first relationship indicating that the first offset value is greater than the second offset value and in response to the phase difference Δ=(α2+T−α1)/2, determining that the link delay range is $n * T + \frac{a1 + a2 + T}{2} \pm \frac{T}{4}$; or in response to the phase difference Δ=(α2+2T−α1)/2, determining that the link delay range is $n * T + \frac{a1 + a2}{2} \pm \frac{T}{4}$; wherein n is an integer.

20. The electronic device of claim 17, wherein when executing the computer program, the processor is further configured to: determine a target link delay range from the plurality of link delay ranges based on the third relationship, wherein the target link delay range is a range within which the estimated delay falls; and determine the unique value of the phase difference corresponding to the target link delay range.

21. The electronic device of claim 11, wherein the first message comprises a first type field and a first length field, wherein the first type field is used for indicating that a type of the first message is a type used for measurement of the phase difference, and the first length field is used for indicating the target slot length; and the second message comprises a second type field, a second length field, and a compensation field, wherein the second type field is used for indicating that a type of the second message is a type used for measurement of the phase difference, the second length field is used for indicating the target slot length, and the compensation field is used for indicating the first offset value.