United States Patent Application Publication	20250258562
Kind Code	A1
Publication Date	August 14, 2025
Inventor(s)	KIM; HYUNGBAE

ELECTRONIC DEVICE

Abstract

An electronic device includes a sensor layer including a sensing region, a peripheral region, first electrode groups in a first direction, second electrode groups crossing the first electrode groups in a second direction, first trace lines electrically connected to the first electrode groups, and second trace lines electrically connected to the second electrode groups, and including a (2-1)-th trace line electrically connected to one of the second electrode groups, and having a first length in the second direction, and a (2-2)-th trace line spaced apart from the (2-1)-th trace line in the first direction while extending in the second direction, and having a second length in the second direction that is substantially equal to the first length, and a sensor driver configured to drive the sensor layer, and to selectively operate in a first mode for sensing a touch input, or in a second mode for sensing a pen input.

Inventors: **KIM; HYUNGBAE (Yongin-si, KR)**

Applicant: **Samsung Display Co., Ltd.** (Yongin-si, KR)

Family ID: **96614490**

Appl. No.: **18/986142**

Filed: **December 18, 2024**

Foreign Application Priority Data

KR	10-2024-0019406	Feb. 08, 2024

Publication Classification

Int. Cl.: **G06F3/041** (20060101); **G06F3/044** (20060101)

U.S. Cl.:

CPC **G06F3/04164** (20190501); G06F3/0446 (20190501); G06F2203/04111 (20130101); G06F2203/04112 (20130101); G06F2203/04114 (20190501)

Background/Summary

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application claims priority to, and the benefit of, Korean Patent Application No. 10-2024-0019406, filed on Feb. 8, 2024, in the Korean Intellectual Property Office, the entire disclosure of which is incorporated herein by reference.

BACKGROUND

[0002] Embodiments of the present disclosure described herein relate to an electronic device capable of sensing an input made by a pen.

[0003] Multimedia electronic devices, such as a television (TV), a cellular phone, a tablet computer, a laptop computer, a navigation, or a game console, include a display device that displays an image. Electronic devices may include an sensor layer (or an input sensor) that provides a touch-based input manner for enabling a user to intuitively, conveniently, and easily input information or a command, in addition to a general input manner, such as a button, a keyboard, or a mouse. The sensor layer may sense a touch or an input of a user. Meanwhile, the demand for using a pen is increased for a user familiar with the input of information through handwriting or for a fine touch input for a corresponding application program (for example, an application program for sketching or drawing).

SUMMARY

[0004] Embodiments of the present disclosure provide an electronic device capable of sensing an input made by a pen.

[0005] According to one or more embodiments, an electronic device may include a sensor layer including a sensing region, a peripheral region adjacent to the sensing region, first electrode groups arranged in a first direction, second electrode groups crossing the first electrode groups, and arranged in a second direction crossing the first direction, first trace lines electrically connected to the first electrode groups, and second trace lines electrically connected to the second electrode groups, and including a (2-1)-th trace line electrically connected to one of the second electrode groups, and having a first length in the second direction, and a (2-2)-th trace line spaced apart from the (2-1)-th trace line in the first direction while extending in the second direction, and having a second length in the second direction that is substantially equal to the first length, and a sensor driver configured to drive the sensor layer, and to selectively operate in a first mode for sensing a touch input, or in a second mode for sensing a pen input.

[0006] Each of the second electrode groups may include a first divided electrode, and a second divided electrode spaced apart from the first divided electrode in the first direction, wherein the (2-1)-th trace line is electrically connected to the first divided electrode, and the (2-2)-th trace line is electrically connected to the second divided electrode.

[0007] At least a portion of the (2-1)-th trace line and a portion of the (2-2)-th trace line may overlap the sensing region, wherein the first length of the (2-1)-th trace line overlaps the sensing region, and wherein the second length of the (2-2)-th trace line overlaps the sensing region.

[0008] The (2-1)-th trace line may be connected to the first divided electrode adjacent to the second divided electrode, wherein the (2-2)-th trace line is connected to the second divided electrode adjacent to the first divided electrode.

[0009] The (2-1)-th trace line and the (2-2)-th trace line may overlap the peripheral region, and may be spaced apart from each other with the first divided electrode and the second divided electrode therebetween.

[0010] The second electrode groups may include a (2-1)-th electrode group, a (2-2)-th electrode group, and a (2-3)-th electrode group sequentially arranged in the second direction, wherein the (2-1)-th electrode group includes a (1-1)-th divided electrode, and a (2-1)-th divided electrode spaced apart from the (1-1)-th divided electrode in the first direction, wherein the (2-2)-th electrode group includes a (1-2)-th divided electrode, and a (2-2)-th divided electrode spaced apart from the (1-2)-th divided electrode in the first direction, wherein the (2-3)-th electrode group includes a (1-3)-th divided electrode, and a (2-3)-th divided electrode spaced apart from the (1-3)-th divided electrode in the first direction, and wherein the second trace lines includes a (1-1)-th divided trace line electrically connected to the (1-1)-th divided electrode, a (2-1)-th divided trace line electrically connected to the (2-1)-th divided electrode, a (1-2)-th divided trace line electrically connected to the (1-2)-th divided electrode, a (2-2)-th divided trace line electrically connected to the (2-2)-th divided electrode, a (1-3)-th divided trace line electrically connected to the (1-3)-th divided electrode, and a (2-3)-th divided trace line electrically connected to the (2-3)-th divided electrode.
[0011] A gap between the (1-1)-th divided trace line and the (2-1)-th divided trace line may be narrower than a gap between the (2-1)-th divided trace line and the (1-2)-th divided trace line.
[0012] The (1-1)-th divided trace line, the (2-1)-th divided trace line, the (1-2)-th divided trace line, the (2-2)-th divided trace line, the (1-3)-th divided trace line, and the (2-3)-th divided trace line may be sequentially arranged in the first direction.
[0013] The (1-3)-th divided trace line, the (2-3)-th divided trace line, the (1-1)-th divided trace line, the (2-1)-th divided trace line, the (1-2)-th divided trace line, and the (2-2)-th divided trace line may be sequentially arranged in the first direction.
[0014] A width of the (1-1)-th divided electrode in the first direction may be narrower than a width of the (1-2)-th divided electrode in the first direction, wherein a width of the (2-1)-th divided electrode in the first direction is wider than a width of the (2-2)-th divided electrode in the first direction.
[0015] A width of the (1-3)-th divided electrode in the first direction may be wider than the width of the (1-2)-th divided electrode in the first direction, wherein a width of the (2-3)-th divided electrode in the first direction is narrower than the width of the (2-2)-th divided electrode in the first direction.
[0016] A width of the (1-3)-th divided electrode in the first direction may be narrower than the width of the (1-1)-th divided electrode in the first direction, wherein a width of the (2-3)-th divided electrode in the first direction is wider than the width of the (2-1)-th divided electrode in the first direction.
[0017] A gap between the (1-3)-th divided electrode and the (2-3)-th divided electrode may overlap the (2-1)-th divided electrode and the (2-2)-th divided electrode, when viewed from the second direction.
[0018] A gap between the (1-3)-th divided electrode and the (2-3)-th divided electrode may overlap the (1-1)-th divided electrode and the (1-2)-th divided electrode, when viewed from the second direction.
[0019] The (2-1)-th trace line may include a first portion extending in the first direction, and a second portion extending in the second direction from the first portion, wherein the (2-2)-th trace line faces the second portion.
[0020] The sensor driver may be configured to receive a first signal through the (2-1)-th trace line and a second signal through the (2-2)-th trace line, and to generate first data by performing a differential computing operation with respect to the first signal and the second signal.
[0021] The second trace lines may include a (2-3)-th trace line electrically connected to another second electrode group among the second electrode groups, and a (2-4)-th trace line spaced apart from the (2-3)-th trace line in the first direction while extending in the second direction, wherein the sensor driver is configured to receive a third signal through the (2-3)-th trace line and a fourth signal through the (2-4)-th trace line, to generate second data by performing a differential

computing operation with respect to the third signal and the fourth signal, and to generate third data by performing the differential computing operation with respect to the first data and the second data.

[0022] The sensor driver may be configured to generate the first data and the second data through at least one of analog differential processing or digital differential processing, wherein the sensor driver is configured to generate the third data through at least one of the analog differential processing or the digital differential processing.

[0023] According to one or more embodiments, an electronic device may include a sensor layer including a sensing region, a peripheral region adjacent to the sensing region, first electrode groups in the sensing region and arranged in a first direction, second electrode groups in the sensing region, and arranged in a second direction crossing the first direction, while crossing the first electrode groups, a first line electrically connected to one of the second electrode groups, a second line having a length substantially equal to a length of the first line in the second direction, in the sensing region, a third line electrically connected to another of the second electrode groups, and a fourth line having a length substantially equal to a length of the third line in the second direction, in the sensing region, and a sensor driver configured to drive the sensor layer, configured to selectively operate in a first mode for sensing a touch input or in a second mode for sensing a pen input, configured to receive a first signal through the first line and a second signal through the second line, configured to generate first data by performing a differential computing operation with respect to the first signal and the second signal, configured to receive a third signal through the third line and a fourth signal through the fourth line, configured to generate second data by performing a differential computing operation with respect to the third signal and the fourth signal, and configured to generate third data by performing a differential computing operation with respect to the first data and the second data.

[0024] The one of the second electrode groups may include a first divided electrode, and a second divided electrode spaced apart from the first divided electrode in the first direction, wherein the another of the second electrode groups includes a third divided electrode, and a fourth divided electrode spaced apart from the third divided electrode in the first direction, wherein the first line is electrically connected to the first divided electrode, and the second line is electrically connected to the second divided electrode, and wherein the third line is electrically connected to the third divided electrode, and the fourth line is electrically connected to the fourth divided electrode.

[0025] The first line and the second line may be insulated from one of the third divided electrode or the fourth divided electrode while crossing the third divided electrode and the fourth divided electrode.

[0026] The first line may include a first portion extending in the first direction, and a second portion extending in the second direction from the first portion, wherein the second line faces the second portion of the first line.

[0027] The sensor driver may be connected to one end of the second line, and an opposite end of the second line is floated.

[0028] According to one or more embodiments, an electronic device may include a first electrode groups in a sensing region, and arranged in a first direction, second electrode groups crossing the first electrode groups in the sensing region, and arranged in a second direction crossing the first direction, a first line in the sensing region, and electrically connected to one of the second electrode groups, a second line in the sensing region, and adjacent to the first line in the first direction, and a third line in the sensing region, and electrically connected to another of the second electrode groups, wherein a gap between the first line and the second line is narrower than a gap between the second line and the third line, and wherein a length of a portion of the first line in the sensing region is substantially equal to a length of a portion of the second line in the sensing region.

[0029] The one of the second electrode groups may include a first divided electrode, and a second divided electrode spaced apart from the first divided electrode in the first direction, wherein the

first line is electrically connected to the first divided electrode, and the second line is electrically connected to the second divided electrode.
[0030] The first line may include a first portion extending in the first direction, and a second portion extending in the second direction from the first portion, wherein the second line faces the second portion of the first line while extending in the second direction.

Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0031] The above and other aspects of the present disclosure will become apparent by describing in detail embodiments thereof with reference to the accompanying drawings.
[0032] FIG. **1**A is a perspective view illustrating an electronic device according to one or more embodiments of the present disclosure.
[0033] FIG. **1**B is a bottom perspective view illustrating an electronic device according to one or more embodiments of the present disclosure.
[0034] FIG. **2** is a perspective view illustrating an electronic device according to one or more embodiments of the present disclosure.
[0035] FIG. **3** is a perspective view of an electronic device according to one or more embodiments of the present disclosure.
[0036] FIG. **4** is a cross-sectional view schematically illustrating a display panel according to one or more embodiments of the present disclosure.
[0037] FIG. **5** is a view illustrating an operation of an electronic device according to one or more embodiments.
[0038] FIG. **6**A is a cross-sectional view of a display panel according to one or more embodiments of the present disclosure.
[0039] FIG. **6**B is a cross-sectional view of a sensor layer according to one or more embodiments of the present disclosure.
[0040] FIG. **7** is a plan view of a sensor layer according to one or more embodiments of the present disclosure.
[0041] FIG. **8** is an enlarged plan view illustrating one sensing unit according to one or more embodiments of the present disclosure.
[0042] FIG. **9**A is a plan view illustrating a first conductive layer of a sensing unit according to one or more embodiments of the present disclosure.
[0043] FIG. **9**B is a plan view illustrating a second conductive layer of a sensing unit according to one or more embodiments of the present disclosure.
[0044] FIG. **9**C is a cross-sectional view of a sensor layer according to one or more embodiments of the present disclosure, which is taken along the line I-I′ shown in FIGS. **9**A and **9**B, respectively.
[0045] FIG. **10**A is a plan view illustrating a first conductive layer of a sensing unit according to one or more embodiments of the present disclosure.
[0046] FIG. **10**B is a plan view illustrating a second conductive layer of a sensing unit according to one or more embodiments of the present disclosure.
[0047] FIG. **10**C is a cross-sectional view of a sensor layer taken along the line II-II′ illustrated in FIGS. **10**A and **10**B according to one or more embodiments of the present disclosure.
[0048] FIG. **11**A is an enlarged plan view of region AA′ illustrated in FIG. **9**A.
[0049] FIG. **11**B is an enlarged plan view of region BB′ illustrated in FIG. **9**B.
[0050] FIG. **12** is a plan view of a sensor layer according to one or more embodiments of the present disclosure.
[0051] FIG. **13**A is a view illustrating an operation of a sensor driver according to one or more embodiments of the present disclosure.

[0052] FIG. **13**B is a view illustrating an operation of a sensor driver according to one or more embodiments of the present disclosure.
[0053] FIG. **14** is a view illustrating a first mode, according to one or more embodiments of the present disclosure.
[0054] FIG. **15** is a view illustrating a second mode according to one or more embodiments of the present disclosure
[0055] FIG. **16**A is a graph illustrating a waveform of a first signal according to one or more embodiments of the present disclosure.
[0056] FIG. **16**B is a graph illustrating a waveform of a second signal according to one or more embodiments of the present disclosure.
[0057] FIG. **17**A is a view illustrating a second mode according to one or more embodiments of the present disclosure.
[0058] FIG. **17**B is a view illustrating a second mode according to one or more embodiments of the present disclosure.
[0059] FIG. **18**A is a view illustrating some components of a sensor layer according to one or more embodiments of the present disclosure.
[0060] FIG. **18**B is an equivalent circuit diagram of an input device and a sensor layer according to one or more embodiments of the present disclosure;
[0061] FIG. **19** is a view illustrating a sensor driver according to one or more embodiments of the present disclosure;
[0062] FIG. **20** is a view illustrating a sensor driver according to one or more embodiments of the present disclosure;
[0063] FIG. **21** is a view illustrating a sensor driver according to one or more embodiments of the present disclosure;
[0064] FIG. **22**A is a plan view of a sensor layer according to one or more embodiments of the present disclosure.
[0065] FIG. **22**B is a view illustrating some components of a sensor layer according to one or more embodiments of the present disclosure.
[0066] FIG. **23** is a plan view of a sensor layer according to one or more embodiments of the present disclosure.
[0067] FIG. **24**A is a view illustrating some components of a sensor layer according to one or more embodiments of the present disclosure.
[0068] FIG. **24**B is a view illustrating a sensing unit in a second mode according to one or more embodiments of the present disclosure.
[0069] FIG. **25** is a plan view of a sensor layer according to one or more embodiments of the present disclosure.

DETAILED DESCRIPTION

[0070] Aspects of some embodiments of the present disclosure and methods of accomplishing the same may be understood more readily by reference to the detailed description of embodiments and the accompanying drawings. The described embodiments are provided as examples so that this disclosure will be thorough and complete, and will fully convey the aspects of the present disclosure to those skilled in the art. Accordingly, processes, elements, and techniques that are redundant, that are unrelated or irrelevant to the description of the embodiments, or that are not necessary to those having ordinary skill in the art for a complete understanding of the aspects of the present disclosure may be omitted. Unless otherwise noted, like reference numerals, characters, or combinations thereof denote like elements throughout the attached drawings and the written description, and thus, repeated descriptions thereof may be omitted.
[0071] The described embodiments may have various modifications and may be embodied in different forms, and should not be construed as being limited to only the illustrated embodiments herein. The use of “can,” “may,” or “may not” in describing an embodiment corresponds to one or

more embodiments of the present disclosure.
[0072] A person of ordinary skill in the art would appreciate, in view of the present disclosure in its entirety, that each suitable feature of the various embodiments of the present disclosure may be combined or combined with each other, partially or entirely, and may be technically interlocked and operated in various suitable ways, and each embodiment may be implemented independently of each other or in conjunction with each other in any suitable manner unless otherwise stated or implied.
[0073] In the drawings, the relative sizes of elements, layers, and regions may be exaggerated for clarity and/or descriptive purposes. In other words, because the sizes and thicknesses of elements in the drawings are arbitrarily illustrated for convenience of description, the disclosure is not limited thereto. Additionally, the use of cross-hatching and/or shading in the accompanying drawings is generally provided to clarify boundaries between adjacent elements. As such, neither the presence nor the absence of cross-hatching or shading conveys or indicates any preference or requirement for particular materials, material properties, dimensions, proportions, commonalities between illustrated elements, and/or any other characteristic, attribute, property, etc., of the elements, unless specified.
[0074] Various embodiments are described herein with reference to sectional illustrations that are schematic illustrations of embodiments and/or intermediate structures. As such, variations from the shapes of the illustrations as a result of, for example, manufacturing techniques and/or tolerances, are to be expected. Further, specific structural or functional descriptions disclosed herein are merely illustrative for the purpose of describing embodiments according to the concept of the present disclosure. Thus, embodiments disclosed herein should not be construed as limited to the illustrated shapes of elements, layers, or regions, but are to include deviations in shapes that result from, for instance, manufacturing.
[0075] For example, an implanted region illustrated as a rectangle will, typically, have rounded or curved features and/or a gradient of implant concentration at its edges rather than a binary change from implanted to non-implanted region. Likewise, a buried region formed by implantation may result in some implantation in the region between the buried region and the surface through which the implantation takes place.
[0076] Spatially relative terms, such as “beneath,” “below,” “lower,” “lower side,” “under,” “above,” “upper,” “over,” “higher,” “upper side,” “side” (e.g., as in “sidewall”), and the like, may be used herein for ease of explanation to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or in operation, in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as “below,” “beneath,” “or “under” other elements or features would then be oriented “above” the other elements or features. Thus, the example terms “below” and “under” can encompass both an orientation of above and below. The device may be otherwise oriented (e.g., rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein should be interpreted accordingly. Similarly, when a first part is described as being arranged “on” a second part, this indicates that the first part is arranged at an upper side or a lower side of the second part without the limitation to the upper side thereof on the basis of the gravity direction.
[0077] Further, the phrase “in a plan view” means when an object portion is viewed from above, and the phrase “in a schematic cross-sectional view” means when a schematic cross-section taken by vertically cutting an object portion is viewed from the side. The terms “overlap” or “overlapped” mean that a first object may be above or below or to a side of a second object, and vice versa. Additionally, the term “overlap” may include stack, face or facing, extending over, covering, or partly covering or any other suitable term as would be appreciated and understood by those of ordinary skill in the art. The expression “not overlap” may include meaning, such as “apart from” or “set aside from” or “offset from” and any other suitable equivalents as would be

appreciated and understood by those of ordinary skill in the art. The terms “face” and “facing” may mean that a first object may directly or indirectly oppose a second object. In a case in which a third object intervenes between a first and second object, the first and second objects may be understood as being indirectly opposed to one another, although still facing each other.

[0078] It will be understood that when an element, layer, region, or component is referred to as being “formed on,” “on,” “connected to,” or “(operatively or communicatively) coupled to” another element, layer, region, or component, it can be directly formed on, on, connected to, or coupled to the other element, layer, region, or component, or indirectly formed on, on, connected to, or coupled to the other element, layer, region, or component such that one or more intervening elements, layers, regions, or components may be present. In addition, this may collectively mean a direct or indirect coupling or connection and an integral or non-integral coupling or connection. For example, when a layer, region, or component is referred to as being “electrically connected” or “electrically coupled” to another layer, region, or component, it can be directly electrically connected or coupled to the other layer, region, and/or component or one or more intervening layers, regions, or components may be present. The one or more intervening components may include a switch, a resistor, a capacitor, and/or the like. In describing embodiments, an expression of connection indicates electrical connection unless explicitly described to be direct connection, and “directly connected/directly coupled,” or “directly on,” refers to one component directly connecting or coupling another component, or being on another component, without an intermediate component.

[0079] In addition, in the present specification, when a portion of a layer, a film, an area, a plate, or the like is formed on another portion, a forming direction is not limited to an upper direction but includes forming the portion on a side surface or in a lower direction. On the contrary, when a portion of a layer, a film, an area, a plate, or the like is formed “under” another portion, this includes not only a case where the portion is “directly beneath” another portion but also a case where there is further another portion between the portion and another portion. Meanwhile, other expressions describing relationships between components, such as “between,” “immediately between” or “adjacent to” and “directly adjacent to,” may be construed similarly. It will be understood that when an element or layer is referred to as being “between” two elements or layers, it can be the only element or layer between the two elements or layers, or one or more intervening elements or layers may also be present.

[0080] For the purposes of this disclosure, expressions such as “at least one of,” or “any one of,” or “one or more of” when preceding a list of elements, modify the entire list of elements and do not modify the individual elements of the list. For example, “at least one of X, Y, and Z,” “at least one of X, Y, or Z,” “at least one selected from the group consisting of X, Y, and Z,” and “at least one selected from the group consisting of X, Y, or Z” may be construed as X only, Y only, Z only, any combination of two or more of X, Y, and Z, such as, for instance, XYZ, XYY, YZ, and ZZ, or any variation thereof. Similarly, the expressions “at least one of A and B” and “at least one of A or B” may include A, B, or A and B. As used herein, “or” generally means “and/or,” and the term “and/or” includes any and all combinations of one or more of the associated listed items. For example, the expression “A and/or B” may include A, B, or A and B. Similarly, expressions such as “at least one of,” “a plurality of,” “one of,” and other prepositional phrases, when preceding a list of elements, modify the entire list of elements and do not modify the individual elements of the list. When “C to D” is stated, it means C or more and D or less, unless otherwise specified.

[0081] It will be understood that, although the terms “first,” “second,” “third,” etc., may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms do not correspond to a particular order, position, or superiority, and are used only used to distinguish one element, member, component, region, area, layer, section, or portion from another element, member, component, region, area, layer, section, or portion. Thus, a first element, component,

region, layer or section described below could be termed a second element, component, region, layer or section, without departing from the spirit and scope of the present disclosure. The description of an element as a “first” element may not require or imply the presence of a second element or other elements. The terms “first,” “second,” etc. may also be used herein to differentiate different categories or sets of elements. For conciseness, the terms “first,” “second,” etc. may represent “first-category (or first-set),” “second-category (or second-set),” etc., respectively.

[0082] In the examples, the x-axis, the y-axis, and/or the z-axis are not limited to three axes of a rectangular coordinate system, and may be interpreted in a broader sense. For example, the x-axis, the y-axis, and the z-axis may be perpendicular to one another, or may represent different directions that are not perpendicular to one another. The same applies for first, second, and/or third directions.

[0083] The terminology used herein is for the purpose of describing embodiments only and is not intended to be limiting of the present disclosure. As used herein, the singular forms “a” and “an” are intended to include the plural forms as well, while the plural forms are also intended to include the singular forms, unless the context clearly indicates otherwise. It will be further understood that the terms “comprises,” “comprising,” “have,” “having,” “includes,” and “including,” when used in this specification, specify the presence of the stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0084] As used herein, the terms “substantially,” “about,” “approximately,” and similar terms are used as terms of approximation and not as terms of degree, and are intended to account for the inherent deviations in measured or calculated values that would be recognized by those of ordinary skill in the art. For example, “substantially” may include a range of +/−5% of a corresponding value. “About” or “approximately,” as used herein, is inclusive of the stated value and means within an acceptable range of deviation for the particular value as determined by one of ordinary skill in the art, considering the measurement in question and the error associated with measurement of the particular quantity (i.e., the limitations of the measurement system). For example, “about” may mean within one or more standard deviations, or within +30%, 20%, 10%, 5% of the stated value. Further, the use of “may” when describing embodiments of the present disclosure refers to “one or more embodiments of the present disclosure.”

[0085] The terms “part” and “unit” refer to a software component or a hardware component to perform a corresponding function. The electronic or electric devices and/or any other relevant devices or components according to embodiments of the present disclosure described herein may be implemented utilizing any suitable hardware, firmware (e.g., an application-specific integrated circuit), software, or a combination of software, firmware, and hardware, to process data or digital signals. For example, the various components of these devices may be formed on one integrated circuit (IC) chip or on separate IC chips. Further, the various components of these devices may be implemented on a flexible printed circuit film, a tape carrier package (TCP), a printed circuit board (PCB), or formed on one substrate. Circuit hardware may include, for example, application specific integrated circuits (ASICs), general purpose or special purpose central processing units (CPUs) that is configured to execute instructions stored in a non-transitory storage medium, digital signal processors (DSPs), graphics processing units (GPUs), and programmable logic devices, such as field programmable gate arrays (FPGAs).

[0086] Software components may indicate data used by executable codes and/or executable codes in a storage medium which is able to be addressed. Accordingly, software components may be, for example, object-oriented software components, class components, and task components, and may include processes, functions, properties, procedures, subroutines, program code segments, drivers, firmware, microcodes, circuits, data, database, data structures, tables, arrangements or variables. Further, the various components of these devices may be a process or thread, running on one or more processors, in one or more computing devices, executing computer program instructions and interacting with other system components for performing the various functionalities described

herein. The computer program instructions are stored in a memory that may be implemented in a computing device using a standard memory device, such as, for example, a random-access memory (RAM). The computer program instructions may also be stored in other non-transitory computer readable media such as, for example, a CD-ROM, flash drive, or the like. Also, a person of skill in the art should recognize that the functionality of various computing devices may be combined or integrated into a single computing device, or the functionality of a particular computing device may be distributed across one or more other computing devices without departing from the spirit and scope of the embodiments of the present disclosure.

[0087] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which the present disclosure belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and/or the present specification, and should not be interpreted in an idealized or overly formal sense, unless expressly so defined herein.

[0088] Hereinafter, embodiments of the present disclosure will be described with reference to accompanying drawings.

[0089] FIG. **1**A is a perspective view of an electronic device **1000** according to one or more embodiments of the present disclosure. FIG. **1**B is a bottom perspective view of the electronic device **1000** according to one or more embodiments of the present disclosure.

[0090] Referring to FIGS. **1**A and **1**B, the electronic device **1000** may be a device activated in response to an electrical signal. For example, the electronic device **1000** may display an image and sense inputs applied from the outside. The external input may be a user input. The input of the user may include any one of various external inputs, such as a part of a physical body of the user, a pen, light, heat, or pressure.

[0091] The electronic device **1000** may include a first display panel DP**1** and a second display panel DP**2**. The first display panel DP**1** and the second display panel DP**2** may be separated from each other. The first display panel DP**1** may be referred to as a main display panel, and the second display panel DP**2** may be an auxiliary display panel or an external display panel.

[0092] The first display panel DP**1** may include a first display unit DA**1**-F and a peripheral area NDA around the first display unit DA**1**-F. The second display panel DP**2** may include a second display unit DA**2**-F. The area of the second display panel DP**2** may be smaller than the area of the first display panel DP**1**. The area of the first display unit DA**1**-F may be greater than the area of the second display unit DA**2**-F to correspond to the sizes of the first display panel DP**1** and the second display panel DP**2**.

[0093] The first display unit DA**1**-F may have a plan substantially parallel to a plane defined by a first direction DR**1** and a second direction DR**2**, when the electronic device **1000** is unfolded. The thickness direction of the electronic device **1000** may be parallel to a third direction DR**3** crossing the first direction DR**1** and the second direction DR**2**. Accordingly, front surfaces (or top surfaces) and back surfaces (or bottom surfaces) of members constituting the electronic device **1000** may be defined based on the third direction DR**3**.

[0094] The first display panel DP**1** or the first display unit DA**1**-F may include a folding region FA being folded and unfolded, and a plurality of non-folding regions NFA**1** and NFA**2** spaced apart from each other while interposing the folding region FA between the non-folding regions NFA**1** and NFA**2**. The second display panel DP**2** may overlap any one of the plurality of non-folding regions NFA**1** or NFA**2**. For example, the second display panel DP**2** may overlap the first non-folding region NFA**1**.

[0095] The display direction of a first image IM**1***a* displayed in a portion of the first display panel DP**1**, for example, in the first non-folding region NFA**1**, and the display direction of a second image IM**2***a* displayed on the second display panel DP**2** may be opposite to each other. For example, the first image IM**1***a* may be displayed in the third direction DR**3**, and the second image

IM**2***a* may be displayed in a fourth direction DR**4** opposite to the third direction DR**3**.
[0096] According to one or more embodiments of the present disclosure, the folding region FA may be bent about a folding axis extending in a direction parallel to a longer side of the electronic device **1000**, for example, a direction parallel to the second direction DR**2**. The folding region FA has a corresponding curvature and a corresponding radius of curvature, when the electronic device **1000** is folded. The first non-folding region NFA**1** and the second non-folding region NFA**2** may face each other, and the electronic device **1000** may be in an inner-folding state, such that that the first display unit DA**1**-F is not exposed to the outside.
[0097] According to one or more embodiments of the present disclosure, the electronic device **1000** may be in an outer-folding state such that the first display unit DA**1**-F is exposed to the outside. According to one or more embodiments of the present disclosure, the electronic device **1000** may be the inner-folding state or the outer-folding state from the state in which the electronic device **1000** is unfolded, and the present disclosure is not limited thereto.
[0098] Although FIG. **1**A illustrates that one folding region FA is defined in the electronic device **1000**, the present disclosure is not limited thereto. For example, a plurality of folding axes and a plurality of folding regions corresponding to the plurality of folding axes are defined in the electronic device **1000**, and the electronic device **1000** may be in the inner-folding state or the outer-folding state in each of the plurality of folding regions, from the state in which the each of the plurality of folding regions is unfolded.
[0099] According to one or more embodiments of the present disclosure, at least one of the first display panel DP**1** or the second display panel DP**2** may sense an input by a pen PN even without a digitizer. Accordingly, because the digitizer to sense the pen PN is omitted, the electronic device **1000** may be thinner and lighter with improved flexibility due to the digitizer added. Accordingly, the design may sense the pen PN even in the second display panel DP**2** in addition to the first display panel DP**1**.
[0100] FIG. **2** is a perspective view of an electronic device **1000**-**1** according to one or more embodiments of the present disclosure. FIG. **3** is a perspective view of an electronic device **1000**-**2** according to one or more embodiments of the present disclosure.
[0101] Although FIG. **2** illustrates that the electronic device **1000**-**1** is a cellular phone, the electronic device **1000**-**1** may include a display panel DP. Although FIG. **3** illustrates that the electronic device **1000**-**2** is a laptop computer, the electronic device **1000**-**2** may include the display panel DP. Although FIG. **3** is the perspective view of an electronic device **1000**-**2**, the coordinate axes included in FIG. **3** are displayed based on the display panel DP within the electronic device **1000**-**2**.
[0102] According to one or more embodiments of the present disclosure, the display panel DP may sense inputs applied to the outside. The external input may be a user input. The input of the user may include any one of various external inputs, such as a part of a physical body of the user, the pen PN (see FIG. **1**A), light, heat, or pressure.
[0103] According to one or more embodiments of the present disclosure, the display panel DP may sense an input made by the pen PN even without the digitizer. Accordingly, because the digitizer to sense the pen PN is omitted, the electronic device **1000**-**1** and **1000**-**2** may be thinner and lighter, which results from the digitizer added.
[0104] Although FIG. **1**A illustrates the electronic device **1000** in a foldable type, and FIG. **2** illustrates the electronic device **1000**-**1** in a bar type, the present disclosure is not limited thereto. For example, the following description may be applied to various electronic devices such as a rollable-type electronic device, a slidable-type electronic device, or a stretchable-type electronic device.
[0105] FIG. **4** is a cross-sectional view schematically illustrating the display panel DP according to one or more embodiments of the present disclosure.
[0106] Referring to FIG. **4**, the display panel DP may include a display layer **100** and a sensor layer

200.
[0107] The display layer **100** may be a component that substantially generates an image. The display layer **100** may include a display region **100**A and a non-display region **100**NA adjacent to the display region **100**A. The image may be displayed on the display region **100**A.
[0108] The display layer **100** may be a light-emitting display layer. For example, the display layer **100** may be an organic light-emitting display layer, an inorganic light-emitting display layer, an organic inorganic light-emitting display layer, a quantum dot display layer, a micro-LED display layer, or a nano-LED display layer. The display layer **100** may include a base layer **110**, a circuit layer **120**, a light-emitting element layer **130**, and an encapsulation layer **140**.
[0109] The base layer **110** may be a member that provides a base surface for disposing the circuit layer **120**. The base layer **110** may have a multi-layer structure or a single-layer structure. The base layer **110** may be a glass substrate, a metal substrate, a silicon substrate, or a polymer substrate, and the present disclosure is not limited thereto.
[0110] The circuit layer **120** may be located on the base layer **110**. The circuit layer **120** may include an insulating layer, a semiconductor pattern, a conductive pattern, and a signal line. An insulating layer, a semiconductor layer, and a conductive layer may be formed on the base layer **110** through a coating or deposition process. Thereafter, the insulating layer, the semiconductor layer, and the conductive layer may then be selectively patterned through multiple photolithography processes.
[0111] The light-emitting element layer **130** may be located on the circuit layer **120**. The light-emitting element layer **130** may include a light-emitting element. For example, the light-emitting element layer **130** may include an organic light-emitting material, an inorganic light-emitting material, an organic-inorganic light-emitting material, a quantum dot, a quantum rod, a micro-LED, or a nano-LED.
[0112] The encapsulation layer **140** may be located on the light-emitting element layer **130**. The encapsulation layer **140** may protect the light-emitting element layer **130** from foreign substances such as moisture, oxygen, and dust particles.
[0113] The sensor layer **200** may be located on the display layer **100**. The sensor layer **200** may include a sensing region **200**A and a peripheral region **200**NA adjacent to the sensing region **200**A. The sensing region **200**A may overlap the display region **100**A, and the peripheral region **200**NA may overlap the non-display region **100**NA.
[0114] The sensor layer **200** may sense an external input applied from the outside. The sensor layer **200** may be an integral-type sensor formed subsequently during the fabricating process of the display layer **100**, or an external-type sensor attached to the display layer **100**. The sensor layer **200** may be referred to as a sensor, an input sensor layer, an input-sensing panel, or an electronic device for sensing input coordinates.
[0115] According to one or more embodiments of the present disclosure, the sensor layer **200** may sense an input made by a passive-type input unit, such as a physical body of a user, and an input to an input device to generate a magnetic field having a corresponding resonance frequency. The input device may be referred to as a pen, an input pen, a magnetic pen, a stylus pen, or an electro-magnetic resonance (EMR) pen.
[0116] FIG. **5** is a view illustrating the operation of the electronic device **1000**, according to one or more embodiments of the present disclosure.
[0117] Referring to FIG. **5**, the electronic device **1000** may include the display layer **100**, the sensor layer **200**, a display driver **100**C, a sensor driver **200**C, a main driver **1000**C, and a power supply circuit **1000**P.
[0118] The sensor layer **200** may sense a first input **2000** or a second input **3000** applied thereto from an outside. Each of the first input **2000** and the second input **3000** may make a change in capacitance of the sensor layer **200** or may induce an induction current to the sensor layer **200**. For example, the first input **2000** may be made by a passive type input unit, such as the physical body

of a user. The second input **3000** may be made by the pen PN or by a radio frequency integrated circuit (RFIC) tag. For example, the pen PN may be a passive type pen or an active type pen.
[0119] According to one or more embodiments of the present disclosure, the pen PN may be a device to generate a magnetic field having a corresponding resonance frequency. The pen PN may be configured to transmit an output signal through an EMR scheme. The pen PN may be referred to as an input device, an input pen, a magnetic pen, a stylus pen, or an EMR pen.
[0120] The pen PN may include an RLC resonance circuit. The RLC resonance circuit may include an inductor L and a capacitor C. According to one or more embodiments of the present disclosure, the RLC resonance circuit may be a variable resonance circuit that varies a resonance frequency. In this case, the inductor L may be a variable inductor and/or the capacitor C may be a variable capacitor, but the present disclosure is not particularly limited thereto.
[0121] The inductor L generates a current by a magnetic field formed in the electronic device **1000**, for example, the sensor layer **200**. However, the present disclosure is not specifically limited thereto. For example, when the pen PN operates in an active type, the pen PN may generate a current even when the magnetic field is not provided from the outside. The generated current is transmitted to the capacitor C. The capacitor C charges the current received from the inductor L, and discharges the charged current to the inductor L. Thereafter, the inductor L may discharge a magnetic field having the resonance frequency. The induction current may flow through the sensor layer **200** by the magnetic field discharged from the pen PN, and the induction current may be transmitted to the sensor driver **200**C while serving as a received signal (or a sensing signal, a signal).
[0122] The main driver **1000**C may control an overall operation of the electronic device **1000**. For example, the main driver **1000**C may control the operations of the display driver **100**C and the sensor driver **200**C. The main driver **1000**C may include at least one microprocessor, and may further include a graphic controller. The main driver **1000**C may be referred to as an application processor, a central processing unit, or a main processor.
[0123] The display driver **100**C may control the display layer **100**. The display driver **100**C may receive image data and a control signal from the main driver **1000**C. The control signal may include various signals. For example, the control signal may include an input vertical synchronization signal, an input horizontal synchronization signal, a main clock, and a data enable signal.
[0124] The sensor driver **200**C may control the sensor layer **200**. The sensor driver **200**C may receive a control signal from the main driver **1000**C. The control signal may include a clock signal of the sensor driver **200**C. In addition, the control signal may further include a mode-determining signal for determining driving modes of the sensor driver **200**C and the sensor layer **200**.
[0125] The sensor driver **200**C may be integrated in the form of an integrated circuit (IC), and may be electrically connected to the sensor layer **200**. For example, the sensor driver **200**C may be directly mounted on a corresponding region of the display panel, or may be mounted through a chip-on-film (COF) scheme on a separate printed circuit board such that the sensor driver **200**C may be electrically connected to the sensor layer **200**.
[0126] The sensor driver **200**C and the sensor layer **200** may alternatively operate in a first mode or a second mode. For example, the first mode may be a mode for sensing a touch input, such as the first input **2000**. The second mode may be a mode for sensing the pen input, such as the second input **3000**. The first mode may be referred to as a touch-sensing mode, and the second mode may be referred to as a pen-sensing mode.
[0127] The switching between the first mode and the second mode may be performed in various switching manners. For example, the sensor driver **200**C and the sensor layer **200** may operate in the first mode and the second mode in a time-division scheme to sense the first input **2000** and the second input **3000**. Alternatively, the switching between the first mode and the second mode may be made by the selection of the user or a corresponding behavior (or input) of the user.

Alternatively, any one of the first mode or the second mode may be activated or deactivated or switched to a remaining mode among the first mode and the second mode through the specification application being activated or deactivated. Alternatively, the sensor driver **200**C and the sensor layer **200** may be maintained in the first mode when sensing the first input **2000**, or may be maintained in the second mode when sensing the second input **3000**, while alternatively operating in the first mode and the second mode.

[0128] The sensor driver **200**C may calculate information on coordinates of an input, based on a signal received from the sensor layer **200**, and may provide a coordinate signal having the coordinate information to the main driver **1000**C. The main driver **1000**C executes an operation corresponding to the user input, in response to the coordinate signal. For example, the main driver **1000**C may operate the display driver **100**C such that a new application image is displayed on the display layer **100**.

[0129] The power supply circuit **1000**P may include a power management integrated circuit (PMIC). The power supply circuit **1000**P may generate a plurality of driving voltages for driving the display layer **100**, the sensor layer **200**, the display driver **100**C, and the sensor driver **200**C. For example, the plurality of driving voltages may include a gate high voltage, a gate low voltage, a first driving voltage (e.g., the voltage of ELVSS), a second driving voltage (e.g., the voltage of ELVDD), or an initialization voltage.

[0130] FIG. **6**A is a cross-sectional view of the display panel DP, according to one or more embodiments of the present disclosure.

[0131] Referring to FIG. **6**A at least one buffer layer BFL is formed on a top surface of the base layer **110** (as used herein, "formed on" or "located on" may mean "above"). The buffer layer BFL may improve a bonding force between the base layer **110** and a semiconductor pattern. The buffer layer BFL may be formed in multiple layers. Alternatively, the display layer **100** may further include a barrier layer. The buffer layer BFL may include at least one of silicon oxide, silicon nitride, or silicon oxynitride. For example, the buffer layer BFL may include a structure in which a silicon oxide layer and a silicon nitride layer are alternately stacked.

[0132] Semiconductor patterns SC, AL, DR, and SCL may be located on the buffer layer BFL. The semiconductor patterns SC, AL, DR, and SCL may include polysilicon. However, the present disclosure is not limited thereto, and the semiconductor patterns SC, AL, DR, and SCL may include amorphous silicon, low-temperature polycrystalline silicon, or an oxide semiconductor.

[0133] FIG. **6**A only partially illustrates the semiconductor patterns SC, AL, DR, and SCL, and the semiconductor patterns are further located in another region. The semiconductor patterns SC, AL, DR, and SCL may be arranged in a corresponding rule across pixels. The semiconductor patterns SC, AL, DR, and SCL may have a different electrical properties, depending on doping states. The semiconductor patterns SC, AL, DR, and SCL may include the first regions SC, DR, and SCL having higher conductivity, and the second region AL having lower conductivity. The first regions SC, DR, and SCL may be doped with an N-type dopant or a P-type dopant. The P-type transistor may include a doped region doped with a P-type dopant, and the N-type transistor may include a doped region doped with an N-type dopant. The second region AL may be a non-doped region or a region doped at a lower concentration than the first regions SC, DR, and SCL.

[0134] The first regions SC, DR, and SCL may have conductivity higher than the conductivity of the second region AL, and may substantially serve as an electrode or a signal line. The second region AL may substantially correspond to an active region AL (or a channel) of a transistor **100**PC. In other words, first portion (see reference numeral AL) among the semiconductor patterns SC, AL, DR, and SCL may be the active region AL of the transistor **100**PC, and second portions among the semiconductor patterns SC, AL, DR, and SCL may be the source region SC or the drain region DR of the transistor **100**PC. A third portion (see reference numeral SCL) among the semiconductor patterns SC, AL, DR, and SCL may be a connection electrode or the connection signal line SCL.

[0135] Each of pixels may have an equivalent circuit including a plurality of transistors, at least one capacitor, and at least one light-emitting element, and the equivalent circuit of the pixel may be modified in various forms. FIG. **6**A illustrates that the pixel includes one transistor **100**PC and one light-emitting element **100**PE, by way of example.
[0136] The source region SC, the active region AL, and the drain region DR of the transistor **100**PC may be formed from the semiconductor patterns SC, AL, DR, and SCL. The source region SC and the drain region DR may extend in directions opposite to each other from the active region AL, when viewed in a cross-sectional view. FIG. **6**A illustrates a portion of the connection signal line SCL formed from the semiconductor patterns SC, AL, DR, and SCL. In one or more embodiments, the connection signal line SCL may be connected to the drain region DR of the transistor **100**PC, when viewed in a plan view.
[0137] A first insulating layer **10** may be located on the buffer layer BFL. The first insulating layer **10** may be a common layer and may overlap with a plurality of pixels to cover the semiconductor patterns SC, AL, DR, and SCL The first insulating layer **10** may be an inorganic layer and/or an organic layer, and may have a single-layer structure or a multi-layer structure. The first insulating layer **10** may include at least one of an aluminum oxide, a titanium oxide, a silicon oxide, a silicon nitride, a silicon oxynitride, a zirconium oxide, or hafnium oxide. The first insulating layer **10** may be a silicon oxide layer in a single layer. The insulating layer of the circuit layer **120**, which is to be described below, in addition to the first insulating layer **10**, may be an inorganic layer and/or an organic layer, and may have a single-layer structure or a multi-layer structure. The inorganic layer may include, but is not limited to, at least one of the above-described materials.
[0138] A gate GT of the transistor **100**PC is located on the first insulating layer **10**. The gate GT may be a portion of a metal pattern. The gate GT overlaps the active region AL. In the process for doping or reducing the semiconductor patterns SC, AL, DR, and SCL, the gate GT may serve as a mask.
[0139] A second insulating layer **20** may be located on the first insulating layer **10** to cover the gate GT. The second insulating layer **20** may be commonly overlapped with the pixels. The second insulating layer **20** may be an inorganic layer and/or an organic layer, and may have a single-layer or multi-layer structure. The second insulating layer **20** may include at least one of silicon oxide, silicon nitride, or silicon oxynitride. The second insulating layer **20** may have a multi-layer structure including a silicon oxide layer and a silicon nitride layer.
[0140] A third insulating layer **30** may be located on the second insulating layer **20**. The third insulating layer **30** may have a single-layer structure or a multi-layer structure. For example, the third insulating layer **30** may have a multi-layer structure including a silicon oxide layer and a silicon nitride layer.
[0141] A first connection electrode CNE**1** may be located on the third insulating layer **30**. The first connection electrode CNE**1** may be connected to the connection signal line SCL through a contact hole CNT-**1** formed through the first insulating layer **10**, the second insulating layer **20**, and the third insulating layer **30**.
[0142] A fourth insulating layer **40** may be located on the third insulating layer **30**. The fourth insulating layer **40** may be a silicon oxide layer in a single layer. A fifth insulating layer **50** may be located on the fourth insulating layer **40**. The fifth insulating layer **50** may be an organic layer.
[0143] A second connection electrode CNE**2** may be located on the fifth insulating layer **50**. The second connection electrode CNE**2** may be connected to the first connection electrode CNE**1** through a contact hole CNT-**2** formed through the fourth insulating layer **40**, and the fifth insulating layer **50**.
[0144] A sixth insulating layer **60** may be located on the fifth insulating layer **50** and may cover the second connection electrode CNE**2**. The sixth insulating layer **60** may be an organic layer.
[0145] The light-emitting element layer **130** may be located on the circuit layer **120**. The light-emitting element layer **130** may include the light-emitting element **100**PE. For example, the light-

emitting element layer **130** may include an organic light-emitting material, an inorganic light-emitting material, an organic-inorganic light-emitting material, a quantum dot, a quantum rod, a micro-LED, or a nano-LED. The following description will be described regarding the light-emitting element **100**PE that is an organic light-emitting element, by way of example, but the present disclosure is not specifically limited thereto.

[0146] The light-emitting element **100**PE may include a first electrode AE, a light-emitting layer EL, and a second electrode CE.

[0147] The first electrode AE may be located on the sixth insulating layer **60**. The first electrode AE may be connected with the second connection electrode CNE**2** through a contact hole CNT-**3** formed through the sixth insulating layer **60**.

[0148] A pixel-defining layer **70** may be located on the sixth insulating layer **60** and may cover a portion of the first electrode AE. An opening **70**-OP is defined in the pixel-defining layer **70**. The opening **70**-OP of the pixel-defining layer **70** exposes at least a portion of the first electrode AE.

[0149] The first display unit DA**1**-F (see FIG. **1**A) may include a light-emitting region PXA and a non-light-emitting region NPXA adjacent to the light-emitting region PXA. The non-light-emitting region NPXA may surround the light-emitting region PXA. According to one or more embodiments, the light-emitting region PXA is defined to correspond to a portion of the first electrode AE, which is exposed by the opening **70**-OP.

[0150] The light-emitting layer EL may be located on the first electrode AE. The light-emitting layer EL may be located in a region defined by the opening **70**-OP. Although FIG. **6**A illustrates that the light-emitting layer EL is located in the opening **70**-OP, the present disclosure is not limited thereto. For example, the light-emitting layer EL may extend to cover a side surface of the pixel-defining layer **70** and a portion of the top surface of the pixel-defining layer **70**, which define the opening **70**-OP.

[0151] According to one or more embodiments of the present disclosure, the light-emitting layer EL may be separately formed with respect to pixels. When the light-emitting layer EL is separately formed with respect to the pixels, each of light-emitting layers EL may emit light of at least one of a blue color, a red color, or a green color. However, the present disclosure is not limited thereto. The light-emitting layer EL may have an integral form, and may be included in the plurality of pixels in common. In this case, the light-emitting layer EL may provide blue light or white light.

[0152] The second electrode CE may be located on the light-emitting layer EL. The second electrode CE may have an integral-type form, and may be located in the plurality of pixels in common.

[0153] According to one or more embodiments of the present disclosure, a hole control layer may be located in the first electrode AE and the light-emitting layer EL. The hole control layer may be located in the light-emitting region PXA and the non-light-emitting region NPXA in common. The hole control layer may further include a hole transfer layer and a hole injection layer. An electron control layer may be interposed between the light-emitting layer EL and the second electrode CE. The electron control layer may include an electron transfer layer and may further include an electron injection layer. The hole control layer and the electron control layer may be formed in the plurality of pixels in common by using an open mask or an ink-jet process.

[0154] The encapsulation layer **140** may be located on the light-emitting element layer **130**. The encapsulation layer **140** may include an inorganic layer, an organic layer, and an inorganic layer sequentially stacked, and layers constituting the encapsulation layer **140** are not limited thereto. The inorganic layers may protect the light-emitting element layer **130** from moisture and oxygen, and the organic layer may protect the light-emitting element layer **130** from a foreign material, such as dust particles. The inorganic layers may include a silicon nitride layer, a silicon oxynitride layer, a silicon oxide layer, a titanium oxide layer, or an aluminum oxide layer. The organic layer may include an acrylic-based organic layer, but the present disclosure is not limited thereto.

[0155] The sensor layer **200** may include a base layer **201**, a first conductive layer **202**, an

intermediate insulating layer **203**, a second conductive layer **204**, and a cover insulating layer **205**.
[0156] The base layer **201** may be an inorganic layer including at least one of silicon nitride, silicon oxynitride, or silicon oxide. Alternatively, the base layer **201** may be an organic layer including an epoxy resin, an acrylic resin, or an imide-based resin. The base layer **201** may have a single-layer structure or a multi-layer structure including layers stacked in the third direction DR**3**. According to one or more embodiments of the present disclosure, the sensor layer **200** may not include the base layer **201**.
[0157] Each of the first conductive layer **202** and the second conductive layer **204** may have a single-layer structure or a multi-layer structure including the layers stacked in the third direction DR**3**.
[0158] Each of the first conductive layer **202** and the second conductive layer **204** having a single-layer structure may include a metal layer or a transparent conductive layer. The metal layer may include molybdenum, silver, titanium, copper, aluminum, or an alloy thereof. The transparent conductive layer may include a transparent conductive oxide, such as indium tin oxide (ITO), indium zinc oxide (IZO), zinc oxide (ZnO), or indium zinc tin oxide (IZTO). In addition, the transparent conductive layer may include a conductive polymer, such as poly(3,4-ethylenedioxythiophene) (PEDOT), metal nanowires, or graphene.
[0159] Each of the first conductive layer **202** and the second conductive layer **204** having a multi-layer structure may include metal layers. The metal layers may have, for example, a three-layer structure of titanium/aluminum/titanium. The conductive layer in the multi-layer structure may include at least one metal layer and at least one transparent conductive layer.
[0160] According to one or more embodiments of the present disclosure, the thickness of the first conductive layer **202** may be greater than or equal to the thickness of the second conductive layer **204**. When the thickness of the first conductive layer **202** is greater than the thickness of the second conductive layer **204**, the resistance of components (e.g., an electrode, a sensing pattern, or a bridge pattern) included in the first conductive layer **202** may be reduced. In addition, because the first conductive layer **202** is located below the second conductive layer **204**, even if the thickness of the first conductive layer **202** is increased, the probability that components included in the first conductive layer **202** are viewed by external light reflection, may be lower than that of the second conductive layer **204**.
[0161] At least one of the intermediate insulating layer **203** or the cover insulating layer **205** may include an inorganic film. The inorganic film may include at least one of an aluminum oxide, a titanium oxide, a silicon oxide, a silicon nitride, a silicon oxynitride, a zirconium oxide, or hafnium oxide.
[0162] At least one of the intermediate insulating layer **203** or the cover insulating layer **205** may include an organic film. The organic film may include at least one of an acrylic resin, a methacryl resin, polyisoprene, a vinyl resin, an epoxy resin, a urethane resin, a cellulose resin, a siloxane resin, a polyimide resin, a polyamide resin, or a perylene resin.
[0163] Although the above-description has been made regarding that the total of two conductive layers of the first conductive layer **202** and the second conductive layer **204** are provided, the present disclosure is not limited thereto. For example, the sensor layer **200** may include at least three conductive layers.
[0164] FIG. **6**B is a cross-sectional view illustrating the sensor layer **200**, according to one or more embodiments of the present disclosure.
[0165] Referring to FIGS. **6**A and **6**B, a second width **204***wt* of a second mesh line MS**2** included in the second conductive layer **204** may be equal to or greater than a first width **202***wt* of a first mesh line MS**1** included in the first conductive layer **202**. When a user USR views the first mesh line MS**1** and the second mesh line MS**2** from the side, because the first mesh line MS**1** has a smaller width than the second mesh line MS**2**, the probability that the first mesh line MS**1** is viewed by the user USR may be reduced.

[0166] Each of the first mesh line MS**1** and the second mesh line MS**2** may include first metal layers M**1**, and a second metal layer M**2** interposed between the first metal layers M**1**. For example, the first metal layers M**1** may include titanium (Ti), and the second metal layer M**2** may include aluminum (Al). However, the present disclosure is not specifically limited thereto.
[0167] According to one or more embodiments of the present disclosure, a first thickness TK**1** of the second metal layer M**2** of the first mesh line MS**1** may be substantially equal to a second thickness TK**2** of the second metal layer M**2** of the second mesh line MS**2**, but the present disclosure is not particularly limited thereto. For example, the first thickness TK**1** may be thicker than the second thickness TK**2**. Alternatively, the second thickness TK**2** may be thicker than the first thickness TK**1**. According to one or more embodiments of the present disclosure, each of the first thickness TK**1** and the second thickness TK**2** may be 1000 angstroms or more, for example, 6000 angstroms.
[0168] FIG. **7** is a cross-sectional view illustrating the sensor layer **200**, according to one or more embodiments of the present disclosure. FIG. **8** is an enlarged plan view illustrating a sensing unit SU according to one or more embodiments of the present disclosure. FIG. **9**A is a plan view illustrating a first conductive layer **202**SU of the sensing unit SU according to one or more embodiments of the present disclosure. FIG. **9**B is a plan view illustrating a second conductive layer **204**SU of the sensing unit SU according to one or more embodiments of the present disclosure. FIG. **9**C is a cross-sectional view of the sensor layer **200** according to one or more embodiments of the present disclosure, which is taken along the line I-I′ shown in FIGS. **9**A and **9**B, respectively.
[0169] Referring to FIG. **7**, the sensor layer **200** may include the sensing region **200**A, and the peripheral region **200**NA adjacent to the sensing region **200**A.
[0170] The sensor layer **200** may include a plurality of first electrode groups **210**G, a plurality of second electrode groups **220**G, a plurality of third electrode groups **230**G, and a fourth electrode group **240**G located in the sensing region **200**A.
[0171] The first electrode groups **210**G may cross the second electrode groups **220**G, respectively. The first electrode groups **210**G may extend in the second direction DR**2**, and may be arranged to be spaced apart from each other in the first direction DR**1**. The second electrode groups **220**G may extend in the first direction DR**1**, and may be arranged to be spaced apart from each other in the second direction DR**2**. The sensing unit SU of the sensor layer **200** may be a region in which one first electrode group **210**G crosses one second electrode group **220**G.
[0172] As illustrated in FIG. **7**, **10** first electrode groups **210**G and five second electrode groups **220**G are provided, and 50 sensing units SU are provided, but the number of first electrode groups **210**G and the number of second electrode groups **220**G are not limited thereto.
[0173] According to one or more embodiments of the present disclosure, each of the second electrode groups **220**G may include a first divided electrode **220**-D**1** and a second divided electrode **220**-D**2**. The first divided electrode **220**-D**1** and the second divided electrode **220**-D**2** may be spaced apart from each other in the first direction DR**1**. Each of the first divided electrode **220**-D**1** and the second divided electrode **220**-D**2** may extend in the first direction DR**1**. The first divided electrode **220**-D**1** and the second divided electrode **220**-D**2** included in one second electrode group **220**G may sense along the same axis (for example, an axis extending in the first direction DR**1**).
[0174] Referring to FIGS. **7** and **8**, each of the first electrode groups **210**G may include first divided electrodes **210***dv***1** and **210***dv***2**. The first divided electrodes **210***dv***1** and **210***dv***2** may extend in the second direction DR**2**, and may be spaced apart from each other in the first direction DR**1**. The first divided electrodes **210***dv***1** and **210***dv***2** may have a symmetrical shape about a line extending in the second direction DR**2**.
[0175] Each of the first divided electrode **220**-D**1** and the second divided electrode **220**-D**2** may include second unit divided electrodes **220***dv***1** and **220***dv***2**. The second unit divided electrodes **220***dv***1** and **220***dv***2** extend in the first direction DR**1** and may be spaced apart from each other in

the second direction DR**2**. The second unit divided electrodes **220***dv***1** and **220***dv***2** may have linear symmetrical shapes about a line extending in the first direction DR**1**.

[0176] Referring to FIGS. **8**, **9**A, **9**B, and **9**C, each of the second unit divided electrodes **220***dv***1** and **220***dv***2** may include a sensing pattern **221** and a bridge pattern **222**. The sensing pattern **221** and the bridge pattern **222** are located in different layers, and the sensing pattern **221** and the bridge pattern **222** may be electrically connected to each other through a first contact CNa. For example, the bridge pattern **222** may be included in the first conductive layer **202**SU, and the sensing pattern **221** and the first divided electrodes **210***dv***1** and **210***dv***2** may be included in the second conductive layer **204**SU. The first conductive layer **202**SU may be included in the first conductive layer **202** of FIG. **6**A, and the second conductive layer **204**SU may be included in the second conductive layer **204** of FIG. **6**A.

[0177] Referring to FIG. **7**, the third electrode groups **230**G may be arranged to be spaced apart from each other in the first direction DR**1**. According to one or more embodiments of the present disclosure, the third electrode groups **230**G may include a plurality of first auxiliary electrodes **230**S that are electrically connected to each other. The number of first auxiliary electrodes **230**S included in each of the third electrode groups **230**G may be variously modified. For example, as the number of first auxiliary electrodes **230**S included in each of the third electrode groups **230**G increases, resistance of each of the third electrode groups **230**G decreases, power efficiency may be improved, and sensing sensitivity may be improved. To the contrary, as the number of first auxiliary electrodes **230**S included in each of the third electrode groups **230**G decreases, a loop coil pattern formed by using the third electrode groups **230**G may be implemented in more various forms.

[0178] Although FIG. **7** exemplarily illustrates which one third electrode group **230**G includes two first auxiliary electrodes **230**S, the present disclosure is not limited thereto. The first auxiliary electrodes **230**S may be located in a one-to-one correspondence to the first electrode groups **210**G. Accordingly, one sensing unit SU may include a portion of one first auxiliary electrode **230**S.

[0179] A coupling capacitor may be defined between one first electrode group **210**G and one first auxiliary electrode **230**S. In this case, an induction current generated during pen sensing may be transferred from the first auxiliary electrode **230**S to the first electrode group **210**G through the coupling capacitor. In other words, the first auxiliary electrode **230**S may serve to supplement the signal transmitted from the first electrode group **210**G to the sensor driver **200**C. Accordingly, when the signal induced to the first auxiliary electrode **230**S is in phase with the signal induced to the first electrode group **210**G, an improved or greatest effect may be obtained. Accordingly, the center of each of the first electrode groups **210**G in the second direction DR**2** may be aligned with the center of each of the first auxiliary electrodes **230**S in the second direction DR**2**. In addition, the center of each of the first electrode groups **210**G in the first direction DR**1** may be aligned with the center of each of the first auxiliary electrodes **230**S in the first direction DR**1**.

[0180] According to one or more embodiments of the present disclosure, because one third electrode group **230**G includes two first auxiliary electrodes **230**S, one third electrode group **230**G may correspond to (or overlap) the two first electrode groups **210**G. Accordingly, the number of first electrode groups **210**G included in the sensor layer **200** may be greater than the number of third electrode groups **230**G. For example, the number of first electrode groups **210**G may be equal to the product of the number of third electrode groups **230**G included in the sensor layer **200** and the number of first auxiliary electrodes **230**S included in each of the third electrode groups **230**G. In FIG. **7**, the number of first electrode groups **210**G is ‘10’, the number of third electrode groups **230**G is ‘5’, and the number of first auxiliary electrodes **230**S included in each of the third electrode groups **230**G may be ‘2’.

[0181] The fourth electrode group **240**G may include a plurality of second auxiliary electrodes **240**S arranged in the second direction DR**2**. Each of the second auxiliary electrodes **240**S may extend in the first direction DR**1**. According to one or more embodiments of the present disclosure,

the second auxiliary electrodes **240**S may be electrically connected to each other.
[0182] A coupling capacitor may be defined between one second electrode group **220**G and one second auxiliary electrode **240**S. In this case, an induction current generated during pen sensing may be transmitted from the second auxiliary electrode **240**S to the second electrode group **220**G through the coupling capacitor. In other words, the second auxiliary electrode **240**S may serve to supplement a signal transmitted from the second electrode group **220**G to the sensor driver **200**C. Accordingly, when the signal induced to the second auxiliary electrode **240**S is in phase with the signal induced to the second electrode group **220**G, an improved or greatest effect may be produced. Accordingly, the center of each of the second electrode groups **220**G in the first direction DR**1** may be aligned with the center of each of the second auxiliary electrode **240**S in the first direction DR**1**. In addition, the center of each of the second electrode groups **220**G in the second direction DR**2** may be aligned with the center of each of the second auxiliary electrode **240**S in the second direction DR**2**.
[0183] Referring to FIGS. **7**, **9**A, and **9**B, each of the first auxiliary electrodes **230**S included in the third electrode group **230**G may include a (3-1)-th pattern **231** and a (3-2)-th pattern **232**. The (3-1)-th pattern **231** and the (3-2)-th pattern **232** are located in different layers, and may be electrically connected to each other through a second contact CNb. The (3-1)-th pattern **231** may be included in the first conductive layer **202**SU, and the (3-2)-th pattern **232** may be included in the second conductive layer **204**SU.
[0184] According to one or more embodiments of the present disclosure, a portion of the (3-1)-th pattern **231** may overlap a portion of each of the first divided electrodes **210***dv***1** and **210***dv***2**. Accordingly, a coupling capacitor may be provided (or formed) between the first electrode group **210**G and the third electrode group **230**G.
[0185] Referring to FIGS. **7**, **9**A, and **9**B, each of the second auxiliary electrodes **240**S included in the fourth electrode group **240**G may include a (4-1)-th pattern **241**, a (4-2)-th pattern **242**, and a (4-3)-th pattern **243**. The (4-2)-th pattern **242** and the (4-3)-th pattern **243** may be located in the same layer, and the (4-1)-th pattern **241** may be located in a different layer from the (4-2)-th pattern **242** and the (4-3)-th pattern **243**. The (4-1)-th pattern **241** and the (4-2)-th pattern **242** may be electrically connected to each other through a third contact CNc, and the (4-1)-th pattern **241** and the (4-3)-th pattern **243** may be electrically connected to each other through a fourth contact CNd. The (4-2)-th pattern **242** and the (4-3)-th pattern **243** may be included in the first conductive layer **202**SU, and the (4-1)-th pattern **241** may be included in the second conductive layer **204**SU.
[0186] According to one or more embodiments of the present disclosure, a portion of the (4-2)-th pattern **242** may overlap the sensing pattern **221** of each of the second unit divided electrodes **220***dv***1** and **220***dv***2**. Accordingly, a coupling capacitor may be defined (or provided or formed) between the second electrode group **220**G and the fourth electrode group **240**G.
[0187] According to one or more embodiments of the present disclosure, the first conductive layer **202**SU may further include dummy patterns DMP. Each of the dummy patterns DMP may be electrically floated or electrically grounded. According to one or more embodiments of the present disclosure, the dummy patterns DMP may be omitted. Because the dummy patterns DMP are located in the empty space, the probability that patterns are viewed by external light reflection may be reduced.
[0188] The sensor layer **200** may further include a plurality of first pads PD**1** connected in one-to-one correspondence to a plurality of first trace lines **210***t* located in the peripheral region **200**NA. The first trace lines **210***t* may be electrically connected in one-to-one correspondence to the first electrode groups **210**G. In other words, one first trace line **210***t* may be connected to one first electrode group **210**G.
[0189] The sensor layer **200** may further include a plurality of second trace lines **220***t* at least partially overlapped with the sensing region **200**A, and a plurality of second pads PD**2** connected in one-to-one correspondence to the plurality of second trace lines **220***t*. The second trace lines **220***t*

may overlap the first electrode groups **210**G and the second electrode groups **220**G, or may be insulated from the first electrode groups **210**G and the second electrode groups **220**G while crossing the first electrode groups **210**G and the second electrode groups **220**G. Accordingly, the area of the peripheral region **200**NA may be reduced. Accordingly, the area occupied by the peripheral region **200**NA on the front surface of the electronic device **1000** (see FIG. **1**A) may be reduced, and a narrower bezel may be implemented.

[0190] The first trace lines **210***t* may be electrically connected in a one-to-one correspondence to the first electrode groups **210**G. The two first divided electrodes **210***dv***1** and **210***dv***2** included in one first electrode group **210**G may be connected to one of the first trace lines **210***t*. Each of the first trace lines **210***t* may include a plurality of branches to be connected to the two first divided electrodes **210***dv***1** and **210***dv***2**. According to one or more embodiments of the present disclosure, the two first divided electrodes **210***dv***1** and **210***dv***2** may be connected to each other in the sensing region **200**A.

[0191] The second trace lines **220***t* may be electrically connected to the second electrode groups **220**G in a 2:1 correspondence to the second electrode groups **220**G. Because the second trace lines **220***t* are electrically connected to the second electrode groups **220**G in the 2:1 correspondence, the number of second trace lines **220***t* may be two times the number of second electrode groups **220**G. In other words, two second trace lines **220***t***1** and **220***t***2** may be electrically connected to one second electrode group **220**G.

[0192] One of the second trace lines **220***t***1** and **220***t***2** may be referred to as the (2-1)-th trace line **220***t***1**, and a remaining one of the second trace lines **220***t***1** or **220***t***2** may be referred to as the (2-2)-th trace line **220***t***2**. The (2-1)-th trace line **220***t***1** may be electrically connected to the first divided electrode **220**-D**1**, and the (2-2)-th trace line **220***t***2** may be electrically connected to the second divided electrode **220**-D**2**.

[0193] At least a portion of each of the (2-1)-th trace line **220***t***1** and the (2-2)-th trace line **220***t***2** may overlap the display region **100**A (see FIG. **4**). For example, when viewed in a plan view, the shape or the area of the display region **100**A may be similar to the shape or the area of the sensing region **200**A.

[0194] According to one or more embodiments of the present disclosure, the (2-1)-th trace line **220***t***1** and the (2-2)-th trace line **220***t***2** electrically connected to one second electrode group **220**G may have substantially equal lengths in the second direction DR**2**. For example, a portion of the (2-1)-th trace line **220***t***1** overlapped with the sensing region **200**A may have a length substantially equal to a length of a portion of the (2-2)-th trace line **220***t***2** overlapped with the sensing region **200**A.

[0195] According to one or more embodiments of the present disclosure, because the second trace lines **220***t* overlap the sensing region **200**A, the second trace lines **220***t* may be spread more widely in the sensing region **200**A than the peripheral region **200**NA. Accordingly, mutual inductances between the pen PN and the second trace lines **220***t* may vary depending on the position of the pen PN (see FIG. **5**).

[0196] According to one or more embodiments of the present disclosure, the sensor driver **200**C (refer to FIG. **5**) may perform a primary differential sensing operation with respect to a signal provided from the (2-1)-th trace line **220***t***1** and a signal provided from the (2-2)-th trace line **220***t***2** before differentially sensing signals received from two different second electrode groups. Mutual inductances of the (2-1)-th trace line **220***t***1** and the (2-2)-th trace line **220***t***2** affecting the distortion of coordinates may be removed through the primary differential sensing operation. Accordingly, the coordinate accuracy sensed by the sensor layer **200** and the sensor driver **200**C may be improved.

[0197] The (2-1)-th trace line **220***t***1** may be connected to one region of the first divided electrode **220**-D**1** adjacent to the second divided electrode **220**-D**2**, and the (2-2)-th trace line **220***t***2** may be connected to one region of the second divided electrode **220**-D**2** adjacent to the first divided electrode **220**-D**1**. For example, each of the (2-1)-th trace line **220***t***1** and the (2-2)-th trace line

220*t***2** may extend from a region adjacent to the gap between the first divided electrode **220**-D**1** and the second divided electrode **220**-D**2**.

[0198] The sensor layer **200** may further include third trace lines **230***rt***1** located in the peripheral region **200**NA, third pads PD**3** connected in one-to-one correspondence to the third trace lines **230***rt***1**, a fourth trace line **240***t*, a fourth pad PD**4** connected to the fourth trace line **240***t*, a fifth trace line **230***rt***2**, and fifth pads PD**5** connected to one end and an opposite of the fifth trace line **230***rt***2**.

[0199] The third trace lines **230***rt***1** may be connected in a one-to-one correspondence to the third electrode groups **230**G, respectively. In other words, the number of third trace lines **230***rt***1** may correspond to the number of third electrode groups **230**G. In FIG. **7**, five third trace lines **230***rt***1** are illustrated.

[0200] According to one or more embodiments of the present disclosure, the third trace lines **230***rt***1** and the third pad PD**3** may be omitted, or a charging driving mode for charging the pen may be omitted. In this case, the sensor layer **200** may sense an input made by an active-type pen, which is able to emit a magnetic field, even though a magnetic field is not provided from the sensor layer **200**.

[0201] The fourth trace line **240***t* may be electrically connected to the second auxiliary electrodes **240**S.

[0202] The fifth trace line **230***rt***2** may be electrically connected to at least one first auxiliary electrode **230**S of the first auxiliary electrodes **230**S. According to one or more embodiments of the present disclosure, the fifth trace line **230***rt***2** may be electrically connected to all of the first auxiliary electrodes **230**S. In other words, the fifth trace line **230***rt***2** may be electrically connected to all of the third electrode groups **230**G. The fifth trace line **230***rt***2** may include a first line portion **231***t* extending in the first direction DR**1** and electrically connected to the third electrode groups **230**G, a second line portion **232***t* extending in the second direction DR**2** from a first end portion of the first line portion **231***t*, and a third line portion **233***t* extending in the second direction DR**2** from a second end portion of the first line portion **231***t*.

[0203] According to one or more embodiments of the present disclosure, each of the resistance of the second line portion **232***t* and the resistance of the third line portion **233***t* may be substantially equal to the resistance of one third electrode group of the third electrode groups **230**G. Accordingly, the second line portion **232***t* and the third line portion **233***t* may function as the third electrode groups **230**G, thereby producing an effect the same as an effect produced when the third electrode groups **230**G are located in the peripheral region. For example, any one of the second line portion **232***t* or the third line portion **233***t* and any one of the third electrode groups **230**G may form a coil. Accordingly, even a pen positioned in a region adjacent to the peripheral region **200**NA may be sufficiently charged by a loop including the second line portion **232***t* or the third line portion **233***t*.

[0204] According to one or more embodiments of the present disclosure, to adjust the resistance of the second line portion **232***t* and the resistance of the third line portion **233***t*, the width of each of the second line portion **232***t* and the third line portion **233***t* in the first direction DR**1** may be adjusted. However, this is provided only for the illustrative purpose. For example, the first to third line portions **231***t*, **232***t*, and **233***t* may have substantially equal widths.

[0205] Referring to FIGS. **9**A and **9**B, areas occupied by components included in the first electrode group **210**G and the second electrode group **220**G in the second conductive layer **204**SU in one sensing unit SU may be wider than areas occupied by components included in the third electrode group **230**G and the fourth electrode group **240**G. A change in capacitance by the first input **2000** (see FIG. **4**) may increase as the distance of the first input **2000** decreases. Accordingly, a component to sense the first input **2000** (see FIG. **4**) may be located while occupying a larger area in a layer adjacent to the surface of the electronic device **1000** (see FIG. **1**A). Accordingly, touch performance may be improved.

[0206] FIGS. **7** to **9**C illustrate the structure in which each of the first to fourth electrode groups **210**G, **220**G, **230**G, and **240**G is divided and respectively located in two conductive layers **202**SU and **204**SU, but the present disclosure is not particularly limited thereto. For example, the first to fourth electrode groups **210**G, **220**G, **230**G, and **240**G may be divided to be arranged in three conductive layers or in four conductive layers.

[0207] According to one or more embodiments of the present disclosure, the third electrode groups **230**G receiving the signal in the charging driving mode may be included in a third conductive layer located under the first and second conductive layers **202**SU and **204**SU. For example, the third conductive layer may be provided under the base layer **201**. The third conductive layer may be located between the base layer **201** and the display layer **100**, may be located under the display layer **100**, or may be included in the display layer **100**.

[0208] The first, second, and fourth electrode groups **210**G, **220**G, and **240**G may be included in the first and second conductive layers **202**SU and **204**SU. For example, when the third electrode groups **230**G are implemented in the form of a separate conductive layer, such as the third conductive layer, the shapes of the third electrode groups **230**G may be more freely designed. For example, the third electrode groups **230**G may be provided in a form including a plurality of coils. In addition, the third electrode groups **230**G may be provided more densely using the third conductive layer. In this case, pen-sensing sensitivity may be improved. According to one or more embodiments of the present disclosure, the third conductive layer may include the fourth electrode group **240**G instead of the third electrode groups **230**G.

[0209] FIG. **10**A is a plan view illustrating a first conductive layer **202**SUa of a sensing unit according to one or more embodiments of the present disclosure. FIG. **10**B is a plan view illustrating a second conductive layer **204**SUa of a sensing unit according to one or more embodiments of the present disclosure. FIG. **10**C is a cross-sectional view of a sensor layer taken along the line II-II′ of FIGS. **10**A and **10**B, respectively.

[0210] Referring to FIGS. **8**, **10**A, **10**B, and **10**C, each of the first electrode groups **210**G may include a plurality of first sensing patterns **211** and a plurality of first bridge patterns **212**. The first sensing patterns **211** are spaced apart from each other in the second direction DR**2**, and the first bridge patterns **212** may extend in the second direction DR**2**, and may be electrically connected to the first sensing patterns **211** through a first contact CNa**1**. Although FIGS. **10**A and **10**B illustrate that two adjacent first sensing patterns **211** are electrically connected to each other through two first bridge patterns **212**, but the present disclosure is not limited thereto. For example, the two adjacent first sensing patterns **211** may be electrically connected to each other through one first bridge pattern **212**, or may be electrically connected to each other through three or more first bridge patterns **212**.

[0211] FIG. **10**B illustrates the first divided electrode **220**-D**1** among the first divided electrode **220**-D**1** and the second divided electrode **220**-D**2**. The first sensing patterns **211** adjacent to each other in the second direction DR**2** may be spaced apart from each other while interposing the first divided electrode **220**-D**1** between the first sensing patterns **211**. According to one or more embodiments of the present disclosure, the first sensing patterns **211**, the first divided electrode **220**-D**1**, and the second divided electrode **220**-D**2** may be included in a second conductive layer **204**SUa, and the first bridge patterns **212** may be included in a first conductive layer **202**SUa. The first bridge patterns **212** may insulate and cross the first divided electrode **220**-D**1** or the second divided electrode **220**-D**2** while overlapping the first divided electrode **220**-D**1** or the second divided electrode **220**-D**2**.

[0212] Each of the first auxiliary electrodes **230**S included in the third electrode group **230**G may extend in the second direction DR**2**. The first auxiliary electrodes **230**S may be included in the first conductive layer **202**SUa. One or more holes may be defined in each of the first auxiliary electrodes **230**S. One first bridge pattern **212** may be located in one hole. Accordingly, the first bridge pattern **212** may be electrically insulated from the first auxiliary electrodes **230**S.

[0213] Each of the second auxiliary electrodes **240**S included in the fourth electrode group **240**G may include a plurality of second sensing patterns **241***a* and a plurality of second bridge patterns **242***a*. The second sensing patterns **241***a* are spaced apart in the first direction DR**1**, and the second bridge patterns **242***a* may extend in the first direction DR**1** to be electrically connected to the second sensing patterns **241***a* through a second contact CNb**1**.
[0214] Although FIGS. **10**A and **10**B illustrate which two adjacent second sensing patterns **241***a* are electrically connected to each other through two second bridge patterns **242***a*, the present disclosure is not limited thereto. For example, in one or more other embodiments, two adjacent second sensing patterns **241***a* may be electrically connected to each other through one second bridge pattern **242***a*, or may be electrically connected to each other through three or more second bridge patterns **242***a*.
[0215] According to one or more embodiments of the present disclosure, the second sensing patterns **241***a* and the first auxiliary electrodes **230**S may be included in the first conductive layer **202**SUa, and the second bridge patterns **242***a* may be included in the second conductive layer **204**SUa. The second bridge patterns **242***a* may be insulated from the first auxiliary electrodes **230**S overlapped with the second bridge patterns **242***a* while crossing the first auxiliary electrodes **230**S overlapped with the second bridge patterns **242***a*.
[0216] Referring to FIGS. **10**A and **10**B, in the second conductive layer **204**SU in one sensing unit SU, areas occupied by components included in the first electrode group **210**G and the second electrode group **220**G may be greater than areas occupied by components included in the third electrode group **230**G and the fourth electrode group **240**G. The change in capacitance due to the first input **2000** (see FIG. **4**) may be greater, as the first input **2000** approaches. Accordingly, a component for sensing the first input **2000** (see FIG. **4**) may be located with a relatively larger area in a layer adjacent to a surface of the electronic device **1000** (see FIG. **1**A). Accordingly, touch performance may be improved.
[0217] According to one or more embodiments of the present disclosure, the first conductive layer **202**SUa may further include first dummy patterns DMP**1**, and the second conductive layer **204**SUa may further include second dummy patterns DMP**2**. Each of the first dummy patterns DMP**1** and the second dummy patterns DMP**2** may be floated or electrically floated. Each of the first dummy patterns DMP**1** and the second dummy patterns DMP**2** may be divided into a plurality of conductive patterns. For example, one first dummy pattern DMP**1** may include a plurality of floating dummy patterns that are separated from each other or electrically isolated from each other.
[0218] Referring to FIG. **10**C, the area of the first auxiliary electrode **230**S and the area of the first sensing pattern **211** may be adjusted. For example, the position of the boundary between the first auxiliary electrode **230**S and the first dummy patterns DMP**1**, and the position of the boundary between the first sensing pattern **211** and the second dummy patterns DMP**2**, may be adjusted. In this case, the area of the overlap region between the first auxiliary electrode **230**S and the first sensing pattern **211** may be adjusted to adjust the capacitance size of a coupling capacitor C-CP between the first auxiliary electrode **230**S and the first sensing pattern **211**.
[0219] FIG. **11**A is an enlarged plan view of region AA′ illustrated in FIG. **9**A. FIG. **11**B is an enlarged plan view of region BB′ illustrated in FIG. **9**B.
[0220] Referring to FIGS. **9**A, **9**B, **11**A, and **11**B, each of the first electrode groups **210**G, the second electrode groups **220**G, the third electrode groups **230**G, the fourth electrode groups **240**G, and the dummy patterns DMP may have a mesh structure. Each of the mesh structures may include a plurality of mesh lines. Each of the plurality of mesh lines has a form extending in a corresponding direction and may be connected to each other. The form may have various forms, such as a straight line, a line having a protrusion, or a uneven line. Openings, in which a mesh structure is not located, may be defined (provided or formed) in each of the first electrode groups **210**G, the second electrode groups **220**G, the third electrode groups **230**G, the fourth electrode groups **240**G, and/or the dummy patterns DMP.

[0221] FIGS. **11**A and **11**B illustrate a mesh structure including mesh lines extending in a first crossing direction CDR**1** crossing the first direction DR**1** and the second direction DR**2**, and mesh lines extending in a second crossing direction CDR**2** crossing the first crossing direction CDR**1**. However, the extending direction of the mesh lines constituting the mesh structure is not particularly limited to those illustrated in FIGS. **11**A and **11**B. For example, the mesh structure may include only mesh lines extending in the first direction DR**1** and the second direction DR**2**, or may include mesh lines extending in the first direction DR**1**, the second direction DR**2**, the first crossing direction CDR**1**, and the second crossing direction CDR**2**. In other words, the mesh structure may be changed in various forms.

[0222] FIG. **12** is a plan view of a sensor layer **200**-**1** according to one or more embodiments of the present disclosure. In the following description with reference to FIG. **12**, components described with reference to FIG. **7** are assigned with the same reference numerals, and the details thereof will be omitted.

[0223] Referring to FIG. **12**, the sensor layer **200**-**1** may include the plurality of first electrode groups **210**G, the plurality of second electrode groups **220**G, the plurality of third electrode groups **230**G, and a plurality of fourth electrode groups **240**G-**1** located in the sensing region **200**A.

[0224] FIG. **12** illustrates two fourth electrode groups **240**G-**1** facing each other in the first direction DR**1**. The fourth electrode groups **240**G-**1** may include a (4-1)-th electrode group **240**G-**1***a* overlapped with the first divided electrodes **220**-D**1** of the second electrode groups **220**G, and a (4-2)-th electrode group **240**G-**1***b* overlapped with the second divided electrodes **220**-D**2** of the second electrode groups **220**G. The (4-1)-th electrode group **240**G-**1***a* includes a plurality of (2-1)-th auxiliary electrodes **240**S**1** arranged in the second direction DR**2**, and the (4-2)-th electrode group **240**G-**1***b* may include a plurality of (2-2)-th auxiliary electrodes **240**S**2** arranged in the second direction DR**2**.

[0225] The sensor layer **200**-**1** may further include fourth trace lines **240***t*-**1** and **240***t*-**2** located in the peripheral region **200**NA. All of the (2-1)-th auxiliary electrodes **240**S**1** included in the (4-1)-th electrode group **240**G-**1***a* are electrically connected to the (4-1)-th trace lines **240***t*-**1**, and all of the (2-2)-th auxiliary electrodes **240**S**2** included in the (4-2)-th electrode group **240**G-**1***b* may be electrically connected to the (4-2)-th trace lines **240***t*-**2**.

[0226] According to one or more embodiments of the present disclosure, routing directions of the first divided electrodes **220**-D**1** and the (2-1)-th auxiliary electrodes **240**S**1** overlapped each other may be different from each other. In addition, the routing directions of the second divided electrodes **220**-D**2** and the (2-2)-th auxiliary electrodes **240**S**2** overlapped each other may be different from each other. The routing directions different from each other refers to the connection positions of the electrodes and the trace lines being different from each other.

[0227] FIG. **13**A is a view illustrating an operation of the sensor driver **200**C (see FIG. **5**) according to one or more embodiments of the present disclosure. FIG. **13**B is a view illustrating an operation of the sensor driver **200**C (see FIG. **5**) according to one or more embodiments of the present disclosure.

[0228] Referring to FIGS. **5** and **13**A, the sensor driver **200**C may be selectively driven in any one of a first operation mode DMD**1**, a second operation mode DMD**2**, or a third operation mode DMD**3**.

[0229] The first operation mode DMD**1** may be referred to as a touch-and-pen-standby mode, the second operation mode DMD**2** may be referred to as a touch-activation-and-pen-standby mode, and the third operation mode DMD**3** may be referred to as a pen activation mode. The first operation mode DMD**1** may be a mode for waiting for the first input **2000** and the second input **3000**. The second operation mode DMD**2** may be a mode for sensing the first input **2000** and waiting for the second input **3000**. The third operation mode DMD**3** may be a mode for sensing the second input **3000**.

[0230] According to one or more embodiments of the present disclosure, the sensor driver **200**C

may be first driven in the first operation mode DMD**1**. When the first input **2000** is sensed in the first operation mode DMD**1**, the sensor driver **200**C may be switched (or changed) to the second operation mode DMD**2**. Alternatively, when the second input **3000** is sensed in the first operation mode DMD**1**, the sensor driver **200**C may be switched (or changed) to the third operation mode DMD**3**.

[0231] According to one or more embodiments of the present disclosure, when the second input **3000** is sensed in the second operation mode DMD**2**, the sensor driver **200**C may be switched to the third operation mode DMD**3**. When the first input **2000** is released (or not sensed) in the second operation mode DMD**2**, the sensor driver **200**C may be switched to the first operation mode DMD**1**. When the second input **3000** is released (or not sensed) in the third operation mode DMD**3**, the sensor driver **200**C may be switched to the first operation mode DMD**1**.

[0232] Referring to FIGS. **5**, **13**A, and **13**B, operations in the first to third operation modes DMD**1**, DMD**2**, and DMD**3** are illustrated in order of time (t).

[0233] In the first operation mode DMD**1**, the sensor driver **200**C may be repeatedly driven in a second mode MD**2**-*d* and a first mode MD**1**-*d*. During the second mode MD**2**-*d*, the sensor layer **200** may be scan-driven to detect the second input **3000**. During the first mode MD**1**-*d*, the sensor layer **200** may be scanned and driven to detect the first input **2000**. Although FIG. **13**B illustrates that the sensor driver **200**C operates in the first mode MD**1**-*d* subsequent to the second mode MD**2**-*d*, the operating order of the sensor driver **200**C is not limited thereto.

[0234] In the second operation mode DMD**2**, the sensor driver **200**C may be repeatedly driven in the second mode MD**2**-*d* and a first mode MD**1**. During the second mode MD**2**-*d*, the sensor layer **200** may be scanned and driven to detect the second input **3000**. During the first mode MD**1**, the sensor layer **200** may be scanned and driven to detect coordinates formed by the first input **2000**.

[0235] In the third operation mode DMD**3**, the sensor driver **200**C may be driven in a second mode MD**2**. During the second mode MD**2**, the sensor layer **200** may be scanned and driven to detect coordinates formed by the second input **3000**. In the third operation mode DMD**3**, the sensor driver **200**C may not operate in the first mode MD**1**-*d* or MD**1** until the second input **3000** is released (or not detected).

[0236] Referring also to FIG. **7**, during the first mode MD**1**-*d* of the first operation mode DMD**1** and the first mode MD**1** of the second operation mode DMD**2**, the third electrode groups **230**G and the fourth electrode group **240**G may be grounded, or may receive a constant voltage. Alternatively, during the first mode MD**1**-*d* and the first mode MD**1**, the third electrode groups **230**G and the fourth electrode group **240**G may be floated. Alternatively, during the first mode MD**1**-*d* and the first mode MD**1**, the third electrode groups **230**G and the fourth electrode group **240**G may receive a signal in phase with a signal applied to the first electrode groups **210**G. In this case, touch noise may be reduced or prevented from being introduced through the third electrode groups **230**G and the fourth electrode group **240**G.

[0237] In the second mode MD**2**-*d* of the first operation mode DMD**1** or the second operation mode DMD**2** and the second mode MD**2** of the third operation mode DMD**3**, one end of each of the third electrode groups **230**G and the fourth electrode group **240**G may be floated. In addition, in the second mode MD**2**-*d* and the second mode MD**2**, an opposite end of each of the third electrode groups **230**G and the fourth electrode group **240**G may be grounded or floated. Accordingly, compensation of the sensing signal may be maximized due to coupling between the first electrode groups **210**G and the third electrode groups **230**G, and due to coupling between the second electrode groups **220**G and the fourth electrode groups **240**G.

[0238] FIG. **14** is a view illustrating a first mode according to one or more embodiments of the present disclosure.

[0239] Referring to FIGS. **5**, **13**B, and **14**, the first mode MD**1**-*d* in the first operation mode DMD**1** and the first mode MD**1** in the second operation mode DMD**2** may include a mutual capacitance detection mode. FIG. **14** is a view illustrating describing a mutual capacitance detection mode in

the first mode MD**1**-*d* of the first operation mode DMD**1** and the first mode MD**1** of the second operation mode DMD**2**.

[0240] In the mutual capacitance detection mode, the sensor driver **200**C may sequentially apply transmit signals TX to the first electrode groups **210**G, and may detect coordinates for the first input **2000** by using a receive signal RX detected through the second electrode groups **220**G. For example, the sensor driver **200**C may be configured to calculate an input coordinate by sensing a change in mutual capacitance between the first electrode groups **210**G and the second electrode groups **220**G.

[0241] FIG. **14** illustrates that the transmit signal TX is applied to one first electrode group **210**G, and that the receive signal RX is output from the second electrode groups **220**G. To clarify a signal expression, one first electrode group **210**G applied with the transmit signal TX is displayed in bold in FIG. **14**. The sensor driver **200**C may detect input coordinates for the first input **2000** by sensing the change in capacitance between the first electrode groups **210**G and the second electrode groups **220**G.

[0242] According to one or more embodiments of the present disclosure, at least one of the first mode MD**1**-*d* of the first operation mode DMD**1** or the first mode MD**1** of the second operation mode DMD**2** may further include a mode (self-capacitance detection mode) for detecting self-capacitance. The sensor driver **200**C may be configured to output driving signals to the first electrode groups **210**G and the second electrode groups **220**G in the self-capacitance detection mode, and to calculate input coordinates by sensing the change in capacitance of each of the first electrode groups **210**G and the second electrode groups **220**G. The operation for outputting the driving signals to the first electrode groups **210**G and the second electrode groups **220**G may be separately operated in mutually different timings, or may temporally overlap each other.

[0243] FIG. **15** is a view illustrating a second mode according to one or more embodiments of the present disclosure. FIG. **15** is a view illustrating a second mode (e.g., a charging driving mode), according to one or more embodiments of the present disclosure. FIG. **16**A is a graph illustrating a waveform of a first signal according to one or more embodiments of the present disclosure. FIG. **16**B is a graph illustrating a waveform of a second signal according to one or more embodiments of the present disclosure.

[0244] Referring to FIGS. **15**, **16**A, and **16**B, the second mode MD**2** may include the charging driving mode. The charging driving mode may include a search-charging driving mode and a tracking-charging driving mode.

[0245] The search-charging driving mode may be a driving mode before sensing the position of the pen. Accordingly, a first signal SG**1** or a second signal SG**2** may be provided to all channels included in the sensor layer **200**. In other words, in the search-charging driving mode, the entire area of the sensor layer **200** may be scanned. When the pen PN is sensed in the search-charging driving mode, the sensor layer **200** may be driven in the tracking-charging driving mode. For example, in the tracking-charging driving mode, the sensor driver **200**C may sequentially output the first signal SG**1** and the second signal SG**2** to a region overlapped with a point where the pen PN is sensed, instead of the entire portion of the sensor layer **200**.

[0246] In the charging driving mode, the sensor driver **200**C may apply the first signal SG**1** to a first pad of the third pads PD**3** and the fifth pads PD**5**, and may apply the second signal SG**2** to a second pad, which is different from the first pad, of the third pads PD**3** and the fifth pads PD**5**. The second signal SG**2** may have a phase that is inverse to the phase of the first signal SG**1**. For example, the first signal SG**1** may be a sinusoidal signal.

[0247] Because the first signal SG**1** and the second signal SG**2** are applied to the at least two pads, a current RFS may have a current path formed from the first pad to the second pad. In addition, because the first signal SG**1** and the second signal SG**2** are sinusoidal signals in an inverse phase relationship, the direction of the current RFS may be periodically changed. According to one or more embodiments of the present disclosure, the first signal SG**1** and the second signal SG**2** may

be square wave signals having phases that are inverse to each other.
[0248] When the first signal SG**1** and the second signal SG**2** have phases that are inverse to each other, noise caused to the display layer **100** (see FIG. **4**) by the first signal SG**1** may be canceled by noise caused by the second signal SG**2**. Accordingly, a flicker phenomenon may not occur in the display layer **100**, and display quality of the display layer **100** may be improved.
[0249] According to one or more embodiments of the present disclosure, the first signal SG**1** may be a sinusoidal signal. However, the present disclosure is not limited thereto, and the first signal SG**1** may be a square wave signal. In addition, the second signal SG**2** may have a corresponding constant voltage. For example, the second signal SG**2** may be a ground voltage. In other words, the pad to receive the second signal SG**2** may be considered to be grounded. Even in this case, the current RFS may flow from the first pad to the second pad. In addition, even if the second pad is grounded, the direction of the current RFS may be periodically changed because the first signal SG**1** is a sinusoidal wave signal or a square wave signal.
[0250] FIG. **15** illustrates that the first signal SG**1** is applied to one third pad PD**3** connected to one third trace line **230***rt***1**, and the second signal SG**2** is applied to one fifth pad PD**5** connected to the fifth trace line **230***rt***2**. The current RFS may flow through a current path defined by the fifth pad PD**5**, the fifth trace line **230***rt***2** connected to the fifth pad PD**5**, the third electrode group **230**G, a portion of a third trace line **230***rt***1** connected to the third pad PD**3**, and the third pad PD**3**. The current path may have a coil shape. Accordingly, in the charging driving mode of the second mode, the resonant circuit of the pen PN may be charged by the current path.
[0251] According to the present disclosure, the current path in a loop coil pattern may be implemented by the components included in the sensor layer **200**. Accordingly, the electronic device **1000** (see FIG. **1**A) may charge the pen PN by using the sensor layer **200**. Accordingly, because a component having a coil to charge the pen PN does not need to be separately added, an increase in thickness of the electronic device **1000**, an increase in weight of the electronic device **1000**, and a decrease in flexibility of the electronic device **1000** may be not made.
[0252] In the charging driving mode, the first electrode groups **210**G, the second electrode groups **220**G, and the fourth electrode group **240**G may be grounded, may receive a constant voltage, or may be electrically floated. For example, the first electrode groups **210**G, the second electrode groups **220**G, and the fourth electrode group **240**G may be floated. In this case, the current RFS may not flow to the first electrode groups **210**G, the second electrode groups **220**G, and the fourth electrode group **240**G.
[0253] FIG. **17**A is a view illustrating a second mode according to one or more embodiments of the present disclosure. FIG. **17**B is a view illustrating a second mode according to one or more embodiments of the present disclosure.
[0254] Referring to FIGS. **17**A and **17**B, the second mode may include the charging driving mode and the pen-sensing driving mode. FIGS. **17**A and **17**B are views illustrating the pen-sensing driving mode. FIG. **17**B illustrates an equivalent circuit view of some components of the single sensor layer **200** through which the first to fourth induction currents Ia, Ib, Ic, and Id generated by the pen PN flow.
[0255] An RLC resonance circuit of the pen PN may discharge a magnetic field having a resonance frequency while discharging charges. By the magnetic field provided through the pen PN, the first induction current Ia may be generated from the first electrode group **210**G, and second induction currents Ib and Ib**1** may be generated from the second electrode group **220**G. In addition, the third induction current Ic may be generated from the third electrode group **230**G, and the fourth induction current Id may be generated from the fourth electrode group **240**G.
[0256] According to one or more embodiments of the present disclosure, the second electrode group **220**G includes the first divided electrode **220**-D**1** and the second divided electrode **220**-D**2**, and the first divided electrode **220**-D**1** and the second divided electrode **220**-D**2** are connected to the (2-1)-th trace line **220***t***1** and the (2-2)-th trace line **220***t***2**, respectively. Accordingly, the first

divided electrode **220**-D**1** and the second divided electrode **220**-D**2** in one second electrode group **220**G, which sense along the same axis, are connected to the (2-1)-th trace line **220***t***1** and the (2-2)-th trace line **220***t***2**, respectively, such that a likelihood of the second induction currents Ib and Ib**1** being canceled may be reduced or prevented.

[0257] A first coupling capacitor Ccp**1** may be formed between the third electrode group **230**G and the first electrode group **210**G, and a second coupling capacitor Ccp**2** may be formed between the fourth electrode group **240**G and the first divided electrode **220**-D**1** of the second electrode group **220**G. The third induction current Ic may be applied to the first electrode group **210**G through the first coupling capacitor Ccp**1**, and the fourth induction current Id may be applied to the first divided electrode **220**-D**1** through the second coupling capacitor Ccp**2**.

[0258] The sensor driver **200**C may receive a first receive signal PRX**1***a* based on the first induction current Ia and the third induction current Ic from the first divided electrode **220**-D**1** of the second electrode group **220**G, and may receive a second receive signal PRX**2***a* based on the second induction current Ib and the fourth induction current Id from the first divided electrode **220**-D**1** of the second electrode group **220**G. In addition, the sensor driver **200**C may receive a third receive signal PRX**2***a-ad* based on the second induction current Ib**1** from the second divided electrode **220**-D**2** of the second electrode group **220**G. The sensor driver **200**C may detect the input coordinates of the pen PN based on the first receive signal PRX**1***a*, the second receive signal PRX**2***a*, and the third receive signal PRX**2***a-ad*.

[0259] According to one or more embodiments of the present disclosure, the ends of the third electrode group **230**G and the fourth electrode group **240**G may be floated. Accordingly, compensation of the sensing signal may be maximized due to coupling between the first electrode group **210**G and the third electrode group **230**G, and due to coupling between the first divided electrode **220**-D**1** and the fourth electrode group **240**G.

[0260] In addition, opposite ends of the third electrode group **230**G and the fourth electrode group **240**G may be grounded or floated. Accordingly, the third induction current Ic and the fourth induction current Id may be sufficiently applied to the first electrode group **210**G and the first divided electrode **220**-D**1** due to coupling between the first electrode group **210**G and the third electrode group **230**G and the coupling between the first divided electrode **220**-D**1** and the fourth electrode group **240**G.

[0261] FIG. **18**A is a view illustrating a partial configuration of a sensor layer according to one or more embodiments of the present disclosure. FIG. **18**B is an equivalent circuit diagram of an input device and a sensor layer according to one or more embodiments of the present disclosure.

[0262] Referring to FIGS. **7**, **18**A, and **18**B, the second electrode groups **220**G may include a (2-1)-th electrode group **220**G**1**, a (2-2)-th electrode group **220**G**2**, a (2-3)-th electrode group **220**G**3**, a (2-4)-th electrode group **220**G**4**, and a (2-5)-th electrode group **220**G**5** sequentially arranged in the second direction DR**2**.

[0263] The (2-1)-th electrode group **220**G**1** may include a (1-1)-th divided electrode **220**-D**11**, and a (2-1)-th divided electrode **220**-D**21** spaced apart from the (1-1)-th divided electrode **220**-D**11** in the first direction DR**1**. The (2-2)-th electrode group **220**G**2** may include a (1-2)-th divided electrode **220**-D**12**, and a (2-2)-th divided electrode **220**-D**22** spaced apart from the (1-2)-th divided electrode **220**-D**12** in the first direction DR**1**. The (2-3)-th electrode group **220**G**3** may include a (1-3)-th divided electrode **220**-D**13**, and a (2-3)-th divided electrode **220**-D**23** spaced apart from the (1-3)-th divided electrode **220**-D**13** in the first direction DR**1**. The (2-4)-th electrode group **220**G**4** may include a (1-4)-th divided electrode **220**-D**14**, and a (2-4)-th divided electrode **220**-D**24** spaced apart from the (1-4)-th divided electrode **220**-D**14** in the first direction DR**1**. The (2-5)-th electrode group **220**G**5** may include a (1-5)-th divided electrode **220**-D**15**, and a (2-5)-th divided electrode **220**-D**25** spaced apart from the (1-5)-th divided electrode **220**-D**15** in the first direction DR**1**.

[0264] The second trace lines **220***t* include a (1-1)-th divided trace line **220***t***11** electrically connected to the (1-1)-th divided electrode **220**-D**11**, a (2-1)-th divided trace line **220***t***21**

electrically connected to the (2-1)-th divided electrode **220**-D**21**, a (1-2)-th divided trace line **220***t***12** electrically connected to the (1-2)-th divided electrode **220**-D**12**, a (2-2)-th divided trace line **220***t***22** electrically connected to the (2-2)-th divided electrode **220**-D**22**, a (1-3)-th divided trace line **220***t***13** electrically connected to the (1-3)-th divided electrode **220**-D**13**, a (2-3)-th divided trace line **220***t***23** electrically connected to the (2-3)-th divided electrode **220**-D**23**, a (1-4)-th divided trace line **220***t***14** electrically connected to the (1-4)-th divided electrode **220**-D**14**, a (2-4)-th divided trace line **220***t***24** electrically connected to the (2-4)-th divided electrode **220**-D**24**, a (1-5)-th divided trace line **220***t***15** electrically connected to the (1-5)-th divided electrode **220**-D**15**, and a (2-5)-th divided trace line **220***t***25** electrically connected to the (2-5)-th divided electrode **220**-D**25**.

[0265] The (1-1)-th divided electrode **220**-D**11** may be referred to as a first divided electrode, the (2-1)-th divided electrode **220**-D**21** may be referred to as a second divided electrode, the (1-2)-th divided electrode **220**-D**12** may be referred to as a third divided electrode, and the (2-2)-th divided electrode **220**-D**22** may be referred to as a fourth divided electrode. The (1-1)-th divided trace line **220***t***11** may be referred to as a first line or a (2-1)-th trace line, the (2-1)-th divided trace line **220***t***21** may be referred to as a second line or a (2-2)-th trace line, and the (1-2)-th divided trace line **220***t***12** may be referred to as a third line or a (2-3)-th trace line, and the (2-2)-th divided trace line **220***t***22** may be referred to as a fourth line or a (2-4)-th trace line.

[0266] According to one or more embodiments of the present disclosure, the (1-1)-th divided trace line **220***t***11**, the (2-1)-th divided trace line **220***t***21**, the (1-2)-th divided trace line **220***t***12**, the (2-2)-th divided trace line **220***t***22**, the (1-3)-th divided trace line **220***t***13**, and the (2-3)-th divided trace line **220***t***23** may be sequentially arranged in the first direction DR**1**.

[0267] According to one or more embodiments of the present disclosure, a gap TS**1** between the (1-1)-th divided trace line **220***t***11** and the (2-1)-th divided trace line **220***t***21** connected to the (1-1)-th divided electrode **220**-D**11** and the (2-1)-th divided electrode **220**-D**21**, respectively, and which sense the same axis and belong to one (2-1)-th electrode group **220**G**1**, may be smaller than a gap TS**2** between the (1-2)-th divided trace line **220***t***12** and the (2-1)-th divided trace line **220***t***21** connected to the (1-2)-th divided electrode **220**-D**12** and the (2-1)-th divided electrode **220**-D**21**, respectively, which belong to the (2-2)-th electrode group **220**G**2** to sense an axis that is different from that of the (2-1)-th electrode group **220**G**1**.

[0268] According to one or more embodiments of the present disclosure, signals provided from the (1-1)-th divided trace line **220***t***11** and the (2-1)-th divided trace line **220***t***21** may be sensed differentially. In this case, mutual inductance of a trace line, which affects the distortion of coordinate, may be removed. As the gap between the (1-1)-th divided trace line **220***t***11** and the (2-1)-th divided trace line **220***t***21** decreases, a first coupling constant K0 of the (1-1)-th divided trace line **220***t***11** and a second coupling constant K1 of the (2-1)-th divided trace line **220***t***21** may be substantially equal to each other. Accordingly, as the (1-1)-th divided trace line **220***t***11** and the (2-1)-th divided trace line **220***t***21** are closer to each other, the mutual inductance may be more effectively removed.

[0269] According to one or more embodiments of the present disclosure, the width of the (1-1)-th divided electrode **220**-D**11** in the first direction DR**1** may be narrower than the width of the (1-2)-th divided electrode **220**-D**12** in the first direction DR**1**, and the width of the (2-1)-th divided electrode **220**-D**21** in the first direction DR**1** may be wider than the width of the (2-2)-th divided electrode **220**-D**22** in the first direction DR**1**. The (1-1)-th divided trace line **220***t***11** and the (2-1)-th divided trace line **220***t***21** may overlap any one of the (1-2)-th divided electrode **220**-D**12** or the (2-2)-th divided electrode **220**-D**22**. For example, the (1-1)-th divided trace line **220***t***11** and the (2-1)-th divided trace line **220***t***21** may overlap the (1-2)-th divided electrode **220**-D**12**.

[0270] The width of the (1-3)-th divided electrode **220**-D**13** in the first direction DR**1** may be wider than the width of the (1-2)-th divided electrode **220**-D**12** in the first direction DR**1**, and the width of the (2-3)-th divided electrode **220**-D**23** in the first direction DR**1** may be narrower than the width

of the (2-2)-th divided electrode **220**-D**22** in the first direction DR**1**. Accordingly, when viewed from the second direction DR**2**, a gap GP between the (1-3)-th divided electrode **220**-D**13** and the (2-3)-th divided electrode **220**-D**23** may be overlapped (e.g., along a second direction DR**2**) with the (2-1)-th divided electrode **220**-D**21** and the (2-2)-th divided electrode **220**-D**22**.

[0271] FIG. **19** is a view illustrating the sensor driver **200**C according to one or more embodiments of the present disclosure. In FIG. **19**, the operation of the sensor driver **200**C in the pen-sensing driving mode will be described.

[0272] Referring to FIGS. **17**A, **18**A, and **19**, the sensor driver **200**C may differentially sense signals received from two different electrode groups. For example, a signal received from the (2-1)-th electrode group **220**G**1** and a signal received from the (2-2)-th electrode group **220**G**2** may be differentially sensed.

[0273] According to one or more embodiments of the present disclosure, the second trace lines **220***t* overlap the sensing region **200**A. In other words, as compared to the case where the second trace lines are located in the peripheral region **200**NA, the second trace lines **220***t* are widely spread in the sensing region **200**A, and mutual inductances between the pen PN and the second trace lines **220***t* may be different from each other. Accordingly, unlike one or more embodiments of the present disclosure, when the (2-1)-th electrode group **220**G**1** and the (2-2)-th electrode group **220**G**2** are directly differentially sensed, the influence by the second trace lines **220***t* is not removed, so that coordinates may be distorted.

[0274] According to one or more embodiments of the present disclosure, before differentially sensing signals received from two different electrode groups, a primary differential sensing operation may be performed to remove the influence by the second trace lines **220***t*. Mutual inductances of the second trace lines **220***t* that affect the distortion of coordinates may be removed by the primary differential sensing operation. Accordingly, the accuracy of coordinates sensed by the sensor layer **200** and the sensor driver **200**C may be improved. Hereinafter, the operation of the sensor driver **200**C will be described in detail.

[0275] The sensor driver **200**C may include a first differential processing circuit **210**C, a second differential processing circuit **220**C, and a third differential processing circuit **230**C. The first differential processing circuit **210**C and the second differential processing circuit **220**C may be circuits that perform the primary differential sensing operation to remove the mutual inductances of the second trace lines **220***t*. The third differential processing circuit **230**C may be a circuit to perform a secondary differential sensing operation with respect to signals received from two different electrode groups.

[0276] The first differential processing circuit **210**C may be configured to receive a first signal PSG**1** from the (1-1)-th divided trace line **220***t***11** connected to the (2-1)-th electrode group **220**G**1**, and a second signal PSG**2** from the (2-1)-th divided trace line **220***t***21**, to perform a differential computing operation with respect to the first signal PSG**1** and the second signal PSG**2**, thereby generating first data AD**1**.

[0277] The second differential processing circuit **220**C may be configured to receive a third signal PSG**3** from the (1-2)-th divided trace line **220***t***12** connected to another second electrode group, for example, the (2-2)-th electrode group **220**G**2**, and a fourth signal PSG**4** from the (2-2)-th divided trace line **220***t***22**, and to perform a differential computing operation with respect to the third signal PSG**3** and the fourth signal PSG**4**, thereby generating second data AD**2**.

[0278] The third differential processing circuit **230**C may be configured to perform a differential computing operation with respect to the first data AD**1** and the second data AD**2** to generate third data CHD.

[0279] The sensor driver **200**C may be configured to generate the first data AD**1** and the second data AD**2** through at least one of analog differential processing or digital differential processing, and may be configured to generate the third data CHD using at least one of the analog differential processing or the digital differential processing. According to one or more embodiments of the

present disclosure, the sensor driver **200**C may generate the first data AD**1** and the second data AD**2** through the analog differential processing, and may generate the third data CHD through the digital differential processing.

[0280] The first differential processing circuit **210**C may include a first charge voltage amplifier AP**1** and a first current conveyor CC**1**. The second differential processing circuit **220**C may include a second charge voltage amplifier AP**2** and a second current conveyor CC**2**. The third differential processing circuit **230**C may include an analog-to-digital converter ADC and a differential computing unit DCC. The components included in each of the first differential processing circuit **210**C, the second differential processing circuit **220**C, and the third differential processing circuit **230**C are not limited to the above-described components. At least some of the above-described components may be omitted, or other components may be added. In addition, the order of connection of the components included in each of the first differential processing circuit **210**C, the second differential processing circuit **220**C, and the third differential processing circuit **230**C may be changed.

[0281] The first differential processing circuit **210**C may receive the first signal PSG**1** and the second signal PSG**2**, and may perform the differential computing operation with respect to the first signal PSG**1** and the second signal PSG**2** to generate the first data AD**1**. The second differential processing circuit **220**C may receive the third signal PSG**3** and the fourth signal PSG**4**, and may perform the differential operation on the third signal PSG**3** and the fourth signal PSG**4** to generate the second data AD**2**. The step of generating the first data AD**1** and the second data AD**2** may be referred to as the primary differential processing operation. Mutual inductance affecting the distortion of coordinates may be removed by the primary differential processing operation.

[0282] The analog-to-digital converter ADC of the third differential processing circuit **230**C may convert the first data AD**1** and the second data AD**2** to output first digital data DID**1** and second digital data DID**2**, respectively. A first weight GA**1** may be applied to the first digital data DID**1**, and a second weight GA**2** may be applied to the second digital data DID**2**. The first weight GA**1** and the second weight GA**2** may be the same or different from each other.

[0283] First weighted data obtained by applying the first weight GA**1** to the first digital data DID**1** and second weighted data obtained by applying the second weight GA**2** to the second digital data DID**2** may be provided to the differential computing unit DCC. The differential computing unit DCC may perform a computing operation with respect to the first weighted data and the second weighted data to output the third data CHD.

[0284] FIG. **20** is a view illustrating a sensor driver **200**C-**1** according to one or more embodiments of the present disclosure. In the following description with reference to FIG. **20**, components described with reference to FIG. **19** are assigned with the same reference numerals, and the details thereof will be omitted.

[0285] Referring to FIG. **20**, the sensor driver **200**C-**1** may include a first differential processing circuit **210**C**1**, a second differential processing circuit **220**C**1**, and a third differential processing circuit **230**C**1**.

[0286] The sensor driver **200**C-**1** may be configured to generate first data DID**1***a* and second data DID**2***a* through at least one of analog differential processing or digital differential processing, and may be configured to generate third data CHDa through at least one of the analog differential processing or the digital differential processing.

[0287] According to one or more embodiments of the present disclosure, the sensor driver **200**C-**1** may generate the first data DID**1***a* and the second data DID**2***a* through the digital differential processing, and may generate the third data CHDa through the digital differential processing.

[0288] The first differential processing circuit **210**C**1** may include an analog-to-digital converter ADC and a first differential computing unit DCC**1**. The second differential processing circuit **220**C**1** may include an analog-to-digital converter ADC and a second differential computing unit DCC**2**. The third differential processing circuit **230**C**1** may include a third differential computing

unit DCC**3**. Components included in each of the first to third differential processing circuits **210**C**1**, **220**C**1**, and **230**C**1** are not limited to the above-described components. At least some of the above-described components may be omitted, or other components may be added.

[0289] The first differential processing circuit **210**C**1** may receive the first signal PSG**1** and the second signal PSG**2**, and may perform analog-to-digital conversion with respect to the first signal PSG**1** and the second signal PSG**2** to generate first digital data DI**1** and second digital data DI**2**. A first weight GA**1***a* may be applied to the first digital data DI**1**, and a second weight GA**2***a* may be applied to the second digital data DI**2**. The first weight GA**1***a* and the second weight GA**2***a* may be the same, or may be different from each other. The first differential computing unit DCC**1** may output the first data DID**1***a* by performing a computing operation with respect to the first digital data DI**1** and the second digital data DI**2** applied with the first weight GA**1***a* and the second weight GA**2***a*, respectively.

[0290] The second differential processing circuit **220**C**1** may receive the third signal PSG**3** and the fourth signal PSG**4**, and may perform analog-to-digital conversion with respect to the third signal PSG**3** and the fourth signal PSG**4** to generate third digital data DI**3** and fourth digital data DI**4**. A first weight GA**1***b* may be applied to the third digital data DI**3**, and a second weight GA**2***b* may be applied to the fourth digital data DI**4**. The first weight GA**1***b* and the second weight GA**2***b* may be the same, or may be different from each other. The second differential computing unit DCC**2** may output the second data DID**2***a* by performing a computing operation with respect to the third digital data DI**3** and the fourth digital data DI**4** applied with the first weight GA**1***b* and the second weight GA**2***b*, respectively.

[0291] The third differential processing circuit **230**C**1** may receive the first data DID**1***a* and the second data DID**2***a*. A third weight GA**3** may be applied to the first data DID**1***a*, and a fourth weight GA**4** may be applied to the second data DID**2***a*. The third weight GA**3** and the fourth weight GA**4** may be the same, or may be different from each other. The third differential computing unit DCC**3** may output the third data CHDa by performing a computing operation with respect to the first data DID**1***a* and the second data DID**2***a* applied with the third weight GA**3** and the fourth weight GA**4**, respectively.

[0292] FIG. **21** is a view illustrating a sensor driver **200**C-**2** according to one or more embodiments of the present disclosure. In the following description with reference to FIG. **21**, components described with reference to FIG. **19** are assigned with the same reference numerals, and the details thereof will be omitted.

[0293] Referring to FIG. **21**, the sensor driver **200**C-**2** may include the first differential processing circuit **210**C, the second differential processing circuit **220**C, and a third differential processing circuit **230**C**2**.

[0294] The sensor driver **200**C-**2** may be configured to generate the first data AD**1** and the second data AD**2** through at least one of analog differential processing or digital differential processing, and may be configured to generate third data CHDb through at least one of the analog differential processing or the digital differential processing. According to one or more embodiments of the present disclosure, the sensor driver **200**C-**2** may generate the first data AD**1** and the second data AD**2** through the analog differential processing, and may generate the third data CHDb through the analog differential processing.

[0295] The third differential processing circuit **230**C**2** may include a third charge voltage amplifier AP**3**, a third current conveyor CC**3**, and an analog-to-digital converter ADC. The components included in the third differential processing circuit **230**C are not limited to the above-described components. At least some of the above-described components may be omitted, and other components may be added. In addition, the connection order of the components included in the third differential processing circuit **230**C may be changed.

[0296] The third charge voltage amplifier AP**3** of the third differential processing circuit **230**C may receive the first data AD**1** and the second data AD**2**, and may perform the differential computing

operation with respect to the first data AD**1** and the second data AD**2** to generate third intermediate data AD**3**. The analog-to-digital converter ADC may convert the third intermediate data AD**3** to output the third data CHDb.

[0297] FIG. **22**A is a plan view of a sensor layer **200-2** according to one or more embodiments of the present disclosure. FIG. **22**B is a view illustrating some components of a sensor layer according to one or more embodiments of the present disclosure. In the following description with reference to FIG. **22**A, components described with reference to FIG. **7** are assigned with the same reference numerals, and the details thereof will be omitted.

[0298] Referring to FIGS. **22**A and **22**B, the sensor layer **200-2** may include the plurality of first electrode groups **210**G, a plurality of second electrode groups **220**Ga, the plurality of third electrode groups **230**G, and the fourth electrode group **240**G.

[0299] Each of the second electrode groups **220**Ga may include a first divided electrode **220**-D**1***a* and a second divided electrode **220**-D**2***a*. The first divided electrode **220**-D**1***a* and the second divided electrode **220**-D**2***a* may be spaced apart from each other in the first direction DR**1**. Each of the first divided electrode **220**-D**1***a* and the second divided electrode **220**-D**2***a* may extend in the first direction DR**1**.

[0300] The second electrode groups **220**Ga may include a (2-1)-th electrode group **220**G**1***a*, a (2-2)-th electrode group **220**G**2***a*, a (2-3)-th electrode group **220**G**3***a*, a (2-4)-th electrode group **220**G**4***a*, and a (2-5)-th electrode group **220**G**5***a* sequentially arranged in the second direction DR**2**.

[0301] The (2-1)-th electrode group **220**G**1***a* may include a (1-1)-th divided electrode **220**-D**11***a*, and a (2-1)-th divided electrode **220**-D**21***a* spaced apart from the (1-1)-th divided electrode **220**-D**11***a* in the first direction DR**1**. The (2-2)-th electrode group **220**G**2***a* may include a (1-2)-th divided electrode **220**-D**12***a*, and a (2-2)-th divided electrode **220**-D**22***a* spaced apart from the (1-2)-th divided electrode **220**-D**12***a* in the first direction DR**1**. The (2-3)-th electrode group **220**G**3***a* may include a (1-3)-th divided electrode **220**-D**13***a*, and a (2-3)-th divided electrode **220**-D**23***a* spaced apart from the (1-3)-th divided electrode **220**-D**13***a* in the first direction DR**1**. The (2-4)-th electrode group **220**G**4***a* may include a (1-4)-th divided electrode **220**-D**14***a*, and a (2-4)-th divided electrode **220**-D**24***a* spaced apart from the (1-4)-th divided electrode **220**-D**14***a* in the first direction DR**1**. The (2-5)-th electrode group **220**G**5***a* may include a (1-5)-th divided electrode **220**-D**15***a*, and a (2-5)-th divided electrode **220**-D**25***a* spaced apart from the (1-5)-th divided electrode **220**-D**15***a* in the first direction DR**1**.

[0302] The second trace lines **220***t* include a (1-1)-th divided trace line **220***t***11***a* electrically connected to the (1-1)-th divided electrode **220**-D**11***a*, a (2-1)-th divided trace line **220***t***21***a* electrically connected to the (2-1)-th divided electrode **220**-D**21***a*, a (1-2)-th divided trace line **220***t***12***a* electrically connected to the (1-2)-th divided electrode **220**-D**12***a*, a (2-2)-th divided trace line **220***t***22***a* electrically connected to the (2-2)-th divided electrode **220**-D**22***a*, a (1-3)-th divided trace line **220***t***13***a* electrically connected to the (1-3)-th divided electrode **220**-D**13***a*, a (2-3)-th divided trace line **220***t***23***a* electrically connected to the (2-3)-th divided electrode **220**-D**23***a*, a (1-4)-th divided trace line **220***t***14***a* electrically connected to the (1-4)-th divided electrode **220**-D**14***a*, a (2-4)-th divided trace line **220***t***24***a* electrically connected to the (2-4)-th divided electrode **220**-D**24***a*, a (1-5)-th divided trace line **220***t***15***a* electrically connected to the (1-5)-th divided electrode **220**-D**15***a*, and a (2-5)-th divided trace line **220***t***25***a* electrically connected to the (2-5)-th divided electrode **220**-D**25***a*

[0303] According to one or more embodiments of the present disclosure, the (1-5)-th divided trace line **220***t***15***a*, the (2-5)-th divided trace line **220***t***25***a*, the (1-3)-th divided trace line **220***t***13***a*, the (2-3)-th divided trace line **220***t***23***a*, the (1-1)-th divided trace line **220***t***11***a*, the (2-1)-th divided trace line **220***t***21***a*, the (1-2)-th divided trace line **220***t***12***a*, the (2-2)-th divided trace line **220***t***22***a*, the (1-4)-th divided trace line **220***t***14***a*, and the (2-4)-th divided trace line **220***t***24***a* may be sequentially arranged in the first direction DR**1**.

[0304] According to one or more embodiments of the present disclosure, the width of the (1-1)-th

divided electrode **220**-D**11***a* in the first direction DR**1** may be narrower than the width of the (1-2)-th divided electrode **220**-D**12***a* in the first direction DR**1**, and the width of the (2-1)-th divided electrode **220**-D**21***a* in the first direction DR**1** may be wider than the width of the (2-2)-th divided electrode **220**-D**22***a* in the first direction DR**1**.

[0305] The width of the (1-3)-th divided electrode **220**-D**13***a* in the first direction DR**1** may be narrower than the width of the (1-1)-th divided electrode **220**-D**11***a* in the first direction DR**1**, and the width of the (2-3)-th divided electrode **220**-D**23***a* in the first direction DR**1** may be wider than the width of the (2-1)-th divided electrode **220**-D**21***a* in the first direction DR**1**. Accordingly, when viewed from the second direction DR**2**, a gap GPa between the (1-3)-th divided electrode **220**-D**13***a* and the (2-3)-th divided electrode **220**-D**23***a* may overlap the (1-1)-th divided electrode **220**-D**11***a* and the (1-2)-th divided electrode **220**-D**12***a*.

[0306] FIG. **23** is a plan view of a sensor layer **200-3** according to one or more embodiments of the present disclosure. FIG. **24**A is a view illustrating some components of the sensor layer **200-3** according to one or more embodiments of the present disclosure. FIG. **24**B is a view to describe a second mode according to one or more embodiments of the present disclosure. In the following description with reference to FIG. **23**, components described with reference to FIG. **7** are assigned with the same reference numerals, and the details thereof will be omitted.

[0307] Referring to FIG. **23**, the sensor layer **200-3** may include the plurality of first electrode groups **210**G, a plurality of second electrode groups **220**Gb, the plurality of third electrode groups **230**G, and the fourth electrode group **240**G, which are located in the sensing region **200**A.

[0308] Each of the second electrode groups **220**Gb may include a first divided electrode **220**-D**1***b* and a second divided electrode **220**-D**2***b*. The first divided electrode **220**-D**1***b* and the second divided electrode **220**-D**2***b* may be spaced apart from each other in the first direction DR**1**. Each of the first divided electrode **220**-D**1***b* and the second divided electrode **220**-D**2***b* may extend in the first direction DR**1**.

[0309] The first divided electrodes **220**-D**1***b* may be arranged to be spaced apart from each other in the second direction DR**2**, and the second divided electrodes **220**-D**2***b* may be arranged to be spaced apart from each other in the second direction DR**2**. According to one or more embodiments of the present disclosure, the lengths or the widths of the first divided electrodes **220**-D**1***b* in the first direction DR**1** may be equal to each other, and the lengths or the widths of the second divided electrodes **220**-D**2***b* in the first direction DR**1** may be equal to each other.

[0310] The sensor layer **200-3** may further include second trace lines **220***tb* and **220***tc*. The second trace lines **220***tb* and **220***tc* may include the first divided trace lines **220***tb* and the second divided trace lines **220***tc*. At least some of the first divided trace lines **220***tb* may be electrically connected to the first divided electrodes **220**-D**1***b*, and the second divided trace lines **220***tc* may be electrically connected to the second divided electrodes **220**-D**2***b*.

[0311] According to one or more embodiments of the present disclosure, the first divided trace lines **220***tb* may overlap the sensing region **200**A, and may be insulated from at least some of the second divided electrodes **220**-D**2***b* while crossing the at least some of the second divided electrodes **220**-D**2***b*. The second divided trace lines **220***tc* may be located in the peripheral region **200**NA. However, this is provided only for the illustrative purpose, and at least some of the second divided trace lines **220***tc* may overlap the sensing region **200**A.

[0312] FIG. **24**A illustrates that the first divided electrodes **220**-D**1***b* and the first divided trace lines **220***tb*. Each of the first divided trace lines **220***tb* may include a (2-1)-th trace line **220***t***1***b* electrically connected to the relevant first divided electrode **220**-D**1***b*, and a (2-2)-th trace line **220***t***2***b* spaced apart from (2-1)-th trace line **220***t***1***b* in the first direction DR**1** while extending in the second direction DR**2**. The (2-1)-th trace line **220***t***1***b* may be referred to as a first line, and the (2-2)-th trace line **220***t***2***b* may be referred to as a second line.

[0313] The (2-2)-th trace line **220***t***2***b* may face the (2-1)-th trace line **220***t***1***b*. For example, the (2-1)-th trace line **220***t***1***b* may include a first portion **220***th* extending in the first direction DR**1** and a

second portion **220***tv* extending from the first portion **220***th* in the second direction DR**2**, and the (2-2)-th trace line **220***t***2***b* may face the second portion **220***tv*.

[0314] One end of the (2-1)-th trace line **220***t***1***b* may be connected to the first divided electrode **220**-D**1***b*, and an opposite end of the (2-1)-th trace line **220***t***1***b* may be electrically connected to the sensor driver **200**C through a second pad PD**2***a*. One end of the (2-2)-th trace line **220***t***2***b* may be floated, and an opposite end of the (2-2)-th trace line **220***t***2***b* may be electrically connected to the sensor driver **200**C through a pad PDa. One end of the second divided trace line **220***tc* may be connected to the second divided electrode **220**-D**2***b*, and the opposite end of the second divided trace line **220***tc* may be electrically connected to the sensor driver **200**C through a second pad PD**2***b*.

[0315] Referring to FIGS. **5**, **24**A, and **24**B, the RLC resonance circuit of the pen PN may emit a magnetic field having a resonance frequency while discharging the charges. The first induction current Ia may be generated from the first electrode group **210**G, and the second induction current Ib may be generated from the first divided electrode **220**-D**1***b*, due to the magnetic field provided by the pen PN. In addition, the third induction current Ic may be generated from the third electrode group **230**G, and the fourth induction current Id may be generated from the fourth electrode group **240**G.

[0316] The first coupling capacitor Ccp**1** may be formed between the third electrode group **230**G and the first electrode group **210**G, and the second coupling capacitor Ccp**2** may be formed between the fourth electrode group **240**G and the first divided electrode **220**-D**1***b*. The third induction current Ic may be transferred to the first electrode group **210**G through the first coupling capacitor Ccp**1**, and the fourth induction current Id may be transferred to the first divided electrode **220**-D**1***b* through the second coupling capacitor Ccp**2**.

[0317] The sensor driver **200**C may receive a first receive signal PRX**1***a*, which are based on the first induction current Ia and the third induction current Ic, from the first electrode group **210**G, and may receive a second receive signal PRX**2***a*, which are based on the second induction current Ib and the fourth induction current Id, from the first divided electrode **220**-D**1***b*. In addition, the sensor driver **200**C may receive a third receive signal PRX**2***a-ada* from the (2-2)-th trace line **220***t***2***b*. The sensor driver **200**C may detect coordinates of an input made by the pen PN based on the first receive signal PRX**1***a*, the second receive signal PRX**2***a*, and the third receive signal PRX**2***a-ada*.

[0318] According to one or more embodiments of the present disclosure, a length LT**1** of the (2-1)-th trace line **220***t***1***b* in the second direction DR**2** may be substantially equal to a length LT**2** of the (2-2)-th trace line **220***t***2***b* in the second direction DR**2** in the sensing region **200**A. The sensor driver **200**C may differentially sense the second receive signal PRX**2***a* that is provided through the (2-1)-th trace line **220***t***1***b* and the third receive signal PRX**2***a-ada* that is provided through the (2-2)-th trace line **220***t***2***b*. In this case, mutual inductance affecting the distortion of coordinates may be removed.

[0319] FIG. **25** is a plan view of a sensor layer **200-4** according to one or more embodiments of the present disclosure. In the following description with reference to FIG. **25**, components described with reference to FIG. **7** are assigned with the same reference numerals, and the details thereof will be omitted.

[0320] Referring to FIG. **25**, the sensor layer **200-4** may include the plurality of first electrode groups **210**G, the plurality of second electrode groups **220**Gb, the plurality of third electrode groups **230**G, and a plurality of fourth electrode groups **240**G-**2**.

[0321] The second electrode groups **220**Gb may include the first divided electrode **220**-D**1***b* and the second divided electrode **220**-D**2***b*. The first divided electrode **220**-D**1***b* and the second divided electrode **220**-D**2***b* may be spaced apart from each other in the first direction DR**1**. Each of the first divided electrode **220**-D**1***b* and the second divided electrode **220**-D**2***b* may extend in the first direction DR**1**.

[0322] The first divided electrodes **220**-D**1***b* may be arranged to be spaced apart from each other in the second direction DR**2**, and the second divided electrodes **220**-D**2***b* may be arranged to be spaced apart from each other in the second direction DR**2**. According to one or more embodiments of the present disclosure, the lengths or the widths of the first divided electrodes **220**-D**1***b* in the first direction DR**1** may be equal to each other, and the lengths or the widths of the second divided electrodes **220**-D**2***b* in the first direction DR**1** may be equal to each other.

[0323] The sensor layer **200**-**4** may further include second trace lines **220***tb*-**1** and **220***tc*-**1**. The second trace lines **220***tb*-**1** and **220***tc*-**1** may include the first divided trace lines **220***tb*-**1** and the second divided trace lines **220***tc*-**1**. The first divided trace lines **220***tb*-**1** are electrically connected in one-to-one correspondence to the first divided electrodes **220**-D**1***b*, and the second divided trace lines **220***tc* may be electrically connected in one-to-one correspondence to the second divided electrodes **220**-D**2***b*. The first divided trace line **220***tb*-**1** may be referred to as a (2-1)-th trace line or a first line, and the second divided trace line **220***tc*-**1** may be referred to as a (2-2)-th trace line or a second line.

[0324] According to one or more embodiments of the present disclosure, the first divided trace lines **220***tb*-**1** and the second divided trace lines **220***tc*-**1** may overlap the non-display region **100**NA (see FIG. **4**) or the peripheral region **200**NA. The first divided trace lines **220***tb*-**1** and the second divided trace lines **220***tc*-**1** may be spaced apart from each other while interposing the first divided electrodes **220**-D**1***b* and the second divided electrode **220**-D**2***b* between the first divided trace lines **220***tb*-**1** and the second divided trace lines **220***tc*-**1**.

[0325] The sensor layer **200**-**4** may include two fourth electrode groups **240**G-**2** facing each other in the first direction DR**1**. The fourth electrode groups **240**G-**2** may include a (4-1)-th electrode group **240**G-**2***a* overlapped with the first divided electrodes **220**-D**1***b* and a (4-2)-th electrode group **240**G-**2***b* overlapped with the second divided electrodes **220**-D**2***b*. The (4-1)-th electrode group **240**G-**2***a* includes the plurality of (2-1)-th second auxiliary electrodes **240**S**1***a* arranged in the second direction DR**2**, and the (4-2)-th electrode group **240**G-**2***b* may include the plurality of (2-2)-th second auxiliary electrodes **240**S**2***a* arranged in the second direction DR**2**.

[0326] The sensor layer **200**-**4** may further include a fourth trace line **240***ta* overlapping the sensing region **200**A. The fourth trace line **240***ta* may be located between the (2-1)-th auxiliary electrodes **240**S**1***a* and the (2-2)-th auxiliary electrodes **240**S**2***a*. All of the (2-1)-th auxiliary electrodes **240**S**1***a* and all of the (2-2)-th auxiliary electrodes **240**S**2** may be connected to one fourth trace line **240***ta*.

[0327] As described above, the input made by the pen may be sensed through the sensor layer, as well as the touch input. Accordingly, the electronic device does not need to further include the additional component (for example, a digitizer) for pen sensing. Accordingly, the electronic device may be thinner, lighter, and more flexible as the digitizer is not added. In addition, at least a portion of the trace lines of the sensor layer may overlap the sensing region or the display region. Accordingly, the area of the peripheral region of the sensor layer may be reduced. Accordingly, the area occupied by the peripheral region on the front surface of the electronic device may be reduced, and the narrower bezel may be implemented. In addition, the sensor driver may be configured to perform the primary differential sensing operation for removing the influence by the trace lines before performing the differential sensing with respect to the signal received from the two electrode groups different from each other. The mutual inductance of the trace lines exerting an influence on the distortion of coordinates may be removed through the primary differential sensing operation. Accordingly, the accuracy of coordinates sensed by the sensor layer and the sensor driver may be improved.

[0328] Although one or more embodiments of the present disclosure has been described for illustrative purposes, those skilled in the art will appreciate that various modifications, and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims. Accordingly, the technical scope of the present disclosure is not

limited to the detailed description of this specification, but should be defined by the claims.
[0329] While the present disclosure has been described with reference to embodiments thereof, it will be apparent to those of ordinary skill in the art that various changes and modifications may be made thereto without departing from the spirit and scope of the present disclosure as set forth in the following claims, with functional equivalents thereof to be included therein.

Claims

1. An electronic device comprising: a sensor layer comprising: a sensing region; a peripheral region adjacent to the sensing region; first electrode groups arranged in a first direction; second electrode groups crossing the first electrode groups, and arranged in a second direction crossing the first direction; first trace lines electrically connected to the first electrode groups; and second trace lines electrically connected to the second electrode groups, and comprising: a (2-1)-th trace line electrically connected to one of the second electrode groups, and having a first length in the second direction; and a (2-2)-th trace line spaced apart from the (2-1)-th trace line in the first direction while extending in the second direction, and having a second length in the second direction that is substantially equal to the first length; and a sensor driver configured to drive the sensor layer, and to selectively operate in a first mode for sensing a touch input, or in a second mode for sensing a pen input.
2. The electronic device of claim 1, wherein each of the second electrode groups comprises a first divided electrode, and a second divided electrode spaced apart from the first divided electrode in the first direction, and wherein the (2-1)-th trace line is electrically connected to the first divided electrode, and the (2-2)-th trace line is electrically connected to the second divided electrode.
3. The electronic device of claim 2, wherein at least a portion of the (2-1)-th trace line and a portion of the (2-2)-th trace line overlap the sensing region, wherein the first length of the (2-1)-th trace line overlaps the sensing region, and wherein the second length of the (2-2)-th trace line overlaps the sensing region.
4. The electronic device of claim 2, wherein the (2-1)-th trace line is connected to the first divided electrode adjacent to the second divided electrode, and wherein the (2-2)-th trace line is connected to the second divided electrode adjacent to the first divided electrode.
5. The electronic device of claim 2, wherein the (2-1)-th trace line and the (2-2)-th trace line overlap the peripheral region, and are spaced apart from each other with the first divided electrode and the second divided electrode therebetween.
6. The electronic device of claim 1, wherein the second electrode groups comprise: a (2-1)-th electrode group, a (2-2)-th electrode group, and a (2-3)-th electrode group sequentially arranged in the second direction, wherein the (2-1)-th electrode group comprises a (1-1)-th divided electrode, and a (2-1)-th divided electrode spaced apart from the (1-1)-th divided electrode in the first direction, wherein the (2-2)-th electrode group comprises a (1-2)-th divided electrode, and a (2-2)-th divided electrode spaced apart from the (1-2)-th divided electrode in the first direction, wherein the (2-3)-th electrode group comprises a (1-3)-th divided electrode, and a (2-3)-th divided electrode spaced apart from the (1-3)-th divided electrode in the first direction, and wherein the second trace lines comprises a (1-1)-th divided trace line electrically connected to the (1-1)-th divided electrode, a (2-1)-th divided trace line electrically connected to the (2-1)-th divided electrode, a (1-2)-th divided trace line electrically connected to the (1-2)-th divided electrode, a (2-2)-th divided trace line electrically connected to the (2-2)-th divided electrode, a (1-3)-th divided trace line electrically connected to the (1-3)-th divided electrode, and a (2-3)-th divided trace line electrically connected to the (2-3)-th divided electrode.
7. The electronic device of claim 6, wherein a gap between the (1-1)-th divided trace line and the (2-1)-th divided trace line is narrower than a gap between the (2-1)-th divided trace line and the (1-2)-th divided trace line.

8. The electronic device of claim 6, wherein the (1-1)-th divided trace line, the (2-1)-th divided trace line, the (1-2)-th divided trace line, the (2-2)-th divided trace line, the (1-3)-th divided trace line, and the (2-3)-th divided trace line are sequentially arranged in the first direction.
9. The electronic device of claim 6, wherein the (1-3)-th divided trace line, the (2-3)-th divided trace line, the (1-1)-th divided trace line, the (2-1)-th divided trace line, the (1-2)-th divided trace line, and the (2-2)-th divided trace line are sequentially arranged in the first direction.
10. The electronic device of claim 6, wherein a width of the (1-1)-th divided electrode in the first direction is narrower than a width of the (1-2)-th divided electrode in the first direction, and wherein a width of the (2-1)-th divided electrode in the first direction is wider than a width of the (2-2)-th divided electrode in the first direction.
11. The electronic device of claim 10, wherein a width of the (1-3)-th divided electrode in the first direction is wider than the width of the (1-2)-th divided electrode in the first direction, and wherein a width of the (2-3)-th divided electrode in the first direction is narrower than the width of the (2-2)-th divided electrode in the first direction.
12. The electronic device of claim 10, wherein a width of the (1-3)-th divided electrode in the first direction is narrower than the width of the (1-1)-th divided electrode in the first direction, and wherein a width of the (2-3)-th divided electrode in the first direction is wider than the width of the (2-1)-th divided electrode in the first direction.
13. The electronic device of claim 6, wherein a gap between the (1-3)-th divided electrode and the (2-3)-th divided electrode overlaps the (2-1)-th divided electrode and the (2-2)-th divided electrode, when viewed from the second direction.
14. The electronic device of claim 6, wherein a gap between the (1-3)-th divided electrode and the (2-3)-th divided electrode overlaps the (1-1)-th divided electrode and the (1-2)-th divided electrode, when viewed from the second direction.
15. The electronic device of claim 1, wherein the (2-1)-th trace line comprises a first portion extending in the first direction, and a second portion extending in the second direction from the first portion, and wherein the (2-2)-th trace line faces the second portion.
16. The electronic device of claim 1, wherein the sensor driver is configured to receive a first signal through the (2-1)-th trace line and a second signal through the (2-2)-th trace line, and to generate first data by performing a differential computing operation with respect to the first signal and the second signal.
17. The electronic device of claim 16, wherein the second trace lines comprise a (2-3)-th trace line electrically connected to another second electrode group among the second electrode groups, and a (2-4)-th trace line spaced apart from the (2-3)-th trace line in the first direction while extending in the second direction, and wherein the sensor driver is configured to receive a third signal through the (2-3)-th trace line and a fourth signal through the (2-4)-th trace line, to generate second data by performing a differential computing operation with respect to the third signal and the fourth signal, and to generate third data by performing the differential computing operation with respect to the first data and the second data.
18. The electronic device of claim 17, wherein the sensor driver is configured to generate the first data and the second data through at least one of analog differential processing or digital differential processing, and wherein the sensor driver is configured to generate the third data through at least one of the analog differential processing or the digital differential processing.
19. An electronic device comprising: a sensor layer comprising: a sensing region; a peripheral region adjacent to the sensing region; first electrode groups in the sensing region and arranged in a first direction; second electrode groups in the sensing region, and arranged in a second direction crossing the first direction, while crossing the first electrode groups; a first line electrically connected to one of the second electrode groups; a second line having a length substantially equal to a length of the first line in the second direction, in the sensing region; a third line electrically connected to another of the second electrode groups; and a fourth line having a length substantially

equal to a length of the third line in the second direction, in the sensing region; and a sensor driver configured to drive the sensor layer, configured to selectively operate in a first mode for sensing a touch input or in a second mode for sensing a pen input, configured to receive a first signal through the first line and a second signal through the second line, configured to generate first data by performing a differential computing operation with respect to the first signal and the second signal, configured to receive a third signal through the third line and a fourth signal through the fourth line, configured to generate second data by performing a differential computing operation with respect to the third signal and the fourth signal, and configured to generate third data by performing a differential computing operation with respect to the first data and the second data.

20. The electronic device of claim 19, wherein the one of the second electrode groups comprises a first divided electrode, and a second divided electrode spaced apart from the first divided electrode in the first direction, wherein the another of the second electrode groups comprises a third divided electrode, and a fourth divided electrode spaced apart from the third divided electrode in the first direction, wherein the first line is electrically connected to the first divided electrode, and the second line is electrically connected to the second divided electrode, and wherein the third line is electrically connected to the third divided electrode, and the fourth line is electrically connected to the fourth divided electrode.

21. The electronic device of claim 20, wherein the first line and the second line are insulated from one of the third divided electrode or the fourth divided electrode while crossing the third divided electrode and the fourth divided electrode.

22. The electronic device of claim 20, wherein the first line comprises a first portion extending in the first direction, and a second portion extending in the second direction from the first portion, and wherein the second line faces the second portion of the first line.

23. The electronic device of claim 20, wherein the sensor driver is connected to one end of the second line, and an opposite end of the second line is floated.

24. An electronic device comprising: first electrode groups in a sensing region, and arranged in a first direction; second electrode groups crossing the first electrode groups in the sensing region, and arranged in a second direction crossing the first direction; a first line in the sensing region, and electrically connected to one of the second electrode groups; a second line in the sensing region, and adjacent to the first line in the first direction; and a third line in the sensing region, and electrically connected to another of the second electrode groups, wherein a gap between the first line and the second line is narrower than a gap between the second line and the third line, and wherein a length of a portion of the first line in the sensing region is substantially equal to a length of a portion of the second line in the sensing region.

25. The electronic device of claim 24, wherein the one of the second electrode groups comprises a first divided electrode, and a second divided electrode spaced apart from the first divided electrode in the first direction, and wherein the first line is electrically connected to the first divided electrode, and the second line is electrically connected to the second divided electrode.

26. The electronic device of claim 24, wherein the first line comprises a first portion extending in the first direction, and a second portion extending in the second direction from the first portion, and wherein the second line faces the second portion of the first line while extending in the second direction.