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(54) **SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SEMICONDUCTOR DEVICE**

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(57) **ABSTRACT**

A method for fabricating a semiconductor device includes: forming a stack body over a substrate; forming channel structures in the stack body, the channel structures having a channel layer penetrating the stack body; forming a contact-level dielectric layer over the stack body and the channel structures; forming a contact hole penetrating the contact-level dielectric layer; forming contact plugs in the contact hole, the contact plugs coupled to the channel layers of the channel structures; recessing the contact plugs to form upper surfaces of the contact plugs that are lower than an upper surface of the contact-level dielectric layer; forming a bit line-level dielectric layer including a spacer layer over the recessed contact plugs; etching the bit line-level dielectric layer to form trenches that expose the recessed contact plugs; and forming a bit line in one or more of the trenches.

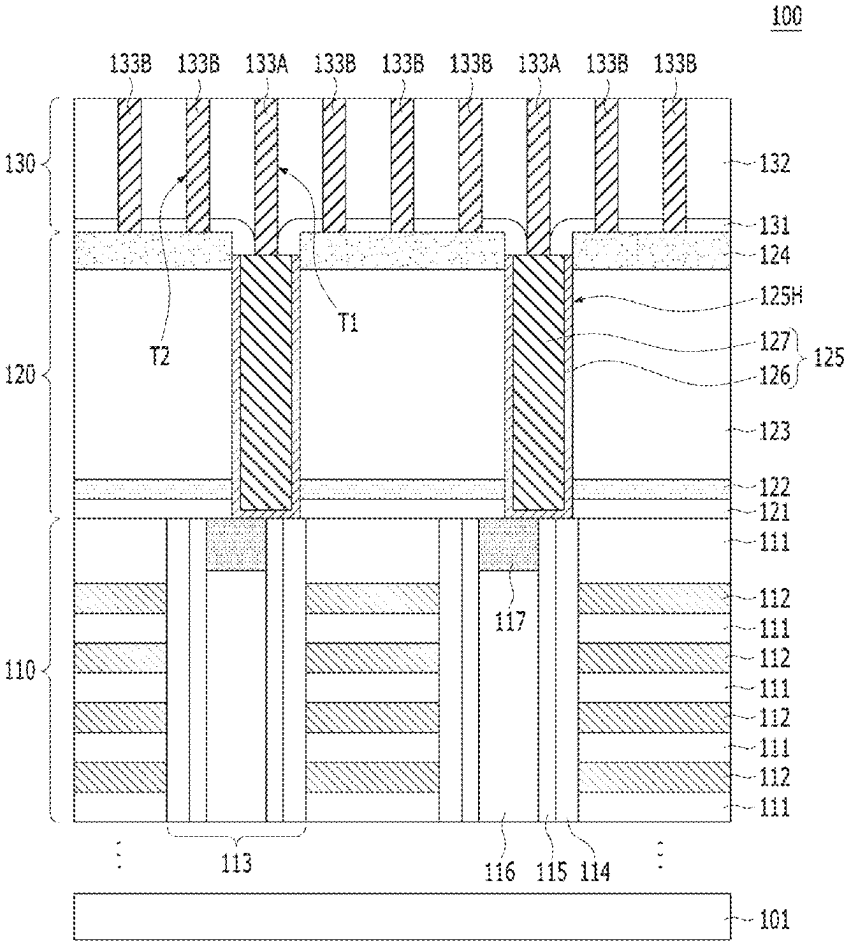

FIG. 1

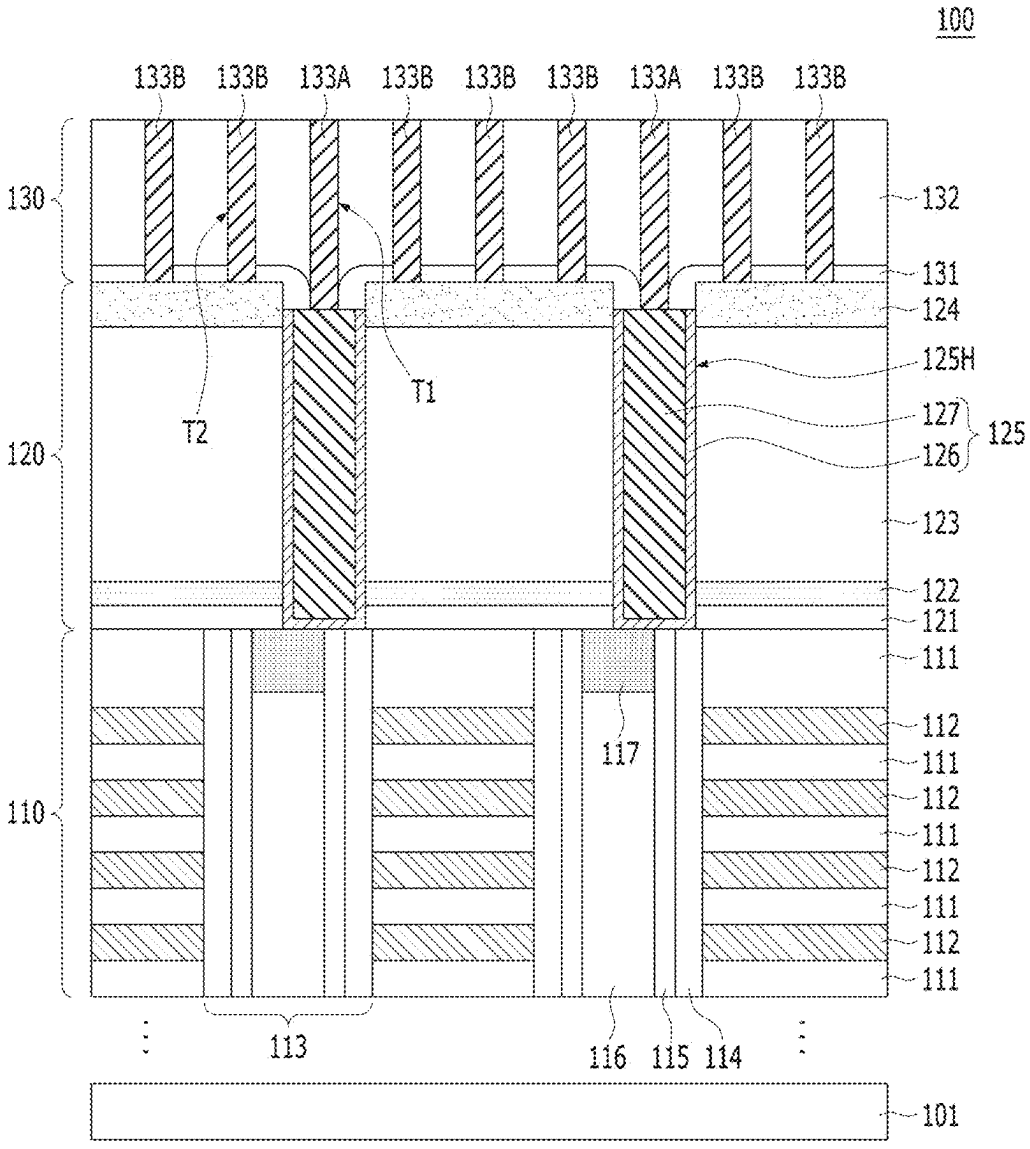
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FIG. 2A

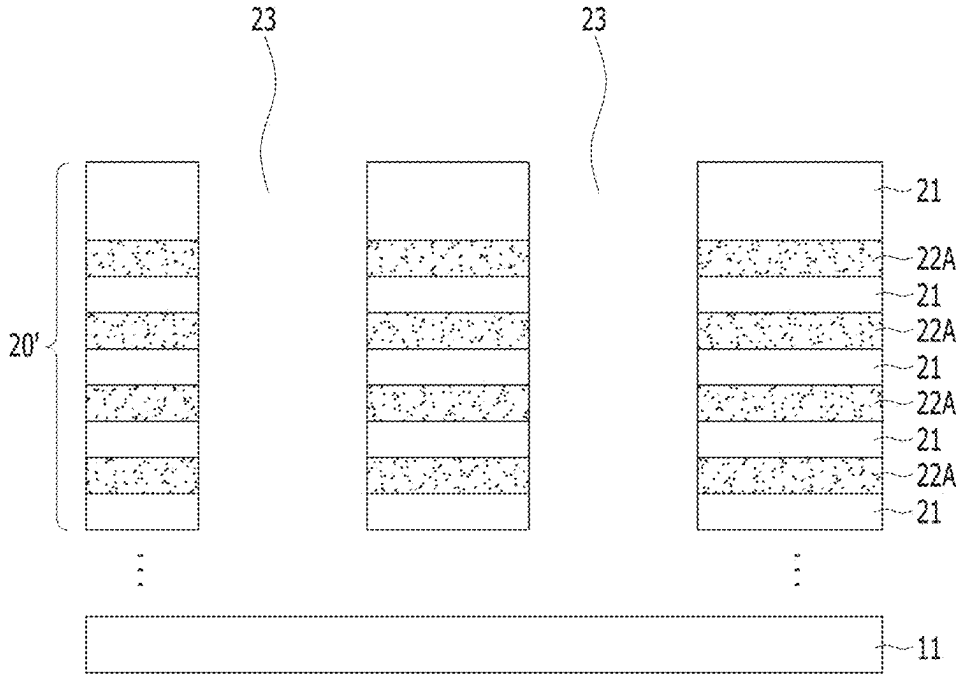

FIG. 2B

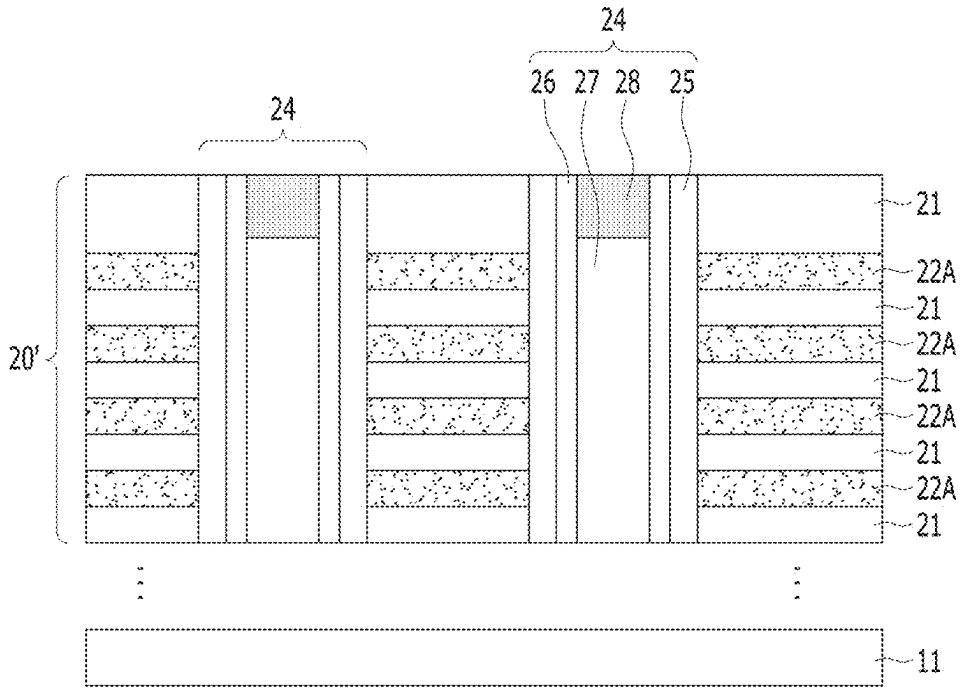

FIG. 2C

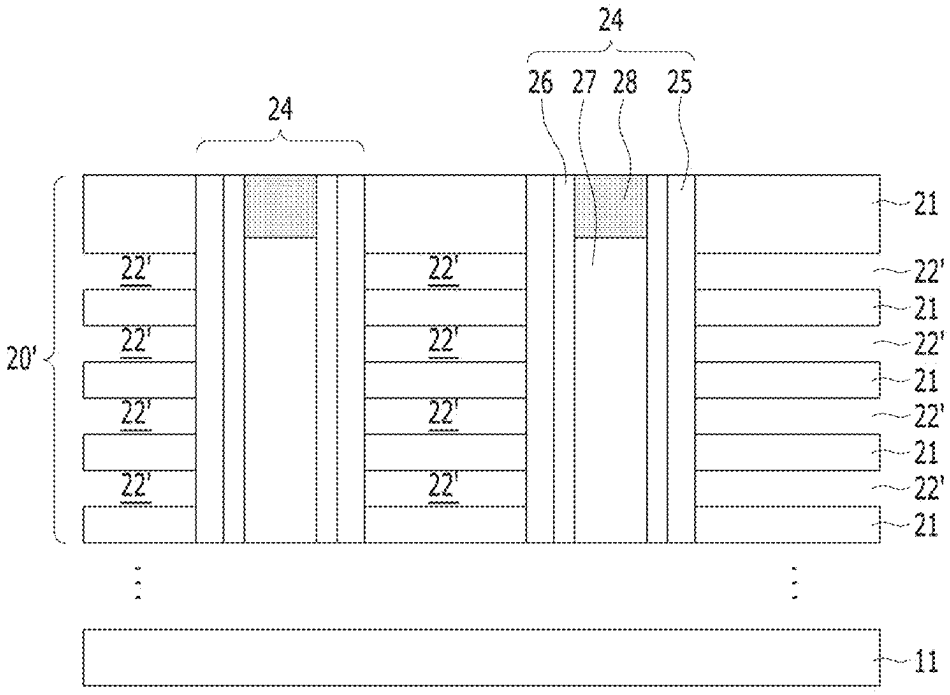

FIG. 2D

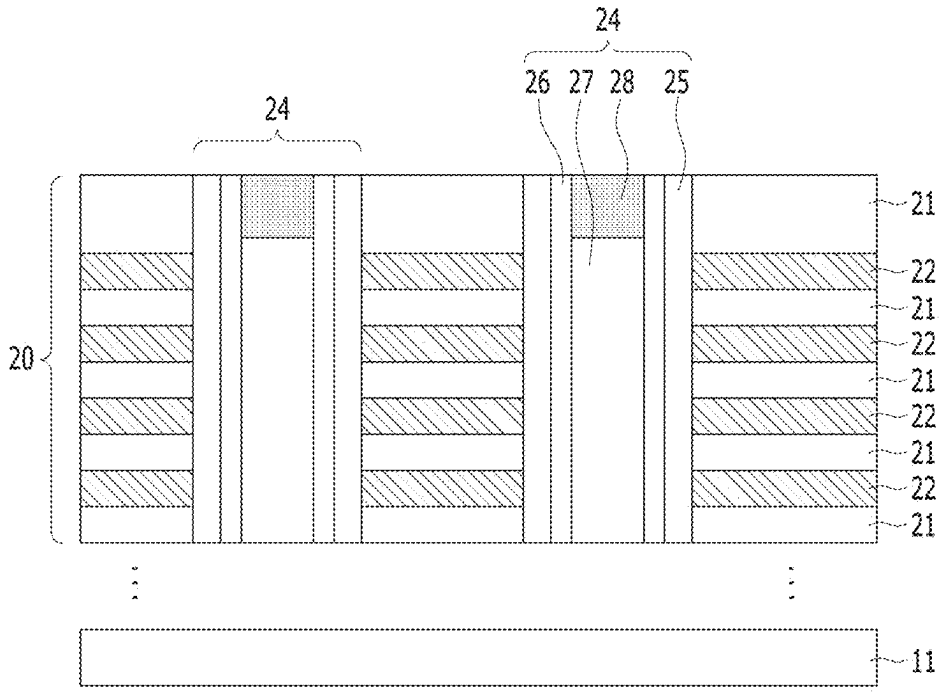

FIG. 2E

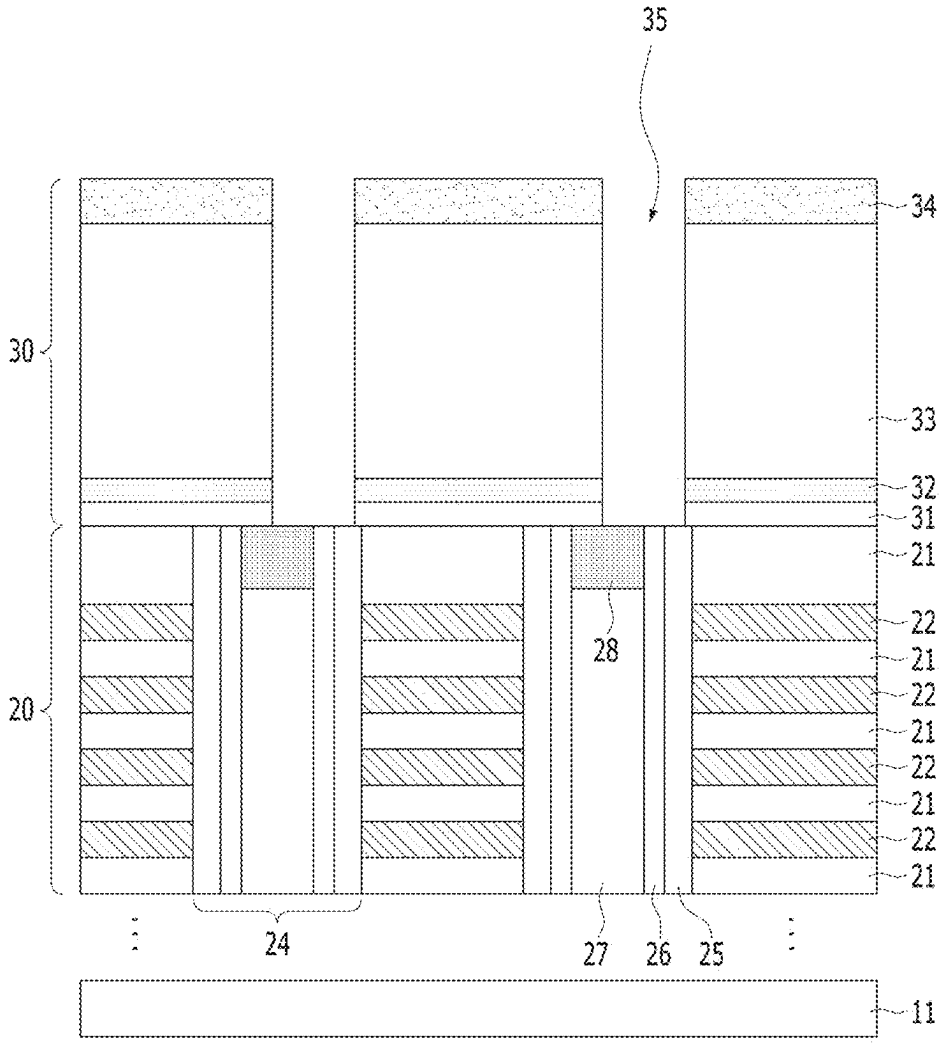

FIG. 2F

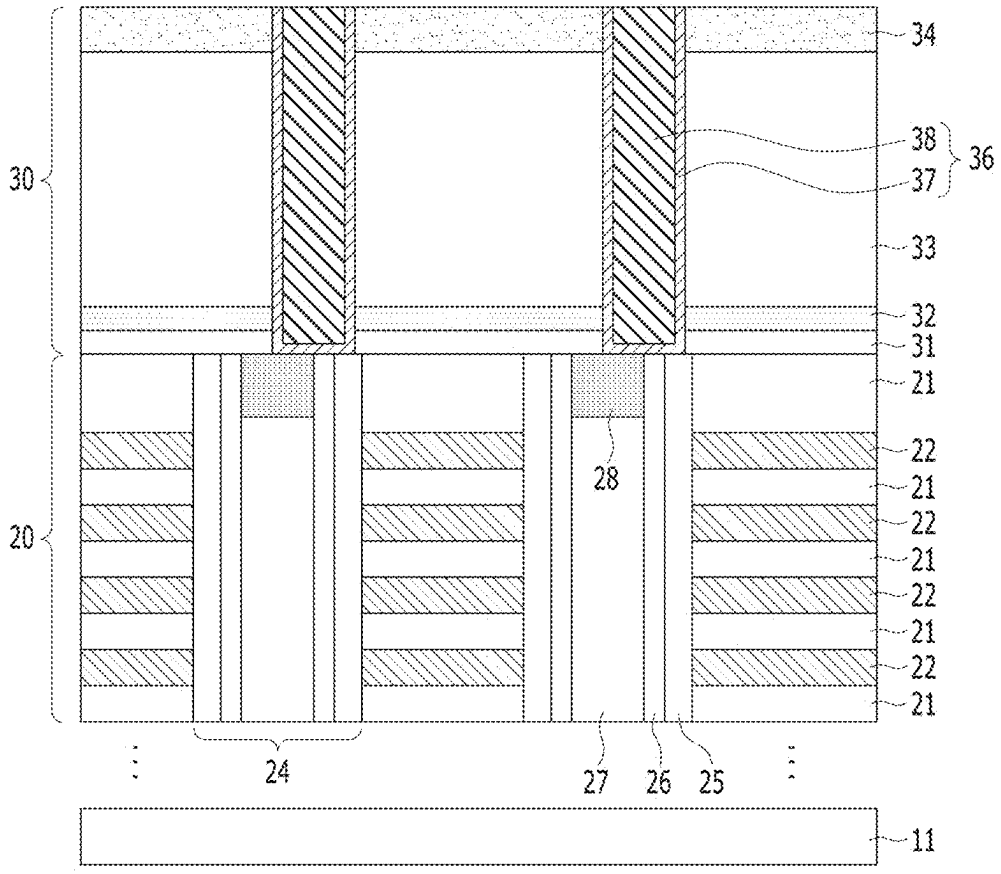

FIG. 2G

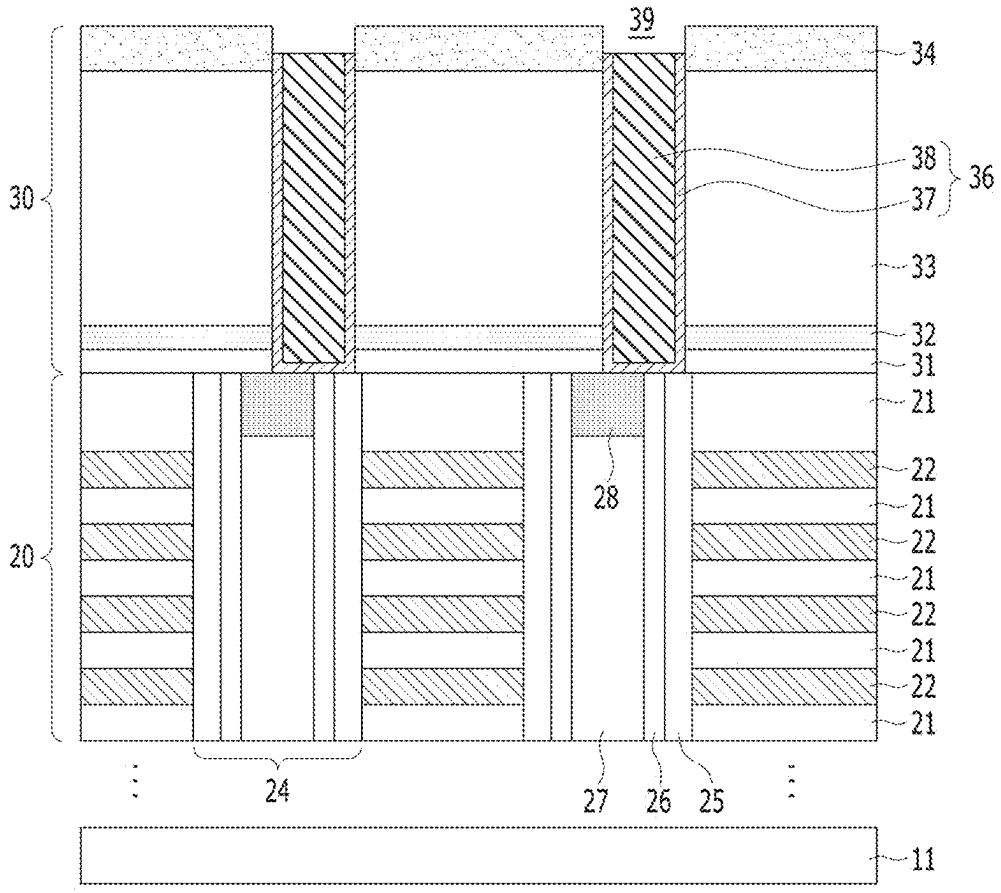
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FIG. 2H

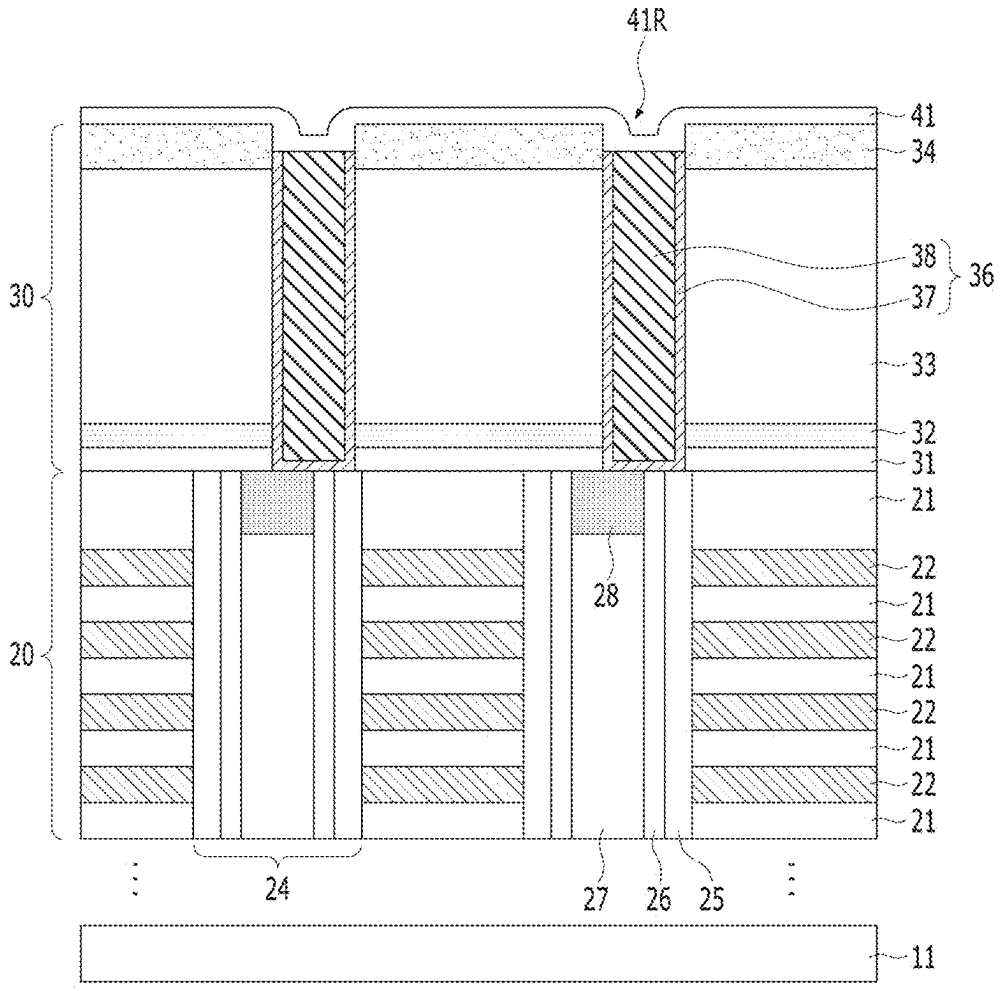
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FIG. 2I

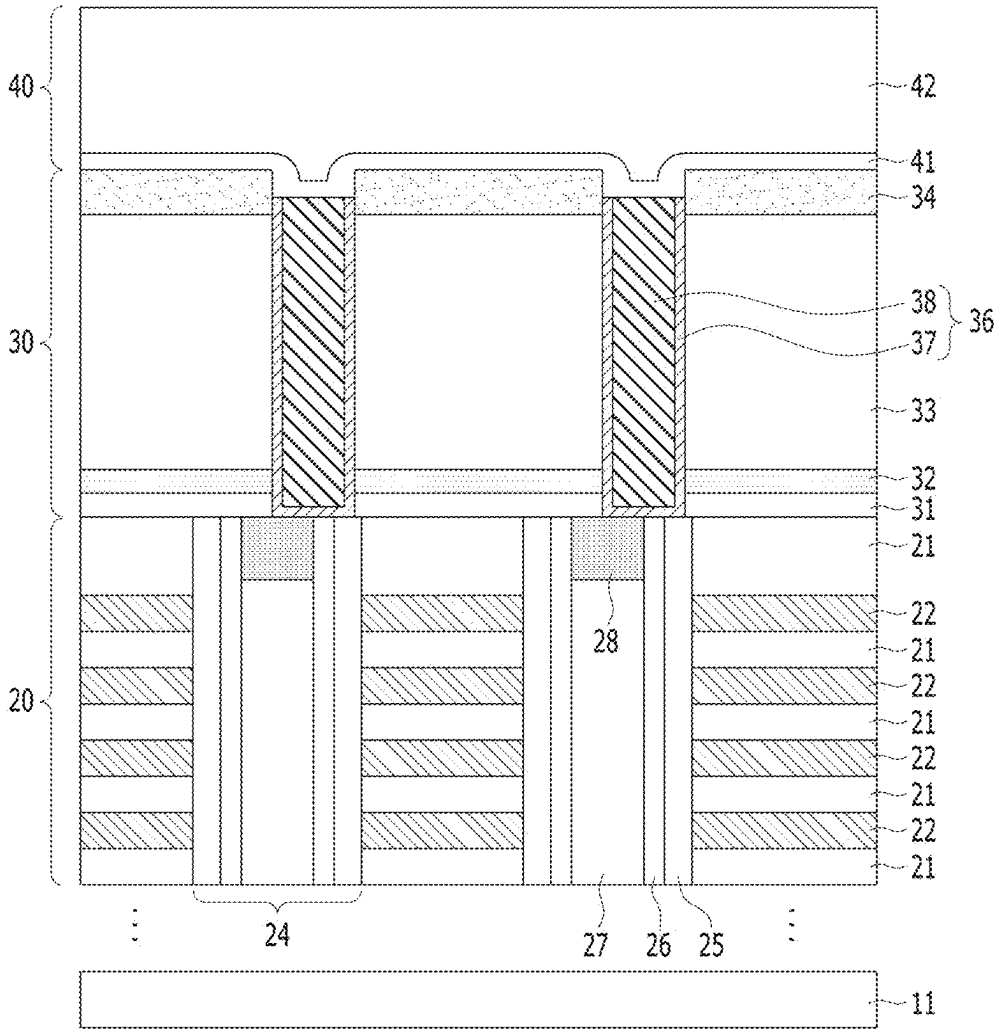
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FIG. 2J

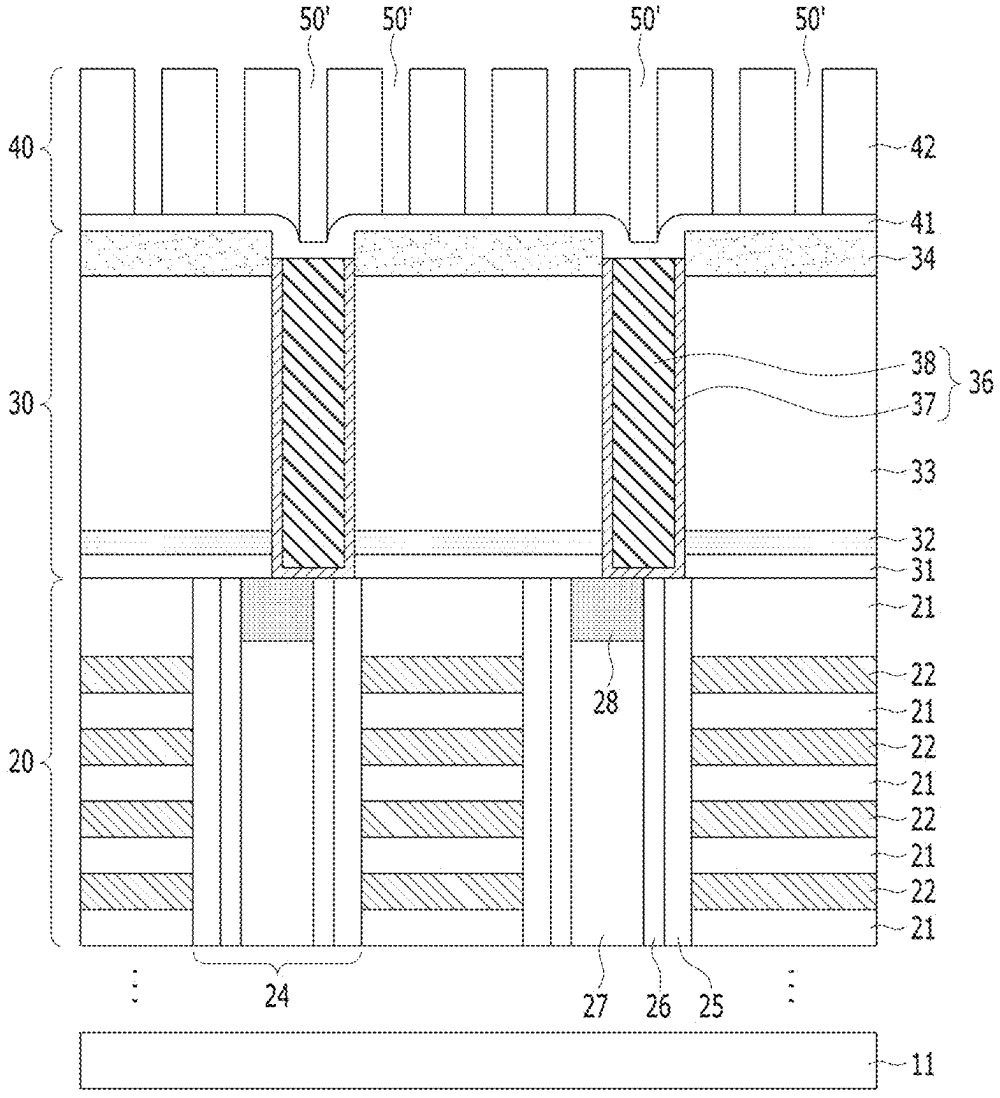
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FIG. 2K

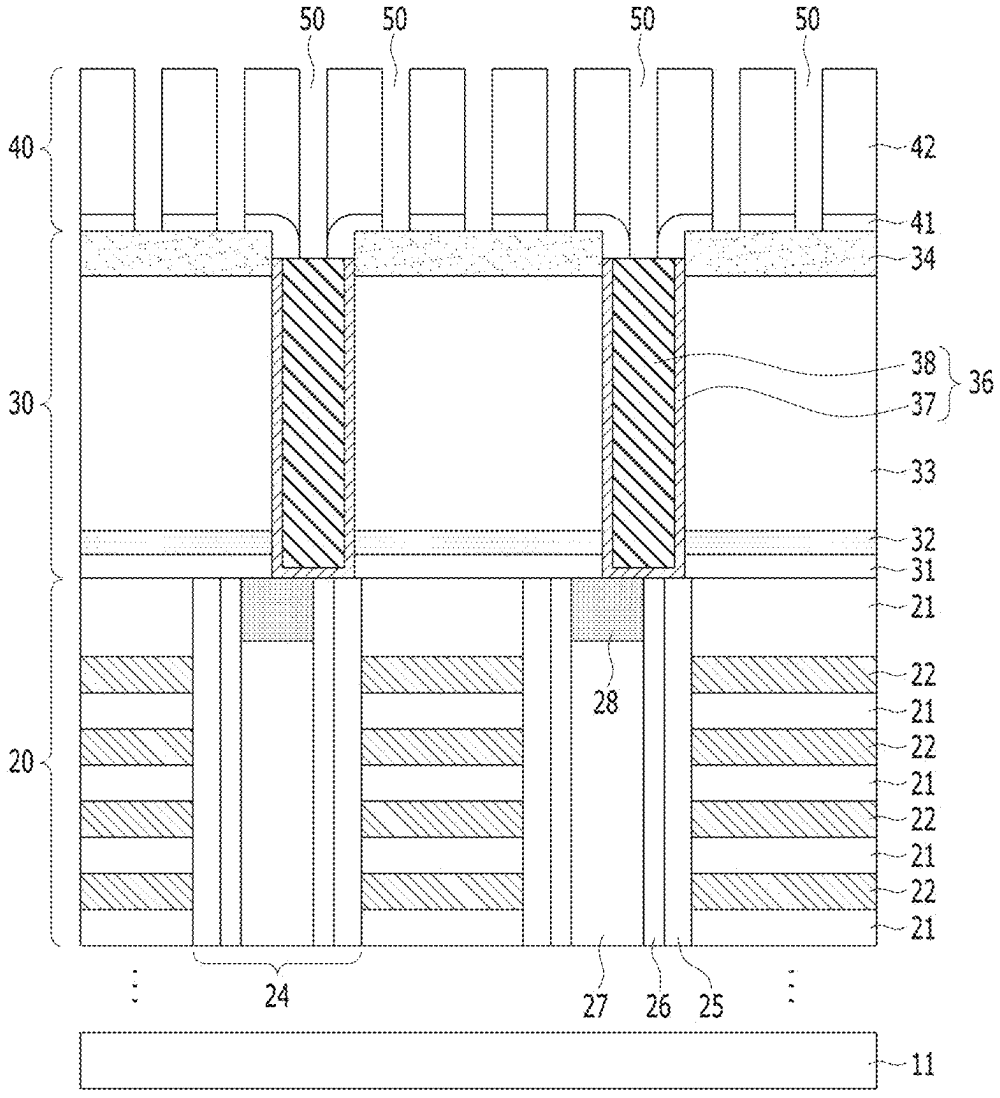
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FIG. 2L

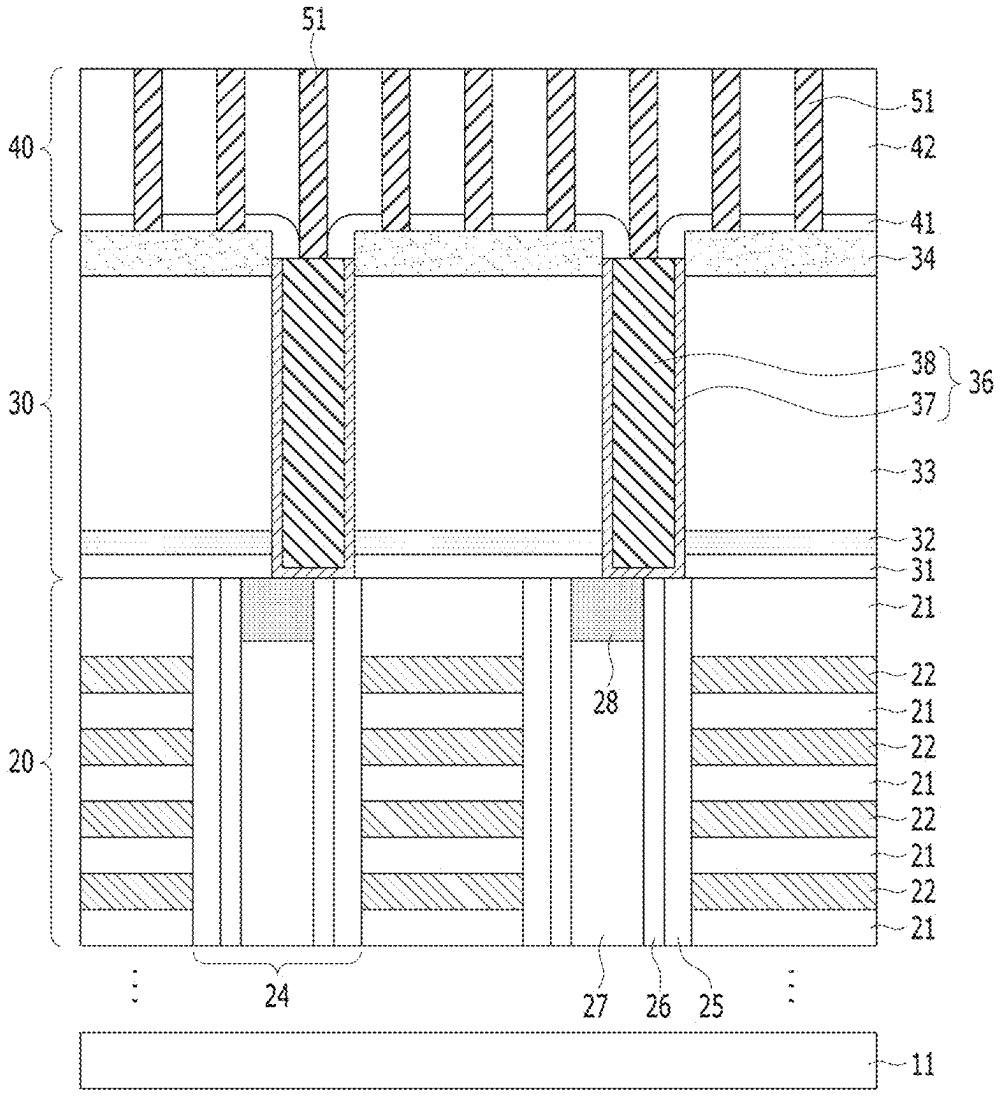
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FIG. 3A

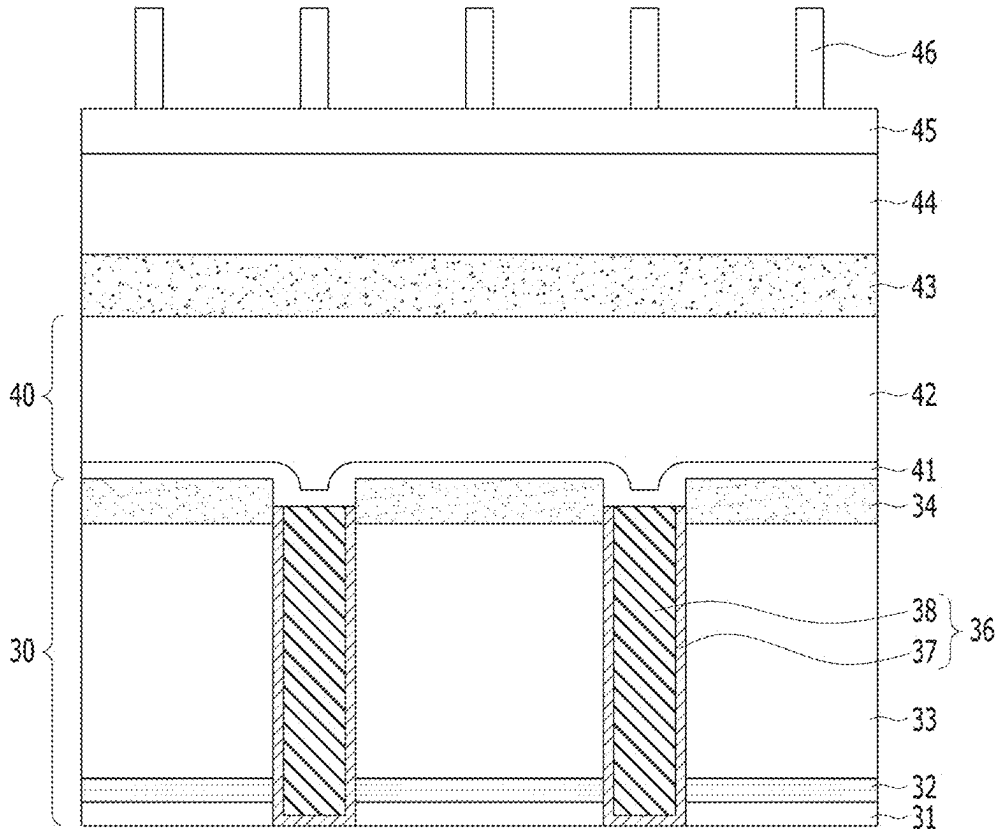


FIG. 3B

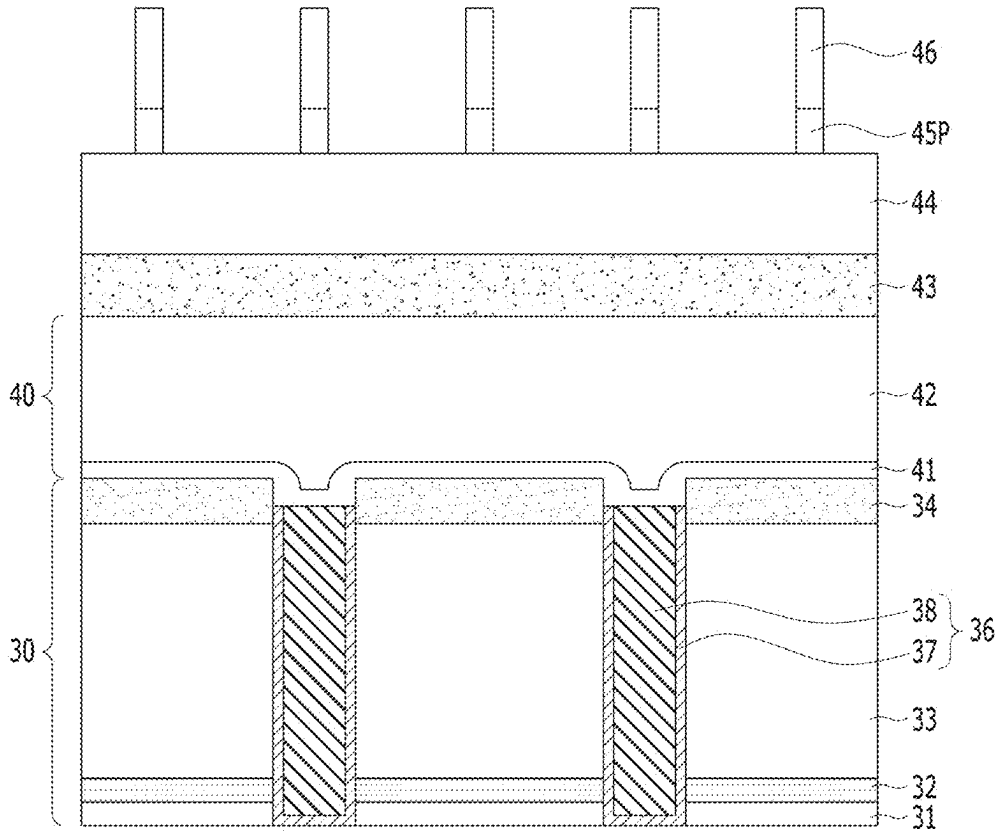


FIG. 3C

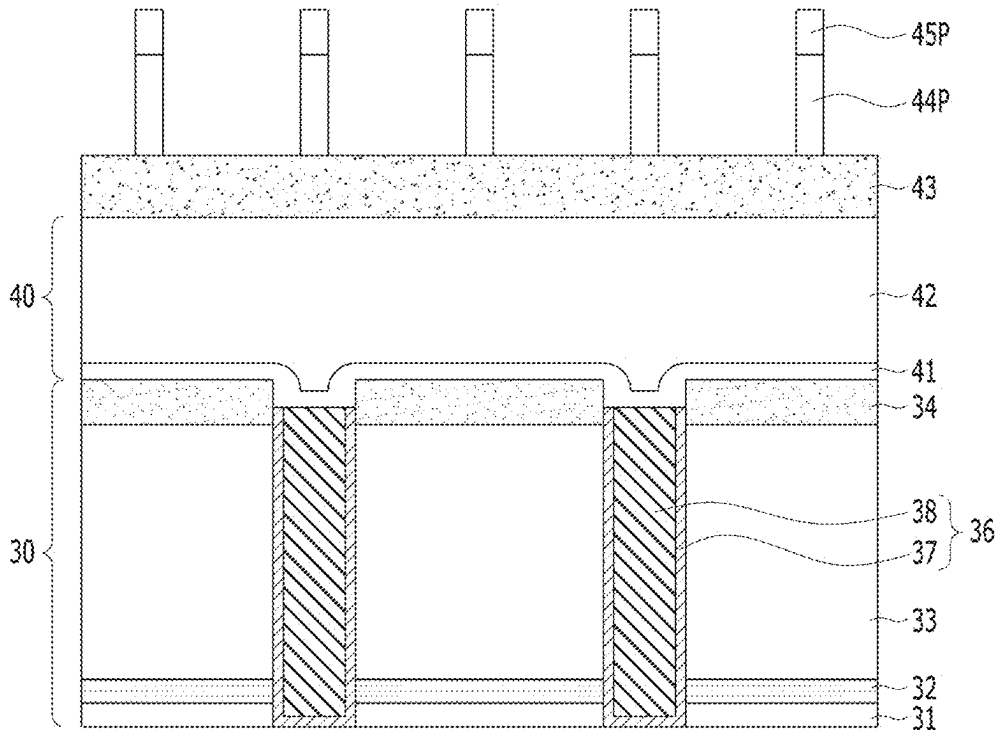


FIG. 3D

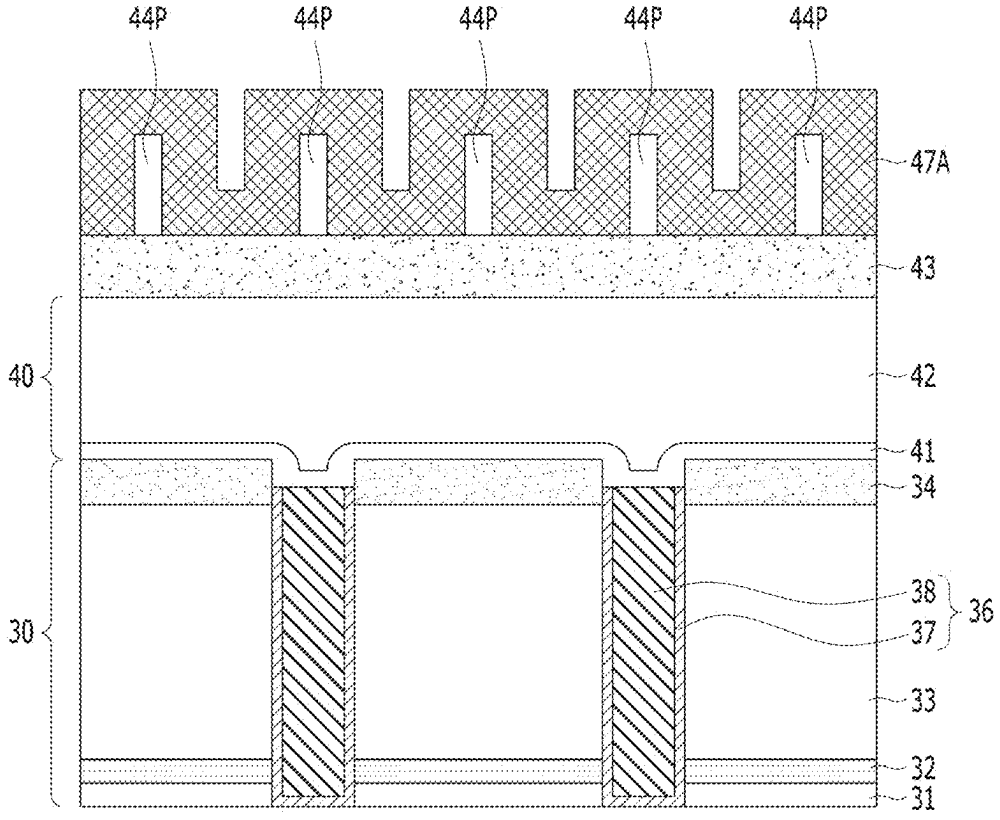


FIG. 3E

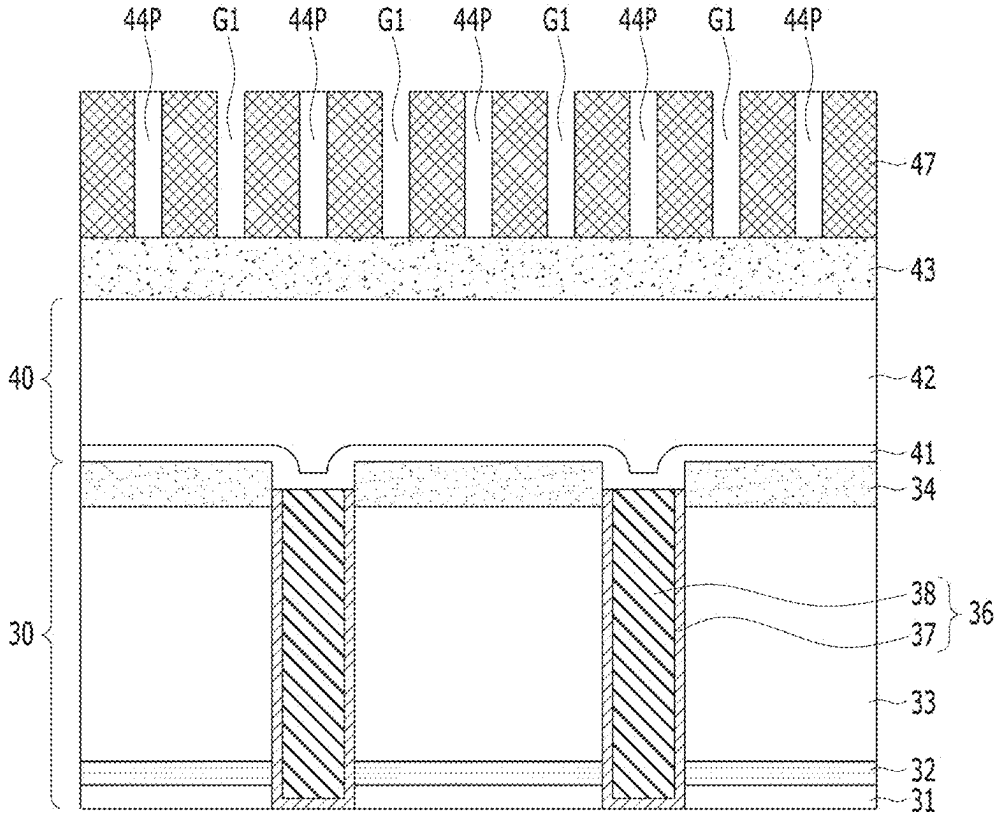


FIG. 3F

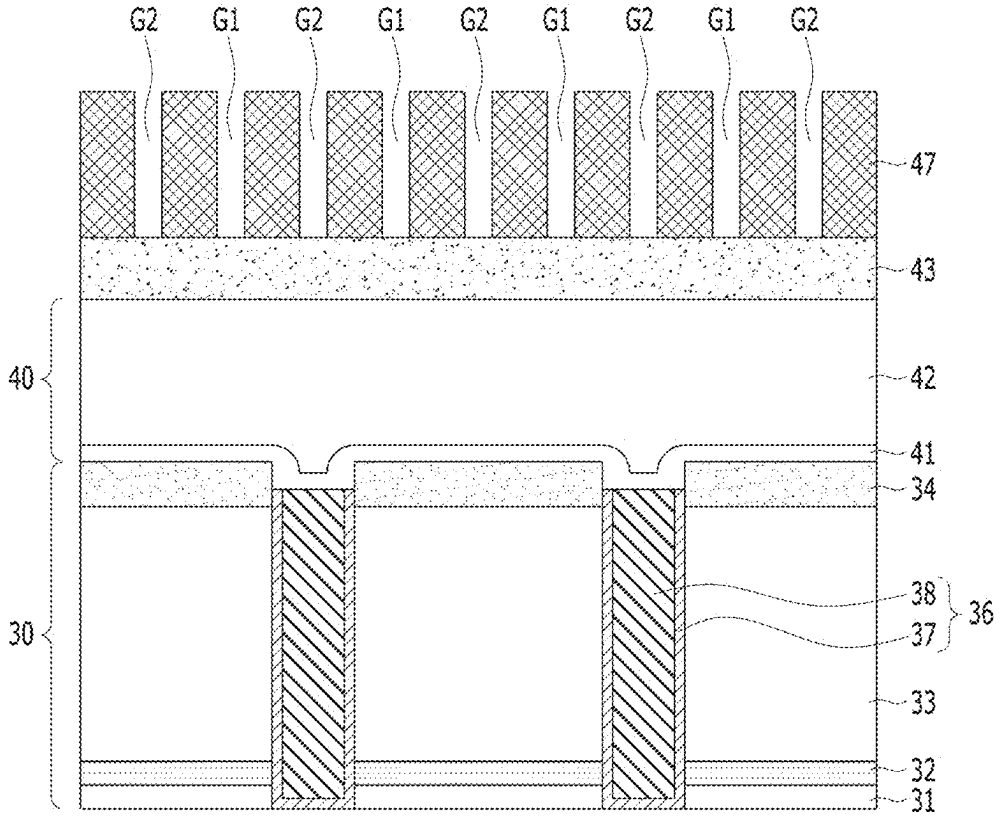


FIG. 3G

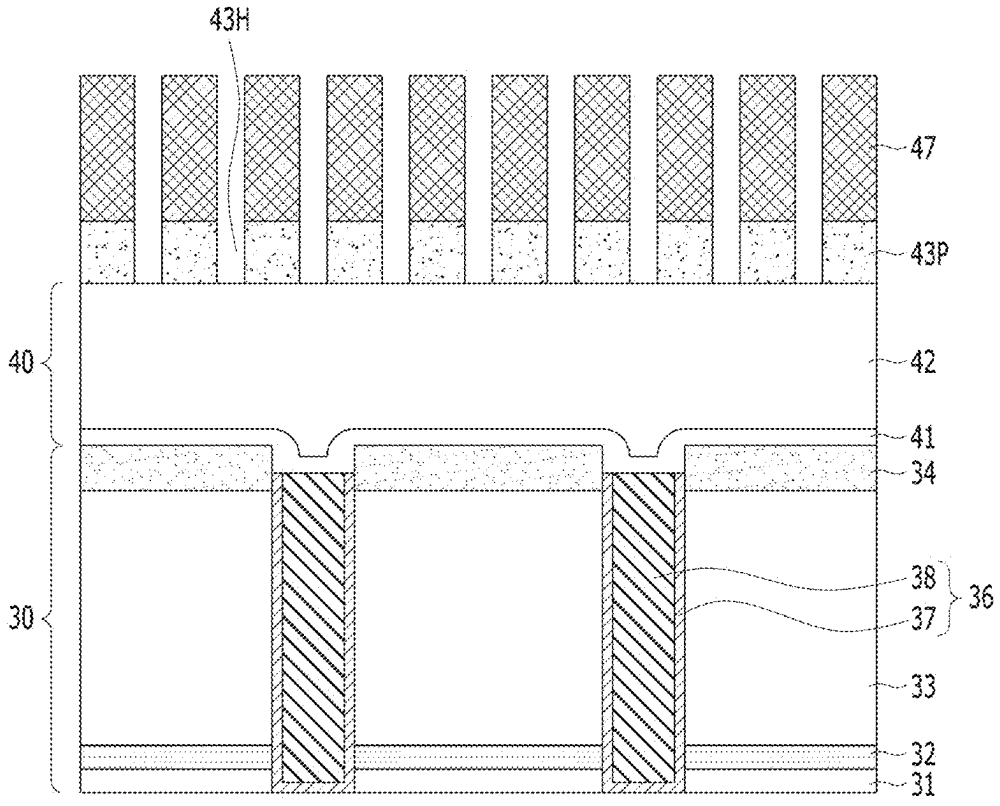
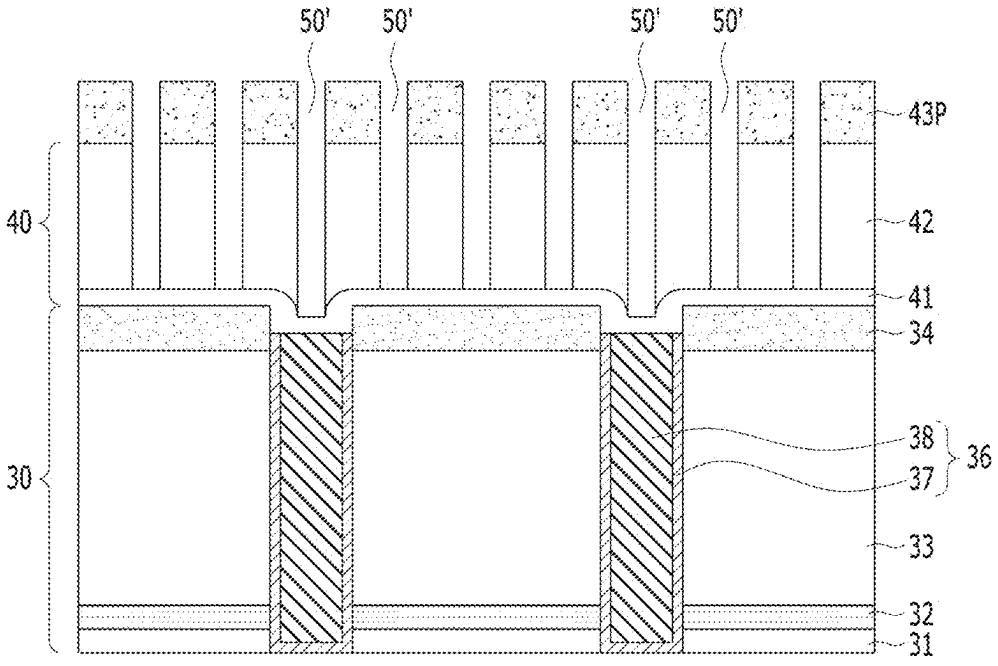


FIG. 3H



SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SEMICONDUCTOR DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a continuation application of U.S. patent application Ser. No. 17/563,779, filed on Dec. 28, 2021, which claims priority under 35 U.S.C. § 119 (a) to Korean application number No. 10-2021-0106582, filed on Aug. 12, 2021, which applications are incorporated herein by reference in their entirety.

BACKGROUND

1. Technical Field

[0002] Exemplary embodiments of the present invention relate to a semiconductor device, and more particularly, to a vertical semiconductor device and a method for fabricating the vertical semiconductor device.

2. Related Art

[0003] As recent information and communication devices are equipped with multiple functions, semiconductor devices are required to have large capacity and high degree of integration. As the size of a semiconductor device for high integration shrinks, the structures of operating circuits and/or interconnections included in the semiconductor device for operation and electrical connection of the semiconductor device are getting more complicated. Accordingly, it is demanded to develop a semiconductor device having excellent electrical characteristics with improved degree of integration.

SUMMARY

[0004] In accordance with an embodiment, a method for fabricating a semiconductor device may include: forming a stack body over a substrate; forming channel structures in the stack body, the channel structures comprising a channel layer penetrating the stack body; forming a contact-level dielectric layer over the stack body and the channel structures; forming a contact hole penetrating the contact-level dielectric layer; forming contact plugs in the contact hole, the contact plugs coupled to the channel layers of the channel structures; recessing the contact plugs to form upper surfaces of the contact plugs that are lower than an upper surface of the contact-level dielectric layer; forming a bit line-level dielectric layer including a spacer layer over the recessed contact plugs; etching the bit line-level dielectric layer to form trenches that expose the recessed contact plugs; and forming a bit line in one or more of the trenches.

[0005] In accordance with an embodiment, a semiconductor device may include: a memory cell stack comprising dielectric layers and gate electrodes that are alternately stacked with each other, the memory cell stack positioned over a substrate; a plurality of channel structures each including a channel layer that penetrates the memory cell stack; a contact-level dielectric layer formed over the channel structures and including a contact hole that exposes each of the channel structures; recessed contact plugs respectively coupled to the channel layers through the contact hole and having an upper surface which is lower than an upper surface of the contact-level dielectric layer; a bit line-level dielectric layer formed over the recessed contact plugs; and a plurality of bit lines formed in the bit line-level dielectric layer, wherein the bit line-level dielectric layer includes a spacer layer in contact with sidewalls of bottom portions of the bit lines.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. **1** is a cross-sectional view illustrating a schematic structure of a semiconductor device in accordance with an embodiment of the present invention.

[0007] FIGS. **2**A, **2**B, **2**C, **2**D, **2**E, **2**F, **2**G, **2**H, **2**I, **2**J, **2**K, and **2**L are cross-sectional views illustrating a method for fabricating a semiconductor device in accordance with an embodiment of the present invention.

[0008] FIGS. **3**A, **3**B, **3**C, **3**D, **3**E, **3**F, **3**G, and **3**H are cross-sectional views illustrating a method for forming preliminary trenches **50'** shown in FIG. **2**J.

DETAILED DESCRIPTION

[0009] Embodiments will be described below in more detail with reference to the accompanying drawings. The embodiments may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Throughout the disclosure, like reference numerals refer to like parts throughout the various figures and embodiments.

[0010] The drawings are not necessarily to scale and in some instances, proportions may have been exaggerated in order to clearly illustrate features of the embodiments. When a first layer is referred to as being "on" a second layer or "on" a substrate, it not only refers to a case where the first layer is formed directly on the second layer or the substrate but also a case where a third layer exists between the first layer and the second layer or the substrate. It will be understood that when an element or layer is referred to as being "connected to" or "coupled to" another element, structure, or layer etc., it can be directly connected or coupled to the other element, structure, or layer etc., or intervening elements, structures, or layers etc., may be present. In contrast, when an element is referred to as being "directly connected to" or "directly coupled to" another element, structure, or layer etc., there are no intervening elements or layers present.

[0011] Embodiments of the present disclosure may be directed to a semiconductor device capable of securing contact margins, and a method for fabricating the semiconductor device.

[0012] FIG. **1** is a cross-sectional view illustrating a schematic structure of a semiconductor device in accordance with an embodiment.

[0013] Referring to FIG. **1**, a semiconductor device **100** may include a memory cell stack **110** disposed over a substrate **101**. The semiconductor device **100** may include a vertical NAND.

[0014] The substrate **101** may include a silicon substrate, a monocrystalline silicon substrate, a polysilicon substrate, an amorphous silicon substrate, a silicon germanium substrate, a monocrystalline silicon germanium substrate, a polycrystalline silicon germanium substrate, a carbon-doped silicon substrate, a combination thereof or a multi-layer thereof. The substrate **101** may include other semiconductor materials, such as germanium. The substrate **101** may include a III/V-group semiconductor substrate, for example,

a compound semiconductor substrate, such as GaAs. The substrate **101** may include a Silicon-On-Insulator (SOI) substrate. Although not illustrated, a peripheral circuit transistor may be formed over the substrate **101**.

[0015] In the memory cell stack **110**, dielectric layers **111** and gate electrodes **112** may be vertically alternately stacked. The memory cell stack **110** may further include a plurality of channel structures **113** penetrating the dielectric layers **111** and the gate electrodes **112**. The channel structure **113** may include a memory layer **114** and a channel layer **115**. The memory layer **114** may include an ONO structure. The ONO structure may include a stack of an oxide, a nitride and an oxide. The memory layer **114** may include a stack of a blocking layer, a charge trapping layer, and a tunnel dielectric layer. The blocking layer and the tunnel dielectric layer may include an oxide, and the charge trapping layer may include a nitride. The channel layer **115** may include a polysilicon layer. According to another embodiment, the blocking layer may include a high-k material, and the high-k material may include aluminum oxide or hafnium oxide. The channel layer **115** may have a cylinder shape having an inner space. The memory layer **114** may surround an outer wall of the channel layer **115**. The channel structure **113** may further include a core dielectric layer **116**. The inner space of the channel layer **115** may be completely filled with the core dielectric layer **116**. The core dielectric layer **116** may include silicon oxide or silicon nitride. A conductive pad **117** coupled to an upper end of the channel layer **115** may be further formed over the core dielectric layer **117**.

[0016] The gate electrodes **112** may surround the channel structure **113**. The channel structure **113** may vertically penetrate the dielectric layers **111** and the gate electrodes **112**. The channel structure **113** may be referred to as a 'vertical channel structure' or a 'pillar channel structure'.

[0017] A contact-level dielectric layer **120** may be formed over the conductive pad **117**. Contact plugs **125** penetrating the contact-level dielectric layer **120** may be formed. A contact hole **125**H may be formed in the contact-level dielectric layer **120**, and a contact plug **125** may be formed in the contact hole. Each contact plug **125** may be coupled to each channel layer **115**. The contact plugs **125** may have an upper surface which is lower than the upper surface of the contact-level dielectric layer **120**, and the contact plugs **125** having this shape may be referred to as 'recessed contact plugs'. The contact plugs **125** may penetrate the contact-level dielectric layer **120**, and the individual contact plugs **125** may be electrically connected to the conductive pad **117** and the channel layer **115**. The contact-level dielectric layer **120** may include a first inter-layer dielectric layer **121**, a first etch stop layer **122**, a second inter-layer dielectric layer **123**, and a second etch stop layer **124**.

[0018] A bit line-level dielectric layer **130** may be formed over the contact-level dielectric layer **120**, and a plurality of bit lines **133**A and **133**B may be formed in the bit line-level dielectric layer **130**. The bit line-level dielectric layer **130** may include a spacer layer **131** and a third inter-layer dielectric layer **132**. The bit lines **133**A and **133**B may be formed by a double patterning process. As for the method of forming the bit lines **133**A and **133**B, FIGS. **2**A to **3**J may be referred to. The spacer layer **131** may cover upper surface edges of the contact plugs **125**. The spacer layer **131** may include silicon nitride. The upper surfaces of the contact plugs **125** may be positioned at a level lower than the upper surfaces of the second etch stop layer **124**. In other words, the upper surfaces of the contact plugs **125** may be recessed lower than the upper surface of the second etch stop layer **124**.

[0019] The bit lines **133**A and **133**B may be formed in the trenches T**1** and T**2**, respectively. The trenches T**1** and T**2** are laterally disposed to each other and include first trenches T**1** exposing the contact plugs **125** and second trenches T**2** between the first trenches T**1**. For example, at least three second trenches T**2** may be positioned between the neighboring first trenches T**1**. The first trenches T**1** and the second trenches T**2** may be separated from each other by the spacer layer **131**. The bottom surfaces of the first trenches T**1** may be positioned at a lower level than the bottom surfaces of the second trenches T**2**.

[0020] The line widths of the bit lines **133**A and **133**B may be smaller than the line widths of the contact plugs **125**. For example, the line widths of the contact plugs **125** may be approximately three times as great as the line widths of the bit lines **133**A and **133**B. For the sake of convenience in description, the bit lines **133**A contacting the contact plugs **125** may be simply referred to as a 'first bit line **133**A' or an 'active bit line', and the bit lines **133**B that do not contact the contact plugs **125** may be simply referred to as a 'second bit line **133**B' or a 'passing bit line'. Three second bit lines **133**B may be positioned between the neighboring first bit lines **133**A. Although not illustrated, the second bit lines **133**B may also be coupled to other contact plugs (not shown).

[0021] The bottom portions of the first and second bit lines **133**A and **133**B, that is, bit line contact portions may be self-aligned to the spacer layer **131**. The first bit lines **133**A and the contact plugs **125** may directly contact each other. In other words, additional bit line contact plugs might not be formed between the first and second bit lines **133**A and **133**B and the contact plugs **125**.

[0022] The second etch stop layer **124** may be covered by the spacer layer **131**. The second etch stop layer **124** and the spacer layer **131** may include the same material. The spacer layer **131** may include a rounding portion, and the rounding portion of the spacer layer **131** may cover edges of the second etch stop layer **124** over the contact plug **125**. The rounding portion of the spacer layer **131** may contact bit line contact portions of the first bit lines **133**A.

[0023] As described above, the contact plugs **125** and the channel structure **113** may be directly coupled. Additional contact plugs might not be positioned between the contact plugs **125** and the channel structure **113**. The contact plugs **125** may have a single contact structure including one contact plug **125**, rather than a multi-layer structure of a plurality of contact plugs.

[0024] Since the contact plugs **125** have a larger line width than the bit lines **133**A and **133**B, the contact area between the contact plugs **125** and the channel structure **113** may be increased, thereby improving the contact resistance.

[0025] As a comparative example, when the line widths of the contact plugs **125** are smaller than the bit lines **133**A and **133**B, the contact area between the contact plugs **125** and the channel structure **113** may be reduced, thus increasing the contact resistance. Also, an overlay margin of the contact plugs **125** and the channel structure **113** may be reduced.

[0026] According to an embodiment, since additional contact plugs are not formed between the contact plugs **125** and the channel structure **113**, the process may be simplified.

[0027] FIGS. **2**A to **2**L are cross-sectional views illustrating a method for fabricating a semiconductor device in accordance with an embodiment.

[0028] Referring to FIG. **2**A, a stack body **20'** may be formed over a substrate **11**. The substrate **11** may include a silicon substrate, a monocrystalline silicon substrate, a polysilicon substrate, an amorphous silicon substrate, a silicon germanium substrate, a monocrystalline silicon germanium substrate, a polycrystalline silicon germanium substrate, a carbon-doped silicon substrate, a combination thereof, or a multilayer thereof. The substrate **11** may include other semiconductor materials, such as germanium. The substrate **11** may include a III/V-group semiconductor substrate, for example, a compound semiconductor substrate, such as GaAs. The substrate **11** may include a Silicon-On-Insulator (SOI) substrate. Although not illustrated, a peripheral circuit transistor may be formed over the substrate **11**.

[0029] The stack body **20'** may include dielectric layers **21** and sacrificial layers **22**A. In the stack body **20'**, the dielectric layers **21** and the sacrificial layers **22**A may be alternately stacked. The dielectric layers **21** and the sacrificial layers **22**A may alternate vertically from the surface of the substrate **11**. The dielectric layers **21** and the sacrificial layers **22**A may be formed of different materials. The sacrificial layers **22**A may have an etch selectivity with respect to the dielectric layers **21**. The dielectric layers **21** may be silicon oxide, and the sacrificial layers **22**A may be silicon nitride. The uppermost dielectric layer **21** may be thicker than the other dielectric layers **21**. The dielectric layers **21** and the sacrificial layers **22**A may be formed by Chemical Vapor Deposition (CVD) or Atomic Layer Deposition (ALD).

[0030] Although not illustrated, after the stack body **20'** is formed, a step structure (not shown) may be formed in a region where a pad portion of the stack body **20'** is to be formed.

[0031] Subsequently, channel openings **23** may be formed in the stack body **20'**. The channel openings **23** may vertically penetrate the stack body **20'**.

[0032] Referring to FIG. **2**B, a channel structure **24** may be formed in the channel opening **23**. The channel structure **24** may extend vertically from the substrate **11**. The channel structure **24** may include a memory layer **25** and a channel layer **26**. The memory layer **25** may be formed on a sidewall of the channel opening **23** and surround an outer wall of the channel layer **26**. The memory layer **25** may be a stack including at least a charge trapping layer. For example, in the memory layer **25**, a blocking layer, a charge trapping layer, and a tunnel dielectric layer may be sequentially stacked. The memory layer **25** may include a stack of silicon oxide, silicon nitride, and silicon oxide, wherein the silicon nitride may serve as a charge trapping layer. The channel layer **26** may include silicon, for example, polysilicon. The memory layer **25** may include an ONO structure, and the ONO structure may include a stack of an oxide, a nitride, and an oxide. According to another embodiment, the blocking layer of the memory layer **25** may include a high-k material, and the high-k material may include aluminum oxide or hafnium oxide. The channel layer **26** may have a cylinder shape having an inner space. A memory layer **25** may surround an outer wall of the channel layer **26**.

[0033] The channel structure **24** may further include a core dielectric layer **27** and a conductive pad **28** over the core dielectric layer **27**. The core dielectric layer **27** may partially fill the inside of the channel layer **26**, and the conductive pad **28** may be positioned over the core dielectric layer **27**. The conductive pad **28** may contact the upper inner wall of the channel layer **26**. The core dielectric layer **27** may include silicon oxide. The conductive pad **28** may include polysilicon, for example, polysilicon which is doped with an impurity.

[0034] Referring to FIG. **2**C, portions of the stack body **20'**, for example, the sacrificial layers **22**A, may be selectively removed. As a result, lateral recesses **22'** may be formed between the dielectric layers **21**. The lateral recesses **22'** may be referred to as lateral air gaps. The lateral recesses **22'** and the dielectric layers **21** may be alternately stacked. When the sacrificial layers **22**A include silicon nitride, the sacrificial layers **22**A may be removed by a chemical including phosphoric acid (H_3PO_4).

[0035] Referring to FIG. **2**D, gate electrodes **22** may be formed. The gate electrodes **22** may fill the lateral recesses **22'**, respectively. The channel structures **24**, the dielectric layers **21**, and the gate electrodes **22** may form the memory cell stack **20**. In the memory cell stack **20**, the dielectric layers **21** and the gate electrodes **22** may be alternately stacked, and a plurality of the channel structures **24** may penetrate the dielectric layers **21** and the gate electrodes **22**.

[0036] The gate electrodes **22** may include a low-resistance material. The gate electrodes **22** may be a metal-based material. The gate electrodes **22** may include a metal, a metal silicide, a metal nitride, or a combination thereof. For example, the metal may include nickel, cobalt, platinum, titanium, tantalum or tungsten. The metal silicide may include nickel silicide, cobalt silicide, platinum silicide, titanium silicide, tantalum silicide or tungsten silicide. The gate electrodes **22** may include titanium nitride and tungsten.

[0037] Referring to FIG. **2**E, a contact-level dielectric layer **30** may be formed over the memory cell stack **20**. The contact-level dielectric layer **30** may have a multi-layer level structure including a plurality of dielectric layers. For example, the contact-level dielectric layer **30** may include a first inter-layer dielectric layer **31**, a first etch stop layer **32**, a second inter-layer dielectric layer **33**, and a second etch stop layer **34**. The first and second inter-layer dielectric layers **31** and **33** may be formed of silicon oxide, and the first and second etch stop layers **32** and **34** may be formed of silicon nitride. According to another embodiment, the first and second inter-layer dielectric layers **31** and **33** may include carbon-containing silicon oxide, and the first and second etch stop layers **32** and **34** may include carbon-containing silicon nitride.

[0038] Subsequently, a contact hole **35** may be formed in the contact-level dielectric layer **30**. The contact hole **35** may be formed by etching the contact-level dielectric layer **30**, and the contact hole **35** may penetrate the contact-level dielectric layer **30**. The contact hole **35** may expose a portion of the conductive pad **28**. The contact hole **35** may expose the channel layer **26** of the channel structure **24**.

[0039] Referring to FIG. **2**F, a contact plug **36** filling the contact hole **35** may be formed. The contact plug **36** may include a metal, a metal nitride, or a combination thereof. The contact plug **36** may include a barrier layer **37** and a plug material **38**. The barrier layer **37** may be titanium nitride, and the plug material **38** may be tungsten. The contact plug **36** may be electrically connected to the conductive pad **28** and the channel layer **26**.

[0040] Referring to FIG. **2**G, the upper surface of the contact plug **36** may be recessed. As a result, a recess portion **39** may be formed over the contact plug **36**. Due to the recess portion **39**, the upper surface of the contact plug **36** may be positioned at a lower level than the upper surface of the second etch stop layer **34**. Hereinafter, the contact plug **36** may be simply referred to as a recessed contact plug **36**.

[0041] Referring to FIGS. **2**H and **21**, a bit line-level dielectric layer **40** may be formed over the recessed contact plug **36**. The bit line-level dielectric layer **40** may have a multi-layer-level structure including a plurality of dielectric layers. For example, the bit line-level dielectric layer **40** may be formed by forming a spacer layer **41** and then forming a third inter-layer dielectric layer **42** over the spacer layer **41**. The spacer layer **41** may be silicon nitride, and the third inter-layer dielectric layer **42** may be silicon oxide. According to another embodiment, the third inter-layer dielectric layer **42** may include carbon-containing silicon oxide, and the spacer layer **41** may include carbon-containing silicon nitride.

[0042] The spacer layer **41** may cover the upper surface of the recessed contact plug **36** and the upper surface of the second etch stop layer **34**. The spacer layer **41** may include a plurality of rounding portions **41**R, and the rounding portions **41**R may cover the edges of the second etch stop layer **34** providing a recessed portion (**39** in FIG. **2**G). The rounding portions **41**R of the spacer layer **41** may partially fill the recess portion **39** of FIG. **2**G.

[0043] Referring to FIGS. **2**J and **2**K, a plurality of trenches **50** may be formed in the bit line-level dielectric layer **40**. The trenches **50** may be features that provide a space where a bit line is to be formed, and a portion of the trenches **50** may expose surfaces of the recessed contact plug **36**. The other portion of the trenches **50** may expose the surface of the second etch stop layer **34**.

[0044] Double patterning may be performed to form the trenches **50**. The trenches **50** may be referred to as a damascene pattern.

[0045] The process of forming the trenches **50** may include forming a preliminary trench **50'** (see FIG. **2**J) by etching the third inter-layer dielectric layer **42**, and etching the spacer layer **41** (see FIG. **2**K) below the preliminary trench **50'** in order to form the trenches **50**. As described above, the trenches **50** may be formed by sequentially etching the third inter-layer dielectric layer **42** and the spacer layer **41**. The double patterning process for forming the preliminary trenches **50'** will be described with reference to FIGS. **3**A to **3**H.

[0046] The spacer layer **41** may serve as an etch stop layer during an etching process for forming the preliminary trenches **50'**.

[0047] Referring to FIG. **2**L, bit lines **51** filling the trenches **50** may be formed. The bit lines **51** may include a metal, a metal nitride, or a combination thereof. The bit lines **51** may include titanium nitride and tungsten. The bit lines **51** may be formed of tungsten alone.

[0048] Hereinafter, a method of forming the trenches **50** and the bit lines **51** will be described. For the sake of convenience in description, the memory cell stack **20** and the substrate **11** will be omitted.

[0049] FIGS. **3**A to **3**H are cross-sectional views illustrating a method for forming preliminary trenches **50'** shown in FIG. **2**J.

[0050] Referring to FIG. **3**A, a first hard mask layer **43** may be formed over the bit line-level dielectric layer **40**. The first hard mask layer **43** may have an etch selectivity with respect to the third inter-layer dielectric layer **42**. The first hard mask layer **43** may include polysilicon.

[0051] A second hard mask layer **44** may be formed over the first hard mask layer **43**. The second hard mask layer **44** may have an etch selectivity with respect to the first hard mask layer **43** and the third inter-layer dielectric layer **42**. The second hard mask layer **44** may include an amorphous carbon layer.

[0052] A third hard mask layer **45** may be formed over the second hard mask layer **44**. The third hard mask layer **45** may have an etch selectivity with respect to the second hard mask layer **44**, the first hard mask layer **43**, and the third inter-layer dielectric layer **42**. The third hard mask layer **45** may include silicon oxynitride. The third hard mask layer **45** may also be referred to as an anti-reflection layer.

[0053] Subsequently, a mask layer **46** may be formed over the third hard mask layer **45**. The mask layer **46** may include a photoresist pattern. The mask layer **46** may extend long in one direction. For example, the mask layer **46** may be a photoresist pattern of a line-shape.

[0054] Referring to FIG. **3**B, the third hard mask layer **45** may be etched by using the mask layer **46**. As a result, a third hard mask layer pattern **45**P may be formed over the second hard mask layer **44**. The third hard mask layer pattern **45**P may extend long in one direction.

[0055] Referring to FIG. **3**C, the second hard mask layer **44** may be etched by using the mask layer **46** and the third hard mask layer pattern **45**P. As a result, a second hard mask layer pattern **44**P may be formed over the first hard mask layer **43**. The second hard mask layer pattern **44**P may extend long in one direction. The second hard mask layer pattern **44**P may be an amorphous carbon layer pattern.

[0056] Subsequently, the mask layer **46** may be removed.

[0057] According to another embodiment, after the mask layer **46** is removed, the second hard mask layer **44** may be etched by using the third hard mask layer pattern **45**P as an etch barrier.

[0058] Referring to FIG. **3**D, after the third hard mask layer pattern **45**P is removed, a sacrificial spacer layer **47**A may be formed over the second hard mask layer pattern **44**P. The sacrificial spacer layer **47**A may include silicon oxide.

[0059] Referring to FIG. **3**E, a sacrificial spacer **47** may be formed. An etch-back process of the sacrificial spacer layer **47**A may be performed to form the sacrificial spacer **47**. The sacrificial spacers **47** may be formed on both sidewalls of the second hard mask layer pattern **44**P. The space between the sacrificial spacers **47**, that is, first gaps G**1** may be formed.

[0060] Referring to FIG. **3**F, the second hard mask layer pattern **44**P may be removed. As a result, second gaps G**2** may be formed in the sacrificial spacer **47**. A plurality of first gaps G**1** and a plurality of second gaps G**2** may be disposed laterally. The first gaps G**1** and the second gaps G**2** may be alternately positioned laterally. The first gaps G**1** and the second gaps G**2** may have the same line width.

[0061] Referring to FIG. **3**G, the first hard mask layer **43** may be etched by using the sacrificial spacer **47** as an etch barrier. As a result, a first hard mask layer pattern **43**P may be formed. The first hard mask layer pattern **43**P may include a plurality of trench-type-openings **43**H.

[0062] Referring to FIG. **3**H, the third inter-layer dielectric layer **42** may be etched by using the first hard mask layer

pattern **43**P as an etch barrier. As a result, preliminary trenches **50'** may be formed. An etching process for forming the preliminary trenches **50'** may stop on the spacer layer **41**.

[0063] Subsequently, referring to FIG. **2**K, the spacer layer **41** below the preliminary trenches **50'** may be etched. As a result, trenches **50** may be formed.

[0064] Subsequently, the first hard mask layer pattern **43**P may be removed.

[0065] Subsequently, referring to FIG. **2**L, a bit line **51** filling the trenches **50** may be formed. The bit line **51** may include a stack of a barrier layer, a seed layer, and a metal layer. The bit line **51** may include copper.

[0066] According to an embodiment, the process for coupling vertical channel structures to a bit line may be simplified.

[0067] According to an embodiment, a contact area between a contact plug and a bit line may be secured by using a spacer layer.

What is claimed is:

1. A method for fabricating a semiconductor device, comprising:
- forming channel structures comprising a channel layer that penetrates a stack body;
- forming a contact-level dielectric layer over the stack body and the channel structures;
- forming a contact hole penetrating the contact-level dielectric layer;
- forming contact plugs in the contact hole, the contact plugs coupled to the channel layers of the channel structures;
- recessing the contact plugs to form upper surfaces of the contact plugs that are lower than an upper surface of the contact-level dielectric layer;
- forming a bit line-level dielectric layer including a spacer layer over the recessed contact plugs;
- etching the bit line-level dielectric layer to form trenches that expose the recessed contact plugs; and
- forming a bit line in one or more of the trenches.

2. The method of claim **1**, wherein the spacer layer includes rounding portions that respectively cover upper surfaces of the recessed contact plugs.

3. The method of claim **2**, wherein the rounding portions of the spacer layer are respectively in contact with a sidewall of a bottom portion of the bit line.

4. The method of claim **1**, wherein the spacer layer includes silicon nitride.

5. The method of claim **1**, wherein the forming of the contact-level dielectric layer over the stack body includes:
- forming a first etch stop layer over the channel structures;
- forming an inter-layer dielectric layer over the first etch stop layer; and
- forming a second etch stop layer over the inter-layer dielectric layer.

6. The method of claim **1**, wherein the forming of the trenches includes:
- forming a first hard mask layer over the bit line-level dielectric layer;
- forming a second hard mask layer over the first hard mask layer;
- etching the second hard mask layer to form second hard mask layer patterns;
- forming sacrificial spacers on sidewalls of the second hard mask layer patterns;
- etching the first hard mask layer by using the sacrificial spacer as an etch barrier to form a plurality of first hard mask layer patterns over the bit line-level dielectric layer; and
- etching the bit line-level dielectric layer by using the first hard mask layer pattern as an etch barrier.

7. The method of claim **6**, wherein the sacrificial spacer is formed by deposition of silicon oxide and an etch-back process.

8. The method of claim **6**, wherein the first hard mask layer includes polysilicon, and the second hard mask layer includes an amorphous carbon layer.

9. The method of claim **1**, wherein in the forming of the trenches,
- the trenches are arranged laterally to each other, and
- the trenches include first trenches that expose the contact plugs and second trenches between the first trenches.

10. The method of claim **9**, wherein the first trenches and the second trenches are isolated from each other by the spacer layer.

11. The method of claim **9**, wherein bottom surfaces of the first trenches are positioned at a lower level than bottom surfaces of the second trenches.

12. A semiconductor device, comprising:
- a plurality of channel structures each including a channel layer that penetrates a memory cell stack;
- a contact-level dielectric layer formed over the plurality of channel structures and including a contact hole that exposes each of the plurality of channel structures;
- recessed contact plugs respectively coupled to the channel layer through the contact hole and having an upper surface which is lower than an upper surface of the contact-level dielectric layer;
- a bit line-level dielectric layer formed over the recessed contact plugs; and
- a plurality of bit lines formed in the bit line-level dielectric layer,
- wherein the bit line-level dielectric layer includes a spacer layer in contact with sidewalls of bottom portions of the plurality of bit lines, and
- wherein rounding portions of the spacer layer cover edges of the second etch stop layer over the contact plug.

13. The semiconductor device of claim **12**, wherein the spacer layer covers portions of an upper surface of the recessed contact plugs.

14. The semiconductor device of claim **12**, wherein the spacer layer includes silicon nitride.

15. The semiconductor device of claim **12**, wherein the bottom surfaces of the bit lines are self-aligned to the spacer layer.

16. The semiconductor device of claim **12**, wherein the bit lines and the contact plugs are in direct contact with each other.

17. The semiconductor device of claim **12**, wherein the recessed contact plugs include titanium nitride and tungsten.

18. The semiconductor device of claim **12**, wherein the recessed contact plugs have a greater width than the bit lines.

19. The semiconductor device of claim **12**, wherein the spacer layer includes the rounding portions that respectively cover upper surfaces of the recessed contact plugs.

20. The semiconductor device of claim **12**, wherein the contact-level dielectric layer includes:
- a first etch stop layer formed over a first inter-layer dielectric layer;

a second inter-layer dielectric layer formed over the first etch stop layer; and

a second etch stop layer formed over the second inter-layer dielectric layer,

wherein the second etch stop layer is covered by the spacer layer, and wherein the second etch stop layer and the spacer layer include substantially the same material.

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