| | |
|---|---|
| United States Patent Application Publication | 20250266331 |
| Kind Code | A1 |
| Publication Date | August 21, 2025 |
| Inventor(s) | NII; Akinori |


# SEMICONDUCTOR DEVICE


## Abstract

A semiconductor device includes a conductive member, a semiconductor element, and a sealing resin. The conductive member includes a wiring portion, and a terminal portion connected to the wiring portion. The semiconductor element faces the wiring portion in a thickness direction and includes an electrode. The wiring portion includes a first portion overlapping with the terminal portion and a second portion not overlapping with the terminal portion as viewed in the thickness direction. The second portion includes a first area between a part overlapping with the electrode as viewed in the thickness direction and a part where the second portion is connected to the first portion. The first portion and the first area constitute a second area as viewed in the thickness direction. The ratio of the second area to the first wiring portion is 60% or less.



**Inventors:** **NII; Akinori (Kyoto-shi, JP)**

**Applicant:** **Rohm Co., Ltd.** (Kyoto-shi, JP)



**Family ID:** **1000008452094**

**Appl. No.:** **19/052834**

**Filed:** **February 13, 2025**

## Foreign Application Priority Data

| | | |
|---|---|---|
| JP | 2024-023528 | Feb. 20, 2024 |

## Publication Classification

**Int. Cl.:** **H01L23/495** (20060101); **H01L23/00** (20060101); **H01L23/31** (20060101)

**U.S. Cl.:**

CPC **H01L23/49548** (20130101); **H01L24/16** (20130101); H01L23/3121 (20130101); H01L23/49579 (20130101); H01L2224/16245 (20130101)

## Background/Summary

TECHNICAL FIELD
[0001] This disclosure relates to a semiconductor device.
BACKGROUND ART
[0002] Various configurations of semiconductor devices with semiconductor elements have been proposed. JP-A-2020-77694 discloses an example of a conventional semiconductor device. The conventional semiconductor device disclosed includes a lead and a semiconductor element. The lead includes a plurality of terminal portions. In the semiconductor device disclosed in JP-A-2020-77694, the semiconductor element is mounted on the lead by flip-chip mounting. The lead includes an obverse face facing one side of a thickness direction. The semiconductor element includes a plurality of electrodes provided on a side face facing the obverse face, and the plurality of electrodes are bonded to the obverse face of the lead via a bonding layer comprising, for example, solder. The lead is electrically connected to an internal circuit of the semiconductor element via at least one of the plurality of electrodes. In the semiconductor device disclosed in JP-A-2020-77694, an electrical current flows between the semiconductor element and the lead via the electrode. The lead is involved in the conduction path between the semiconductor element and a wiring board on which the semiconductor device is mounted. Semiconductor devices configured from such a way have room for improvement in their electrical characteristics.

---

## Description

BRIEF DESCRIPTION OF THE DRAWINGS
[0003] FIG. **1** is a perspective view of a semiconductor device according to a first embodiment of the present disclosure.
[0004] FIG. **2** is a plan view of the semiconductor device according to the first embodiment of the present disclosure (the sealing resin is omitted).
[0005] FIG. **3** is a plan view of the semiconductor device according to the first embodiment of the present disclosure (the semiconductor element and the sealing resin are omitted).
[0006] FIG. **4** is a bottom view of the semiconductor device according to the first embodiment of the present disclosure.
[0007] FIG. **5** is a front view of the semiconductor device according to the first embodiment of the present disclosure.
[0008] FIG. **6** is a back view of the semiconductor device according to the first embodiment of the present disclosure.
[0009] FIG. **7** is a right-side view of the semiconductor device according to the first embodiment of the present disclosure.
[0010] FIG. **8** is a left-side view of the semiconductor device according to the first embodiment of the present disclosure.
[0011] FIG. **9** is a cross-sectional view taken along a line IX-IX in FIG. **3**.
[0012] FIG. **10** is a cross-sectional view taken along a line X-X in FIG. **3**.
[0013] FIG. **11** is a cross-sectional view taken along a line XI-XI in FIG. **3**.
[0014] FIG. **12** is a cross-sectional view taken along a line XII-XII in FIG. **3**.
[0015] FIG. **13** is a cross-sectional view taken along a line XIII-XIII in FIG. **3**.
[0016] FIG. **14** is a partially enlarged view of FIG. **3**.
[0017] FIG. **15** is a partially enlarged view of FIG. **9**.
[0018] FIG. **16** is a plan view similar to FIG. **3**, showing a semiconductor device according to a first variation of the first embodiment.

[0019] FIG. **17** is a cross-sectional view taken along a line XVII-XVII in FIG. **16**.
[0020] FIG. **18** is a cross-sectional view taken along a line XVIII-XVIII in FIG. **16**.
[0021] FIG. **19** is a partially enlarged view of FIG. **16**.
[0022] FIG. **20** is a partially enlarged view of FIG. **17**.
[0023] FIG. **21** is a plan view similar to FIG. **3**, showing a semiconductor device according to a second variation of the first embodiment.
[0024] FIG. **22** is a cross-sectional view taken along a line XXII-XXII in FIG. **21**.
[0025] FIG. **23** is a cross-sectional view taken along a line XXIII-XXIII in FIG. **21**.
[0026] FIG. **24** is a partially enlarged view of FIG. **21**.
[0027] FIG. **25** is a partially enlarged view of FIG. **22**.

## DETAILED DESCRIPTION OF EMBODIMENTS

[0028] The following describes preferred embodiments of the present disclosure in detail with reference to the drawings.
[0029] In the present disclosure, the terms such as “first”, “second”, and “third” are used merely as labels and are not intended to impose ordinal requirements on the items to which these terms refer.
[0030] In the description of the present disclosure, the expression “An object A is formed in an object B”, and “An object A is formed on an object B” imply the situation where, unless otherwise specifically noted, “the object A is formed directly in or on the object B”, and “the object A is formed in or on the object B, with something else interposed between the object A and the object B”. Likewise, the expression “An object A is disposed in an object B”, and “An object A is disposed on an object B” imply the situation where, unless otherwise specifically noted, “the object A is disposed directly in or on the object B”, and “the object A is disposed in or on the object B, with something else interposed between the object A and the object B”. Further, the expression “An object A is located on an object B” implies the situation where, unless otherwise specifically noted, “the object A is located on the object B, in contact with the object B”, and “the object A is located on the object B, with something else interposed between the object A and the object B”. Still further, the expression “An object A overlaps with an object B as viewed in a certain direction” implies the situation where, unless otherwise specifically noted, “the object A overlaps with the entirety of the object B”, and “the object A overlaps with a part of the object B”. Also, the phrase “an object A (or the material thereof) contains a material C” includes “an object A (or the material thereof) is made of a material C” and “an object A (or the material thereof) is mainly composed of a material C”. Furthermore, in the description of the present disclosure, the expression “A surface A faces (a first side or a second side) in a direction B” is not limited to the situation where the angle of the surface A to the direction B is **90**° and includes the situation where the surface A is inclined with respect to the direction B.

### First Embodiment

[0031] The semiconductor device of a first embodiment of the present disclosure will be described based on FIGS. **1** to **15**. The semiconductor device A**10** in the present embodiment includes a first conductive member **1**A, a second conductive member **1**B, a pair of third conductive members **1**C, pluralities of conductive members **1**D, **1**E, **1**F, a semiconductor element **3** and a sealing resin **4**. The package format of the semiconductor device A**10** is a QFN (Quad For Non-Lead Package). The package format of the semiconductor device A**10** is not to QFN. The specific configuration of the limited semiconductor element **3** is not particularly limited, and the semiconductor element **3** is, for example, a flip-chip type LSI (Large Scale Integration).
[0032] FIG. **1** is a perspective view of the semiconductor device A**10**. FIG. **2** is a plan view of the semiconductor device A**10**, with the sealing resin **4** transparent. FIG. **3** is a plan view of semiconductor device A**10**, in which the semiconductor element **3** and the sealing resin **4** are omitted. FIG. **4** is a bottom view of the semiconductor device A**10**. FIG. **5** is a front view of the semiconductor device A**10**. FIG. **6** is a back view of the semiconductor device A**10**. FIG. **7** is a right-side view of the semiconductor device A**10**. FIG. **8** is a left-side view of the semiconductor

device A**10**. FIG. **9** is a cross-sectional view taken along a line IX-IX in FIG. **3**. FIG. **10** is a cross-sectional view taken along a line X-X in FIG. **3**. FIG. **11** is a cross-sectional view taken along a line XI-XI in FIG. **3**. FIG. **12** is a cross-sectional view taken along a line XII-XII in FIG. **3**. FIG. **13** is a cross-sectional view taken along a line XIII-XIII in FIG. **3**. FIG. **14** is a partially enlarged view of FIG. **3**. FIG. **15** is a partially enlarged view of FIG. **9**. In FIG. **2**, the omitted sealing resin **4** is indicated as an imaginary line (double-dotted line). In FIG. **3**, the omitted semiconductor element **3** and sealing resin **4** are indicated as imaginary lines (two dotted lines), respectively.

[0033] In the following explanation, the thickness direction (the plan-view direction) of the semiconductor device (the first conductive member **1**A) is referred to as a "thickness direction z". A direction orthogonal to the thickness direction z is referred to as a "first direction x". direction orthogonal to the thickness direction z and the first direction x is referred to as a "second direction y".

[0034] In the explanation of the semiconductor device A**10**, one side of the first direction x is referred to as an "x**1** side of the first direction x", and the other side is referred to as an "x**2** side of the first direction x". One side of the second direction y is referred to as an "y**1** side of the second direction y", and the other side of the second direction y is referred to as an "y**2** side of the second direction y". One side of the thickness direction z is referred to as an "z**1** side of the thickness direction z", and the other side of the thickness direction z is referred to as an "z**2** side of the thickness direction z". Note that the terms such as "top", "bottom", "upward", "downward", "upper surface", and "lower surface" are used to indicate the relative position between parts, etc., in the thickness direction z and do not necessarily define the relationship with respect to the direction of gravity.

[0035] The sealing resin **4** covers the first conductive member **1**A, the second conductive member **1**B, the pair of third conductive members **1**C, a part of each of the pluralities of conductive members **1**D, **1**E, **1**F, and the semiconductor element **3**, as shown in FIGS. **1** to **3** and **9** to **13**. The sealing resin **4** has electrical insulating properties. The constituent material of the sealing resin **4** is, for example, black epoxy resin. As viewed in the thickness direction z, the sealing resin **4** is rectangular.

[0036] As shown in FIGS. **5** to **8**, the sealing resin **4** includes a resin obverse face **41**, a resin reverse face **42**, a first resin side face **431**, a second resin side face **432**, a third resin side face **433**, and a fourth resin side face **434**. The resin obverse face **41** and the resin reverse face **42** face opposite each other in the thickness direction z. The resin obverse face **41** faces the z**1** side of the thickness direction Z. The resin reverse face **42** faces the z**2** side of the thickness direction z. The first resin side face **431** and the second resin side face **432** face opposite each other in the first direction x. The first resin side face **431** faces the x**1** side of the first direction x. The second resin side face **432** faces the x**2** side of the first direction x. The third resin side face **433** and the fourth resin side face **434** face opposite each other in the second direction y. The third resin side face **433** faces the y**1** side of the second direction y. The fourth resin side face **434** faces the y**2** side of the second direction y.

[0037] The first conductive member **1**A, the second conductive member **1**B, the pair of third conductive members **1**C, and the pluralities of conductive members **1**D, **1**E, **1**F each carry a semiconductor element **3**, as shown in FIGS. **9** to **13**. These conductive members **1**A to **1**F provide, for example, a conductive path between the semiconductor element **3** and wiring substrates on which the semiconductor device A**10** is mounted. The constituent materials of the conductive members **1**A-**1**F include, for example, copper (Cu). The conductive members **1**A-**1**F may be formed from the same lead frame.

[0038] As shown in FIG. **3**, the first conductive member **1**A is located on the center of the semiconductor device A**10** in the second direction y. The first conductive member **1**A includes a first wiring portion **11** and a first terminal portion **21**, as shown in FIGS. **3**, **4** and **9**. The first wiring portion **11** extends in the first direction x as a whole. In the present embodiment, the first wiring

portion **11** extends from the end on the x**1** side of the first direction x to the end on the x**2** side of the first direction x in the semiconductor device A**10**. The first wiring portion **11** includes a first obverse face **11***a* and a first intermediate face **11***b*. The first obverse face **11***a* faces the z**1** side of the thickness direction z. The first obverse face **11***a* faces the semiconductor element **3** and supports the semiconductor element **3**. The first intermediate face **11***b* is offset in the z**2** side of the thickness direction z with respect to the first obverse face **11***a*. The first intermediate face **11***b* faces the opposite side of the first obverse face **11***a* (z**2** side of the thickness direction z). The first obverse face **11***a* and the first intermediate face **11***b* are covered by the sealing resin **4**. The first obverse face **11***a*, which supports the semiconductor element **3**, may be plated with silver (Ag).

[0039] The first terminal portion **21** is connected to the first wiring portion **11** on the z**2** side of the thickness direction Z. The first terminal portion **21** extends in the first direction x. The first terminal portion **21** extends from the end on the x**1** side of the first direction x to the end on the x**2** side of the first direction x in the semiconductor device A**10**. As viewed in the thickness direction z, the first terminal portion **21** has a long rectangular shape with the first direction x as the longitudinal direction. The first terminal portion **21** includes a first reverse face **21***a* and a pair of end faces **21***b*. The first reverse face **21***a* faces opposite to the first obverse face **11***a* of the first wiring portion **11**. The first reverse face **21***a* faces the z**2** side of the thickness direction z. The first reverse face **21***a* is exposed from the resin reverse face **42** of the sealing resin **4**. The pair of end faces **21***b* are located at both ends of the first terminal portion **21** in the first direction x. One end face **21***b* faces the x**1** side of the first direction x and is exposed from the first resin side face **431** of the sealing resin **4**. The other end face **21***b* faces the x**2** side of the first direction x and is exposed from the second resin side face **432** of the sealing resin **4**. Each of the pair of end faces **21***b* is connected to the first reverse face **21***a*. The first reverse face **21***a* and the pair of end faces **21***b*, which are exposed from the sealing resin **4**, may be plated with tin (Sn). Alternatively, a plurality of metals may be applied, for example, nickel (Ni), palladium (Pd), and gold (Au), stacked in this order.

[0040] The first wiring portion **11** overlaps with the entirety of the first terminal portion **21** as viewed in the thickness direction z. Hence, the area of the first wiring portion **11** is larger than the area of the first terminal portion **21** as viewed in the thickness direction z. In the semiconductor device A**10**, the first wiring portion **11** includes a first portion **111** and a second portion **112**. The first portion **111** is a part overlapping with the first terminal portion **21** as viewed in the thickness direction z. The second portion **112** is a part not overlapping with the first terminal portion **21** as viewed in the thickness direction z. The first terminal portion **21** is connected to the first portion **111** on the z**2** side of the thickness direction z. The second portion **112**, which does not overlap with the first terminal portion **21** as viewed in the thickness direction z, includes a first intermediate face **11***b*. The first intermediate face **11***b* is located between the first obverse face **11***a* and the first reverse face **21***a* in the thickness direction z. Details of the first wiring portion **11** will be described later.

[0041] As shown in FIG. **3**, the second conductive member **1**B is located on the y**2** side of the second direction y in the semiconductor device A**10**. The second conductive member **1**B is spaced apart from the first conductive member **1**A on the y**2** side of the second direction y, and is adjacent to the first conductive member **1**A. The second conductive member **1**B includes a second wiring portion **12** and a second terminal portion **22**, as shown in FIGS. **3**, **4**, **9**, **11**, and **12**. The second wiring portion **12** includes a part extending in the first direction x and a part extending in the second direction y, and generally has a T-shape as viewed in the thickness direction z. In the present embodiment, the part extending in the first direction x of the second wiring portion **12** extends from the end on the x**1** side of the first direction x to the end on the x**2** side of the first direction x in the semiconductor device A**10**. The part extending in the second direction y of the second wiring portion **12** extends from the center of the part extending in the first direction x to the end on the y**2** side of the second direction y in the semiconductor device A**10**. The second wiring

portion **12** includes a second obverse face **12***a* and a second intermediate face **12***b*. The second obverse face **12***a* faces the z**1** side of the thickness direction z. The second obverse face **12***a* faces the semiconductor element **3** and supports the semiconductor element **3**. The second intermediate face **12***b* is offset in the z**2** side of the thickness direction z with respect to the second obverse face **12***a*. The second intermediate face **12***b* faces opposite side of the second obverse face **12***a* (z**2** side of the thickness direction z). The second obverse face **12***a* and the second intermediate face **12***b* are covered by the sealing resin **4**. The second obverse face **12***a*, which supports the semiconductor element **3**, may be plated with silver.

[0042] The second terminal portion **22** is connected to the second wiring portion **12** on the z**2** side of the thickness direction z. The second terminal portion **22** extends in the second direction y. The second terminal portion **22** extends in the semiconductor device A**10** from the center in the first direction x to the end on the y**2** side of the second direction y. As viewed in the thickness direction z, the second terminal portion **22** has a long rectangular shape with the second direction y as the longitudinal direction. The second terminal portion **22** includes a second reverse face **22***a* and an end face **22***b*. The second reverse face **22***a* faces the opposite side of the second obverse face **12***a* of the second wiring portion **12**. The second reverse face **22***a* faces the z**2** side of the thickness direction z. The second reverse face **22***a* is exposed from the resin reverse face **42** of the sealing resin **4**. The end face **22***b* faces the y**2** side of the second direction y. The end face **22***b* is connected to the second reverse face **22***a* and is exposed from the fourth resin side face **434** of the sealing resin **4**. The second reverse face **22***a* and the end face **22***b*, which are exposed from the sealing resin **4**, may be plated with tin. Alternatively, a plurality of metals may be applied, for example, nickel, palladium, and gold stacked in this order.

[0043] The second wiring portion **12** overlaps with the entirety of the second terminal portion **22** as viewed in the thickness direction z. The second wiring portion **12** includes a protruding portion **121**. In the second wiring portion **12**, the protruding portion **121** protrudes from the center in the first direction x of the part extending in the first direction x to the y**1** side of the second direction y.

[0044] As shown in FIG. **3**, the pair of third conductive members **1**C are located on the y**2** side of the second direction y in the semiconductor device A**10**. The pair of third conductive members **1**C are separated from each other in the first direction x. The pair of third conductive members **1**C are located on both sides of the first direction x, respectively, sandwiching the second conductive member **1**B (second terminal portion **22**). One of the third conductive members **1**C is located on the x**1** side of the first direction x and the other of the third conductive members **1**C is located on the x**2** side of the first direction x. Each third conductive member **1**C includes a third wiring portion **13** and a third terminal portion **23**, as shown in FIGS. **3**, **4** and **12**. The third wiring portion **13** includes a part extending in the first direction x and a part extending in the second direction y, and generally has an L-shape as viewed in the thickness direction z. The third wiring portion **13** includes a third obverse face **13***a* and a third intermediate face **13***b*. The third obverse face **13***a* faces the z**1** side of the thickness direction z. The third obverse face **13***a* faces the semiconductor element **3** and supports the semiconductor element **3**. The third intermediate face **13***b* is offset in the z**2** side of the thickness direction z with respect to the third obverse face **13***a*. The third intermediate face **13***b* faces the opposite side of the third obverse face **13***a* (z**2** side of the thickness direction z). The third obverse face **13***a* and the third intermediate face **13***b* are covered by the sealing resin **4**. The third obverse face **13***a*, which supports the semiconductor element **3**, may be plated with silver.

[0045] Each third terminal portion **23** is connected to the third wiring portion **13** on the z**2** side of the thickness direction z. Each third terminal portion **23** includes a part extending in the first direction x and a part located on the y**2** side of the second direction y, these two parts being separated from each other. Each third wiring portion **13** overlaps with the entirety of the relevant third terminal portion **23** as viewed in the thickness direction z. Each third terminal portion **23** includes a third reverse face **23***a* and end faces **23***b* and **23***c*.

[0046] The third reverse face **23***a* faces the opposite side of the third obverse face **13***a* of the third wiring portion **13**. The third reverse face **23***a* faces the z**2** side of the thickness direction z. The third reverse face **23***a* is exposed from the resin reverse face **42** of the sealing resin **4**. The respective end faces **23***b* face the x**1** side or the x**2** side of the first direction x. The respective end faces **23***b* are connected to the third reverse face **23***a* and are exposed from the first resin side face **431** or the second resin side face **432** of the sealing resin **4**. Each end face **23***c* faces the y**2** side of the second direction y. Each end face **23***c* is connected to the third reverse face **23***a* and is exposed from fourth resin side face **434** of the sealing resin **4**. The third reverse face **23***a* and the end faces **23***b*, **23***c*, which are exposed from the sealing resin **4**, may be plated with tin. Alternatively, a plurality of metals may be applied, for example, nickel, palladium, and gold stacked in this order.
[0047] As shown in FIG. **3**, the plurality of conductive members **1**D are located on the y**2** side of the second direction y in the semiconductor device A**10**. In the illustrated example, a pair of conductive members **1**D are spaced apart from each other in the first direction x. The pair of conductive members **1**D are located on both sides of the first direction X**1** respectively, sandwiching the pair of third conductive members **1**C. One of the conductive members **1**D is located on the x**1** side of the first direction x and near a corner on the y**2** side of the second direction y, and the other of the conductive members **1**D is located on the x**2** side of the first direction x and near a corner on the y**2** side of the second direction y. Each conductive member **1**D includes a wiring portion **14** and a terminal portion **24**, as shown in FIGS. **3** and **4**. The wiring portion **14** includes an obverse face **14***a*. The obverse face **14***a* faces the z**1** side of the thickness direction z. The obverse face **14***a* faces the semiconductor element **3** and supports the semiconductor element **3**. The obverse face **14***a* is covered by the sealing resin **4**. The obverse face **14***a*, which supports the semiconductor element **3**, may be plated with silver.
[0048] Each terminal portion **24** is connected to the wiring portion **14** on the z**2** side of the thickness direction z. Each wiring portion **14** overlaps with the entirety of the relevant terminal portion **24** as viewed in the thickness direction z. Each terminal portion **24** includes a reverse face **24***a* and end faces **24***b*, **24***c*. The reverse face **24***a* faces opposite to the obverse face **14***a* of the wiring portion **14**. The reverse face **24***a* faces the z**2** side of the thickness direction z. The reverse face **24***a* is exposed from the resin reverse face **42** of the sealing resin **4**. The respective end faces **24***b* face the x**1** side or the x**2** side of the first direction x. The respective end faces **24***b* are connected to the reverse face **24***a* and are exposed from the first resin side face **431** or the second resin side face **432** of the sealing resin **4**. Each end face **24***c* faces the y**2** side of the second direction y. Each end face **24***c* is connected to the reverse face **24***a* and is exposed from fourth resin side face **434** of the sealing resin **4**. The reverse face **24***a* and the end faces **24***b*, **24***c*, which are exposed from the sealing resin **4**, may be plated with tin. Alternatively, a plurality of metals may be applied, for example, nickel, palladium, and gold stacked in this order.
[0049] As shown in FIG. **3**, the plurality of conductive members **1**E are located on the y**1** side of the second direction y in the semiconductor device A**10**. The plurality of conductive members **1**E are spaced apart from each other in the first direction x. Each conductive member **1**E includes a wiring portion **15** and a terminal portion **25**, as shown in FIGS. **3**, **4**, and **9**. Each wiring portion **15** includes an obverse face **15***a* and an intermediate face **15***b*. The obverse face **15***a* faces the z**1** side of the thickness direction z. The obverse face **15***a* faces the semiconductor element **3** and supports the semiconductor element **3**. The intermediate face **15***b* is offset in the z**2** side of the thickness direction z with respect to the obverse face **15***a*. The intermediate face **15***b* faces the opposite side of the obverse face **15***a* (z**2** side of the thickness direction z). The obverse face **15***a* and the intermediate face **15***b* are covered by the sealing resin **4**. The obverse face **15***a*, which supports the semiconductor element **3**, may be plated with silver.
[0050] Each terminal portion **25** is connected to the wiring portion **15** on the z**2** side of the thickness direction z. Each wiring portion **15** overlaps with the entirety of the relevant terminal portion **25** as viewed in the thickness direction z. Each terminal portion **25** includes a reverse face

**25***a* and an The reverse face **25***a* faces opposite to the end face **25**b. obverse face **15***a* of the wiring portion **15**. The reverse face **25***a* faces the z**2** side of the thickness direction z. The reverse face **25***a* is exposed from the resin reverse face **42** of the sealing resin **4**. The end face **25***b* faces the y**1** side of the second direction y. The end face **25***b* is connected to the reverse face **25***a* and is exposed from the third resin side face **433** of the sealing resin **4**. The reverse face **25***a* and the end face **25***b*, which are exposed from the sealing resin **4**, may be plated with tin. Alternatively, a plurality of metals may be applied, for example, nickel, palladium, and gold stacked in this order.

[0051] As shown in FIG. **3**, the plurality of conductive members **1**F are disposed in the y**1** side of the second direction y with respect to the first conductive member **1**A. The conductive members **1**F are located between the first conductive member **1**A and the conductive members **1**E in the second direction y. Certain conductive members **1**F are located on the x**1** side of the first direction x in the semiconductor device A**10**. The remainder of the conductive members **1**F are located on the x**2** side of the first direction x in the semiconductor device A**10**. Each conductive member **1**F includes a wiring portion **16** and a terminal portion **26**, as shown in FIGS. **3**, **4** and **13**. The wiring portion **16** includes an obverse face **16***a* and an intermediate face **16***b*. The obverse face **16***a* faces the z**1** side of the thickness direction z. The obverse face **16***a* faces the semiconductor element **3** and supports the semiconductor element **3**. The intermediate face **16***b* is offset in the z**2** side of the thickness direction z with respect to the obverse face **16***a*. The intermediate face **16***b* faces the opposite side of the obverse face **16***a* (z**2** side of the thickness direction z). The obverse face **16***a* and the intermediate face **16***b*, are covered with the sealing resin **4**. The obverse face **16***a*, which supports the semiconductor element **3**, may be plated with silver.

[0052] Each terminal portion **26** is connected to the wiring portion **16** on the z**2** side of the thickness direction z. Each wiring portion **16** overlaps with the entirety of the relevant terminal portions **26** as viewed in the thickness direction z. Each terminal portion **26** includes a reverse face **26***a* and an end face **26***b*. The reverse face **26***a* faces opposite to the obverse face **16***a* of the wiring portion **16**. The reverse face **26***a* faces the z**2** side of the thickness direction z. The reverse face **26***a* is exposed from the resin reverse face **42** of the sealing resin **4**. The respective end faces **26***b* face the x**1** side or the x**2** side of the first direction x. The respective end faces **26***b* are connected to the reverse face **24***a* and are exposed from the first resin side face **431** or the second resin side face **432** of the sealing resin **4**. The reverse face **26***a* and the end faces **26***b*, which are exposed from the sealing resin **4**, may be plated with tin. Alternatively, a plurality of metals may be applied, for example, nickel, palladium, and gold stacked in this order.

[0053] The semiconductor element **3** is mounted on the first conductive member **1**A, the second conductive member **1**B, the pair of third conductive members **1**C, and the pluralities of conductive members **1**D, **1**E, **1**F, as shown in FIGS. **3** and **9** to **13**. The semiconductor element **3** includes an element body **30**, a plurality of first electrodes **31**, a plurality of electrodes **32**, and a plurality of electrodes **33**. Although detailed description and illustration are omitted, the element body **30** includes, for example, a semiconductor layer with an internal circuit, the internal circuit with a switching circuit and a controlling circuit electrically connected to the switching circuit. The switching circuit configures, for example, an n-channel MOSFET, and the controlling circuit controls the switching circuit to drive the switching circuit normally.

[0054] As shown in FIGS. **9** to **13**, in the thickness direction Z, the first electrodes **31**, the electrodes **32** and the electrodes **33** are located on the side facing the first obverse face **11***a*, the second obverse face **12***a*, the third obverse face **13***a* and the obverse faces **14***a* to **16***a*, respectively. The first electrodes **31**, the electrodes **32**, and the electrodes **33** are located below the element body **30** (on the z**2** side of the thickness direction z). Each of the first electrodes **31** is electrically connected to the first wiring portion **11** (first obverse face **11***a*) of the first conductive member **1**A via the bonding layer **39**. Hence, the element body **30** (semiconductor element **3**) is electrically connected to the first conductive member **1**A. Each of the electrodes **32** is electrically connected to either the second wiring portion **12** (second obverse face **12***a*) of the second conductive member **1**B

or the third wiring portion **13** (third obverse face **13***a*) of each third conductive member **1**C via the bonding layer **39**. Hence, the element body **30** (semiconductor element **3**) is electrically connected to the second conductive member **1**B and the pair of third conductive members **1**C. Each of the electrodes **33** is electrically connected to one of the wiring portion **14** (obverse face **14***a*) of each conductive member **1**D, the wiring portion **15** (obverse face **15***a*) of each conductive member **1**E and the wiring portion **16** ((obverse face **16***a*) of each conductive member **1**F via the bonding layer **39**. Hence, the element body **30** (semiconductor element **3**) is electrically connected to the pluralities of conductive members **1**D, **1**E, **1**F. The bonding layer **39** is electrically conductive. In the example represented by the semiconductor device A**10**, the bonding layer **39** is a metal containing tin and silver or a solder, for example.

[0055] Each of the first conductive member **1**A, the second conductive member **1**B, and the pair of third conductive members **1**C is electrically connected to the switching circuit of the semiconductor element **3** (element body **30**). Each of the first conductive member **1**A, the second conductive member **1**B, and the pair of third conductive members **1**C provides a path for the main circuit current to be switched by the semiconductor element **3** (aforementioned switching circuit), for example. Each of the pluralities of conductive members **1**D, **1**E, **1**F receives electric power (voltage) to drive the controlling circuit or electrical signals to be transmitted to the controlling circuit, for example.

[0056] The first wiring portion **11** will be described with reference to FIGS. **14** and **15**.

[0057] As described above, the first wiring portion **11** includes the first portion **111** and the second portion **112**. The first portion **111** is a part overlapping with the first terminal portion **21** as viewed in the thickness direction z, and the second portion **112** is a part not overlapping with the first terminal portion **21** as viewed in the thickness direction z. Each of the first portion **111** and the first terminal portion **21** extends in the first direction x.

[0058] In the present embodiment, the second portion **112** includes a first extending portion **113** and a second extending portion **114**. The first extending portion **113** extends from the first portion **111** to the y**1** side of the second direction y. The second extending portion **114** extends from the first portion **111** to the y**2** side of the second direction y. The first extending portion **113** has a length along the second direction y at the x**1** side or the x**2** side of the first direction x that is smaller than a length along the second direction y at the center of the first direction x. This is due to avoid interference between the first wiring portion **11** and its adjacent conductive members **1**F (wiring portion **16**) on the y**1** side of the second direction y (see FIG. **3**).

[0059] In the present embodiment, the first electrodes **31** are arranged along the first direction x. The first electrodes **31** overlap with the first portion **111** as viewed in the thickness direction z. More specifically, a part of each first electrode **31** overlaps with the first portion **111**, and the remainder of each first electrode **31** overlaps with the first extending portion **113** (second portion **112**) as viewed in the thickness direction z.

[0060] The first extending portion **113** (second portion **112**) includes a first region **112**A, which is a trapezoid region extending in the first direction x as viewed in the thickness direction z that overlaps with the first electrodes **31** and is connected to the first portion **111**. The first region **112**A is sum of a region with the first direction x as the longitudinal direction in which the first electrodes **31** are arranged and a region between each end of the region with the first direction x as the longitudinal direction and the most distant position from the boundary of the first extending portion **113** (second portion **112**) and the first portion **111**.

[0061] The first extending portion **113** includes a first inner portion **113**A and a first outer portion **113**B. The first inner portion **113**A is connected to the first portion **111**, and forms the first region **112**A. The first outer portion **113**B is connected to the first inner portion **113**A, and is offset in the y**1** side of the second direction y with respect to the first inner portion **113**A.

[0062] As shown in FIGS. **14** and **15**, a first dimension L**1**, which is a length of the first outer portion **113**B along the second direction y, is larger than a second dimension L**2**, which is a length

of the first terminal portion **21** along the second direction y. For example, the first dimension L**1** is 1.5 to 2.5 times the second dimension L**2**.

[0063] The second extending portion **114** includes a recess **114***a*. The recess **114***a* is recessed to the y**1** side of the second direction y more than other parts at the center of the second extending portion **114** in the first direction x. The recess **114***a* is provided corresponding to the protruding portion **121** of the second wiring portion **12** in the second conductive member **1**B. The recess **114***a* overlaps with entirety of the protruding portion **121** as viewed in the second direction y.

[0064] The part necessary for a path for electrical current between the semiconductor element **3** and the first terminal portion **21** (hereinafter referred to as a "necessary portion" as appropriate) in the first wiring portion **11** of the first conductive member **1**A includes the first portion **111**, which overlaps with the first terminal portion **21** as viewed in the thickness direction z, and the first region **112**A. In FIG. **14**, the entirety of the first wiring portion **11** is shown with hatching that diagonally falling to the right. Also, the necessary portion for flow of electrical current in the first wiring portion **11** (the first portion **111** and the first region **112**A) are shown with hatching that diagonally rising to the right. In the example shown in FIG. **14**, as viewed in the thickness direction z, the edge of the first region **112**A on the y**1** side of the second direction y corresponds to line segments extending in the first direction x tangential to the ends at the y**1** side of the second direction y of the first electrodes **31**, which are arranged in the first direction x.

[0065] As viewed in the thickness direction z, the ratio of a second area S**2** (sum of the area of the first portion **111** and the area of the first region **112**A), which is the area of the necessary portion of the path for electrical current (the first portion **111** and the first region **112**A) relative to a first area S**1**, which is the area of the entirety of the first wiring portion **11**, is 60% or less, for example. The ratio of the second area S**2** to the first area S**1** is preferably 20% to 50%. In the present embodiment shown in FIG. **14**, the ratio of the second area S**2** to the first area S**1** is 42.2%.

[0066] In the present embodiment, a part of the first wiring portion **11** that is unnecessary as the path for electrical current between the semiconductor element **3** and the first terminal portion **21** (hereinafter referred to as the "unnecessary portion" as appropriate) is other than the necessary portion (the first portion **111** and the first region **112**A). Specifically, the unnecessary portion is the second extending portion **114** and a part of the first extending portion **113** (mainly the outer first portion **113**B) other than the first region **112**A (inner first portion **113**A). The ratio of the area of the unnecessary portion of the path for electrical current is at least 40%, and preferably 50% to 80% in the first wiring portion **11**.

[0067] Next, the effects of the present embodiment will be described.

[0068] The semiconductor device A**10** includes the first conductive member **1**A, the semiconductor element **3** and the sealing resin **4**. The first conductive member **1**A includes the first wiring portion **11** and the first terminal portion **21** connected to the first wiring portion **11** on the z**2** side of the thickness direction z. The first wiring portion **11** includes the first obverse face **11***a* facing the z**1** side of the thickness direction z, and the first terminal portion **21** includes the first reverse face **21***a* facing the z**2** side of the thickness direction z, the first reverse face **21***a* being exposed from the resin reverse face **42** of the sealing resin **4**. The semiconductor element **3** includes the plurality of first electrodes **31** provided on the side facing the first obverse face **11***a* in the thickness direction z, the plurality of first electrodes **31** being electrically connected to the first obverse face **11***a*. The first wiring portion **11** includes the first portion **111** overlapping with the first terminal portion **21** as viewed in the thickness direction z, and a second portion **112** not overlapping with the first terminal portion **21** as viewed in the thickness direction z. As viewed in the thickness direction z, the ratio of the second area S**2** (sum of the area of the first portion **111** and the area of the first region **112**A), which is the area of the necessary portion of the path for electrical current, relative to the first area S**1**, which is the area of the entirety of the first wiring portion **11**, is 60% or less. Such a configuration results in that the ratio of the unnecessary portion of the path for electrical current is 40% or more in the first wiring portion **11**. The increased unnecessary the path for electrical

current in the first wiring portion **11** in this manner improves the electrical characteristics of the semiconductor device A**10** such as reducing the impedance between the semiconductor element **3** and the first terminal portion **21**.

[0069] The ratio of the area of the necessary portion of the path for electrical current (second area S**2**) to the area of the first wiring portion **11** (first area S**1**) is 20% to 50%. In this manner, the ratio of the area of the unnecessary portion of the path for electrical current is 50% to 80% in the first wiring portion **11**. Such a configuration reduces the excessively large ratio of the unnecessary portion in the first wiring portion **11**, which is desirable for downsizing the semiconductor device A**10**.

[0070] The first extending portion **113** includes the first inner portion **113**A and the first outer portion **113**B. The first inner portion **113**A is connected to the first portion **111** and forms the first region **112**A. The first outer portion **113**B is a portion connected to the first inner portion **113**A and is offset in the y**1** side of the second direction y with respect to the first inner portion **113**A. The first dimension L**1**, which is the length of the first outer portion **113**B along the second direction y, is larger than the second dimension L**2**, which is the length of the first terminal portion **21** along the second direction y. Such a configuration may efficiently reduce the ratio of the area of the necessary portion of the path for electrical current (second area S**2**) to the area of the first wiring portion **11** (first area S**1**). In other words, the ratio of the area of the unnecessary portion of the path for electrical current in the first wiring portion **11** may be efficiently increased. Therefore, this structure is suitable for improving electrical characteristics of the semiconductor device A**10**.

[0071] The first dimension L**1**, which is the length of the first outer portion **113**B along the second direction y, is 1.5 to 2.5 times the second dimension L**2**, which is the length of the first terminal portion **21** along the second direction y. The increased length of the first extending portion **113** in the second direction y (dimension **1** L**1**) in this manner improves the effect of preventing the sealing resin **4** from peeling off from the first conductive member **1**A, as well as improving the electrical characteristics of the semiconductor device A**10** described above.

[0072] FIGS. **16** to **25** illustrate variations of the semiconductor device of the present disclosure. In these figures, elements identical or similar to the above embodiment are denoted by the same reference signs as those of the above embodiment, and redundant explanations are omitted. Various parts of embodiments may be selectively used in any appropriate combination as long it as is technically compatible.

First Variation of the First Embodiment

[0073] FIGS. **16** to **20** show a semiconductor device A**11** according to a first variation of the first embodiment. FIG. **16** is a plan view similar to FIG. **3**, showing the semiconductor device A**11**. In FIG. **16**, the semiconductor element **3** and the sealing resin **4** are omitted for the sake of understanding. In FIGS. **16** to **20**, the omitted semiconductor element **3** and sealing resin **4** are shown as imaginary lines (two dotted lines), respectively. FIG. **17** is a cross-sectional view taken along a line XVII-XVII in FIG. **16**. FIG. **18** is a cross-sectional view taken along a line XVIII-XVIII in FIG. **16**. FIG. **19** is a partially enlarged view of FIG. **16**. FIG. **20** is a partially enlarged view of FIG. **17**.

[0074] The semiconductor device A**11** of the present variation differs from the semiconductor device A**10** of the above embodiment in the arrangement of the plurality of first electrodes **31**. Accordingly, the configuration of the first extending portion **113** differs from the above embodiment. In the semiconductor device A**11**, the first electrodes **31** are arranged along the first direction x as with the above embodiment. On the other hand, in this variation, all of the first electrodes **31** overlap with the first portion **111** as viewed in the thickness direction z. Hence, none of the first electrodes **31** overlaps with the first extending portion **113** (second portion **112**) as viewed in the thickness direction z. As a result, the first extending portion **113** (second portion **112**) does not include the first region **112**A. Also, the first extending portion **113** does not have distinction between the first inner portion **113**A and the first outer portion **113**B as in the above

embodiment.
[0075] As shown in FIGS. **19** and **20**, a dimension L**3**, which is the length of the first extending portion **113** along the second direction y, is larger than the dimension L**2**, which is the length of the first terminal portion **21** along the second direction y. The dimension L**3** is two to three times the second dimension L**2**, for example.
[0076] In the first wiring portion **11** of the first conductive member **1**A, the necessary portion of the path for electrical current between the semiconductor element **3** and the first terminal portion **21** is the first portion **111** overlapping with the first terminal portion **21** as viewed in the thickness direction z. In FIG. **19**, the entirety of the first wiring portion **11** is shown with hatching that diagonally falling to the right. Also, the necessary portion of the path for electrical current (first portion **111**) of the first wiring portion **11** is shown with hatching that diagonally rising to the right.
[0077] As viewed in the thickness direction z, the ratio of the second area S**2** (area of the first portion **111**), which is the area of the necessary portion of the path for electrical current (the first portion **111**), relative to the first area S**1**, which is the area of the entirety of the first wiring portion **11** is 60% or less, for example. The ratio of the second area S**2** to the first area S**1** is preferably 20% to 50%. In this variation shown in FIG. **19**, the ratio of the second area S**2** to the first area S**1** is 34.6%.
[0078] In the present variation, the unnecessary portion of the path for electrical current between the semiconductor element **3** and the first terminal portion **21** is other than the necessary portion (first portion **111**) in the first wiring portion **11**. Specifically, the unnecessary portion is the second portion **112** (first extending portion **113** and second extending portion **114**). The ratio of the area of the unnecessary portion of the path for electrical path in the first wiring portion **11** is 40% or more, and preferably 50% to 80%.
[0079] In the present variation of the semiconductor device A**11**, the first wiring portion **11** of the first conductive member **1**A includes the first portion **111** overlapping with the first terminal portion **21** as viewed in the thickness direction z, and the second portion **112** not overlapping with the first terminal portion **21** as viewed in the thickness direction z. The ratio of the second area S**2** (area of the first portion **111**), which is the area of the necessary portion of the path for electrical current, relative to the first area S**1**, which is the area of the first wiring portion **11**, is 60% or less, as viewed in the thickness direction z. Such a configuration results in that the ratio of the unnecessary portion of the path for electrical current is 40% or more in the first wiring portion **11**. The increased unnecessary portion of the path for electrical current in the first wiring portion **11** in this manner improves the electrical characteristics of the semiconductor device A**11** such as reducing the impedance between the semiconductor element **3** and the first terminal portion **21**.
[0080] The ratio of the area of the necessary portion of the path for electrical current (second area S**2**) to the area of the first wiring portion **11** (first area S**1**) is 20% to 50%. In this manner, the ratio of the area of the unnecessary portion of the path for electrical current is 50% to 80% in the first wiring portion **11**. Such a configuration reduces the excessively large ratio of the unnecessary portion in the first wiring portion **11**, which is desirable for downsizing the semiconductor device A**11**.
[0081] The dimension L**3**, which is the length of the first extending portion **113** along the second direction y, is larger than the second dimension L**2**, which is the length of the first terminal portion **21** along the second direction y. Such a configuration may effectively reduce the ratio of the area of the necessary portion of the path for electrical current (second area S**2**) to the area of the first wiring portion **11** (first area S**1**). In other words, the ratio of the area of the unnecessary portion of the path for electrical current in the first wiring portion **11** may be efficiently increased. Therefore, the semiconductor device A**11** has the structure suitable for improving its electrical characteristics.
[0082] The dimension L**3**, which is the length of the first extending portion **113** along the second direction y, is two to three the second dimension L**2**, which is the length of the first terminal portion **21** along the second direction y. The increased length of the first extending portion **113** in the

second direction y (dimension L**3**) in this manner improves the effect of preventing the sealing resin **4** from peeling off from the first conductive member **1**A, as well as improving the electrical characteristics of the semiconductor device A**11** described above.

Second Variation of the First Embodiment

[0083] FIGS. **21** to **25** show a semiconductor device A**12** according to a second variant of the first embodiment. FIG. **21** is a plan view similar to FIG. **3**, showing the semiconductor device A**12**. In FIG. **21**, the semiconductor element **3** and the sealing resin **4** are omitted, for the sake of understanding. In the same figures, the omitted semiconductor element **3** and sealing resin **4** are shown as imaginary lines (two dotted lines), respectively. FIG. **22** is a cross-sectional view taken along a line XXII-XXII in FIG. **21**. FIG. **23** is a cross-sectional view taken along a line XXIII-XXIII in FIG. **21**. FIG. **24** is a partially enlarged view of FIG. **21**. FIG. **25** is a partially enlarged view of FIG. **22**.

[0084] The semiconductor device A**12** of the present variation differs from the semiconductor device A**10** of the above embodiment in the arrangement of the plurality of first electrodes **31**. In the semiconductor device A**12**, the first electrodes **31** are arranged along the first direction x as with the above embodiment. On the other hand, in the present variation, all of the first electrodes **31** overlap with the first extending portion **113** (second portion **112**) as viewed in the thickness direction Z. In addition, in the present variation, the number of first electrodes **31** arranged along the first direction x is less than that in the semiconductor device A**10**, so that the spacing between adjacent first electrodes **31** in the first direction x is larger than that in the semiconductor device A**10**.

[0085] In the present variation, as with the semiconductor device A**10**, the first region **112**A is the trapezoidal region in the first extending portion **113** (second portion **112**) as viewed in the thickness direction z that overlaps with the first electrodes **31** and is connected to the first portion **111**. The first region **112**A is sum of the region with the first direction x as the longitudinal direction in which the first electrodes **31** are arranged and the region between each end of the region with the first direction x as the longitudinal direction and the most distant position from the boundary of the first extending portion **113** (second portion **112**) and the first portion **111**.

[0086] In the present variation, the first extending portion **113** includes a first inner portion **113**A and a first outer portion **113**B, as with the semiconductor device A**10**. The first inner portion **113**A is connected to the first portion **111** and forms the first region **112**A. The first outer portion **113**B is connected to the first inner portion **113**A and is offset in the y**1** side of the second direction y with respect to the first inner portion **113**A.

[0087] As shown in FIGS. **24** and **25**, the first dimension L**1**, which is the length of the first outer portion **113**B along the second direction y, is larger than the second dimension L**2**, which is the length of the first terminal portion **21** along the second direction y. The first dimension L**1** is 1.5 to 2.5 times the second dimension L**2**, for example.

[0088] The necessary portion of the path for electrical current between the semiconductor element **3** and the first terminal portion **21** in the first wiring portion **11** of the first conductive member **1**A is the first portion **111** and the first region **112**A overlapping with the first terminal portion **21** as viewed in the thickness direction z. In FIG. **24**, the entirety of the first wiring portion **11** is shown with hatching that diagonally falling to the right. In addition, the necessary portion of the path for electrical current in the first wiring portion **11** (first portion **111** and first region **112**A) are shown with hatching that diagonally rising to the right. In the example shown in FIG. **24**, as viewed in the thickness direction z, the edge of the first region **112**A on the y**1** side of the second direction y corresponds to line segments extending in the first direction x tangential to the ends at the y**1** side of the second direction y of the first electrodes **31**, which are arranged in the first direction x.

[0089] As viewed in the thickness direction z, the ratio of the second area S**2** (sum of the area of the first portion **111** and the first region **112**A), which is the area of the necessary portion of the path for electrical current (the first portion **111** and the first region **112**A), relative to the first area

S**1**, which is the area of the entirety of the first wiring portion **11** is 60% or less, for example. The ratio of the second area S**2** to the first area S**1** is preferably 20% to 50%.
[0090] In this variation shown in FIG. **24**, the ratio of the second area S**2** to the first area S**1** is 49.6%.
[0091] In the present variation, the unnecessary portion of the path for electrical current between the semiconductor element **3** and the first terminal portion **21** is other than the necessary portion (first portion **111** and the first region **112**A) in the first wiring portion **11**. Specifically, the unnecessary portion is the portion other than the first region **112**A (mainly the first inner portion **113**A) in the first extending portion **113** (mainly the first outer portion **113**B) and the second extending portion **114**. The ratio of the area of the unnecessary portion of the path for electrical path in the first wiring portion **11** is 40% or more, and preferably 50% to 80%.
[0092] In the present variation of the semiconductor device A**12**, the first wiring portion **11** of the first conductive member **1**A includes the first portion **111** overlapping with the first terminal portion **21** as viewed in the thickness direction z, and the second portion **112** not overlapping with the first terminal portion **21** as viewed in the thickness direction z.
[0093] As viewed in the thickness direction z, the ratio of the second area S**2** (sum of the area of the first portion **111** and the first region **112**A), which is the area of the necessary portion of the path for electrical current, relative to the first area S**1**, which is the area of the entirety of the first wiring portion **11** is 60% or less. Such a configuration results in that the ratio of the unnecessary portion of the path for electrical current is 40% or more in the first wiring portion **11**. The increased unnecessary portion of the path for electrical current in the first wiring portion **11** in this manner improves the electrical characteristics of the semiconductor device A**12** such as reducing the impedance between the semiconductor element **3** and the first terminal portion **21**.
[0094] The ratio of the area of the necessary portion of the path for electrical current (second area S**2**) to the area of the first wiring portion **11** (first area S**1**) is 20% to 50%. In this manner, the ratio of the area of the unnecessary portion of the path for electrical current is 50% to 80% in the first wiring portion **11**. Such a configuration reduces the excessively large ratio of the unnecessary portion in the first wiring portion **11**, which is desirable for downsizing the semiconductor device A**12**. Otherwise, the semiconductor device A**12** has the same effects as the semiconductor device A**10** of the above embodiment.
[0095] The semiconductor devices according to the present disclosure are not limited to the embodiments described above. The specific configuration of each part of a semiconductor device according to the present disclosure may suitably be designed and changed in various manners.
[0096] In the above embodiment, the case is described in which the first conductive member **1**A, the second conductive member **1**B, the pair of third conductive members **1**C, and the pluralities of conductive members **1**D, **1**E, **1**F are each formed from a lead, but the present disclosure is not limited thereto. The first conductive member **1**A, the second conductive member **1**B, the pair of third conductive members **1**C, and the pluralities of conductive members **1**D, **1**E, **1**F may be configured, for example, by metal plating in a desired shape.
[0097] The present disclosure includes the embodiments described in the following clauses.
Clause 1
[0098] A semiconductor device comprising:
[0099] a first conductive member including: [0100] a first wiring portion with a first obverse face facing one side of a thickness direction, and [0101] a first terminal portion connected to the first wiring portion and including a first reverse face facing another side of the thickness direction;
[0102] a semiconductor element located in a side facing the first obverse face in the thickness direction and including at least one electrode electrically connected to the first obverse face; and
[0103] a sealing resin covering a part of the first wiring portion, a part of the first terminal portion, and the semiconductor element, and including a resin reverse face facing another side of the thickness direction,

[0104] wherein the first reverse face is exposed from the resin reverse face,
[0105] the first wiring portion includes a first portion overlapping with the first terminal portion as viewed in the thickness direction and a second portion not overlapping with the first terminal portion as viewed in the thickness direction,
[0106] the second portion includes a first intermediate face located between the first obverse face and the first reverse face in the thickness direction and facing another side of the thickness direction,
[0107] the first intermediate face is covered by the sealing resin,
[0108] the first wiring portion includes a first area as viewed in the thickness direction,
[0109] the second portion includes a first region between a part overlapping with the at least one electrode and a part connected to the first portion as viewed in the thickness direction,
[0110] the first portion and the first region constitute a second area, and
[0111] the ratio of the second area to the first area is 60% or less.

Clause 2

[0112] The semiconductor device according to clause 1, wherein the ratio of the second area to the first area is 20% to 50%.

Clause 3

[0113] The semiconductor device according to clause 1 or 2, wherein the first portion and the first terminal portion extend in a first direction orthogonal to the thickness direction.

Clause 4

[0114] The semiconductor device according to clause 3, wherein the at least one electrode comprises a plurality of electrodes that are arranged along the first direction.

Clause 5

[0115] The semiconductor device according to clause 4, wherein at least a part of each of the plurality of electrodes overlaps with the first portion as viewed in the thickness direction.

Clause 6

[0116] The semiconductor device according to clause 4 or 5, wherein the second portion includes a first extending portion extending from the first portion to one side of a second direction orthogonal to the thickness direction and the first direction.

Clause 7

[0117] The semiconductor device according to clause 6, wherein at least one of the plurality of the electrodes overlaps with the first portion and the first extending portion as viewed in the thickness direction.

Clause 8

[0118] The semiconductor device according to clause 6 or 7, wherein the first extending portion includes a first inner portion connected to the first portion and constituting at least a part of the first region, and a first outer portion connected to the first inner portion and offset in one side of the second direction with respect to the first inner portion, [0119] a first dimension, which is a length of the first outer portion along the second direction, is larger than a second dimension, which is a length of the first terminal portion along the second direction.

Clause 9

[0120] The semiconductor device according to clause 8, wherein the first dimension is 1.5 to 2.5 times the second dimension.

Clause 10

[0121] The semiconductor device according to any one of clauses 6 to 9, wherein the second portion includes a second extending portion extending from the first portion to another side of the second direction.

Clause 11

[0122] The semiconductor device according to clause 10, further comprising a second conductive member including a second wiring portion with a second obverse face facing the one side of the

thickness direction, and a second terminal portion with a second reverse face connected to the second wiring portion on another side of the thickness direction and facing another side of the thickness direction,

[0123] wherein the second conductive member is disposed in another side of the second direction with respect to the first conductive member.

Clause 12

[0124] The semiconductor device according to clause 11, wherein the second wiring portion includes a protruding portion protruding to the one side of the second direction,

[0125] the second extending portion overlaps with the entirety of the protruding portion as viewed in the second direction and includes a recess recessed into the one side of the second direction.

Clause 13

[0126] The semiconductor device according to any one of clauses 1 to 12, wherein the first conductive member contains copper. Clause 14.

[0127] The semiconductor device according to clause 13, wherein the first conductive member is formed from a lead.

REFERENCE NUMERALS

[0128] A**10**, A**11**, A**12**: Semiconductor device [0129] **1**A: First conductive member [0130] **1**B: Second conductive member [0131] **1**C: Third conductive member [0132] **1**D, **1**E, **1**F: Conductive member [0133] **11**: First wiring portion **11***a*: First obverse face [0134] **11***b*: First intermediate face **111**: First portion [0135] **112**: Second portion **112**A: First region [0136] **113**: First extending portion **113**A: First inner portion [0137] **113**B: First outer portion **114**: Second extending portion [0138] **114***a*: Recess [0139] **12**: Second wiring portion [0140] **12**b: Second intermediate face **12***a*: Second obverse face [0141] **13**: Third wiring portion **121**: Protruding portion [0142] **13**a: Third obverse face **13***b*: Third intermediate face [0143] **14**, **15**, **16**: Wiring portion **14***a*, **15***a*, **16***a*: Obverse face [0144] **21**: First terminal portion **15***b*, **16***b*: Intermediate face [0145] **21**a: First reverse face **22**: Second terminal portion [0146] **23**: Third terminal portion **22***a*: Second reverse face [0147] **23**a: Third reverse face **24**, **25**, **26**: Terminal portion [0148] **24***a*, **25***a*, **26**a: Reverse face [0149] **21***b*, **22***b*, **23***b*, **23***c*, **24***b*, **24***c*, **25***b*, **26***b*: End face [0150] **3**: Semiconductor element **30**: Element body [0151] **31**: First electrode **32**, **33**: Electrode [0152] **39**: Bonding layer **4**: Sealing resin [0153] **41**: Resin obverse face **42**: Resin reverse face [0154] **431**: First resin side face **432**: Second resin side face [0155] **433**: Third resin side face **434**: Fourth resin side face [0156] L**1**: First dimension L**2**: Second dimension [0157] L**3**: Dimension S**1**: First area S**2**: Second area [0158] x: First direction y: Second direction [0159] z: Thickness direction

## Claims

**1**. A semiconductor device comprising: a first conductive member including: a first wiring portion with a first obverse face facing one side of a thickness direction, and a first terminal portion connected to the first wiring portion and including a first reverse face facing another side of the thickness direction; a semiconductor element located in a side facing the first obverse face in the thickness direction and including at least one electrode electrically connected to the first obverse face; and a sealing resin covering a part of the first wiring portion, a part of the first terminal portion, and the semiconductor element, and including a resin reverse face facing another side of the thickness direction, wherein the first reverse face is exposed from the resin reverse face, the first wiring portion includes a first portion overlapping with the first terminal portion as viewed in the thickness direction and a second portion not overlapping with the first terminal portion as viewed in the thickness direction, the second portion includes a first intermediate face located between the first obverse face and the first reverse face in the thickness direction and facing another side of the thickness direction, the first intermediate face is covered by the sealing resin, the first wiring portion includes a first area as viewed in the thickness direction, the second portion

includes a first region between a part overlapping with the at least one electrode and a part connected to the first portion as viewed in the thickness direction, the first portion and the first region constitute second area, and the ratio of the second area to the first area is 60% or less.

**2**. The semiconductor device according to claim 1, wherein the ratio of the second area to the first area is 20% to 50%.

**3**. The semiconductor device according to claim 1, wherein the first portion and the first terminal portion extend in a first direction orthogonal to the thickness direction.

**4**. The semiconductor device according to claim 3, wherein the at least one electrode comprises a plurality of electrodes that are arranged along the first direction.

**5**. The semiconductor device according to claim 4, wherein at least a part of each of the plurality of electrodes overlaps with the first portion as viewed in the thickness direction.

**6**. The semiconductor device according to claim 4, wherein the second portion includes a first extending portion extending from the first portion to one side of a second direction orthogonal to the thickness direction and the first direction.

**7**. The semiconductor device according to claim 6, wherein at least one of the plurality of the electrodes overlaps with the first portion and the first extending portion as viewed in the thickness direction.

**8**. The semiconductor device according to claim 7, wherein the first extending portion includes a first inner portion connected to the first portion and constituting at least a part of the first region, and a first outer portion connected to the first inner portion and offset in one side of the second direction with respect to the first inner portion, a first dimension, which is a length of the first outer portion along the second direction, is larger than a second dimension, which is a length of the first terminal portion along the second direction.

**9**. The semiconductor device according to claim 8, wherein the first dimension is 1.5 to 2.5 times the second dimension.

**10**. The semiconductor device according to claim 6, wherein the second portion includes a second extending portion extending from the first portion to another side of the second direction.

**11**. The semiconductor device according to claim 10, further comprising a second conductive member including a second wiring portion with a second obverse face facing the one side of the thickness direction, and a second terminal portion with a second reverse face connected to the second wiring portion on another side of the thickness direction and facing another side of the thickness direction, wherein the second conductive member is disposed in another side of the second direction with respect to the first conductive member.

**12**. The semiconductor device according to claim 11, wherein the second wiring portion includes a protruding portion protruding to the one side of the second direction, the second extending portion overlaps with the entirety of the protruding portion as viewed in the second direction and includes a recess recessed into the one side of the second direction.

**13**. The semiconductor device according to claim 1, wherein the first conductive member contains copper.

**14**. The semiconductor device according to claim 13, wherein the first conductive member is formed from a lead.