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(54) **AGING RESILIENT LEVEL SHIFTER**

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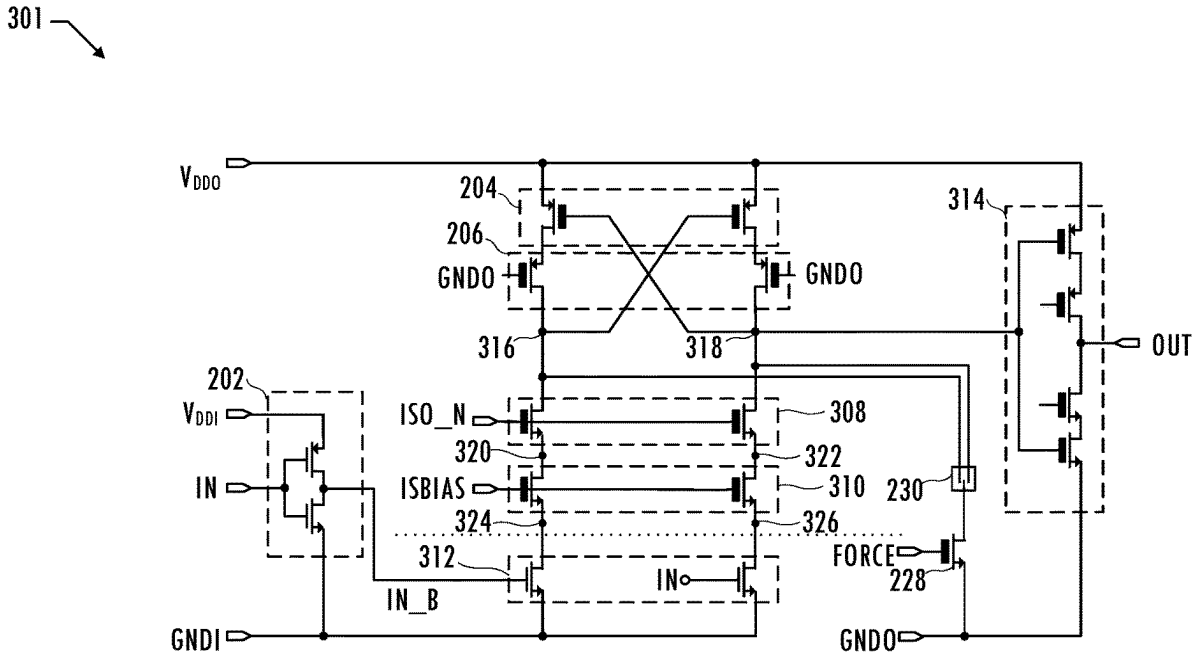
(57) **ABSTRACT**

An aging resilient level shifter has an increased lifetime as compared to a conventional level shifter. In at least one embodiment, a method for level-shifting a received signal from a first voltage domain to a second voltage domain includes controlling a cross-coupled pair of transistors according to an input signal and a complementary input signal to generate a signal on a pair of complementary nodes. The cross-coupled pair of transistors has a first doping type and the controlling uses a pair of transistors having a second doping type. The second doping type is complementary to the first doping type. The method includes isolating the pair of transistors from the pair of complementary nodes using a pair of isolation transistors and a pair of cascode transistors. The pair of cascode transistors is coupled between the pair of transistors and the pair of complementary nodes.



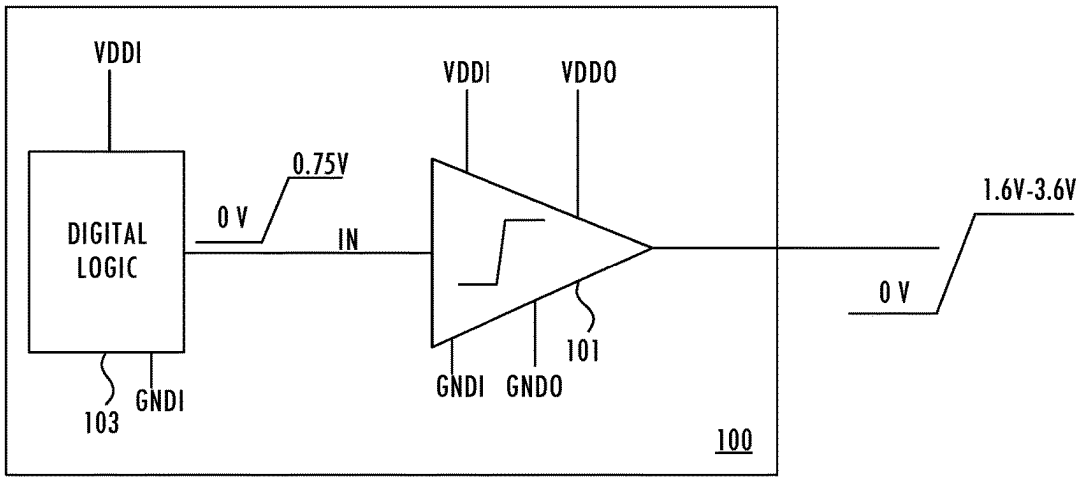

VDDI
DIGITAL LOGIC
0.75V
0 V
IN
VDDI
VDDO
101
GNDI
GNDO
103
GNDI
100
1.6V-3.6V
0 V

FIG. 1

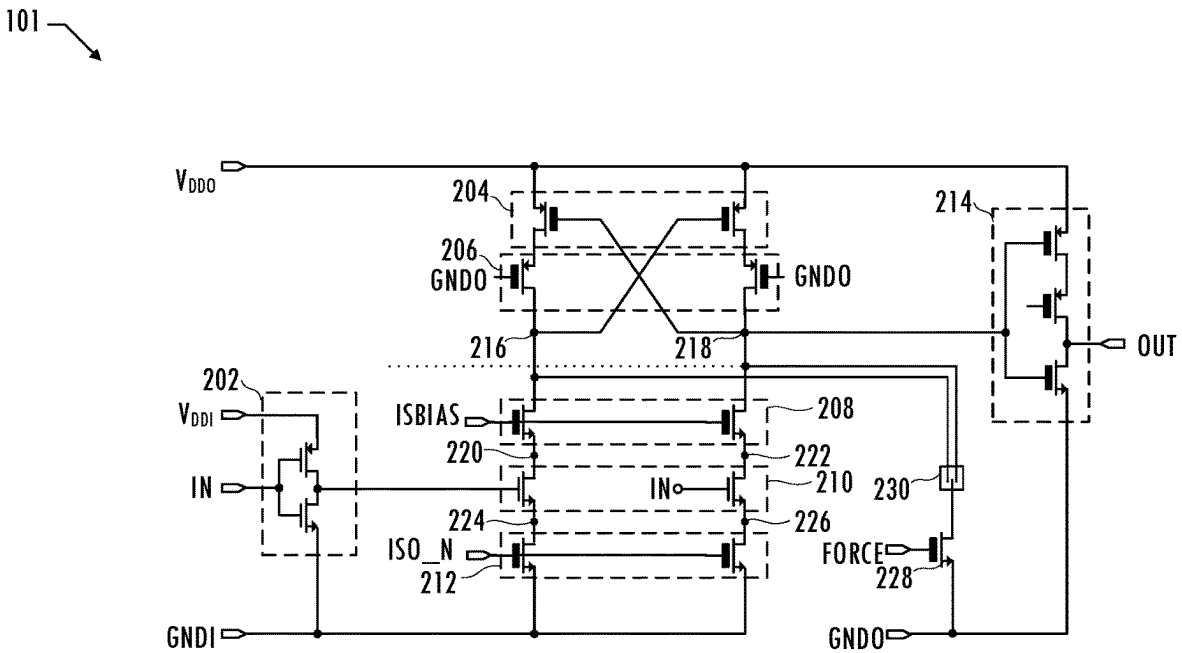

101
VDDO
204
206
GNDO
GNDO
214
216
218
OUT
202
VDDI
IN
ISBIAS
208
220
222
IN
210
230
224
226
ISO_N
212
FORCE
228
GNDI
GNDO

FIG. 2

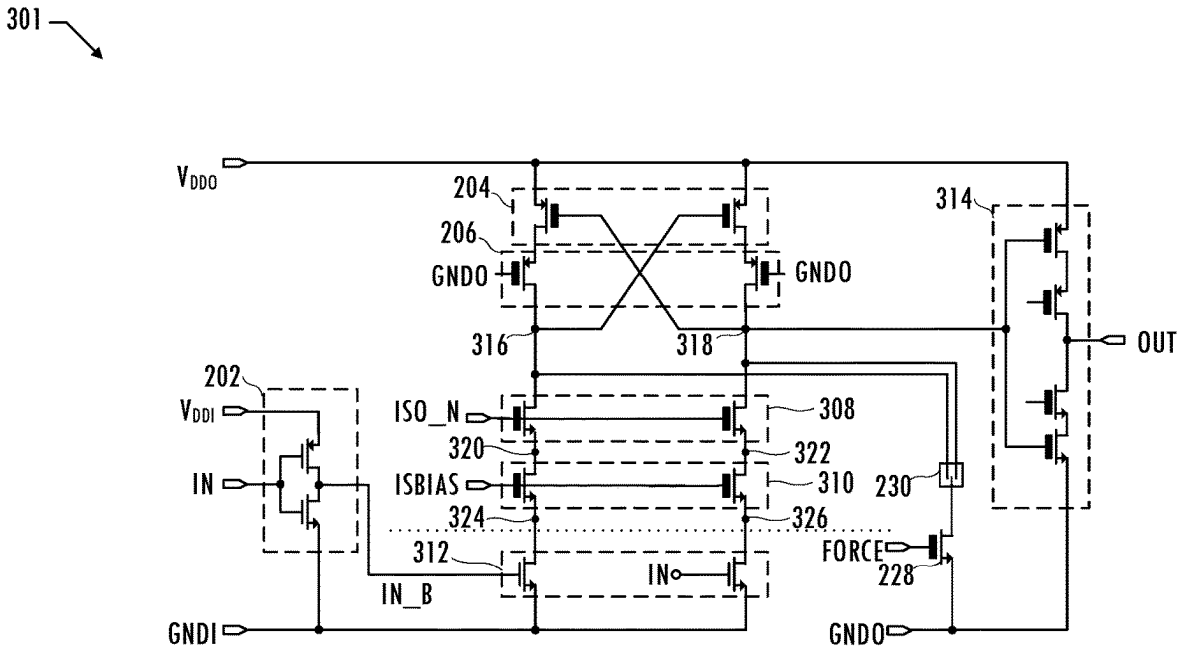

301
V_{DDO}
204
206
GNDO
GNDO
314
316
318
OUT
202
V_{DDI}
ISO_N
308
320
322
IN
ISBIAS
310
230
324
326
312
IN
FORCE
228
IN_B
GNDI
GNDO

FIG. 3

AGING RESILIENT LEVEL SHIFTER

BACKGROUND

Field of the Invention

[0001] The invention relates to integrated circuits and more particularly to circuits for converting signals from one voltage domain to another voltage domain.

Description of the Related Art

[0002] In general, a level shifter is a circuit that translates signals from one voltage domain to another voltage domain to provide interoperability between integrated circuits having different voltage requirements. For example, a conventional level shifter converts signals generating in a low power domain (e.g., a processor operating with a power supply voltage of 1 V) to signals for use by circuits in a high power domain (e.g., analog input/output circuits operating at 3.6 V). Reuse of level shifter circuits originally designed for a target manufacturing process (e.g., a 40 nm process) in a later-developed manufacturing process (e.g., 22 nm process) may have acceptable performance over some operating conditions. However, hot carrier injection degrades the performance of a conventional level shifter circuit under extreme operating conditions, e.g., high supply voltage (e.g., 3.8 V), low temperature (e.g., −40 C.), and high signaling frequency (greater than 1 MHz). Simulations indicate that such degradation causes performance of the level shifting circuit to fall out of a target range in less than one year. Accordingly, improved techniques for level shifting are desired.

SUMMARY OF EMBODIMENTS OF THE INVENTION

[0003] In at least one embodiment, a method for level-shifting a received signal from a first voltage domain to a second voltage domain includes controlling a cross-coupled pair of transistors according to an input signal and a complementary input signal to generate a signal on a pair of complementary nodes. The cross-coupled pair of transistors has a first doping type and the controlling uses a pair of transistors having a second doping type. The second doping type is complementary to the first doping type. The method includes isolating the pair of transistors from the pair of complementary nodes using a pair of isolation transistors and a pair of cascode transistors. The pair of cascode transistors is coupled between the pair of transistors and the pair of complementary nodes. In an embodiment, the pair of transistors comprise low-voltage transistors and the and the cross-coupled pair of transistors, the pair of isolation transistors, and the pair of cascode transistors comprise high-voltage transistors. In an embodiment, the pair of transistors are in the first voltage domain and the cross-coupled pair of transistors, the pair of cascode transistors, and the pair of isolation transistors are in the second voltage domain. In an embodiment, the first voltage domain has an input power supply voltage level above an input ground and the second voltage domain has an output power supply voltage level above an output ground. In an embodiment, the output power supply voltage level is greater than the input power supply voltage level.

[0004] In at least one embodiment, a level shifter includes a cross-coupled pair of transistors coupled between a first power supply node and a first pair of nodes. The cross-coupled pair of transistors has a first doping type. The level shifter includes a pair of isolation transistors coupled between the first pair of nodes and a second pair of nodes. The pair of isolation transistors has a second doping type. The second doping type is complementary to the first doping type. The level shifter includes a pair of cascode transistors coupled between the second pair of nodes and a third pair of nodes. The pair of cascode transistors has the second doping type. The level shifter includes a pair of transistors coupled between the third pair of nodes and a second power supply node. The pair of transistors has the second doping type. The pair of transistors is configured to receive an input signal and a complementary input signal. In an embodiment, the level shifter includes an input circuit coupled between the second power supply node and a third power supply node and is configured to generate the complementary input signal based on the input signal. In an embodiment, the level shifter includes an output circuit coupled between the first power supply node and a fourth power supply node and is configured to generate an output signal on an output node based on a signal on the first pair of nodes. In an embodiment, the first power supply node is configured to receive an output power supply voltage level above an output ground and the third power supply node is configured to receive an input power supply voltage level above an input ground. The output power supply voltage level is greater than the input power supply voltage level. The second power supply node is coupled to an input ground. In an embodiment, the pair of transistors comprise low-voltage transistors and the cross-coupled pair of transistors, the pair of isolation transistors, and the pair of cascode transistors comprise high-voltage transistors.

[0005] In at least one embodiment, a level shifter includes a first circuit having low-voltage transistors coupled between a pair of complementary nodes and a first ground. The first circuit is responsive to an input signal and a complementary input signal generated in a first voltage domain. The level shifter includes a second circuit comprising high-voltage transistors coupled between the pair of complementary nodes and an output power supply node and configured to generate complementary signals on the pair of complementary nodes in a second voltage domain. In an embodiment, the level shifter includes an input buffer circuit comprising second low-voltage transistors coupled between an input power supply node and an input ground and configured to generate the complementary input signal based on the input signal generated in the first voltage domain. In an embodiment, the level shifter includes an output circuit comprising second high-voltage transistors coupled between the output power supply node and an output ground and responsive to a signal on a node of the pair of complementary nodes to generate an output signal in the second voltage domain.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

[0007] FIG. **1** illustrates a circuit diagram of an integrated circuit system including a level shifter circuit.

[0008] FIG. **2** illustrates a circuit diagram of a conventional level shifter of an integrated circuit.

[0009] FIG. **3** illustrates a circuit diagram of an exemplary aging resilient level shifter of an integrated circuit consistent with at least one embodiment of the invention.

[0010] The use of the same reference symbols in different drawings indicates similar or identical items.

DETAILED DESCRIPTION

[0011] An aging resilient level shifter having improved aging performance includes high-voltage isolation transistors in a cascode configuration with high-voltage cascode transistors, which are in a cascode configuration with low-voltage input transistors, thereby reducing stress on the high-voltage cascode transistors coupled to the low-voltage input transistors. The aging resilient level shifter has an increased lifetime as compared to a conventional level shifter. An aging simulation indicates that the cascode transistors of the aging resilient level shifter have a negligent threshold voltage shift (e.g., a threshold voltage shift of less than 15 mV) as compared to a threshold voltage shift of over 500 mV of the cascode transistors in the conventional level shifter.

[0012] Referring to FIG. **1**, a conventional level shifter shifts signal voltages from a low voltage domain to signal voltages in a high voltage domain. For example, digital logic **103** operates in a first voltage domain, which includes input power supply node VDDI and input ground GNDI with signal swings between 0 V and an input power supply voltage level in the range of 0.75 V to 0.90 V. Level shifter **101** receives digital signal IN from digital logic **103** in the low voltage domain and shifts the signal level to generate signal OUT a second voltage domain, e.g., a high voltage domain for an interface to analog circuits (e.g., circuits for communicating externally from integrated circuit **100**). In an embodiment, the second voltage domain includes output power supply node VDDO and output ground GNDO with signal swings between 0 V and an output power supply voltage level in the range of 1.6 V to 3.6 V.

[0013] FIG. **2** illustrates a circuit diagram of a conventional low-to-high level shifter including input buffer **202**, cross-coupled transistors **204**, and output buffer **214**. Input buffer **202** includes low-voltage transistors and output buffer **214** includes high-voltage transistors. An exemplary integrated circuit manufacturing process provides transistors having different breakdown voltages and speeds of operation as a result of gate terminals formed using oxide layers of different thicknesses. An exemplary high-voltage transistor has a thicker gate oxide and therefore has a higher breakdown voltage but is slower than a low-voltage transistor that has a thinner gate oxide thickness. High-voltage transistors are indicated in the figures by transistors having filled, rectangular gate terminals.

[0014] Cross-coupled transistors **204** are high-voltage p-channel metal oxide semiconductor field effect transistors (MOSFETs) (i.e., high-voltage PMOS transistors) having source terminals coupled to output power supply node VDDO and drain terminals coupled to corresponding PMOS transistors of cascode transistors **206**, which are also high-voltage PMOS transistors and have gate terminals coupled to output ground GNDO (i.e., cascode transistors **206** are on). In general, cascode configuration refers to a series coupling of a common-source transistor (e.g., transistors **204**), which has high impedance node, to a common gate transistor, i.e., a cascode transistor (e.g., cascode transistors **206**), to increase output impedance. Since there is no direct coupling from output to input, a cascode configuration improves input-to-output isolation, reduces the Miller effect, and increases bandwidth of the common source configuration.

[0015] Nodes **216** and **218**, which are coupled to respective gate terminals of cross-coupled transistors **204** and respective drain terminals of cascode transistors **206**, are also coupled to respective drain terminals of cascode transistors **208**, which are high-voltage n-channel MOSFETs (i.e., high-voltage NMOS transistors) and have gate terminals coupled to bias signal ISBIAS. In at least one embodiment, bias signal ISBIAS has a voltage level in the range of 1.25 V to 1.45 V when the temperature is greater than 25 C. and has a voltage level in the range of 1.35 V to 1.55 V when the temperature is less than 25 C. Corresponding source terminals of cascode transistors **208** are coupled to nodes **220** and **222** and drain terminals of pulldown transistors **210**, which are low-voltage NMOS transistors. Corresponding source terminals of pulldown transistors **210** are coupled to nodes **224** and **226** and corresponding drain terminals of isolation transistors **212**, which are high-voltage NMOS transistors that are controlled by control signal ISO_N and have source terminals coupled to input ground GNDI. In at least one embodiment, control signal ISO_N is generated by a buffer, which is powered by the same power supply as output power supply node VDDO. When control signal ISO_N='1', then it will equal VDDO.

[0016] In at least one embodiment of level shifter **101**, the low voltage domain may be disabled, but the high voltage domain is enabled. Isolation transistors **212** isolate the input from the output when the input is undefined (e.g., when the low voltage domain is disabled and control signal ISO_N='0'). When the cross-coupled branches float (i.e., are undefined) isolation transistors **212** are off and control signal FORCE is configured to enable transistor **228** to force node **216** and node **218** to predetermined states (i.e., '1' and '0,' respectively, or '0' and '1,' respectively) via switch **230** according to a predetermined value of a read-only memory, fuse, or other selection technique. In general, isolation transistors **212** are positioned to be directly connected to a power supply node (e.g., at the bottom of the cross-coupled branches) to reduce the likelihood of impedance changes from affecting the rest of level shifter **101** and influencing performance. In another embodiment, switch **230** is omitted, transistor **228** of level shifter **101** is coupled to node **216**, and control signal FORCE is configured to enable transistor **228** to force node **216** and node **218** to '0' and '1,' respectively. In yet another embodiment, switch **230** is omitted, transistor **228** of level shifter **101** is coupled to node **218**, and control signal FORCE is configured to enable transistor **228** to force node **216** and node **218** to '1' and '0,' respectively.

[0017] Changing the state of cross-coupled transistors **204** requires a strong low-voltage transistor. When level shifter **101** is simulated under extreme operating conditions, e.g., VDDO=3.8 V, temperature of −40 C., and input signal IN toggling at a frequency of higher than 1 MHz, cascode transistors **208** suffer significant deterioration due to the hot carrier injection aging effect and level shifter **101** malfunctions before one year of operation. The increase in threshold voltage of cascode transistors **208** reduces the headroom of pulldown transistors **210**, making pulldown transistors **210** too weak to toggle cross-coupled transistors **204**. Thus, cascode transistors **208** are considered past their useful lifetime. An aging simulation of level shifter **101** predicts a

threshold voltage shift of greater than 500 mV in cascode transistors **208** after ten years.

[0018] An instantiation of level shifter **101** is typically used for each control signal that is provided to analog circuitry in an integrated circuit device. If aging causes those level shifters to fail, then the integrated circuit device is no longer functional. A technique for reducing effects of aging on a level shifter includes reducing stress on cascode transistors **208** coupled to bias signal ISBIAS while maintaining suitable voltage headroom for pulldown transistors **210**.

[0019] Referring to FIG. **3**, in at least one embodiment, aging resilient level shifter **301** includes input buffer **202**, cross-coupled transistors **204**, and output buffer **314**. Input buffer **202** includes low-voltage transistors and output buffer **314** includes high-voltage transistors. Cross-coupled transistors **204** are high-voltage PMOS transistors having source terminals coupled to output power supply node VDDO and having drain terminals coupled to corresponding PMOS transistors of cascode transistors **206**, which are also high-voltage PMOS transistors and have gate terminals coupled to output ground GNDO. Nodes **316** and **318**, which are coupled to respective gate terminals of cross coupled transistors **204** and respective drain terminals of cascode transistors **206**, are also coupled to respective drain terminals of isolation transistors **308**, which are high-voltage NMOS transistors, have gate terminals controlled by control signal ISO_N, and have corresponding source terminals coupled to cascode transistors **310**, which are controlled by bias signal ISBIAS. In at least one embodiment, bias signal ISBIAS has a voltage level in the range of 1.25 V to 1.45 V when the temperature is greater than 25 C. and has a voltage level in the range of 1.35 V to 1.55 V when the temperature is less than 25 C. Corresponding source terminals of cascode transistors **310** are coupled to nodes **324** and **326** and respective drain terminals of pulldown transistors **312**, which are low-voltage NMOS transistors. Source terminals of pulldown transistors **312** are coupled to input ground GNDI.

[0020] In at least one embodiment of level shifter **301**, the low voltage domain may be disabled, but the high voltage domain is enabled. Isolation transistors **308** isolate the input from the output when the input is undefined (e.g., when the low voltage domain is disabled and control signal ISO_N='0'). When the cross-coupled branches float (i.e., are undefined) isolation transistors **308** are off and control signal FORCE is configured to enable transistor **228** to force node **316** and node **318** to predetermined states (i.e., '1' and '0,' respectively, or '0' and '1,' respectively) via switch **230** according to a predetermined value of a read-only memory, fuse, or other selection technique. Isolation transistors **308** are not directly connected to a power supply node, which generally increases the likelihood that impedance changes caused by the bulk effect of isolation transistors **308** affects the rest of the level shifter circuit and under some circumstances may degrade performance. However, when control signal ISO_N='1,' ISO_N will equal the voltage on output power supply node VDDO, which is greater than the shifted threshold voltage and isolation transistors **308** will be fully turned on. Isolation transistors **308** are in a cascode configuration with cascode transistors **310** thereby reducing the stress on cascode transistors **310** (e.g., limits the gate-to-source voltage of cascode transistors **310** to a voltage level no greater than 0.7 V). Although isolation transistors **308** are exposed to aging, when control signal ISO_N='1', stress from hot carrier injection is worse for large drain-to-source voltages, in general. Although isolation transistors **308** may have 3.8V at the drain terminal, their source terminals are limited by ISO_N-VGs_**308**. Since a buffer that is powered by the voltage on output power supply node VDDO (e.g., VDDO=3.8V) generates control signal ISO_N, their source voltage will be one threshold voltage lower than the voltage on the gate terminal. Hence, the drain-to-source voltages of isolation transistors **308** are limited to 0.8-0.9 V. Accordingly, isolation transistors **308** do not experience substantial stress from hot carrier injection. Simulation of level shifter **301** operating under extreme conditions (e.g., VDDO=3.8 V, temperature of −40 C., and input signal IN toggling at a frequency of higher than 1 MHz), cascode transistors **310** have a threshold voltage shift of less than 15 mV after ten years and have a predicted lifetime of greater than 100 years.

[0021] Thus, aging resilient level shifting techniques have been described. The description of the invention set forth herein is illustrative and is not intended to limit the scope of the invention as set forth in the following claims. The terms "first," "second," "third," and so forth, as used in the claims, unless otherwise clear by context, are to distinguish between different items in the claims and do not otherwise indicate or imply any order in time, location or quality. For example, "a first received signal" and "a second received signal" do not indicate or imply that the first received signal occurs in time before the second received signal. Variations and modifications of the embodiments disclosed herein may be made based on the description set forth herein, without departing from the scope of the invention as set forth in the following claims.

What is claimed is:

1. A method for level-shifting a received signal from a first voltage domain to a second voltage domain, the method comprising:

controlling a cross-coupled pair of transistors according to an input signal and a complementary input signal to generate a signal on a pair of complementary nodes, the cross-coupled pair of transistors having a first doping type and the controlling using a pair of transistors having a second doping type, the second doping type being complementary to the first doping type; and

isolating the pair of transistors from the pair of complementary nodes using a pair of isolation transistors and a pair of cascode transistors, the pair of isolation transistors and the pair of cascode transistors being coupled between the pair of transistors and the pair of complementary nodes.

2. The method as recited in claim **1**

wherein pair of transistors comprise low-voltage transistors, and

wherein the cross-coupled pair of transistors, the pair of isolation transistors, and the pair of cascode transistors comprise high-voltage transistors.

3. The method as recited in claim **1**

wherein the pair of transistors are in the first voltage domain, and

wherein the cross-coupled pair of transistors, the pair of cascode transistors, and the pair of isolation transistors are in the second voltage domain.

4. The method as recited in claim **1** wherein the first voltage domain has an input power supply voltage level above an input ground and the second voltage domain has an output power supply voltage level above an output ground,

the output power supply voltage level being greater than the input power supply voltage level.

5. The method as recited in claim **1** wherein the pair of isolation transistors reduce stress on the pair of cascode transistors.

6. The method as recited in claim **1** further comprising:

receiving the input signal in the first voltage domain; and

generating the complementary input signal based on the input signal in the first voltage domain,

wherein the input signal and the complementary input signal have a first voltage swing between an input power supply voltage level and an input ground.

7. The method as recited in claim **6** further comprising:

buffering an intermediate signal on a first node of the pair of complementary nodes in the second voltage domain to generate an output signal,

wherein the output signal has a second voltage swing between an output power supply voltage level and an output ground,

wherein the receiving and generating uses low-voltage transistors, and

wherein the buffering uses high-voltage transistors.

8. The method as recited in claim **1**

wherein the pair of isolation transistors are configured as a pair of cascode transistors with respect to the pair of cascode transistors, thereby reducing stress on the pair of cascode transistors.

9. A level shifter comprising:

a cross-coupled pair of transistors coupled between a first power supply node and a first pair of nodes, the cross-coupled pair of transistors having a first doping type;

a pair of isolation transistors coupled between the first pair of nodes and a second pair of nodes, the pair of isolation transistors having a second doping type, the second doping type being complementary to the first doping type;

a pair of cascode transistors coupled between the second pair of nodes and a third pair of nodes, the pair of cascode transistors having the second doping type; and

a pair of transistors coupled between the third pair of nodes and a second power supply node, the pair of transistors having the second doping type, the pair of transistors being configured to receive an input signal and a complementary input signal.

10. The level shifter as recited in claim **9** further comprising:

an input circuit coupled between the second power supply node and a third power supply node and configured to generate the complementary input signal based on the input signal.

11. The level shifter as recited in claim **10** further comprising:

an output circuit coupled between the first power supply node and a fourth power supply node and configured to generate an output signal on an output node based on a signal on the first pair of nodes.

12. The level shifter as recited in claim **10** wherein the first power supply node is configured to receive an output power supply voltage level above an output ground and the third power supply node is configured to receive an input power supply voltage level above an input ground, the output power supply voltage level being greater than the input power supply voltage level, the second power supply node being coupled to input ground.

13. The level shifter as recited in claim **11**

wherein the input circuit receives the input signal, the input signal having a first voltage swing between an input power supply voltage level on the third power supply node and an input ground on the second power supply node,

wherein the output signal has a second voltage swing between an output power supply voltage level on the first power supply node and an output ground on the fourth power supply node, and

wherein the input power supply voltage level is less than the output power supply voltage level.

14. The level shifter as recited in claim **11**

wherein the pair of transistors and the input circuit comprise low-voltage transistors; and

wherein the output circuit, the cross-coupled pair of transistors, the pair of isolation transistors, and the pair of cascode transistors comprise high-voltage transistors.

15. The level shifter as recited in claim **11**

wherein the input circuit and the pair of transistors are in a first voltage domain, and

wherein the cross-coupled pair of transistors, the pair of isolation transistors, the pair of cascode transistors, and the output circuit are in a second voltage domain.

16. The level shifter as recited in claim **9** wherein the pair of isolation transistors are configured as a pair of cascode transistors with respect to the pair of cascode transistors, thereby reducing stress on the pair of cascode transistors.

17. A level shifter comprising:

a first circuit comprising low-voltage transistors coupled between a pair of complementary nodes and a first ground, the first circuit being responsive to an input signal and a complementary input signal generated in a first voltage domain; and

a second circuit comprising high-voltage transistors coupled between the pair of complementary nodes and an output power supply node and configured to generate complementary signals on the pair of complementary nodes in a second voltage domain.

18. The level shifter as recited in claim **17** further comprising:

an input buffer circuit comprising second low-voltage transistors coupled between an input power supply node and an input ground and configured to generate the complementary input signal based on the input signal generated in the first voltage domain; and

an output circuit comprising second high-voltage transistors coupled between the output power supply node and an output ground and responsive to a signal on a node of the pair of complementary nodes to generate an output signal in the second voltage domain.

19. The level shifter as recited in claim **17** wherein the second circuit comprises:

a cross-coupled pair of transistors coupled between the output power supply node and a second pair of complementary nodes, the cross-coupled pair of transistors having a first doping type;

a pair of isolation transistors coupled between the second pair of complementary nodes and a third pair of complementary nodes, the pair of isolation transistors having a second doping type; and

a pair of cascode transistors coupled between the third pair of complementary nodes and the pair of complementary nodes, the pair of cascode transistors having the second doping type,

wherein the first circuit comprises a pair of transistors coupled between the third pair of complementary nodes and the first ground, the pair of transistors having the second doping type.

20. The level shifter as recited in claim **19** wherein the pair of isolation transistors are configured as a pair of cascode transistors with respect to the pair of cascode transistors, thereby reducing stress on the pair of cascode transistors.

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